Phd Thesis Ms. Tanvika Garg

by Sumit kale

Submission date: 11-Dec-2025 01:09PM (UTC+0530)
Submission ID: 2843240310
File name: Thesis_writing_final.pdf (4.95M)
Word count: 34529
Character count: 192764

DESIGN AND PERFORMANCE IMPROVEMENT OF GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS FOR POWER ELECTRONICS APPLICATIONS

Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

in

Electronics and Communication Engineering

by

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December, 2025

ACKNOWLEDGEMENTS

I am deeply grateful to those who have supported me throughout this journey, making it both meaningful and fulfilling. This dissertation marks not just an achievement but the beginning of a new chapter.

First and foremost, I thank the Almighty for His blessings, strength, and guidance. My heartfelt gratitude goes to my supervisor, **Dr. Sumit Kale**, from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, for his invaluable mentorship, encouragement, and insightful guidance. His patience and belief in my work have been instrumental in my research.

I extend my sincere appreciation to my doctoral committee members for their valuable feedback and to **Prof. Neeta Pandey**, Head of the Department of Electronics and Communication Engineering and **Prof. O. P. Verma**, Former Head of the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, along with the faculty and staff, for their continuous support. I am also thankful to **Delhi Technological University** for providing essential resources and a conducive research environment.

A special thanks to my colleagues and friends — **Dr. Shivani, Mr. Vishal, Dr. Palak, Mr. Rohit, Ms. Aparna, and Ms. Shabana** —for their encouragement and support.

This thesis is dedicated to my parents**, Mr. Ramesh Garg** and **Mrs. Neeta Garg,** and my twin sister, **Ms. Tulika Garg**, whose unwavering love and support have been my greatest strength. Lastly, my sincere gratitude to all friends, mentors, and well-wishers who have contributed to this journey.

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CANDIDATE'S DECLARATION

I, **Tanvika Garg**, hereby certify that the work which is being presented in the thesis entitled **Design and Performance Improvement of Gallium Nitride High Electron Mobility Transistors for Power Electronics Applications** in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the **Department of Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **August 2021** to **June 2025** under the supervision of **Dr. Sumit Kale**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

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CERTIFICATE BY THE SUPERVISOR

Certified that **Tanvika Garg** (Enrollment No.: 2K21/PHDEC/06) has carried out their research work presented in this thesis entitled **"Design and Performance Improvement of Gallium Nitride High Electron Mobility Transistors for Power Electronics Applications"**, for the award of **Doctor of Philosophy** from the Department of Electronics and Communication Engineering, Delhi Technological University, under my guidance and supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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Place: New Delhi
Date:

Dedicated to my Parents and Twin Sister

In appreciation of their

unwavering love, support, and encouragement

DESIGN AND PERFORMANCE IMPROVEMENT OF GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS FOR POWER ELECTRONICS APPLICATIONS

TANVIKA GARG

ABSTRACT

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have emerged as a pivotal technology in power electronics due to their superior material properties, including a wide bandgap, high electron mobility, and excellent thermal stability. Despite their advantages, key challenges such as gate leakage current, breakdown voltage limitations, and high on-resistance hinder their widespread adoption in high-power applications. This thesis systematically presents novel structural and material engineering approaches to optimize GaN HEMTs for high performance in power electronics applications.

In this thesis, we have designed novel device design techniques for GaN HEMT to improve performance by minimizing gate leakage current, reducing on-resistance, and enhancing breakdown voltage. To reduce gate leakage current, we have introduced MIS and p-GaN structures, Gaussian-doped p-GaN HEMT, and Omega (Ω)-shaped gate p-GaN MIS-HEMT. Additionally, we have presented p-GaN HEMTs with an AlInN/AlN/GaN double heterostructure and an InAlGaN back-barrier to improve on-resistance, as well as stepped AlGaN hybrid buffer GaN HEMTs to enhance breakdown voltage. We have also investigated an analytical model to examine the effects of buffer traps on 2DEG density and gate leakage current, particularly at cryogenic temperatures.

To suppress gate leakage current, an enhancement-mode GaN HEMT with an MIS and p-GaN structure has been designed. By integrating a high-k HfO_2 dielectric layer, this device reduces tunneling effects and improves the threshold voltage while maintaining high drain current performance. In addition, we have introduced a Gaussian-doped p-GaN that incorporates a controlled doping profile in the GaN channel to minimize electric field variations. This approach significantly reduces gate leakage current while improving transconductance and current drive capability. Furthermore, an Omega (Ω)-shaped gate has been introduced in p-

GaN MIS-HEMT, demonstrating a significant reduction of gate leakage, enhanced breakdown voltage, and improved reliability. This is achieved through optimized dielectric stress distribution.

The on-resistance has been reduced by implementing a p-GaN HEMT with an AlInN/AlN/GaN double heterostructure and an InAlGaN back-barrier. The AlInN/GaN interface increases 2DEG density, improving current handling, while the InAlGaN back-barrier confines electrons, enhancing efficiency.

Breakdown voltage and BFOM are enhanced by integrating a stepped AlGaN hybrid buffer into the p-GaN HEMT. The optimized lower aluminum concentration reduces surface defects, improves breakdown voltage, and decreases leakage current. The design outperforms conventional HB-HEMTs with higher breakdown voltage, improved BFOM, enhanced transconductance, and lower small-signal capacitances.

We have developed an analytical model to examine buffer trap effects and cryogenic temperature on 2DEG density and gate leakage in p-GaN HEMT. It incorporates thermionic emission, Poole-Frenkel emission, and thermally-assisted tunneling to describe leakage mechanisms and analyzes buffer trap influence on Schottky barrier potential drop and electric field distribution. The findings offer key insights for optimizing device structures to suppress leakage current.

The proposed device architectures have been extensively validated using numerical simulations, ensuring their feasibility for real-world power electronics applications. The findings of this thesis contribute to the ongoing evolution of GaN HEMT technology, providing a strong foundation for future research in high-efficiency, high-reliability power semiconductor devices.

LIST OF PUBLICATIONS

SCIE/SCI Indexed Journals

1. **T. Garg** and S. Kale, "Optimization of structural parameters in Omega(Ω) Shaped gate p-GaN MIS-HEMT for performance improvement", **Micro and Nanostructures**, vol. 188, Feb. 2024, doi: 10.1016/j.micrna.2024.207793.
2. **T. Garg** and S. Kale, "A novel p-GaN HEMT with AlInN/AlN/GaN double heterostructure and InAlGaN back-barrier," **Microelectronics Reliability**, vol. 145, 2023, doi: 10.1016/j.microrel.2023.114998.
3. **T. Garg** and S. Kale, "A novel stepped AlGaN hybrid buffer GaN HEMT for power electronics applications," **Microelectronics Reliability**, vol. 149, 2023, doi: 10.1016/j.microrel. 2023.115232.
4. **T. Garg** and S. Kale "Analytical Modeling of Buffer Trap Effects on 2DEG Density and Gate Leakage Current in p-GaN HEMT at Cryogenic Temperatures," **Micro and Nanostructures** (Revision Submitted)

International Journal

1. **T. Garg** and S. Kale, "Recent Developments, Reliability Issues, Challenges and Applications of GaN HEMT Technology," in **IEEE Electron Devices Reviews**, vol. 1, no. 1, pp. 16-30, Oct. 2024, doi: 10.1109/EDR.2024.3491716.

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Patent

1. **Tanvika Garg et al.**, "A Novel Dual-k Double-Sided Dielectric p-GaN MISHEMT for Power Electronics Application" (Patent Published)

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LIST OF ABBREVIATIONS

2DEG	2-Dimensional Electron Gas
2DHG	2-Dimensional Hole Gas
AC	Alternating Current
AI	Artificial Intelligence
Al	Aluminium
Al_2O_3	Aluminium Oxide
AlGaN	Aluminium Gallium Nitride
AlInN	Aluminium Indium Nitride
AlN	Aluminium Nitride
ASM	Advanced Spice Model
Au	Gold
BD	Built-in Diode
BFOM	Baliga Figure of Merit
CMOS	Complementary Metal Oxide Semiconductor
D2DEG	Dual 2-Dimensional Electron Gas
DC	Direct Current
D-FP	Drain Field Plate
EMI	Electro-Magnetic Interference
E-mode	Enhancement mode
EVs	Electric Vehicles
Fe	Iron
F-graphene	Fluorinated Graphene
GaON	Gallium Oxynitride
Ga_2O_3	Gallium Oxide
GaO_xN_{1-x}	Gallium Oxynitride
GaN	Gallium Nitride
GD-HEMT	Gaussian Doped High Electron Mobility Transistor
GGFP	Grated Gate Field Plate
GTE	Gate Termination Extension
GW	GigaWatt
HB-HEMT	Hybrid Buffer High Electron Mobility Transistor

HEMT	High Electron Mobility Transistor
HEVs	Hybrid Electric Vehicles
HfO_2	Hafnium Oxide
ICP-RIE	Inductively Coupled Plasma Reactive Ion Etching
InAlGaN	Indium Aluminium Gallium Nitride
IO-pGaN	Island Ohmic p-type Gallium Nitride
IoT	Internet of Things
I-graphene	Intrinsic Graphene
IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide
$LaLuO_3$	Lanthanum Lutetium Oxide
Mg	Magnesium
MG-HEMT	Metal Insulator Semiconductor and p-type Gallium Nitride High Electron Mobility Transistor
MODFET	Modulation-Doped Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOCVD	Metal-Organic Chemical Vapor Deposition
MIS	Metal Insulator Semiconductor
MIS-HEMT	Metal Insulator Semiconductor High Electron Mobility Transistor
NCD	Nanocrystalline Diamond Gated
Ni	Nickel
n-GaN	n-type Gallium Nitride
p-AlGaN	p-type Aluminium Gallium Nitride
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PFE	Poole-Frenkel Emission
p-GaN	p-type Gallium Nitride
PSAG	p-type Gallium Nitride Stripe Array Gate
RF	Radio Frequency
Si	Silicon
SiC	Silicon Carbide
SiN	Silicon Nitride

SOI	Silicon on Insulator
SnO_2	Tin Oxide
SRH	Shockley-Read-Hall
STEPHB-HEMT	Stepped Hybrid Buffer High Electron Mobility Transistor
SuFP	Super Field Plate
TaN	Tantalum Nitride
TAT	Thermally Assisted Tunneling
TCE	Trichloroethylene
TE	Thermionic Emission
TUG	Thin Upward Graded
UCCM	Unified Charge Control Model
WBG	Wide Band Gap

LIST OF SYMBOLS

ΔV_{AlGaN}	Potential Drop
σ_{AlGaN}	Sheet Charge Density
n_s	Sheet Density of 2DEG
q	Electron Charge
ε	Dielectric constant
ϕ_b	Surface Barrier Height
E_f	Fermi Level Position
ΔE_C	Conduction Band Discontinuity
f_{max}	Cutoff Frequency
V_{ds}	Drain-to-Source Voltage
R_{ON}	ON-Resistance
THz	Terahertz
V_{th}	Threshold Voltage
$R_{on,sp}$	Specific ON-Resistance
V_G	Gate Voltage
μ	micro
V_{GS}	Gate-to-Source Voltage
°C	Degree Celsius
I_g	Gate Current
I_d	Drain Current
V_d	Drain Voltage
$I_{ds,max}$	Maximum Drain Current
g_m	Transconductance
MHz	Megahertz
C_{gs}	Gate-to-Source Capacitance
C_{gd}	Gate-to-Drain Capacitance
C_{ds}	Drain-to-Source Capacitance
E_t	Trap Energy Level
E_C	Conduction Band Edge
n_{trap}	Trap Electron Density
E_T	Trap Activation Energy

N_T	Trap Concentration
β-$(Al_xGa_{1-x})_2O_3$	Beta-Aluminium Gallium Oxide
Ω-shaped	Omega-shaped

CHAPTER 1

INTRODUCTION

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have attracted considerable interest in recent years owing to their outstanding material characteristics, which make them ideal for high power applications [1]. These transistors utilize a heterostructure composed of GaN and AlGaN layers, enabling the creation of a two-dimensional electron gas (2DEG) at their interface, which provides high electron mobility and excellent electrical performance [2]. This high electron mobility significantly reduces resistance, thereby minimizing conduction losses and enabling faster switching speeds compared to conventional semiconductor technologies. As a result, GaN HEMTs offer advantages such as higher power density, and improved efficiency, making them an excellent choice for power electronics where power handling capabilities are essential [3], [4]. Additionally, GaN HEMTs exhibit superior thermal and voltage endurance, allowing them to function effectively in extreme environments, including high-temperature and high-power conditions [5], [6]. Their robustness and ability to maintain efficiency under harsh operating conditions further enhance their suitability for advanced power conversion, and aerospace applications. The continued development of GaN-based power devices has led to innovations in energy-efficient systems. Figure 1.1 depicts the diverse range of applications for GaN HEMT across various voltage levels, highlighting their significance in modern semiconductor technology [7], [8]. Over the years, significant research efforts on GaN HEMTs have resulted in notable advancements in their efficiency, reliability, and overall performance. However, despite these improvements, their widespread commercialization remains hindered by a critical challenge—their inherently normally-on operation, which raises concerns related to safety and cost-effectiveness. To enhance fail-safe functionality, improve system reliability, and simplify circuit design, achieving normally-off

operation has become a crucial objective in GaN power electronics. Various techniques have been explored to address this issue, including fluoride plasma treatment, gate recessing, and the incorporation of p-GaN gate structures. Among these methods, the integration of p-GaN gates has emerged as the most practical and commercially viable approach, offering an optimal balance between performance and reliability. This technique involves modifying the epitaxial structure to control the polarization-induced 2DEG. This approach not only ensures enhanced device safety but also facilitates seamless integration into power electronics applications, making GaN HEMTs a promising solution for next-generation power semiconductor technologies.

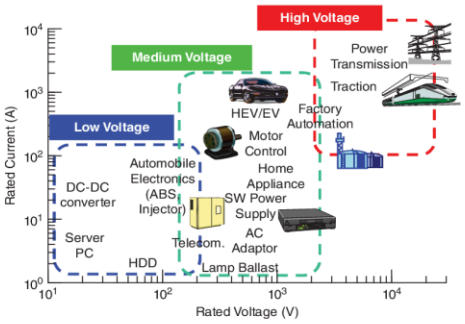

Fig. 1.1: GaN HEMT applications by voltage range: Low Voltage (10 V–100 V) – Consumer Electronics and Automotive; Medium Voltage (100 V–1000 V) – Electric Vehicles, Industrial and Telecom; High Voltage (1000 V–10,000 V)– Power Transmission, Rail and Automation.

1.1 Motivation

The increasing demand for energy-efficient power electronics across various sectors—including renewable energy, electric vehicles, data centers, and advanced industrial systems—has highlighted the need for next-generation semiconductor technologies. Although silicon-based power devices are well-established and commonly used, they are constrained by limitations in efficiency, thermal tolerance,

and voltage capability, making them less suitable for meeting the stringent requirements of modern power applications. In contrast, GaN HEMTs have emerged as a promising alternative due to their superior properties, including a wider bandgap, enhanced breakdown voltage, increased electron mobility, and excellent thermal management. These advantages make GaN HEMTs a pivotal technology for future power electronics, enabling greater efficiency, higher switching speeds, and more compact and lightweight system designs compared to silicon devices. Despite their potential, the adoption of GaN HEMT in high power electronics is still limited by several challenges, including issues related to device design, thermal management, material quality, and cost-effective fabrication techniques. Addressing these challenges requires a deeper understanding of the physical phenomena governing device operation, as well as innovative design approaches and simulation frameworks that can accurately predict device behavior under high power conditions. Additionally, optimizing GaN HEMTs for various power electronics applications demands a thorough investigation of their performance metrics under real-world operating conditions. These research efforts are critical for bridging the gap between the theoretical advantages of GaN HEMTs and their practical implementation in power systems. This research is motivated by the opportunity to contribute to the advancement of GaN HEMT technology through comprehensive design and simulation studies. The outcomes of this research aim to advance the design and simulation of GaN HEMT, enhancing its performance and reliability for power electronics applications. This research has significant potential in contributing to more efficient and sustainable energy systems, supporting global efforts to improve energy utilization and reduce environmental impact.

1.2 Objectives

The primary aim of this research is to design and simulate GaN HEMTs tailored for power electronics applications. Given the increasing demand for efficient and reliable power devices, this study focuses on addressing key performance challenges associated with GaN HEMTs, such as breakdown voltage, ON-resistance, and gate leakage. Through comprehensive design and simulation efforts, this research seeks to

develop optimized GaN HEMT structures that can offer enhanced performance, contributing to the advancement of power electronics. The specific objectives outlined in this study aim to tackle these challenges systematically, ultimately improving the efficiency of GaN HEMTs for high power applications. Objectives are listed as below:

1. Improvement of the reliability of GaN HEMT by reducing gate leakage.
2. Reduction and optimization of the on-resistance of GaN HEMT for improved performance.
3. Enhancement of the breakdown voltage of GaN HEMT to withstand high voltages.
4. Development of an analytical model for gate leakage optimization of GaN HEMT structure.

1.3 Thesis organization

The thesis comprises seven chapters, which are organized as follows:

Chapter 1: Introduction This chapter presents an overview of GaN HEMTs, discussing their properties, applications, and key challenges. The motivation behind the research and its significance in power electronics applications are elaborated. The chapter also outlines the objectives of the research and provides a brief description of the adopted methodologies.

Chapter 2: Literature Review This chapter provides a comprehensive review of existing GaN HEMT technologies, focusing on advancements in device architectures, buffer layer optimizations, and gate engineering techniques. Key performance metrics such as gate leakage current, on-resistance, and breakdown voltage, are analyzed. Various approaches, including p-GaN gate technology and dielectric engineering, are reviewed to highlight their impact on improving device performance.

Chapter 3: Optimization and Suppression of Gate Leakage Current This chapter focuses on structural and material engineering approaches to suppress gate leakage current and enhance device reliability. Three advanced device architectures are proposed and analyzed:

- **An enhancement-mode GaN HEMT integrating an MIS and p-GaN structure**, which employs a high-k HfO_2 dielectric layer to suppress tunneling effects, improve threshold voltage stability, and enhance current handling capabilities.
- **A Gaussian-doped p-GaN HEMT**, which utilizes a controlled doping profile in the GaN channel to minimize electric field variations, leading to a 27% reduction in gate leakage current, a 7% improvement in maximum drain current, and a 67% enhancement in transconductance.
- **An Omega (Ω)-shaped gate p-GaN MIS-HEMT**, which reduces gate leakage through optimized dielectric stress distribution, achieving a 14% reduction in gate leakage and a 20% increase in maximum drain current.

Extensive numerical simulations are performed to validate the proposed designs, ensuring their feasibility for power applications. The chapter provides an in-depth analysis of electric field distribution, tunneling suppression, and doping optimization strategies to improve device performance.

Chapter 4: A p-GaN HEMT with AlInN/AlN/GaN Double Heterostructure and InAlGaN Back-Barrier

This chapter investigates strategies for reducing on-resistance to enhance current drive capability in GaN HEMTs. A novel p-GaN HEMT design featuring an AlInN/AlN/GaN double heterostructure and an InAlGaN back-barrier is proposed. The simulation results indicate significant improvements in R_{ON} and maximum drain current, with a reduction of 85% in R_{ON} and an increase of 231% in drain current compared to conventional designs. The chapter also examines the impact of these optimizations on power loss reduction.

Chapter 5: A Stepped AlGaN Hybrid Buffer GaN HEMT

To address the challenge of low breakdown voltage in GaN HEMTs, this chapter explores novel device architectures incorporating a stepped hybrid AlGaN buffer layer. The impact of step thickness and electric field distribution on breakdown voltage improvement is analyzed. Simulation results demonstrating a 20% enhancement in breakdown voltage are presented, along with a discussion on Baliga's Figure of Merit (BFOM) improvements.

Chapter 6: Analytical Modeling of Buffer Trap Effects on 2DEG Density and Gate Leakage Current at Cryogenic Temperature

This chapter presents a physics-based analytical model to examine buffer trap effects on p-GaN HEMTs at cryogenic temperatures. Incorporating key trap parameters and solving the Schrödinger-Poisson equations, the model evaluates 2DEG density and gate leakage mechanisms. A comparison with experimental data confirms its accuracy, showing a 33% increase in 2DEG density and a 99% reduction in gate leakage. These findings highlight the model's potential for optimizing p-GaN HEMTs in cryogenic power applications.

Chapter 7: Conclusion, Future Scope, and Social Impact

This chapter summarizes the key findings of the research, emphasizing the advancements achieved in GaN HEMT technology for power electronics applications. Potential future research directions, including further optimizations in gate engineering, buffer layer modifications, and experimental refinements, are discussed. The chapter also highlights the broader impact of the research in advancing high-efficiency and high-reliability power semiconductor devices, contributing to sustainable energy solutions.

1.4 References

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CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

The evolution of semiconductor technology has witnessed a paradigm shift with the emergence of GaN HEMTs, a promising solution to the limitations of traditional silicon-based devices. This chapter delves into a comprehensive literature review of GaN HEMTs, addressing their working principles, material properties, and technological advancements. Beginning with an overview of wide bandgap semiconductors and the role of GaN, the discussion progresses through the fundamental principles underlying the device's operation, particularly the critical role of polarization effects and 2DEG formation. The review further explores early milestones in GaN HEMT development, followed by recent innovations tailored for high-power applications, such as p-GaN HEMTs, MIS-HEMTs, and advancements in device engineering.

This review also comprehensively highlights the critical performance metrics that dictate the operational efficiency and reliability of GaN HEMTs, particularly emphasizing gate leakage current, on-resistance, and breakdown voltage. These parameters serve as fundamental indicators for assessing the suitability of GaN HEMTs in power applications. The breakdown voltage determines the device’s capacity to tolerate high electric fields without failure, while the on-resistance influences conduction losses and directly impacts power efficiency. On the other hand, gate leakage current is crucial for evaluating device robustness, particularly under high-voltage and high-temperature stress conditions.

To facilitate a systematic understanding, the review presents a detailed comparative analysis of recent advancements in GaN HEMT technologies through structured tabular summaries. These tables consolidate key findings from contemporary

literature, allowing for a clear evaluation of how various device architectures and fabrication techniques have influenced performance improvements.

2.2 Types of GaN HEMT Technology

2.2.1 GaN HEMT Technology based on Orientation

2.2.1.1 A Lateral GaN HEMT Technology

A lateral GaN HEMT uses the wide-bandgap semiconductor material GaN, as the channel material [8], [9]. The lateral structure of the device means that the current flows in a horizontal direction along the surface of the semiconductor material. The basic structure of a lateral GaN HEMT is depicted in Fig. 2.1.

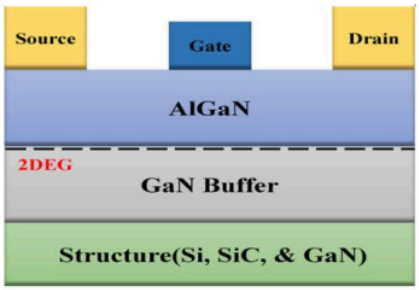

Fig. 2.1: Schematic of Lateral GaN HEMT

A gate electrode is placed between the drain and source regions. When the gate voltage is applied, an electric field is formed, which controls the electrons flowing in the channel. The high electron mobility in the channel results in high current density and high switching speeds.

2.2.1.2 A Vertical GaN HEMT Technology

A vertical GaN HEMT utilizes a vertical current flow path. The device typically consists of a thin layer of GaN semiconductor material grown on a substrate, with a metal contact layer on top of the GaN layer. A gate electrode separated from the GaN layer by a dielectric layer is presented in Fig. 2.2. In a vertical GaN HEMT, the current flows from top to down. The vertical structure of the device provides several

advantages over lateral GaN HEMTs [9]. For example, it allows for a larger active area and lower on-resistance, as the current flows through the entire thickness of the GaN layer.

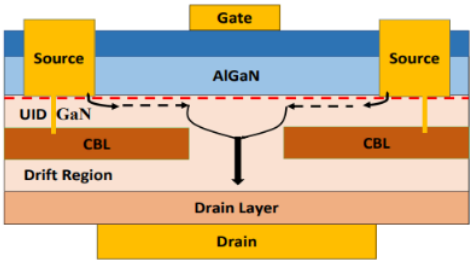

Fig. 2.2: Schematic of Vertical GaN HEMT

2.2.2 GaN HEMT Technology Based on Mode of Operation

2.2.2.1 Normally-on

A Normally-On GaN HEMT is engineered to remain in the ON state even when no gate bias is applied. This behavior is enabled by a specific structure that includes an AlGaN/GaN heterojunction, as illustrated in Fig. 2.3. The heterojunction is central to the device's functionality [10], as it gives rise to a 2DEG channel at the channel interface. This 2DEG channel enables efficient current conduction. The AlGaN with a wider bandgap than GaN serves as a barrier that confines electrons within the 2DEG and prevents their diffusion into the depletion region. As a result, the device conducts without needing an external gate voltage. Normally-On GaN HEMTs exhibit key performance benefits, including low on-resistance, high drain current capability, fast switching, and high breakdown voltage. These advantages make them suitable for power electronics applications where default conduction is beneficial, such as in power supplies, inverters, and motor control systems.

2.2.2.2 Normally-off

A normally-off GaN HEMT is specifically designed to remain in the OFF state when no gate bias is applied. These transistors are known for their higher breakdown

voltage, lower leakage current, and rapid switching capabilities, making them ideal for applications in power electronics where default-off behavior is preferred. Various techniques have been developed to achieve normally-off behavior in GaN HEMTs [11], [12], including (a) the cascode configuration, (b) employing thin or ultra-thin barrier layers combined with fluorine ion implantation, (c) utilizing a p-GaN gate structure (as illustrated in Fig. 2.4), and (d) implementing a recessed gate design.

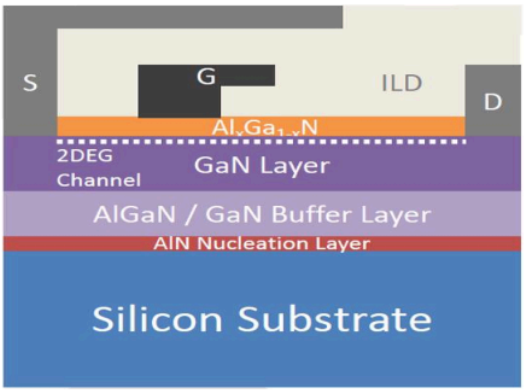

Fig. 2.3: Schematic of Depletion mode GaN HEMT

In the cascode approach, a series connection of transistors is used, where one device modulates the gate voltage of the other. Typically, a normally-on GaN HEMT operates in saturation with increased drain-source and gate-source voltages, which in turn controls the switching behavior of an additional MOSFET in the configuration. This setup effectively enables normally-off functionality.

Another method involves fluorine implantation in conjunction with thin or ultra-thin barrier layers. This technique introduces fluorine atoms at the gate-channel interface, which lowers the barrier height and decreases the electron concentration in the channel. As a result, the device becomes easier to turn off, achieving the desired normally-off operation.In a GaN HEMT featuring a p-GaN gate, the gate region is doped with acceptor elements such as magnesium (Mg), creating a depletion zone at

the gate-channel interface. This depletion region modulates the 2DEG, enabling effective control of the channel current. In contrast, a GaN HEMT incorporating a recessed gate involves etching the gate electrode into the device surface, forming a trench within the GaN layer. This recessed structure reduces the gate length and increases the electric field across the gate, leading to improved switching speed and enhanced breakdown voltage.

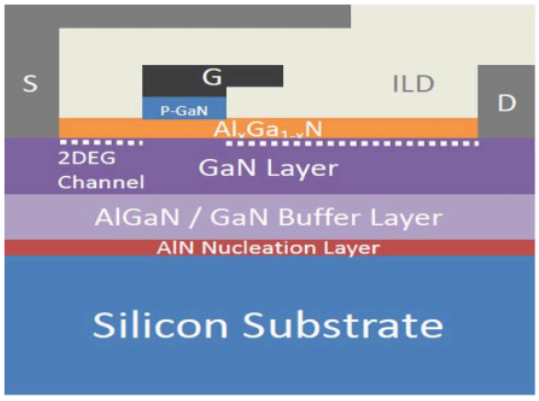

Fig. 2.4: Schematic of Enhancement mode GaN HEMT

2.3 Working Principle of GaN HEMT

2.3.1 Wide Bandgap Compound Semiconductor: GaN

Due to the limitations in performance of silicon-based devices and the increasing demand for advanced capabilities, alternative semiconductor materials are being explored for next-generation electronics. WBG semiconductors such as GaN, SiC and β-Ga_2O_3, have emerged as strong candidates due to their outstanding electrical characteristics [1]–[4]. Unlike silicon, which has a relatively narrow bandgap, WBG materials provide improved performance, including higher breakdown voltage, greater efficiency, enhanced reliability, and better thermal management. GaN, for example, has a bandgap two to four times greater than silicon, resulting in transistors with reduced leakage currents and increased stability under elevated temperatures.

Additionally, WBG materials exhibit superior thermal conductivity, reduced power dissipation, and substrate leakage, which make them advantageous for applications like high-power amplifiers [5], [6].

2.3.2 Crystal Structure and Polarization of GaN

GaN is a wide-bandgap semiconductor crystallizing in the hexagonal wurtzite form. Its lattice comprises two interleaved face-centered hexagonal sublattices stacked vertically to produce the three-dimensional crystal [7]. The wurtzite unit cell consists of two overlapping tetrahedra, each containing four gallium and four nitrogen atoms. Due to the asymmetric atomic arrangement, the wurtzite lattice exhibits polarity along the axis perpendicular to the hexagonal planes, commonly referred to as the c-axis. This intrinsic polarization arises from the electronegativity difference between Ga and N atoms, yielding a dipole moment along the c-axis.

The operation of a GaN HEMT relies fundamentally on the GaN/AlGaN heterojunction and the polarization phenomena present at that interface. These piezoelectric and spontaneous polarization effects are pivotal for forming the 2DEG, which underpins the device's superior electron mobility and overall performance. In a standard GaN HEMT architecture, the epitaxial growth of AlGaN atop GaN, establishing a heterointerface. Due to the different lattice constants and material properties of GaN and AlGaN, large polarization fields develop at this junction.

Two distinct polarization contributions govern the heterojunction behavior: piezoelectric polarization and spontaneous polarization. Spontaneous polarization is inherent to materials lacking centrosymmetry—such as GaN and AlGaN—and manifests as a built-in dipole moment even in the absence of external stress. While both layers possess this intrinsic polarization, it is generally more pronounced in AlGaN due to its higher aluminum fraction. Piezoelectric polarization emerges when the AlGaN layer is strained by the mismatched lattice of the GaN. Depending on the Al composition, the AlGaN film experiences either tensile or compressive strain when grown on GaN, inducing an additional polarization component. The superposition of spontaneous and piezoelectric polarizations generates a strong

electric field at the heterointerface. This field causes band bending, forming a quantum well where electrons from the AlGaN layer are drawn into and confined, giving rise to the 2DEG. Because these electrons reside in a potential well spatially separated from ionized donors, scattering is reduced, enabling exceptionally high mobility [8].

2.3.3 The Formation and Calculation of the 2DEG Density

2.3.3.1 Formation of the 2DEG in AlGaN/GaN heterostructure

The AlGaN layer induces polarization charges, resulting in positive charges at the AlGaN/GaN interface and negative charges on the AlGaN surface. This polarization creates an internal electric field within the AlGaN layer, which in turn affects the energy band profile and shifts the Fermi level toward the AlGaN/GaN interface. This effect is similar to applying an external voltage across a thin, isolated AlGaN layer, resembling a planar capacitor with the AlGaN acting as the dielectric, as illustrated in Fig. 2.5. The electric field present in the AlGaN layer, along with its n-type doping, causes conduction electrons to move toward the positively charged region, resulting in electron accumulation. This accumulation generates positive space charges within the AlGaN, leading to band bending. As this process continues, the Fermi level eventually reaches a stable, flat state. The inherent electric field in the AlGaN is neutralized by the opposing built-in field, which flattens the previously tilted energy band. Since GaN has a lower Fermi level compared to AlGaN (as shown on the left side of Fig. 2.6), electrons flow from the AlGaN into the GaN when the two materials are brought into contact, forming a two-dimensional electron gas (2DEG). This electron transfer proceeds until the Fermi levels in both AlGaN and GaN align, achieving equilibrium, as illustrated on the right side of Fig. 2.6 [9].

2.3.3.2 Calculation of the 2DEG density in AlGaN/GaN heterostructure

Figure 2.7 depicts the charge distribution in an AlGaN/GaN heterostructure, revealing the formation of three distinct dipoles. The first dipole, $\pm\sigma_{AlGaN}$, results from polarization charges within the AlGaN layer, while the second, $\pm\sigma_{GaN}$, is due to

polarization effects in the GaN layer. The third dipole, linked to the two-dimensional electron gas (2DEG), corresponds to the ionized surface charge $\pm\sigma_S$. These dipoles are modeled as planar plate capacitors labeled C_1, C_2, and C_3. Although these capacitors do not influence electrons beyond their internal boundaries, they sustain a finite electric field between their parallel plates. The magnitude of this electric field is determined by the equation $E = \sigma/\varepsilon$, where σ is the surface charge density on the opposing plates and ε is the dielectric constant of the material separating them. In areas where multiple pairs of charged planes overlap, the resulting electric field is determined by the algebraic sum of their charges. As a result, the electric field intensity within the AlGaN layer is influenced by the contributions of charges from C_1 and C_2, which correspond to the polarization-induced charges in the AlGaN layer and the charge associated with the 2DEG, respectively.

$$\frac{\Delta V_{AlGaN}}{d} = \frac{\sigma_{AlGaN}}{\epsilon} - \frac{qn_s}{\epsilon} \tag{2.1}$$

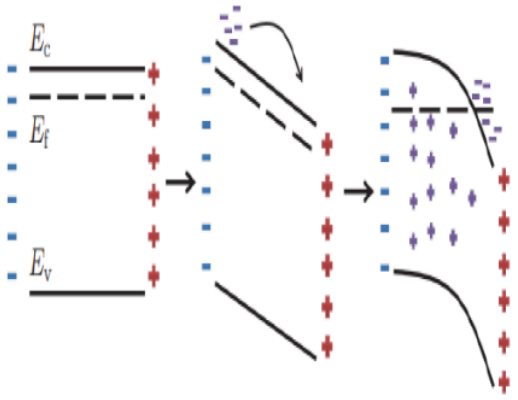

Fig. 2.5: Considering an n-doped AlGaN film freestanding but strained equivalently to an AlGaN/GaN heterostructure, the polarization field causes electrons to traverse from one side to the other. Consequently, the energy bands bend and fixed positive charges accumulate in the AlGaN layer [9].

where ΔV_{AlGaN} is the potential drop across the conductive band of the AlGaN surface and the AlGaN/GaN interface as shown in Fig. 2.8, d is the thickness of the AlGaN

layer, σ_{AlGaN} is the sheet charge density that is induced by AlGaN polarization, n_s is the sheet density of 2DEG, q is the electron charge, and ϵ is the dielectric constant of AlGaN. The potential drop ΔV_{AlGaN} can be expressed as

$$q\Delta V_{AlGaN}=q\square_b + E_f - \Delta E_C \tag{2.2}$$

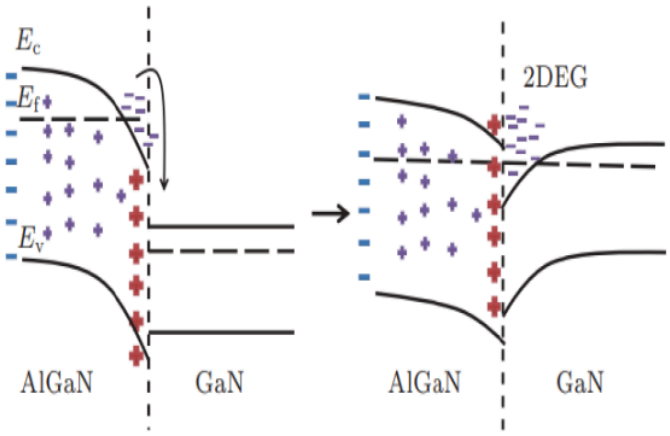

Fig. 2.6: Energy-band diagram of an n-doped AlGaN/GaN heterostructure. Upon contact, electrons transfer into the GaN side, accumulate at the interface, and form a 2DEG [9].

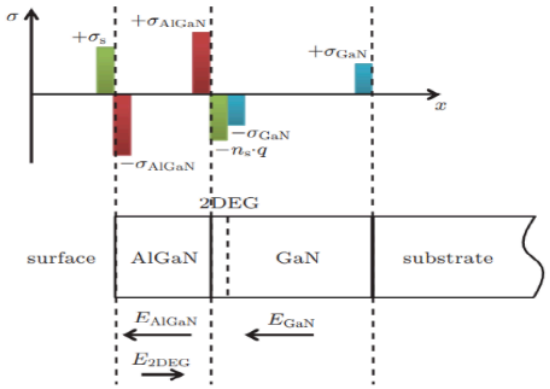

Fig. 2.7: Charge distribution profile of an AlGaN/GaN heterostructure [9].

where ϕ_b is the surface barrier height, E_f is the Fermi level position with respect to the GaN conduction-band edge at the AlGaN/GaN interface, and ΔE_C is the conduction band discontinuity between GaN and AlGaN as shown in Fig. 2.8. Therefore, based on Eqs. (2.1) and (2.2), the sheet density of 2DEG can be expressed as [9].

$$n_s = \frac{\sigma_{AlGaN}}{q} - \left(\frac{\epsilon}{q^2 d}\right)\left(q\phi_b + E_f - \Delta E_C\right) \tag{2.3}$$

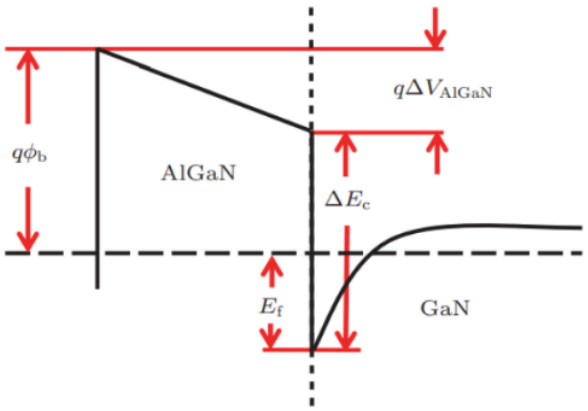

Fig. 2.8: Conductive band diagram of an AlGaN/GaN heterostructure [9].

2.4 Early Advancements in GaN HEMT Technology

The emergence of GaN HEMT technology in the early 1990s marked a revolutionary step forward in semiconductor advancements. In 1993, M. Asif Khan and his team introduced the n-GaN/AlGaN heterojunction HEMT, showcasing remarkable characteristics such as a 28 mS/mm transconductance at 300 K and 46 mS/mm at 77 K [10]. In 1994, they presented a GaN HFET with a 0.25 μm gate length, achieving a cut-off frequency of 11 GHz and an oscillation frequency of 35 GHz. The exceptionally high fmax was attributed to the low parasitic output conductance in the saturation regime, establishing its suitability for millimeter-wave and microwave applications [11]. In 1996, Y.F. Wu et al. developed GaN HFETs and MODFETs, achieving significant channel current densities and high power outputs. The

MODFET demonstrated a channel current density exceeding 300 mA/mm and exhibited excellent large voltage I-V characteristics up to V_{ds} = 60V, enabling a FWS class A amplifier power output exceeding 2 W/mm [12]. Further progress was made in 1999 when Lester F. Eastman demonstrated enhanced GaN HFETs grown on p-type SiC substrates, which outperformed sapphire substrates [13]. His work achieved a power-added efficiency of 78% on SiC compared to 50% on sapphire.

In 2001, Karmalkar and colleagues proposed a systematic approach for optimizing field plate device designs to enhance performance while minimizing the impact on on-resistance and frequency response. They identified increasing the insulator's dielectric constant beneath the field plate as a promising technique to enhance device performance [14]. Saito et al., in 2006, introduced a recessed gate structure for GaN HEMTs, allowing for gate threshold voltage adjustment without increasing on-resistance. This was accomplished by the selective reduction of the 2DEG density under the gate [15]. Two years later, Wong et al. demonstrated an N-face MIS-HEMT with excellent DC and RF characteristics at specific optical gate lengths. Using AlN for electron confinement eliminated alloy scattering and provided a robust back-barrier mechanism, addressing short-channel effects in highly scaled sub-micrometer devices [16].

In 2011, Hilton et al. reported normally-off GaN HEMT tailored for power electronics application by employing p-GaN gate alongside a GaN buffer doped with carbon. The addition of an AlGaN back-barrier in conjunction with the buffer effectively suppressed early off-state punch-through, yielding low R_{ON} and a robust V_{th} of 1.1 V for dependable switching. These devices demonstrated a breakdown capability of 1000 V with a gate drain spacing of 6 μm [17]. Such achievements represented pivotal steps in advancing GaN HEMT technology and catalyzed further R&D efforts to push its performance limits.

2.5 GaN HEMTs for High-Power Applications

Recent developments on GaN HEMTs highlight their strong potential for high-power applications, driven by GaN's superior material properties like wide bandgap, high

breakdown field, and thermal stability. Research increasingly aims at device innovations that enhance power density, efficiency, and reliability, critical for high-power performance in challenging environments. Key developments include p-GaN gate engineering, GaN MIS-HEMTs, field-plated GaN HEMTs, Fluorine implanted GaN HEMTs, and gate-recessed GaN HEMTs to mitigate issues such as premature device failure in power electronics applications.

2.5.1 p-GaN HEMTs

The p-GaN HEMT has emerged as a promising device for power electronics applications, leveraging GaN's inherent qualities such as its wide bandgap, high electron mobility, and robust breakdown characteristics. Unlike conventional GaN HEMTs, p-GaN HEMTs employ a p-GaN layer under the gate to deplete the underlying 2DEG at the zero gate voltage. This configuration allows for normally-off behavior, a desirable feature in power electronics for safety and energy efficiency.

2.5.1.1 Gate Engineered p-GaN HEMTs

Recent advancements in gate engineering have significantly enhanced the performance of p-GaN HEMTs by modifying the gate region to improve the control over the 2DEG density and reduce gate leakage currents. Techniques such as incorporating dielectric layers, varying gate lengths, and adjusting the p-GaN cap layer thickness have been explored to improve device reliability, minimize power losses, and ensure stability under high-stress conditions. For instance, the integration of fluorinated and intrinsic graphene as gate insertion layer in p-GaN HEMT has demonstrated improvements in device performance, including better ON/OFF current ratios, increased threshold voltage, and reduced gate leakage, while also enhancing thermal stability due to an improved Schottky barrier height and interface quality [18]. Similarly, the use of indium–tin–oxide gate electrodes in p-GaN HEMT has shown superior gate stability under forward bias, coupled with improvements in current handling and transconductance compared to conventional Schottky gate materials [19]. To address surface damage caused by selective etching, the introduction of a p-AlGaN layer between the p-GaN and AlGaN layers has proven

effective in minimizing plasma damage through low-damage etching processes, resulting in enhanced threshold voltage stability and reduced ON-resistance [20]. Additionally, the adoption of a fin-gate structure with tri-gates and fin trenches extending into the gate-to-drain region has significantly improved on-state resistance, saturation current, and threshold voltage stability by effectively managing carrier traps [21]. These advancements in gate engineering techniques highlight their potential in overcoming challenges such as gate leakage suppression, surface damage reduction, and threshold voltage stability.

2.5.1.2 Buffer Engineered p-GaN HEMTs

The performance of p-GaN HEMT is heavily influenced by the properties of the buffer layer, which plays a crucial role in determining device characteristics such as V_{th}, R_{ON}, and reliability. Buffer engineering, involving modifications in composition, thickness, and doping of the buffer, has been extensively studied to address challenges such as charge trapping, dislocation density, and strain, all of which can impact device performance. Hybrid buffer structures with varied aluminum compositions have been proposed to enhance breakdown voltage and the power figure of merit, offering improved switching characteristics over conventional designs [22]. Stepped hybrid buffer layers have been explored to optimize electric field distribution near the gate-drain interface, thereby significantly enhancing the breakdown voltage [23]. However, efficient methods to boost breakdown voltage while minimizing buffer leakage current without compromising specific on-resistance are still needed. Investigations into β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ buffer layers with a p-GaN gate have highlighted the critical impact of doping concentration, buffer thickness, and gate-drain distance on both ON-state and OFF-state performance, revealing the trade-offs between breakdown voltage and the power figure of merit [24].

2.5.1.3 Passivation Engineered p-GaN HEMTs

Passivation engineering has emerged as a critical approach to addressing challenges in p-GaN HEMTs, including gate leakage, threshold voltage instability, and surface

charge effects, which impact long-term device stability and performance. Advanced passivation strategies, such as dielectric passivation layers, surface treatments, and multi-layered passivation stacks, have demonstrated significant improvements in minimizing surface traps, stabilizing threshold voltage, and enhancing device reliability. Active-passivation techniques, involving mechanisms like mobile hole screening and hole emission, have been employed to mitigate dynamic ON-resistance degradation by clearing surface and buffer traps. These methods have further evolved to incorporate metal/insulator structures to expand gate drive margins, enabling enhanced threshold stability and improved ON-resistance under varying operational conditions [25]. Additionally, active-passivation designs with thinned p-GaN layers and virtual body structures have been introduced to counteract dynamic degradation caused by hot-electron stress, offering substantial resilience compared to conventional designs [26]. Strain-enhancing layers, achieved through selective regrowth of AlN/AlGaN, have been implemented to reshape surface electric fields, balancing ON-resistance and breakdown voltage while suppressing current collapse. Furthermore, crystalline passivation layers, such as GaO_x/GaO_xN_{1-x}, formed through advanced surface treatments and annealing, have shown promise in restoring the 2DEG beneath the p-GaN layer and maintaining high breakdown voltage [27].

2.5.2 GaN MIS-HEMTs

GaN MIS-HEMTs have gained prominence for high-power applications due to their ability to suppress gate leakage currents while maintaining excellent 2DEG mobility, making them highly reliable for advanced power electronics. The integration of high-κ gate dielectrics, such as $LaLuO_3$ thin films, has demonstrated superior static performance, including high ON/OFF ratios and enhanced drain current, though strategies to mitigate dynamic ON-resistance degradation at high drain bias remain underexplored [28]. Interface charge engineering, using methods like oxygen plasma treatments and post-metallization annealing, has been shown to improve electron mobility and threshold voltage stability, yet optimizing these techniques to achieve robust normally-off operation while addressing issues like remote impurity scattering requires further investigation [29]. Low-temperature fabrication processes for GaN-

on-Si substrates, employing gold-free metal stacks, have shown promise for scalable, CMOS-compatible devices, though optimizing these methods to maintain high electrical performance is still a challenge [30]. Incorporating advanced features such as pulsed laser-deposited interface protection layers and trench termination structures has improved breakdown voltage and reduced interface trap density, highlighting the potential for enhanced device reliability, but the interplay between these elements demands more detailed exploration [31]. The identification of deep-level traps in GaN buffers as contributors to threshold voltage instability underscores the importance of optimized buffer designs, particularly in high-voltage applications on Si substrates, where trap effects are pronounced [32]. High-performance normally-off fin-MIS-HEMTs with optimized gate-recessed fin structures and low work function metal-source contact ledges have achieved notable stability and breakdown voltage, yet further refinement is needed to improve dynamic performance and scalability [33]. Studies on dynamic ON-resistance in MIS-gated AlGaN/GaN HEMTs have highlighted the influence of gate bias and the benefits of high-κ oxides in enhancing gate control, but a deeper understanding of these mechanisms is required, particularly in comparison to Schottky-gated devices [34]. Additionally, low-damage atomic layer etching processes have shown potential for improving recessed gate performance, revealing that reduced AlGaN thickness increases electric field strength at the gate edge, which can impact breakdown voltage and trap-assisted tunnelling [35

2.6 Applications of GaN HEMT Technology

GaN HEMTs have become indispensable across various industries due to their exceptional performance characteristics. In power electronics, they are widely employed in high-frequency and high-power applications, including power supplies, inverters, and converters for renewable energy systems [13]-[15]. Their high electron mobility and low on-resistance enable efficient power conversion, reducing switching losses, enhancing energy efficiency, and supporting more compact system designs. In radio frequency (RF) and microwave applications, GaN HEMTs play a vital role in telecommunications, radar systems, and wireless communication

networks [16], [17]. Their ability to operate at high frequencies, combined with low parasitic capacitance, makes them ideal for high-speed data transmission and signal amplification, supporting the advancement of next-generation communication technologies. The automotive industry has also embraced GaN HEMTs, particularly in electric vehicles (EVs) and hybrid electric vehicles (HEVs) [18]-[20]. Their fast switching speeds and robustness improve power management, enhancing vehicle performance and extending battery life. However, the industry's push towards autonomous driving and connected vehicles introduces challenges such as managing electromagnetic interference (EMI) and ensuring thermal reliability under extreme conditions. In aerospace and defense, GaN HEMTs are highly valued for their ability to handle high power and resist radiation, making them ideal for radar systems, electronic warfare, and satellite communications. While these characteristics make GaN HEMTs reliable in harsh environments, there is a need for more research on their long-term reliability under extreme conditions.

2.7 Literature Review

The advancement of GaN HEMTs has been a focal point of research due to their potential for high-performance power electronics applications. Over the years, significant efforts have been made to enhance key performance metrics such as gate leakage current, breakdown voltage, and R_{ON}, which are critical for achieving reliable and efficient device operation. Furthermore, analytical modeling has played a pivotal role in understanding and optimizing these parameters, providing deeper insights into device behavior and facilitating the design of innovative structures. This section offers a comprehensive review of the existing literature, summarized in tabular format, focusing on the major findings in breakdown voltage enhancement, on-resistance improvement, gate leakage current reduction, and analytical modeling for gate leakage current optimization.

Table 2.1: Literature on Breakdown Voltage of GaN-HEMT

Ref	Author Name & Year	Design Technique	Findings
[36]	Chen et al. (2010)	Self-aligned Enhancement-mode AlGaN/GaN HEMTs Using 25 keV Fluorine Ion Implantation	The study presents self-aligned enhancement mode AlGaN/GaN HEMTs developed through 25 keV fluorine ion implantation, attaining a threshold voltage of +0.6 V and an off-state breakdown voltage of 254 V while exhibiting minimal current collapse.
[37]	Hilt et al. (2011)	Normally-off High-Voltage p-GaN Gate GaN HFET with Carbon-Doped Buffer	The study reports a normally-off p-GaN gate GaN HFET incorporating a carbon-doped buffer and AlGaN back-barrier, achieving a breakdown voltage of 1000 V, an on-state resistance of 0.62 mΩ·cm², and a high power figure-of-merit of 1.6 GW/cm².
[38]	Su et al. (2014)	Enhancement-Mode GaN-Based HEMTs on the Si Substrate with a P-Type GaN Cap Layer	The study presents an enhancement-mode AlGaN/GaN HEMT fabricated on a silicon substrate with a p-type GaN cap, achieving a 1630 V off-state breakdown voltage and enhanced suppression of leakage current, making it suitable for high-power applications.
[39]	Chitransh et al.(2017)	Field Plated GaN HEMT	The study investigates an AlGaN /GaN HEMT incorporating an AlN spacer and a field plate, showing a breakdown voltage between 231 V and 235 V based on GaN channel

Ref	Author Name & Year	Design Technique	Findings
			thickness, indicating its suitability for high-power applications.
[40]	Yang et al. (2018)	AlGaN/GaN MIS-HEMT With AlN Interface Protection Layer and Trench Termination Structure	The study introduces a normally-off AlGaN/GaN MIS-HEMT featuring an AlN interface protection layer and trench termination, achieving a 412 V off-state breakdown voltage while enhancing interface quality through reduced trap density and improved electric field modulation.
[41]	Fletcher et al. (2019)	AlGaN/GaN HEMT using discrete field plate technique	The research examines AlGaN/GaN HEMTs employing a discrete field plate approach, resulting in a 330 V breakdown voltage, a cut-off frequency of 20 GHz, and lowered gate source and gate drain capacitances, highlighting their suitability for high power, high frequency applications.
[42]	Liu et al. (2019)	A GaN based RB MIS-HEMT with Schottky-MIS hybrid Drain and TUG-AlGaN Barrier Layer	The study proposes a GaN-based RB-MIS-HEMT with a Schottky-MIS hybrid drain and a thin upward graded AlGaN barrier, delivering a reverse breakdown voltage of 900 V, a low drain offset voltage of 0.60 V, and an on-state voltage of 1.80 V at 100 mA/mm, making it well-suited for reverse blocking power applications.
[22]	Liu et al. (2020)	*p*-GaN-gate GaN HEMT with a hybrid AlGaN buffer	The study presents a p-GaN gate GaN HB-HEMT incorporating a

Ref	Author Name & Year	Design Technique	Findings
		layer for power electronics applications	hybrid AlGaN buffer layer, demonst-rating a simulated offstate breakdown voltage of 1450 V, a low specific ON-resistance of 0.47 mΩ·cm², and an enhanced Baliga's figure of merit of 4.47 GW/cm², highlighting its potential for power electronics applications.
[43]	Zhang et al. (2020)	Gallium Nitride Dual Two-Dimensional Electron Gas HEMT	The study introduces a GaN dual two-dimensional electron gas HEMT (D2DEG-HEMT) with a vertical channel structure, achieving a simulated off-state breakdown voltage of 465 V and delivering greater power density than a conventional GaN recessed gate MIS-HEMT with identical device dimensions.
[44]	Huang et al.(2020)	Normally-OFF AlGaN/GaN Fin- MIS-HEMT on Silicon with Low Work Function Metal-Source Contact Ledge	The study showcases a high-performance normally off AlGaN /GaN fin-MIS-HEMT fabricated on a silicon substrate, utilizing a low work function metal-source contact ledge to achieve an off-state breakdown voltage of 810 V, a specific ON-resistance of 0.63 mΩ·cm², and superior dynamic R_{ON} stability.
[45]	Zhang et al. (2020)	GaN HEMT using Super Field Plate Technique	The paper presents an innovative super field plate (SuFP) approach that enables a charge balance effect in lateral power devices, achieving a

Ref	Author Name & Year	Design Technique	Findings
			simulated breakdown voltage over 300 V without utilizing the drift region and offering improved electric field uniformity over conventional techniques.
[46]	Bhatt et al. (2021)	AlGaN/GaN HEMT with a Grated Gate Field Plate	The study explores AlGaN/GaN HEMTs featuring grated gate field plates (GGFP), achieving a breakdown voltage of 272 V and a 60% increase in cutoff frequency relative to standard GFP HEMTs, thereby enhancing overall device performance.
[47]	Du et al. (2021)	GaN HEMT on Free-Standing GaN Substrate	The study reports AlGaN/GaN HEMTs developed on a free-standing GaN substrate, attaining an off-state breakdown voltage of 193 V, a low contact resistance of 0.23 Ω·mm, and outstanding RF performance characterized by a Johnson's figure-of-merit of 5.0 THz·V.
[48]	Wei et al. (2021)	Normally-OFF AlGaN/GaN HEMTs using Etching-Free p-GaN Stripe Array Gate	The study presents normally-off AlGaN/GaN HEMTs utilizing an etching-free p-GaN stripe array gate (PSAG), achieving a high off-state breakdown voltage of 1449 V, a low specific R_{ON} of 2.73 mΩ·cm², and enhanced thermal stability along with improved surface electric field distribution.
[49]	Hult et al.	GaN-on-SiC MIS-HEMTs on	The study showcases a novel buffer-

Ref	Author Name & Year	Design Technique	Findings
	(2022)	a “Buffer-Free” Hetero-structure	free AlGaN/GaN-on-SiC MIS-HEMT built on a semi-insulating SiC substrate, achieving a high off-state breakdown voltage of 1622 V, along with low leakage current and enhanced efficiency for power switching applications.
[50]	Langpoklakpam et al. (2023)	GaN MIS-HEMT with Drain Field Plate Structure and Passivation Dielectrics	The study introduces a novel GaN MIS-HEMT featuring a two-step drain field plate (D-FP) structure, achieving an improved off-state breakdown voltage of 1587 V—350 V higher than that of conventional GaN MIS-HEMTs—while preserving stable DC performance.
[51]	Cui et al. (2024)	p-GaN Gate HEMT on Sapphire with Gate Termination Extension	The study presents an enhancement-mode p-GaN gate HEMT with a gate termination extension (GTE) on a sapphire substrate, achieving a high breakdown voltage of 2573 V and enhanced suitability for kilovolt-class power switching applications.
[52]	Wang et.al (2024)	Ohmic-Like p-GaN Gate HEMT With a Built In Reverse Diode	The study presents an ohmic-like p-GaN gate HEMT integrated with a built-in diode (BD), offering improved gate reliability, a gate breakdown voltage exceeding 100 V, an off-state breakdown voltage of 961 V, and enhanced forward gate stability under high-stress conditions.

Ref	Author Name & Year	Design Technique	Findings
[53]	Kumar et.al (2024)	p-GaN gate HEMTs on 200 mm engineered substrates	The study showcases enhancement-mode p-GaN gate HEMTs fabricated on 200 mm QST® engineered substrates, achieving an off-state breakdown voltage of 1800 V along with outstanding wafer scale uniformity.

Table 2.2: Literature on On-Resistance of GaN-HEMT

Ref	Author Name & Year	Design Technique	Findings
[37]	Hilt et.al (2011)	p-GaN Gate GaN HFET with Carbon-Doped Buffer	The study reports normally-off p-GaN gate GaN HFETs that exhibit a low on-state resistance of 7.4 Ω·mm at a 6 µm gate-drain spacing and a high breakdown voltage of 1000 V, while effectively balancing on-resistance and threshold voltage.
[54]	Jiang et.al (2013)	1.4-kV AlGaN/GaN HEMTs on a GaN-on-SOI Platform	AlGaN/GaN HEMTs fabricated on a GaN-on-SOI platform achieve a low on-resistance of 3.92 mΩ·cm², indicating high efficiency and strong potential for power electronic applications.
[55]	Wei et.al (2015)	GaN Double channel MOS-HEMT (DC-MOS-HEMT)	The proposed device attains a low R_{ON} of 6.9 Ω·mm and a specific R_{ON} of 1.48 mΩ·cm², attributed to the high field-effect mobility in the lower channel.

Ref	Author Name & Year	Design Technique	Findings
[56]	Cen et.al (2017)	Enhancement-mode p-GaN HEMT Power Electronic Device	The proposed enhancement-mode device achieved a specific on-resistance of 0.45 mΩ·cm², indicating low conduction loss and high efficiency for power electronic applications.
[22]	Liu et.al (2020)	*p*-GaN-gate GaN HEMT with a hybrid AlGaN buffer layer	The proposed p-GaN gate GaN HEMT with a high breakdown voltage and a hybrid AlGaN buffer layer achieves a low specific R_{ON} of 0.47 mΩ·cm², showcasing its effectiveness for power electronics applications.
[44]	Huang et.al (2020)	Normally-OFF AlGaN/GaN Fin-MIS-HEMT on Silicon With Low Work Function Metal-Source Contact Ledge	The study demonstrates that the proposed normally-off AlGaN/GaN Fin-MIS-HEMT, incorporating a low work function metal-source contact ledge, achieves a specific on-resistance of 0.63 mΩ·cm², enabling high efficiency and reduced power loss in power applications.
[19]	Chang et.al (2021)	p-GaN/AlGaN/GaN HEMTs with an Indium-Tin-Oxide Gate Electrode	The study highlights that p-GaN/AlGaN/GaN HEMTs utilizing indium tin oxide (ITO) gate electrodes attain a specific on-resistance of 1.86 mΩ·cm², providing lower resistance and enhanced gate stability over traditional Schottky gate configurations.
[49]	Hult et.al (2022)	GaN-on-SiC MIS-HEMTs on a "Buffer-Free" Hetero-	The study shows that buffer-free GaN-on-SiC MIS-HEMTs achieve a

Ref	Author Name & Year	Design Technique	Findings
		structure	specific R_{ON} of 3.61 mΩ·cm², combining low conduction resistance with high breakdown voltage capabilities.
[53]	Kumar et.al (2024)	p-GaN gate HEMTs on 200 mm engineered substrates	The study reports a low specific ON-resistance of 5.8 mΩ·cm² for 1.2 kV enhancement-mode p-GaN gate HEMTs, exhibiting excellent wafer-scale uniformity with a σ_{Ron} of 1.2% across 200 mm engineered QST® substrates.
[57]	Wang et.al (2024)	AlGaN/GaN-Based Lateral Schottky Barrier Diodes with a High-k Field Plate	The device achieves a low specific ON-resistance of 3.2 mΩ·cm².
[58]	Shen et.al (2024)	p-GaN/AlGaN/GaN HEMTs with Selective Regrowth AlN/AlGaN Strain Layers	The study shows that incorporating a selective regrowth (SR) AlN/AlGaN strain layer in p-GaN gate HEMTs decreases the specific on-resistance by 11.9%—from 2.26 to 1.99 mΩ·cm²—and improves the breakdown voltage from 476 V to 661 V compared to the standard design.
[59]	Chen et.al (2024)	Gold-Free GaN HEMT devices with Gate-Field Plate and Hybrid Drain	The study reports that the GaN HEMT exhibited an on-resistance between 108 and 152 mΩ·mm, with dynamic-to-static on-resistance ratios ranging from 1.98 to 17.2 based on the off-state drain bias up to 400 V.

Table 2.3: Literature on Gate Leakage of GaN-HEMT

Ref	Author Name & Year	Design Technique	Findings
[60]	Rajabi et al. (2011)	AlGaN/GaN/AlGaN Double Heterojunction High Electron Mobility Transistor	The inclusion of a magnesium doping layer in the AlGaN buffer of AlGaN/GaN/AlGaN double hetero-junction HEMTs effectively suppresses subthreshold gate leakage current by improving the electric field distribution and reducing field peaks near the gate.
[61]	Anderson et.al (2013)	Nanocrystalline Diamond-Gated AlGaN/GaN HEMT	The device exhibits significantly reduced gate leakage current compared to conventional Ni/Au-gated devices, due to the NCD /AlGaN hetero-junction, which limits reverse leakage and enables stable operation at higher gate voltages
[62]	Huang et.al (2016)	Normally-OFF GaN MIS-HEMTs Fabricated on Ultra-Thin-Barrier AlGaN/GaN Heterostructure	The device exhibits low gate leakage current, attributed to the Al_2O_3 gate dielectric and optimized LPCVD-SiN_x passivation, which suppresses deep interface states
[63]	Tang et.al (2018)	AlGaN/GaN HEMTs with AlN/SiNx Passivation	The device achieves low gate leakage current, maintaining leakage below 1 μA/mm at V_{DS} up to 632 V, due to the strong polarization effects of the AlN/SiN_x stack
[64]	Zhou et al. (2020)	p-GaN HEMTs Using Metal/Graphene Gates	The insertion of intrinsic graphene (I-graphene) or fluorinated graphene (F-graphene) in p-GaN HEMTs reduces gate leakage current by 50 times in

Ref	Author Name & Year	Design Technique	Findings
			reverse bias compared to devices without graphene, significantly improving gate performance.
[65]	Yu et al. (2020)	MIS p-GaN-Gated HEMTs with Gate-All-Around Structure	The gate-all-around MIS p-GaN HEMT achieves an ultra-low gate leakage current of 10^{-8} mA/mm at VG=5V, significantly outperforming conventional Schottky gate devices in terms of leakage suppression.
[19]	Chang et.al (2021)	p-GaN/AlGaN/GaN HEMTs with an Indium-Tin-Oxide Gate Electrode	The study demonstrates that p-GaN/AlGaN/GaN HEMTs with an indium-tin-oxide (ITO) gate electrode exhibit a significantly reduced gate leakage current, remaining stable up to a gate voltage of 11 V, surpassing the performance of traditional Ni/Au Schottky gate contacts.
[66]	L. Zhang et al. (2022)	p-Channel FET With SiN_x /GaON Staggered Gate Stack	The study demonstrates that GaN p-FETs with a SiN_x/GaON staggered gate stack exhibit significantly suppressed gate leakage currents at small gate voltages ($\|V_G\| < 4$ V), attributed to the effective barriers provided by the GaON layer and the staggered band alignment.
[67]	Chand et al. (2022)	InAlN/AlN/GaN HEMT using aluminium gallium nitride back barrier	The study demonstrates that incorporating an AlGaN back barrier in InAlN/AlN/GaN gate-recessed HEMTs reduces gate leakage current by up to 15 times compared to

Ref	Author Name & Year	Design Technique	Findings
			devices without a back barrier, enhancing power efficiency and reliability.
[68]	Baby et al. (2023)	TaN Gated p-GaN E-Mode HEMT	The device demonstrates a significantly reduced forward gate leakage current, achieving values three orders of magnitude lower than Ti/Au-gated devices. Its gate leakage is 60 μA/mm at a gate voltage of 8 V and 150°C.
[69]	Dai et al. (2024)	AlGaN/GaN HEMT with Island-Ohmic *p*-GaN	The proposed Island-Ohmic p-GaN gate HEMT (IO-PGaN) achieves a moderate gate leakage current (~20 μA/mm at V_{GS} = 6 V), significantly reducing leakage compared to Ohmic-p-GaN HEMTs while maintaining better stability than Schottky-p-GaN HEMTs.
[52]	Wang et al. (2024)	Ohmic-Like p-GaN Gate HEMT With a Built-In Reverse Diode	The ohmic-like p-GaN gate HEMT with a built-in diode demonstrates a significant reduction in gate leakage current, clamped at 0.3 mA/mm under a forward gate voltage of 100 V, showcasing improved gate reliability and thermal stability compared to conventional Schottky-contact devices.
[70]	Liu et al. (2024)	p-GaN HEMT With AlN/GaN/AlN Double Barriers Cap Layer	The p-GaN HEMT with an AlN/GaN/AlN double-barriers cap layer achieves an ultra-low gate leakage current of 2.74×10^{-6} mA/mm

Ref	Author Name & Year	Design Technique	Findings
			at V_{GS}=9 V, a three-order reduction compared to conventional p-GaN HEMTs, demonstrating enhanced gate reliability.

Table 2.4: Literature on Analytical Modeling of Gate Leakage in GaN-HEMT

Ref	Author Name & Year	Design Technique	Findings
[71]	Khandelwal et al.(2011)	A Physics-Based Analytical Model for 2DEG Charge Density in AlGaN/GaN HEMT Devices	The proposed physics-based analytical model for 2DEG charge density in AlGaN/GaN HEMTs effectively captures the relationship between the Fermi level and 2DEG density, showing strong consistency with numerical results over a broad range of gate voltages.
[72]	Khandelwal et al.(2012)	A Physics-Based Compact Model for Drain Current in AlGaN/GaN HEMT Devices	The proposed physics-based compact model for drain current in AlGaN/GaN HEMTs accounts for key phenomena including velocity saturation, self-heating, and channel length modulation, and closely matches experimental data across different device structures and operating regimes.
[73]	Khandelwal et al.(2012)	A Physics-Based Compact Model of Gate Capacitance in AlGaN/GaN HEMT Devices	The proposed physics-based compact model accurately predicts gate capacitance in AlGaN/GaN HEMTs by incorporating a continuous

Ref	Author Name & Year	Design Technique	Findings
			analytical expression for 2DEG charge density, demonstrating strong agreement with experimental data across all operating regions.
[74]	Yigletu et al. (2013)	A Compact Charge-Based Physical Model for AlGaN /GaN HEMTs	The compact charge-based physical model for AlGaN/GaN HEMTs accurately determines 2DEG charge density by considering only the first energy level, simplifying the model while maintaining strong agreement with experimental I-V data.
[75]	Karumuri et al.(2014)	A Continuous Analytical Model for 2-DEG Charge Density in AlGaN/GaN HEMTs Valid for All Bias Voltages	The proposed analytical model for 2DEG charge density in AlGaN/GaN HEMTs considers both electron charges in the AlGaN barrier layer and Fermi–Dirac statistics, providing continuous and accurate predictions of charge density across all operational regions.
[76]	Guang et al. (2015)	Formation of a two-dimensional electron gas at AlGaN/GaN heterostructure and the derivation of its sheet density expression	The study derives a corrected analytical expression for the 2DEG sheet density in AlGaN/GaN heterostructures, resolving confusion in widely cited models and demonstrating that the polarization-induced charge in AlGaN alone contributes to the 2DEG formation.
[77]	Ghosh et al. (2017)	Modeling the Effect of the Two-Dimensional Hole Gas in a GaN/AlGaN/GaN Heterostructure	The analytical model developed for GaN/AlGaN/GaN hetero-structures includes the effects of the two-dimensional hole gas (2DHG) along

Ref	Author Name & Year	Design Technique	Findings
			with the 2DEG, accurately predicting electron concentration and surface barrier height, showing strong agreement with experimental data.
[78]	Albahrani et al.(2020)	Extreme Temperature Modeling of GaN HEMTs	The enhanced ASM-GaN compact model accurately incorporates temperature-dependent trapping effects to predict the behavior of AlGaN/GaN HEMTs across a wide temperature range (22°C to 500°C), achieving strong alignment with experimental results.
[79]	Shanbhag et al.(2022)	Compact Modeling of Static and Transient Effects of Buffer Traps in GaN HEMTs	The proposed model for GaN HEMTs captures the buffer trap's static and transient effects, accurately predicting the shift in threshold voltage and reduction in 2DEG density under steady-state and pulsed conditions with excellent agreement with experimental data.
[80]	Bhat et al. (2024)	A Comprehensive Model for Gate Current in E-Mode p-GaN HEMTs	The proposed physics-based analytical model for gate current in p-GaN HEMTs integrates Schrödinger-Poisson equations to account for sub-band energy states and effectively predicts gate leakage mechanisms, including thermionic emission, Poole-Frenkel emission, and thermally assisted tunneling, across a wide bias and temperature range.

2.8 Research Gaps

While the literature demonstrates remarkable progress in GaN HEMT technology, several gaps remain, hindering the full realization of its potential in power electronics:

- High gate leakage in GaN HEMTs limits reliability is not fully solved.
- The impact of on-resistance on the efficient operation of GaN HEMT has not been thoroughly explored in the existing research.
- The breakdown voltage remains a crucial issue that must be addressed for GaN HEMT devices to withstand high voltages.
- Analytical models for gate leakage are limited and do not fully capture all leakage mechanisms for accurate optimization.

2.9 Summary

This chapter provided a comprehensive exploration of advancements and challenges in GaN HEMT technology, with a particular emphasis on their applications in power electronics. Through an extensive review of existing literature, this chapter has highlighted the transformative potential of GaN HEMTs in overcoming the limitations of traditional silicon-based power devices due to their superior material properties such as a wide bandgap, high breakdown voltage, and exceptional thermal stability.

The literature underscored significant progress in enhancing critical performance metrics such as breakdown voltage, on-resistance, and gate leakage current. Innovations like p-GaN gate engineering, buffer optimization, and passivation techniques have driven substantial improvements in device performance and reliability. Additionally, the development of advanced device architectures, including multi-channel heterostructures and field-plated designs, has paved the way for improved power density and efficiency. Analytical modeling efforts have further provided valuable insights into device behavior, enabling precise optimization for high-power and high-frequency applications.

This chapter has also identified emerging trends and technologies, such as GaN MIS-HEMTs and novel gate engineering techniques, that hold promise for addressing existing limitations. However, there remains a pressing need for innovative solutions to mitigate issues like current collapse and gate leakage. The insights gained from this literature review serve as a foundation for addressing the identified research gaps and advancing the field of GaN HEMT technology. The knowledge synthesized here not only contributes to the academic understanding of GaN HEMTs but also provides a roadmap for future research aimed at realizing their full potential in high-performance and reliable power electronics systems.

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CHAPTER 3

OPTIMIZATION AND SUPPRESSION OF GATE LEAKAGE CURRENT

3.1 Introduction

The previous chapter explored the development and evolution of GaN HEMT technology over the years, highlighting the key research contributions that inspired further exploration into related structures and underlying principles. This chapter presents the optimization and analysis of novel p-GaN HEMT designs aimed at improving performance in power electronics applications by reducing gate leakage current. The first approach introduces an enhancement-mode GaN HEMT that integrates a p-GaN layer with an HfO_2 dielectric beneath the metal gate. The p-GaN layer acts as a barrier to suppress tunneling, while the HfO_2 layer, with a lower density of trap sites compared to SiN, further reduces gate leakage. This device demonstrates superior performance, achieving lower leakage current, higher maximum drain current, and an improved threshold voltage. The second approach explores a Gaussian-doped p-GaN HEMT, where donor impurities are introduced into the GaN channel layer through a controlled doping profile. This method effectively minimizes electric field variations at the channel interface, significantly reducing gate leakage current and enhancing off-state performance. The third approach features an Omega (Ω)-shaped gate p-GaN MIS-HEMT, which encapsulates the dielectric layer above the p-GaN layer to ensure a more uniform stress distribution, thereby minimizing dielectric breakdown risks and enhancing device reliability. Optimization efforts focused on the gate dielectric's thickness, length, and material, leading to improved breakdown voltage, higher threshold voltage, and reduced gate leakage current. Comparative analysis highlights the superior performance of the proposed devices over conventional designs, demonstrating key improvements in gate leakage current, breakdown voltage,

threshold voltage, on-current, and transconductance. Additionally, optimization strategies targeting gate leakage reduction are employed to achieve optimal device performance, making these designs suitable for high-power electronics applications.

3.2 An Enhancement Mode GaN HEMT with MIS and p-GaN structure

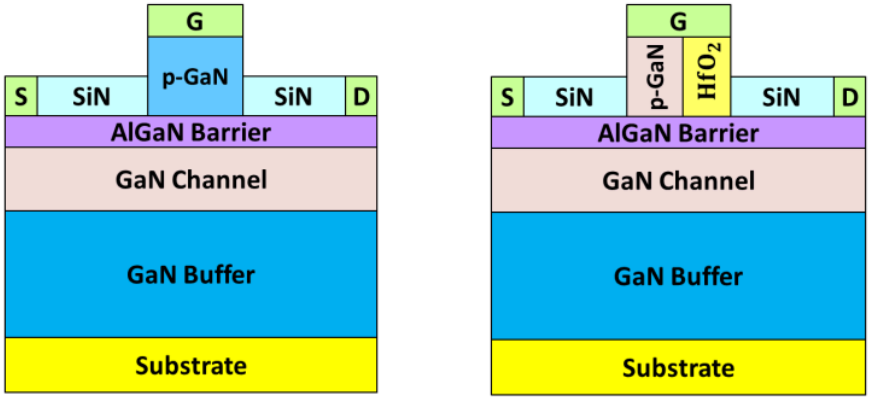
This section introduces a novel enhancement-mode GaN HEMT (MGHEMT) designed to reduce gate leakage current by integrating a p-GaN layer and an HfO_2 layer beneath the metal gate. The p-GaN layer acts as a barrier to suppress tunneling, while the HfO_2 layer, with its lower density of trap sites compared to SiN, further minimizes gate leakage. In this design, the p-GaN layer forms a Schottky contact with the gate, and the incorporation of the MIS structure within the gate area enhances gate control, reduces leakage current, and increases current capacity. Additionally, the proposed device demonstrates superior performance in terms of reduced gate leakage current, enhanced maximum drain current, and an improved threshold voltage compared to reported devices. The selective passivation on the drain side lowers capacitance, potentially improving device speed and performance, while the dielectric layer, with its higher bandgap compared to p-GaN, provides a more substantial potential barrier, effectively reducing tunneling current through the gate dielectric.

3.2.1 Device structure, Calibration, and Simulation setup

Fig. 3.1 (a) and Fig. 3.1 (b) depict the schematic diagrams of the conventional p-GaN HEMT and the proposed MGHEMT, respectively. The MGHEMT design incorporates a p-GaN layer in parallel with an HfO_2 layer, which is positioned beneath the metal gate within the device architecture. The structural parameters of the proposed MGHEMT are summarized in Table 3.1. The AlGaN barrier layer features an aluminum composition of 0.2, while the p-GaN layer in both devices has a doping concentration of $3\times10^{17}\ cm^{-3}$.

For calibration purposes, the p-GaN HEMT design included parameters such as a 2 µm $Al_{0.25}Ga_{0.75}N$ buffer layer, an 85 nm GaN channel layer, a 15 nm $Al_{0.26}Ga_{0.74}N$

barrier layer, and a 110 nm thick p-GaN layer [1]. Figure 3.2 compares the experimental and simulated transfer characteristics, demonstrating excellent



(a) (b)

Fig. 3.1: The schematic diagram of (a) the conventional device and (b) the proposed MG-HEMT

Table 3.1: The structural parameters of the proposed MGHEMT

S.No.	Parameter	Value
1.	p-GaN layer in parallel with the HfO_2 layer thickness ($T_{Parallel}$)	110 nm
2.	AlGaN barrier layer thickness ($T_{AlGaNbarrier}$)	15 nm
3.	GaN channel layer thickness ($T_{GaNchannel}$)	85 nm
4.	GaN buffer layer thickness ($T_{GaNbuffer}$)	2 μm
5.	SiN passivation layer thickness ($T_{SiNpassivation}$)	300 nm

agreement and confirming the accuracy of the simulation models. These simulations utilized the SRH model, GaN polarization model, high- and low-field mobility models, Fermi–Dirac statistics, and the Toyabe model. Furthermore, carrier transport in the channel was modeled using drift-diffusion transport based on Boltzmann theory, providing a comprehensive simulation framework [1].

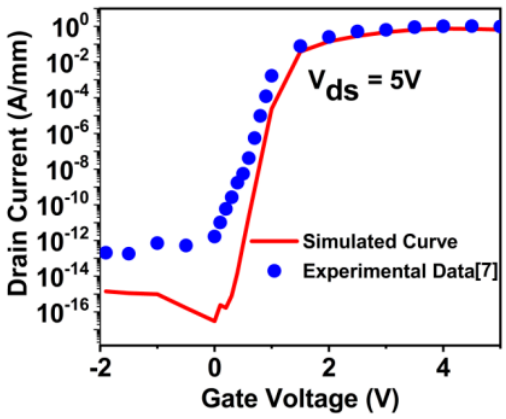


Fig. 3: Calibration of the p-GaN HEMT

3.2.2 Results and Discussion

This section examines the DC and AC characteristics of the proposed device. Fig. 3.3(a) illustrates the electric field characteristics in the MGHEMT for various dielectric constants of the insulator layer. To enhance device performance, a high-k dielectric material was employed, known for its superior charge storage capacity compared to low-k alternatives. This selection effectively reduces the electric field within the device, as high-k materials inherently provide greater capacitance per unit area. Fig. 3.3(b) demonstrates the corresponding gate leakage current, showing that the reduced electric field lowers the likelihood of electron tunneling. HfO_2, with its high dielectric constant, achieves the lowest electric field and gate leakage current, making it the optimal dielectric material for the device.

To further optimize device performance, minimizing gate leakage current was critical for improving reliability. Simulations were conducted by varying the length of the HfO_2 dielectric layer (L_{dt}) to study its effect on the device's electrical characteristics. Adjusting L_{dt} systematically from 2.5 µm to 2.8 µm in 0.1 µm increments, while keeping other parameters constant, revealed that the lowest gate leakage current occurred at L_{dt} = 2.7 µm. This length represents the optimal value for reducing leakage and enhancing reliability, as shown in Fig. 3.4(a). Temperature-dependent gate current versus gate voltage (I_g-V_g) curves were also analyzed over a temperature range of 200 K to 400 K. The results (in Fig. 3.4(b)) show that gate leakage current increases with temperature due to higher carrier concentrations and thermal energy, which facilitate tunneling.

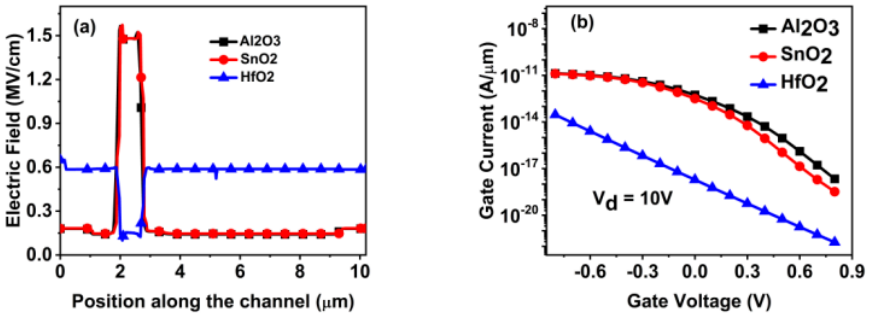


Fig. 3.3: The comparison of the proposed device with respect to the dielectric constant of the insulating layer (a) the electric field and (b) the gate leakage current.

A comparative analysis of the DC and AC characteristics of the conventional p-GaN HEMT and the optimized MGHEMT was performed. Fig. 3.5(a) reveals the electric field distributions, highlighting the effective suppression of the channel electric field in the proposed device due to the HfO_2 dielectric layer [2]. Consequently, the proposed device exhibits a significantly lower gate leakage current, as presented in Fig. 3.5(b). The C-V characteristics of the MGHEMT, presented in Fig. 3.6(a), demonstrate its superior performance over the conventional p-GaN HEMT, with

reduced parasitic capacitance and lower power consumption. Fig. 3.6(b) compares transconductance, where the proposed device outperforms the conventional p-GaN HEMT, indicating improved current drive capability.

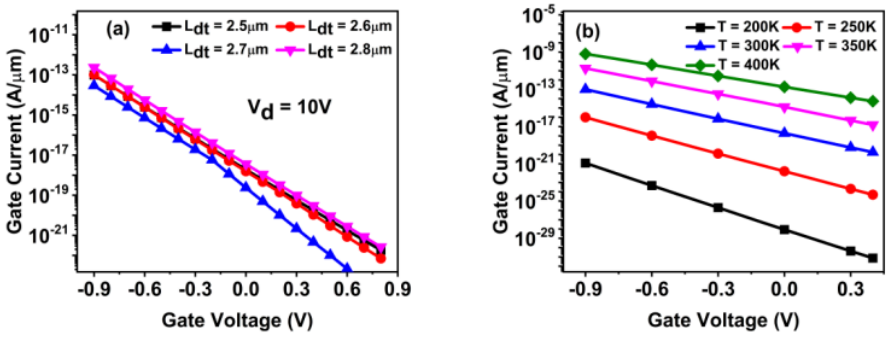


Fig. 3.4: (a) The gate leakage current for different values of length of the HfO_2 dielectric layer (L_{dt}), and (b) The temperature-dependent I_g-V_g curves of the proposed device from 200 K to 400 K.

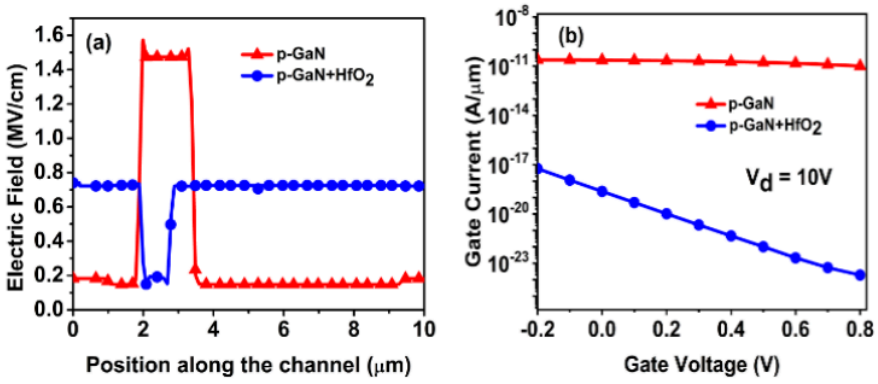


Fig. 3.5: (a) The electric field and (b) the gate leakage current comparison of the proposed and conventional device.

Fig. 3.7(a) and Fig. 3.7(b) depict the I_d-V_d and I_d-V_g characteristics, respectively. In Fig. 3.7(a), the MGHEMT achieves a significantly higher maximum drain current ($I_{ds,max}$), reaching 1 A/μm, surpassing the 0.6 A/μm of the conventional p-GaN

HEMT. Additionally, fixed charges at the interface or within the HfO_2 layer influence the device's threshold voltage, as shown in Fig. 3.7(b). Table 3.2 provides a comparative summary of the proposed MGHEMT and previously reported devices.

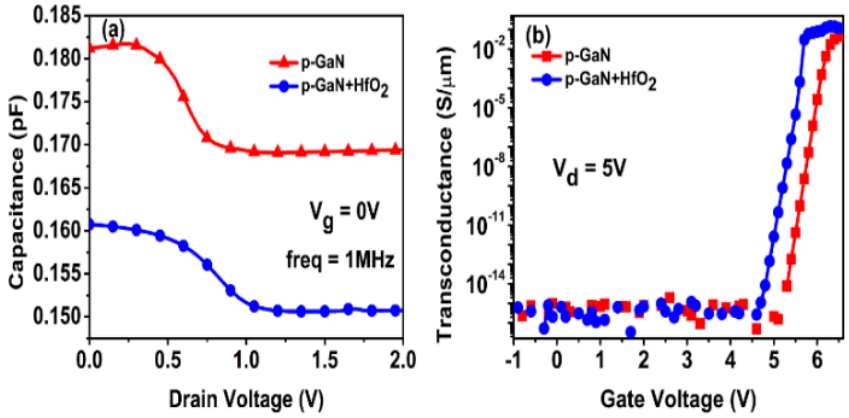


Fig. 3.6:(a) Gate capacitance and (b) transconductance comparison of the proposed and conventional device.

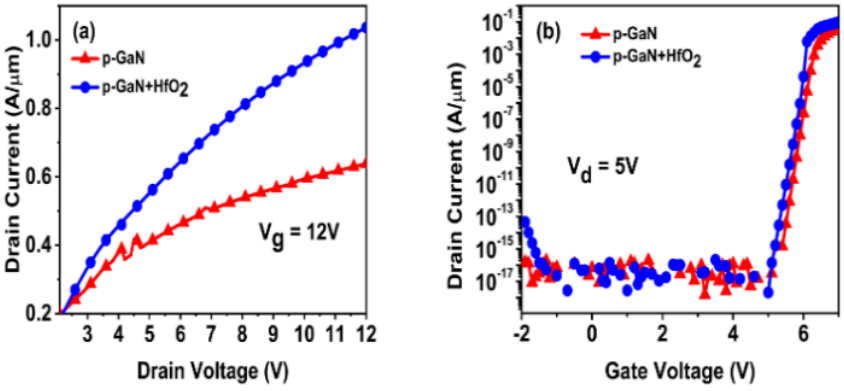


Fig. 3.7:(a) I_d-V_d and (b) I_d-V_g characteristics comparison of the conventional and proposed device

3.3 A Gaussian Doped p-GaN HEMT

A novel p-GaN HEMT has been designed and investigated to enhance performance in power electronics applications by employing a Gaussian doping technique to introduce donor impurities into the GaN channel layer. This controlled doping

Table 3.2: Comparison of performance parameters of the proposed device with the reported literature

Reference	Gate Leakage Current (A/μm)	Maximum Drain Current (A/μm)	Threshold Voltage (V)
[3]	10^{-15}	0.35	2.5
[4]	10^{-18}	0.8	-15
[5]	10^{-17}	0.7	-5
Conventional p-GaN HEMT	10^{-12}	0.6	0.49
This work	**10^{-21}**	**1**	**5**

approach creates a gradual doping profile, minimizing electric field variations at the channel interface and significantly reducing gate leakage current, thereby improving the device's off-state performance. Comparative analysis demonstrates that the proposed device outperforms conventional p-GaN HEMTs without doping in the GaN channel layer, achieving reduced gate leakage current, higher maximum drain current, increased on-current, and enhanced transconductance. Optimization strategies are employed to further minimize gate leakage current and achieve optimal device performance. Additionally, a comparative evaluation of the proposed device's performance parameters against those of previously reported devices has been presented. By effectively reducing leakage current, Gaussian-doped GaN HEMTs improve efficiency, making them highly suitable for high-performance power electronics applications where leakage control is critical.

3.3.1 Device structure, Calibration, and Simulation setup

Fig. 3.8(a) and Fig. 3.8(b) illustrate the schematic structures of the conventional p-GaN HEMT and the proposed Gaussian Doped High Electron Mobility Transistor (GDHEMT), respectively. The GDHEMT design incorporates a Gaussian doping technique to introduce donor impurities into the GaN channel layer. Table 3.3 outlines the parameters of the proposed GDHEMT structure. Both devices feature an AlGaN barrier layer with an aluminum composition of 0.2 and a p-GaN layer with a doping concentration of 3×10^{17} cm^{-3}.

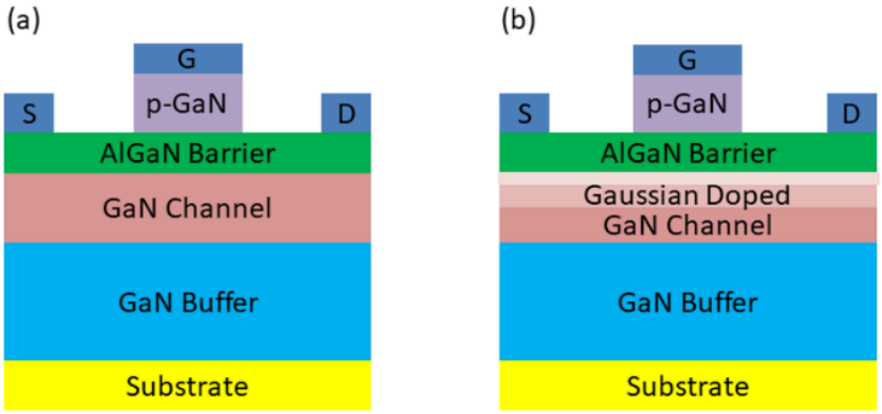


Fig. 3.8: The schematic diagram of (a) the conventional device and (b) the proposed GD-HEMT.

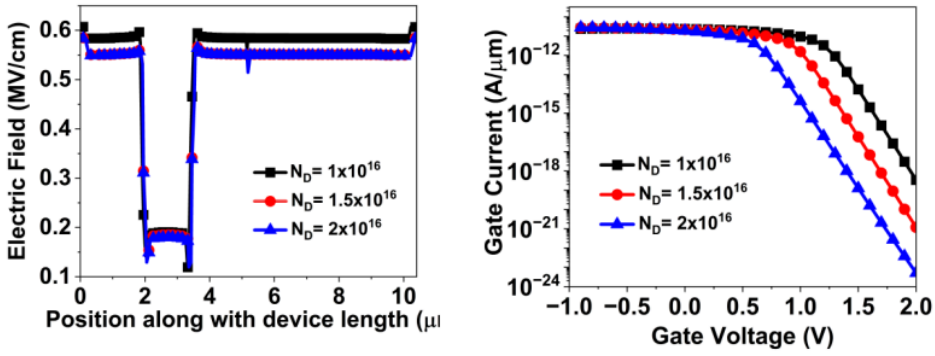
3.3.2 Results and Discussion

This section explores the DC characteristics of the proposed GDHEMT, comparing them with those of the conventional device to evaluate performance differences. Fig. 3.9(a) illustrates the electric field characteristics of the GDHEMT for various doping concentrations in the GaN channel layer. The incorporation of the Gaussian doping technique introduces donor impurities into the channel, creating a smooth doping profile that minimizes electric field variations at the channel interface. A higher

donor concentration (N_D) increases charge density and ensures a more uniform distribution of charge carriers, effectively reducing gate leakage current and improving the device's off-state performance, as presented in Fig. 3.9(b).

Table 3.3: The structural parameters of the proposed GD-HEMT

S.No.	Parameter	Value
1.	p-GaN layer thickness (T_{GaN})	110 nm
2.	AlGaN barrier layer thickness ($T_{AlGaNbarrier}$)	15 nm
3.	GaN channel layer thickness ($T_{GaNchannel}$)	85 nm
4.	GaN buffer layer thickness ($T_{GaNbuffer}$)	2 μm



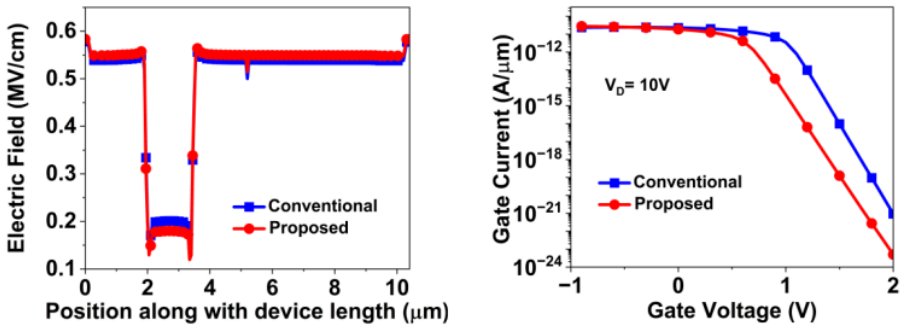
(a) (b)

Fig. 3.9: The comparison of the proposed GD-HEMT with respect to dopant concentration (a) the electric field and (b) the gate leakage current.

Fig. 3.10(a) presents the electric field distributions, highlighting the reduction of the electric field within the channel of the GDHEMT, achieved through Gaussian doping

of the channel layer. Consequently, as depicted in Fig. 3.10(b), the GDHEMT exhibits significantly lower gate leakage current compared to the conventional device, which lacks channel doping.

Fig. 3.11 compares the I_d-V_g characteristics, demonstrating that the GDHEMT outperforms the conventional p-GaN HEMT. The proposed device achieves a notably higher on-current and improved current drive capability. Fig. 3.12 compares the I_d-V_d characteristics of the GDHEMT and the conventional device, showing a maximum drain current ($I_{ds,max}$) of 0.75 A/µm for the GDHEMT, surpassing the 0.69 A/µm achieved by the conventional device. Table 3.4 provides a detailed comparison of the performance parameters of the proposed GDHEMT with those of previously reported devices.



(a) (b)

Fig. 3.10: (a) The electric field and (b) the gate leakage current comparison of the proposed and conventional device.

3.4 Omega(Ω)-Shaped gate p-GaN MIS-HEMT

This section focuses on the optimization and analysis of a novel p-GaN MIS-HEMT featuring an Omega (Ω)-shaped gate structure that encapsulates the dielectric layer above the p-GaN layer. This design effectively reduces stress on the gate dielectric, ensuring a more uniform stress distribution, minimizing the risk of dielectric

breakdown, and enhancing device reliability. The increased distance between the Ω-shaped gate and the channel reduces gate leakage current, lowering power consumption. Optimization efforts targeted key design parameters, including gate dielectric thickness, length, and material, to achieve optimal performance. Simulation results, validated through experimental calibration, indicate that increasing the gate dielectric thickness improves threshold voltage, reduces gate leakage current, and enhances breakdown voltage. Extending the gate dielectric length further enhances threshold voltage and breakdown voltage, while selecting a high-k dielectric material significantly boosts breakdown voltage. The comparison of the proposed device with state-of-the-art devices indicates that the proposed device is superior in terms of improved breakdown voltage, higher threshold voltage, and reduced gate leakage current. Furthermore, a detailed sequence of fabrication steps has been outlined for practical realization.

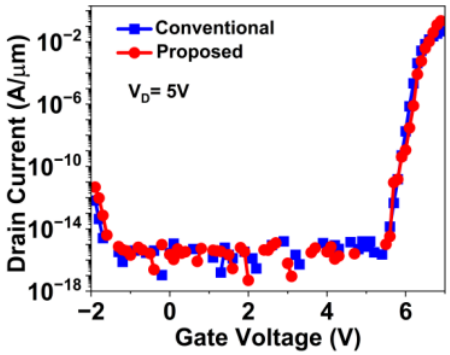


Fig. 3.11: I_d-V_g comparison of the proposed GD-HEMT and the conventional device

3.4.1 Device structure, simulation setup, calibration, and fabrication

The proposed device, depicted in Fig. 3.14, features an Ω-shaped gate encircling the dielectric layer above the p-GaN layer. The structure consists of multiple layers, including a 110 nm thick p-GaN layer, a 15 nm thick AlGaN barrier, an 85 nm thick

GaN channel, a 2 µm thick GaN buffer, and a 165 nm thick SiN passivation layer. It also incorporates three electrodes for the source, gate, and drain. The AlGaN barrier

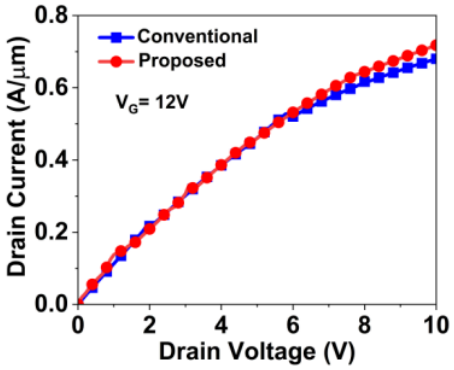


Fig. 3.12: I_d-V_d comparison of the proposed GD-HEMT and the conventional device

Table 3.4: Comparison of performance parameters of the proposed GD-HEMT with the reported devices

Reference	Gate Leakage Current (A/μm)	$I_{ds,max}$ (A/μm)	g_m (S)
[3]	10^{-15}	0.35	-
[4]	10^{-18}	0.8	-
[5]	10^{-17}	0.7	0.6
Conventional p-GaN HEMT	10^{-21}	0.6	0.2
This work	**10^{-23}**	**0.75**	**1**

layer contains 30% Aluminum, and the p-GaN layer has a doping density of $3\times10^{15}/cm^3$. Fabrication of the proposed device follows a CMOS-compatible process, outlined in Fig. 3.15(a) to 3.15(g). The layers, including the 110 nm p-GaN layer, 15 nm AlGaN barrier, 85 nm GaN channel, and 2 µm GaN buffer, are grown via metal-organic chemical vapor deposition (MOCVD), as shown in Fig. 3.15 (a).

Device isolation is achieved using Cl_2/BCl_3-based ICP-RIE, depicted in Fig. 3.15(b). Ohmic contacts are deposited for the source and drain, as shown in Fig. 3.15(c). The gate dielectric (HfO_2) is grown exclusively over the p-GaN cap region through a controlled deposition process. After the p-GaN layer is formed, an omega-shaped etching process is used to define the gate structure. The gate dielectric is deposited only on the p-GaN cap area, leaving other regions exposed, as shown in Fig. 3.15(d) and Fig. 3.15(e). Following this, metal (Ni/Au) is deposited to form the gate, and a self-alignment process ensures precise alignment with the etched features, eliminating additional masking steps, as illustrated in Fig. 3.15(f). Annealing enhances the metal-semiconductor interface properties for optimal device performance. Finally, a SiN_x passivation layer is deposited using plasma-enhanced chemical vapor deposition (PECVD), as shown in Fig. 3.15(g). This fabrication process enables precise gate dielectric coverage and alignment, optimizing the characteristics of the Ω-shaped p-GaN MIS-HEMT.

3.4.2 Results and Discussion

This section conducts a thorough analysis focused on enhancing the essential performance metrics of the proposed device. The target parameters for improvement include the breakdown voltage, threshold voltage, and gate leakage current. The optimization strategy systematically investigates the gate dielectric properties, specifically its length, thickness, and dielectric constant. By strategically varying these parameters, the study evaluates their influence on the device's performance and operational characteristics. The objective is to determine the most effective configuration that increases breakdown voltage, refines threshold voltage, and minimizes gate leakage current, ultimately improving the device's efficiency and reliability.

3.4.2.1 Effects of variation in the gate dielectric material

The influence of varying the dielectric constant of the gate dielectric material on the device's performance is analyzed. The materials considered in the simulation include SiN, Al_2O_3, SnO_2, and HfO_2. An increase in the dielectric constant of the gate

dielectric layer leads to an enhancement in the device's breakdown voltage, as reported in [6]. This relationship between the breakdown voltage and the dielectric layer material is illustrated in Fig. 3.16(a). A higher dielectric constant reduces theimproving the breakdown voltage. electric field stress across the dielectric layer at a given voltage as depicted in Fig 3.16(b).

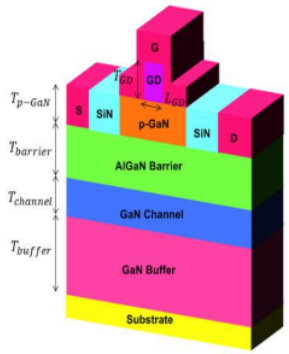


Fig. 3.14: The structure of the proposed device

3.4.2.2 Effects of scaling the thickness of gate dielectric

Fig. 3.17(a) illustrates the transfer characteristics of the proposed device with variations in gate dielectric thickness (T_{GD}) ranging from 20 nm to 60 nm. A thicker dielectric layer increases the physical separation between the gate metal and the GaN channel, making it more challenging for electrons to tunnel through the barrier. This results in a higher threshold voltage, reflecting improved gate control, as shown in Fig. 3.17(b). Additionally, the threshold voltage is inversely related to the gate capacitance. As the dielectric thickness increases, the gate capacitance decreases, as indicated in Fig. 3.17(c). This decrease in capacitance leads to a rise in the device's threshold voltage [4]. However, the dielectric thickness does not affect parameters such as electron mobility in the GaN channel, the carrier concentration in the 2DEG, or the drain voltage, leaving the on-current unchanged at 300 mA/mm.Fig. 3.18(a)

demonstratesthat increasing the dielectric thickness from 20 nm to 60 nm reduces the gate leakage current [7]. A thicker dielectric layer lowers the probability of electron tunneling through the barrier, reducing gate leakage. Furthermore, field emission becomes a significant contributor to gate leakage in thicker dielectrics. Field

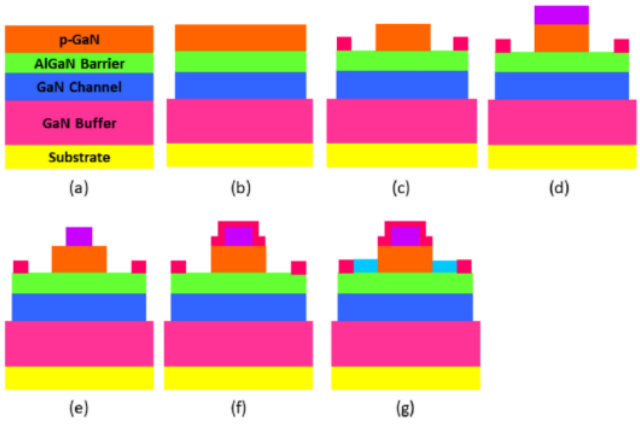


Fig. 3.15: The fabrication process for the proposed device

emission involves electron ejection from the semiconductor into the dielectric under a high electric field. As dielectric thickness increases, the electric field intensity diminishes, decreasing the likelihood of field emission, as depicted in Fig. 3.18(b).Fig. 3.19(a) shows the dependence of gate leakage current on the temperature of the proposed device. When the temperature rises from 280 K to 400 K in 20 K increments, carriers in the GaN layer gain thermal energy, increasing their ability to tunnel through the dielectric, which raises the gate leakage current. Additionally, higher temperatures amplify lattice vibrations in the GaN layer, creating extra states in the bandgap and increasing tunneling opportunities through the dielectric, contributing to higher gate leakage. Fig. 3.19(b) highlights the relationship between dielectric thickness and breakdown voltage. As the thickness of the gate dielectric layer increases, the breakdown voltage also rises [7]. A thicker dielectric layer ensures a more uniform electric field distribution across its volume. The increased

thickness spreads the electric field lines over a larger distance, reducing localized field intensities and enhancing the breakdown voltage.

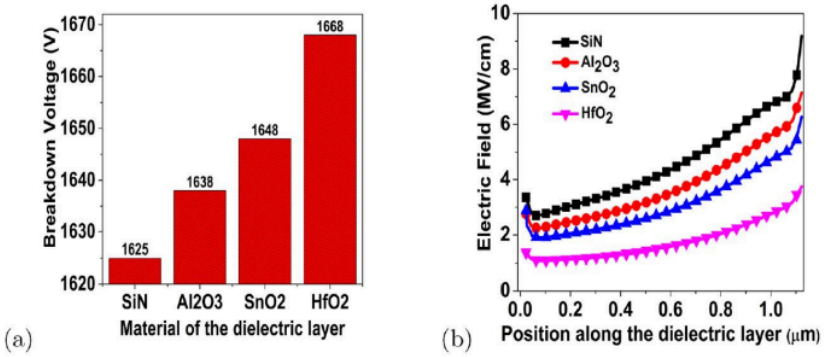


Fig. 3.16: Impact of different gate dielectric materials on (a) breakdown voltage and (b) electric field of the proposed device

3.4.2.3 Effects of variation in the gate dielectric length

This section compares the performance of the device for different gate dielectric lengths (L_{GD}), as illustrated in Fig. 3.20(a)-(b) and Fig. 3.21(a)-(b). The optimized gate dielectric thickness, determined as 60 nm in the previous section, is maintained constant, while four different gate dielectric lengths are analyzed: 0.08, 0.10, 0.12, and 0.14 μm. Fig. 3.20(a) shows the transfer characteristics of the device for varying dielectric lengths, and Fig. 3.20(b) highlights an increase in the threshold voltage with longer gate dielectric lengths. This behavior is explained by a conceptual model. Since the threshold voltage is inversely related to gate capacitance, an increase in dielectric length reduces the capacitance between the gate and the p-GaN layer, as demonstrated in Fig. 3.21(a). This decrease in capacitance results in a higher threshold voltage. Additionally, a longer dielectric weakens the electric field strength between the gate and the GaN channel layer. This reduced field strength lowers the gate's control over the charge carriers in the GaN channel, necessitating a higher gate voltage for effective modulation, thereby increasing the threshold voltage. However, parameters such as electron mobility in the GaN channel, carrier concentration in the

2DEG, and drain voltage remain unaffected by dielectric length, keeping the on-current constant at 300 mA/mm. Fig. 3.21(b) indicates that increasing the dielectric length also improves the breakdown voltage. A longer dielectric length reduces the electric field intensity near the edges of the p-GaN layer, resulting in a more uniform electric field distribution. This mitigates the formation of localized high electric fields, which could otherwise lead to breakdown [8]. Consequently, the reduced field concentration at the p-GaN edges contributes to an enhanced breakdown voltage. Based on these findings, the optimal values for the gate dielectric thickness (T_{GD}) and length (L_{GD}) are determined to be 60 nm and 0.14 μm, respectively. Additionally, HfO_2 is identified as the most suitable gate dielectric material for the proposed device. Thus, the optimized configuration consists of T_{GD} = 60 nm, L_{GD} =

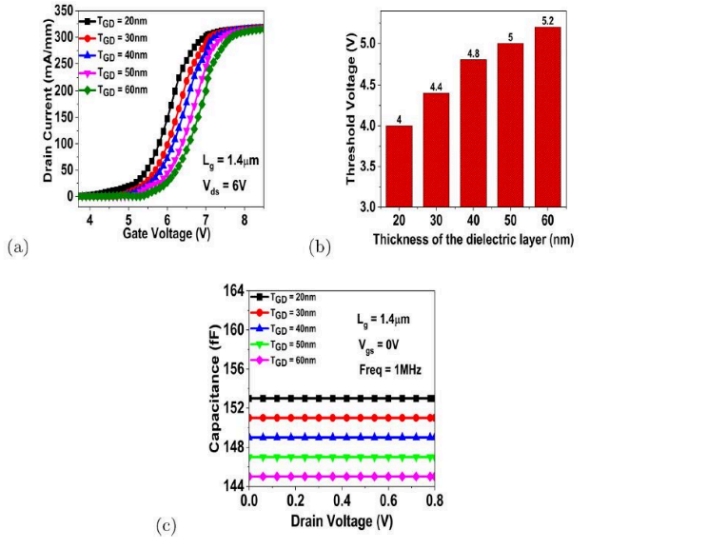


Fig. 3.17: Impact of different gate dielectric thicknesses on (a) transfer characteristics, (b) threshold voltage and (c) c-v characteristics of the proposed device.

Table 3.5: Performance Comparison of the Proposed Device for varying gate dielectric thicknesses.

Gate Dielectric Thickness (nm)	Specific On-Resistance ($m\Omega \cdot cm^2$)	Breakdown Voltage (V)	BFOM (GW/cm^2)
60	3.33	1668	0.8355
50	3.33	1659	0.8265
40	3.33	1650	0.8175
30	3.33	1641	0.8086
20	3.33	1632	0.7998

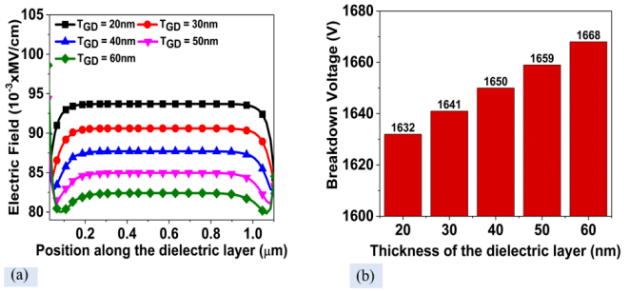


Fig. 3.18: Impact of different gate dielectric thicknesses on (a) I_g-V_g characteristics and (b) electric field of the proposed device.

0.14 μm, and HfO_2 as the gate dielectric. Table 3.5 and Table 3.6 presents the performance comparison of the proposed device for varying gate dielectric thicknesses and lengths, respectively.

As summarized in Table 3.7, the proposed device demonstrates a high breakdown voltage, positioning it as a strong candidate for high-power electronics applications. Moreover, significant improvements in gate leakage current and threshold voltage are achieved compared to previously reported GaN HEMT-based devices.

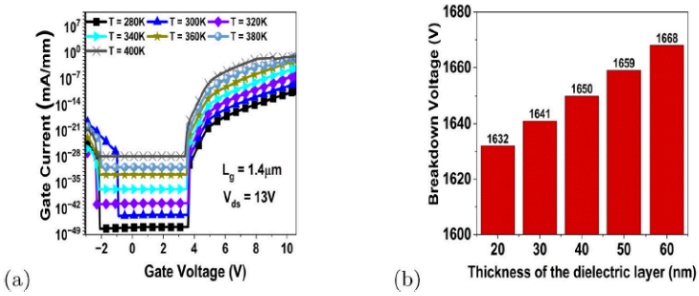


Fig. 3.19: (a) I_g-V_g characteristics of the proposed device with respect to temperature and (b) Impact of different gate dielectric thicknesses on breakdown voltage of the proposed device.

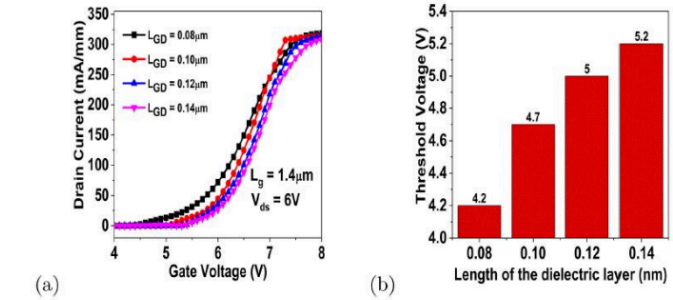


Fig. 3.20: Impact of different gate dielectric lengths on (a) I_d-V_g characteristics and (b) threshold voltage of the proposed device.

3.5 Summary

This chapter explores the design, optimization, and performance of novel enhancement-mode GaN HEMTs to reduce gate leakage current. Three advanced architectures—MGHEMT, GDHEMT, and Ω-shaped gate p-GaN MIS-HEMT—are

investigated. The MGHEMT reduces gate leakage by 14% and improves threshold voltage by 50%, while the GDHEMT achieves a 27% gate leakage reduction and 67% transconductance enhancement. The Ω-shaped gate p-GaN MIS-HEMT optimizes dielectric properties by reducing gate leakage current, increasing threshold voltage, and improving breakdown voltage compared to state-of-the-art devices.

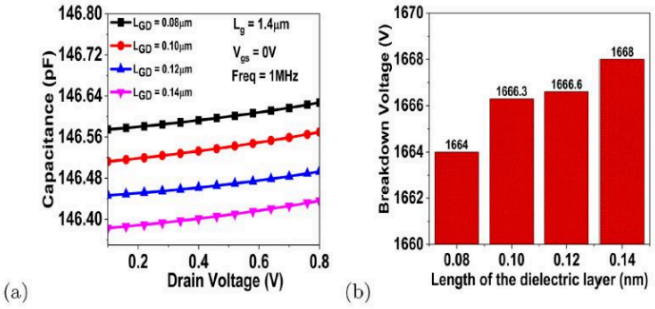


Fig. 3.21: Impact of different gate dielectric lengths on (a) C-V characteristics and (b) breakdown voltage of the proposed device.

Table 3.6: Performance Comparison of the Proposed Device for varying gate dielectric lengths.

Gate Dielectric Length (μm)	Specific On-Resistance (mΩ·cm²)	Breakdown Voltage (V)	BFOM (GW/cm²)
0.14	3.33	1668	0.8355
0.12	3.33	1666.6	0.8341
0.10	3.33	1666.3	0.8338
0.08	3.33	1664	0.8315

Table 3.7: Performance comparison of the proposed device with the state-of-the-art devices in the literature.

Parameters	In-Situ AlN/p-GaN Gate HEMT [9]	$Al_{0.25}Ga_{0.75}N$/AlN/ $Al_xGa_{(1-x)}N$/GaN MIS-HEMT [10]	Drain Field Plate Structure with Passivation Dielectrics [11]	This work
Threshold Voltage (V)	3.9	3	9.1	**5.2**
Min Gate Leakage Current (mA/mm)	10^{-16}	10^{-26}	-	**10^{-41}**
Breakdown Voltage (V)	1380	600	1587	**1668**

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CHAPTER 4

MINIMIZING ON-RESISTANCE FOR ENHANCED DEVICE PERFORMANCE

4.1 Introduction

GaN-based HEMTs are extensively utilized in high-power and high-frequency applications due to their remarkable properties, including low on-resistance, high current capacity, and rapid switching speed [1]. These advantages are attributed to the formation of a high-density two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction [2]. Despite their extensive commercial applications, AlInN/GaN-based HEMTs are gaining research attention because of their enhanced performance compared to traditional AlGaN/GaN HEMTs [3]. This interest arises from limitations in AlGaN HEMTs, such as lattice mismatch-induced strain and adverse polarization effects, which can degrade frequency response and increase current collapse [4]. Additionally, the negative surface states and polarization effects in AlGaN/GaN HEMTs negatively impact drain current, compromising device reliability and stability [5], [6].

To address these challenges, researchers are exploring heterostructures that combine AlN and InN [7]. AlInN/GaN HEMTs show the potential to outperform conventional AlGaN/GaN HEMTs, offering higher 2DEG charge densities due to their larger bandgap and stronger polarization effects [8]. The spontaneous polarization in AlInN can induce up to three times more charge, resulting in higher current density in the epitaxial layer without mechanical constraints. While normally-off HEMTs with superlattice AlGaN/GaN channels have demonstrated high on-current density and threshold voltage [9], achieving the required 2DEG density in AlGaN HEMTs necessitates a high AlN content in the barrier layer, which complicates material growth [10].

To overcome these limitations, a single heterojunction AlInN/GaN HEMT was introduced, which forms a negative polarization charge, thereby reducing the equilibrium carrier concentration in the channel [11]. Furthermore, a high-performance multi-channel AlInN/GaN heterostructure has been developed, featuring five stacked heterojunctions that enhance 2DEG density and reduce sheet resistance (R_{sh}). Compared to AlGaN/GaN devices with an equivalent number of heterojunctions, AlInN/GaN devices achieve better R_{sh}. The lattice-matched AlInN barrier and GaN channel also mitigate strain-induced defects caused by piezoelectric effects, leading to lower on-resistance (R_{on}) and improved current drive efficiency. However, these multi-channel AlInN/GaN HEMTs exhibit higher gate leakage current than their AlGaN/GaN counterparts. To address this, a GaN cap layer was incorporated into AlInN/GaN HEMTs to reduce gate leakage by minimizing the thermionic emission and tunneling components. Although this approach slightly reduces the transconductance peak, it improves device performance by decreasing gate leakage [13]. Further optimization is necessary to enhance the current drive efficiency, transconductance (g_m), on-resistance (R_{on}), and gate leakage.

This study proposes a novel enhancement-mode p-GaN HEMT featuring a double AlInN/AlN/GaN heterostructure with a quaternary InAlGaN back-barrier. This is the first design that integrated a p-GaN layer and InAlGaN back-barrier within a double AlInN/AlN/GaN heterostructure. The p-GaN layer enables normally-off operation by creating a depletion region at the heterojunction between the gate and channel, thereby modulating the 2DEG and controlling channel current. The stacked double AlInN/AlN/GaN heterostructure facilitates 2DEG formation at the layer interfaces, resulting in high 2DEG density and mobility, which in turn reduces resistance and enhances current drive efficiency. The addition of an InAlGaN back-barrier significantly improves channel current effectively.

4.2 Device structure, simulation setup, calibration, and fabrication

The schematic of the proposed device is shown in Fig. 4.1, which incorporates a p-GaN gate, a double AlInN/GaN heterojunction, and a quaternary InAlGaN back-

barrier. The double heterostructure consists of an 8 nm AlInN barrier layer positioned above an AlN spacer layer and a GaN channel measuring 1 nm and 30 nm in thickness, respectively. The AlInN barrier layer features a wider bandgap and lower electron affinity compared to the GaN channel layer. The conduction band offset, combined with the differences in spontaneous and piezoelectric polarization between the barrier and channel layers, creates a quantum well at the heterointerface. This well traps electrons (forming the 2DEG) and establishes the channel. An AlN spacer is incorporated between the barrier and channel layers to minimize ionized impurity scattering. The InAlGaN back-barrier and Fe-doped GaN buffer layer are 4 nm and 2 µm thick, respectively. The back-barrier raises the conduction band, reducing leakage pathways beneath the buffer layer and confining the 2DEG within the channel. The GaN buffer layer is included to facilitate heat dissipation. Additionally, a silicon nitride (SiN) passivation layer is applied to the device structure. The p-GaN gate is doped with Mg at a concentration of 8.5×10^{17} cm^{-3}, while the GaN buffer is doped with Fe at 2.6×10^{16} cm^{-3}.

Fig. 4.1: Schematic of the proposed structure

The fabrication process for the proposed device follows a CMOS-compatible workflow, as illustrated in Figs. 4.2(a)–(f). The p-GaN HEMT features an AlInN/AlN/GaN double heterostructure along with an InAlGaN back-barrier, which

is grown using metal-organic chemical vapor deposition (MOCVD). The epitaxial layers comprise an 8 nm AlInN barrier layer, a 1 nm AlN spacer layer, a 30 nm GaN channel layer forming the double heterostructure, a 4 nm InAlGaN layer, and a 2 µm GaN buffer layer, as shown in Fig. 4.2(a). Device mesa isolation is carried out using dry etching with a Cl_2/BCl_3-based inductively coupled plasma reactive ion etching (ICP-RIE) process, as depicted in Fig. 4.2(b) [14]-[16]. Ohmic contacts for the source and drain are formed using e-beam evaporation after selectively etching the p-GaN layer with plasma, as illustrated in Figs. 4.2(c) and 4.2(d) [17]. These ohmic contacts are optimized by performing rapid thermal annealing at 780°C for 30 seconds in a nitrogen atmosphere [18], [19]. A SiN_x passivation layer is deposited via plasma-enhanced chemical vapor deposition (PECVD) following the definition of the gate foot using electron beam lithography (EBL), as depicted in Figs. 4.2(e) and 4.2(f).

4.3 Results and Discussion

4.3.1 DC and AC behavior of the proposed device for different InAlGaN thickness

This section explores the device's performance in terms of its DC and AC characteristics. Fig. 4.3 illustrates the output characteristics of the proposed device for varying InAlGaN thicknesses, highlighting that the maximum drain current is achieved with a 4 nm thickness. At this thickness, the device exhibits a drain current (I_D) of 1.99 A/mm. The high drain current is attributed to several factors, including the excellent electron mobility of the AlInN/GaN material system, the significant barrier height of the AlInN/GaN heterojunction, and the thin channel design. The high electron mobility of AlInN/GaN facilitates rapid charge transport, enabling high-speed operation. Additionally, the substantial barrier height at the AlInN/GaN interface enhances electron injection efficiency from the source into the channel, while the thin channel structure minimizes resistance to electron flow, further enhancing I_d [20]. The I_d-V_g characteristics of the proposed device, shown in Fig. 4.4, also indicate optimal performance at an InAlGaN thickness of 4 nm, yielding the

highest on-current. A thinner InAlGaN back-barrier improves the current-voltage characteristics by enhancing electron transport and reducing electron scattering. This

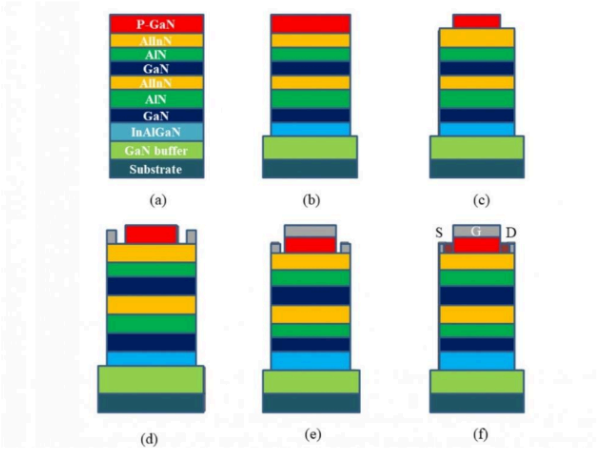


Fig. 4.2: Fabrication steps of the proposed device (a) Starting wafer (b) mesa isolation by dry etching (c) p- GaN layer etching (d) ohmic contact formation of source-drain(e) gate contact formation (f) passivation with deposited SiN layer

results in decreased resistance and higher electron mobility [21]. Fig. 4.5 presents the capacitance-voltage (C-V) characteristics of the HEMT, with the best results observed at an InAlGaN thickness of 4 nm. The thinner back-barrier increases the effective channel width, thereby altering the parasitic capacitances of the device compared to other thicknesses [22].

Lower parasitic capacitances reduce power consumption since less charge is required to maintain the gate voltage. This reduction leads to improved energy efficiency and high switching speeds, as the removal of stored charge allows the device to switch more rapidly [12]. As shown in Fig. 4.6, the gate leakage current is minimized in the proposed device due to the wide bandgap of the InAlGaN layer. This layer acts as a

barrier, increasing the electron barrier height and effectively suppressing electron leakage [23].

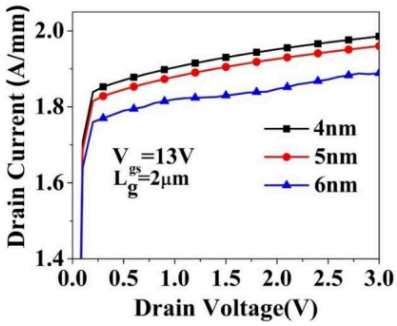


Fig. 4.3: I_d-V_d characteristics of the proposed device for different values of InAlGaN thickness.

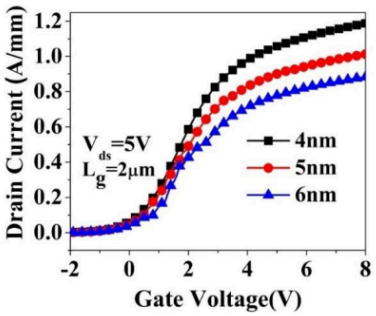


Fig. 4.4: I_d-V_g characteristics of the proposed device for different values of InAlGaN thickness.

4.3.2 Optimized performance parameters of the proposed device

The optimization was performed to achieve the best device performance by minimizing R_{on} and maximizing I_{ds}. A lower R_{on} reduces energy losses during

conduction, while a higher I_{ds} enhances the device's current drive efficiency. To evaluate these parameters, simulations were performed for varying thicknesses of the InAlGaN back-barrier layer. The thickness of this layer has a substantial impact on the electrical properties of the device. A thinner back-barrier facilitates better electron transport, resulting in lower R_{on} and higher I_{ds}. Conversely, a thicker back-barrier diminishes electron transport, increasing R_{on} and decreasing I_{ds}. This behavior is attributed to the improved electron transport and confinement in the channel region for a thinner back-barrier layer [24].

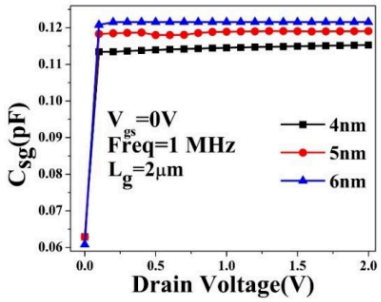


Fig. 4.5: The capacitance-voltage characteristics of the proposed device for different values of InAlGaN thickness

The simulations considered back-barrier thicknesses ranging from 4 nm to 6 nm, in 1 nm increments, while keeping other device parameters constant. Fig. 4.7 demonstrates the variations in R_{on} and I_{ds} with different back-barrier thicknesses. The results show that the optimal R_{on} of approximately 1.507 Ω·mm and the highest I_{ds} of about 1.99 A/mm are achieved at a thickness of 4 nm. Further simulations were conducted to analyze the DC performance parameters of the optimized device.

Figs. 4.8(a) and 4.8(b) reveal a high electron concentration in the channel regions. Figure 4.9 shows significant electron concentration near the interfaces of the heterostructures, with an interface charge density of approximately 9.8×10^{13} cm^{-3}.

This high electron concentration is due to the formation of a two-dimensional electron gas (2DEG) at the AlInN/GaN interface. The AlInN layer acts as an electron barrier, while the GaN layer serves as a high-mobility channel. The difference in

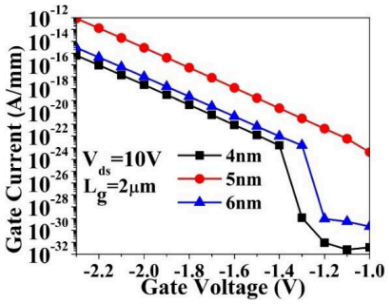


Fig. 4.6: The gate leakage current with respect to gate voltage of the proposed device for different values of InAlGaN thickness

electron affinities between AlInN and GaN causes electrons to accumulate at the interface, forming a 2DEG. This 2DEG creates a high-conductivity channel and enhances electron concentration. The quality of the AlInN/GaN interface also contributes to this phenomenon by reducing interface resistance and facilitating 2DEG formation. Fig. 4.10 confirms that the majority of current conduction occurs in the upper channel due to donor-like surface states near the upper channel. Fig. 4.11 highlights that the strong electric field is present within the channel, a result of the wide bandgap of the GaN layer and the high electron mobility of the 2DEG. This electric field improves device performance by increasing current density, reducing resistance, and lowering gate leakage. Fig. 4.12 presents the energy band diagram of the device in the on-state. The structure comprises a GaN layer sandwiched between AlInN and AlN layers. The bandgap differences between these materials create potential barriers that prevent electron and hole leakage, forming quantum wells at the heterojunctions. These quantum wells enhance 2DEG concentration, improving current capability and efficiency. Additionally, the valence band edge of the AlInN

Table 4.1: Performance Comparison of the Proposed Device for Varying InAlGaN Thicknesses.

InAlGaN Thickness (nm)	Specific On-Resistance ($m\Omega \cdot cm^2$)	Breakdown Voltage (V)	BFOM (GW/cm^2)
4	1.507	2010	2.6808
5	1.531	1800	2.116
6	1.584	1500	1.420

Table 4.2: The parameter comparison of the proposed and state-of-the-art devices.

R_{on} ($m\Omega.cm^2$)	I_{ds} (A/mm)	V_{th} (V)	g_m (mS/mm)	Ref
12.5	0.473	-9.2	97.9	**[9]**
10	0.355	1.1	-	**[10]**
-	0.6	0.9	300	**[26]**
1.507	**1.99**	**0.2**	**354**	**This work**

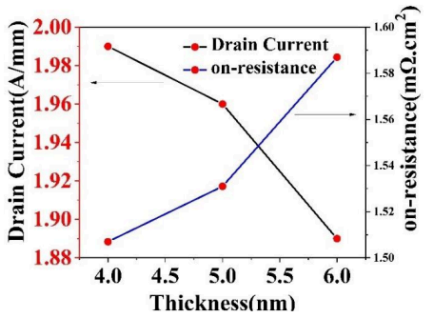
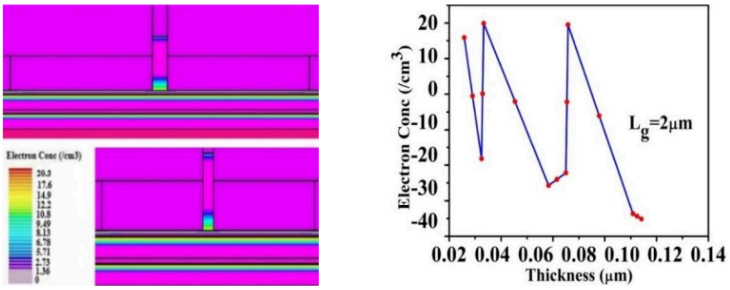


Fig. 4.7: Optimization of the proposed device for InAlGaN thickness of 4 nm, 5 nm and 6 nm with respect to on-resistance and drain current.



(a) (b)

Fig. 4.8: The electron concentration in the proposed device (a) Contour plot and (b) Graphical representation.

layer is higher than that of GaN, which prevents hole flow from GaN into AlInN. The double heterostructure of AlInN/AlN/GaN in the normally-off HEMT effectively confines electrons within the conduction channel, reducing gate leakage and enhancing device efficiency [25]. Table 4.1 presents performance comparison of the proposed device for varying InAlGaN thicknesses. Table 4.2 compares the proposed device's performance metrics with state-of-the-art devices, focusing on on-resistance (R_{on}), maximum drain current (I_{ds}), threshold voltage (V_{th}), and transconductance (g_m). The results show that the proposed p-GaN HEMT with an AlInN/AlN/GaN double heterostructure and InAlGaN back-barrier outperforms existing devices in terms of I_{ds}, R_{on}, and g_m; however, the threshold voltage (V_{th}) is better in previously reported devices.

4.4 Summary

In this chapter, a novel p-GaN HEMT incorporating an AlInN/AlN/GaN double heterostructure and an InAlGaN back-barrier has been successfully presented. Simulation results demonstrate a substantial enhancement in the on-resistance and maximum drain current of the proposed device. Specifically, the on-resistance and

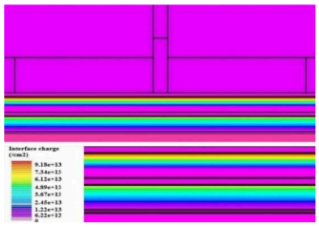


Fig. 4.9: Contour plot of the interface charge for the proposed device.

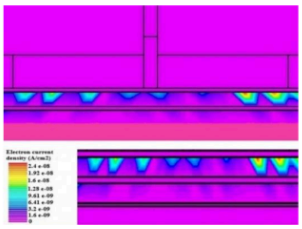
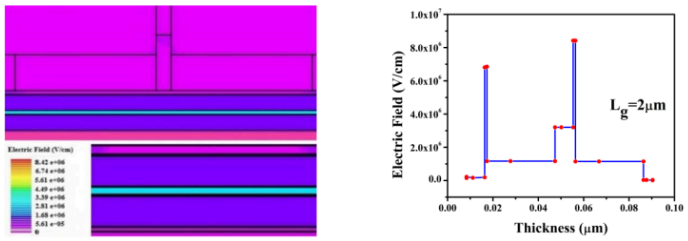


Fig. 4.10: Contour plot of the electron current density for the proposed device.



(a) (b)

Fig. 4.11: The electric field in the proposed device (a) Contour plot and (b) Graphical representation.

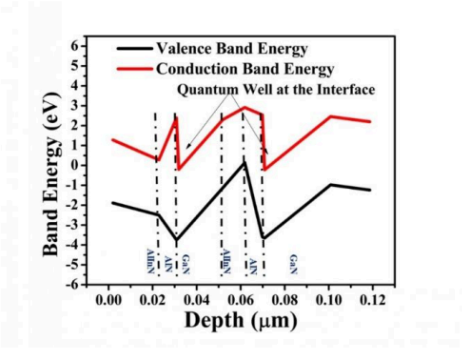


Fig. 4.12: On-state energy band diagram of the proposed device

maximum drain current show improvements of 85% and 231%, respectively, compared to existing devices. The device achieves a peak transconductance of 354 mS/mm and a threshold voltage of approximately 0.2 V. The proposed design also reduces power losses during switching, attributed to its low parasitic capacitance values. Additionally, the strong electric field generated within the device

4.5 References

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CHAPTER 5

ENHANCING BREAKDOWN VOLTAGE FOR IMPROVED EFFICIENCY AND PERFORMANCE

5.1 Introduction

The development of HEMTs has been driven by the growing need for devices capable of high-speed switching, high-power handling, and low-noise operation [1,2]. GaN-based HEMTs, in particular, are widely utilized in high-power and high-frequency applications due to their exceptional characteristics, including high breakdown voltage, low ON resistance, high current capabilities, and rapid switching [3,4]. Achieving a combination of high breakdown voltage and low ON-resistance (R_{on}) remains a key focus in power device research.

Numerous structural and material innovations have been introduced to improve the breakdown voltage of GaN HEMTs [5]. However, these new designs often come with their limitations. A significant challenge in GaN HEMTs under breakdown conditions is the issue of electric field crowding at the gate electrode. To address this, field-plate techniques have been employed, demonstrating notable effects in devices with short gate-drain distances [6]. However, in devices with longer gate-drain distances, the improvement in breakdown voltage is less pronounced. Incorporating an AlGaN back-barrier has also been explored to enhance breakdown voltage, but this approach does not fully mitigate electric field crowding and introduces a thermal barrier that adversely affects device performance under high-power conditions [7].

The HB-HEMT was developed by integrating a p-GaN gate and a hybrid AlGaN buffer consisting of two regions with different Al compositions (a and b). This design improved breakdown voltage and the Baliga figure of merit (BFOM), though it resulted in a slight reduction in the peak transconductance. Additionally, the HB-

HEMT exhibited high specific ON resistance and lower maximum drain current [8,9]. Subsequently, the PSAG-HEMT was introduced using hydrogen plasma treatment to enhance maximum drain current. Despite this improvement, its performance was temperature-sensitive, with the maximum drain current decreasing as temperature increased. The PSAG-HEMT also demonstrated a low threshold voltage and BFOM [10].

The S-HEMT, featuring a stepped hybrid GaN/AlN buffer layer, was another attempt to improve breakdown voltage. However, it faced challenges such as reduced threshold voltage, degraded specific ON resistance, and less favorable breakdown characteristics [3]. Overall, these earlier designs fell short of achieving significant advancements in breakdown voltage, BFOM, and threshold voltage for power electronics. Moreover, issues such as reduced transconductance, higher specific ON resistance, and lower maximum drain current persisted.

In this chapter, a novel device architecture called the stepped hybrid AlGaN buffer HEMT (STEPHB-HEMT) is proposed to enhance overall device performance. The STEPHB-HEMT introduces a stepped hybrid AlGaN buffer layer with reduced Al content, which minimizes surface defects. This design reduces buffer leakage current, leading to improved breakdown voltage. Compared to the conventional HB-HEMT, the proposed device demonstrates enhanced breakdown voltage and transconductance, along with reduced small-signal capacitances. The device models have been calibrated using experimental data to validate the simulation results. Additionally, fabrication steps have been proposed for the practical realization of the STEPHB-HEMT, and optimization strategies have been employed to achieve the best possible performance. The STEPHB-HEMT has been benchmarked against state-of-the-art devices, showing superior performance in key parameters.

5.2 Device structure, simulation setup, calibration, and fabrication

The schematic representations of the proposed STEPHB-HEMT and the conventional HB-HEMT are shown in Fig. 5.1(a) and Fig. 5.1(b), respectively. The STEPHB-HEMT incorporates a stepped hybrid AlGaN buffer layer, with the step

interface positioned between the gate and drain. The structure of the proposed device consists of several layers, including a 110 nm thick p-GaN layer, a 15 nm thick AlGaN barrier, an 85 nm thick GaN channel, a 2 μm thick hybrid AlGaN buffer, and a 300 nm thick SiN passivation layer.

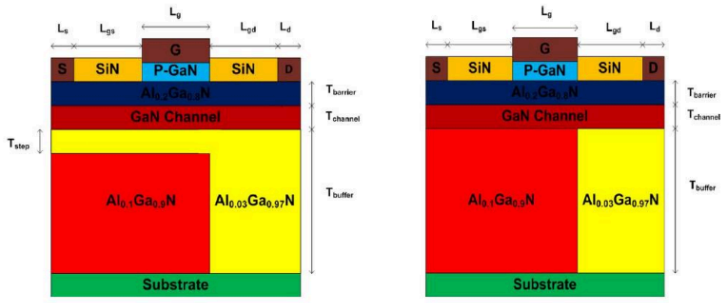

Fig. 5.1: The structure of (a) Proposed STEPHB-HEMT and (b) HB-HEMT

Table 5.1: The main structural parameters of the proposed STEP-HBHEMT device.

Parameters	Unit	Value	Description
L_s	μm	1	Source electrode length
L_g	μm	1.4	Gate electrode length
L_d	μm	1	Drain electrode length
L_{step}	μm	6.9	AlGaN step length
L_{gs}	μm	1	Gate-to-source distance
L_{gd}	μm	6	Gate-to-drain distance
$T_{p\text{-}GaN}$	nm	110	p-GaN layer thickness
$T_{barrier}$	nm	15	AlGaN barrier thickness
$T_{channel}$	nm	85	Thickness of the GaN channel
T_{buffer}	μm	2	Thickness of the buffer layer
T_{step}	μm	110-130	Thickness of the AlGaN step

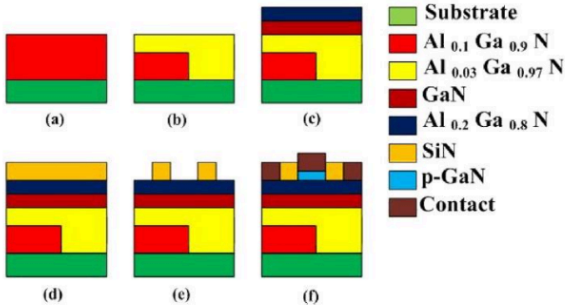

Fig. 5.2: Fabrication steps of the proposed STEPHB-HEMT (a) Starting wafer (b) partial etching of $Al_{0.1}Ga_{0.9}N$ (c) Growth of the GaN channel layer and the $Al_{0.2}Ga_{0.8}N$ barrier layer over $Al_{0.03}Ga_{0.97}N$ (d) deposition of the SiN passivation layer (e) selective plasma etching of a p-GaN layer (f) metallization of ohmic contacts.

Additionally, the device includes the gate, source, and drain electrodes. The aluminum composition in the AlGaN barrier is set at 20%, and the density of dopants in the p-GaN layer is 3×10^{17} cm^{-3}. Table 5.1 provides the primary structural parameters of the proposed device.

The fabrication process for the proposed device can be carried out using a CMOS-compatible flow, illustrated in Figs. 5.2(a)–5.2(f). Initially, the epitaxial structure of the p-GaN HEMT with an $Al_{0.1}Ga_{0.9}N$ buffer is grown using metal-organic chemical vapor deposition (MOCVD), as shown in Fig. 5.2(a) [11,12]. The subsequent step involves cleaning the sample with organic solvents, including acetone, isopropyl alcohol (IPA), and trichloroethylene (TCE). After cleaning, the sample is rinsed with de-ionized water and dried using a nitrogen blow. The $Al_{0.1}Ga_{0.9}N$ layer is partially etched using BCl_3 plasma reactive ion etching, as illustrated in Fig. 5.2(b). Next, the GaN channel layer and $Al_{0.2}Ga_{0.8}N$ barrier layer are grown on top of the $Al_{0.03}Ga_{0.97}N$ layer through MOCVD, as depicted in Fig. 5.2(c). A SiN passivation layer is then deposited using plasma-enhanced chemical vapor deposition (PECVD), as shown in

Fig. 5.2(d). Finally, selective plasma etching of the p-GaN layer is performed, followed by the formation of ohmic contacts through electron beam evaporation, as presented in Figs. 5.2(e) and 5.2(f).

5.3 Results and Discussion

This section examines the device's performance by analyzing its DC and AC characteristics. Additionally, a comparison has been made between the DC and AC properties of the conventional HB-HEMT and the proposed STEPHB-HEMT. The proposed device has also been optimized by varying the step thickness to attain optimal performance.

5.3.1. Comparison of the DC behavior of conventional HB-HEMT and proposed STEPHB-HEMT

This section discusses the DC behavior of the proposed device. The simulation of its DC characteristics considers an AlGaN buffer layer with a low aluminum (Al) content, which has a higher bandgap compared to an AlGaN buffer layer with a high Al content. A lower Al concentration in the buffer layer makes it more challenging for Ga atoms to diffuse through to the surface of the GaN layer. Consequently, the AlGaN buffer with low Al content proves more effective in minimizing surface defects [13]. Conversely, increasing the Al mole fraction in the buffer layer can result in more defects at the GaN layer surface [14], which negatively affects device performance by increasing the gate leakage current [15]. An increase in gate leakage current raises the electric field in the device, potentially lowering its breakdown voltage [16]. On the other hand, a low Al concentration reduces surface defects, subsequently decreasing leakage current and enhancing the breakdown voltage of the device. Figure 5.3(a) illustrates the electric field distribution at the breakdown for both the conventional HB-HEMT and the proposed STEPHB-HEMT. Incorporating a step in the low-Al-content AlGaN buffer in the proposed design alters the electric field distribution, effectively suppressing the electric field near the gate edge. This design modification mitigates the peak electric field at the drain-side edge of the

gate. Furthermore, the electric field near the drain edge of the gate is more concentrated in the HB-HEMT compared to the proposed device.

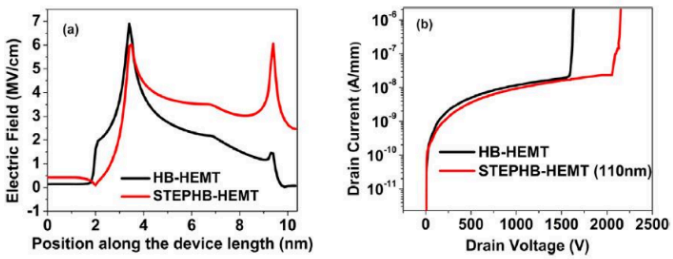

Fig. 5.3: Comparison between HB-HEMT and proposed STEPHB-HEMT with respect to (a) Electric field distribution and (b) Breakdown voltage

Consequently, the proposed STEPHB-HEMT achieves a higher breakdown voltage due to the reduced Al concentration in the AlGaN buffer step. Fig. 5.3(b) compares the breakdown characteristics of the HB-HEMT and STEPHB-HEMT with L_{gd} of 6 µm in the off-state. The STEPHB-HEMT's breakdown voltage is significantly higher, measured at 2149 V, compared to the conventional HB-HEMT.

Fig. 5.4 presents contour plots of the electron concentration for the HB-HEMT and STEPHB-HEMT. The variation in Al content within the AlGaN buffer of the STEPHB-HEMT results in differences in spontaneous and piezoelectric polarization. This leads to a non-uniform distribution of the 2DEG along the GaN channel, which modulates the electric field distribution under breakdown conditions. This enhanced electric field distribution contributes to the significantly higher breakdown voltage of the STEPHB-HEMT compared to the HB-HEMT [8]. Figs. 5.5(a) and 5.5(b) display the I_d–V_d and I_d–V_g characteristics, respectively. As the energy level of the buffer layer aligns with the GaN channel, a few electrons transfer from the channel to the buffer due to the 2DEG's high mobility. This electron transfer reduces the channel's electron density, subsequently lowering the drain current. To avoid such leakage, the AlGaN buffer should have a slightly higher energy level than the channel. The

reduced Al concentration in the AlGaN buffer enhances its energy level, increasing the 2DEG density and, thus, the drain current [17]. Figure 5.5(a) indicates that the proposed STEPHB-HEMT

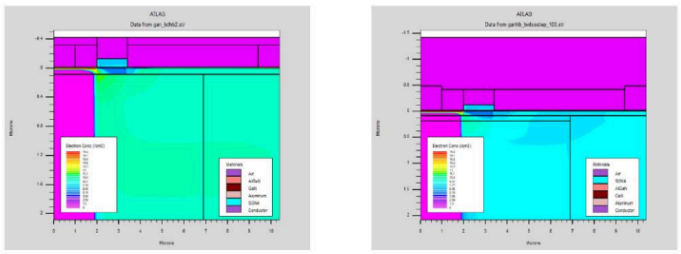

Fig. 5.4: Contour plot of electron concentration in (a) HB-HEMT and (b) Proposed STEPHB-HEMT

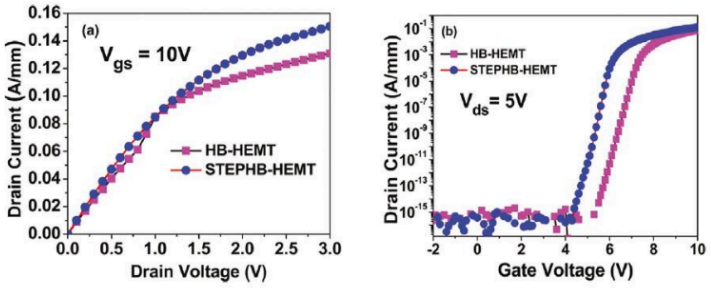

Fig. 5.5: The I-V characteristics of HB-HEMT and proposed STEPHB-HEMT (a) Output characterictics and (b) Transfer characteristics

achieves a higher maximum drain current ($I_{ds,max}$) of 150 mA/μm compared to 130 mA/μm for the HB-HEMT.

5.3.2. Comparison of the AC behavior of conventional HB-HEMT and proposed STEPHB-HEMT

The AC behavior of the proposed device is introduced by simulating capacitance-voltage (C-V) characteristics which are shown in Fig. 5.6 [17]. The simulation of three interelectrode capacitances, C_{gs}, C_{gd}, and C_{ds}, has been performed and converted into C_{oss}, C_{rss}, and C_{iss} as follows:

$$C_{oss} = C_{gd} + C_{ds} \tag{5.1}$$

$$C_{rss} = C_{gd} \tag{5.2}$$

$$C_{iss} = C_{gs} + C_{gd} \tag{5.3}$$

The AlGaN buffer step with a low aluminum mole concentration reduces the parasitic capacitances in a GaN HEMT by reducing the electric field strength [18]. The smaller values of C_{oss}, C_{rss}, and C_{iss} at V_{ds}=400 V for STEPHB-HEMT indicate that the charge stored in the parasitic capacitances is constantly replenished to maintain the gate voltage. This, in turn, results in decreased power consumption and increased efficiency. In addition, low parasitic capacitances can also provide high switching speed, as the charge stored in the capacitances is removed before the device can switch.

5.3.3 Optimization of the Device Design Parameters

This section focuses primarily on analyzing the breakdown voltage and power handling capabilities of the proposed device. To enhance the breakdown voltage, the step thickness in the AlGaN buffer layer was optimized. The breakdown voltage was evaluated for different step thicknesses (110 nm, 120 nm, and 130 nm) in the AlGaN buffer layer. A maximum breakdown voltage of 2149 V was achieved with a step thickness of 110 nm. This higher breakdown voltage is attributed to the lower electric field strength in thinner steps, which results in improved breakdown performance. The breakdown voltages of the STEPHB-HEMT for various step

thicknesses (T_{step}) are illustrated in Fig. 5.7(a), while Fig. 5.7(b) shows the optimization of breakdown voltage concerning T_{step}. The breakdown voltage values for different step thicknesses are summarized in Table 5.2.

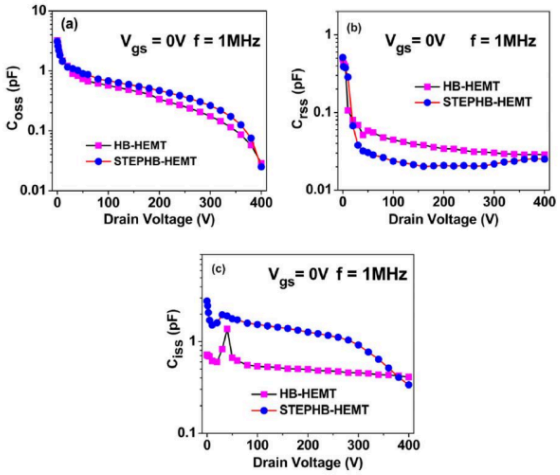

Fig. 5.6: The C-V characteristics of HB-HEMT and proposed STEPHB-HEMT with (a) C_{oss} (b) C_{rss} and (c) C_{iss}

Table 5.3 provides a comparison of the DC performance of the proposed structure with state-of-the-art devices. The results indicate that the p-GaN HEMT with the stepped hybrid AlGaN buffer demonstrates superior breakdown voltage, Baliga's figure of merit (BFOM), and threshold voltage compared to previously reported devices. These findings highlight the significant influence of the stepped hybrid AlGaN buffer on the electrical performance of p-GaN HEMTs.

5.4 Summary

This chapter successfully reports a novel p-GaN HEMT for high-power electronic applications. The proposed device incorporates a stepped hybrid AlGaN buffer layer,

and through the optimization of the step thickness, a remarkable 20% improvement in breakdown voltage is achieved compared to state-of-the-art devices.

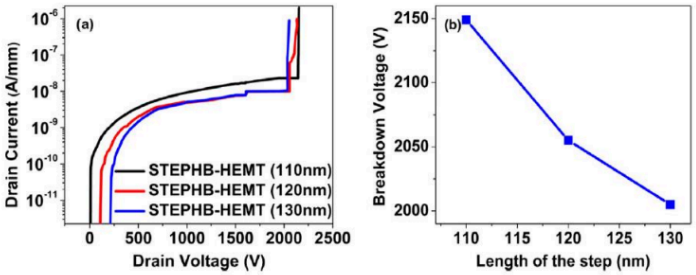

Fig. 5.7: The breakdown voltages of the STEPHB-HEMT with different values of the T_{step} and (b) Optimization of the STEPHB-HEMT at different values of T_{step} with respect to breakdown voltage

This significant increase in breakdown voltage is attributed to the redistribution of the electric field along the channel, resulting in enhanced performance. Furthermore, the proposed device demonstrates a 4% improvement in BFOM compared to existing devices, indicating enhanced power handling capabilities. Additionally, the device exhibits high transconductance and low small signal capacitances. Therefore, the results presented in this chapter demonstrate the promising potential of the proposed p-GaN HEMT with a stepped hybrid AlGaN buffer layer as a high-performance power electronic component.

Table 6.2: The values of breakdown voltage at different values of T_{step}.

Tstep (nm)	Breakdown voltage (V)
110	2149
120	2055
130	2005

Table 6.3: Performance comparison of the proposed STEPHB-HEMT with the state-of-the-art devices.

Parameters	HB-HEMT [8]	PSAG-HEMT [10]	S-HEMT [3]	STEPHB-HEMT (Proposed Device)
Breakdown Voltage (V)	1450	1449	1781	**2149**
$I_{ds,max}$ (A/mm)	0.6	0.245	0.254	**0.12**
Threshold Voltage (V)	1.7	0.8	1.1	**4.05**
ON-current (A/mm)	0.1	0.1	0.004	**0.1**
Ron (mΩ.cm^2)	0.47	2.73	4.42	**0.99**
BFOM (GW/cm^2)	4.47	0.769	0.72	**4.67**

5.5 References

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CHAPTER 6

ANALYTICAL MODELING OF BUFFER TRAP EFFECTS ON 2DEG DENSITY AND GATE LEAKAGE CURRENT AT CRYOGENIC TEMPERATURES

6.1 Introduction

GaN-based devices are highly attractive for power applications due to their exceptional material properties [1]-[5]. However, the normally-ON nature of GaN HEMTs poses challenges for reliable operation, necessitating a high threshold voltage [6]-[8]. The p-GaN gate approach [9] effectively achieves a reasonable threshold voltage, with cryogenic operation offering benefits such as reduced thermal noise, enhanced mobility, and improved reliability for high-power applications.

Nevertheless, the reliable operation of p-GaN HEMTs at room temperature is significantly impacted by buffer traps, particularly donor impurities within the GaN buffer. Li et al. showed that unionized donor traps slow electron release, increasing dynamic resistance and reducing 2DEG density [10], while Raja et al. reported that hot electron interactions with the buffer exacerbate trapping, leading to higher gate leakage currents and degraded dynamic ON resistance [11]. Although carbon doping improves breakdown voltage, it also introduces additional electron trapping, complicating the relationship between leakage current and 2DEG density [12]. Furthermore, donor-like defects and accumulated charges disrupt the p-GaN/AlGaN interface's electric field, causing threshold voltage instability and degrading long-term device reliability [13], [14].

To address these challenges, we present a model to optimize gate leakage current and 2DEG concentration in p-GaN HEMTs with acceptor buffer traps at cryogenic temperatures. The model, based on parameters such as Fermi level (E_F), trap concentration (N_T), and activation energy (E_T), incorporates self-consistent

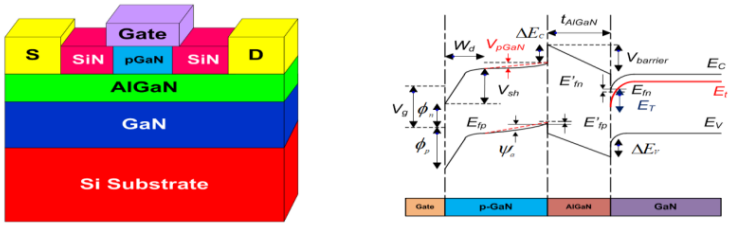
Schrödinger-Poisson solutions to analyze interface potentials and 2DEG behavior. .In contrast to previous analytical models for p-GaN HEMTs, which have been developed primarily for room-temperature operation and typically assume fully ionised dopants and temperature-independent trap charge, the present work introduces a cryogenic-temperature-aware framework. The model explicitly accounts for (i) the temperature dependence of buffer-trap occupancy via Eqs. (6.9)–(6.12), (ii) the cryogenic modification of permittivity and polarisation-induced voltage drops through Eqs. (6.3)–(6.7), and (iii) the resulting changes in both the 2DEG density and the electric-field-dependent gate leakage components. This enables a quantitative description of p-GaN HEMT behaviour from nominal down to cryogenic temperatures, which, to the best of our knowledge, has not been reported previously.By integrating leakage current mechanisms like thermionic emission, thermally assisted tunneling, and Poole-Frenkel emission, our approach demonstrates that buffer traps can enhance 2DEG density and mitigate leakage currents under extreme conditions. Our research significantly contributes to the existing literature on p-GaN HEMTs and provides valuable insights for the design and development of future enhancement-mode GaN devices in extreme temperature environments.

6.2 Device Schematic and Energy Band Diagram

Figure 6.1(a) illustrates the schematic of a conventional p-GaN HEMT, for which the proposed analytical model has been formulated. The device's epitaxial structure includes a 2 µm-thick Fe-doped GaN buffer layer grown on a silicon substrate, with N_a of 3×10^{13} cm^{-3}. Above this layer lies a 10 nm-thick AlGaN barrier, labeled as t_{AlGaN}. At the top of the structure is a heavily magnesium-doped p-GaN cap layer, with a thickness ($t_{p\text{-}GaN}$) of 70 nm and a doping level of 1×10^{19} cm^{-3}, which introduces acceptor-like characteristics. The model is developed using parameters sourced from prior research [15], as detailed in Table 6.1, along with several established physical constants.

Figure 6.1(b) shows the energy band profile extending from the gate down to the substrate. When a positive gate voltage (V_g) is applied to the Schottky contact

formed between the metal gate and the p-GaN layer, the junction becomes reverse-biased, causing an increase (ΔW) in the width of the depletion region within the p-GaN compared to the zero-bias condition. This widened depletion region enhances the injection of holes into the triangular quantum well at the p-GaN/AlGaN interface, leading to an increase in the 2DEG concentration in the channel. Although magnesium diffusion may slightly affect the electric field distribution in the AlGaN layer, the barrier's thinness and low doping concentration allow the field to be reasonably considered uniform. The applied gate voltage is partially dropped across the AlGaN barrier, while the remainder modulates the depletion region, facilitating the generation of both electron and hole gases. As indicated in Fig. 6.1(b), the trap energy level E_t closely follows the conduction band edge E_C but its position relative to the Fermi level E_F varies with depth and temperature. Traps located below E_F are ionised and contribute a positive space charge in the buffer, which in turn modifies the band bending and the 2DEG density at the AlGaN/GaN interface.



(a) (b)

Fig. 6.1 (a) Schematic and (b) Energy band diagram for the p-GaN HEMT at ON-state.

6.3 Model Formulation

6.3.1 Model Electrostatics for Buffer Traps at Cryogenic Temperatures

In the case of the p-GaN HEMT, the channel charge density is represented by n (cm^{-2}), while the trap electron density within the GaN layer is denoted as n_{trap} (cm^{-2}). The

density of trapped electrons is influenced by several factors, including the Fermi level (E_F), trap concentration (N_T), and trap activation energy (E_T) [16]. The charge density for the p-GaN HEMT, determined through a self-consistent solution of the Schrödinger-Poisson equations, is expressed as [17]

$$n + n_{trap} = R\left(V_G - V_{OFF} - \frac{E_F}{q}\right) \tag{6.1}$$

where

$$R = \frac{1}{q\left(\frac{t_{AlGaN}}{\epsilon_{AlGaN,cryo}} + \frac{t_{p-GaN}}{\epsilon_{GaN,cryo}}\right)} \tag{6.2}$$

A detailed derivation of Eq. (6.1) from the coupled Schrodinger—Poisson equations is provided in Appendix A. Here, E_F represents the Fermi level measured relative to the conduction band edge (E_C) at the heterojunction interface. V_G denotes the externally applied gate voltage, while V_{OFF} refers to the threshold voltage. The threshold voltage, V_{OFF}, is defined as the minimum gate voltage necessary to establish a conductive channel between the source and drain terminals. It is expressed as follows [18]

$$V_{OFF} = -\left(\phi_{cryo} + \frac{\sigma_{p-GaN} t_{p-GaN}}{\epsilon_{GaN,cryo}} + \frac{qN_D t_{AlGaN}^2}{2\epsilon_{AlGaN,cryo}} - V_{pz,cryo}\right) \tag{6.3}$$

where

$$V_{pz,cryo} = v_0\left(1 + \alpha_{pz,AlGaN}\Delta T\right) \tag{6.4}$$

$$\epsilon_{AlGaN,cryo} = \epsilon_{AlGaN}(1 + \beta_{AlGaN}\Delta T) \tag{6.5}$$

$$\epsilon_{GaN,cryo} = \epsilon_{GaN}(1 + \beta_{GaN}\Delta T) \tag{6.6}$$

and

$$\Delta T = \left|\frac{T_{dev}}{T_{norm}} - 1\right| \tag{6.7}$$

Here, ϕ_{cryo} denotes the Schottky barrier height at the cryogenic device temperature T_{dev} ; its temperature dependence is given explicitly in Eq. (6.17) as $\phi_{cryo} = \phi_p\,(1 + \alpha_p\Delta T)$. Here, $v_0 = \frac{\sigma_{AlGaN}\, t_{AlGaN}}{\epsilon_{AlGaN,cryo}}$, t_{p-GaN} is the thickness, σ_{p-GaN} is the polarization

charge and $\epsilon_{GaN,cryo}$ is the permittivity of the p-GaN layer at cryogenic temperature. Moreover, t_{AlGaN} is the thickness, σ_{AlGaN} is the polarization charge and $\epsilon_{AlGaN,cryo}$ is the permittivity of the AlGaN barrier layer at cryogenic temperature. Further, T_{dev} and T_{norm} are the cryogenic temperature and nominal temperature of the device, respectively. β_{AlGaN}, β_{GaN}, and $\alpha_{pz,AlGaN}$, can be obtained from [19], [20]. Consequently, the electric field at the GaN surface (for $t_{AlGaN} << t_{p-GaN}$) can be articulated from (6.1), as

$$E = \frac{q(n+n_{trap})}{\epsilon_{AlGaN,cryo}} \tag{6.8}$$

The trap energy level (E_t) aligns with (E_C) but changes relative to (E_F) within the buffer. Assuming a triangular potential well at the heterojunction and considering that traps with energy levels below (E_F) are ionized, we introduce an effective width W that represents the distance from the GaN surface, as:

$$W = \frac{E_F+E_T}{qE} \tag{6.9}$$

Therefore, n_{trap} can be derived using Fermi–Dirac statistics as:

$$n_{trap} = N_T \int_0^W \frac{1}{1+exp\left(\frac{E_t(y)-E_F}{qV_{th}}\right)} dy \tag{6.10}$$

where

$$E_t(y) = qyE - E_T \tag{6.11}$$

Here, N_T, V_{th}, and $E_t(y)$ represent the trap concentration (in cm^{-3}), the thermal voltage, and the variation of the trap energy level within the buffer, respectively. By solving the given integral and assuming $(E_F + E_T) > qV_{th}$, the expression for n_{trap} is derived as follows:

$$n_{trap} = N_T\left(W - \frac{V_{th}\ln(2)}{E}\right) \tag{6.12}$$

Using (6.1), (6.8), (6.9), and (6.12), we obtain

$$n_{trap}^2 + (n + N_T)n_{trap} + N_T(n - RV_{GOT}) = 0 \tag{6.13}$$

for which the solution yields

$$n_{trap} = \frac{-(n+N_T)+\sqrt{(n+N_T)^2-4N_T(n-RV_{GOT})}}{2} \quad (6.14)$$

where

$$V_{GOT} = V_G - V_{OFF} - E_T - \left(\frac{kT}{q}\ln(2)\right) \quad (6.15)$$

The buffer traps contribute a temperature-dependent space charge that alters the electrostatics of the gate stack. As shown in Fig.6.1(b), traps with density N_T and activation energy E_T are distributed within the GaN buffer and follow the conduction band edge E_C, while their occupancy depends on the local Fermi level E_F. The resulting ionised trap charge density $\rho_t(z) = q\ N_T\ [1 - f_t(T)]$ modifies the boundary condition at the AlGaN/GaN interface and increases the net positive charge that must be screened by the two-dimensional electron gas (2DEG). Through Eq.(6.8), this trap-induced charge directly enhances the vertical electric field in the AlGaN barrier and thus affects both the 2DEG density and the field-dependent gate leakage mechanisms modelled in Section 6.3.4. At cryogenic temperatures, the change in trap occupancy $f_t(T)$ leads to a different balance between buffer charge and interfacial polarisation, which explains the trends observed in Section 6.4.

6.3.2 Model Electrostatics for Potential Variations at Cryogenic Temperatures including Buffer Traps

6.3.2.1 Schottky Barrier Potential Drop

At cryogenic temperatures, the Schottky barrier potential drop (V_{sh}) in p-GaN HEMTs become crucial due to the shifting energy levels of charge carriers, affecting their ability to overcome the barrier. This voltage drop across the p-GaN depletion layer is a key parameter, derived from the 1-D Poisson's equation, especially when the gate-source voltage (V_{gs}) exceeds the threshold voltage (V_{th}). In the below equation, the value of α_p can be obtained from [21].

$$V_{sh} = \frac{qN_a}{2\epsilon_{GaN,cryo}}\left(\sqrt{\frac{2\epsilon_{GaN,cryo}(\phi_{cryo}-\psi_a)}{qN_a}} + \frac{n+n_{trap}}{N_a}\right)^2 \quad (6.16)$$

where,

$$\phi_{cryo} = \phi_p(1 + \alpha_p \Delta T) \quad (6.17)$$

6.3.2.2 AlGaN Barrier Potential Drop

At low temperatures, the change in the electric field within the AlGaN barrier affects the potential drop ($V_{barrier}$), which can be calculated using the 1-D Poisson's equation. Thus, the potential drop across the AlGaN barrier at cryogenic temperatures can be calculated using the equation:

$$V_{barrier} = \left(\frac{\sigma_{p-GaN}}{\epsilon_{AlGaN,cryo}} t_{AlGaN}\right) - \left(\frac{q\eta N_a}{\epsilon_{AlGaN,cryo}} t_{AlGaN}^2\right) - \left(\frac{q\,(n + n_{trap})}{\epsilon_{AlGaN,cryo}} t_{AlGaN}\right) \quad (3.18)$$

Here, ηN_a represents the fraction of Mg dopants out-diffused from p-GaN into AlGaN [22].

6.3.3 Equation for Potential Balance and Fermi Dirac Statistics

To improve the physical accuracy of our model, we account for the voltage drops occurring across different resistive elements along the current conduction path. In addition to the previously calculated voltage drops across the sheet resistance (V_{sh}) and the AlGaN barrier ($V_{barrier}$), we now include a finite resistance located in the neutral region of the p-GaN layer adjacent to the AlGaN barrier, labeled as $R_{p\text{-}GaN}$. This resistance introduces an additional voltage drop, $V_{p\text{-}GaN}$. The overall potential distribution is then analyzed using a potential balance equation, as illustrated in the energy band diagram shown in Fig. 6.1(b), spanning from the gate metal to the GaN buffer layer, we establish the following relationship between, V_g. and the voltage drop in different regions which simplifies to (6.19) and (6.20), where $D_{n(p)} = \frac{m^*_{n(p)}}{\pi\hbar^2}$ (2-D Density of states), $m_n^* = 0.22\, m_0$, $m_p^* = 0.80\, m_0$, $\gamma_{0,n} = 2.12\, x\, 10^{-12}\, Vm^{4/3}$, $\gamma_{0,p} = 2.5\, x\, 10^{-12}\, Vm^{4/3}$, $p = \eta N_a t_{AlGaN} + n$, $V_{pGaN} = I_g\, x\, R_{pGaN}$, $E_{f(n/p)}$ is

quasi-Fermi level, $E'_{f(n/p)}$ is fermi level w.r.t the conduction band at AlGaN/GaN interface / Fermi level w.r.t the valence band at p-GaN/AlGaN interface and ψ_a is activation energy of the Mg dopants.

$$V_g = E_{g,GaN} - \phi_{cryo} + \psi_a + \Delta V_{sh} + V_{pGaN} + E'_{fp} - V_{barrier} + E'_{fn} \quad (6.19)$$

$$V_g = E_{g,GaN} - \phi_{cryo} + \psi_a + \gamma_{0,n}\left(n + n_{trap}\right)^{\frac{2}{3}} + \gamma_{0,n}p^{\frac{2}{3}} + \left(\frac{t_{AlGaN}}{\epsilon_{AlGaN,cryo}}\right)\left(q\left(n + n_{trap}\right) + \eta N_a t_{AlGaN} - \sigma_{p-GaN}\right) + \left(kT_{dev}\right)\left(\frac{\frac{\left(n+n_{trap}\right)}{e^{\frac{D_n}{kT_{dev}}}-1}}{\frac{p}{e^{\frac{D_p}{kT_{dev}}}-1}}\right) + \frac{qN_a}{2\epsilon_{GaN,cryo}}\left(\sqrt{\frac{2\epsilon_{GaN,cryo}\left(\phi_{cryo}-\psi_a\right)}{qN_a}} + \frac{n+n_{trap}}{N_a}\right)^2 \quad (6.20)$$

6.3.4 Model Electrostatics for Gate Leakage Mechanism at Cryogenic Temperatures including Buffer Traps

To model gate leakage across a wide range of gate voltages, we consider various physical phenomena, with a drain voltage (V_d) of zero. Potentials are calculated using equations (6.1) through (6.18), and charge density (n) is derived from equation (6.20) to evaluate leakage current. We use three main mechanisms to interpret gate leakage, emphasizing the role of buffer traps and cryogenic temperatures on device behavior under different bias conditions, as follows.

6.3.4.1 Thermionic Emission

At low positive bias, the leakage current's temperature dependence is significant [23,24], but buffer traps and cryogenic temperatures add complexity to the thermionic emission (TE) mechanism. Buffer traps reduce the availability of free carriers for TE by immobilizing them, while the decreased thermal energy further limits the ability of carriers to overcome the Schottky barrier at the metal/p-GaN interface. The current density resulting from this mechanism is given as

$$J_{TE} = AT_{dev}^2 \, exp\left(\frac{-q\left(\phi_{cryo} - \beta\sqrt{E_{max}}\right)}{kT_{dev}}\right) \quad (6.21)$$

where $A = \frac{4\pi m^* k^2}{h^3}$ represents the Richardson constant, and $\beta = \sqrt{\frac{q\pi}{\epsilon_{GaN,cryo}}}$. The maximum electric field (E_{max}) used to calculate the leakage in a low bias range across the metal/p-GaN layer is given as

$$E_{max} = \sqrt{\frac{2qN_a\left(V_g - V_{sh} + V_{barrier}\right)}{\epsilon_{GaN,cryo}}} \quad (6.22)$$

6.3.4.2 Thermally Assisted Tunneling

In p-GaN HEMTs under high forward bias, the steeper band structure at the Schottky junction enhances thermally assisted tunneling (TAT) [24]. However, at cryogenic temperatures, buffer traps modify the barrier profile and charge distribution, influencing TAT-driven leakage current. Although tunneling is generally temperature-independent, reduced thermal energy decreases the thermal assistance, while buffer traps introduce localized energy states that affect tunneling, leading to a unique temperature-dependent TAT current density, which is calculated as

$$J_{TAT} = C_{TAT} E_{sh} exp\left(-\frac{\left(q\phi_{cryo} - \frac{1}{6}\left(\frac{qhE_{sh}}{4\pi kT_{dev}\sqrt{m^*}}\right)^2\right)}{kT_{dev}}\right) \quad (6.23)$$

where, $C_{TAT} = \sqrt{2\pi m^* kT_{dev}}\left(\frac{q}{h}\right)^2$ and $E_{sh} = V_{sh}/W_d$

6.3.4.3 Poole Frenkel Emission

In p-GaN HEMTs under negative bias, gate leakage occurs via Poole-Frenkel emission (PFE) through the p-GaN cap sidewalls and passivation layer [24]. This mechanism describes the emission of carriers from trap states under the influence of an electric field, which lowers the effective potential barrier height. At cryogenic temperatures, the effects of buffer traps and the altered electric field distribution are amplified, causing substantial modifications in the PFE-driven leakage current. The PF emission current density is given as

$$J_{PFE} = C_{PFE} E \, exp\left(\frac{-q\left(\phi_t - \beta\sqrt{E}\right)}{kT_{dev}}\right) \quad (6.24)$$

where $C_{PFE} = q\mu_n n$ and $\beta = \sqrt{\frac{q\pi}{\epsilon_{GaN,cryo}}}$ and $E = \frac{V_g}{L_{gs}}$; L_{gs} is the shortest distance between the source and the gate.

6.4 Results and Discussion

This section presents the comparative analysis of p-GaN HEMT under varying temperature conditions. We examined three configurations: the conventional p-GaN HEMT, p-GaN HEMT with Fe deep acceptor buffer impurities that serve as buffer traps (a) at nominal temperature (Model A), and (b) at cryogenic temperature (Model B). The key innovation of Model B relative to both the conventional model and Model A is that it consistently incorporates the temperature dependence of buffer-trap occupancy, incomplete ionisation, and cryogenic permittivity into the electrostatics of the device. As a result, the predicted 2DEG density, potential drops (Fig. 6.3), and gate-leakage components (Fig. 6.4) exhibit a stronger and qualitatively different temperature dependence than would be obtained by simply extrapolating room-temperature models to lower temperatures. Our analytical modeling reveals distinct differences in device behavior across these scenarios, particularly in the 2DEG density, potential variations, and gate leakage current. This analysis provides insights into optimizing p-GaN HEMT performance across various operating conditions.

Figure 6.2(a) presents the variation 2DEG density (n_s) with gate voltage (V_g). Among the configurations, Model B achieves the highest 2DEG density due to the presence of Fe traps in the GaN buffer, which capture free electrons and generate a strong negative potential. This enhances electron confinement at the interface. At cryogenic temperatures, the Fe traps remain fully occupied, minimizing leakage into the buffer and maintaining 2DEG stability, making Model B highly suitable for low-temperature, high-performance applications. The difference between the conventional model and Model A arises from the explicit inclusion of ionised buffer-trap charge in the electrostatics of Model A. The Fe-related deep acceptor traps in the GaN buffer capture free electrons and thereby contribute an additional positive space charge q N_T (1 - f_t) in Poisson's equation. This enhances the downward bending of the conduction band and increases the polarisation-induced electric field at the

AlGaN/GaN interface, so that a larger 2DEG sheet density n_s is required to satisfy charge neutrality. In contrast, the conventional model neglects the trap-related charge and therefore underestimates the net positive charge in the buffer, leading to a lower predicted n_s.

Figure 6.2(b) illustrates the effect of the acceptor concentration (N_a) in the p-GaN layer on 2DEG density. An increase in N_a strengthens the electric field at the interface, attracting more electrons into the channel. The presence of Fe traps helps stabilize this field by capturing surplus electrons in the buffer, thus avoiding fluctuations in charge. This results in a stable and controllable 2DEG density that scales consistently with N_a, demonstrating both tunability and reliability.

In Figure 6.2(c), the impact of AlGaN barrier thickness (t_{AlGaN}) on 2DEG density is analyzed. As the barrier becomes thinner, the electric field intensifies, thereby enhancing the 2DEG density. Fe traps help maintain this density by localizing electrons and minimizing leakage into the buffer, allowing even thin AlGaN layers to support high and stable 2DEG levels, which is advantageous for compact device architectures.

Figure 6.2(d) examines how temperature influences both 2DEG density and threshold voltage (V_{th}). At low temperatures, Fe traps are fully filled, leading to a stable charge distribution and maximizing the 2DEG density. As temperature rises, some electrons escape from the Fe traps due to thermal excitation, reducing the 2DEG density and causing an increase in V_{th} due to buffer leakage. This underlines the importance of Fe traps in preserving stable electrical behavior under cryogenic conditions.

Figure 6.3(a) shows that the Schottky barrier potential drop (V_{sh}) is greatest in Model B, attributed to stronger electron confinement provided by Fe traps, which enhances charge buildup at the metal-semiconductor interface. This reflects the effectiveness of Fe traps in supporting high-field regions. Additionally, Figure 6.3(b) reveals that the Schottky barrier electric field (E_{sh}) is also highest in Model B, owing to improved charge stability in the GaN buffer. This ensures reliable performance under high

electric fields with minimal leakage, which is essential for cryogenic device operation.

Fig. 6.3(b) presents the electric field (E_{sh}) at the Schottky barrier. Model B exhibits the highest E_{sh} due to the stabilization of charges in the GaN buffer. This ensures that the device can sustain high electric fields without excessive leakage or instability, a critical requirement for cryogenic operation.

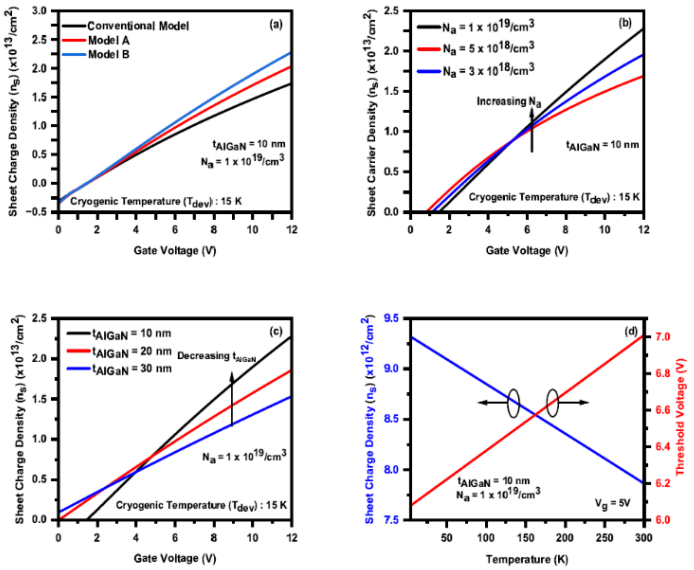


Fig. 6.2: (a) Comparison of n_s across the conventional model [15], Model A and Model B. (b) Comparison of n_s with varying N_a in the p-GaN layer for the model B. (c) Comparison of n_s concerning AlGaN barrier thickness for model B, and (d) Plot showing the variation of threshold voltage and n_s with temperature.

The AlGaN barrier potential drop ($V_{barrier}$) is lowest in Model B (depicted in Fig. 6.3(c)). This reduction is due to the uniform charge distribution achieved by Fe traps, which neutralize polarization-induced charges more effectively. This leads to

improved electrostatic stability across the AlGaN barrier. The Model B exhibits the lowest maximum electric field (E_{max}) in the buffer, as depicted in Fig. 6.3(d). Fe traps reduce charge accumulation in critical regions, promoting a uniform electric field distribution and lowering peak electric fields. This reduction enhances device reliability and minimizes the risk of breakdown.

Figs. 6.4(a)-(d) present the components of gate leakage current: Poole-Frenkel emission (PFE), thermionic emission (TE), and thermally-assisted tunneling (TAT). Model B shows significantly lower gate leakage currents in all mechanisms compared to other configurations.

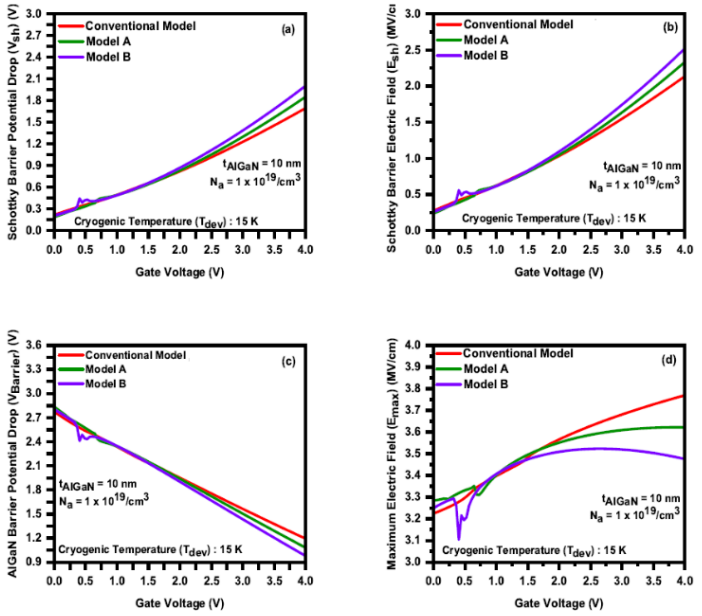


Fig. 6.3: Comparison of (a) V_{sh}, (b) E_{sh}, (c) $V_{barrier}$, and (d) E_{max} across the conventional model [17], Model A and Model B.

At cryogenic temperatures, Fe traps suppress PFE by immobilizing electrons. TE and TAT are also minimized due to the deep energy level of Fe traps and reduced thermal energy. This results in a 99% reduction in gate leakage current, making Model B highly suitable for cryogenic applications. Fig. 6.5 (a) and (b) compare the experimental and modelled total gate leakage current $I_{g,TOTAL}$ for three different temperatures and cryogenic temperature, respectively. Conventional model is benchmarked against an experimental device referenced from [15], [25]. This calibration confirms that the model accurately replicates the observed behavior,

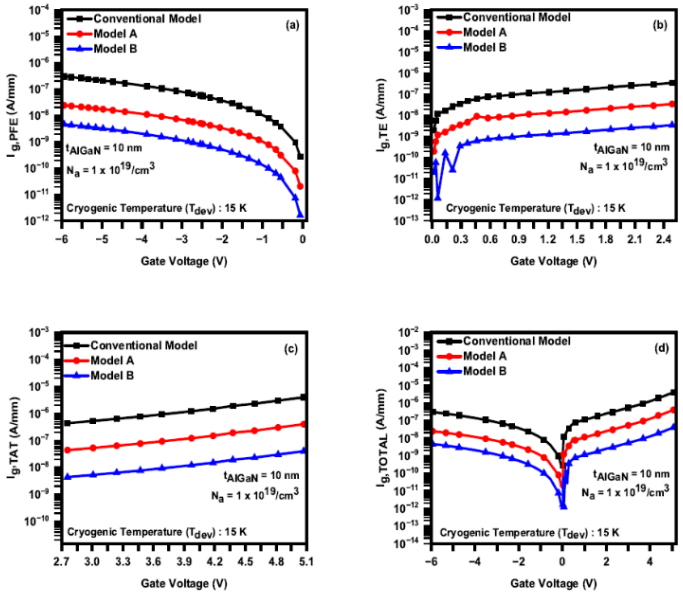
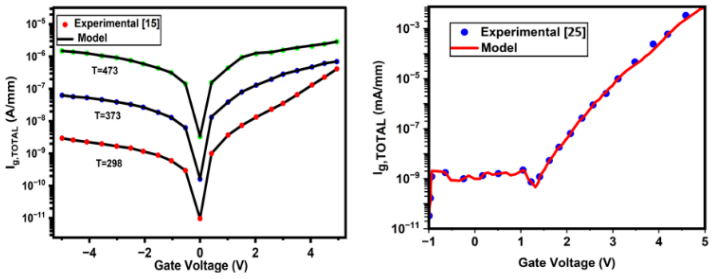


Fig. 6.4: Comparison of gate leakage current components (a) $I_{g,PFE}$, (b) $I_{g,TE}$, (c) $I_{g,TAT}$,and (d) total gate leakage current ($I_{g,TOTAL}$) across the conventional model [17], Model A and Model B.

aligning closely with the experimental data. Table 6.1 provides a comparison of device parameters obtained in this paper using the conventional model, Model A, and

Model B. The table highlights that Model B demonstrates improvements in parameters that are favorable for cryogenic power electronic applications [26]-[32]. The results demonstrate that Fe deep acceptor traps play a vital role in enhancing the performance of p-GaN HEMTs at cryogenic temperatures. They improve 2DEG density, reduce leakage currents, and stabilize electric fields, ensuring reliable and efficient operation. This makes the Fe-trap model a promising approach for advanced cryogenic device applications.



(a) (b)

Fig. 6.5: Experimental results validating the calibration of gate leakage current over the entire bias range.

6.5 Summary

In summary, we developed a physics-based model to analyze buffer trap effects on p-GaN HEMTs at cryogenic temperatures, incorporating the Fermi level (E_F), trap concentration (N_T), and activation energy (E_T). Compared to the conventional model, the proposed Model B shows a 33% increase in 2DEG density. The model also predicts a 99% reduction in gate leakage current by suppressing carrier tunneling and thermal activation through mechanisms like thermionic emission, thermally-assisted tunneling, and Poole-Frenkel emission. These results demonstrate significant improvements in device performance, highlighting the potential for cryogenic power electronics applications.

TABLE 6.1: Comparison of parameters derived from the models presented in this chapter

Parameters	Conventional Model [17]	This work (Model A)	This work (Model B)
n_s (x10^{13} /cm^2)	2.25	2	1.5
V_{sh} (V)	1.65	1.8	1.95
E_{sh} (MV/cm)	2	2.25	2.5
$V_{barrier}$ (V)	1.35	1.2	1.05
E_{max} (MV/cm)	3.75	3.6	3.45
$I_{g,TOTAL}$ (A/mm)	10^{-10}	10^{-11}	10^{-12}

Appendix A: Derivation of the 2DEG density expression (Eq. (6.1))

The charge-control relation in Eq. (6.1),

$$n + n_{trap} = R\left(V_G - V_{OFF} - \frac{E_F}{q}\right)$$

is obtained by solving the coupled Schrodinger–Poisson equations for the p-GaN/AlGaN/GaN gate stack under the triangular quantum-well approximation. The one-dimensional Poisson equation can be written as

$$\frac{d}{dz}\left[\epsilon(z)\frac{d\phi(z)}{dz}\right] = -\rho(z)$$

with $\rho(z) = \rho_{pol}(z) + qn\delta(z - z_0) + \rho_t(z)$, where ρ_{pol} is the fixed polarisation charge, n is the 2DEG sheet density at the AlGaN/GaN interface ($z = z_0$), and ρ_t is the trap-related charge in the GaN buffer. Integrating Poisson's equation from the gate metal to the 2DEG plane and enforcing continuity of the displacement field at the AlGaN/GaN interface yields

$$Q_{tot} = -\epsilon_{AlGaN,cryo}\frac{V_G - V_{OFF}}{t_{AlGaN}} = Q_{pol} + Q_{2DEG} + Q_{trap}$$

where $Q_{2DEG} = -qn$ and $Q_{trap} = -qn_{trap}$. Rearranging gives

$$n + n_{trap} = \frac{1}{q\left(\frac{t_{AlGaN}}{\epsilon_{AlGaN,cryo}} + \frac{t_{p-GaN}}{\epsilon_{GaN,cryo}}\right)}\left(V_G - V_{OFF} - \frac{E_F}{q}\right)$$

from which the factor R in Eq. (6.2) follows directly. An equivalent relation can be obtained from a Q–C–V analysis under the same electrostatic assumptions.

Appendix B: Derivation of Eqs. (12) and (13)

Starting from the definition of the trap electron density in Eq. (10),

$$n_{trap} = N_T \int_0^W \frac{1}{1+exp\left(\frac{E_t(y)-E_F}{qV_{th}}\right)} dy$$

with $E_t(y) = qyE - E_T$ from Eq. (6.11), we introduce the variable

$$u = \frac{E_t(y) - E_F}{qV_{th}} = \frac{qEy - E_T - E_F}{qV_{th}}$$

so that $du = (E/V_{th})dy$ and the integration limits y = 0 and y = W correspond to $u_0 = -(E_F + E_T)/qV_{th}$ and $u_W = 0$, respectively. The integral can then be written as

$$n_{trap} = N_T \frac{V_{th}}{E} \int_{u_0}^0 \frac{1}{1+\exp(u)} du$$

For $(E_F + E_T) \gg qV_{th}$ we have $u_0 \ll 0$, and the lower limit can be extended to

$$\int_{-\infty}^{0} \frac{1}{1+\exp(u)} du = ln2$$

Using $W = (E_F + E_T)/(qE)$ from Eq. (6.9), the above relations lead to

$$n_{trap} = N_T\left(W - \frac{V_{th}\ln(2)}{E}\right)$$

which corresponds to Eq. (6.12) in the main text.

Next, substituting Eqs. (6.1), (6.8), (6.9) and (6.12) into the expression for the electric field and rearranging terms, we obtain the quadratic equation

$$n_{trap}^2 + (n + N_T)n_{trap} + N_T(n - RV_{GOT}) = 0$$

which is Eq. (6.13). Solving this quadratic equation yields Eq. (6.14) for n_{trap} in terms of n, N_T and V_{GOT}.

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CHAPTER 7

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

7.1 Conclusion

This thesis highlights that the performance of GaN HEMTs for power electronics applications can be significantly improved by introducing novel device architectures and advanced material engineering. This thesis presents substantial advancements in GaN HEMT technology, focusing on the design, analysis, and optimization of novel structures to address key challenges such as gate leakage current, breakdown voltage, and on-resistance. The research objectives have been achieved through a combination of analytical modeling and numerical simulations.

The key findings of the research are presented, highlighting the advancements made in GaN HEMT technology for power electronics applications. Additionally, it discusses the broader implications of this work in developing high-performance and reliable power semiconductor devices, ultimately supporting the advancement of energy-efficient and sustainable technologies.

Advancements and challenges in GaN HEMT technology are explored, emphasizing its potential for high-power applications. It covered key performance metrics, including breakdown voltage, on-resistance, and gate leakage, along with innovations like p-GaN gate engineering and buffer optimization. The chapter also highlighted analytical modeling and emerging architectures, such as GaN MIS-HEMTs and multi-channel heterostructures, for improved reliability. This review provided a foundation for further advancements in GaN HEMT technology and power electronics.

The MGHEMT is presented that integrates an MIS structure with p-GaN, achieving a 14% reduction in gate leakage, a 20% increase in maximum drain current, and a 50%

improvement in threshold voltage. Additionally, the GDHEMT, employing a Gaussian doping technique, reduced gate leakage by 27%, improved drain current by 7%, and enhanced transconductance by 67%. Furthermore, a novel GaN HEMT featuring Ω-shaped gate p-GaN MIS-HEMT has been designed. This novel structure demonstrated a 33% increase in threshold voltage, a 5% enhancement in breakdown voltage, and reduced gate leakage due to optimized dielectric parameters.

A p-GaN HEMT featuring an AlInN/AlN/GaN double hetero-structure with an InAlGaN back-barrier is demonstrated. The device achieves high 2DEG density, low on-resistance, and improved current drive, with the back-barrier ensuring electron confinement and reduced gate leakage. Simulations show an 85% reduction in on-resistance, a 231% increase in drain current, and a peak transconductance of 354 mS/mm. The optimized 4 nm InAlGaN back-barrier enhances channel confinement and minimizes parasitic capacitances.

A p-GaN HEMT incorporating a stepped hybrid AlGaN buffer for high-power applications is investigated, demonstrating significant improvements in breakdown voltage, BFOM, and transconductance. Optimization of the buffer step thickness led to a 20% increase in breakdown voltage and a 4% enhancement in BFOM by redistributing the electric field and reducing leakage current. The device also exhibited low small-signal capacitances, enabling reduced power consumption and high switching speeds.

A physics-based model to analyze buffer trap effects in p-GaN/AlGaN/GaN HEMTs at cryogenic temperatures, incorporating Fermi level ($\boldsymbol{E_F}$), trap concentration ($\boldsymbol{N_T}$), and activation energy ($\boldsymbol{E_T}$) is developed. Compared to the conventional model (Model A), the proposed Model B demonstrated a 33% increase in 2DEG density and a 99% reduction in gate leakage current by suppressing carrier tunneling and thermal activation through thermionic emission, thermally-assisted tunneling, and Poole-Frenkel emission. These findings highlight significant improvements in device performance, establishing the proposed model as a promising approach for cryogenic power electronics applications.

These findings demonstrate significant advancements in GaN HEMT technology through novel device architectures and material engineering. The proposed designs effectively address key challenges such as gate leakage, breakdown voltage, and on-resistance, enhancing efficiency and reliability. The combination of analytical modeling and simulations has provided deep insights into device behavior, leading to optimized high-performance structures. This thesis paves the way for next-generation GaN HEMTs in power electronics, enabling improved efficiency and high-power operation.

Table 7.1: Comparative analysis of performance parameters of the proposed devices.

Proposed Device	Gate Leakage Current (A/μm)	ON-Resistance (mΩ.cm^2)	Breakdown Voltage (V)	Maximum Drain Current (A/μm)	Threshold Voltage (V)	BFOM (GW/cm^2)
MGHEMT	10^{-21}	--	--	1	5	--
GDHEMT	10^{-23}	--	--	0.75	5.8	--
Ω-shaped gate p-GaN MIS-HEMT	10^{-35}	3.33	1668	--	5.2	0.8355
p-GaN HEMT with AlInN/AlN/GaN Dou-ble Heterostructure and InAlGaN Back-Barrier	10^{-32}	1.507	2010	1.99	0.2	2.6808
STEPHB-HEMT	--	0.99	2149	0.12	4.05	4.67
P-GaN HEMT at Cryogenic Temperature with Buffer Traps	10^{-12}	--	--	--	6.1	--

7.2 Future Scope and Social Impact

GaN HEMTs have significant potential for technological advancements and societal impact due to their superior properties, such as high breakdown voltage, high power density, and high-frequency operation. Below are some important directions for further research and their associated social impacts:

7.2.1 Research Directions

- Fabricate the proposed GaN HEMT devices to validate simulation outcomes through experimental verification.
- Analyze the reliability of GaN HEMTs under thermal and electrical stress using advanced diagnostic techniques.
- Employ AI and machine learning for performance optimization and predictive modeling of GaN HEMTs.
- Explore GaN HEMT behavior at cryogenic temperatures for quantum and aerospace application readiness.

7.2.2 Social Impact

- Experimental validation enables real-world deployment of optimized GaN devices in power electronics.
- Improved reliability ensures longer device lifespans in critical high-voltage, high-temperature environments.
- AI integration supports sustainable and cost-efficient semiconductor design.
- Cryogenic operation research facilitates advancements in quantum computing and space exploration.

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LinkedIn: www.linkedin.com/in/tanvikagarg

Contact Address: B-7/101 First Floor, Plot Side, Sector-17, Rohini, PIN: 110089, New Delhi, India

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EDUCATION

Ph.D. in Electronics and Communication Engineering

Delhi Technological University, New Delhi, India | 2021 – present

Dissertation Title: Design and Performance Improvement of Gallium Nitride High Electron Mobility Transistor for Power Electronics Applications

Advisor: Dr. Sumit Kale

- Focused on designing, simulating, and optimizing Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) for power electronics, improving key performance metrics such as breakdown voltage, gate leakage current, and on-resistance. Conducted analytical modeling at cryogenic temperatures to assess and enhance device reliability and performance under extreme conditions.
- Awarded the **Commendable Research Award** for excellence in research by Delhi Technological University, recognizing outstanding contributions in the field of GaN HEMTs for power electronics applications.

- Coursework CGPA: 8.50/10

Master of Technology (M.Tech) in Electronics and Communication Engineering
National Institute of Technology, Delhi, India | 2019 – 2021

- Specialization in Electronics and Communication Engineering
- *Thesis Title*: FPGA-Based Implementation of Low Latency SRAM-based TCAM for Group Updation
- GPA: 8.41/10 (Rank: 3rd)
- GATE Qualified (2019)

Bachelor of Technology (B.Tech) in Information and Communication Technology
Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar, Gujarat, India| 2009 – 2013

- Major in Information and Communication Technology
- CPI: 7.35/10
- AIEEE Rank:11357

PUBLICATIONS

Journal Papers

- Tanvika Garg and Sumit Kale, "Recent Developments, Reliability Issues, Challenges and Applications of GaN HEMT Technology," in *IEEE Electron Devices Reviews*, doi: 10.1109/EDR.2024.3491716.

- Tanvika Garg, Sumit Kale, "A novel p-GaN HEMT with AlInN/AlN/GaN double heterostructure and InAlGaN back-barrier", *Microelectronics Reliability*, vol. 145, pp.114998, 2023, doi: 10.1016/j.microrel.2023.114998.

- Tanvika Garg, Sumit Kale, “A novel stepped AlGaN hybrid buffer GaN HEMT for power electronics applications”, *Microelectronics Reliability*, vol. 149, pp.115232, 2023, doi: 10.1016/j.microrel.2023.115232.

- Tanvika Garg, Sumit Kale, “Optimization of structural parameters in Omega(Ω)-Shaped gate p-GaN MIS-HEMT for performance improvement”, *Micro and Nanostructures*, vol. 188, pp.207793, 2024, doi: 10.1016/j.micrna.2024.207793.

- Tanvika Garg and Sumit Kale “Analytical Modeling of Buffer Trap Effects on 2DEG Density and Gate Leakage Current in p-GaN HEMT at Cryogenic Temperatures”, IEEE Transactions on Devices and Materials Reliability (Under Review)

Conference Papers

- T. Garg and S. Kale, "A Novel Enhancement Mode GaN HEMT with MIS and p-GaN structure," *2024 IEEE 9th International Conference for Convergence in Technology (I2CT)*, Pune, India, 2024, pp. 1-3, doi: 10.1109/I2CT61223.2024.10543334.

- T. Garg and S. Kale, "A Gaussian Doped p-GaN HEMT for Power Electronics Application," *2024 IEEE Third International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, India, 2024, pp. 1007-1010, doi: 10.1109/ICPEICES62430.2024.10719370.

- Sachin, Riya, S. Soni, S. Kale and T. Garg, "An Enhancement Mode Double T- Gate Field Plate GaN HEMT for Power Electronics Application," *2024 IEEE Third International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, India, 2024, pp. 1016-1020, doi: 10.1109/ICPEICES62430.2024.10719173.

- Bharti, M. and Garg, T., “Analysis of SPA Scheme for Massive MIMO”, In: Bansal, R.C., Agarwal, A., Jadoun, V.K. (eds) *Advances in Energy Technology. Lecture Notes in Electrical Engineering*, vol 766. *Springer*, Singapore, 2022, doi: 10.1007/978-981-16-1476-7_5.

- Bharti, M., Joshi, A. and Garg, T., “Controlling an SSB-SC Amplitude Modulator Using a Second-Order Control System”, In: Bansal, R.C., Agarwal, A., Jadoun, V.K. (eds) *Advances in Energy Technology. Lecture Notes in Electrical Engineering,* vol 766. *Springer*, Singapore, 2022, doi:10.1007/978-981-16-1476-7_44.

- Bharti, M., Shukla, M., Joshi, A. and Garg, T., “Simultaneous Frequency and SSB Modulation for Ultrasonic Speakers”, In: Bansal, R.C., Agarwal, A., Jadoun, V.K. (eds) *Advances in Energy Technology. Lecture Notes in Electrical Engineering*, vol 766. Springer, Singapore, 2022, doi:10.1007/978-981-16-1476-7_45.

Book Chapters

- Manisha Bharti and Tanvika Garg, "Testing of Semiconductor Scaled Devices", in *Nanoscale Semiconductors*, CRC Press, 2022, pp. 175-186.

- Manisha Bharti and Tanvika Garg, "Quantum Computing", in *Wireless Communication Security*, John Wiley & Sons, Inc., 2022, pp. 59-68.

- Tanvika Garg and Manisha Bharti, “Congestion Control Protocols for UWSNs” in *Energy-Efficient Underwater Wireless Communications and Networ*king, IGI Global, 2021, pp. 85-100.

- Tulika Garg, Manisha Bharti and Tanvika Garg, “Wireless Underground Sensor Networks” in *Harnessing the Internet of Things (IoT) for a Hyper-Connected Smart World*, Apple Academic Press, 2022, pp. 179-195.

Patents

- Tanvika Garg et al., "A Novel Dual-k Double-Sided Dielectric p-GaN MIS-HEMT for Power Electronics Application". **(Patent Published)**
- Tanvika Garg et al., "T-shaped Control-Gate with Dual-Cavity Silicon Nanowire Reconfigurable FET (TCG-DC SiNW RFET) based Biosensor". **(Patent Published)**

Professional Organizations

- ORCID member ID: 0009-0004-9145-5170
- Web of Science Researcher ID: LMP-0307-2024
- Google Scholar ID: WvakSrgAAAAJ

TEACHING EXPERIENCE

Teaching Assistant

1. Analog Electronics, Department of Electronics and Communication Engineering, Delhi Technological University, August-November (2022 and 2023), January-ongoing (2025)

2. VLSI Design, Department of Electronics and Communication Engineering, Delhi Technological University, January-April (2023 and 2024) and January-ongoing (2025).

3. Basic Electronics Circuits, Department of Electronics and Communication Engineering, Delhi Technological University, August-November (2024).

- Assisted in teaching
- Supervised lab sessions and helped students with assignments and projects

- Graded exams and assignments

TECHNICAL SKILLS

- **Programming Languages**: MATLAB, Verilog
- **Software/Tools**: LaTeX, Origin, Microsoft Visio, LTSpice, Cadence Virtuoso, Microsoft Office
- **Simulation & Modeling**: Silvaco Atlas TCAD, MATLAB

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ORIGINALITY REPORT

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PRIMARY SOURCES

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3	Zarak Bhat, Sheikh Aamir Ahsan. "A Comprehensive Model for Gate Current in E-Mode p-GaN HEMTs", IEEE Transactions on Electron Devices, 2024 Publication	1%
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