REALISATION OF SIMULATED IMMITTANCES USING MODERN ACTIVE BUILDING BLOCKS

A Thesis Submitted

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by

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(Meghana Shrivastava)

CANDIDATE's DECLARATION

I Meghana Shrivastava hereby certify that the work which is being presented in the thesis entitled "Realisation of Simulated Immittances Using Modern Active Building Blocks " in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of Electrical Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from 1.08.2021 to 31.07.2025 under supervision of Prof. Pragati Kumar and Prof. Data Ram Bhaskar. The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(Meghana Shrivastava)

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and that the statement made by the candidate is correct to the best of our knowledge.

Signature of Supervisor(s) **Signature of External Examiner**

CERTIFICATE BY THE SUPERVISOR(s)

This is to certify that the thesis entitled **Realisation of Simulated Immittances Using Modern Active Building Blocks** submitted by **Ms. Meghana Shrivastava (2K21/PHDEE/15)** for the award of degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Delhi Technological University, Delhi, is the record of students own work carried out by her under our supervision. The contents of this research work have not been submitted in part or fully to any other institute or university for the award of any degree.

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ABSTRACT

The simulation of passive components, including resistors, capacitors, and inductors, is essential in the design of compact and adjustable analog signal processing/-generation circuit applications. Conventional passive components frequently need substantial chip area and lack electronic tunability, make them less appropriate for integrated circuit (IC) applications. This work addresses these limitations by implementing simulated immittances employing active building blocks (ABBs), specifically the Current Feedback Operational Amplifier (CFOA), Current Follower Differential Input Transconductance Amplifier (CFDITA), and Second Generation Voltage Conveyor (VCII). These ABBs provide benefits including low-voltage functionality, good linearity, electronic tunability, and straightforward integration. Various immittance simulator circuits, both grounded and floating, are developed and validated by simulation utilizing macro model and CMOS technology. These circuits are utilized in analog filters, oscillators, impedance matching networks, sensors, biomedical circuits, and signal production systems. The proposed circuits are validated using simulation tools like PSpice and Cadence Virtuoso utilizing 180nm CMOS technology. Practical results are also obtained to verify the performance of the circuits and to confirm their feasibility for hardware implementation. The proposed designs exhibit enhanced performance regarding compactness, power efficiency, and frequency response, making them suitable for application in analog integrated circuits.

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LIST OF SYMBOLS

Symbol	Description
g_m	Transconductance
V_{BIAS}	Input bias voltage
R	Resistor
C	Capacitor
C_{eq}	Equivalent Capacitor
R_{eq}	Equivalent Resistor
L_{eq}	Equivalent Inductance
Ω	Ohm
W	Width
L	Length
R_P	Parasitic Resistance
R_Z	Parasitic Resistance
r_x	Parasitic Resistance
C_P	Parasitic Capacitance
C_Z	Parasitic Capacitance
I_{in}	Input Current
V_{in}	Input Voltage
Z_{in}	Input Impedance
Y_{in}	Input Admittance
I_{B0}	Bias Current
I_{B1}	Bias Current
α	Alpha
β	Beta
γ	Gamma
Max	Maximum

Min	Minimum
Sig	Sigma
f_L	Lower Operating Frequency
f_H	Higher Operating Frequency
P_{dis}	Total Quiescent Power Dissipation
BW	Bandwidth
Q	Quality Factor
K	Multiplication Factor
V_c	Control Voltage
V_{BE}	Base-emitter Voltage
R_{Bias}	Biasing Resistance
V_T	Thermal Voltage

LIST OF ABBREVIATIONS

ABB	Active Building Block
BJT	Bipolar Junction Transistor
BPF	Band Pass Filter
CM	Capacitance Multiplier
CC	Current Conveyor
CCII	Second Generation Current Conveyor
CFOA	Current Feedback Operational Amplifier
CDTA	Current Differencing Transconductance Amplifier
CCCCTA	Current Controlled Current Conveyor Transconductance Amplifier
CFTA	Current Follower Transconductance Amplifier
CMOS	Complementary Metal Oxide Semiconductor
CFDITA	Current Follower Differential Input Transconductance Amplifier
CDBA	Current Differencing Buffered Amplifier
CBTA	Current Backward Transconductance Amplifier
CCIIITA	Third-generation Current Conveyor Transconductance Amplifier
DRC	Design Rule Check
DDCC	Differential Difference Current Conveyor
DVCC	Differential Voltage Current Conveyor
DX-CCTA	Dual-X Current Conveyor Transconductance Amplifier
DVTC	Differential Voltage to Current Converter
DVCVS	Differential Voltage-Controlled Voltage Source
FCM	Floating Capacitance Multiplier
FTFN	Four Terminal Floating Nullors
FDNR	Frequency Dependent Negative Resistor
FDNC	Frequency Dependent Negative Conductance
FIS	Floating Immittance Simulator

GCM	Grounded Capacitance Multiplier
HPF	High Pass Filter
IC	Integrated Circuit
LVS	Layout and Schematic Extraction
LPF	Low Pass Filter
MTC	Mixed Translinear Cell
MF	Multiplication factor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NGCM	Negative Grounded Capacitance Multiplier
Op-Amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PSPICE	Personal Simulation Program with Integrated Circuit Emphasis
SFI	Simulated Floating Inductance
THD	Total Harmonic Distortion
VDTA	Voltage Differencing Transconductance Amplifier
VDBA	Voltage Differencing Buffered Amplifier
VCII	Second Generation Voltage Conveyor
VDCC	Voltage Differential Current Conveyor

Chapter 1

Introduction

This Thesis focuses on the "Realisation of simulated immittances using modern active building blocks". A variety of new circuit configurations, both grounded and floating immittance simulators have been presented, employing current feedback operational amplifiers (CFOAs), current follower differential input transconductance amplifier (CFDITAs) and second generation voltage conveyor (VCIIs) as the primary active components.

Passive elements i.e. resistors, inductors and capacitors are the most important electrical elements necessarily used in the area of analog signal processing/generation circuit applications. In integrated circuit technology, the large-valued physical passive elements require large surface area on silicon chip. For this reason, various researchers are mainly focused on the realisation of immittance simulator circuits using modern active building blocks (ABB) to replace the bulky physical passive elements.

Immittance simulator circuits can be used to realize lossless (ideal) capacitance multipliers/ lossy (non-ideal) capacitance multipliers in the form of series RC, parallel RC, lossless (ideal) inductance simulator/lossy inductance simulator in the form of a

series RL, parallel RL, frequency dependent negative resistance (FDNR)/ frequency dependent negative conductance (FDNC) etc using different types of amplifiers and active building blocks (ABB) with other passive components. Immittance simulators are also used in sinusoidal oscillator design, circuit cancellation of unavoidable parasitic elements and designing of active filters, multivibrators, impedance matching circuits, sensors, biomedical circuits etc. The use of grounded or floating immittances, positive or negative immittances in analog signal processing/ generation circuits are widely explored in the open literature. Different amplifier topologies, realisable in both CMOS and bipolar technology are being proposed which exhibit greater performance such as simple circuit layout, improved linearity, higher frequency range with lower power dissipation and higher slew rates. Nowadays in low-medium frequency applications mostly active inductors or capacitors are used instead of passive inductor or capacitor because of many advantages such as requirement of less chip area, improved quality factor. Also various parameters of realised circuits electronically tuned through biasing current(s) or voltage(s).

The operational amplifier (op-amp) has been the most commonly used building block in analog circuit design, particularly in the early days of analog integrated circuits, when signal processing was primarily performed in "voltage mode." One of the most widely produced op-amps, the IC 741, functioned as a differential voltage-controlled voltage source (DVCVS). It was widely utilized in various signal processing and generation applications, supporting both linear and nonlinear circuit implementations. Numerous immittance simulator circuits employing op-amps have been reported in [1] [2] [3] [4] [5]. Though Op-amp has served as the basic building block in analog circuit design, researchers and circuit designers have also stimulated various immittance simulator circuits using different traditional active building blocks such as operational transconductance amplifiers (OTA) [6] [7] [8] [9] [10] [11] [12] [13] [14]

[15] [16] [17] [18] [19] [20] [21] [22] and current conveyors (CC) [23] [24] [25] [26] [27]. Voltage mode op-amp circuits have been known for their limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product. Also, the limited slew rate of the op-amp affects the large signal and high frequency operation. When wide bandwidth, low power consumption and low voltage operation are needed simultaneously, the voltage mode op-amp is not suitable. These drawbacks can be eliminated using current conveyors or current conveyors based active elements. Second generation current conveyor (CCII) and its variants as active building blocks are used to simulate various immittance simulator circuits which are reported in [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40][41] [42] [43] [44] [45] [46] [47] [48] [49].

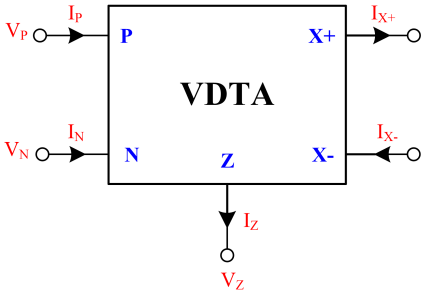
Since the output impedance of CCII is high and for voltage mode operation, the output impedance should be low, which limits the suitability of CCII based immittance simulators for voltage mode signal processing. Because of limitations of traditional active building blocks, many researchers and circuit designers use modern active building blocks such as current feedback operational amplifiers (CFOA), second generation voltage conveyors (VCII), current differencing buffered amplifiers (CDBA), current differencing transconductance amplifiers (CDTA), voltage differencing buffered amplifiers (VDBAs), third-generation current conveyor transconductance amplifiers (CCIIITA), current backward transconductance amplifiers (CBTA), current follower differential input transconductance amplifier (CFDITA), voltage differential current conveyor (VDCC) etc. to simulate various immittance circuits. Many modern active building blocks are less complex as compared to traditional ABBs. Modern ABBs are also electronically tunable through biasing current(s) which can be used to implement an automatic control system. The operational frequency range is also wider in case of modern ABBs as compared to traditional

ABBs. The functional block diagrams and port characteristics of some modern active building blocks ([50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62]) are illustrated below in Fig. 1.1 and Fig. 1.2.

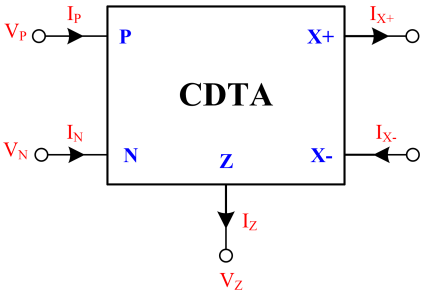
Among the numerous newly developed analog active building blocks (ABBs), only a few—specifically operational transconductance amplifiers (OTAs), current conveyors (CCs), and current feedback operational amplifiers (CFOAs)—have been commercially available as off-the-shelf integrated circuits [63]. Since this Thesis focuses on modern ABBs, particularly CFOAs, CFDITAs and VCIIs, it is appropriate to provide a brief overview of these components.

1.0.1 Current feedback operational amplifiers

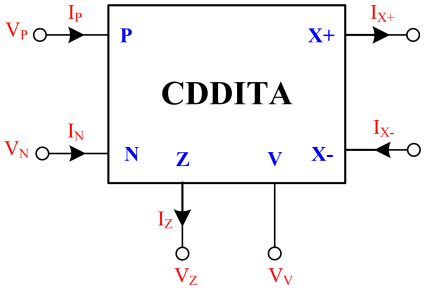
CFOAs are increasingly attracting interest from researchers for use in both linear and nonlinear signal processing and generation applications. This is largely due to their superior AC performance, high linearity, and excellent pulse response. With extremely high slew rates—ranging from several hundred to several thousand volts per microsecond—CFOAs enable the design of circuits that can operate across significantly wider frequency ranges compared to conventional operational amplifiers. CFOAs have been fabricated as integrated circuits by various manufacturers, including Analog Devices (model AD844) [64]. The bipolar implementation of this device is illustrated in Fig. 1.3 [63], and its corresponding pin configuration is provided in Fig. 1.4. In the internal structure of the CFOA, transistors Q_1 through Q_4 form a mixed translinear cell (MTC). The collector currents of transistors Q_2 and Q_3 are mirrored using two modified Wilson current mirror circuits—one p-n-p (comprising transistors Q_5 to Q_8) and one n-p-n (comprising Q_9 to Q_{12}). These mirrors replicate the input current I_X at the output terminal Z, resulting in $I_Z = I_X$. Two constant current sources, each supplying a current of I_B, ensure equal emitter currents in



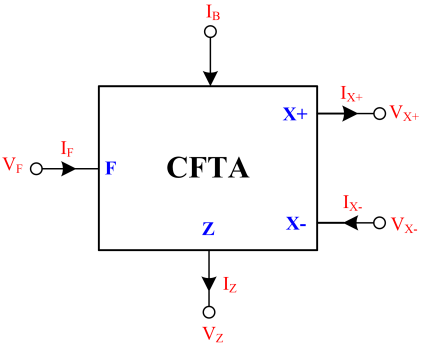
(a) $I_P = 0 = I_N$, $I_Z = g_{m1}(V_P - V_N)$ *and* $I_{X\pm} = \pm g_{m2} V_Z$



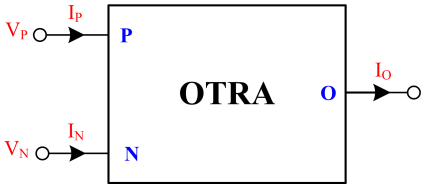
(b) $V_P = V_N = 0$, $I_Z = (I_P - I_N)$, $I_{X\pm} = \pm g_m V_Z$



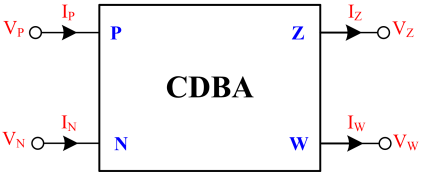
(c) $V_P = V_N = 0, I_Z = (I_P - I_N)$ *and* $I_{X\pm} = \pm g_m(V_Z - V_V)$



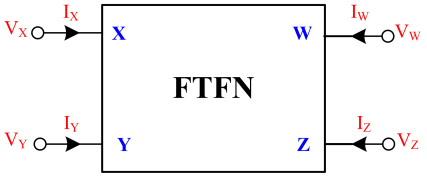
(d) $V_F = 0, I_Z = I_F$ *and* $I_{X\pm} = \pm g_m V_{X\pm}$



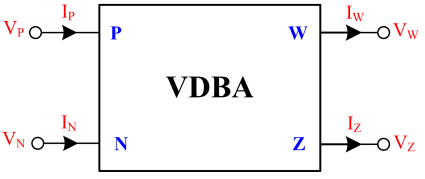
(e) $V_P = 0, V_N = 0 V_0 = R_m(I_P - I_N)$



(f) $V_P = V_N = 0, I_Z = (I_P - I_N)$ *and* $V_W = V_Z$

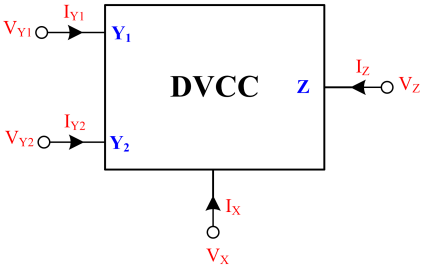


(g) $V_X = V_Y = 0, I_X = 0, I_Y = 0, I_W = I_Z, V_W$, V_Z are arbitrary

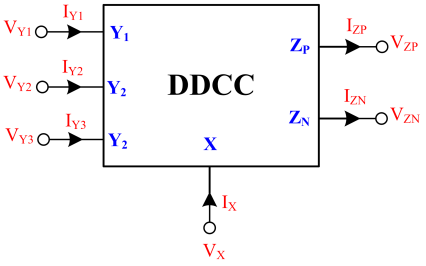


(h) $I_P = I_N = 0, V_Z = (V_P - V_N), V_W = V_Z$

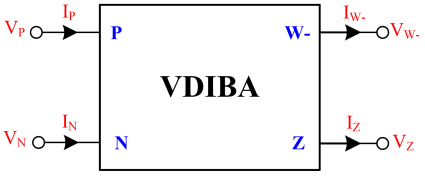
Figure 1.1: Functional block diagrams and port characteristics of (a) VDTA [50] (b) CDTA [51] (c) CDDITA [50] (d) CFTA [52] (e) OTRA [53] (f) CDBA [54] (g) FTFN [55] (h) VDBA [50]



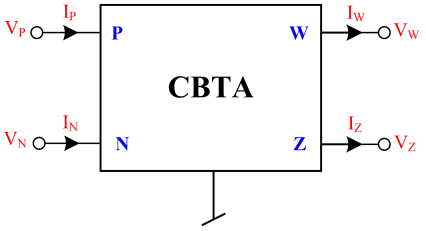
(a) $I_{Y1} = I_{Y2} = 0, V_X = (V_{Y1} - V_{Y2})$ *and* $I_Z = I_X$



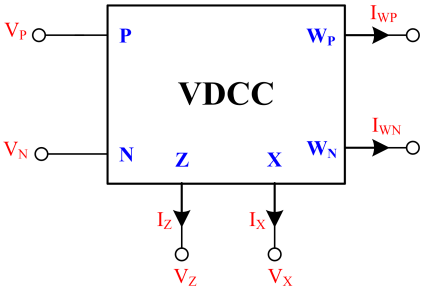
(b) $V_X = (V_{Y1} - V_{Y2}), I_{Y1} = I_{Y2} = I_{Y3} = 0, I_{ZP} = -I_X$ *and* $I_{ZN} = I_X$



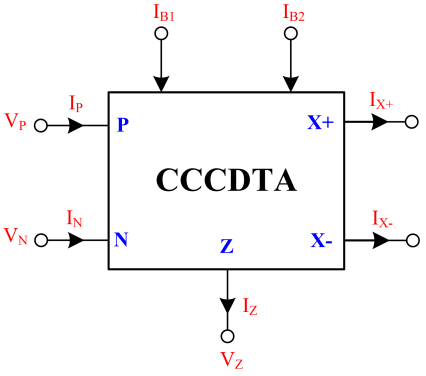
(c) $I_P = I_N = 0, I_Z = g_m(V_P - V_N)$ *and* $V_W = -V_Z$



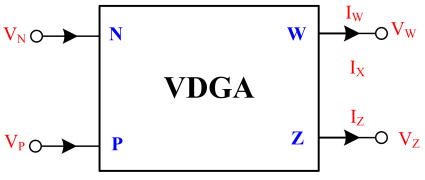
(d) $I_Z = g_m(V_P - V_N), V_W = V_Z, I_P = I_W$ *and* $I_N = -I_W$



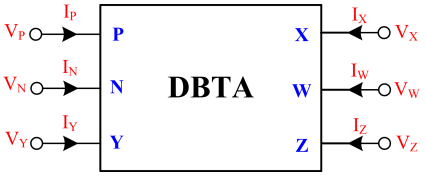
(e) $I_N = I_P = 0, I_Z = g_m(V_P - V_N), V_X = V_Z, I_{WP} = I_X$ *and* $I_{WN} = -I_X$



(f) $V_P = V_N = 0, I_Z = I_P - I_N$ *and* $I_{X\pm} = \pm g_m V_Z$



(g) $I_P = I_N = 0, V_Z = g_m(V_P - V_N)$ *and* $V_W = V_Z$



(h) $V_P = V_N = V_Y, I_Y = 0, I_Z = (I_P - I_N), V_W = V_Z$ *and* $I_X = \pm g_m V_Z$

Figure 1.2: Functional block diagrams and port characteristics of (a) DVCC [56] (b) DDCC [57] (c) VDIBA [58] (d) CBTA [59] (e) VDCC [50] (f) CCCDTA [60] (g) VDGA [61] (h) DBTA [62]

transistors Q_1 and Q_4. This configuration enforces a zero input current at terminal Y ($I_Y = 0$) when a voltage V_Y is applied. When $I_X = 0$, it follows that $V_X = V_Y$, and the output current at the Z terminal (I_Z) becomes zero [63]. In the case where

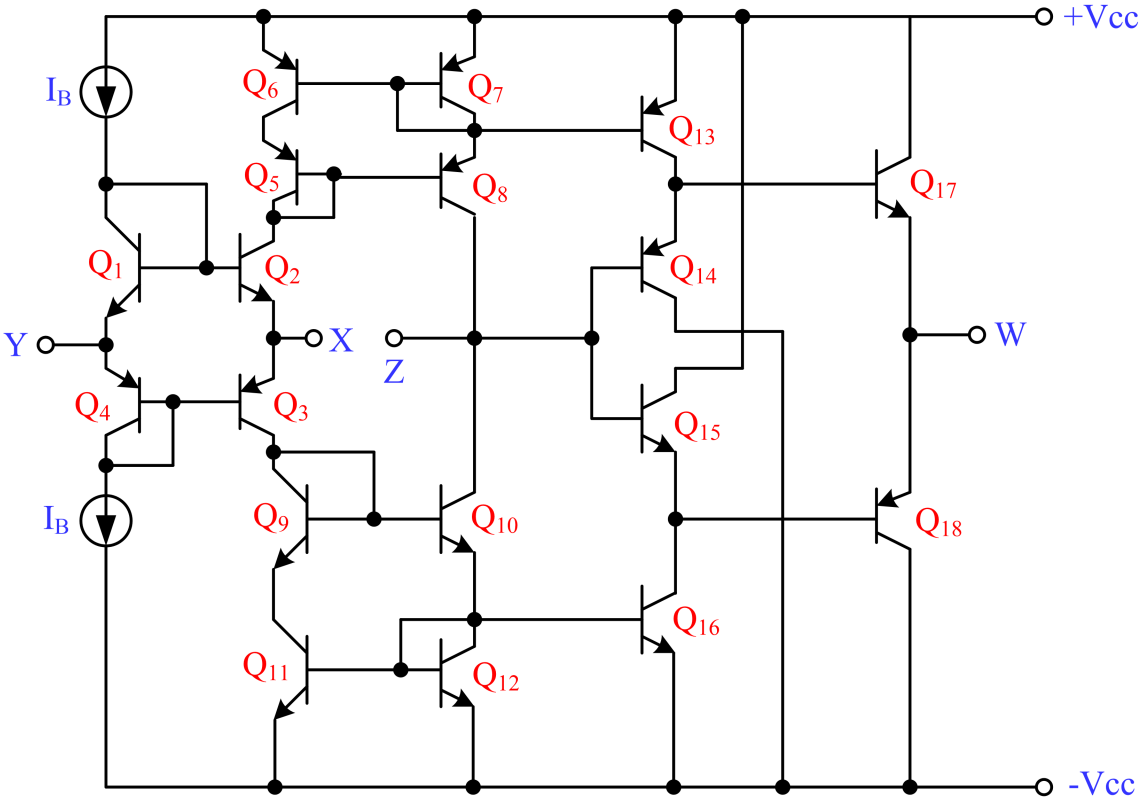


Figure 1.3: Schematic diagram of the CFOA AD844 [63]

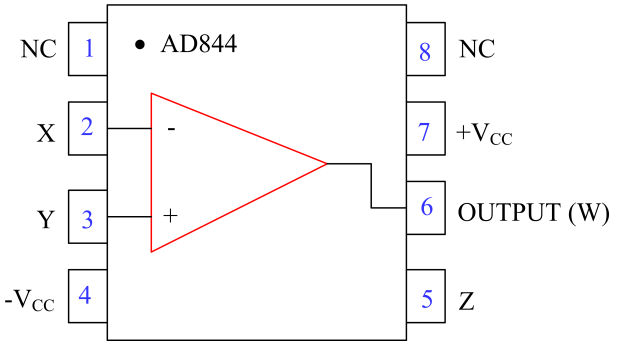


Figure 1.4: Pin diagram of AD844 [64]

$I_X \neq 0$, a detailed circuit analysis based on the exponential relationship between

collector currents and base-emitter voltages of transistors Q_1–Q_4 yields the following expression:

$$I_Z = I_X = -2I_B \sinh\left(\frac{V_Y - V_X}{V_T}\right) \tag{1.1}$$

For small currents ($I_X \ll 2I_B$), an approximate linear relationship between V_X, V_Y, and the small-signal resistance r_X is:

$$V_X \approx V_Y + r_X I_X \tag{1.2}$$

where $r_X = \frac{V_T}{2I_B}$.

If the Z terminal is connected to an external impedance/load Z_L, a voltage V_Z appears at this node. This voltage is transferred through a voltage follower constructed using another mixed translinear cell (MTC) comprising transistors Q_{13}–Q_{18}, where Q_{13} and Q_{16} provide the necessary DC bias current. The final stage follows a relationship analogous to Equation (1.2), resulting in $V_W \approx V_Z$. The ideal behavior of the CFOA and its equivalent circuit are depicted in Fig. 1.5. The port relationships can be represented using the following set of equations in matrix form:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_w \end{bmatrix} \tag{1.3}$$

Fig. 1.5 illustrates the symbolic representation of an ideal CFOA.

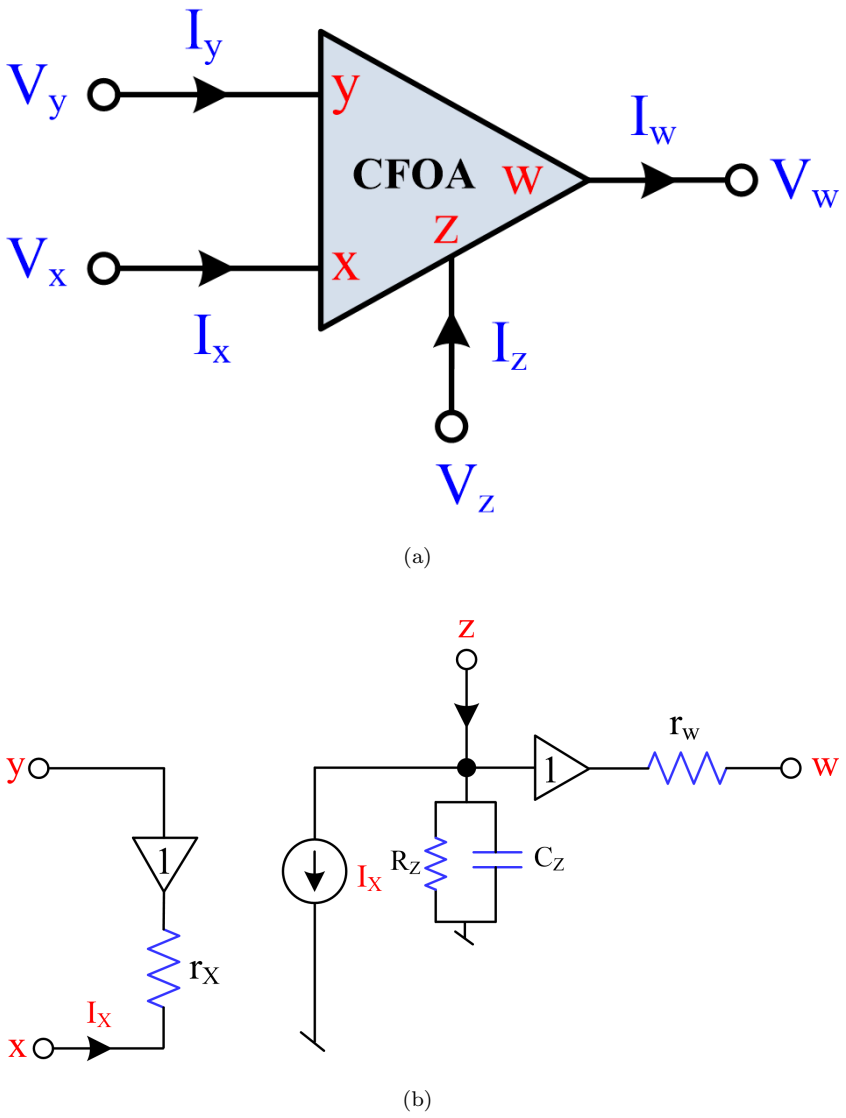


Figure 1.5: (a) Symbolic representation of CFOA (b) Equivalent circuit

A detailed overview of the AD844-type CFOA parameters is presented in Table 1.1.

Table 1.1: Parameters of AD844 [64]

Parameters	**Bipolar CFOA**
Operating range	±18V
Bandwidth	60 MHz
DC power dissipation	1.1 Watt
Input common mode voltage	±18V
Quiescent current	6.5 mA
Differential input voltage	6 V
Slew rate	2000 V/μs
Parasitic elements	r_x = 50Ω, R_Z=3MΩ, C_Z = 4.5pF

1.0.2 Current follower differential input transconductance amplifier (CFDITA)

CFDITA combines the capabilities of a current follower and a differential input transconductance amplifier, offering superior performance in analog circuit applications. The development of CFDITA commenced with the advent of the Current Differencing Transconductance Amplifier (CDTA), which integrated current differencing and transconductance amplification. Although CDTA enabled numerous analog signal processing functions, it demonstrated constraints regarding input impedance and complexity. To address these issues, the Current Follower Transconductance Amplifier (CFTA) was introduced, streamlining the architecture by substituting the current differencing unit with a current follower. The generalized current follower differential-input transconductance amplifier (GCFDITA), first reported in [65], provides the basis for the CFDITA. As stated in their formulation, when the control parameter $\alpha = 1$, the GCFDITA simplifies to the CFDITA. Hence, the CFDITA can be regarded as a special case of the more versatile GCFDITA architecture. CFDITA was developed to improve performance by integrating differential input capabilities, hence improving linearity and controllability in analog circuits.

The CFDITA, as shown in Fig. 1.6, is symbolically represented as a four terminal

active device. In its current follower stage, the current at Z-terminal follows the current of F-terminal. This stage is followed by a differential input transconductance amplifier that produces an output current at O-terminal. Furthermore, the output current at O-terminal is proportional to the voltage difference between Z and V-terminals. The ideal terminal relationships between currents and voltages of CFDITA are expressed in equation (1.4).

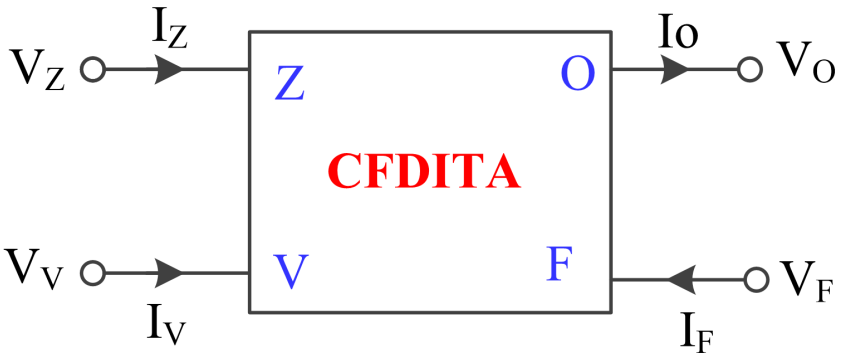


Figure 1.6: Symbol of CFDITA

$$I_V = 0, I_Z = I_F, I_O = g_m(V_Z - V_V), V_F = 0 \tag{1.4}$$

where gm is the transconductance of CFDITA

1.0.2.1 Advantages of CFDITA Over Other Modern ABBs

The CFDITA offers numerous benefits that render it an appropriate active component for analog signal processing applications:

- **Hybrid Nature:** Integrates voltage-mode control (differential input) with current-mode output (transconductance), accommodates both voltage-mode and current-mode circuits, hence enhancing versatility.

- **Exceptional Linearity:** The differential input and transconductance stage enhance linearity, particularly in filter and oscillator configurations.
- **Wide Bandwidth:** Provides improved frequency response relative to traditional OTAs, rendering it suitable for high-frequency circuits.
- **Low Input Impedance and High Output Impedance:** Appropriate for cascading in current-mode circuits without causing loading effects.
- **Enhanced Integration Capability:** Due to its CMOS implementation, it is readily integrable in VLSI, in contrast to certain complex conventional blocks such as OTAs and CCIIs.
- **Tunable Transconductance:** Transconductance (g_m) can be electronically adjusted using bias current, providing versatility in adaptive and programmable circuits.
- **Enhanced Frequency Response:** In comparison to OTA, CCII, or CFOA, CFDITA frequently demonstrates superior bandwidth, particularly in low-power, high-frequency applications..
- **Efficient for Immittance Simulation:** Optimal for the implementation of various immittance simulator circuits.

1.0.2.2 CMOS Realization of CFDITA

In this section, we have proposed CMOS implementation of CFDITA. The CFDITA consists of two components: a current follower unit operating as the input stage and a differential input transconductance amplifier unit operating as the output stage. Fig. 1.7 illustrates the CFDITA CMOS implementation. The transistors M_1-M_9 constitute the current follower unit, whereas the transistors M_{10}-M_{18} comprise

the differential input transconductance amplifier stage. The transconductance of CFDITA is electronically tunable via input bias voltage V_{BIAS}.

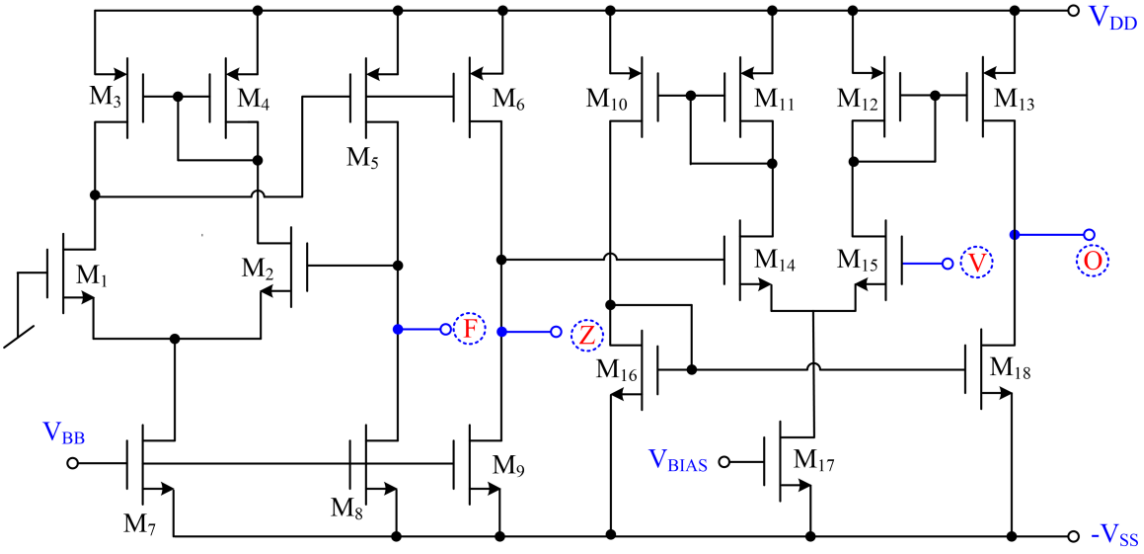


Figure 1.7: Proposed CMOS implementation of CFDITA

To validate the proposed CMOS implementation of CFDITA, PSPICE simulations were conducted utilizing 180 nm TSMC CMOS characteristics. The aspect ratios of the MOS transistors are presented in Table 1.2. For simulation results, the supply voltages and bias voltages used were V_{DD} = -V_{SS}= 1.32V, V_{BIAS} = 0.78V and V_{BB}= -0.7V respectively.

Table 1.2: Aspect ratios of the MOSFETs used in Fig. 1.7

MOS transistors	**W(μm)**	**L(μm)**
M_1, M_2	0.36	0.18
M_3, M_4	1.44	0.18
M_5, M_6	3.6	0.18
M_7, M_8, M_9	16.2	0.18
M_{10}, M_{13}	2.88	0.36
M_{11}, M_{12}, M_{16}, M_{18}	1.44	0.36
M_{14}, M_{15}	3.6	0.36
M_{17}	5.44	0.36

Fig. 1.8(a) illustrates the frequency response of CFDITA for the current gain (I_Z/I_F). The 3-dB bandwidth for current gain (I_Z/I_F) depicted in Fig. 1.8(a) is determined to be 42.9 GHz. The DC transfer characteristic of CFDITA from terminal F to terminal Z is illustrated in Fig. 1.8(b). Current I_F appears to be linearly correlated with current I_Z within the range of -5mA to 5mA. The input current linear range of the proposed CMOS CFDITA is excellent. Fig. 1.8(c) illustrates the fluctuation of transconductance g_m (I_O/V_Z with $V_V = 0$) while the bias voltage V_{BIAS} changes from -0.5V to -1.2V. The maximum value of g_m is 6.38 mS. Fig. 1.8(d) depicts the frequency response of the transconductance of the proposed circuit, demonstrating its variation from 1kHz to 100GHz. It is evident that g_m remains consistently about 7.4 mS across a broad frequency range upto 10GHz, signifying exceptional stability in low and mid-frequency ranges. The practical implementation of CFDITA using commercially available IC AD844 and LM13700 is shown in Fig. 1.9

1.0.3 Second generation voltage conveyor (VCII)

VCII was first proposed by I. M. Filanovsky in 1980 has been reported in [66]. In recently years, VCII has gained significant attention from researchers owing to its straightforward circuit-level integration, higher operating frequency range, minimal power consumption, compact chip area, and the presence of both high as well as low-impedance current output/voltage input terminals. VCIIs emerge as optimal selections for circuits featuring voltage-derived outputs. The ease with which VCII facilitates the subtraction and addition of current signals is attributed to its low-impedance input terminal [67]. The symbolic representation of VCII± is shown in Fig. 1.10. The current input terminal Y in this device has low impedance (ideally zero). The high-impedance (ideally infinite) current output port known as the X

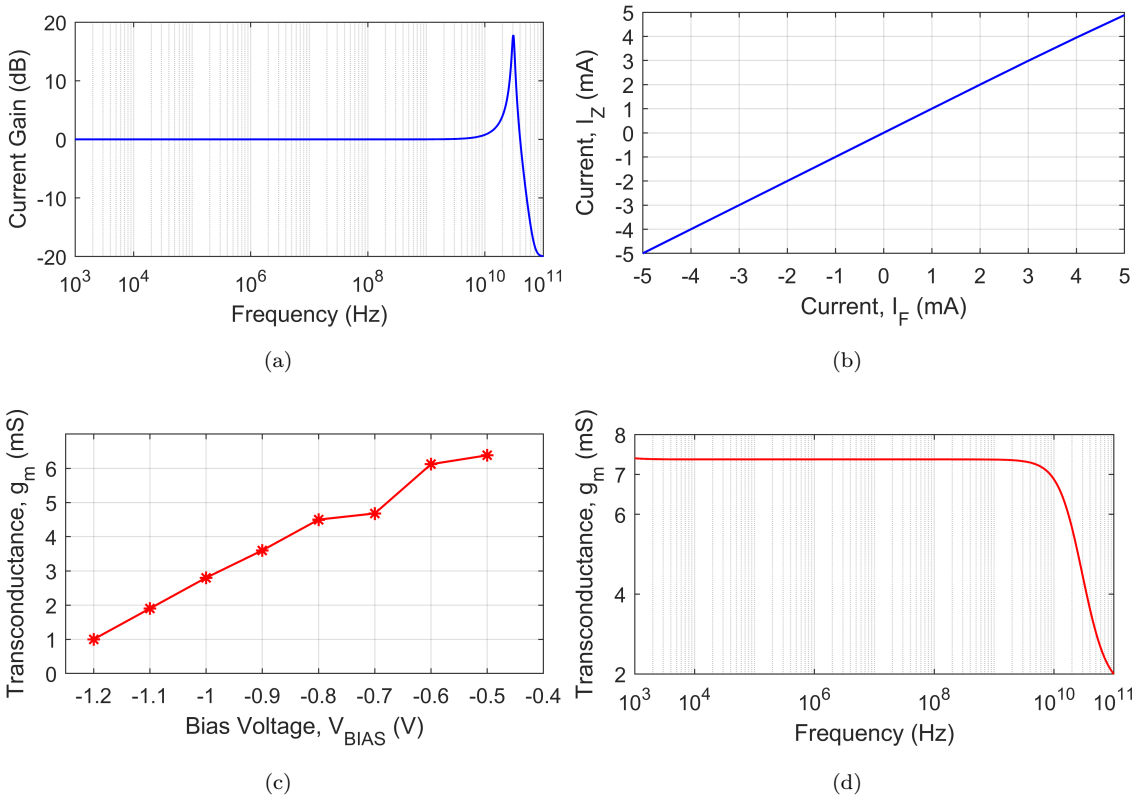


Figure 1.8: (a)Frequency response of current gain (b) DC current transfer characteristic (c) Variation of transconductance with V_{BIAS} (d) Variation of transconductance with frequency

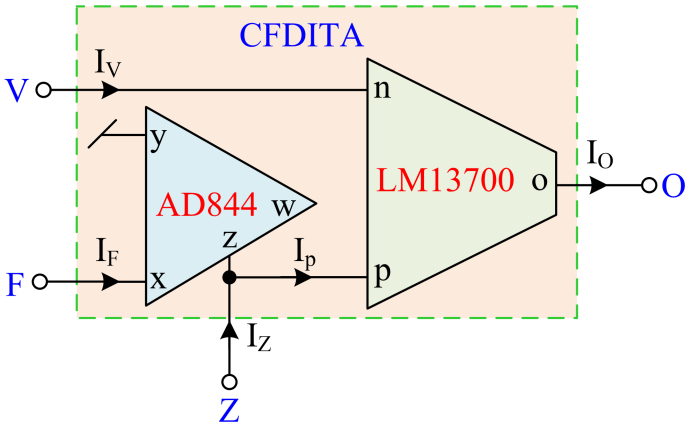


Figure 1.9: Implementation of CFDITA using commercially available ICs

terminal receives the current entering at the Y terminal. The voltage generated at the X terminal is transmitted to the Z terminal, a low-impedance voltage output terminal that, ideally, has zero resistance. The relationships between port currents

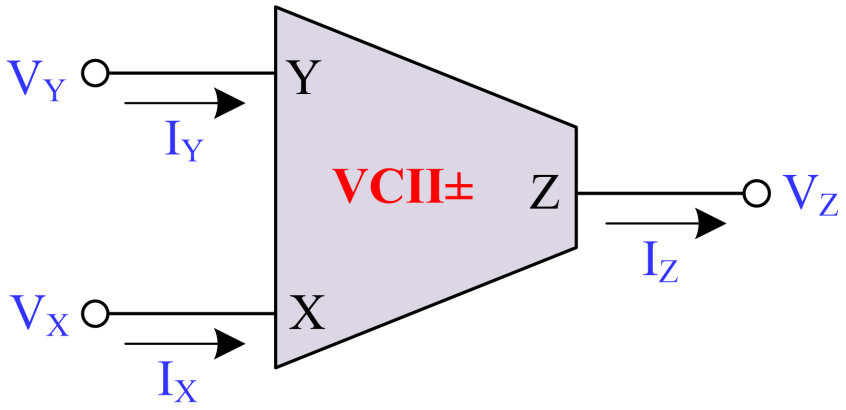


Figure 1.10: Symbol of VCII

and voltages of VCII± are given by:

$$I_X = \pm I_Y, V_Z = V_X \; and \; V_Y = 0 \tag{1.5}$$

1.0.3.1 CMOS implementation of VCII ±

The CMOS implementation of VCII+ and VCII- are shown in Fig. 1.11 based on the implementation reported in [68].

In Fig. 1.11(a), VCII+ is realized using a series connection of a current buffer composed of transistors M_1 to M_7 and a voltage buffer consisting of transistors M_8 to M_{12}. The existing buffer section has a negative feedback loop with M_2 to M_5 MOS transistors to ensure low impedance at the Y terminal. The input current is conveyed from the Y terminal to the X terminal via a basic current mirror composed of M_6 and M_7 MOS transistors. In the voltage buffer section, the voltage generated at the X terminal is conveyed to the Z terminal via the established voltage buffer using M_8 to M_{12} MOS transistors. The low impedance at the Z terminal is facilitated by a negative feedback loop including transistors M_8 to M_{11}. MOS transistors M_{13} to M_{18} are utilized for biasing purposes.

In the VCII- circuit depicted in Fig. 1.11(b), identical current and voltage buffers are employed. The basic current mirror composed of M_{18} and M_{19} MOS transistors is utilized to deliver the inverting current gain between the Y and X terminals. I_{B1} functions as a current source. Additionally, M_8 and M_9 MOS transistors are incorporated to ensure appropriate biasing at the X terminal.

To confirm the operational effectiveness of the CMOS VCII+ and VCII- configurations, implemented with 0.18µm TSMC technology specifications in PSPICE simulation tool. The PMOS and NMOS transistor aspect ratios in Fig. 1.11 were set at 40.5µm/0.54µm and 13.5µm/0.54µm, respectively. The DC power supply voltages used to bias VCII+ and VCII- were ± 0.9V, and the biasing currents I_{B0} and I_{B1} were both selected as 25µA. The DC transfer characteristic of VCII+ and VCII- from terminal Y to terminal X is illustrated in Fig. 1.12 (a) and Fig. 1.12 (b). Current I_Y appears to be linearly correlated with current I_X within the range of -100μA to 100μA. Fig. 1.12 (c) and Fig. 1.12 (d) shows a linear relationship between V_Z and V_X within the range of -130mV to 130mV for VCII+ and -60mV to 60mV for VCII-.

Fig. 1.13 (a) and Fig. 1.13(b) illustrates the frequency response of current gain (I_X/I_Y) and voltage gain (V_Z/V_X) of VCII+ respectively. The 3-dB bandwidth for current gain (I_X/I_Y) and voltage gain (V_Z/V_X) are determined to be 1 GHz. The frequency response of current gain (I_X/I_Y) and voltage gain (V_Z/V_X) of VCII- are shown in Fig. 1.13 (c) and Fig. 1.13(d). The 3-dB bandwidth for current gain (I_X/I_Y) is 1 GHz and for voltage gain (V_Z/V_X) is 761.886MHz.

VCII is implemented using off-the-shelf commercially available IC AD844. VCII+ can be implemented with only one IC AD844 while two ICs are required for the implementation of VCII-. Fig. 1.14 illustrates the AD844-based implementation of VCII+ and VCII- configurations.

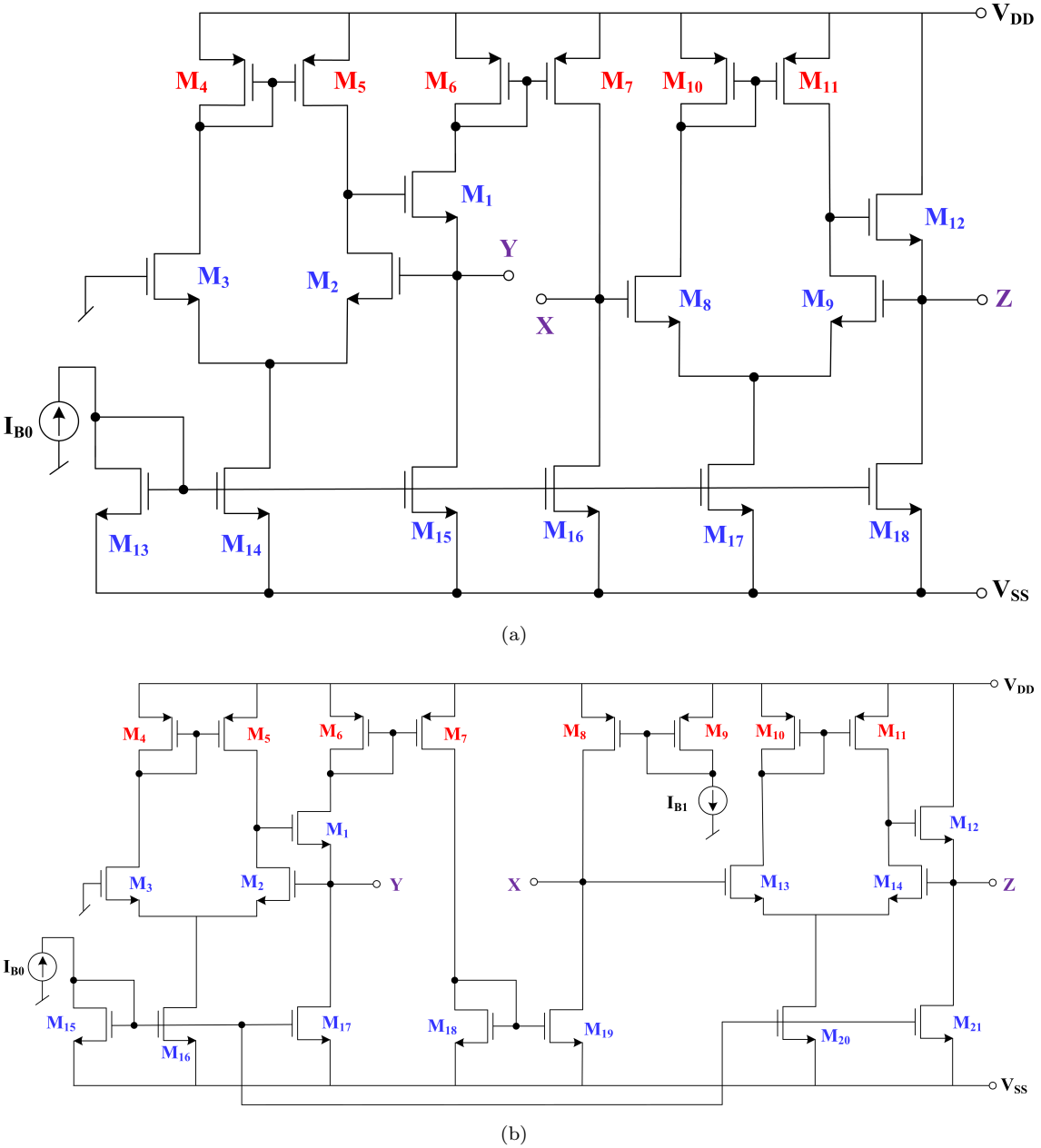


Figure 1.11: CMOS structure [68] of (a) VCII+ and (b) VCII-

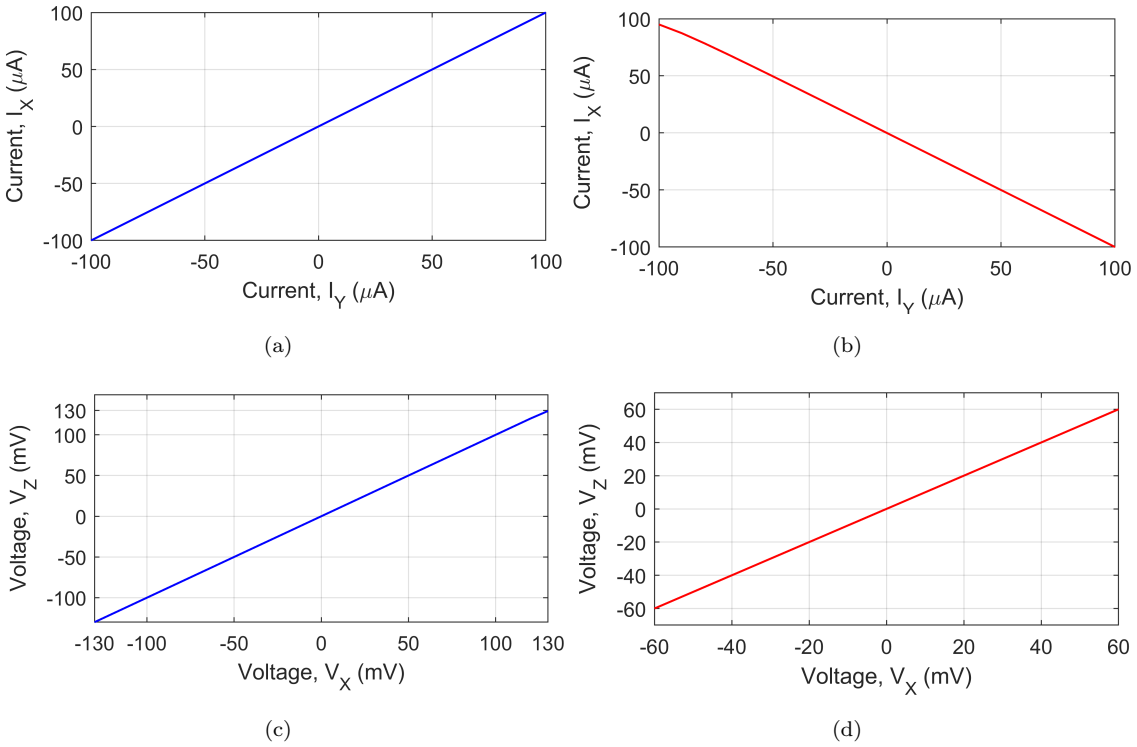


Figure 1.12: (a) DC current transfer characteristic of VCII+ (b) DC current transfer characteristic of VCII- (c) DC voltage transfer characteristic of VCII+ (d) DC voltage transfer characteristic of VCII-

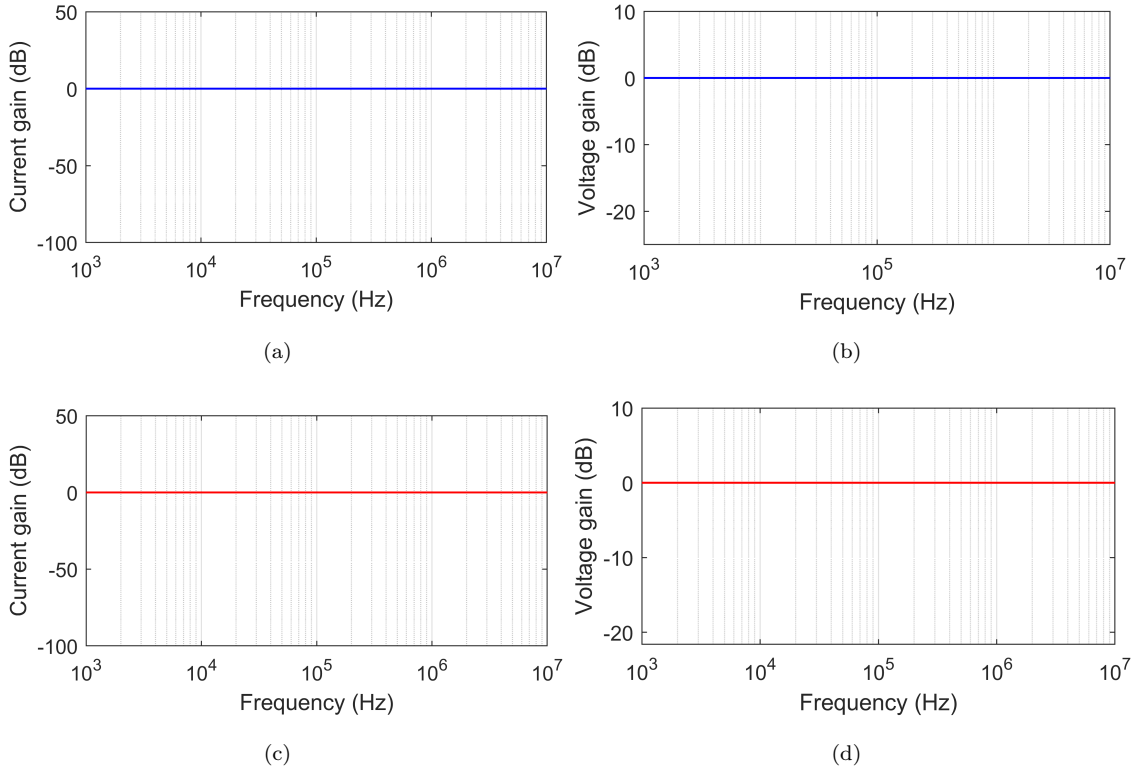


Figure 1.13: (a) Frequency response of current gain of VCII+ (b) Frequency response of voltage gain of VCII+ (c) Frequency response of current gain of VCII- (d) Frequency response of voltage gain of VCII-

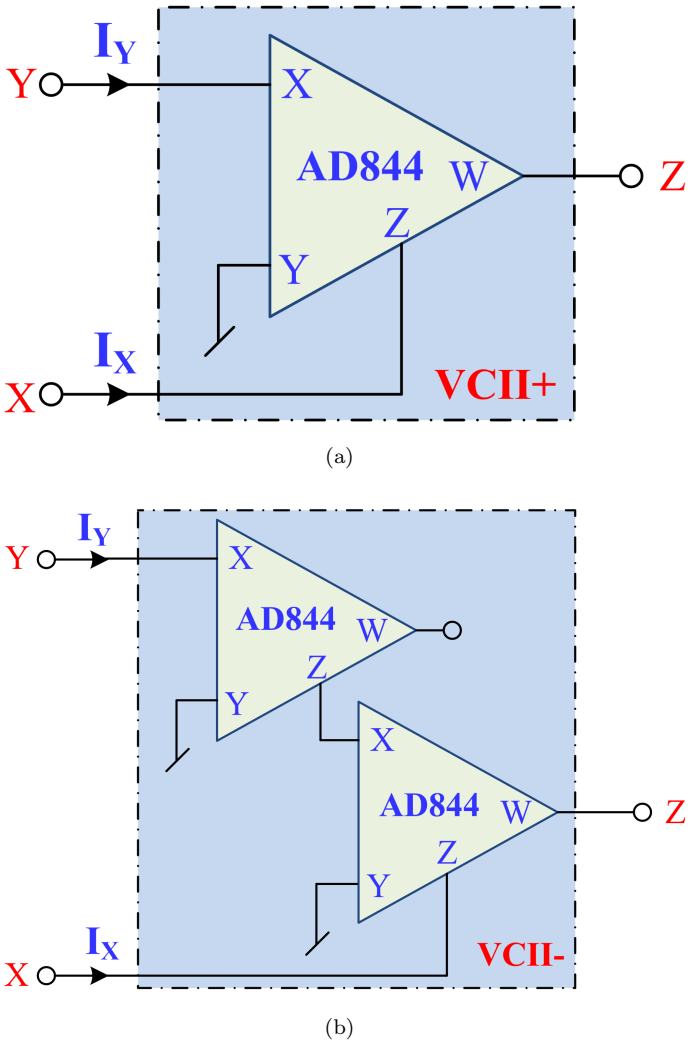


Figure 1.14: AD844-based implementation of (a) VCII+ (b) VCII- [68]

1.1 Research Objectives

Various grounded and floating immittance simulator circuits—both lossless and lossy have been extensively explored in the literature, utilizing a variety of modern active building blocks. These circuits are pivotal in analog signal processing, enabling the simulation of capacitors, inductors and other passive components through active devices. Different ABBs based grounded immittance simulator circuits [69] [70] [71] [32] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] and floating immittance simulator circuits [99] [100] [101] [102] [103] [104] [105] [106] [107] [108] [109] have been reported. In [110], an active inductor employing both grounded as well as floating mode using Dual-X Current conveyor Transconductance Amplifier (DXCCTA) has been reported. Another floating as well as grounded immittance simulator circuits have been reported in [111] [112] [113] [114]. Electronically tunable capacitance multipliers using VDBA have been reported in [115] [116] [117] [118]. In [119], a new tunable impedance multiplier circuit with high multiplication factor, which can realize a positive or a negative impedance multiplier has been presented. It consists of a current feedback operational amplifier CFOA, an OTA, a grounded resistor and the impedance to be scaled.

In [120], a resistorless floating lossy series R-L type inductor circuit employing two VDBAs and only a grounded capacitor has been proposed. Various lossy inductance simulators have been reported in [121] [122] [123] [124] [125] [126].

Immittance simulator based on CFOAs have been reported in [127] [128] [129] [130] [131] [132] [133] [134] [135] [136] [137] [138] [139].

CFOA based floating immittance simulator circuits have been reported in [140] [141]

[142] [143] [144] [145] [146] [147] [148] [149] [150]. CFDITA based immittance simulator circuits have been reported in [151] [152] [153]. VCII-based immittance simulator circuits have been reported in [154] [155] [156] [157] [158] [68] [159] [160] [67].

From a detailed literature survey of the immittance simulators available in the open literature, it has been found that:

- No single off-the-shelf available IC and grounded capacitor-based negative capacitance multiplier has been reported in the literature with high multiplication factor (> 1000).
- No lossy capacitance multiplier circuit has been reported yet, whose multiplication factor can be controlled independently.
- No single CFDITA-based grounded capacitance multiplier circuit has been reported yet in the open literature whose multiplication factor can be controlled electronically.
- No single CFDITA-based lossy grounded inductor has been reported yet.

In view of the above literature survey, following research objectives were found

- Classification of different immittance simulation circuits realized with modern active building blocks other than operational amplifier, operational transconductance amplifier (OTA), and second-generation current conveyor (CCII).
- Realisation of novel capacitance multiplier circuits using modern active building blocks.
- Realisation of immittance simulator circuits with modern active building blocks realizable with off-the-shelf available components.
- Realisation of RC-active filters using simulated immittances.

1.2 Organisation of Thesis

The Thesis is organized as follows:

Chapter 2 deals with CFOA-based grounded and floating immittance simulator circuits. Three new single CFOA-based grounded capacitance multiplier (CM) circuits and three floating immittance simulator circuits using CFOAs have been presented. To substantiate the feasibility of the proposed circuits, macro model of CFOA has been used, and the simulations have been performed in Personal Simulation Program with Integrated Circuit Emphasis (PSPICE). The functionality of the proposed structures has also been validated experimentally using commercially available IC AD844-type CFOA.

In **Chapter 3**, we have presented two grounded lossy/lossless capacitance multiplier circuits using CFDITA. The performance of the proposed CM circuit is validated using a CMOS CFDITA. The results are further validated with experimental results using the AD844 and LM13700 ICs.

Chapter 4 deals with the realisation of immittance simulator circuits using second generation voltage conveyor (VCII). VCII based series and parallel immittance simulator circuits have been proposed .These circuits implement parallel/series resistor–inductor (RL), parallel/series resistor–capacitor (RC), parallel/series capacitor–frequency dependent negative resistance (CD), and capacitance multiplier configurations employing only two second-generation voltage conveyors (VCII±). The SPICE simulation tool was used to validate the feasibility of the presented circuits. Further validation was carried out through layout design in Cadence Virtuoso, employing 0.18 μm CMOS technology. Also, the claimed theory is verified by experimental results based on the VCII implementation with commercially available IC AD844.

Chapter 5 of the Thesis presents a summary of the research work presented and some suggestions for future work on the ideas explored.

Chapter 2

CFOA-based Novel Realisation of Capacitance Multiplier and Floating Immittance Circuits

2.1 Introduction

The present Chapter deals with CFOA-based grounded capacitance multiplier and floating immittance simulator circuits. Three new single CFOA-based grounded capacitance multiplier (CM) circuits and three floating immittance simulator circuits using CFOAs have been proposed in this Chapter.

Capacitance multiplier circuits are important active building blocks (ABBs) of analog circuits which are used to simulate larger capacitance value from small physical capacitance. For low frequency applications, mostly higher value capacitance is used that increases the size of capacitor (which requires large area on silicon chip and thus not suitable, from the view point of IC fabrication) [161] [162]. Consequently, to

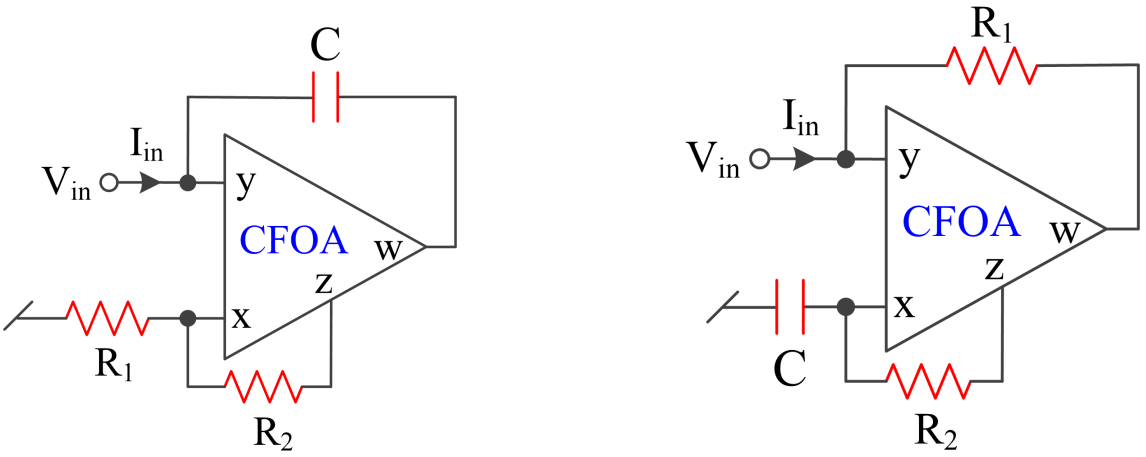
alleviate these limitations, researchers and circuit designers stimulate various positive and negative capacitances using CM circuits employing different active building blocks. These CM circuits may find numerous applications in the design of low frequency filters, low frequency oscillators and integration of a phase locked loop filter. Previously, a large number of negative CM circuits with different properties employing various active building blocks (ABB) have been reported in [80] [119] [155] [156] [157] [163]. Since this chapter deals with capacitance multiplier circuits realised with single CFOA, it is worthwhile to present a brief description of previously reported CM circuits realised with CFOAs.

In [131], six different negative capacitance multiplier circuits have been reported. Wherein four of the presented circuits employ two CFOAs with all grounded passive elements while the other two circuits require only a single CFOA, two resistors and one capacitor. In the first circuit (Fig. 4 of [131]) shown here in Fig. 2.1(a) capacitor is floating whereas in second configuration (Fig. 5 of [131]) displayed in Fig. 2.1(b), a grounded capacitor is used.

In [132], various grounded immittance function simulators have been presented out of which one circuit provides a negative capacitance multiplier realized with single CFOA, a grounded capacitor and three resistors (two of them are grounded and one is floating) with a matching condition of two resistors. This negative CM circuit is shown in Fig. 2.2.

The negative capacitance multiplier circuit of Fig. 2.3 using an inverting CFOA, two resistors and one capacitor has been reported in [133]. This circuit design exhibits minimal susceptibility to temperature fluctuations. Through PSPICE simulations, the obtained results corroborate the theoretical analysis across the frequency range of 100KHz to 6MHz.

In [134], an inverting CFOA, one grounded capacitor and two resistors based grounded



(a) C_{eq} = -C$R_2/2R_1$ (b) C_{eq} = -C$R_2/2R_1$

Figure 2.1: Negative grounded capacitance multiplier circuits reported in [131]

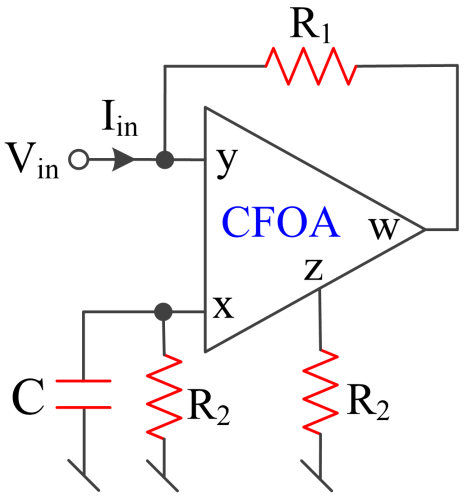


Figure 2.2: Negative capacitance multiplier circuit proposed in [132], C_{eq} = -CR_2/R_1

CM configuration has been proposed. The multiplication factor of the reported circuit works satisfactorily within the frequency range of 1Hz to 30kHz.

In [135], a negative lossless grounded capacitance multiplier circuit employing a single CFOA, four resistors, and a grounded capacitor has been presented. To enhance power efficiency, the CFOA's internal structure utilizes dynamic threshold-voltage MOSFET (DTMOS) transistors.

In [136], two grounded capacitance multiplier circuits (Fig. 3 of [136]) have been

proposed which employ one modified CFOA, two resistors and one capacitor without requiring critical active and passive component-matching conditions (Fig. 2.4).

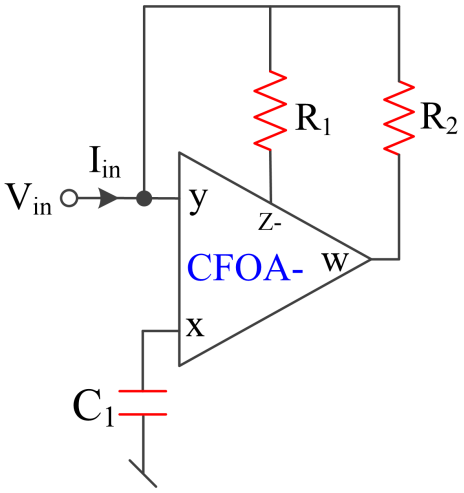
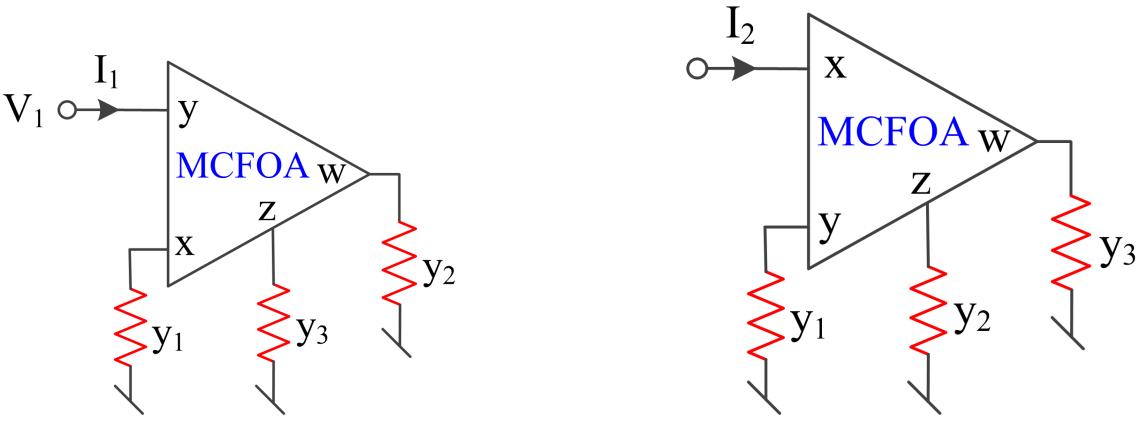


Figure 2.3: Grounded capacitance multiplier circuit proposed in [133], $C_{eq} = C_1(1+R_2/R_1)$

In [137], three unified structures of immittance simulators were proposed, requiring a single CFOA and four/five impedances/admittances. Different combinations of these impedances/admittances yield different immittance functions, such as lossy/lossless inductors and capacitance multipliers, and grounded frequency-dependent positive



(a) $C_{eq} = C_1G_2/G_3$ (b) $C_{eq} = C_1G_2/G_3$

Figure 2.4: Grounded capacitance multiplier proposed in [136]

resistances. Two of the three configurations provide capacitance multiplier and grounded negative capacitance divider circuits.

From the above description, it appears that no single CFOA-based negative capacitance multiplier has been presented yet which can provide high multiplication factor (greater than 1200) employing grounded capacitor without any passive component matching condition(s).

After thoroughly reviewing the available literature and considering the key factors for the realization of a CM circuit, this chapter introduces a new topology for negative grounded capacitance multiplier circuits. The proposed circuits utilize a CFOA, one capacitor, and two resistors. The ability to achieve negative capacitance multiplication by varying the resistance values is discussed in Section 2.2.

2.2 The Proposed Negative Grounded Capacitance Multiplier Circuits

In this section, three negative grounded capacitance multiplier configurations are presented. The proposed circuits employ only a single current feedback operational amplifier (CFOA), two resistors and one capacitor which are displayed in Fig.2.5[1].

The circuits shown in Fig. 2.5(a) and Fig. 2.5(c) have been designed, using a methodology similar to the one proposed in [164] for the design of a positive grounded capacitance multiplier circuit, as shown in Fig. 2.6(a) whereas the NGCM circuit proposed in Fig. 2.5(b) is designed using an approach similar to the one proposed in [165] as given in Fig. 2.6(b). Topologically, the circuit of Fig. 2.5(b) is similar to

[1]A. Raj, D. R. Bhaskar, M. Shrivastava, and P. Kumar, "New negative-grounded capacitance multiplier circuits," International Journal of Circuit Theory and Applications, vol. 51, no. 3, pp. 1476–1491, 2023.

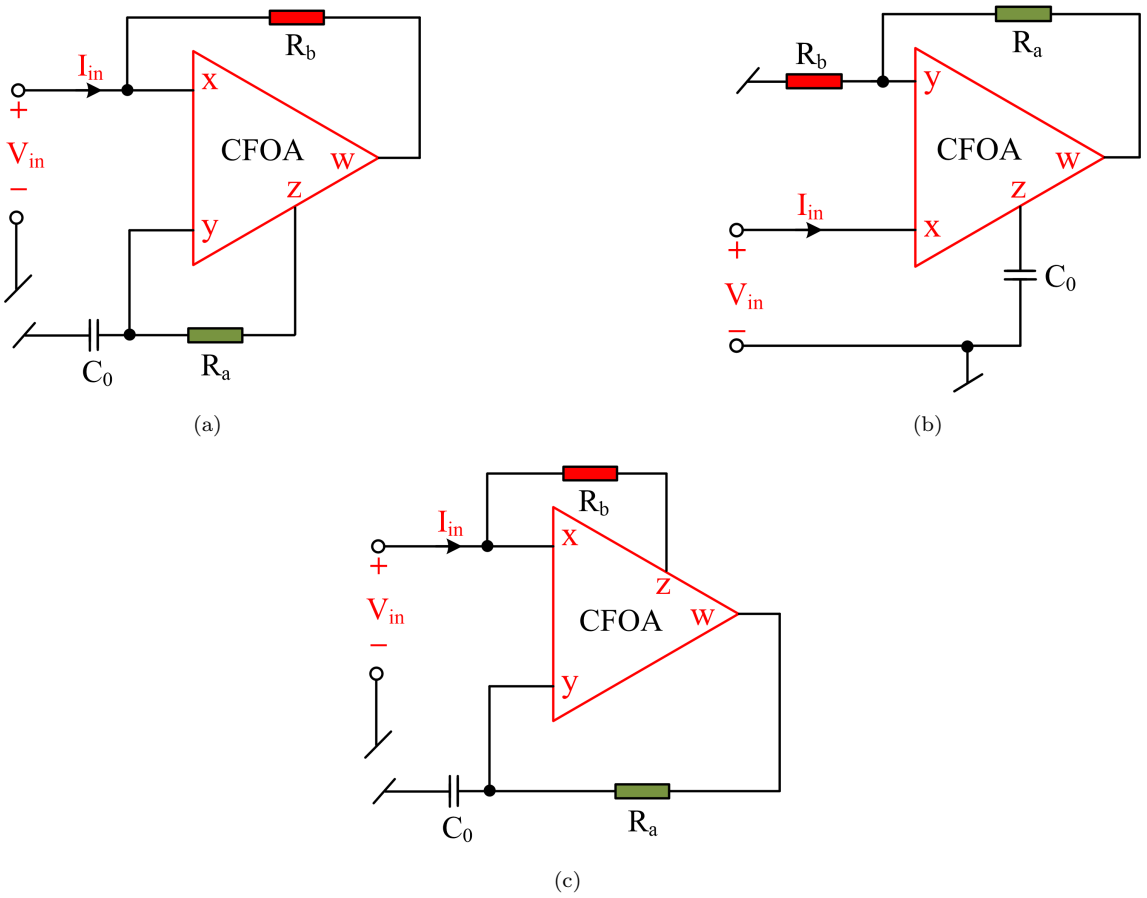


Figure 2.5: Proposed negative grounded capacitance multiplier circuits employing grounded capacitor

the circuit presented in[134]where an inverting CFOA (ICFOA) is used as an active element for realization of a positive CM circuit. Assuming ideal CFOA conditions: $I_y = 0$, $V_x = V_y$, $V_w = V_z$ and $I_z = I_x$, a routine circuit analysis of the circuits of Fig. 2.5 yields the input impedance of the first two proposed circuits (Fig. 2.5 (a) and Fig. 2.5 (b)) as:

$$\frac{V_{in}}{I_{in}} = Z_{in} = \frac{-1}{sC_0\left(1+\frac{R_a}{R_b}\right)} = \frac{-1}{sC_{eq1}} \tag{2.1}$$

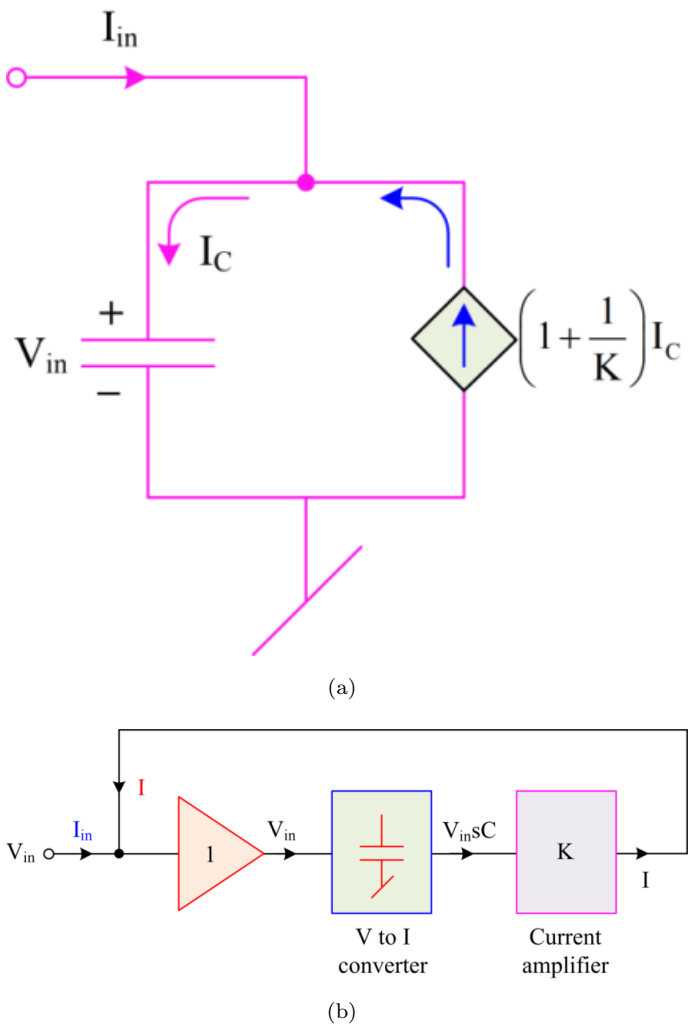


Figure 2.6: Approaches used for the realization of NGCM (a) current mode approach [164] (b) voltage mode approach [165]

while for the third proposed circuit (Fig.2.5(c)), the input impedance is expressed as:

$$\frac{V_{in}}{I_{in}} = Z_{in} = \frac{-R_b}{2sC_0R_a} = \frac{-1}{sC_{eq2}} \tag{2.2}$$

where

$$C_{eq1} = C_0\left(1 + \frac{R_a}{R_b}\right) \; and \; C_{eq2} = 2C_0\frac{R_a}{R_b} \tag{2.3}$$

The input impedances obtained from equations (2.1) and (2.2) yield negative capacitance whose multiplication factors may be adjusted by varying the resistances

R_a and R_b. For such realizations, no matching constraints have been required and also the proposed circuits utilize grounded capacitor which is beneficial from the view point of IC fabrication and parasitic absorption. A notable feature has been observed from the circuit of Fig. 2.5(b) that the multiplication factor of the proposed capacitance multiplier may be controlled electronically for which the tuning grounded resistor R_b can be replaced by a voltage controlled resistor.

2.2.1 Non-ideal Analysis

To analyse the effects of parasitic resistances and capacitances available at the input and output ports of CFOA, non-ideal analysis has been carried out for which a resistance r_x available at the X-terminal of CFOA is taken into account and at terminal-Z, a parallel combination of R_P and $1/sC_P$ has been considered. Complete non-ideal capacitance multiplier circuits of Fig. 2.5 are shown in Fig. 2.7.

Reanalysis of the circuits of Fig. 2.7 yield the following non-ideal impedances:

$$Z_{in1} = \frac{s^2(C_0C_pR_ar_xR_b) + sR_br_x(C_p + C_0(1+\frac{R_a}{R_p})) + (\frac{r_xR_b}{R_p} - R_b)}{s^2C_0C_pR_a(R_b+r_x) + s\{R_b(C_p+C_0) + C_0R_a(1+\frac{R_b}{R_p}) + C_0r_x(1+\frac{R_a}{R_p}) + C_pr_x\} + \frac{R_b+r_x}{R_p}} \tag{2.4}$$

$$Z_{in2} = \frac{sr_x\{R_b(C_p+C_0) + R_aC_0 + \frac{R_aR_bC_p}{Rp}\} + r_x(\frac{R_b+R_a}{R_p}) - R_b}{s\{R_b(C_p+C_0) + R_a(C_p+C_0)\} + \frac{R_b+R_a}{R_p}} \tag{2.5}$$

$$Z_{in3} = \frac{s^2C_0C_pR_aR_br_x + sr_x(C_pR_a + C_0R_b + \frac{C_0R_aR_b}{R_p}) + r_x(1+\frac{R_ar_x}{R_p}) - R_a}{s^2R_bC_0C_p(r_x+R_a) + s(C_pr_x + \frac{C_0R_br_x+C_pR_aR_b+C_0R_aR_b}{R_p} + 2C_0R_b) + \frac{r_x+R_a}{R_p}} \tag{2.6}$$

From equations (2.4) − (2.6) , it may be noted that the parasitic elements of the CFOA ($r_x = 50\Omega$, R_p = 3x106Ω and C_p = 4.5x10-12 F) affect the input impedances of the proposed NGCMs. These effects can be minimized with the proper selection

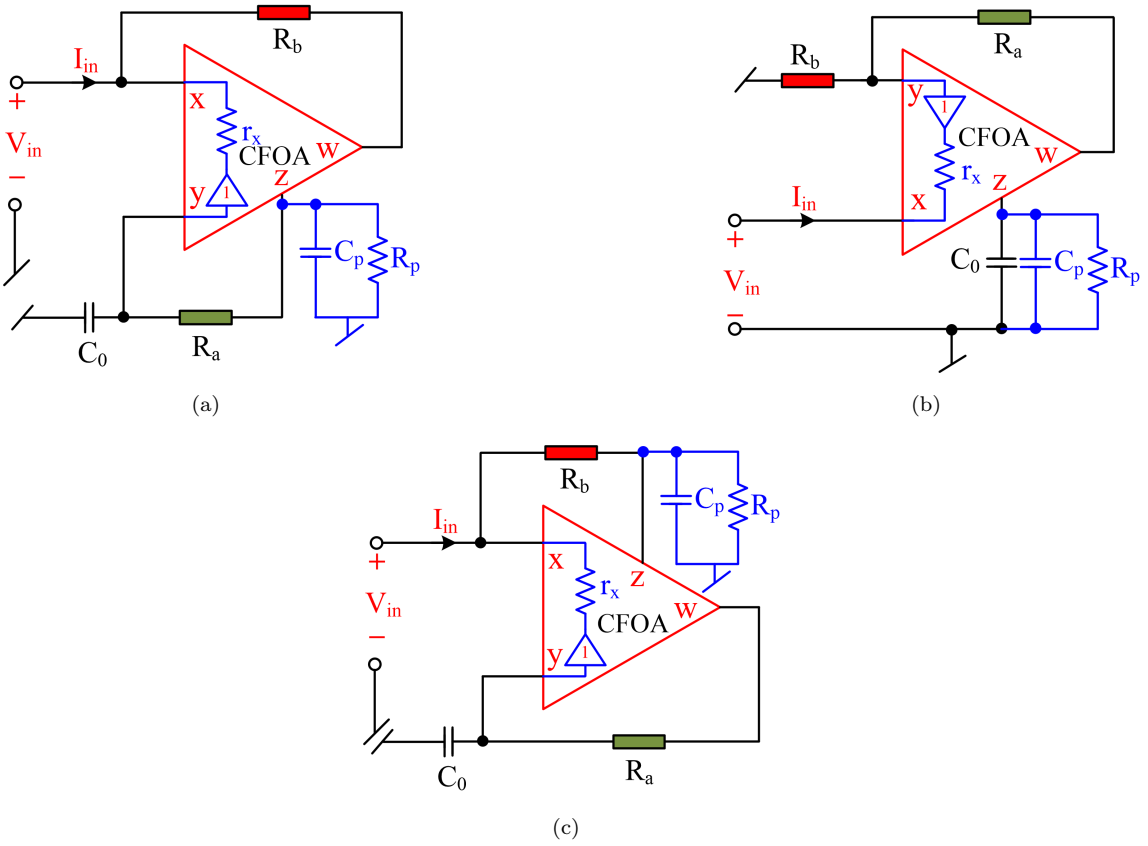
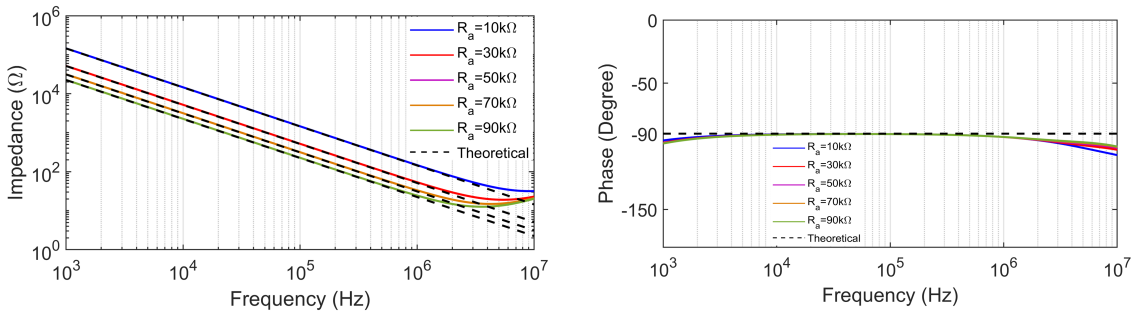


Figure 2.7: Complete proposed NGCMs with parasitic elements of CFOA

of the external passive components (R_a, $R_b \gg r_x$, R_a, $R_b \ll R_p$ and $C_0 \gg C_p$). Taking these considerations into account, the non-ideal impedances may turn into their ideal values as given in equations (2.1) and (2.2).

2.2.2 Simulation results

The functionality of the proposed circuits of Fig. 2.5 has been validated using macro model of AD844 in PSPICE simulator. The DC power supplies of value ± 12V were used to bias AD844. In simulation results, the variations in impedance and phase of the proposed NGCMs with frequency have been demonstrated. For the justification of robustness of the proposed NGCM circuits, Monte-Carlo simulations and temperature analysis have also been carried out. Noise analysis and power



(a) (b)

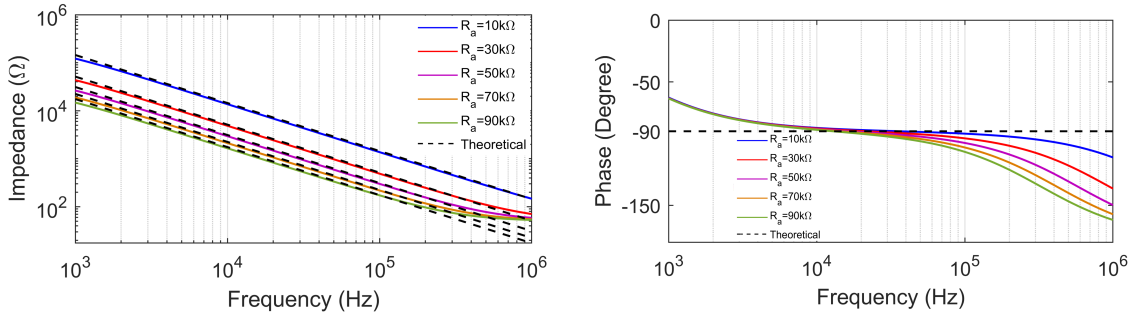
Figure 2.8: Frequency responses of (a) impedance and (b) phase of proposed capacitance multiplier of Fig. 2.5(a)

supply rejection ratio (PSRR) analysis have also been carried out for all the presented circuits.

2.2.2.1 Frequency responses

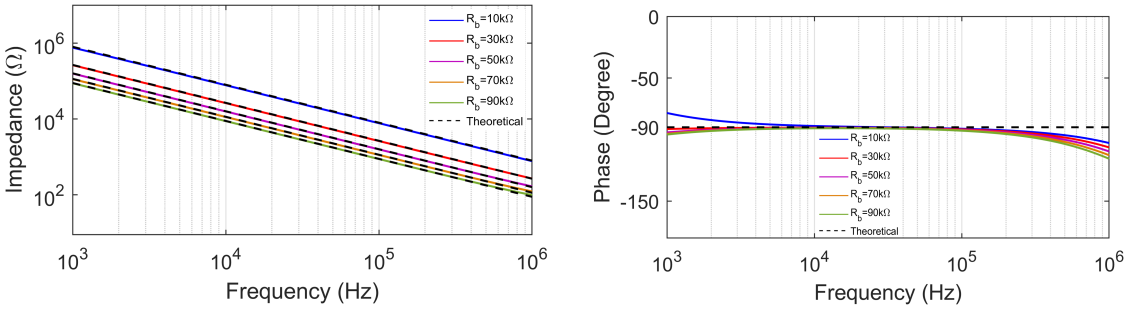
Frequency responses of the proposed circuits of Fig. 2.5 have been shown in Fig. 2.8 for which the passive components were chosen as: $R_b = 1$ kΩ, $C_0 = 100$ pF and $R_a =$ 10 kΩ, 30kΩ, 50kΩ, 70kΩ, 90kΩ resulting $C_{eq} =$ 1.1nF, 3.1nF, 5.1nF, 7.1nF, 9.1nF for Fig. 2.5(a) and Fig. 2.5(b) respectively whereas for Fig. 2.5(c), the component values were selected as: $R_b = 10$kΩ, $C_0 = 100$pF and $R_a = 10$kΩ, 30kΩ, 50kΩ, 70kΩ, 90kΩ resulting $C_{eq} =$ 0.2nF, 0.6nF, 1nF, 1.4nF, 1.8nF respectively. The theoretical (dashed lines) and simulated (coloured lines) impedances and their phases have been demonstrated in Fig. 2.8, Fig. 2.9 and Fig. 2.10 for the circuits of Fig. 2.5(a), Fig. 2.5(b) and Fig. 2.5(c) respectively.

From Fig. 2.8 - Fig. 2.10, it is observed that the magnitudes of impedance of all the proposed circuits are in good agreement with theoretical ones. The phases of the impedance of Fig. 2.5(a) and Fig. 2.5(c) are very close to their corresponding theoretical value i.e. 90° within the frequency range of 4kHz – 1MHz while for the circuit of Fig. 2.5(b), the phases are slightly deviates with its ideal value.



(a) (b)

Figure 2.9: Frequency responses of (a) impedance and (b) phase of proposed capacitance multiplier of Fig. 2.5(b)



(a) (b)

Figure 2.10: Frequency responses of (a) impedance and (b) phase of proposed capacitance multiplier of Fig. 2.5(c)

For the variation in capacitance value, resistor R_a was varied during simulations from 100kΩ to 1000kΩ for the circuits of Fig. 2.5(a), Fig. 2.5(c) and for the circuit of Fig. 2.5(b), R_a was varied from 10kΩ to 200kΩ. The results of simulated multiplication factor with their corresponding theoretical values have been displayed in Fig. 2.11.

From Fig. 2.11, it is seen that the variation in multiplication factor with the variation of resistor R_a for the circuits of Fig. 2.5(a) and Fig. 2.5(c) are in good agreement with their corresponding theoretical values with maximum percentage error of 3% while in the case of Fig. 2.5(b), for lower value of capacitance, the performance of the circuit is in good agreement with their theoretical ones. A sample

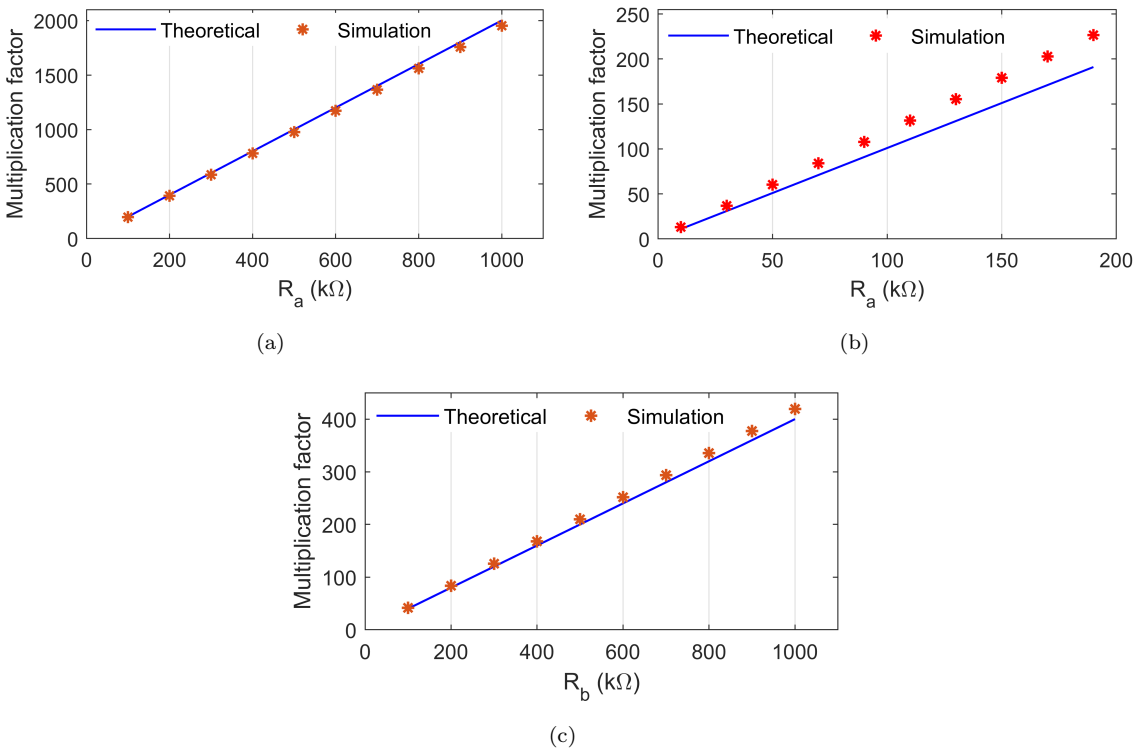


Figure 2.11: Variation of multiplication factor for different values of tuning resistor (a) Fig. 2.5 a (b) Fig. 2.5 b (c) Fig. 2.5 c

frequency response of capacitance of the circuit of Fig. 2.5(a) has also been displayed in Fig. 2.12 for which the passive component values were chosen as $R_b = 0.5\text{k}\Omega$, $C_0 = 100\text{pF}$ and R_a was varied from $200\text{k}\Omega$ – $2000\text{k}\Omega$.

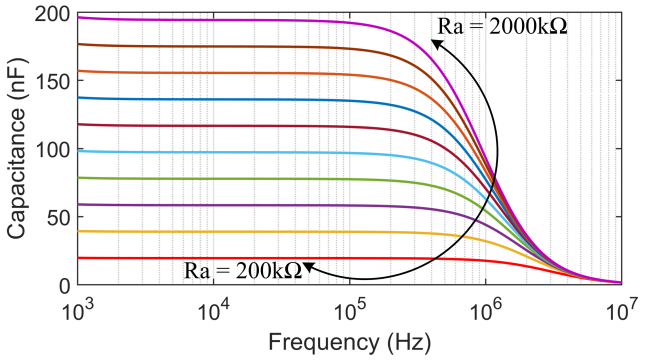
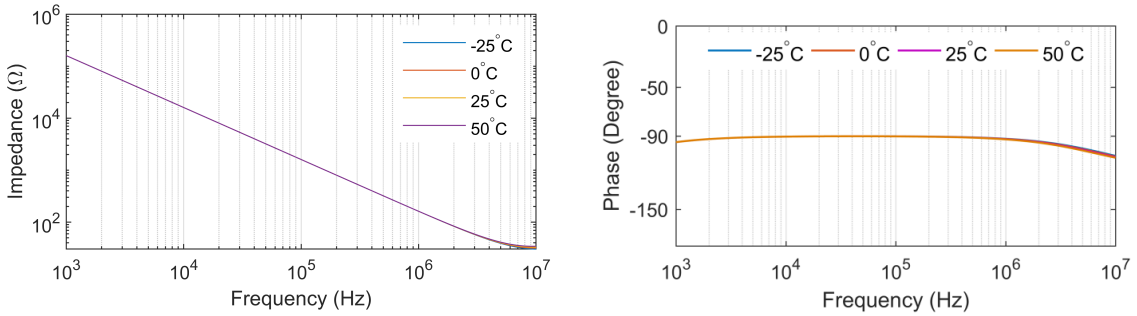


Figure 2.12: Variation in capacitance with frequency by varying resistor R_a of Fig. 2.5(a)



(a) (b)

Figure 2.13: Frequency responses of impedance and phase of capacitance multipliers at different temperatures for Fig. 2.5(a)

From Fig. 2.12, it is observed that the maximum value of capacitance for the circuit of Fig. 2.5(a) obtained through simulations is around 195.16nF which is close to their corresponding theoretical value of 200.1nF with a percentage error of 2.46%.

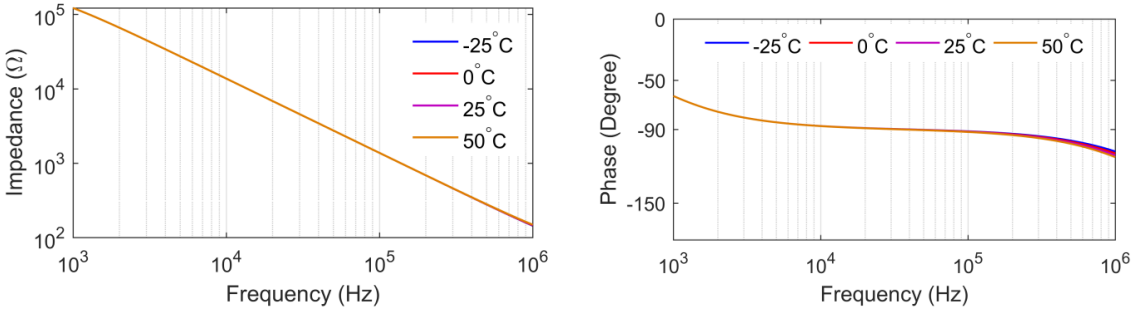
2.2.2.2 Temperature variation analysis

The proposed circuits were also simulated at different temperatures for testing the performance of the robustness and validated by varying the temperature from -25°C to 50°C. The frequency responses of the impedance and phase for different temperatures of the circuits of Fig. 2.5(a-c) have been displayed in Fig. 2.13, Fig. 2.14 and Fig. 2.15 respectively.

From the results displayed in Fig. 2.13 - Fig. 2.15, it can be seen that the effect of temperature on the impedance and phase of the proposed NGCMs are insignificant and thus, the proposed NGCM circuits are insensitive with the temperature.

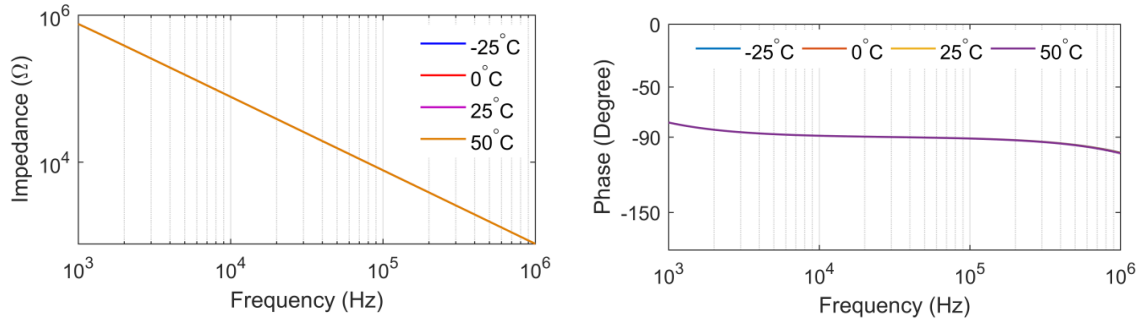
2.2.2.3 Monte-Carlo simulations

The robustness of the proposed capacitance multipliers has also been tested using Monte-Carlo simulations for which the circuits were run for 100 samples with 10%



(a) (b)

Figure 2.14: Frequency responses of impedance and phase of capacitance multipliers at different temperatures for Fig. 2.5(b)

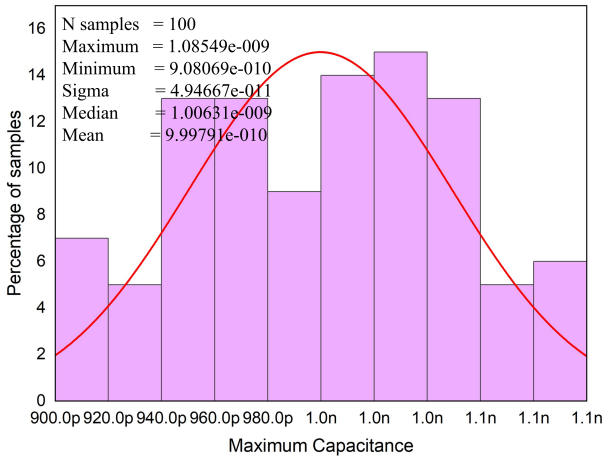


(a) (b)

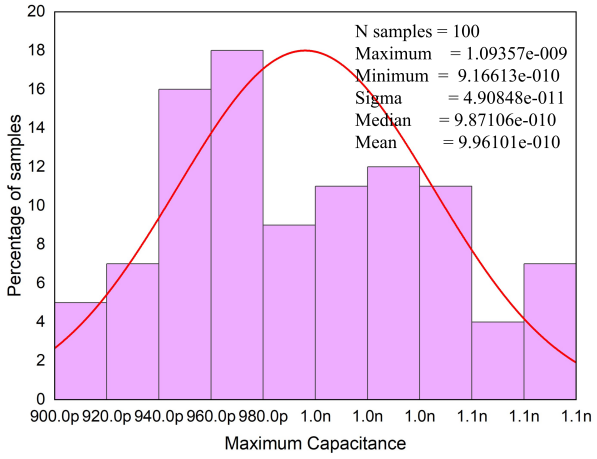
Figure 2.15: Frequency responses of impedance and phase of capacitance multipliers at different temperatures for Fig. 2.5(c)

tolerance in resistors and the capacitor. The resulting histograms for the variation in maximum capacitance due to these tolerances have been displayed in Fig. 2.16 - Fig. 2.18. In Fig. 2.16 (a-c), the changes in maximum capacitance due to variations in R_a, R_b and C_0 for the circuit of Fig. 2.5(a) have been demonstrated. Similarly, the histograms of maximum capacitance with the variation in R_a, R_b and C_0 for the circuits of Fig. 2.5(b) and Fig. 2.5(c) have been displayed in Fig. 2.17 (a-c) and Fig. 2.18 (a-c) respectively.

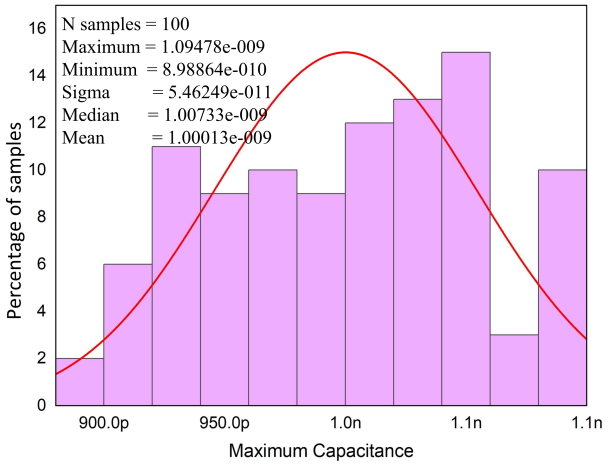
The histogram results shown in Fig. 2.16 - Fig. 2.18 obtained from Monte-Carlo simulations have been concluded in Table 2.1 in which the maximum and minimum capacitance value have been provided for the theoretical value of 1nF.



(a)

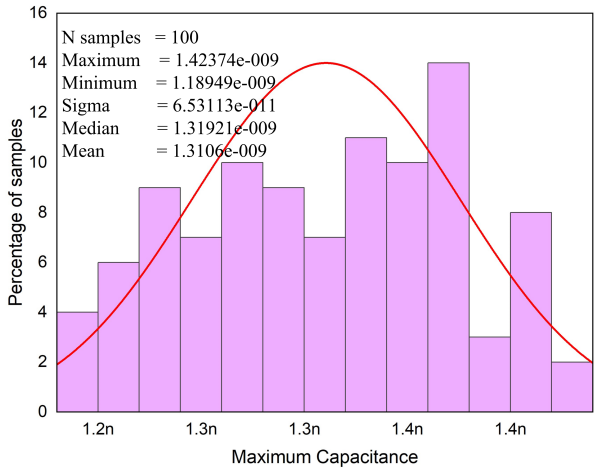


(b)

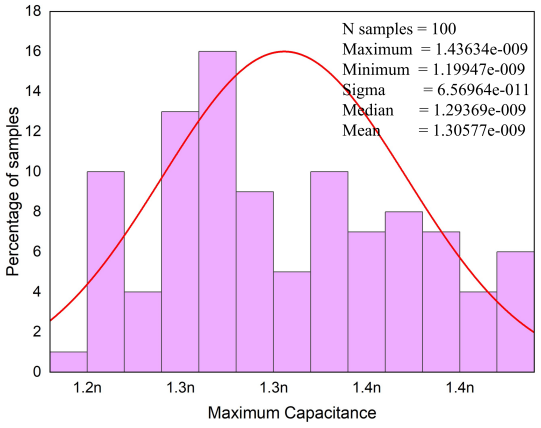


(c)

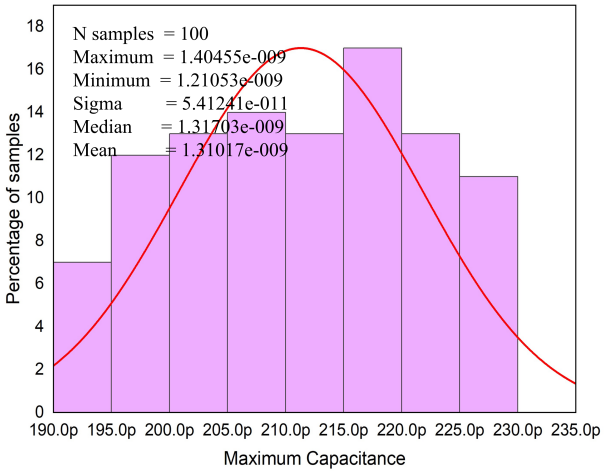
Figure 2.16: Histograms of the circuits of Fig. 2.5(a) obtained through Monte-Carlo simulations



(a)

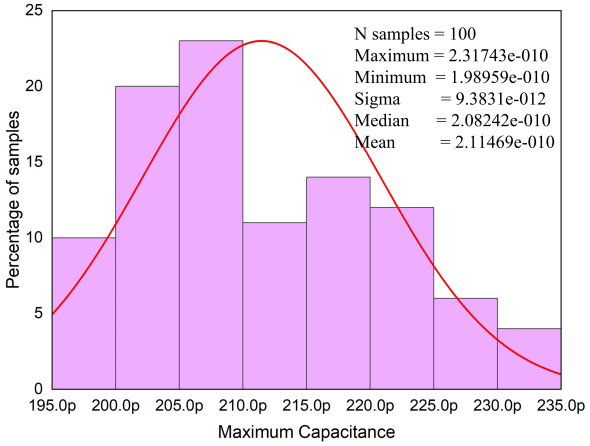


(b)

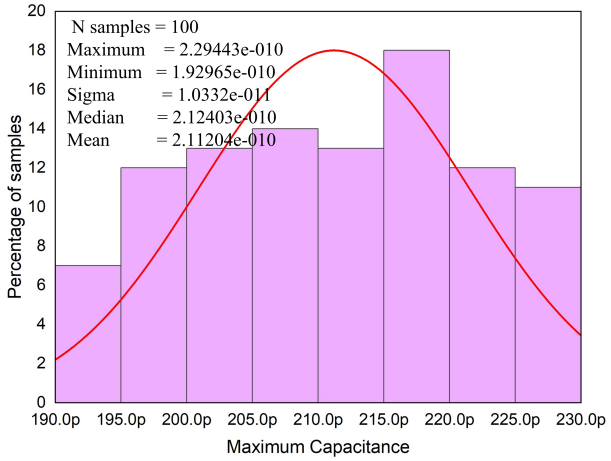


(c)

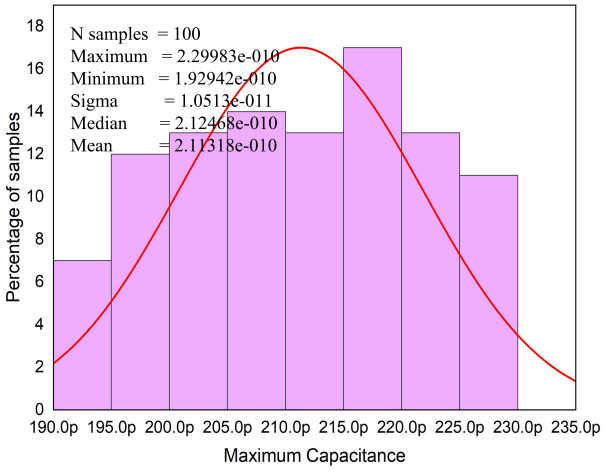
Figure 2.17: Histograms of the circuits of Fig. 2.5(b) obtained through Monte-Carlo simulations



(a)



(b)



(c)

Figure 2.18: Histograms of the circuits of Fig. 2.5(c) obtained through Monte-Carlo simulations

Table 2.1: Statistical data obtained from Monte-Carlo simulations

	Variation in capacitance due to R_a			Variation in capacitance due to R_b			Variation in capacitance due to C_0		
	Max (nF)	Min (nF)	Sig (nF)	Max (nF)	Min (nF)	Sig (nF)	Max (nF)	Min (nF)	Sig (nF)
Fig. 2.7a	1.08549	0.908069	0.0494	1.09357	0.91663	0.049	1.09478	0.898864	0.054
Fig. 2.7b	1.29382	1.083	0.05877	1.30517	1.09197	0.05913	1.2774	1.1011	0.049
Fig. 2.7c	1.13547	0.92794	0.05755	1.12464	0.91895	0.05735	1.12048	0.92313	0.05

From Table 2.1, it is concluded that the deviation in capacitance (maximum and minimum) value due to variations in resistors (R_a and R_b) and capacitor (C_0) has been found insignificant.

2.2.2.4 Noise and power supply rejection ratio analysis

To observe the effect of noise on MF of NGCM circuits, we have carried out noise analysis in PSPICE by varying the resistors R_a used in the circuits of Fig. 2.5. For such analysis, resistor R_a was varied from 50kΩ – 200kΩ. The resulting input noise (in $\mu V\sqrt{Hz}$) for all three circuits presented in Fig. 2.5 have been displayed in Fig. 2.19(a-c).

We have also simulated the power supply rejection ratio (PSRR) for the proposed NGCM circuits for which a voltage of magnitude 0.5V was superimposed on the nominal DC power supply voltage (alternately with both positive and negative bias) and PSRR was measured at input node of the simulate NGCMs. AC responses of the PSRR in the working range of the proposed NGCM circuits (1kHz – 1MHz) is shown in Fig. 2.20(a-c).

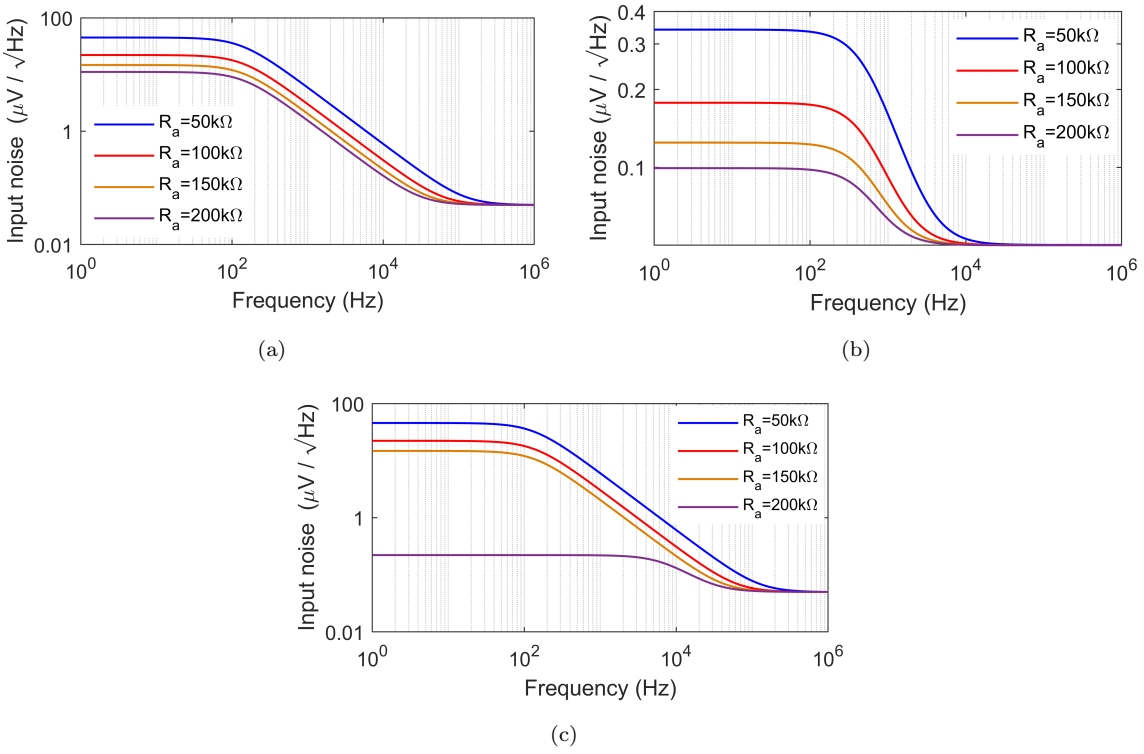


Figure 2.19: Effect of noise on proposed NGCM circuits for different values of resistors R_a for (a) Fig. 2.5(a), (b) Fig. 2.5(b), (c) Fig. 2.5(c)

From Fig. 2.19(a-c), it is noted that the maximum input noises observed in the presented circuits of Fig. 2.5 are below to $100\mu\text{V}\sqrt{Hz}$ for Fig. 2.5(a) and Fig. 2.5(c) while for Fig. 2.5(b), it is below to $0.35\mu\text{V}\sqrt{Hz}$. From Fig. 2.20, the minimum value of PSRR for the proposed NGCM circuits were obtained as -66.14dB (251kHz), -79.53dB (79.43kHz) and -66.25dB (323.2kHz) for Fig. 2.5(a), Fig. 2.5(b) and Fig. 2.5(c) respectively.

2.2.3 Experimental results

To test the performance of the proposed circuits experimentally, the circuits of Fig. 2.5 were bread-boarded with commercially available IC AD844 type CFOA using 5% tolerance resistors and 10% tolerance capacitor. For the validation of time responses

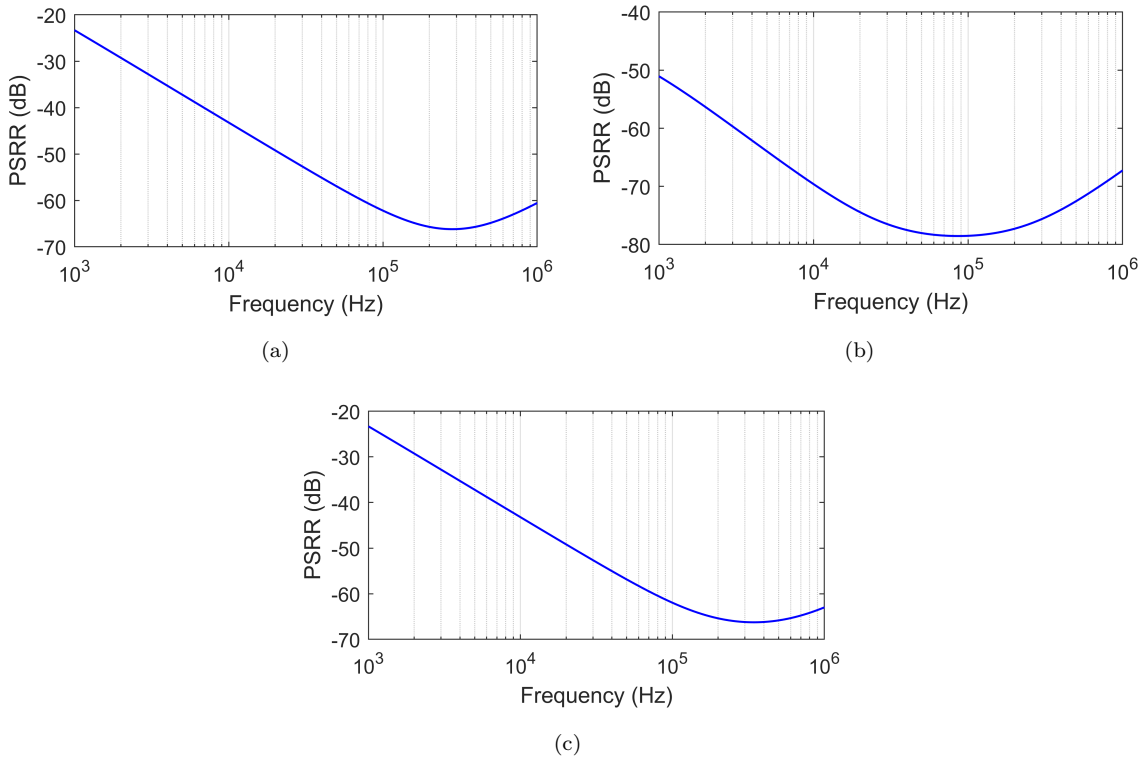


Figure 2.20: Simulated PSRR of the proposed NGCM circuits for (a) Fig. 2.5(a), (b) Fig. 2.5(b) (c) Fig. 2.5(c)

of the given NGCM circuits, the NGCM circuits were driven by a sinusoidal current (obtained by a V-I converter as shown in Fig. 2.21) and the corresponding voltage responses were obtained to determine the corresponding capacitance and multiplication factors. The complete circuit realization of one of the proposed circuits has been displayed in Fig. 2.21 based on which the experimental results were performed. A sinusoidal input voltage with amplitude 6V peak-peak was taken and the frequency was set at 10 kHz for generating an input current (I_{in}) of amplitude 1.2mA peak –peak by choosing the value of resistor R = 5 kΩ. The experimental set-up of the circuit of Fig. 2.5(a) has also been demonstrated in Fig. 2.22. The power supply voltages used for the biasing of AD844s were selected as ±12V. The circuit of Fig. 2.5(a) was tested experimentally for different values of multiplication factor (MF) for which the passive components used were: $R_b = 1\text{k}\Omega$, $C_0 = 100\text{pF}$ and $R_a = 10\text{k}\Omega$,

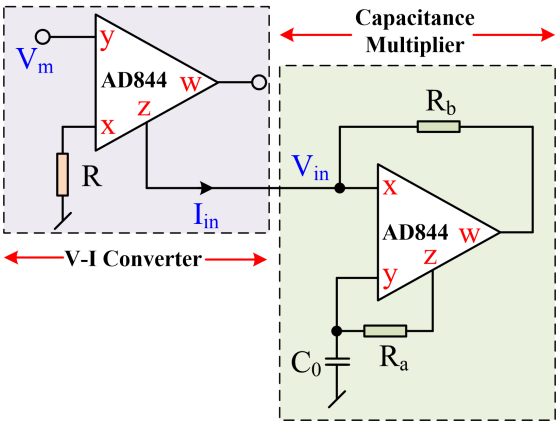


Figure 2.21: Complete circuit realization of current excited negative capacitance multiplier circuit of Fig. 2.28(a)

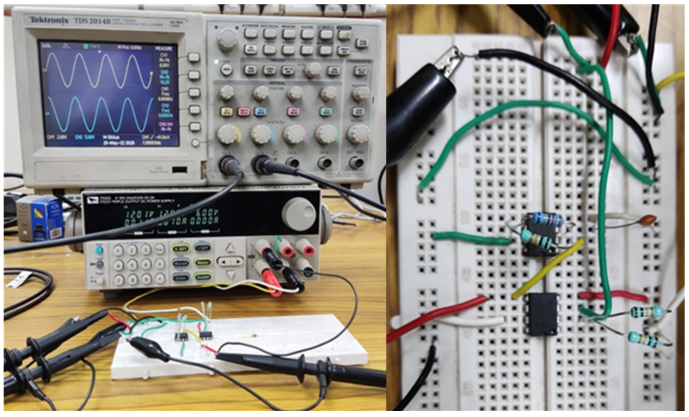


Figure 2.22: Experimental setup of circuit of Fig. 2.5(a)

100kΩ, 563kΩ and 1000kΩ corresponding to the MF equal to 11, 101, 564 and 1001 respectively. The experimental input voltage supplied to the circuit (corresponding to the input current) and the input voltage applied to NGCM of the circuit of Fig. 2.5 for different values of MF have been displayed in Fig. 2.23.

From Fig. 2.23, the magnitude of impedance of the Fig. 2.5(a) has been calculated from which the equivalent capacitance values, and therefrom the corresponding MFs have been evaluated. From the results of Fig. 2.23, the experimental capacitance values are obtained as 1.122nF, 9.937nF, 56.118nF and 95.398 corresponding to theoretical values of 1.1nF, 10.1nF, 56.4nF and 100.1nF for different values of R_a = 10kΩ, 100kΩ, 564kΩ and 1000kΩ respectively. The multiplication factors have been

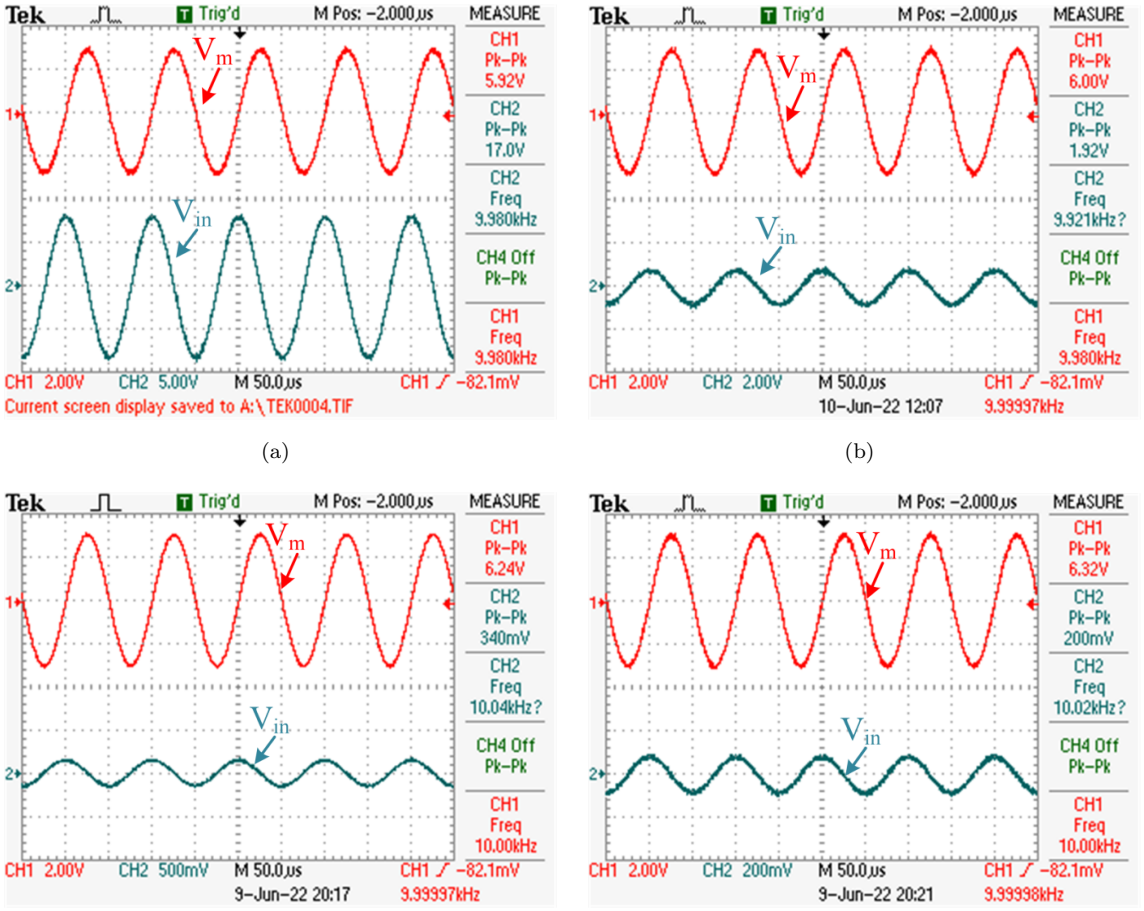
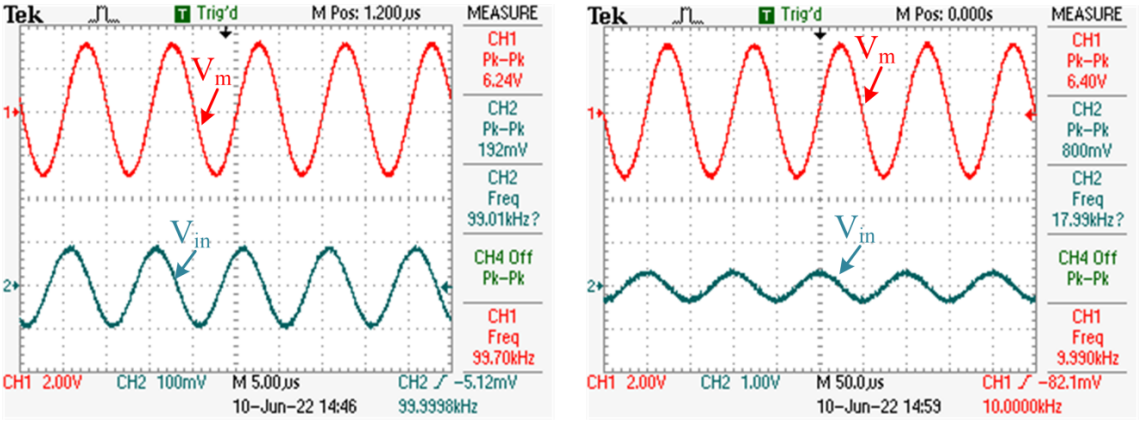


Figure 2.23: Time domain input and output waveforms of the proposed circuit of Fig. 2.5(a) for different values of MFs

evaluated therefrom which are 11.22, 99.375, 561.18 and 953.9 for the designed values of 11, 101, 564 and 1001 with maximum percentage error of 4.6%. The phase between V_m and V_{in} (shown in Fig. 2.21) have also been recorded experimentally and found to be -91.2°, -93°, -90.4° and -91.9° which are very close to their corresponding ideal value -90°.

Similarly, the sample results of time domain responses of the circuits of Fig. 2.5(b) and Fig. 2.5(c) have also been shown in Fig. 2.24 using the following passive components: $R_a = 100\text{k}\Omega$, $R_b = 1\text{k}\Omega$ and $C_0 = 100\text{pF}$ and correspondingly the MFs yield to be 101 and 200 respectively. The experimentally obtained capacitance values are



(a) (b)

Figure 2.24: Time domain waveforms for the circuits (a) Fig. 2.5(b) (b) Fig. 2.5(c)

9.937nF and 21.8nF and the MFs of both the circuits have been evaluated as 99.37 and 218 which are in close proximity with the theoretical values (101 and 200) with maximum percentage error of 9%.

The phase difference between input and output waveforms of the results shown in Fig. 2.24 have been obtained experimentally and are found to be -87°, and -90° respectively which are very close with the theoretical values. The Experimental verification of capacitance values of the proposed NGCM circuits for different multiplication factors have also been carried out. Theoretical and experimental results of capacitance with multiplication factors for the circuits displayed in Fig. 2.5 have been shown in Fig. 2.25. From Fig. 2.25, it is seen that the experimentally obtained value of capacitance of circuit of Fig. 2.5(a) for different values of MF (upto 1000) matches well with its theoretical value while experimentally obtained capacitance of circuit of Fig. 2.5(b) and Fig. 2.5(c) matched well with their theoretical counterparts for MF upto 120 and 300 respectively. Thus, the simulated and experimental results demonstrated in Fig. 2.8 – Fig. 2.25 validate the feasibility of the proposed NGCM circuits.

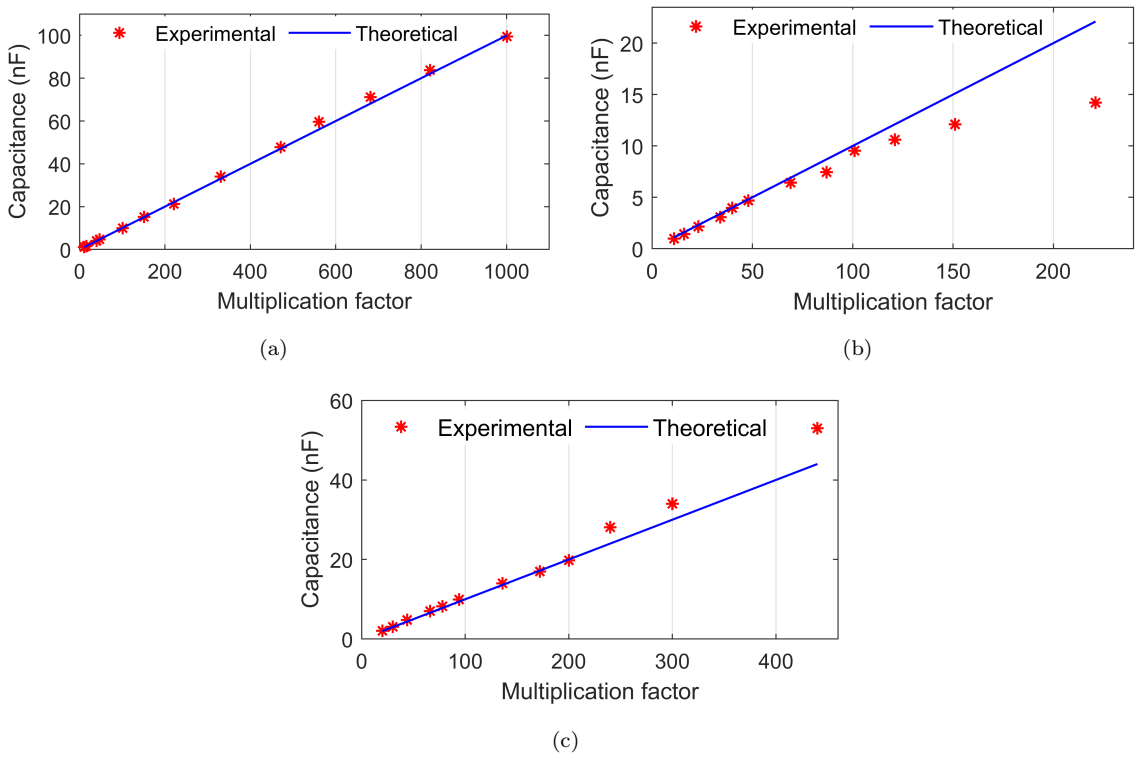


Figure 2.25: Variation in capacitance value for different multiplication factors

2.3 Floating immittance simulator circuits using CFOAs

Floating immittance simulators are circuits that are designed to simulate passive components—resistors, capacitors , and inductors in a floating configuration, meaning they are not directly grounded. These simulators are especially beneficial in integrated circuit (IC) design, where the incorporation of actual inductors is frequently unfeasible due to spatial limits and other limitations. Over the years, a large number of floating immittance simulator circuits of lossless/lossy type using various active building blocks have been presented in [166] [167] [168] [169] [170] [171] [172] [173] [174] [175] [176] [177] [178] [179] [180] [181] [182] [183] [184] [185]. CFOA is widely used in the design of various structures of immittance simulators

due to its significant advantageous features of offering very high slew rate (2000V/µs for AD844 type CFOA), elimination of the gain-bandwidth conflict, having accessibility of compensation pin (TZ) that provides additional flexibility in analog circuit design as compared to conventional op-amp. Various research groups around the world have reported different configurations of floating immittance simulators i.e., floating series/parallel R-L and R-C circuits, as well as floating FDNR, floating lossless inductor, and floating capacitance multiplier circuits using CFOAs [186].

The work presented in this chapter pertains to floating-type lossless inductor, parallel/series R-L, parallel/series R-C, parallel/series C-D, floating lossless capacitance multiplier circuits and floating FDNR, a brief review of previously reported CFOA-based floating immittance simulators are included to put the presented work in proper perspective.

In [140], a floating generalized impedance converter using four CFOAs and five impedances (Fig. 2.26) has been reported. The presented circuit can provide floating FDNR, floating inductance, and floating capacitor using appropriate choice(s) of impedances.

A lossy/lossless synthetic floating inductance simulator, which employs two CFOAs, two capacitors, and three resistors shown in Fig. 2.27, has been presented in [141]. The circuit presented in [141] lacks independent tunability features for inductance. In [142], a floating series R-L simulator circuit has been reported using two CFOAs, two resistors and one capacitor. This circuit allow independent tunability of inductance using a single resistor without requiring any matching constraints.

Furthermore, a floating lossless inductor realization, derived from a filter configuration reported in [143], is presented in [144]. This circuit employs three CFOAs, one

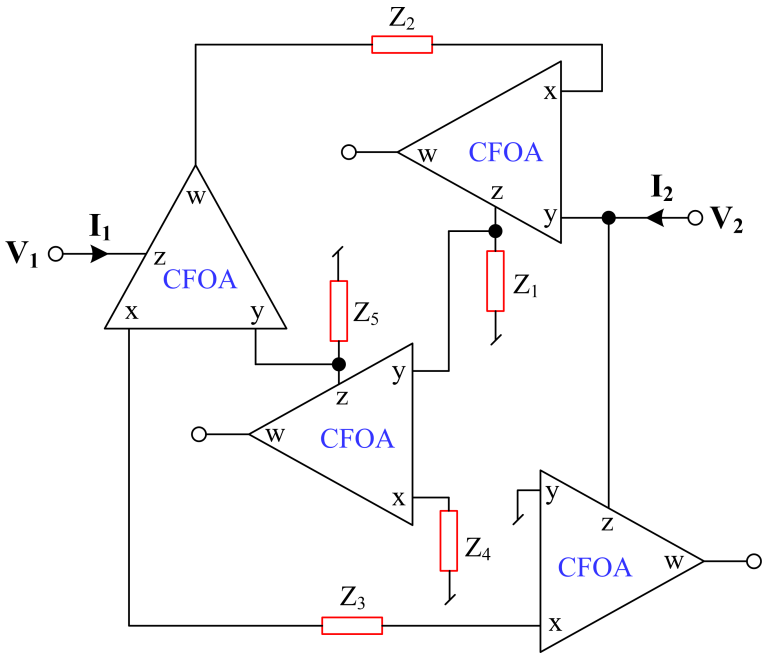


Figure 2.26: Generalized impedance converter circuit proposed in [140],Z_{1-2}=$Z_2Z_3Z_4/Z_1Z_5$

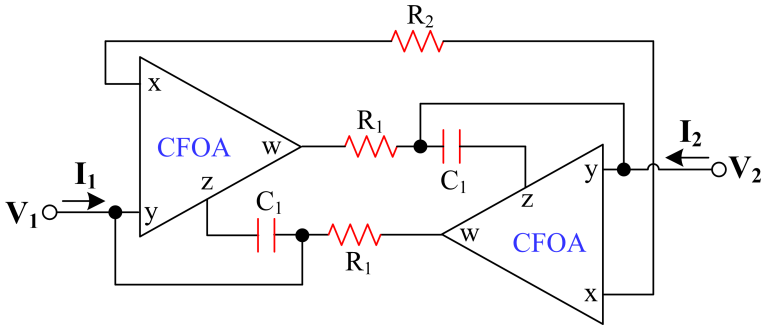
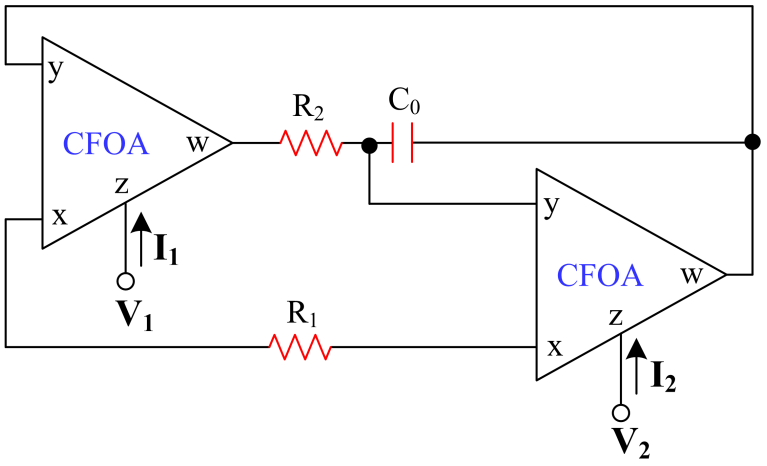


Figure 2.27: Floating inductor proposed in [141], Y_{1-2} = (R_2-R_1/R_1R_2)+1/s$C_1R_1R_2$

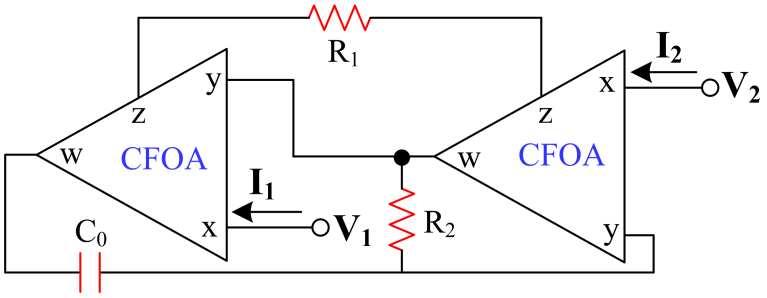
grounded capacitor, and two resistors (one of which is replaced by an array of resistors and a controlled NMOS for digital tuning), providing independent tunability.

Additionally, two configurations of series R-L (Fig. 2.28(a)) and parallel R-L (Fig. 2.28(b)) simulators employing two CFOAs, two resistors and one capacitor have been presented in [145]. Both circuits possess independent tunability features of inductance and do not require any component matching constraints.

A lossless negative immittance emulator using three CFOAs and three impedances



(a) $Y_{1-2}=1/(R_1+sR_1R_2C_0)$



(b) $Y_{1-2}= (1/R_1)+(1/sR_1R_2C_0)$

Figure 2.28: (a) Floating simulator (b) Floating inductor simulator proposed in [145]

has been presented in [146]. This emulator discusses floating negative lossless inductance, resistance, and capacitance multipliers, with the proper choice(s) of impedances, all of which have independent controllability.

In [147], four floating immittance simulator circuits (positive/negative) are presented. Three of these circuits utilize three CFOAs and three impedances, while the fourth circuit employs two CFOAs and three impedances. These emulators are capable of realizing both lossy and lossless inductance and capacitance multiplier circuits, depending on the appropriate selection(s) of impedances.

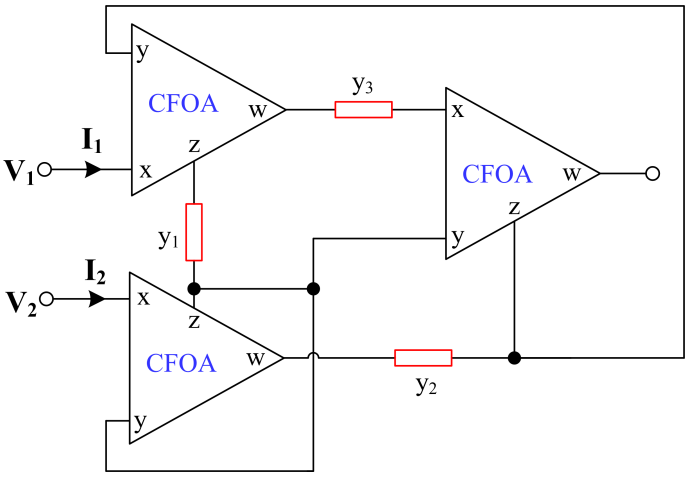
Additionally, [148] reports seven configurations of floating immittance realization

circuits, using two CFOAs along with three to four impedances. These configurations enable the realization of various lossy/lossless and positive/negative impedance functions by appropriately selecting the impedances.

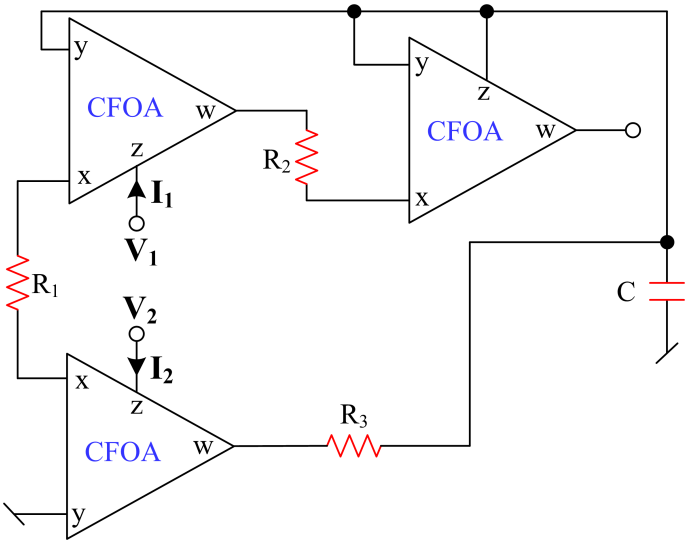
In [149], a unified configuration of an immittance simulator circuit has been reported. This circuit employs three CFOAs to provide floating frequency-dependent resistor and floating capacitance multiplier functions, achieved by properly selecting three admittances as displayed in Fig. 2.29(a) . The derived circuits possess independent tunability features and do not necessitate any matching constraints. A simulated floating inductor (SFI) has also been presented as shown in Fig. 2.29(b). The SFI design includes three resistors and a grounded capacitor, with only one resistive matching condition.

In [150], a lossless floating immittance simulator (FIS) based on an inverting CFOA has been presented. The proposed FIS can achieve a floating capacitance multiplier (FCM), a simulated floating inductor (SFI), and a floating frequency-dependent negative resistor (FFDNR) by selecting appropriate passive elements. The design is implemented with a minimal number of passive components and does not require any resistor or capacitor matching conditions, although all the passive elements are chosen to be floating.

From the preceding descriptions, it is clear that, despite the existence of a number of floating lossy/lossless parallel R-L, parallel R-C, parallel C-D, and capacitance multiplier circuit realizations using various active building blocks, research on novel realizations of these circuits is still on-going. To the best of our knowledge, no existing floating immittance simulator circuit based on CFOA has been reported that is capable of offering four distinct functions: floating parallel R-L, parallel R-C, parallel C-D, and lossless floating capacitance multiplier circuits. Hence, in this chapter, we present a new floating immittance simulator circuit employing three



(a) Y_{1-2}=y_1y_2/y_3



(b) Y_{1-2}=$1/R_1$(sCR_2R_3+R_2-R_3)

Figure 2.29: (a) Floating simulator (b) Floating inductor simulator proposed in [149]

CFOAs, capable of producing parallel R-L, parallel R-C, parallel C-D, and lossless floating capacitance multiplier circuits through appropriate selection of three passive elements. The presented floating parallel simulator circuit can be also modified as floating lossless immittance simulator and floating series immittance simulator, as discussed in Section 2.4, Section 2.5 and Section 2.6.

2.4 Floating parallel immittance simulator

In this section, a new configuration of a floating parallel immittance simulator employing CFOAs has been presented.The proposed generalized topology for realizing parallel R-L, parallel R-C, parallel C-D, and lossless floating CM (with appropriate choice(s) of branch impedances), employing three CFOAs and three impedances is depicted in Fig. 2.30[2].

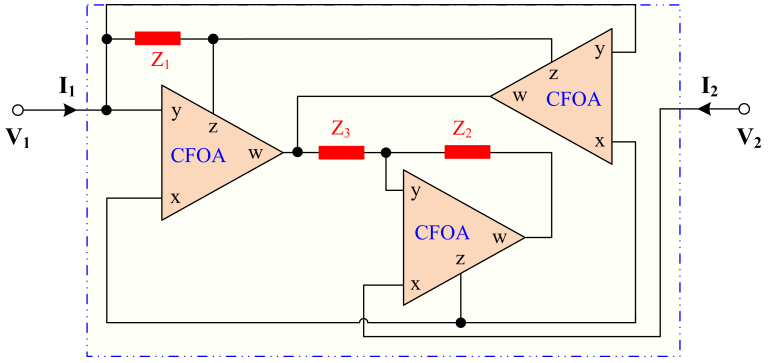


Figure 2.30: Proposed floating immittance simulator circuit

A routine analysis of the circuit of Fig. 2.30, using the voltage current relationships of CFOA, yields the following matrix equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{Z_1}\left[1+\frac{Z_3}{Z_2}\right]\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = Y_{in}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.7}$$

where

$$Y_{in} = \frac{1}{Z_1}\left[1+\frac{Z_3}{Z_2}\right] \tag{2.8}$$

Appropriate choice(s) of impedances Z_1, Z_2 and Z_3 obtained in equation (2.7) yield different types of immittance simulator circuits like floating parallel R-L, floating

[2]D. R. Bhaskar, M. Shrivastava, A. Raj, and P. Kumar, "Floating parallel lossy inductance, parallel lossy capacitance, parallel C-D, and lossless capacitance multiplier circuits using current feedback operational amplifiers," International Journal of Circuit Theory and Applications, vol. 52, no. 3, pp. 1489–1517, 2024.

parallel R-C, floating parallel C-D and lossless floating capacitance multiplier. The realizations of these circuits are described here.

Case I: To simulate a floating parallel R-L impedance using equation (2.7), one must select specific impedances: $Z_1 = R_1$, $Z_2 = R_2$, and $Z_3 = 1/\text{sC}$. The matrix equation that describes the parallel R-L circuit is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R_1} + \frac{1}{sR_1R_2} \end{bmatrix} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.9}$$

Case II: If the impedances of equation (2.7) are chosen as: $Z_1 = R_1$, $Z_2 = 1/\text{sC}$ and $Z_3 = R_2$, then the circuit of Fig. 2.30 yields a floating parallel R-C simulator whose matrix equation can be obtained as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R_1} + \frac{sCR_2}{R_1} \end{bmatrix} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.10}$$

Case III: If we select $Z_1 = 1/\text{s}C_1$, $Z_2 = 1/\text{s}C_2$, and $Z_3 = R_3$, the circuit depicted in Fig. 2.30 will simulate a floating parallel C-D simulator, and its matrix equation can be expressed as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = (sC_1 + s^2C_1C_2R_3) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.11}$$

Case IV: A lossless FCM can be simulated with $Z_1 = 1/\text{s}C_1$, $Z_2 = R_2$, and $Z_3 = R_3$.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = sC_1 \begin{bmatrix} 1 + \frac{R_3}{R_2} \end{bmatrix} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = sC_{eq} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.12}$$

From equations (2.9) – (2.12), it can be observed that the circuit presented in Fig. 2.30 can provide four different types of floating immittance simulator circuits. The

first and second realizations are floating parallel R-L and floating parallel R-C type simulator circuits in which inductance and capacitance can be independently controlled through resistor R_2 whereas in the parallel C-D simulator circuit, the value of D can be independently varied through resistor R_3. Lastly, from equation (2.12), when the circuit of Fig. 2.30 simulates a lossless floating capacitance multiplier, the value of equivalent capacitance C_{eq} has two degrees of freedom and can be independently controlled through resistors R_2 and/or R_3.

2.4.1 Non-Idealities of CFOAs on the proposed immittance simulator circuit

The effect of non-ideal gains of the CFOA on the proposed circuit has been evaluated using the terminal characteristic equations represented by $V_X = \beta V_Y$, $I_Z = \alpha I_X$ and $V_W = \gamma V_Z$, resulting into the non-ideal short circuit admittance matrix:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{Z_1} \begin{bmatrix} \frac{\gamma_1\beta_2 Z_2 + \gamma_2\beta_1\beta_2 Z_3}{\gamma_1\beta_2 Z_2} & -\frac{Z_3+Z_2}{\gamma_1\beta_2 Z_2} \\ -\frac{\gamma_1\beta_2 Z_2 + \gamma_2\beta_1\beta_2 Z_3}{\gamma_1\beta_2 Z_2} & \frac{Z_3+Z_2}{\gamma_1\beta_2 Z_2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.13}$$

where α_i, β_i, and γ_i (i$\rightarrow$1-3) are the non-ideal gains of CFOA and are ideally equal to 1. From equation (2.13), it is noted that the effect of non-ideal gains on the impedance values is insignificant and the expressions approach the ideal expressions when the values of these gains approach 1.

The influences of parasitic resistances and capacitances present at the terminals of CFOAs X and Z have been considered in order to analyze the non-ideal impedance. The complete non-ideal floating immittance simulator circuit of Fig. 2.30 , incorporating the parasitic elements of CFOAs, is depicted in Fig. 2.31. Upon closer examination of Fig. 2.31, it becomes evident that the parasitic capacitances and

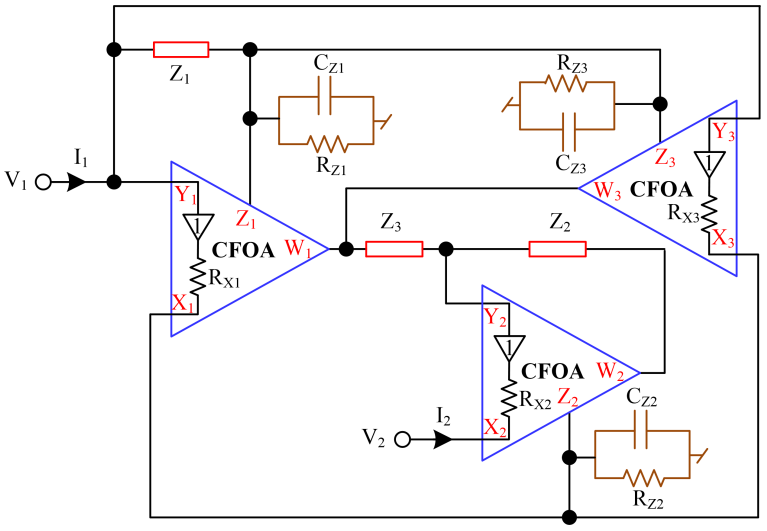


Figure 2.31: Complete proposed immittance simulator circuit with parasitic elements of CFOAs

resistances at the terminals of $CFOA_1$ and $CFOA_3$ can be combined. Reanalysing the circuit depicted in Fig. 2.31 leads to the derivation of the subsequent expression for the non-ideal impedance. Assuming that all the resistors at terminal 'X' are equal ($R_{X1} = R_{X2} = R_{X3} = R_X$), and similarly, all the resistors and capacitors connected to terminal 'Z' are identical ($R_{Z1} = R_{Z2} = R_{Z3} = R_Z$, and $C_{Z1} = C_{Z2} = C_{Z3} = C_Z$), the non-ideal impedance can be formulated as:

$$(\frac{V_1 - V_2}{I_1})' = \left(\frac{Z_1 Z_2}{Z_2 + Z_3}\right)\left[\frac{1 + R_X(sC_Z + \frac{1}{R_Z})(1 + \frac{Z_3}{Z_2} + \frac{R_X}{Z_1}) + \frac{R_X}{Z_1}(1 + \frac{Z_3}{Z_2})}{1 - (sC_Z + \frac{1}{R_Z})(\frac{R_X Z_3}{Z_2 + Z_3})}\right] \tag{2.14}$$

Based on equation (2.14), it is evident that the impedance of the proposed circuit is influenced by the parasitic effects of the CFOAs, especially at lower frequencies. This influence can be alleviated through the appropriate selection of external components (as elaborated in the Simulation section), while considering the parasitic element values of the CFOAs (e.g., $R_X = 50\Omega$, $R_Z = 3\text{M}\Omega$, and $C_Z = 4.5\text{pF}$).

2.4.2 Prominent Application Examples of Proposed Simulator Circuits

The various application examples of the proposed simulator circuits discussed in Section 2.4 are presented here.

2.4.2.1 Lag Compensator

A lag compensator has been designed to demonstrate the usability of the proposed parallel R-L simulator circuit. Fig. 2.32 shows the circuit model of the lag compensator, where the floating R-L simulator is terminated with a resistor. The transfer

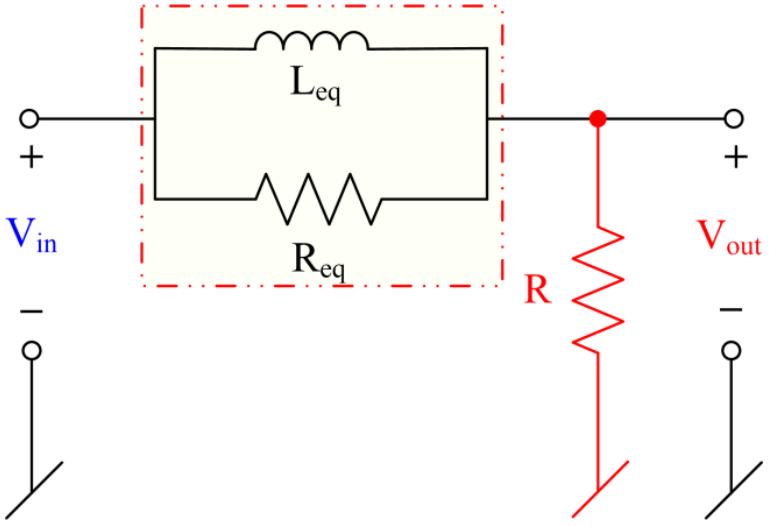


Figure 2.32: Circuit model for the design of lag compensator

function of the circuit shown in Fig. 2.32 can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{\beta}\left(\frac{s+\frac{1}{\tau_1}}{s+\frac{1}{\beta\tau_1}}\right) \tag{2.15}$$

where

$$\tau_1 = \frac{L_{eq}}{R_{eq}} and \beta = \left(1+\frac{R_{eq}}{R}\right) > 1 \tag{2.16}$$

The circuit shown in Fig. 2.32 has been implemented using the proposed parallel R-L circuit simulator as shown in Fig. 2.30.

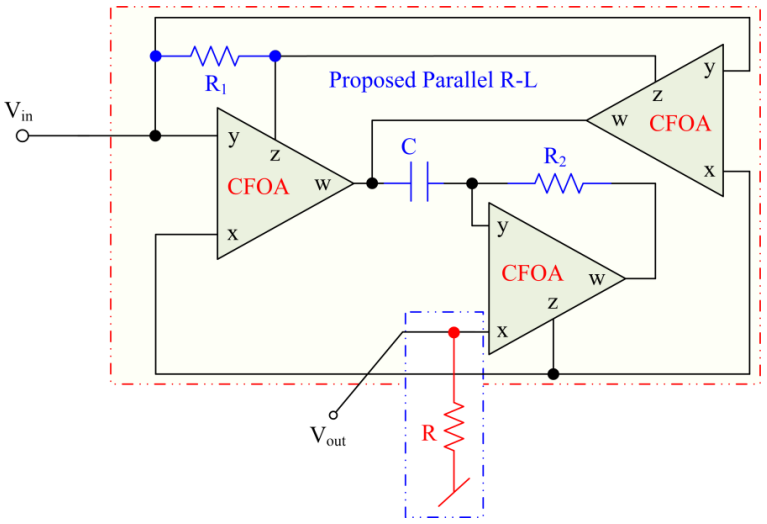


Figure 2.33: CFOA-based lag compensator using proposed floating parallel R-L simulator circuit

The transfer function of lag compensator can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R}{R_1 + R}\left(\frac{s + \frac{1}{CR_2}}{s + \frac{R}{CR_2(R_1+R)}}\right) \tag{2.17}$$

Comparing equations (2.15) and (2.17), the time constant τ_1 and β_1 can be obtained as:

$$\tau_1 = \frac{1}{CR_2} and \beta = \left(1 + \frac{R_1}{R}\right) \tag{2.18}$$

The parameters of lag compensator obtained in (2.18) can be controlled independently using different resistors.

2.4.2.2 Lead Compensator

The prominent application of the proposed floating parallel R-C circuit described in section 2.4 is a lead compensator, and its circuit model is shown in Fig. 2.34. Circuit

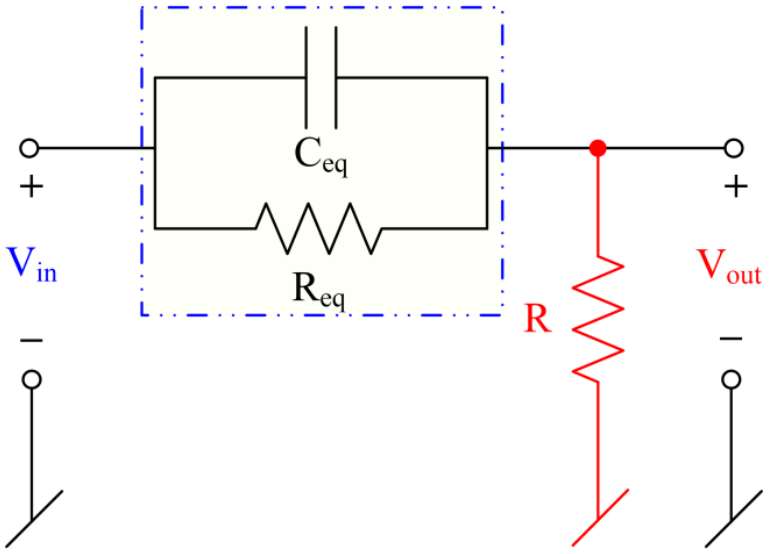


Figure 2.34: Circuit model of the lead compensator using parallel floating R-C simulator circuit

analysis of Fig. 2.34 yields the following transfer function for lead compensator:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{s + \frac{1}{\tau_2}}{s + \frac{1}{\alpha\tau_2}} \right) \tag{2.19}$$

where

$$\tau_2 = \frac{1}{R_{eq}C_{eq}} and \alpha = \left(\frac{R}{R + R_{eq}} \right) < 1 \tag{2.20}$$

The CFOA-based lead compensator using the model shown in Fig. 2.34 is demonstrated in Fig. 2.35.

The analysis of the circuit shown in Fig. 2.35 (assuming ideal CFOAs) yields the following expression:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{s + \frac{1}{CR_2}}{s + \frac{1}{CR_2 \frac{R}{R+R_1}}} \right) \tag{2.21}$$

The values of τ_2 and α of the lead compensator can be obtained by comparing equations (2.19) and (2.21) , as:

$$\tau_2 = \frac{1}{CR_2} and \alpha = \left(\frac{R}{R + R_1} \right) \tag{2.22}$$

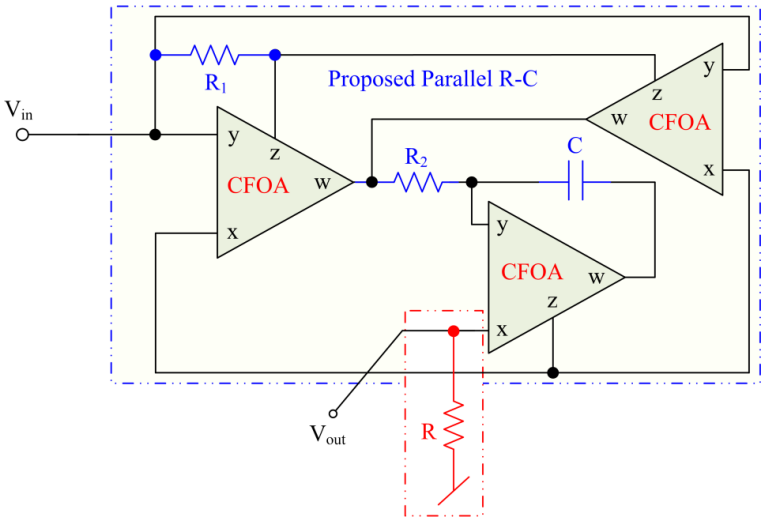


Figure 2.35: Lead compensator using proposed floating parallel R-C simulator circuit

By examining equations (2.21) and (2.22), it can be observed that the zero of the lead compensator is located closer to the origin compared to the pole of the lead compensator.

2.4.2.3 First-Order High-pass Filter

An application example of the lossless FCM circuit as a first order high-pass filter is shown in Fig. 2.36. The transfer function of the high pass filter (HPF) shown in Fig. 2.36 can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{sRC_{eq}}{1+sRC_{eq}}\right) \tag{2.23}$$

The circuit shown in Fig. 2.36 has been implemented using the proposed lossless FCM simulator as shown in Fig. 2.37.

Assuming ideal CFOAs, the transfer function of the circuit of Fig. 2.37 can be

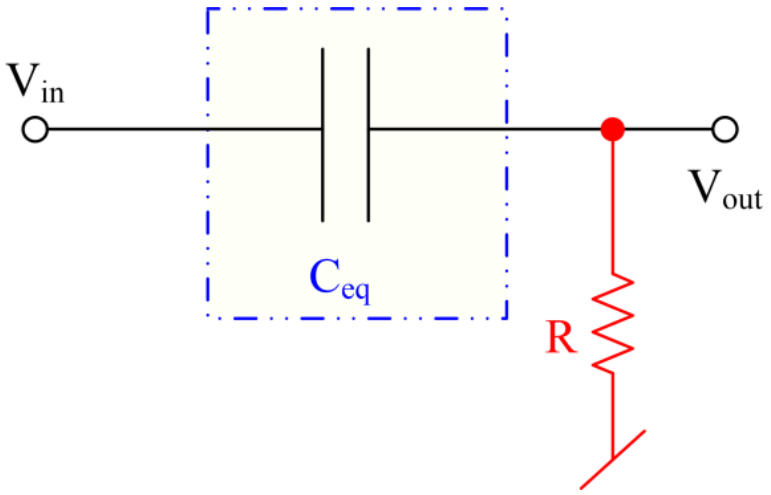


Figure 2.36: Circuit model for the realization of first-order HPF

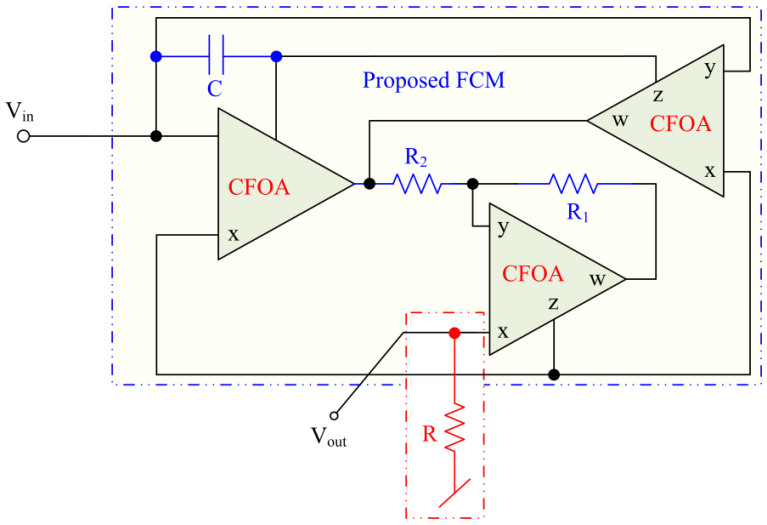


Figure 2.37: First-order high-pass filter circuit as an application example of proposed lossless FCM simulator circuit

written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sRC\left(1+\frac{R_2}{R_1}\right)}{1+SRC\left(1+\frac{R_2}{R_1}\right)} \tag{2.24}$$

From equation (2.24), the cut-off frequency of the HPF can be obtained as:

$$W_{HPF} = R\left(1+\frac{R_2}{R_1}\right)C \tag{2.25}$$

The application examples presented here demonstrate the practical usability of the proposed circuits in both control systems and analog signal processing.

2.4.2.4 Realization of 4th order Butterworth LPF

An application example of the floating parallel RL, parallel RC, and parallel CD circuits as a 4th order Butterworth filter which is based on the normalized passive RLC prototype illustrated in Fig. 2.38 and utilizes transformation T2 [145], [187]. The resulting transformed circuit is depicted in Fig. 2.39. The passive realization of

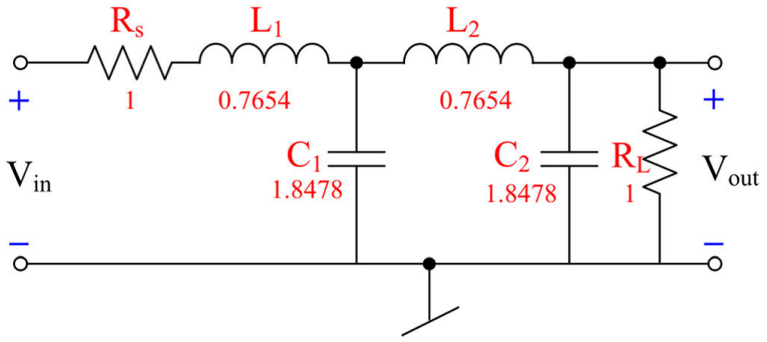


Figure 2.38: Normalized fourth-order Butterworth filter

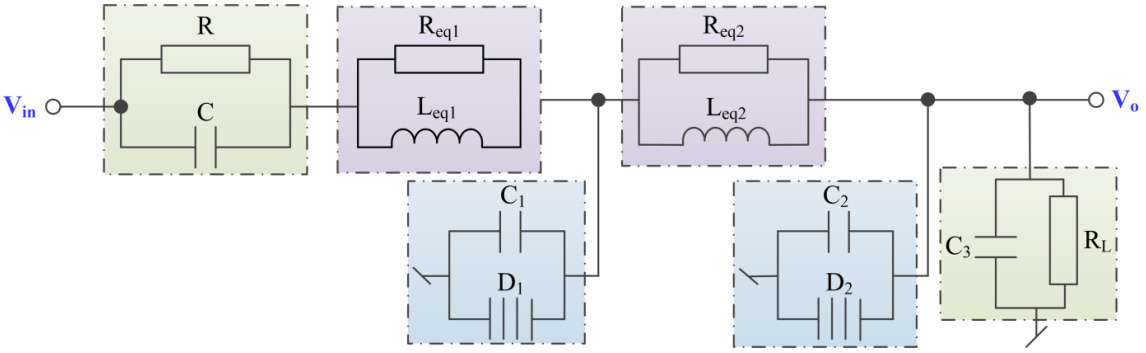


Figure 2.39: Transformation of the passive RLC circuit of 4th order Butterworth Filter shown in Fig. 2.38

the Butterworth circuit shown in Fig. 2.39 has been incorporated with the suggested

parallel RL, parallel RC, and parallel CD configurations, and the complete circuit is illustrated in Fig. 2.40.

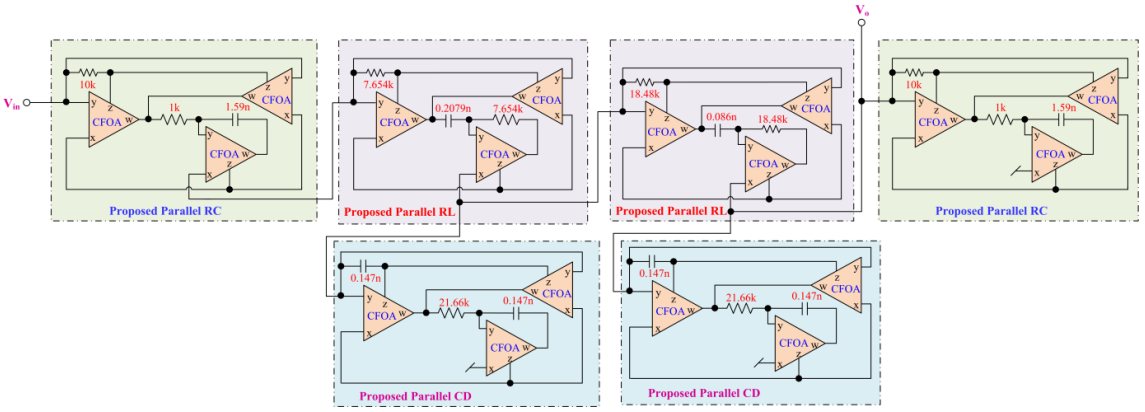
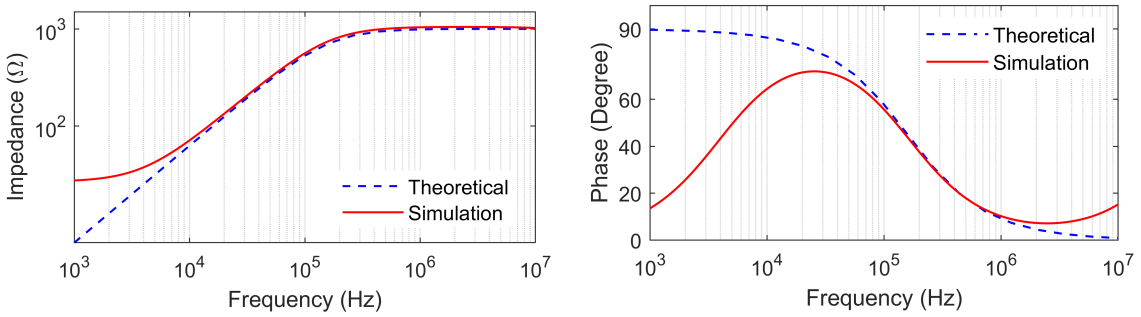


Figure 2.40: 4th order Butterworth LPF circuit using parallel RL, parallel RC and parallel CD circuits [145]

The filter circuit has been designed for a nominal frequency of 100 kHz, and the values of the passive components used are displayed in Fig. 2.40. The frequency responses of the circuit implemented in Fig. 2.40 have been discussed in Simulation results section.

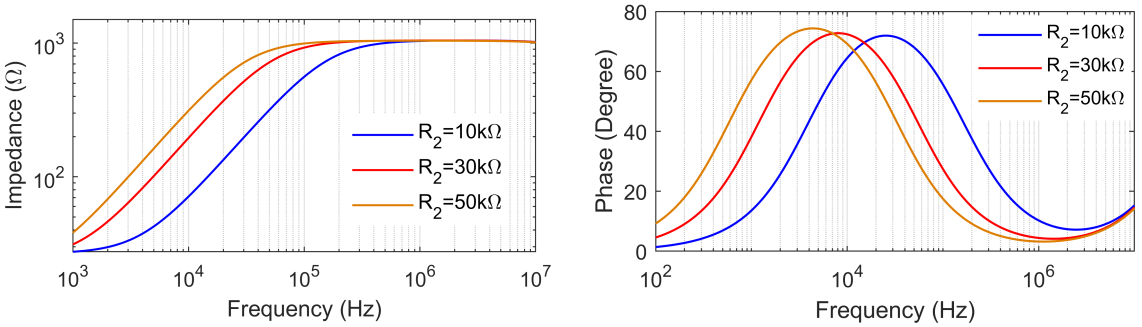
2.4.3 Simulation results

To validate the different functionalities derived from the circuit shown in Fig. 2.30, macro model of AD844-type CFOA is used. For the biasing of CFOA, DC power supply voltages of value ±10V were used. Various simulation results such as frequency responses, transient responses, Monte-Carlo analysis, and temperature analysis are performed for different circuit realizations as discussed in Section 2.4. The simulation results of various functions have been provided in consecutive sections.



(a) (b)

Figure 2.41: Frequency responses of impedance and phase of the circuit of Fig. 2.30



(a) (b)

Figure 2.42: Frequency responses of parallel R-L simulator showing tunability of (a) magnitude (b) phase

2.4.3.1 Results for parallel R-L circuit

To simulate the floating parallel R-L circuit, we used passive components, such as $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, and $C_3 = 100\text{pF}$. Fig. 2.41 demonstrates the simulated frequency responses of the impedance and phase of the simulator, along with theoretical evaluations. The variations in inductance value of the parallel R-L circuit have been displayed in Fig. 2.42 by changing the value of resistor R_2 from 1kΩ to 10kΩ. The transient responses of input voltage and current for a sinusoidal voltage with amplitude of 0.1V and a frequency of 100 kHz are displayed in Fig. 2.43

From Fig. 2.41 and Fig. 2.42, it is evident that the simulated results of floating

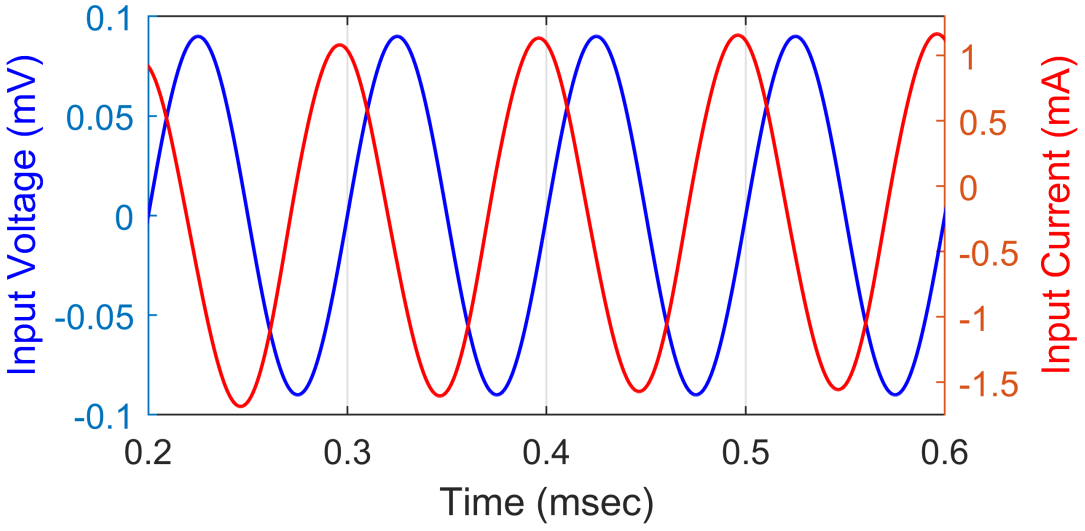
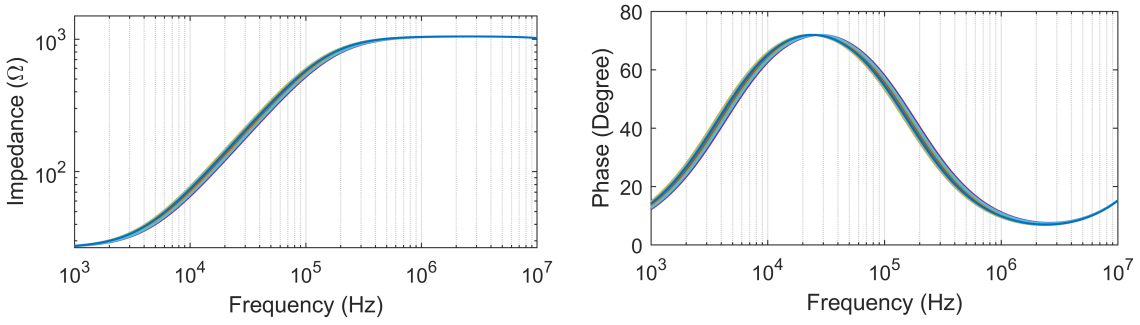


Figure 2.43: Transient responses of input voltage and current for parallel R-L simulator circuit

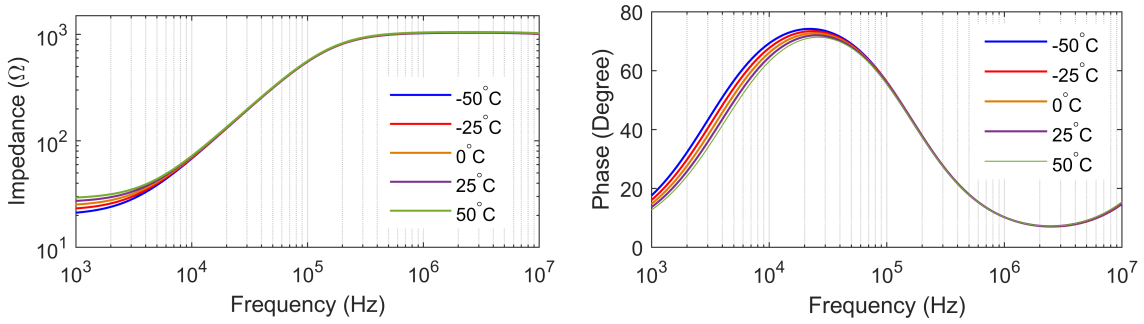


(a) (b)

Figure 2.44: Monte-Carlo results with 5% Gaussian distribution in R deviation (a) magnitude responses (b) Phase responses

parallel R-L circuit are in proper accordance with the theoretical evaluations up to a frequency range of 10kHz – 1MHz. The proposed parallel R-L circuit was also simulated for Monte-Carlo and temperature analyses. In the Monte-Carlo analysis, a 5% tolerance was applied to resistor R_1, and the resulting magnitude and phase results are displayed in Fig. 2.44. For the temperature analysis, the circuit was simulated at temperatures ranging from -50°C to 50°C in increments of 25°C, and the corresponding results are presented in Fig. 2.45.

From Fig. 2.44, the simulated magnitude response of the impedance obtained



(a) (b)

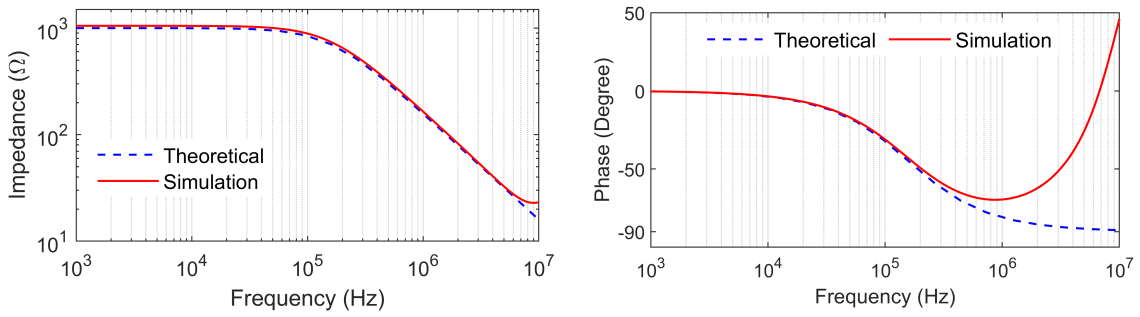
Figure 2.45: Frequency responses of impedance for variation in temperature (a) magnitude (b) phase

from Monte-Carlo simulations shows slight effects in the frequency range of 3kHz to 200kHz. Additionally, from Fig. 2.45, the phase of the impedance exhibits significant temperature variations below 40kHz, whereas the impedance of the parallel R-L circuit demonstrates insignificant changes when temperature changes between -50°C to 50°C.

2.4.3.2 Results for parallel R-C circuit

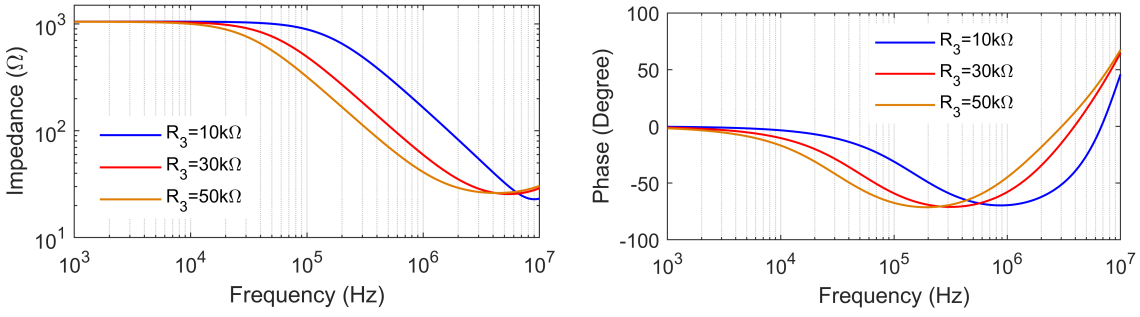
Simulations similar to those conducted for a parallel R-L circuit have been carried out for the proposed floating parallel R-C simulator circuit. The passive component values used in the simulations were $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, and C = 100pF, resulting in R_{eq} and C_{eq} values of 1kΩ and 1.1nF, respectively. A sinusoidal input voltage with a magnitude of 100mV and a frequency of 100kHz was applied to analyze the effect of time-domain analysis. Various simulation results related to the parallel R-C simulator have been shown in Fig. 2.46 to Fig. 2.50.

From Fig. 2.46, it can be observed that the simulated magnitude and phase responses of the parallel R-C circuit match well with the theoretical evaluations over a wide range of frequencies. Specifically, the impedance magnitude matches the theoretical values within the frequency range of 1kHz to 6MHz, while the phase matches



(a) (b)

Figure 2.46: Frequency responses of impedance for parallel R-C simulator circuit (a) Magnitude and (b) phase



(a) (b)

Figure 2.47: Frequency responses showing tunability in (a) magnitude and (b) phase

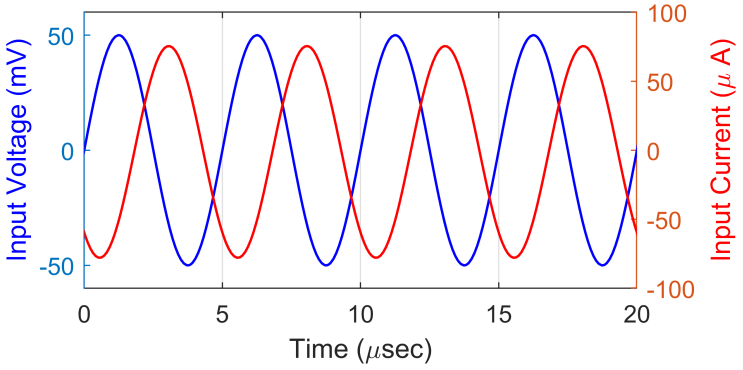
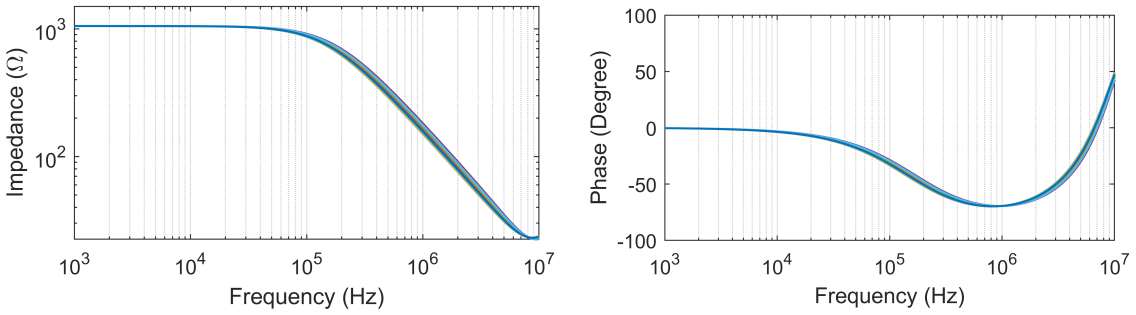


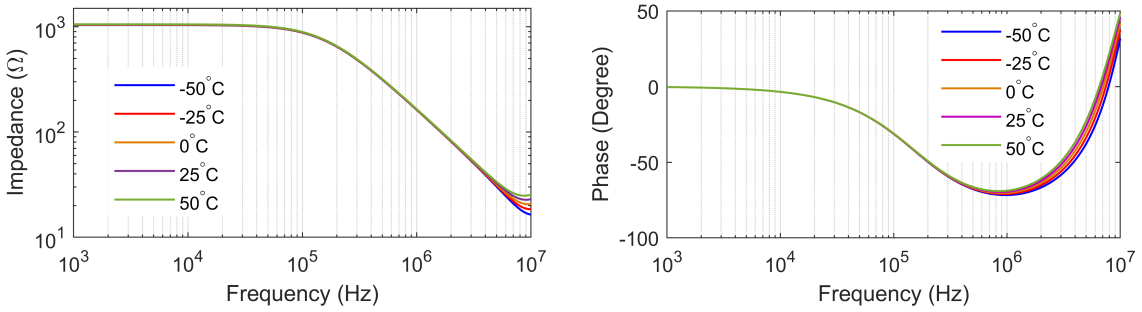
Figure 2.48: Input voltage and current of the impedance of parallel R-C simulator circuit

between 1kHz to 300kHz. It can be observed from the simulated results presented in Fig. 2.49 that the magnitude and phase of the impedance of the parallel R-C simulator circuit are not significantly affected over a wide frequency range within



(a) (b)

Figure 2.49: Monte-Carlo results of (a) magnitude (b) phase with 10% deviations in resistor



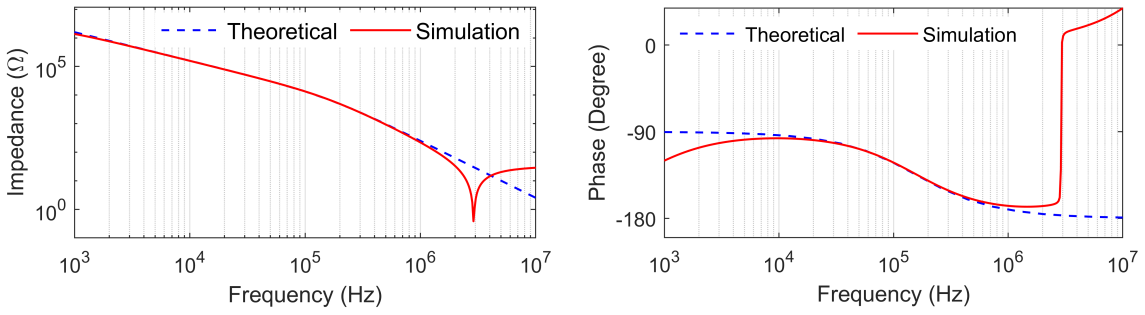
(a) (b)

Figure 2.50: Magnitude and phase responses of parallel R-C circuit for different temperature (a) magnitude (b) phase

the tolerance provided for resistor R_2. Furthermore, the temperature analysis results suggest that the proposed parallel R-C circuit simulator is less sensitive to changes in temperature.

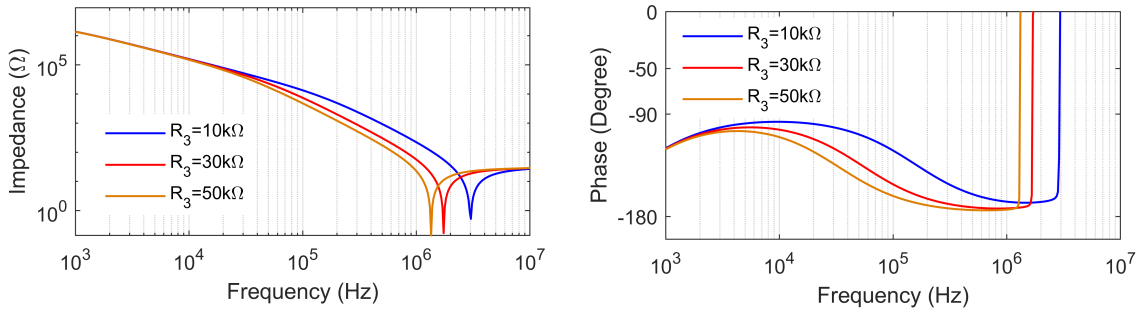
2.4.3.3 Results for parallel C-D configuration

To validate the functionality of the proposed parallel C-D simulator circuit, the frequency responses of magnitude and phase of impedance, variations in magnitude and phase of impedance for different values of R_3, and transient responses of input voltage and current are presented. For the simulation purpose, the values of passive components were used as: $C_1 = 100\text{pF}$, $C_2 = 100\text{pF}$, and $R_3 = 10\text{k}\Omega$. To show



(a) (b)

Figure 2.51: Frequency responses of (a) magnitude and (b) phase of parallel C-D circuit



(a) (b)

Figure 2.52: Frequency responses of impedance of parallel C-D simulator (a) magnitude and (b) phase

the transient responses of input voltage and current, a sinusoidal input voltage of magnitude of 50mV at a frequency of 200kHz was applied. The corresponding results are displayed in Fig. 2.51 – Fig. 2.53.

Monte-Carlo and temperature analyses have also been carried out and the corresponding results are shown in Fig. 2.54 and Fig. 2.55 respectively.

Fig. 2.54 and Fig. 2.55 show that the proposed parallel C-D simulator has insignificant deviations, even when a 10% Gaussian deviation is applied to resistor R_3, and when there are changes in temperature from -50°C to 50°C. From the results shown in Fig. 2.51 – Fig. 2.55, it is observed that the simulation results obtained for parallel C-D simulator circuit match with the theoretical evaluations.

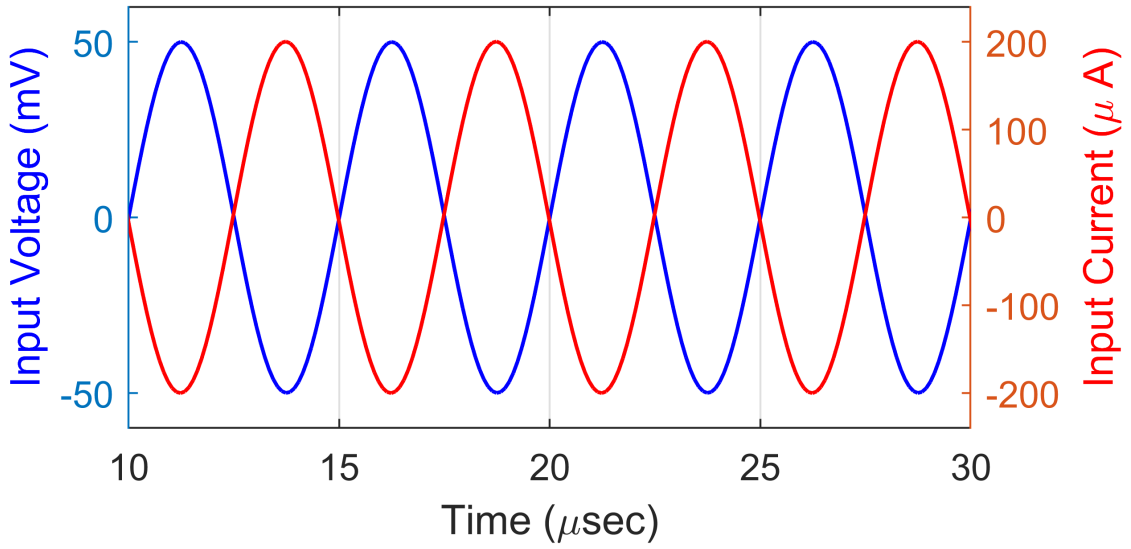
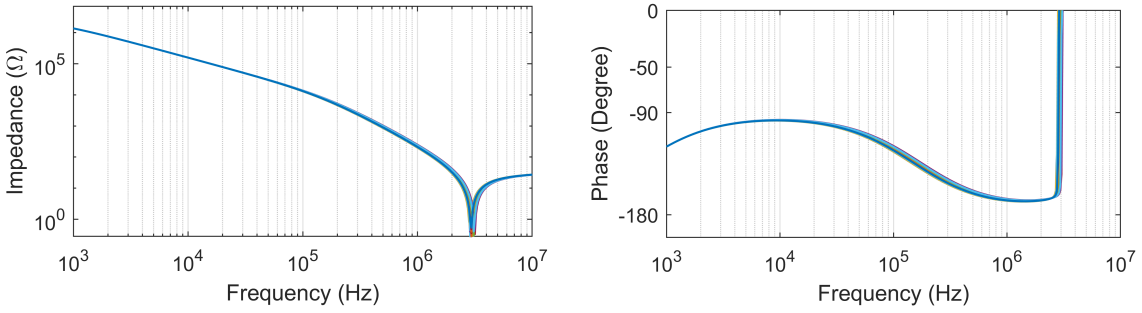


Figure 2.53: Transient responses of input voltage and current of parallel C-D simulator circuit

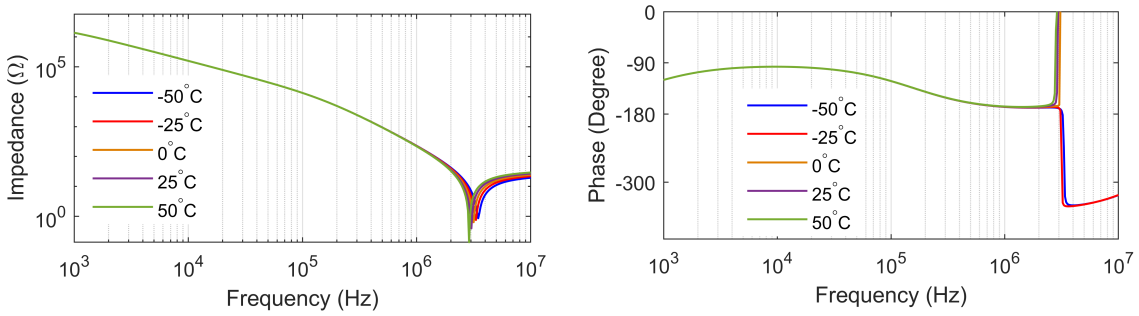


(a) (b)

Figure 2.54: Monte-Carlo simulations results for 10% Gaussian deviation in resistor R_3

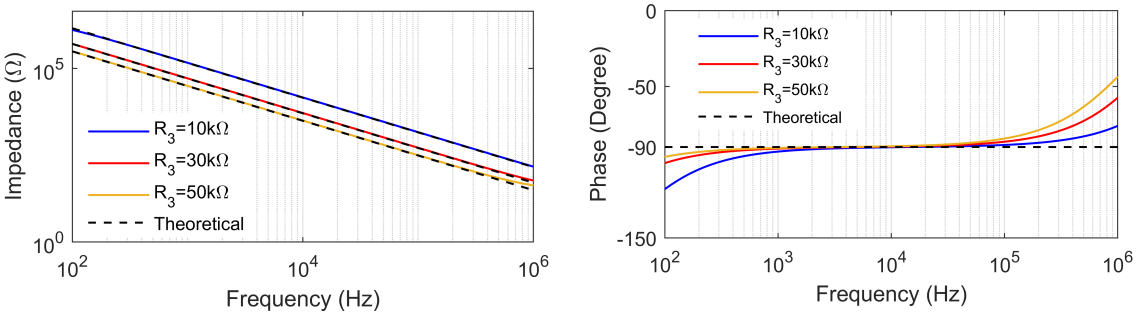
2.4.3.4 Results for floating capacitance multiplier circuit

Frequency analyses of the proposed floating lossless capacitance multiplier circuit derived from Fig. 2.30 have been demonstrated by selecting passive component values as: $C_1 = 100$pF and $R_2 = 1$kΩ and R_3 =10kΩ, 30kΩ and 50kΩ. The respective magnitude and phase responses of impedance of FCM have been shown in Fig. 2.56. Equivalent capacitance for different values of resistance for the lossless FCM circuit has been carried out and the results have been displayed in Fig. 2.57(a) for which



(a) (b)

Figure 2.55: Frequency responses of impedance of parallel C-D simulator showing variation in temperature (a) magnitude and (b) phase

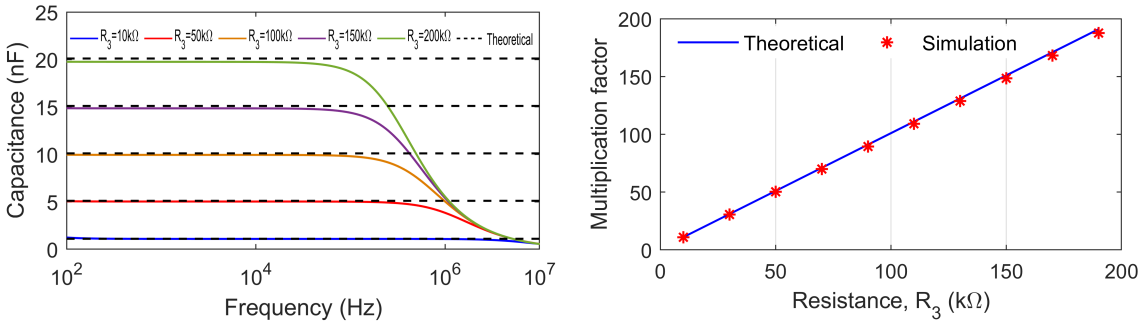


(a) (b)

Figure 2.56: Frequency responses of the proposed floating capacitance multiplier (a) magnitude and (b) phase

resistor R_3 has been varied with the values 10kΩ, 50kΩ, 100kΩ, 150kΩ, 200kΩ R_2 = 1 kΩ and C = 100pF resulting in C_{eq} as 1.1nF, 5.1nF, 10.1nF 15.1nF and 20nF respectively. We have also shown the multiplication factors of the capacitor with their corresponding theoretical values as displayed in Fig. 2.57(b) for which resistor R_3 was varied during simulations from 10kΩ to 200kΩ.

From Fig. 2.57(b), it is seen that the variation in multiplication factor of lossless FCM with the variation of resistor R_3 are in good agreement with their corresponding theoretical values with maximum percentage error of 1.5%. Time-domain analysis has been performed for the proposed FCM circuit for which a sinusoidal input voltage of magnitude 50mV at 10 kHz has been applied. The simulated transient



(a) (b)

Figure 2.57: (a) Variations in capacitance with frequency by varying resistor R_3 of Fig. 2.30 (b) Variation of multiplication factor for different values of tuning resistor R_3

responses of input voltage and input current of the proposed lossless FCM have been shown in Fig. 2.58. Monte-Carlo simulations have been performed for the FCM with

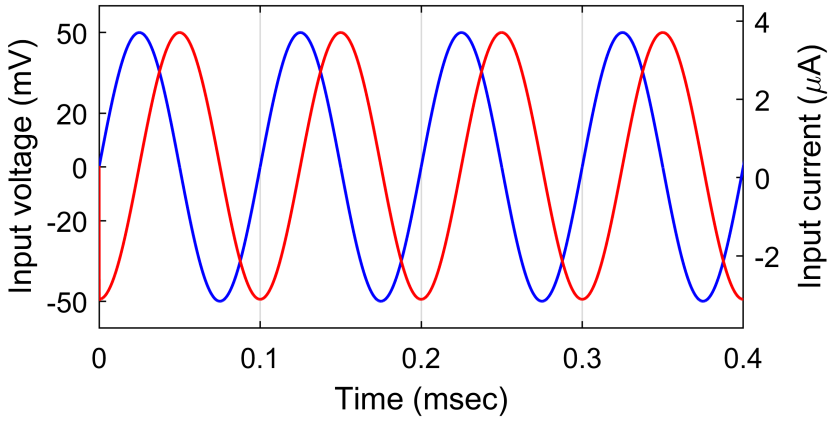


Figure 2.58: Time responses of input voltage and current of FCM

100 runs. The results have been shown in Fig. 2.59 in which the passive component values deviate uniformly with 10%. The robustness of the simulated capacitance has also been tested using Monte-Carlo simulations for which the circuits were run for 100 samples with 10% tolerance in resistors and capacitor. The corresponding Monte-Carlo results for the variation in maximum capacitance due to these tolerances have been displayed in Fig. 2.60. In Fig. 2.60(a-c), the changes in maximum capacitance due to variations in R_2, R_3 and C have been demonstrated in which the maximum and minimum capacitance values have been provided for the theoretical

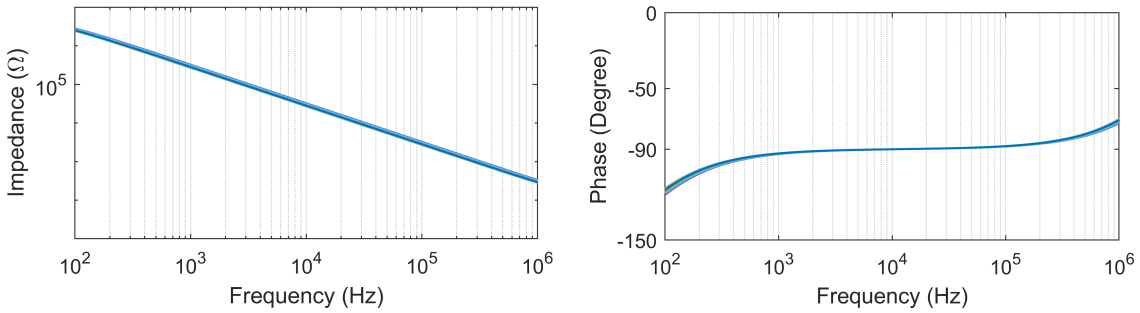


Figure 2.59: Monte-Carlo simulation results of the proposed FCM (a) magnitude (b) phase

value of 1.1nF by selecting resistors (R_3=10kΩ and R_2 = 1 kΩ) and capacitor C_1 = 100pF. The proposed circuit was also simulated at different temperatures for testing the performance of the robustness and validated by varying the temperature from -50°C to 100°C. The frequency responses of the impedance and phase for different temperatures of the lossless FCM circuit have been displayed in Fig. 2.61(a) and 2.61(b) respectively.

The application example of FCM as a first order high pass filter has also been simulated for a nominal frequency of 159kHz and the corresponding frequency responses are demonstrated in Fig. 2.62. The variation of Total Harmonic Distortion (THD) with respect to input voltages has also been conducted for both the FCM circuit and the first-order HPF using the PSPICE simulation tool. The corresponding results are shown in Fig. 2.63. The input voltage has been ranged from 10mV to 100mV for both circuits, operating at a frequency of 100kHz.

To validate the performance of the 4th order Butterworth filter illustrated in Fig. 2.40, the circuit is configured for a nominal frequency of 100 kHz. The simulated frequency responses are presented in Fig. 2.64. The frequency obtained through simulations is approximately 93 kHz, which closely aligns with the theoretical value. From the above simulation results shown in Fig. 2.41 – Fig. 2.64, it is seen that the

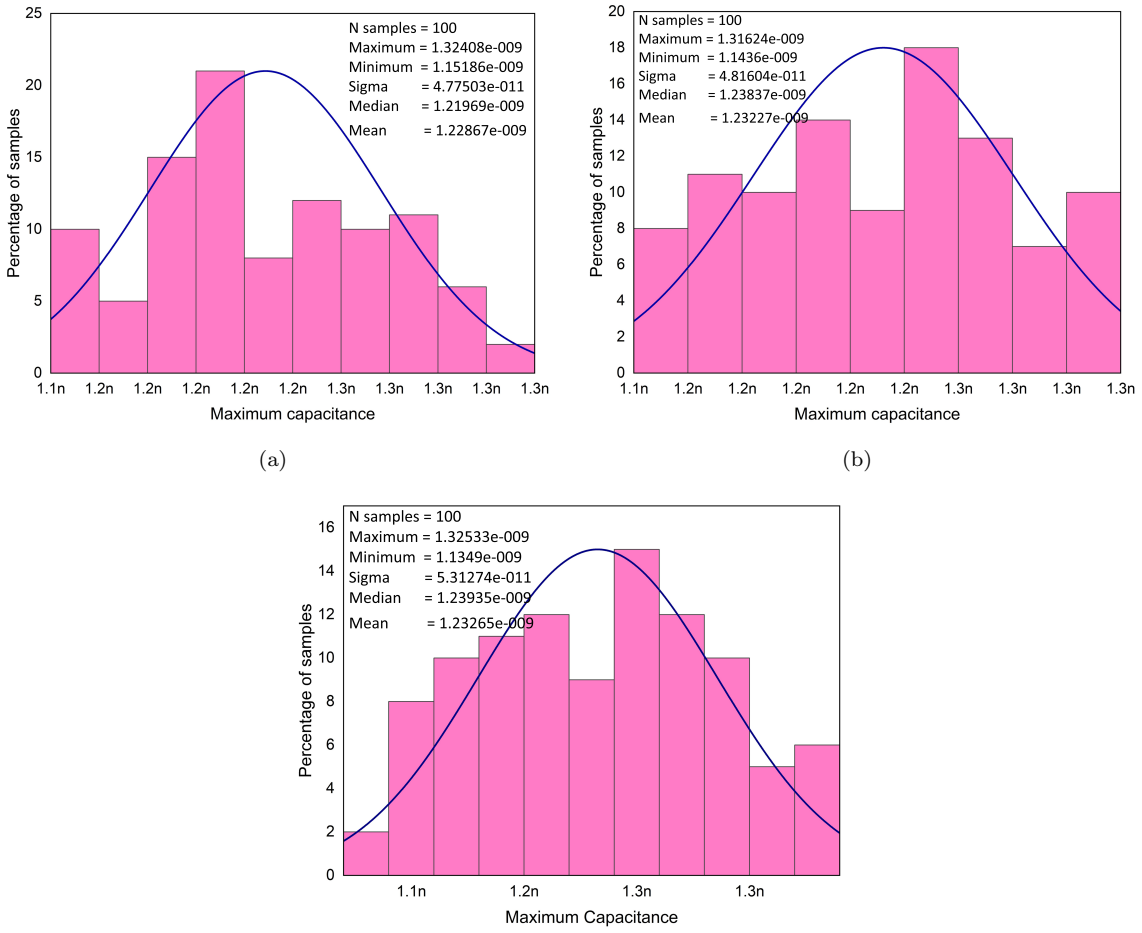


Figure 2.60: Histograms obtained through Monte-Carlo simulations for circuit of Fig. 2.30

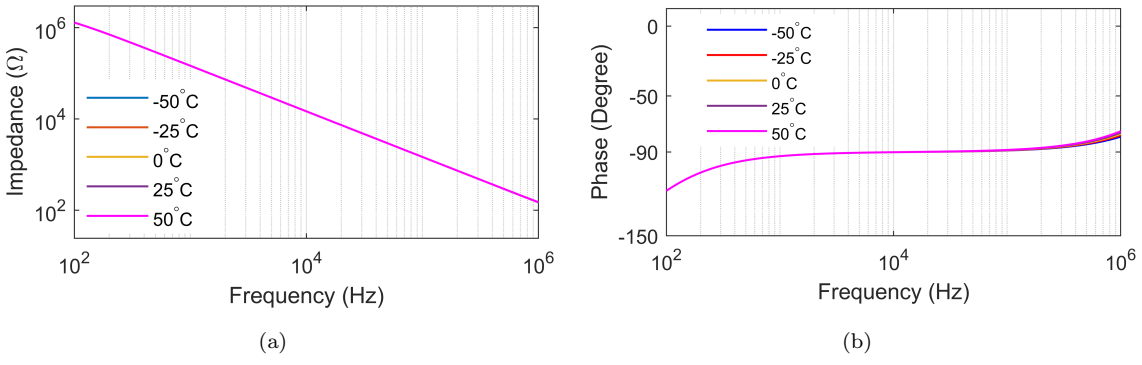


Figure 2.61: Frequency responses of (a) impedance and (b) phase of FCM at different temperatures

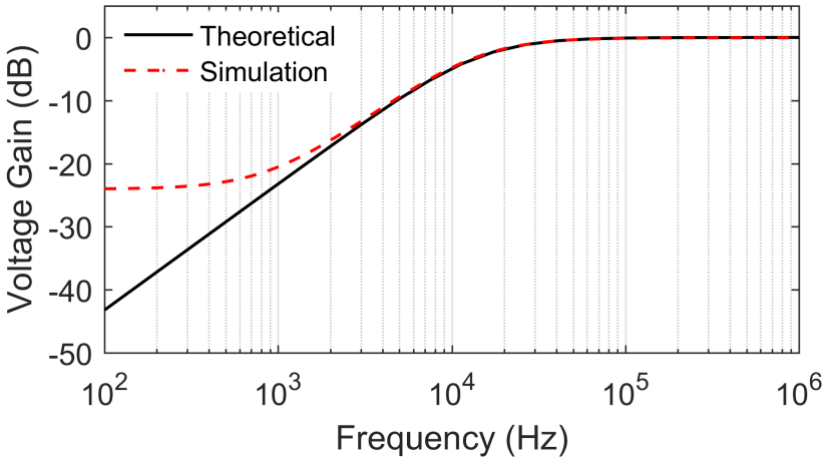


Figure 2.62: Frequency responses of first order HPF circuit

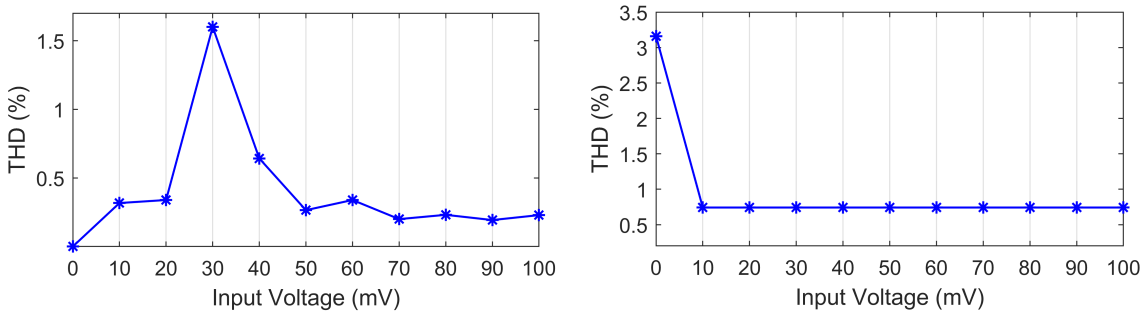


Figure 2.63: THD variation with respect to input voltages of the (a) FCM and (b) HPF

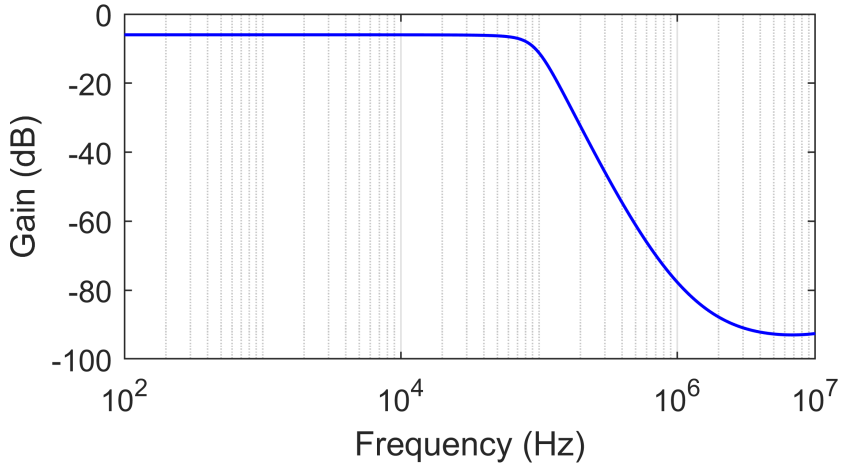


Figure 2.64: Frequency responses of 4th order Butterworth filter shown in Fig. 2.40

proposed floating immittance simulator circuits work properly and the results also match with the theoretical evaluations.

2.4.4 Experimental Results

The functions derived from the proposed circuit depicted in Fig. 2.30 were subjected to experimental testing. This experimentation involved the use of commercially available off-the-shelf IC AD844 type CFOAs, 5% tolerance resistors, and 10% tolerance capacitors. In order to conduct these tests across all circuits, a voltage-to-current converter [188] was employed to drive the circuits. Subsequently, the input impedance and phase measurements were obtained from port 1 with port 2 grounded, and vice-versa. To conserve space, we have herein presented the experimental findings alongside simulation results and theoretical assessments performed using a parallel RL simulator. For this purpose, passive components were chosen with values used in the simulations. The experimental input impedance and phase characteristics observed at both port 1 and port 2 are graphically depicted in Fig. 2.65. We have also experimentally tested the proposed lossless FCM circuit as an integrator using the test circuit shown in Fig. 2.66 using commercially available IC AD844 type CFOA. The experimental set-up of the FCM has been demonstrated in Fig. 2.67 and the corresponding experimental transient results are shown in Fig. 2.68.

From Fig. 2.68, it is observed that the voltage across capacitor (V_O) is approximately 90° apart with the applied voltage (V_m) that validates the performance of integrator circuit.

The proposed circuit has also been experimentally verified by providing experimental results of the applications of the different functions obtained from the circuit of Fig.

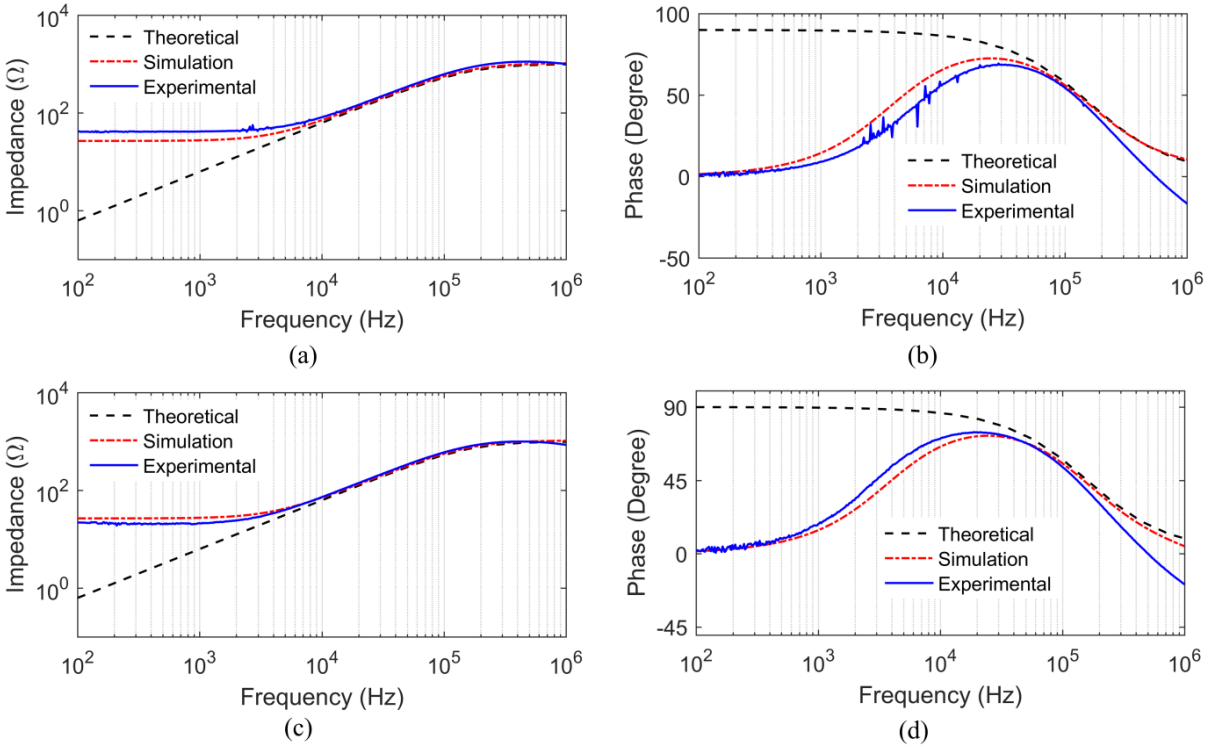


Figure 2.65: Frequency response of input impedance and phase seen from (a-b) port 1 (c-d) port 2

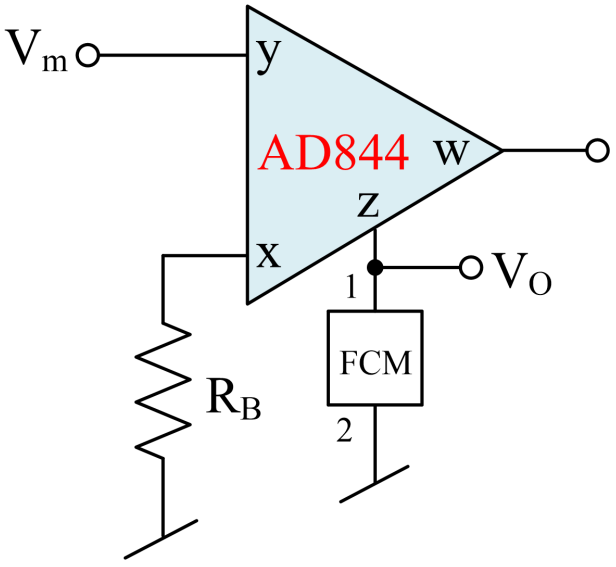


Figure 2.66: Experimental test circuit for the FCM

2.30. The commercially available ICs AD844 with 5% tolerance in resistors and 10% tolerance in capacitors were used. The power supply voltages used for the biasing of AD844s were selected as ±15V. For all the application examples, the sinusoidal

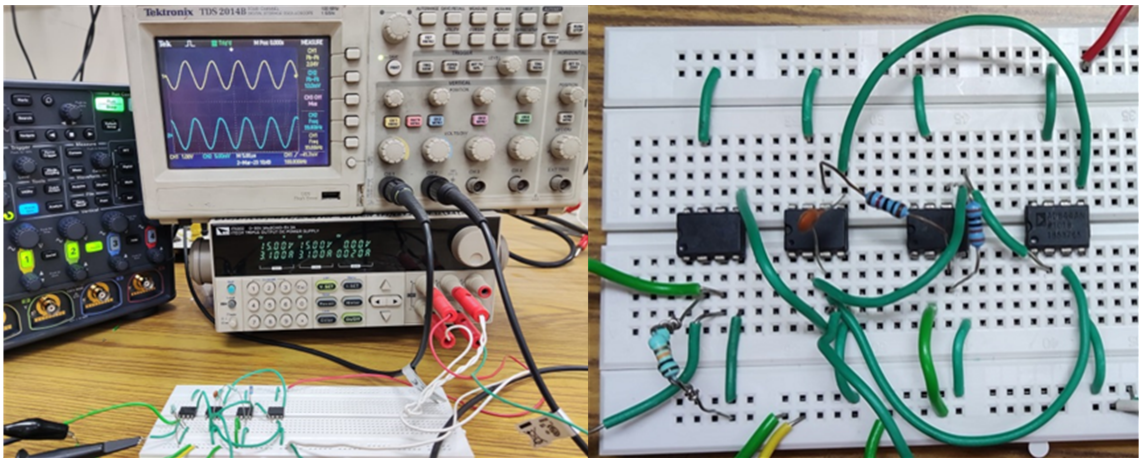


Figure 2.67: Experimental test circuit for the FCM

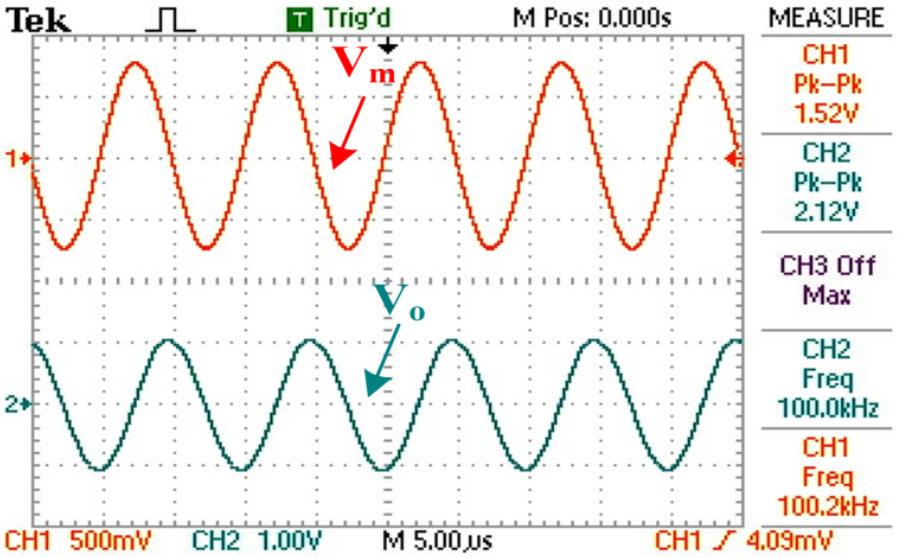


Figure 2.68: The input and output voltages of the test circuit shown in Fig. 2.66

input voltage signal with 4V peak-peak was applied.

2.4.4.1 Lag compensator

To verify the performance of application example of parallel R-L circuit experimentally as lag compensator (Fig. 2.33), the following values of passive components were used: $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, R = 10kΩ and C = 100pF. The experimental

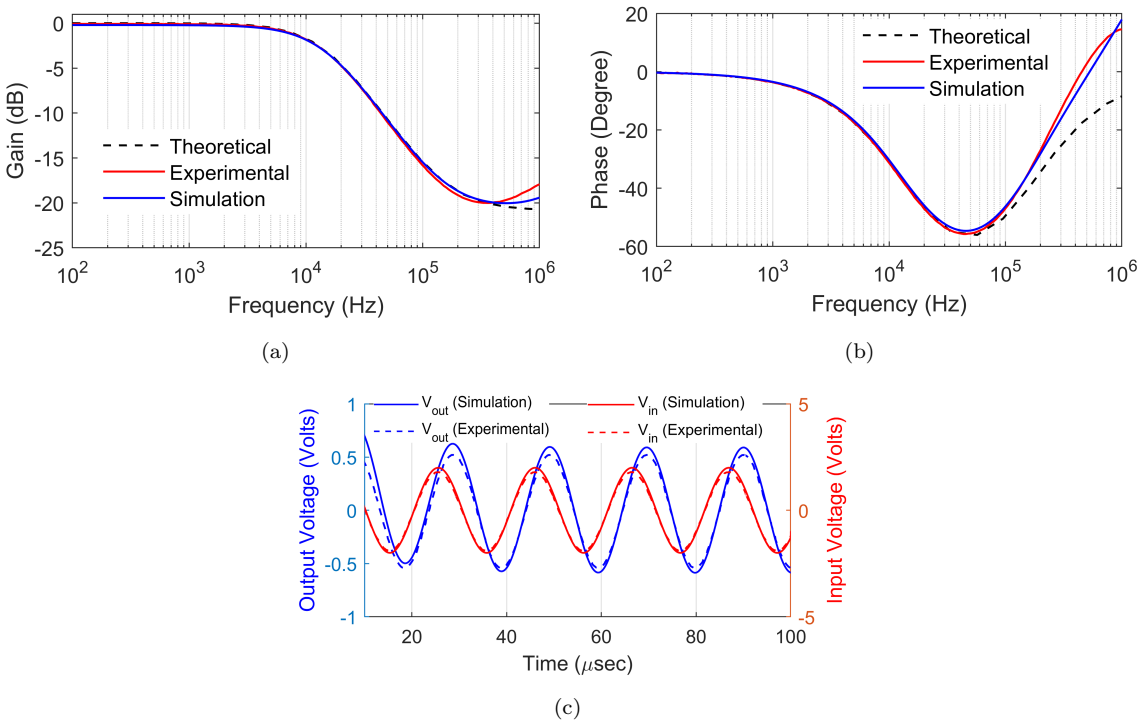


Figure 2.69: (a and b) Frequency responses of magnitude and phase (c) Input and output voltages of lag compensator

frequency responses of magnitude and phase of lag compensator along with simulated results and theoretical evaluations are shown in Fig. 2.69(a) and Fig. 2.69(b) respectively, whereas Fig. 2.69(c) shows the transient input and output voltages of the lag compensator.

From Fig. 2.69(b), it is observed that the maximum phase lag of the compensator is 56° at 42.6kHz and it can also be verified by the transient responses of input and output voltage where output voltage is lagging with the input voltage.

2.4.4.2 Lead compensator

To test the workability of lead compensator shown in Fig. 2.35 experimentally, the passive components used were $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, R = 10kΩ and C = 100pF. The frequency responses of magnitude and phase of the lead compensator are displayed

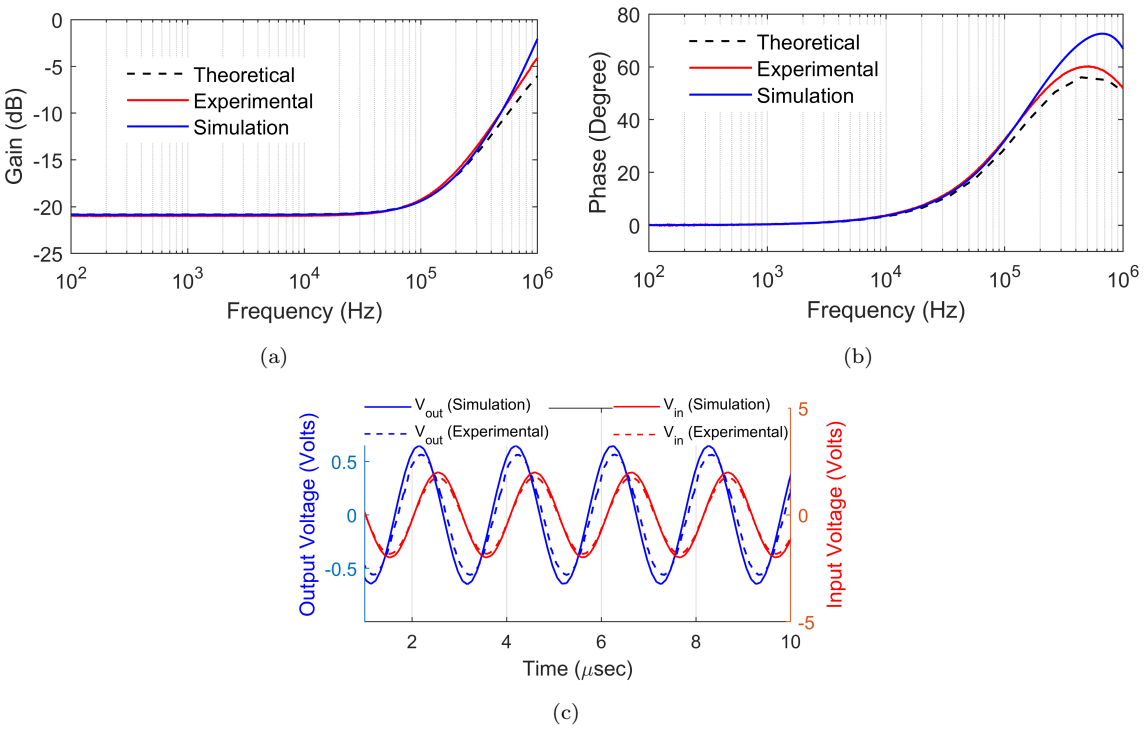


Figure 2.70: (a and b) Frequency responses of magnitude and phase (c) Input and output voltages of lead compensator

in Fig. 2.70 (a-b). The time-domain responses of input and output voltages of the lead compensator at the maximum phase lead are shown in Fig. 2.70 (c) for which an input sinusoidal signal of amplitude 4V peak to peak at a frequency 490kHz was applied.

From Fig. 2.70 (b), it is observed that the maximum phase for the lead compensator is 59.24 ° at a frequency of 489.8kHz. Fig. 2.70 (c) shows that the output voltage is leading with the input voltage which validates the functionality of the lead compensator.

2.4.4.3 First-order high pass filter

To verify the performance of first-order high-pass filter shown in Fig. 2.37, the filter circuit was bread boarded for a nominal frequency of 159kHz using following

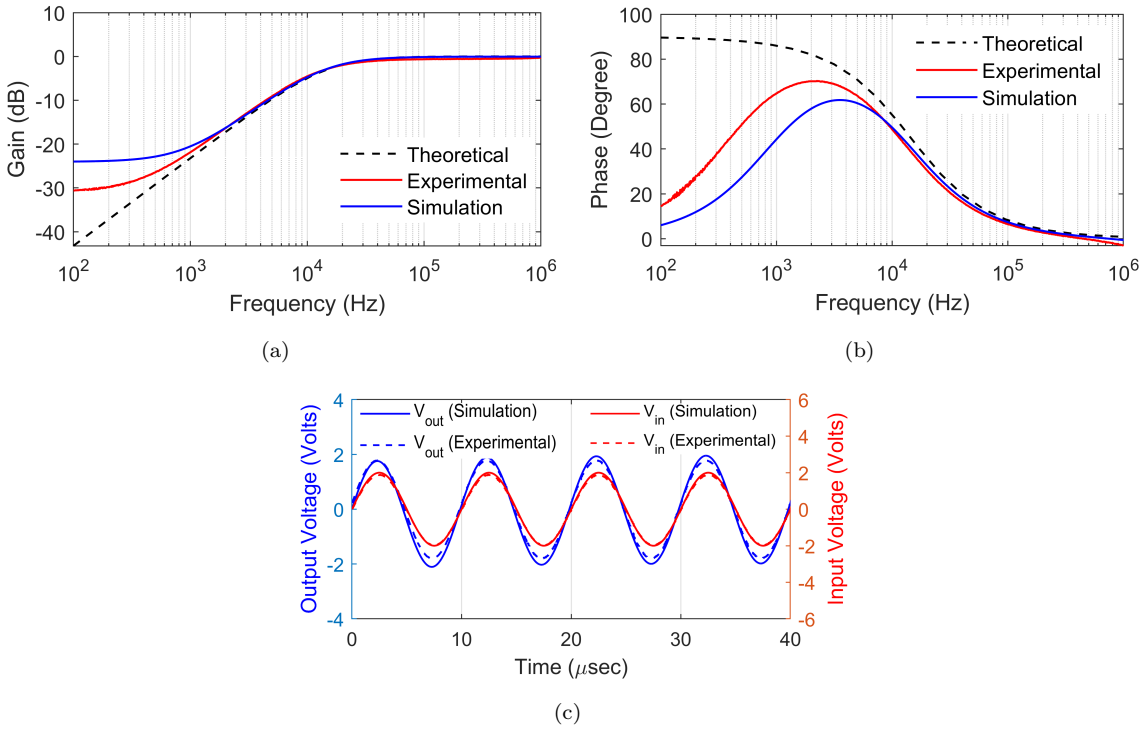


Figure 2.71: (a and b) Experimental frequency responses and (c) transient responses of first-order high-pass filter

passive component values: $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, R = 10kΩ, and C = 100pF. Fig. 2.71 shows the experimental frequency responses of magnitude and phase along with simulation results and theoretical evaluations, as well as the input and output transient voltages.

2.5 Floating lossless immittance simulator

A simple artifice in the circuit presented in Fig. 2.30 allows the same circuit to function as a floating lossless immittance simulator whose circuit (Fig. 2.72) description and function realizations are discussed below. A routine analysis of the circuit of Fig. 2.72, using the voltage-current relationships of CFOA, yields the following matrix

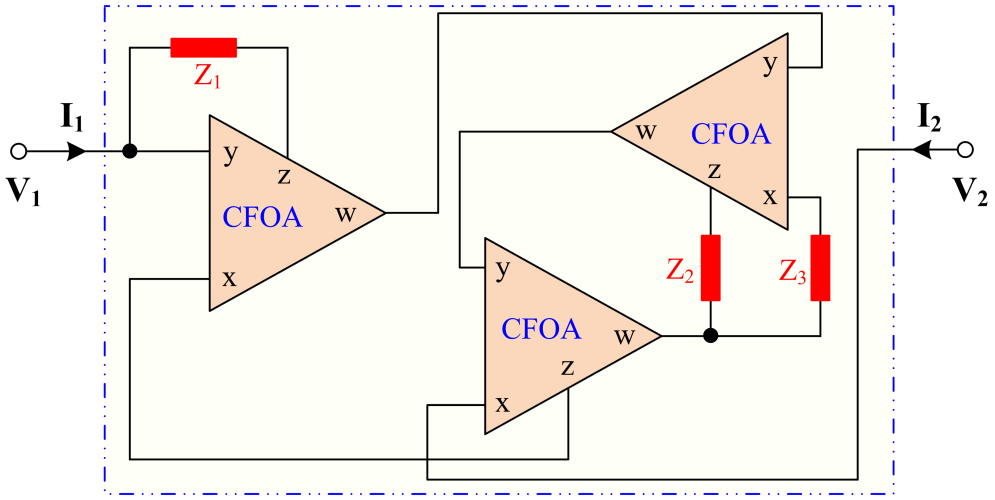


Figure 2.72: Modified floating lossless immittance simulator circuit

equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{Z_3}{Z_1 Z_2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = Y_{in} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.26}$$

where

$$Y_{in} = \frac{Z_3}{Z_1 Z_2} \tag{2.27}$$

Proper choice(s) of impedances Z_1, Z_2 and Z_3 of Fig. 2.72 obtained in equation (2.26) yield different types of immittance simulator circuits i.e., lossless floating inductance simulator, lossless floating capacitance multiplier and floating FDNR. The realizations of these circuits are described here.

Case I: $Z_1 = R_1$, $Z_2 = R_2$, and $Z_3 = 1/\mathrm{s}C_3$. The matrix equation that describes the floating inductance simulator is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sR_1R_2C_3} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.28}$$

Case II: $Z_1 = 1/\mathrm{s}C_1$, $Z_2 = R_2$ and $Z_3 = R_3$, then the circuit of Fig. 2.72 yields a floating capacitance multiplier whose matrix equation can be obtained as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{sC_1R_3}{R_2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.29}$$

Case III: If we select $Z_1 = R_1$, $Z_2 = 1/\mathrm{s}C_2$, and $Z_3 = R_3$, the circuit depicted in Fig. 2.72 will simulate a floating capacitance multiplier, and its matrix equation can be expressed as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{sC_2R_3}{R_1} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.30}$$

Case IV: A floating FDNR can be simulated with $Z_1 = 1/\mathrm{s}C_1$, $Z_2 = 1/\mathrm{s}C_2$, and $Z_3 = R_3$.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = s^2C_1C_2R_3 \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.31}$$

From equations (2.28) $-$ (2.31), it can be noticed that the circuit depicted in Fig. 2.72 is capable of realizing floating lossless inductor, floating capacitor, and floating FDNR circuits. A noteworthy feature of these circuits is their independent tunability, which can be achieved through resistor(s).

2.5.1 Simulation results

To verify the various functionalities derived from the circuit depicted in Fig. 2.72, a macro model of the AD844-type CFOA was utilized. The CFOA was biased using DC power supply voltages of $\pm$10V. Different simulation results, including frequency

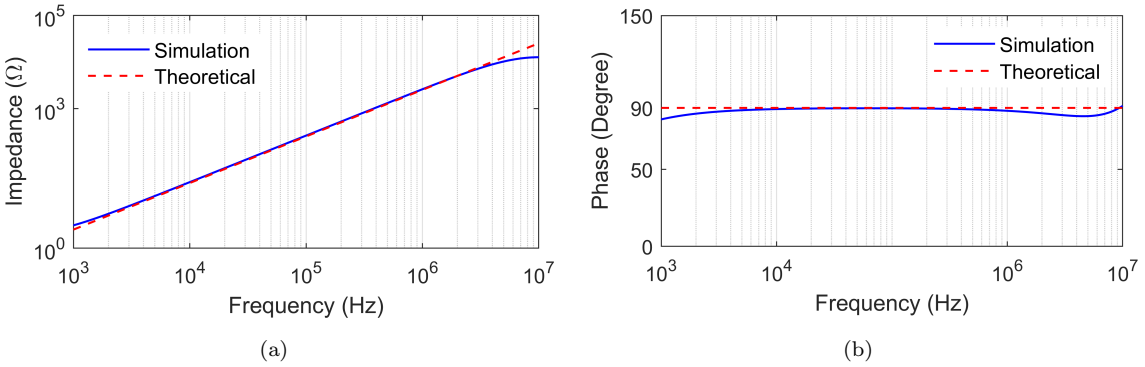


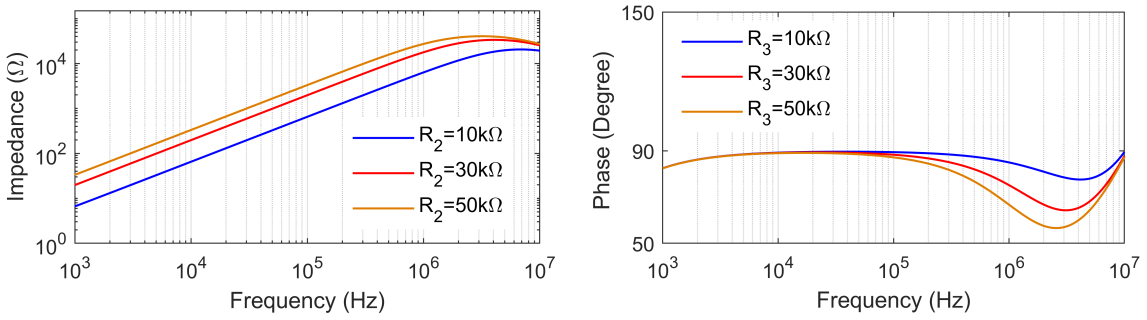
Figure 2.73: Frequency responses of (a) impedance and (b) phase of proposed lossless floating inductor of Fig. 2.72

responses, transient responses, Monte Carlo analysis, and temperature analysis, were conducted for various circuit realizations as discussed above. The simulation results for these various functions are presented in the following sections.

2.5.1.1 Results for floating inductance simulator

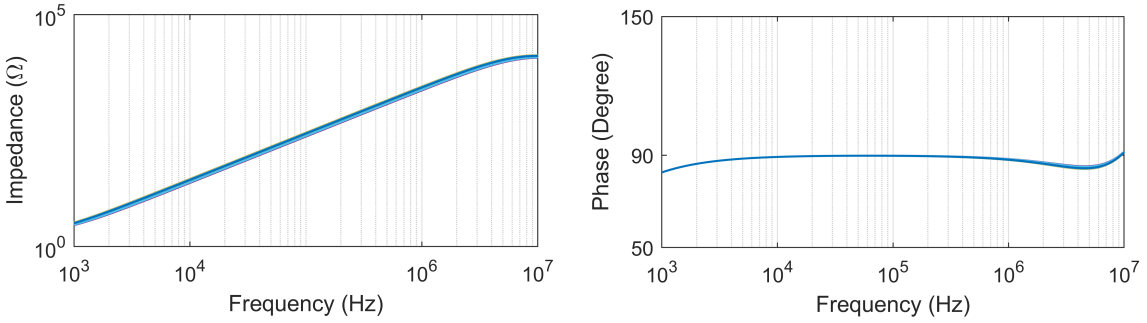
To simulate the floating inductance simulator,passive components were used, such as $R_1 = 1\text{k}\Omega$, $R_2 = 4\text{k}\Omega$, and $C_3 = 100\text{pF}$ provides L_{eq}=400uH. Fig. 2.73 illustrates the simulated frequency responses of the impedance and phase of the simulator, along with theoretical evaluations. The variations in inductance value of floating inductor simulator have been displayed in Fig. 2.74 by changing the value of resistor R_2 (10kΩ, 30kΩ, 50kΩ). Figures 2.73 and 2.74 show that the simulated results of the floating inductor simulator align well with theoretical evaluations within the frequency range of 1kHz to 5MHz. The proposed inductor simulator was also simulated for Monte-Carlo analysis. In the Monte-Carlo analysis, a 5% tolerance was applied to resistor R_1, and the resulting magnitude and phase results are displayed in Fig. 2.75.

From Fig. 2.75, the simulated magnitude response of the impedance obtained from Monte-Carlo simulations shows slight effects in the frequency range of 1kHz to



(a) (b)

Figure 2.74: Frequency responses of floating inductor simulator showing tunability of (a) magnitude (b) phase



(a) (b)

Figure 2.75: Monte-Carlo results with 5% Gaussian distribution in R deviation (a) magnitude responses (b) Phase responses

10MHz. An application in Fig. 2.76 demonstrates the effectiveness of the floating inductor, providing both the outputs of a voltage mode(VM) notch filter (NF) and a low-pass filter (LPF). Transfer function of the NF and LPF are demonstrated

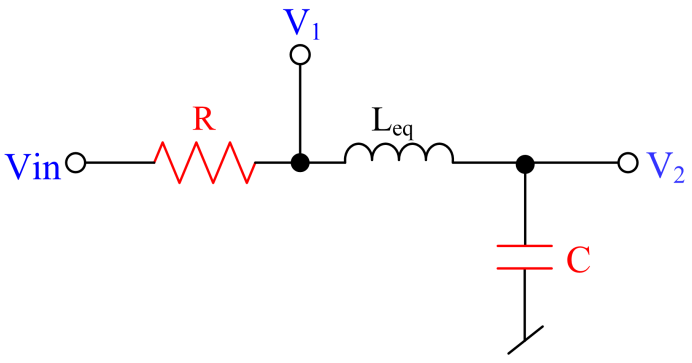
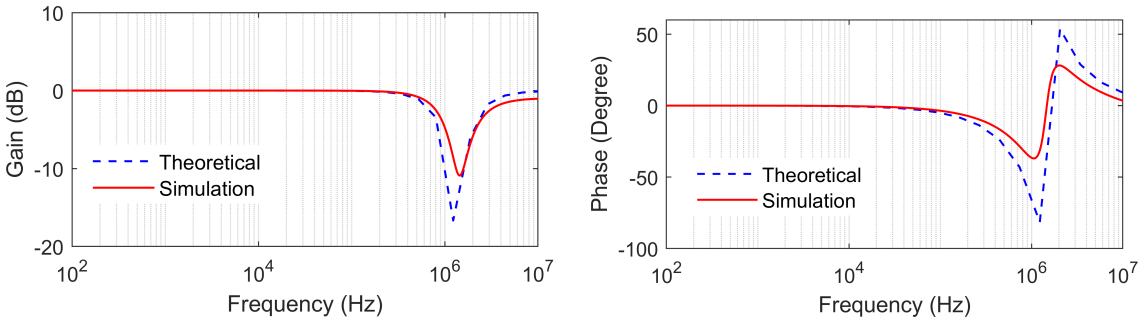


Figure 2.76: NF and LPF as an application example of floating inductor simulator



(a) (b)

Figure 2.77: Frequency responses of NF (a) gain (b) phase

as follows:

$$\frac{V_1(s)}{V_{in}(s)} = \frac{s^2 L_{eq} C + 1}{s^2 L_{eq} C + sRC + 1} \tag{2.32}$$

$$\frac{V_2(s)}{V_{in}(s)} = \frac{1}{s^2 L_{eq} C + sRC + 1} \tag{2.33}$$

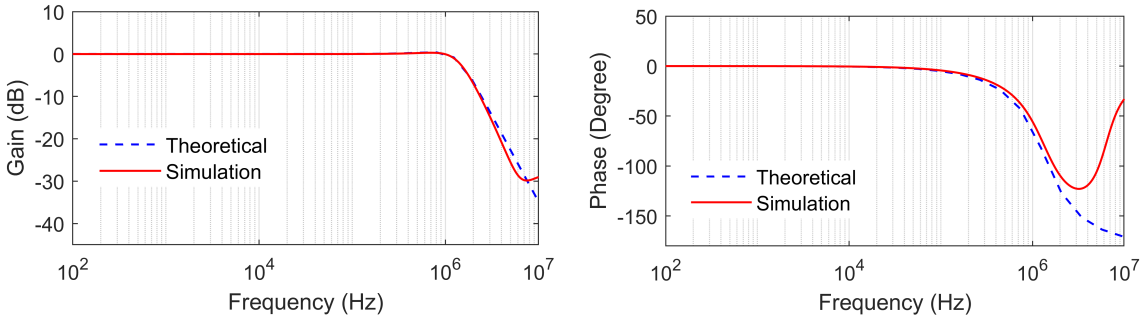
From equations (2.32) and (2.33), the cut-off frequency of the NF and LPF can be obtained as:

$$F = \frac{1}{2\pi\sqrt{L_{eq}C}} \tag{2.34}$$

The introduced floating inductor has also been evaluated in the VM filter application shown in Fig. 2.76. The component values selected for the floating inductor are C_3 = 100 pF, R_1 = 500Ω, and R_2= 4kΩ, resulting in an equivalent inductance, L_{eq}, of 200 μH. Additionally, for the VM filter in Fig. 2.76, passive components were chosen as C = 50 pF and R = 2 kΩ. Consequently, the center frequency F is approximately 1.59 MHz. The AC gain and phase responses for the NF and LPF outputs of the VM filter are illustrated in Fig. 2.77 and Fig. 2.78 respectively.

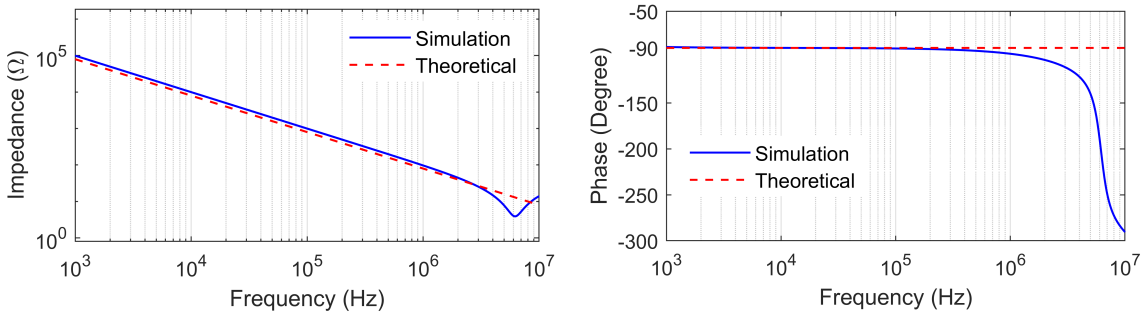
2.5.1.2 Results for capacitance multiplier circuits

The passive component values used in the simulations of floating capacitance multiplier circuits, FCM-1 and FCM-2 of Fig. 2.72 were selected as: R_2 = 100Ω, R_3



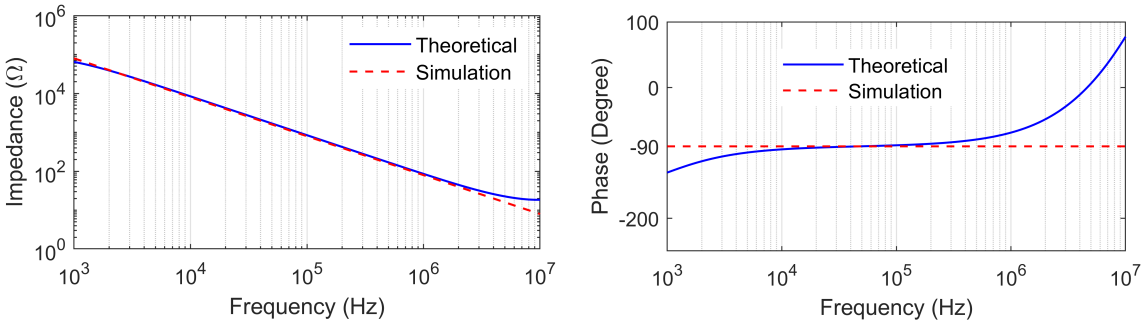
(a) (b)

Figure 2.78: Frequency responses of LPF (a) gain (b) phase



(a) (b)

Figure 2.79: Frequency responses of FCM-1 circuit (a) magnitude and (b) phase

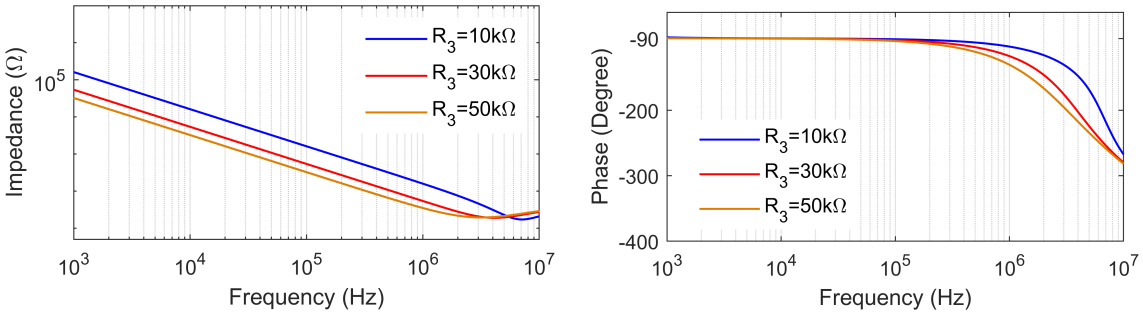


(a) (b)

Figure 2.80: Frequency responses of FCM-2 circuit (a) magnitude and (b) phase

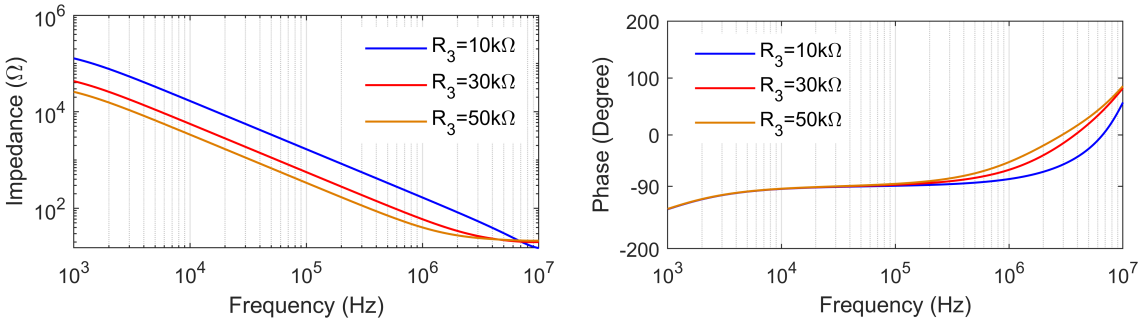
= 2kΩ, and C_1 = 100pF(for FCM-1;R_1 = 100Ω, R_3 = 2kΩ, and C_2 = 100pF(for FCM-2) and the corresponding results have been shown in Fig. 2.79 and Fig. 2.80 respectively.

Frequency responses of magnitude and phase of FCM-1 for different value of resistor



(a) (b)

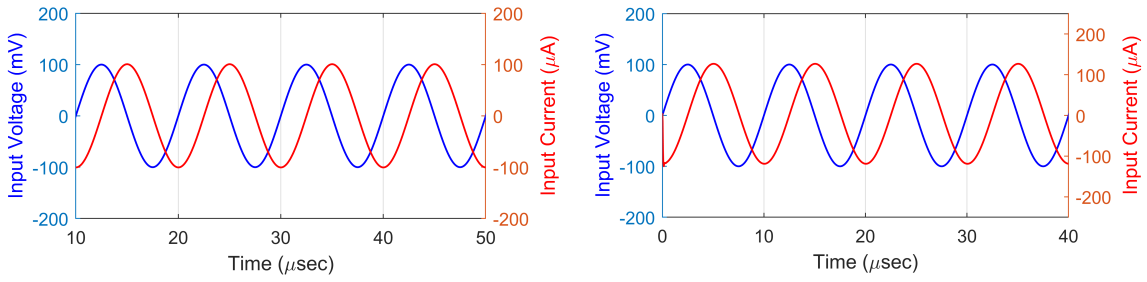
Figure 2.81: Frequency responses of FCM-1 circuit at different values of resistor R_3 (a) Magnitude and (b) phase



(a) (b)

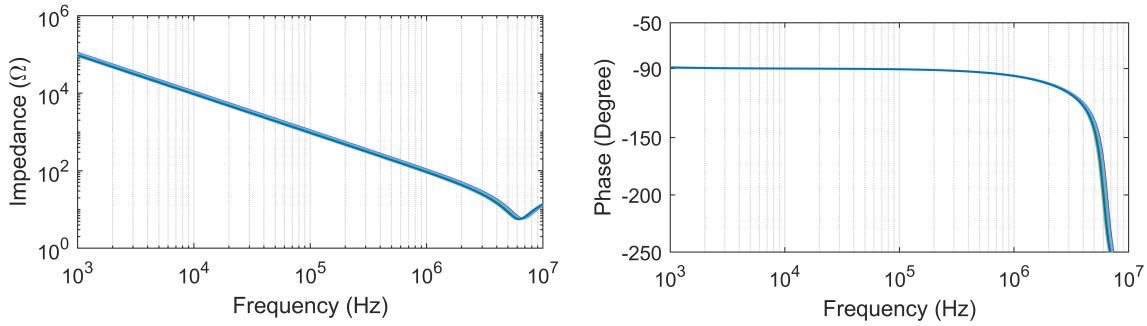
Figure 2.82: Frequency responses of FCM-2 circuit at different values of resistor R_3 (a) Magnitude and (b) phase

R_3(10kΩ, 30kΩ, 50kΩ), R_2 = 1kΩ and C_1 = 100pF have been shown in Fig. 2.81 Similarly, for FCM-2 value of resistor R_3 were 10kΩ, 30kΩ, 50kΩ, R_1 = 1kΩ and C_2 = 100pF and results have been shown in Fig. 2.82 A sinusoidal input voltage with a magnitude of 100mV and a frequency of 100kHz was applied to analyze the effect of time-domain analysis on both FCM circuits (FCM-1 and FCM-2). The corresponding waveforms of input voltage and input current have been shown in Fig. 2.83. Monte-Carlo simulations have been performed for the FCM-1 and FCM-2 with 100 runs. The results have been shown in Fig. 2.84 and 2.85 respectively, in which the passive component values deviate uniformly with 10%. The FCM-1 and FCM-2 circuits were also simulated across a range of temperatures to evaluate its robustness, with tests conducted from -50°C to 100°C. The frequency responses of impedance



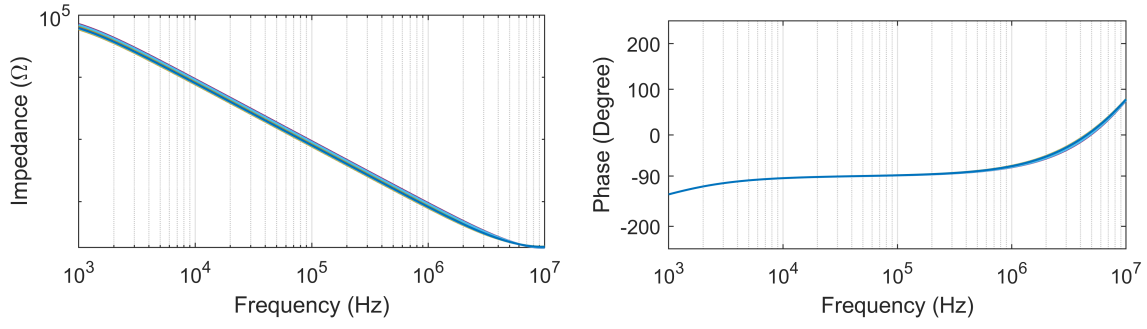
(a) (b)

Figure 2.83: Transient responses of (a) FCM-1 circuit (b) FCM-2 circuit



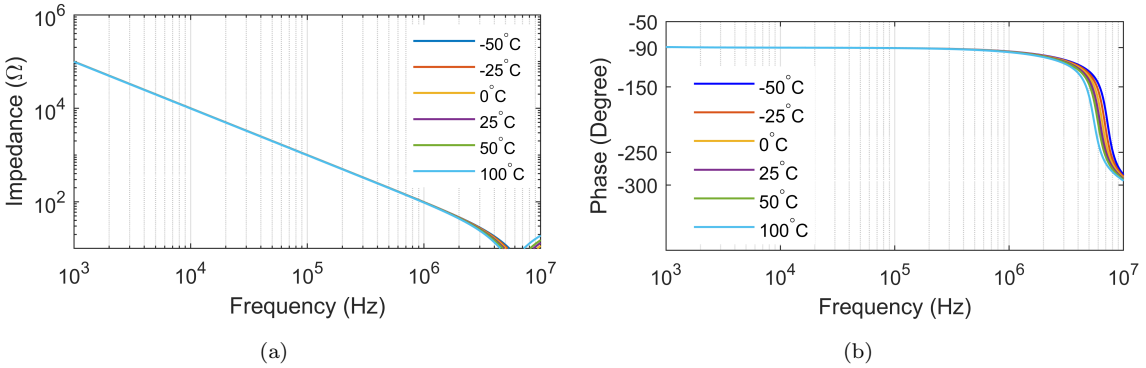
(a) (b)

Figure 2.84: Monte-Carlo simulations results of FCM-1 for 10% Gaussian deviation in resistor R_3



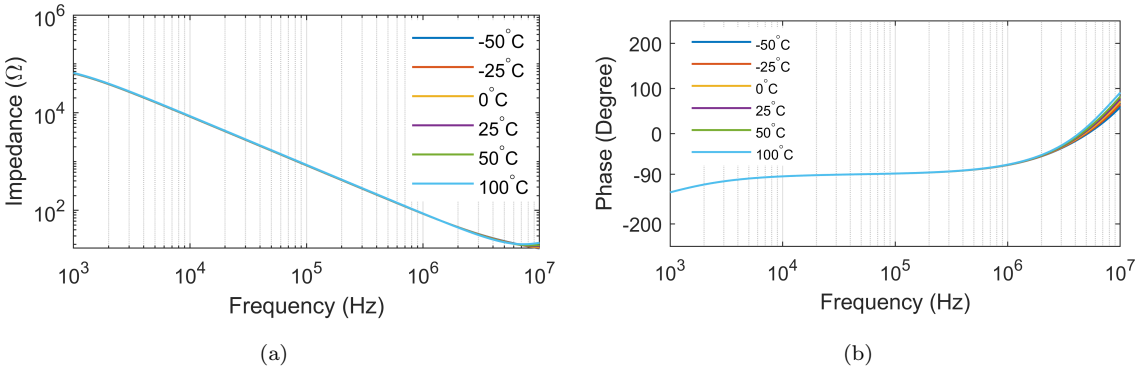
(a) (b)

Figure 2.85: Monte-Carlo simulations results of FCM-2 for 10% Gaussian deviation in resistor R_3



(a) (b)

Figure 2.86: Frequency responses of (a) impedance and (b) phase of FCM-1 at different temperatures



(a) (b)

Figure 2.87: Frequency responses of (a) impedance and (b) phase of FCM-2 at different temperatures

and phase for the FCM-1 circuit and FCM-2 circuit at various temperatures are shown in Fig. 2.86 and 2.87, respectively.

From Fig. 2.79 and 2.80, it can be observed that the simulated magnitude and phase responses of the FCM-1 and FCM-2 match well with the theoretical evaluations over a wide range of frequencies. Specifically, the impedance magnitude matches the theoretical values within the frequency range of 1kHz to 5MHz, while the phase matches between 1kHz to 800kHz for FCM-1 and between 10kHz to 500kHz for FCM-2.

The simulated results in Fig. 2.84 and Fig. 2.85 indicate that the magnitude and phase of the impedance in the FCM-1 and FCM-2 circuits remain relatively stable

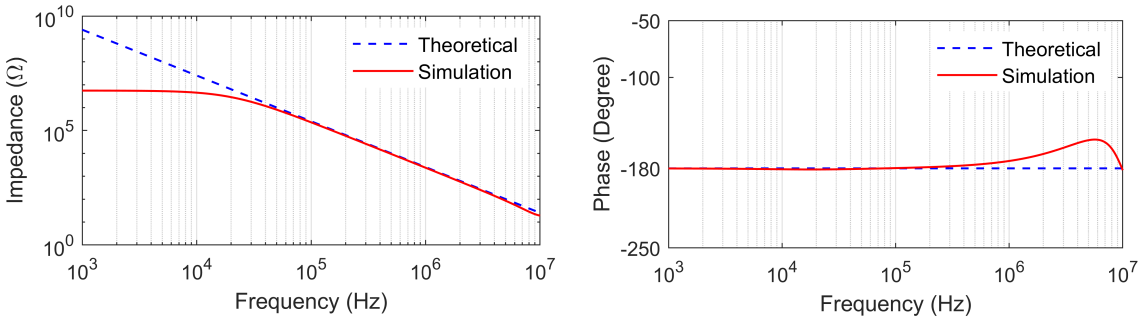


Figure 2.88: Frequency responses of (a) magnitude and (b) phase of floating FDNR circuit

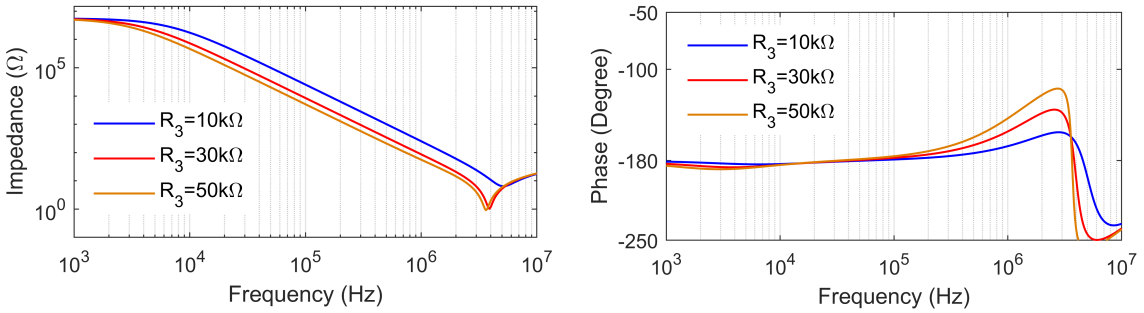
across a broad frequency range, even with 10% variations in resistor R_3. Additionally, the temperature analysis suggests that the proposed FCM-1 and FCM-2 circuits exhibit low sensitivity to temperature changes.

2.5.1.3 Results for FFDNR

To validate the functionality of the proposed floating FDNR circuit, the frequency responses of magnitude and phase of impedance, variations in magnitude and phase of impedance for different values of R_3, and transient responses of input voltage and current are presented. For the simulation purpose, the values of passive components were used as: $C_1 = 100$pF, $C_2 = 100$pF, and $R_3 = 1$kΩ. The corresponding results are displayed in Fig. 2.88 – Fig. 2.89.

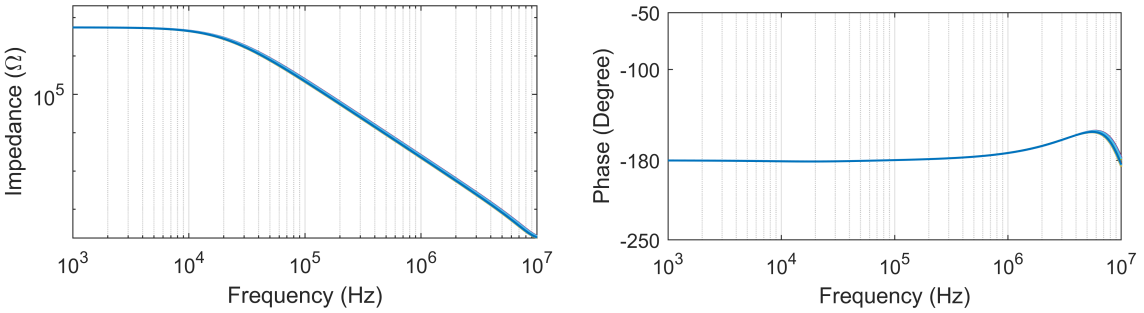
Monte-Carlo and temperature analyses have also been carried out and the corresponding results are shown in Fig. 2.90 and Fig. 2.91 respectively.

From the results shown in Fig. 2.88 – Fig. 2.91, it is observed that the simulation results obtained for floating FDNR circuit match with the theoretical evaluations. In order to verify the performance of the FFDNR, a band pass filter (BPF) circuit has been design using proposed FFDNR denoted in Fig. 2.92 Transfer function of



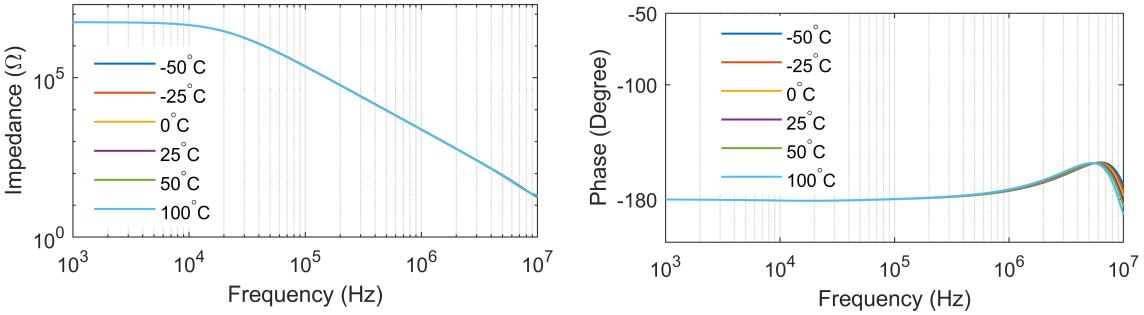
(a) (b)

Figure 2.89: Frequency responses of impedance of floating FDNR (a) magnitude and (b) phase



(a) (b)

Figure 2.90: Monte-Carlo simulations results for 10% Gaussian deviation in resistor R_3



(a) (b)

Figure 2.91: Frequency responses of impedance of floating FDNR showing variation in temperature (a) magnitude and (b) phase

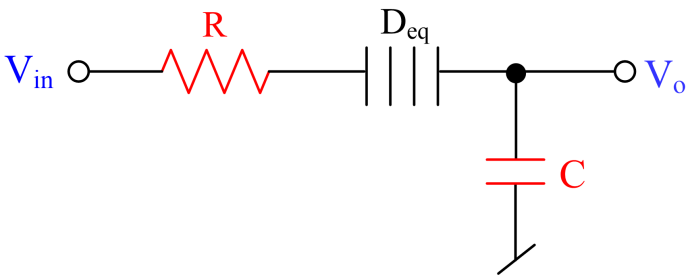
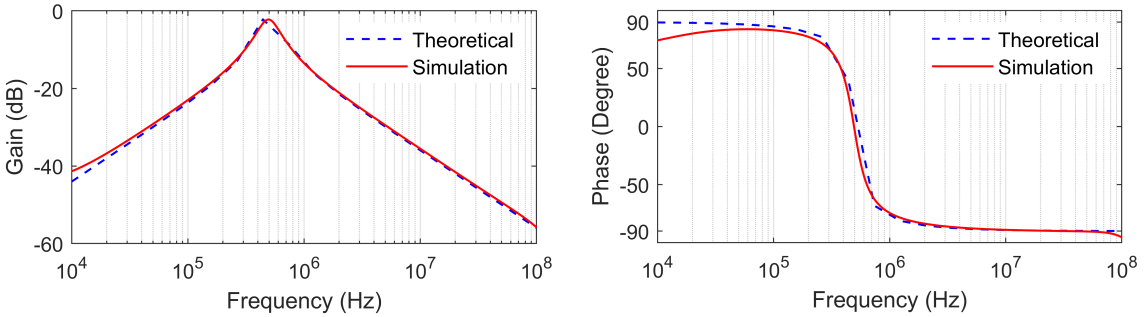


Figure 2.92: BPF as an application example of FFDNR



(a) (b)

Figure 2.93: (a) Magnitude (b) phase response of BPF

the BPF is demonstrated as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sD_{eq}}{s^2RCD_{eq} + sD_{eq}C + C} \tag{2.35}$$

From equation (2.35), the cut-off frequency of the BPF can be obtained as:

$$F_{BPF} = \frac{1}{2\pi\sqrt{RD_{eq}}} \tag{2.36}$$

For the pole frequency of 503.1kHz, passive components for realizing the BPF are selected as $C_1 = C_2 = 100$pF, $R_3 = 1$kΩ, R = 10kΩ. The corresponding magnitude and phase responses of BPF shown in Fig. 2.93

2.6 Floating Series immittance simulator

The proposed floating parallel simulator circuit can be also modified as floating lossy series immittance simulator whose circuit realization in shown in Fig. 2.94. Circuit

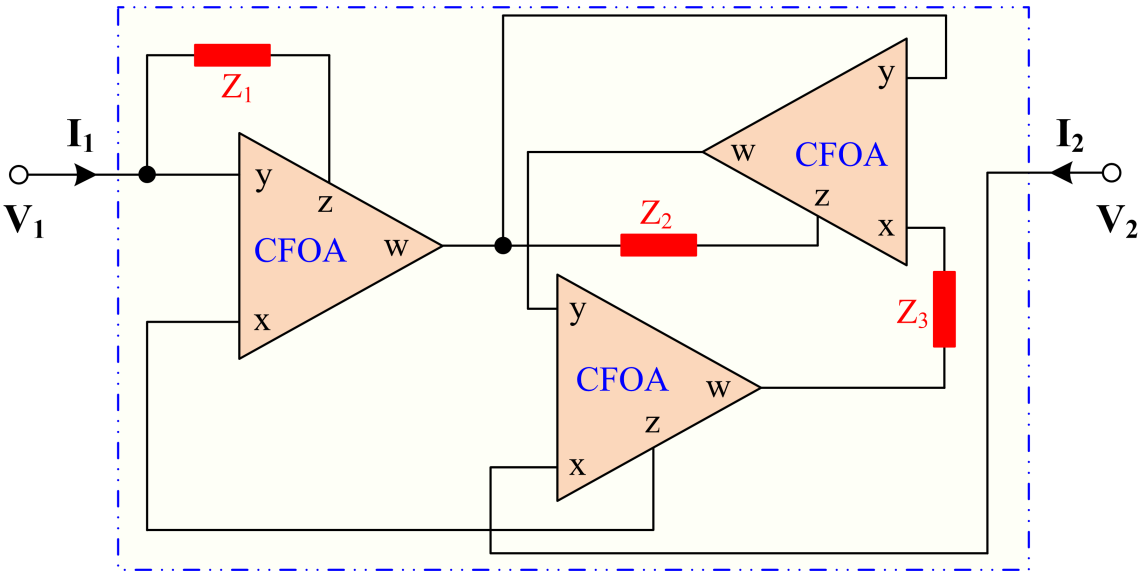


Figure 2.94: Floating series-type lossy immittance simulator circuit

analysis of Fig. 2.94 yields the following impedance matrix as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{Z_1\left[1+\frac{Z_2}{Z_3}\right]} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = Y_{eq} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.37}$$

where

$$Y_{eq} = \frac{1}{Z_1\left[1+\frac{Z_2}{Z_3}\right]} \tag{2.38}$$

Proper choice(s) of impedances Z_1, Z_2 and Z_3 of Fig. 2.94 obtained in equation (2.37) yield different types of immittance simulator circuits like floating series R-L, floating series R-C, floating series C-D, and floating capacitance divider. The realizations of these circuits are described here.

Case I: To design a floating series R-L simulator using equation (2.37), one must

select specific impedances: $Z_1 = R_1$, $Z_2 = R_2$, and $Z_3 = 1/\mathrm{s}C_3$. The matrix equation that describes the series R-L circuit is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{(R_1 + sR_1R_2C_3)} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.39}$$

Case II: If the impedances of equation (2.37) are chosen as follows: $Z_1 = R_1$, $Z_2 = 1/\mathrm{s}C_2$ and $Z_3 = R_3$, then the circuit of Fig. 2.94 yields a floating series R-C simulator whose matrix equation can be obtained as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{\left[R_1 + \frac{R_1}{sC_2R_3}\right]} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.40}$$

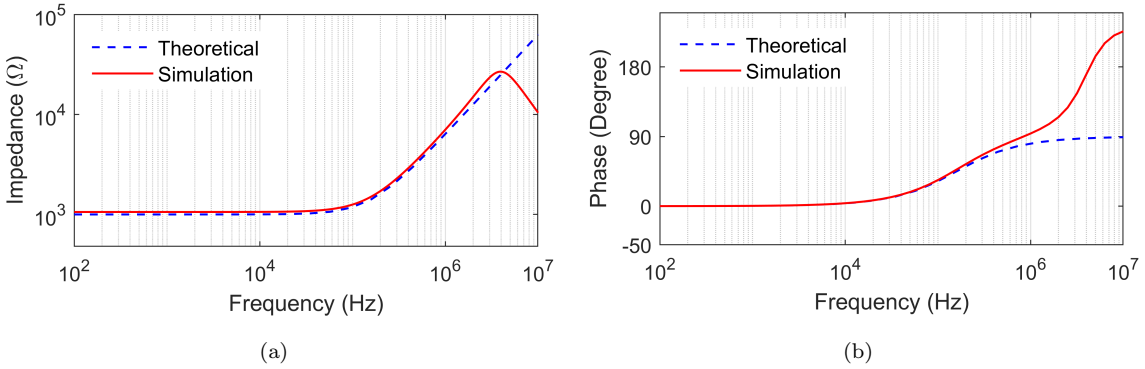
Case III: If we select $Z_1 = 1/\mathrm{s}C_1$, $Z_2 = 1/\mathrm{s}C_2$, and $Z_3 = R_3$, the circuit depicted in Fig. 2.94 will produce a floating series C-D simulator, and its matrix equation can be expressed as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{\left[\frac{1}{sC_1} + \frac{1}{s^2C_1C_2R_3}\right]} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.41}$$

Case IV: A floating capacitance divider can also be simulated with the following selection of impedances $Z_1 = 1/\mathrm{s}C_1$, $Z_2 = R_2$, and $Z_3 = R_3$.$Z_1 = 1/\mathrm{s}C_1$, $Z_2 = R_2$, and $Z_3 = R_3$.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{\frac{1}{sC_1}\left[1 + \frac{R_2}{R_3}\right]} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.42}$$

From equations (2.39) – (2.42), it is observed that the circuit shown in Fig. 2.94 can provide four different series type impedance simulators with the proper selection of impedances.



(a) (b)

Figure 2.95: Frequency responses of floating series R-L circuit (a) magnitude and (b) phase

2.6.1 Simulation results

The simulation results of the proposed floating series type immittance simulator circuit of Fig. 2.94 were performed using macro model of AD844 type CFOA in PSPICE simulator. The DC supply voltage of value ±15V were used to bias AD844. Various analyses such as frequency responses, transient responses, Monte-Carlo analysis, temperature analysis are performed for different circuit realizations.

2.6.1.1 Results for series R-L circuits

For the simulation of floating series R-L circuits derived from Fig. 2.94, resistors (R_1 = 1kΩ, R_2 = 10kΩ), capacitor (C_3 = 100pF) are selected, resulting R_{eq} and L_{eq} values are 1kΩ and 1mH respectively. The simulated frequency responses of the impedance and phase with theoretical values have been displayed in Fig. 2.95. The variations of impedance and phase of the series R-L circuits have been displayed in Fig. 2.96 by selecting the value of resistor R_2 = 10kΩ, 30kΩ, 50kΩ. The transient responses of input voltage and current for a sinusoidal voltage with amplitude of 50mV and a frequency of 200 kHz are displayed in Fig. 2.97.

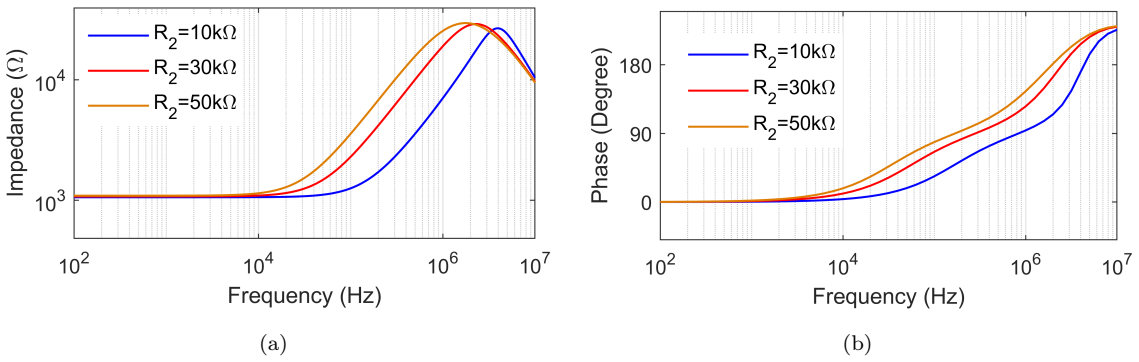


Figure 2.96: Frequency responses of floating series R-L circuit at different values of resistor R_2 (a) magnitude and (b) phase

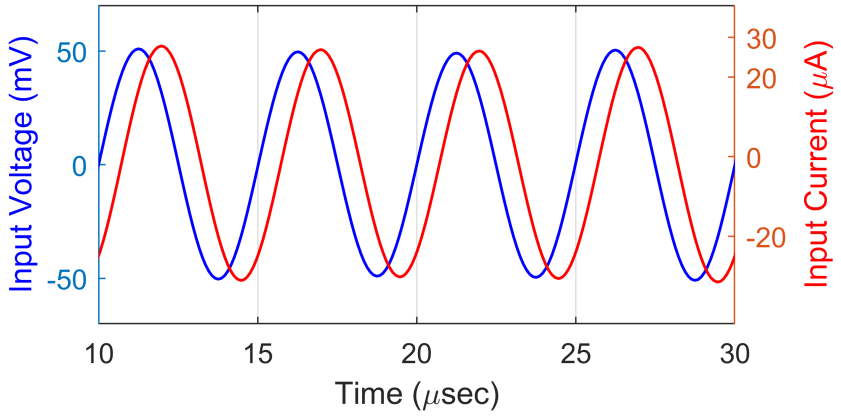


Figure 2.97: Time responses of floating series R-L circuit

From Fig. 2.95, the simulated frequency response of impedance and phase of floating series RL circuit are in proper accordance with the theoretical propositions up to a frequency range of 100Hz — 4MHz for impedance response and 100Hz — 500kHz for phase response. The proposed series R-L circuits were also simulated for Monte-Carlo and temperature analyses. In the Monte-Carlo analysis, a 10% tolerance was applied to resistor R_2, and the resulting magnitude and phase results are displayed in Fig. 2.98. For the temperature analysis, the circuits were simulated at temperatures ranging from -50°C to 50°C in increments of 25°C, and the corresponding results are presented in Fig. 2.99.

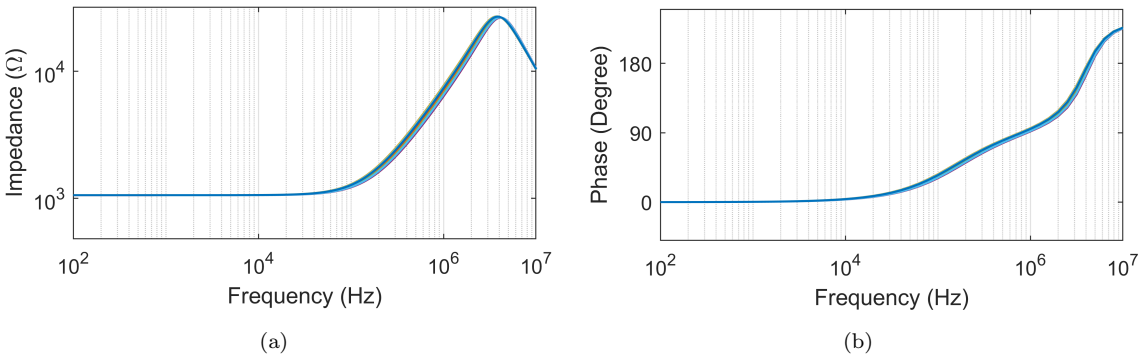


Figure 2.98: Monte-Carlo simulations results for 10% Gaussian deviation in resistor R_2

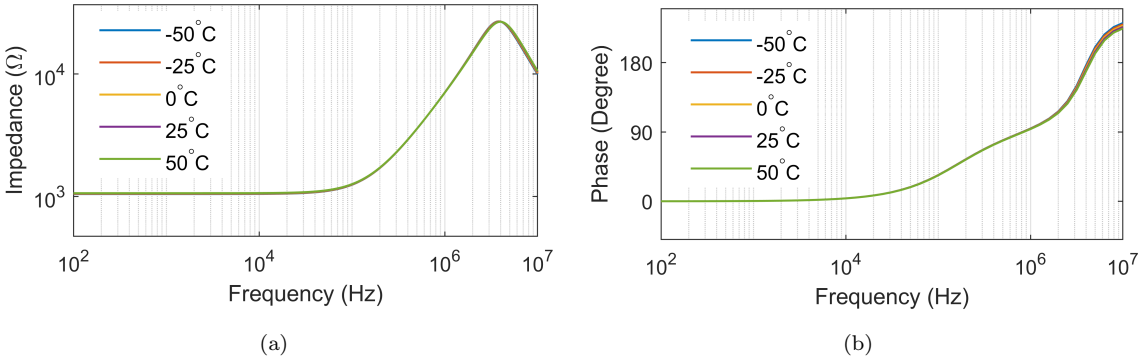
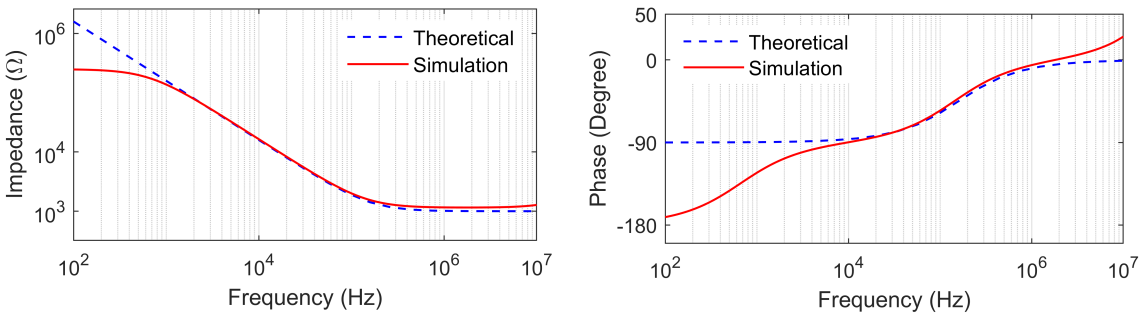


Figure 2.99: Frequency responses of floating series R-L showing variation in temperature (a) magnitude and (b) phase

2.6.1.2 Results for series R-C circuit

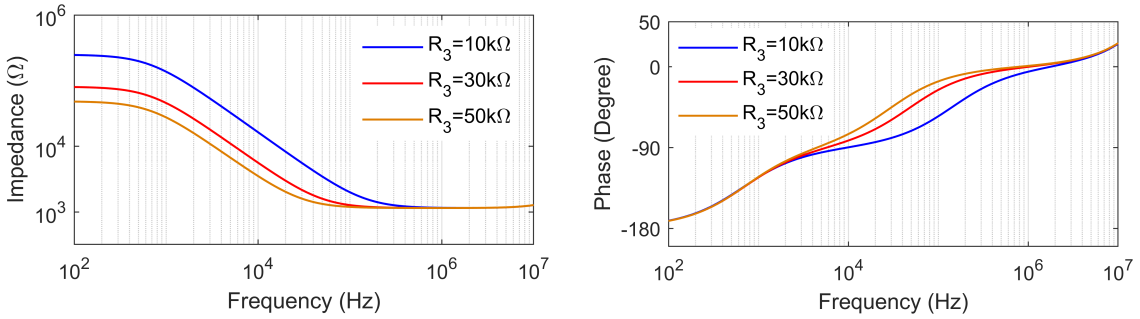
Simulation of the series R-C circuit of has been performed by selecting passive component values : $R_1 = 1\text{k}\Omega$, $R_3 = 10\text{k}\Omega$, and $C_2 = 100\text{pF}$, resulting in R_{eq} and C_{eq} values of $1\text{k}\Omega$ and 1nF, respectively. The magnitude and phase responses of series R-C have been shown in Fig. 2.100. Variation of impedance and phase responses for different value of resistor R_3= $10\text{k}\Omega$, $30\text{k}\Omega$, $50\text{k}\Omega$ have been shown in Fig. 2.101. A sinusoidal input voltage with a magnitude of 50mV and a frequency of 100kHz was used for time-domain analysis displayed in Fig. 2.102.

From Fig. 2.100, it can be observed that the simulated impedance matches the theoretical values within the frequency range of 1kHz to 9.3MHz, while the phase



(a) (b)

Figure 2.100: Frequency responses of series R-C circuit (a) magnitude and (b) phase



(a) (b)

Figure 2.101: Frequency responses of series R-C circuit at different values of resistor R_3 (a) magnitude and (b) phase

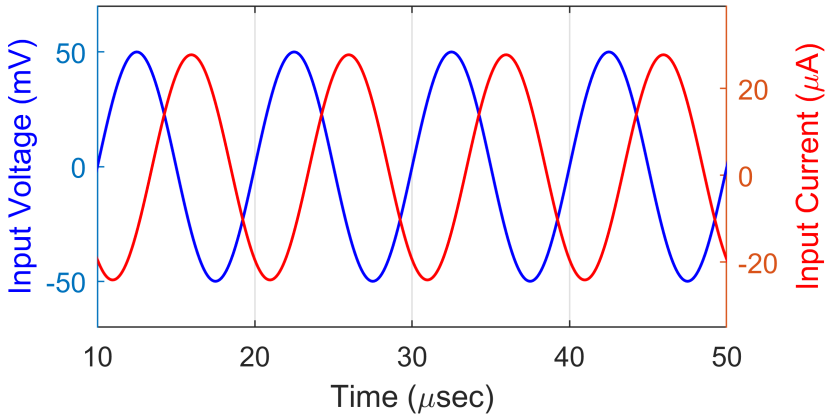
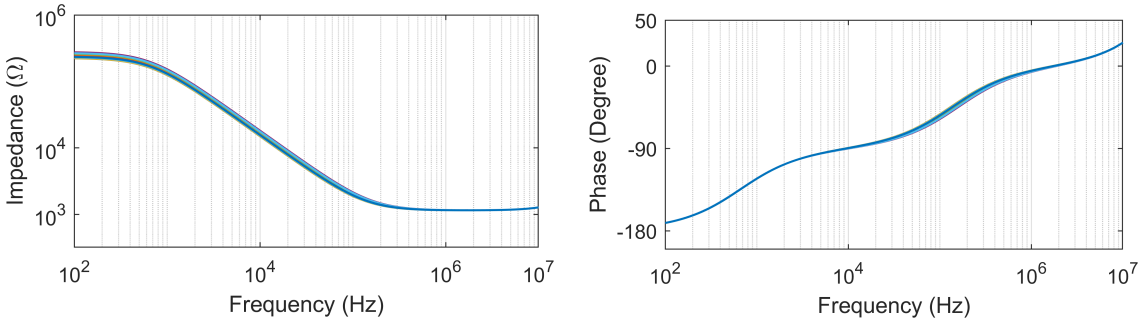


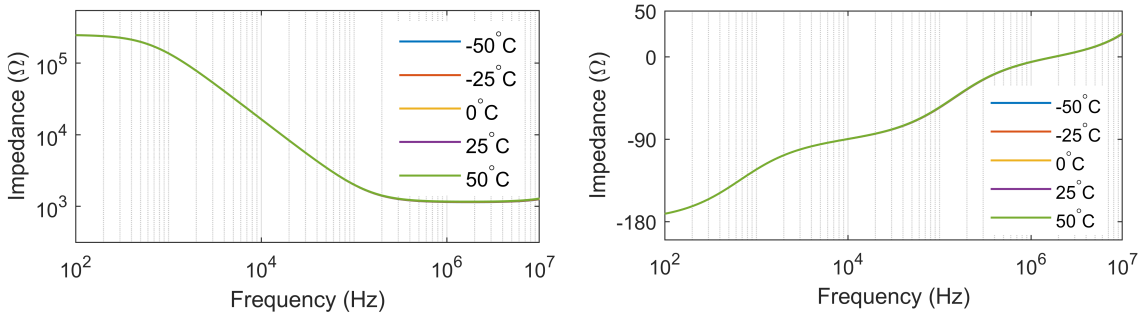
Figure 2.102: Time responses of series R-C circuit

matches between 9kHz to 1.5MHz. Monte-Carlo and temperature analyses have also been simulated and the corresponding results are shown in Fig. 2.103 and Fig. 2.104 respectively. The simulated magnitude and phase responses of the impedance



(a) (b)

Figure 2.103: Monte-Carlo simulations results for 10% Gaussian deviation in resistor R_3



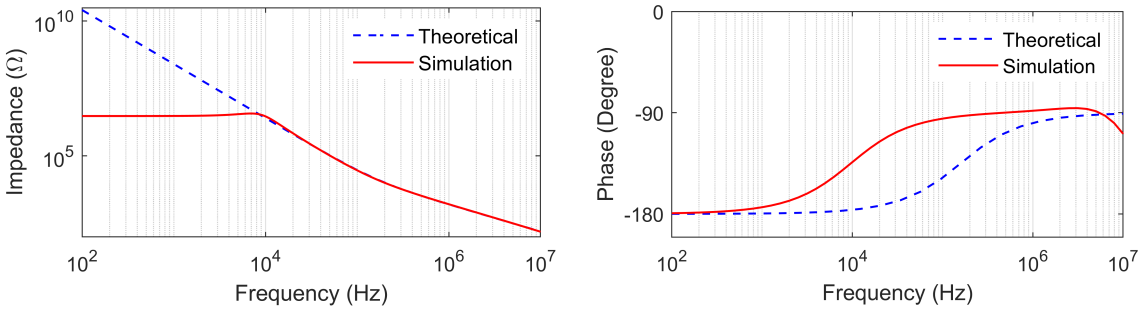
(a) (b)

Figure 2.104: Frequency responses of floating series R-C showing variation in temperature (a) magnitude and (b) phase

obtained from Monte-Carlo simulation results displayed in Fig. 2.103 shows less effects in the frequency range of 100Hz to 160kHz and 33kHz to 670kHz respectively. Furthermore, the temperature analysis results presented in Fig. 2.104 suggest that the proposed series RC circuits is less sensitive to changes in temperature.

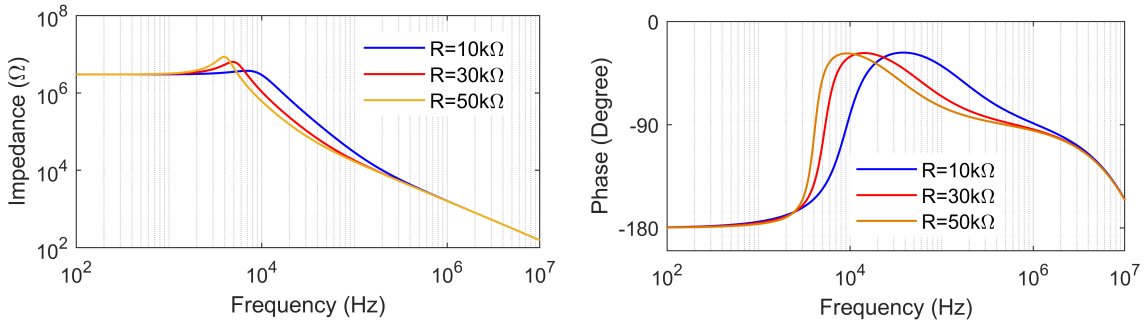
2.6.1.3 Results for series C-D configurations

To verify the functionality of the proposed series C-D circuit of Fig. 2.94, the frequency responses of magnitude and phase of impedance performed using C_1 = 100pF, C_2 = 100pF, and R_3 = 10kΩ have been shown in Fig. 2.105, variations in magnitude and phase of impedance for different values of resistor R_3 (10kΩ, 30kΩ,



(a) (b)

Figure 2.105: Frequency responses of series C-D circuit (a) magnitude and (b) phase



(a) (b)

Figure 2.106: Frequency responses of series C-D circuit at different values of resistor R_2 (a) magnitude and (b) phase

50kΩ) have been displayed in Fig. 2.106, and transient responses of input voltage and current are performed for a sinusoidal input voltage of magnitude 50mV at a frequency of 100kHz by selecting C_1 = 100pF, C_2 = 100pF, and R_3 = 10kΩ have been shown in Fig. 2.107. From the results shown in Fig. 2.105, it is observed that the simulation results obtained for series C-D circuit match with the theoretical propositions. Monte-Carlo and temperature analyses have also been simulated and the corresponding results are shown in Fig. 2.108 and Fig. 2.109 respectively. Fig. 2.108 and Fig. 2.109 show that the proposed series C-D simulator has insignificant changes, even when a 10% tolerance is applied to resistor R_3, and when there are changes in temperature from -50°C to 50°C.

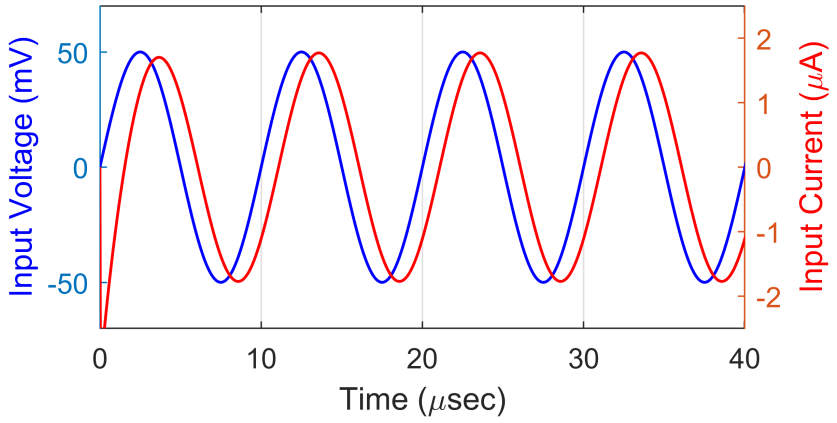


Figure 2.107: Time responses of series C-D circuit

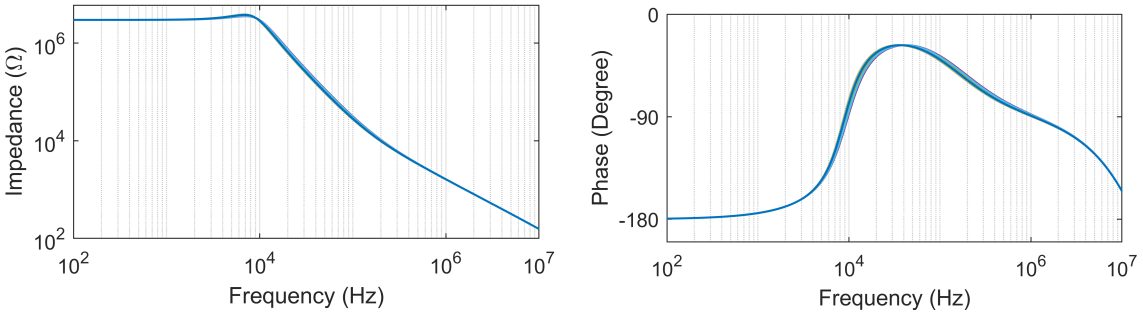
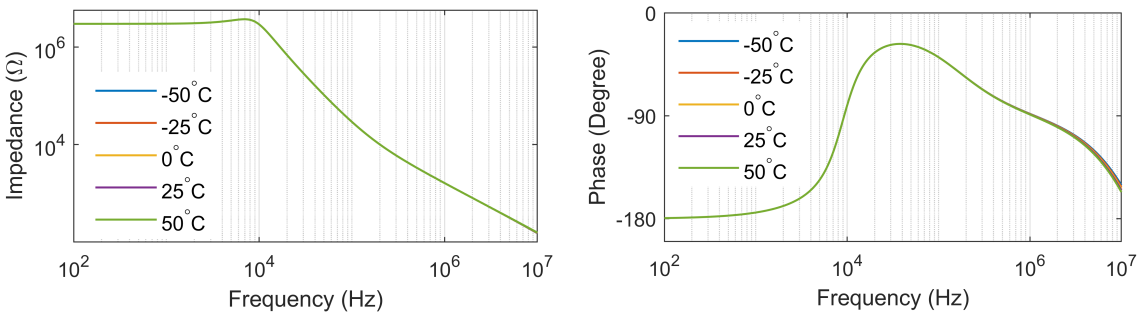


Figure 2.108: Monte-Carlo simulations results for 10% Gaussian deviation in resistor R_3

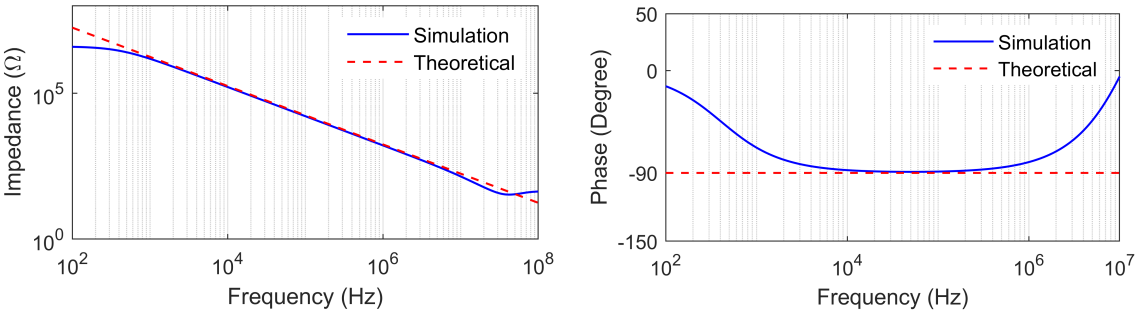
2.6.1.4 Results for floating capacitance divider circuit

Frequency analyses of the proposed floating capacitance divider circuit derived from Fig. 2.94 have been simulated by selecting passive component values as: $C_1 = 100$pF and $R_2 = 1$kΩ and $R_3 = 10$kΩ resulting in $C_{eq} = 90.9$pF and the respective magnitude and phase responses of impedance with their theoretical values have been shown in Fig. 2.110. AC Monte-Carlo simulations for Fig. 2.94 have been performed with 100 runs have with 10% tolerance in resistor R_3 displayed in Fig. 2.111. Time-domain analysis has been performed using a sinusoidal input voltage of magnitude 50mV at 100 kHz. The simulated transient responses of input voltage and input current of the proposed floating capacitance divider circuits have been shown in Fig. 2.112.



(a) (b)

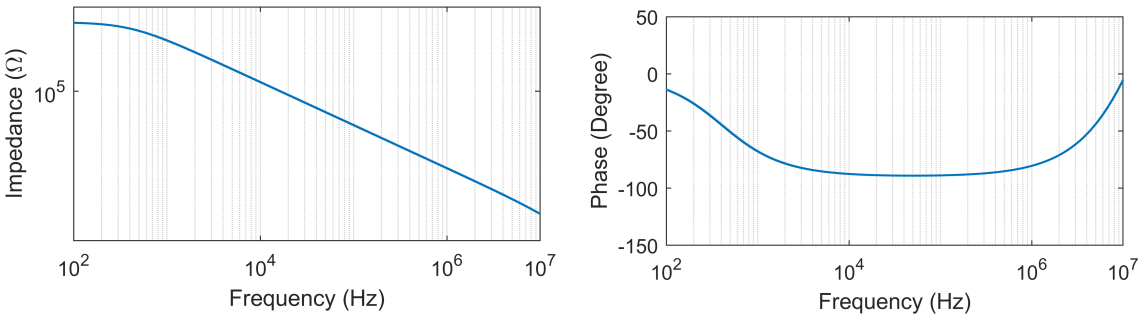
Figure 2.109: Frequency responses of floating series C-D showing variation in temperature (a) magnitude and (b) phase



(a) (b)

Figure 2.110: Magnitude and phase responses of the proposed floating capacitance divider circuit

The proposed circuits of Fig. 2.94 were also simulated at different temperatures for testing the performance and validated by varying the temperature from -50°C to 50°C. The frequency responses of the impedance and phase for different temperatures have been displayed in Fig. 2.113.



(a) (b)

Figure 2.111: AC Monte-Carlo simulation results of magnitude and phase of proposed floating Capacitance divider circuit

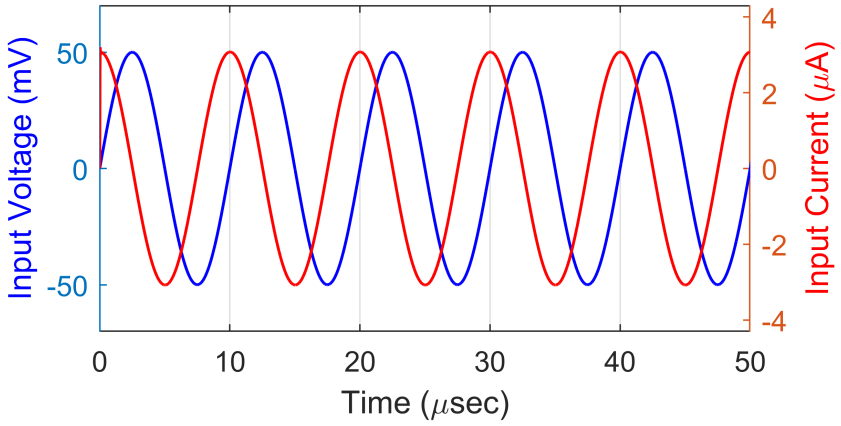
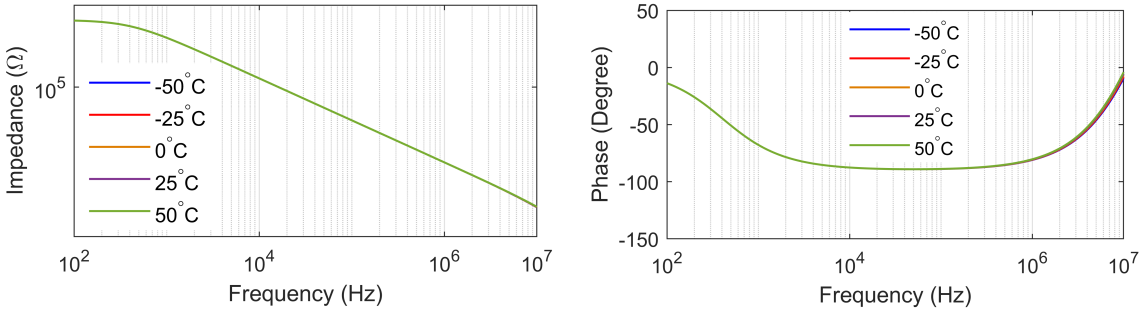


Figure 2.112: Time responses of input voltage and current of floating capacitance divider circuit



(a) (b)

Figure 2.113: Impedance and phase responses of Floating capacitance divider circuit at different temperatures

2.7 Concluding remarks

In this Chapter, we have presented three new configurations of negative grounded capacitance multipliers employing single CFOA. The proposed circuits are characterized by the following advantageous features simultaneously: (i) use of single ABB, (ii) no passive component matching constraints required, (iii) use of only single grounded capacitor (iv) high multiplication factor and (v) use of off-the-shelf available components only. The maximum multiplication factors of the proposed NGCMs have been obtained as 2001, 201 and 400 respectively. Various simulation results viz. frequency responses, transient responses, Monte-Carlo analysis, temperature analysis, noise analysis and PSRR analysis using PSPICE simulations have been included. The impedance and phase of the presented circuits have found to be insensitive with the changes in temperature. Sample experimental results employing AD844 type CFOA have also been included to validate the theoretical propositions.

Additionally,three floating immittance simulator circuits based on three CFOAs and three impedances have also been presented in this Chapter. The proposed circuit can be configured as a floating parallel/series R-L, floating parallel/series R-C, floating parallel/series C-D, an floating lossless capacitance multiplier simulator, floating lossless inductor simulator, floating FDNR circuits depending on the choice(s) of branch impedances. In all the presented simulator circuits, the value of L, C, D and lossless capacitance can be independently controlled through a single resistor without requiring any matching constraint of passive elements. Various application examples of the proposed circuits are presented to justify the theoretical analysis. The validation of the presented simulator circuits has been verified through several simulations using the macro model of AD844 type CFOA, which includes frequency responses, transient responses, Monte-Carlo analysis, and temperature analysis. Experimental results demonstrating the applications of proposed floating

simulator circuits have also been included using AD844 type CFOAs to validate the theoretical propositions.

Chapter 3

Single CFDITA based Grounded Capacitance Multiplier Circuits

3.1 Introduction

In Chapter 2, we have presented several grounded and floating immittance simulator circuits using CFOA. In the present Chapter we have proposed two grounded lossy/lossless capacitance multiplier circuits using CFDITA.

Different types of transconductance amplifiers have also been used in previous research works to design CMs, including operational transconductance amplifiers, voltage differencing transconductance amplifiers, and current follower transconductance amplifiers including CFDITA. Lossy and lossless grounded capacitance multipliers have been previously reported in various research papers, whose aim is to increase the value of a capacitor without introducing any loss or degradation in the circuit's performance. By providing a brief overview of these previously reported single ABB

based lossy and lossless GCMs, the proposed work can be better understood and contextualized.

3.1.1 Lossy capacitance multiplier

In [77], a lossy capacitance multiplier has been presented using a single voltage differencing transconductance amplifier (VDTA) and one capacitor, with an electronically tunable multiplication factor falling in the range of 115 to 150.

In [81], three CM circuits have been implemented using a single VDTA (two of them are lossless employing one VDTA, one grounded resistor and a floating capacitor) while the third is a lossy grounded capacitance multiplier implemented with one grounded resistor and one floating capacitor with a tunable multiplication factor remaining constant from 10 kHz to 1 MHz. The VDTA in all these circuits is implemented with Arbel-Goldminz cell (one half of complete VDTA configuration).

In [189], two immittance simulator (series RC and parallel RC) circuits have been implemented using a single voltage difference transconductance amplifier (VDTA) and one grounded capacitor, with electronically tunable multiplication factors without passive component matching requirements.

In [113], two grounded immittance simulator circuits (one series RC and one parallel RC) have been presented, using a single VDTA, one grounded resistor, and one grounded capacitor. The multiplication factor of these circuits can also be controlled electronically without requiring any passive component matching conditions.

In [190], a grounded parallel-type RC simulator circuit has been presented using two differential voltage to current converters (DVTC), two resistors, and one capacitor with adjustable equivalent capacitance.

In [191], a grounded RC impedance simulator employing two DVTC, two resistors and one capacitor has been reported with independently controllable equivalent capacitance.

A differential voltage buffer (DVB), electronically controllable CCII (ECCII-) and a single- capacitor based capacitance multiplier has been presented in [192]. The reported circuit can also be used as lossy capacitance multiplier while considering the output resistance of DVB and input resistance at input terminal of ECCII-.

In [193], a lossy capacitance multiplier circuit has been realized using a dual output operational transconductance amplifier (DO-OTA) with sink current, source current and a grounded capacitor.

Two lossy capacitance multipliers were implemented in [19], one using two single-output operational transconductance amplifiers (SO-OTA) and a floating capacitor, and another using a dual output operational transconductance amplifier (DO-OTA) and a floating capacitor. The third circuit was a DO-OTA-based three-stage capacitance multiplier consisting of three DO-OTAs and one capacitor.

A lossy capacitance multiplier circuit based on a single VDTA and one capacitor was reported in [194]. In this circuit, electronic control of capacitance is not possible, but resistance can be adjusted electronically.

From above description, it is seen that there have been limited number of designs of lossy capacitance multipliers in the open literature using various ABBs. No single CFDITA based lossy capacitance multiplier circuit has been proposed yet. A circuit with parallel immittance simulator having negative resistance and positive capacitance is useful in oscillator design and only one circuit, using two CFOAs, two resistors and one capacitor, has been reported in [128]. Therefore, in this chapter,

a new lossy capacitance multiplier circuit is proposed using a single CFDITA, one resistor and one capacitor has been discussed in Section 3.2.

3.1.2 Lossless capacitance multiplier

Op-amp based capacitance multiplier circuit has been reported in [1] employ a Op-amp in the unity gain connection, two resistors and a grounded capacitor.

In [26], three circuit configurations for the component multiplier using IC AD844, configured as a CCII+ with a buffer, have been proposed.

A translinear loop consisting of four transistors has been utilized in [195] to implement a CM circuit, incorporating impedance and four current sources. The circuit's multiplication factor can be adjusted by varying two currents, and the maximum achievable multiplication factor is 300. References [127], [128] and [130] describe CM circuits that utilize two CFOAs along with one capacitor and a minimum of two resistors to attain a positive MF.

Reference [25] discusses two distinct CM circuits. The first circuit employs a single current gain CCII- and one capacitor, while the other circuit utilizes one CCII+, one CCII-, two resistors, and one capacitor to realize a positive CM circuit. .Another CCII- based capacitance multiplier circuit has been reported in [196].

Reference [197] reports a CM circuit based on a DXCCII, two MOS resistors, and one capacitor, with a maximum achievable capacitance MF of 50.

A grounded capacitance multiplier circuit, based on a single TFTFN and one capacitor, is discussed in Ref. [198] Additionally, the article discusses the conversion of a grounded-type CM circuit into its floating counterparts.

In [193], both lossy and lossless common-mode circuits have been documented, employing operational transconductance amplifiers (OTA). These circuits allow for a maximum achievable scale factor of 10.

Another noteworthy circuit, utilizing OTA and CCII, is presented in [119]. It facilitates both positive and negative impedance multiplier circuits with a maximum MF of up to 400.

In [81], two circuits have been implemented and both of these circuits use a resistor and one capacitor to realize the CM circuit. The maximum achievable MF for these circuits is up to 20. In contrast, the circuit described in reference [**?**] does not necessitate a resistor for such implementation, and the maximum MF achievable is up to 115.

References [199] and [200] employ only one capacitor alongside active devices to achieve the function of impedance multiplication/CM. The maximum MF of capacitance obtained in [199] is 315, while in [200] this value is 25.

Reference [194] introduces a VDTA-based lossy capacitance and inductance simulator employing a single VDTA and one capacitor, without any matching constraints on passive components. In reference [74] , an electronically controllable CM circuit is discussed, employing a third-generation current conveyor transconductance amplifier (CCIIITA) along with one capacitor, capable of achieving an MF value of 50.

Reference [192] explores the use of a differential buffer and a current conveyor-based CM circuit, discussing both lossy and lossless structures.

Reference [79] presents two lossless positive/negative grounded capacitance multipliers, utilizing a current follower transconductance amplifier (CFTA), one resistor, and one capacitor. Using these circuits, an MF value of 10 can be achieved.

Reference [163] discusses the existence of two CFTAs, two resistors, and one capacitor, employed in two distinct grounded positive/negative capacitance multiplier circuit configurations. These circuits were verified to attain a maximum MF of 10 in both modes.

In [201], a capacitance multiplier utilizing a differential input buffered transconductance amplifier (DBTA) has been introduced. This circuit incorporates one DBTA, one grounded resistor, and one grounded capacitor. Notably, the MF of this circuit can be electronically adjusted via the transconductance of the DBTA.

Additionally, [202] employs a combination of a translinear stage and OTA stage to design a capacitance multiplier circuit, suitable for low frequency applications.

In [80], a capacitance multiplier circuit has been detailed, utilizing a single operational transresistance amplifier, one unity gain voltage buffer, three resistors, and one capacitor, for both positive and negative applications. Notably, electronic control is facilitated by substituting the resistors in the circuit with their MOS counterparts.

Reference [165] discusses a capacitance multiplier circuit based on a single current differencing transconductance amplifier (CDTA), incorporating one resistor and one capacitor. Moreover, the paper introduces an approach to convert grounded capacitance multiplier circuit into its floating counterpart.

A positive grounded capacitance multiplier has been reported in [78] employing one CCCDTA and one capacitor. The multiplication factor of the reported circuit can be enhanced upto 150.

In [203], a capacitance multiplier circuit was proposed employing a single active element MO-VDTA based on Arbel-Goldminz cells where large capacitance values and small chip areas are needed, such as in biomedical applications. This circuit was

implemented on the basis of current mode design. The multiplication factor can be tuned between 120 and 750 according to the input bias currents.

Another MO-VDTA based capacitance multiplier built by employing DTMOS transistors has been reported in [204].

Recently, interesting circuits of grounded capacitance multiplier circuits using CFDITAs have been reported in the literature [151]–[153]

A grounded capacitance multiplier was reported in [151] using CFDITA, two resistors and one capacitor providing multiplication factor upto 30 (Fig 3.1). The transpose of this circuit has also been introduced using one VDBA, two resistors and one capacitor.

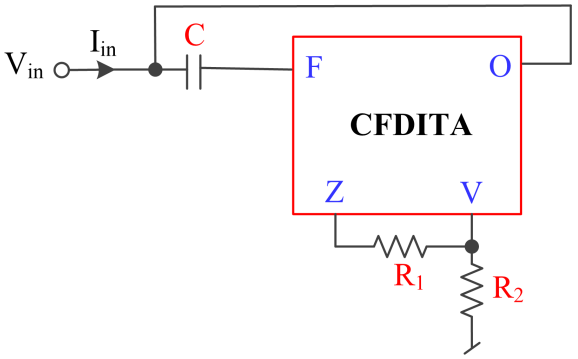


Figure 3.1: Capacitance multiplier circuit proposed in [151]

,

$$C_{eq} = C(1 + g_m R_1)$$

In [152], a grounded capacitance multiplier circuit has been presented employing one current follower differential input transconductance amplifier(CFDITA), three resistors and one capacitor which is shown Fig. 3.2.
Conversely, the circuit detailed in [153] utilized three CFDITAs in conjunction with two capacitors has been shown in Fig. 3.3.

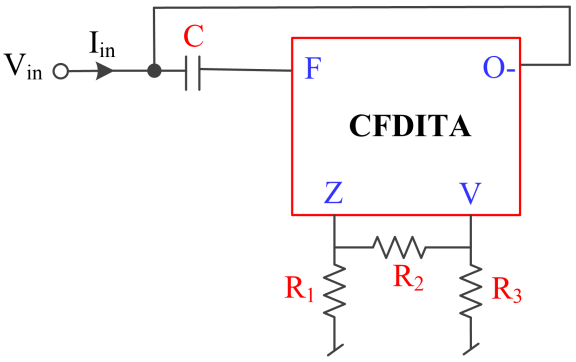


Figure 3.2: Grounded capacitance multiplier circuit proposed in [152]

,

$$C_{eq} = C\left(1 + \frac{g_m R_1 R_2}{R_1 + R_2 + R_3}\right)$$

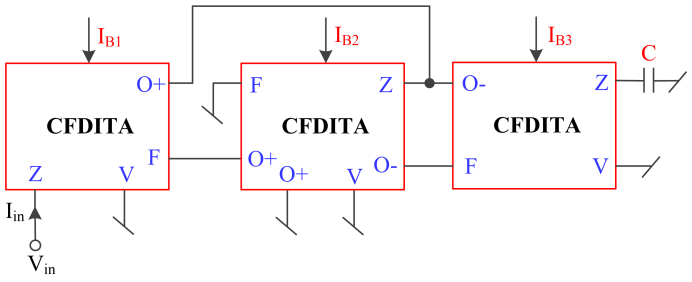


Figure 3.3: Capacitance multiplier circuit proposed in [153]

$C_{eq} = \frac{g_{m11}C}{g_{m32}}$; $g_{m11} = \sqrt{k_n I_{B1}}$, $g_{m32} = \sqrt{k_n I_{B3}}$

From the aforementioned descriptions of the lossless CM circuits, it can be observed that there is no reported circuit using CFDITA as of yet that offers electronically controllable capacitance utilizing a single CFDITA along with canonic number of one resistor and capacitor with a high MF value of up to 9202. In this chapter, new capacitance multiplier and parallel RL simulator circuits capable of both positive and negative multiplication factors are introduced. These circuits utilize a single CFDITA as the ABB in combination with one resistor and one capacitor. The proposed CM circuit can significantly boost the equivalent capacitance, up to 9202 times its original value, by adjusting the resistor. Furthermore, it can be electronically tuned, achieving up to 1800 times enhancement, by varying the transconductance

of the CFDITA, as discussed in Section 3.3.

3.2 Grounded Lossy Capacitance Multiplier

The proposed lossy capacitance multiplier circuit is shown in Fig. 3.4(a)[1] which employs a single CFDITA, one resistor and one virtually grounded capacitor and its equivalent circuit is displayed in Fig. 3.4(b). The input admittance of the proposed circuit of Fig. 3.4 (a) is obtained using ideal terminal equations of CFDITA (I_V = 0, $I_Z = I_F$, $I_O = g_m$ (V_Z - V_V) and $V_F = 0$) and is found to be:

$$\frac{I_{in}}{V_{in}} = Y_{in} = sC(2 + g_m R) - g_m = sC_{eq} - \frac{1}{R_{eq}} \tag{3.1}$$

where

$$C_{eq} = C(2 + g_m R) \; and \; R_{eq} = \frac{1}{g_m} \tag{3.2}$$

From equation (3.1), it is noted that the input admittance seen into terminal 'A' yields a grounded lossy capacitance i.e., a negative resistance in parallel with a positive capacitance. From the expression of C_{eq}, it can be observed that the multiplication factor of the capacitance can be adjusted independently through the resistance R.

3.2.1 Non-ideal Analysis

The proposed circuit has been analysed using non-ideal model of CFDITA as shown in Fig. 3.5. where R_F is the parasitic resistance at terminal-F, $Z_Z = (R_Z \parallel 1/\mathrm{s}C_Z)$,

[1]M. Shrivastava, P. Kumar, A. Raj, and D. R. Bhaskar, "Single current follower differential input transconductance amplifier based grounded lossy capacitance multiplier with large multiplication factor," International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 37, no. 1, e3139, 2024.

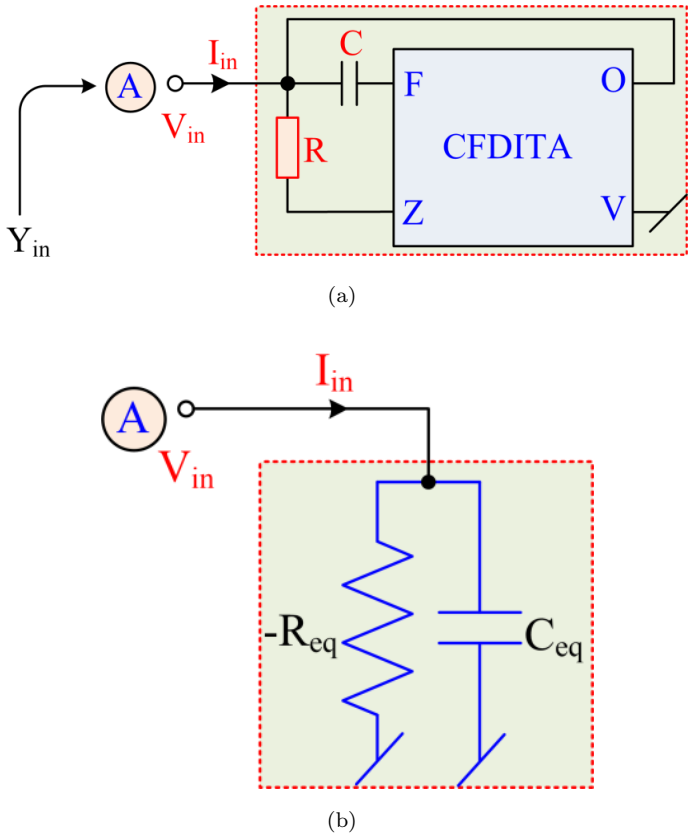


Figure 3.4: (a) Proposed lossy grounded capacitance multiplier circuit (b) Equivalent circuit

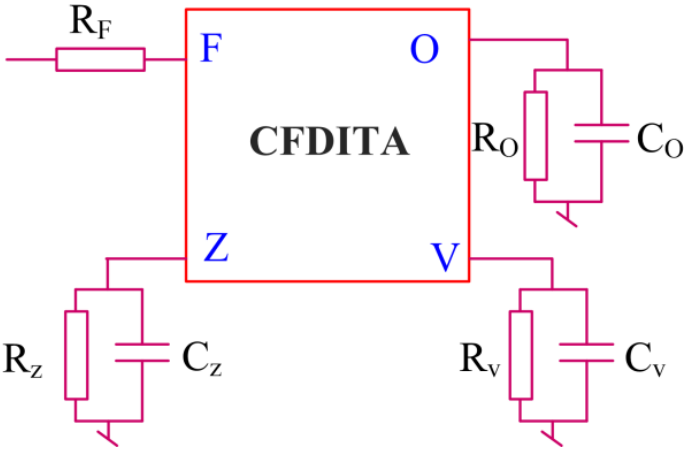


Figure 3.5: Non-ideal model of CFDITA including parasitic elements

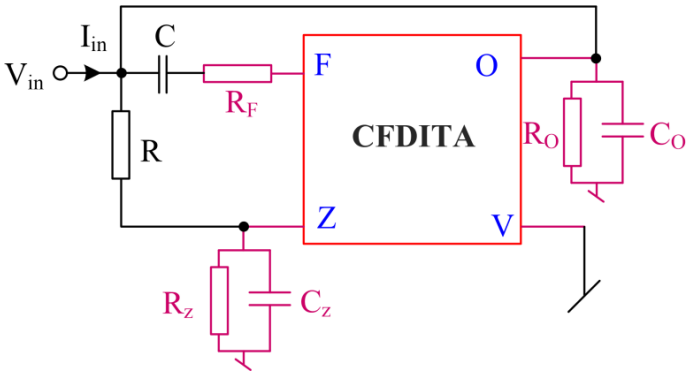


Figure 3.6: Proposed capacitance multiplier circuit including CFDITA parasitic

$Z_O = (R_O \parallel 1/\mathrm{s}C_O)$ and $Z_V = (R_V \parallel 1/\mathrm{s}C_V)$ are the parasitic available at terminals Z, O and V respectively. The values of different parasitic resistances and capacitances of CFDITA at different terminals have been quantitatively evaluated and provided in Table 3.1.

Table 3.1: Parasitic resistances and capacitances values of CFDITA

Parameter	***Values***
R_F	***139.243 nΩ***
R_V	***64.91 GΩ***
R_Z	***311.86 GΩ***
R_O	***108.271 GΩ***
C_V	***1. 55 fF***
C_Z	***3.25 fF***
C_O	***0.000029 fF***

The complete structure of proposed capacitance multiplier including CFDITA parasitic is shown in Fig. 3.6. Considering the non-ideal effects of CFDITA, a routine circuit analysis of the circuit in Fig. 3.6 yields the expression for the non-ideal input admittance as:

$$Y'_{in} = \frac{1}{(\frac{1}{sC} + R_F)}[1 - (\frac{\frac{1}{sC} + R_F - R}{1 + \frac{R}{R_Z} + sC_Z R})(g_m + \frac{1}{R})] + (\frac{1}{R} + \frac{1}{R_O} + sC_O) \qquad (3.3)$$

Equation (3.3) highlights the significant influence of the parasitic resistances and capacitances of CFDITA on the proposed circuit and provides approximate equations to limit the lower (f_L) and higher (f_H) operating frequencies of the proposed circuit.

$$f \gg f_L \cong \frac{1}{2\pi}\left\{\frac{g_m R+1}{CR+\frac{CR^2}{R_Z}+C(g_m R+1)(R_Z-R)}\right\}$$
$$f \ll f_H \cong \frac{1}{2\pi}\left\{\frac{1}{CR_F+C_Z\left(\frac{RR_Z}{R+R_Z}\right)}\right\}$$

Substituting the values of parasitic resistances and capacitances from Table 3.1 into equation (3.3) reveals that the effect of parasitic on the CM circuit is reduced. Furthermore, this effect can be minimized through the appropriate selection of external passive components, such as ensuring that 1/sC is much greater than R_F and R is much smaller than R_Z and R_O. The simulation results demonstrate the effectiveness of these measures and have been discussed in simulation results section.

3.2.2 SPICE Simulation Results

The proposed lossy capacitance multiplier circuit has been validated using CMOS CFDITA, and its workability has been established through its implementation in 0.18µm CMOS technology using CFDITA, as shown in Fig. 3.7. Table 3.2 lists the aspect ratios of the transistors employed in the implementation.

For simulation results, the supply voltages and bias voltages used were V_{DD} = -V_{SS} = 1.32V V_{Bias} = 0.78V and V_{BB}= -0.7V respectively. The transconductance (g_m) was calculated as 4.6mS for the selected bias voltage. The passive component values used

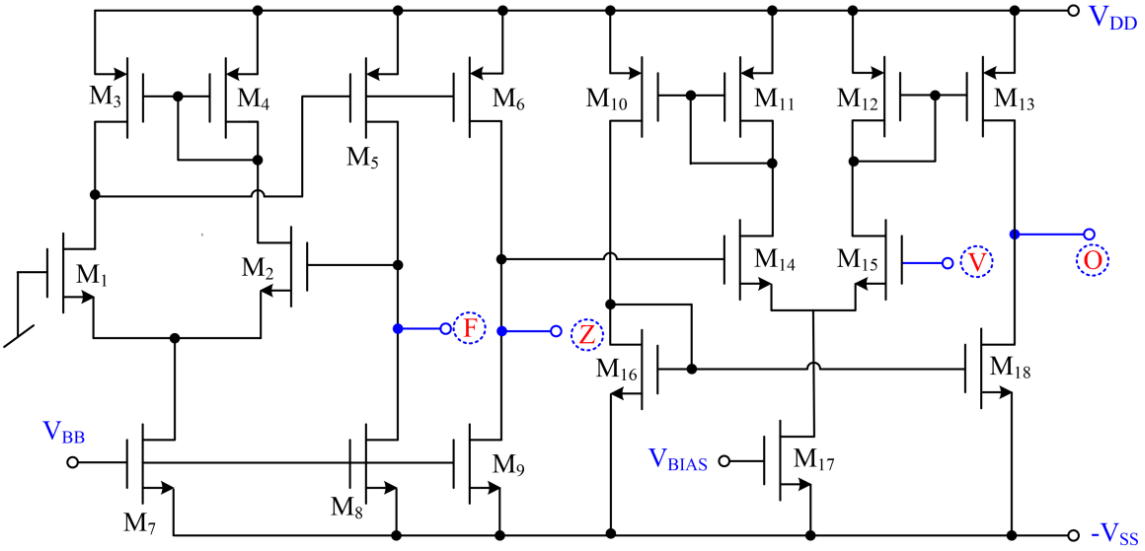
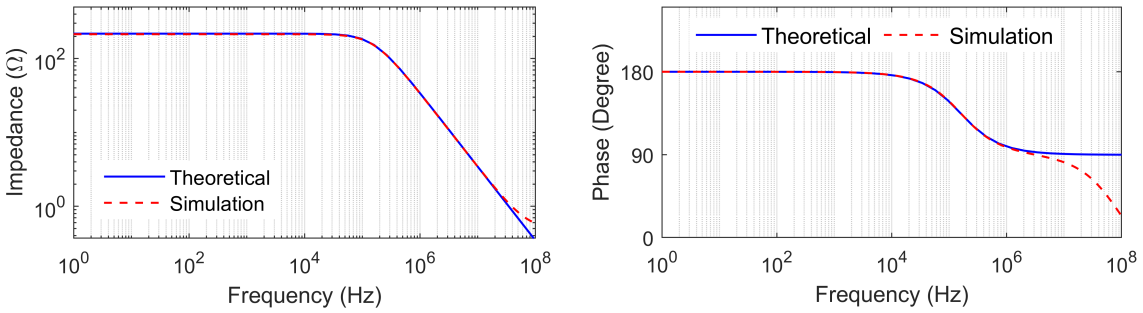


Figure 3.7: Proposed CMOS realization of CFDITA

Table 3.2: Aspect ratios of the MOSFETs used in 3.7

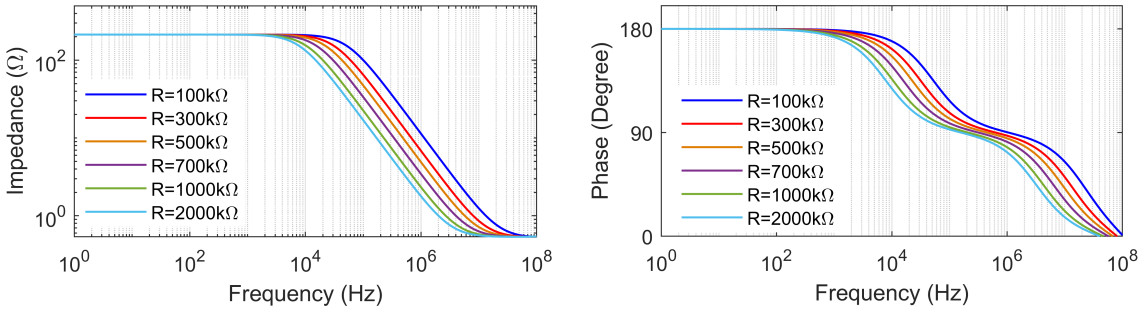
MOS transistors	***W(μm)***	***L(μm)***
M_1, M_2	***0.36***	***0.18***
M_3, M_4	***1.44***	***0.18***
M_5, M_6	***3.6***	***0.18***
M_7, M_8, M_9	***16.2***	***0.18***
M_{10}, M_{13}	***2.88***	***0.36***
M_{11}, M_{12}, M_{16}, M_{18}	***1.44***	***0.36***
M_{14}, M_{15}	***3.6***	***0.36***
M_{17}	***5.44***	***0.36***

for the simulation were taken as R = 100kΩ and C = 10pF. The magnitude and phase frequency responses of the proposed circuit, along with the corresponding theoretical evaluations, are illustrated in Fig. 3.8. Based on the observations made in Fig. 3.8, it can be concluded that the simulated impedance magnitude is consistent with the theoretical calculations over a frequency range spanning from 1Hz to 40MHz. Furthermore, the simulated phase of the lossy capacitance multiplier agrees with the theoretical value up to a frequency range of 1Hz to 3MHz. Additionally, the circuit's frequency analyses were conducted for various values of the controlling resistor (R =



(a) (b)

Figure 3.8: (a) Magnitude and (b) phase responses of proposed circuit

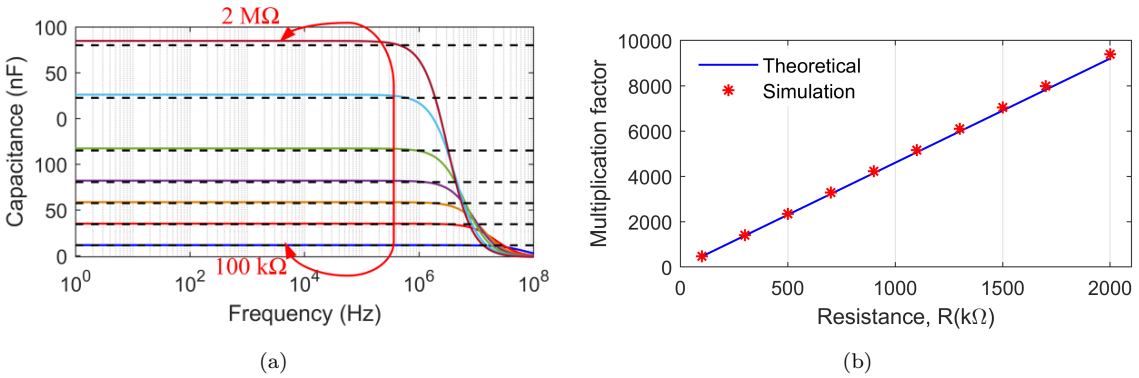


(a) (b)

Figure 3.9: Frequency responses of the proposed lossy capacitance multiplier (a) magnitude and (b) phase

100kΩ, 300kΩ, 500kΩ, 700kΩ, 1000kΩ, and 2000kΩ) while maintaining C at 10pF. The impedance's magnitude and phase frequency responses are presented in Fig. 3.9.

Observing Fig. 3.9, it can be concluded that changing resistor R results in a change in capacitance value while maintaining a constant impedance resistance of 281.2Ω, close to the ideal value of 282Ω. In Fig. 3.10(a) and Fig. 3.10(b), the analysis of the equivalent capacitance and the variations of the MF with resistance R are presented. The resistor R was varied from 100kΩ – 2MΩ in steps of 100kΩ, 300kΩ, 500kΩ, 700kΩ, 1MΩ and 2MΩ, while keeping g_m = 3.55mS and C = 10pF, resulting in C_{eq} values of 3.57nF, 10.67nF, 17.77nF, 24.87nF, 35.52nF and 71.02nF respectively.



(a) (b)

Figure 3.10: (a) Variation in capacitance by varying resistor R of the circuit of Fig. 3.4 and (b) Variation of multiplication factor for different values of R of the circuit of Fig. 3.4

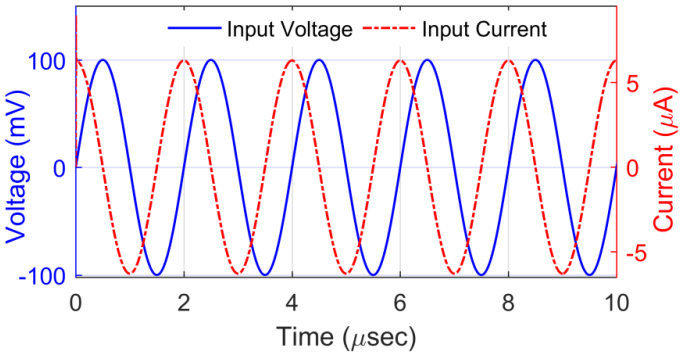
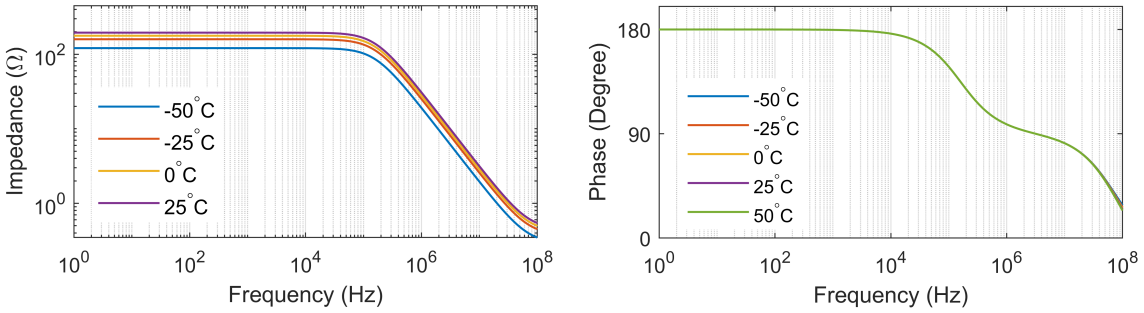


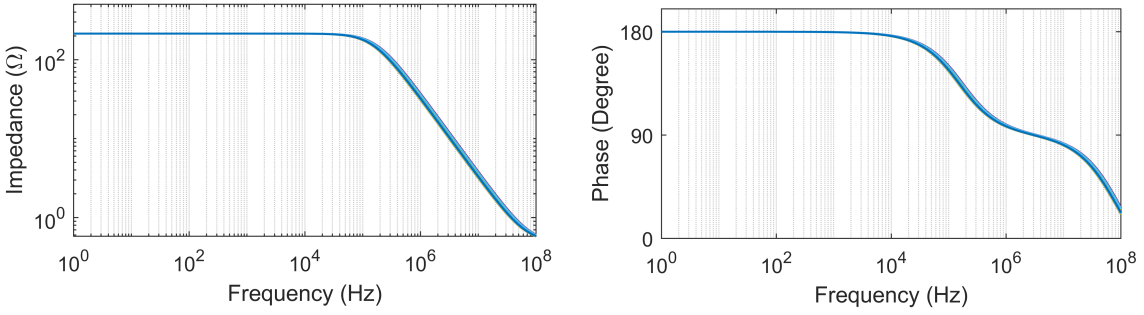
Figure 3.11: Simulated transient responses of input voltage and input current

The results depicted in Fig. 3.10(a) demonstrates that the simulated equivalent capacitances correspond closely with the theoretical values. Additionally, the MF is found to vary from 357 to 9202 as the resistance R is varied from 100k Ω to 2M Ω, which is consistent with the theoretical outcomes. Time-domain analysis has also been performed on the proposed circuit using a sinusoidal input voltage of 100mV magnitude at a frequency of 500 kHz. The resulting transient responses of the input voltage and input current of the proposed impedance are shown in Fig. 3.11. The proposed circuit has also been tested for robustness by performing temperature analysis, Monte-Carlo analysis and noise analysis. For temperature analysis, proposed circuit has been simulated for different temperatures varying from -50° C to 25° C and the corresponding results of magnitude and phase of the



(a) (b)

Figure 3.12: Frequency responses of proposed circuit for temperature variation (a) impedance and (b) phase



(a) (b)

Figure 3.13: Monte Carlo simulations with 5% Gaussian distribution in R deviation (a) magnitude responses (b) phase responses

impedance have been demonstrated in Fig. 3.12. For Monte-Carlo simulations, a tolerance of 5% has been provided in resistor and the proposed circuit simulated for 200 runs and the results have been shown in Fig. 3.13 (a) and (b). Noise is produced by both resistors and semiconductor devices, with its magnitude varying based on the frequency. To observe the effect of noise on multiplication factor of proposed circuit, noise analysis has been performed using different values of resistor R (100k Ω, 500k Ω, 1000k Ω) and C = 10pF and the corresponding result has been shown in Fig. 3.14.

The responses of Fig. 3.12 show that the magnitude of the impedance of the proposed circuit is affected by temperature changes from -50°C – 25°C due to the dependence

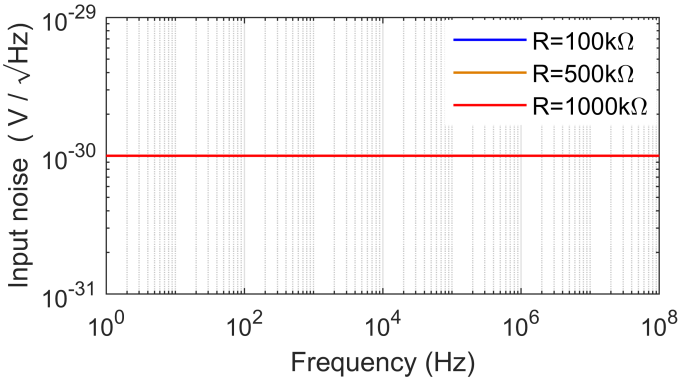


Figure 3.14: Simulated noise analysis responses

of transconductor, while the phase of the impedance remains largely unchanged across different temperatures. Fig. 3.13(a) and(b) display the Monte-Carlo results indicating that the proposed circuit's impedance and phase exhibit lower variability even in the presence of tuning resistor deviations. Fig. 3.14 indicates that the proposed circuit is relatively unaffected by noise, and that the input noise remains constant regardless of the value of the resistor R.

3.2.3 Layout Simulation Results

To validate the feasibility of the proposed capacitance multiplier circuit, pre-layout and post-layout simulations were conducted using the Cadence Virtuoso simulation tool. The layout of the proposed CMOS CFDITA is depicted in Fig. 3.15 and is designed using 0.18µm technology parameters. The MOSFET's width and length values were kept the same as those listed in Table 3.2. The power supply voltages, V_{DD} and V_{SS}, were set to 0.9V, while the bias voltage, V_{Bias}, was set to 0.4V. To confirm the feasibility of the proposed circuit, the layout of the CM circuit passed all physical verification checks, including design rule check (DRC), layout and schematic extraction (LVS), and RC extraction. The pre-layout and post-layout impedance and phase of the lossy capacitance multiplier are depicted in Fig. 3.16.

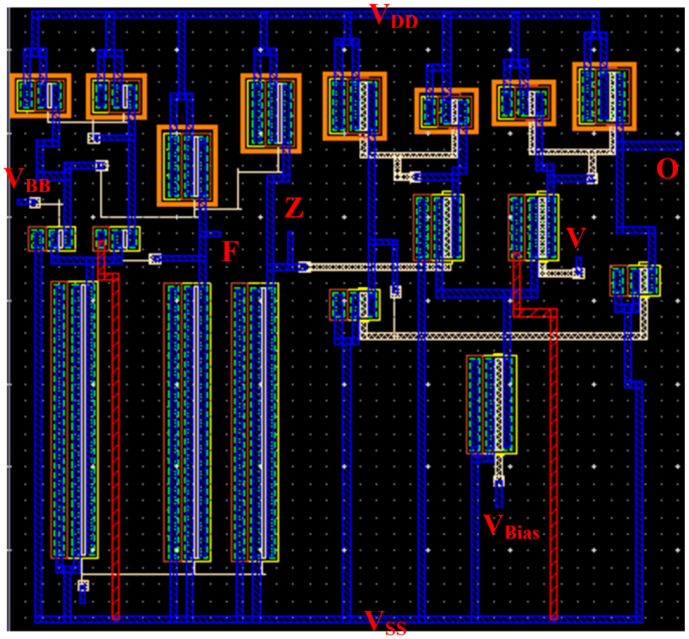
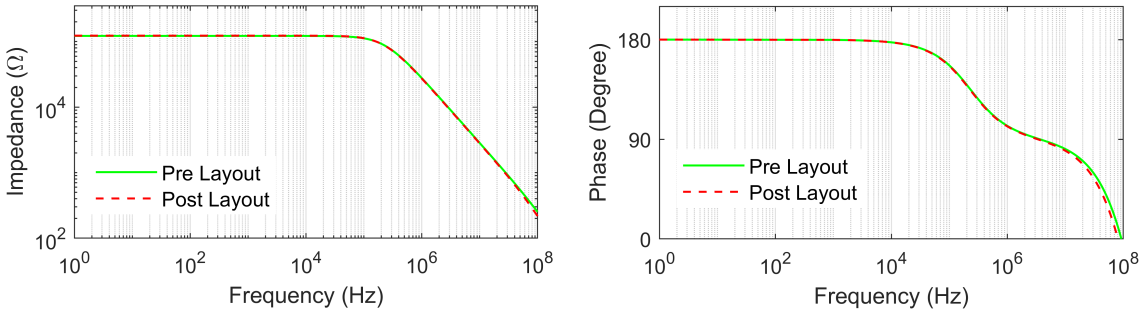


Figure 3.15: Layout of CFDITA



(a) (b)

Figure 3.16: Pre and post layout frequency responses of (a) impedance and (b) phase of the proposed CM circuit

From Fig. 3.16, it can be concluded that the pre-layout simulated magnitude and phase responses closely align with the post-layout results over a broad frequency range, spanning from approximately 1 Hz to 100 MHz. Thus, these results confirm the validity of the proposed configuration.

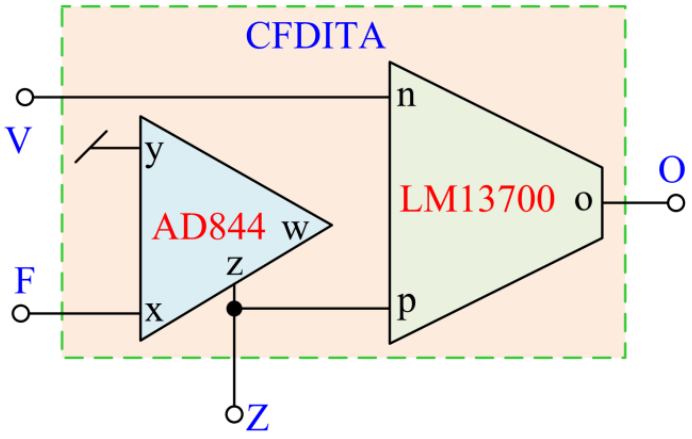


Figure 3.17: Implementation of CFDITA using commercially available ICs

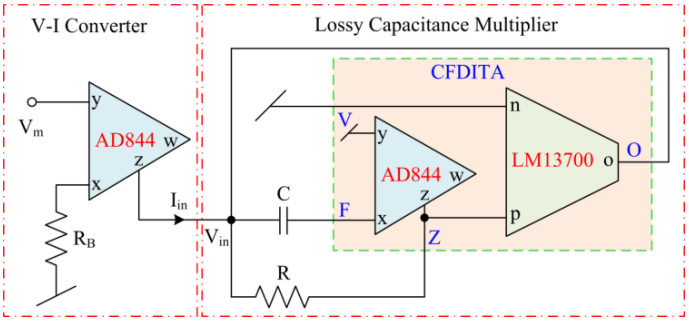


Figure 3.18: Schematic arrangement of proposed lossy capacitance multiplier using available off-the-shelf ICs

3.2.4 Experimental Results

The proposed circuit has also been verified experimentally using CFDITA implemented with commercially available ICs AD844 and LM13700 (Fig. 3.17) whose circuit realization has been demonstrated in Fig. 3.18. The schematic diagram of the proposed circuit (using Fig. 3.17) has been displayed in Fig. 3.18.

From Fig. 3.18, the frequency responses of magnitude and phase of the impedance of the proposed circuit can be obtained by evaluating the ratio of V_{in} and V_m, (V_m = I_{in} x R_B) which is proportional to V_{in} and I_{in}. A snapshot of experimental setup for the circuit in Fig. 3.4 is shown in Fig. 3.19, where both the ICs used were biased

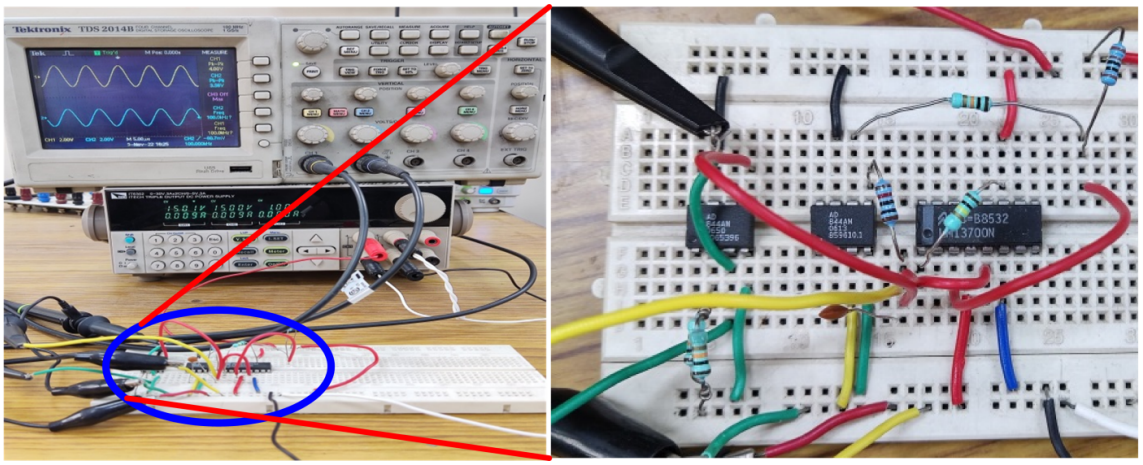


Figure 3.19: Snapshot of experimental setup of the lossy capacitance multiplier circuit of Fig. 3.4

using DC power supplies with a voltage of ±15V. Transconductance of LM13700 in Fig. 3.17 was set to 5.55mS by using equation (2.11) with R_{Bias} = 100kΩ, VT = 26mV and V_{BE} = 0.7V.

$$g_m = \frac{I_{Bias}}{2V_T}; where I_{Bias} = \frac{2V_{CC} - V_{BE}}{R_{Bias}} \tag{3.4}$$

The passive components used for the experimental verification are R = 10kΩ and C = 100pF, resulting in an equivalent capacitance of C_{eq} = 5750pF. The frequency responses of the magnitude and phase responses between V_m and V_{in} of the experimental setup, as shown in Fig. 3.19, are displayed in Fig. 3.20. The experimental transient responses of V_m and V_{in} for the proposed circuit, with an input voltage of magnitude 4V at different frequencies (100 kHz and 150 kHz), are shown in Fig. 3.21.

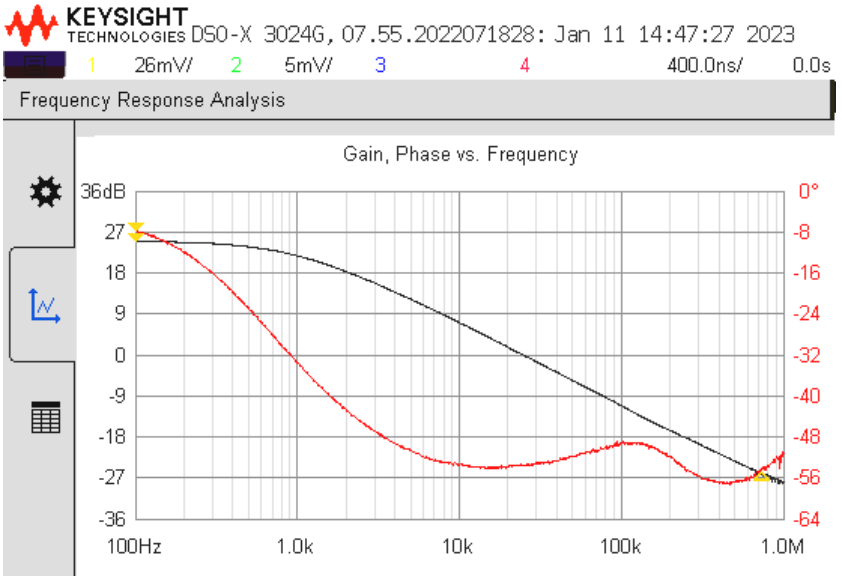
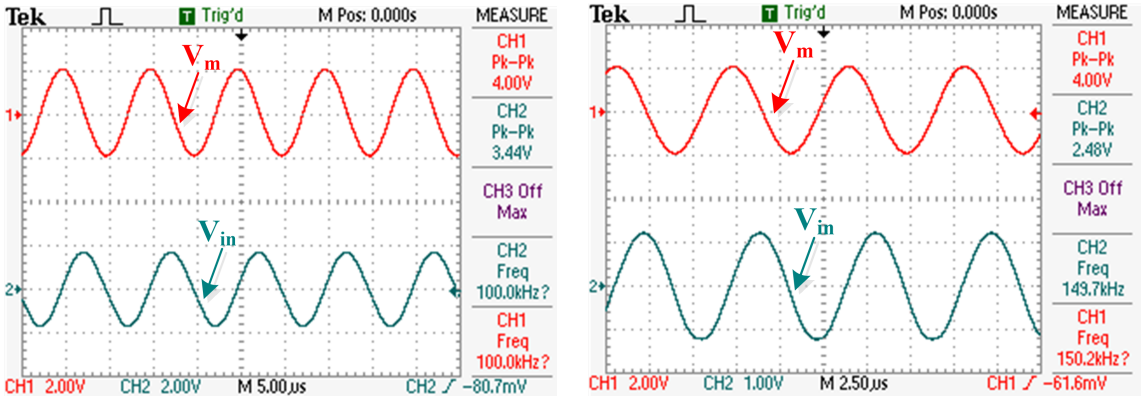


Figure 3.20: Frequency responses (a) magnitude (b) phase of the experimental setup shown in Fig. 3.18



(a) (b)

Figure 3.21: Experimental transient responses of proposed circuit at (a) 100kHz and (b) 150kHz

3.3 Grounded Lossless Capacitance Multiplier Circuit

The proposed lossless positive and negative grounded capacitance multiplier circuits are shown in Fig. 3.23[2] which utilize only one CFDITA, in conjunction with only one resistor and one virtually grounded capacitor.

In the literature, various topologies have been reported for implementing positive capacitance multipliers [156], [165], [164].Recently a very elegant and yet very simple circuit of positive capacitance multiplier using the concept of ideal gyrators has been presented in [205] which also includes a very exhaustive bibliography on CM. Most of these circuits utilize voltage feedback mode and current feedback mode approaches, as illustrated in [164]. In this section, we present a circuit model depicted in Fig. 3.22 , which is employed for designing new CM circuits.

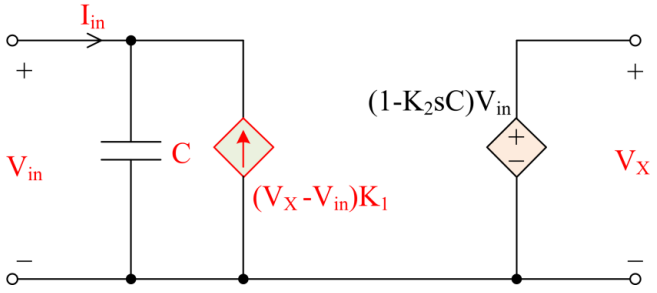


Figure 3.22: Approach to implement of CM circuits

The circuit analysis of Fig. 3.23, assuming an ideal CFDITA yields the expressions of the impedance of both the circuits as follows:

$$\left.\frac{V_{in}}{I_i}\right|_{\text{Fig 3(a)}} = Z_{in}|_{(a)} = \frac{1}{sC(2+g_mR)} = \frac{1}{sC_{eq1}} \tag{3.5}$$

[2]A. Raj, M. Shrivastava, D. R. Bhaskar, and P. Kumar, "Enhancement of multiplication factor of capacitor using single current follower differential input transconductance amplifier," International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 37, no. 4, e3279, 2024.

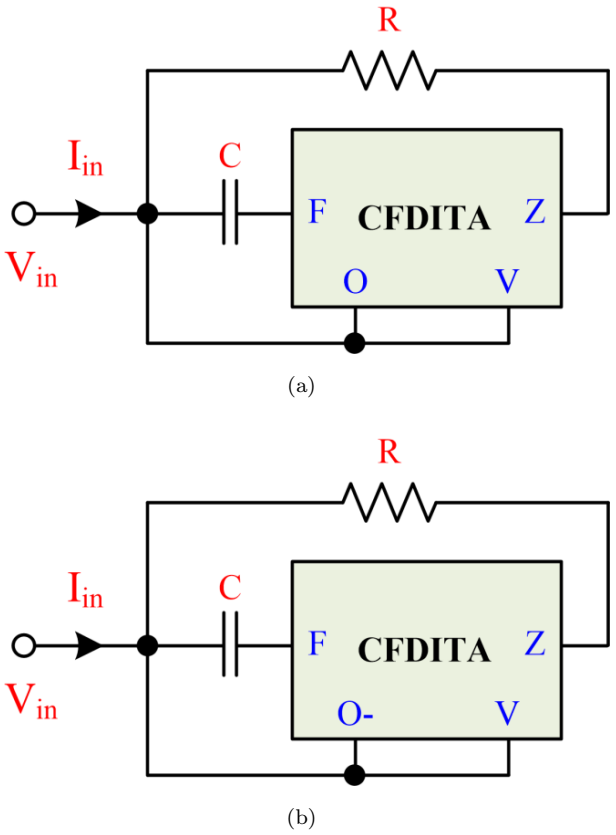


Figure 3.23: Proposed lossless grounded capacitance multiplier circuits

$$\left.\frac{V_{in}}{I_i}\right|_{\text{Fig 3(b)}} = Z_{in}|_{(b)} = \frac{1}{sC(2-g_mR)} = \frac{-1}{sC_{eq2}} \tag{3.6}$$

where

$$C_{eq1} = C(2+g_mR) \; and \; C_{eq2} = C(2-g_mR) \tag{3.7}$$

From equation (3.5), we can conclude that the equivalent capacitance (C_{eq1}) of the circuit in Fig. 3.23 (a) yields a positive capacitance multiplication factor (MF) of (2 + g_mR). Similarly, equation (3.6) demonstrates that the MF for the circuit in Fig. 3.23 (b) can be either positive or negative. It can provide a positive multiplication factor of up to 2 and a negative MF if the value of g_mR greatly exceeds 2. In both the circuits, the MF can be independently and electronically adjusted using the transconductor of the CFDITA and by varying resistor R, within the constraints of the CFDITA. A notable feature of the circuits in Fig. 3.23 is its ability to function

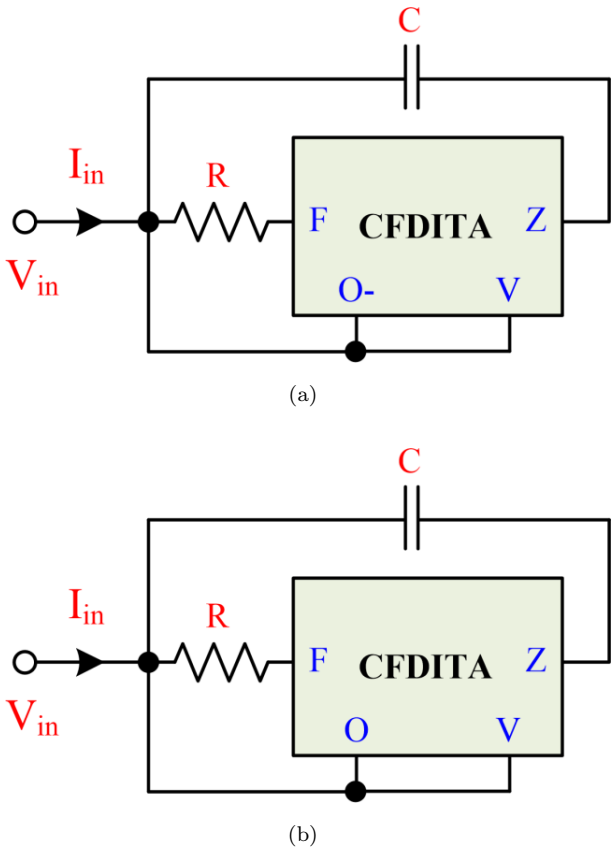


Figure 3.24: Proposed lossy parallel-type RL simulator circuits

as a parallel RL simulator circuits when the passive components are interchanged using RC:CR transformation. The modified circuit's implementation is depicted in Fig. 3.24. Assuming ideal CFDITA, routine analysis of parallel lossy RL circuits of Fig. 3.24 yield the following input admittance:

$$\left.\frac{I_{in}}{V_{in}}\right|_{\text{Fig 4(a)}} = Y_{in} = \frac{1}{Z_{in}} = \frac{2}{R} + \frac{g_m}{sCR} = \frac{1}{R_{eq}} + \frac{1}{sL_{eq}} \tag{3.8}$$

$$\left.\frac{I_{in}}{V_{in}}\right|_{\text{Fig 4(b)}} = Y_{in} = \frac{1}{Z_{in}} = \left(\frac{2}{R} - \frac{g_m}{sCR}\right) = \frac{1}{R_{eq}} - \frac{1}{sL_{eq}} \tag{3.9}$$

The expressions for admittance obtained in equations (3.8) and (3.9), it is worth noting that the inductance achieved in the proposed lossy inductance simulator circuits is independently tunable through the transconductance of the CFDITA.

This tunability can be further controlled electronically by adjusting the bias current. Additionally, the resistor employed in both circuits is effectively grounded, given that the voltage at terminal F of the CFDITA is zero. This can be further replaced with its MOS counterparts, making it highly suitable for IC integration.

3.3.1 Non-ideal Analysis

The non-ideal gains of the CFDITA are considered, and the terminal characteristics are modified as provided in equation (3.10) for the evaluation of the input impedance of the proposed circuits.

$$\begin{bmatrix} I_r \\ I_z \\ V_F \\ I_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha & 0 \\ 0 & 0 & 0 & 0 \\ -\beta g_m & \beta g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_r \\ V_z \\ I_F \\ V_o \end{bmatrix} \tag{3.10}$$

where α and β are non-ideal current and transconductance gains.

The input impedance of the circuits shown in Fig. 3.23 and Fig. 3.24, accounting for non-ideal gains, can be expressed as:

$$\left(\frac{V_{in}}{I_{in}}\right)'\Big|_{\text{Fig 3.23 (a)}} = \frac{1}{sC(1+\alpha+\alpha\beta g_m R)} \tag{3.11}$$

$$\left(\frac{V_{in}}{I_{in}}\right)'\Big|_{\text{Fig 3.23 (b)}} = \frac{1}{sC(1+\alpha-\alpha\beta g_m R)} \tag{3.12}$$

$$\left(\frac{I_{in}}{V_{in}}\right)'\Big|_{\text{Fig 3.24 (a)}} = \frac{\alpha+1}{R} + \frac{g_m\alpha\beta}{sCR} \tag{3.13}$$

$$\left(\frac{I_{in}}{V_{in}}\right)'\Big|_{\text{Fig 3.24 (b)}} = \frac{\alpha+1}{R} - \frac{g_m\alpha\beta}{sCR} \tag{3.14}$$

It is noteworthy from equations (3.11) to (3.14) that the non-ideal gain significantly impacts the impedance and admittance of both the GCM and parallel inductance simulator circuits, leading to deviations from unity, especially at higher frequencies. Consequently, the equivalent and inductance values experience notable alterations in the higher frequency range. We quantitatively assessed these changes, deriving approximate values for α and β as 0.96 and 0.98, respectively. Upon substituting these values into equations (3.11) to (3.14), we observed that the non-ideal expressions closely approximate the ideal values.

3.3.2 Simulation Results

To validate the performances of the proposed capacitance multiplier and lossy parallel RL simulator circuits, CMOS CFDITA shown in Fig. 3.7 has been used. D.C. power supply voltages for the CFDITA were chosen as V_{DD} = -V_{SS} = 1.32V and the bias voltage V_{BIAS} was set to -0.7V. The bias voltages V_{BIAS} and V_{BB} were set to -0.78V and 0.7V respectively to ensure that the transconductance of CFDITA would be 4.6mS. Simulation results have been provided to analyze frequency and phase responses, time responses of input voltage and current, Monte-Carlo simulation results, and process-corner-voltage-temperature effects. The simulated frequency responses of magnitude and phase of the lossless capacitance circuit alongwith the theoretical evaluations are demonstrated in Fig. 3.25 for which g_m was set to 4.6mS and that includes a capacitor and resistor of values 10pF and 100kΩ respectively.

The results depicted in Fig. 3.25 clearly demonstrate that the impedance and phase characteristics of the proposed CM closely align with the theoretical values across a broad frequency range spanning from 0.1 Hz to 100 MHz and 1Hz to 2MHz respectively. The transient responses of input voltage and current are demonstrated in Fig.

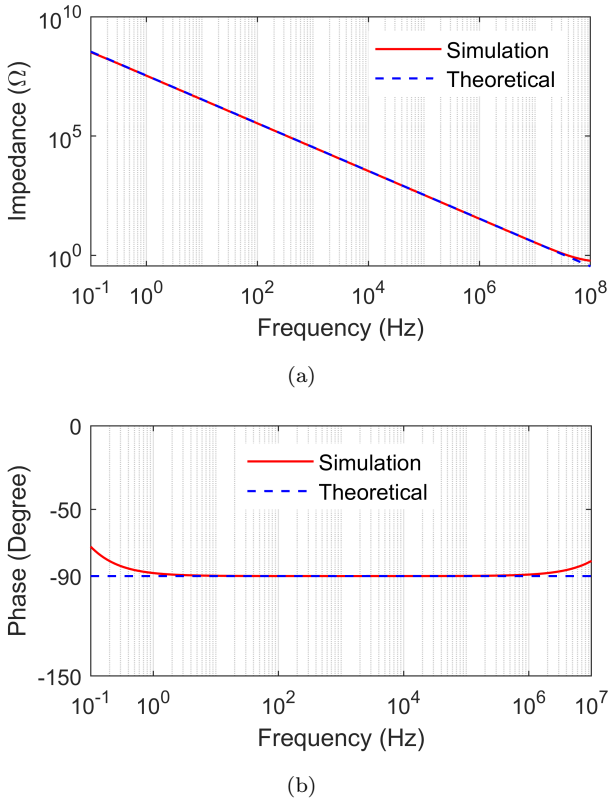


Figure 3.25: Simulated magnitude and phase of the impedance of CM circuit along with theoretical evaluations

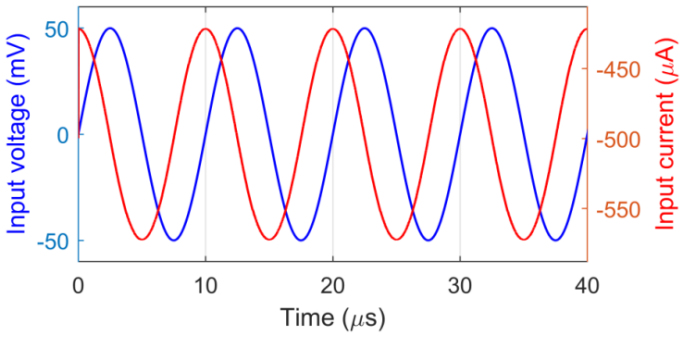
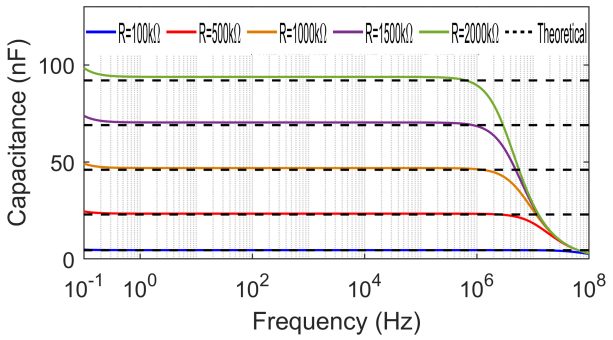
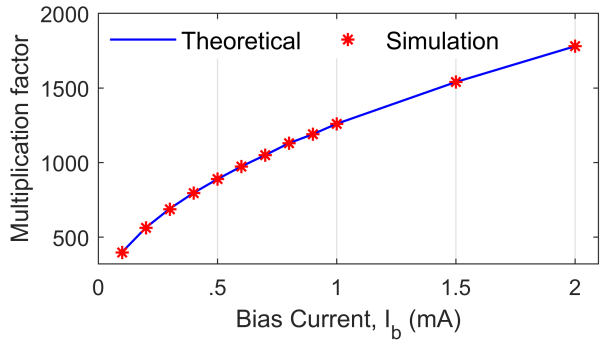


Figure 3.26: Transient input voltage and current of CM circuit at 100kHz

3.26 for which a sinusoidal input voltage of magnitude 100mV at 100 kHz is applied. The variation in capacitance of the circuits shown in Fig. 3.23 was also examined by repeatedly measuring transient and frequency responses. The value of resistor R was altered from 100kΩ to 2MΩ and this adjustment resulted in capacitance values ranging from 4.6nF to 92.02nF while maintaining a constant g_m of 4.6mS. The



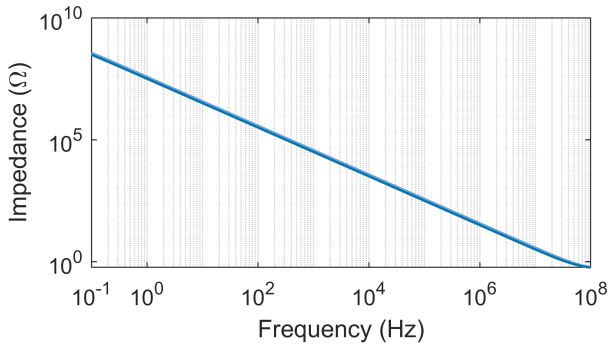
(a)



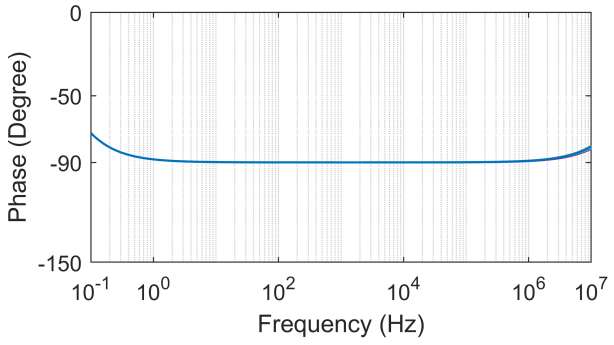
(b)

Figure 3.27: (a) Variation in capacitance with Resistor R (b) Variation in MF with I_{Bias}

frequency responses of capacitance have been shown in Fig. 3.27 (a). Furthermore, with variation in transconductance (g_m) of the CFDITA results into variation in MF upto 1800 and the corresponding results are illustrated in Fig. 3.27 (b). The results shown in Fig. 3.27 indicate that the simulated capacitance obtained through the proposed circuit is in good agreement with the theoretical values. Monte-Carlo simulations were performed on the proposed capacitance multiplier circuits to test their robustness. The simulations involved applying uniform deviations of 10% in resistance with 200 samples. The frequency responses of magnitude and phase and histogram results of maximum capacitance by varying resistor R are displayed in Fig. 3.28(a) – Fig. 3.28(c) respectively. Temperature analysis has also been performed on the proposed circuit to assess its performance under different temperature conditions. The simulation results of magnitude and phase under different temperatures



(a)



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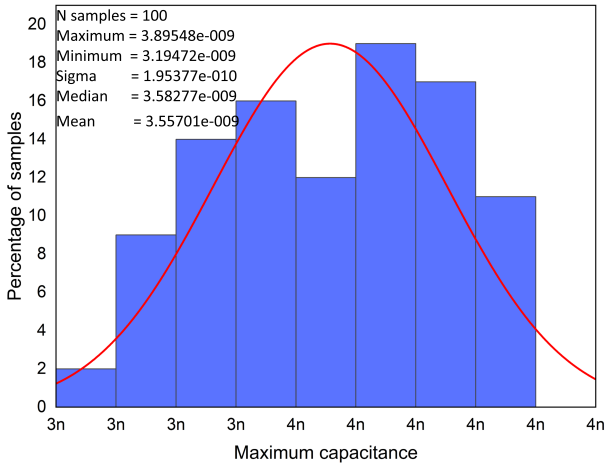


(c)

Figure 3.28: Monte-Carlo results (a) Magnitude (b) Phase (c) Histogram

are shown in Fig. 3.29 .

Based on the results depicted in Fig. 3.29 , it is apparent that the magnitude and phase of the impedance have a negligible impact upto 100°C temperature. Similar analyses were conducted for the proposed lossy parallel simulator circuit, and the

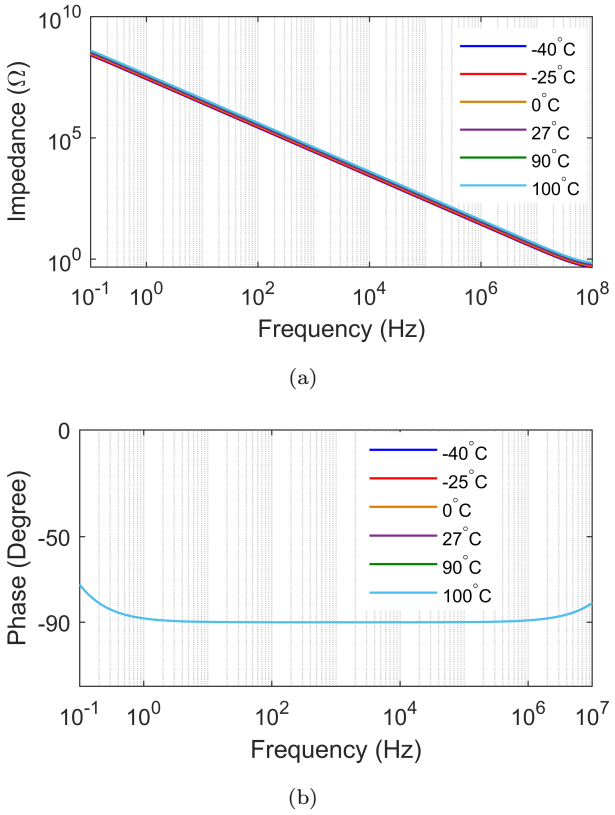
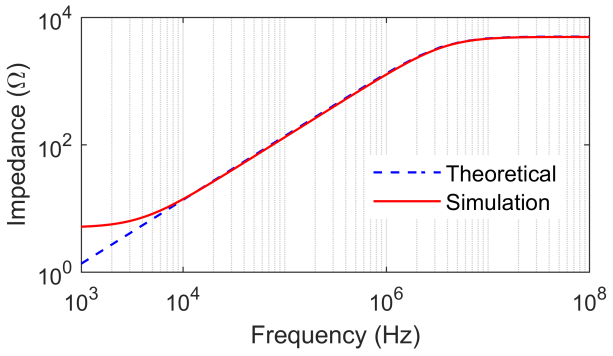
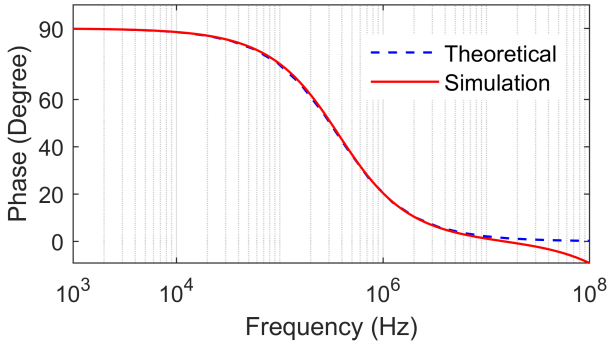


Figure 3.29: Simulated (a) magnitude and (b) phase responses of CM circuit under different temperatures

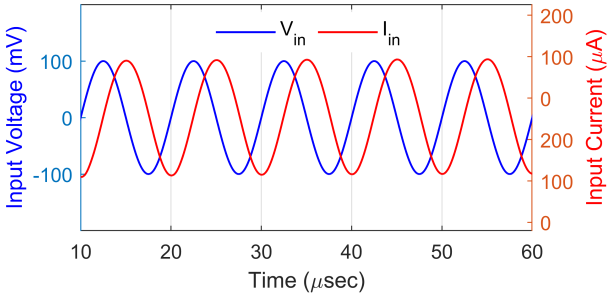
corresponding results are showcased in Fig. 3.30 . The transconductance g_m was set to 4.56mS and the passive elements selected for the results were R = 10kΩ and C = 100pF. For the obtainment of transient responses, a sinusoidal voltage of magnitude 100mV at a frequency of 100kHz was applied to the input of the circuit and the simulated input voltage and current are displayed in Fig. 3.30(c). From the results shown in Fig. 3.30(a) and (b), it is observed that the magnitude of the parallel RL circuit closely matches the theoretical predictions within the frequency range of 8 kHz to 100 MHz whereas the phase of the simulator is in good agreement with the theoretical values in the frequency range of 1kHz – 10MHz. To evaluate and compare the overall performance of the proposed GCM circuit, the figure of merit (FoM) for the GCMs is expressed as in [206]:



(a)



(b)



(c)

Figure 3.30: Simulated frequency and transient responses of the proposed parallel RL circuit (a) Magnitude responses (b) Phase responses (c) Input voltage and current

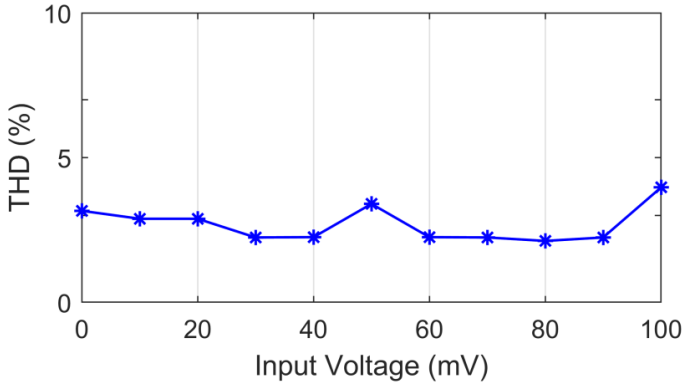


Figure 3.31: Variation in THD with input voltage

$$FoM_{GCM} = \frac{K \cdot BW}{P_{dis}} = \frac{K(f_2 - f_1)}{P_{dis}} \tag{3.15}$$

where = Total quiescent power dissipation of the circuit, K = Multiplication factor and BW = Bandwidth over which the quality factor of capacitor has a value $|Q|>$ 10. The FoM for the GCM circuit was evaluated with C = 10pF, K = 9202, BW approximately equal to 1MHz, and the value was found to be 147kHz/µW. The simulations were also conducted to analyze the total harmonic distortions of the proposed circuit, and the variation of THD with input voltage has been depicted in Fig. 3.31. From Fig. 3.31, it is observed that the maximum THD is 4% when the input voltage varies between 10mV and 100mV. The simulations results shown in Fig. 3.25 to Fig. 3.31 validate the performance of the proposed capacitance multiplier and lossy inductance simulator circuits and demonstrate their robustness under varying conditions.

3.3.3 Experimental Results

The workability of the presented CM circuits has also been validated experimentally using CFDITA implemented with off-the-shelf ICs AD844 and LM13700. The complete structure of experimental schematic of the circuit of Fig. 3.23(a) using AD844

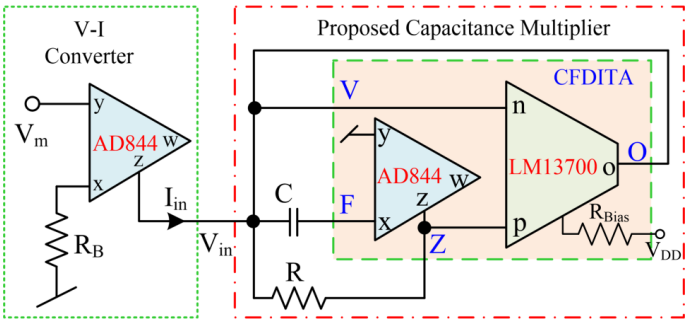
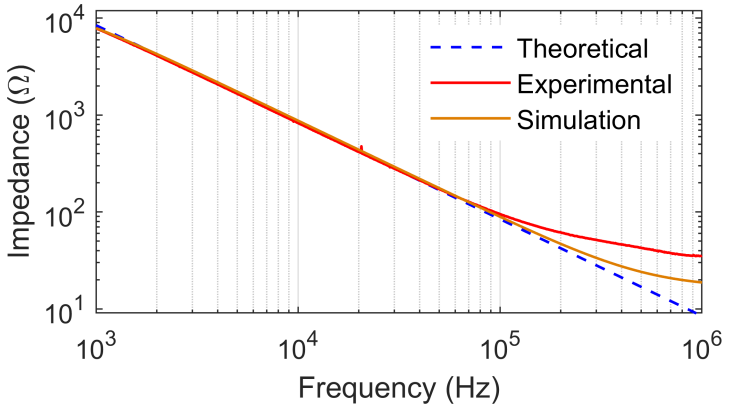


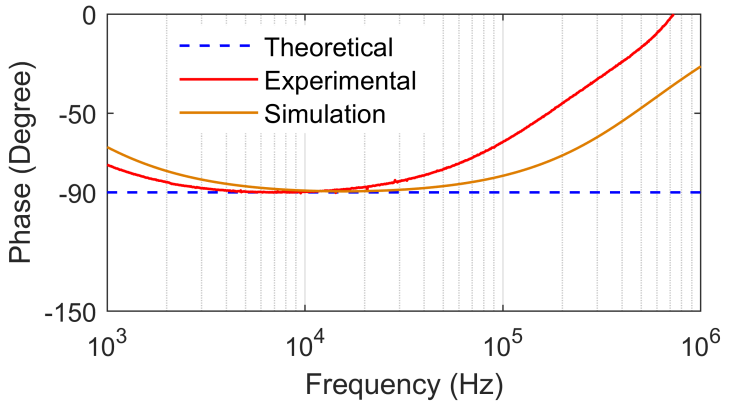
Figure 3.32: Schematic of proposed CM circuit using off-the-shelf ICs

and LM13700 is presented in Fig. 3.32. The ICs AD844 and LM13700 used in Fig. 3.32 were biased with power supply voltages of ± 12V. The passive components in the experimental verification circuit were selected as R = 10kΩ, C = 1nF, R_B = 2.2kΩ and the value of transconductance g_m was set to 5.5mS (for R_{Bias} = 100kΩ) using the formula given in [207] resulting an equivalent capacitance value of 57nF. The experimental frequency responses of magnitude and phase of the proposed circuit are shown in Fig. 3.33(a-b), while the transient responses to a sinusoidal input voltage of 1V peak-to-peak at 1.5 kHz are displayed in Fig. 3.33(c). From Fig. 3.33(a), it is seen that the experimental magnitude response of the capacitance multiplier aligns with the simulated and theoretical responses within the frequency range of 1kHz to 100kHz. Fig. 3.33(b) illustrates that the theoretical phase response remains constant at –90°, while both the simulated and experimental plots show deviation at higher frequencies. This variation arises from the non-idealities of the active building block and parasitic effects.

The derived parallel RL circuit was tested experimentally using passive component values of R = 10kΩ, R_{Bias} = 100kΩ, and C = 1nF. The obtained frequency responses of impedance and phase, as well as the macro model of AD844 and theoretical evaluations, are illustrated in Fig. 3.34(a)–(b). Additionally, Fig. 3.34(c) showcases time-domain results with a sinusoidal input voltage of magnitude 2V at a frequency of 100kHz for further validation. The experimental results depicted in Fig. 3.34(a)



(a)



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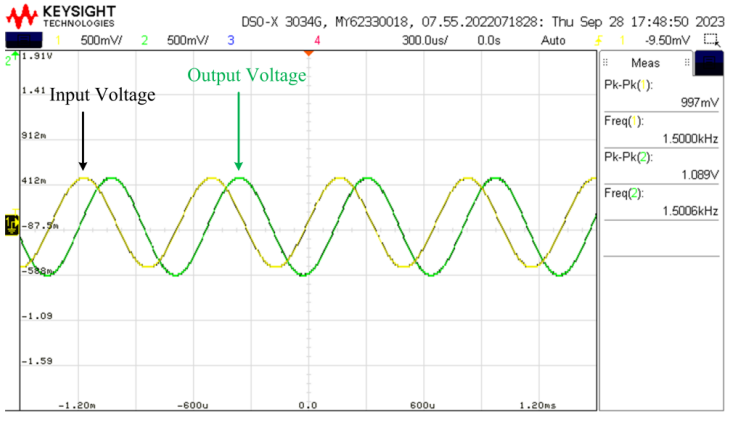
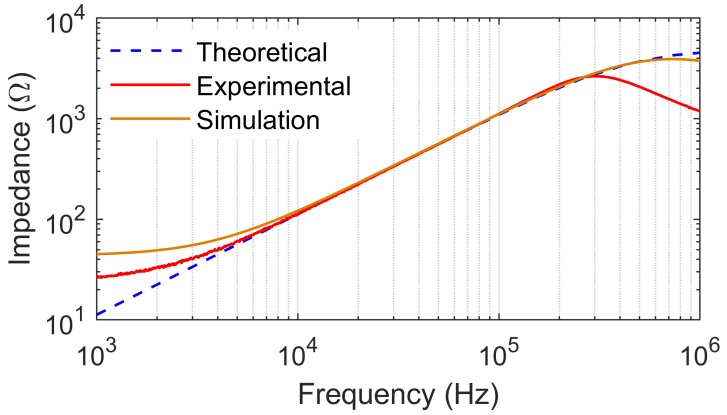
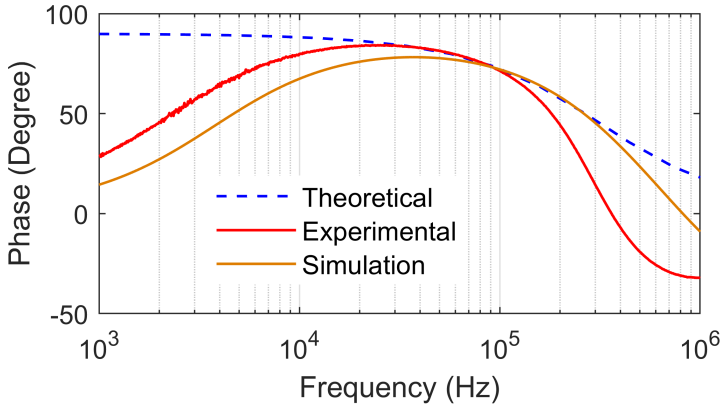


(c)

Figure 3.33: Experimentally obtained magnitude, phase and time domain results for CM circuit



(a)



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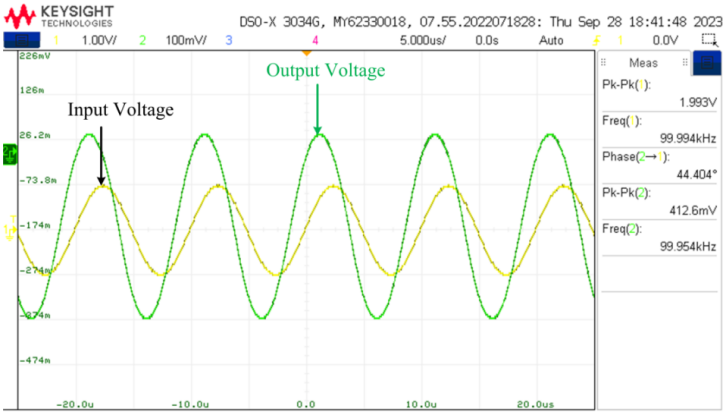


(c)

Figure 3.34: Experimentally obtained frequency and transient responses of parallel RL simulator

indicate that the experimentally obtained frequency responses of the magnitude of the lossy inductor align with the simulated and theoretical results within the frequency range of 5kHz to 300kHz. From the results illustrated in Fig. 3.34(b), it is seen that the phase between input and output voltages is approximately 44.4°. The simulated and experimental phase responses deviate from the theoretical one due to practical nonidealities. Simulation shows slight phase lag at higher frequencies, while the experimental response exhibits a larger deviation owing to additional parasitics and component tolerances in the hardware setup.

3.3.4 Application examples

As an application, the proposed positive capacitance multiplier and parallel RL simulator were used to design first-order low-pass filter and second-order high-pass filter respectively whose circuit models and their active realizations using the proposed simulators are illustrated in Fig. 3.35 amd Fig. 3.36 respectively.

Assuming ideal CFDITA, the transfer functions of the circuits shown in Fig. 3.35 and Fig. 3.36 can be expressed as:

LPF:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+sC_{eq}R_A} = \frac{1}{1+sC(2+g_mR)R_A} \tag{3.16}$$

HPF:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2L_{eq}R_{eq}C_A}{s^2L_{eq}R_{eq}C_A+sL_{eq}+R_{eq}} = \frac{s^2CC_AR^2}{s^2CC_AR^2+2sCR+g_mR} \tag{3.17}$$

The performances of the derived low-pass and high-pass filters were experimentally validated for a nominal frequency of 110kHz using the following passive component values: For LPF: R = 2.2kΩ, C = 100pF, R_A=1kΩ, R_{Bias} = 100kΩ for g_m=5.6mS For

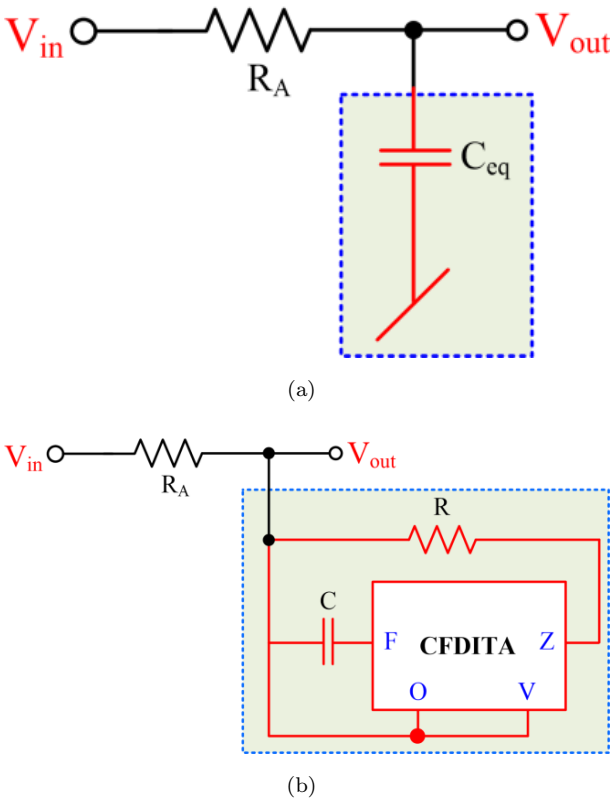


Figure 3.35: Application example of proposed capacitance multiplier as first order low pass filter (a) circuit model (b) Implementation using CFDITA

HPF: R = 1MΩ, C = C_A = 100pF, R_{Bias} = 100kΩ for g_m=5.6mS The experimentally obtained frequency responses of gain and phase of the LPF and HPF are displayed in Fig. 3.37 and Fig. 3.38respectively.

The simulation and experimental results shown in Fig. 3.25 – Fig. 3.38, thus, validate the effectiveness of the proposed capacitance multiplier and parallel lossy RL simulator circuits.

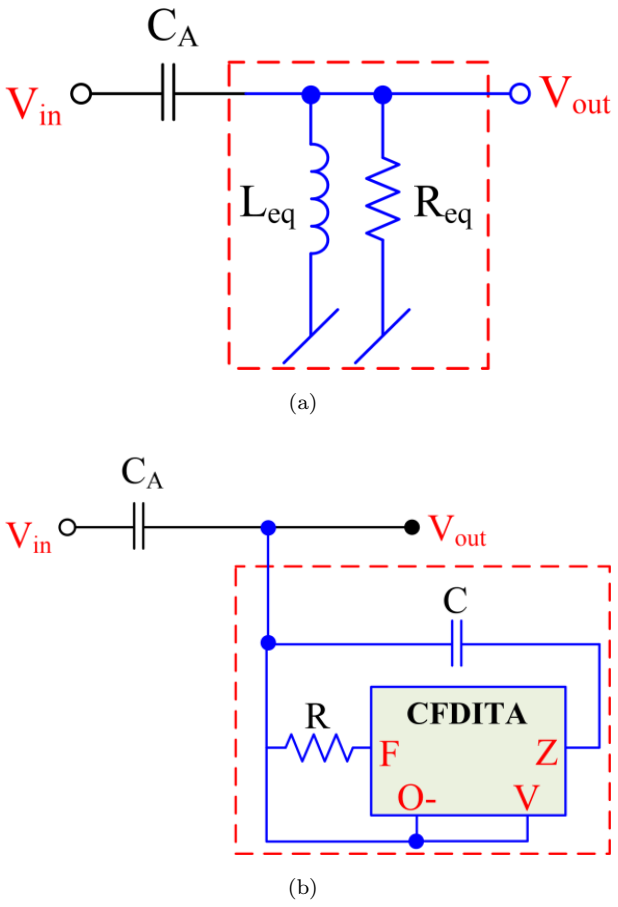


Figure 3.36: Application example of proposed capacitance multiplier as second order high pass filter (a) circuit model (b) Realization using CFDITA

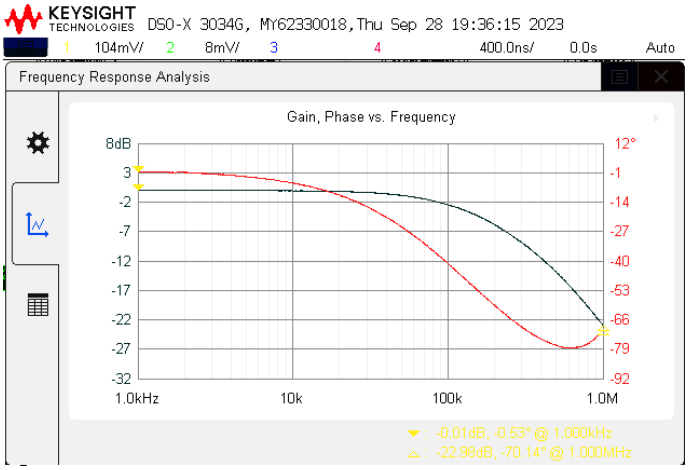


Figure 3.37: Experimentally obtained frequency response of first order LPF shown in Fig. 3.35

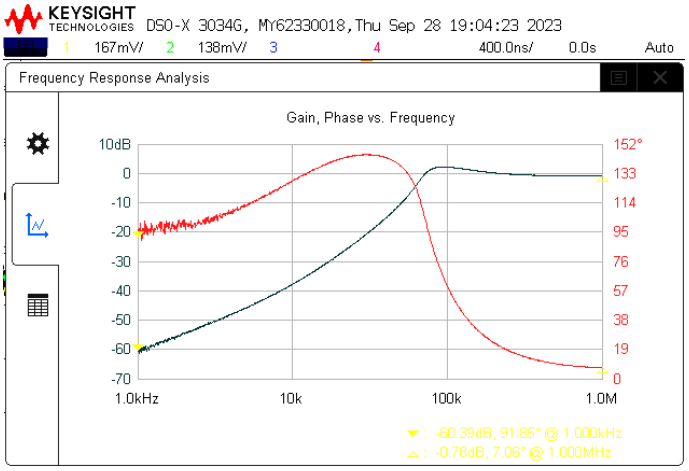


Figure 3.38: Experimentally obtained frequency response of second order HPF shown in Fig. 3.36

3.4 Concluding remarks

A lossy capacitance multiplier circuit using a CFDITA, one resistor and one capacitor (virtually grounded) has been presented in this Chapter. The proposed circuit offers independent control over the multiplication factor (up to 7102) without requiring passive component matching. Non-ideal analysis of the presented circuit has been carried out using non-ideal model of CFDITA. The performance of the proposed circuit has been verified through simulations results using a 0.18µm TSMC technology CMOS CFDITA. Pre-layout and post-layout results have also been appended. The results were further validated through experiments with commercially available ICs AD844 and LM13700.

Two novel capacitance multiplier circuits capable of providing positive and negative multiplication factors have been presented in this Chapter. Both the circuits utilize a single CFDITA, one resistor, and one virtually grounded capacitor. These circuits enable electronic enhancement of the capacitor's value by up to 1800 times its original magnitude. Additionally, the capacitance multiplication factor can be independently adjusted to reach values of up to 9202 by manipulating the resistor

independently. Furthermore, the adaptability of these circuits extends to the implementation of parallel RL simulators, allowing for independent control of inductance in the derived circuits. The chapter also includes practical application examples that highlight the versatility of these proposed circuits. To validate their performance, SPICE simulations and experimental tests were conducted, both of which exhibited good agreement with the theoretical predictions.

Chapter 4

VCII-based Immittance Simulator Circuits

4.1 Introduction

This Chapter deals with realisation of immittance simulator circuits using second generation voltage conveyor (VCII). VCII based series and parallel immittance simulator circuits have been proposed in this Chapter. Synthetic series and parallel immittance simulators are vital for designing and synthesizing active networks, playing a crucial role in tasks such as active ladder design and filter realization. These simulators are essential for tasks like active filters, sinusoidal oscillators, parasitic cancellation, compensators, and impedance matching circuits [208]. Consequently, various approaches for active simulation of immittances have been suggested in the literature. These simulators can be implemented as grounded and floating types, incorporating both lossless and lossy configurations. The circuits simulated by grounded immittance can offer a range of functions, including lossless inductor and capacitor

circuits, series/parallel RL, series/parallel RC circuits, frequency-dependent positive/negative resistors, as well as series/parallel CD circuits.

VCII has recently gained significant attention from researchers owing to its straightforward circuit-level integration, higher operating frequency range, minimal power consumption, compact chip area, and the presence of both high as well as low-impedance current output/voltage input terminals. VCIIs emerge as optimal selections for circuits featuring voltage-derived outputs. The ease with which VCII facilitates the subtraction and addition of current signals is attributed to its low-impedance input terminal [67]. In addition to the conventional VCII structures, improved low-voltage VCII structure have also been reported in [209] [210]. As this chapter focuses on VCII based grounded immittance simulator circuits realised with two VCIIs, it is beneficial to provide a brief overview of previously reported grounded immittance simulator circuits designed with VCIIs.

Several VCII-based grounded capacitance multipliers [154] [155] [156] [157] [158] [160], grounded inductor simulator [68], floating inductance simulator [159], grounded frequency dependent negative resistance (FDNR)/ frequency dependent negative conductance (FDNC) and series RL/ parallel RL [67] have been presented.

In [154], three positive and one negative lossless grounded capacitance multipliers (GCMs) were presented as shown in Fig. 4.1 All of these GCMs were constructed utilizing two VCIIs, one capacitor, and two resistors. Passive component matching was unnecessary for the implementation of a GCM. The multiplication factor of GCMs can be adjusted by altering the values of two resistances as needed.
A single EVCII+ based positive CM circuit has been presented in [155] wherein only one passive component has been used which is a floating capacitor as displayed in Fig. 4.2. The same circuit can provide negative multiplication factor by replacing EVCII+ with EVCII-.

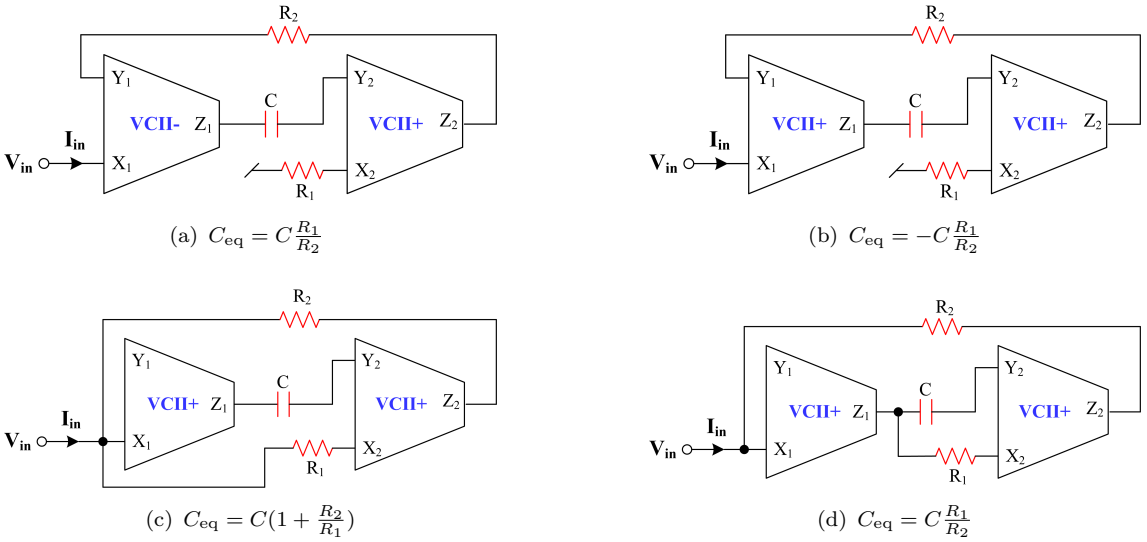


Figure 4.1: Lossless grounded capacitance multiplier circuits proposed in[154]

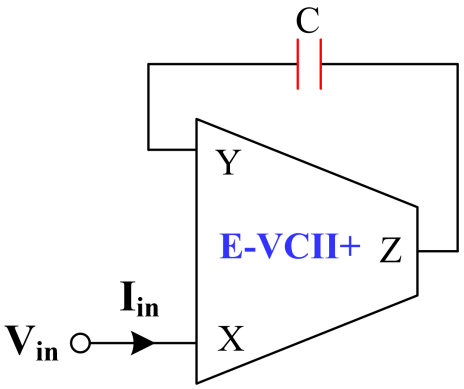
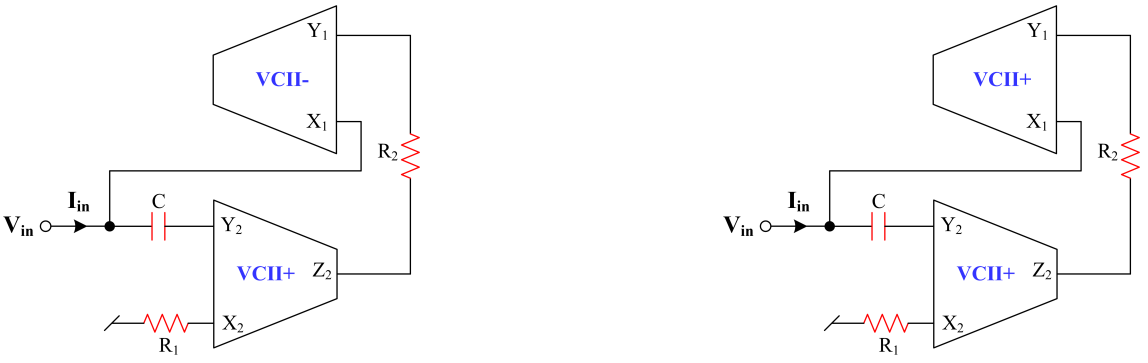


Figure 4.2: VCII based grounded CM circuit with positive multiplication factor proposed in [155], $C_{eq} = KC$

In [156], a novel implementation of a grounded capacitance multiplier employing two VCIIs, two resistors, and one grounded capacitor has been proposed as shown in Fig. 4.3. This circuit can generate multiplication factors ranging from -50 to +50.

Resistor-free floating positive/negative capacitance multiplier circuits design employs one dual-output VCII and one electronically adjustable differential voltage



(a) $C_{\text{eq}} = C(1 + \frac{R_1}{R_2})$ (b) $C_{\text{eq}} = C(1 - \frac{R_1}{R_2})$

Figure 4.3: VCII-based grounded capacitive multiplier circuit proposed in [156] with (a) positive multiplication factor (b) negative multiplication factor

(a) $C_{\text{eq}} = KC$ (b) $C_{\text{eq}} = -KC$

Figure 4.4: (a) Floating positive capacitive multiplier circuit proposed in [157] (b) Floating negative capacitive multiplier circuit proposed in [157]

current conveyor (E-DVCC) as active building blocks (ABBs), together with a single grounded capacitor have been reported in [157] shown in Fig. 4.4 The simulated capacitance value is regulated by a control voltage V_C, which governs the current gain between the X and Z terminals of the E-DVCC. The circuit does not consist of any matching conditions.

In [158], a novel CMOS tunable active inductor simulator (AIS) for both positive and negative configurations, together with a positive capacitance and resistance multiplier and a negative capacitance and resistance simulator have been introduced. The proposed designs employ a single modified VCII ±, one grounded capacitor, and two resistors as shown in Fig. 4.5.

(a) $Z_{in} = \frac{Z_1 Z_3}{Z_2}$ (b) $Z_{in} = -\frac{Z_1 Z_3}{Z_2}$

Figure 4.5: (a) Positive impedance simulator circuit proposed in [158] (b) Negative impedance simulator circuit proposed in [158]

A grounded inductor simulator using the VCII has been proposed in [68]. The proposed inductor simulator uses two VCIIs, two resistors, and one grounded capacitor, making it ideal for integration. Importantly, this simulator lacks restrictive matching constraints as shown in Fig. 4.6

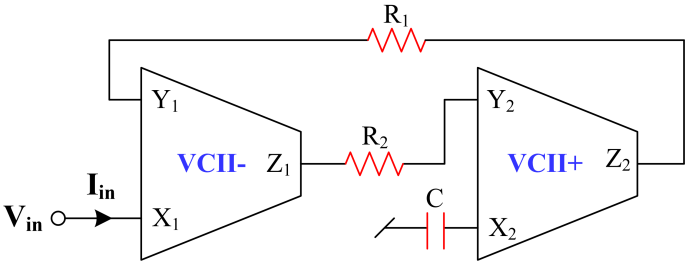


Figure 4.6: VCII-based simulated grounded inductor proposed in [68], $L_{eq} = CR_1R_2$

An electronically tunable resistor-less floating inductance simulator implemented using VCII has been proposed in [159]. The proposed circuit utilizing the intrinsic resistors at the Y terminals of the VCIIs has three VCIIs and a grounded capacitor. A control current is used to adjust the simulated inductance by varying the impedance at the Y terminal of the VCII. In [67],a grounded frequency-dependent negative resistor (FDNR) and a frequency-dependent negative conductance (FDNC) have been proposed as shown in Fig. 4.7 Furthermore, two lossy parallel and series R-L inductor simulators have been developed. The FDNR necessitates two VCII, two capacitors, and one grounded resistor. FDNC is executed utilizing three VCII, three

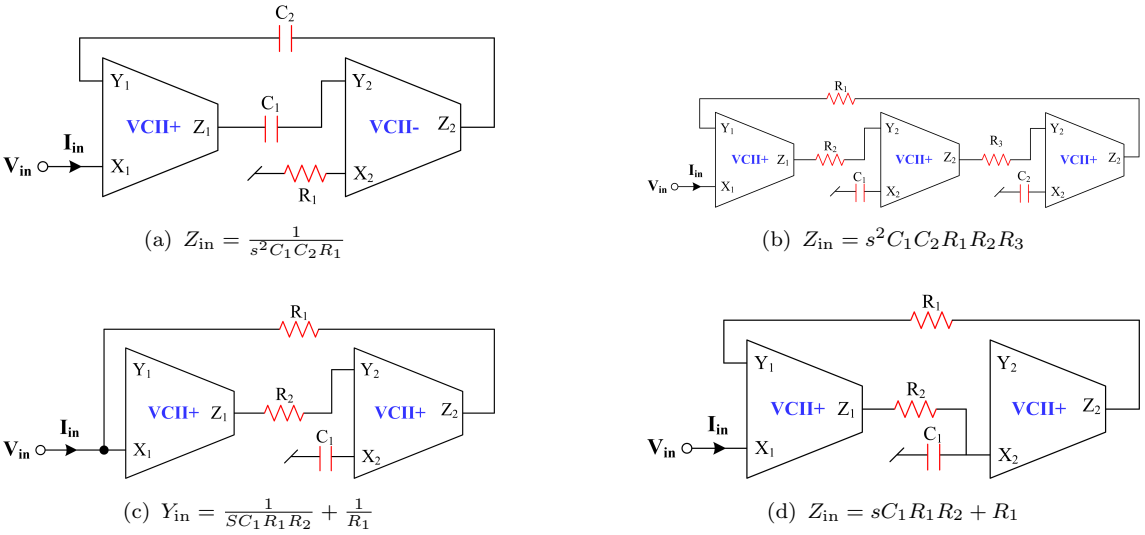


Figure 4.7: (a) FDNR (b) FDNC (c) Parallel R-L (d) Series R-L proposed in [67]

resistors, and two grounded capacitors. The R-L inductor emulators necessitate two VCII, two resistors, and one grounded capacitor. All the exhibited immittance simulators do not necessitate any form of passive component matching. In view of the above literature, it appears that no two-VCII-based immittance simulator circuit has been presented (employing intrinsic property of VCII) yet that can provide series/parallel RL, series/parallel RC, series/parallel CD and capacitance divider/-multiplier using three passive elements without any passive component matching condition(s). To address this research gap, this chapter introduces four novel generalized topologies for grounded series/parallel immittance simulator circuits that utilize only two VCIIs and three impedances, all without requiring any matching conditions to realize series/parallel RL, series/parallel RC, series/parallel CD, and capacitance divider/multiplier configurations.

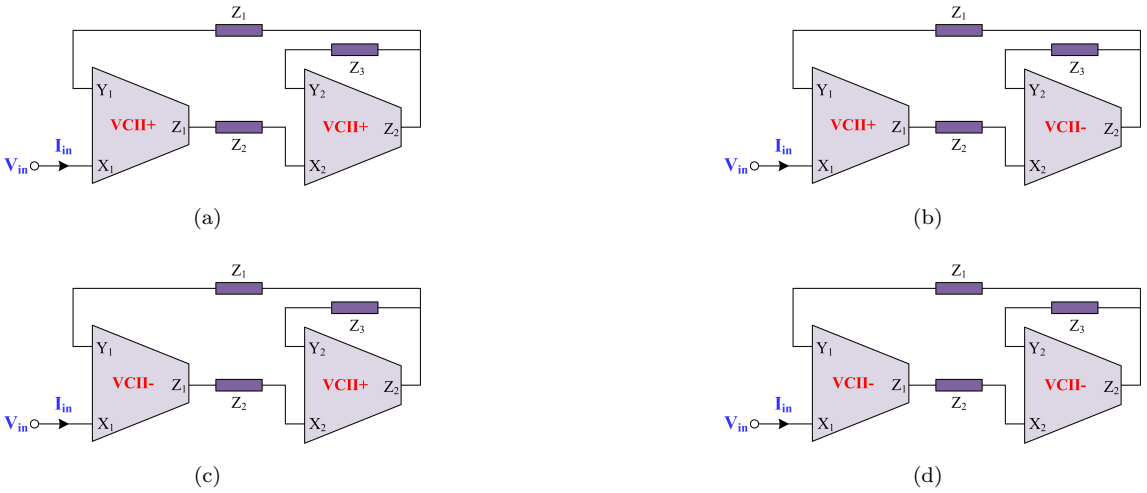


Figure 4.8: Proposed generalized grounded series immittance simulators

4.2 Grounded series type immittance simulators using VCII

In this section, four generalized configurations of grounded series-type immittance simulators are proposed. The presented circuits realize series R-L, series R-C, and series C-D simulators using only two second-generation voltage conveyors (VCII±) as active elements in conjunction with three impedances, without requiring any matching conditions which are displayed in Fig. 4.8[1].

The relationships between port currents and voltages of VCII± are given by: $I_x = \pm I_y$, $V_z = V_x$ and $V_y = 0$, a routine analysis of the circuits of Fig. 4.8 using the port voltage-current relationships of VCII, yields the following impedance equations:

$$\text{Circuit 1:} \quad \frac{V_{in}}{I_{in}} = Z_{in} = Z_1\left(1 + \frac{Z_2}{Z_3}\right) \tag{4.1}$$

$$\text{Circuit 2:} \quad \frac{V_{in}}{I_{in}} = Z_{in} = Z_1\left(1 - \frac{Z_2}{Z_3}\right) \tag{4.2}$$

[1]M. Shrivastava, D. R. Bhaskar, and P. Kumar, "VCII-Based Generalized Configurations for Grounded Series-type Immittance Simulators," Journal of Circuits, Systems and Computers, 2025.

$$\text{Circuit 3:} \quad \frac{V_{in}}{I_{in}} = Z_{in} = -Z_1\left(1 + \frac{Z_2}{Z_3}\right) \tag{4.3}$$

$$\text{Circuit 4:} \quad \frac{V_{in}}{I_{in}} = Z_{in} = -Z_1\left(1 - \frac{Z_2}{Z_3}\right) \tag{4.4}$$

Proper choices of impedances, Z_1, Z_2, and Z_3 substituted into equations (4.1) – (4.4), lead to various types of series immittance simulators, including grounded series R-L, grounded series R-C and grounded series C-D. The realizations of these circuits are detailed in Table 4.1. From Table 4.1, it is noted that the proposed circuits are

Table 4.1: Generalized Table for Circuits and Realization Types

Circuit	**Impedance Choices**	**Input Impedance (Z_{in})**	**Realization Type**
1	$Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3$	$R_1 + sR_1R_2C_3 = R_{eq} + sL_{eq}$	Series R-L
	$Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3$	$R_1 + \frac{R_1}{sC_2R_3} = R_{eq} + \frac{1}{sC_{eq}}$	Series R-C
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$\frac{1}{sC_1} + \frac{1}{s^2C_1C_2R_3} = \frac{1}{sC_{eq}} + \frac{1}{s^2D_{eq}}$	Series C-D
	$Z_1 = \frac{1}{sC_1}, Z_2 = R_2, Z_3 = R_3$	$\frac{1}{sC_1}\left(1 + \frac{R_2}{R_3}\right) = \frac{1}{sC_{eq}}$	Cap. divider
2	$Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3$	$R_1 - sR_1R_2C_3 = R_{eq} - sL_{eq}$	Series R-(-L)
	$Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3$	$R_1 - \frac{R_1}{sC_2R_3} = R_{eq} - \frac{1}{sC_{eq}}$	Series R-(-C)
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$\frac{1}{sC_1} - \frac{1}{s^2C_1C_2R_3} = \frac{1}{sC_{eq}} - \frac{1}{s^2D_{eq}}$	Series C-(-D)
3	$Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3$	$-R_1 - sR_1R_2C_3 = -R_{eq} - sL_{eq}$	Series (-R)-(-L)
	$Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3$	$-R_1 - \frac{R_1}{sC_2R_3} = -R_{eq} - \frac{1}{sC_{eq}}$	Series (-R)-(-C)
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$\frac{1}{sC_1} - \frac{1}{s^2C_1C_2R_3} = -\frac{1}{sC_{eq}} - \frac{1}{s^2D_{eq}}$	Series (-C)-(-D)
4	$Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3$	$-R_1 + sR_1R_2C_3 = -R_{eq} + sL_{eq}$	Series (-R)-L
	$Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3$	$-R_1 + \frac{R_1}{sC_2R_3} = -R_{eq} + \frac{1}{sC_{eq}}$	Series (-R)-C
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$-\frac{1}{sC_1} + \frac{1}{s^2C_1C_2R_3} = -\frac{1}{sC_{eq}} + \frac{1}{s^2D_{eq}}$	Series (-C)-D

capable to provide various grounded impedance simulators such as series R-L, series R-C, series C-D, and a capacitance divider with appropriate choices of impedances.

4.2.1 Non-ideal analysis

The effect of the non-ideal gains of the VCIIs on the circuits presented in Fig. 4.8 has been assessed using the terminal characteristic equations: $I_X = \pm\beta_i I_Y$, $V_Z = \alpha_i V_X$, and $V_Y = 0$, where i = 1-2, indicates number of VCII±. The non-ideal voltage and current gains cause changes in the realization of the immittance circuits. To investigate the impact of tracking errors, a re-analysis of the proposed immittance circuits has been conducted, and the modified impedance values are provided in equations (4.5) – (4.8).

$$\text{Circuit 1:} \quad \frac{V_{\text{in}}}{I_{\text{in}}} = Z_1\left(\frac{1}{\beta_1\alpha_1\alpha_2} + \frac{\beta_2 Z_2}{\beta_1\alpha_1 Z_3}\right) \tag{4.5}$$

$$\text{Circuit 2:} \quad \frac{V_{\text{in}}}{I_{\text{in}}} = Z_1\left(\frac{1}{\beta_1\alpha_1\alpha_2} - \frac{\beta_2 Z_2}{\beta_1\alpha_1 Z_3}\right) \tag{4.6}$$

$$\text{Circuit 3:} \quad \frac{V_{\text{in}}}{I_{\text{in}}} = -Z_1\left(\frac{1}{\beta_1\alpha_1\alpha_2} + \frac{\beta_2 Z_2}{\beta_1\alpha_1 Z_3}\right) \tag{4.7}$$

$$\text{Circuit 4:} \quad \frac{V_{\text{in}}}{I_{\text{in}}} = -Z_1\left(\frac{1}{\beta_1\alpha_1\alpha_2} - \frac{\beta_2 Z_2}{\beta_1\alpha_1 Z_3}\right) \tag{4.8}$$

From equations (4.5) – (4.8), it is observed that the effect of non-ideal gains on the impedance values is insignificant and the expressions approach the ideal expressions when the values of these gains approach unity.

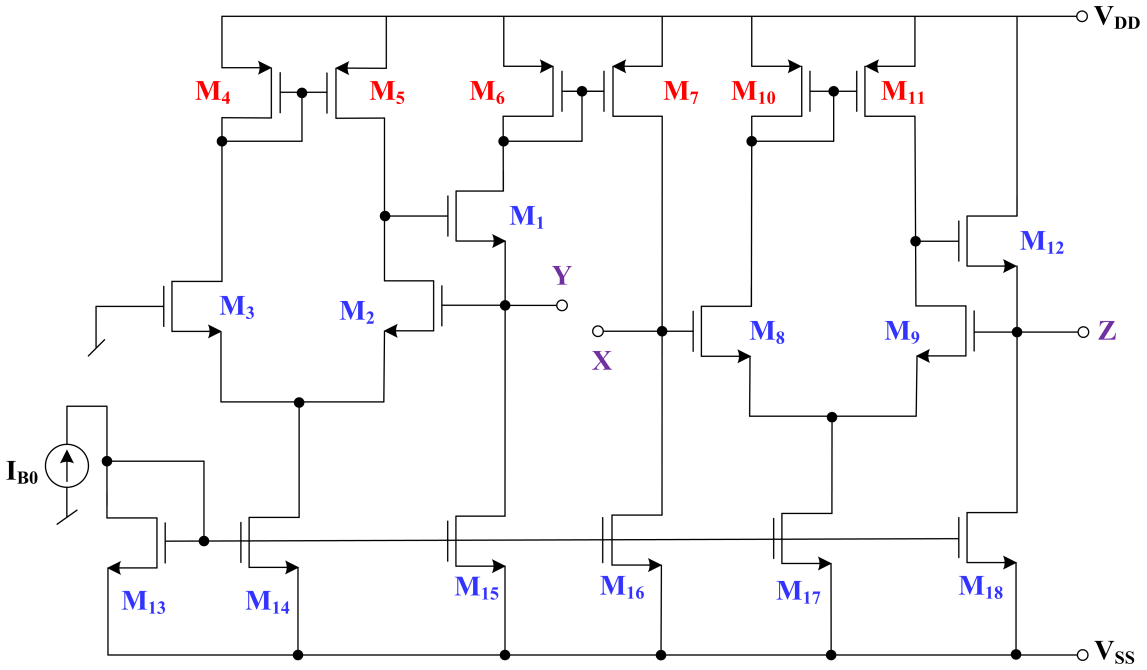
4.2.2 PSPICE simulation results using CMOS VCIIs

To verify the functionality of the proposed grounded series immittance simulator circuits, we utilized CMOS VCII+ and VCII-, implementing them with 0.18µm TSMC technology parameters, as depicted in Fig. 4.9. The aspect ratios of the PMOS and NMOS transistors used in Fig. 4.9 are 40.5µm/0.54µm and 13.5µm/0.54µm, respectively. The DC power supply voltages used for biasing the VCII+ and VCII- were ±0.9V, and the biasing currents I_{B0} and I_{B1} were chosen as 25µA. The validation of all the proposed immittance simulator circuits shown in Fig. 4.8 included various analyses, such as magnitude and phase responses of impedance, time-domain responses of input voltage and current, as well as Monte-Carlo analysis.

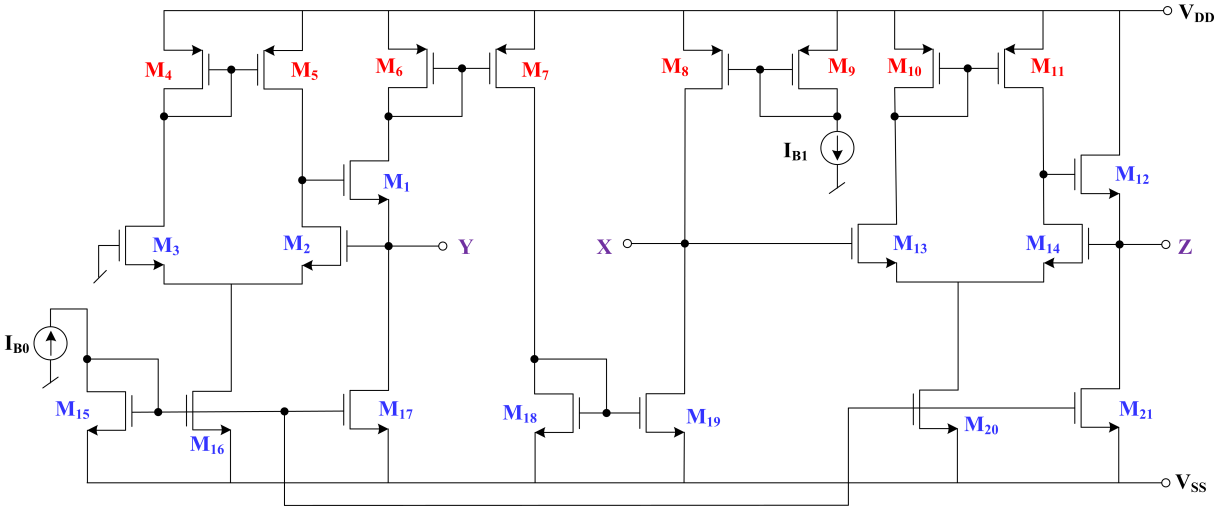
4.2.2.1 Results for Circuit-1

For the simulation of the series R-L simulator, we selected the following passive component values: $R_1 = 1\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, and capacitor $C_3 = 100\text{pF}$. These values resulted in equivalent resistance (R_{eq}) and equivalent inductance (L_{eq}) values of 1kΩ and 10mH, respectively. The simulated frequency responses of impedance and phase, along with theoretical evaluations, are displayed in Fig. 4.10. To further explore the characteristics of the series R-L circuits, we varied the value of resistor R_2, considering values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ. The corresponding variations in impedance and phase are presented in Fig. 4.11.

From Fig. 4.10, the simulated frequency response of impedance and phase of series RL circuit of Fig. 4.8(Circuit-1) are in proper accordance with the theoretical propositions up to a frequency of 1MHz for both impedance and phase response. The proposed series R-L simulator was also subjected to Monte-Carlo analysis. In this

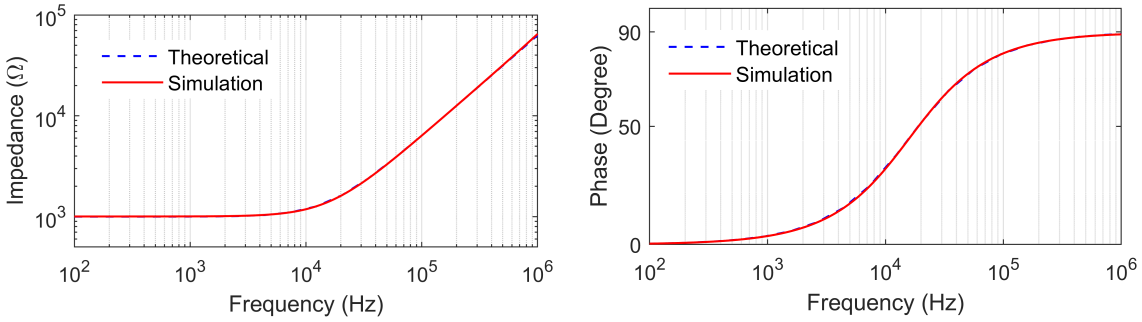


(a)



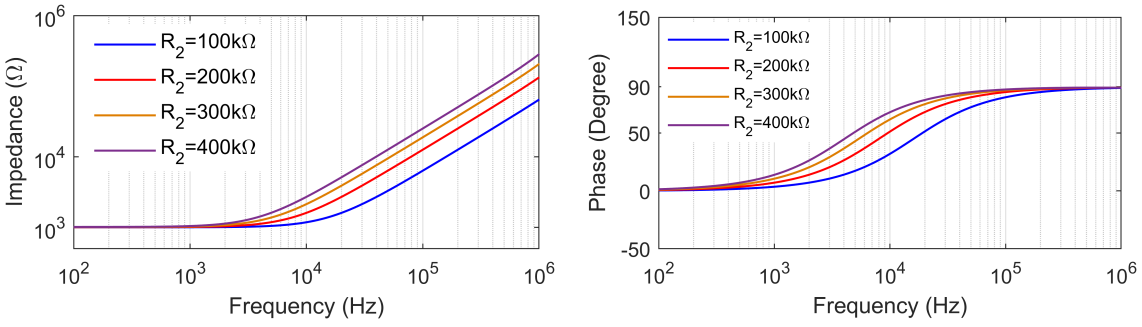
(b)

Figure 4.9: CMOS structure [68] of (a) VCII+ and (b) VCII-



(a) (b)

Figure 4.10: Frequency responses of series R-L simulator (a) impedance and (b) phase



(a) (b)

Figure 4.11: Frequency responses of series R-L simulator for different values of R_2 (a) magnitude (b) phase

analysis, a 10% deviation was introduced to resistor R_2, and the resultant magnitude and phase results are depicted in Fig. 4.12. Additionally, Fig. 4.13 illustrates the transient responses of input voltage and current for the series R-L simulator, where a sinusoidal voltage with amplitude of 100mV and a frequency of 100 kHz was applied.

Simulation results for the series R-C circuit in Fig. 4.8(Circuit-1) were conducted using the following passive component values: $R_1 = 1\text{k}\Omega$, $R_3 = 100\text{k}\Omega$, and $C_2 = 100\text{pF}$, which resulted in equivalent resistance and equivalent capacitance (C_{eq}) values of 1kΩ and 10nF, respectively. The magnitude and phase responses are displayed in Fig. 4.14. To further explore the characteristics of the series R-C circuit, we varied the value of resistor R_3, considering values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ.

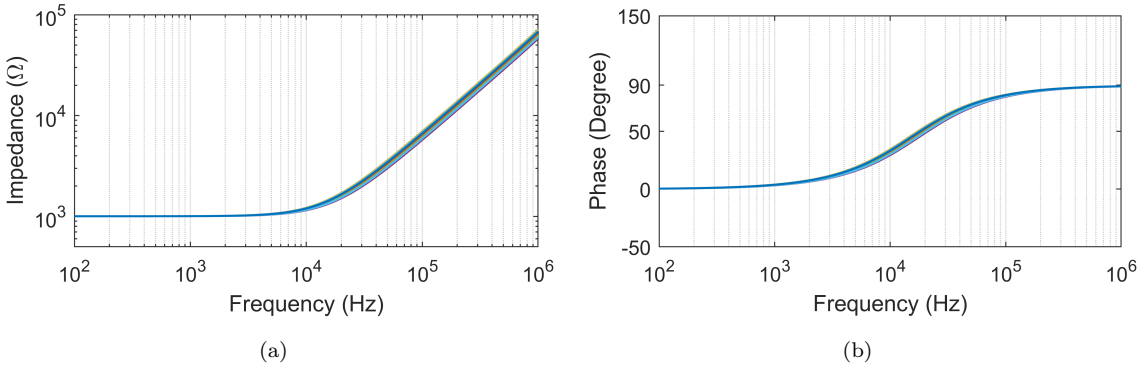


Figure 4.12: AC Monte-Carlo results of series R-L simulator (a) magnitude responses (b) Phase responses

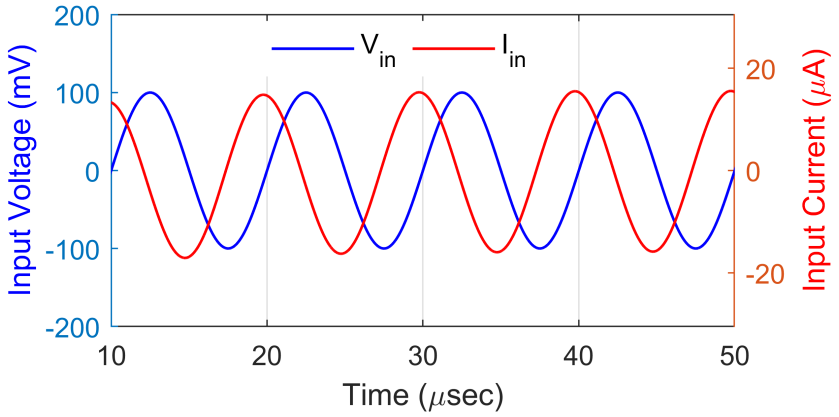
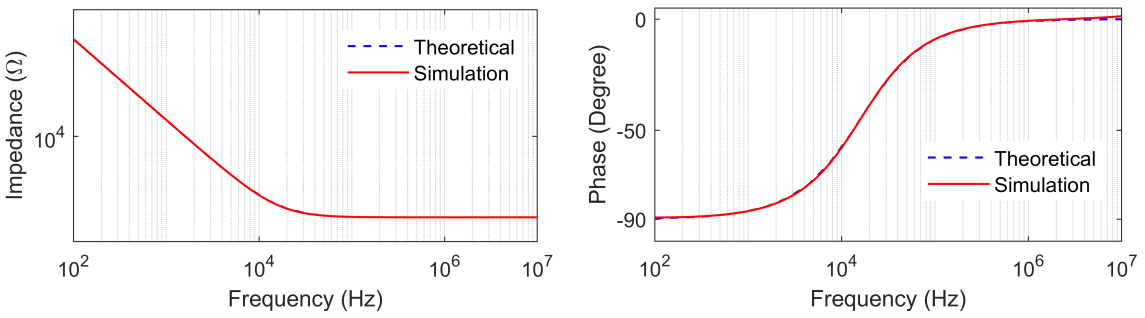


Figure 4.13: Transient responses of input voltage and current of series R-L simulator

The corresponding variations in impedance and phase responses are depicted in Fig. 4.15.

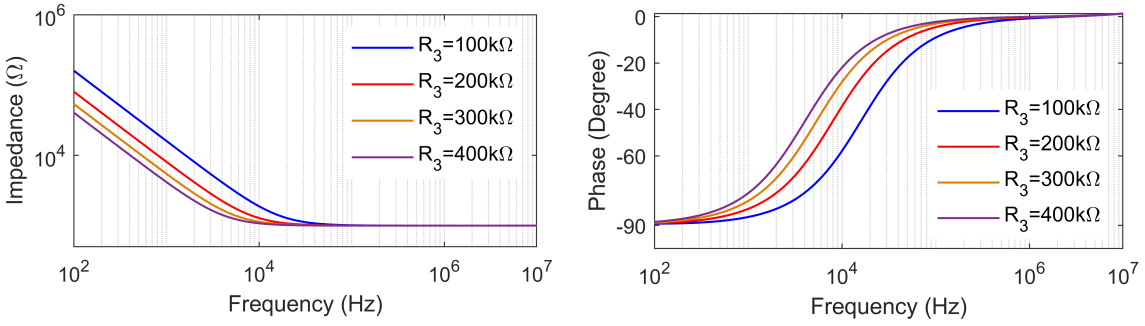
From Fig. 4.14, it can be observed that the simulated impedance and phase responses match the theoretical values upto 10MHz. The simulated magnitude and phase responses of the series R-C simulator, as obtained from the Monte-Carlo analysis, are presented in Fig. 4.16. For the time-domain analysis, a sinusoidal input voltage with a magnitude of 100mV and a frequency of 10kHz was applied, and the corresponding input voltage and current waveforms are illustrated in Fig. 4.17.

To validate the functionality of the proposed series C-D circuit of Fig. 4.8 (Circuit-1), the frequency responses of impedance magnitude and phase were measured using



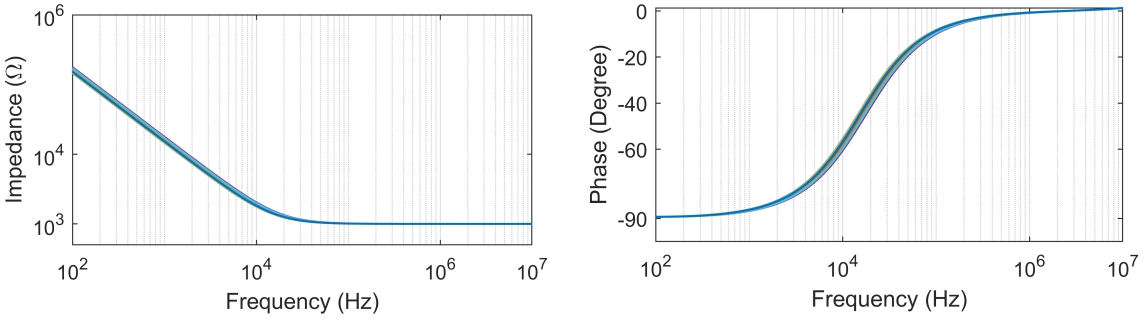
(a) (b)

Figure 4.14: Frequency responses of series R-C simulator (a) impedance and (b) phase



(a) (b)

Figure 4.15: Frequency responses of series R-C simulator for different value of resistors (a) magnitude (b) phase



(a) (b)

Figure 4.16: AC Monte-Carlo results of series R-C simulator (a) magnitude responses (b) Phase responses

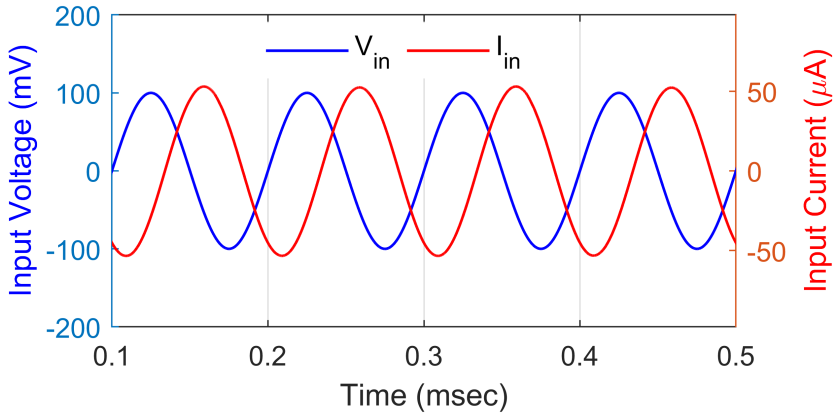
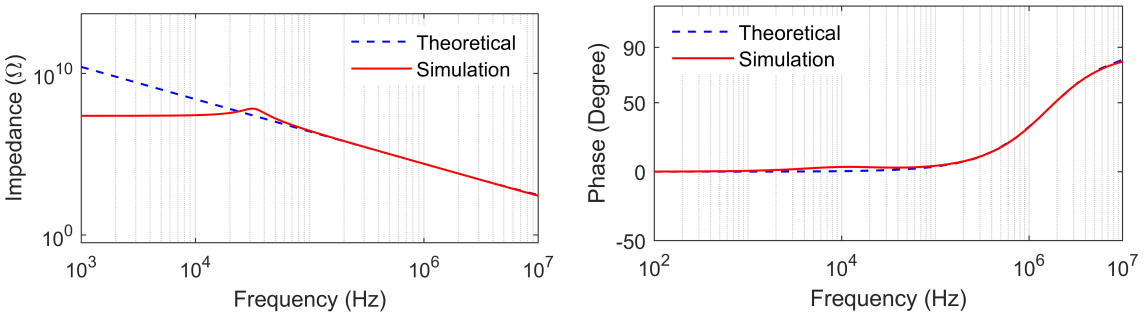


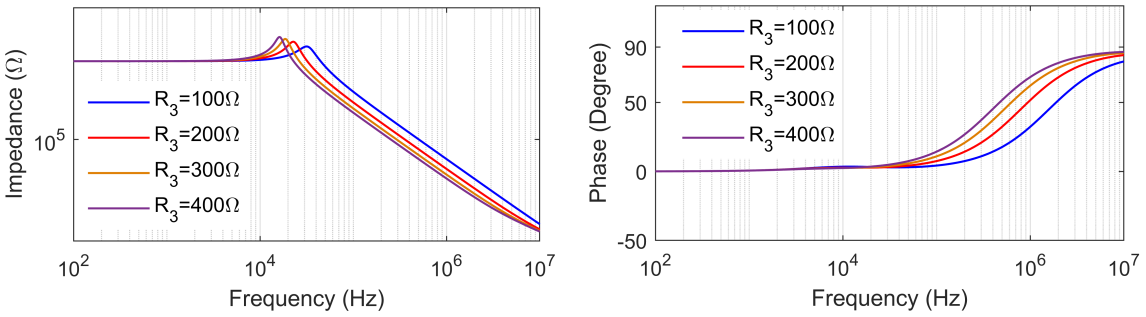
Figure 4.17: Transient responses of input voltage and current for series R-C simulator



(a) (b)

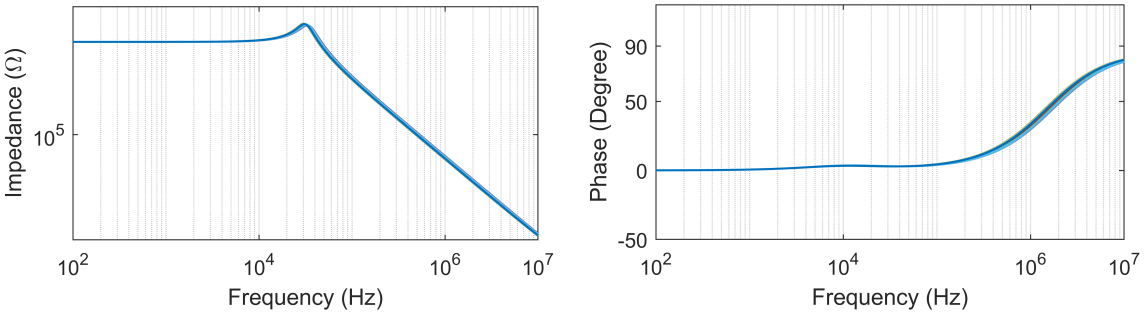
Figure 4.18: Frequency responses (a) impedance and (b) phase of the series C-D simulator of Circuit-1

C_1 = 100pF, C_2 = 100pF, and R_3 = 100Ω. These responses are displayed in Fig. 4.18. Furthermore, variations in impedance magnitude and phase for different resistor values (100Ω, 200Ω, 300Ω, 400Ω) are illustrated in Fig. 4.19. From Fig. 4.18, it can be observed that the simulated impedance matches with the theoretical values within the frequency range of 30kHz to 10MHz, while the phase matches between 100Hz to 10MHz. Monte-Carlo analysis has also been performed and the corresponding results are shown in Fig. 4.20. Transient responses of input voltage and current are also performed for a sinusoidal input voltage of magnitude 10mV at a frequency of 100kHz for C_1 = 100pF, C_2 = 100pF, and R_3 = 100Ω has been shown in Fig. 4.21.



(a) (b)

Figure 4.19: Frequency responses of (a) magnitude (b) phase of series C-D simulator at different value of resistors



(a) (b)

Figure 4.20: AC Monte-Carlo results of series C-D simulator (a) magnitude responses (b) Phase responses

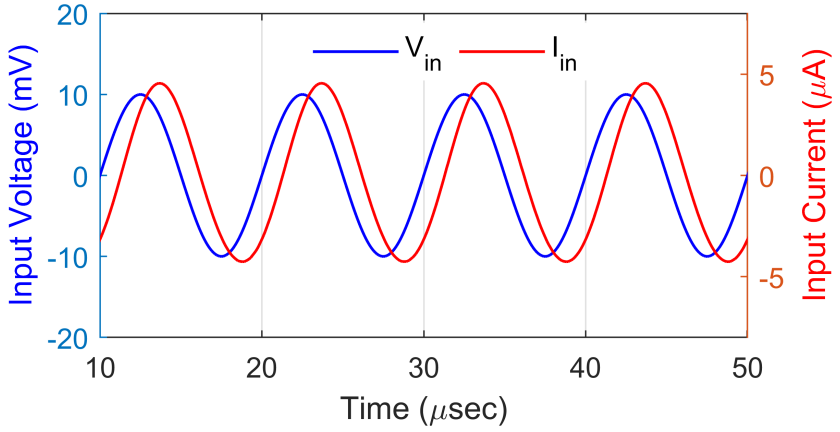
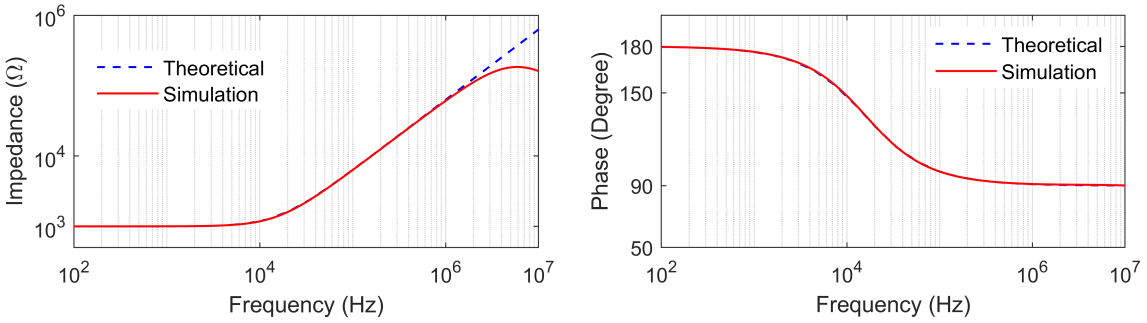
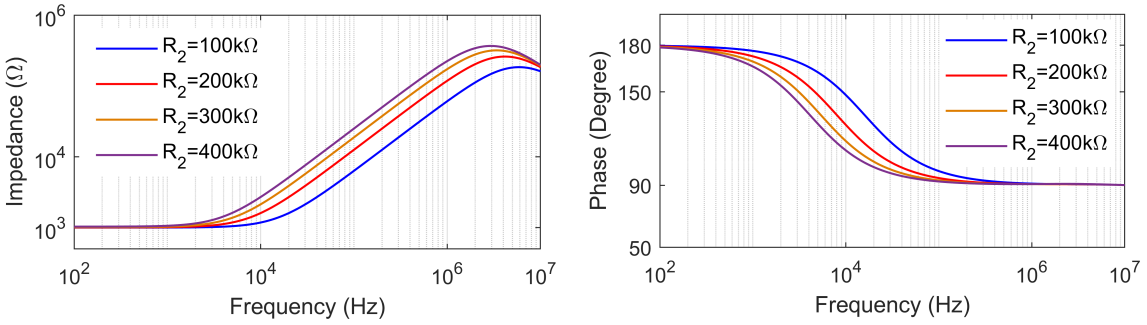


Figure 4.21: Transient responses of input voltage and current for series C-D simulator of Circuit-1



(a) (b)

Figure 4.22: Frequency responses of series R-L simulator of Circuit-2 (a) impedance and (b) phase



(a) (b)

Figure 4.23: Frequency responses of series R-L simulator of Circuit-2 for different values of R_2 (a) magnitude (b) phase

4.2.2.2 Results for Circuit-2

We choose the following values for the passive components in the series R-L simulator of Fig. 4.8 (Circuit-2) simulation: R_1 = 1kΩ, R_2 = 100kΩ, and capacitor C_3 = 100pF. Equivalent resistance (R_{eq}) and equivalent inductance (L_{eq}) of 1kΩ and 10mH, respectively, were obtained from these values. Fig. 4.22 shows the simulated impedance and phase frequency responses as well as theoretical analyses. In an effort to investigate the properties of the series R-L circuits even more, we tested the resistor R_2, taking values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ into consideration. Fig. 4.23 shows the associated changes in impedance and phase.

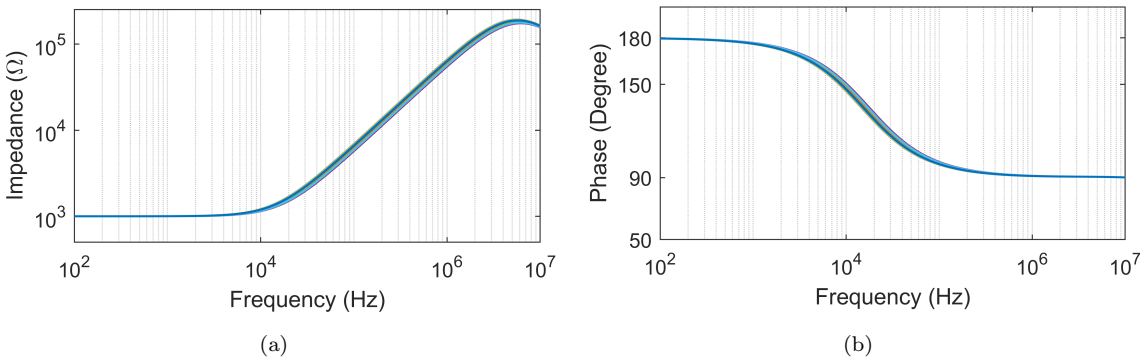


Figure 4.24: AC Monte-Carlo results of series R-L simulator of Circuit-2 (a) magnitude responses (b) Phase responses

The simulated impedance and phase responses of the series RL circuit of Circuit-2 shown in Fig. 4.22 are in good agreement with the theoretical values up to a frequency of 1MHz for impedance response and 10MHz for phase response. Monte-Carlo analysis has also been performed. The magnitude and phase findings of resistor R_2 after a 10% variation was applied in this analysis are shown in Fig. 4.24. Furthermore, Fig. 4.25 shows the transient responses of the input voltage and current for the series R-L simulator, to which a 100 kHz frequency and 100 mV amplitude sinusoidal voltage were applied.

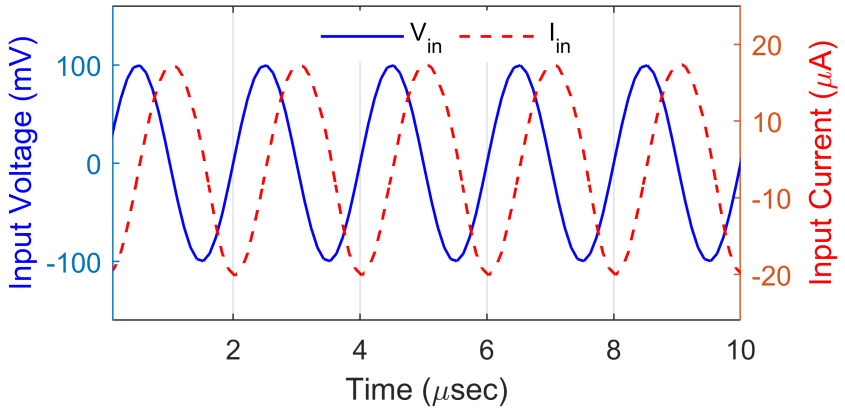
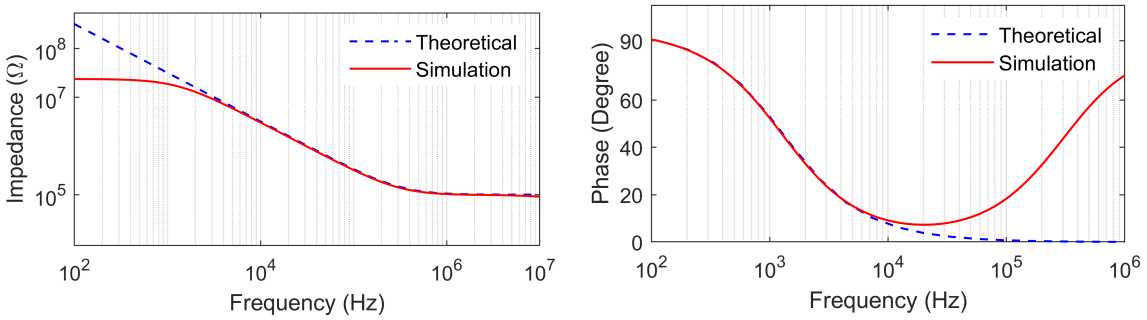


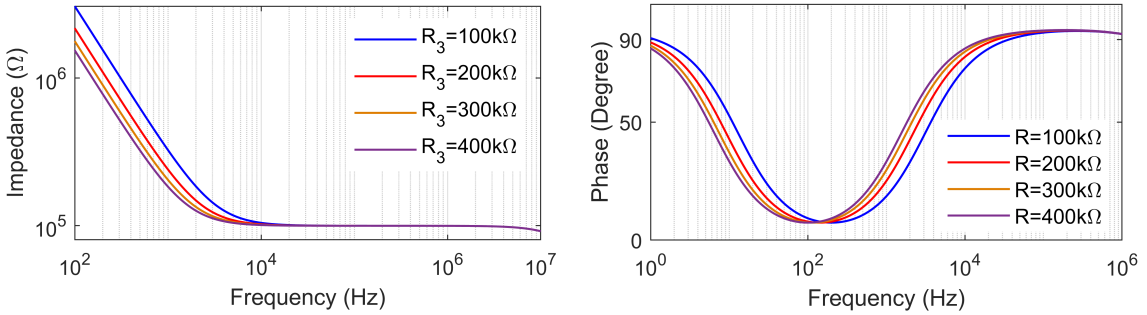
Figure 4.25: Transient responses of input voltage and current of series R-L simulator of Circuit-2

The simulation results for the series R-C circuit in Fig. 4.8 (Circuit-2) were obtained using the following passive component values: $R_1 = 100\text{k}\Omega$, $R_3 = 100\text{k}\Omega$, and $C_2 =$



(a) (b)

Figure 4.26: Frequency responses of series R-C simulator of Circuit-2 (a) impedance and (b) phase



(a) (b)

Figure 4.27: Frequency responses of series R-C simulator of Circuit-2 for different value of resistors (a) magnitude (b) phase

100pF. The magnitude and phase responses are shown in Fig. 4.26. To further examine the behavior of the series R-C circuit, we varied the value of resistor R_3, using values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ. The resulting changes in impedance and phase responses are illustrated in Fig. 4.27.

Fig. 4.26 shows that the simulated impedance and phase responses align with the theoretical values up to 10 MHz for impedance and up to 10 kHz for phase. Fig. 4.28 shows the simulated magnitude and phase responses of the series R-C simulator as determined by the Monte-Carlo analysis. The related input voltage and current waveforms are shown in Fig. 4.29. A sinusoidal input voltage with a magnitude of 100 mV and a frequency of 10 kHz was applied for the time-domain analysis.

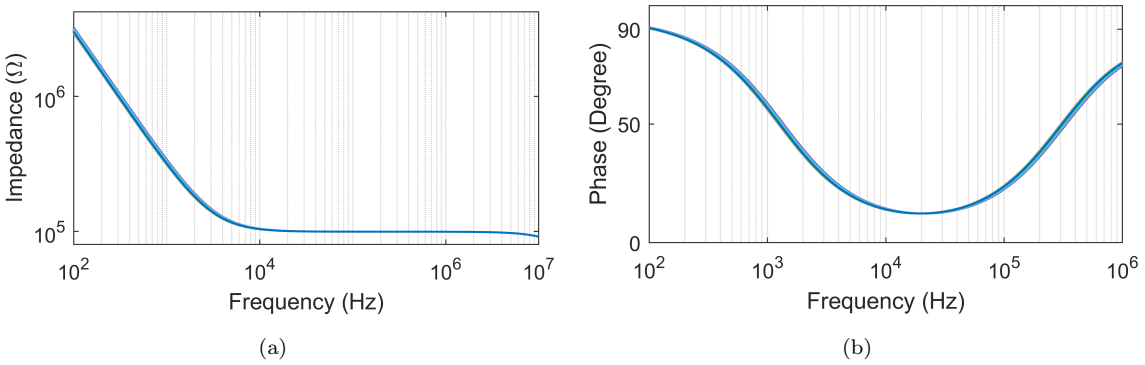


Figure 4.28: AC Monte-Carlo results of series R-C simulator of Circuit-2 (a) magnitude responses (b) Phase responses

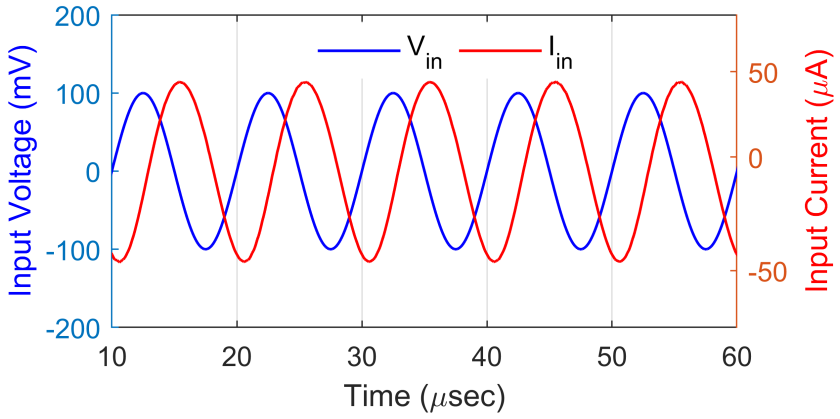
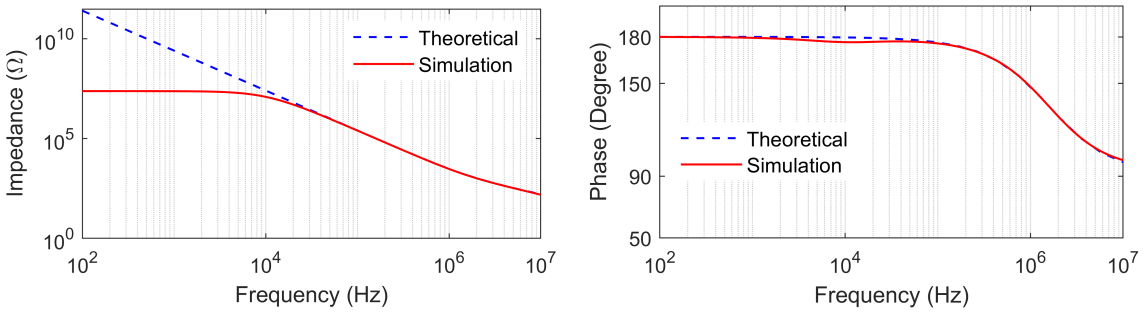


Figure 4.29: Transient responses of input voltage and current for series R-C simulator of Circuit-2

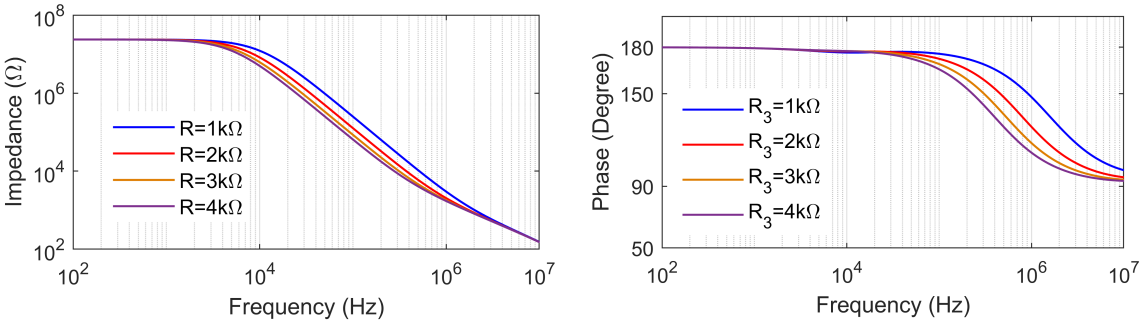
Using $C_1 = 100$pF, $C_2 = 100$pF, and $R_3 = 1$kΩ, the frequency responses of the impedance magnitude and phase were measured in order to verify the operation of the proposed series C-D circuit of Fig. 4.8 (Circuit-2). The responses are displayed in Fig. 4.30. Moreover, Fig. 4.31 shows variations in impedance magnitude and phase for various resistor values (1kΩ, 2kΩ, 3kΩ, and 4kΩ).

Monte-Carlo analysis has also been performed and the corresponding results are shown in Fig. 4.32. Transient responses of input voltage and current are performed for a sinusoidal input voltage of magnitude 50mV at a frequency of 100kHz by selecting $C_1 = 1$nF, $C_2 = 1$nF, and $R_3 = 10$kΩ has been shown in Fig. 4.33.



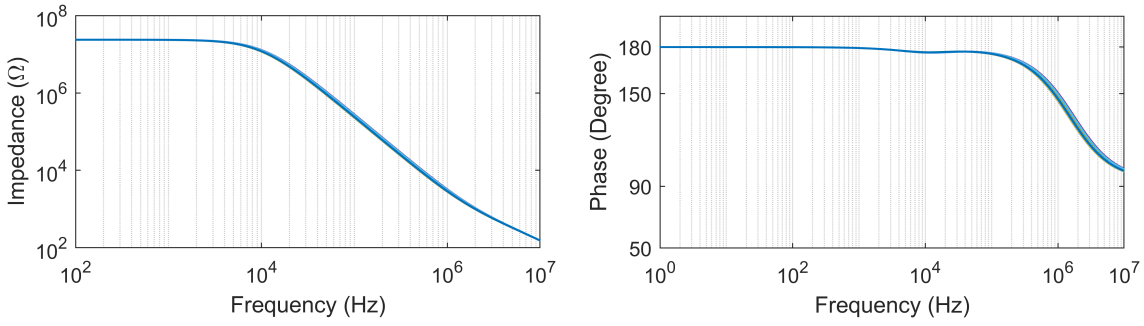
(a) (b)

Figure 4.30: Frequency responses (a) impedance and (b) phase of the series C-D simulator of Circuit-2



(a) (b)

Figure 4.31: Frequency responses of (a) magnitude (b) phase of series C-D simulator at different value of resistors



(a) (b)

Figure 4.32: AC Monte-Carlo results of series C-D simulator (a) magnitude responses (b) Phase responses

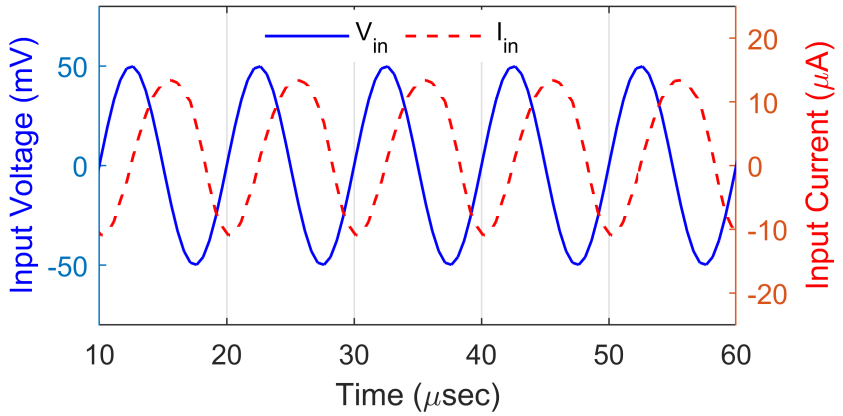
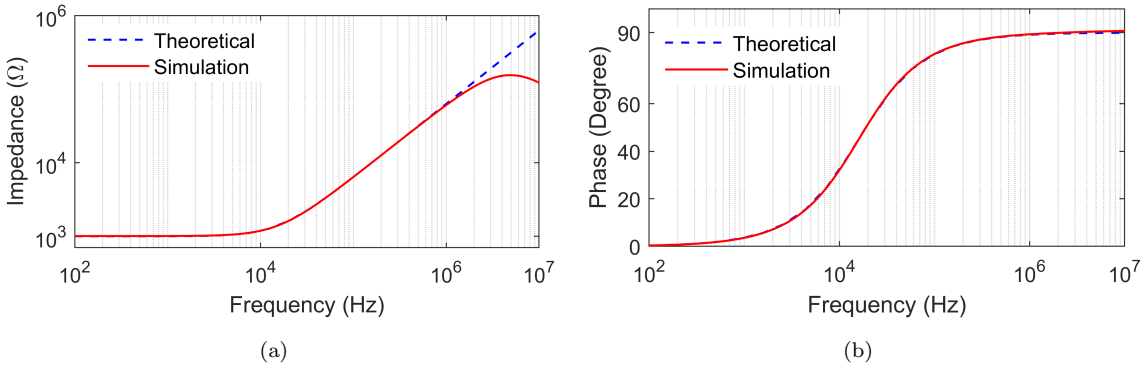


Figure 4.33: Transient responses of input voltage and current for series C-D simulator of Circuit-2



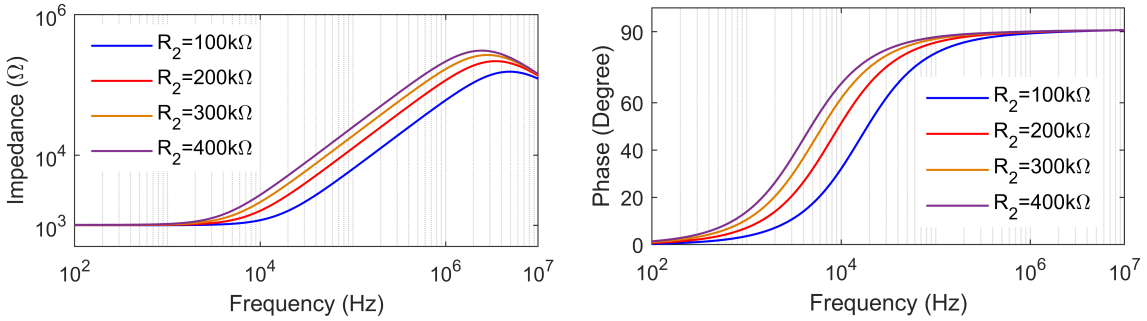
(a) (b)

Figure 4.34: Frequency responses of series R-L simulator (a) impedance and (b) phase of Circuit-3

4.2.2.3 Results for Circuit-3

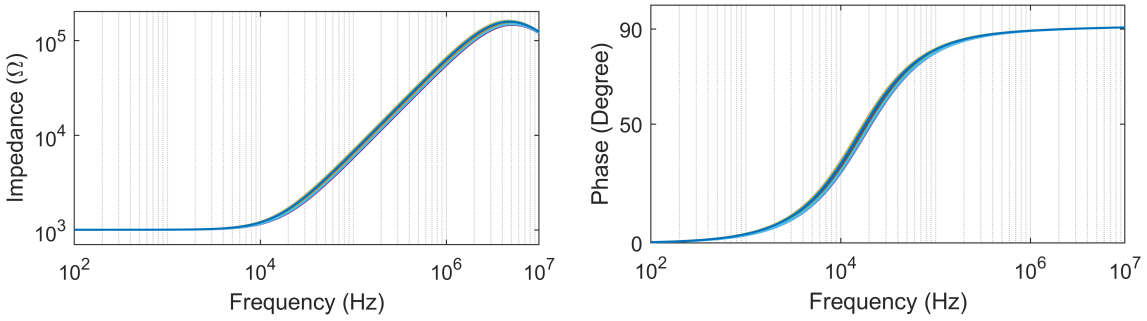
The proposed series R-L circuit of Fig. 4.8(Circuit-3) has been tested by selecting $R_1 = 1\text{k}\Omega$, $R_2 = 100$ kΩ and $C_3 = 100\text{pF}$. The theoretical and simulated impedance and phase results have been shown in Fig. 4.34. The variation in impedance and phase at different values of resistor R_2 (100kΩ, 200kΩ, 300kΩ, 400kΩ) have been depicted in Fig. 4.35.

From Fig. 4.34, the simulated frequency response of impedance and phase of series RL circuit of Fig. 4.8 (Circuit-3) are in proper accordance with the theoretical propositions up to a frequency range of 100Hz — 1MHz for impedance response and



(a) (b)

Figure 4.35: Frequency responses of series R-L simulator for different values of R_2 (a) magnitude (b) phase



(a) (b)

Figure 4.36: AC Monte-Carlo results of series R-L simulator of Circuit-3 (a) magnitude responses (b) Phase responses

100Hz — 10MHz for phase response. AC Monte-Carlo analysis has been carried out to check the robustness for the series R-L circuit of Fig. 4.8(Circuit-3), when 10% tolerance is applied to resistance R_2. The simulated impedance phase of AC Monte-Carlo analyses have been shown in Fig. 4.36. A sinusoidal input voltage signal with 100mV at 100kHz is applied. The input voltage and input current waveforms have been displayed in Fig. 4.37.

R_1 = 1kΩ, C_2 = 100pF and R_3 =100kΩ are selected as the passive components for series RC of Fig. 4.8(Circuit-3). AC magnitude and phase responses have been illustrated in Fig. 4.38. Frequency responses of magnitude and phase at different values of resistor R_3 (100kΩ, 200kΩ, 300kΩ, 400kΩ) have been shown in Fig. 4.39.

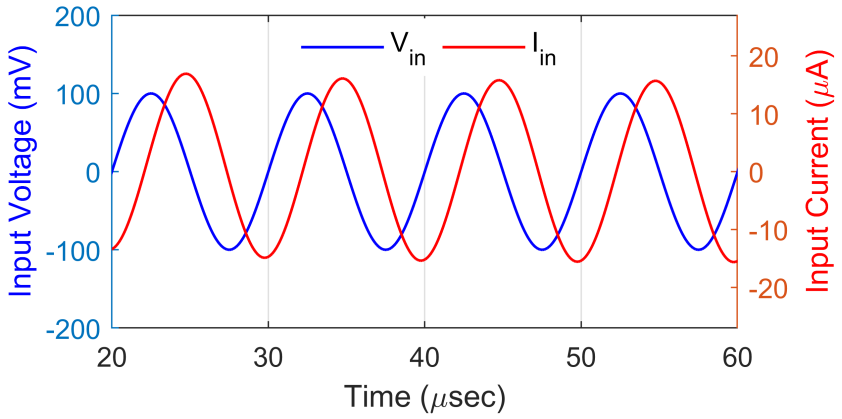


Figure 4.37: Transient responses of input voltage and current of series R-L simulator of Circuit-3

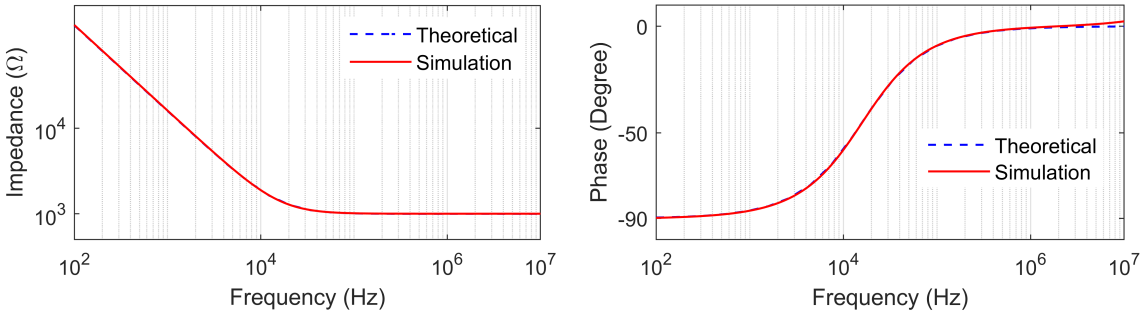
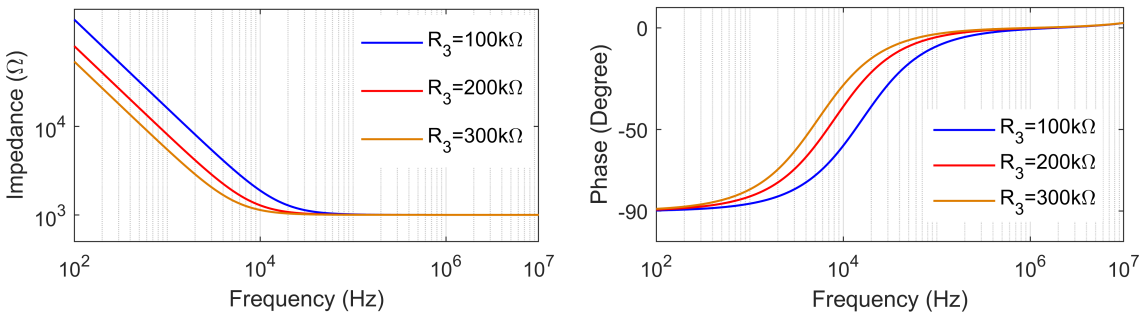


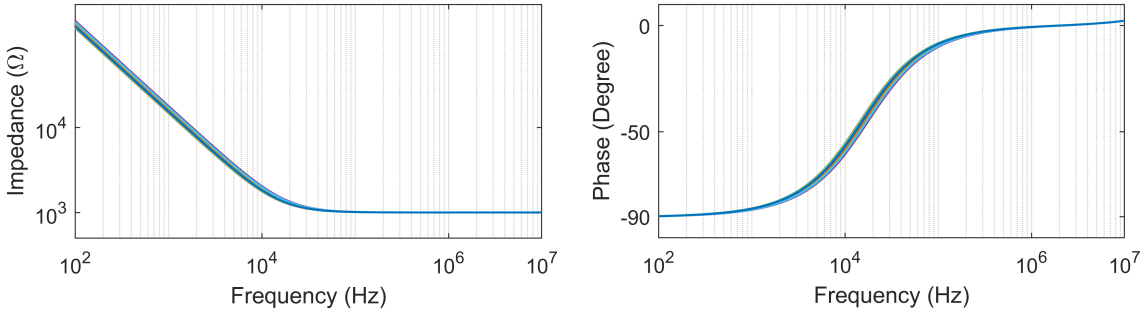
Figure 4.38: Frequency responses of series R-C simulator (a) impedance and (b) phase

From the results shown in Fig. 4.38, it is observed that the simulation results obtained for series R-C circuits of Fig. 4.8(Circuit-3) match with the theoretical propositions. AC Monte- Carlo simulation results for the series RC with 100 runs are given in Fig. 4.40 in which the resistor R_3 value deviates uniformly with 10%. A sinusoidal input voltage signal of amplitude 100mV at 10kHz is applied. Thus, the applied input voltage and input current waveforms have been shown in Fig. 4.41. The series C-D simulator of Fig. 4.8(Circuit-3) is tested by setting the passive component values as $C_1 = C_2 = 100$pF and resistor $R_3 = 1$kΩ. The simulated magnitude and phase responses with theoretical values have been displayed in Fig. 4.42. The variation in magnitude and phase responses at different values of resistor R_3 (1kΩ, 2kΩ, 3kΩ, 4kΩ) have been displayed in Fig. 4.43. From Fig. 4.42(a)



(a) (b)

Figure 4.39: Frequency responses of series R-C simulator for different value of resistors (a) magnitude (b) phase



(a) (b)

Figure 4.40: AC Monte-Carlo results of series R-C simulator (a) magnitude responses (b) Phase responses

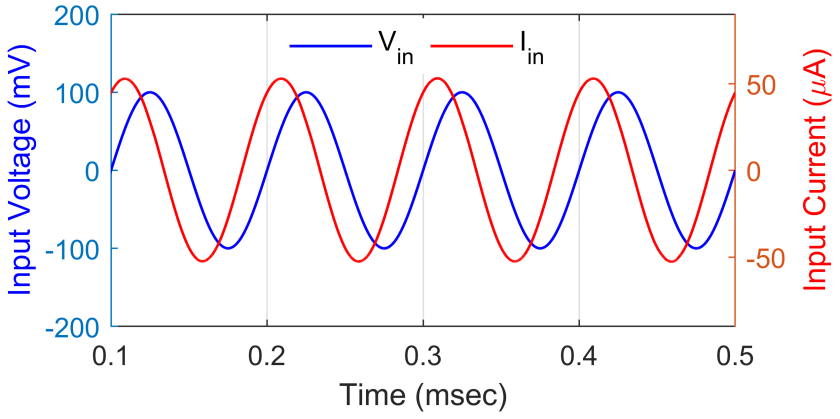
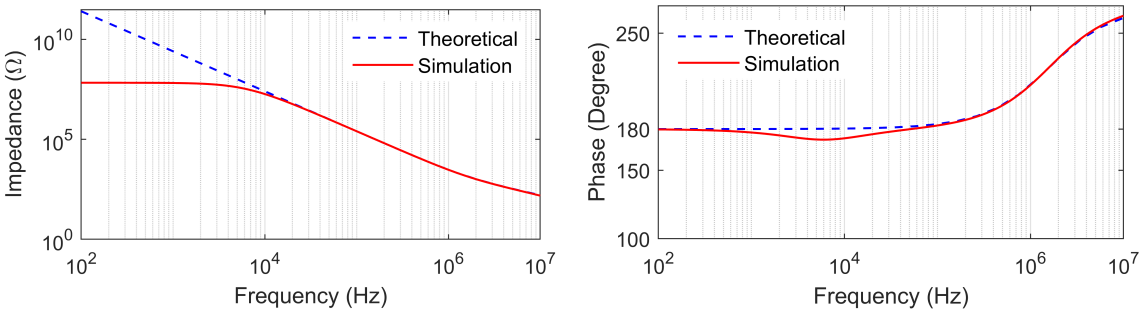


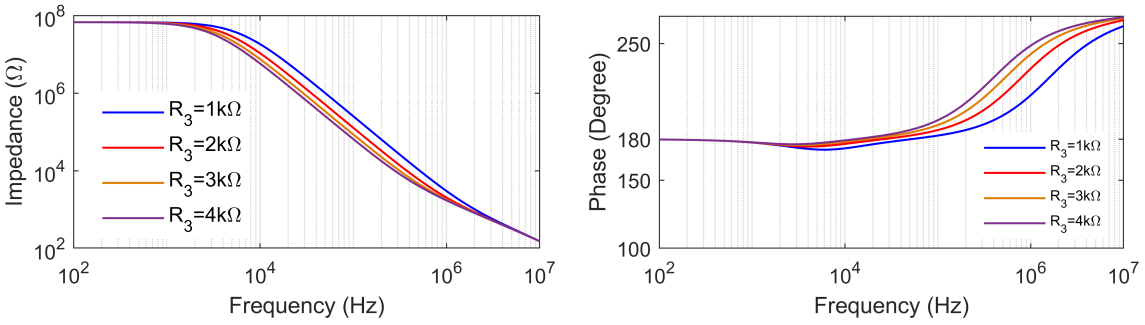
Figure 4.41: Transient responses of input voltage and current for series R-C simulator

and (b), it is evident that the simulated results of series C-D circuit are in proper accordance with the theoretical evaluations up to a frequency range of 1kHz – 10MHz



(a) (b)

Figure 4.42: Frequency responses (a) impedance and (b) phase of the series C-D simulator of Circuit-3



(a) (b)

Figure 4.43: Frequency responses of (a) magnitude (b) phase of series C-D simulator at different value of resistors

for impedance response and 100Hz—10MHz for phase response. The simulated magnitude and phase of AC Monte-Carlo analysis have been shown in Fig. 4.44. The transient responses of input voltage and input current have been displayed in Fig. 4.45 when input voltage of amplitude 10mV at 100kHz is applied.

4.2.2.4 Results for Circuit-4

The proposed series R-L circuit, as shown in Fig. 4.8 (Circuit-4), was tested with the following component values: $R_1 = 1$ kΩ, $R_2 = 100$ kΩ, and $C_3 = 100$ pF. The theoretical and simulated results for impedance and phase are presented in Fig. 4.46. Additionally, Fig. 4.47 illustrates how the impedance and phase change with

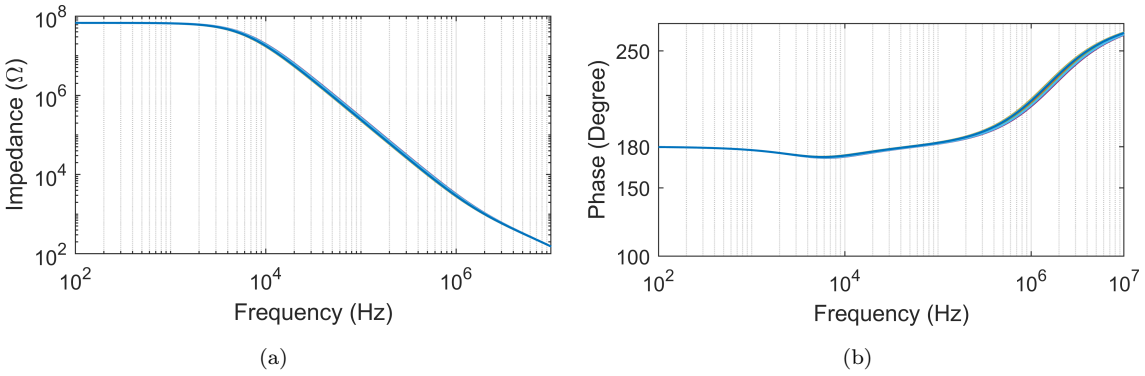


Figure 4.44: AC Monte-Carlo results of series C-D simulator (a) magnitude responses (b) Phase responses

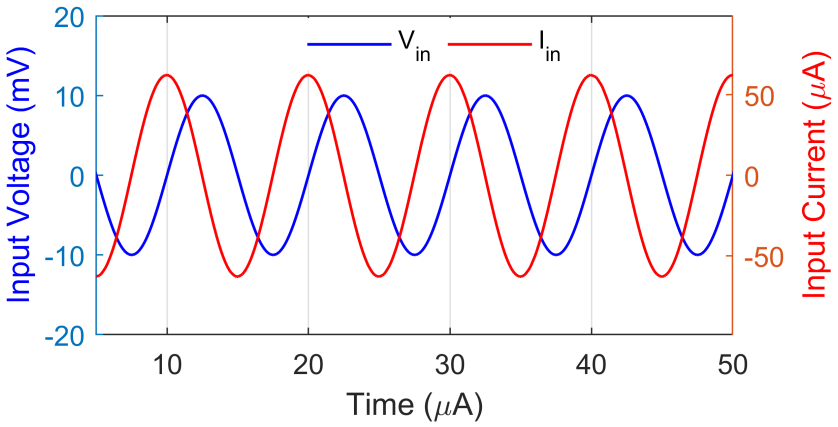
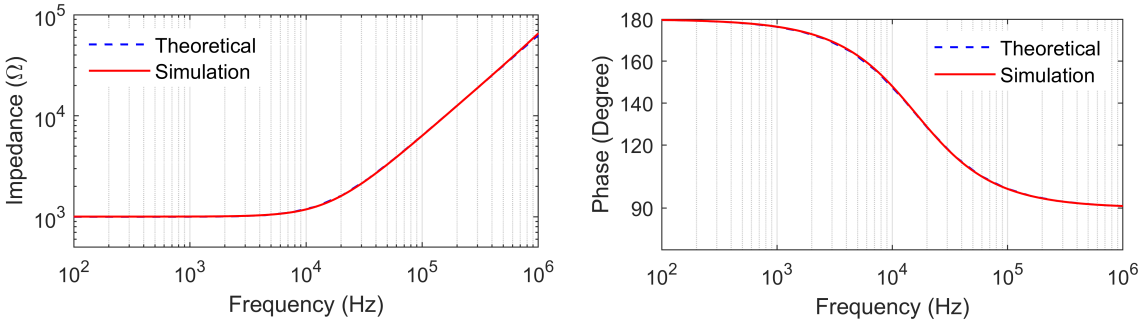


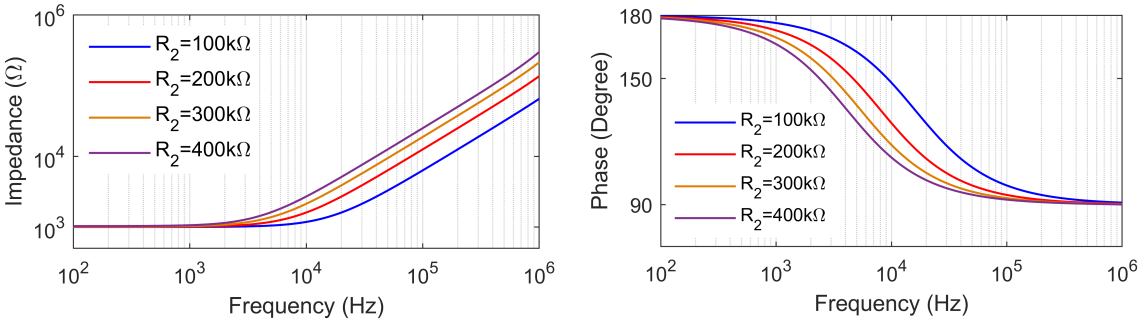
Figure 4.45: Transient responses of input voltage and current for series C-D simulator of Circuit-3

varying resistor values for R_2 (100 kΩ, 200 kΩ, 300 kΩ, and 400 kΩ). According to Fig. 4.46, the simulated frequency response of impedance and phase for the series RL circuit (Fig. 4.8, Circuit-4) aligns well with the theoretical predictions, showing consistency within the frequency range of 100 Hz to 1 MHz for impedance, and 100 Hz to 1 MHz for phase response. An AC Monte-Carlo analysis was performed to evaluate the robustness of the series R-L circuit in Fig. 4.8 (Circuit-4) when a 10% tolerance is applied to the resistance R_2. The simulated impedance and phase results from the Monte-Carlo analysis are presented in Fig. 4.48. A sinusoidal input voltage of 100 mV at 500 kHz was applied, and the corresponding input voltage and current waveforms are shown in Fig. 4.49.



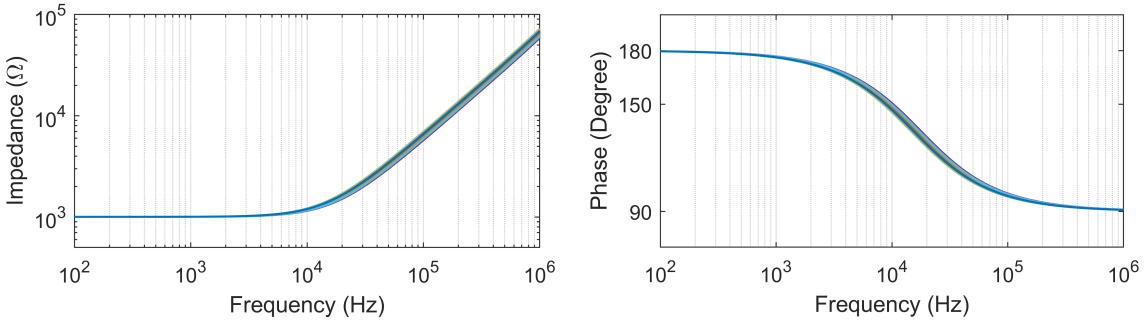
(a) (b)

Figure 4.46: Frequency responses of series R-L simulator (a) impedance and (b) phase of Circuit-4



(a) (b)

Figure 4.47: Frequency responses of series R-L simulator for different values of R_2 (a) magnitude (b) phase



(a) (b)

Figure 4.48: AC Monte-Carlo results of series R-L simulator of Circuit-4 (a) magnitude responses (b) Phase responses

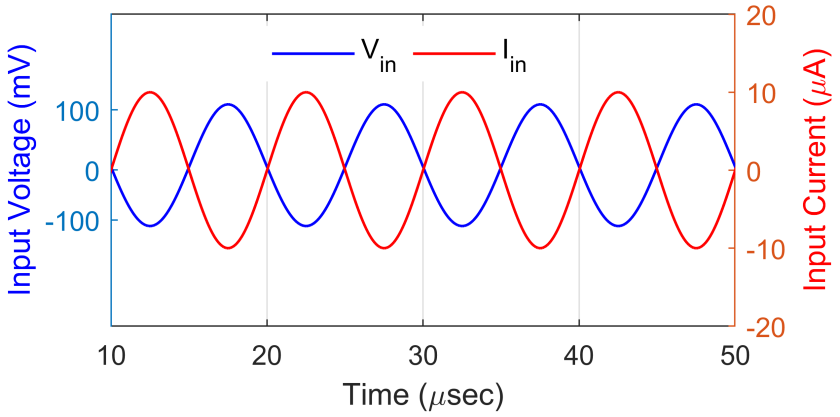
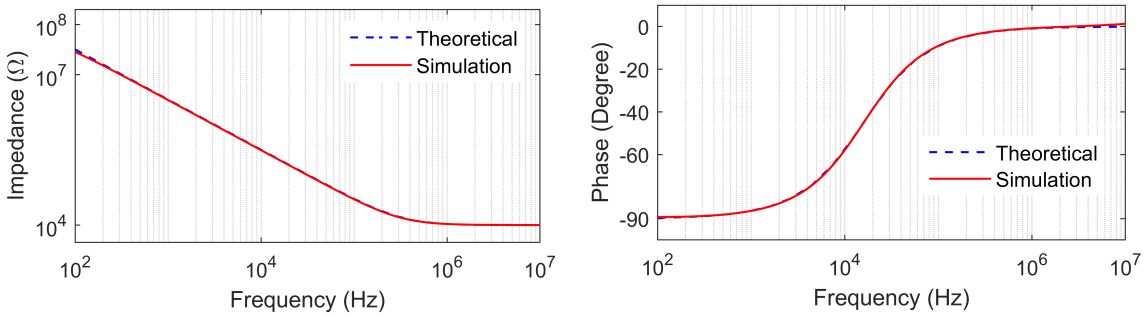


Figure 4.49: Transient responses of input voltage and current of series R-L simulator of Circuit-4

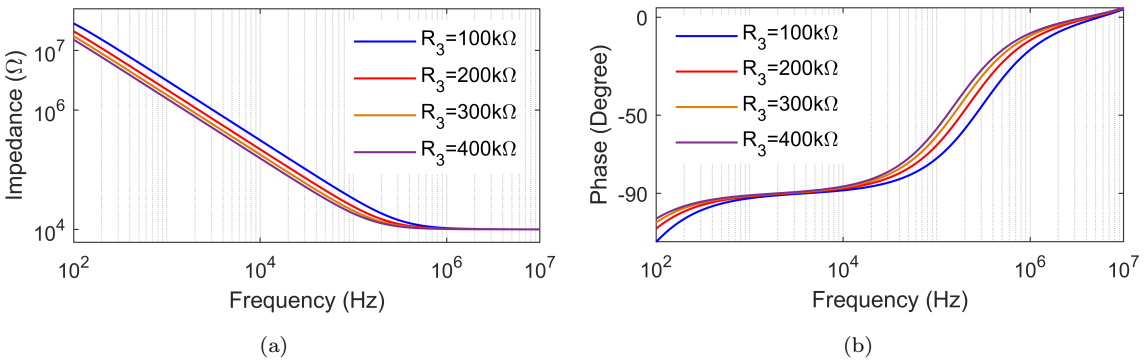


(a) (b)

Figure 4.50: Frequency responses of series R-C simulator (a) impedance and (b) phase

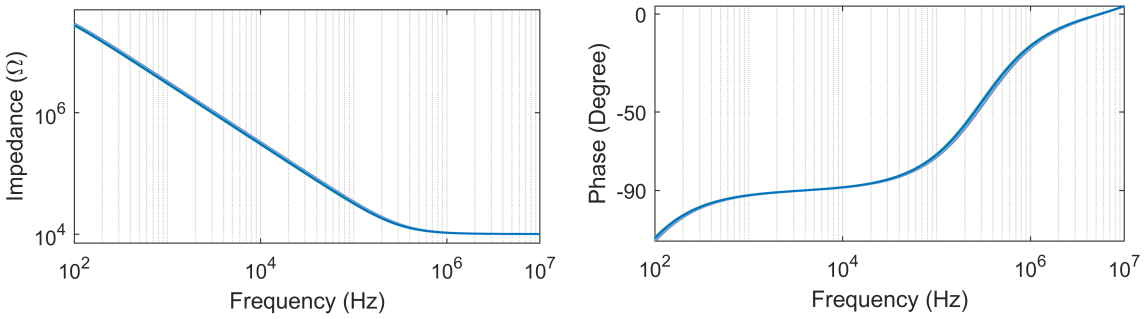
For the series RC circuit in Fig. 4.8(Circuit-4), the passive components selected are $R_1 = 1$ kΩ, $C_2 = 100$ pF, and $R_3 = 100$ kΩ. The AC magnitude and phase responses are presented in Fig. 4.50. Additionally, Fig. 4.51 shows the frequency responses of magnitude and phase for different values of the resistor R_3 (100 kΩ, 200 kΩ, 300 kΩ and 400 kΩ).

The results presented in Fig. 4.50 indicate that the simulation outcomes for the series R-C circuits in Fig. 4.8 (Circuit-4) are in agreement with the theoretical predictions. The AC Monte-Carlo simulation results for the series RC circuit, based on 100 runs, are presented in Fig. 4.52. In this analysis, the value of resistor R_3 varies uniformly by 10%. A sinusoidal input voltage of 100 mV amplitude at 10 kHz



(a) (b)

Figure 4.51: Frequency responses of series R-C simulator for different value of resistors (a) magnitude (b) phase



(a) (b)

Figure 4.52: AC Monte-Carlo results of series R-C simulator (a) magnitude responses (b) Phase responses

is applied, and the corresponding input voltage and current waveforms are displayed in Fig. 4.53.

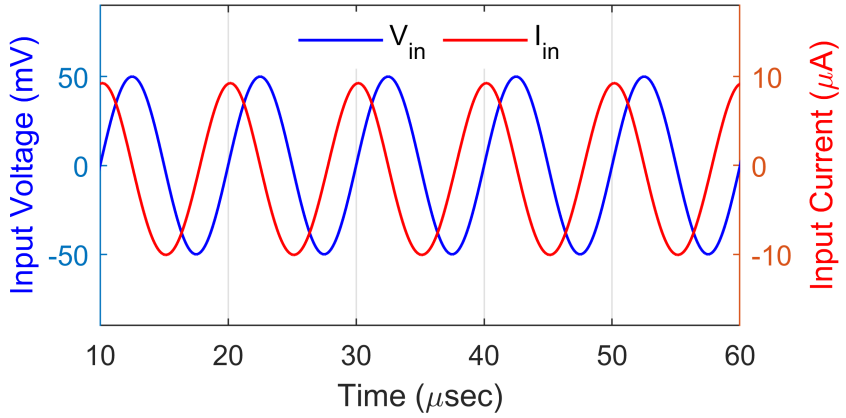
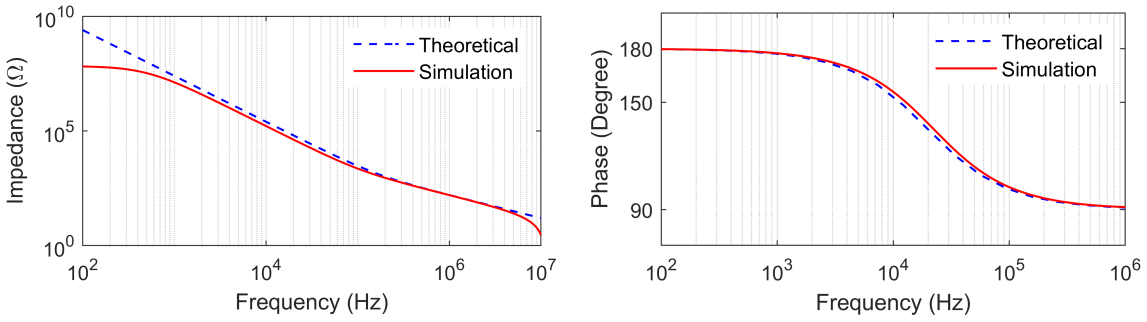
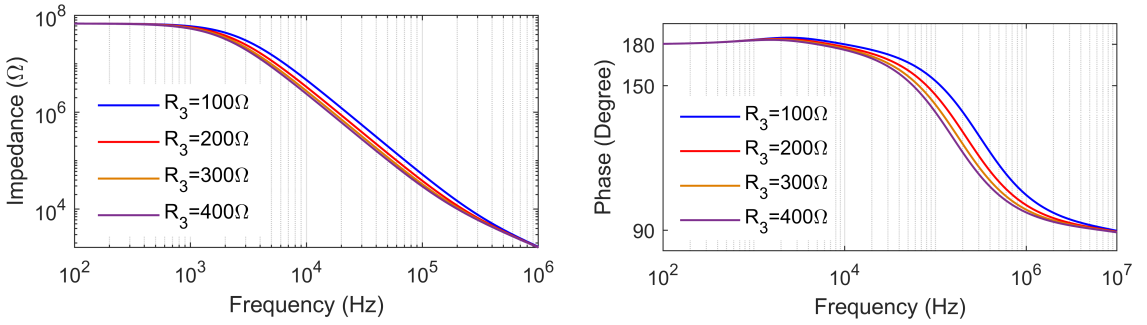


Figure 4.53: Transient responses of input voltage and current for series R-C simulator



(a) (b)

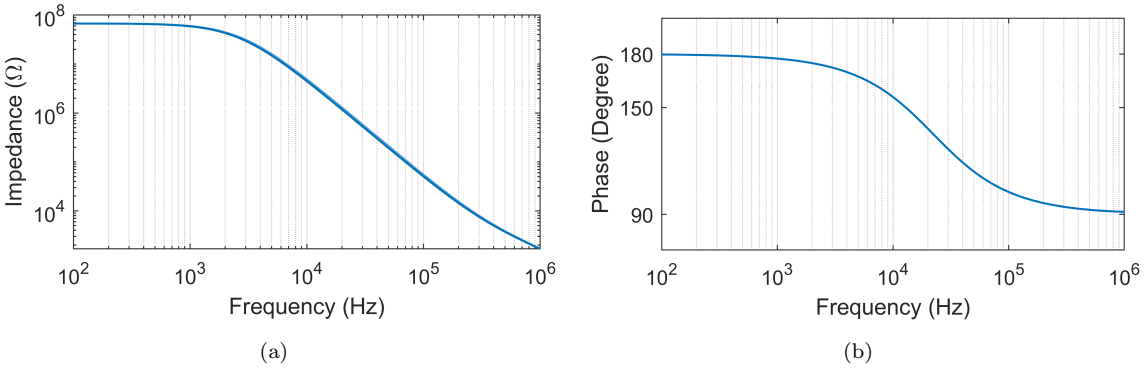
Figure 4.54: Frequency responses (a) impedance and (b) phase of the series C-D simulator of Circuit-4



(a) (b)

Figure 4.55: Frequency responses of (a) magnitude (b) phase of series C-D simulator at different value of resistors

The series C-D circuit simulator in Fig. 4.8(Circuit-4) was tested with the passive component values set to $C_1 = C_2 = 100$ pF and $R_3 = 100\Omega$. The simulated magnitude and phase responses, along with the theoretical values, are shown in Fig. 4.54. Fig. 4.55 illustrates the variation in magnitude and phase responses for different values of resistor R_3 (100Ω, 200Ω, 300Ω, and 400Ω). As shown in Fig. 4.54, the simulated results of the series C-D circuit align closely with the theoretical calculations within the frequency range of 1 kHz to 10 MHz for the impedance response and 100 Hz to 10 MHz for the phase response. Fig. 4.56 shows the simulated magnitude and phase from the Monte Carlo AC analysis. Furthermore, Fig. 4.57 illustrates the transient responses of the input voltage and current when a 10 mV amplitude input voltage at 100 kHz is applied.



(a) (b)

Figure 4.56: AC Monte-Carlo results of series C-D simulator (a) magnitude responses (b) Phase responses

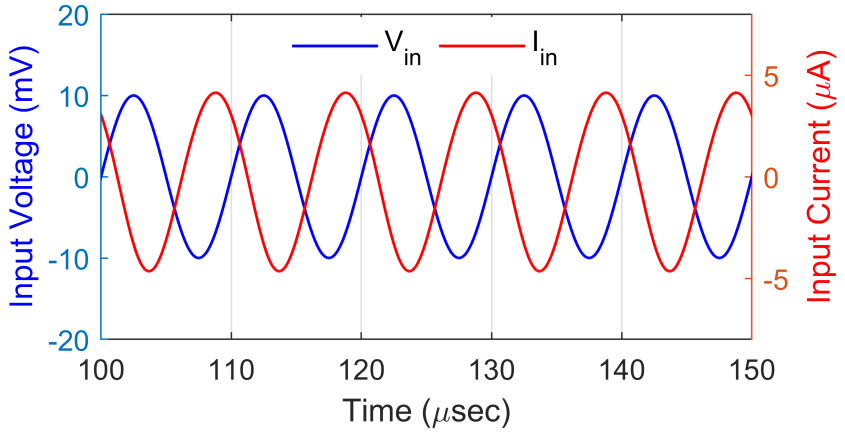
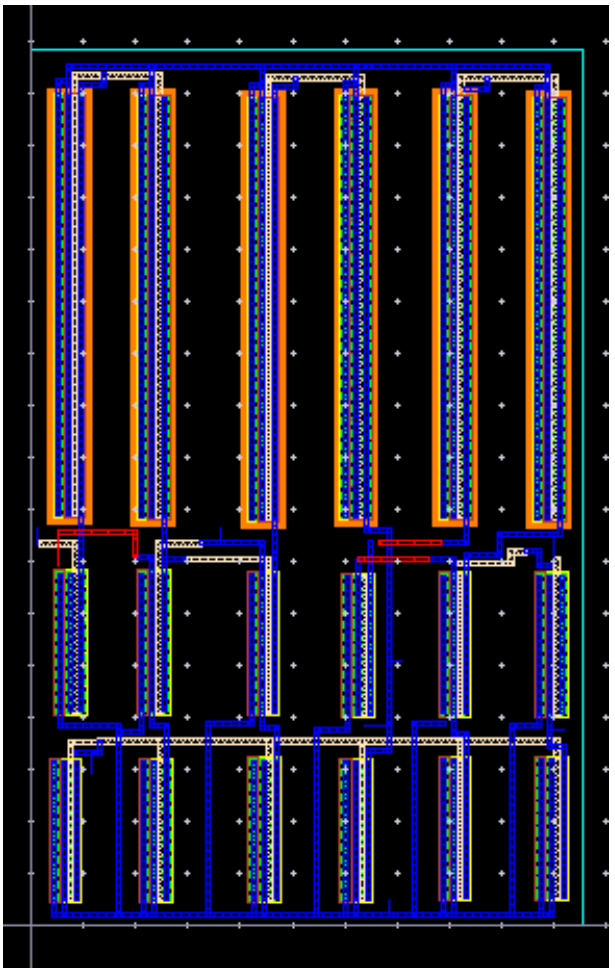


Figure 4.57: Transient responses of input voltage and current for series C-D simulator of Circuit-4

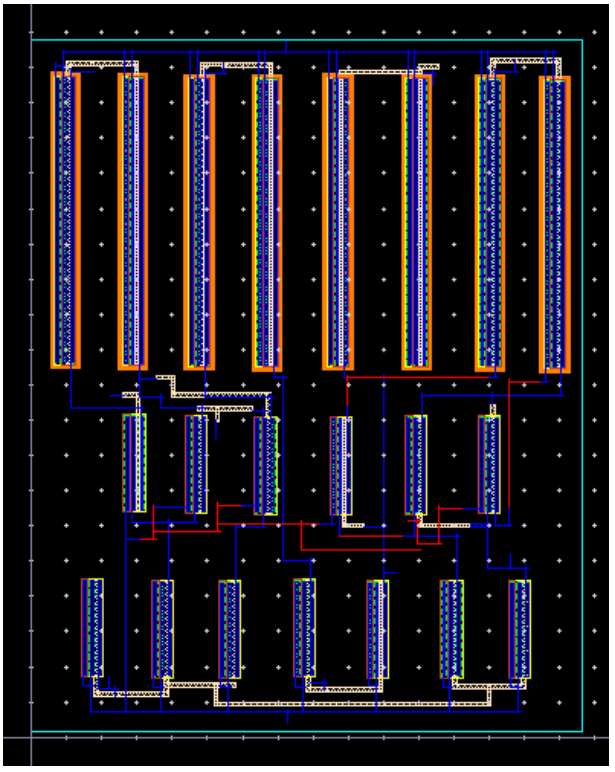
4.2.3 Pre and Post layout simulations

To further validate the workability of the proposed grounded series immittance circuits, pre-layout and post-layout simulations were conducted for Circuit-1 of Fig. 4.8 using the Cadence Virtuoso simulation tool. The layouts of the proposed CMOS VCII+ and VCII- have been shown in Fig. 4.58.

The NMOS and PMOS width and length values were kept same as considered in Fig. 4.9. The power supply voltages, VDD and VSS, were set to 0.9V, while the bias currents, I_{B0} and I_{B1} were set to 25µA and the value of R_1 = 1k, C_2 = 10pF, R_3 = 10kΩ are selected for series RC and R_1 = 1kΩ, R_2 = 10kΩ and C_3 = 10pF



(a)



(b)

Figure 4.58: Layout design of (a) VCII+ and (b) VCII-

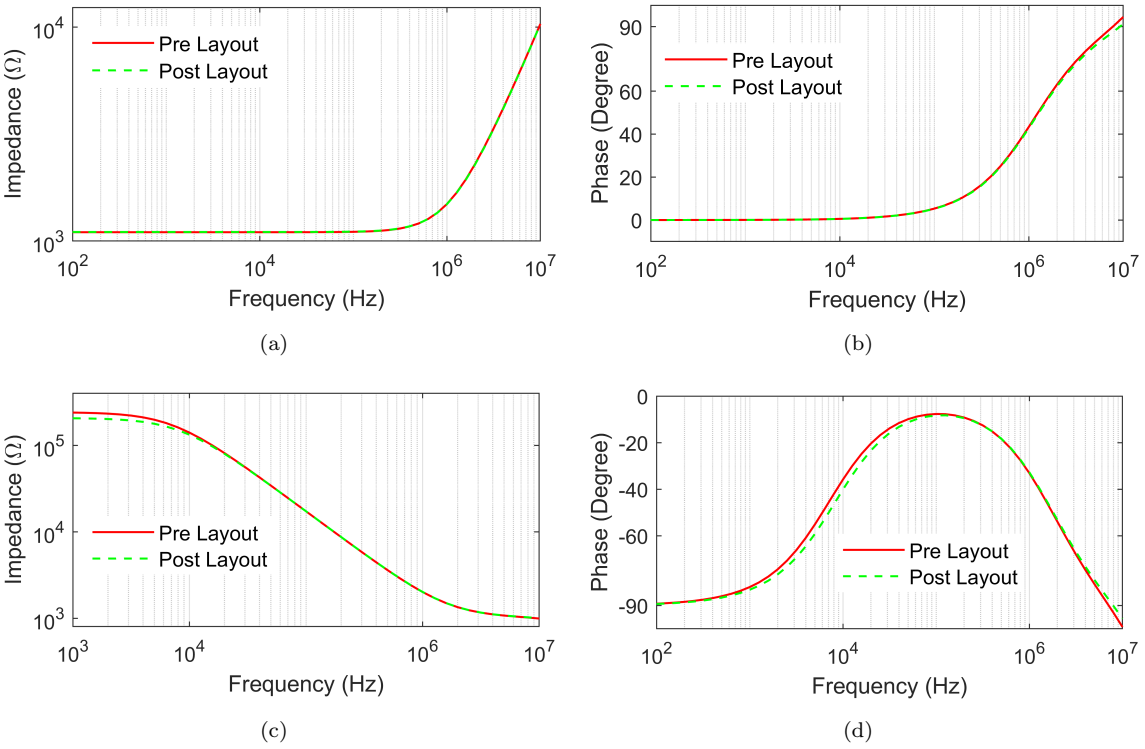


Figure 4.59: Frequency response of (a) magnitude of series R-L (b) phase of series R-L (c) magnitude of series R-C (d) phase of series R-C

are selected for series RL. To confirm the feasibility of the proposed circuit, the layout of the circuit of Fig. 4.8(Circuit-1) passed all physical verification checks, including design rule check (DRC), layout and schematic extraction (LVS), and RC extraction. The pre-layout and post-layout impedance and phase of the series RL, series RC of Fig. 4.8(Circuit-1) are depicted in Fig. 4.59. From Fig. 4.59, it can be concluded that the pre-layout simulated magnitude and phase responses closely align with the post-layout results. Thus, these results confirm the validity of the proposed configurations.

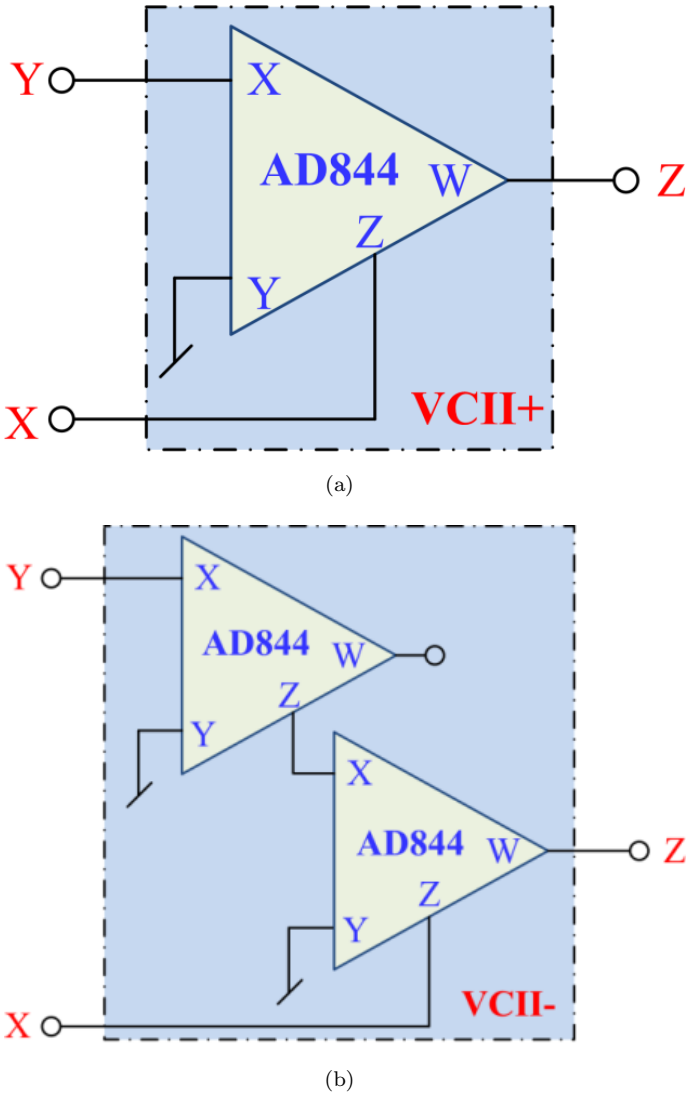


Figure 4.60: AD844 implementation of (a) VCII+ (b) VCII- [68]

4.2.4 Experimental results

To experimentally evaluate the proposed immittance simulator circuits, VCII is implemented using off-the-shelf commercially available IC AD844. One IC is necessary for the implementation of VCII+ and two ICs are required for the implementation of VCII-. Fig. 4.60 illustrates the AD844-based VCII+ and VCII- configurations.

The series RL simulator derived from Circuit-1 of Fig. 4.8 was experimentally tested using the circuit shown in Fig. 4.61 by selecting $R_1 = 1\text{k}\Omega$, $R_2 = 100\text{k}\Omega$ and

$C_3 = 100$pF. To bias AD844s, the power supply voltages were set to ±15V. Passive

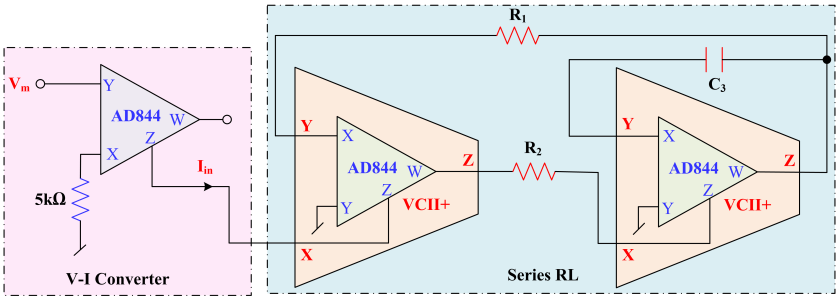
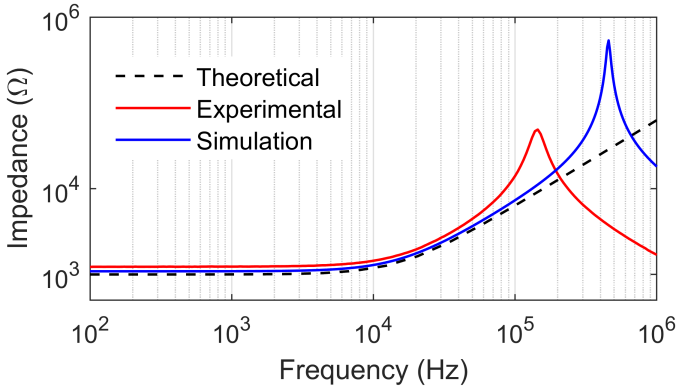
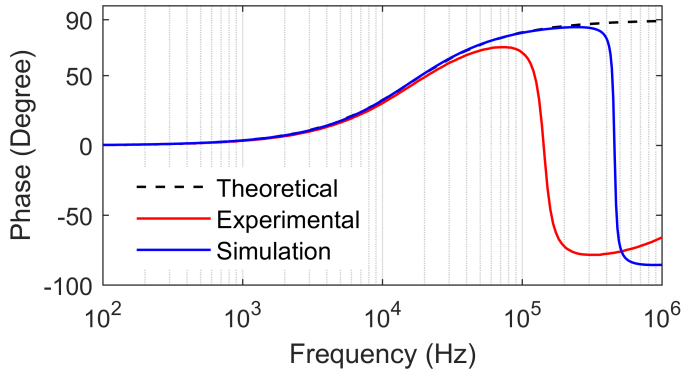


Figure 4.61: Complete circuit realization of series RL simulator of Circuit-1 of Fig. 4.8

components with a 5% tolerance for resistors and a 10% tolerance for capacitors were used. Fig. 4.62 illustrates the equivalent impedance and phase responses.



(a)



(b)

Figure 4.62: Experimental results of series RL simulator for Circuit-1 of Fig. 4.8(a) input impedance (b) phase

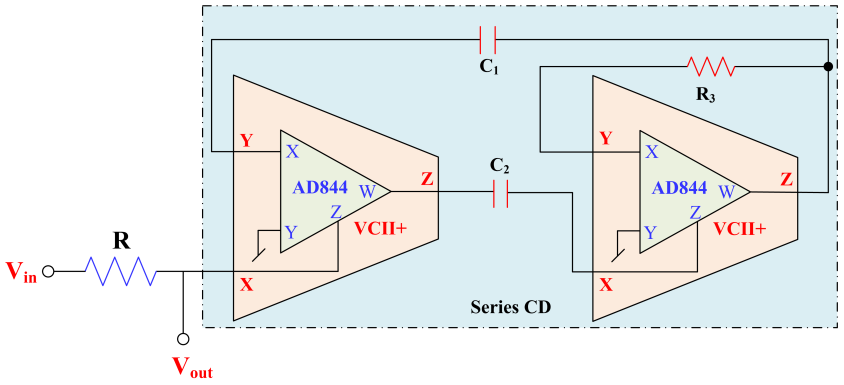


Figure 4.63: Second order low pass filter as an application example of series CD of Circuit-1 of Fig. 4.8

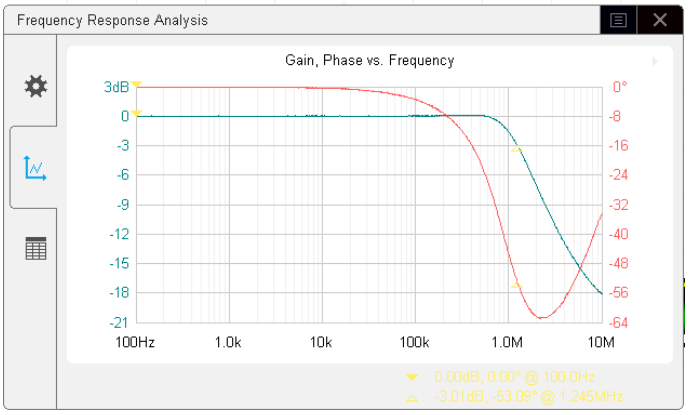
The transfer function of second order low pass filter can be written as:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{s^2 C_1 C_2 R_3 R + s C_2 R_3 + 1} \tag{4.9}$$

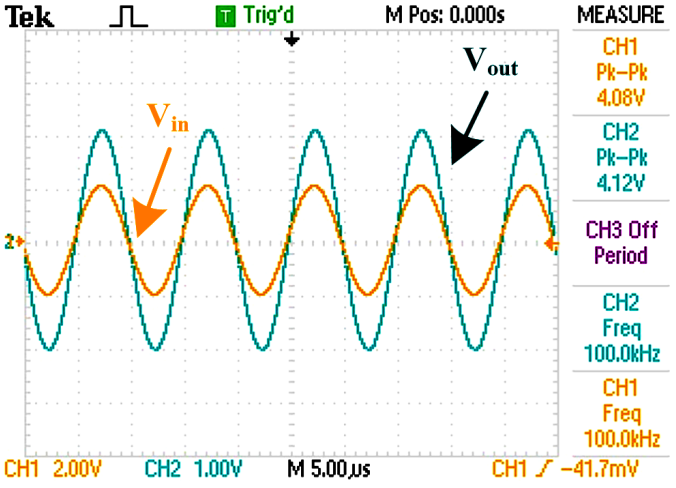
The cut-off frequency obtained from the equation (4.9) is:

$$f_0 = \frac{1}{2\pi\sqrt{C_1 C_2 R_3 R}} \tag{4.10}$$

The experimental results depicted in Fig. 4.62 indicate that the magnitude response and phase response of the proposed series RL simulator closely correspond with the simulated and theoretical outcomes across a frequency range of 100Hz to 60kHz. To verify the usability of proposed immittance simulator circuits, an application example of series CD of Circuit-1 of Fig. 4.8 has been used to design a second order low pass filter as shown in Fig. 4.63. The transfer function and cut-off frequency are given in equation (4.9) and (4.10) respectively. The passive component values selected as $C_1 = C_2 = 100$pF, $R_3 = 1$kΩ and R = 1kΩ to obtain a cut-off frequency of 1.59MHz. Fig. 4.64 shows the experimental frequency response of magnitude and phase, also transient response of sinusoidal input voltage of 4V peak-peak at 100kHz.



(a)



(b)

Figure 4.64: (a) Experimentally obtained frequency responses and (b) transient responses of second-order low pass filter

The simulated and experimental results displayed in Fig. 4.10 – Fig. 4.64, thus, validate the functionality of the proposed grounded series immittance simulator circuits and their applications.

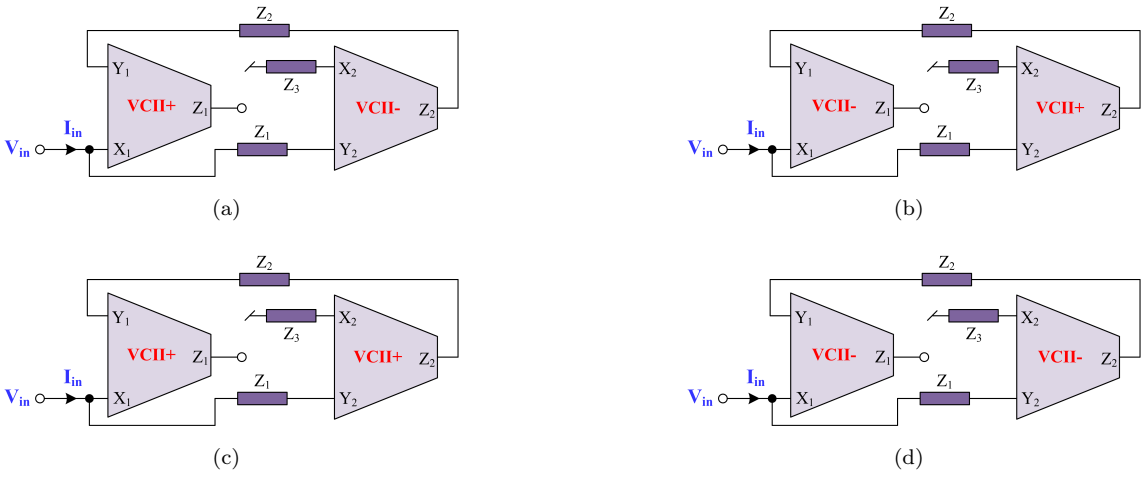


Figure 4.65: Proposed generalized grounded parallel immittance simulators (a) Circuit-1 (b) Circuit-2 (c) Circuit-3 (d) Circuit-4

4.3 Grounded parallel type immittance simulators using VCII

This section introduces four generalized configurations of grounded parallel-type immittance simulators. The proposed circuits are capable of realizing parallel R-L, R-C, C-D simulators and capacitance multiplier using only two second-generation voltage conveyors (VCII±) as active components, along with three passive impedances. Notably, these designs do not require any impedance matching conditions. The proposed generalized grounded parallel immittance simulator circuits employing two VCIIs and three impedances are shown in Fig. 4.65[2].

Performing a standard analysis on the circuits depicted in Fig. 4.65, utilizing the

[2]M. Shrivastava, D. R. Bhaskar, and P. Kumar, "VCII-based immittance simulators: Generalized parallel configurations," International Journal of Circuit Theory and Applications, 2024.

port voltage-current correlations (I_x= $\pm I_y$, V_z = V_x and V_y=0), results in the following admittance equations:

$$\text{Circuit 1 \& Circuit 2}: \quad \frac{I_{\text{in}}}{V_{\text{in}}} = Y_{\text{in}} = \frac{1}{Z_1}\left(1 + \frac{Z_3}{Z_2}\right) \tag{4.11}$$

$$\text{Circuit 3 \& Circuit 4}: \quad \frac{I_{\text{in}}}{V_{\text{in}}} = Y_{\text{in}} = \frac{1}{Z_1}\left(1 - \frac{Z_3}{Z_2}\right) \tag{4.12}$$

By selecting appropriate impedances, Z_1, Z_2, and Z_3, and substituting them into equations (4.11)-(4.12), a range of immittance simulators can be achieved, such as grounded parallel RL, parallel RC, parallel CD, and grounded capacitance multiplier circuits. The implementations of these circuits are elaborated in Table 4.2.

Table 4.2: Immittance realizations obtained from the generalized circuit of Fig. 4.65

Circuits	Impedance choices	Input admittance (Y_{in})	Realization type
Circuit 1 & Circuit 2	$Z_1 = R_1, Z_2 = R_2, Z_3 = \frac{1}{sC_3}$	$Y_{\text{in}} = \frac{1}{R_1} + \frac{1}{sR_1R_2C_3} = \frac{1}{R_{\text{eq}}} + \frac{1}{sL_{\text{eq}}}$	Parallel R-L
	$Z_1 = R_1, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$Y_{\text{in}} = \frac{1}{R_1} + \frac{sC_2R_3}{R_1} = \frac{1}{R_{\text{eq}}} + sC_{\text{eq}}$	Parallel R-C
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$Y_{\text{in}} = sC_1 + s^2C_1C_2R_3 = sC_{\text{eq}} + s^2D_{\text{eq}}$	Parallel C-D
	$Z_1 = \frac{1}{sC_1}, Z_2 = R_2, Z_3 = R_3$	$Y_{\text{in}} = sC_1\left(1 + \frac{R_3}{R_2}\right) = sC_{\text{eq}}$	Positive Capacitance Multiplier
Circuit 3 & Circuit 4	$Z_1 = R_1, Z_2 = R_2, Z_3 = \frac{1}{sC_3}$	$Y_{\text{in}} = \frac{1}{R_1} - \frac{1}{sR_1R_2C_3} = \frac{1}{R_{\text{eq}}} - \frac{1}{sL_{\text{eq}}}$	Parallel R-(-L)
	$Z_1 = R_1, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$Y_{\text{in}} = \frac{1}{R_1} - \frac{sC_2R_3}{R_1} = \frac{1}{R_{\text{eq}}} - sC_{\text{eq}}$	Parallel R-(-C)
	$Z_1 = \frac{1}{sC_1}, Z_2 = \frac{1}{sC_2}, Z_3 = R_3$	$Y_{\text{in}} = sC_1 - s^2C_1C_2R_3 = sC_{\text{eq}} - s^2D_{\text{eq}}$	Parallel C-(-D)
	$Z_1 = \frac{1}{sC_1}, Z_2 = R_2, Z_3 = R_3$	$Y_{\text{in}} = sC_1\left(1 - \frac{R_3}{R_2}\right) = sC_{\text{eq}}$	Positive/Negative Capacitance Multiplier

Table 4.2 highlights that the proposed circuits can realize grounded parallel RL, parallel RC, parallel CD, as well as positive/negative capacitance multiplier functionalities through judicious selection of impedances.

4.3.1 Non-ideal and parasitic analyses

Considering the effect of the non-ideal gains of the VCIIs on the circuits presented in Fig. 4.65 has been assessed using the terminal characteristic equations: I_X =

$\pm\beta_i I_Y$, $V_Z = \alpha_i V_X$ and $V_Y = 0$, where i = 1-2, indicates number of VCII±, α and β are voltage and current gain respectively. Changes in the realization of immittance circuits are caused by non-ideal voltage and current gains. To investigate the impact of tracking errors, a re-analysis of the proposed immittance circuits has been conducted, and the modified admittance values are provided in equations (4.13) – (4.14).

$$\text{Circuit 1 \& Circuit 2 :} \quad \frac{I_{\text{in}}}{V_{\text{in}}} = \frac{1}{Z_1}\left(1 + \frac{\beta_1\alpha_2 Z_3}{Z_2}\right) \tag{4.13}$$

$$\text{Circuit 3 \& Circuit 4 :} \quad \frac{I_{\text{in}}}{V_{\text{in}}} = \frac{1}{Z_1}\left(1 - \frac{\beta_1\alpha_2 Z_3}{Z_2}\right) \tag{4.14}$$

Observing equations (4.13) – (4.14), it becomes apparent that the influence of non-ideal gains on the admittance values is negligible, with the equations approaching ideal values as these gains approach unity. Fig. 4.66 illustrates the non-ideal model of the VCII±, encompassing its parasitic elements. R_Y signifies the parasitic resistance associated to the low-impedance current input terminal Y, whereas R_Z represents the parasitic resistance originating from the low-impedance voltage output terminal Z. Ideally, both R_Y and R_Z should be equate to zero. The parasitic resistance R_X and parasitic capacitance C_X, linked in parallel, contribute to the parasitic effects of the high-impedance current output terminal X, which ideally should possess an infinite impedance. Fig. 4.67 depicts the complete circuits shown in Fig. 4.65, including the parasitic resistors and capacitor of VCIIs shown in Fig. 4.66. Reanalyzing the circuit shown in 4.67, the non-ideal admittance expressions for Circuit-1 and Circuit-2 and Circuit-3 and Circuit-4, as given in equations (4.15) and (4.16), are derived under the assumption that all resistors connected to terminal 'Y' are equal (i.e.,$R_{Y1} = R_{Y2} = R_Y$), all resistors at terminal 'Z' are equal (i.e.,$R_{Z1} = R_{Z2} = R_Z$), and all resistors and capacitors connected to terminal 'X' are identical (i.e.,$R_{X1} = R_{X2} = R_X$, and

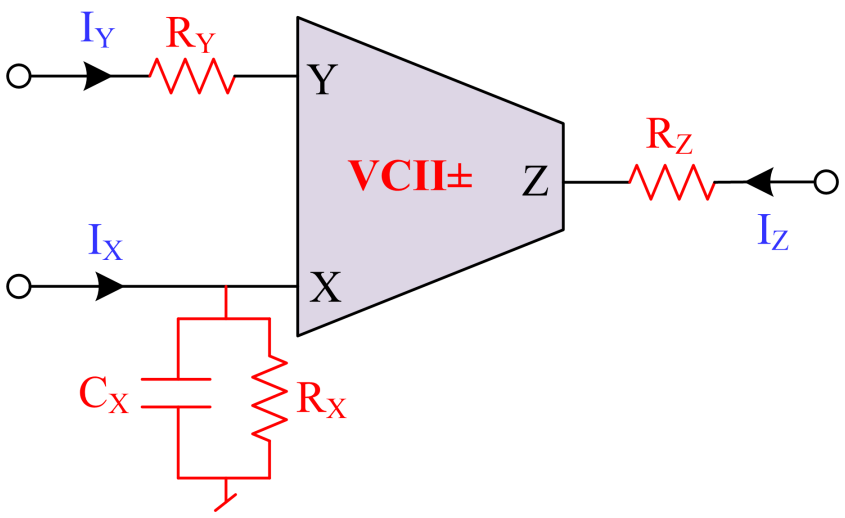


Figure 4.66: Non-ideal model of VCII± with parasitic element

$C_{X1} = C_{X2} = C_X$).

$$\frac{I_{\text{in}}}{V_{\text{in}}} = \frac{(R_Z + Z_2 + R_Y)(R_X + Z_3 + sC_X R_X Z_3)[R_X + (R_Y + Z_1)(1 + sC_X R_X)] + Z_3 R_X^2}{R_X(R_Y + Z_1)(R_Z + Z_2 + R_Y)(R_X + Z_3 + sC_X R_X Z_3)} \tag{4.15}$$

$$\frac{I_{\text{in}}}{V_{\text{in}}} = \frac{(R_Z + Z_2 + R_Y)(R_X + Z_3 + sC_X R_X Z_3)[R_X + (R_Y + Z_1)(1 + sC_X R_X)] - Z_3 R_X^2}{R_X(R_Y + Z_1)(R_Z + Z_2 + R_Y)(R_X + Z_3 + sC_X R_X Z_3)} \tag{4.16}$$

The simplified non-ideal admittance in the form of parallel RL circuit(when $Z_1 = R_1$, $Z_2 = R_2$, $Z_3 = \frac{1}{sC_3}$) for Circuit 1 & Circuit 2 and Circuit 3 & Circuit 4 are derived in equation (4.15) and (4.16) can be formulated as:

$$\frac{I_{in}}{V_{in}} = \frac{R_X + (R_Y + R_1)(1 + sC_X R_X)}{R_X(R_Y + R_1)} + \frac{R_X^2}{sC_3 R_X(R_Y + R_1)(R_Z + R_2 + R_Y)\left(R_X + \frac{1+sC_X R_X}{sC_3}\right)} \tag{4.17}$$

$$\frac{I_{in}}{V_{in}} = \frac{R_X + (R_Y + R_1)(1 + sC_X R_X)}{R_X(R_Y + R_1)} - \frac{R_X^2}{sC_3 R_X(R_Y + R_1)(R_Z + R_2 + R_Y)\left(R_X + \frac{1+sC_X R_X}{sC_3}\right)} \tag{4.18}$$

Equations (4.17) and (4.18) reveal that the admittance of the proposed parallel RL circuit is affected by the parasitic resistance and parasitic capacitance of the VCIIs, particularly noticeable at lower frequencies. Mitigating this influence involves

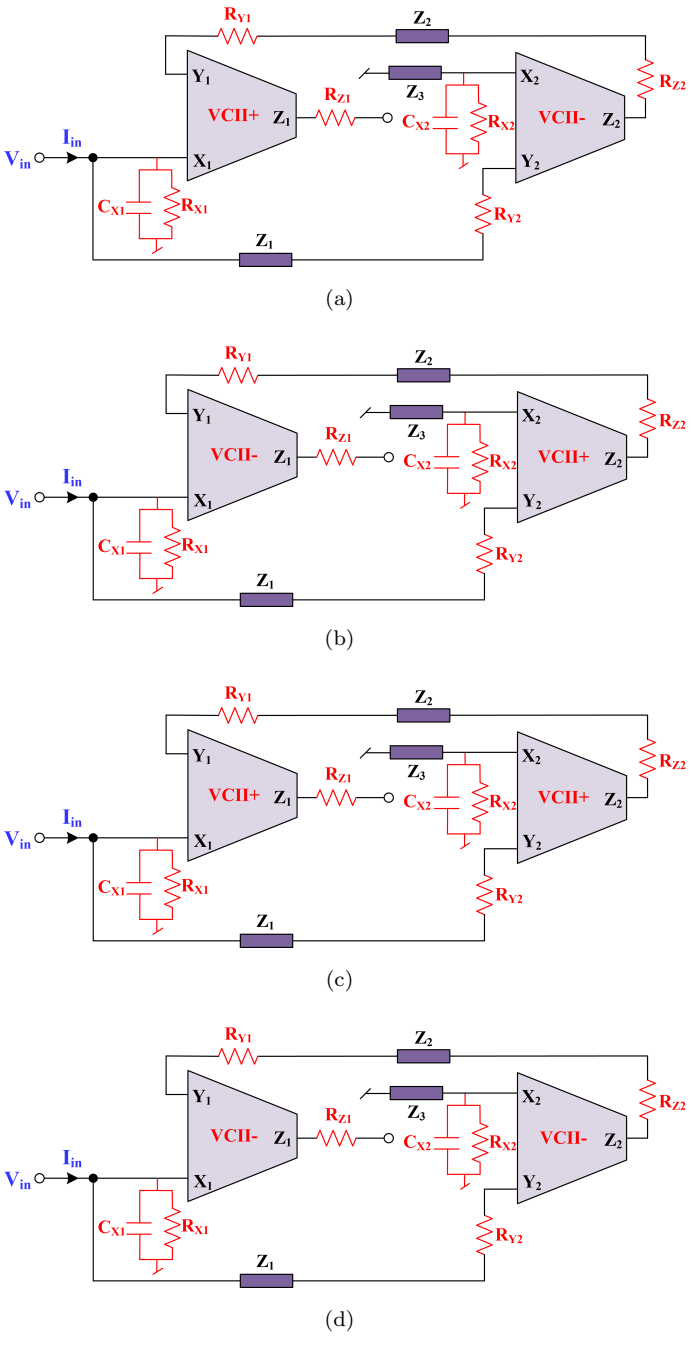


Figure 4.67: Complete proposed generalized grounded parallel immittance simulators with parasitic elements of VCII (a) Circuit-1 (b) Circuit-2 (c) Circuit-3 (d) Circuit-4

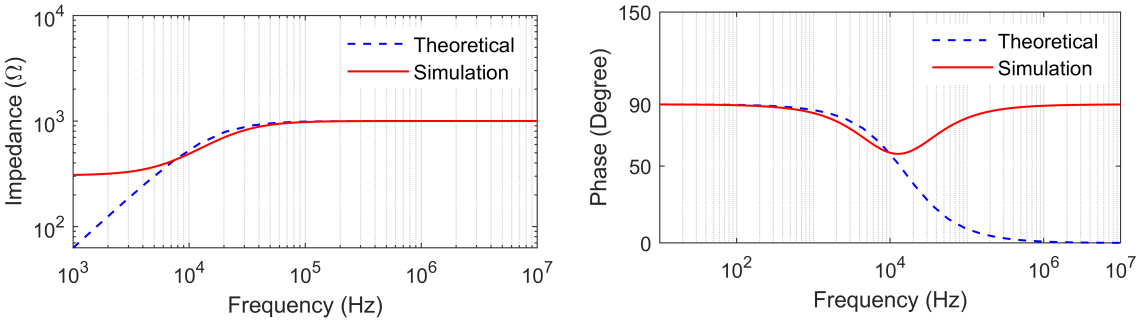
selecting appropriate external components, as explained in the simulation section, while taking into account the parasitic resistance and capacitance values of the VCIIs (e.g., $R_X = 23.729\text{M}\Omega$, $C_X = 670\text{pF}$, $R_Y = 4.6\Omega$, and $R_Z = 4.4\Omega$).

4.3.2 Simulation results using CMOS VCII

To confirm the operational effectiveness of the proposed grounded parallel immittance simulator circuits, we employed CMOS VCII+ and VCII- configurations, implemented with 0.18µm TSMC technology specifications, as shown in Fig. 4.9. The PMOS and NMOS transistor aspect ratios in Fig. 4.9 were set at 40.5µm/0.54µm and 13.5µm/0.54µm, respectively. The DC power supply voltages used to bias VCII+ and VCII- were ±0.9V, and the biasing currents I_{B0} and I_{B1} were both selected as 25µA. To confirm the effectiveness of all the immittance simulator circuits depicted in Fig. 4.65, a comprehensive validation process was undertaken. This validation encompassed multiple analyses, including assessments of impedance magnitude and phase responses, evaluations of time-domain behaviors for input voltage and current, and Monte-Carlo simulations.

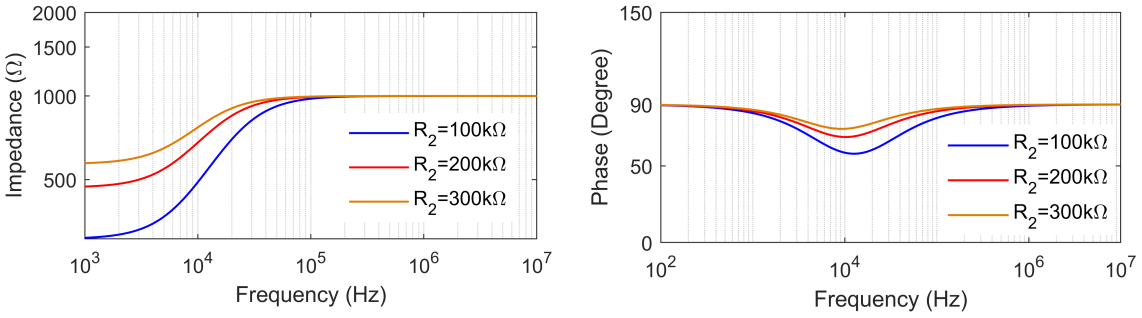
4.3.2.1 Results for Circuit-1

To simulate the parallel RL immittance simulator, we opted for the following specific values for the passive components: $R_1 = 1\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, and $C_3 = 100\text{pF}$. These chosen values led to equivalent resistance (R_{eq}) and equivalent inductance (L_{eq}) values of 1kΩ and 10mH, respectively. Fig. 4.68 illustrates the theoretical and simulated frequency responses of impedance and phase. To further investigate the characteristics of the parallel R-L circuits, we introduced variations in the value of resistor R_2. We considered resistor values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ. The



(a) (b)

Figure 4.68: Frequency responses of parallel RL simulator



(a) (b)

Figure 4.69: Frequency responses of parallel R-L simulator for different values of R_2

resulting variation in impedance and phase are showcased in Fig. 4.69. From Fig. 4.68, the simulated frequency responses for impedance and phase of the parallel RL circuit of Fig. 4.65 (Circuit-1) align closely with the theoretical expectations within a frequency range of 10kHz to 10MHz for impedance and 1Hz to 10kHz for phase responses. Furthermore, the proposed parallel RL simulator underwent Monte-Carlo analysis. This analysis involved introducing a 10% variation in resistor R_2, and the resulting variations in impedance and phase are depicted in Fig. 4.70. Additionally, Fig. 4.71 shows the time-domain responses of both input current and voltage for the parallel RL simulator. In this evaluation, a sinusoidal input voltage with an amplitude of 100mV and a frequency of 10kHz was applied.

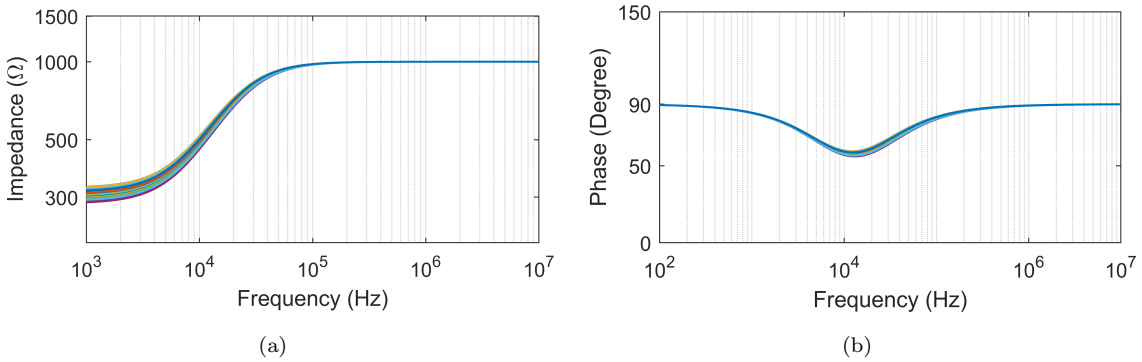


Figure 4.70: AC Monte-Carlo results of parallel RL simulator

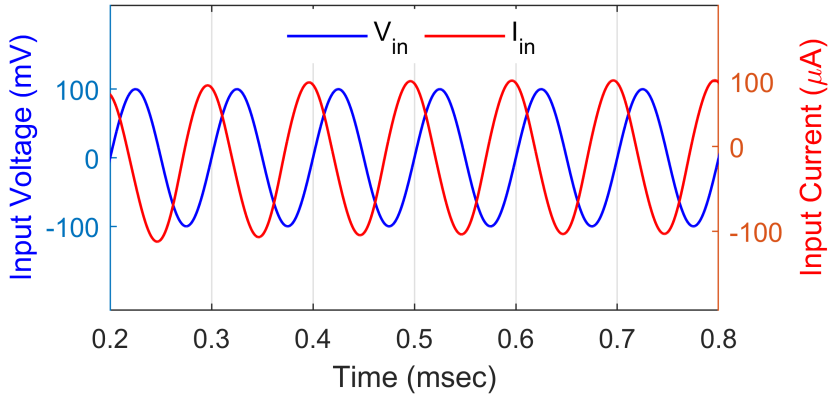
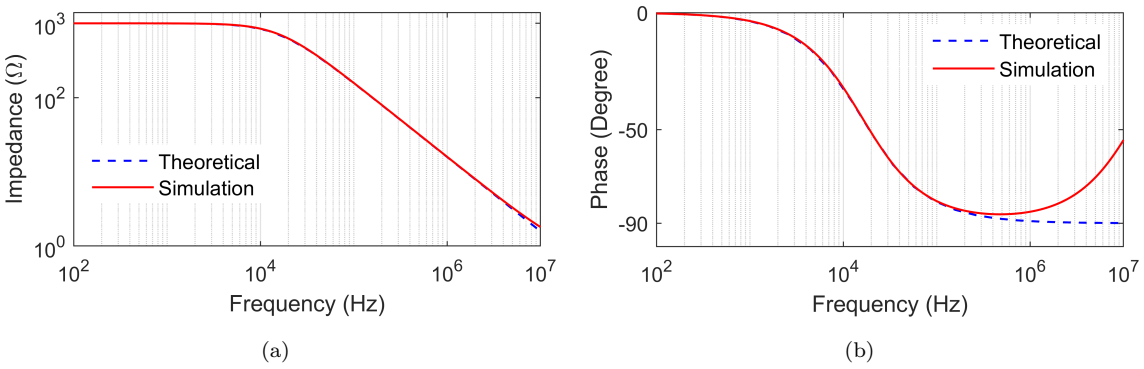


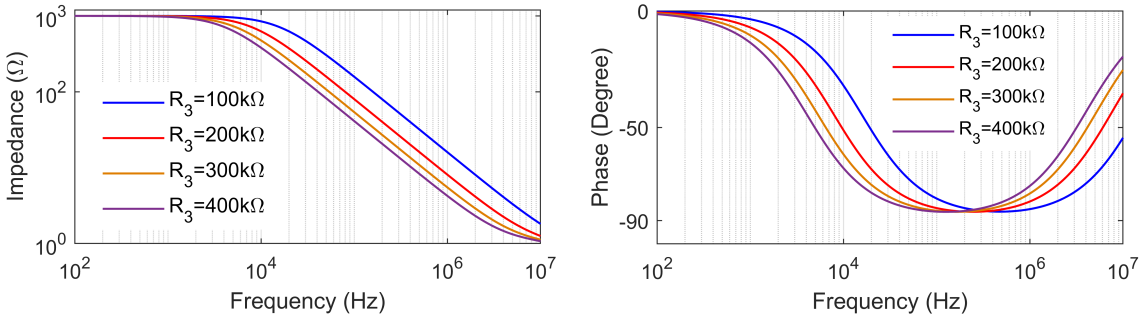
Figure 4.71: Transient responses of parallel RL simulator

In order to analyze the parallel RC immittance simulator of Fig. 4.65 (Circuit-1), simulations were carried out with specific passive component values: R_1 = 1kΩ, R_3 = 100kΩ, and capacitor C_2 = 100pF. These choices resulted in equivalent resistance (R_{eq}) and equivalent capacitance (C_{eq}) values of 1kΩ and 10nF, respectively. The resultant magnitude and phase responses are presented in Fig. 4.72. For a more comprehensive exploration of the parallel RC circuit, we performed variations in the value of resistor R_3. Specifically, we considered resistor values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ. The corresponding variations in parallel RC circuit impedance and phase responses are illustrated in Fig. 4.73. Observing Fig. 4.72, it is clear that the simulated frequency responses of the parallel RC simulator circuit align with the theoretical evaluations from 100Hz to 10MHz. Fig. 4.74 displays the simulation



(a) (b)

Figure 4.72: Theoretical and simulated frequency responses of parallel R-C simulator

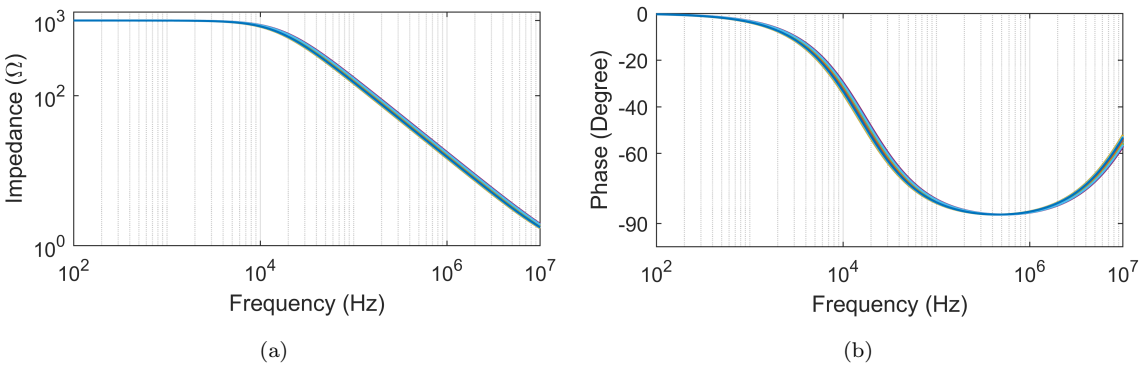


(a) (b)

Figure 4.73: The change in (a) impedance and (b) phase of parallel RC simulator of Circuit-1 for different value of R3

results of impedance and phase of the parallel RC circuit, derived from the Monte-Carlo analysis. In the time-domain analysis, an input voltage of sinusoidal form with an amplitude of 100 mV and a frequency of 10 kHz was utilized, with the resulting input voltage and current waveforms depicted in Fig. 4.75.

To verify the effectiveness of the proposed parallel CD circuit depicted in Fig. 4.65 (Circuit-1), the frequency responses of impedance magnitude and phase were measured using C_1 = 100pF, C_2 = 100pF, and R_3 = 1kΩ. The obtained frequency response is presented in Fig. 4.76. Additionally, Fig. 4.77 illustrates the variations in impedance magnitude and phase, showcasing the impact of different resistor values (1kΩ, 2kΩ, 3kΩ, 4kΩ) on the Circuit-1 performance. Observing Fig. 4.76



(a) (b)

Figure 4.74: AC Monte-Carlo results of parallel RC simulator of Circuit-1 (a) magnitude responses (b) Phase responses

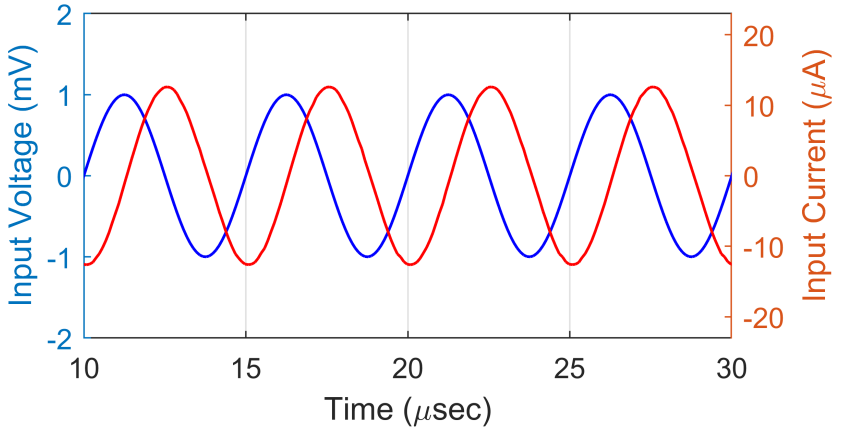
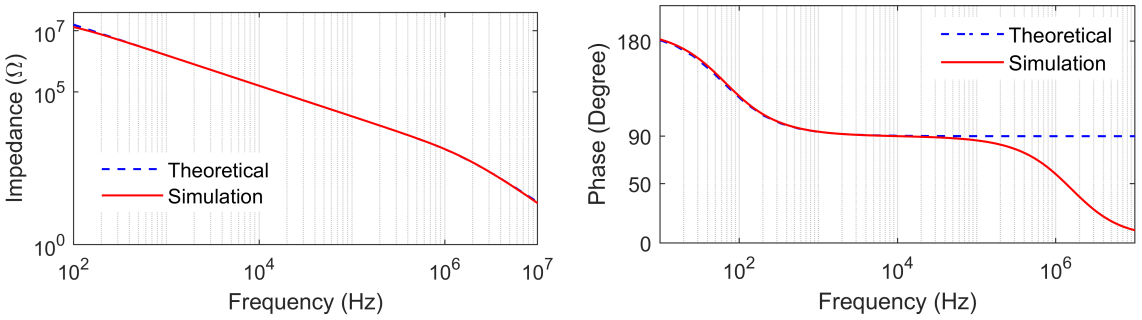


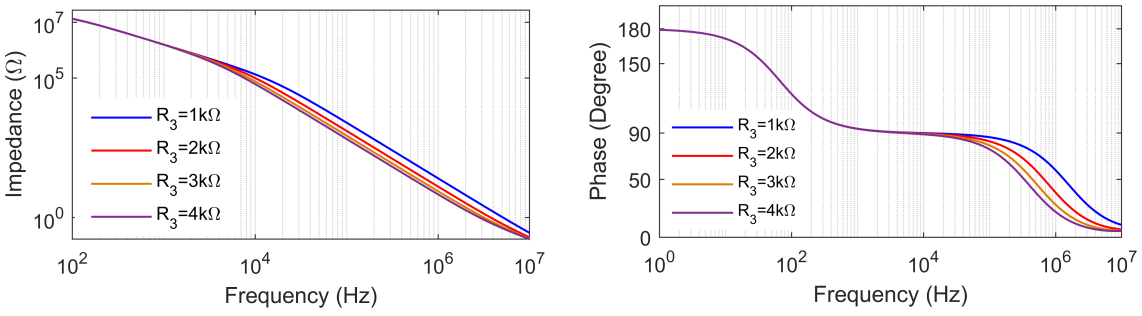
Figure 4.75: Time-domain input voltage and current responses for a parallel RC simulator

reveals that the simulated impedance closely corresponds to the theoretical values throughout the frequency ranging from 100Hz to 10MHz. Moreover, the phase closely matches between the frequencies of 1Hz to 500kHz. Monte Carlo analysis was conducted, and the outcomes are depicted in Fig. 4.78. An input voltage of sinusoidal form with an amplitude of 100 mV and a frequency of 100 kHz was employed to analyze the time-domain responses of the input current and voltage. The corresponding results are illustrated in Fig. 4.79. Simulation results for the capacitance multiplier circuit in Fig. 4.65 (Circuit-1) were conducted using the following passive component values: C_1 = 100pF, R_2 = 1kΩ and R_3 = 100kΩ which resulted in equivalent capacitance (C_{eq}=10.1nF). The impedance and



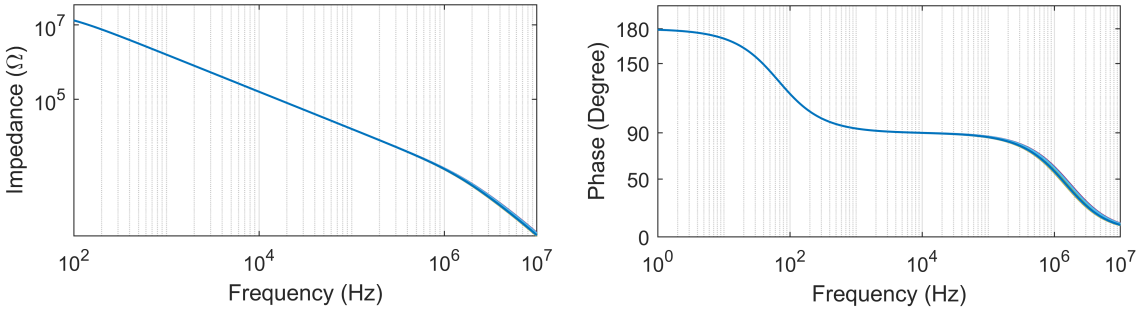
(a) (b)

Figure 4.76: Frequency responses of the parallel CD simulator of Circuit-1



(a) (b)

Figure 4.77: Variation in frequency responses of parallel CD simulator



(a) (b)

Figure 4.78: AC Monte-Carlo results of parallel C-D simulator

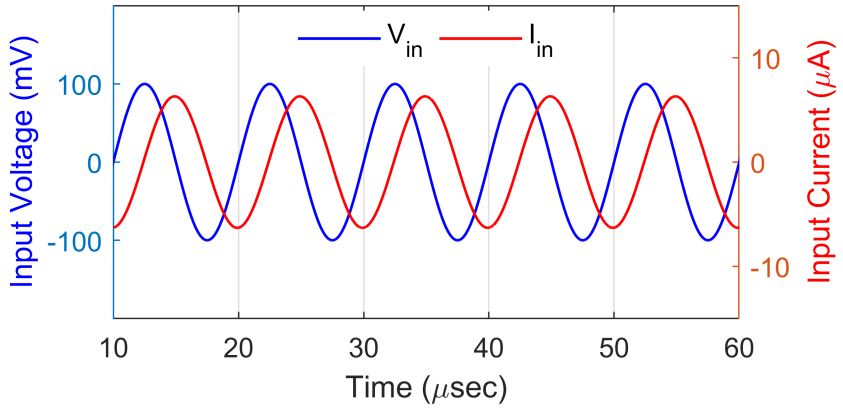
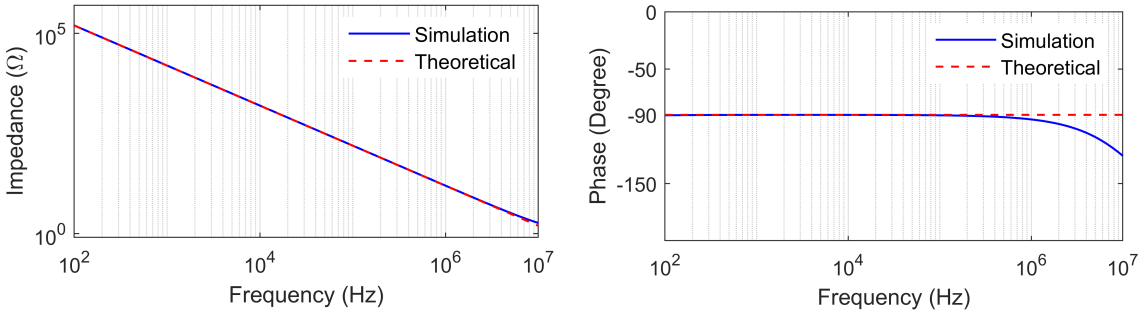


Figure 4.79: Transient responses for parallel C-D simulator of Circuit-1

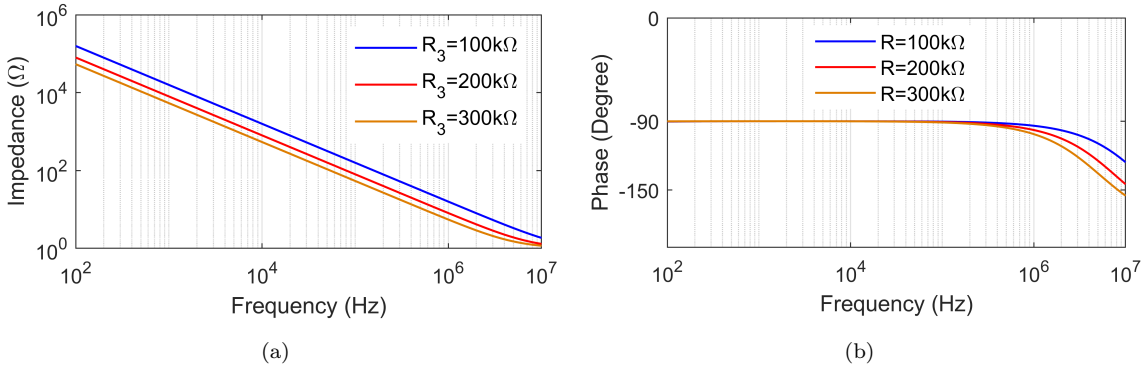


(a) (b)

Figure 4.80: Frequency responses of capacitance multiplier circuit of Circuit-1 (a) impedance and (b) phase

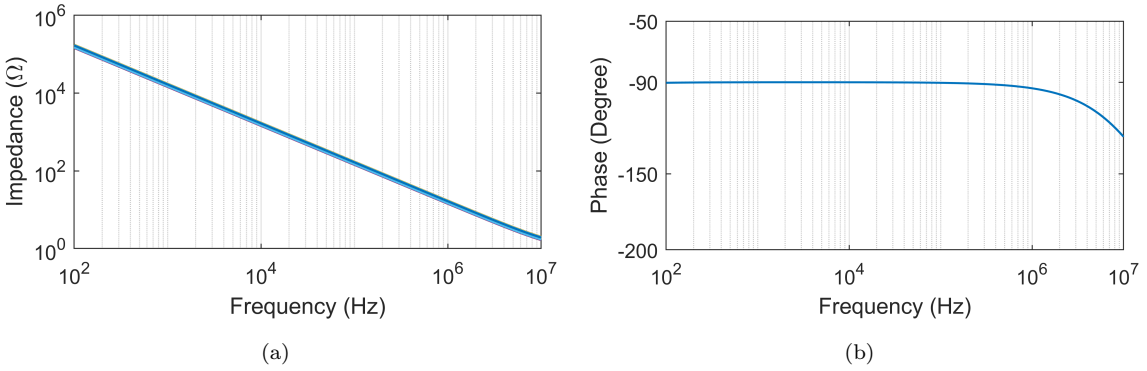
phase responses are displayed in Fig. 4.80. To further explore the workability of the capacitance multiplier circuit, we varied the value of resistor R_3, considering values of 100kΩ, 200kΩ and 300kΩ. The corresponding variations in impedance and phase responses are depicted in Fig. 4.81.

Observing Fig. 4.80, it is apparent that the simulation results of impedance and phase closely correspond to the theoretical values across frequency ranges of 100Hz - 10MHz and 100Hz -1MHz, respectively. Fig. 4.82 presents the magnitude and phase responses of the capacitance multiplier, obtained through Monte Carlo analysis. In Fig. 4.83(a), the equivalent capacitance for different resistance values in the capacitance multiplier circuit is illustrated. Specifically, resistor R_3 is varied across



(a) (b)

Figure 4.81: Frequency responses of capacitance multiplier circuit for different value of resistors (a) magnitude (b) phase



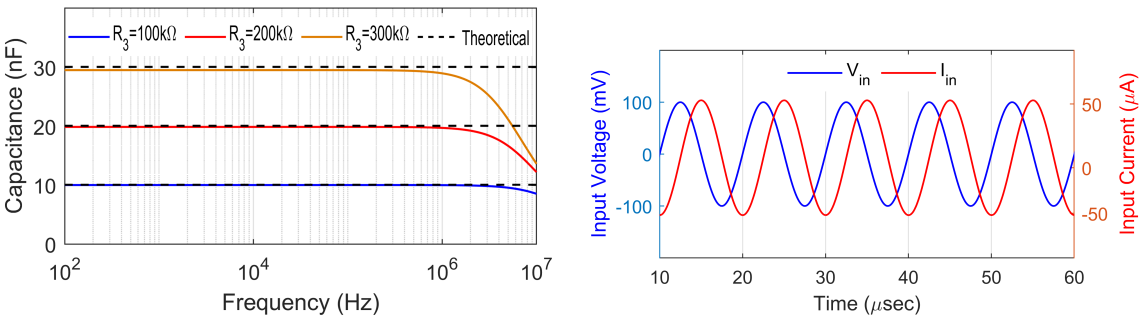
(a) (b)

Figure 4.82: AC Monte-Carlo results of capacitance multiplier

values of 100kΩ, 200kΩ, and 300kΩ, while maintaining R_2 at 1 kΩ and C_1 at 100pF, resulting in C_{eq} values of 10.1nF, 20.1nF, and 30.1nF respectively. An input voltage of sinusoidal form with a frequency of 100kHz and an amplitude of 100mV was used in the time-domain analysis. The resulting input voltage and current waveforms are depicted in Fig. 4.83(b).

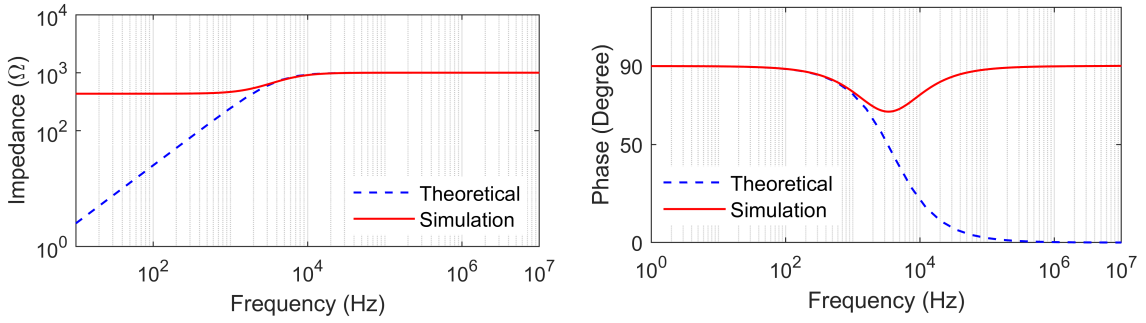
4.3.2.2 Results for Circuit 2

We employed passive components to simulate the parallel R-L circuit, specifically R_1 = 1kΩ, R_2 = 100kΩ, and C_3 = 100pF. Fig. 4.84 illustrates the simulated frequency responses of the impedance and phase of the simulator, accompanied by theoretical



(a) (b)

Figure 4.83: (a) Variations in capacitance of Fig. 4.65 (Circuit-1) (b) Transient responses of capacitance multiplier circuit

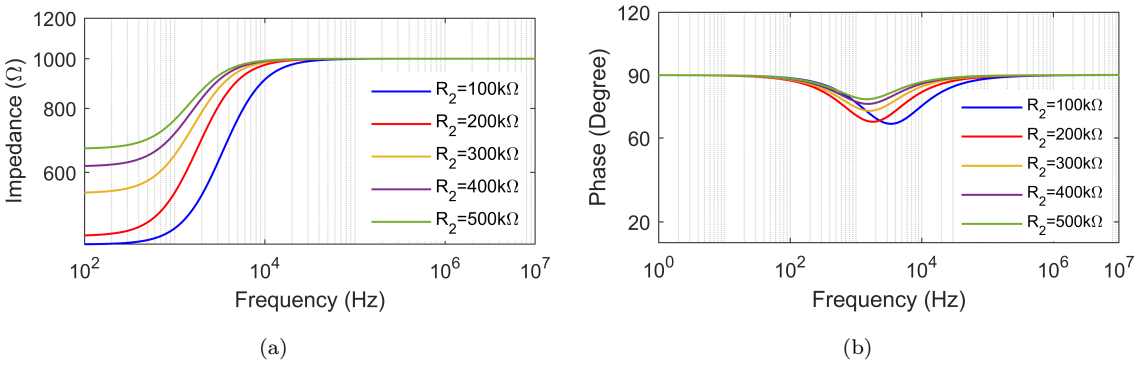


(a) (b)

Figure 4.84: Frequency responses of parallel RL simulator of Circuit-2

assessments. Fig. 4.85 illustrates the fluctuations in impedance and phase values of the parallel R-L circuit when the resistance R_2 is altered from 100kΩ to 500kΩ. Fig. 4.86 illustrates the transient responses of input voltage and current for a sinusoidal voltage with an amplitude of 50mV and a frequency of 10 kHz.

Fig. 4.84,demonstrate that the simulated outcomes of the parallel R-L circuit align accurately with the theoretical assessments within the frequency range of 10kHz to 10MHz for impedance and 1Hz to 10kHz for phase response. The proposed parallel R-L circuit was additionally simulated for Monte Carlo analysis. A 10% tolerance was added to resistor R_2 in the Monte-Carlo analysis, with the resultant magnitude and phase depicted in Fig. 4.87. Simulations analogous to those performed for a parallel R-L circuit have been executed for the proposed parallel R-C simulator of



(a) (b)

Figure 4.85: Frequency responses of parallel R-L simulator of Circuit-2 for different values of R_2

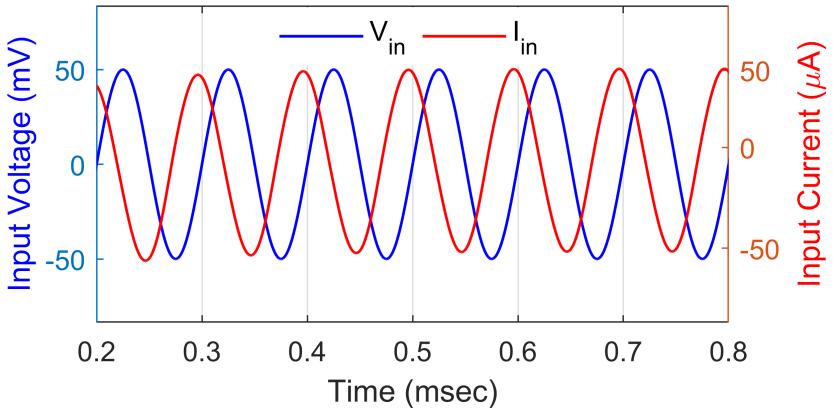
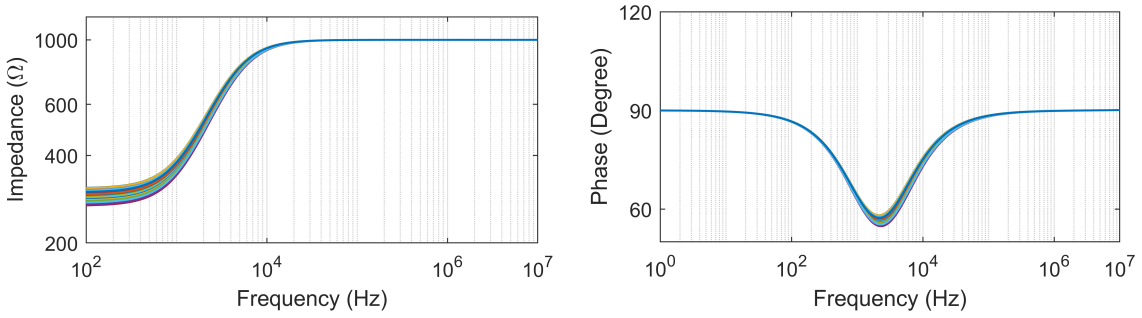


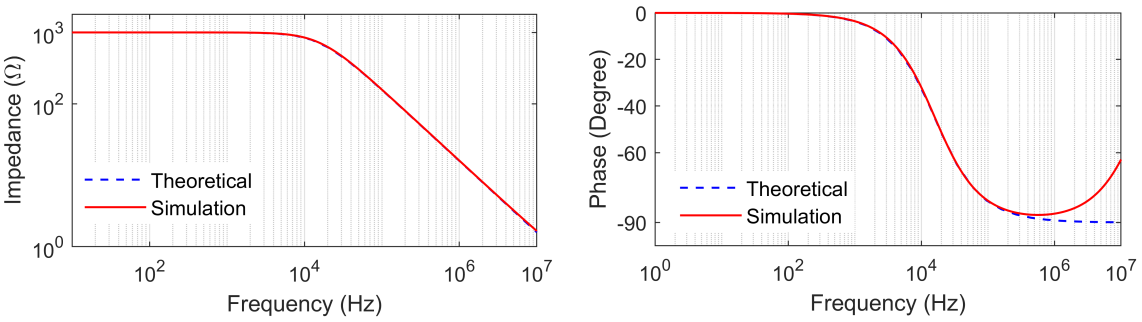
Figure 4.86: Transient responses for parallel RL simulator of Circuit-2

Circuit-2. The passive component values utilized in the simulations were $R_1 = 1\text{k}\Omega$, $R_3 = 100\text{k}\Omega$, and $C_2 = 100\text{pF}$, yielding equivalent resistance (R_{eq}) and capacitance (C_{eq}) values of 1kΩ and 10nF, respectively.Impedance and phase values change when R_3 is changed from 100kΩ to 500kΩ have been shown in Fig. 4.88 As seen in Fig. 4.88, the simulated frequency responses of the parallel RC simulator closely match the theoretical predictions, with good agreement observed from 1 Hz to 10 MHz for impedance and from 1 Hz to 500 kHz for phase. Fig. 4.90 presents the simulation results for the impedance and phase of the parallel RC circuit obtained through Monte Carlo analysis. A sinusoidal input voltage of 10mV magnitude and 100kHz frequency was applied to examine the impact of time-domain analysis shown in Fig.



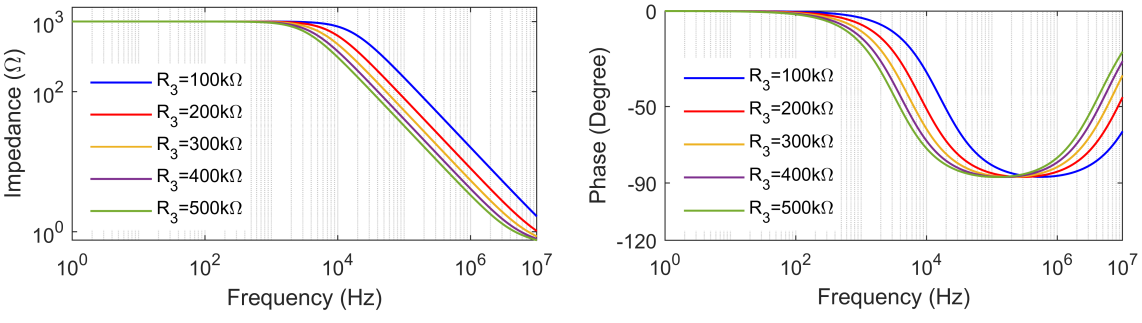
(a) (b)

Figure 4.87: AC Monte-Carlo results of parallel RL of Circuit-2



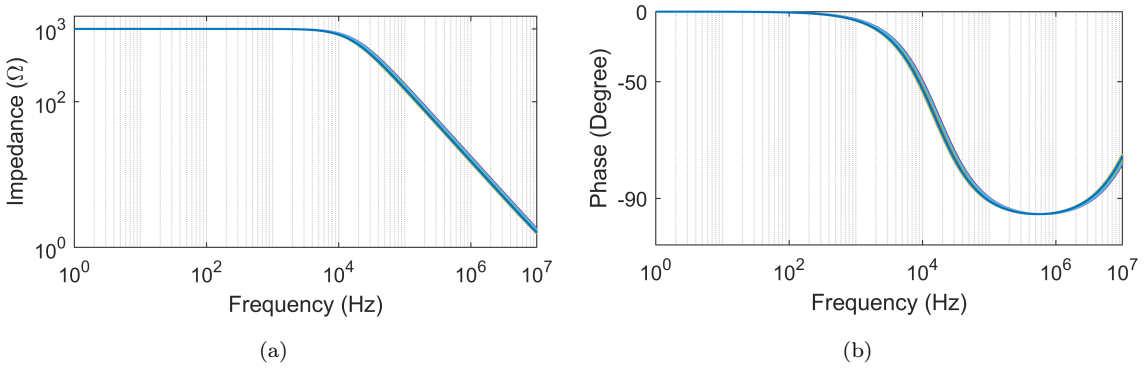
(a) (b)

Figure 4.88: Theoretical and simulated frequency responses of parallel R-C simulator of Circuit-2



(a) (b)

Figure 4.89: The change in (a) impedance and (b) phase of parallel RC simulator of Circuit-2 for different value of R_3



(a) (b)

Figure 4.90: AC Monte-Carlo results of parallel RC simulator of Circuit-2 (a) magnitude responses (b) Phase responses

4.91.

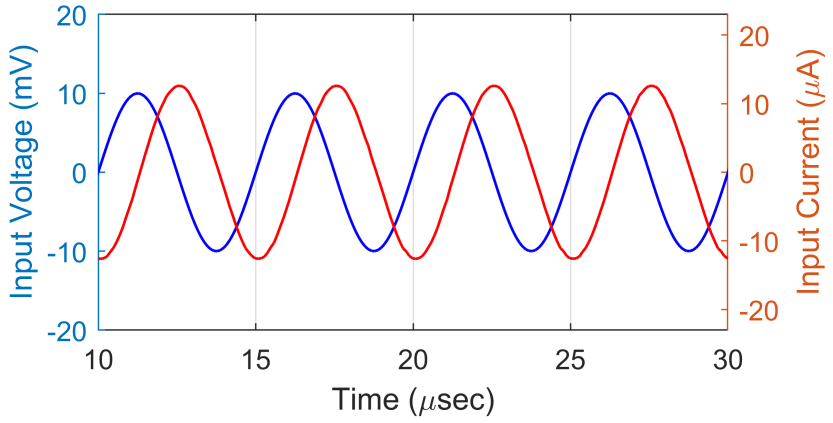
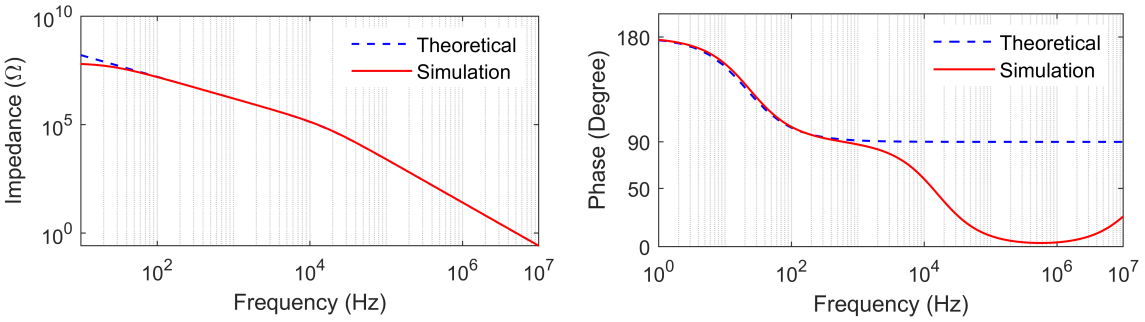


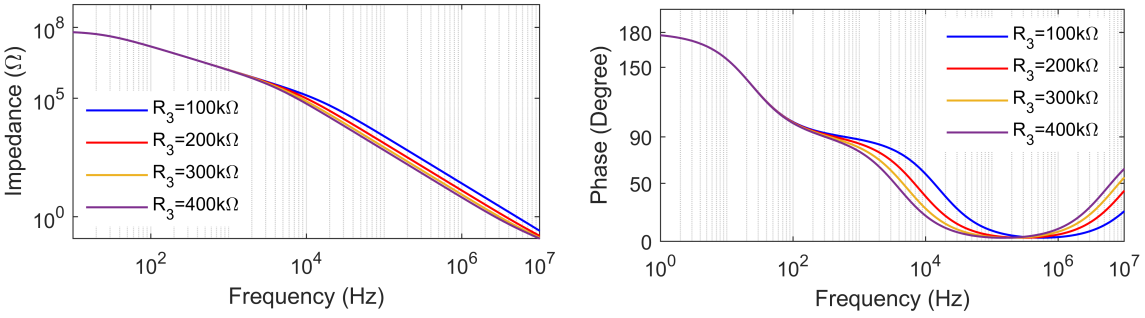
Figure 4.91: Time-domain input voltage and current responses for a parallel RC simulator of Circuit-2

To verify the performance of the proposed parallel C-D simulator circuit, the frequency responses of impedance magnitude and phase, the variations in impedance magnitude and phase for different values of R_3, the transient responses of input voltage and current and Monte-carlo analysis are presented. For simulation purposes, the passive component values were set as $C_1 = 100$ pF, $C_2 = 100$ pF, and $R_3 = 100$ kΩ. A sinusoidal input voltage with an amplitude of 10 mV at 200 kHz was applied to observe the transient behavior. The corresponding results are shown in Fig. 4.92 to Fig. 4.95.



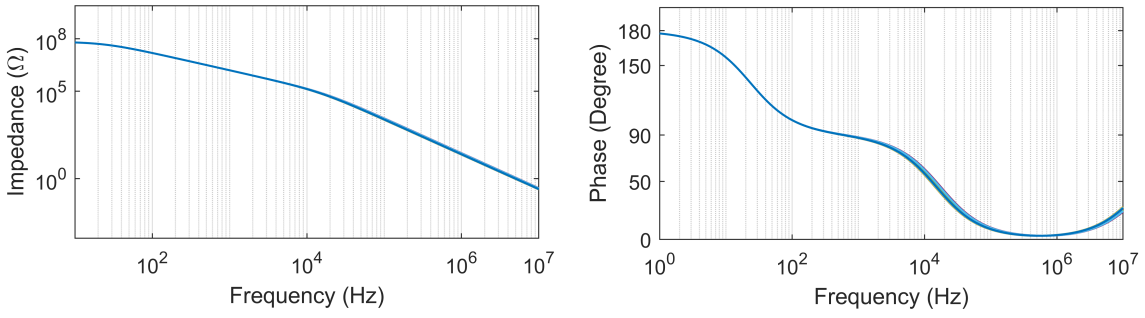
(a) (b)

Figure 4.92: Frequency responses of the parallel CD simulator of Circuit-2



(a) (b)

Figure 4.93: Variation in frequency responses of parallel CD simulator



(a) (b)

Figure 4.94: AC Monte-Carlo results of parallel C-D simulator

The frequency analysis of the proposed capacitance multiplier of Circuit-2, was performed using passive component values of $C_1 = 100$ pF, $R_2 = 1$ kΩ, and $R_3 = 100$ kΩ. The corresponding magnitude and phase responses of the FCM's impedance are illustrated in Fig. 4.96. The frequency response of variation in impedance and

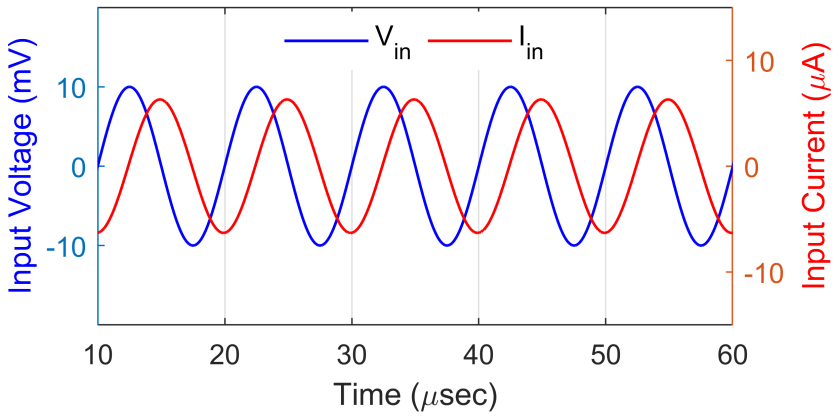
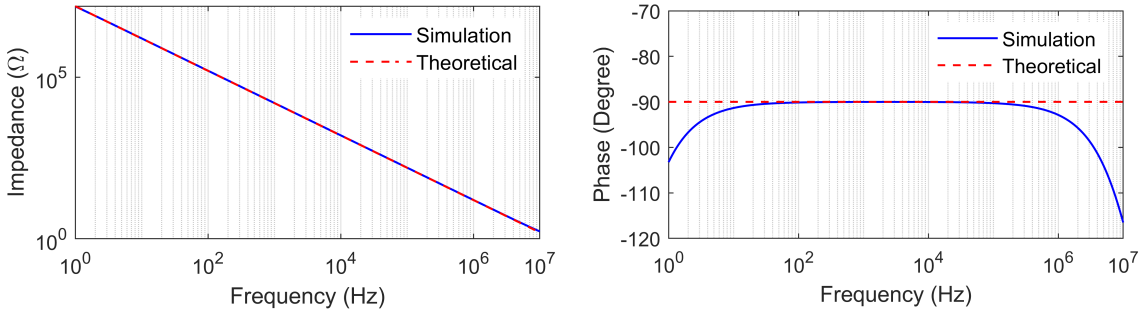


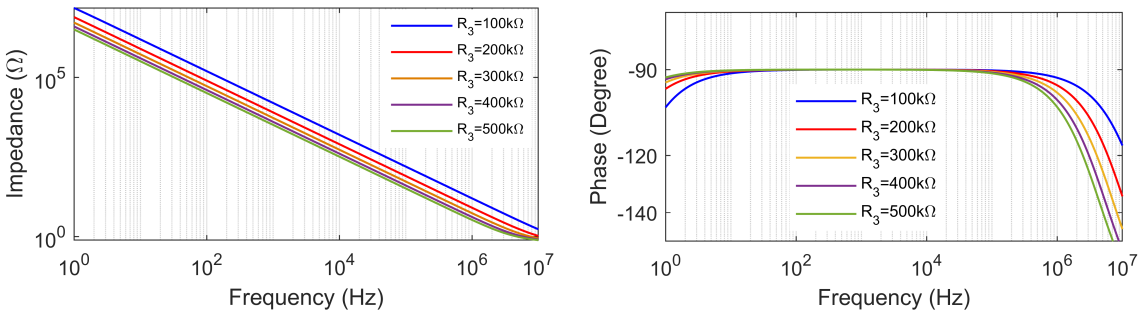
Figure 4.95: Transient responses for parallel C-D simulator of Circuit-2



(a) (b)

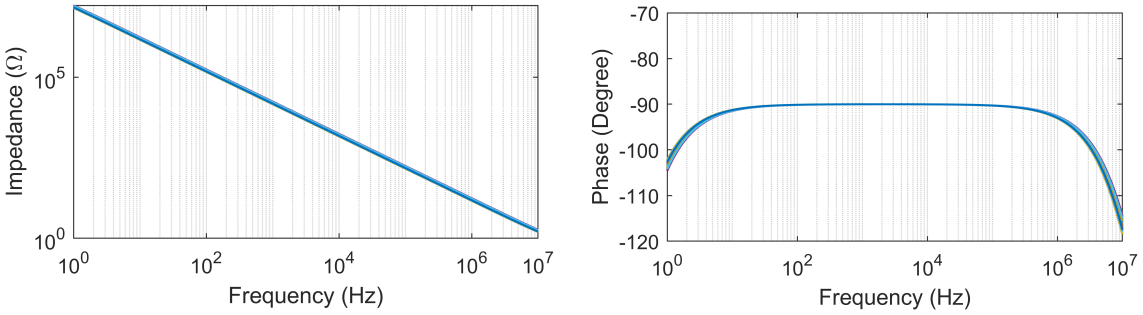
Figure 4.96: Frequency responses of capacitance multiplier circuit of Circuit-2 (a) impedance and (b) phase

phase for different value of resistor R_3 (100kΩ, 200kΩ, 300kΩ, 400kΩ and 500kΩ) have been shown in Fig. 4.97. Monte-Carlo simulations have been performed for the CM with 100 runs. The results have been shown in Fig. 4.98 in which the passive component values deviate uniformly with 10%. The equivalent capacitance for various resistance values was evaluated and is presented in Fig. 4.99(a), where R_3 was varied across 100 kΩ, 200 kΩ, 300 kΩ, 400 kΩ, and 500 kΩ, with R_2 fixed at 1 kΩ and C_1 at 100 pF, resulting in equivalent capacitances of 10.1 nF, 20.1 nF, 30.1 nF, 40.1 nF, and 50.1 nF, respectively. Additionally, Fig. 4.99(b) shows the time domain analysis for which a sinusoidal input voltage of magnitude 10mV at 100 kHz has been applied.



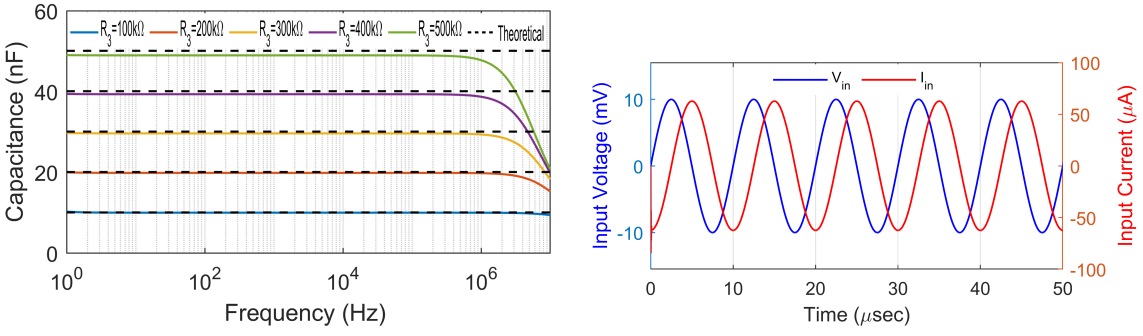
(a) (b)

Figure 4.97: Frequency responses of capacitance multiplier circuit for different value of resistors (a) magnitude (b) phase



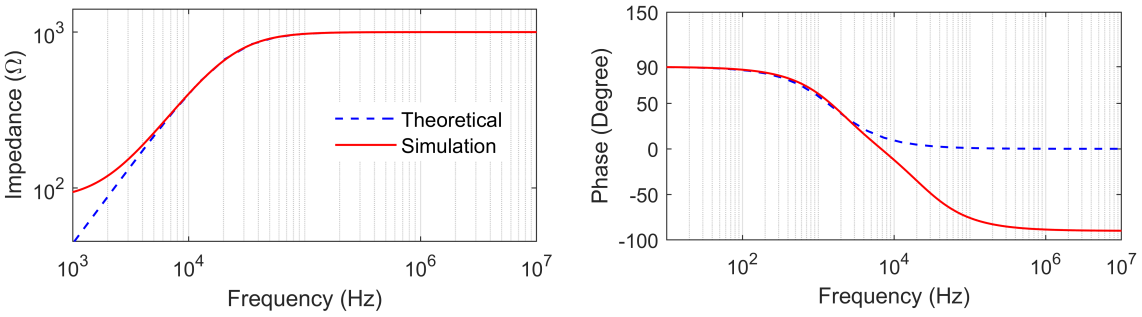
(a) (b)

Figure 4.98: AC Monte-Carlo results of capacitance multiplier



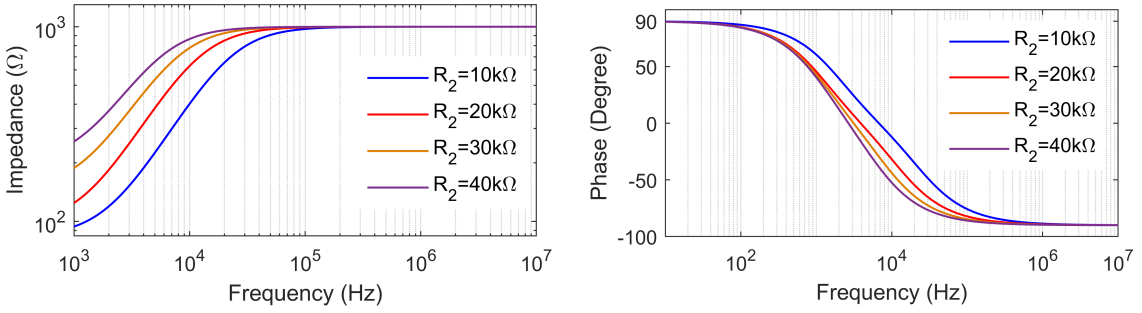
(a) (b)

Figure 4.99: (a) Variations in capacitance of Fig. 4.65(Circuit-2) (b) Transient responses of capacitance multiplier circuit



(a) (b)

Figure 4.100: Frequency responses of parallel RL simulator of Circuit-3

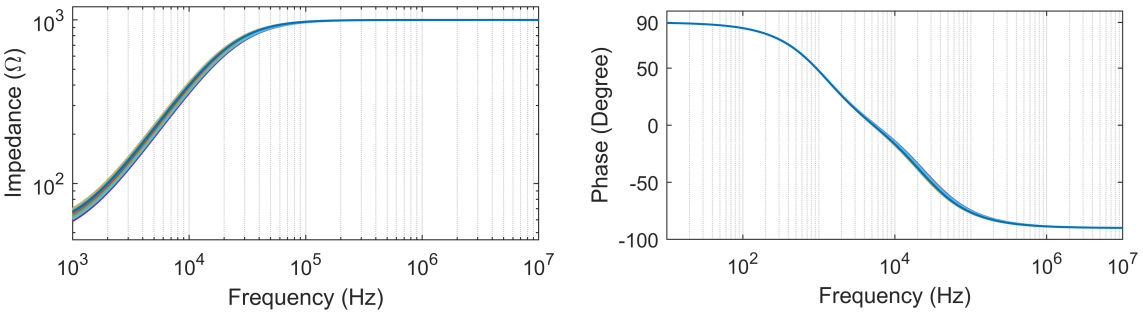


(a) (b)

Figure 4.101: Frequency responses of parallel R-L simulator of Circuit-3 for different values of R_2 (a) magnitude (b) phase

4.3.2.3 Results for Circuit-3

To simulate the parallel RL immittance simulator, we used $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, and $C_3 = 100\text{pF}$ for passive components. The selected values resulted in 1kΩ and 10mH equivalent resistance and inductance values. Fig. 4.100 shows theoretical and simulated impedance and phase frequency responses. We changed resistor R_2 to study parallel R-L circuits. We examined resistor values of 10kΩ, 20kΩ, 30kΩ, and 40kΩ. Fig. 4.101 shows the impedance and phase variation. Fig. 4.100 shows that the parallel RL circuit of Fig. 4.65 (Circuit-3) simulated frequency responses for impedance and phase match theoretical predictions within a frequency range of 10kHz to 10MHz for impedance and 1Hz to 10kHz for phase. The suggested parallel



(a) (b)

Figure 4.102: AC Monte-Carlo results of parallel R-L simulator of Circuit-3 (a) magnitude responses (b) Phase responses

RL simulator was Monte-Carlo analyzed. Fig. 4.102 shows the impedance and phase fluctuations caused by a 10% resistor R_2 variation. Additionally, Fig. 4.103 displays the parallel RL simulator's input current and voltage time-domain responses. In this evaluation, a 100mV sinusoidal input voltage was applied at 10kHz.

The parallel RC immittance simulator in Fig. 4.65 (Circuit-3) was analyzed using

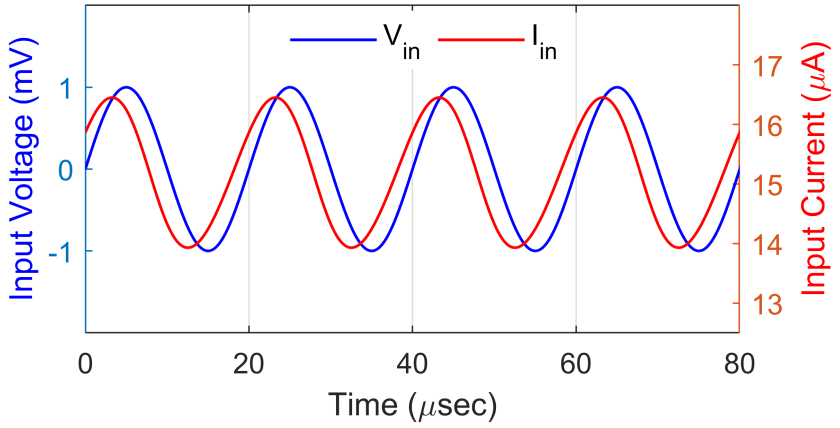
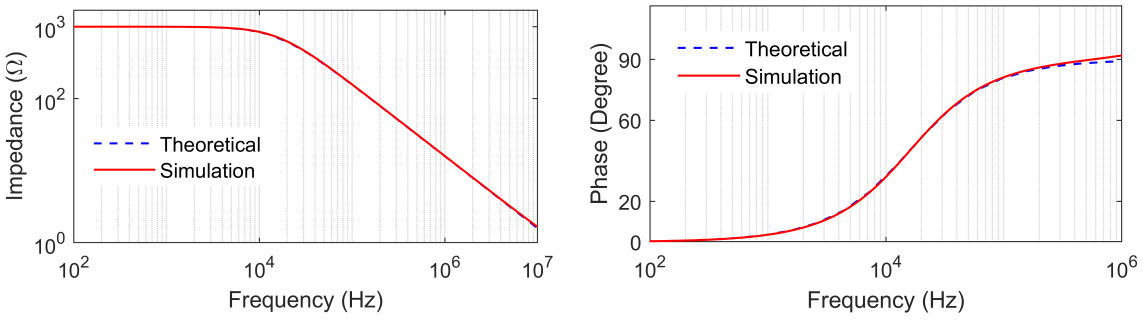


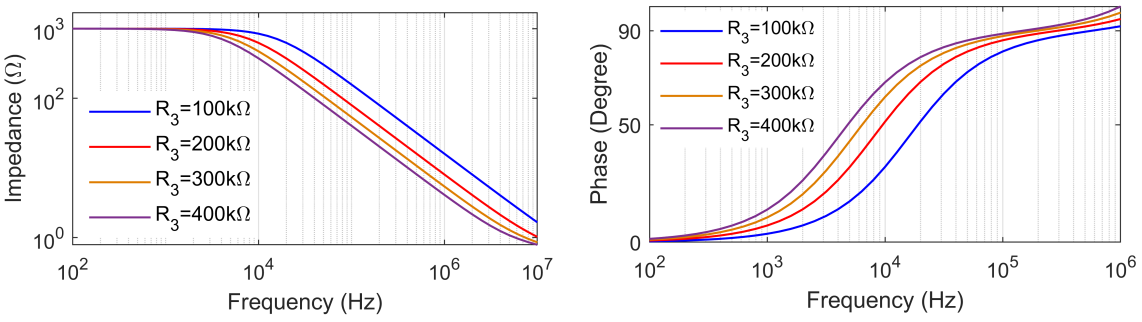
Figure 4.103: Transient responses of input voltage and current of parallel R-L simulator

particular passive component values: $R_1 = 1\text{k}\Omega$, $R_3 = 100\text{k}\Omega$, and $C_2 = 100\text{pF}$. Based on these options, the equivalent resistance (R_{eq}) and capacitance (C_{eq}) were 1kΩ and 10nF, respectively. Fig. 4.104 shows magnitude and phase responses. To better understand the parallel RC circuit, we changed resistor R_3. We examined



(a) (b)

Figure 4.104: Frequency responses of parallel RC simulator of Circuit-3

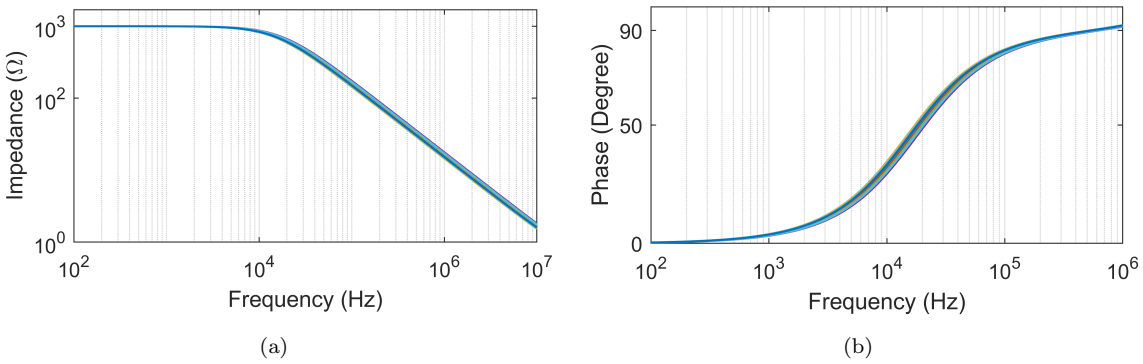


(a) (b)

Figure 4.105: Frequency responses of parallel R-C simulator of Circuit-3 for different values of R_3 (a) magnitude (b) phase

resistor values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ. Fig. 4.105 shows parallel RC circuit impedance and phase responses.

As shown in Fig. 4.104, the parallel RC simulator circuit's simulated frequency responses match theoretical values from 100Hz to 10MHz. The Monte-Carlo analysis simulation results for parallel RC circuit impedance and phase are shown in Fig. 4.106. The time-domain analysis used a sinusoidal input voltage with an amplitude of 100 mV and a frequency of 10 kHz, as shown in Fig. 4.107. To validate the parallel CD circuit in Fig. 4.65 (Circuit-3), frequency responses of impedance magnitude and phase were tested using $C_1 = 100$pF, $C_2 = 100$pF, and $R_3 = 10$kΩ. The frequency response is shown in Fig. 4.108. Fig. 4.109 shows how changing



(a) (b)

Figure 4.106: AC Monte-Carlo results of parallel R-C simulator of Circuit-3 (a) magnitude responses (b) Phase responses

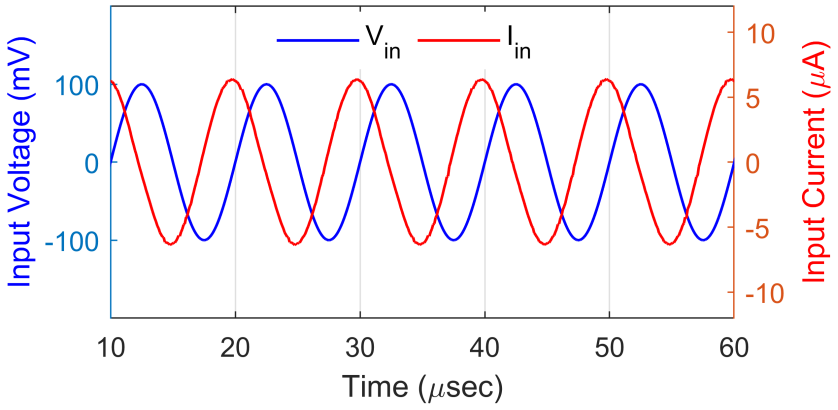
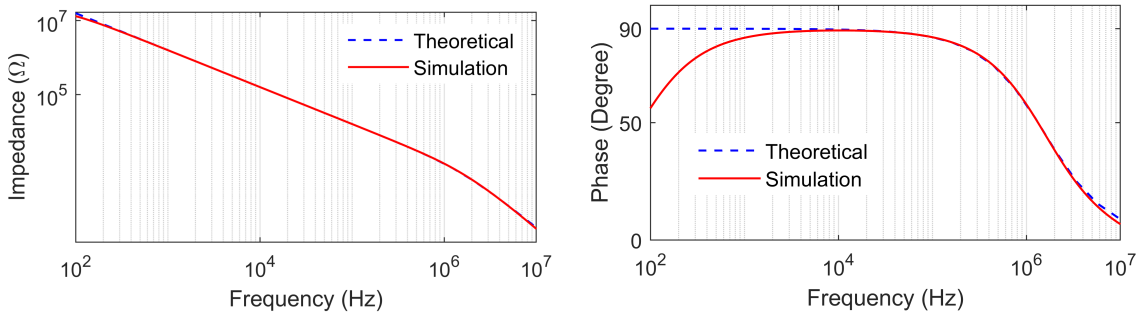


Figure 4.107: Transient responses of input voltage and current of parallel R-C simulator

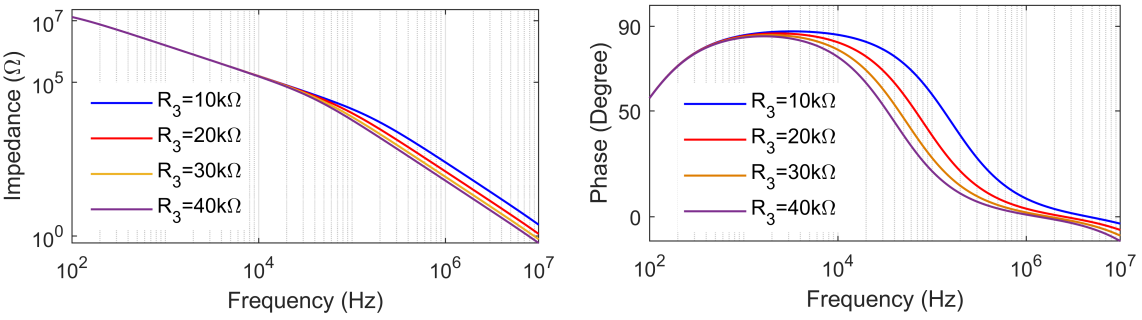
resistor values (10kΩ, 20kΩ, 30kΩ, 40kΩ) affect Circuit-3 performance by varying impedance magnitude and phase. Fig. 4.108 shows that the simulated impedance matches theoretical values from 100Hz to 10MHz. Phase is also close between 1Hz and 500kHz. Monte Carlo results are shown in Fig. 4.110. An input voltage of sinusoidal form with an amplitude of 100 mV and a frequency of 100 kHz was used to investigate the input current and voltage time-domain responses. Results are shown in Fig. 4.111.

Simulation results for Fig. 4.65(Circuit-3) capacitance multiplier circuit simulations used the following passive component values: Equivalent capacitance (C_{eq}=10.1nF) was achieved with $C_1 = 100$pF, $R_2 = 1$kΩ, and $R_3 = 100$kΩ. Fig. 4.112 shows phase and impedance responses. To test the capacitance multiplier circuit, we explored



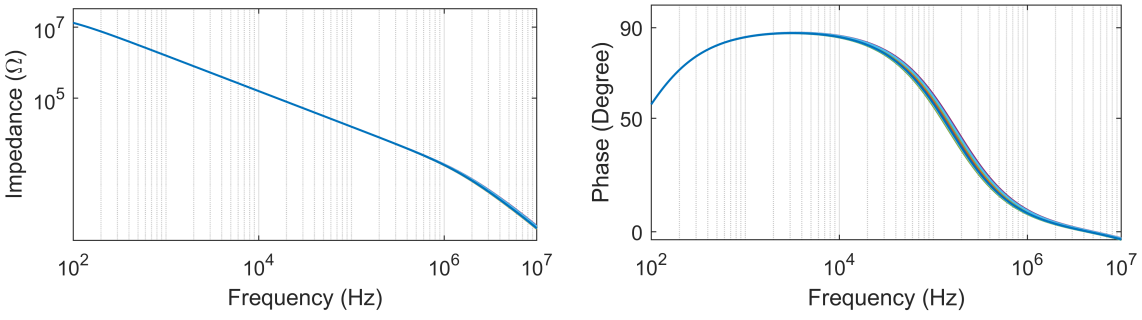
(a) (b)

Figure 4.108: Frequency responses of parallel CD simulator of Circuit-3



(a) (b)

Figure 4.109: Frequency responses of parallel C-D simulator of Circuit-3 for different values of R_3 (a) magnitude (b) phase



(a) (b)

Figure 4.110: AC Monte-Carlo results of parallel C-D simulator of Circuit-3 (a) magnitude responses (b) Phase responses

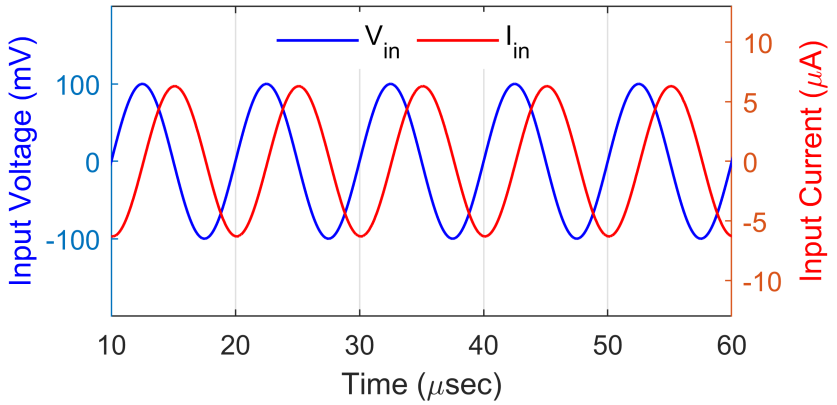
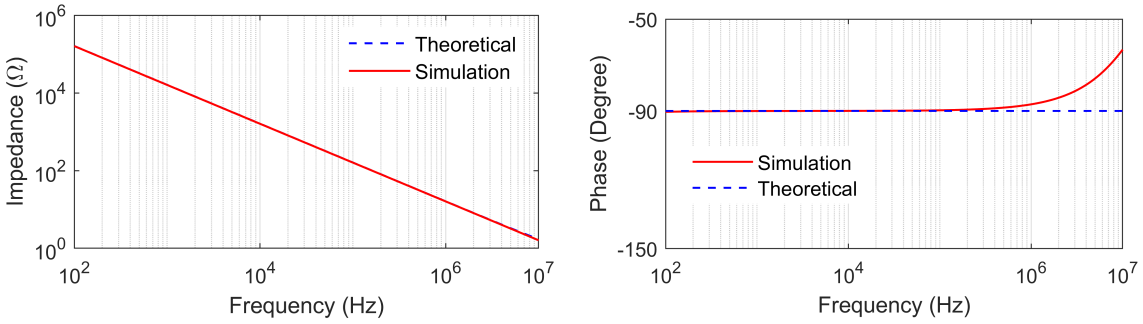


Figure 4.111: Transient responses of input voltage and current of parallel C-D simulator



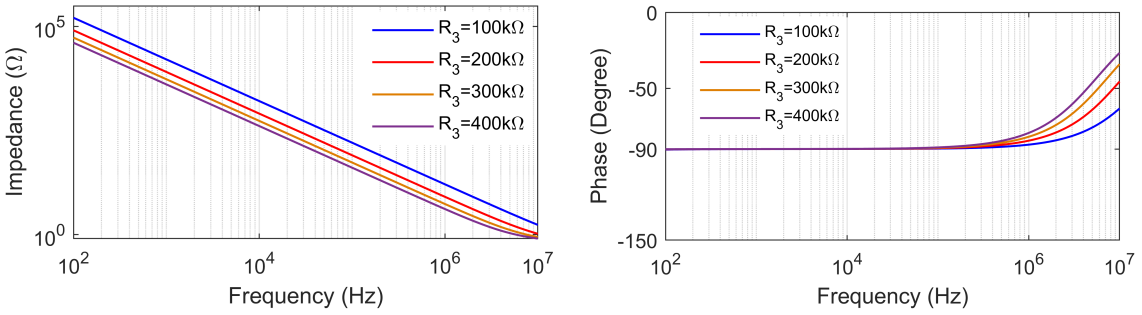
(a) (b)

Figure 4.112: Frequency responses of capacitance multiplier of Circuit-3

resistor R_3 values of 100kΩ, 200kΩ, and 300kΩ. Fig. 4.113 shows impedance and phase responses. In Fig. 4.112, the simulation findings of impedance and phase match the theoretical values over 100Hz -10MHz and 100Hz -1MHz frequency ranges. Monte Carlo analysis responses are shown in Fig. 4.114. Time-domain analysis employed a sinusoidal input voltage with a frequency of 100kHz and magnitude of 100mV. Fig. 4.115 shows the input voltage and current waveforms.

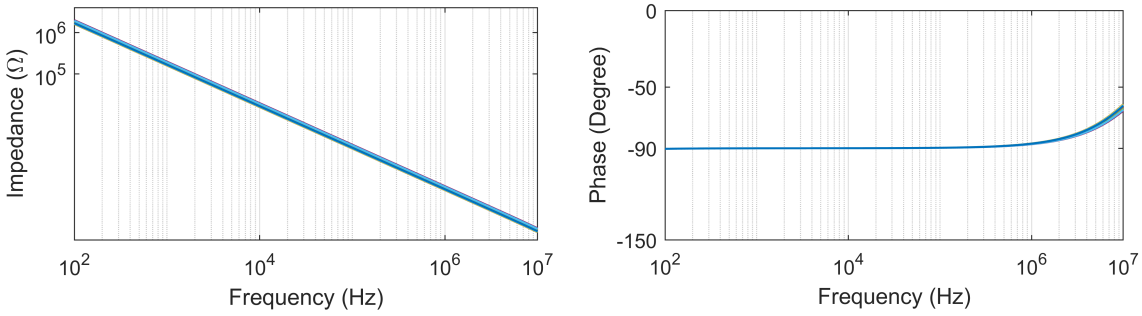
4.3.2.4 Results for Circuit-4

To simulate the parallel R-(-L) simulator of Circuit-4, we used passive component values of $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, and $C_3 = 100\text{pF}$. The equivalent resistance (R_{eq})



(a) (b)

Figure 4.113: Frequency responses of capacitance multiplier of Circuit-3 for different values of R_3 (a) magnitude (b) phase



(a) (b)

Figure 4.114: AC Monte-Carlo results of capacitance multiplier of Circuit-3 (a) magnitude responses (b) Phase responses

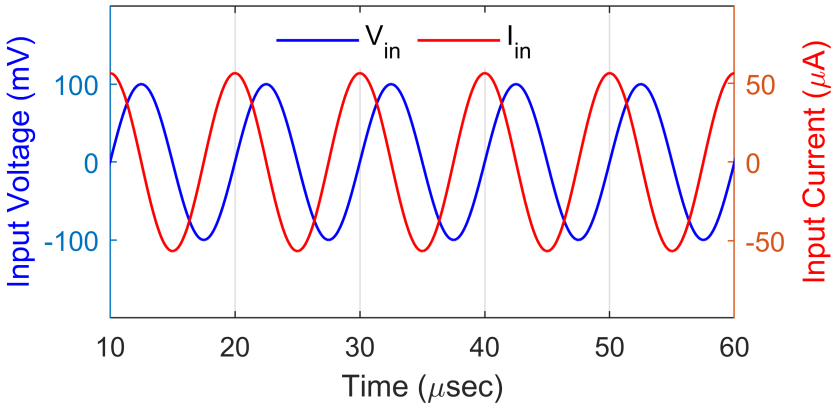
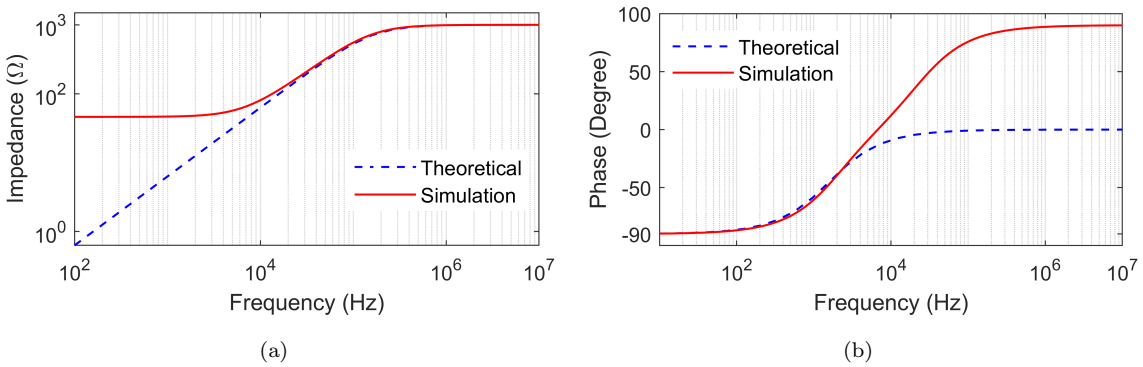


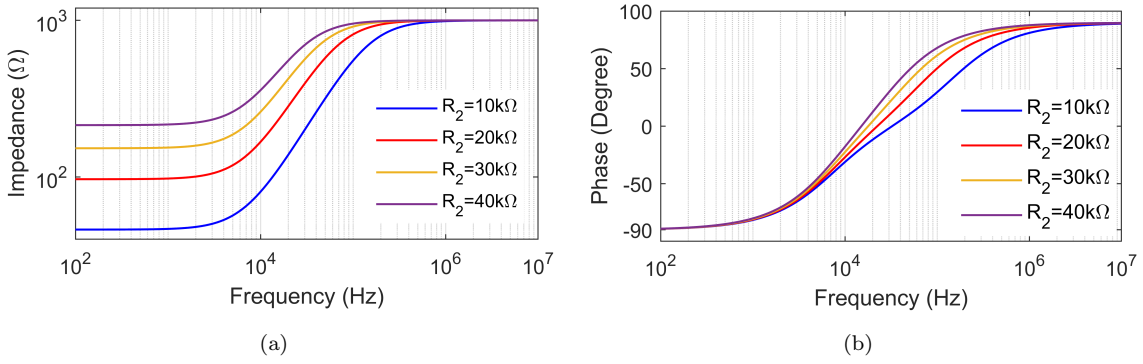
Figure 4.115: Transient responses of input voltage and current of capacitance multiplier of Circuit-3

and equivalent inductance (L_{eq}) values were 1kΩ and 1mH, respectively. Fig. 4.116



(a) (b)

Figure 4.116: Frequency responses of parallel R-(-L) simulator of Circuit-4

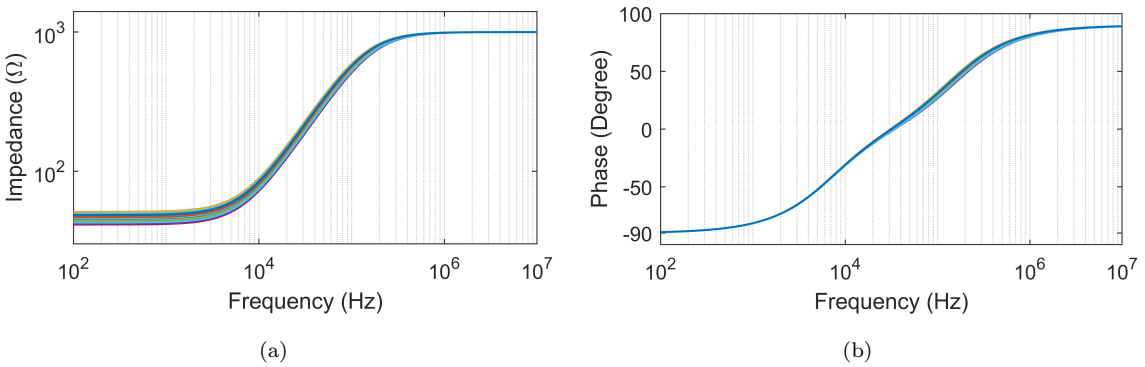


(a) (b)

Figure 4.117: Frequency responses of parallel R-(-L) simulator of Circuit-4 for different values of R_2 (a) magnitude (b) phase

shows theoretical and simulated impedance and phase frequency responses. To examine the functioning of parallel R-(-L) circuit, we tested resistor R_2 values of 10kΩ, 20kΩ, 30kΩ, and 40kΩ. Fig. 4.117 shows impedance and phase fluctuations.

Fig. 4.116 shows that the simulated frequency response of impedance and phase of the parallel R-(-L) circuit of Fig. 4.65 (Circuit-4) matches theoretical predictions up to 100Hz–10MHz for impedance and 1Hz-400kHz for phase. Monte-Carlo analysis was performed on the proposed parallel R-(-L) simulator. This analysis used a 10% resistor R_2 variation, and Fig. 4.118 shows the magnitude and phase findings. In addition, Fig. 4.119shows the parallel R-(-L) simulator's transient input voltage and current responses to a 1mV sinusoidal voltage at 100 kHz.



(a) (b)

Figure 4.118: AC Monte-Carlo results of parallel R-(-L) simulator of Circuit-4 (a) magnitude responses (b) Phase responses

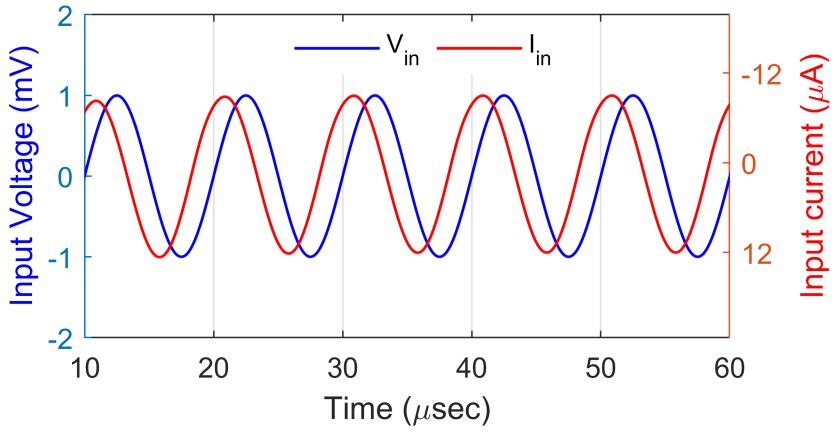
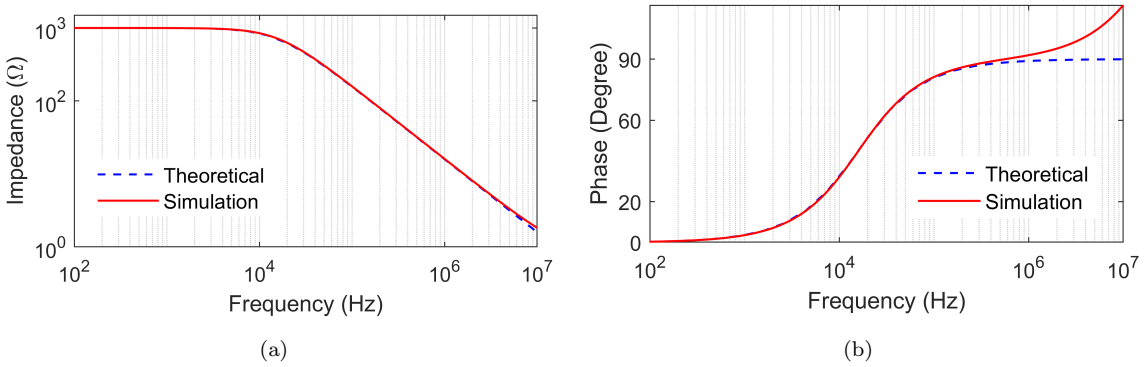


Figure 4.119: Transient responses of input voltage and current of parallel R-(-L) simulator

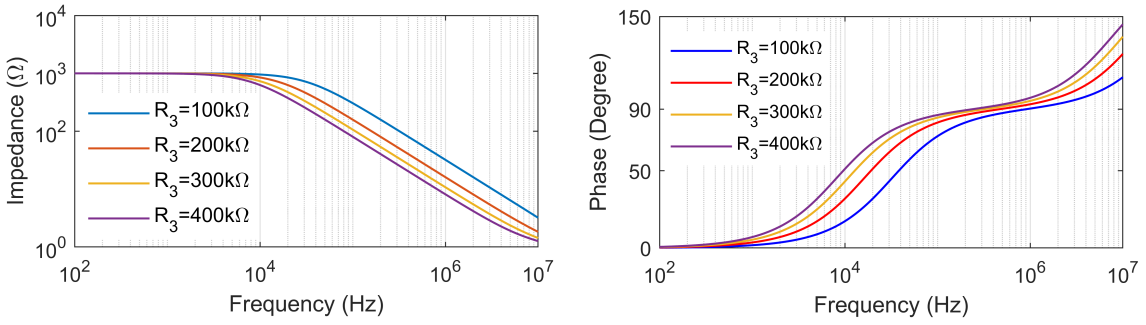
The simulation results for parallel R-(-C) of Fig. 4.65 (Circuit-4) show equivalent resistance (R_{eq}) and capacitance (C_{eq}) values of 1kΩ and 10nF, respectively, with passive component values of R_1 = 1kΩ, R_3 = 100kΩ, and C_2 = 100pF. The magnitude and phase responses are shown in Fig. 4.120. To analyze the parallel R-(-C) circuit, we tested resistor R_3 values of 100kΩ, 200kΩ, 300kΩ, and 400kΩ and impedance and phase variation responses shown in Fig. 4.121.

Fig. 4.120 shows that the simulated impedance and phase match theoretical values from 100Hz to 10MHz (impedance) and 100Hz to 1MHz(phase). The magnitude and phase responses of the parallel R-(-C) circuit, as determined from the Monte Carlo simulation, are presented in Fig. 4.122. For the time-domain analysis, a sinusoidal



(a) (b)

Figure 4.120: Frequency responses of parallel R-(-C) simulator of Circuit-4



(a) (b)

Figure 4.121: Frequency responses of parallel R-(-C) simulator of Circuit-4 for different values of R_3 (a) magnitude (b) phase

input signal with an amplitude of 50mV and a frequency of 100kHz was employed. The corresponding input voltage and current waveforms are shown in Fig. 4.123. In order to assess the effectiveness of the proposed parallel C-(-D) configuration illustrated in Fig. 4.65(Circuit-4), the frequency responses of impedance magnitude and phase were measured with C_1 = 100pF, C_2 = 100pF, and R_3 = 100kΩ. The corresponding results are displayed in Fig. 4.124. Frequency responses of parallel C-(-D) simulator of Circuit-4 for different values of R_2 (100kΩ, 200kΩ, 300kΩ, 400kΩ) have been displayed in 4.125

As observed from Fig. 4.124, the simulated impedance exhibits excellent correlation

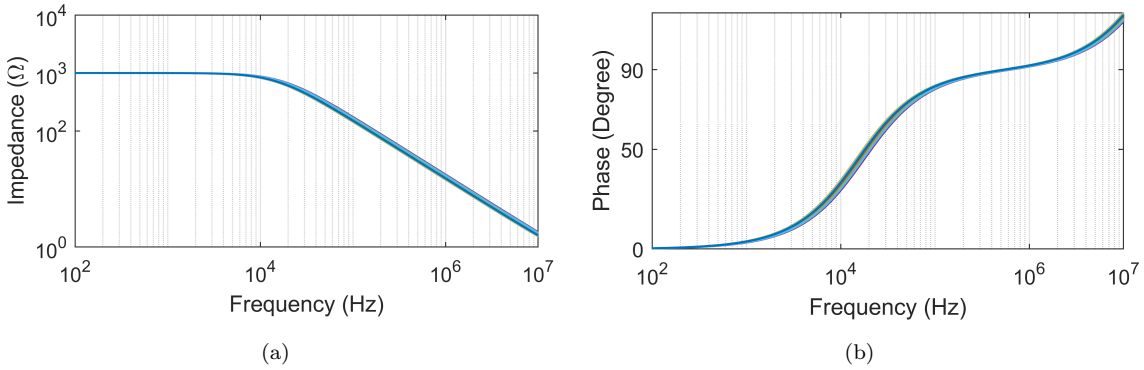


Figure 4.122: AC Monte-Carlo results of parallel R-(-C) simulator of Circuit-4 (a) magnitude responses (b) Phase responses

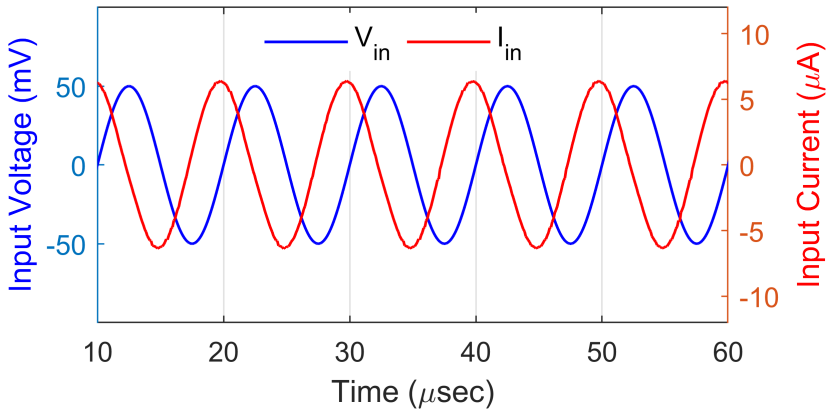
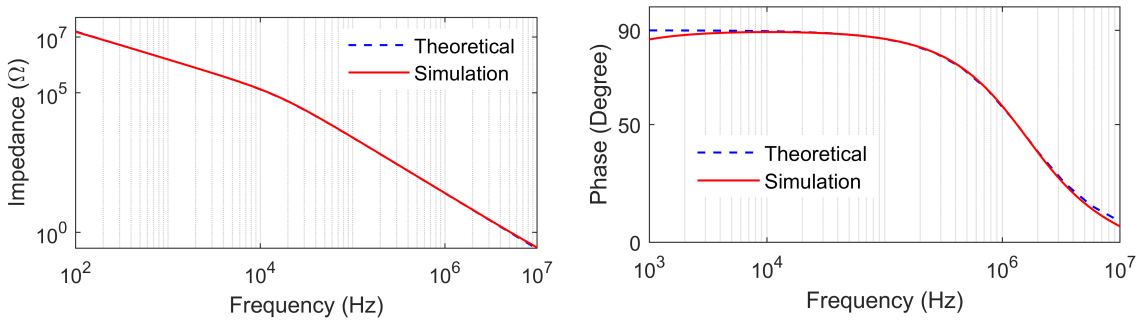


Figure 4.123: Transient responses of input voltage and current of parallel R-(-C) simulator

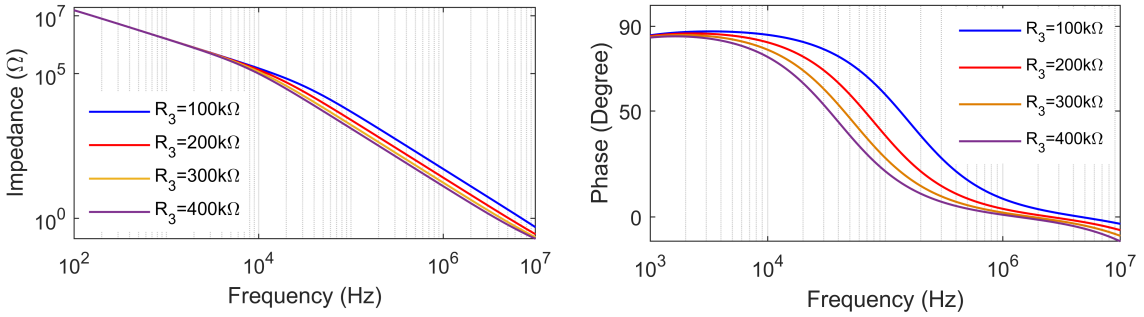
with the theoretical values over the frequency range of 100 Hz to 10 MHz. Furthermore, the phase response closely matches the theoretical prediction between 1 kHz and 10 MHz. Monte-Carlo analysis has also been performed and the corresponding results are shown in Fig. 4.126. To examine the time-domain responses of the input current and voltage, a 50 mV, 100 kHz sinusoidal input was utilized. The corresponding results are shown in Fig. 4.127.

The simulation of the capacitance multiplier circuit shown in Fig. 4.65(Circuit-4) was carried out using passive component values of $C_1 = 100$ pF, $R_2 = 1$ kΩ, and $R_3 = 100$ kΩ. The corresponding impedance and phase responses are presented in Fig. 4.128. The variation in magnitude and phase responses at different values of



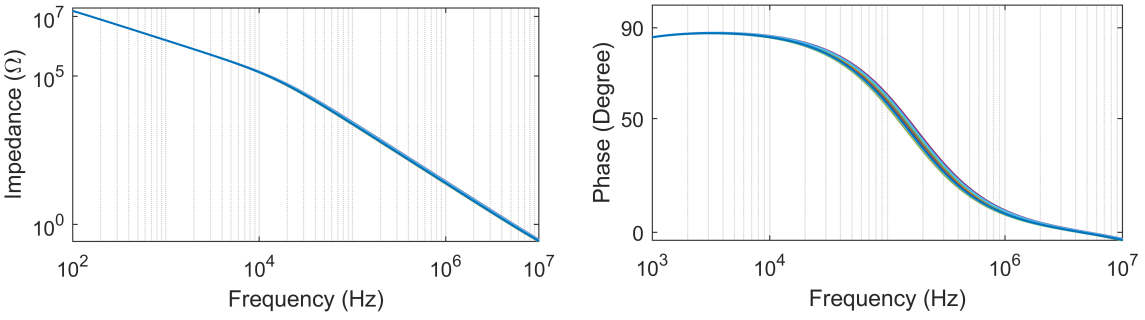
(a) (b)

Figure 4.124: Frequency responses of parallel C-(-D) simulator of Circuit-4



(a) (b)

Figure 4.125: Frequency responses of parallel C-(-D) simulator of Circuit-4 for different values of R_3 (a) magnitude (b) phase



(a) (b)

Figure 4.126: AC Monte-Carlo results of parallel C-(-D) simulator of Circuit-4 (a) magnitude responses (b) Phase responses

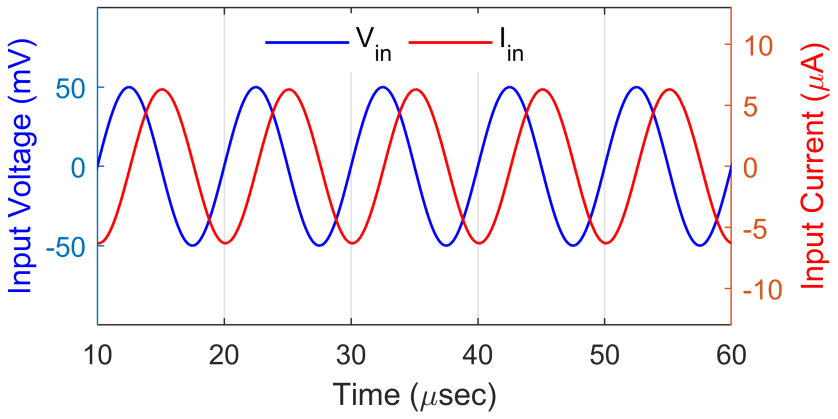
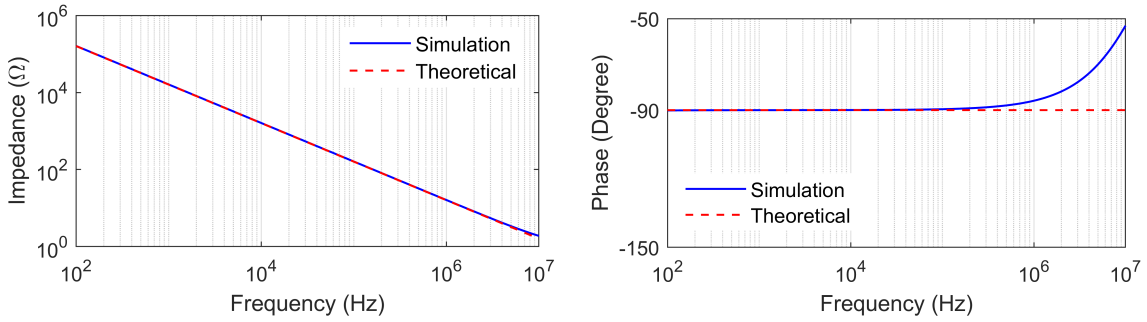


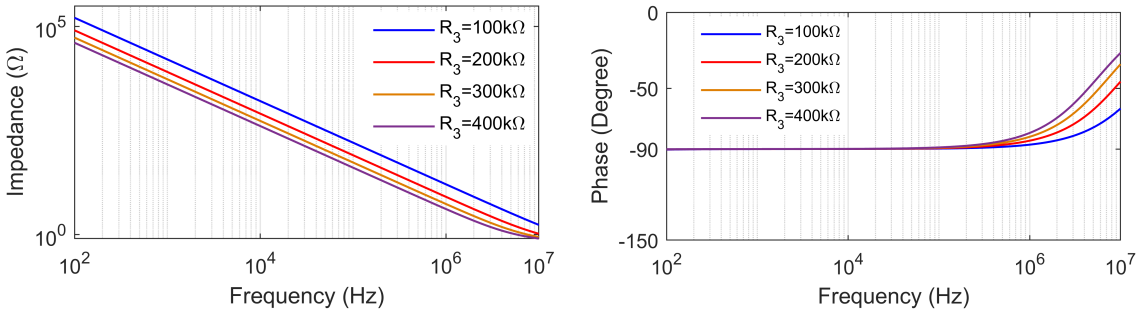
Figure 4.127: Transient responses of input voltage and current of parallel C-(-D) simulator



(a) (b)

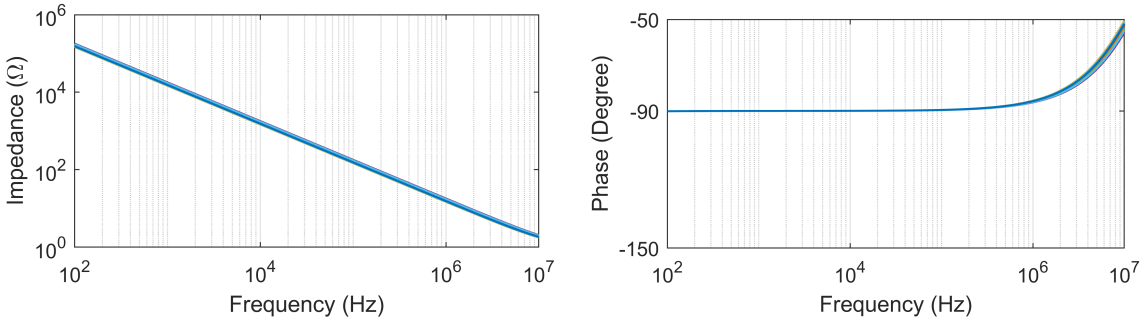
Figure 4.128: Frequency responses of capacitance multiplier of Circuit-4

resistor R_3 (100kΩ, 200kΩ, 300kΩ, 400kΩ) have been displayed in Fig. 4.129. As shown in Fig. 4.128, the simulation results for impedance and phase demonstrate close conformity with theoretical values within the frequency intervals of 100 Hz to 10 MHz and 100 Hz to 500 kHz, respectively. The AC Monte-Carlo simulated magnitude and phase are shown in Fig. 4.130, while Fig. 4.131 depicts the transient responses of the input voltage and current for a 100 mV, 100 kHz input signal.



(a) (b)

Figure 4.129: Frequency responses of capacitance multiplier of Circuit-4 for different values of R_3 (a) magnitude (b) phase



(a) (b)

Figure 4.130: AC Monte-Carlo results of capacitance multiplier of Circuit-4 (a) magnitude responses (b) Phase responses

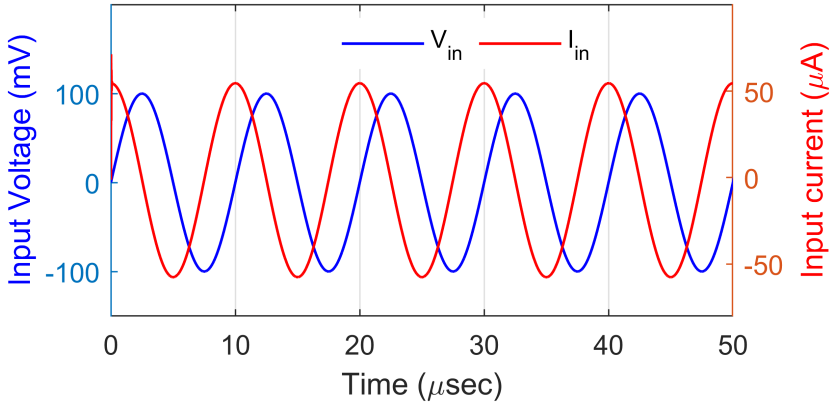


Figure 4.131: Transient responses of input voltage and current of capacitance multiplier of Circuit-4

4.3.3 Pre and Post layout simulations

To confirm the practicality of the proposed grounded parallel immittance circuits, both pre-layout and post-layout simulations were executed for Circuit-1 as depicted in Fig. 4.65, utilizing the Cadence Virtuoso simulation tool. The designs of the CMOS VCII+ and VCII- proposed were represented in Fig. 4.58. For the capacitance multiplier, the values chosen were $R_2 = 1\text{k}\Omega$, $C_1 = 100\text{pF}$, and $R_3 = 100\text{k}\Omega$, while for parallel RL, $R_1 = 10\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, and $C_3 = 10\text{nF}$ were selected. The Circuit-1 configuration shown in Fig. 4.65 successfully passed all physical validation assessments, encompassing the design rule check (DRC), layout and schematic extraction (LVS), as well as RC extraction. Fig. 4.132 illustrates pre-layout and post-layout impedance and phase data for both the capacitance multiplier and parallel RL of Circuit-1. The close alignment between pre-layout simulated responses and post-layout results in Fig. 4.132 confirms the validity of the proposed configurations.

4.3.4 Exemplary application of proposed parallel immittance simulator circuits

The application of the proposed parallel RL and positive capacitance multiplier of Fig. 4.65(Circuit-1) have also been validated by designing a second-order high pass filter (HPF) and first-order low pass filter (LPF) respectively shown in Fig. 4.133. Circuit analysis of Fig. 4.133 yields the transfer functions and cut-off frequencies as shown in Table 4.3.

For a pole frequency nominally set at 159 kHz, the second order HPF circuit using the parallel RL circuit presented in Fig. 4.133 (a), for which the passive components

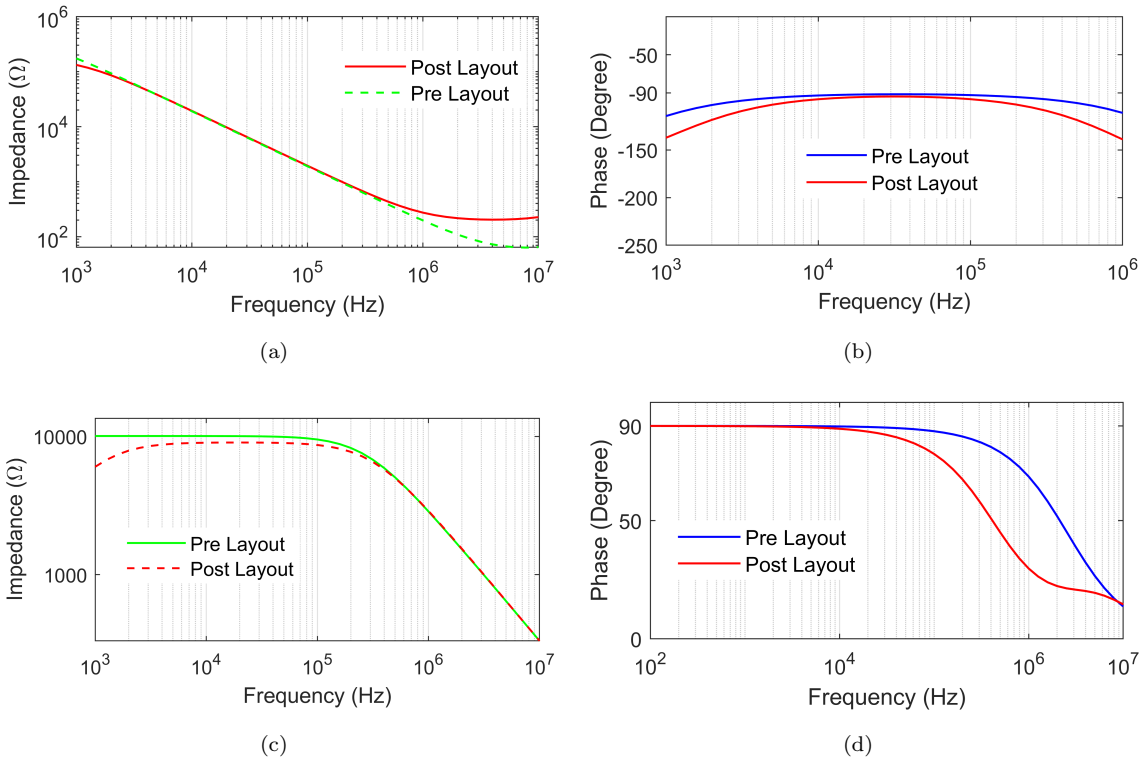


Figure 4.132: Frequency response of (a) magnitude of capacitance multiplier (b) phase of capacitance multiplier (c) magnitude of parallel R-L (d) phase of parallel R-L

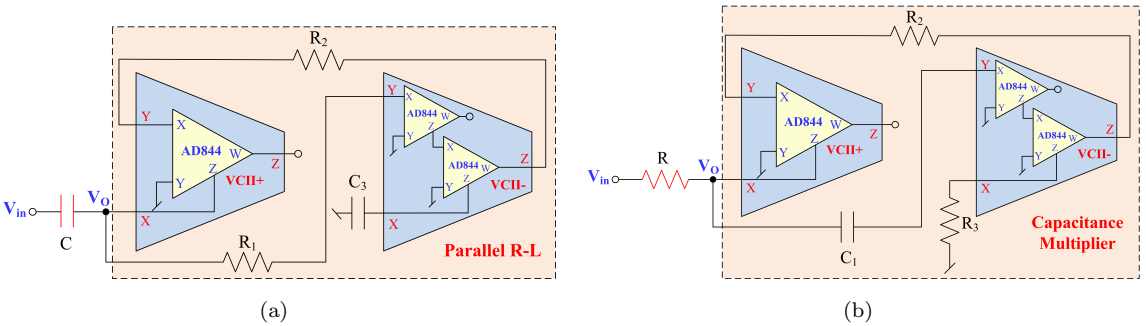


Figure 4.133: Design of filters using parallel RL and capacitance multiplier circuit of Fig. 4.65(Circuit-1)

Table 4.3: Transfer functions and cut-off frequencies obtained from the circuits of Fig. 4.133

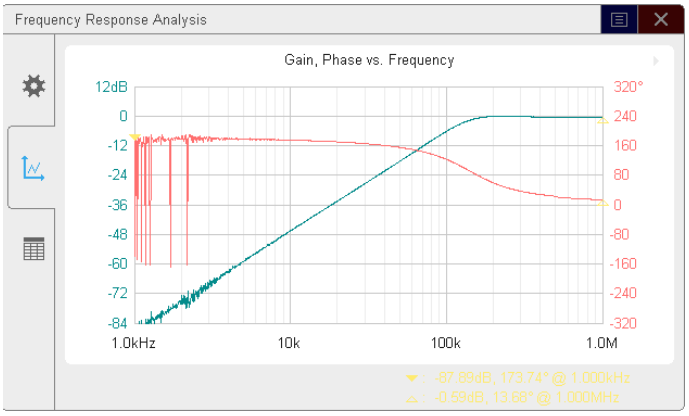
Filter Realization	Transfer Function	Cut-off Frequency
Second-order HPF	$\frac{V_o(s)}{V_{in}(s)} = \frac{s^2}{s^2+s\left(\frac{1}{R_{eq}C}\right)+\left(\frac{1}{L_{eq}C}\right)}$ where $R_{eq} = R_1, \quad L_{eq} = sC_3R_1R_2$	$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} = \frac{1}{2\pi\sqrt{R_1R_2C_3C}}$
First-order LPF	$\frac{V_o}{V_{in}} = \frac{1}{sRC_{eq}+1}$ where $C_{eq} = C_1\left(1+\frac{R_3}{R_2}\right)$	$f_o = \frac{1}{2\pi RC_{eq}}$

C, C_3, R_1 and R_2 were chosen to have values of 1nF, 1nF, 1kΩ and 1kΩ. Fig. 4.134 (a) illustrates the experimentally obtained second order HPF frequency response. Similarly, the first order LPF circuit using the capacitance multiplier circuit presented in Fig. 4.133 (b), for which the passive components C_1 = 1nF, $R_2 = R_3$ = 1 kΩ and R = 1kΩ were chosen to design a filter of pole frequency of 79.5kHz. Fig. 4.134 (b) illustrates the experimentally obtained LPF frequency response.

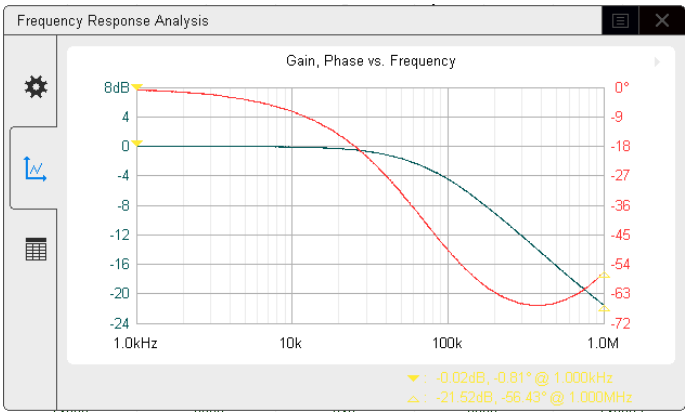
4.3.5 Experimental results

In order to conduct an experimental validation of the proposed parallel immittance simulator circuits, VCII+ and VCII- are incorporated utilizing off-the-shelf IC AD844 shown in Fig. 4.60. The parallel RL simulator derived from Circuit-1 of Fig. 4.65 was experimentally tested using the circuit shown in Fig. 4.135 (a) by selecting R_1 = 1kΩ, R_2 = 100kΩ and C_3 = 100pF. The biasing of AD844s was achieved using power supply voltages of ±15V. Passive components with a tolerance of 5% for resistors and 10% for capacitors were utilized. The relevant experimental impedance and phase responses are depicted in Fig. 4.136.

According to the experimental findings presented in Fig. 4.136, it is evident that the impedance and phase responses of the proposed parallel RL simulator closely align with both the simulated and theoretical outcomes within a frequency range of 100Hz to 100kHz and 5kHz to 100kHz respectively. The capacitance multiplier derived from Circuit-1 of Fig. 4.65 was experimentally tested using the circuit shown

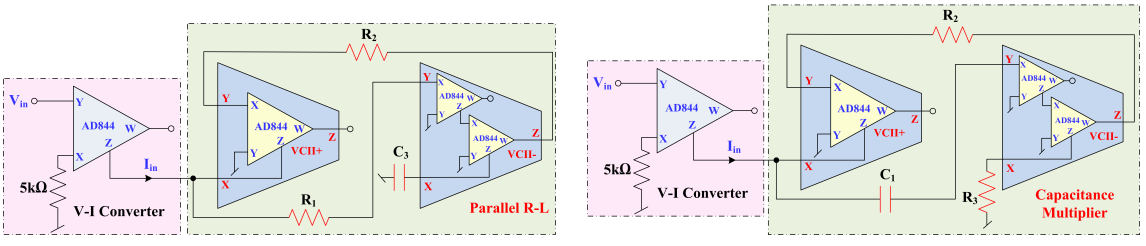


(a)



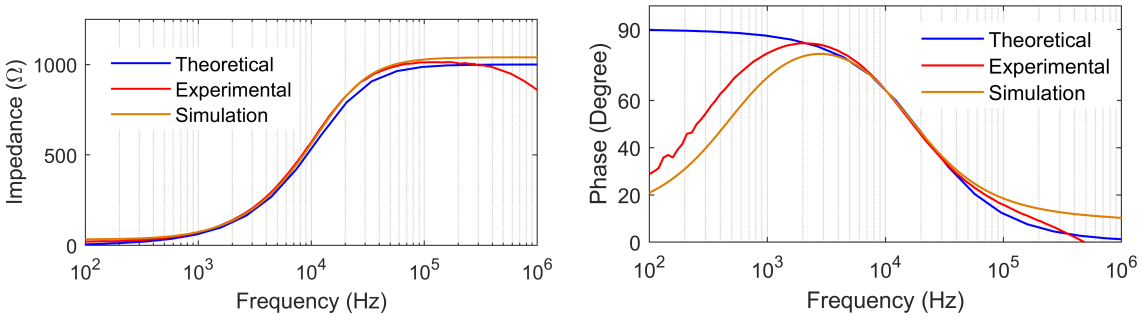
(b)

Figure 4.134: Frequency response of (a) second order HPF using parallel RL circuit of Fig. 4.65 (Circuit-1) and (b) first order LPF using capacitance multiplier circuit of Fig. 4.65 (Circuit-1)



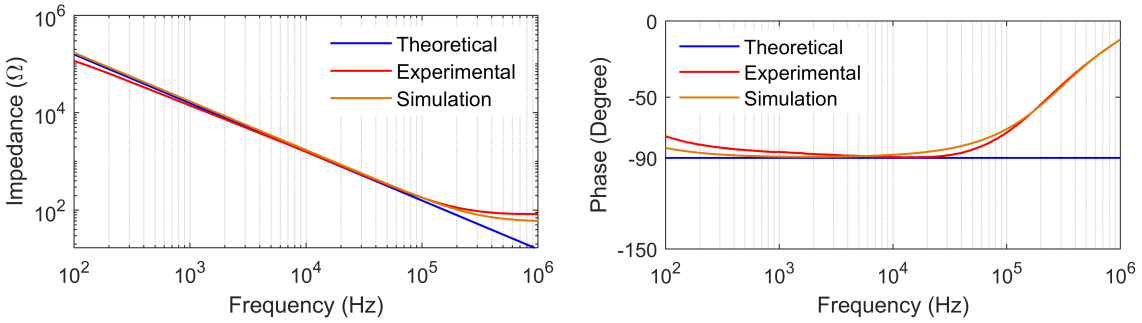
(a) (b)

Figure 4.135: Complete circuit realization of (a) parallel RL simulator (b) capacitance multiplier of Circuit-1 of Fig. 4.65



(a) (b)

Figure 4.136: Experimental results of parallel RL simulator derived from Circuit-1 of Fig. 4.65 (a) input impedance (b) phase



(a) (b)

Figure 4.137: Experimental results of capacitance multiplier derived from Circuit-1 of Fig. 4.65 (a) input impedance (b) phase

in Fig. 4.135 (b) by selecting $C_1 = 100\text{pF}$, $R_2 = 1\text{k}\Omega$ and $R_3 = 100\text{k}\Omega$. The corresponding impedance and phase responses of capacitance multiplier circuit have been shown in Fig. 4.137. From the experimental findings displayed in Fig. 4.137, it is evident that the impedance and phase characteristics of the proposed capacitance multiplier closely correspond with both the simulated and theoretical results. This alignment is particularly notable within the frequency ranges of 100 Hz to 100 kHz for impedance and 500 Hz to 50 kHz for phase.

4.3.6 Concluding remarks

This Chapter introduces four new generalized series and parallel grounded immittance simulator circuits, each employing two VCIIs and three impedances using intrinsic property of VCIIs. Depending on the selection of passive elements, these proposed circuits can function as grounded series/parallel RL, grounded series/parallel RC, grounded series/parallel CD simulators and capacitance multiplier. Notably, the L, C and D of these derived simulators can be controlled independently, without any matching constraints. An application example, as a second-order LPF, second order HPF and first order LPF have also been discussed to validate the usability of the proposed circuits. To validate the performance of the proposed circuits, extensive simulations were conducted using CMOS VCIIs. Pre/post layout results of one of the circuits have also been appended and found to be consistent with the expected performance, validating the robustness and accuracy of the proposed design. Furthermore, the experimental results of the series RL simulator,parallel RL simulator and capacitance multiplier circuit were carried out using VCIIs implemented with commercially available AD844 ICs, thereby providing empirical support for the theoretical propositions.

Chapter 5

Concluding Remarks and Future Scope of Work

5.1 Concluding Remarks

In **Chapter 2**, we have introduces three novel configurations of negative grounded capacitance multipliers (NGCMs) with a single CFOA. The proposed circuits utilize a single ABB, a single grounded capacitor, eliminate passive component matching, achieve high multiplication factors (up to 2001). Their performance has been corroborated using extensive PSPICE simulations encompassing frequency, transient, noise, Monte-Carlo, temperature, and PSRR evaluations, demonstrating stable impedance and phase characteristics over varying temperatures.

Furthermore, three floating immittance simulator circuits utilizing three CFOAs and three impedances are introduced, capable of simulating various floating R-L, R-C, C-D, FDNR, and lossless L/C configurations. These circuits provide individually adjustable immittance values through a single resistor, independent of passive

matching limitations. Theoretical assertions are verified by both simulation and experimental findings utilizing AD844-type CFOAs, illustrating practical feasibility and application versatility.

Chapter 3 introduces a lossy capacitance multiplier circuit employing a CFDITA, a single resistor, and a virtually grounded capacitor. The circuit enables independent control of the multiplication factor (up to 7102) without necessitating passive component matching. The performance is evaluated using a non-ideal CFDITA model and corroborated through pre-layout and post-layout simulations utilizing 0.18µm TSMC CMOS technology, as well as experimental verification using AD844 and LM13700 ICs.

Additionally, two capacitance multiplier circuits able to provide both positive and negative multiplication factors are introduced. Each configuration employs a single CFDITA, one resistor, and one grounded capacitor, providing capacitance augmentation of up to 1800 times, with tunable multiplication factors to 9202 via resistor adjustment. These circuits can be modified to create parallel RL simulators with separately adjustable inductance. Comprehensive SPICE simulations and experimental findings validate the practical feasibility of the designs and corroborate the theoretical analysis, illustrating the circuits adaptability and application potential.

Chapter 4 introduces four new generalized grounded immittance simulator circuits comprising both series and parallel configurations each employing two VCIIs and three impedances, using intrinsic property of VCIIs. By appropriate selection of passive components, these circuits can implement grounded RL, RC, CD simulators, and capacitance multipliers. An essential benefit is the independent adjustment of L, C, and D values without necessitating passive component matching.

Application example, including a second-order low-pass filter (LPF), a second-order high-pass filter (HPF), and a first-order LPF, have been presented to illustrate the circuits adaptability. The functionality and robustness of the proposed circuits have been validated by CMOS VCII-based simulations, encompassing both pre- and post-layout outcomes, which correspond closely with theoretical predictions. Additional validation is obtained through experimental implementations of series and parallel RL simulators and a capacitance multiplier utilizing AD844-based VCIIs, offering empirical corroboration for the proposed circuits.

5.2 Future Scope

- **Low-voltage and Low-power circuits**: As integrated circuits progress towards battery operated and portable devices, the development of low-voltage and ultra-low-power immittance simulators utilizing ABBs is essential. Creating circuits that operate under sub-1V conditions can enhance their utility in biomedical and IoT applications.

- **Nano CMOS Implementation**:These circuits can be implemented utilizing modern CMOS technologies (65nm, 45nm, etc.) to evaluate area, power, and speed trade-offs. VLSI integration will improve with layout-aware design and device-level parasitic elimination.

- **Digitally Programmable and Tunable Immittance Simulators**: Digitally tunable resistors/transconductances or bias-controlled ABBs can create programmable and adaptive circuits for reconfigurable analog signal processing, machine learning accelerators, and neuromorphic systems.

- **Fully Integrated Systems and ASIC Realization**: A combination of immittance simulators with signal processing components, including filters, oscillators, and modulators, into a comprehensive analog front-end ASIC represents a potential domain. This encompasses layout optimization, floor planning, and fabrication viability.

- **Fractional-Order Immittance Simulation**: There is growing interest in fractional-order elements for biomedical and control applications. Research can enhance contemporary ABB-based systems to implement fractional-order capacitors, inductors, and differentiators.

- **Temperature Stability and Process variation Tolerance**: Enhancing temperature stability and process tolerance by adaptive biasing or compensation approaches would augment the reliability of these circuits under diverse environmental conditions..

- Application of immittance simulator circuits in emerging areas such as sensor interface design, analog signal conditioning, and edge analog computing.

- **Machine Learning for Analog Design**: Utilizing AI/ML algorithms to optimize component values and performance measures (e.g., THD, bandwidth, PSRR) may represent a future trend in the automated design of ABB-based immittance simulators.

- Future work may focus on developing higher-order and multifunctional analog signal-processing blocks using the improved low-voltage VCII structures [] []

5.3 Societal Impact

The implementation of simulated immittances through modern active building blocks has important societal impacts by facilitating the development of small, energy-efficient, and economical analog signal processing circuits. These circuits can substantially contribute to:

- **Healthcare and Biomedical Instrumentation:** Compact, low-power analog front-ends for the capture of bio-signals, including ECG, EEG, and wearable health monitoring devices.
- **Environmental Monitoring:** Implementation of analog interfaces in economical, battery-powered sensor nodes for the real-time assessment of air, water, and soil quality.
- **Education and Research:** Providing accessible design solutions with commercially available components for laboratory instruction, prototyping, and creativity in resource-limited environments.
- **Sustainable Electronics:** The reduction in the necessity for large passive components results in less material usage, hence promoting environmentally friendly and sustainable hardware design.
- **Technology Access:** Facilitating the advancement of analog systems in regions with restricted access to sophisticated digital technology by providing feasible, cost-effective analog alternatives.

5.3.1 Linking Research Objectives with SDGs for Societal Impact

The Fig. 5.1 illustrates four research objectives in immittance simulation circuits using modern active building blocks, each of which significantly contributes to several United Nations Sustainable Development Goals (SDGs) such as SDG 7 (Affordable and Clean Energy), SDG 9 (Industry, Innovation and Infrastructure), SDG 12 (Responsible Consumption and Production) and SDG 13 (Climate Action).

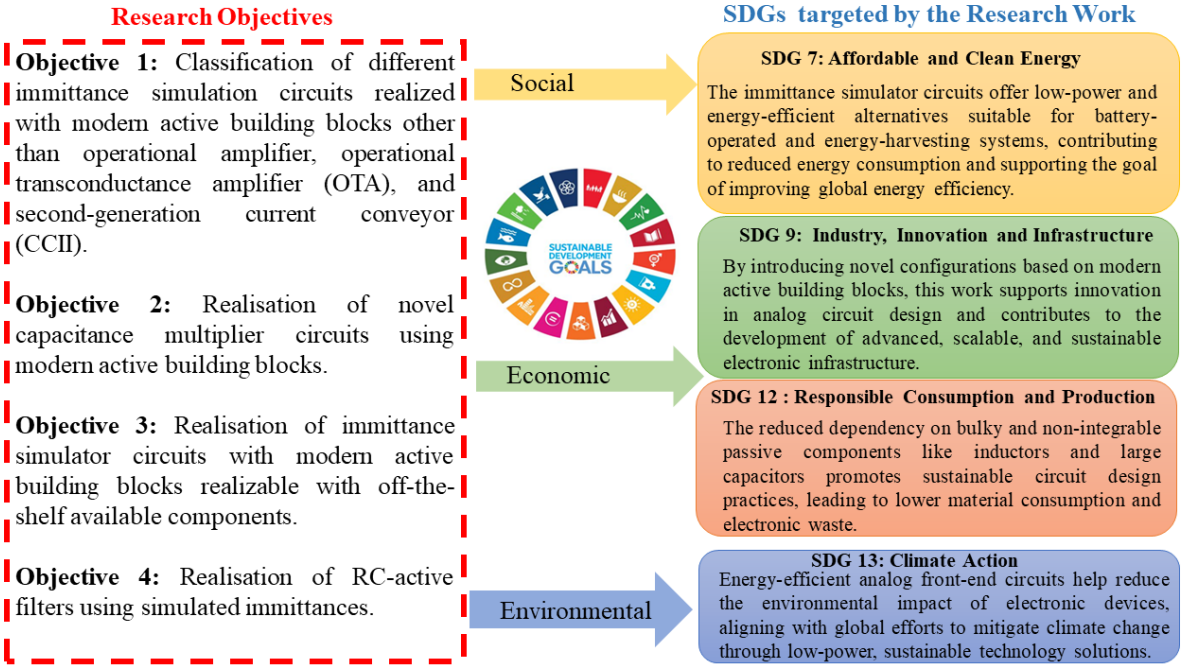


Figure 5.1: Incorporation of Sustainable Development Goals with the thesis objectives

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LIST OF PUBLICATIONS

Journals

1. D. R. Bhaskar, M. Shrivastava, A. Raj, and P. Kumar, "Floating parallel lossy inductance, parallel lossy capacitance, parallel C-D, and lossless capacitance multiplier circuits using current feedback operational amplifiers," International Journal of Circuit Theory and Applications, vol. 52, no. 3, pp. 1489–1517, 2024.

2. M. Shrivastava, D. R. Bhaskar, and P. Kumar, "VCII-based immittance simulators: Generalized parallel configurations," International Journal of Circuit Theory and Applications, 2024.

3. M. Shrivastava, P. Kumar, A. Raj, and D. R. Bhaskar, "Single current follower differential input transconductance amplifier based grounded lossy capacitance multiplier with large multiplication factor," International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 37, no. 1, e3139, 2024.

4. A. Raj, M. Shrivastava, D. R. Bhaskar, and P. Kumar, "Enhancement of multiplication factor of capacitor using single current follower differential input transconductance amplifier," International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 37, no. 4, e3279, 2024.

5. A. Raj, D. R. Bhaskar, M. Shrivastava, and P. Kumar, "New negative-grounded capacitance multiplier circuits," International Journal of Circuit Theory and Applications, vol. 51, no. 3, pp. 1476–1491, 2023.

6. M. Shrivastava, D. R. Bhaskar, and P. Kumar, "VCII-Based Generalized Configurations for Grounded Series-type Immittance Simulators," Journal of Circuits, Systems and Computers, 2025.

Presentations and proceedings in International Conferences

1. M. Shrivastava, P. Kumar, and D. R. Bhaskar, "Single CFOA-based grounded negative impedance simulator circuit," in 2023 International Conference on Modeling, Simulation & Intelligent Computing (MoSICom), IEEE, 2023, pp. 94–98.

2. M. Shrivastava, P. Kumar, and D. R. Bhaskar, "Negative capacitance multiplier configuration using single CFOA employing grounded capacitor," in 2022 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), IEEE, 2022, pp. 1–4.

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Education

2021 – 2025 **Ph.D., Delhi Technological University, New Delhi, India, (Thesis Submitted)**.
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2019 – 2021 **M.Tech, Control and Instrumentation System, Jamia Millia Islamia, New Delhi (CGPA:9.41)**.
Thesis title: *Design and Fabrication of impedance sensor for moisture measurement in grains*.

2013 – 2017 **B.Tech, Instrumentation Engineering, Bundelkhand Univeristy, Jhansi(82.11%)**.
Thesis title: *Bidirectional Visitor Counter using Infrared sensor and Microcontroller*.

2012 – 2013 **Intermediate, Central Board of Secondary Education(81.2%)**.

2010 – 2011 **Matriculation, Central Board of Secondary Education(CGPA:9.4)**.

Research Publications

Journal Articles

1. **M. Shrivastava**, D. Bhaskar, and P. Kumar, "VCII-based generalized configurations for grounded series-type immittance simulators," *Journal of Circuits, Systems and Computers*, 2025.
2. D. R. Bhaskar, **M. Shrivastava**, A. Raj, and P. Kumar, "Floating parallel lossy inductance, parallel lossy capacitance, parallel C-D, and lossless capacitance multiplier circuits using current feedback operational amplifiers," *International Journal of Circuit Theory and Applications*, vol. 52, no. 3, pp. 1489–1517, 2024.
3. **M. Shrivastava**, D. R. Bhaskar, and P. Kumar, "VCII-based immittance simulators: Generalized parallel configurations," *International Journal of Circuit Theory and Applications*, 2024.
4. **M. Shrivastava**, P. Kumar, A. Raj, and D. R. Bhaskar, "Single current follower differential input transconductance amplifier based grounded lossy capacitance multiplier with large multiplication factor," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 37, no. 1, e3139, 2024.
5. A. Raj, **M. Shrivastava**, D. R. Bhaskar, and P. Kumar, "Enhancement of multiplication factor of capacitor using single current follower differential input transconductance amplifier," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 37, no. 4, e3279, 2024.
6. A. Raj, D. R. Bhaskar, **M. Shrivastava**, and P. Kumar, "New negative-grounded capacitance multiplier circuits," *International Journal of Circuit Theory and Applications*, vol. 51, no. 3, pp. 1476–1491, 2023.

Conference Proceedings

1. **M. Shrivastava**, P. Kumar, and D. R. Bhaskar, "Single CFOA-based grounded negative impedance simulator circuit," in *2023 International Conference on Modeling, Simulation & Intelligent Computing (MoSICom)*, IEEE, 2023, pp. 94–98.
2. **M. Shrivastava**, P. Kumar, and D. R. Bhaskar, "Negative capacitance multiplier configuration using single CFOA employing grounded capacitor," in *2022 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME)*, IEEE, 2022, pp. 1–4.

Skills

Languages	Strong reading, writing and speaking competencies for English.
Simulation Tool	LTSpice, ANSYS, Proteus, PSpice, Cadence Virtuoso, MATLAB, LATEX.
Technical ability	PCB Design, Hardware implementation, Sensor fabrication.

Miscellaneous Experience

Awards and Achievements

- 2025 **Received the Research and Innovation Excellence Award as a research scholar**.
- 2024 **Received the Research and Innovation Excellence Award as a research scholar**.
- 2021 **Receiving a Delhi Technological University fellowship as a research scholar**.
- 2020 **Received a scholarship as a top-ranked student in the M.Tech degree program**.
- 2013 **Received a IOCL (Indian Oil Corporation Limited) Scholarship during B.tech degree program**.