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Shubham Sharma

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Designing of Battery Charger with Totem-Pole PFC and Phase-Shift Full Bridge Converter

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Submitted by:

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I, Shubham Sharma, Roll No. 2K23/PES/05 student of MTech (Power Electronics & Systems), hereby declare that the project Dissertation titled **"Designing of Battery Charger with Totem-Pole PFC and Phase-Shift Full Bridge Converter"** which is submitted by me to the Department of Electrical Engineering, Delhi Technological university, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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Date: 7th June 2025

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CERTIFICATE

I hereby certify that the project Dissertation titled **"Designing of Battery Charger with Totem-Pole PFC and Phase-Shift Full Bridge Converter"** which is Submitted by **Shubham Sharma,** Roll No. **2K23/PES/05**, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date: 31st May 2025

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ABSTRACT

High reliability and efficiency are critical factors in the development of a battery charger. Therefore, battery charging systems must be designed to comply with grid standards and ensure safe operation. This research discusses the design of a charger that incorporates a Totem-Pole Power Factor Correction (PFC) and a Phase-Shift Full Bridge (PSFB) DC-DC converter. Implementing a power factor correction (PFC) converter will allow one to connect straight to the power grid for AC/DC power conversion and maximize the actual power going to the downstream DC/DC converters. The Phase-Shift full-bridge (PSFB) converter is a high-performance power supply with very fast transient response, given its high-power density and high converter efficiency. The devices are engineered to comply with Power Factor requirements and ensure isolation between the voltage source and the battery. The integration of PSFB provides these areas with galvanic isolation and efficient DC-DC conversion capabilities. A PSFB design built on the Modular Hardware-System-Common Redundant Power Supply (M-CRPS) base specification shows the ability of a PSFB converter. The integration of these topologies results in a charger design that is both compact and highly efficient. The device is capable of operating across a range of voltages while maintaining a stable output power suitable for battery charging.

Simulation and experimental findings support and examine the power and efficiency aspects. This work assumes that battery chargers can be developed utilizing these systems. This research also addresses the challenges associated with charging technology by enhancing efficiency, reliability, and compliance with stringent regulations.

Keywords- *Battery charger Topology, Phase-Shift Full Bridge (PSFB), Power Factor Correction, Soft-Switching, Totem-Pole PFC, Zero Voltage Switching (ZVS)*

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LIST OF ABBREVIATIONS

PFC	Power Factor Correction
TP-PFC	Totem-Pole Power Factor Correction
PSFB	Phase-Shift Full Bridge
DAB	Dual Active Bridge
M	Mutual inductance
k	Coupling coefficient
EV	Electric vehicle
Pri	Primary
Sec	Secondary
SRs	Synchronous Rectifiers
P	Parallel
WBG	Wide Bang Gap
SOC	State of charge
VA	Volt-ampere
LC	Filter circuit (series inductor and parallel capacitors)
EMI	Electromagnetic Interference
PTE	Power transfer efficiency
TP	Transferred power

Chapter 1
INTRODUCTION

1.1. Background

This chapter presents an outline of Battery charging systems with Power Factor Correction configuration, including galvanic isolation with different topologies used, and their accomplishments. Additionally, this thesis highlights its objectives, scope, and contributions of the proposed topologies that can be used in a battery charger with increased efficiency and several other benefits.

1.1.1. Introduction to Various Battery Charger Topologies

The design of battery chargers with high efficiency, power factor correction, and isolation has been a widely common significant area of research in recent years. Several studies have explored different topologies, combinations and control strategies to improve efficiency, enhance overall performance, and improve the system's Power Factor. Various topologies have emerged, connected with different architectures to provide isolation, correct the Power Factor near unity and improve the overall efficiency of the Battery Charger.

The conventional boost PFC is one of the most widely used topologies in battery chargers due to its very simple design and ease of achieving a high-power factor. A single-phase Boost PFC was implemented in a 3.3 kw battery charger, achieving a power factor of 0.99 and efficiency of 95% [1]. However, a drawback of this topology is the presence of a diode bridge rectifier, which introduces limits to efficiency improvement and significantly high conduction losses in the system.

A high-frequency flyback converter was designed for portable electronics, achieving an efficiency of 85% with a minimum number of components [2]. This study highlighted the advantages of galvanic isolation and ease of implementation. However, flyback converters suffer from high voltage stress on the switch and limited power handling capability, which makes them unsuitable for high-power applications such as Battery Chargers. Also, significantly high-power losses make these topologies inconvenient in modern use cases.

In [3], the author presented a bridgeless Totem-Pole PFC circuit using Gan-based switches, demonstrating an efficiency of over 98% with reduced conduction losses. The study highlighted the advantage of Totem-Pole PFC with minimum switching losses and improved thermal performance. A full-bridge LLC resonant converter is implemented in an 11-kw fast EV Charger, which achieves efficiency of 97% with minimal electromagnetic interference (EMI) [4]. The study highlighted that LLC converters provide excellent voltage regulation and reduced switching losses, making them suitable for high-power applications. However, the design complexity and sensitivity to component variation require careful tuning of the resonant circuit.

The Dual Active Bridge (DAB) converter is a widely used isolation topology for battery charging due to its bidirectional power transfer capability, soft-switching operation, and very high efficiency. A 10-kw bidirectional EV Battery charger that achieves an efficiency of 96% across a wide range of loads. However, the DAB converter also requires precise control strategies to handle variation in battery voltage to ensure stable operation [5].

Several researchers have investigated the Totem-Pole PFC topology due to its abilities, such as higher efficiency, low component count, Low Total Harmonic Distortion and near unity power Factor. The suggested Battery Charger is the integration of a Totem-Pole Power Factor Correction (PFC) stage and a Phase-Shift Full Bridge (PSFB) DC-DC converter. This strategy is focused on designing battery chargers [6] by improving efficiency, reducing the number of components required, and maintaining a small size. One of the most important parameters of the Totem-Pole PFC topology is that it has a power factor as close to unity as possible, has low total harmonic distortion (THD) and conduction losses, and exhibits a low circuit complexity.

Utilizing the best of these two topologies, the proposed system is expected to operate efficiently over a wide range of input voltages and battery chemistries and yet provide high efficiency under all operating conditions. This paper also presents the findings of a rigorous analysis of design models, simulation, and laboratory tests, demonstrating the feasibility of integrating both Totem-Pole PFC and PSFB converter stages into a single battery charger.

Through good layout design, precise component selection, and the implementation of an effective control strategy, this work demonstrates how performance is not compromised at the expense of meeting existing grid standards and environmental protection regulations.

As seen in Fig. 1, A battery charger typically consists of two conversion stages: An isolated DC/DC converter with a wide voltage output for the battery and an AC/DC converter with PFC [7] [8]. Dual Active Bridge (DAB) converters and LLC resonant converters are the two most popular isolated DC/DC converters. For high efficiency and high-power density, high frequency soft-switching technology is frequently used in LLC resonant converters and DAB converters.

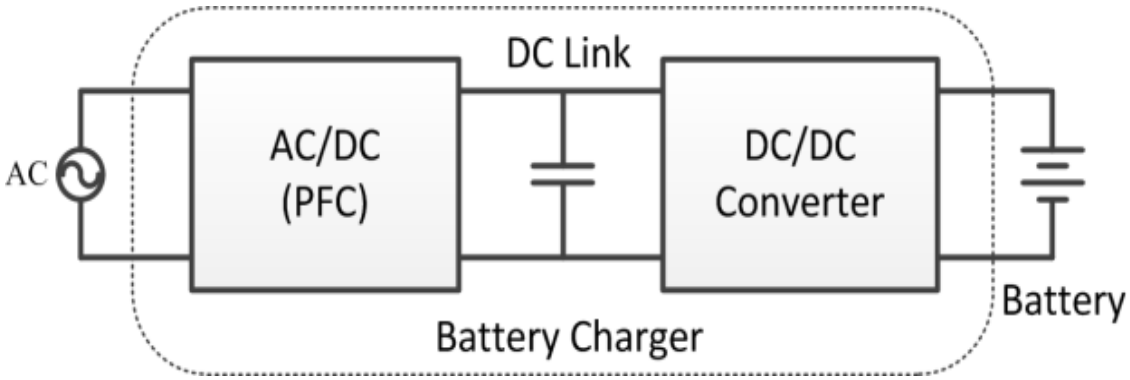

Fig.1.1 Typical circuit architecture of a battery charger.

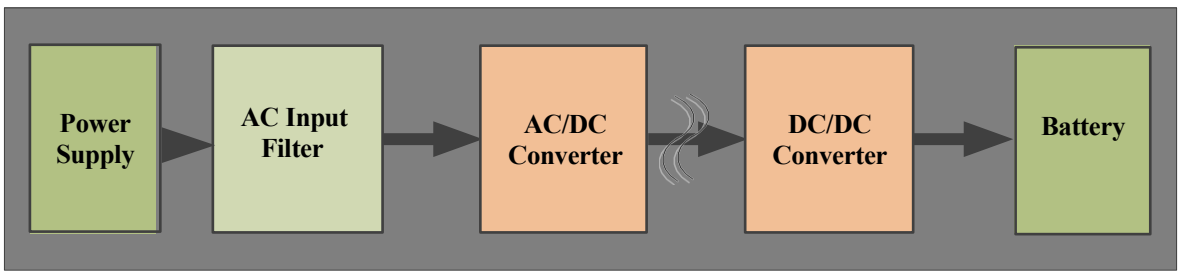

Fig.1.2 Basic Power flow diagram of Battery Charger

1.1.1. Applications of Battery Charger

Essential tools that restore the energy in rechargeable batteries are battery chargers, which let many devices in many industries run. The planned use of the batteries these chargers power directly influences their design and execution. With an eye toward electric vehicle (EV) charging infrastructure, below is an examination of the several uses for charged batteries [9]:

1. Electrified transportation and electric vehicles (EVs)

This is a well-known and fast-growing area of battery charger technology. The primary power source for: Battery electric cars, or BEVs, run only on electricity kept in large battery packs.

Chargers onboard (OBCs) Built into the BEV, OBCs convert AC power from public or private AC charging stations (Level 2) or household outlets (Level 1) into DC electricity to charge the vehicle's high-voltage traction battery. The electric motor or motors are then powered by the charged battery. OBC design influences charging speed at home or at business, grid interface, and user convenience.

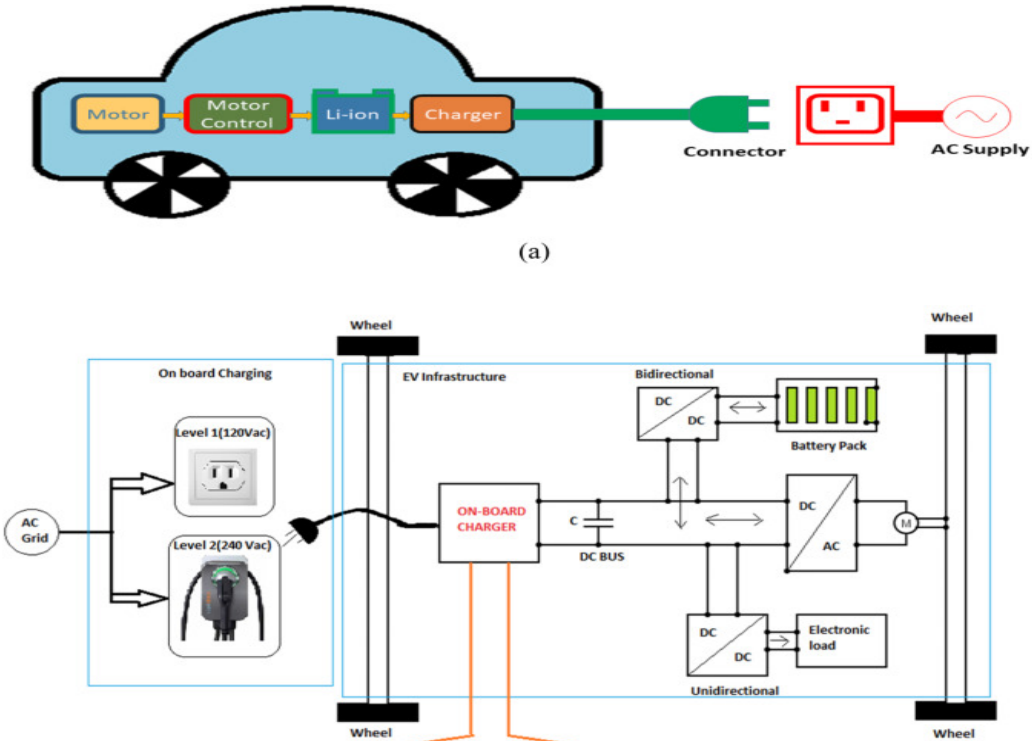

Fig.1.3 Power flow diagram of E. V. Battery Charger

Level 3 high-power charging stations called Off-Board chargers, sometimes referred to as DC fast chargers, send high-voltage DC power straight to the BEV battery, bypassing the OBC. This makes possible far quicker charging times, which are required for quick top-ups and long-distance travel. Charged batteries in these systems allow EVs to travel on routes comparable to those travelled by internal combustion engine cars [10].

2. **Electronics for consumers**

Communication, information access, and entertainment all depend on charged batteries in mobile devices—smartphones, tablets. Usually small AC-DC converters, chargers follow USB power delivery guidelines. Increasingly popular are wireless (inductive) chargers.

These depend on rechargeable batteries charged by specific AC-DC chargers, therefore allowing portable entertainment and mobility. For health monitoring, communication, and other smart activities, small, low-power chargers—often proprietary (magnetic, pogo-pin) or wireless—keep these devices powered. Users may take pictures and videos free from power source tethering by charging removable battery packs with specialized external chargers on cameras and camcorders [11].

Usually powered by USB, the batteries offer hours of untethered audio pleasure.

The portability and wireless freedom provided by these gaming devices depend on charged batteries. Essentially portable batteries, power banks are themselves charged (usually via USB) and then used to power other electronic devices on the go.

3. **Tools and Equipment Powered**

Cordless power tools provide notable convenience and mobility:

Drills, saws, sanders, grinders, lawn and garden equipment: These tools use strong battery packs (often Li-ion based) charged by dedicated chargers. To reduce downtime for professional and DIY users, fast chargers are common in this category. In places without convenient access to mains power, the charged batteries supply the power required for gardening, maintenance, and construction activities [12].

4. **Commercial and Industrial Uses**

A wide variety of devices are powered by batteries, therefore improving efficiency and adaptability. Material Handling Equipment (Forklifts, Pallet Jacks, AGVs - Automated Guided Vehicles) Large battery packs—traditionally lead-acid, progressively Li-ion—are charged using industrial-grade battery chargers, including conventional, opportunity, and fast-charging systems. Charged batteries power activities in distribution centers, manufacturing plants, and warehouses. "Opportunity charging" lets batteries be charged during brief pauses without

requiring swap out.

5. **Backup Power Systems (UPS - Uninterrupting Power Supplies):**
   Critical Infrastructure (Data Centers, Hospitals, Telecom): Integrated float or standby chargers in UPS systems keep batteries—usually lead-acid or Li-ion—at full charge. Should there be a power outage, these charged batteries immediately supply power to stop data loss, service disruption, or failure of vital life-support systems. UPS for Home and Office Smaller UPS systems protect other electronics and personal computers using the same concept.

1.2. Motivation

The fast spread of portable electronics, the growing electric vehicle (EV) market, and the rising integration of renewable energy systems have highlighted the critical need of advanced battery charging technologies. No longer merely supplementary devices, battery chargers are essential for the efficiency, performance, and usability of systems powered by batteries. Conventional charger designs frequently disappoint as these systems call for quicker charging times, more power capabilities, and more energy efficiency, showing constraints in efficiency, power density, and general performance. This calls for a paradigm change toward more advanced power conversion topologies with some major improvements.

Often using a diode bridge rectifier followed by a standard boost Power Factor Correction (PFC) stage and a hard-switched DC-DC converter, traditional battery chargers have several disadvantages. The diode bridge rectifier naturally creates notable conduction losses, so restricting the front-end efficiency. Although traditional boost PFCs increase power factor, their efficiency might be improved more. Furthermore, hard-switching methods in the DC-DC stage cause significant switching losses, particularly at higher frequencies, so limiting the possible power density and usually calling for large thermal management solutions. These inefficiencies raise running costs and energy use. Moreover, the growing harmonic rules all around call for cleaner power extraction from the grid, which presents difficulties for more basic PFC circuits. This study emphasizes the design of a battery charger using a mix of two sophisticated

power converter topologies—the Totem-Pole Power Factor Correction (PFC) converter and the Phase-Shifted Full-Bridge (PSFB) DC-DC converter—to overcome these constraints and satisfy the strict requirements of modern applications—such as high-efficiency power supplies for telecom and data centers, fast chargers for electric vehicles, and grid-interactive power systems.

1.3. Objective and Scope

This study mostly intends to design, test, and possibly construct a high-efficiency, high-power-factor battery charger. Combining two complex power electronic topologies—a Phase-Shifted Full-Bridge (PSFB) DC-DC converter and a Totem-Pole Power Factor Correction (PFC) stage—will help to accomplish.

Objective: To get low total harmonic distortion (THD) at the AC input and near unity power factor, model and design a bridgeless Totem-Pole PFC rectifier. Design and model a Phase-Shifted Full-Bridge DC-DC converter for efficient power transfer and galvanic isolation, appropriate for battery charging profiles (e.g., constant current, constant voltage). A comprehensive control system for both the PFC stage (e.g., average current mode control) and the PSFB converter (e.g., phase-shift control, including soft-switching techniques such Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) to minimize switching losses) is to be developed.

Using MATLAB/Simulink, comprehensive simulations will help to confirm the performance of the distinct stages and the integrated charger system under various operating conditions—line voltage fluctuations, load changes. Examination:

To assess the efficiency of the entire battery charger system and identify key loss reduction areas in both converter stages.

Investigate how component selection—e.g., MOSFETs, diodes, magnetics—affects the performance, efficiency, and power density of the charger.

To investigate the stability of the control loop for both PFC.

Scope:

1. System Specifications: Defining the input voltage range (e.g., universal AC input 90-265V).
2. Specifying the output voltage and current ratings for the battery (e.g., 64V Li-ion battery, 8A charging current).
3. Stating the charger's desired power level (e.g., 500W, 1kW).
4. Establishing the intended efficiency, for example, >95%.
5. Setting the desired power factor (e.g., >0.99) and THD criteria (e.g., <5% per applicable standards including IEC 61000-3-2).

Converter Topology: Thorough design and analysis of the power stages, including choice of semiconductor switches (GaN MOSFETs) are common for totem-pole PFC due to their performance benefits), magnetic components (inductors, transformers), and filter components.

Control System: Development and simulation of digital or analog control schemes for both converters. This covers gate drive circuits and controller design (e.g., PI Controller).

Research on control strategies to maximize performance, such as advanced PFC control algorithms or ZVS for the PSFB converter.

Chapter 2

Literature Review

2.1. Introduction and Evolution of Battery Charging Technologies

As portable electronics, electric vehicles (EVs), and energy storage systems have proliferated, efficient, small, high-performance battery chargers have been in great demand. Early battery charger designs employed basic rectification and large line-frequency transformers, which produced poor power quality, low efficiency, and large form factors. Improved performance requirements pushed the use of switch-mode power supply (SMPS) methods, which permitted more efficiency, smaller component sizes, and higher switching frequencies[13].

Standard has become high power factor, low input current harmonics, and precise output voltage/current control with two-stage charger designs comprising a DC-DC converter back-end and a Power Factor Correction (PFC) front-end. Following international standards such as IEC 61000-3-2, the PFC stage forms the input current to be sinusoidal and in phase with the input voltage. The split DC-DC stage then provides the regulated output voltage and current required for optimal battery charging (e.g., constant current-constant voltage, CC-CV profiles) [14]-[20].

2.1.1. Power Factor Correction (PFC) Topologies:

2.1. Conventional Boost PFC Converter: Because of its steady input current and straight forward control, the traditional boost converter has been the workhorse for active PFC. Its efficiency is therefore limited, particularly at greater power levels, since the diode bridge rectifier at the input causes significant conduction losses. Specific applications have also seen investigation of other topologies such as buck, buck-boost, and flyback PFC converters, which usually have their own efficiency, component stress, or power handling capacity restrictions.

Advantages:

1. Simple design and control
2. Reliable operation
3. Well-documented and widely understood

Disadvantages:

1. Lower efficiency compared to advanced topologies
2. Larger passive components (inductors and capacitors)
3. Higher total harmonic distortion (THD)

2.2 Interleaved PFC: Interleaved PFC converters employ multiple boost converters operating out of phase to share the load current. This method reduces current ripple and enhances efficiency.

Advantages:

1. Reduced input current ripple
2. Improved efficiency compared to conventional PFC
3. Smaller passive components due to current sharing

Disadvantages:

1. More complex control and design
2. Increased component count
3. Potential for imbalance between phases

2.3. Bridgeless PFC Converter: Bridgeless topologies have attracted much interest to surpass the constraints of traditional PFC converters. Bridgeless PFC converters can be more efficient by cutting the number of semiconductor devices in the present path. Among the several bridgeless topologies are the bridgeless boost, bridgeless SEPIC, and bridgeless cûk converters. Some bridgeless designs may experience higher electromagnetic interference (EMI) or more complicated control needs even while they enhance efficiency [21].

2.1.2. DC-DC converters for battery charging:

A battery charger's DC-DC stage offers isolation and exact voltage/current control for the battery. There are several topologies available, each with its trade-offs.

2.1 Flyback Converter: For low power uses (<150W), flyback converters are straightforward and affordable. Its application in higher power uses is constrained, though, by significant transformer leakage inductance and high switch stress [22].

2.2 Forward Converter: Appropriate for medium power levels—up to a few hundred watts. Though it needs a reset mechanism for the transformer core and may have more switch voltage stress, it provides better efficiency and power handling than flyback [23].

2.3 LLC Resonant Converter: High efficiency is its hallmark since it can run at high switching frequencies and ZVS capability across a broad load range. Its output voltage control range, though, may be constrained and its complexity greater, particularly for broad output voltage changes common in battery charging [24].

2.2. Proposed Configuration

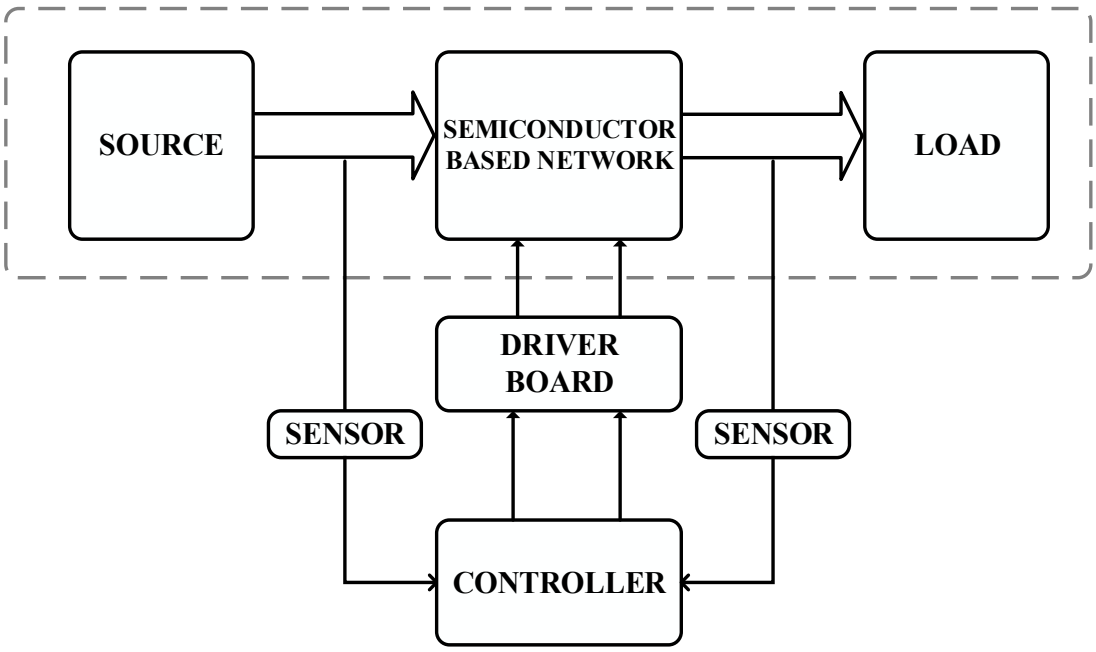

Fig.2.1 Proposed Block Diagram for Battery Charger

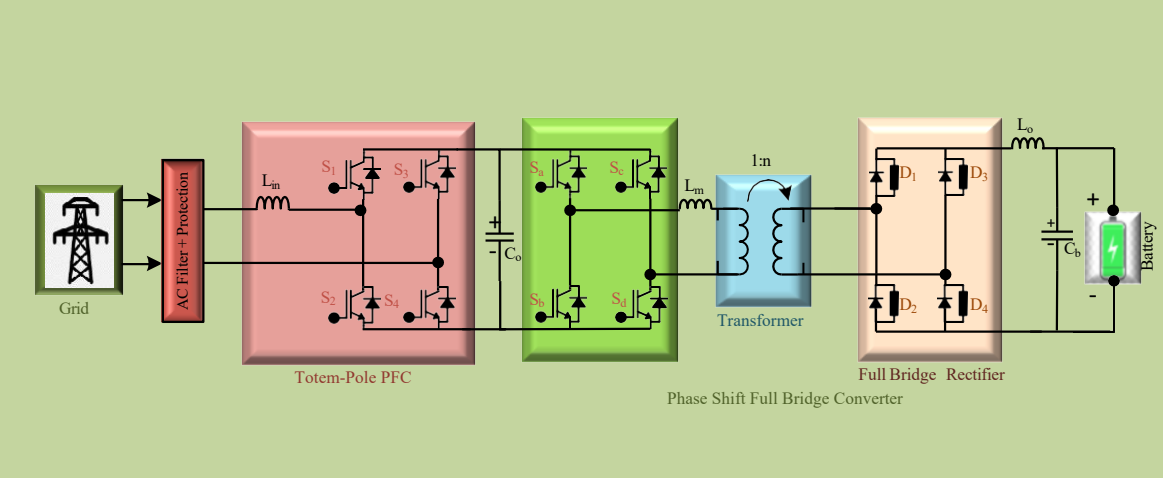

Fig.2.2 Proposed Battery Charger Configuration

2.2.1. Totem-Pole PFC Converter:

With the possibility of very high efficiency (almost 99%) and great power density, the totem-pole PFC converter has become a very promising bridgeless topology. Usually MOSFETs, this topology substitutes actively controlled switches for the input diode bridge [25]-[35].

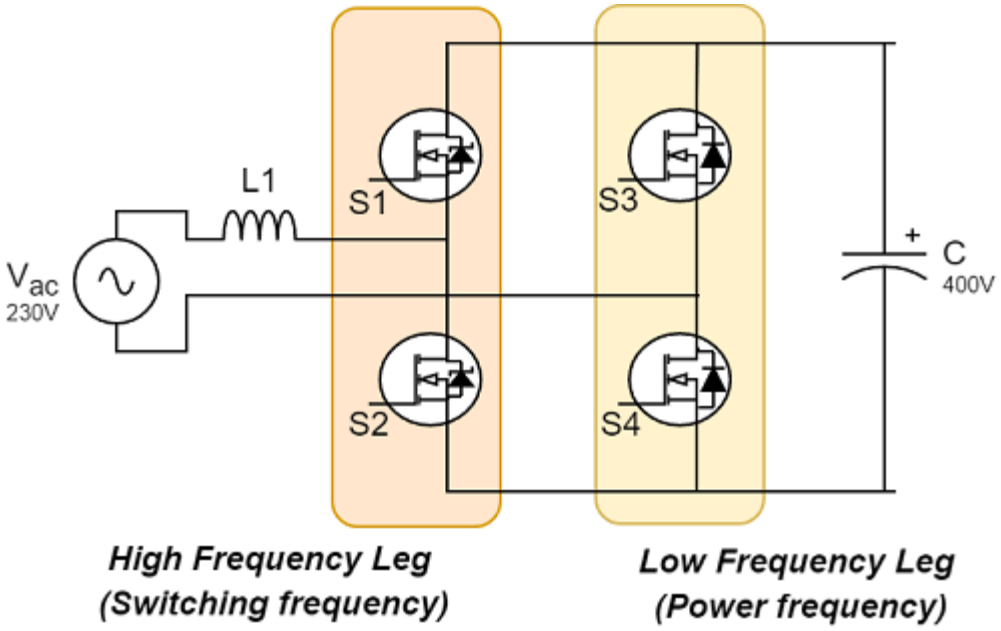

Fig.2.3. Totem Pole Power Factor Correction Configuration

Benefits of Totem-Pole PFC:

1. High Efficiency: Removes the voltage drop and losses linked to the diode bridge. The use of wide-bandgap (WBG) semiconductors like Gallium Nitride (GaN) and Silicon Carbide (SiC) MOSFETs further reduces conduction and switching losses, enabling operation at higher frequencies.

2. Reduce Component Count: Compared to certain other bridgeless topologies, it may have a straighter forward power loop design.

3. High Power Density: WBG devices' higher switching frequencies allow for smaller passive components (capacitors, inductors).

Difficulties of Totem-Pole PFC:

Control Complexity: Especially for attaining continuous conduction mode (CCM) operation and controlling zero-crossing distortions, it calls for advanced control techniques. Many times, digital control is preferred.

Switching Loss in Slow Lag: In the traditional totem-pole PFC, one leg switches at line frequency (slow leg) and the other at high frequency (fast leg). If not controlled correctly, the body diodes of the MOSFETs in the slow leg can experience considerable reverse recovery losses, especially with silicon MOSFETs. Highly beneficial in reducing this problem are GaN devices, with their zero reverse recovery charge.

Dead Time Management: Dead-time control is essential to avoid shoot-through in the high-frequency leg.

EMI: While offering high efficiency, careful design is needed to manage EMI due to high dv/dt and di/dt.

Recent research in totem-pole PFC focuses on advanced control techniques (e.g., adaptive dead-time control, zero-voltage switching (ZVS) for the fast leg), the use of GaN and SiC devices to push efficiency and frequency limits, and thermal management solutions for high-power-density designs.

2.2.2. Phase Shift Full Bridge Converter (PSFB):

The Phase Shift Full Bridge (PSFB) converter is a popular choice for medium to high-power isolated DC-DC applications (hundreds of watts to several kilowatts) since it can provide ZVS for the primary switches, so lowering switching losses and ZVS.

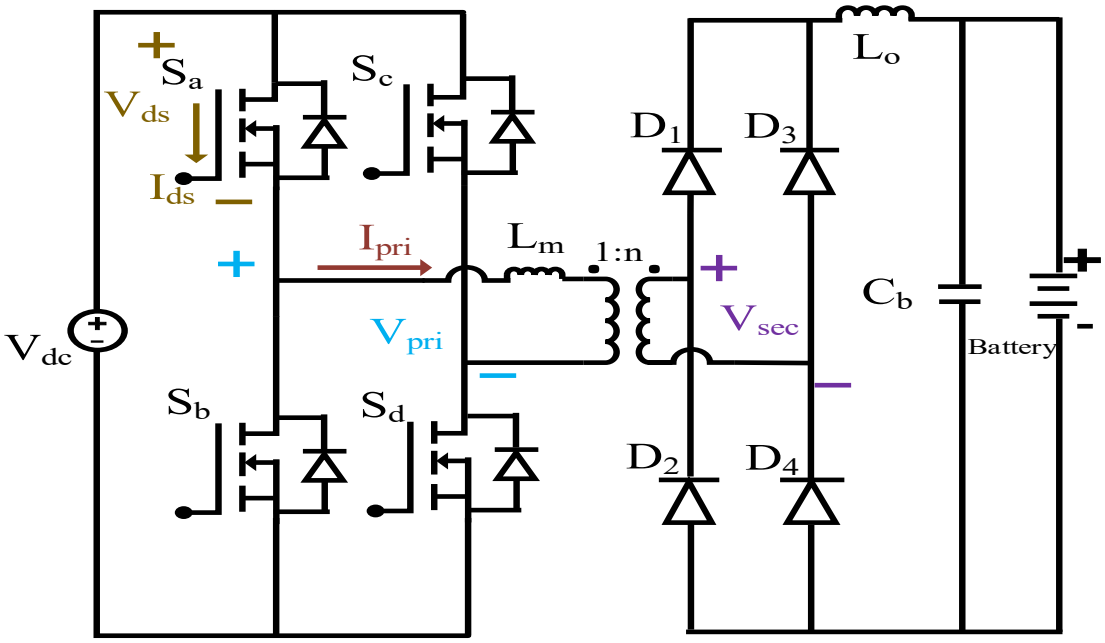

Fig. 2.4. Phase Shift Full Bridge Converter

1. Benefits of PSFB Conversion

1. **Zero Voltage Switching (ZVS):** Primary switches' capacity to reach zero voltage

switching (ZVS) over a significant load range produces high efficiency.

2. **High Power Capability:** Appropriate for charging high power applications
3. **Galvanic Isolation**: The high-frequency transformer offers galvanic isolation as Protection of Battery
4. **Constant Frequency operation**: Reduces magnetic control and design complexity.

2. Challenges of Phase Shift Full Bridge (PSFB) Converter:

1. Especially under light loads, circulating currents could run in the primary side and raise conduction losses during the freewheeling period.
2. Keeping ZVS under light load conditions can be difficult and usually calls for altered control techniques or auxiliary circuits.
3. Reverse recovery losses and notable voltage ringing can affect the secondary side rectifier diodes. Efficiency is usually increased by synchronous rectification using MOSFETs [37].

4. The design must consider the loss of effective duty cycle caused by the leakage inductance of the transformer.
5. Complexity: More complex than simpler topologies, such forward converters or flyback [38].

Chapter 3
System Design of the Battery Charger

3.1. Introduction

A Totem-Pole Power Factor Correction (PFC) and a Phase Shift Full Bridge (PSFB) converter are the two stages of a power conversion design used in battery charging systems. With a high power factor and low harmonic distortion, this configuration is designed to effectively convert AC power to the DC power required for battery charging. Every stage is optimally designed to improve the power factor, provide high galvanic isolation, and enable efficient direct current (DC) conversion to reduce energy loss and provide uniform system operational efficiency. The initial stage of this configuration is a Totem-Pole Power Factor Correction (PFC) circuit, which offers maximum efficiency by synchronising the input voltage and current. The DC output of the PFC stage is used as an input to the second stage, thus providing efficient and continuous power transmission across the system.

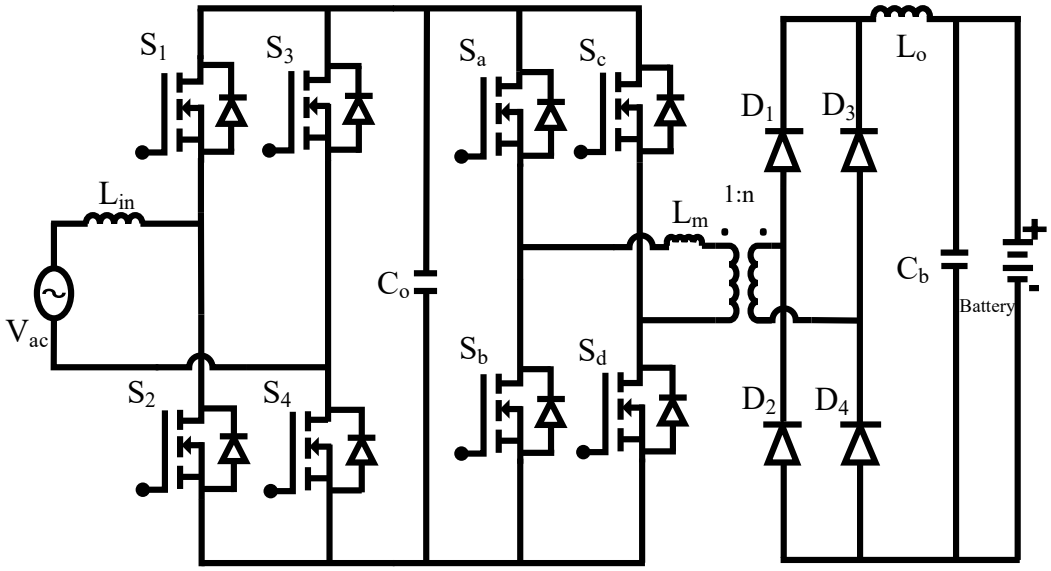

Fig. 3.1 Battery Charger Configuration

3.2. Totem Pole Power Factor Correction

Traditional Power Factor Correction (PFC) methods, like the traditional boost PFC, are in common use in a variety of applications.

A totem pole converter is a derived topology of a boost-PFC converter, and it achieves higher efficiency compared to all the other boost-PFC derived topologies.

This figure shows the circuit for the totem pole converter:

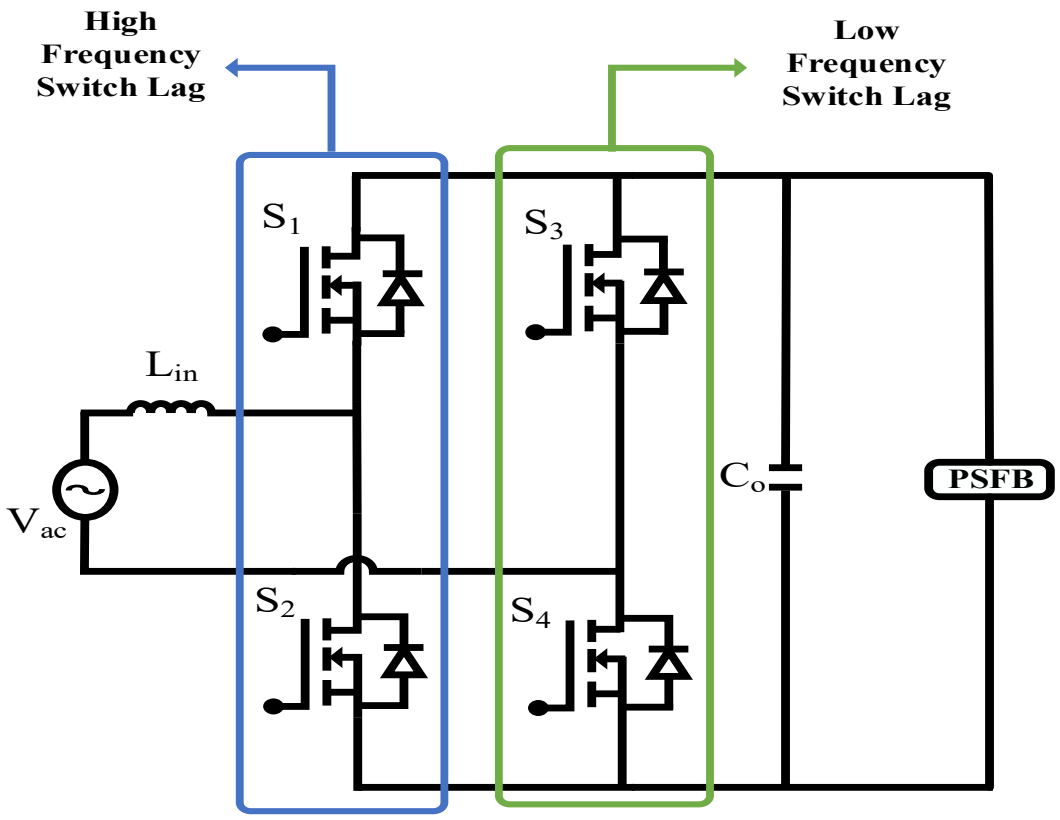

Fig. 3.2 Totem Pole PFC Configuration

One of the greatest strengths of Totem-Pole PFC is that it significantly improves power factor performance with high efficiency and smaller component sizes. Additionally, the enhanced power quality favours the overall power system, lowering the grid load by improving equipment reliability. Out of the three types discussed, the Totem-Pole PFC converter is the most compact and efficient. It is a great option for contemporary battery charging systems due to its high efficiency, low total harmonic distortion (THD), and reduced component count.

It is especially appropriate for applications where efficiency and power density are crucial, despite its higher initial cost and more intricate control requirements.

A high-frequency leg and a low-frequency leg make up a totem pole converter. The switching frequency is used by the high-frequency leg. Wide band gap (WBG) devices are used in the high-frequency legs because they have low switching energy and faster switching times.

Power frequency is used by the low-frequency leg. MOSFETs or silicon-based diodes are used in low-frequency legs to provide unidirectional or bidirectional power flow.

For the high-frequency and low-frequency legs of the model, silicon carbide (SiC) and silicon (Si) based MOSFETs are used. The controller keeps the intermediate capacitor voltage at a predetermined level while achieving unity power factor (UPF) at the supply terminals.

Table 3.1. Comparative Table of Different Topology for PFC

Features	Conventional PFC	Interleaved PFC	Totem-Pole PFC
Topology	Boost Converter	Multiple Boost Converters	Bridgeless
Efficiency	~90-95%	~95-97%	>98%
Power Factor	~0.95	~0.98	~0.99
THD	Higher	Moderate	Low
Inductor Size	Large	Medium	Small
Capacitor Size	Large	Medium	Small
Component Count	Low	High	Low
Control Complexity	Simple	Moderate	High
Cost	Low	Moderate	High

The totem-pole PFC structure establishes a new benchmark in performance and efficiency for power factor correction. By achieving high-frequency operation and reduced conduction losses, the design comfortably addresses the expanding requirements of emerging power electronics. Its efficiency-centred design also advances a more power-efficient energy platform to the advantage of the grid infrastructure[20] and end users in terms of improved power quality and lower aggregate energy consumption. This leads to making this topology a trending choice as a PFC circuit, but the complexity in controlling the circuit makes this more complex to implement in the battery charger.

3.3. Phase Shift Full Bridge (PSFB) Converter

Following the Power Factor Correction (PFC) phase, the controlled direct current (DC) voltage is converted into a high-frequency alternating current (AC) signal through a Phase-Shift Full Bridge (PSFB) Converter. The AC signal, which has a square wave nature, is filtered through a particular two-winding transformer that doubles as a galvanic isolation and output voltage adaptation to charging battery specifications. The transformer provides an efficient and stable power supply regardless of load changes.

Diodes rectify the AC output to produce a stable DC voltage for battery charging. The optimal design practices are employed to minimise conduction and switching losses to a large degree, contributing to higher efficiency, longer component life, and higher overall system reliability. In Figure 4, a full-bridge converter with a diode rectifier. Phase-Shift Full Bridge (PSFB) is common in high-performance power supplies with faster transient response, high power density and high converter efficiency. Automotive and aerospace uses also need high power density, as lightweight means that transport carriers will have improved energy efficiency. Increasing the converter switching frequency helps to lower the weight by lowering the magnetic volt-seconds and hence its size. Higher switching frequency results in more regular hard-switching transients, which leads to larger switching losses. Increasing the turn-on speed to lower the overlapped area may help to lower switching losses, but a faster voltage-changing slew rate will produce more noise and electromagnetic interference. Conversely, soft-switched turn-on is accomplished by letting the negative drain-to-source current discharge the MOSFET output capacitor voltage prior to the gate voltage rising. One of the best things about the PSFB topology is that it can make the primary-side MOSFETs switch at zero voltage (ZVS). To get ZVS, you usually use the energy stored in the transformer's leakage inductance (or an externally added resonant inductor, L_m) to charge and discharge the output capacitances (C_b) of the MOSFETs during the dead time between the switching transitions of the devices in each leg. When the voltage across the MOSFETs is already zero (or very near to it), turning them on greatly cuts down on the switching losses that happen when voltage and current overlap at the same time. This lets the device work at greater switching frequencies, which means fewer magnetic parts and capacitors and higher power density, with just a minor drop in efficiency.

But the resonant transitions that ZVS needs cause something called "Duty cycle loss." This is the part of the switching period when the primary current is changing direction through the resonant inductor and the voltage across the transformer primary is almost zero, which means that no power is being sent to the secondary. The design needs to take this loss in effective duty cycle into account, especially when a wide variety of output voltages is needed.

There are different ways to rectify on the secondary side. A current doubler rectifier is often the best choice for applications that need a lot of output current, like charging batteries. This is because it splits the output current across two inductors, which can cut down on conduction losses, improve thermal distribution, and make magnetic components smaller. To cut down on rectification losses, modern high-efficiency PSFB converters nearly often use synchronous rectifiers (SRs) with MOSFETs instead of diodes.

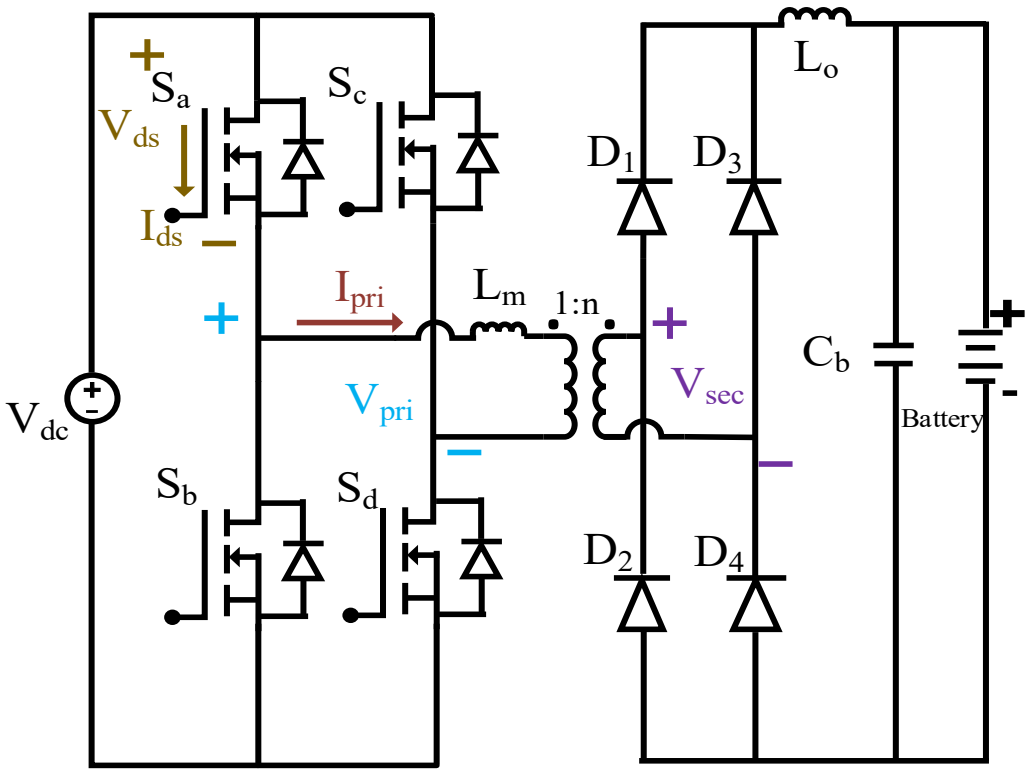

Fig. 3.3. Phase-Shift Full Bridge (PSFB) Converter

The absence of current and voltage overlap at the MOSFET turn-on transient causes no turn-on switching losses, which enables the PSFB to run at a high switching frequency and keep great efficiency at the same time. Because it can be constructed highly effectively, galvanically isolated, and with low switching losses, this PSFB converter is a structure that is commonly employed in high-power applications like battery chargers. Power Supply Units (PSUs) for AI and

edge computing with quick load transients, as well as battery charger applications, including electric vehicle.

3.1.1. Benefits of Phase Shift Full Bridge Converter: The isolation is yet another essential advantage of the PSFB topology, and it occurs through a high-frequency transformer. This isolation provides safety by offering electrical insulation between the battery and voltage grid, thereby protecting user and the battery. Also, the transformer provides the added advantage of voltage transformation such that, the charger can handle a broad spectrum of input and output voltage levels.

3.1.2. Losses in PSFB Converter: Transformer windings and power switches both have conduction losses from current flow, and core losses within the transformer through magnetic hysteresis and eddy currents etc.

3.1.3. Relevance in Battery Charging: In battery charging systems, the Phase-Shift Full Bridge (PSFB) converter is the preferred choice since it can handle high levels of power efficiently while minimizing thermal stress. Its galvanic isolation capability makes it safety-compliant, and its adaptive voltage conversion capability allows it to support a range of battery configurations.

3.4. Mode of Operations of Charger

The Totem-Pole PFC offers a high-power factor in addition to high-efficiency AC-DC conversion, and the Phase Shift Full Bridge (PSFB) converter offers isolated DC-DC conversion.

3.4.1. **Positive Half-Cycle Operation**

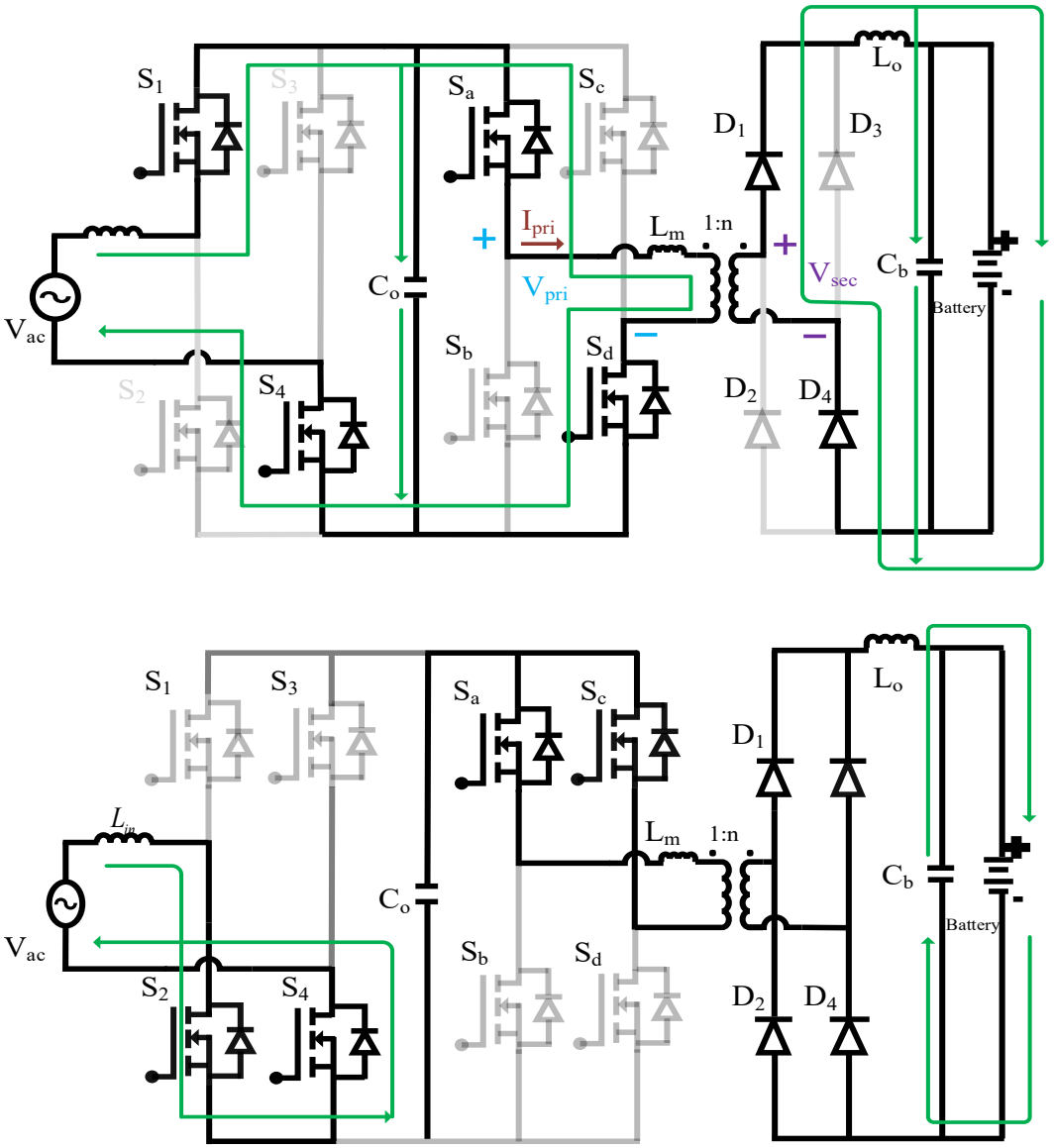

Fig. 3.4. Positive Cycle for Input AC: Mode of Operations

In the positive half cycle of the AC input, the Totem-Pole Power Factor Correction (PFC) S_3 is turned off and S_4 is turned on at the grid frequency, steering the inductor current too closely to follow the rising slope of the line voltage and increasing and charging energy onto the DC link capacitor. The Phase-Shift Full Bridge (PSFB) converter then accurately controls power transmission to the battery by phase relationship modulation of its bridge

switches. A phase difference is created between leg 1 MOSFET driving signals (S_a and S_b) and leg 2 MOSFETs driving signals (S_c and S_d), while all four driving signals keep their duty cycle unchanged. This Phase-Shifting reduces switching losses and enhances overall efficiency, especially during varying load or line conditions.

Mode 1. During this phase of the switching sequence for the positive half cycle, the S_1 switch remains on and the S_2 switch stays inactive. Consequently, current from the AC source passes through the input inductor L_{in}, temporarily storing energy before delivering it to the DC link. Within the PSFB converter, switches S_a and S_d are enabled, forming a conduction path to the primary of the transformer, and the secondary winding conducts the current to the battery. With the help of the rectifier circuit at the secondary side of the transformer, which transfers the energy to capacitor C_b, thereby boosting the DC link voltage to the desired level.

Mode 2. After the inductor has supplied its stored energy, switch S_1 is turned off while switch S_2 is activated, putting the circuit into a freewheeling phase. During this interval, the system accumulates additional energy in the output capacitor, bolstering the DC link before the following conduction path. In the PSFB section, switch S_d is deactivated to facilitate current freewheeling through S_a and S_c. This free-wheeling path continues a constant current flow without inducing sudden voltage or current oscillations in the primary winding of the transformer. On the secondary side, the transformer voltage returns to zero and the output inductor starts to release its energy to the load.

3.4.2. Negative Half Cycle:

During the negative half of the AC input supply, the Totem-Pole PFC S_3 is turned on and S_4 is turned off all the time at grid frequency stage, carefully managing conduction paths to ensure inductor current follows while channeling energy onto the DC link capacitor. Through judicious switching control, the circuit retains a high-power factor, minimizes distortion, and provides a robust high-voltage rail for the subsequent converter.

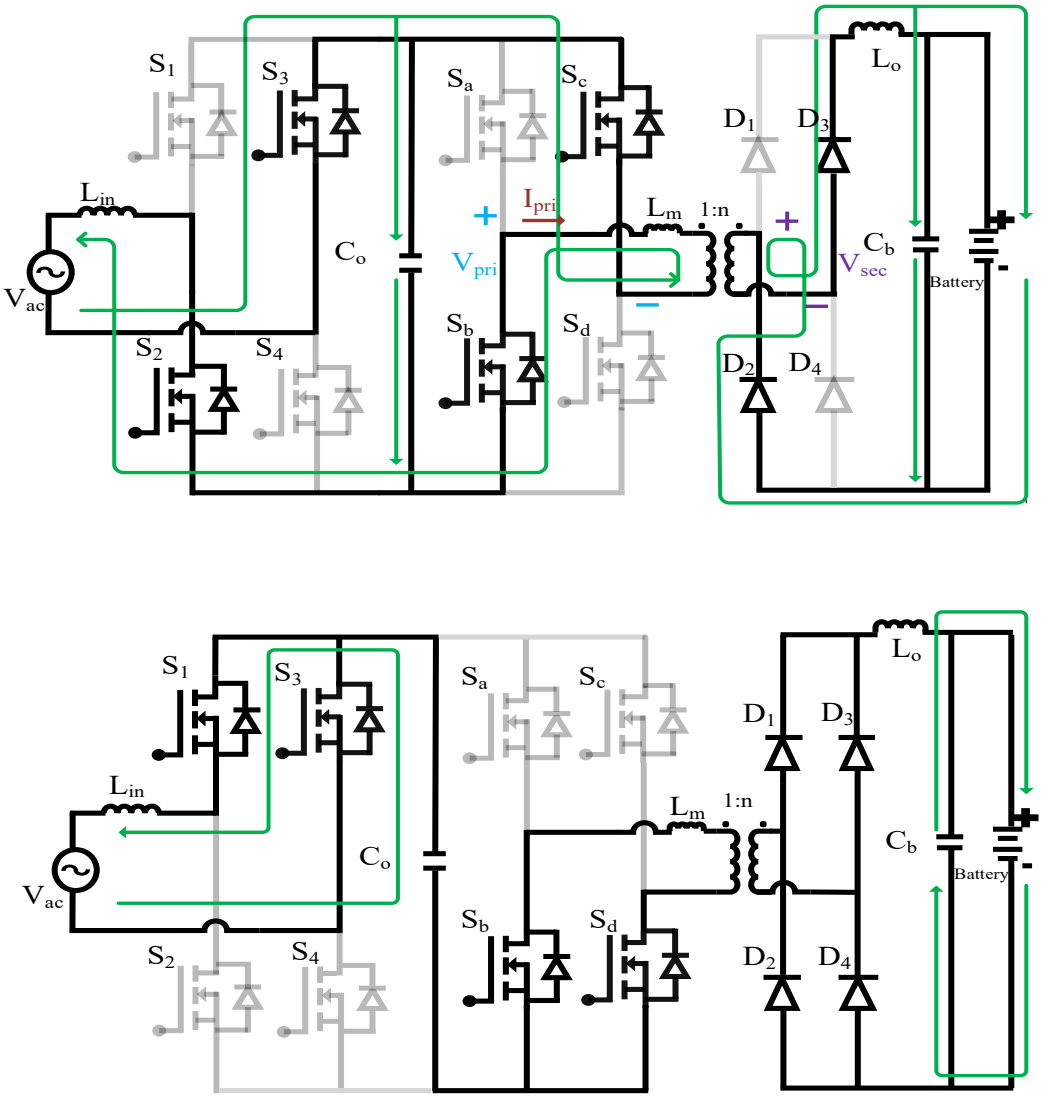

Fig. 3.5. Negative Cycle for Input AC: Mode of Operations

Mode 3. During this mode, switch S_1 is switched on while switch S_2 is kept off, creating a path that directs the inductor current through switch. In the corresponding Phase-Shift Full Bridge (PSFB) stage, switches S_b and S_c are

reactivated to drive current through the primary winding of the transformer. On the transformer's secondary side, D_3 and D_4 conduct, sending electrical power to the battery and supporting the regulated output voltage. This stage leads to providing a stable output at the battery terminal for continued charging.

Mode 4. In the final segment of the switching sequence for the negative half cycle, switch S_1 remains active while S_2 remains off, permitting the output capacitor C_0 to receive charge. Within the PSFB converter, switch S_c is deactivated, allowing the primary current to freewheel through S_c and S_d. On the secondary side, the transformer sees zero volts across its terminals, resulting in the output inductor discharging into the load. This synchronised control maintains a constant output current and voltage and prevents unnecessary stress on the converter components.

Table3.2. Different Switching Cycle for TotemPole PFC

Switch	Positive AC Voltage Cycle	Negative AC Voltage Cycle
S1	Working as a synchronous switch	Working as a control switch
S2	Working as a control switch	Working as a synchronous switch
S3	Permanently off	Permanently on
S4	Permanently on	Permanently off

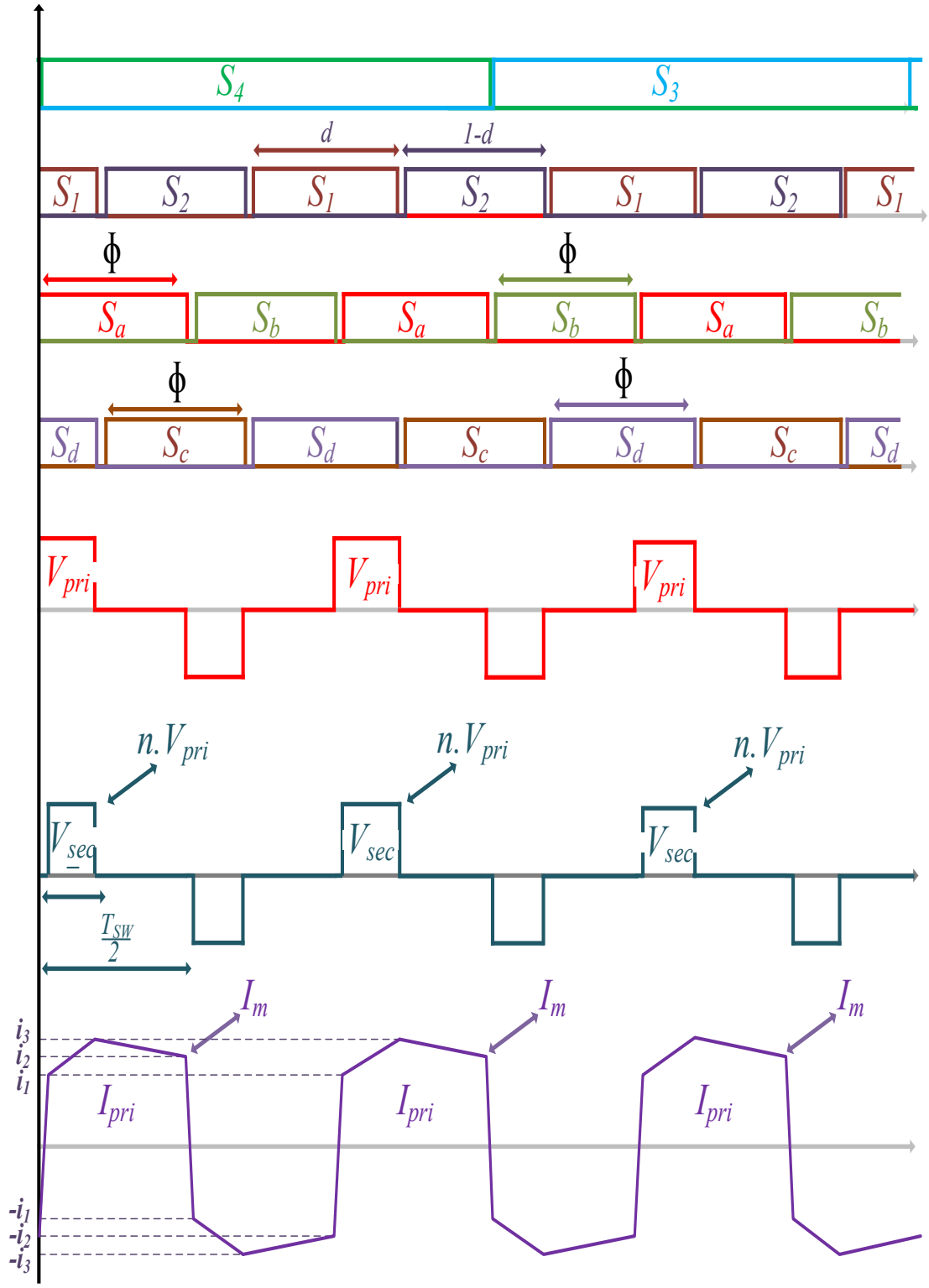

Fig. 3.6. Switching Cycle, Primary, Secondary Voltage and Primary Current of Transformer

Chapter 4
Designing of Proposed Charger

4.1. Totem Pole PFC Designing

The totem-pole PFC topology usually has two high-frequency switches, and two low-frequency switches set up in a full-bridge configuration that is directly connected to the AC line and does not have an input diode rectifier. SiC or GaN MOSFETs are often used for the high-frequency switches that do the PWM chopping. This helps reduce switching losses and lets the system work at high frequencies. In some setups, the low-frequency switches can be Si MOSFETs or even diodes. These switches change at the AC line frequency.

4.1.1. Input Filter Inductor (L_{in}) Design

The input inductor in a totem-pole PFC stage is an important part that shapes the input current, limits ripple and keeps the system running smoothly [39].

Purpose: The main jobs of the input inductor (L_{in}) are to keep the CCM running by limiting the input current ripple, filter out the high frequency switching components, and help turn the input current into a sine wave that is in phase with the input voltage. This gives a high-power factor and low THD.

Minimum Inductance (L_{inmin}): The inductance value is mostly set to keep the peak-to-peak current ripple (ΔIL_{in}) below a specific percentage of the maximum peak input current. This percentage is usually between 20% and 40%. This makes sure that CCM works and keeps the strains on the parts in check.

An equation for the minimum inductance, derived from the [40] guide, is:

$$L_{min} = \frac{D \cdot (1 - D) \cdot V_{\text{out}}}{I_{\text{ripple}}\% \cdot F_{\text{swpfc}}}$$

$$L_{min} = \frac{0.5 \times (1 - 0.5) \times 400}{0.3 \times 16 \times \sqrt{2} \times 100 \times 10^3} = 147\mu H$$

Or

$$L = \frac{1}{\text{Ripple}} * \frac{V_{ac}^2}{P_O} * (1 - \frac{\sqrt{2} * V_{ac}}{V_O}) * T$$

To maintain CCM operation, the minimum inductance value can be calculated when the duty cycle D=0.5, where D is the duty cycle, V_{out} is the PFC output DC voltage, $I_{ripple}\%$ is the desired peak-to-peak ripple current as a percentage of the peak input current, and F_{sw} is the switching frequency. In PFC applications, the duty cycle $D(t) = 1 - \frac{V_{\text{in}}(t)}{\text{Vout}}$ varies with the instantaneous AC input voltage $V_{in}(t)$. This condition typically occurs when the instantaneous input voltage $|V_{\text{in}}(t)| = \frac{V_{\text{out}}}{2}$. The design should consider the operating point that results in the maximum required inductance or the minimum inductance that satisfies ripple constraints across the entire line cycle.

Since the switching current in a PFC application varies across the AC-line cycle, the average inductor current can be used to calculate the average switching losses across the AC-line cycle. The average input current is given as [41]:

$$I_{L.avg} = \frac{P_o}{V_{ac}} \cdot \frac{2 \cdot \sqrt{2}}{\pi}$$

$$I_{L,avg} = \frac{550}{230} \times \frac{2 \times \sqrt{2}}{3.14}$$

$$= 2.15\text{A}$$

4.1.2. Maximum Inductor Current (IL_{max}): The inductor must be designed to handle the peak current without its core saturating. This peak current typically occurs at the minimum RMS input voltage ($V_{in,rms,min}$) and full load. The equation from is:

$$IL_{\text{max}} = \frac{\sqrt{2} \times \text{Pout}}{V_{\text{in}}} \times \left[1 + \frac{\text{I}_{\text{ripple}}\%}{2}\right]$$

$$IL_{\text{max}} = \frac{\sqrt{2} \times 550}{230} \times \left[1 + \frac{0.3}{2}\right]$$

$$IL_{\text{max}} = 3.887\text{A}$$

where P_{out} is the output power. Core saturation must be avoided as it leads to a rapid decrease in inductance and a potentially damaging increase in current [42]. Maintaining low THD and EMI at full load is crucial for PFC applications, but so are light loads where the converter tends to operate in DCM mode and the inducer current is low. A swinging choke is typically utilized for this purpose because it offers both a controlled inductance at high load and a higher

inductance at low DC bias current.

The inductance vs DC bias of the AC choke is presented in figure 7.

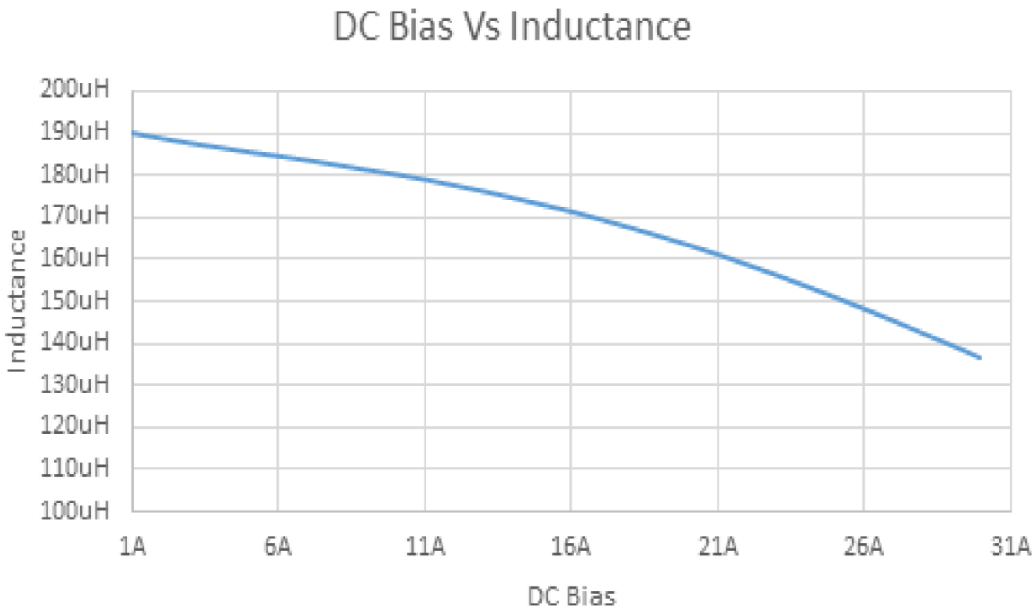

Fig 4.1: Totem-Pole PFC Input inductor: L vs DC bias [41]

4.1.3. Output DC Link Capacitor (C_o) Design: The DC link capacitor is an important part of the totem-pole PFC stage that stores and filters energy. The DC link capacitor (C_o) has several important jobs. It stabilizes the DC output voltage (V_o) that goes to the downstream DC/DC converter. It also stores energy to keep the output power steady during short AC line sags or dropouts (hold-up time). Finally, it filters out the low-frequency voltage ripple that is a normal part of the PFC rectification process (at twice the AC line frequency for a single-phase PFC system).

Sizing based on Hold-up Time (t_{hold}): For applications that need to keep working during short AC power outages, the hold-up time requirement usually sets the minimum capacitance value. Using the energy balance concept, capacitance we need.

$$C_o \geq \frac{2 \cdot P_o \cdot t_{\text{hold}}}{V_o^2 - V_{o,\text{min}}^2}$$

$$C_{\text{o}} = \frac{2 \times 550 \times 10 \times 10^{-3}}{400^2 - 345^2}$$

$$= 2.68\mu F$$

where P_o is the output power, t_{hold} is the required hold-up time, V_o is the nominal DC link voltage, and $V_{o,min}$ is the minimum allowable DC link voltage during the

hold-up period.

Sizing based on Output Voltage Ripple (ΔV_o): The capacitor must also be large enough to limit the peak-to-peak voltage ripple at twice the line frequency to an acceptable level for the downstream converter .

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{\text{line}} \cdot \Delta V_{o,pp} \cdot V_o}$$

$$C_o = \frac{550}{2 \times 3.14 \times 50 \times 0.2 \times 400} = 2.01\mu F$$

Therefore, 2.68 μF is the minimum required DC capacitance to fulfil these two criteria.

Capacitor Selection: The final capacitance value chosen should be the larger of the values calculated from the hold-up and ripple requirements. Often, multiple capacitors are paralleled to achieve the required total capacitance, improve RMS current handling, and reduce overall ESR and ESL.

4.2. Phase Shift Full Bridge Converter Designing:

The PSFB converter is a popular choice for the isolated DC/DC stage in high-power battery chargers due to its ability to achieve high efficiency and power density [43].

4.2.1. Output Inductor and Capacitor Filter Designing (L_o and C_b): The LC output filter is important because it changes the high-frequency rectified voltage from the transformer secondary into a smooth DC output that may charge a battery.

The output filter, which has an inductor (L_o) and a capacitor (C_b), turns the pulsing DC voltage from the secondary-side rectifier into a stable DC output voltage. It reduces the voltage ripple at the switching frequency and its harmonics, and it stores energy to keep the output voltage steady when the load varies quickly.

Design of the Output Inductor (L_o): The main job of the output inductor is to keep the peak-to-peak output current ripple (ΔIL_o) at a certain level, usually a percentage of the whole load current (for example, 10–30%), while making sure that Continuous Conduction Mode (CCM) works over the whole load range.

The voltage across an inductor can be found using the equation $V_L = L\frac{di}{dt}$. During the part of the switching cycle when power comes from the secondary, the voltage across the inductor is about $V_{L,on} = V_{\text{rect,avg}} - V_{\text{out}}$ which $V_{\text{rect,avg}}$ is the average rectified voltage that comes before the filter. Vout is the output voltage. $V_{L,off} = V_{\text{rect,avg}} - V_{\text{out}}$ throughout the freewheeling phase.

$$\Delta I_{L_o} = \frac{V_{\text{in,ref}}(1 - \text{D}) \cdot T_{\text{sw}}}{2 \cdot L_o}$$

is the ripple current, where $T_{sw} = \frac{1}{f_{sw}}$ is the time it takes to switch. A simpler calculation for lowest inductance, based on 1 (originally for an PSFB but usable in principle), takes into account the highest voltage that may be applied to the inductor and aims for a certain maximum ripple current.

$$L_{o,min} = \frac{V_{in,ref,max}}{4 \cdot \Delta I_{out,ripple,max} \cdot 2 \cdot f_{sw}}$$

$$L_{o,min} = \frac{400}{8 \cdot 0.8 \cdot 100 \cdot 10^3}$$

$$L_{o,min} = 0.00625\text{H}$$

$V_{in,ref,max}$ is the maximum effective voltage that drives the inductor. It is the rectified secondary voltage minus the output voltage, which happens at a duty cycle that maximizes this difference or ripple. $\Delta I_{out,ripple,max}$ is the maximum peak-to-peak output inductor current ripple that is allowed. If the highest ripple happens when the effective duty cycle for charging the inductor is 0.5 is what gives birth to the factor of 4 (or 8 in the modified form).

Output Capacitor (C_b) Design: The output capacitor is sized primarily to limit the peak-to-peak output voltage ripple (ΔV_o) caused by the inductor current ripple flowing through it, and to meet transient response requirements during sudden load changes. The voltage ripple due to the capacitance itself can be approximated by considering the charge accumulated/discharged by the ripple current:

$$\Delta V_{o,cap} = \frac{\Delta Q}{C_o} = \frac{1}{C_o}\int i_C(t)dt$$

For a triangular inductor current ripple, the charge stored/released by the capacitor over a quarter of the ripple period (assuming ripple frequency is $2 \cdot f_{sw}$) is approximately

$$\frac{1}{2} \cdot \frac{\Delta I_{L_o,max}}{2} \cdot \frac{T_{sw}}{2} = \frac{\Delta I_{L_o,max}}{8 \cdot f_{sw}},$$

This leads to,

$$C_{o,\min} \approx \frac{\Delta I_{L_o,max}}{8 \cdot f_{sw} \cdot \Delta V_{o,pp,max}}$$

Where, $V_{o,pp,max}$ is the maximum allowable peak-to-peak output voltage ripple.

Here the difference in the denominator (8 vs. 16) can arise from definitions of ripple frequency or how the charge is calculated. It is crucial to use consistent definitions, So

$$C_{o,\min} \approx \frac{\Delta I_{L_o,max}}{16 \cdot f_{sw} \cdot \Delta V_{o,pp,max}}$$

Provides,

$$C_o = \frac{\Delta I_{L_o} \cdot D_{\text{on}} \cdot T_{sw}}{\Delta V_{\text{o,ripple}}}$$

which is another form based on total charge during $D_{on.}$

4.3. Key Semiconductor and Passive Component Selection:

The battery charger's performance, efficiency, and reliability all depend on picking the right power semiconductors and passive parts. This part talks about things you should think about for these important pieces.

4.3.1. Power Semiconductor Selection (MOSFETs/IGBTs for PFC and PSFB):

The choice of switching devices is fundamental to achieving the desired performance metrics.

Totem-Pole PFC Switches: The high-frequency leg of the totem-pole PFC that does the PWM switching often uses Wide Bandgap (WBG) semiconductors like Silicon Carbide (SiC) MOSFETs or Gallium Nitride (GaN) HEMTs. People like these devices because they switch quickly, don't lose much power when they do, and can work at high temperatures. All these things help them get a lot of power in a small space and be very efficient. The low-frequency leg switches at the AC line frequency and can use regular Si MOSFETs or, in some designs that need to save money, diodes.

PSFB Switches: The main-side switches of the PSFB converter are usually high-voltage Si MOSFETs. SiC MOSFETs can also be used for PSFB designs or applications that need the most efficiency at very high frequencies, though. Most of the time, the secondary-side synchronous rectifiers (SRs) are low-voltage Si MOSFETs with very low R_{DS} (on) to cut down on conduction losses.

Table 4.1. : Comparison of Power Semiconductor Technologies (Si, SiC, GaN)

Parameter	**Silicon (Si) MOSFET**	**Silicon Carbide (SiC) MOSFET**	**Gallium Nitride (GaN) HEMT**
Typical RDS(on) per area	Higher	Lower	Lowest
Gate Charge (Qg)	Moderate to High	Lower than Si for similar rating	Lowest
Reverse Recovery (Qrr) of Body Diode	Significant	Very Low / Near Zero	No body diode (typically, but has reverse conduction mechanism)
Switching Speed	Slower	Faster	Fastest
Typical Vth	2-4 V	2-5 V (varies)	1-2 V (enhancement mode)
Cost	Lowest	Higher	High, decreasing
Gate Drive Complexity	Mature, simpler	Requires higher V_{gs} (e.g., +20V/-5V), sensitive to ringing	Requires precise VGS (e.g., +6V/0V), very sensitive to overshoot, low $V_{gs,max}$
Operating Temperature	Lower Max Tj	Higher Max Tj	Moderate to High Max Tj

Table 4.2. Capacitor Technology Characteristics for Power Electronics

Capacitor Type	**Typical Capacitance Range**	**Typical Voltage Range**	**Relative ESL**	**Ripple Current Capability**
Aluminum Electrolytic	µF to F	Up to ~600 V	Moderate to High	Moderate
Tantalum Electrolytic	µF to mF	Up to ~75 V	Moderate	Moderate
Film (Polypropylene, Polyester)	nF to hundreds of µF	Up to kV range	Low	High
Ceramic MLCC (Class I: C0G/NP0)	pF to tens of nF	Up to kV range	Very Low	Moderate
Ceramic MLCC (Class II/III: X7R, X5R, Y5V)	nF to hundreds of µF	Up to ~100 V (higher for specialized)	Very Low	High

Table 4.3. Comparison of Different Control Strategies for Totem-Pole PFC and PSFB

Converter Stage	Control Mode	Key Characteristics	Pros	Cons	Typical Implementation
TotemPole PFC	Average Current Mode Control (ACMC)	Regulates average inductor current. Requires sinusoidal reference.	Well-understood, good current shaping.	Requires bidirectional current sensing and processing. May need d_{FF} for best THD.	Analog or Digital
TotemPole PFC	Peak Current Mode Control (PCMC)	Regulates peak inductor current. Requires slope compensation.	Fast response, inherent current limit.	Bidirectional sensing complex. Susceptible to noise. Stability needs care.	Analog or Digital
TotemPole PFC	Duty-Ratio Feedforward (d_{FF})	Pre-calculates duty based on V_{in} / V_{out} . Used with ACMC/PCMC.	Improves THD, reduces current loop burden, faster transient response.	Requires accurate V_{in} and V_{out} sensing.	Digital
PSFB	Voltage Mode Control (VMC)	Error amplifier output directly controls phase shift.	Simpler implementation, less sensitive to current noise.	Slower transient response. Requires DC blocking capacitor for transformer.	Analog or Digital
PSFB	Peak Current Mode Control (PCMC)	Primary current compared to voltage loop output to set phase shift.	Faster transient response, inherent current limit, potential for flux balancing.	Complex current sensing, noise sensitivity, requires slope compensation.	Analog or Digital
PSFB	Adaptive ZVS/Dead-time Control	Adjusts dead-times based on operating conditions.	Optimizes ZVS over wider range, improves efficiency.	Adds complexity, requires sensing/estimation of load/line.	Digital

Chapter 5

Mathematical Modelling and Analysis

5.1. Totem Pole PFC Converter:

The low-frequency bridge arm adjusts the current routes in totem-pole PFC during both positive and negative half-cycles of the input AC voltage. But its states stay symmetrical, which makes it easier to set up a single main circuit model [44] .

Basic State Equations

Let *d(t)* be the duty ratio, $i_{in}(t)$ be the inductor current, V_{co} the output voltage, and R be the load resistance

$$\begin{aligned} \mathbf{L}_{in}\frac{d\boldsymbol{i}_{\text{in}}(\boldsymbol{t})}{\boldsymbol{dt}} &= \boldsymbol{v}_{ac}(\boldsymbol{t}) - (\mathbf{1}-\boldsymbol{d}(\boldsymbol{t}))\boldsymbol{v}_{Co}(\boldsymbol{t}) \\ \mathbf{C}_{o}\frac{d\boldsymbol{v}_{C_o}(\boldsymbol{t})}{\boldsymbol{dt}} &= (\mathbf{1}-\boldsymbol{d}(\boldsymbol{t}))\boldsymbol{i}_{in}(\boldsymbol{t}) - \frac{\boldsymbol{v}_{C_o}(\boldsymbol{t})}{\boldsymbol{R}} \end{aligned} \tag{1}$$

$$\boldsymbol{d}(\boldsymbol{t}) = \begin{cases} \mathbf{1}, \mathbf{0} < \boldsymbol{t} < \boldsymbol{dT_s} \\ \mathbf{0}, \boldsymbol{dT_s} < \boldsymbol{t} < \boldsymbol{T_s} \end{cases}$$

The term **1−d(t)** in the equations corresponds to the interval when energy is transferred to the output load.

5.1.1. Large-Signal Modelling using Generalized State-Space Averaging (GSSA)

The model's accuracy depends on the order of the Fourier series expansion. We use first-order Fourier coefficients in our analysis to find a middle ground between accuracy and complexity.

5.1.2. Derivation of 0-Average Index Equations

The 0-average (DC component) equations are derived from the basic state equations, D_{avg} be the average duty cycle ($\langle d \rangle_0$).

The 0-average equations, adapted from with user-defined variables and considering Vac_{peak} as the amplitude of the input voltage that contributes to the $B \cdot Vac_{peak}$ term in the state-space model, are

$$\mathbf{L}_{in}\frac{d\langle i_{\mathrm{Lin}}\rangle_0}{dtc} = \mathbf{Vac}_{\mathrm{peak}} - \langle v_{\mathrm{Co}}\rangle_0 + \langle dv_{\mathrm{Co}}\rangle_0$$
$$\mathbf{C}_o\frac{d\langle v_{\mathrm{Co}}\rangle_0}{dt} = \langle i_{\mathrm{Lin}}\rangle_0 - \langle di_{\mathrm{Lin}}\rangle_0 + \frac{\langle v_{\mathrm{Co}}\rangle_0}{R} \quad (2)$$

Here, $\langle x\rangle_k$ is the k^{th} Fourier coefficient of variable x, satisfying

$$\langle x\rangle_k = \frac{1}{T}\int_{t-T}^{t} x(\tau)\cdot e^{-jk\omega t}dt$$

And in this research, define

$$\mathbf{Re}[\langle x\rangle_k] = \langle x\rangle_k^R,$$
$$\mathbf{Im}[\langle x\rangle_k] = \langle x\rangle_k^I$$

In above equations,

$$\langle dv_{\mathrm{Co}}\rangle_0 = \langle d\rangle_0\langle v_{\mathrm{Co}}\rangle_0 + 2\cdot(\langle d\rangle_1^R\langle v_{\mathrm{Co}}\rangle_1^R + \langle d\rangle_1^I\langle v_{\mathrm{Co}}\rangle_1^I),$$
$$\langle di_{\mathrm{Lin}}\rangle_0 = \langle d\rangle_0\langle i_{\mathrm{Lin}}\rangle_0 + 2\cdot(\langle d\rangle_1^R\langle i_{\mathrm{Lin}}\rangle_1^R + \langle d\rangle_1^I\langle i_{\mathrm{Lin}}\rangle_1^I)$$

Here, $\langle \mathbf{d}\rangle_1^{\mathbf{R}}$ and $\langle \mathbf{d}\rangle_1^{\mathbf{I}}$ are the real and imaginary parts of the first Fourier coefficient of the instantaneous duty cycle d(t) respectively, given by

$$\langle d\rangle_0 = d$$
$$\langle d\rangle_1^R = \frac{1}{2\pi}\int_0^{2\pi d}\cos(2\omega\tau)\mathrm{d}(\omega\tau) = \frac{\sin(2\pi d)}{2\pi}$$
$$\langle d\rangle_1^I = -\frac{1}{2\pi}\int_0^{2\pi \mathrm{d}}\sin(2\omega\tau)d(\omega\tau) = \frac{\cos(2\pi\mathrm{d})-1}{2\pi}$$

For example, the 0-average (DC) part of the inductor current derivative $d\langle i\ Lin\rangle\ 0\ /dt$ is affected by both average values and the products of the first-order harmonic components of the duty cycle and capacitor voltage, such as $\langle d\rangle_1^R\langle V_{Co}\rangle_1^R$.

$$\mathbf{L}_{in}\frac{d\langle i_{\mathrm{Lin}}\rangle_1}{dt} = \mathbf{Vac}_{\mathrm{peak}} - \langle v_{\mathrm{Co}}\rangle_1 + \langle dv_{\mathrm{Co}}\rangle_1 - j\mathbf{L}_{in}\omega_s\langle i_{\mathrm{Lin}}\rangle_1$$
$$\mathbf{C}_o\frac{d\langle v_{\mathrm{Co}}\rangle_1}{dt} = \langle i_{\mathrm{Lin}}\rangle_1 - \langle di_{\mathrm{Lin}}\rangle_1 - \frac{\langle v_{\mathrm{Co}}\rangle_1}{R} - j\mathbf{C}_o\omega_s\langle v\rangle_1 \quad (3)$$

Where,

$$\langle dv_{\mathrm{Co}}\rangle_1 = \langle d\rangle_0\langle v_{\mathrm{Co}}\rangle_1 + \langle d\rangle_1\langle v_{\mathrm{Co}}\rangle_0$$
$$= (\langle d\rangle_0\langle v_{\mathrm{Co}}\rangle_1^R + \langle d\rangle_1^R\langle v_{\mathrm{Co}}\rangle_0) + (\langle d\rangle_0\langle v_{\mathrm{Co}}\rangle_1^I + \langle d\rangle_1^I\langle v_{\mathrm{Co}}\rangle_0)j$$
$$\langle di_{\mathrm{Lin}}\rangle_1 = \langle d\rangle_0\langle i_{\mathrm{Lin}}\rangle_1 + \langle d\rangle_1\langle i_{\mathrm{Lin}}\rangle_0$$
$$= (\langle d\rangle_0\langle i_{\mathrm{Lin}}\rangle_1^R + \langle d\rangle_1^R\langle i_{\mathrm{Lin}}\rangle_0) + (\langle d\rangle_0\langle i_{\mathrm{Lin}}\rangle_1^I + \langle d\rangle_1^I\langle i_{\mathrm{Lin}}\rangle_0)j$$

5.1.3. Derivation of 1-Average Index Equations

Similarly, the 1-average (fundamental component at switching frequency ω_s) equations for the state variables are derived. Let $\omega=2\pi f_s$ be the angular switching frequency. Adapted from [33]

$$\mathbf{L}_{in}\frac{d\langle i_{\mathrm{Lin}}\rangle_1^R}{dt} = \mathbf{Vac}_{peak} + \langle d\rangle_1^R\langle v_{\mathrm{Co}}\rangle_0 + \mathbf{L}_{in}\omega\langle i_{\mathrm{Lin}}\rangle_1^I + (\langle d\rangle_0 - 1)\langle v_{\mathrm{Co}}\rangle_1^R$$

$$\mathbf{L}_{in}\frac{d\langle i_{\mathrm{Lin}}\rangle_1^R}{dt} = \langle d\rangle_1^I\langle v_{\mathrm{Co}}\rangle_0 - \mathbf{L}_{in}\omega\langle i_{\mathrm{Lin}}\rangle_1^R + (\langle d\rangle_0 - 1)(\langle v_{\mathrm{Co}}\rangle_1^I)$$

$$\mathbf{C}_o\frac{d\langle v_{\mathrm{Co}}\rangle_1^I}{dt} = -\langle d\rangle_1^R\langle i_{\mathrm{Lin}}\rangle_0 + (1 - \langle d\rangle_0)\langle i_{\mathrm{Lin}}\rangle_1^R - \frac{1}{R}\langle v_{\mathrm{Co}}\rangle_1^R - \mathbf{C}_o\omega\langle v_{\mathrm{Co}}\rangle_1^I$$

$$\mathbf{C}_o\frac{d\langle v_{\mathrm{Co}}\rangle_1^I}{dt} = -\langle d\rangle_1^I\langle i_{\mathrm{Lin}}\rangle_0 + (1 - \langle d\rangle_0)\langle i_{\mathrm{Lin}}\rangle_1^I - \mathbf{C}_o\omega\langle v_{\mathrm{Co}}\rangle_1^R - \frac{1}{R}\langle v_{\mathrm{Co}}\rangle_1^I \quad (4)$$

5.1.4. Complete Large-Signal State-Space Model

Combining the 0-average and 1-average equations, the GSSA large-signal model of the totem-pole PFC can be expressed in state-space form as:

$$\frac{dX}{dt} = A\cdot X + B\cdot Vac_{peak} \quad (5)$$

Where the state variable X,

$$X = [\langle i_{\mathrm{Lin}}\rangle_0, \langle v_{\mathrm{Co}}\rangle_0, \langle i_{\mathrm{Lin}}\rangle_1^R, \langle i_{\mathrm{Lin}}\rangle_1^I, \langle v_{\mathrm{Co}}\rangle_1^R, \langle v_{\mathrm{Co}}\rangle_1^I]^T$$

$$A = \begin{bmatrix} 0 & \frac{\langle d\rangle_0 - 1}{\mathbf{L}_{in}} & 0 & 0 & \frac{2\langle d\rangle_1^R}{\mathbf{L}_{in}} & -\frac{2\langle d\rangle_1^I}{\mathbf{L}_{in}} \\ \frac{1 - \langle d\rangle_0}{\mathbf{C}_o} & -\frac{1}{R\cdot \mathbf{C}_o} & -\frac{2\langle d\rangle_1^R}{\mathbf{C}_o} & -\frac{2\langle d\rangle_1^I}{\mathbf{C}_o} & 0 & 0 \\ 0 & \frac{\langle d\rangle_1^R}{\mathbf{L}_{in}} & 0 & \omega_s & \frac{\langle d\rangle_0 - 1}{\mathbf{L}_{in}} & 0 \\ 0 & \frac{\langle d\rangle_1^I}{\mathbf{L}_{in}} & -\omega & 0 & 0 & \frac{\langle d\rangle_0 - 1}{\mathbf{L}_{in}} \\ -\frac{\langle d\rangle_1^R}{\mathbf{C}_o} & 0 & \frac{1 - \langle d\rangle_0}{\mathbf{C}_o} & 0 & -\frac{1}{R\cdot Co} & -\omega \\ -\frac{\langle d\rangle_1^I}{\mathbf{C}_o} & 0 & 0 & \frac{1 - \langle d\rangle_0}{\mathbf{C}_o} & \omega_s & -\frac{1}{R\cdot \mathbf{C}_o} \end{bmatrix}$$

Where, the input matrix B,

$$\boldsymbol{B} = \left[\frac{\mathbf{1}}{\mathbf{L}_{\boldsymbol{in}}}, \mathbf{0}, \frac{\mathbf{1}}{\mathbf{L}_{\boldsymbol{in}}}, \mathbf{0}, \mathbf{0}, \mathbf{0}\right]^{\boldsymbol{T}}$$

At a steady-state operating point, the time derivatives of the state variables are zero, i.e., X˙=0. Therefore, the steady-state values of the Fourier coefficients, $\mathbf{X_{ss}}$, can be determined by :

$$X_{ss} = -A^{-1}\, B.u \tag{6}$$

$$\boldsymbol{X_{ss}} = [\langle \boldsymbol{i}_{\mathbf{Lin}} \rangle_{\mathbf{0}}, \langle \boldsymbol{v}_{\mathbf{Co}} \rangle_{\mathbf{0}}, \boldsymbol{i}_{\mathbf{Lin}}\rangle_{\mathbf{1}}^{\boldsymbol{R}}, \langle \boldsymbol{i}_{\mathbf{Lin}} \rangle_{\mathbf{1}}^{\boldsymbol{I}}, \langle \boldsymbol{v}_{\mathbf{Co}} \rangle_{\mathbf{1}}^{\boldsymbol{R}}, \langle \boldsymbol{v}_{\mathbf{Co}} \rangle_{\mathbf{1}}^{\boldsymbol{I}}]^{\boldsymbol{T}}$$

The time-domain inductor current $i_{Lin}(t)$ and output capacitor voltage $V_{Co}(t)$ can then be

reconstructed using these steady-state Fourier coefficients:

$$\begin{aligned} \boldsymbol{i}_{\mathrm{Lin}}(\boldsymbol{t}) &\approx \langle \boldsymbol{I}_{\mathrm{Lin}} \rangle_{\mathbf{0}} + \mathbf{2}\langle \boldsymbol{I}_{\mathrm{Lin}} \rangle_{\mathbf{1}}^{\boldsymbol{R}} \mathbf{cos}\,(\boldsymbol{\omega t}) - \mathbf{2}\langle \boldsymbol{I}_{\mathrm{Lin}} \rangle_{\mathbf{1}}^{\boldsymbol{I}} \mathbf{sin}\,(\boldsymbol{\omega t}) \\ \boldsymbol{v}_{\boldsymbol{Co}}(\boldsymbol{t}) &\approx \langle \boldsymbol{V}_{\boldsymbol{Co}} \rangle_{\mathbf{0}} + \mathbf{2}\langle \boldsymbol{V}_{\boldsymbol{Co}} \rangle_{\mathbf{1}}^{\boldsymbol{R}} \mathbf{cos}\,(\boldsymbol{\omega t}) - \mathbf{2}\langle \boldsymbol{V}_{\boldsymbol{Co}} \rangle_{\mathbf{1}}^{\boldsymbol{I}} \mathbf{sin}\,(\boldsymbol{\omega t}) \end{aligned} \tag{7}$$

Because the state variables have a low 1-average index and the injected perturbations happen seldom, small-signal linearization is mostly done with respect to the 0-average index.

5.1.5. Small-Signal Modelling:

The idea of "low-frequency disturbances" means that the small-signal model is best for looking at dynamics that are well below the switching frequency. This is a common feature of averaged models and limits the control bandwidth that can be achieved if this model is used to design a controller.

The variables that have been changed are:

$$\begin{aligned} \mathbf{d}(\boldsymbol{t}) &= \mathbf{D} + \boldsymbol{\Delta}\mathbf{d}(\boldsymbol{t}) \\ \mathbf{i}_{\boldsymbol{Lin}}(\boldsymbol{t}) &= \mathbf{I}_{\boldsymbol{Lin}} + \boldsymbol{\Delta}\langle \boldsymbol{i}_{\mathbf{Lin}} \rangle(\boldsymbol{t}) \\ \mathbf{v}_{\boldsymbol{co}}(\boldsymbol{t}) &= \mathbf{V}_{\boldsymbol{co}} + \boldsymbol{\Delta}\langle \boldsymbol{v}_{\boldsymbol{Co}} \rangle(\boldsymbol{t}) \end{aligned} \tag{8}$$

Where, D, I_{Lin}, V_{co}, respectively represent the steady-state d and corresponding steady-state values of the state variables.

Where $\boldsymbol{\Delta d_{avg}(t)}$, $\boldsymbol{\Delta\langle i_{\mathrm{Lin}}\rangle(t)}$, $\boldsymbol{\Delta\langle v_{Co}\rangle(t)}$ represent the injected low-frequency small perturbations satisfying,

$$|\boldsymbol{D}| \gg |\boldsymbol{\Delta d}(\boldsymbol{t})|, |\boldsymbol{I}| \gg |\boldsymbol{\Delta}\langle \boldsymbol{i}_{\mathbf{Lin}} \rangle(\boldsymbol{t})|, |\boldsymbol{V}| \gg |\boldsymbol{\Delta}\langle \boldsymbol{v}_{\boldsymbol{Co}} \rangle(\boldsymbol{t})|$$

Small-signal linearization is mostly done with respect to the 0-average index because the state variables have a low 1-average index and the injected perturbations happen infrequently.

We can get, by putting Eq. (6) and Eq. (8) into Eq. (5) and ignoring the second-order terms.

$$\frac{d\Delta\langle i_{\text{Lin}}\rangle_0}{dt} = M_{\text{custom}} \cdot \Delta d_{\text{avg}} + \frac{\mathrm{D}-1}{\mathrm{Lin}}\Delta\langle v_{\text{Co}}\rangle_0$$

$$\frac{d\Delta\langle v_{\text{Co}}\rangle_0}{dt} = N_{\text{custom}} \cdot \Delta d_{\text{avg}} - \frac{\mathrm{D}-1}{C_o}\Delta\langle i_{\text{Lin}}\rangle_0 - \frac{1}{R \cdot C_o}\Delta\langle v_{\text{Co}}\rangle_0$$

Where,

$$M_{custom} = \frac{2\cos(2\pi \mathrm{D})}{\mathrm{L}_{in}} \cdot \langle v_{\text{Co}}\rangle_1^R - \frac{2\,sin(2\pi D)}{\mathrm{L}_{in}} \cdot \langle v_{\text{Co}}\rangle_1^I + \frac{\langle v_{\text{Co}}\rangle_0}{\mathrm{L}_{in}}$$

$$N_{custom} = -\frac{2\cos(2\pi D)}{\mathrm{C}_o} \cdot \langle i_{\text{Lin}}\rangle_1^R + \frac{2\,sin(2\pi D)}{\mathrm{C}_o} \cdot \langle i_{\text{Lin}}\rangle_1^I - \frac{\langle i_{\text{Lin}}\rangle_0}{\mathrm{C}_o}$$

Performing a Laplace transformation,

$$\Delta\langle i_{\text{Lin}}\rangle_0 = \frac{M_{custom} \cdot \mathrm{s} + (\frac{M_{custom}}{\mathrm{RC}_o} + \frac{(\mathrm{D}-1)\cdot \mathrm{N}}{\mathrm{L}_{in}})}{\mathrm{s}^2 + \frac{\mathrm{L}}{\mathrm{RC}_o} \cdot \mathrm{s} + \frac{(\mathrm{D}-1)^2}{\mathrm{L}_{in}C_o}} \cdot \Delta\mathrm{d} \triangleq \mathrm{G_{id}} \cdot \Delta\mathrm{d}$$

$$\Delta\langle v_{\text{Co}}\rangle_0 \quad \mathrm{cc} = \frac{\frac{N_{custom}}{N_{custom}} \cdot \mathrm{s} - \frac{\mathrm{D}-1}{C_o}}{\mathrm{s} + [\frac{1}{\mathrm{RC}_o} + \frac{\mathrm{B}\cdot(\mathrm{D}-1)}{M_{custom}\mathrm{L}_{in}}]} \cdot \Delta\langle i_{\text{Lin}}\rangle_0 \triangleq \mathrm{G_{vi}} \cdot \Delta\langle i_{\text{Lin}}\rangle_0$$

5.2. Phase Shift Full Bridge Converter:

The duty ratio is defined by,

$$d = d_l + d_e \tag{9}$$

The characteristic values of the leakage and output inductor current waveform as shown in Fig 3.6 [45],

$$i_1 = \left[\frac{v_{dc}}{L_m} - \frac{n \cdot v_o}{L_o}\right] \cdot \frac{d_l}{2} \cdot \frac{T_{sw}}{2} \tag{10}$$

$$i_3 = \frac{n^2 \cdot v_{dc} - n \cdot v_o}{L_o + n^2 \cdot L_m} \cdot d_e \cdot \frac{T_{sw}}{2} + i_1 \tag{11}$$

$$\boldsymbol{i_2 = i_3 - \frac{n \cdot v_o}{L_o + n^2 \cdot L_m} \cdot (1 - d) \cdot \frac{T_{sw}}{2}} \tag{12}$$

The averaged rectified voltage is

$$v_{\text{rec}} = \frac{2}{T_{sw}} \cdot \int_0^{\frac{T_{sw}}{2}} \tilde{v}_{\text{rec}}(t) \cdot dt \tag{13}$$

$$v_{rec} = n \cdot v_{dc} \cdot d_e + n \cdot (i_1 - i_2) \cdot L_m \cdot \frac{2}{T_{sw}} \tag{14}$$

By replacing Equations (1)– (4) into Equation (6), the rectified voltage as function of V_o, V_{dc}, $\mathbf{d_l}$ and $\mathbf{d}$ [35] is obtained:

$$\boldsymbol{v_{rec}} = \frac{\boldsymbol{L_o \cdot v_{dc} \cdot n \cdot d - (L_o \cdot v_{dc} \cdot n + L_m \cdot v_o \cdot n^2) \cdot d_l + L_m \cdot v_o \cdot n^2}}{\boldsymbol{L_m \cdot n^2 + L_o}} \tag{15}$$

The average output inductor current is,

$$i_o = \frac{2}{T_{sw}} \cdot \int_0^{\frac{T_{sw}}{2}} \tilde{l}_L(t) \cdot dt \tag{16}$$

$$i_o = \frac{1}{2 \cdot n} \cdot [(i_1 - i_2) \cdot d + (i_2 - i_3) \cdot d_l + i_2 + i_3] \tag{17}$$

Equation (18) is obtained by integrating Equations (9)– (12) into Equation (17) and solving for d_l. Equation (18) shows that the operating point conditions determine the blanking time interval.

$$\boldsymbol{d_l = \frac{T_{sw} \cdot L_o \cdot L_m \cdot [v_{dc} \cdot n^2 \cdot (d^2 - 2 \cdot d) + v_o \cdot n] + 4 \cdot i_L \cdot ({L_o}^2 \cdot L_m \cdot n + L_o \cdot L_m^2 \cdot n^3)}{T_{sw} \cdot ({L_o}^2 \cdot v_{dc} - L_m^2 \cdot v_o \cdot n^3 - L_o \cdot L_m \cdot v_{in} \cdot n^2 + d \cdot L_o \cdot L_m \cdot v_{dc} \cdot n^2)}} \tag{18}$$

$$\boldsymbol{i_{in} = \frac{2}{T_{sw}} \cdot \int_0^{\frac{T_{sw}}{2}} \tilde{I}_{in}(t) \cdot dt} \tag{19}$$

$$\boldsymbol{i}_{\text{in}} = \frac{\mathbf{1}}{\mathbf{2}}[\boldsymbol{i_1} + \boldsymbol{i_3}] \cdot \boldsymbol{d} - \frac{\mathbf{1}}{\mathbf{2}} \cdot (\boldsymbol{i_2} + \boldsymbol{i_3}) \cdot \boldsymbol{d_l} \tag{20}$$

The average rectified voltage as a function of the duty ratio, d, input voltage, V_{in}, output voltage, V_o, and output inductor current, I_o, has been obtained by substituting Equation (18) into Equation (15). The output inductor voltage's small signal is obtained following linearization and perturbation [36] .

$$\hat{v}_L = \hat{v}_{rec} - \hat{v}_o \tag{21}$$

$$\hat{v}_L = K_{vld} \cdot \hat{d} + K_{vlvi} \cdot \hat{v}_{dc} + K_{vlvo} \cdot \hat{v}_o + K_{vlil} \cdot \hat{l}_L \tag{22}$$

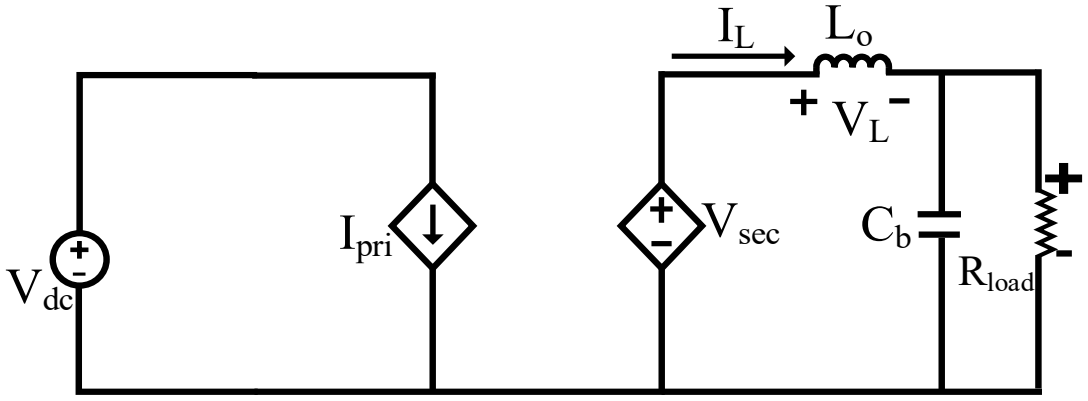

Fig. 5.1 Averaged model of the PSFB converter with R Load

From the circuit, we can say that,

$$\hat{\boldsymbol{l}}_{\boldsymbol{o}} = \frac{\hat{\boldsymbol{v}}_{\boldsymbol{L}}}{\boldsymbol{Z_L(s)}} \tag{23}$$

Replacing Equation (23) into Equation (22), the output inductor current as function of $\hat{d}$, $\widehat{V_{in}}$ and $\widehat{V_o}$ obtained

$$\hat{l}_L = \frac{K_{\text{vld}}}{Z_L(s) - K_{\text{vlil}}} \cdot \hat{d} + \frac{K_{\text{vlvi}}}{Z_L(s) - K_{\text{vlil}}} \cdot \hat{v}_{\text{in}} + \frac{K_{\text{vlvo}}}{Z_L(s) - K_{\text{vlil}}} \cdot \hat{v}_o$$

Therefore, the characteristic coefficients of the output port are finally obtained:

$$A_o(s) = \frac{K_{vld}}{Z_L(s) - K_{vlil}}$$

$$B_o(s) = -\frac{K_{\text{vlvo}}}{Z_L(s) - K_{\text{vlil}}}$$

$$C_o(s) = \frac{K_{\text{vlvi}}}{Z_L(s) - K_{\text{vlil}}}$$

By plugging Equations (2)–(4) and (10) into Equation (12), we can find the average input current as a function of the duty ratio, d, the input voltage, V_{dc}, the output voltage, V_{out}, and the output inductor current, i_o. We get the characteristic coefficients of the input port after linearizing and perturbing.

$$A_i(s) = K_{iid} + K_{iidl} \cdot K_{dld} + K_{iidl} \cdot K_{dlil} \cdot A_o(s)$$
$$B_i(s) = -[K_{\text{iivo}} + K_{\text{iidl}} \cdot K_{\text{dlvo}} - K_{\text{iidl}} \cdot K_{\text{dlil}} \cdot B_o(s)]$$
$$C_i(s) = K_{iivi} + K_{iidl} \cdot K_{dlvi} + K_{iidl} \cdot K_{dlil} \cdot C_o(s)$$

Note: The constant coefficients of all the Equation are given in **Appendix A**

Chapter 6

Simulation Study and Conclusion

The suggested battery charger, which incorporates a Totem-Pole Power Factor Correction (PFC) circuit and a Phase-Shift Full Bridge (PSFB) converter, was designed, simulated, and experimented to test its efficiency, power factor, and performance. The results show that the system corrects the power factor effectively, reduces switching losses, and achieves stable charging of the battery with high efficiency.

6.1. Stage 1: Totem Pole Power Factor Correction

The first stage of the charger is responsible for power factor correction and ensuring that input current is in phase with input volage. A totem-Pole PFC topology was implemented in simulation, achieve high efficiency and reduced switching losses.
In Figure 8. The input voltage and input current waveform are shown here, where it can be observed that the current waveform closely follows the voltage waveform.

The simulation results demonstrate that the Power Factor achieved is 0.99, indicating near-unity power factor operation. The Totem-Pole PFC stage is designed to provide a stable output of 400V DC with minimal ripple, which then serves as the input for the Phase-Shift Full Bridge (PSFB) converter in the next stage. The output voltage is maintained at 400V DC throughout the process, showing the PFC stage's ability to handle varying load conditions efficiently and confirming the effectiveness of the output capacitor and control strategy.

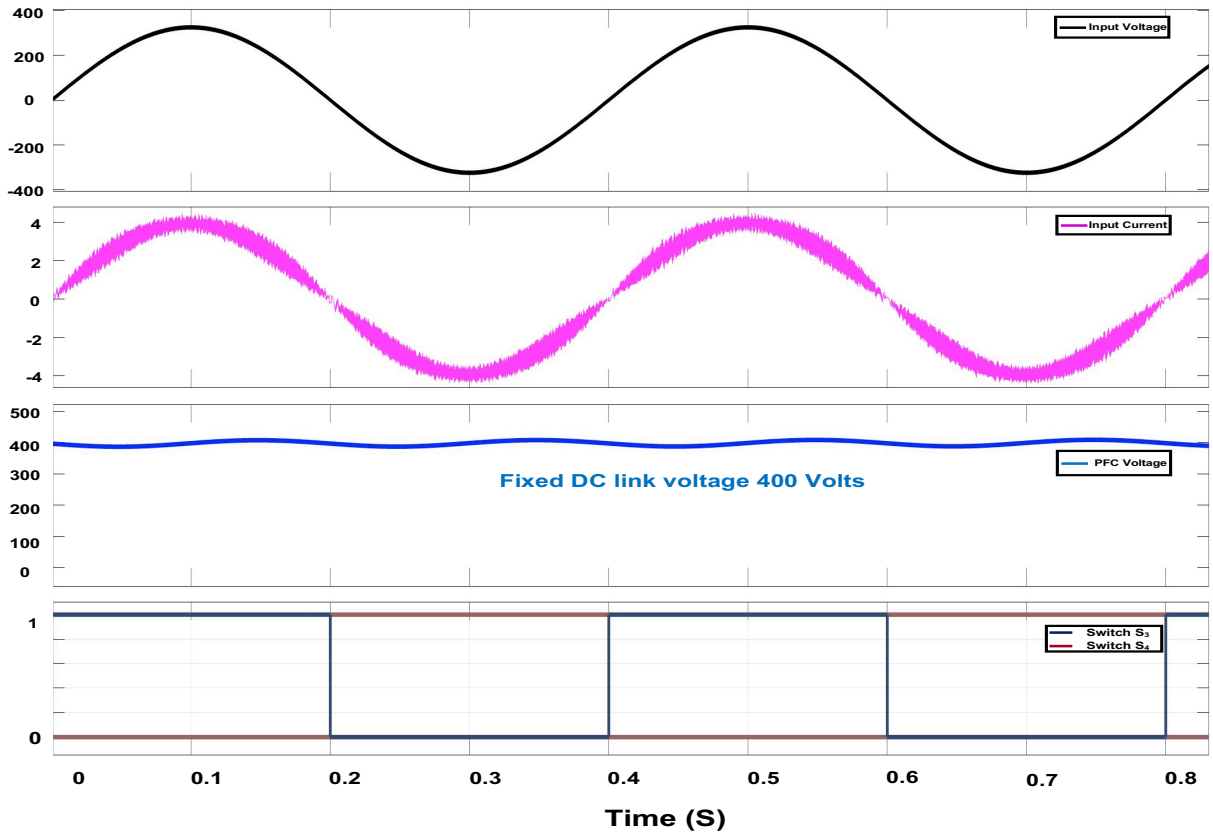

Fig. 6.1. Input Voltage, Input Current, DC Link Output Voltage, Switching Cycle of Totem-Pole PFC

6.2. Stage 2: Phase Shift Full Bridge (PSFB) Converter

The primary side of the Phase-Shift Full Bridge converter receives output from Totem-Pole PFC stage. Using the Phase-Shift control method, the DC voltage is transformed into an AC wave at this stage; the AC waveform is then faded to the transformer's primary winding. Shown in Figure 9. Because L_m switches its current polarity using the applied V_{PFC}, Secondary Voltage (*Vsec*), pulse width is less than Vpri since it causes no voltage on the transformer winding, hence causing a reduced Vsec pulse width, a phenomenon known as duty-cycle loss. The larger the L_m inductance, the larger the duty-cycle loss (the difference in pulse lengths between *Vpri* and *Vsec*). Smaller L_m inductance will help to enable a larger Diode efficiency on the secondary side of a transformer for a broader duty-cycle variation range.

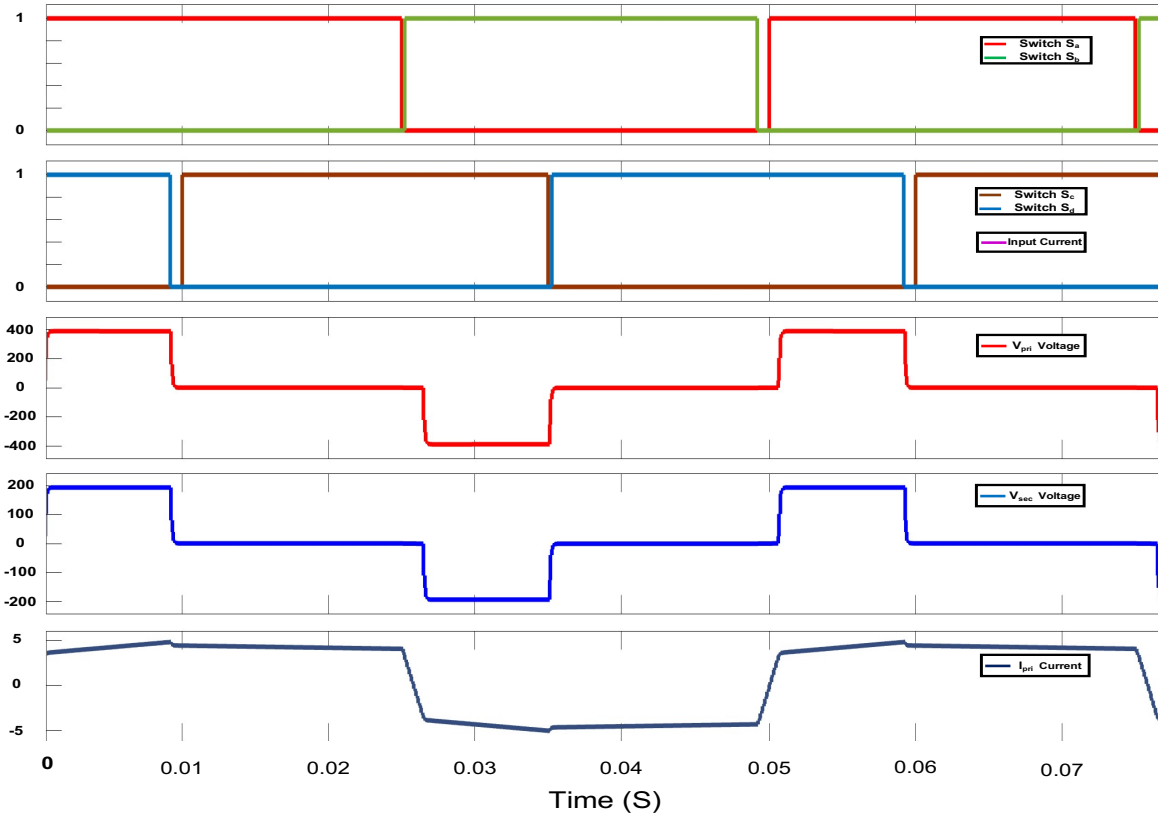

Fig. 6.2. Switching Cycle, Primary and Secondary Voltage, and Primary Current of Transformer.

Soft switching at the primary-side MOSFETs is achieved by energy stored in L_m during switching transients. Especially at mild loads, a short L_m inductance means less energy will be stored in the inductor, which can be inadequate to discharge the output capacitor voltage of MOSFET Switches for achieving the soft switching capability of a converter.

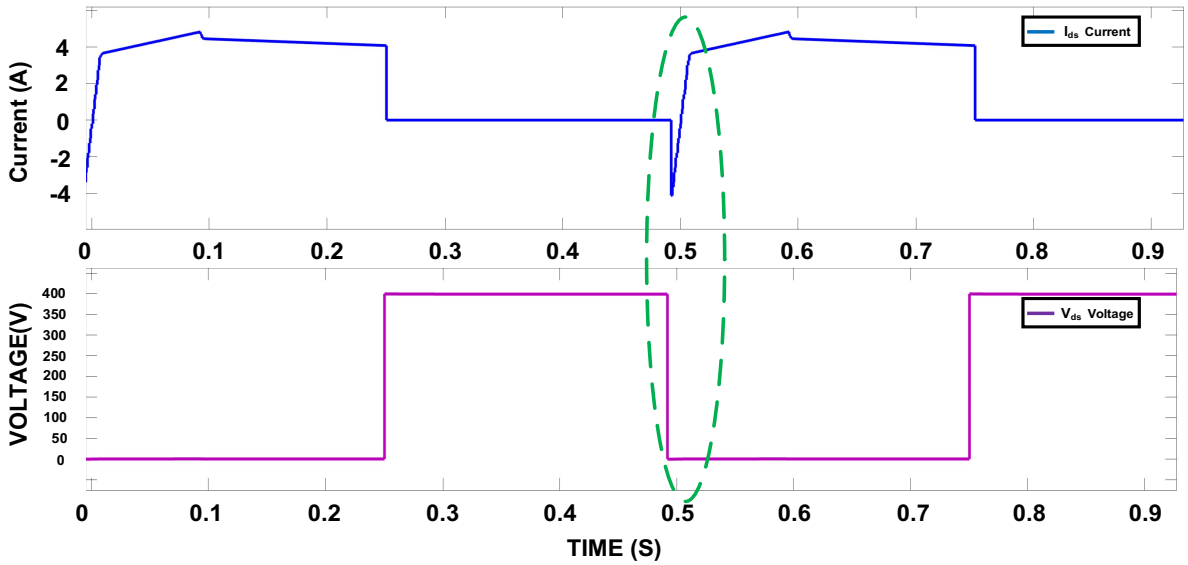

Fig. 6.3. PSFB MOSFET Current and Voltage with ZVS.

The final stage of the battery charger is converting the rectified AC output from the transformer into a pure DC voltage suitable for charging the Battery. This was achieved using a rectifier and an LC Filter, which filters out the current voltage ripples and ensures a stable DC Output

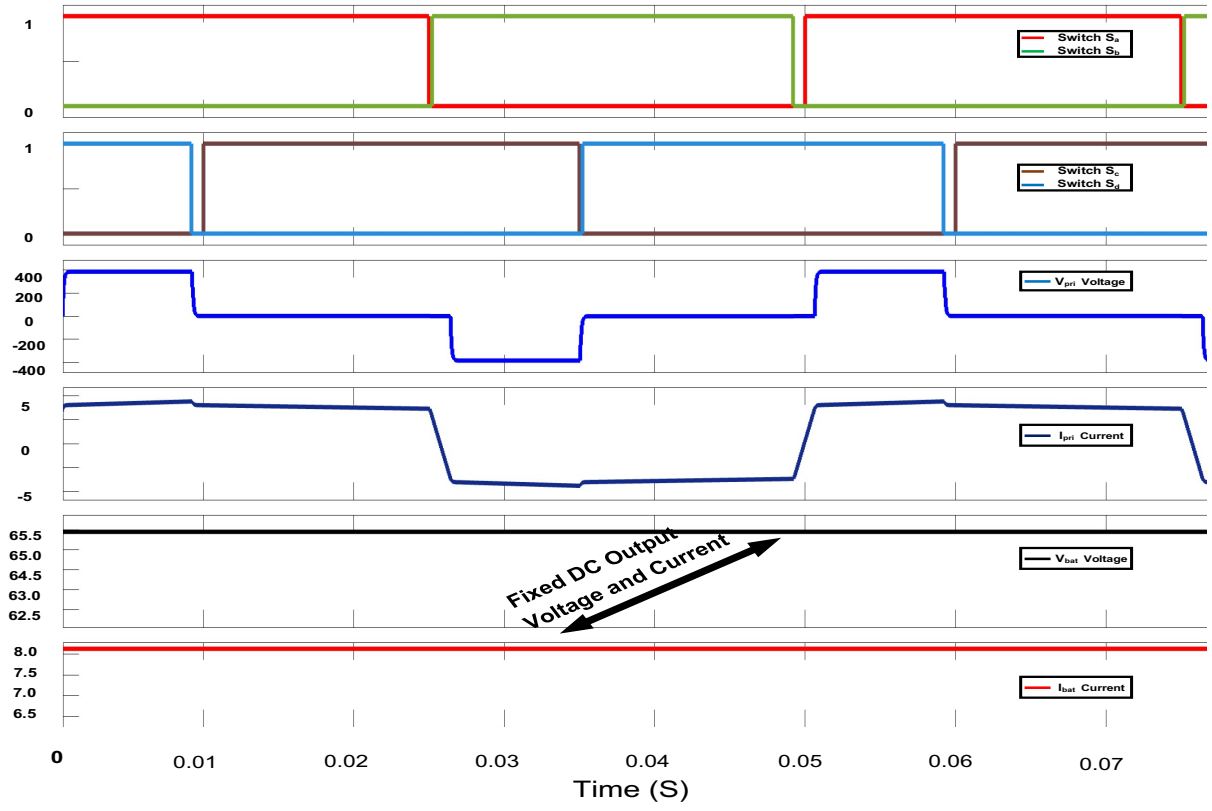

Fig. 6.4. Switching Cycle, Primary Voltage, and Current of Transformer, Output Voltage and Current for Battery Charging

The charging voltage and current are within the required limits, ensuring safe and efficient battery charging without excessive stress on the battery cells.

6.3. Conclusion

This study shows how to design, build, and use a high-efficiency battery charging system that uses advanced power electronics topologies, such as a Totem-Pole Power Factor Correction (PFC) circuit and a Phase-Shift Full Bridge (PSFB) DC-DC converter. The proposed charger design is meant to meet the growing needs of electric vehicle (EV) infrastructure by providing high power quality, system reliability, and operational efficiency.

The charger has three separate parts:

The first stage is the Totem-Pole PFC Stage. In this stage, a single-phase AC supply is sent into a Totem-Pole PFC, which fixes the power factor to almost one (~0.99). This stage changes the input AC to a controlled 400 V DC output while keeping an amazing efficiency of 99%. This means that very little power is lost, and energy is used more effectively.

Phase-Shift Full Bridge (PSFB) DC-DC Converter: The second stage uses a PSFB converter to change the regulated DC voltage into a high-frequency AC square wave. This makes it possible for a high-frequency transformer to transfer energy more efficiently. This stage separates the grid and the battery electrically, which makes things safer and lets you change the voltage level by changing the number of turns on the transformer. The voltage is lowered to meet the needs of charging the battery. The PSFB uses soft-switching methods like Zero Voltage Switching (ZVS) to cut down on switching losses by a lot, which makes the overall converter efficiency about 95%.

In the last step, the AC signal is rectified and sent through an LC filter to make sure the DC output is smooth and free of ripples. This steady output voltage and current are very important for charging batteries safely, reliably, and efficiently. They help the batteries last longer and work better over time.

The proposed charger will do the following important things:

High Power Factor (about ~0.99):

The Totem-Pole PFC stage made this possible by keeping reactive power to a minimum and following international grid standards.

High Overall Efficiency (~95%): The Totem-Pole PFC and PSFB topology work together to make the system very efficient at converting energy, which cuts down on energy losses and thermal stress.

Table 6.1. Other measurement results (Power, PF, Cos ϕ, and efficiency) for battery-charging mode.

Parameter	1	2	3	4	5	6	7	8	9	10
Power [kW]	0.24	0.456	0.665	0.876	1.086	1.294	1.502	1.712	1.912	1.959
PF [-]	0.87	0.96	1	1	1	1	1	1	1	1
Cos ϕ [-]	0.96	0.99	1	1	1	1	1	1	1	1
Efficiency [%]	90.02	94.8	95.66	96.9	96.37	96.37	96.37	96.5	96.7	96.7

Good Electrical Isolation: The PSFB stage uses a high-frequency transformer to keep the input and output separate, which keeps both the charger and the battery system safe.

Stable and Pure DC Output: The output filtering stage reduces voltage and current ripple, which makes charging safer and more reliable and helps the battery last longer.

6.4. Future Scope

While the proposed charger topology demonstrates high efficiency and power quality, there remains considerable potential for further research and development. Future work can focus on the following areas to enhance system performance, reliability, and applicability:

The proposed charger topology shows high efficiency and power quality, but there is still a lot of room for more research and development. To make the system work better, be more reliable, and be more useful, future work can focus on the following areas:

1. **Exploration of Advanced Control Strategies:** Implementing more sophisticated control algorithms such as Model Predictive Control (MPC), Artificial Neural Networks (ANN), or Fuzzy Logic Controllers can significantly improve dynamic response, load regulation, and stability under varying load and grid conditions. These methods can also improve power factor correction and lower total harmonic distortion (THD), which lets the system meet stricter grid standards.

2. Better thermal management: Using advanced thermal modeling and smart thermal management systems that monitor temperature in real time and use active cooling methods can help heat spread out better. This can make the system more reliable, the charger last longer, and keep working at a high level of efficiency even when it's running at high power all the time.

3. Digital Implementation and Real-Time Monitoring: By combining digital signal processors (DSPs) or microcontrollers with high-speed computation capabilities, it is possible to monitor, find faults, and adaptively control in real time. IoT-based monitoring can also make it possible to do diagnostics, predictive maintenance, and system updates over the air from a distance. This is especially useful for EV charging stations.

4. Scalability and Modularization: Making the charger system modular and scalable can help it work with a lot of different types of vehicles, from two-wheelers to heavy electric vehicles. Modular architecture also makes it easier to keep up with and make improvements in the future.

5. Better EMI Filtering and Compliance: Future designs can focus on making electromagnetic interference (EMI) filtering methods better so that they meet international EMC standards, especially at the high switching frequencies that are common in totem-pole PFC and PSFB topologies.

6.Small and Light Design: The charger's physical size and weight can be greatly reduced without affecting performance by using advanced materials like wide bandgap semiconductors (SiC or GaN). This would be very helpful for applications that use onboard chargers.

In conclusion, the proposed topology is a great starting point for making a battery chargers that work well. The identified future directions show how to make the system smarter, more efficient, and better able to meet the needs of electric mobility as they arise.

Reference

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Appendix A

The complete set of equations for the small-signal formulation of the PSFB converter is provided below:

$$K_{vlvo} = -\frac{L_m^2 \cdot V_{dc} \cdot (D \cdot L_o \cdot n^2 + L_o)}{T_{sw} \cdot (L_m \cdot n^2 + L_o)} \cdot \frac{K_2}{K_1^2}$$

$$K_1 = {L_o}^2 \cdot V_{dc} - L_m^2 \cdot V_o \cdot n^3 - L \cdot L_m \cdot V_{dc} \cdot n^2 \cdot (1 - D)$$

$$K_2 = T_{sw} \cdot V_{dc} \cdot (D^2 \cdot L_m^2 \cdot n^4 + L_o^2 - L_o \cdot L_m \cdot n^2) + K_4$$

$$K_3 = T_{sw} \cdot V_{dc} \cdot D \cdot (L_o \cdot L_m \cdot n^2 - 2 \cdot L_m^2 \cdot n^4)$$

$$K_4 = K_3 + 4 \cdot I_L \cdot (L \cdot L_m^2 \cdot n^3 + L_m^3 \cdot n^5)$$

$$K_{vlil} = -\frac{4 \cdot L_o \cdot L_m \cdot n^2 \cdot (L \cdot V_{dc} + L_m \cdot V_o \cdot n)}{T_{sw} \cdot K_1}$$

$$K_{vlvi} = \frac{L_o \cdot n \cdot (K_5 + K_7 + K_{10} - K_{12})}{T_{sw} \cdot (L_m \cdot n^2 + L_o) \cdot K_1^2}$$

$$K_5 = T_{sw} \cdot D^2 \cdot [V_{dc}^2 \cdot K_6 + L_{lk}^4 \cdot V_o^2 \cdot n^6]$$

$$K_6 = L_o^3 \cdot L_m \cdot n^2 + L_o^2 \cdot L_m^2 \cdot n^4$$

$$K_7 = T_{sw} \cdot [L_o^2 \cdot L_m^2 \cdot V_o^2 \cdot n^2 + K_8]$$

$$K_8 = D \cdot (K_9 + V_o^2 \cdot (L_o \cdot L_m^3 \cdot n^4 - L_m^4 \cdot n^6))$$

$$K_9 = V_{dc}^2 \cdot (L_o^4 - L_o^2 \cdot L_m^2 \cdot n^4)$$

$$K_{12} = 2 \cdot T_{sw} \cdot D \cdot V_o \cdot V_{in} \cdot (L_o^2 \cdot L_m^2 \cdot n^3 + L_o \cdot L_m^3 \cdot n^5)$$

$$K_{vld} = \frac{L_o \cdot V_{dc} \cdot n \cdot (K_{13} + K_{15} + K_{17} + K_{19})}{T_{sw} \cdot (L_m \cdot n^2 + L) \cdot K_1^2}$$

$$K_{13} = 2 \cdot T_{sw} \cdot D \cdot V_o \cdot V_{dc} \cdot K_{14} + T_{sw} \cdot L_o^4 \cdot V_{dc}^2$$

$$K_{14} = L_o \cdot L_m^3 \cdot n^5 - L_o^2 \cdot L_m^2 \cdot n^3$$

$$K_{15} = 4 \cdot I_L \cdot [K_{16} + V_o \cdot (L_m^2 \cdot L_m^3 \cdot n^4 + L_o \cdot L_m^4 \cdot n^6)]$$

$$K_{16} = V_{dc} \cdot (L_o^3 \cdot L_m^2 \cdot n^3 + L_o^2 \cdot L_m^3 \cdot n^5)$$

$$K_{17} = T_{sw} \cdot V_o \cdot V_{dc} \cdot K_{18} - T_{sw} \cdot L_o^2 \cdot L_m^2 \cdot V_{in}^2 \cdot n^4$$

$$K_{18} = L_o^2 \cdot L_m^2 \cdot n^3 - L_m^3 \cdot n^5 \cdot L \cdot (D^2 + 2)$$

$$K_{19} = T_{sw} \cdot V_o^2 \cdot \left(L \cdot L_m^3 \cdot n^4 - n^6 \cdot (L_m^4 - 2 \cdot D \cdot L_m^4)\right)$$

$$K_{iivi} = K_{20} \cdot (L_o \cdot D_l + D \cdot L_m \cdot n^2 - L_m \cdot n^2 \cdot D_l)$$

$$K_{20} = \frac{T_{sw} \cdot (D - D_l)}{4 \cdot L_o^2 \cdot n^2 + 4 \cdot L_o \cdot L_m}$$

$$K_{iivo} = \frac{L_m \cdot T_{sw} \cdot n^3 \cdot D_l^2 - D \cdot L_m \cdot T_{sw} \cdot n^3 \cdot D_l}{4 \cdot L_o \cdot L_m \cdot n^2} + K_{21}$$

$$K_{21} = \frac{K_{22} - 2 \cdot T_{sw} \cdot n \cdot D_l^2 + T_{sw} \cdot n \cdot D_l}{4 \cdot L_m \cdot n^2 + 4 \cdot L_o}$$

$$K_{22} = 2 \cdot T_{sw} \cdot n \cdot D \cdot D_l - T_{sw} \cdot n \cdot D^2$$

$$K_{dlil} = \frac{4 \cdot L \cdot L_m \cdot n \cdot (L_m \cdot n^2 + L)}{T_{sw} \cdot K_1}$$

$$K_{iid} = \frac{T_{sw} \cdot \left(K_{23} + 2 \cdot D \cdot L_o \cdot L_m \cdot (V_{dc} \cdot n^2 - V_o \cdot n)\right)}{4 \cdot L_o \cdot L_m \cdot (L_m \cdot n^2 + L)}$$

$$K_{23} = V_{dc} \cdot D_l \cdot (L_o^2 - 2 \cdot L_o \cdot L_m \cdot n^2) + K_{24}$$

$$K_{24} = V_o \cdot D_l \cdot (L_o \cdot L_m \cdot n - L_m^2 \cdot n^3)$$

$$K_{iidl} = \frac{T_{sw} \cdot (K_{25} + K_{27} + L \cdot L_m \cdot V_o \cdot n)}{4 \cdot L_o \cdot L_m \cdot (L_m \cdot n^2 + L)}$$

$$K_{25} = K_{26} + 2 \cdot V_o \cdot D_l \cdot (L_m^2 \cdot n^3 - L_o \cdot L_m \cdot n)$$

$$K_{26} = 2 \cdot V_{dc} \cdot D_l \cdot (L_o \cdot L_m \cdot n^2 - L_o^2)$$

$$K_{27} = D \cdot (L_o^2 \cdot V_{in} - K_{28} + L_o \cdot L_m \cdot V_o \cdot n)$$

$$K_{28} = L_m^2 \cdot V_o \cdot n^3 + 2 \cdot L_o \cdot L_m \cdot V_{dc} \cdot n^2$$

$$K_{dld} = 1 - \frac{K_{29} + K_{31}}{T_{sw} \cdot K_1^2}$$

$$K_{29} = 4 \cdot I_L \cdot V_{dc} \cdot \left(L_o^3 \cdot L_m^2 \cdot n^3 + L_0^2 \cdot L_m^3 \cdot n^5\right) + K_{30}$$

$$K_{30} = T_{sw} \cdot L_m^4 \cdot V_o^2 \cdot n^6$$

$$K_{31} = T_{sw} \cdot L_o^4 \cdot V_{dc}^2 - T_{sw} \cdot L_o^2 \cdot L_m^2 \cdot K_{32}$$

$$K_{32} = V_o \cdot V_{dc} \cdot n^3 + V_{in}^2 \cdot n^4$$

$$K_{dlvo} = \frac{L_o \cdot L_m \cdot n \cdot (K_{33} + K_{35})}{T_{sw} \cdot K_1^2}$$

$$K_{33} = T_{sw} \cdot V_{dc} \cdot D \cdot K_{34} + T_{sw} \cdot V_{in} \cdot L_o^2$$

$$K_{34} = L_o \cdot L_m \cdot n^2 + D \cdot L_m^2 \cdot n^4 - 2 \cdot L_m^2 \cdot n^4$$

$$K_{35} = 4 \cdot I_L \cdot K_{36} - T_{sw} \cdot V_{dc} \cdot L_o \cdot L_m \cdot n^2$$

$$K_{36} = L_o \cdot L_m^2 \cdot n^3 + L_m^3 \cdot n^5$$

$$K_{dlvi} = -\frac{L_o \cdot L_m \cdot n \cdot (K_{37} + K_{39})}{T_{sw} \cdot K_1^2}$$

$$K_{37} = 4 \cdot I_L \cdot D$$

$$K_{38} = L_o^2 \cdot L_m \cdot n^2 + L_o^2 \cdot L_m^2 \cdot n^4$$

$$K_{39} = T_{sw} \cdot V_o \cdot D \cdot K_{40} + T_{sw} \cdot V_o \cdot (L_o^2 - L_o^2 \cdot L_m \cdot n^2)$$

$$K_{40} = L_o \cdot L_m \cdot n^2 - 2 \cdot L_m^2 \cdot n^4 + D \cdot L_m^2 \cdot n^4$$