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CHAPTER 1

INTRODUCTION

1.1 Motivation and Background

In the rapidly evolving field of digital electronics, low power consumption, compact circuit design, and high performance have become essential requirements, especially with the growing proliferation of portable and batteryoperated devices. As technology scales down, the demand for energy-efficient circuits becomes critical to ensure reliability and prolonged battery life in embedded systems, Internet of Things (IoT) devices, and edge computing applications.

One persistent challenge in digital systems is the switch-bouncing phenomenon. Mechanical switches, though simple in construction, exhibit contact bounce when toggled, generating a series of spurious transitions before settling to a stable logic level. These unwanted transitions can cause erroneous signals in digital circuits, leading to faulty data processing, incorrect triggering of logic functions, and degraded system reliability. Traditionally, switch debouncing has been addressed using various hardware and software techniques, but these solutions often come with trade-offs in terms of circuit complexity, power consumption, and timing reliability.

An efficient approach to mitigate switch bounce is to use a Schmitt Trigger, a fundamental circuit that introduces hysteresis—a property that ensures a distinct threshold for signal rising and falling edges. By creating this hysteresis, a Schmitt Trigger effectively suppresses noise and small fluctuations at the input, thus providing a clean, stable digital output. It is an ideal solution for switch debouncing applications, where the input signal is inherently prone to noise and multiple transitions.

However, implementing Schmitt Triggers using traditional CMOS logic can lead to increased power consumption, area overhead, and complex design requirements, [1] especially when aiming for low-power, high-density systems. Therefore, it becomes crucial to explore alternative logic design techniques that can offer lower power dissipation, smaller area footprint, and reduced propagation delays, without compromising the core functionality of the Schmitt Trigger.

1.2 Research Focus: GDI-Based Schmitt Trigger Design

This research proposes a novel approach for designing a Schmitt Trigger-based switch debounce circuit by leveraging the Gate Diffusion Input (GDI) technique. GDI is a well-established method for implementing digital logic gates with a minimal number of transistors, resulting in lower power consumption, reduced propagation delays, and smaller silicon area compared to conventional CMOS designs.

In this work, the Schmitt Trigger is constructed using NAND gates, which are in turn implemented using the GDI technique [6]. This combination provides a power-efficient, compact, and reliable solution for hardware debouncing applications. By replacing conventional CMOS NAND gates with GDI-based NAND gates, the Schmitt Trigger circuit inherits the advantages of reduced power dissipation and optimized performance, making it suitable for integration into modern digital systems where energy efficiency is paramount.

The proposed GDI-based Schmitt Trigger effectively eliminates unwanted glitches and noise from the switch input, stabilizing the output signal without the need for external clocking mechanisms or complex sequential logic. This makes the design not only simpler but also asynchronous, allowing for seamless integration into a wide range of digital systems, including low-power embedded devices, user-interface circuits, and control systems.

1.3 Objectives and Contributions

The primary objective of this thesis is to design, simulate, and evaluate a low-power Schmitt Trigger circuit using GDI-based NAND gates for switch debouncing applications. The key goals of this research include:

- Designing a Schmitt Trigger circuit that effectively mitigates the effects of switch bouncing by introducing hysteresis characteristics.
- Implementing GDI-based NAND gates to optimize the power and area performance of the Schmitt Trigger circuit.
- Simulating the proposed design using industry-standard tools (such as LTspice) to evaluate its behaviour in terms of power consumption, propagation delay, and stability.
- Demonstrating the application of the GDI-based Schmitt Trigger in a switch debounce circuit, validating its effectiveness through simulation results and waveform analysis.

- Comparing the performance of the GDI-based Schmitt Trigger solution against conventional logic implementations, highlighting its advantages in power and performance metrics.

CHAPTER 2
LITERATURE REVIEW

2.1 Fundamentals of Switch Debouncing Phenomenon

2.1.1 Switch Bouncing Phenomenon

It has been observed how a push button or switch operates: it just presses to change its state. Switches are used in electronics for a variety of purposes. Mostly, they are used to drive or represent distinct voltage levels, which makes the system binary, that is, it can be either ON or OFF or have high or low voltage levels. In order to express the binary logic of 0s (zeroes) and 1s (ones), these voltage levels, for example, 5 Volts = High = ON = closed circuit and 0 Volts = Low = OFF = open circuit, are useful.

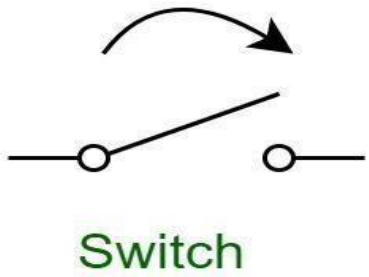

Fig. 2.1 - Basic Switch

Fig4: Basic Switch However, a lot goes on behind the straightforward push buttons on our keyboards and other gadgets [3]. In essence, a basic button consists of two metal contacts that come into contact when the user presses the button. The underlying circuit is then completed by these metal contacts, which also

alert the sensing element—typically a microcontroller—that the button has been pressed.

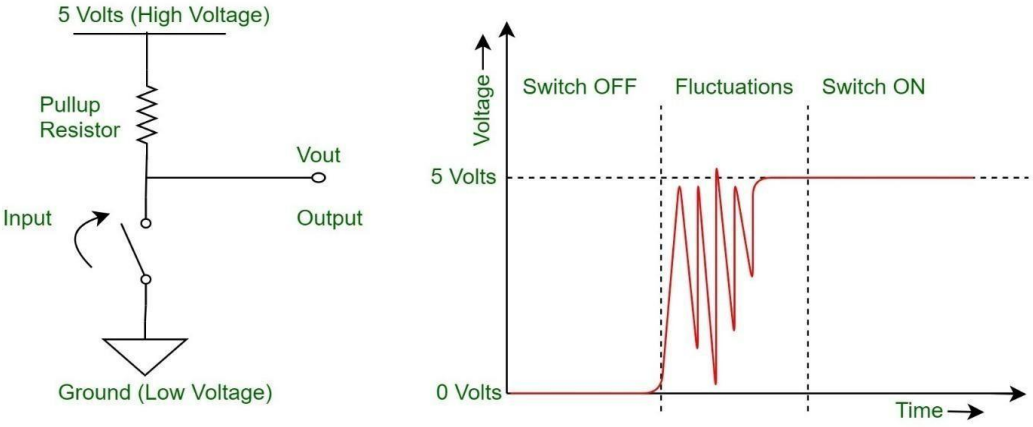

Fig. 2.2- Switch Bounce Graph

2.1.2 Traditional Debounce Methods (SR Flip-Flop, RC filters, D Flip-Flop)

In this category, there are various implementations of circuits which can be used for eliminating the effect of switch debouncing right at the hardware level. The different types of circuits used are:

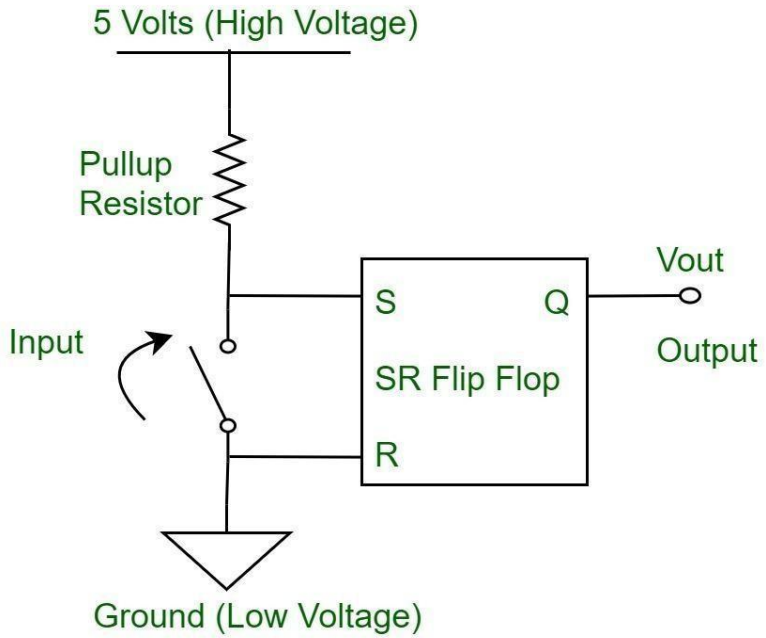

Fig. 2 .3- Switch Debounce using SR Flip Flop

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It has been observed that the usage of D flip flop consumes less power than SR Flip Flop. So, considering the same case in the switch debounce circuit the SR Flip Flop is replaced by D Flip Flop as shown in the figure Fig2.4

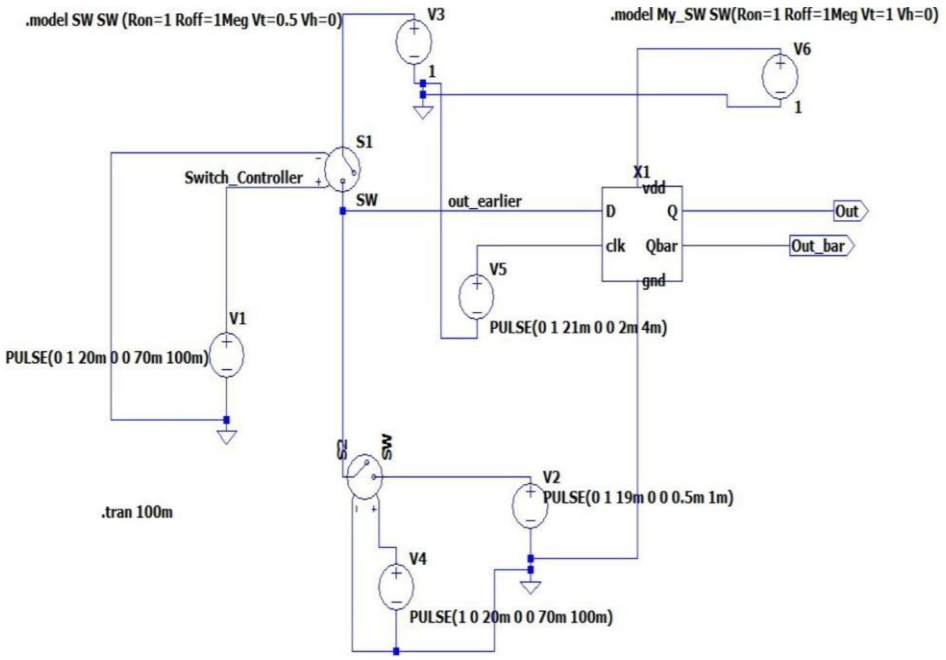

Fig. 2 .4- D flip flop for switch debounce

The D flip flop used a power consumption technique that is GDI (Gate Diffusion Input) and both NAND gates using CMOS and GDI have been compared. It has been observed that the power consumption in CMOS-based NAND D flip flop is 9uW, and power consumption in GDI-based NAND D flip flop is 4.8uW. So there is almost 100% decrement in power consumption in case of GDI NAND D flip flop than CMOS NAND D flip flop.

2.2 Schmitt Trigger: Theory and Applications

2.2.1 Working Principle

A Schmitt Trigger is a fundamental circuit element used in digital and analog systems to convert a noisy or analog input signal into a clean, stable digital output. It is a comparator with positive feedback that introduces hysteresis, enabling it to reject noise and small fluctuations in the input signal [4].

Unlike a standard comparator or logic gate that changes state at a single threshold voltage, the Schmitt Trigger has two distinct threshold voltages:

The upper threshold voltage (VUT), at which the output transitions from low to high as the input rises.

The lower threshold voltage (VLT), at which the output transitions from high to low as the input falls.

This dual-threshold behaviour introduces a dead zone between VLT and VUT, where small variations in the input do not affect the output [2]. As a result, the Schmitt Trigger effectively cleans up signals with slow edges or noise, providing a sharp, noise-free digital output transition.

In practical terms, when the input signal exceeds VUT, the output is set to a logic high level. When the input drops below VLT, the output resets to logic low. For input values between these two thresholds, the output retains its previous state, creating a memory-like effect that enhances noise immunity.

This behavior makes Schmitt Triggers ideal for applications such as:

Signal conditioning: Cleaning up noisy sensor inputs.

Debouncing mechanical switches: Eliminating spurious transitions caused by switch bouncing.

Oscillator circuits: Generating square waves from slow or analog input signals.

Wave shaping circuits: Converting analog or slowly varying signals into sharp digital edges.

2.2.2 Hysteresis Characteristics

The defining feature of a Schmitt Trigger is its **hysteresis curve**—a graphical representation of its input-output relationship [9]. This hysteresis behaviour is characterized by the two distinct threshold voltages (VUT and VLT) and the resulting **hysteresis width (ΔV)**, defined as:

$$\Delta V = V_{UT} - V_{LT}$$

The presence of hysteresis ensures that the Schmitt Trigger output does not rapidly toggle in response to minor, rapid fluctuations near the switching threshold. Instead, the circuit remains in its current state until the input crosses the respective threshold.

The typical **transfer characteristic** of a Schmitt Trigger shows:

- A sharp transition from low to high output when the input crosses V_{UT}.

• A corresponding sharp transition from high to low output when the input falls below V_{LT}.

This behaviour provides:

- **Noise immunity**: Preventing false triggering due to small voltage spikes.
- **Stable switching**: Ensuring the output changes state only for significant input changes.
- **Signal regeneration**: Producing clean digital transitions from slowly changing or noisy inputs.

The hysteresis property is especially critical in debouncing applications, where mechanical switches introduce rapid, unintended transitions that need to be suppressed.

2.2.3 Advantages in Digital Systems

The Schmitt Trigger offers several key advantages that make it an essential building block in digital systems:

- **Noise Rejection**: By introducing hysteresis, the Schmitt Trigger

ensures that small, rapid fluctuations in the input signal (such as those from noisy sensors or mechanical switch bounce) do not cause unwanted changes in the output. This makes it highly reliable in real-world conditions where signal integrity is often compromised.

- **Improved Signal Integrity**: Schmitt Triggers produce sharp, clean digital transitions from inputs with slow edges or gradual transitions. This is particularly useful in circuits where precise timing and well-defined logic levels are critical.
- **Asynchronous Operation**: Unlike flip-flop-based debounce circuits, the Schmitt Trigger does not rely on a clock signal. This makes it ideal for systems where simplicity, low latency, and asynchronous behavior are desired.
- **Low Component Count**: Schmitt Triggers can be implemented

using simple gate configurations (such as NAND or NOR gates with feedback), making them compact and resource-efficient.

• **Versatility**: Schmitt Triggers are widely used in a variety of digital applications, including:

- Switch debouncing.
- Waveform shaping.
- Square wave generation (oscillators).
- Pulse width modulation.
- Threshold detection in analog-to-digital conversions.

By combining the **GDI technique** with the Schmitt Trigger design, this thesis aims to further enhance the power and area efficiency of such circuits, enabling their integration into **low-power embedded systems**, **IoT devices**, and **portable electronics** where energy efficiency is paramount.

2.3 Logic Design using GDI

With the growing demand for faster, more compact, and energy-efficient digital applications—especially in portable devices—researchers have been exploring new solutions to overcome the limitations of traditional CMOS technology. Over the years, various logic design techniques have emerged, each aiming to boost circuit performance.

However, most Pass Transistor Logic (PTL) designs face two key challenges [5]. The first is the **threshold voltage drop** across single-channel pass transistors, which leads to lower current drive and slower operation.

Several PTL-based approaches have been proposed to tackle these issues:

1. **Transmission Gate CMOS (TG)**: TG logic uses both nMOS and pMOS transistors in parallel to achieve full logic-level swings, making it possible to implement complex logic functions with fewer transistors.
2. **Complementary Pass-Transistor Logic (CPL)**: CPL uses

nMOS pass transistors for logic functions, complemented by CMOS inverters at the outputs. It offers the benefits of lower power consumption and a small 17 stack height, but suffers from static power loss due to the low voltage swings at the inverter gates. To address this, variants like LCPL (with pMOS restoration transistors) and SRPL (with cross-coupled inverters) have been introduced to improve the swing and reduce power loss.

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3. **Double Pass-Transistor Logic (DPL)**: DPL combines both nMOS and pMOS transistors in its design, enabling full-swing operation without needing extra restoration circuitry. It also helps reduce DC power consumption.

These approaches reflect the continuous effort in logic design to balance speed, area, and power efficiency in modern digital systems.

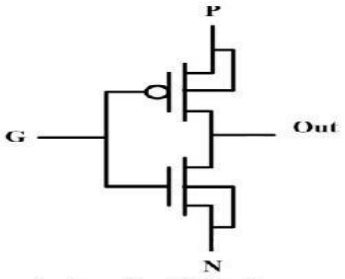


Fig 1: Basic GDI Structure

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	NOT
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

Fig. 2.5: GDI basic cell and its Truth Table

This technique has been used to create NAND gate like:-

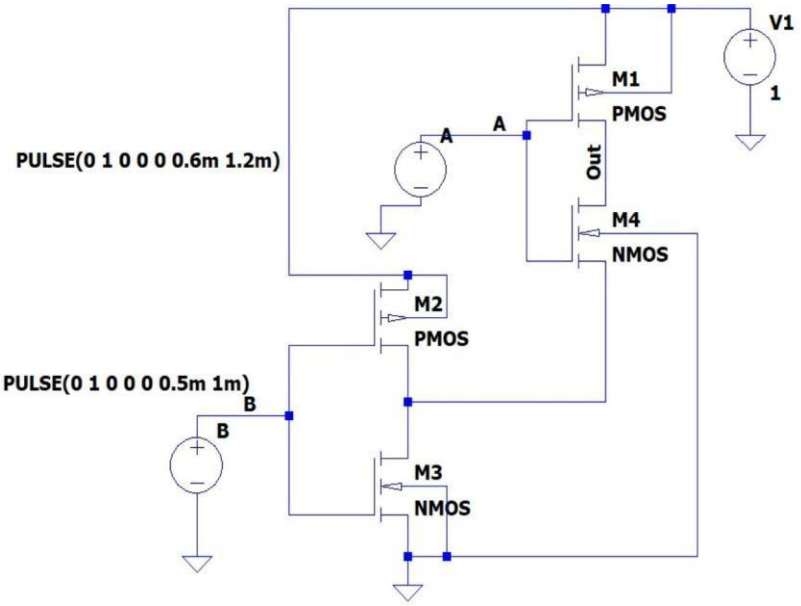


Fig. 2.6: NAND gate using GDI in LTspice

2.4 Comparison between GDI, CMOS, TG and N-PG

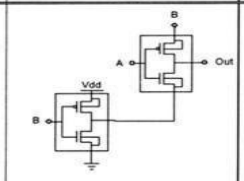
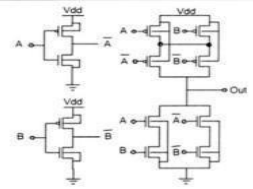
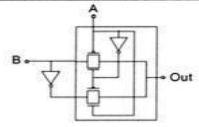
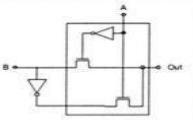
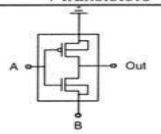
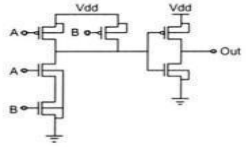
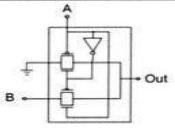
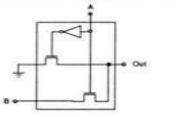
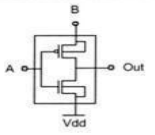
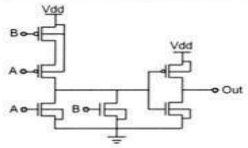
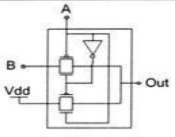
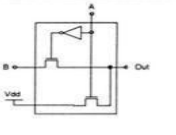
	GDI	CMOS	TG	N-PG
XOR				
	4 transistors	12 transistors	8 transistors	6 transistors
AND				
	2 transistors	6 transistors	6 transistors	4 transistors
OR				
	2 transistors	6 transistors	6 transistors	4 transistors

TABLE 2.1: LOGIC GATE COMPARISONS (GDI, CMOS, TRANSMISSION GATE, AND nMOS PASS GATE) USING THE CIRCUIT TOPOLOGIES

Gate type in series	Logic expression	GDI			CMOS			TG			N-PG		
		Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.
MUX	$\overline{A}B + AC$	35.7	1.1	8	49.7	2.1	24	44.9	1.0	16	47.5	3.1	16
OR	$A + B$	26.3	1.2	8	32.9	1.7	12	36.2	1.3	16	32.6	2.7	16
AND	AB	25.7	0.9	8	34.1	1.4	12	30.8	0.8	16	30.1	2.8	16
F1	$\overline{A}B$	31.2	0.8	8	45.2	1.5	12	31.8	1.1	16	31.8	2.5	16
F2	$\overline{A} + B$	32.0	1.3	8	43.1	1.9	12	33.2	1.4	16	29.6	3.5	16

TABLE 2.2: Multiple gates representation using GDI, CMOS, TG and pass gate

2.5 Switch Debounce using D flip flop

So above there are several ways to transform many logic functions using GDI technique [1]. While the formation of NAND gate using CMOS and GDI technique it has been observed that the power dissipation in NAND gate CMOS is 1.6uW and by using GDI NAND gate the power consumption is 1uW. So there is decrement of 60 percent.

Than there is a D flip flop have been made using the NAND gate. The undefined input conditions SET = "0" and RESET = "0" are prohibited in the SR NAND Gate Bistable circuit. That is the SR flip flop's disadvantage. This condition:

1. Override the action of latching feedback.
2. Make both outputs equal to one.

Give up control over the input, which initially changes to 1, leaving the other input at "0," which controls the latch's final state. An inverter is required to stop this from occurring. To create a different kind of flip flop circuit known as a D flip flop, Delay flip flop, D-type Bistable, or D-type flip flop, we connect the inverter between the Set and Reset inputs.

Of all the timed flip flop varieties, the D flip flop is the most significant. It guarantees A gated SR flip-flop with an inverter linked between the inputs is used tc that neither delay flip-flop to enable a single input D (Data). of the two inputs—S nor R—ever equals 1 simultaneously. the

The "D" designated single data input is utilized instead of the "Set" input, and the inverter is used for the complementary "Reset" input [2]. Consequently, a level-sensitive SR flip flop is the building block for the level-sensitive D-type or D flip flop. Thus, in this case, S=D and R= ~D (complement of D).

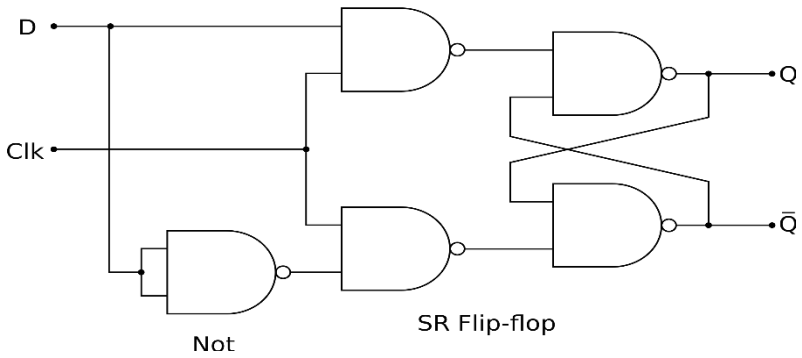


Fig. 2 .7:- Basic D flip flop using NAND gate [1]

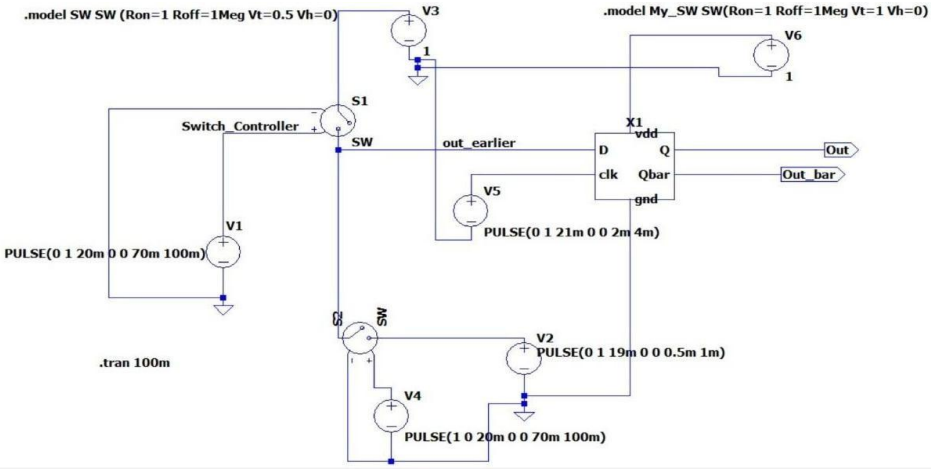


Fig. 2.8- Switch Debounce using D flip flop

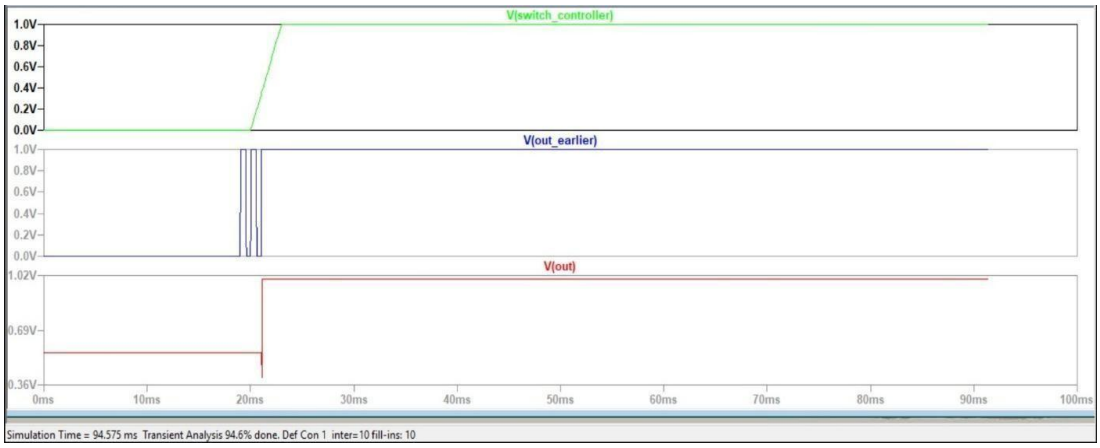


Fig. 2.9- Output of Switch Debounce using D flip flop

2.6 GDI NAND Gate representation: -

NAND using CMOS:

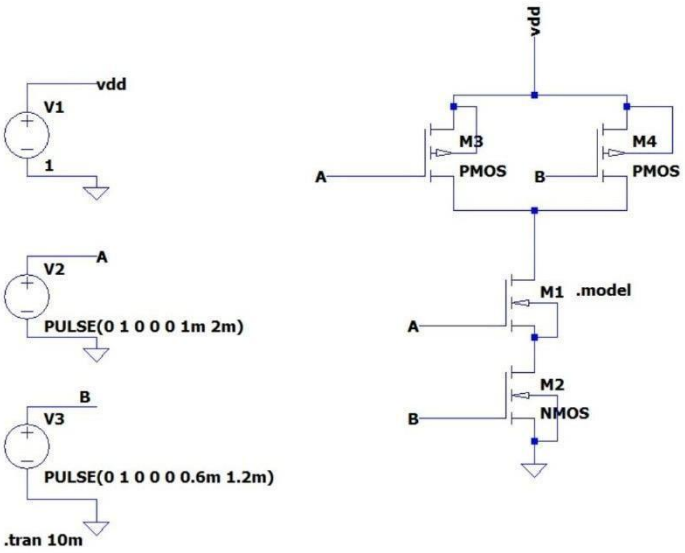


Fig. 2.10: NAND using CMOS

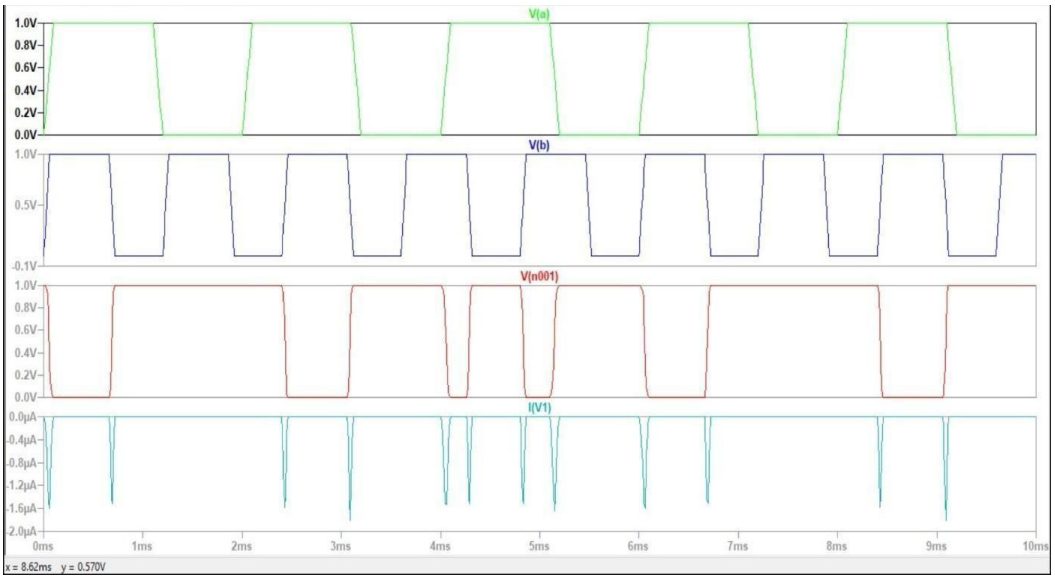


Fig. 2. 11 Output waveform of NAND gate using CMOS

2.7 NAND using GDI:

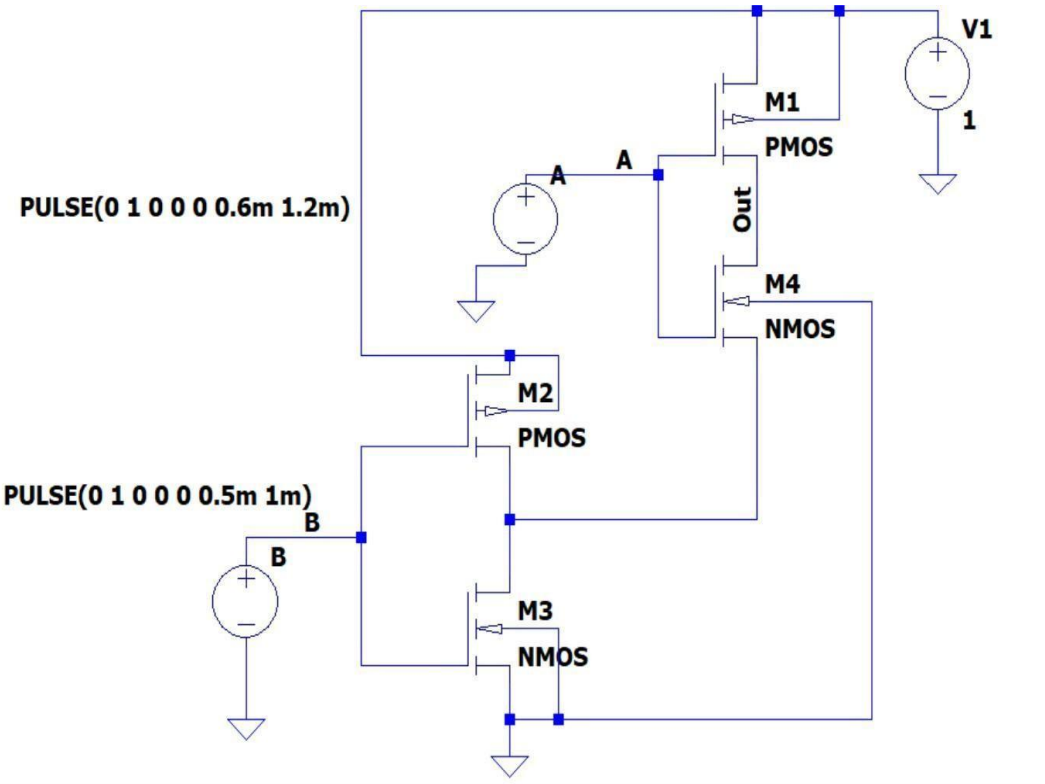


Fig. 2.12: NAND using GDI

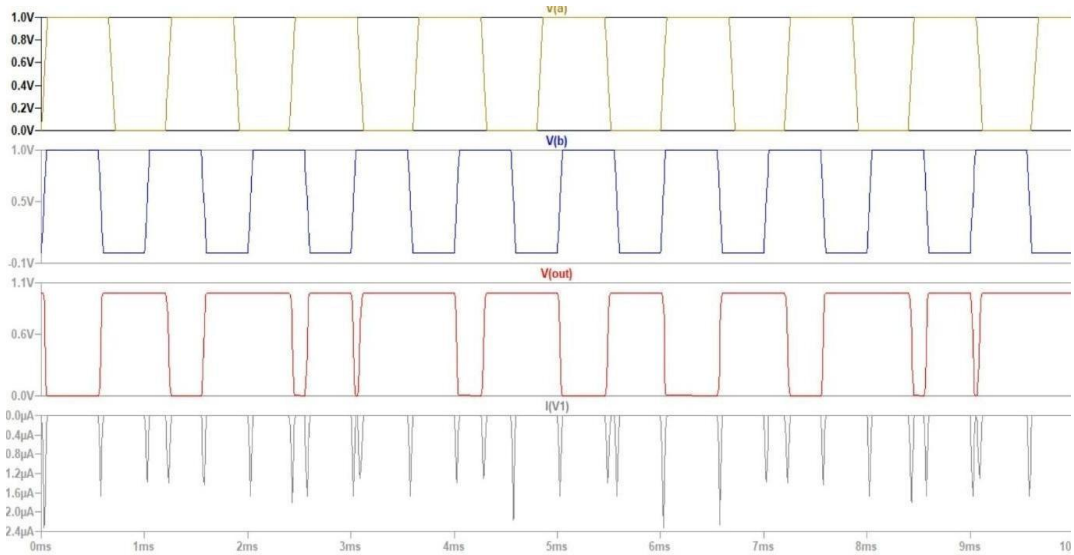


Fig. 2.13: Output waveform of NAND using GDI

One of the major advantage of using GDI technique is that they have very less leakage current as in all the stages both pmos and nmos are in stacking.

In stacked MOSFET configurations, leakage power is reduced due to the "stack effect." When multiple transistors are turned off, the leakage current from the first transistor in the stack causes a voltage to build up at the intermediate node [1]. This voltage, in turn, raises the source voltage of the next transistor in the stack, thereby reducing its gate-to-source voltage and further suppressing leakage.

As a result, the overall leakage current is diminished in the stacked configuration, since each transistor in the chain contributes to lowering the current flow. This phenomenon enables better control over static power consumption, making stacking an effective technique for leakage reduction in modern CMOS designs.

Here also, the very short circuit power as been seen as there is no such time when there is both NMOS and PMOS are ON and there is contact between power to ground.

In CMOS logic circuits, short-circuit power is minimized during switching transitions due to the inherent design of complementary pMOS and nMOS transistors [1]. During normal switching operation, at any given time, either the pMOS or the nMOS is conducting, but not both simultaneously for long periods.

This complementary behavior ensures that the direct current path from the power supply (VDD) to ground is momentarily established only during very brief transitions when the input signal changes. However, due to the relatively short overlap time and the symmetrical, sharp switching characteristics of CMOS devices, the shortcircuit current flow is limited.

As a result, short-circuit power dissipation is significantly reduced compared to other logic families (such as pseudo-NMOS or static logic families), making CMOS technology highly efficient for low-power applications.

2.8 D flip flop using CMOS based NAND:

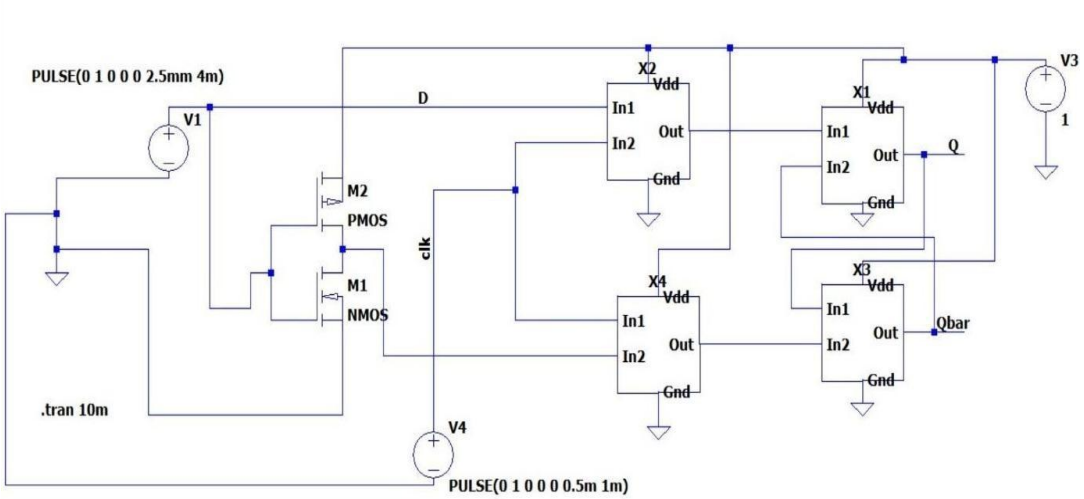


Fig. 2.14: D flip flop using CMOS based NAND

As there is less leakage power and leakage current is seen so with respect to the characteristics of the mosfet ie:-

For Vds>Vgs-Vth the current would

Saturation Region: ID = μCox W/2L (VGS − VT H)^2

As the leakage current is decreasing of the Id will be more so it will change the output load easily and which results in less delay [4]. Increase the width of transistors in the **critical path** to provide higher current drive, which helps charge/discharge nodes more quickly.

2.9 D flip flop using GDI based NAND:

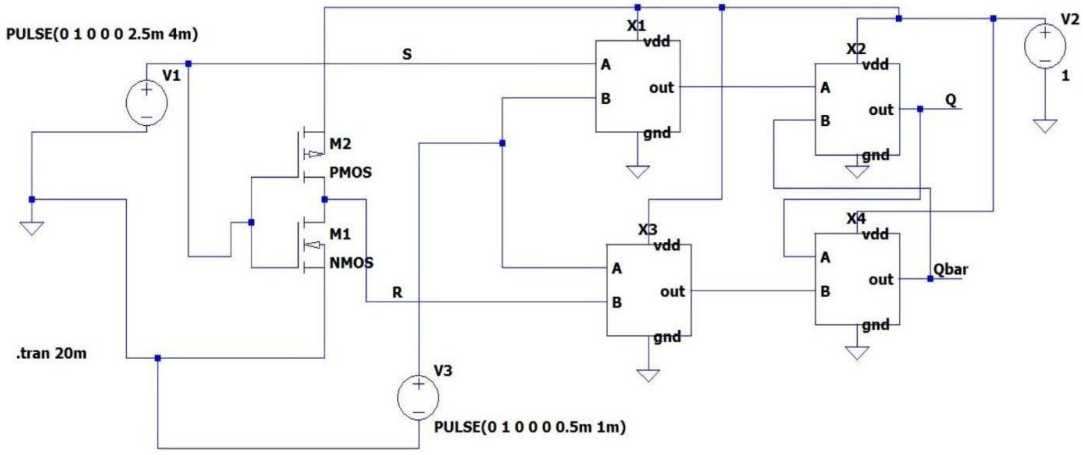


Fig. 2.15: D flip flop using GDI based NAND

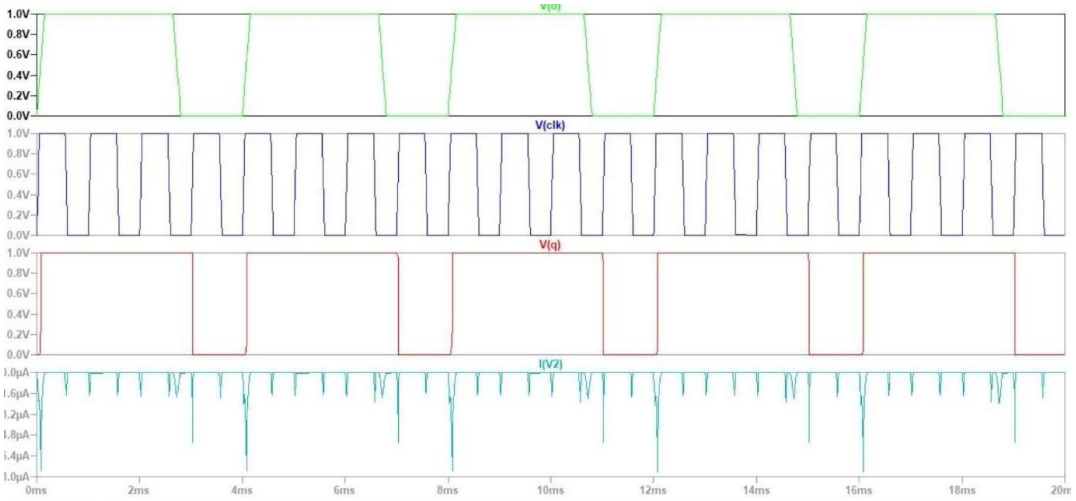


Fig. 2.15: Output waveform of D flip flop using GDI based NAND

2.10 Implementation of switch bounce circuit in LTspice:

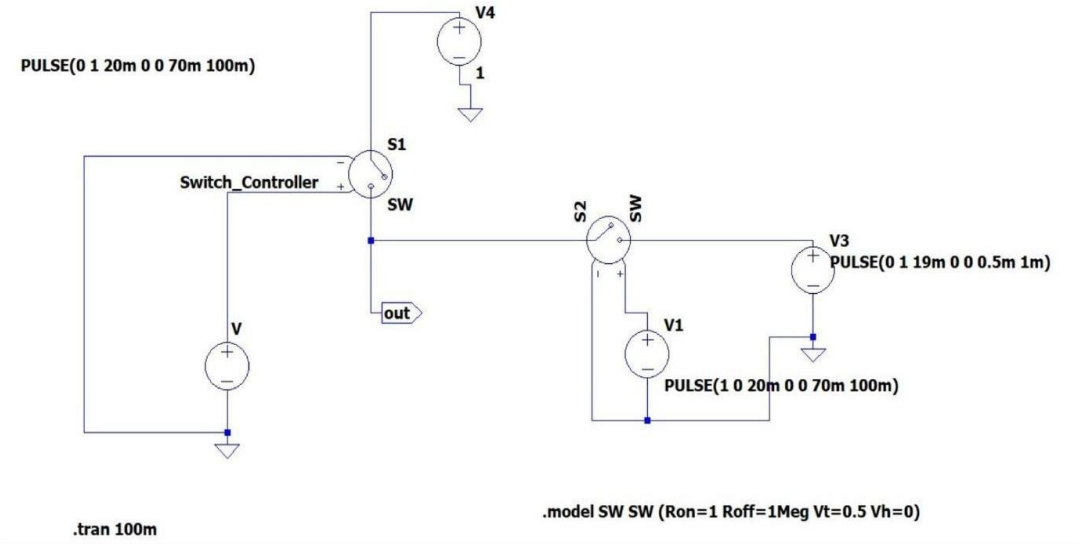


Fig. 2.16: Implementation of switch bounce circuit in LTspice

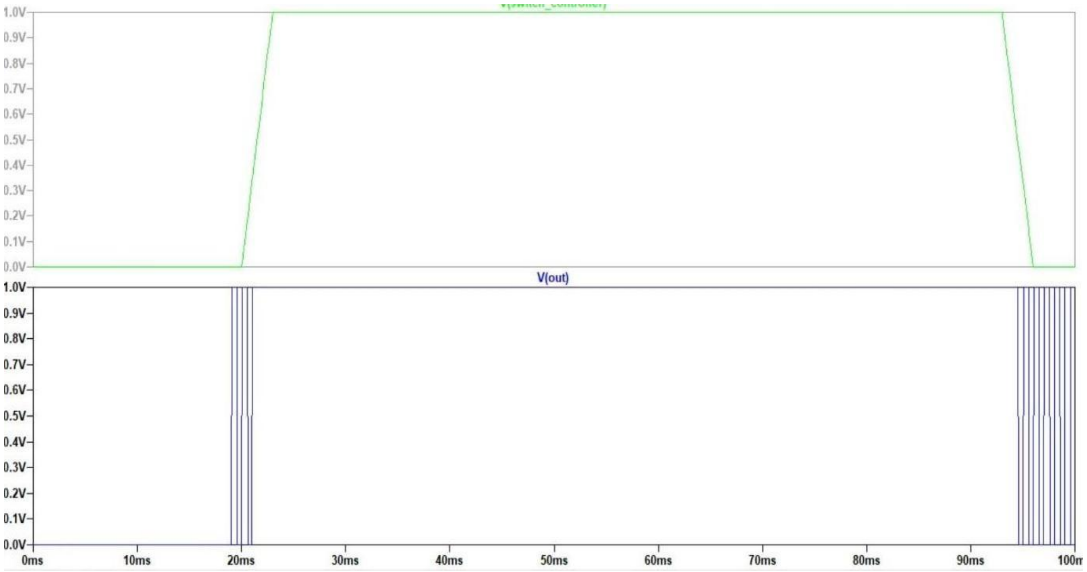


Fig. 2.17: Output of Switch bounce circuit

Here we can see that the noisy signal is getting converted to a neat and clean square waveform. This is because the DFF is storing it's value at the first clock than replicating the same.

2.11 Switch Debouncing Circuit using D flip flop:

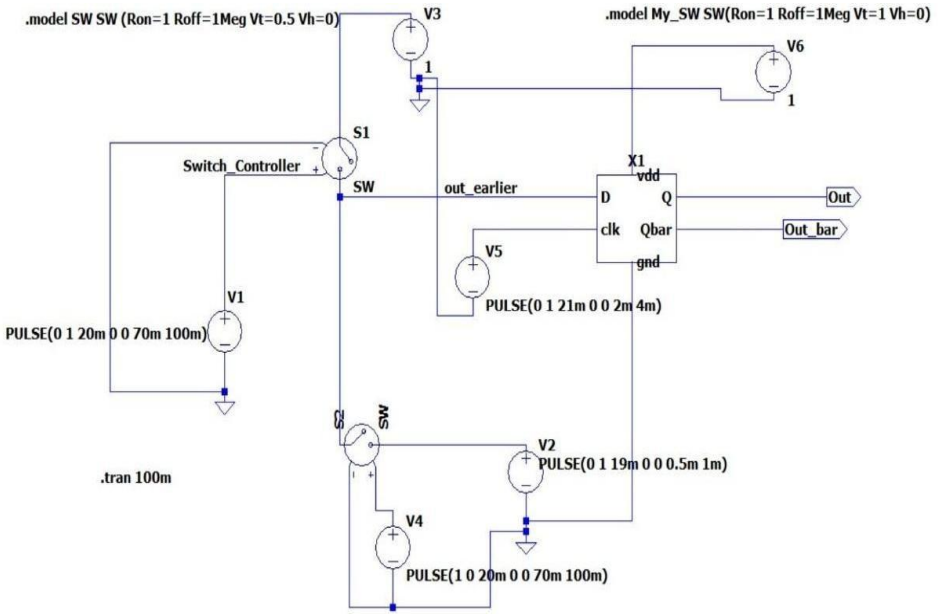


Fig. 2.18: Switch Debouncing Circuit using D flip flop

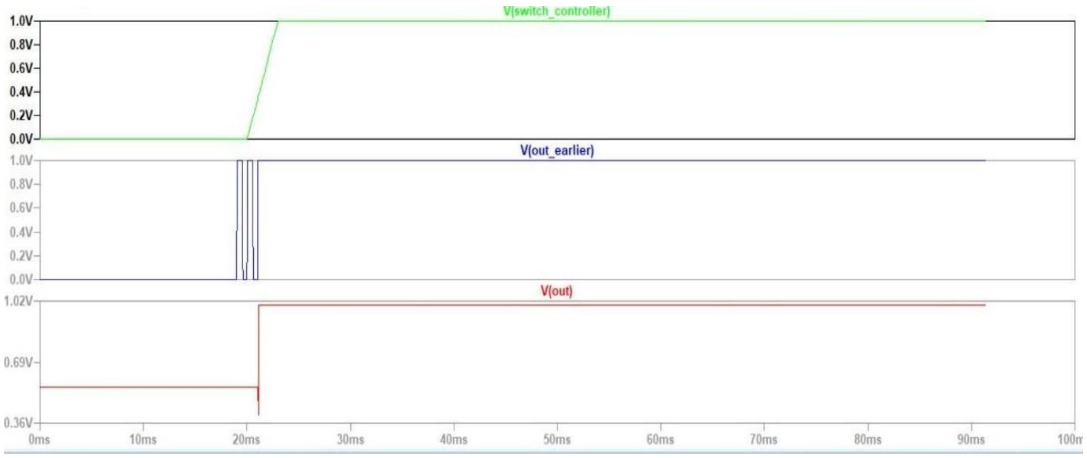


Fig. 2.19: Output of Switch Debounce circuit using D flip flop

CHAPTER 3

DESIGN METHODOLOGY

3.1 Overview of the proposed approach

There is a special methodology that has been followed which uses a Schmitt trigger to switch and debounce a bouncing circuit.

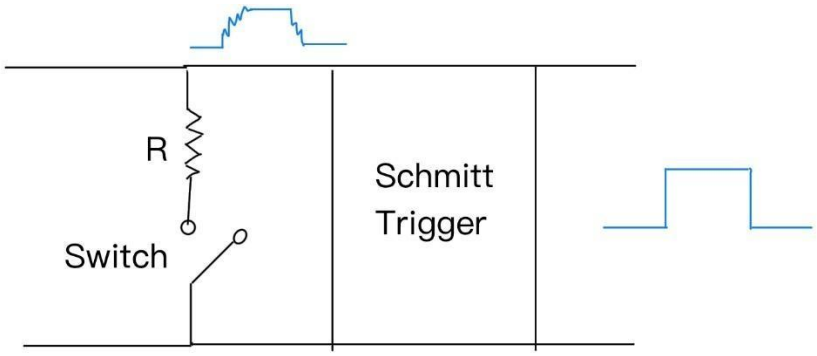


Fig. 2.20:- Switch Debouncing Methodology using Schmitt Trigger

A Schmitt trigger helps solve the problem of switch debounce by introducing hysteresis into the circuit. This means the input signal must pass a certain threshold before it triggers a change in the output, and it won't switch back until it crosses a second, separate threshold. This hysteresis prevents small fluctuations or noise—like those caused by a bouncing mechanical switch—from creating multiple unwanted transitions in the output. So, the Schmitt trigger essentially smooths out the noisy signal from the switch and ensures a clean, stable output transition.

3.2 Implementation of Schmitt trigger using NAND gate

A NAND gate can be thought of as a decision-maker in a circuit. It is given two inputs, and it is designed to check whether both inputs are ON (1). If both inputs are ON, the output is switched OFF (0). In all other cases – whether one input is OFF or both are OFF – the output is kept ON (1).

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The NAND gate is known as a NOT AND gate because it performs the opposite of an AND gate. It is considered a fundamental building block in digital logic design, and many circuits are built using NAND gates.

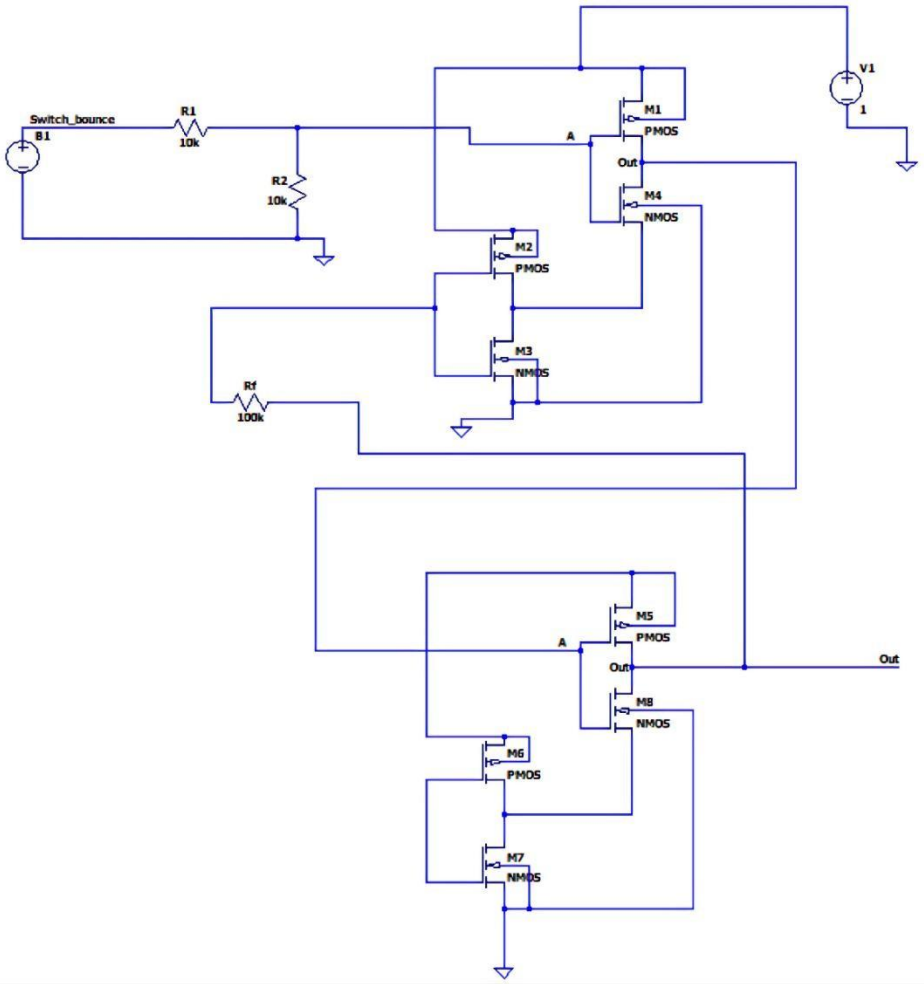

Fig. 3.1:- Implementation of switch debounce using NAND gate based Schmitt trigger

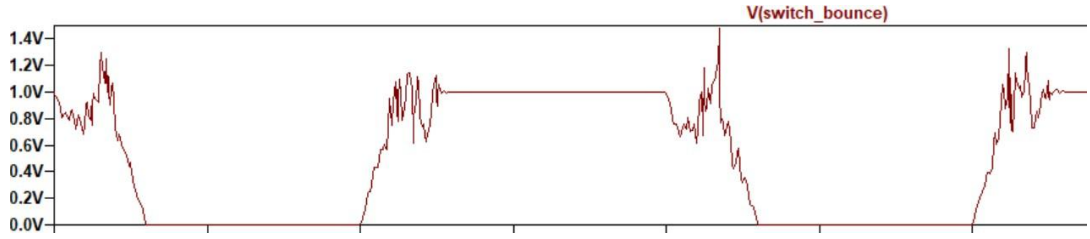

Fig. 3.2:- Input switch bounced signal

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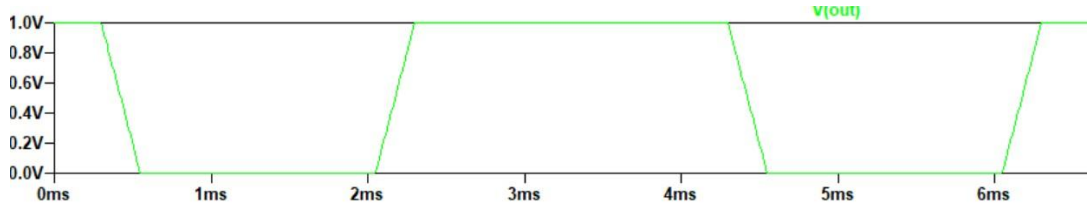

Fig. 3.3:- Output of the Switch Debounce

3.3 Hysteresis Calculations: -

[9] A Schmitt trigger has a feature called hysteresis that helps clean up noisy signals. It does this by setting two different points where the output changes. One point is for when the signal goes up, and the other is for when the signal goes down. So, the output doesn't switch back and forth wildly every time there's a small glitch or noise in the signal.

This makes a Schmitt trigger really useful for things like switch debounce, where a mechanical switch might bounce and cause messy signals. The Schmitt trigger waits for the signal to go past a certain point before changing the output, helping to keep the output smooth and stable.

Calculation of V_{HT} and V_{LT}:-

For R1=10 kΩ

R2=10 kΩ

Rf= 100 kΩ

For threshold voltage of the NAND gate Vth=0.35

For upper threshold (V_{HT})

V_{HT} = (R1+R2)/R2 * Vth

= (10k+10k)/10k * 0.35

= 0.7V

For lower threshold calculation (V_{LT})

V_{LT}= ((R1 || R2) || Rf)/R2 * Vth

= 0.16V

Hysteresis will look like:-

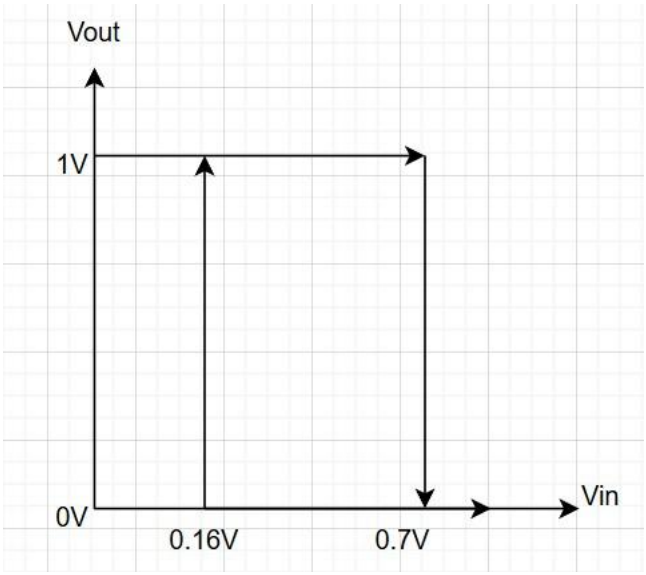

Fig. 3.4- Hysteresis of the applied Schmitt Trigger

A Schmitt trigger has this cool feature where it waits for the signal to cross a certain level before it flips the output. In this case, it has two thresholds:

- If your signal goes above 0.7 volts, the output jumps up (to, say, 1 or 5 volts).
- If your signal drops below 0.16 volts, the output drops down.

Between these two points—0.16 volts and 0.7 volts—the output stays put. It doesn't react to small wobbles or noise in the signal.

So, imagine a bouncy switch that keeps flipping up and down randomly when it's pressed. If you feed that noisy signal into a Schmitt trigger, the trigger won't care about those tiny ups and downs. It'll only change the output when the input clearly crosses those specific points.

That way, the Schmitt trigger gives you a nice, clean, stable output that doesn't flip-flop every time there's a tiny spike in the input. That's why it's great for fixing problems like switch bounce.

3.4 Applying Switch Debounce using Schmitt Trigger:-

When you press a physical switch, it doesn't always give a clean 0 to 1 voltage change [11]. Instead, because of mechanical imperfections, it bounces—the voltage might jump between 0 and 1 several times very quickly before settling. This is called switch bounce**.**

Now, if you directly feed this bouncy signal into a digital circuit, the circuit might get confused and think the switch is being pressed and released multiple times. That's a problem!

Here's where the Schmitt trigger comes to the rescue.

Let's say the switch voltage bounces up and down between 0 and 1, but gradually increases overall:

- The Schmitt trigger ignores the small, random fluctuations and only switches the output when the signal crosses the upper threshold—in your case, 0.7 volts.
- Once it switches high, even if the signal dips back down slightly (but stays above 0.16 volts), the output remains high.
- The output only switches low if the signal drops below 0.16 volts.

So, the Schmitt trigger effectively filters out the bouncing noise from the switch. It doesn't react to every little change—it waits for the signal to cross a clear boundary, either high or low.

That's why it's so useful for switch debouncing! It makes sure the output only changes once per actual press of the switch, not every time the signal jitters.

CHAPTER 4
FUTURE SCOPE

4.1 Future research methodology

This is our proposed figure of the switch debounce circuit. The input from the switch is passed to the input in the figure above. For the input, we will be producing the noisy waveform using the LTspice [13]. The noisy input produced by the LTspice circuit is given to the XOR gate, as well as to a DFF, which has an output port from which a clean signal can be obtained. Here output of the RC circuit is passed to the output port after a delay of five clock. cycles. The switch debounce circuit, after sampling the first transition (initial state) on the switch, waits for a predetermined time (settling time) and checks whether the current state matches the sampled state. If there is a match, it is a valid transition (state change of switch), otherwise, it is considered as a glitch (bounce) and ignored. The circuit further continues to sample the switch state. In this way, the circuit will respond to only one pulse generation and not several state transitions caused by contact bouncing.

Here one of the inputs to XOR gate is the output from the last D-FF and another is from the terminal which is connected to bouncing input. If both the inputs of the XOR gates are equal, the output of XOR gate will be LOW else it will be HIGH which serves as clock to the final stage DFF from which Qout which is the final output without any bouncers are obtained. The output of the final stage DFF will retain the previous state till the clock goes high. The clock will go high only after pre-determined time during which the sampled state (bounce-free) has to be stable [17]. In D flip flop, reset is used because flip flop is often used for implementation of circuits that can have many possible states, where the response of circuit depends not only the inputs but also on the states that the circuit is in at that time. Hence reset is used to obtain the initial state of the DFF. Electrostatic discharge (ESD) [7], which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all ICs. Due to electrical over stress (EOS) which is caused due to high voltages exceeding the data sheet values, gate oxide dielectric breakdown which might

damage the ICs. Hence input and output pads are used for the debounce circuit to avoid the damage.

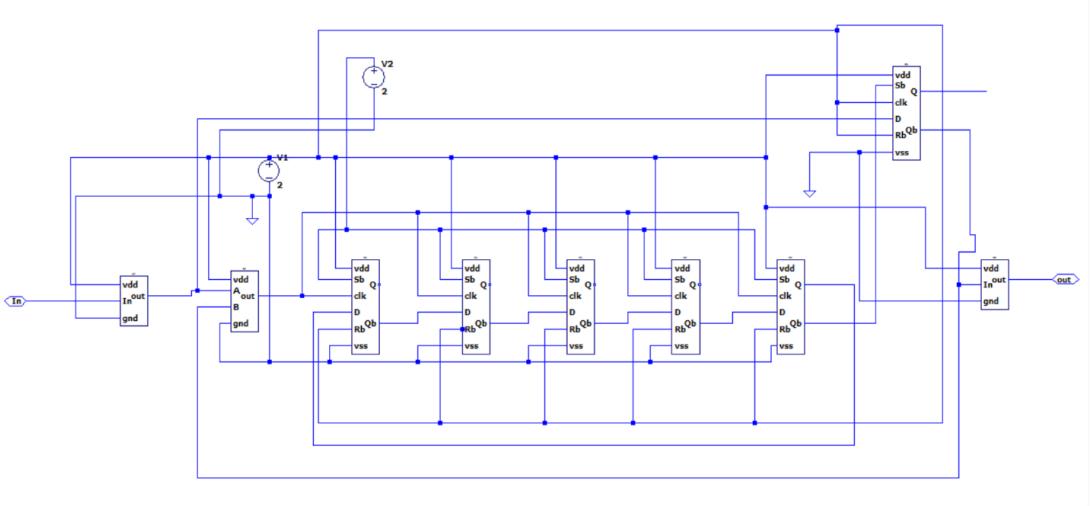

Fig 4.1 Cascading DFF to avoid the problem of switch bouncing.

In the above figure it has been done that the there are DFF made into cascades to basically make the samples of the input switch bouncing signals. There are samples made and then the system will decide the constant samples to keep so judge the following signal [5]. That if the signal is going from 0 to 1 then in between the transition there is so many voltages achieved between them then the system will take multiple samples of the signal, in the above figure the number of samples that are taken are 5 and then these samples are compared such that there values average is taken and then the side values are compared that is initial 2 samples are compared with the last 2 samples, if these samples are different then it will be assumed that the signal is changing from 1st sample value to 2nd sample value. If the samples average value of the first 2 and the last 2 are same that means the signal is constant and this constant signal can be judged by watching that how close they are actually to the 0 or 1 [4]. By using this methodology it becomes easy to get the proper refined signal out of the switch bounced signal which is the target of this thesis and our research.

4.2 Comparison between switch debounce circuit using CMOS and GDI

Circuit Description	Average Power	Area	Output delay
Switch Debounce using CMOS based DFF	2.46E-07	228568.microns^2	3.95ns
Switch Debounce using GDI based DFF	1.95E-07	23487.3microns^2	2.8ns

Table 4.1- Comparing the switch debounce circuit between using CMOS and GDI.

So here we are reducing the power a delay on the cost of the increase in area. The reduction of circuit area is achieved by minimizing the number of transistors required for logic gate implementation [6]. In conventional CMOS logic, multiple transistors are used to realize even basic gates, which leads to an increase in the layout size. However, by applying techniques such as the Gate Diffusion Input (GDI) method, the same logic functions can be achieved with fewer transistors. As a result, the overall area occupied by the circuit is significantly reduced. Additionally, the complexity of interconnections is minimized, which further contributes to a more compact layout. This reduction in area not only enables the design of smaller and more efficient circuits but also supports the integration of a larger number of functionalities within a limited chip space. By optimizing the circuit in this way, lower power consumption and improved performance can also be achieved, making the design more suitable for portable and battery-powered applications.

CHAPTER 5
CONCLUSIONS

In this thesis, I set out to tackle a common yet critical problem in digital systems—switch bouncing—by designing a hardware debounce circuit that is both low-power and efficient. The approach I followed was to build a Schmitt Trigger-based debounce circuit, where the Schmitt Trigger itself was implemented using NAND gates. To make the design even more optimized, these NAND gates were created using the Gate Diffusion Input (GDI) technique, a proven method for reducing power consumption, propagation delay, and overall area in digital circuits.

Through simulation and analysis, I demonstrated that the GDI-based NAND gates are highly effective in reducing power usage compared to traditional CMOS designs [9]. The Schmitt Trigger designed using these GDI NAND gates exhibited a clear hysteresis behavior, with an upper threshold voltage of 0.7V and a lower threshold voltage of 0.16V. This hysteresis characteristic was key in stabilizing the output signal, effectively suppressing the noise and transient glitches caused by switch bouncing. As a result, the final debounce circuit was able to deliver a stable and clean output in the presence of noisy and fluctuating inputs—solving the switch bounce problem efficiently.

Beyond just solving the problem at hand, this thesis also highlights the broader potential of using GDI logic techniques in real-world digital designs. By integrating GDI into fundamental circuits like NAND gates, [10] and then building higher-level functions like Schmitt Triggers and debounce circuits, we can achieve significant improvements in power efficiency—something that is especially important for today's battery-powered devices and embedded systems.

In conclusion, this project not only provides a practical solution for switch debouncing using a Schmitt Trigger, but also serves as a proof-of-concept for how GDI-based logic design can be used to build more power-aware and area-efficient digital systems. This approach opens doors for future exploration into applying GDI

techniques in other sequential and combinational circuits—like counters, registers, and memory elements—paving the way for low-power, high-performance digital electronics in the era of portable and energy-conscious devices.

Furthermore, the choice to implement the Schmitt Trigger using NAND gates—the universal building blocks of digital logic—ensures that the design remains modular, scalable, and easy to integrate into a variety of digital circuits. By employing the GDI technique for constructing these NAND gates, the circuit achieves remarkable reductions in power consumption, propagation delay, and silicon area when compared to traditional CMOS-based implementations [11]. This is particularly significant in the context of modern digital systems, where energy efficiency is a top priority due to the growing demand for portable, battery-operated, and resource-constrained devices such as wearables, IoT nodes, and embedded systems.

The simulations conducted as part of this work validate the effectiveness of the proposed design [13]. The GDI-based Schmitt Trigger demonstrates robust behavior in the presence of noisy, bouncing input signals, producing a clean, stable output suitable for interfacing with microcontrollers, digital counters, and other logic circuits. The power consumption analysis reveals substantial savings compared to conventional CMOS logic, confirming that GDI is a viable and superior alternative for low-power digital design. The waveform results clearly illustrate the suppression of bounce-induced glitches, thereby solving the core problem of mechanical switch instability in a hardware-efficient manner.

Beyond just solving the switch bounce problem, this thesis contributes to the broader field of low-power digital design by showcasing how fundamental circuit elements—like the Schmitt Trigger—can be reimagined using innovative design techniques like GDI. The approach taken here is modular and generalizable; the same design philosophy can be extended to other digital components, such as counters, shift registers, oscillators, and even small-scale memory cells. This opens up exciting possibilities for further research and development in the domain of ultra-low-power VLSI circuits.

Moreover, this work emphasizes the importance of rethinking standard design practices in the light of power, area, and performance constraints. While CMOS technology has been the industry standard for decades, this project demonstrates that alternative techniques like GDI can offer tangible benefits in specific use cases, particularly when power efficiency is critical. The GDI-based Schmitt Trigger design

thus stands as a testament to the potential of non-conventional design methodologies in meeting the demands of modern electronics.

In conclusion, this thesis presents a practical, effective, and power-conscious solution to the problem of switch bouncing—a solution that is not only applicable in theory but also validated through simulations and analysis. It underscores the role of GDI logic as a valuable tool in the arsenal of digital designers seeking to build circuits that are both functional and energy-efficient [19]. This work paves the way for further exploration of GDI-based circuits in more complex applications, potentially contributing to the design of next-generation low-power digital systems that are increasingly relevant in our technology-driven world.

Further we can get more better techniques of low powering in Switch Debouce circuit [17]. Also, we can make the layout of the circuit and can check the possible input and the compatibility of the outer noise with the different layers of the layout. The applications that are implemented using GDI can be used to further the implementation of circuitlike counters where the particular gate can be replaced with this low-power technique. Similarly, some memories include so many transistors which require synchronization and very little delay, and for this application, we can use this low-power technique. Similarly, it can be used in shift registers. The application of switches has always under consideration in digital as well as analog circuits. Further we can generate a better switch debounce circuit which uses active element like BJT, MOSFET as switches [19]. However, some still remain unexplored and have the ability of providing promising benefits in terms of improvisation in area, power consumption and speed of the circuits.