M.TECH (Power Electronics and Systems)

DESIGN AND DEVELOPMENT OF SOLAR GRID INTERFACED SYSTEM AND THEIR APPLICATIONS TO EV CHARGING INFRASTRUCTURE

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Submitted by

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DECLARATION

I, Ravi Ranjan Chaudhary, Roll No. 2K23/PES/08 student of M.Tech (Power Electronics and Systems), hereby declare that the project Dissertation titled **"Design and Development of Solar Grid Interfaced System and their Applications to EV Charging Infrastructure"** which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original work and not previously used for the award of any Degree.

Place: Delhi **RAVI RANJAN CHAUDHARY**
Date: 2nd June 2025

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"Design and Development of Solar Grid Interfaced System and their Applications to EV Charging Infrastructure"** which is submitted by RAVI RANJAN CHAUDHARY (2K23/PES/08), Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This study uses surplus electricity from renewable energy sources and power networks with extra capacity to provide a unique and integrated method to high-efficiency battery charging systems. The suggested technique reduces reliance on the central grid while permitting optimal battery charging and discharging by using self-tuning filters (STFs) to obtain undistorted fundamental load current. Through adaptive charging procedures, this technique not only increases the use of renewable energy but also prolongs battery life by intelligently managing extra power. We develop and analyse a power conversion system based on an interleaved totem-pole converter with power factor correction (PFC) enabled, followed by a full-bridge LLC resonant converter, to support this strategy. This dual-stage architecture combines the high-efficiency soft-switching properties of the LLC stage with the near-unity power factor and decreased input current ripple benefits of the totem-pole PFC stage. The combined system is designed for uses including grid-integrated renewable storage systems and electric vehicle (EV) charging that need for small, high-performance AC-DC power conversion. For both converter stages, a thorough analysis of component selection, control schemes, and operating principles is given. The effectiveness of the suggested system is validated by simulation results, which show good efficiency throughout a broad input voltage and load range. Possible directions for further study are also noted, such as the system's scalability for larger-scale implementations and interaction with cutting-edge energy management platforms. All things considered, this

work presents a potential path for intelligent, efficient, and sustainable power conversion in next-generation energy infrastructure.

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CHAPTER 1

INTRODUCTION

Performance and analysis of solar grid interface EV charging infrastructure by using STF Controller

The increasing global demand for electric vehicles (EVs) necessitates the establishment of a comprehensive network of EV charging stations. A multi-faceted strategy is being implemented to oversee critical elements such as battery charging and discharging, optimizing vehicle routes, and guaranteeing the seamless functioning of the controllers [1].

Charging stations must be established at residential properties and commercial establishments to accommodate the requirements of both private and business sectors. Renewable energy sources, particularly photovoltaic (PV) technology, are essential for energizing these stations [2].

Recent improvements in photovoltaic technology have markedly enhanced solar energy generation, rendering it more efficient, cost-effective, and accessible.

Furthermore, due to the increasing focus on renewable energy and combating climate change, the integration of energy efficiency measures has become essential. Nonetheless, a significant problem persists in regulating unforeseen variations in renewable energy production [3].

An innovative method for optimizing battery charging in renewable energy systems has been devised, employing a dynamic mechanism referred to as a Self-Tuning Filter (STF) [4-5].

The STF, in conjunction with a phase-locked loop (PLL), can enhance power quality, particularly under suboptimal grid conditions. This technology efficiently directs extra energy, whether from solar photovoltaic panels or the electrical grid, towards optimal battery charge. The STF algorithm optimizes energy flow by continuously assessing real-time data, including solar panel energy output, grid power supply, and a building's current energy usage [6-7].

This approach improves system stability, diminishes dependence on the grid, optimizes the utilization of renewable energy, and enhances the efficiency of battery charging and discharging. This strategy clearly presents the possibility for more sustainable energy management, providing tangible advantages for both energy consumers and the environment.

PFC- Interleaved Boost converter Full bridge LLC resonant DC- DC Converter

In recent years, the increasing acceptance of electric vehicles (EVs), the expansion of data centres, and the incorporation of renewable energy sources into the grid have significantly heightened the demand for small, dependable, and highly efficient power conversion devices. These applications necessitate AC-DC converters that provide high power density and efficiency while adhering to stringent grid-side power quality criteria, including minimal harmonic distortion and near-unity power factor [8]. The interleaved totem-pole power factor correction (PFC) converter, in conjunction with a full-bridge LLC

resonant converter, has emerged as a viable solution for medium to high power applications among several configurations utilized to achieve these objectives. Conventional PFC circuits, such as the boost converter, have historically been employed to comply with regulatory power quality standards like IEC 61000-3-2. Nonetheless, these converters function under hard-switching conditions, resulting in increased switching losses, decreased efficiency, and heightened thermal stress on semiconductor devices especially at elevated switching frequencies [9]. Furthermore, the diode bridge in traditional PFC configurations introduces significant conduction losses, particularly in high-power applications. The bridgeless totem-pole PFC converter architecture has garnered considerable interest in contemporary literature and industrial applications to address these limitations. This topology removes the input diode bridge and permits either unidirectional or bidirectional operation, contingent upon the configuration. The totem-pole PFC converter, when utilized with wide bandgap (WBG) semiconductor devices like silicon carbide (SiC) MOSFETs, delivers exceptional performance characterized by diminished conduction losses, enhanced switching frequency capability, and superior thermal performance [10][11] GaN devices provide effective operation in continuous conduction mode (CCM) at high frequencies, minimizing the size of passive components and improving power density [12].

An additional improvement to the totem-pole PFC design entails the implementation of interleaving. Interleaving multiple PFC phases with an appropriate phase shift leads to the mitigation of input current ripple, enhanced thermal distribution among power devices, and less EMI emissions [13]. This method is particularly advantageous at power levels of

2–7 kW and higher, where current capacity and thermal regulation are paramount issues. Furthermore, interleaved operation alleviates the strain on each individual switch, thus enhancing system dependability and longevity [14]. While an efficient AC-DC front-end stage has its advantages, the DC-DC conversion stage is equally crucial for maintaining output voltage regulation, providing galvanic isolation when necessary, and enhancing overall efficiency. The full-bridge LLC resonant converter is distinguished among isolated DC-DC topologies for its capability to facilitate soft-switching, namely zero voltage switching (ZVS) for primary switches and zero current switching (ZCS) for secondary rectifiers, across an extensive load range [15]. The resonant characteristics of the LLC architecture enable operation at elevated frequencies with diminished switching losses and electromagnetic interference (EMI), rendering it optimal for compact and thermally efficient devices. Moreover, the LLC converter's frequency modulation control mechanism facilitates effective load regulation and is comparatively simpler to construct than pulse-width modulation (PWM)-controlled hard-switched converters. This renders it especially appropriate for high-efficiency applications, including electric vehicle onboard chargers, server power supply, and industrial automation systems [16]. It also guarantees that efficiency remains elevated under partial load conditions, a significant factor in practical applications since converters seldom function at full load consistently. This research presents a thorough design and analysis of a 6.6 kW interleaved totem-pole power factor correction converter supplying a full-bridge LLC resonant converter. The converter is designed to function with a universal AC input (often 85–265 V) and deliver a regulated high-voltage DC output appropriate for applications like electric vehicle DC chargers. The

aim of this study is to utilize the synergistic advantages of the interleaved totem-pole PFC stage and the soft-switching LLC resonant topology to attain a high-performance, low-loss power conversion system. A major issue in this integrated architecture is the optimal design and coordination of both phases. The output of the PFC stage must correspond precisely with the input specifications of the LLC stage, especially for voltage level, dynamic response, and control loop stability. The interleaved PFC stage must guarantee minimal harmonic distortion and a high-power factor at the input, while maintaining a steady DC bus voltage despite fluctuations in line and load conditions. Simultaneously, the LLC step necessitates meticulous tuning (by resonant tank design and transformer selection) to guarantee zero-voltage switching across a broad load spectrum, uphold output voltage regulation, and satisfy isolation criteria where relevant [17]. This study primarily concentrates on optimizing the efficiency of the entire system. Simulation and analytical findings indicate that the suggested topology can attain a peak efficiency above 96% at rated capacity (6.6 kW), with efficiency curves remaining generally constant across partial load scenarios. The interleaving technology, utilization of SIC-based fast-switching devices, meticulous thermal design, and soft-switching operation of the LLC stage facilitate this achievement. Furthermore, the performance of EMI and thermal distribution are evaluated to guarantee practical viability and adherence to industrial requirements. The proposed design technique encompasses component selection (e.g., inductors, resonant components, transformers, and MOSFETs), steady-state and dynamic modelling, control strategy formulation, and simulation-based validation utilizing platforms such as MATLAB/Simulink. The application of sophisticated digital

controllers, such as those from Texas Instruments, is examined for the real-time execution of interleaved power factor correction and resonant converter control strategies This study examines the design trade-offs faced in practical situations, including efficiency versus cost, size versus thermal performance, and switching frequency versus electromagnetic interference (EMI). Special emphasis is placed on the issues presented by light-load operation, grid disturbances, and transient load circumstances, all of which can affect the overall efficacy of the power supply system. These elements are assessed via both simulation and empirical data to guarantee the proposed system's robustness and reliability. This research advances the field of power electronics by introducing a high-efficiency, compact, and scalable AC-DC power conversion system utilizing a 6.6 kW interleaved totem-pole PFC front-end and a full-bridge LLC resonant DC-DC stage. The suggested converter topology, when executed using contemporary WBG semiconductor devices and digital control methodologies, signifies an innovative answer for future energy systems.

CHAPTER 2

LITERATURE SURVEY

2.0 General

PQ issues have caused major problems in power distribution systems. Non-linear loads inject harmonics in the grid which deteriorate both grid voltage and grid current. The grid current related problems can be solved by Shunt Active Power Filter (SAPF). The SAPF is designed to improve power factor, harmonics in source current, performs load balancing and reactive power balance. The grid voltage related issues such as voltage sag, swell, DC offset, harmonics are addressed by the Phase Locked Loop techniques. They generate the sinusoidal unit in phase template even under weak grid conditions for generation of reference current signals. Phase Locked Loop Techniques are needed for synchronizing the power electronic equipment with the grid. PLLs track the phase angle and the grid voltage while synchronizing. New and adaptive neural network controllers are used for mitigation of power quality problems for SAPF in single-phase and three-phase grid connected systems. The adaptive PLL techniques are designed for mitigating grid voltage problems.

2.1 Literature Survey

Current based and voltage-based power quality problems are discussed in this section. There are various voltage and current based power quality problems. The voltage-based power quality problems in grid include voltage sag, swell, harmonics, voltage flicker, DC

offset, phase angle change, frequency change, fluctuations and notches. The current based power quality problems are poor power factor, reactive power burden, harmonics current, unbalanced currents. The power quality problems and solutions are discussed as follows.

2.1.1 Power Quality Problems and Solutions

Power distribution systems feed a variety of loads-linear loads, mixed loads and non-linear loads. Non-linear loads consist of solid-state devices. They use cycloconverters, AC voltage controllers, computers, televisions etc. [17-21]. The solid-state devices have many benefits of lower cost, reduced maintenance and less wear and tear. Moreover, the non-linear loads inject harmonics in to the system [22-25]. Power quality problems related to current drawn from the AC mains are poor power factor, reactive power burden, harmonics current, unbalanced currents. They cause voltage harmonics, spikes, notches, voltage dip, voltage swell at the point of common coupling [26].

2.1.2 Integration of Renewable Energy Resources to the Grid

These days integration of renewable energy resources with the grid is increasing due to the increased price of fossil fuels, increased global warming and pollution. However, photovoltaic sources have gained importance compared to other renewable energy resources due to availability of solar energy in abundance. In PV based VSC the efficiency of the SAPF is increased as it performs dual function of bidirectional flow transfer and as well as shunt compensation. Therefore, VSC does not remain idle but performs all the time [27-31]. The PV feedforward term is added to mitigate DC link voltage fluctuations during integration of renewable energy resources [32-33]. The VSC may be directly

connected to the PV source through DC link referred to as Single Stage Topology or can be integrated through DC-DC boost converter based Double Stage Topology. In this thesis, Double Stage Topology is used. It offers various advantages of reducing the control complexity though the device count is less in single stage, it has an increased operation region and more flexibility due to independent Maximum power point tracking techniques. The solar PV power being non-linear in nature uses maximum power techniques which vary the duty cycle of boost converter array to attain maximum power from the PV [34-39].

2.1.3 Power Quality Standards

The international standards related to power quality has been developed by various organizations such as Institute of Electrical and Electronics Engineers (IEEE) and International Electro Technical Commission (IEC). These standards are developed, updated and imposed to maintain the power quality level [40-41].

2.2 PLL Control Algorithms

The grid voltage related issues such as voltage sag, swell, DC offset, harmonics are addressed by the Phase Locked Loop techniques [42-47]. They generate the sinusoidal unit in phase template under weak grid conditions for generation of reference current signals. The Phase Locked Loop Techniques are used for synchronizing the power electronic equipment's with the grid. PLLs track the phase angle and the grid voltage while synchronizing [48-51]. The accurate estimation improves the performance of the

power electronic converters. Various PLLs are described in the literature [52-67]. SRFT PLL is discussed in [68-72].

2.3 PV Battery Interfaced Control Algorithms

PV interfaced battery connected systems in both grid connected and islanded mode have also been discussed in literature. The current control mode is used in grid connected mode and voltage control is used in islanding condition [73-74]. Current control mode is developed to improve power quality problem and voltage control mode provides synchronization in the absence of utility grid [75-76].

2.4 Power Factor Correction

Power factor correction (PFC) is a crucial method employed in power electronics to enhance the efficiency and quality of electrical energy consumption. It optimizes the utilization of power from the grid by synchronizing the current waveform with the voltage waveform. Both waveforms should ideally be exactly in-phase and sinusoidal, yielding a power factor of unity [77-80]. Many contemporary electronic devices, particularly those with non-linear loads such as power converters and motor drives, draw distorted currents, resulting in a diminished power factor. This not only induces energy losses but also exerts additional strain on the power grid, potentially leading to increased electricity costs due to utility penalties. Power factor adjustment is employed to resolve this issue through either passive or active ways. Passive [81-83].

2.4.1 Bridgeless Totem-pole PFC

The bridgeless totem-pole power factor correction (PFC) converter is a contemporary and highly efficient configuration utilized for AC-DC conversion, especially in applications where power density and energy efficiency are paramount, including electric vehicle (EV) chargers, data centres, and industrial power supplies.[84-86] In contrast to conventional boost PFC circuits that utilize a full-bridge diode rectifier, the totem-pole PFC omits this bridge and employs fast-switching semiconductor devices (usually GaN or SiC FETs) to facilitate current flow during both phases of the AC cycle. This "bridgeless" structure markedly diminishes conduction losses and enhances overall efficiency, frequently attaining power conversion efficiencies above 98% [87-88]. In this design, high-frequency switches function continuously during the AC cycle, while low-frequency MOSFETs or diodes establish the requisite unidirectional pathways. The outcome is a more straightforward conduction pathway, a reduction in components, and enhanced thermal efficiency [89-90].

2.5 LLC Resonant DC-DC Converter

A specific LLC converter topology known as the Series Resonant Converter (SRC) has a comparatively large magnetizing inductance that is not engaged in the resonance action [91-94]. Compared to the traditional series resonant converter, the LLC converter offers numerous advantages. For instance, it maintains extremely high efficiency while controlling the output voltage throughout large line and load fluctuations with a comparatively tiny switching frequency variation. Throughout the whole operating range,

it can also function at zero voltage switching (ZVS). An illustration of the Full Bridge LLC converter that shows the magnetizing inductance and all other parameters mirrored to the transformer's primary side In contrast to conventional resonant converters, it is evident that the two inductors (Lr and Lm) and the resonant capacitor (Cr) offer special features in terms of switching losses as well as static and dynamic properties [95-96]. Although the LLC converter can function with either frequency modulation (FM) or pulse width modulation (PWM), we will only examine how it behaves in the most prevalent scenario of frequency modulation [97-99].

CHAPTER 3

DESIGN AND ANALYSIS OF GRID CONNECTED SYSTEMS

3.0 General

A three-phase non-linear load is coupled to a three-phase 110V supply [100]. The Battery charging block diagram is shown in Fig.3.1, The charging station's primary goal is to guarantee that there is excess power, which is sum of power generated by the PV (P_{pv}) and Grid power (P_{grid}) minus power consumed by the load (P_{Load}). Available for Battery charging. The charging and discharging of battery are controlled by the bi-directional converter switching. Through a DC-DC Boost converter, the PV array is connected to DC-link.

3.1System Configuration of SAPF in Grid Connected System

In single-phase and three-phase systems, respectively, the traditional H-bridge and three-phase three-leg voltage source converter topologies are covered in this section.

3.1.1System Configuration of STF in Three-Phase Grid Connected System

A PV integrated grid-connected distribution system that feeds both linear and non-linear loads connected at the PCC makes up the suggested system. Diode bridge rectifiers with series R-L loads are used to mimic non-linear loads. With the source impedance Zs (source resistance Rs and inductance Ls), interfacing inductor Lf, ripple filter Rc, diode bridge

rectifier, and VSC with DC link capacitance all connected collectively at PCC, the system design is displayed in Fig.1 shows the circuit diagram of a three-phase double-stage grid-tied PV system with Self Tunning Filter (STF) attached. The STF is implemented through six IGBTs paired with anti-parallel diodes, alongside a DC link capacitor of substantial capacity. It has a self-supporting DC voltage bus with a large DC capacitor. It is more widely used because it is lighter, cheaper, and expandable to multilevel and multi-step versions to enhance the performance with lower switching frequencies.

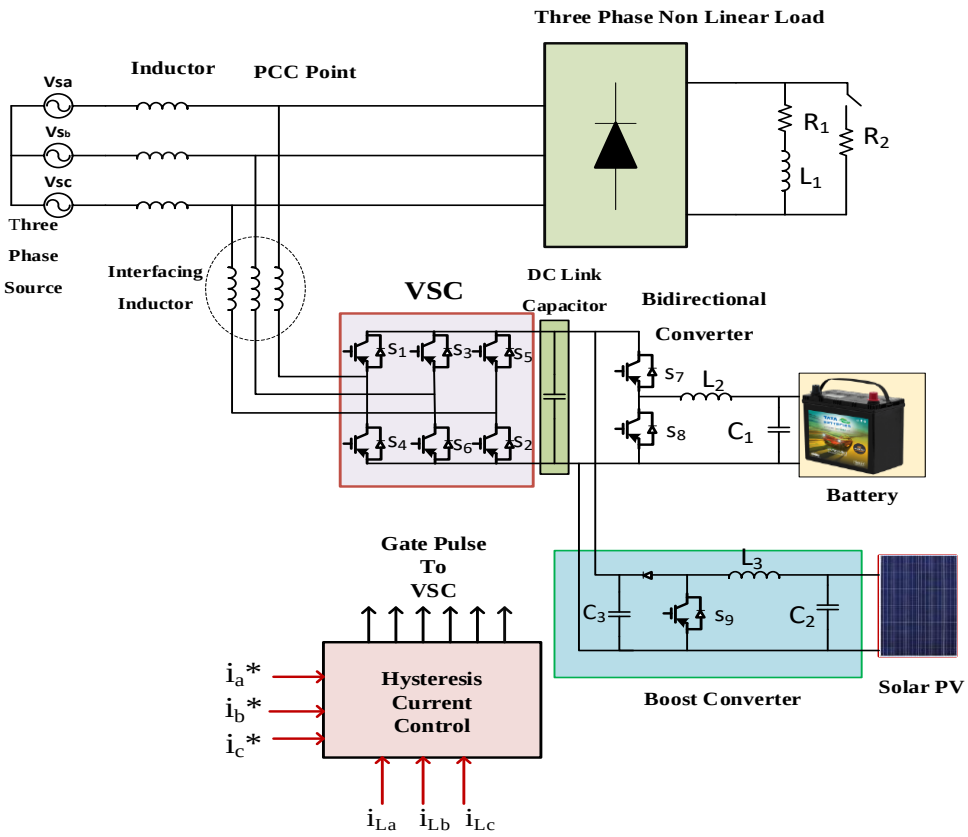

Fig.3. 1 System Configuration Model

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The source impedance links the three-phase supply to the load. Interfacing inductors are used to minimize the ripples in compensating current. Non-linear load is implemented using six diodes in a bridge configuration as an uncontrolled rectifier, on the DC side load resistance and inductance are connected.

A boost converter is attached to the PV system, facilitating integration with the STF. The boost converter with the help of MPPT (P&O) algorithm helps in extracting the maximum power from the PV array. PV voltage and current are measured for maximum power extraction. The STF is used in mitigating power quality problems with the help of suitable control algorithms and this is discussed in successive chapters. The DC link voltage is controlled with the help of a PI controller. The specification of interfacing inductors, boost converter and PV array are determined in subsequent sections.

3.2 Design Aspects of Shunt Compensator System

The next section discusses the design specifics of the several SAPF integrated system parameters. Calculations for DC link voltage and DC link capacitance are included in this section. Fig. 3.1 shows the schematic block diagram of a battery-interfaced PV integrated grid-connected system with an interacting inductor. Both single-phase and three-phase system designs are covered.

3.2.1 Design of Three-Phase systems

Here are the selection criteria for the aforementioned parameters in a Three-phase system.

3.2.2 Calculation of DC Link Voltage

The voltage at DC link should be sufficient enough to compensate for the switching losses happening in the IGBT switches. For proper PWM control, the system should have greater DC link voltage than the peak value of line-to-line supply voltage in the three-phase system. The peak value is given as:

$$V_m = \frac{\sqrt{2}V_{LL}}{\sqrt{3}} \tag{3.1}$$

Where V_m is the peak value of AC terminal voltage and V_{LL} refers to line to line rms AC Voltage

Therefore, the DC bus voltage (VDC) is defined as

$$V_{DC} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{3.2}$$

where m is the modulation index and is considered as 1 and V_{LL} is the AC line output voltage of grid taken as 110V. On substituting value of DC bus voltage is obtained as

$$V_{DC} = \frac{2\sqrt{2}\times 110}{\sqrt{3}} = 179.6V \tag{3.3}$$

Thus, the DC link voltage (V_{DC}) is calculated as 179.60V and the reference is taken as 200V.

3.2.3 DC Link Capacitor

The logic behind the design of the DC capacitor is governed by the reduction in the DC bus voltage upon the application of the load and rise in the DC bus voltage on removing the load. Using the principle of conservation of energy, the equation for C_{DC} is

$$0.5C_{DC}[(V_{DC2}^2) - (V_{DC1}^2)] = k[3V_{ph}\alpha It] \tag{3.4}$$

$$C_{DC} = \frac{k[3V_{ph}\alpha It]}{0.5[(V_{DC2}^2) - (V_{DC1}^2)]} \tag{3.5}$$

where V_{DC1} is the reference DC voltage and V_{DC2} is the minimum voltage level of the DC bus, α is the overloading factor,V_{ph} is the phase voltage, κ is gain constant, I is the phase current of the VSC, and t is the time by which the DC bus voltage is to be recovered. Considering $V_{DC2} = 200V$, $V_{DC1} = 179.60V$, α = 1.2, V_{ph} = 89.5V, 'κ' = 0.05, I_{ph} = 25A, t = 0.02s. We get $C_{DC} = 2081uF$. Therefore, the chosen value of $C_{DC} = 3000uF$.

3.2.4 Interfacing Inductor

The compensating current generated by the STF contains ripples, to filter out these ripples we use interfacing inductors. Also, it should be made sure that the voltage drop across the inductors is not too high which may affect the normal operation of STF. The value for interfacing inductor is calculated with the help of this formula

$$L_f = \frac{\sqrt{3}mV_{DC}}{12\alpha f_s I_{crpp}} \tag{3.6}$$

considering 'α'=1.2, switching frequency $f_s = 10KHz$, modulation index (m) = 1, DC bus voltage $V_{DC2} = 200V$, current ripple $I_{crpp} = 2.5\ A$, the value of interfacing inductor L_f is calculated as

$$L_f = \frac{\sqrt{3}\times1\times200}{12\times1.2\times10\times10^3\times2.5} = 0.962mH \tag{3.7}$$

rounding the obtained value to 1mH is used in simulation setup.

3.2.5 Selection of Non-Linear Load

A MATLAB/SIMULINK environment is used to mimic the setup that was explained. A resistor and an inductor coupled in series with a load rating of 25V, 30A are used for linear loads. Using a diode bridge rectifier, non-linear loads are linked. The system's load current

and PF can be adjusted to suit needs by altering the load impedance. The diode bridge rectifier's DC side features a fixed inductor of 40mH and a variable resistor load (20-80Ω).

3.2.6 Selection of Solar PV Array

Table 1 Solar Panel Properties

Attribute	**Specification**
Model name	Kyocera Solar KD250GX-LFB2
Maximum Power (P_{mp})	634.5 W
Open Circuit Voltage (V_{oc})	36.3 V
Short Circuit Current (I_{sc})	7.84 A
Voltage at Maximum Power (V_{mp})	29 V
Current at Maximum Power (I_{mp})	7.35 A
Modules Connected in Series per String	3
String Connected in Parallel	1
Voltage temperature coefficient (%/C)	-0.334
Current temperature coefficient(%/C)	0.048

PV module of Kyocera Solar KD250GX-LFB2 available in the SIMULINK library has been used with the below specifications:

3.2.7 Design Inductor and Capacitor for BOOST Converter

$$L_b = \frac{D \times V_{mp}}{\Delta I_{pv} \times f_{sw}} = \frac{0.5 \times 29}{0.291 \times 10 \times 10^3} = 4.98mH \quad (3.8)$$

Lb is calculated as 4.95mH and taken as 5mH, where D is the duty cycle, V_{mp} is the voltage at maximum power, ΔI_{pv} is the ripple in inductor current, fsw is the switching frequency of IGBT.

$$C_b = \frac{D \times I_{out}}{\Delta V_{out} \times f_{sw}} = \frac{0.5 \times 10}{20 \times 10 \times 10^3} = 100uF \quad (3.9)$$

C_b is the calculated as 100μF and taken as 150μF, where D is the duty cycle, I_{out} is the output current, ΔV_{out} is ripple in boost output voltage i.e 10% of the output voltage V_{out} which is 200V.

3.2.8 Design specifications of Battery

The design specifications for battery integrated system described. Here the Lead Acid Battery of 154V,20Ah is taken as the battery capacity, Initial state of charge=31%.

A bidirectional converter operation is designed. In buck mode, the inductor filter design is carried out as

$$D = \frac{V_{batt}}{V_{dc}} = \frac{154}{200} = 0.77 \quad (3.10)$$

$$L_b = \frac{D \times (V_{DC} - V_{batt})}{\Delta I_L \times f_{sw}} = \frac{0.77 \times (200 - 154)}{0.1 \times 7 \times 10 \times 10^3} = 8.36mH \quad (3.11)$$

In Boost mode

$$D = \frac{V_{DC} - V_{batt}}{V_{dc}} = \frac{200 - 154}{200} = 0.23 \quad (3.12)$$

$$L_b = \frac{(D \times V_{batt})}{\Delta I_L \times f_{sw}} = \frac{0.23 \times (154)}{0.1 \times 7 \times 10 \times 10^3} = 5.06mH \quad (3.13)$$

Therefore, the required value of inductor chosen is 10 mH. Here V_{batt} is the battery voltage, V_{DC} is the DC Link voltage and ΔIL is the charging current which is considered as 20% of fsw where fsw is the frequency of switching which is considered as 10kHz.

CHAPTER 4

DESIGN AND ANALYSIS OF CONTROL ALGORITHEMS OF POWER QUALITY ISSUE IN THREE PHASE GRID CONNECTED PHOTOVOLTIC AND BATTERY CHARGING SYSTEM

4.0 General

This article presents the development of a strategy based on the Self Tuning Filter algorithm estimating the active power signals of load current. The technique is formulated by extracting the fundamental component which is free from harmonics. The Self Tunning Filter (STF) algorithm produces a reference current signal to regulate the VSC, which controls the PCC voltage, current in an integrated PV-grid system and consist of a battery. Estimating the reference current is necessary for regulating the Voltage Source Converter (VSC) in a Photovoltaic (PV)-grid system. The hysteresis PWM controller block processes the difference between the estimated and measured AC currents(i_{sabc}) to generate gate pulses for the IGBTs. These gate pulses are used for the switching operation of the VSC, which in turn removes the current-based power quality problems in integrated PV-grid systems

4.1 Control Strategy

4.1.1 Mathematical Analysis of Control Strategy of STF

Strategy for mathematical control, there are Three processes are involved in PV- STF operation: (i) MPPT control and (ii) VSC switching control (iii) Battery charging discharging (V2G & G2V). To get the most power out of the PV array, MPPT control is

utilised. Estimating the fundamental load component, DC link voltage regulation and switching losses, PV-feedforward component, unit template estimation, and reference current generation are all part of VSC switching control. In the sections and chapters that follow, several controllers have been created and examined.

4.1.2 Synchronous Reference Frame Theory (SRFT)

The SRFT controller is implemented utilizing source voltage (V_s), source current (i_s),, load current (i_L),, and DC link voltage(V_{dc}), as input parameters. The SRFT controller necessitates the conversion of voltage and current data from a single-phase system into d-q components. Therefore, the initial conversion to the $\alpha\beta$ frame of reference is executed. A secondary pseudo phase is generated by introducing a 90° lag to the original signal. Consequently, the measured grid-connected current and voltage are acquired in the α frame. The signals in the β frame is produced by moving the matching signal by 90 degrees. The load current in the $\alpha\beta$ frame is denoted by the aforementioned approach.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_L(\omega t + \varphi) \\ i_L(\omega t + \varphi + \frac{\pi}{2}) \end{bmatrix} \tag{4.1}$$

The stationary frame $i_{L\alpha}$ and $i_{L\beta}$ is converted to the synchronously rotating frame i_{Ld} and i_{Lq} using the Park transformation matrix.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -cos(\omega t) \\ cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_{L\alpha}.\sin(\omega t) - i_{L\beta}cos(\omega t) \\ i_{L\alpha}cos(\omega t) + i_{L\beta}.\sin(\omega t) \end{bmatrix} \tag{4.2}$$

SRFT PLL is employed to synchronize signals and produce unit-in-phase $\sin(\omega t)$ and unit-in-quadrature $cos(\omega t)$templates.

The measured currents (i_{Ld}, i_{Lq}) exhibit significant harmonics that require elimination. The $\overline{i_{Ld}}$ represents the filtered fundamental component of load current. The presenti_{Ld} is partitioned into fundamental and harmonic active components of load current, whereas i_{Lq} is divided into fundamental reactive and harmonic components.

$$i_{Ld} = \overline{i_{Ld}} + \widetilde{i_{Ld}}, i_{Lq} = \overline{i_{Lq}} + \widetilde{i_{Lq}} \tag{4.3}$$

AC components are removed using High Pass Filters, whereas DC components are extracted using Low Pass Filters. The controller is engineered to ensure that the source current comprises solely the fundamental estimated active component of load current while the load harmonics and reactive current component are provided by the Shunt Active Power Filter, hence allowing the $i_{Lq}{}^{*}$ component to be set to zero. The reference source current is produced by taking the inverse Park Transformation

4.2.2 MPPT Algorithm

One well-known method for Maximum Power Point Tracking (MPPT) in photovoltaic (PV) systems is the Perturb and Observe (P&O) algorithm, which is used to collect as much power as possible from the solar panels. For the next iteration, we measure the voltage (V) and current (I) to calculate the power (P = V × I) after first providing a reference value for panel voltage and power. The new power output is computed following a little disturbance to the voltage or current. The perturbation continues in the same direction if the power rises ($P_{new} > P_{old}$), if the power falls, the direction of the perturbation reverses. The PV system's operating point converges towards the Maximum Power Point (MPP) with the aid of this iterative process. The algorithm's simplicity and

convenience of use make it popular. It may, however, be slow to react to abrupt changes in the environment and occasionally move in the wrong direction, causing oscillations about the MPP. The P&O algorithm is nevertheless a mainstay in PV system optimisation in spite of these limitations. In general, the characteristic curve in Figure 4.1 can be explained as follows:

• $\frac{\delta P}{\delta V} > 0$ and $V < V_{mp}$ i.e left side of MPP.

• if • $\frac{\delta P}{\delta V} = 0$ and $V = V_{mp}$ i.e at MPP.

• if • $\frac{\delta P}{\delta V} < 0$ and $V > V_{mp}$ i.e Right side of MPP.

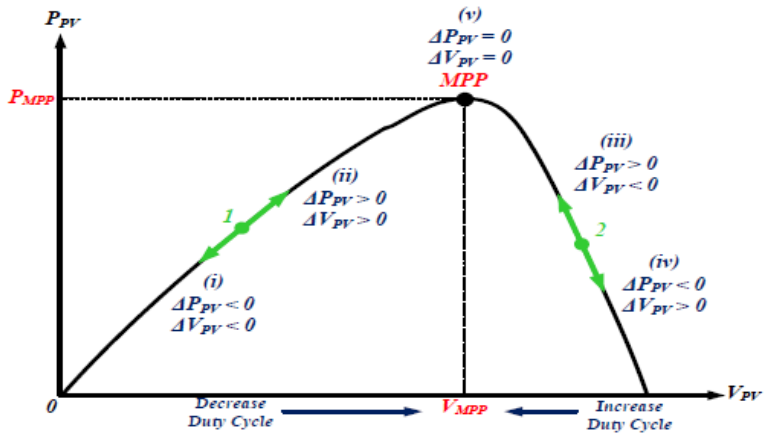


Fig.4. 1 Maximum Power Curve

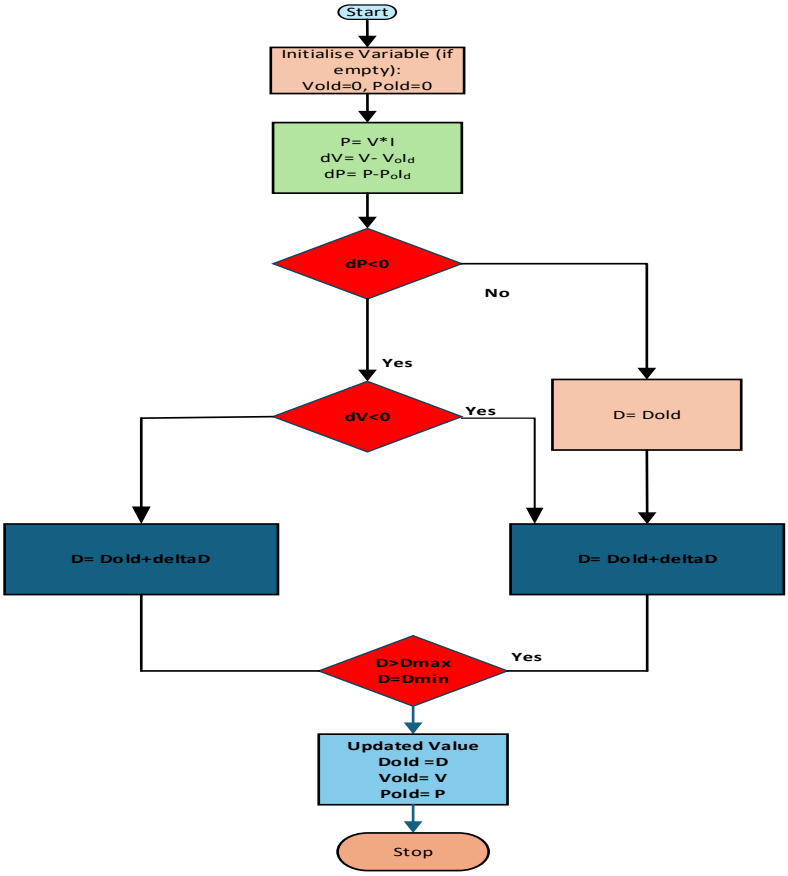


Fig.4. 2 Flow Chart of MPPT

This version of the P&O method, which is contained in the Appendix, provides a reference voltage value that is compared to the measured panel voltage (VPV). The difference between the two serves as an error signal, which is then sent to the PI controller. The necessary duty ratio for PWM generation is obtained from the PI controller's output, which is compared to a carrier signal before being sent to the IBGT's gate terminal. Because it includes a closed loop control mechanism, this method will provide higher MPP tracking performance than the one where we produce duty cycle. An MPPT with a P and O basis optimises the solar array's power output under uncertain PV circumstances. The duty ratio

is compared to the sawtooth wave, and the boost converter's switching pulses are produced, as seen in Fig 4.2.

According to estimates, the PV feed forward

$$i_{pv\_eff} = \frac{2 \times P_{pv}}{3V_t} \tag{4.4}$$

4.3 VSC Switching Algorithm

Depending on whether the system is single phase or three phase, different algorithms have different designs. In single-phase and three-phase systems, respectively, four and six switching pulses are produced. Generally speaking, both systems' controller designs include the following standard procedures:

(i) Estimation of Fundamental Load current

The algorithm is intended to extract the distorted basic component of the load current. The techniques that extract the essential component of the load current for three-phase systems are Synchronous Reference Frame Theory (SRFT), Self-Tunning Filter (STF) Legendre Functional Neural Network (LFNN), Trigonometric Functional Link Neural Network (TFLNN), and Second Order Generalised Integrator (SOGI).

(ii) DC Link Voltage Regulation and Estimation of Switching Losses

For STF to operate, the DC Link voltage must be controlled. A PI controller is used to control the DC Link voltage. The PI controller receives the error, which is the difference between the reference DC link voltage (V_{DC}^{*}) and the measured DC link voltage (V_{DC}). In order to maintain the DC Link voltage and make up for switching losses occurring in the STF, the difference provides the $iLoss$ component that is taken from the grid.

$$vde(n) = V_{DC}^{*} - V_{DC} \tag{4.5}$$

$$i_{eff} = i_{loss} + i_{lfil} - i_{PVeff} - i_{batt\_eff} \quad (4.6)$$

4.3.1 Mathematical Analysis of Control in Three-Phase Grid Connected System

Below is a discussion of how to calculate the PV feedforward component and generate reference source current in Three-phase grid-connected systems.

4.3.2 Self-Tunning Filter Controller (STF)

Self-tuning filters take out the basic component of an input signal by feeding the output back into the input signal. In this case, the α and β components of i_{alpha} and i_{beta}.

$$i_{l\alpha fil} = \left(\frac{K \times i_{\alpha} - K \times i_{l\alpha fil}}{S}\right) - \left(\frac{\omega \times i_{l\beta fil}}{S}\right) \quad (4.7)$$

$$i_{l\beta fil} = \left(\frac{K \times i_{l\beta} - K \times i_{l\beta fil}}{S}\right) - \left(\frac{\omega \times i_{l\alpha fil}}{S}\right) \quad (4.8)$$

i_{alpha} and i_{beta} are distorted due to the linked nonlinear loads. Therefore, to obtain filtered

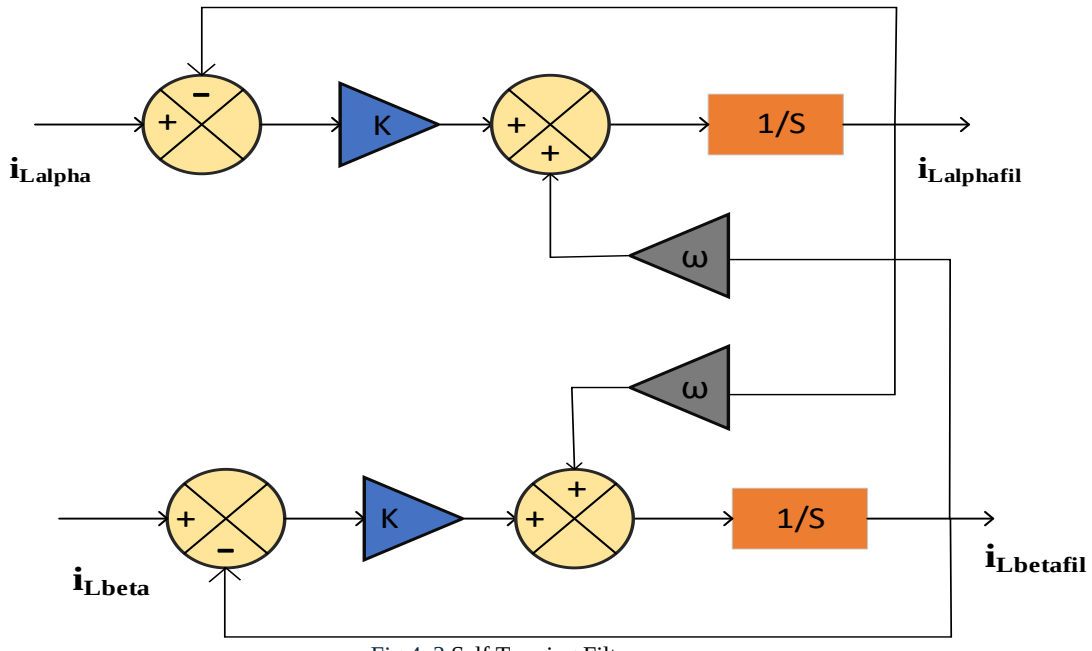


Fig.4. 3 Self Tunning Filter

and distortion-free values for the α and β components of load currents, a self-tuning filter is needed as shown in Fig.4.3 Clark's transformation can be used to extract the α and β details of load currents.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4.9}$$

A fundamental part of load current can be calculated as

$$\mathrm{i_{lfil}} = \sqrt{\mathrm{i}^2_{\mathrm{l}\alpha\mathrm{fil}} + \mathrm{i}^2_{\mathrm{l}\beta\mathrm{fil}}} \tag{4.10}$$

Under weak grid circumstances, the unit template approach utilized in is unreliable. Phase-locked loop (PLL) technology is the method of choice in non-ideal situations. Phase-locked loops are commonly used to synchronize and track parameters like frequency and phase angle.

(i) Calculation of PV Feedforward Component

The purpose of the PV feedforward component is to minimise grid voltage and current oscillations caused by changes in PV insolation while accounting for the contribution from the PV array. The feedforward element is interpreted as

$$i_{pv\_eff} = \frac{2 \times P_{pv}}{3V_t} \tag{4.11}$$

where Ppv is the maximum power, Vt is the peak amplitude of grid voltage.

(ii) Estimation of Unit Templates for Three-Phase Systems

The values of V_{Sa}, V_{sb}, V_{sc} represent the three-phase supply voltages at the point of

common coupling. These voltages' magnitude is determined using the formula Vt, represented in

$$V_t = \sqrt{\frac{2}{3}(v_a^2 + v_b^2 + v_c^2)} \tag{4.12}$$

Unit templates for Three phases are calculated as

$$u_{ia} = \frac{v_a}{V_t},\ u_{ib} = \frac{v_b}{V_t},\ u_{ic} = \frac{v_c}{V_t} \tag{4.13}$$

3.3.6 BSE Control

The DC-link voltage is expected to remain constant during the dynamics at Vdc*. The reference current of battery generated using a PI controller by sending the error obtained

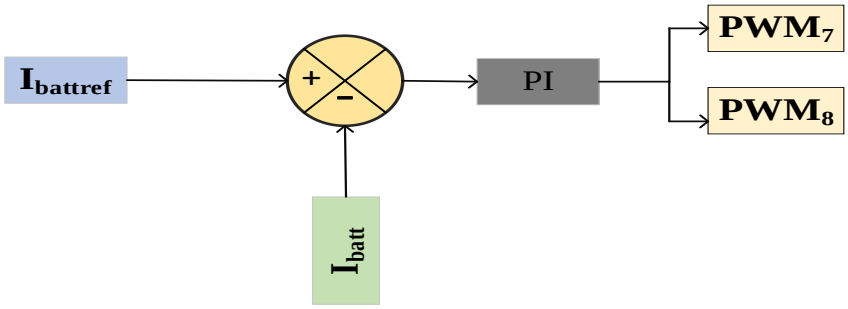


Fig.4. 4 Battery control algorithm

by subtracting the measured DC link voltage from Vdc*. Following that, the reference current of battery is compared to the battery current and provided to the PI controller, which uses it to generate the gating pulses of the bidirectional converter, as shown in Fig.4 According to estimates, the Battery feed-forward component is

$$i_{batt\_eff} = \frac{2 \times V_{batt} \times I_{batt}}{3V_t} \tag{4.14}$$

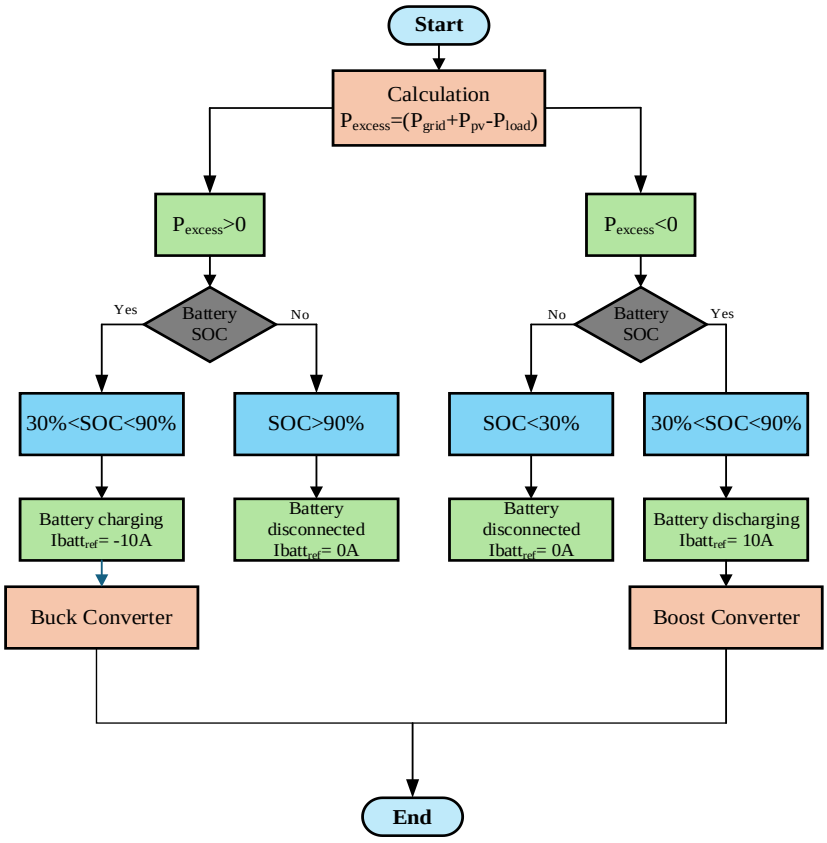


Fig.4. 5 Battery charging/discharging Algorithm

Compute the excess power first, represented by P_{excess}. If there is more power than zero and the battery is charged at a constant current of 10A while the state of charge is between 30% and 90% To avoid overcharging, stop charging the battery if the SOC is greater than 90% and the P_{excess} is also greater than zero. Battery discharge with constant current of 10A if excess power is less than zero and the state of charge is between 30% and 90%. To avoid a deep discharge, cease charging the battery if the SOC is less than 30% and the P_{excess} is also less than zero shown in fig.4.6.

4.4 The Reference Grid Current Calculation

The total amount of fundamental in-phase current that must be drawn from the grid is as the following:

$$i_{eff} = i_{loss} + i_{lfil} - i_{PVeff} - i_{batt\_eff} \quad (4.15)$$

Where i_{lfil} is the estimated fundamental component of the load current, i_{loss} is the loss component described in this section shown in fig.6, i_{PVeff} is the PV feed forward component and i_{batt_eff} is the battery feed forward component.

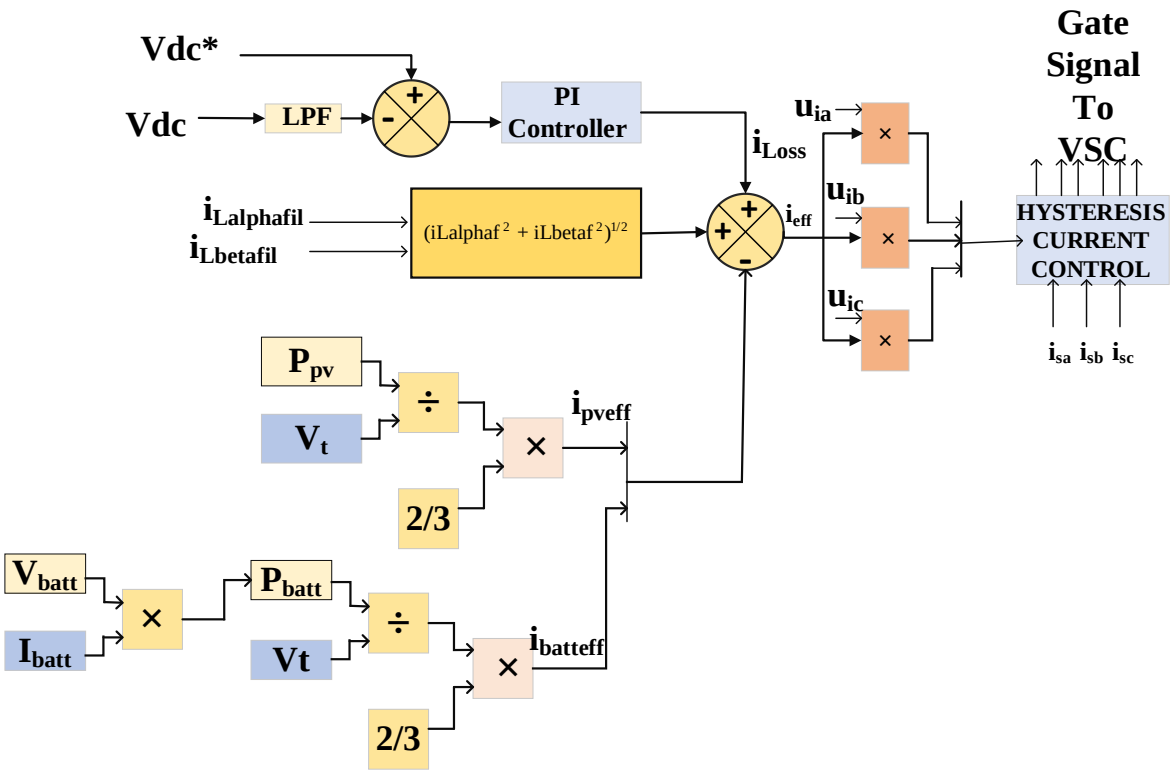


Fig.4. 6 Gate signal generation for Inverter

The final reference currents are calculated as:

$$i_{saref} = I_{eff} * u_{ia},$$
$$i_{sbref} = I_{eff} * u_{ib}, \quad (4.16)$$
$$i_{scref} = I_{eff} * u_{ic}$$

4.5 Simulation Results

STF is compatible with Phase Locked Loop (PLL) and Shunt Active Pass Filter. STF creates the essential component needed for compensation under typical grid conditions, whereas PLL is used when disturbances such as phase shifts, frequency changes, voltage sags, or swelling cause the grid to become weaker.

In this MATLAB Simulink model, Power Quality enhancement is examined in conjunction with analysis conducted under the Renewable + Grid to battery (R+G)2V mode and Renewable + battery to Grid (R+V)2G. As shown in Fig.4.7(b), the battery was charged by the grid and renewable energy sources, and after 0.6s, the load demand increased above the capacity of the grid, which was then met by the battery and renewable energy sources which is shown in Fig.4.8.

4.5.1 (R+G)2V Mode

In this mode, additional connected electric loads to the system receive power injection from the solar PV system. The EV battery is charged using the residual power, or excess power, which is sum of power generated by the PV (P_{pv}) and Grid power (P_{grid}) minus power consumed by the load (P_{Load}). The solar PV power is used to power the grid and EV batteries for 0.6s. The state of charge (SOC) of the battery rises and reaches about 30.103%.

It then rises until it reaches 90%, at which point it will halt to avoid. Which is shown in Fig.4.7.

4.5.2 (R+V)2G Mode

In order to meet the load demand, the system switches to a mode where energy is now

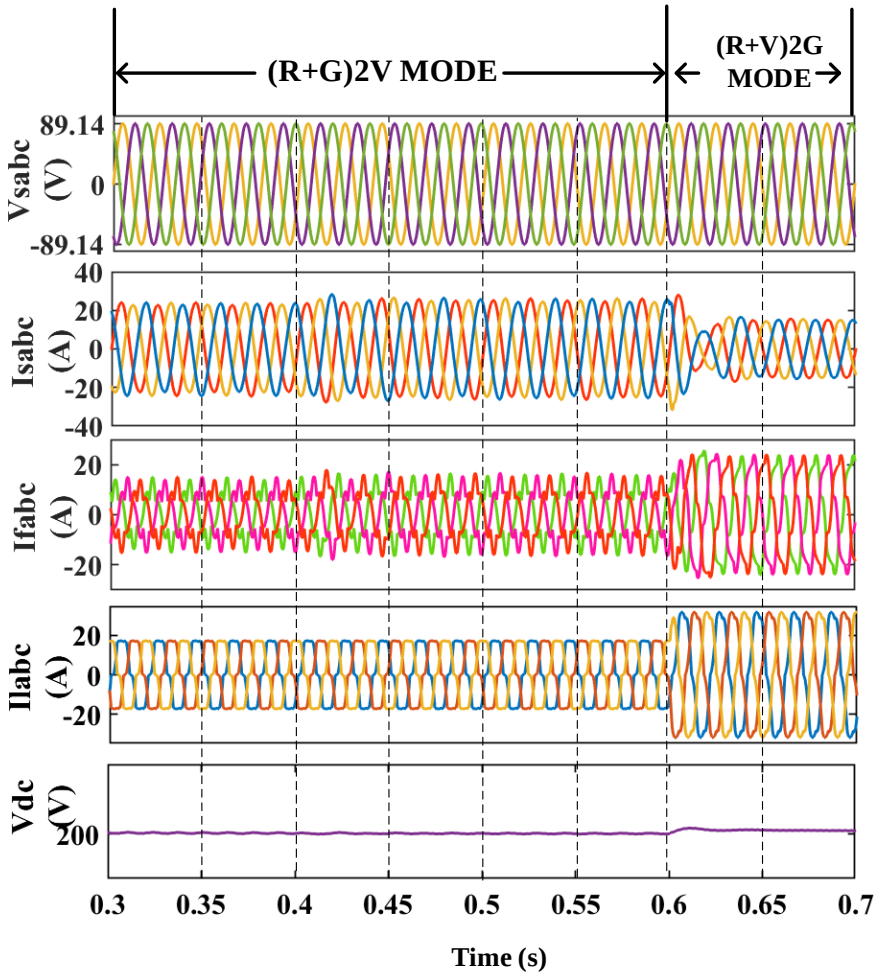


Fig.4. 7 Steady state waveforms of source voltage (v_{sabc}), source current (i_{sabc}), load current (i_{labc}), compensator current (i_{fabc}) and DC Link voltage (V_{dc}) under non-linear load conditions

transferred by the battery for discharge. Consequently, the battery's State of Charge starts to drop at 0.9 s, going from 30.103% to 30.001%. To save the battery from completely

draining, the battery will cease to discharge when the SOC hits precisely 30% as shown in Fig. 4.8.

4.6 Performance Under Changing Solar Irradiation

Under normal grid conditions, without the PV panels, a source current of 15A is used to match a load current of 15 A. The PV array delivers a maximum power of 680 W at 1000W/m2. Using MPPT, an active power of 639.45 W is supplied at the DC link. Performance analysis for the grid-tied PV system under changing irradiation is done in two distinct scenarios.

4.6.1 Irradiation change from $1000\ w/m^2$ to $500\ w/m^2$

See Fig.8 between 0 s and 0.4 s, when the solar irradiation is at $1000\ w/m^2$, the source current decreases to 23.2 A to fulfil the load current and charging current of the battery both, as it is shared by both PV and source currents. The load power of 2.727 kW is partially supplied by the source power of 2.047 kW and PV power of 0.680 kW. The source current increases to 25 A to match the load demand as the solar irradiation drops to 500W/m2 at t = 0.55 s. Consequently, the PV current decreases while the grid current increases proportionally to satisfy the load demand and battery charging current 35 A. The PV power decreases to 0.325 kW, and the source power increases to 2.402 kW to meet the total load power of 2.727 kW. The DC-link voltage VDC decreases and stabilizes at the desired value of 200V through the action of the PI controller.

4.6.2 Zero Irradiation

when PV array becomes inactive, it generates zero power because the irradiance is zero as well as shown in Fig.4.8. Now, the source and Battery completes load power requirement. When solar irradiation decreases to zero.

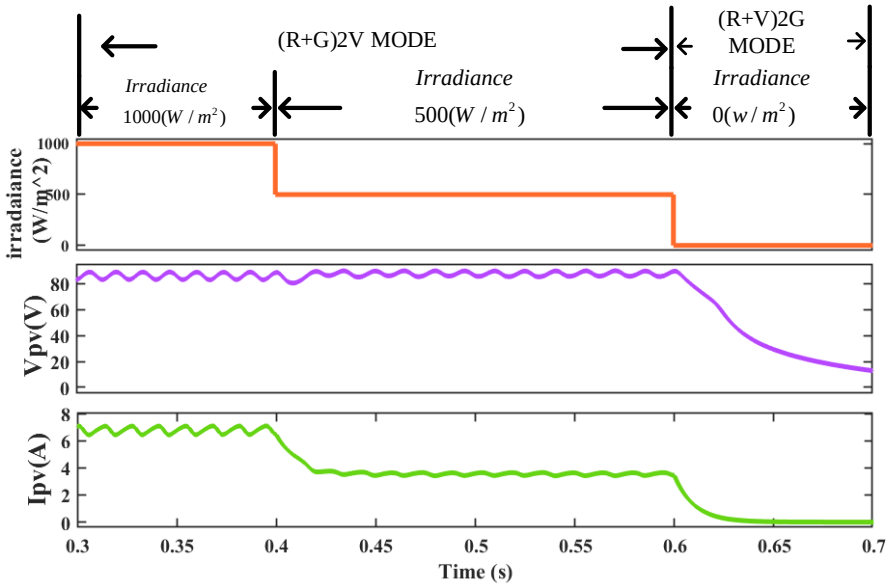


Fig.4. 8 Irradiance, Solar PV voltage (V_{pv}) and Solar PV current (I_{pv})

4.7 Performance of Battery

Fig illustrates the waveforms of SOC (%), Battery Current, battery voltage, and PV current, respectively. Here, the battery starts charging, increasing its state of charge (SOC) from 30.1001% to 30.103%. Also, the Battery voltage starts increasing from 150.6V. The battery starts charging with a current of 10A. The battery discharges when the photovoltaic (PV) current gets below 10 A, decreasing its state of charge (SOC) from 30.103%. to 30.102%. Also, Battery voltage increases from 150.6V to 146V.

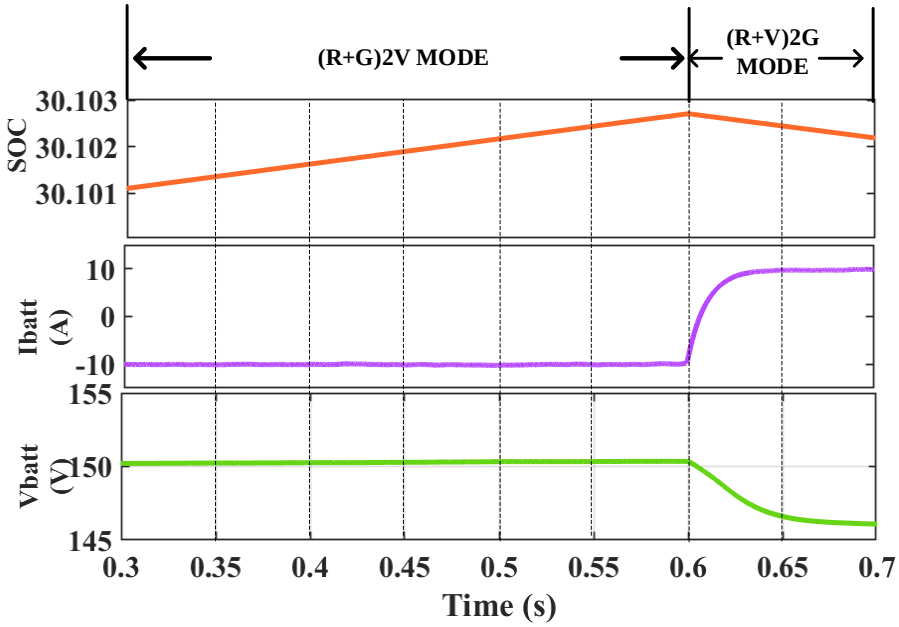


Fig.4. 9 State of charge (SOC), battery current (i_{batt}), battery voltage (v_{batt})

4.5 Power Balance of The System During Steady State Condition

These waveforms are illustrated in Fig.10 The photovoltaic (PV) array has a power output of 680 W when exposed to an irradiance of 1000 w/m^2. However, it is now injecting 639.45 W into the DC link. During 0.5s to 0.6s, the entire power load of 2.272 kW is supplied solely by the source and the photovoltaic (PV) source is linked. At solar irradiation levels of 1000 w/m^2, the load power of 2.25 kW is partially supplied by a source power of 1.800 kW and a PV power of 0.634 kW, with a time interval ranging from 0.128 s to 0.4 s. During the time interval from 0.4 s to 0.6 s, the solar irradiation decreases

to 500 w/m^2. As a result, the power generated by the photovoltaic (PV) system decreases to 0.325 kW. To compensate for this reduction and satisfy the total load power of 2.727 kW, the power from the external source increases to 2.402 kW. Fig.4.10 also shows that

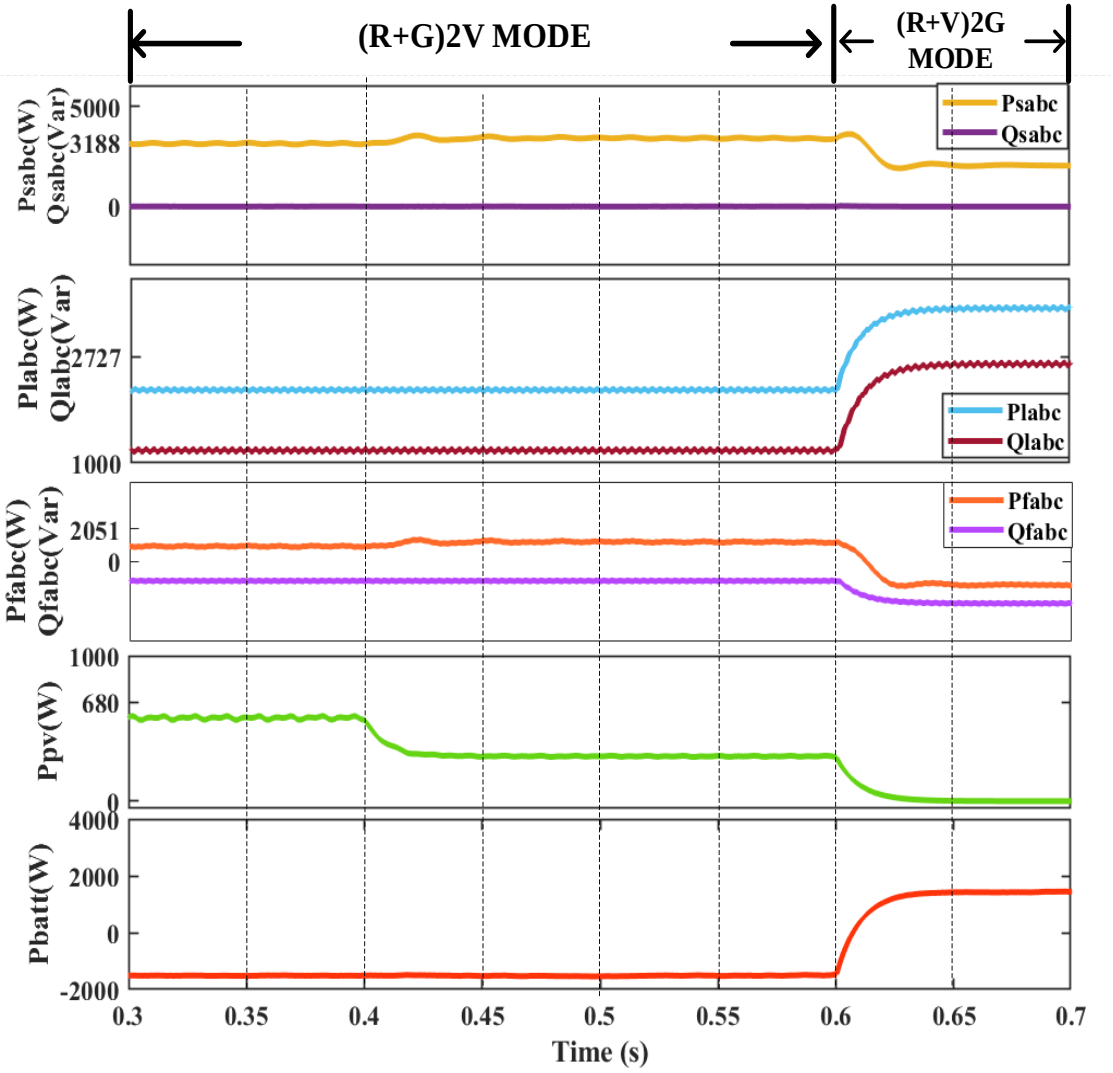


Fig.4. 10 Source Power (P_{sabc}), load Power (P_{labc}), compensator Power (P_{fabc}), $Solar\ Power(P_{pv})$ battery Power (P_{batt})

with changing irradiance, the power output of the PV system also varies according to load

demand. The load demand of reactive power is supplied by the compensator and absorbed by the non-linear load. The source does not absorb any desired reactive power.

4.6 THD (Total Harmonic Distortion)

It has been noted that the load current THD of 22.89% in Fig.4.11(c) has improved source current THD to 2.52% in Fig.4.11(b). In order to meet IEEE-519 standards, the inverter

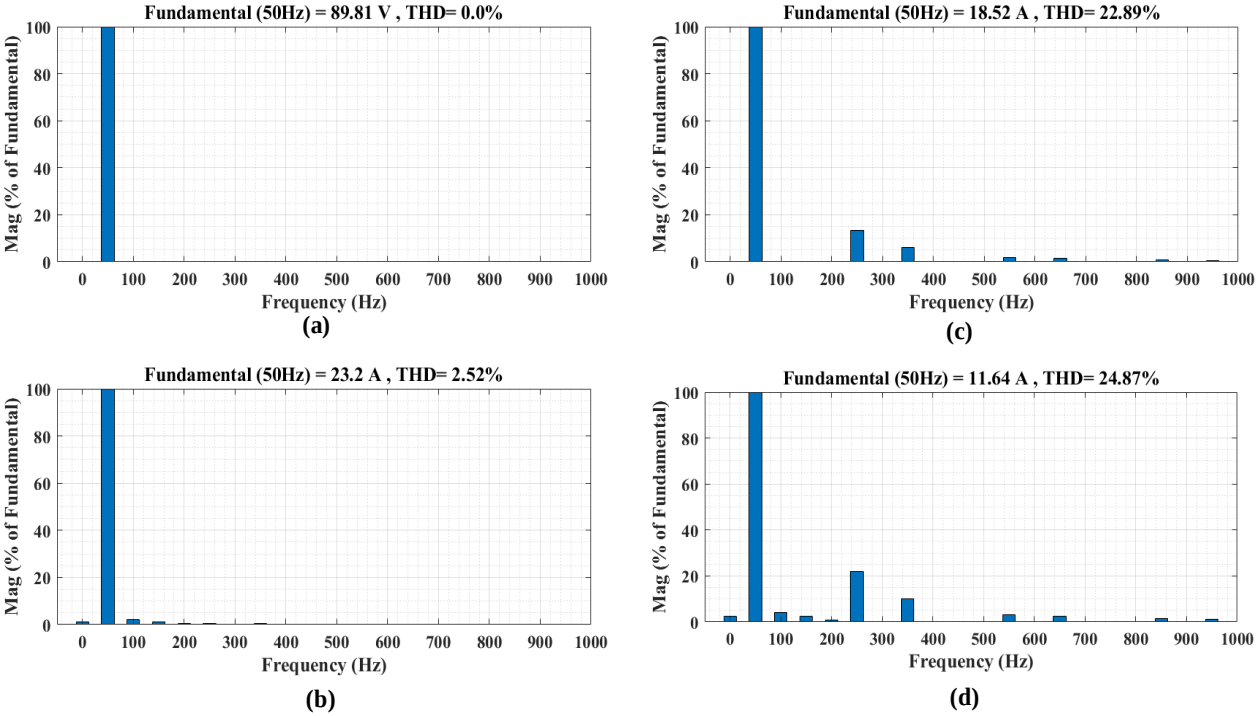


Fig.4. 11(a) THD of source voltage (v_{sabc}) (b) THD of source current (i_{sabc}) (c) THD of load current (i_{labc}) (d) THD of compensating current (i_{fabc})

sent a compensating current with a THD of 24.87%, which eliminated the harmonics in the load current and improved the source current's THD below 5%

4.7 Comparative Analysis with Other Conventional Algorithms

The This approach outperforms traditional techniques for extracting fundamental components. The weight convergence comparison between STF and one traditional algorithm makes this evident. The primary component extracted from the load current is weight convergence. To demonstrate the method's superiority, weight convergence with various controllers is carried out under varying load conditions and dynamics. This is accomplished by estimating the fundamental weight of the load current using the suggested STF algorithm and contrasting it with the traditional time domain method, the SRFT algorithm. A thorough comparison has been conducted based on a number of

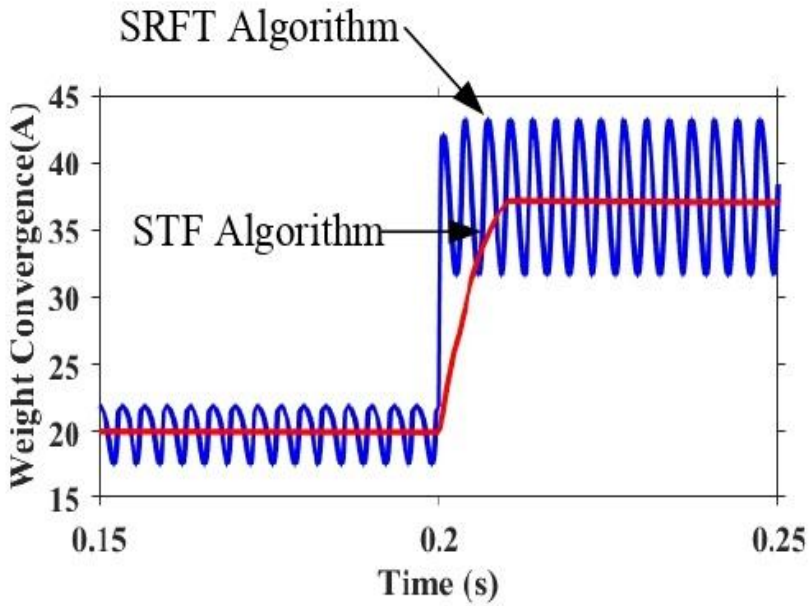


Fig.4. 12 Comparison analysis of weight convergence of different algorithm

parameters, including algorithm type, implementation complexity, THD in source current, settling and sampling times, oscillation, and overshoot. Table 2 contains a compilation of these findings

Table 2 Performance Analysis of proposed algorithm comparison with other conventional technique

Parameter	STF	SRFT
Complexity in Implementation	Less	More
THD in grid current	2.52%	4.51%
Settling time	Moderate	Fast
PLL Requirement	No	Yes
Sampling Time	40us	70us
Oscillation	Almost negligible	Very high

Additionally, Fig.4.12 compares weights using two distinct techniques. It is discovered that

SRFT has the fastest weight convergence, whereas STF moderate has almost no oscillations and overshoot when detecting changes in load and accomplishes.

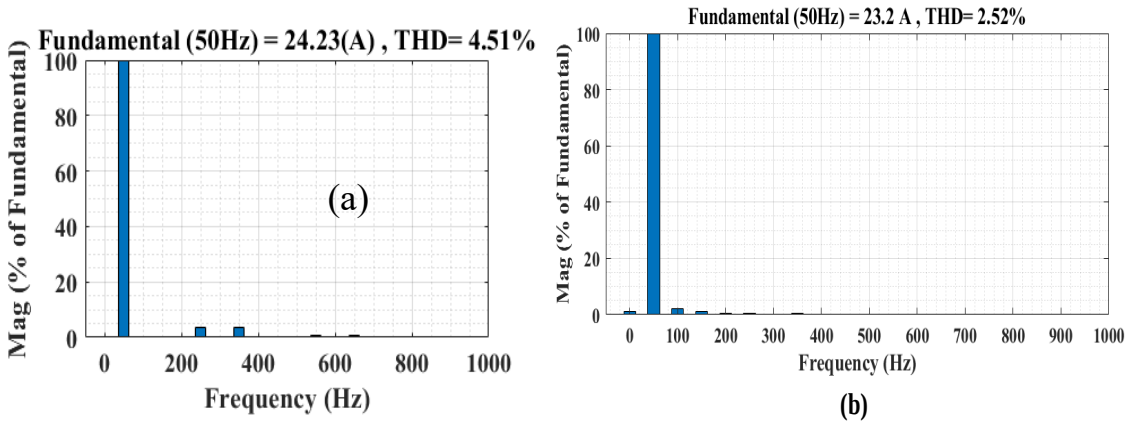


Fig.4. 13 THD of source current of SRFT ($i_{sabc\prime}$) (b) THD of source current of STF (i_{sabc})

CHAPTER 5

DESIGN AND ANALYSIS OF PFC- INTERLEAVED TOTEM-POLE CONVERTER -FED FULL BRIDGE LLC RESONANT CONVERTER

5.0 General

The investigation of innovative power converter topologies has been prompted by the increasing need for small and effective power conversion devices, especially in applications using renewable energy and electric car charging. The design and thorough analysis of an interleaved totem-pole converter based on power factor correction (PFC) combined with a full-bridge LLC resonant converter are presented in this study. In order to provide a high-performance AC-DC power conversion solution, the suggested architecture combines the soft-switching advantages of the LLC topology with the high efficiency and near-unity power factor capabilities of the interleaved totem-pole PFC stage. The design restrictions, control strategies, component selection, and operating principles of both converter stages are thoroughly examined. While the LLC resonant stage guarantees effective voltage regulation under a range of load situations, the interleaved PFC totem-pole stage reduces input current ripple and improves thermal performance. In order to ensure smooth power delivery with low switching losses and enhanced electromagnetic compatibility, the integration of these two stages is examined.

5.1 System Configuration and operation principle

The system is a high-efficiency battery charger that consists of a resonant LLC DC-DC

converter after an interleaved totem-pole PFC stage. Before being fed into the interleaved totem-pole PFC, which uses two parallel legs of MOSFETs and diodes to convert AC to high-voltage DC while keeping a power factor close to unity, the AC input is first filtered and shaped using inductors and EMI components. A high-frequency inverter transforms

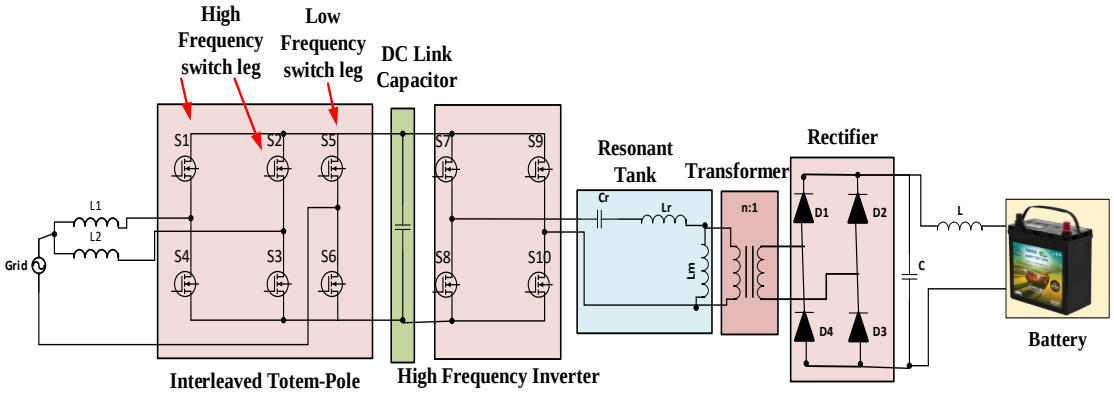


Fig.5. 1Charger system configuration

this DC into high-frequency AC for the LLC resonant tank after smoothing it with a DC-link capacitor. Soft-switching operation is made possible by the LLC tank, which is made up of inductors and a capacitor. This lowers losses and increases efficiency. For high-efficiency DC conversion, this high-frequency AC is rectified using synchronous rectifiers after being routed through an isolated transformer for voltage stepping shown in fig.5.1. Lastly, the battery is charged using the controlled DC output, with the proper voltage and current management according to the battery's specifications.

5.1.1 Interleaved Totem-pole PFC

The interleaved totem-pole bridgeless power factor correction (PFC) circuit is an efficient AC-DC conversion method commonly employed in contemporary power electronics applications, including electric vehicle chargers, data centres, and renewable energy

systems. This topology employs active switches instead of diode bridges, hence minimizing conduction losses and enhancing overall performance, in contrast to conventional PFC circuits. The term "totem-pole" denotes the configuration of switches in a vertical alignment, whilst "bridgeless" indicates the removal of the traditional full-bridge diode rectifier.

In a conventional AC-DC rectifier, the input current traverses a full-bridge rectifier composed of four diodes. This configuration, albeit straightforward, incurs power losses attributable to the voltage drops between the diodes. The totem-pole PFC enhances this by substituting two diodes with fast-switching transistors (such as GaN or SiC FETs), which may be actively regulated to operate with significantly reduced losses. This enhances efficiency and enables the converter to exert superior control over the input current waveform, facilitating improved power factor performance.

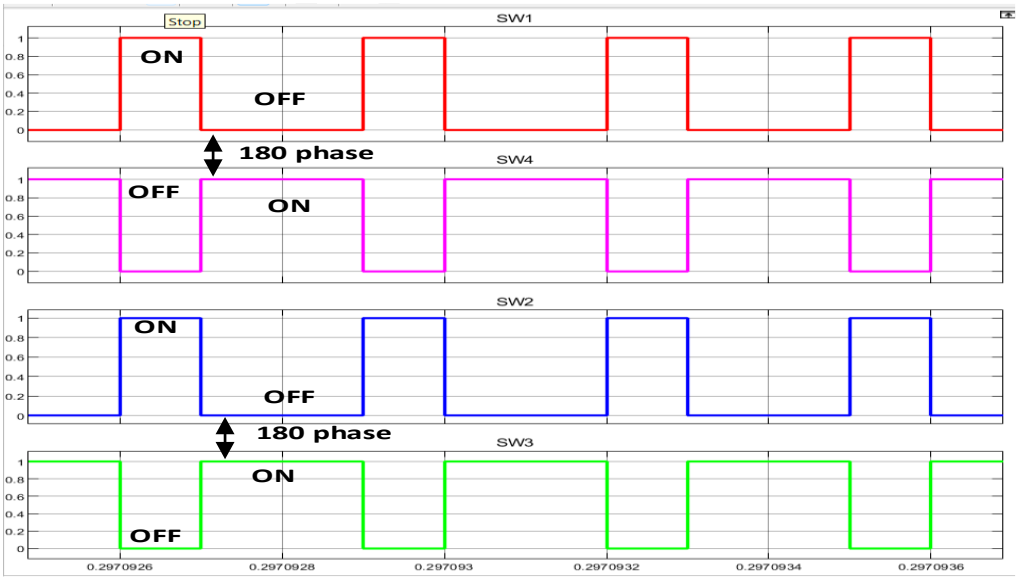


Fig.5. 2 gate pulse for interleaved totem-pole PFC(a) PWM_{SW1} (b) PWM_{SW4} (c) PWM_{SW2} (b) PWM_{SW3}

Interleaving is a method in which many power stages function asynchronously with one another. In a two-phase interleaved totem-pole power factor correction (PFC) system, the switches in each leg function 180 degrees out of phase shown in Fig.5.2. This indicates that when one leg is at the apex of its switching cycle, the other leg is at the nadir. This technique distributes the input current across numerous pathways, so diminishing the ripple in both the input and output currents. It additionally reduces heat stress on individual components, leading to enhanced dependability and an extended lifespan of the power supply.

The functionality of the totem-pole PFC varies with the polarity of the AC input voltage. In the positive half-cycle, the current traverses from the AC source through the high-frequency switch in the active leg, passes through the boost inductor, and enters the output capacitor and load. A low-frequency switch or diode facilitates the return pathway. In the negative half-cycle, the alternate switches engage current traverses a distinct active leg, although the operation fundamentally stays unchanged. This symmetry enables the circuit to sustain uninterrupted power delivery with negligible switching losses.

5.1.2 LLC Resonant DC- DC Converter

Four identical switches exhibit parasitic capacitances. Cds_7, Cds_8, Cds_9, and Cds_{10}; C_{out} is sufficiently large to maintain a steady output voltage Vo. The output voltage Vo fluctuates with the switching frequency fr of the LLC resonant converter. During the energy transfer from the primary to the secondary side of transformers, the magnetizing inductors Lm constrained, resulting in resonance between Lr and Cr, characterized by the resonance frequency fr.

$$f_r = \frac{1}{2 \times \pi \sqrt{L_r \times C_r}}$$

If energy is not transferred to the secondary side, the load will be sustained by discharging the output capacitor Co, resulting in resonance within Lr, Cr, Lm with the second resonant frequency designated as fm. Pulse Frequency Modulation (PFM) is utilized to control the output voltage of the proposed LLC resonant converter. The switching network operates with a 50% duty cycle at a switching frequency fs.

5.1.1 Mode 1 ($t_0 - t_1$):

Prior to t_0; S_7, S_8; S_9 and S_{10} are deactivated. At t D t0; Dds_7 and Dds_{10} conduct, the drain-source voltages of S_7 and S_{10} diminish from Vdc to zero, therefore establishing the circumstances for ZVS turn-on. In this mode, energy is transmitted from the primary to the secondary side of transformers, where resonance occurs between Lr and Cr. Diodes D_1, D_3, conduct, causing the resonant current i_{Lr} to decrease sinusoidally in the negative direction. The voltages of L_m clamped to nVo, while the magnetizing currents i_{Lm} decrease linearly in the negative direction (iLm =im). The primary currents of the transformers are equal to iLr - im > 0.

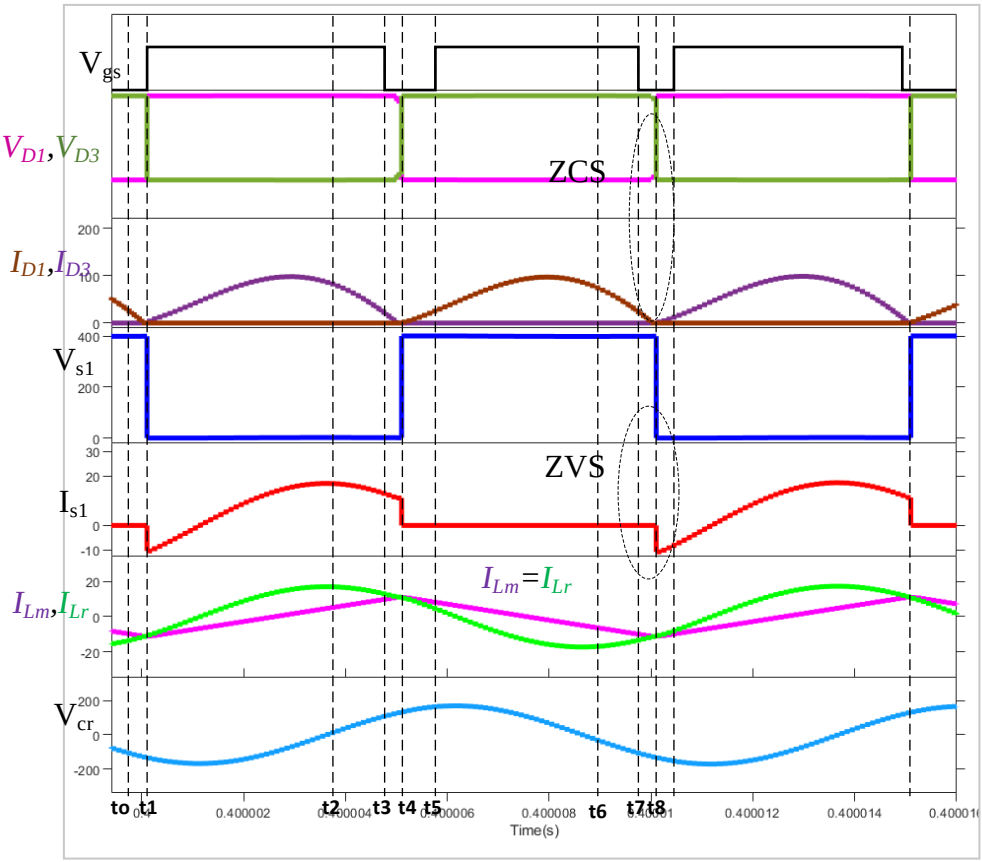


Fig.5. 3 (a) gate to source voltage (V_{gs}), (b) Diode Voltage (V_{D1}), (C) Diode Current (I_D), (d) Voltage across Switch (V_{s1}), (e) Switch Current (I_{s1}), (f) Resonant Inductor current and magnetizing current (I_{Lr}, I_{Lm}), (g) voltage across Resonant Capacitor (V_{cr})

5.1.2Mode 2 ($t_1 - t_2$):

At t = t_1, zero-voltage switching (ZVS) turn-on of switches S_7 and S_{10} is achieved. In this mode, the resonant current i_{Lr} varies sinusoidally in the positive direction. Given that D1, D3 are conducting, the voltages across Lm remain fixed at nVo. The primary currents of the transformers are equal to i_{Lr} - i_m > 0, facilitating energy transfer from the input to the load at the resonant frequency fr.

5.1.3 Mode 3 ($t_2 - t_3$):

At t = t_2, L_m commence resonance with Cr and Lr, resulting in a resonant frequency of fm. The magnetizing currents iL_m increase and equal the resonant current i_{Lr}, while the primary currents of both transformers become zero. In this mode, the load is powered by the output filter capacitor C_{out}, and the energy from the primary side is no longer conveyed to the secondary side. As D_1, D_3 deactivate spontaneously with zero current switching (ZCS), the reverse recovery loss is eradicated.

5.1.4 Mode 4 ($t_3 - t_4$):

At time t equals t_3, S_7 and S_{10} are deactivated. In this mode, the parasitic capacitors Cds_7, Cds10 resonate with Lr; Cds_7 and Cds_{10} are charged by the resonant current iLr, while Cds8 and Cds9 discharge. At time t D = t_4, the voltages of Cds_7 and Cds_{10} increase to Vdc, whilst the voltages of Cds_8 and Cds_9 decrease to zero.

5.1.5 Mode 5 ($t_4 - t_5$):

At t = t4, D_2, D_3 are all in the on-state. Dds_8 and Dds_9 conduct after the parasitic capacitors finish charging and discharging, resulting in zero drain-source voltages for S_8 and S_9, so establishing the conditions for Zero Voltage Switching (ZVS). Resonance transpires between Cr and Lr; as iLr and iLm diminish, the primary currents of the transformers equal iLr - im < 0, and the voltages of the magnetizing inductors Lm -nVo.

5.1.6 Mode 6 ($t_5 - t_6$):

At time t = t_5, the ZVS turn-on of S_8 and S_9 is achieved, with iLr = 0. In this mode, resonance transpires between Cr and Lr at frequency fr. The resonant current iLr decreases in the negative direction, while iLm transition linearly from positive to negative. Energy is transferred from the primary side to the secondary side of the two transformers.

5.1.7 Mode 7 ($t_6 - t_7$):

At time t = t6, when iLm1 and iLm equal iLr, the resonant tank including Cr, Lr, Lm resonates at frequency fm. Consequently, energy from the primary side is not transferred to the secondary side of the two transformers; the load Ro is solely powered by Cout. The reverse recovery losses of diodes D_2, D_3 are diminished due to zero-current switching (ZCS) turn-off.

5.1.8 Mode 8 ($t_7 - t_8$):

At t = t_7, S_8 and S_9 are deactivated, while D_1, D_3 are in a conducting state. In this mode, resonance transpires among Cds_7, Cds_{10}, Cds_8, Cds_9, and Lr; Cds_8 and Cds_9 are energized via resonant current iLr, whereas Cds_7 and Cds_{10} undergo discharge. At t8, the voltages of Cds8 and Cds9 ascend to Vdc, while the voltages of Cds_7 and Cds_{10} diminish to zero.

5.2 Design of Interleaved Totem-pole

5.2.1 Calculation of DC Link Voltage

The DC link voltage should be higher than the peak of single-phase grid voltage.

$$V_{DC} = \sqrt{2}V_{rms} \tag{5.1}$$

$$V_{DC} = \sqrt{2} \times 230 = 325.269\ V \tag{5.2}$$

Hence, the DC Link voltage is chosen as 400 V

5.2.2 DC Link Capacitor

The logic behind the design of the DC capacitor is governed by the reduction in the DC bus voltage upon the application of the load and rise in the DC bus voltage on removing the load. Using the principle of conservation of energy, the equation for C_{DC} is

$$C_{DC} = \frac{P_{out}}{\Delta V \times 2\pi f_{ac} \times V_{out,min}^2} \tag{5.3}$$

$$C_{DC} = \frac{6600}{0.03 \times 2\pi \times 50 \times 394^2} = 4511\ uF \tag{5.4}$$

5.2.3 EMI Inductor

High-frequency noise produced by power electronic switching circuits (such as PFC stages and inverters) is suppressed by an EMI (Electromagnetic Interference) inductor, which stops it from returning to the power grid or entering delicate electronics. The value for EMI inductor is calculated with the help of this formula

$$L_1 = \frac{1}{I_{ripple}} \frac{V_{rms}^2}{P_{out}} \left(1 - \frac{\sqrt{2}V_{rms}}{Vout}\right) \frac{1}{F_{sw}} \tag{5.5}$$

$$L_1 = \frac{1 \times 230^2}{0.2 \times 6600 \times 100 \times 10^3} \left(1 - \frac{\sqrt{2} \times 230}{400}\right) = \ 0.74872\ uH \tag{5.6}$$

$$L_2 = \frac{1}{I_{ripple}} \frac{V_{rms}^2}{P_{out}} \left(1 - \frac{\sqrt{2}V_{rms}}{Vout}\right) \frac{1}{F_{sw}} \tag{5.7}$$

$$L_2 = \frac{1 \times 230^2}{0.2 \times 6600 \times 100 \times 10^3} \left(1 - \frac{\sqrt{2} \times 230}{400}\right) = \ 0.74872\ uH \tag{5.8}$$

5.3 Design of LLC DC-DC Resonant converter component

The next stage of power conversion, in this case an LLC resonant converter, uses the regulated DC-link voltage (V_{DC}) set to 400 volts, which is usually the output of a previous power stage, like a rectifier or PFC converter. The maximum output voltage (V_{out}) that

the converter is expected to supply is 56 volts, which is the voltage that could be used to power a DC load or charge a battery. Fr stands for the LLC converter's resonance frequency. The converter's LC (inductor-capacitor) network naturally resonates at this frequency. It establishes the frequency at which the converter operates most efficiently and is a crucial design component. f_{sw} is a representation of the converter's switching frequency. During operation, the power switches (such as MOSFETs) are turned on and off at this frequency. We can control the converter's output voltage by altering fsw. To compare how far the switching frequency is from the resonant frequency, we define a normalized frequency, represented as f_n. It is given by:

$$f_n = \frac{f_{sw}}{f_o} \tag{5.9}$$

This normalized frequency helps us analyse the performance of the LLC converter more generally, without being tied to specific frequency values. Operating at the resonant frequency means $f_n = 1$, which is typically the point of highest efficiency. Operating above or below this value affects the voltage gain and efficiency of the converter in predictable ways.

Depending on the charging current and rate, the drained battery is charged in the CC mode, raising the battery pack voltage to 56 V. In addition, the battery of the e-bike is charged in the CV mode, and the current used to charge the battery decreases. Thus, by altering its DC-link voltage V_{DC}, LLC converter is intended to operate the below-resonance operation zone above 53.5 V. The transformer turns ratio, taking into account 53.5 V as the nominal output voltage at which the converter functions in pure resonance, is provided as

$$n = \frac{V_{in\_nom}}{2 \times V_{out\_nom}} \tag{5.10}$$

$$n = \frac{400}{2 \times 48} = 4.1666 \tag{5.11}$$

As a result, 25 primary turns (Np) and 6 secondary turns (Ns) are chosen for the main power transformer (Tx). Because of the lower core loss, the transformer's maximum designed flux density of 0.15 T is chosen to have a lower temperature rise. The transformer equation provides the lowest allowed switching frequency as

$$f_{min0.15T} = \frac{V_{DC}}{2 \times 4.44 \times \emptyset \times N_p \times A_e} \tag{5.12}$$

$$f_{min0.15T} = \frac{400}{2 \times 4.44 \times 0.15 \times 25 \times 1.62 \times 10^{-4}} = 74.1482\ KHz \tag{5.13}$$

In order to determine the resonant tank characteristics, the LLC converter's resonant frequency, which is greater than f_{min}, is chosen to be 100 kHz, while the lowest operating frequency is set at 75 kHz.

M_g stands for the resonant converter gain, which is the ratio of the input and output voltages, and is written as

$$M_g = \frac{V_{01}}{V_{i1}} = \frac{8 \times \omega_x^2 \times (m-1)}{\pi^2 \times \sqrt{\left((m \times \omega_x^2\right)^2 + Q^2 \times \omega_x^2 (\omega_x^2 - 1) \times (m-1)^2)}} \tag{5.14}$$

Where,

$Q = \frac{\omega_0 \times L_r}{R_e}$, $\omega_0 = \frac{1}{\sqrt{L_r \times C_r}}$, $\omega_x = \frac{\omega}{\omega_o}$, $m = \frac{L_{m \times L_r}}{L_r}$

Q = Quality Factor,

$\omega_0 =$ Resonant Frequency,

m= ratio of magnetising inductance and resonant inductance to the resonant inductance

5.3.1 AC equivalent load resistance (R_e)

The AC equivalent load resistance, denoted by Re, is shown as

$$R_e = \frac{8 \times n^2 \times V_{out}^2}{P_{out}} \tag{5.15}$$

$$R_e = \frac{8 \times 4.166^2 \times 48^2}{6600} = 48.48\ \Omega \tag{5.16}$$

5.3.2 Resonant Peak Current

The peak current passing through the primary switching devices is also the resonant peak current passing through the LLC inductor.

$$I_{Lr} = \frac{2 \times \pi \times P_{out}}{2 \times V_{DC}} \tag{5.17}$$

$$I_{Lr} = \frac{2 \times \pi \times 6600}{2 \times 400} = 51.8362\ A \tag{5.18}$$

Now we have selected Q and m value by the help of gain vs frequency curve

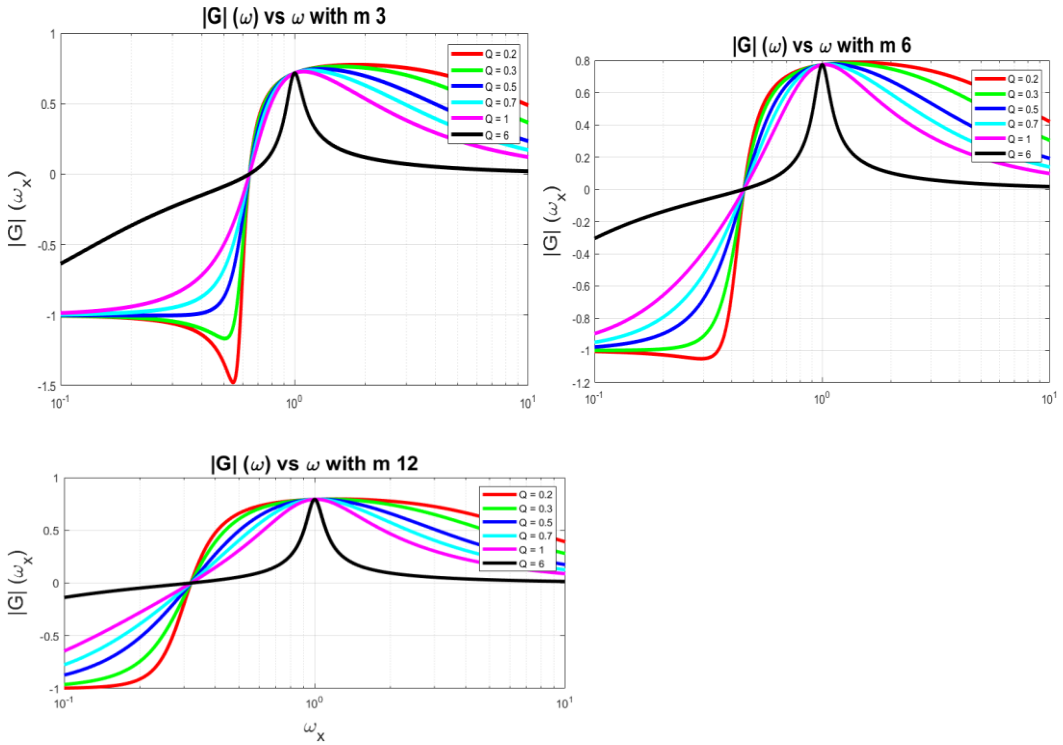


Fig.5. 4 (a) Gain Vs Frequency Curve when m=3, (b) Gain Vs Frequency Curve when m=6 (c) Gain Vs Frequency Curve when m=3

By seen above Gain Vs Frequency we have selected Qmax = 0.5 and m= 6.3 which is shown in Fig.5.4(b).

4.3.3 Resonant Capacitor

Since 100 kHz is chosen as the Resonant frequency, the resonant capacitor Cr is given as

$$C_r = \frac{I_{Lr}}{2\pi \times f_r \times V_{DC}} \tag{5.19}$$

$$C_r = \frac{21.2057}{2\pi \times 100 \times 10^3 \times 400} = 206.25\ nF \tag{5.20}$$

So, we taken resonant capacitor 210 nF.

4.3.4 Resonant Inductor

With the resonant capacitor Cr set at 210 nF and the resonant frequency fr, the resonant inductor Lr is provided as

$$f_r = \frac{1}{2\pi\sqrt{L_r \times C_r}} \tag{5.21}$$

$$L_r = 12.06\ \text{uH} \tag{5.22}$$

4.3.5 Magnetising Inductor

The air gap that is created in the primary transformer to provide the magnetizing inductance is stated as

$$m = \frac{L_m \times L_r}{L_r} \tag{5.23}$$

$$L_m = 66.33\ uH \tag{5.24}$$

5.4 Modelling of Control Algorithm

The LLC resonant converter and the Interleaved Totem-pole AC-DC converter are discussed separately for the control of the suggested battery charger.

CHAPTER 6

CONTROL STRATEGY AND RESULTS FOR INTERLEAVED TOTEM-POLE PFC CONVERTER AND LLC RESONANT

6.0 General

The control approach of an interleaved totem-pole power factor correction (PFC) converter is essential for maintaining efficient and stable performance under diverse load and input situations. In power electronics applications, particularly in electric vehicle charging and data centres, the necessity for good power quality and efficiency renders the selection and implementation of appropriate control techniques imperative. The totem-pole PFC architecture, especially when interleaved, has substantial benefits including less input current ripple, enhanced thermal management, and high-frequency performance owing to Sic-based fast-switching devices. A comprehensive control method is established to fully exploit these advantages, incorporating an outer voltage control loop, inner current control loops, power factor regulation, feedback conditioning, and synchronised PWM generation.

6.1 Voltage control Loop

The voltage controller constitutes the external loop of the control architecture. The major purpose is to regulate the converter's DC output voltage, maintaining it at a consistent level typically approximately 400V despite variations in load or input voltage. This is accomplished by consistently juxtaposing the measured output voltage with a reference

value. The resultant error signal is processed by a proportional-integral (PI) controller, which modifies the magnitude of the reference input current. The output of this voltage loop does not directly actuate the switching devices but instead establishes the amplitude for the current reference waveform. This modulation enables the system to dynamically

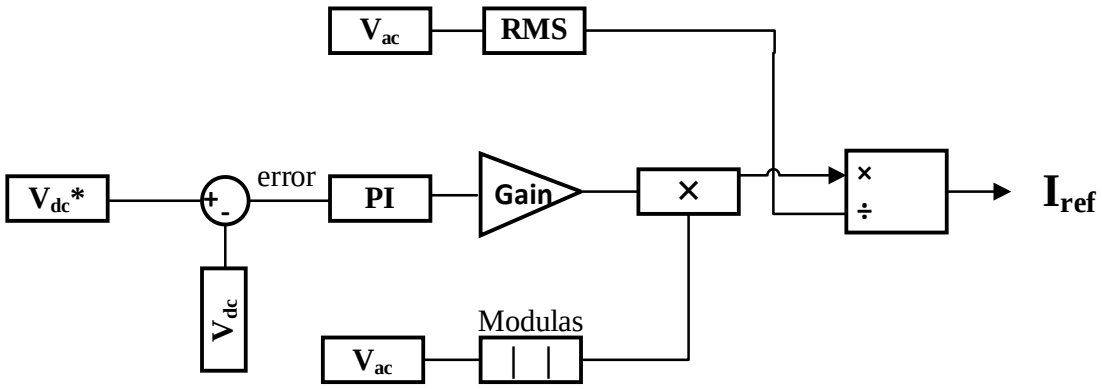


Fig.6. 1 Voltage Close loop Controller

regulate the power drawn from the grid, thus stabilising the DC output voltage.

The voltage control loop executes the subsequent steps:

- The output voltage measured is juxtaposed with the intended voltage reference.
- The error signal is processed by a Proportional-Integral (PI) controller to produce a control signal.
- This output represents the amplitude of the reference current waveform, guaranteeing that the power supplied from the AC input aligns with the load requirements.
- The loop may have filters and limiters to prevent instability or overshoots during abrupt load variations.

6.2 Current Control Loop

The inner current control loops ensure the maintenance of the specified input current profile. In an interleaved architecture, two loops are typically present—one designated for each leg of the converter. Each loop functions autonomously while maintaining synchronisation, allowing the two legs to alternate in conducting portions of the AC input current. The loops obtain the sinusoidal reference current produced by the power factor block, which is scaled according to the output of the voltage controller. The inductor current is measured and compared to the reference value, with the error being processed through a PI controller. The output from each current controller specifies the necessary duty cycle for the corresponding leg. The converter achieves optimal power quality by ensuring that the current remains in phase with the voltage while interleaving the legs at a 180-degree phase difference, resulting in reduced ripple and improved efficiency.

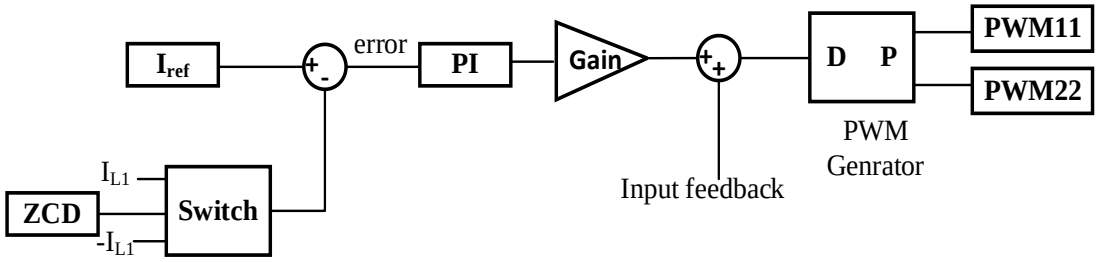


Fig.6. 3 Inner Loop Current controller 1

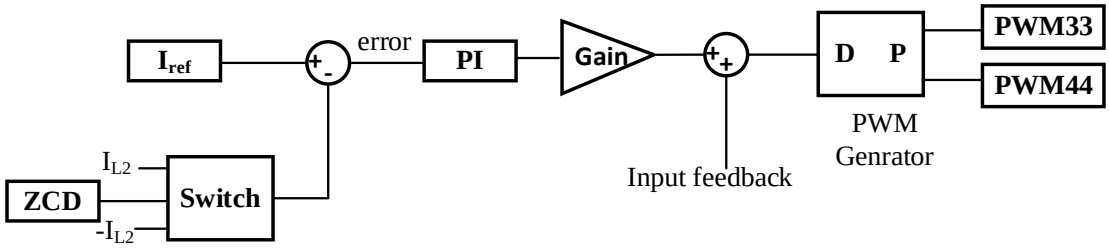


Fig.6. 2 Inner Loop Current controller 2

The current control loop comprises the following components:

- The reference current signal originates from the voltage controller and power factor block.
- Measurement of inductor currents in real-time (i_{L1} for leg 1 and i_{L4} for leg 2, respectively).
- A proportional-integral (PI) controller that evaluates the present error.
- Utilisation of feedforward or feedback compensation based on the measured output voltage.
- Creation of the suitable duty cycle signal.

6.3 Power Factor and Reference Current Generation

Achieving a high-power factor is a primary performance objective of the PFC converter. This design incorporates a specific block that computes the power factor and produces a pure sinusoidal reference for the current controllers.

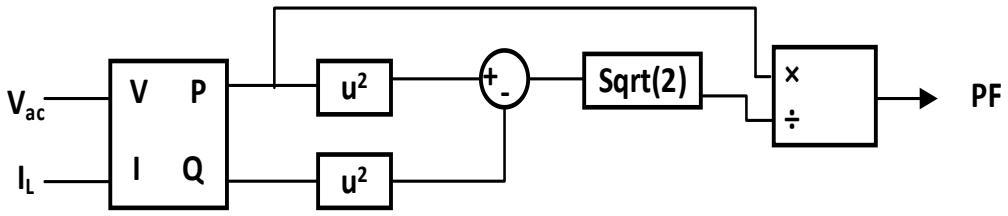


Fig.6. 4 Power Factor Calculation

This module measures the input voltage and current in real-time and computes their root mean square (RMS) values. A normalised sinusoidal waveform is produced that is

synchronised with the AC input voltage using these data. The waveform is subsequently adjusted according to the voltage controller's output to align with the real-time power requirements. The converter compels the input current to adhere to this waveform, so minimising harmonics and ensuring conformity with international standards like IEC 61000-3-2.

6.4 PWM Generation for Interleaved Legs

Pulse-width modulation (PWM) is the method by which control signals are converted into switching actions in the power stage. This interleaved totem-pole PFC architecture incorporates two distinct PWM generation blocks, one for each leg. These blocks obtain the modulated duty cycle signals from their corresponding current controllers.

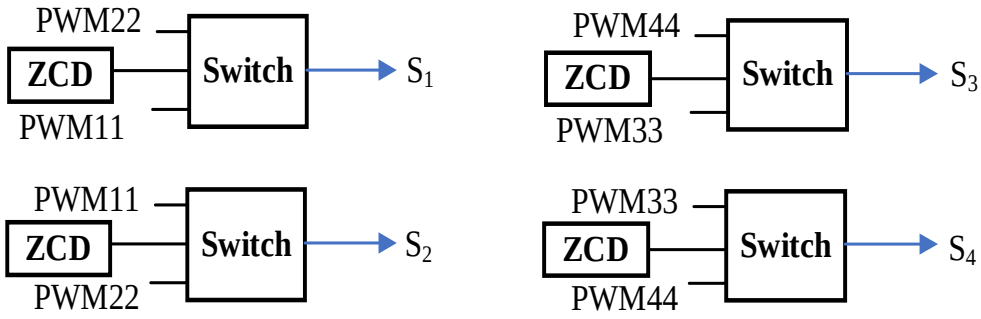


Fig.6. 5 switching pulse for Interleaved Totem-pole pfc

A triangle carrier signal generates the PWM, and to facilitate interleaving, the carrier signals are phase-shifted by 180 degrees between the two legs. This phase shift guarantees that when one leg is activated, the other is deactivated, and vice versa. The cumulative impact results in the cancellation of input current ripple, a doubling of the effective

switching frequency at the input, and a substantial reduction in electromagnetic interference (EMI).

6.5 Zero-Current Detection (ZCD)

The control system, principally intended for continuous conduction mode (CCM) operation, incorporates a zero-current detection (ZCD) mechanism to facilitate light load or boundary conduction mode operation. The ZCD circuit identifies the precise instant when the inductor current reaches zero. This information can optimise the timing of the subsequent switching event to facilitate gentle switching or transition to boundary conduction mode (BCM) for enhanced efficiency at light loads.

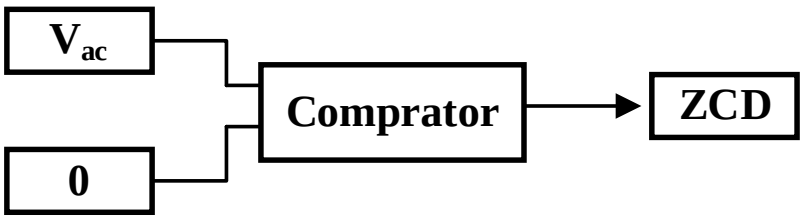


Fig.6. 6 Zero crossing detector

The ZCD mechanism, in conjunction with the PWM logic, minimises switching losses and enhances the longevity of the switching devices. In an interleaved system, it is essential to prevent false triggering or interference between legs; hence, accurate timing and filtering are vital.

6.6 Feedback Conditioning

Dependable and noise-free feedback is crucial for reliable control loop functionality. This design incorporates a specialised feedback processing block that guarantees the proper

filtering and scaling of all voltage and current signals. Analogue feedback from voltage and current sensors is initially processed using anti-aliasing filters to eliminate high-frequency switching noise.

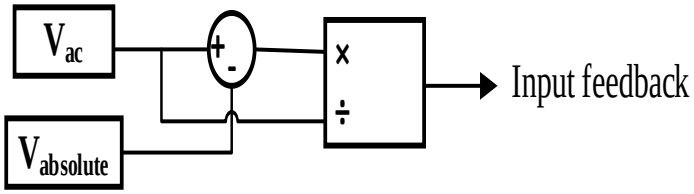


Fig.6. 7 Input Feedback

The signals are subsequently attenuated to conform to the voltage range of the digital controller's ADC (Analog-to-Digital Converter). Furthermore, software low-pass filters are utilised to mitigate measurement jitter. Effective feedback conditioning guarantees the precision of control decisions and safeguards against instability caused by measurement noise or delays. This block has protection systems, including over-voltage, under-voltage, and over-current detection, to guarantee safe operation.

6.7 Benefits of Interleaved Control Strategy

The outlined interleaved control method presents numerous practical advantages:

6.7.1 Minimised Input Current Ripple: Interleaving essentially doubles the current ripple frequency, facilitating EMI filtering and diminishing losses in the input stage.

6.7.2 Thermal Distribution: Power loss is allocated between two legs, mitigating thermal stress on each component and improving reliability.

6.7.3 Rapid Transient Response: The dual-loop control architecture (voltage and current loops) facilitates swift reactions to input or load variations.

Enhanced Efficiency: The ZCD-based operation and diminished conduction losses facilitate efficiencies exceeding 98% in some systems.

6.7.4 Scalability: The modular design facilitates straightforward expansion to additional phases (e.g., 3-phase interleaving for enhanced power levels).

6.8 Closed-Loop Control of LLC Resonant Converter for Constant Voltage and Constant Current Operation

The LLC resonant converter finds extensive application in high-efficiency power conversion scenarios, such as battery chargers and power supplies. To accommodate diverse load requirements and guarantee effective battery charging, it is essential to implement a strong control strategy. This section explores the design and operational principles of a closed-loop control system for an LLC converter that can function in both constant current (CC) and constant voltage (CV) modes.

6.8.1Dual-Mode Control's Significance in Battery Charging

Battery charging generally comprises two principal phases: the Constant Current (CC) mode during the first charging stage and the Constant Voltage (CV) mode as the battery approaches full charge. The CC mode facilitates the swift charging of the battery at a constant current until it attains a specified voltage threshold. Subsequently, the constant

voltage (CV) mode assumes control, preserving the voltage at a fixed level as the current progressively diminishes. This transition guarantees effective charging while preventing battery damage from overvoltage or overheating. Consequently, the implementation of a dual-mode control scheme in the LLC converter is crucial for performance and safety.

6.8.2 Outer Voltage Control Loop (CV)

The outer loop of the controller manages voltage regulation. It functions mostly during the constant voltage phase of charging when the battery voltage approaches its maximum limit (e.g., 56V in this model). The reference voltage is juxtaposed with the actual battery voltage feedback, and the resultant error is transmitted to a Proportional-Integral (PI) controller. This controller modulates the output to eradicate steady-state faults and dynamically respond to voltage fluctuations. The output of this PI controller serves as the reference current for the inner current loop, establishing a cascaded control system that guarantees accurate regulation.

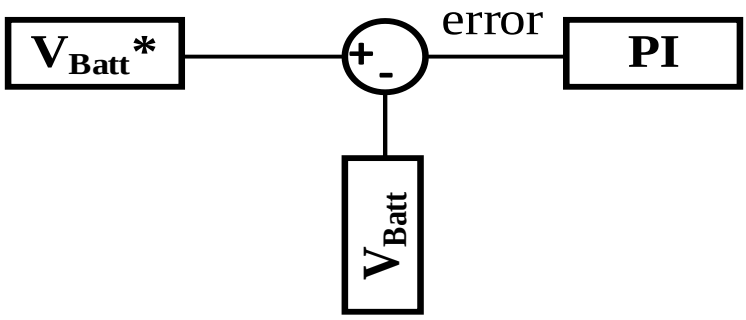


Fig.6. 8 Outer Voltage close loop For LLC Resonant Converter

$$V_e(n) = V_{Batt}^{*} - V_{Batt} \tag{6.1}$$

6.8.3 Inner Current Control Loop (CC Regulation)

The inner loop regulates current, particularly during the initial phases of charging when battery voltage is low and current demand is elevated. The reference current from the voltage loop is juxtaposed with the actual measured current, and the discrepancy is handled using a secondary PI controller. The controller's output regulates the LLC converter, usually by varying its switching frequency. This modulation guarantees that the output current accurately tracks the reference, sustaining a constant charging current and enhancing power conversion efficiency.

$$I_e(n) = I_{Li}^* - I_{Li} \tag{6.2}$$

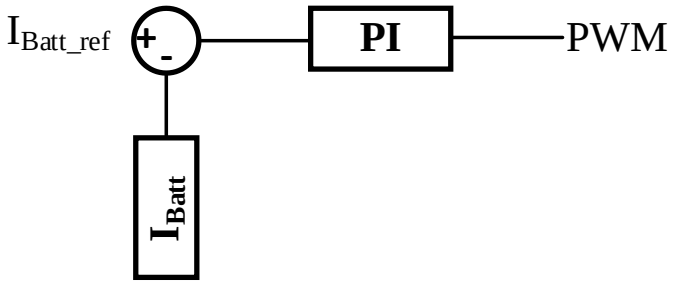


Fig.6. 9 Inner close loop For LLC Resonant Converter

6.8.4 Mode Selection Logic: Switching Between CC and CV

An essential feature of the design is its capacity to autonomously transition between CC and CV modes according to real-time system conditions. The comparator block manages the decision-making process by overseeing the output of the current loop. If the present controller output exceeds a specific threshold or waveform reference, it signifies that the

converter is in the Constant Current (CC) phase. Alternatively, the system transitions to constant voltage mode.

This mode determination is further enhanced through the application of logical processes, including NOT gates and signal selectors. Based on the outcome, the controller determines whether to utilise the voltage loop or the current loop output for modulating the LLC converter. This seamless transition guarantees smooth operation without voltage or current overrun, while preserving the intended power delivery profile during the charging cycle.

6.8.5 Control Signal Generation and Modulation

The ultimate control output following mode selection is transmitted to the modulation unit of the LLC converter. In LLC converters, modulation frequently entails frequency regulation, as the converter gain depends on the switching frequency. In CC mode, the controller may function the converter close to its resonance frequency, where the gain is elevated, thereby providing sufficient current. In CV mode, the frequency can be adjusted upward or downward to keep the output voltage within safe parameters. This advanced frequency regulation facilitates soft-switching, hence minimising losses and enhancing the longevity of the converter.

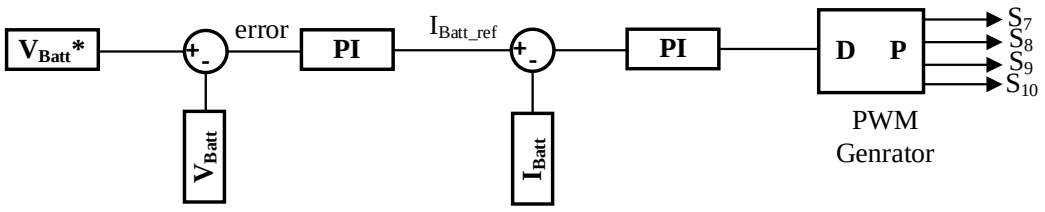


Fig.6. 10 controller of LLC Resonant DC DC Converter

6.9 SIMULATION RESULTS AND DISCUSSION

Using a 48 V and 100 Ah battery pack, the simulation verification of the new charger with Sic Interleaved Totem-pole and LLC Resonant DC-DC converter is shown in this section. The performance of the charger in steady state as well as for transients in source voltage and DC-link voltage is documented and discussed as follows.

6.9.1 Interleaved Bridgeless Totem-pole PFC

The initial stage of the charger is tasked with power factor adjustment and ensuring that the input current is synchronised with the input voltage. A totem-pole PFC topology was built in simulation, achieving great efficiency and decreased switching losses.

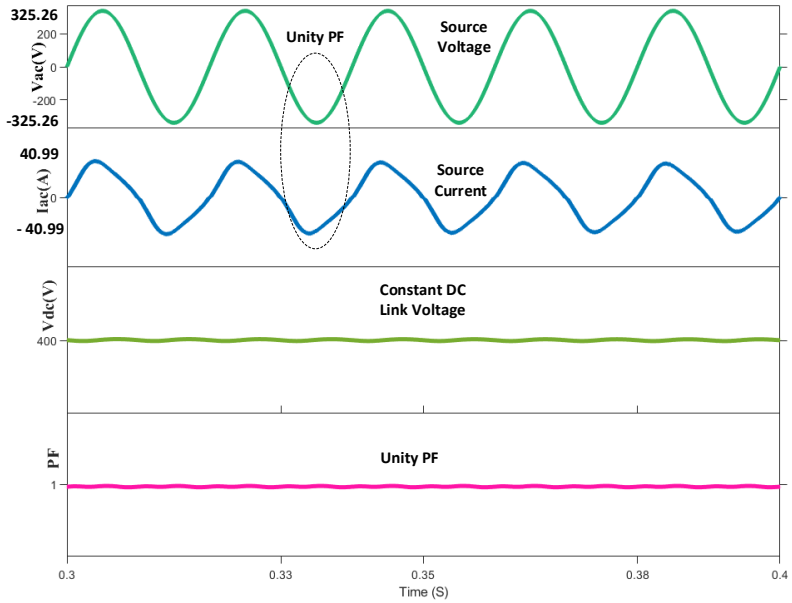


Fig.6. 11 (a) Source Voltage (V_{ac}), (b) Source Current (I_{ac}), (C) Dc Link Voltage (V_{DC}), (d) Power Factor

Refer to Figure 8. The input voltage and current waveforms are presented, demonstrating that the current waveform roughly aligns with the voltage waveform. The simulation findings indicate a Power Factor of 0.99, signifying near-unity power factor operating. The Totem-Pole PFC stage is engineered to deliver a stable output of 400V DC with minimal ripple, which then functions as the input for the LLC Resonant DC-DC converter in the following stage. The output voltage remains at 400V DC during the operation, demonstrating the PFC stage's capacity to manage fluctuating load conditions well and validating the performance of the output capacitor and management technique.

6.9.2 LLC Resonant DC-DC Converter

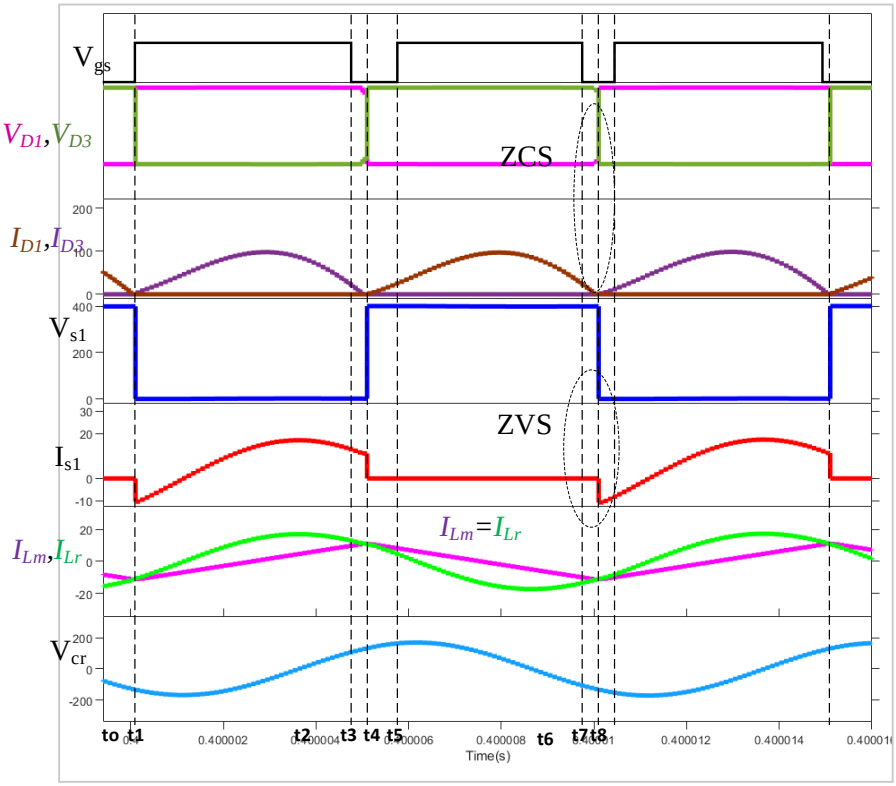


Fig.6. 12 (a) gate to source voltage (V_{gs}), (b) Diode Voltage (V_{D1}), (C) Diode Current (I_D), (d) Voltage across Switch (V_{s1}), (e) Switch Current (I_{s1}), (f) Resonant Inductor current and magnetizing current (I_{Lr}, I_{Lm}), (g) voltage across Resonant Capacitor (V_{cr})

The illustration depicts essential switching nodes and current/voltage waveforms of the LLC resonant converter throughout one switching cycle, distinctly delineated by time intervals from t0 to t7. This waveform analysis is crucial for validating soft-switching phenomena—Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS)—which enhance the efficiency and minimize switching losses of the LLC topology.

6.9.2.1 Gate-Source Voltage (V_{gs})

The initial graph illustrates the gate signals (V_{gs}) administered to the primary-side switches. These digital impulses oscillate between high and low logic levels, intermittently activating and deactivating the switches. The clear and precise transitions signify optimal gate driving devoid of delay or overlap, crucial for effective resonant functioning and the attainment of soft-switching.

6.9.2.2 Diode Voltages (V_{D1}, V_{D3})

The second graph illustrates the voltages across the output rectifier diodes D1 and D3. The voltages diminish to zero immediately prior to the diodes commencing conduction, indicating Zero Current Switching (ZCS). This is essential for reducing diode reverse recovery losses and enhancing the overall efficiency of the converter. The alternating operation of D1 and D3 guarantees the complete bridge rectification of the resonant AC waveform.

6.9.2.3 Diode Currents (I_{D1}, I_{D3})

This waveform illustrates the current flowing between diodes D1 and D3. Each diode conducts sinusoidal current, characteristic of resonant converters. The current becomes zero precisely as the diode deactivates, confirming the Zero Current Switching (ZCS)

condition. The waveform's symmetry illustrates equitable load distribution among the diodes on alternate half-cycles.

6.9.2.4 Switch Node Voltage (V_{s1})

V_{S1} denotes the voltage at the midpoint of the primary-side full bridge. The waveform alternates between elevated and diminished voltage levels in relation to the input voltage and ground. The abrupt transitions synchronized with the gate signals validate Zero Voltage Switching (ZVS) the switches activate when V_{S1} approaches zero, therefore minimizing switching losses and electromagnetic interference (EMI).

6.9.2.5 Resonant Tank Current (I_{s1})

The current traverses the resonant tank, comprising the resonant inductor and capacitor, and exhibits a sinusoidal characteristic. The waveform is uninterrupted and devoid of sudden changes, signifying that the converter functions in resonant mode. During switching events, the current provides adequate energy to attain zero-voltage switching by discharging the output capacitance of the MOSFET.

6.9.2.6 Magnetizing and Resonant Inductor Currents (I_{Lm}, I_{Lr})

The sixth plot illustrates the magnetizing current (I_{Lm}) and the resonant inductor current (I_{Lr}). Initially, $I_{Lm}$and I_{Lr} are practically indistinguishable, indicating operating close to resonance. These waveforms facilitate comprehension of power transfer and energy storage within the converter. The sinusoidal form of I_{Lr} signifies effective energy transfer within the resonant tank, whereas I_{Lm} maintains a steady flux in the transformer core.

6.9.2.7 Resonant Capacitor Voltage (V_{cr})

The last graph illustrates the voltage across the resonant capacitor (V_{cr}), which oscillates sinusoidally, as anticipated in a resonant tank. This waveform is essential for structuring the resonant current and sustaining ZVS conditions. The uninterrupted and fluid waveform verifies appropriate resonance characteristics and meticulously selected components.

6.10 Battery Charging Characteristics

The analysis of the LLC resonant DC-DC converter's performance during battery charging employs three primary metrics: State of Charge (SOC), battery current (I_{Batt}), and battery voltage (V_{Batt}). The simulation results are displayed for a time span of 0 to 0.5 seconds, emphasizing the dynamic behaviour and steady-state response of the converter.

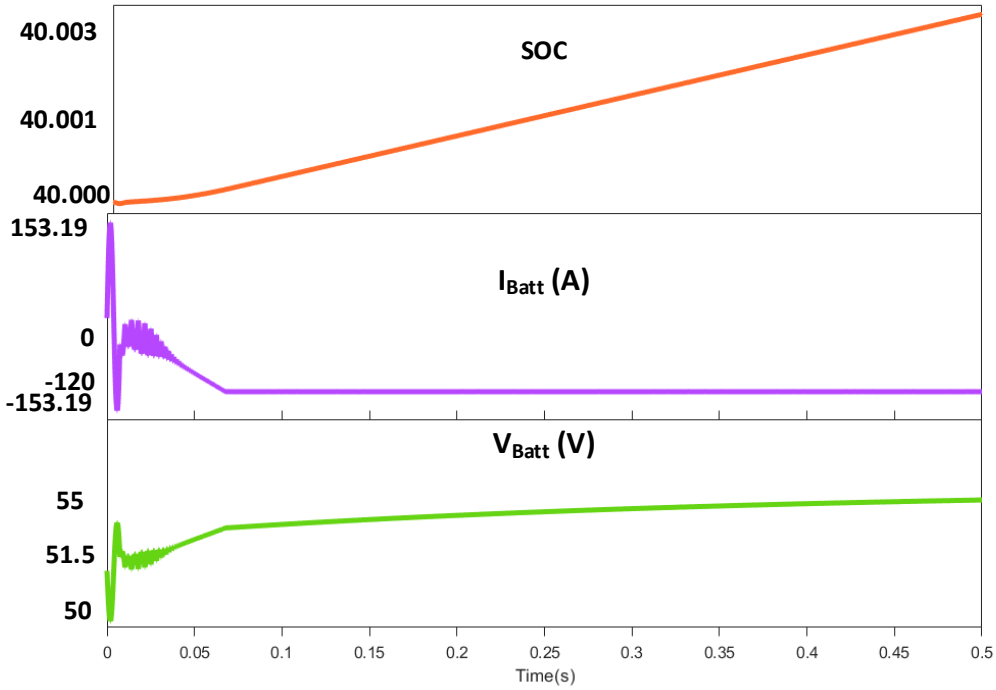


Fig.6. 13 (a) State of Charge (SOC), (b) Battery Current (I_{Batt}), (c) battery Voltage (V_{Batt})

6.10.1 State of Charge (SOC)

The uppermost graph depicts the fluctuation of SOC throughout time. The state of charge (SOC) commences at 40% and progressively rises during the simulation. The curve demonstrates a smooth and nearly linear ascent, signifying a consistent and reliable charging process. This behaviour verifies that the converter is efficiently delivering energy to the battery without sudden swings. Despite the limited time frame, the positive slope of the State of Charge (SOC) trajectory distinctly indicates the initiation and advancement of battery charging shown in Fig.6.13(a).

6.10.2 Battery Current

The central plot illustrates the battery current (I_{Batt}) during the charging duration. A transitory oscillating response is initially detected, typical of resonant converters owing to their intrinsic reactive components and soft-switching transitions. The oscillations rapidly stabilize, and the current levels off at roughly -120 A. The negative polarity indicates that current is flowing into the battery, suggesting charging. The rapid attenuation of oscillations signifies a finely calibrated resonant tank circuit and an efficient control technique, guaranteeing little stress on the converter's power devices while sustaining constant current (CC) mode operation shown in Fig.6.13(b).

6.10.3 Battery Voltage

The lower graph illustrates the battery voltage (V_{Batt}) Initially, the voltage displays minor oscillations akin to the current waveform, which are rapidly attenuated when the system reaches a steady state. The voltage initiates at roughly 50 V and ascends gradually to about 55 V. This gradual increase indicates a regulated charging procedure in which the

converter sustains a consistent output voltage. The lack of overshoot and voltage spikes indicates that the converter's output remains within the permissible range for safe and efficient battery charging shown in Fig.6.13(c).

6.11 Total Hormonic Distortion (THD)

It has been noted that the THD of Source current 7.947% in Fig.6.14(a) and THD of Source Voltage 0.00 % seen in Fig.6.14(b) In order to meet IEEE-519 standards, the high frequency inverter improved the source current's THD below 8%

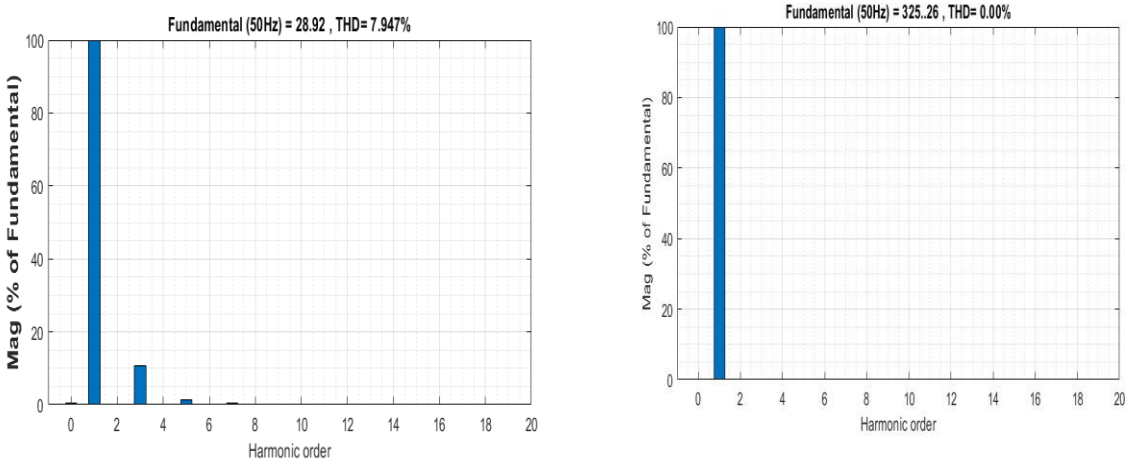


Fig.6. 14 (a) THD of source current (i_{ac}), (b) THD of source voltage (v_{ac})

CHAPTER 7

CONCLUSION AND FUTURE WORK

This study focuses on the modelling and simulation of Renewable to Grid + Battery R2(G+V) mode and Renewable + Battery to Grid (R+V)2G in a three-phase system. The system consists of three converters: an AC-DC bidirectional converter, a DC-DC boost converter, and a bidirectional DC-DC converter. The grid-side converter is controlled by a self-tuning filter controller, which lowers harmonics. The results illustrate the effective operation and performance improvements achieved using the proposed strategy. As demonstrated by the comparison results, the suggested algorithm STF converges moderately, requires no transformation block or PLL, and involves less computations, overshoot, and oscillations. Grid current's total harmonic distortion (THD) is below the IEEE-519 Standard's acceptable range.

The article ends by suggesting possible avenues for future research, opening the door for Advanced Algorithms for Real-Time Tuning by using Machine Learning and AI, Integration Enhanced Battery Health Monitoring and Management and more advancements in this important area of study.

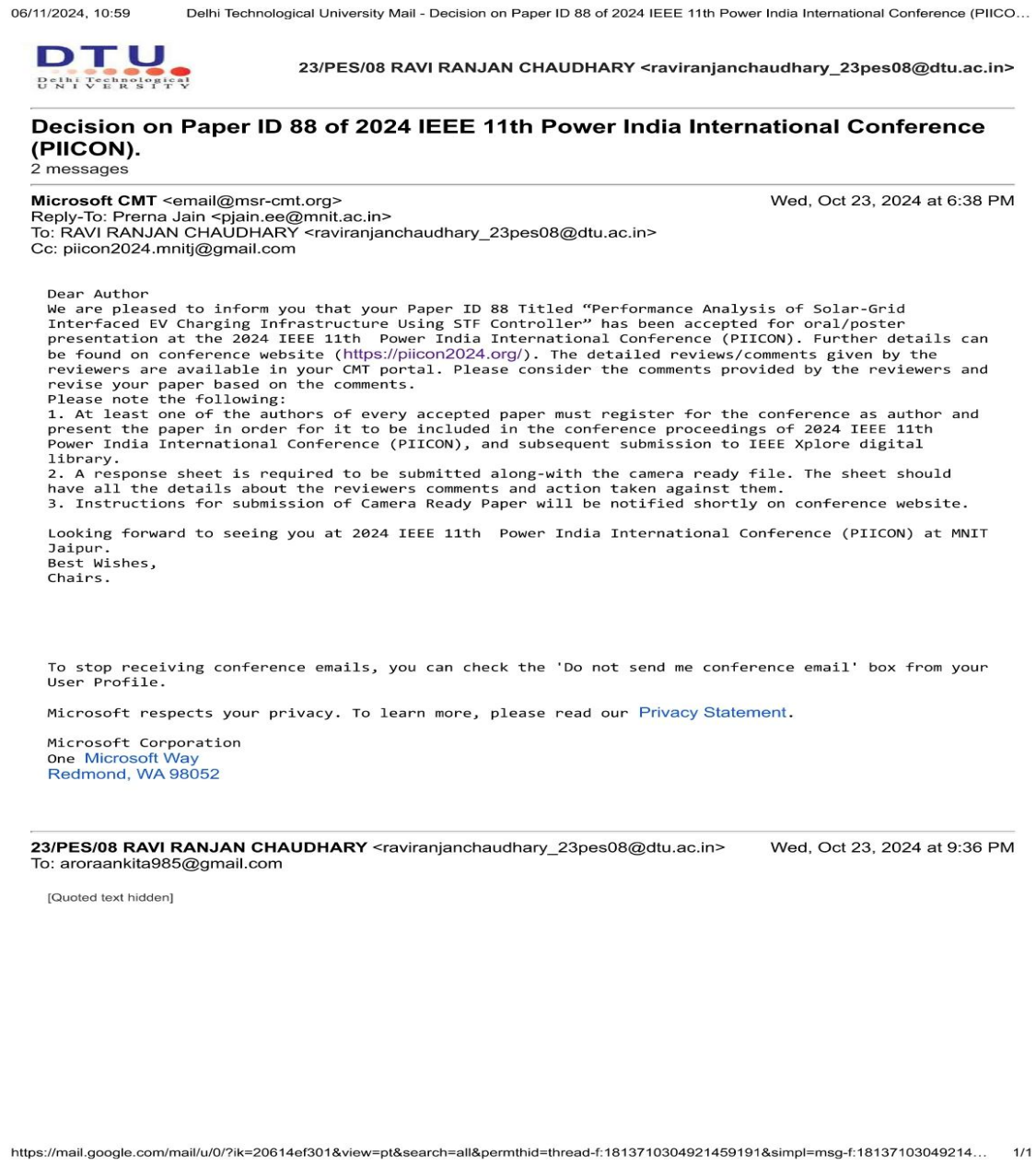
Future research can concentrate on the following areas even though the suggested charger architecture shows excellent efficiency and power quality: 1. Examining sophisticated control techniques for additional efficiency gains and improved control for higher power.

2. Improving heat management and system dependability through thermal management optimization. Higher charging efficiency and a longer charger life are the results of this.

3. Vehicle-to-grid (V2G) applications are made possible by integrating bidirectional power flow.

LIST OF PUBLICATION

*Ravi Ranjan Chaudhary, A. Arora, Sikandar Ali khan, "Performance analysis of Solar-Grid Interfaced EV Charging Infrastructure Using STF Controller," in *2024 IEEE 11th Power India International Conference (PIICON-2024), Malaviya Institute of Technology, (MNIT) Jaipur, Rajasthan India, 10-12 December. 2024, p. 6.*



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Dear Author
We are pleased to inform you that your Paper ID 88 Titled "Performance Analysis of Solar-Grid Interfaced EV Charging Infrastructure Using STF Controller" has been accepted for oral/poster presentation at the 2024 IEEE 11th Power India International Conference (PIICON). Further details can be found on conference website (https://piicon2024.org/). The detailed reviews/comments given by the reviewers are available in your CMT portal. Please consider the comments provided by the reviewers and revise your paper based on the comments.
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