

DESIGN AND IMPLEMENTATION OF LOW POWER ARITHMETIC AND SHIFT REGISTER CIRCUITS USING GDI TECHNIQUE

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for the Degree of**

**MASTER OF TECHNOLOGY
In
VLSI DESIGN AND EMBEDDED SYSTEMS**

by

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CANDIDATE'S DECLARATION

I Amartya Roy, Roll No. 2K23/VLS/08 hereby certify that the work which is being presented in the thesis entitled ‘ **Design and Implementation of Low Power Arithmetic and Shift Register Circuits Using GDI Technique** ’in partial fulfillment of the requirements for the award of the Degree of Master of Technology (VLSI and Embedded Systems), submitted in the Department of Electronics and Communication Engineering , Delhi Technological University is an authentic record of my own work carried out during the period from March 2024 to May 2025 under the supervision of **Prof. Neeta Pandey** (Professor) and **Dr. Harikesh Dalal** (Asst. Professor)

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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Certified that 2K23/VLS/08 has carried out their research work presented in this thesis entitled “**Design and Implementation of Low Power Arithmetic and Shift Register Circuits Using GDI Technique**” for the award of **Master of Technology** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

This thesis presents a comparative study of GDI and TGDI techniques, implemented and analyzed on both combinational and sequential digital circuits, including D Flip-Flops, Ripple Carry Adders (RCA), Carry Select Adder (CSA), Serial-In Parallel-Out (SIPO) shift register, and Linear Feedback Shift Register (LFSR).

The arithmetic circuits under consideration Ripple Carry Adder (RCA) and Carry Select Adder (CSA) were designed using both GDI and TGDI logic styles. Simulation results using Cadence Virtuoso at 2V and 180nm CMOS technology demonstrated that the TGDI based RCA achieved a 38.2% reduction in delay and a 21.8% improvement in power-delay product (PDP) compared to its GDI counterpart. Similarly, the TGDI based CSA showed a 38.4% reduction in delay and a 23.1% improvement in PDP over the GDI based design. These enhancements confirm the effectiveness of TGDI logic in improving circuit speed and energy efficiency, making it a promising choice for arithmetic operations in low-power digital systems.

For shift register-based sequential circuits, including the Serial-In Parallel-Out (SIPO) shift register and the Linear Feedback Shift Register (LFSR), TGDI logic again outperformed its GDI counterpart. The TGDI based SIPO circuit showed a 41.6% delay reduction and a 25.8% improvement in PDP, while the LFSR design achieved a 33.8% lower delay and a 17.1% enhancement in PDP. Despite slightly higher power consumption, TGDI's reduced delay leads to better overall energy efficiency and performance. These results confirm TGDI's strong potential in modern VLSI designs where compactness, speed, and power efficiency are critical.

LIST OF PUBLICATIONS

- [1] A.Roy , N. Pandey , H. Dalal “**Implementation of Linear Feedback Shift Register circuit (LFSR) Using Transmission Gate Diffusion Input(TGDI) Technique**” Submitted and accepted (Publication in progress) in the 6th IEEE India Council International Subsections Conference (**INDISCON 2025**)
- [2] A.Roy , N. Pandey , H. Dalal “**Energy Efficient 4-Bit Ripple Carry Adder Design Using Transmission Gate Diffusion Input (TGDI) Technique**” Submitted and accepted (Publication in progress) in the 6th IEEE India Council International Subsections Conference (**INDISCON 2025**)

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LIST OF ABBREVIATIONS

	WORD	ABBREVIATIONS
1.	Very Large Scale Integration	VLSI
2.	Complementary Metal-Oxide-Semiconductor	CMOS
3.	Gate Diffusion Input	GDI
4.	Transmission Gate Diffusion Input	TGDI
5.	Transmission Gate	TG
6.	Power Delay Product	PDP
7.	Ripple Carry Adder	RCA
8.	Serial-In Parallel-Out	SIPO
9.	Linear Feedback Shift Register	LFSR
10.	D Flip-Flop	DFF
11.	Flip-Flop	FF
12.	Microwatt	μW / uW
13.	Picosecond	ps
14.	Femtojoule	fJ
15.	Nanojoule	nJ
16.	Integrated Circuit	IC
17.	Application Specific Integrated Circuit	ASIC
18.	Hardware Description Language	HDL
19.	Register Transfer Level	RTL
20.	Computer-Aided Design	CAD
21.	Design Rule Check	DRC
22.	Process Design Kit	PDK
23.	N-type Metal-Oxide Semiconductor	NMOS
24.	P-type Metal-Oxide Semiconductor	PMOS
25.	Micrometer	μm / um
26.	Nanometer	nm
27.	Supply Voltage	VDD
28.	Simulation Program with Integrated Circuit Emphasis	SPICE
29.	Clock	CLK

30.	Setup Time	SETUP
31.	Hold Time	HOLD
32.	Ripple Carry Adder	RCA
33.	Carry Select Adder	CSA
34.	Serial In Parallel Out	SIPO
35.	Linear Feedback Shift Register	LFSR

CHAPTER 1

INTRODUCTION

Chapter 1 highlights the development of techniques along with technologies for low power circuits. The literature review of Gate Diffusion Input (GDI) technique helps us to observe that we can achieve more faster speed in circuits if we do some modifications in the current GDI technique. If we use Transmission Gate in place of normal GDI gates, we get the swing for full voltage along with the delay time of the given system is comparatively less.

1.1 OVERVIEW

With the rapid advancement of semiconductor technologies and the proliferation of portable electronic devices, power consumption has emerged as a critical design parameter alongside speed and area. In modern digital systems—especially in battery-operated applications such as smartphones, wearables, biomedical implants, and wireless sensors reducing the power consumption is important to extend battery usage time, improve thermal stability in order to ensure overall system reliability. High power dissipation in Very Large Scale Integration (VLSI) circuits can lead to increased leakage currents, thermal hotspots, and long-term degradation of device performance. As technology scales into nanometer regimes, both dynamism in power which is happening because of the switching activity and static power because of the leakage in the currents significantly impact the budget of the power, underscoring the importance of low-power design methodologies.

To address these challenges, a wide range of low-power design techniques have been explored at various abstraction levels from system and architectural strategies to circuit-level optimizations. Among these, the GDI method has gained a lot of attention because of its ability to implement complex logic functions using fewer transistors than traditional CMOS, resulting in reductions in area, power, and switching activity. However, GDI circuits may suffer from reduced voltage swing and signal degradation. To overcome these drawbacks, the Transmission Gate Diffusion Input (TGDI) technique integrates transmission gate logic into the GDI framework, ensuring full voltage swings, better signal integrity, and improved speed. Though TGDI designs might introduce slightly higher dynamic power due to additional control signals, they typically yield better overall efficiency

of the energy being measured by Power Delay Product (PDP).

This thesis explores designing along with analysis of key combinational as well as the circuits which are sequential in nature using both GDI and TGDI techniques, specifically focusing on a 4-bit Ripple Carry Adder (RCA), 4 bit Carry Select Adder (CSA), a 4-bit Linear Feedback Shift Register (LFSR), and a 4-bit Serial-In Parallel-Out (SIPO) register. The objective here is evaluating and comparing the circuits in terms of performance, in the way of consumption of power, delay along with the the PDP, providing a comprehensive understanding of the trade-offs involved in using GDI and TGDI methodologies. By leveraging the advantages of these low-power design techniques, the work aims to contribute toward the development of energy-efficient digital systems suitable for next-generation portable and high-performance applications.

1.2 Literature Review

The GDI methodology has come out to be a powerful option for conventional CMOS design, particularly in reducing power consumption and transistor count. A GDI-based D flip-flop was proposed in [1], achieving high speed and reduced area compared to traditional CMOS approaches. Further optimization of the GDI technique was introduced in [2], where the authors modified standard GDI logic to enhance performance in portable and low-energy devices. GDI's efficacy in arithmetic circuits was demonstrated in [3], where a Carry Select, Adder was designed to improve power, delay, and area metrics. These works collectively highlight the versatility of GDI in both sequential and combinational logic applications.

To address limitations of conventional GDI and exploit hybrid logic benefits, TGDI logic has been explored among several recent studies. A CNTFET based TGDI logic design was introduced in [12], showing improved power and performance for nanoscale technologies. In [5], TGDI was applied to multiplier circuits, significantly reducing power and transistor count. These innovations underscore the potential of TGDI as a viable option for ultra-low power arithmetic and data path components.

Transmission gate-based logic has also proven effective in designing sequential elements. Energy-efficient flip-flop designs based on transmission-gate multiplexers were proposed in [6], focusing on reducing dynamic power without sacrificing performance. Similarly, a high-frequency flip-flop architecture was introduced in [7], optimized for low power and high-speed operation in modern VLSI systems. Expanding beyond basic flip-flops, a novel full adder cell using a dual-mode TGDI (DMTGDI) technique was introduced in [5], achieving significant

improvements in the power-delay product, making it ideal for low-power ALU implementations.

Efforts to improve power efficiency extend to shift registers and LFSR based designs. A latch-based shift register implementation using pulsed latches was explored in [8], emphasizing reduced switching activity and clock power. Inspired by such designs, TGDI-based SIPO shift registers [9] are being used as an energy efficient alternative. LFSR design optimization was studied in [8], where the authors revisited logic structure selection to minimize area and power in cryptographic circuits. Similarly, the potential of structural and logic-level enhancements in SIPO architectures was examined in [10], motivating further exploration of TGDI logic in sequential data storage systems.

Arithmetic logic design continues to benefit from innovative logic styles. A low-power RCA was developed using an effective and optimal pass transistor logic in [11], highlighting that even simple circuits can benefit from non CMOS techniques. Also, in [3] a low power CSA has been developed using advance transistor logic. Such findings paved the way for exploring TGDI as a suitable replacement for traditional CMOS and pass-transistor-based arithmetic blocks.

1.3 Motivation

Through the detailed literature review, it has become evident that GDI and its derivative logic styles like TGDI offer impactful advantage as it reduces power usage, smaller area and enhanced speed in comparison to the regularly used CMOS logic. These techniques have shown significant improvements in basic logic gates, multiplexers, and flip-flops, particularly in applications where power efficiency is critical. However, despite these promising characteristics, there remains a noticeable gap in applying GDI and TGDI logic to fundamental digital components such as RCA, CSA, SIPO shift registers, and LFSR. These blocks will be the core building elements in arithmetic units, data converters, and cryptographic systems respectively, are being used in different VLSI model. Most existing designs for RCA, SIPO, and LFSR still rely on conventional CMOS or transmission gate logic, which, while reliable, are not optimal in terms of power efficiency—especially in context of low-power embedded systems, portable devices and IoT applications. The lack of reported work on TGDI based implementations of these blocks suggests an unexplored area of research, which presents an opportunity for innovation. This motivates the present work: to explore and implement GDI and TGDI based designs for RCA, CSA, SIPO, and LFSR circuits, with the aim of achieving superior power efficiency, lower transistor count, and competitive performance. By addressing this gap, the research contributes to formation of an energy efficient digital model suited for next-generation low-power VLSI systems.

1.4 Thesis Organization

Here thesis is being made in such a manner that there are several chapters to present systematically the research work and my findings.

Chapter 1: Introduction : This chapter highlights development of techniques and technologies for the low power circuits. The literature review of GDI technique helps us to observe that we can achieve more faster speed in circuits if we do some modifications in the current GDI technique. If we use Transmission Gate in place of normal GDI gates we get the swing to full voltage along with the delay in time for system is comparatively less

Chapter 2: GDI and TGDI Technique : This chapter presents the detailed design and working principles of the GDI) and TGDI techniques, including the modifications introduced for improved performance.

Chapter 3: Arithmetic Circuits : Here the focus is on the design along with implementation in arithmetic circuits, specifically the full adder along with 4-bit RCA and CSA, using both GDI and TGDI techniques. The functionality and performance aspects of these circuits are discussed in detail.

Chapter 4: Implementation of D Flip Flop : Here we have properly described and made the working of an D flip-flop using GDI and TGDI techniques. This chapter covers the circuit structures, delay, and performance evaluation of the flip-flop designs

Chapter 5: Shift Registers : This chapter covers the design and working of sequential circuits used in this thesis . Here 4-bit LFSR and the 4-bit SIPO registers have implemented by usage GDI and TGDI approaches.

Chapter 6: Conclusion: This chapter offers an overview of the studies, inferences made from the findings, and recommendations for additional research.

CHAPTER 2

GDI AND TGDI TECHNIQUES

Chapter 2 highlights Gate Diffusion Input (GDI) and Transmission Gate Diffusion Input (TGDI) techniques are employed to implement various logic circuits. These techniques are known for their ability to make the number of transistors being used are reduced which are being required in logic gate design, thereby achieving lower power consumption, reduced area, and decreased delay. The circuits were simulated using Cadence Virtuoso at 2V(for 0.18 μ m technologies, respectively), 100MHz , with capacitance of load 100fF. The Aspect Ratio of the MOSFET taken under consideration are (2 μ m/0.18 μ m). Key metrics her are the consumption of power along with delay as well a the Power-Delay Product (PDP) were have made a detailed study to evaluate, later compare efficiency of GDI and TGDI implementations with conventional CMOS logic.

2.1 Gate Diffusion Input (GDI) Technique

Like a CMOS inverter, a basic GDI cell is being formed by using two transistors: an NMOS and a PMOS. The source/drain and gate terminals in GDI, however, are set up differently: The terminals that are the source and drain of the NMOS and PMOS transistors, respectively, are made to have connection to the inputs N (N-well or P-substrate) and P (P-well or N-substrate). G is the transistors' shared gate input. D is the output obtained from the transistors' drain terminals. A CMOS inverter's construction is quite similar to that of the GDI circuit. The P of CMOS inverter is made to have connection with VDD, while the N source is grounded. It has three inputs (G, P, N) where G node is being used as the common gate inputs of our NMOS along with the PMOS, P node is being used as the source of Drain for PMOS input and N node is acted as the Drain or Source of the given NMOS input. Logic gates including AND, OR, NOR, and MUX have been designed employing the GDI approach, [1] which will reduce the circuit's count of transistor and hence lowers area and power demands. To create distinct logic functions, this cell is utilized to apply various inputs to G, P, and N.

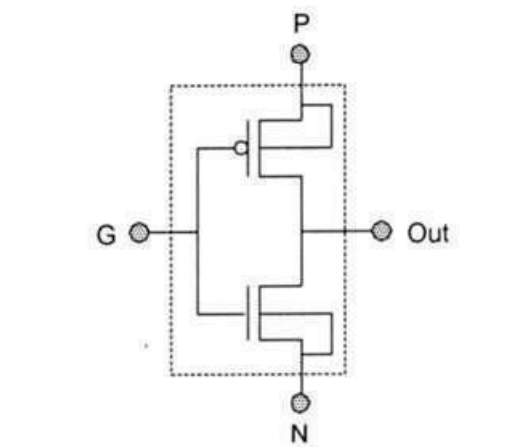


Fig. 2.1 : Basic GDI Cell[1]

In GDI cell, when gate G value is High, the NMOS gets activated and we get output as GN . And when using gate G value comes out low, then the output obtained is $G'P$. So, from here we can conclude that overall output of GDI cell is $GN + G'P$. Along with help of this technique we can implement various combinational logic gates. A table has been provided below :

Table 2.1 : Logic Function of GDI Cell

N	P	G	OUT	FUNCTION
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$A'B + AC$	MUX
0	1	A	A'	NOT

2.2 Simulations Using GDI Technique

Here, we have simulated logic gates using the GDI Techniques and analyzed their results like Power, Delay and Energy efficiency of the circuit.

2.2.1 INVERTER

The inverter is a basic and fundamental digital logical gate which is being used to reverse or inverts the input signal[12]. It is also referred to as a NOT gate. To put it another way, a logical low (0) will be output and reverse of it if the input is a logical high (1). In Fig 2.2 there is the basic representation of an inverter:

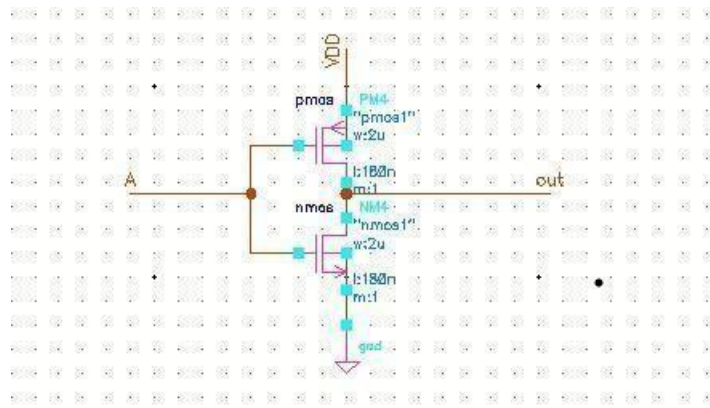


Fig. 2.2 : Schematic of Inverter Gate[1]

The timing waveform of the above circuit is shown in Fig 2.3:

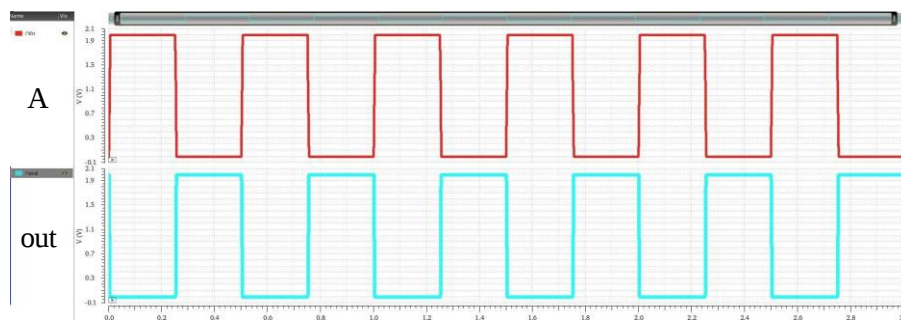


Fig. 2.3 : Transient Analysis of Inverter Gate

Here the input provided is A, voltage source VDD is provided at P and N is grounded. Thus by our expression . $Out = A.0 + A'1 = A'$ (inverted). While logic 1 is passed as input , we can see the output is logic 0 ,which verifies the operation of inverter gate.

2.2.2 AND GATE

The logical AND gate which implemented is simple logical gate which has a value high (1) , both the pins of inputs are at being made to high (1). For any value of the input is at low (0) , we see that the overall output given of the gate used is being made to low(0) . [12] .The schematic is shown in Fig 2.4 :

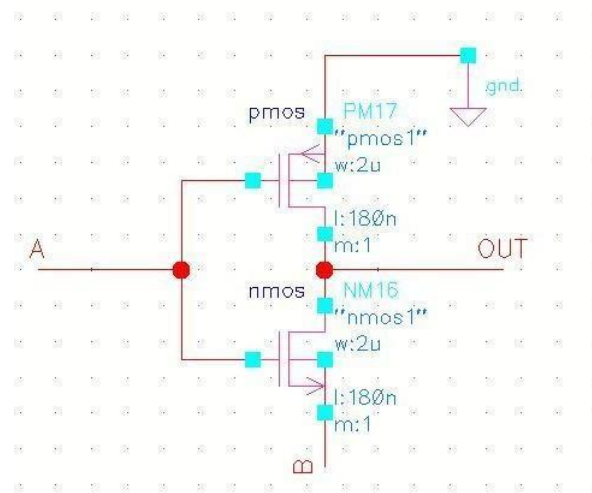


Fig. 2.4 : Schematic of AND Gate[1]

Timing waveform of the above circuit is being represented in the Fig 2.5 :

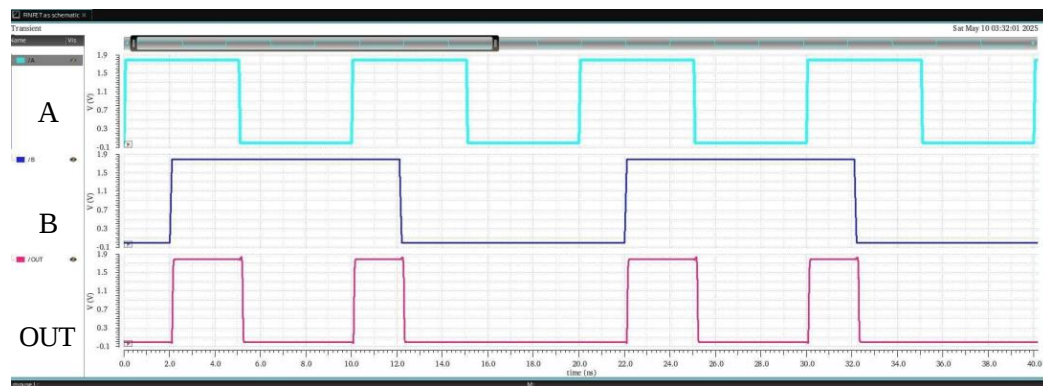


Fig. 2.5 : Transient Analysis of AND Gate

Here the input provided is A, P is grounded and N is provided with 2nd input (B). Thus by our expression, $Out = A.B + A'0 = AB$. From the above figure also, we can see when A is being kept high whereas the B is also being kept high, the output which is obtained is also being made high and in other cases its low. Thus, it verifies the operation of AND gate.

2.2.3 OR GATE

The logical OR gate which forms the basis of the logic circuits which performs the disjunction logical operation. Which is a fundamental block in combinational logic, used widely in digital systems for decision-making processes. The primary function of an OR gate is to make a logic high ('1') at output end if any one or more of the given inputs to it are high. It only outputs a logic low ('0') [1] when all inputs are low.

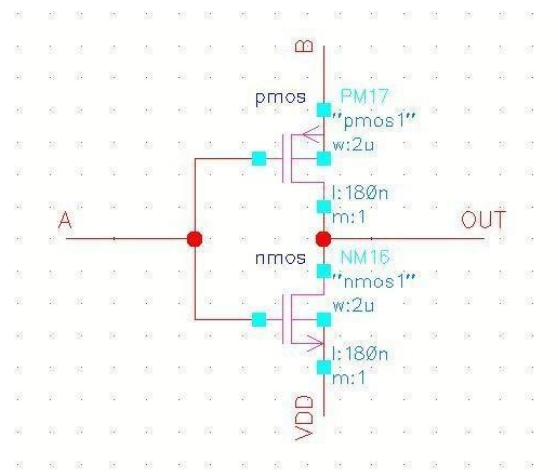


Fig. 2.6 : Schematic of OR Gate[1]

The timing waveform of the above circuit is shown in Fig

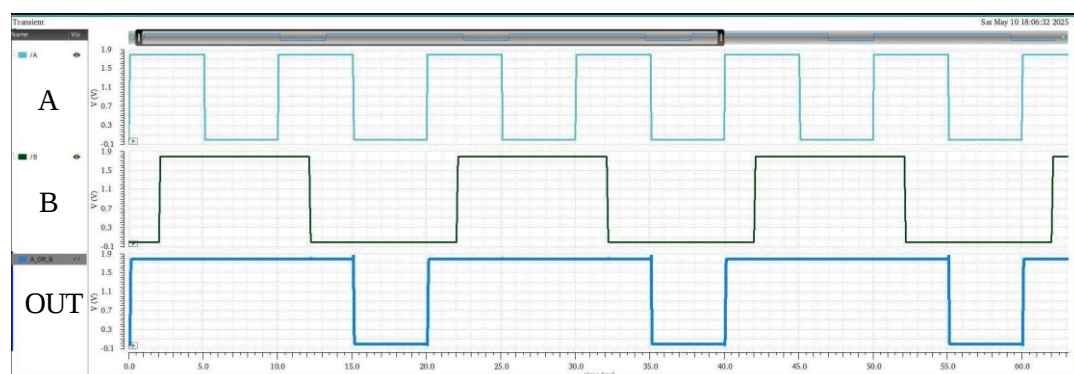


Fig. 2.7 : Transient Analysis of OR Gate

Here the input provided is A, N is connected with power supply (VDD) and P is connected with 2nd input (B). Thus by our expression . $Out = A'.B + A.1 = A+B$. In the figure also , we can see when either A or the other input B is high, the

output which is being obtained is also high , else it's low. Thus we can say , the OR operation is getting verified.

2.2.4 XOR GATE

There is another basic logic gate which is XOR (exclusive-OR) where the gate outputs give high (1) only in event that the true inputs are odd in number. It operates in an exclusive OR fashion, which means that if one and only one of its inputs is 1, it will output 1.

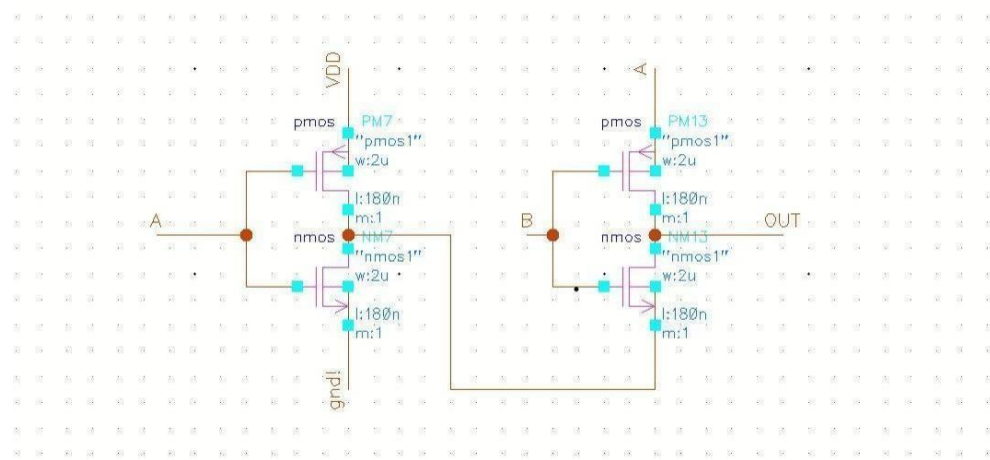


Fig. 2.8: Schematic of XOR Gate[1]

The timing waveform of the above circuit is shown in Fig 2.9 :

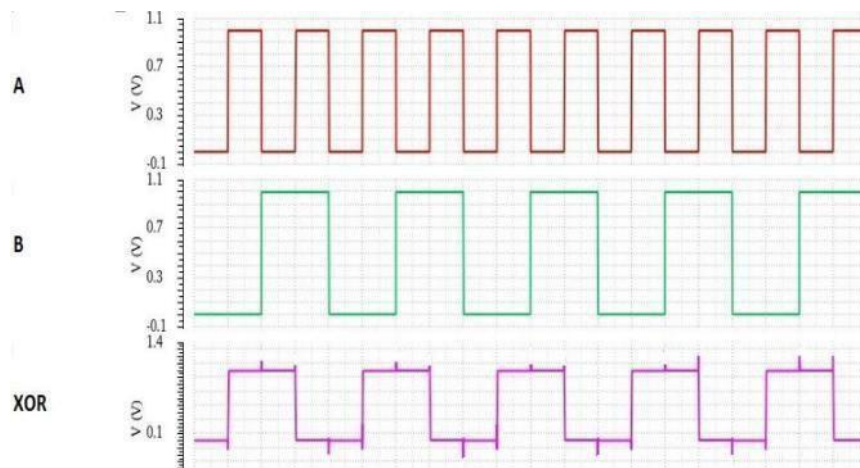


Fig. 2.9: Transient Analysis of XOR Gate

Here , we can see when either of the input is high and the other is low , we are getting output as high. And when both the inputs are high or low, the output is low. This matches the functionality of XOR operation and thus we can say XOR gate operation is verified.

2.2.5 MUX

It's a combinational circuit where Select lines decide which of the input should be passed as the Output . Equation of MUX can be shown as :

$$Y = S'd0 + Sd1 \quad (2.1)$$

Where d0 and d1 are the two inputs in the 2x1 mux and S is the Select line. A schematic is shown in Fig 2.10

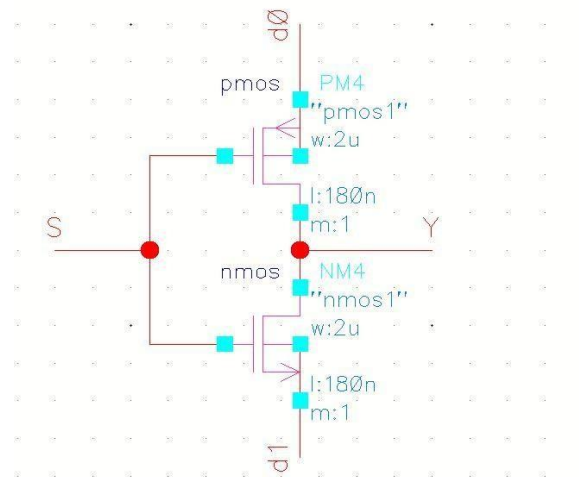


Fig. 2.10: Schematic of MUX

The timing waveform of the above circuit is shown in Fig 2.11

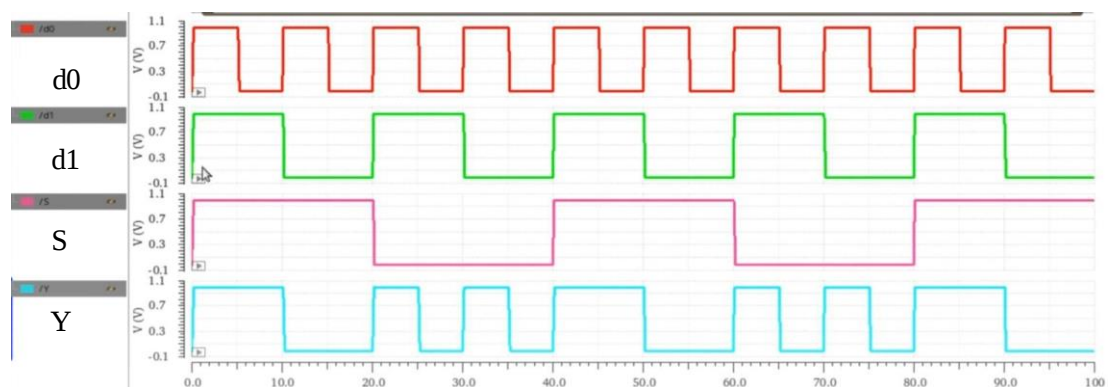


Fig. 2.11: Timing waveform of MUX

From Fig. 20 , we can see when $S=1$, the d1 value is passed in Y and when $S = 0$, d0 value is passed. This verifies that the above circuit is working as expected.

2.3 Transmission Gate Diffusion Input (TGDI) Technique

Here TGDI technique [12] is an extension of the GDI methodology, combining the main advantage of transmission gates with an compact structure of GDI logic. In TGDI, the basic cell utilizes transmission gates instead of traditional pass transistors, which consist of a combination of both of the NMOS as well as the PMOS transistors which are being handled by the complementary gate signals. This would allow for bidirectional signal flow with reduced voltage degradation, offering improved performance over conventional GDI in certain logic implementations. A TGDI cell generally includes three main control inputs: G (control signal), and P and N (data inputs applied through transmission gates). The outputs are being taken from the transmission gate's common connection area. By effectively using transmission gates, TGDI enhances signal integrity and supports full logic-level swing, which is especially beneficial in low-voltage digital circuits. Like GDI, TGDI is also being used in order to perform various logical functions such as AND, OR, XOR, and multiplexers with a reduction in the number of transistors in comparison to standard CMOS designs. The reduce in the number of transistor count translates into savings chip area, power usage, and propagation delay, making TGDI a promising approach for designing of our circuit with lesser power and a very good high performance.

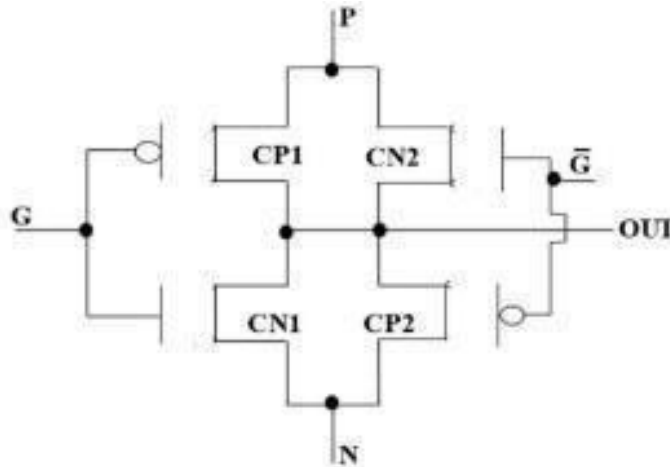


Fig. 2.12 : Basic TGDI Cell[12]

Here, when $G=0$, CP1 gate and CN2 gates get activated .Thus the $OUT = G'P$. Similarly, when $G=1$,CN1 and CP2 gets activated , thus the output is GN . So , combining both the equation we get the overall output as $G'P + GN$.. Using this logic ,we can implement various Boolean function. A table is provided below

Table 2.2 : Logic Function of TGDI Cell

P	N	G	OUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	AB	AND
B	1	A	A+B	OR
B	0	A	(AB)'	NAND
B'	0	A	(A+B)'	NOR

2.4 Simulation Using TGDI Technique

Here, we have simulated logic gates using the TGDI Techniques and analyzed their results like Power, Delay and Energy efficiency of the circuit.

2.4.1 INVERTER

An inverter is simple logic gate which reverses or inverts input signal. It is also referred to as a NOT gate. To put it another way, a logical low (0) will be the output obtained whereas on the contrary if input we are giving is a logical high (1).

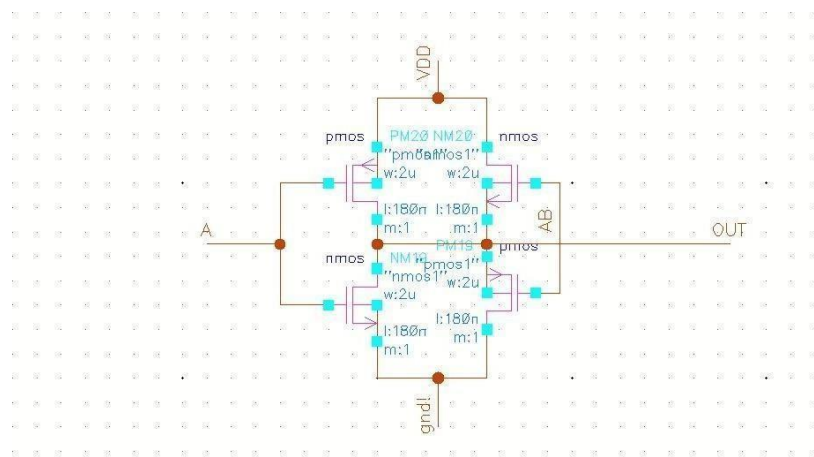


Fig. 2.13 : Schematic of Inverter Gate[12]

The timing waveform of the discussed circuit from the above is represented in Fig 2.14 :

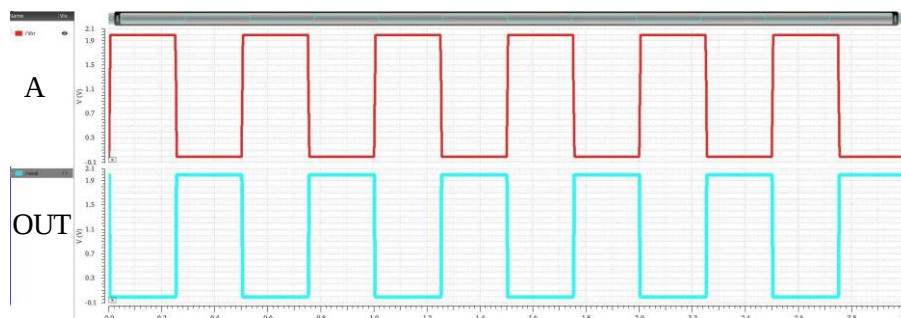


Fig. 2.14 : Timing waveform of Inverter Gate

Here the input provided is A, voltage source VDD is provided at P and N is grounded. Thus by our expression . $Out = A \cdot 0 + A' \cdot 1 = A'$ (inverted). While logic 1 is passed as input , we can see the output is logic 0 ,which verifies the operation of inverter gate

2.4.2 AND GATE

A logic gate whose outputs are being used as true or high (1) only during all of our given input values are being true or high(1). The AND gate would operate based on the basis that the output is true only when all input conditions are satisfied. The expression of logic in the AND gate is : $OUT = A \cdot B + A' \cdot 0 = AB$.

The Schematic representation of our circuit is being represented as follows :

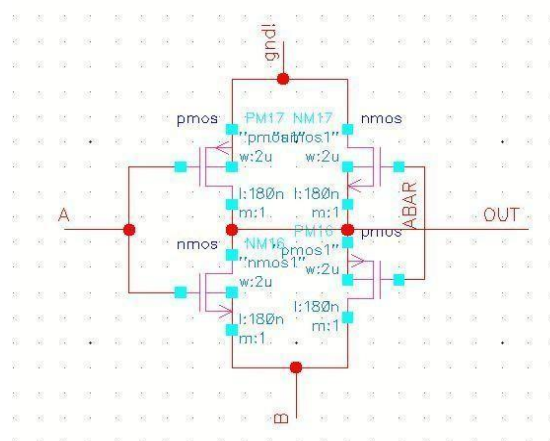


Fig. 2.15 : Schematic of AND Gate[5]

The timing waveform of the discussed circuit from the above is represented in Fig 2.16 :

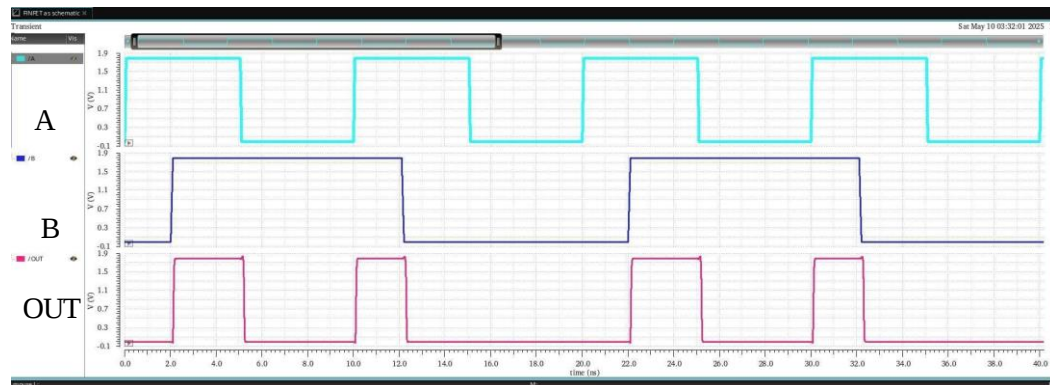


Fig. 2.16 : Timing waveform of AND Gate

Here the input provided is A, P is grounded and N is provided with 2nd input (B) . Thus by our expression . $Out = A.B + A'0 = AB$. From the above figure also , we can see that when A is high along with B is being high, the obtained value is being made high whereas in other cases its low. Thus , it verifies the operation of AND gate.

2.4.3 OR GATE

The logic gate which gives the output values to be true or high (1) if any one of its inputs is true or high (1). The OR gate output is false only in the case where all inputs are false. The logical expression for the output is: $Y = A + B$. In this logic, if either input A or B is 1, the output will also be 1. The only situation when the output is being made to 0 is when both of its inputs are 0. The output from the circuit is: $OUT = A.1 + A'.B = A+B$.

The representation of the circuit is shown in Fig 2.17 :

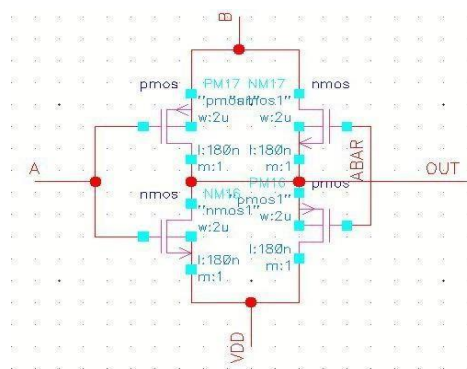


Fig. 2.17 : Schematic of OR Gate[5]

The timing waveform of the discussed circuit from the above is represented in Fig 2.18 :

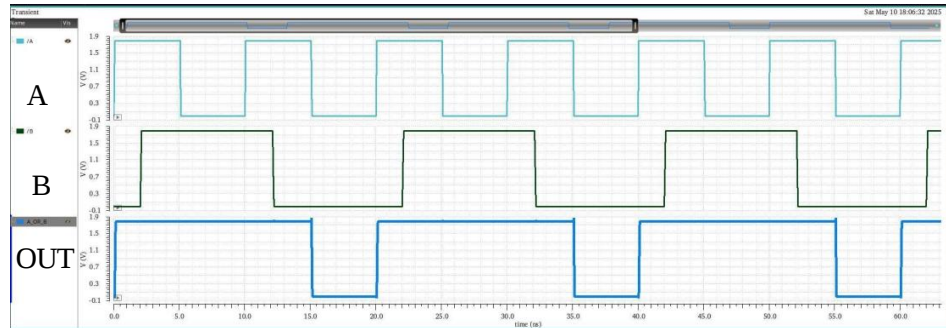


Fig. 2.18 : Timing waveform of OR Gate

Here the input provided is A, N is connected with power supply (VDD) and P is connected with 2nd input (B). Thus by our expression . Out = $A'.B + A.1 = A+B$. In the figure also , we can see when either A or the B is made high, the obtained output is also high , else it's low. Thus we can say , the OR operation is getting verified.

2.4.4 XOR GATE

There is another basic logic gate which is XOR (exclusive-OR) where the gate outputs give high (1) only in event that the true inputs are odd in number. It operates in an exclusive OR fashion, which means that if one and only one of its inputs is 1, it will output 1.

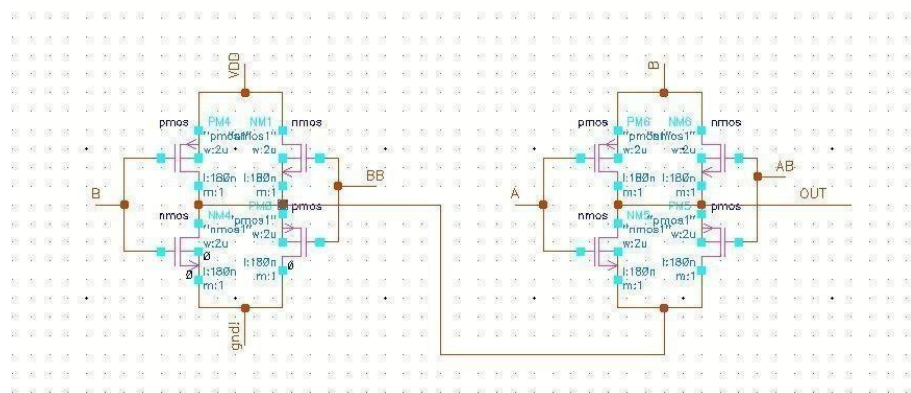


Fig. 2.19 : Schematic of XOR Gate[5]

The timing waveform of above logical circuit is as shown in the Fig 2.20 :

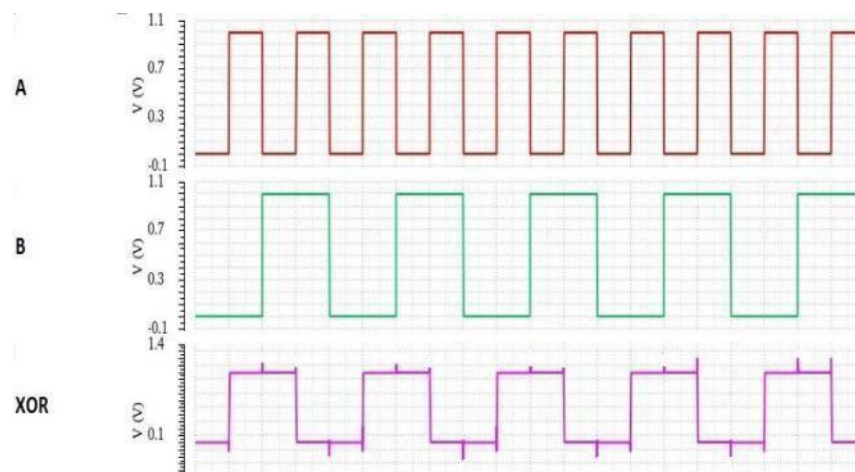


Fig. 2.20 : Timing waveform of XOR Gate

Here , we can see when either of the given input is going to high where as the other part is going to low which would make the output to go high . And when given inputs are high or low, the output is low. This matches the functionality of XOR operation and thus we can say XOR gate operation is verified.

2.4.5 MUX

It's a combinational circuit where Select lines decide which of the input should be passed as the Output . Equation of MUX can be shown as :

$$Y = S'd_0 + Sd_1 \quad (2.2)$$

Where d0 and d1 are the two inputs in the 2x1 mux and S is the Select line. A schematic is shown in Fig 2.21

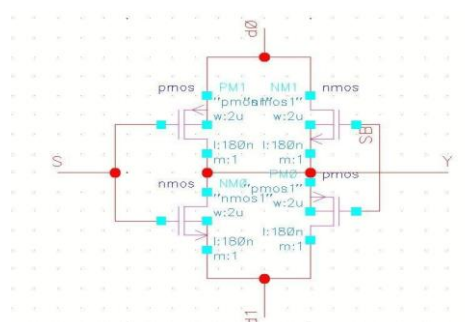


Fig 2.21 : Schematic of MUX

The timing waveform of the above circuit is shown in Fig 2.22

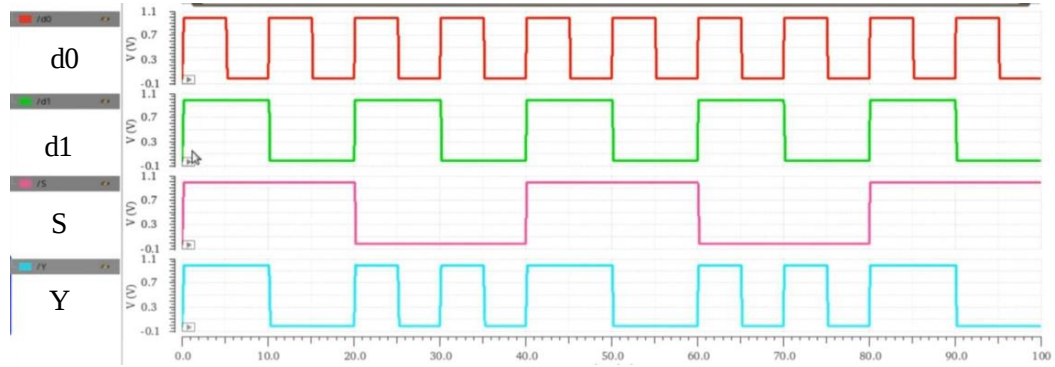


Fig 2.22 : Timing waveform of MUX using TGDI technique

From Fig. 20 , we can see when $S=1$, the d1 value is passed in Y and when $S = 0$, d0 value is passed. This verifies that the above circuit is working as expected.

2.5 Comparison

To evaluate the performance benefits of the GDI and TGDI techniques, several fundamental digital circuits were implemented using both methods. Key performance parameters such as the delay in propagation , consumption of power , and PDP, were have taken into account and measured each circuit. The comparison is presented in the table below, highlighting the improvements in delay and energy efficiency achieved by the TGDI approach over the conventional GDI design.

Table 2.3 : Comparison Table of Logic gates with GDI and TGDI techniques

Circuit	Delay(ps)		Power(uW)		PDP(pJ)	
	GDI	TGDI	GDI	TGDI	GDI	TGDI
Inverter	20.11	13.23	20.53	25.66	0.412	0.339
AND	22.78	14.98	58.45	73.06	1.330	1.094
OR	24.81	16.32	59.44	74.30	1.474	1.212
XOR	34.92	22.82	87.54	109.43	3.056	2.495
MUX	37.34	24.2	81.37	101.3	3.04	2.45

The comparative analysis of GDI and TGDI implementations for basic logic gates reveals significant improvements in delay and PDP with TGDI, albeit

with an increase in power consumption. For the inverter, the delay reduces from 20.11 ps in GDI to 13.23 ps in TGDI, while power consumption increases from 20.53 μW to 25.66 μW ; correspondingly, the PDP improves from 0.412 pJ to 0.339 pJ. Similarly, the AND gate exhibits a delay reduction from 22.78 ps to 14.98 ps, with power rising from 58.45 μW to 73.06 μW , and PDP decreasing from 1.330 pJ to 1.094 pJ. The OR gate shows a delay decrease from 24.81 ps to 16.32 ps, power consumption increase from 59.44 μW to 74.30 μW , and PDP improvement from 1.474 pJ to 1.212 pJ. For the XOR gate, delay is reduced from 34.92 ps to 22.82 ps, power increases from 87.54 μW to 109.43 μW , and PDP lowers from 3.056 pJ to 2.495 pJ. Additionally, MUX also shows a significant drop in delay from 37.34ps to 24.2 ps, and also PDP decrease from 3.04pJ to 2.45pJ. These results demonstrate that while TGDI circuits consume approximately 25% more power, they achieve about 30-35% faster operation and consequently better energy efficiency as reflected by lower PDP values.

2.6 Summary

In this chapter, the GDI and TGDI techniques were explored as efficient other ways to generally used CMOS logic in our low-power digital circuit design. Basic logic gates were designed using both GDI and TGDI methodologies, and their performances were evaluated on the basis of consumption of power, along with the delay in propagation, and PDP. The circuits which we have used have been implemented and simulated with the help of the Cadence Virtuoso tool at the 180 nm technology node, with an operating voltage of 2V and a transistor sizing of $W/L = 0.2 \mu\text{m} / 180 \text{ nm}$. From the data presented, it is evident that TGDI outperforms GDI in terms of both speed and power efficiency across all tested circuits. The reduction in delay and PDP is particularly notable in more complex circuits like the XOR gate and the inverter, where TGDI achieves lower delay and energy usage compared to GDI. A comparative analysis of the results demonstrated the effectiveness of TGDI in optimizing both dynamic performance and power consumption, which makes it to be a promising alternative in designing low-power and high-speed VLSI systems. This study forms the foundational basis for implementing larger digital blocks using these techniques in subsequent chapters.

CHAPTER 3

ARITHMETIC CIRCUIT

Chapter 3 highlights the analysis of arithmetic circuits, which are fundamental building blocks in digital systems. Here, the Full Adder, Ripple Carry Adder (RCA), and Carry Select Adder (CSA) have been implemented using the Gate Diffusion Input (GDI) and Transmission Gate Diffusion Input (TGDI) techniques. These designs were developed and simulated using the Cadence Virtuoso tool to evaluate their effectiveness in terms of critical performance metrics. The chapter presents a comparative study of the consumption in power, along with the delay, and power-delay product (PDP) of these adders, highlighting the trade-offs and advantages offered by the GDI and TGDI methodologies. The objective is to demonstrate how these low-power design techniques can optimize arithmetic circuit performance for energy-efficient digital applications.

3.1 INTRODUCTION

Arithmetic circuits form a basic for the components in the systems which are digital, responsible for the performance of the operations which are essential especially in the math like that of addition, subtraction, product and division of the binary numbers. These circuits are integral to the functionality of various computing platforms, ranging from simple micro controllers to complex supercomputers. Among these operations, addition is the most frequently used and serves as the foundation for implementing other arithmetic functions. Consequently, optimizing adder circuits is an important because it would enhance the overall metrics like that of the performance of our systems which are digital[13]

Arithmetic circuitry can be broadly categorized into combinational as well as the sequential types. Combinational circuits, such as adders, subtractors, multipliers, and comparators, produce outputs only on the basis of the present inputs. In contrast, sequential circuits, like accumulators and arithmetic logic units (ALUs), incorporate memory elements and their outputs depending both on the inputs of the previous and current states. The design of these circuits must consider factors like speed, power consumption, and silicon area, especially in the context of modern applications that demand high performance and energy efficiency.

To address these challenges, innovative logic design methodologies have emerged. One such approach is the GDI technique, which allows for the performance of functions which are complex in nature with fewer transistors in comparison to traditional CMOS designs. GDI would offer an edge in terms of reduction in the consumption of power, propagation delay, and silicon area. Another advancement is the TGDI technique, which combines the benefits of GDI with transmission gate logic to further enhance performance and signal integrity. These methodologies have paved the way for development of low-power, high-speed arithmetic circuits suitable for modern VLSI system.

3.2 Full Adder

The Full Adder is one of the essential component in our digital logic design and arithmetic circuitry, playing a central role in the binary addition process that underpins nearly every computational operation in digital systems. As digital devices process information in binary form, arithmetic operations like that of the addition, subtraction, multiplication, and division are all derived from basic binary addition. The full adder facilitates this process by enabling the combination of three input bits: two bits which are significant and a carry-in which is being taken from the previous stage. These outputs which are obtained are a sum bit along with the carry-out, which is propagated to the upcoming significant position in multi-bit addition. Unlike the half adder, which is limited to handling only two input bits, the full adder's inclusion of the carry-in input makes it suitable for constructing more complex adder circuits, such as Ripple Carry Adders, Carry Look-Ahead Adders, and Carry Select Adders, which are used to perform operations on multi-bit binary numbers. The logical expressions defining a full adder's output are typically realized using fundamental logic gates like XOR, AND, and OR. The sum is obtained by a three-input XOR operation, and the carry-out is calculated using a combination of AND and OR gates. These expressions can be translated into circuit-level designs using CMOS or other logic design techniques, depending on the performance requirements.[13]

These are being widely regarded as the heart of arithmetic units because of its indispensable role in enabling basic and advanced operations within ALUs, digital processors, and custom VLSI circuits. Its metrics like that of the performance are being directly influencing the speed, area, and the overall efficiency of power of an entire digital system. As a result, numerous design optimizations have been explored to enhance the full adder's efficiency, especially in terms of reducing delay, minimizing consumption of power, along with lowering transistor count. In recent years, with these ever-incremental in the demand for a lower-power and a higher speed electronic devices particularly in portable and battery-operated systems— alternative logic design styles such as GDI and TGDI have emerged as promising solutions for full adder implementations. These methods aim overallly reduce the complexity of our given circuit while maintaining or even improving critical performance parameters. Consequently, the full adder has not

only maintained its relevance but has also become a focal point for ongoing research in low-power VLSI design.

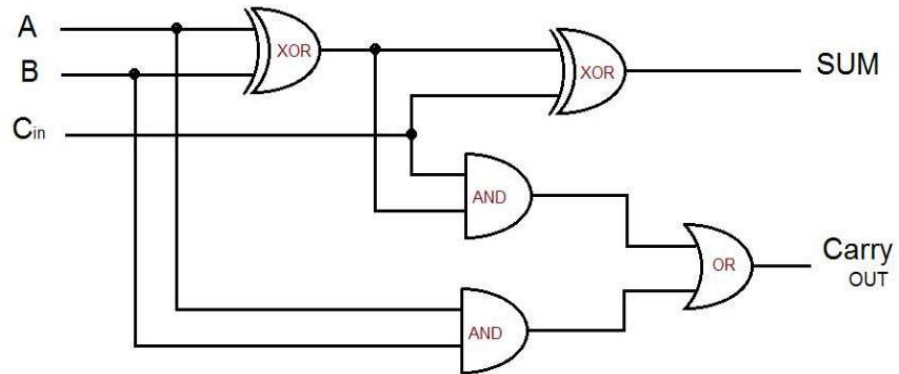


Fig. 3.1 : Block Diagram of Full Adder [14]

The truth table below details possible input combinations along with the output values corresponding to them, providing a comprehensive way to represent the circuit's logical behavior.

Table 3.1 : Truth Table of Full Adder

INPUT			OUTPUT	
A	B	C _{in}	SUM	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3.2.1 GDI Based Full Adder

Here, we have implemented a Full Adder circuit using the GDI technique, as introduced in Chapter 2. The Full Adder is a combination of XOR, AND and OR gates. By leveraging the GDI technique to implement these gates, the Full Adder design benefits from reduced transistor count, leading in the less consumption of power and faster switching speeds in comparison to conventional CMOS implementations. This approach ensures a compact and efficient arithmetic unit suitable for low-power digital systems.[5]

The schematic representation of the Full Adder using GDI technique is shown in Fig 3.2 :

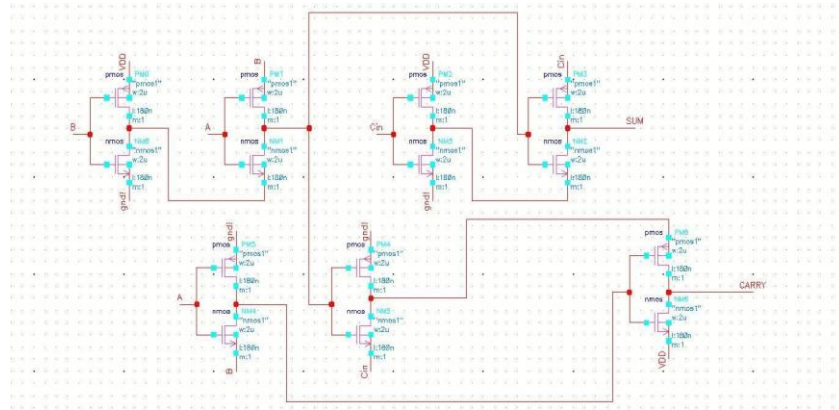


Fig. 3.2 : Schematic of Full Adder using GDI Technique

The functionality of the Full adder circuit with the usage of the GDI technique shown in Fig. 3.2 is tested through simulation using Cadence Virtuoso. All the transistors in the circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is being represented below in Fig 3.3.

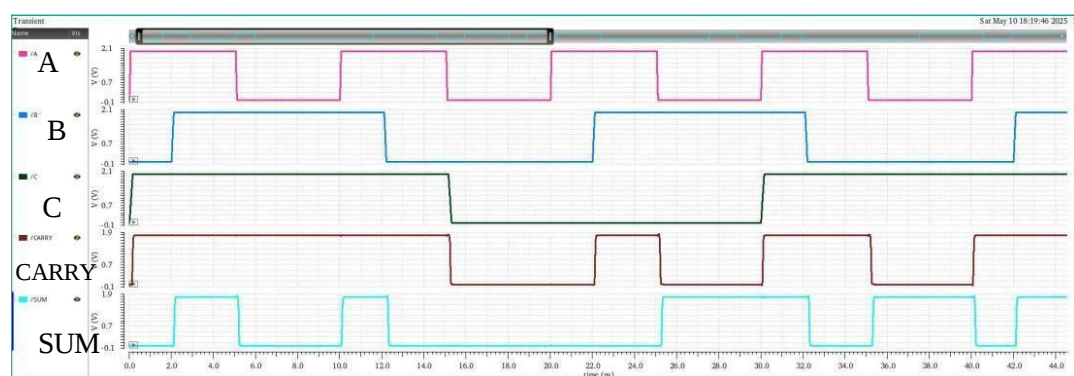


Fig. 3.3 :Timing waveform of Full Adder using GDI technique

In Fig 3.3 , we can see when A and B is high ,the summation of them is being made to a lower value and the carry is given as high. Similarly A , B , Cin is being high when the sum is being high and Carry is high . This verifies the

operation of Full Adder circuit.

In Fig. 3.4 the timing waveform have been zoomed to show the delay occurring among the input (Cin) and the output (Cout) is shown :

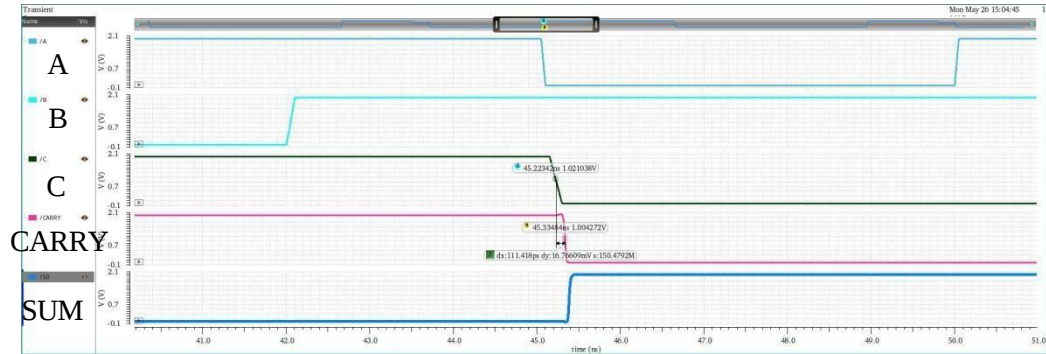


Fig. 3.4 : Propagation Delay of Full Adder using GDI technique

The delay and power consumption are observed 111.41ps and 260.49uW respectively.

3.2.2 TGDI Based Full Adder

Here, we have implemented a Full Adder circuit using the GDI technique, as introduced in Chapter 2. The Full Adder is a combination of XOR , AND and OR gates . By leveraging the TGDI technique to implement these gates, the Full Adder design have full voltage swing and faster switching speeds compared to conventional CMOS implementations and GDI implementations .. This approach ensures a compact and efficient arithmetic unit suitable for low-power digital systems[5].

The Schematic of Full Adder using TGDI technique is shown in Fig. 3.5 :

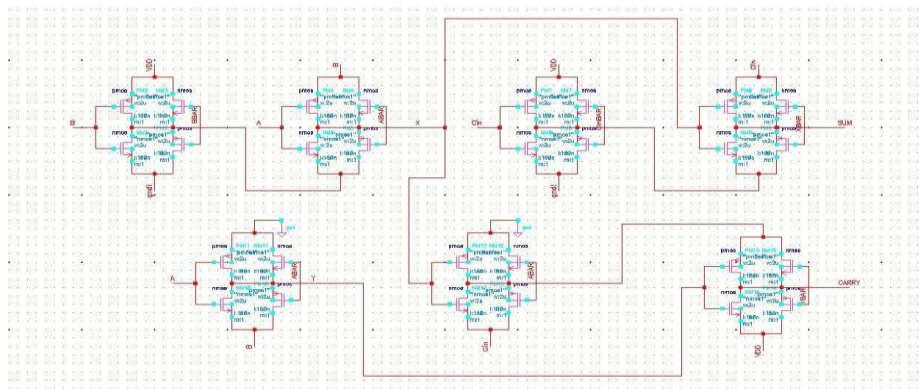


Fig. 3.5 : Schematic of Full Adder using TGDI technique

The functionality of an Full adder circuit using TGDI technique depicted in Fig. 3.5 is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2um/0.18um). The timing waveform is depicted in Fig 3.6

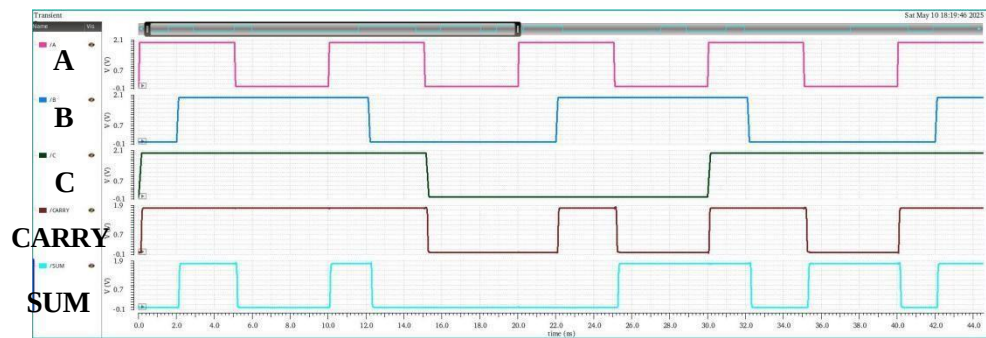


Fig. 3.6 : Timing Waveform of Full Adder using TGDI technique

In Fig 3,6 , we can see when A and also the B is high ,the obtained sum is being made to low whereas the obtained carry is being made to high. Similarly A , B , Cin is high , the Sum which is being obtained is being made high and Carry also is high . This verifies the operation of Full Adder circuit.

In Fig 3.7 , we have zoomed the timing waveform to show the delay between the input (Cin) and the output (Cout) :

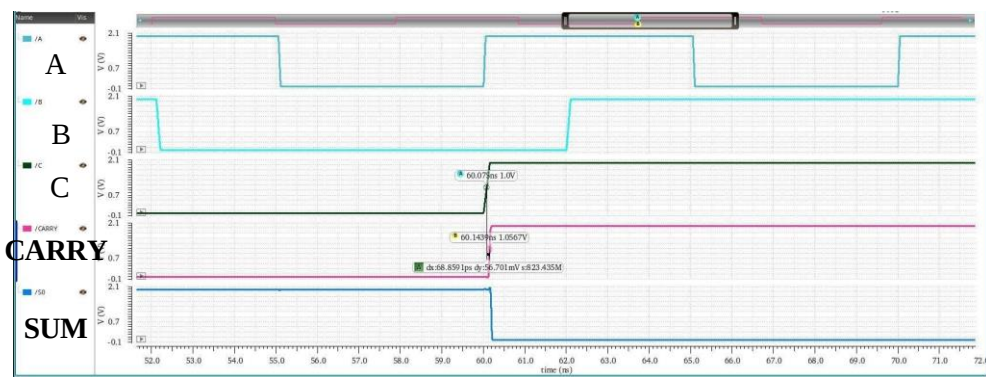


Fig. 3.7 : Propagation Delay of Full Adder using TGDI technique

From Fig. 3.7 , we can observe delay and power consumption are 68.85ps and 325.61uW respectively.

3.2.3 Comparison

To evaluate the performance differences between the conventional GDI and the proposed TGDI logic styles, key parameters like that of consumption of power, also with the delay in propagation, and PDP were analyzed. These comparative results are summarized in the table below.

Table 3.2 : Comparison Table of Full Adder using GDI and TGDI technique

Parameters	GDI	TGDI
Power	260.49 μ W	325.61 μ W
Delay	111.41ps	68.85ps
Power Delay Product	29.02f J	22.42f J

In the comparative analysis of GDI and TGDI circuits, it is observed that while GDI offers lower power consumption at 260.49 μ W compared to 325.61 μ W in TGDI—making it approximately 20% more power-efficient—the TGDI circuit significantly outperforms GDI in terms of speed and energy efficiency. TGDI achieves a much lower propagation delay of 68.85 ps versus GDI's 111.41 ps, reflecting a 38.2% improvement in speed. Additionally, the Power-Delay Product (PDP) of TGDI is 22.42 fJ, which is 22.7% lower than the 29.02 fJ observed in GDI, indicating a substantial gain in energy efficiency. Therefore, although GDI is preferable for ultra-low-power applications, TGDI proves to be a more optimal choice for the high speed as well as the energy-conscious designs, offering a better balance between performance and efficiency.

3.3 Ripple Carry Adder (RCA)

The RCA [3] is a basic and one of the simplest of binary adders, constructed by cascading multiple full adder units. Each full adder in the chain adds corresponding bits from two input operands along with the carry-in obtained from our previous stages. These carry-out from each full adder becomes the carry-in for our next, making the signal of carry to "ripple" throughout the adder stages which starts from our least significant bit (LSB) to the bit which is most significant (MSB). While the RCA's straightforward design makes it easy to implement and understand, it suffers from a significant drawback: propagation delay. Since each of the full adder must have to wait for the carry-in from its previous ones, the overall addition time increases linearly with the number of bits. This delay becomes a bottleneck in high-speed computing applications, where rapid arithmetic operations are essential. Despite its limitations, the RCA remains relevant in scenarios where simplicity and low power consumption are prioritized over speed. Moreover, advancements in logic design techniques, such as GDI and TGDI, have been applied to RCAs to

mitigate delay issues and enhance performance. By optimizing the design of individual full adders within the RCA, it's possible to achieve a balance between speed, power efficiency, and circuit complexity.

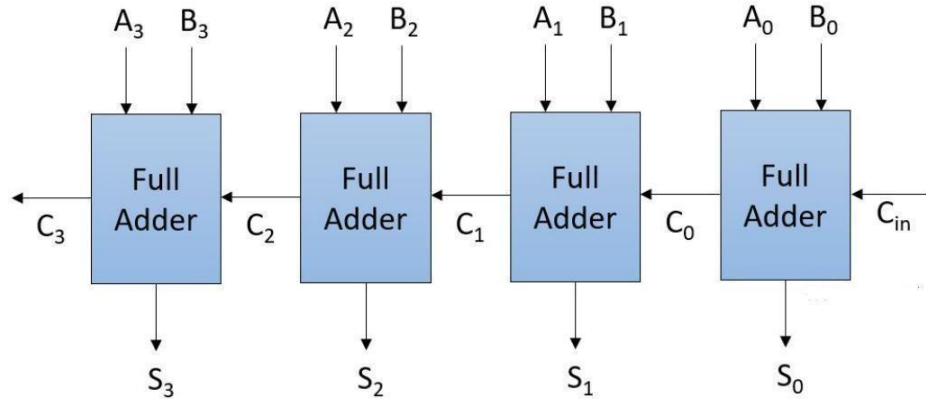


Fig. 3.8 : Block Diagram of 4 Bit Ripple Carry Adder (RCA)[3]

3.3.1 Working Principle

A 4-bit RCA is a circuit where we have designed to make summation of two 4-bit numbers in the binary form using a series of 1-bit full adders which are being connected in a sequence. Each of the full adder in the chain are being responsible for the addition of corresponding bits from the input operands along with carry from the previous stage. The term "ripple" refers to the manner in which the output of carry from each full adder propagates or ripples through to the next. In the RCA the fundamental block is the 1-bit full adder, which takes three inputs where two of them are the operand bits A and B , and along with that a carry-in bit called C_{in} . These would give us two outputs, they are bit of sum S along with a bit of carry-out C_{out} . The sum is being formulated with the help of the equation:

$$S_i = A_i \oplus B_i \oplus C_i \quad (3.1)$$

where $\oplus$ denotes the XOR operation.

The carry-out from each stage is computed as:

$$C_{i+1} = (A_i B_i) + (B_i C_i) + (A_i C_i) \quad (3.2)$$

This expression ensures that there is a carry being formed if at least two of the input bits being high (logic 1). For a 4-bit adder, the inputs are denoted as $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ and the sum outputs as $S = S_3S_2S_1S_0$. The carry-out of each full adder becomes the carry-in of the next stage. The initial carry-in C_0 is usually set to 0. The structure can be broken down into four stages: Let A_i and B_i be

the i th bits of the input binary numbers, and C_i be the carry-in for stage i :

$$\text{Sum}_i = A_i \oplus B_i \oplus C_i \quad (3.3)$$

$$C_{i+1} = (A_i \cdot B_i) + (C_i \cdot (A_i \oplus B_i)) \quad (3.4)$$

The total delay (T_{RCA}) of a 4-bit Ripple Carry Adder is:

$$T_{\text{RCA}} = 4 \times T_{\text{FA}} \quad (3.5)$$

where T_{FA} is the propagation delay of a single full adder.

3.3.2 GDI Based RCA

Here, we have implemented a RCA circuit with the GDI technique, as introduced in Chapter 2. The RCA consisting of a cascade of Full Adder cells where we take carry output from each stage is propagated to the next. By utilizing the GDI technique to design each Full Adder cell within the RCA, the overall circuit benefits from a significant reduction in transistor count, resulting in lower consumption of power and increased switching speed in comparison to traditional CMOS based RCA designs. This makes the GDI-based RCA an efficient and compact solution for performing fast arithmetic operations in low-power digital applications.

The schematic of 4 bit Ripple Carry Adder using GDI technique is being depicted as below

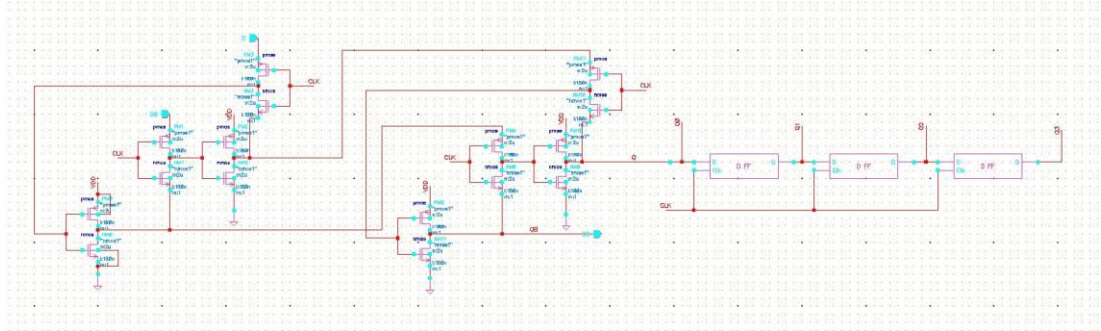


Fig. 3.9 Schematic of 4 Bit RCA

Here, four Full Adders are cascaded to form the overall structure. An internal schematic of one Full Adder is shown to illustrate its design and operation.

The functionality of the 4 Bit RCA circuit using GDI technique shown in Fig. 3.9 is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μm technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration

are (2um/0.18um). The timing waveform is shown in Fig 3.10

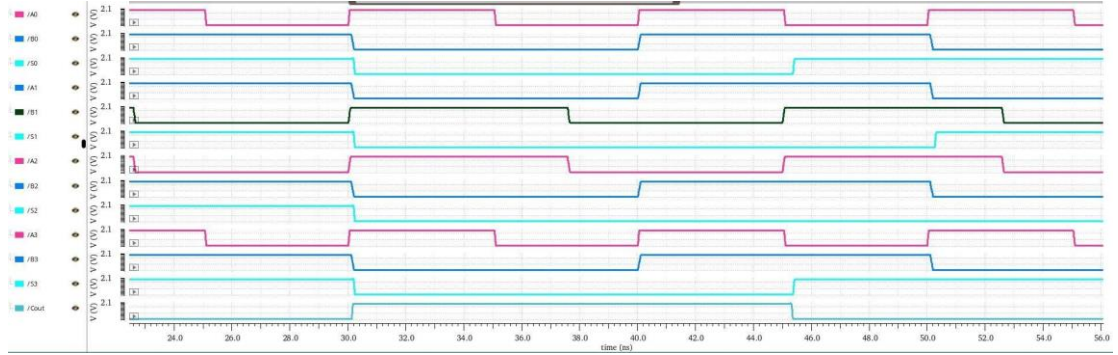


Fig. 3.10 : Transient Analysis of 4 Bit RCA

In Fig 3.10, we can see that $SUM_i = A_i \oplus B_i \oplus C_i$ and $C_{i+1} = (A_i \cdot B_i) + (C_i \cdot (A_i \oplus B_i))$ is working as expected. When $A_0 = B_0 = C_0 = 1$ (high), then $S_0 = 1$ (high) and C_1 is (1) high. Thus, we can say the Full Adder operation is verified. Here 4 Full Adders are cascaded to get the final Cout.

Delay Calculation of 4 Bit Ripple Carry Adder circuit :

As discussed in eq (3.6), the total delay for 4 Bit Ripple Carry Adder is :

$$T_{RCA} = 4 \times T_{FA}$$

where T_{FA} is the propagation delay of a single full adder.

In chapter 3.2.2, we have calculated delay of Full Adder = 111.41ps.

Thus, Total Delay = $4 \times 111.41\text{ps} = 445.64\text{ps}$

Additionally, the power observed for the circuit is : 1023.6 uW

3.3.3 TGDI BASED RCA

Here, we have implemented a RCA circuit using the TGDI technique, which builds upon the GDI approach introduced in Chapter 2. In the TGDI based RCA, transmission gates are integrated within each Full Adder cell to realize the required logic functions, ensuring full voltage swing and improved signal integrity. This approach overcomes common voltage degradation and noise margin limitations seen in pure GDI circuits. The bidirectional operation of transmission gates

enhances signal propagation, thereby reducing the carry delay across the stages of the RCA. The enhanced driving capability offered by transmission gates makes the TGDI based RCA a robust and efficient choice for high-speed, low-power digital arithmetic units.

The Schematic of 4 Bit RCA using TGDI technique is shown in Fig 3.11

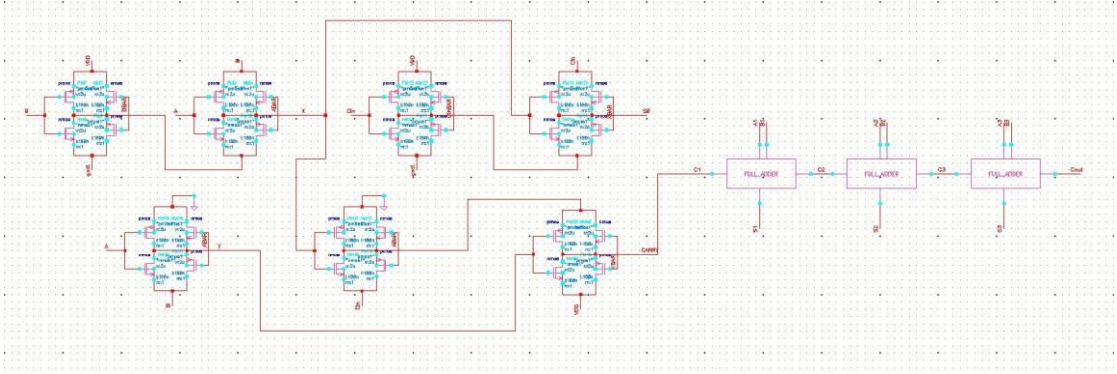


Fig. 3.11 : Schematic of 4 Bit RCA using TGDI technique

Here, four Full Adders are cascaded to form the overall structure. An internal schematic of one Full Adder is shown to illustrate its design.

The functionality of the 4 Bit RCA circuit using TGDI technique shown in Fig. 3.12 is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is shown in Fig 3.12

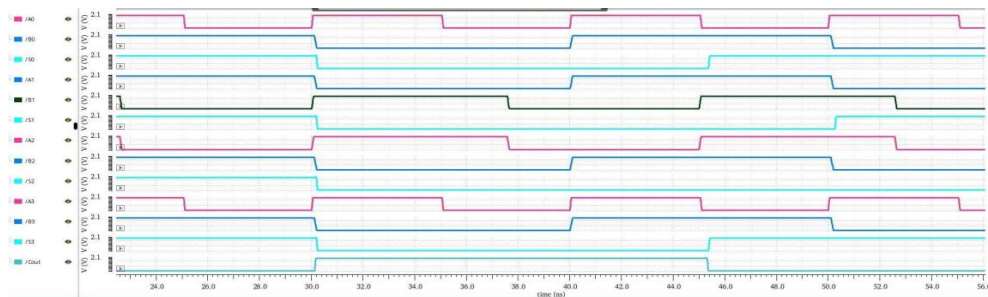


Fig. 3.12 : Transient Analysis of 4 Bit Ripple Carry Adder (RCA) using TGDI technique

In the above figure , we can see that $(SUM)_i = A_i \oplus B_i \oplus C_i$ and $C_{i+1} = (A_i \cdot B_i) + (C_i \cdot (A_i \oplus B_i))$ is working as expected . When $A_0 = B_0 = C_0 = (1)$ high , then S_0

= 1 (high) and C_1 is (1) high. Thus, we can say the Full Adder operation is verified. Here 4 Full Adder are cascaded to get the final Cout.

Delay Calculation of 4 Bit Ripple Carry Adder circuit :

As discussed in eq (3.6), the total delay for 4 Bit Ripple Carry Adder is :

$$T_{RCA} = 4 \times T_{FA}$$

where T_{FA} is the propagation delay of a single full adder.

In chapter 3.3.2 , we have calculated delay of Full Adder = 68.85ps

Total Delay = 4 x 68.85ps = 275.4 ps

The Power observed for the circuit is : 1302.4 uW

3.3.4 Comparison

To assess the performance improvements achieved by the TGDI circuit over the conventional GDI design, key metrics including consumption of power , along with the delay in propagation as well as the PDP were evaluated. The following table presents a comparative analysis based on these parameters.

Table 3.3 : Comparison Table of RCA using GDI and TGDI technique

Parameters	GDI	TGDI
Power	1023.6uW	1302.4 uW
Delay	445.64ps	275.4ps
Power Delay Product	456.28 f J	356.7 f J

In the analysis 4 bit RCA, the GDI technique exhibits lower power consumption at 1023.6 μ W, compared to 1302.4 μ W in TGDI, resulting in a 21.4% improvement in power efficiency. However, TGDI demonstrates a significantly faster performance, with a propagation delay of 275.4 ps, which is 38.2% faster than the 445.64 ps observed in GDI. The Power-Delay Product (PDP) further highlights TGDI's superiority in energy efficiency, achieving 358.76 fJ compared to 456.28 fJ in GDI an improvement of 21.3%. These results reinforce the advantage of TGDI in terms of an highly performing application where it has speed along with the energy optimization which is critical.

3.4 Carry Select Adder (CSA)

The CSA [15] is an efficient adder architecture which is being made to overcome the delay limitations of traditional RCAs. In an RCA, should keep on waiting for the carry coming from the previous stage, resulting in a linear increase in delay with the number of bits. This carry propagation bottleneck makes RCAs unsuitable for high-speed arithmetic operations. The CSA addresses this issue by dividing the input bits into multiple segments. Each segment performs two parallel additions here one assumes that the carry coming is zero whereas the other assumes that it is one. Once actual carry is obtained from the previous block, a multiplexer would select which one is the correct output. This parallelism significantly reduces overall delay, making CSA a popular choice for high-speed applications such as processors and digital signal processing units. However, the improved speed of CSAs comes at the cost of increased hardware complexity and power consumption, as each block requires duplicate logic for both carry-in conditions. To optimize power and area without compromising speed, modern VLSI design incorporates low-power techniques such as GDI and TGDI. The technique of GDI would allow for the implementation of a complex logic functionality by using fewer transistors than conventional CMOS design, which leads to reduced power dissipation and chip area. TGDI further enhances this by using transmission gates to ensure better voltage levels and reduced leakage currents.[11]

By integrating GDI and TGDI into CSA architecture, designers can significantly reduce power consumption and transistor count while maintaining high performance. This makes CSA with GDI/TGDI an ideal solution for power-sensitive and portable electronic systems.

The Block Diagram of a 4 Bit Carry Select Adder (CSA)

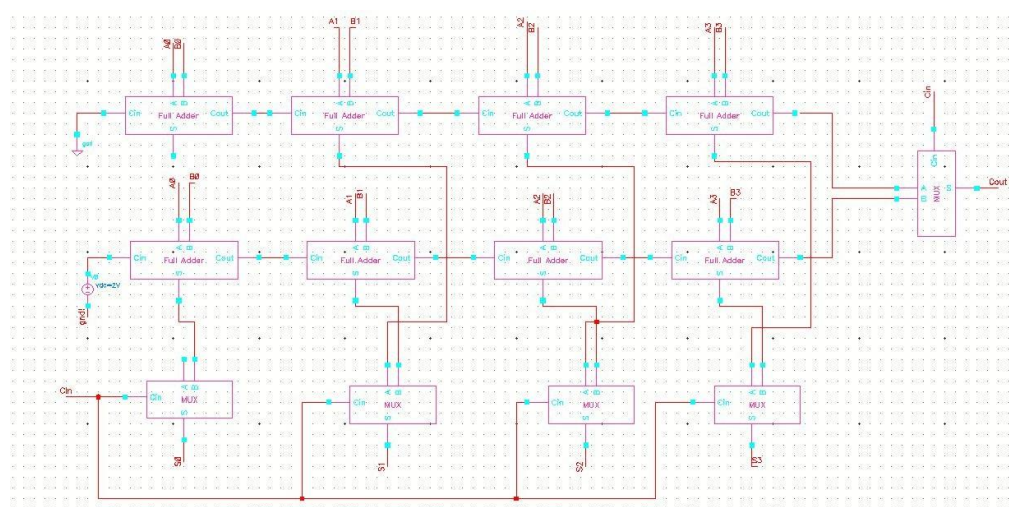


Fig 3.13 : Block Diagram of 4 Bit Carry Select Adder (CSA)

3.4.1 Working of CSA

The CSA improves the speed of binary addition by dividing the n -bit input into smaller segments. Each segment computes the sum and carry twice once assuming the incoming carry is 0, and once assuming it is 1. This method avoids waiting for the carry to ripple through every bit sequentially. Once the actual carry-in from the previous segment is known, a multiplexer selects the correct sum and carry outputs for that segment. Typically, the adder is split into about $\sqrt{n}$ segments, each of size $\sqrt{n}$, which reduces the overall delay. The total delay of the CSA can be approximated as [16]:

$$T_{CSA} = T_{FA} \times \sqrt{n} + T_{MUX} \times (\sqrt{n} - 1) \quad (3.7)$$

Where T_{FA} is the delay of a full adder, and T_{MUX} is the delay of the 2:1 multiplexer.

3.4.2 GDI Based 4 Bit CSA

Here, we have implemented a CSA circuit using the GDI technique introduced in Chapter 2. In the GDI-based CSA, full adder blocks and multiplexers are designed using GDI logic, which reduces transistor count and power consumption compared to conventional CMOS implementations. The parallel addition of segments assuming carry-in values of zero and one is efficiently realized with compact GDI-based full adders, while the selection of correct outputs is performed by GDI-based 2:1 multiplexers. This approach significantly reduces power dissipation, area, and propagation delay in the CSA architecture. The GDI technique enables a scalable and modular CSA design that is suitable for high-speed, low-power arithmetic units in modern VLSI systems.

The schematic of 4 bit CSA is shown in Fig. 3.14

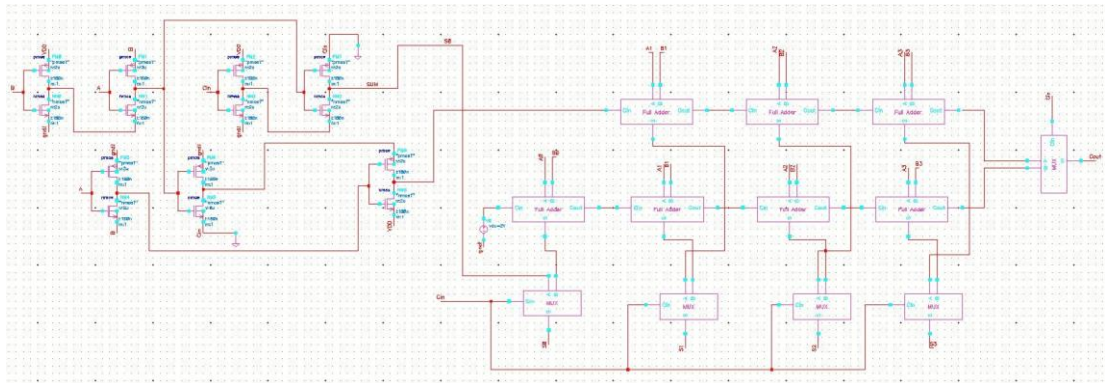


Fig 3.14 Schematic of 4 bit CSA using GDI Technique

Here, eight Full Adders and 5 MUX are used to form the overall structure. An internal schematic of one Full Adder is shown to illustrate its design.

The functionality of the 4 Bit CSA circuit using GDI technique shown in Fig. 3.12 is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is shown in Fig 3.15

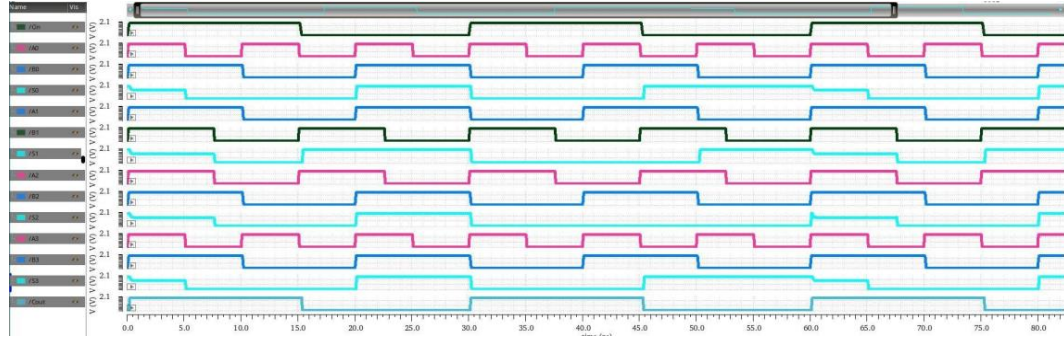


Fig 3.15 Timing Waveform of 4 bit CSA using GDI Technique

Delay Calculation :

In chapter 2 and chapter 3 , we have calculated the delay of Full Adder and MUX, using those values we may calculate the delay of 4 bit CSA circuit.

$$T_{FA} = 111.41\text{ps}$$

$$T_{MUX} = 37.34\text{ps}$$

Using eq (3.7), we can calculate the delay of 4 bit CSA circuit as follows :

$$\begin{aligned} T_{CSA} &= T_{FA} \times \sqrt{n} + T_{MUX} \times (\sqrt{n} - 1) \\ &= 111.41 \times \sqrt{4} + 37.34 \times (\sqrt{4} - 1) \\ &= 260.16\text{ps} \end{aligned}$$

Additionally , Power observed of the circuit = 2490.77 uW.

3.4.3 TGDI Based 4 BitCSA

Here, we have implemented a CSA circuit using the TGDI technique, which enhances the GDI approach discussed in Chapter 2. In the TGDI based CSA, both full adder blocks and multiplexers are realized using TGDI logic, integrating transmission gates to improve signal integrity and voltage swing. This design overcomes the voltage degradation and noise margin challenges associated with pure GDI circuits, delivering robust and reliable operation. This approach

significantly reduces propagation delay in the CSA architecture. The TGDI technique enables a scalable and modular CSA design that is suitable for high-speed, low-power arithmetic units in modern VLSI systems

The schematic of 4 bit CSA is shown in Fig 3.16

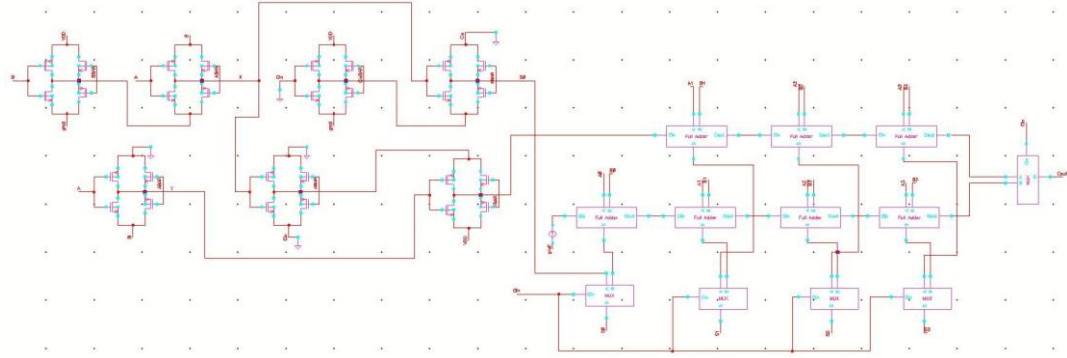


Fig 3.16 Schematic of 4 bit CSA using GDI Technique

Here, eight Full Adders and 5 MUX are used to form the overall structure. An internal schematic of one Full Adder is shown to illustrate its design.

The functionality of the 4 Bit CSA circuit using TGDI technique shown in Fig. 3.17, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is shown in Fig 3.17

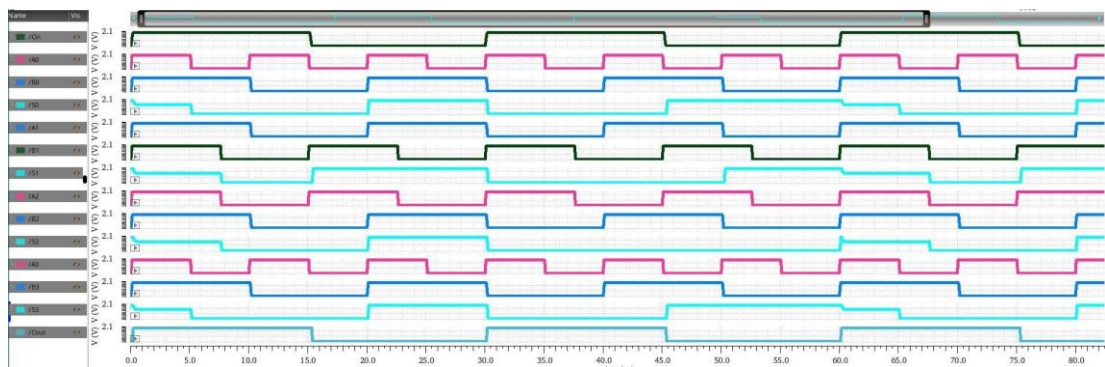


Fig 3.17 Timing Waveform of 4 bit CSA using GDI Technique

Delay Calculation :

In chapter 2 and chapter 3 , we have calculated the delay of Full Adder and MUX, using those values we may calculate the delay of 4 bit CSA circuit.

$$T_{FA} = 68.85\text{ps}$$

$$T_{MUX} = 24.2\text{ps}$$

Using eq (3.7), we can calculate the delay of 4 bit CSA circuit as follows :

$$\begin{aligned} T_{CSA} &= T_{FA} \times \sqrt{n} + T_{MUX} \times (\sqrt{n} - 1) \\ &= 68.85 \times \sqrt{4} + 24.2 \times (\sqrt{4} - 1) \\ &= 160.2\text{ps} \end{aligned}$$

Additionally , Power observed of the circuit = 3111.38 uW.

3.4.4 Comparison :

To assess the performance improvements achieved by the TGDI circuit over the conventional GDI design, key metrics including consumption of the power, delay of the propagation , and PDP were evaluated. The following table presents a comparative analysis based on these parameters.

Table 3.4 : Comparison Table of CSA using GDI and TGDI technique

Parameters	GDI	TGDI
Power	2490.77uW	3111.38uW
Delay	260.16ps	160.2ps
Power Delay Product	647.97f J	498.31 fJ

A 4-bit CSA was analyzed using GDI and TGDI logic styles. The TGDI based design consumed about 24.9% more power (3111.38 μW vs. 2490.77 μW) but achieved a 38.4% reduction in delay (160.2 ps vs. 260.16 ps) compared to GDI. As a result, its Power Delay Product (PDP) improved by 23.1%, reducing from 647.97 fJ (GDI) to 498.31 fJ (TGDI). Despite higher power usage, TGDI offers superior speed and energy efficiency, making it better suited for performance-critical applications.

3.5 Summary

This chapter presents the design and analysis of arithmetic circuits using GDI and TGDI logic styles. Initially, a Full Adder was implemented using both techniques as the foundational block. Using these Full Adders, two types of adders CSA and RCA were constructed. Each circuit underwent transient analysis to evaluate its dynamic performance. Key performance metrics including power consumption, propagation delay, and PDP were calculated for both logic styles. The simulation results revealed that TGDI based designs, while consuming slightly more power, demonstrated a significant improvement in delay and PDP compared to their GDI counterparts. This improvement makes TGDI a more efficient option for high-speed, low-energy digital arithmetic applications.

CHAPTER 4

IMPLEMENTATION OF D FLIP FLOP

Chapter 4 highlights the implementation of D Flip Flop using Gate Diffusion Input (GDI) and Transmission Gate Diffusion Input (TGDI) techniques. These designs were developed and being simulated with the help of the Cadence Virtuoso tool to assess their performance based on key parameters such as consumption in power, delay, and power-delay product (PDP). The chapter provides a comparative analysis of the GDI and TGDI based implementations, highlighting their respective benefits and trade-offs in achieving low-power and high-performance shift register designs for modern digital applications.

4.1 Introduction

The D Flip-Flop, also known as the Data or Delay Flip-Flop, is a fundamental building block in sequential digital circuits.[1] It is widely used for the storage as well as the transfer of data in synchronizing signals, and constructing memory elements in both combinational and sequential logic systems. The primary function of a D Flip-Flop is being used to capture and hold the value of the input data (D) at a specific edge of the clock signal—either rising or falling and then hold that value stable at the output (Q) until the next triggering clock edge. This characteristic makes the D Flip-Flop an essential element in designing registers, counters, state machines, and data storage units. In modern VLSI systems, the design of D Flip-Flops must meet stringent requirements in terms of speed, area, and, most importantly, consumption of the power. As technology scales down and devices become more compact, power dissipation has emerged as a critical concern, especially in battery-powered and portable electronics. Traditional CMOS-based implementations of D Flip-Flops, although robust, involve a relatively high number of transistors and experience substantial switching activity, both of which contribute significantly to dynamic and static power losses. To address these issues, several low-power design techniques have been proposed and developed over the years. Among them, GDI and TGDI have gained prominence due to their ability to reduce transistor count, switching activity, and overall power consumption without compromising functional accuracy. GDI is an innovative design technique that modifies the input configuration of standard CMOS gates. It enables the implementation of various logic functions with fewer transistors, thereby

minimizing dynamic power dissipation and saving chip area. In GDI-based D Flip-Flops, the reduced number of logic gates and short critical paths lead to enhanced speed and reduced energy consumption. [17]

On the other hand, TGDI builds upon the principles of GDI by incorporating transmission gates into the logic structure. Transmission gates act as bidirectional switches that pass both logic high and low levels efficiently, resulting in better signal integrity and reduced delay. In TGDI based D Flip-Flops, the use of transmission gates facilitates faster transitions and full voltage swing at the output, making them highly suitable for high-speed and low-voltage operations. In this thesis, both GDI and TGDI techniques have been employed to design and implement D Flip-Flops with the goal of achieving low power consumption, reduced silicon area, and improved delay performance. Simulation results of the proposed designs demonstrate that TGDI outperforms both GDI and traditional CMOS in terms of speed, while still maintaining power efficiency. The optimized flip-flop architectures serve as the foundational units in the development of advanced sequential circuits like SIPO registers and LFSRs discussed earlier in this chapter.

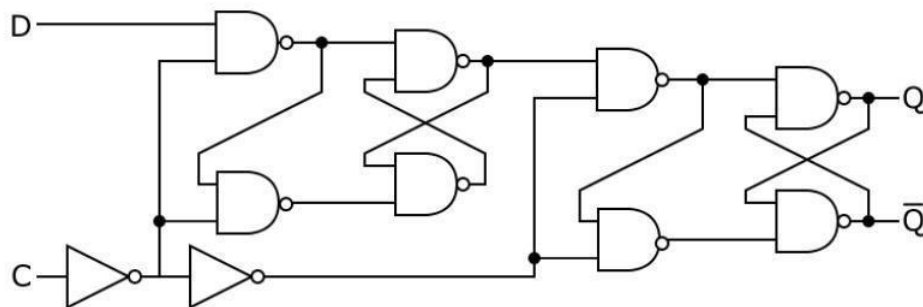


Fig. 4.1 : D Flip Flop[1]

Table 4.1 : Truth Table of D Flip Flop

CLK	D	Q	Q'
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

4.2 GDI Based D Flip Flop

Here, we have implemented the DFF using the GDI technique. The GDI method leverages a unique transistor-level configuration where the gate, source, and drain terminals of NMOS and PMOS transistors are independently controlled to realize complex logic functions with a lesser number of transistors in comparison to conventional CMOS designs. Internally, a typical DFF consists of logic gates such as AND, OR, and inverters arranged to store and transfer data based on the clock signal. In the GDI based DFF, these conventional gates are replaced by their GDI counterparts, which use a reduced number of transistors by sharing diffusion regions and minimizing transistor count. This structural modification results in a more compact circuit with lower power consumption and faster switching due to decreased capacitive loading. While the basic operation of the DFF remains unchanged, the GDI approach optimizes the internal gate implementation to improve overall efficiency, making it suitable for low-power and high-speed applications.[1], [17] The Schematic of D Flip Flop using GDI is shown below :

The schematic of positive edge triggered D FF is shown in Fig 4.2

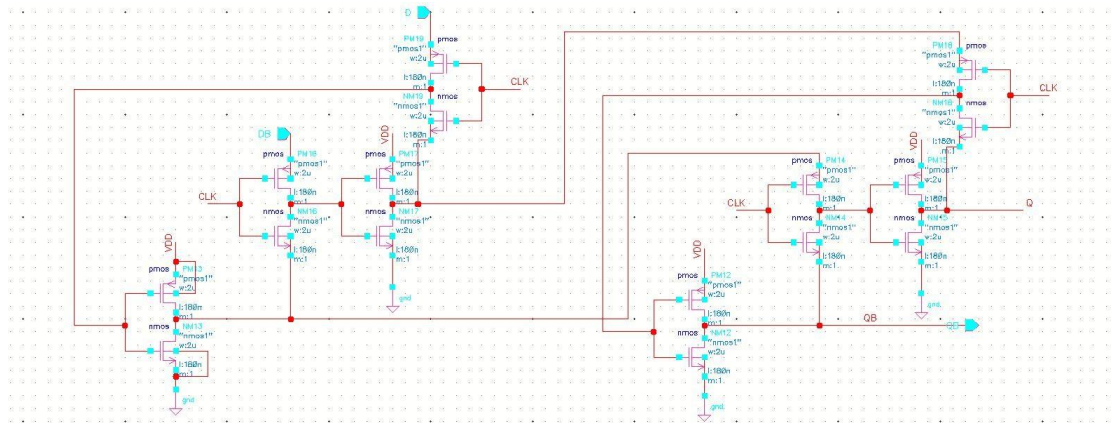


Fig. 4.2 : Schematic of D FF using GDI technique

The functionality of the positive edge triggered D FF circuit using GDI technique shown in Fig. 4.3, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2um/0.18um). The timing waveform is shown in Fig 4.3

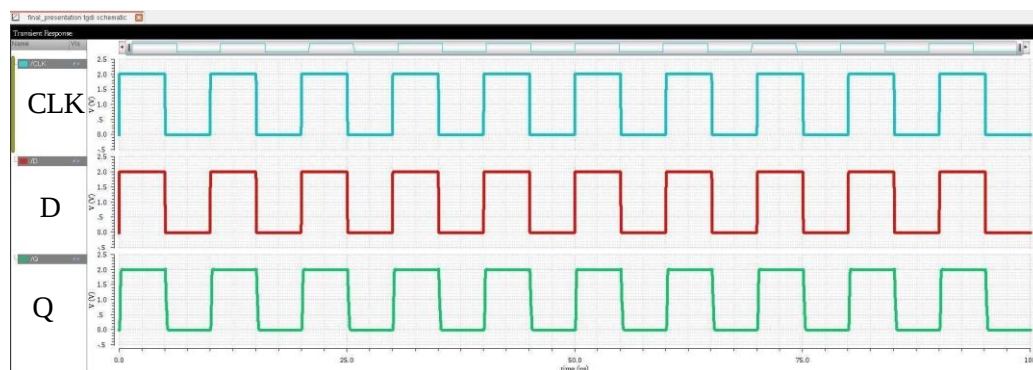


Fig. 4.3 : Timing waveform of D FF using GDI technique

Fig 4.3 is the timing waveform of a positive edge triggered D Flip Flop, we can see when D is high , Q is also high . This verifies that the circuit is working as expected.

The SETUP time analysis is shown in Fig 4.4

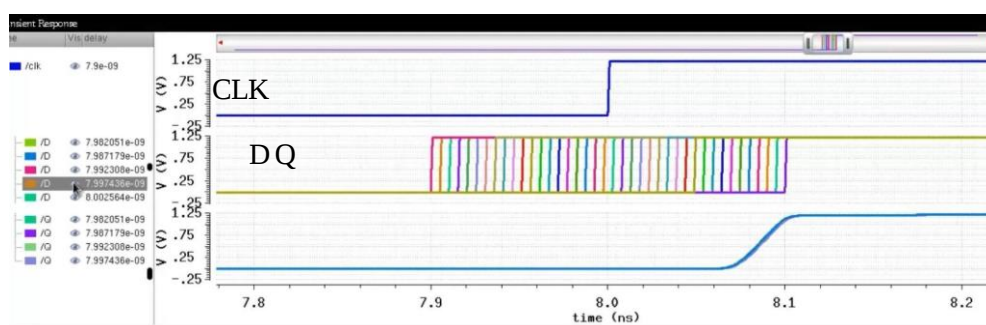


Fig. 4.4 : Setup Analysis of D Flip Flop using GDI technique

The timing waveform in Fig 4.3 has been zoomed to show the delay in Fig 4.5

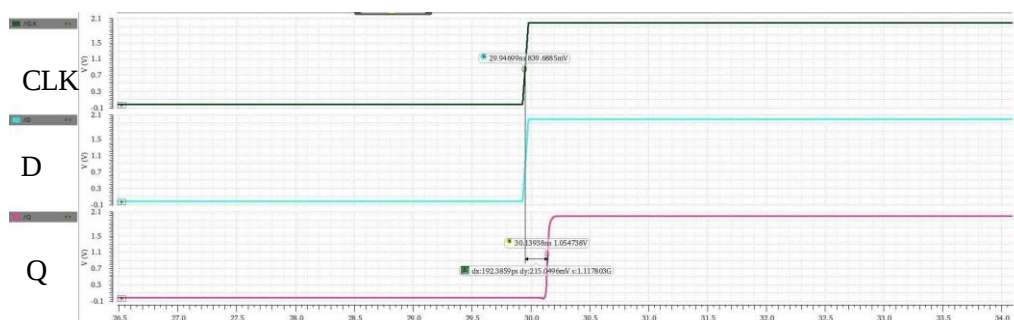


Fig. 4.5 : Propagation Delay of D Flip Flop using GDI technique

It may be observed from Fig 4.4 and Fig 4.5,

Setup Time = 97ps

Hold Time = 0

CLK-Q delay = 192.3ps

Thus ,delay of the D -FF = 192.3ps

The Power observed for the circuit is = 275uW.

4.3 TGDI Based D FF

Here, we have implemented the DFF using the TGDI technique, which extends the GDI approach by integrating transmission gates into the design. . In the TGDI based DFF, transmission gates are strategically placed in the data and clock paths to ensure reliable data storage and full voltage swing at the outputs. This modification improves signal integrity, reduces threshold voltage losses, and minimizes noise susceptibility compared to pure GDI designs. Additionally, TGDI based DFFs exhibit faster switching speeds due to the efficient charging and discharging of nodes through transmission gates, resulting in lower propagation delays. Overall, TGDI based D Flip-Flops offer an efficient, low-power, and high-performance solution suitable for modern VLSI applications where speed and power are critical.

Schematic Diagram of positive edge D Flip Flop is shown in Fig 4.6 :

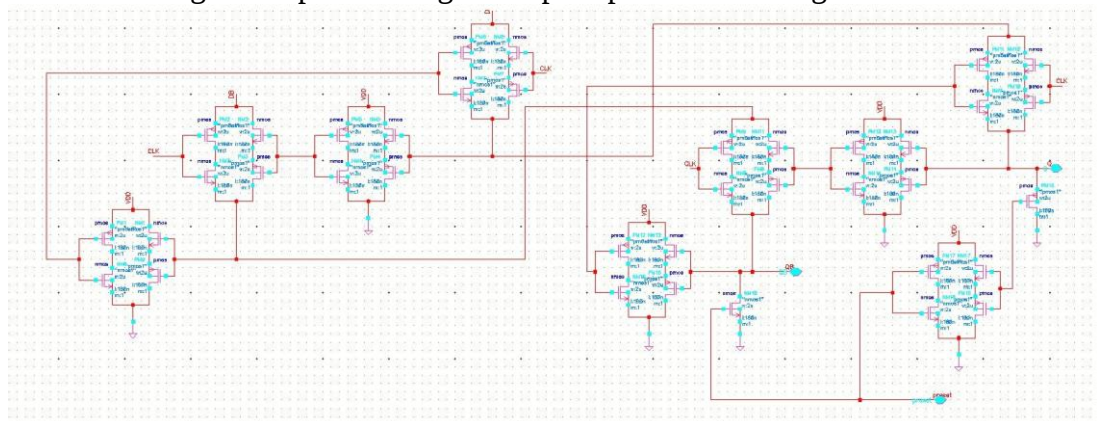


Fig. 4.6 :Schematic of D Flip Flop using TGDI technique

The functionality of the positive edge triggered D FF circuit using TGDI technique shown in Fig. 4.7, is tested through simulation using Cadence Virtuoso.

The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m).

The timing waveform is shown in Fig 4.7

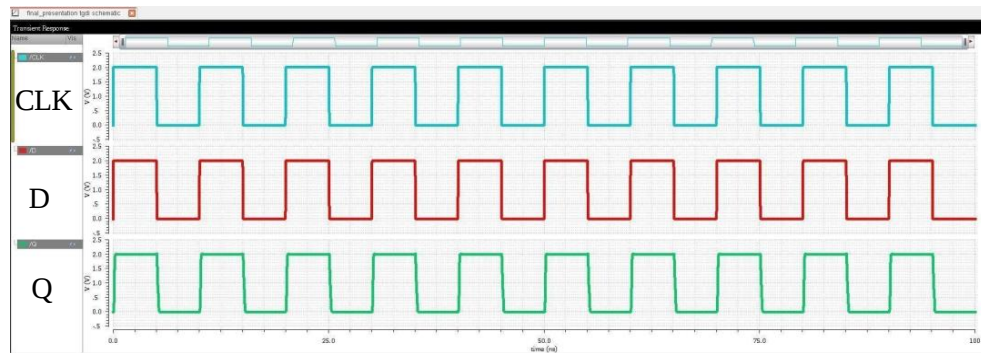


Fig. 4.7 :Timing waveform of D Flip Flop using TGD technique

Fig 4.7 is the timing waveform of a positive edge triggered D Flip Flop, we can see when D is high , Q is also high . This verifies that the circuit is working as expected.

The SETUP time is shown in Fig 4.8,

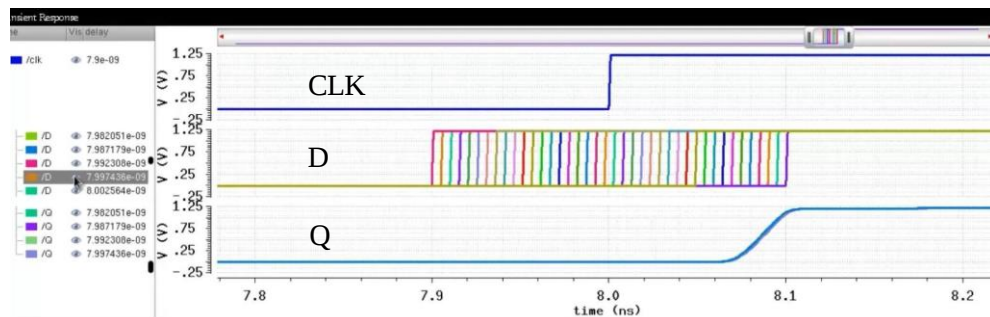


Fig. 4.8 Setup Time Analysis of D Flip Flop using TGD technique

The timing waveform in Fig 4.7 has been zoomed to show the delay in Fig 4.9

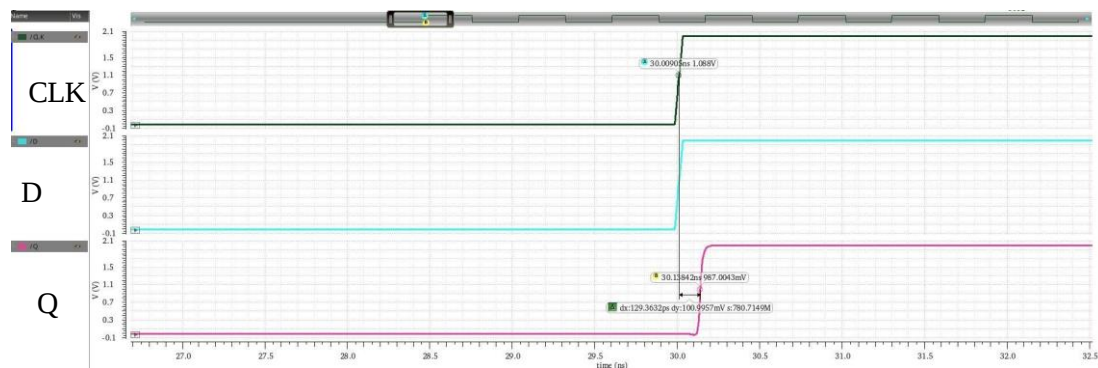


Fig. 4.9 :Propagation delay of D Flip Flop using TGDI technique

It may be observed from Fig 4.8 and Fig 4.9,

Setup Time = 62.4ps

Hold Time = 0s

CLK-Q delay = 129.3ps

Hence , Delay of the D -FF = 129.3ps

Additionally , the Power observed of the circuit : 343.8 uW

4.4 Comparison

To assess the performance improvements achieved by the TGDI circuit over the conventional GDI design, key metrics including power consumption, propagation delay, and PDP were evaluated. The following table presents a comparative analysis based on these parameters.

Table 4.2 : Comparison Table of D FF with GDI and TGDI technique

Parameters	GDI	TGDI
Power	275uW	343.8uW
Delay	192.3ps	129.3ps
Power Delay Product	52.9f J	44.4f J

The comparison shows that while GDI consumes less power (275 μW) than TGD (343.8 μW), TGD offers significantly lower delay (129.3 ps vs. 192.3 ps). As a result, TGD achieves a better Power-Delay Product (44.4 fJ vs. 52.9 fJ), making it more energy-efficient and suitable for high-speed, performance-critical applications despite the slight increase in power.

4.5 Summary

This chapter presented a comparative study of D flip-flop implementations using GDI and TGD techniques. Key performance like the consumption of power, delay in propagation, and PDP were analyzed in order to determine the suitability of each approach for low-power digital designs. The GDI-based flip-flop consumed 275 μW , while the TGD design consumed 343.8 μW , reflecting a 24.97% increase in power consumption. However, this power trade-off resulted in a significant speed improvement the TGD flip-flop achieved a delay of 129.3 ps, which is 32.77% lower than the GDI delay of 192.3 ps. Consequently, the TGD design also achieved a PDP of 44.4 fJ, compared to 52.9 fJ for the GDI design, resulting in a 16.06% improvement in energy efficiency. These results demonstrate that while TGD incurs slightly higher power usage, it offers substantial improvements in delay and overall energy efficiency. Thus, TGD proves to be a more balanced and performance-optimized solution for designing sequential circuits like D flip-flops in high-speed, low-power VLSI applications.

CHAPTER 5

SHIFT REGISTERS

Chapter 5 highlights the designing and analysis of shift register circuits, which are essential components in digital systems for data storage, transfer, and sequence generation. In this work, 4-bit Serial-In Parallel-Out (SIPO) and Linear Feedback Shift Register (LFSR) architectures have been implemented using Gate Diffusion Input (GDI) and Transmission Gate Diffusion Input (TGDI) techniques. These designs were developed and being simulated with the help of the Cadence Virtuoso tool to assess their performance based on key parameters such as consumption in power, delay, and power-delay product (PDP). The chapter provides a comparative analysis of the GDI and TGDI based implementations, highlighting their respective benefits and trade-offs in achieving low-power and high-performance shift register designs for modern digital applications.

5.1 Introduction

Shift registers are essential sequential logic circuits composed of cascaded D Flip-Flops, which is being used for the storage as well as the transfer of the data based on the clock signal. Each flip-flop in the register represents one bit of storage, and data is shifted from one stage to the next with every clock pulse. This clock-driven operation allows for precise control over data timing, making shift registers highly reliable for sequential data handling. They have a key and crucial role in various digital applications like that of a data buffering, serialization, and format conversion. For example here like in the systems of communication, the shift registers which are being used for the conversion of parallel data into the serial form for the transmission and later make it to parallel at the receiver end and in the digital signal processing we would help in the implementation of time delays, FIR filters, and register-based operations. In embedded systems, shift registers extend I/O capabilities and help in compact data storage and retrieval mechanisms.

The basic type of the shifting registers include SIPO, which takes in serial data and outputs it in parallel form, and LFSR, which use feedback logic to generate pseudo-random sequences. These configurations are critical in the applications like the pseudo random number generating, the detection of the error and the correction it, and cryptographic systems. Their versatility, simplicity of

design, and adaptability to various data formats make them indispensable components in modern digital design.

5.2 Serial In Parallel Out Register (SIPO)

In modern digital systems, the efficient handling, storage, and transfer of data which are one of the most critical factor for the determination of the overall performance and functionality of electronic devices. [18] Among various data storage and transfer components, shift registers would play an essential role because of their simplicity and versatility. A SIPO register is a particular kind of shift register which would take in data serially, a single bit at a time later the outputs then complete data simultaneously in parallel form. This characteristic makes SIPO registers especially useful in applications where data must be transmitted over limited input lines and then made available for parallel processing, such as microcontrollers, communication interfaces, digital displays, and embedded system designs. Typically, SIPO registers are implemented using conventional CMOS logic based on flip-flops connected in cascaded fashion. While CMOS technology is well established, it has challenges in terms of the consumption of power, transistor count, and circuit delay, particularly as digital device to scale down and in size and grow in complexity. The growing demand for portable, battery-powered, and high-speed devices has intensified the need for innovative circuit design techniques that reduce power consumption and chip area without compromising performance.[9]

In order to address the above shortcomings here the thesis explores the design and implementation of SIPO registers using GDI and TGDI techniques. GDI is a promising low-power design methodology that reduces transistor count by modifying the input configuration of transistors, thereby minimizing switching power and area. TGDI further enhances this approach by integrating transmission gates, which provide better signal integrity and faster switching speeds. These techniques have demonstrated an crucial and good improvement in the efficiency of the power along with the delay in comparison to the traditional CMOS logic, making them ideal candidates for shift register design in modern VLSI and FPGA environments. This research aims to analyze the architectural design of SIPO registers using GDI and TGDI methods, implement the circuits using hardware description languages, and simulate their performance in terms of consumption of power along with the delay in the propagation, also the area of the silicon. The results will be compared against conventional CMOS implementations to highlight the advantages and trade-offs of each technique. Through this work, the thesis contributes to advancing low-power and compact circuit design strategies, which are critical for the development of next-generation digital systems, including Internet of Things (IoT) devices, wearable technology, and other embedded applications where energy efficiency and compactness are paramount. In summary, the project provides a comprehensive study of SIPO registers with an emphasis on novel low-power design techniques. It aims to deliver optimized register architectures suitable for high-performance digital circuits, offering a valuable reference for researchers and engineers involved in the design of power-efficient

digital hardware.

The Block Diagram of 4 bit Serial In Parallel Out register is shown in Fig 5.1

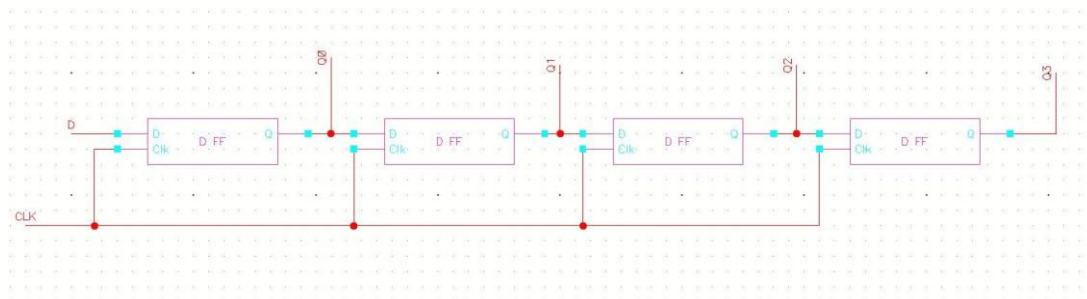


Fig. 5.1 : Block Diagram of 4 bit SIPO Register

The State Transition table of the above circuit is shown below :

Table 5.1 : State Transition Table of Serial In Parallel Out Register

CLK	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	1	0	0	1

5.2.1 Working of SIPO

A SIPO shift register which would be sequential and converts serial data input into parallel output. It comprises of a chain of flip-flops which are being connected like series, where each clock pulse shifts data by one bit into the register. After n clock cycles, corresponding to the different bits in register, the entire serial input word is available simultaneously at the parallel outputs. The key timing parameters affecting the performance of a SIPO register are the clock-to-Q delay (T_{clk-q}) the time for a flip-flop to propagate data after the clock edge—and the setup time (T_{setup}) the minimum time the input must be in a stable state before the clock edge. The clock period (T_{clk}) must be at least the sum of these delays to ensure reliable operation:[10]

$$T_{clk} \geq T_{clk-q} + T_{setup} \quad (5.1)$$

Because data is shifted sequentially through N flip-flops, the total delay to load the full data word and make all outputs valid is approximately:

$$T_{loading_delay} \geq N \times T_{clk} \quad (5.2)$$

In this thesis, the delay characteristics of SIPO registers implemented using GDI and TGDI techniques are compared. Although TGDI consumes higher power, it offers significantly lower clock-to-Q delay, enabling a shorter clock period and thus reducing the overall load time. Since consumption is being given as the product of power and delay which is being given by:

$$\text{PDP} = \text{Power} \times T_{\text{loading_delay}} \quad (5.3)$$

The reduction in delay provided by TGDI leads to lower overall energy usage despite the higher power consumption. This demonstrates the advantage of TGDI technology for high-speed, energy-efficient serial-to-parallel data conversion circuits.

5.2.2 GDI Based SIPO

Here, we have implemented a SIPO shift register by usage of the GDI technique, which enhances conventional CMOS logic by applying inputs differently to transistors to realize complex functions with fewer components. The GDI based SIPO register has been designed to efficiently receive serial data and output it in parallel. By leveraging the GDI approach, the design achieves significant reductions in count of the transistor, consumption of the power, and delay in propagation compared to traditional CMOS implementations. This results in a more better and compact along with efficient power sequential circuit without the competition of functionality. The GDI technique thus addresses the limitations of conventional CMOS by minimizing switching activity and silicon area, making it well-suited for low-power, high-speed digital systems, especially in portable and battery-operated devices.

The Schematic of 4 bit SIPO Register is shown in Fig 5.2 :

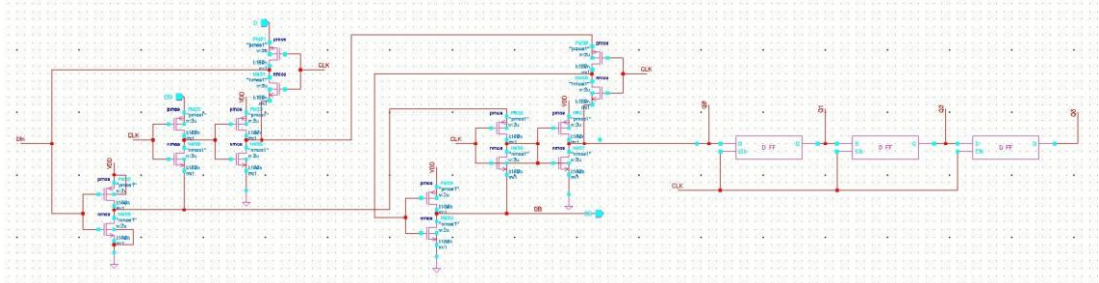


Fig. 5.2 : Schematic of 4 bit SIPO Register using GDI technique

The functionality of 4 bit SIPO register circuit using GDI technique shown in Fig.

5.2, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is being represented in Fig 5.3.

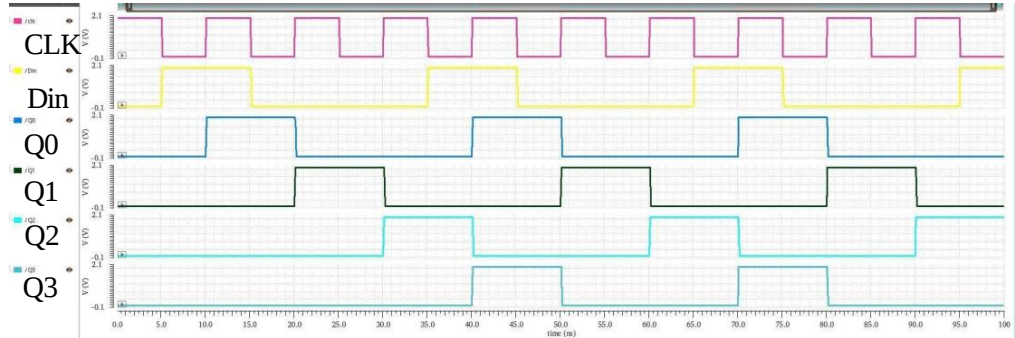


Fig. 5.3 : Timing waveform of SIPO Register using GDI technique

In Fig 5.3 , we can look that with each of the CLK pulse , the Din is getting shifted across the D Flip Flops. All D Flip flops are positive edge triggered. Thus , get a clear idea that the circuit is working as we have expected.

In chapter 4 , we have already calculated the timing parameters of D Flip Flop using GDI technique. The data obtained were as follows :

Setup Time = 97ps
 Hold Time = 0s
 CLK-Q delay = 192.3ps

Loading delay of 4 bit SIPO circuit is calculated as follows:

$$T_{\text{loading_delay}} = N \times T_{\text{clk-q}} , \quad (5.4)$$

where N is the no .of Flip Flops

Using eq (5.1) , $T_{\text{clk}} \geq 192.3 + 97\text{ps} = 289.3\text{ps}$

Thus total loading delay of the circuit is,

$$\begin{aligned} \Rightarrow T_{\text{loading_delay}} &= N \times T_{\text{clk}} \\ &= 4 \times 289.3\text{ps} \\ &= 1157.2 \text{ ps} \end{aligned}$$

Additionally , Power observed of the circuit: 1083.8 μ W

5.2.3 TGDI Based SIPO

Here, we have implemented a SIPO shift register with the usage of the TGDI technique, which extends the GDI approach by incorporating transmission gates into the design. Transmission gates, composed of parallel nMOS and pMOS transistors being controlled by complementary signal, enable the circuit to pass both logic high and logic low levels without voltage degradation. In the TGDI based SIPO register, transmission gates are strategically placed to ensure reliable data transfer and full voltage swing at the outputs. This integration improves signal integrity, reduces threshold voltage losses, and minimizes noise susceptibility compared to pure GDI designs. As a result, the TGDI based SIPO register achieves faster switching speeds, lower propagation delays, and enhanced power efficiency while maintaining a reduced transistor count and compact area. These advantages make TGDI an effective technique for designing low-power, high-performance sequential circuits suitable for modern VLSI, it is very much useful for the portable and battery operated systems in the digital domain.

The Schematic of 4 bit SIPO is shown in Fig 5.4 :

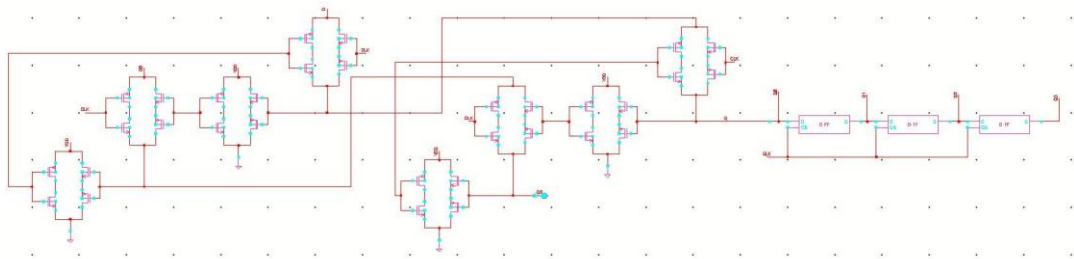


Fig. 5.4 : Schematic of SIPO Register using TGDI technique

The functionality of 4 bit SIPO register circuit using GDI technique shown in Fig. 5.2, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m).

The timing waveform is represented in Fig 5.5

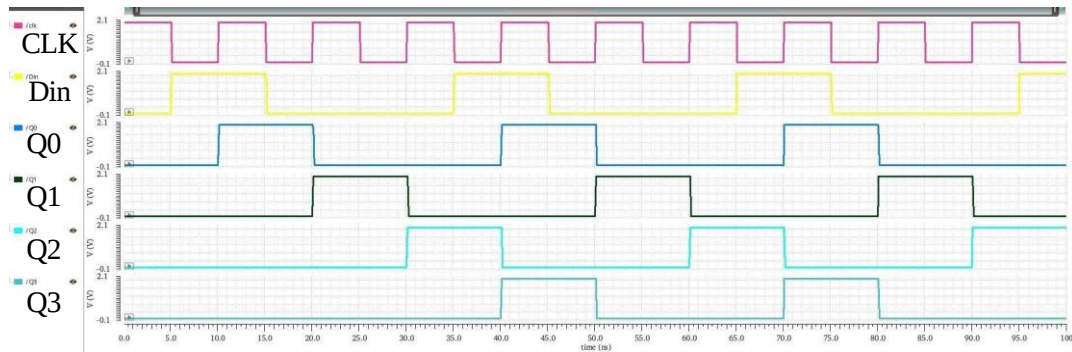


Fig. 5.5 : Transient Analysis of SIPO Register using TGD technique

In the figure , we can clearly observe that each CLK pulse , along with the Din is getting shifted across the D Flip Flops. All D Flip Flops are positive edge triggered circuit. Thus , we can get a clear idea that the circuit is working as we would expect it.

In chapter 4 , we have already calculated the timing parameters of D FF using TGD technique. The data obtained were as follows :

Setup Time = 62.4ps

Hold Time = 0s

CLK-Q delay = 129.3ps

Loading delay of 4 bit SIPO circuit is calculated as follows:

$$T_{\text{loading_delay}} = N \times T_{\text{clk-q}} , \quad (5.5)$$

where N is the no .of Flip Flops

$$\text{Using eq (5.1) , } T_{\text{clk}} \geq 129.3 + 62.4\text{ps} = 191.7\text{ps}$$

Thus total loading delay of the circuit is,

$$\begin{aligned} \Rightarrow T_{\text{loading_delay}} &= N \times T_{\text{clk}} \\ &= 4 \times 191.7\text{ps} \\ &= 766.8 \text{ ps} \end{aligned}$$

Additionally , Power observed of the circuit: 1375.2uW

5.2.4 Comparison

To analyze the performance benefits of TGDI logic in sequential circuit design, a comparison was carried out using a SIPO register. Key parameters like that of the consumption of power along with the delay as well as the PDP were measured for both GDI and TGDI based implementations. The results, presented in the table below, provide insight into how TGDI affects the overall efficiency of the SIPO register.

The delay considered here is the Loading delay of the entire SIPO register.

TABLE 5.2 : Comparison Table of SIPO using GDI and TGDI technique

Parameters	GDI	TGDI
Power	1083.8 μ W	1375.2 μ W
Delay	1312ps	766.8 ps
Power Delay Product	1.422nJ	1.054nJ

From the above we get a clear idea that TGDI based SIPO register consumes about 27% more power than its GDI counterpart. However, it achieves a significant delay reduction of approximately 42%, which in turn results in a 26% improvement in the Power Delay Product. This demonstrates that TGDI logic, while slightly more power-intensive, offers faster operation and better overall efficiency in the energy, making it like one of the most well-suited one for timing-critical applications in modern VLSI systems.

5.3 Linear Feedback Shift Register (LFSR)

A 4-bit LFSR is a simple yet effective sequential circuit widely used for applications in number generation such as that of pseudo random number, cryptography, and also in digital testing.[8] It consists of four flip-flops connected in series, where the output of certain flip-flops which are being combined using XOR for the generation of the feedback input to our flip-flop which is first. The selection of these states is based on a primitive polynomial that guarantees the LFSR produces a maximal-length sequence. The number of states it will travel before repeating itself depends on how the seed values are provided. To provide the seed values, we have added Preset and Reset in the D FF which were discussed in earlier chapter. The 4-bit LFSR cycles through maximum 15 possible non-zero states before repeating, thereby providing a long pseudo-random sequence relative to its size.. The operation of the 4-bit LFSR is synchronous, which is clock controlled. On every pulse of clock, contents of our flip-flops are being made to shift by one position towards the output. Simultaneously, the feedback value, which

is the XOR of selected flip-flop outputs (taps), is fed into the first flip-flop. This feedback ensures the sequence evolves in a pseudo-random manner, which is deterministic but appears random over time. The total delay along the critical path includes three main components. First is the clock- to-Q delay, which is the overall amount of time taken for a flip flops output to respond after giving the clock edge. Second is the delay introduced by the XOR gates used in the feedback path, which depends on the number of XOR operations and their implementation. The overall loading delay of the 4-bit LFSR can be estimated using the following formula:

$$T_{\text{loading_delay}} = T_{\text{CLK-Q}} + T_{\text{setup}} + T_{\text{XOR}} \quad (5.6)$$

The Block Diagram of the circuit is in Fig 5.6

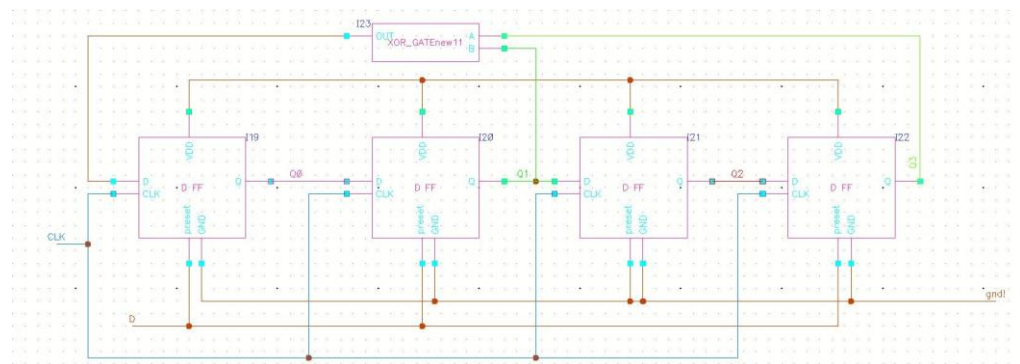


Fig. 5.6 : Block Diagram of LFSR circuit

A following table has been made to see how the values are modified in the register. Initially D0,D1,D3 are preset to high voltage and Q2 grounded. We have taken the feedback of Q1 andQ3 and passed it through a XOR gate and fed that output in D0.

Table 5.3 : State transition Table of LFSR circuit

CLK	Q0	Q1	Q2	Q3
-	1	1	0	1
1	0	1	1	0
2	1	0	1	1
3	1	1	0	1
4	0	1	1	0
5	1	0	1	1
6	1	1	0	1

5.3.1 LFSR Based on GDI

Here, we have implemented a LFSR using the GDI technique, which improves upon conventional CMOS logic by applying inputs to multiple transistor terminals to realize complex logic functions with fewer components. The GDI based LFSR is designed to efficiently generate pseudo-random sequences using a reduced transistor count, leading for a lower consumption in power along with a smaller silicon area in comparison to our traditional CMOS implementations. By minimizing switching activity and propagation delay, the GDI technique enhances overall speed and power efficiency without compromising functionality. This makes the GDI- based LFSR an ideal choice for low-power, high-performance digital systems, especially in portable and battery-operated because her the energy efficiency is crucial. The schematic of LFSR using GDI is shown in Fig 5.7 :

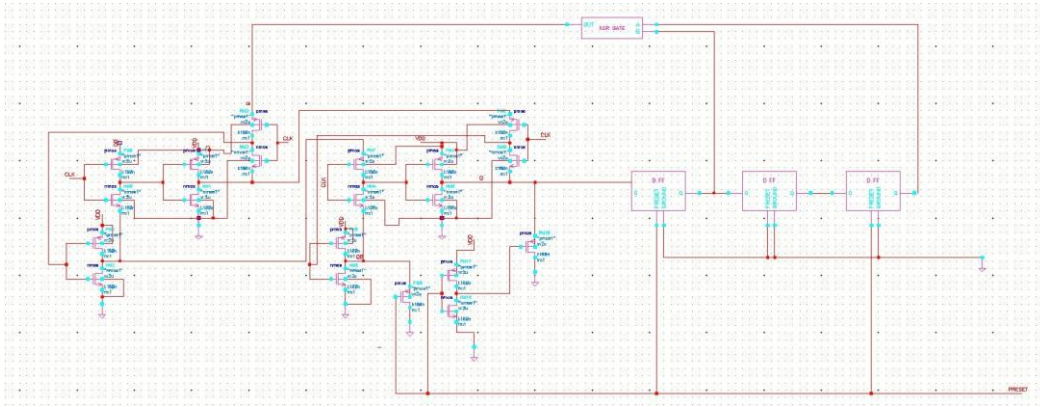


Fig. 5.7 : Schematic of LFSR using GDI technique

The functionality of 4 bit LFSR register circuit using GDI technique shown in Fig. 5.12, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is shown in Fig 5.8

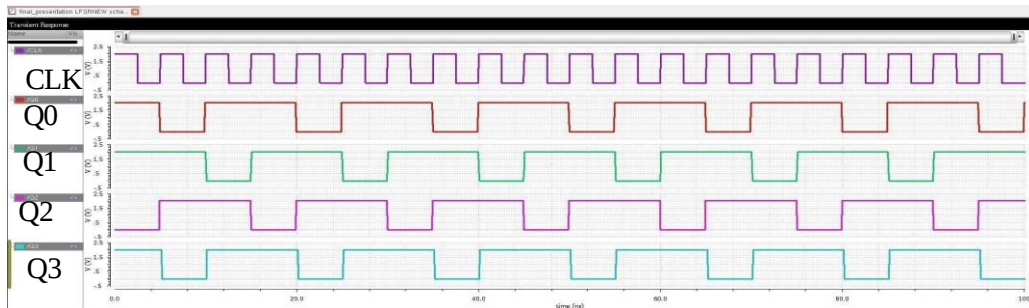


Fig. 5.8 : Transient Analysis of LFSR using GDI technique

In the figure, we can see with each clk pulse , the data is propagating and Q1 and Q3 is XOR ed and fed into D. All D flip flops present here are positive edge triggered D Flip Flop . Thus validating the functionality of the LFSR which is made here.

In chapter 4 , we have already calculated the timing parameters of D FF using GDI technique. The data obtained were as follows :

Setup Time = 97ps

Hold Time = 0s

CLK-Q delay = 192.3ps

The delay of XOR gate is calculated in chapter 2 section , using that value

Txor: 34.92 ps

Using eq(5.4), the loading delay of the circuit is :

$$\begin{aligned} &= T_{clk-q} \text{ delay} + T_{xor} + T_{setup} \\ &= 192.3\text{ps} + 34.92\text{ps} + 97\text{ps} \\ &= 324.22\text{ps} \end{aligned}$$

Additionally power observed of the circuit : 1187.54 uW

5.3.2 LFSR based on TGDI

Here, we have implemented a LFSR along with the TGDI technique, which extends the GDI approach by incorporating transmission gates into the design. Here the Transmitting gates, consists of the parallel nMOS and pMOS transistors which are being controlled by the complementary of signals, allow the circuit to pass both logic high and logic low levels without voltage degradation. In the TGDI-based LFSR, transmission gates are strategically used to ensure reliable data shifting and full voltage swing at the outputs. This integration improves signal integrity, reduces threshold voltage losses, and minimizes noise susceptibility compared to pure GDI designs. As a result, the TGDI-based LFSR achieves faster switching speeds, lower propagation delays, and enhanced power efficiency while maintaining a reduced transistor count and compact area.

The Schematic Diagram representation of LFSR using TGDI is depicted in Fig 5.9

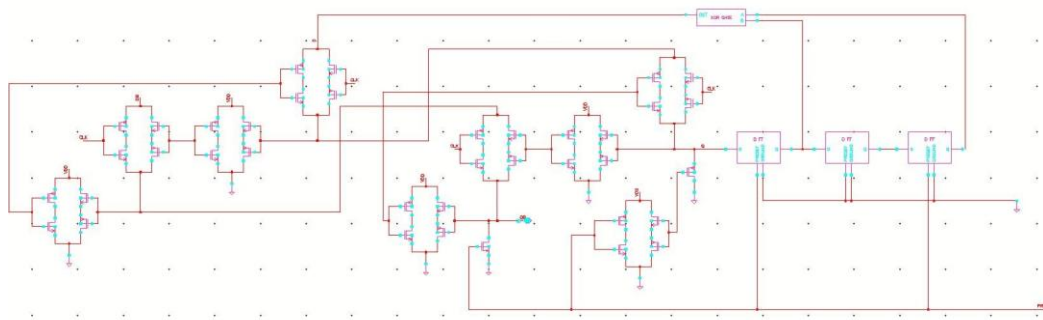


Fig. 5.9 : Schematic of LFSR using TGDI technique

The functionality of 4 bit LFSR register circuit using TGDI technique shown in Fig. 5.13, is tested through simulation using Cadence Virtuoso. The circuit were simulated at 2V(for 0.18 μ m technologies, respectively), 100MHz , with load capacitance of 100fF. The Aspect Ratio of all MOSFET taken under consideration are (2 μ m/0.18 μ m). The timing waveform is shown in Fig 5.10

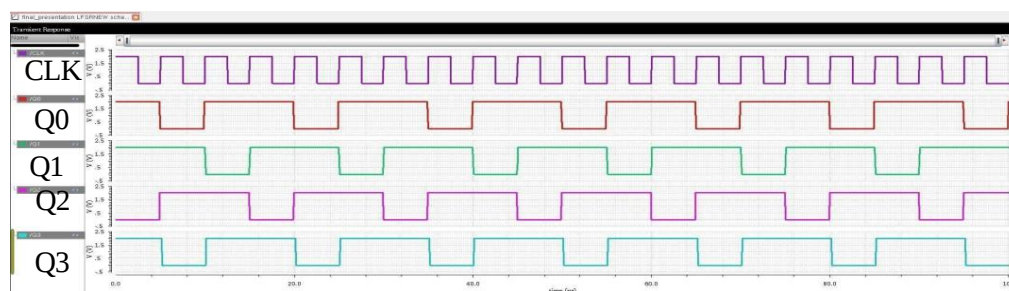


Fig. 5.10 : Transient Analysis of LFSR using TGDI technique

In the figure, we can see with each clk pulse , the data is propagating and Q1 and Q3 is XOR and fed into D. All D FF are positive edge triggered. Thus it is validating the functionality of the LFSR which is made here

In chapter 4. , we have already calculated the following data's of D FF using TGDI technique . So using those data

Setup Time = 62.4ps
 Hold Time = 0s
 CLK-Q delay = 129.3ps

The delay of XOR gate is also calculated in chapter 2. Using that data,

Txor : 22.82 ps

$$\begin{aligned} T_{\text{loading_delay}} &= T_{\text{clk-q delay}} + T_{\text{xor}} + T_{\text{setup}} \\ &= 214.52 \text{ ps} \end{aligned}$$

Additionally , Power Observed of the circuit : 1484.63 uW

5.3.3 Comparison

The following table presents we get and clear analysis of the consumption of power along with the delay, and PDP for the LFSR implemented using two different logic techniques. These metrics are critical for evaluating the efficiency and speed of the design. Power consumption reflects the energy used during operation, delay indicates the speed at which the LFSR can process data, and the PDP provides an overall measure of energy efficiency by combining both power and delay.

Table 5.3 : Comparison Table of LFSR using GDI and TGDI technique

Parameters	GDI	TGDI
Power	1187.54 uW	1484.63 uW
Delay	324.22ps	214.52ps
Power Delay Product	385 fJ	319 fJ

The 4-bit LFSR designed using TGDI logic was compared against the GDI implementation in Cadence Virtuoso. The TGDI based design consumes approximately 27% more power than the GDI counterpart but achieves a significant delay reduction of around 42%. This reduction in delay leads to increment of about 26% in the PDP. These results indicate that while TGDI incurs a higher power cost, it offers faster operation and better energy efficiency, making it a suitable choice for timing-critical applications.

5.4 Summary

In this chapter, SIPO registers and 4-bit LFSR were implemented and simulated using GDI and TGDI techniques in Cadence Virtuoso. The metrics of performance including consumption of power, along with delay, and PDP were analyzed on both designs. For the SIPO circuitry, the GDI implementation consumed 1083.8 μW power with a delay of 1312 ps, resulting in a PDP of 1.422 nJ. In comparison, the TGDI design consumed higher power at 1375.2 μW but achieved a significantly reduced delay of 766.8 ps, lowering the PDP to 1.054 nJ. Similarly, for the LFSR circuit, the GDI approach showed consumption of power of 1187.54 μW along with the delay of 324.22 ps with a PDP of 385 fJ. The TGDI design, while consuming more power at 1484.63 μW , improved delay to 214.52 ps

and reduced PDP to 319 fJ. These results highlight that although TGDI circuits tend to consume more power, they offer substantial delay improvements that contribute to better overall energy efficiency. Thus, TGDI proves advantageous for applications requiring faster operation and enhanced power-delay trade-offs in modern VLSI systems.

CHAPTER 6

CONCLUSION

6.1 Conclusion

This project explored design as well as the implementation of fundamental digital components—Ripple Carry Adders (RCA), Carry Select Adder (CSA), Serial-In Parallel- Out (SIPO) shift registers, and Linear Feedback Shift Registers (LFSR)—using Gate Diffusion Input (GDI) and Transmission Gate Diffusion Input (TGDI) logic styles. Through careful design and analysis, it was demonstrated that both GDI and TGDI techniques can significantly reduce power consumption and transistor count while maintaining or improving circuit performance compared to traditional CMOS implementations. The extensive literature review highlighted the power and area efficiency advantages of GDI and TGDI, but also revealed a research gap in their application to essential building blocks such as RCA, CSA, SIPO, and LFSR. Addressing this gap, the project successfully developed TGDI-based architectures for these components, illustrating their potential for integration into the lower power and higher performing VLSI systems. Simulation results and comparative studies confirmed that TGDI-based designs provide a promising approach to reducing dynamic and static power dissipation without compromising speed or reliability. These findings underline the feasibility of adopting TGDI logic styles in next-generation digital circuit designs, particularly in applications where power efficiency is critical. Overall, this work contributes to the ongoing efforts to optimize digital circuit design by offering novel TGDI-based implementations for key sequential and combinational components. Future work could extend these designs to larger and more complex systems, explore further optimization techniques, and evaluate the influence of our process variations on real silicon fabrication which are in proposed architectures.

6.2 Future Work

The promising results obtained in this project open us several different ways for the research as well as the development. One potential way is the extension in TGDI and GDI techniques to more complex arithmetical units like the carry look-ahead adders, multipliers, and dividers, which may yield even greater power and area optimizations. Additionally, future work can focus on integrating the TGDI

based RCA, CSA, SIPO shift registers, and LFSR into larger digital systems like that of the microprocessor, like the digital signal processor along with the cryptographic modules, to evaluate their benefits at the system level. Furthermore, implementing the proposed designs on silicon through FPGA prototyping or ASIC fabrication can validate simulation results and demonstrate practical feasibility. Another promising area is exploring the performance of TGDI and GDI circuits under low-voltage and near-threshold conditions, which is critical for ultra-low-power applications like Internet of Things (IoT) devices and wearables. Finally, the development of design automation tools and CAD flows tailored for TGDI and GDI logic styles could significantly ease their adoption in industrial VLSI design, promoting wider use of these power-efficient techniques in next-generation digital integrated circuits.

6.3 SOCIAL IMPACT

The social impact of this thesis work is summarized as follows:

- 1. Energy Efficiency:** The proposed TGDI and GDI based designs demonstrate significant reductions in power consumption. This supports the development of sustainable digital systems with lower energy requirements, which is particularly beneficial in large-scale computing and consumer electronics.
- 2. Extended Battery Life:** Reduced power usage makes these designs ideal for battery powered applications, including portable medical devices, smartphones, and wearable technologies, thereby improving user experience and device longevity.
- 3. Environmental Sustainability:** Lower energy demands at the hardware level contribute to decreasing the environmental footprint of digital devices, aligning with global goals for sustainable technology development.
- 4. Digital Accessibility:** Energy-efficient and low-transistor-count designs can reduce manufacturing and operational costs, making electronic devices more accessible in energy-constrained or economically challenged regions.
- 5. Support for IoT and Wearables:** The optimized designs are particularly suitable for integration into ultra-low-power applications such as Internet of Things (IoT) nodes, smart sensors, and wearable devices, enhancing their performance and energy sustainability.
- 6. Economic and Industrial Relevance:** By reducing silicon area and power consumption, these designs can lower production costs and energy usage in industrial applications, fostering economic efficiency and competitiveness in the semiconductor industry.

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LIST OF PUBLICATIONS AND THEIR PROOFS

- [1] A.Roy , N. Pandey , H. Dalal “**Implementation of Linear Feedback Shift Register circuit (LFSR) Using Transmission Gate Diffusion Input(TGDI) Technique**” Submitted and accepted (Publication in progress) in the 6th IEEE India Council International Subsections Conference (**INDISCON 2025**)

Notification of Review Decision for Submission #2598 - INDISCON 2025  



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Dear Amantya Roy,

Congratulations!

We are pleased to inform you that your paper #2598 titled "Implementation of Linear Feedback Shift Register circuit (LFSR) Using Transmission Gate Diffusion Input(TGDI) Technique", submitted to INDISCON 2025 has been Accepted for presentation in the Oral Session.

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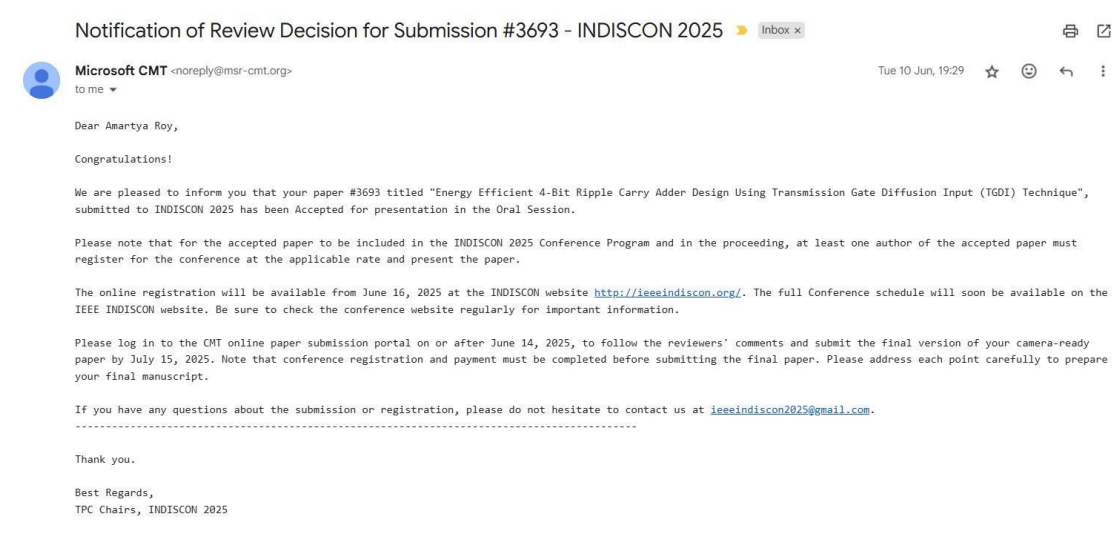
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Thank you.

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- [2] A.Roy , N. Pandey , H. Dalal “**Energy Efficient 4-Bit Ripple Carry Adder Design Using Transmission Gate Diffusion Input (TGDI) Technique**” Submitted and accepted (Publication in progress) in the 6th IEEE India Council International Subsections Conference (**INDISCON 2025**)





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PROFILE & VALUE

- Skilled EM/IR Engineer with 8 months of experience, including distinguished expertise in implementing Tool Flow Methodology (TFM) for Full-Chip (EM/IR) Signoff, amplifying the efficiency of SoC design strategies.
- Profound experience in **RedHawk** and **RedHawk_SC** for power integrity and signoff analysis
- Worked in **Cadence Virtuoso** for circuit design and layout.
- Used **Proteus** for circuit simulation and PCB design.
- Technical Proficiency in **C++**, **Java**, **Python**, **Verilog**, **Linux**

EXPERTISE

- EM/IR Signoff Analysis
- Tool Methodology Flow(TFM)
- ASIC Design Flow
- Physical Design
- STA
- Cadence Virtuoso
- RedHawk_SC

EDUCATION

Masters: Delhi Technological University, Delhi
M.Tech in VLSI & Embedded System (2023-2025)
CGPA: 7.49 (till 2nd Semester)

Bachelors : Cooch Behar Government Engineering College
B.Tech in ECE (2019-2023)
CGPA : 9.09

CAREER PROGRESSION

POST GRADUATE ENGINEER INTERN : ANSYS SOFTWARE Pvt. Ltd.

(JUNE 2024 -Till Now)

- Dealing with EM-IR flow in Signoff analysis using Industry Standard RedHawk and RedHawk_SC tool.
- Well acquainted with PDN analysis issues debugging grid weakness, static/dynamic EM/IR analysis.
- In-rush current analysis in low power designs, optimizing power integrity and ensuring stable system performance.

INTERNSHIP PROJECTS

Project: EM/IR Analysis for a Full Chip

- Facilitated Flow flushes in RedHawk_SC like early power grid checks, power calculations, static IR, dynamic IR (vector less, VCD-based), electromigration analysis and inrush analysis for power gated domains to carryout EMIR Signoff activities on latest technology nodes.
- Developed a script to perform version to version comparison and debug design-related issues.
- Automated the extraction and export of the entire run.py script from a database(DB) using a Python script, streamlining the retrieval process for in-house runs.

COLLEGE PROJECTS

- **Design and Analysis of D Flip Flop Using Transmission Gate Diffusion Input (TGDI) Technique**
Implemented transmission gate concept with GDI concept and found device having less delay overall in Cadence Virtuoso
- **Leakage Power Suppression and Stability Improvement in 6T SRAM Using Stacked Configuration.**
Implemented various stackings in the 6T SRAM model structure and compared their results in Cadence Virtuoso
- **Implementation of FIFO using Verilog**
FIFO (First In First Out) is a memory queue which controls the data flow between two modules .
- **Traffic Signal Controller:**
Designed and simulated a traffic signal controller using 8051 microcontroller in **Proteus** for real-time control of traffic flow.

TECHNICAL SKILLS

- **Tools :** RedHawk , RedHawk_SC , Cadence Virtuoso , Proteus , Xilinx Vivado , Linux
- **Programming Languages :** Python , Java , C++ , Verilog
- **Area of Interest :** Digital IC Design , Low Power Techniques , Physical Design ,ASIC Design Flow

Achievements/Participation

- Qualified in Gate 2022, 2023 in both ECE/EE paper.
- Participated in INTER College Football and Basketball games.