M.Tech. Thesis

NANO-SCALE, TEMPERATURE SENSITIVE, ANALYTICAL MODELING INCORPORATING QUANTUM EFFECTS OF SC, JL, DG STACK (SC-JL-DG) MOSFET FOR ANALOG INDUSTRY APPLICATIONS AT LEADING FREQUENCIES

Prajvi Udar

May, 2025

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A Thesis Submitted
In Partial Fulfillment of the Requirements
for the Degree of

MASTER OF TECHNOLOGY

In

VLSI AND EMBEDDED SYSTEMS

by

PRAJVI UDAR
(2K23/VLS/06)

Under the Supervision of

Dr. Sonam Rewari
Assistant Professor, ECE, DTU

Dr. Deepika Sipal
Assistant Professor, ECE, DTU

Department of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-110042. India

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Prajvi Udar

(2K23/VLS/06)

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-42

CANDIDATE'S DECLARATION

I Prajvi Udar, hereby certify that the work which is being presented in the thesis entitled "Quantum Effects Induced Temperature-Sensitive, Ultradoped SC, JL, DG Stack (USC-JL-DG)Semiconductor FET for Analog Applications -Analytical Modelling" in partial fulfillment of the requirements for the award of the Degree of Master of Technology, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August 2023 to May 2025 under the supervision of Dr. Sonam Rewari, Assistant Professor and Dr. Deepika Sipal, Assistant Professor of Department of Electronics and Communication Engineering, Delhi Technological University.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-42

CERTIFICATE BY THE SUPERVISOR(s)

Certified that **Prajvi Udar (**2K23/VLS/06) has carried out their search work presented in this thesis entitled **"Quantum Effects Induced Temperature-Sensitive, Ultradoped SC, JL, DG Stack (USC-JL-DG)Semiconductor FET for Analog Applications -Analytical Modelling"** for the award of **Master of Technology** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under our supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

Signature

(Dr. Sonam Rewari)

(Assistant Professor)

(DTU, Shahbad Daulatpur,
Main Bawana Road,
Delhi-42)

Signature

(Dr. Deepika Sipal)

(Assistant Professor)

(DTU, Shahbad Daulatpur,
Main Bawana Road,
Delhi-42)

Date:

ABSTRACT

This work presents an in-depth investigation into the analog and radio-frequency (RF) performance characteristics of a novel Junction-Less Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor (JL-DG-MOSFET) architecture featuring a gate oxide stack. The study specifically targets the influence of device scaling and structural modifications on analog performance metrics and their suitability for high-performance, low-power analog/RF circuit applications. A significant aspect of the device's operation is the emergence of quantum mechanical effects due to aggressive channel length scaling, which plays a vital role in determining its small-signal behavior.

Key Figures of Merit (FOMs) for analog design are analyzed to evaluate the efficiency and robustness of the JL-DG-MOSFET. These include the cut-off frequency (f_T), gain-frequency product (GFP), transconductance-frequency product (TFP), output conductance (g_d), Early voltage (V_{EA}), intrinsic gain (A_V), transconductance efficiency (g_m/I_D), and the transconductance (g_m) itself. The behavior of these parameters is critically assessed to determine the device's amplification capabilities, signal bandwidth handling, and overall analog reliability.

All simulations and characterizations are conducted using the ATLAS device simulator, which allows for precise numerical modeling of the JL-DG-MOSFET under varying biasing and geometrical conditions. The simulated results consistently align with theoretical expectations, validating the physical modeling and demonstrating the potential of this device structure for future analog and RF integrated circuits. The results not only confirm the benefits of using a junction-less structure in reducing leakage and variability but also highlight the advantages of double-gate control in enhancing electrostatic integrity and analog responsiveness.

This research provides a valuable framework for understanding the analog design trade-offs in emerging multi-gate, junction-less transistors and contributes to the broader effort of developing energy-efficient, scalable analog devices for next-generation nanoscale CMOS technologies.

LIST OF PUBLICATIONS

[1] P. Udar, D. Sipal, A. Goel, and S. Rewari “Nano-Scale, Temperature-Sensitive, Analytical Modeling Incorporating Quantum Effects of SC, JL, DG Stack (SC-JL-DG) MOSFET for Analog-Industry Applications at Leading Frequencies" Submitted Under review in Springer Nature(Silicon) Journal- 2025

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
JL	Junctionless
DG	Double Gate
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SCEs	Short-Channel Effects
DIBL	Drain-Induced Barrier Lowering
GAA	Gate-All-Around
DMSG	Dual Metal Gate Surrounding Gate
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
GBW / GBWP	Gain Bandwidth Product
GFP	Gain-Frequency Product
TFP	Transconductance-Frequency Product
TCAD	Technology Computer-Aided Design
QME	Quantum Mechanical Effects
BQP	Bohr Quantum Potential
ECB	Electron Conduction Band
HVB	Hole Valence Band
EVB	Electron Valence Band
WKB	Wentzel-Kramers-Brillouin (Approximation)
EOT	Equivalent Oxide Thickness
VFB	Flat-Band Voltage
TGF	Transconductance Generation Factor
GTFP	Gain-Transconductance-Frequency Product
DOS	Density of States
FFT	Fast Fourier Transform
1-dB CP	1-dB Compression Point
RDF	Random Dopant Fluctuation
FCC	Face-Centered Cubic
BCC	Body-Centered Cubic
CMOS	Complementary Metal-Oxide-Semiconductor

CHAPTER 1

INTRODUCTION

Double gate MOSFETs are emerging as one of the most encouraging ways to lessen SCEs (Short-channel-effects) as CMOS scaling moves closer to its ideal state. Quantum effects [1] are now important in downsized devices in addition to SCEs, particularly when the gate length is less than 20 nm. When the gate length of a device falls below 20 nm, its electrostatic control rapidly declines. Due to the impact of quantum confinement on the carrier's motion, the distribution phenomena and transport characteristics of charge carriers differ from those of classical carriers [1]. Several analytical models for Junctionless Transistors have been published, including Dual Metal Gate engineered Surrounding Gate structure (DMSG) [2], Gate and Drain work function engineered Double Gate structure [3, 4], Gate All Around structure (GAA) [5], and Electrostatic potential distribution, subthreshold current, threshold voltage, and SCEs for Double Gate structure (DG) [6–8]. According to reports, the device's performance will be enhanced by inserting the gate-stack, by developing a high-K layer over the SiO_2 [9–11]. The JL DG FET's preliminary analysis and result are likely to be successful, and they highlight the necessity of a thorough examination of the devices' applicability for contemporary wireless communication systems, including radio frequency integrated circuit (RFIC) design, cellular phones, wireless networks, navigation systems, radio broadcasting, etc.

As semiconductor fabrication technologies push the boundaries of miniaturization, traditional transistor architectures increasingly struggle with performance degradation. Key challenges include threshold voltage roll-off, poor subthreshold swing, and increased leakage currents, all of which can compromise power efficiency and signal fidelity. To address these limitations, researchers have proposed various multigate structures, among which the Double-Gate (DG) configuration stands out due to its superior electrostatic integrity. Meanwhile, the junctionless approach simplifies fabrication by eliminating abrupt junctions, offering process-friendly characteristics and reduced variability in ultra-scaled nodes [12]. By merging the double-gate architecture with junctionless operation, the resulting device benefits from improved control over channel potential and suppression of short-channel effects. This synergy also enables a more uniform electric field distribution along the channel, which can enhance carrier transport and device reliability [13]. For analog and RF circuit designers, these characteristics translate into better linearity,

increased transconductance, and lower noise – all critical in modern high-performance electronics. Furthermore, incorporating a gate stack that uses high-κ dielectric materials improves gate capacitance without compromising gate leakage, ensuring high-frequency compatibility while maintaining power efficiency [14].

The analog/RF performance of conventional double gate devices has been studied by several researchers [15-17], but there are just a few papers on JL DG devices that explore their usefulness for analog/mixed-signal system-on-chip applications [18, 19]. Cho et al. [18] investigated the RF performance of JL nanowire devices in a recent work; however, the impact of downscaling on the RF/analog performance was not thoroughly examined and is still largely unknown. Therefore, better RFIC design for wireless communication systems requires an understanding of how gate-length down scaling affects the DG JL FET's performance figure-of-merits. To ensure low inter-modulation and higher-order, the RF system must be linear [19]. Numerous system-level methods that need for intricate circuitry are currently available to reduce these unwanted signals with frequencies distinct from the input signal.

With increasing demands for compact and power-efficient transceivers in 5G, IoT, and wearable technologies, the focus has shifted toward intrinsic linearity at the transistor level. While system-level linearization techniques such as feedback and digital predistortion are widely used, they come with trade-offs in complexity and energy consumption [20]. By achieving better linearity within the device itself, circuit designers can build simplified and more efficient RF systems. Junctionless DG MOSFETs, owing to their symmetric architecture and undoped channel, provide a promising platform for these applications [21].

Thus, it becomes beneficial to make an effort to improve linearity at device-level. Analog & RF (radio-frequency) performance analysis of nanoscale devices is made possible by current research. Linearity, noise figure, cutoff frequency, and inherent gain make up the performance requirements for analog and radio frequency circuits [22–27].

In addition to linearity, parameters like high gain-bandwidth product and low output conductance are essential for RF amplifier stages and analog signal processing. Junctionless DG MOSFETs inherently demonstrate low parasitic resistance due to their uniformly doped channel, which also reduces sensitivity to random dopant fluctuations—a major source of mismatch in scaled CMOS [28]. Their simplified structure and robust control over the conduction path make them suitable

candidates for integration into RF front-end components, including low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), and mixers [29].

Moreover, the electrostatic potential across the channel in JL DG devices tends to remain more stable across process variations, allowing more predictable behavior in both analog and digital domains. This is crucial when transistors are used in systems-on-chip (SoCs), where maintaining analog integrity alongside high-speed digital blocks becomes increasingly difficult due to substrate noise coupling and voltage fluctuations [30].

Another vital consideration is the role of quantum effects in ultra-scaled devices. As dimensions shrink below 10 nm, the assumptions of classical charge transport models begin to break down. Instead, phenomena like quantum confinement and tunneling become dominant, altering capacitance, threshold voltage, and mobility [31]. Accurate modeling of such effects is essential not only for understanding device physics but also for correctly predicting performance under real operating conditions. Advanced simulation platforms, including Silvaco ATLAS TCAD, incorporate quantum-corrected drift-diffusion models that help bridge this gap [32].

Therefore, in this paper, our main interest is to investigate both, the analog application for the Junctionless Double-Gate Stack MOSFET whilst considering quantum mechanical effects. To investigate analog & RF performance parameters of the device for wireless-communication applications, section IV depicts the results for the same. The section is divided in four parts respectively studying the analog, RF and linearity for the proposed device. Parameters like intrinsic gain (A_V), TGF, g_d, g_m, V_{EA}, f_T, Gain-Bandwidth Product, S parameters, VIP_2, VIP_3 & others are extensively discussed here. Simulations are done using the Silvaco ATLAS TCAD software show that the device parameters are suitable for better performance.

Ultimately, the ability of JL DG MOSFETs to meet the rigorous demands of modern analog/RF applications lies in their unique blend of structural simplicity, robust scalability, and superior electrostatics. When accurately modeled with quantum effects and verified through simulation, these devices show great promise for integration into next-generation wireless communication systems and analog signal chains [33, 34].

CHAPTER 2

LITERATURE SURVEY

2.1 EVOLUTION OF MOSFET ARCHITECTURES FOR SCALING

The relentless pursuit of Moore's Law has driven the miniaturization of MOSFETs, leading to significant challenges in maintaining device performance at nanometer scales. Traditional bulk MOSFETs suffer from short-channel effects (SCEs), including threshold voltage roll-off, drain-induced barrier lowering (DIBL), and increased leakage currents, which degrade device reliability and performance [35]. To mitigate these issues, multi-gate structures such as Double-Gate (DG) MOSFETs have been proposed. DG MOSFETs offer superior electrostatic control over the channel, effectively suppressing SCEs and improving subthreshold characteristics [36]. The symmetrical gate configuration in DG MOSFETs enhances gate control, leading to improved scalability and performance in analog and RF applications [37].

2.2 JUNCTIONLESS TRANSISTOR CONCEPT AND INTEGRATION WITH DG ARCHITECTURE

The Junctionless (JL) transistor concept emerged as a solution to the complexities associated with junction formation in traditional MOSFETs. In JL transistors, the channel is uniformly doped, and current conduction is modulated by gate-induced depletion, eliminating the need for abrupt junctions [38].

Colinge et al. introduced the JL transistor, demonstrating its potential for simplified fabrication and reduced variability [39]. Integrating the JL concept with DG architecture combines the benefits of both approaches, resulting in Junctionless Double-Gate (JL DG) MOSFETs that exhibit excellent electrostatic control and simplified manufacturing processes [40]. Analytical and simulation studies have explored various JL DG structures, including Dual Material Gate (DMG) configurations, which further enhance device performance by modulating the electric field distribution along the channel [41]. These advancements have shown promise in

improving analog and RF characteristics, making JL DG MOSFETs suitable for high-frequency applications.

2.3 GATE STACK ENGINEERING AND HIGH-K INTEGRATION

As device dimensions shrink, gate leakage becomes a significant concern. Incorporating high-κ dielectrics into the gate stack has been a pivotal development in addressing this issue. High-κ materials, such as HfO_2, allow for increased gate capacitance without the associated leakage currents of traditional SiO_2 dielectrics [42].

In JL DG MOSFETs, gate stack engineering with high-κ materials enhances gate control, reduces leakage currents, and improves overall device performance. Studies have shown that integrating high-κ dielectrics leads to better subthreshold swing, increased transconductance, and improved analog gain, which are critical parameters for analog and RF applications [43].

Furthermore, the combination of high-κ dielectrics with metal gates allows for work function tuning, enabling precise threshold voltage control. This integration is essential for optimizing the performance of JL DG MOSFETs in analog and RF circuits, where device linearity and gain are paramount [44].

2.4 ANALOG AND RF PERFORMANCE METRICS IN SCALED DEVICES

The analog and RF performance of MOSFETs is characterized by parameters such as transconductance (g_m), output conductance (g_d), intrinsic gain (A_V), cutoff frequency (f_T), and maximum oscillation frequency (f_{max}). These metrics are crucial for evaluating device suitability in high-frequency applications. In JL DG MOSFETs, the elimination of junctions and the double-gate configuration contribute to enhanced analog and RF performance. Studies have reported improvements in gm and A_V, as well as higher f_T and f_{max} values, compared to conventional MOSFETs [45]. However, scaling down the gate length in JL DG MOSFETs presents challenges. Shorter gate lengths can lead to increased SCEs, affecting device linearity and gain. Research has indicated that careful optimization of device dimensions and materials is necessary to maintain high analog and RF performance in scaled JL DG MOSFETs [46].

2.5 LINEARITY AND NOISE IN NANOSCALE MOSFETS

Linearity is a critical parameter in analog and RF circuits, as nonlinearities can lead to signal distortion and intermodulation. JL DG MOSFETs offer advantages in linearity due to their uniform doping and symmetrical structure, which result in a more uniform electric field distribution along the channel [47]. Noise performance, particularly flicker (1/f) noise and thermal noise, is another important consideration. The absence of abrupt junctions in JL DG MOSFETs reduces carrier trapping and scattering, leading to lower noise levels. This characteristic makes JL DG MOSFETs attractive for low-noise amplifier applications in RF circuits [48].

2.6 QUANTUM EFFECTS AND THE NEED FOR ACCURATE MODELING

As MOSFET dimensions approach the nanometer scale, quantum mechanical effects become significant. Quantum confinement and tunneling phenomena can alter carrier transport, affecting device characteristics such as threshold voltage and subthreshold swing.

Accurate modeling of these quantum effects is essential for predicting device behavior and performance. Advanced simulation tools, such as TCAD, incorporate quantum mechanical models to analyze the impact of quantum effects on JL DG MOSFETs. Studies have shown that quantum confinement can lead to increased threshold voltage and reduced carrier mobility, necessitating careful design considerations [49].

2.7 IDENTIFIED RESEARCH GAPS

Despite the advancements in JL DG MOSFET research, several areas require further investigation:

- **Comprehensive Analysis**: While individual aspects of JL DG MOSFET performance have been studied, a holistic analysis encompassing analog, RF, linearity, and noise characteristics is lacking.
- **Quantum Effects**: The impact of quantum mechanical effects on analog and RF performance metrics in JL DG MOSFETs needs more in-depth exploration.
- **Scaling Challenges**: Understanding the trade-offs and limitations associated with scaling JL DG MOSFETs for high-frequency applications remains an open area of research.

Addressing these gaps is crucial for the development of JL DG MOSFETs optimized for analog and RF applications in advanced integrated circuits.

CHAPTER 3

QUANTUM EFFECTS IN MOSFETS

3.1 SCALING OF MOSFET

Challenge 1: Threshold Voltage and Leakage Trade-Offs

To preserve the switching speed of MOSFETs at lower supply voltages, it is necessary to proportionally reduce the threshold voltage (V_T). However, this reduction introduces unintended consequences. A lower V_T leads to an increase in subthreshold leakage current, which significantly impacts the power efficiency and performance reliability of the device. Moreover, achieving a lower threshold voltage often necessitates thinning the gate oxide layer. This, in turn, results in an increase in gate oxide tunneling current—a form of leakage that further deteriorates the device's performance by diminishing the I_{on}/I_{off} current ratio, thus reducing switching precision and operational control.

Challenge 2: Short-Channel Effects and Electrostatic Control

The continual miniaturization of MOSFETs also introduces electrostatic integrity issues. As the channel length shrinks, two-dimensional electrostatic interactions between the gate and the source/drain regions become more prominent. This electrostatic charge sharing leads to a further decline in threshold voltage and an increase in subthreshold swing. Consequently, the gate's control over the channel weakens, leading to a lower I_{on}/Io_{ff} ratio and degraded switching behavior. These short-channel effects limit the scalability and reliability of conventional MOSFET architectures.

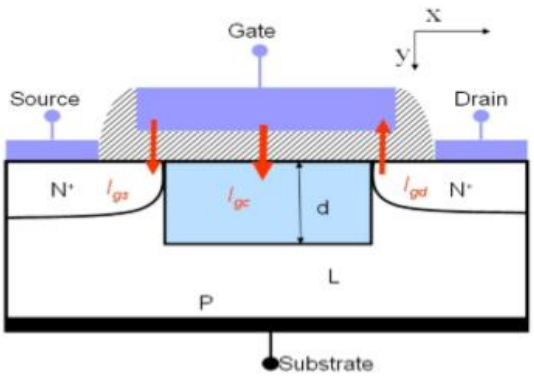


Fig. 3.1 Tunneling current in a MOSFET. I_{gs}: tunneling between gate and source; I_{gc}: tunneling between gate and channel; I_{gd}: tunneling between gate and drain

3.2 BLOCH'S THEOREM

A Bloch wave (or Bloch function) describes the quantum behavior of particles, such as electrons, in a periodic potential—typically a crystal lattice. It is mathematically represented as a plane wave modulated by a function with the periodicity of the lattice[50]. According to Bloch's theorem, the wave function Ψ of an electron in a crystalline solid can be written in the form:

$$\Psi_r = e^{ik\cdot r}u(r) \tag{3.1}$$

Here, u(r) is a periodic function with the same periodicity as the crystal lattice. This theorem implies that the energy eigenstates in a crystal can be completely described using Bloch waves, laying the foundation for understanding electronic band structures [50]. In semiconductors, the periodic function $u_c(r)$ satisfies:

$$u_c = u_r(\vec{r} + \vec{R}) \tag{3.2}$$

where R is a lattice vector. Similarly, in reciprocal space, for a wave vector k, there exists a periodic function ϕ_k such that:

$$\phi(k) = \phi(k)(r^{\rightarrow} + R^{\rightarrow}) \tag{3.3}$$

$$\phi_c = e^{ik\vec{r}}\,\phi_k(\vec{k},\vec{r}) \tag{3.4}$$

Solving Eqns (3.1) and (3.2) provides the E–k relationship, which describes the dependence of energy on wave vector, ultimately determining the band structure. Carrier motion in semiconductors follows this E–k relationship, and for weak electric fields, electrons and holes can be treated as quasi-classical particles with an effective mass m^* defined by:

$$m^* = \frac{\frac{1}{\hbar^2}\partial^2 E}{\partial \kappa^2} \tag{3.5}$$

In such conditions, the carriers' quantum behavior is masked, and their motion can be modeled using classical mechanics. However, when dimensions become comparable to the de Broglie wavelength or when subjected to strong external fields, this approximation breaks down. The external field can no longer be treated as a small perturbation, and quantum mechanical effects (QMEs) such as tunneling and quantized energy levels become significant. In such nanoscale regimes, one must solve the time-independent Schrödinger equation, incorporating both the periodic crystalline potential $U_C(r)$ and the external potential $V_E(r)$:

$$-\frac{\hbar^2}{2m_0}\nabla^2\Psi_c + [U_C(\vec{r}) + V_E(\vec{r})]\Psi_c(\vec{r}) = E\Psi_c(\vec{r}) \tag{3.6}$$

where:

- $\hbar = h/2\pi = 1.054 \times 10^{-34}$ J.S is the reduced Planck constant,
- $m_0 = 0.911 \times 10^{-27}$ kg is the electron rest mass,
- $U_C(\vec{r})$ is the periodic potential from the crystal lattice,
- $V_E(\vec{r})$ represents the potential due to an external electric field.

In large crystals, $V_E(\vec{r})$ is usually negligible compared to $U_C(\vec{r})$, and the equation simplifies to:

$$-\frac{\hbar^2}{2m_0}\nabla^2\Psi_c + U_C(\vec{r})\Psi_c(\vec{r}) = E\Psi_c(\vec{r}) \tag{3.7}$$

This simplified model is valid only when quantum interference and boundary effects are negligible [51].

3.3 QUANTUM MECHANICAL EFFECTS

3.3.1 Introduction to Quantum Tunneling

Quantum tunneling is a fundamental phenomenon of quantum mechanics wherein a subatomic particle transitions through a potential energy barrier, despite possessing insufficient kinetic energy to overcome it classically. This effect is explained through the probabilistic nature of wavefunctions, where a particle's presence vanishes from one side of a potential well and reappears on the other side without any conventional current flowing within the barrier itself. This non-intuitive behavior, although negligible in larger devices, becomes increasingly significant in nanoscale semiconductor structures such as modern MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors).

3.3.2 Tunneling Concerns in Scaled MOSFETs

With aggressive downscaling of MOSFETs, reducing the gate oxide thickness is essential to enhance gate control and suppress short-channel effects. However, this approach introduces a critical challenge—quantum tunneling of carriers through the thin gate oxide. Though the resulting gate leakage current might be minor compared to the drain current (I_d), its cumulative impact substantially elevates the standby power consumption of the integrated circuit, especially in low-power applications.

The thickness of the gate dielectric directly influences the tunneling probability. A thicker oxide layer limits the extension of electron wavefunctions into the barrier, reducing tunneling effects. Conversely, in sub-2 nm silicon dioxide layers, electron wavefunctions penetrate the barrier easily, resulting in considerable gate leakage current due to tunneling [50][51].

3.3.3 Tunneling Mechanisms in MOSFETs

In scaled devices, several tunneling processes are observed:

- **Electron Conduction Band (ECB) Tunneling**: Dominates in n-MOSFETs, where electrons tunnel from the gate into the conduction band of the channel.

- **Hole Valence Band (HVB) Tunneling**: Prominent in p-MOSFETs, with holes tunneling into the valence band.

- **Electron Valence Band (EVB) Tunneling**: Occurs only under high gate voltages that exceed typical digital CMOS operating levels, rendering it negligible for practical circuit operation [52].

The prevalence of tunneling is strongly influenced by the energy band alignment and the barrier height, which itself is determined by the electron affinity difference between the oxide and the adjacent materials (metal or semiconductor). This creates a potential barrier given by:

$$E = q\chi \tag{3.8}$$

Where χ is the electron affinity of the oxide and q is the elementary charge.

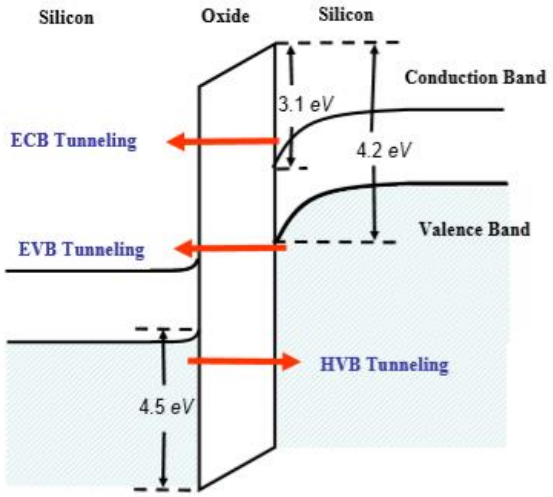


Fig 3.2 Energy band diagram for tunneling components in an MOS structure

3.3.4 Trapezoidal Potential Barrier and WKB Approximation

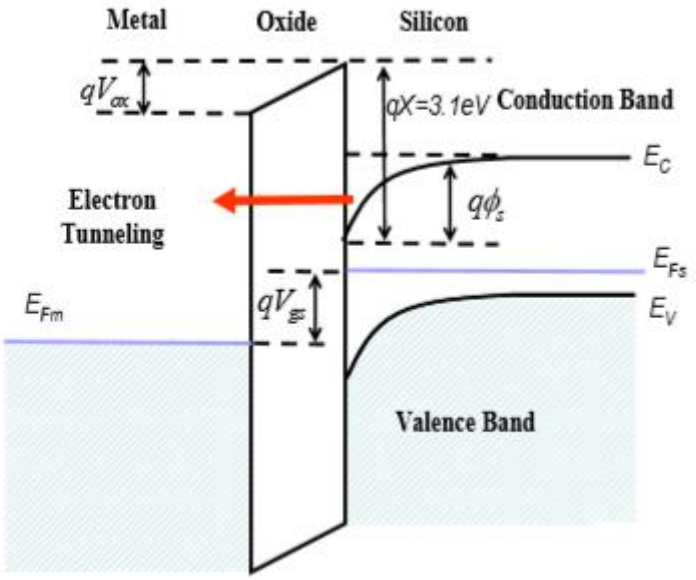


Fig 3.3 Potential at the junction

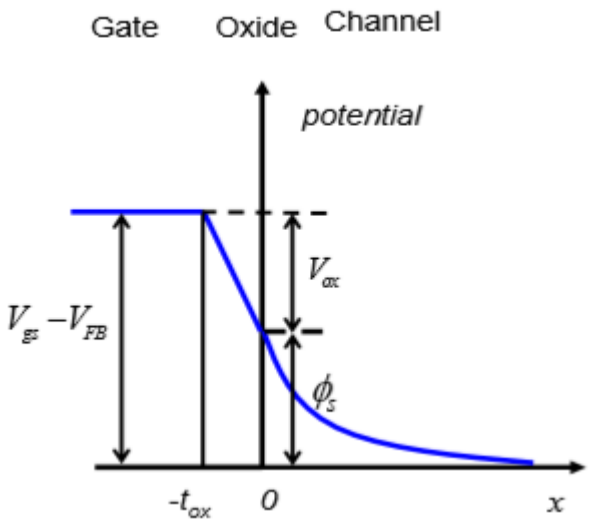


Fig. 3.4 Potential distribution in the gate-to-channel direction for a metal-gate MOSFET

Due to the applied gate-to-source voltage V_{gs}, the potential barrier assumes a trapezoidal shape. The voltage drop across the oxide is given as[53]:

$$V_{ox} = V_{gs} - V_{FB} - \phi_S \quad (3.9)$$

Where V_{FB} is the flat-band voltage and ϕ_S is the surface potential. Consequently:

$$qV_{gs} = E_{Fs} - E_{Fm} \tag{3.10}$$

Using the Wentzel–Kramers–Brillouin (WKB) approximation, the tunneling probability through a trapezoidal barrier is estimated as:

$$D(E_x) = -\frac{2}{\hbar}\int_{x1}^{x2}\sqrt{2m_{OX}(E_b(x) - E_x)}\,dx \tag{3.11}$$

Where:

- E_x is the electron's kinetic energy in the x-direction.
- t_{ox} is the oxide thickness.
- $m_{OX} = 0.35m_o$, the effective mass of the electron in the oxide.
- E_b is the average potential barrier height:

$$E_b(x) = q\chi + qV_{ox}.\frac{x}{t_{ox}} \tag{3.12}$$

3.3.5 Many-Electron Case and Fermi-Dirac Statistics

For systems with many electrons, individual electrons can occupy a continuum of energy states. The probability of occupancy of any energy level E is defined by the Fermi-Dirac distribution:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_f}{kT}\right)} \tag{3.13}$$

Where E_f is the Fermi energy, k is Boltzmann's constant, and T is the absolute temperature. Although hole tunneling is theoretically possible, the higher potential barrier for holes compared to electrons renders hole tunneling significantly less probable in typical device conditions.

3.3.6 Tunneling Effects in Polysilicon Gate Structures

In MOSFETs using polysilicon gates, the voltage drop across the gate itself must be accounted for. This causes an upward band bending near the polysilicon/oxide interface. The oxide voltage drop becomes:

$$V_{OX} = V_{gs} - \varphi_s - V_p \tag{3.14}$$

Where V_p is the voltage drop within the polysilicon gate given by:

$$V_p = \frac{1}{2}\left(\frac{q}{\epsilon_{Si}}\right) N_{Gate} X_{Gate}^2 \tag{3.15}$$

Here, N_{Gate} is the doping concentration and X_{Gate} is the gate depletion depth. For $V_{gs} > V_T$, the depletion width becomes:

$$X_{Gate} = \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} \sqrt{\left(1 + \frac{2\epsilon_{ox}^2 (V_{gs} - \varphi_s - V_{FB})}{q\, N_{Gate} \epsilon_{Si} t_{ox}^2}\right)} - 1 \tag{3.16}$$

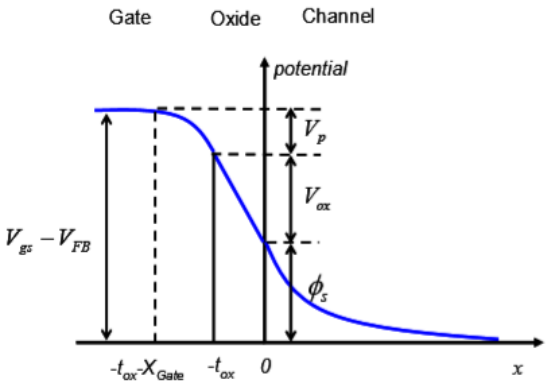


Fig. 3.5 Potential diagram for the poly-silicon gate MOSFET

As the gate voltage increases, polysilicon depletion leads to reduced electric field at the oxide interface. Therefore, the tunneling density in polysilicon gates is typically lower than that in metal gates at the same gate bias.

3.3.7 High-κ Gate Dielectrics as a Solution

To suppress direct tunneling while preserving gate control, the semiconductor industry has transitioned from conventional SiO_2 to high-dielectric constant (high-κ) materials like hafnium oxide (HfO_2) and hafnium silicate ($HfSiO_2$). These materials enable an increase in physical thickness while maintaining or

improving the gate capacitance, which is crucial for controlling short-channel effects without incurring excessive leakage[54].

The equivalent oxide thickness (EOT) of a high-κ dielectric compared to SiO_2 is defined as:

$$E_{OT} = \frac{\epsilon_{ox}}{\kappa\epsilon_o} t_1 \tag{3.17}$$

Where t_1 is the physical thickness of the high-κ dielectric, and κ is its relative dielectric constant. A higher κ value effectively reduces the EOT, enhancing gate control while suppressing quantum tunneling currents[55].

CHAPTER 4

QUANTIZATION MODEL

The quantization model is instrumental in mitigating short-channel effects (SCEs) in MOSFETs. Advancements in device technology have led to the adoption of highly doped channels and ultra-thin gate oxides. While the increased vertical electric field aids in maintaining gate control over the channel against drain potential influences, it also confines the movement of the narrow potential well[56].

From quantum theory, the energy levels of channel carriers are discrete rather than continuous, as predicted by classical models. This quantization leads to a redistribution of carrier density near the Si/SiO_2 interface compared to classical predictions.

$$|\Psi(x,t)|^2\,dx = \left\{ \begin{array}{l} \text{probability of finding the particle} \\ \text{between } x \text{ and } (x+dx), \text{ at time } t. \end{array} \right\}$$

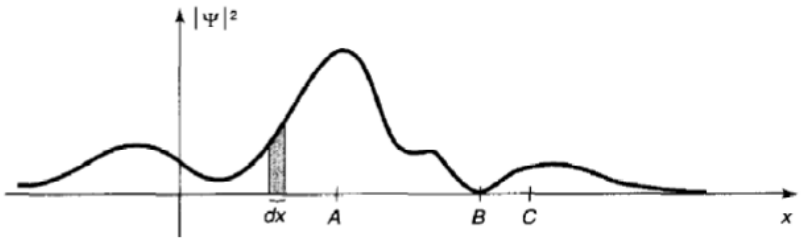


Fig. 4.1 Probability distribution

To analyze quantum mechanical effects (QMEs) in MOSFETs, it's essential to introduce the wave function characterizing inversion charges based on the Schrödinger equation:

$$-\frac{\hbar^2}{2m^*}\nabla^2\Psi(\mathrm{x},\mathrm{y}) - q\phi(x,y)\Psi(x,y) = E\Psi(x,y) \qquad (4.1)$$

Where:

- $\hbar$ is the reduced Planck's constant,
- m^* is the effective mass of electrons in silicon,
- $\Psi(x,y)$ is the electron wavefunction,
- q is the electron charge,
- $\phi(x,y)$ is the electric potential,
- E is the energy of the electrons.

The electric potential $\phi(x,y)$ is determined by the Poisson equation:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{q}{\epsilon_{Si}}\left(N_A+n(x,y)\right) \tag{4.2}$$

Where:

- ε_{Si} is the permittivity of silicon,
- N_A is the doping concentration of the channel,
- n(x,y) is the electron density.

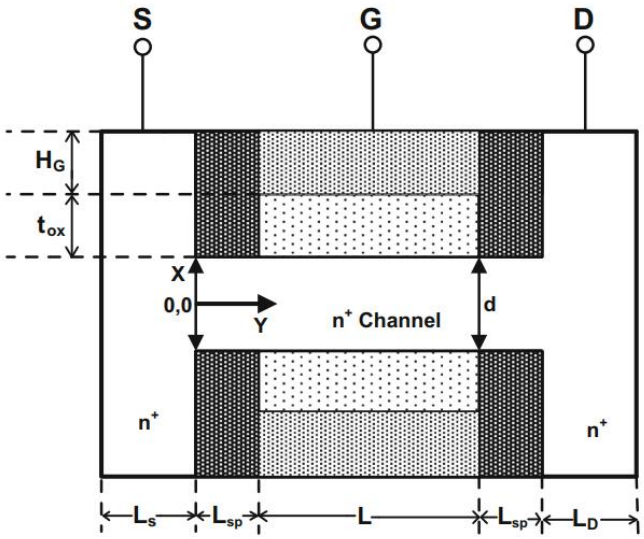


Fig. 4.2 Cross-sectional view of double gate junctionless transistor

Figure 2.1 illustrates a double-gate (DG) junctionless n-MOSFET. Here, H_G, t_{ox}, and d represent the thicknesses of the metal layer, oxide layer, and channel, respectively. L, L_{sp}, L_S, and L_D denote the lengths of the channel, spacer, source, and drain regions, respectively. The coordinate system is defined with the Y and X directions along and perpendicular to the channel, respectively, and the Z direction

along the channel's width. To solve for the actual DG junctionless MOSFET, we first consider a simplified approach by solving a one-dimensional (1D) Schrödinger equation for an infinite potential well.

4.1 ONE-DIMENSIONAL INFINITE POTENTIAL WELL

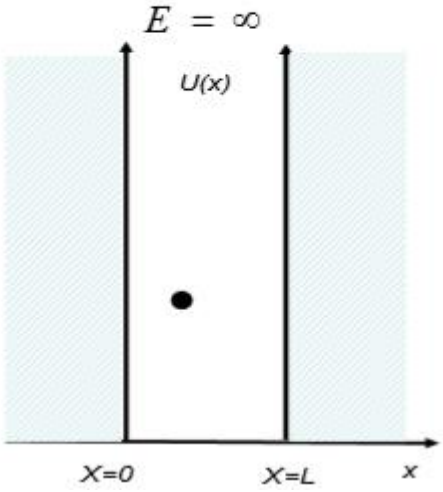


Fig. 4.3 Potential Well

In this model, the potential V(x)V(x)V(x) is defined as:

$$V(x) = \begin{cases} 0, & 0 < x < a \\ \infty, & x \leq 0 \end{cases} \tag{4.3}$$

The wave function Ψ(x)must vanish where V(x)=∞, leading to the boundary conditions:

$$\Psi(x) = 0 \forall x < 0, x > a \tag{4.4}$$

Within the interval 0<x<a0 < x < a0<x<a, the time-independent Schrödinger equation becomes:

$$\frac{d^2\Psi}{dx^2} = -\frac{2mE}{\hbar^2}\Psi \tag{4.5}$$

Letting $k^2 = \frac{2mE}{\hbar^2}$, we have:

$$\Rightarrow \frac{\partial^2 \Psi}{\partial x^2} = -k^2 \Psi \tag{4.6}$$

The general solution is:

$$\Psi(x) = c_1 \cos(kx) + c_2 \sin(kx) \tag{4.7}$$

Applying the boundary conditions:

1. $\Psi(0) = 0$ implies $c_1 = 0$,
2. $\Psi(a) = 0$ leads to $c_2 \sin(ka) = 0$, which implies $ka = n\pi$, where n=1,2, 3…n

Therefore, the normalized wave function is:

$$\Psi_n = \sqrt{\frac{2}{a}} \sin(n\pi x / a) \tag{4.8}$$

The corresponding energy levels are:

$$E = \frac{\hbar^2 k^2}{2m} = \frac{\hbar^2 \pi^2 n^2}{2ma^2} \forall n = 1,2,3,4, \ldots \tag{4.9}$$

This model provides a foundational understanding of quantum confinement in semiconductor devices.

4.2 TWO-DIMENSIONAL SCHRÖDINGER EQUATION IN A RECTANGULAR POTENTIAL WELL

Extending the analysis to two dimensions, consider a rectangular potential well where the potential energy U(x,y) is[57]:

$$U(x,y) = \begin{cases} 0, & x \leq \frac{d}{2} \\ \infty, & x \geq \frac{d}{2} \end{cases} \tag{4.10}$$

Assuming electron motion in the x and y directions, the two-dimensional Schrödinger equation is:

$$-\frac{\hbar^2}{2m^*}\nabla^2\Psi_n(x,y) - q\phi(x,y)\Psi_n(x,y) = E_n\Psi_n(x,y) \quad (4.11)$$

Within the well, where U(x,y)=0, the equation simplifies to[58]:

$$-\frac{\hbar^2}{2m^*}\left[\frac{\partial^2\Psi_n(x,y)}{\partial x^2}+\frac{\partial^2\Psi_n(x,y)}{\partial y^2}\right] = E_n\Psi_n(x,y) \quad (4.12)$$

Employing separation of variables:

$$\Psi(x,y) = X(x)Y(y) \quad (4.13)$$

Substituting into the equation yields:

1. For X(x):

$$\Rightarrow -\frac{\hbar^2}{2m^*}\left[\frac{\partial^2\Psi_n(x,y)}{\partial x^2}\right] = E_xX(x) \quad (4.14)$$

2. For Y(y):

$$\Rightarrow -\frac{\hbar^2}{2m^*}\left[\frac{\partial^2\Psi_n(x,y)}{\partial y^2}\right] = E_xY(y) \quad (4.15)$$

Where $E=E_x+E_y$.

Solving for X(x):

$$X(x) = A_x\sin(k_xx) + B_x\cos(k_xx) \quad (4.16)$$

Applying boundary conditions:

- $X(\frac{d}{2})=0$, (4.17)
- $X(-\frac{d}{2})=0$, (4.18)

We find that:

$$k = \frac{n\pi}{d}\forall n = 1,2,3,\ldots \quad (4.19)$$

Similarly, for Y(y), assuming infinite potential walls at y=0 and y=L:

$$Y(y) = A_y \sin(k_y y) + B_y \cos(k_y y) \tag{4.20}$$

Applying boundary conditions:

- Y(0)= 0, (4.21)
- Y(L)= 0, (4.22)

We deduce:

$$k = \frac{m\pi}{L} \forall n = 1,2,3, \ldots \tag{4.23}$$

The normalized wave function is[59]:

$$\Psi_{n,m}(x,y) = \sqrt{\frac{2}{d}} \sin \frac{n\pi x}{d} . \sqrt{\frac{2}{L}} \sin \frac{m\pi y}{L} \tag{4.24}$$

The energy levels are:

$$E_{n,m} = \frac{\hbar^2 \pi^2}{2m^*} \left(\frac{n^2}{d^2} + \frac{m^2}{L^2} \right) \tag{4.25}$$

These quantized energy states are pivotal in understanding the behavior of electrons in confined systems, such as quantum wells and nanostructures.

CHAPTER 5

BAND STRUCTURE AND PROPERTIES

The band structure of a solid is a fundamental concept in solid-state physics that describes the range of energy levels that electrons within a material can occupy. It is critical in determining whether a material behaves as a conductor, semiconductor, or insulator, based on the distribution and separation of these energy levels. Specifically, a band structure represents the allowed energy states of electrons as a function of their wave vector $\vec{k}$, which corresponds to momentum in a periodic crystal lattice [60][61].

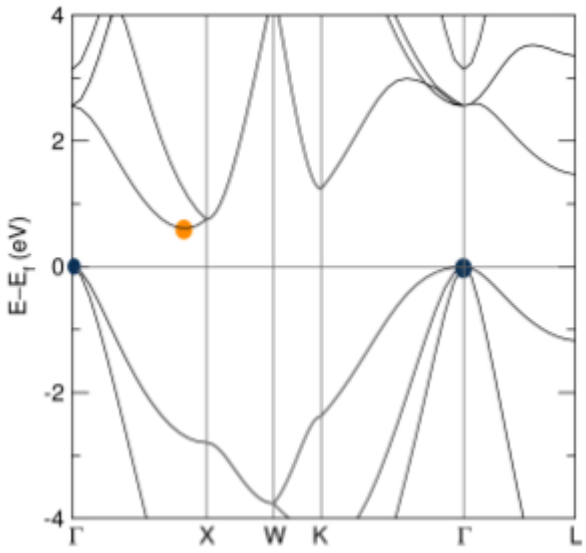


Fig. 5.1 Band Structure of Silicon

A band structure diagram is a graphical representation that maps the relationship between electron energy and momentum within the first Brillouin zone, a uniquely defined region in reciprocal space. These diagrams are often referred to as

"spaghetti plots" due to the tangled appearance of multiple energy bands. Despite their complexity, they allow researchers to extract crucial information about a material's electronic behavior. For instance:

- If the valence band maximum (VBM) and the conduction band minimum (CBM) do not overlap and are separated by an energy gap, the material is an insulator or a semiconductor, depending on the size of the gap [60].
- If these bands overlap or touch, the material exhibits metallic or semi-metallic behavior.
- The nature of the band gap (direct or indirect) is determined by whether the VBM and CBM occur at the same $\vec{k}$-point in the Brillouin zone.
- The curvature of the energy bands around the extrema indicates the effective mass of charge carriers, and thus provides insight into carrier mobility [62].

For instance, the band structure of silicon (Si) reveals that its CBM and VBM are located at different $\vec{k}$-points. The conduction band minimum lies near the X point, while the valence band maximum is near the Γ point. This results in an indirect band gap of approximately 1.1 eV at room temperature (though some computational models may estimate it around 0.62 eV due to underestimation in Density Functional Theory without advanced corrections) [63]. This indirect gap makes Si less efficient for optoelectronic applications like LEDs, where direct recombination of electrons and holes is desired.

The energy eigenvalues $E(\vec{k})$ that constitute the band structure are calculated using solutions to the Schrödinger equation with a periodic potential, as described by Bloch's theorem. These calculations are carried out in reciprocal space (k-space), which reflects the momentum characteristics of electrons rather than their positions [60][61]. The use of wave vector $\vec{k}$, representing the electron's crystal momentum, simplifies the problem by taking advantage of the periodicity of the lattice.

The crystal momentum (also known as quasi-momentum) is defined by:

$$\vec{p}_{crystal} = \hbar \vec{k} \tag{5.1}$$

Where:

- $\vec{p}_{crystal}$ is the crystal momentum,
- $\hbar$ is the reduced Planck's constant,
- $\vec{k}$ is the wave vector.

In crystals, the allowed $\vec{k}$-values are constrained to the first Brillouin zone, which is the Wigner-Seitz cell in reciprocal space [61]. This zone contains all the unique momentum states of electrons due to the periodic nature of the lattice.

For face-centered cubic (FCC) lattices—common in semiconductors such as GaAs, Si, and Ge—the Brillouin zone exhibits high-symmetry points labeled as Γ (center), X, L, and K, among others. The electronic band extrema often lie at or near these symmetry points. For example:

- In Silicon, the CBM is at the X point, and the VBM is at Γ → indirect gap [4].
- In Gallium Arsenide (GaAs), both CBM and VBM are at Γ → direct gap, which is optimal for photon emission [62].

Thus, band structure analysis serves as a powerful predictive tool for determining the electronic, optical, and transport properties of materials. Understanding how these bands arise, shift with strain, doping, or size (as in nanostructures), and interact with external fields is crucial for the design of semiconductor devices like transistors, solar cells, photodetectors, and quantum dots [62][63].

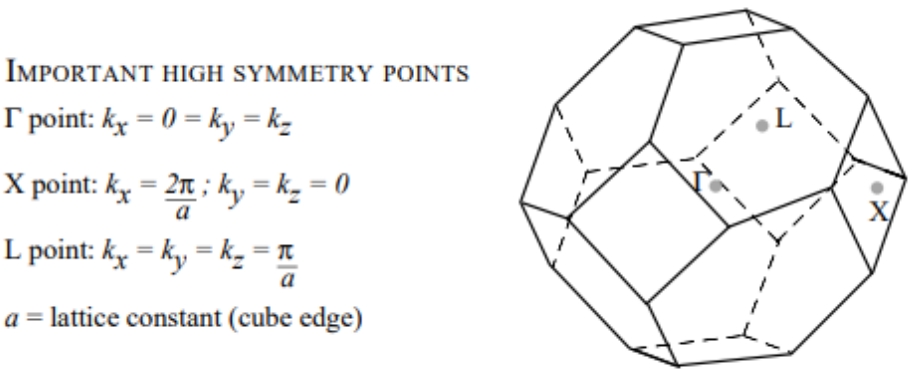


Fig. 5.2- Brillouin Zone for fcc lattice

To understand the origin of electronic band structures, it is necessary to begin with the quantum mechanical treatment of a free particle, particularly how its energy relates to its wavenumber k. This foundation is essential for progressing to the more complex periodic systems found in crystalline solids.

We start by solving the time-independent Schrödinger equation for a free particle moving in one dimension, where no external potential is acting on the system. The governing equation is:

$$-\frac{\frac{\hbar^2}{2m}\partial^2\Psi(x)}{\partial x^2} = E\Psi(x) \tag{5.2}$$

where:

- $\hbar$ is the reduced Planck constant,
- m is the mass of the particle,
- Ψ(x) is the spatial part of the wave function,
- and E is the total energy of the particle.

A trial solution to this differential equation, motivated by the wave-like nature of particles, is:

$$\Psi(x) = Ce^{ikx} \tag{5.3}$$

where C is a normalization constant, i=$\sqrt{-1}$, and k is the wavenumber, which characterizes the number of wave cycles per unit length. Substituting this into the Schrödinger equation yields:

$$\frac{\partial^2\Psi(x)}{\partial x^2} = i^2k^2Ce^{ikx} = -k^2Ce^{ikx} \tag{5.4}$$

$$\Rightarrow \frac{\frac{\hbar^2}{2m}\partial^2\Psi(x)}{\partial x^2} = \frac{\hbar^2}{2m}k^2Ce^{ikx} \tag{5.5}$$

$$\Rightarrow E\Psi(x) = \frac{\hbar^2}{2m}k^2\Psi(x) \tag{5.6}$$

Therefore, we obtain the energy–wavevector relation:

$$E = \frac{\hbar^2}{2m}k^2 \tag{5.7}$$

This quadratic dependence of energy on the wavevector k is a defining characteristic of free particle dispersion and forms the basis for understanding electron motion in crystalline solids [64][65].

To develop an intuitive understanding of the wavenumber k, we turn to the de Broglie hypothesis, which postulates the wave-particle duality of matter. The de Broglie relation is given as:

$$\lambda = \frac{h}{mv} = \frac{h}{p} \tag{5.8}$$

where:

- λ is the de Broglie wavelength of the particle,
- h is Planck's constant,
- p= mv is the linear momentum of the particle.

Instead of wavelength λ, we often use the wavenumber defined as:

$$k = \frac{2\pi}{\lambda} \tag{5.9}$$

which describes how many wave cycles fit into a unit distance. Combining the two expressions, the momentum p can be expressed as:

$$p = \hbar k \tag{5.10}$$

Substituting this into the classical kinetic energy expression:

$$E = \frac{1}{2}mv^2 = \frac{p^2}{2m} \tag{5.11}$$

$$\Rightarrow E = \frac{\hbar^2}{2m}k^2 \tag{5.12}$$

This re-derives the quantum mechanical result obtained from solving the Schrödinger equation, thereby reinforcing the consistency between classical and quantum interpretations of a free particle's energy [66].

The implications of this relation are profound. Even though kkk is defined in terms of inverse length (1/ length), it connects directly to momentum, wavelength, and energy. This is particularly crucial in the context of solid-state physics, where electrons are not entirely free but instead experience a periodic potential due to the ion cores in a crystal lattice.

By extending this simple model to periodic systems using Bloch's theorem, and considering the electron's behavior in the first Brillouin zone, one derives the electronic band structures fundamental to understanding semiconductors, insulators, and conductors. In such periodic systems, the same energy–wavevector relationship becomes more complex, leading to the formation of allowed energy bands and band gaps [64][67]. This foundational understanding is critical for interpreting

more advanced topics such as effective mass theory, density of states, and carrier dynamics in semiconductors.

5.1 JUSTIFICATION FOR PARABOLIC ENERGY BANDS

To explore the origin of parabolic energy bands, consider a one-dimensional chain of atoms. Suppose *n* atoms are arranged linearly, each separated by a uniform distance a*a*. The position of the n^{th} atom is denoted by x_n, while its equilibrium position is:

$$x_n^{eq} = na \tag{5.13}$$

The displacement from equilibrium is given by:

$$\delta x_n = x_n - x_n^{eq} \tag{5.14}$$

For simplicity, we restrict our analysis to motion along a single spatial dimension.

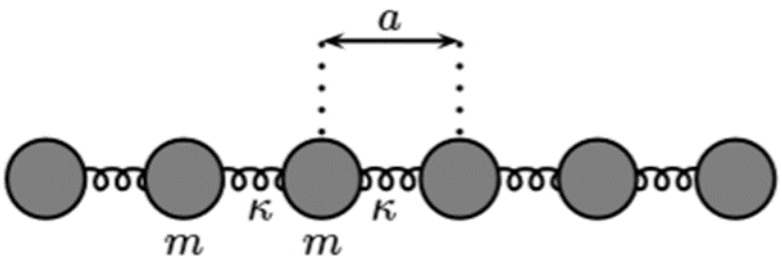


Fig. 5.3 The one-dimensional monatomic harmonic chain. Each ball has mass m and each spring has spring constant κ. The lattice constant, or spacing between successive masses at rest, is a.

At sufficiently low temperatures, atomic vibrations can be approximated using a harmonic potential, similar to that of a simple harmonic oscillator. Under this assumption, the total potential energy of the system becomes:

$$V_{TOT} = \sum V(x_{i+1} + x_i) = \sum \frac{k}{2}(x_{i+1} - x_i - a)^2 \tag{5.15}$$

$$\Rightarrow V_{TOT} = \sum \frac{k}{2}(\delta x_{i+1} - \delta x_i)^2 \tag{5.16}$$

The force acting on the n^{th} atom is derived from the gradient of the total potential energy:

$$F_n = -\frac{\partial V_{TOT}}{\partial x_n} = k(\delta x_{n+1} - \delta x_n) + k(\delta x_{n-1} - \delta x_n) \tag{5.17}$$

Which simplifies to:

$$F_n = k(\delta x_{n+1} + \delta x_{n-1} - 2\delta x_n) \tag{5.18}$$

Assuming a wave-like solution of the form:

$$\delta x_n = Ae^{iwt - ikx_n^{eq}} = Ae^{iwk - ikna} \tag{5.19}$$

Substituting into the equation of motion yields:

$$-m\omega^2 Ae^{i\omega t - ikna} = kAe^{i\omega t}e^{-ika(n+1)} \tag{5.20}$$

$$m\omega^2 = 2k(1 - \cos ka) = 4ksin^2\frac{ka}{2} \tag{5.21}$$

Solving this leads to the dispersion relation:

$$\omega = 2\sqrt{\frac{k}{m}}\left|\sin\frac{ka}{2}\right| \tag{5.22}$$

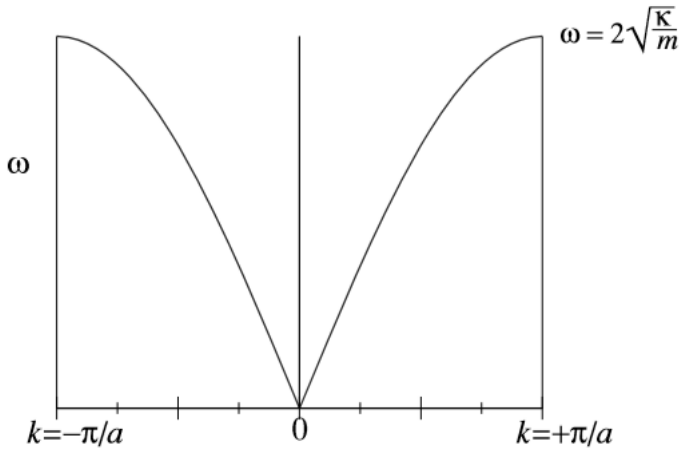


Fig. 5.4 Dispersion relation for vibrations of the one-dimensional monatomic harmonic chain. The dispersion is periodic in k → k +2π/a

This expression describes the dispersion relation, which is inherently periodic due to the sinusoidal dependence on k. In the long-wavelength limit (small k), the sine function can be approximated linearly, leading to a quadratic dependence of energy on wavevector. This quadratic behavior is characteristic of parabolic energy bands. A similar approach can be extended to tight-binding models and three-

dimensional lattices, where the resulting energy-momentum relations also exhibit parabolic characteristics near the band extrema.

5.2 RECIPROCAL LATTICE AND THE BRILLOUIN ZONE

In the previous discussion, we plotted the dispersion relation only within the interval $-\frac{\pi}{a} \leq k \leq \frac{\pi}{a}$. This restriction is not arbitrary—it reflects a fundamental property of periodic systems: the dispersion relation is inherently periodic in wavevector, such that:

$$k \rightarrow k + \frac{2\pi}{a} \tag{5.23}$$

This periodicity arises from the underlying periodic structure in real space. More generally, any system with spatial periodicity aa will exhibit a corresponding periodicity of $\frac{2\pi}{a}$ in reciprocal space (also known as k-space).

This concept implies that if a system remains unchanged under a spatial translation $x \rightarrow x + a$, then in reciprocal space, the dispersion relation remains invariant under $k \rightarrow k + \frac{2\pi}{a}$. The smallest repeating unit in k-space is referred to as the Brillouin zone, with the first Brillouin zone defined as the region centered around k=0, typically spanning from −π/a to π/a. The points $k = \pm\frac{\pi}{a}$ are symmetric about the origin and are separated by $\frac{2\pi}{a}$.

It is worth reflecting on why the dispersion curve repeats with $k \rightarrow k + \frac{2\pi}{a}$. This periodicity means that a wavevector shifted by $\frac{2\pi}{a}$ describes a physically indistinguishable oscillation mode from the original. Mathematically, this is because:

$$e^{-i2\pi np} = 1 \tag{5.24}$$

for any integer p*p*, which implies that wavefunctions differing by integer multiples of 2*π*/*a* in wavevector are identical at all lattice points.

This leads to the definition of the reciprocal lattice—a set of wavevectors in k-space that are physically equivalent to k=0. In contrast, the original set of atomic positions xn=na forms the direct lattice (or real-space lattice). These can be expressed as:

$$x_n = \cdots -2a, -a, 0, a, 2a, \ldots \tag{5.25}$$

$$G_n = \cdots -2\left(\frac{2\pi}{a}\right), -\frac{2\pi}{a}, 0, \frac{2\pi}{a}, 2\left(\frac{2\pi}{a}\right), \ldots \tag{5.26}$$

A defining property of the reciprocal lattice is that for any reciprocal lattice vector G_m, the following condition holds for all real-space lattice points x_n:

$$e^{iG_m x_n} = 1 \tag{5.27}$$

This condition ensures that Gm is a valid member of the reciprocal lattice.

However, this equivalence between k and $k+G_m$ can be conceptually challenging. For instance, we often associate a wavevector kk with a wavelength $\lambda=2\pi/k$. But if k and $k+G_m$ are physically indistinguishable, which wavelength should we use—$\frac{2\pi}{k}$ or $\frac{2\pi}{k+Gm}$?

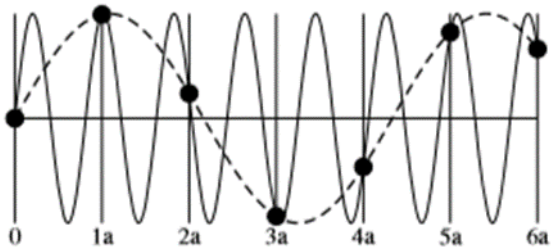


Fig. 5.5 Symmetry Points

The resolution lies in recognizing that this equivalence only holds at discrete lattice points $x_n=na$. Between these points, the wavefunctions corresponding to k and $k+\frac{2\pi}{a}$ differ. Therefore, it is meaningless to assign a unique wavelength based solely on the wavevector when sampling is restricted to lattice points. This phenomenon, where different wavevectors yield indistinguishable results at discrete sampling points, is known as aliasing.

CHAPTER 6

EFFECTIVE MASS AND ORIENTATION

6.1 EFFECTIVE MASS AND DISPERSION

Within the framework of the tight-binding model, the energy spectrum of electrons in a periodic potential is given by:

$$E = E_0 - 2tcoska \tag{6.1}$$

Unlike the case of free electrons, this dispersion relation exhibits both a maximum and a minimum energy, meaning that electrons can only occupy states within a specific energy range—referred to as an energy band. The term "band" is used to describe both this energy interval and the continuous segment of the dispersion curve associated with it.

The dispersion relation—the functional dependence of energy on wavevector k—plays a central role in determining how electrons respond to external forces. In quantum mechanics, electrons behave as wave packets, and their motion is governed by the group velocity, which is derived from the dispersion relation. When an electric field is applied, it shifts the wavevectors of the components of the wave packet, causing the electron to accelerate. Thus, the electron's response to forces is entirely dictated by the shape of the dispersion curve [68]. For a free electron, the dispersion is:

$$E = \frac{\hbar^2 \mathrm{k}^2}{2m} \tag{6.2}$$

where m is the actual mass of the electron. However, near the bottom of a conduction band in a solid, the dispersion takes the form:

$$E = \frac{\hbar^2 \mathrm{k}^2}{2m^*} \tag{6.3}$$

Here, m* is the effective mass, which characterizes how the electron behaves under external forces in the crystal. This effective mass is not a physical mass but a parameter derived from the curvature of the band structure.

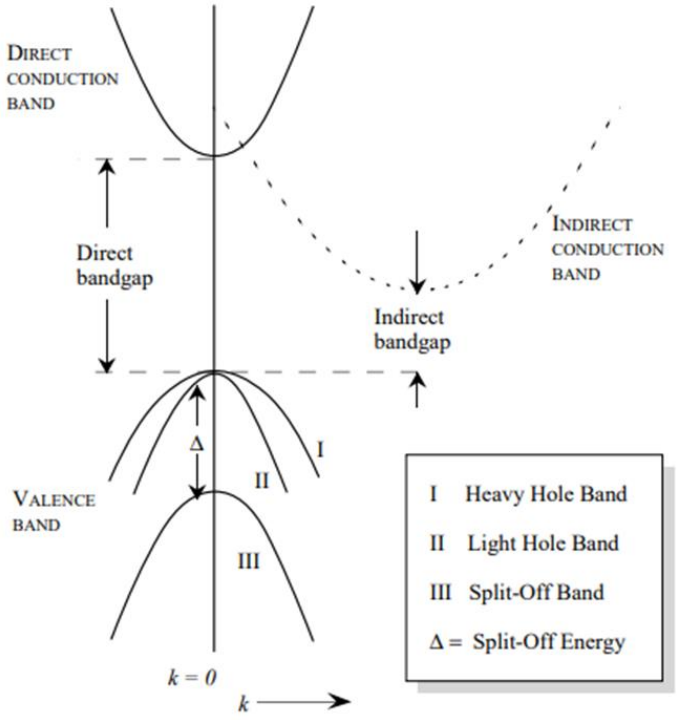


Fig. 6.1 Different type of bandgap

Interestingly, near the top of the valence band, the dispersion still has the same form but with a negative effective mass. This implies that electrons near the valence band maximum move in the opposite direction to the applied force. This counterintuitive behavior arises purely from the curvature of the band and is independent of whether the band is full or empty. If a single electron were placed near the top of the valence band (a hypothetical and unstable scenario), it would move "backward" in response to a force.

The bandwidth—the energy difference between the top and bottom of the band—defines the range of energies for which k-states exist. Outside this range, no such states are available. The formation of this band structure is due to hopping between atomic orbitals, which causes some states to shift below and others above the

original atomic energy level ϵ_0. This is analogous to the formation of bonding and antibonding orbitals in molecular systems [69]

When the band is partially filled, the total energy of the electrons decreases as atoms are brought closer together and the bandwidth increases. This energy reduction contributes to the metallic bonding in solids. The mobility of electrons in metals allows them to adjust their positions as the lattice deforms, which explains why metals are typically soft and malleable.

Near the bottom of the band, the dispersion can be approximated as parabolic. Expanding for small kk, we get:

$$E(k) = constant + ta^2k^2 \tag{6.4}$$

For t<0, the energy minimum occurs at the Brillouin zone boundary k=π/a, and the expansion would be centered around that point instead. This parabolic behavior mirrors that of free electrons:

$$E_{free}(k) = \frac{\hbar^2}{2m}k^2 \tag{6.5}$$

To match this form, we define the effective mass m∗ such that:

$$\frac{\hbar^2k^2}{2m^*} = ta^2k^2 \tag{6.6}$$

$$\Rightarrow m^* = \frac{\hbar^2}{2ta^2} \tag{6.7}$$

Thus, the effective mass encapsulates how the electron behaves dynamically in the crystal, and it depends entirely on the hopping parameter t, not on the actual electron mass. It's also important to note that the wavevector k in this context represents the crystal momentum, a quantum number arising from the periodicity of the lattice.

6.2 EFFECTIVE MASS OF THE ELECTRON

Near the bottom of the conduction band, the energy of an electron can be approximated by a quadratic expansion:

$$E = E_{min} + \alpha(k - k_{min})^2 + \cdots \tag{6.8}$$

From this expression, the effective mass m∗ is defined through the second derivative of energy with respect to wavevector k:

$$\frac{\hbar^2}{m^*} = \frac{\partial^2 E}{\partial k^2} = 2\alpha \tag{6.9}$$

This effective mass characterizes how an electron responds to external forces within the crystal. Importantly, it is not the actual mass of the electron but a parameter derived from the curvature of the energy band [70]

In modern solid-state physics, it is conventional to define the effective mass of holes—which are the absence of electrons near the top of the valence band—as positive, even though the curvature of the band is downward. The energy of a hole near the valence band maximum is given by:

$$E_{hole} = constant + \frac{\hbar^2(k - k_{max})^2}{2m^*_{hole}} \tag{6.10}$$

Additionally, the energy associated with the absence of an electron in a given k-state is the negative of the energy of the electron in that state:

$$E(absence\ of\ e^-\ in\ k\ state) = -E(electron\ in\ k\ state) \tag{6.11}$$

This inversion is essential in understanding hole dynamics in semiconductors.

6.3 VALLEYS IN BAND STRUCTURES

For simplicity, we neglect the spin of the electron in this discussion. However, in general, spin–orbit coupling can influence the dispersion relation, leading to spin-dependent band structures and modifying properties such as the effective g-factor of electrons.

In many semiconductors, the conduction band minimum does not occur at a single point in the Brillouin zone. Instead, there may be multiple equivalent minima,

known as valleys, located at different k-points but having the same energy. This phenomenon arises due to the crystal symmetry.

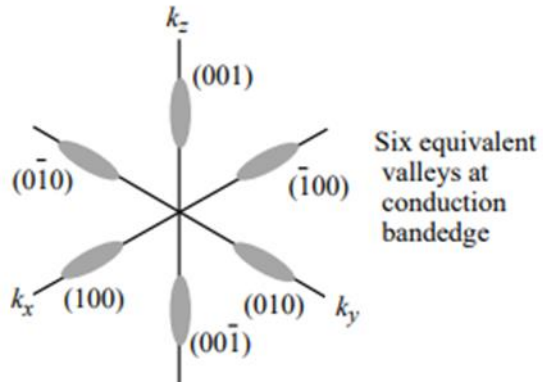


Fig. 6.2 Valleys at conduction bandedge

For instance, in silicon, which has a face-centered cubic (FCC) lattice with a basis, there are six equivalent conduction band minima located approximately at (±5.3/a, 0,0), (0,±5.3/a,0), and (0,0,±5.3/a). These are referred to as valleys, and the presence of multiple valleys is a key feature in valleytronics and advanced semiconductor physics[71].

Each valley exhibits anisotropic effective mass, characterized by:

- A longitudinal mass $m_{e,l}^*$ along the direction of the valley.
- Two transverse masses $m_{e,t}^*$ in the perpendicular directions.

In silicon, these values are:

$m_{e,l}^*=0.97m_0$, $m_{e,t}^*=0.19m_0$

where $m_0=9.11\times10-31$ kg is the free electron mass. This anisotropy significantly affects charge transport and mobility in semiconductors.

6.4 MILLER INDICES AND ⟨100⟩ ORIENTATION

Miller indices are a standardized notation system used in crystallography to describe the orientation of planes and directions within a crystal lattice. Each set of

planes is identified by a triplet of integers (hkℓ), known as the Miller indices, which correspond to the intercepts of the plane with the crystallographic axes. These indices are derived from the reciprocal of the intercepts and are typically reduced to their smallest integer values [72]

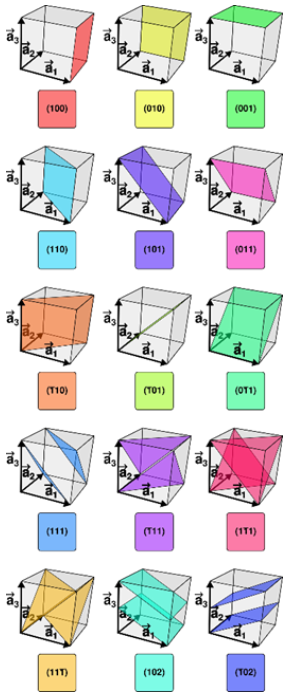


Fig. 6.3 Miller Indices

In this notation:

- Negative integers are denoted with a bar (e.g., 3 for −3).
- The indices are written in parentheses (hkl) to denote planes.
- Square brackets [hkl] indicate a specific direction.
- Angle brackets ⟨hkl⟩ represent a family of equivalent directions due to crystal symmetry.
- Curly braces {hkl} denote a family of equivalent planes.

For example, in a cubic crystal system, the directions [100],[010], and [001] are all symmetry-equivalent and collectively represented as ⟨100⟩. Similarly, the planes (100), (010), and (001) are grouped as {100} [73].

Although the primitive lattice vectors in face-centered cubic (FCC) and body-centered cubic (BCC) structures are not orthogonal, Miller indices are typically defined with respect to the cubic supercell, allowing them to align with Cartesian directions for simplicity.

In this research, we focus on the ⟨100⟩ orientation of silicon, a choice driven by its favorable surface properties. The ⟨100⟩ surface of silicon exhibits a lower atomic density compared to other orientations, which results in fewer dangling bonds. This reduction in surface states leads to enhanced carrier mobility, making it a preferred orientation in semiconductor device fabrication.

CHAPTER 7

DENSITY OF STATES

In solid-state and condensed matter physics, the density of states (DOS) describes the number of quantum states available for occupation at each energy level. It is typically expressed as a probability density function and represents an average over space and time for the system's accessible states. The DOS is fundamentally linked to the system's dispersion relation, which defines how energy varies with wavevector k. A high DOS at a particular energy implies a large number of available states at that energy[74].

In semiconductors, the DOS plays a critical role near the band edges. For instance, in the conduction band, as the electron energy increases, more states become available. Conversely, within the band gap, the DOS is zero, indicating no available states. This implies that an electron at the conduction band edge must lose at least the band gap energy to transition to the valence band.

The DOS can be defined for various quantum systems—electrons, phonons, or photons—and can be expressed as a function of either energy or wavevector. To convert between these forms, the dispersion relation E(k) must be known[75]. The mobile charge carrier density n(x) is given by:

$$n(x) = \frac{1}{\Delta V} \sum_{i=1.j=1}^{j=2} \left[g_{i=1} \int_{-\frac{d}{2}}^{\frac{d}{2}} |\psi(x)|^2 \partial x \right] \tag{7.1}$$

Where g_i=1 is the degeneracy of the i^{th} valley and $\Delta V = Wd\Delta L$ is the volume element. Alternatively:

$$n(x) = \int_{E_{i,j}}^{\infty} g(E) f(E) \partial E \tag{7.2}$$

Or

$$n(x) = \int_{E_{i,j}}^{\infty} D(E) f(E) \partial E \tag{7.3}$$

Here, D(E) is the 1D density of states, and f(E) is the Fermi-Dirac distribution function. In 1D systems, the allowed wavevectors are:

$$k_x = \frac{n\pi}{d} \tag{7.4}$$

The total number of states is calculated by evaluating the volume of 1/8 of a sphere in k-space and dividing by the volume of a single state:

$$N = 2 \times \frac{1}{8} \times \left(\frac{d}{\pi}\right)^3 \times \frac{4}{3} \times \pi \times k^3 \tag{7.5}$$

Differentiating with respect to energy:

$$\frac{dN}{dE} = \frac{dN}{dk} \times \frac{dk}{dE} = \frac{\left(\frac{d}{\pi}\right)^3 \pi k^3 dk}{dE} \tag{7.6}$$

Given:

$$E = \frac{\hbar^2 k^2}{2m^*} \Rightarrow \frac{dk}{dE} = \frac{m^*}{\hbar^2 k} \tag{7.7}$$

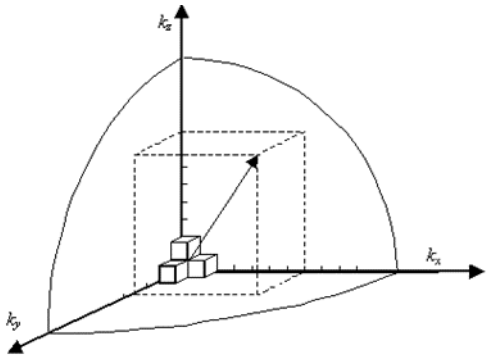


Fig. 7.1 Solution of different value of k

The 1D density of states becomes:

$$g_{c,1D} = \frac{dN_{1D}}{dE} = \sqrt{\frac{2\pi m^*}{\hbar^2}} \frac{1}{\sqrt{E - E_{min}}} \forall E \geq E_{min} \tag{7.8}$$

7.1 MAIN CALCULATIONS

Assuming a ⟨100⟩ orientation of silicon, we consider two valleys with effective masses $0.19m_0$ (i = 1) and $0.97m_0$ (i = 2). Since over 90% of electrons occupy the lowest sub-band $E_{1,1}$ we simplify the Poisson equation as:

$$\frac{\partial^2\varphi(x)}{\partial x^2} = \frac{q}{\epsilon_{Si}}N_D + \frac{Q_{1,1}}{q\epsilon_{Si}} + \frac{Q_{1,2}}{q\epsilon_{Si}} \tag{7.9}$$

The 1D mobile charge carrier density is:

$$n_{1D}(x) = \frac{g_{i=1}\sqrt{2m^*_{d,i}}}{W\hbar d\pi}\int_{E_{i,j}}^{\infty}\frac{\left(E - E_{i,j}\right)^{-\frac{1}{2}}dE}{1 + e^{\frac{E-E_{Fn}}{kT}}} \tag{7.10}$$

Using the substitution $\varepsilon = \frac{E-E_{i.j}}{k_bT}$, we get:

$$n_{1D}(x) = \frac{g_{i=1}}{w_d}\sqrt{\frac{2m^*_{d,i}kT}{\pi\hbar^2}}\int\left(\frac{\varepsilon^{-\frac{1}{2}}}{1 + e^{\varepsilon-\eta_F}}\right)\partial\varepsilon \tag{7.11}$$

$$\Rightarrow n_{1D}(x) = \frac{g_{i=1}}{w_d}\sqrt{\frac{2m^*_{d,i}kT}{\pi\hbar^2}}F_{-\frac{1}{2}}(\eta_F) \tag{7.12}$$

Where:

$$\eta_F = \frac{E_F - E_{i,j}}{kT} \tag{7.13}$$

7.2 FERMI DIRAC SOLUTION

The general Fermi-Dirac integral is defined as:

$$F_j = \frac{1}{\Gamma(j+1)}\int_0^{\infty}\frac{\varepsilon^j\partial\varepsilon}{1 + \exp(\varepsilon - \eta_F)} \tag{7.14}$$

For degenerate semiconductors:

$$F_m(x) = \left(\frac{E_{Fn} - E_{i.j}}{kT}\right)^{m+1} \tag{7.15}$$

For non-degenerate semiconductors:

$$F_m(x) = exp\left(\frac{E_{Fn} - E_{i.j}}{kT}\right) \tag{7.16}$$

Thus, the final charge densities are:

$$Q_{1,1} = \frac{g_{i=1}}{Wd}\sqrt{\frac{2m_{d,1}^{*}kT}{\pi\hbar^2}}e^{\frac{E_{Fn}-E_{1,1}}{kT}} \tag{7.17}$$

$$Q_{1,2} = \frac{g_{i=1}}{Wd}\sqrt{\frac{2m_{d,1}^{*}kT}{\pi\hbar^2}}e^{\frac{E_{Fn}-E_{1,2}}{kT}} \tag{7.18}$$

These expressions are essential for modeling carrier distributions in low-dimensional semiconductor systems [74][75][76].

CHAPTER 8

SURFACE POTENTIAL AND THRESHOLD VOLTAGE MODEL

8.1 SURFACE POTENTIAL

The electrostatic potential in the surface region of a silicon semiconductor is governed by Poisson's equation, which relates the electric field to the local charge distribution. The energy expression is given by:

$$E^2(x) = \left(\frac{\partial\psi}{\partial x}\right)^2 = \frac{2kTN_a}{\varepsilon_{Si}}\left[\left(e^{-\frac{q\psi}{kT}} + \frac{q\psi_s}{kT} - 1\right) + \frac{n_i^2}{N_a^2}\left(e^{\frac{q\psi}{kT}} - \frac{q\psi_S}{kT} - 1\right)\right] \quad (8.1)$$

This equation typically requires numerical methods for a full solution. However, in the depletion region, where $2\psi_B > \psi > \frac{kT}{q}$, the dominant term simplifies the expression to:

$$E = \sqrt{\frac{2qN_a\psi}{\epsilon_{Si}}}, \frac{\partial\psi}{\partial x} = -\sqrt{\frac{2qN_a\psi}{\epsilon_{Si}}} \quad (8.2)$$

Integrating both sides:

$$\int_{\psi_S}^{\psi} \frac{\partial\psi}{\sqrt{\psi}} = \int_0^x \sqrt{\frac{2qN_a}{\epsilon_{Si}}}\,dx \quad (8.3)$$

$$\Longrightarrow \psi = \psi_S\left(1 - \sqrt{\frac{2qN_a}{2\varepsilon_{Si}\psi_S}}\,x\right)^2 \quad (8.4)$$

This parabolic potential profile is a standard approximation in MOS capacitor modelling[77].

Assuming a 2D potential of the form:

$$\varphi(x,y) = \varphi_1(y) + x\varphi_2(y) + x^2\varphi_3(y) \tag{8.5}$$

and applying boundary conditions:

- $\varphi\left(\pm\frac{d}{2}, y\right) = \varphi_S(y)$ (8.6)
- $\frac{\partial\varphi(x,y)}{\partial x}_{x=0} = 0$ (8.7)
- $\frac{\partial\varphi(x,y)}{\partial x}|_{x=\pm\frac{d}{2}} = \frac{C_{ox}}{\epsilon_{Si}}[V_{GS} - \varphi_S(x) - V_{FB}]$ (8.8)

we derive:

$$\varphi(x,y) = \varphi_s(y)\left[1 + \frac{dC_{ox}}{4\varepsilon_{Si}}\right] - \frac{dC_{ox}}{4\varepsilon_{Si}}[V_{gs} - V_{fb}] - \frac{x^2 C_{ox}}{d\varepsilon_{Si}}[V_{gs} - V_{fb} - \varphi_s(y)] \tag{8.9}$$

This expression captures the electrostatic potential distribution in the channel under gate control [78].

Now the 2D Poisson equation for the electrostatic potential becomes:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = \frac{qN_D}{\varepsilon_{Si}} + \frac{1}{\varepsilon_{Si}}[Q_{(1,1)} + Q_{(1,2)}] \tag{8.10}$$

This can be separated into:

- A 1D Poisson equation:
$$\frac{\partial^2\varphi(x,y)}{\partial x^2} = \frac{qN_D}{\varepsilon_{Si}} + \frac{1}{\varepsilon_{Si}}[Q_{(1,1)} + Q_{(1,2)}] \tag{8.11}$$
- And a 2D Laplace equation:
$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = 0 \tag{8.12}$$

Solving this using Fourier series expansion and boundary conditions, we obtain:

$$\varphi_S(x,y) = \sum_{r=1}^{\infty} \frac{1}{\sinh\rho y} \times [V_r' \sinh\rho y + V_r \sinh\rho(L-y)] \times \left[\sin\rho x + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} d\rho \cos\rho x\right] \tag{8.13}$$

The final expression for the potential includes:

$$\varphi(x,y) = \frac{e^{\rho L} - 1}{2\sinh \rho L}\left[e^{-\rho y} + e^{\rho(y-L)}\right](V_b + \beta) + \frac{V_{ds}\cos \rho y}{2\sinh \rho L} - \beta \tag{8.14}$$

Where:

$$\rho = \frac{\frac{4C_{ox}}{d}}{\sqrt{1 + \frac{dC_{ox}}{4\varepsilon_{Si}} - \frac{x^2 C_{ox}}{d}}} \tag{8.15}$$

And the minimum surface potential is:

$$\varphi_s|_{min} = 2\sqrt{c_1 c_2} - \beta \tag{8.16}$$

These expressions are essential for modeling short-channel effects, threshold voltage roll-off, and electrostatic integrity in modern nanoscale MOSFETs[79].

8.2 THRESHOLD VOLTAGE

To evaluate the impact of quantum mechanical effects (QME) on the threshold voltage of a double-gate (DG) junctionless MOSFET, we define the shift in threshold voltage as:

$$\Delta V_{TH} = V_{TH1QM} - V_{TH1CL} \tag{8.17}$$

This difference is derived based on the depletion depth in both classical and quantum mechanical models[80].

8.2.1 Classical Model

The classical depletion charge is given by:

$$Q_{CL} = \int_0^{\infty} qN_D \exp\left(-\frac{q\varphi_S}{kT}\right) dx \tag{8.18}$$

Assuming $\phi p(x) \equiv \psi_S$, and applying the 1D Poisson equation:

$$\frac{\partial^2 \varphi_s}{\partial x^2} = \frac{qN_D}{\varepsilon_{Si}}\left[1 + e^{\frac{q\varphi_s}{kT}}\right] \tag{8.19}$$

Integrating:

$$\int_0^{\frac{d\varphi_s}{dx}} \frac{d\varphi_s}{dx} d\left(\frac{d\varphi_s}{dx}\right) = \frac{qN_D}{\varepsilon_{Si}} \int_0^{\varphi} 1 + \exp\left(\frac{q\varphi_s}{kT}\right) d\varphi \tag{8.20}$$

Thus, the total charge density becomes:

$$Q_T = \varepsilon_{Si} E|_{x=\pm\frac{d}{2}} \tag{8.21}$$

With boundary conditions:

$$\frac{d\varphi}{dx}|_{x=0} = 0 and \varphi\left(\pm\frac{d}{2}\right) = \varphi_s \tag{8.22}$$

This leads to:

$$Q_T = \sqrt{2qN_D\varepsilon_{Si}}\left[\varphi_s - \varphi_0 + \frac{1}{\beta}\left(e^{\varphi_s\beta} - e^{\varphi_0\beta}\right)\right]^{\frac{1}{2}} \forall\beta = \frac{q}{kT} \tag{8.23}$$

Approximating:

$$Q_T = \frac{qL_D^2 N_D}{x_{d.CL}}\left\{1 - e^{-\frac{q^2 N_D d^2}{8kT\varepsilon_{Si}}}\right\} e^{\frac{q\varphi_s}{kT}} \tag{8.24}$$

Where:

$$L_d is the debye length given by: \sqrt{\frac{\varepsilon_{Si}}{qN_D\lambda}} \forall\lambda = \frac{kT}{q} \tag{8.25}$$

At threshold:

$$Q_T(\varphi_S)|_{\varphi_s=2\varphi_F} = \frac{qL_D^2 N_D}{x_{d,CL}} \tag{8.26}$$

8.2.2 Quantum Mechanical Effects

In the quantum model, the inversion charge is:

$$Q_{1,1} = qN_{1D,DOS}e^{\frac{E_F - E_{1,1}}{kT}} \tag{8.27}$$

Taking logarithms:

$$kTln\left(\frac{Q_{1,1}}{qN_{1D,DOS}}\right) = E_F - E_{1,1} \tag{8.28}$$

At threshold, the gate voltage shifts the Fermi level:

$$qV_{gs} = q\varphi_s - q\varphi_F - \frac{E_g}{2} \tag{8.29}$$

Substituting:

$$\frac{qN_D x_{d,Qm}^2}{2\varepsilon_{Si}} = E_{1,1} + q\varphi_F + \frac{E_g}{2} + kTln\left|\frac{Q_{1,1}}{qN_{1D.DOS}}\right| - \varphi_0 \tag{8.30}$$

Comparing with the classical model:

$$x_{qm}^2 - x_{d,CL}^2 = \frac{2\varepsilon_{Si}}{q^2 N_D}\{E_{1,1} - q\varphi_0\} + 2L_D^2 \ln\left(\frac{\frac{Q_{1,1}}{qN_D}N_{DOS3}}{N_{DOS1}}\right) \tag{8.31}$$

$$x_{d.qm} = x_{d.CL}\left\{1 + \frac{\{E_{1,1} - q\varphi_0\}}{2q\varphi_F}\right\}^{\frac{1}{2}} \tag{8.32}$$

8.2.3 Combined Model

The shift in depletion depth is:

$$\Delta x = x_{d.qm} - x_{d.CL} = \sqrt{\frac{4\varepsilon_{Si}}{qN_D}}\left[\sqrt{1 + \frac{\{E_{1,1} - q\varphi_0\}}{2q\varphi_F}} - 1\right] \tag{8.33}$$

The corresponding shift in surface potential:

$$\Delta\phi_s = \frac{qN_D}{2\varepsilon_{Si}} \times \frac{2\varepsilon_{Si}}{q^2 N_D}\left[E_{1,1} - q\phi_0\right] \tag{8.34}$$

Now, using:

$$\Delta V_{GS} = \Delta\varphi_s \left[\frac{dV_{GS}}{d\varphi_s}|_{\varphi_s = 2\varphi_F}\right] \tag{8.35}$$

From MOS capacitor theory:

$$V_{GS} = V_{FB} + \varphi_S + \frac{\sqrt{2\varepsilon_{Si}\varphi_S qN_D}}{C_{ox}} \tag{8.36}$$

Differentiating:

$$\frac{dV_{GS}}{d\varphi_s}|_{\varphi_s = 2\varphi_F} = 1 + \frac{1}{2C_{ox}}\sqrt{\frac{q\varepsilon_{Si}N_D}{2\varphi_F}} \tag{8.37}$$

Thus, the final expression for threshold voltage shift is:

$$\Delta V_{Th} = \Delta V_{GS} = \Delta\varphi_s\left(\frac{dV_{GS}}{d\varphi_s}|_{\varphi_s = 2\varphi_F}\right) = \frac{E_{1,1} - q\varphi_0}{q}\left(1 + \frac{1}{2C_{ox}}\sqrt{\frac{q\varepsilon_{Si}N_D}{2\varphi_F}}\right) \tag{8.38}$$

This model captures the quantum confinement-induced shift in threshold voltage for DG junctionless MOSFETs [80][81][82].

CHAPTER 9

DEVICE DESIGN

With continuous downscaling of CMOS technology nodes, traditional bulk MOSFETs face serious challenges including short-channel effects (SCEs), leakage current, variability, and increased fabrication complexity. One promising alternative to conventional transistor architecture is the Junctionless Double-Gate MOSFET (JLDG-MOSFET). Unlike conventional transistors, junctionless devices do not require source/drain junction formation and use a uniformly doped channel of the same polarity as the source and drain regions. This not only simplifies the fabrication process but also improves control over the channel electrostatics due to the double-gate structure, making the architecture highly suitable for analog and RF applications at nanoscale geometries [83].

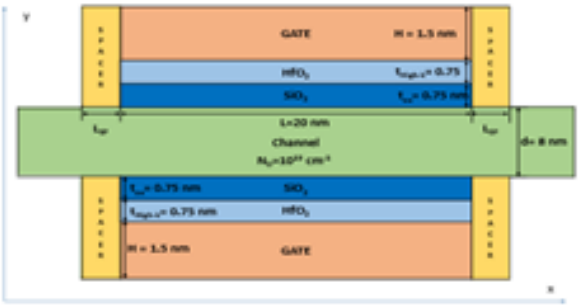


Fig. 9.1 Two-D Exhibit for Gate--Stack Device

The device design discussed in this work is simulated using the Silvaco ATLAS TCAD tool, which allows precise control of process parameters, doping profiles, and physical modeling. Quantum mechanical effects and advanced mobility models are included to achieve an accurate analysis of analog and RF behavior under real operating conditions.

9.1 DEVICE STRUCTURE

The simulated JLDG MOSFET features a double-gate configuration with symmetrical gates on either side of a uniformly doped silicon channel. The gate stack comprises a dual dielectric—high-κ hafnium dioxide (HfO_2) layered over a thin silicon dioxide (SiO_2) interfacial layer. The gates are made of heavily doped n^+ polysilicon to reduce series resistance and support high-frequency operation[84]. The choice of materials ensures better gate capacitance and reduced leakage while allowing for aggressive scaling. The key structural benefits include:

- Enhanced gate electrostatics due to symmetrical double-gate control.
- Elimination of junction formation steps, enabling reduced process complexity.
- Improved scalability and drive current performance at low supply voltages.
- Minimized short-channel effects and improved subthreshold characteristics.

The channel is uniformly n-type doped, which facilitates the junctionless operation by keeping the entire channel in depletion mode under zero gate bias. Current modulation is achieved by electrostatically depleting or accumulating carriers within the channel via the gate voltage, rather than by forming inversion layers as in traditional MOSFETs.

9.2 PHYSICAL DIMENSIONS AND DOPING PROFILE

The dimensions and doping parameters of the simulated device are selected to reflect realistic values in alignment with sub-22 nm technology nodes. These are summarized below:

Table 9.1 Device Parameters

Parameter	**Value**	**Description**
Channel Length (L)	20 nm	Distance between source and drain contacts
Channel Thickness (Tch)	10 nm	Thickness of the uniformly doped silicon film
Gate Oxide Stack	1 nm SiO_2 + 2 nm HfO_2	Dual-layer dielectric for better control and leakage
Gate Material	n^+ polysilicon	High conductivity and compatibility with process flow
Doping Concentration (Channel)	$1\times10^{19}cm^{-31}$	Uniformly applied to source, drain, and channel
Spacer Region	5 nm	Electrically inactive region to isolate the gate
Substrate	Lightly doped silicon bulk	Acts as a mechanical support and isolation

The selection of a thin body helps to ensure full depletion of the channel, which is essential for proper junctionless transistor operation [85].

9.3 SIMULATION ENVIRONMENT AND CONFIGURATION

All simulations were conducted using Silvaco ATLAS, a 2D physics-based Technology Computer-Aided Design (TCAD) simulator. This tool provides accurate solutions to the Poisson and drift-diffusion equations along with optional quantum corrections for modeling nanoscale semiconductor devices.

9.3.1 Physical Models Enabled

To ensure accurate representation of the real-world physics, several important physical models were activated:

- **FERMI**: To include Fermi-Dirac statistics for high doping.
- **BGN (Bandgap Narrowing)**: Accounts for band structure modification due to heavy doping in the source, drain, and channel regions.

- **CVT (Concentration and Field-Dependent Mobility)**: Models reduction in carrier mobility at high fields and concentrations.
- **FLDMOB (Field-Dependent Mobility)**: Refines mobility further by modeling velocity saturation.
- **SRH (Shockley-Read-Hall)**: Handles recombination-generation processes in the channel.
- **QME (Quantum Mechanical Effects)**: Enables the **density-gradient model** to account for quantization of carriers due to confinement in thin channels [85][86].

9.3.2 Mesh Design and Biasing Conditions

A non-uniform mesh was employed to achieve higher resolution in critical regions such as the oxide–semiconductor interface and the channel near the source and drain contacts. The grid density was increased in these regions to capture sharp gradients in carrier concentrations and electric fields.

Biasing Conditions:

- **Gate Voltage (VGS)**: Varied from 0 V to 1.2 V.
- **Drain Voltage (VDS)**: 0.05 V for analog characteristics; swept up to 1.0 V for RF parameters.
- **Source**: Grounded.
- **Substrate**: Grounded for simplicity and symmetry.

9.4 QUANTUM MECHANICAL EFFECTS IN THIN CHANNELS

In ultra-thin body devices such as the one designed here, quantum confinement becomes non-negligible. At channel thicknesses of 10 nm or less, electrons experience spatial confinement perpendicular to the current flow, which leads to discrete energy levels and alters the carrier distribution in the channel.

To account for these effects, the density-gradient quantum correction model was enabled in ATLAS. This model approximates quantum behavior by introducing an additional potential derived from the second derivative of the carrier density. It is particularly useful when solving the Schrödinger equation directly is computationally expensive.

These quantum corrections lead to:

- **Threshold voltage shifts** due to centroid displacement of carriers.
- **Reduced inversion capacitance**, impacting transconductance (g_m).
- **Modified subthreshold behavior**, especially in short-channel devices [84][86].

9.5 MATERIAL AND PROCESS CONSIDERATIONS

The choice of high-κ materials such as HfO_2 is driven by the need to maintain high gate capacitance without incurring leakage current penalties. The use of a thin SiO_2 interfacial layer ensures compatibility with silicon and minimizes interface traps.

The n^+ polysilicon gate is retained for this simulation setup to maintain consistency with existing CMOS flow, although alternative work-function-tunable materials like TiN could also be explored in future work. The uniformly doped silicon layer simplifies process integration by avoiding the need for abrupt junctions, which are difficult to form at nanoscale dimensions.

CHAPTER 10

RESULTS AND DISCUSSION

This chapter presents an extensive evaluation of the analog, radio-frequency (RF), and linearity performance characteristics of the proposed Junctionless Double-Gate Stack MOSFET (JL DG-Gate Stack MOSFET) structure, with quantum mechanical effects (QMEs) included using the Bohr Quantum Potential (BQP) model. All simulations were carried out using the Silvaco ATLAS TCAD tool, which employs advanced numerical iteration methods such as Newton-Raphson and Gummel decoupling to solve the drift-diffusion and Poisson equations self-consistently.

The performance analysis in this section is organized into four main subsections: (A) analog performance, (B) RF performance, (C) linearity metrics, and (D) summary of findings. Key parameters such as transconductance (g_m), output conductance (g_d), intrinsic gain (A_V), cutoff frequency (f_T), and linearity metrics (VIP2, VIP3, IIP3) are thoroughly examined across varying gate lengths of 10 nm, 15 nm, and 20 nm.

10.1 ANALOG-PERFORMANCE PARAMETERS

The analog-performance of the JL DG-Gate Stack-MOSFET has been examined in this section. Here, the most crucial variables, including intrinsic gain (A_V), trans-conductance-generation-factor (TGF), output conductance (g_d), trans-conductance (g_m) and early-voltage (V_{EA}), are simulated and shown. Eqn. 10.1 formulates the transconductance of the MOSFET, which is responsible for determining the amplifier's gain. For analog applications, the enhanced transconductance with increased carrier transport efficiency is preferable for gate stack topologies. Plotting the transconductance change with respect to VGS at VDS = 0.5 V, is exhibited in Figure 10.1. It clearly displays, that as the channel-length is reduced, the transconductance decreases.

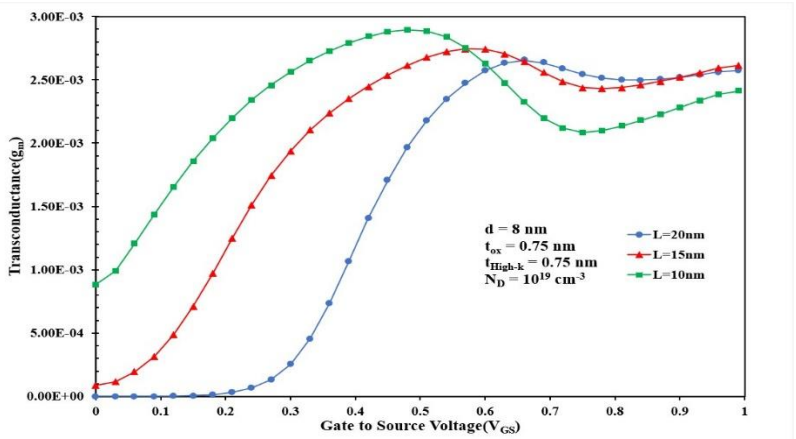


Fig 10.1 g_m V_{GS} for varied channel lengths and V_{DS}=0.5V

As a useful metric for gauging the effectiveness of current translation into transconductance, Figure 10.2 displays the transconductance generation factor (TGF). Input device capability is decreased and power dissipation is increased with a lower TGF. To attain a desired value of transconductance, TGF illustrates how to use current efficiently.

In order to implement analog circuits that run at lower operating voltage, higher value of TGF is useful. This is exhibited in Eqn. 10.2 as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{10.1}$$

$$TGF = \frac{g_m}{I_D} \tag{10.2}$$

Figure 10.2 clearly shows that as channel length decreases, the TGF for the device starts degrading from 85.61253 V^{-1} in 20nm device to 22.6873 V^{-1} in 10nm device. This occurs due to the rise in ID value as L is curtailed, resulting in a low g_m/I_D ratio. A higher-TGF is undesirable for microwave systems with superior linearity, while a lower value of TGF is not a disadvantage, as the power-consumption in the subthreshold region is minimal.

The output conductance, g_d, is determined using Eqn. 10.3.

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \tag{10.3}$$

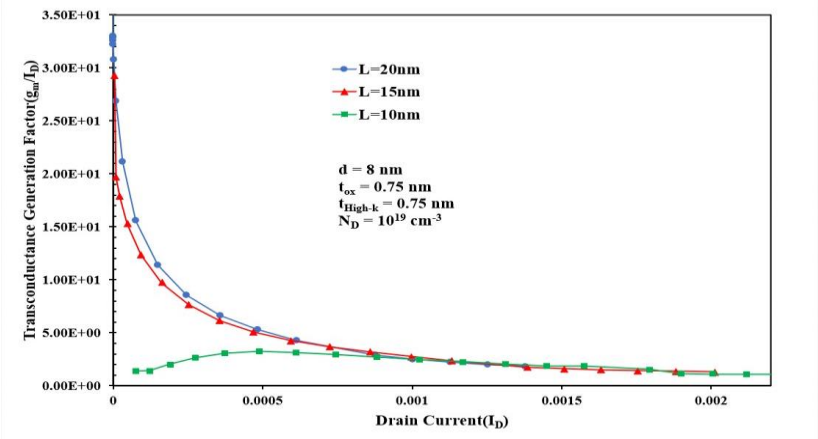


Fig. 10.2 TGF as a function of V_{GS} for varied channel lengths with V_{DS}=0.5V

Achieving a high gain in CMOS circuits (analog), requires transistors with lower gd. A higher g_d signifies low output resistance, which increases the drain-current, as V_{DS} rises in the region of saturation. The increase is influenced by factors such as DIBL and channel length modulation (CLM).

Furthermore, a low g_d leads to a higher ratio of drain-current to output-conductance, which corresponds to the device's early-voltage as shown in Eqn. 10.4.

Figure 10.3 shows how output conductance (g_d) varies for varying channel lengths in relation to gate-to-source voltage (V_{GS}). The standard output requirement must be met with a high output resistance. However, when the gain electric field penetrates more deeply, preventing the current from saturating, Figure 10.3 clearly shows that output-resistance decreases, with the downscaling of gate-length. According to Figure 10.3, the device with channel length 20nm has a low g- value that allows it to have strong control over CLM and DIBL.

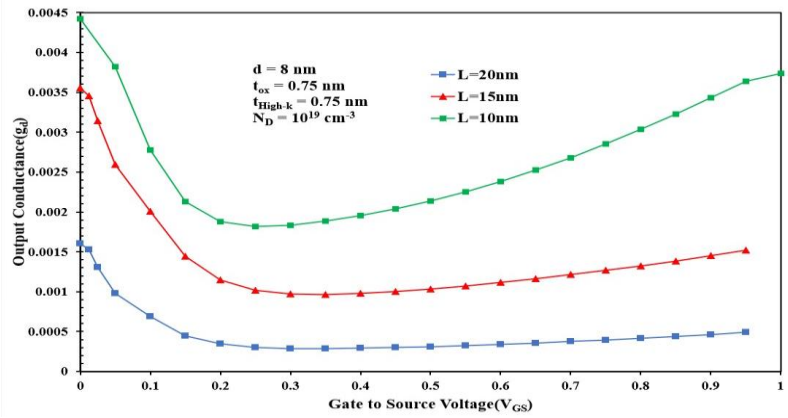


Fig. 10.3 Output Conductance(g_d) versus V_{GS} for varied channel lengths with V_{DS}=0.5V

Because there are competing requirements on a device, power –dissipation and gain are traded off. Although the higher drain-current results in higher gain values, it also causes more power loss. This dissipation of power may cause the device's temperature to rise, thereby impacting its functionality. Since the ratio of g_m to g_d indicates a device's inherent gain, g_m (gate-control) and g_d (drain-control) are crucial small-signal-parameters in analog circuit design. The intrinsic gain and early voltage for a device is given by:

$$V_{EA} = \frac{I_D}{g_d} \tag{10.4}$$

$$A_V = \frac{g_m}{g_d} = \frac{g_m}{I_D} V_{EA} \tag{10.5}$$

Figure 10.4 and 10.5 exhibits the modulation of Intrinsic-Gain and Early-Voltage for device length varying from 20nm down to 10nm. It is shown that as the channel length is downscaled to 10nm, the intrinsic gain of the device reduces. A similar trend can be observed in early voltage. As the channel length decreases, early voltage for the device reduces for operating voltages.

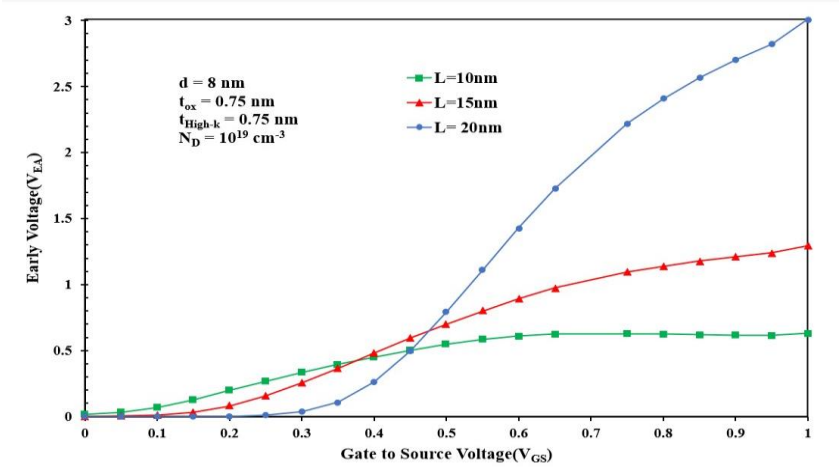


Fig. 10.4 Early-voltage with respect to V_{GS} for varied channel-lengths at V_{DS}=0.5V

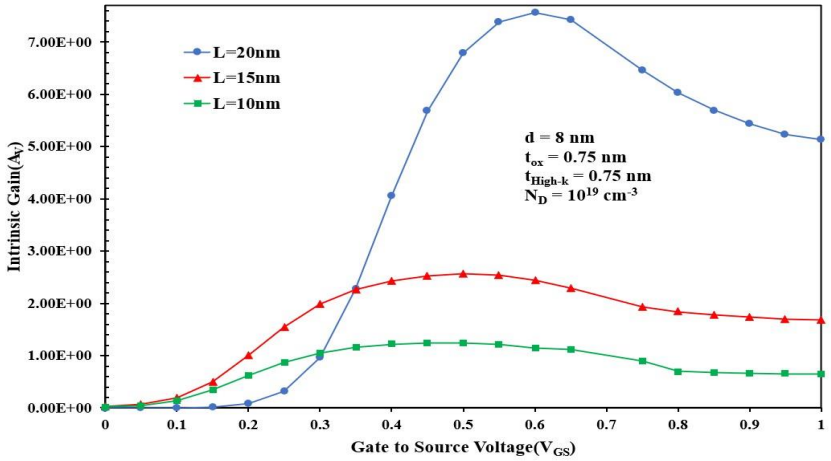


Fig. 10.5 Intrinsic gain (A_V) versus V_{GS} for varied channel length at V_{DS}=0.5V

The parameters for analog performance have been tabulated in Table 10.1 summarising the trend for different channel length for V_{DS}=0.5V and V_{GS}=0.5V.

Table 10.1 Device parameter variation for different channel length at V_{DS}=0.5V & V_{GS}=0.5V

Table 10.1 Device parameter variation for different channel length at V_{DS}=0.5V & V_{GS}=0.5V

Device Parameters	Channel Length		
	L=20nm	L=15nm	L=10nm
Transconductance(S)	0.00288594	0.00267668	0.00217819
Output Conductance(S)	0.000309459	0.00103454	0.00214021
Early Voltage(V)	0.792679179	0.699889615	0.546303473
Gain(dB)	67.86327106	25.64057455	20.39420431
TGF(V^{-1})	85.6125314	36.63516933	22.68739795

10.2 RADIO-FREQUENCY-PERFORMANCE PARAMETERS

This section examines the RF-performance using common figures of merit, including the following: (a) f_T (cut-off frequency); (b) GBW; (c)S parameters as well as several others.

It is evident that the parasitic-resistances and the Miller-capacitance ratio C_{GD}/C_{GS}, have a significant impact on RF performances. The plot of C_{GD} & C_{GS} against V_{GS} for varied gate-lengths is exhibited in Figure 10.6 and 10.7 respectively. Figure 10.6 and 10.7 shows that when channel length reduces, C_{GD}/C_{GS} falls as well. When comparing multiple gate devices to single gate devices, it was shown that the C_{GD}/C_{GS} ratio rises [11]. A decrease in SCEs is indicated by an improvement in this ratio, and when L decreases, this results in a decrease in Miller capacitance. Consequently, an enhanced frequency of operation results from the decrease in Miller capacitances compensating for the rise in parasitic capacitances. It has been noted that as V_{GS} rises to saturation, both C_{GS} and C_{GD} begin to rise. As anticipated, after saturation, both values stabilize since the connection is unaffected by the extra V_{DS}.

The cut-off frequency may be defined as the lowest-frequency, at which the current-gain becomes unity.

$$f_T = \frac{g_m}{2\pi C_{GS}\sqrt{1+2\frac{C_{GD}}{C_{GS}}}} \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})} \tag{10.6}$$

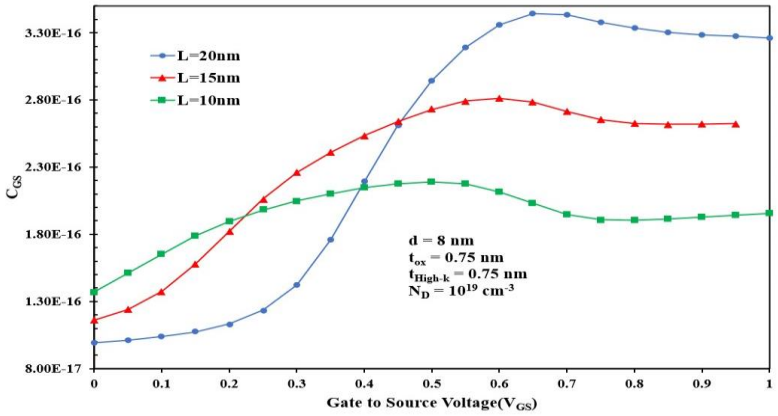


Fig. 10.6 C_{GS} versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

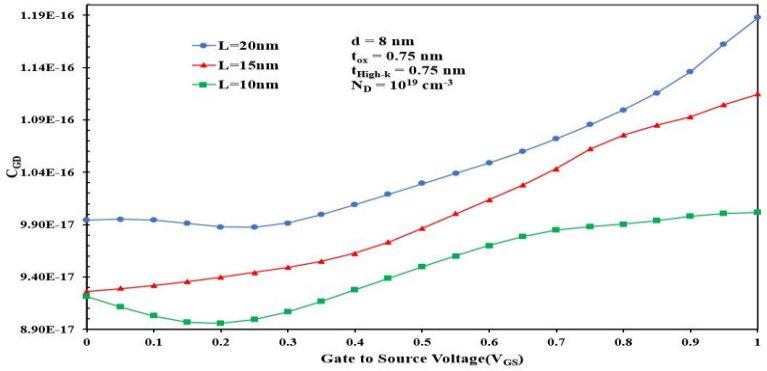


Fig. 10.7 C_{GD} versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

Variation in f_T with regard to I_D is depicted in Figure 10.8. Given that g_m is directly proportional to 1/L and C_{GD}/C_{GS} is proportional to L, f_T is exhibiting a $1/L^2$ dependence. f_T achieves a maximum value at a certain gate bias after reaching a lower value at the subthreshold region and rising with I_D. The transconductance is at its highest & the gate-to-source/drain-capacitance is at its lowest at the f_T peak. A trade-off between power-efficiency and bandwidth is demonstrated by the fact that f_T decreases as the channel length (L) increases. However, a higher f_T can be attained by increasing the interface-charge-trap-density.

One way to analyse a device's AC analysis is to think of it as a 2-port network. The scattering-parameters, S_{11} and S_{22}, which represents the reflection-coefficients, at ports 1 and 2, respectively, are the device metrics used to match the terminal and port impedances. In order to achieve optimal matching at the ends and minimal reflection, the values for these reflection coefficients should be as low as possible, preferably zero. The variation in reflection coefficients with regard to frequency is seen in Figure 10.9 and 10.10. The statistics clearly show that the DG-JL-

MOSFET with channel length 10nm has the lowest reflection coefficient values, which also drop as the frequency rises.

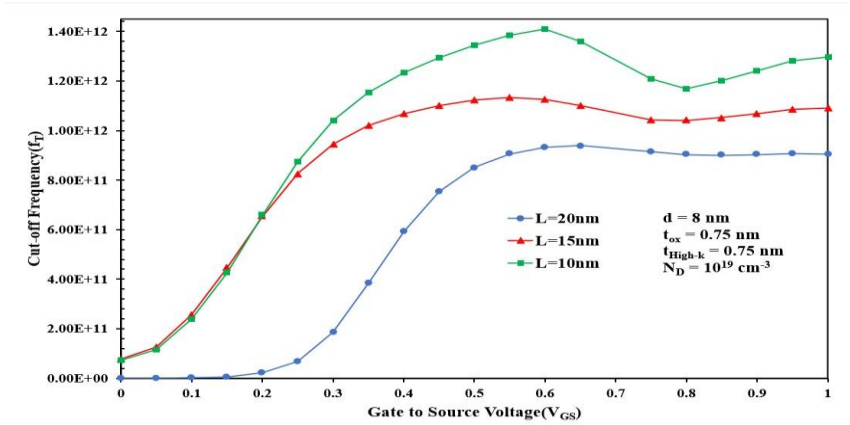


Fig. 10.8 f_T with respect to V_{GS} for varied channel-lengths at V_{DS}=0.5V

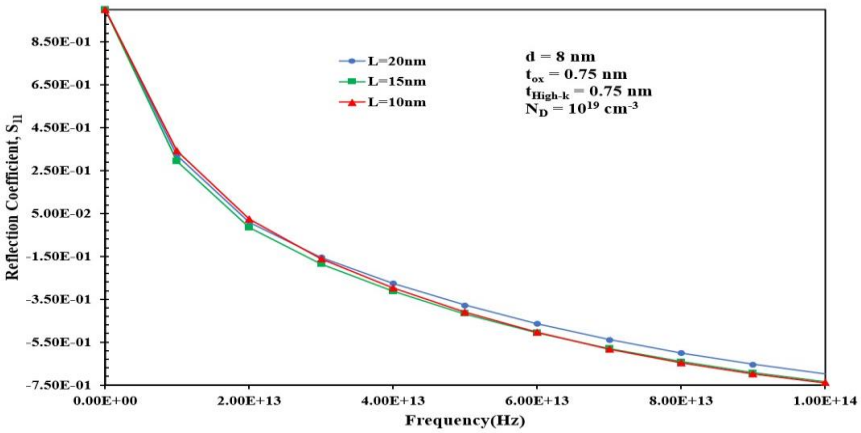


Fig. 10.9 Reflection coefficient (S_{11}) with respect to V_{GS} for varied channel-lengths at V_{DS}=0.5V

This, results from improved channel gate control, which enhances the band-to-band-carrier-generation-rate & g_m and I_D, lowers reflection, and ultimately improves port matching.

The stability of a device at higher frequencies is significantly influenced by the reverse transmission coefficient, or S_{12}, also known as the reverse voltage gain. Its magnitude should thus be greater in order to provide better stability and voltage gain.

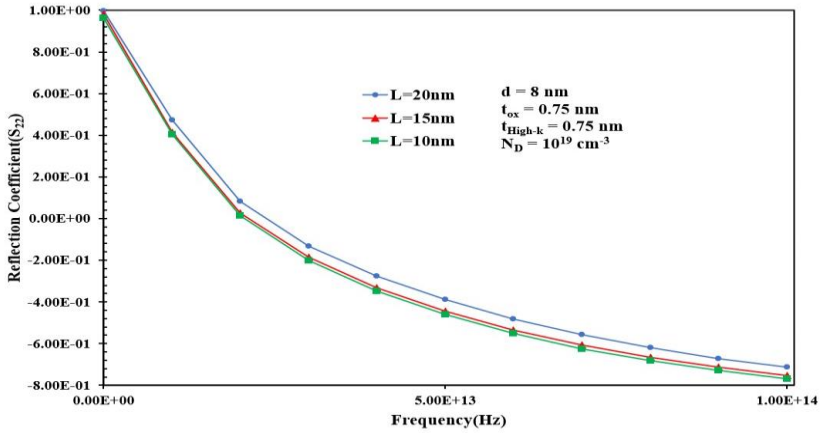


Fig. 10.10 Reflection coefficient (S_{22}) with respect to V_{GS} for varied channel-lengths at V_{DS}=0.5V

The transmission coefficient was shown in Figure 10.11, and it is evident that, in comparison to the other device designs and as the frequency increases, the DG-JL-Gate-Stack MOSFET displays the largest magnitude of S_{12} which slowly then decreases. Also as the channel-length is reduced, the S_{12} decrements. This is as a result of the device's enhanced performance, which reduces SCEs.

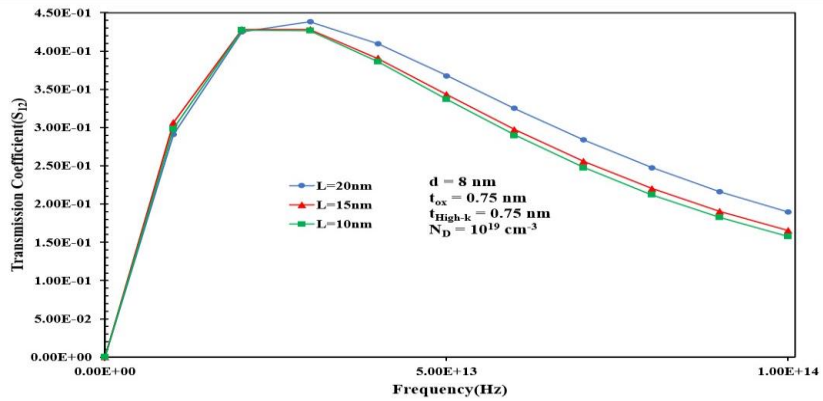


Fig. 10.11 Transmission coefficient (S_{12}) with respect V_{GS} for varied channel-lengths at V_{DS}=0.5V

Since the forward voltage gain, also known as the transmission coefficient, S_{21}, determines the device's gain, its magnitude should be as high as achievable. As seen in Figure 10.12, the device with channel length as 20nm has the highest magnitude of S_{21} when compared to other channel length and when the frequency is increased.

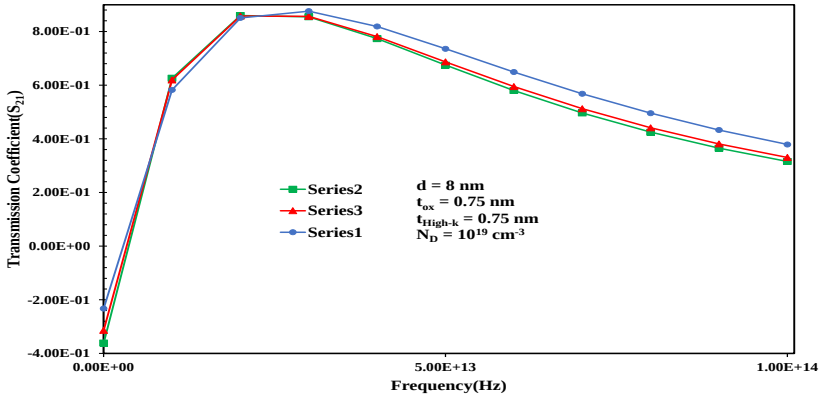


Fig. 10.12 Transmission coefficient (S_{21}) with respect to V_{GS} for varied channel-lengths at V_{DS}=0.5V

Figure 10.13 illustrate the current gain versus V_{GS} for various channel-lengths. It is thus evident, that, as the channel-length is decreased, the current gain for the device increases. This is because as the channel length is curtailed, the electric field has superior channel control, owing to higher electron velocity, which in turn leads to increased current gain, as evidently seen in the figure.

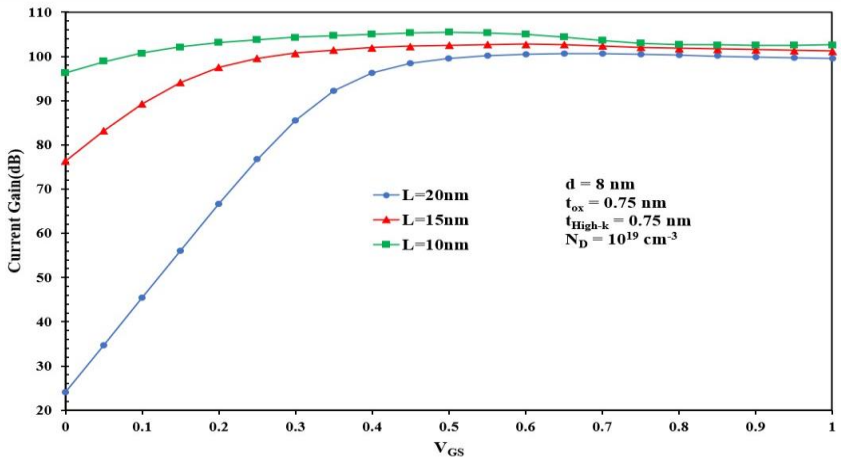


Fig. 10.13 Current gain(dB) versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

10.3 LINEARITY PERFORMANCE PARAMETERS

Trans-conductance & output-conductance are the two main reasons for nonlinearity in a MOSFET. When frequency is taken into consideration, the transconductance linearity is the main emphasis of this research because, to its whip-hand feature in modern RF systems & circuits. The second derivative of the

transconductance is inversely-proportional to linearity, which is directly-proportional to transconductance. The following provides g_{m1}, g_{m2}, and g_{m3} in the linearity analysis for a JL DGMOS:

$$g_{m1} = \frac{\partial I_{DS}}{\partial V_{GS}}, g_{m2} = \frac{\partial^2 I_{DS}}{\partial V_{GS}^2}, g_{m3} = \frac{\partial^3 I_{DS}}{\partial V_{GS}^3} \tag{10.7}$$

The extrapolated gate-voltage-amplitudes at which, the 2nd & 3rd order-harmonics, align with the fundamental-tone of the device's I_D, are represented by VIP_2 and VIP_3, respectively. To achieve higher linearity and lower distortion, these figure-of-merits (FOMs) should be optimized to the highest possible values. They are the proper ones that determine the distortion characteristics from DC parameters.

$$VIP_2 = [4*(\frac{g_{m1}}{g_{m2}})]_{V_{DS}=constant} \tag{10.8}$$

$$VIP_3 = [\sqrt{24*(\frac{g_{m1}}{g_{m2}})}]_{V_{DS}=constant} \tag{10.9}$$

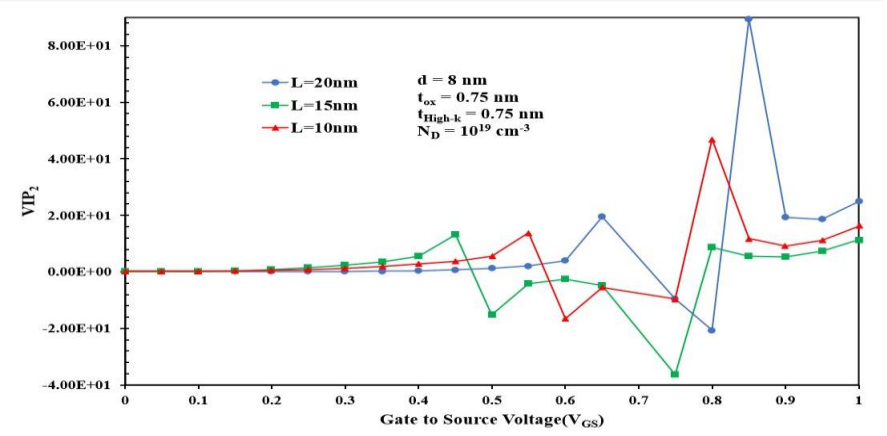


Fig. 10.14 VIP_2 versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

Figure 10.14 & 10.15 exhibits the modulation in VIP_2 and VIP_3 respectively with respect to V_{GS} for varied channel-lengths. It can be seen that the highest value of VIP_2 is obtained for channel length 20nm and starts degrading as the

channel length starts reducing. This is due to reduced harmonic distortion, which improves carrier transport efficiency, gate leakages, and ultimately device gain.

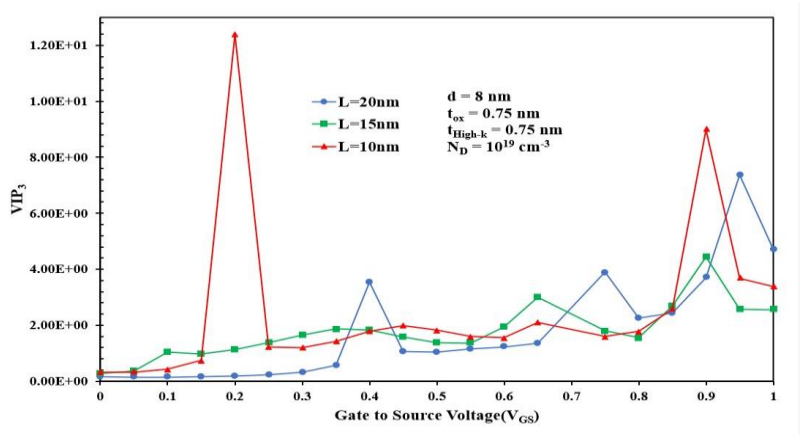


Fig. 10.15 VIP_3 versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

The VIP_3 peak is a manifestation of the 2nd order-interaction effect & the suppression of the 3rd order non-linearity by device internal-feedback within the device, which operates around a second-order nonlinearity. As seen in Figure 10.15, this peak is more linear than its dominant counterparts, since it is the strongest in the 10-nm channel-length range.

As stated in Eqn. 10.10, IIP3 depicts the extrapolated input-power at which, the powers of the fundamental & 3rd order-harmonics are equivalent.

$$IIP_3 = \frac{2 * g_{m1}}{3 * g_{m3} * R_S} = \frac{2 * (\frac{\partial I_D}{\partial V_{GS}})}{3 * R_S * (\frac{\partial^3 I_D}{\partial V^3_{GS}})} \tag{10.10}$$

Where, R_S = 50 Ω for RF and analog applications.

Figure 10.16 illustrates the modulation in IIP_3 with respect to gate-to-source voltage for varied channel lengths. IIP_3 decreases significantly at 10 nm channel length compared to 15 or 20 nm channel length.

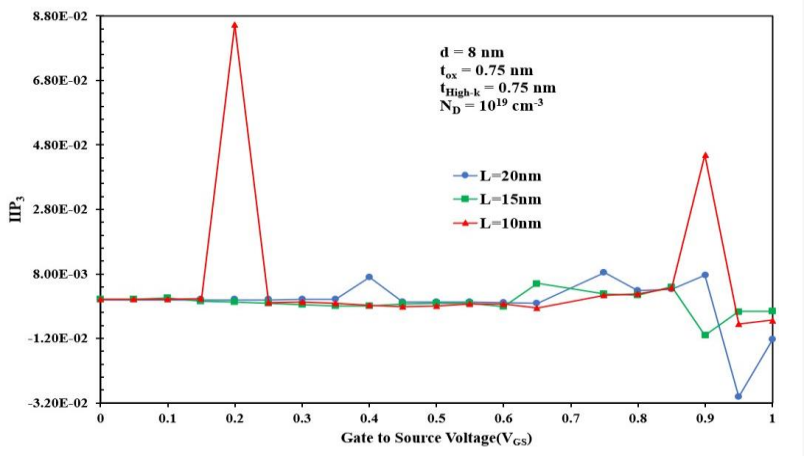


Fig. 10.16 IIP_3 versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

The GTFP, which is expressed in Eqn. 10.11 and displayed in Figure 10.17 by both the intrinsic-gain & the switching-speed, is a distinctive figure of merit for analog/RF performances.

$$GTFP = \left(\frac{g_m}{g_d}\right)\left(\frac{g_m}{I_D}\right) f_T = A_V * TFP \tag{10.11}$$

It's noteworthy that the switch from mild to strong inversion coincides with the GTFP peak value occurring at a remarkably low gate-to-source voltage level. As a result, we obtain useful data that circuit designers may use to determine the ideal area that attains the optimum overall trade-off between speed, gain, and conductance.

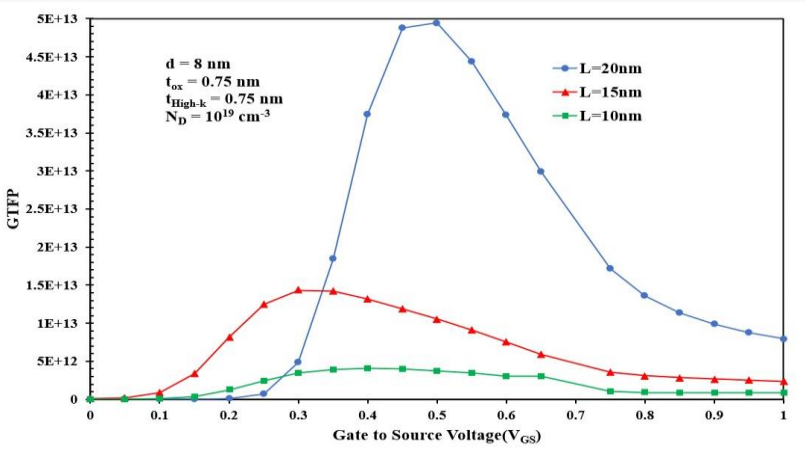


Fig. 10.17 GTFP versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

In moderate to high-speed devices, the product of g_m/I_D & f_T, or TFP, as determined by Eqn. 10.12 indicates a trade-off between power & bandwidth.

$$TFP = (\frac{g_m}{I_D}) * f_T \tag{10.12}$$

$$GFP = (\frac{g_m}{g_d}) * f_T \tag{10.13}$$

Similarly, a crucial characteristic for operational-amplifiers in high-frequency applications is the gain frequency product, or GFP, as stated in Eqn. 10.13. Figure 10.19 plots the GFP versus V_{GS} at V_{DS}=0.5V, whereas Figure 10.18 plots the TFP against V_{GS} at V_{DS}= 0.5V. According to the Figure, GFP and TFP begin to rise linearly as V_{GS} rises in the zone of subthreshold, reach an optimal value, and then begin to fall in the saturation zone.

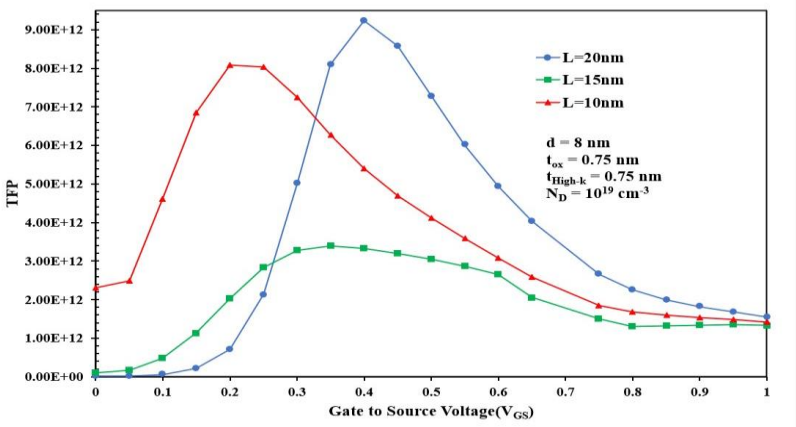


Fig. 10.18 TFP versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

The power-level that causes the gain to decrease by 1-dB, from its small-signal value, is represented as the 1-dB compression-point. For an amplifier circuit, this value is important since it gives a general idea of the highest input-power, that the circuit can sustain while maintaining a given level of gain.

$$1-dBcompressionpoint = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \tag{10.14}$$

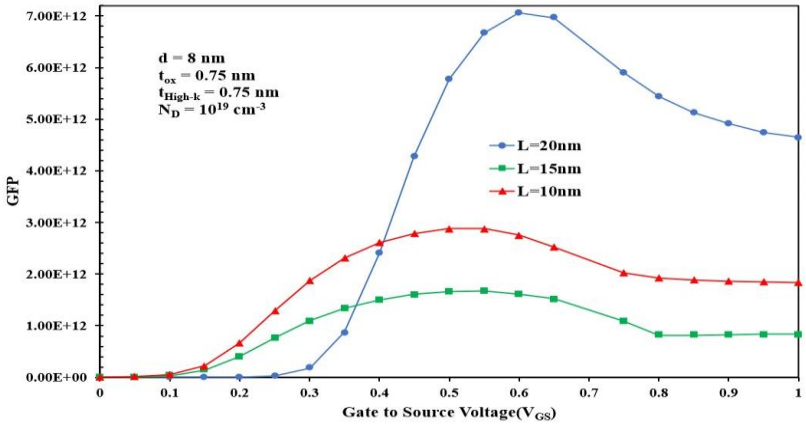


Fig. 10.19 GFP versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

Figure 10.20 makes it abundantly evident that, owing to superior gate-control & therefore stronger trans-conductance, JL DG- Gate Stack MOSFET devices with channel-lengths (15 & 20 nm) have a lower 1-dB compression point than devices with channel-lengths of 10 nm.

The JL DG- Gate Stack MOSFET device's shorter channel length characteristic makes it a favourable and advantageous candidate for high-linearity, ultra-wide-band (UWB), low-noise-amplifier (LNA) design & RF applications. The 1-dB compression-point should be increased to ensure lower distortion-operation.

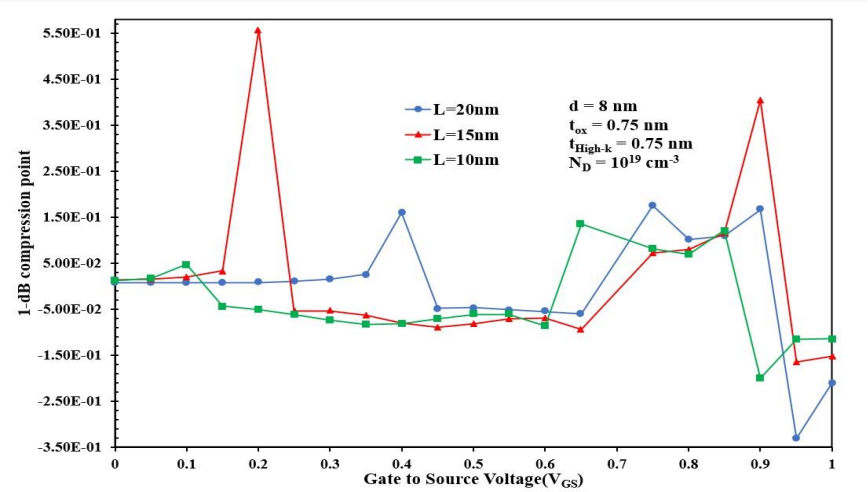


Fig. 10.20 1-dB compression point versus V_{GS} for varied channel-lengths at V_{DS}=0.5V

CHAPTER 11

CONCLUSION, FUTURE SCOPE, AND SOCIAL IMPACT

In this thesis, a comprehensive study of the Junctionless Double-Gate Stack MOSFET (JL DG-Stack MOSFET) has been carried out with an emphasis on analog and RF performance under the influence of quantum mechanical effects (QMEs). The device structure, modeled in Silvaco ATLAS, utilizes a high-κ dielectric stack over a uniformly doped silicon channel, eliminating the need for junction formation. The double-gate configuration further enhances electrostatic control and channel modulation.

The quantum effects were incorporated using the Bohr Quantum Potential (BQP) model, which successfully captured confinement phenomena in ultra-thin channels. The drift-diffusion simulations, augmented with QME corrections and advanced mobility models, allowed the extraction of vital device parameters like gm, gd, fT, AV, VIP2, VIP3, and IIP3 across gate lengths of 10 nm, 15 nm, and 20 nm.

The key conclusions drawn from this study are summarized below:

- Transconductance (gm) is highest for longer gate lengths, with degradation observed at sub-15 nm due to velocity saturation and short-channel effects.

- Intrinsic gain (AV) and Early voltage (VEA) drop with scaling, indicating that analog performance is sensitive to electrostatic degradation at nanoscale.

- RF metrics such as cut-off frequency (fT) and gain-bandwidth product (GBW) improve significantly with downscaling due to shorter carrier transit time and reduced gate capacitance.

- Linearity metrics such as VIP3 and IIP3 show optimum values at longer gate lengths (20 nm), suggesting better linear response for high-frequency analog applications.

Thus, the junctionless DG stack configuration demonstrates a well-balanced profile between scaling feasibility, fabrication simplicity, and analog/RF performance, making it a strong candidate for future nanoscale RF-CMOS and mixed-signal technologies.

11.1 FUTURE SCOPE

While this work has explored various performance dimensions of the proposed JL DG-Stack MOSFET, several avenues remain for further investigation:

- Inclusion of variability analysis: Process variations such as random dopant fluctuation (RDF), oxide thickness variation, and work function instability could be analyzed to assess the robustness of the design.

- 3D TCAD simulations: Extension to 3D geometry would allow more accurate modeling of parasitics, especially fringing fields and layout-dependent effects in realistic IC environments.

- Thermal performance studies: At nanoscale, self-heating and thermal noise could impact analog and RF figures of merit and deserve in-depth analysis.

- Alternate gate materials: Exploring metal gates with tunable work functions could enhance threshold control and reduce gate resistance.

- Integration into circuit-level design: Simulating the device in RF amplifier topologies (e.g., LNA or mixer circuits) can validate its practical viability.

Furthermore, incorporation of non-conventional channel materials such as III-V semiconductors, 2D materials (e.g., MoS_2), or strain engineering could further push the device's capabilities beyond current CMOS limits.

11.2 SOCIAL IMPACT

The continued scaling of CMOS technology is central to next-generation electronics, from high-speed communication systems to ultra-low-power IoT devices. The junctionless double-gate MOSFET proposed and analyzed in this work aligns with the industry's goal of simplifying fabrication while maintaining high-performance operation at reduced power supply voltages.

Some of the anticipated societal impacts of this work include:

- Energy-efficient electronics: By enabling low-power analog and RF operation, the device contributes to greener and more sustainable semiconductor technologies.

- Accessible communication infrastructure: The potential for high-frequency performance supports development in 5G/6G and wireless sensor networks, extending digital connectivity to underserved regions.

- Educational and research advancement: The modeling framework and simulation methodology serve as a foundation for future academic projects and device innovation.

By proposing a realistic, scalable, and performance-oriented transistor architecture, this work offers a meaningful step toward next-generation CMOS technologies with broad industrial and societal relevance.

REFERENCES

[1] J.-P. Colinge, J. C. Alderman, W. Xiong, C. R. Cleavelin, et al., "Quantum–mechanical effects in trigate SOI MOSFETs," IEEE Transactions on Electron Devices, vol. 53, no. 5, pp. 1131–1136, May 2006.

[2] J. Charles Pravin, D. Nirmal, P. Prajoon, and M. M. Anuja, "A new drain current model for a dual metal Junctionless transistor for enhanced digital circuit performance," IEEE Transactions on Electron Devices, vol. 63, pp. 3782–3789, 2016.

[3] Y. Wang, C. Shan, Z. Dou, L. G. Wang, and F. Cao, "Improved performance of nanoscale junctionless transistor based on gate engineering approach," Microelectronics Reliability, vol. 55, pp. 318–325, 2015.

[4] B. R. Raad, D. Sharma, P. Kondekar, K. Nigam, and D. S. Yadav, "Drain work function engineered doping-less charge plasma TFET for Ambipolar suppression and RF performance improvement," IEEE Transactions on Electron Devices, vol. 63, pp. 3950–3957, 2016.

[5] S. Bari, D. De, and A. Sarkar, "Effect of gate engineering in JLSRG MOSFET to suppress SCEs: an analytical study," Physica E: Low-dimensional Systems and Nanostructures, vol. 67, pp. 143–151, 2015.

[6] K. C. D. Sarma and S. Sharma, "An approach for complete 2-D analytical potential modelling of fully depleted symmetric double gate junctionless transistor," Journal of Computational Electronics, vol. 14, pp. 717–725, 2015.

[7] J. H. Woo, J. M. Choi, and Y. K. Choi, "Analytical threshold voltage model of junctionless double-gate MOSFETs with localized charges," IEEE Transactions on Electron Devices, vol. 60, pp. 2951–2955, 2013.

[8] T. Chaudhary and G. Khanna, "A 2D potential based threshold voltage model analysis and comparison of Junctionless symmetric double gate vertical slit field effect transistor," IETE Journal of Research, vol. 0, pp. 1–10, 2017.

[9] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-κ/metal-gate stack and its MOSFET characteristics," IEEE Electron Device Letters, 2004.

[10] J. Ajayan, D. Nirmal, P. Prajoon, and P. J. Charles, "Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-K dielectrics for high speed applications," AEU - International Journal of Electronics and Communications, vol. 79, pp. 151–157, 2017.

[11] A. Sharma, A. Jain, Y. Pratap, and R. S. Gupta, "Effect of high-k and vacuum dielectrics as gate stack on a junctionless cylindrical surrounding gate (JL-CSG) MOSFET," Solid-State Electronics, vol. 123, pp. 26–32, 2016.

[12] J.-P. Colinge, "Multigate SOI MOSFETs," Microelectronics Journal, vol. 36, no. 7, pp. 695–700, 2005.

[13] R. Chau, et al., "Advanced silicon gate stack, source/drain, and channel engineering for high-performance CMOS," in IEDM Technical Digest, 2003.

[14] W. Kim, et al., "High-k dielectric materials and MOSFETs for future scaling," IEEE Transactions on Electron Devices, vol. 55, no. 1, pp. 90–96, 2008.

[15] S. K. Pati, K. Koley, A. Dutta, et al., "Study of body and oxide thickness variation on analog and RF performance of underlap DG-MOSFETs," Microelectronics Reliability, vol. 54, pp. 1137–1142, 2014.

[16] S. K. Swain, A. Dutta, S. Adak, et al., "Influence of channel length and high-K oxide thickness on subthreshold analog/RF performance of graded channel and gate stack DG-MOSFETs," Microelectronics Reliability, vol. 61, pp. 24–29, 2016.

[17] S. Adak, A. Sarkar, S. Swain, et al., "High performance AlInN/AlN/GaN p-GaN back barrier gate-recessed enhancement mode HEMT," Superlattices and Microstructures, vol. 75, pp. 347–357, 2014.

[18] S. Cho, K. R. Kim, B. G. Park, et al., "RF performance and small signal parameter extraction of junctionless silicon nanowire MOSFETs," IEEE Transactions on Electron Devices, vol. 58, pp. 1388–1396, 2011.

[19] R. T. Doria, M. A. Pavanello, R. D. Trevisoli, et al., "Junctionless multiple-gate transistors for analog applications," IEEE Transactions on Electron Devices, vol. 58, pp. 2511–2519, 2011.

[20] B. Razavi, RF Microelectronics, 2nd ed., Prentice Hall, 2011.

[21] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed., Pearson, 2003.

[22] B. Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice Hall, 1998.

[23] J.-P. Colinge, "Fully-depleted SOI CMOS for analog application," IEEE Transactions on Electron Devices, vol. 45, no. 5, pp. 1010–1016, 1998.

[24] B. Razavi, "CMOS technology characterization for analog and RF design," IEEE Journal of Solid-State Circuits, vol. 34, no. 3, pp. 268–276, 1999.

[25] V. Kilchytska, A. Nève, L. Vancaillie, D. Levacq, S. Adriaensen, H. V. Meer, K. De Meyer, C. Raynaud, M. Dehan, J.-P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," IEEE Transactions on Electron Devices, vol. 50, no. 3, pp. 577–588, 2003.

[26] N. Mohankumar, B. Syamal, and C. K. Sarkar, "Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs," IEEE Transactions on Electron Devices, vol. 57, no. 4, pp. 820–826, 2010.

[27] A. Sarkar, A. K. Das, S. De, and C. K. Sarkar, "Effect of gate engineering in double gate MOSFETs for analog/RF applications," Microelectronics Journal, vol. 43, no. 11, pp. 873–882, 2012.

[28] G. M. Rebeiz, RF MEMS: Theory, Design, and Technology, Wiley, 2003.

[29] M. A. Pavanello and J.-P. Colinge, "Analog design with double-gate and FinFET devices," IEEE Circuits and Devices Magazine, vol. 21, no. 5, pp. 29–36, 2005.

[30] K. H. Yeo, et al., "Low noise and high linearity CMOS RF circuits," IEEE Journal of Solid-State Circuits, vol. 38, no. 3, pp. 316–324, 2003.

[31] J.-P. Colinge, "The junctionless transistor," Nature Nanotechnology, vol. 5, pp. 225–229, 2010.

[32] R. Huang, et al., "Carrier transport modeling and performance of nanoscale junctionless DG MOSFETs," IEEE Transactions on Electron Devices, vol. 57, no. 1, pp. 107–115, 2010.

[33] A. Rahman and M. S. Lundstrom, "A compact scattering model for nano-scale double-gate MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 3, pp. 481–489, 2002.

[34] SILVACO Inc., Atlas User's Manual: Device Simulation Software, 2023.

[35] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed., Wiley-Interscience, 2006.

[36] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed., Cambridge University Press, 2009.

[37] D. J. Frank, et al., "Device scaling limits of Si MOSFETs and their application dependencies," Proceedings of the IEEE, vol. 89, no. 3, pp. 259–288, 2001.

[38] J. P. Colinge, et al., "Nanowire transistors without junctions," Nature Nanotechnology, vol. 5, pp. 225–229, 2010.

[39] J. P. Colinge, et al., "Junctionless nanowire transistors," IEEE Electron Device Letters, vol. 31, no. 5, pp. 430–432, 2010.

[40] A. K. Sharma, et al., "Performance analysis of junctionless double-gate MOSFETs," Microelectronics Journal, vol. 42, no. 7, pp. 1004–1010, 2011.

[41] S. Roy, et al., "Dual-material gate junctionless MOSFET: A novel device for analog/RF applications," IEEE Transactions on Electron Devices, vol. 60, no. 10, pp. 3215–3220, 2013.

[42] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, no. 10, pp. 5243–5275, 2001.

[43] M. Houssa, et al., "High-κ gate dielectrics: Current status and new materials," Materials Science and Engineering: R: Reports, vol. 51, no. 4–6, pp. 37–85, 2006.

[44] J. Robertson, "High dielectric constant oxides," Eur. Phys. J. Appl. Phys., vol. 28, no. 3, pp. 265–291, 2004.

[45] B. Baral, et al., "Effect of gate length downscaling on RF/analog performance of junctionless double-gate MOSFET," Adv. Ind. Eng. Manag., vol. 5, no. 1, pp. 130–137, 2016.

[46] K. E. Kaharudin, et al., "Effect of channel length variation on analog and RF performance of junctionless double-gate vertical MOSFET," J. Eng. Sci. Technol., vol. 14, no. 4, pp. 2181–2194, 2019.

[47] R. Saha, et al., "Impact of work function on analog/RF and linearity parameters in step-FinFET," Indian J. Phys., vol. 95, pp. 2387–2392, 2021.

[48] S. Misra, et al., "Study of DC and analog/RF performances analysis of short channel surrounded gate junctionless graded channel gate stack MOSFET," Trans. Electr. Electron. Mater., vol. 24, pp. 178–187, 2023.

[49] M. Shalchian, et al., "Charge-based model for ultrathin junctionless DG FETs, including quantum confinement," arXiv preprint, arXiv:1808.06685, 2018.

[50] N. W. Ashcroft and N. D. Mermin, Solid State Physics, Brooks/Cole, 1976.

[51] D. K. Ferry and S. M. Goodnick, Transport in Nanostructures, Cambridge University Press, 1997.

[52] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed., Cambridge University Press, 2013.

[53] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed., Wiley-Interscience, 2006.

[54] M. Lundstrom, Fundamentals of Carrier Transport, Cambridge University Press, 2000.

[55] I. Ferain, C. A. Colinge, and J. P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," Nature, vol. 479, no. 7373, pp. 310–316, 2011.

[56] J. Xiang-Wei and L. Shu-Shen, "Quantum confinement effects and source-to-drain tunneling in ultra-scaled double-gate silicon n-MOSFETs," Chin. Phys. B, vol. 21, no. 2, p. 027304, 2012.

[57] A. Svizhenko, M. P. Anantram, T. R. Govindan, B. Biegel, and R. Venugopal, "Two Dimensional Quantum Mechanical Modeling of Nanotransistors," arXiv preprint, arXiv:cond-mat/0111290, 2001.

[58] B. A. Biegel, M. G. Ancona, C. S. Rafferty, and Z. Yu, "Efficient Multi-Dimensional Simulation of Quantum Confinement Effects in Advanced MOS Devices," NASA Tech. Rep., 2000.

[59] J. Xu, "The impact of quantum confinement on the electrical characteristics of ultrathin-channel GeOI MOSFETs," J. Semicond., vol. 35, no. 4, p. 044004, 2014.

[60] N. W. Ashcroft and N. D. Mermin, Solid State Physics, Holt, Rinehart and Winston, 1976.

[61] C. Kittel, Introduction to Solid State Physics, 8th ed., Wiley, 2005.

[62] P. Y. Yu and M. Cardona, Fundamentals of Semiconductors: Physics and Materials Properties, 4th ed., Springer, 2010.

[63] J. Singh, Semiconductor Devices: Basic Principles, Wiley, 1993.

[64] C. Kittel, Introduction to Solid State Physics, 8th ed., Wiley, 2005.

[65] D. J. Griffiths, Introduction to Quantum Mechanics, 3rd ed., Cambridge University Press, 2018.

[66] R. Eisberg and R. Resnick, Quantum Physics of Atoms, Molecules, Solids, Nuclei, and Particles, 2nd ed., Wiley, 1985.

[64] C. Kittel, Introduction to Solid State Physics, 8th ed., Wiley, 2005.

[65] D. J. Griffiths, Introduction to Quantum Mechanics, 3rd ed., Cambridge University Press, 2018.

[66] R. Eisberg and R. Resnick, Quantum Physics of Atoms, Molecules, Solids, Nuclei, and Particles, 2nd ed., Wiley, 1985.

[67] N. W. Ashcroft and N. D. Mermin, Solid State Physics, Holt, Rinehart and Winston, 1976.

[68] TU Delft, "Tight-binding model," Open Solid State Notes, https://ocw.tudelft.nl

[69] Rutgers University, "The Tight Binding Method," https://www.physics.rutgers.edu

[70] Wikipedia, "Effective mass (solid-state physics)," https://en.wikipedia.org/wiki/Effective_mass_(solid-state_physics)

[71] University College London, "Solid State Physics – Lecture Notes," https://www.ucl.ac.uk/phys

[72] Materials Science & Engineering, "Miller Indices," https://www.materials.manchester.ac.uk

[73] Wikipedia, "Miller Index," https://en.wikipedia.org/wiki/Miller_index

[74] Portland State University, "Lecture 3: Density of States & Intrinsic Fermi Level," https://web.cecs.pdx.edu/~gerry

[75] University at Albany, “Semiconductor Statistics,” https://www.albany.edu

[76] National Dong Hwa University, Taiwan, “Density of States in Semiconductors,”, https://phys.ndhu.edu.tw

[77] TU Wien, “4.1 Semiconductor Equations,” https://www.iue.tuwien.ac.at

[78] Academic Library, “Basic Semiconductor Equations,” https://www.academiclibrary.com

[79] University of California, San Diego, “Lecture on Poisson–Boltzmann Equation,” https://courses.ucsd.edu

[80] Springer, “Modeling of Threshold Voltage and Subthreshold Current of JL-DG MOSFETs,” , https://link.springer.com

[81] A. Author(s), “Fast Estimation of Threshold Voltage in JL-DG MOSFETs,” arXiv preprint, , https://arxiv.org

[82] A. Author(s), “Analysis of DC Parameters in JL-DG MOSFETs with QME,” ResearchGate, https://www.researchgate.net

[83] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed., Cambridge University Press, 2013.

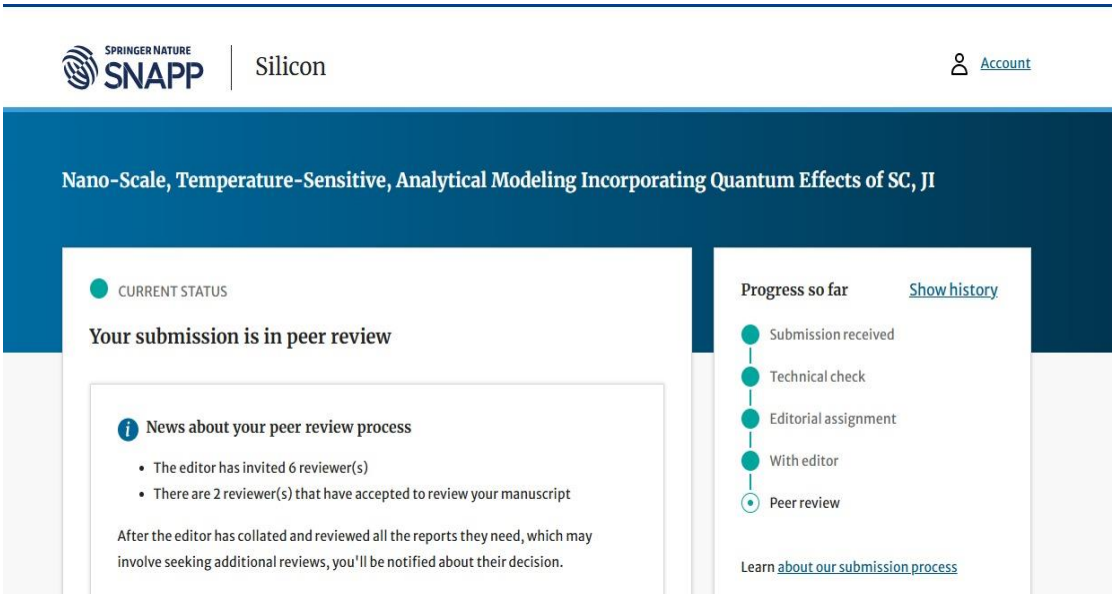
[84] Prajvi Udar, Anubha Goel and R. S. Gupta (2023), “Quantum Effect dependent modelling of Short Channel Junctionless Double Gate Stack (SC-JL-DG) MOSFET for Analog Applications” *Microelectronics Journal (Elsevier)*, vol. 134, pp. 105726.

[85] Prajvi Udar, Anubha Goel and R. S. Gupta (2024), “Nanoscale Temperature Dependent Quantum-Effect Analytical model of Short- Channel, Junction-Less, Double-Gate Stack (SC-JL-DG) MOSFET for Analog Applications at Higher Frequencies” *Microelectronics Journal (Elsevier)*, vol. 134, pp. 105726.

[86] Silvaco International, ATLAS User’s Manual, Version 5.22.3.R, Silvaco Inc., 2022.

LIST OF PUBLICATIONS

[1] P. Udar, D. Sipal, A. Goel, and S. Rewari “Nano-Scale, Temperature-Sensitive, Analytical Modeling Incorporating Quantum Effects of SC, JL, DG Stack (SC-JL-DG) MOSFET for Analog-Industry Applications at Leading Frequencies" Submitted Under review in Springer Nature(Silicon) Journal- 2025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PRAJVI UDAR

MTech in VLSI and Embedded Systems
Delhi Technological University, Delhi

+91-8800667880
prajviudar@gmail.com
LinkedIn

SUMMARY

Technology oriented student intern with good debugging and analytical skills, possessing good communication skills as well, currently looking for job opportunities to apply my engineering knowledge for the growth of the organization while tailoring my own skills at the same time.

EDUCATION

Degree	Institute	Year of Passing	CGPA/Percentage
MTech in VLSI	Delhi Technological University, Delhi	2023- Pursuing	8.13
BTech in ECE	Maharaja Agrasen Institute of Technology, GGSIPU, Delhi	2018-2022	9.05
Intermediate	Vivekananda School, Delhi	2018	94

EXPERIENCE

- **NXP Semiconductors** *July 2024- June 2025*
  Intern (Advanced Chip Engineering) **Noida**
  - Contributed to SOC integration efforts by implementing signal and power routing strategies for analog blocks and macros, with emphasis on minimizing routing effects like crosstalk, parasitics and IR drop to ensure analog performance.
  - Actively participated in debugging the signoff checks including DRC, LVS and ERC for the HIFI 5 DSP for audio and voice processing applications at 16nm technology node, utilizing industry standard tool, Siemen's Calibre and also working with the Innovus Database for the same.
  - Carried out comprehensive research on designing an I/O ring to strengthen ESD protection and achieve optimal performance for the specific test case design.
  - Explored the ESD checks and actively debugged ESD errors using PERC at 16nm technology node on HIFI5 and a provided testcase
  - Explored various aspects of floorplan, placement, CTS and routing.
  - Designed and executed TCL and Makefile scripts to generate cdl and Caltex files
  - Demonstrated strong problem- solving skills, adaptability, and eagerness to learn in a dynamic engineering environment.

PROJECTS

- **Inverter Chain Design ESD, DRC, LVS and IO ring Optimization**
  - Designed the I/O ring for an inverter chain-based architecture with integrated digital voltage domains. Implemented ESD protection using PERC and ESRA, while also troubleshooting and resolving DRC, LVS, and ERC issues in the design.
- **Low Power D latch design using MCML Tri state buffer**
  - Designed and implemented a low-power D latch with an MCML tri-state buffer in Virtuoso for optimized performance.
- **Verilog Vending Machine**
  - Designed and built an FSM based vending machine in Verilog having 3-4 products generation based on user input.

TECHNICAL SKILLS

- **Programming Languages-** Verilog HDL, TCL
- **Design Tools-** Siemens Calibre, Cadence Innovus, Cadence Virtuoso and LtSpice, Cadence Conformal
- **Key Courses-** Low power Digital Design, Physical Design, CMOS, Basics of STA, Analog and Digital electronics, Silvaco

CERTIFICATIONS

- **Innovus Block Implementation with Stylus Common UI** Cadence Design Systems
- **Basic Static Timing Analysis** Cadence Design Systems

RESEARCH WORK AND PUBLICATIONS

- **Title-** Nanoscale Temperature Dependent Quantum-Effect Analytical Model of Short- Channel, Junction-Less, Double-Gate Stack (SC-JL-DG) MOSFET for Analog Applications at Higher Frequencies", Microelectronics Journal, Volume 141, 2023, 105952, ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2023.105952. *2023*
- **Title-** Quantum Effect dependent modelling of Short Channel Junctionless Double Gate Stack (SC-JL-DG) MOSFET for Analog Applications" Microelectronics Journal (Elsevier), vol. 134, pp. 105726, (Online ISSN: 0026-2692, Digital Identifier: https://doi.org/10.1016/j.mejo.2023.105726. *2022*

ACHIEVEMENTS

- Women in Engineering (WIE) Chairperson at IEEE MAIT. *2020*
- Training on Analog and Digital circuit CMOS design and application using PSPICE under the guidance of Mr. P.K. Sinha