M. Tech (Power Electronics and Systems)

Vipul Thakur

2025

DESIGN AND ANALYSIS OF A BI-POLAR LOW VOLTAGE D.C SYSTEM

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY

IN

POWER ELECTRONICS AND SYSTEMS

Submitted by

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"**DESIGN AND ANALYSIS OF A BI-POLAR LOW VOLTAGE D.C SYSTEM**"** which is submitted by VIPUL THAKUR (2K23/PES/12), Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ACKNOWLEDGMENT

I would like to express my heartfelt gratitude to my respected teacher and mentor **Saurabh Mishra, Assistant Professor,** Department of Electrical Engineering for their invaluable guidance, unwavering support, and expert insights throughout this journey. Their dedication and expertise have been instrumental in shaping this work. Grateful to all the Electrical Engineering faculties, Power Electronics laboratory, PhD scholars, and laboratory assistants for their valuable inputs.

A special note of thanks goes to my mother and father, their boundless love, encouragement, and unwavering faith have been my pillar of strength. Her sacrifices and support have been the cornerstone of my endeavours.

Lastly, my heartfelt thanks to all my friends who have stood by me, offering support, encouragement, and moments of relief during challenging times. Your camaraderie and companionship have made this journey memorable.

Thank you to everyone who played a part, directly or indirectly, in the realization of this endeavour. Your contributions will forever be cherished.

Date: 31th May, 2025

Place: Delhi

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ABSTRACT

This thesis presents a comprehensive study on the design, analysis, and control of bipolar DC-DC converters tailored for low-voltage DC (LVDC) bipolar distribution systems. Bipolar LVDC systems offer a flexible and efficient means of power distribution, particularly in renewable energy-integrated microgrids. A key challenge in such systems is maintaining voltage balance across the positive and negative rails, which is addressed using specialized bipolar DC-DC converters acting as voltage balancers. The thesis begins with the classification of various bipolar converter topologies, configurations, and interconnections. It then introduces and analyses two main converter designs: the Boost derived and the boost-luo interleaved (NBLI) DC-DC converters. The Boost derived converter is designed as a single-input dual-output topology by interleaving boost stages and buck-boost. Time multiplex regulation strategy presented for independently regulate both output capacitors, maintaining balanced voltages in the bipolar bus. The NBLI converter is designed for high-gain, high-efficiency operation with reduced current ripple and lower stress on switching components. Interleaving improves dynamic response and power density, making it suitable for high-current applications. Furthermore, additional converter topologies including a dual-output buck and buck-boost-based converter, and a boost-SEPIC interleaved converter are explored. These designs offer independent voltage control, minimal component stress, and reduced right-half-plane zero issues, improving overall system reliability. Also, the classification of bipolar DC system with its connection configurations and derived topologies for bipolar operations are presented. Control strategies for each topology are formulated using open-loop and voltage-mode feedback methods. Presented converters effectively enhance voltage balancing, current sharing, and load regulation in bipolar LVDC systems. Overall, the thesis delivers technically robust converter designs and control schemes that improve performance, reliability, and scalability in bipolar LVDC system and the performance of the presented DC-DC converter is verified by the MATLAB/Simulink simulation modal.

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CHAPTER 1

INTRODUCTION

1.1 General Aspects

Power distribution in DC is made possible by the development of modern technologies and pursuit of sustainability. Advancement in modest, incredibly resilient, dependable, and efficient dc distribution system has gained attention due to the modernization of electronic loads, rise of renewable energy sources (RESs), and the use of energy storage systems (ESSs). Although been widely utilized in the past, unipolar DC bus design has found challenging to meet the efficiency and reliability requirements of many emerging applications, which includes as server rooms and swift EV charging stations. As demonstrated in Fig. 1, The connections to the utility grid allow for the conceptualization of bipolar DC microgrids. in consideration. Compared with the unipolar DC bus, Data facilities, residential buildings, and intelligent industrial parks each made significant utilization of the bipolar dc bus system given that it delivers greater versatility, stability, and efficiency. These grids, often operating at ±350 V, require DC-DC converters with monopolar input and bipolar output to independently control voltages while minimizing leakage current by grounding the PV panel's negative pole. One of the main features of bipolar grids is that it drops amplitude of the potential relative to earth, managing higher loads to be tied to their all power. A bipolar DC system having ±170 V may be used with either a 170 V or 340 V voltage supply, enhancing its flexibility.

The main issue is associated with the potential of a voltage disparity among the bipolar poles. Throughout its operation, loads with varying nominal powers might be attached to either the upper or lower pole; as a result, each pole's voltage level tends to change yielding a voltage imbalance. A microgrid's dc buses can be regulated through a variety of approaches. The voltage balancer is a piece of equipment utilized for controlling the microgrid's dc voltage imbalance. In the bipolar LVDC distribution system application, DC–DC converter, a SIDO bipolar converter, acts as a voltage balancer shown in Fig.

1.1. When converting renewable energy sources like solar or wind into multiple regulated DC outputs, bi-polar output DC-DC converters are optimal approach.

1.2 State of The Art on DC Bipolar Grid

The centralized framework in One of the most fundamental bipolar DC micro grid arrangements to support voltage is shown in Fig. 1.1. A bipolar DC-DC converter, or voltage balancer, acts as a power electronic circuit with energy-storage elements like inductors and capacitors as well as power electronic semiconductors. Depending on the voltage imbalance, their only function is to move power between positive pole to negative pole or the other way around.

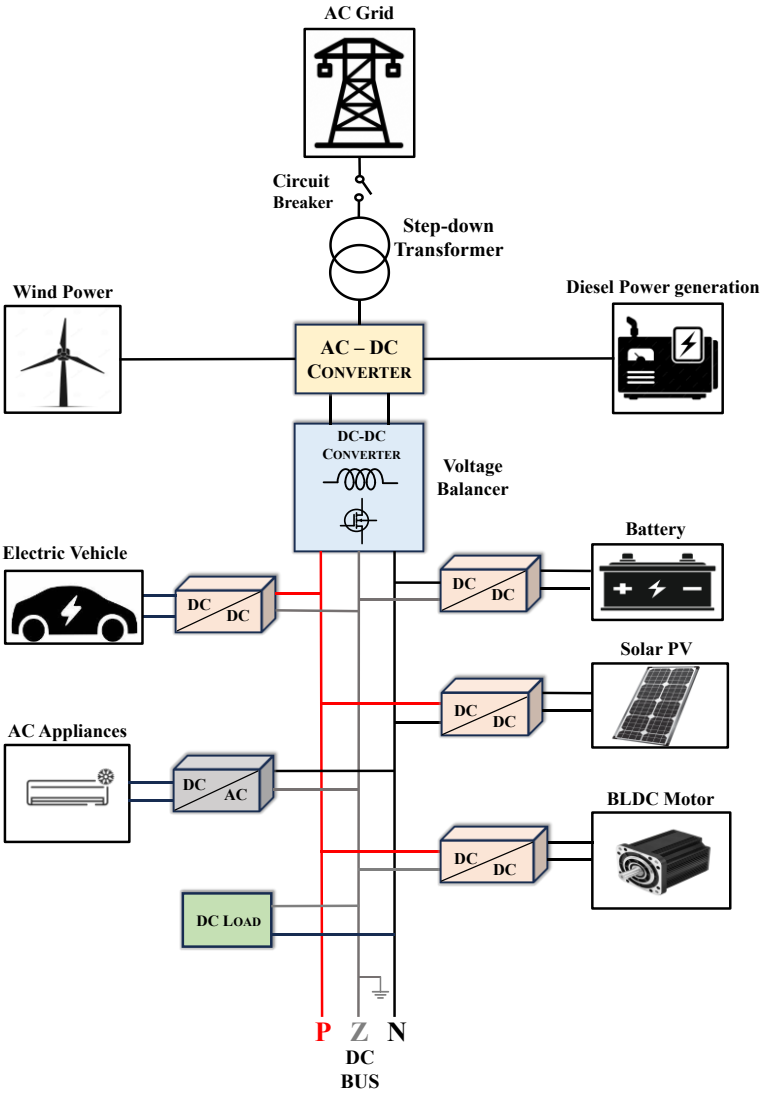

Fig. 1.1 Bipolar LVDC Connected to Grid

Homes and utilities can use the bipolar LVDC, a DC bus framework with 3 wire DC lines, as a small DC supply system, as illustrated in Fig. 1. It links a distribution system with several DC power sources and loads employing three voltage levels. They offer advantages such boasts smaller size, lesser elements, and a cheaper price compared to using separate converters, though they introduce design complexity and limit output power. Here, in thesis the presented converter i.e. SIDO bipolar DC-DC converter topology integrates boost and buck-boost converters, sharing a one inductor to efficiently deliver power and independently charge two capacitors. Generator and load with bipolar connections.

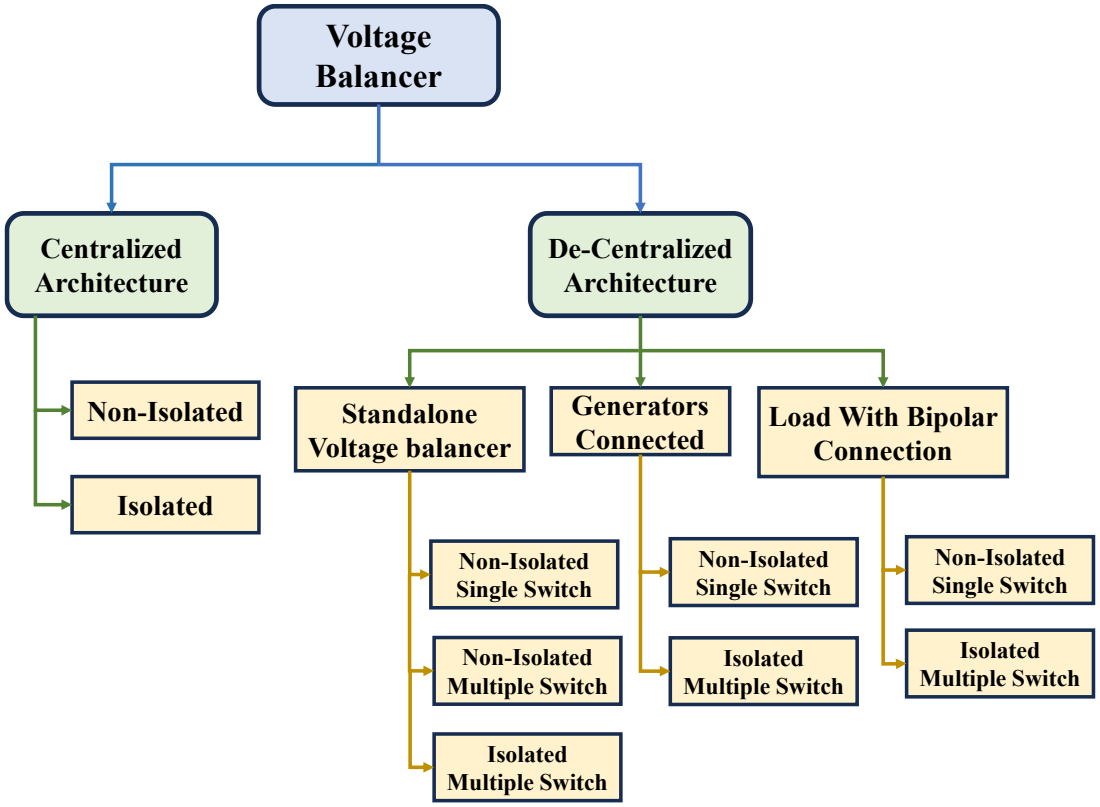

Fig. 1.2 Classification of Voltage Balancers in Bipolar DC System

This integration improves voltage gain, reduces semiconductor stress, and minimizes current stress and filter size. These converters also act as voltage balancers, ensuring stable operation in bipolar low-voltage DC (LVDC) systems used for high-power microgrids.

TABLE 1.1 Applications Voltage Level of Bipolar System

Utilizations	Voltage Potential
Data Facilities	± 190 V
Flight System	± 270 V
Residential Places	± 170 V
Water Ships	± 750 V
EV Charge Facilities	$> \pm 269$ V

Compared to conventional one output transforms integrated SIDO and Single-Input Multi-Output (SIMO) designs minimize the quantity of elements, system volume, and cost, while enhancing the efficiency and reliability of DC microgrids interfacing with renewable energy sources and AC systems.

1.3 Conclusion

Bipolar LVDC system that is connected to the grid is depicted in Figure 1 as a DC bus structure with 3 wire DC lines that operates as a DC bipolar network. In a three-voltage distribution system, it connects several DC energy sources and loads to enhance its reliability and efficiency.

CHAPTER 2

LITERATURE SURVEY

2.1 General Aspects

This section comprises the literature survey of the bipolar DC system

LVDC power systems have received growing interest in present times mainly in the growth of DC renewable power generation and consumption. This happens because of the advantages in terms of power transformation efficiency and adaptability of control. Low wattage rating renewable energy sources (RES) will be increasingly prevalent in domestic applications in future in a manner to match increasing energy needs and minimize the carbon emissions [1]-[3].

It is feasible to directly integrate photovoltaics as a source of power without an AC connection. in commercial, residential, or industrial buildings with DC grids. When working on bipolar DC grids (Fig. 1), such as those that have ± 350 V, DC/DC converters that can govern both voltages independently must be worked with. In order to prevent leakage current, the PV panels' negative pole needs to be grounded. SIDO DC-DC converters are so regularly employed to transform DC produced by small wind turbines or solar panels into a variety of regulated DC output voltages. For high-power microgrids, bipolar DC grids are now a suitable option. This is mainly due to the higher power transmission capability of this architecture. In bipolar DC grids, DC-DC converters, which require a bipolar output and a monopolar input can connect any distributed generation system. [3]-[11]

According to polarity, DC microgrids can be categorized as unipolar, bipolar, or homopolar. The most adaptable of these is the bipolar DC microgrid (BDCM). Three-wire DC distribution used by bipolar microgrid design consisted of a $+V_{dc}$ line, a neutral line, and a $-V_{dc}$ line. Key perk the method is providing that, output-side power converters could select input voltage from the voltage levels: $+V_{dc}$, $-V_{dc}$, or $2V_{dc}$. One of the primary characteristics of bipolar grids is that they reduce the voltage's magnitude in relation to ground, enabling larger loads to be connected to their full rating. By Taking an example for instance, here bipolar LVDC system having ±24 V

we can utilized with either a 24 V or 48 V as voltage source, resulting in improving its flexibility. Thus, BDCM system offers pliability and increased efficiency as well as reliability [11]-[19].

High-power microgrids can now be adequately served by bipolar DC grids. This is mostly because to the higher power transmission capability of this design. The DC-DC converters, should need to be connected mono input and bipolar output, required to connect any distributed generation system to bipolar DC grids. Being that the loads and sources are not evenly distributed between the two poles, the bipolar DC microgrid is prone to voltage and current imbalances. To maintain equilibrium of these DC microgrids, particular power electronic-based solutions are therefore needed [19]-[25].

Even though BDCM has many benefits, but linking RESs to BDCM is difficult because of the bipolar voltages, which must have to be proportionated for best functioning. Here, DC-DC converter that integrates the RESs with BDCM needs to be capable of high voltage gain. The RESs and BCDMs are interfaced using three-level boost (TLB) converters. TLBs' non-isolated structure allows them to efficiently proportionate output voltages and more effectiveness as well as affordability. Nevertheless, voltage gain of TLB converters is limited, and they lack an interleaved structure. Bipolar output voltages of many high gain DC-DC converters are presented for counteract voltage gain constraints of TLB converters. Nonetheless, converter in [6] lacks interleaving, has high switching losses, and is unable to achieve perfect balance under all loading conditions, whereas converter in [9] having restricted functional limit in regard to duty cycle [25]-[31].

During integration with RESs or battery as source units, an interleaved structure is recommended because it lowers source current ripple, increasing RES MPPT performance and input power source's longevity. In [10], a Boost-Zeta Interleaved (NBZI) multiport, non-isolated converter is displayed. With a single input and dual outputs (SIDO), presented topology consists of a boost and zeta converter combination. The topology's principal objective is to produce regulated DC voltage, which qualifies it for LVBDCM. Here, converter is optimal for low voltage bi-polar DC grid but converter have relatively low voltage gain. Although converter have relatively low voltage gain, it is ideal for low voltage bipolar DC grids. In [11], a

Boost-Cuk derived converter for a bipolar DC microgrid with an interleaved topology is proposed and current control approach is employed. [31]-[34]

The boost and buck-boost converters are combined in this case. The demonstrated system combines the traditional boost and buck-boost converters and charges two output capacitors by transferring input energy through a single inductor. Dual output DC–DC converters need to have voltage balancing for some applications, such as bipolar low-voltage DC (LVDC) supply networks. [35]-[41]

DC microgrids are usually designed to connect to an ac grid and/or additional sources of renewable energy to increase the quantity of electrical power available to the microgrid. Compared to conventional boost and buck-boost converters, the semi-conductor (switches) devices' maximum voltage stress is reduced and their output voltage gain is increased. [42]-[46].

The effective filter size, current stress, and current rating of the switches are likewise decreased by interleaving [13]. One frequent approach is to design a SIDO DC-DC converter using a topology that can provide both step-up and step-down abilities for voltage. With it, the converter can efficiently manage output voltage across the two output channels while converting input voltage to necessary output voltage levels.. [47]-[50].

Compared to two independent DC-DC converters, SIDO DC-DC converters provide several benefits, such as fewer parts, a little size, and a reduced cost. However, they may also have some drawbacks, like more sophisticated and sensitive design and lower output power than two independent converters. [51]-[54].

Additionally, DC-DC converters are essential in a variety of applications, such as renewable energy, portable chargers, and PFC. Several distinct traditional SISO DC–DC converters are used to offer various voltages in numerous outputs from a single dc source. Boost, buck-boost, buck, cuk, flyback, and SEPIC converters are examples of these converters. However, the usage of multiple independent SISO converters has resulted in an increase in the system volume, cost, and number of components. Multiple SISO converters have been paired to create a single-input multi-output (SIMO) DC–DC converter in order reduce the number of components. [55]-[59].

A bipolar output DC–DC converter serves as the voltage balancer in Figure 1 for bipolar LVDC distribution system application. This facility might effectively connect energy storage systems (ESSs) to fulfil the same purpose. To cut down on components, a single-input multi-output (SIMO) DC–DC converter was created by combining several SISO converters. [60]-[64].

2.2 Objectives of Thesis

The objectives of thesis work are as follows:

1. To facilitate understanding of bipolar low-voltage (LVDC) systems and role of bipolar DC-DC converter as voltage balancer.
2. Classification of various bipolar DC-DC converter topologies, connections and configurations.
3. To design and analyse presented Boost Buck-Boost (BBB) converter for the Bipolar LVDC system.
4. To design a control scheme for BBB DC-DC converter to charge two output capacitors independently.
5. To design and analyse presented non-isolated boost-luo interleaved (NBLI) DC-DC converter for the Bipolar Low voltage DC (LVDC) system
6. To design a control scheme for output voltage control of NBLI DC-DC converter.
7. To verify the performance of the presented bipolar DC-DC converter by the MATLAB/Simulink simulation modal.

2.3 Outline of Thesis

This section gives insight about the presented work in this thesis. The bipolar DC system with DC-DC converter as voltage balancer converter, classification of various bipolar DC-DC converter topologies, design and analysis of Boost Buck-Boost (BBB) DC-DC converter by interleaving boost and buck-boost DC-DC converters, design and analyse of presented non-isolated boost-luo interleaved (NBLI) converter. Here, overview of boost, buck-boost, zeta, luo presented converter as follows:

Chapter 1: In Chapter 1, an introduction to comprehensive bipolar LVDC distribution system presented, incorporating overview for evaluation to comprehensively explore its fundamentals. Furthermore, this chapter explores the brief introduction about the presented step-up SIDO converter in this thesis.

Chapter 2: This chapter involves the literature survey which includes the introduction to the overview of the bipolar presented topology which is of bipolar output derived DC-DC converters. The objectives of the thesis are also represented in this section respectively.

Chapter 3: Here in chapter 3, section 3.1 explores This chapter explores the classification of bipolar DC system, connection configuration in bipolar system, and different DC-DC converters derived topologies. Also, with classification of bipolar DC system is based on DC-DC converter topologies, connection configuration of converters and their architecture.

Chapter 4: This chapter presents a This chapter explores the design and analysis of presented SIDO Boost Buck-Boost converter which includes state-space analysis, design, implementation of Time multiplexed control scheme and simulation analysis of the presented converter.

Chapter 5: This chapter presents a SIDO non-isolated boost-luo type converter is presented. Appropriate for low voltage bi-polar DC microgrid applications and renewable power sources such as fuel cells and solar PV. Here, the two outputs are designated for the Boost and Luo converter, respectively. Presented converter have steady source current with nominal ripples because of the implementation of interleaving technique along with considerable high gain. Objective of the presented converter is to increase the power handling capacity by creating multi ports at the output and provide high gain. Interleaving of the converter, lowers the switches current rating, effective filter size, and current stress. As a result, a low voltage bipolar system would benefit greatly from the presented topology. This converter operates as voltage balancer in bipolar system.

Chapter 6: This chapter introduces a novel SIDO DC-DC converter. The two degrees of freedom in this presented converter enable the outputs to be independently regulated. Additional benefits involve a low component count, a simple design, and less voltage stress on the switching components. Right half s-plane zeros do not exist in this topology independently of the converter parameters. The two degrees of freedom in this suggested converter allow the outputs to be distinctly regulated.

Chapter 7: For a low-voltage bipolar dc microgrid application, a boost-SEPIC interleaved type dc-dc converter is presented in this configuration. With two outputs, the suggested converter combines a boost and SEPIC converter in parallel. It works effectively in a bipolar dc microgrid setting for low-voltage, high-current applications. DC-DC buck converter and boost-SEPIC interleaved converter functioning as a load converter controlled by voltage loop control. The suggested converter's dynamic modelling and steady-state analysis are provided in detail. Results from simulations are presented to validate the converter's performance.

2.4 Conclusion

This chapter comprises the literature survey of thesis where the overview about chapters is discussed. Here, objectives of thesis, outline of thesis with each chapter are discussed respectively. On concluding this chapter, following chapters are classifications of bipolar DC system and following with derived bipolar DC-DC converter topological chapters are presented.

CHAPTER 3

CLASSIFICATION OF BI-POLAR DC SYSTEM

This chapter explores the classification of bipolar DC system, connection configuration in bipolar system, and different DC-DC converters derived topologies.

3.1 General Aspects

The classification of bipolar DC system is based on the DC-DC converter topologies, connection configuration of converters and their architecture.

3.2 Connection Configuration in Bi-polar DC System

Two fundamental architectures of voltage balancers are 1) distributed and 2) centralized. Here, a single voltage balancer linked to converter which links to AC electric grid is installed. This design clearly has a drawback, particularly in long-line dc microgrids. Voltage losses on the lines at location farthest from centralized voltage balancer use may result in a substantial voltage imbalance.

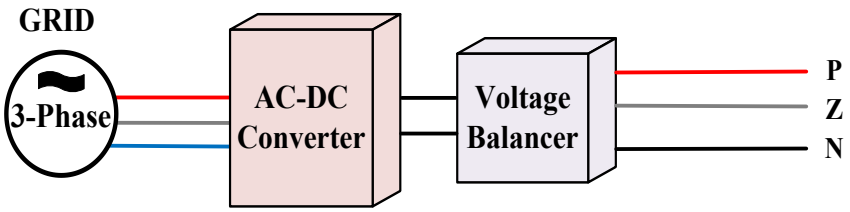

Fig. 3.1 Centralized Architecture of Bipolar DC System

Now, 2nd architecture that roles multiple voltage balancers in the microgrid's weakest sections can be designed to get around this. Since several voltage balancers are necessary along DC lines in this setup, the cost is higher.

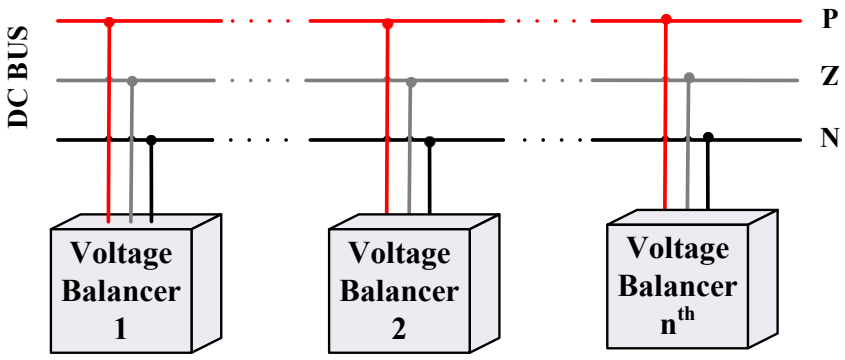

Fig. 3.2 Decentralized Architecture of Bipolar DC system

Bipolar DC microgrids are distinguished by their adaptable load and power source connections, which can be made in three different ways: Positive-to-negative (PN), zero-to-negative (ZN), and positive-to-zero (PZ) are three. If no corrective action is taken, unequal consumption will result in a voltage imbalance.

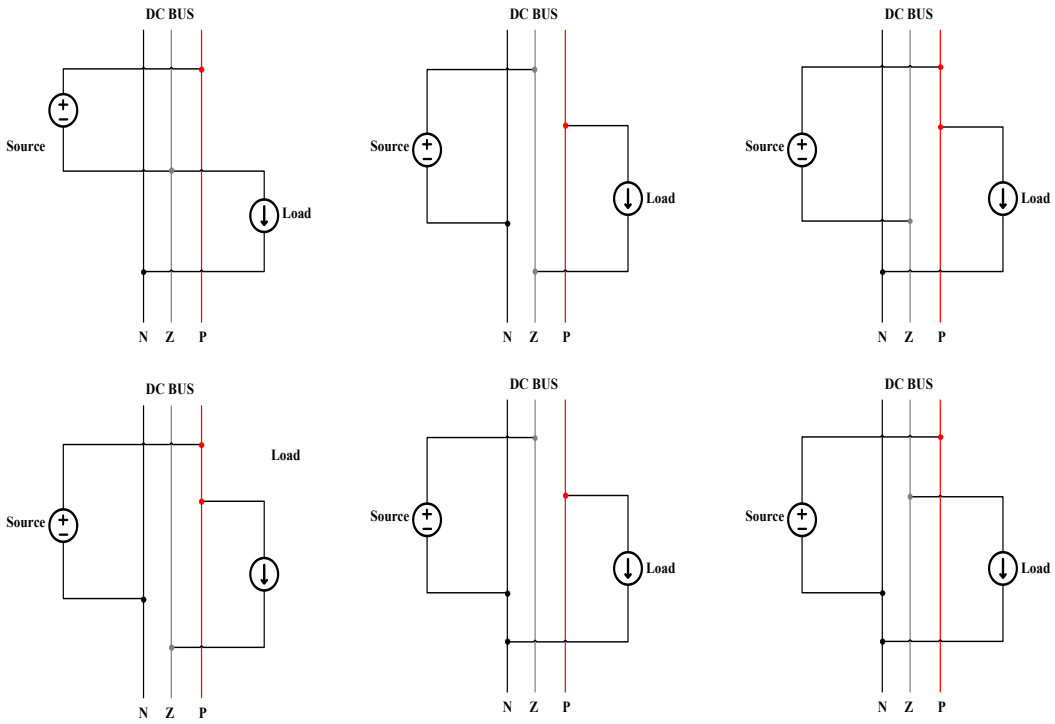

Fig. 3.3 Six Connections Produce Bipolar DC Microgrid Voltage Imbalance

An uncontrollable voltage imbalance in the microgrid can arise from asymmetrically combined converter interfaced components. The protection system may be affected, and sectors or even the entire microgrid may be disconnected as a result. In the

following three scenarios, the voltage balancer, or bipolar DC-DC converters, and imbalance issue do not arise:

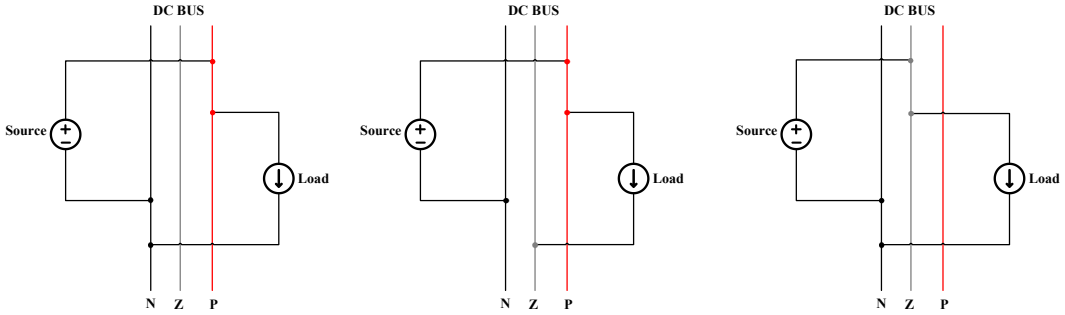

Fig. 3.4 Connection Configuration to Mitigate Voltage Imbalance

The imbalance issue does not arise in the three scenarios. Specifically, no issue related to voltage imbalance will arise if both the sources and loads are PN linked, or PZ or ZN connected, as shown in here.

3.3 Boost Derived Bipolar DC-DC Converter Topologies

The Boost derived bipolar DC-DC converter topologies with single and multi-switch configuration as follows:

3.3.1 Single-Switch Boost Derived Bipolar DC-DC Converter Topologies

1. The reduction of input current ripple by the use of integrated magnetic cores. This topology shows a combination of the Zeta converter and the buck-boost. The value obtained with the buck-boost cell is equal to the gain of each of its outputs.

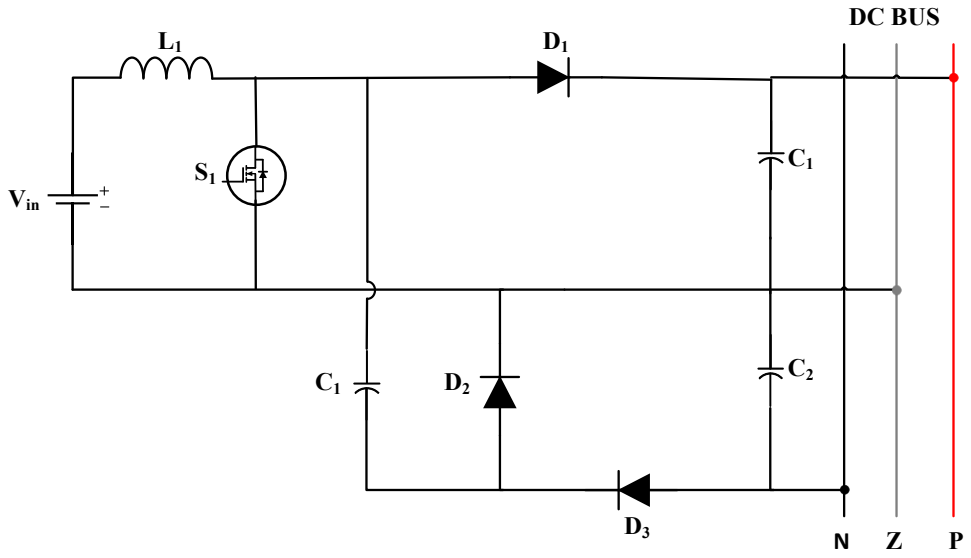

Fig. 3.5 Boost Self-Lift Type Type DC-DC Converter

3.3.2 Multi-Switch Boost Derived Bipolar DC-DC Converter Topologies

1. Depending on power switching, the three-level boost converter enables either balanced or unbalanced energy transfer.

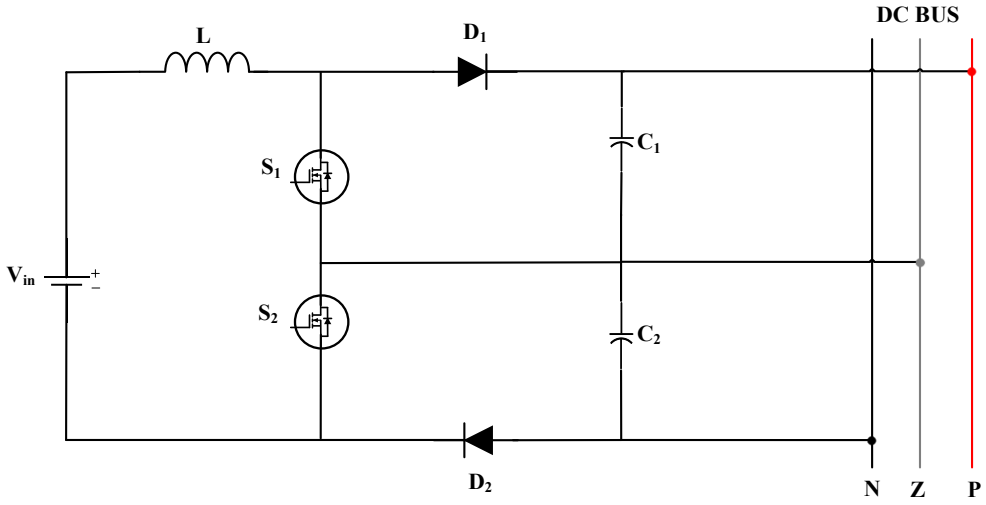

Fig. 3.6 Boost self-lift type DC-DC Converter

2. Due to earlier solution's discontinuous input current, certain applications, like PV generators, have constraints that necessitate the use of extra input filters. The input-parallel output-series converter in conjunction with two dc-dc converters.

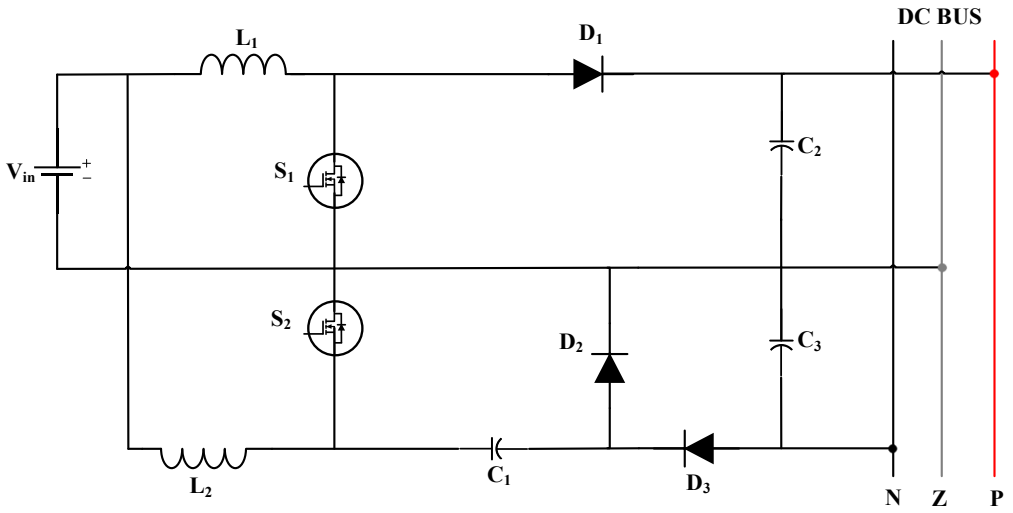

Fig. 3.7 Multi switch input-parallel output-series type DC-DC Converter

3. Integrating 2 bidirectional converters, such interleaved boost-SEPIC converter shown in Fig. 3.8, is one method. Both converters have their outputs connected in series and their input sides connected in parallel (interleaved). An ESS (such as a battery) or RES (such as PVs) can be used as the input source.

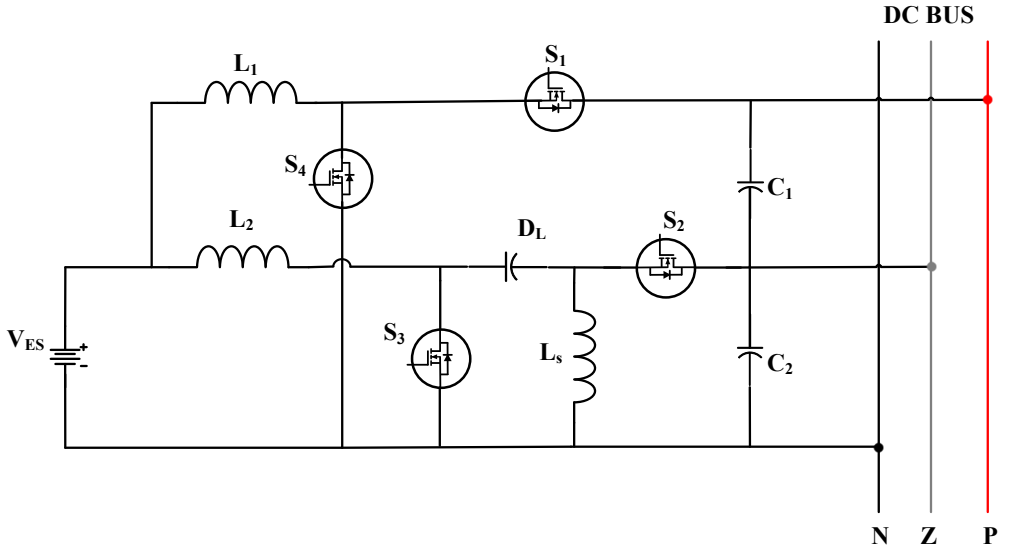

Fig. 3.8 Interleaved bidirectional boost-SEPIC

4. In this presentation, the bipolar DC system application is represented by an interleaved boost-SEPIC converter. It has the potential to operate in both directions as well.

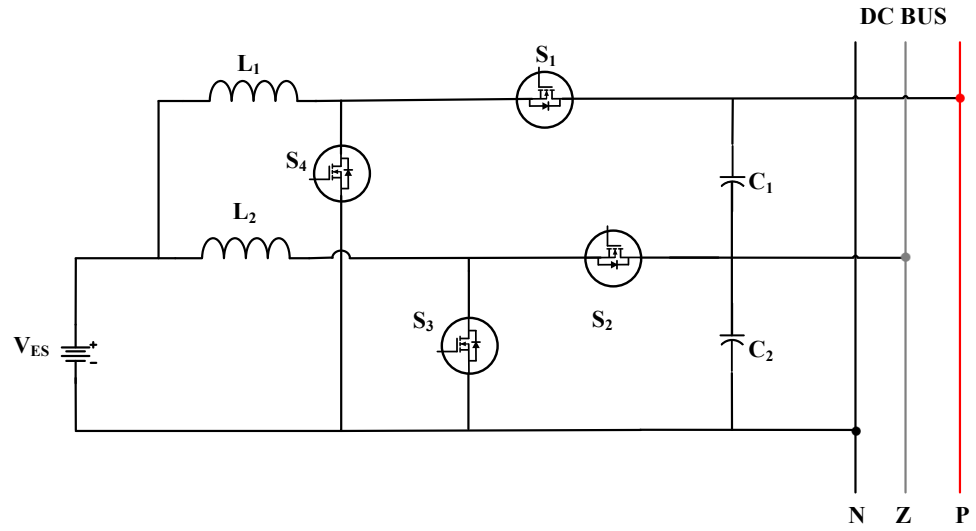

Fig. 3.9 Interleaved bidirectional boost-SEPIC

5. This topology comprises a single input, double output boost and zeta converter. Providing regulated bipolar output at 24- and 48-volts DC is the primary objective of the presented topology, which makes it suitable for low voltage bipolar DC systems. Creating regulated bipolar output at 24- and 48-volts DC is the main goal of the suggested topology, thereby rendering it suited to low voltage bipolar DC system.

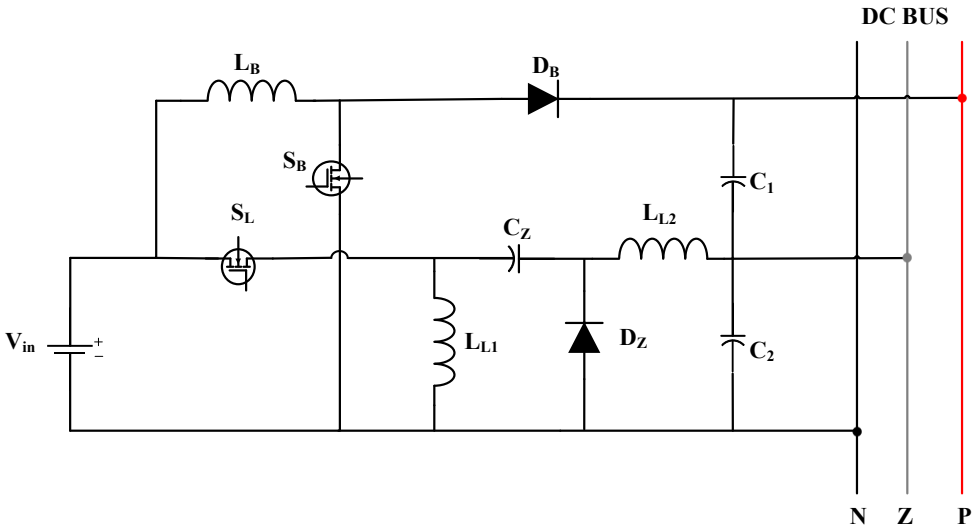

Fig. 3.10 Interleaved bidirectional boost and zeta

6. Here, a two-output SEPIC converter and parallel boost are utilized. For low-voltage, high-current applications, it performs admirably in a bipolar dc system. This converter is appropriate for a low-voltage bipolar dc microgrid.

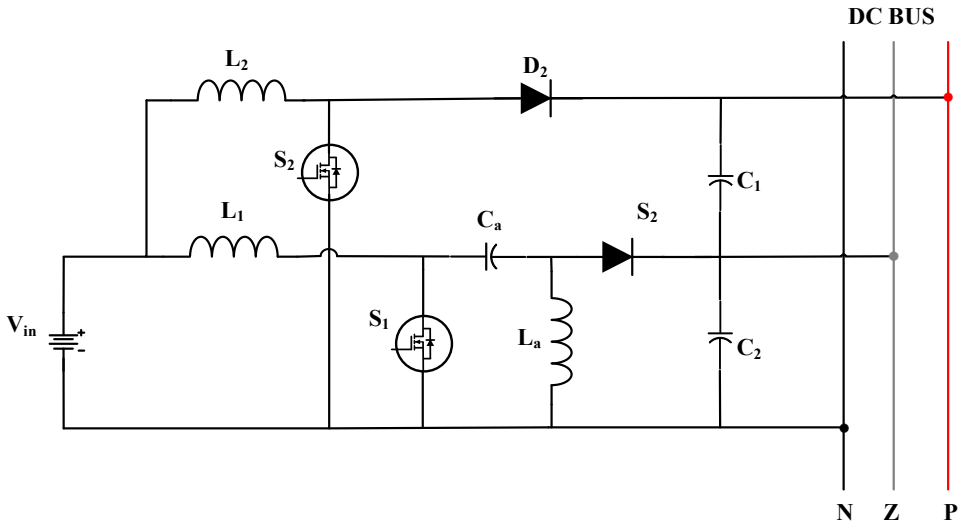

Fig. 3.11 Interleaved boost-SEPIC

3.4 Buck-Boost Derived Bipolar DC-DC converter Topologies

The Buck Boost derived bipolar DC-DC converter topologies with single and multi-switch configuration as follows:

3.4.1 Single-Switch Buck-Boost Derived Bipolar DC-DC Converter Topologies

1. This is a representation of the buck-boost using the Zeta converter. The value obtained with the buck-boost cell is equal to the gain of each of its outputs.

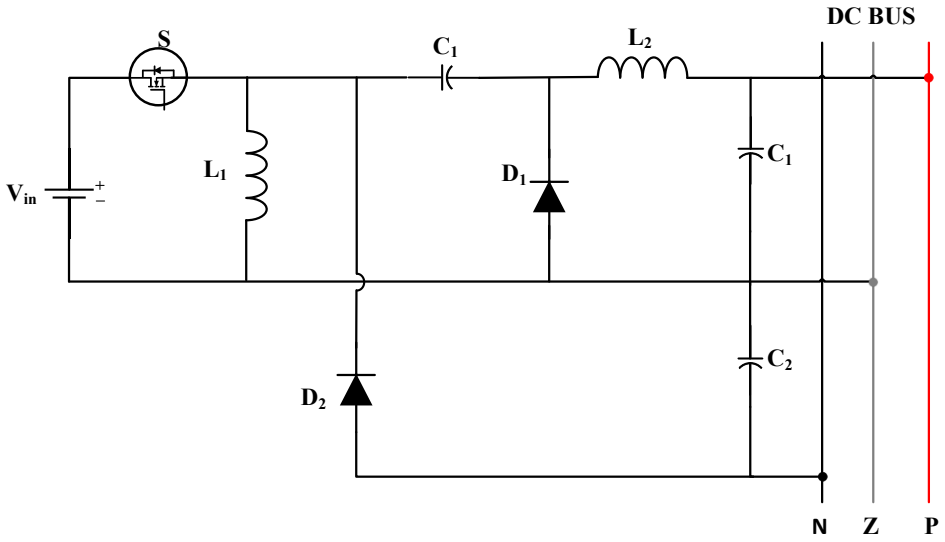

Fig. 3.12 Circuit diagram of Bi-Polar buck boost Zeta converter DC-DC converter

3.4.2 Multi-Switch Buck-Boost Derived Bipolar DC-DC Converter Topologies

Here, multi-switch buck-boost derived bipolar DC-DC converter topologies are as:

1. The converter controls the bipolar system's input and output power and provides a voltage balancing function, delivering power to the system during overload conditions.

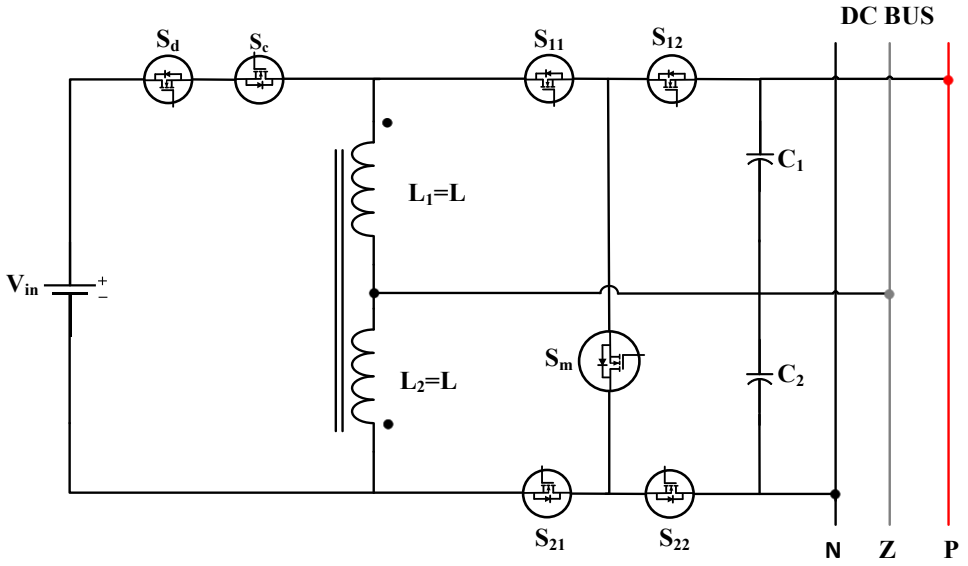

Fig. 3.13 Circuit diagram of Bi-Polar multidirectional buck–boost converter

2. Here, the rectifier provides the input DC, and the centralized voltage balancer of the half bridge or buck-boost types is displayed. extensively used, typically installed as a second stage in unidirectional or bidirectional grid rectifiers, among other applications.

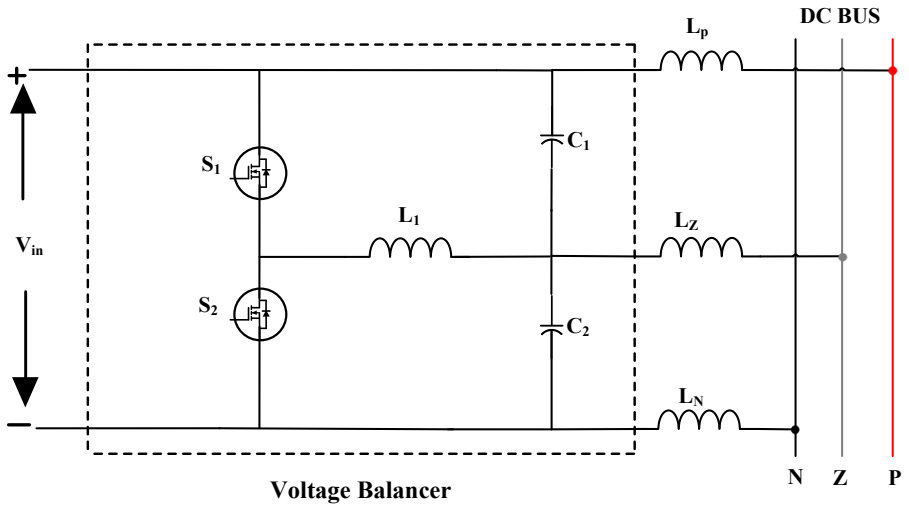

Fig. 3.14 Circuit Diagram of Bi-Polar Buck–Boost Converter Type Voltage Balancer

3. In this circumstance, Since the input dc voltage is supplied by the rectifier, bipolar side can be supplied by an overall voltage that is lower compared to the input dc voltage. The reduction of turn-off switching losses is the primary benefit.

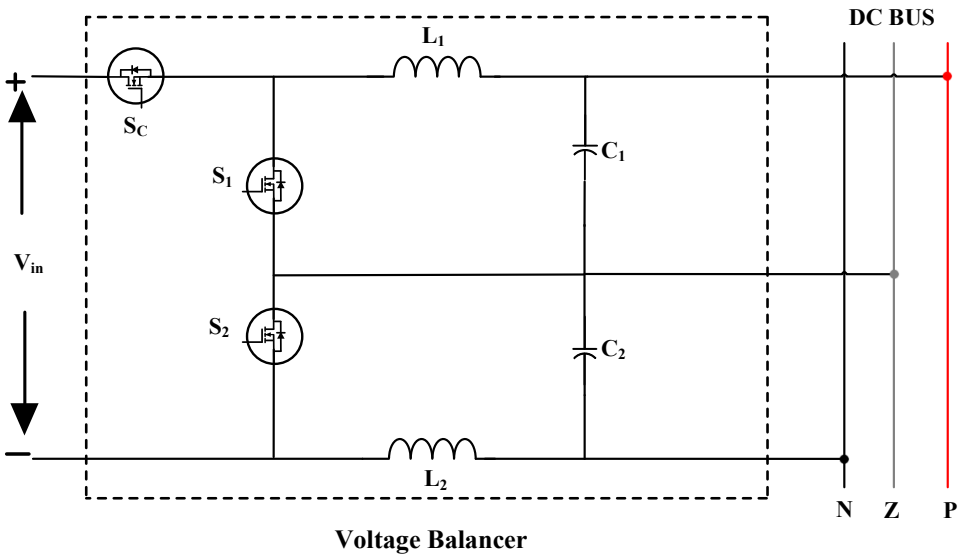

Fig. 3.15 Circuit diagram of Bi-Polar Improved buck–boost converter type voltage balancer

4. Three-level structures which offer both buck and boost operation, based on the SEPIC and buck-boost. Due to the former solution's discontinuous input current, certain applications—like PV generators have limitations that mandate the inclusion of additional input filters.

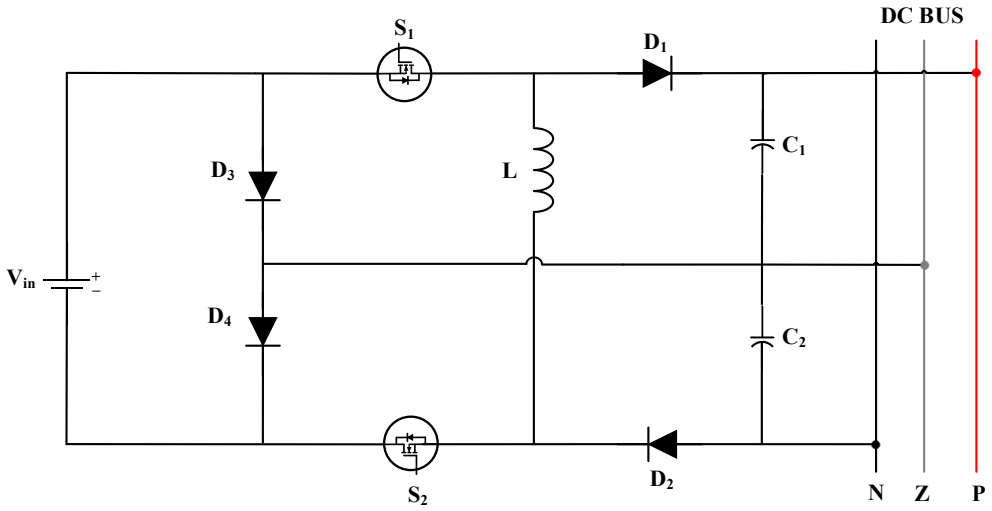

Fig. 3.16 Circuit diagram of Bi-Polar three-level buck-boost converter

5. A three-level buck-boost architecture with an ESS help balance the bipolar DC microgrid. Energy can be transferred by the ESS to one or both output capacitors by coordinating the switching operation of S2 and S3 in boost mode.

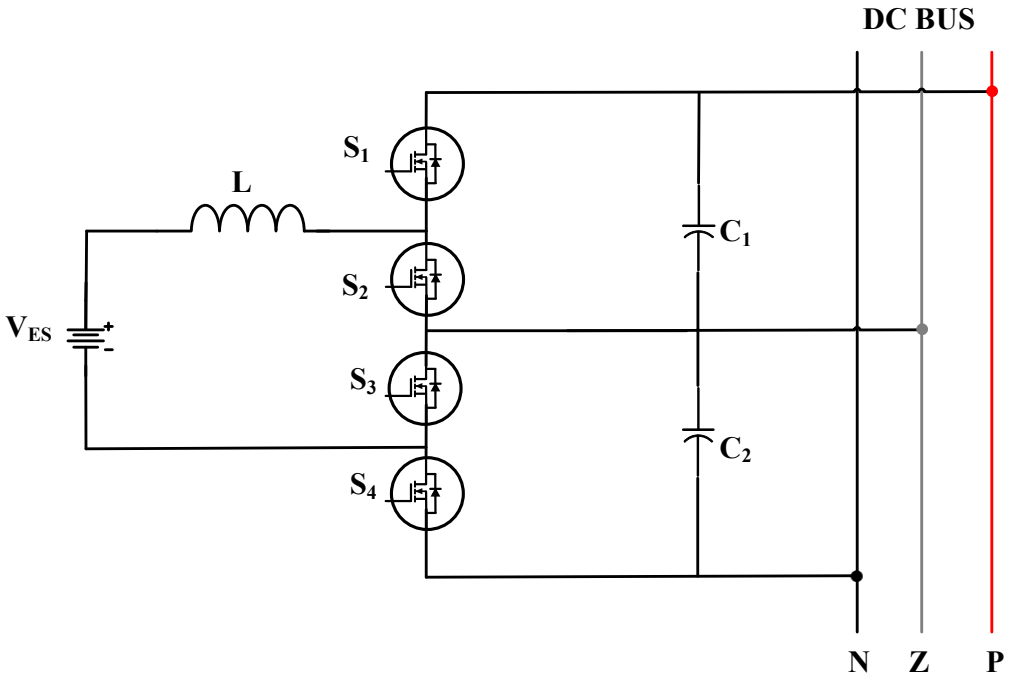

Fig. 3.17 Circuit diagram of Bi-Polar three-level bidirectional buck-boost type converter

6. A front-end quadratic boost cell (QBC) efficiently offers the buck-boost voltage gain feature, while a three-switch based LC-cell (TSLC) is in charge of bi-polar load voltage realization. Even under operating conditions with a positive output load voltage, this bi-polar converter provides enhanced boosting capability albeit possessing lesser controlled switching devices.

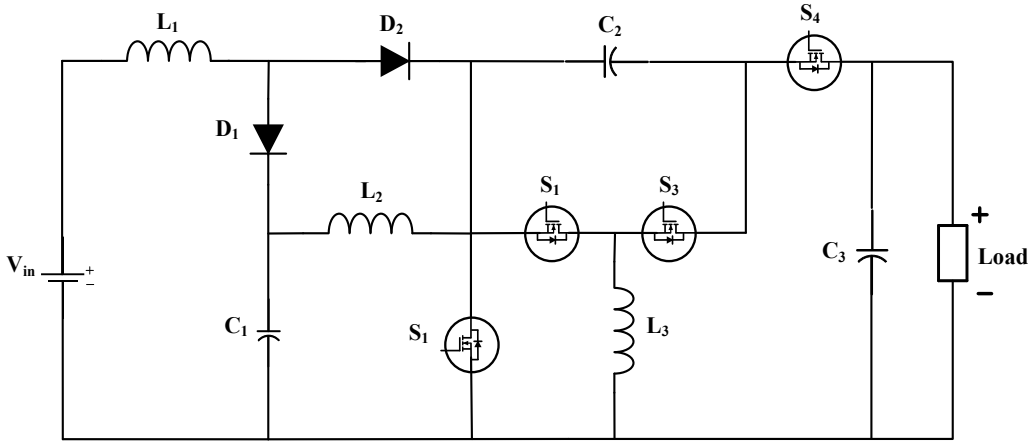

Fig. 3.18 Circuit diagram of Bi-Polar Buck-Boost Converter

7. The modified SEPIC-cuk DC–DC converter can function as a bidirectional dc–dc converter alongside to a voltage balancer. Bidirectional power flow allows the converter to make up for unbalanced power.

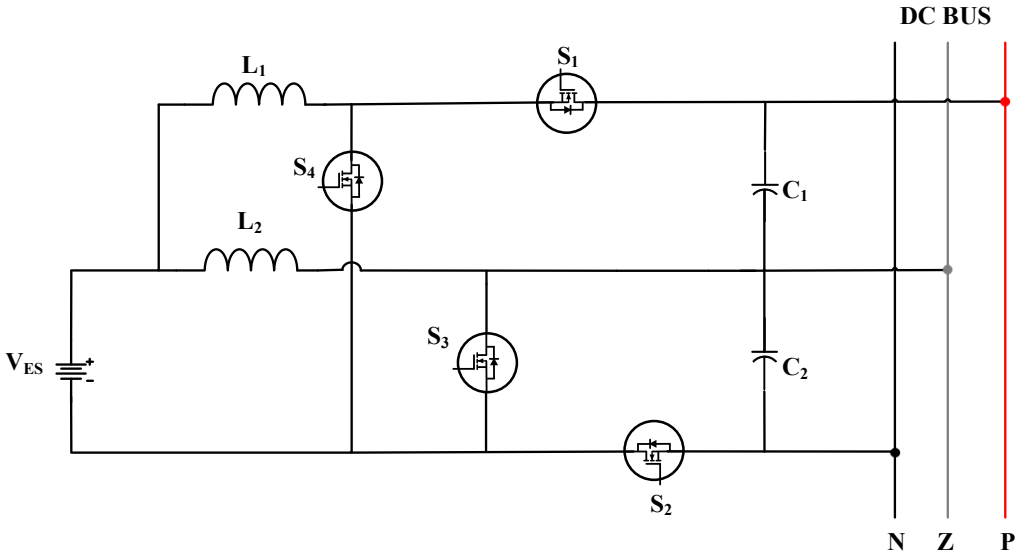

Fig. 3.19 Bidirectional modified SEPIC-cuk DC–DC converter

3.4.3 Boost and Buck Boost Derived Bipolar DC-DC Converter Topologies

The Boost and Buck-Boost derived bipolar DC-DC converter topologies with single and multi-switch configuration as follows:

1. This converter's architecture uses boost and buck-boost converters using a shared inductor to enable voltage balancing as well as a common-ground condition. making it appropriate for low-voltage bipolar DC systems.

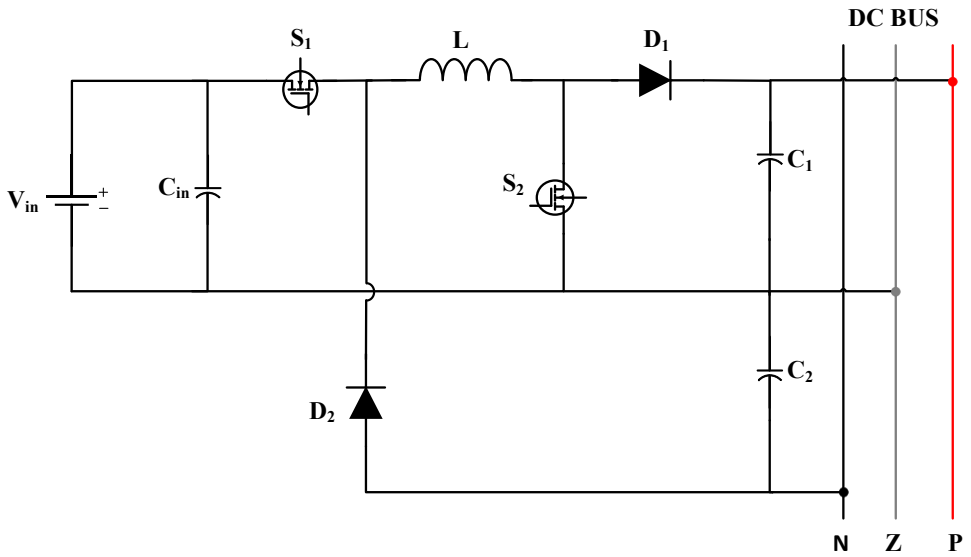

Fig. 3.20 Circuit diagram of Bi-Polar Boost Derived Interleaved DC-DC converter

2. Here, boost-luo interleaved DC-DC converter for low voltage bi-polar DC microgrid. presented converter integrates boost and negative Luo topologies. When compared to traditional converters of the same rating, the interleaving approach offers the advantages of lower current stress and less source current ripple. The converter that is being presented offers interleaving advantages in addition to multiple output voltage levels.

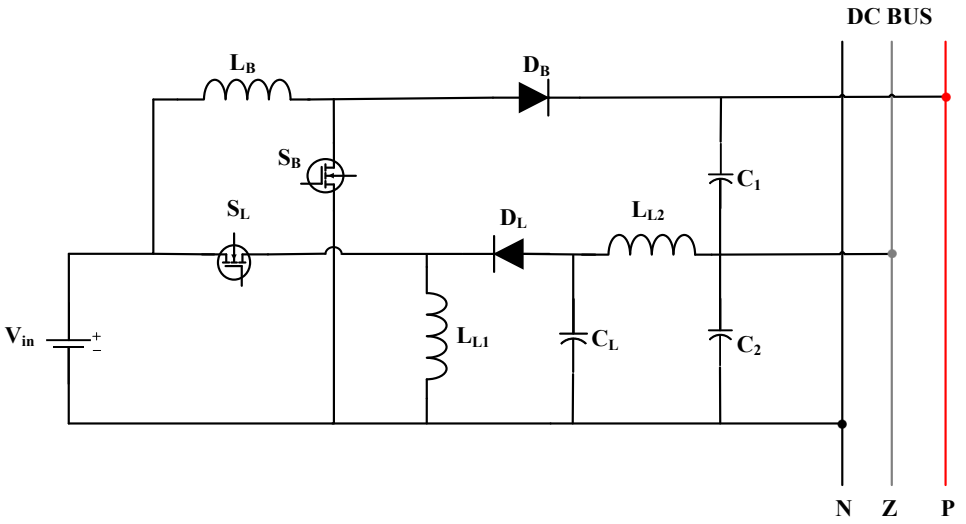

Fig. 3.21 Circuit diagram of Boost-Luo interleaved DC-DC converter

3.4.4 Buck and Buck Boost Derived Bipolar DC-DC Converter Topologies

The Buck and Buck-Boost derived bipolar DC-DC converter topologies with single and multi-switch configuration as follows:

1. A DC-DC converter based on buck and buck/boost structures is presented here. The output of both circuits, buck and buck-boost, adjusts swiftly to variations in duty cycles.

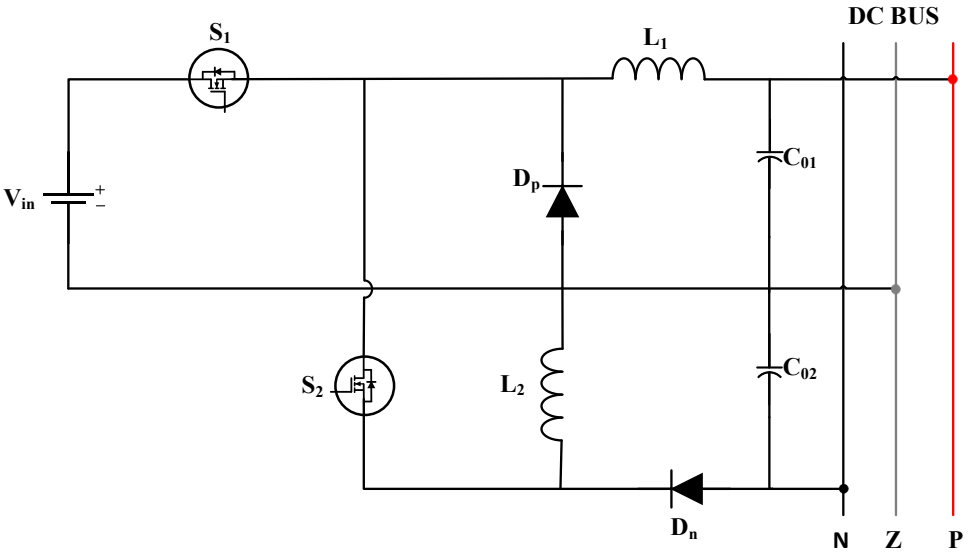

Fig. 3.22 Circuit diagram of Buck Buck-Boost interleaved DC-DC converter

3.5 Load Connection in Bipolar DC System

In order to support the networks' voltage balance, several different topologies with connected loads have been presented for use in the bipolar microgrid:

1. The bipolar DC system's three-level DC–DC buck converter topology for load connection keeps network voltage balance.

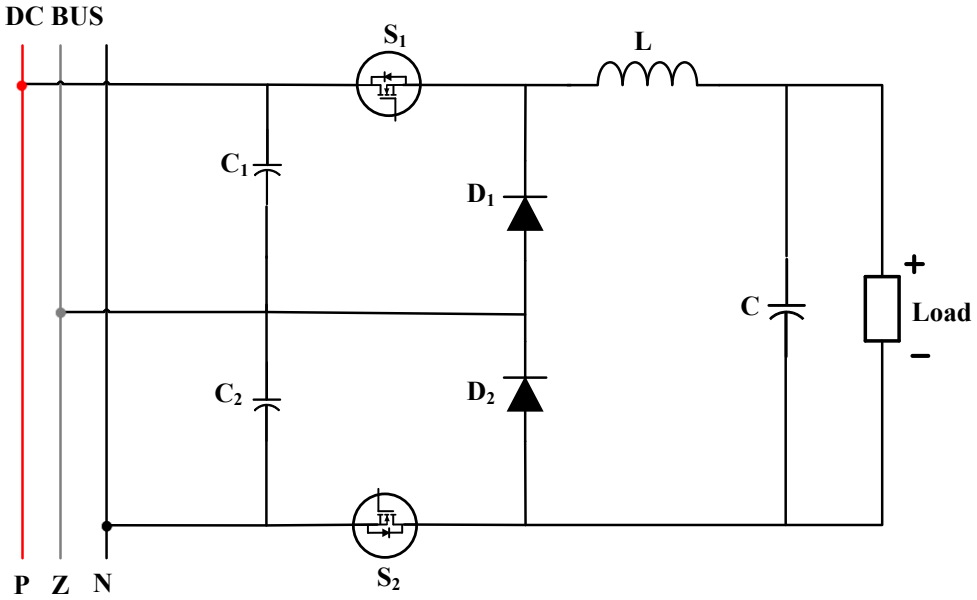

Fig. 3.23 Circuit diagram of three-level buck converter's load Connection in bipolar system

2. The bipolar DC system's three-level DC–DC boost converter topology for load connection to maintain network voltage balance.

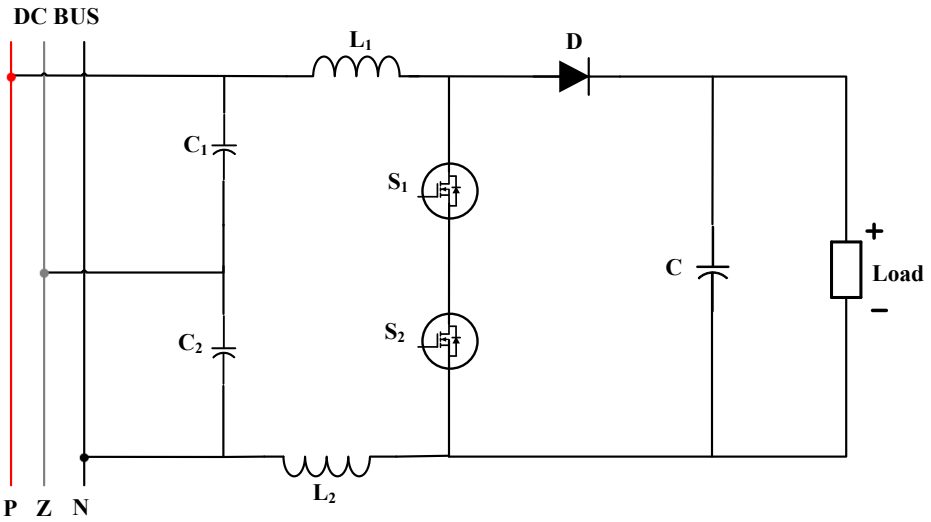

Fig. 3.24 Circuit diagram of three-level boost converter's load Connection in bipolar system

3. The bipolar DC system's three-level DC–DC boost converter topology for load connection to maintain network voltage balance.

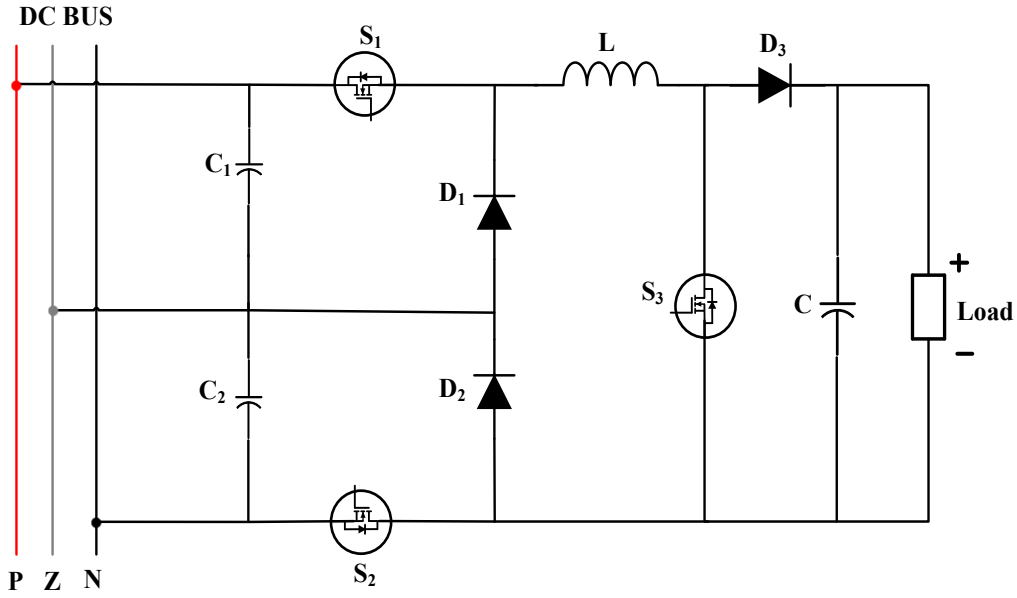

Fig. 3.25 Circuit diagram of three-level boost converter's load Connection in bipolar system

3.6 Conclusion

In this chapter 3, concludes classification of bipolar DC system, connection configuration in bipolar system, and different DC-DC converters derived topologies. The classification is based on the topology and connection configuration respectively.

CHAPTER 4

DESIGN DEVELOPMENT AND ANALYSIS OF BI-POLAR BOOST DERIVED INTERLEAVED DC-DC CONVERTER

4.1 General Aspect

This chapter explores the design and analysis of presented single input dual output Boost Buck-Boost (SIDO BBB) converter which includes state-space analysis, design, implementation of Time multiplexed control scheme and simulation analysis of the presented converter.

4.2 Schematic of Bi-Polar Boost Derived Interleaved DC-DC Converter

The circuit configuration of Boost Buck-Boost DC-DC converter with DC bus and the bipolar output configuration respectively.

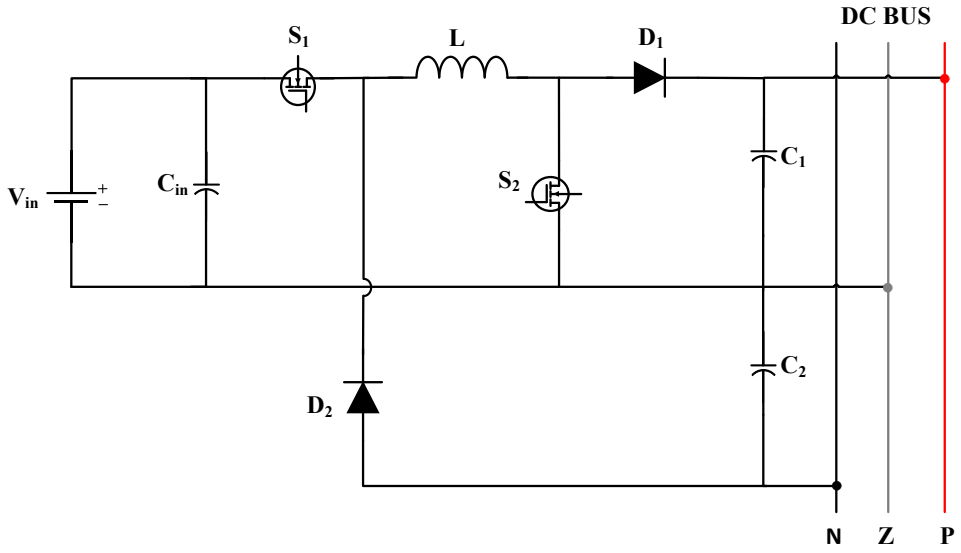

Fig. 4.1 Circuit diagram of Bi-Polar Boost Derived Interleaved DC-DC Converter

4.3 Modes of Operation

For analysis, resistive load is taken, The SIDO BBB converter is a 4^{Th} order, non-isolated consisting of one inductor, one input capacitor and two output capacitors, two diodes, and two switches as shown in Figure. The SIDO BBB converter can operate in

two different modes: boost and buck boost. Boost and buck-boost converters operate sequentially throughout each operating cycle, respectively, in this respect.

Boost Mode ($t_0 < t < T/2$)

Mode 1: State 1, ON state, [t_0–t_1]: As S_1 and S_2 turn on, inductor begins to be magnetized by the input voltage source's energy. From its lowest value of ILmin1 to its maximum value of I_{Lmax1}, the inductor current rises linearly. In this state, D_1 and D_2 aren't in operation.

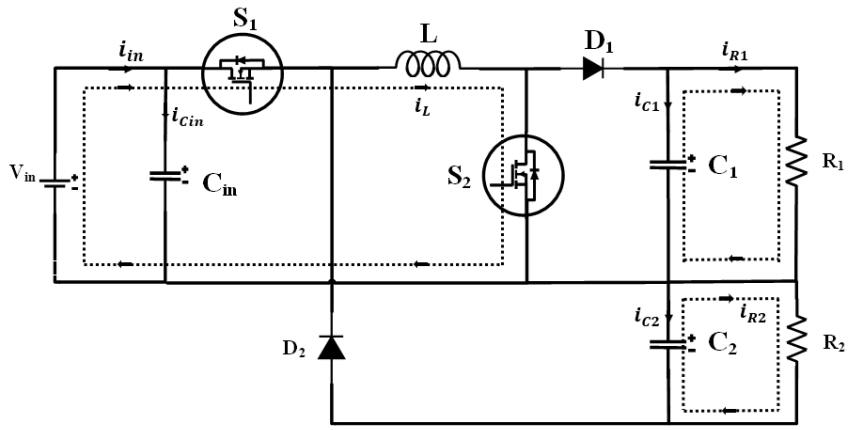

Fig. 4.2 Mode 1 of Operation

Mode 2: OFF state, [t_1–t_2]: While S_2 and D_2 are OFF, S_1 and D_1 are ON. The output capacitor C_1 is entirely energized by inductor's magnetized energy passing through D_1.

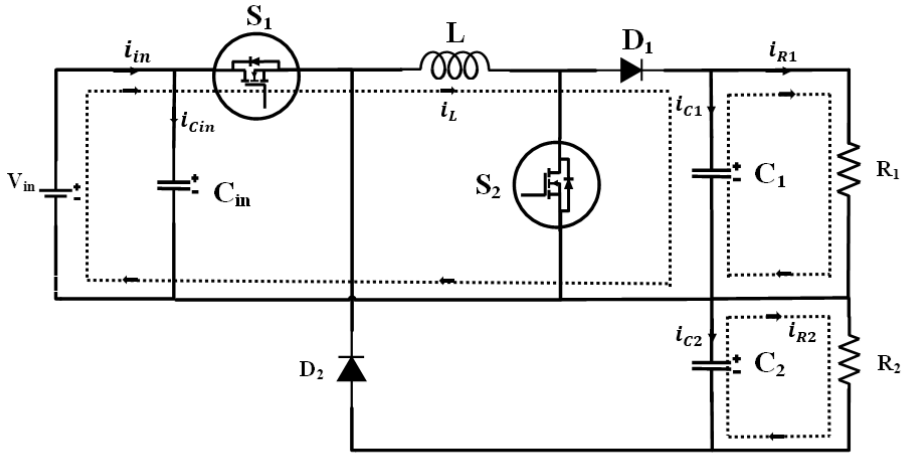

Fig. 4.3 Mode 2 of Operation

Buck-boost mode

Mode 3: (T/2 < t < T): S_1 and S_2 are ON, whereas D1 and D_2 are OFF in State 3, ON state, [t_3–t_4]. The inductor becomes magnetized by the input source's energy.

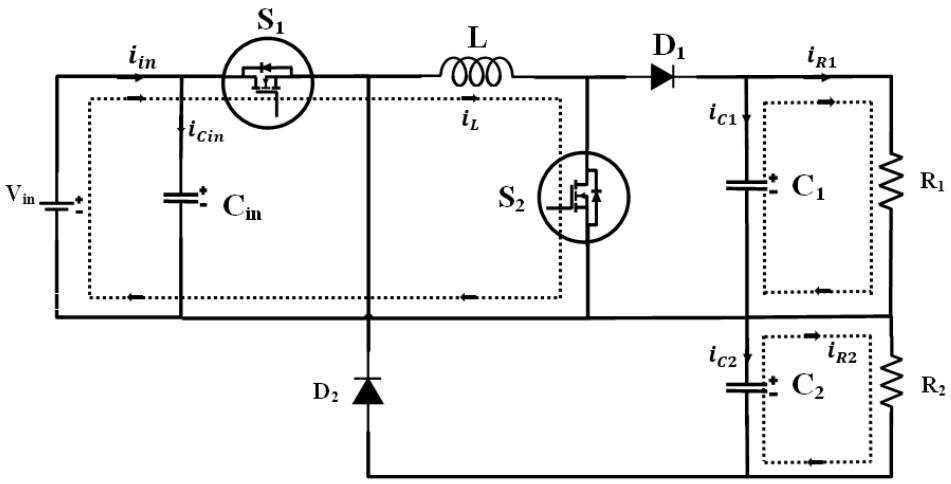

Fig. 4.4 Mode 3 of Operation

Mode 4:

State 4, OFF state, [t4–t5]: When S_1 and D_1 are off, S_2 and D_2 are on. The output capacitor C_2 is entirely energized by the inductor's magnetized energy.

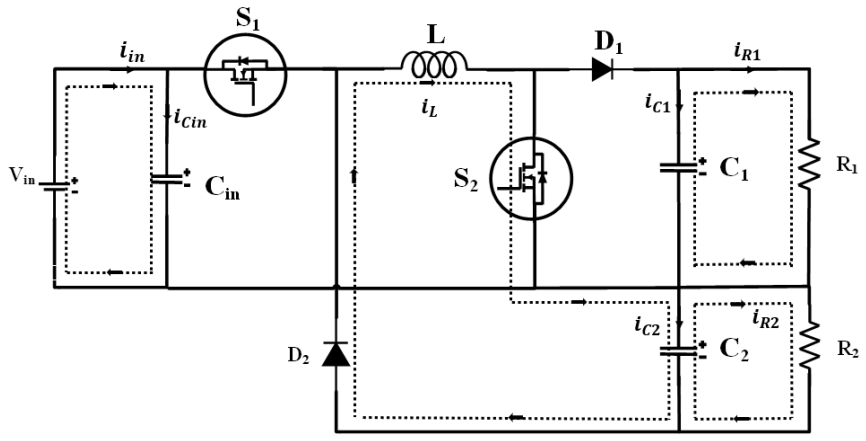

Fig. 4.5 Mode 4 of Operation

4.4 Modelling of Bi-Polar Boost Derived Interleaved DC-DC Converter

State-space Analysis:

State-space averaging is a powerful method for analysing the dynamic behaviour of DC-DC converters. It involves representing the converter in a state-space form, which provides a mathematical framework to study its time-domain response, stability, and control system design.

The process of applying small signal analysis to the presented converter involves several steps:

- Identifying the Operating Point: The first step necessitates determining the steady-state

  or the quiescent point, around which the system's behaviour will be analysed.

- b) Derivation of State Space Model: The second step involves the derivation of the state

  space model involves translating its circuit equations into a matrix form that

  encapsulates the system's inherent dynamics.

- c) State Space Averaging: This approach results in a linear, time-invariant model that

  accurately describes the dynamic behaviour of the converter, simplifying the analysis.

The converter's small-signal behaviour is analysed by deriving the state space from the circuit equations. The following equations define the output voltage as the output variable, the input voltage as the controlled input variable, the inductor current and capacitor voltages as state variables, and the output voltage as the output variable.

$$X = \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} \tag{4.1}$$

And here, $u = [V_{\text{in}}]$, $y = [V_{\text{outputs}}]$;

$$\dot{x} = Ax + Bu \tag{4.2}$$

$$y = Cx + Eu \tag{4.3}$$

Mode 1: State space equations of SIDO BBB in mode 1 is as follows:

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{4.4}$$

$$\frac{dVc_{in}}{dt} = \frac{i_{in} - i_L}{c} \tag{4.5}$$

$$\frac{dVc_1}{dt} = \frac{-i_{R1}}{c_1} \tag{4.6}$$

$$\frac{dVc_2}{dt} = \frac{-i_{R2}}{c_2} + \frac{-i_{R1}}{c_1} \tag{4.7}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dVc_{in}}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{c} \\ 0 & \frac{-1}{c_1 R_1} & 0 & 0 \\ 0 & 0 & \frac{-1}{c_2 R_2} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \begin{bmatrix} 0 \\ \frac{1}{C} \\ 0 \\ 0 \end{bmatrix} i_{in} \tag{4.8}$$

$$\begin{bmatrix} V_{01} \\ V_{02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} i_{in} \tag{4.9}$$

Mode 2: The state space equations of SIDO BBB converter in mode 2 is given by:

$$\frac{di_L}{dt} = \frac{V_{in-}V_{C1}}{L} \tag{4.10}$$

Mode 3: The state space equations of SIDO BBB converter in mode 3 is given by:

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{4.11}$$

$$\frac{dVc_{in}}{dt} = \frac{i_{in} - i_L}{c} \tag{4.12}$$

$$\frac{dVc_1}{dt} = \frac{-i_{R1}}{c_1} \tag{4.13}$$

$$\frac{dVc_2}{dt} = \frac{-i_{R2}}{c_2} + \frac{-i_{R1}}{c_1} \tag{4.14}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dVc_{in}}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{c} \\ 0 & \frac{-1}{c_1R_1} & 0 & 0 \\ 0 & 0 & \frac{-1}{c_2R_2} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \begin{bmatrix} 0 \\ \frac{1}{C} \\ 0 \\ 0 \end{bmatrix} i_{in} \tag{4.15}$$

$$\begin{bmatrix} V_{01} \\ V_{02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} i_{in} \tag{4.16}$$

Mode 4: The state space equations of SIDO BBB converter in mode 4 is given by:

$$\frac{di_L}{dt} = -\frac{V_{C_2}}{L} \tag{4.17}$$

$$\frac{dVc_{in}}{dt} = \frac{i_{in}}{c_{in}} \tag{4.18}$$

$$\frac{dVc_1}{dt} = \frac{V_{C_1}}{R_1c_1} \tag{4.19}$$

$$\frac{dVc_2}{dt} = \frac{i_L + \left(i_{R_1} - i_{R_2}\right)}{c_2} \tag{4.20}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dVc_{in}}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{c_1R_1} & 0 \\ \frac{1}{c_2} & 0 & \frac{1}{c_1R_1} & \frac{-1}{c_2R_2} \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \begin{bmatrix} 0 \\ \frac{1}{C} \\ 0 \\ 0 \end{bmatrix} i_{in} \tag{4.21}$$

$$\begin{bmatrix} V_{01} \\ V_{02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ Vc_{in} \\ Vc_1 \\ Vc_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} i_{in} \tag{4.22}$$

The ratio of the switch-ON time to the total switching period is known as the duty cycle (D). Using the following formula, it determines the output voltage (Vo) in relation to the input voltage (Vs).:

$$V_{01} = \frac{V_{in}}{1 - d_2} \tag{4.23}$$

$$V_{02} = \frac{V_{in} d_1}{1 - d_1} \tag{4.24}$$

When d_1 and d_2 are equal, the converter's voltage can be balanced during the integrated boost-buck-boost method. The aggregate voltage gain in this instance is estimated by

In CCM operation, the proposed SI-SIDO converter's voltage gain is the sum of the voltage gains in boost (M1) and buck-boost (M2) modes. This is the definition of the overall voltage gain as follows:

$$M = \frac{1 - d_1 d_2}{(1 - d_1)(1 - d_2)} \tag{4.25}$$

The desired ripple current (ΔiL) and the switching frequency (fsw) are employed to calculate the inductor value (L). The inductor values are calculated using the following equations:

$$L = \left\{ \begin{matrix} \frac{V_{in} d_2}{\triangle\, i_L * f_{sw}} = \frac{(V_{01} - V_{in})(1 - d_2)}{\triangle\, i_L * f_{sw}} \\ \frac{V_{in} d_1}{\triangle\, i_L * f_{sw}} = \frac{V_{02}(1 - d_1)}{\triangle\, i_L * f_{sw}} \end{matrix} \right\} \tag{4.26}$$

4.5 Design Specification:

TABLE 4.1 Design Specification of Presented Converter

Parameters	Symbol	Values
Input Voltage	V_{in}	50 V
Output Voltages	V_{02}, V_{01}	75.44, 75.23 V
Duty Cycles for (S_1, S_2)	d_1, d_2	0.606, 0.35
Input Capacitor	C_{in}	1500 μF
Inductor	L	400 μH
Current Ripple in Inductor (L)	$\triangle i_L$	10% of I_L
Switching Frequency	f_{sw}	50 kHz
Output Capacitors	C_1, C_2	1500 μF
Input current	i_{in}	3.9 A
Load Resistances (R_1, R_2)	R_1, R_2	85 Ω
Time Sharing Factor	TSF	20 ms

Here, the required switching pulses are provided by a simple open loop control strategy that is based on preset duty cycles.

4.6 Control Scheme

For a suitable converter, a time-multiplexed control scheme is created to independently charge two output capacitors while offering varying voltage levels for different requirements.

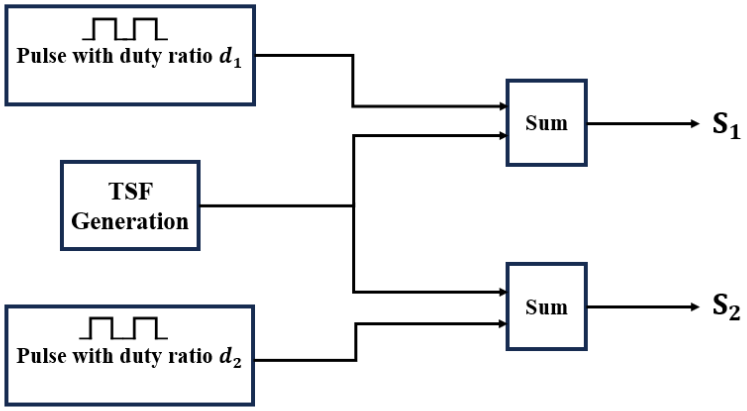

Fig. 4.6 Block diagram of the presented Time Multiplexing Control Scheme

The presented converter work by alternating between the boost and buck-boost converters. To split the boost's and the boost's operation cycles buck–boost converters, a TSF is employed.

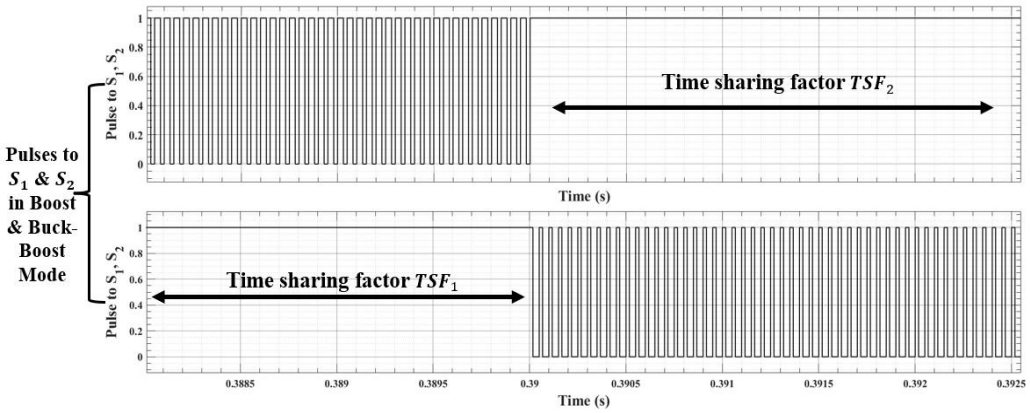

Fig. 4.7 Time Sharing Factor for S_1 and S_2

The circuit implementation for the time multiplexed control is operated on MATLAB Simulink. TSF1 is from [t_0, T/2] and TSF2 is [T/2, T]. Boost & buck–boost modes

working during first (TSF1), next (TSF2) interval. Here both TSF's are equal i.e. TSF1 and TSF2 are 0.01 s.

Moreover, two duty cycles (d_1 and d_2) have been set for the S_1 and S_2's high switching frequency (fsw) modes. To deal with the sharing issue, the TMC scheme uses TSF_1

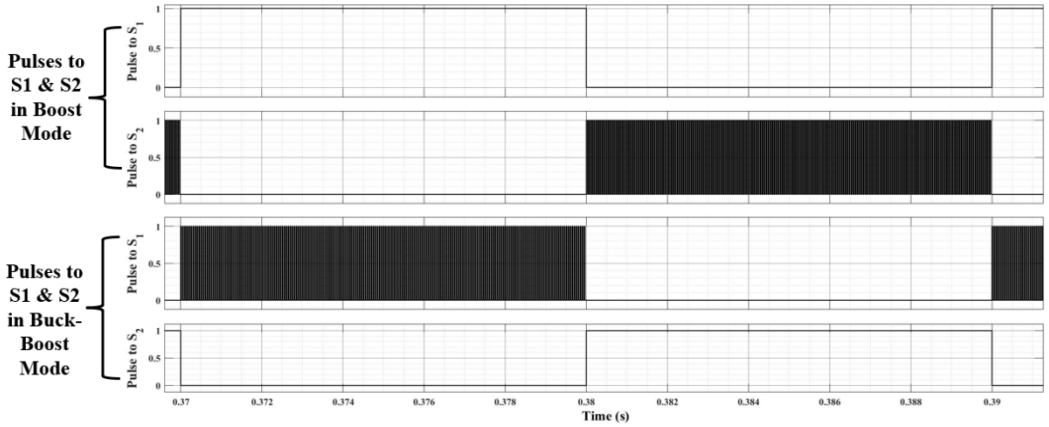

Fig. 4.8 Pulses to Switches

The inductor current's charge and discharge triangle is formed during TSF_1 and TSF_2, due to the short time period T (TSF). The inductor current's charging and discharging times during a single period T are equal to T/2 since $TSF_1 = TSF_2$. The converter's boost and buck-boost modes combine when conduction time ($TSF= TSF_1 + TSF_2$) is much less than 20 ms.

This work shows how a Bi-Polar Boost Buck-Boost DC-DC converter with time-multiplexed control can operate by sending pulses to switches. Number of full pulsating cycles that every cycle endures during time T can be employed to estimate number of conduction period for boost and buck-boost. As an outcome, each mode's operating cycle count can be represented as:

$$N_{\text{operating-cycles}} = \frac{T}{2T_{SW}} = \frac{TSF_1}{T_{SW}} = \frac{TSF_2}{T_{SW}} \tag{4.27}$$

Buck-boost and boost operation modes are specified for S_1 and S_2 by determining the duty-cycles of d_1 and d_2. Additionally, the switching scheme with TSF = 20 ms was presented. The results of the SIDO BBB converter simulation in MATLAB/Simulink are laid out in this chapter as follows.:

4.7 Results and Discussion

This section illustrates the SIDO BBB converter's simulation results for CCM operations. MATLAB/Simulink was used to design and model the converter; the simulation's outcomes are displayed. To provide CCM operating conditions for the resistive load range of 85 Ω, a switching frequency of 30 kHz was chosen. 50V, 20 ms, 400 μH, and 1500 μF are input voltage, TSF, inductor, and output capacitors, in that order. The converter's performance during CCM operation is demonstrated using output loads of 85 Ω. Additionally, the pulsating control has TSF = 20 ms it was presented.

4.7.1 Input Current and Inductor Current:

Time period T integrated during the integrated boost buck-boost method is significantly less than T individual. Here, inductor current is charged and discharged through boost and buck-boost operation modes. Converter's inductor current in charging mode is equal to and balanced with the discharging mode because TSF1=TSF2=T integrated/2. It is evident that the inductor current ripple be lowered by using a larger inductor and a larger switching frequency.

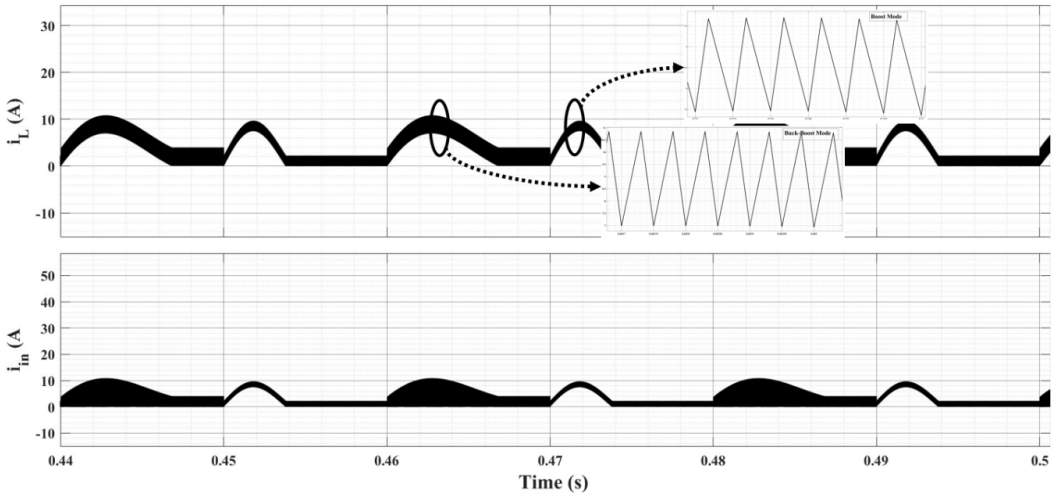

Fig. 4.9 Inductor current and Input current waveforms

The input current ripple's waveform follows that of the inductor current ripple. On the other hand, presented converter's input capacitor reduces high-frequency ripples in input current waveform and ensures a constant input current. Therefore, input current ripple ranges from 70% to 90% of inductor current ripple, depending on the size of input capacitor.

To avoid inductor saturation, the buck-boost mode inductor can be used in each of boost and buck-boost modes of presented converter. Because DC-link output capacitors are charged independently throughout the two independent operation modes, voltage balancing condition is provided even when the output loads are unbalanced.

4.7.2 Output Current and Voltage of SIDO BBB converter:

Here, the output current i.e. of positive, negative, and neutral can be observed. The output current having same amplitude but having different polarities and neutral current fluctuates between positive and negative respectively.

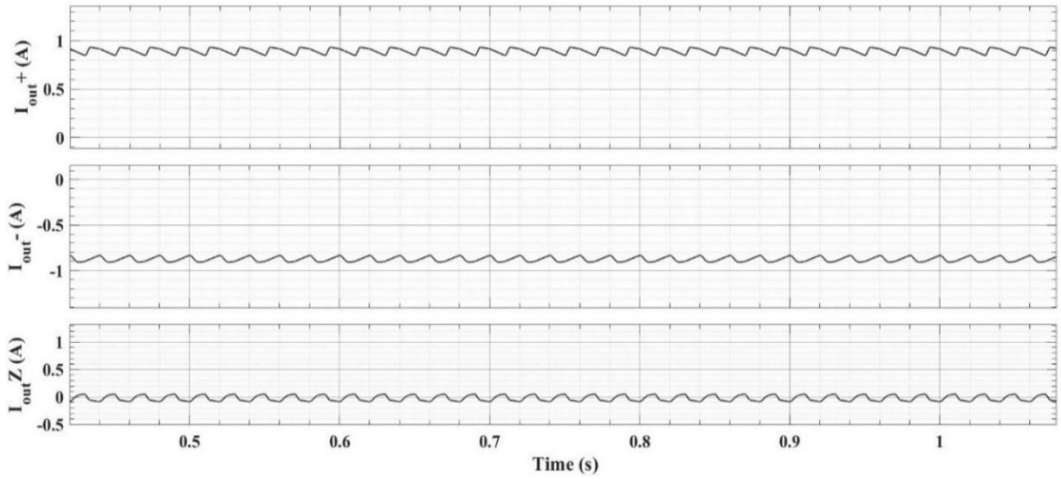

Fig. 4.10 Output current waveforms

For the dc-link voltage balancing to function, the converter must operate in either continuous or partly continuous operation [CCM + boundary conduction mode (BCM)] while the load varies. Therefore, a suitable switching frequency must be chosen to guarantee the CCM working mode for a specific range of loads.

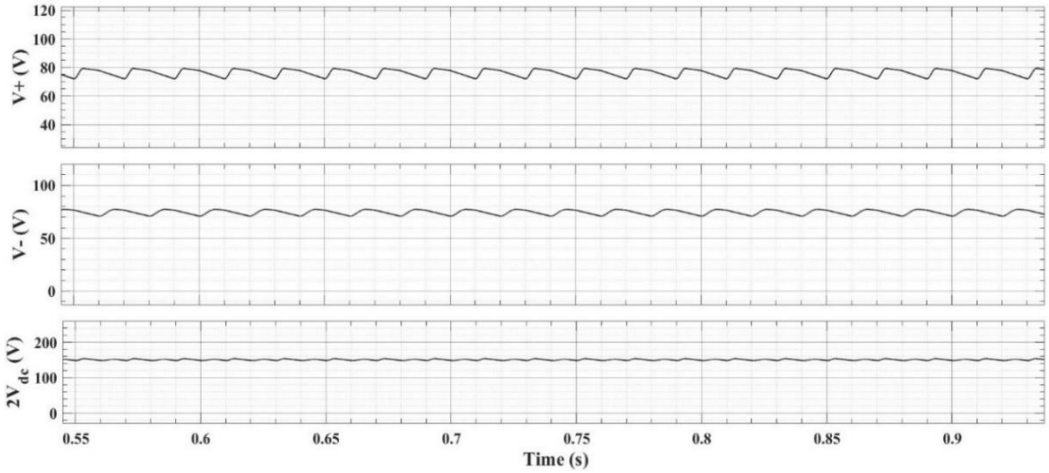

Fig. 4.11 Output Voltage waveforms

When d_1 and d_2 are equal, the total output voltage gains of the two operating techniques are equal, but the voltage balancing condition only happens during combined boost-buck-boost operating method.

4.8 Conclusion

The theoretical analysis and simulation results investigated in this study. The power density and efficiency of the converter improved through the inclusion of a single inductor in the structure of the SIDO BBB converter topology which was presented. In a bipolar LVDC system, the DC-DC converter that is being presented may be beneficial in helping of regulating the voltage. One inductor, one input capacitor, two output capacitors, two diodes, and two switches with less circuit elements make up the 4th order, non-isolated converter that is being presented. In this situation, the inherited voltage balancing capability is appropriate for applications that require a bipolar dc-link feeder. The suggested converter operated far better because it only used one inductor in a simple layout, that reduced the converter's size and weight.

For suggested converter, a TMC control is created to independently charge two output capacitors and supply varying voltage levels for various needs. Converter's voltage was balanced within a specified load range using open loop control technique. The suggested converter could supply power to the 3L-NPC inverters' dc-link capacitors. The resistive load's CCM conditions for operation are defined by the 50 kHz switching frequency.

CHAPTER 5

DESIGN DEVELOPMENT AND ANALYSIS OF BOOST-LUO INTERLEAVED DC-DC CONVERTER

5.1 General Aspect

Here, a single input dual output (SIDO) non-isolated boost-luo (NBLI) type DC-DC converter is presented. This topology is appropriate for low voltage bi-polar DC microgrid (LVBDCM)applications and renewable power sources such as fuel cells and solar PV. In NBLI converter, the two outputs are designated for the Boost and Luo converter, respectively. Presented converter have steady source current with nominal ripples because of the implementation of interleaving technique along with considerable high gain. Objective of the presented converter is to increase the power handling capacity by creating multi ports at the output and provide high gain.

5.2 Schematic of Boost-Luo Interleaved Converter

The presented converter integrates boost and negative Luo topologies. When compared to traditional converters of the same rating, the interleaving approach offers the advantages of lower current stress and less source current ripple.

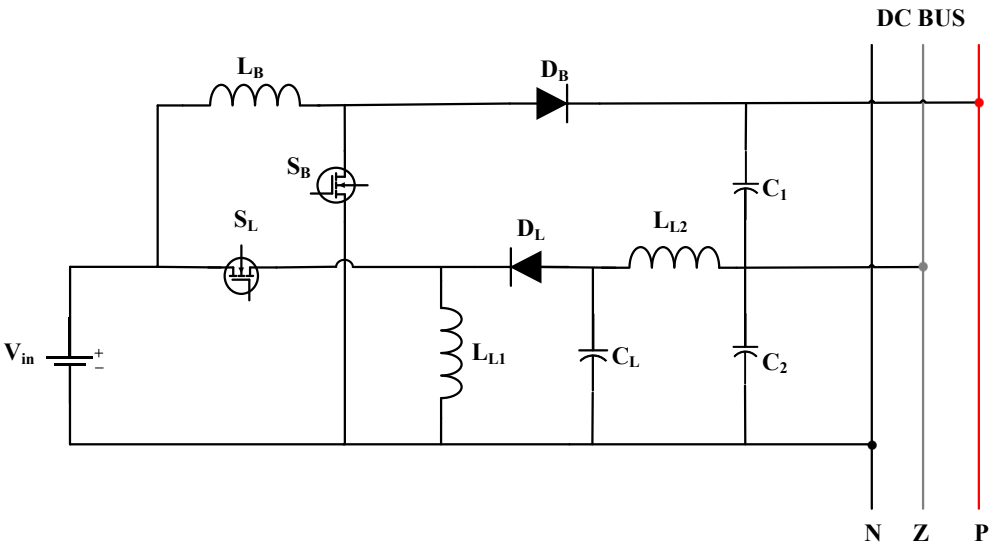

Fig. 5.1 Circuit diagram of Boost-Luo interleaved DC-DC converter

Here, circuit configuration is with DC bus connection. The converter that is being presented offers interleaving advantages in addition to multiple output voltage levels. In this regard, a NBLI converter is presented here. For a variety of applications, the converter can provide balanced or non-balanced output voltages, keeping output voltages steady even when loads are not balanced. On account of its voltage balancing capability, presented converter delivers DC-link voltage stabilization for bipolar low-voltage applications DC (LVDC) distribution systems. This work comprises presented converter's designing, modelling and output voltage control. The efficacy of the presented system is verified in MATLAB/Simulink.

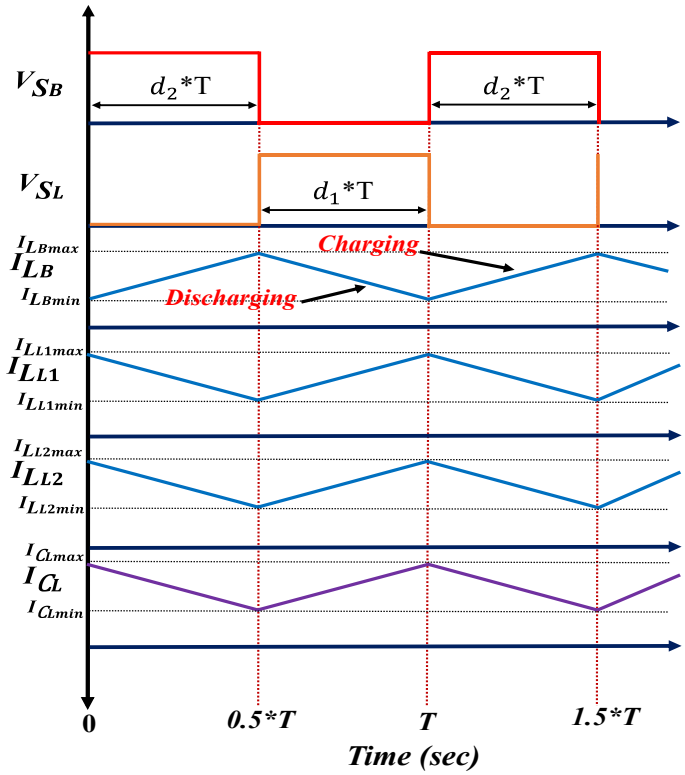

Fig. 5.2 Steady state waveform of SIDO NBLI converter in CCM

The schematic representation for the NBLI DC-DC converter is shown in Fig. 2, which also shows the presented DC-DC converter configuration. 48V bus is linked to Boost converter's output, while 24V bus is linked to the Luo converter's output. Topology that is being presented combines a SIDO configuration with interleaving Boost-Luo converters. The input and output sides of the switching cells are connected in parallel and series, respectively. In the two-phase scenario, pulses for switching are delivered to S_L and S_B in an interleaved manner, means they are 180° degrees apart. When S_L is

operating the S_B will be off and vice versa. V_{in} refers to voltage of input source; in this case, a battery is employed, and its voltage can range from 16 to 26 V. V_o is the overall DC bus voltage following by V_1, V_2 are the Boost and Luo output voltages. The Boost side boasts a load resistor R_{L1}, diode D_B, active switch S_B, and inductor L_B. The Luo side includes load resistor R_{L2}, diode D_L, capacitors C_2, C_L, active switch S_L, and inductors L_{L1} and L_{L2}. As RESs can have low voltages between 18 and 26 V, negative Luo converter is selected to interconnect with 24 V buses and a Boost to interconnect with 48 V buses. Luo converter is interleaved with Boost converter for its advantages, like low output voltage ripple, provides high efficiency and voltage gain with low conduction losses. In order to ensure CCM, the inductors are purposefully designed. Filter capacitors, resistive load linked within ports P-Z and Z-N as C_1, R_{L1} and C_2, R_{L2} respectively. Here, P-Z and Z-N are the poles i.e. positive (P), negative (N), neutral (Z) respectively.

5.3 Modes of Operation

Here, NBLI DC-DC converter's operating modes and a steady-state analysis of the converter in continuous conduction mode (CCM) are employed in this section. Ideal and lossless power components are assumed; parasitic components are not taken into account, and both converters have equal inductance and output capacitances values. Four CCM modes are presented based on the switching functions of S_B and S_L switches. These modes are represented in Table 1 as follows:

TABLE 5.1 Conducting States of SIDO NBLI Converter

Conducting States $S_{B\&}S_L$	**Modes**	L_B	L_{L1}	L_{L2}	C_L	C_1	C_2
00	Passive Mode 1	D	D	D	C	C	C
01	Active Mode 1	D	C	D	D	C	C
10	Active Mode 2	C	D	C	C	D	D
11	Passive Mode 2	C	C	C	D	D	D

- C- Charging, D- Discharging.

Representing voltage gains for CCM operation as per Fig. 2 are expressed as:

$$V_2 = \frac{V_{in} * d_1}{(1-d_1)} \tag{5.1}$$

$$V_0 = V_1 + V_2 = V_{in} \frac{1}{(1-d_2)} \tag{5.2}$$

here d_1, d_2 indicates duty cycles of switches S_L and S_B respectively.

$$M_B = \frac{V_0}{V_{in}} = \frac{1}{(1-d_2)} \tag{5.3}$$

$$M_L = \frac{V_2}{V_{in}} = \frac{d_1}{(1-d_1)} \tag{5.4}$$

M_B and M_L are gain of voltage for NBLI's Boost and Luo converters and V_{in} is source voltage respectively in CCM. Here, V_{C1} and V_{C2} are equal to V_1 and V_2.

(1) Passive Mode 1: When S_L and S_B gated voltages are low, this mode starts. When neither of the active switches are conducting. R_{L1} is supplied with input source and L_b. L_{L1} will use its stored energy to charge C_L, and L_{L2} will release its energy to R_{L2}. Fig. 3 represents the circuit that goes with this mode.

$$V_{LB} = V_{in} - V_{C1} + V_{CL} - V_{C2} - V_{CL} \tag{5.5}$$

$$V_{LL1} = V_{CL} \tag{5.6}$$

$$V_{LL2} = V_{CL} - V_{C2} \tag{5.7}$$

$$V_0 = V_{C1} + V_{C2} \tag{5.8}$$

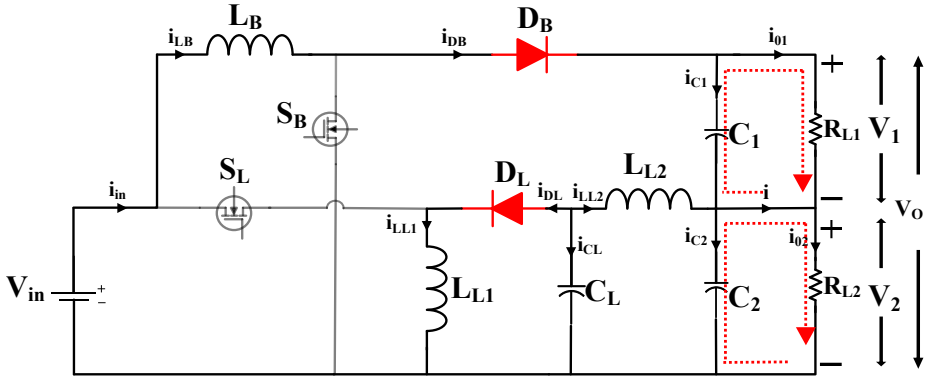

Fig. 5.3 Passive mode 1

(2) Active Mode 1: For S_L, mode starts when the pulse for gating is low, and switch S_B, it is high. S_L is conducting when switch S_B is not conducting. Luo and Boost section share the input current. Supply input is charging L_{L1}, L_{L2} is discharging.

Connected load (R_{L1}) is receiving energy from L_B in the Boost section. Fig. 4 represents circuit with this mode.

$$V_{LB} = V_{in} - V_{C1} + V_{LL2} - V_{CL} \tag{5.9}$$

$$V_{LL1} = V_{in} \tag{5.10}$$

$$V_{LL2} = V_{CL} - V_{C2} \tag{5.11}$$

$$V_0 = V_{C1} + V_{C2} \tag{5.12}$$

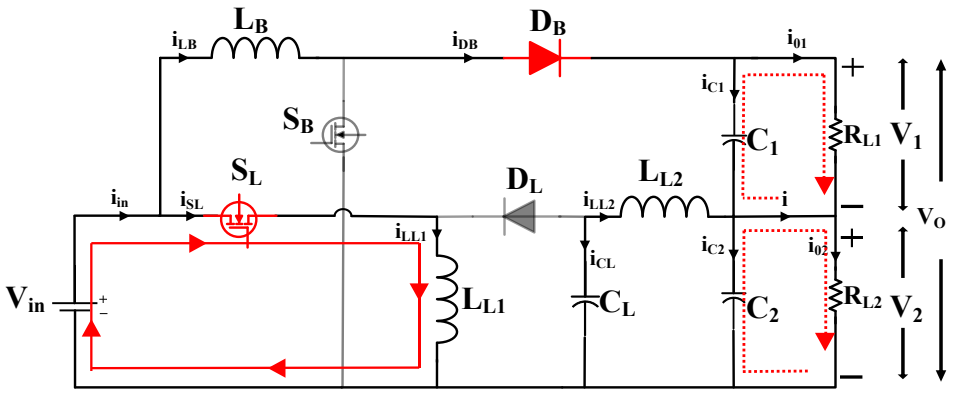

Fig. 5.4 Active mode 1

(3) Active Mode 2: When the gated voltage is high for S_B and low for S_L, this mode starts. S_B conducts as switch S_L aren't conducting. L_B is being charged by the input source, and C_1 discharges to load R_{L1}. L_{L2} is charging, L_{L1} is discharging through diode D_L. Fig. 5 depicts the circuit that goes with this mode.

$$V_{LB} = V_{in} \tag{5.13}$$

$$V_{LL1} = V_{CL} \tag{5.14}$$

$$V_{LL2} = V_{CL} - V_{C2} \tag{5.15}$$

$$V_0 = V_{C1} + V_{C2} \tag{5.16}$$

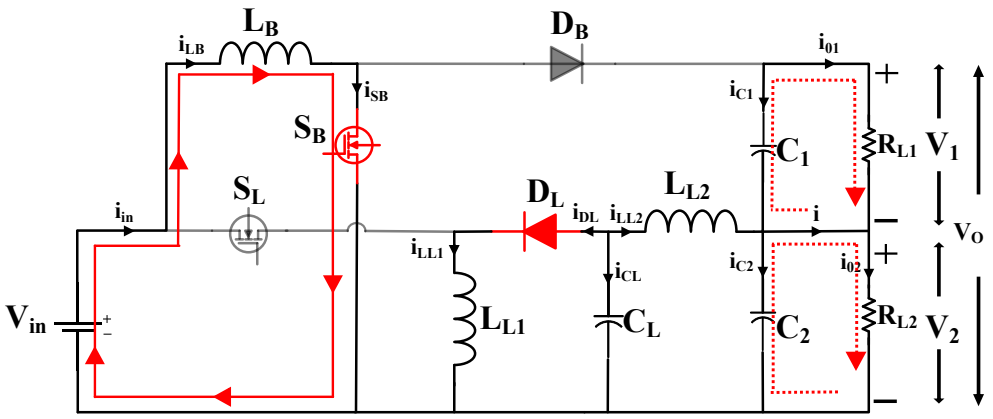

Fig. 5.5 Active mode 2

(4) Passive Mode 2: When gated voltages for S_L and SB are conducting, this mode starts. L_B and L_{L1} are being charged by the input source. C_L in the boost section provides the energy needed to load R_{L1}. In the Luo section, C_2 discharges and provides power to load R_{L2}. Fig. 6 displays the circuit that corresponds to this mode.

$$V_{LB} = V_{in} \tag{5.17}$$

$$V_{LL1} = V_{in} \tag{5.18}$$

$$V_{LL2} = V_{CL} - V_{C2} \tag{5.19}$$

$$V_0 = V_{C1} + V_{C2} \tag{5.20}$$

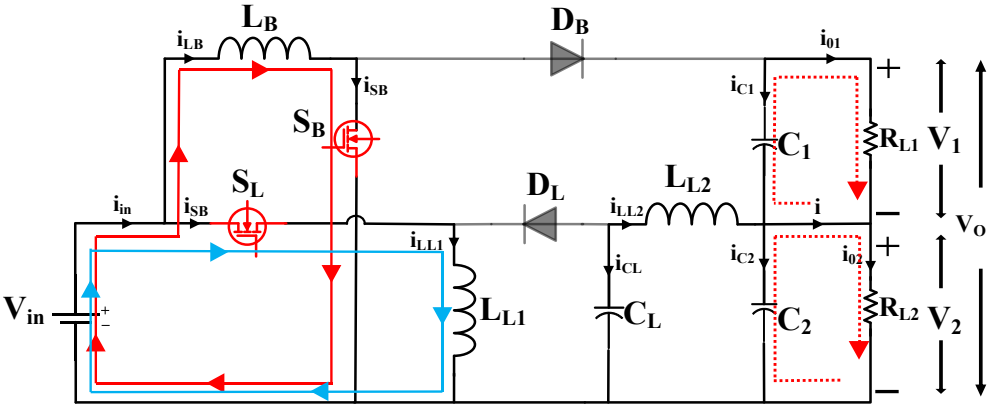

Fig. 5.6 Passive mode 2

5.4 Modelling of Boost-Luo Interleaved DC-DC Converter

This section comprises of the dynamic modelling and control implementation strategy for NBLI converter.

SIDO NBLI converter offers two operational modes. In the case of CCM, duty cycle regulation is employed to govern the input current and inductor currents at the input side. Corresponding dynamic model needs to be acquired in order to operate converter in each of the modes. Employs the state-space averaging method for getting converter's dynamic model. By taking into account a slight variation in the state variables (i_{LB}, V_1 for Boost, i_{LL1}, i_{LL2}, V_{CL}, V_2 for Luo) and duty cycles (d_1, d_2) of each section of converter, small signal analysis is carried out to produce a linearized AC model around a DC operation point as follows:

$$i_{Lm} = I_{Lm} + \hat{i}_{Lm} \tag{5.27}$$

$$v_{Cm} = V_{Cm} + \hat{v}_{Cm} \tag{5.28}$$

$$d_m = D_m + \hat{d}_m \tag{5.29}$$

In this case, m = b, L which is notation for Boost (b) and Luo (L) converter's representation. I_{Lm}, v_{Cm}, d_m are the current, voltage and duty cycle of NBLI converter which are subjected into perturbation for obtaining AC and DC model. In Eq. (30)-(35), A_m, B_m, C_m are average state space matrices for Boost and Luo converter, where A_m, B_m i.e. (A_{1m}, B_{1m}, A_{2m}, B_{2m}) are state and input matrix for active mode 1, 2.

$$A_b = A_{1b} \times d_2 + A_{2b} \times (1 - d_2) \tag{5.30}$$

$$B_b = B_{1b} \times d_2 + B_{2b} \times (1 - d_2) \tag{5.31}$$

$$C_b = C_{1b} \times d_2 + C_{2b} \times (1 - d_2) \tag{5.32}$$

$$A_L = A_{1L} \times d_1 + A_{2L} \times (1 - d_1) \tag{5.33}$$

$$B_L = B_{1L} \times d_1 + B_{2L} \times (1 - d_1) \tag{5.34}$$

$$C_L = C_{1L} \times d_1 + C_{2L} \times (1 - d_1) \tag{5.35}$$

The state vector X_m, in which m = b, L where, m representing Boost and Luo respectively. Here, steady state values of state vector are provided as follows:

$$X_b = \begin{bmatrix} I_{Lb} \\ V_O \end{bmatrix} = -A_b^{-1} \times B_b \times V_{in} \tag{5.36}$$

$$X_L = \begin{bmatrix} I_{LL1} \\ I_{LL2} \\ V_{CL} \\ V_2 \end{bmatrix} = -A_L^{-1} \times B_L \times V_{in} \tag{5.37}$$

Eq. (27), (28), and (29) are placed in the state-space averaged equations to produce the small signal model. Small signal and DC terms are then separated and further simplified. Then, laplace transformations to state spaceequations are used to formulate the resulting transfer functions, G(s) and T(s). The following are the expressions for the Boost and Luo converters i.e. G(s) and T(s) respectively:

$$G(s) = \frac{\hat{x}_b}{\hat{d}_2} = \left[sI - A_b\right]^{-1} \times \left[\left(A_{1b} - A_{2b}\right) X_b + \left(B_{1b} - B_{2b}\right) \times V_{in}\right] = \begin{bmatrix} G_{11} \\ G_{21} \end{bmatrix} \tag{5.38}$$

$$T(s) = \frac{\hat{x}_L}{\hat{d}_1} = \left[sI - A_L\right]^{-1} \times \left[\left(A_{1L} - A_{2L}\right) X_L + \left(B_{1L} - B_{2L}\right) \times V_{in}\right] = \begin{bmatrix} T_{11} \\ T_{21} \\ T_{31} \\ T_{41} \end{bmatrix} \tag{5.39}$$

$$\frac{\hat{V}_0}{\hat{d}_2} = V_0 \left\{ \frac{(R_T) \times (1 - D_2) - L_B(s)}{(1 - D_2) \times (s^2 R_T \times L_B \times C_T + L_B(s) + R_T \times (1 - D_2)^2)} \right\} \tag{5.40}$$

5.5 Design Specification

The desired current ripple can be achieved by selecting Boost's side inductance value, minimum values are calculated as indicated in expression as follows:

$$L_{B\min.} \geq \frac{d_2 \left(1 - d_2\right)^2 \times R_{L1}}{2 \times f_s} = \frac{0.5 \times \left(1 - 0.5\right)^2 \times 11.25}{2 \times 50 \times 10^3} = 16.75 \mu H \tag{5.21}$$

Similarly, Luo's inductors L_{L1} and L_{L2} can be expressed as shown

$$L_{L1\min.} \geq \frac{V_{in} \times d_1}{2 \times \Delta i_{LL1} \times f_s} = \frac{24 \times 0.5}{2 \times 1.9 \times 50 \times 10^3} = 63 \mu H \tag{5.22}$$

$$L_{L2\min.} \geq \frac{V_{in} \times \left(1 - d_1\right)}{2 \times \Delta i_{LL2} \times f_s} = \frac{24 \times \left(1 - 0.5\right)}{2 \times 1.3 \times 50 \times 10^3} = 80 \mu H \tag{5.23}$$

Following is converter's minimum capacitance sizing, so that desired voltage ripple is achieved: (I = output current)

$$C_{1\min.} \geq \frac{d_2}{\frac{\Delta V_1}{V_1} \times R_{L1} \times f_s} = \frac{0.5}{\frac{0.1}{48} \times 11.52 \times 50 \times 10^3} = 416.6\mu F \tag{5.24}$$

$$C_{2\min.} \geq \frac{I \times d_1}{\Delta V_{C2} \times f_s} = \frac{9.8 \times 0.5}{0.89 \times 50 \times 10^3} = 115.29\mu F \tag{5.25}$$

$$C_{L\min.} \geq \frac{I \times d_1}{\Delta V_{CL} \times f_s} = \frac{9.8 \times 0.5}{1.3 \times 50 \times 10^3} = 75.38\mu F \tag{5.26}$$

TABLE 5.2 Specifications of NBLI Converter

Specifications	**Symbols**	**Values**	**Units**
Input Voltage	V_{in}	24	V
DC bus Voltage	V_0	48	V
Output Voltage (Luo side)	V_2	24	V
Rated Power	P_o	450	W
Frequency of Switching	f_s	50	kHz
Inductor	L_B, L_{L1}, L_{L2}	100	μH
Luo Capacitor	C_L	80	μF
Output capacitors	C_1, C_2	1000	μF
Load Resistances	R_1, R_2	11.52, 10	Ω
PI for V_0/d_2	K_p, K_i	0.0009978, 0.77	-
PI for V_2/d_1	K_p, K_i	0.0000044, 0.0799	-

Here, Table II contains a list of chosen parameters used in converter design. Ziegler-Nichols tuning method is implemented for tuning transfer functions.

$$\frac{\hat{V}_0}{\hat{d}_2} = \frac{1.528 \times 10^4 \text{s-} 1.76 \times 10^8}{\text{s}^2 + 173.6\text{s} + 2 \times 10^6} \tag{5.27}$$

Lag compensator is designed, aims to improve the overall stability of converter, boost section (C_{boost}) as follows:

$$C_{\text{boost}} = \frac{-0.47107 * (s + 1845)}{s * (s + 3.5)} \tag{5.27}$$

5.6 Control Scheme

An appropriate closed-loop control has been designed to control the NBLI converter's output voltages (V_0 and V_2). G(s) and T(s) are employed in voltage controller design for the converter that is being presented here.

Applicable control-to-state $G_{21}(s)$ and $T_{41}(s)$ of NBLI's for output voltage control of V_0 and V_2 are obtained by replacing these parameters of table II. V_{0ref} and V_{2ref} are the reference voltages that are set to be desired output voltages respectively. The control signals are the error signals produced by comparing measured output voltages (V_o) and (V_2) with reference voltages. Voltage control is achieved by employing PI control method. PI controller is implemented and tuned; its gains modified to prevent the output voltage from being impacted by dynamic.

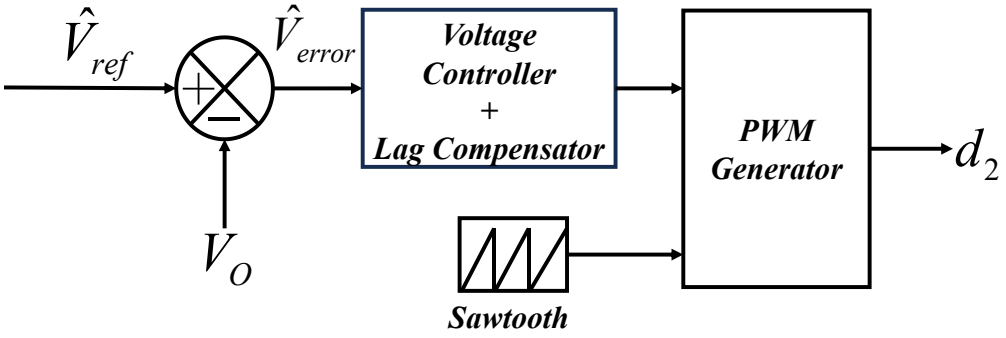

Fig. 5.7 Output Voltage V_0 Control

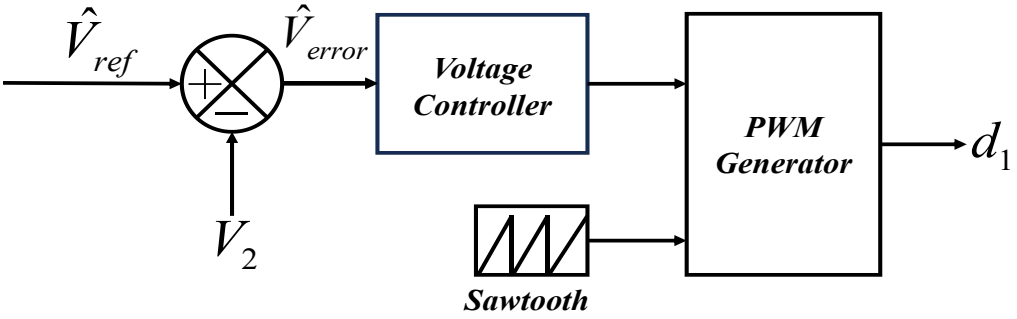

Fig. 5.8 Output Voltage V_2 Control

conditions. Tuned controller eliminates error, which are the difference between V_o, V_2 and V_{0ref}, V_{2ref}. Fig. 8 and 9 display the control schematic for output voltage control.

5.7 Result & Discussion

This section contains simulation results of NBLI converter, a 450 W system demonstrated with presented DC-DC converter. System is validated in MATLAB/ Simulink.

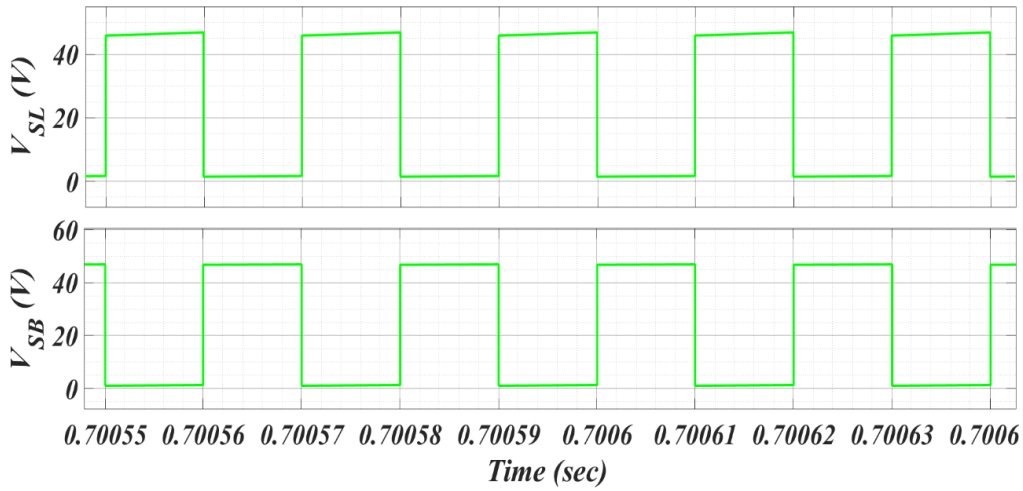

Fig. 5.9 Voltage Stress across switches V_{SL} (V), V_{SB} (V)

The converter's operation, here Boost side controls the 48 V (V_O) and Luo side controls the 24 V (V_2) output voltages. Performance of system is analysed through waveforms of different parameters.

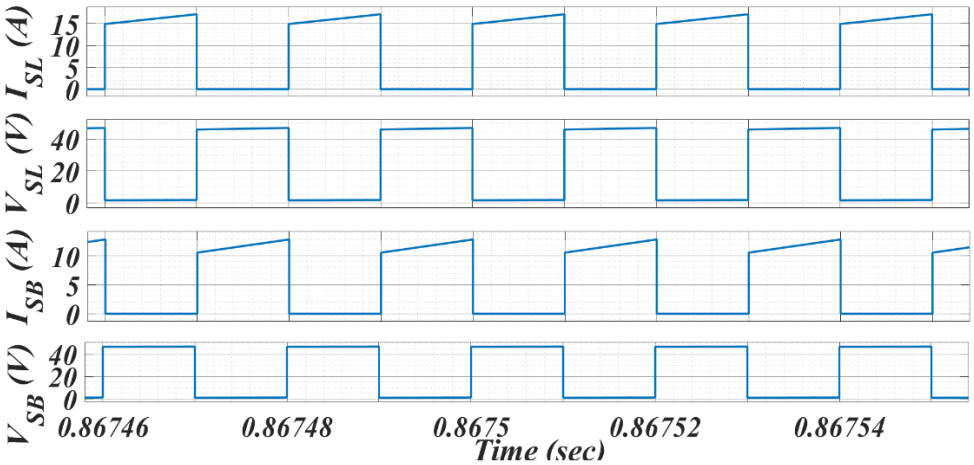

Fig. 5.10 Switches voltage stress V_{SL} (V), V_{SB} (V), Current I_{SL} (A), I_{SB} (A)

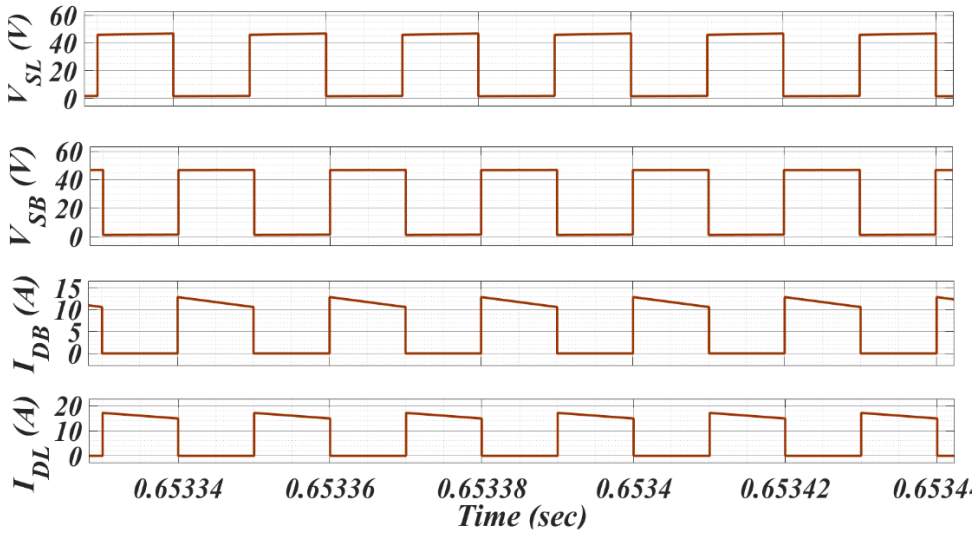

Fig. 5.11 Switch Voltage Stress (V_{SL}), (V_{SB}), Diode current (I_{DB}), (I_{DB})

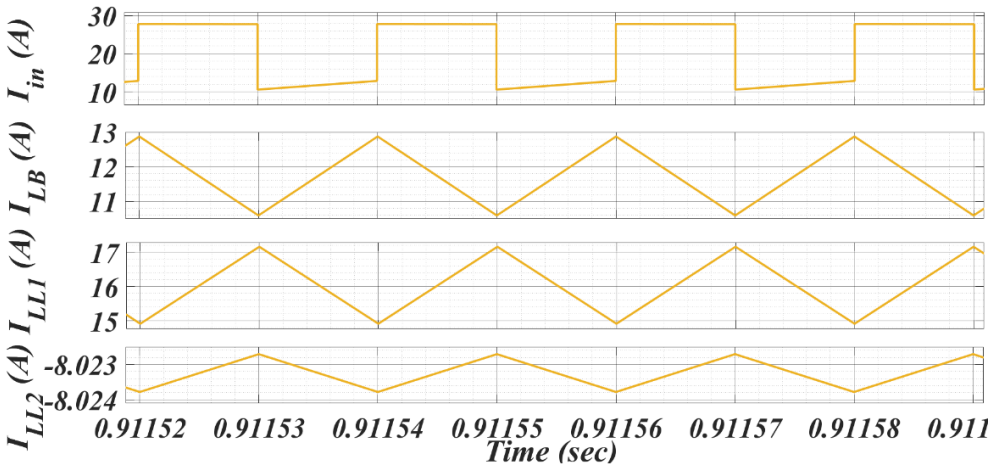

Fig. 5.12 Input current I_{in} (A) and Inductor Currents of Boost and Luo converters I_{LB} (A), I_{LL1} (A), I_{LL2} (A)

Switches' voltage stress and current (V_{SB}), (V_{SL}), (I_{SB}), (I_{SL}) input current (I_{in}), Boost inductor currents (I_{LB}), Luo inductor currents (I_{LL1}), (I_{LL2}), diode current (I_{DB}), (I_{DL}), Input current I_{in}.

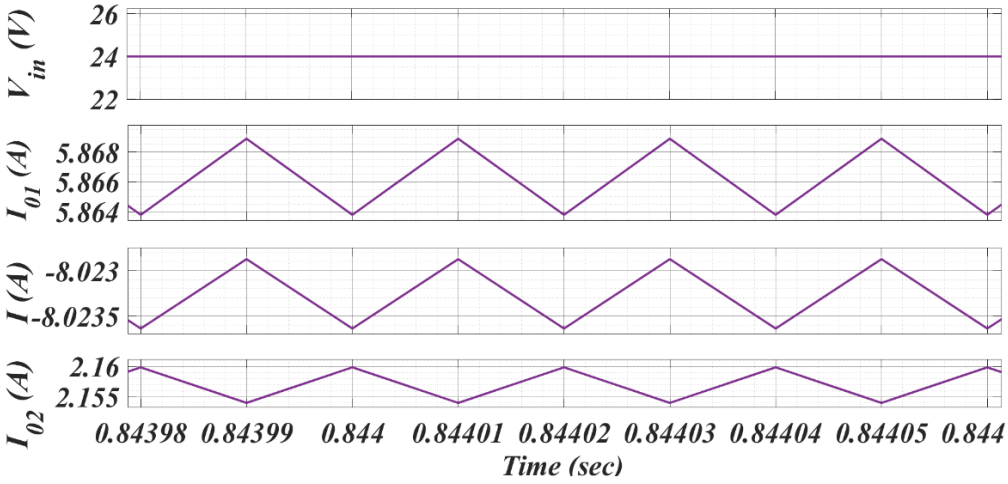

Fig. 5.13 Input Voltage V_{in} (V), and Output Currents I_{01} (A), I (A), I_{02} (A)

and Inductor Currents of Boost and Luo converters (I_{LB}), (I_{LL1}), (I_{LL2}), Input Voltage (V_{in}) and Output Currents (I_{01}), (I), (I_{02}) (A) are presented in figures from Fig. 5.12-13 respectively.

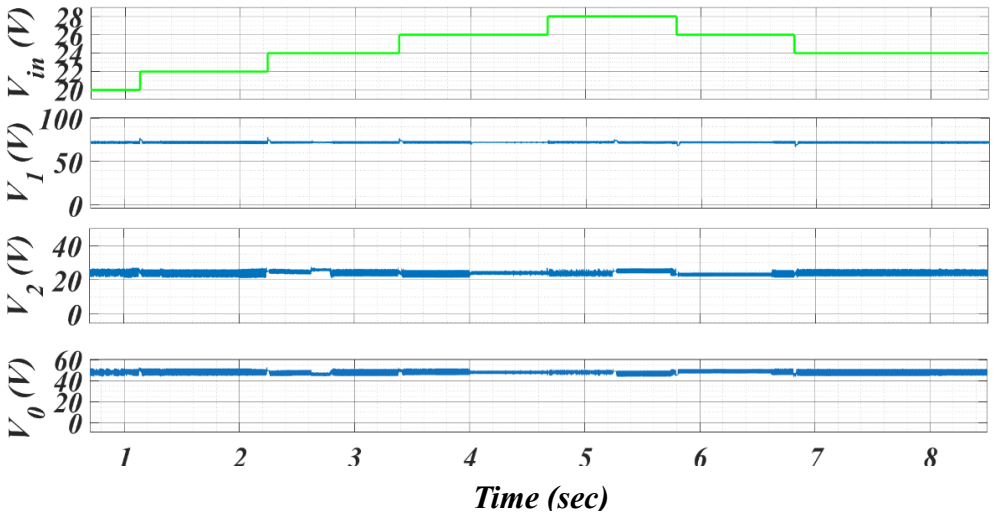

Fig. 5.14 Voltage Control of output voltages for dynamic source voltage

Fig. 5.14 represents output voltages control of V_1 i.e. 72 V, V_2 = 24 V, and V_0 is 48 V. Voltage control for dynamic source voltage (V_{in}) is shown in this representation of output voltages V_1 (V), V_2 (V), and V_0 (V).

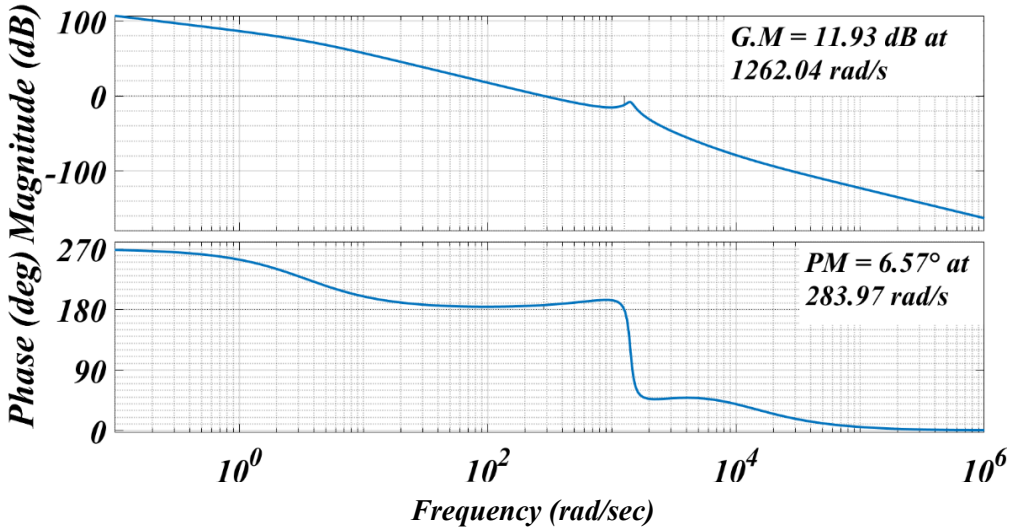

Fig. 5.15 Bode Plot of Compensated Boost section

In Fig. 5.15, Compensated bode plots of transfer functions GV_0/d_2 is presented. Employing the lag compensator for plot representing $G_{21}(s)$. For $G_{21}(s)$, phase margin (PM) is 6.57° at 283.97 rad/sec and gain margin (GM) is 119.93 dB at 1262.04 rad/sec.

5.8 Conclusion

A non-isolated SIDO NBLI DC-DC converter intended for BDCM operation, is presented here. Due to interleaving of Boost and Luo converters, the input source current ripples are reduced. Presented converter is suitable for interfacing battery or PV as source to LVBDCM and providing multiple voltage levels V_1, V_2, and V_0 as output resulting in reducing requirement for several converters.

This chapter provided CCM's steady-state analysis in detail, design and analysis of converter, dynamic modelling, operating principle, VCM of converter and simulation results. Without voltage controller, output voltages are having alterations, for VCM PI controller approach is implemented to obtain constant intended output voltage levels. NBLI can provide bidirectional operation by substituting diodes (D_B and D_L) with MOSFETs/IGBTs as S_{B1} and S_{L1}. Body diodes of substituted switches function in manner of primary. Interleaving of the converter, lowers the switches current rating, effective filter size, and current stress.

Scope of improving the overall converter's stability by designing compensator, involving parasitic, losses and efficiency calculations, comparison of various interleaved topologies can be included. NBLI Converter's performance is validated and analysed by simulation results.

CHAPTER 6

DESIGN DEVELOPMENT AND ANALYSIS OF BI-POLAR BUCK BUCK-BOOST DC-DC CONVERTER

6.1 General Aspect

Based on buck and buck/boost structures, a single-input dual-output DC-DC converter is presented. With the use of two degrees of freedom, the outputs of this suggested converter can operate on its own and adjusted. Other advantages include low component count, low voltage stress across the switching components, and a straightforward structure. Regardless of the converter parameters, this topology is free of right half s-plane zeros.

6.2 Schematic of Bi-Polar Buck Buck-Boost DC-DC Converter

Figure 1 shows the circuit schematic for the presented dual-output buck boost converter. Two inductors (L_1 and L_2), two switches (S_1 and S_2), two diodes (D_p, D_n), two capacitors (C_{o1}, C_{o2}), and an input DC source (Vin) make up this converter. Two asymmetric outputs are generated by this circuit: a negative buck-boost (V_n) and a positive buck (V_p). The output capacitors C_{o1} and C_{o2} are linked in parallel as by positive and negative output loads (R_{L1} and R_{L2}, respectively).

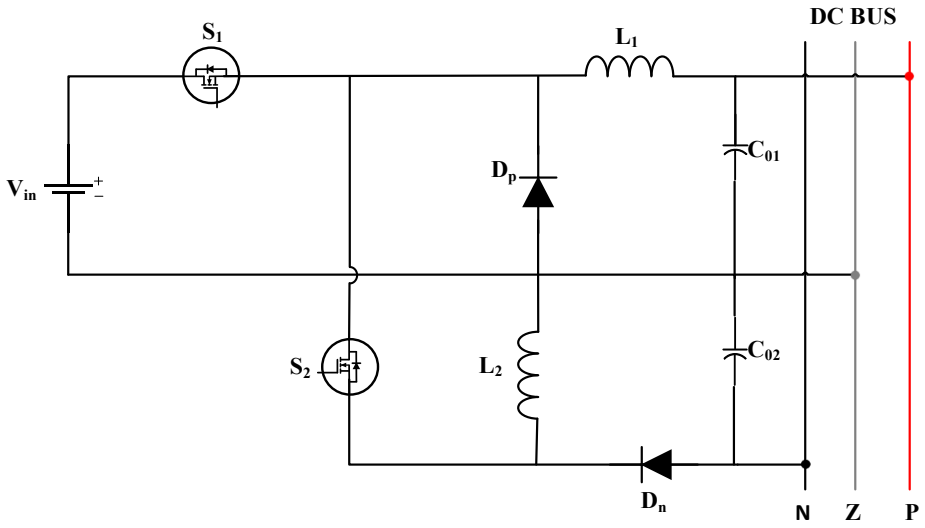

Fig. 6.1 Circuit Diagram of Boost-Luo Interleaved DC-DC Converter with DC bus

Figures 6.2 and 6.3-6.6 show the main waveforms and the associated circuit for each mode of the presented converter. The following figures make it evident that the two power switches of the suggested converter do not work in tandem, so their switching logic does not need dead time. Both of the circuit's outputs benefit from the diode Dp and switch S_2's performances. By default, if both of the proposed converter's switches (S_1 and S_2) are turned on simultaneously in Fig. 6.2.

The fundamental waveforms of one switching cycle converter and its analogous circuits are shown; d1 represents the operational degree of freedom. The introduced topology in CCM works in the following three steps:

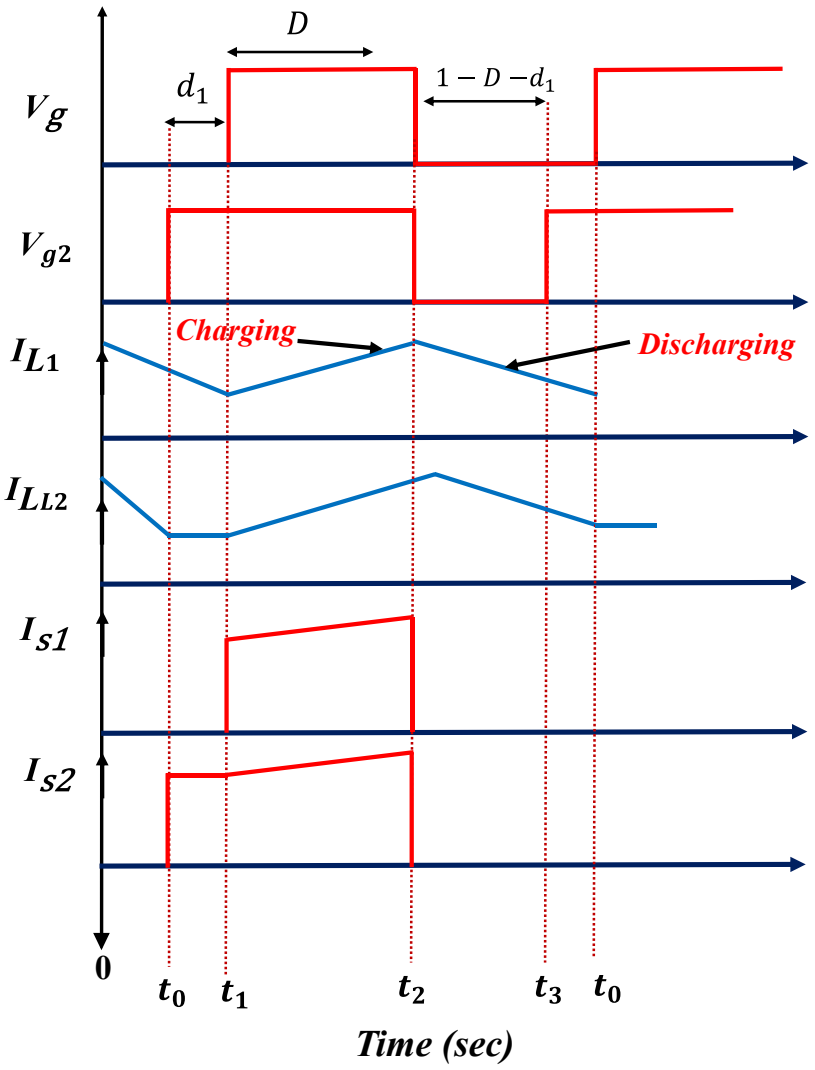

Fig. 6.2 Steady State Waveform of Buck Buck-Boost Converter

6.3 Modes of Operation

All semiconductor devices are considered as ideal in order to simplify presented circuit analysis. Converter capacitors' ESRs and diodes' forward voltage drops are neglected. Since all of capacitors and inductors are large enough, their voltage and current remain constant throughout a single switching cycle. Here, resistive load is linked in series with inductive load, R_{L1} to L_{01} and R_{L2} to L_{02}, respectively.

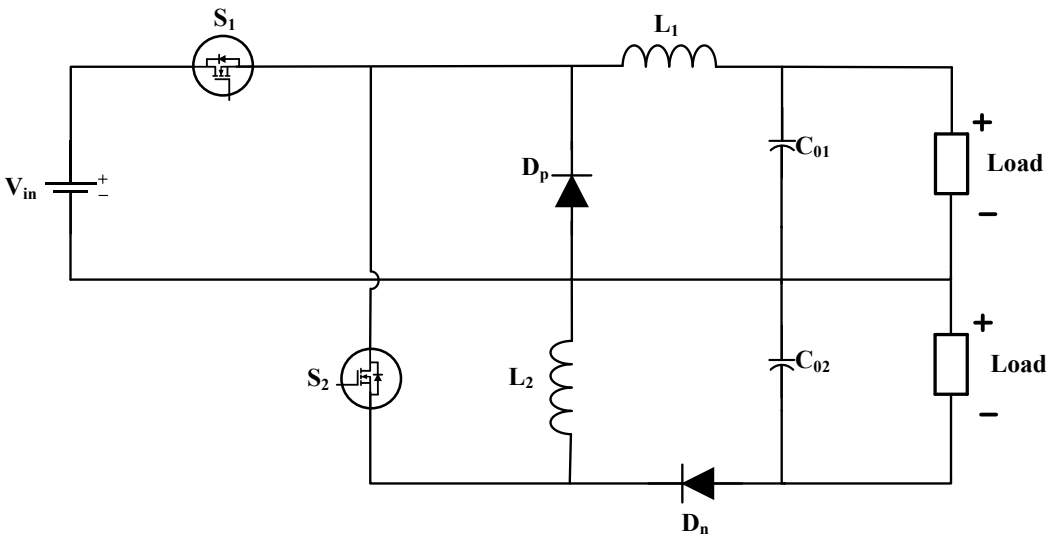

Fig. 6.3 Circuit diagram of Boost-Luo interleaved DC-DC converter with Resistive load

Operating state 1: While power switch S_1 is turned off, switch S_2 is turned on to start this stage. Diode D_p is conducting and Diode D_n is reverse-biased, as shown in Fig. 3(a). In this mode, the output capacitor C_{o1} receives inductor's energy while inductor L_2's current remains constant.

Input DC voltage is clamped to the power switch S_1. In addition, C_{O2} capacitor releases the energy it has stored into negative load. In this step, the following equations are written:

$$V_{L1} = -V_{Co1} \tag{6.1}$$

$$V_{L2} = 0 \tag{6.2}$$

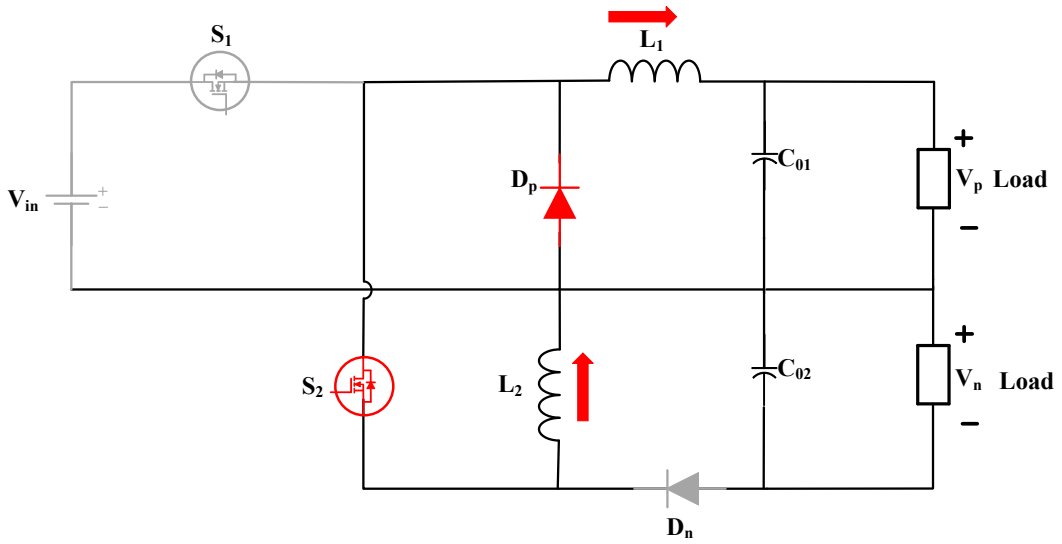

Fig. 6.4 Circuit diagram of Operating state 1 DC-DC converter

Operating state 2: The equivalent circuit of the introduced converter in operating mode II is shown. Diodes are off and two power switches, S_1 and S_2, are on in this mode. The input DC source provides energy to the inductors L_1 and L_2. Consequently, there is a linear increase in their currents (I_{L1} and I_{L2}). This span of time serves to write the equations below:

$$V_{L1} = V_{in} - V_{Co1} \tag{6.3}$$

$$V_{L2} = V_{in} \tag{6.4}$$

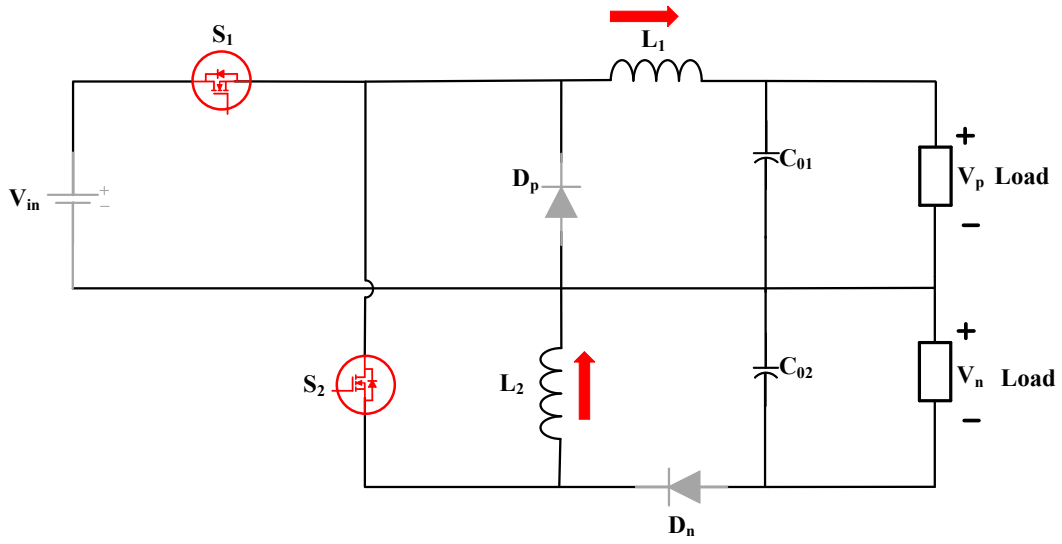

Fig. 6.5 Circuit Diagram of Operating State 2 DC-DC Converter

Operating state 3: When the power switches S_1 and S_2 are simultaneously turned off, this stage starts (Fig. 3(c)). The diodes D_p and D_n are forward-biased in this mode. The output capacitors C_{o1} and C_{o2} in the positive and negative cells receive the stored energy from the inductors L_1 and L_2 during this time. Furthermore, the power switches are clamped to the negative output voltage and the input DC source. This mode expresses the following equations:

$$V_{L1} = -V_{Co1} \tag{6.5}$$

$$V_{L2} = -V_{Co2} \tag{6.6}$$

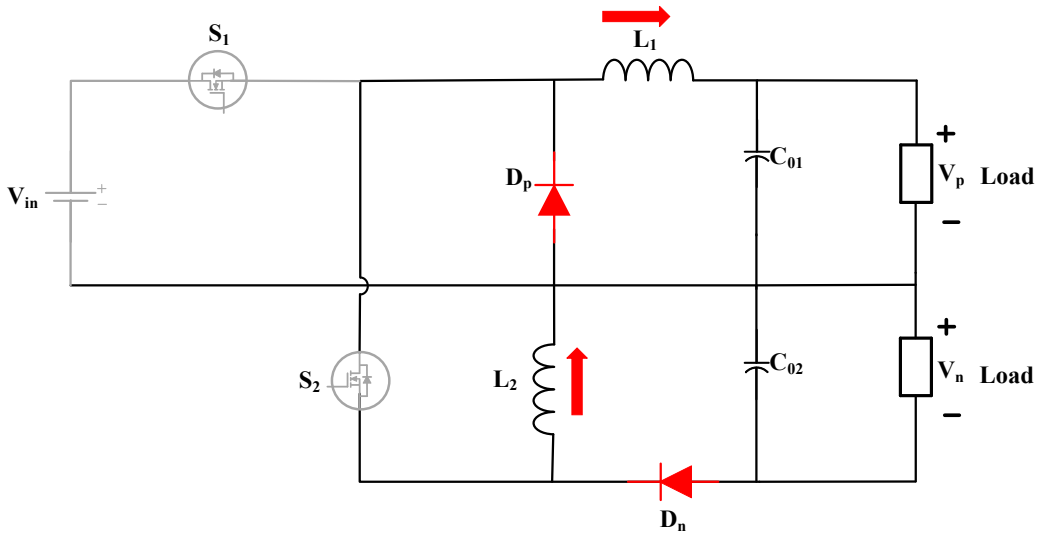

Fig. 6.6 Circuit diagram of Operating state 3 DC-DC converter

Positive and negative voltage gains of the presented converter is adjusted separately across an extensive range in the second duty cycle (d_1). Presented converter's duty cycle d_1 has the ability to reduce the cross-regulation effect. Ideal negative voltage gain (M_{o2}) versus duty cycles D and d_1 is shown. Using these numbers, it is possible to obtain high voltage gains at low main duty cycles by slightly raising the parameter d_1. In addition, positive output voltage is used to calculate main duty cycle (D) value. Once parameter D has been determined, desired M_{o2} can be used to determine value of d_1.

6.3 Modelling of Bi-Polar Buck Buck-Boost DC-DC Converter

Presented topology's small signal derivation is given in this section. State-space averaging technique is employed for this purpose.

Following are the converter's state equations in operation state 1:

$$\frac{di_{L1}}{dt} = -\frac{V_{Co1}}{L_1} \tag{6.7}$$

$$\frac{di_{L2}}{dt} = -\frac{V_{Co2}}{L_2} \tag{6.8}$$

$$\frac{di_{Lo1}}{dt} = V_{Co1} - R_{L1} i_{Lo1} \tag{6.9}$$

$$\frac{di_{Lo2}}{dt} = V_{Co2} - R_{L2} i_{Lo2} \tag{6.10}$$

$$\frac{dv_{Co1}}{dt} = \frac{i_{L1}}{C_{o1}} - i_{Lo1} \tag{6.11}$$

$$\frac{dv_{Co2}}{dt} = \frac{i_{L2}}{C_{o2}} - i_{Lo2} \tag{6.12}$$

Equations of operating mode-2 as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{v_{Co1}}{L_1} \tag{6.13}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2} \tag{6.14}$$

$$\frac{di_{Lo1}}{dt} = V_{Co1} - R_{L1} i_{Lo1} \tag{6.15}$$

$$\frac{di_{Lo2}}{dt} = V_{Co2} - R_{L2} i_{Lo2} \tag{6.16}$$

$$\frac{dv_{Co1}}{dt} = \frac{i_{L1}}{C_{o1}} - i_{Lo1} \tag{6.17}$$

$$\frac{dv_{Co2}}{dt} = -i_{Lo2} \tag{6.18}$$

Equations of operating mode-2 as follows:

$$\frac{di_{L1}}{dt} = -\frac{V_{Co1}}{L_1} \tag{6.19}$$

$$\frac{di_{L2}}{dt} = 0 \tag{6.20}$$

$$\frac{di_{Lo1}}{dt} = V_{Co1} - R_{L1} i_{Lo1} \tag{6.21}$$

$$\frac{di_{Lo2}}{dt} = V_{Co2} - R_{L2} i_{Lo2} \tag{6.22}$$

$$\frac{dv_{Co1}}{dt} = \frac{i_{L1}}{C_{o1}} - i_{Lo1} \tag{6.23}$$

$$\frac{dv_{Co2}}{dt} = -i_{Lo2} \tag{6.24}$$

The weighting factors can be applied to get converter's averaged model, which includes d_1, d, and (1-d_1 d), for conduction modes 1, 2, and 3.:

$$\begin{aligned} x &= Ax + Bu \\ y &= cx + du \end{aligned} \tag{6.25}$$

Here,

$$\begin{aligned} \mathrm{A} &= d_1 A_1 + dA_2 + \left(1 - d_1 - d\right) A_3 \\ \mathrm{B} &= d_1 B_1 + dB_2 + \left(1 - d_1 - d\right) B_3 \\ \mathrm{C} &= d_1 C_1 + dC_2 + \left(1 - d_1 - d\right) C_3 \\ \mathrm{D} &= d_1 D_1 + dD_2 + \left(1 - d_1 - d\right) D_3 \end{aligned} \tag{6.25}$$

where y is the output voltage, x is average value of variable states, and u is input DC voltage. A, B, C, and D are state coefficient matrices. It is possible to obtain results of voltage-to-control transfer functions by applying minor disturbances to variable states (33), while ignoring DC terms.

Laplace transformation, each output voltage's control-to-output functions can be found. Accompanying simplification, below are transfer functions in concise form:

$$G_{vod}(s)=\frac{\hat{v}_{o1}}{\hat{d}}=\frac{\left(R_{L1}+L_{o1}S\right)A_4}{B_5\cdot S^3+B_6\cdot S^2+B_7\cdot S+B_8} \tag{6.26}$$

$$G_{vod}(s)=\frac{\hat{v}_{o2}}{\hat{d}}=\frac{\left(R_{L2}+L_{o2}S\right)A_2}{B_1\cdot S^3+B_2\cdot S^2+B_3\cdot S+B_4} \tag{6.27}$$

It is clear that RHPZ is eliminated regardless of the specifications of suggested converter circuit. Notably, a left-hand zero and a left-hand pole are introduced to transfer functions in order to account for R-L loads for envisioned DC-DC converter.

6.5 Design Specification

Desired current ripple can be achieved by selecting Buck side inductance value, and are calculated as indicated in expression as follows:

$$L_1=\frac{DV_{L1}}{\Delta I_{L1}f}>\frac{D(1-D)V_{in}}{0.2I_{L1}f} \tag{6.28}$$

$$L_2=\frac{\left(1-D-d_1\right)V_{L2}}{\Delta I_{L2}f}>\frac{\left(1-D-d_1\right)V_{O2}}{\Delta I_{L2}f} \tag{6.29}$$

In this case, f is the switches' switching frequency. By considering into account (13)–(14), the converter's output capacitors (Co1 and Co2) can be chosen in the manner as follows to reduce the output voltage ripple:

$$C_{o1}>\frac{DI_P}{\Delta V_{Co1}f} \tag{6.30}$$

$$C_{o2}>\frac{DI_N}{\Delta V_{Co2}f} \tag{6.31}$$

Notably, unlike aside high gain DC-DC converters, one recommended has no restrictions on duty cycle selection other than to steer clear of duty cycle values that are near unity. High current stresses on components in relatively high-duty cycles (near unity) cause step-up DC-DC converters to lose efficiency. As a result, the maximum duty cycle typically gets restricted to D<0.8.

TABLE 6.1 Specifications of Buck Buck-boost Converter

Specifications	**Symbols**	**Values**	**Units**
Input Voltage	V_{in}	50	V
Duty cycles	D, d_1	0.6, 0.2	–
Rated Power	P_o	450	W
Frequency of Switching	f_s	50	kHz
Inductor	L_1, L_2	1, 600	$mH, \mu H$
Load Inductor	L_{01}, L_{02}	2	mH
Output capacitors	C_1, C_2	100	μF
Load Resistances	$R_{L1,}R_{L2}$	100, 100	Ω

6.6 Control scheme

Here, for the control scheme for presented DC-DC converter with two switches using open-loop PWM is a straightforward method where each switch is driven by a fixed duty cycle. In this setup, no feedback from the output is used. Instead, PWM signals are generated based on predefined timing to control when each switch turns on and off.

For instance, one switch might handle the buck-boost stage while the other manages the buck stage, each operating during specific intervals of the switching cycle. While this method is simple and easy to implement, it doesn't adapt to changes in input voltage or load, which can affect performance. The cross-regulation effect is lessened by an extra (d_1) through a period of frolicking, which permits output voltages to be changed separately.

6.7 Result & Discussion

This section displays Buck Buck-boost converter simulation results for CCM activities. MATLAB/Simulink was used to build and model the converter; simulation results are displayed.

In order to offer CCM conditions of operation of resistive load range of 100 Ω, a switching frequency of 30 kHz was used.

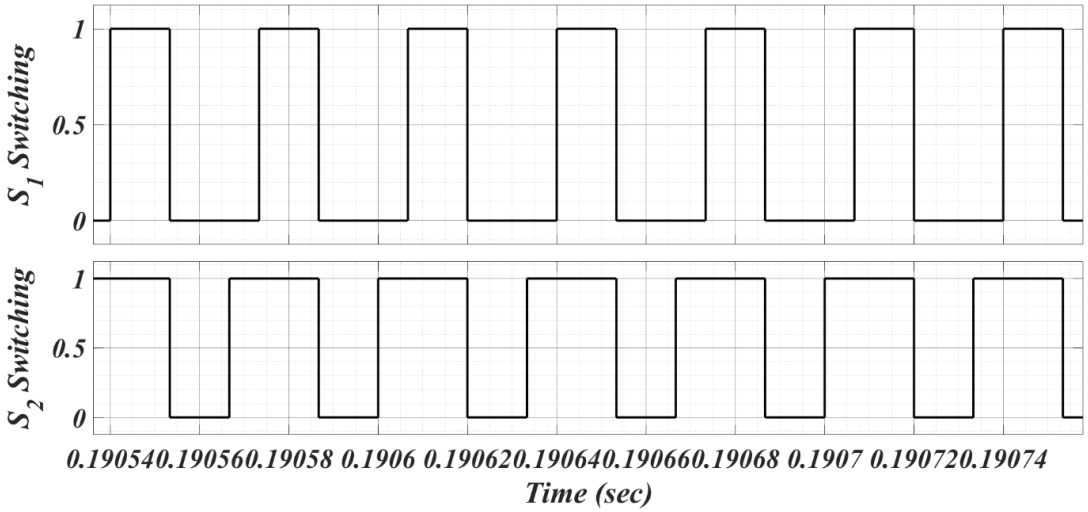

Fig. 6.7 Switching operation of switches S_1 and S_2

The input voltage, inductors, and output capacitors are 50V, 1mH and 600uH, and 100 µF, load inductor are 2mH respectively.

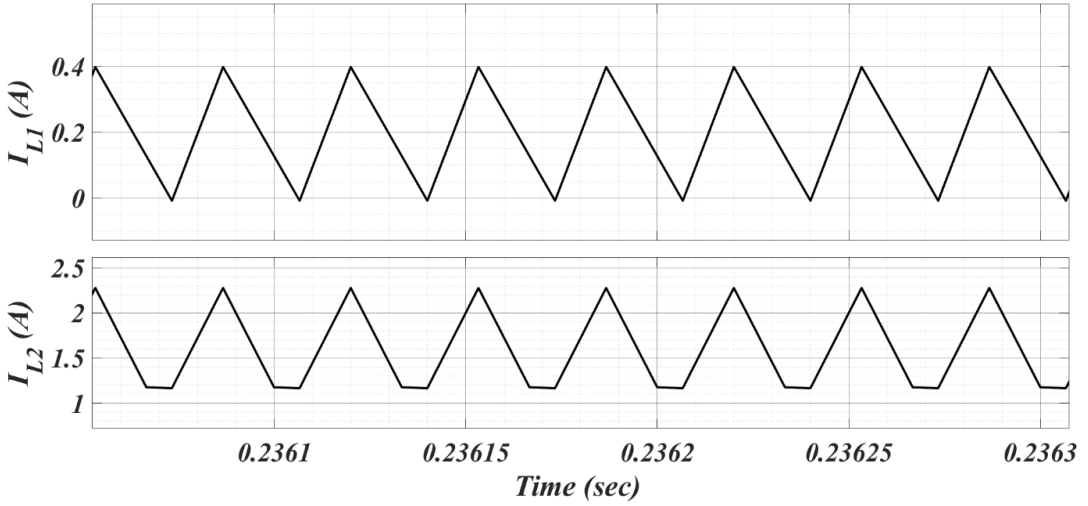

Fig. 6.8 Inductor currents I_{L1} (A), I_{L2} (A)

The output loads of 100 Ω are employed to demonstrate converter's effectiveness throughout CCM operating period..

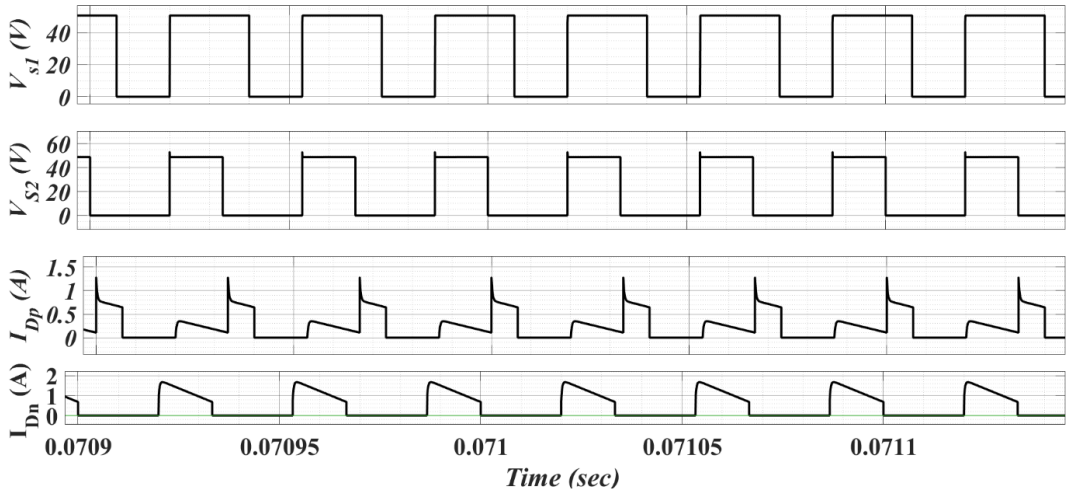

Fig. 6.9 Voltage Stress across S_1, S_2 (V_{S2}, V_{S1}) and Diode D_p, D_n Current (I_{Dp}, I_{Dn})

Here, presenting the simulation voltage stress across S_1, S_2 (V_{S2}, V_{S1}) and diode D_p, D_n current through (I_{Dp}, I_{Dn}) are as respectively.

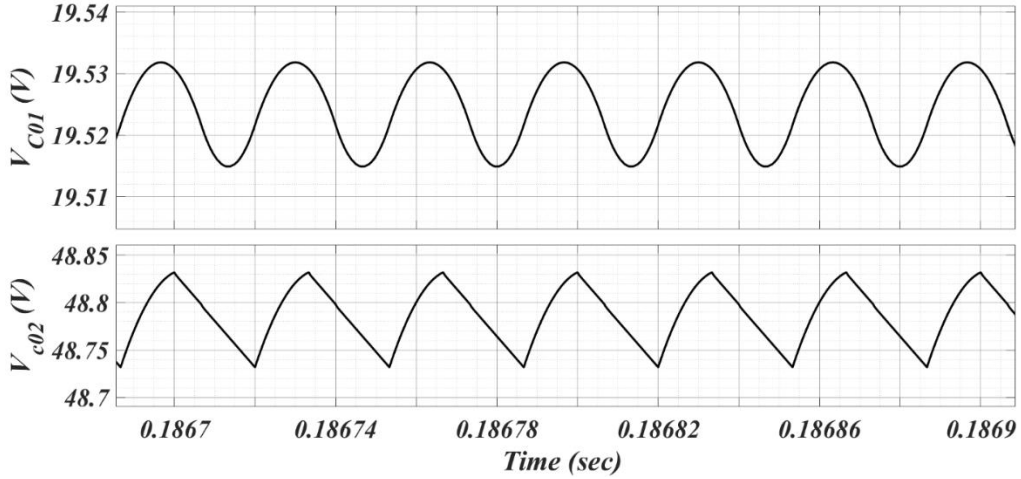

Fig. 6.10 Voltage Stress capacitors V_{C01}, V_{C02} (V)

Here, presenting the simulated voltage Stress across capacitors V_{C01} (V), V_{C02} (V) are as respectively.

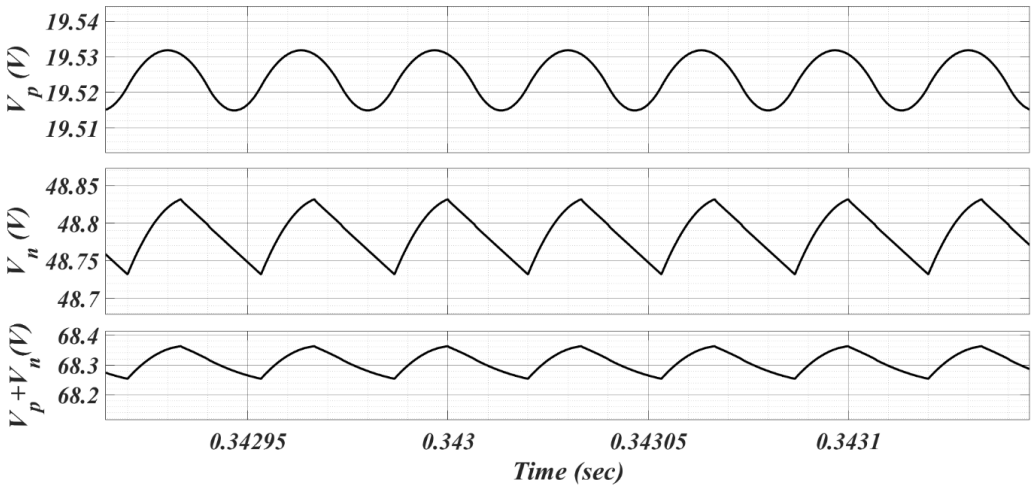

Fig. 6.11 Output Voltages across load V_p, V_n, V_p+V_n (V)

These are the output voltages across load, where V_p+V_n are the sum of both the output voltages respectively.

6.8 Conclusion

In conclusion, these are the primary benefits of the Buck Buck-boost that is being offered. Two distinct outputs in form of a Buck and a Buck-Boost converter, degrees of freedom for varying output voltages separately, min. phase behaviour, a high voltage gain ratio, and same cycle are characteristics of DC-DC bipolar topology.

DC frameworks with a quick initial reaction can use the converter that is being described.

CHAPTER 7

DESIGN DEVELOPMENT AND ANALYSIS OF BIPOLAR BOOST-SEPIC INTERLEAVED DC-DC CONVERTER WITH ACTIVE LOAD

7.1 General Aspect

For low-voltage bipolar dc microgrid application, a boost-SEPIC interleaved type dc-dc converter is suggested in this architecture. With two outputs, the suggested converter combines a boost and SEPIC converter in parallel. It works effectively in a bipolar dc microgrid setting for low-voltage, high-current applications. DC-DC buck converter and boost-SEPIC interleaved converter functioning as a load converter controlled by voltage loop control.

The suggested converter's dynamic modelling and steady-state analysis are provided in detail. Results from simulations are shown to confirm the converter's functionality.

7.2 Schematic of Bipolar interleaved DC-DC Converter

The presented converter integrates boost-SEPIC interleaved topologies. When compared to traditional converters of the same rating, the interleaving approach offers the advantages of lower current stress and less source current ripple. Here, circuit configuration is with DC bus connection. The converter that is being presented offers interleaving advantages in addition to multiple output voltage levels. A boost-SEPIC interleaved converter presented here. For a variety of applications, the converter can provide balanced or non-balanced output voltages, keeping output voltages steady even when loads are not balanced. On account of its voltage balancing capability, presented converter delivers voltage balancing capabilities for bipolar applications in LVDC systems.

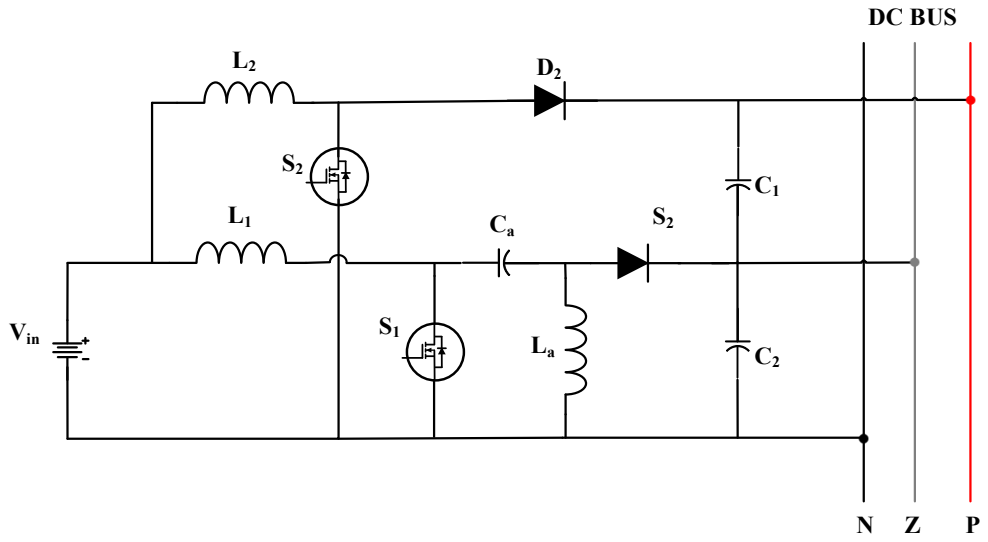

Fig. 7.1 Circuit diagram of Boost-SEPIC interleaved DC-DC converter with DC bus

The schematic representation for the NBLI DC-DC converter is shown in Fig. 2, which also shows the presented DC-DC converter configuration. 48V bus is linked to Boost converter's output, while 24V bus is linked to the Luo converter's output.

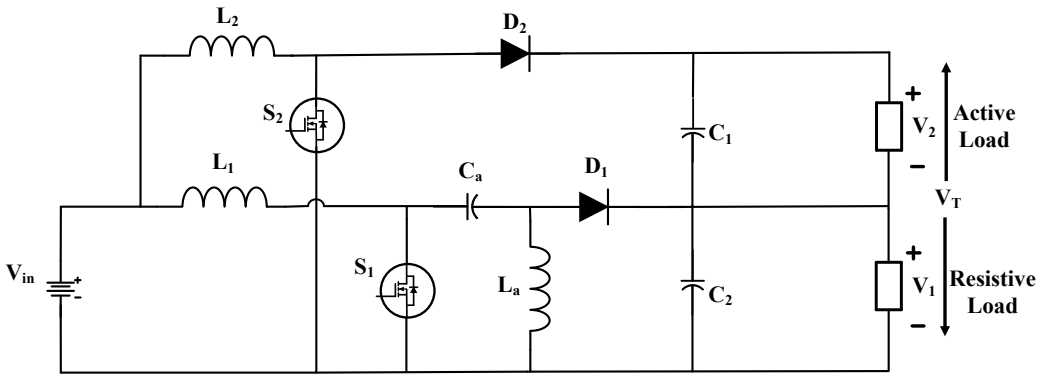

Fig. 7.2 Circuit diagram of Boost-SEPIC interleaved converter with Active and Resistive load

Topology that is being presented combines a SIDO configuration with interleaving Boost-SEPIC converters. The input and output sides of the switching cells are connected in parallel and series, respectively. In the two-phase scenario, pulses for switching are delivered to S_1 and S_2 in an interleaved manner, means they are 180° degrees apart. When S_1 is operating the S_2 will be off and vice versa. V_{in} refers to voltage of input source; in this case, a battery is employed, and its voltage can range from 16 to 26 V. V_o is the overall DC bus voltage following by V_1, V_2 are the Boost and SEPIC output voltages.

The Boost side boasts an active load i.e. a buck converter having input V_2, L and C are designed, diode D_1, active switch S_2, and inductor L_2. The SEPIC side includes load resistor R_L, diode D_L, capacitors C_2, active switch S_1, and inductors L_1 and L_a. As RESs can have low voltages between 18 and 26 V, SEPIC converter is selected to interconnect with load and a Boost to interconnect with active load. SEPIC converter is interleaved with Boost converter for its advantages, like low output voltage ripple, provides high efficiency and voltage gain with low conduction losses.

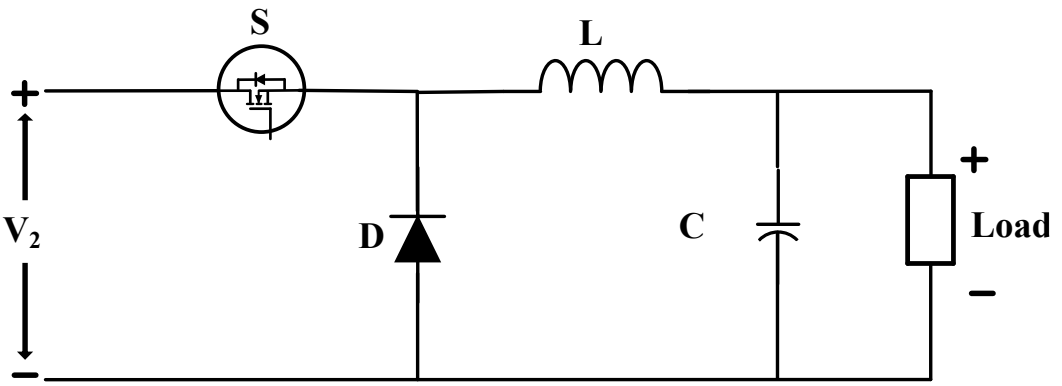

Fig. 7.3 Circuit diagram of Buck Converter as Active load

In order to ensure CCM, the inductors are purposefully designed. Filter capacitors, resistive load linked within ports P-Z and Z-N as C_1, R_{L1} and C_2, R_{L2} respectively. Here, P-Z and Z-N are the poles i.e. positive (P), negative (N), neutral (Z) respectively.

7.3 Modes of Operation

Here, boost-SEPIC interleaved converter's operating modes and a steady-state analysis of the converter in continuous conduction mode (CCM) are employed in this section. Ideal and lossless power components are assumed; parasitic components are not taken into account.

Four CCM modes are presented based on the switching functions of S_1 and S_2 switches. These modes are represented in Table 1 as follows:

TABLE 7.1 Conducting States of Boost-SEPIC Converter

Conducting States $S_{B\&}S_L$	Modes	L_1	L_2	C_1	C_2
00	Passive Mode 1	D	D	C	C
01	Active Mode 1	D	C	C	D
10	Active Mode 2	C	D	C	C
11	Passive Mode 2	C	C	D	D

❖ C- Charging, D- Discharging.

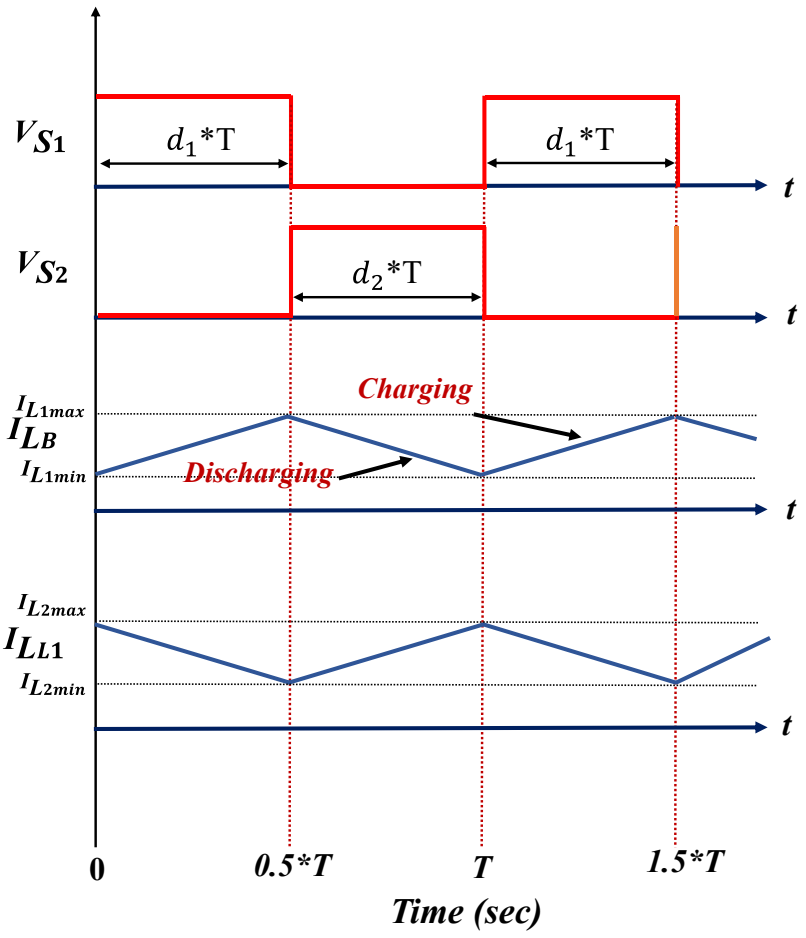

Fig. 7.4 Steady State Waveform of Boost-SEPIC-Interleaved Converter

1) Passive Mode 1: When S_1 and S_2 gated voltages are low, this mode starts. When neither of the active switches are conducting. Here, the both inductors are discharging and both capacitors are charging. Fig. 3 represents the circuit that goes with this mode:

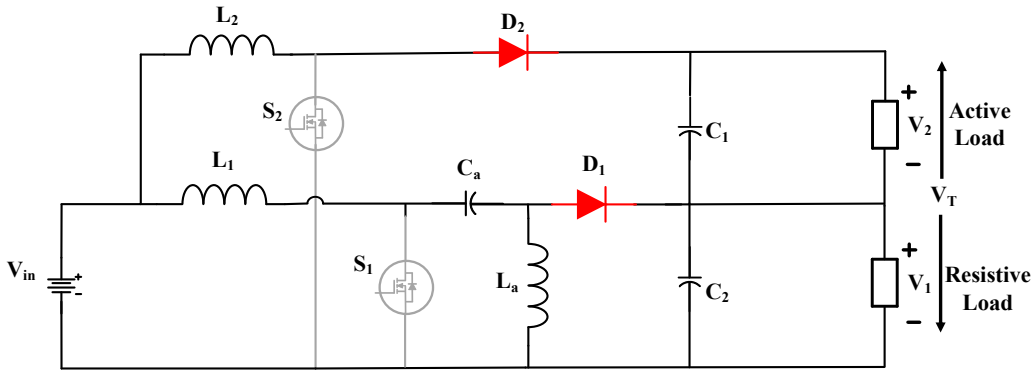

Fig. 7.5 Circuit Diagram of Boost-SEPIC Interleaved Converter in Passive Mode 1

(2) Active Mode 1: For S_1, mode starts when the pulse for gating is low, and switch S_2, it is high. S_1 is conducting when switch S_2 is not conducting. Here, the inductor (L_1) is discharging and (L_2) is charging, capacitor (C_1) is charging and (C_2) is discharging. Following figure represents the circuit that goes with this mode:

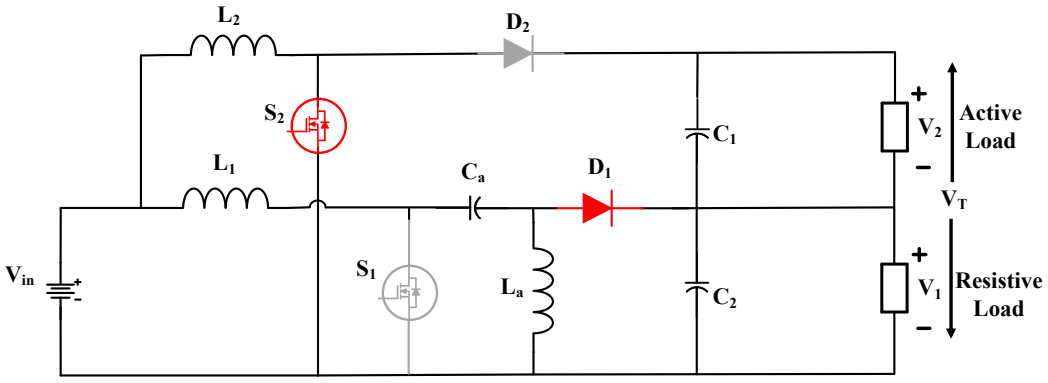

Fig. 7.6 Circuit diagram of Boost-SEPIC interleaved converter in Active mode 1

(3) Active Mode 2: For S_2, mode starts when the pulse for gating is low, and switch S_1, it is high. S_2 is conducting when switch S_1 is not conducting. Here, the inductor (L_2) is discharging and (L_1) is charging, capacitor (C_2) is charging and (C_1) is discharging. Following figure represents the circuit that goes with this mode:

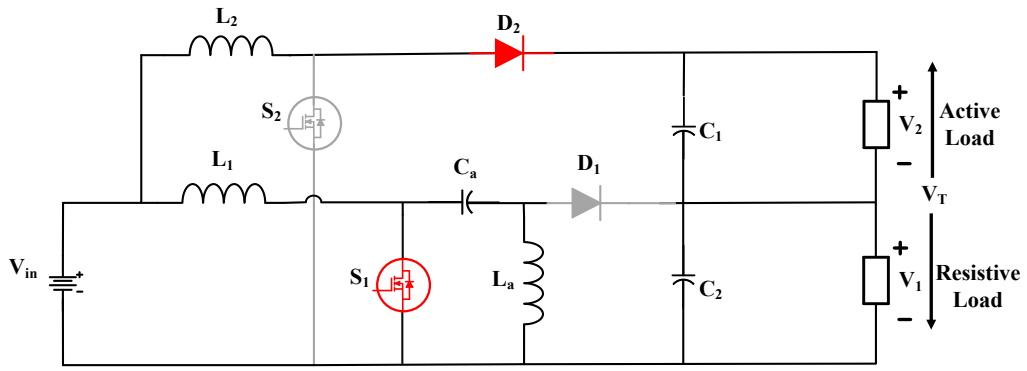

Fig. 7.7 Circuit diagram of Boost-SEPIC interleaved converter in Active mode 2

(1) Passive Mode 2: When S_1 and S_2 gated voltages are high, this mode starts. When the active switches are conducting. Here, the both inductors are charging and both capacitors are discharging. Fig. 3 represents the circuit that goes with this mode as follows:

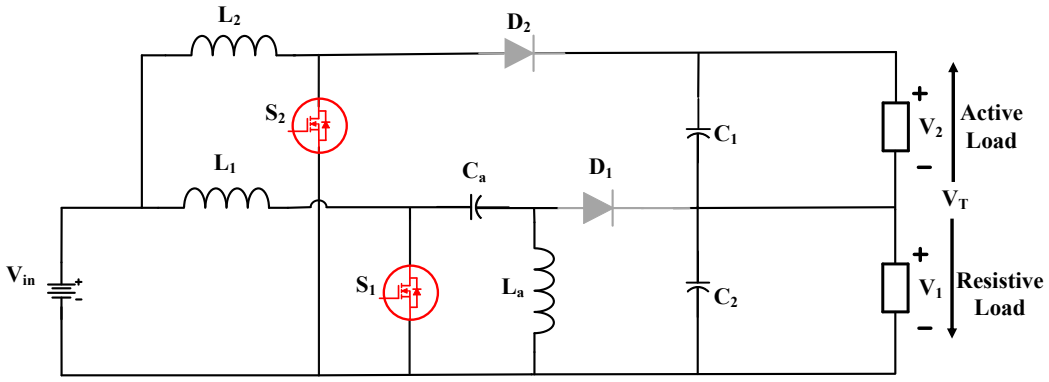

Fig. 7.8 Circuit diagram of Boost-SEPIC interleaved converter in Passive mode 2

7.4 Modelling of Bipolar Interleaved DC-DC Converter

Duty ratios of converter's S_1 and S_2 switches are displayed above, respectively. Relationship among the output voltages V_o and V_{in} and input voltage during steady-state and operation is explained below.

$$V_1 = V_{in} \times \frac{D_1}{1 - D_1} \tag{7.1}$$

If the system depicted in Fig. 1 makes use of the converter in Fig. 2, then:

$$V_T = V_1 + V_2 = V_{in} \times \frac{1}{1 - D_2} \tag{7.2}$$

Input voltage is taken to be equal to V in order to analyse converter's performance and demonstrate the of ripple in flow of electricity from the source is as small as possible:

$$V_{\text{in}} = V_1 = \frac{V_T}{2} \tag{7.3}$$

$$D_1 = D_2 = 0.5 \times T_s \tag{7.4}$$

Because duty ratios along with input inductors being identical for both converters, the current ripple in each will be equal. Current fluctuation in inductors is as follows: L and L_2:

$$\Delta i_{L1} = \Delta i_{L2} = \frac{V_{in}}{L} \times DT_S \tag{7.5}.$$

7.5 Design Specification

The different converter and controller design parameters are shown in the following table. With the parameters listed in the table:

Conducting States as following inductor and source currents:

$$\begin{aligned} i_{L1}(t) &= \frac{V_{\text{in}}}{L} \times t + I_{\text{min1}} \\ i_{L2}(t) &= -\frac{V_{\text{in}}}{L} \times t + I_{\text{max2}} \end{aligned} \tag{7.6}$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) = I_{\text{min1}} + I_{\text{max2}} \tag{7.7}$$

The inductor currents and source current for the Conducting States 2, and for conditions are as follows:

$$i_{L1}(t) = -\frac{V_{\text{in}}}{L} \times t + I_{\max 1}$$
$$i_{L2}(t) = -\frac{V_{\text{in}}}{L} \times t + I_{\min 2} \tag{7.8}$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) = I_{\max 1} + I_{\min 2} \tag{7.9}$$

It is evident from that, in hypothetical scenario described is no ripple in current pulled from source, ripple current obtained from input will be lower than that of a traditional non-isolated converter of equal potential.

TABLE 7.2 Specifications of Boost-SEPIC Converter

Specifications	**Symbols**	**Values**	**Units**
Input Voltage	V_{in}	22	V
Duty cycles	d_2, d_1	0.5, 0.5	–
Rated Power	P_o	200	W
Frequency of Switching	f_s	30	kHz
Inductor	L_1, L_2, L_a	250, 250, 350	μH
Total Output Voltage	V_T	48	V
Output capacitors	C_1, C_2, C_a	1000	μF
Load Resistances	$Buck, R_2$	-, 11.52	Ω
PI for V_1/d_2	K_p, K_i	0.009678, 0.87	-
PI for V_{AL}/d	K_p, K_i	0.00044, 0.0689	-

Here, Table 7.2 contains a list of chosen parameters used in converter design.

7.6 Control Scheme

Since the buck converter is an active load coupled to boost-SEPIC interleaved converter, a suitable closed-loop control has been developed to regulate its switching function. Voltage controller design under consideration makes use of the transfer functions G(s) and T(s).

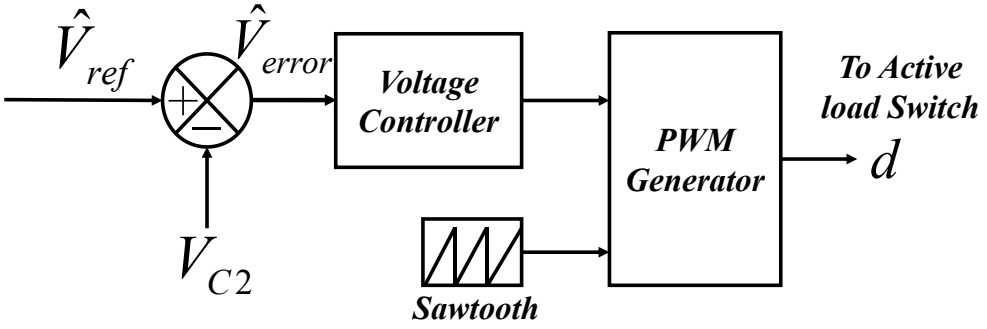

Fig. 7.9 Output Voltage Active Load Buck Converter

The input source that is linked to the suggested converter determines the mode of operation. A dynamic model of converter must be acquired in order to run it in V_C or CC mode. Using the state-space averaging technique, a continuous averaged model for each individual converter is created in order to get dynamic model of the converter.

Presuming that state variables are somewhat perturbed (i_{Ll}, i_{L2}, v_1, v_2) and duty ratios (d_1, d_2) linear small-signal AC paradigm is derived for every single converter about a DC functioning position. (I_{Ll}, I_{L2}, I_{La}, V_{ca}, V_1, and V_2).

$$i_{Lx} = I_{Lx} + \hat{i}_{Lx}$$
$$v_x = V_x + \hat{v}_x \quad (7.10)$$

$$d_y = D_y + \hat{d}_y \quad (7.11)$$

Applying Laplace transforms, we get:

$$T(s) = \frac{x_b^{\bullet}}{d_2} = \left[SI - A_b\right]^{-1} \times \left[\left(A_{1b} - A_{2b}\right) X_B + \left(B_{1b} - B_{2b}\right) V_{in}\right] = \begin{bmatrix} T_{11} \\ T_{21} \end{bmatrix} \quad (7.12)$$

$$G(s)=\frac{x_s^{\blacklozenge}}{d_1}=\left[SI-A_s\right]^{-1}\times\left[\left(A_{1s}-A_{2s}\right)X_S+\left(B_{1s}-B_{2s}\right)V_{in}\right]=\begin{bmatrix}G_{11}\\G_{21}\\G_{31}\\G_{41}\end{bmatrix} \tag{7.13}$$

For boost (b) and SEPIC (s) converters, mean state and input matrix are A) and B), where j = b, s. When switch for both converter in ON state, state and input matrices for boost (b) and SEPIC (s) converters are A_j) and B_j (where j = b, s). Likewise, when each converter's switch in OFF position, A_2) and B_{2j} are achieved. State vector for boost and SEPIC converter, X_j (where j = B, S), is determined by:

$$\begin{aligned}X_S &= \begin{bmatrix}I_{L1}\\I_{La}\\V_{Ca}\\V_1\end{bmatrix}\\ X_B &= \begin{bmatrix}I_{L2}\\V_T\end{bmatrix}\end{aligned} \tag{7.14}$$

Steady-state value of state vector given as following equations:

$$\begin{aligned}X_S &= -A_s^{-1}\times B_s\times Vin\\ X_B &= -A_b^{-1}\times B_b\times Vin\end{aligned} \tag{7.15}$$

Different converter and controller design parameters are presented. The converter's control-to-state transfer functions, are derived using parameters shown in the table. Therefore, the suggested converter's pertinent transfer functions (G_{11}(s) and T_{11}(s)) are provided by:

$$\frac{i_{L1}(s)}{d_1(s)}=\frac{1.8\times10^5 s^3+1.2\times10^8 s^2+4\times10^{11}s+1.31\times10^{14}}{s^4+966s^3+4\times10^6 s^2+2\times10^9 s+3.8\times10^{12}} \tag{7.16}$$

$$\frac{i_{L2}(s)}{d_2(s)}=\frac{1.897\times10^5 s+16.433\times10^6}{s^2+356.7s+8.539\times10^5} \tag{7.17}$$

Expression for the buck DC-DC converter’s control to output voltage transfer function as follows;

$$\frac{V_o(s)}{d(s)}=\frac{RV_{in}}{s^2LCR+Ls+R} \tag{7.18}$$

7.7 Result & Discussion

This section contains simulation results of NBLI converter, a 250 W system demonstrated with presented DC-DC converter. System is validated in MATLAB/ Simulink.

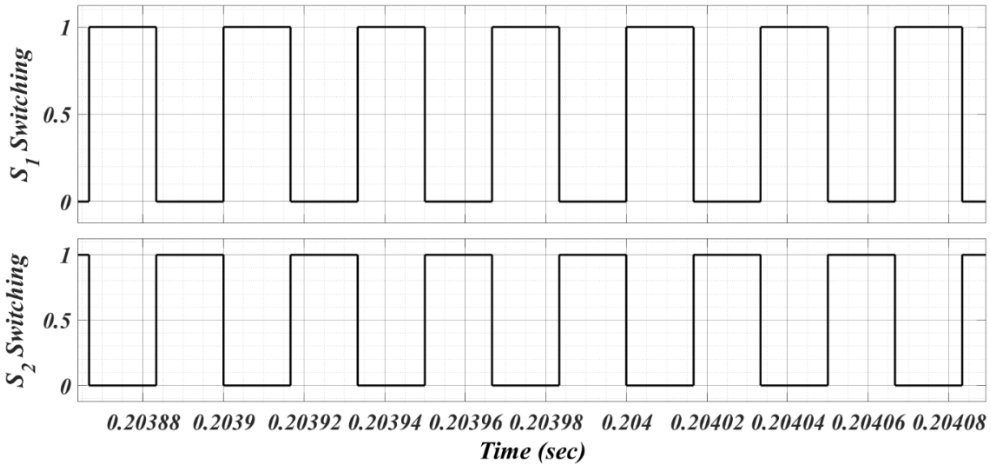

Fig. 7.10 Switching operation of active switches S_1 and S_2

Here, in this configuration both the active switches S_1 and S_2 have equal operating period, duty cycle (d_1 and d_2) is 50% of period (T).

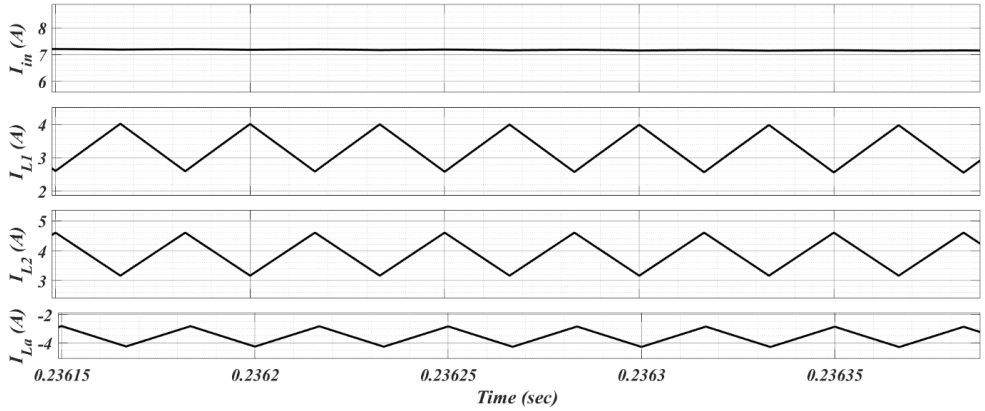

Fig. 7.11 Input Current I_{in} (A), Inductor currents I_{L1} (A), I_{L2} (A), I_{La} (A)

Here, above figure shows the inductor currents when input voltage is 22 V, Inductor currents i_{L1} and i_{L2} are observed to be 180° phase shifted.

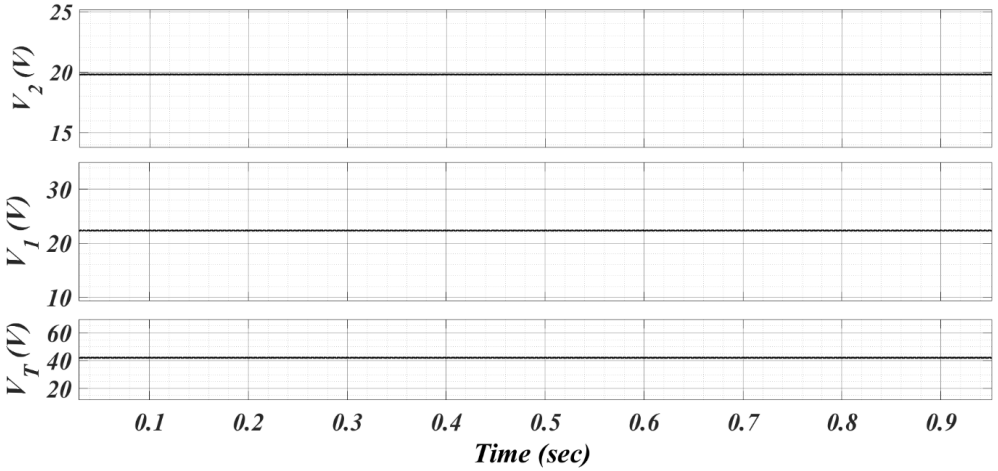

Fig. 7.12 Output voltages V_2 (V), V_1 (V), V_T (V)

The open loop control of presented control's output voltage is presented here, the voltage levels of both boost and SEPIC side converter V_2 (V), V_1 (V) are of same levels i.e. bipolar operation of converter and the total output voltage V_T (V) is addition of both V_2 (V), V_1 (V) output voltages respectively.

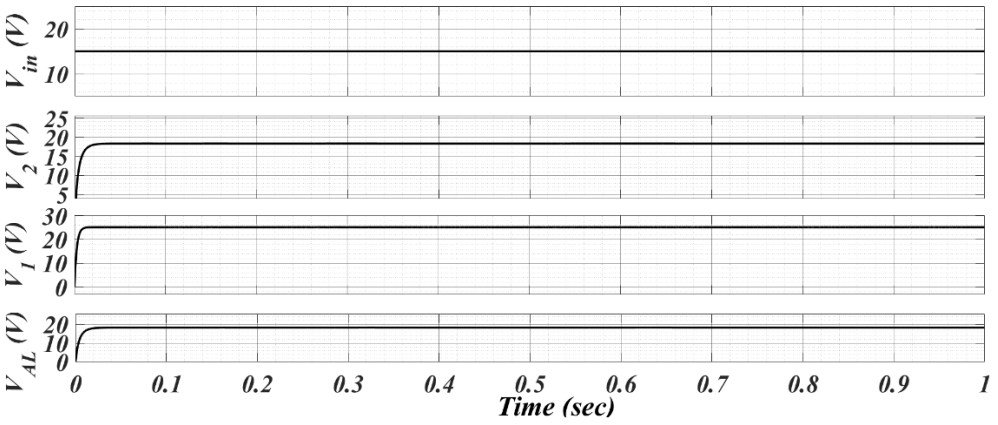

Fig. 7.13 Output voltages V_1 (V), V_2 (V) with active load V_{AL} (V)

Here, representing input voltage V_{in} (V), output voltages V_1 (V), V_2 (V) with active load i.e. buck converters output voltage V_{AL} (V).

The bode plot of G_{11} and T_{11} transfer functions are presented for control to inductor currents I_{L1} (A), I_{L2} (A).

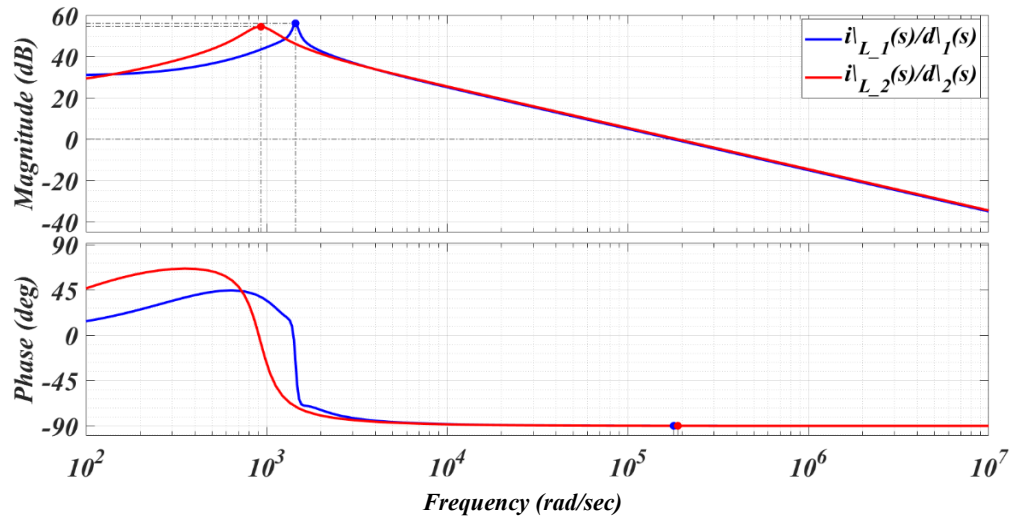

Fig. 7.14 Bode Plot of G_{11} and T_{11} Transfer Functions

Here, Gain Margin: Inf dB, Phase Margin: 90.10° at 180008.55 rad/s for transfer function (G_{11}) and Gain Margin: Inf dB and Phase Margin: 90.08° at 189704.19 rad/s for transfer function (T_{11}) respectively.

7.8 Conclusion

In order to interface an energy-storing system that is connected as an input, a boost-SEPIC combination converter is presented and examined. It is evident that the converter that is being described has minimal input current ripple. There is a 180° phase shift in inductor currents i_{L1} and i_{L2}. The duty cycle (d1 and d2) of active switches S1 and S2 is 50% of period (T), and their working periods are equal. The boost and SEPIC side converters have the identical voltage levels V_2 (V) and V_1 (V), indicating that the converter operates bipolarly. The total output voltage (V_T (V) is the sum of the V_2 (V) and V_1 (V) output voltages. Phase margin for transfer function G_{11} is 90.10°, while gain margin is Inf dB. Phase margin for transfer function T_{11} is 90.08°, while gain margin is Inf dB. Switches' current stress and current ratings are low because of interleaving effect. Converter's performance is demonstrated through presentation of simulation data. To present functionality and efficacy of converter, an open loop simulation involving a buck converter and a resistive load is connected and displayed.

Chapter 8

CONCLUSION

The design, analysis, and application of sophisticated bipolar outcome DC-DC converters for bipolar low-voltage DC (LVDC) systems conclude the work that was presented. The need for dependable and effective DC distribution networks has increased due to the growing integration of energy storage systems (ESSs), RESs and contemporary electronic loads. Bipolar DC microgrids, in particular, offer notable advantages over traditional unipolar systems, including greater power transmission capability, improved reliability, and reduced voltage stress with respect to ground, enabling more flexible and efficient load integration.

The importance of voltage balancing and the role of DC-DC converters as voltage balancers were emphasized, highlighting their significance in maintaining system equilibrium amidst uneven load and source distribution. Key contributions include the development of a BBB converter and NBLI converter. The BBB converter, with its time-multiplexed control and interleaved structure, demonstrated the ability to independently regulate dual outputs with improved efficiency. The NBLI converter, on the other hand, was designed to offer high voltage gain, minimal current ripple, and improved performance for RES integration. Both converters are suitable for bipolar LVDC systems, particularly in residential and commercial settings. Further topologies, including Buck Buck-Boost and Boost-SEPIC interleaved converters, were analysed and simulated. These converters exhibit benefits like low voltage tension, reduced component count, high gain efficiency, making them ideal for compact, high-performance DC microgrids.

Overall, presented DC-DC converter designs provide a robust foundation for advancing bipolar DC distribution systems. The detailed simulation results and dynamic modelling confirm their potential in practical implementation. Outcomes of this work contributes in further research and development in energy distribution in bipolar system, particularly in the context of renewable integration and next-generation microgrid infrastructures.

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LIST OF PUBLICATION

1. V. Thakur, S. Mishra, “An Interleaved DC-DC Converter for Low Voltage Bi-Polar DC Microgrid,” *1st International Conference on Power Electronics Converters in Transportation and Energy Application* (PECTEA-2025).
   Venue: IIT Bhubaneswar, Odisha, India from 18-21 June, 2025.
   Paper ACCEPTED