

DIGITAL MOS LSI CIRCUITS DESIGN OF 4X4 6T SRAM ARRAY

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by

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I **KUNCHA AKHILESH KUMAR** Roll no: **2K23/VLS/18** hereby certify that the work which is being presented in the thesis entitled **Digital MOS LSI Circuits Design of 4X4 6T SRAM Array** in partial fulfillment of the requirements for the award of the Degree of **Master of Technology**, submitted in the Department of **Electronics and Communication**, Delhi Technological University is an authentic record of my own work carried out during the period from June 2024 to May 2025 under the supervision of **Dr. AVINASH RATRE** and **Dr. CHHAVI DHIMAN** .

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ABSTRACT

Progress in CMOS and bigger need for quick, powerful digital systems, building effective memory subsystems is now very important. Since it is both fast and stable, Static Random-Access Memory (SRAM) is still important, especially for on-chip cache systems. In this work, the schematic design and simulation of a 4×4 SRAM array are presented, all using 6-transistor (6T) cells and 130nm CMOS technology. Important elements found in the architecture include a 2×4 row decoder, precharge circuitry on the bit lines and write drivers. Initially, the design process happened and was approved with the SYMICA EDA environment at the beginning or schematic level. These parameters were evaluated by extracting read delay, write delay and Static Noise Margin (SNM) during simulation. According to the simulation, the time for reading is 0.123 ns and the time for writing is 0.254 ns. Changes in conditions do not greatly affect the SNM read, hold or write margins, with numbers of 0.34 V, 0.13 V and 0.53 V, respectively, confirming the stability and noise resistance of the storage. The study also considers the effects of changing transistor sizes and circuit arrangements on how stable, quickly operating and space-efficient SRAM is, showing you the compromises needed for best results. This work serves as a foundational study for scalable SRAM architectures and demonstrates a complete design flow suitable for integration in low-power, high-performance digital systems.

In addition, this research is in line with the SDGs set by the United Nations. Advantages obtained through semiconductor memory and innovative digital circuit design help achieve SDG 9 (Industry, Innovation and Infrastructure) directly. In addition, designing VLSI systems that consume less energy and take up less space supports SDG 12 (Responsible Consumption and Production) which leads to sustainable and environmentally friendly technology.

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LIST OF ABBREVIATIONS

SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
CMOS	Complementary Metal-Oxide Semiconductor
SNM	Static Noise Margin
VDD	Supply Voltage
W/L	Width/Length Ratio of a Transistor
EDA	Electronic Design Automation
LSI	Large Scale Integration
VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
CR	Cell Ratio
PR	Pull-up Ratio
IC	Integrated Circuit
HDL	Hardware Description Language
PCB	Printed Circuit Board
CAD	Computer-Aided Design
ASIC	Application Specific Integrated Circuit
SoC	System on Chip

CHAPTER 1

INTRODUCTION

1.1 Background

In this chapter we have discussed Semiconductor memory technologies have evolved dramatically in recent years, these advancements have been driven to satisfy the requirement and demand of a system which is quick and more resource efficient digital systems. In high-performance applications, particularly in microprocessors and embedded systems, the memory would play an decisive role for determining overall system throughput [1]. The closer and faster the memory, the lower the latency and the better the performance of the processor.

Among available memory types, Static Random-Access Memory (SRAM) is crucial and much more efficient in terms of low latency, high speed, and ease of integration with logic circuits. Unlike Dynamic RAM (DRAM), SRAM would keep its contents as long as there is continuous supply of power, without requiring refresh cycles [2]. This makes it the preferred memory for cache implementations in CPUs and various on-chip memory solutions in ASICs and SoCs.

This thesis focuses on the design, implementation, and analysis of a 4×4 SRAM array using the conventional 6-transistor (6T) cell topology, realized in 130nm CMOS technology. The simulation and validation are conducted using the SYMICA EDA tool. Key performance metrics like read delay, write delay, and Static Noise Margin (SNM) are analyzed to evaluate stability and operational efficiency.

1.2 Motivation

With technology scaling and increased integration, the memory subsystem becomes both a bottleneck and a key area of innovation. Recent trends indicate that memory can occupy nearly 50% of the total chip area in modern processors, particularly when large L1 and L2 caches are implemented [6].

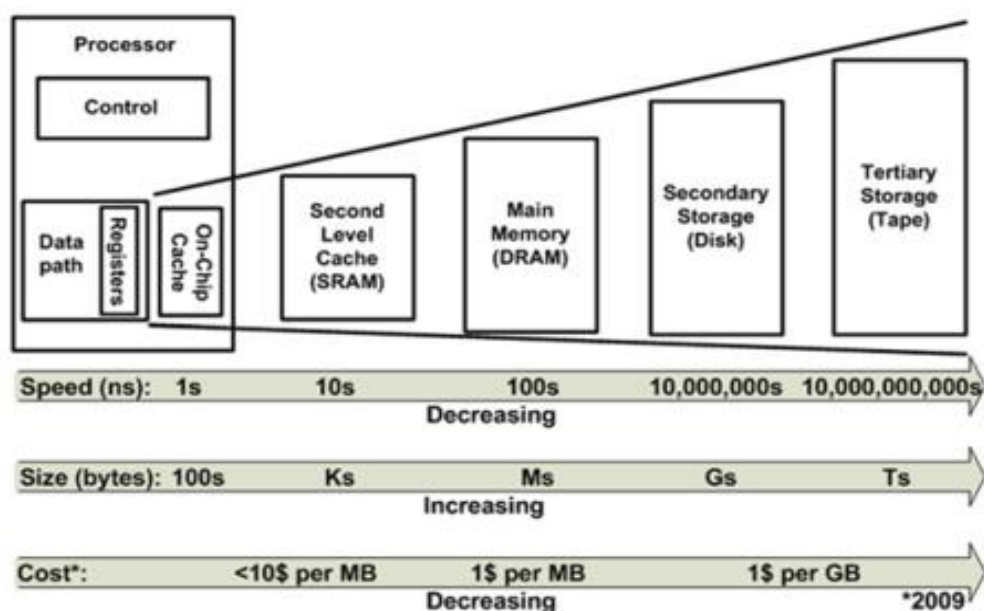


Fig. 1.1 Hierarchy of memory

The motivation behind this work stems from the need to understand how transistor sizing, cell architecture, and peripheral circuits (like decoders and precharge units) influence overall performance. By exploring the impact of different design parameters on delay and noise margins, this thesis aims to identify trade-offs that optimize both speed and stability without significantly increasing area or power.

1.3 Types of Semiconductor Memories

The memories are being classified to several types based on their access mechanisms and volatility [2]. The three major types include:

- **Random Access Memory (RAM)** — Supports arbitrary accessing to memory modules. Includes volatile memory types like SRAM and DRAM.
- **Serial Access Memory** — Supports sequential access and is typically slower. Common in applications like EEPROM.
- **Content Addressable Memory (CAM)** — Enables access based on data rather than address, useful in search applications.

RAM itself is subdivided as follows:

- Static RAM (SRAM) Uses cross-coupled inverters and does not require refresh cycles. Fast and reliable, but consumes more area [1].
- Dynamic RAM (DRAM) Stores charge on a capacitor and requires periodic refreshing. Denser and lower power but slower and less robust.

This thesis focuses solely on SRAM due to its superior access time and stability, particularly in read/write intensive applications.

1.4 Problem Statement

Though SRAM is famous for being reliable and fast, its efficiency depends greatly on things like electrical noise, sudden changes in supply voltage and errors in designing the transistors. There are three major obstacles found in designing SRAM.

1. Safeguarding against Mistakes While Accessing – When you access data, it's important to control changes due to transistor sizing [7].
2. Reducing Latency – Making the network more responsive must not decrease Static Noise Margin (SNM).
3. Use of Larger Transistors– Increasing the size of transistors stabilizes the cell, but at the cost of more silicon area and increased power [5].

In order to face these problems, this thesis introduces a 4×4 SRAM array that uses finely tuned transistor sizes as well as the necessary supporting circuitry. Through simulating the architecture, its timing characteristics and noise tolerance are carefully tested.

1.5 Objectives

To ensure that development is systematic, the thesis provides these important aims:

- Design a 6T SRAM cell in CMOS 90nm technology.
- Implement a 4×4 SRAM array using the designed cells.
- Design and integrate supporting circuits such as decoders, precharge units, and write drivers.
- Simulate read and write operations to measure delays and verify functionality.
- Analyze SNM under hold, read, and write conditions using standard methods.
- Interpret trade-offs between area, stability, and performance.

This aims further assist in meeting SDG 9 by spurring developments in digital hardware and energy-saving VLSI circuits. Besides, they contribute to SDG 4 (Quality Education) as they develop a frame that can be useful for teaching about and doing research on semiconductor memory design.

CHAPTER 2

LITERATURE STUDY

2.1 Introduction

Here we have studied how Static Random-Access Memory (SRAM) plays a very important and crucial role in high-speed digital circuits, especially in modern microprocessors and embedded systems. Unlike Dynamic RAM (DRAM), SRAM offers faster access time and does not require refresh cycles, making it suitable for cache memories and performance-critical applications. Over the decades, SRAM cell structures have evolved to achieve higher stability, lower power consumption, and improved noise margins. This chapter reviews foundational designs, scaling challenges, and architectural improvements focused on peripheral circuits that support SRAM performance.

2.2 Foundational SRAM Design

The regular 6-Transistor (6T) SRAM cell or module is being generally used for the modern-day digital systems because of their well-balanced trade off among speed, stability and area of utilization. This generally comprises a combination of cross coupled CMOS inverters which would create a bistable circuit to retain a single bit information. Also, the two NMOS access transistors are being governed by the word line would connect the cell to complementary bit lines enabling data read and write operations.

This configuration is inherently stable and because of its stable design the configuration has data retention as long as it receives uninterrupted power supply, eliminating the need for refresh cycles, unlike DRAM. Consequently, 6T SRAM is preferred for applications requiring high-speed memory, such as CPU caches and

embedded systems. However, as technology nodes scale down into the deep submicron range, the design becomes increasingly susceptible to noise, process variations, and transistor mismatches, potentially impacting the cell's noise margins and stability. As a consequence, engineering reliable CMOS technology now requires creating custom transistor sizes and choosing designs that are resistant to noise.

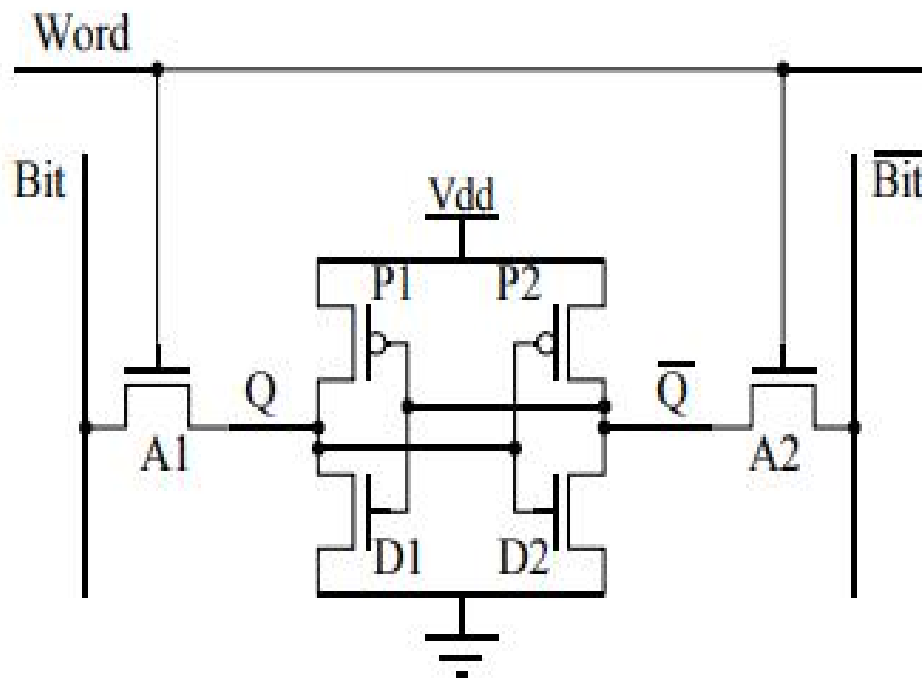


Fig. 2.1: Standard 6T SRAM cell

2.3 Precharge Circuit

For SRAM to work correctly, both read and write operations depend on bit lines. It is important for dependable and high-speed memory access that these lines are turned on with a stable and known voltage. This happens by connecting a precharge circuit to the bit line and its inverse (bit_{bar}), making sure both reach VDD voltage before the word line is switched. If this step is omitted, the voltages between the bit lines might not differ enough to correctly tell the logic being stored which may lead to errors or slower speed.

Precharging sets the bit lines in a balanced way so that exact differential detection can occur. This sensitivity helps the sense amplifier find tiny voltage rises coming from the memory cell after reading. Besides, preparing the voltage with the precharge phase cuts down on noise, makes signals stronger and more reliable and gets the memory array ready to function quickly during writing and reading.

Figure 4.1 illustrates the standard precharge circuit implemented in this work. In this configuration, PMOS transistors are used to charge both the bit and bit_bar lines up to VDD. These transistors are controlled by a clock or precharge enable signal. When this control signal is low, the PMOS devices turn ON, effectively connecting the bit lines to the positive supply and charging them. This ensures that the bit lines begin each operation at a well-defined logic high level.

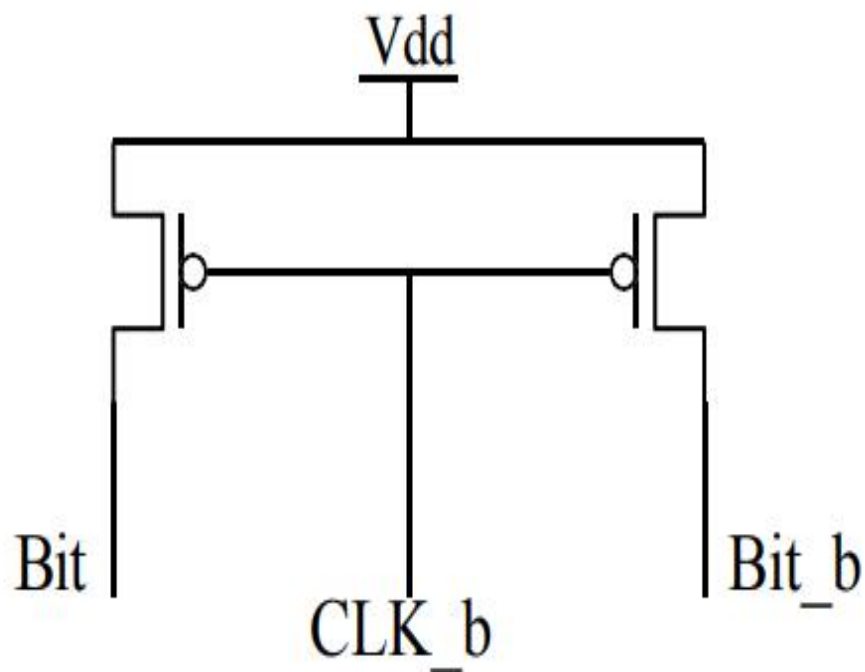


Fig.2.2: Bit Line Precharge Circuit

An alternative approach, depicted in Figure 4.2, leverages a pseudo-nMOS logic structure for precharging. In this method, a single always-ON PMOS transistor is paired with an NMOS transistor that is controlled by a clock or control signal. This configuration allows the PMOS transistor to continuously pull the bit line high, while the NMOS transistor switches the current path based on the control input. Although this technique reduces the overall transistor count and saves layout area, it introduces a significant drawback in the form of increased static power consumption. Since the PMOS remains continuously ON and the NMOS may also conduct simultaneously, a direct path for the current from the supply voltage (VDD) to ground, resulting in continuous power dissipation.

Despite the increased power overhead, pseudo-nMOS precharge circuits may be considered in area-constrained designs, especially in scenarios where speed is not a critical requirement or where higher power dissipation is acceptable. Most of the time, in advanced SRAM designs (like this thesis), the traditional precharge circuit using PMOS transistors is chosen. People use CMOS for these reasons: it runs speedily, ensures good communication between parts and does not drain current when turned off.

Generally, precharge circuits are very important in SRAM, influencing the memory's speed, how much power it consumes and the accuracy of data stored. A design may use PMOS or pseudo-nMOS primarily based on its required performance, how much area is available and how much current is needed for operation.

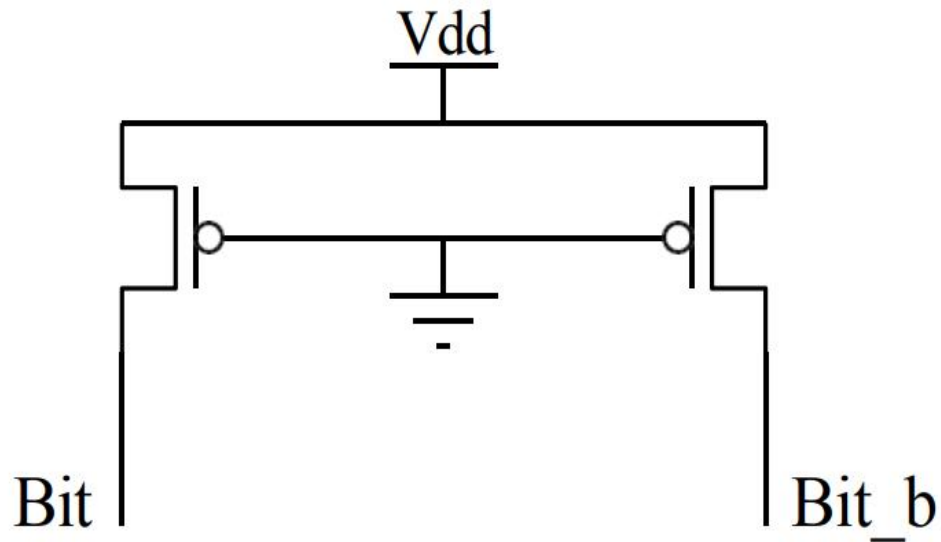


Fig. 2.3: Alternate pseudo-nMOS Precharge Circuit

2.4 Decoder Design

Rows in an SRAM array are accessed by row decoders that identify the correct word line. They mainly work by transforming binary addresses to a one-hot encoded output which ensures that only a single memory row can be active at one time. Selective activation permits the chosen word line to connect its row of SRAM cells to the bit lines, supporting either reading or writing data in that row without disturbing others. To avoid data corruption that may happen if many rows were used at once, only one row must be activated at a time.

The use of a 2×4 decoder is presented here which translates two input bits into one of four possible outputs. The six data outputs go to specific word lines which are the four rows of the 4×4 SRAM matrix. Inverters and AND gates are used to make the decoder, so it is reliable and uses less energy.

Every output from the decoder matches the state of A0 and A1 together with their inverted values which is unique for each output. Each output of the decoder is turned on when the right set of inputs is applied which follows minterm generation. This way, the SRAM array can choose exactly which row to work with. For example:

- W0 increases to high when A1 is 0 and A0 is also 0.
- Output W1 rises high when the inputs are $A1 = 0$ and $A0 = 1$.
- W2 takes a high level when A1 is 1 and A0 is 0.
- W3 goes to high if A1 is 1 and A0 is also 1.

Because of this implementation, just one decoder output is active and one word line is used to access the memory at a time. The outputs of the decoder are developed using CMOS (Complementary Metal-Oxide-Semiconductor) technology and 2-input AND gates. Every gate is made up of a PMOS pull-up network and a NMOS pull-down network. A high signal at both inputs turns on the NMOS transistors which forces the output to a high level. If only one input is active, the PMOS transistors allow the pull-down path to work, so the output voltage goes to 0V. The dual structure makes the circuit run smoothly, consume less energy and ensure the SRAM decoder operates reliably and at low power.

A decoder's output goes to one of the four rows in the SRAM array to allow for the selected memory cells to be accessed during reading and writing. A group of CMOS AND and NOT gates are used in the decoder circuit to ensure that the required address decoding is done. Fig. 3.3 draws a typical CMOS AND gate used in this decoder circuit. The appropriate sizing of these logic gates helps make sure that only the right word line is activated, without adding too much delay or causing extra electrical noise. Picking the right size memory cells ensures the device operates without problems and memory is easy to access.

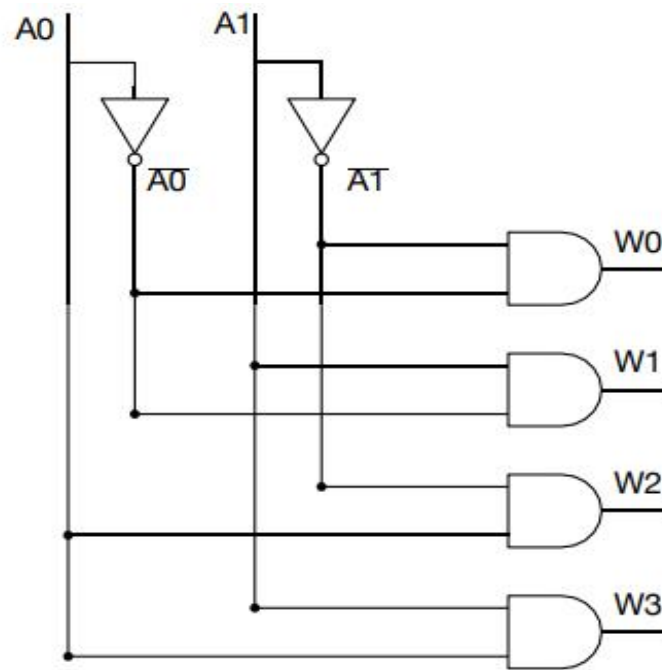


Fig. 2.4: 2×4 Decoder used for row selection

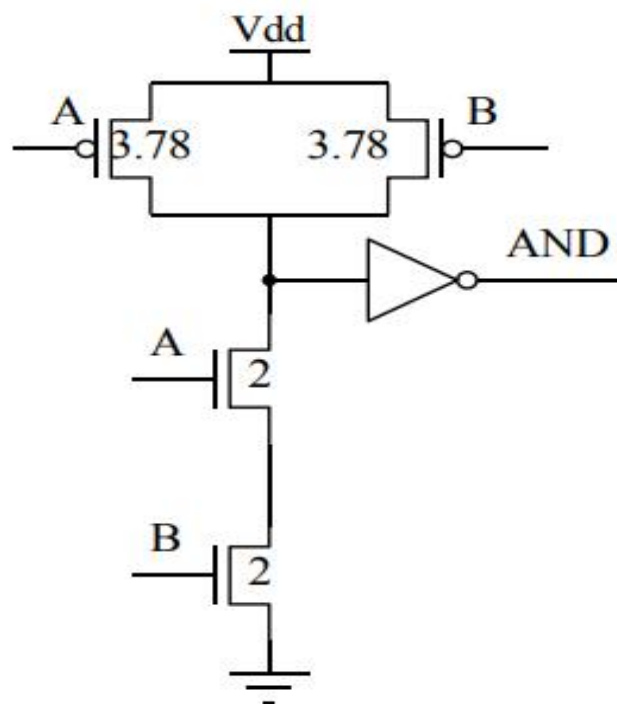


Fig 2.5: CMOS AND Gate used in decoder design

2.5 Write Driver and Column Circuitry

The column circuitry in SRAM arrays is quickly introduced here to help prepare for a more detailed look later in Chapter 4. For SRAM to work steadily and efficiently, it counts on column circuits which contain the write driver, precharge unit and sometime a sense amplifier. These items put together direct how data moves as reading or writing operations are performed. Using appropriate voltage levels on the bitlines, the writing driver completes the process of putting the intended logic value into the right memory cell. The precharge circuit plays a vital role in restoring the bitlines to a predefined voltage level (typically VDD) before a read or write operation begins, thereby enabling consistent performance and minimizing access delays. When present, the sense amplifier significantly enhances read speed by amplifying the small voltage differences on the bitlines caused by the SRAM cell's state. These circuits directly influence access time, energy consumption, and overall stability of the memory array. The design methodology and simulation results of these circuits will be elaborated in subsequent chapters, with reference to Figures 4 and 5 of the cited work to support the design rationale.

2.6 Limitations

The existing literature on SRAM design, while extensive, presents several limitations. Many studies are conducted under ideal conditions, often neglecting real-world variations such as temperature, voltage fluctuations, and process corners. Additionally, much of the research is focused at the cell level, overlooking the behavior and integration of peripheral circuits like decoders and write drivers in full SRAM arrays. Trade-offs involving power consumption, area efficiency, and performance are not always comprehensively analyzed. Furthermore, a significant number of works rely solely on schematic-level simulation without post-layout validation, which limits practical applicability. Challenges introduced by advanced technology scaling such as leakage currents and device mismatches—are

also insufficiently addressed. Lastly, benchmarking methods across different studies often lack standardization, making direct performance comparisons difficult. These limitations emphasize the necessity of a complete and realistic design methodology, which this thesis aims to fulfill.

CHAPTER 3

METHODOLOGY

3.1 Design Flow

The design and analysis of the 4×4 SRAM array in this thesis follow a structured methodology. The process begins with the transistor-level design of a single 6T SRAM cell and extends to the development of a complete 4×4 memory array with peripheral circuitry. All simulations and schematic validations are performed using the SYMICA tool and Ltspice on a 90nm CMOS technology node.

The design flow consists of the following major steps:

1. Transistor-level design of a single 6T SRAM cell.
2. Design of row decoder using a 2×4 CMOS logic structure.
3. Development of bit line precharge and write driver circuits.
4. Assembly of the complete 4×4 SRAM array with address decoding.
5. Simulation of read/write operations and noise margin analysis.

3.2 Technology and Tools Used

- Technology Node: CMOS 90nm.
- Design Tool: SYMICA (for schematic entry and transient analysis).

- Supply Voltage: $V_{DD} = 1.2V$.
- Simulation Frequency: 20 MHz for read/write operations.

This technology node was chosen for its balance between modern feature scaling and ease of simulation. It allows exploration of real-world trade-offs between noise margin, delay, and area efficiency.

3.3 SRAM Array Structure

The SRAM array implemented in this thesis is organized as a 4×4 matrix, comprising a total of 16 individual SRAM cells. These cells are systematically arranged into 4 rows and 4 columns, allowing for structured memory addressing and streamlined physical layout. Each row is said to be being associated to a dedicated line of word while the column is being connected to the pair of complementary lines of bit. This configuration facilitates efficient signal routing and supports reliable column-level operations for read and write functions. To select a specific row for access, a 2×4 decoder is employed. This decoder which is present would take the access of 2-bit input which is binary and will activate exactly one among all the four different lines word (W0 to W3) using one-hot encoding. Such selective activation ensures that only one of the given row is accessed at a given time, thereby preventing potential conflicts during memory operations. The output of the decoder directly controls the gates of the access transistors in the SRAM cells of the targeted row, enabling safe and accurate data retrieval or storage. Each column in the SRAM array shares a pair of common complementary bit lines . These bit lines serve as the data pathways for both reading and writing of operations. During read operation, voltage stored in the selected memory cell alters the differential voltage between the different bit lines . This can then be detected by external sensing circuitry, such as sense amplifiers in larger memory arrays.

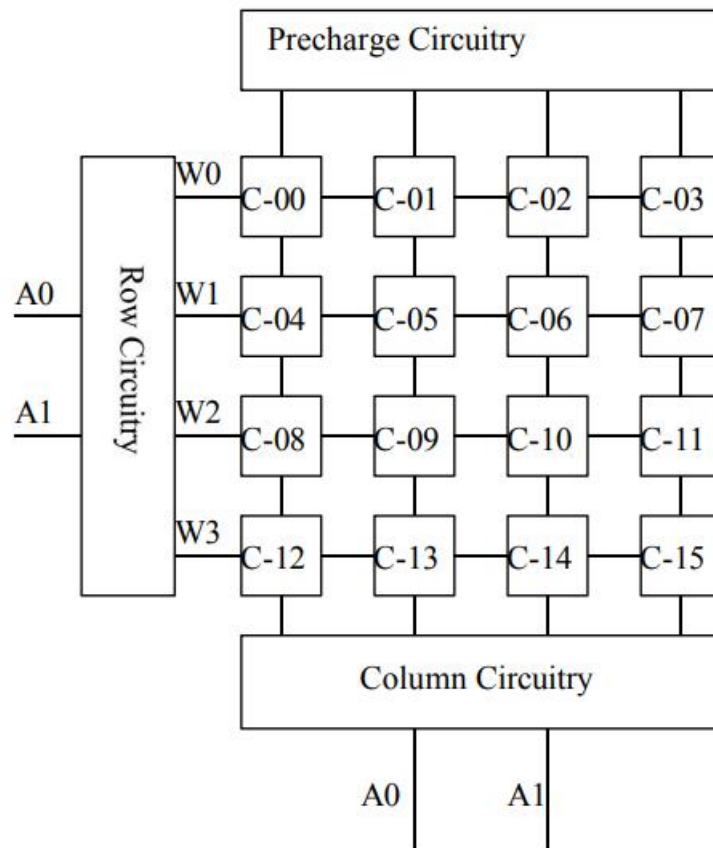


Fig. 3.1: Block diagram of the 4×4 SRAM array

In a write operation, the bit lines are driven by dedicated write driver circuits, which impose the desired logic level onto the selected memory cell, effectively overwriting its previous contents. While this thesis focuses on a 4×4 memory array, where the column logic is relatively simple, column selection logic still plays a vital role. It determines which bit line pair is active during a given operation. In larger arrays, this functionality would be handled by a column decoder in combination with multiplexers to isolate and select the desired column. However, in the 4×4 configuration used here, shared bit lines and global read/write control signals are sufficient to manage column-level operations.

The architecture supports full random access to any memory cell within the array. This is accomplished by specifying a 2-bit row address, which enables the corresponding word line through the decoder, and by using the bit lines for data input or output depending on whether a write or read operation is being performed. This

structural organization not only simplifies the simulation and testing process but also reflects the general design principles of larger SRAM arrays commonly employed in modern processor caches. Moreover, the modular nature of this design makes it inherently scalable. Additional rows and columns can be incorporated by expanding the decoder and column driver circuitry, thereby forming the basis for more extensive and practical SRAM-based memory subsystems in real-world VLSI applications.

3.4 Decoder Implementation

A 2×4 decoder is implemented using CMOS logic. The decoder takes two bits of binary input, then asserts one of four available output lines of word (W_0 to W_3). Using AND and NOT gates, these logic gates can execute the usual minterm-based decoding logic. Because of this approach, each decoder's output is only given to one input address group, so the SRAM selects the right word lines with no errors.

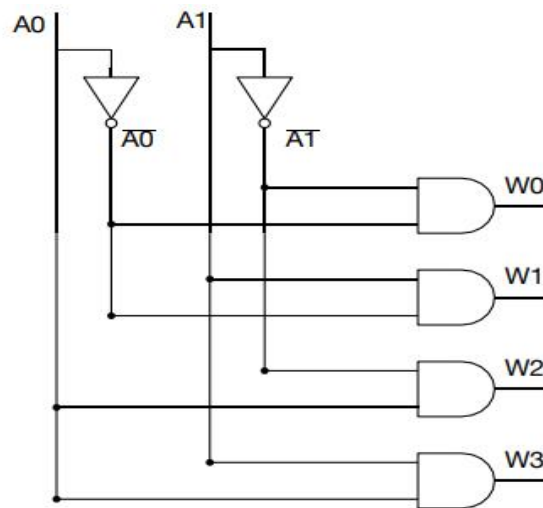


Fig. 3.2: 2×4 Decoder schematic used to enable row access

All the AND gates in the decoder are constructed with CMOS logic which has complementary pull-up and pull-down transistor networks. Such applications use CMOS logic mainly because it requires very little static power and is highly resistant

to noise which are important for reliable memory addressing. Fig. 3.3 shows the common CMOS AND gate found in a decoder.

The output of the AND gate goes high only when both input signals are high, just like minterm-based decoding demands. Each gate has to be sized in a way that provides enough drive strength to the word lines without introducing any suffering in quality or timing.

The physical row height of the decoder is the same as the height of the rows in the SRAM cells. Not only does the same structure result in orderly internal parts, but it also helps integrate with the memory easily. Bringing everything into place minimizes problems in wiring, reduces leakage in signals and raises both the data integrity and access speed.

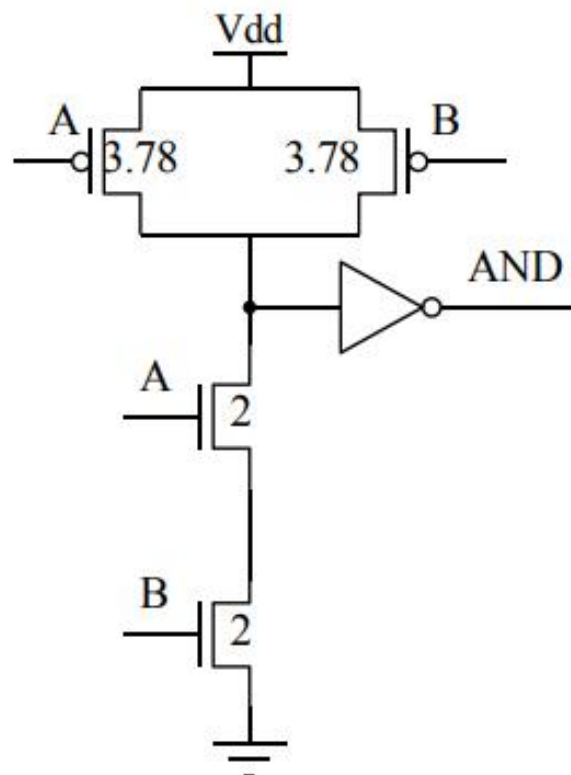


Fig. 3.3: CMOS AND Gate used in decoder logic

3.5 Transistor Sizing

How an SRAM cell behaves is strongly affected by its transistor sizes. Among the most significant factors are two design ratios, called the Cell Ratio (CR) and the Pull-up Ratio (PR). The Cell Ratio is the ratio of the width of the pull-down transistor to that of the access transistor. The read operation is mainly supported by CR, so that a higher CR makes it less likely that the stored value will get disturbed. The Pull-up Ratio, by comparison, describes the ratio between the pull-up PMOS transistor size and the access transistor size, affecting how easily the cell is programmed.

Dimensions for transistors in the design are picked to ensure good performance and stability at the same time.

The pull-up PMOS transistors have dimensions $W/L = 1\mu\text{m} / 130\text{nm}$
 Each of the NMOS devices for pull-down is set to have a ratio of $3\mu\text{m} / 130\text{nm}$.
 NMOS transistors are given default sizes of $W/L = 2\mu\text{m} / 130\text{nm}$.

The ratio of MOSFETs was designed to support success in read operations, good write operations, adequate area and acceptable power use.

3.6 Peripheral Circuit Integration

Along with the 6T memory cell, the way an SRAM array performs largely depends on its peripheral circuits. The auxiliary circuits take care of reading and writing by working with the memory cells through the bit lines. The shape and running of the machines shapes the rate, accuracy and power effectiveness of everything in the system. The design includes two important peripheral parts along every column which are the Bit Line Precharge Unit and the Write Driver Circuit.

Before a read operation starts, the Bit Line Precharge Unit sets the bit and bit-bar signals to the high voltage level (usually VDD). Charging the cell in advance makes the sensing circuit start with a known and equal voltage, making it reliable at sensing the memory cell's stored voltage when it changes just a little. It also improves how the data is transmitted and access to memory remains steady and correct.

Write Driver Circuits actively drive data onto the bit lines during a write operation. By strongly pulling one of the bit lines low (while the other remains high), the write driver overrides the stored data in the cell, ensuring that the new value is successfully written when the word line is asserted.

These components form the backbone of column-level control and are activated conditionally based on the current operation (read or write). Their design must balance strength, speed, and area—while avoiding noise coupling and minimizing delay.

During a read cycle, the precharge units are enabled at the beginning to set both bit lines to VDD. When the word line is subsequently activated, the stored value in the cell causes one of the bit lines to begin discharging, creating a detectable differential voltage. During a write cycle, the write driver sets one bit line to logic high and the other to logic low, enforcing the new data into the accessed cell through its access transistors. These peripheral blocks must be carefully designed not only to perform their functions correctly but also to avoid disturbing adjacent bit lines and rows in the array. The sizing of transistors in these units significantly influences performance metrics like write delay and read stability. The detailed schematic-level design and operation of these peripheral circuits will be presented in the next chapter.

3.7 Addressing and Read/Write Setup

Each cell in the 4×4 array is uniquely addressable using a 2-bit row address and column select logic. The complete operation flow includes:

1. Precharging the bit lines.
2. Activating a word line via decoder.
3. Writing via the write driver or reading by sensing the bit lines.
4. Read and write operations are simulated using testbenches that vary control signals (word line, write enable, data in) over a clocked timeline to analyze transient waveforms.

CHAPTER 4

DESIGN AND SIMULATION

4.1 Introduction

This chapter presents the detailed schematic-level design of the complete SRAM system. The process begins with the peripheral circuits—precharge units, write drivers, and column circuits and integrates these with the 6T SRAM cells and row decoder. The entire 4×4 SRAM array is simulated using the SYMICA tool to validate read and write functionality and evaluate delay parameters.

4.2 Precharge Circuit Design

Before initiating any kind of operation such as the read or write in an SRAM array, it is essential to bring the bit line—to a known and stable voltage. This step is crucial to ensure the accuracy and reliability of the subsequent memory access operation. The process of equalizing and charging these lines to the supply voltage level is known as precharging.

The performance of an SRAM array is tied to how its peripheral circuits are designed in addition to the 6T memory cell. Opening and closing bit lines allow the auxiliary circuits to talk to the memory cells and manage reading and writing. The efficiency, correctness and speed of the whole system are all affected by the shape and working of the machines. The internal design of every column makes use of two side tools, the Bit Line Precharge Unit and the Write Driver Circuit.

When read operation begins, the Bit Line Precharge Unit adjusts the bit and the bit-bar to be at their maximum voltage level, usually VDD. If you charge the cell in advance, the sensing circuit will begin with the same voltage and will be reliable at sensing any slight changes in the memory cell's voltage. Errors are reduced, since both data transmission and memory access are consistently improved.

As a result, the lines are being precharged to the full supply voltage level. This implementation ensures that each memory read begins with an unbiased and noise-free condition on the bit lines, allowing even small voltage differences—caused by the data being stored in accessed cell will be sensed accurately.

The precharge circuitry, although simple in its structure, plays a foundational role in maintaining the speed, correctness, and robustness of SRAM operations. In large arrays, it is typically combined with control logic to enable selective or conditional precharging, but in the 4×4 SRAM array presented here, a global and synchronous precharging approach proves sufficient and effective.

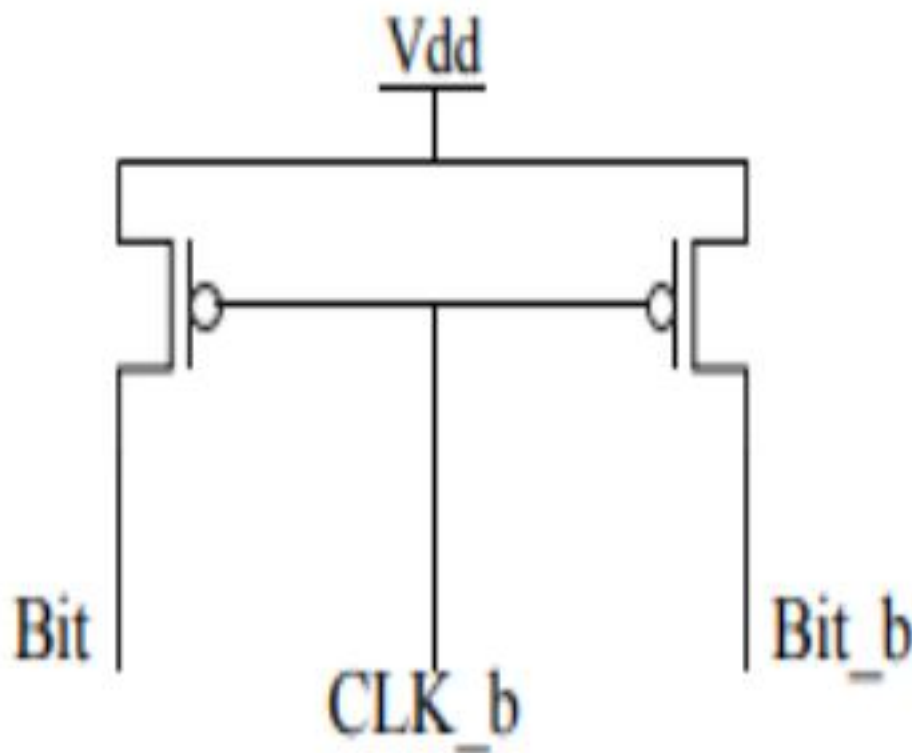


Fig. 4.1: Bit Line Precharge Circuit using PMOS switches

An alternative precharge configuration, shown in Fig. 4.2, employs a pseudo-nMOS approach. This reduces the number of transistors and overall area, though it increases static power consumption due to continuous conduction paths.

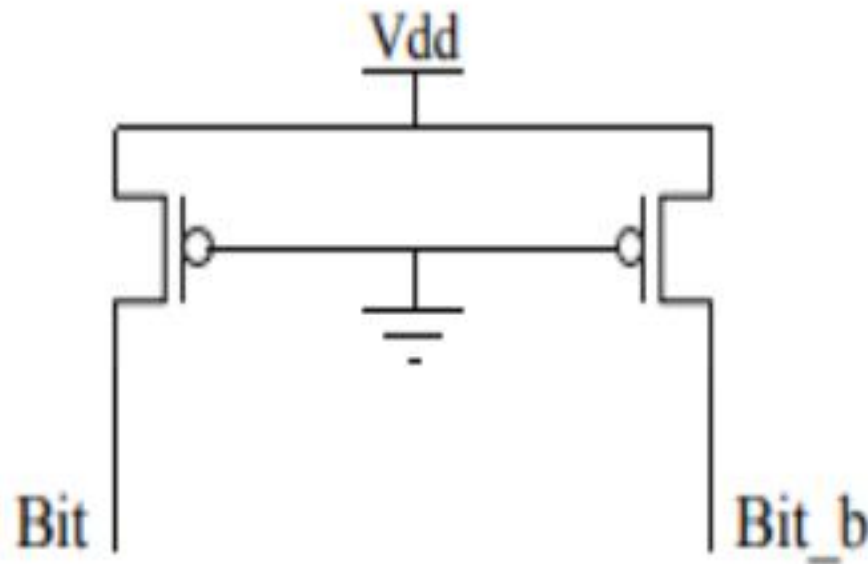


Fig. 4.2: Pseudo-nMOS based Precharge Circuit

In the current design, the standard precharge circuit was selected due to its better signal integrity and reduced noise susceptibility.

4.3 Write Driver Design

The write driver is a critical component in SRAM architecture, responsible for imposing a desired logic level on our bit lines which are there during the write function. Its primary function is to overwrite the existing value stored in the SRAM cell by applying a stronger signal than the internal cell inverters, thereby forcing the cell to change its state when the corresponding word line is activated.

In a standard 6T SRAM cell, data is held stably by cross-coupled inverters, making it naturally resistant to changes. To successfully write new data, the write driver must overcome this stable feedback loop. This is achieved by driving a strong differential signal on the bit lines pulling one line low while the other remains high depending on the input data to be written.

The write driver circuit includes MOSFET switches that are controlled by two signals: a write enable signal and the input data. When a write operation is initiated, these transistors actively drive one bit line to ground (logic '0') while the other stays at the supply voltage level (VDD), corresponding to the binary value intended to be stored.

The mechanism guarantees the voltage opposing the existing logic state of the memory cell, so the new data can be maintained. The results of the data overwrite process depend a lot on how the transistors in the write driver are sized. Correct sizing is required to have new data written successfully and rapidly, especially if the PMOS transistors connected to SRAM cells are purposely made weak to facilitate writing.

When building the design, the write driver was made to offer high drive capabilities without causing much delay. By optimizing, flexible and fast data writing is achieved without affecting the security of the whole memory array. When the clock speed is high or the process, voltage or temperature vary (PVT), the proper performance of the write driver becomes extra important.

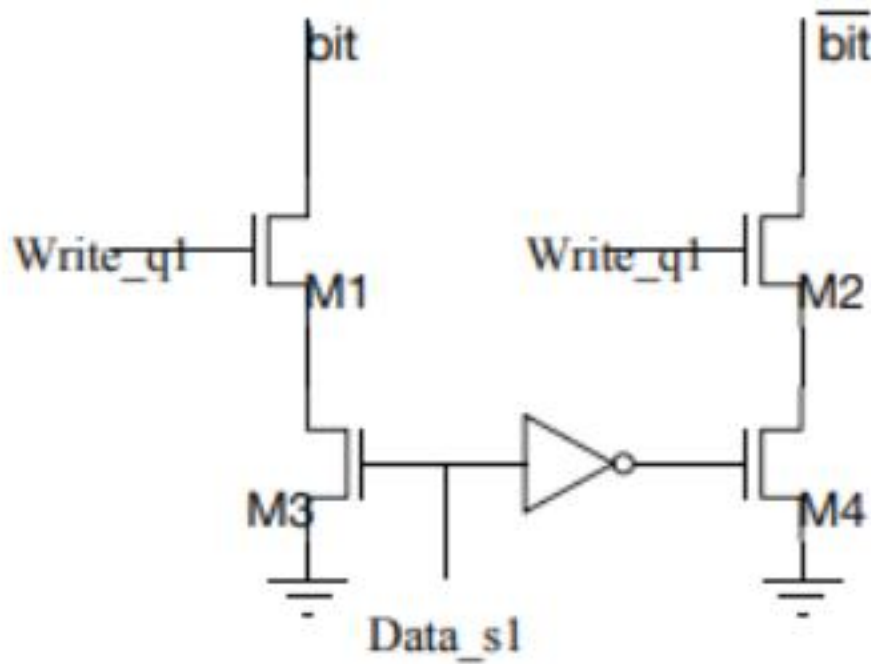


Fig. 4.3: Write Driver Circuit

4.4 Column Circuit Integration

In the SRAM array architecture, each column consists of a vertical path through which read and write operations are performed. Every column shares a complementary pair of bit lines namely bit and bit_ that connect all memory cells in that column. These shared lines serve as the primary medium for transferring data into and out of the selected cell during write and read operations, respectively.

To enable correct functioning, each column there is an integration of the precharge circuit along with the write driver which are present. These two sub-circuits operate conditionally based on the control signals indicating whether a read or write cycle is currently underway. During a read cycle, the precharge circuit ensures that both bit lines are initially charged to the supply voltage level (VDD),

In addition, the layout of bit lines along with the nearby circuitry maximizes the area savings. Duplicating the circuitry for all memory cells in a column lets the chip save on silicon space and results in a smaller design. The process makes circuit layout smaller and allows larger arrays to be built more easily which makes it valuable and efficient for designing everyday VLSI systems

Due to its patterned structure, the SRAM array behaves in the same way reliably and consistently, also making it simple to connect signals and arrange the chip internally. For dependable operation, every column circuit is separate from the others electrically which minimizes problems such as interference and data damage. When different rows are read one after another, this isolation keeps the signal strong and stops cross-talk from occurring.

In addition, the layout of bit lines along with the nearby circuitry maximizes the area savings. Duplicating the circuitry for all memory cells in a column lets the chip save on silicon space and results in a smaller design. The process makes circuit layout smaller and allows larger arrays to be built more easily which makes it valuable and efficient for designing everyday VLSI systems.

4.5 Simulation Setup

The SRAM array is tested using transient simulation in SYMICA. Key aspects of the setup include:

- Input testbench that asserts clock, data, and address lines.
- Word line activation using the decoder.
- Precharging followed by a read or write command.

Each operation is simulated at a clock frequency of 20 MHz, and the simulation window includes one full read and write cycle.

4.6 Read and Write Timing Measurement

Assessing the performance of designed SRAM array, timing characteristics such as read and write delays are critical. These delays directly affect how quickly data can be accessed or stored, impacting the overall speed and efficiency of the memory system.

Read Delay is defined as duration between the word line activation (when it reaches 50% of its high level) and the point where the bit line voltage drops to 50% of the supply voltage $VDDV_{DD}$. This measurement provides insight into the responsiveness of the memory during a read operation. In the simulations performed, the bit line responded rapidly, and the read delay was observed to be:

$$\text{Read Delay} = 0.873 \text{ ns} - 0.75 \text{ ns} = \mathbf{0.123 \text{ ns}}$$

This low value demonstrates the effectiveness of the access transistor sizing and precharge configuration, ensuring swift read access.

Write Delay refers to the time from the moment the word line is activated (again at 50% transition) to a point where the internal node used for storage is 50% of the final value being written. It reflects how effectively the write driver can override the existing stored value in the cell. From the simulation data:

$$\text{Write Delay} = 1.004 \text{ ns} - 0.75 \text{ ns} = \mathbf{0.254 \text{ ns}}$$

This result confirms that the write driver has sufficient strength to reliably flip the stored bit within a short time window. Together, these timing values demonstrate that the 4×4 SRAM array designed in this thesis can operate at high clock speeds with minimal latency, making it suitable for integration in high-performance digital systems.

CHAPTER 5

EXPERIMENTS AND RESULTS

5.1 Introduction

Here we will be discussing simulation outcomes of implemented 4x4 SRAM array which was focused on important performance parameters including the delay of read, delay of write and the Static Noise Margin(SNM). All results are obtained through transistor-level simulation using the SYMICA tool, targeting CMOS 90nm technology with $V_{DD} = 1.2V$.

5.2 Decoder Output Validation

The decoder circuit used in the SRAM design is validated by applying binary address inputs and observing the activation of the corresponding word lines. As depicted here in Fig. 5.1, the correct word line is asserted based on input values A0 and A1. This confirms correct operation of the 2x4 decoder under the applied address sequence, ensuring proper row selection in the SRAM array.

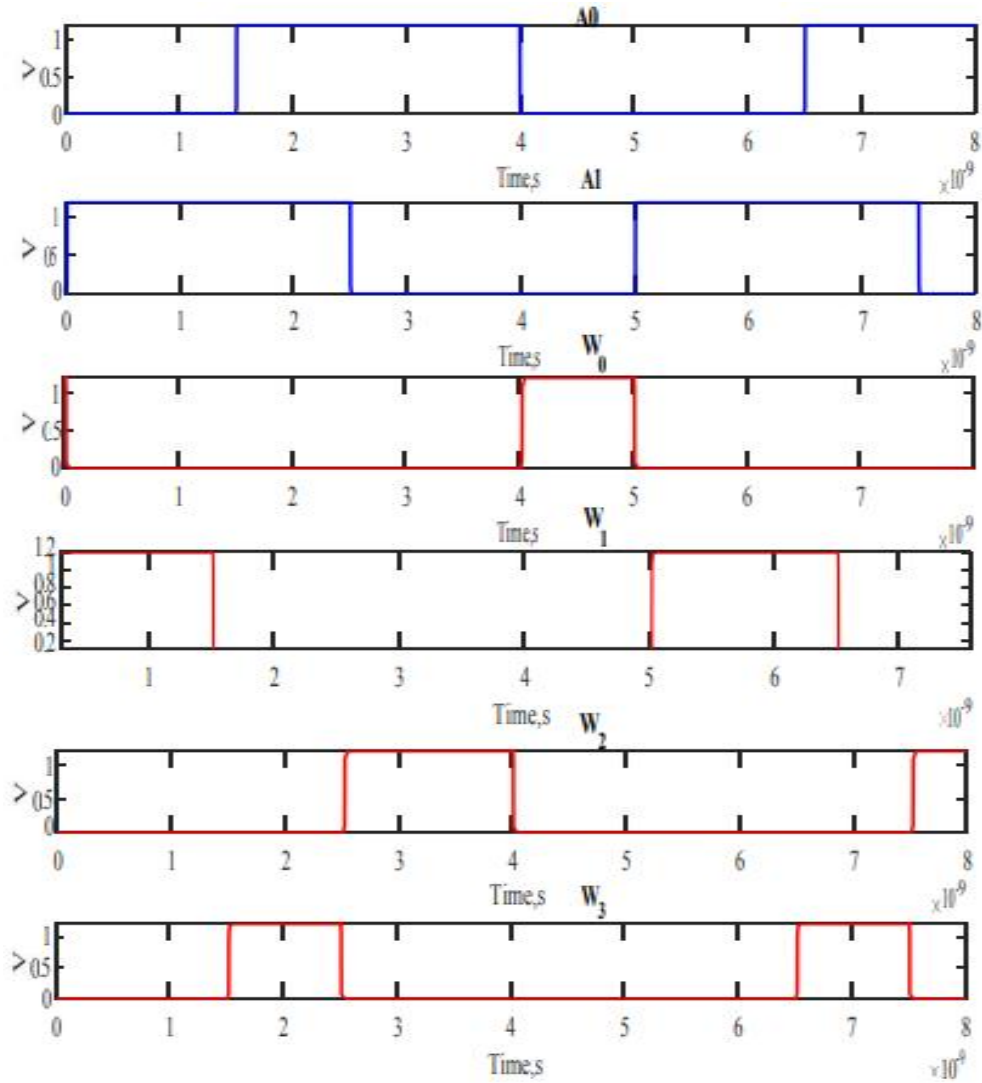


Fig. 5.1: Decoder output timing

5.3 Read Operation Analysis

To simulate the operation of read here the lines of bits are initially being precharged followed by enabling word line and then monitoring the voltage changes at those bit lines and storage nodes present. The waveform shown in Fig. 5.2 confirms that the bit line is discharged correctly based on the stored value.

operation of read here the lines of bits are initially being precharged followed by enabling word line and then monitoring the voltage changes at those bit lines and storage nodes present. The waveform shown in Fig. 5.2 confirms that the bit line is discharged correctly based on the stored value.

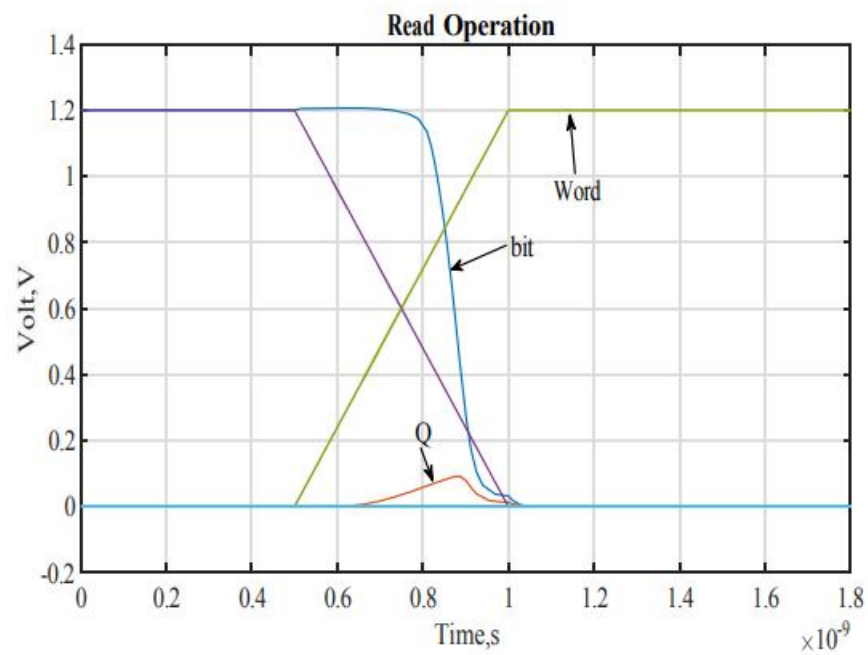


Fig. 5.2: Read operation simulation: Word line and bit line timing

The read delay is computed as the total duration taken for bit line to fall to half of V_{DD} after the word line reaches 50%. From the waveform:

$$\text{Read Delay} = 0.873 \text{ ns} - 0.75 \text{ ns} = 0.123 \text{ ns}$$

5.4 Write Operation Analysis

As depicted in Fig 5.3, the write operation would be involved in pulling one bit line to low via the write driver while keeping the word line active compelling the cell to latch new data. The delay which is being associated with writing is calculated from the moment the word line is being triggered to the point when the output node Q attains half of its desired voltage level

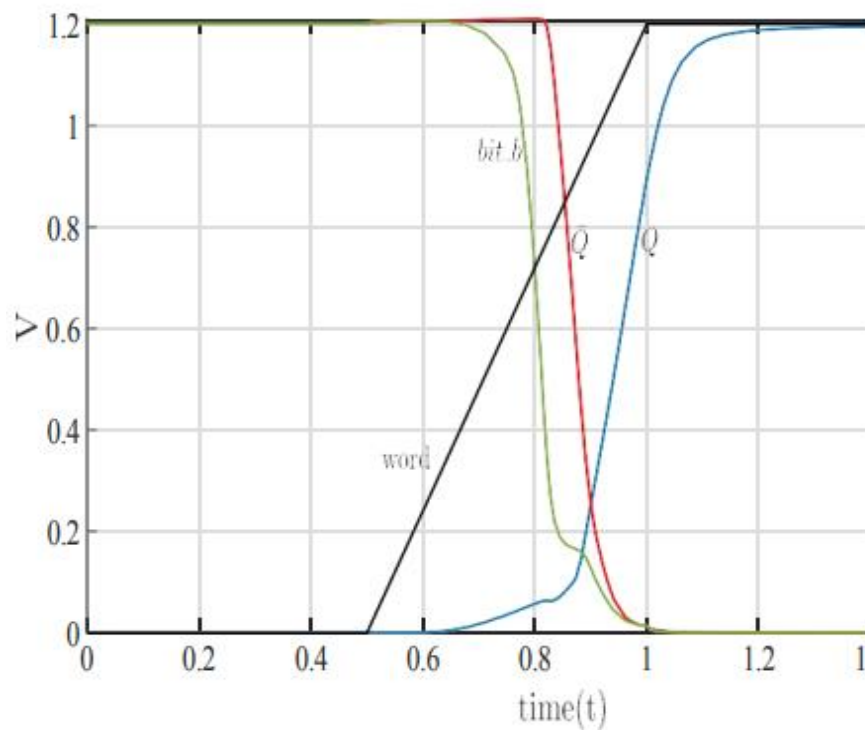


Fig. 5.3: Write operation simulation: Bit line driven low and Q node switching

5.5 Static Noise Margin (SNM) Analysis

Static Noise Margin (SNM) helps determine how stable a SRAM cell is when performing three basic functions: hold, read and write. They present the cell's ability to keep its state or change it in response to wrong electrical stimulation.

When DC noise is put at the internal nodes of the cross-coupled inverters, butterfly curves help in measuring SNM. The largest square lying within the butterfly plot's lobes represents the SNM which tells us the maximum level of interference the cell can tolerate.

5.5.1 Hold SNM

You can see the resistance of the SRAM cell to random error when it is holding information by looking at Fig. 5.4. When mirrored inverter voltage transfer curves are available, the side length of the largest square that can fit within the curves is used to calculate Static Noise Margin (SNM). The square demonstrates how stable the cell is when it is not in use because it shows the greatest amount of noise voltage that the cell can handle before changing its recorded state.

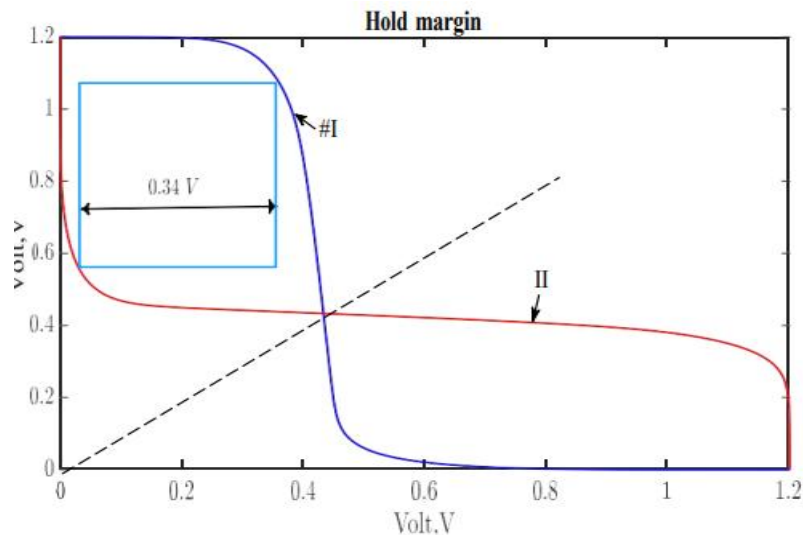


Fig. 5.4: Hold Margin SNM Plot (Measured Hold SNM: 0.34V)

5.5.2 Read SNM

During reading, first a bit line is precharged and then it is connected to the interior nodes of the SRAM cell. This kind of connection puts the information stored in the gate at risk of being lost since there is voltage division through the access transistors. Fig. 5.5 illustrates the SNM approach in this situation which seeks to maintain system harmony by handling the recovery of clean data.

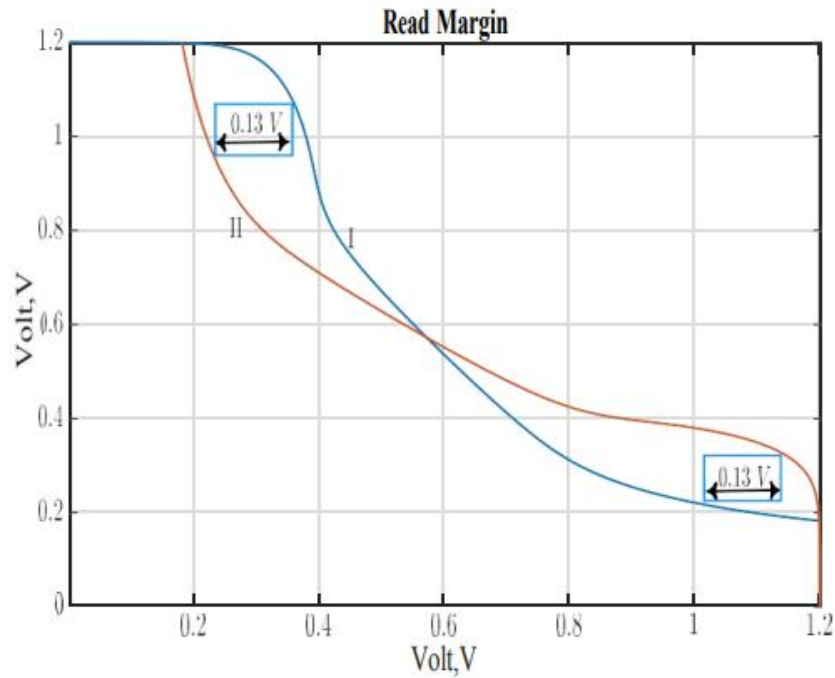


Fig. 5.5: Read Margin SNM Plot (Measured Read SNM: 0.13V)

5.5.3 Write SNM

It determines the rate at which new data can be put into the memory cell over its existing state to observe if the cell allows the new data to overwrite it. When you write a cell, the SNM plot indicates the safe range in which the cell can continue to stay written successfully (Fig. 5.6).

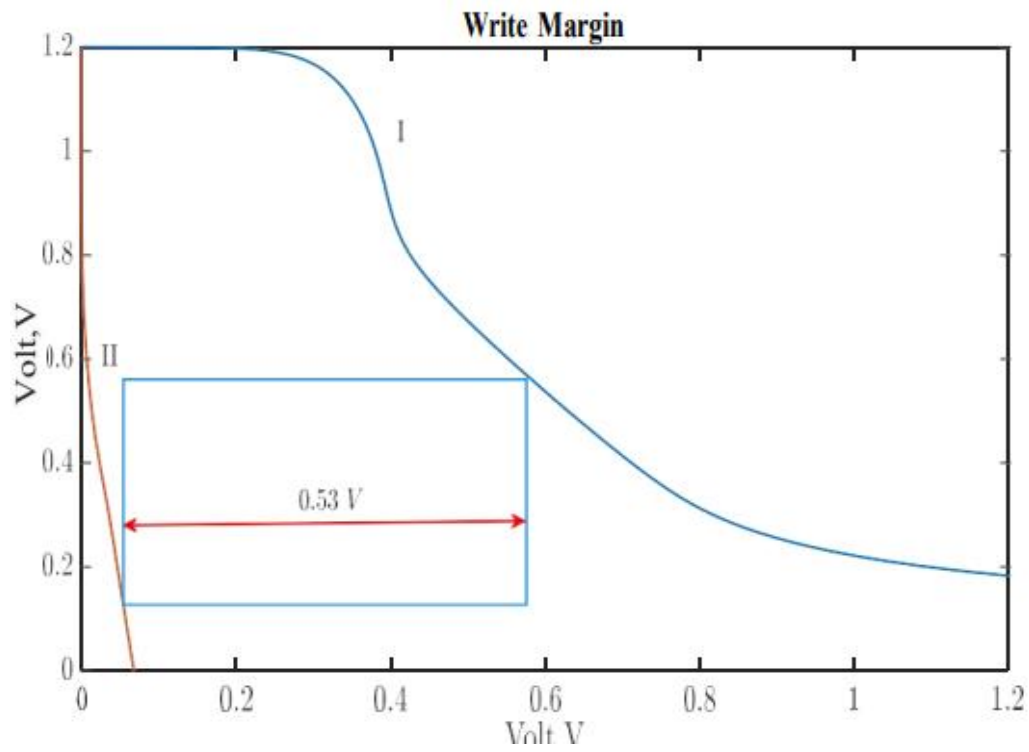


Fig. 5.6: Write Margin SNM Plot (Measured Write SNM: 0.53V)

5.6 SNM Dependence and Observations

The SNM of the SRAM cell is influenced by:

- Cell Ratio (CR): A higher CR improves read SNM but increases cell area.
- Pull-up Ratio (PR): Lower PR improves write margin.
- Supply Voltage (V_{DD}): SNM scales with V_{DD} ; increasing it improves all SNM types.
- Threshold Voltage (V_T): SNM increases with higher V_T , but temperature reduces V_T , thus lowering SNM at high temperatures.

CHAPTER 6

CONCLUSION, FUTURE WORK AND SOCIAL IMPACT

6.1 Conclusion

This thesis presented the design, simulation, and analysis of a 4×4 Static Random-Access Memory (SRAM) array using a conventional 6-transistor (6T) memory cell implemented in 130nm CMOS technology. The design was carried out at the transistor level, integrating essential peripheral circuits including a 2×4 decoder, precharge units, and write driver modules. The design objectives focused on achieving reliable operation, minimizing read/write delays, and maintaining adequate stability across all operation modes.

It brings improvements and better resources for semiconductor circuit technology which is in line with the goals of both SDG9 and SDG12 globally. Because of this research, sustainable electronics are possible which benefits SDG 13 (Climate Action) and helps move technology toward greater sustainability.

A comprehensive simulation study was conducted using the SYMICA tool. Key timing metrics were evaluated:

- Read Delay: 0.123 ns
- Write Delay: 0.254 ns

The Static Noise Margin (SNM), a critical metric for determining the robustness of SRAM cells, was evaluated in three operational modes:

- Hold SNM: 0.34 V indicating strong immunity against noise in idle conditions.
- Read SNM: 0.13 V confirming reliable read access under precharged bit line conditions.
- Write SNM: 0.53 V validating the strength of the write driver and writeability of the cell.

It was verified that the decoded output is correct and allowed the address scheme to function properly. Peripheral circuits including the bit line precharge units and write drivers demonstrated functional correctness in all test conditions. Integration of these blocks with the memory core yielded a scalable and operational 4×4 memory architecture.

Key contributions of this work include:

- Full custom transistor-level design of a 6T SRAM-based array with decoder and column circuits.
- Optimization of transistor sizing to balance speed, noise margin, and area. Simulation-based validation of read/write timing and SNM, critical for stability analysis.
- Demonstration of a complete design methodology applicable to scalable SRAM arrays.

Overall, the project achieves its design objectives and provides valuable insights into SRAM design trade-offs in submicron technologies.

6.2 Limitations

While the implemented design performs well under simulation, the following limitations are noted:

- The array size (4×4) is relatively small and not representative of real-world cache sizes.
- No layout, parasitic extraction, or post-layout simulation has been conducted.
- The design does not include sense amplifiers, which are often required in larger arrays for accurate data readout.
- Power analysis was not included in this thesis but is important for complete SRAM characterization.

6.3 Future Work

This work can be extended in several important directions:

1. **Scaling to Larger Arrays:** The current 4×4 array can be expanded to 16×16 , 64×64 , or 128×128 for practical memory blocks, with row/column decoders scaled accordingly.
2. **Incorporating Sense Amplifiers:** Future versions can include differential sense amplifiers to improve read speed and accuracy in larger arrays.
3. **Low Power Techniques:** Implementation of power-saving methods such as power gating, dynamic voltage scaling, or multi-threshold transistors to minimize leakage and dynamic power.
4. **Layout and Physical Verification:** Full custom layout design with DRC, LVS, and post-layout simulations can be performed using CAD tools like Cadence Virtuoso.
5. **Monte Carlo and Corner Analysis:** Statistical simulations to evaluate process variations and worst-case scenarios for SNM and timing.
6. **Temperature and Voltage Variations:** Additional analysis under varying temperature and V_{DD} conditions to ensure reliability across all operating environments.

6.4 Social Impact

- Helps manufacture electronics that are better for the environment and saves power in today's digital systems.
- Low-Cost Embedded Systems: Makes it possible for the Internet of Things in health, agriculture and education fields by giving access to economical memory solutions.
- Supports the rise of bespoke VLSI design expertise, adds skilled people to the industry and helps train future semiconductor workers.
- Make in India support helps improve domestic work in semiconductors in line with the country's self-reliance plans.
- Starting Point for Innovation: Sets the stage for progress in edge computing, AI and the Internet of Things for memory systems.

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EDUCATION

Year	Degree	Institute	CGPA/%
2023 - 2025	M.Tech (VLSI Design And Embedded System)	Delhi Technological University (DTU), New Delhi	7 CGPA
2014 - 2018	B.Tech (ECE)	Army Institute Of Technology (AIT), Pune	62%
2013	12 th (BIEAP)	Ascent Junior College, Vishakapatnam	84.2%
2011	10 th (CBSE)	Kendriya Vidyalaya NAD, Vishakapatnam	8.2 CGPA

ACADEMIC PROJECTS

- Digital MOS LSI Circuits Design Of 4X4 6T SRAMArray (Under Conference and Publication)** (Ongoing)
 - Designed a 4x4 SRAM array using 6T SRAM cells, focusing on enhancing speed and stability of digital systems
 - Analyzed key performance parameters like read margin, hold margin, write margin, read delay, and write delay to assess the speed and stability of the SRAM memory
 - Implemented memory access using a 2-bit address with a 2x4 decoder for efficient data retrieval.
- UART Receiver with Character Display on FPGA** (FEB 2025 - MAY 2025)
 - Developed a UART Receiver in Verilog and implemented it on an FPGA. Used RealTerm to transmit ASCII characters to the FPGA via the UART protocol.
 - The received characters were decoded and displayed on a 7-segment display, enabling real-time visualization of ASCII input
- A VERILOG-BASED MUSICAL INSTRUMENT TANPURA** (Aug 2024 - Dec 2024)
 - A Verilog implementation of the Indian musical instrument Āṇpuraū using FSM and counters/timers.
 - Modeled repeating musical notes (‘Pa2’, ‘Sa’, ‘Pa1’) with FSMs to generate a reference pitch for Indian classical music.
 - Simulated the design using Xilinx Vivado, producing cyclic musical patterns.
- SYNCHRONOUS FIFO USING VERILOG | VIVADO** (Aug 2024 - Dec 2024)
 - Designed and implemented a Synchronous FIFO (First In, First Out) memory system using Verilog to manage data storage and retrieval with precise timing control.
 - Utilized Vivado for synthesizing and simulating the FIFO design, ensuring reliable performance in high-speed data transfer applications.
- 6T SRAM | CADENCE VIRTUOSO** (Mar 2024 - Jul 2024)
 - Designed the schematic of a 6T SRAM on Cadence virtuoso.
 - Plotted the Static Noise Margin (SNM) curve, Butterfly graph, and analysed power consumption variation with temperature.
- 16x8-BIT WORDS SRAM DEVICE USING VERILOG** (Dec 2023 - Feb 2024)
 - Implemented a 16x8-bit SRAM device in Verilog with synchronous write and read operations, verified using testbenches in Xilinx Vivado.

TECHNICAL SKILLS

Category	Details
Courses	Physical Design Flow, ASIC Design Flow, Digital Electronics, Digital IC Design, Digital Design Using HDL, Static Timing Analysis (STA), Verilog, Physical Design
Extra Courses	Physical Design courses from VLSIEXPERT, Verilog, System Verilog courses from NPTEL, UDEMY
Tools	Cadence Virtuoso, Xilinx Vivado ISE, LTspice, VS Code, EDA Playground, Synopsys tools: (VCS, VERDI, SpyGlass, Design compiler)
Languages	Verilog, C, SystemVerilog (Basics), Linux

WORK EXPERIENCE & INTERNSHIP

- Training of Design and Verification - ASICGURU (Internship)** (FEB 2025 - MAY 2025)
 - Internship Training Program: Pursuing a course on design and verification using Verilog and SystemVerilog conducted by ASICGURU.com, led by SHELLY GUPTA(Founder)(ex-Synopsis) and PUNEET AGGARWAL, Senior Director of RD at Synopsys Inc.
- Internship Training Program at VLSI EXPERT RTL-to-GDSII (Internship)** (DEC 2024 - Feb 2025)
 - Physical Design Trainee: Utilized Synopsys tools to complete the RTL-to-GDSII flow, including Design Compiler for synthesis, IC Compiler II for place and route, and Prime Time for timing analysis at 32nm technology node.
- Interviewer and Evaluator (Relevel by Unacademy)** (May 2022 - 2025)
 - Worked as a freelance interviewer and evaluator at Relevel by Unacademy.
- Automation Test Engineer, ATOS, Bangalore** (Aug 2021 - Feb 2022)
 - Worked on an RPA (Robotic Process Automation) project as a BLUE PRISM Certified Developer.
 - Designed multiple value-adding business processes as a modeler.
- Automation and Manual Tester, ATOS, Bangalore** (Aug 2018 - Jul 2021)
 - Worked as a test engineer in Siemens projects, handling both manual and automation test cases.

POSITIONS OF RESPONSIBILITY

- Placement Coordinator of M.Tech VLSI:** Coordinated with students and recruiters to organize 15+ recruitment drives and workshops; expanded employer network and increased student placements significantly enhancing employability skills.
- Captain of Cricket Team:** Led the AIT College Cricket Team to win consecutive championships for three years.
- Head of Research and Development, IEEE AIT:** Conducted Self Interest Group workshops and organized competitions during the annual technical fest AKRITI.

EXTRA-CURRICULAR ACTIVITIES AND ACHIEVEMENTS

- Insta Award by ATOS (3 Times):** Recognized for resolving complex scenarios halting development projects.
- Blogging and Reading:** Blogger on Quora with over 2 million hits.
- Cricket Achievements:** Played for Karnataka State Cricket Association (Division 4).