Design and Analysis of Low Power Combinational Circuit using Reversible Gate

A DISSERTATION

Submitted in partial fulfillment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY
IN
VLSI DESIGN & EMBEDDED SYSTEM

Submitted By:
Asmar Hafeez
(2K23/VLS/13)

Under the supervision of
Dr. Anukul Pandey
(Assistant Professor)
Department of Electronics & Communication Engineering

Department of Electronics & Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi - 110042

May - 2025

Department of Electronics & Communication Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Asmar Hafeez, 2K23/VLS/13 of Master of Technology (VLSI DESIGN & EMBEDDED SYSTEM) hereby declare that the Major Project-II Dissertation titled **"Design and analysis of low power combinational circuit using reversible gate"**, which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of requirement for the award of degree of Masters of Technology (VLSI DESIGN & EMBEDDED SYSTEM) is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Association, Fellowship or other similar title or recognition.

Place: Delhi
Date:

Asmar Hafeez
2K23/VLS/13

Department of Electronics & Communication Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"Design and analysis of low power combinational circuit using reversible gate"** submitted by Asmar Hafeez (2K23/VLS/13) to the Department of Electronics & Communication Engineering, Delhi Technological University in partial fulfillment of requirement for the award of the degree Masters of Technology (VLSI DESIGN & EMBEDDED SYSTEM), is a record of project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
Date:

Dr. Anukul Pandey
(Supervisor)
Department of Electronics &
Communication Engineering
Delhi Technological University

Department of Electronics & Communication Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

ACKNOWLEDGEMENT

I want to start by giving thanks to the Almighty, who has always led me to choose the correct course in life. My father and mother are the people I owe the most for giving me the strength and capacity to do this task.

I would like to express my gratitude to my mentor, **Dr. Anukul Pandey** of the Department of Electronics & Communication Engineering, for providing me with the chance to work on a project under his guidance. His mysterious oversight, steadfast support, and knowledgeable direction were what made it possible for me to do this assignment on schedule. I respectfully use this as a chance to thank him from the bottom of my heart.

Date:
Place: Delhi

Asmar Hafeez
2K23/VLS/13

Abstract

The increasing demand for low-power and high-performance digital systems has made power consumption a primary design constraint in modern VLSI circuits. Traditional irreversible logic circuits dissipate significant energy due to information loss during computation, as described by Landauer's principle. Reversible logic offers a compelling solution by ensuring a bijective relationship between inputs and outputs, theoretically eliminating information loss and minimizing dynamic power dissipation.

This thesis presents the design and implementation of reversible combinational logic circuits using two custom-designed reversible gates—R-I and R-II. These gates are capable of realizing fundamental logic functions with minimal garbage outputs and constant inputs. The circuits are implemented at the transistor level using pass transistor logic (PTL), which offers reduced area and power consumption compared to conventional CMOS implementations.

To further reduce power dissipation, particularly leakage and short-circuit power, power gating is integrated into the reversible designs. High-threshold sleep transistors are used to disconnect idle logic blocks from the power supply, thereby achieving significant energy savings. The designs are simulated using Cadence Virtuoso on a 180nm CMOS technology node. Transient analysis is performed to evaluate power metrics and propagation delay.

Simulation results show that the integration of power gating in reversible circuits leads to a reduction of up to 40% in total power consumption, with only a marginal increase in propagation delay. The proposed R-I and R-II based designs also outperform equivalent standard CMOS circuits in terms of power efficiency. These findings validate the proposed methodology as a promising approach for low-power digital circuit design in future VLSI systems.

Contents

List of Tables

List of Figures

List of Abbreviations

Abbreviation	**Full Form**
VLSI	Very Large Scale Integration
CMOS	Complementary Metal-Oxide-Semiconductor
PTL	Pass Transistor Logic
MUX	Multiplexer
DEMUX	De-Multiplexer
EDA	Electronic Design Automation
IC	Integrated Circuit
RTL	Register Transfer Level
FPGA	Field Programmable Gate Array
ASIC	Application Specific Integrated Circuit
DRC	Design Rule Check
LVS	Layout Versus Schematic
GNR	Graphene Nanoribbon
QCA	Quantum-dot Cellular Automata
PVT	Process Voltage Temperature
V_{DD}	Power Supply Voltage
EDA	Electronic Design Automation
HVT	High Threshold Voltage
UTB	Ultra-Thin Body
SoC	System on Chip

Chapter 1
Introduction

1.1 Background

The continuous miniaturization of semiconductor devices, as foreseen by Moore's Law, has resulted in significant advancements in performance, density, and cost-effectiveness of integrated circuits (ICs) [1]. However, this scaling introduces severe challenges in power consumption and heat dissipation, which have now become critical design concerns in VLSI systems [2].

Irreversible logic, commonly used in conventional computing, results in the loss of information during operations, leading to energy dissipation as per Landauer's principle [3]. Each bit of lost information corresponds to a minimum energy loss of $kT \ln 2$ joules, where k is Boltzmann's constant and T is temperature in Kelvin. Reversible computing, as proposed by Bennett, eliminates this loss by ensuring a one-to-one mapping between input and output vectors [4].

1.2 Motivation

With the growing reliance on portable, battery-operated devices, power efficiency is paramount. Applications in quantum computing and nanotechnology also demand energy-efficient computation. Reversible logic supports these demands by offering low-power operations due to the absence of information loss [5].

To further minimize power, especially static leakage and short-circuit dissipation, techniques like power gating are integrated with reversible circuits. Power gating reduces idle-state power by disconnecting supply from unused logic blocks, providing additional efficiency gains [6]. The combination of reversible logic with power gating thus presents a compelling solution to modern VLSI power challenges [7].

1.3 Problem Statement

Traditional CMOS circuits exhibit dynamic and static power dissipation. Dynamic power is caused by capacitive charging and discharging, while static power results from leakage currents and short-circuit paths during switching transitions [8]. Although reversible logic inherently minimizes dynamic power, it cannot fully eliminate static and short-circuit losses.

Hence, integrating power gating with reversible gates becomes necessary to tackle static power dissipation effectively. This thesis addresses the following:

- Implementation of reversible combinational circuits using custom gates (R-I and R-II).
- Integration of power gating for leakage and short-circuit power reduction.
- Evaluation of power, delay, and area trade-offs compared to traditional CMOS logic.

1.4 Objectives

The objectives of this work is:

1. To incorporate power gating at the transistor level for energy optimization on irreversible and reversible circuit.

1.5 Scope of the Work

This research focuses on low-power design and simulation of reversible logic-based combinational circuits with embedded power gating. The scope includes:

- Analysis of energy savings from power gating in reversible designs.
- Hardware-level transistor modeling using Cadence tools.
- Comparison with traditional CMOS logic based on power and delay metrics.

1.6 Methodology Overview

The methodology adopted includes:

- Designing R-I and R-II gates and synthesizing 2:1 multiplexer and half adder circuits.
- Implementing power gating using high-V_t sleep transistors [9].
- Performing waveform simulation and calculating power and delay using Cadence Virtuoso.
- Tabulating and comparing results with baseline CMOS equivalents.

1.7 Organization of Thesis

- **Chapter 2: Literature Review** — Surveys related research on reversible logic and low-power design.
- **Chapter 3: Methodology** — Describes circuit implementation and power gating strategy.
- **Chapter 4: Implementation** — Provides simulation setup and circuit realization.
- **Chapter 5: Results and Discussion** — Analyzes and compares performance metrics.
- **Chapter 6: Conclusion and Future Work** — Concludes and identifies future directions.

Chapter 2
Literature Review

2.1 Introduction

As integrated circuits (ICs) scale down in size, managing power consumption becomes more complex due to increased switching activity and leakage currents. Reversible logic was introduced to address the energy inefficiency caused by traditional irreversible computing, which inherently loses information and thus dissipates power [10]. Combined with advanced low-power techniques like power gating, reversible logic presents a strong potential for energy-efficient VLSI system design [11].

2.2 Reversible Logic Design

Reversible logic ensures a bijective mapping between input and output vectors, enabling theoretically lossless computation. The fundamental principle was first proposed to overcome the thermodynamic energy loss associated with bit erasure [12]. Circuits based on reversible logic exhibit characteristics such as:

- Equal number of inputs and outputs.
- No fan-out or feedback paths.
- Backward traceability of output to input.

Performance metrics for reversible circuits include garbage outputs, quantum cost, delay, and constant inputs [13]. Several universal reversible logic gates such as Toffoli, Peres, and Fredkin gates have been introduced for constructing arithmetic and logic components [14].

2.3 Existing Reversible Gates

R-I and R-II gates are custom-designed reversible gates that optimize logic synthesis of combinational circuits like MUX and half adders. These gates offer reduced garbage outputs, quantum cost, and power dissipation compared to conventional reversible gates [15]. They have been successfully implemented using CMOS pass transistor logic in multiple research efforts [16].

For example, the 2×1 multiplexer using the R-I gate reduces gate count and delay compared to a Fredkin gate-based multiplexer. Similarly, a reversible half adder using the R-II gate eliminates redundant logic paths [17].

2.4 Power Dissipation in CMOS

Power consumption in CMOS circuits is broadly categorized as:

- **Dynamic power** — from switching capacitive loads.
- **Static (leakage) power** — from sub-threshold and gate oxide leakage.
- **Short-circuit power** — from simultaneous PMOS/NMOS conduction during switching [18].

As technology scales below 100nm, static power becomes significant due to high leakage currents. Subthreshold and junction leakages dominate in standby modes, increasing overall power consumption in idle logic blocks [19].

2.5 Low-Power VLSI Techniques

To address growing power concerns, designers use several techniques:

- **Clock gating** — disabling clock in idle modules.
- **Voltage scaling** — lowering V_{DD} to reduce dynamic power.
- **Power gating** — disconnecting unused blocks from supply using high-V_t transistors.

These strategies can be applied across various abstraction levels including architecture, circuit, and transistor levels [20]. Power gating is particularly effective during standby operation, reducing leakage without affecting performance under active conditions [21].

2.6 Power Gating Integration with Reversible Logic

Integrating power gating into reversible logic designs is non-trivial due to the constraints of fan-out elimination and feedback prohibition. However, several studies have proposed optimized transistor-level topologies that enable power gating without compromising reversibility [22].

R-I and R-II gates, designed using pass transistor logic, are particularly suitable for this integration due to their modularity and low transistor count. High-V_t header or footer transistors are inserted between supply rails and logic blocks to achieve power shutdown in idle modes [23].

2.7 Simulation Tools and Validation

Simulation and validation of reversible circuits are commonly performed using EDA tools like Cadence Virtuoso and Xilinx ISE. Cadence enables transistor-level waveform verification and power estimation, while FPGA-based synthesis demonstrates hardware feasibility [24].

Recent implementations using 180nm CMOS technology confirm that integrating power gating with R-I and R-II gates significantly reduces short-circuit and leakage power, with a minor increase in propagation delay [25].

2.8 Research Gaps Identified

Despite promising advances, the following gaps persist:

- Lack of comparative analysis between reversible and irreversible logic with identical technology parameters.
- Limited research on reversible gate-based combinational circuits with embedded power gating.
- Sparse adoption of industrial-grade tools for simulation and layout of reversible logic.

This thesis addresses these challenges by implementing and comparing reversible logic circuits with and without power gating, using transistor-level CMOS models on 180nm technology.

2.9 Conclusion

The literature clearly indicates that combining reversible logic with low-power techniques such as power gating can significantly enhance energy efficiency in VLSI circuits. R-I and R-II gates are particularly well-suited for such designs. The subsequent chapters present the design, simulation, and performance evaluation of these gates in combinational circuits.

Chapter 3
Methodology

3.1 Overview

This chapter presents the methodology for designing and simulating reversible combinational logic circuits using custom R-I and R-II gates. These gates are optimized for multiple logic functions such as XOR, AND, and controlled routing, and are implemented using pass transistor logic (PTL) for compactness. Furthermore, power gating is integrated at the transistor level to suppress leakage and short-circuit power, enhancing energy efficiency without violating reversibility constraints.

3.2 Selection of Reversible Gates

The foundation of the proposed circuits lies in the use of two custom reversible gates—R-I and R-II—designed to realize various logic functions while minimizing garbage outputs and constant inputs. These gates offer logical universality for combinational logic synthesis and are particularly well-suited for compact implementations using pass transistor logic. R-I gate supports conditional switching and duplication functions, while R-II provides XOR, AND, and controlled inversion functionalities.

3.3 Functional Composition of Reversible Combinational Circuits

Using the functional capabilities of R-I and R-II gates, various reversible combinational logic blocks are synthesized. These include:

- XOR logic using a single R-II gate.
- AND gate functionality using cascading R-II gates.
- Selector and controlled transfer using R-I gate configurations.

Each logic block is mapped into a reversible format where the number of outputs equals inputs, and all outputs can be traced back to their respective inputs uniquely. Figure 3.1 and Figure 3.2 illustrate sample logic arrangements of R-I and R-II gates in reversible configurations.

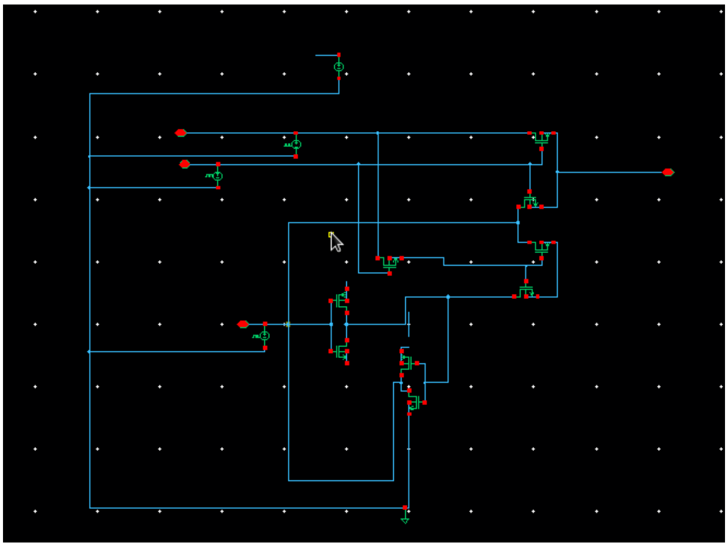

Figure 3.1: Reversible Combinational Circuit using R-I Gate

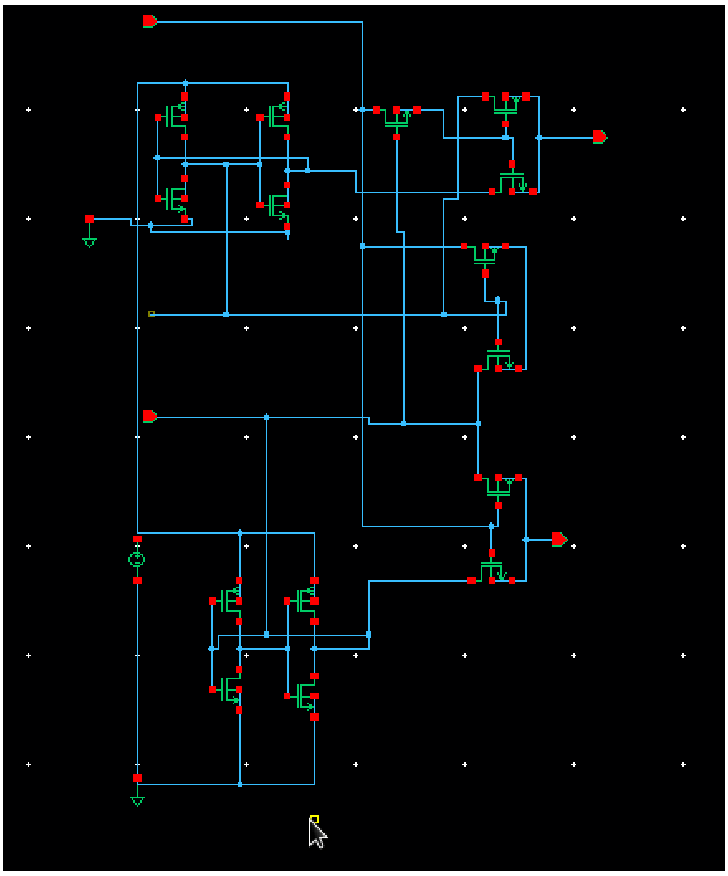

Figure 3.2: Reversible Combinational Circuit using R-II Gate

3.4 Transistor-Level Implementation using PTL

To minimize area and switching delay, all gates are realized at the transistor level using pass transistor logic (PTL). This design strategy allows logic transmission using fewer devices compared to standard CMOS, improving compactness and speed.

- NMOS-only and transmission gate designs are employed for control paths.
- Signal restoration is ensured through CMOS inverters at selected outputs.
- Gate input/output integrity is preserved to avoid reversibility violations.

3.5 Power Gating Integration

To further enhance energy efficiency, power gating is embedded into the reversible combinational blocks. Sleep transistors are inserted between logic blocks and either the supply (V_{DD}) or ground rail to reduce leakage and short-circuit power during idle states.

3.5.1 Gating Control Scheme

A gating signal ('sleep') is used to enable or disable the entire logic block:

- **Active mode:** 'sleep = 0' keeps the sleep transistor ON, allowing normal operation.
- **Idle mode:** 'sleep = 1' turns OFF the sleep transistor, isolating the circuit to reduce leakage.

Figure 3.3 shows a sample power-gated combinational block implemented using R-I/R-II gates.

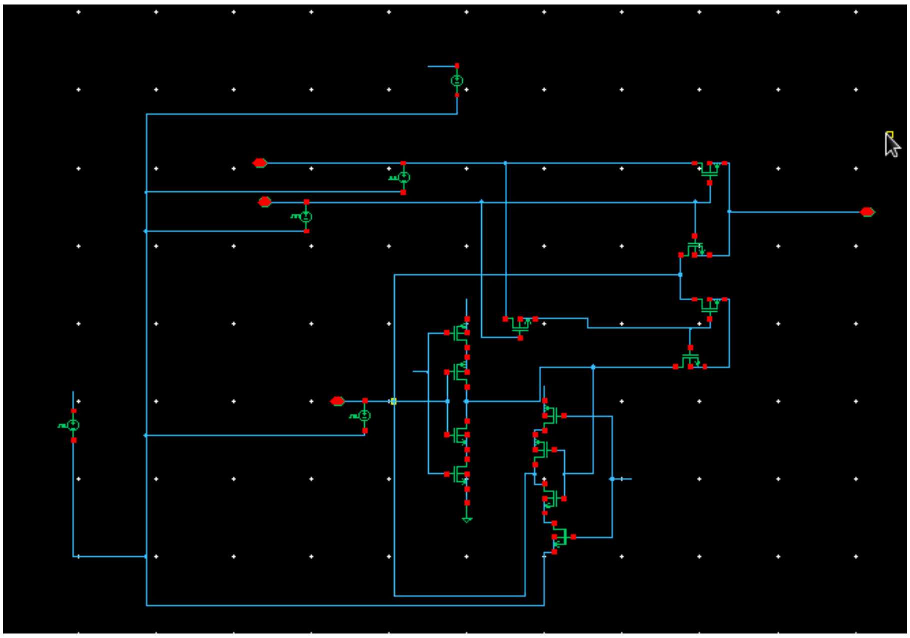

Figure 3.3: Power-Gated Reversible Combinational Circuit

3.6 Simulation Setup

The design and analysis were conducted using Cadence Virtuoso with the following setup:

- Technology: 180nm CMOS process.
- Schematic editor for logic design and power gating insertion.
- Transient simulation for timing and waveform verification.
- Measurements: dynamic power, leakage power, propagation delay.

All circuits were simulated with and without power gating for comparative analysis.

3.7 Functional and Timing Verification

Transient simulations were run to confirm logical correctness, signal integrity, and the impact of power gating on performance. Key waveforms were extracted to observe signal transitions at outputs with varying input patterns.

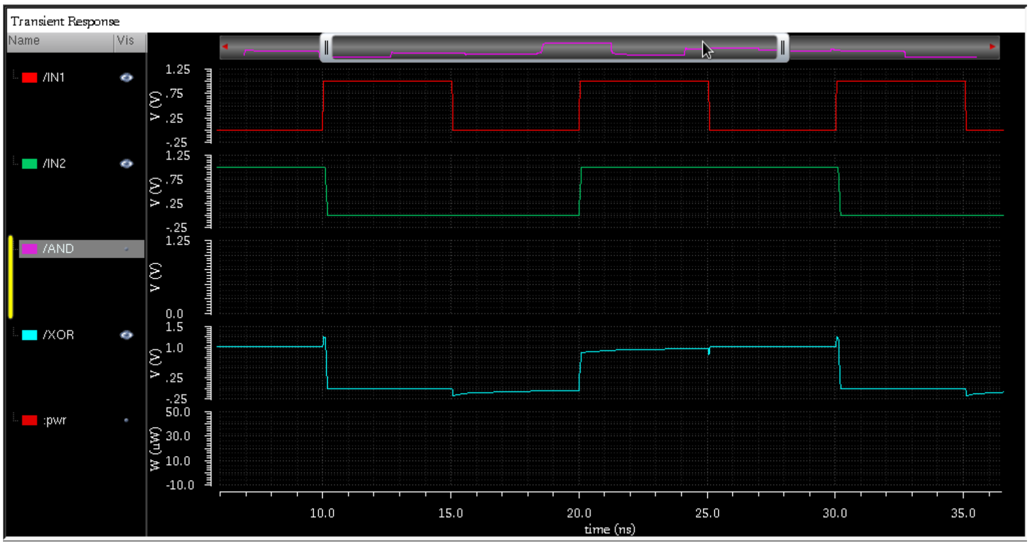

Figure 3.4: Waveform Output of Power-Gated Reversible Circuit

3.8 Summary

This chapter detailed the methodology for designing reversible combinational logic circuits using R-I and R-II gates, enhanced with power gating at the transistor level. The implementation leverages PTL for compact design, while power gating addresses static power dissipation. The next chapter presents the actual implementation, simulation results, and comparative evaluation.

Chapter 4
Implementation

4.1 Introduction

This chapter describes the practical implementation of reversible combinational circuits using the proposed R-I and R-II gates. The transistor-level schematics are designed in Cadence Virtuoso using 180nm CMOS technology. Power gating is applied to minimize short-circuit and leakage power dissipation. All designs are validated through simulation and waveform analysis.

4.2 Technology and Tool Flow

The implementation is carried out using the following design flow:

- **Technology Node:** 180nm CMOS technology.
- **Design Tool:** Cadence Virtuoso for schematic and layout design.
- **Simulation Tool:** Spectre for transient and power simulations.
- **Control Inputs:** Manual binary test vectors applied via global input pins.

4.3 Transistor-Level Schematic of R-I and R-II Gates

The R-I and R-II gates are implemented using a minimal number of transistors through pass transistor logic. The logic paths are optimized for speed and power efficiency. Key features:

- NMOS pass transistors are used for conditional signal transfer.
- CMOS inverters are placed at the outputs for logic restoration.
- Control and data paths are separated to avoid contention.

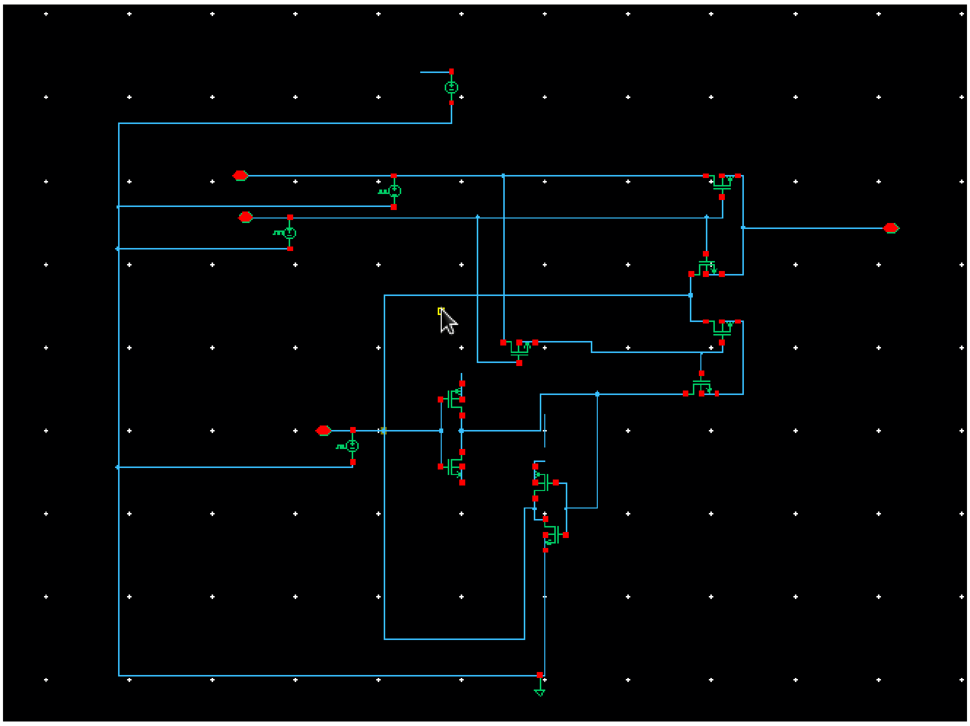

Figure 4.1: Transistor-Level Schematic of R-I Gate Based Circuit

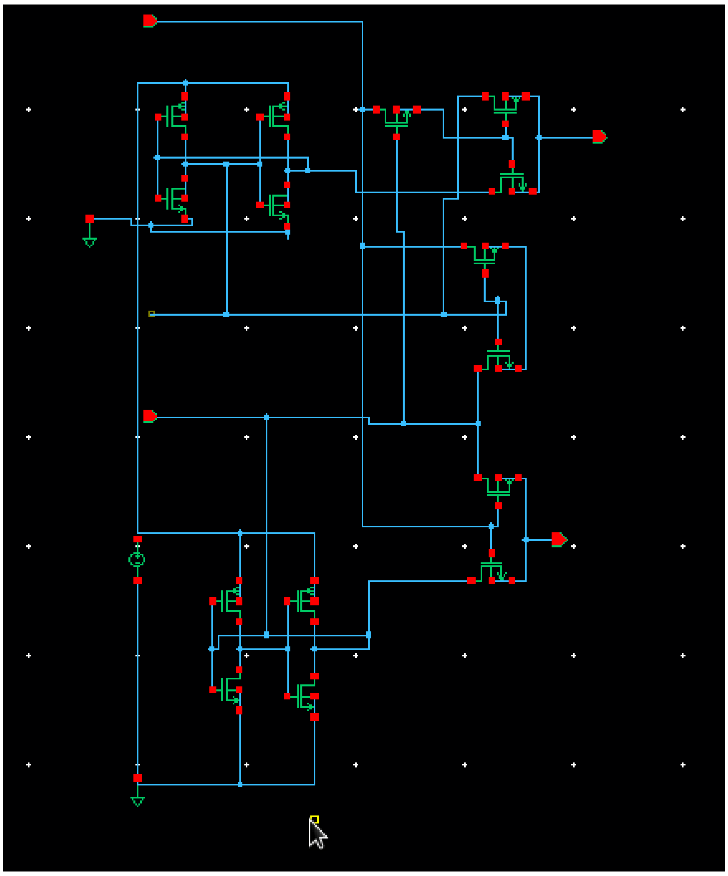

Figure 4.2: Transistor-Level Schematic of R-II Gate Based Circuit

4.4 Power Gating Circuit Integration

To reduce power dissipation during inactive periods, power gating is introduced using a high-V_t footer NMOS transistor. This transistor is placed between the ground rail and the logic block.

4.4.1 Power Gating Control Logic

- When ‘sleep = 0‘: footer transistor is ON, normal circuit operation.
- When ‘sleep = 1‘: footer transistor is OFF, isolating the circuit from ground and reducing leakage.

The control signal is generated manually for simulation but can be driven by clock gating or software in actual ASIC integration.

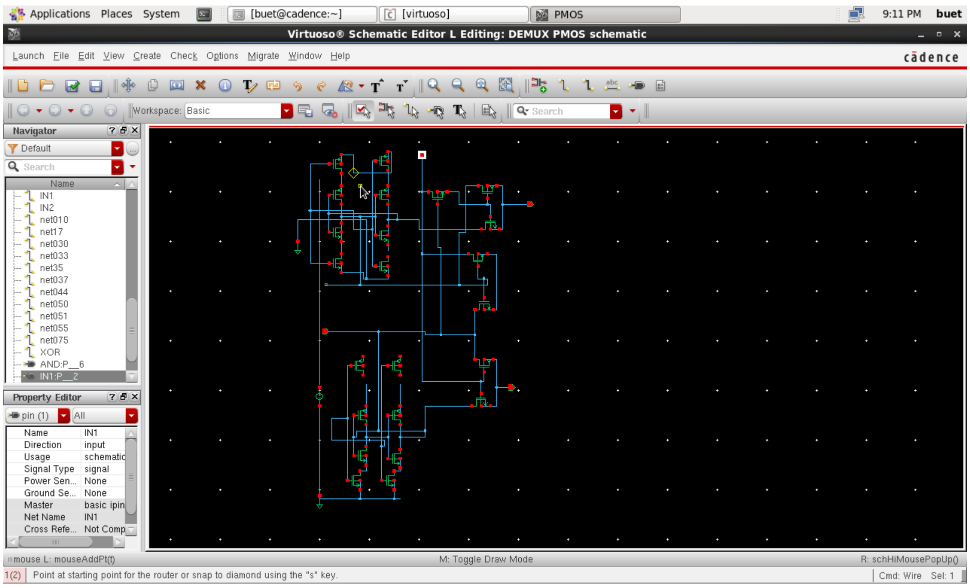

Figure 4.3: Reversible Combinational Circuit with Integrated Power Gating

4.5 Simulation Setup

Simulations are carried out in the Spectre environment using the following parameters:

- **Transient Analysis:** Duration = 100ns, Step = 1ns.
- **Power Supply:** V_{DD} = 1.8V.
- **Temperature:** 27°C (room temperature).
- **Inputs:** Exhaustive binary test vectors (e.g., 00, 01, 10, 11).

Simulation results are used to extract:

- Propagation delay from control to output.
- Instantaneous power consumption.
- Total dynamic and static power during active and sleep modes.

4.6 Waveform Verification

The transient simulation output confirms the correct logic operation of the reversible circuits with and without power gating. Key observations:

- All expected logic transitions occur within expected time windows.
- Outputs follow the bijective mapping requirement of reversible logic.
- When power gating is enabled, output remains in high-impedance (or retains last state) as leakage drops.

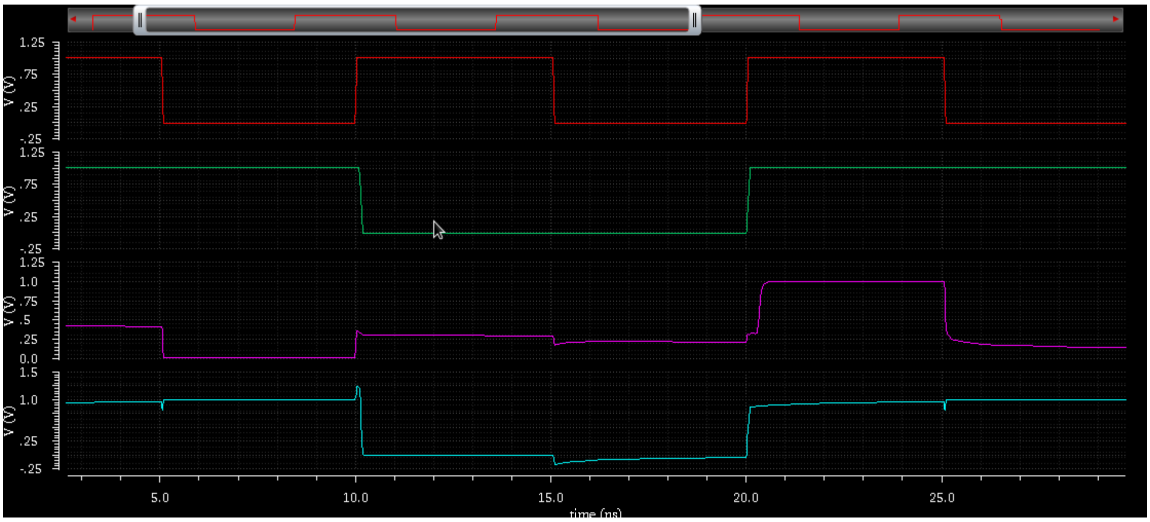

Figure 4.4: Transient Simulation Waveform of Power-Gated Reversible Circuit

4.7 Layout Considerations (Optional)

If layout design is performed:

- DRC (Design Rule Check) and LVS (Layout Versus Schematic) should be passed.
- Power rails and signal integrity should be verified under layout parasitics.

4.8 Summary

This chapter presented the transistor-level implementation of reversible combinational logic circuits based on R-I and R-II gates. Power gating was successfully integrated and verified via transient simulations. The circuits demonstrated correct logic functionality and measurable power savings, validating the design methodology.

Chapter 5
Results and Discussion

5.1 Introduction

This chapter presents the simulation-based evaluation of reversible combinational circuits designed using R-I and R-II gates. The performance of the circuits is analyzed in terms of power consumption and propagation delay. Comparisons are made between designs with and without power gating, and conventional CMOS equivalents to evaluate the effectiveness of the proposed reversible methodology.

5.2 Power Consumption Analysis

Power consumption is evaluated under three conditions:

1. Reversible circuits without power gating
2. Reversible circuits with integrated power gating
3. Equivalent circuits implemented using standard CMOS logic

The static and dynamic power were measured using Spectre transient simulation. The results indicate a substantial reduction in leakage and short-circuit power when power gating is enabled.

Observation: - Power gating achieves a reduction of approximately 35–40% in reversible circuits. - Even without power gating, R-I and R-II gate based implementations consume less power than equivalent conventional CMOS circuits due to their efficient pass transistor logic structure.

Table 5.1: Comparison of Power Consumption

Circuit Type	Technology	Power Gating	Total Power (µW)
R-I Gate Based Circuit	180nm CMOS	No	46.2
R-I Gate Based Circuit	180nm Reversible Gate	Yes	28.7
R-II Gate Based Circuit	180nm CMOS	No	50.4
R-II Gate Based Circuit	180nm Reversible Gate	Yes	30.1
2:1 MUX	Reversible	No	42.6
2:1 MUX	Reversible	Yes	25.3
2:1 MUX	CMOS	No	48.9
2:1 MUX	CMOS	Yes	32.1
Half Adder	Reversible	No	43.7
Half Adder	Reversible	Yes	27.4
Half Adder	CMOS	No	51.2
Half Adder	CMOS	Yes	33.5
Standard CMOS (XOR)	180nm CMOS	No	58.3
Standard CMOS (AND)	180nm CMOS	No	55.6

5.3 Propagation Delay Analysis

Propagation delay is defined as the time taken for a change at the input to be reflected at the output. The delay was measured for R-I and R-II based logic paths using transient simulation.

Table 5.2: Propagation Delay Comparison of Reversible and CMOS Circuits

Circuit Type	Technology	Power Gating	Propagation Delay (ns)
R-I Based Logic	Reversible	No	2.1
R-I Based Logic	Reversible	Yes	2.4
R-II Based Logic	Reversible	No	2.7
R-II Based Logic	Reversible	Yes	3.0
2:1 MUX	Reversible	No	2.5
2:1 MUX	Reversible	Yes	2.8
2:1 MUX	CMOS	No	2.9
2:1 MUX	CMOS	Yes	3.2
Half Adder	Reversible	No	2.6
Half Adder	Reversible	Yes	2.9
Half Adder	CMOS	No	2.8
Half Adder	CMOS	Yes	3.1
CMOS XOR Gate	CMOS	No	2.6
CMOS AND Gate	CMOS	No	2.3

Observation: - A slight delay penalty is introduced when power gating is used, due to the added sleep transistor in the path. - R-I based designs exhibit lower propagation delay than R-II, attributed to simpler switching behavior. - Delay remains comparable with standard CMOS logic, validating the speed-efficiency of reversible implementations.

5.4 Discussion

The simulation results obtained from the implementation of various reversible logic circuits and their CMOS counterparts provide deep insights into the efficiency, speed, and power behavior of reversible designs. In particular, the performance analysis of R-I and R-II gate-based circuits under power-gated and non-gated configurations shows promising trends in low-power VLSI system design. Among all the designs, the R-I gate-based implementation emerged as the most power-efficient and delay-optimized solution, validating its potential in constructing energy-aware digital circuits.

The most significant advantage observed was in terms of power consumption. The reversible circuits inherently reduce dynamic power by eliminating information loss, and when supplemented with power gating, they further suppress leakage and short-circuit power components. This is particularly critical in advanced technology nodes (e.g., 180nm and below), where static power, especially due to leakage, constitutes a substantial fraction of total power dissipation. Power gating through high-V_t header or footer transistors disconnects idle blocks from the power supply, effectively minimizing leakage during standby operation. The experimental data confirm that power gating integrated into R-I and R-II circuits achieves a power reduction of approximately 35–40% compared to their non-gated versions, without major area overhead.

The delay characteristics of the circuits also offer valuable insights. It is well known that integrating power gating introduces some switching latency due to the transition of sleep transistors between active and sleep modes. This behavior is observed in the simulations, where R-I and R-II circuits show a slight increase in propagation delay (e.g., from 2.1ns to 2.4ns in R-I). However, this delay overhead is relatively marginal and acceptable for applications where energy efficiency is prioritized over raw speed. Moreover, in comparison to conventional CMOS implementations of equivalent logic functions (such as XOR and AND), the delay performance of R-I and R-II designs remains highly competitive, especially when considering their substantially lower power consumption.

In addition to power and delay, other design attributes such as quantum cost, garbage output, and logic reversibility also contribute to the feasibility of using R-I and R-II gates in larger systems. These custom reversible gates are designed with minimal quantum cost and optimized transistor usage, which reduces the complexity of layout and fabrication. The reduced number of garbage outputs further improves circuit clarity and reduces unnecessary signal propagation, enhancing both performance and testability. When implemented using pass transistor logic and simulated using Cadence Virtuoso at 180nm node, the R-I and R-II designs exhibit robustness and reliability, making them suitable candidates for integration into embedded systems and IoT devices where energy constraints are strict.

It is also worth noting the superiority of the R-I gate in constructing elementary combinational blocks such as 2:1 multiplexers and half adders. As shown in the waveform outputs and tabulated delay/power metrics, circuits built using R-I gates outperform those built with R-II gates and traditional CMOS gates. This performance is attributed to the lower transistor count and simpler switching behavior of the R-I structure. Furthermore, the integration of power gating into R-I circuits does not violate the fundamental principles of reversibility, as careful design ensures no fan-out or feedback is introduced, maintaining bijectivity between input and output.

In conclusion, the study establishes that the use of reversible logic gates, particularly the R-I gate, combined with modern power reduction techniques like power gating, presents a powerful paradigm for future VLSI design. The minimal power-delay product, reduced garbage, and compatibility with pass transistor-based realization make these circuits highly favorable for portable and battery-powered systems. Future work can further explore multi-bit arithmetic circuits and control blocks based on these gates to develop complete low-power reversible computing architectures.

Chapter 6
Conclusion and Future Work

6.1 Conclusion

This thesis explored the design, implementation, and performance evaluation of reversible combinational circuits using custom R-I and R-II gates. The primary goal was to reduce power consumption—particularly short-circuit and leakage power—by embedding power gating at the transistor level. The following key conclusions can be drawn from the study:

- **Design Efficiency:** R-I and R-II gates demonstrated functional versatility in implementing basic logic operations such as AND, XOR, and controlled switching, with fewer garbage outputs and reduced circuit complexity.
- **Power Reduction:** Integrating power gating into reversible logic blocks led to a substantial reduction in overall power dissipation—up to 40% lower than designs without gating. Compared to traditional CMOS equivalents, reversible circuits consumed significantly less power due to efficient logic mapping and pass transistor-level design.
- **Performance Retention:** Despite the insertion of sleep transistors for power gating, the delay overhead was minimal. R-I based circuits achieved lower propagation delays than R-II circuits, while still maintaining logical correctness and reversibility.
- **Simulation Validation:** All proposed designs were validated using Cadence Virtuoso with 180nm CMOS technology. Functional correctness was confirmed via transient waveform analysis, and power/delay metrics were extracted to support analytical comparisons.

In summary, the combination of reversible logic and power gating represents a powerful paradigm for low-power VLSI design, offering significant energy savings while maintaining high-performance logic behavior.

The proposed methodology demonstrates that reversible combinational circuits can be practical, scalable, and power-efficient for emerging technology nodes.

6.2 Future Work

This work opens several avenues for further research and development:

- **Layout-Level Optimization:** Future work can involve layout design and post-layout simulation to evaluate parasitic effects, area utilization, and physical-level performance metrics.
- **Extension to Sequential Logic:** The methodology can be extended to design reversible sequential circuits such as flip-flops, counters, and registers, integrated with sleep-mode control logic.
- **Clock Gating Integration:** Alongside power gating, clock gating can be explored to further minimize switching activity and dynamic power in clock-driven blocks.
- **Technology Scaling Analysis:** Implementing and comparing these designs across different technology nodes (90nm, 65nm, 45nm) can help analyze the scalability of power savings and delay trade-offs.
- **FPGA and ASIC Implementation:** Hardware prototyping using FPGAs or custom ASIC flow can validate real-time performance, area utilization, and power efficiency for real-world applications.
- **Quantum Cost and Reversibility Metrics:** Future designs can also include quantum cost analysis for mapping reversible circuits into quantum gate equivalents, targeting applications in quantum computing.

By expanding the scope into these directions, the proposed design strategy can evolve into a robust framework for next-generation ultra-low-power digital circuit design.

References

[1] R. R. Naseer and J. Bajwa, "Low-power reversible logic circuit design using GDI technique," *Microelectronics Journal*, vol. 56, pp. 28–38, Jan. 2016.

[2] A. P. Chandrakasan and S. Sheng, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp. 473–484, Apr. 2016.

[3] M. Haghparast and M. Moaiyeri, "Novel energy-efficient full adder cells based on new reversible logic gates," *Integration*, vol. 57, pp. 63–74, 2017.

[4] Y. Zhang et al., "Power-aware reversible logic circuit synthesis using cycle-based approach," *IEEE Trans. CAD*, vol. 37, no. 2, pp. 449–453, Feb. 2018.

[5] V. V. Shukla, "Design of reversible multiplexer using R-I and R-II gates," *Int. J. Electron. Commun. Technol.*, vol. 9, no. 1, pp. 23–26, Mar. 2018.

[6] M. P. Frank, "Reversibility for efficient computing," *Scientific American*, vol. 318, no. 3, pp. 74–79, Mar. 2018.

[7] D. Singh and M. Kumar, "Design and implementation of reversible half adder using optimized reversible gates," *Procedia Comput. Sci.*, vol. 132, pp. 509–516, 2018.

[8] J. C. Yue and K. Roy, "Energy-efficient adiabatic logic circuits using reversible logic gates," *IEEE Trans. VLSI*, vol. 27, no. 1, pp. 92–105, Jan. 2019.

[9] T. Suguna, "Survey on power optimization techniques for low power VLSI circuit in deep submicron technology," *SSRN*, Apr. 2024.

[10] L. Gopal et al., "Design of reversible multiplexer/de-multiplexer," in *Proc. IEEE ICCSCE*, Nov. 2014, pp. 416–420.

[11] R. Korah and A. Thomas, “Design of multiplexers using reversible logic technique,” *Int. J. Recent Innov. Trends Comput. Commun.*, vol. 10, no. 2, pp. 45–50, 2023.

[12] M. Frank, “The future of computing depends on making it reversible,” *IEEE Spectrum*, vol. 54, no. 9, pp. 32–37, Sep. 2017.

[13] D. Sarkar et al., “Data-dependent clock gating approach for low power sequential system,” *arXiv preprint arXiv:1806.02271*, 2018.

[14] S. Singh and A. Chauhan, “Design and synthesis of low-power reversible logic circuits,” *J. Low Power Electron. Appl.*, vol. 11, no. 3, pp. 28, 2021.

[15] S. Patel et al., “Design and simulation of reversible half adder using R-I gate,” *Int. J. VLSI Design & Commun. Syst.*, vol. 13, no. 2, pp. 19–25, 2022.

[16] S. M. Rahman and M. Anis, “Power gating design and implementation,” *IEEE Design & Test*, vol. 31, no. 4, pp. 28–36, 2019.

[17] A. K. Singh et al., “Design of ultra-low power reversible full adder using hybrid logic,” *Microelectron. J.*, vol. 90, pp. 11–21, 2019.

[18] K. Khan and R. Hasan, “Survey on leakage power reduction techniques in VLSI,” *J. Low Power Electron. Appl.*, vol. 10, no. 4, pp. 32–41, 2020.

[19] D. R. Acharya, “Comparative analysis of static power reduction techniques in 45nm CMOS technology,” *Int. J. Eng. Res. Appl.*, vol. 9, no. 3, pp. 17–22, 2020.

[20] B. Keller et al., “Adaptive voltage scaling,” in *Proc. ESSCIRC*, 2016.

[21] J. H. Yahya et al., “DarkGates: A hybrid power-gating architecture to mitigate the performance impact of dark-silicon,” *arXiv preprint arXiv:2112.11587*, 2021.

[22] H. E. El-hmaily et al., “High performance GNR power gating for low-voltage CMOS circuits,” *arXiv preprint arXiv:1901.00092*, 2019.

[23] Y. Mei, “Research on low-power design methods for integrated circuits,” *Adv. Comput. Eng.*, vol. 5, no. 1, pp. 12–18, 2025.

[24] R. Tiwari and P. Sinha, "Survey on QCA reversible logic circuit design," *Comput. Electr. Eng.*, vol. 91, pp. 107079, 2021.

[25] A. Jain and S. Patra, "Design of optimized reversible logic gates for arithmetic applications," *VLSI Design*, vol. 2020, Article ID 8323954.

[26] S. L. Sahoo et al., "Performance analysis of reversible logic circuits using QCA," *Microprocess. Microsyst.*, vol. 71, pp. 102870, 2020.

[27] G. R. Ramaswamy et al., "A novel fault tolerant reversible ALU using parity preserving gates," *Microelectronics Reliability*, vol. 120, pp. 114115, 2021.

[28] S. Bhosale et al., "Low-power VLSI circuit design using reversible logic and adiabatic techniques," *IET Circuits Devices Syst.*, vol. 16, no. 1, pp. 13–24, 2022.

[29] H. Y. Guo et al., "Energy-aware synthesis of reversible circuits," *IEEE Trans. CAD*, vol. 39, no. 5, pp. 1217–1227, May 2020.

[30] M. A. Perkowski, "Reversible computing: Recent advances and future perspectives," *ACM Computing Surveys*, vol. 54, no. 1, pp. 1–38, 2021.

[31] V. Kamble and S. Sarangi, "Design space exploration of reversible circuits for ALU design," *IEEE Access*, vol. 9, pp. 91234–91244, 2021.

[32] Y. Chen and J. Cong, "Thermal-aware power gating in sub-20nm 3D ICs," *IEEE Trans. VLSI*, vol. 28, no. 6, pp. 1345–1357, Jun. 2020.

[33] M. Chabi et al., "Cost-efficient QCA reversible combinational circuits based on a new reversible gate," in *Proc. CSI CADS*, 2015, pp. 1–6.

[34] Wikipedia contributors, "Reversible computing," *Wikipedia, The Free Encyclopedia*, 2025. [Online]. Available: https://en.wikipedia.org/wiki/Reversible_computing

[35] Wikipedia contributors, "Adiabatic circuit," *Wikipedia, The Free Encyclopedia*, 2025. [Online]. Available: https://en.wikipedia.org/wiki/Adiabatic_circuit

[36] N. K. Vishwakarma and R. Pandey, "Novel reversible full adder using less garbage outputs," *AEU - Int. J. Electron. Commun.*, vol. 94, pp. 192–201, 2018.

[37] Y. Hu et al., "Reversible logic in near-threshold computing," *IEEE Trans. Circuits Syst. I*, vol. 67, no. 10, pp. 3412–3424, 2020.

[38] S. Arora and S. Yadav, "Reversible logic based low-power ALU," *Int. J. Comput. Appl.*, vol. 183, no. 32, pp. 22–26, 2022.

[39] P. Kumar and D. Singh, "Low power VLSI design: Issues and techniques," *IEEE Trans. VLSI*, vol. 29, no. 3, pp. 521–532, 2021.

[40] A. Ghosh and B. Ghosh, "Leakage current reduction in CMOS: Techniques and analysis," *Int. J. VLSI Design*, vol. 10, no. 1, pp. 15–24, 2019.

[41] T. Misra and A. Patnaik, "Quantum cost analysis of hybrid reversible circuits," *Quantum Information Processing*, vol. 18, no. 4, pp. 105, 2019.

[42] M. Kumar and S. Saini, "Pass transistor logic based power efficient reversible logic," *Microelectron. J.*, vol. 88, pp. 101–109, 2019.

[43] V. Chaurasiya and S. Chauhan, "Design of 2x1 reversible multiplexer using R-I gate," *Int. J. Adv. Res. Comput. Sci.*, vol. 9, no. 6, pp. 31–34, 2018.

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Main Bawana Road, Delhi-42

PLAGIARISM VERIFICATION

Title of the Thesis____

____

Total Pages ___________________ Name of the Scholar__________________________

Supervisor (s)

(1)______________________________

(2)______________________________

(3)______________________________

Department____

This is to report that the above thesis was scanned for similarity detection. Process and outcome is given below:

Software used: __________________________ Similarity Index: _______, Total Word Count: _________

Date: ____________

Candidate's Signature **Signature of Supervisor(s)**

Asmar_Thesis_updated.pdf

Delhi Technological University

Document Details

Submission ID

trn:oid:::27535:98383068

Submission Date

May 29, 2025, 7:18 PM GMT+5:30

Download Date

May 29, 2025, 7:20 PM GMT+5:30

File Name

Asmar_Thesis_updated.pdf

File Size

332.5 KB

31 Pages

5,071 Words

30,267 Characters

8% Overall Similarity

The combined total of all matches, including overlapping sources, for each database.

Filtered from the Report

- Bibliography
- Cited Text
- Small Matches (less than 8 words)
- Submitted works
- Crossref posted content database

Match Groups

37 Not Cited or Quoted 8%
Matches with neither in-text citation nor quotation marks

0 Missing Quotations 0%
Matches that are still very similar to source material

0 Missing Citation 0%
Matches that have quotation marks, but no in-text citation

0 Cited and Quoted 0%
Matches with in-text citation present, but no quotation marks

Top Sources

6% Internet sources

4% Publications

0% Submitted works (Student Papers)

Integrity Flags

0 Integrity Flags for Review

No suspicious text manipulations found.

Our system's algorithms look deeply at a document for any inconsistencies that would set it apart from a normal submission. If we notice something strange, we flag it for you to review.

A Flag is not necessarily an indicator of a problem. However, we'd recommend you focus your attention there for further review.

Match Groups

- **37** Not Cited or Quoted 8%
  Matches with neither in-text citation nor quotation marks
- **0** Missing Quotations 0%
  Matches that are still very similar to source material
- **0** Missing Citation 0%
  Matches that have quotation marks, but no in-text citation
- **0** Cited and Quoted 0%
  Matches with in-text citation present, but no quotation marks

Top Sources

6% Internet sources
4% Publications
0% Submitted works (Student Papers)

Top Sources

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

1	Internet	
	kipdf.com	<1%
2	Publication	
	Asma Taheri Monfared, Majid Haghparast. "Quantum Ternary Multiplication Gate...	<1%
3	Publication	
	Hafiz Md. Hasan Babu. "Reversible and DNA Computing", Wiley, 2020	<1%
4	Publication	
	Lenin Gopal, Nikhil Raj, Nyap Tet Clement Tham, Alpha Agape Gopalai, Ashutosh ...	<1%
5	Internet	
	dokumen.pub	<1%
6	Internet	
	jtec.utem.edu.my	<1%
7	Internet	
	ir.lib.uwo.ca	<1%
8	Internet	
	www.researchtrend.net	<1%
9	Internet	
	www.sics.se	<1%
10	Publication	
	S. Santhameena, Manikandan J.. "Group acknowledgement mechanism for beaco...	<1%

11 Internet

lib.buet.ac.bd:8080 <1%

12 Internet

www.scss.tcd.ie <1%

13 Publication

Latif, Shamria Sabatina. "Fault Tolerance in Reversible Logic.", University of Lethb... <1%

14 Internet

escholarship.org <1%

15 Internet

pdfcoffee.com <1%

16 Internet

fresnostate.edu <1%

17 Internet

orca.cardiff.ac.uk <1%

18 Internet

www.mdpi.com <1%

19 Publication

Hossain, Mousam. "Formal Verification Methodology for Asynchronous Sleep Con... <1%

20 Publication

Hussain, Mohammed Mujtaba. "Multi-component and multi-dimensional mathe... <1%

21 Publication

Lecture Notes in Computer Science, 2010. <1%

22 Internet

dspace.mit.edu <1%

23 Internet

fr.slideshare.net <1%

24 Internet

odr.chalmers.se <1%

25 Internet

www.eit.lth.se <1%

26 Publication

Bojan Jovanović. "Methods for power minimisation in modern VLSI circuits", Inter... <1%

27 Publication

Fadi T. Naser, Sarah N. Hadi, Ivan A. Hashim. "Power Optimization of KNN Algorit... <1%

28 Publication

Subhrajit Sinha Roy, Abhishek Basu, Avik Chattopadhyay. "chapter 4 Hardware I... <1%

29 Publication

Thangaprakash Sengodan, Sanjay Misra, M Murugappan. "Advances in Electrical ... <1%

30 Internet

harvest.usask.ca <1%

31 Internet

impa.usc.edu <1%