M.Tech.
Thesis

Achieving Glitch Free Cross Domain Crossing Signal

DEEPTI

May,
2025

ACHIEVING GLITCH FREE CROSS DOMAIN CROSSING SIGNAL

A Thesis Submitted
In Partial Fulfillment of the Requirements
for the Degree of

MASTER OF TECHNOLOGY

In

VLSI AND EMBEDDED SYSTEMS

by

DEEPTI
(2K23/VLS/09)

Under the Supervision of
Sumit Khandelwal
Asst. Professor, ECE Dept.

Department of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY
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Shahbad Daulatpur, Main Bawana Road, Delhi-110042. India

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The successful completion of any task is incomplete and meaningless without giving any due credit to the people who made it possible without which the project would not have been successful and would have existed in theory.

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CANDIDATE'S DECLARATION

I Deepti, Roll No. 2K23/VLS/09 hereby certify that the work which is being presented in the thesis entitled **'Achieving Glitch Free Cross Domain Crossing Signal'** in partial fulfillment of the requirements for the award of the Degree of Master of Technology (VLSI and Embedded Systems), submitted in the Department of Electronics and Communication Engineering , Delhi Technological University is an authentic record of my own work carried out during the period from January 2025 to May 2025 under the supervision of **Sumit Khandelwal.**

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

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CERTIFICATE BY THE SUPERVISOR

Certified that 2K23/VLS/09 has carried out their search work presented in this thesis entitled "**Achieving Glitch Free Cross Domain Crossing Signal** " for the award of **Master of Technology** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

Glitches—unintended signal transitions—pose significant challenges to the performance and reliability of digital circuits, particularly in synchronous systems and complex System-on-Chip (SoC) designs with multiple clock domains. This paper focuses on employing structural verification techniques to achieve glitch-free circuit operation.

We investigate and mitigate glitch occurrences early in the design process through the application of advanced verification methodologies, including formal verification and simulation-based approaches. The study begins with a comprehensive analysis of the origins and types of glitches in digital circuits. Subsequently, we introduce structural verification frameworks specifically designed to identify and rectify potential glitch-inducing configurations.

Furthermore, in the context of increasingly intricate SoC designs incorporating multiple clock domains, we present a solution for detecting clock domain crossing (CDC) glitches by integrating formal verification and static timing analysis techniques. This paper also explores the utilization of formal verification tools for sequential equivalence checking between a flawed design and its corrected version when CDC glitches are discovered at later stages of the design cycle. We model, simulate, and verify designs against predefined glitch-free specifications using industry-standard tools to demonstrate the effectiveness of the proposed techniques.

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CL = Capacitive load

Pdynamic = Dynamic Power

CLK = Clock

I = Current

V = Voltage

T = Time

ABBREVIATIONS

CDC: Clock Domain Crossings

IC: Integrated Circuit

CMOS: Complementary Metal Oxide Semiconductor

SOC: System On Chip

FF: Flip Flops

LTSpice: Linear Technologies Simulation Program for Integrated Circuit Emphasis

CHAPTER 1
INTRODUCTION

The rapid advancement of microelectronics has led to the development of increasingly complex and powerful integrated circuits (ICs), driven by the growing demand for enhanced functionality and processing capabilities within compact form factors. However, this pursuit of performance introduces a significant challenge: power consumption. Excessive power dissipation not only limits battery life in portable devices and increases operational costs in large systems but also poses thermal management issues that can impact reliability and performance. Consequently, **low-power Very-Large-Scale Integration (VLSI)** design has emerged as a critical discipline, focusing on a collection of methodologies and strategies aimed at minimizing the overall dynamic and static power consumption of integrated circuits. Techniques such as dynamic voltage and frequency scaling (DVFS), clock gating, power gating, and multi-threshold CMOS (MTCMOS) are commonly employed to achieve power efficiency in ICs. DVFS adjusts the supply voltage and clock frequency based on workload demands, reducing power consumption during low-performance periods. Clock gating selectively disables clock signals to inactive modules, minimizing unnecessary switching activity. Power gating completely shuts off power to unused blocks, effectively reducing static power dissipation. MTCMOS utilizes transistors with varying threshold voltages to balance performance and leakage power. By integrating these techniques, designers can optimize power consumption without compromising the functionality and performance of integrated circuits. Low-power design aims to minimize the total energy consumption of integrated circuits (ICs) by optimizing the power usage of individual components. In CMOS digital circuits, power dissipation is primarily categorized into dynamic and static components. Dynamic power arises from the charging and discharging of capacitive loads during transistor switching activities. It includes switching power, which is the energy required to change the state of a node, and short-circuit power, which occurs during brief periods when both pull-up and pull-down networks of a gate are simultaneously conducting. Static power, conversely, is the power consumed when the circuit is in a stable state and ideally should be zero. However, static power is primarily due to leakage currents flowing through transistors even when they are supposedly "off." These leakage currents can be categorized into subthreshold leakage, gate-induced drain leakage, and

junction leakage, each contributing to the overall static power dissipation. As technology scales down, static power has become a significant concern, often approaching or exceeding dynamic power consumption in modern ICs.

The magnitude of both dynamic and static power consumption in integrated circuits is influenced by several key parameters:

1. **Frequency, Activity, and Transition Time:**

Dynamic power is directly proportional to the switching frequency and the activity factor (the probability of a node switching). Faster transition times can also contribute to increased short-circuit power.

2. **Voltage:**

Power consumption has a strong dependence on the supply voltage. Dynamic power is proportional to the square of the voltage ($P_{dynamic} \propto V_{DD}^2$), while static power due to subthreshold leakage also increases exponentially with decreasing threshold voltage, often necessitated by lower supply voltages for performance.

3. **Leakage Current:**

Static power is directly proportional to the leakage current, which is influenced by factors such as transistor dimensions, temperature, and supply voltage.

4. **Peak Current:**

While not directly in the average power equation, peak current demands impact power delivery network design and can influence voltage droop and overall system stability.

5. **Capacitive Load**:

Dynamic power is directly proportional to the capacitive load being switched ($P_{dynamic} \propto C_L$). Reducing the capacitance of nodes can significantly lower power consumption.

The intricate interplay of these parameters necessitates careful consideration and trade- offs during the design process. For instance, lowering the supply voltage is a highly effective way to reduce both dynamic and static power. However, it can also lead to increased circuit delays and reduced noise margins, potentially impacting performance. Low power design techniques aim to navigate these trade-offs, striving to achieve the highest possible performance with the minimum possible power expenditure.

Several established low power design techniques are employed at various stages of the design flow to address these challenges:

Clock Gating:

Clock gating is a widely adopted technique in digital circuit design, particularly within Very Large Scale Integration (VLSI) systems, aimed at reducing dynamic power consumption. It involves selectively disabling the clock signal to portions of a circuit when they are not in use, thereby reducing dynamic power consumption. The fundamental principle behind clock gating is that digital circuits consume power primarily during state transitions, which are driven by clock signals. By preventing the clock from toggling in inactive sections of a circuit, designers can significantly lower the overall power requirements. This selective clocking effectively reduces the toggle rate, which is a significant contributor to dynamic power dissipation. The implementation of clock gating can be achieved through various methods:

Integrated Clock Gating (ICG) Cells:

These are standard cells provided by semiconductor libraries that incorporate gating logic to control the clock signal.

Manual Insertion:

Designers can manually insert gating logic into the design, specifying the conditions under which the clock should be disabled.

Automatic Insertion:

Modern synthesis tools can automatically insert clock gating based on enable conditions specified in the Register Transfer Level (RTL) code.

Multi-Voltage Design:

The multi-voltage design technique capitalizes on the fact that various functional blocks within a complex chip have differing performance requirements. Instead of operating the entire chip at the highest voltage dictated by the most critical path, this approach partitions the chip into multiple voltage domains. As the power equation reveals, reducing the voltage has a profound impact on both dynamic and static power components. While designing the entire chip at a higher voltage offers simplicity, the power penalty can be substantial. Implementing multi-voltage design requires careful consideration of level shifters at the boundaries between different voltage domains to ensure correct signal transfer. These level shifters are essential for

proper communication between blocks operating at different voltage levels, ensuring data integrity and system reliability.

Power Gating:

Power gating is a highly effective technique in VLSI design aimed at minimizing power consumption by completely disconnecting the power supply to inactive circuit blocks. This approach eliminates both dynamic and static power dissipation during periods of inactivity, making it particularly beneficial for modules that remain idle for extended durations. The implementation of power gating involves introducing power switches—typically high-threshold PMOS or NMOS transistors—into the power distribution network. These switches are controlled by a power management unit that determines when to activate or deactivate specific blocks based on their activity status. To ensure proper functionality, additional components such as isolation cells are employed to prevent unwanted signal propagation between powered-down and active blocks, thereby maintaining signal integrity. Furthermore, retention registers may be utilized to preserve the state of the powered-down blocks, allowing for a seamless transition back to active mode without data loss. However, the adoption of power gating necessitates careful consideration of design aspects, including the sizing of power switches to handle peak currents, managing the slew rate of control signals to prevent rush currents, and addressing the challenges of state retention and wake-up latency. Despite these complexities, power gating remains a cornerstone in low-power VLSI design, especially in applications where energy efficiency is paramount.

While these techniques primarily focus on reducing overall power consumption, another critical aspect of robust digital design, particularly in complex SoCs, is ensuring the reliable transfer of signals between different clock domains. This leads us to the crucial topic of Clock Domain Crossing (CDC) and the challenges it presents**, Achieving Glitch-Free Clock Domain Crossing Signal.**

Specifically, this study examines scenarios where signals launched in a faster clock domain must adhere to strict timing constraints to prevent the generation of glitches in the slower receiving clock domain. We delve into the classification of synchronous CDC based on the phase and frequency relationships of the source and destination clocks, highlighting the significant metastability risks associated with asynchronous clock domains. The design

principles we explore emphasize meeting timing constraints by avoiding fractional cycle-time transfers across clock domain boundaries.

In essence, this introductory chapter sets the stage for a comprehensive exploration of low power VLSI design principles and the critical challenge of achieving glitch-free clock domain crossing. By understanding the sources of power consumption and the complexities introduced by multiple clock domains, we can appreciate the significance of employing sophisticated design and verification techniques to build reliable and efficient digital systems. The subsequent chapters will delve deeper into specific methodologies and their application in addressing these crucial aspects of modern VLSI design.

1.1 PROBLEM STATEMENT

This chapter delves into the critical issue of achieving glitch-free operation within combinational logic circuits, a fundamental aspect of low-power VLSI design. Glitches—unwanted transient transitions in signal states before settling to their intended value—pose significant challenges to the performance, reliability, and power efficiency of digital systems, even within a single clock domain. In combinational circuits, where the output ideally reflects the current input instantaneously, glitches arise due to inherent propagation delays through various paths in the logic network. Variations in these path delays can cause input changes to arrive at the output at different times, leading to spurious transitions. These glitches not only result in incorrect logic levels but also contribute to increased power consumption, as each unwanted transition consumes energy. Addressing this issue requires meticulous design strategies to balance path delays and minimize the occurrence of glitches, thereby enhancing the efficiency and reliability of digital circuits. These glitches, despite being temporary, can have detrimental consequences:

Spurious Switching:

Glitches cause unnecessary charging and discharging of capacitances in subsequent circuits, leading to increased dynamic power consumption. In high-activity designs, the cumulative effect of numerous glitches can significantly impact the overall power budget.

Incorrect Latching:

In synchronous systems, the outputs of combinational circuits are often sampled by sequential elements (flip-flops) triggered by a clock edge. If a glitch occurs near the clock edge and violates the setup and hold time requirements of the flip- flop, it can lead to the incorrect latching of an intermediate, unintended value, resulting in functional errors.

Timing Violations:

Glitches can propagate through the circuit and potentially create false transitions that trigger downstream logic prematurely or cause timing violations in critical paths.

Increased EMI (Electromagnetic Interference):

The rapid voltage transitions associated with glitches can contribute to increased electromagnetic emissions, potentially affecting the functionality of nearby circuits or systems.

Reduced Noise Margin:

Glitches can temporarily reduce the noise margin of subsequent gates, making them more susceptible to other noise sources and potentially

leading to unreliable operation.

Therefore, ensuring glitch-free operation in combinational circuits is crucial for achieving high performance, low power consumption, and reliable digital systems. Traditional design methodologies often rely on careful timing analysis and simulation to identify and mitigate potential glitch hazards. However, these methods can be time- consuming and may not guarantee the complete absence of glitches across all operating conditions and process variations.

This work specifically addresses the problem of systematically achieving glitch-free combinational circuit operation through the application of structural verification techniques. Unlike simulation-based methods that rely on exercising the design with a limited set of input stimuli, structural verification analyzes the circuit's topology and logical structure to identify potential glitch-generating configurations.

The core problem we aim to solve is:

How can we leverage structural analysis and formal verification methods to effectively identify, analyze, and ultimately eliminate or minimize the occurrence of glitches in combinational logic circuits during the design phase, thereby ensuring robust and efficient operation?

How to address this:

To address this problem, we will investigate and develop structural verification frameworks capable of :

Static Glitch Analysis:

Developing techniques to statically analyze the circuit structure to identify potential glitch hazards based on path length disparities and logic gate characteristics. This involves modeling the propagation delays of individual gates and analyzing the conditions under which input changes can lead to spurious output transitions.

Formal Verification of Glitch-Free Properties:

Exploring the application of formal verification tools and techniques to prove the absence of glitches under all possible input transitions. This might involve defining formal specifications for glitch-free behavior and using model checking or theorem proving to verify that the circuit design adheres to these specifications.

Identifying and Characterizing Glitch-Prone Structures:

Pinpointing common logic configurations and circuit topologies that are inherently susceptible to generating glitches. This knowledge can then be used to guide design choices and avoid such structures were critical.

Developing Structural Transformation Techniques:

Investigating potential structural modifications or design techniques that can be applied to eliminate or significantly reduce the likelihood and impact of glitches without compromising the intended functionality of the circuit. This could involve techniques like path balancing, hazard filtering, or the strategic insertion of delay elements.

Integration with Standard Design Flows: Exploring how these structural verification techniques can be seamlessly integrated into existing VLSI design flows and utilized with industry-standard tools for efficient glitch analysis and mitigation.

The focus of this investigation is on addressing glitches arising from the inherent structure and propagation delays within combinational logic, independent of clock domain crossing issues. By developing and applying sophisticated structural verification methodologies, we aim to provide a more robust and systematic approach to achieving glitch-free combinational circuit operation, leading to improved performance, reduced power consumption, and enhanced reliability in digital systems. The subsequent sections will delve into the specific techniques and methodologies employed to tackle this critical problem.

1.2 STRUCTURE OF THESIS

The thesis comprises eight distinct chapters. Chapter 1 has the Introduction, presenting an overview of CDC and some of the problems due to CDC. In Chapter 2, literature survey has been done. Chapter 3 gives details of the background information and the blocks that have been employed in the design. The discussion on the proposed mutator designs is outlined in Chapter 4. Chapter 5 discusses the simulation results. A comparison of proposed mutator with the existing literature is shown in Chapter 6. To verify the efficiency of the design, the proposed mutator circuits are applied in an adaptive learning application in Chapter 7. Finally, Chapter 8 concludes the entire study that has been presented.

CHAPTER 2

LITERATURE SURVEY

This chapter consolidates the primary insights and significant contributions from the reviewed literature, presenting a detailed summary of the current advancements in tackling clock domain crossing (CDC) challenges and ensuring glitch-free performance in sophisticated digital systems.

The complexities involved in addressing CDC problems are emphasized by [1], which brings attention to the rising intricacy of System-on-Chips (SoCs) and the shortcomings of traditional simulation and static timing analysis techniques in securing dependable data exchanges across asynchronous clock domains. The study advocates for the use of customized and multifaceted verification approaches tailored to the unique demands of CDC verification. It introduces a methodical process designed to effectively confront this critical issue.

The difficulty in detecting glitches through formal verification techniques is examined in [2], which critiques the inefficiency of current commercial tools in identifying these short-lived anomalies in CDC scenarios. The authors introduce a new methodology centered around symbolic ternary simulation and offer a rigorous formal definition for a "glitch-free" circuit. Their approach leverages the ACL2 theorem prover to expose both deliberately inserted and potentially real-world glitches, demonstrating the value of formal verification for comprehensive glitch detection.

The foundational concept of metastability and the utility of synchronizers are explored in [3] and [4]. Metastability, resulting from signal transitions captured near clock edges, is highlighted as a major reliability concern capable of causing unpredictable behavior, illustrated by an actual spacecraft failure case [3]. The exponential relationship between metastability resolution time and circuit reliability is explained, emphasizing the importance of synchronizers in allowing adequate time for metastable states to settle [3].

A broader exploration of CDC verification obstacles is presented in [4], which outlines the constraints of static CDC verification tools, especially in intricate designs with analog IPs. The paper underlines the importance of comprehensive design evaluations and reveals

vulnerabilities in current ASIC signoff procedures that could lead to post-silicon defects. A well-rounded methodology is proposed, incorporating modeling, timing verification, and dynamic validation while advocating for cross-functional collaboration among design teams.

To reinforce CDC verification, [5] recommends the integration of formal verification methods focused on assertion-based validation. This includes formulating precise assertions to encapsulate correct signal handoff and metastability scenarios, applying temporal logic for cross-domain timing analysis, and utilizing model and equivalence checking techniques. The paper also stresses the need to validate synchronization structures and employ diverse testing strategies, such as randomized tests, to expand verification coverage.

The approach outlined in [6] targets the generation of glitch-free CDC signals by combining formal verification, static timing analysis, and sequential equivalence checking. Acknowledging the growing complexity of verifying multi-clock SoCs and the limitations of RTL modeling in addressing analog-related CDC problems such as metastability, the study advocates for formal verification through sequential equivalence checking to ensure glitch elimination between erroneous and corrected designs, even in the presence of combinational logic across domains with varying clock frequencies.

In relation to energy-efficient design, [7] investigates the implications of metastability in CDC for near-threshold-voltage (NTV) multi-voltage/frequency domain Network-on-Chips (NoCs). Traditional multi-stage synchronizers are seen to introduce latency challenges. To address this, the authors propose a metastability prediction and mitigation (MPAM) mechanism using a triple-phase clock monitoring system and a metastability-resilient clocking scheme aimed at achieving a balance between power efficiency and system dependability.

From a fabrication standpoint, [8] discusses the identification, diagnosis, and resolution of CDC faults in post-silicon multi-clock SoC environments. Despite sound design methodologies, variations in manufacturing processes can still cause data transfer errors. This work introduces a CDC-fault dictionary to detect and locate CDC-related issues, along with post-silicon clock path adjustment techniques to restore proper function.

Although not directly centered on CDC glitch mitigation, [9] introduces an enhanced power gating strategy incorporating data retention and clock gating for low-power VLSI designs. This technique prioritizes energy conservation during idle states while maintaining performance

integrity, utilizing retention flip-flops and additional clock gating. The study underscores the relevance of glitch prevention in low-power circuits, where even minor disturbances can adversely affect efficiency and functionality.

Together, these studies illustrate the complex nature of ensuring reliable CDC in modern digital architectures. They reveal the insufficiencies of conventional verification methods and champion the integration of advanced strategies such as formal verification, timing analysis, and innovative synchronization and fault mitigation techniques. Additionally, they highlight the growing importance of low-power design considerations and post-fabrication validation. This collection of research forms a solid theoretical base for continued exploration into achieving robust, glitch-free operation in increasingly intricate integrated circuits.

CHAPTER 3
BACKGROUND AND BLOCKS USED

ACTIVE BLOCK FOR THE PROPOSED CDC CIRCUIT:

Ensuring robust data transfer between synchronous clock domains operating at both integer and non-integer frequency ratios presents a significant challenge in modern System-on-Chip (SoC) architectures. One primary design objective is to eliminate timing dependencies that involve fractional cycle times between flip-flops across different clock domains. Aiming for a minimum timing margin equivalent to at least one full cycle of the faster clock is a common design goal. This section explores the theoretical foundations of a Clock Domain Crossing (CDC) circuit, particularly focusing on scenarios involving non-integer clock ratios and the risks of glitch occurrences.

Consider a case involving a 3:2 ratio between a high-speed clock (Clk1) and a slower clock (Clk2), as outlined conceptually in Figure 1 (not shown here but described contextually). In this configuration, the rising edge differences between Clk1 and Clk2 can result in edge separations of 1.5T, 1T, or 0.5T, where ‘T’ denotes the period of Clk1, the faster clock. To maintain reliable data capture in the slower domain, the design intent is to ensure that any data launched from Clk1 is stable for at least one Clk1 cycle (1T) before being sampled by Clk2.

Figure 2a shows a simplified CDC design block. In this example, flip-flops F1 and F2 are part of the Clk1 domain, while flip-flop F3 operates under Clk2. Signals T1 and T2, triggered by Clk1, traverse through combinational logic—specifically, an AND gate—before being captured by F3 on the Clk2 domain.

A significant issue arises when analyzing transitions from the faster domain that align with Clk1 edges creating fractional timing relationships with Clk2. For example, if F1 and F2 initiate transitions at a 0.5T offset from a Clk1 edge (denoted as 'X' in Figure 2b), this violates the intended requirement of maintaining at least a full Clk1 cycle (1T) between data launch and capture.

Moreover, such early launches at 0.5T present a high likelihood of generating glitches in the combinational logic. As depicted in Figure 2b, the AND gate combines T1 and T2, both

originating from the Clk1 domain. Suppose T1 changes from 1 to 0 and T2 from 0 to 1 at the Clk1 edge marked 'X'. Ideally, the output T3 of the AND gate should become 0. However, due to differing path delays, T1 and T2 may reach the AND gate input at slightly different times. This misalignment can briefly produce an incorrect transition or glitch on T3 before it stabilizes at 0.

The real concern arises if a rising edge of Clk2 coincides with this temporary glitch on T3. In the 3:2 clocking scenario, a Clk2 edge appears 0.5T after the Clk1 edge 'X'. If this Clk2 edge samples T3 while the glitch is present, flip-flop F3 could capture an incorrect logic level, resulting in a malfunction.

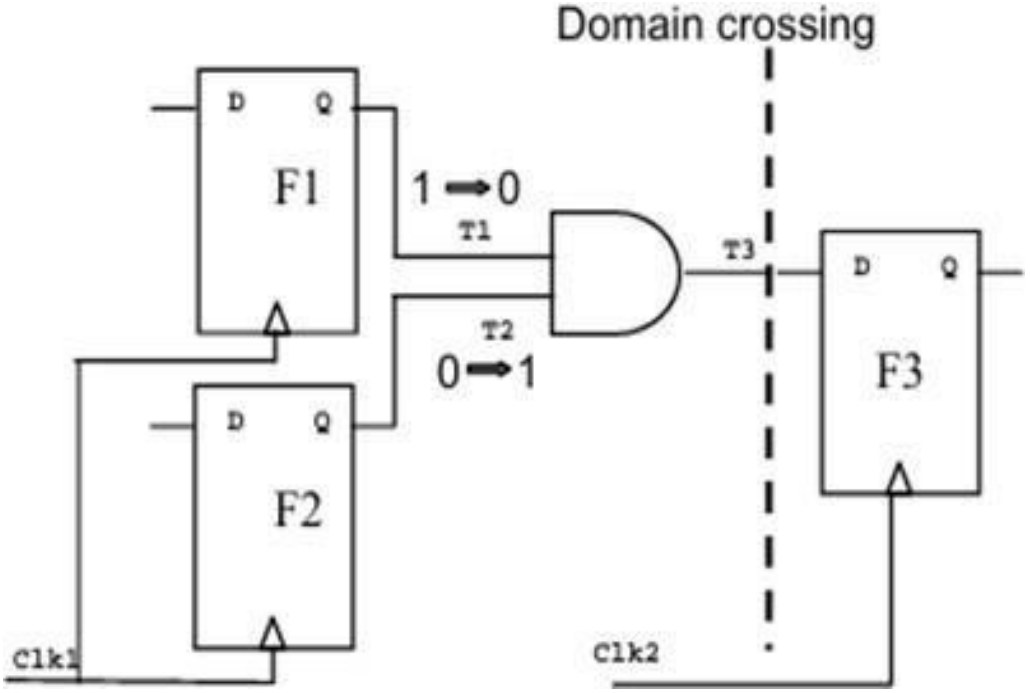

Figure 3.1

To prevent functional errors caused by glitches, the recommended solution is to avoid initiating data transfers from the faster Clk1 domain at clock edges that introduce unfavorable fractional cycle-time alignments—such as the 0.5T edge marked as 'X' in the 3:2 clocking scheme. Ensuring that data is launched only on Clk1 edges that maintain a timing buffer of at least one full cycle (1T) before the Clk2 sampling edge helps minimize the risk of the slower clock capturing a glitch caused by closely timed signal transitions in the faster domain.

The paper outlines an effective methodology to manage this issue, leveraging both formal verification and static timing analysis (STA). Formal verification offers a mathematical guarantee that, across all possible operating conditions and clock ratios, any transient glitch originating in one domain does not lead to setup or hold time violations in the receiving domain. Meanwhile, static timing analysis helps define and enforce constraints on inter-domain timing, ensuring that the design maintains the required minimum cycle-time separation and avoids data launches at hazardous Clk1 edges such as 'X'.

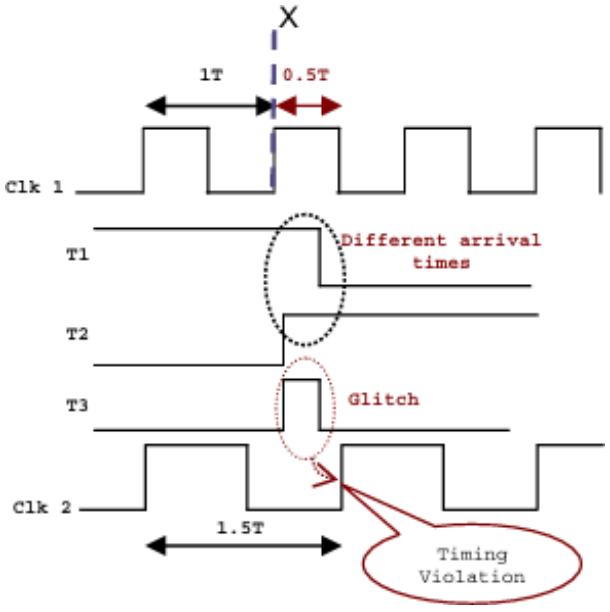

Figure 3.2

3.1 CDC BASED CIRCUITS:

CDC (Clock Domain Crossing) based circuits are digital systems specifically designed to manage the transfer of signals between different clock domains. A clock domain refers to a segment of a synchronous circuit that operates under a single, unified clock signal. In modern VLSI designs—especially in complex Systems-on-Chip (SoCs)—multiple clock domains are commonly used, each potentially running at different frequencies or phases to enhance the performance and reduce power consumption of individual functional units.

The primary challenge in designing CDC circuits stems from the lack of synchronization between clock domains. Signals transitioning from one domain to another do not align with the timing of the receiving domain's clock. As a result, this misalignment can introduce a critical problem known as metastability.

Metastability occurs when a flip-flop in the receiving clock domain captures an input signal that changes state too close to its active clock edge—violating setup and hold time constraints. When this happens, the output of the flip-flop can enter an unstable, undefined voltage state that lies between logical ‘0’ and ‘1’. This metastable condition can persist for an uncertain duration before the flip-flop eventually settles into a valid logic level. If the metastable state doesn’t resolve before the next clock edge attempts to sample the flip-flop's output, the system may latch incorrect data, potentially leading to downstream errors and functional failures.

Implications of Clock Domain Crossing:

Functional Errors:

Metastability can lead to the receiving logic interpreting an unstable signal as either a '0' or a '1' inconsistently, resulting in incorrect data processing and unpredictable behavior.

Timing Violations:

Signals crossing domains can also cause setup and hold time violations in the receiving flip-flops, further exacerbating the risk of metastability.

Data Incoherency:

For multi-bit signals (buses) transferred asynchronously, different bits might experience different delays and resolve from metastability at different times, leading to a period of invalid or incoherent data in the receiving domain.

Glitches: As highlighted in the provided text, even with seemingly stable logic levels, timing variations in the launching clock domain can create transient unwanted signal changes (glitches) in the combinatorial logic that follows the launching flip-flops. If these glitches occur close to the sampling edge of the receiving clock domain, they can be erroneously captured, leading to functional errors that might not be apparent in functional simulations with ideal timing

CHAPTER 4

SIMULATION RESULTS AND ANALYSIS

The objective of the proposed circuit is to enable dependable data transfer between two synchronous clock domains—Clk1 (the faster clock) and Clk2 (the slower clock)—that operate at a non-integer 3:2 frequency ratio. The main issue being tackled is the risk of the slower Clk2 domain inadvertently capturing glitches generated within the faster Clk1 domain, which occur due to rapid and closely timed signal transitions. Such glitches, if sampled, can lead to functional errors. To ensure reliable communication across these domains, the design employs synchronization techniques using flip-flops. A key focus is on avoiding data launches from Clk1 that create fractional timing intervals relative to Clk2, as these conditions increase the likelihood of glitches being sampled by the slower domain.

The foundational theory behind this method is rooted in analyzing the timing limitations and challenges involved in asynchronous data communication. In systems operating across multiple clock domains, clock edges are not synchronized and may exhibit differing phase relationships. Specifically, in a scenario with a 3:2 clock ratio, the rising edges of Clk2 align at time intervals of 1.5T, 1T, and 0.5T relative to the rising edges of Clk1, where T denotes the clock period of Clk1.

The purpose of the design is to eliminate fractional cycle-time dependencies between clock domains by ensuring a minimum setup time equivalent to one full cycle of the faster clock (1T). This means that data originating from the Clk1 domain must reach the receiving flip-flop in the Clk2 domain with adequate timing slack before the relevant active edge of Clk2.

Issues emerge when data is triggered by a Clk1 edge that is immediately followed by a Clk2 sampling edge—particularly at the 0.5T offset in the 3:2 clock ratio. When combinational logic exists between the source flip-flops (clocked by Clk1) and the destination flip-flop (clocked by Clk2), and several input signals to this logic change simultaneously due to the Clk1 transition, variations in logic path delays can cause brief, unintended transitions—also known as

glitches—at the output of the combinational circuitry.

Take, for instance, a typical CDC scenario involving an AND gate as the combinational logic element. If signals T1 and T2—originating from flip-flops F1 and F2 in the Clk1 domain—change state on a Clk1 edge (such as the critical 0.5T offset edge 'X'), and these changes reach the AND gate with slight timing differences, the resulting output T3 may momentarily reflect an incorrect value (a glitch) before stabilizing to the correct state. If this glitch is captured by a rising edge of Clk2, it may propagate incorrect data to the Clk2 domain's downstream logic, potentially leading to a malfunction.

To address this potential hazard, the proposed design introduces an implicit restriction on when data can be launched from the higher-frequency Clk1 domain. By maintaining the requirement of a minimum setup window equal to one full Clk1 cycle (1T), any data launch from Clk1 that would result in less than 1T before the subsequent Clk2 sampling edge is either strictly avoided or treated with heightened precaution. This approach specifically aims to eliminate risks associated with the 0.5T timing window in the 3:2 clock ratio.

The core synchronization mechanism to prevent the propagation of both metastable states (though not explicitly the focus of glitch prevention here, it's an inherent concern in CDC) and the erroneous capture of glitches relies on the strategic placement of synchronizer flip-flops at the clock domain boundary. While the provided text doesn't explicitly show the synchronizer implementation, the underlying principle for reliable CDC involves at least a two-stage flip-flop synchronizer in the receiving Clk2 domain for each signal crossing from Clk1.

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THEORETICAL OPERATION WITH SYNCHRONIZERS FOR GLITCH PREVENTION:

Data Launch in Clk1: Data originates in the Clk1 domain and is held stable by flip-flops (F1, F2 in the example) until a launching Clk1 edge

Restricted Launch Edges: The key to preventing glitch capture lies in ensuring that data is primarily launched on Clk1 edges that provide a sufficient time window (at least 1T) before the next active edge of the slower Clk2. This constraint avoids scenarios where the combinatorial logic in the Clk1 domain has insufficient time to settle after a transition before being sampled by Clk2.

Combinatorial Logic in Clk1 Domain: Signals from the launching flip-flops pass through combinatorial logic. It is within this logic that glitches can potentially be generated due to varying path delays when multiple inputs change around the same Clk1 edge.

Synchronization in Clk2 Domain: To reliably capture the output of the combinatorial logic in the Clk2 domain, a synchronizer stage is essential. A typical synchronizer consists of at least two series-connected flip-flops clocked by Clk2.

First Synchronizer Flip-Flop (in Clk2): This flip-flop samples the output of the combinatorial logic (which might contain a glitch if a problematic launch occurred) on the rising edge of Clk2. If the input is metastable or contains a glitch close to the Clk2 edge, this flip-flop itself might enter a metastable state. However, it has a full Clk2 cycle to resolve to a stable '0' or '1'.

Second Synchronizer Flip-Flop (in Clk2): This flip-flop samples the output of the first synchronizer flip-flop on the next rising edge of Clk2. By this time, the output of the first flip-flop is highly likely to have resolved to a stable logic level, thus preventing the propagation of metastability or the capture of a very short-duration glitch.

How Synchronizers Help Prevent Glitch Capture (in the context of restricted launch edges):

By restricting data launches in Clk1 to edges that provide sufficient settling time (>= 1T) before a Clk2 edge, we minimize the chances of a glitch being present at the input of the first synchronizer flip-flop in the Clk2 domain at the exact moment of the Clk2 sampling

edge. The combinatorial logic in the Clk1 domain has more time to settle to its final value after a Clk1 launch before the next Clk2 sampling opportunity.

Even if a short glitch does occur and propagates to the input of the first synchronizer flip-flop, the two-stage synchronizer acts as a temporal filter. The first flip-flop might temporarily capture the effect of the glitch, but the second flip-flop, sampling a full Clk2 cycle later, is likely to capture the correct, settled value. The probability of a metastable state persisting through both synchronizer stages and causing a functional error is significantly reduced.

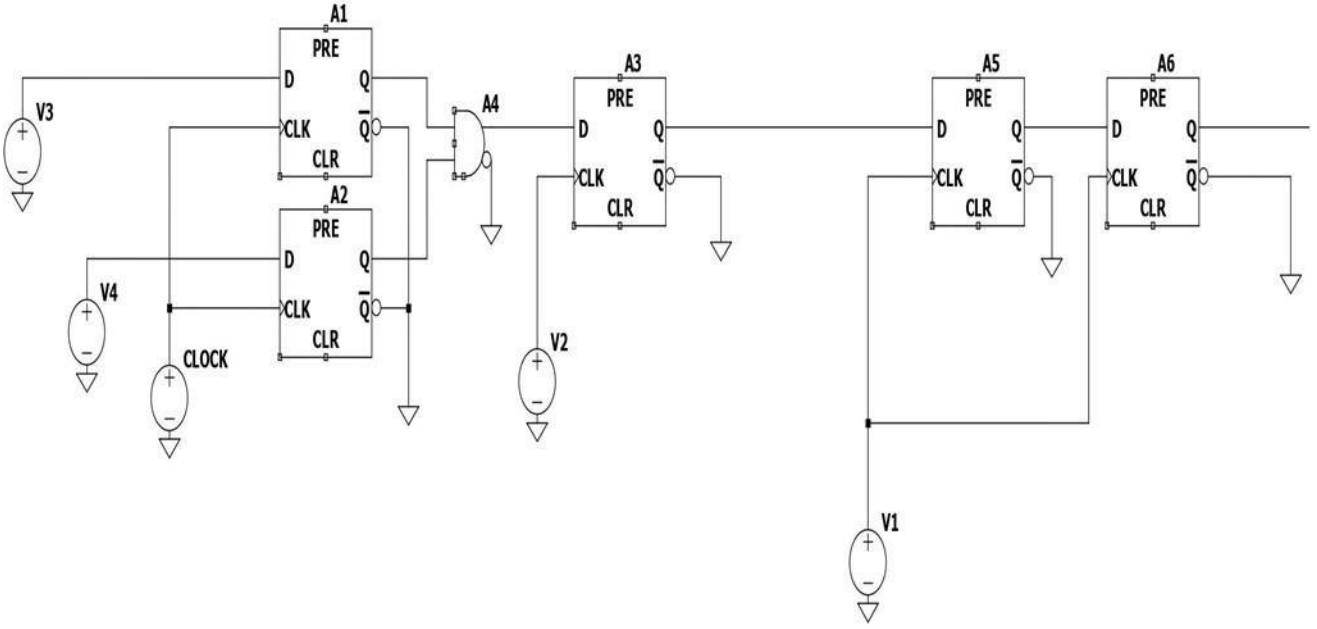

Figure 4.1

RESULTS

1. Arrival of Glitch

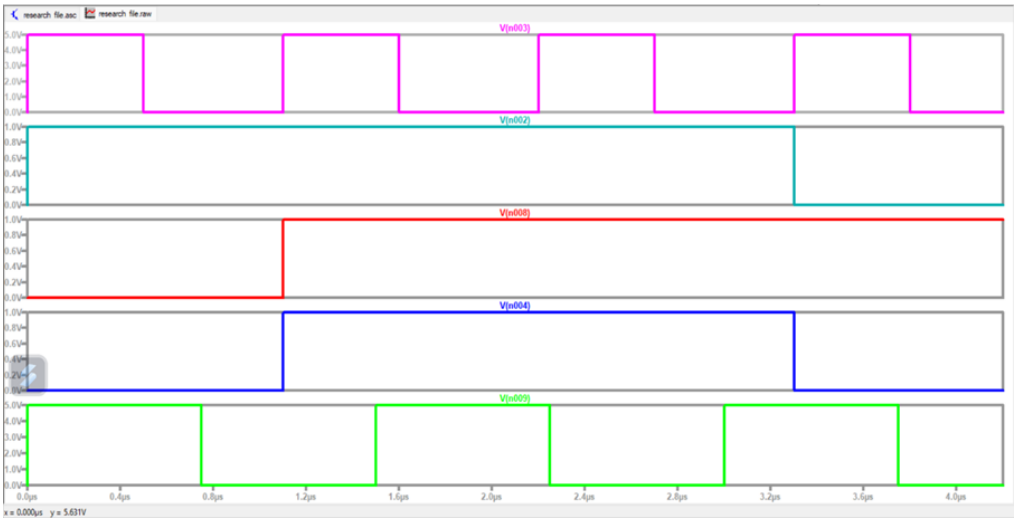

Figure 4.2.

2. Clean Circuit after applying Synchronizers

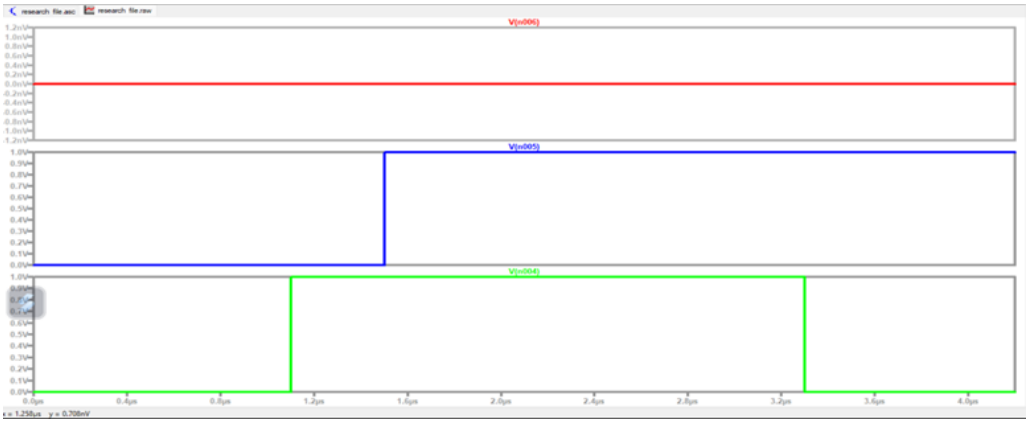

Figure 4.3

REPRESENTATION OF SIGNAL

Signal	**Time Period**		**Signal Represented by**
D1	2u		V(n001)
D2	1u		V(n010)
Clk1	1.1u		V(n003)
D1(out)			V(n002)
D2(out)			V(n007)
Clk2	1.5u		V(n008)
Glitch			V(n004)
Clk3	2u		V(n009)

Table 4.1

DURATION OF GLITCH

Signal	Time of Changing signal
D1(out)	1.1u
D2(out)	3.3u
Glitch	1.1u to 3.3u

Table 4.2

CHAPTER 5

COMPARISON OF PROPOSED CIRCUIT WITH EXISTING LITERATURE

The primary difference lies in the scope and the specific problem being addressed:

Existing one focuses on the detection of glitches, primarily within the context of synchronous designs that might be influenced by non-synchronous signals or operate in close proximity to CDC interfaces. The proposed solution is a specific simulation-based technique (symbolic ternary simulation) tailored for identifying these transient signal anomalies.

Proposed one focuses on the broader challenge of verifying the correctness and reliability of signal transfers across different clock domains (CDC verification) in complex SoCs. It highlights the limitations of traditional functional simulation in capturing analog-level issues like metastability, which are inherent to asynchronous transfers. The emphasis is on the need for improved methodologies in general for CDC verification.

However, there is a clear interconnection between these two descriptions:
Glitches are a potential consequence of poorly managed or inadequately verified CDC interfaces. The timing uncertainties and potential for race conditions at clock domain boundaries can indeed manifest as glitches in signals crossing these domains or in logic driven by such signals. The inadequacy of existing tools to detect glitches in CDC circuits directly relates to the broader challenges of CDC verification.
While proposes a specific simulation technique for glitch detection, the broader need for improved CDC verification methodologies might encompass other approaches like formal verification, advanced static timing analysis, and specialized CDC-aware simulation techniques, which could also contribute to preventing and detecting glitches in CDC paths.

IN ESSENCE:

Existing ones zooms in on the specific problem of glitch detection, particularly in scenarios involving synchronous logic interacting with asynchronous elements or in the vicinity of CDC interfaces, and proposes a simulation-based solution.

Proposed one provides a wider perspective on the overall challenges of ensuring reliable communication between different clock domains in complex SoCs, highlighting the limitations of traditional functional simulation in capturing critical analog-level issues like metastability and emphasizing the need for more sophisticated verification methodologies.

Both descriptions contribute to the understanding of the complexities involved in designing and verifying modern digital circuits. While one focuses on a specific type of transient signal anomaly and its detection, the other addresses the broader systemic challenges of ensuring reliable communication across asynchronous boundaries, a context where glitches can indeed arise and pose significant problems. Therefore, advancements in both glitch detection techniques and overall CDC verification methodologies are crucial for building robust and reliable SoC.

The comparison table concludes that:

- The proposed mutator circuits require only single active block as compared to others present in the literature which requires more than one type of active blocks.
- The memristor used in the proposed mutators do not require an active block, they are made entirely of transistors while that present in literature consists of active blocks.
- PHL curves for the proposed meminductor mutator are obtained upto a frequency of 2MHz while that reported in literature was only few Hz to KHz.
- PHL curves for the proposed memcapacitor mutator are obtained upto a frequency of 15MHz while that reported in literature was only few Hz to KHz.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

This study has explored the significant challenges that glitches and clock domain crossing (CDC) issues present in contemporary digital circuit design, highlighting their adverse effects on system performance, reliability, and overall functional correctness. A key insight from this investigation is the identification of metastability—typically triggered by violations of setup or hold time when asynchronous signals traverse between different clock domains—as the most critical concern in CDC scenarios. When such signals are captured by the destination clock near their transition period, they may enter a metastable state, where the signal level becomes undefined. If not properly managed, this unstable condition can propagate through the system, resulting in data corruption and potentially severe operational failures.

Although metastability is an unavoidable physical characteristic of asynchronous data transfers, this analysis emphasizes the importance of using synchronizers—particularly a two-stage flip-flop arrangement in the receiving clock domain—as a robust countermeasure. These synchronizers act as a temporal buffer, greatly minimizing the likelihood that a metastable signal will propagate beyond the synchronization boundary. By allowing additional time for the signal to settle to a valid logic level, the risk of metastability affecting downstream logic is significantly reduced. While this method does not eliminate metastability itself, it effectively contains its influence, ensuring it does not disrupt the broader system.

In summary, the central conclusion of this work is a reaffirmation of the effectiveness of widely adopted synchronization techniques—specifically, the dual flip-flop synchronizer—in managing metastability risks in CDC designs. Through the thoughtful integration of such mechanisms, engineers can substantially improve the dependability and correctness of systems operating across multiple clock domains, safeguarding them against the unpredictable effects of metastable events.

Future Work:

Building upon the findings and insights of this study, several promising avenues for future research and exploration have been identified:

Technology Scaling and Process Variations:

To develop a deeper understanding of glitch behavior and clock domain crossing (CDC) challenges, future research should include simulations across a range of semiconductor technology nodes. As fabrication processes continue to advance and device geometries shrink, transistor properties—such as switching speed and sensitivity to process variations—undergo significant changes. Examining how these evolving characteristics influence glitch occurrence and metastability handling in CDC circuits can offer critical insights for designing more resilient systems at smaller technology nodes.

Power Consumption Analysis of Mitigation Techniques:

Techniques used to minimize glitches and ensure reliable CDC synchronization can introduce additional power demands. Future studies should investigate the power overhead associated with various mitigation strategies. This includes assessing the balance between enhanced system reliability and energy efficiency across different synchronization mechanisms and glitch suppression methods. Gaining a clear understanding of these power-related trade- offs is essential for developing digital systems that are both energy-efficient and highly reliable, particularly in environments with strict power constraints.

Formalization and Automation of Verification:

Although this study emphasizes the role of synchronizers, future research should aim to develop a detailed research paper encompassing theoretical evaluations, simulation outcomes, and formal verification processes aimed at ensuring glitch-free and dependable CDC designs. Such a contribution would enhance the current body of knowledge and could lead to the development of more formalized and automated verification frameworks for assessing the effectiveness of various mitigation strategies.

Exploration of Advanced Synchronization Techniques:

In addition to the conventional dual flip- flop synchronizer, future research should investigate and assess more sophisticated synchronization methods, such as the Handshake CDC protocol. This approach, which employs control signals like "request" and "acknowledge," provides a stronger mechanism for accurate synchronization by explicitly managing data transfers between clock domains. Evaluating these techniques in terms of performance, area overhead, and power consumption—and comparing them against simpler synchronizers—would offer valuable insights. Additionally, examining other advanced schemes, including pulse synchronizers or bundled data protocols, could further enhance understanding of how-to achieve dependable CDC

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