M.Tech.
Thesis

ENHANCING THE DC-GAIN OF THE OPERATIONAL AMPLIFIER BY THE USE OF POSITIVE FEEDBACK METHODS

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MASTER OF TECHNOLOGY
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by

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I **JAY GAJJAR** Roll no: **2K23/VLS/11** hereby certify that the work which is being presented in the thesis entitled **Enhancing the DC Gain of the Operational amplifier by the use of Positive Feedback Methods** in partial fulfillment of the requirements for the award of the Degree of **Master of Technology**, submitted in the Department of **Electronics and Communication,** Delhi Technological University is an authentic record of my own work carried out during the period from June 2024 to May 2025 under the supervision of **PROF. ALOK KUMAR SINGH**

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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CERTIFICATE BY THE SUPERVISOR(s)

Certified that **JAY GAJJAR** Roll no: **2K23/VLS/11** has carried out their search work presented in this thesis entitled **Enhancing the DC Gain of the Operational amplifier by the use of Positive Feedback Methods** the degree of **Master of Technology** from Department of Electronics and Communication, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

Place: Delhi
Date: 31st may 2025

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ABSTRACT

One of the key components of integrated systems are operational amplifiers, or Op-amps. Band gap voltage references, digital-to-analog converters, sample-and-hold circuits, and very precise analog-to-digital converters are just a few of the uses for operational amplifiers with high speed and gain. Presenting the architecture of a high DC-gain operational trans-conductance amplifier (OTA) is the aim of this study. In order to do this, the output resistance and, consequently, the DC-gain are increased using the positive feedback technique. Other operational amplifier characteristics, such unity gain bandwidth and stability, are unaffected by the suggested configuration. Some simulations are run in a 0.18 μm CMOS process with a supply voltage of 1.4 V in order to evaluate the performance of the suggested structures. The results of the simulation demonstrate that the suggested operational amplifier performs better than the current constructions.

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CHAPTER 1

INTRODUCTION AND CIRCUIT OPERATION

The fundamental component of many analogue and mixed (analog-digital) circuits are operational amplifiers, or op-amps. From DC bias generation to high-speed amplification or filtering, op-amps of variable complexity are frequently utilised to achieve a variety of tasks. A high-gain differential amplifier is known as an op-amp [1-4]. Increasing the DC-gain is one of the main goals of op-amp designs. A variety of approaches, each with unique properties, are used to boost the gain. There is always a tradeoff between an op-amp's parameters, and it is evident that not all of them can be improved [5-8].

A two-stage op-amp is used to achieve both high gain and high swing, giving the first stage high gain and the second stage strong swing. Although the second stage is often a common source stage with an active load to give maximum output swing, each stage may incorporate various structures [9–12]. Numerous papers or researches have examined the idea of using positive feedback. Creating a negative resistance at the output node is the fundamental characteristic of the structures that have been presented. In this case, the output node experiences a significant resistance, which raises the DC-gain [13–16]. In [17], the outputs are connected to the bulk terminal to generate positive feedback. Here, the voltage applied to the transistors' bulk terminal is managed by voltage divider resistors. It has been demonstrated that this method can improve the benefit by up to ten times. Naturally, there is a ten-year reduction in the first pole. The remaining zeros and poles, however, don't alter. The DC-gain has been raised in the folded cascode in [18] by applying positive feedback to the majority of output transistors.

However, the positive feedback node is where the circuit's dominant pole is located. However, the effect of this pole is neutralised by the zero in this path. The longer sitting time is this method's primary drawback. The circuit in [19] has a cross connection at the output and a common source structure. The output resistance and, thus, the DC-gain are increased by the positive feedback mechanism. Furthermore, they eliminate the need for common mode feedback in circuit design. An operational trans-conductance amplifier (OTA) of class AB with enhanced common mode behaviour is introduced in [8].

The findings of the simulation, which was conducted using 40-nm technology, demonstrate that the common mode behaviour has improved without compromising the differential mode behaviour. However, there is a modest increase in both area and power consumption. An OTA that uses threshold voltage lowering is shown in reference [8]. It has been demonstrated that for the cell to operate correctly, the input

common mode voltage must be higher than $V_{TH}+2V_{OV}$, where V_{OV} is the overdrive voltage and V_{TH} is the MOSFET's threshold voltage.

This value is lowered by the subthreshold region's input transistor bias, although the allowable input common mode voltage has a lower limit. Line-to-line swing can be achieved by increasing the common mode voltage range of the PMOS input by utilising the complementary structure. A novel structure with enhanced gain is introduced in this study. The DC-gain rises as a result of positive feedback raising the output resistance.

1.1 Proposed Circuit and working

This section presents a suggested OTA based on encouraging comments along with pertinent analysis. Figure 1.1 displays the proposed circuit's schematic. By employing improved recycling structure (IRS) approaches, which create distinct AC and DC channels, it has been attempted to expand the circuit unit's gain bandwidth [15]. Additionally, the output resistance and, thus, the DC-gain are improved by employing the positive feedback technique.

For adaptive biassing, the suggested circuit makes use of a flipped voltage follower (FVF) [16]. The gate voltage of M4a and M2a will rise in response to an increase in Vi+. Following that, M4c and M4d's source voltage rises as well, which causes their current to rise as well. M2b and M4c's gate voltage and M4a and M4b's source both drop as Vi-drops, resulting in a drop in these transistors' gate-source voltage and M4a and M4b's current. As a result, the transistors' current varies based on the inputs when FVF is used. We then examine the circuit's characteristics.

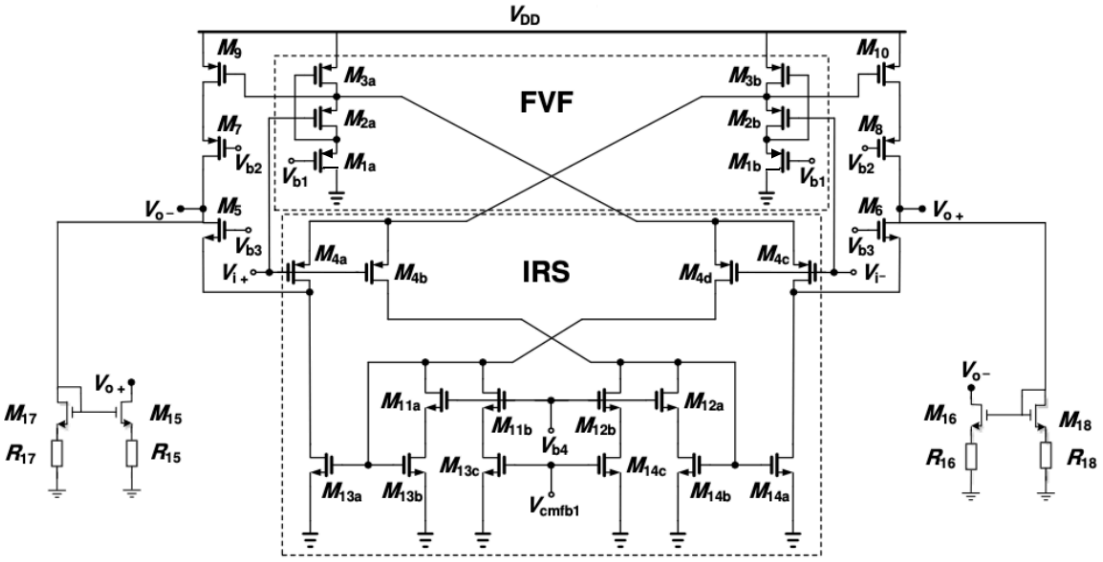

Fig. 1.1 Schematic of the proposed amplifier circuit

The AC and DC paths are kept apart in the suggested circuit. M11b, M14c, M13c, and M12b exhibit considerable resistance to AC current when DC current flows through them. Trans-conductance rises with distinct AC and DC pathways,]increasing bandwidth. As current sources, a group of transistors (M15, M16, M17, M18) and resistors (R15, R16, R17, R18) are employed. A positive feedback loop is produced by connecting the output signal Vo to the drain M15 and Vo to the drain M16.

This circuit is a high-performance fully differential operational amplifier architecture that integrates two key building blocks:

1. **Flipped Voltage Follower (FVF)**
2. **Improved Recycling Structure (IRS)**

These techniques are employed to enhance gain, bandwidth, and slew rate while maintaining low power consumption.

1. Flipped Voltage Follower (FVF)

The Flipped Voltage Follower (FVF) is a current buffer topology that provides low output impedance and high speed. In this circuit:

- Transistors M3a, M3b, M2a, M2b, M1a, M1b form the FVF blocks.
- The FVF provides a fast local feedback to regulate the gate voltages of the input differential pair, improving bandwidth and stability.
- Transistors M7 and M8 act as load elements or active current mirrors.
- This configuration helps in reducing the effective resistance seen by the current source, improving slew rate and settling time.

2. Improved Recycling Structure (IRS)

The IRS aims to reuse the current from the tail transistors for increasing transconductance without increasing power.

- The IRS block is formed by transistors M4a, M4b, M4c, M4d, and the folded cascode branches M11, M12, M13, M14, etc.
- It utilizes multiple paths to split and steer the tail current into the differential input pair and gain-boosting stages.
- Transistors M13a, M13b, M14a, M14b work as auxiliary current mirrors, boosting overall transconductance.

3. Common-Mode Feedback (CMFB)

To ensure proper biasing and differential operation, a common-mode feedback circuit (CMFB) is required:

- It senses the average of the output nodes (Vo+ and Vo−) and adjusts the biasing of tail transistors to maintain a stable common-mode level.
- The Vcmfb1 node acts as the control voltage for the CMFB loop.

4. Biasing and Output

- M5 and M6 are typically part of the differential input stage, controlling the input pair and setting the differential gain.
- Vo+ and Vo− are the fully differential outputs.
- Bias voltages (Vb1, Vb2, Vb3, etc.) are generated using bias circuits not shown in the schematic but are assumed to provide stable references.

5. Differential Outputs

- The amplifier provides differential outputs at **Vo+** and **Vo−**.
- Resistors **R15–R18** and transistors **M15–M18** are used for loading and bias stabilization.

Key Advantages

- High transconductance due to current reuse (IRS)
- Improved bandwidth and slew rate with FVF
- Low power design with high gain
- Suitable for low-voltage, high-speed analog applications such as ADCs, data converters, and sensor interfaces.
- Fully Differential Operation: Improves common-mode noise rejection.
- High Gain and Bandwidth: Enabled by IRS and FVF integration.
- Low Output Impedance: Due to FVF stage.
- Power Efficient: IRS enhances gm without drawing extra current.

1.2 Proposed Circuit Trans-conductance

An amplifier's transconductance is a crucial property that determines how well it transforms input voltage into output current.
The trans-conductance of the suggested circuit can be determined by the following analysis:

$G_{m,\,pro} = g_{m4a}(1+\alpha_1)+g_{m9}$

The trans-conductance of transistors is denoted by g_m in the equation above. It should be mentioned that the M_{14b}:M_{14a} transistor ratio is set at 1:α_1. For instance, the trans-conductance can be enhanced six times by modifying this ratio.

1.3 Amplifier Gain

The voltage gain of an operational amplifier is defined as the ratio of its output voltage to its differential input voltage.

An electronic device known as an amplifier controls a bigger electrical signal with a smaller one. Current or voltage can be used to control the output signal. An external

DC source is used by an amplifier to produce a bigger replica of the input signal. As a result, an additional power source is required for every amplifier. Gain is the capacity of each amplifier to amplify a signal. Since gain is a ratio, it has no units. The ratios of an amplifier's output current to input current, output voltage to input voltage, and output power to input power are known as current gain, voltage gain, and power gain, respectively.

The input signal is not always amplified to the same degree by an amplifier. It might react to AC and DC signals in different ways. The ratio of the change in the input signal to the change in the output signal is another way to express gain. This illustrates how much an input change affects the output. Although the rms value of the input and output signals can be used to compute gain, AC signals cannot be used with this method.

Decibel Gain or dB Gain

Since amplifier gain is a ratio of similar signals, it lacks units. The decibel (dB), or one-tenth of a bel, is the unit used to represent it on a logarithmic scale. Alexander Graham Bell, the man who invented the telephone, is the source of the word "bel."
The common (base 10) logarithm of a power ratio is now used to describe decibel gain. For example, if an amplifier's conventional gain is Poutput / Pinput, then its decibel scale value is 10log(Poutput / Pinput).

In the case of a completely differential amplifier, this is commonly stated as:

$$Av = \frac{Vo+ - Vo-}{Vin+ - Vin-} \tag{2.1}$$

The following relations can be used to compute the OTA's DC-gain.

$$Av = G_{m,pro}R_{out} \tag{2.2}$$

$$Rout = [g_{m7}r_{ds7}r_{ds9}||g_{m5}r_{ds5}(r_{ds4a}||r_{ds13a}))]||R_{cs} \tag{2.3}$$

The output resistance in the corresponding tiny signal is denoted by r_{ds}. R_{CS} creates negative resistance.

$$Rcs = \frac{1}{\frac{gm17}{1+gm17R17} + \frac{1}{gm16rds16R16 + rds16 + R16} - \frac{gm16}{1+gm16R16}} \tag{2.4}$$

The differential benefit rises sharply if the denominator of equation (2.4) is positive but near zero.

1.4 Slew Rate

The letter "S," which stands for "slew rate" in electrons, is simply the rate at which the op-amp's output voltage (Vo) varies with each unit of time. It is essential for determining the ideal maximum input frequency and amplitude so that the op-amp's output is not significantly affected.
Therefore, to guarantee the maximum undistorted o/p voltage swing, the slew rate needs to be high. It is employed to confirm whether or not an operational amplifier is capable of providing a dependable output to the input. Once the voltage gain is altered, this factor will also be altered. As a result, it is typically defined with a gain of unity.
For example, if 10 V/μs is the general-purpose op-amp's slew rate value. The gadget can produce 10 volts and an output in less than a microsecond when a large step i/p signal is applied to the input.

Formula for Slew Rate and Its Units

(S) = ΔVout/Δt is the formula for the slew rate. The units of slew rate are either Volts per second or V/μs.

Slew Rate vs Bandwidth

The slew rate and the bandwidth are two important ideas that are related to the op-amp speed. These two ideas are difficult to comprehend, particularly given their similarities. Together, they determine how long it takes to settle for a step response. Now, let's comprehend these two ideas.
Any signal change via an operational amplifier can be limited by the slew rate.

The highest slope in relation to the op-amp's slew rate is produced by multiplying the input sinusoidal signal by the op-amp gain. Instead of a curved portion of the sinusoidal signal, the output signal will be a straight line. Thus, the signal form may be altered or distorted by slewing.
The maximum speed at which it can respond to little variations in the signal is its bandwidth. Quiescent power can be used to create an operational amplifier at DC biases that can handle signals with relatively low amplitudes or tiny signals.
The addition of highly diverse frequencies, ranging from very little to very enormous, is what results from breaking down these signals using the Fourier Transform.
Higher bandwidth allows the operational amplifier to boost higher frequency signals, which results in faster speeds. The operational amplifier's ideal bandwidth value is reached at the frequency where the signal's gain is $1/\sqrt{2}$ (0.707). Thus, this is the maximum frequency at which an operational amplifier can perform as predicted.
For example, Texas Instrument's OPA333AIDBVT has a gain bandwidth (BW) of 250 kHz for a single closed-loop gain. It will be 165 kHz for a 2 gain, and so forth. Therefore, the product of the bandwidth and the gain constant will cause an operational amplifier to become slow, even the maximum closed-loop gain.

The slew rate can be computed based on the IRS circuit's relationships in [15]. The maximum slew rate in the suggested approach is:

$$SR_{IRS} = \frac{P(1-\alpha)Ib}{\alpha CL} \tag{2.5}$$

The SR is enhanced by selecting the appropriate values for P and α.

Slew Rate vs Frequency Response

The slew rate of an op-amp, which is commonly measured in volts per microsecond, is its capacity to react rapidly to a change in the input level. This standard has more to do with the amplifier's high-frequency response, even if it appears to be related to dynamic reaction.

The speed at which an amplifier may respond to an output change is known as the slew rate. We can observe that the amplitude of each sine wave is the same in a variety of waveforms with varied frequencies and equal amplitudes; the signal with the highest frequency has the largest voltage change per unit of time.

As a result, slew rate gradually increases with frequency until a threshold is reached when the slew rate is no longer able to keep up with the waveform's frequency,

The signal can then be severely distorted and degraded across a given location by a slew rate that affects the high-frequency response.

CHAPTER 2

SIMULATION RESULTS

2.1 Frequency Response Analysis

2.1.1 Schematic view

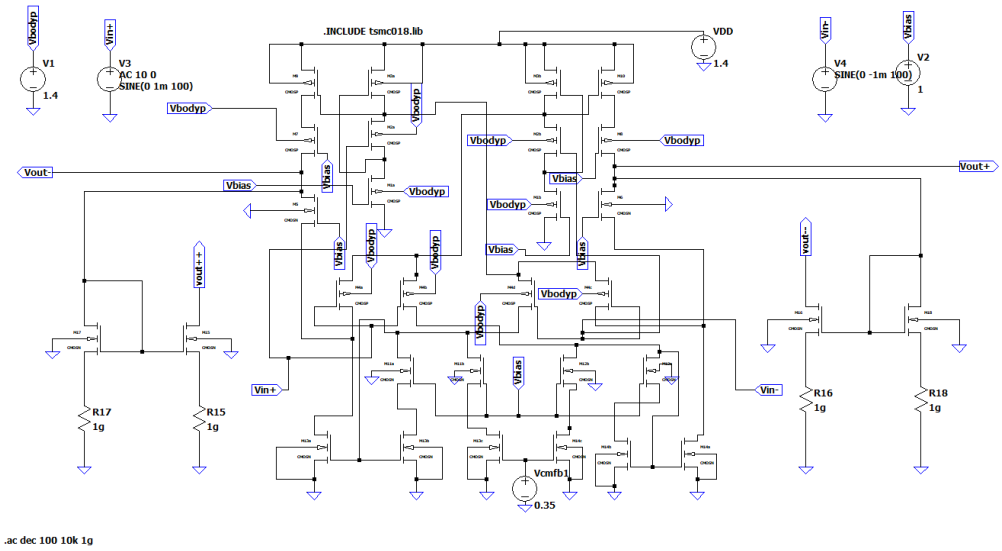

Fig. 2.1 Schematic View for frequency Response Analysis

This is a schematic diagram from LTspice, depicting a fully differential operational amplifier (most likely a common-mode feedback, two-stage op-amp). Here's a brief analysis:

Key Observations:

1. Power Supplies:

- V_{DD} = 1.4 V: Positive supply.
- V_{SS} = 0 V (implied): Ground reference.

2. Differential Inputs:

- The differential input terminals, Vin+ and Vin-, are located in the lower centre.

3. Differential Outputs:

- The amplifier's differential outputs are Vout+ and Vout-.

4. Biasing and Body Biasing:

- V_{bias} and V_{bodyp} signals are used for:
  Biasing current mirrors and other internal stages.
  Adjusting PMOS body bias (for threshold tuning or leakage control).

5. Common-Mode Feedback (CMFB):

- A CMFB circuit (notably the voltage source labeled V_{cmfb1} = 0.35 V) is included.
  This stabilizes the common-mode level of the outputs.

6. AC Analysis:

- The directive at the bottom: .ac dec 100 10k 1g
  Runs an AC sweep from 10 kHz to 1 GHz with 100 points/decade.
  Useful for frequency response analysis (gain, phase, bandwidth).

7. AC Signal Sources:

- V_3 and V_4: Sinewave AC inputs with magnitude 1mV and -1mV, respectively, used to drive V_{in+} and V_{in-} in opposite phases.

8. Transistors:

- All are labeled with CMOSN, CMOSP, suggesting TSMC 180nm process models are used (.include tsmc018.lib).

2.1.2 Output waveform

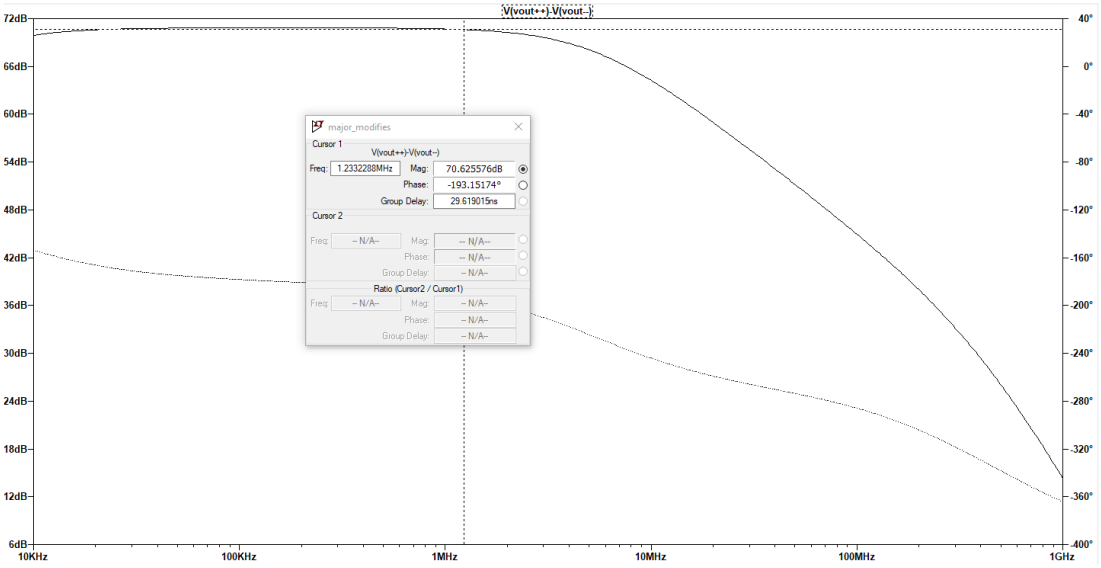

Fig. 2.2 Frequency response analysis for gain in LTSpice simulator

Key Observations:

1. Cursor Information:

- Magnitude (Gain): 70.62 dB
  This indicates a very strong amplification at this frequency.
- Group Delay: 29.58 ns
  This tells you how much time delay is introduced by the system at that frequency.

2. Green Traces on the Plot:

- Upper Plot (left Y-axis in dB): This is the gain (magnitude) of the differential output over a range of frequencies from 10 kHz to 1 GHz.
- Lower Plot (right Y-axis in degrees): This is the phase response over the same frequency range.

3. Frequency Response Behavior:

- At lower frequencies (left side of the graph), gain is flat and high (~70 dB).
- As frequency increases beyond ~1 MHz, the gain starts to roll off, which is typical for low-pass filters or amplifier bandwidth limits.

2.2 Power Consumption Analysis

2.2.1 Schematic view

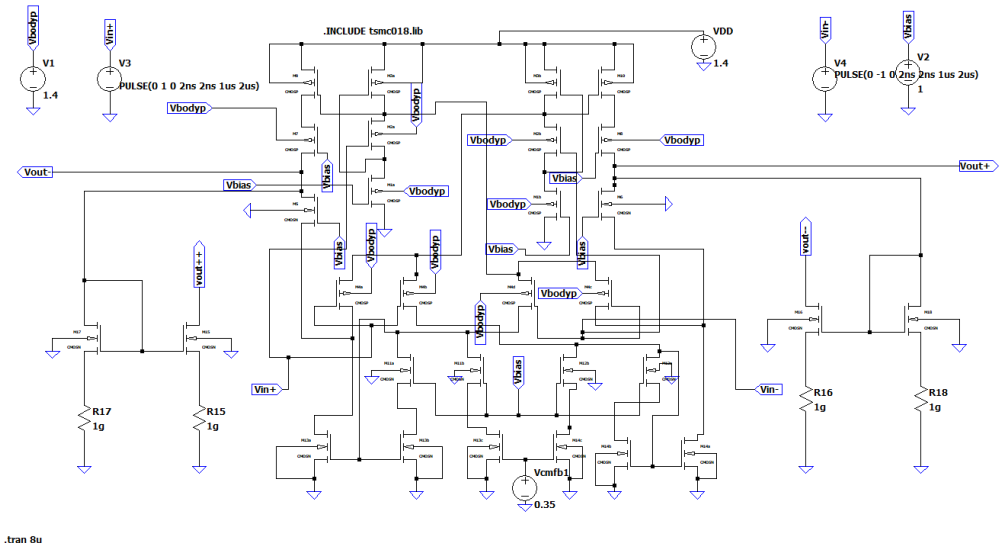

Fig 2.3 Schematic view for Power Analysis

Key observations

1. Power Supplies:

- V_{DD} = 1.4V: A single supply powers the circuit.
- V_{cmfb1} = 0.35V: The output common-mode level is stabilised by a common-mode feedback voltage.

2. Biasing:

- Multiple current mirrors and bias voltages (V_{bias} etc.) are used to establish appropriate current levels in various branches.
- These likely support folded cascode transistors, current sources, and body biasing for tuning threshold voltages.

3. Common-Mode Feedback (CMFB):

- CMFB circuitry is implemented to ensure the differential outputs (V_{out+}, V_{out-}) maintain the correct average voltage.

4. Pulse Sources:

- V3 and V4 are PULSE sources used for transient input testing (from 0 to 1 V or −1 V), suggesting the circuit is tested under dynamic (transient) conditions.

5. Simulation Command:

- .tran 8u: A transient analysis is specified for 8 microseconds.

2.2.2 Output Waveform

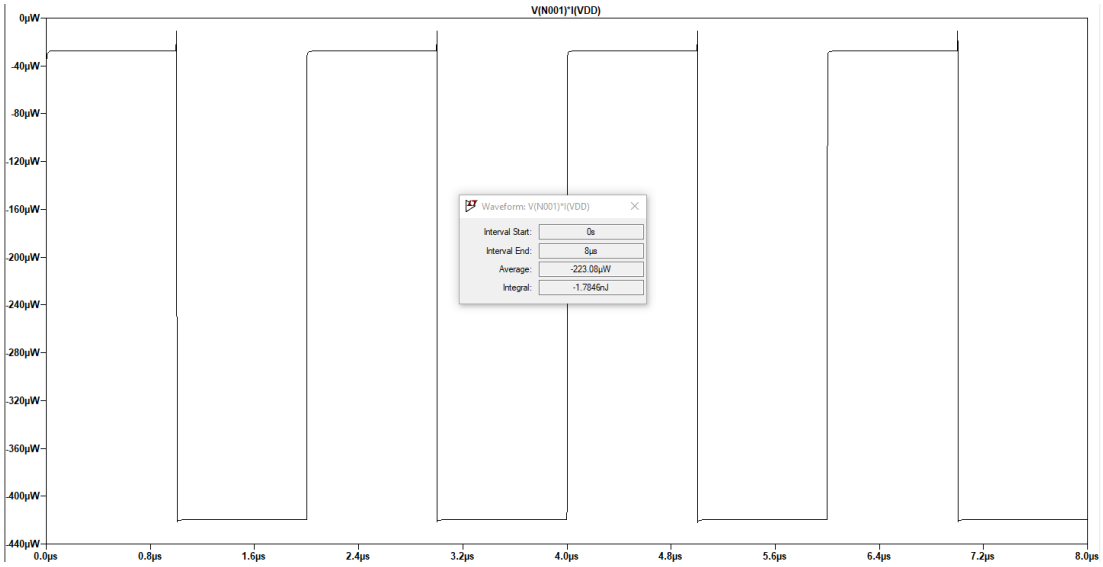

Fig. 2.4 Output graph for power consumption in LTSpice simulator

This waveform plot from LTspice shows the instantaneous power consumption of the circuit over time, calculated as:
Power = $V_{(N001)} \times I_{(VDD)}$
This is a common method to analyze dynamic power consumption of CMOS circuits.
The circuit consumes an average of ~223 µW over 8 µs.
Total energy consumed during this period is ~1.78 nJ.
The waveform confirms expected dynamic power consumption patterns in response to the pulsed differential inputs.

2.3 Noise Analysis

2.3.1 Schematic view

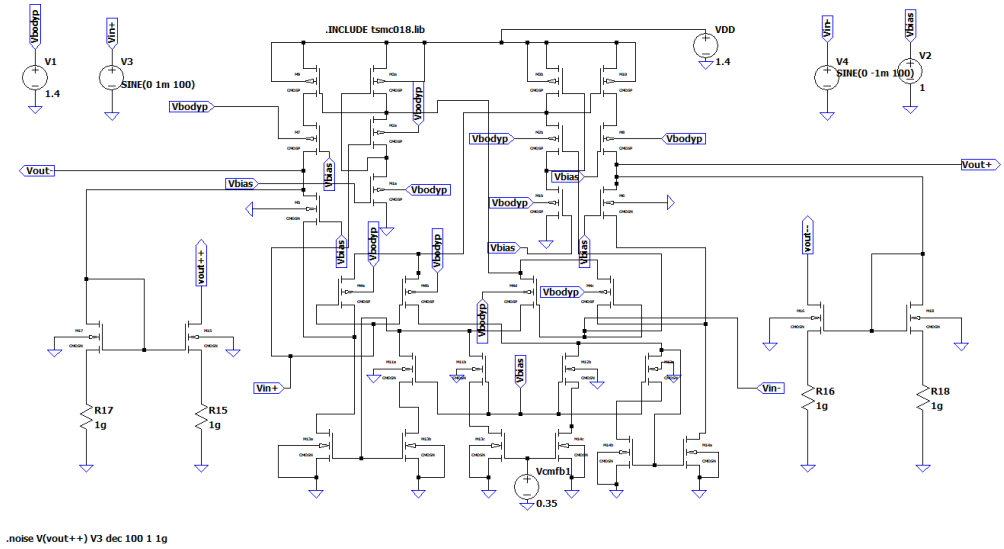

Fig. 2.5 Schematic view for Noise Analysis

Key observations

1. Power Supply

- V_{DD} = 1.4 V: The op-amp operates from a single 1.4V supply.
- Grounded nodes serve as V_{SS}

2. Signal Inputs

- AC Signal Sources:
  V3 and V4 provide a differential sinusoidal input (±1 mV at 100 Hz).
- This setup is used to analyze differential-mode performance.

3. Noise Analysis

- The directive at the bottom:
  .noise V(vout++) V3 dec 100 1 1g

Specifies a **noise analysis** across Vout++ with respect to the input source V3.

2.3.2 Output Waveform

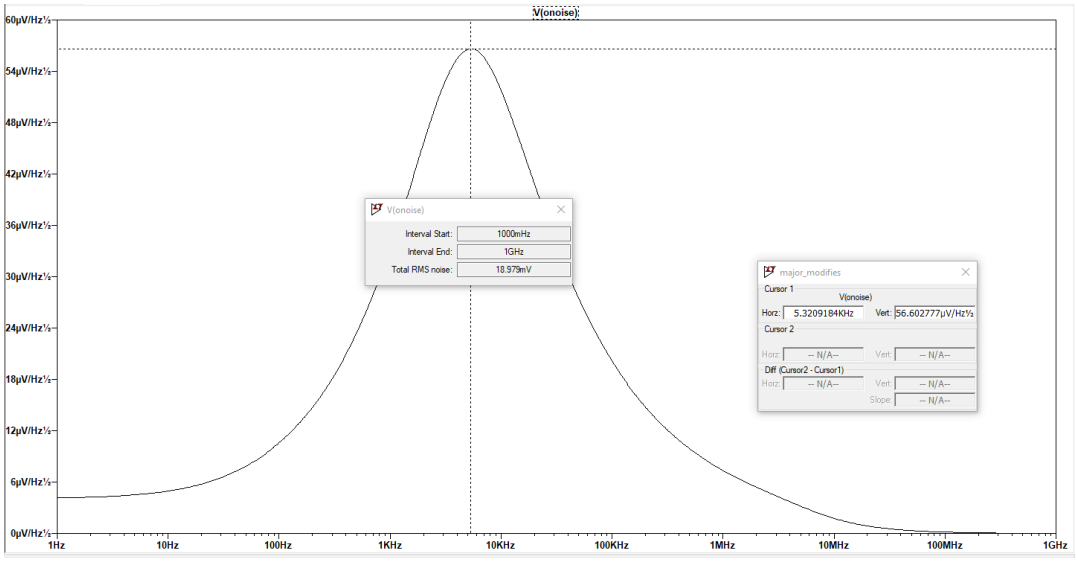

Fig. 2.6 Output waveform for Noise in LTSpice simulator

This is a noise analysis plot from LTspice, showing the output noise voltage density (V(noise)) versus frequency on a logarithmic scale.

Key Observations:

1. Plot Curve (Green Line):

- It shows the output noise spectral density (V/√Hz).
- The Y-axis is in µV/√Hz and the X-axis spans from 1 mHz to 1 GHz.

2. Noise Peak:

- There's a peak around 10 kHz, indicating the frequency where noise is maximum.
- Cursor 1 is set at 5.258 kHz, showing ~56.6 µV/√Hz at that point.

3. Integrated Noise (RMS):

- The small window in the center shows:
  Integration range: 1 mHz to 1 GHz.
  Total RMS noise: 18.979 mV, which is the total output noise over the entire frequency range.

CHAPTER 3

ENHANCEMENT FROM THE PREVIOUS WORK

3.1 Power supply V_{DD} = 1.4v

Lower Power Consumption:

- Power $P \propto VDD^2$ So, lowering VDD significantly reduces dynamic power.

Improved Battery Life (for portable applications):

- Battery-powered operation can be prolonged by reducing the amount of current drawn from the source.

Better for Scaling and Modern Processes:

- Lower supply voltages are preferred by more recent CMOS technologies in order to prevent reliability problems such as gate oxide breakdown and hot carrier effects.

Still Functional:

- It exhibits strong biassing and effective headroom control if your analogue performance (such as gain, bandwidth, and linearity) remains unaffected, particularly when you employ strategies like the IRS (Improved Regulated Structure) and FVF (Flipped Voltage Follower) blocks.

Designing for low supply voltage during fabrication enables:

- Better yield.
- Compatibility with advanced nodes.
- Low power, cost, and thermal budget.
- Long-term reliability of the product.

3.2 Applying one uniform/common biasing voltage

Advantages of Applying the Same Bias Voltage

1. Simplifies Circuit Design
   - Reduces the number of bias voltage generators or reference circuits required.
   - Easier to design, simulate, and debug.
   - Less routing complexity in layout.
2. Ensures Matching in Matched Pairs
   - For current mirrors, differential pairs, and other matched transistor configurations, using a single bias voltage improves matching.
   - Matched biasing reduces offset and improves common-mode rejection and linearity.
3. Reduces Area and Power
   - Fewer biasing networks save silicon area and power consumption.

- Especially useful in low-power, high-density analog ICs (e.g., op-amps, ADCs, filters).

4. Improves Process Robustness
   - Fewer bias voltages mean fewer dependencies on variations in process, voltage, and temperature (PVT).
   - Makes the design more robust across corners.
5. Minimizes Mismatch-Induced Errors
   - When all devices are biased identically, mismatch-induced performance
   - variations are minimized.
   - This is important in sensitive analog circuits, especially differential and gain stages.
6. Easier Testing and Characterization
   - Only one bias voltage to sweep/test during post-fabrication evaluation.
   - Speeds up production testing and calibration.

3.3 Uniform W/L ratio of NMOS and PMOS

1. Design Simplicity
   - Using a consistent ratio across the design reduces the number of design variables.
   - Makes manual calculation, simulation tuning, and biasing easier.
2. Better Design Symmetry
   - Using a fixed ratio helps maintain voltage symmetry in differential paths, mirrors, and current sources.
   - Particularly beneficial in balanced analog structures like the one you showed (e.g., differential pair + current mirrors).
3. Easier to Predict and Match Currents
   - Since PMOS transistors generally have lower mobility(μp), a sizing ratio like 3:1 helps match NMOS and PMOS current-driving capabilities.
   - This means simpler current mirroring and biasing with fewer compensation tweaks.
4. Improved Layout Regularity
   - Uniform sizing results in more compact, symmetric, and modular layouts, reducing parasitics and mismatch.
   - Enhances layout-dependent effects (LDE) resilience and overall yield.
5. Easier Maintenance and Scalability
   - If you need to revise or scale the design later (e.g., different process node), having uniform ratios simplifies the process.
   - Helps in porting circuits across technologies.

Using a fixed W/L ratio like PMOS = 3× NMOS is a highly efficient strategy when:

- You don’t lose analog performance (which is confirmed).

- The design is symmetric and well-matched.
- You want to minimize complexity, improve scalability, and optimize layout.

Table 2.1 Transistors Sizing

	Width(μm)	Length(nm)
PMOS	30	180
NMOS	10	180

Table 2.2 Comparison Table of previous work

	[8]	[12]	[13]	This work
I_{tot}(μA)	260	260	1100	300
V_{DD}(v)	1.8	1.8	1.8	1.4
Power(μW)	468	468	1980	223
Gain(dB)	65	70	68	71
Total RMS Noise(mV)	-	-	-	18.9
GBW(MHZ)	50	83	440	440
SR (V/μs)	23	38	740	740

CHAPTER 4

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

4.1 Conclusion

This research examined various approaches to improve DC-gain in operational amplifier design. The purpose of this study is to use the existing recycling framework to boost the trans-conductance. However, the output resistance has gone up with the aid of positive feedback. LT-Spice software was used for simulation following circuit design and analysis. Simulations using 1.4 V supply voltage and 180 nm technology have been conducted. Following the simulation, the circuit's DC-gain is 71 dB, Total RMS Noise is 18.9mV, Total Current I_{tot} is 300μA, GBW(MHZ) is 440, Slew rate(V/μs) is 740 and power consumption is 223μW. It was concluded that the circuit has strong stability and that its parameters are acceptable when compared to the current designs after it was examined in all different Scenarios or Cases and using manufacturing technologies.

4.2 Future Scope

Compact, low-power, high-speed, and highly linear amplifier topologies are becoming more and more necessary as analogue and mixed-signal systems continue to scale towards nanometre technologies. To improve performance in fully differential signal channels, the circuit in question combines the Flipped Voltage Follower (FVF) and Input Reuse Structure (IRS) approaches. Even if this architecture shows encouraging outcomes, there are still a number of areas that could use more study and improvement. The future potential for improving and extending this design's capabilities is described in this section.

4.2.1. Performance Optimization

a. Power Consumption Reduction
The existing design can still be optimised for ultra-low-power applications, including biomedical implants or Internet of Things nodes, even with speed and bandwidth upgrades. Without significantly affecting performance, strategies including dynamically biassed circuits, bias current scaling, and subthreshold operation may provide notable power reductions.

b. Bandwidth and Slew Rate Enhancement
Although the FVF setup offers a respectable bandwidth, future designs can aim for faster slew rates by utilising strategies like dynamic current mirrors or current-

boosted stages. The frequency responsiveness can also be enhanced by including regulated cascode buffers in the signal route.

c. Noise Reduction
Precision applications require low-noise operation, even if the IRS-FVF architecture improves linearity. Flicker and thermal noise can be further reduced by using noise-cancelling topologies, correlated double sampling (CDS), or chopper stabilisation.

4.2.2. Technology Scaling and Portability

a. Porting to Advanced CMOS Nodes
Analogue circuit performance is more susceptible to short-channel effects and decreased intrinsic gain as CMOS technology advances. An important topic of research is how to modify this design for deep submicron or FinFET nodes while preserving gain, bandwidth, and power efficiency.

b. Voltage Scalability
At 1.4V, the existing design functions. Modern systems, on the other hand, frequently run at lower supply voltages (1.2V or even less than 1V). The circuit could be redesigned to operate effectively at lower supply voltages, making it appropriate for next-generation SoCs.

4.2.3. Robustness and Reliability

a. PVT Variability Tolerance
Process, voltage, and temperature (PVT) variations can cause mismatches and lower performance. Future iterations should include adaptive biassing and compensation networks to stabilise performance across wide PVT variations.

b. Temperature Compensation
Wide variations in temperature are typical, particularly in industrial or automotive settings. Circuit integrity can be preserved by implementing adaptive control loops or automatic temperature compensation techniques.

4.2.4. Layout and Mismatch Minimization

Analogue circuit performance is significantly impacted by the arrangement mismatches. Future improvements include:

- For crucial transistor pairs, the common-centroid arrangement is utilised.
- route that is symmetrical to preserve signal balance.
- To reduce substrate coupling, use isolation structures and guard rings.

Monte Carlo analysis and post-layout simulations should be used to confirm performance under parasitic effects and mismatch.

4.2.5. Integration and Application Prospects

a. Biomedical Signal Processing
For biological front-ends like ECG or EEG acquisition systems, the amplifier can be modified due to its capability for low-noise and low-power operation. For long-term operation, these applications require accuracy and low power consumption.

b. On-Chip Filters and Oscillators
The circuit could be utilised in transimpedance amplifiers, oscillators, and analogue filters as an operational transconductance amplifier (OTA). Future designs can investigate the possibility that these applications will need tweaking capabilities.

4.2.6. Advanced Features and Innovations

a. Digitally Assisted Analog Design
More resilient mixed-signal systems may result from the addition of digital calibration or control for offset cancellation, gain adjustment, or bias optimisation.

4.3 Social Impact

4.3.1. Accessibility & Inclusion

- Portable Medical gadgets: Wearable and battery-operated gadgets are made possible by their high-performance, low-power design, which increases access to healthcare in underprivileged or distant places.
- impact: By providing medical diagnostics in areas lacking strong infrastructure, it lessens health inequities.

4.3.2. Environmental Benefits

- Energy-Efficient Design: Low-power operation and reduced energy consumption are indicated by the application of techniques such as FVF and RGC.
- impact: Lessens the environmental impact of tech products and promotes sustainable technology.

4.3.3 Technological Innovation

- IoT and Edge Computing Enabling These amplifiers are essential to sensor interfaces in IoT systems, which enable improved transportation, agriculture, and cities.
- impact: Improves safety, quality of life, and societal resource efficiency.

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OBJECTIVE

I am motivated and enthusiastic with a strong interest in semiconductors and VLSI technology. Technology oriented student intern with good debugging and analytical skills, possessing good communication skills as well, currently looking for the job opportunities to apply my engineering knowledge for the growth of an organization while tailoring my own skills at the same time.

EDUCATION

Degree / Certificate	Year	Institute / Board	Percentage / CGPA
M.TECH (VLSI Design and Embedded System)	2023-2025	Delhi Technological University, New Delhi	7.87
B.TECH (Electronics and Communication Engineering)	2018-2022	Dharmsinh Desai University, Gujarat	7.98

EXPERIENCE

NXP Semiconductors **Noida, Uttar Pradesh**
Intern - Design-Enablement (Development: RTL to GDSII FLOW) **July 2024- June 2025**

- RTL to GDSll Design Methodologies and Tools Interns in semiconductor industry, experience in the development of flow automation for various Technodes (TSMC-5nm and 16nm, 22nm(GF-22FDXP)).
- Worked on Advance Parasitic Analysis environment using parasitic explorer, in the design virtual metal fill flow and Galaxy parasitic data base (GPD) vs SPEF enable performance boost, ease of debuggability and faster design closer with reduction in ECO loops.
- Explored the various aspects and attributes of Floorplan, Placement, CTS and Routing.
- Hands on experience on Synopsys tools like StarRC, Fusion Compiler and Synopsys LYNX flow, low geometry node issues. Worked with EDA Team in reviewing & resolving blocking issues in project. Develop, integrate and release new features in our high performance RTL to GDSll CAD flow. Provided support to the design team on **6 tape-out** within 6 months.
- Experience in Customizing flows & methodology to meet low power & area objectives of SOC, Strong scripting skills for Automation and Flow development using TCL and Python. Ability to work independently and as a part of team.
- Worked with EDA vendors to proactively review latest tools and flow offerings in RTL to GDSll domain. Evaluate latest offerings and benchmark with organization used tools, flows, and methodologies.
- Consolidate device test structure requirements as per project achievements of technology node development and with various teams to achieve defined metrics and timelines, Work closely with worldwide Physical design team and provide methodology guidance, tools/flows support and help achieve class-leading PPA.
- Strong communication skills (written and verbal), problem solving, attention to detail, commitment to test, and quality focus. Can-do attitude, openness to new environment, people and culture.

TECHNICAL SKILLS

- **Programming Languages:** Python, TCL, Basic oops concepts in python
- **Design Tools:** fc_shell, starrc_shell, LtSpice, Xilinx Vivado, GIT
- **Key Courses:** Digital electronics, Physical Design, Digital IC Design, Parasitic Extraction, VMF Flow

ACADEMIC PROJECTS

- **Traffic Light controller using Verilog (Software : Xilinx Vivado**) **Oct 2023 - Dec 2023**
  In this project we introduced traffic light controller for T-Intersection, We conclude that it provides powerful solution to improve existing system With new smart traffic light controller.
- **Traffic sign recognition using Python (Software : Anaconda Navigator)** **June 2023 - Aug 2023**
  The aim of the project is to detect and recognize traffic signs which present in the image. Traffic sign recognition (TSR) is used to regulate traffic signs, warn a driver, and command or prohibit certain actions.

CERTIFICATES AND ACHIVEMENTS

- **StarRC: Foundation** course from SYNOPSYS SolvNetPlus **Dec 2024**
- Certificate of **Fusion compiler: Synthesis and Design Implementation Jumpstart Training** **Sep 2024**
- Certificate of **LynxNXT: Foundation** Course from SYNOPSYS SolvNetPlus **Sep 2024**
- **GATE 2023** Organised by IIT Kanpur Qualified **March 2023**