STUDY AND DESIGN OF CHAOTIC OSCILLATORS USING ACTIVE BUILDING BLOCKS

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by

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Certified that **BRIJ NANDAN SINGH** Roll no: **2K23/VLS/01** has carried out their research work presented in this thesis entitled **Study and Design of Chaotic Oscillators using Active Building Blocks** for the degree of **Master of Technology** from Department of Electronics and Communication, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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I **BRIJ NANDAN SINGH** Roll no: **2K23/VLS/01** hereby certify that the work which is being presented in the thesis entitled **Study and Design of Chaotic Oscillators using Active Building Blocks** in partial fulfillment of the requirements for the award of the Degree of **Master of Technology**, submitted in the Department of **Electronics and Communication,** Delhi Technological University is an authentic record of my own work carried out during the period from June 2024 to June 2025 under the supervision of **Dr. KRITI SUNEJA .**

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Place: New Delhi **BRIJ NANDAN SINGH**

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ABSTRACT

For a long time, people have captured by and continued to study chaotic circuits because of their detailed and unpredictable nature. This exploration reviews chaotic circuits, covering their core concepts, how they are used and the consequences of using them. We explore how the main theories behind chaotic behavior are explained by how feedback loops and nonlinearity add to these electrical system dynamics. Several circuit topologies known for their chaotic behavior, for example the Lorenz system and Chua's circuit and their corresponding representing mathematical models are covered in the article. In addition, we study how chaotic circuits are use in several fields, including optimization strategies, generating numbers randomly and secure communications.

Nonlinear components in the equations that manage chaos cause the system's results to be complex. Several types of nonlinearities found in chaotic systems are quadratic, exponential and hyperbolic. Typically, a chaotic system is defined by equations involving nonlinear terms and by adding, subtracting and scaling variables. In hardware for chaotic systems, operational amplifiers (Opamps) are used as common active elements. Since these current mode active blocks can pass signals of both current and voltage, their designs are often more compact.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

DVCCTA : Differential Voltage Current Conveyor Transconductance Amplifier
CFOA : Current Feedback Operational Amplifier
OTRA : Operational Trans Resistance Amplifier
VDBA : Voltage Differencing Buffered Amplifier
CCII : Current Conveyer II
VDTA : Voltage Differencing Transconductance Amplifier
FTFN : Four Terminal Floating Nullor
DC : Direct Current
I : Current
V : Voltage
FDNR : Frequency Dependent Negative Resistor
CMOS : Complementary Metal Oxide Semiconductor
KHz : Kilohertz
MHz : Megahertz
GHz : Gigahertz
R : Resistor
L : Inductor
C : Capacitor
IC : Integrated Circuits
MOS : Metal Oxide Semiconductor
TSMC : Taiwan Semiconductor Manufacturing Company
Max. : Maximum
Min. : Minimum
u : Micro(10^-6)
m : Milli(10^-3)
ASIC : Application Specific Integrated Circuits
ECG : Electrocardiography
AI : Artificial Intelligence
SDGs : Sustainable Development Goals
5G : Fifth Generation

LIST OF PUBLICATIONS

[1] B N Singh and K. Suneja, " Realization of Chaotic Circuit using Different Analog Building Blocks and its use in secure Communication," *International Conference on Data Science and Applications (ICDSA 2025) accepted to be presented on July 16-18, 2025, at Malaviya National Institute of Technology Jaipur, India*.

CHAPTER 1

INTRODUCTION

1.1 Background

In 1983, Leon Chua [1] described his circuit, and it turned out to be a central topic in the fields of nonlinear dynamics and chaos theory. Through combining theory with experiments on this circuit, it has revealed more about deterministic chaos. Below, you will find a summary of how electricity became important, its applications now and how it might be used in future, based on knowledge from research and practical applications. In chaotic dynamics, plain and fixed rules create the illusion of randomness. Systems like these, found in finance and meteorology, all have three traits: complicated patterns, nonlinear behavior and extreme sensitivity to their beginning state. Weather outcomes are sometimes radically different just because of a little change in basic temperature.

Just as in weather systems, the motions of fluids can also become complex and filled with random patterns. Chaotic systems can show up in the world of life science too, like when species interact or when diseases are being spread between them. Multi-variable actions in financing markets are mirrored by macroeconomic models and the movements of stock markets which commonly appear chaotic. Communication systems [10] once relied on chaotic circuits to secure the way they sent information through telecommunications technology. It is important that secure communications hide the contents of the information delivered from potential eavesdroppers. Even in the abstract world of mathematics, chaotic maps and fractals demonstrate how simple equations can generate complex and unpredictable patterns, underscoring the ubiquity of chaos in both natural and abstract systems.

1.2 Realization of chaotic systems using Active Building blocks

To make chaotic systems with analog tools, we use the complex nature of physical parts to model the behavior of chaos in mathematics and in the real world. Chaos theory can be examined by researchers and engineers using analog circuits which let them control and investigate chaotic elements.

Because of the careful arrangement of circuits including nonlinear elements such as Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [14], Current Feedback Operational Amplifier (CFOA) [17], Operational Trans resistance Amplifier (OTRA) [13], Voltage Differencing Buffered Amplifier (VDBA) [16], Current Conveyor- II (CC-II) [15] and Voltage Differencing Transconductance Amplifier (VDTA) [7]. We can create systems that behave in a chaotic way. Table 1.1 illustrates the evaluation of the different active building blocks.

Analog implementations make it possible to explore the behavior of chaotic systems by connecting theory to experiments. Several domains make use of them such as random encryption, the production of random numbers and secure conversations. No matter the advances in technology, analog models of chaotic systems are still important for interpreting and working with different forms of nonlinearity found in the world.

By applying constituent governing equations, it becomes possible to realize other chaotic systems in hardware. It is usually necessary to use three state variable energy reservoirs to build a chaotic system in hardware. Here, AD712 Opamp [4] blocks are included to fabricate a summer/subtractor, buffer and invertor that are required in secure communication.

1.3 Synchronization in chaotic systems

Sometimes, chaotic systems can become coordinated even though they both seem to show totally random behaviors. How strongly correlated the systems are will decide if the synchronization is complete or just general. Even though their histories are very different, these systems end up following the same path over time. Although their developments follow distinct paths, generalized synchronization makes it possible for the systems to be related.

It is often needed to link different parts of chaotic systems by feedback loops to keep them synchronized. By changing the coupling and other parameters, researchers can create synchronization between the systems. The result can be seen in secure communication, where both encryption and decryption depend on chaotic systems that are synchronized.

1.4 Chua’s Circuit

Chua's circuit [1] was initially presented in 1984, and it caused experimental pandemonium. This electronic chaotic circuit has been utilized in numerous chaos-related fields. It is well-liked because it displays a variety of chaotic behaviors that more intricate circuits display.

1.4.1 Chua's Circuit Description

Chua's circuit features three elements that safely store energy. C1, C2 and L are the three components of the circuit that hold the energy. Many of these parts are available to purchase right away. The network includes a passive component R which helps dissipate energy. Using a variable resistor or potentiometer that the user can adjust helps create chaos in a couple of ways.

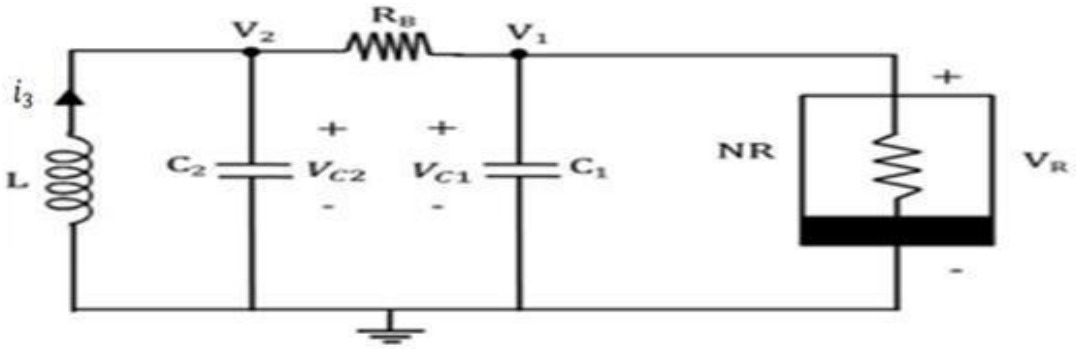

Fig. 1.1: Chua's Circuit

Such systems can be set up to look at chaotic and complex behavior. One basically needs Chua's diode, a key object that behaves as a negative resistor, to build nonlinear active systems. A circuit is made of semiconductors, passive resistors and a battery. It is designated by the name NR. The V2 and V1 were aimed at demonstrating how oscillations occur. The following set of equations are used to describe the Chua's Circuit dynamics [4]:

$$C_1 \frac{dv_1}{dt} = G(v_2 - v_1) - f(v_1) \quad (1.1)$$

$$C_2 \frac{dv_2}{dt} = G(v_1 - v_2) + i_3 \quad (1.2)$$

$$L \frac{di_3}{dt} = -v_2 \quad (1.3)$$

where voltage across capacitor C1 is $\mathbf{V_1}$, voltage across capacitor C_2 is $\mathbf{V_2}$, current across inductor L is $\mathbf{i_3}$ and **f(v1)** nonlinear function and **G** is reciprocal of **R**.

1.4.2 Chua's Diode [4]

The way Chua's Circuit behaves depends on C1, C2, L, R and a specific nonlinear characteristics function. Several active electronic components are used in this thesis to realize the Chua's diode for chaos creation. To get chaos in a circuit, a non-linear component should be included. The irregular feature in the system is the Chua's diode. Defined parts and ordinary batteries can be combined to make a chua diode.

Fig. 1.2: Chua Diode Symbol

1.4.3 V-I Characteristics of Chua's Circuit

Nonlinear function of voltage A locally active resistor is represented by iR = f (vR), whose slope on the curve is negative. The Chua circuit provides piecewise odd linear-symmetric characteristics for three segments. The following equation defines this relation [4].

$$i_R = f(v_R) = G_b v_R + 0.5 \cdot (G_a - G_b)\left(\left|v_R + B_p\right| - \left|v_R - B_p\right|\right) \tag{1.4}$$

where i_R current through chua diode, v_R is voltagr across it, G_a and G_b are the slopes and ± Bp denote the breakpoint

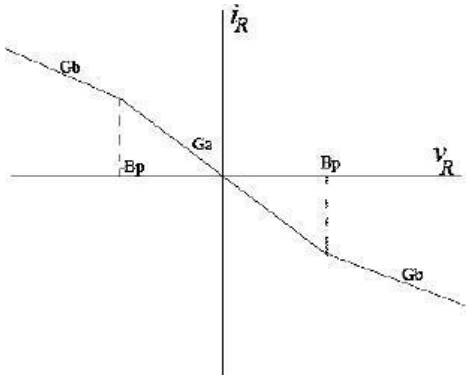

Fig. 1.3: V-I Characteristics of Chua's Circuit

1.5 Conclusion

Even though it is built with only resistors, an inductor, capacitors and the nonlinear Chua diode, the circuit is famous for creating the well-known double scroll shape in chaotic attractors. The model of this system which depends on three different differential equations, enables researchers to thoroughly study chaos through topological entropy and bifurcations. Since its output cannot be controlled, chaotic signals from the circuit serve as the base for data encryption and cryptography. In the next chapters, we will learn how using active building pieces can produce chaotic circuits and help transmit secure messages.

CHAPTER 2

BASIC TERMINOLOGY

2.1 Introduction

Chaotic systems make it easy to explain the difficulties of dynamical systems which is why they keep advancing. Chaotic systems are defined by three state variables whose behavior is regulated by specific rules. The connection between state variables and constant parameters is shown in the system using non-linear differential equations. To know the necessary parameter values, bifurcation diagrams are used and to see the detailed characteristics of chaotic systems, numerical simulations are carried out. Terms linked to chaotic systems are being provided in this chapter for your convenience.

2.2 Active Building Blocks

In this chapter we are discussing about different Active building Blocks. They are AD712 Opamp [4], AD844 [7] based FTFN [5] and VDTA [9].

2.2.1 AD712 Opamp

Analog Devices is behind the AD712, a cutting-edge operational amplifier that handles high speeds and accuracy. Because its noise is very low, its slew rate is high and its input bias current is low, it is well suited to applications where putting together accurate analog signals is required. Many applications in medical electronics, instrumentation and analog circuit research make use of this twin op-amp integrated circuit, mainly because it allows for both accurate and speedy amplification. The Port characteristics of an AD712 can be described as below equations:

$$V_{out} = A(V_+ - V_-) \tag{2.1}$$

where **Vout** is the output voltage, **A** represents the voltage gain of AD712, **V+** and **V-** are the voltages at noninverting and inverting terminals.

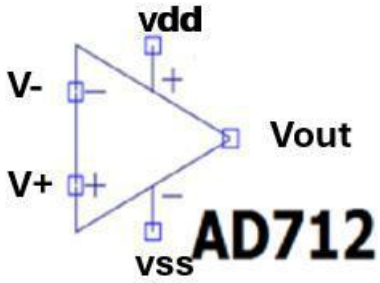

Fig. 2.1: Symbol of AD712

The Ltspice simulations are performed, taking supply voltages as ± 9V. The DC current characteristic of AD712 is shown in Fig. 2.3.

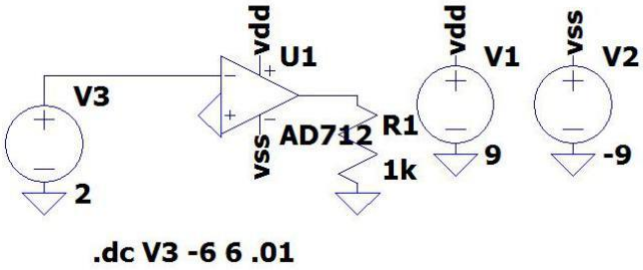

Fig. 2.2: Schematic of AD712 Opamp

Fig. 2.3: I-V characteristics of AD712 Opamp

2.2.1.1 Basic Circuit Applications of AD712

This sub-section describes the basic circuit applications of AD712 which have been used in the upcoming part of this thesis.

2.2.1.1.1 Buffer

The op-amp circuit with the simplest task is the buffer or voltage follower. The setup works by connecting the input to the non-inverting terminal and leads the output to the inverting input (negative feedback) directly. It provides the right impedance matching since it offers a unity gain (what goes in equals what comes out) with much less output impedance and a high level of input impedance. It keeps loading effects at bay by separating each stage in an analog signal system.

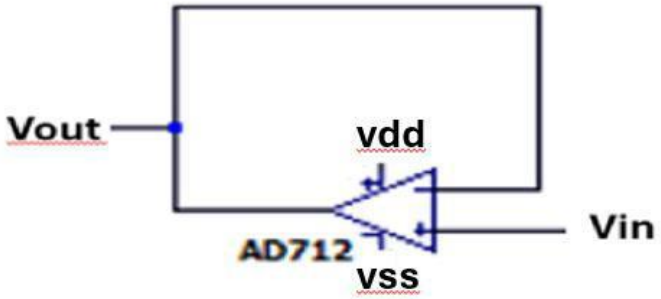

Fig. 2.4: Buffer using Ad712 Opamp

2.2.1.1.2 Subtractor/Summer

A subtractor/summer uses an op-amp with multiple inputs and weighted resistors to perform arithmetic operations.

Subtractor: It provides an output proportional to the difference between two input voltages (Vout = R2/R1 x (Vin1 – Vin2)).

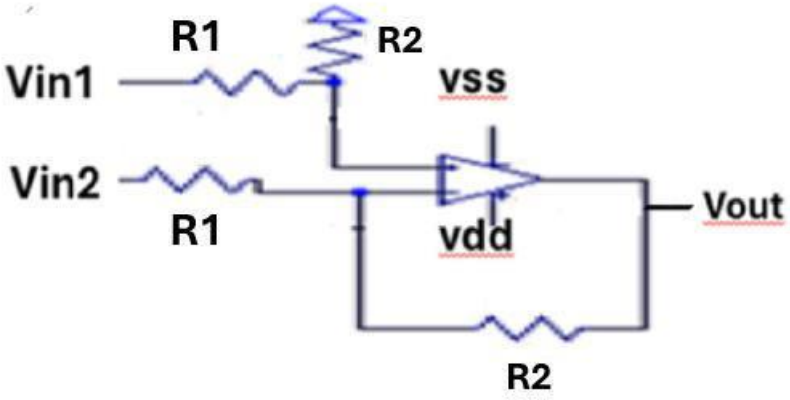

Fig. 2.5: Subtractor circuit using AD712 Opamp

Summer: It adds weighted inputs using inverting or non-inverting configurations (Vout = -Rf/R1 × (Vin1 + Vin2)).

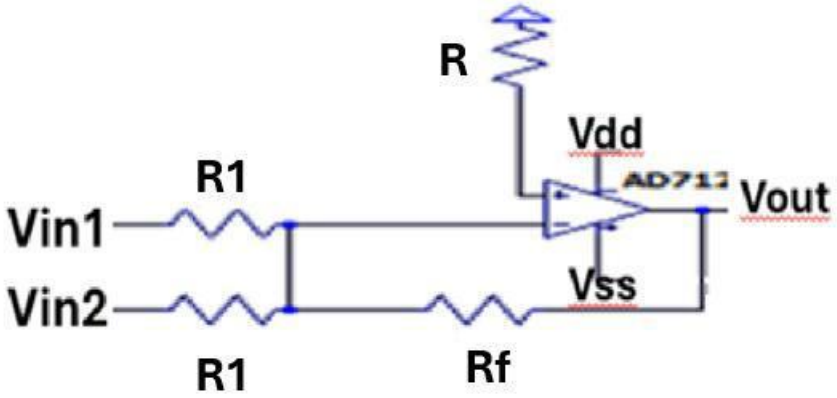

Fig. 2.6: Summer circuit using AD712 Opamp

2.2.1.1.3 Inverter

The Opamp, together with a resistor, is used by an inverting amplifier to switch the polarity of the input signal. When Rf acts as the feedback resistor and Ri is the input resistor, we calculate Vout as − (Rf/Ri) × Vin. If a circuit needs phase reversal, it is used in oscillators, filters and signal processing circuits.

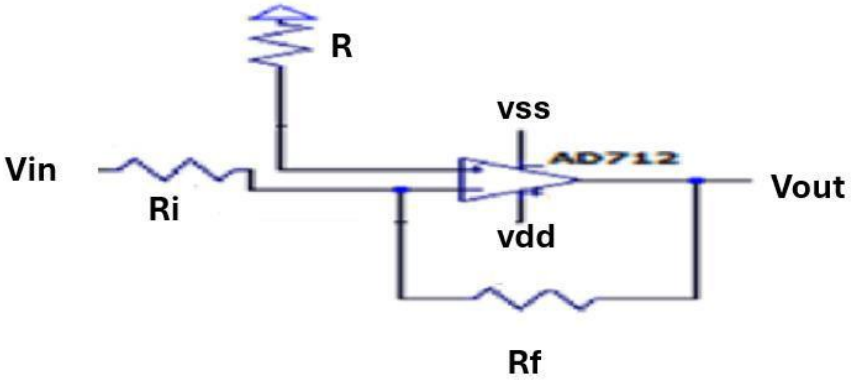

Fig. 2.7: Invertor circuit using AD712 Opamp

2.2.2 AD844 based FTFN [5]

The AD844 from Analog Devices is suitable for use as a floating transimpedance amplifier or as a first-generation current conveyor (CCII). A hub is needed since it allows the formation of a Four Terminal Floating Nullor (FTFN). Apart from power sources, the FTFN has four terminals. X, Y, Z and W are what they are called. This section provides equations to describe the port features of an FTFN.

$$Vx = Vy \quad (2.2)$$
$$Ix = Iy = 0 \quad (2.3)$$
$$Iz = Iw \quad (2.4)$$

Fig: 2.8, Fig: 2.9 represents the symbol representation using AD844 based FTFN and current characteristics in LTSPICE respectively.

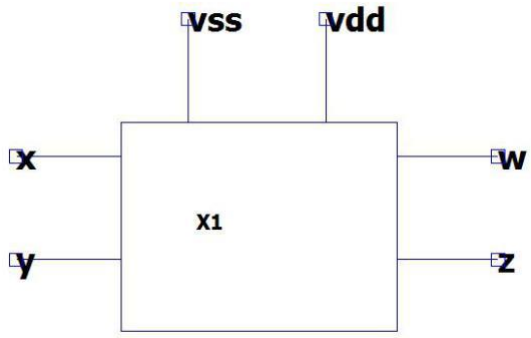

Fig. 2.8: Symbol of FTFN

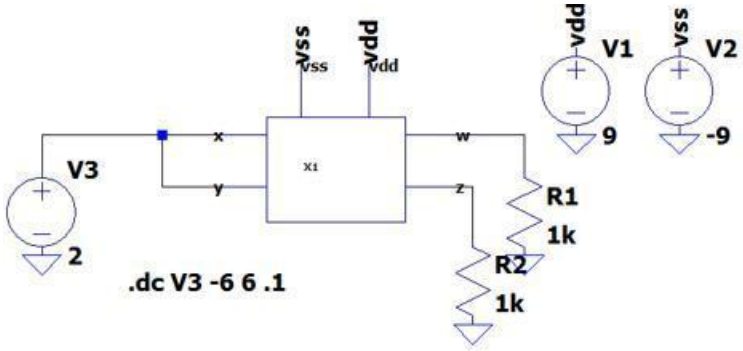

Fig. 2.9: Schematic of FTFN Realization

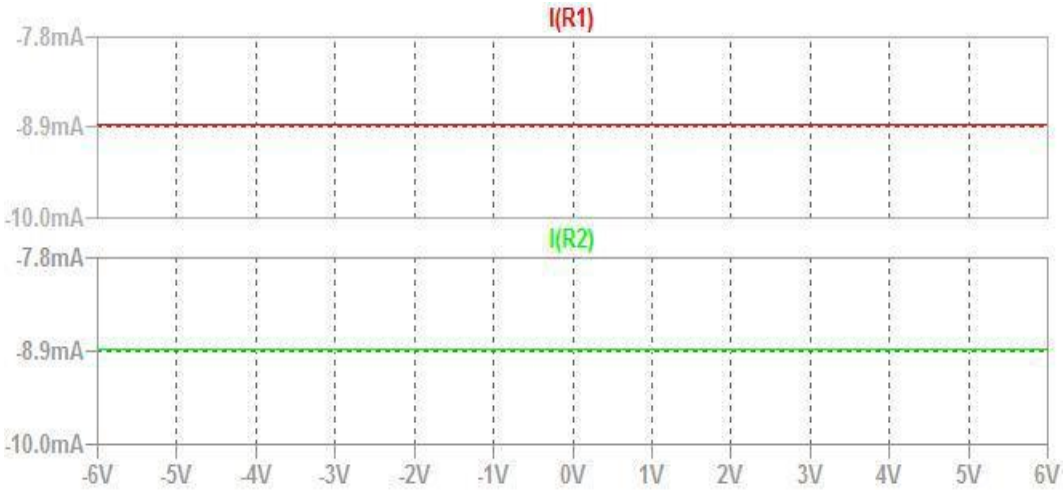

Fig. 2.10: I-V characteristics at w and z terminal for given Vx=Vy

2.2.3 VDTA [7]

We see from Fig: 2.11 that VDTA has five terminals which makes it a versatile active building block. The voltage drop at Z in VDTA is transformed into current at terminals X+ and X- (negative of X+) using gm2 and the differential input voltage (VP-VN) is transformed into a current at the Z terminal by gm1. External bias currents can govern how conductance is controlled in solid electrolytes. Since resistance is high for terminals P and N (IP and IN), currents traveling through them are almost non-existent.

Because VDTA has separate transconductances, designers can use it to achieve multiple purposes, all with the same active block or by adding another capacitor. The Mask app includes simulators for biquad filters, oscillators, inductance and FDNR which stands for frequency dependent negative resistor. This is also important because this block's input is voltage, and output is current which makes it straight-forward to use for transconductance mode applications.

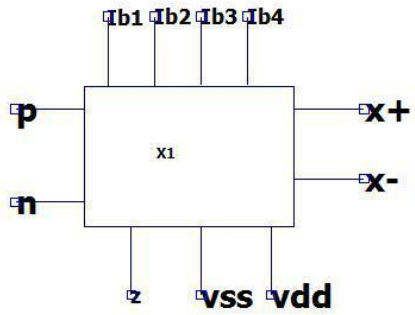

Fig. 2.11: Symbol of VDTA

In this section we have implemented VDTA using CMOS. The realization of VDTA using CMOS is shown in Fig: 2.12.

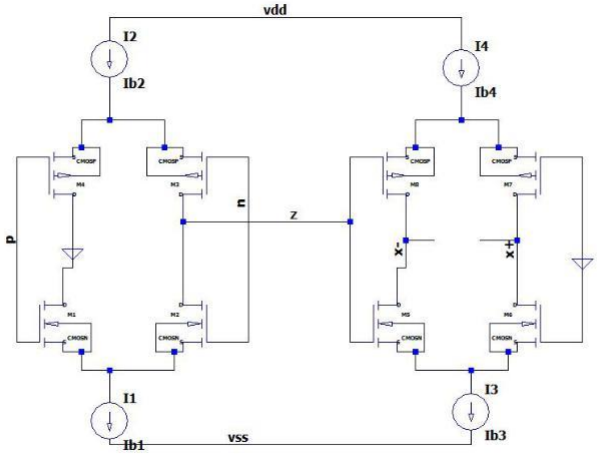

Fig. 2.12: Realization of VDTA using CMOS

A pair of transconductance circuits are added to the CMOS design to increase the efficiency of the VDTA. The transconductances gm1 and gm2 in Figure 5 are controlled by the bias currents IB1 and IB2 and IB3 and IB4 respectively. A VDTA's port characteristics can be described with these two equations [7]:

$$I_z = g_{m1}(V_P - V_N) \quad (2.5)$$
$$I_{x^+} = g_{m2}(V_P - V_N) \quad (2.6)$$
$$I_{x^-} = -g_{m2}(V_P - V_N) \quad (2.7)$$

where gm1 and gm2 are the transconductance set by bias currents in transconductance circuits from (IB1 & IB2) and (IB3 & IB4) respectively.

Table: 3.1 Aspect ratios of the transistors used for realization of VDTA [7]

MOS No.	W/L Ratio	MOS No.	W/L Ratio
M1	3.6 µm / 0.36 µm	M5	3.6 µm / 0.36 µm
M2	3.6 µm / 0.36 µm	M6	3.6 µm / 0.36 µm
M3	16.64 µm / 0.36 µm	M7	16.64 µm / 0.36 µm
M4	16.64 µm / 0.36 µm	M8	16.64 µm / 0.36 µm

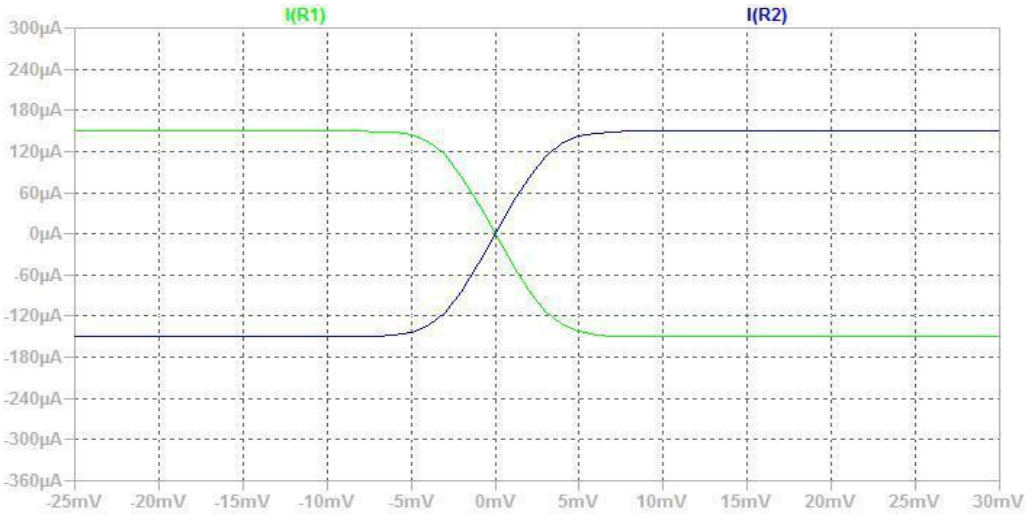

Fig. 2.13: I-V characteristics at X+ and X- terminals

2.3 Conclusion

In this chapter, we looked at the properties, port equations and construction of different kinds of active building blocks. We will build a chaotic oscillator with these active building blocks and later use it for safe communication.

CHAPTER 3

REALIZATION OF CHUA's CIRCUIT USING AD712 OPAMP

3.1 Introduction

By incorporating a third nonlinear feedback effect, Chua's circuit demonstrates chaotic behavior, noticeable as double-scroll attractors, bifurcations and other complex actions. The Chua's circuit consists of a linear resistor, a nonlinear resistor (Chua's diode), two capacitors and an inductor. Usually, chaos in circuits is achieved by setting operational amplifiers (op-amps) along with diodes or other nonlinear resistors.

Because of its fast speed, exact operation, low bias input and excellent noise control, the AD712 is perfect for such applications. It suits creating Chua's circuit and other active parts since these two features keep things stable and faithful as chaotic signals are produced. Traditionally, the circuits built by Chua using op-amps have required firm designs to control noise and component differences and the AD712 should handle these well.

3.2 Chua's Circuit Design using AD712 Opamp [4]

The most important aspect of Chua's circuit uses an op-amp instead of Chua's diode which is a nonlinear resistor. The nonlinear resistor can be constructed with the AD712 dual op-amp following Fig. 3.1.

The PWL (Piece Wise Linear) voltage-current characteristic found in the AD712 is provided by the two op-amps used. To have the required negative resistant regions, both the op-amps and resistors are biased in the circuit. With this design, integration and prototype building are fewer challenges.

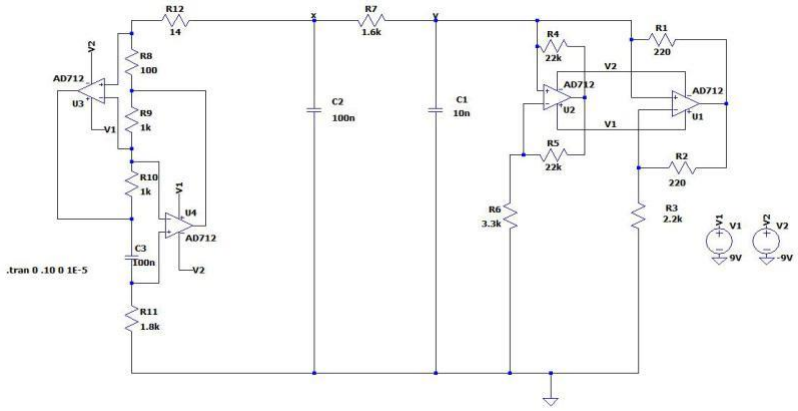

Fig. 3.1: Simulated schematic of Chua's circuit using AD712 Opamp in Ltspice

3.3 Simulation Results

The following figures shows the circuit variables V(x), V(y) and a double-scroll attractor simulated using Ltspice for Chua's circuit using AD712 Opamp. Simulated attractors from Ltspice with component values R7 = 1.6KΩ, C1= 10 nF, C_2 = 100 nF etc.

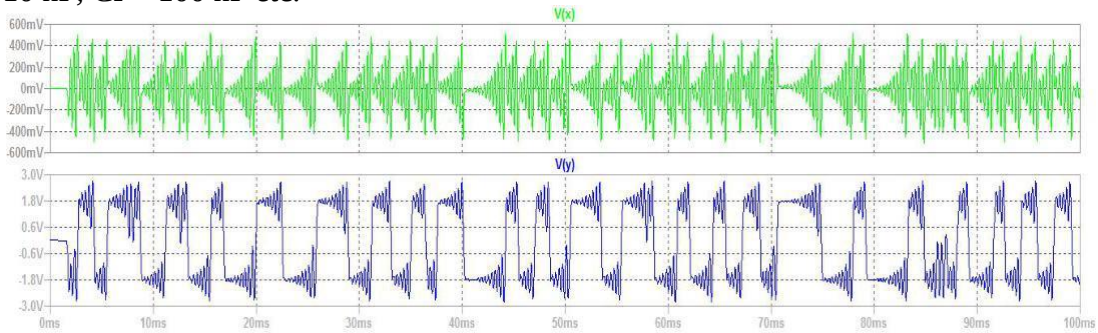

Fig. 3.2: Spectrum of chaotic circuit dynamics of V(x) and V(y)

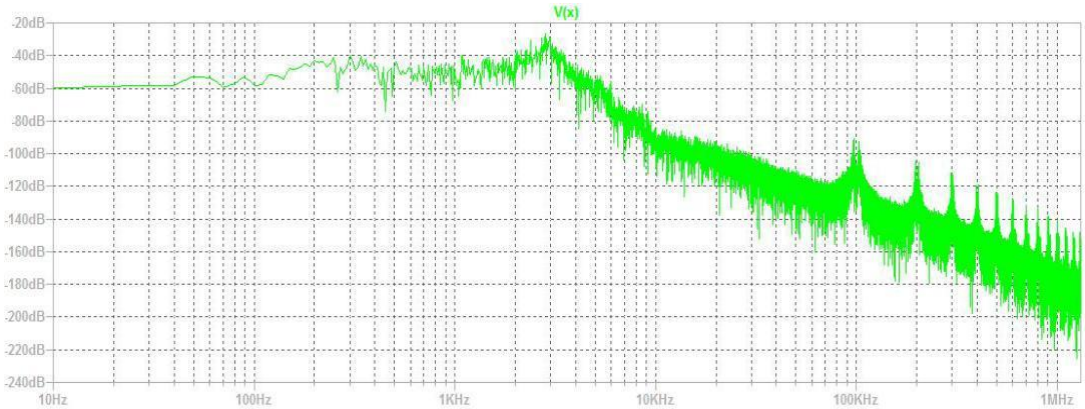

Fig. 3.3: The chaotic spectrum for simulated time waveform V(x) from AD712 Opamp based chua's circuit

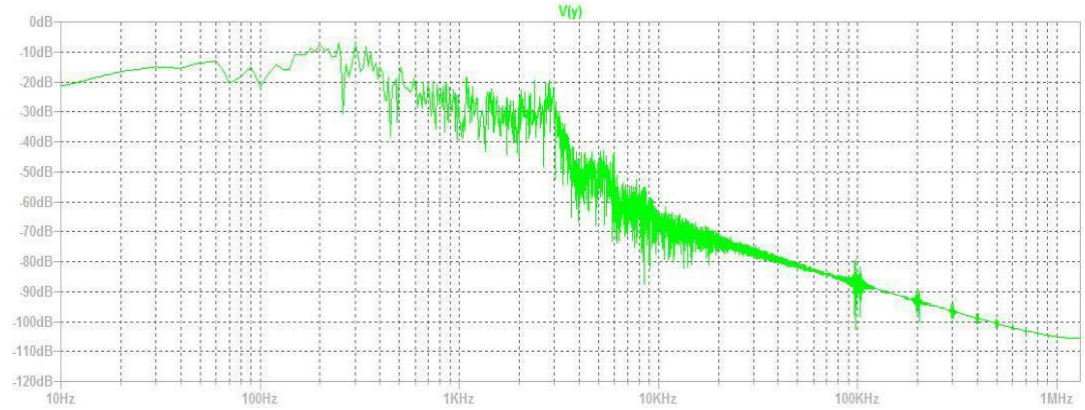

Fig. 3.4: The chaotic spectrum for simulated time waveform V(y) from AD712 Opamp based Chua's circuit

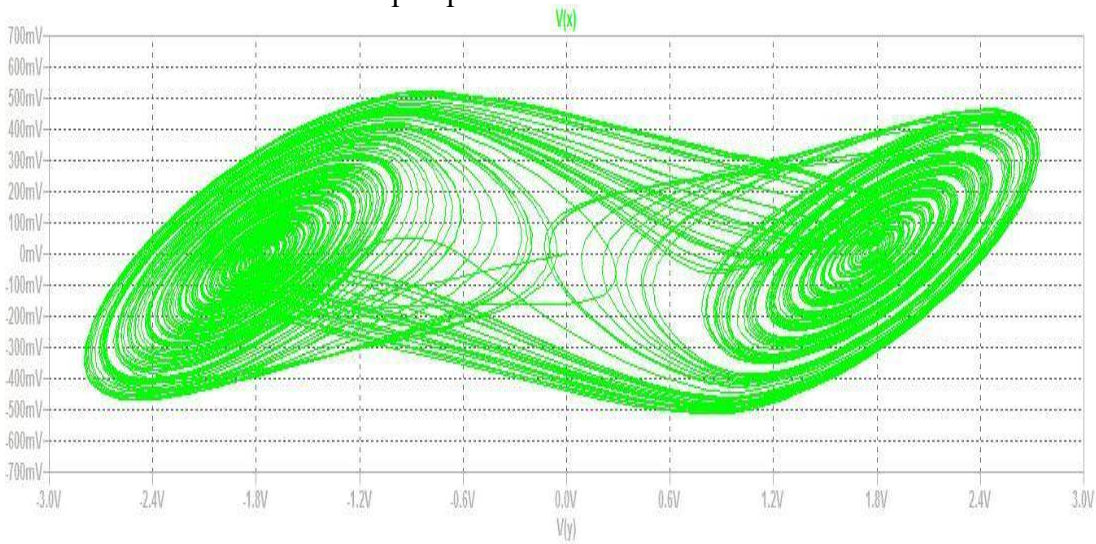

Fig. 3.5: Simulated Double Scroll for Chua's circuit using AD712 Opamp

3.4 Conclusion

In this chapter, the AD712 Opamp is employed to model the chaotic characteristics of the chua's circuit. Chapters ahead will show how this type is used in secure communication. During simulation, the voltage waveforms V(x) and V(y) show a range of 300 KHz to 1 MHz and 1 KHz to 100 KHz, as shown in above Figures. Integrated circuits that must be compact and fit within a narrow frequency range from 300KHz to 1MHz are best served by this type of circuit. The AD712 is a convenient choice for Chua's circuit owing to its accurate design and two op-amps. Engineers and researchers can clearly represent chaotic behavior with off-the-shelf units thanks to their high speed and little electronic noise.

CHAPTER 4

REALIZATION OF CHUA's CIRCUIT USING FTFN

4.1 Introduction

Originally proposed in 1983, Chua's circuit is special because it is a chaotic system with detailed nonlinear movements and a dead-simple circuit that produces the double scroll attractor. Most known approaches involve adding nonlinear Chua diodes and passive devices such as resistors, capacitors and inducers, yet they often need to use op-amps or CCIIs in their complex setups. Still, these types of circuits have several disadvantages, for example limited frequency range, using many parts and being susceptible to parasitic effects.

In analog circuit design, the Four-Terminal Floating Nullor (FTFN) [5] has become a superior active element. FTFN is perfect for current-mode chaotic systems because of its inherent stability, broad dynamic range, and versatility in both voltage and current modes.

4.2 Chua's Circuit Design using FTFN [6]

The FTFN realization of Chua's circuit is made up of two FTFN cascaded together. To make FTFN, two AD844 ICs are used. We used the FTFN in Fig: 4.1 to realize Chua's circuit. The supply voltages are assumed to be within ± 9 V. The values of the resistor (R), inductor (L), and capacitors (C1 and C2) are assumed to be 10nF, 100nF, 18 mH, and 1.8Kohm, respectively.

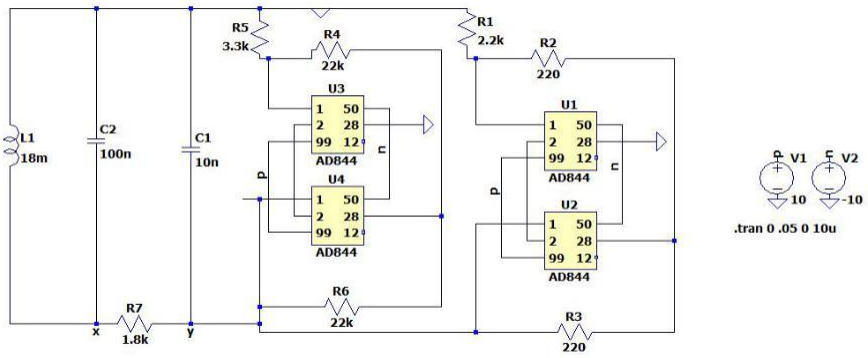

Fig. 4.1: Simulated schematic of Chua's circuit using FTFN in Ltspice

4.3 Simulation Results

The FTFN-based Chua's circuit for the Ltspice simulations shows double-scroll chaotic behavior with C1 = 10 nF, C2 = 100 nF, and R7 = 1.8 KΩ. FTFNs based on AD844 were used to run the Ltspice simulations.

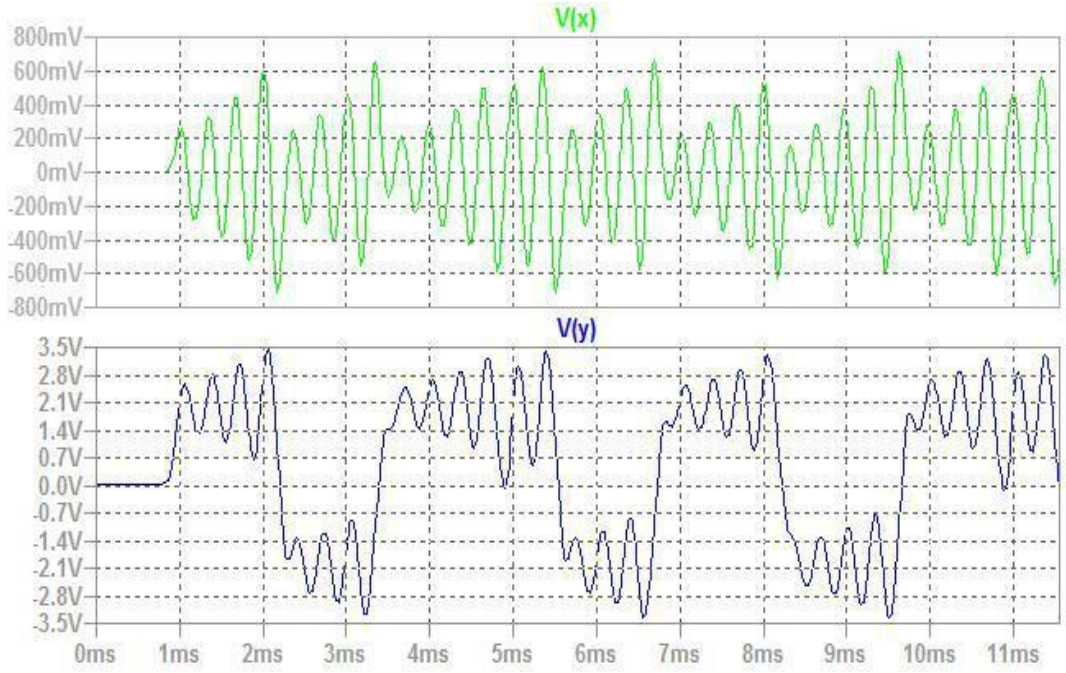

Fig. 4.2: Spectrum of chaotic circuit dynamics of V(x) and V(y)

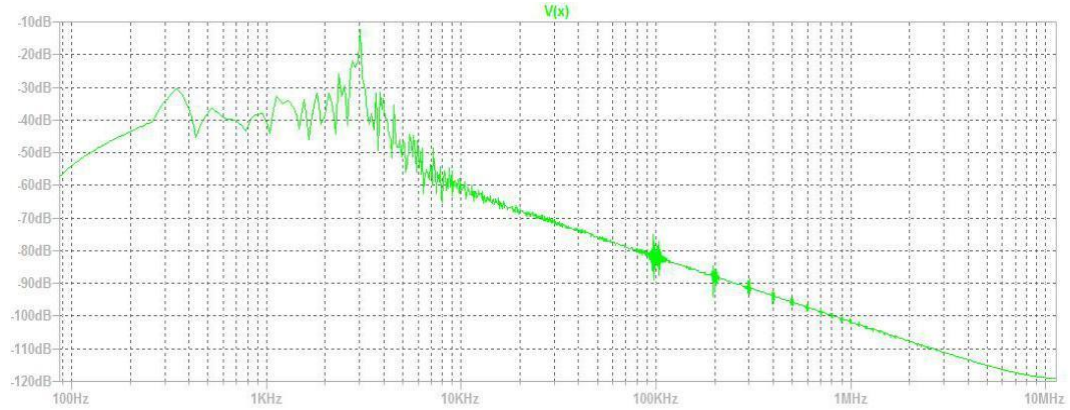

Fig. 4.3: The chaotic spectrum for simulated time waveform V(x) from FTFN based Chua's circuit

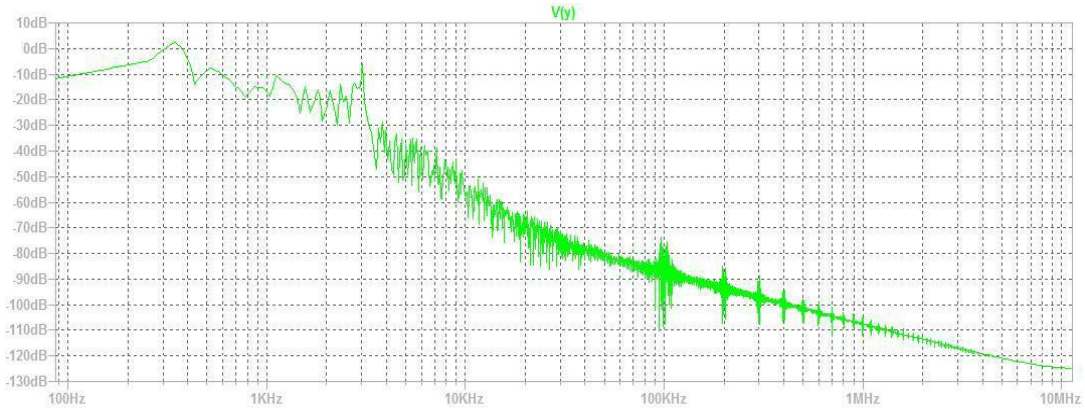

Fig. 4.4: The chaotic spectrum for simulated time waveform V(y) from FTFN based Chua's circuit

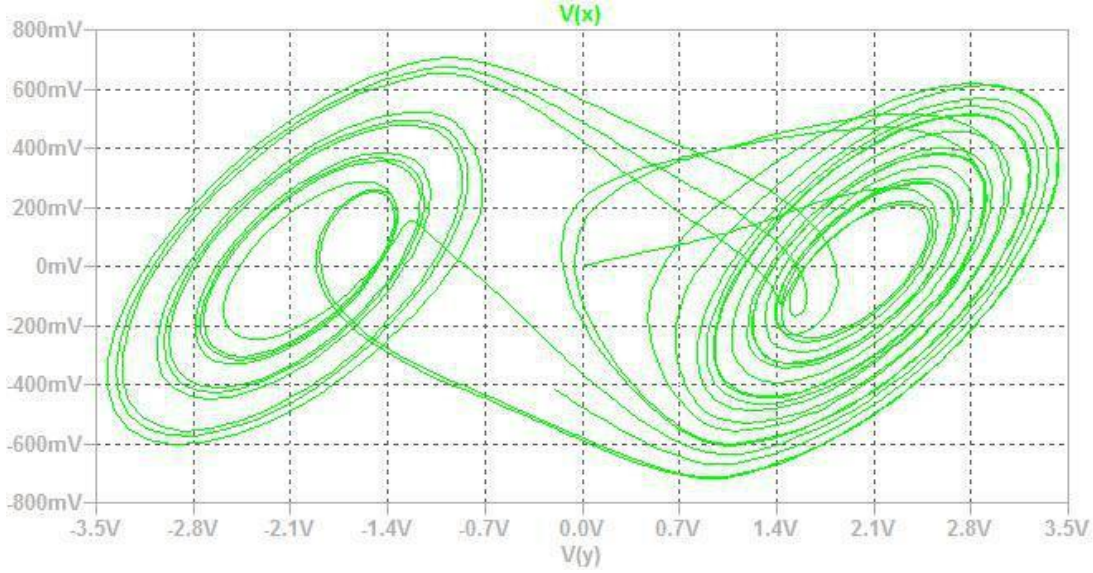

Fig. 4.5: Simulated Double Scroll for Chua's circuit using FTFN

4.4 Conclusion

The FTFN-based Chua's circuit displays its first chaotic behavior, according to the simulation results. Chua's diode gives the designer new options for implementing chaotic communication systems in integrated circuits.

This chapter uses FTFN to imitate the chaotic nature of the chua's circuit, which will be employed in future chapters for secure communication. The chaotic spectrum range for V(x) and V(y) during simulation is 4 KHz to 100 KHz and 4 KHz to 100 KHz, respectively, as shown in Fig. Because it will take up less space in practice, this circuit is best suited for integrated circuit applications with frequencies between 4 KHz and 100 KHz.

CHAPTER 5

REALIZATION OF CHUA's CIRCUIT USING VDTA

5.1 Introduction

The performance of a chaotic system is heavily dependent on how it was initially setup. Weather behaves in a way that is typical for a chaotic system. Three special features of a chaotic system include non-linearity, high sensitivity to the starting conditions and that the path is never repeated. Much research has shown that all three criteria are accomplished by the Chua's chaotic oscillator. You can see the main classical Chua's oscillator, shown in Figure. Examples of applications for chaotic systems are image sensing, music, washing machines, cellular neural networks, information security in communication, random number generation and checking heart beats.

For chaotic circuit design, the Voltage Differencing Transconductance Amplifier (VDTA) is now widely regarded as a top active element. These devices have several benefits such as saving power, providing large bandwidth (up to MHz) and having high slew rates, as well as being adjustable by biasing currents. Limitations cause Chua's diodes to excel at replacing common op amps and imitating inductors to cut down on passive parts. These VDTA [8] circuits have lately demonstrated better frequency reach and less sensitivity to the variations in their materials, making their chaotic output suitable for application in encryption and safe communication tasks.

5.2 Chua's Circuit Design using VDTA [7]

The Chua's chaotic oscillator that was developed with VDTA is displayed in Fig: 5.1. One VDTA and three storage elements C1, C2, and L are used to make it happen. It sustains the high frequency spectrum surrounding the chaotic oscillator's high dominant frequency. This design's VDTA's CMOS architecture allows for chaotic oscillations with a prominent frequency in the tens of megahertz

range. The next section talks about simulating the oscillator to get different chaotic responses.

The supply voltage is assumed to be ±0.9 V. The bias currents (IB1, IB2, IB3, and IB4) of VDTA are assumed to be IB1 = IB2 = 100 mA and IB3 = IB4 = 35 mA for the Chua's chaotic oscillator circuit implementation, as seen in Fig: 5.1. The values of the resistor (R), inductor (L), and capacitors (C1 and C2) are assumed to be 1645 ohm, 10 pF, 100 pF, and 18 uH, respectively.

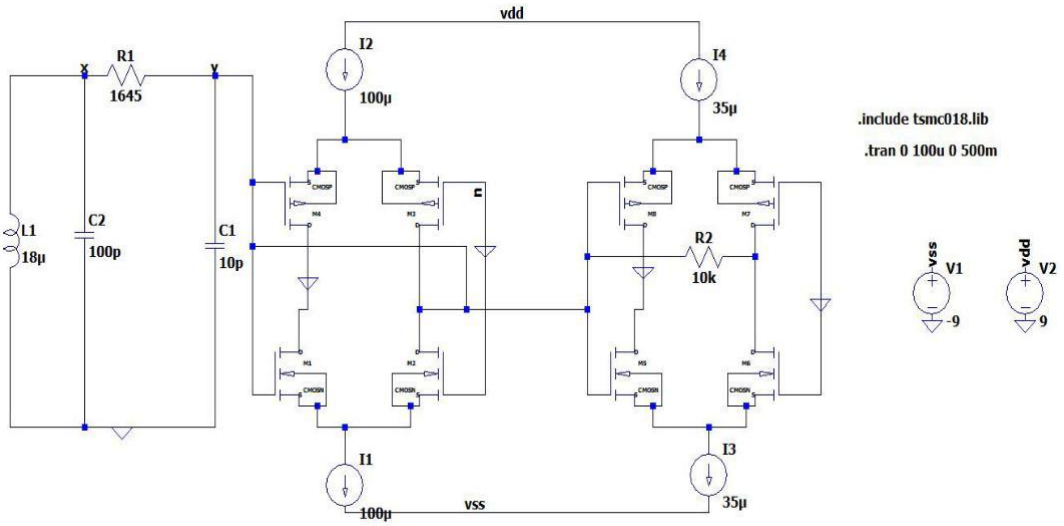

Fig. 5.1: Simulated schematic of Chua's circuit using FTFN in Ltspice

5.3 Simulation Results

We use the Ltspice application with TSMC CMOS 0.18 µm process characteristics to run the simulations. Table: 3.1 provides the transistors' aspect ratios. VDD = −VSS = 9 V is utilized for supply voltages, and biasing currents I1 = I2 = 100µA and I3 = I4 = 35µA are employed. Fig: 5.5 shows the double scroll chaotic circuit using VDTA.

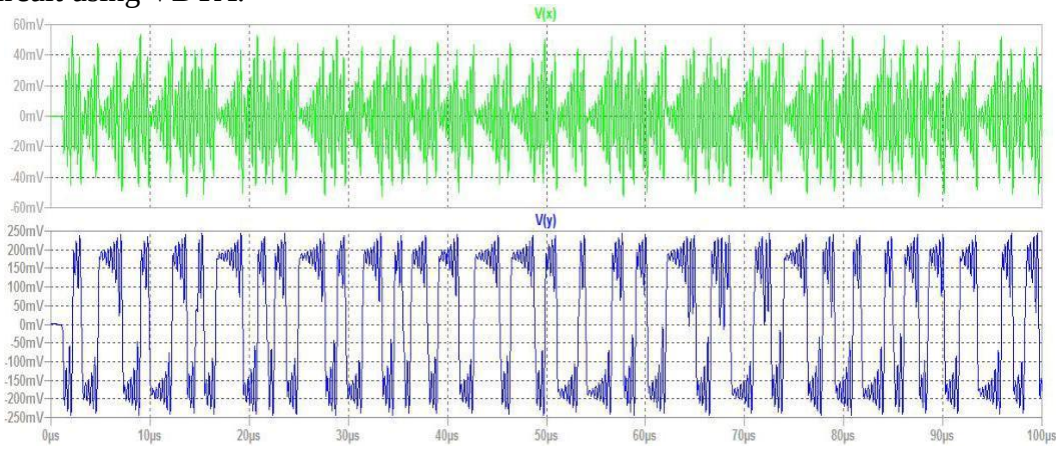

Fig. 5.2: Spectrum of chaotic circuit dynamics of V(x) and V(y)

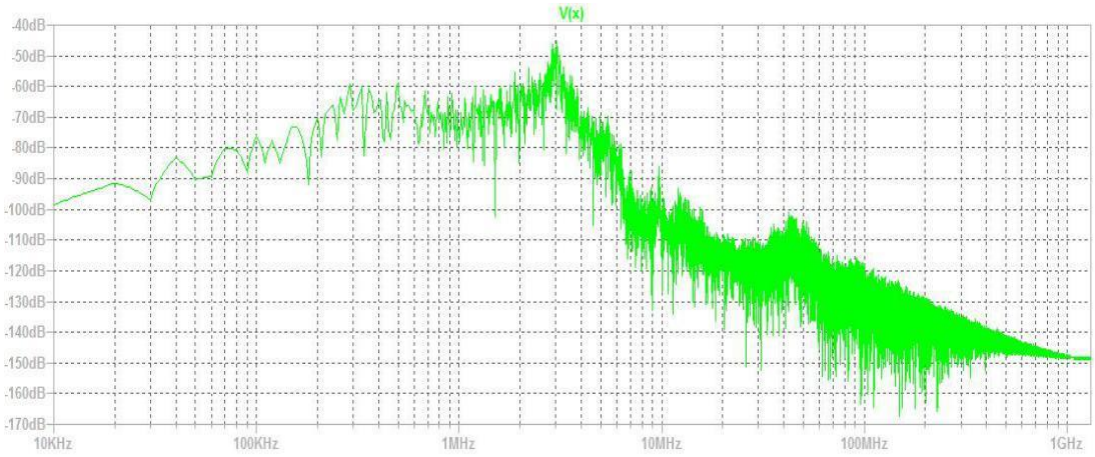

Fig. 5.3: The chaotic spectrum for simulated time waveform V(x) from VDTA based Chua's circuit

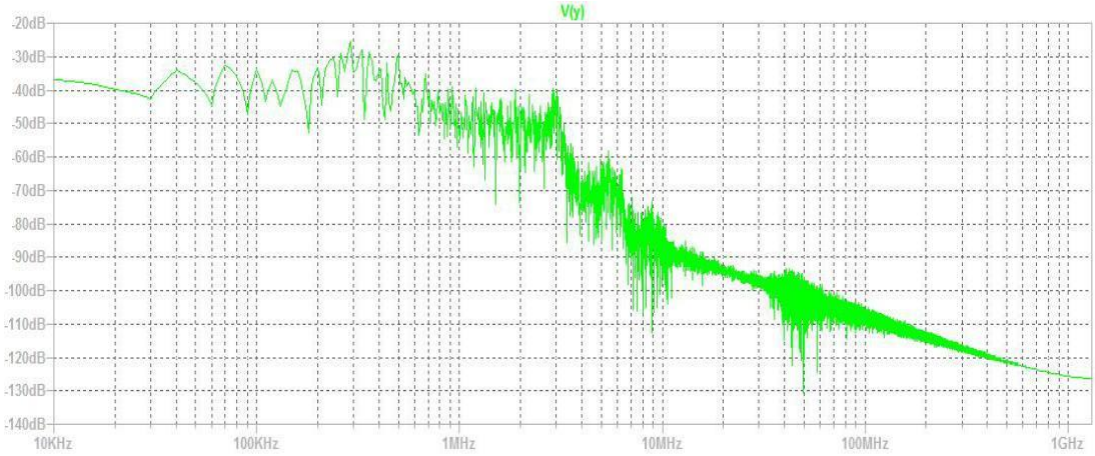

Fig. 5.4: The chaotic spectrum for simulated time waveform V(y) from VDTA based Chua's circuit

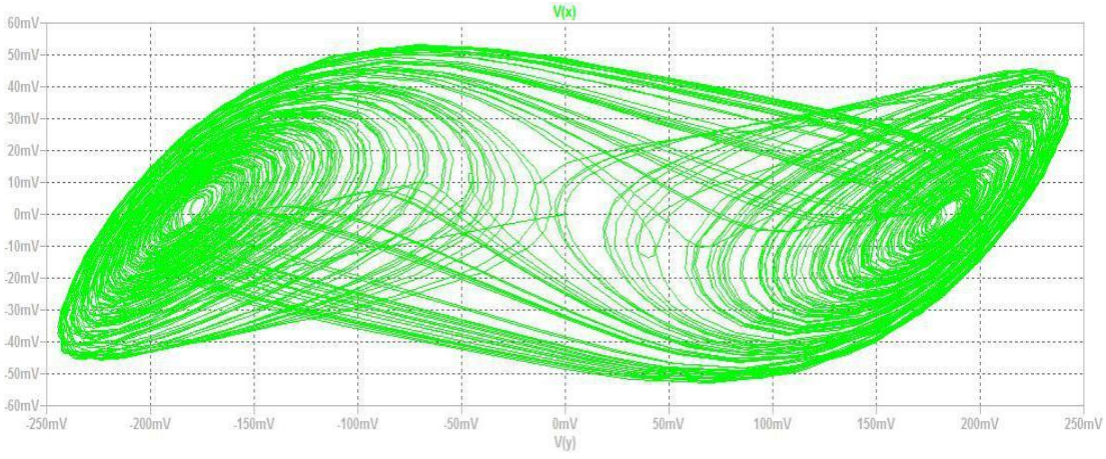

Fig. 5.5: Simulated Double Scroll for Chua's circuit using VDTA

5.4 Conclusion

This chapter discusses a novel use of Chua's chaotic oscillator that makes use of a voltage differencing transconductance amplifier block (VDTA). The basic Chua's oscillator uses fewer passive components and analog building pieces to create a small and simple Chua's diode. The circuit offers a range of chaotic reactions. Responses with high frequency are justified by the non-ideality analysis.

Chua's circuit was implemented in this chapter using VDTA, simulating its chaotic character. Future chapters will employ this circuit for secure communication. During the simulation, the chaotic spectrum ranges for V(x) and V(y) are 800 KHz to 1 GHz and 800 KHz to 500 MHz, respectively, as illustrated in Fig. Since it will take up less space in practice, this circuit is best suited for integrated circuit applications operating in the 800KHz to 1GHz frequency range.

CHAPTER 6

HYBRID REALIZATION OF CHUA'S CIRCUIT

6.1 Introduction

This section introduces two hybrid implementations of Chua's circuit, which are created by combining VDTA, FTFN, and AD712 Opamp. The ensuing subsections provide specifics on the circuit parameters and topology that result in a double-scroll attractor. The hybrid realizations' chaotic characteristics are demonstrated, and they are then applied to secure communication.

6.2 Hybrid Realization [9]

6.2.1 Hybrid -I Realization of Chua's Circuit

Using two AD712 Opamps biased with ±9 V for inductor generation, two AD844 based FTFN blocks biased with ±10 V for Chua's diode, and a few resistors and capacitors, Fig: 6.1 illustrates a Hybrid-I implementation of Chua's circuit. The circuit displays a double-scroll attractor behavior, which is used in secure communication, when C4 = 10 nF, C5 = 100 nF, and R19 = 1.8 KΩ.

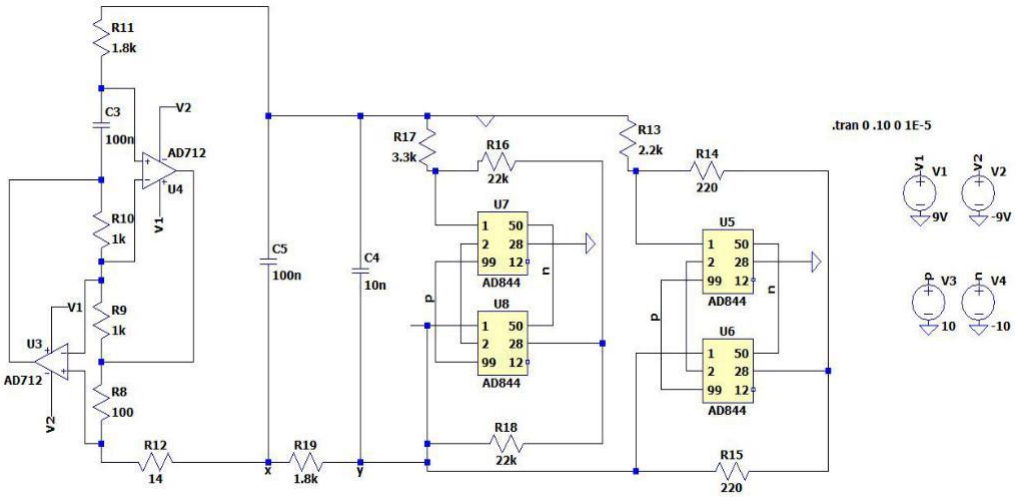

Fig. 6.1: Simulated schematic of Hybrid- I realization of Chua's circuit in Ltspice

6.2.2 Hybrid -II Realization of Chua's Circuit

Using two AD712 Opamps biased with ±9 V for inductor generation, one MOS-based VDTA block biased with ±9 V for Chua's diode, and a few resistors and capacitors, Fig: 6.2 illustrates a Hybrid-I implementation of Chua's circuit. The circuit displays a double-scroll attractor behavior, which is used in secure communication, when C1 = 10 nF, C2 = 100 nF, and R1 = 1.6 KΩ.

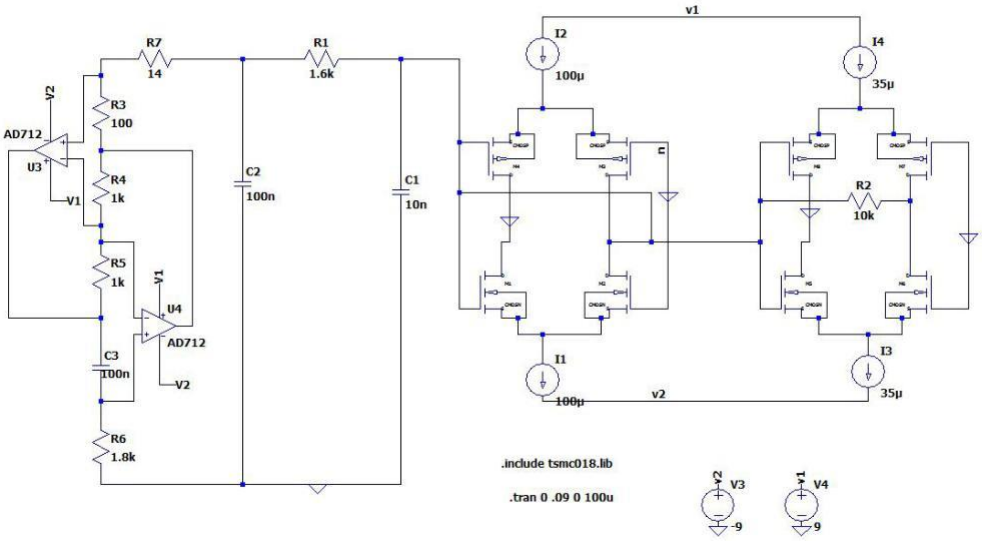

Fig. 6.2: Simulated schematic of Hybrid- II realization of Chua's circuit in Ltspice

6.3 Simulation Results

6.3.1 Simulation of Chua's Circuit using Hybrid- I

The Ltspice application was used to do simulations with TSMC CMOS 0.18 μm process parameters. This section contains a simulated Hybrid-I realization created with FTFN and an Ad712 Opamp. The range of the chaotic spectrum for V(x) and V(y) during simulation is 1 KHz to 500 KHz and 1 KHz to 200 KHz, respectively, as illustrated in Fig: 6.4 and Fig: 6.5. Since its practical implementation will take up less volume, this circuit is best suited for integrated circuit applications with frequencies between 1KHz and 500KHz. The simulation's findings show that the circuit of the Hybrid-I Chua displays its initial chaotic behavior. The designer of integrated circuits for chaotic communication systems has additional options because to Chua's diode.

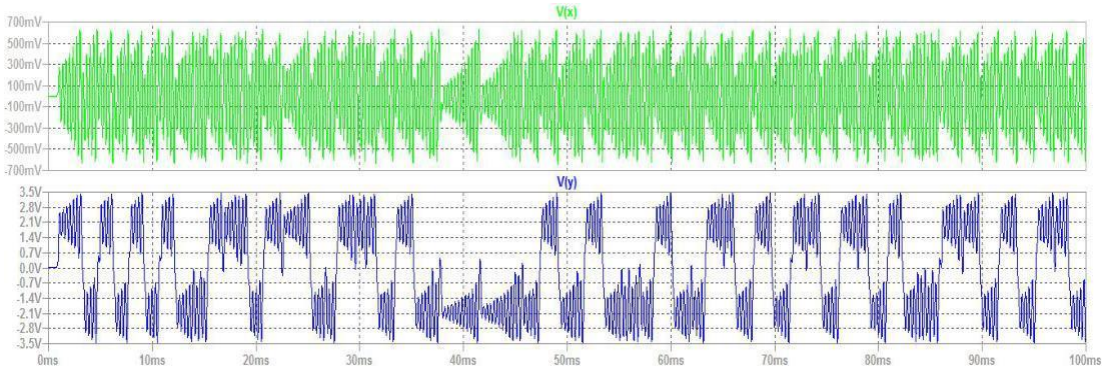

Fig. 6.3: Spectrum of chaotic circuit dynamics of V(x) and V(y)

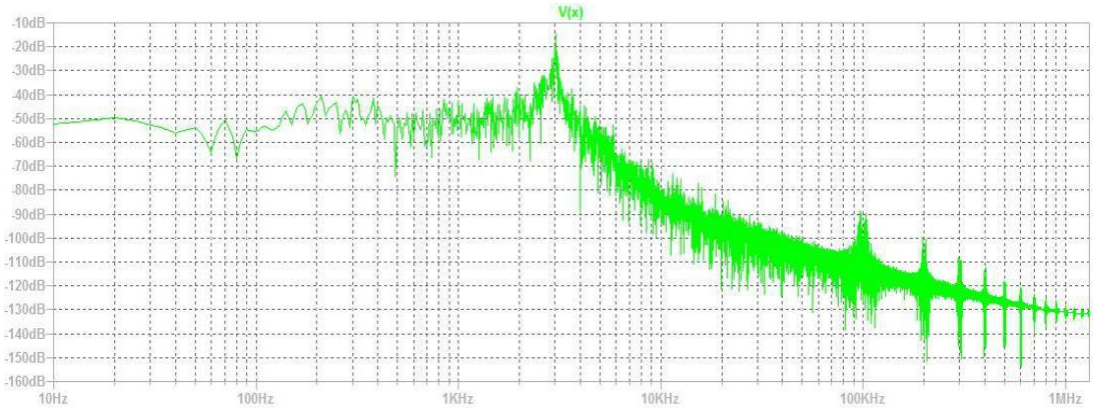

Fig. 6.4: The chaotic spectrum for simulated time waveform V(x) from Hybrid -I based Chua's circuit

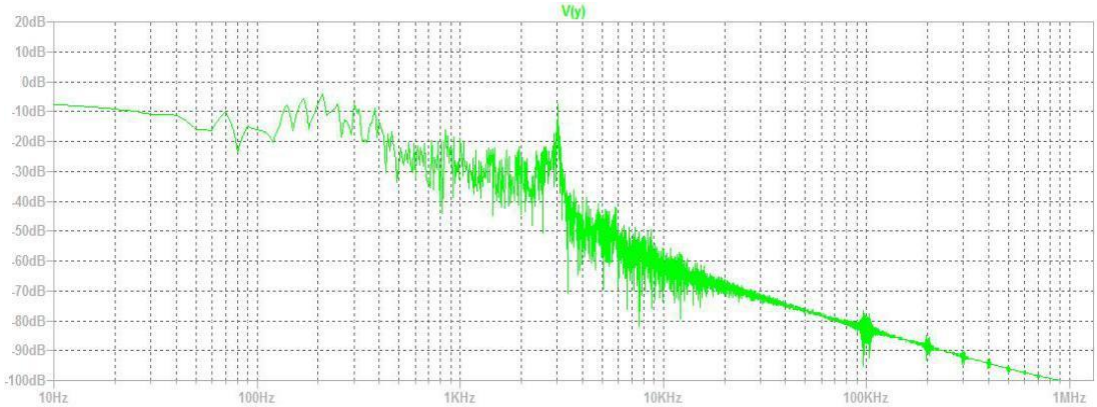

Fig. 6.5: The chaotic spectrum for simulated time waveform V(x) from Hybrid -I based Chua's circuit

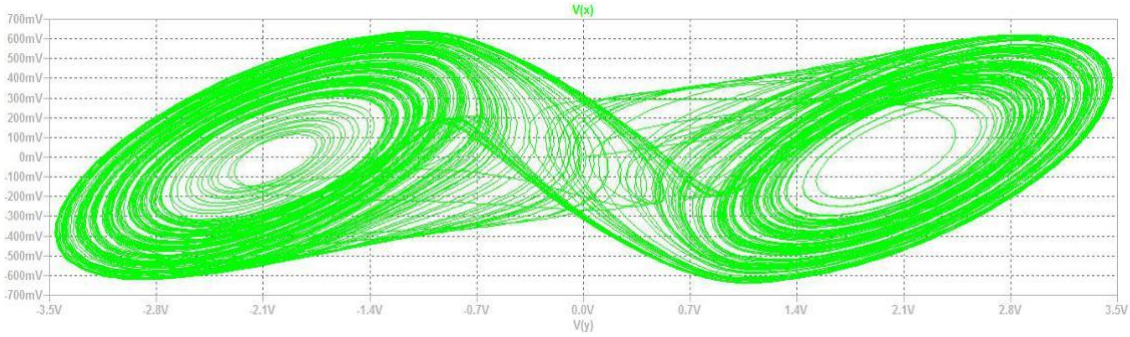

Fig. 6.6: Simulated Double Scroll for Chua's circuit using Hybrid -I

6.3.2 Simulation of Chua's Circuit using Hybrid- II

Simulations utilizing TSMC CMOS 0.18 μm process parameters were conducted using the Ltspice application. The Ad712 Opamp and VDTA were used to create the simulated Hybrid-II realization in this part. The chaotic spectrum range for V(x) and V(y) during simulation is between 1KHz and 800KHz, as illustrated in Fig: 6.8 and Fig: 6.9. Because it will take up less space in practice, this circuit is best suited for integrated circuit applications with frequencies between 1KHz and 800KHz. According to the simulation results, the circuit of the Hybrid-I Chua displays its initial chaotic behavior. Chua's diode gives the designer new options for implementing chaotic communication systems in integrated circuits.

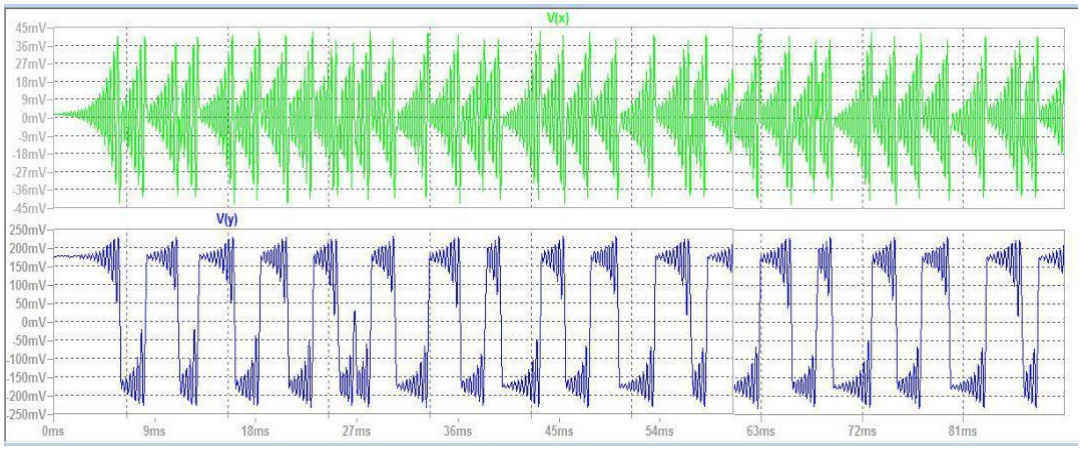

Fig. 6.7: Spectrum of chaotic circuit dynamics of V(x) and V(y)

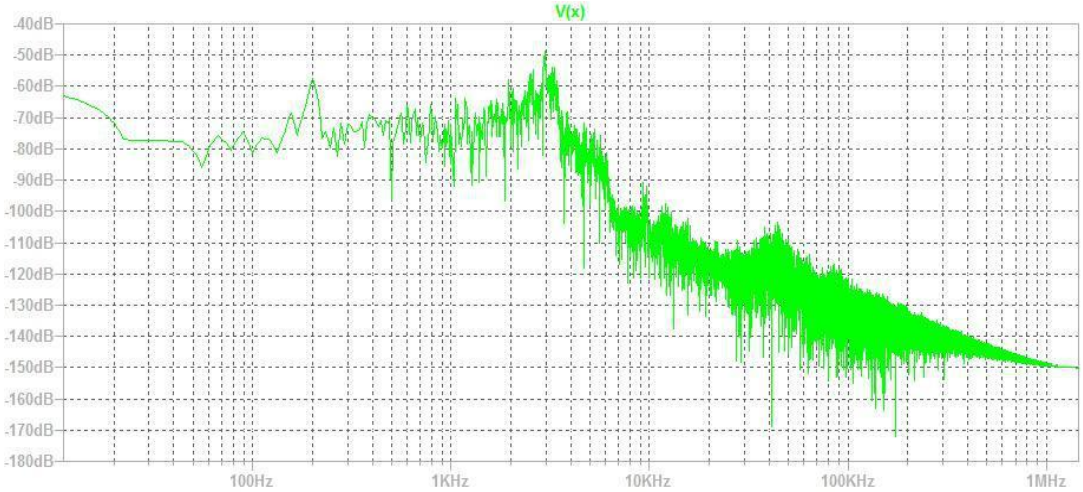

Fig. 6.8: Chaotic spectrum for simulated time waveform V(y) from Hybrid -II based Chua's circuit

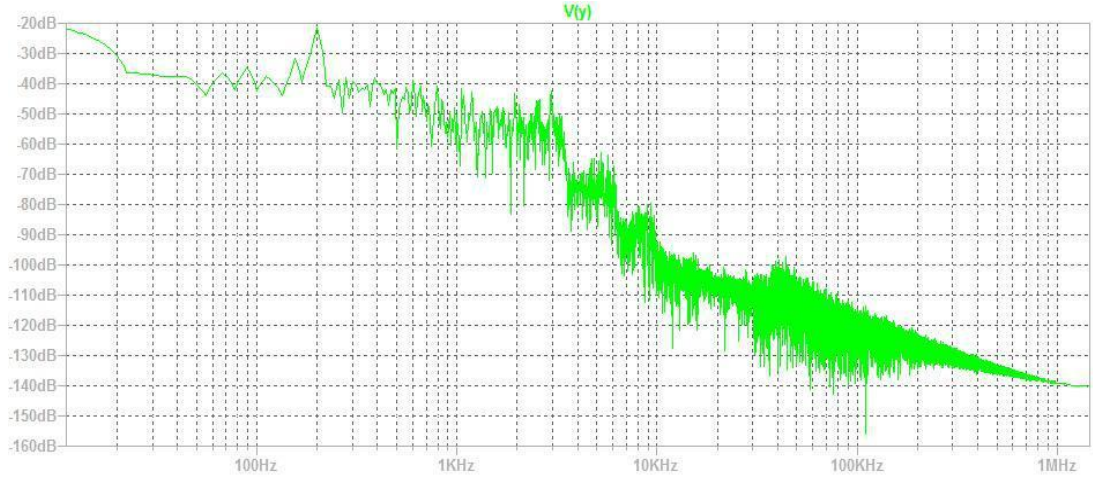

Fig. 6.9: Chaotic spectrum for simulated time waveform V(y) from Hybrid -II based Chua's

circuit

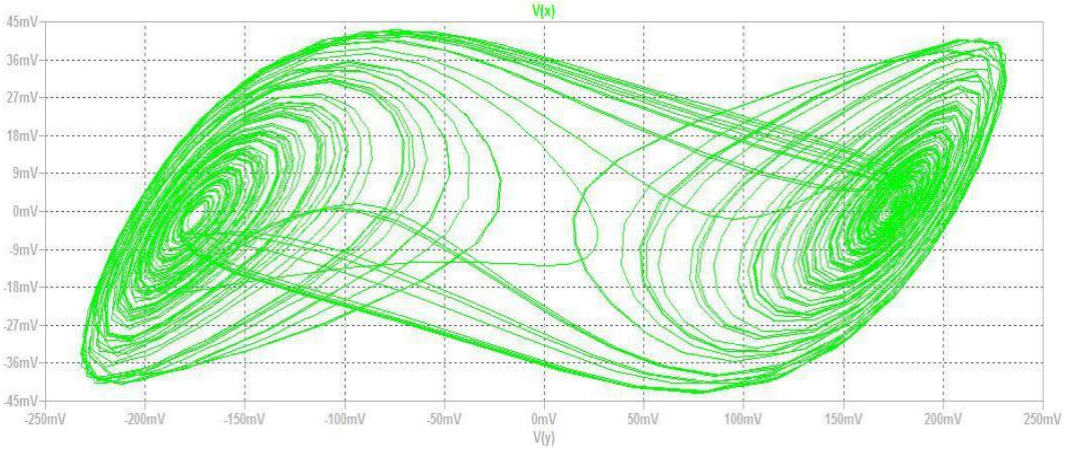

Fig. 6.10: Simulated Double Scroll for Chua's circuit using Hybrid -II

6.4 Conclusion

In this chapter, we used various active building pieces to simulate the Hybrid-I and Hybrid-II realizations of Chua's circuit. Chua's circuit based on Hybrid-I and Hybrid- II show its initial chaotic behavior, according to the simulation results. For the integrated circuit realization of chaotic communication systems, this gives the designer new options. This insight will be applied to secure communication in the upcoming chapter.

CHAPTER 7

APPLICATION OF CHUA'S CIRCUIT

7.1 Introduction

Chua's Circuit, known for being the simplest electronic circuit capable of generating chaotic behavior, has found numerous applications in scientific, engineering, and communication domains. The inherent nonlinearity and sensitivity to initial conditions make it an ideal system to model, analyze, and apply in areas that exploit or require unpredictability, secure transmission, and complex dynamics.

7.2 Application in Secure Communication [10]

Secure communication is one of the key areas where chaos is used. Fig: 7.1 displays the communication system's block diagram. Synchronization was one of the issues encountered during the communication system's deployment. The chaotic systems at the transmitter and the receiver are being precisely matched.

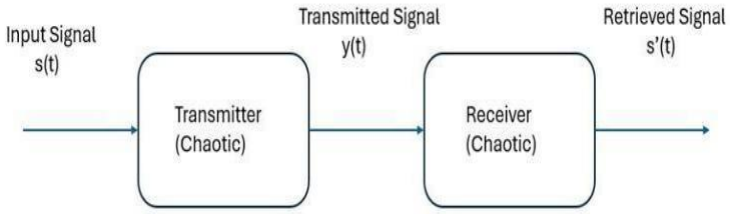

Fig. 7.1: Block Diagram of Communication System

7.2.1 Transmitter [10]

The transmitter's internal block diagram is displayed in Fig: 7.2. The transmitter creates the resultant signal R(t) by masking the information signal s(t) with the chaotic signal Vc1(t) produced by the chua's circuit using a summer. The inverter is used to transmit the resulting signal without any phase shift after the

buffer has been utilized to obtain the signal without attenuation. A chaotic masking technique is used to superimpose the input signal (message) on top of the chaotic signal. The carrier in this case is the chaotic oscillator. Over the channel, the combined signal is sent.

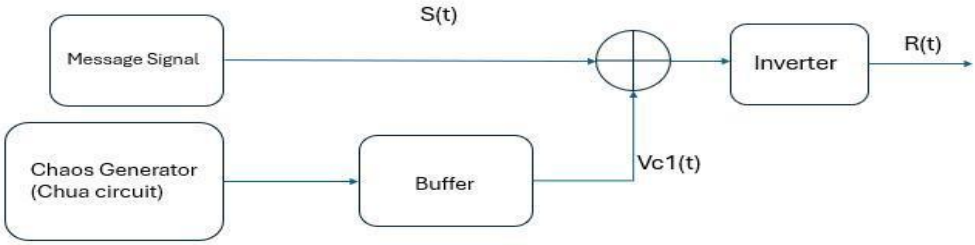

Fig. 7.2: Internal Block Diagram of Transmitter

7.2.2 Receiver [10]

The receiver's internal block diagram is displayed in Fig: 7.3. A chua's circuit like the one at the transmitter is used in the receiver to produce a chaotic signal Vc1(t) that precisely matches the chaotic signal produced at the transmitter. A subtractor is used to process the transmitter's signal R(t) and the chaotic signal Vc1(t) produced by the receiver's chaotic system (Chua's circuit). The result is S'(t) = R(t) - Vc1(t), which is the same as the message signal. When coupling, the buffer ensures that the signal is not attenuated. Using the same circuit characteristics, a synchronous version of the chaotic oscillator is created. The received composite signal is subtracted from the recreated chaos to recover the message signal.

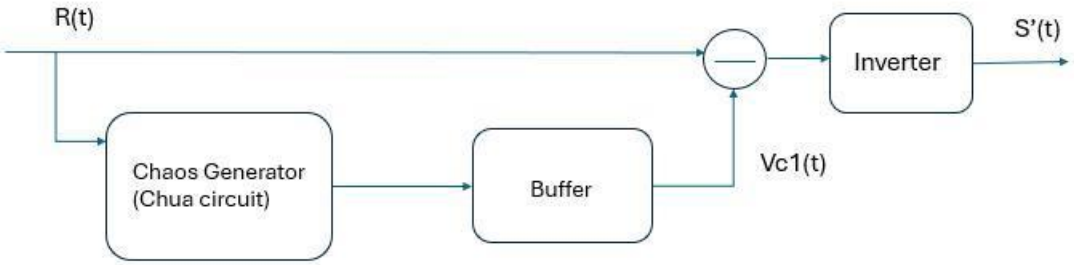

Fig. 7.3: Internal Block Diagram of Receiver

7.3 Circuit Implementation for Secure Communication System using different Active Building Blocks [10]

The use of nonlinear chaotic signals for data encryption and transmission, known as chaos-based communication, has gained popularity due to the rising need for safe and energy-efficient communication systems. Chaotic systems, in contrast to

conventional encryption methods, are naturally suited for secure analog transmission because of their large frequency range, great sensitivity to beginning conditions, and pseudo-random behavior. This section covers the actual circuit implementation of these systems employing a variety of active building pieces, including hybrid combinations, FTFN, VDTA, and Opamp.

7.3.1 Realization using AD712 Opamp

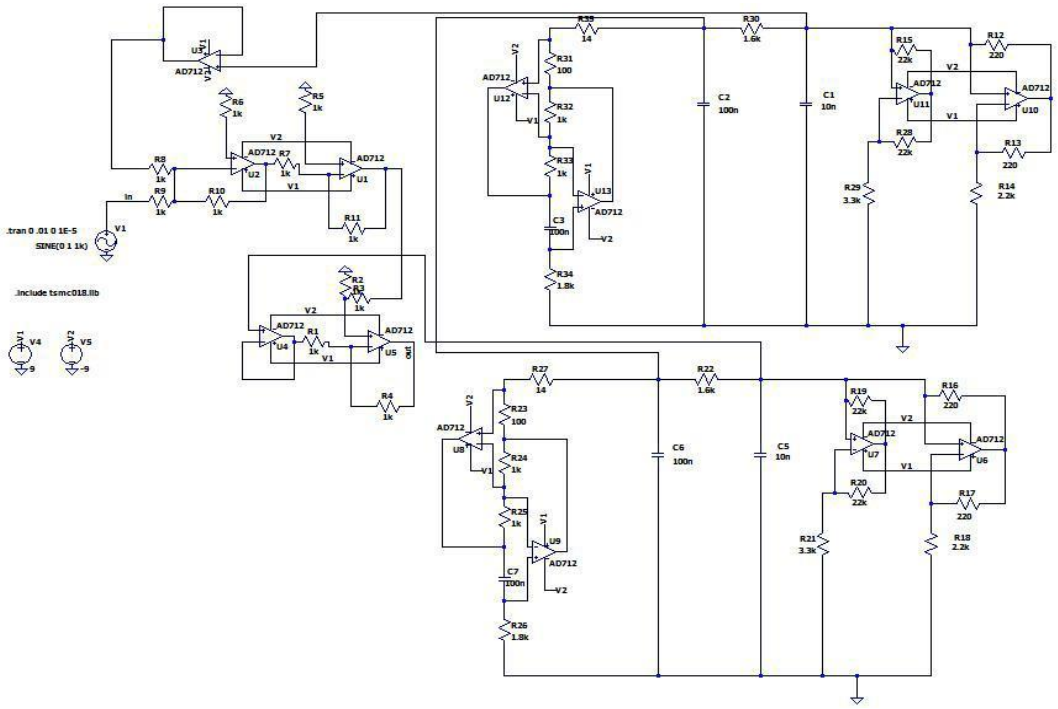

Fig. 7.4: Circuit Implementation for Secure Communication System using AD712 Opamp

7.3.2 Realization using FTFN

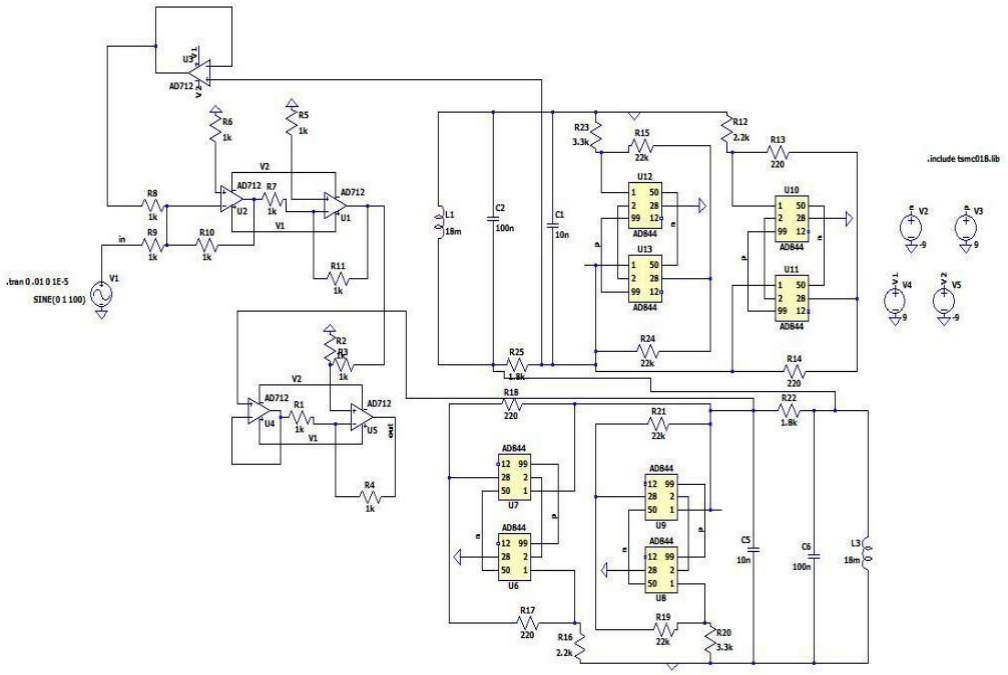

Fig. 7.5: Circuit Implementation for Secure Communication System using FTFN

7.3.3 Realization using VDTA

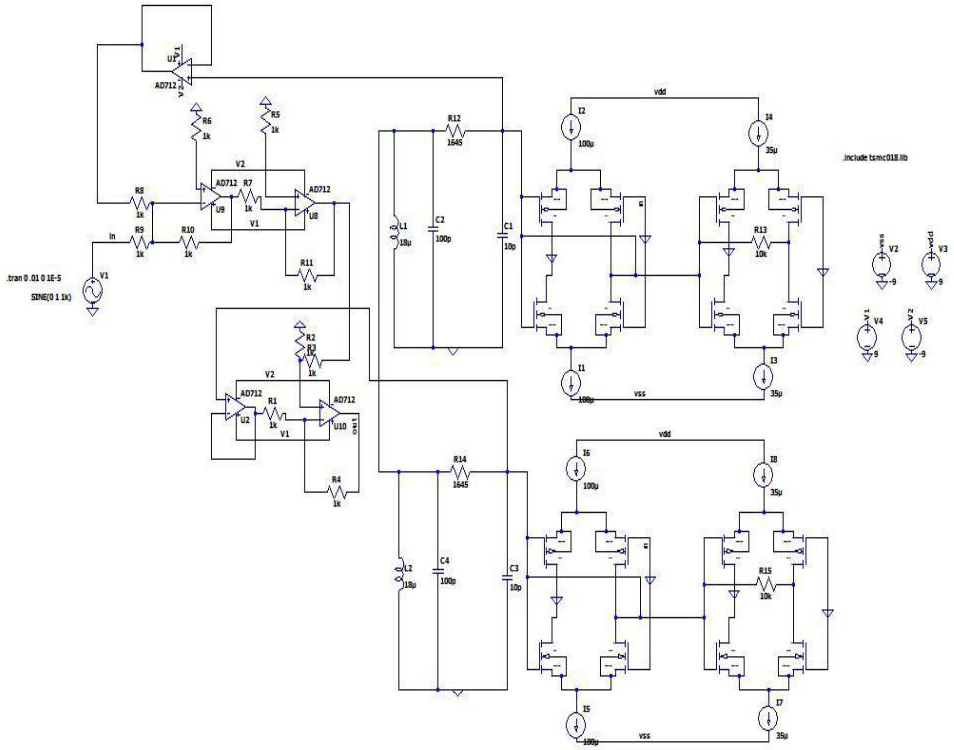

Fig. 7.6: Circuit Implementation for Secure Communication System using VDTA

7.3.4 Realization using Hybrid -I

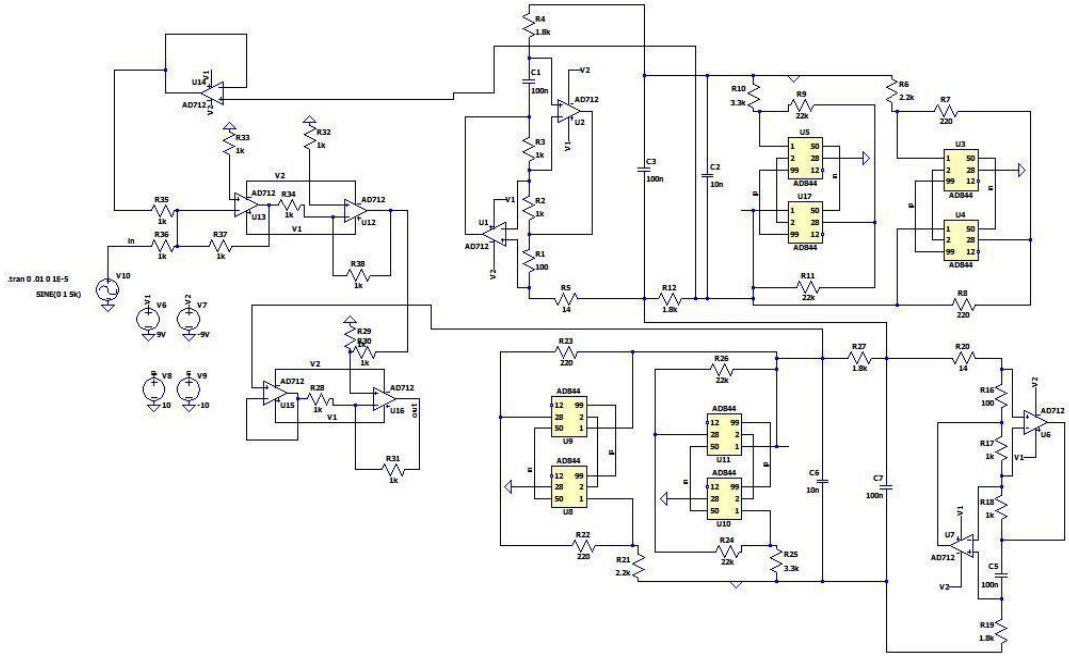

Fig. 7.7: Circuit Implementation for Secure Communication System using Hybrid -I

7.3.5 Realization using Hybrid -II

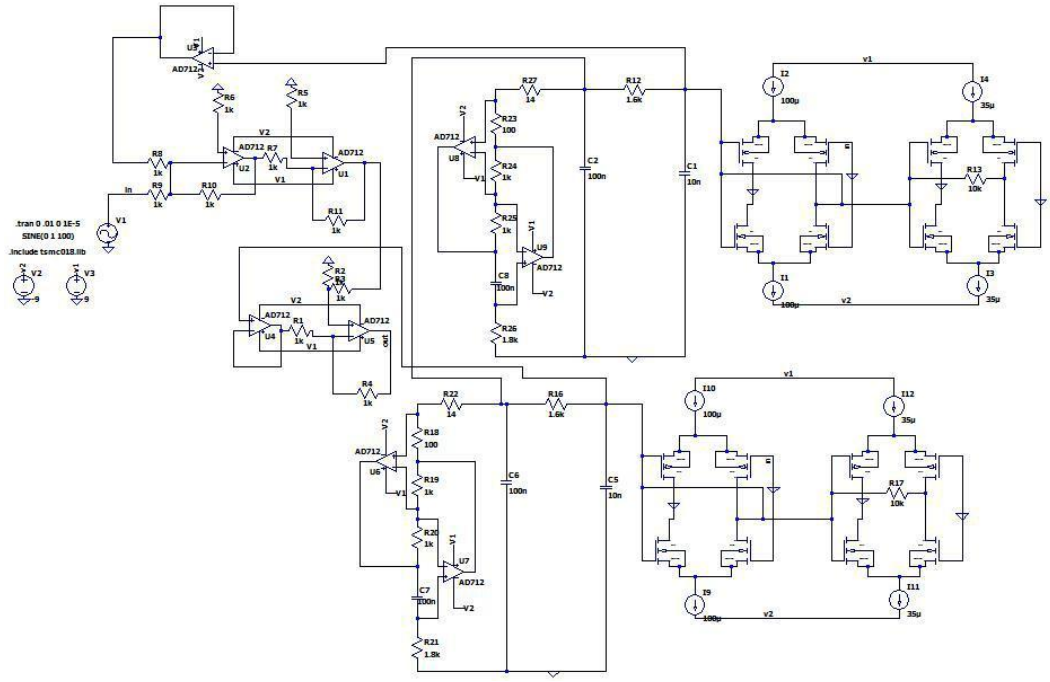

Fig. 7.8: Circuit Implementation for Secure Communication System using Hybrid -II

7.4 Simulation Results

7.4.1 Simulation results of AD712 Opamp

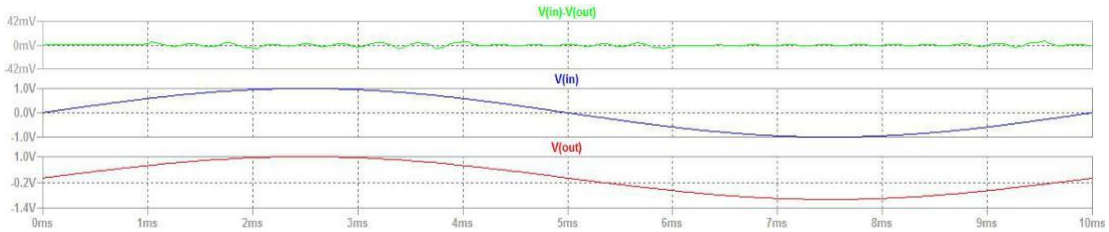

Fig. 7.9: Plot for Vin, Vout, and its difference at 100Hz

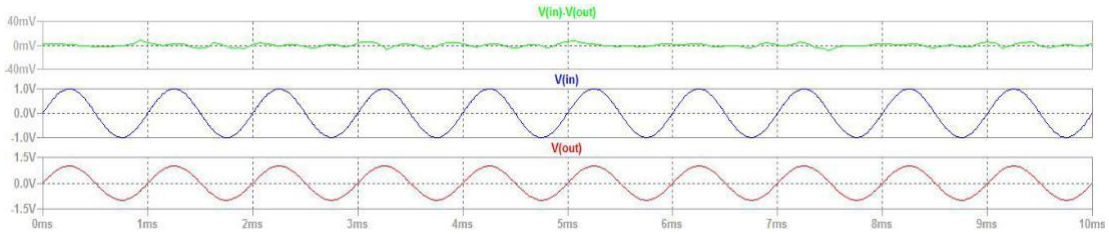

Fig. 7.10: Plot for Vin, Vout, and its difference at 1KHz

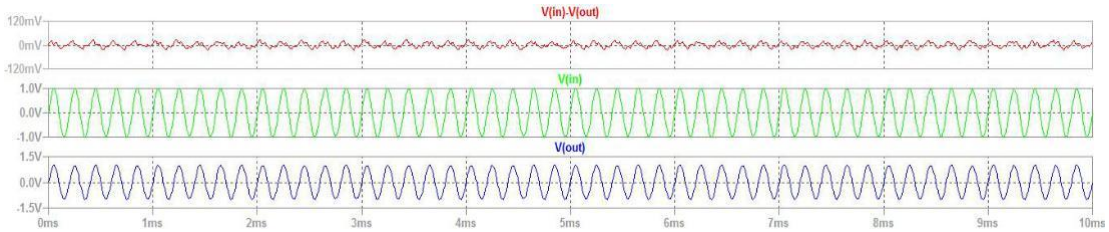

Fig. 7.11: Plot for Vin, Vout, and its difference at 5KHz

7.4.2 Simulation results of FTFN

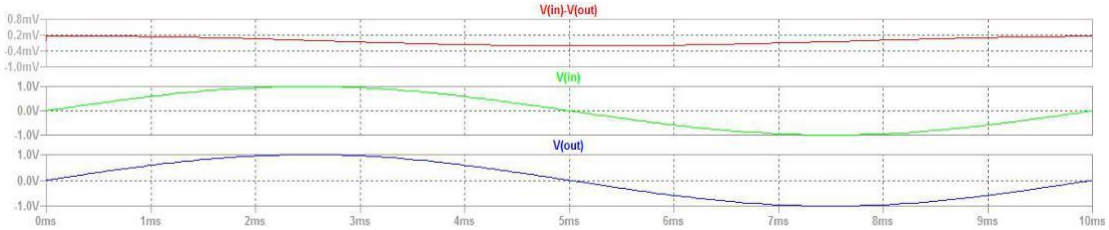

Fig. 7.12: Plot for Vin, Vout, and its difference at 100Hz

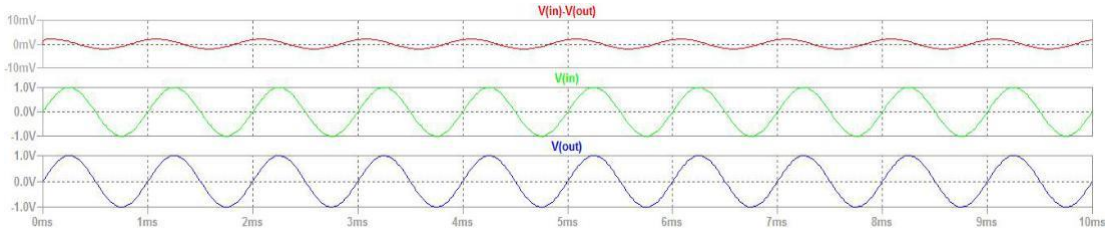

Fig. 7.13: Plot for Vin, Vout, and its difference at 1KHz

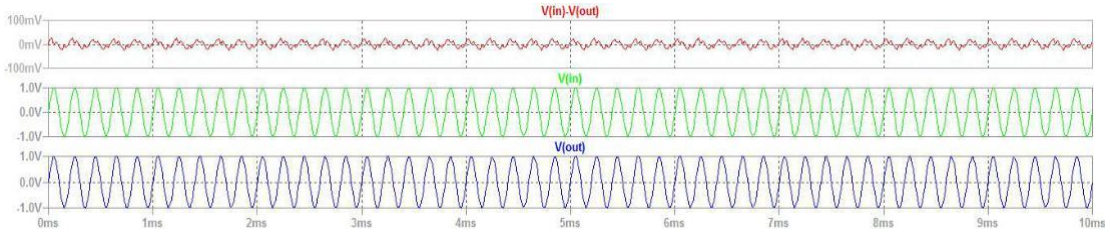

Fig. 7.14: Plot for Vin, Vout, and its difference at 5KHz

7.4.3 Simulation results of VDTA

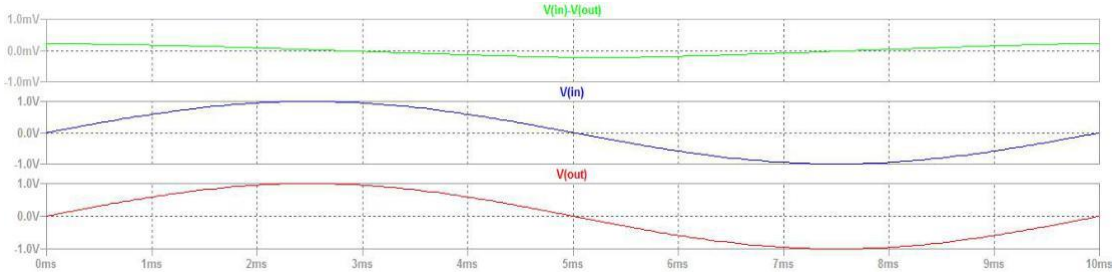

Fig. 7.15: Plot for Vin, Vout, and its difference at 100Hz

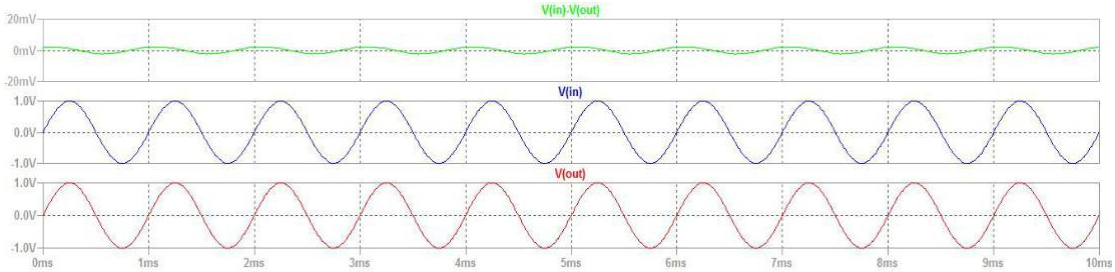

Fig. 7.16: Plot for Vin, Vout, and its difference at 1KHz

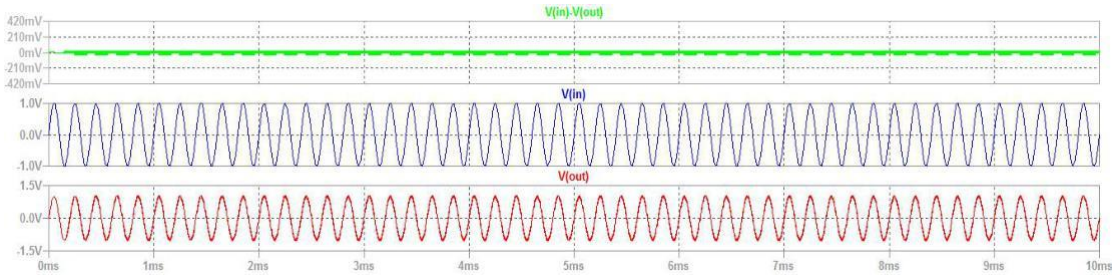

Fig. 7.17: Plot for Vin, Vout, and its difference at 5KHz

7.4.4 Simulation results of Hybrid- I

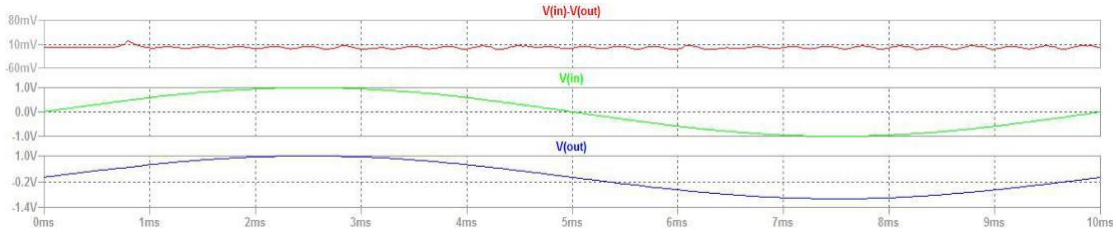

Fig. 7.18: Plot for Vin, Vout, and its difference at 100Hz

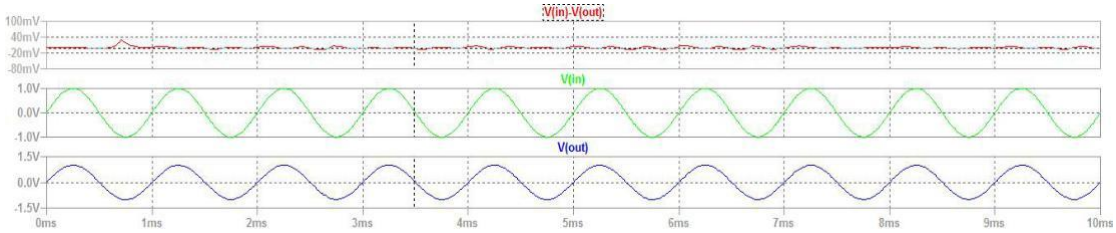

Fig. 7.19: Plot for Vin, Vout, and its difference at 1KHz

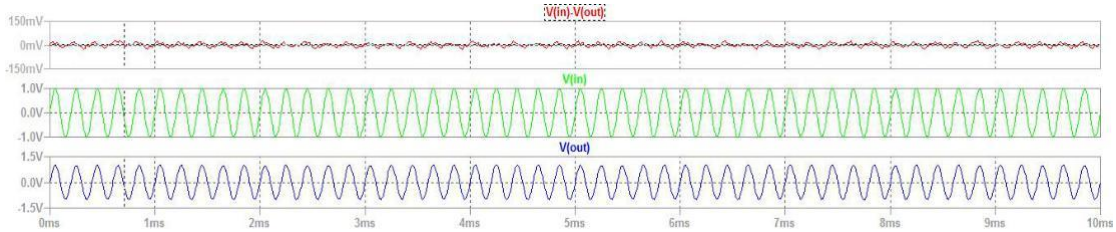

Fig. 7.20: Plot for Vin, Vout, and its difference at 5KHz

7.4.5 Simulation results of Hybrid- II

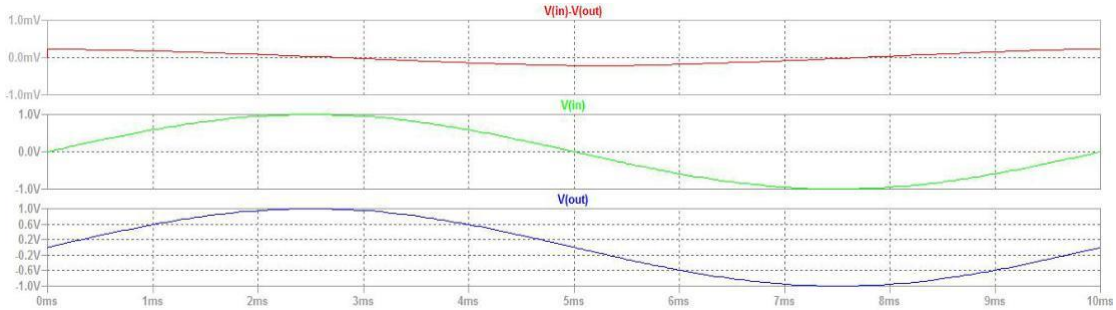

Fig. 7.21: Plot for Vin, Vout, and its difference at 100Hz

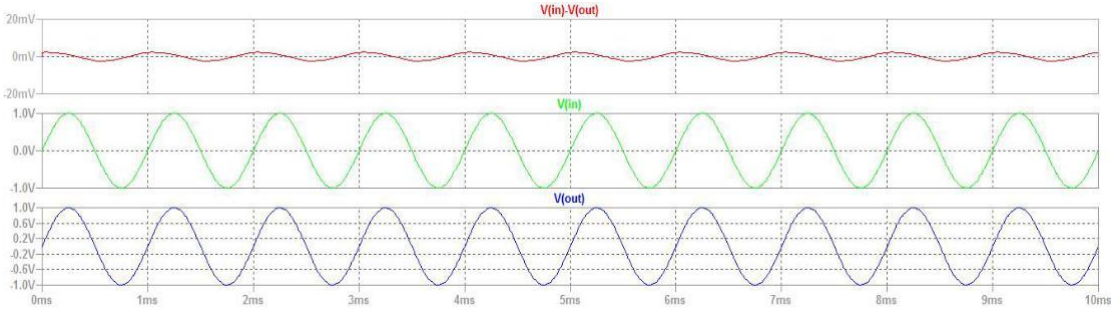

Fig. 7.22: Plot for Vin, Vout, and its difference at 1KHz

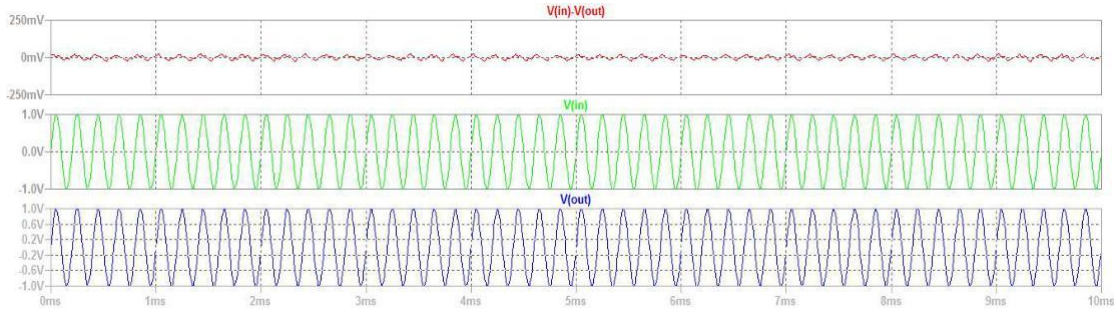

Fig. 7.23: Plot for Vin, Vout, and its difference at 5KHz

7.5 Conclusion

This chapter shows how a variety of active building blocks may be used to effectively realize chaos-based secure communication through various circuit implementations. the chaotic phenomenon utilizing various Active Building Blocks and a straightforward and well-known circuit known as Chua's circuit. We've employed these circuits for safe communication. Using different Active Building Blocks at different frequencies, the Vin-Vout Range of the retrieved signal for Chua's circuit is compared in the table.

Table: 7.1 Max. and Min. variation in Vin-Vout using chaos generator using active building blocks at various frequencies

Different Active Building Blocks	**100Hz**		**1 KHz**		**5 KHz**	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
Opamp	-7.0129m	5.067m	-8.03m	7.35m	-25.13m	20.93m
FTFN	-198.42u	158.4u	-1.98m	2.05m	-18.95m	21.10m
VDTA	-221.00u	219.0u	-2.38m	2.25m	-36.00m	36.00m
Hybrid- I	-5.63m	182.2m	-5.84m	28.5m	-25.60m	26.23m
Hybrid- II	-215.00u	220.0u	-2.39m	2.28m	-23.52m	20.47m

**m represents Milli, u represents Micro

CHAPTER 8

CONCLUSION, FUTURE SCOPE AND SOCIAL IMAPACT

8.1 Conclusion

The thesis includes a detailed study of chaotic systems and, as we proceed, we expand on this by designing chaotic circuits that involve Opamp, FTFN, VDTA and two hybrid circuits that eye their ability to securely transmit information across several spectrums. Table 8.1 display the comparison on how many components used and which combination can be used for which range of applications. This research focuses on understanding how chaotic signals are used in secure analog communication systems.

An Opamp is used in this Chua's Circuit [4]

With the AD712 Opamp, a typical Chua's oscillator was constructed which generated a double-scroll attractor. With piecewise-linear elements, the nonlinear resistor was developed, leading to stable and inexpensive chaotic behavior. I demonstrated double scrolling and modified a message signal.

FTFN chaotic oscillator [5]

The AD844-based Four Terminal Floating Nullor (FTFN) improved the performance at higher frequencies. As a result, the circuit needed fewer passive parts and demonstrated better linearity, particularly for high-speed use. The circuit showed double-scroll attractor behavior and applied it to modulate a message signal.

Chaotic Generator Created Based on VDTA [7]

This amplifier was selected because it could operate at a low voltage and used relatively few passive parts. It was discovered that the design, due to being compact and programmable, could be implemented well in CMOS technology. Found that the system can make two unstable loops and controlled how a feedback signal changed.

The idea of Hybrid Chaotic Circuits [9]

Two new circuits fusing key aspects of Opamp-VDTA and Opamp-FTFN were created. Using Opamps' wide bandwidth and the adjustability of

VDTAs/FTFNs, the chaos-based system was enhanced in terms of its complexity, stability and spectrum range. Improved both the bandwidth and reliability of synchronization needed for secure communication.

Communication System Implementation [10]

The signal of each chaotic generator was masked within a chaos communication system by superimposing the message signal on a chaotic carrier. The hardware cir12cuits for chaos had identical settings, helping achieve successful synchronization and signal decoding. The system can prove it operates effectively when signals are received successfully. A comparison of the waveforms at the sender and receiver sides confirmed that signal recovery was successful.

Table: 8.1 Comparison of components used and frequency range of chua's circuit using different active building blocks

Different Active Building Blocks	No. Of Components	Components	Frequency Range	
			V(x)	V(y)
Opamp	19	R-12 C-3 AD712-4	300KHz-1MHz	1KHz-100KHz
FTFN	14	R-7 C-2 L-1 AD844-4	4KHz-100KHz	4KHz-100KHz
VDTA	13	R-2 C-2 L-1 MOS-8	800KHz-1GHz	800KHz-500MHz
Hybrid- I	21	R-12 C-3 AD712-2 AD844-4	1KHz-500KHz	1KHz-200KHz
Hybrid- II	20	R-7 C-3 MOS-8 AD712-2	1KHz-800KHz	1KHz-800KHz

8.2 Future Scope

The research lays a robust foundation for several advanced studies and practical innovations:

ASIC and CMOS Implementation: The presented circuits can be optimized and implemented using standard CMOS technology, making them suitable for on-chip secure communication modules in IoT devices and embedded systems.

Digital and Mixed-Signal Realization: Future work could explore digitally programmable chaotic circuits using FPGAs or microcontrollers, enabling real-time reconfigurability and broader application domains such as adaptive encryption systems.

Multi-dimensional Chaos Systems: Expanding the circuit design to support 3D or n-scroll attractors can increase the entropy and encryption strength, ideal for complex secure systems or data hiding.

Application in Biomedical Signal Processing: Chaos-based systems can be used in medical telemetry for secure and low-power transmission of ECG or other vital signals, where data privacy and integrity are critical.

Integration with Modern Wireless Standards: The circuits may be adapted to function as physical-layer encryption modules in modern wireless systems like 5G, Zigbee, or Bluetooth, thereby enhancing native security.

AI and Chaos: Research may also focus on how chaotic signals can be used for neural network training, random weight initialization, or chaos-inspired algorithms in AI systems. This research supports many advanced investigations and practical inventions.

8.3 Social Impact

The implications of this work go beyond academic and technological domains, offering notable societal contributions:

Secure and Affordable Communication: The chaotic circuits can be deployed in resource-constrained environments (like rural regions, disaster zones) to ensure privacy and reliability in communication without heavy encryption hardware.

National Cybersecurity and Defense: Chaos-based analog encryption offers an indigenous, hard-to-crack alternative to conventional methods, making it attractive for defense applications requiring secure real-time voice or data transmission.

Educational Enhancement: The designs serve as valuable educational tools for engineering students to understand nonlinear dynamics, analog circuit design, and encryption, fostering innovation and research in core electronics.

Sustainability: With low power requirements and compact design, the circuits align with energy-efficient electronics, contributing to the broader goal of sustainable technology development.

Healthcare Data Protection: Integration of chaotic systems in medical electronics can protect patient data during remote diagnostics, especially with growing telemedicine adoption.

Digital Inclusion: Secure, low-cost communication circuits enable marginalized communities to safely access communication networks, reducing the digital divide.

8.4 Sustainable Development Goals

The thesis on "Study and Design of Chaotic Oscillators using Different Active Building Blocks for Communication Systems" aligns with several United Nations Sustainable Development Goals (SDGs). Here's a list of the relevant goals your work supports. Relevant Sustainable Development Goals (SDGs):

1. SDG 4 – Quality Education
Promotes practical and research-oriented learning in nonlinear systems, electronics, and secure communication. Supports engineering education by developing indigenous, simulation-based learning tools.

2. SDG 7 – Affordable and Clean Energy
Your low-power circuit designs contribute to energy-efficient electronic systems, especially suitable for embedded and portable devices.

3. SDG 9 – Industry, Innovation, and Infrastructure
Advances innovation in secure communication technologies. Encourages indigenous development of hardware solutions, reducing reliance on imported technologies. Supports the integration of analog cryptography in industrial and IoT infrastructure.

4. SDG 10 – Reduced Inequalities
By enabling low-cost, secure communication systems, your work helps bridge the digital divide for remote and underserved communities.

5. SDG 11 – Sustainable Cities and Communities
Enables development of secure, decentralized communication systems for smart cities, disaster communication networks, and rural connectivity.

6. SDG 12 – Responsible Consumption and Production

Encourages design of resource-efficient systems with fewer components, reduced complexity, and lower energy usage.

7. SDG 16 – Peace, Justice, and Strong Institutions
Enhances digital privacy and secure communication, which is critical for civil liberties and governance. Useful in secure public communication systems, law enforcement, and military-grade communication channels.

8. SDG 17 – Partnerships for the Goals
Encourages academic-industrial collaboration for developing indigenous, scalable technologies for secure communication, especially in national missions and public infrastructure.

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LIST OF PUBLICATIONS WITH PROOF

[1] B N Singh and K. Suneja, " Realization of Chaotic Circuit using Different Analog Building Blocks and its use in secure Communication," *International Conference on Data Science and Applications (ICDSA 2025) accepted to be presented on July 16-18, 2025, at Malaviya National Institute of Technology Jaipur, India*.

DTU Delhi Technological University

23/VLS/01 BRIJ NANDAN SINGH <brijnandansingh_23vls01@dtu.ac.in>

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Dear Brij Nandan Singh,

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PROFILE & VALUE

- **Enthusiastic VLSI and Embedded Systems aspirant having 10 months of hands-on expertise in VLSI design and verification, specializing in LVS and LPE.**
- **Developing design components for Process Design Kits (PDK), with scope covering LVS deck development, and testing.**
- **Experienced in creating layouts for different PDKs and optimizing design flows for Physical Verification, allowing me to deliver high-quality results and ensure project success.**
- **Performed Alpha testing and IP regression for different PDKs to ensure compliance with design specifications and have established efficient workflows for Physical verification, including LVS and LPE.**

EXPERIENCE

STUDENT TECHNICAL INTERN TRAINEE

NXP Semiconductor | Tools: Calibre, PVS, Virtuoso, Quantus(QRC), StarLite, LPEQA

July 2024 – Present Noida, India

- **5nm,16nm,28nm,130nm_pdk_TSMC:** Directed physical verification for IPs and Allcell including detailed LVS clean-up .
- **22nm,40nm_pdk_GF:** Managed LVS compliance ensuring quality sign-off also addressing LVS issues and ERC violations share the timely fix.
- **Layout design and RC Extraction:** Implemented All basic Logic gates and done the RC extraction for the same.
- **Block-level Physical Verification:** I led and managed block-level verification flows, including LVS to ensure compliance with TSMC and other foundry-specific design rules at advanced nodes.
- **Physical Verification Automation:** Spearheaded the automation of verification tasks using TCL, optimizing the verification cycle and reducing errors across multiple projects.
- **LVS Fixing:** Expertise in resolving LVS violations.

DEVELOPER

TCS

July 2019 – June 2023 Noida, India

- **Maximo Consultant in SEADRILL and CARDINAL HEALTH Account:** Contributed to multiple enhancements and defect resolutions. Also shared several process improvement activities which enhances the productivity.

TECHNICAL SKILLS

Category	Details
Courses	ASIC Design Flow, Digital Electronics, Digital IC Design, Verilog, Static Timing Analysis (STA)
Tools	Cadence Virtuoso, Calibre, PVS, StarLite, Quantus QRC, LTspice, Xilinx Vivado ISE
Languages	C, TCL, Linux, SKILL
Physical Verification	DRC, LVS, LPE, Layout Optimization, Test Case Creation

EDUCATION

Master of Technology (VLSI DESIGN & EMBEDDED SYSTEMS)

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2012 Varanasi, U.P.

- **CGPA 10**

ACADEMIC PROJECTS

Design of Full Adder VLSI

- Designed 1 bit full adder by using cadence virtuoso, gpdk 180nm technology is used.

Moore FSM Sequence Detector

- This was implemented using Xilinx ISE Design Suite.

ACHIEVEMENTS

- **Service & Commitment Award:** 22-Jul-2022
- **Star of the Month Award:** 11-Apr-2022
- **On The Spot Award:** 16-Mar-2021
- **Coordinator in SHAURYOTSAVA 2017, I.E.T. Lucknow.**