Study and simulation of VCII+ and its applications

A

MINOR PROJECT REPORT

Submitted by

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MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEM

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CERTIFICATE

This is to certify that the Minor project titled **"Study and simulation of Voltage Conveyor II+ and its application"** is a bonafide record of work done by **Nikkee Kumari, Roll No. 2K19/VLS/09** at **Delhi Technological University, New Delhi** for the Minor Project. This project was carried out under my supervision and has not been submitted anywhere else, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

Date: 24.1.21

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At the end I would like to express my sincere thanks to all friends and others who helped me directly and indirectly during this project work.

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ABSTRACT

In this project, simulation of an analog block "Second Generation Voltage Conveyor" has been implemented at 180nm technology node. Technology node has been reduced in order to reduce the area requirement in such a way to improve its characteristics. Static Power dissipation is also getting reduced because of reduction in Mosfet sizes and Supply Voltages. Delay also reduces with reduction in Technology Node and Supply Voltages

In the end, simulation work has been carried using this block in applications like Amplifier, Integrator, Differentiator, V to I convertor, Voltage Buffer and Current Buffer to check the transient and frequency response of these applications. The performance of all the designs is investigated through extensive Cadence Virtuoso simulations using 180nm technology node and 0.9volt Power Supply.

Chapter-1 Introduction

1.1 background

Electronic systems are an inseparable part of everyday life. Analog circuits comprise a large part of electronic systems. As the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power and area consumption. Therefore, with the growing popularity and demand for the battery-operated portable devices such as mobile phones, tablets, and laptops, the designers try to reduce power consumption and area of such systems while preserving their speed. Optimizing the W/L ratio of transistors is one approach to decrease the power-delay product (PDP) of the circuit while preventing the problems resulted from reducing the supply voltage.

Recently, a new class of active building blocks called voltage conveyors (VCs) has attracted the attention of researchers. The sparkling feature of VCs is having both high impedance current output port and a low impedance voltage output port. Therefore, they can be suitably used in applications requiring output signal in the form of voltage or current.

1.1 Second Generation Voltage Conveyor (VCII+)

It is a three-port analog block, where terminals are denoted by X, Y, and Z. The outputs of its three ports in terms of their corresponding inputs at relatively low frequencies are represented by

$$\mathbf{Ix \approx - \beta * Iy,}$$

$$\mathbf{Vz = \alpha * Vx,}$$

$$\mathbf{Vy = 0}$$

where α and β (close to unity) are current gain between Y and X terminals and voltage gain between X and Z terminals, respectively.

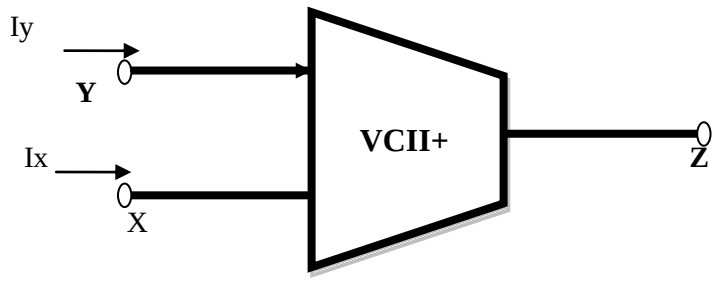

Fig.1.1.1. VCII+ symbol

Y and Z terminals in VCII+ have a low impedance (ideally zero) while X is a high impedance (ideally infinite) terminal.

The Y terminal is a current input terminal with ideally zero input impedance, the X terminal is a current output terminal with ideally infinite impedance and finally the Z terminal is a voltage output terminal which has ideally zero impedance. Therefore, the internal structure of a VCII+ consists of a current buffer between Y and X terminals and a voltage buffer between X and Z terminals.

1.2 Organisation of report

This report work is organized into 4 chapters.

Chapter 1 deals with the introduction of VCII+ as a convenient building block that provides a simplified approach to the design of analog systems with either current or voltage outputs.

Chapter 2 presents the simulation of characteristics of Voltage Conveyor II+.

Chapter 3 presents the simulation work of applications designed using VCII+. These applications are: Voltage Amplifier, Voltage Integrator, Voltage Differentiator , V to I convertor, Voltage Buffer, Current Buffer.

Chapter 4 concludes the work with brief summary of this dissertation and future scope of this work.

Chapter-2

2.1. Implementation of a VCII+ at 180nm CMOS Technology (Supply Voltages ±0.9volt)

A CMOS implementation of a VCII+ [1] is shown in Fig.2.1. It is composed of a current buffer between Y and X terminals and a voltage buffer between X and Z terminals. The current buffer is formed with transistors M1-M7 and current sources IB1-IB4, while the voltage buffer is also made of M8, MA1-MA3 and IB5- IB7 current sources. Negative feedback loop, established by M1-M3, sets the offset voltage at Y terminal equal to ground and reduces its impedance. The second negative feedback loop, formed by M4-M7 transistors, further reduces the impedance at Y terminal and transfers input current to X terminal. Also, a super transistor (MA1-MA3) [2-3] has been used in the implementation of voltage buffer. The negative feedback loop in the super transistor provides a very low impedance at Z terminal and a high accuracy in transferring voltage signals between X and Z terminals.

This circuit is implemented at 180nm CMOS Technology and Supply Voltages of ±0.9Volt are used**.**

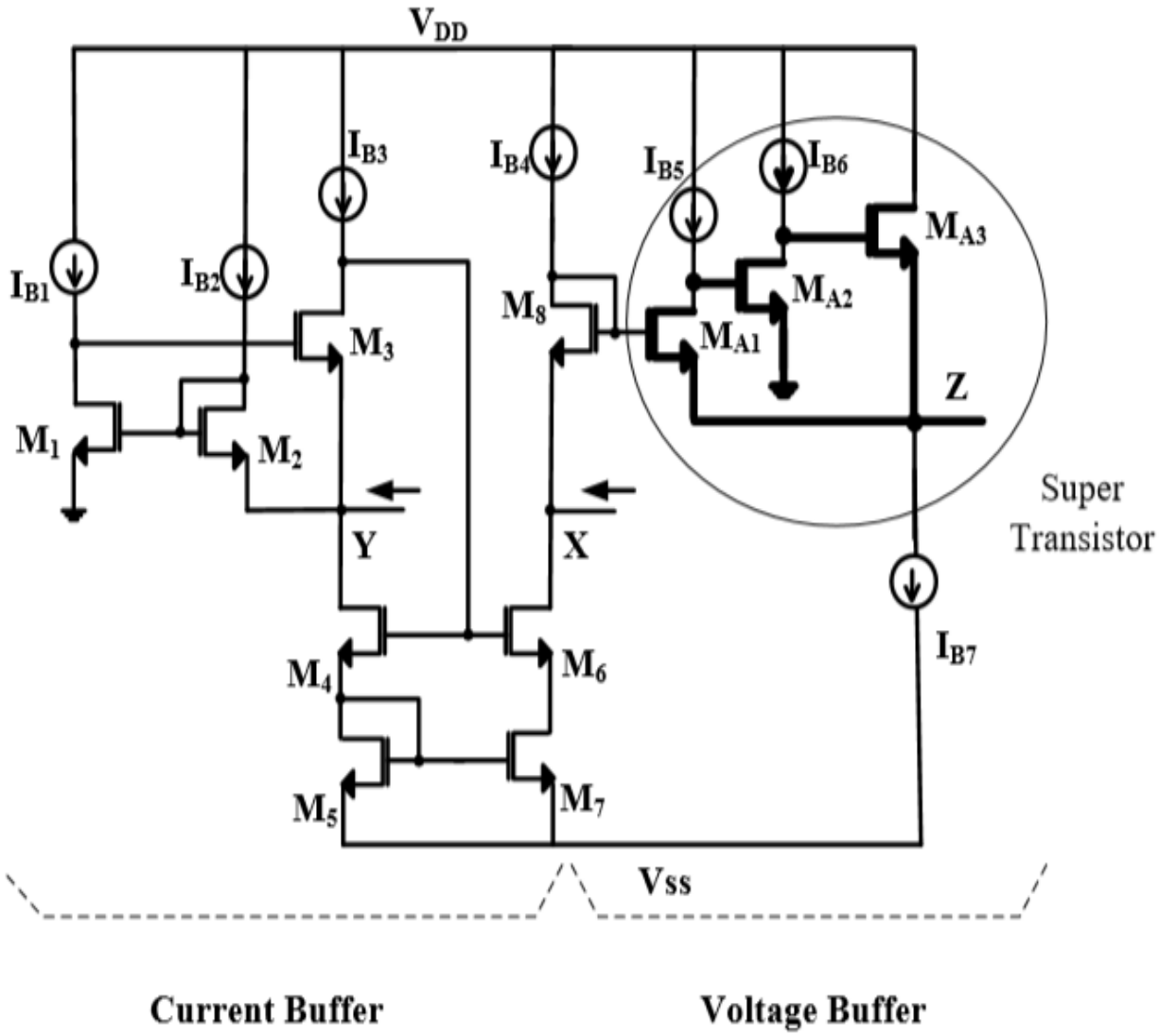

Fig.2.1.1 CMOS implementation of a VCII+

Mentioned below are the aspect ratios of MOSFET transistors and the values of current sources used in this simulation.

TABLE-I. Transistors Aspect ratios

Transistor	W(um)	L(um)	Type
M1	18	0.180	nmos
M2	18	0.180	nmos
M3	18	0.180	nmos
M4	1.8	1.8	nmos
M5	1.8	1.8	nmos
M6	1.8	1.8	nmos
M7	1.8	1.8	nmos
M8	45	1.8	nmos
MA1	45	1.8	nmos
MA2	1.8	0.180	nmos
MA3	1.8	0.180	nmos

TABLE-II. The value of current sources

Current Source	Value(uAmp)
IB1	8
IB2	8
IB3	7.5
IB4	15.5
IB5	15.5
IB6	7
IB7	23

2.2 Simulation Results

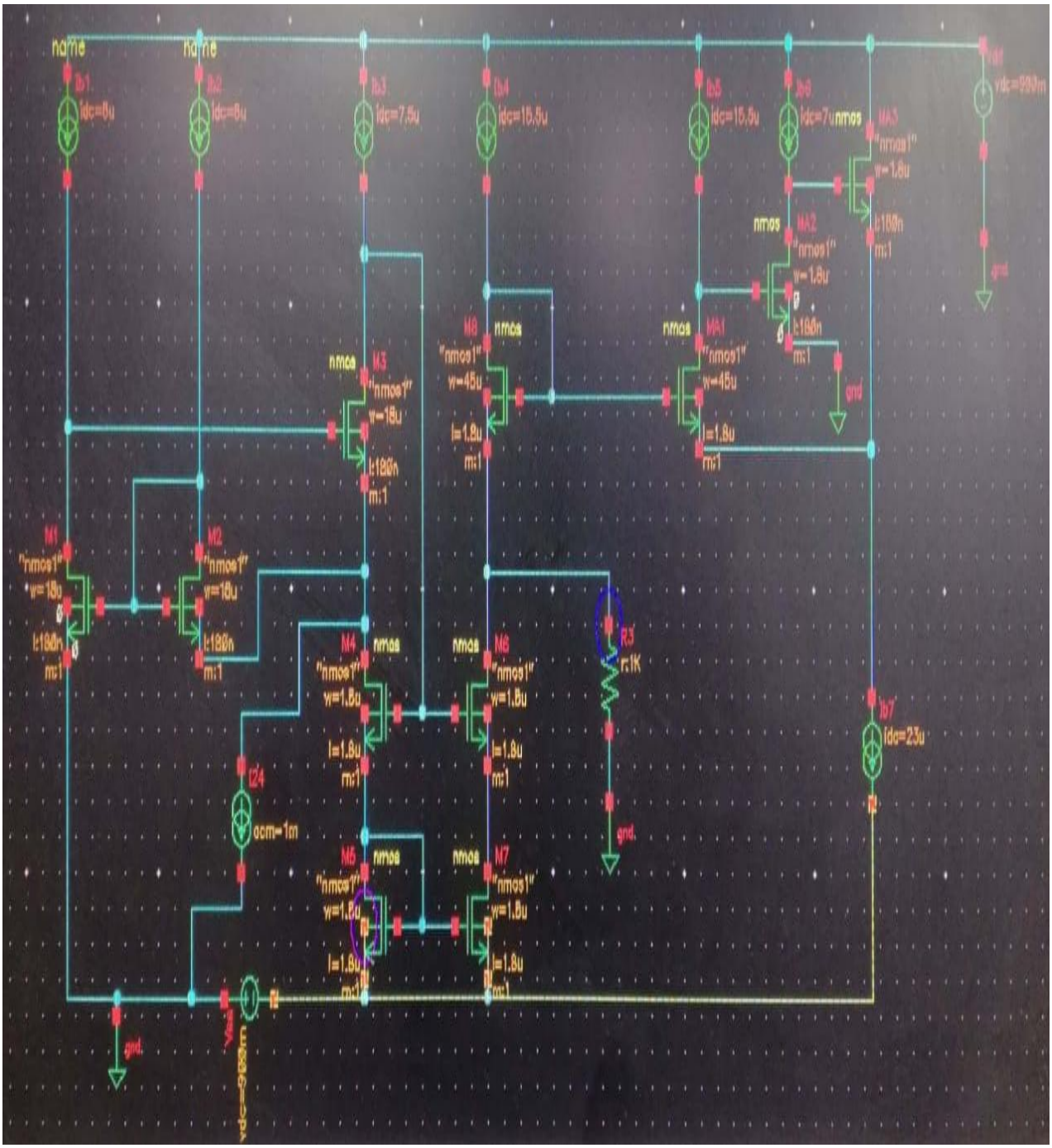

Fig.2.2.1 schematic for VCII+ circuit simulation

There is a current buffer that exists between node Y and node X of VCII+. Ideal value of β is Unity. From graph in fig 2.2.2,

β lies in the range **0.994 to 1.002**.

When Ix=0 there is current of **73.22 pAmp** flowing through Y node. This is happening because current gain β is not unity. So there is a small offset in the range of picoAmp.

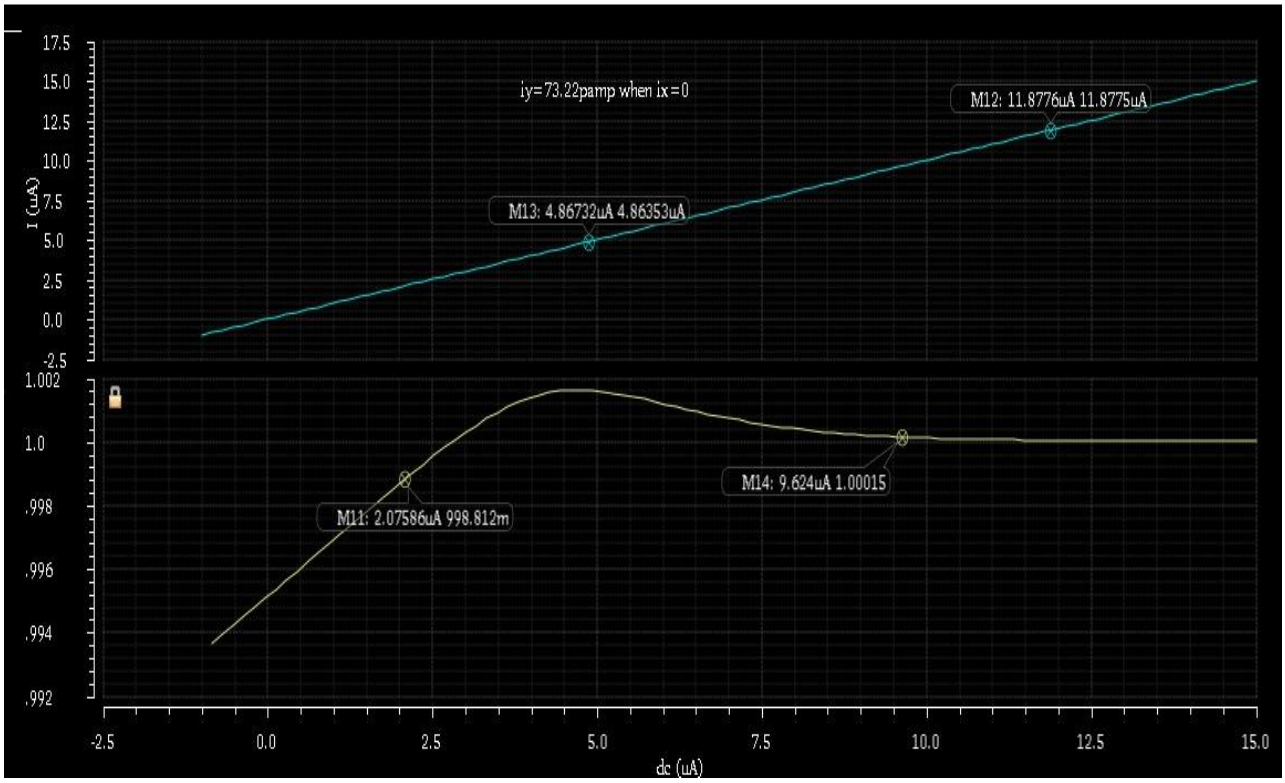

Fig.2.2.2 graph for Ix v/s Iy and current gain β

There is a voltage buffer between Z and X node of Voltage Conveyor II+ i.e Vz = α Vx where α is voltage gain. Ideal value of α should be 1. Value of α as shown in graph of fig 2.2.3.

α = 0.99

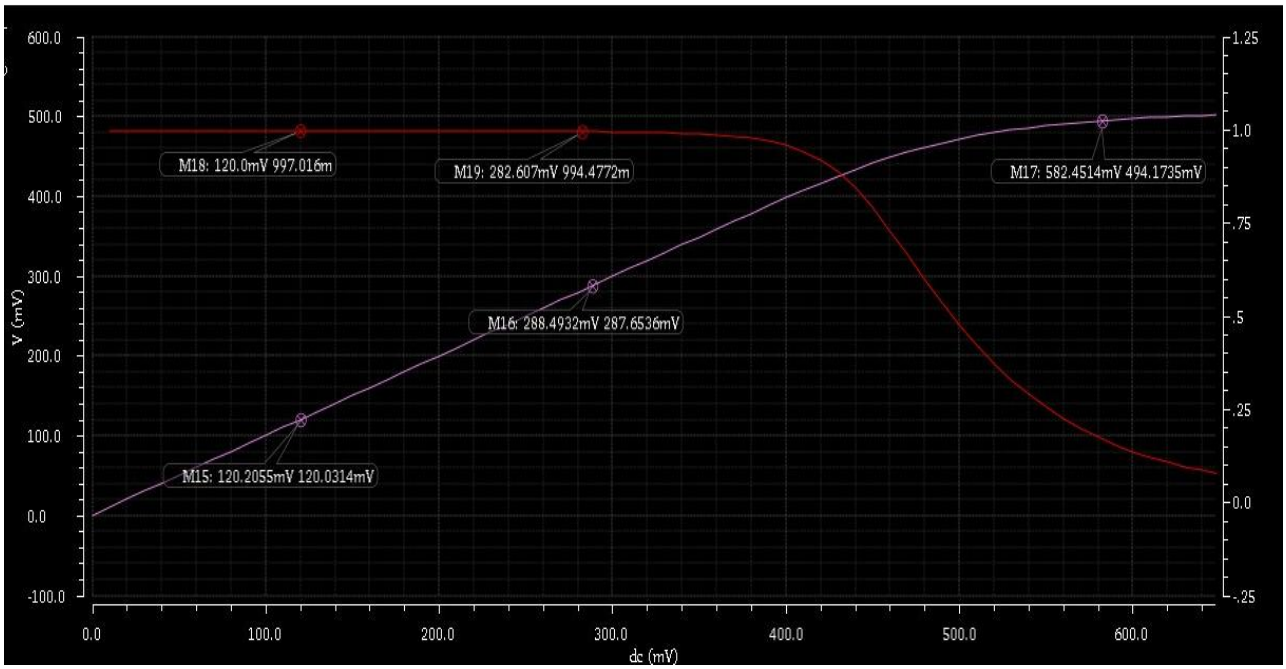

Fig.2.2.3 Plot for Vz v/s Vx and Voltage gain α

Parasitic Impedances are present at three nodes X, Y, Z of Voltage Conveyor II+. The Y terminal is a current input terminal with ideally zero input impedance, the X terminal is a current output terminal with ideally infinite impedance and finally the Z terminal is a voltage output terminal which has ideally zero impedance.

From graph in fig 2.2.4 calculated values for parasitic at different nodes are (**10KHz frequency**)

Node X:

Rx=1.7965MΩ Cx=3.353nF

Node Y:

Ry=65.999Ω Ly=4.04uH

Node Z:

Rz=0.7641 Ω Lz=1.58uH

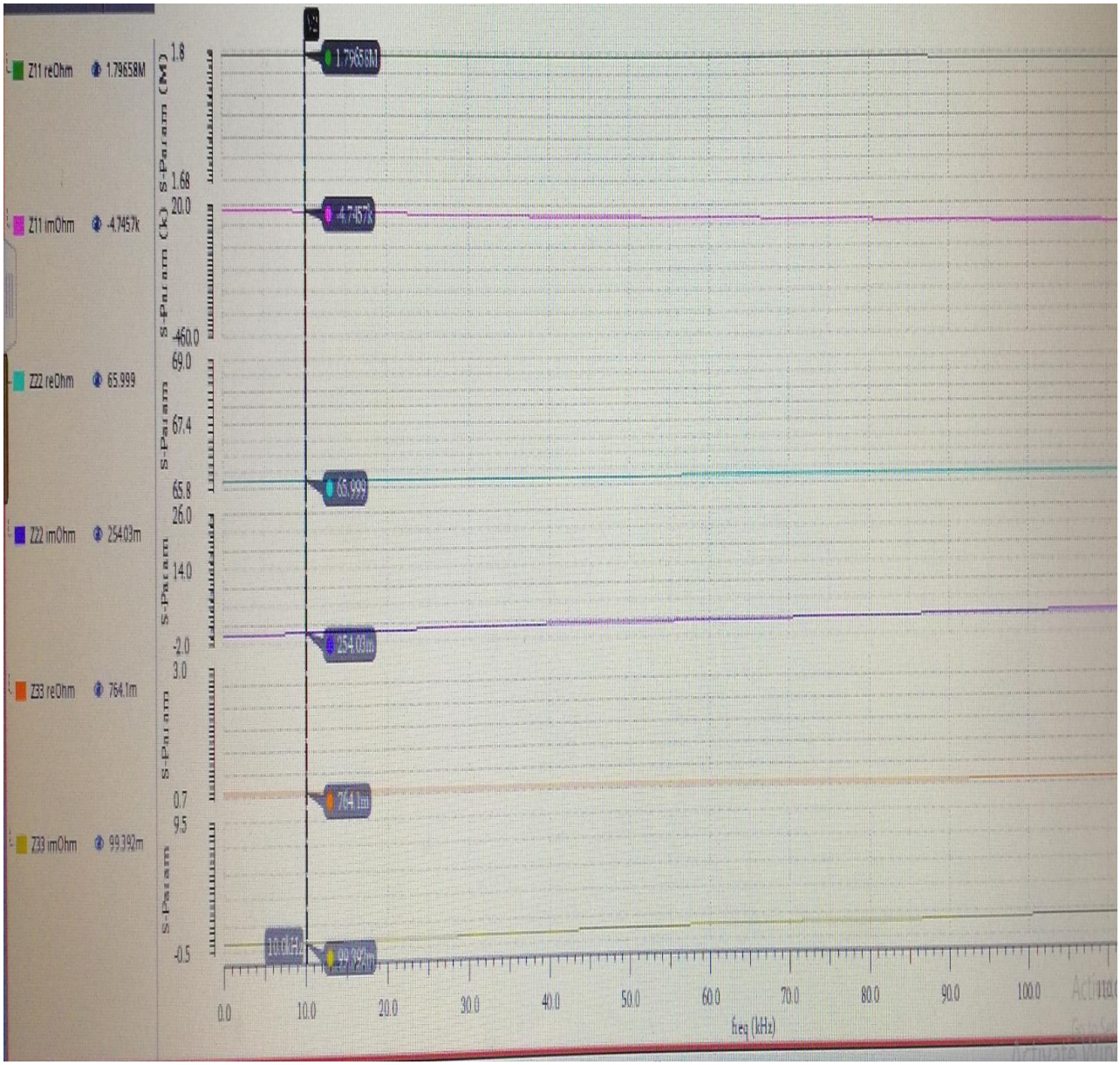

Fig.2.2.4 Graph for calculating parasitic impedences at nodes X, Y And Z.

TABLE-III The proposed VCII+ performance parameters

Parameter	Value	Ideal Value
Technology node	180nm	-
Supply Voltages	±0.9volt	-
Rx , Cx	1.7965MΩ , 3.353nF	∞
Ry , Ly	65.999Ω , 4.04uH	0
Rz , Lz	0.7641Ω , 1.58uH	0
α	0.99	1
β	0.99	1
Static Power Consumption	152.1uWatt(84.5µAmp)	-

Chapter-3 VCII+ applications

3.1. Voltage Amplifier

Function of Voltage Amplifier is to produce an amplified replica of applied input voltages. Voltage conveyor can be used as to implement a voltage amplifier as shown below in fig.3.1.1.

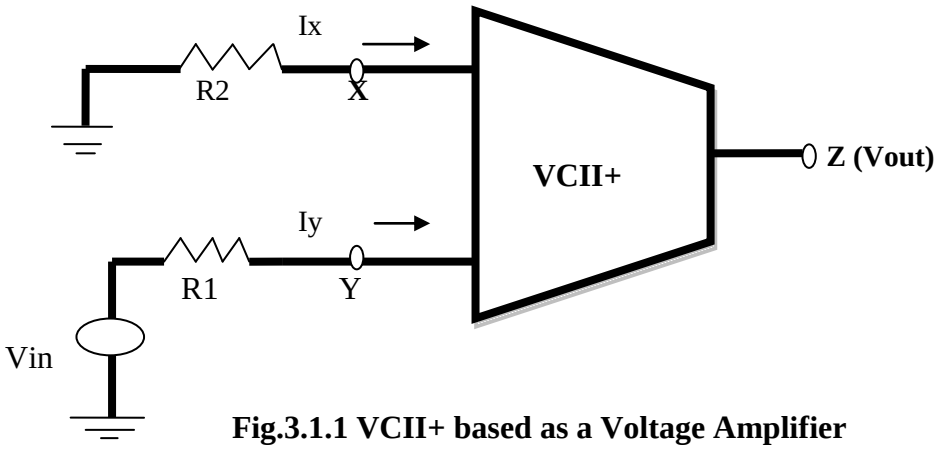

Fig.3.1.1 VCII+ based as a Voltage Amplifier

By ignoring the parasitic of VCII+ nodes, Current flowing through node Y can be found as

$$Iy = Vin / R1$$

as node Y is at Ground Potential. As a result of the current-buffer between Y and X terminals, *Vx* is found as:

$$Vx = -R2*Iy = - R2*\beta*(Vin/R1)$$

There is a voltage buffer between Z and X node of Voltage Conveyor II having voltage gain of β. Combining all the above relations, Voltage Gain of amplifier using VCII+ can be found as

$$\mathbf{Av = Vout /Vin = -\beta*\alpha*(R2/R1)}$$

where values of α and β are close to unity. Realizing Voltage Amplifier using VCII+ requires only one VCII+ block that results in reduced power consumption and a simpler circuitry. Transfer functions implemented with VCII exhibit wider frequency performance.

3.1.1 Response of Voltage Amplifier to a step input

Transient analysis is done in order to check the step response of voltage amplifier and the delay associated with it. A step of 10mvolt is applied as input signal.

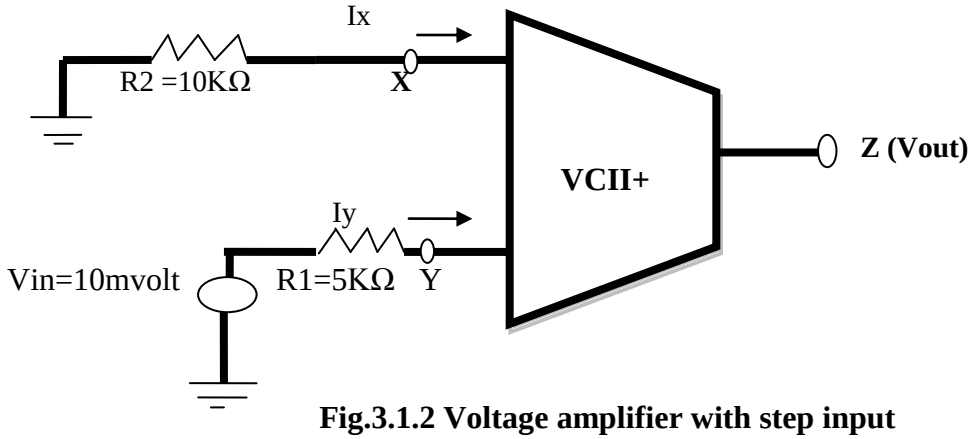

Fig.3.1.2 Voltage amplifier with step input

Value of Resistances R1 and R2 used for transient analysis are: **R2 = 10KΩ and R1= 5KΩ**.

Voltage Amplifier Realized is of inverting type using VCII+. Gain of amplifier Av using the above values of resistances:

Voltage Gain of amplifier Av=2.

There is an offset of 1mvolt as can be seen from the simulated graph below. This offset is present because of values of β and α are close to unity i.e 0.99 and not unity which is the ideal value. Delay is 38nsec.

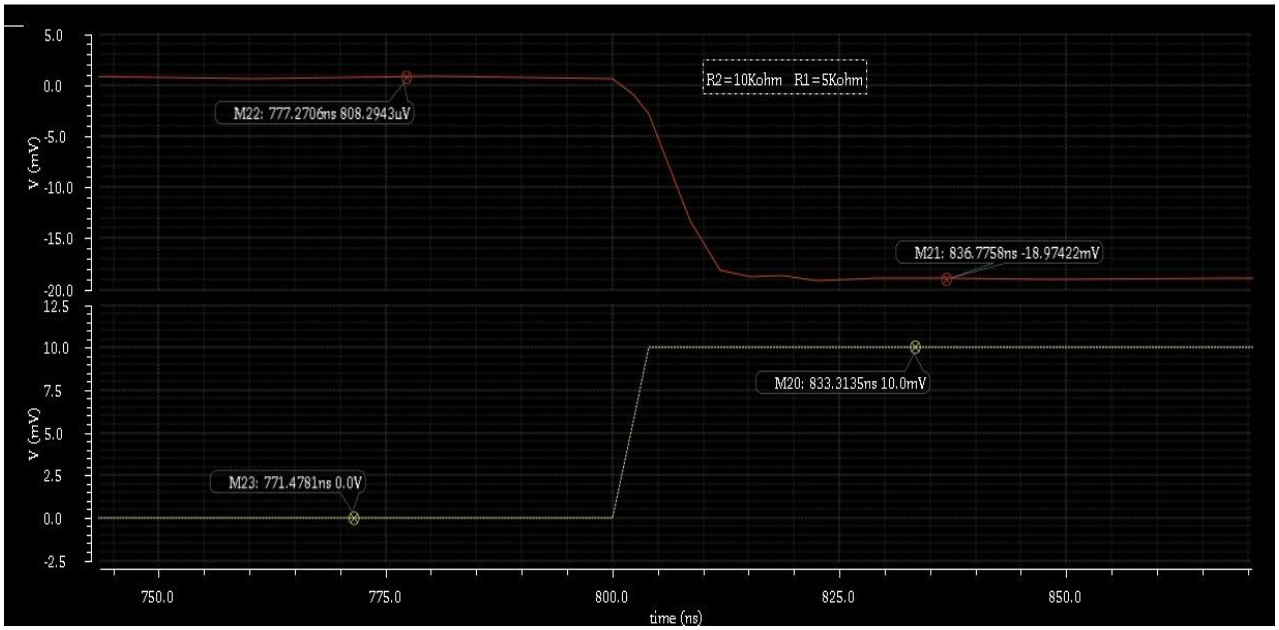

Fig 3.1.3 Step Response of Voltage Amplifier

3.1.2 Frequency Response analysis of Voltage Amplifier for different gains

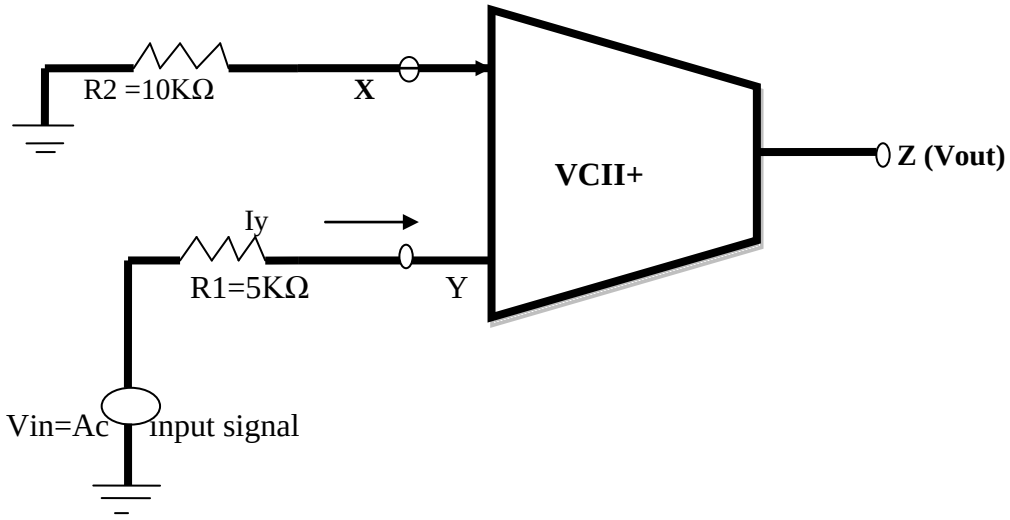

Fig.3.1.4 voltage amplifier for frequency analysis with gain 2.

AC analysis of voltage amplifier is done in order to check the Gain and Bandwidth. A unit amplitude ac signal is used as input and frequency is varied for this analysis. Bandwidth is high as there is no feedback used in realizing it. As shown in fig 3.1.4, Values of Resistances are**:** R2=10KΩ, R1=5KΩ.

Using these values calculated ideal Gain is:

Av = Vout / Vin = 2 = 6.02dB.

But the actual gain as can be seen from the fig 3.1.5 is 5.92 dB. There is a deviation of 0.1dB from the ideal value. 3dB Bandwidth as can be seen from below graph at voltage gain of 2 is:

3dB Bandwidth = 151.69 MHz.

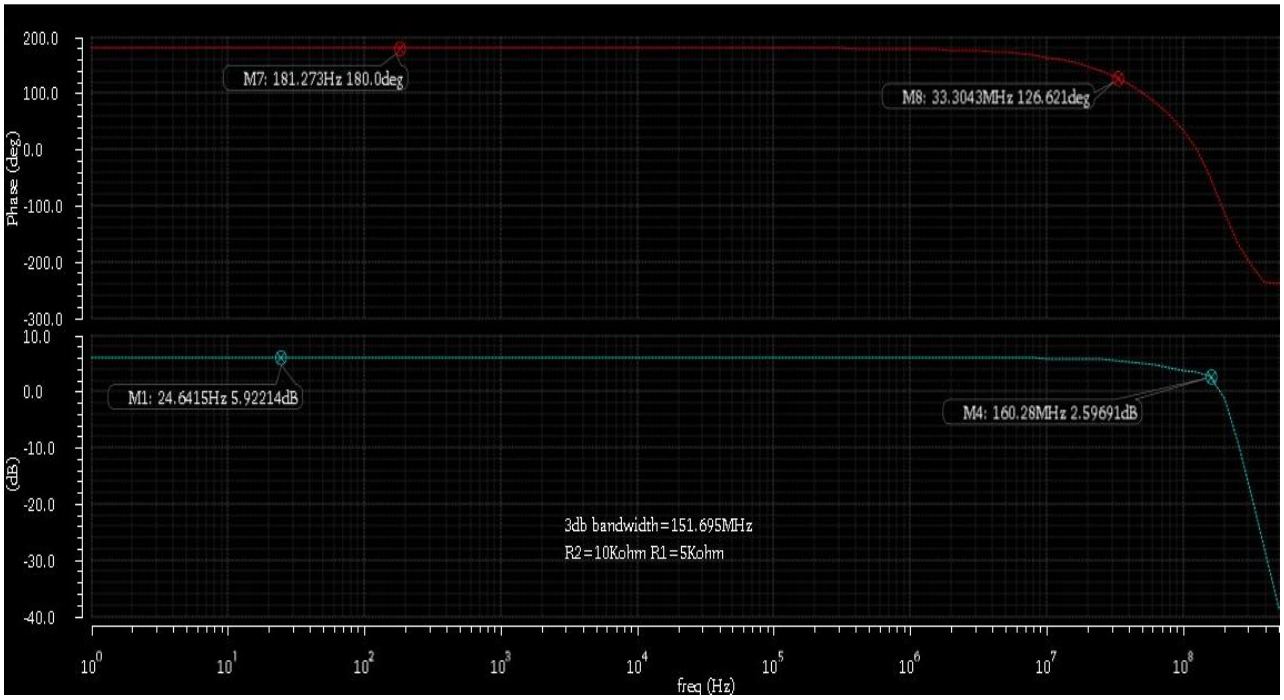

Fig 3.1.5 Frequency Response plot of voltage amplifier with voltage gain 2.

Frequency response for amplifier gain of 5 is shown in fig 3.1.6. Values of Resistances in fig 3.1.6 are: **R2=5KΩ, R1=1 KΩ**. Using these values calculated Gain is:

Ideal gain Av = Vout / Vin = **5 =13.97dB.**

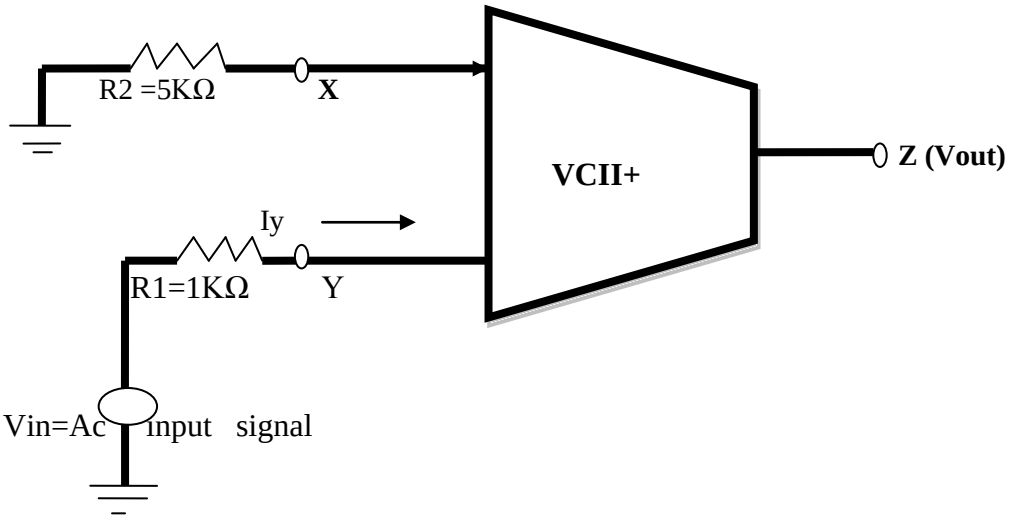

Fig 3.1.6 frequency analysis of voltage amplifier for a voltage gain of 5

But the actual gain as can be seen from the frequency plot in fig 3.1.7 is 13.679 dB. There is a deviation of 0.3dB from the ideal value. 3dB Bandwidth as can be seen from below graph at voltage gain of 5 is:

3dB Bandwidth = 50.23 MHz.

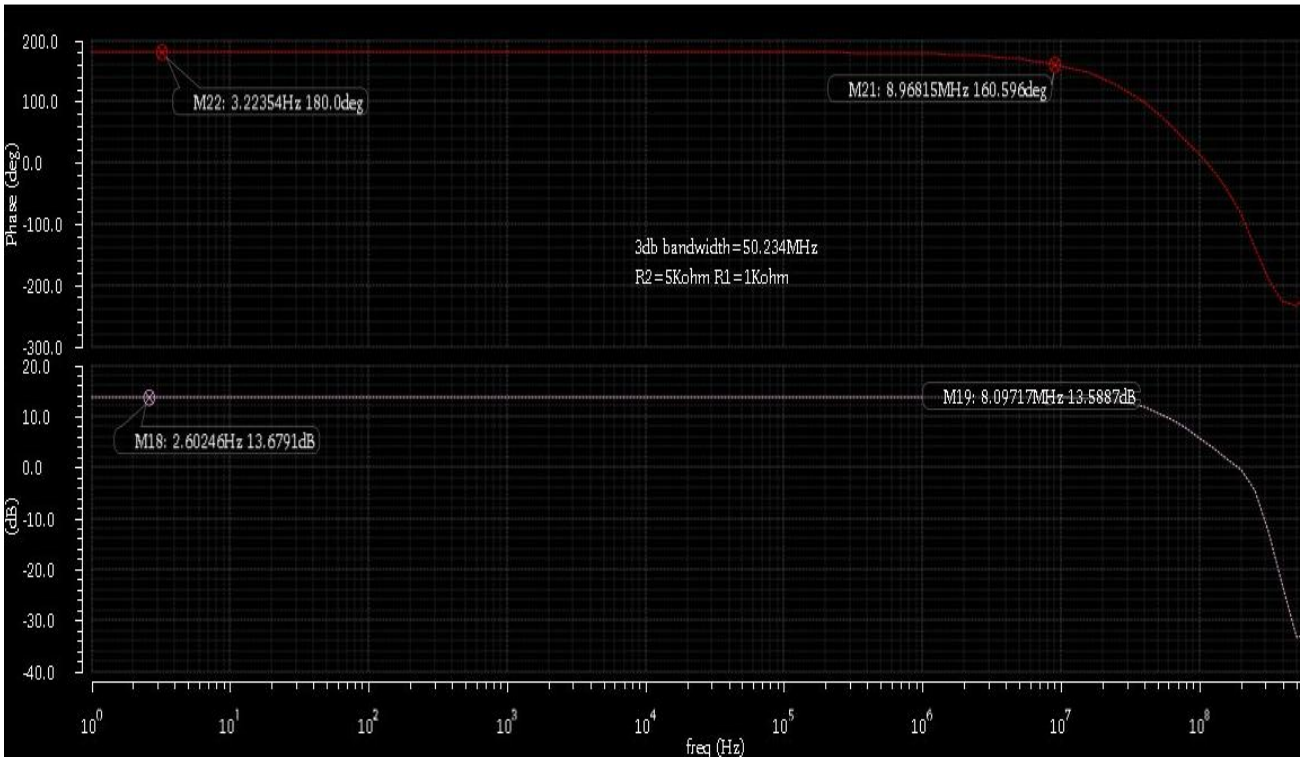

Fig 3.1.7 Gain and Phase plot of voltage amplifier with gain of 5.

3.2 Voltage Differentiator

Mathematical operation of Differentiation is being performed by this circuit and output follows the rate of change of input. Fig 3.2.1 shows the application of VCII+ to perform a voltage differentiation. In this circuit, the transfer function is found as (by ignoring VCII parasitic):

Vout / Vin = α β S C R

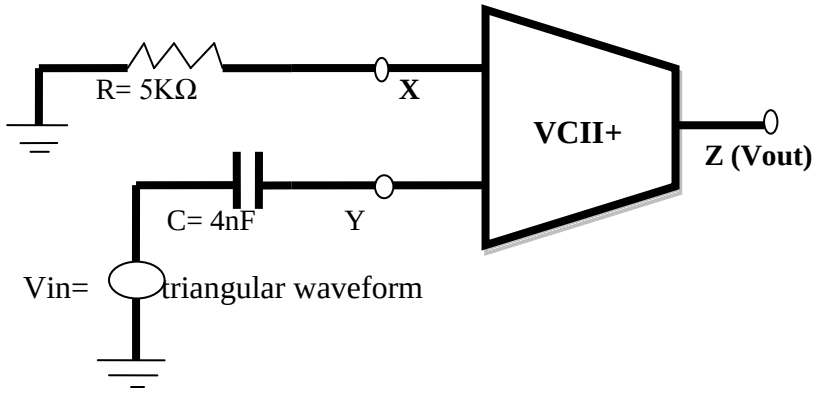

Fig 3.2.1 Voltage Differentiator using vcII+

As shown in Fig 3.2.2 is the simulated graph for Voltage Differentiator. In this graph input waveform is a triangular waveform having peak to peak voltage of ±100mVolt. Output is a square waveform having peak to peak value of ±20mVolt and is inverted.

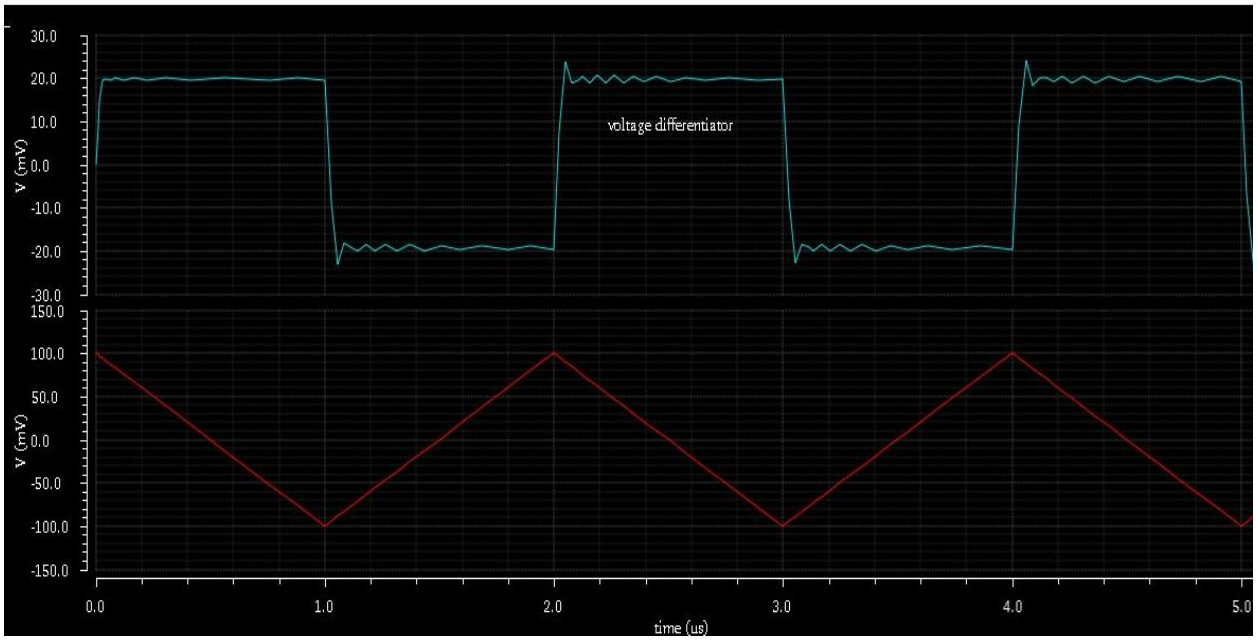

Fig 3.2.2 Simulated graph for Voltage Differentiator

Again, in this case, the advantage of using a VCII as a voltage differentiator is that only one building block is required. It is important to note that, for differentiator application, the output is inverted.

Compared to Op-amp Based differentiator, VCII based circuits enjoy low power consumption and reduced complexity.

3.3 Voltage Integrator

Mathematical operation of Integration is being performed by this circuit and input follows the rate of change of output. Fig 3.3.1 shows a voltage integrator realized using VCII+. The transfer function of VCII+ based voltage integrator (by ignoring parasitic) is expressed as:

$$\mathbf{Vout / Vin = \beta * \alpha * (1/S\ C\ R)}$$

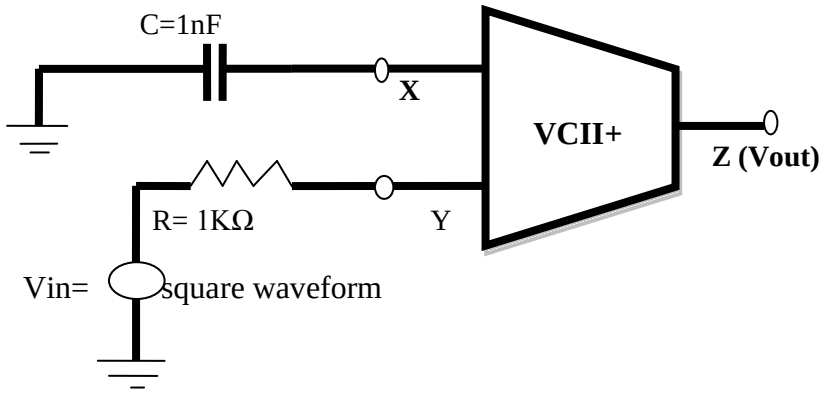

Fig 3.3.1 Voltage Integrator realized using VCII+

Input as shown in fig 3.3.2 is a square waveform with **peak to peak ±100mvolt**. Output of Integrator using VCII+ is a triangular waveform with **peak to peak approx ±500mvolt** with very small offset. Output waveform is also inverted. It is important to note that, for integrator application, the output is inverted. Compared to Op-amp Based integrator, VCII based circuits enjoy low power consumption and reduced complexity.

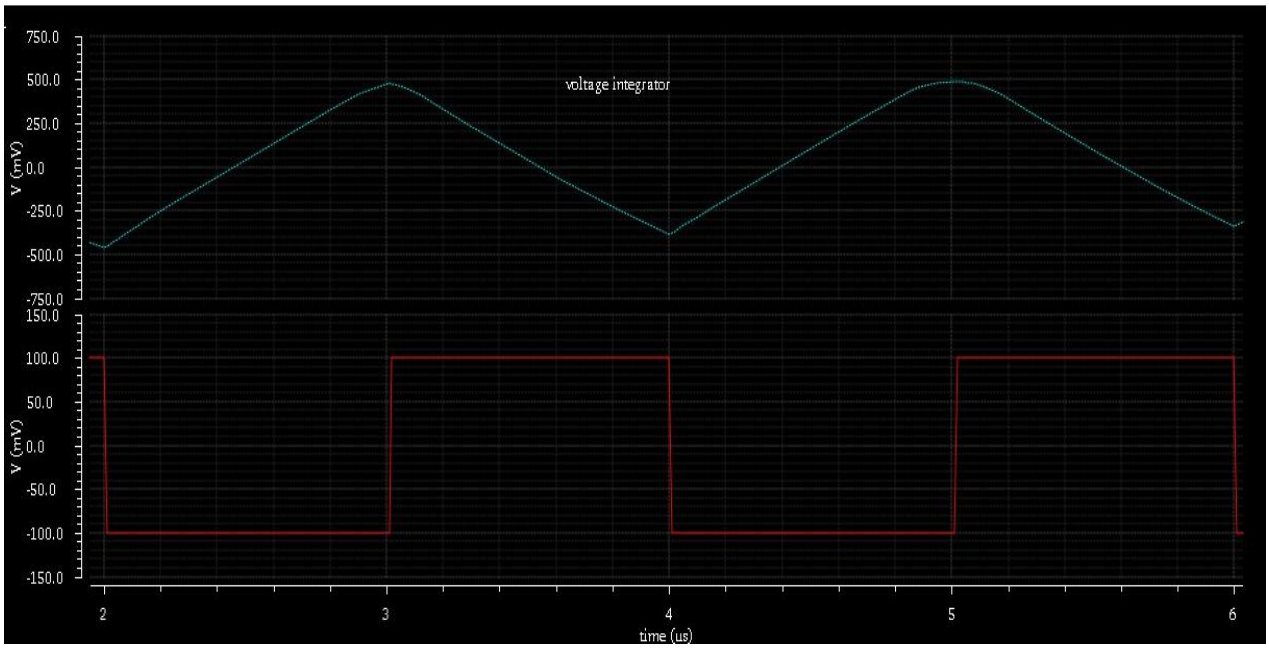

Fig 3.3.2 Voltage Integrator simulated graph

3.4 Current Buffer

Current Buffer is an electronic circuit used to transfer current from input having less impedence to output having high impedances. It is designed to prevent signal sources from getting affected because of any difference in amount of current drawn by output loads. Show in the fig 3.4.1 is application of VCII+ as current buffer. Current input in the range 0 to 15µAmp is applied at the input node Y. Current Output is taken at node X. The transfer function of a current buffer:

$$\mathbf{Iout / Iin = \beta}$$

The input impedance is equal to *Zy* and the output impedance is *Zx*.

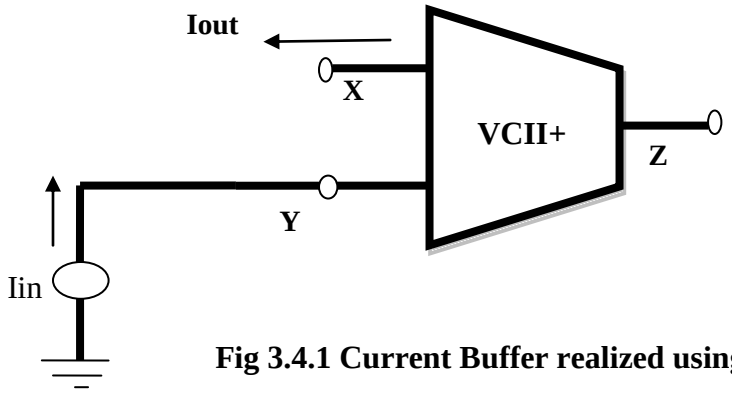

Fig 3.4.1 Current Buffer realized using VCII+

From above graph fig 3.4.2 it can be seen that output current is following the input current. value of current buffer gain lies in the range **0.994 to 1.002.**

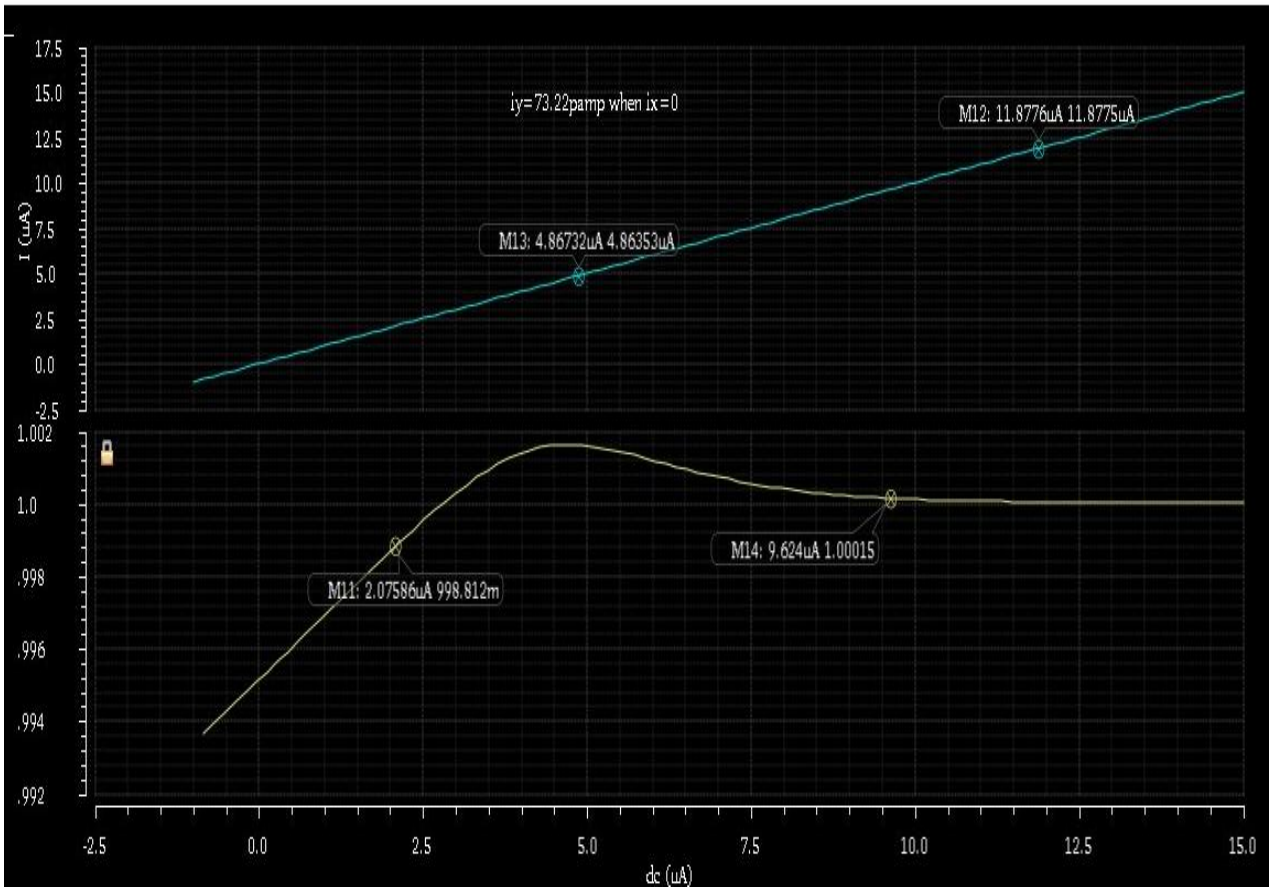

Fig. 3.4.2 Simulated graph for current buffer

3.5 Voltage Buffer

Voltage buffer Circuit can also be implemented using VCII+.For a voltage buffer, the transfer function:

Vout / Vin= α

For VCII-based voltage buffer, the input impedance is equal to *Zx* and the output impedance is *Zz*.

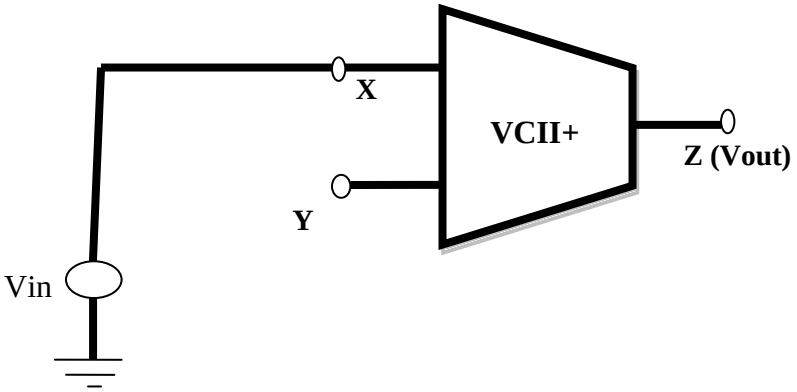

Fig 3.5.1 Voltage Buffer realized using VCII+

Shown in fig 3.5.2 is simulated graph for Voltage buffer. Its gain is close to unity for voltage below 400mVolt.

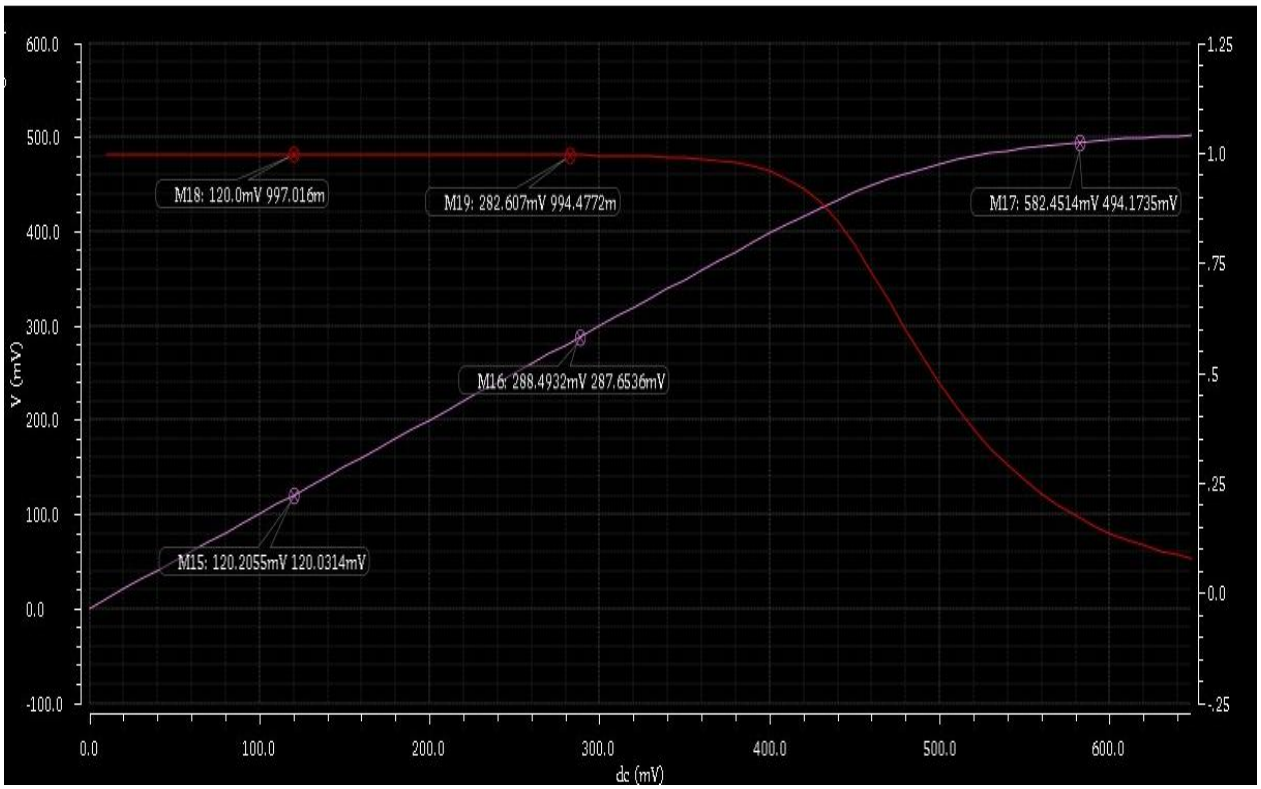

Fig.3.5.2 Voltage Buffer simulation result

3.6 V to I Converter

Fig 3.6.1 shows the application of VCII as V to I converter. Input voltage is applied at Y terminal and output current is taken at X terminal. Output current proportional to input voltage is obtained and proportionality constant is defined by the value of R choosen. By ignoring terminals parasitic, a simple analysis gives its transfer function as:

Iout / Vin = β / R.

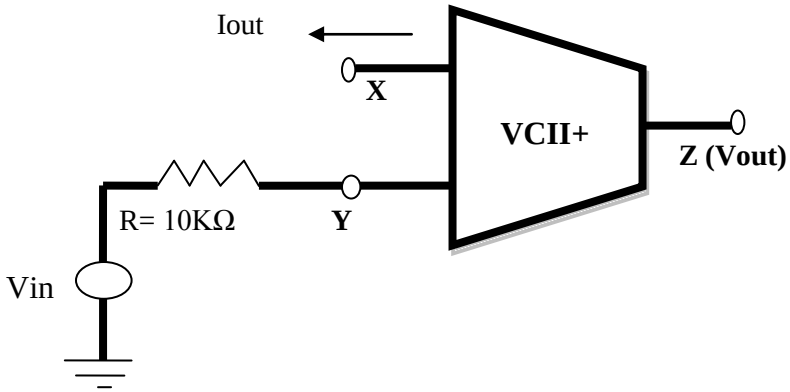

Fig 3.6.1 V to I converter using VCII+

Shown in fig 3.6.2 is a simulation graph for V to I converter. Value of resistance R used is **10KΩ.** Input voltage of 20mvolt is used. And a current of 2mAmp is obtained at the output node which is node X. Current obtained is inverted in nature.

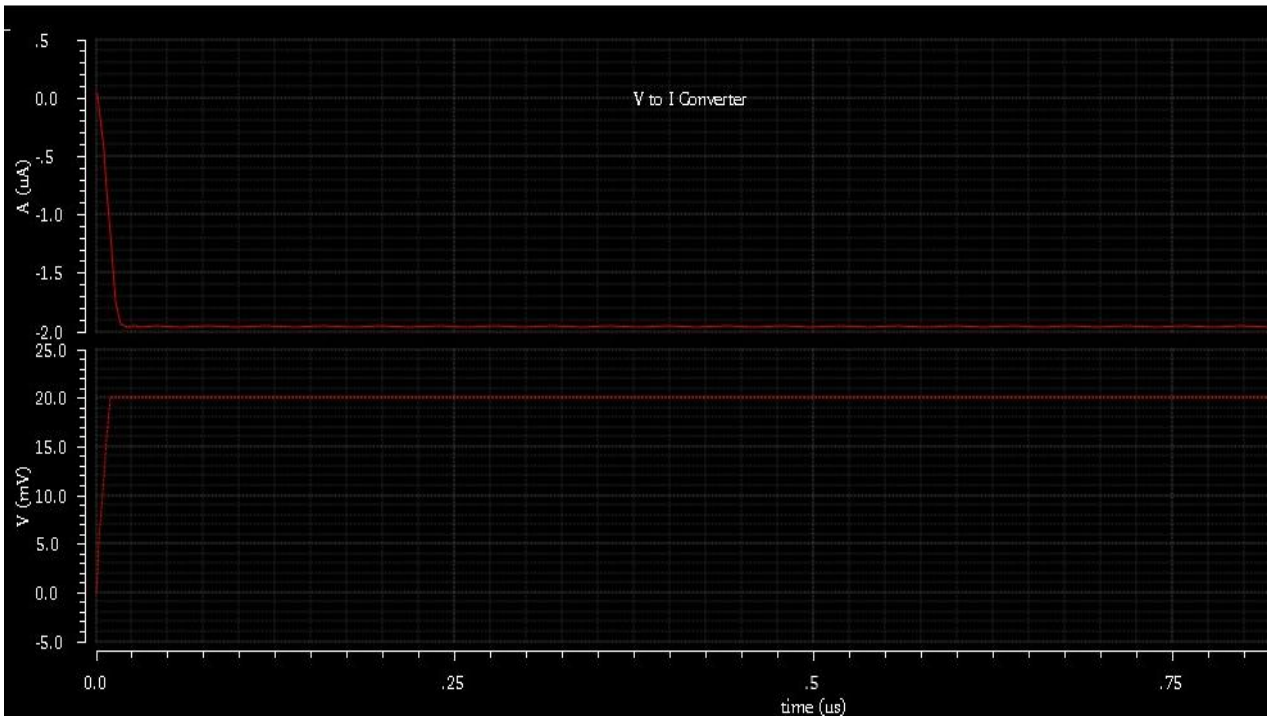

Fig.3.6.2 V to I converter simulated graph

Chapter-4 Conclusion

VCII+ as a analog building block is simulated at 180nm technology node using Cadence Virtuoso. Area is reduced by reducing the technology node from 350nm to 180nm. Static Power Consumption has been also reduced by reducing the voltage source to ±0.9 volt. Characteristics of VCII+ is either improved or it remain as it was earlier in the research paper.

VCII+ block is then used to build applications like Integrator, Differentiator, Voltage Amplifier, V to I convertor, Current Buffer and Voltage Buffer. Using VCII+ in these applications resulted in higher 3dB Bandwidth and less Power consumption. Reducing technology node also improves the delay of the circuit.

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