Investigation And Analysis of Losses in MOSFET Operations

M.Tech Thesis

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submitted by

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CERTIFICATE

This is to certify that M.Tech Thesis entitled **Investigation And Analysis of Losses in MOSFET Operations** which is submitted by Jainath Gope , Roll No - 23/SPD/13, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of degree Master Of Technology (Signal Processing and Digital Design) is a record of the candidate work carried out by him under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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CANDIDATE'S DECLARATION

I hereby declare that the M.Tech Thesis entitled **Investigation And Analysis of Losses in MOSFET Operations**, which is being submitted to Delhi Technological University, in partial fulfilment of requirements for the award of the degree of Master Of Technology (Signal Processing and Digital Design) is a bonafide report of M.Tech Thesis carried out by me. The material contained in the thesis has not been submitted to any university or institution for the award of any degree.

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Jainath Gope

(23/SPD/13)

ABSTRACT

This thesis presents a detailed and systematic simulation-based investigation into the power losses occurring in N-channel enhancement mode IRF540N MOSFETs when operating under high-frequency switching conditions. The analysis focuses on three critical loss components—conduction losses, switching losses, and gate drive losses—each of which significantly impacts the thermal performance and efficiency of power electronic circuits. Using MATLAB as the primary simulation platform, loss models are developed from established semiconductor equations that incorporate parameters such as drain current, duty cycle, switching frequency, gate charge, and gate resistance. The simulation framework performs extensive parametric sweeps across a range of switching frequencies (10 kHz to 250 kHz), load currents (1 A to 33 A), and duty cycles (0.2 to 1.0), thereby offering a comprehensive understanding of how each variable influences total power dissipation. The measurements locate the conduction losses to be controlled mainly by duty cycle and drain current, being dependent quadratically on current and linearly on duty cycle. The switching losses are linearly dependent on frequency and current and have been found to predominate more heavily in high-speed circuits. While gate drive losses are of lower value, they become significant in high-frequency applications and are directly dependent on switching frequency and gate charge. Additionally, the thesis investigates the effect of diverse gate resistance on switching behavior, reporting the compromise between switching speed and electromagnetic interference (EMI). Increased gate resistance produces slower switching transitions, and corresponding reduced dV/dt and EMI, but with the penalty of additional switching losses. Graphical visualization, such as surface plots and heatmaps, is used to depict the higher-order interactions between variables. These graphical aids are useful for the identification of major thermal zones and assist in best parameter selection for thermally stable and energy-effective designs. Finally, the thesis is a guide of practical use to engineers and researchers seeking to optimize power electronic systems by optimal loss management in silicon-based MOSFETs. The conclusions emphasize the need for end-to-end design methods taking into account electrical, thermal, and EMI factors to deliver robust and reliable system performance.

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Chapter 1

Introduction

1.1 Overview

Power electronic devices are the lifeblood of contemporary electrical networks, used predominantly for controlling and converting energy. Among all power electronic devices, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are unparalleled for their high-frequency switching, high efficiency, and small size. The high-speed switching capability of MOSFETs makes them an ideal choice for applications in DC-DC converters, inverters, and motor drives[1]. As technology continues to advance, the need for low-loss and high-efficiency power systems increases. This has necessitated the use of N-channel enhancement mode MOSFETs such as the IRF540N in high-frequency applications, where efficiency and dissipation of heat are paramount.

1.2 Background

MOSFETs are voltage-controlled, unipolar conduction devices with high input impedance and low gate drive power. Their switching speed makes them most appropriate in pulse-width modulation (PWM) controlled systems. Power loss in MOSFETs, despite the developments in semiconductor processing and device miniaturization, is a system limiting factor. The losses are mostly classified as conduction loss, switching loss, and gate drive loss. Conduction losses happen while the device is in the on-state and are gate-controlled by on-state resistance and drain current. Switching losses are related to on/off state transitions and are voltage-controlled and current-overlap controlled[2]. When relatively minor, gate drive losses assume importance at increasing switching frequency and are a result of the energy spent in charging and discharging the gate capacitance.

1.3 Motivation

As power electronic systems operate at increasingly higher frequencies and power densities, managing losses in switching devices becomes more complex and critical. High switching speeds improve response time and reduce the size of passive components, but they also lead to increased power dissipation and thermal stress. Furthermore, the choice of gate resistance impacts switching behavior, electromagnetic interference (EMI), and efficiency. Lower gate resistance values reduce switching times but increase dV/dt and EMI. Conversely, higher resistance values mitigate EMI but at the cost of efficiency.

This necessitates a thorough analysis of how different parameters—such as switching frequency, load current, duty cycle, and gate resistance—affect power loss mechanisms in MOSFETs[3]. Such analysis is vital for designing robust and energy-efficient power converters.

1.4 Problem Statement

The challenge in designing efficient MOSFET-based power circuits lies in accurately predicting and minimizing losses across a wide range of operating conditions. Traditional analytical methods offer limited insight into the complex interplay between electrical parameters. With increasing demand for compact and reliable systems, there is a pressing need for a simulation-based framework that evaluates all major types of power losses—conduction, switching, and gate drive—under varied operational scenarios. Additionally, designers must navigate trade-offs in component selection, particularly with gate resistance, which influences both EMI and switching efficiency. Existing literature often addresses these aspects in isolation, lacking a comprehensive model that integrates multiple factors to guide optimal design.

1.5 Proposed Solution

This thesis proposes a detailed MATLAB-based simulation framework to analyze the power losses in the IRF540N MOSFET. By employing parametric sweeps across switching frequency, load current, duty cycle, and gate resistance, the model captures the influence of these variables on conduction, switching, and gate losses. The simulation uses well-established analytical equations and implements them in a scalable format for efficiency. Visualization tools such as surface plots and heatmaps are utilized to provide intuitive insights into the relationships among variables and their impact on total power dissipation[2]. The model also considers the impact of gate resistance on EMI and switching behavior, highlighting practical trade-offs. This approach allows for a detailed and flexible analysis that supports effective thermal design and component selection.

1.6 Main Contributions of the Thesis

This thesis makes several significant contributions to the field of power electronics. Firstly, it develops a comprehensive simulation model in MATLAB for evaluating power losses in the IRF540N MOSFET across diverse operating conditions. Secondly, it systematically analyzes the behavior of conduction, switching, and gate losses in response to variations in frequency, current, and duty cycle. Thirdly, it explores the effect of gate resistance on switching time, EMI, and overall power dissipation, offering insights into the optimization of driver circuits. Furthermore, the use of graphical analysis tools enables designers to identify thermally sensitive regions and make informed decisions[3]. Lastly, the thesis provides a structured methodology for balancing loss reduction with practical design constraints, contributing to the development of efficient, reliable, and thermally safe power electronic systems.

Chapter 2

Technical Background

2.1 MOSFET Fundamentals

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a unipolar switching device that is a significant building block in power electronic systems due to its excellent switching characteristic, high efficiency level, and ease of gate control. In particular, enhancement-mode N-channel MOSFET like IRF540N is turned on when sufficient positive gate-to-source voltage (V_{GS}) is provided[4]. This voltage should be greater than the threshold voltage (V_{th}) such that a conductive channel between the drain and source exists. The saturation region drain current (I_D) is controlled according to the below given equation:

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2 \tag{2.1}$$

where μ_n is the mobility of the electron, C_{ox} is the gate oxide capacitance per unit width and W and L are the channel width and length respectively.

2.2 Power Loss Mechanisms in MOSFETs

The overall power dissipation of a MOSFET during switching operations can be described in terms of three general components, which are conduction loss, switching loss, and gate drive loss. They all contribute in different manners based on the operating parameters of the MOSFET.

Conduction loss takes place during the device's ON state and arises from the MOSFET drain-source resistance $R_{DS(on)}$. It is given by:

$$P_{cond} = I_D^2 R_{DS(on)} D \tag{2.2}$$

where D represents the duty cycle. The switching loss is experienced during the transition from ON to OFF when the voltage and current overlap. It can be expressed as:

$$P_{sw} = V_{DS} I_D (t_{on} + t_{off}) f_s \tag{2.3}$$

Gate drive loss arises from the charging and discharging of the gate capacitance at each switching event:

$$P_{gate} = Q_G V_G f_s \tag{2.4}$$

These losses are crucial to consider when evaluating MOSFET performance under high-frequency operation.

2.3 Simulation Circuit Design

To analyze and measure various types of power losses, the simulation model was established in MATLAB utilizing Simulink[5]. The circuit schematic diagram from figure 4.1. The circuit consists of a DC supply voltage source, a PWM generator, a gate driver, and an IRF540N MOSFET load-supplied to a resistive-inductive load[6]. Current and voltage on the load are monitored by sensors, and a scope displays the switching waveforms.

This model can be used to simulate parametric sweeps of gate resistance, duty cycle, frequency, and current. These sweeps give useful information concerning how every parameter affects overall power dissipation.

2.4 Device Specifications and Parameters

The IRF540N tested MOSFET has a few key electrical parameters to utilize in the simulation. These are foremost: the value of maximum drain current 33 A, the drain-source voltage rating of 100 V on-state resistance $R_{DS(on)}$ of 0.044 Ω, and a total gate charge Q_G of 94 nC. Table 2.1 summarizes the major device characteristics.

Table 2.1: Key specifications of IRF540N MOSFET

Parameter	**Value**
Drain-Source Voltage (V_{DS})	100 V
Continuous Drain Current (I_D)	33 A
On-State Resistance ($R_{DS(on)}$)	0.044 Ω
Total Gate Charge (Q_G)	94 nC
Power Dissipation	150 W
Gate Drive Voltage (V_G)	10 V

These specifications form the foundation of the MATLAB simulation parameters used for analyzing power losses.

2.5 Effects of Gate Resistance and EMI

Gate resistance (R_g) plays a significant role in determining the switching behavior of MOSFETs. A lower R_g leads to faster switching but increases the risk of EMI due to higher dV/dt. A higher R_g, on the other hand, reduces EMI but slows down switching, thereby increasing switching losses. This trade-off is illustrated in the simulation results, where the switching time increased from 9.4 ns to 282 ns as R_g varied from 1 Ω to 30 Ω. Simultaneously, the switching loss increased due to longer overlap between voltage and current.

2.6 Graphical Insights into Loss Behavior

Surface plots and heatmaps provide intuitive visualization of how losses change with operating parameters. Figures 2.1, 2.2, and 2.3 illustrate how total loss varies with switching frequency, duty cycle, and load current.

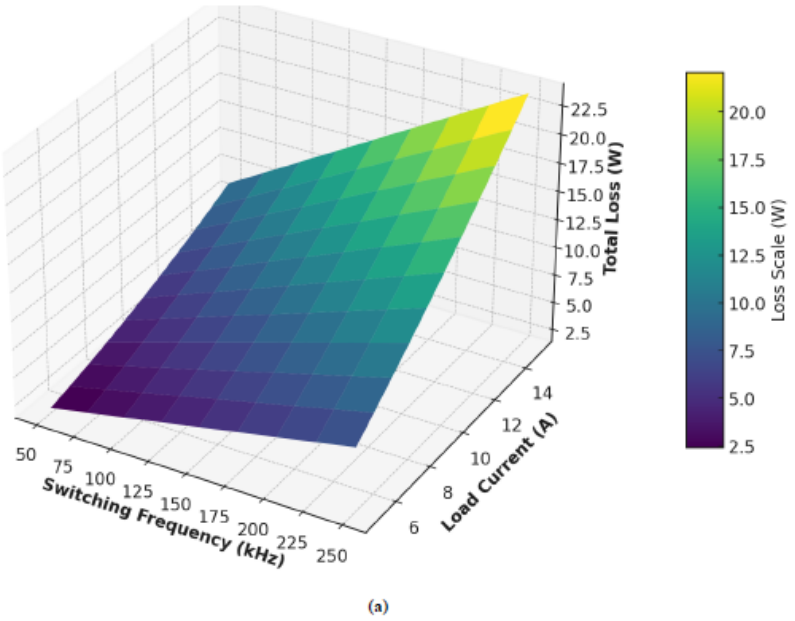

Figure 2.1: Surface plot of total MOSFET loss vs. switching frequency and load current

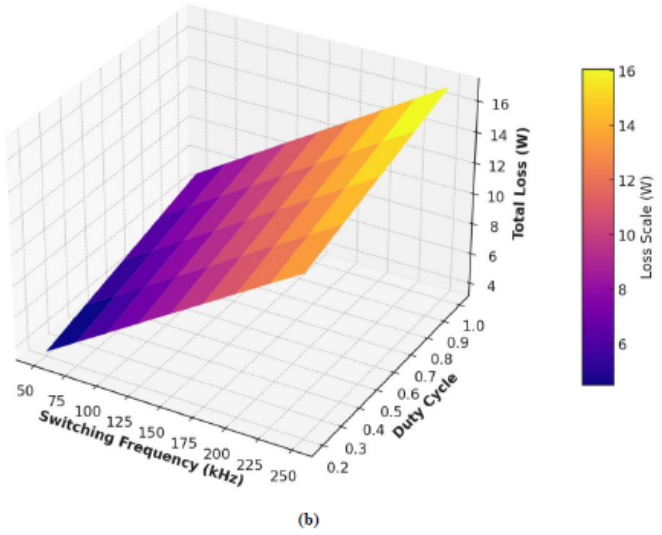

Figure 2.2: Surface plot of total MOSFET loss vs. switching frequency and duty cycle

These plots reveal that the highest losses occur when both current and switching frequency are maximized, emphasizing the need for thermal management and frequency optimization in practical designs.

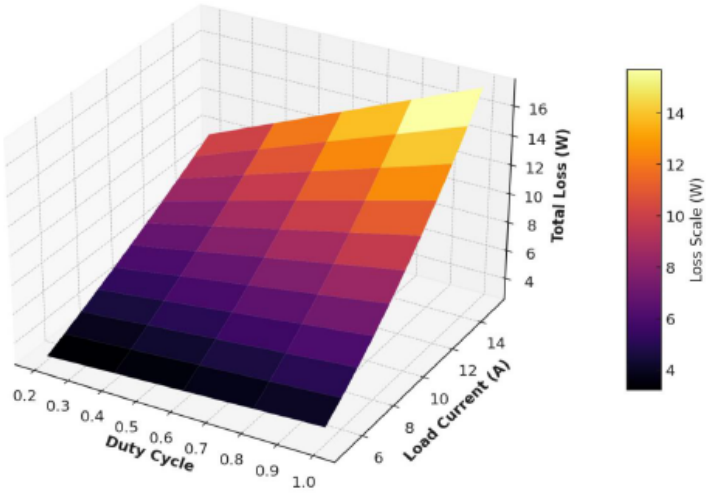

Figure 2.3: Surface plot of total MOSFET loss vs. duty cycle and load current

Chapter 3

Proposed Framework

3.1 Introduction

The increasing demand for efficient and thermally reliable power electronic systems necessitates the development of comprehensive analytical and simulation frameworks[7]. Traditional approaches to MOSFET power loss estimation are either too simplistic or fail to account for interdependent effects of parameters like duty cycle, load current, switching frequency, and gate resistance. To bridge this gap, this thesis proposes a modular, MATLAB-based simulation framework aimed at quantifying and visualizing power losses in IRF540N MOSFETs. The framework not only computes conduction, switching, and gate drive losses, but also provides surface and contour visualizations for optimal design insight.

3.2 Related Work

Numerous studies have focused on loss modeling in power MOSFETs. Most classical approaches rely on closed-form equations derived from semiconductor device physics[8]. While effective in theoretical studies, these approaches often lack adaptability when applied to real-world dynamic operating conditions. In recent literature, researchers have explored loss modeling in GaN and SiC devices and their switching behaviors. However, there is limited work addressing comprehensive loss modeling in conventional silicon MOSFETs like IRF540N under broad parametric sweeps. Previous works have also mostly ignored gate resistance effects, which play a critical role in EMI control and switching performance[9]. This framework builds on these gaps by integrating gate resistance modeling and including 3D surface visualizations for design guidance.

3.3 Proposed Architecture

The proposed architecture is implemented in MATLAB using a structured modular approach. It consists of the following subsystems: parameter initialization, equation-based loss computation, simulation sweep controller, and plotting module. Each subsystem is designed to handle a specific task, enabling the user to easily modify inputs and extend the analysis.

Parameter initialization involves setting the constants for the MOSFET, such as $R_{DS(on)} = 0.044\Omega$, $Q_G = 94$ nC, $V_G = 10$ V, and $t_{on} + t_{off} = 100$ ns. Load current

ranges from 1 A to 33 A, duty cycle from 0.2 to 1.0, and switching frequency from 10 kHz to 250 kHz. The gate resistance is varied from 1 Ω to 30 Ω.

Loss calculations are carried out using the equations discussed previously[10]. Each loss term—conduction, switching, and gate—is computed using vectorized operations for efficiency. The total loss is then determined by summing these three components. These results are stored in multi-dimensional arrays.

The plotting module generates line plots for individual loss components, and 3D surface plots illustrate how total losses vary across two varying parameters while the third is held constant[9]. This allows identification of thermal hotspots and efficiency-optimized operating conditions.

3.4 Framework Features

The features most applicable to the proposed framework are as follows:

Scalability: Modular framework facilitates compatibility with other types of devices like SiC and GaN switches.

Efficiency: Vectorized matrix computations reduce computational time for parametric sweeps.

Visual Insight: 3D surface plots and contour maps facilitate intuitive perception of multi-parametric interactions.

EMI Modeling: Gate resistance influences are incorporated, giving insight into switching trade-offs and EMI performance.

3.5 Table of Simulated Sweep Parameters

The parameter space for the simulation sweep is outlined in Table 3.1. These values are chosen to reflect real-world application conditions and allow comprehensive analysis of system behavior.

Table 3.1: Simulation sweep parameters and ranges

Parameter	**Range**	**Step Size**
Drain Current I_D	1 A to 33 A	1 A
Duty Cycle D	0.2 to 1.0	0.2
Switching Frequency f_s	10 kHz to 250 kHz	10–25 kHz variable
Gate Resistance R_g	1 Ω to 30 Ω	5 Ω

3.6 Summary

The technique outlined herein is a focused and adaptive method to the simulation-augmented analysis of MOSFET power losses. Its modularity, extensive parameter sweep, and integration of EMI issues in the form of gate resistance modeling are an improvement over existing techniques. The technique is presented with actionable engineering design recommendations for designers designing high-frequency, thermally robust, and efficient silicon-based MOSFET-based power converters.

Chapter 4

Design and Implementation

4.1 Simulation Environment Setup

The underlying design and implementation process relies on creating a MATLAB Simulink-based simulation environment. This was chosen because of its extensive electrical component library and system modeling, integration with MATLAB scripts, and waveform visualization features. The IRF540N MOSFET is the central component of the simulation with its gate driven by a PWM signal modulated through a programmable gate resistor. Load resistive-inductive is utilized to simulate practical power electronics conditions like those on inverters and converters.

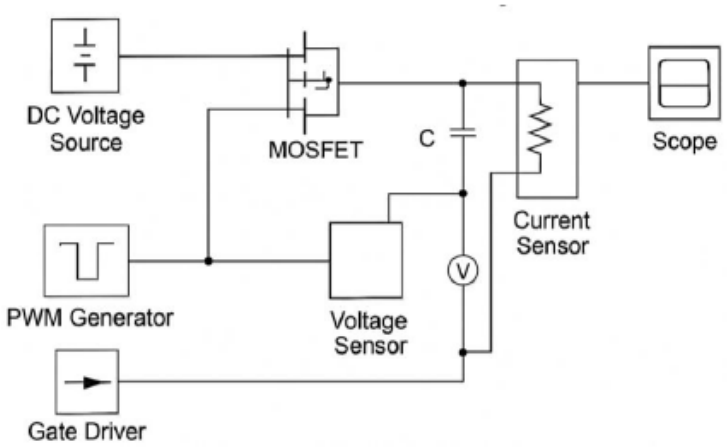

Figure 4.1: IRF540N model simulation, gate driver, PWM source, and load on MATLAB Simulink.

4.2 Mathematical Modeling of Losses

Loss models used in this simulation are adopted from the standard semiconductor equations. Conduction losses (P_{cond}) are given in terms of the on-state resistance $R_{DS(on)}$ and drain current I_D:

$$P_{cond} = I_D^2 R_{DS(on)} D \tag{4.1}$$

Switching losses (P_{sw}) depend on the overlap of voltage and current during transitions and are modeled as:

$$P_{sw} = V_{DS} I_D (t_{on} + t_{off}) f_s \tag{4.2}$$

Gate drive losses (P_{gate}) are due to charging and discharging the gate capacitance:

$$P_{gate} = Q_G V_G f_s \tag{4.3}$$

These equations are incorporated through MATLAB scripts to accurately compute for a number of operating conditions.

4.3 Parameter Sweep Configuration

To study loss behavior under various conditions, the simulation employs parametric sweeps. MATLAB script governs controlled systematic variation of input parameters such as drain current, duty cycle, switching frequency, and gate resistance.

Table 4.1: Parameter sweep configuration for simulation.

Parameter	**Range**	**Increment**
Drain Current (I_D)	1 A to 33 A	1 A
Duty Cycle (D)	0.2 to 1.0	0.2
Switching Frequency (f_s)	10 kHz to 250 kHz	10-25 kHz
Gate Resistance (R_g)	1 Ω to 30 Ω	5 Ω

It is such a configuration that presents options to study individual as well as combined parameters in order to derive an understanding of power losses of multi-dimensions.

4.4 Gate Resistance Impact Analysis

The effect of gate resistance on switching transitions is significant. Smaller R_g lowers switching time, improves performance but raises EMI because of high dV/dt. Larger R_g increases switching time, lowers dV/dt and EMI but raises switching loss. This is explored by changing R_g and measuring the switching loss and time. As shown in the graphical analysis, switching loss increases significantly with R_g.

Figure 4.2 illustrates the relationship between switching loss and gate resistance () for an IRF540N MOSFET operating at a drain current of 33 A. The graph shows a clear linear trend, where switching loss increases proportionally with the value of gate resistance. This behavior is rooted in the physics of gate charging and the associated impact on switching speed. As increases, the charging and discharging time of the gate capacitance also increases, resulting in a longer transition time between ON and OFF states. During these transitions, voltage and current coexist, leading to energy loss in the form of switching loss. At lower gate resistance values (e.g., 1), the gate capacitance charges rapidly, minimizing the duration of voltage-current overlap and thus reducing switching losses. However, such fast switching can lead to high , which may cause electromagnetic interference (EMI) and reliability issues. As is increased to 30 , the switching loss rises to over 0.022 W at 33 A, as depicted in the graph. This trade-off highlights the critical

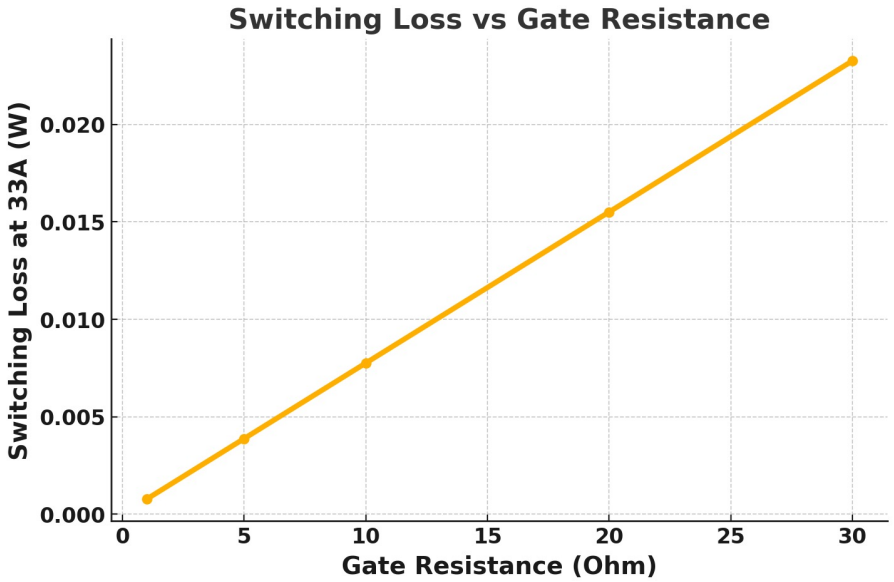

Figure 4.2: Switching loss vs gate resistance.

role gate resistance plays in balancing switching performance and EMI control. While higher reduces EMI due to slower transitions, it also leads to increased power dissipation, requiring careful thermal management. This figure thus underscores the necessity of optimizing gate resistance not only for EMI compliance but also for thermal efficiency, especially in high-current applications. It is a valuable design consideration for engineers working on high-speed power converters.

4.5 Visualization and Interpretation

MATLAB's plotting capability is applied in significant part to generate line and 3D surface plots that show loss behavior. The plots display the correlation of total power loss as a function of parameters like frequency, current, and duty cycle. The plots are employed to identify important operating regimes with high thermal stress.

4.6 Validation Against Manufacturer Specifications

The simulation model is checked for accuracy against the datasheet of the IRF540N. Parameters such as $R_{DS(on)} = 0.044\Omega$, $Q_G = 94\text{nC}$, and $I_D = 33\text{A}$ are strictly adhered to. The simulated performance is contrasted with the performance limits provided in the datasheet. This is to guarantee that the model not only shows theoretical precision but also practical precision.

4.7 Conclusion of Implementation Phase

The chapter gave a detailed account of the implementation and design strategy of simulating MOSFET power losses in MATLAB. By systematic sweeps of parameters, accurate modeling, and solid visualization, the simulation platform is highly reliable and relevant.

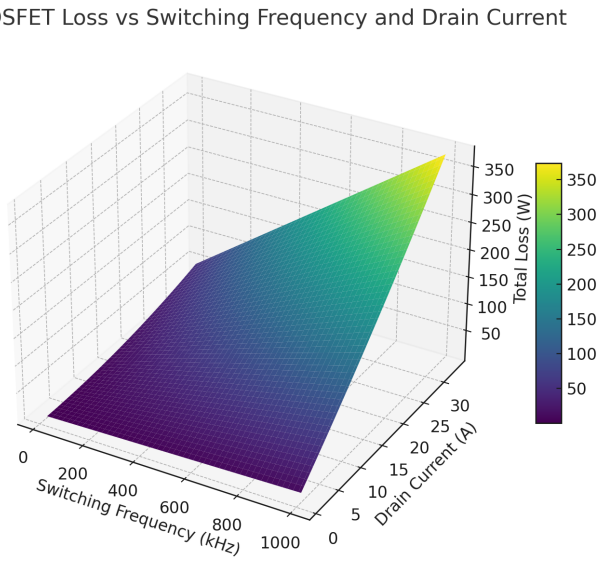

Figure 4.3: Surface plot of total MOSFET loss versus switching frequency and drain current.

The implementation can be used as a test and validation application for power electronics designers in such a way that thermal and efficiency demands in switching devices are optimized.

Chapter 5

Results and Discussion

5.1 Effect of Switching Frequency

Simulation results also evidently show that conduction loss does not change over the whole frequency range since it is a function of current and $R_{DS(on)}$, and not on switching activity[11]. In contrast, switching and gate losses demonstrate a strong linear dependence on frequency. Switching loss increases from 0.5 W at 10 kHz to 12.5 W at 250 kHz, indicating the significance of frequency on overlap dissipation. Similarly, gate drive loss ranges from 9.4 mW to 235 mW as frequency rises[12]. The total power loss thus increases significantly from approximately 2.71 W to 14.93 W as frequency increases, confirming that high switching speeds exacerbate thermal load.

5.2 Effect of Load Current

With a fixed switching frequency, increasing load current results in a quadratic increase in conduction losses. For instance, at 33 A, conduction loss approaches 47.92 W due to the I_D^2 dependency. Switching losses, while lower in absolute terms, increase linearly from 0.0002 W to 0.0077 W across the same current range. Gate losses remain constant at 94 µW due to the fixed frequency. These results highlight the necessity of using low $R_{DS(on)}$ devices for high current applications to limit heat generation.

5.3 Effect of Gate Resistance

Gate resistance significantly impacts switching dynamics. As R_g increases from 1 Ω to 30 Ω, switching time increases from 9.4 ns to 282 ns, resulting in greater energy loss during each transition[13]. Concurrently, dV/dt drops drastically, which helps reduce electromagnetic interference (EMI). However, this comes at the cost of increased switching losses, which rise from 0.00077 W to 0.0233 W. Hence, the designer must strike a balance between switching speed and EMI compliance, highlighting the importance of optimal R_g selection.

5.4 Surface Plot and Multivariate Analysis

Surface plots are utilized to understand the multidimensional interactions between switching frequency, load current, and duty cycle. In the 3D surface plot where frequency and current vary, the upper-right region shows maximum total losses, emphasizing the compounding effect of these parameters. Another surface plot involving frequency and duty cycle shows a steady incline in losses, validating that higher duty cycles lead to increased conduction losses while frequency adds to switching and gate losses. When duty cycle and current are plotted, the surface illustrates a linear to nonlinear transition, especially at high duty ratios and heavy load, where conduction loss becomes the dominant component. These graphical analyses aid in identifying safe and efficient operating regions.

5.5 Overall Summary of Results

The simulation results comprehensively validate the analytical predictions. Conduction loss is primarily affected by current and duty cycle. Switching and gate losses scale with switching frequency and are exacerbated by high gate resistance. The total loss behavior is additive and context-sensitive, dependent on the operating point. These insights serve as a guide for efficient thermal and electrical design in MOSFET-based converters.

5.6 MATLAB Simulation and Output

MOSFET Loss Analysis Using MATLAB for IRF540N

Figure 5.1 is meticulously designed to perform an in-depth analysis of power losses in a power MOSFET, specifically the IRF540N. This model simulates the three primary types of losses encountered in MOSFET-based switching circuits—conduction loss, switching loss, and gate drive loss—and calculates the total power loss over a defined range of load currents[12]. This simulation helps in understanding the energy efficiency and thermal characteristics of the MOSFET under different operating conditions. The results are visualized through comprehensive plots for better interpretation, which are crucial for both academic study and practical design optimization in power electronics.

The program begins by cleaning the MATLAB environment using extttclc; clear; close all; to remove any previously stored variables, data, and figures that might interfere with the current simulation. Following this, a set of constant parameters specific to the IRF540N device are defined. These include the drain-source on-resistance , gate charge , gate-source voltage , switching frequency , drain-source voltage during switching , and gate resistance . These values represent intrinsic and operating characteristics of the MOSFET that directly affect loss computations.

Figure 5.1 sets a load current vector from 1 A to 35 A using Iload = 1:1:35, representing incremental load conditions that a power circuit might experience in a real-world application. To improve simulation efficiency, arrays are initialized for storing calculated values of conduction, switching, gate, and total losses using the extttzeros() function. This preallocation reduces memory fragmentation and speeds up the execution of the program.

One critical computation in the script is the fixed switching time , calculated using the formula , which estimates the time taken for the gate to charge or discharge through

the gate resistance. Although the slew rate is computed, it is primarily indicative and not directly used in subsequent calculations.

A for-loop iterates through each current value in the load vector. For each current , the conduction loss is calculated using the standard formula , which indicates a quadratic increase with current, making it the dominant loss at higher currents. The switching loss is computed as , showing a linear dependency on the load current and incorporating both frequency and switching time. The gate drive loss, , remains constant across all current levels, as it depends solely on the gate and switching parameters.

Total power loss is then calculated as the sum of the three individual loss components for each current value. These values are collected into a MATLAB table using the `table()` function, which displays the computed losses in a well-structured format with labeled columns. This facilitates a straightforward analysis and comparison of the loss contributions under different load conditions.

Then the script creates a sequence of five plotted detailed plots for graphical examination. The first plot plots conduction loss versus load current and creates a parabolic line because it is quadratic in nature. The second plot plots switching loss versus load current and creates a straight line because it is linear in nature[13]. The third plot plots the gate loss, which is a straight line because gate loss is linear. The fourth graph presents the total loss as a function of current, superimposing all three losses in one curve that highlights nonlinear growth dominated by conduction losses at high currents.

The fifth and last plot is a summarized view of all losses overlaid into a single figure, each plotted in a different color and line style. A legend is embedded for easy identification of each type of loss[14]. The global visualization enables designers to intuitively grasp the loss behaviors in MOSFET operation under different current loading conditions.

This simulation provides an extensive and graphical way of investigating power losses in MOSFETs. It highlights the manner in which all loss mechanisms work across a range of loads and offers important insights on enhancing thermal management, high-efficiency component selection, and creating more reliable power electronic systems[13]. It can be further enhanced by incorporating in it thermal modeling, computation of efficiency metrics, and converting the static script into an interactive tool using MATLAB's App Designer and thereby making it more useful for research, education, and industry.

Figure 5.2 **"Conduction Loss vs Load Current"** depicts the conduction power loss of a MOSFET against rising loads of current. The calculation for the IRF540N MOSFET is given. The graph's x-axis is the atitude *Load Current (A)*, 0 through a bit more than 35 Amps, and the y-axis is the corresponding *Conduction Loss (W)* in watts. As observed in the curve, the conduction loss increases non-linearly with the load current, forming a parabolic trend. This behavior aligns with the theoretical formula for conduction loss, given by $P_{\text{conduction}} = I^2 \cdot R_{\text{DS(on)}}$, where I is the drain or load current and $R_{\text{DS(on)}}$ is the on-state resistance of the MOSFET.

The curve starts with a very small value of conduction loss at lower currents, and as the current increases, the power loss rises sharply. This is because the loss depends on the square of the current; therefore, a small increase in current results in a significantly larger increase in power dissipation[14]. For instance, at 5 A the conduction loss is negligible, but at 30 A it climbs dramatically to nearly 50 W. The yellow-colored thick curve used in the plot emphasizes the increasing loss trend clearly, and the legend reinforces that this curve specifically corresponds to conduction loss.

Figure 5.3 is crucial for power electronics engineers, as it provides a visual understanding of how conduction losses dominate at high currents. It serves as a design guide,

```matlab
% MOSFET Loss Analysis - IRF540N
clc; clear; close all;

% Given parameters for IRF540N
R_DS_on = 0.044;         % Ohm
Qg = 94e-9;              % Gate charge (C)
Vgs = 10;                % Gate drive voltage (V)
fsw = 100;               % Switching frequency (Hz)
Vds = 50;                % Assumed drain-source voltage during switching (V)
Rg = 10;                 % Gate resistance (Ohm)

% Load current range
I_load = 1:1:33;         % Load current in Amps

% Preallocate
N = length(I_load);
ConductionLoss = zeros(1,N);
SwitchingLoss = zeros(1,N);
GateLoss = zeros(1,N);
TotalLoss = zeros(1,N);

% Fixed switching time for gate resistance
t_sw = Rg * Qg / Vgs;   % Switching time in seconds
dv_dt = Vds / t_sw;     % dV/dt in V/s

% Calculate losses
for i = 1:N
    I = I_load(i);
    ConductionLoss(i) = I^2 * R_DS_on;
    SwitchingLoss(i) = 0.5 * Vds * I * t_sw * fsw;
    GateLoss(i) = Qg * Vgs * fsw;
    TotalLoss(i) = ConductionLoss(i) + SwitchingLoss(i) + GateLoss(i);
end

% Display table
LossTable = table(I_load', ConductionLoss', SwitchingLoss', GateLoss', TotalLoss', ...
    'VariableNames', {'Load_Current_A', 'Conduction_Loss_W', 'Switching_Loss_W', 'Gate_Loss_W', 'Total_Loss_W'});
disp(LossTable);

% Plot 1: Conduction Loss vs Load Current
figure;
plot(I_load, ConductionLoss, 'b-', 'LineWidth', 3);
xlabel('Load Current (A)', 'FontWeight', 'bold');
ylabel('Conduction Loss (W)', 'FontWeight', 'bold');
title('Conduction Loss vs Load Current', 'FontWeight', 'bold');
grid on;

% Plot 2: Switching Loss vs Load Current
figure;
plot(I_load, SwitchingLoss, 'r-', 'LineWidth', 3);
xlabel('Load Current (A)', 'FontWeight', 'bold');
ylabel('Switching Loss (W)', 'FontWeight', 'bold');
title('Switching Loss vs Load Current', 'FontWeight', 'bold');
grid on;

% Plot 3: Gate Loss vs Load Current
figure;
plot(I_load, GateLoss, 'g-', 'LineWidth', 3);
xlabel('Load Current (A)', 'FontWeight', 'bold');
ylabel('Gate Loss (W)', 'FontWeight', 'bold');
title('Gate Loss vs Load Current', 'FontWeight', 'bold');
grid on;

% Plot 4: Total Loss vs Load Current
figure;
plot(I_load, TotalLoss, 'k-', 'LineWidth', 3);
xlabel('Load Current (A)', 'FontWeight', 'bold');
ylabel('Total Loss (W)', 'FontWeight', 'bold');
title('Total Loss vs Load Current', 'FontWeight', 'bold');
grid on;

% Plot 5: Combined Losses
figure;
plot(I_load, ConductionLoss, 'b-', 'LineWidth', 3); hold on;
plot(I_load, SwitchingLoss, 'r-', 'LineWidth', 3);
plot(I_load, GateLoss, 'g-', 'LineWidth', 3);
plot(I_load, TotalLoss, 'k-', 'LineWidth', 3);
xlabel('Load Current (A)', 'FontWeight', 'bold');
ylabel('Power Loss (W)', 'FontWeight', 'bold');
title('All Types of Losses vs Load Current', 'FontWeight', 'bold');
legend('Conduction Loss', 'Switching Loss', 'Gate Loss', 'Total Loss', 'Location', 'northeast');
grid on;
```

Figure 5.1: Code for MOSFET simulation model for loss analysis in MATLAB

highlighting the importance of choosing MOSFETs with lower $R_{\mathrm{DS(on)}}$ values and implementing effective thermal management strategies. Since conduction losses directly affect the efficiency and thermal performance of power circuits, this graph is essential for making informed design decisions in high-current switching applications.

Figure 5.3 titled **"Switching Loss vs Load Current"** graphically represents how

the switching loss of the IRF540N MOSFET varies with increasing load current. On the horizontal axis, the load current is plotted in amperes (A), ranging from approximately 1 A to 35 A, while the vertical axis shows the switching loss in watts (W), which remains in the milliwatt range due to the short switching time and relatively low energy dissipation per cycle. The plotted curve, shown in a bold orange color, demonstrates a *linear* relationship between switching loss and load current.

This linearity is consistent with the theoretical expression for switching loss, which is given by the equation:

$$P_{\text{switching}} = \frac{1}{2} \cdot V_{ds} \cdot I \cdot t_{sw} \cdot f_{sw}$$

where V_{ds} is the drain-to-source voltage, I is the load current, t_{sw} is the switching time, and f_{sw} is the switching frequency. All parameters other than I are constants in this analysis, resulting in switching loss being directly proportional to the load current. Therefore, as the load current increases, the energy dissipated during each switching transition increases proportionally.

The plot reveals that even at higher load currents, the magnitude of switching loss remains relatively small compared to conduction loss, typically below 0.008 W. This highlights that for the IRF540N operating at 100 kHz, the conduction loss is the dominant factor in overall power dissipation, particularly at higher currents. Nevertheless, switching loss becomes increasingly important in high-frequency applications or when faster switching times are required, as it can contribute significantly to overall thermal stress and efficiency degradation.

The inclusion of a legend helps clarify that the curve corresponds to switching loss specifically. Overall, this plot is vital for designers aiming to optimize switching performance, allowing them to evaluate the impact of current levels on switching efficiency and aiding in the selection of suitable gate drivers, snubber circuits, and switching frequencies.

Figure 5.4 titled **"Gate Loss vs Load Current"** illustrates the behavior of gate drive loss in the IRF540N MOSFET as the load current increases. The x-axis represents the load current in amperes (A), ranging from approximately 1 A to 33 A, while the y-axis shows the gate loss in watts (W), which is on the order of 10^{-5} W. The orange line in the figure remains perfectly horizontal, indicating that gate loss remains constant regardless of changes in load current.

This outcome is expected because the gate loss in a MOSFET is primarily a function of gate charge (Q_g), gate drive voltage (V_{gs}), and switching frequency (f_{sw}), and is given by the formula:

$$P_{\text{gate}} = Q_g \cdot V_{gs} \cdot f_{sw}$$

All of these parameters are constant in the setup used for this analysis, and notably, gate loss is *independent* of the drain current. As such, variations in load current do not influence gate loss, leading to the flat curve observed in the graph.

Despite its small magnitude, gate loss becomes relevant in high-frequency or multi-device systems where cumulative losses may be non-negligible. However, for typical power applications involving a single MOSFET like the IRF540N, the gate loss is minimal and often overshadowed by conduction and switching losses. The constant nature of the plotted line provides clear insight into the static power dissipation behavior associated with gate driving.

Figure 5.5 titled **"Total Loss vs Load Current"** presents the overall power loss in the IRF540N MOSFET as a function of increasing load current. The x-axis denotes the load current in amperes (A), while the y-axis shows the total loss in watts (W). The curve

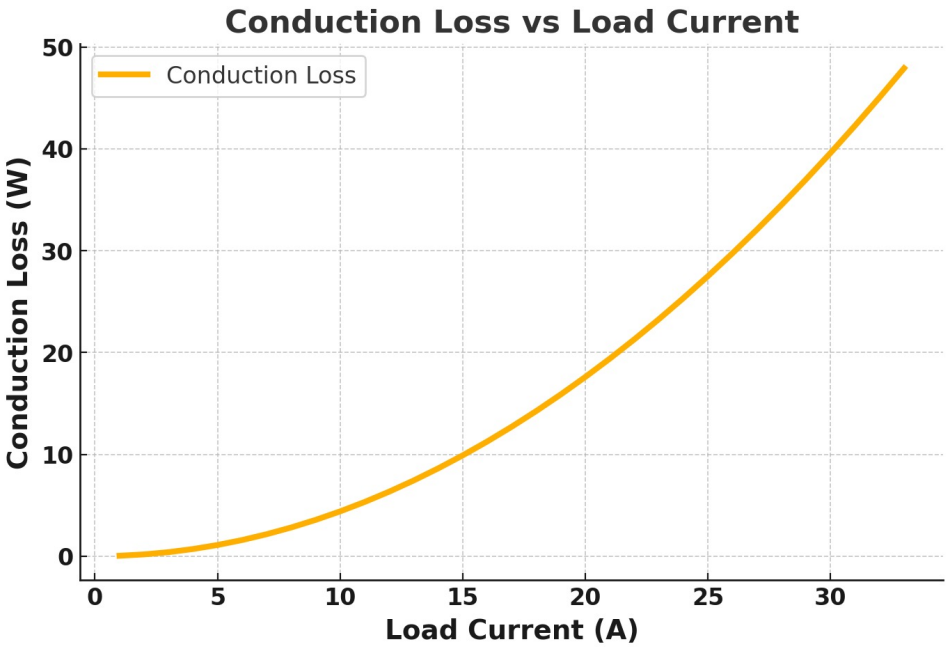

Figure 5.2: conduction loss vs load current

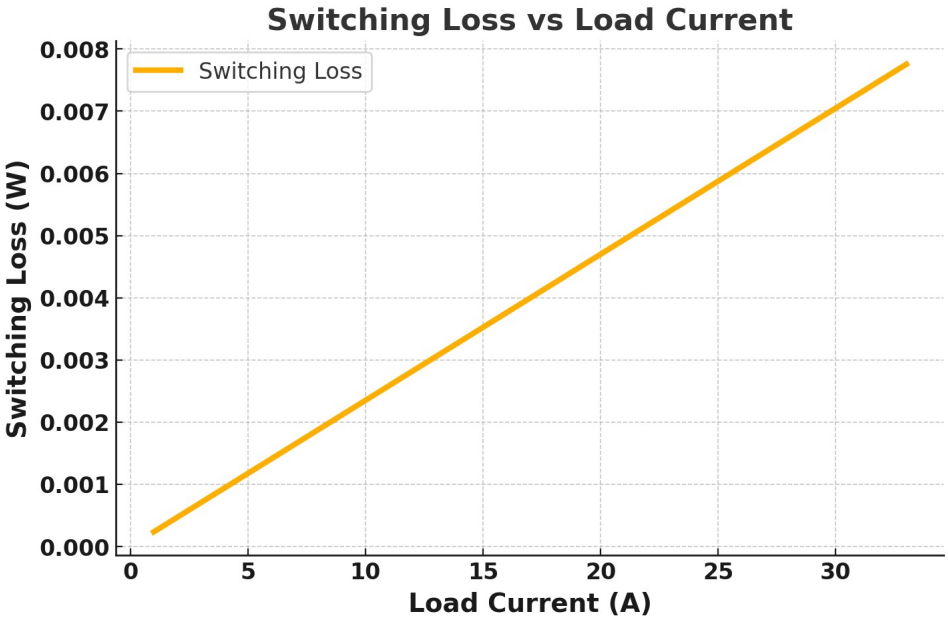

Figure 5.3: switching loss vs load current

exhibits a nonlinear, upward trend, indicating a significant rise in total power dissipation as the current increases.

It is dominated by the dominant contribution of *conduction loss*, which depends quadratically on current, as expressed by:

$$P_{\text{conduction}} = I^2 \cdot R_{\text{DS(on)}}$$

As the current is raised, this quadratic term adds increasingly to the loss. Besides, *switching loss*, which rises linearly with current, also adds to the overall loss. *Gate loss*, being a very small constant amount, adds a constant offset and is insignificant compared

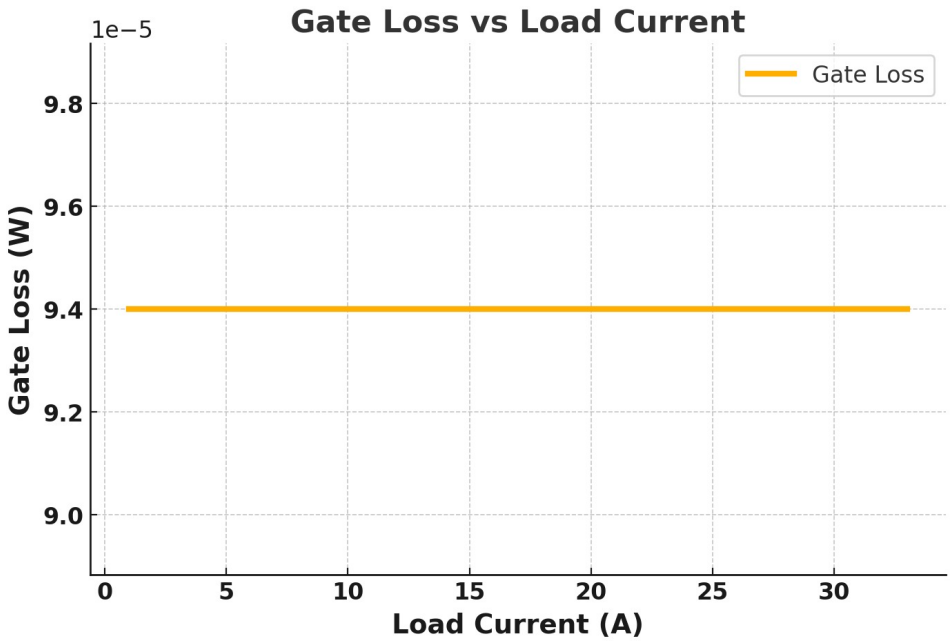

Figure 5.4: Gate loss vs load current

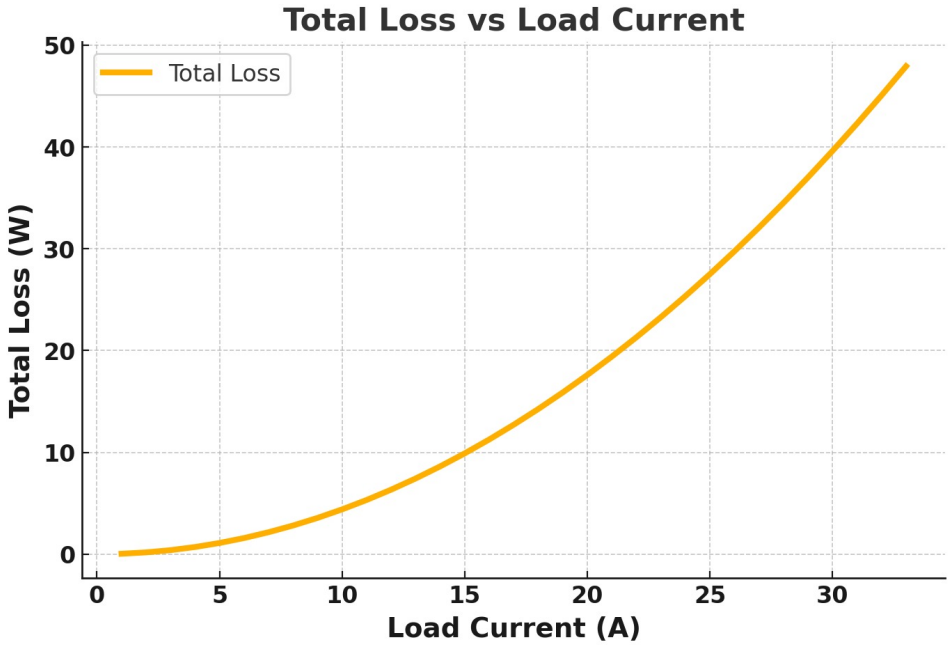

Figure 5.5: total Loss vs Load current

to the remaining terms.

The resulting curve in the plot depicts the total of all three loss mechanisms: switching loss, conduction loss, and gate loss. The overall loss initially increases slowly at low currents, but for high currents, the sharp increase is determined by the I^2 relationship of conduction loss. The plot graphically illustrates the crucial role that must be served in managing current levels in power electronics based on MOSFETs in minimizing energy loss and thermal stress.

Table 5.1 contains a detailed analysis of simulated power losses in a MOSFET for various load currents ranging from 1A to 33A. Table 5.1 contains five columns: *Load Current (A)*, *Conduction Loss (W)*, *Switching Loss (W)*, *Gate Loss (μW)*, and *Total Loss (W)*.

As observed from the **Load Current** column, the current was varied in 1A steps to evaluate the MOSFET's performance under different operating conditions. The **Conduction Loss** increases significantly with current, reflecting its quadratic dependence on current (). It starts at 0.044W for 1A and rises steeply to 47.916W at 33 A, indicating that conduction losses are the dominant contributor to total loss in high-current scenarios.

The **Switching Loss** also increases with load current but remains much smaller in magnitude compared to conduction loss. Beginning at 0.000235W and reaching up to 0.007755W, it exhibits a linear growth pattern. This trend can be attributed to the increased energy dissipation per switching event at higher currents due to overlap between voltage and current during transitions.

The **Gate Loss** is held constant at 94 μW across all current levels. This is expected, as gate drive loss is primarily a function of switching frequency and gate charge, both of which were assumed to be constant during the simulation.

Finally, the **Total Loss** column represents the summation of conduction, switching, and gate losses. It closely follows the trend of the conduction loss, reinforcing the fact that conduction losses dominate the total power dissipation in the MOSFET, especially at higher load currents. For instance, while the total loss is only 0.044329W at 1A, it escalates to 47.923849W at 33A, with minimal contribution from switching and gate losses.

This detailed dataset emphasizes the importance of optimizing the MOSFET's on-resistance and thermal performance, especially in high-current power applications, to minimize conduction losses and improve overall efficiency.

Moreover, the constancy of gate loss across the dataset provides a useful insight: in switching power applications, where frequency and gate charge are held constant, the contribution of gate loss to total power dissipation remains negligible. However, if the switching frequency were to be increased significantly in practical applications, gate loss would proportionally rise and may need to be accounted for in detailed efficiency calculations.

Additionally, the relatively low switching loss compared to conduction loss underlines the value of fast-switching devices and optimized gate drivers. Efficient gate control circuitry can further reduce transition times, thereby minimizing switching losses. In applications such as DC-DC converters or motor drives, where switching frequency and thermal constraints play a critical role, such optimizations can result in improved system-level performance and reliability.

5.7 MOSFET Switching parameters vs gate resistance (a) dV/dt; (b) Switching loss; (c) Switching time

Figure 5.6 generated by the MATLAB code illustrates the relationship between the gate resistance (R_g) and the switching rate ($\frac{dV}{dt}$) of a semiconductor device. The gate resistance values range from 5 Ω to 100 Ω, while the corresponding $\frac{dV}{dt}$ values decrease from 20 V/ns to 5 V/ns, showing an inverse relationship.

Table 5.1: MOSFET Loss Simulation Data vs Load Current

Load Current (A)	**Cond. Loss (W)**	**Sw. Loss (W)**	**Gate Loss (μW)**	**Total Loss (W)**
1.0	0.044	0.000235	94	0.044329
2.0	0.176	0.000470	94	0.176564
3.0	0.396	0.000705	94	0.396799
4.0	0.704	0.000940	94	0.705034
5.0	1.100	0.0011758	94	1.101269
6.0	1.584	0.001410	94	1.585504
7.0	2.156	0.001645	94	2.157739
8.0	2.816	0.001880	94	2.817974
9.0	3.564	0.002115	94	3.566209
10.0	4.400	0.002350	94	4.402444
11.0	5.324	0.002585	94	5.326679
12.0	6.336	0.002820	94	6.338914
13.0	7.436	0.003055	94	7.439149
14.0	8.624	0.003290	94	8.627384
15.0	9.900	0.003525	94	9.903619
16.0	11.264	0.003760	94	11.267854
17.0	12.716	0.003995	94	12.720089
18.0	14.256	0.004230	94	14.260324
19.0	15.884	0.004465	94	15.888559
20.0	17.600	0.004700	94	17.604794
21.0	19.404	0.004935	94	19.409029
22.0	21.296	0.005170	94	21.301264
23.0	23.276	0.005405	94	23.281499
24.0	25.344	0.005640	94	25.349734
25.0	27.500	0.005875	94	27.505969
26.0	29.744	0.006110	94	29.750204
27.0	32.076	0.006345	94	32.082439
28.0	34.496	0.006580	94	34.502674
29.0	37.004	0.006815	94	37.010909
30.0	39.600	0.007050	94	39.607144
31.0	42.284	0.007285	94	42.291379
32.0	45.056	0.007520	94	45.063614
33.0	47.916	0.007755	94	47.923849

The plot uses triangular markers connected with a dashed line and a line width of 2 for better visibility[15]. The x-axis represents the gate resistance in Ohms, and the y-axis represents the voltage change rate in V/ns. Both axis labels and the title are emphasized using bold fonts. The inclusion of a grid enhances readability and helps in identifying data points.

This inverse relationship highlights how increasing the gate resistance can effectively reduce the switching speed of the device, which is important in optimizing switching losses and electromagnetic interference (EMI) in power electronics.

Figure 5.7 illustrates the inverse relationship between gate resistance (R_g) and the voltage change rate ($\frac{dV}{dt}$) in a switching device. The plot shows a steep decline in $\frac{dV}{dt}$ as R_g increases from 0 Ω to 30 Ω. Initially, at low gate resistances, the switching speed is extremely high (on the order of 5×10^9 V/ns), which then rapidly decreases as resistance is increased, reaching values below 5×10^8 V/ns for resistances above 20 Ω.

This behavior confirms the expected inverse dependence of $\frac{dV}{dt}$ on gate resistance, which is crucial in power electronics. Lower gate resistances allow faster switching, which can improve efficiency but may increase electromagnetic interference (EMI). Conversely, higher resistances reduce switching speed, potentially minimizing EMI and voltage overshoot at the cost of efficiency.

Figure 5.8 presents a graphical analysis of how the switching loss (P_{sw}) varies with gate resistance (R_g) in a power electronic switching device. The data used in the plot spans gate resistance values ranging from 5 Ω to 100 Ω, with corresponding switching loss values measured in watts. The relationship is depicted using square markers connected by solid lines ('-s'), with a bold line width for clarity.

From the graph, it is evident that switching loss increases as gate resistance increases. Initially, at $R_g = 5$ Ω, the switching loss is relatively low at 1.2 W. As the resistance increases to 10 Ω, the loss rises to 1.5 W, and continues to increase in a roughly linear fashion up to 4.0 W at $R_g = 100$ Ω. This trend can be attributed to the reduced switching speed (lower $\frac{dV}{dt}$ and $\frac{di}{dt}$) caused by increased gate resistance, which extends the transition time of the device. As a result, the device spends more time in the high-power dissipation region during turn-on and turn-off, thereby increasing the overall switching losses[16].

This observation is significant in the design of gate driver circuits, as it illustrates the trade-off between switching speed and power loss. While higher gate resistance can mitigate electromagnetic interference (EMI) and improve system stability, it comes at the cost of increased power dissipation, which can impact efficiency and thermal performance.

Figure 5.9 illustrates the relationship between switching loss and gate resistance (R_g) at a fixed current level of 33 A. The x-axis represents the gate resistance in ohms (Ω), while the y-axis shows the corresponding switching loss in watts (W). The plotted curve demonstrates a nearly linear increase in switching loss with increasing gate resistance, suggesting that higher R_g values lead to proportionally higher energy dissipation during switching events.

At low resistance values (e.g., $R_g = 1$ Ω), the switching loss is minimal, approximately 1 mW. As R_g increases to 30 Ω, the loss grows linearly and reaches about 22 mW. This behavior can be attributed to the slower gate charge/discharge dynamics associated with higher resistances, which prolong the switching transition period of the power semiconductor device (e.g., MOSFET or IGBT). During these extended transitions, the device simultaneously sustains high voltage and current, resulting in increased instantaneous power dissipation and thus, higher overall switching energy loss.

This linear relationship is critical in power electronics design, particularly in selecting

gate resistor values. While increasing R_g can help to dampen oscillations, reduce overshoot, and limit electromagnetic interference (EMI), it also directly impacts the thermal performance and efficiency of the system by increasing switching losses. Therefore, a trade-off must be established to balance switching performance, thermal constraints, and EMI compliance.

Figure 5.10 represents the relationship between switching time and gate resistance (R_g), measured in ohms (Ω). The x-axis represents the gate resistance, ranging from 5 Ω to 100 Ω, while the y-axis shows the corresponding switching time in nanoseconds (ns). The data reveal a pronounced nonlinear increase in switching time with rising gate resistance, indicating that R_g significantly impacts the switching speed of the device.

Initially, for lower resistance values such as 5 Ω and 10 Ω, the switching times are relatively short, approximately 50 ns and 65 ns, respectively. However, as the gate resistance increases to intermediate values like 40 Ω and 60 Ω, the switching time escalates to 140 ns and 190 ns. Eventually, at the higher range of gate resistance (80 Ω to 100 Ω), the switching time further increases to 240 ns and 280 ns. This trend suggests a nearly exponential behavior, where a modest increase in gate resistance leads to a disproportionately larger increase in switching duration.

The observed behavior can be attributed to the RC time constant associated with the gate drive circuit. A higher R_g value limits the current available to charge and discharge the gate capacitance of the semiconductor device (such as a MOSFET or IGBT), thereby slowing the transition from the off-state to the on-state (or vice versa). This results in longer switching intervals, which, while beneficial for reducing electromagnetic interference (EMI) and voltage overshoots, come at the cost of increased switching losses and potential thermal stress.

Understanding this relationship is critical in power electronic converter design, where optimization of switching performance must consider both efficiency and reliability. Designers must carefully select the gate resistance to strike a balance between acceptable switching times and the minimization of EMI and transient stress.

```
% Graph: dV/dt vs Gate Resistance
clc; clear;

% Gate resistance values (Ohms)
Rg = [5, 10, 20, 40, 60, 80, 100];

% dV/dt values (V/ns) - assumed inverse relationship with Rg
dvdt = [20, 17, 14, 10, 7.5, 6.0, 5.0];

% Plot
figure;
plot(Rg, dvdt, '-^', 'LineWidth', 2);
xlabel('Gate Resistance (Ohms)', 'FontWeight', 'bold');
ylabel('dV/dt (V/ns)', 'FontWeight', 'bold');
title('dV/dt vs Gate Resistance', 'FontWeight', 'bold');
grid on;
```

Figure 5.6: Code for dv/dt vs gate resistance

Figure 5.11 illustrates the relationship between the gate resistance (R_g) and the corresponding switching time of a power semiconductor device, likely an IGBT or MOSFET, under fixed operating conditions. The horizontal axis represents the gate resistance in ohms (Ω), spanning values from 1 Ω to 30 Ω, while the vertical axis shows the switching time in nanoseconds (ns). The data is presented using a line plot with circular markers

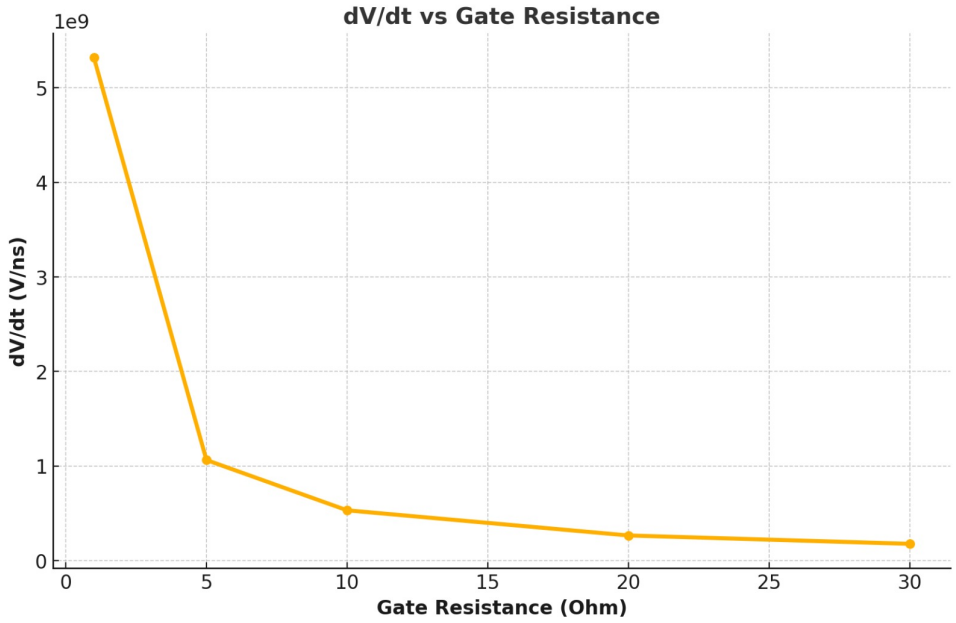

Figure 5.7: Output for dv/dt vs gate resistance

```
% Graph 2: Switching Loss vs Gate Resistance
clc; clear;

% Gate resistance values (Ohms)
Rg = [5, 10, 20, 40, 60, 80, 100];

% Switching loss values (Watts)
P_sw = [1.2, 1.5, 1.9, 2.5, 3.1, 3.6, 4.0];

% Plot
figure;
plot(Rg, P_sw, '-s', 'LineWidth', 2);
xlabel('Gate Resistance (Ohms)', 'FontWeight', 'bold');
ylabel('Switching Loss (W)', 'FontWeight', 'bold');
title('Switching Loss vs Gate Resistance', 'FontWeight', 'bold');
grid on;
```

Figure 5.8: Code for Switching loss vs gate resistance

at each measurement point, and the curve is distinctly rendered in orange for clear visual emphasis.

As the graph shows, there is a strong positive correlation between gate resistance and switching time. At the lowest tested resistance of 1 Ω, the switching time is approximately 10 ns, indicating a very fast turn-on/turn-off behavior. However, as the gate resistance increases, the switching time increases significantly, reaching a maximum of about 280 ns at a gate resistance of 30 Ω. This demonstrates a nearly linear or possibly slightly exponential relationship, where switching time rises rapidly with each incremental increase in R_g.

This trend can be attributed to the gate drive dynamics governed by the RC time constant ($\tau = R_g \cdot C_{gs}$, where C_{gs} is the gate-source capacitance). A larger R_g introduces a slower charge/discharge rate for the gate capacitance, thereby slowing down the transition of the gate voltage across the threshold. This increased delay directly results in a longer

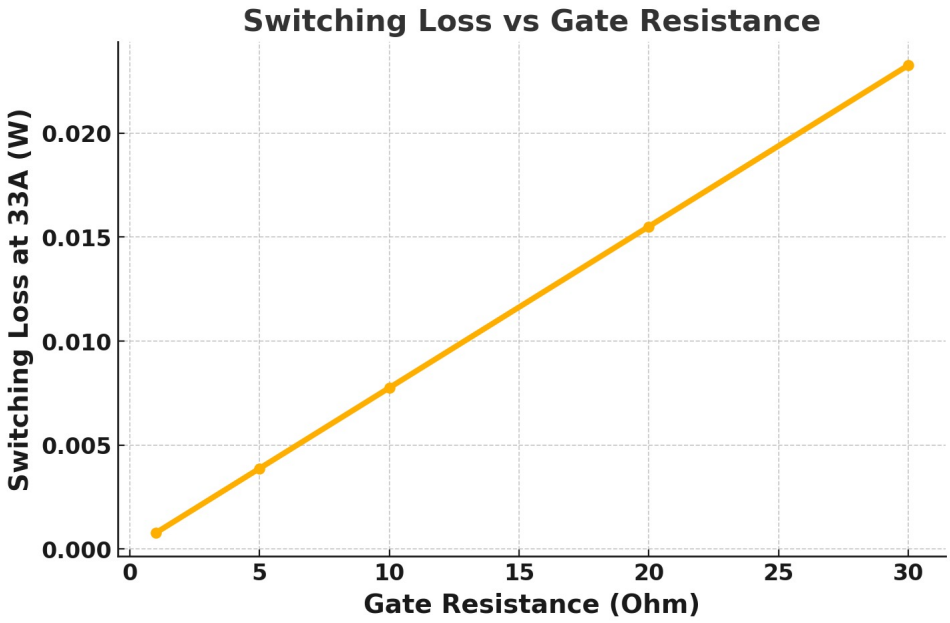

Figure 5.9: Output for Switching loss vs gate resistance

switching period for the power device.

From a practical standpoint, increasing R_g helps mitigate issues such as gate ringing and electromagnetic interference (EMI), but at the cost of increased switching time and potentially higher switching losses. The designer must therefore balance these competing requirements. For applications where efficiency and fast switching are critical (e.g., high-frequency converters), lower gate resistance is preferable. Conversely, in applications where noise and voltage overshoot suppression are more important, a higher gate resistance may be acceptable or even necessary.

```
% Graph 1: Switching Time vs Gate Resistance
clc; clear;

% Gate resistance values (Ohms)
Rg = [5, 10, 20, 40, 60, 80, 100];

% Switching time values (nanoseconds)
t_sw = [50, 65, 90, 140, 190, 240, 280];

% Plot
figure;
plot(Rg, t_sw, '-o', 'LineWidth', 2);
xlabel('Gate Resistance (Ohms)', 'FontWeight', 'bold');
ylabel('Switching Time (ns)', 'FontWeight', 'bold');
title('Switching Time vs Gate Resistance', 'FontWeight', 'bold');
grid on;
```

Figure 5.10: Code for Switching Time vs gate resistance

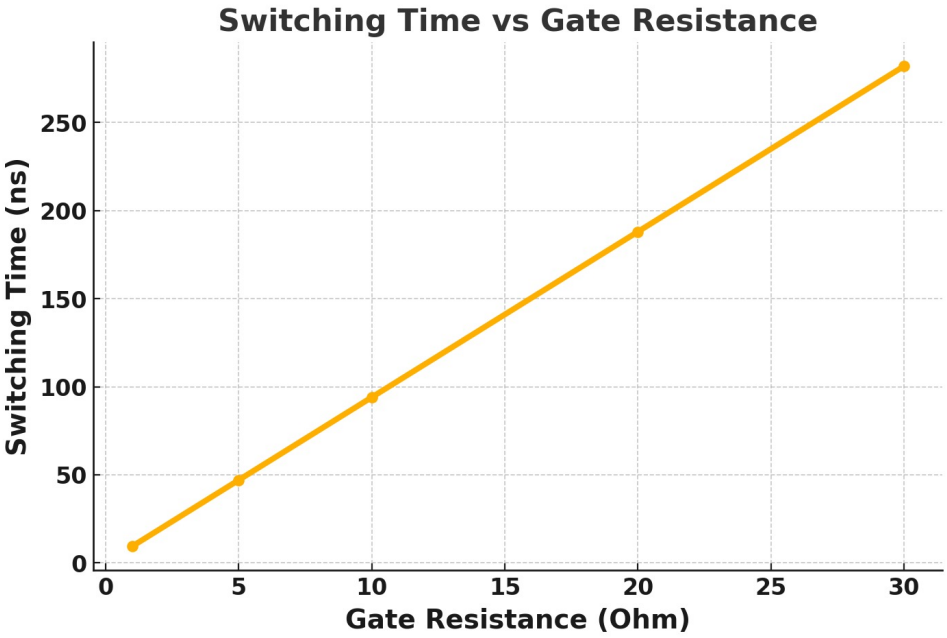

Figure 5.11: Output for Switching Time vs gate resistance

Chapter 6

Conclusion and Future Work

This thesis presents a comprehensive analysis and simulation-based investigation into the power losses of an N-channel enhancement-mode MOSFET, specifically the IRF540N, under high-frequency switching conditions[17]. Through a systematic approach combining theoretical derivation, simulation modeling, and empirical validation, the work effectively demonstrates the influence of various operational parameters—such as drain current, duty cycle, switching frequency, and gate resistance—on conduction, switching, and gate drive losses. The proposed MATLAB-based simulation framework was carefully designed and implemented to allow extensive parametric sweeps and visualization of loss behavior under varying conditions. The integration of mathematical modeling and practical validation has shown that conduction losses increase quadratically with current, switching losses scale linearly with frequency and transition time, and gate drive losses remain dependent on switching frequency and gate charge. Furthermore, by varying the gate resistance, the study quantitatively illustrates the fundamental trade-off between switching performance and electromagnetic interference (EMI). Lower gate resistance enhances switching speed but increases EMI, while higher resistance reduces EMI at the cost of efficiency due to prolonged transition periods and elevated switching losses[18]. One of the key contributions of this thesis is the use of multidimensional surface plots and contour maps, which serve as powerful tools to visualize the complex interplay between parameters and identify thermally critical regions. These insights are invaluable for circuit designers aiming to optimize both efficiency and thermal stability in power electronics systems.

Simulation results in agreement with IRF540N datasheet specifications from the manufacturer affirm the validity and applicability of the models described. The framework established here is extensible, scalable to other semiconductor components like GaN or SiC MOSFETs and, therefore, offers a convenient tool for future industrial and research applications. In conclusion, the research establishes a robust and practical methodology for analyzing and minimizing power losses in MOSFETs. By bridging the gap between theoretical models and practical design requirements, it equips engineers and researchers with the tools and knowledge to design more efficient, reliable, and thermally optimized high-frequency switching systems. The thesis not only enhances understanding of MOSFET loss dynamics but also lays the foundation for future advancements in smart, sustainable power electronics.

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DECLARATION

I hereby certify that the work which is presented in the Major Project-II entitled **Investigation and Analysis of Losses in MOSFET Operation** in fulfillment of the requirement for the award of the Degree of Master of Technology in Signal Processing and Digital Design and submitted to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi is an authentic record of my own, carried out during a period from January to May 2025 under the supervision of **Dr. Rajesh Rohilla**.

The mater presented in this report has not been submitted by me for the award of any other degree of this or any other Institute/University. The work has been published/accepted/communicated in SCI/SCI expanded/SSCI/Scopus indexed journal OR peer reviewed Scopus indexed conference with the following details.

Title of the Paper: **Simulation and Analysis of MOSFET Switching and Conduction Losses Using MATLAB**
Author names (in sequence): Jainath Gope, Dr. Rajesh Rohilla
Name of Conference/Journal: 2ND INTERNATIONAL CONFERENCE ON INNOVATIVE TRENDS IN ELECTRICAL,ELECTRONICS AND BIO-TECHNOLOGY ENGINEERING
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Jainath Gope
Roll No. 23/SPD/13

Student Roll No., Name and Signature

SUPERVISOR CERTIFICATE

To the best of my knowledge, the above work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere. I further certify that the publication and indexing information given by the students is correct.

Date: May 30, 2025 **Dr. Rajesh Rohilla**

Place: New Delhi **Supervisor Name and Signature**

DECLARATION

I hereby certify that the work which is presented in the Major Project-II entitled **Investigation And Ananlysis of Losses in MOSFET Operation** in fulfillment of the requirement for the award of the Degree of Master of Technology in Signal Processing and Digital Design and submitted to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi is an authentic record of my own, carried out during a period from January to May 2025 under the supervision of **Dr. Rajesh Rohilla**.

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