SIGNAL PROCESSING AND GENERATING CIRCUITS USING OTRA AS A BUILDING BLOCK

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Certificate

This is to certify that the thesis titled "**Signal Processing and Generating Circuits using OTRA as a Building Block**" being submitted by Rajeshwari Pandey to the Department of Electronics and Communication Engineering, Delhi University, Delhi, for the award of the degree of Doctor of Philosophy, is a record of bonafide research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in this thesis have not been submitted to any other university or institute for the award of any degree or diploma.

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Abstract

The low-voltage and low-power mixed mode circuit design has gained importance with the advent of the portable electronic and mobile communication systems. More and more mixed mode circuit blocks, are being integrated onto a single chip in an effort to reduce overall cost and space and to improve system performance. This requires the scaling of CMOS technology. The reliability and density factors associated with technology scaling demand for downsized supply voltages. This trend of continuous reduction of the supply voltage poses serious challenges to the analog designers. To circumvent this conflict instead of using costly CMOS technologies with lower thresholds, it is desirable to use low voltage circuit techniques that are compatible with standard CMOS processes.

In last few decades the current-mode processing has emerged as an alternative design technique. Ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain, as current mode circuits are designed for lower voltage swings. While fundamentally any design techniques is limited by device characteristics there may be specific applications where current-mode circuits provide one or more of the following advantages: higher bandwidth, better signal linearity, higher slew rates, lower power consumption, and better accuracy. Additionally, current-mode circuits are often less complex than the voltage-mode circuits, which may lead to significant chip area savings.

Emergence of various current-mode analog building blocks is outcome of the considerable progress in current-mode analog signal processing. Operational transresistance amplifier (OTRA) among those is of relatively recent origin. It is a high gain current input voltage

output device which provides advantages of current mode design techniques and can readily be used for voltage-mode applications.

A wide variety of OTRA based system applications, ranging from filters, oscillators, multivibrators through general analog interfacing, are available in literature. In this research work design and development of signal generating and processing circuits using OTRA as building block is presented. The prime concern of the designs is to provide better quality response, introduce versatility and modularity, and to develop circuits which could be better implemented in integrated circuit form.

Exploring the important research topic of active inductance simulation, OTRA based five inductance simulation topologies have been proposed. A single OTRA based lossy inductance topology and two topologies of lossless inductance using two OTRAs are presented. Further an important contribution is development of single OTRA based lossless grounded inductance, as, no such topology exists in the literature.

Single OTRA based two; biquadratic multifunction structures, development of single- input multiple output (SIMO) biquadratic universal filter and wave method based realization of higher order resistively terminated LC ladder filters is the research contribution in the field of filter design.

Single OTRA based designs are single- input single-output (SISO) configurations and can realize low pass (LP), high pass (HP), and band pass (BP) filter functions. The proposed circuits do not impose any component constraints in contrast to the similar class of existing circuits.

Single amplifier based biquad (SAB) is a useful choice for power efficient design. However, SABs are less versatile and more sensitive to parameter changes as compared to multiamplifier filters. As an improvement over presented SISO structures a SIMO biquadratic universal filter is proposed which provides all standard responses simultaneously. Concept of electronic tunability of filter parameters has also been introduced.

Multiamplifier filters can be used for design of biquads and higher order filters. Higher order filters using doubly terminated lossless ladders have low sensitivity to component tolerances. However, these use inductors, which are difficult to realize in an IC form. Wave method can be used for realizing higher order resistively terminated LC ladder filters which does not require use of inductors. In this work, OTRA based electronically tunable wave active filter structures are presented which are highly modular and can readily be used.

Signal generators are an important class of electronic circuits. A number of sinusoidal oscillator circuits are proposed which include a sinusoidal oscillator; a third order quadrature oscillator and three multiphase sinusoidal oscillators. The proposed sinusoidal oscillator and third order quadrature oscillator are MOS-C implemented and can be tuned electronically.

An important contribution is development of few OTRA based linear and nonlinear applications. Under linear class of applications, a transimpedance instrumentation amplifier and feedback controllers are propossed whereas a voltage controlled multivibrator, a pulse width modulator and an analog multiplier have been proposed as nonlinear applications.

Practical design issues pertaining to nonidealities associated with OTRA have been addressed for all the proposed structures. The proposed designs are verified either through SPICE simulations or combination of SPICE simulations and experimental evaluations.

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1. Rajeshwari Pandey, Neeta Pandey Sajal K. Paul A. Singh B. Sriram, and K. Trivedi **"New Topologies of Lossless Grounded Inductor Using OTRA"** Journal of Electrical and Computer Engineering Volume 2011, Article ID 175130, 6 pages, doi:10.1155/2011/175130.

2. Rajeshwari Pandey, Neeta Pandey, Mayank Bothra and Sajal K. Paul **"Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators,"** Journal of Electrical and Computer Engineering Volume 2011, Article ID 586853, 8 pages doi:10.1155/2011/586853.

3. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, B. Sriram, **"Single OTRA based analog multiplier and its applications,"** ISRN Journal of Electronics Volume 2012, Article ID 890615, 7 pages,doi:10.5402/2012/890615.

4. Rajeshwari Pandey, Saurabh Chitransi, Neeta Pandey, Chandra Shekhar. **"Single OTRA based PD Controllers,"** International Journal of Engineering Science and Technology, vol. 4, pp.1426-1437, 2012.

5. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, A. Singh, B. Sriram, and K. Trivedi, "**Voltage Mode OTRA MOS-C Single Input Multi Output Biquadratic Universal Filter**," Advances in Electrical and Electronic Engineering, vol.10, pp. 337-344, 2012.

6. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, "**Electronically Tunable Transimpedance Instrumentation Amplifier based on OTRA**," Journal of Engineering, Volume 2013, Article ID 648540, 5 pages, doi.org/10.1155/2013/648540.

7. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, "**Voltage Mode Pulse Width Modulator Using Single Operational Transresistance Amplifier,"** Journal of Engineering, Volume 2013, Article ID 309124, 6 pages, doi.org/10.1155/2013/309124.

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2. Rajeshwari Pandey, Neeta Pandey, Ajay Singh, B. Sriram, Kaushalendra Trivedi **"Grounded Immittance Simulator Using Single OTRA with a Signal Processing Application,"** International Conference on Electronics and Computer Technology, ICECT- 2011, pp. 404– 406, April 2011

3. Mayank Bothra, Rajeshwari Pandey, Neeta Pandey, **"Versatile Voltage Controlled Relaxation Oscillators Using OTRA,"** International Conference on Electronics and Computer Technology, ICECT- 2011, pp, 394 – 398, April 2011.

4. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Mandeep Singh, Manish Jain **"Voltage Mode single OTRA based Biquadratic Filters,"** International Conference on Communication and Computer Technology, ICCCT-12, pp, 63 – 67, Nov. 2012.

5. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul "**MOS-C Third Order Quadrature Oscillator using OTRA,"** Third International Conference on Communication and Computer Technology, ICCCT-12, pp. 77 -80, Nov. 2012.

6. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Mandeep Singh, Manish Jain, "**Voltage Mode Biquadratic Filter using Single OTRA,"** Fifth India International Conference on Power Electronics, IICPE-2012, pp. 1 - 4, Dec. 2012.

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Practical design issues pertaining to nonidealities associated with OTRA have been addressed for all the proposed structures. The proposed designs are verified either through SPICE simulations or combination of SPICE simulations and experimental evaluations.

CHAPTER – 1
INTRODUCTION

1.1 BACKGROUND

The low-voltage and low-power mixed mode circuit design is the current trend in VLSI industry where both analog and digital circuitry can be fabricated using standard digital CMOS technology on the same silicon substrate. Though in the decade of eighties electronic system design witnessed a pardigm shift from analog to digital domain yet analog circuits have proved fundamental necessity in many of today's complex high performance systems. It is difficult, sometimes impossible, to substitute analog function with their digital counterparts in application areas such as digital and mobile communication, memories, microprocessors and sensor design, irrespective of advances in CMOS technology. The analog functions most often needed are amplification, filtering, sample and hold, signal comparison and analog-to-digtal conversion. The VLSI technology has evolved to a level of integration as high as 100 million transistors on a single chip. This requires the scaling of CMOS technology, however, threshold voltage does not scale in a linear fashion with the reduction in minimum device length. The reliability and density factors associated with technology scaling demand for downsized supply voltages. This trend of continuous reduction of the supply voltage does not put restriction on the digital circuit design but poses serious challenges such as reduced input common mode range, output swing and linearity, to analog design. To circumvent this conflict instead of using costly CMOS technologies with lower thresholds, it is desirable to use low voltage circuit techniques that are compatible with standard CMOS processes [1].

The information processed by lumped electric networks can be represented by either nodal voltages or branch currents of networks [2]. The analog circuits where the circuit performance is determined in terms of voltage levels at various nodes including input and output nodes are referred to as voltage-mode (VM) circuits. The VM circuits are required to provide large output swing while minimizing the total power consumption. This leads to high impedance node architecture of the VM circuits. However, the parasitic capacitances present in the circuits need to be charged and discharged with large voltage swing, thereby limiting the speed and slew rate of the VM circuits. In VM circuit the BJTs and FETs despite being current devices are generally arranged into voltage oriented networks [3]. The current signal is transferred into voltage domain causing system bandwidth to reduce, as parasitic capacitances with high valued node resistances create dominant pole at low frequency. Thus

simultaneous low voltage, low power and wide bandwidth operations are difficult to achieve in VM circuits.

Over the last few decades current-mode (CM) processing has emerged as an alternative design technique using current signals for signal processing [4]. The CM circuits are low impedance node networks, and thus low time constant circuits, too. This improves system performance in terms of speed and slew rate. In current amplifiers the transistors are useful almost up to their unity gain bandwidth f_T, thereby resulting in wider bandwidth. Yet another advantage of CM circuits results from the nonlinear characteristic of transistors. In FETs the volatge is proportional to square root of current in saturation region of operation; likewise in BJTs the voltage depends logrithmically on current. If current instead of voltage is used as signal, the output swing reduces and hence the CM circuits can operate under low supply voltage [5]. Thus for a fixed supply voltage the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. Additionally, in CM circuits the addition and subtraction operation can be performed by joining the terminals at a single point resulting in simple architecture as compared to VM circuits. This may result in power and chip area saving.

Thus ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain, as current mode circuits are designed for lower voltage swings.

Current- mode signal processing has resulted in emergence of numerous analog building blocks [6] – [34] which are used for realization of various signal processing and generation circuits as presented in [6] – [34] and references cited there in. The current conveyor (CC) [6], a voltage/current hybrid circuit, is the most extensively explored block. The three generations of CC namely CCI, CCII [7], and CCIII [8], were introduced way back in 1968, 1970 and 1995 respectively and differ in terms of port characteristics. Variety of modifications in the basic conveyor structure, for more effective utilization, led to introduction of various CC based newer elements [9] – [19]. An operational transconductance amplifier OTA [20], is a voltage controlled current source and is appropriate for driving capacitive loads only. In order to maintain compatibility with existing

voltage processing circuits, it is necessary to convert the output signal of OTA to voltage using transconductor. Current feedback operational amplifier CFOA [21], [22] has terminal characteristics similar to CCII followed by a voltage follower. The Four Terminal Floating Nullor (FTFN) [23], Operational Floating Amplifier (OFA) [24], Differential Difference OFA (DDOFA) [25] and Differential Difference Amplifier (DDA) [26], are fully balanced structures and hence are more immune to noise. The circuit element Operational Transresistance Amplifier (OTRA) [27] is a current controlled voltage source (CCVS). The Current Differencing Buffered Amplifier (CDBA) [28], a four terminal block, is a generalization of OTRA and consists of a Current Differencing Unit (CDU) and a unity-gain voltage buffer. A variant of CDBA called Current Controlled CDBA (CC-CDBA), introducing electronic control of circuit parameters, is described in [29]. It exploits the bias current dependence feature of parasitic input resistances of the CDU for electronic tunability. Another active block, the Current Differencing Transconductance Amplifier (CDTA) reported in [30], operates as a current-mode amplifier. The input subsection of the CDTA is a CDU which is followed by the multiple-output OTA. CDTA applications are well-suited for on-chip implementation as these do not require the use of external resistors [4]. The Current Controlled CDTA (CCCDTA) [31] is a modification of CDTA which provides the electronic control of circuit parameters, based on the same priciple as used in CC-CDBA. Yet another class of current mode blocks having voltage differencing input stage, has also emerged relatively recently. Voltage Differencing Transconductance Amplifier (VDTA) [32], [33] and Voltage Differencing Buffered Amplifier (VDBA) [34] are two representative blocks of this class.

1.2 NEED FOR OTRA BASED CIRCUITS

The OTRA is a high gain current input voltage output device. It has two input terminals which are virtually grounded and one low impedance output terminal. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances. Since the OTRA has a current input and voltage output, a shunt- shunt feedback configuration is used, which places the feedback network and amplifier in parallel. A parallel configuration is suitable for low voltage operations, as it minimizes stacking of transistors thus providing more head room for signal swing. Using

current feedback techniques, OTRAs have a bandwidth almost independent of closed-loop voltage gain. It provides advantages of current mode design techniques and gives voltage output, therefore, can directly drive voltage mode circuits.

In this work, signal generating and processing circuits using OTRA as building block have been developed with the objective of

- Providing design with better quality response
- Exploring versatility
- Introducing electronic tunability
- Getting circuits with easy implementation in IC form

1.3 AVAILABLE LITERATURE AND SCOPE OF WORK

The aviailabe literature on OTRA [27], [35] – [40], [42] – [71] can be classified on the basis of following aspects

(i) OTRA Implementations [27], [35] – [40]

(ii) OTRA models [70], [71]

(iii) OTRA based applications [35], [36], [43] – [69].

Various implementations of OTRA are available in the open literature. It can be realized by using commercially available CFOA AD844 [35]. Alternately, various integrated circuit implementations [27], [36] – [40] are also available. The OTRA proposed in [27] is implemented using a differential current controlled current source followed by a voltage buffer. Reference [36] reported an OTRA structure which is based on cascaded connection of the modified differential current conveyor (MDCC) [41] and a common source amplifier. The OTRA presented in [37] consists of a low voltage regulated cascode current mirror with a low voltage regulated cascode load as the core of the circuit, common source amplifiers gain boosting stage and level shifters followed by common source output stage. The OTRA structure available in [38] is similar to [36] but uses smaller number of current mirrors. This reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Due to smaller number of transistors the power dissipation is also reduced. The CMOS

OTRA realization in [39] uses same input stage as in [38] while a differential gain stage is used instead of the single common source amplifier. This differential stage reduces the DC offset current and increases the DC open loop transresistance gain. Yet another differential OTRA structure, suitable for low supply voltages, is reported in [40]. It uses two symmetrically placed basic input cells consisting of four transistors each. Each cell forms two Class AB current mirror connections [40]. The input unit is followed by gain stage consisting of differential amplifier. The non buffered dual differential outputs are buffered through unity gain configurations [40]. It is a completely differential design structure.

A generalized admittance matrix model for OTRA and COA is introduced in [70] which can be used for computing transfer functions of fully differential analog circuits. A nullor-based model for the OTRA, consisting of four nullors and three grounded resistors has been proposed in [71]. This model can be seen as a behavioral model at the circuit level of abstraction and is of great use in CAD tools. It can easily be applied to compute small-signal characteristics of OTRAs-based analog circuits.

A wide variety of system applications, ranging from inductance simulators [59] – [64], filters [36], [42] – [58], oscillators [36], [51] – [53], [61], [65], through multivibrators [35], [66] – [69] have been developed using OTRA. These applications based on input and output signal type can broadly be classified as voltage-mode (VM), current-mode (CM) and transimpedance-mode (TIM) structures. In VM circuits voltage is used to represent both input and output signals whereas in CM circuits it is current. In TIM structures, input is a current signal and output is taken as voltage signal.

Active inductance simulation has been an important research topic in active network synthesis and finds application in areas such as filter design, oscillator design, phase shifters and parasitic element cancellation. Study of existing literature on OTRA revealed that several lossy and lossless grounded inductance topologies have been reported. Single OTRA based grounded parallel lossy inductance topologies are available in [59], [60]. Grounded lossless inductors employing two OTRAs are proposed in [61] and [62]. Reference [63] presents a single OTRA and a buffer based grounded frequency dependent negative resistance (FDNR) and an inductor. Negative inductance simulation topologies based on a single OTRA, have

been proposed in [64]. All available lossless inductor configurations provide non interactive control on inductance value.

An exhaustive literature surevey gave an insight to explore the additional topologies of single OTRA based lossy inductance and two OTRA based lossless inductance. Also to the best of author's knowledge no single OTRA based lossless inductor was reported in the literature. To fill this void five topologies of lossy/lossless inductance have been presented in this work.

Electronic filters find widespread usage in communications and instrumentation. A vast literature available on OTRA based filters can be classified in terms of (i) type of filter: low pass (LP), high pass (HP), band pass (BP), band reject (BR), all pass (AP), multifunction and universal, (ii) number of input and output signals: single input single output (SISO), single input multiple outputs (SIMO), multiple inputs single output (MISO) and multiple inputs multiple outputs (MIMO), (iii) filter order: first order, biquadratic and higher order structures.

Voltage mode integrators using OTRA are reported in [36], [42], [43]. Structures available in [36] [42] [44] [45] can be classified as VM universal SISO structures. The VM structures reported in [36], [46] fall under SIMO category and are multifunction filters. Work reported in [47] is VM universal MISO filter configuration whereas in [48] a VM multifunction MIMO structure is reported. Few VM first order all pass topologies [51], [52] and second order all pass structures [52], [53] are also available in literature. Linear transformation (LT) high order active filters have the advantage that every section of the original LC ladder prototype can be realized by using active elements individually. VM high order LT filters using OTRAs are presented in [49], [50]. A third order VM Chebyshev LPF is presented in [42].

OTRA based current mode integrator and differentiator structures are presented in [54]. Two different CM SISO universal biquad structures are also discussed in [54]. A first order CM all pass structure is proposed in [55]. Current mode linear transformation MOSFET-C filters based on OTRAs and simplified MOSFET resistor circuits are available in [56].

Reference [57] presents a TIM first order all pass filter and a TIM universal MISO filter using OTRA is presented in [58].

Single active element based filter is a useful choice for power efficient design. It is evident from literature review that all available single OTRA based VM filters required component selection for realization of various responses. Additionally, reported structures are needed to fulfill the component matching constraint and/or condition on components. These structures do not provide high quality factor (Q_0) with moderate component spread. Therefore, in this work single OTRA based two; VM biquadratic multifunction SISO structures are presented which can realize LP, HP, and BP filter functions without imposing component constraints.

Currently available literature suggested that no OTRA based SIMO structure was available that provided all five standard responses simultaneously. This has motivated the development of a five outputs SIMO universal filter.

Higher order filters using doubly terminated lossless ladders have low sensitivity to component tolerances. However, these use inductors, which are difficult to realize in an IC form. To avoid the use of inductors, element replacement and operational simulation techniques are used.Wave method can also be used for realizing higher order resistively terminated LC ladder filters. In this work, OTRA based electronically tunable wave active filter structures are presented which are highly modular and can readily be used.

Signal generators are an important class of circuits and find wide application in electronic system design. Available literature on signal generators can broadly be classified as (i) sinusoidal and (ii) non linear oscillators. A number of schemes have been proposed in the literature to realize OTRA based sinusoidal oscillators [61], [65]. Quadrature oscillators (QO) are reported in [36], [51] – [53]. Five sinusoidal oscillator circuits, consisting of a single phase, a quadrature phase and three multiphase circuits are presented in this thesis with improved features such as noninteractive frequency control, electronic tunability, low harmonic distortion and better accuracy.

Few nonlinear signal generators using OTRA are also available in open literature, which find extensive applications in nonlinear circuits. The design of bistable multi vibrator is proposed

in [66] and OTRA based VM square wave generator is discussed in [35]. Current-mode monostable [67], [68] and bistable [69] multivibrators structures using OTRA have also been explored. The available literature revealed that the area of nonlinear signal generation has not been explored extensively and has lot of potential. Therefore, a nonlinear oscillator circuit with its proposed usage is presented. Two nonlinear applications of OTRA namely, analog multiplier and pulse width modulator (PWM) have also been included in this thesis. Additionally, transimpedance instrumentation amplifier (TIA) and feedback controllers, which do not find a mention in the available literature, are presented as linear applications of OTRA.

1.4 ORGANIZATION OF THE THESIS

There has been a constant upsurge in electronic system design to cater the needs of the market. Traditionally the analog subsystems were progressively being replaced by digital systems to adapt to the continuing reduction in feature size of digital devices in VLSI implementation. However, analog design has gained a renewed interest due to the designs catering high frequency applications and is becoming increasingly important with growing opportunities. Continuous time techniques do not require anti-alaising and smoothing filters. Additionally clock feed-through, fold over noise, etc. are no longer an issue as these circuits do not require clocked operations. Conventional op-amp is not a suitable candidate for these designs owing to its high frequency limitations. This problem can be addressed by using current mode blocks and design techniques. In this study some investigations, on the application of OTRA in analog electronic design, have been carried out.

Chapter 1 presents an account of the evolution of current mode signal processing and a brief review of various current mode analog building blocks that emerged for analog electronic design. A review of existing work on signal processing and generation circuits using OTRA has been presented thereafter. This is followed by the outline of the research work presented in this study.

Chapter 2 is devoted to the study of the OTRA with an aim to bring most of the published information related to OTRA implementations. A detailed analysis of the CMOS

implementation of OTRA, used for PSPICE simulation of various circuits proposed in this thesis, is included and has also been characterized using SPICE to validate its functionality.

Active inductance simulation has been an important research topic in active network synthesis and these simulated inductors find application in areas such as filter design, oscillator design, phase shifters and parasitic element cancellation. In **chapter 3** OTRA based new grounded immittance simulation topologies have been explored and a brief review of existing literature in the area is also presented.

Electronic filters find widespread usage in communications and instrumentation. This led to explore the arena of filter design using OTRA and **chapter 4** is a record of it. After a brief review of available literature the chapter coveres the design of proposed filter configurations based on single and multiple amplifiers. Multiamplifier filters are further classified as biquads and higher order filters. MOS–C realization of multiamplifier filters has also been attempted.

Signal generation using OTRA is the theme of **Chapter 5** with prime focus on sinosoidal signal generators, also known as linear oscillators. General scheme of sinosoidal signal generation is discussed, firstly, followed by design description of proposed oscillators.

Chapter 6 deals with the instrumentation and conrol applications of OTRA. It describes the design of OTRA based transimpedance instrumentation amplifier and the most popularly used feedback controllers, namely proportional, proportional-derivative, proportional integral and proportional derivative and integral.

In **Chapter 7** nonlinear applications of OTRA are proposed. Realization of a voltage controlled multivibrator and its application in a compound pulse frequency and width modulator is dealt with first. Design of a pulse width modulator is described thereafter. The concluding application presented in the chapter, is an OTRA based four quadrant analog multiplier which finds wide variety of applications in communication and signal processing. Two typical examples of this multiplier; squarer and amplitude modulator are also attempted.

The work is concluded on the roadmap outlined above in **Chapter 8.**

CHAPTER – 2
OPERATIONAL TRANSRESISTANCE AMPLIFIER

2.1 INTRODUCTION

Ever since its development the operational amplifier (op-amp) is an integral part of analog signal processing and generating circuits. It is intended to implement closed loop voltage processing circuits which are known as voltage-mode (VM) circuits. However high frequency performance of these circuits is limited due to constant gain-bandwidth product and low slew rate of the op-amps. The attempt to overcome this problem has led to the development of current-mode (CM) signal processing. In CM signal processing, current is used as the active variable in preference to voltage, either throughout the circuit or only in certain critical areas [72]. CM techniques can achieve a considerable improvement in system performance in terms of bandwidth, signal linearity, slew rate and power consumption. Consequently CM signal processing has progresssed considerably in past few decades and has resulted in emergence of various CM analog building blocks [4] and OTRA [36] among those is of relatively recent origin. The OTRA is a high gain current input voltage output device. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances making OTRA appropriate for high frequency applications.

In order to maintain compatibility with existing voltage processing circuits, it is necessary to convert the input and output signals of current-mode circuits to voltage, using transconductors and transresitors respectively. This has the disadvantage of increasing both the chip area and power dissipation. However circuits using OTRA as the active element benefit from the current processing capabilities at the input terminals, and can directly drive the existing VM signal processing circuits thus eliminating the requirement of additional circuitry and associated power consumption, at the output.

In this chapter OTRA has been dealt with in detail. The ideal OTRA is introduced first which is followed by its nullor based model. This model can be used in CAD tools to compute fully-symbolic small-signal characteristics of OTRA-based analog circuits. The existing OTRA realizations have been taken up later. Few basic applications of the OTRA such as voltage amplifiers, adder, subtractor, and integrator circuits are also described. The chapter

concludes with description of passive resistor realization in OTRA based circuits with its MOS based counterpart thereby making circuits suitable from integration viewpoint.

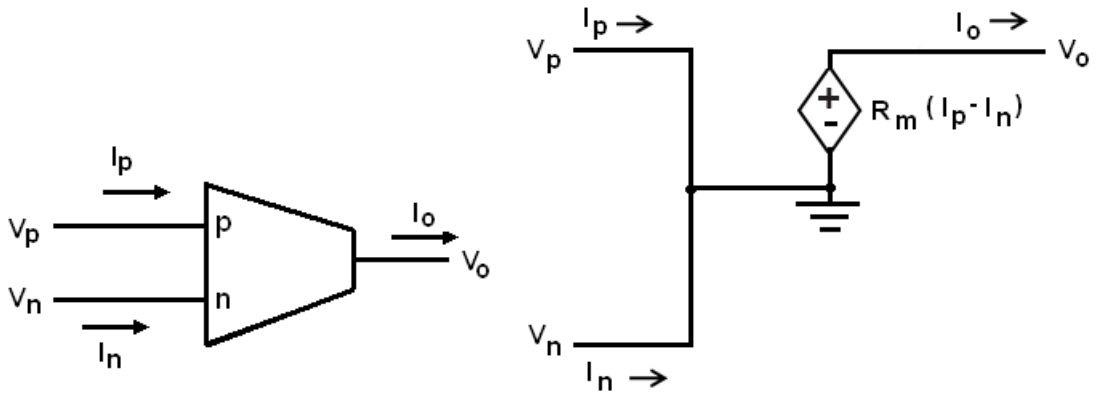
2.2 THE IDEAL OTRA

The circuit symbol of an OTRA [36] is shown in Fig. 2.1(a). An Ideal OTRA senses the difference of the currents at its two input terminals, namely p and n, amplifies it and provides a resulting voltage at the output terminal. For ideal operations the input terminal voltages should be zero. Additionally the output voltage should be independent of the current that may be drawn from the output terminal by the load impedance. Putting together, an equivalent OTRA circuit model can be drawn as shown in Fig. 2.1(b) and the port characteristics of OTRA can be expressed by (2.1) where R_m is transresistance gain of OTRA. For ideal operations the R_m approaches infinity and forces the input currents to be equal.

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_0 \end{bmatrix} \tag{2.1}$$

Though the above idealized conditions can not be realized in practice yet the use of such an ideal OTRA model simplifies the mathematical analysis of OTRA circuits. The practical OTRA circuits are made to approximate the idealized characteristics. The equivalent circuit model of a practical OTRA is shown in Fig. 2.2 where R_p and R_n represent terminal resistances of p and n ports respectively.

OTRA in the simplest way can be used in an open loop configuration; however, its gain being infinity the output voltage saturates either at positive or negative satutation level. This operation has a limited number of applications. Thus OTRA must be used in a negative feedback configuration where the output is not driven into saturation and the circuit behaves linearly. Since the OTRA has a current input and voltage output a shunt- shunt feedback configuration is used which places the feedback network and amplifier in parallel. A parallel configuration is suitable for low voltage operations as it minimizes stacking of transistors thereby providing more head room for signal swing [37]. Also using current feedback techniques OTRAs have a bandwidth almost independent of closed-loop gain.



(a) (b)

Fig. 2.1 (a) OTRA circuit Symbol. (b) Equivalent circuit.

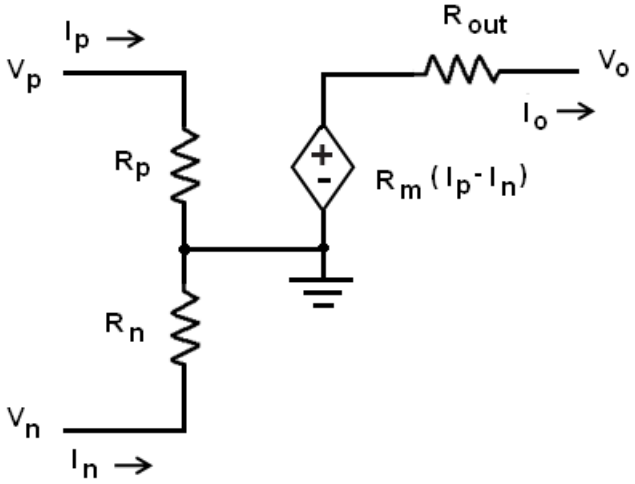


Fig. 2.2 Equivalent circuit model of a practical OTRA.

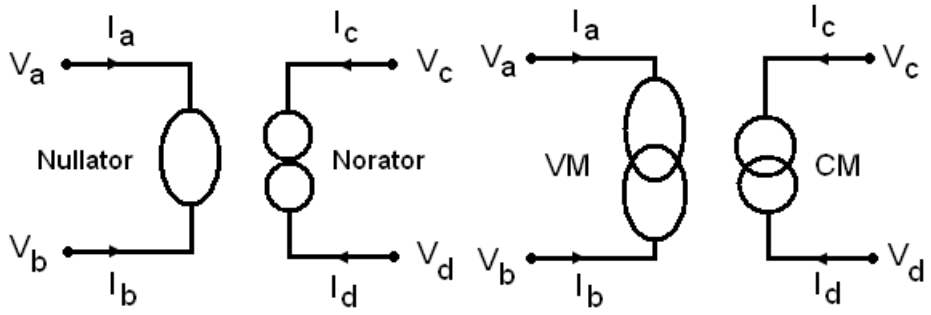
2.3 NULLOR BASED OTRA MODEL

The nullor is an ideal element which is composed of a nullator, connected at the input port and a norator, connected at the output port, as shown in Fig. 2.3 (a) [73]. The terminal characteristics of nullator can be represented as

$$V_b = V_a = \text{arbitrary} \text{ and } I_b = I_a = 0 \quad (2.2)$$

Similarly the terminal equations for the norator can be expressed as

$$V_d \neq V_c = \text{arbitrary} \text{ and } I_d = -I_c \quad (2.3)$$



(a) (b)

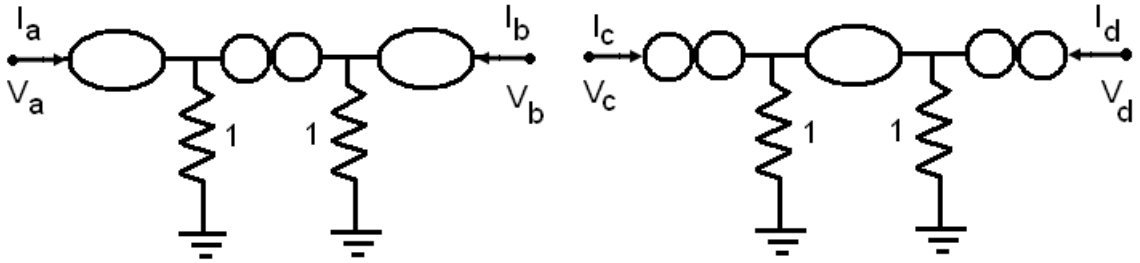
Fig. 2.3 Pathological elements [73]. (a) Nullor. (b) VM-CM pair.

The nullor with inverting characteristics can be implemented with voltage mirror- current mirror (VM-CM) pair as shown in Fig. 2.3(b) [73]. This pair is also an ideal element and it is composed of a VM at the input port and a CM at the output port. The VM and CM can be characterized by (2.4) and (2.5) respectively

$$V_b = -V_a = \text{arbitrary} \text{ and } I_b = I_a = 0 \tag{2.4}$$

$$V_d \neq V_c = \text{arbitrary} \text{ and } I_d = I_c \tag{2.5}$$

The VM-CM can also be modeled using nullators, norators along with unity grounded resistors as shown in Fig. 2.4.



(a) (b)

Fig. 2.4 Nullor based models [73] of (a) Voltage mirror (VM). (b) Current mirror (CM).

The nullators, norators and VM-CM pair collectively are known as pathological elements. The behavior of active devices can be modeled using pathological elements. Thus the analog circuits can be transformed to nullor and/or VM-CM pairs based equivalent circuits and symbolic analysis techniques can be applied to approximate small-signal characteristics of

these analog circuits. The nullor based model of OTRA [71] is shown in Fig. 2.5. According to the nullor concept if one terminal of a nullator is connected to signal-ground, the other terminal is considered as a virtual ground; therefore, a node of low impedance is obtained. Also, nullator does not allow current to flow through it. In OTRA the currents I_p and I_n enter into the low impedance input terminals. This can be modeled with the nullor if one terminal of the nullator is connected to signal-ground and the input current is flowing through the norator. Hence, both the input terminals can be modeled with current followers (CFs), as shown in Fig. 2.5. The output voltage is the difference of the input currents multiplied by the transresistance gain, R_m, which is ideally infinity; therefore, a change of direction of I_n must be required to force the input currents to be equal. A current mirror as shown in Fig. 2.4 (b) is used to reverse the direction of I_n. A voltage follower consisting of a nullor is used at the output terminal, where the current difference is transformed to voltage by R_m.

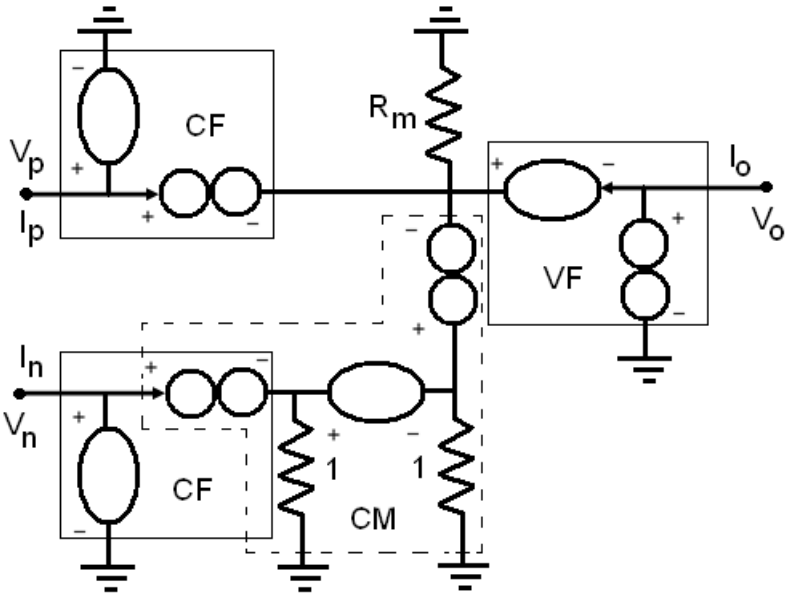


Fig. 2.5 Nullor based model of OTRA [71].

2.4 NONIDEAL MODEL OF OTRA

The transresistance gain R_m of an OTRA should ideally be infinity. However, in practice it is finite and its effect along with the frequency limitations associated with the OTRA must be considered [36]. Thus the R_m can be represented using a single-pole model given by

$$R_m(s) = \left(\frac{R_0}{1+{}^{s}/_{\omega_0}}\right) \tag{2.6}$$

where R_0 is DC open loop transresistance gain. For high frequency applications, the transresistance gain, $R_m(s)$, can be expressed as

$$R_m(s) \approx \left(\frac{1}{{}^{s}/_{R_0\omega_0}}\right) = \left(\frac{1}{sC_p}\right);\ C_p = \frac{1}{R_0\,\omega_0} \tag{2.7}$$

The C_p is called the parasitic capacitance of OTRA.

2.5 OTRA IMPLEMENTATION

In this section a review of existing literarture on OTRA implementation is presented. An extensive review suggests that various implementations of OTRA are available in literature and are based on:

(i) Using commercially available AD844 (CFOA) ICs [35].

(ii) Using integrated circuit implementations [27], [36] – [40].

2.5.1 CFOA Based Realization

CFOAs are commercially available as IC AD844. The circuit symbol of CFOA is shown in Fig. 2.6 and the port relations of a CFOA can be characterized by

$$V_x = V_y\,;\ I_y = 0;\ I_z = I_x;\ V_w = V_z \tag{2.8}$$

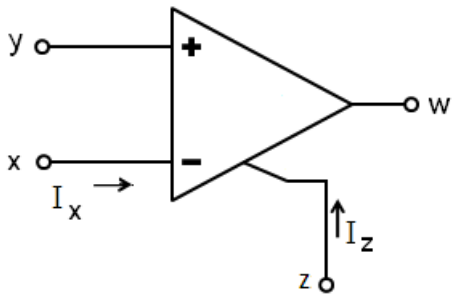


Fig. 2.6 CFOA circuit Symbol.

The OTRA can be realized using two AD844 CFOA ICs as shown in Fig. 2.7 [35]. From Fig. 2.7 various currents can be calculated as

$$I_{z1} = I_p \tag{2.9}$$

$$I_{x2} = I_n - I_{z1} \tag{2.10}$$

$$I_{z2} = I_{x2} \tag{2.11}$$

From (2. 9) and (2.10), the current through z_2 terminal can be computed as

$$I_{z2} = I_n - I_p \tag{2.12}$$

The voltages at various ports may be written as

$$V_p = V_{1-} = V_{1+} = 0 \tag{2.13}$$

$$V_n = V_{2-} = V_{2+} = 0 \tag{2.14}$$

$$V_o = V_{z2} = -I_{z2}R_{Z2} = (I_p - I_n)R_{Z2} \tag{2.15}$$

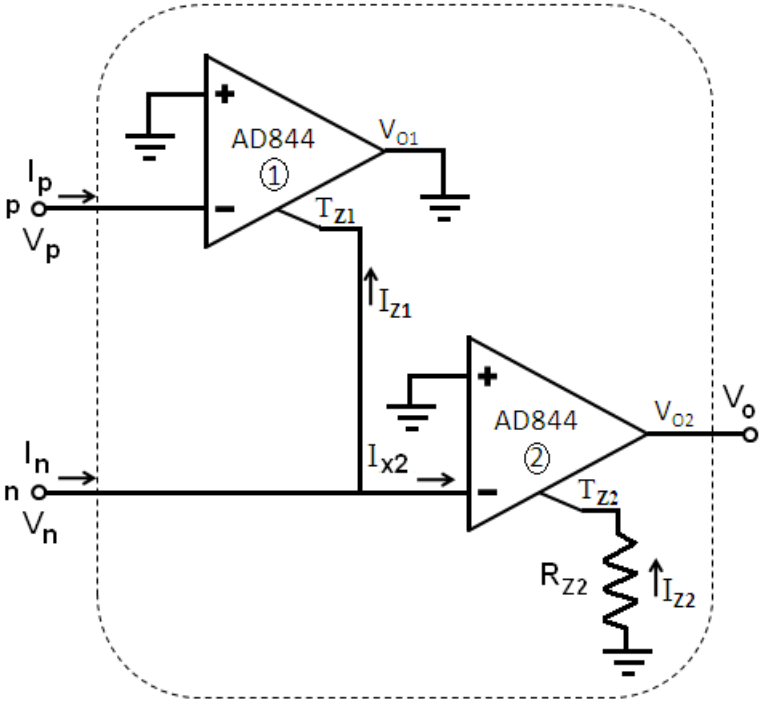


Fig. 2.7 OTRA realization using CFOA AD844 [35].

Ideally the input resistance at the x terminal of CFOA is zero and is infinite at the z terminal. However for the AD844 CFOA the input resistance R_x is around 50 Ω and R_z is around 3 MΩ [74].

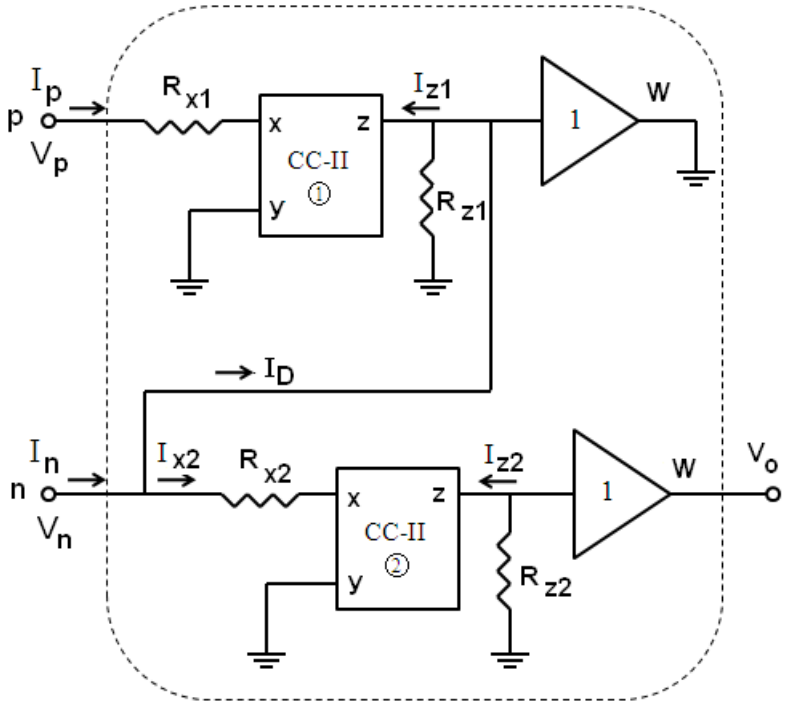


Fig. 2.8 Equivalent circuit of OTRA constructed with AD844 [66].

To investigate the effect of the parisitic resistances (R_x and R_z), the CFOAs have been replaced with current conveyors having finite input resistances (R_x) and finite resistance at its z terminal (R_z) in Fig. 2.7 and the equivalent circuit model [66] with parisitics for non ideal analysis is presented in Fig. 2.8. From Fig. 2.8 various currents can be computed as

$$I_{z1} = I_p \tag{2.16}$$

$$I_D = I_{z1}\left(\frac{R_{z1}}{R_{x2}+R_{z1}}\right) \tag{2.17}$$

$$I_{x2} = I_n - I_D \tag{2.18}$$

$$I_{z2} = I_{x2} \tag{2.19}$$

Ideally I_D should be equal to I_{z1}, which can be approximated only if $R_{z1}>>R_{x2}$, which is true for AD844. Also the approximation that the input terminals are virtually grounded will be true only if the external resistance at the input terminal of the OTRA is much larger than R_X. If these two conditions are satisfied the OTRA constructed with AD844 closely approximates an ideal OTRA.From (2.16), (2.17), (2.18) and (2.19) the output voltage V_o, taking into account the above mentioned approximations, can be calculated as

$$V_o = (I_p - I_n)R_{z2} \tag{2.20}$$

where R_{z2} is the transresistance gain of the OTRA.

2.5.2 Intgrated Circuit Implementation

Various integrated circuit implementations of OTRA [27], [36]–[40] are available in literature and are briefly described in this section. The OTRA implementation of [27] consists of a differential current controlled current source followed by a voltage buffer. The OTRA proposed in [36] is based on cascaded connection of the modified differential current conveyor (MDCC) [41] and a common source amplifier. The MDCC provides the current differencing operation whereas the common source amplifier provides the high gain stage [36]. The OTRA presented in [37] consists of a low voltage regulated cascode current mirror with a low voltage regulated cascode load as the core of the circuit, common source amplifiers gain boosting stage and level shifters followed by common source output stage [37]. The OTRA structure available in [38] is similar to [36] but uses smaller number of current mirrors than [36]. This reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Due to smaller number of transistors the power dissipation is also reduced. The CMOS OTRA realization in [39] uses same input stage as in [38] while a differential gain stage is used instead of the single common source amplifier. This differential stage reduces the DC offset current and increases the DC open loop transresistance gain. Yet another differential OTRA structure is proposed in [40]. It uses two symmetrically placed basic input cells consisting of four transistors each. Each cell forms two Class AB current mirror connections. This basic input unit is followed by four similar basic cells to decrease the process variation effects [40]. Gain is provided using three stages of differential amplifier. The non buffered, dual differential outputs are buffered through

unity gain configurations which are designed using CMOS op-amps [40]. This structure is a completely differential design.

2.6 CMOS OTRA [38] USED IN THIS WORK

This section describes the OTRA implementation used to verify the functionality of all the circuit structures proposed in this thesis. The CMOS based OTRA structure proposed in [38] has been reproduced in Fig. 2.9. The circuit operation is based on the assumptions that all the transistors (M1- M14) operate in saturation region and the transistor groups (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are perfectly matched. Transistors M8-M11 form current mirrors wherein the transistor M8 sets the reference current I_B which is repeated by M9-M11thus forcing equal currents in the transistors M1, M2 and M3. This provides the gate to source voltages of M1, M2 and M3 and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs M10-M11 and M12-M13 provide the current differencing operation, thus developing gate to source voltage for M14 which is connected as common source amplifier and provides the high gain.

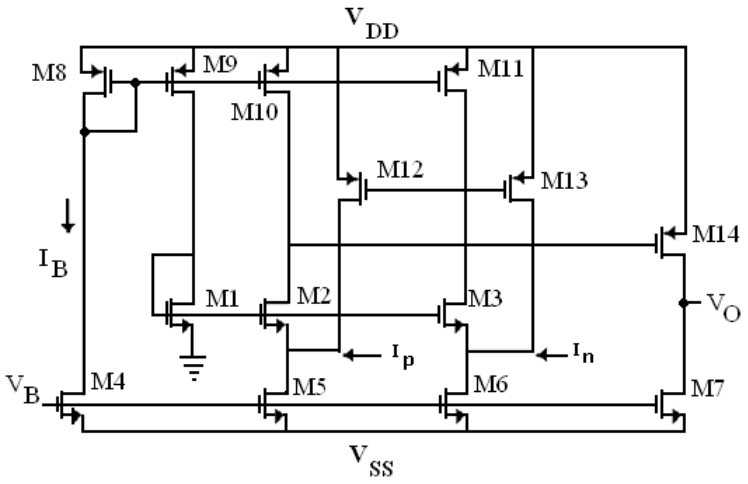


Fig. 2.9 CMOS Realization of OTRA Proposed in [38].

2.6.1 OTRA Characterization

The SPICE simulation is performed using 0.5µm, CMOS process parameters provided by MOSIS (AGILENT) which are listed in Table 2.1. Supply voltages for simulations are taken

as ± 1.5 V. Aspect ratios used for different transistors are same as in [38] and are given in Table 2.2.

Table 2.1: Device Model parameters.

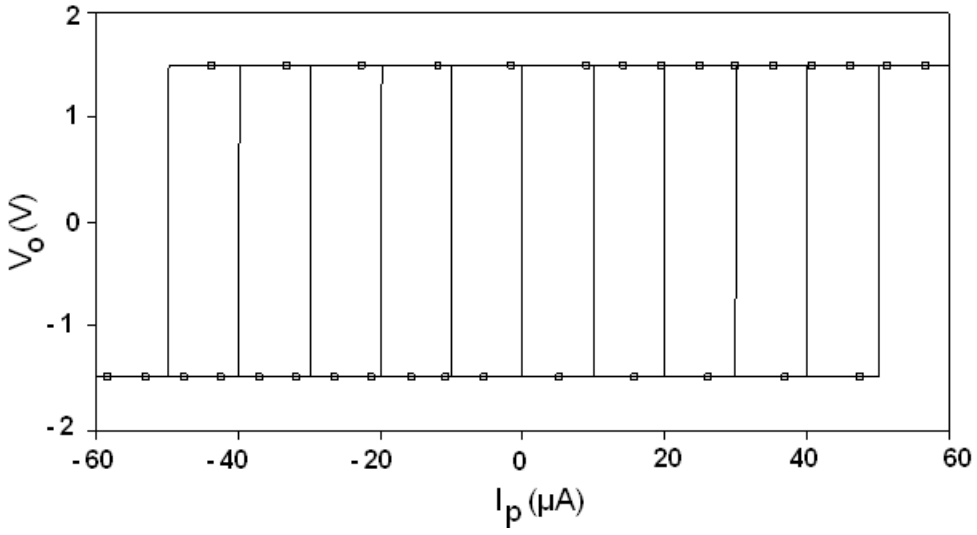
Device Type	Model parameters
NMOS	LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=.905 THETA=.129 GAMMA=.69 KAPPA=0.1 AF=1 WD=1.1E-7 CJ=76.4E-5 MJ=.357 CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11
PMOS	LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81 LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=.905 THETA=.12 GAMMA=.76 KAPPA=2 AF=1 WD=1.4E-7CJ=85E-5 MJ=.429 CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 NFS=.52E11

Table 2.2: Aspect ratio of the transistors in OTRA circuit.

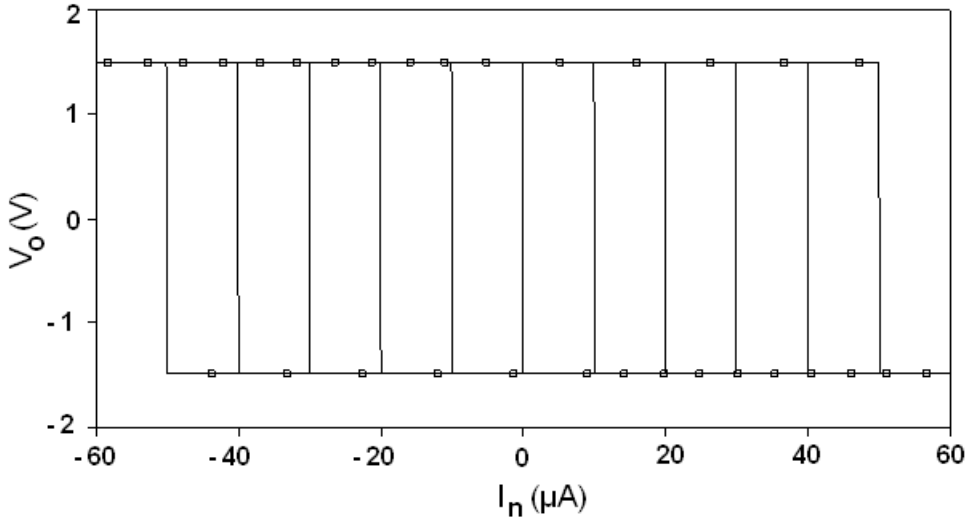
Transistor	W(µm)/L(µm)
M1-M3	100/2.5
M4	10/2.5
M5,M6	30/2.5
M7	10/2.5
M8-M11	50/2.5
M12,M13	100/2.5
M14	50/0.5

The DC transfer characteristic of the OTRA is shown in Fig. 2.10 which shows that input differential current range is -50 µA to 50 µA. The input resistance is plotted in Fig. 2.11 and

its value is observed to be 13 Ω. The AC characteristic is shown in Fig. 2.12. It shows that the DC open loop transresistance gain is 95.8 dBΩ. The gain bandwidth product equals 19.56 GHz Ω. The power dissipation of the circuit is 1.17 mW. These results are summarized in Table 2.3.



(a)



(b)

Fig. 2.10 DC Transfer Characteristics in (a) Noninverting, (b) Inverting configuration.

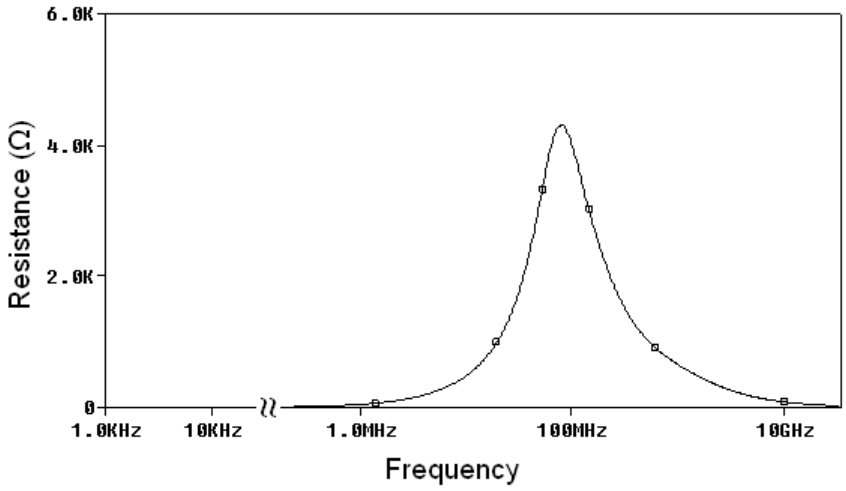


Fig. 2.11 Input resistances of the OTRA.

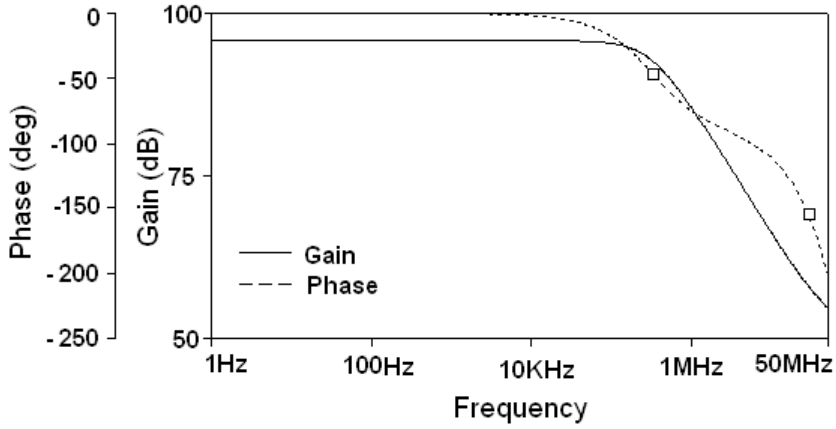


Fig. 2.12 Frequency Response of the open loop tranresistance gain.

Table 2.3: Simulated results of the circuits shown in Fig. 2.9.

Parameters	Results
Input current dynamic range	-50 to 50 μA
Input resistances R_p, R_n	≈ 13 Ω
DC open loop transresistance	95.8 dBΩ
Gain bandwidth product	19.56 GHzΩ
Transresistance gain B.W. (-3dB)	317 KHz
Total power dissipation	1.17 mW

2.7 BASIC CIRCUIT APPLICATIONS

This section describes the basic circuit applications of OTRA which have been used in this thesis.

2.7.1 Inverting Voltage Amplifier

An inverting amplifier is shown in Fig. 2.13. It consists of an OTRA and two resistors R_1 and R_2 where R_2 is connected from output to negative input terminal n, thus closing the loop around OTRA. The current at terminal n can be computed as

$$i_n = \frac{v_{in}}{R_1} + \frac{v_o}{R_2} \tag{2.21}$$

And the current at terminal p can be expressed as

$$i_p = 0 \tag{2.22}$$

Assuming the OTRA to be ideal, voltage gain of the amplifier can be computed by equating the currents of p and n terminal resulting in

$$\frac{v_{in}}{R_1} + \frac{v_o}{R_2} = 0 \tag{2.23}$$

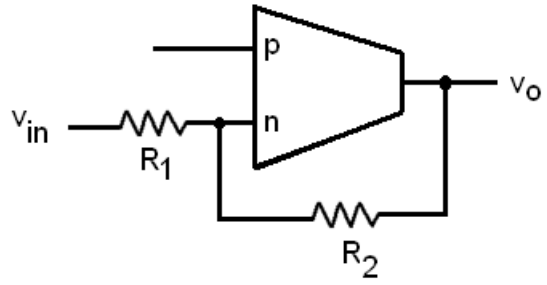


Fig. 2.13 Inverting amplifier.

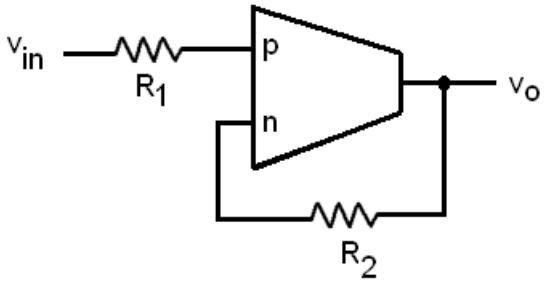


Fig. 2.14 Noninverting amplifier.

Thus the close loop inverting gain can be computed to be

$$\frac{v_o}{v_{in}} = -\frac{R_2}{R_1} \tag{2.24}$$

2.7.2 Noninverting Voltage Amplifier

A noninverting amplifier consists of an OTRA and two resistors R_1 and R_2 as shown in Fig. 2.14. The current at terminal n and p can respectively be computed as

$$i_n = \frac{v_o}{R_2} \tag{2.25}$$

$$i_p = \frac{v_{in}}{R_1} \tag{2.26}$$

Assuming the OTRA to be ideal, voltage gain of the amplifier can be computed as

$$\frac{v_{in}}{R_1} = \frac{v_o}{R_2} \tag{2.27}$$

Thereby resulting in voltage gain as

$$\frac{v_o}{v_{in}} = \frac{R_2}{R_1} \tag{2.28}$$

2.7.3 The Summing Amplifier

An OTRA based summer is shown in Fig. 2.15 and can be used as a weighted summer. The circuit makes use of a single OTRA, a feedback resistor R_F and N feed- in resistors (R_1 to R_N) through which input signals v_1 to v_N are applied. By equating the current at the inverting and the non inverting terminal, the output voltage can be obtained as given by (2.29) which can be further simplified to (2.30) if $R_1 = R_2 = \ldots. = R_N = R_F = R$.

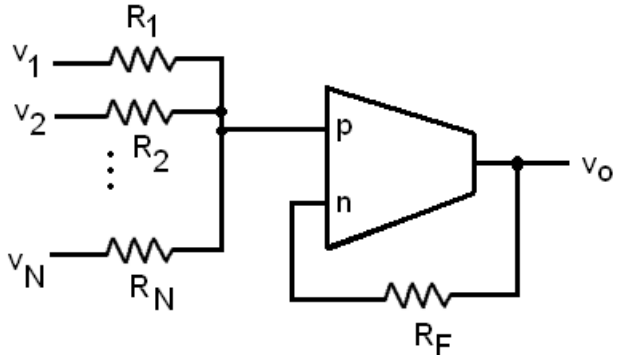


Fig. 2.15 The summing amplifier.

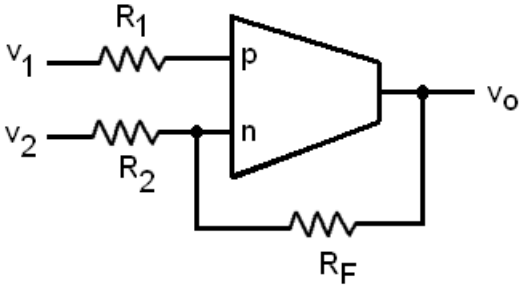


Fig. 2.16 The difference amplifier.

$$v_O = \frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \cdots \frac{R_F}{R_N} v_N \quad (2.29)$$

$$v_O = v_1 + v_2 + \cdots + v_n \quad (2.30)$$

2.7.4 The Difference Amplifier

Considering the OTRA to be ideal the output voltage for the circuit shown in Fig. 2.16, can be expressed as

$$v_O = \frac{R_F}{R_1} v_1 - \frac{R_F}{R_2} v_2 \quad (2.31)$$

Thus the circuit can be used as a difference amplifier with a gain of $^{R_F}/_{R}$ if $R_1 = R_2 = R$ and the output voltage can be written as

$$v_O = \frac{R_F}{R} (v_1 - v_2) \quad (2.32)$$

The circuit of Fig. 2.16 can also be used as a subtractor if $R_1 = R_2 = R_F$ and the ouput voltage can be expressed as

$$v_O = (v_1 - v_2) \quad (2.33)$$

2.7.5 Lossy Integrator

The circuit shown in Fig. 2.17(a) represents an inverting lossy integrator. Assuming the OTRA to be ideal and using the concept of current feedback, the transfer function can be computed as

$$\frac{v_o}{v_{in}} = \frac{-\left(^{R_F}/_{R}\right)}{1+sCR} \quad (2.34)$$

From (2.34) the DC gain (K) of the integrator can be found to be

$$K = -\frac{R_F}{R} \quad (2.35)$$

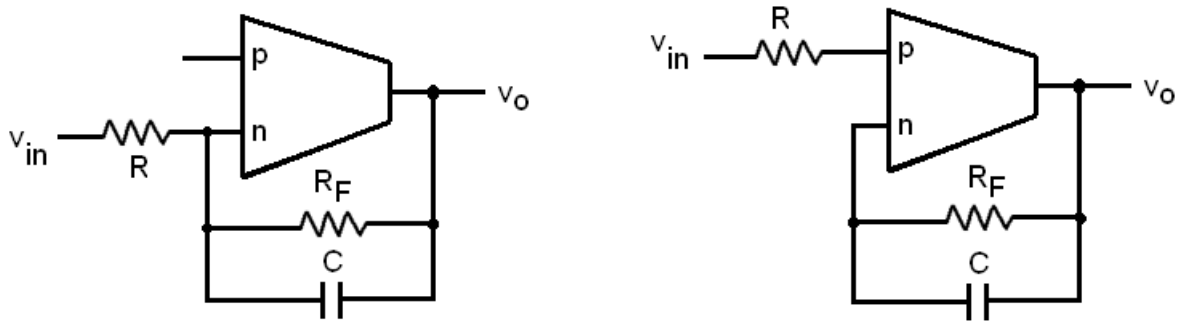
And the 3-dB frequency (ω_0) is observed to be

$$\omega_0 = \frac{1}{CR} \quad (2.36)$$

Applying input voltage at p terminal of OTRA a noninverting integrator can be realized as depicted in Fig. 2.17(b) and its transfer function can be expressed as

$$\frac{v_o}{v_{in}} = \frac{\left({}^{R_F}/_{R}\right)}{1+sCR} \tag{2.37}$$

having a non inverting DC gain of $K = {}^{R_F}/_{R}$ and ω_0 being same as (2.36).



(a) (b)

Fig. 2.17 Lossy integrator configurations (a) Inverting. (b) Noninverting.

2.8 ACTIVE RESISTOR REALIZATION USING OTRA

It is well know that the linear passive resistor consumes a large chip area as compared to the linear resistor implementation using transistors operating in non-saturation region. The current differencing property of the OTRA allows the resistors connected to the input terminals of OTRA to be implemented using MOS transistors with complete non-linearity cancellation [36].

The circuit configuration of Fig. 2.18 shows MOS based resistor realization. Assuming that M_a and M_b are matched transistors and operating in ohmoc region the currents I_a and I_b [75] can be expressed as

$$\begin{aligned} I_a &= K_n(V_a - V_T)(V_{DSa}) + x_1 V_{DSa}^2 + x_2 V_{DSa}^3 + \cdots \\ &= K_n(V_a - V_T)(V_1 - V_2) + x_1(V_1 - V_2)^2 + x_2(V_1 - V_2)^3 + \cdots \end{aligned} \tag{2.38}$$

$$I_b = K_n(V_b - V_T)(V_{DSb}) + x_1 V_{DSb}^2 + x_2 V_{DSb}^3 + \cdots$$
$$= K_n(V_b - V_T)(V_1 - V_2) + x_1(V_1 - V_2)^2 + x_2(V_1 - V_2)^3 + \cdots \quad (2.39)$$

where $K_n = \mu\, C_{OX}\, \frac{W}{L}$ and μ, C_{OX} and W/L represent standard transistor parameters.

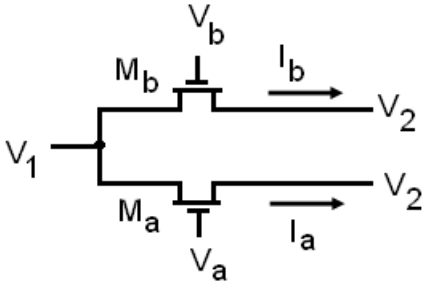


Fig. 2.18 MOS based resistor realization [36].

Since the transistors M_a and M_b are perfectly matched and have equal drain to source voltages, the difference of the currents flowing in the two transistors can be expressed as

$$(I_a - I_b) = K_n(V_a - V_b)(V_1 - V_2)$$
$$= G(V_1 - V_2) \quad (2.40)$$

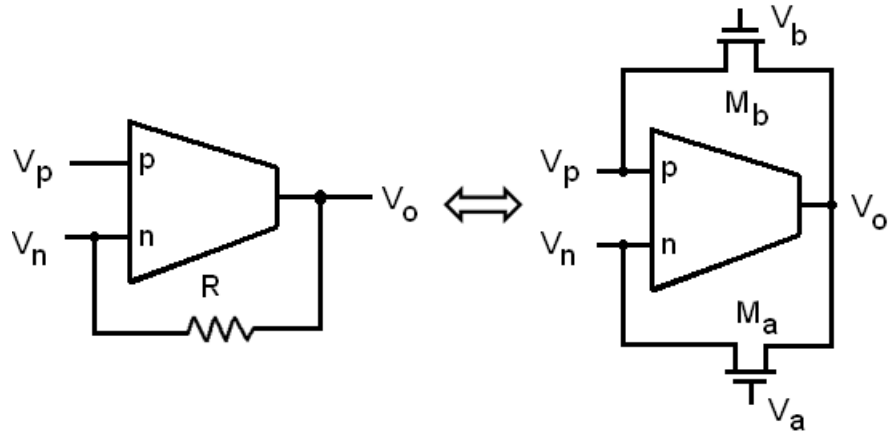


Fig. 2.19 MOS implementation of a linear resistance connected between negative and output terminals of OTRA.

From (2.40) it can be observed that and a resistor $R = {}^{1}/_{G}$ can be implemented, cancelling both even and odd non-linearities. The value of the resistance may be computed to be

$$R = \frac{1}{K_n(V_a - V_b)} \tag{2.41}$$

K_n is determined through model parameters and W/L ratio of the transistors used to implement the resistor.Once K_N value is fixed the resistance value can be adjusted by appropriate choice of gate voltages thereby making it electronically tunable.

2.9 CONCLUDING REMARKS

In this chapter an ideal OTRA along with its terminal characterstics is presented. Nullor based model of OTRA has also been described. Nonidealities of practically realized OTRA are taken into consideration which would be helpful in performance evaluation of any OTRA based circuit. A brief on existing literature on OTRA realization is presented. The OTRA CMOS realization proposed in [38] is explained and characterized using SPICE. Few basic applications of the OTRA are also described which can be readily used in designing the complex applications. Finally MOS based resistor realization using the current differencing property of OTRA has been discussed which helps in making circuits fully integrable and electronically tunable.

CHAPTER – 3

ACTIVE INDUCTANCE SIMULATION

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey Sajal K. Paul A. Singh B. Sriram, and K. Trivedi **"New Topologies of Lossless Grounded Inductor Using OTRA"** Journal of Electrical and Computer Engineering Volume 2011, Article ID 175130, 6 pages, doi:10.1155/2011/175130.

2. Rajeshwari Pandey, Neeta Pandey, Ajay Singh, B.Sriram, Kaushalendra Trivedi**, "Novel grounded inductance simulator using single OTRA,"** Int. J. Circuit Theory and Application doi : 10.1002/cta. 1905.

3. Rajeshwari Pandey, Neeta Pandey, Ajay Singh, B. Sriram, Kaushalendra Trivedi **"Grounded Immittance Simulator Using Single OTRA with a Signal Processing Application,"** International Conference on electronics and Computer Technology, (ICECT-2011), pp.404- 406, April 2011.

3.1 INTRODUCTION

Inductors find application in areas such as filter design, oscillator design, phase shifters and parasitic element cancellation. But realization of a spiral inductor in an integrated circuit has some drawbacks in terms of the usage of space, weight, cost and tunability. This resulted in design of inductorless active RC filters, oscillators etc., thus making active inductance simulation an important research topic in active network synthesis. The simulated active inductors only mimic some properties of the real inductors and cannot replace them in all possible applications of inductors. Despite this limitation, their usages are wide spread in analog design which leads the analog designers to explore this area to the extent possible.

This chapter deals with the realization of both lossy and lossless active grounded inductance simulation using OTRA. The chapter begins with the design description of lossy grounded inductance which is followed by design details concerning lossless grounded inductance simulation. A brief account of existing literature on OTRA based grounded inductance simulation is presented before describing the proposed work.

3.2 LITERATURE REVIEW ON INDUCTANCE SIMULATION

Review of earlier work suggests that both lossy and lossless grounded inductor topologies using OTRA have been reported in open literature. A number of grounded parallel lossy inductor topologies using single OTRA were proposed in [59], [60], which can realize L parallel with R, (-L) parallel with R, (-L) parallel with (±R), (±L) parallel with R; and L and C parallel with (±R). Two topologies which simulate grounded parallel lossy inductor using two OTRAs were proposed in [62]. These topologies realized L parallel with R and (-L) parallel with R. A lossless grounded inductor using two OTRAs was also proposed in [62] apart from lossy inductor topologies. A lossless grounded inductor topology using two OTRAs was presented in [61] and this inductor was used to design an LC oscillator. A lossless grounded inductance simulator using an OTRA and a buffer [63] came up recently in 2011. This topology could also simulate grounded frequency-dependent negative-resistance (FDNR). Actively simulated negative inductors play an important role in

cancellation/compensation of parasitic inductances and can also be used in microwave circuits for impedance matching. A single OTRA based generic grounded negative inductance simulator was proposed in [64] from which four different topologies could be deduced.

3.3 LOSSY GROUNDED INDUCTOR

This section presents the design of proposed lossy grounded inductor which can realize inductance types (±L) parallel with R. Two application example of the proposed lossy inductor are also discussed.

3.3.1 Proposed Circuit

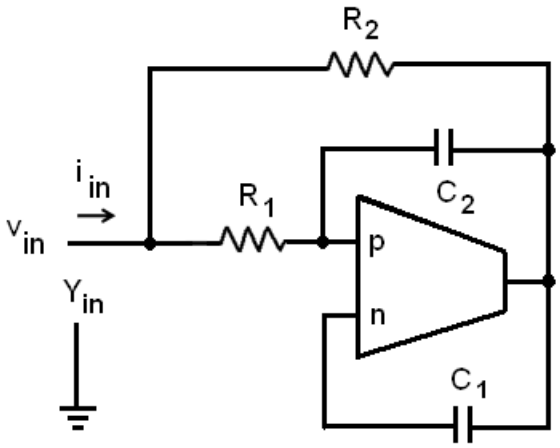


Fig. 3.1 Lossy grounded inductor.

The proposed grounded immittance simulator is shown in Fig. 3.1. Using routine analysis of the circuit the expression for input admittance Y_{in} can be written as

$$Y_{in} = G_1 + G_2 - \frac{G_1 G_2}{s(C_1 - C_2)} \tag{3.1}$$

which represents an impedance of type $L_{eq} \| R_{eq}$, where

$$R_{eq} = \frac{1}{G_1+G_2},\ L_{eq} = \frac{(C_1-C_2)}{G_1G_2} \text{ and } \quad R_i = \frac{1}{G_i} \tag{3.2}$$

Proper choice of C_1 and C_2 may result in realization of inductance type (+L) parallel with R or inductance type (-L) parallel with R.

3.3.2 Nonideality Analysis

In analysis so far, ideal characteristics of the OTRA have been considered. However, the effect of the parasitics needs to be taken into consideration for performing nonideality analysis. Using the nonideal model of OTRA as shown in Fig. 2.8, the circuit of Fig. 3.1 can be redrawn as shown in Fig. 3.2.

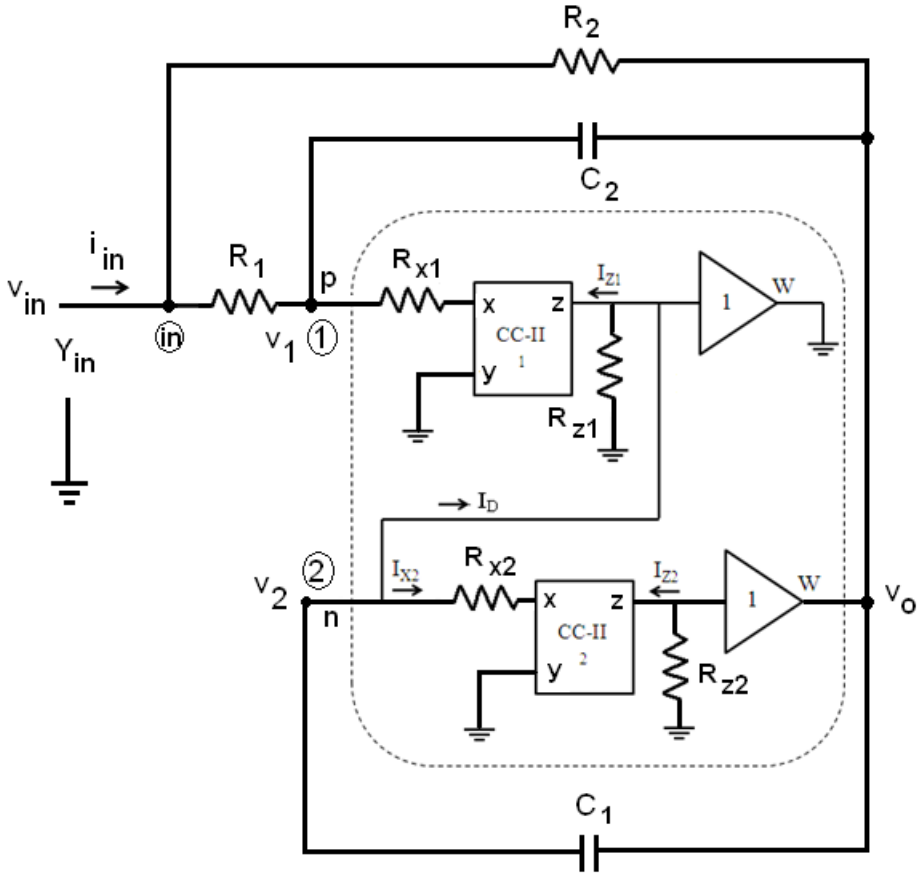


Fig. 3.2 Nonideal model of the proposed lossy inductor.

Nodal equations at input node and nodes 1 and 2 can respectively be written as

$$\frac{(v_{in}-v_1)}{R_1} = i_{in} + \frac{(v_o-v_{in})}{R_2} \tag{3.3}$$

$$\frac{(v_{in}-v_1)}{R_1} + (v_o-v_1)sC_2 = \frac{v_1}{R_{x1}} \tag{3.4}$$

$$(v_o-v_2)\, sC_1 = \frac{v_2}{R_{z1} \| R_{x2}} \tag{3.5}$$

Equations (3.3), (3.4) and (3.5) can be solved, assuming $R_{x1} = R_{x2} = R_x$ and using the relation $R_x << R_{z1}$, resulting in

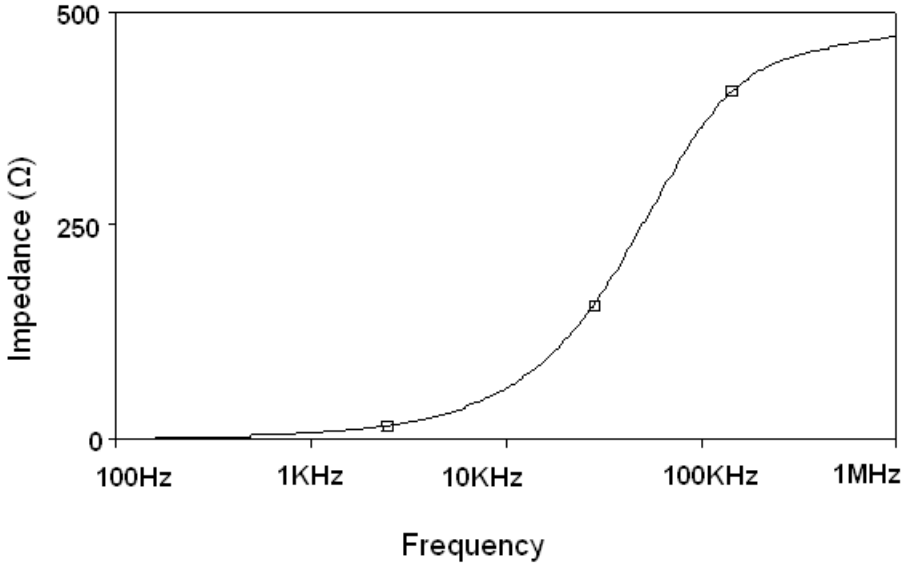
$$i_{in} = (G_1 + G_2)\, v_{in} - \frac{G_1 G_2 (1+sC_1 R_x (1+R_2))}{s(C_1-C_2)}\, v_{in} \tag{3.6}$$

From (3.6) the input admittance can be computed to be

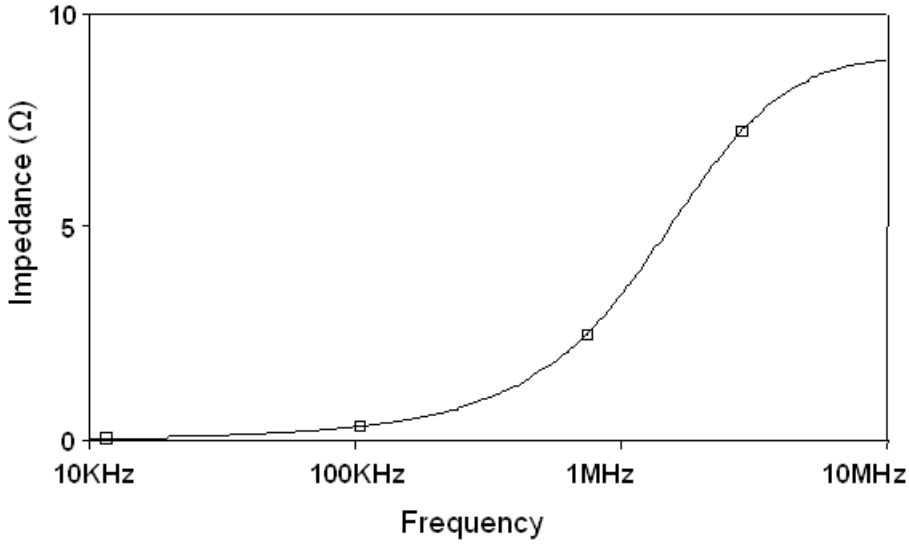
$$Y_{in}(s)\Big|_n = (G_1 + G_2) - \frac{G_1 G_2}{s(C_1-C_2)} (1 + sC_1 R_x (1 + R_2)) \tag{3.7}$$

3.3.3 Simulation Results

The functionality of the proposed simulated lossy inductor is verified through SPICE simulation using CFOA based realization of OTRA as discussed in section 2.4.1. Impedance magnitude response of the simulated lossy inductor having L_{eq} = 1 mH and R_{eq} = 500 Ω, realized using component values as C_1 = 2 nF, C_2 = 1 nF, and $R_1 = R_2$ = 1 KΩ is given in Fig. 3.3(a). Impedance magnitude response of another instance of lossy inductor with L_{eq} = 1 µH and $R_{eq} \approx$ 10 Ω, implemented through C_1 = 2 nF, C_2 = 1 nF, R_1 = 100 Ω and R_2 = 10 Ω; is depicted in Fig. 3.3(b). It is observed that the impedance value remains within ± 10% of the theoretically calculated value in the frequency range of 100 Hz – 100 KHz for 1 mH. For inductance value of 1 µH the frequency range is found to be 10 KHz - 1.5 MHz. It indicates that the frequency range, over which the inductance value remains almost constant, decreases with increasing value of simulated inductance.



(a)



(b)

Fig.3.3 Impedance magnitude responses (a) L_{eq} = 1mH, R_{eq} = 500Ω,
(b) L_{eq} = 1μH, R_{eq} = 10 Ω.

3.3.4 Signal Processing Applications

To show the application of the proposed immittance simulator a current mode filter, giving

high pass and band pass responses, and an LC oscillator are designed. The workability of these applications is verified through SPICE simulation.

3.3.4.1 Current Mode Filter

The designed current mode filter configuration is shown in Fig. 3.4. The simulated lossy inductor replaces the parallel R L circuit. Current transfer functions can be written as

$$\frac{i_R}{i_{in}} = \frac{s\frac{(G_{eq}+G)}{C}}{s^2 + s\frac{(G+G_{eq})}{C} + \frac{1}{CL_{eq}}} \tag{3.8}$$

$$\frac{i_C}{i_{in}} = \frac{s^2}{s^2 + s\frac{(G+G_{eq})}{C} + \frac{1}{CL_{eq}}} \tag{3.9}$$

where G_{eq} = 1/ R_{eq} and G = 1/ R. The filter functions can be characterized by following parameters

$$\omega_0 = \frac{1}{\sqrt{CL_{eq}}}, \quad Q_0 = \frac{1}{(G+G_{eq})}\sqrt{\frac{C}{L_{eq}}} \tag{3.10}$$

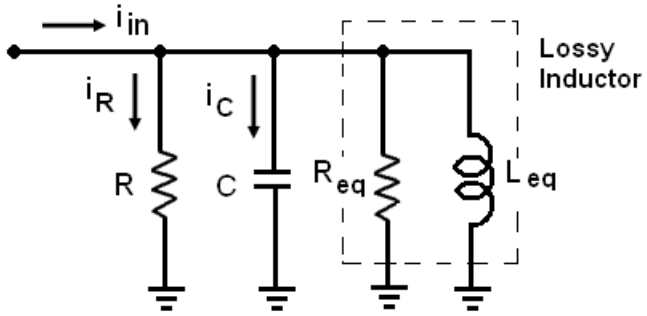


Fig. 3.4 Current Mode Filter.

To verify the functionality of the proposed current mode filter a design having f_0 = 79.6 KHz and Q_0 = 0.25 is developed, for which the capacitance value C = 1nF is chosen and accordingly L_{eq} is computed to be 4 mH and R = 1 KΩ. For realizing L_{eq} = 4 mH, the values of capacitive components are chosen as C_1 = 2 nF and C_2 = 1 nF and the resistive

components are calculated as $R_1 = R_2 = 2$ KΩ. The simulated frequency responses for the current mode BP and HP filters are shown in Fig. 3.5 and are found to be in close agreement with the theoretical predictions.

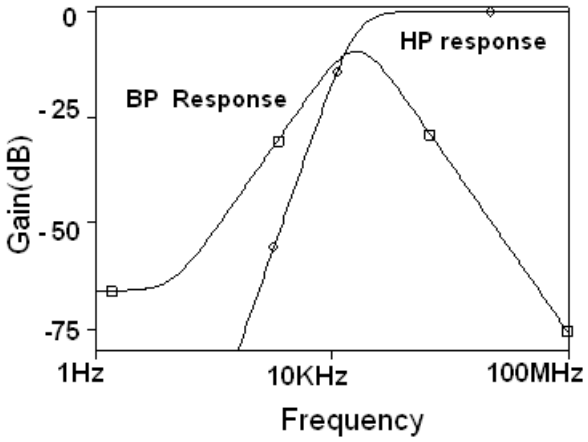


Fig. 3.5 Frequency Response of current mode filter.

3.3.4.2 Realization of an LC Oscillator

An LC oscillator is designed using new simulated inductor and is shown in Fig. 3.6. From the routine analysis of the circuit various current equations can be written as

$$I_p = \frac{v_1}{R_1}, I_n = \frac{v_o}{R_2} \tag{3.11}$$

Therefore v_1 can be expressed as

$$v_1 = \frac{R_1}{R_2} v_o \tag{3.12}$$

Nodal equation at node 1 can be written as

$$\frac{v_1}{R_1} + \frac{v_1}{Z} + \frac{(v_1 - v_o)}{R_3} = 0 \tag{3.13}$$

where $Z = X_C \| X_{L_{eq}} \| R_{eq} = \frac{R_{eq} L_{eq}}{s^2 C R_{eq} L_{eq} + s L_{eq} + R_{eq}}$ (3.14)

Substituting v_1 and Z from (3.12) and (3.14) respectively in (3.13) results

$$s^2 + \frac{s}{CR_{eq}} + \frac{1}{CL_{eq}} = \frac{R_2 - (R_1 + R_3)}{CR_1R_3} \tag{3.15}$$

From (3.15) the condition of oscillation (CO) and frequency of oscillation (FO) can be expressed as

CO: $R_2 = (R_1 + R_3)$ (3.16)

FO: $\omega_0 = \frac{1}{\sqrt{CL_{eq}}}$ (3.17)

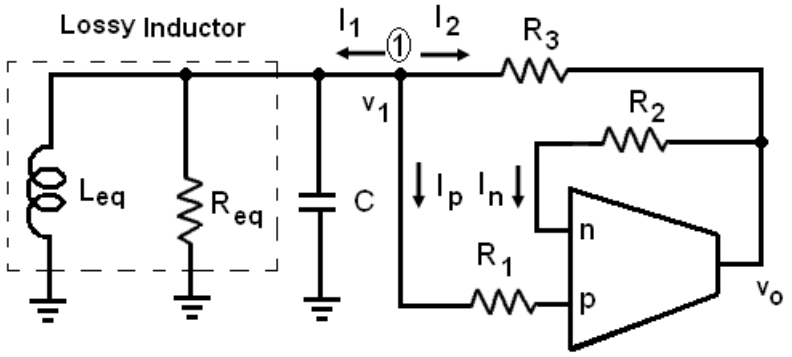


Fig. 3.6 LC oscillator using realized lossy inductor.

A typical simulation for element values R_1 = 4 KΩ, R_2 = 8 KΩ, R_3 = 4 KΩ, R_{eq} = 16 KΩ, L_{eq} = 0.64 mH and C = 10 pF is shown in Fig. 3.7. The simulated f_o is observed to be 1.92 MHz as against the theoretical value of 1.99 MHz and are in close agreement.

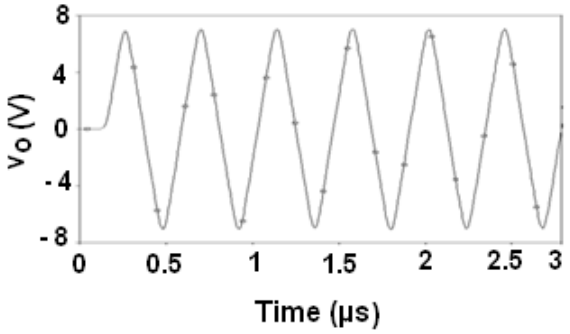


Fig. 3.7 Simulation result of LC oscillator.

3.4 LOSSLESS GROUNDED INDUCTANCE SIMULATION

This section deals with OTRA based lossless grounded active inductance simulation and describes two different design topologies involving (i) two OTRAs and (ii) single OTRA.

3.4.1 Two OTRA Based Circuits

Two different topologies of lossless grounded inductor using two OTRAs, in addition to already existing structures in the literature [61], [62] are proposed in this section and are shown in Fig. 3.8 (a) and (b) respectively. The input admittance of the circuit of Fig. 3.8 (a) can be computed as

$$Y_{in}(s) = (G_1 + G_3 + G_5 - \frac{G_1 G_5}{G_4}) + \frac{G_2 G_3 G_5}{sC_1 G_4} \tag{3.18}$$

The input admittance Y_{in} will be purely inductive if following condition is met

$$G_1 + G_3 + G_5 = \frac{G_1 G_5}{G_4} \tag{3.19}$$

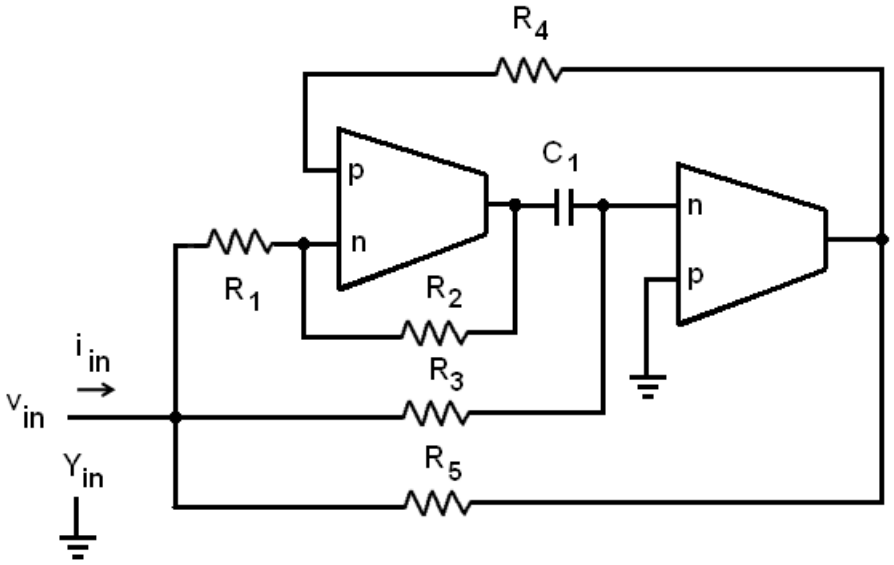
Similarly for inductance topology of Fig. 3.8 (b) input admittance is given by

$$Y_{in}(s) = (G_1 + G_2 + G_4 - \frac{G_2 G_4}{G_3}) + \frac{G_1 G_2 G_5}{sC_1 G_3} \tag{3.20}$$

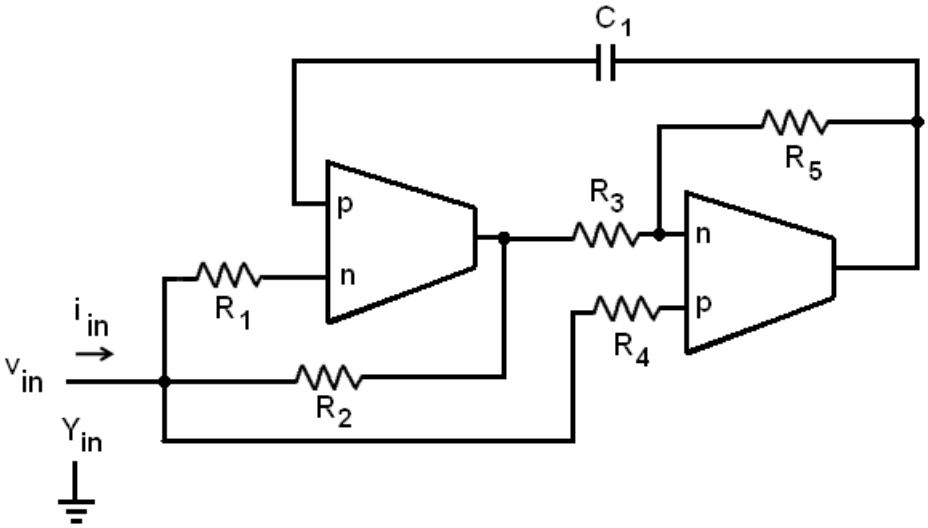
It will be purely inductive provided

$$G_1 + G_2 + G_4 = \frac{G_2 G_4}{G_3} \tag{3.21}$$

The equivalent inductance values along with conditions are summarized in Table 3.1. It is clear from Table 3.1 that for both the topologies the inductance value can be controlled independent of condition of realization.



(a)



(b)

Fig. 3.8 Lossless grounded inductors. (a) Topology-I. (b) Topology-II.

Table 3.1: Inductors realized by the topologies shown in Fig. 3.8.

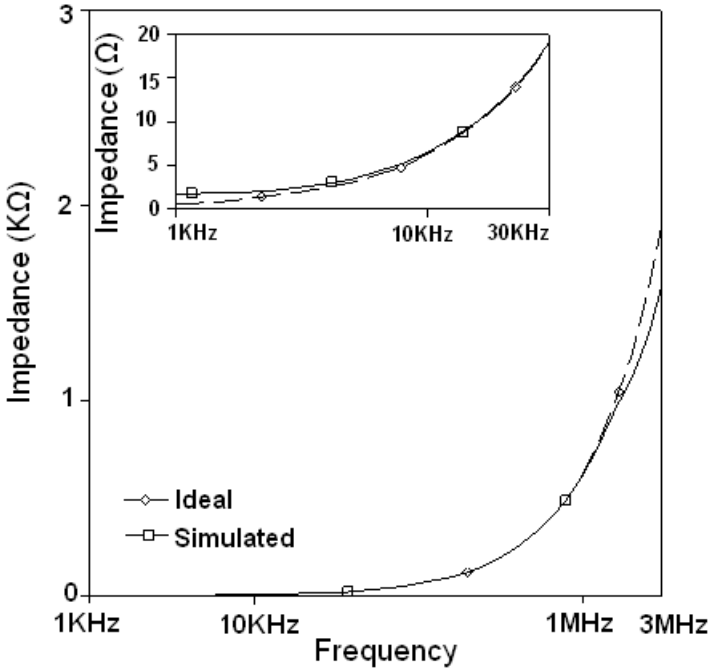
Figure	Condition	L_{eq}	Non Interactive Control
Fig.2(a)	$G_1 + G_3 + G_5 = \frac{G_1 G_5}{G_4}$	$\frac{C_1 G_4}{G_2 G_3 G_5}$	Independent Control on condition through G_1 and on value through G_2.
Fig.2(b)	$G_1 + G_2 + G_4 = \frac{G_2 G_4}{G_3}$	$\frac{C_1 G_3}{G_1 G_2 G_5}$	Independent Control on condition through G_4 and on value through G_5.

3.4.1.1 Simulation Results

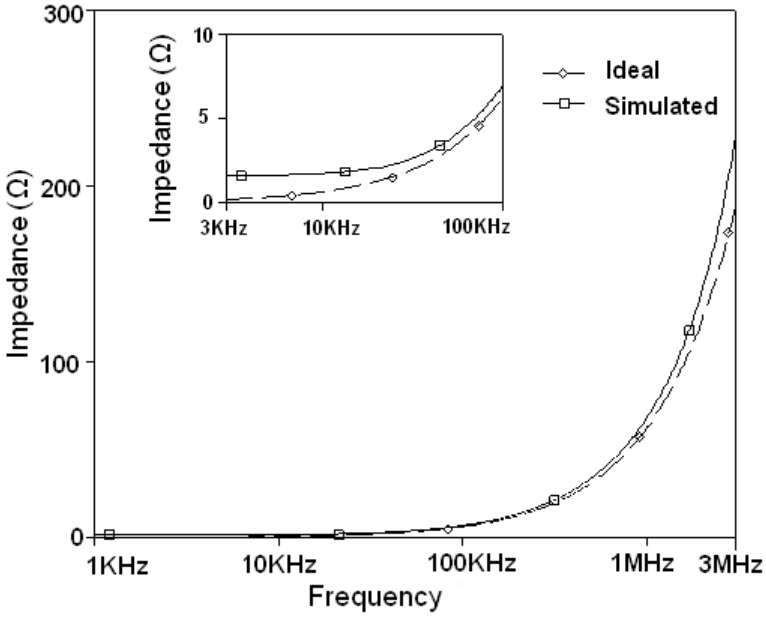
Two inductor instances of value L_{eq} = 100 µH and L_{eq} = 10 µH are simulated using inductor topologies of Fig. 3.8 (a) and (b) respectively. To obtain these inductance values the component values are chosen as $R_1 = R_2 = R_3 = R_5$ = 1 KΩ, R_4 = 3 KΩ, C_1 = 300 pF for L_{eq} = 100 µH and $R_1 = R_2 = R_4 = R_5$ = 1 KΩ, R_3 = 3 KΩ, C_1 = 30 pF for L_{eq} = 10 µH respectively. The CMOS schematic of OTRA shown in Fig. 2.9 is used for simulation. The ideal and simulated impedance magnitude responses of 100 µH and 10 µH inductors are shown in Fig 3.9 (a) and (b) respectively. The inset depicts the enlarged view of magnitude response in lower frequency range. It is observed that the inductance instance of 100 µH remains well within the ± 10% of the designed value in the frequency range of 3 KHz - 1.2 MHz whereas that of 10 µH in the frequency range of 10 KHz - 1.2 MHz.

3.4.1.2 Applications

In this section some applications of the proposed topologies have been presented. Both the topologies may be used for constructing filter and oscillator circuits.



(a)

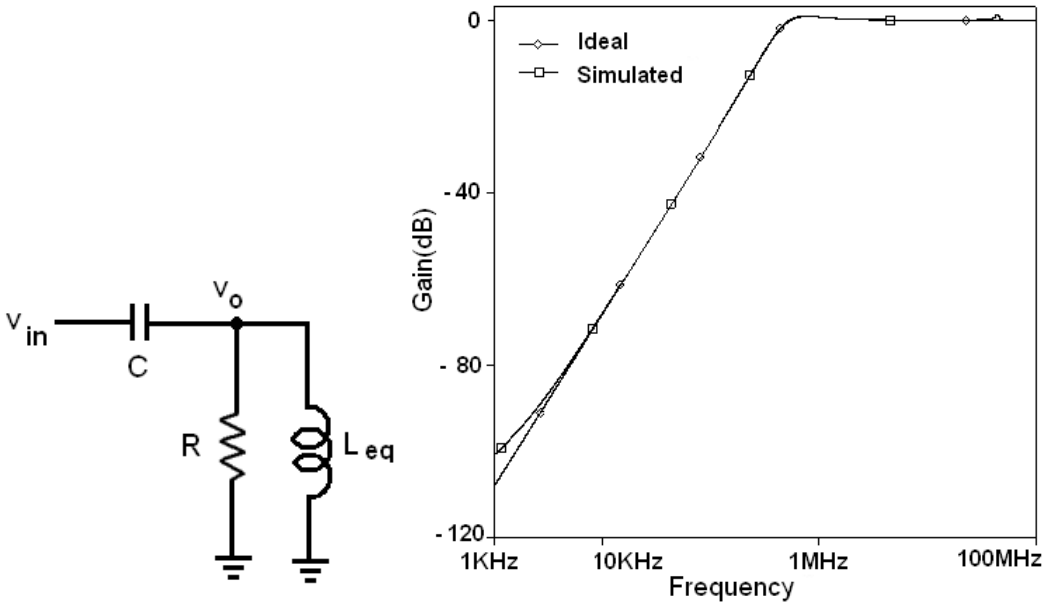


(b)

Fig. 3.9 Impedance magnitude response (a) 100 µH. (b) 10 µH.

3.4.1.2.1 High Pass Filter

A high pass filter, as shown in Fig. 3.10 (a), can be constructed using proposed inductors.



(a) (b)

Fig. 3.10 (a) Simulated Inductance based HPF. (b) Frequency response of HPF.

The transfer function for high pass response is obtained as

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + \frac{s}{CR} + \frac{1}{L_{eq}C}} \tag{3.22}$$

and is characterized by

$$\omega_0 = \frac{1}{\sqrt{C\,L_{eq}}} \text{ and } \quad Q_0 = R\sqrt{\frac{C}{L_{eq}}} \tag{3.23}$$

The functionality of the HPF is verified by deigning a filter having lower cutoff frequency of 503.2 KHz and $Q_0 = 1$. The component values for the design are chosen as $L_{eq} = 0.1$ mH and C = 1 nF. The value of resistor R is computed to be 300 Ω. Inductor topology of Fig. 3.8(a) is

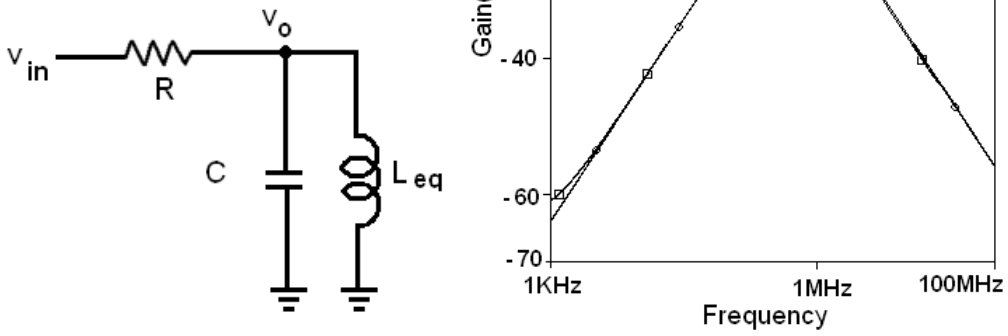
used for realizing the grounded inductor of value 0.1 mH, with component values as C_1 = 300 pF and $R_1 = R_2 = R_3 = R_5$ = 1 KΩ, R_4 = 3 KΩ. The simulated frequency response of the HPF using SPICE is depicted in Fig. 3.10(b). Simulated value of lower cut off frequency is obtained as 505 KHz which is in close agreement to the theoretical value of 503.2 KHz.

3.4.1.2.2 Band Pass Filter

The proposed inductor topologies may also be used to obtain band pass response using the circuit given in Fig. 3.11(a). Using routine analysis the transfer function for band pass response can be obtained as

$$\frac{v_o}{v_{in}} = \frac{\frac{s}{CR}}{s^2 + \frac{s}{CR} + \frac{1}{L_{eq}C}} \tag{3.24}$$

where $\omega_0 = \frac{1}{\sqrt{C\,L_{eq}}}$ and $Q_0 = R\sqrt{\frac{C}{L_{eq}}}$ (3.25)



(a) (b)

Fig. 3.11(a) Simulated Inductance based BPF. (b) Frequency response of BPF.

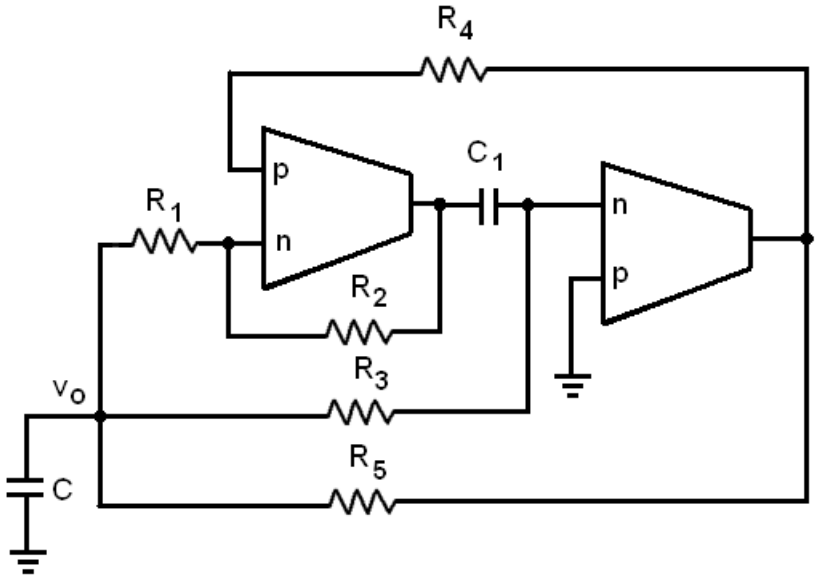
This theoretical proposition is verified through simulations using the topology of Fig. 3.8 (b). A BPF is designed having center frequency of 503.29 KHz. The component values are computed as R = 1 KΩ and C = 1 nF for a chosen value of L_{eq} = 0.1 mH. The value of L_{eq} = 0.1 mH is obtained using component values of $R_1 = R_2 = R_4 = R_5$ = 1 KΩ, R_3 = 3 KΩ, and C_1 = 300 pF. The simulated frequency response of the BPF is depicted in Fig. 3.11(b). It may be observed that the simulated and theoretical responses closely follow each other.

3.4.1.2.3 LC Oscillator

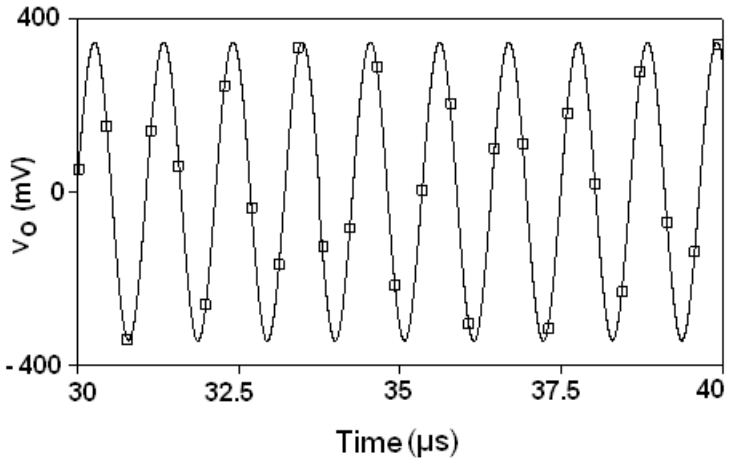
An LC Oscillator can also be realized using the proposed inductor topologies. Fig. 3.12 (a) shows the schematic of an LC oscillator using topology of Fig. 3.8 (a) for which the condition of oscillation (CO) and frequency of oscillation (FO) can be computed as

$$\text{CO: } G_1 + G_3 + G_5 = \frac{G_1 G_5}{G_4} \tag{3.26}$$

$$\text{FO: } \omega_0 = \frac{1}{\sqrt{L_{eq}C}} = \sqrt{\frac{R_4}{CC_1R_2R_3R_5}} \tag{3.27}$$



(a)



(b)

Fig.3.12 (a) Simulated inductance based LC oscillator. (b) Output of LC oscillator.

Figure 3.12(b) show simulated output of oscillator for L_{eq} = 0.1 mH and C = 300 pF. Simulated frequency of oscillation is found to be 860 KHz as against the calculated value of 876.2 KHz with % error of 1.85%.

3.4.1.3 Experimental Verification

The functionality of proposed inductor topologies is also confirmed experimentally. The OTRA is realized using two CFOAs (IC AD844AN) for experimental work. The HPF of Fig. 3.10 (a) is prototyped with R = 680 Ω, C = 1 nF and L_{eq} = 1 mH. Inductor topology of Fig 3.8 (a) is used with component values $R_1 = R_2 = R_3 = R_5$ = 1 KΩ, R_1 = 3 KΩ and C_1 = 3 nF, to simulate L_{eq} = 1 mH. Theoretical, simulated and experimental frequency responses are shown in Fig. 3.13 and it is observed that the experimental response is almost in agreement with the theoretical and simulated responses.

The oscillator circuit of Fig. 3.12(a) is also tested experimentally. The output waveform observed on oscilloscope is shown in Fig. 3.14. The observed frequency of oscillation is found to be 872.5 KHz, which is in close agreement to theoretically calculated value of 876.2 KHz.

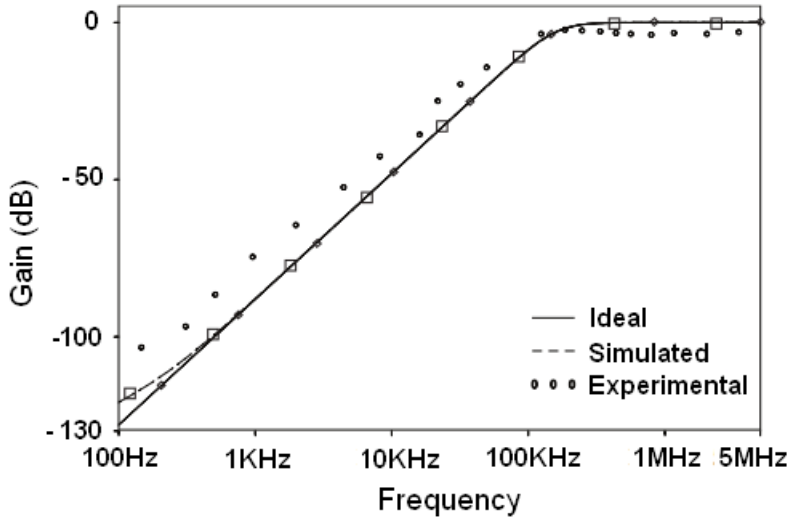


Fig. 3.13 Ideal, simulated and experimental frequency responses of HPF of Fig. 3.10(a).

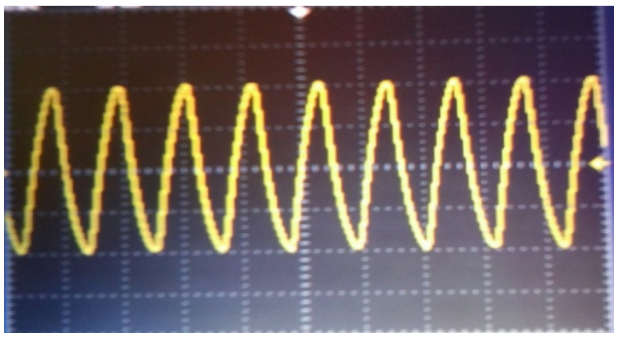


Fig. 3.14 Experimental output of LC oscillator.

3.4.2 Single OTRA Based Circuit

In this section a grounded simulated inductor topology based on a single OTRA is proposed. It provides non interactive control between inductance value and realizabilty condition. The proposed lossless grounded inductor is shown in Fig. 3.15. From routine analysis of the circuit the input admittance $Y_{in}(s)$ can be expressed as

$$Y_{in}(s) = (3G - \frac{C_1 G}{C_2}) + \frac{G^2}{sC_2}, \text{ where G = 1/R} \quad (3.28)$$

The admittance Y_{in} will be purely inductive if following condition is met

$$C_1 = 3C_2 \tag{3.29}$$

The inductance value that results is

$$L_{eq} = \frac{C_2}{G^2} = C_2R^2 \tag{3.30}$$

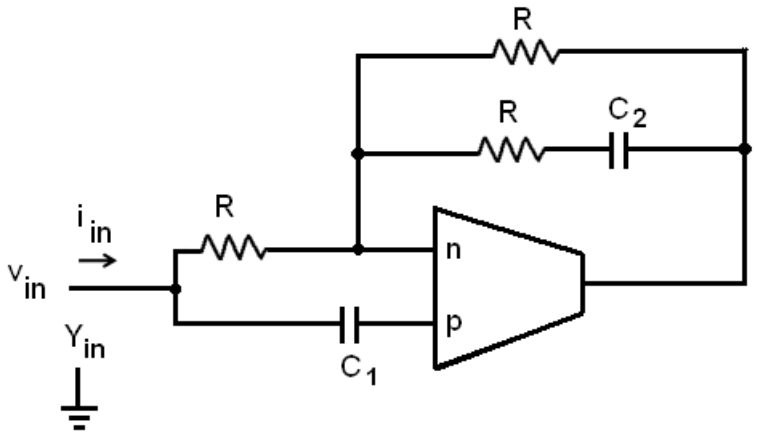


Fig. 3.15 Single OTRA based lossless grounded inductor.

Thus inductance value can be adjusted by appropriate selection of R without disturbing the condition of realization of inductor, as it does not depend on resistance R. It may be noted that the floating resistors can be implemented using one-port active MOS resistor architecture [76], [77] wherein the resistance values can be adjusted by simply changing the dc control voltage thus making inductor value electronically tunable.

3.4.2.1 Nonideality Analysis

In this section the effect of finite transresistance gain on inductor is considered and for high frequency applications, passive compensation is employed. Taking the effect of nonideality of OTRA into account (3.28) modifies to

$$Y_{in}(s)\big|_n = 2G + sC_1 - \frac{(sC_1 - G)\,(sC_2 + G)\,\varepsilon_{uc}(s)}{sC_2} \tag{3.31}$$

where $\varepsilon_{uc}(s) = \frac{1}{1+\left(1+\frac{sC_2}{G}\right)\frac{C_p}{C_2}}$ (3.32)

is uncompensated error function.

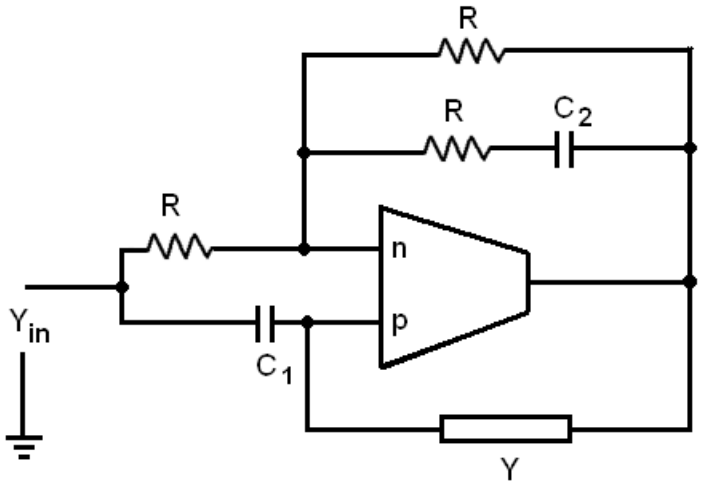


Fig. 3.16 High Frequency Compensation.

For high-frequency applications, compensation methods must be employed to account for the error so introduced in the admittance function. High frequency passive compensated topology of the simulated inductance is shown in Fig. 3.16. Routine analysis of Fig. 3.16 results in compensated admittance function given as

$$Y_{in}(s)\big|_{n\_c} = 2G + sC_1 - \frac{(sC_1-G)(sC_2+G)}{sC_2}\ \varepsilon_c(s) \quad (3.33)$$

where $\varepsilon_c(s) = \frac{1}{1+(sC_p-Y)\frac{(G+sC2)}{GsC_2}}$ (3.34)

is compensated error function.

By taking Y = sC_p, $\varepsilon_c(s)$ reduces to 1, which makes (3.33) same as (3.28). The effect of single pole model of R_m can thus be eliminated by connecting a single capacitor having value C_p in place of Y as shown in Fig. 3.16.

3.4.2.2 Simulation Results

The performance of the simulated inductor is evaluated with SPICE simulation using CMOS schematic of OTRA shown in Fig. 2.9. Impedance magnitude responses of simulated and ideal inductors for L_{eq} = 10 µH and 1mH are given in Fig. 3.17(a) and (b) respectively. Component values for L_{eq} = 10 µH are chosen as R = 1 KΩ, C_1 = 30 pF and C_2 = 10 pF and those for L_{eq} = 1 mH are R = 10 KΩ, C_1 = 30 pF and C_2 = 10 pF. Inductance value remains within ± 10% in the frequency range of 8 KHz - 5.0 MHz for 10 µH whereas for 1 mH the frequency range is found to be 200 Hz - 2.5 MHz. It indicates that the frequency range, over which the inductance value remains almost constant, decreases with increasing value of simulated inductance. The dynamic range of the proposed active inductor is simulated to be 71 dB. Total power consumption of the proposed inductor is simulated to be 0.809 mW.

3.4.2.3 Applications

In this section the workability of the proposed grounded inductor has been illustrated by realizing a BP filter and an LC oscillator.

3.4.2.3.1 Band Pass Filter

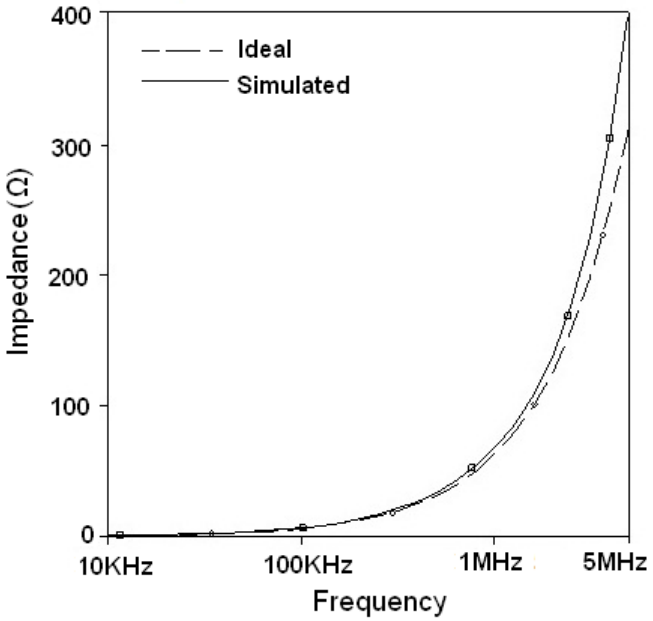
A BP filter, as shown in Fig. 3.18 (a), is constructed using proposed inductor and using routine analysis the transfer function can be obtained as

$$\frac{v_o}{v_{in}} = \frac{\frac{s}{C_B R_B}}{s^2 + \frac{s}{C_B R_B} + \frac{1}{L_{eq} C_B}} \tag{3.35}$$

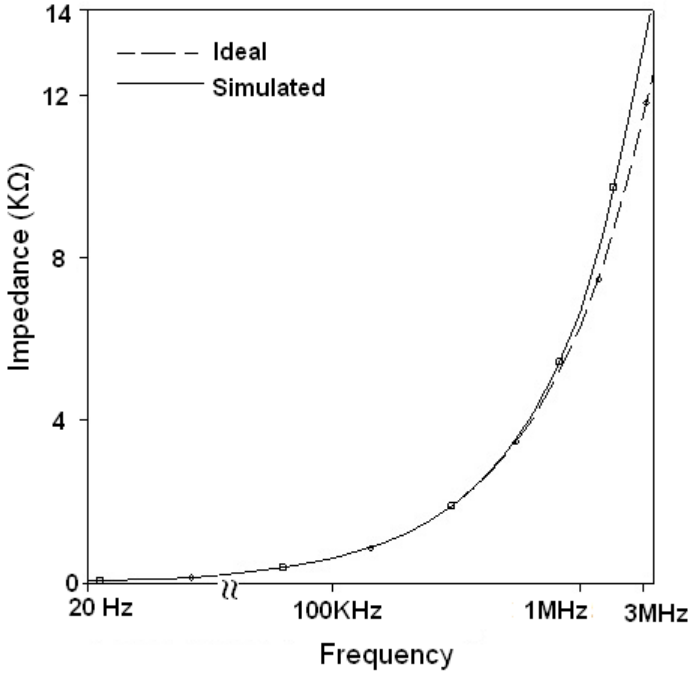
where $\omega_0 = \frac{1}{\sqrt{L_{eq} C_B}} = \frac{1}{R\sqrt{C_2\, C_B}}$, $Q_0 = R_B \sqrt{\frac{C_B}{L_{eq}}} = \frac{R_B}{R}\sqrt{\frac{C_B}{C_2}}$ (3.36)

This suggests that the Q_0 can be independently controlled by varying R_B without affecting the centre frequency ω_0. Passive sensitivities for ω_0 and Q_0 can be calculated as follows

$$S_{C_2}^{\omega_0} = S_{C_B}^{\omega_0} = -\frac{1}{2}, S_R^{\omega_0} = -1,\ S_{R_B}^{Q_0} = 1, S_R^{Q_0} = -1,\ S_{C_B}^{Q_0} = \frac{1}{2}, S_{C_2}^{Q_0} = -\frac{1}{2} \tag{3.37}$$



(a)



(b)

Fig. 3.17 Impedance magnitude response (a) L_{eq} = 10 µH (b) L_{eq} = 1 mH.

To see the correctness of the theoretical proposition, the BP filter of Fig.3.18 (a) is designed having a centre frequency of 1.59 MHz. The component values are computed as R_B = 1 KΩ, C_B = 1 nF and L_{eq} = 10 µH. The L_{eq} = 10 µH is obtained by choosing R = 1 KΩ, C_1 = 30 pF and C_2 = 10 pF. The simulated frequency response of the filter using CMOS OTRA of Fig. 2.9 is depicted in Fig. 3.18 (b). The simulated results are in close agreement with the theoretical predictions. Figure 3.18 (c) shows the frequency response of the BPF, for different Q_0 values as 0.5, 5, 10 and 20, for which value of R_B is chosen as 50 Ω, 100 Ω, 1 KΩ, and 2 KΩ respectively while keeping C_B = 1 nF and L_{eq} = 10 µH as constant.

3.4.2.3.2 LC Oscillator

Using the BPF of Fig. 3.18 an LC oscillator can be realized as shown in Fig. 3.19 (a), for which the characteristic equation is obtained as

$$s^2 + \frac{s((R_{o1}+R_{o2})-R_{o3})}{R_{o2}(R_{o2}+R_{o1})} + \frac{1}{L_{eq}C_{o1}} = 0 \tag{3.38}$$

From characteristic equation the CO and FO can be derived as

CO: $$(R_{o1} + R_{o2}) = R_{o3} \tag{3.39}$$

FO: $$f_0 = \frac{1}{2\pi\sqrt{(L_{eq}C_{o1})}} \tag{3.40}$$

The simulated output waveform of the oscillator topology of Fig. 3.19 (a) for component values of R_{o1} = 4.6 KΩ, R_{o2} = 400 Ω, R_{o3} = 5 KΩ, C_{o1} = 1 nF and L_{eq} = 10 µH is shown in Fig. 3.19 (b) and the output frequency spectrum is depicted in Fig. 3.19 (c). The simulated frequency of oscillation being 1.53 MHz is in close agreement with the theoretically calculated value of 1.59 MHz. The % total harmonic distortion (%THD) being 0.49%, is a considerably low value.

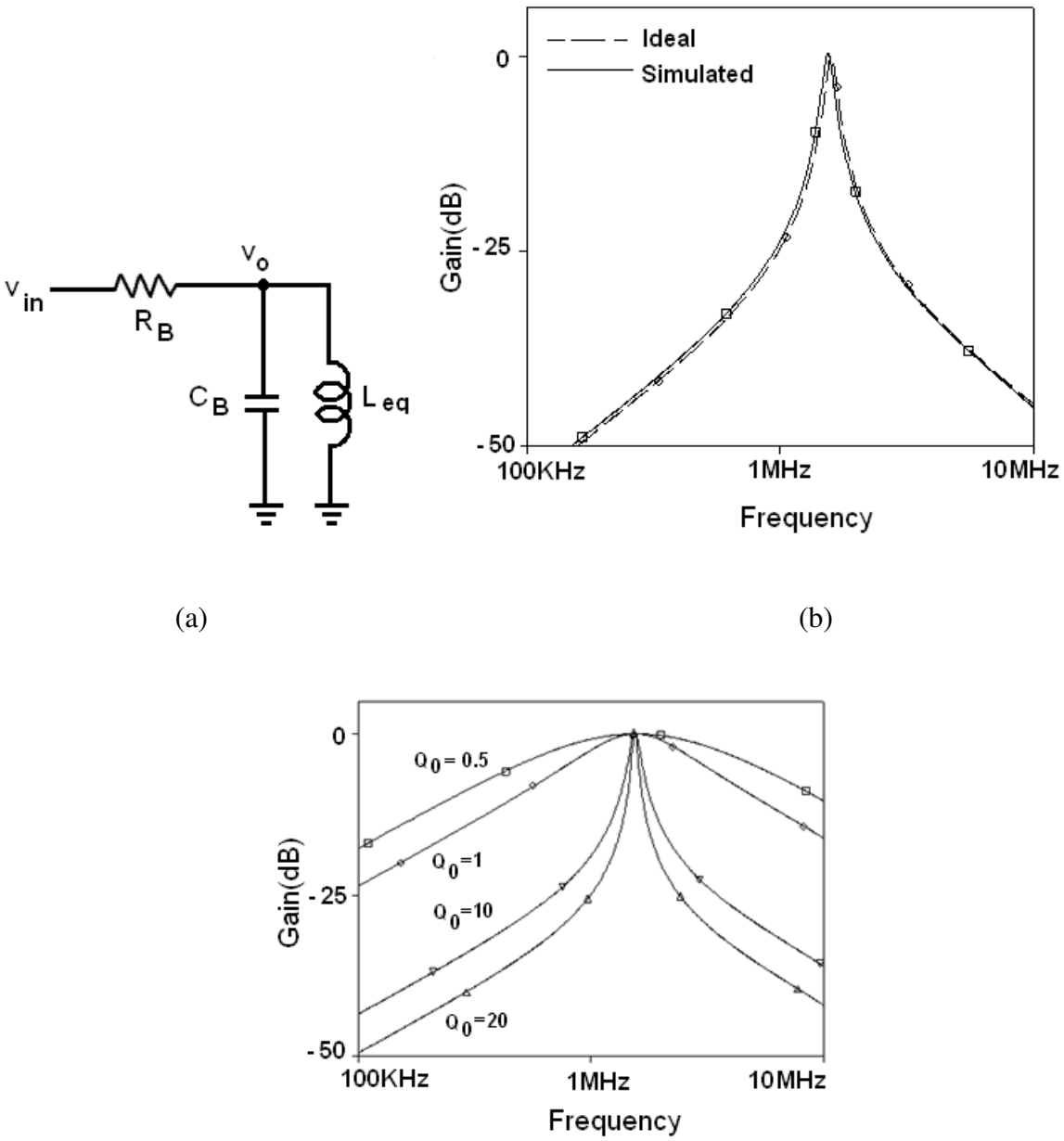
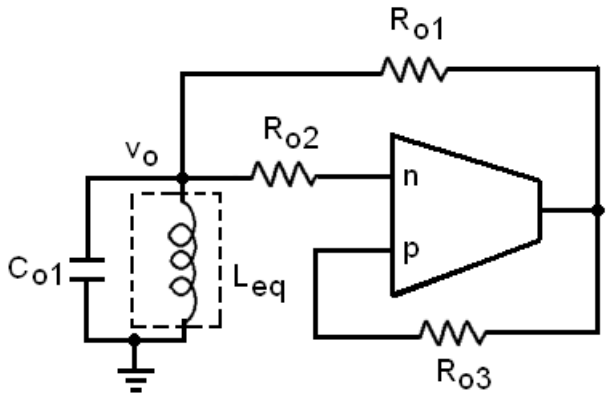
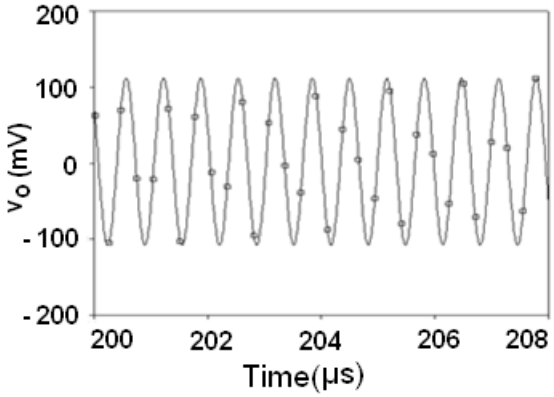


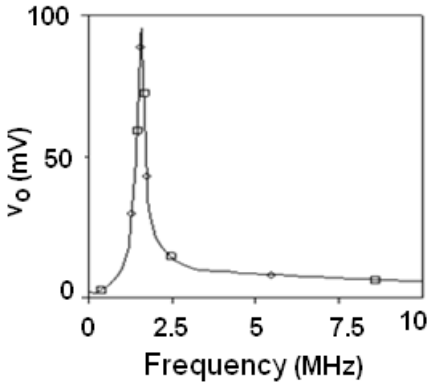
Fig. 3.18 (a) BPF using single OTRA based simulated inductance. (b) Frequency response.

(c) BP response for different Q_0 values with $\omega_0 = 1.59$ MHz.



(a)





(b) (c)

Fig. 3.19 (a) LC oscillator using single OTRA based simulated inductance. (b) Oscillator output. (c) Frequency spectrum.

3.4.2.4 Experimental Verification

The functionality of the proposed grounded inductor is verified experimentally also. The commercial IC AD844AN is used to implement an OTRA as shown in Fig. 2.7 with a supply voltage of ± 5V. The BPF of Fig. 3.18 (a) is prototyped with C_B = 1 nF, R_B = 1 KΩ, and L_{eq} = 100 μH. The L_{eq} = 100 μH is implemented with component values of C_1 = 330 pF, C_2 = 100 pF and R = 1 KΩ. Theoretical, simulated (using macromodel of AD844) and experimental frequency responses are shown in Fig. 3.20. It is observed that the experimental cut off frequency (478 KHz) is close to theoretical (501 KHz) and simulated (493 KHz)

values. The oscillator circuit of Fig. 3.19 (a) is also tested experimentally for C_{o1} = 1 nF and L_{eq} = 5 µH. The L_{eq} = 5 µH is implemented with component values of R = 680 Ω, C_1 = 33 pF and C_2 = 10 pF. The output waveform observed on oscilloscope is shown in Fig. 3.21. The observed frequency of oscillation is found to be 2.47 MHz, as against theoretically calculated value of 2.3 MHz. The minor deviations in experimental results can be attributed to component tolerance of ± 10%, used for experiments.

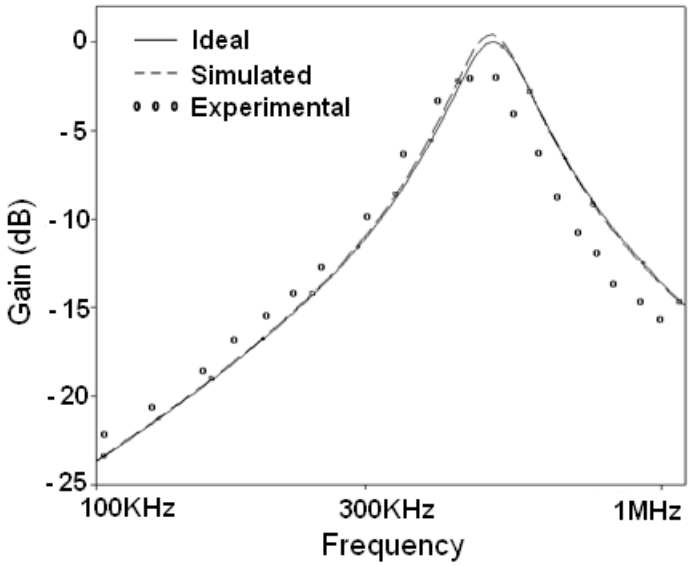


Fig. 3.20 Ideal, simulated and experimental frequency responses of BPF of Fig. 3.18 (a).

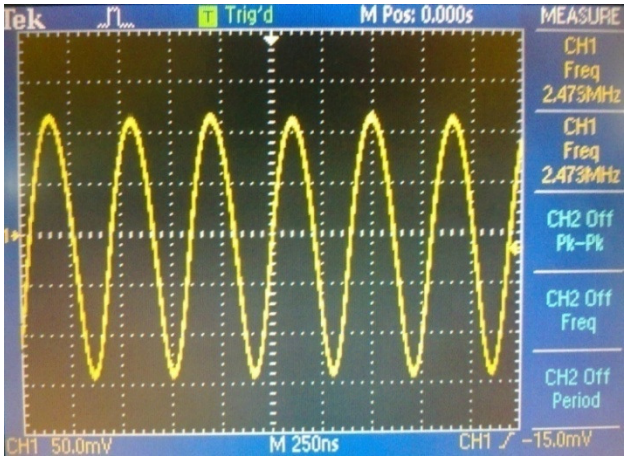


Fig. 3.21 Experimental output of LC oscillator of Fig. 3.19 (a).

3.4. 3. Comparison

Table 3.2 shows the comparison of the proposed OTRA based grounded inductors with the previously reported lossless grounded inductors [61] – [64]. The study of Table 3.2 reveals that topologies presented in [61], [62] and those proposed in section 3.4.1 use more number of active and passive components as compared to the proposed single OTRA based topology. In the most recently published topology [63] though the number of passive components is reduced by one yet it uses an extra active element (buffer) as compared to the proposed circuit. The topology in [64] uses same number of active components and an extra passive component and simulates negative grounded inductor.

To compare the performance of all the circuits reported in [61] – [64] with proposed work in terms of power consumption and frequency range of operation an inductance (L_{eq}) value of 1 mH was implemented using CFOA based OTRA realization with supply voltage of ± 10V. Table 3.3 records the power consumption of various circuits and the observations indicating the range of frequency in which the inductor value remains well within the ± 10% of the designed value. Similar observations with CMOS based OTRA realization as given in Fig. 2.9, with supply voltages of ± 1.5V are also listed in Table 3.3. It is observed that the proposed single OTRA based topology outperforms both in terms of frequency range and power consumption, except for lossless negative inductor [64]. The components required for implementing an inductance (L_{eq}) value of 1 mH are given in the last column of Table 3.3. This suggests that the proposed single OTRA based circuit consumes the optimum chip area in terms of active component count and also the area used in terms passive components is minimum as compared to all existing circuits except the one presented in [63].

Table 3.2: Comparison of proposed lossless grounded inductor topologies with previously reported work.

Ref.	No. of active components	No. of passive components	Passive component matching required	Type of simulated inductor	Non-interactive tuning of L_{eq}
[61]	Two OTRA	Single capacitor, Five resistors	Yes	Lossless inductor	Yes
[62]	Two OTRA	Single capacitor, Five resistors	Yes	Lossless Inductor	Yes
Proposed Work of section 3.4.1	Two OTRA	Single capacitor, Five resistors	Yes	Lossless Inductor	Yes
[63]	Single OTRA Two; An OTRA and a Buffer	Two capacitors, Two resistors	Yes	Lossless Inductor	Yes
[64]	Single OTRA	Single capacitor, Five resistors	Yes	Lossless negative Inductor	Yes
Proposed Single OTRA based topology	Single OTRA	Two capacitors, Three resistors	Yes	Lossless Inductor	Yes

Table 3.3: Useful frequency range and power consumption of 1 mH inductor.

Ref.	CFOA based OTRA realization		CMOS based OTRA realization		Components used for L_{eq} = 1 mH implementation
	Frequency Range	Power consumption	Frequency Range	Power consumption	
[61]	150Hz-100KHz	0.533W	200Hz-1MHz	1.5mW	OTRAs : Two,Capacitor : One (1nF), Resistors : Five (1KΩ,1KΩ,1KΩ,1KΩ,3KΩ)
[62]	150Hz - 30KHz	0.553W	200Hz - 1.2MHz	1.604mW	OTRA: Two, Capacitor: One (1nF), Resistors: Five (1KΩ,1KΩ,1KΩ,1KΩ,4KΩ)
Proposed work of section 3.4.1	200Hz-100KHz	0.53W	200Hz-1.2MHz	1.63mW	OTRA: Two,Capacitor :One (3nF), Resistors: Five (1KΩ,1KΩ,1KΩ,1KΩ,3KΩ)
[63]	200Hz-100KHz	0.53W	300Hz-2MHz	1.59mW	OTRA: One, Buffer: One, Capacitors: Two (1nF,1nF), Resistors: Two (1KΩ,1KΩ)
[64]	250Hz-350KHz	0.262W	200Hz-3MHz	0.79mW	OTRA: One, Capacitor: One (3nF), Resistors: Five (1KΩ,1KΩ,1KΩ,1.5KΩ,3KΩ)
Proposed single OTRA based topology	200Hz - 100KHz	0.26	200Hz - 2.5MHz	0.809 mW	OTRA: One,Capacitors: Two (1nF,3nF), Resistors: Three (1KΩ,1KΩ,1KΩ)

3.5 CONCLUDING REMARKS

Following grounded parallel inductance simulation topologies are proposed in this chapter

1. Single OTRA based lossy inductance simulator
2. Two topologies of lossless inductance using two OTRAs
3. Single OTRA based lossless grounded inductor

In lossless inductance topologies the value of simulated inductance can be tuned independent of the condition of realization. The effect of nonidealities of OTRA on the proposed inductance's performance has been analyzed and compensation methods for high frequency applications are also presented. Application examples such as filters and LC oscillators using various proposed topologies have been included to demonstrate their practical use. SPICE simulations and experimental results are included to verify the theoretical propositions. It is found that the results obtained are in close agreement with the ideal values. Hence it is expected that the proposed topologies will provide a design option to integrated circuit designers where grounded lossy/lossless inductor applications are required.

CHAPTER - 4
OTRA BASED FILTERS

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, A. Singh, B. Sriram, and K. Trivedi, "**Voltage Mode OTRA MOS-C Single Input Multi Output Biquadratic Universal Filter**," Advances in Electrical and Electronic Engineering, vol.10 no. 5, pp. 337-344, 2012.

2. Mayank Bothra, Rajeshwari Pandey, Neeta Pandey, and Sajal K. Paul, **"Operational Trans-Resistance Amplifier based Tunable Wave Active Filters,**" Accepted in Radioengineering Journal.

3. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Mandeep Singh, Manish Jain "**Voltage Mode single OTRA based Biquadratic Filters**," Third International Conference on Communication and Computer Technology (ICCCT'12), pp. 63-66, 2012.

4. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Mandeep Singh, Manish Jain, "**Voltage Mode Biquadratic Filter using Single OTRA,"** IEEE 5th India International Conference on Power Electronics (IICPE'13), pp. 1- 4, 2012.

4.1 INTRODUCTION

Electronic filter is an essential building block of communication and instrumentation systems. It is a linear two port frequency selective network which allows signals in a specified frequency range to be passed (the filter passband), while rejecting frequencies outside this range (the filter stop band). Ideally in pass band the magnitude of signal transmission is unity whereas in stop band it is zero. Filters are classified according to the function they perform in terms of frequency range as pass band and stop band. A filter for which passband extends from zero to a definite frequency, known as cutoff frequency, is a low pass filter. A high pass filter stops the frequency range from zero to cutoff frequency and allows rest to pass. In band pass filter a continuum of signal frequencies is allowed to pass while all other frequencies are stopped. The band reject filter is complement of the band pass filter where a continuum frequency band is rejected allowing rest of the frequencies to pass. These filter structures can be classified as voltage input voltage output (voltage mode-VM), current input current output (Current mode-CM), voltage input current output (Transadmittance mode-TAM), and current input voltage output (Transimpedance mode-TIM) type as per the choice between voltage and current as two possible input and output signals. A further classification may be based upon the filter order; number of inputs and outputs available, cascadability and number of active building blocks used. This classification can be used as an assessment criterion to select a particular structure for a specific application.

This chapter concerns with the realization of OTRA based biquadratic and higher order filters. The work has been classified as single and multiamplifier filters. For the applications having power consumption as an important design constraint, single amplifier based biquadratic (SAB) filter is a useful choice. However SABs are less versatile and more sensitive to parameter changes when compared to multiamplifier filters. Multiamplifier filter is a preferred option for designing high quality factor (Q_0) filters. This leads to the developement of OTRA based multiamplifier configurations which are further categorised as second order and higher-order filters in the work presented.

In the following section a brief record of earlier work dealing with the filter design using OTRA is presented.

4.2 REVIEW OF EXISTING LITERATURE

In synchronization with the theme of this chapter the filter structures reported in the literature are categorised in terms of single and multiamplifier filters in voltage/current/transimpedance mode.

VM filters presented in [44], [47], [51] - [53] are single amplifier filters and are further classified as first order [51] - [53] or biquadratic [44], [47], [52], [53] filters. Few first order all pass topologies are presented in [51] - [53] whereas in [52], [53] second order notch and all pass filter structures are also presented.A biquad single input single output (SISO) configuration is presented in [44] which can synthesize LP, HP, BP, BR and AP responses by appropriate component selection. The SAB presented in [47] is a multiple input single output (MISO) structure which provides all five standard filter responses; namely LP, HP, BP, BR and AP, by lifting the nodes for input excitation.

The structures proposed in [36], [42], [45], [46], [48] - [50] are VM multiamplifier biquadratic filters. The filters presented in [36], [46] are single input multiple output (SIMO) structures. OTRA based Tow Thomas and KHN biquad structures are presented in [36] whereas [46] presents a different approach of realizing three standard filter functions available in KHN biquad. In [42] two different MISO universal filter configurations are presented.The biquad of [45] is a SISO structure which provides all five standard filter responses and is based on Fleischer-Tow scheme whereas in [48] a VM multiple input multiple output (MIMO) structure providing LP, HP, BP, and BR responses is reported.

The filter structures presented in [42], [49], [50] are VM higher order multiamplifier filters. A third order Chebyshev LPF is presented in [42] and the design approach for higher order filters using linear transformation method is outlined in [49], [50].

Current mode single amplifier based first order all pass structure is reported in [55]. The structures of [54], [56] are multiamplifier filters.Two different universal biquad

configurations are available in [54] which are MISO structures whereas in [56] linear transformation based CM higher order filter design method is presented.

TIM filters have not gained much attention as revealed by the reported work. TIM type single amplifier based first order all pass filter is available in [57] whereas [58] presents multiamplifier MISO universal biquad providing all five standard responses.

4.3 SINGLE OTRA BASED BIQUADRATIC FILTERS

Several OTRA based VM SAB filters [44], [47], [52], [53] have been proposed in literature. A detailed study of these structures shows that

- Component selection is required for obtaining various filter responses in [44], [47], [52], [53]
- Component matching and/or condition on components need to be satisfied for filter realization in [44], [47], [52], [53]
- Independent adjustment of angular frequency and quality factor is not possible in [44], [47], [52]
- Large component spread is required for obtaining high Q_0 value in [44], [47], [52], [53]
- Filter responses are obtained by lifting of nodes for input excitation in [47]

Thus all SAB filters not only require component selection for realization of various responses but also need to fulfill the component matching constraint and/or condition on components. Further these structures do not provide high Q_0 value with moderate component spread. Therefore in this work, two SAB filter configurations are presented which impose neither any condition on components nor require component matching constraints.

4.3.1 SAB Topology-I

The proposed SAB topology-I is shown in Fig. 4.1 and is based on Sallen Key approach. The transfer function of the circuit of Fig. 4.1 can be expressed as

$$\frac{v_o}{v_{in}} = \frac{KY_3Y_4}{D} \tag{4.1}$$

Where D and K are respectively given as

$$D = Y_3(Y_2 + Y_4 + Y_6) + Y_4(Y_2 + Y_5 + Y_6) + Y_2Y_5 + Y_5Y_6 - KY_4Y_5 \tag{4.2}$$

$$K = \frac{Y_2}{Y_1} \tag{4.3}$$

It realizes the LP, HP and BP filter functions by appropriate admittance selection. The appropriate admittance choices, which result in three required filter responses, are listed in Table 4.1. It may be noted that admittances Y_1 and Y_2 remain G_1 and G_2 respectively for all the responses so the value of K will be given as ratio of G_2 and G_1. Using the admittance choices given in Table 4.1 the LP response can be expressed as

$$\left.\frac{V_0}{V_{in}}\right|_{LP} = \frac{{}^{KG_3\,G_4}/_{C_1C_2}}{s^2+s\left(\frac{C_2(G_3+G_4)+C_1G_2+C_1G_4(1-K)}{C_1C_2}\right)+\left(\frac{G_3G_4+G_2G_4+G_2G_3}{C_1C_2}\right)} \tag{4.4}$$

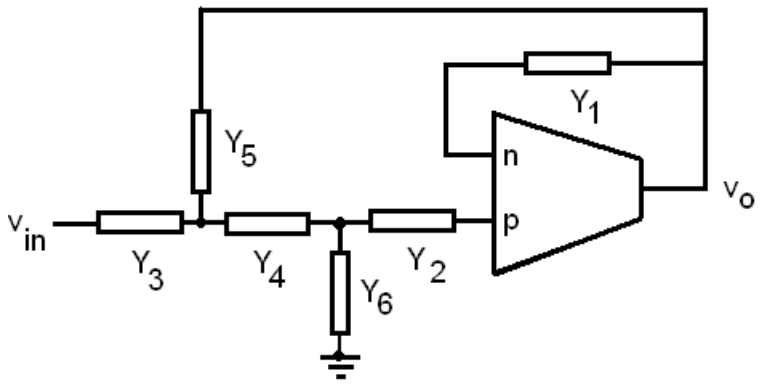


Fig. 4.1 Proposed SAB topology-I.

From (4.4) the resonant angular frequency (ω_0), the quality factor (Q_0) and filter Gain (H_0) for LP response can be obtained as

$$\left.\omega_0\right|_{LP} = \sqrt{\left(\frac{G_3G_4+G_2G_4+G_2G_3}{C_1C_2}\right)} \tag{4.5}$$

$$Q_0\big|_{LP} = \frac{\sqrt{(G_3G_4+G_2G_4+G_2G_3)C_1C_2}}{C_2(G_3+G_4)+C_1G_2+C_1G_4(1-K)} \tag{4.6}$$

$$H_0\big|_{LP} = \frac{KG_3G_4}{(G_3G_4+G_2G_4+G_2G_3)} \tag{4.7}$$

Table 4.1: Admittance Selection for SAB topology-I.

Filter Function	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
LowPass	G_1	G_2	G_3	G_4	sC_1	sC_2
HighPass	G_1	G_2	sC_1	sC_2	G_3	G_4
Band Pass	G_1	G_2	G_3	sC_1	G_4	sC_2

For appropriate admittance choices the HP response can be obtained as below

$$\left.\frac{V_0}{V_{in}}\right|_{HP} = \frac{K\,s^2}{s^2+s\left(\frac{C_1(G_2+G_4)+C_2(G_2+G_4)+G_3C_2(1-K)}{C_1C_2}\right)+\left(\frac{G_2G_3+G_3G_4}{C_1C_2}\right)} \tag{4.8}$$

The filter parameters ω_0, Q_0 and H_0 for HP response can be expressed as

$$\omega_0\big|_{HP} = \sqrt{\frac{G_3(G_2+G_4)}{C_1C_2}} \tag{4.9}$$

$$Q_0\big|_{HP} = \frac{\sqrt{(G_2G_3+G_3G_4)C_1C_2}}{C_1(G_2+G_4)+C_2(G_2+G_4)+G_3C_2(1-K)} \tag{4.10}$$

$$H_0\big|_{HP} = K \tag{4.11}$$

The BP response with proper admittance choices, enlisted in Table 4.1, is given by

$$\left.\frac{V_0}{V_{in}}\right|_{BP} = \frac{\frac{K\,sG_3}{C_2}}{s^2+s\left(\frac{C_1(G_2+G_3)+C_2(G_3+G_4)+C_1G_4(1-K)}{C_1C_2}\right)+\frac{G_2(G_3+G_4)}{C_1C_2}} \quad (4.12)$$

From (4.12) the values of ω_0, Q_0 and H_0 for the BP response can be computed as

$$\omega_0|_{BP} = \sqrt{\frac{G_2(G_3+G_4)}{C_1C_2}} \quad (4.13)$$

$$Q_0|_{BP} = \frac{\sqrt{C_1C_2G_2(G_3+G_4)}}{C_1(G_2+G_3)+C_2(G_3+G_4)+C_1G_4(1-K)} \quad (4.14)$$

$$H_0|_{BP} = \frac{KC_1G_3}{C_1(G_2+G_3)+C_2(G_3+G_4)+C_1G_4(1-K)} \quad (4.15)$$

Table 4.2 lists the H_0, ω_0 and Q_0 for all the three responses when all the conductances except G_1, the K determining component, are set equal to G and all capacitors are set equal to C. This suggests that the H_0 and Q_0, for all the responses, can be controlled by varying K without affecting the ω_0 and by adjusting the capacitance value ω_0 can be tuned independently. With MOS transistor implementation of G_1 as outlined in chapter 2, the filter parameters Q_0 and H_0 can be electronically tuned. Filter circuit of Fig. 4.1 can be redrawn as Fig. 4.2 wherein G_1 is implemented using MOS transistors M_a and M_b.

4.3.1.1 Sensitivity Analysis

The passive sensitivities of ω_0 and Q_0 for the LPF configuration can be expressed as

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2},\ S_{G_1}^{\omega_0} = 0,\ S_{G_2}^{\omega_0} = \frac{1}{2} - \frac{G_3G_4}{2(G_3G_4+G_2G_4+G_2G_3)},$$

$$S_{G_3}^{\omega_0} = \frac{1}{2} - \frac{G_2G_4}{2(G_3G_4+G_2G_4+G_2G_3)},\ S_{G_4}^{\omega_0} = \frac{1}{2} - \frac{G_2G_3}{2(G_3G_4+G_2G_4+G_2G_3)} \quad (4.16)$$

$$S_{C_1}^{Q_0} = \frac{1}{2} - \frac{C_1G_2+C_1G_4(1-K)}{C_2(G_3+G_4)+C_1G_2+C_1G_4(1-K)} \quad S_{C_2}^{Q_0} = \frac{1}{2} - \frac{C_2(G_3+G_4)}{C_2(G_3+G_4)+C_1G_2+C_1G_4(1-K)} \quad (4.17)$$

Table 4.2: Filter parameters for equal component design.

Filter Function	Filter Gain (H_0)	Angular Frequency(ω_0)	Quality Factor (Q_0)
Low Pass	$K/3$	$\sqrt{3}G/C$	$\sqrt{3}/(4-K)$
High Pass	K	$\sqrt{2}G/C$	$\sqrt{2}/(5-K)$
Band Pass	$K/(5-K)$	$\sqrt{2}G/C$	$\sqrt{2}/(5-K)$

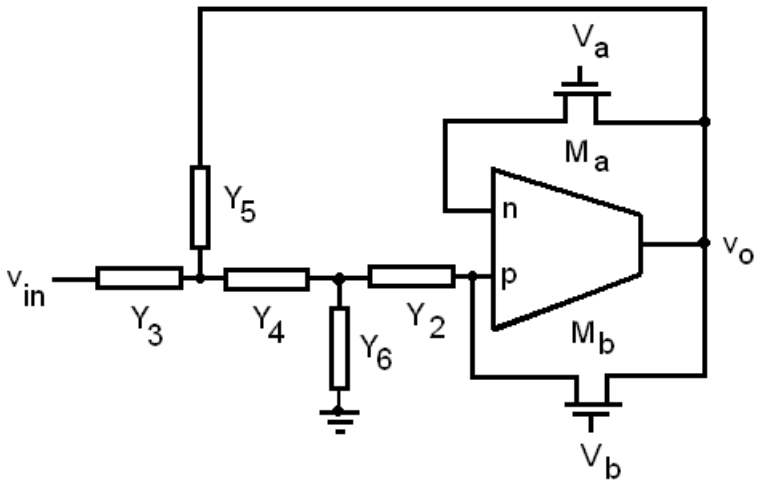


Fig. 4.2 Electronically tunable SAB Topology-I.

The passive sensitivities of ω_0 and Q_0 for the HPF configuration can be computed as

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}, \quad S_{G_2}^{\omega_0} = \frac{1}{2} - \frac{G_4}{2(G_4+G_2)}, S_{G_1}^{\omega_0} = 0, \quad S_{G_3}^{\omega_0} = \frac{1}{2}, \quad S_{G_4}^{\omega_0} = \frac{1}{2} - \frac{G_2}{2(G_4+G_2)} \quad (4.18)$$

$$S_{C_1}^{Q_0} = \frac{1}{2} - \frac{C_1(G_2+G_4)}{C_1(G_2+G_4)+C_2(G_2+G_4)+C_2G_3(1-K)}$$

$$S_{C_2}^{Q_0} = \frac{1}{2} - \frac{C_2(G_2+G_4)+C_2G_3(1-K)}{C_1(G_2+G_4)+C_2(G_2+G_4)+C_2G_3(1-K)} \quad (4.19)$$

The passive sensitivities of ω_0 and Q_0 for the BPF configuration can be calculated as

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2},\ S_{G_1}^{\omega_0} = 0,\ S_{G_2}^{\omega_0} = \frac{1}{2},\ S_{G_3}^{\omega_0} = \frac{1}{2} - \frac{G_4}{2(G_3+G_4)},\ S_{G_4}^{\omega_0} = \frac{1}{2} - \frac{G_3}{2(G_3+G_4)} \quad (4.20)$$

$$S_{C_1}^{Q_0} = \frac{1}{2} - \frac{C_1(G_2+G_3)+C_1G_4(1-K)}{C_1(G_2+G_4)+C_2(G_3+G_4)+C_1G_4(1-K)},$$

$$S_{C_1}^{Q_0} = \frac{1}{2} - \frac{C_2(G_3+G_4)}{C_1(G_2+G_3)+C_2(G_3+G_4)+C_1G_4(1-K)} \quad (4.21)$$

It is clearly observed from (4.16) and (4.21) that the passive sensitivities for all the filter responses are lower than 1/2 in magnitude so the filter configurations may be termed as insensitive.

4.3.1.2 Nonideality Analysis

The response of the filter may deviate due to nonideality of OTRA in practice. Taking the nonideality effect as discussed in section 2.3, into account (4.4), (4.8) and (4.12) modify to (4.22), (4.23) and (4.24) respectively

$$\left.\frac{V_0}{V_{in}}\right|_{LP\_n} = \frac{\frac{K}{(1+sC_p/G_1)} G_3 G_4 / C_1C_2}{s^2+s\left(\frac{C_2(G_3+G_4)+C_1G_2+C_1G_4\left(1-\frac{K}{(1+sC_p/G_1)}\right)}{C_1C_2}\right)+\left(\frac{G_3G_4+G_2G_4+G_2G_3}{C_1C_2}\right)} \quad (4.22)$$

$$\left.\frac{V_0}{V_{in}}\right|_{HP\_n} = \frac{\frac{Ks^2}{(1+sC_p/G_1)}}{s^2+s\left(\frac{C_1(G_2+G_4)+C_2(G_2+G_4)+G_3C_2\left(1-\frac{K}{(1+sC_p/G_1)}\right)}{C_1C_2}\right)+\left(\frac{G_2G_3+G_3G_4}{C_1C_2}\right)} \quad (4.23)$$

$$\left.\frac{V_0}{V_{in}}\right|_{BP\_n} = \frac{\frac{KsG_1}{(1+sC_p/G_1)C_2}}{s^2+s\left(\frac{C_1(G_2+G_3)+C_2(G_3+G_4)+C_1G_4\left(1-\frac{K}{(1+sC_p/G_1)}\right)}{C_1C_2}\right)+\frac{G_2(G_3+G_4)}{C_1C_2}} \quad (4.24)$$

The sC_p term appearing in parallel to G_1 will result in introduction of paraasitic pole having radian frequency as $\omega = G_1/C_p$. The pole frequency for the biquad is typically expressed as G_i/C_i. The effect of the parasitic pole can be ignored by selecting $C_i >> C_p$, so that the pole frequency of the biquad is much lower than the parasitic pole frequency.

4.3.1.3 Simulation Results

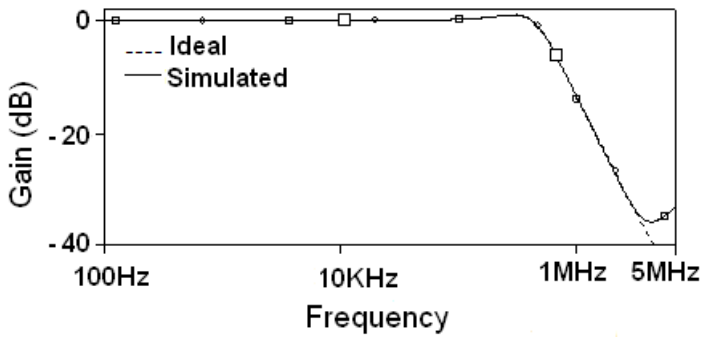
The workability of the proposed SAB is verified thruogh SPICE simulation using OTRA CMOS schematic of Fig. 2.9. The LPF and HPF have been designed for f_0 = 500 KHz for which capacitance values are chosen as $C_1 = C_2$ = 100 pF. Various conductances to obtain the LP and HP responses are computed as

LPF: G_1 = 0.05 mS, G_2 = 0.1 mS, $G_3 = G_4$ = 0.2 mS

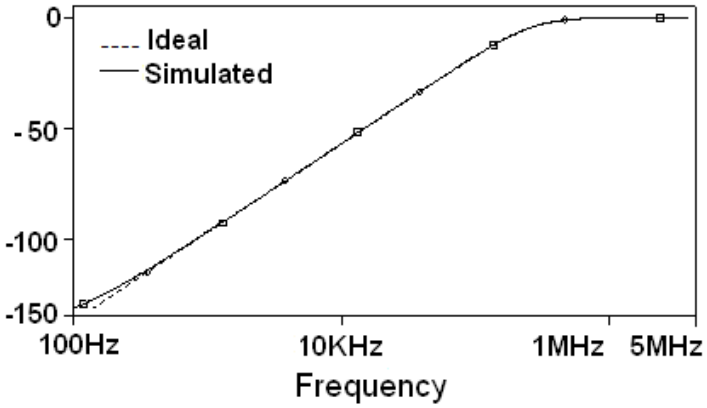
HPF: $G_1 = G_2$ = 0.1 mS, G_3 = 0.2 mS, G_4 = 0.1 mS.

The BP function is demonstrated through a design having f_0 = 750 KHz and Q_0 = 0.56. The capacitors are chosen as $C_1 = C_2$ = 30 pF and conductance values are computed to be G_1 = 0.04 mS, $G_2 = G_3 = G_4$ = 0.1 mS. The ideal and simulated LP, HP and BP responses are shown in Fig. 4.3(a), (b) and (c) respectively. It can be observed that there is a close agreement between the theoretical and simulated responses except that low pass transmission deviates from ideal response at frequencies well above cutoff and starts increasing at a rate of 20dB/dec. This behaviour can be explained using high frequency model of LPF shown in Fig. 4.4 which is based on the assumption that C_1 and C_2 become effectively short at high frequencies as compared to G_3 and G_4. The filter transfer function can now be expressed as

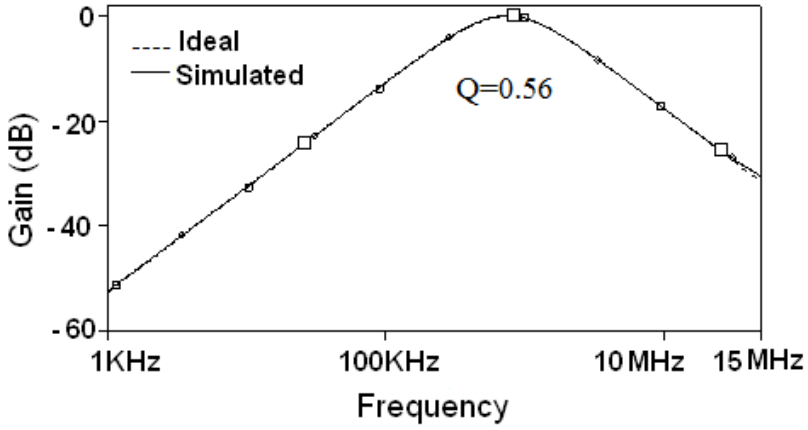
$$\frac{v_0}{v_{in}} = \frac{1}{\frac{G_4}{G_3}+\frac{1}{G_3Z_0}+1} \quad (4.25)$$



(a)



(b)



(c)

Fig. 4.3 Frequency response of proposed SAB topology -I (a) LP. (b) HP. (c) BP.

Assuming $Z_0 \ll \frac{1}{G_3}$, (4.25) reduces to

$$\frac{v_0}{v_{in}} \approx Z_0 G_3 \tag{4.26}$$

where Z_0 is the closed-loop output impedance and can be expressed as

$$Z_0(s) = \frac{R_{out}}{1+\frac{R_m(s)}{K}} \tag{4.27}$$

The R_{out} represents the output resistance of OTRA.The feedback factor, K, is constant however the open loop gain, $R_m(s)$, is frequency dependant. Representig $R_m(s)$ with a single pole model as discussed in section 2.3, (4.27) modifies to

$$Z_0(s) = R_{out} s K C_p \tag{4.28}$$

Assuming R_{out} is mainly resistive, Z_0 becomes inductive and increases at a rate of 20 dB/dec at high frequencies and the transfer function expressed by (4.26) appears to be a first order HP response.

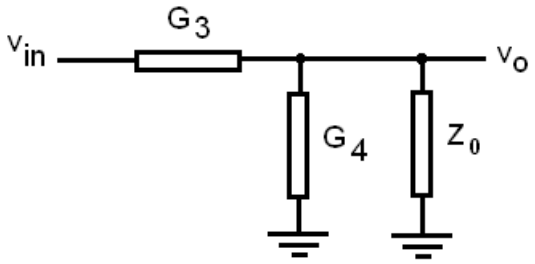
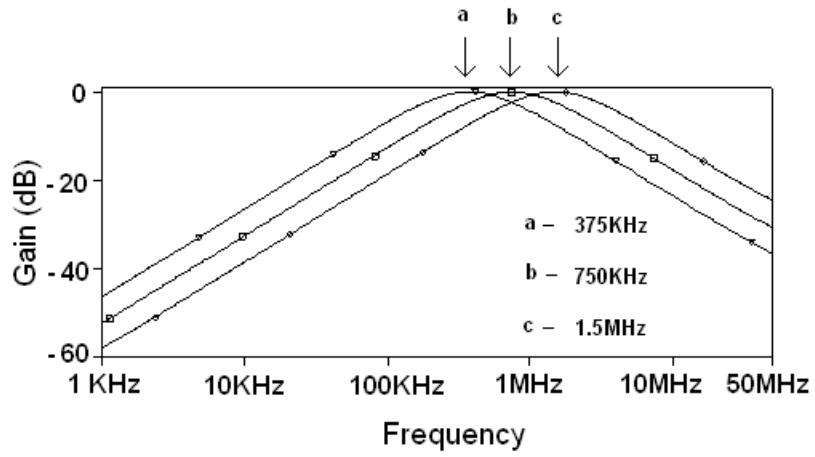


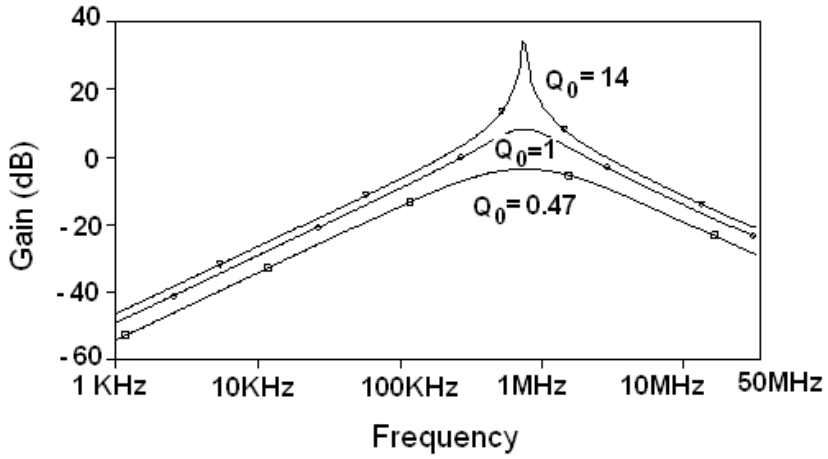
Fig. 4.4 High frequency model of LPF.

To show the orthogonal adjustment of f_0 and Q_0 the BP response for f_0 = 375 KHz, 750 KHz and 1.5 MHz has been plotted in Fig. 4.5(a) while keeping Q_0 fixed at 0.56. The simulation results for Q_0 = 14, 1 and 0.47, when f_0 remains constant at 750 KHz, is shown in Fig. 4.5(b). The Q_0 tuning can be accomplished through G_1 and f_0 can be adjusted by simultaneous change in capacitance values. It is evident from Fig. 4.5(a) and (b) that f_0 and Q_0 are orthogonally tunable. For electronic tuning of the filter parameters the gate voltages of the transistors used to implement G_1 need to be controlled. For the transistors M_a and M_b used for resistance realization as shown in Fig.4.2, the aspect ratio is taken as W/L = 10µm/2µm. The

values of gate bias voltages used for tuning of G_1 and Q_0 as obtained are listed in Table 4.3.



(a)



(b)

Fig. 4.5 Orthognal tunabiltiy of BP response (a) ω_0 adjustment (b) Q_0 adjustment.

Table 4.3: Component values used for orthogonal tunability of Q_0.

V_a (V)	V_b (V)	G_1 (mS)	K	Q_0
1.2	0.556	0.5	2	0.47
1.0	0.635	0.28	4	1
1.0	0.73	0.2	5	14

4.3.2 SAB Topology-II

The second filter topology proposed is shown in Fig. 4.6 and using routine analysis the transfer function of this circuit can be expressed as

$$\frac{V_o}{V_{in}} = \frac{-Y_1 Y_3}{D} \tag{4.29}$$

where $D = (Y_1 + Y_2 + Y_3 + Y_4)Y_5 + Y_3 Y_4$ (4.30)

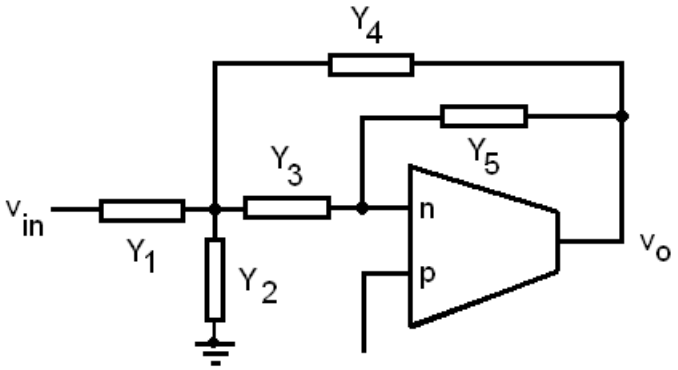


Fig. 4.6 Proposed SAB topology-II.

The appropriate admittance choices, which result in three required filter responses, are listed in Table 4.4.

Table 4.4: Admittance Selection for SAB topology-II.

Filter Function	Y_1	Y_2	Y_3	Y_4	Y_5
Low Pass	G_1	sC_1	G_2	G_3	sC_2
High Pass	sC_1	G_1	sC_2	sC_3	G_2
Band Pass	G_1	G_2	sC_1	sC_2	G_3

Using the admittance choices given in Table 4.4 the LP response can be expressed as

$$\left.\frac{V_0}{V_{in}}\right|_{LP} = \frac{-G_1 G_2/C_1C_2}{s^2+s\left(\frac{(G_1+G_2+G_3)}{C_1}\right)+\left(\frac{G_2G_3}{C_1C_2}\right)}$$

(4.31)

The LPF can be characterized by filter parmeters given by (4.32), (4.33) and (4.34) respectively.

$$\omega_0|_{LP} = \sqrt{\left(\frac{G_2G_3}{C_1C_2}\right)} \tag{4.32}$$

$$Q_0|_{LP} = \frac{\sqrt{G_2G_3C_1}}{\sqrt{C_2(G_1+G_2+G_3)}} \tag{4.33}$$

$$H_0|_{LP} = \frac{-G_1}{G_3} \tag{4.34}$$

Using appropriate admittance choices as given in Table 4.4 the HP response can be obtained as below

$$\left.\frac{V_0}{V_{in}}\right|_{HP} = \frac{-s^2C_1/C_3}{s^2+s(G_2(C_1+C_2+C_3)/C_2C_3))+(G_1G_2)/(C_2C_3)} \tag{4.35}$$

and can be characterized by ω_0, Q_0 and H_0 as given by (4.36), (4.37) and (4.38) respectively.

$$\omega_0|_{HP} = \sqrt{\frac{G_1G_2}{C_2C_3}} \tag{4.36}$$

$$Q_0|_{HP} = \frac{\sqrt{G_1C_2C_3}}{\sqrt{G_2(C_1+C_2+C_3)}} \tag{4.37}$$

$$H_0|_{HP} = -C_1/C_3 \tag{4.38}$$

The BP response with proper admittance choices from Table 4.4 can be deduced as

$$\left.\frac{V_0}{V_{in}}\right|_{BP} = \frac{-sG_1/C_2}{s^2+s(G_3(C_1+C_2)/C_1C_2)+(G_3(G_1+G_2)/C_1C_2)} \quad (4.39)$$

The filter parameters ω_0, Q_0 and H_0 can be expressed as

$$\omega_0|_{BP} = \sqrt{\frac{(G_1+G_2)G_3}{C_1C_2}} \quad (4.40)$$

$$Q_0|_{BP} = \frac{\sqrt{C_1C_2(G_1+G_2)}}{\sqrt{G_3}(C_1+C_2)} \quad (4.41)$$

$$H_0|_{BP} = \frac{-G_1C_1}{G_3(C_1+C_2)} \quad (4.42)$$

Thus it is clear that no component matching / conditions on components are required for all the three responses.

4.3.2.1 Sensitivity Analysis

The passive sensitivities of ω_0 and Q_0 for the LPF can be computed as

$$S_{G_1}^{\omega_0} = 0, S_{G_2}^{\omega_0} = S_{G_3}^{\omega_0} = \frac{1}{2}, S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2} \quad (4.43)$$

$$S_{G_1}^{Q_0} = -1 + \frac{G_1}{(G_1+G_2+G_3)}, S_{G_2}^{Q_0} = \frac{1}{2} - \frac{G_2}{(G_1+G_2+G_3)}, \; S_{G_3}^{Q_0} = \frac{1}{2} - \frac{G_3}{(G_1+G_2+G_3)},$$

$$S_{C_1}^{Q_0} = -S_{C_2}^{Q_0} = \frac{1}{2} \quad (4.44)$$

The passive sensitivities of ω_0 and Q_0 for the HPF can be expressed as

$$S_{C_1}^{\omega_0} = 0, S_{C_2}^{\omega_0} = S_{C_3}^{\omega_0} = -\frac{1}{2}, S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = \frac{1}{2} \quad (4.45)$$

$$S_{C_1}^{Q_0} = -1 + \frac{C_1}{(C_1+C_2+C_3)}, S_{C_2}^{Q_0} = \frac{1}{2} - \frac{C_2}{(C_1+C_2+C_3)}, S_{C_3}^{Q_0} = \frac{1}{2} - \frac{C_3}{(C_1+C_2+C_3)}, S_{G_1}^{Q_0} = -S_{G_2}^{Q_0} = \frac{1}{2},$$

$$S_{G_1}^{Q_0} = -S_{G_2}^{Q_0} = \frac{1}{2} \quad (4.46)$$

The passive sensitivities of ω_0 and Q_0 for BPF can be computed as

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}, S_{G_1}^{\omega_0} = \frac{1}{2} - \frac{G_2}{2(G_1+G_2)}, S_{G_2}^{\omega_0} = \frac{1}{2} - \frac{G_1}{2(G_1+G_2)}, S_{G_3}^{\omega_0} = \frac{1}{2} \quad (4.47)$$

$$S_{C_1}^{Q_0} = \frac{1}{2} - \frac{C_1}{(C_1+C_2)}, S_{C_2}^{Q_0} = \frac{1}{2} - \frac{C_2}{(C_1+C_2)}, S_{G_1}^{Q_0} = \frac{1}{2} - \frac{G_2}{(G_1+G_2)},$$

$$S_{G_2}^{Q_0} = \frac{1}{2} - \frac{G_1}{(G_1+G_2)}, S_{G_3}^{Q_0} = -\frac{1}{2} \quad (4.48)$$

It is clearly observed from (4.43) to (4.48) that the passive sensitivities for all the three responses are lower than 1/2 in magnitude and therfore the filter configuration can be termed as insensitive.

4.3.2.2 Nonideality Analysis

The filter responses expressed by (4.31), (4.35) and (4.39) are derived considering the ideal behaviour of OTRA. In practice due to parasitics of OTRA the ideal responses get modified and can be represented as

$$\left.\frac{V_0}{V_{in}}\right|_{LP\_n} = \frac{\frac{-G_1 G_2}{C_1(C_2+C_p)}}{s^2+s\left(\frac{(G_1+G_2+G_3)}{C_1}\right)+\left(\frac{G_2 G_3}{C_1(C_2+C_p)}\right)} \quad (4.49)$$

$$\left.\frac{V_0}{V_{in}}\right|_{HP\_n} = \frac{-s^2 C_1/C_3}{s^2+s\left(\frac{(G_2+sC_p)(C_1+C_2+C_3)}{C_2 C_3}\right)+\left(\frac{G_1(G_2+sC_p)}{C_2 C_3}\right)} \quad (4.50)$$

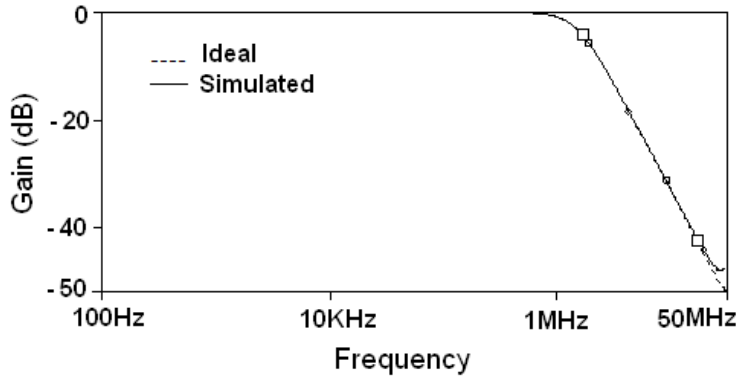
$$\left.\frac{V_0}{V_{in}}\right|_{BP\_N} = \frac{-sG_1/C_2}{s^2+s\left(\frac{(G_3+sC_p)(C_1+C_2)}{C_1 C_2}\right)+\left(\frac{(G_3+sC_p)(G_1+G_2}{C_1 C_2}\right)} \quad (4.51)$$

The effect of C_p in case of LP response can be eliminated by pre-adjusting the value of C_2

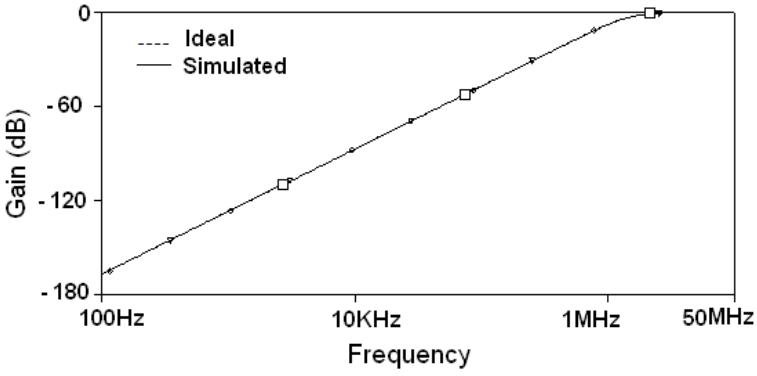
thus achieving self-compensation. The sC_p term appearing in parallel to G_2 in HP response and G_3 in BP response will introduce parasitic poles in the filter functions. The effect of the parasitic pole so introduced in HP and BP responses can be ignored by selecting the C_2 and C_3 to be much higher than the C_p thereby keeping the parasitic pole frequency far off from the filter poles.

4.3.2.3 Simulation Results

The proposed filter circuits are verified through PSPICE simulations while using CMOS OTRA realization of Fig 2.9. The LP and HP filter configurations were designed to give Butterworth response for an f_0 of 1.5 MHz. For LP response the capacitors are chosen as C_1 = 450 pF, C_2 = 100 pF and the conductances are computed as $G_1 = G_2 = G_3$ = 2 mS. For HP response capacitances are chosen as $C_1 = C_2 = C_3$ = 100 pF and the conductances are calculated as G_1 = 2 mS, G_2 = 0.45 mS. The ideal and simulated LP and HP responses are shown in Fig. 4.7(a) and (b) respectively and it may be noted that both the responses the ideal and simulated curves are in close agreement.



(a)



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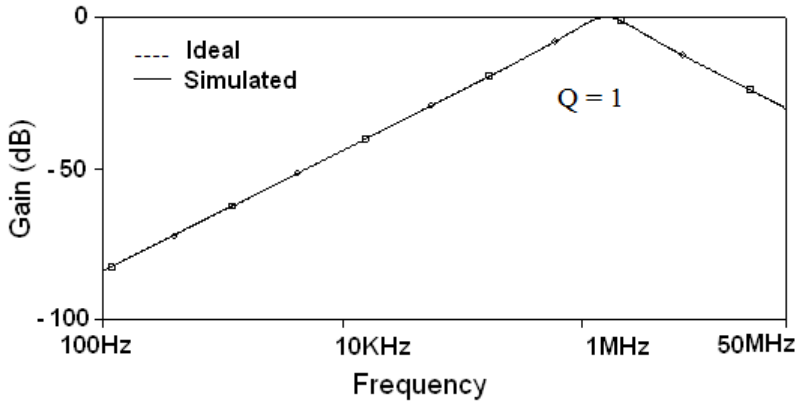
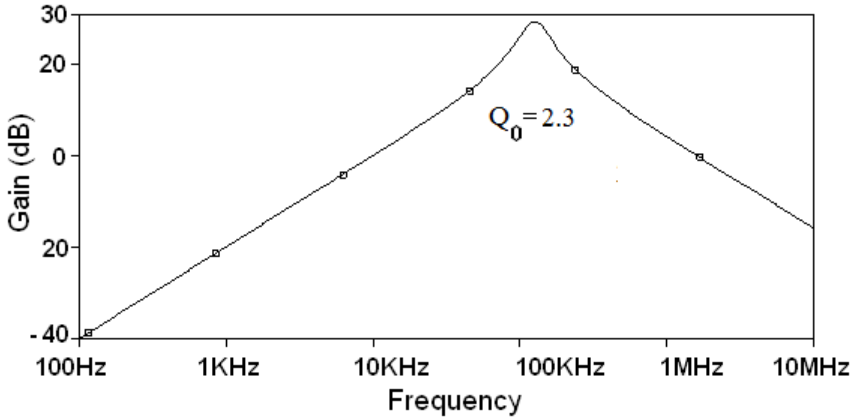


(c)



(d)

Fig. 4.7 Frequency responses of SAB topology -II. (a) LP. (b) HP. (c) BP for f_0 = 1.6 MHz, Q_0 = 1. (d) BP for f_0 = 125 KHz, Q_0 = 2.3.

The BP response having center frequency f_0 = 1.6 MHz and Q_0 = 1 is shown in Fig. 4.7(c) for which C_1 and C_2 are chosen as 10 pF and accordingly the conductance are computed as $G_1 = G_2 = 0.1$ mS and $G_3 = 0.03125$ mS. The BP response for an f_0 = 125 KHz and Q_0 = 2.3 is shown in Fig. 4.7(d). It is obsereved that the theoretical and simulated behaviours of the filter are in close agreement.

4.4 OTRA BASED MULTIAMPLIFIER FILTERS

In this section multiple OTRAs based filters have been discussed which can realize biquads and higher order filter functions. In this section a multiamplifier biquadratic universal filter is proposed which is followed by the design of a multiamplifier higher order filter based on wave method.

4.4.1 Biquadratic Universal Filter

Many voltage-mode biquadratic universal filters using multiple OTRAs are available in open literature [36], [42], [44], [45], [47]. The structures available in [36], [44], [45] are SISO type and those presented in [42], [47] are MISO type and provide only one standard filter function at a time. Exhaustive survey suggests that though OTRA based SIMO [36], [46] and MIMO [48] structures providing multiple outputs are available in open literature yet none can provide more than three outputs simultaneously and do not qualify for universal filter. To fill this gap a SIMO universal filter which realizes all five standard responses is proposed and discussed in this section. The proposed universal filter is shown in Fig. 4.8. Using straightforward analysis of circuit of Fig. 4.8 the transfer functions at various nodes can be obtained as

$$\frac{v_{o1}}{v_{in}} = \frac{s^2 G_1 C_1 C_2}{D(s)} \tag{4.52}$$

$$\frac{v_{o2}}{V_{in}} = \frac{sC_2 G_1 G_4}{D(s)} \tag{4.53}$$

$$\frac{v_{o3}}{v_{in}} = \frac{G_1 G_4 G_6}{D(s)} \tag{4.54}$$

$$\frac{v_{o4}}{v_{in}} = \frac{\frac{G_7}{G_9} s^2 C_1 C_2 G_1 + \frac{G_8}{G_9} G_1 G_4 G_6}{D(s)} \tag{4.55}$$

$$\frac{v_{o5}}{v_{in}} = \frac{\frac{G_7 G_{11}}{G_9 G_{12}} s^2 C_1 C_2 G_1 - \frac{G_{10}}{G_{12}} sC_2 G_1 G_4 + \frac{G_8 G_{11}}{G_9 G_{12}} G_1 G_4 G_6}{D(s)} \tag{4.56}$$

where $D(s) = s^2C_1C_2G_3 + sC_2G_4G_5 + G_2G_4G_6$ and $G_i = \frac{1}{R_i}$ (4.57)

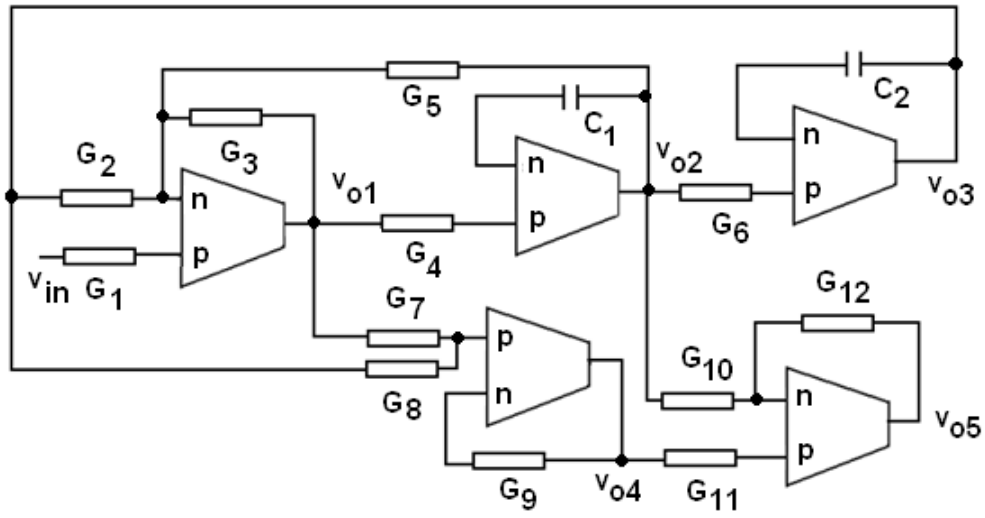


Fig. 4.8 Proposed biquadratic universal filter.

Equations (4.52) – (4.56) clearly indicate that HP, BP, LP, BR and AP responses are available at $v_{o1}, v_{o2}, v_{o3}, v_{o4}$ and v_{o5} respectively. BR and AP responses are obtained subjected to conditions given by (4.58) and (4.59) respectively.

$G_7 = G_9,\ G_1G_8 = G_2G_9$ (4.58)

$G_1G_{10} = G_5G_{12},\ G_7G_{11} = G_9G_{12},\ G_1G_8G_{11} = G_2G_9G_{12}$ (4.59)

Using (4. 52) – (4.56), various filter gains can be computed as

$G_{HP} = G_{BR} = G_{AP} = \frac{G_1}{G_3}, G_{BP} = \frac{G_1}{G_5}, G_{LP} = \frac{G_1}{G_2}$ (4.60)

The ω_0 and the Q_0 can be characterized by

$\omega_0 = \sqrt{\frac{G_2G_4G_6}{C_1C_2G_3}}$ (4.61)

$Q_0 = \frac{1}{G_5}\sqrt{\frac{C_1G_2G_3G_6}{C_2G_4}}$ (4.62)

This suggests that the Q_0 can be independently controlled by varying G_5 without affecting the ω_0. It can be noted from (4.61) that simultaneous adjustment of G_2 and G_4 results in orthogonal tuning of ω_0. Also the filter gain can be controlled through G_1 without affecting ω_0 and Q_0. The sensitivities of ω_0 and Q_0 with respect to each passive component are low and can be obtained as

$$S_{G2}^{\omega_0} = S_{G4}^{\omega_0} = S_{G6}^{\omega_0} = \frac{1}{2}, S_{G3}^{\omega_0} = S_{C1}^{\omega_0} = S_{C2}^{\omega_0} = -\frac{1}{2} \tag{4.63}$$

$$S_{G5}^{Q_0} = 1,\ S_{C1}^{Q_0} = S_{G2}^{Q_0} = S_{G3}^{Q_0} = S_{G6}^{Q_0} = \frac{1}{2}, S_{G4}^{Q_0} = S_{C2}^{Q_0} = -\frac{1}{2} \tag{4.64}$$

The expressions for sensitivity are simpler and independent of components used in contrast to SAB topologies of Fig. 4.1 and Fig. 4.5.

4.4.1.1 MOS–C Implementation

The proposed configuration is made fully integrated by implementing the resistors using matched transistors operating in linear region as explained in section 2.8. The MOS-C implemented universal filter configuration is shown in Fig. 4.9. The resistance value may be

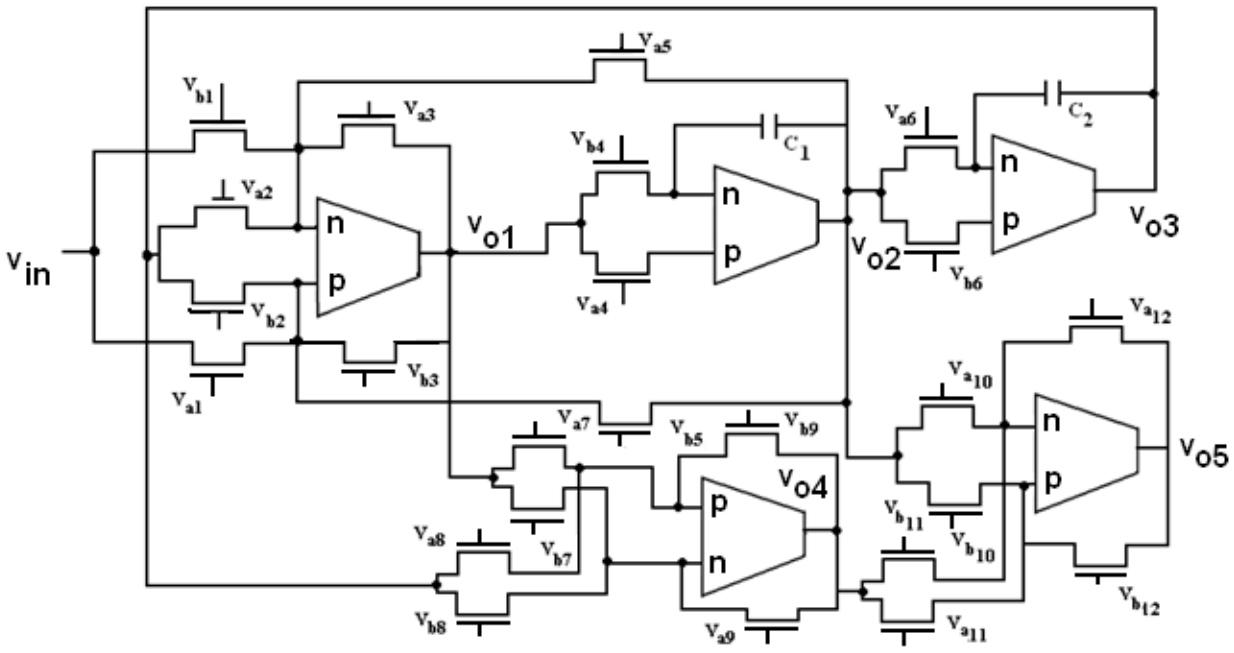


Fig. 4.9 OTRA MOS-C universal filter.

adjusted by appropriate choice of gate voltages thereby making filter parameters electronically tunable. It also exhibits the feature of orthogonal controllability of ω_0 and Q_0 f through gate bias voltage.

4.4.1.2 Nonideality Analysis

The response of the filter may deviate due to nonideality of OTRA in practice.Taking this effect into account the transfer functions of the circuit of Fig. 4.8 modify to

$$\left.\frac{V_{01}}{V_{in}}\right|_n = \frac{s^2 G_1 (C_1+C_p)(C_2+C_p)}{D(s)} \tag{4.65}$$

$$\left.\frac{V_{02}}{V_{in}}\right|_n = \frac{s(C_2+C_p)G_1 G_4}{D(s)} \tag{4.66}$$

$$\left.\frac{V_{03}}{V_{in}}\right|_n = \frac{G_1 G_4 G_6}{D(s)} \tag{4.67}$$

$$\left.\frac{V_{04}}{V_{in}}\right|_n = \frac{\frac{G_7}{(G_9+sC_p)}s^2(C_1+C_p)\,(C_2+C_p)\,G_1 + \frac{G_8}{(G_9+sC_p)}G_1 G_4 G_6}{D(s)} \tag{4.68}$$

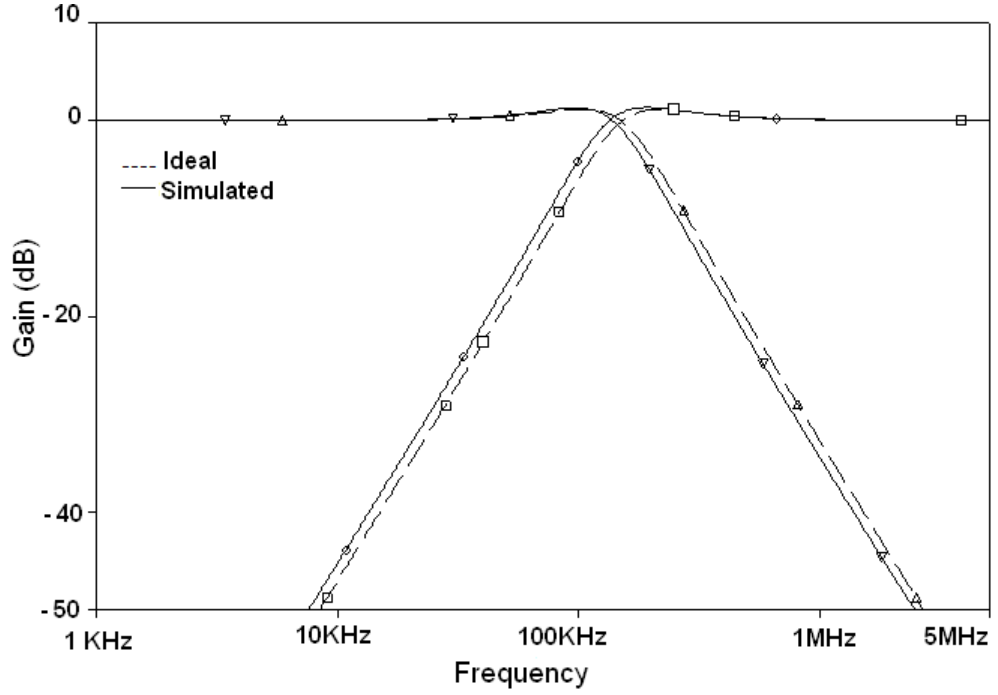
$$\left.\frac{V_{05}}{V_{in}}\right|_n = \frac{\frac{G_7 G_{11}}{G_9(G_{12}+sC_p)}s^2(C_1+C_p)\,(C_2+C_p)G_1 - \frac{G_{10}}{(G_{12}+sC_p)}s\,(C_2+C_p)G_1 G_4 + \frac{G_8 G_{11}}{(G_{12}+sC_p)(G_9+sC_p)}G_1 G_4 G_6}{D(s)} \tag{4.69}$$

where $D(s) = s^2(C_1+C_p)(C_2+C_p)(G_3+sC_p) + s(C_2+C_p)G_4 G_5 + G_2 G_4 G_6$ (4.70)

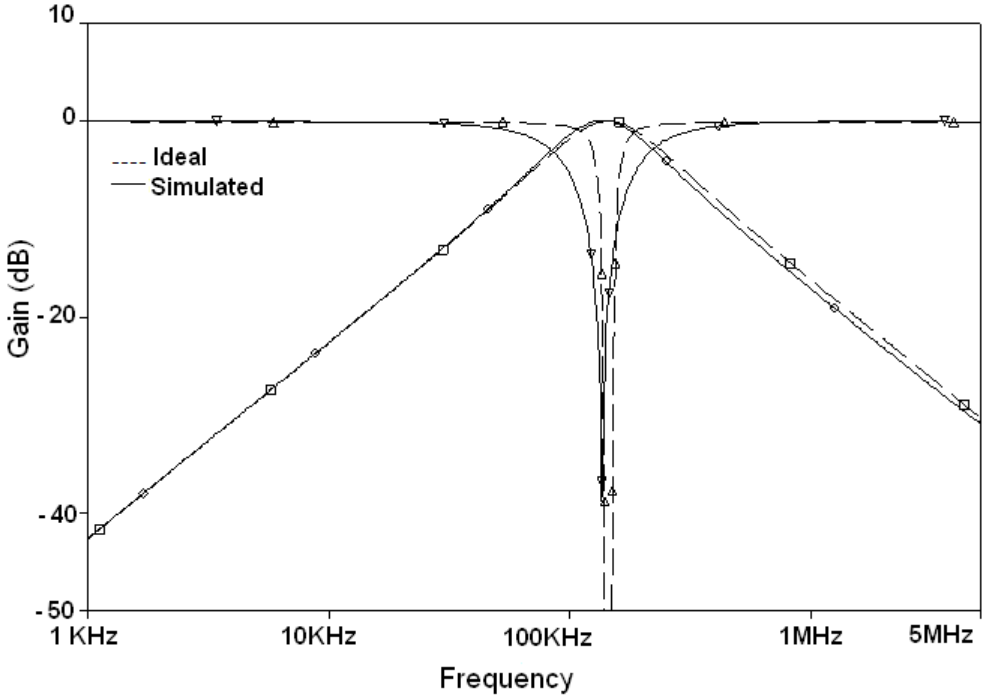
The effect of C_p can be eliminated by pre-adjusting the value of capacitors C_1 and C_2 and thus achieving self-compensation. The sC_p term appearing in parallel to G_i for i = 3,9,12 will result in introduction of parasitic pole having radian frequency as $\omega = G_i/C_p$. By selecting the circuit components C_1 and $C_2 >> C_p$ the parasitic pole can be placed far away from the filter poles and thereby the effect of this additional pole can be eleminated.

4.4.1.3 Simulation Results

The working of the proposed SIMO biquadratic universal filter is verified through SPICE simulations. For simulations aspect ratio for all transistors used for resistance realization is taken as W/L = 5µm/5µm. The proposed SIMO biquadratic universal filter is designed for the resonant frequency (f_0) of 120 KHz and $Q_0 = 1$ with component values $C_1 = C_2 = 100$ pF and for which $R_i \approx 10.5$ KΩ for i = 1, 2 . . . 12. The value of R_i was set by taking the gate voltages as $V_{ai} = 1.4$ V and $V_{bi} = 0.75$ V for all i = 1, 2, . . . , 12. Figure 4.10 shows the simultaneously available LP, HP, BP, BR and AP frequency responses. The ideal and simulated responses are found to be in close agreement. Simulated power consumption for the proposed universal filter is 4.04 mW. Orthogonal tunability of Q_0 with R_5 at f_0 = 11.5 KHz is shown in Fig. 4.11 for BP filter. This is obtained by selecting $C_1 = C_2 = 50$ pF, and $R_i = 272$ KΩ for i = 1,…, 4, 6,…, 12 for different values of R_5. The values of Q_0 as obtained and gate bias voltages used for tuning of R_5 are listed in Table 4.5.



(a)



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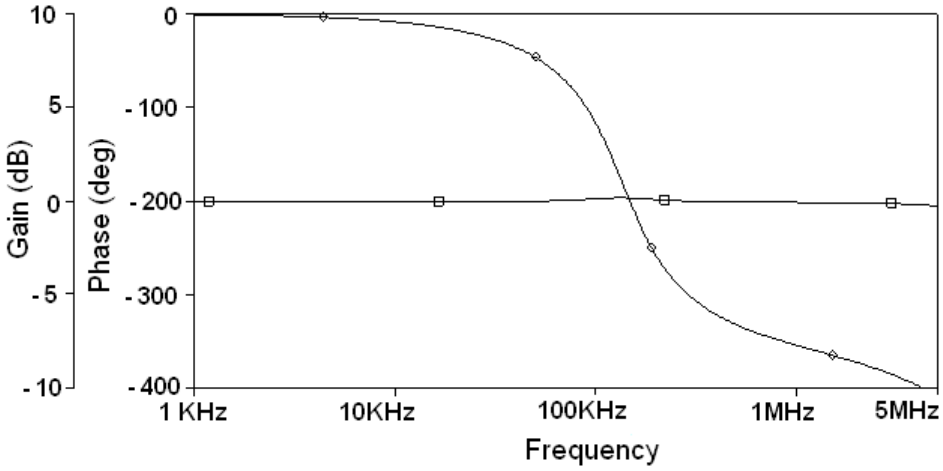


(c)

Fig. 4.10 Simulated frequency responses of the proposed circuit (a) LPF and HPF.

(b) BPF and BRF. (c) APF.

Table 4.5: Component values used for orthogonal tunability of Q_0.

S.No.	BiasVoltage V_{a5}(V)	Bias Voltage V_{b5}(V)	R_5(KΩ)	Q_0	f_0 (KHz)
1.	0.76	0.75	≈680	2.5	11.5
2.	0.80	0.75	≈136	0.5	11.5
3.	0.85	0.75	≈68	0.25	11.5
4.	0.95	0.75	≈34	0.125	11.5

The f_0 is electronically tunable by varying the gate voltage and is verified through simulations as depicted in Fig. 4.12 for BR filter. Values of f_0, for $C_1 = C_2 = 50$ pF and $R_i \approx 23$ KΩ for i = 1, 3, 5, ... , 12, along with different gate voltages chosen for simultaneously varying R_2 and R_4 are listed in Table 4.6.

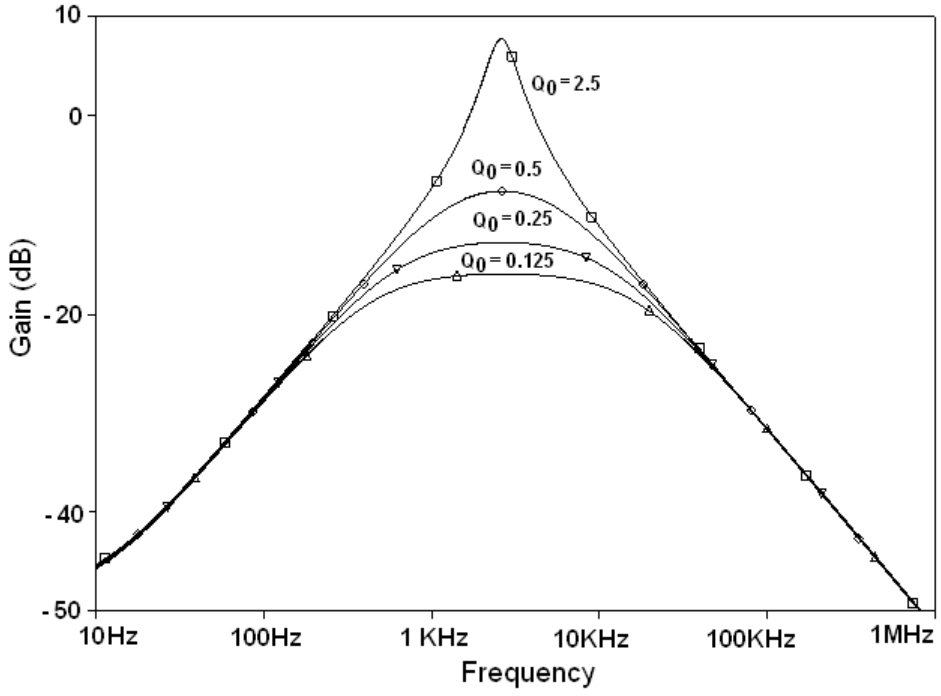


Fig. 4.11 BP response for different Q_0 values.

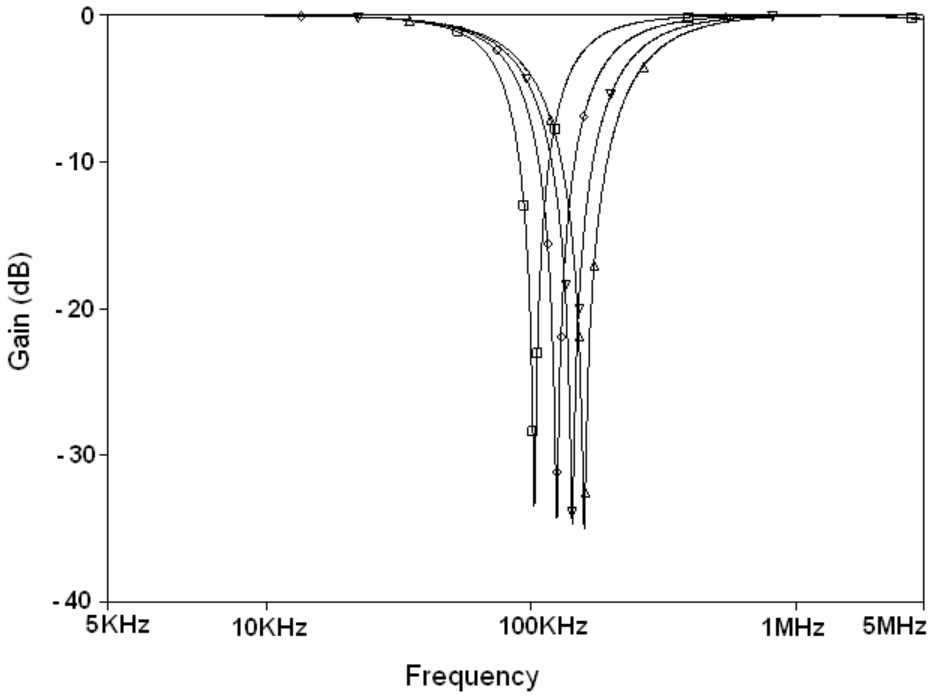
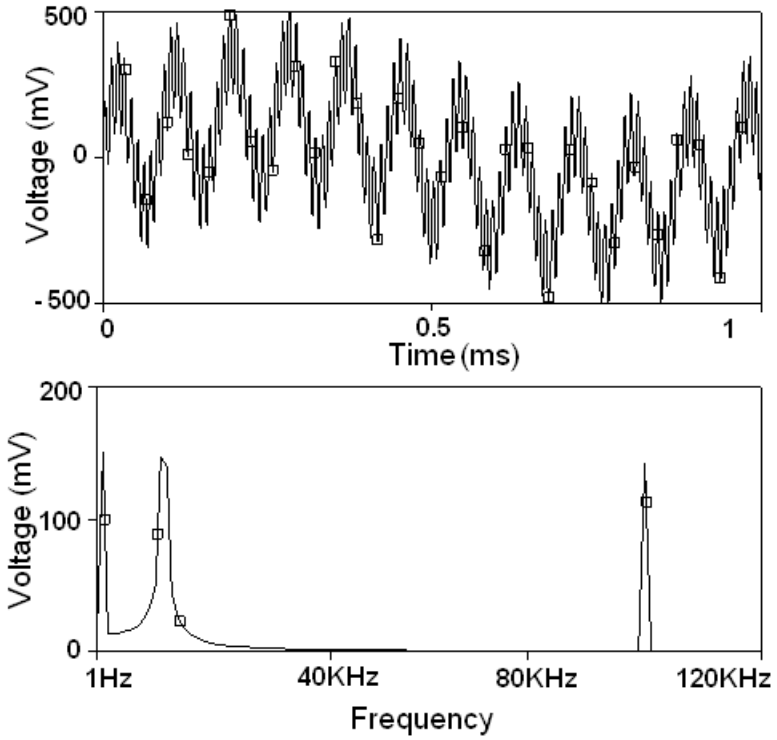


Fig. 4.12 BR response for different f_0 values.

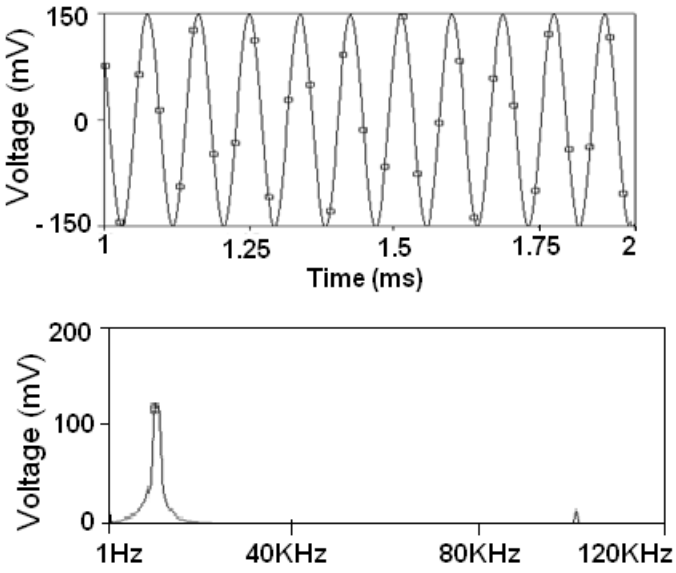
Table 4.6: Component values used to make f_0 electronically tunable.

S. No.	Bias Voltage V_{a4}(V)	Bias Voltage V_{b4} (V)	R_2, R_4 (KΩ)	f_0 (KHz)	Q_0
1.	1.1	0.9	≈34	113.8	1
2.	1.2	0.9	≈23	138.4	1
3.	1.3	0.9	≈17	160.0	1
4.	1.4	0.9	≈14	179.0	1

The time domain behavior of the BP filter is also studied by applying three sinusoidal frequency components, a low frequency signal of 1 KHz, a high frequency component of 100 KHz and the third component of 11.5 KHz which is f_0 of the BP filter. The transient response of the filter circuit is shown in Fig. 4.13. It may be noted that the frequency components other than f_0 are significantly attenuated.



(a)



(b)

Fig. 4.13 Simulated transient response of BP filter. (a) Input signal and its frequency spectrum (b) Output transient response and frequency spectrum.

To check the quality of the output of BP filter, the percentage total harmonic distortion (%THD) with the sinusoidal input signal is obtained as shown in Fig. 4.14. It is observed that the %THD remains considerably low [78] for input signal values till 60 mV. Simulated power consumption for the proposed universal filter is 4.04 mW.

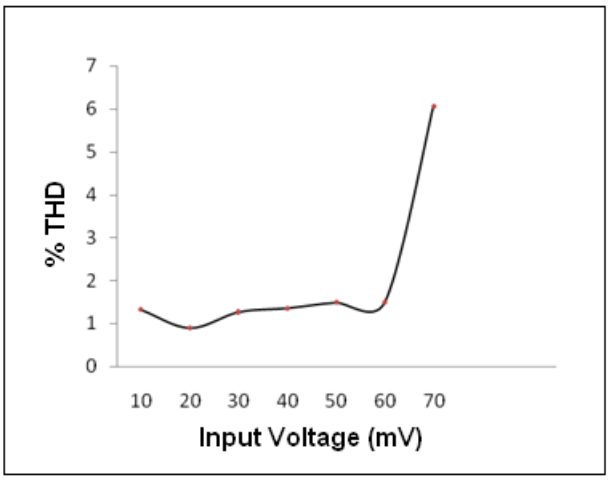


Fig. 4.14 % THD variation with input signal amplitude.

4.4.2 OTRA Based Higher Order Filters

There are many advantages of higher order filters using doubly terminated lossless ladders, like, low sensitivity to component tolerances, ample design information and design tables that can be readily applied. However, inductor realization in an integrated circuit is a challenging task. There are various techniques that circumvent these shortcomings like element replacement and operational simulation. In operational simulation signal flow graphs are used to emulate the relationship between various passive elements. These are then physically realized using lossy and lossless integrators [79]. Realiziation of lossless integrators is difficult because of non ideal characteristics of passive components used. Besides, floating capacitors are used in this topology, which are not very favorable in IC implementation. In the case of element replacement approach, inductors are replaced by gyrators. Although this practice leads to good results with low noise sensitivity, realizing high quality floating inductors proves to be difficult [79]. Another element replacement method using Frequency Dependent Negative Resistance (FDNR) was proposed by Bruton

[80], which works well with low pass filters. LC ladder filters can also be emulated using Linear Transformation approach wherein every section of the original ladder prototype can be realized by using active elements individually [81]. The only drawback of this method is that it uses lossless integrators.

Apart from these approaches, the wave method [79], is also used for realizing higher order resistively terminated LC ladder filters. It uses wave equivalents for different passive elements which can be readily substituted to realize a filter. In this approach, the filter realization is based on modeling the forward and reflected voltage waves. The available wave active filters [79], [82] – [88] use various active blocks such as OTA [82], current amplifier [83], CMOS cascode current mirror [84], FPAA [85], OPAMP [79], [86], CFOA [87], and DVCCCTA [88] and operate in current [82] – [85] and voltage [79], [86] – [88] mode. In this section design approach for realization of OTRA based higher order wave filter is presented. First the concept of wave filter is elaborated which is then employed for OTRA based wave filter realization. Simulation results for a third order Butterworth filter realized using wave method, are shown in subsequnt section.

4.4.2.1 Wave Filter Approach

The concept of wave filter is introduced in [79], [86]. This approach talks of applying scattering parameters to ladder filters. It uses voltage waves instead of power waves. Scattering matrix of a two port network is given as

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{4.71}$$

In a two port network having a series branch admittance Y, as shown in Fig. 4.15, the scattering parameters, assuming the normalization resistance as R_n, are obtained as

$$S_{11} = \frac{1}{2R_nY+1}, S_{12} = \frac{2R_nY}{2R_nY+1}, S_{21} = \frac{2R_nY}{2R_nY+1}, S_{22} = \frac{1}{2R_nY+1} \tag{4.72}$$

For a series branch inductance L, using (4.72), (4.71) reduces to

$$B_1 = \frac{1}{(\frac{2R_n}{sL})+1} A_1 + \frac{\frac{2R_n}{sL}}{(\frac{2R_n}{sL})+1} A_2 \quad (4.73)$$

$$B_2 = \frac{\frac{2R_n}{sL}}{(\frac{2R_n}{sL})+1} A_1 + \frac{1}{(\frac{2R_n}{sL})+1} A_2 \quad (4.74)$$

This can be further simplified to

$$B_1 = A_1 - \frac{1}{(1+s\tau_L)}(A_1 - A_2) \quad (4.75)$$

$$B_2 = A_2 + \frac{1}{(1+s\tau_L)}(A_1 - A_2) \quad (4.76)$$

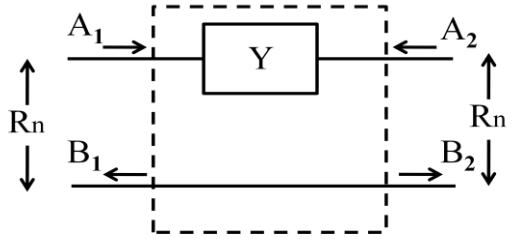


Fig. 4.15 Series branch admittance Y.

In (4.76) $\tau_L = L/2R_n$ is the time constant. Figure 4.16(a) shows the symbolic representation of the wave equivalent of series branch inductor L. To calculate the S-matrix for series branch capacitance C, (4.71) reduces to

$$B_1 = \frac{1}{2sCR_n+1} A_1 + \frac{2sCR}{2sCR_n+1} A_2 \quad (4.77)$$

$$B_2 = \frac{2sCR_n}{2sCR_n+1} A_1 + \frac{1}{2sCR_n+1} A_2 \quad (4.78)$$

Simplifying further (4.77) and (4.78) can be expressed as

$$B_1 = A_2 + \frac{1}{1+s\tau_C}(A_1 - A_2) \quad (4.79)$$

$$B_2 = A_1 - \frac{1}{1+s\tau_C}(A_1 - A_2) \tag{4.80}$$

where $\tau_C = 2CR_n$ is the time constant. It is observed that (4.75) and (4.76) are similar to (4.79) and (4.80) respectively, and can be obtained from each other by interchanging the output terminals B_1 and B_2. This result can be generalized to show that for a series branch admittance Y, its dual admittance (Y') can be obtained as

$$Y' = \frac{1}{4R_n{}^2 Y} \tag{4.81}$$

Accordingly the wave equivalent symbol of series branch capacitance C, can be drawn as shown in Fig. 4.16 (b).

(a) (b)

Fig. 4.16 Wave equivalent of series branch elements. (a) Inductance L, $\tau_L = L/2R_n$.

(b) Capacitance C, $\tau_C = 2CR_n$.

For an inductor L connected in series with capacitance C in a series arm the wave equivalent can be obtained by cascading the wave equivalents of L and C. If the terminals are interchanged, the wave equivalent for a tank circuit connected in series branch can be obtained. Table 4.7 [79], [86] gives wave equivalents for all the series branch elements. Proceeding in a similar manner, wave equivalents for shunt branch elements can also be derived. Table 4.8 [79], [86] lists the results for shunt branch elements.

Table 4.7: Wave equivalents of series branch elements [79], [86].

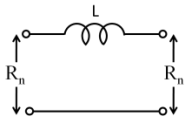
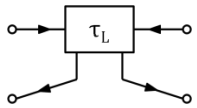
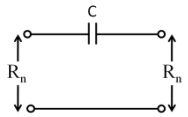
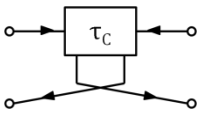
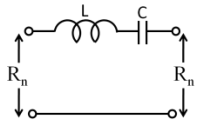
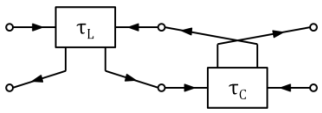
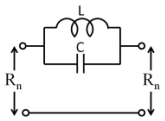
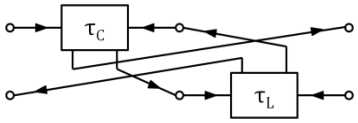
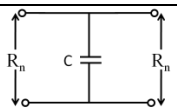
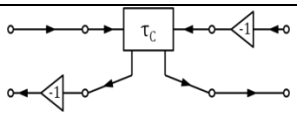
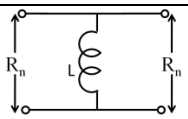
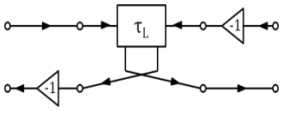
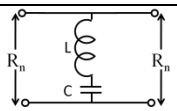
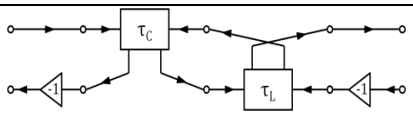
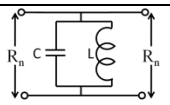
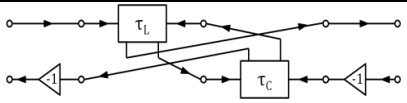
Series Branch Elements	Wave Equivalents
	
	
	
	

Table 4.8: Wave equivalents of shunt branch elements [79], [86].

Shunt Branch Elements	Wave Equivalents
	
	
	
	

4.4.2.2 OTRA Based Wave Active Filter

In this section a systematic approach for realizing higher order resistively terminated LC ladder filters, using wave method, which employs OTRA has been discussed. A closer study of (4.75),

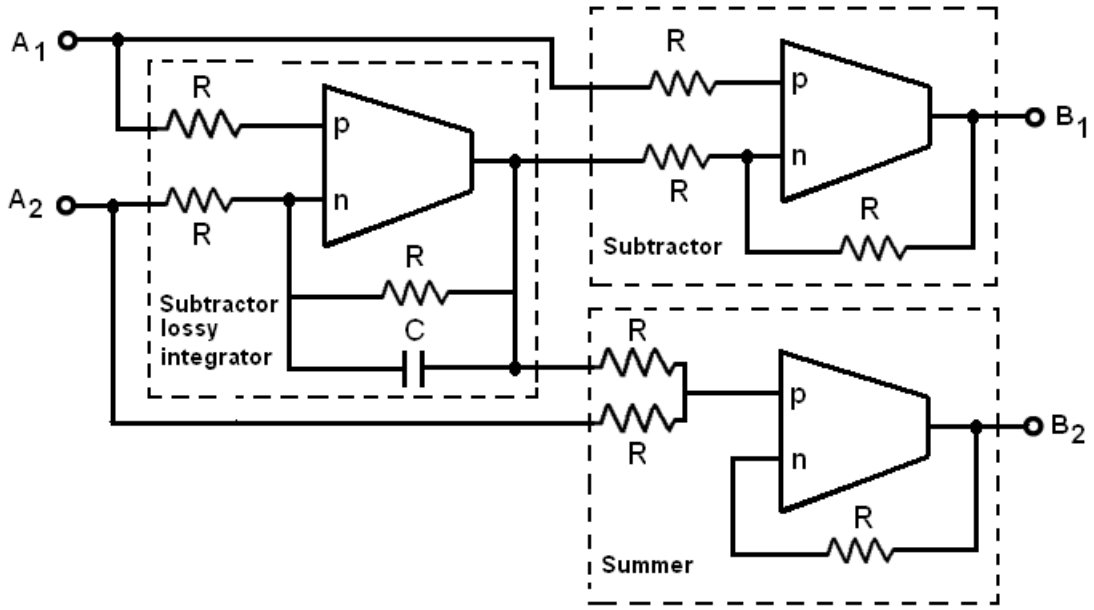


Fig. 4.17 OTRA based wave equivalent of series branch inductor.

Using these blocks the wave equivalent for a series branch inductor, defined by (4.75) and (4.76) represented symbolically by Fig. 4.16 (a), can be obtained and is shown in Fig. 4.17. The dashed blocks indicate the OTRA based basic circuits constituting the wave equivalent of series branch inductor. The MOS-C equivalent of circuit of Fig. 4.17 is shown in Fig. 4.18 wherein all passive resistors are implemented using MOS transistors operating in non saturation region. This elementary block alongwith inverter can now be used to synthesize the wave equivalents for all the elements listed in Table 4.7 and Table 4.8. The circuit in Fig. 4.17 can be described by the following equations

$$B_1 = A_1 - \frac{1}{1+sCR}(A_1 - A_2) \tag{4.82}$$

$$B_2 = A_2 + \frac{1}{1+sCR} \quad (A_1 - A_2) \tag{4.83}$$

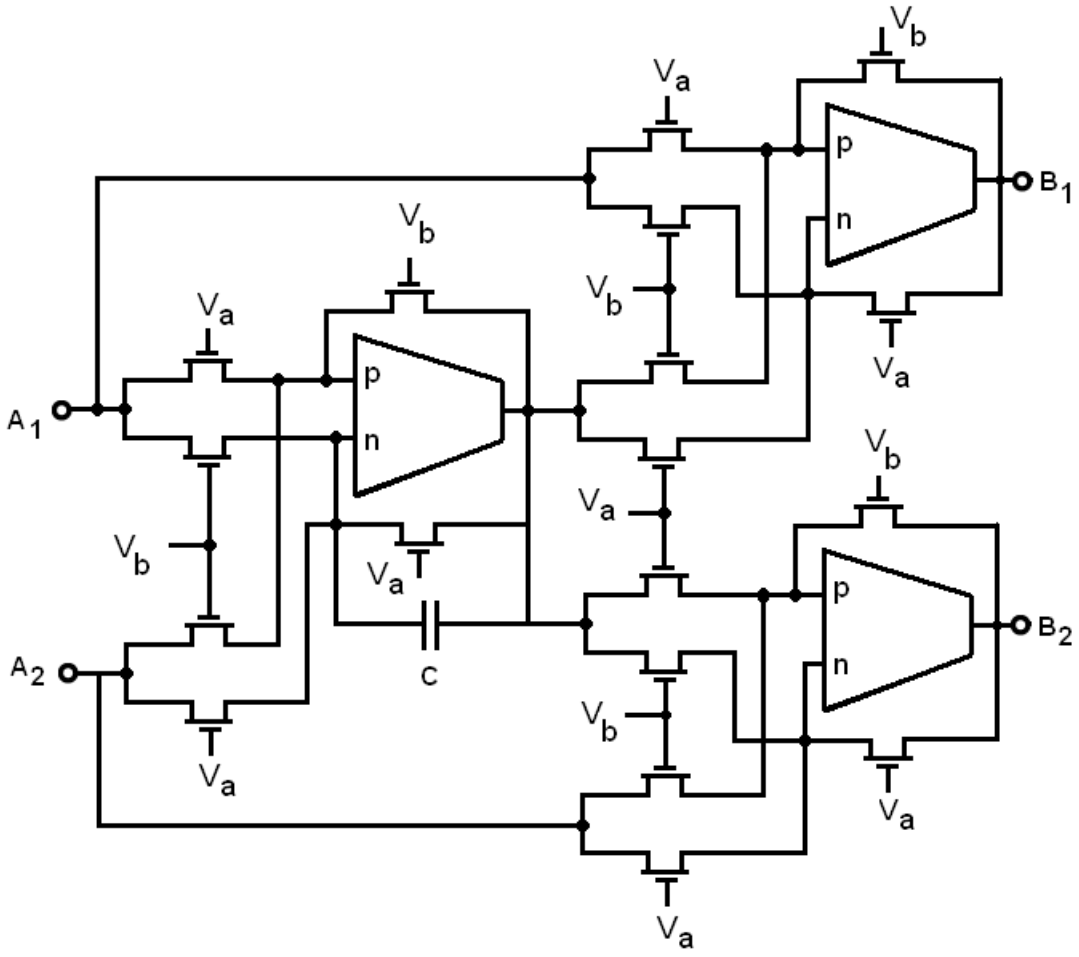


Fig. 4.18 MOS–C equivalent of series branch inductor.

The actual value of inductance L_A realized by circuit of Fig. 4.17 would be obtained by comparing (4.82) with (4.75) or (4.83) with (4.76). The realized value can be expressed as

$$L_A = 2R_nCR \tag{4.84}$$

Similarly, comparing (4.82) and (4.79) or (4.83) and (4.80), the capacitance value realized (C_A) can be written as

$$C_A = \frac{CR}{2R_n} \tag{4.85}$$

Similarly, the actual values of L and C for wave equivalents of shunt branch elements can be given by

$$L_A = \frac{R_n CR}{2} \tag{4.86}$$

$$C_A = \frac{2CR}{R_n} \tag{4.87}$$

For a filter if L_n and C_n are the normalized inductor and capacitor values respectively, ω_0 be the normalizing pole frequency and R_n is the normalizing resistance, then to de-normalize L_n and C_n following expressions can be used

$$L_A = \frac{R_n}{\omega_0} L_n \tag{4.88}$$

$$C_A = \frac{1}{R_n \omega_0} C_n \tag{4.89}$$

Using different notation of C for L_A and C_A, i.e. C_L and C_C respectively, (4.84) and (4.85) can be restated as

$$L_A = 2R_n C_L R \tag{4.90}$$

$$C_A = \frac{C_C R}{2R_n} \tag{4.91}$$

From (4.88) - (4.91) C_L and C_C can be expressed as

$$C_L = \frac{1}{2\omega_0 R} L_n \tag{4.92}$$

$$C_C = \frac{2}{\omega_0 R} C_n \tag{4.93}$$

The expression, for controlling ω_0 using R, needs to be worked out for each circuit. A simple algorithm can be worked out to achieve the exact expression and range of tunability. For the frequency ω_0, C_L and C_C are calculated in terms of R, as per the L_n and C_n values. For a suitable R value, once C_L and C_C have been fixed, either equation (4.92) or (4.93) can be used to describe the relationship between R and ω_0 as

$$\omega_0 = \frac{K}{R} \tag{4.94}$$

K can be expressed as

$$K = \frac{2C_n}{C_C} = \frac{L_n}{2C_L} \tag{4.95}$$

Substituting R from (2.41) in (4.94) one may get

$$\omega_0 = KK_n(V_a - V_b) \tag{4.96}$$

Equation (4.96) describes the electronic tunability of ω_0 by varying gate votages V_a and /or V_b of the transistors used to implement the linear resistor.

4.4.2.3 Simulation Results

To demonstrate the wave filter approach using OTRA, a doubly terminated third order Butterworth low pass filter (LPF), as shown in Fig. 4.19, has been implemented and simulated using SPICE. The normalized values of components are L_{n1} = 2, C_{n1} = 1 and C_{n2} = 1.The design specifications of LPF are taken to be f_P = 200 KHz and maximum attenuation in pass band α_{MAX} is 3 dB.

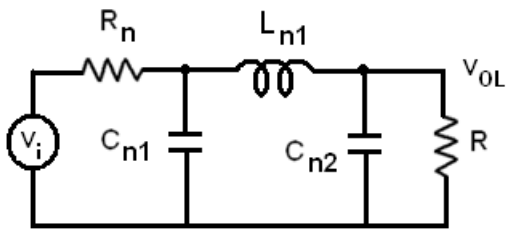


Fig. 4.19 3rd order low pass Butterworth filter.

The value of normalizing resistance R_n is chosen to be 2.5 KΩ. De-normalizing the values of L_{n1}, C_{n1} and C_{n2}, L_A and C_A can be computed as

$$L_A = 3.98 \text{ mH}, C_{A1} = C_{A2} = 318.31 \text{ pF} \tag{4.97}$$

Setting R initially to 12 KΩ, the value of C_L for L_{A1} can be calculated as 66.33 pF and that of C_C for C_{A1} and C_{A2} as 132.66 pF. The value of K, as per (4.95) is 1.508×10^{10}. The W/L ratio for the transistors used for implementing linear resistors is taken as 10µm/2.5µm. For this simulation exercise, the value of K_N was found to be 5.25×10^{-4} A/V^2. The required V_a and V_b values for R to be 12 KΩ were computed to be 0.908 V and 0.75 V. The wave

equivalent circuit of the LPF is shown in Fig. 4.20 in which the reflected waves are available at v_{OL} and v_{OH}. These outputs complement each other by virtue of wave theory [86]. Thus as the v_{OL} represents the LPF response; its complementary high pass output is available at v_{OH}. Fig. 4.21 shows the simulated LPF response of the circuit at v_{OL}. The complementary high pass output v_{OH}, as represented in Fig. 4.20, has been plotted in Fig. 4.22. The proposed circuit can be tuned to different cut-off frequencies by controlling the voltage difference (V_a - V_b) as described by (4.96). Comparison between theoretical and the observed frequencies obtained by variation of control voltage difference (V_a - V_b) is shown in Fig. 4.23.

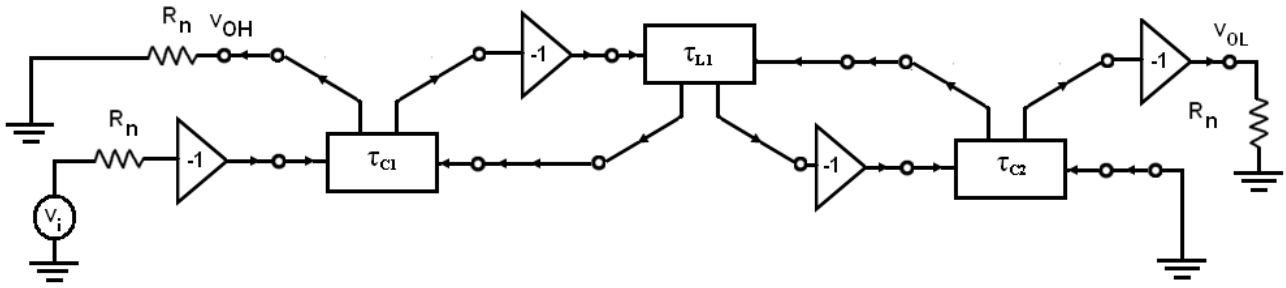


Fig. 4.20 Wave equivalent of circuit of LPF of Fig. 4.19.

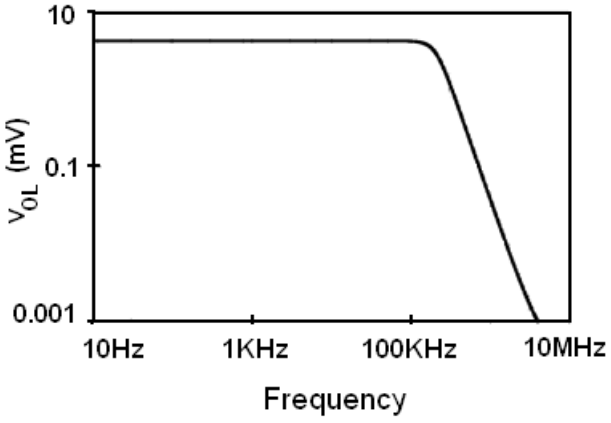


Fig. 4.21 LP response (V_{OL}).

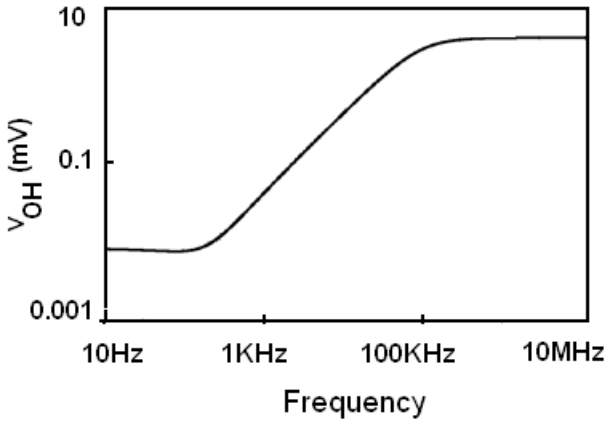


Fig. 4.22 Complementary HP response (V_{OH}).

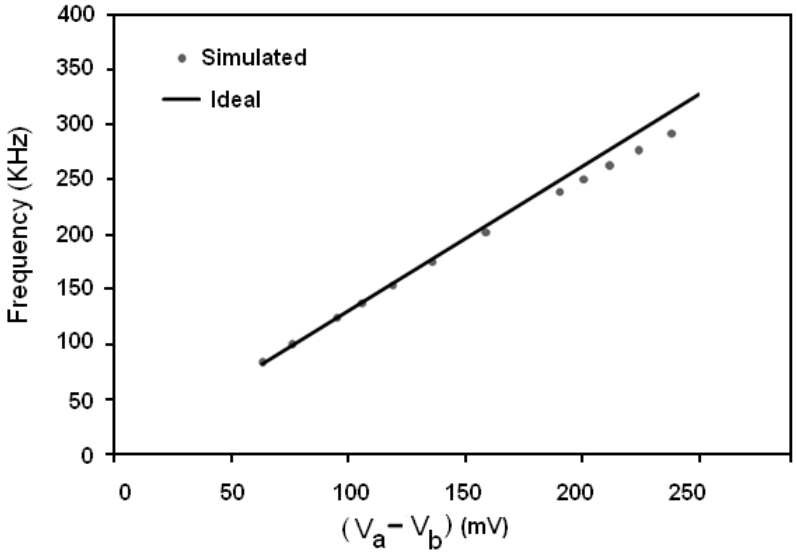


Fig. 4.23 Comparison curve between theoretical and observed frequency.

The performance comparision of the proposed circuit with the previous voltage mode structures [79], [86] – [88] is summarized in Table 4.9. It may be noted that the topology presented in [78] shows best THD result, however the structure is not electronically tunable. Although the most recently reported work [88] is having better THD performance its simulated power consumption is higher as compared to the proposed one. The relevant data for structures of [79], [86] is not available in the literature, which are designed using commercially available op-amps.

Table 4.9: Comparison with the voltage mode filter structures.

Ref	Active block and technology used	Filter structure	% THD	Power consumption (mW)	Output noise voltage ($V/HZ^{1/2}$)	Electronic tunability
[78]	CFOA (Commercially available IC AD844 with ± 5V power supply)	3rd order elliptic Low pass	1% for 1V pp signal	Not available	Not available	No
[79]	DVCCCTA (CMOS Technology- 0.25µm, Power supply ± 1.25V)	4th order Butterworth Low pass	Less than 5% up to 225 mV pp signal	59.2	8.36×10^{-8}	Yes
Proposed work	OTRA CMOS Technology- (0.5µm, Power supply ±1.5 V)	3rd order Butterworth Low pass	Less than 5% up to 125 mV pp signal	10.7	7.28×10^{-8}	Yes

4.5 CONCLUDING REMARKS

Single and multi amplifier based VM filter topologies are proposed in this chapter. SAB is a preferred choice when low power consumption is the primary design concern. To cater this design need two SAB topologies are presented which can be used to synthesize LP, HP and

BP filter functions with appropriate admittance choices. These topologies do not impose any matching constraints on components, in contrast to all existing structures. The first configuration is based on Sallen Key approach while the second is based on multiple feedback topology. High Q_0 realization with moderate component spread and independent adjustment of ω_0 and Q_0 are the high points of the first topology. Passive sensitivities for both the configuration are quite low, though are dependent on components used.

Multiamplifier filters are superior to SABs in terms of passive sensitivity and versatility; basis enough to explore multiamplifier design and has led to the design of two; multiamplifier filter topologies. A universal biquadratic filter realizing all five standard filter functions simultaneously is proposed first. The filter parameters ω_0 and Q_0 can be orthogonally tuned. This is succeeded by design details of higher order resistively terminated LC ladder using wave method and is implemented through multiple OTRAs. It uses wave equivalents for different passive elements which can be readily substituted in higher order resistively terminated LC ladder to realize a filter. MOS-C implementation of universal biquad and wave active filter configurations is also presented which makes filter parameters electronically tunable.

All proposed structures are validated through SPICE simulations. The effect of nonidealities of OTRA on filter responses is also analysed.

CHAPTER – 5
SIGNAL GENERATORS USING OTRA

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey, Mayank Bothra,and Sajal K. Paul **"Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators,"** Journal of Electrical and Computer Engineering Volume 2011, Article ID 586853, 8 pages doi:10.1155/2011/586853.

2. Rajeshwari Pandey, Neeta Pandey, Rajendra Kumar, and Garima Solanki, **"A Novel OTRA Based Oscillator with Non Interactive Control,"** International Conference on Communication and Computer Technology (ICCCT'10), pp.658 – 660, Sept.2010.

3. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul "**MOS-C Third Order Quadrature Oscillator using OTRA,"** Third International Conference on Communication and Computer Technology (ICCCT'12), pp.77 – 80, Nov. 2012.

5.1 INTRODUCTION

Signal generators are an important class of circuits and find wide application in communication, instrumentation and measurement, and control systems. Generating signal carriers for information transmission, clock pulses for timing and control, test signals for automatic test and measurement and audio signals for music and speech synthesis are some of the most common examples.These systems require signals of variuos standard shapes such as sinusoidal, square, triangular, sawtooth etc. Thus the function of a signal generator is to produce a waveform of prescribed characteristics such as shape, frequency, amplitude, and duty cycle. Sometimes these characteristics are designed to be programmable via some suitable external control signals. In general, signal generators employ some form of feedback together with devices possessing frequency dependent characteristis to produce signals. Signal generators can broadly be classified as (i) Harmonic/Sinusoidal oscillators and (ii) Non linear/Relaxation oscillators. Sinusoidal oscillators are also termed as linear oscillators. In this chapter design of various sinusoidal oscillators using OTRA is dealt with. In the following section a review of reported work on sinusoidal oscillators is presented.

5.2 SINUSOIDAL OSCILLATOR

The sine wave is one of the most fundamental waveforms since any other waveform can be expressed as a Fourier combination of basic sine waves. Sinusoids can be generated either by appropriate shaping the triangular waveform or through a positive feedback loop consisting of an amplifier and a frequency selectve network. All the proposed circuits discussed in this chapter utilize the positive feedback approach which is described briefly in this section.

The functional block diagram of a positive feedback loop consisting an amplifier having transfer function $A(s)$ and a frequency selective network with transfer function β (s) is shown in Fig. 5.1, wherein x_s and x_o represent the input and output signals respectively and x_f is the feedback signal.The closed loop gain $A_f(s)$ of this system can be derived as

$$A_f(s) = \frac{A(s)}{1-A(s)\beta(s)} \tag{5.1}$$

The characteristic equation of this system can thus be written as

$$1 - A(s)\beta(s) = 0 \tag{5.2}$$

where $A(s)\beta(s)$ is called the loop gain $L(s)$. If at a specific frequency the loop gain of this system is equal to unity then A_f will be infinite implying that at this frequency the circuit will have a finite output for zero input signal. Such a circuit is by definition is an oscillator. Thus the condition for the closed loop system to provide sustained oscillations of frequency ω_0 can be represented as

$$L(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1 \tag{5.3}$$

This condition is known as the Barkhuasen criterion. For the circuit to oscillate at a single frequency the oscillation criterion must be satisfied for a single frequency only; else the resulting waveform will not be a simple siusoid.

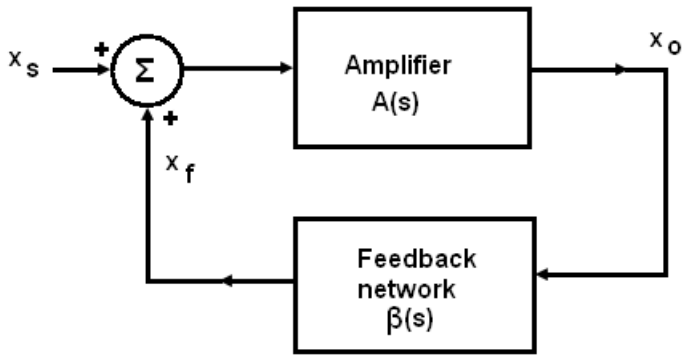


Fig. 5.1 Functional block of a sinusoidal oscillator.

In following subsections sinusoidal oscillators that provide single phase, quadrature phase and multiphase ouputs have been proposed. All the proposed circuits utilize the positive feedback approach and Barkhuasen criterion is satisfied for a single frequency only.

5.2.1 Single Phase Oscillator

Only a few OTRA based single phase oscillator circuits [61], [65] are available in literature

and a detailed study of these structures suggests that these circuits

- Use floating passive element [65]
- Do not have non interactive control on CO and FO [61], [65]
- Do not support equal component usage which is preferred from integrated circuit implementation viewpoint [65]
- Have complex CO and /or FO [61], [65]

Therefore in the following section a single phase oscillator is presented, having all the passive components virtually grounded with non interactive control on FO and CO and also supports equal component design.

5.2.1.1 Proposed Circuit

The proposed oscillator circuit is shown in Fig. 5.2. Using routine analysis the characteristic equation of the proposed oscillator can be expressed as

$$s^2C_1C_3 + s(C_1G_3 - C_2G_1) + G_1G_2 = 0 \quad \text{where } G_i = \frac{1}{R_i} \tag{5.4}$$

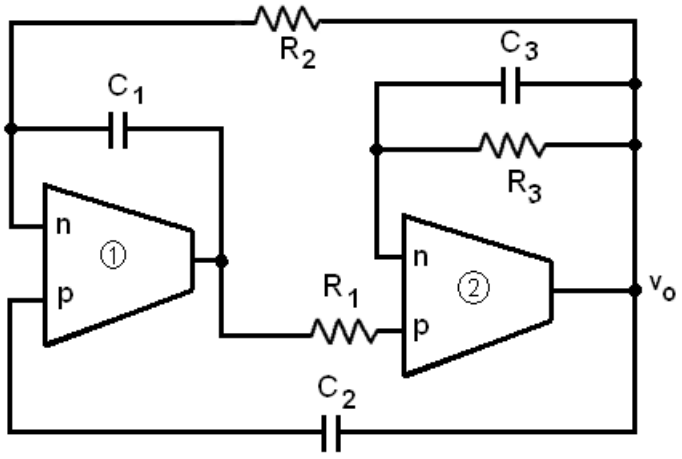


Fig. 5.2 The proposed sinusoidal oscillator.

From (5.4) the condition of oscillation (CO) and frequency of oscillation (FO) can

respectively be derived as

CO: $C_1G_3 = C_2G_1$ (5.5)

FO: $f_0 = \frac{1}{2\pi}\sqrt{\frac{G_1G_2}{C_1C_3}}$ (5.6)

It is clear that FO can be controlled independent of CO through resistance R_2; and it is also possible to achieve independent control of CO by varying C_2.

5.2.1.2 MOS-C Implementation

The proposed configuration can be made fully integrated by implementing the resistors using matched transistors operating in linear region as explained in section 2.8. The MOS-C implemented oscillator is shown in Fig. 5.3. The resistance value may be adjusted by appropriate choice of gate voltages thereby making CO and FO electronically tunable. It also exhibits the feature of orthogonal controllability of ω_0 and Q_0 through gate bias voltage.

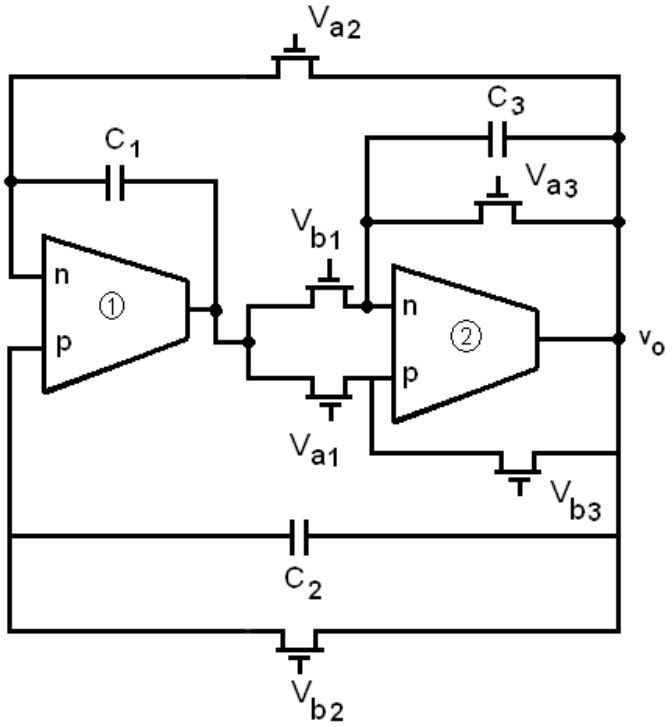


Fig. 5.3 MOS-C Implemented Oscillator.

5.2.1.3 Sensitivity Analysis

The passive sensitivities of the frequency of oscillation of the proposed oscillators may be computed as

$$S_{C_1}^{\omega_0} = S_{C_3}^{\omega_0} = S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = -\frac{1}{2} \tag{5.7}$$

All passive sensitivities are lower than unity in magnitude.

5.2.1.4 Nonideality Analysis

In analysis so far, ideal characteristics of the OTRA have been considered. However, due to the parasitics of the OTRA the behaviour of the proposed circuit may deaviate. Taking this effect into account (5.4) modifies to

$$s^2(C_1 + C_p)(C_3 + C_p) + s\big((C_1 + C_p)G_3 - C_2G_1\big) + G_1G_2 = 0 \tag{5.8}$$

Hence the modified CO and FO can be computed to be

$$(C_1 + C_p)G_3 = C_2G_1 \tag{5.9}$$

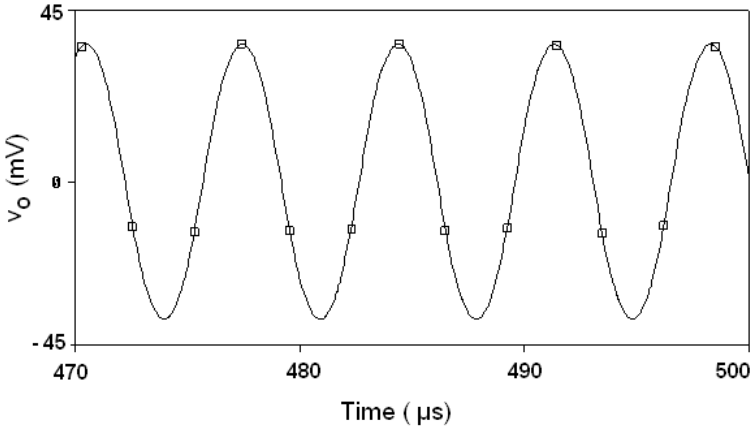
$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_1G_2}{(C_1+C_p)(C_3+C_p)}} \tag{5.10}$$

However from (5.8) it may be noted that the effect of C_p can be absorbed in C_1 and C_3 without increasing the order of the circuit and hence achieving self compensation.

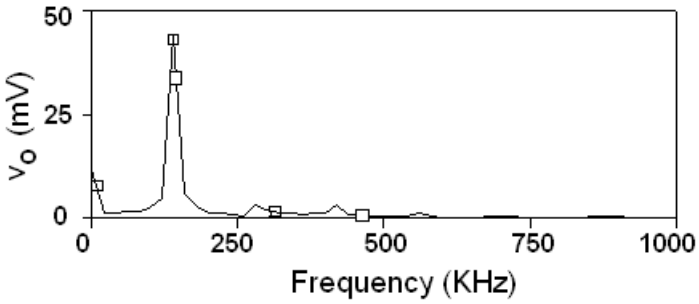
5.2.1.5 Simulation and Experimental Results

To verify the theoretical predictions, an oscillator for frequency of 159 KHz is designed and simulated through SPICE using 0.5µm, CMOS process parameters provided by MOSIS (AGILENT). The CMOS schematic of OTRA [38] as shown in Fig. 2.9 is used for simulations. The resistive component values for this design are computed as R_1 = 10 KΩ, R_2 = 50 KΩ, R_3 = 10 KΩ for chosen values of C_1 = 20 pF, C_2 = 30 pF and C_3 = 100 pF. A

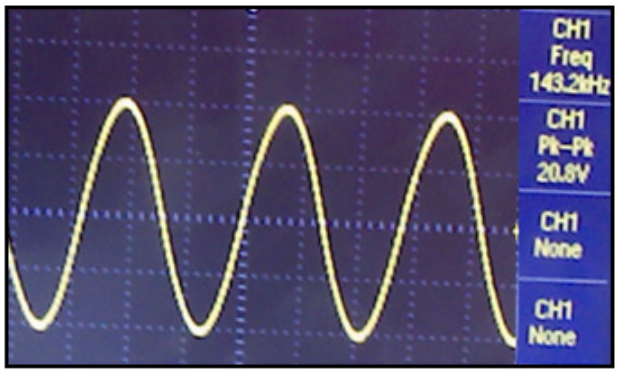
simulated output of the designed circuit is depicted in Fig. 5.4(a). The simulated output frequency is observed to be 156.82 KHz and is in close agreement with the theoretical value. The frequency spectrum of the output is shown in Fig. 5.4(b). The % THD was observed to be 4.79 %. The working of the proposed oscillator is verified experimentally as well, using



(a)



(b)



(c)

Fig. 5.4 Oscillator output. (a) Simulated result. (b) Frequency spectrum.
(c) Experimental result.

comercially available IC AD844 to implement OTRA. The component values are chosen as chosen $R_1 = R_3 = 10$ KΩ, $R_2 = 51$ KΩ, $C_1 = 22$ pF, $C_2 = 33$ pF and $C_3 = 100$ pF. The experimental output is depicted in Fig. 5.4(c) having experimental FO as 143.2 KHz. Minor variations in experimental results can be attributed to component values difference and the CFOA parasitics.

5.2.2 Quadrature Oscillator

Quadrature oscillators (QO) provide two single frequency outputs which are in quadrature phase. QOs are widely used in the field of communication, instrumentation and power electronics. In communications QO circuits are commonly used in single-sideband generators, and quadrature mixers [89]. They are also utilized for vector generators or selective voltmeters [89]. QO can be designed as either second order or third order systems. Compact realization is one of the key advantages of second order design as it uses fewer numbers of passive and/or active components whereas third order QO gives better accuracy, frequency response, and low harmonic distortion. One can trade off compact realization, for better distortion performance achieved out of third order realization, depending upon the application. Few second order QOs using OTRA [36], [51], [53], [57] are available in open literature however no third order QO design has been reported so far. Tapping this gap and keeping the advantage of third order QO in view, an OTRA based third order QO has been designed and is presented in following subsection.

5.2.2.1 Proposed Circuit

The general scheme of third order QO, as depicted in Fig. 5.5, is discussed in [90] and has been adapted for implementation with OTRA. It consists of a second order LPF having transfer function A(s) and an inverting integrator in feedback loop with transfer β(s). This forms a closed loop system having loop gain as A(s) β(s) and the criterion for oscillations to occur, is given by

$$1 - A(s)\beta(s) = 0 \tag{5.11}$$

If this criterion is satisfied the closed loop system will produce sustained oscillations. The voltages v_1 and v_2 will have quadrature phase relationship as v_2 is integrated output of v_1.

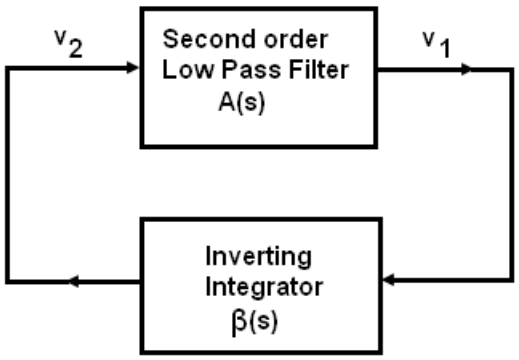


Fig. 5.5 Functional block diagram of QO [90].

The proposed third order QQ circuit is shown in Fig. 5.6. It consists of an OTRA based second order LPF [44] and an inverting integrator connected in feedback. The LPF consists of OTRA 1 and associated circuitry, whereas the OTRA 2 and passive components R_1 and C_1 form the inverting integrator.

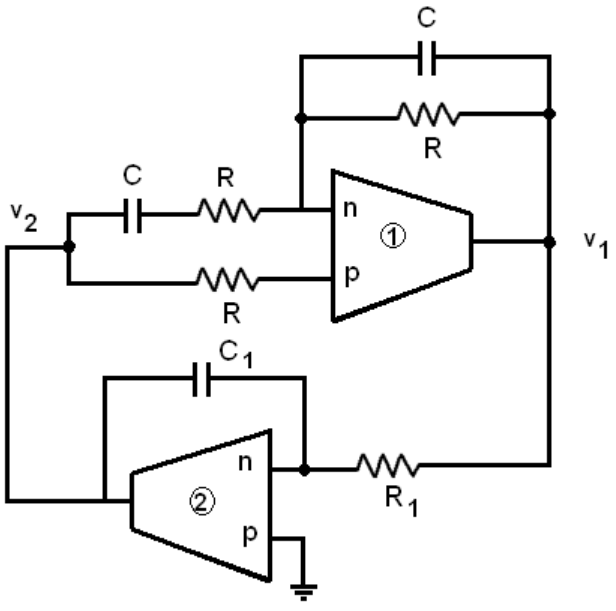


Fig. 5.6 OTRA based QO.

Using routine analysis the characteristic equation of circuit can be expressed as

$$s^3C^2C_1 + 2s^2C_1GC + sC_1G^2 + G^2G_1 = 0 \quad (5.12)$$

where $G = \frac{1}{R}$ and $G_1 = \frac{1}{R_1}$.

The CO and FO can be derived from this characteristic equation of (5.12) as

FO: $f_0 = \frac{G}{2\pi C}$ (5.13)

CO: $\frac{G}{C} = \frac{G_1}{2C_1}$ (5.14)

By suitable selection of G and C values the FO can be adjusted to desired value and proper selection of G_1 and C_1 would satisfy the CO.

5.2.2.2 MOS-C Implemented QO

The resistors connected to the input terminals of OTRA can be implemented using MOS transistors operating in non-saturation region thereby making oscillator circuit MOS-C realizable and the oscillator frequency electronically tunable. The MOS-C implementation of the proposed circuit is shown in Fig. 5.7.

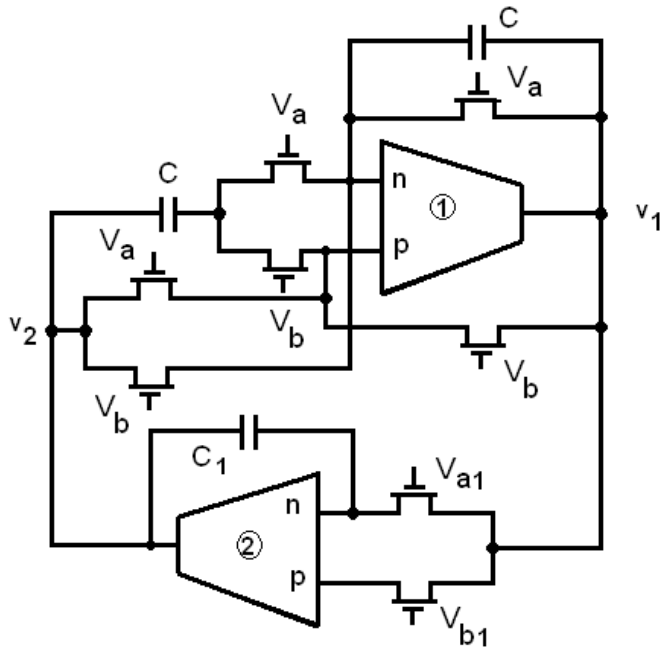


Fig. 5.7 MOS implementation of QO.

5.2.2.3 Nonideality Analysis

The output of the QO may deviate due to non-ideality of OTRA in practice. Considering the effect of nonideality of OTRA into account (5.12) modifies to

$$s^3C(C+C_p)(C_1+C_p)+s^2G(C_1+C_p)(2C+C_p)+sG^2(C_1+C_p)+G^2G_1=0 \quad (5.15)$$

From (5.15) it is found that the FO changes to

$$f_0=\frac{G}{2\pi\sqrt{C(C_p+C)}} \quad (5.16)$$

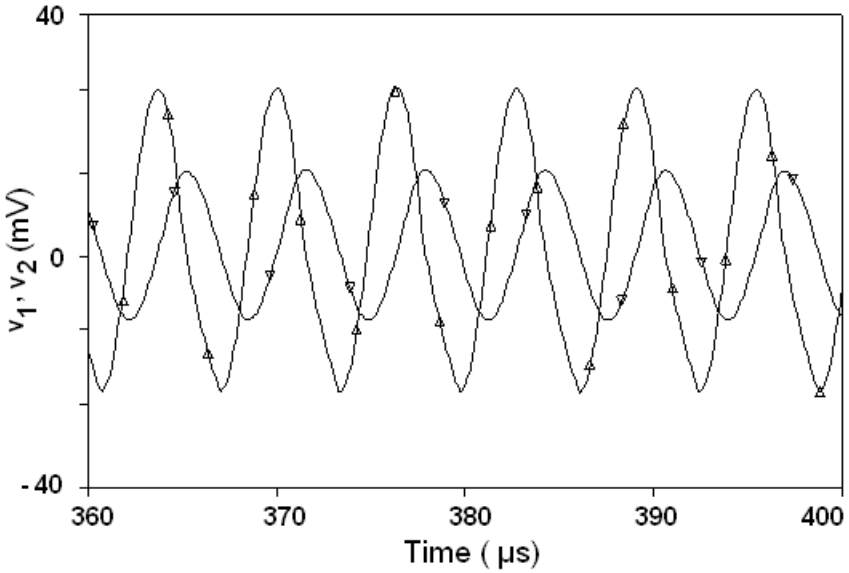
The modified CO can be expressed as

$$\frac{G}{C}=\frac{G_1(C+C_p)}{(C_p+C_1)(2C+C_p)} \quad (5.17)$$

The effect of C_p can be eliminated by pre-adjusting the value of capacitors C and C_1, which are connected in feedback path of the low pass filter and in inverting integrator respectively, thus achieving self compensation.

5.2.2.4 Simulation Results

The functionality of the proposed QO is verified through SPICE simulations using CMOS schematic of OTRA shown in Fig. 2.9 with 0.5 μm AGILENT CMOS process parameters. For all transistors used for resistance realization W/L ratio is taken as 10μm/2μm. The proposed QO is designed to work at 159 KHz by selecting the component values as C_1 = C = 100 pF, R = 10 KΩ and R_1 = 5 KΩ. The gate voltage V_b and V_{b1} are set to be 0.86 V and 0.73 V respectively while keeping V_a = V_{a1} = 1.0 V for designing R = 10KΩ, R_1 = 5KΩ. Simulated FO was observed to be 150 KHz. The resistance values designed using MOSFETs might differ slightly from the theoretically calculated values causing slight deviation between theoretical and simulated FO. The output of the QO is shown in Fig. 5.8 (a) and Fig. 5.8 (b) depicts the frequency spectrum. The % THD was observed to be 4.1%.



(a)

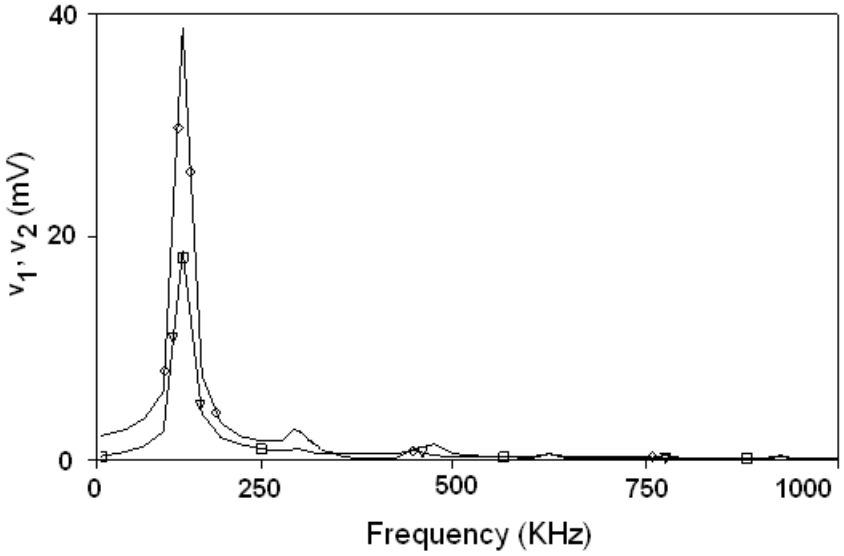


Fig. 5.8 (a) Output of proposed QO at 159 KHz.(b) Frequency spectrum.

5.2.3 Multiphase Sinusoidal Oscillator

Multiphase sinusoidal oscillators (MSO) provide n outputs equally spaced in phase and find extensive application in the field of power electronics and communications. In

communications MSO circuits are commonly used in single-sideband generators, and phase modulators. They are also utilized for control of single phase-to-three-phase PWM converters [91], and for a decoupled dynamic control of a six-phase two-motor drive system [92].

An extensive literature review revealed that OTRA based MSO circuits have not been reported earlier. Exploring this void three MSO circuits are proposed and their detailed description is presented in following section. The first circuit utilizes n OTRAs such that $n \geq 3$, to produce n odd-phase oscillations which are equally spaced in phase and are of equal amplitude. The second circuit utilizes (n+1) OTRAs having $n \geq 4$, to produce n odd or even phase oscillations equally spaced in phase. The third circuit utilizes a single-resistance-controlled (SRCO) sinusoidal oscillator circuit employing a single OTRA [65], whose output is subsequently used to drive a phase shifter network. The phase shifter circuit consists of OTRA based (n-1) noninverting LPFs giving a total of n phase oscillations. The circuit is tunable and has a low component count. An Automatic Gain Control circuitry (AGC) has also been implemented for the second and third circuit, which helps in the stabilization of the signal amplitude.

5.2.3.1 Proposed Circuit-I

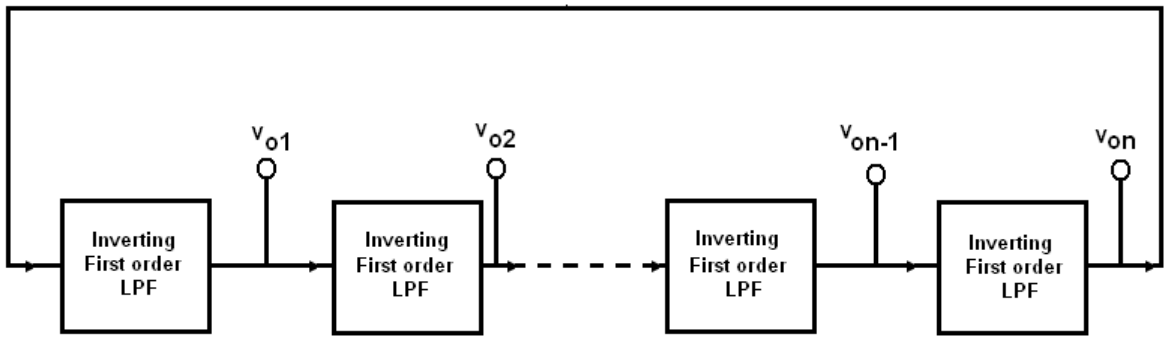
The first circuit is based on the scheme discussed in [93] and has been adapted for implementation with OTRA. It consists of n cascaded stages of first-order inverting LPFs. The output of the n th stage is fed back to the input of the first stage as shown in Fig. 5.9 (a). The OTRAs based circuit implementation of this scheme is shown in Fig. 5.9 (b). The OTRAs have been connected in the inverting mode such that the gain G(s) of each block can be expressed as

$$G(s) = \left(-\frac{K}{1+sCR}\right) \tag{5.18}$$

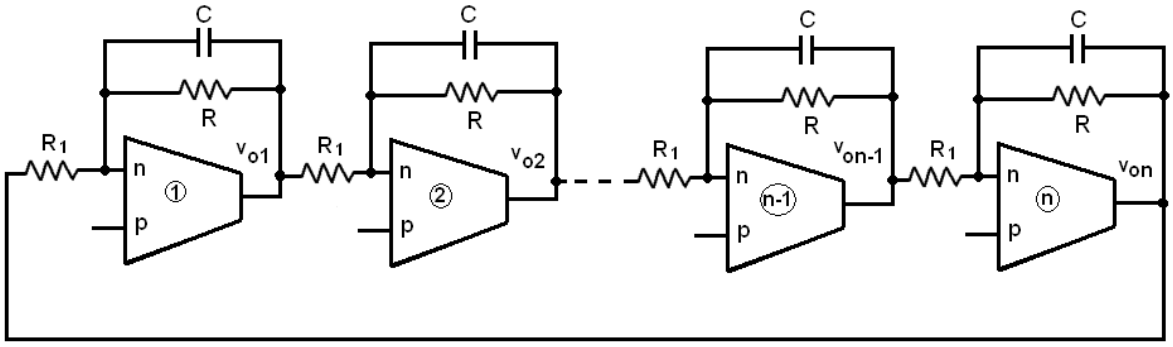
where $K = \frac{R}{R_1}$

From Fig. 5.9 (b), the open loop gain L(s) can be expressed as

$$L(s) = \left(-\frac{K}{1+sCR}\right)^n \tag{5.19}$$



(a)



(b)

Fig. 5.9 (a) Generalized scheme for producing n – odd phase oscillation.
(b) OTRA based circuit.

For oscillations to occur, the Barkhausen criterion [84] must be satisfied, hence

$$\left(-\frac{K}{1+sCR}\right)^n = 1 \tag{5.20}$$

The above equation yields

$$(1+sCR)^n + (-1)^{n+1} K^n = 0 \tag{5.21}$$

Equation (5.21) will converge only for odd values of n such that n ≥ 3. Thus the circuit will give rise to equally spaced oscillations having a phase difference of (360/n) °. Considering the case for n = 3 then (5.21) reduces to

$$(1 + j\omega_0 CR)^3 + K^3 = 0 \tag{5.22}$$

Equating real and imaginary parts of (5.22) gives the FO and CO as

FO: $f_0 = \sqrt{3}/(2\pi RC)$ (5.23)

CO: $K = 2$ (5.24)

Similarly for n=5, (5.21) would reduce to

$$(1 + j\omega_0 CR)^5 + K^5 = 0 \tag{5.25}$$

Hence FO and CO can be obtained as

FO: $f_0 = 0.727/(2\pi RC)$ (5.26)

CO: $K = 1.236$ (5.27)

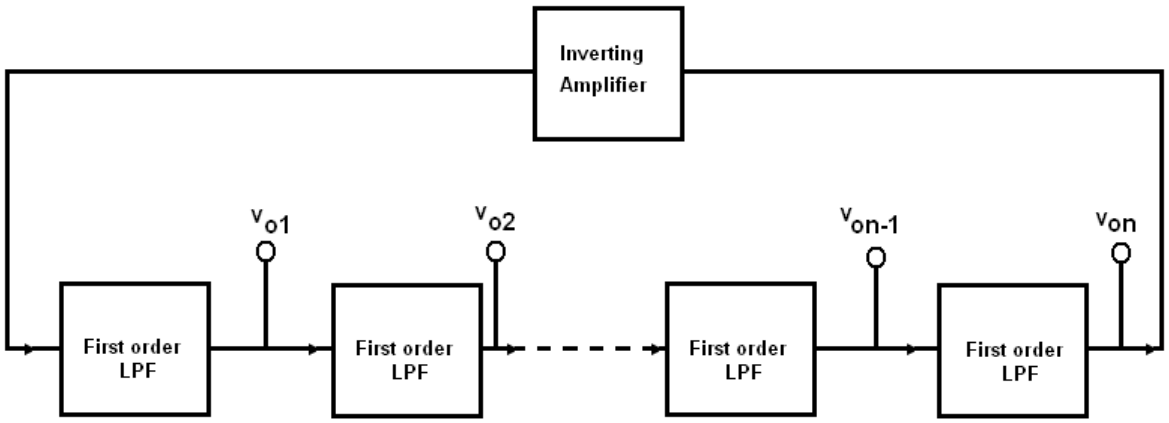
The proposed circuit is simple to realize and has a low component count. It produces n odd-phase oscillations of equal amplitudes with a phase difference of (360/n)° and an iterative control of CO and FO can be achieved for the oscillator.

5.2.3.2 Proposed Circuit-II

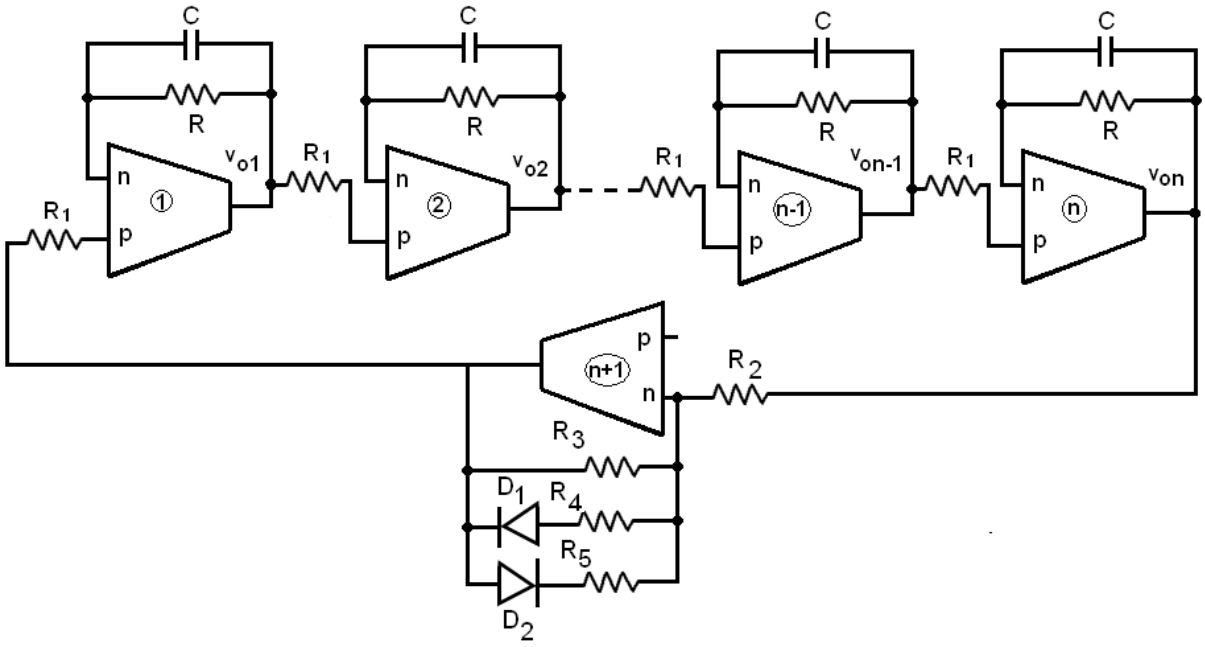
In this subsection another scheme is used which is capable of producing n odd or even phase oscillations. The block diagram of this scheme is shwon in Fig. 5.10(a) which employs n cascaded non inverting first order LPFs and an inverting voltage amplifier circuit in the feedback loop. The OTRA based implementation of this scheme is shown in Fig. 5.10(b). An inverting voltage amplifier with a simple AGC circuit is connected in the feedback loop of the oscillator. For stabilization of the signal amplitude the inverting voltage amplifier can be designed with automatic gain control circuitry (AGC). In OTRA based MSO of Fig. 5.10(b),

the diodes D_1 and D_2 along with resistors R_4, and R_5 constitute the AGC circuit. The gain G(s) of each block can be computed as

$$G(s) = \left(\frac{K}{1+sCR}\right) \tag{5.28}$$



(a)



(b)

Fig. 5.10(a) Generalized scheme for producing n – odd / even phase oscillations. (b) OTRA based circuit with AGC.

where K = (R/R_1). The loop gain for the system can be expressed as

$$L(s) = (-1)K_X \left(\frac{K}{1+sCR}\right)^n \tag{5.29}$$

$$K_X = \frac{R_3}{R_2} \tag{5.30}$$

K_X is effectively maintained at a value 1 with the help of the AGC circuitry. After applying the Barkhausen criterion the characteristic equation is obtained as

$$(1 + sCR)^n + K^n = 0 \tag{5.31}$$

The equation converges for all value of $n \geq 3$, odd or even. As an example for n = 4, (5.31) reduces to

$$(1 + j\omega_0 CR)^4 + K^4 = 0 \tag{5.32}$$

which gives FO and CO as

FO: $f_0 = 1/(2\pi RC)$ (5.33)

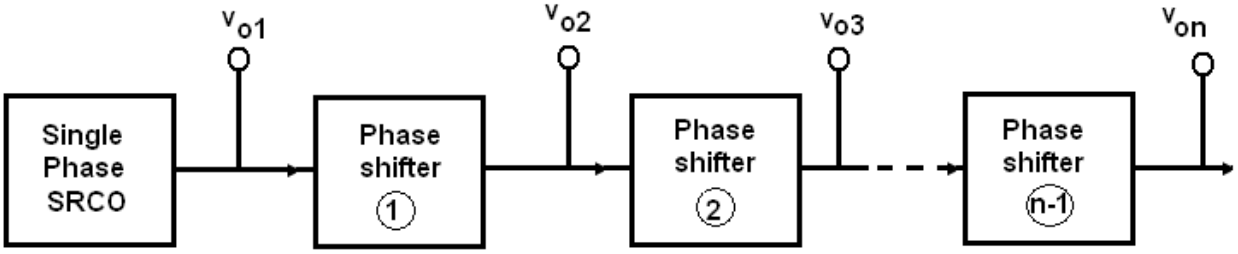
CO: $K = 1.414$ (5.34)

For n = 3, the characteristic equation, FO and CO would be same as (5.25), (5.26) and (5.27) respectively. Initially K_X is kept at a value slightly higher than 1 so that the oscillations can begin, once the amplitude crosses a certain threshold the diodes get switched on and bring down the value of resistance R_3 thus bringing down the effective value of K_X. This is possible because the input terminals of the OTRA are virtually grounded. Thus, a dynamic equilibrium maintains the value of K_X at 1. Noninteractive tuning of this circuit is not possible as CO and FO are not independent. However, the circuit is versatile and can achieve both even and odd phase oscillations. The oscillations achieved are equally spaced in phase having a phase difference of (180/n)°.

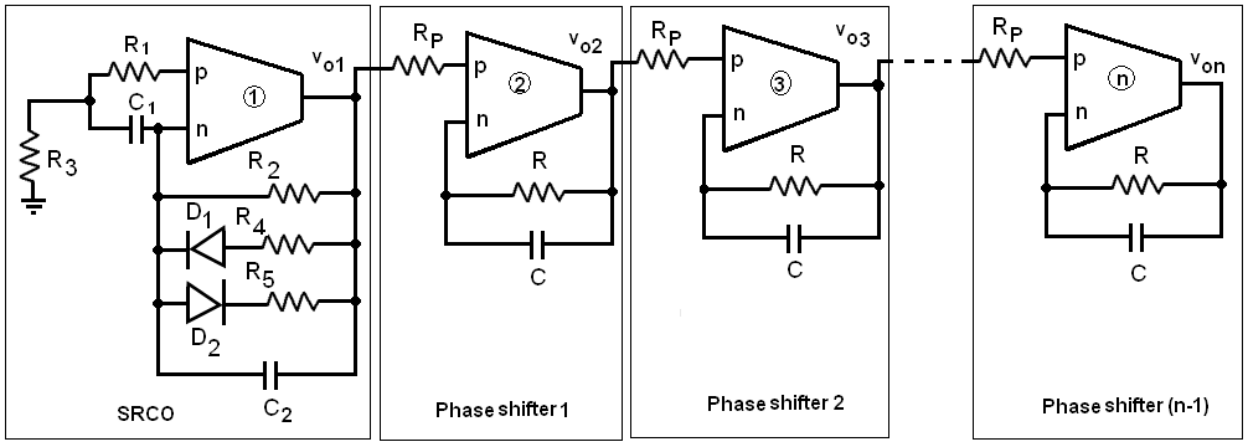
5.2.3.3 Proposed Circuit-III

The scheme of third circuit is shown in Fig. 5.11(a). It uses an SRCO followed by (n-1) phase shifter blocks thus producing n phase shifted outputs. The OTRA based configuration is shown in Fig. 5.11(b). It is based on a SRCO oscillator proposed in [65] to which an AGC circuit similar to one used in circuit II has also been added. The open loop gain of this circuit [65] is obtained as

$$L(s) = \left(\frac{sC_2R_2R_3(1-sC_1R_1)}{R_1+R_3+sR_1R_3(C_1+C_2)}\right) \tag{5.35}$$



(a)



(b)

Fig. 5.11 (a) SRCO based MSO. (b) OTRA based implementation.

Accordingly, the FO and CO for SRCO oscillator are obtained as

FO: $$f_0 = \frac{1}{2\pi}\sqrt{\frac{R_1+R_3}{C_1C_2R_1R_2R_3}} \quad (5.36)$$

CO: $$\frac{R_2}{R_1} = \frac{C_1}{C_2} + 1 \quad (5.37)$$

It can be observed that by controlling R_3 the frequency can be controlled without affecting the CO, which makes the circuit tunable. AGC has been achieved by adjusting R_2, which is used to control the loop gain, as seen from (5.35). At the output of the SRCO with AGC, (n-1) subsequent OTRA based phase shifter blocks can be connected to produce n oscillation. The phase shift produced by each phase shifter block can be given as

$$\theta = tan^{-1}(\omega_0 CR) \quad (5.38)$$

To add to the flexibility, if the OTRA in the phase shifter block is connected in inverting mode the phase shift produced will be

$$\theta = 180° - tan^{-1}(\omega_0 CR) \quad (5.39)$$

Hence, the phase shifter can be adjusted to obtain a phase shift of either 0°-90° or 90°-180° depending on its configuration. This circuit provides the flexibility of achieving the desired phase shift without connecting too many active elements.

5.2.3.4 Nonideality Analysis

The output of the proposed circuits may deviate from the theoretical predictions due to nonidealities associated with CFOAs used for realizing OTRA. In this section the nonideality analysis for Circuit II which provides both even and odd phase outputs, is presented. Considering the nonideal model of CFOA as shown in Fig. 2.8, the non inverting OTRA based LPF block can be redrawn as shown in Fig. 5.12. KCL at nodes 1 and 2 can respectively be written as

$$\frac{(v_{in}-v_1)}{R_1} = \frac{v_1}{R_{x1}} \tag{5.40}$$

$$\frac{(v_o-v_2)}{R_1} + (v_o-v_2)sC = \frac{v_2}{R_{z1} \| R_{x2}} \tag{5.41}$$

Assuming $R_{x1} = R_{x2} = R_x$ and using the relation $R_x << R_{z1}$, from (5.40) and (5.41) the transfer function of non inverting LPF can be expressed as

$$\frac{v_o}{v_{in}} = \frac{K\,(1+sCR_x)}{(1+sCR)} \tag{5.42}$$

Using (5.42) the loop gain given by (5.29) modifies and can be represented as

$$L(s)|_n = (-1)K_X\left(\frac{K(1+sCR_x)}{1+sCR}\right)^n \tag{5.43}$$

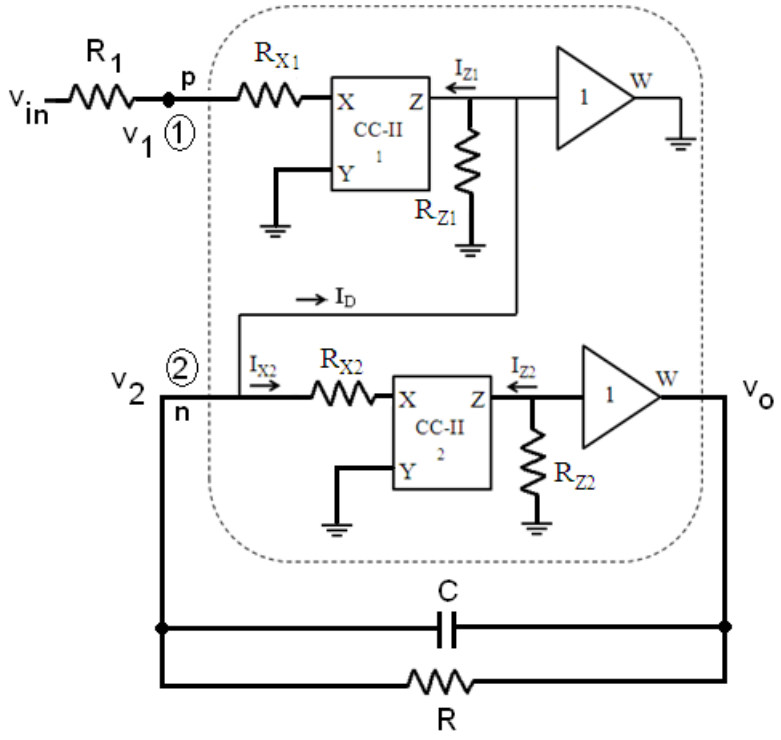


Fig. 5.12 Nonideal model of the non inverting LPF.

Assuming K_x =1, the modified characteristic equation can be written as

$$(1 + sCR)^n + K^n(1 + sCR_x)^n = 0 \quad (5.44)$$

For n = 3 the CO and FO for the circuit can be deteremined as

$$\text{FO:} \quad f_0 = \frac{\sqrt{3}\,(R+R_xK^3)}{2\pi\sqrt{(R^3+K^3{R_x}^3)\,C}} \quad (5.45)$$

$$\text{CO:} \quad (K^3+1) = 9\frac{(R+R_xK^3)(R^2+K^3{R_x}^2)}{(R^3+K^3{R_x}^3)} \quad (5.46)$$

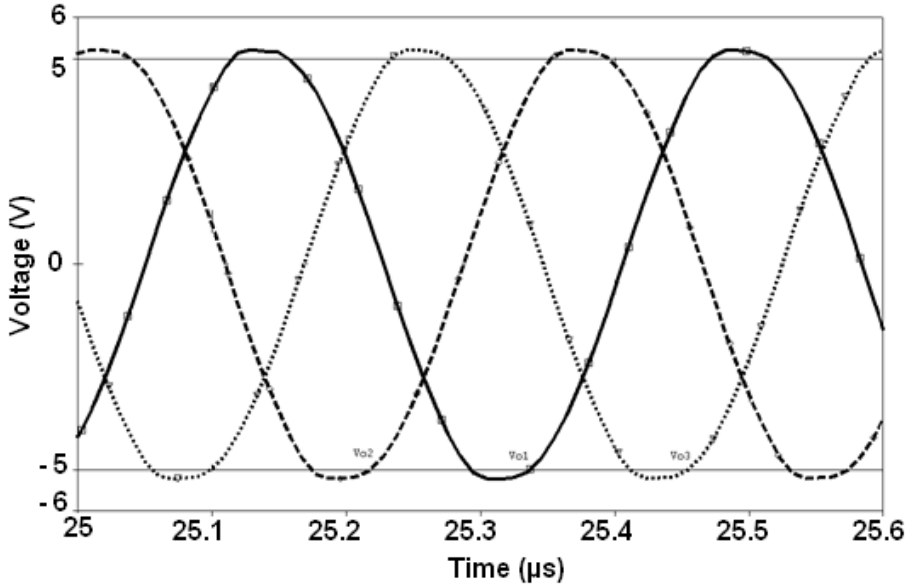
Since R_X << R then (5.45) and (5.46) respectively reduce to (5.23) and (5.24).Thus the deviation from ideal behavior caused due to practical model can be kept small if the external resistors are chosen to be much larger than R_x .

The nonideality analysis for Circuit I and Circuit III can be worked out in a similar manner.

5.2.3.5 Simulation and Experimental Results

The proposed circuits have been simulated using SPICE to validate the theoretical predictions, employing OTRA realization of Fig. 2.7. Simulation results of circuit I having n = 3 and component values R_1 = 0.5 KΩ, R = 1 KΩ and C = 100 pF are shown in Fig. 5.13(a). The simulated frequency of oscillation was 2.838 MHz against the calculated value of 2.757 MHz having frequency error of 2.93%. The simulated and theoretical frequency of oscillation as a function of capacitance (C) is depicted in Fig. 5.13 (b). It shows that the simulated values are in close agreement with the ideal values.

Figure 5.14 (a) shows the simulation results of circuit II having n = 4 and component values R_1 = 0.707 KΩ, R = 1 KΩ and C = 100 pF. The simulated value achieved was 1.595 MHz against the theoretical value of 1.591 MHz with a frequency error of 0.25%. The simulated and theoretical frequencies of oscillation as a function of capacitance (C) are shown in Fig. 5.14(b) and both the curves are in close agreement.



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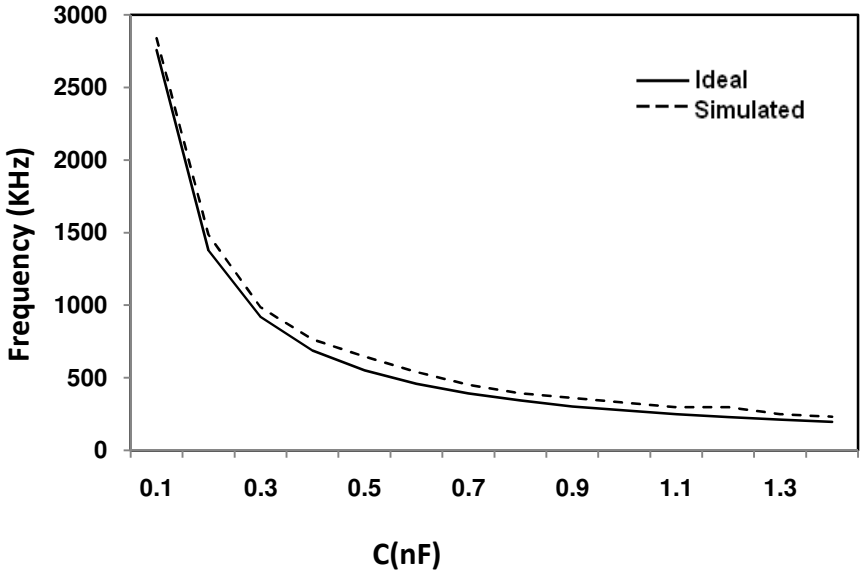
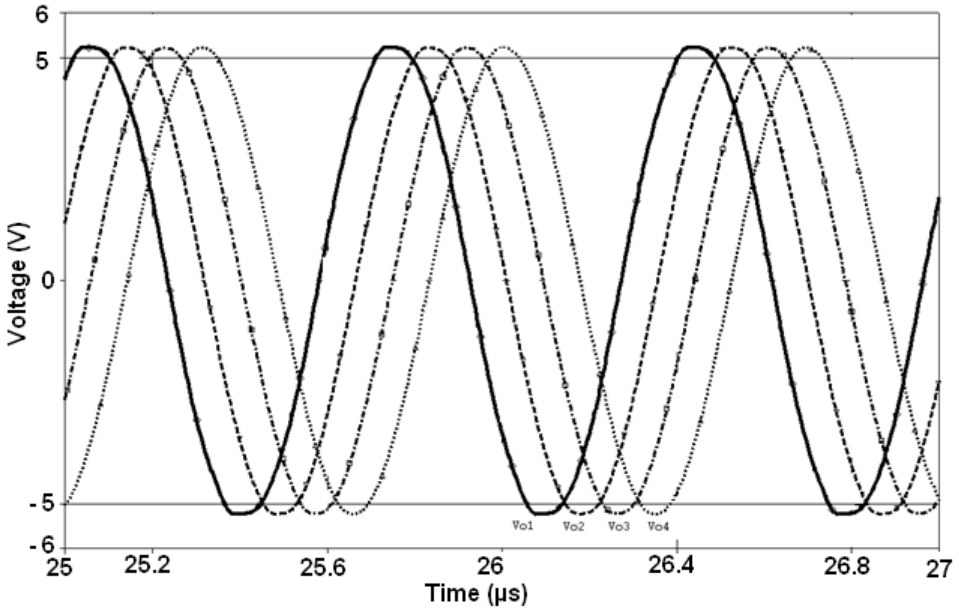


(b)

Fig. 5.13 Simulation result for circuit I. (a) Output waveform for n = 3.

(b) Frequency error curve.



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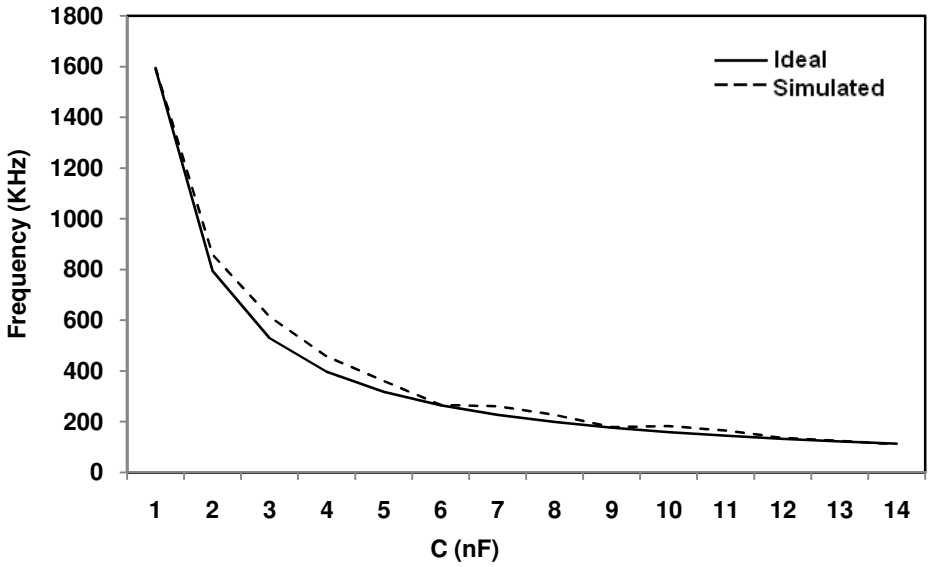
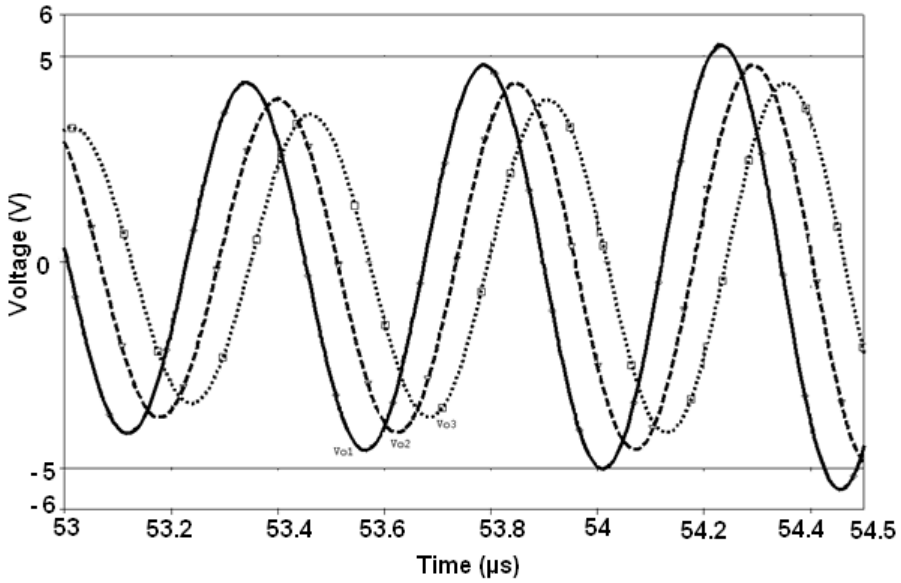


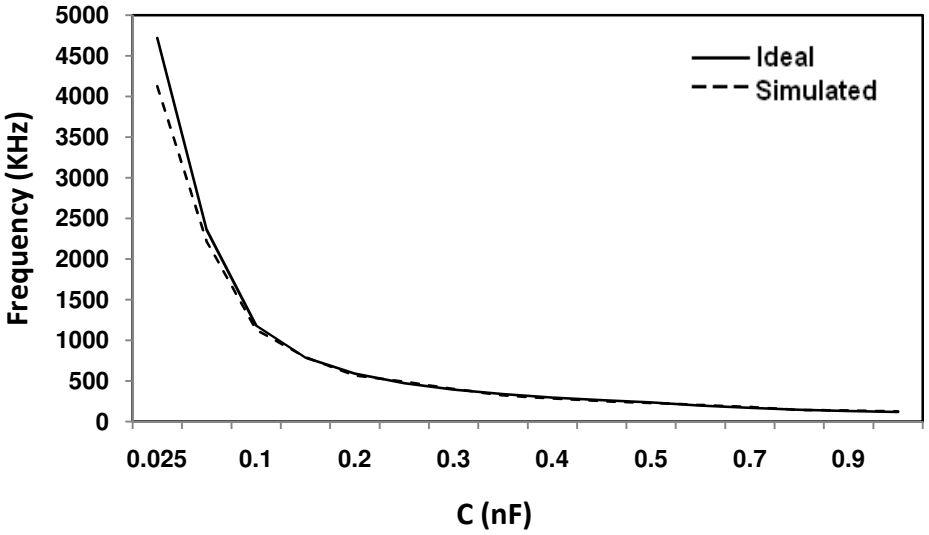
(b)

Fig. 5.14 Simulation results for circuit II. (a) Output waveforms for n = 4. (b) Frequency error curve.

The simulation results of circuit III having two phase shifter blocks along with the SRCO are depicted in Fig. 5.15(a). The design is obtained for an FO of 2.361 MHz with a phase shift of 45^0. The component values chosen are $R_1 = R_3 = R_4 = R_5 = R_P = 1$ KΩ, $R_2 = 2$ KΩ, R = 1.434 KΩ and $C_1 = C_2 = C = 50$ pF.



(a)

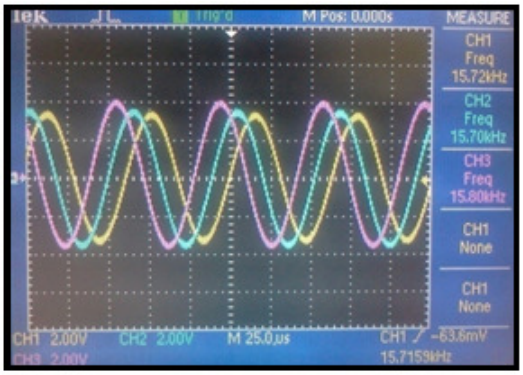


(b)

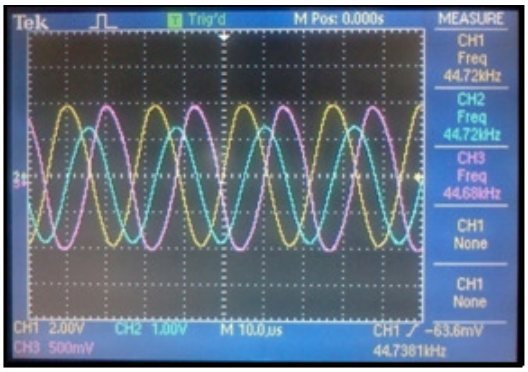
Fig. 5.15 Simulation results for circuit III (a) Output waveforms having two phase shifter networks of 45° each. (b) Frequency error curve.

The observed FO was 2.220 MHz against the calculated value of 2.361 MHz. The simulated and theoretical frequencies of oscillation as a function of capacitance are shown in Fig. 5.15 (b).

The functionality of the proposed MSO circuits is verified through hardware also. The commercial IC AD844AN is used to implement an OTRA as discussed in section 2.8. Supply voltages used are ± 5 V. Figure 5.16(a) shows the experimental results for circuit II, having, n = 3 for component values R_1 = 2.7 KΩ, R = 5.4 KΩ, $R_3 = R_4 = R_5$ = 1 KΩ and C = 3.3 nF. Observed FO is around 15.7 KHz and is in close agreement to calculated FO of 15.469 KHz. The output of circuit III consisting of SRCO along with two phase shifter blocks is depicted in Fig. 5.16 (b) for component values $R_1 = R_P$ = 2.7 KΩ, R_2 = 5.4 KΩ, $R_4 = R_5$ = 1 KΩ, R_3 = 250 Ω, R = 10 KΩ and $C = C_1 = C_2$ = 3.3 nF. These component values result in theoretical FO as 43.4 KHz and the observed frequency is around 44.72 KHz. The slight variation in experimental values of FO, from phase to phase, as seen in Fig. 5.16 may be due to tolerance of the component values.



(a)



(b)

Fig. 5.16 (a) Experimental result for circuit II for n = 3, (b) Experimental result for circuit III with two phase shifter blocks.

5.3 CONCLUDING REMARKS

In this chapter OTRA based VM single, quadrature and multiphase sinusoidal oscillator configurations are presented. The proposed single and quadrature phase structures provide

non interactive control on FO and CO both and are made electronically tunable through MOS implemented resistors. Design description of three MSO circuits follows this sequence. The MSO circuit-I provides only odd phase oscillations whereas the remaining two structures provide both even and odd phase oscillations. These circuits are very accurate in producing a wide range of oscillation frequency with the desired phase shift. Hence, they are capable of replacing voltage mode op-amps based MSO as they are free from the limitations of conventional voltage mode op-amps.

SPICE simulations, are included to demonstrate the workability of all proposed oscillators. Experimental results for MSO circuits have also been included. The effect of non ideal behavior of OTRA in practice has been analyzed for all proposed structures.

CHAPTER – 6
INSTRUMENTATION AND CONTROL APPLICATIONS OF OTRA

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, "**Electronically Tunable Transimpedance Instrumentation Amplifier based on OTRA**," Journal of Engineering, Volume 2013, Article ID 648540, 5 pages, doi.org/10.1155/2013/648540.

2. Rajeshwari Pandey, Saurabh Chitransi, Neeta Pandey, Chandra Shekhar. **"Single OTRA based PD Controllers,"** International Journal of Engineering Science and Technology, vol. 4 no.4, pp.1426-1437, 2012.

6.1 INTRODUCTION

Electronic instrumentation serves to amplify, shape and convert an analog signal into a form suitable for measurement, recording and/ or for further processing [94]. In instrumentation system quite often the analog signal is derived from a transducer which converts the physical quantity to be measured into an electrical signal either voltage or current [94]. In some cases this processed signal can be used as a part of automatic feedback control system to control the system parameters and thus improving system performance.

This chapter deals with the instrumentation and control applications of OTRA and describes the design of an OTRA based transimpedance instrumentation amplifier (TIA) followed by classical analog controllers namely proportional (P), proportional-derivative (PD), proportional integral (PI) and proportional derivative and integral (PID). A brief review of ava33ilable work on TIA and analog controllers has also been included.

6.2 INSTRUMENTATION AMPLIFIER

Instrumentation amplifier (IA) is an essential part of electronic instrumentation system which faithfully amplifies low level differential output of the transducer in the presence of high common mode noise. The gain of an amplifier is defined as ratio of output and input parameters. The choice between voltage and current as two possible input and output signals leads to four type of amplifiers namely the voltage controlled voltage source (VCVS) or voltage amplifier, the current controlled current source (CCCS) or current amplifier, the voltage controlled current source (VCCS) or transadmittance amplifier, the current controlled voltage source (CCVS) or transimpedance amplifier. VCVS and VCCS are suitable for amplification of signals from voltage-source transducers whereas for amplification of signals from current-source transducers CCCS and CCVS would be a better choice wherein the current input can be directly processed without conversion to voltage signal.

A review of earlier work suggests that a number of IAs have been proposed in literature [95] – [99], which are suitable for amplification of signals from voltage-source transducers and produce voltage output. The conventional operational amplifier based IA [95], [96] aren't capable of operating at higher frequencies because of slew rate and fixed

gain-bandwidth-product limitations [3]. The configurations proposed in [97] – [99] use the second-generation current conveyor (CCII). An op-amp based TIA is presented in [100] and is designed, for a specific low frequency application in a gamma-ray dosimeter. It consists of two current to voltage converters followed by an amplifier and uses three opamps and nine resistors. An extensive literature review reveals that no OTRA based IA has been proposed in open literature.

6.3 PROPOSED TRANSIMPEDANCE INSTRUMENTATION AMPLIFIER

OTRA is the most suitable analog building block for transimpedance type signal processing due to its very nature of current input and voltage output. The proposed OTRA based TIA circuit is shown in Fig. 6.1. It consists of two input buffers and a subtractor designed using three OTRAs and five resistors.

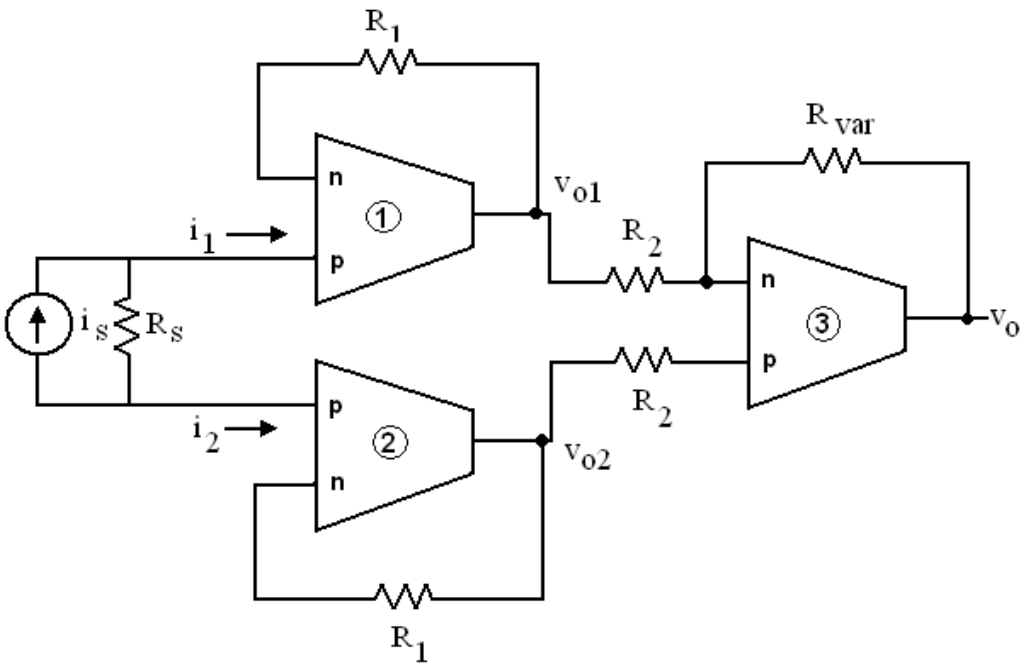


Fig. 6.1 The proposed TIA

The differential current signal from the current source/transducer is represented as i_s and can be written as

$$i_s = (i_1 - i_2) \tag{6.1}$$

The voltages v_{o1} and v_{o2} in Fig. 6.1 can be expressed as

$$v_{o1} = i_1 R_1 \tag{6.2}$$

$$v_{o2} = i_2 R_1 \tag{6.3}$$

The differential transimpedance gain (A_d) for the amplifier can be computed as

$$A_d = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2} \tag{6.4}$$

It can be seen from (6.4) that A_d can be adjusted by varying resistance R_{var}.

6.3.1 Nonideality Analysis

Taking into account the nonideality of OTRA as explained in section 2.8, the output voltages at different nodes of TIA can be expressed as

$$V_{o1}\big|_n = \frac{i_1 R_1}{1 + sC_{P1}R_1} \tag{6.5}$$

$$V_{o2}\big|_n = \frac{i_2 R_1}{1 + sC_{P2}R_1} \tag{6.6}$$

$$V_o\big|_n = \frac{-R_1 R_{var}}{R_2(1 + sC_{P3}R_{var})}\left(\frac{i_1}{(1 + sC_{P1}R_1)} - \frac{i_2}{(1 + sC_{P2}R_1)}\right) \tag{6.7}$$

where C_{pi} is the parasitic capacitance of i^{th} OTRA. Considering $C_{p1} = C_{p2} = C_{p3} = C_p$, the A_d given by (6.4) modifies to

$$A_d\big|_n = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2}\, \varepsilon_{uc}(s) \tag{6.8}$$

Where

$$\varepsilon_{uc}(s) = \frac{1}{(1 + sC_P R_1)(1 + sC_P R_{var})} \tag{6.9}$$

is uncompensated error function.

It is to be noticed from (6.8) that the gain A_d can be adjusted by R_{var} R_1/ R_2 and the bandwidth (BW) is controlled by $\varepsilon_{uc}(s)$. Thus the gain of the amplifier remains same as ideal one and can be adjusted by varying R_{var} without affecting the BW as C_p is a small value. From (6.7) by using $i_1 = i_2 = i_c$, the transimpedance common mode gain (A_c) can be computed as

$$A_c = \frac{v_0}{i_c} = \frac{-R_1 R_{var}}{R_2(1+sC_{P3}R_{var})}\left(\frac{1}{(1+sC_{P1}R_1)} - \frac{1}{(1+sC_{P2}R_1)}\right) \tag{6.10}$$

For perfectly symmetric circuits having $C_{p1} = C_{p2} = C_{p3} = C_p$, the output common mode voltage will be zero. This property of common mode voltage cancellation is known as common-mode rejection. The extent to which a common mode signal is rejected by an IA is measured by the performance parameter common mode rejection ratio (CMRR) defined as the ratio of differential gain to common mode gain. For the proposed TIA CMRR can be computed as

$$CMRR = \frac{A_d}{A_c} = \frac{2+s(C_{p1}+C_{p2})R_1}{s(C_{P2}-C_{p1})R_1} \tag{6.11}$$

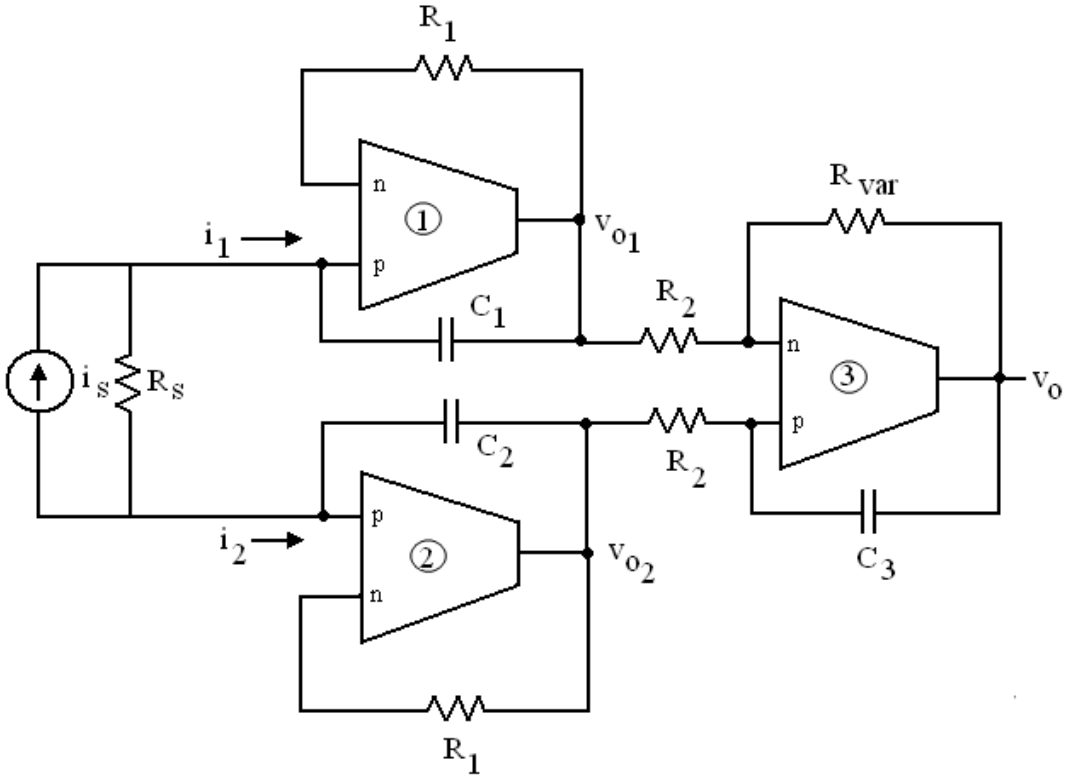


Fig. 6.2 TIA with high frequency compensation.

For high-frequency applications, compensation methods must be employed to account for the error $\varepsilon_{uc}(s)$ introduced in (6.4) and given by (6.9). High frequency passive compensated topology of the TIA is shown in Fig. 6.2. Routine analysis of Fig. 6.2 results in

$$A_d = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2}\, \varepsilon_c(s) \tag{6.12}$$

where $\varepsilon_c(s)$ is compensated error function and is given by

$$\varepsilon_c(s) = \frac{1}{(1+R_1 s(C_P - C_1))(1+R_{var} s(C_P - C_3))} \tag{6.13}$$

By taking $C_1 = C_2 = C_3 = C_p$, $\varepsilon_c(s)$ reduces to 1, which makes (6.12) same as (6.4). The effect of single pole model of R_m can thus be eliminated.

6.3.2 MOS – C Realization

Using the method of active implementation of passive resistors as explained in section 2.8, the proposed configuration is made fully integrated. The MOS based implementation of the proposed TIA is shown in Fig. 6.3 wherein R_1, R_2 and R_{var} are

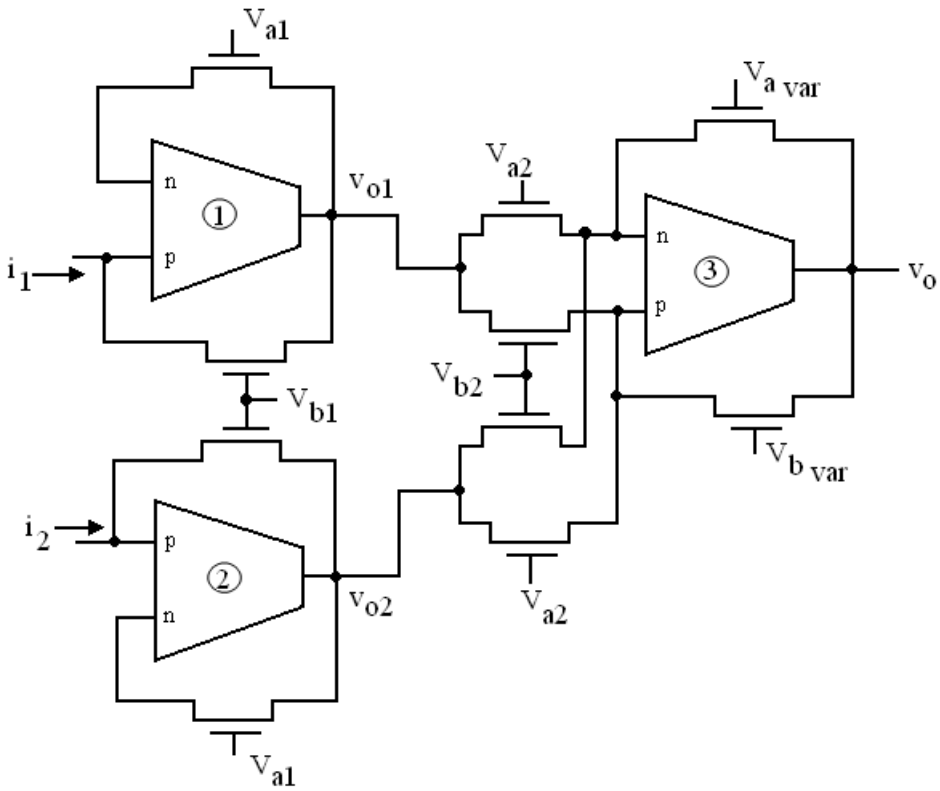
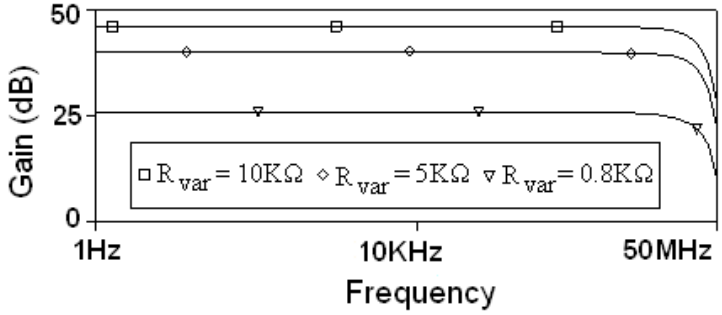


Fig. 6.3 MOS based implementation of the proposed TIA.

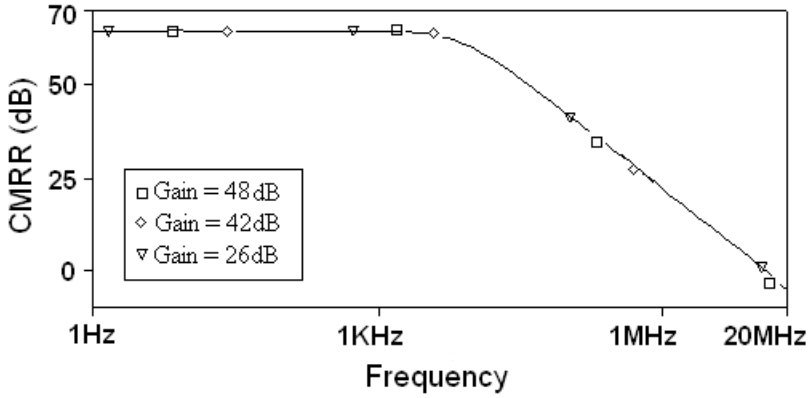
implemented using MOS transistors operating in linear region. The resistance value may be adjusted by appropriate choice of gate voltages. This not only makes the circuit suitable for integration but also makes the TIA gain electronically tunable.

6.3.3 Simulation and Experimental Results

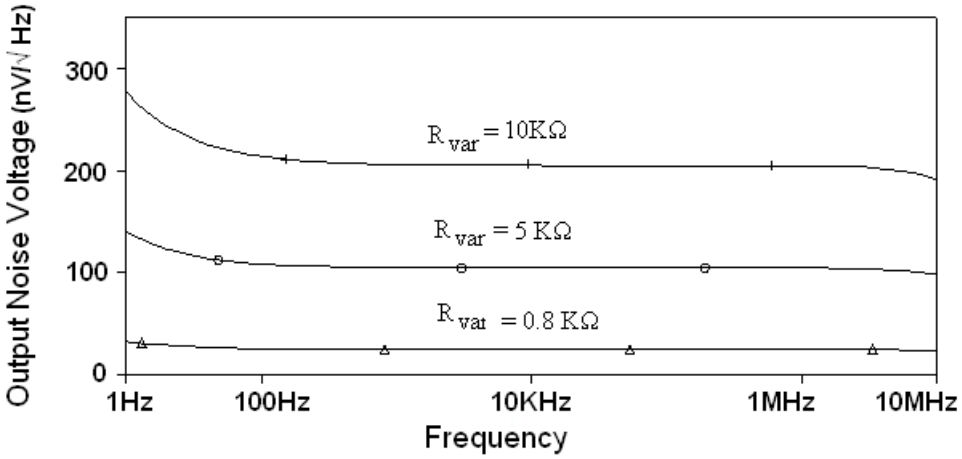
The performance of the proposed TIA is verified through SPICE simulation using CMOS implementation of the OTRA discussed in section 2.5. The frequency response of the proposed amplifier is shown in Fig. 6.4 (a). The input differential current was chosen as 5 mA. The component values are taken as $R_1 = 5$ KΩ and $R_2 = 1$ KΩ. The R_{var} is assigned values as 0.8 KΩ, 5 KΩ and 10 KΩ for which the differential gains obtained were 26 dB, 42 dB and 48 dB respectively. The 3 dB frequency of the amplifier is 10 MHz for all the three cases confirming that the bandwidth of the amplifier is independent of gain. Total power consumption of the proposed TIA is simulated to be 4.93 mW. Figure 6.4 (b) shows the CMRR responses of the circuit for differential gains of 26 dB, 42 dB, and 48 dB. It is observed that the proposed TIA exhibits a CMRR magnitude of 64.5 dB and bandwidth of 10 KHz, which is independent of gain. The simulation results of the noise performance analysis of the proposed TIA for different values of R_{var} are depicted in Fig. 6.4 (c). It may be noticed from the Fig. 6.4 (c) that the noise level being low would result in high signal-to-noise ratio of the TIA. A hardware prototype of the proposed TIA is also designed to test its functionality experimentally. The OTRA is realized using commercial IC AD 844AN as explained in section 2.4.1. Supply voltages used are ± 5 V. The experimental and simulated frequency response for the TIA, for R_1 = 5 KΩ, $R_2 = 1$ KΩ and R_{var} = 10 KΩ, are shown in Fig. 6.5(a) and CMRR response is shown in Fig. 6.5 (b). The slight variations in experimental and simulated results may be attributed to component tolerances. Observed outputs showing the performance of the proposed TIA at 70 KHz and 2 MHz for $R_1 = 5$ KΩ, $R_2 = 1$ KΩ and R_{var} = 10 KΩ are given in Fig. 6.5(c) and (d) respectively.



(a)



(b)



(c)

Fig. 6.4 Simulation results of the proposed TIA. (a) Frequency response. (b) CMRR response. (c) Output noise spectral density.

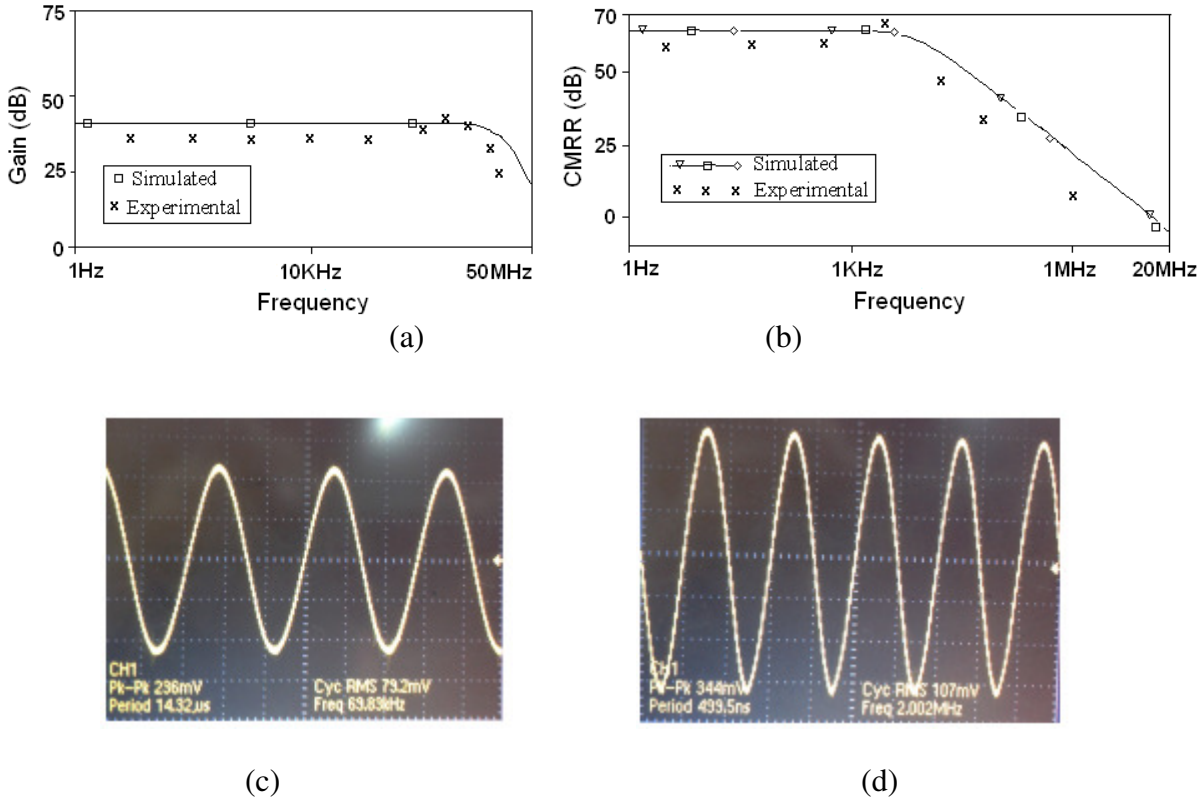


Fig. 6.5 Experimental results of the proposed TIA.(a) Frequency Response for R_{var}=10 Ω. (b) CMRR Response. (c) Output for 70 KHz input. (d) Output for 2 MHz input.

6.4 CONTROLLERS

A controller monitors and modifies the operational conditions of a given dynamical system. These operational conditions are referred to as measured output variables and can be modified by adjusting certain input variables. The controller calculates the difference between a measured output variable and a desired set point as an error value and attempts to minimize the error by adjusting the process control inputs. In general, controllers can be classified as (i) conventional (ii) non conventional controllers. For conventional controllers apriori knowledge of the mathematical model of the process to be controlled is required in order to design a controller whereas for unconventional controllers this information is generally not required. Proportional (P), proportional-derivative (PD), proportional-integrator (PI) and proportional derivative and integral (PID) controllers, are few typical examples of conventional controllers and neuro, fuzzy controllers are representatives of the unconventional class. The controllers based on proportional-

integral-derivative (PID) algorithm are most popularly used in the process industries. These are used to control various processes satisfactorily with proper tuning of controller parameters. In a PID controller as shown in Fig. 6.6 the proportional, integral and the derivative of the error signal E(s) are summed up to calculate the output actuating signal U(s) of the controller.

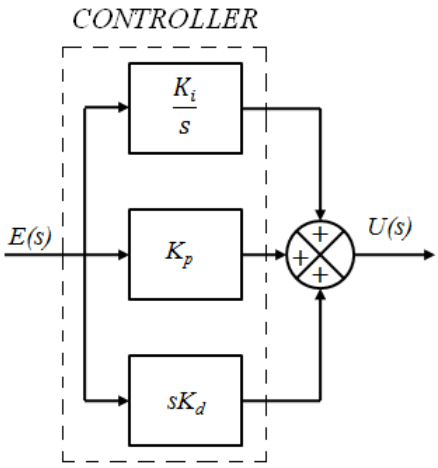


Fig. 6.6 PID controller.

Thus the transfer function $G_{PID}(s)$ of the PID controller can be written as

$$G_{PID}(s) = \frac{U(s)}{E(s)} = K_p + \frac{K_i}{s} + K_d\, s \tag{6.14}$$

where K_p, K_i and K_d are the proportional, integral and derivative constants, respectively. A second order unity feedback control system using PID controller is shown in Fig. 6.7. If in Fig. 6.6 only proportional action is considered, then it becomes a proportional controller where actuating signal depends on the instantaneous value of the control error.

The transfer function of proportional controller can be represented as

$$G_P(s) = \frac{U(s)}{E(s)} = K_p \tag{6.15}$$

The closed loop transfer function of the control system with P controller can be expressed as

$$T_P(s) = \frac{K_p\omega_n^2}{s^2+2\xi\omega_n s+K_p\omega_n^2} \tag{6.16}$$

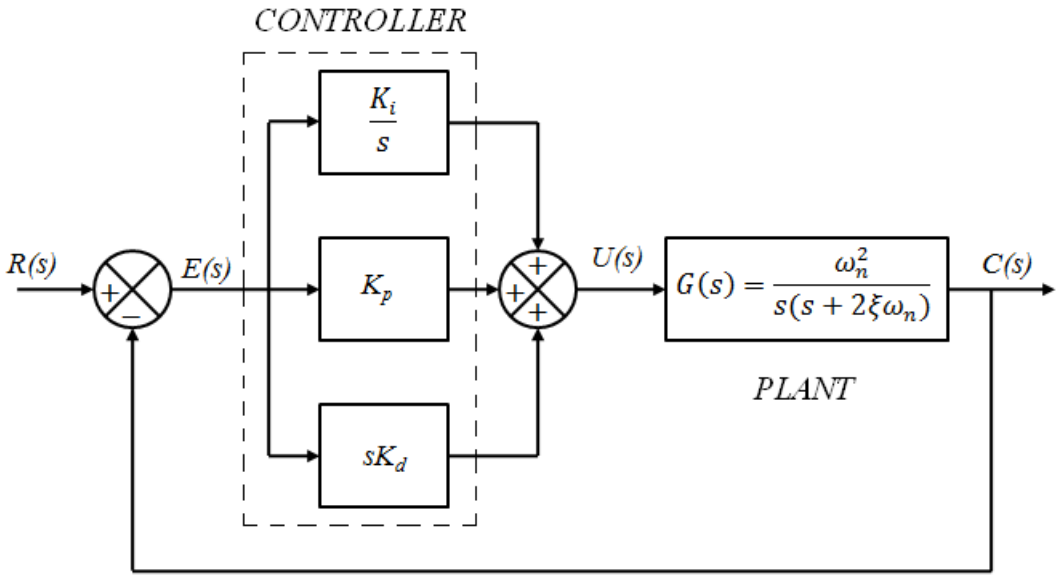


Fig. 6.7 Block diagram of a control system with PID controller.

The standard characteristic polynomial, D(s), of second order system [101] is given by

$$D(s) = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{6.17}$$

where ω_n is natural frequency of oscillations and ξ represents the damping factor. On comparing the denominator of (6.16) with (6.17) it is observed that by using P controller in feedback, natural frequency increases and damping ratio decreases by a factor $\sqrt{K_p}$, which results in reduction of peak time, rise time and steady state error. However, the maximum peak overshoot increases for P controller.

From the controller block of Fig. 6.6 if only proportional and integral actions are considered into account the resulting controller is known as PI controller. The transfer function $G_{PI}(s)$, of the PI controller so obtained can be given by

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{6.18}$$

and the transfer function of the closed loop system can be computed as

$$T_{PI}(s) = \frac{(K_i + sK_p)\omega_n^2}{s^3 + 2\xi\omega_n s^2 + (K_i + sK_p)\omega_n^2} \tag{6.19}$$

PI controller increases the order of the system. It improves steady state response by reducing the steady state error however it has a negative effect on speed of the response and overall stability of the system.

A PD controller can be derived from the generalized controller block of Fig. 6.6 if proportional and derivative actions only are taken into consideration thus the actuating signal U(s) is sum of proportional to the error signal E(s) and its rate of change. Transfer function of a PD Controller $G_{PD}(s)$, can be expressed as

$$G_{PD}(s) = K_p + K_d\, s \tag{6.20}$$

The transfer function of second order unity feedback control system using PD controller can be computed to be

$$T_{PD}(s) = \frac{(K_p+sK_d)\omega_n^2}{s^2+(2\xi\omega_n+K_d\omega_n^2)s+K_p\omega_n^2} \tag{6.21}$$

Considering $K_p = 1$, and comparing denominator of (6.21) with (6.17), it can be noticed that natural frequency, does not change while damping ratio increases. This results in reduction of the peak overshoot, rise time, peak time and settling time; however it does not affect the steady state error.

From the discussion so far it can be concluded that in a given system the proportional action improves the rise time of the system, the integral action improves the steady-state error whereas the derivative action improves the degree of stability. So, none alone is capable of achieving the complete improvement in system performance [101]. This leads to the motivation of using a PID controller so that the system performance can be optimized.

Classical analog controllers [102] − [104] are generally designed using operational amplifiers. However the op-amp based circuits, being voltage mode, have their own limitations of constant gain bandwidth product and low slew rate. It is well known that inherent wide bandwidth which is almost independent of closed loop gain, greater linearity, and large dynamic range; are the key performance features of current mode technique [3]. Therefore the current mode building blocks would be good alternative of op-amp for designing the analog controllers. Literature survey on PID controllers reveals that number of current mode building blocks such as OTA [105], CDBA [106] and

CCII [107] – [109] have been used to implement analog controllers. However no OTRA based controllers are available in open literature.

6.5 PROPOSED CONTROLLER CIRCUITS

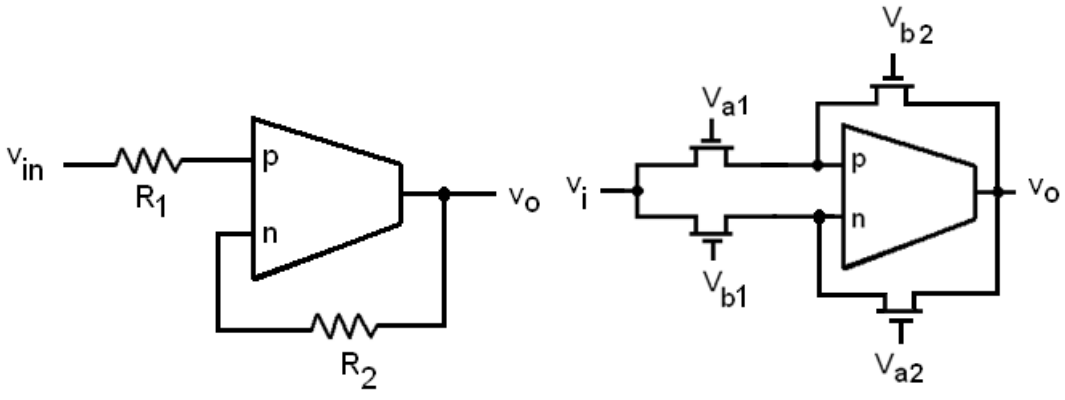
In this section, OTRA based realization of the classical controllers discussed in section 6.4, namely P, PI, PD and PID has been proposed. The proposed circuits can be made fully integrated by implementing the resistors using MOS transistors operating in non-saturation region. This also facilitates electronic tuning of the controller parameters. Finally influence of controllers on performance of a second order system is also evaluated.

6.5.1 P Controller

The proposed P controller is shown in the Fig. 6.8(a). The circuit is basically a voltage controlled voltage source [36] and its transfer function can be expressed as

$$G_P(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_2}{R_1} \tag{6.22}$$

Equation (6.22) represents the controller parameter K_p which can be tuned by changing either R_1 or R_2, or both. Electronic tuning of K_p can be achieved by implementing the resistors R_1 and R_2 using MOS transistors operating in non-saturation region, and then controlling their gate bias as shown in Fig. 6.8(b).



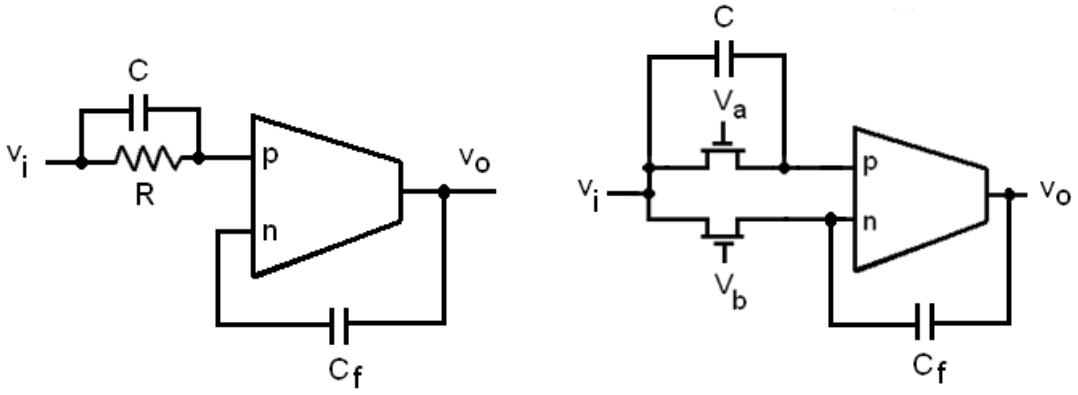
(a) (b)

Fig. 6.8 (a) OTRA based P Controller. (b) MOS– C implemented P Controller.

6.5.2 PI Controller

The OTRA based proposed PI controller is shown in Fig. 6.9(a) and its MOS-C implementation is shown in Fig. 6.9(b). Using routine analysis of this controller the voltage transfer function can be computed as

$$G_{PI}(s) = \frac{V_o}{V_i} = \frac{C}{C_f} + \frac{1}{sC_fR} \tag{6.23}$$



(a) (b)

Fig. 6.9 (a) OTRA based PI Controller. (b) MOS− C implemented PI Controller.

From (6.23) the controller parameters can be expressed as

$$K_p = \frac{C}{C_f},\ K_i = \frac{1}{C_fR} \tag{6.24}$$

It is clear from (6.24) that K_p value can be adjusted independent of K_i by varying C, and K_i can be independently controlled by varying R.

6.5.3 PD Controller

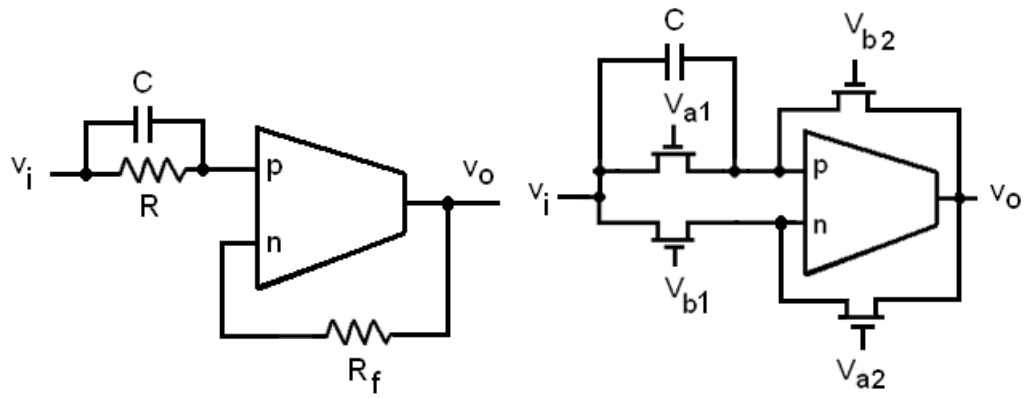
Figure 6.10 shows the proposed PD controller circuit and the transfer function of this controller can be obtained as

$$G_{PD}(s) = \frac{V_o}{V_i} = \frac{R_f}{R} + sCR_f \tag{6.25}$$

Equation (6.25) results in

$$K_p = \frac{R_f}{R},\ K_d = CR_f \tag{6.26}$$

From (6.26) it is clear that by varying R, K_p value can be adjusted independent of K_d and by simultaneous variation of R_f and R, K_d can be independently controlled. In MOS–C implemented structure, as shown in Fig. 6.10 (b), the controller parameters can be electronically tuned through appropriate choice of gate voltages of the transistors used for implementing the resistive elements.



(a) (b)

Fig. 6.10 (a) Proposed PD Controller. (b) MOS− C implemented PD Controller.

6.5.4 PID Controller

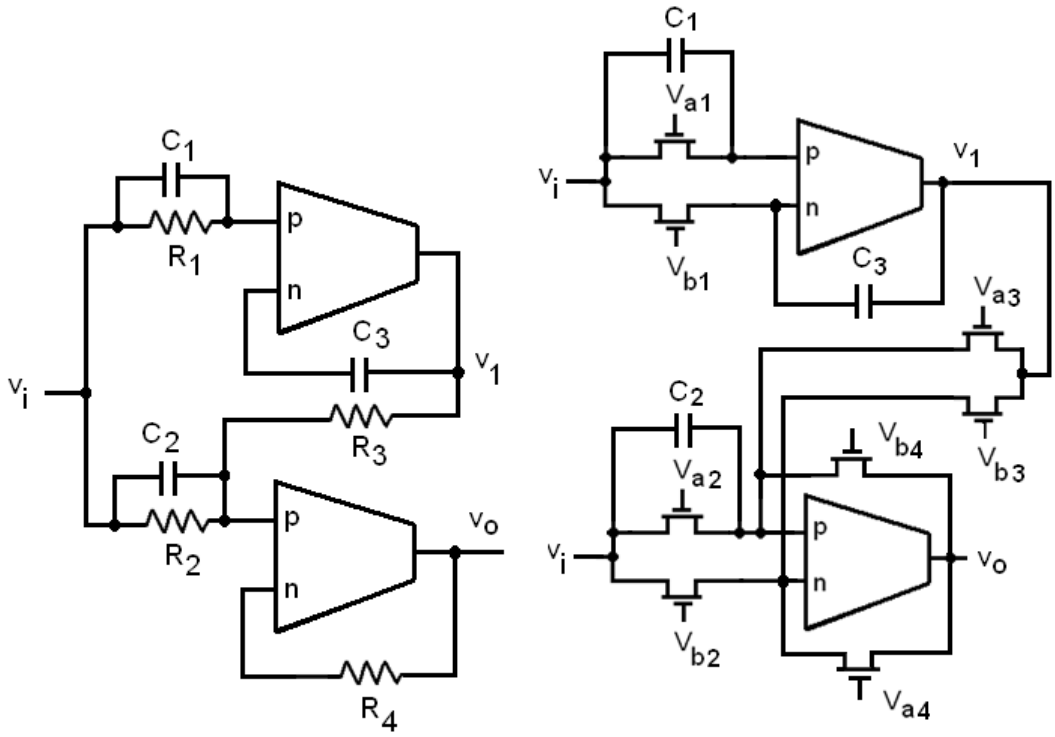
The proposed PID-Controller can be derived by combining the proposed PI and PD controllers and is shown in Fig. 6.11. The routine analysis of this circuit gives the transfer function of the controller as

$$G_{PID}(s) = \frac{V_o}{V_i} = \left(\frac{R_4}{R_2} + \frac{R_4}{R_3}\frac{C_1}{C_3}\right) + \frac{R_4}{sC_3R_1R_3} + sC_2R_4 \qquad (6.27)$$

From (6.27) the controller parameters can be identified as

$$K_p = \frac{R_4C_1}{R_3C_3} + \frac{R_4}{R_2}\ , K_i = \frac{R_4}{R_1R_3C_3} \quad \text{and} \quad K_d = C_2R_4 \qquad (6.28)$$

It is clear from (6.28) that K_p value can be adjusted independently by varying R_2, independent tuning of K_i is possible through R_1 variation whereas K_d can be controlled independently by simultaneous variation of R_2 , R_3 and R_4.



(a) (b)

Fig. 6.11 (a) OTRA based PID Controller. (b) MOS− C implemented PID Controller.

6.6 NONIDEALITY ANALYSIS

The behaviour of the OTRA based circuits may deviate from the ideal one in practice. This section examines the effect of nonideality of OTRA as discussed in section 2.3, on proposed controllers and suggests the compensation so as to make them suitable for high frequency applications.

6.6.1 Nonideality analysis of P controller

Considering the effect of nonideality of OTRA, the controller transfer function given by (6.22) modifies to

$$G_P\big|_n(s) = \frac{R_2}{R_1} \quad \varepsilon_{uc}(s) \tag{6.29}$$

where $\varepsilon_{uc}(s) = \frac{1}{(1+sC_pR_2)}$ is uncompensated error function.

The error $\varepsilon_{uc}(s)$, so introduced must be accounted for; therefore compensation must be employed for high-frequency applications. Considering the circuit of Fig. 6.12 the transfer function can be written as

$$G_P\big|_{n\_c}(s) = \frac{R_2}{R_1}\,\varepsilon_c(s) \tag{6.30}$$

where $\varepsilon_c(s) = \frac{1}{1+R_2(sC_p-Y)}$ is compensated error function.

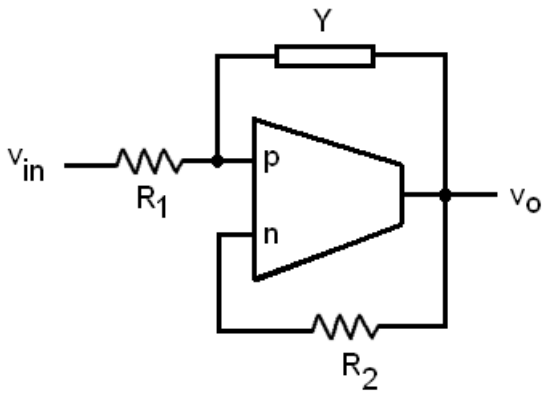


Fig. 6.12 Compensated P controller.

By choosing Y = sC_p, $\varepsilon_c(s)$ reduces to its ideal value of unity thereby making (6.29) same as (6.22). Thus, passive compensation of the P controller can be achieved by using a single capacitor connected between the output and the non-inverting terminal of the OTRA.

6.6.2 Nonideality Analysis of PI Controller

The PI controller transfer function in presence of nonidealities given by (6.23) modifies to

$$G_{PI}\big|_n(s) = \left(\frac{1}{s(C_f+C_p)R} + \frac{C}{(C_f+C_p)}\right) \tag{6.31}$$

By pre-adjusting the value of capacitors C_f, the effect of C_p can be eliminated and self compensation can be achieved.

6.6.3 Nonideality Analysis of PD Controller

Due to the nonideality effect of OTRA the transfer function of PD controller changes and

can be expressed as

$$G_{PD}\big|_{n}(s) = \frac{R_f}{R(1+sC_pR_f)} + \frac{sCR_f}{1+sC_pR_f} \tag{6.32}$$

For high-frequency applications, compensation methods must be employed to account for the error introduced in (6.24). Considering the circuit shown in Fig. 6.13, (6.32) modifies to

$$G_{PD}\big|_{n\_c}(s) = \frac{R_f}{R(1+R_f(sC_p-sY))} + \frac{sCR_f}{1+R_f(sC_p-sY)} \tag{6.33}$$

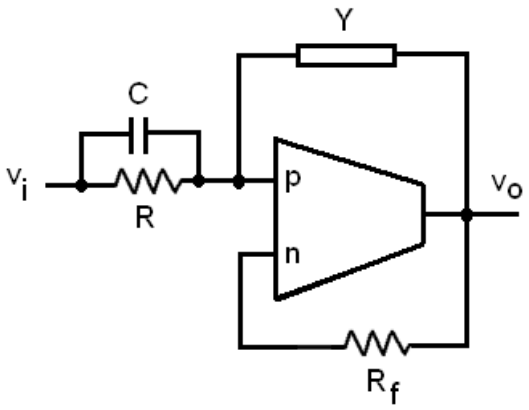


Fig. 6.13 Compensated PD Controller.

By taking Y = sC_p, (6.33) reduces to (6.24). So the error can be eliminated by connecting a single capacitor between the non inverting terminal and the output as shown in Fig. 6.13, and the passive compensation can be achieved.

6.6.4 Nonideality Analysis of PID Controller

The modified transfer function of the PID controller, due to nonideality of OTRA can be computed as

$$G_{PID}\big|_{n}(s) = \left(\frac{R_4C_1}{R_3\,(C_3+C_{p1})(1+sC_{p2}R_4)} + \frac{R_4}{R_2(1+sC_{p2}R_4)}\right) + \left(\frac{R_4}{R_1R_3\,s(C_3+C_{p1})(1+sC_{p2}R_4)}\right) + \left(\frac{sC_2R_4}{(1+sC_{p2}R_4)}\right) \tag{6.34}$$

Passive compensation method is employed to account for the error introduced in (6.27). The effect of C_{p1} can be eliminated by pre-adjusting the value of capacitors C_3 and thus achieving self compensation. The sC_{p2} term appearing in parallel to R_4 will result in introduction of a parasitic pole having radian frequency as $\omega = 1/R_4C_{p2}$. The effect of C_{p2} can be eliminated by connecting a single admittance Y between the noninverting and the output terminals as shown in Fig. 6.14.

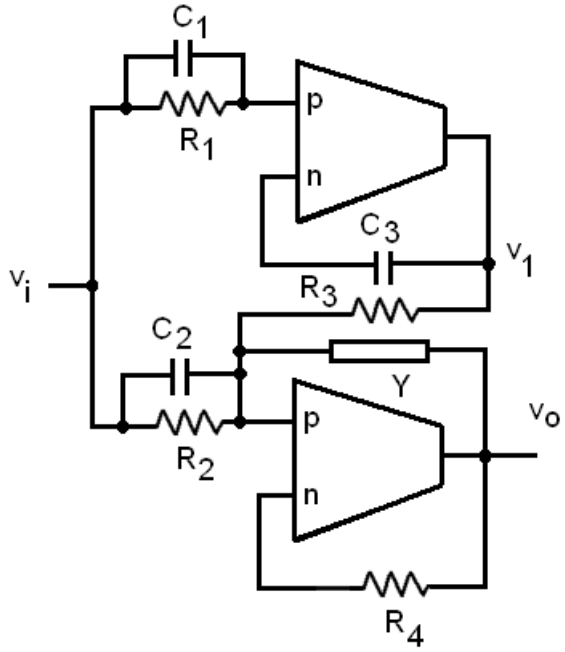


Fig. 6.14 Compensated PID Controller.

Considering the circuit of Fig. 6.14., (6.34) modifies to

$$G_{PID}\big|_{n\_c}(s) = \left(\frac{R_4C_1}{R_3\,C_3\left(1+s(C_{p2}-Y)R_4\right)} + \frac{R_4}{R_2\left(1+s(C_{p2}-Y)R_4\right)}\right)$$

$$+\left(\frac{R_4}{R_1R_3\,sC_3(1+s(C_{p2}-Y)R_4)}\right) + \left(\frac{sC_2R_4}{R_2(1+s(C_{p2}-Y)R_4)}\right) \qquad (6.35)$$

By taking $Y = sC_{p2}$, (6.35) reduces to (6.27) thus eliminating the effect of C_{p2} and hence achieving the passive compensation.

6.7 SIMULATION RESULTS

The functionality of all the proposed controller circuits is verified through SPICE simulations using circuit schematic of Fig. 2.9 for OTRA realization.

6.7.1 P Controller

For the simulation of proposed P controller (Fig. 6.8), the passive component values are chosen as R_1 = 10 KΩ and R_2 = 20 KΩ. An aspect ratio of W/L = 0.18µm/0.54µm is used for both the transistors used for implementing passive resistor R_1 whereas for those used to implement R_2 the aspect ratio is chosen to be 0.18µm/1.08µm. Gate voltages are set as $V_{a1} = V_{a2}$ = 1.2 V, V_{b1} = 0.59 V and V_{b2} = 0.64 V which result in resistance values as $R_1 \approx$ 10 KΩ and $R_2 \approx$ 20 KΩ. These passive component values result in controller parameter value K_P = 2. For time domain analysis, a 3 mV, 2.5 MHz sinusoidal input voltage is applied. The ideal and simulated frequency responses of the P controller are depicted in Fig. 6.15 and the time domain responses are shown in Fig. 6.16. Figure 6.17 shows the transfer curve of P controller for different values of K_P for which R_1 is kept constant at 10 KΩ and R_2 is varied. In MOS implemented circuit value of R_2 is changed by modifying gate voltage V_{b2} while keeping V_{a2} constant. The gate voltage V_{a2} is assigned a value of 1.2 V and V_{b2} is placed at 0.64 V, 0.89 V, and 0.99 V resulting in R_2 values of 20 KΩ, 30 KΩ and 40 KΩ respectively. This shows the electronic tunability feature of the proposed controller.

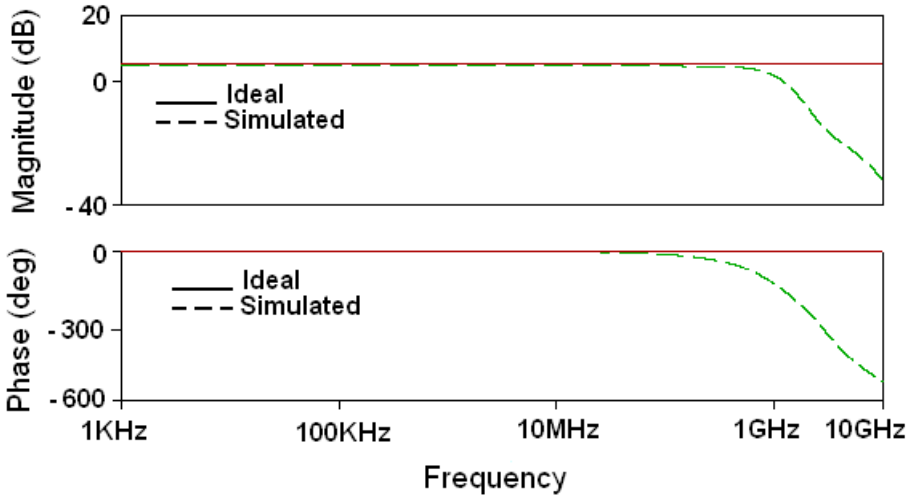


Fig. 6.15 Frequency response of P controller.

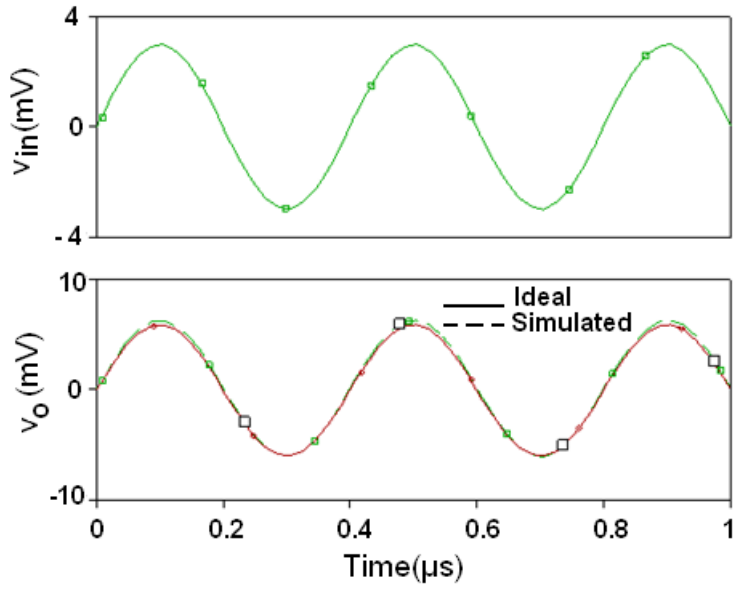


Fig. 6.16 Transient response of the P controller.

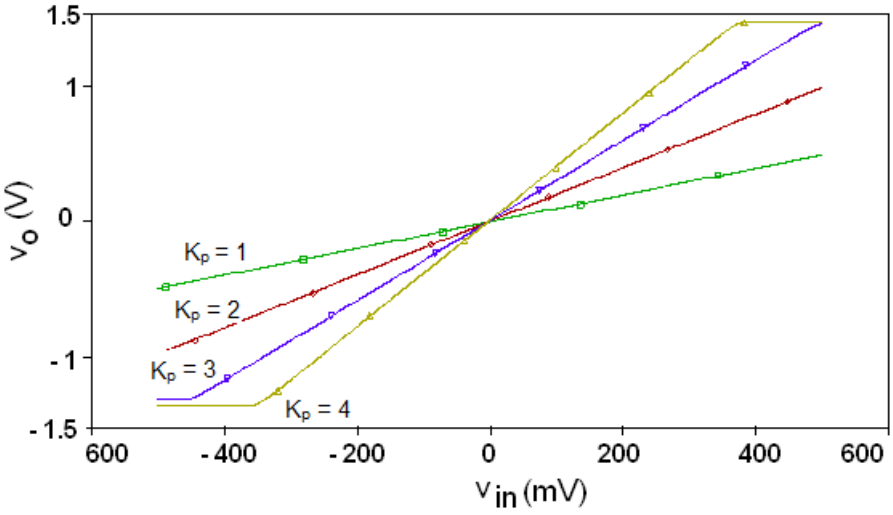


Fig. 6.17 Transfer curve of P controller.

6.7.2 PI Controller

For the simulation of proposed PI controller (Fig. 6.9) the passive component values are chosen as R_1 = 50 KΩ, C_1 = 4 pF and C_f = 2 pF. An aspect ratio of W/L = 0.18µm/1.08µm is used and gate voltages are set as V_{a1} = 1 V and V_{b1} = 0.5 V for the transistors used to implement resistor R_1 which result in resistance value as $R_1 \approx$ 50 KΩ. Using the passive component values the controller parameters are computed to as K_p = 2 and $K_i = 10^7\ s^{-1}$. For time domain analysis, a 3 mV step input voltage with

20 ns rise time is applied. The ideal and simulated frequency responses of the PI controller are depicted in Fig. 6.18 and the time domain responses for the controller are shown in Fig. 6.19.

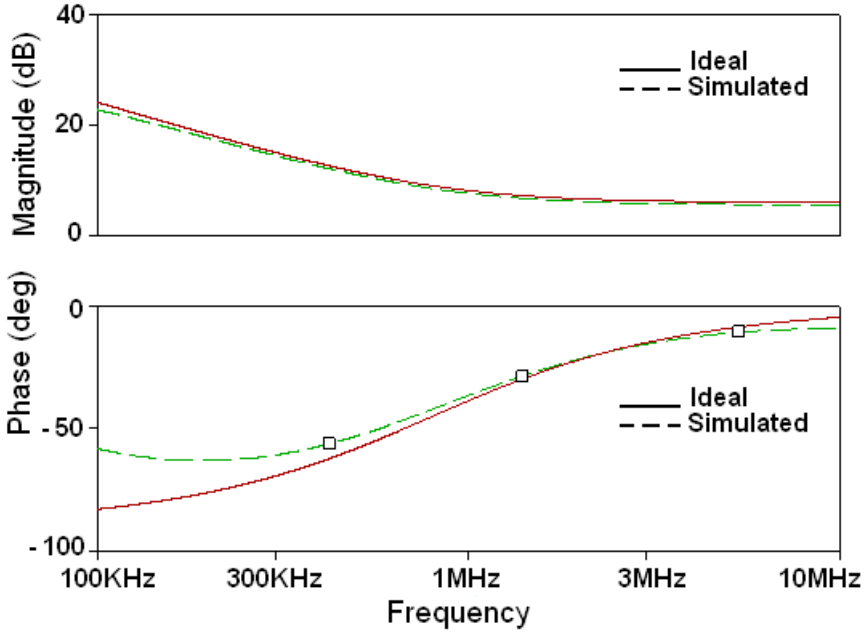


Fig. 6.18 Frequency response of the PI Controller.

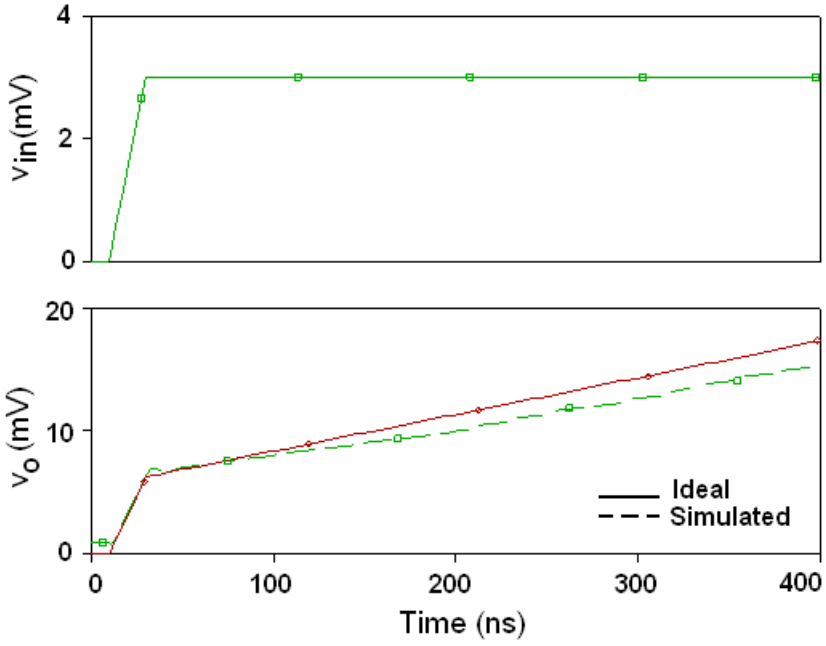


Fig. 6.19 Transient response of the PI Controller.

6.7.3 PD Controller

The passive component values for proposed PD controller are chosen as R = 10 KΩ, R_f = 20 KΩ and C = 20 pF. For MOS-C implemented controller an aspect ratio of W/L = 0.18µm/0.54µm is chosen for the transistors used for implementing R whereas W/L = 0.18µm/1.08µm is used for the transistors which realize R_f. Gate voltages are set as $V_{a1} = V_{a2} = 1.2$ V, $V_{b1} = 0.59$ V and $V_{b2} = 0.64$ V which result in resistance values as R ≈ 10 KΩ and R_f ≈ 20 KΩ.The controller parameters are computed to be $K_p = 2$ and $K_d = 0.4$ µs. For transient analysis of PD controller, a 3 mV peak triangular input voltage is applied. The ideal and simulated frequency responses of the PD controller are shown in Fig. 6.20 whereas in Fig. 6.21 the transient responses are shown. Both ideal and simulated results are found in close agreement.

6.7.4 PID Controller

For the proposed PID controller shown in Fig. 6.11, the values of passive element are chosen as $R_1 = R_2 = R_3 = R_4 = 50$ KΩ, $C_1 = C_3 = 10$ pF and $C_2 = 0.05$ pF. For time domain analysis, a 3 mV step signal with 10 ns rise time is applied. For MOS-C implemented PID controller shown in Fig. 6.14(b) an equal aspect ratio of W/L= 0.18µm/1.8µm, is chosen for all the transistors used for implementing the resistances.

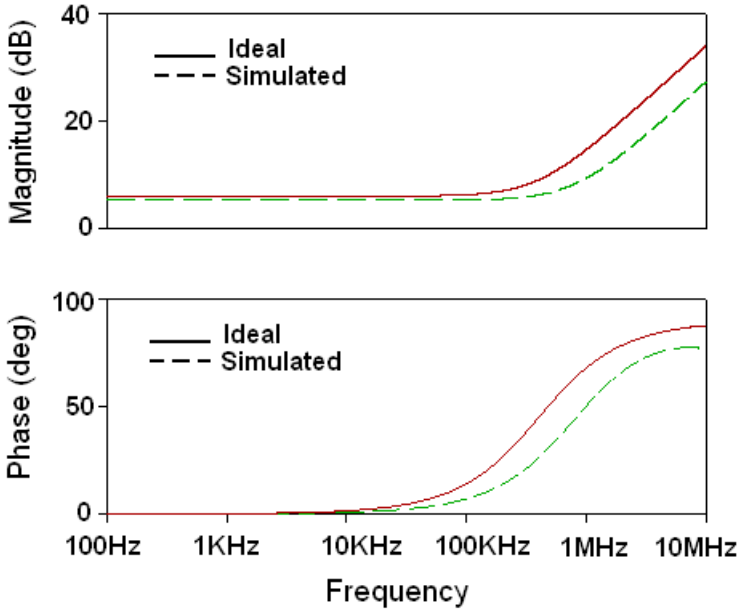


Fig. 6.20 Frequency response of the PD Controller.

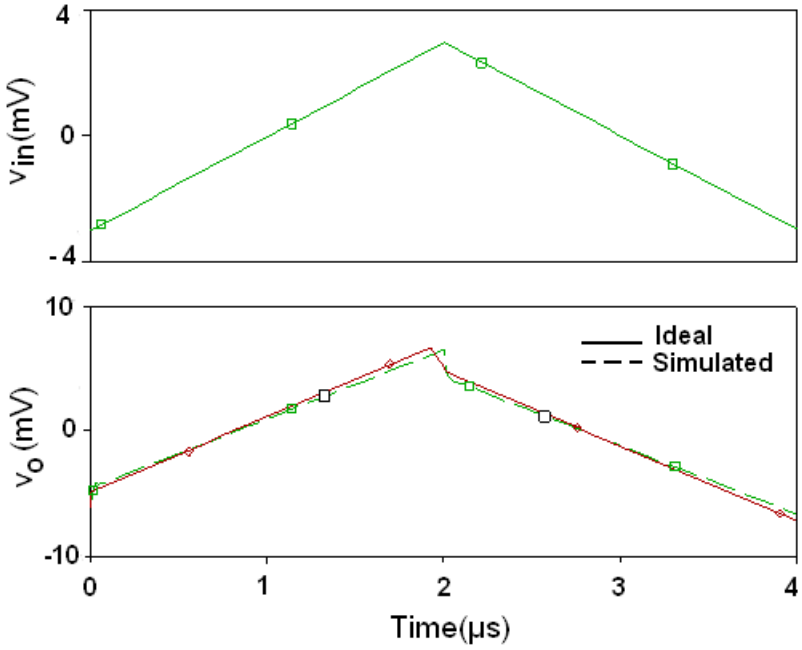


Fig. 6.21 Transient response of the PD Controller.

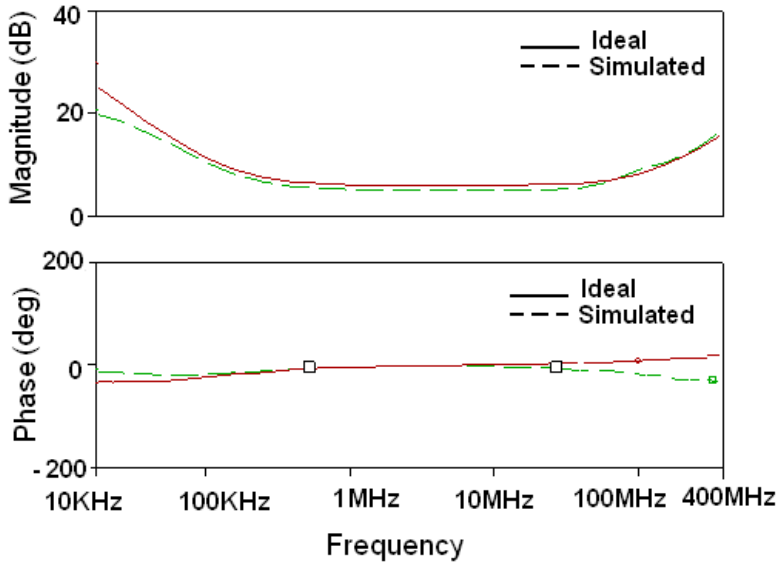


Fig. 6.22 Frequency response of the PID Controller.

Gate voltages are set as $V_{a1}= V_{a2} = V_{a3} = V_{a4} = 1$ V and $V_{b1}= V_{b2} = V_{b3} = V_{b4} = 0.5$ V which result in resistance values as $R_1 = R_2 = R_3 = R_4 \approx 50$ KΩ and the chosen value of capacitances are $C_1 = C_3 = 10$ pF and $C_2 = 0.05$ pF. Using these passive component values various controller parameters can be computed as $K_p = 2$, $K_i = \frac{R_4}{R_1 R_3 C_3} = 2 \times 10^6\ s^{-1}$ and $K_d = C_2R_4 = 2.5$ ns. Figure 6.22 represents the ideal and simulated frequency responses of PID controller and the transient responses are shown

in Fig. 6.23.

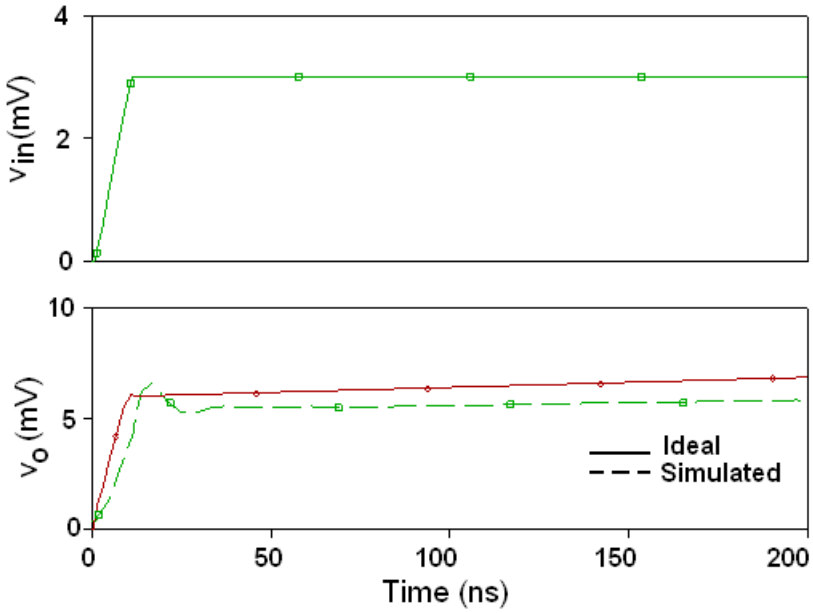


Fig. 6.23 Transient response of the PID Controller.

6.8 PERFORMANCE EVALUATION OF THE PROPOSED CONTROLLERS

To evaluate the performance of various controllers their effect on a second order plant is analyzed by forming a closed loop system as shown in Fig. 6.24. An LPF [44] as shown in Fig. 6.25 is used as a second order system. The LPF circuit can also be made electronically tunable by implementing all the related resistors using MOS transistors operating in linear region. The transfer function of the LPF using equal component design with $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C$ can be derived as

$$\frac{V_0(s)}{V_i(s)} = \frac{\frac{1}{R^2C^2}}{s^2+2\frac{s}{CR}+\frac{1}{R^2C^2}} \tag{6.36}$$

The LPF of Fig. 6.25 can be characterized by

$$\omega_n = \frac{1}{RC} \ , \xi = 1 \tag{6.37}$$

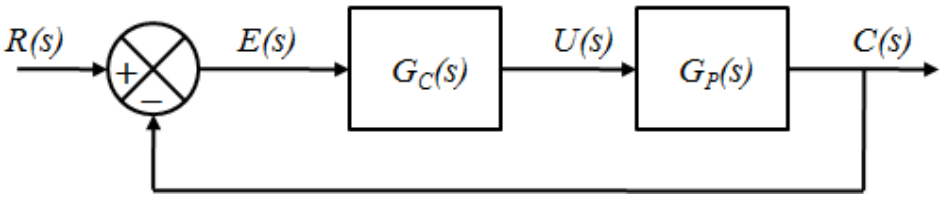


Fig. 6.24 Closed loop control system.

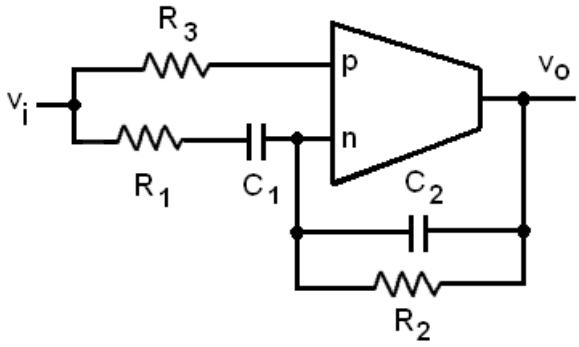


Fig. 6.25 The second order low pass filter.

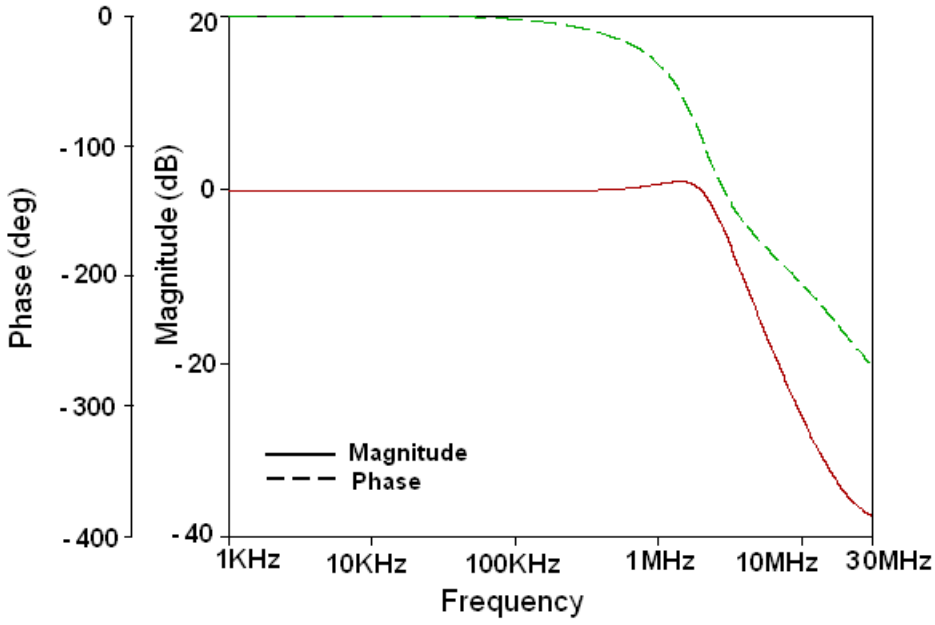


Fig. 6.26 Frequency response of the second order LPF.

First the step response of the open loop second order system is studied and then the effect of various proposed controllers is observed by realizing a closed loop system. The LPF is designed for ω_n = 3.98 MHz and ξ = 1.0 for which capacitance values are chosen as

$C_1 = C_2 = 20$ pF and the resistance value is computed as $R_1 = R_2 = R_3 = 2$ KΩ. The frequency response of the LPF is shown in Fig. 6.26. For time domain analysis a step signal of 50 mV is applied and the simulated response is shown in Fig. 6.27.

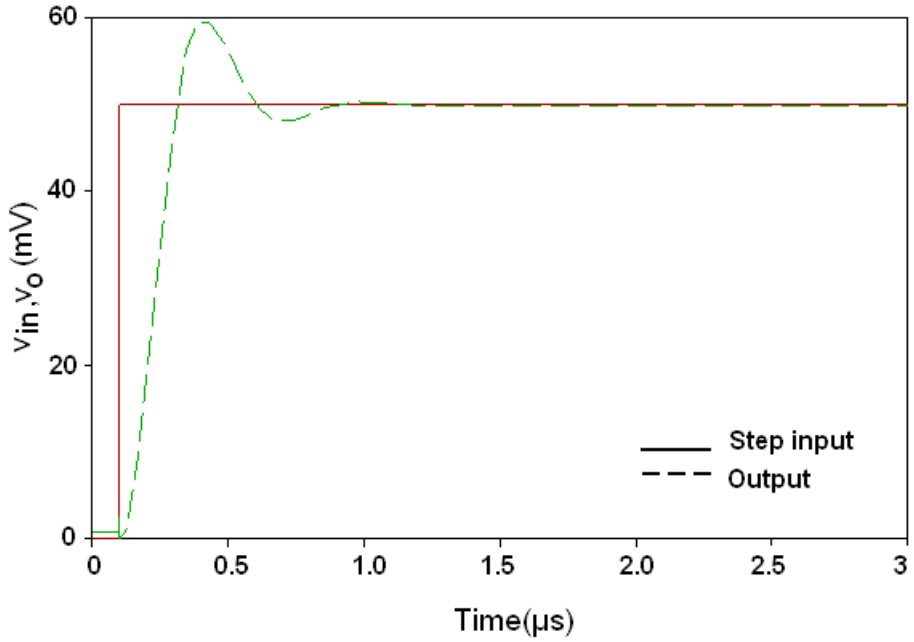
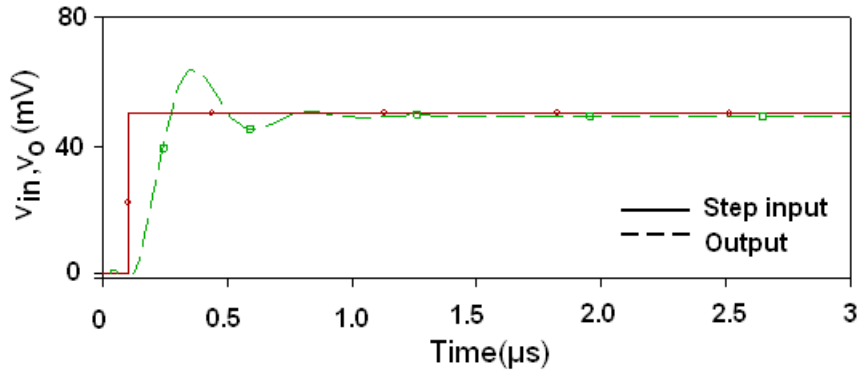
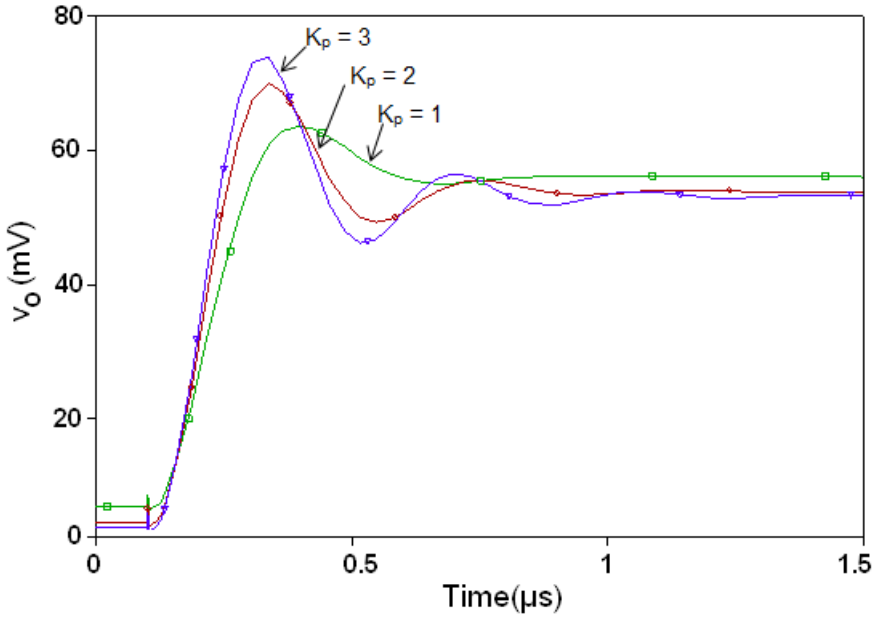


Fig. 6.27 Step Response of the LPF.

To compare the performance of the second order system with and without P-controller, step responses of the system for a 50 mV step input are recorded while choosing $K_P = 2$. Step response of the closed loop system is shown in Fig. 6.28 (a) whereas the effect of varying K_p on closed loop second order system response ,with K_p = 1, 2 and 3 respectively, has been shown in Fig. 6.28 (b). These values of K_p are achieved by keeping $R_1 = 10$ KΩ, while changing R_2 from 10 KΩ to 30 KΩ in steps of 10 KΩ. In MOS-C implemented controller R_2 is varied by assigning different gate voltage to the transistors used to realize this resistor. It is observed from Fig. 6.28 (b) that the rise time reduces with increasing magnitude of K_p however, the peak overshoot increases. For fair comparison the performance parameters such as overshoot, peak output, rise time and settling time are measured and recorded in Table 6.1 and it was observed that the system performance improves with P controller in terms of rise time; however, the peak overshoot percentage and settling time are increased.



(a)



(b)

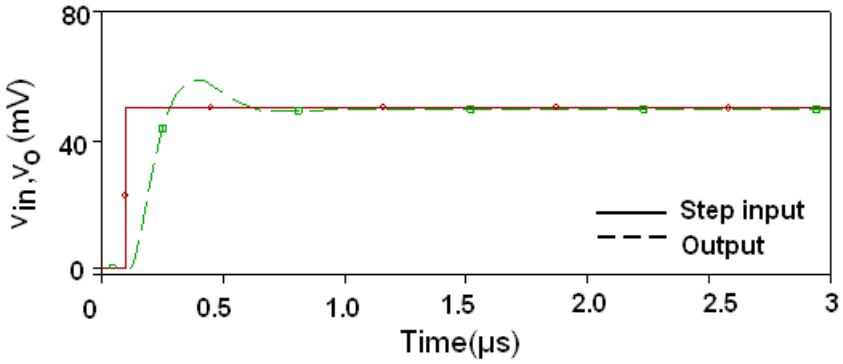
Fig. 6.28 (a) Step Response of second order closed loop system with P controller.

(b) Step response with variable K_p.

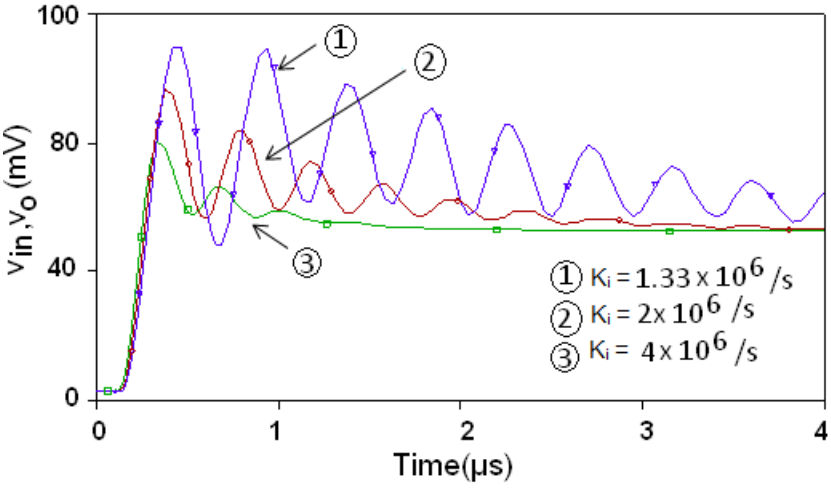
Table 6.1: Performance Comparison of closed loop system with and without P controller.

Parameter	Without P-Controller	With P-Controller
Overshoot	19.56 %	30.14 %
Peak output	58.26 mV	62.64 mV
Rise time	140.43 ns	108.75 ns
Settling time	303.12 ns	675.11 ns

The step response of closed loop system with PI controller is shown in Fig. 6.29 (a) having $K_p = 2$ and $K_i = 10^7 s^{-1}$ and Fig. 6.29 (b) shows step response for varying values of K_i while keeping $K_p = 2$ constant. The performance parameters for PI controller are recorded in Table 6.2 which indicates that PI controller influences mainly the settling time as compared to all other parameter.



(a)



(b)

Fig. 6.29 (a) Step response of closed loop system with PI controller. (b) Step response with variable K_i keeping K_p constant.

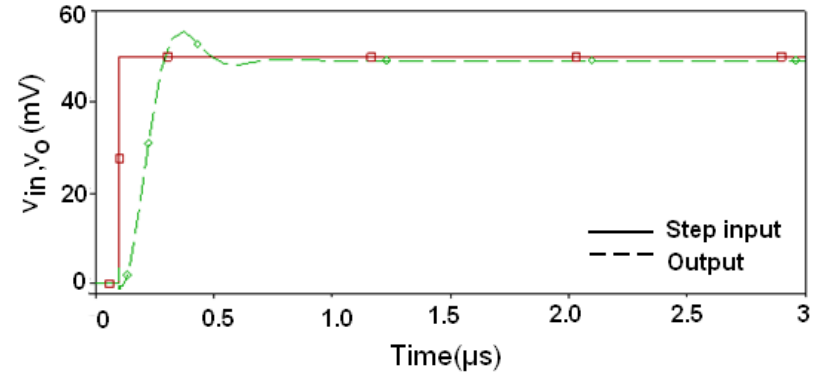
The closed loop step response with PD controller is depicted in Fig. 6.30(a) with $K_p = 2$ and $K_d = 0.4$ μs and in Fig. 6.30(b) step response for varying values of K_d while keeping $K_p = 2$ constant, is shown. Table 6.3 lists the performance parameters for PD controller and there form it can be observed that the PD controller improves all the parameter, prominently overshoot and very small improvement in settling time is observed.

Table 6.2: Performance Comparison of closed loop system with and without PI controller.

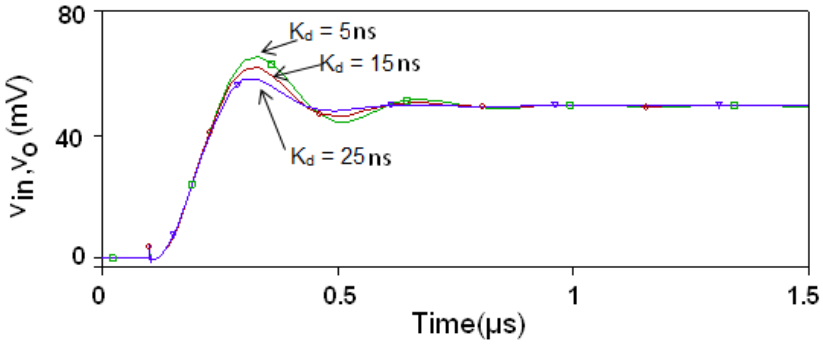
Parameter	Without PI Controller	With PI Controller
Overshoot	19.56 %	18.76 %
Peak output	58.26 mV	57.83 mV
Rise time	140.43 ns	112.28 ns
Settling time	303.12 ns	266.11 ns

Table 6.3: Performance Comparison of closed loop system with and without PD controller.

Parameter	Without PD Controller	With PD Controller
Overshoot	19.56 %	12.89 %
Peak output	58.26 mV	56.53 mV
Rise time	140.43 ns	124.27 ns
Settling time	303.12 ns	278.97 ns



(a)



(b)

Fig. 6.30 (a) Step Response of second order closed loop system with PD controller. (b) Step response with variable K_d keeping K_p constant.

Step response of the closed loop system with PID controller for a 50 mV step signal having $K_p = 2$, $K_i = 2 \times 10^6\ s^{-1}$ and $K_d = 2.5$ ns is shown in Fig. 6.31. The performance parameters are recorded in Table 6.4 which clearly shows a notable improvement in all the system performance parameters.

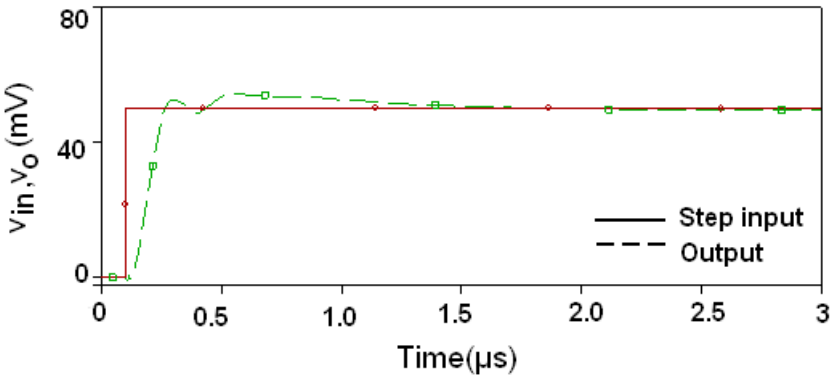


Fig. 6.31 Step Response of closed loop second order system with PID controller.

Table 6.4: Performance Comparison of closed loop system with and without PID controller.

Parameter	Without PID Controller	With PID Controller
Overshoot	19.56 %	8.16 %
Peak output	58.26 mV	52.59 mV
Rise time	140.43 ns	99.75 ns
Settling time	303.12 ns	252.27 ns

6.9 PERFORMANCE COMPARISON OF THE CONTROLLERS

In Table 6.5 performance parameters of all the four types controllers studied so far are summarized. This table clearly indicates the PD controller prominently improves the overshoot whereas PI controller influences mainly the settling time as compared to all other parameter. PID includes best features of all individual controllers and results in improvement of all the performance measure parameters as is also verified through step response for a 50 mV step signal shown in Fig. 6.31.

Table 6.5: Performance Comparison of closed loop system with and without controllers

Parameter	Open loop LPF	With P Controller	With PD Controller	With PI Controller	With PID Controller
Overshoot	19.56 %	30.14 %	12.89 %	18.76 %	8.16 %
Peak output	58.26 mV	62.64 mV	56.53 mV	57.83 mV	52.59 mV
Rise time	140.43 ns	108.75 ns	124.27 ns	112.28 ns	99.75 ns
Settling time	303.12 ns	675.11 ns	278.97 ns	266.11 ns	252.27 ns

6.10 CONCLUDING REMARKS

This chapter describes OTRA based circuits suitable for instrumentation and control application. TIA, suitable for amplification of signals from current-source transducers, is proposed first. The proposed amplifier provides high gain for a wide range of frequencies, having a 3dB bandwidth independent of its gain. The gain of the proposed amplifier is electronically tuned by implementing the passive resistor using MOS transistor which also makes circuit MOS-C implementable. The proposed circuit can easily be compensated for parasitics. The proposed circuit, to the best knowledge of author, is the only TIA which uses current mode techniques, though an opamp based TIA is proposed in [100] which uses three opamps and nine resistors; quite a large number as compared to proposed TIA.

The design of OTRA based controllers, namely P, PI, PD and PID controllers have been presented next. The controller parameters K_p, K_d and K_i can be adjusted independently and are elctronically tunable as well. The effect of the proposed controllers on a second order closed loop system was analyzed. Performance analysis reveals that PD controller improves percentage overshoot, PI controller refines settling time while PID as a combination of the two, enhances transient as well as steady state time response of the system.

All the circuits presented in this chapter are validated through SPICE simulations. Experimental results are also included for TIA. The simulated results are in line with the proposed theory. The effect of OTRA parasitics, on the performance of all proposed applications, is also analyzed. For high-frequency applications, compensation methods are employed, to account for the error introduced due to parasitics.

CHAPTER – 7
OTRA BASED NONLINEAR CIRCUITS AND THEIR APPLICATIONS

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, "**Voltage Mode Pulse Width Modulator Using Single Operational Transresistance Amplifier,"** Journal of Engineering, Volume 2013, Article ID 309124, 6 pages, doi.org/10.1155/2013/309124.

2. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, B. Sriram, **"Single OTRA based analog multiplier and its applications,"** ISRN Journal of Electronics Volume 2012, Article ID 890615, 7 pages, doi:10.5402/2012/890615.

3. Mayank Bothra, Rajeshwari Pandey, Neeta Pandey, **"Versatile Voltage Controlled Relaxation Oscillators Using OTRA,"** International Conference on Electronics and Computer Technology, (ICECT-2011), pp. 394-398, April 2011.

7.1 INTRODUCTION

The circuits proposed so far are designed to behave linearly. In these circuits the output signal varies with input signal in a linear manner and this behaviour is realized through negative feedback. Another class of circuits, termed as nonlinear circuits, possesses highly nonlinear input to output characteristics. Nonlinear behaviour can be achieved either by using a high gain amplifier in open loop or through positive feedback or by implementing the feedback network with nonlinear elements [103] such as diodes, transistors and analog switches etc. Nonlinear operations on analog signals are often required in communication, instrumentation and measurement, and control system design. Therefore this chapter is devoted to nonlinear applications of OTRA. Design of a voltage controlled multivibrators (VCM) is described first and an application of this circuit in the field of communication is also illustrated. A modulator circuit based on pulse modulation scheme is presented next and can be used for applications such as speed control of DC motors and DC to DC converters. These proposed applications use OTRA in positive feedback. Analog multiplier is yet another application proposed in this chapter which can be used for various analog operations such as true RMS conversion, analog division, square and square root computation, voltage controlled amplification, filtering and oscillation.

7.2 VOLTAGE CONTROLLED MULTIVIBRATOR

Non linear oscillators are used to generate waveforms like square, triangular, sawtooth etc. These generators essentially employ a basic circuit building block known as bistable multivibrator or Schmitt trigger. The square and triangular waveforms can be generated by using a general scheme of connecting an integrator in feedback loop of a bistable multivibrator. If the frequency of this waveform can be controlled by an external control voltage then this generator is known as voltage controlled multivibrators (VCM). The VCMs are an important class of circuits and find application in function generators, frequency synthesizers and communications. In the following subsection OTRA based VCM has been presented which can also be used as a general square/triangular waveform generator by grounding the control voltage terminal.

7.2.1 Proposed Circuit

The proposed circuit is based on the concept that a triangular/square wave can be generated by using a current source to alternately charge and discharge a capacitor followed by a Schmitt trigger [110]. The charging begins when capacitor voltage falls to a lower threshold voltage V_{TL}

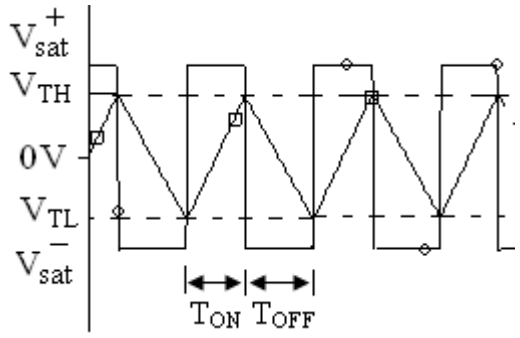


Fig. 7.1Charging/Discharging of capacitor.

resulting in the output of the Schmitt trigger to switch to positive saturation level V_{sat}^{+}. Similarly if the capacitor voltage rises to an upper threshold V_{TH} the discharging takes place and Schmitt trigger output is forced to negative saturation level V_{sat}^{-} as shown in Fig. 7.1. If the value of the charging/discharging current is made to depend on an external control voltage V_C then the charging time (T_{ON}) and discharging time (T_{OFF}) will also be a function of external control voltage. The proposed circuit is shown in Fig. 7.2. The circuit can be viewed as two cascaded blocks. Circuitry comprising of OTRA 1, resistance R_3 and capacitor C_1 is a simple integrator, while the circuit consisting of OTRA 2, resistors R_2 and R_4 is a Schmitt trigger [66] working in the clockwise mode. Control voltage V_C controls the charging and discharging current through resistor R_1.The triangular wave is available at the output of integrator whereas, at the output of Schmitt trigger a square wave is obtained.

The output of the integrator provides the upper and lower threshold limits of the Schmitt trigger which can be calculated respectively as

$$V_{TH} = \frac{R_2}{R_4} V_{sat}^{+} \tag{7.1}$$

$$V_{TL} = \frac{R_2}{R_4} V_{sat}^{-} \tag{7.2}$$

where V_{sat}^{+} and V_{sat}^{-} signify the positive and negative saturation output levels respectively of the Schmitt trigger. For frequency calculation of the output signal, the time taken by the capacitor to charge and discharge to V_{TH} and V_{TL} must be calculated. The time taken by the C_1 to charge to V_{TH} from level V_{TL} is given by

$$T_{ON} = \frac{(V_{TH} - V_{TL})\, C_1 R_1 R_3}{V_{sat}^{+} R_1 + V_C R_3} \tag{7.3}$$

whereas, the time taken by the C_1 to discharge to V_{TL} from level V_{TH} can be expressed as

$$T_{OFF} = \frac{(V_{TL} - V_{TH}) C_1 R_1 R_3}{V_{sat}^{-} R_1 + V_C R_3} \tag{7.4}$$

The frequency (f) of the output signal is given by

$$f = \frac{1}{T_{ON} + T_{OFF}} \tag{7.5}$$

If V_{TH} and V_{TL} are assumed to be equal in magnitude to V_T and V_{sat}^{+} and V_{sat}^{-}, to V_O then the frequency can be expressed as

$$f = \frac{(V_O R_1)^2 - (V_C R_3)^2}{4 V_O V_T C_1 {R_1}^2 R_3} \tag{7.6}$$

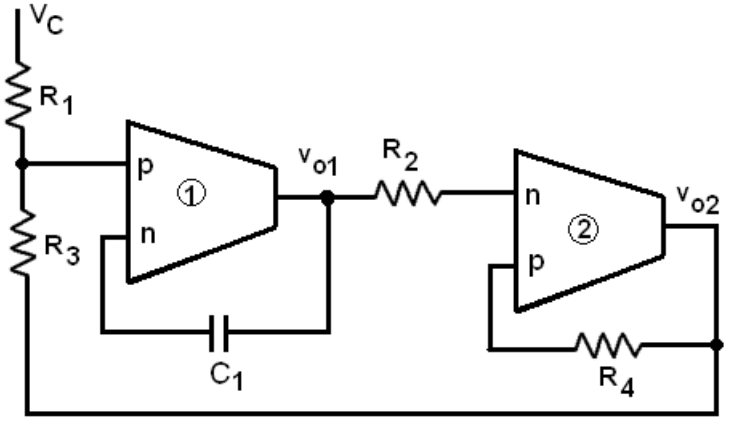


Fig. 7.2 The proposed VCM circuit

The frequency of output waveform is a function of applied control voltage and is described by the equation

$$f = f_0 + KV_C^2 \tag{7.7}$$

where $f_0 = \frac{V_O}{4V_T C_1 R_3}$ and $K = \frac{-R_3}{4V_O V_T C_1 {R_1}^2}$ (7.8)

It is observed that frequency of the output waveform is a function of applied control voltage (V_C). The change in frequency with respect to control voltage V_C can be expressed as

$$\frac{\partial f}{\partial V_C} = \frac{-V_C R_3}{2V_O V_T C_1 {R_1}^2} \tag{7.9}$$

and sensitivity of output frequency, to changes in the input control voltage level, is given by

$$S_f^{V_C} = \frac{2}{1-\frac{(V_O R_1)^2}{(V_C R_3)^2}} \tag{7.10}$$

It may be noted from (7.10) that sensitivity of output frequency can be adjusted to the desired level by controlling value of R_3 and /or R_1. Tuning range of this oscillator circuit is dictated by (7.3) if V_C is negative or by (7.4) if V_C is positive, as expression for T_{ON} and T_{OFF} on the whole must be positive. Also, amplitude of triangular wave (V_T) can be changed by changing values of R_2 and /or R_4 as shown in (7.1) and (7.2).

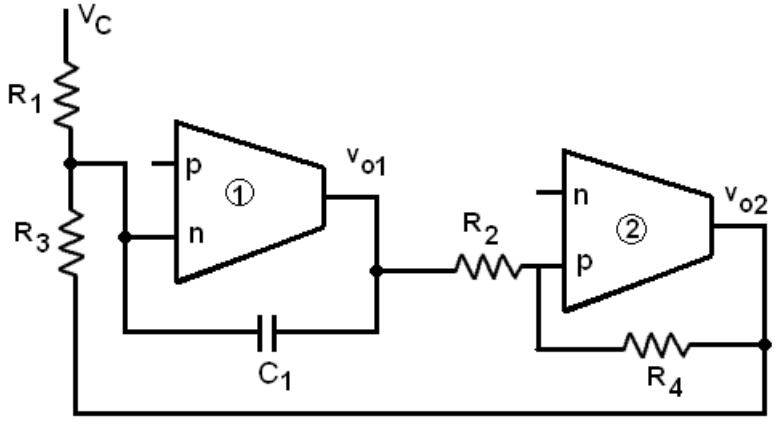


Fig.7.3. Alternate Configuration of VCM

An alternate VCM configuration with Schmitt trigger connected in the counter clock wise mode and the integrator connected in inverting mode is proposed in Fig. 7.3. This structure gives outputs differing in phase as obtained from the configuration given in Fig. 7.2. However all the relevant equations would remain same as those computed for the circuit of Fig. 7.2.

7.2.2 Nonideality Analysis

For this application, OTRA was realized using CFOA as given in Fig. 2.7. The nonidealities of CFOA modify threshold limits of the Schmitt trigger as

$$V_{TH} = \frac{R_2+(R_x \| R_z)}{R_4+R_x} V_{sat}^{+} \tag{7.11}$$

$$V_{TL} = \frac{R_2+(R_X \| R_z)}{R_4+R_x} V_{sat}^{-} \tag{7.12}$$

Typically $R_z >> R_x$ so $R_x \| R_z \approx R_x$, Equations (7.11) and (7.12) reduce to (7.1) and (7.2) respectively if R_2 and $R_4 >> R_x$ so external resistance connected at the input of OTRA should be much larger than R_x.

7.2.3 Simulation and Experimental Results

The proposed circuit is simulated through SPICE, using CFOA based OTRA realization to validate the theoretical results. Supply voltages used for simulation are ± 5 V. Component values are chosen as $R_1 = R_2 = 500\ \Omega$, $R_3 = 1\ K\Omega$, $R_4 = 750\ \Omega$ and $C_1 = 1$ nF. The output voltage of proposed VCM, without external control voltage, corresponding to a 50% duty cycle is shown in Fig. 7.4 (a). The resulting frequency of oscillation for the chosen component values is obtained as 347.2 KHz. Simulation results for three different values of V_C namely 0.8 V, 1.5 V and - 2.0 V are shown in Fig. 7.4 (b)–(d) respectively and corresponding frequencies of oscillation are obtained as 310 KHz, 215 KHz and 114.4 KHz respectively. It is evident from Fig. 7.4 that the output frequency and duty cycle can be controlled using V_C. It may be noted from (7.7) and (7.8) that the frequency of the output waveform can be tuned by (i) varying control voltage V_C and (ii) changing R_3 and /or C_1

while keeping V_C constant. Tuning curves of the proposed VCM with V_C are shown in Fig. 7.5. Tuning with V_C for different values of C_1 shown in Fig.7.5 (a) whereas, Fig. 7.5 (b) shows tuning with V_C for different R_3 values. It can be observed from Fig. 7.5 that the output frequency reduces with increasing magnitude of V_C. The variation of frequency with C_1 has been depicted in Fig. 7.6 (a) and Fig. 7.6 (b) shows the variation of frequency with R_3 while keeping V_C as a parameter. Figure 7.6 clearly shows that for a fixed value of V_C an increase in C_1 or R_3 results in reduced output frequency. These observations corroborate with the theoretical propositions.

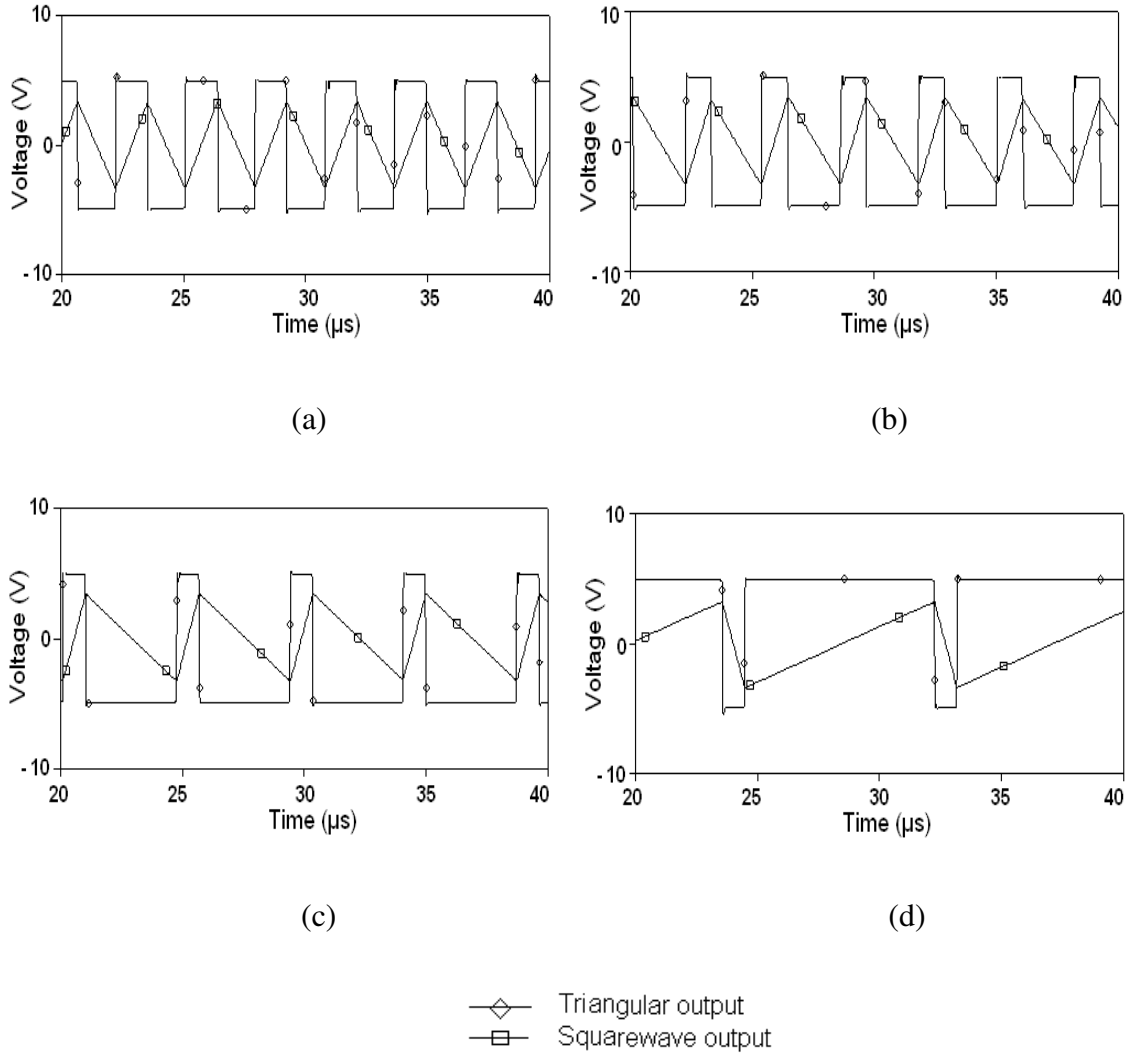
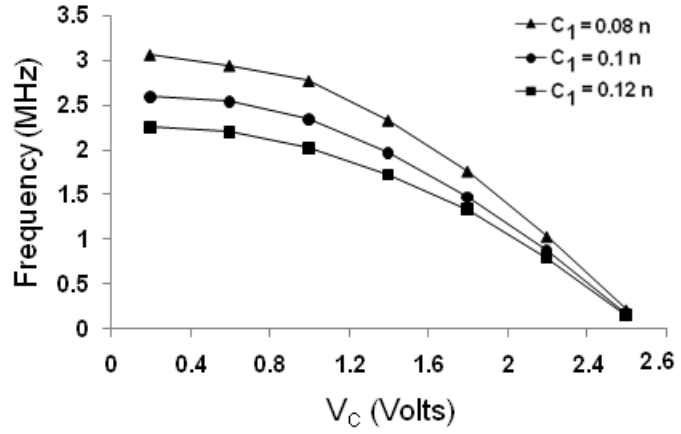
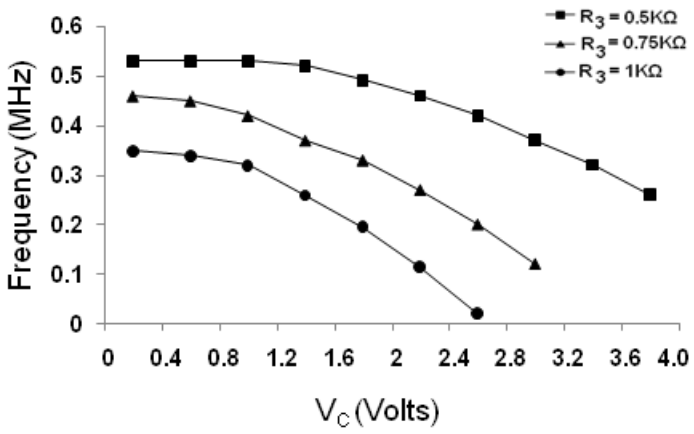


Fig.7.4 Simulated output of VCM for (a) $V_C = 0$ V (b) $V_C = 0.8$ V (c) $V_C = 1.5$ V (d) $V_C = -2$ V



(a)



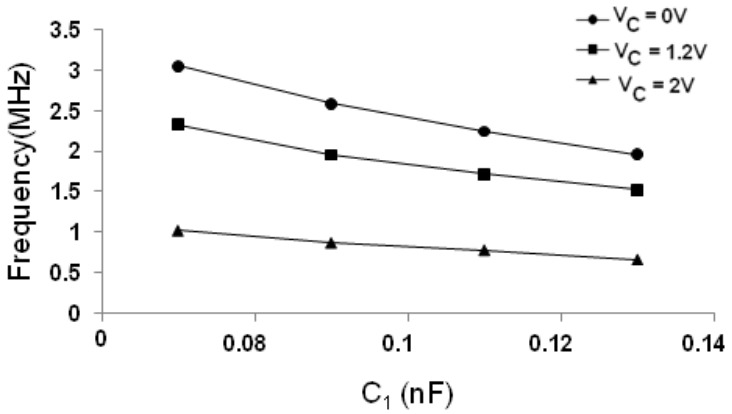
(b)

Fig.7.5 Tuning curves of proposed VCM (a) with C_1 as a parameter.

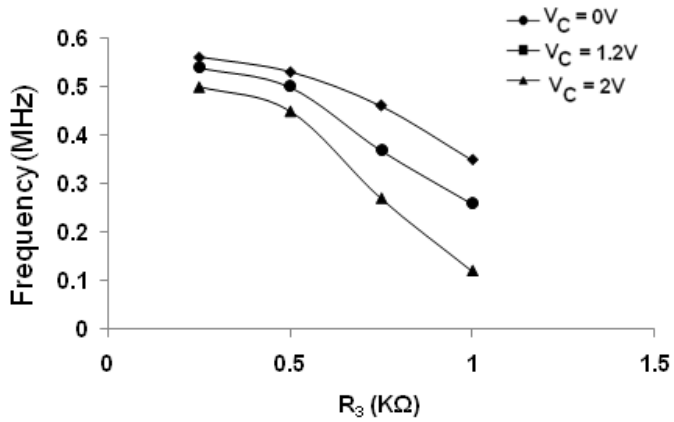
(b) with R_3 as a parameter.

The workability of VCM circuit is also established through experimental results. Component values are chosen as $R_1 = R_2 = 470\ \Omega$, $R_3 = 680\ \Omega$, $R_4 = 750\ \Omega$ and $C_1 = 1$ nF for all experimental outputs. Experimental output of the proposed circuit, without control voltage, is shown in Fig 7.7(a) whereas the output for V_C values of 2 V and – 2 V are shown in Fig. 7.7(b) and (c) respectively. Comparison between the theoretical; simulated and the experimentally observed frequency of oscillations is shown in Fig. 7.8. It is observed that the deviation between the calculated and the simulated frequencies becomes prominent at higher frequencies as the time taken by the OTRA to change its output level becomes comparable to

T_{ON} and T_{OFF} at higher frequencies. It is observed that the frequencies up to approximately 3 MHz are possible to achieve with these circuits with suitable component choices. Although, high frequencies are achievable however a trade-off to be made between high frequency and accuracy as the gap between the predicted theoretical frequency and the simulated frequency in the simulations becomes larger with the increasing frequencies.

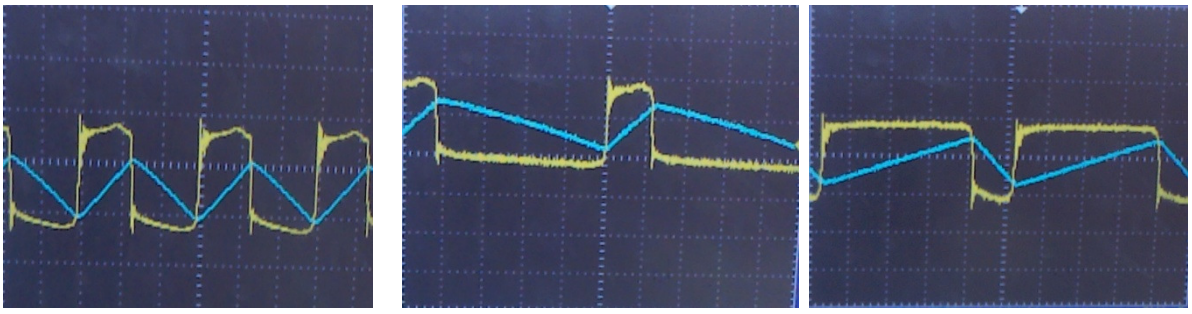


(a)



(b)

Fig. 7.6 Frequency variation curves (a) with C_1 (b) with R_3.



(a) (b) (c)

Fig. 7.7 Experimental results for different values of V_C. (a) V_C = 0 V. (b) V_C = 2.0 V. (c) V_C = - 2.0 V.

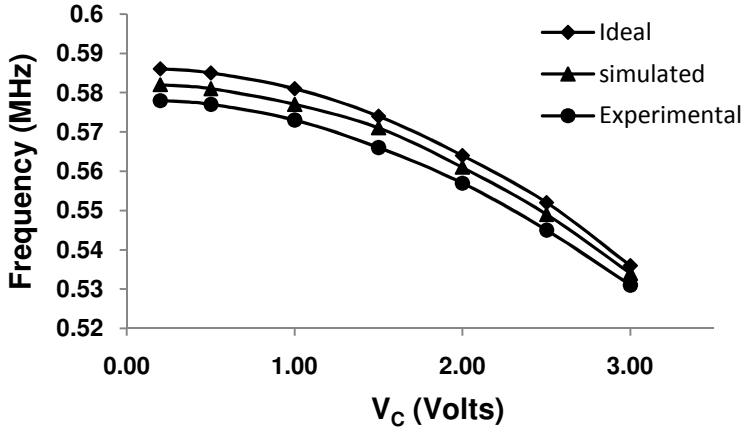


Fig. 7.8 Comparison Curve

7.2.4 Compound Pulse Frequency and Width Modulator

As an application example of proposed VCM circuit, a modulator circuit suitable for moderate distance transmission is presented in this section. In application areas like broadband and local area network, there is a definite need of transmitting both analog and digital signals over short and medium distances. Optical fibres are the ideal transmission media choice for transmitting these multiplexed signals. However the modulation and multiplexing methods play important role in realizing a high performance bandwidth (BW) efficient system. Analog modulation techniques despite being simple and BW efficient

cannot provide required signal to noise ratio (SNR) performance when used in optical communication. The digital modulation techniques, provide the required SNR performance, but, suffer from system complexity and bandwidth overheads. Pulse time modulation (PTM) is an alternate modulation scheme, in which one of the parameters associated with pulse train such as frequency, width or position is modulated to carry information. This scheme is suitable for moderate distance transmission as it offers much improved noise performance when compared to analog modulation while utilizing sufficiently lesser BW than digital modulation. Further, for multiplexing more than one channel PTM can use compound multiplexing technique wherein any two parameters of the pulse train are modulated respectively by two channels. These multiplexing techniques are self synchronizing as rising and falling edges convey different channel's information.

The OTRA based compound pulse frequency and width modulator (CPFWM) designed in this section adapts the scheme outlined in [111]. The block diagram of CPFWM is shown in Fig. 7.9.

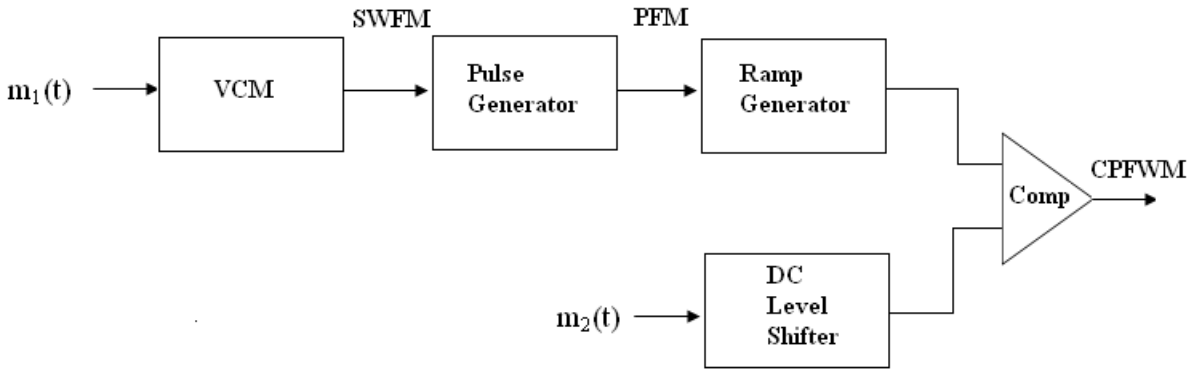


Fig. 7.9 compound pulse frequency and width modulator (CPFWM) [111].

A modulating signal $m_1(t)$ controls the VCM which produces a square wave frequency modulated (SWFM) signal at the output. This output is then passed through a differentiator to produce a train of frequency modulated pulses (PFM). This PFM output resets a ramp generator whose output is a linear ramp with variable period proportional to frequency of PFM signal which in turn is proportional to first modulating signal $m_1(t)$. The modulated ramp is then compared with a DC level shifted second modulating signal $m_2(t)$ which has

been taken as a data signal. The output of the comparator is the desired CPFWM signal which contains information about m_1 (t) and m_2 (t) in the form of modulated frequency and width respectively. In OTRA based design each block of CPFWM is implemented using OTRAs and is shown in Fig. 7.10.

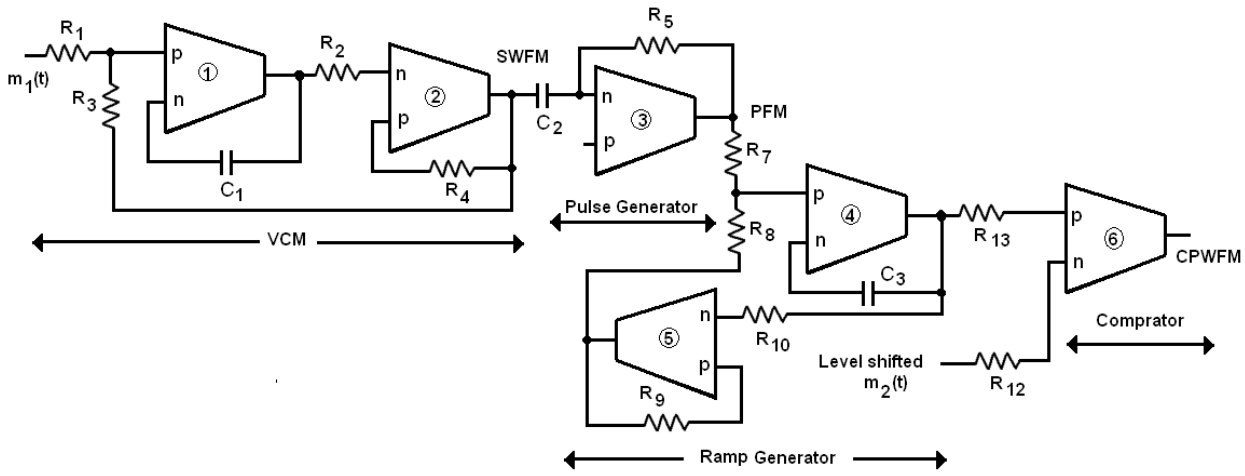


Fig. 7.10 OTRA based CPFWM.

7.2.4.1 Simulation Results

To verify the workability of this design the circuit is simulated using SPICE wherein the OTRA is implemented using CFOA as shown in Fig. 2.7. Modulating signal $m_1(t)$ is chosen as a 2 V, 10 KHz sinusoid and modulating signal m_2 (t) is a digital signal with ON and OFF periods of 1 µs and 2 µs respectively. Simulated wave shapes at the output of each block of the CPFWM are depicted in Fig. 7.11. The modulating signals $m_1(t)$ and level shifted $m_2(t)$ are shown in Fig. 7.11(a) and (b) respectively. SWFM signal at the output of VCM is shown in Fig. 7.11(c) which when passed through pulse generator produces a frequency modulated pulse train as shown in Fig. 7.11(d). The output of the frequency modulated ramp generator is shown in Fig. 7.11(e). This on comparison with DC level shifted signal m_2 (t) generates the desired CPFWM output which is both pulse frequency and width modulated signal.

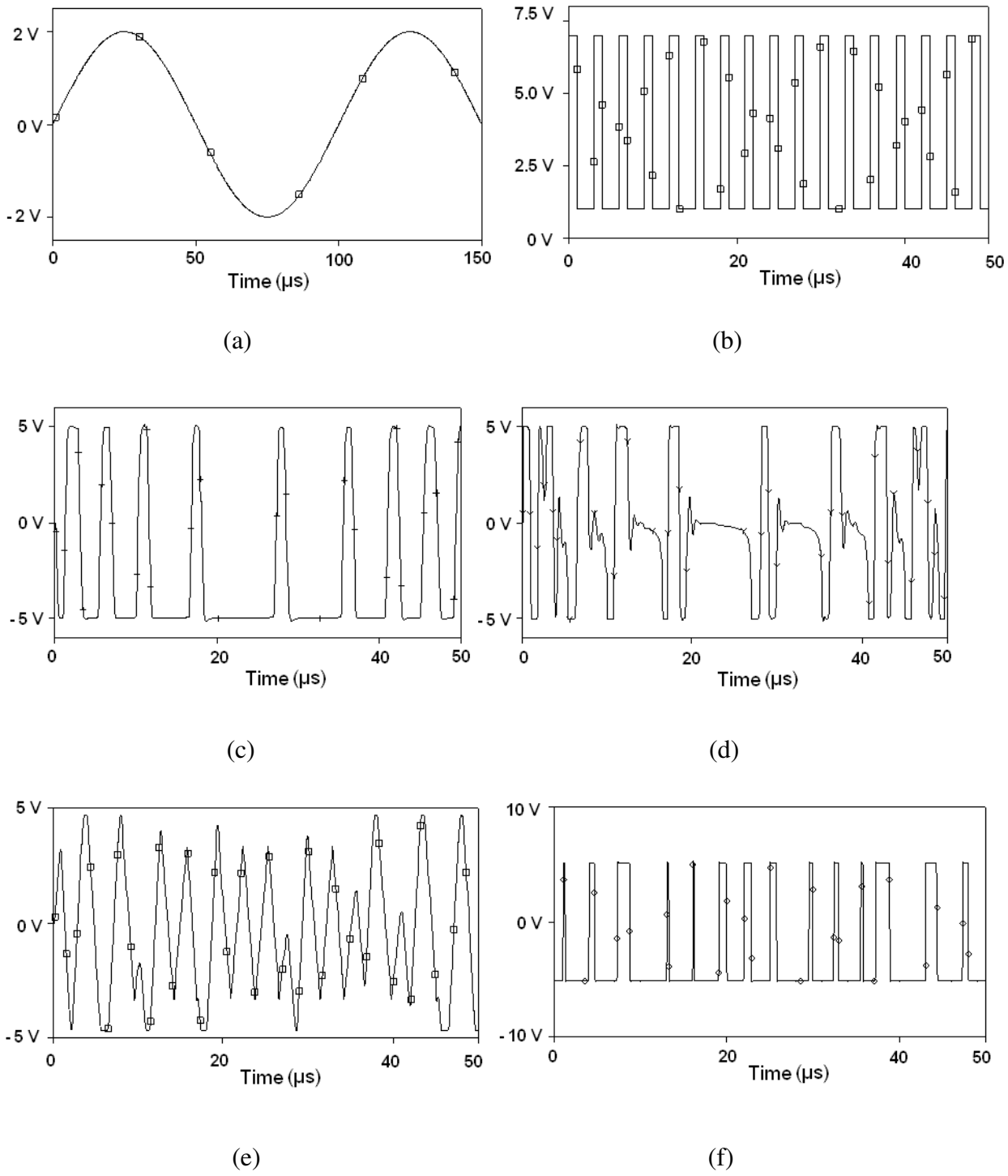


Fig. 7.11 (a) $m_1(t)$. (b) Level shifted $m_2(t)$. (c) SWFM output. (d) Output of pulse generator. (e) Output of ramp generator. (f) CPFWM output.

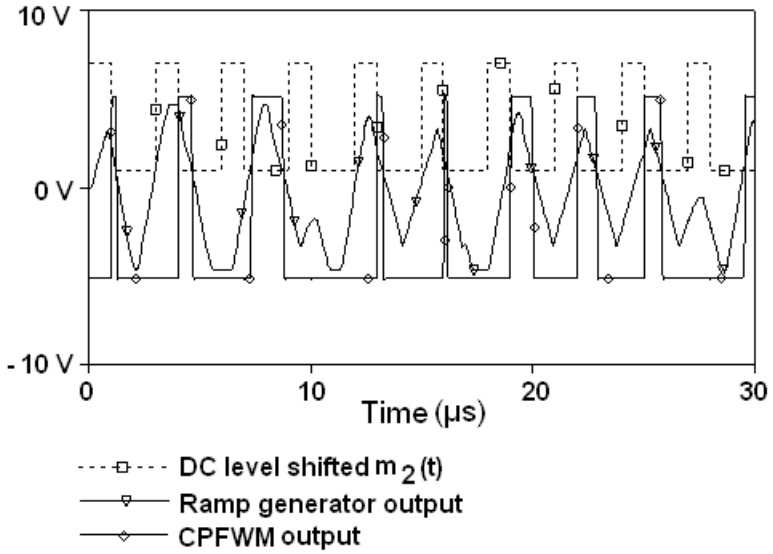


Fig. 7.12 Signal m_2 (t), ramp generator and CPFWM outputs.

Figure 7.12 depicts DC level shifted signal m_2 (t), frequency modulated ramp generator output and CPFWM output on a single scale. It clearly shows that the modulator output switches to other level of saturation as ramp output crosses level shifted m_2 (t) thus producing CPFWM output. The frequency spectrum of CPFWM output is presented in Fig. 7.13 in which X1 and X2 peaks represent the m_1(t) and m_2(t) signals respectively.

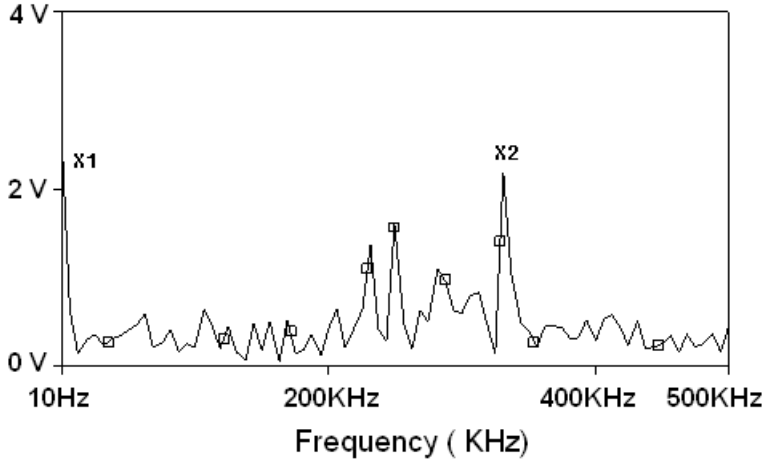


Fig.7.13 The frequency spectrum of CPFWM output.

7.3 PULSE WIDTH MODULATOR

PWMs are widely used in communication systems, DC motor speed controller, power conversion control circuits [112] – [114] and instrumentation. In pulse width modulation scheme the width of pulses of a pulse train is changed in accordance to voltage level of modulating signal. The PWM generators are available in Integrated Circuits (ICs) form; however their internal circuitry is somewhat complex and typically consists of current sources, flip-flop, comparators and analog switches [115]. Apart from these readily available ICs, the PWM circuits available in open literature can be classified as digital and analog. In analog PWMs the modulated signal is most commonly generated by comparing a modulating signal with a sawtooth or triangular waveform. Alternatively information signal can first be combined with a sawtooth or triangular waveform and this combined signal is compared with a reference level to generate PWM signal. This can be implemented using a Schmitt trigger with an RC circuit in feedback loop [95]. Extensive literature review reveals that PWMs based on this concept are available using op-amps [96], Current conveyor II (CCII) [115] and operational transconductance amplifier (OTA) [116], [117]. However, OTRA based PWM circuits have not been reported in the existing literature. Therefore an OTRA based pulse width modulator (PWM) is put forward in the following subsection.

7.3.1 Proposed Circuit

The general scheme of PWM is depicted in Fig. 7.14. The modulating signal and carrier signal are first summed up and then PWM output signal is generated by comparing the summation signal and reference level.

The proposed PWM circuit is shown in Fig. 7.15. The circuit consisting of OTRA, resistors R_F, R_L and capacitor C serves as square wave generator. Exponential voltage waveform across capacitor C serves as carrier waveform. The modulating signal $v_{in}(t)$ and the carrier wave are summed up at node p through resistor R_s. Thus the voltage across the capacitor will be summation of carrier and modulating signal and the PWM output is available at v_o.

The resistor R_F and capacitor C form a positive feedback loop. V_{sat}^{+} or V_{sat}^{-} are the two possible saturation levels of output v_0. Assuming initially that v_0 switches to saturation level V_{sat}^{+} at t = 0, as shown in Fig. 7.15. This results in charging of the capacitor present in the feedback loop and the voltage across the capacitor reaches V_{TH}, a value at which I_p, the current through p terminal becomes slightly less than the current through n terminal, I_n. As a result the output voltage switches to V_{sat}^{-} and the capacitor starts charging in the opposite direction. Now as capacitor voltage approaches V_{TL} the output once again switches back to V_{sat}^{+}.

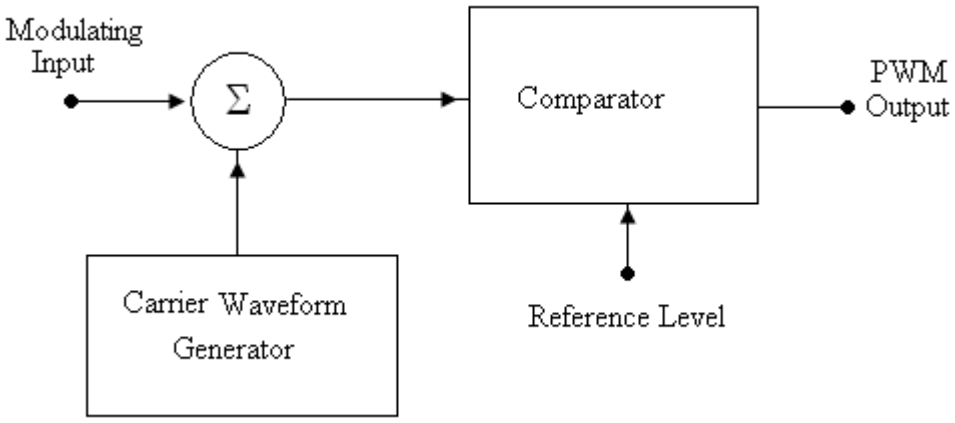


Fig. 7.14 The scheme of PWM [115].

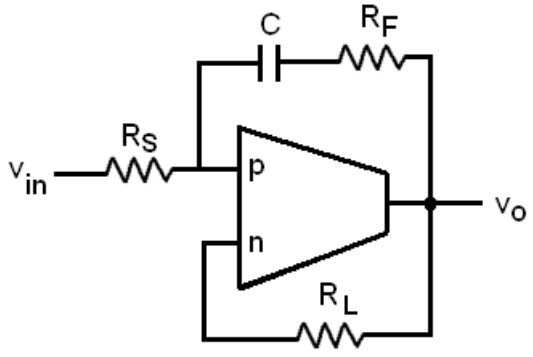


Fig. 7.15 The OTRA PWM circuit.

The V_{TH} and V_{TL} values can be obtained from the routine analysis of this PWM circuit, and are expressed as

$$V_{TH} = V_{sat}^{+}\left(1 - \frac{R_F}{R_L}\right) + v_{in}(t)\frac{R_F}{R_S} \tag{7.13}$$

$$V_{TL} = V_{sat}^{-}\left(1 - \frac{R_F}{R_L}\right) + v_{in}(t)\frac{R_F}{R_S} \tag{7.14}$$

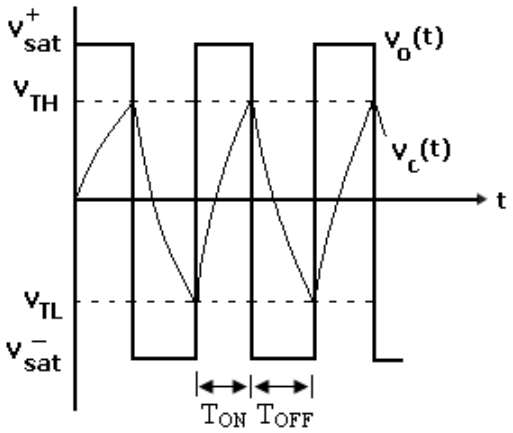


Fig. 7.16 Output of the square wave generator of Fig. 7.15.

Using (7.13) and (7.14) the on period (T_{on}) and off period (T_{off}) can be computed as

$$T_{ON} = R_F C\ ln\ \frac{\left[\frac{2R_L}{R_F} - 1\right] - \frac{v_{in}(t)R_L}{V_{sat}^{+}R_S}}{\left[1 - \frac{v_{in}(t)R_L}{V_{sat}^{+}R_S}\right]} \tag{7.15}$$

$$T_{OFF} = R_F C\ ln\ \frac{\left[\frac{2R_L}{R_F} - 1\right] - \frac{v_{in}(t)R_L}{V_{sat}^{-}R_S}}{\left[1 - \frac{v_{in}(t)R_L}{V_{sat}^{-}R_S}\right]} \tag{7.16}$$

The overall period of the modulated output is given by

$$T = T_{ON} + T_{OFF} \tag{7.17}$$

And the duty factor (D) can be computed as

$$D = \frac{T_{ON}}{T} \times 100\% \tag{7.18}$$

Thus the duty cycle of the output can be controlled with the help of modulating signal $v_{in}(t)$ as is evident from (7.15) and (7.16).

7.3.2 Nonideality Analysis

The nonidealities associated with OTRA may cause the output of the proposed PWM to deviate from ideal response. To account for this error the nonideal circuit model of OTRA as shown in Fig. 2.7 is used. The threshold limits of the output due to the nonidealities get modified to

$$V_{TH} = V_{sat}^{+}\left(1 - \frac{R_F+R_x}{R_L+R_X \| R_Z}\right) + v_{in}(t)\frac{R_F+R_x}{R_S+R_x} \tag{7.19}$$

$$V_{TL} = V_{sat}^{-}\left(1 - \frac{R_F+R_x}{R_L+R_X \| R_Z}\right) + v_{in}(t)\frac{R_F+R_x}{R_S+R_x} \tag{7.20}$$

Typically $R_z >> R_x$, therefore parallel combination of R_x and R_z can be approximated to R_x .The external resistance R_L, R_F, and R_S at the input of the OTRA should be chosen much larger than R_X. As a result (7.19) and (7.20) reduce to (7.13) and (7.14) respectively and the effect of nonidealities may practically be ignored.

7.3.3 Simulation and Experimental Results

The functionality of the proposed circuit is verified through SPICE simulations. The OTRA is realized using current feedback operational amplifiers (CFOA) IC AD844 as shown in Fig. 2.7. For all the simulations presented in this section, the component values are chosen as R_F = 20 KΩ, R_L= 70 KΩ, R_S = 80 KΩ and C = 200 pF. Figure 7.17 shows the output voltage of the PWM when modulating signal is not applied and corresponds to a 50% duty cycle. The observed output frequency is 66.7 KHz as against the calculated value of 69.7 KHz. Simulated output of pulse width modulator is shown in Fig. 7.18 for a 5 V, 1 KHz sinusoidal modulating signal. The summed up modulating and carrier signal are shown in Fig. 7.18 (a) whereas modulating signal and the PWM output are depicted in Fig. 7.18 (b).

The output of pulse width modulator for an 8 V, 2.2 KHz modulating signal and a 5 V, 40 KHz modulating signal are shown in Fig. 7.19 and Fig. 7.20 respectively.

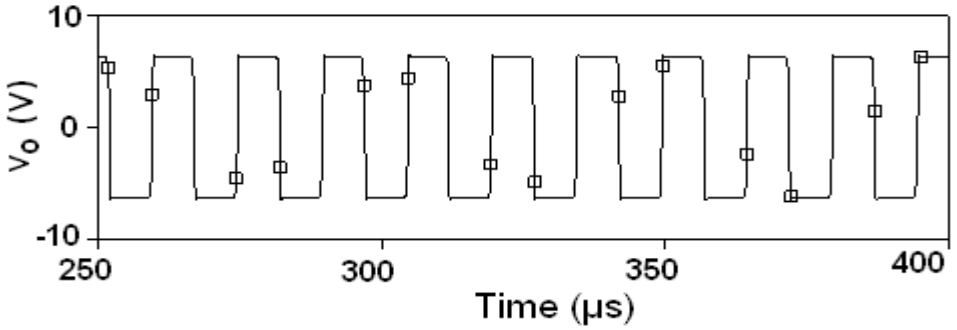
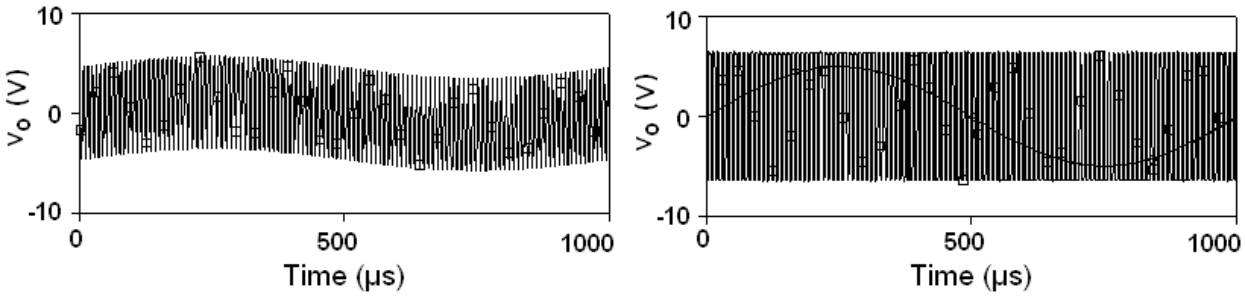
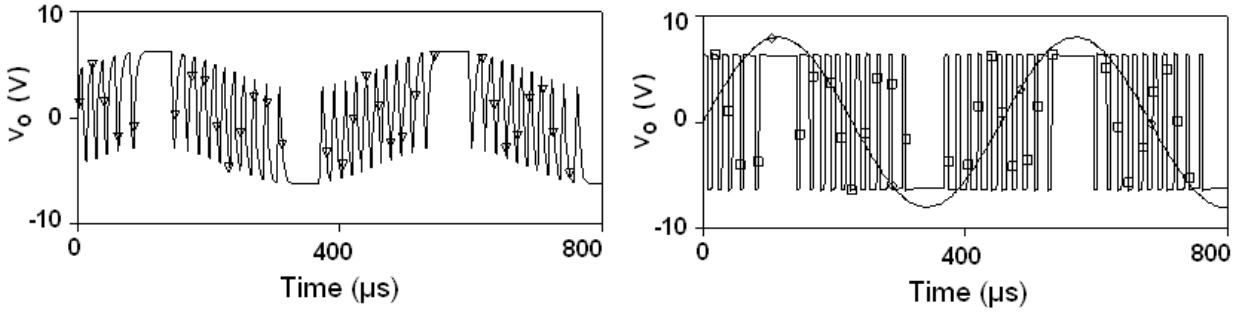


Fig. 7.17 PWM output without modulating signal.



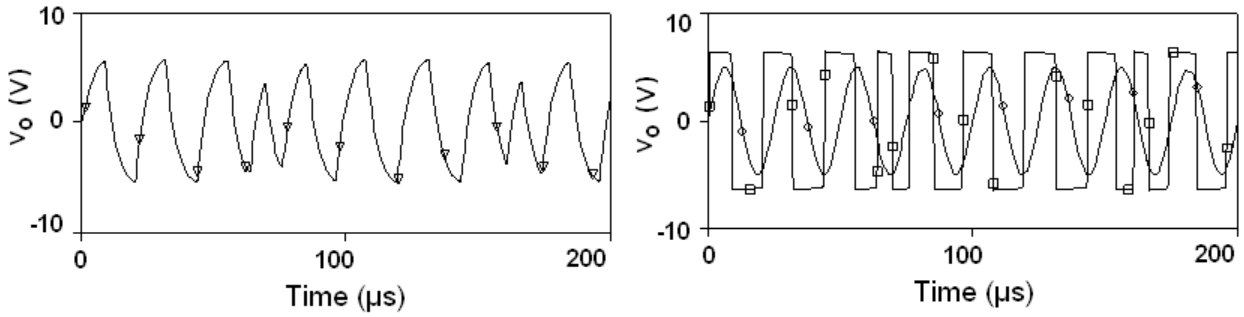
(a) (b)

Fig. 7.18 (a) Summed up modulating (5V, 1 KHz) and carrier signal.(b) Modulating and PWM output signals.



(a) (b)

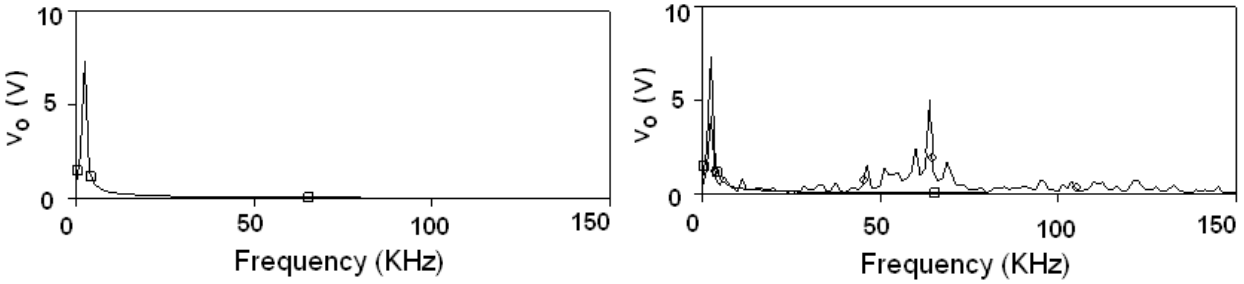
Fig. 7.19 (a) Summed up modulating (8 V, 2.2 KHz) and carrier signal. (b) Modulating and PWM output signals.



(a) (b)

Fig. 7.20 (a) Summed up modulating (5 V, 40 KHz) and carrier signal. (b) Modulating signal and PWM output signal.

Frequency spectrum of the pulse width modulator for 8 V, 2.2 KHz modulating signal is shown in Fig. 7.21 which consists of modulating component and carrier signal. Thus the modulating signal can be recovered with the help of an appropriate low pass filter.



(a) (b)

Fig. 7.21 Frequency spectrum. (a) Modulating signal. (b) Modulated signal.

Fig. 7.22 shows the variation of theoretically computed and simulated % duty factor of the modulator with the applied input signals. This shows that the two results closely match with each other.

The functionality of the proposed pulse width modulator circuits is verified through hardware also using commercial IC AD844AN to implement an OTRA. Supply voltages used are ± 5 V and component values chosen are R_F = 20 KΩ, R_L = 70 KΩ, R_S = 80 KΩ and C = 200 pF. Figure.7.23 shows typical experimental results of the circuit for two different

modulating signals. PWM output for an 8 V, 2.2 KHz modulating signal is depicted in Fig. 7.23(a). Another screen shot of oscilloscope is shown in Fig. 7.23 (b) for a high frequency modulating signal of 5 V, 40 KHz. These experimental results are in close agreement to simulated results.

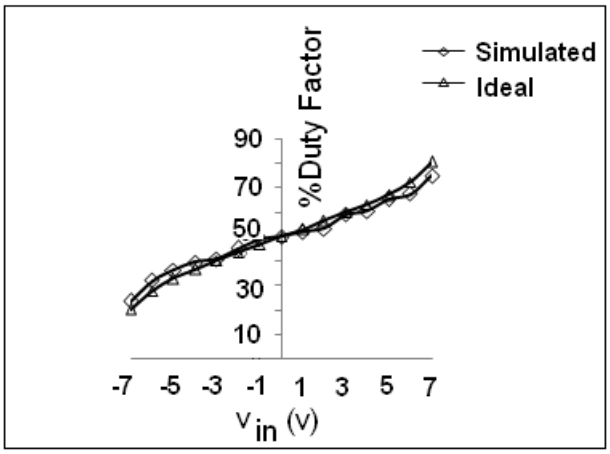


Fig. 7.22 Variation of duty factor with applied input signal.

(a) (b)

Fig. 7.23 Experimental results. (a) PWM output for an 8 V, 2.2 KHz modulating signal. (b) PWM output for a 5 V, 40 KHz modulating signal.

7.3.4 Comparison

In this section a comparison of the proposed work with the previously reported analog PWM circuits [96], [115] – [117] is presented, which are all based on the concept of comparing a modulating signal with a reference sawtooth or triangular waveform to generate PWM signal. A detailed comparison of these circuits is shown in Table 7.1. The PWM topology of [96], which is a classical opamp based design, uses same number of active and passive components as in proposed circuit. However the opamp based circuits show limited high frequency performance due to lower slew rate and constant gain-bandwidth product of the op-amps. The CCII based PWM has the advantage of generating accurate PWM signal with high operating frequencies [115] and in the OTA based PWMs the output amplitude and frequency of can be independently/electronically tuned [116]. Despite these advantages the circuits proposed in [115] – [117] suffer a drawback of using excessive number of active elements. OTA based PWM presented in [117] used derivative method for PWM generation. In derivative method the duty cycle of PWM signal depends on a differentiated result of the modulating signal. This method is not suitable for applications where the changes in modulating signal are rare, such as in power converters [116]. The proposed circuit is simpler as compared to the topologies of [115] – [117], since it uses the exponential voltage waveform across the capacitor of the square wave generator as carrier wave and hence does not require additional circuitry, needed for triangular/ sawtooth waves. Though being a non linear signal the exponential carrier wave yields relatively inaccurate PWM signal at lower carrier frequencies as compared to the triangular/saw tooth wave, yet one can trade off accuracy for simplicity depending upon the application. Additionally, the input terminals of OTRA being virtually grounded the proposed circuit is free from parasitic effects.

7.4 ANALOG MULTIPLIER

In analog-signal processing need often arises for a circuit that takes two analog inputs and produces an output proportional to their product and is known as analog multiplier. A multiplier that accepts inputs of either polarity and preserves the correct polarity relationship at the output is referred to as a four quadrant multiplier. A two quadrant multiplier puts a

constraint that one of input signals must be unipolar whereas a one quadrant multiplier requires both inputs to be unipolar. A number of circuits are reported in literature relating to analog multipliers [118] – [129]. Circuits presented in [118] – [123] are based on Gilbert multiplier [129] whereas the other class of the circuits [124] – [128] is implemented using active analog blocks such as operational transconductance amplifier [124], differential difference current conveyors [125], current feedback amplifiers [126], current-controlled current conveyor [127] and current difference buffered amplifier [128]. No OTRA based analog multiplier circuit is available in open literature and prompted the design of OTRA based multiplier.

Table 7.1: Comparison between the proposed and the previously reported work.

Ref.	No. of Active Components	No. of passive components	Carrier signal Type	Electronic Tunability
[96]	Single OpAmp	Single capacitor, Three resistors	Exponential	No
[115]	Single CC-II , Two Opamps	Single capacitor, Three resistors	Triangular	No
[116]	(i) Two OTAs, an inverter and a MOS switch (ii) Four OTAs and an inverter	(i) Single capacitor, Single resistor (ii) Single capacitor, Single resistor	(i)Sawtooth (ii)Triangular	Yes Yes
[117]	Three OTAs	Single capacitor, Two resistors	Triangular	Yes
Proposed	Single OTRA	Single Capacitor, Three resistors	Exponential	No

7.4.1 Proposed Circuit

The proposed circuit is a single OTRA based four quadrant analog multiplier, which does not use any external passive components and hence is suitable for integration. Figure 7.24 shows OTRA based multiplier structure. The transistor M_1, M_2, M_3, and M_4 are matched transistors and operate in the linear region. The voltages v_1 and v_2 represent small signals, whereas V_{C1}, V_{C2} and V_{DC} are the bias voltages. OTRA inputs keep the sources of the two transistors M_1, M_2 virtually grounded. The drain current for the MOS transistor operating in triode region [95] is given by

$$I_D = K_n \frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS} \tag{7.21}$$

where K_n is process transconductance, W and L respectively represent the channel width and length of the of the MOSFET. The other terms have their usual meaning. Using (7.21) the currents through p and n terminals of OTRA i.e. i_p and i_n respectively, can be expressed as

$$i_p = K_n \frac{W}{L}\left((V_{DC} + v_1) - V_T) - \frac{v_2}{2}\right) v_2 \quad + K_n \frac{W}{L}\left((V_{C1} - V_T) - \frac{v_o}{2}\right) v_o \tag{7.22}$$

$$i_n = K_n \frac{W}{L}\left((V_{DC} - V_T) - \frac{v_2}{2}\right) v_2 + K_n \frac{W}{L}\left((V_{C2} - V_T) - \frac{v_0}{2}\right) v_0 \tag{7.23}$$

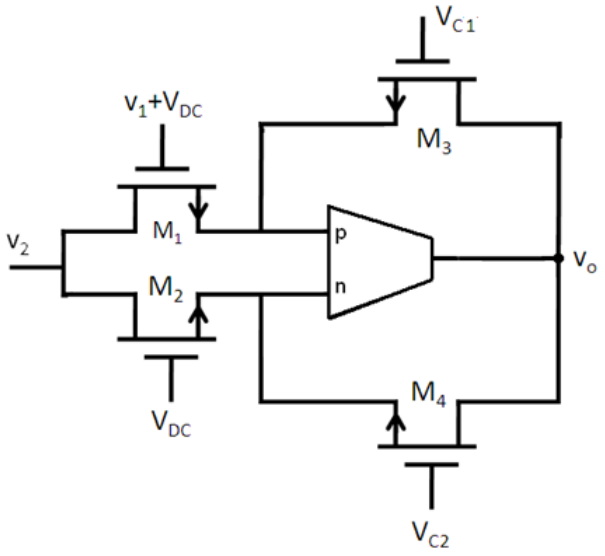


Fig. 7.24 Proposed OTRA based multiplier structure.

As R_m approaches infinity the input currents are forced to be equal resulting in

$$v_o = {}^{v_1 v_2}/_{(V_{C2}-V_{C1})} = K\, v_1 v_2 \tag{7.24}$$

where K is proportionality constant and is the inverse of difference of gate voltages of M_3 and M_4.

7.4.2 Implementation Scheme to Superimpose a Small Signal on DC Bias

As can be seen from the Fig. 7.24 the gate voltage of M_1 is (V_{DC} + v_1) which is a small signal superimposed over a dc bias. This voltage addition can be implemented using scheme proposed in Fig. 7.25 wherein v_x is small signal voltage and V_C is bias voltage. If M_{P1} and M_{P2} are matched transistors and are operating in saturation then their drain currents will be equal resulting in

$$\frac{1}{2}\, K_p \frac{W}{L} ((v - V_C) - V_{tp})^2 = \frac{1}{2}\, K_p \frac{W}{L} ((v_x - v) - V_{tp})^2 \tag{7.25}$$

which gives

$$v = \frac{(V_C + v_x)}{2} \tag{7.26}$$

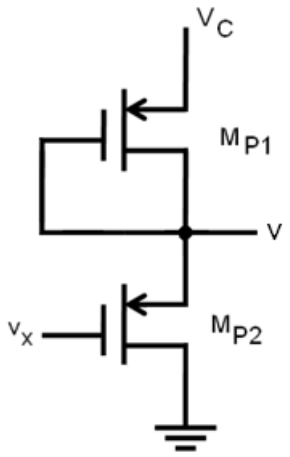


Fig. 7.25 Scheme for implementing an ac superimposed on dc bias.

The voltage given by (7.26) can be used as the gate voltage for transistor M_1 of Fig. 7.24. Similarly gate voltage for transistor M_2 can be obtained from (7.26) by making $v_x = 0$. Substituting these values of gate voltages in (7.24) the output of the multiplier gets modified to

$$v_o = K' v_1 v_2 \quad \text{where} \quad K' = \frac{K}{2} \tag{7.27}$$

7.4.3 MOS Based Multiplier Structure

The complete MOS based multiplier structure is depicted in Fig. 7.26 which incorporates the voltage addition scheme of Fig. 7.25. As the transistors M_1, M_2, M_3 and M_4 need to operate in the triode region for proper operation of the multiplier so the following conditions should be satisfied.

$$((V_C + v_1)/2 - V_{tn}) > v_2 \tag{7.28}$$

$$((V_C/2) - V_{tn}) > v_2 \tag{7.29}$$

$$(V_{C1} - V_{tn}) > v_o \tag{7.30}$$

$$(V_{C2} - V_{tn}) > v_o \tag{7.31}$$

Now using equations (7.26) along with (7.28) - (7.31) the conditions for input signals v_1 and v_2, can be computed as

$$V_{tp} < v_1 < (V_C + 2V_{tp}) \tag{7.32}$$

$$v_2 < \frac{(V_C + v_1)}{2} - V_{tn} \tag{7.33}$$

These equations suggest that the dynamic input range of the multiplier is controlled by V_C.

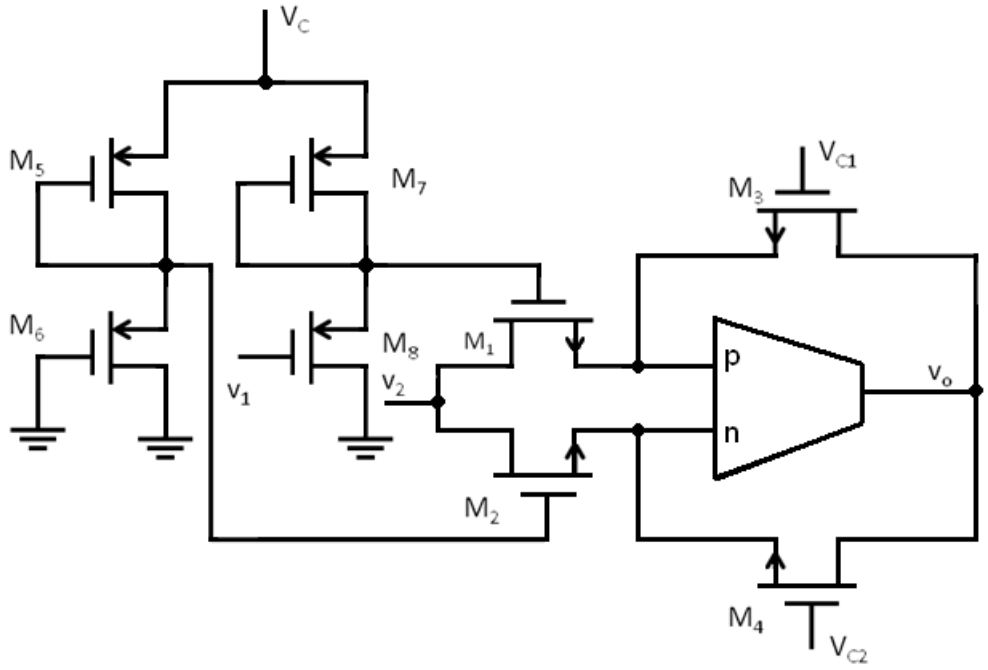


Fig. 7.26 Complete multiplier circuit.

7. 4. 4 Nonideality Analysis

In this section the effect of transistor capacitances and finite trans-resistance gain of OTRA on multiplier is considered and compensation is employed for high frequency applications. While deriving the multiplier output expressed by (7.24) the effect of transistor capacitances was ignored. However for high frequency applications this effect needs to be considered. Due to transistor capacitances the currents i_p given by (7.21) modifies and can be written as

$$i_p = K_n \frac{W}{L}\left((V_{DC} + \mathrm{v}_1) - V_T) - \frac{v_2}{2}\right) v_2 + K_n \frac{W}{L}\left((V_{C1} - V_T) - \frac{v_0}{2}\right) v_0 + v_1 s C_{gs1} \qquad (7.34)$$

where C_{gs1} is gate to source capacitance of M_1, however the current i_n remains same as (7.22). The effect of C_{gs1} can be compensated by adding a MOSFET M_9, operating in triode region, at the inverting terminal of OTRA as shown in Fig. 7.27. The effective gate to source capacitance of M_9 should be equal to C_{gs1}. The modified i_n can be expressed as

$$i_n = K_n \frac{W}{L}\left((V_{DC} - V_T) - \frac{v_2}{2}\right) v_2 + K_n \frac{W}{L}\left((V_{C2} - V_T) - \frac{v_0}{2}\right) v_0 + v_1 s C_{gs1} \qquad (7.35)$$

The third term in (7.35) results due to gate to source capacitance of M_9.

Using i_p and i_n given by (7.34) and (7.35) and the finite value of R_m given by (2.7), the output of multiplier v_o can be evaluated as

$$v_o = \frac{{v_1 v_2}/{(V_{C2}-V_{C1})}}{1+{sC_p}/{(K_n \frac{W}{L}(V_{C2}-V_{C1}))}} \tag{7.36}$$

and hence the 3 dB bandwidth of the multiplier can be expressed as

$$BW = \frac{K_n \frac{W}{L}(V_{C2}-V_{C1})}{C_p} \tag{7.37}$$

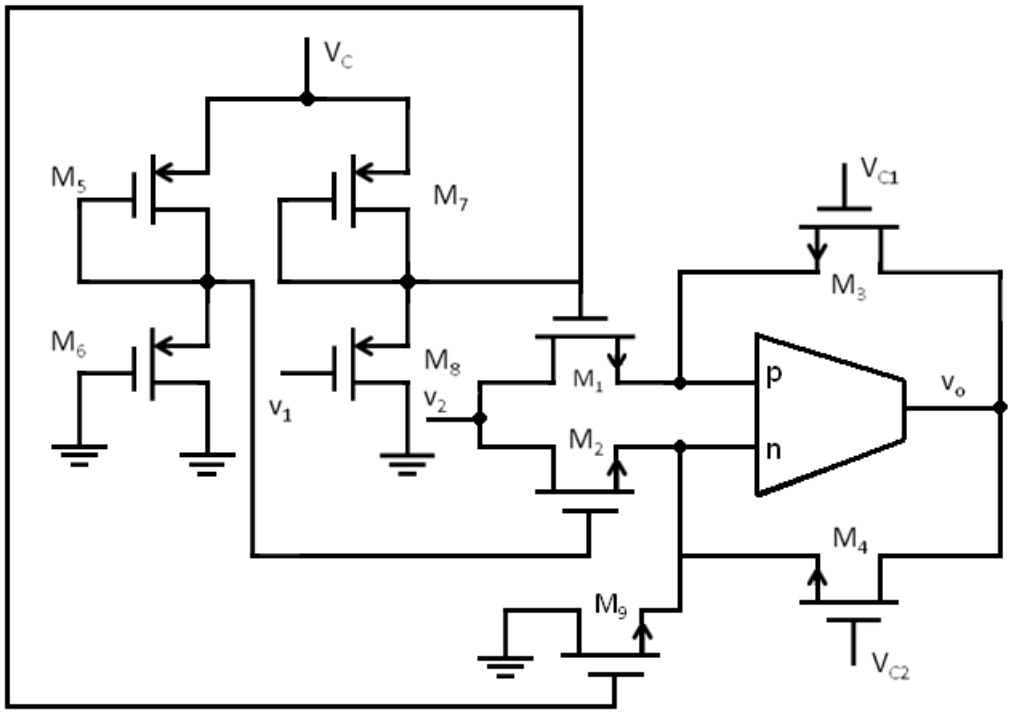


Fig.7.27 Complete multiplier circuit with C_{gs} compensation of Transistor M_1.

7.4.5 Simulation Results

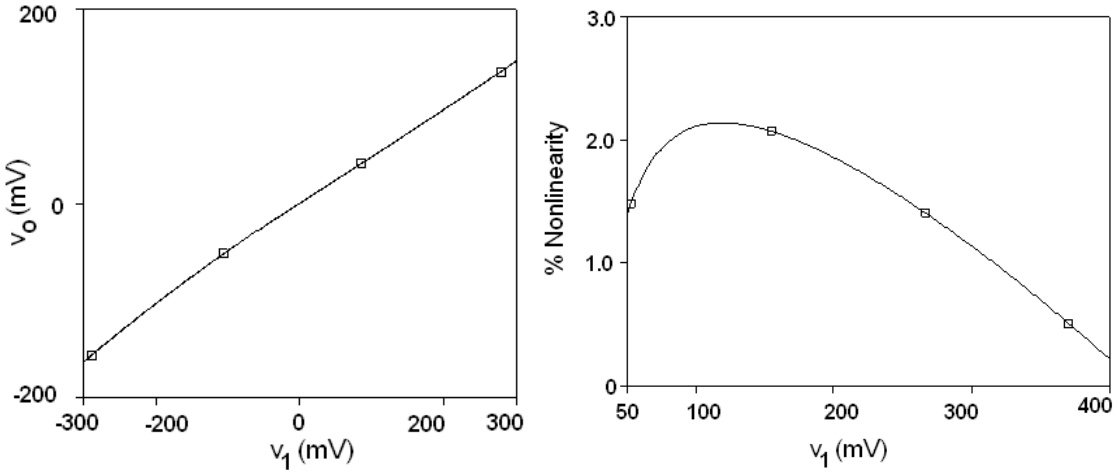
The functionality of the proposed multiplier is verified through SPICE simulation using

0.5µm CMOS parameters provided by MOSIS (AGILENT). The CMOS OTRA schematic shown in Fig. 2.9 is used for simulation. All the transistors M_1-M_8 were used with equal aspect ratios having W/L = 1µm/0.5µm. Control voltage are taken as V_C = 2 V, V_{C1} = 1 V and V_{C2} = 1.25 V.

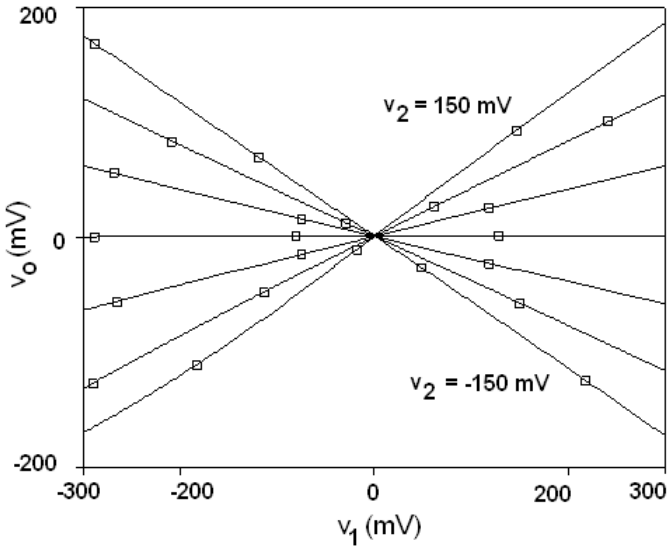
Multiplier performance is generally specified in terms of accuracy and nonlinearity. Accuracy represents the maximum deviation of the actual output from the ideal value whereas the nonlinearity represents the maximum output deviation from the best-fit straight line for the case where one input is kept fixed and the other is varied from end to end. Both accuracy and nonlinearity are expressed as a percentage of full-scale output.

Figure 7.28 depicts the DC transfer characteristics of the proposed multiplier. The transfer curve v_o versus v_1, with v_2 kept constant at 250 mV, is shown in Fig. 7.28 (a). It may be noted that v_o varies almost linearly with v_1. The nonlinearity curve, representing maximum percent deviation from ideal transfer characteristic, as a function of input voltage v_1 is shown in Fig. 7.28 (b). It is observed that the maximum nonlinearity over the entire input range does not exceed 2.05%. In Fig. 7.28 (c) v_o is plotted with respect to v_1 for different values of v_2. Voltage v_1 is swept from -300 mV to 300 mV while v_2 is varied from -150 mV to 150 mV in steps of 50 mV. It shows that the proposed circuit is a four quadrant multiplier.

Multiplier dynamics are specified in terms of the small signal 3dB BW and the 1% absolute-error BW [103] representing the frequency where the output magnitude starts deviate from its low frequency value by 1%. The frequency response of the proposed multiplier is shown in Fig. 7.29 for which v_1 is kept constant at 200 mV whereas v_2 is taken as an ac source having amplitude 250 mV. The 3dB bandwidth is found to be 8 MHz and the 1% absolute-error BW is observed to be 0.98 MHz.



(a) (b)



(c)

Fig. 7.28 DC transfer characteristic. (a) v_o versus v_1 with $v_2 = 250$ mV. (b) Nonlinearity curve with $v_2 = 250$ mV. (c) v_o versus v_1 when v_2 is varied from -150 mV to 150 mV.

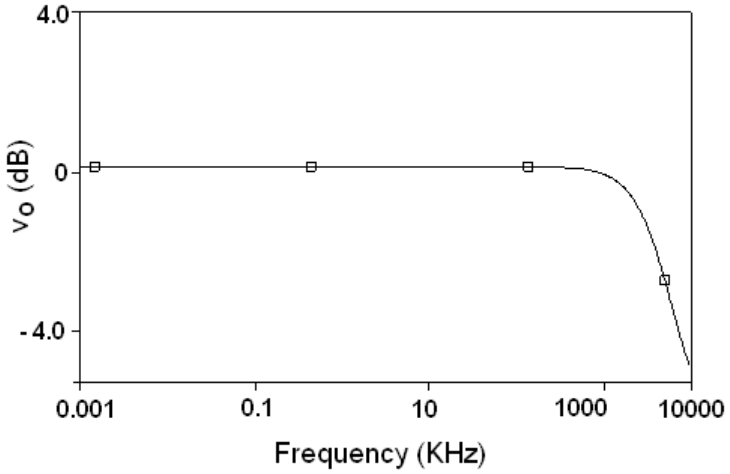


Fig. 7.29 AC characteristic of the proposed multiplier.

Figure 7.30 show the total harmonic distortion (% THD) as a function of input signal amplitude when a constant dc voltage (250 mV) is applied to v_2 while a 1 KHz sinusoidal signal is applied to v_1 with varying amplitude. It can be seen that the maximum % THD remains under 0.2% for the entire input range. Total power consumption of the proposed multiplier is 0.83 mW when $v_1 = v_2 = 0$ V, $V_C = 2$ V, $V_{C1} = 1$ V and $V_{C2} = 1.25$ V.

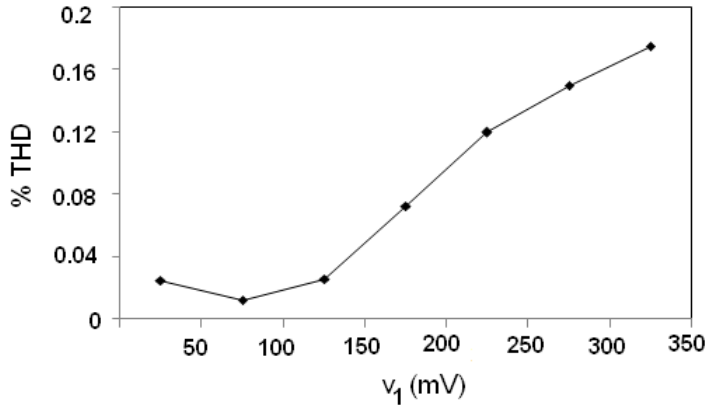


Fig. 7.30 THD versus input signal amplitude.

7.4.6 Applications

The analog multiplier provides the basis for variety of other analog operations, such as true RMS conversion, analog division, square and square root computation, various forms of linearization and voltage controlled amplification, filtering and oscillation [103]. Therefore it finds extensive applications in the area of analog computing, signal processing, communication and measurement. In this section two applications of the proposed analog multiplier along with simulation results to verify their workability, are presented.

7.4.6.1 Squarer

The proposed multiplier can be used as a squarer circuit if $v_1 = v_2 = v_{in}$. The output of the multiplier is given by

$$v_o = K' v_{in}^2 \tag{7.38}$$

The square transfer characteristics is shown Fig. 7.31 wherein v_{in} is varied from - 400 mV to 400 mV.

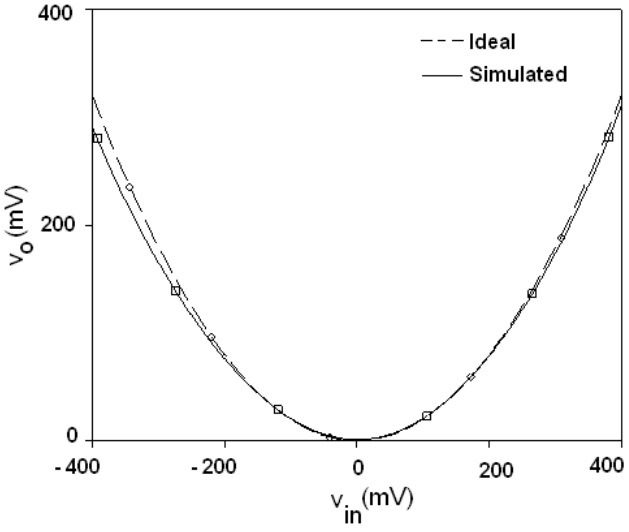


Fig. 7.31 Squarer transfer characteristics.

If an input ac signal $v_{in} = A\cos\omega_1 t$ is applied then using the trigonometric identity the output can be computed as

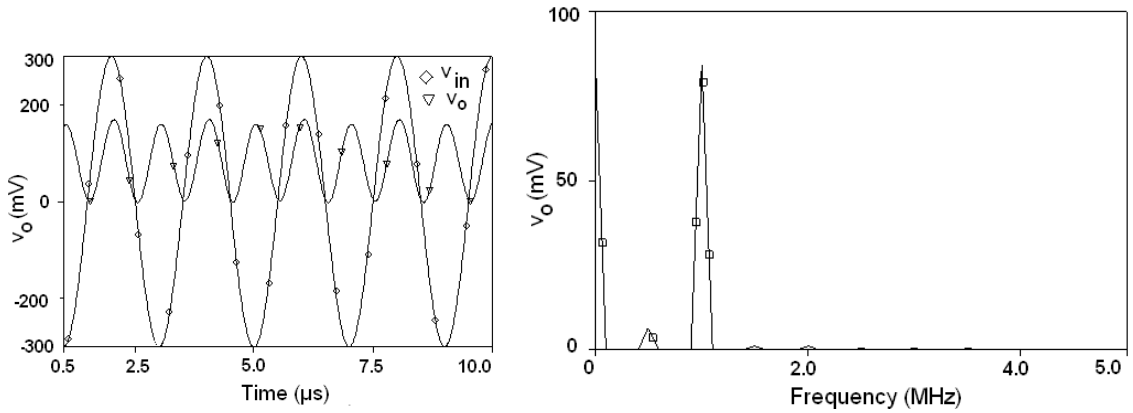
$$v_o = \frac{A^2}{2}(1 + \cos 2\omega_1 t) \tag{7.39}$$

which represents a sinusoid having double as frequency than the input signal with a dc value of $\frac{A^2}{2}$. If a 300 mV, 500 KHz sinusoid is applied as input the theoretical output of the proposed multiplier can be computed as

$$v_o = 90\ (1 + \cos 2\Pi \text{ x } 10^6 t\ ) \tag{7.40}$$

This output represents a 1 MHz sinusoid to which a 90 mV dc component is added.

The observed output of the squarer for an input signal of 300 mV, 500 KHz sinusoid, is shown in Fig. 7.32. The squared output is shown in Fig. 7.32(a) and the spectrum of squared output is shown in Fig. 7.32(b). From the spectrum it can be seen that the simulated output is exactly in tune with the theoretical proposition.



(a) (b)

Fig. 7.32 Output of the square (a) Time domain response. (b) Frequency spectrum.

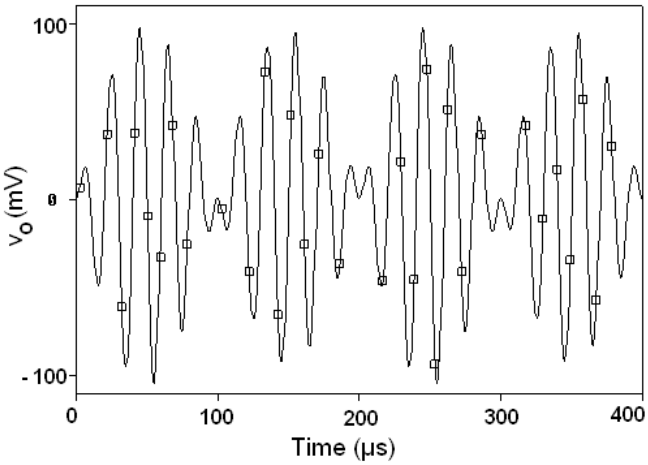
7.4.6.2 Amplitude Modulator

The proposed multiplier, being a four quadrant multiplier, can be used as an amplitude modulator (AM). Considering input signals as $v_1 = A_1 \cos \omega_1 t$ and $v_2 = A_2 \cos \omega_2 t$ then the product of these two signals can be expressed as

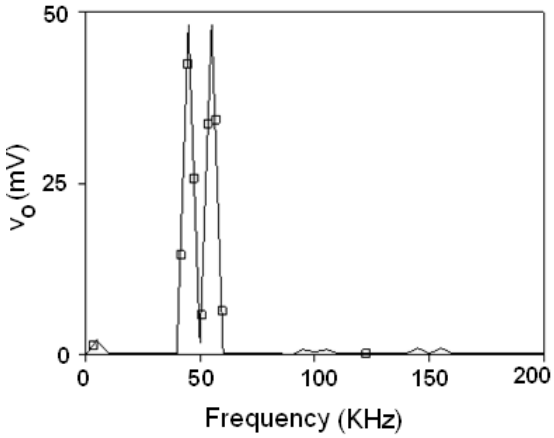
$$v_o = \frac{A_1 A_2}{2}\ (\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t) \tag{7.41}$$

indicating that the output consists of two components with frequencies equal to the difference and sum of the input frequencies and represents the output of a balanced modulator.

To verify the modulation function a 200 mV, 5 KHz signal is multiplied by 250 mV, 50 KHz signal. Figure 7.33 shows the output of the proposed multiplier confirming the modulation function. The time domain response of the multiplier is shown in Fig. 7.33(a) and Fig. 7.33(b) displays the frequency spectrum which represents two components of frequencies 45 KHz and 55 KHz respectively both having an amplitude of 100 mV and are in agreement with the theoretical values.



(a)



(b)

Fig. 7.33 Multiplication of two sinusoids (a) Time domain response.

(b) Frequency spectrum.

7.5 CONCLUDING REMARKS

This chapter deals with few nonlinear applications of OTRA. Following circuits are proposed in this chapter which find widespread applications in communication, instrumentation and measurement, and control system design

1. Voltage controlled multivibrator
2. Pulse width modulator
3. Analog multiplier

The proposed VCM circuit has a wide range of frequency of oscillation which can be controlled through an external voltage. It can also be used as a general square/triangular waveform generator by grounding the control voltage terminal. It provides adjustable amplitude of the triangular wave signal and also provides adjustable sensitivity (Hz per Volts). As an application of the proposed VCM, a modulator circuit based on PTM scheme is presented which uses compound multiplexing technique for multiplexing two channels, carrying analog and digital information respectively. It can be used for moderate distance communication such as in local area networks.

The pulse width modulator presented, uses a simple modulation scheme wherein the modulating signal is combined with an exponential carrier waveform and compared with a reference. The exponential carrier wave being a non linear signal yields relatively inaccurate PWM signal at lower carrier frequencies as compared to the triangular/saw tooth wave. However, this scheme uses minimum number of active and passive components and one can trade off accuracy for simplicity depending upon the application.

The workabilty of VCM and PWM circuits is verified through SPICE simulations and experimental results using IC AD844 for OTRA realization and the results are found in close agreement with theoretical results.

A four quadrant analog multiplier, proposed as the concluding application, does not require any passive element thus making it suitable for integration. Various performance parameters are evaluated through SPICE simulations and are found in close agreement to theoretical predictions. Its application as a squarer and an amplitude modulator are also discussed and their workability is verified through simulations.

CHAPTER – 8
CONCLUSION

This thesis presents design and synthesis of signal processing and generating circuits using OTRA, a current mode analog building block of relatively recent origin. In this chapter a summary of the major conclusions of the work reported in various chapters of the thesis are presented.

8.1 SUMMARY OF WORK PRESENTED IN THIS THESIS

The introductory chapter presents a short note on evolution of current mode signal processing, its advantages and a brief review of various current mode analog building blocks that emerged for analog electronic design. A review of earlier work on signal processing and generation circuits using OTRA has also been presented in this chapter.

A detailed study of the OTRA has been presented in chapter 2. The ideal OTRA, its nullor based model, the effect of nonidealities on ideal circuit model and the OTRA realizations available in literature have been reviewed. The CMOS OTRA implementation presented in [30] is discussed and characterized using SPICE to validate its functionality. This OTRA configuration is used to verify the workability of the circuit structures proposed in this study. Few basic circuit applications of the OTRA such as voltage amplifiers, adder, subtractor, and integrator, which can be readily used as plug-in modules wherever needed, are also described. In OTRA based circuits, how passive resistor can be implemented using MOSFETs is discussed in concluding section which not only makes circuits suitable from integration viewpoint but also introduces electronic tunability in the circuit. Chapters 3 to 7 present the research contribution of this study.

In chapter 3 design of lossy and lossless active grounded inductance simulator topologies have been dealt with. A brief review of existing literature in the area has been presented first followed by the design of a lossy inductance topology based on single OTRA, two lossless inductor topologies using two OTRAs and yet another lossless inductor based on a single OTRA. The proposed lossy inductor can realize ± L parallel with R. It uses a single OTRA, two resistors and two virtually grounded capacitors. The two OTRA based topologies presented use five resistors and one capacitor apart from OTRAs and for both the topologies the inductance value can be controlled independent of condition of realization. The next

design structure discussed is a new grounded simulated inductor topology based on single OTRA, three resistors and two capacitors. It provides non interactive control between inductance value and realizabilty condition. For the proposed topologies effect of nonidealities associated with OTRA has also been taken into consideration. The workability of all these structures is verified through SPICE simulations. The lossy inductor topology is simulated using CFOA based realization of OTRA wheras the lossless inductor topologies are simulated using the CMOS implementation of the OTRA. To demonstrate the practical use of the proposed topologies few applications have been realized using component replacement technique. The theoretical propositions are also verified through experimental results wherein OTRA is realized using ICs AD844.

Realization of OTRA based biquadratic and higher order filters is presented in chapter 4. A brief record of earlier work dealing with the filter design using OTRA is also presented. The work reported in this chapter has been classified as single and multiamplifier filters. For the applications having power consumption as an important design constraint, single active element based (SAB) filter is a useful choice. In this work, single OTRA based two biquadratic filter topologies are presented which can realize the LP, HP, and BP filter functions by appropriate admittance selection. The first configuration is based on Sallen Key approach wheareas the second configuration is based on multiple feedback topology. High Q_0 realization with moderate component spread is possible through first topology which also provides independent adjustment of ω_0 and Q_0. SABs are less versatile and more sensitive to parameter changes when compared to multiamplifier filters.This led to design of multiamplifier configurations which are further categorised as biquads and higher-order filters. Review of earlier work suggested that no OTRA based structure that provided all five standard responses simultaneously was available. To fill this gap a biquadratic universal filter, with simultaneous five outputs, is developed. It exhibits the feature of orthogonal controllability of ω_0 and Q_0. The chapter is concluded with wave method based higher order filter design using OTRA. It uses wave equivalents for different passive elements which can be readily substituted in higher order resistively terminated LC ladder to realize a filter. The proposed universal biquad and wave active filter configurations are made fully integrated by implementing the resistors using matched transistors operating in linear region. The

resistance value may be adjusted by appropriate choice of gate voltages thereby making filter parameters electronically tunable. All proposed structures are validated through SPICE simulations. The simulated results closely follow the theoretical propositions.The filter configurations are also analyzed in the light of nonidealities of OTRA.

Chapter 5 deals with sinusoidal signal generation. General scheme of sinusoidal signal generation is discussed in the chapter followed by design description of proposed sinusoidal oscillators. Design of a single phase, a third order quadrature phase and three multiphase sinusoidal oscillators is presented in this chapter. The proposed single phase sinusoidal oscillator uses two OTRAs three resistors and three capacitors. This oscillator circuit provides independent control on frequency and condition of oscillation which are made electronically tunable through MOS implemented resistors. It also supports equal component usage; a preferred choice from integrated circuit implementation viewpoint. The third order quadrature oscillator is designed using two OTRAs four resistors and three capacitors. Frequency and condition of oscillation can be made orthogonal through iterative control and are electronically tunable. The MSO circuits find wide applications in communication, instrumentation and control. Out of three proposed MSOs the first structure utilizes ‘n’ inverting LPFs to produce ‘n’ odd-phase oscillations which are equally spaced in phase and are of equal amplitude. The second configuration uses ‘n’ noninverting LPFs and an inverting amplifier having $n \geq 3$, to produce ‘n’ odd or even phase oscillations equally spaced in phase. The third circuit is based on a concept of using an SRCO followed by a phase shifter network. The phase shifter circuit uses (n-1) OTRA based inverting/noninverting LPF blocks to give a total of ‘n’ oscillations. An Automatic Gain Control circuitry (AGC) has also been implemented which helps in the stabilization of the signal amplitude. To analyze the behaviour of the proposed circuits in presence of the parasitics of the OTRA, nonideality analysis is performed for all the proposed structures. Workability of all oscillator circuits is verified through SPICE simulations. The simulated results closely follow the theoretical propositions. The workability of MSO circuits is established experimentally also.

Chapter 6 deals with instrumentation and conrol applications of OTRA. OTRA based transimpedance instrumentation amplifier (TIA) is proposed as first application. For amplification of signals from current-source transducers TIA is a preferred choice and due to

its very nature of current input and voltage output OTRA is the most suitable ABB for TIM signal processing wherein the current input can be directly processed without conversion to voltage signal. The proposed TIA shows a high 3 dB bandwith which is independent of gain. Its functionality is verified through SPICE simulatios. The simulated 3 dB frequency of the amplifier is 10 MHz and is independent of gain. The proposed TIA exhibits a CMRR magnitude of 64.5dB and bandwidth of 10 KHz, independent of gain. The noise performance analysis of the proposed TIA suggests that it also exhibits a high signal-to-noise ratio. The workability of the proposed TIA is tested experimentally also.

In succession, design of feedback controllers based on proportional-integral-derivative (PID) algorithm is presented. Feedback controllers are most popularly used in the process industries, to control various processes satisfactorily, with proper tuning of controller parameters. The proposed analog controllers namely proportional (P), proportional derivative (PD), proportional integral (PI) and proportional derivative and integral (PID) controllers have orthogonally tunable proportional, integral and derivative constants. Functionality of the proposed circuits is verified through SPICE simulations. The effect of the proposed controllers on step response of a second order system is analyzed and their performance is evaluated on the basis of various process parameters. It is observed that PID controller enhances transient as well as steady state response of the system which is in tune with the well established result of control theory.

The effect of OTRA parasitics, on the performance of all proposed applications in this chapter, is also analyzed. For high-frequency applications, compensation methods are employed, to account for the error introduced due to parasitics. All the applications are made fully integrated by implementing the resistors using MOS transistors operating in non-saturation region. This also facilitated electronic tuning of the circuit parameters.

In Chapter 7 nonlinear applications of OTRA are proposed. Realization a VCM circuit having a wide range of frequency of oscillation which can be controlled through an external voltage is presented first. It can provide adjustable amplitude of the triangular wave signal and also provides adjustable sensitivity (Hz per Volts). This circuit can also be used as a general square/triangular waveform generator by grounding the control voltage terminal and

is capable of operating approximately up to 3MHz. An application of the proposed VCM as a compound pulse frequency and width modulator (CPFWM) is illustrated. It uses compound multiplexing technique for multiplexing two channels, carrying analog and digital information respectively. This can be a suitable choice for moderate distance communication such as in local area networks.

Another modulator circuit using a simple modulation scheme is presented next. This scheme uses minimum number of active and passive components wherein the modulating signal is combined with an exponential carrier waveform and compared with a reference. The exponential carrier wave being a non linear signal yields relatively inaccurate PWM signal at lower carrier frequencies as compared to the triangular/saw tooth wave, however, one can trade off accuracy for simplicity depending upon the application.

A four quadrant analog multiplier which can be used for various analog operations such as true RMS conversion, analog division, square and square root computation, voltage controlled amplification, filtering and oscillation is also presented. It does not require any passive element and is suitable for integration. Its application as a squarer and an amplitude modulator is also discussed.

Various performance parameters for analog multiplier are evaluated through SPICE simulations using 0.5 μm CMOS process parameters from MOSIS (AGILENT) and are found in close agreement to theoretical predictions. Workability of the proposed VCM and PWM applications is verified through SPICE simulations using CFOA based realization of OTRA and experimental results are also included.

8.2 AUTHOR'S ENDING NOTE

The current-mode approach represents an efficient way to realize CMOS circuits and has made a great impact on IC design. It claims to provide advantages such as higher BW and slew rates, lower power consumption, improved linearity, and smaller chip area, in contrast to their voltage–mode counterparts. The complexity of a circuit determines its performance. Current-mode circuits are often less complex than the voltage-mode circuits they are compared to [130], thus explaining the performance differences.

It is also worth mentioning, that advantages offered by CM circuits are often achieved at the cost of higher distortion and gain variation [130]. Also, there are applications in which the VM techniques are more approporiate. For example to realize the voltage buffers with rail to rail input and output swing, and to fulfill low input offset current requirement, voltage-mode op-amp is a preferred choice [5] . Thus conglomoration of two domains would be a further step in evolution of analog IC design where, the research findings of CM techniques may give valuable insight to voltage-mode designers and the techniques like Miller feedback, offset compensation used in classical voltage-mode design [130], can also be used in circuits that process current signals.

Emerged as an alternative analog design approach, the current-mode techniqe has broadened the horizon of analog IC design by giving way to a number of active building blocks for analog signal processing. These blocks may serve one or more of the variety of specific requirements imposed on the analog subsystems working in various operating modes [4]. This study explored circuit applications of one such active element, OTRA, which is most suitable for transimpedace mode applications. It is expected that this study would serve as a ready reckoner of available information on OTRA and circuits built using the block.

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