DESIGN AND IMPLEMENTATION OF LOW-POWER AND HIGH-SPEED VOLTAGE LEVEL SHIFTER

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DECLARATION

I, Harshit Kumar (23/C&I/02), solemnly affirm that the dissertation titled, "**Design and Implementation of Low-Power and High-Speed Voltage Level Shifter**", is the product of my independent and original research work guided by **Dr. Chaudhry Indra Kumar** and **Dr. Ashish Rajeshwar Kulkarni**, Department of Electrical Engineering, Delhi Technological University, Delhi.

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Harshit Kumar

23/C&I/02

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

Signature of Supervisor

Signature of external examiner

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CERTIFICATE

This is to certify that the dissertation titled " **Design and Implementation of Low-Power and High-Speed Voltage Level Shifter**" submitted by Harshit Kumar (23/C&I/02) in partial fulfilment of the requirements for the degree of Master of Technology in "**Control and Instrumentation**" has been completed under our supervision.

The dissertation embodies original research work conducted by the candidate under our guidance. The results obtained and interpretations made in this dissertation are based on the work carried out by the student. The methods, experiments, and conclusions presented reflect substantial research and development in the area of Voltage Level Shifter.

We certify that the student has successfully completed all research-related tasks, including literature review, system design, simulation, data analysis, and result validation, in accordance with the university's standards. We have reviewed the entire dissertation and found it satisfactory for submission.

We also confirm that, to the best of our knowledge, the work reported herein is free from any form of plagiarism and adheres to the ethical standards prescribed by the institution.

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ABSTRACT

Voltage Level Shifters (VLS) are critical blocks in modern integrated circuits, especially in systems-on-chip (SoCs) where several voltage domains exist, for the best power efficiency and performance. With scaling technology and the trend toward lower supply voltages, the need for efficient, reliable, and high-speed voltage level shifters has been enormous. Voltage level shifter circuits enable signal communication between voltage level differing blocks without compromising signal integrity or adding excessive power loss. This thesis starts with an extensive overview of the current voltage level shifter architectures, ranging from the conventional voltage level shifter to the wilson current mirror voltage level shifter and other prominent topologies. Such architectures are thoroughly evaluated. The designs of the voltage level shifters proposed in this thesis are optimized to cater to various use cases, from energy-limited devices like battery-wearables to high-speed systems. The simulation results indicate that the power dissipation and delay of propagation of the designed circuits are minimal, striking a reasonable balance between speed and power efficiency in a practical sense. The results highlight the flexibility of the design to modern mixed-voltage systems and offer valuable insights into effective voltage level shifter circuit design.

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LIST OF ABBREVIATIONS

The abbreviations utilized in this thesis are included below

CMOS	Complementary Metal-Oxide-Semiconductor
SOC	System on Chip
IC	Integrated Circuits
V_{DDH}	High Supply Voltage
V_{DDL}	Low Supply Voltage
VLS	Voltage Level Shifter
WCMVLS	Wilson Current Mirror Voltage Level Shifter
ROWCMLS	Reflected Output based Wilson Current Mirror Voltage Level Shifter
HPVLS	High Performance Voltage Level Shifter
SSVLS	Single Supply Voltage Level Shifter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
VLSP	Proposed Voltage Level Shifter

CHAPTER 1.

INTRODUCTION

1.1. Introduction

The continuous advancement of semiconductor technology has made it possible to shrink transistor sizes and fit billions of transistors within a single chip. This has made way for new frontiers of power efficiency, functionality, and performance in integrated circuits (ICs). With the growing complexity of modern digital systems, they increasingly employ a variety of supply voltage levels to achieve maximum power and performance [1]. For instance, a processor's central processing unit (CPU) might be operated at a reduced voltage to conserve power, but the input/output (I/O) peripherals might be operated at an increased voltage to maintain legacy system and peripheral compatibility with external equipment [2].

However, communication among subcircuits operating at another voltage poses a huge design challenge: reliable and safe voltage translation. That is where voltage level shifters come into action. A voltage level shifter is a circuit that translates a digital signal between two voltage domains without degrading the quality of the signal or destroying the components of the circuit. The circuits are particularly required in System-on-Chip (SoC) designs [3], where various power-consuming subsystems need to exchange information with one another. A voltage domain is, say, a collection of circuit elements in a chip running at the same supply voltage. The domains are electrically decoupled as much as their power supply is concerned but may be logically coupled to form a harmonious system. Voltage compatibility was never a primary concern in traditional digital design, as circuits typically were being operated off of one supply voltage. But with growing power constraints—particularly in battery-powered systems such as smartphones, tablets, and Internet of Things (IoT) devices—voltage domains grew widespread. Voltage level shifters have thus taken center stage in digital circuit design [4].

In the progress of semiconductor technology, power efficiency has become a key design parameter alongside performance. The drive for low-power devices, particularly in mobile and battery-driven systems, has created a proliferation of circuits that operate at varying voltage levels. This creates a basic challenge: guaranteeing the communication between such circuits. This is where voltage level shifters help [5].

A voltage level shifter (or a level translator) is a critical circuit that translates logic levels between two voltage domains [6]. Such components are pervasive in today's electronic systems, especially in System-on-Chip (SoC) designs, where heterogeneous modules might be operating at different voltage levels. Without voltage level shifters, heterogeneous systems with different voltage requirements would be impractical and unreliable to integrate.

Although voltage level shifters address the issue of incompatibility in voltage levels, their design is not straightforward. Most traditional level shifter architectures are plagued by high propagation delay, increased static and dynamic power consumption, and decreasing performance at lower voltages [7]. This poses a bottleneck in high-speed and low-power applications, where each nanosecond and microwatt matters.

This chapter discusses the overall role of voltage level shifters, including their significance, and need in existing and future integrated circuit (IC) design.

1.2. Importance of Voltage Level Shifter

The main function of a voltage level shifter is to safeguard low-voltage devices from exposure to higher voltage signals that may be beyond their maximum voltage tolerance. For instance, if a 5V microcontroller's signal is fed directly to a 3.3V sensor without level conversion, it may either destroy the sensor or result in inconsistent performance. A 1.8V device's signal may also not be recognized as a valid high-level input by a 3.3V or 5V device [8], causing communication failure. Level shifters work around this by changing the levels of the signals up or down so that all devices receive signals within their voltage tolerance.

Voltage level shifters become a necessity when working with mixed-voltage designs wherein modules operate on varying supply voltages and must communicate with each other. Conventional level shifter circuits suffer from drawbacks such as high propagation delay, high power consumption, and weak driving capability, particularly at low voltages [9]. Thus, a low-power and high-speed design is critical in high-end applications like mobile phones, Internet of Things (IoT), and medical sensors.

In Short, Voltage level shifters are significant because:

- Power Management: Enable low-power and high-performance blocks to converse.

- Interoperability: Enables devices to converse with each other at varied logic levels, enabling the inclusion of mixed components.
- Data Integrity: Prevent signal degradation or misinterpretation.
- Device Protection: Protects from voltage mismatch damage by preventing components from operating outside of their proper voltage ranges.
- System Integration: Enable IP blocks belonging to multiple vendors or to an alternate technology node to be utilized.

1.3. Need for voltage level shifter

The two of the most important design parameters in the semiconductor world today are power and speed. In embedded and mobile systems, power savings inherently extend the battery life and decrease thermal emissions. At the same time, high-speed operation is vital to satisfy real-time processing demands and provide good system responsiveness.

For the case of voltage level shifters, low power is a critical requirement to keep leakage currents low, particularly when circuits spend lengthy periods in an idle state. Dynamic power proportional to switching frequency and voltage also needs to be kept as low as possible without compromising on performance. Simultaneously, having fast transition times ensures signal integrity is not compromised and timing requirements are satisfied between clock domains.

1.4. Design Challenges

Designing and applying voltage level shifters poses a number of technical and practical difficulties. The difficulties arise from considerations of signal integrity, timing, voltage compatibility, and power—particularly in mixed-signal or high-speed systems [10].

- Signal Speed and Propagation Delay

Level shifters present some latency while transferring signals across voltage domains. When the speed is low, this latency is insignificant, but in high-speed digital systems (e.g., SPI or memory buses), even slight latency can result in timing mismatches. This may result in data corruption, synchronization issues, or even total communication failure.

- Signal Integrity and Voltage Compatibility

Certain level shifter devices do not function with extremely minimal-voltage domains such as 0.9V or 0.5V or may have narrow threshold margins. Operational failure happens when the high and low voltage levels of an input signal remain undefined because the system fails to interpret the signal levels accurately. This may lead to erroneous logic level interpretation leads to system malfunctions alongside communication breakdowns.

- Power Consumption

Certain active level shifter circuits dissipate large amounts of static or dynamic power, particularly when repeatedly converting rapid or high-frequency signals. It is a very important issue in battery-powered or low-power embedded systems such as IoT gadgets or wearables.

- Directionality and Control

Although unidirectional level shifters are straightforward, bidirectional level shifters are complicated. In communications such as I²C where direction changes dynamically, mismanagement of direction can lead to bus contention. This may destroy components or seize communication, particularly when both parties attempt to drive the line in opposing directions.

- PCB Layout and Component Choice

Poor PCB layout—such as excessive traces, poor decoupling, or improper grounding—can cause noise and cross-talk. In addition, the use of incorrect pull-up resistor values or incorrect MOSFETs could result in inaccurate operation. Leads to unreliable or unstable voltage switching, especially in close or high-speed designs.

The following table summarizes challenges highlighted above.

Table 1.1: Challenges in Designing a VLS circuit

Challenge	Description	Impact
Propagation Delay	Time lag introduced by shifting	Timing mismatches
Signal Integrity	Noise, overshoot, glitches	Data corruption
Voltage Compatibility	Incorrect logic interpretation	Functional errors
Power Consumption	High dynamic/static loss	Reduced battery life
PCB Layout	Poor routing and design	Unstable signals

1.5. Applications

Voltage level shifters are used in various fields of electronics like:

- Microcontroller Interfacing: Interfacing microcontrollers with other peripherals of varying voltages.
- Communication: Facilitating communication between devices having different logic levels to provide correct signal translation.
- Sensor Integration: Interfacing sensors with varying voltages to microcontrollers or processors.
- Signal Conditioning: Conditioning signals for compatibility between the components in order to have effective data transfer.

Briefly, they allow the integration of new low-voltage components into current systems, enable intercommunication between logic families, and help designers implement power and performance levels without sacrificing system integrity.

1.6. Problem Statement

Most of the conventional level shifters in high-speed designs might be hampered by increased dynamic power due to fast switching, and low-power designs might suffer from penalties with lower speed as a result of weaker drive strength and increased delays. Moreover, most traditional level shifter circuits are not optimized for use in aggressive technology scaling. Lower supply voltages cause the transistor performance to worsen, thereby creating a challenge to sustain fast switching and low leakage currents. This also makes efficient level shifter design in advanced CMOS nodes more challenging.

In order to solve these problems, this thesis presents a new voltage level shifter designs that meets the requirements. The new design is intended to be appropriate for modern applications, especially in low-power digital systems like mobile processors, wearable devices, and power-constrained embedded systems.

1.7. Thesis Organization

The content of the thesis is organized into following chapters:

- Chapter I: INTRODUCTION
- Chapter II: LITERATURE REVIEW

- Chapter III: PROPOSED VOLTAGE LEVEL SHIFTER DESIGN WITH ENHANCED POWER EFFICIENCY
- Chapter IV: PROPOSED HIGH PERFORMANCE VOLTAGE LEVEL SHIFTER DESIGN WITH SINGLE SUPPLY
- Chapter V: PROPOSED DESIGN OF VOLTAGE LEVEL SHIFTER FOR IOT APPLICATIONS
- Chapter VI: SIMULATION AND RESULTS
- Chapter VII: CONCLUSIONS AND FUTURE SCOPE

Chapter I – This chapter gives a brief introduction about Voltage Level Shifter.

Chapter II – This chapter includes the background needed for understanding the working of the VLS. Further it includes a review of the existing VLS configuration.

Chapter III – This chapter introduces the proposed Voltage Level Shifter Design with Enhanced Power Efficiency. The chapter comprise their construction, working and result.

Chapter IV – This chapter introduces the proposed Voltage Level Shifter design with single supply. The chapter comprise their construction, working and result.

Chapter V – This chapter introduces the proposed Design of Voltage Level Shifter for IOT applications. The chapter comprise their construction, working and result.

Chapter VI – All proposed designs are compared with previous designs in this chapter.

Chapter VII – Concluding remarks about the proposed designs are recorded in this section and further scope has been discussed.

CHAPTER 2.

LITERATURE REVIEW

2.1 Overview

The implementation of VLS within VLSI systems proves essential because they establish data communication between blocks with separate supply voltage requirements. Modern SoCs together with mixed-signal designs require optimized robust level shifter circuits because they fulfil two essential functions: maintaining signal integrity and minimizing power usage and preserving logical integrity.

The chapter starts with the basic concepts of MOSFET, CMOS, and Voltage level shifter. The chapter then proceeds to present different VLS topologies. Traditional level shifters, while simple, suffer from high power consumption. Newer designs incorporate dynamic and hybrid approaches to address these shortcomings. This chapter presents a comprehensive survey of existing voltage level shifter architectures. It evaluates their operational principles, performance parameters, and identifies gaps that this thesis aims to address.

2.2 Voltage Level Shifter

Voltage level shifters are simple electronic circuits or components employed to convert digital signals from one voltage level to another so that the different components, which work at various supply voltages, can communicate with each other seamlessly.

In modern electronic circuits, it is usually the case that various integrated circuits (ICs) work at different logic voltage levels of, for example, 1.2V, 1.8V, 2.5V, 3.3V, and 5V. This diversity is necessitated due to the need to increase power efficiency, reduce heat dissipation, and allow high-speed operation [11]. As such, the demand for compatibility between these devices makes it a vital design criterion, and this is where voltage level shifters come into place.

2.2.1 Operation

A voltage level shifter is a circuit that detects a digital signal at one voltage level on the input and creates the same signal at a different voltage level on the output. The logic state of the signal (HIGH or LOW) is not altered, but the absolute voltage values are adjusted to match the receiving circuit.

The process generally involves tracking the transitions of the input signal and utilizing circuit components (such as transistors or logic gates) energized by two voltages, one for each domain (say, 1.2V and 3.3V). Upon the input signal transitioning to HIGH or LOW, the level shifter internally causes the respective switching mechanism to fire off and produce an output signal at the correct voltage on the output side [12].

The steps-by-step process involved in the working is explained below:

- Voltage Sensing: The level shifter checks the input voltage through transistors or logic gates. It identifies whether the input signal is in the HIGH (logic 1) or LOW (logic 0) state depending upon threshold voltages.
- Internally, the logic state (0 or 1) of the input signal, independent of the actual voltage, is interpreted by the level shifter. That is, 1.2V is HIGH in one universe and 3.3V is HIGH in another. The logic meaning is maintained.
- Voltage Translation: Depending on the level of logic interpreted by it, the level shifter then switches the circuitry that regenerates the signal employing the output voltage supply. This output employs the proper HIGH and LOW voltages in the receiving system (e.g., 3.3V HIGH or 0V LOW).
- Signal Synchronization: In this process, attention is paid to maintaining timing and edges (rising and falling edges). Proper level shifters guarantee that the output also changes state in synchronism with the input, refraining from signal skew or delay beyond acceptable thresholds.
- Isolation and Protection: Most level shifters allow for electrical isolation between the input and output realms, which shields low-voltage devices from exposure to harmful high voltages during interfacing.

2.3 Logic Level Thresholds

The voltage level thresholds define the logic '0' and logic '1' in digital circuits. The thresholds depend on the transistor sizing, supply voltage (V_{DD}), and threshold voltage (V_{TH}). In level shifters, the input logic levels must be accurately translated to match the output domain [13].

2.4 Traditional VLS

2.4.1 Structure

Traditional VLS design is the most basic form of a voltage level shifter and is often used in low-speed applications due to its simplicity and low cost [14]. This design typically consists of a cross coupled PMOS half latch operating at V_{DDH} as shown in Fig.2.1. The design also contains a pair of complementary transistors (PMOS and NMOS) operating at V_{DDL}, arranged to create an inverter circuit. The primary function of the CMOS inverter in this context is to invert the input logic signal.

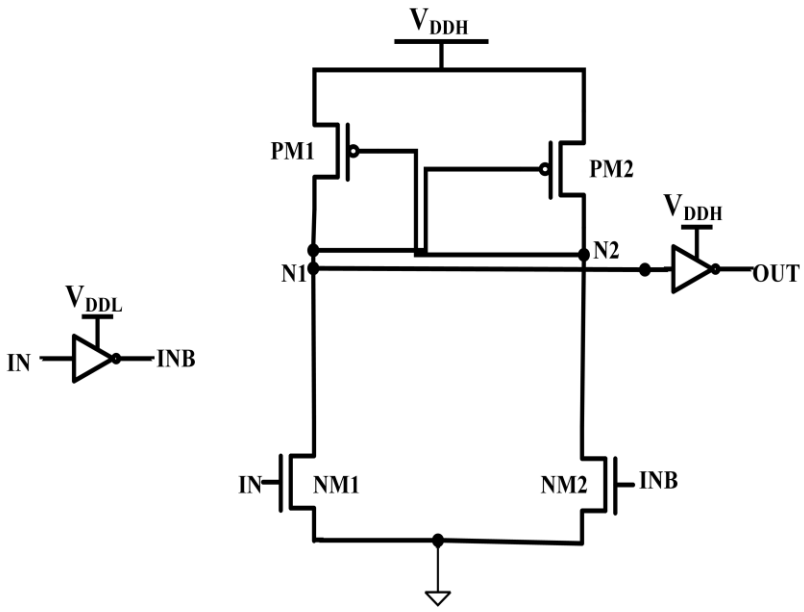

Fig. 2.1: Traditional Voltage Level Shifter Schematic

2.4.2 Working

VLS operates through the cooperation of PMOS transistors PM1 and PM2 in cross-coupled configuration with NMOS pull-down transistors NM1 and NM2.

When the input signal is high, NM1 transistor turns ON, pulling node N1 to ground and NM2 turns OFF, charging node N2. This activates the PMOS transistor of the output inverter, resulting in a high output. The node N2 charged keeps the transistor PM1 OFF.

When the input goes low, the roles of the NMOS devices switches. Now, NM1 will turn OFF and NM2 will turn ON. This results in node N1 to charge and node N2 to discharge, as a result PMOS transistors PM1 turn ON and PM2 to turn OFF, resulting in output to be low.

But there is contention at node N1 and N2 among pull-down devices running at V_{DDL} and pull-up devices running at V_{DDH} [15]. Therefore, traditional level shifter cannot work properly when value difference between V_{DDH} and V_{DDL} is great.

2.4.3 Advantages:

- Simple Architecture: The design is straightforward, which makes it easy to implement and maintain. This is especially useful for educational purposes and legacy systems.
- Compatibility: Since it's a conventional method, it is widely compatible with older circuits and can be integrated without major design changes.
- Low Power Consumption: This design is energy-light in terms of raw power draw, which can be beneficial in applications where minimizing power usage is important (e.g., battery-operated or always-on devices).

Disadvantages:

- High Delay: The circuit experiences significant delay during level shifting, making it less suitable for high-speed digital systems.
- Inefficient for Modern Needs: It does not cater to the demands of modern low-power, high-speed portable electronics.
- Poor Energy Utilization: Despite simple power needs, the overall energy per operation is high due to the delay.

2.5 Wilson Current Mirror VLS (WCMVLS)

2.5.1 Structure

The Wilson Current Mirror LS as shown in Fig.2.2 resolves the contention issue by utilising a current mirror instead of the cross-coupled structure [16]. This design facilitates the elevation of the output node to V_{DDH} in instances where the input signal is characterized as high. However, this setup does possess a significant limitation characterized by the continuous and static flow of current

through transistors NM1 and PM1 when the input remains in a high state. The Wilson Current Mirror-based Voltage Level Shifter generates its operation through the combination of low-voltage-controlled PMOS pair PM1 along with PM2 and NMOS devices NM1 and NM2. A current mirror uses a pair of transistors to generate a reference current that controls the voltage across the load, resulting in more stable and predictable output behaviour [17].

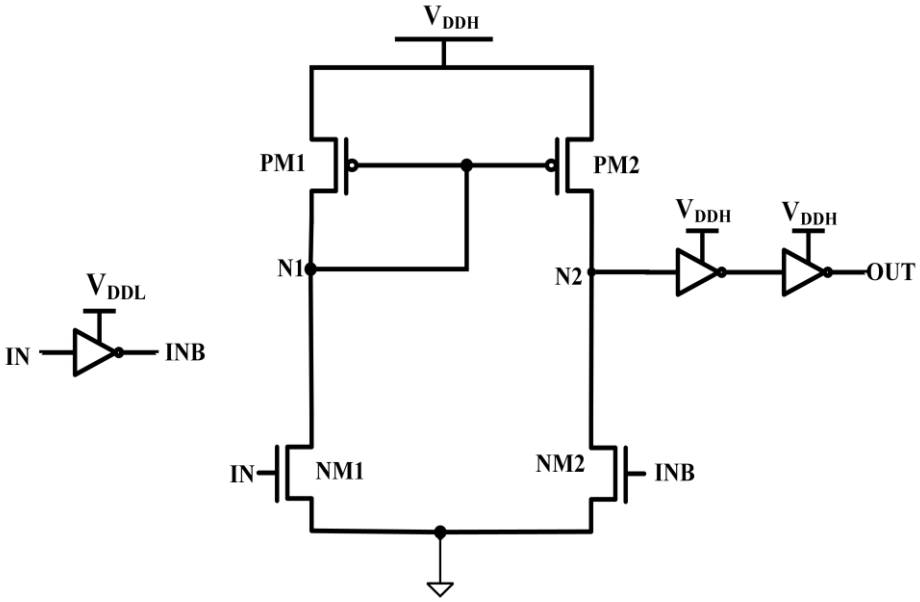

Fig. 2.2: Wilson Current Mirror Voltage Level Shifter Schematic

2.5.2 Working

When the input is high, NM1 transistor turns ON which results in the grounding of node N1. As a result of N1 being grounded, transistors PM1 and PM2 turns ON and a transition current flow through transistor PM1 and transistor NM1. This current is mirrored by transistor PM2 resulting in the charging of Node N2 to V_{DDH}. As a result, the output reaches high logic level.

Conversely, when input is low, the NM2 transistor is activated, which results in the OUT signal being lowered and transistor NM1 is simultaneously deactivated, deactivating the transistors PM1 and PM2. Hence, the output reaches low logic level.

2.5.3 Advantages:

- Faster Operation: This design significantly improves speed, enabling quicker level shifting which is important for time-sensitive circuits.
- Improved Signal Handling: Capable of handling rapid input transitions more smoothly due to its optimized control path.
- Better Signal Integrity: The current mirror stabilizes the output, providing more reliable voltage level shifting.

Disadvantages:

- High Power Consumption: The speed improvements are achieved at the cost of increased power usage, which is a drawback in power-sensitive applications.
- Reduced Battery Efficiency: Not ideal for mobile or battery-powered systems where energy saving is a priority.
- Thermal Concerns: Higher power leads to more heat generation, requiring thermal management in dense circuits.

2.6 Reflected Output based WCMLS (ROWCMLS)

2.6.1 Structure

Fig.2.3 displays the circuit diagram for the hybrid architecture of the voltage level shifter [18]. To further enhance the performance of Wilson Current Mirror VLS circuits, Reflected Output-based WCMLS designs incorporate additional transistors. This modification reduces the delay in switching and improves the efficiency of voltage level shifting by ensuring that the output voltage is more stable during signal transitions.

A PMOS diode PM1 is placed in series with NM1 to further lower power usage. NM3 and PM5 are not activated simultaneously due to the diode connected transistor PM1. In this design, the input inverter is removed by using only the input signal (IN).

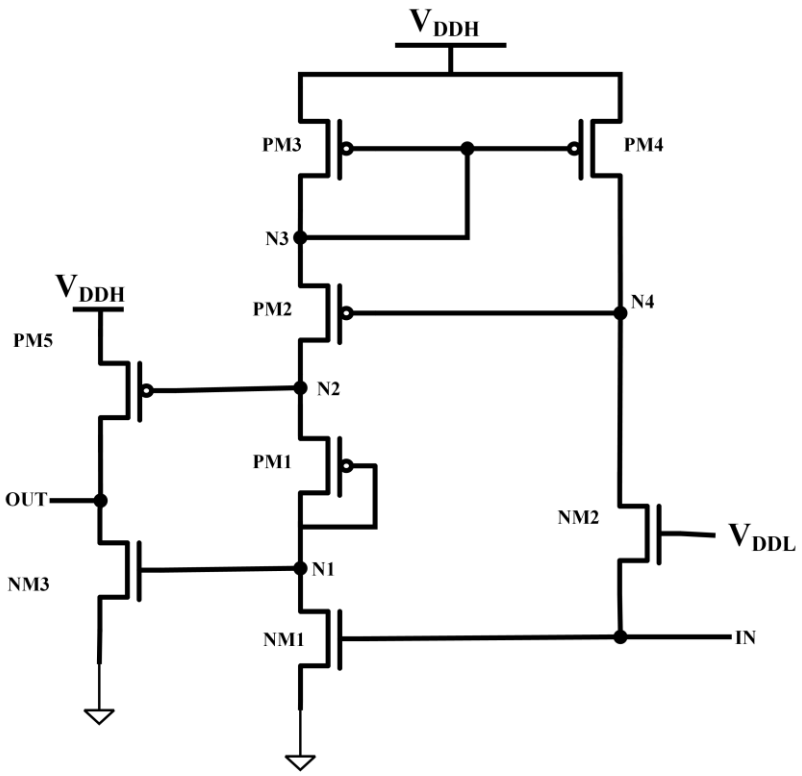

Fig. 2.3: Reflected Output based WCMLS Schematic

2.6.2 Working

When input is high, transistor NM1 is ON pulling down the node N1 to ground, which propagates to node N2. Also, the input reaches node N4 at the gate of PM2 through pass transistor NM2, resulting in PM2 turning OFF. As a result, node N2 discharges completely to ground and PMOS transistor PM5 turns ON and output is charged to V_{DDH} and output gets a high logic level. By adding a PMOS diode connected transistor PM1 in series with transistor NM1, results in a voltage differential between nodes N1 and N2, which in turn prevents transistors PM5 and NM3 from activating simultaneously.

On the other hand, when input is low, NM1 turns OFF and PM2 turns ON, which allows a current to flow in the branch and charge the nodes N2 and N3 to V_{DDH}. As a result, the transistor NM3 turns ON resulting in output node being grounded and the output gets low logic level.

2.6.3 Advantages:

- Balanced Performance: It maintains a trade-off between speed and power consumption, making it a well-rounded solution for general-purpose applications.
- Reduced Output Loading: By controlling unnecessary switching at the output, it helps conserve energy and stabilize circuit operation.
- Energy Efficiency: Better suited than some other designs for systems requiring moderate power efficiency without sacrificing too much speed.

Disadvantages:

- Limited Optimization: May require further tuning for performance-critical or energy-critical applications.
- Design Complexity: Slightly more complex than basic traditional VLS due to additional output control mechanisms.
- Increased Area: The addition of transistors increases the circuit's area, which may be a limitation in miniaturized systems.

2.7 High Performance VLS (HPVLS)

2.7.1 Structure

The circuit diagram of the voltage level shifter is shown in the Fig.2.4. The design is optimized for high-speed applications. The primary goal of the proposed VLS design is to mitigate these limitations by achieving high-speed operation, and precise voltage shifting [19]. This design incorporates additional control transistors that dynamically create and break current paths depending on the output state, thereby reducing the transition delay.

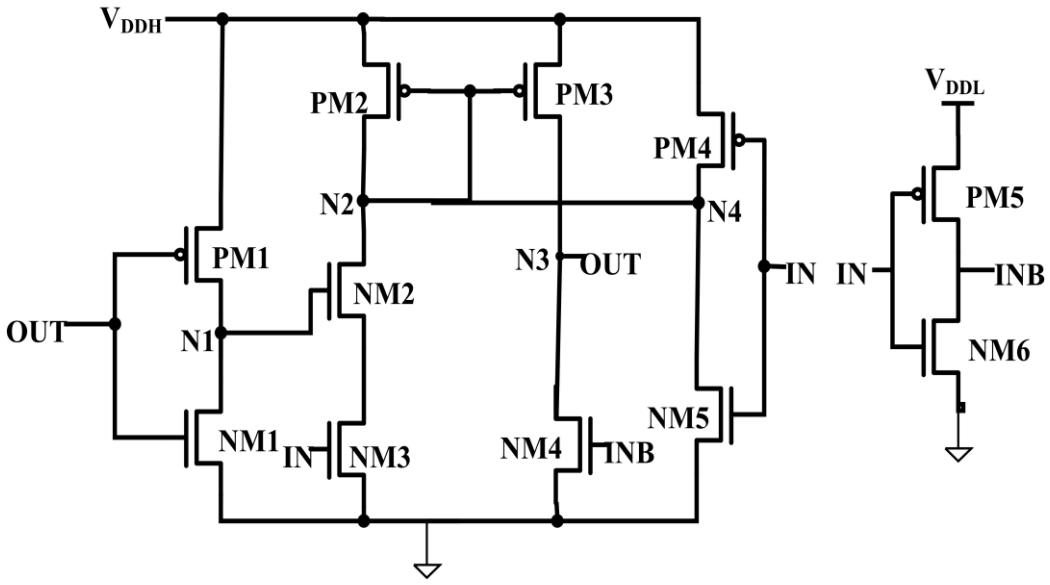

Fig. 2.4: High Performance Voltage Level Shifter Schematic

2.7.2 Working

Assuming initial output voltage to be low and IN signal is high. In this scenario, transistor NM2 and NM3 turns ON and thus the node N2 is pulled down to ground. This results in a current path being generated and a transition current flowing through PM2, NM2 and NM3. With this current mirrored within transistor PM3, the OUT terminal undergoes an elevation to the V_{DDH} level under the influence of PM3. Once the OUT signal reaches the V_{DDH} threshold, the current path generated by PM2, NM2, and NM3 is disengaged. In this situation, transistor NM5 maintains its active state, passing a low signal to both the gate terminals of PM2 and PM3. This function guarantees that the pull-up strength is maintained even after the operation of the current mirror has been terminated. When the IN-signal transitions to low level while the OUT signal remains elevated is considered. During this transition, transistor NM4 is activated, resulting in the grounding of the OUT node. Simultaneously, transistor PM4 turns ON, deactivating the pull-up transistor PM3.

2.7.3 Advantages:

- Optimized for Speed: Delivers the fastest response among the VLS designs, ideal for high-performance and real-time systems.

- High Throughput: Supports circuits where rapid data processing and minimal delay are necessary, such as processors and high-speed communication units.
- Precision in Timing: Suitable for high-frequency systems that require accurate timing control.

Disadvantages:

- Very High Power Usage: The design consumes significantly more power, making it inefficient for long-term or energy-constrained environments.
- Low Energy Efficiency: Despite the speed, the total energy per operation is high, leading to operational inefficiencies.
- Thermal Management Required: May require additional hardware or design considerations to manage the heat produced during operation.
- Complex Design and Optimization: It requires complex design strategies to optimize performance without compromising the required voltage shifts.

2.8 Single Supply VLS (SSVLS)

2.8.1 Structure

The circuit diagram of voltage level shifter is depicted in Fig.2.5. The design is based on differential cascade voltage switch logic. Using a single supply voltage (V_{DDH}), it eliminates the drawbacks of dual-supply designs, reducing system cost and complexity. The implementation employs 10 MOSFETs, with NMOS and PMOS transistors configured to optimize power consumption and speed [20]. Through the combination of a stacked NMOS network (NM1–NM4) and cross-coupled PMOS pair (PM1 and PM2) the Single Supply Voltage Level Shifter performs voltage level translation from low to high voltage while using V_{DDH} as its single power source.

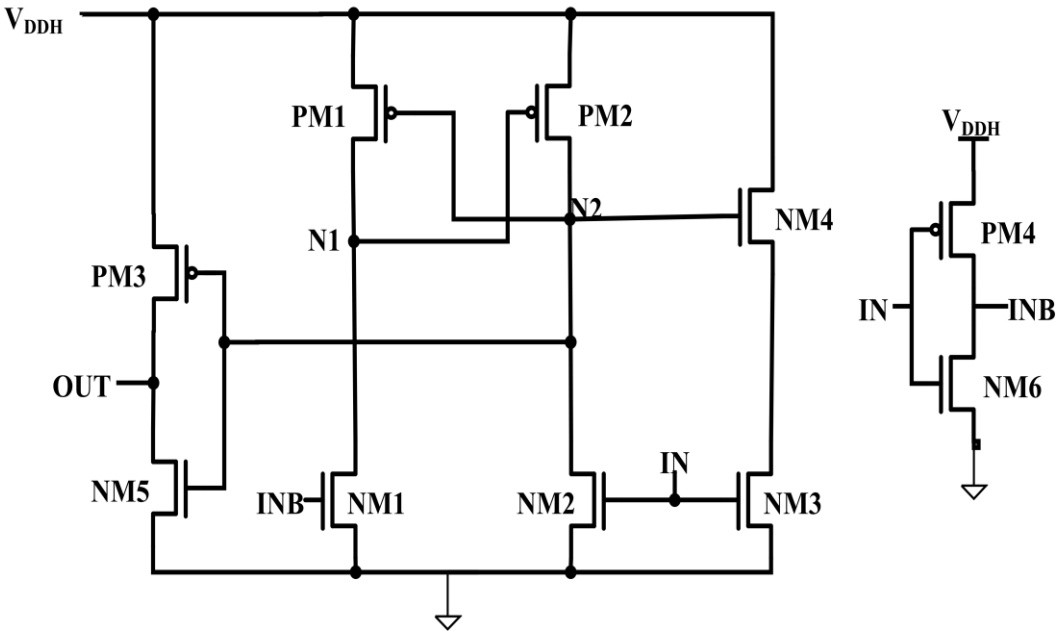

Fig. 2.5: Single Supply Voltage Level Shifter Schematic

2.8.2 Working

When the input voltage IN is low, NM2 and NM3 transistors are in OFF state, whereas NM1 transistor is in ON state, thereby node N1 gets discharged, thus PM2 transistor gets ON. Thus, N2 node begins to charge via transistor PM2. Now N2 node is in high logic which makes transistor NM5 turn ON, thereby we obtain a zero potential at output terminal.

When input voltage is high, both NM2 and NM3 transistors become ON, while NM1 transistor becomes OFF. Thus, node N2 discharges causing the PM1 transistor to turn ON and the node N1 begins charging. Thus, the PM2 transistor gets OFF. Owing to the PM2 transistor turning OFF, N2 node completely discharges, because of that reason PM3 transistor turns ON and we obtained high logic at the output node.

2.8.3 Advantages:

- Lower Dynamic Power: Operates using a reduced voltage swing, effectively decreasing dynamic power consumption during transitions.
- Noise Reduction: Smaller voltage changes generate less electrical noise, making the design suitable for sensitive analog-mixed circuits.
- Energy Conscious Design: Well-suited for designs where average power usage needs to be minimized without entirely sacrificing functionality.

Disadvantages:

- Increased Delay: The reduced swing results in slower transitions, which affects the speed of the circuit.
- Timing Instability: Lower swing levels can introduce variability in timing, potentially complicating circuit synchronization.
- Limited High-Speed Use: Not appropriate for applications where quick signal propagation is essential.

2.9 Conclusion

This chapter presented a comprehensive survey of the designs of multiple voltage level shifters, focusing on their circuit architecture and the working involved to enable consistent voltage translation across different logic levels. The review covered conventional level shifters and more recent and specialized designs for enhancing low-voltage and high-speed performance. Each level shifter type was tested according to a number of key performance parameters, such as propagation delay, static and dynamic power dissipation, etc. To help present a clear comparison, the following table represents the summary, highlighting the strengths and limitations of each design side by side. Through this comparative analysis, the trade-offs engineers have to make when selecting a proper level shifter for certain applications, like mobile devices, high-speed processors, or ultra-low-power systems, are made apparent.

Table 2.1: Comparative Study of Existing Designs

Design	Delay(ns)	Power(μW)	Energy efficiency	Remarks
Traditional VLS	132.95	4.12	547.8	Low power consumption but very high delay but good energy efficiency.
WCMVLS	50.72	70.74	3587.9	Fast design, but high power leading to low energy efficiency.
ROWCMLS	69.3	15.1	1046.43	Balanced performance with moderate delay and better energy efficiency.
HPVLS	47.9	137.7	6595.83	Fastest design, but extremely high power resulting in worst energy efficiency.
SSVLS	140.65	24.18	3400.92	Highest delay with moderate power, resulting in low energy efficiency.

In spite of the range of available solutions, the review demonstrates that most traditional level shifters fail to provide an ideal compromise between power efficiency and speed, especially under tight voltage and scaling conditions. These performance gaps highlight the necessity for a new design paradigm that can achieve low power consumption and high-speed operation and be robust in modern CMOS environments

CHAPTER 3

PROPOSED VOLTAGE LEVEL SHIFTER DESIGN WITH ENHANCED POWER EFFICIENCY

3.1. Overview

The new voltage level shifter (VLSP1) architecture proposed here is intended to overcome the limitation posed by traditional architectures, which provides high performance and energy efficiency using an intelligent dual-supply switching mechanism. In contrast to the traditional design, in this architecture, a switching between the lower supply voltage (V_{DDL}) and the higher supply voltage (V_{DDH}) is dynamically selected for bidirectional efficient voltage level translation. This chapter is a comprehensive description of the proposed design, beginning with the discussion of design and specifications. Then, it details the design method, the circuit topology, and the techniques used to enhance speed and reduce power consumption. The working of the level shifter is described afterwards. Simulation results are given to confirm the accuracy of circuit behaviour, for example, waveform properties, delay of propagation, power consumption, and energy efficiency. These findings confirm the appropriateness of the circuit for power-efficient operations in modern VLSI systems, where level shifting between different voltage domains must be efficient.

3.2. Design Specifications

The voltage level shifter is designed to cross two disparate voltage domains: a low-voltage 0.5V and a high-voltage 1.8V domain. The level shifter facilitates communication between these domains to occur seamlessly by safely and reliably converting logic levels without incurring significant delay or power overhead.

One of the most significant features of this level shifter is that it is bidirectional, having the ability to translate signals in both directions—0.5V to 1.8V and 1.8V to 0.5V—depending on the needs of the system's data flow. This bidirectionality is particularly beneficial in use in applications involving dynamic data exchange, e.g., bus interfaces, memory access protocols, and peripheral

communications where signals have to travel back and forth across low- and high-voltage domains.

3.3. Voltage Level Shifter Structure

Fig.3.1 shows the schematic of the proposed Voltage Level Shifter (VLSP1). The design is differential cascade voltage switch logic based. In the proposed design, 8 MOSFETs have been employed, NM1-NM4 transistors are NMOS and PM1-PM4 transistors are PMOS. The NM4 and PM4 transistor make an inverter which is utilized to provide the inverted input signal (INB) to the design.

In the proposed circuit, the operation depends on the input voltages applied to nodes IN and INB, which control the states of transistors NM1, NM2, NM3 and PM3. These transistors influence the voltages at various circuit nodes, ultimately determining the output voltages.

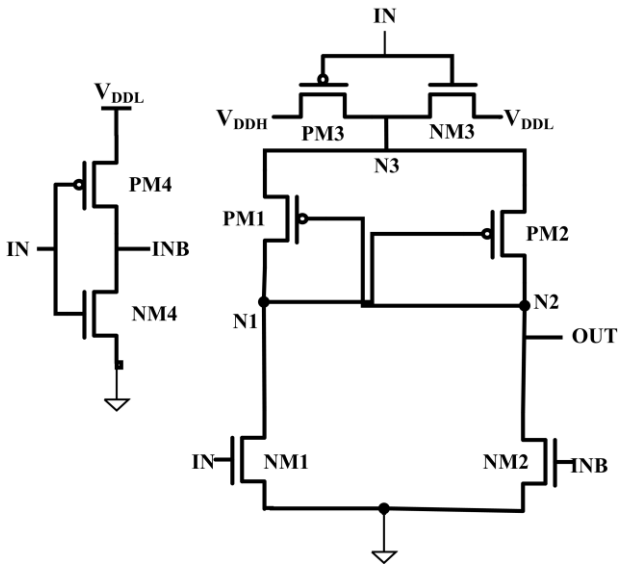

Fig. 3.1: Proposed VLSP1 Structure

3.4. Working of the Proposed Voltage Level Shifter (VLSP1)

The transistors PM3 (a p-type MOSFET) and NM3 (an n-type MOSFET) are configured to act as a voltage selector circuit that dynamically chooses between two power supply rails — a high voltage level V_{DDH} = 1.8 V and a low voltage level V_{DDL} = 0.9 V — based on the logic level of the input signal IN.

- When the input IN is at 0.9 V, PM3 is turned ON due to the sufficient gate-to-source voltage differential (since the source is at 1.8 V and the gate is at 0.9 V), while NM3 is OFF because its gate-to-source voltage is below the threshold required to conduct. As a result, Node N3 is pulled up to V_{DDH} (1.8 V) through PM3.
- In contrast, when IN is at 1.8 V, PM3 turns OFF due to the absence of sufficient gate-to-source bias, while NM3 turns ON (as Vgs = 1.8 V), providing a conductive path from Node N3 to V_{DDL} (0.9 V). Hence, Node N3 is pulled down to 0.9 V.

This switching behaviour of PM3 and NM3 ensures that Node N3 is always biased correctly based on the logic state of IN, thereby enabling proper control of subsequent transistors in the circuit.

The next stage of the level shifter involves transistors NM1, NM2, PM1 and PM2, which collectively generate the final output voltage level by leveraging complementary inputs IN and INB. These signals are inverses of each other and ensure non-overlapping conduction paths to prevent short circuits and unnecessary power consumption.

- Case 1: IN = Low (0 V), INB = High (0.9 V)

  In this scenario, NM1 is OFF because its gate voltage (logic low input signal) is insufficient to turn it on. However, NM2 is turned ON by the high level of INB. As a result, Node N2 is connected to ground via NM2, causing it to discharge. The discharge of N2 causes the output node to be pulled down to 0 V (logic low), since there is no active pull-up through PM2 in this configuration. This ensures a robust logic low at the output terminal.
- Case 2: IN = High (1.8 V), INB = Low (0.9 V)

  Here, NM1 is turned ON as the gate receives a high voltage, allowing it to conduct and discharge Node N1 to ground. At the same time, NM2 is OFF because of logic low input signal which is not sufficient to turn it on. The discharge of N1 pulls the gate of PM2 low, turning PM2 ON. When PM2 conducts, it provides a charging path from the voltage supply (node N3) to the output node. This causes the output node to charge up, resulting in a logic high output.

3.5. Results

Simulation of the demonstrated voltage level shifter design proves efficient level translation of an input voltage of 0.9 V (in red) to an output voltage of 1.8 V

(in blue), as indicated in Fig.3.2(a), and input voltage of 1.8 V (in red) to an output voltage of 0.9 V (in blue), as indicated in Fig.3.2(b). The waveforms prove correct functionality, with crisp and well-aligned input/output signal transitions. The output is a faithful replica of the input, validating the circuit's stable switching behaviour.

The design has a propagation delay of 113.97 picoseconds. Additionally, the circuit has ultra-low power dissipation at only 0.43 µW, presenting it as very appropriate for use in systems with energy constraints. The energy efficiency of 49.01 confirms an acceptable trade-off between power and performance.

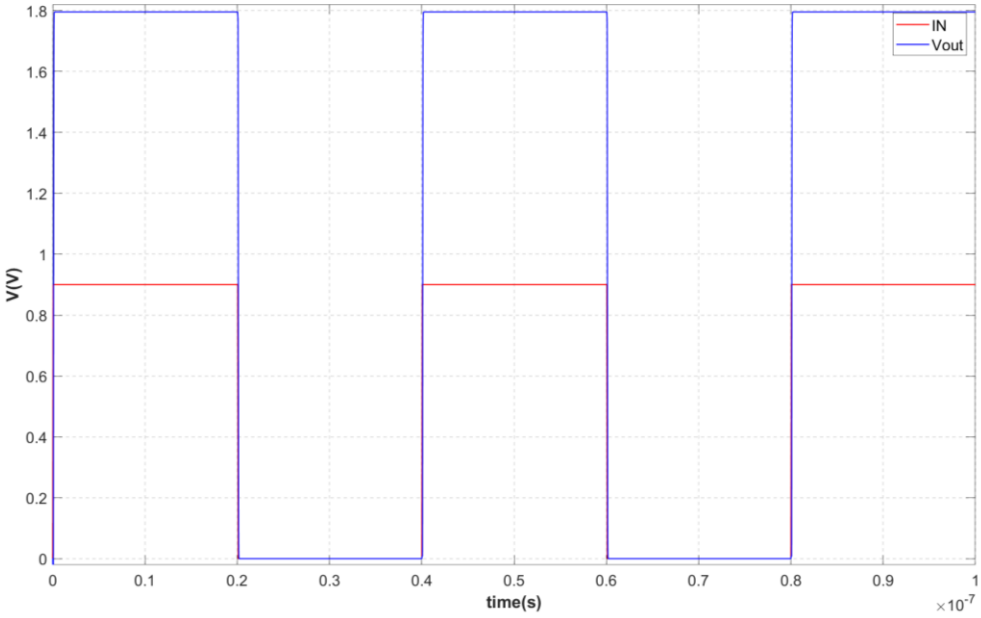

Fig. 3.2(a): Upscale

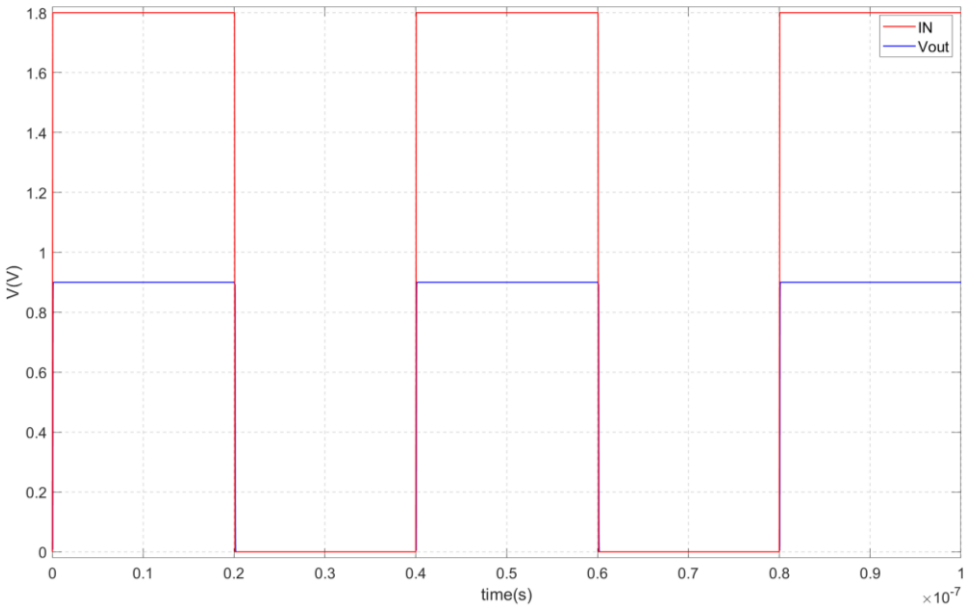

Fig. 3.2(b): Downscale

3.6. Conclusion

In this chapter, the design of the proposed voltage level shifter (VLSP1) was analysed comprehensively through its operation and shown with simulation results. The waveform verified effective voltage translation from 0.9 V to 1.8 V for upscaling and 1.8 V to 0.9 V for downscaling, indicating effective performance of the circuit under test conditions. The demonstrated propagation delay and very low power consumption confirms its suitability for low-power applications. An energy efficiency of 49.01 also indicates the circuit's ability to suit present VLSI systems wherein performance and power optimization are of prime importance. In conclusion, the findings confirm that the proposed design meets the required demands and can easily be utilized to be employed in systems requiring low-power consumption and efficient voltage level conversion in current VLSI systems.

CHAPTER 4

PROPOSED HIGH PERFORMANCE VOLTAGE LEVEL SHIFTER DESIGN WITH SINGLE SUPPLY

4.1. Overview

The proposed voltage level shifter (VLSP2) structure aims to eliminate shortcomings observed in the available structures by achieving a high level of performance with single-supply simplification.A major innovation of this design lies in the utilization of a Wilson current mirror configuration, which provides improved control over the flow of current and thus leads to higher energy efficiency and lower propagation delay. The entire development of the proposed design, its specifications, and design structure, are explained in this chapter. Next, the working of the circuit is explained in detail to emphasize how it accomplishes efficient level shifting. Simulation results are presented to verify design functionality and performance and are supported with waveform analysis and key parameters such as propagation delay, energy efficiency, and power dissipation. The chapter concludes the results by demonstrating that the proposed VLS meets the requirements of today's low-power, high-speed digital systems.

4.2. Design Specifications

The voltage level converter is designed to interface two distinct voltage domains, one operating at a low supply of 0.5V and another higher supply voltage of 1.2V. Effective communication between these voltage domains is supported by the level converter via safe logic level conversion without adding perceivable delay or energy overhead.

One of the key advantages of this design is its ability to maintain balance in power and voltage when operated in single supply mode, which simplifies the power delivery network and minimizes area and complexity in design. Single-supply operation eliminates the need for additional power rails or complex biasing schemes, thereby making the level shifter compatible with low-profile and power-limited systems.

4.3. Voltage Level Shifter Structure

The circuit consists of ten MOSFETs—five NMOS (NM1 to NM5) and five PMOS (PM1 to PM5) as depicted in the Fig.4.1. The topology of the circuit is designed to provide that the circuit can convert a low-voltage logic input signal to a higher voltage logic output with just the single supply voltage (V_{DDH}).

The circuit operation is dependent on the meticulous control of charging and discharging of internal nodes, which in turn control the switching action of the output transistors. The design makes sure that only one of the output transistors (PM5 or NM5) will be conducting at a given time, hence preventing direct current paths that would cause static power loss. Additionally, the application of the diode-connected PMOS (PM3) and Wilson current mirror configuration helps provide better control of internal node voltages that allow mirroring to be done accurately and smoothly even in changing conditions of loads and supplies.By maintaining controlled transitions at internal nodes and using the Wilson current mirror for signal translation, the proposed VLS achieves high speed and power-efficient operation.

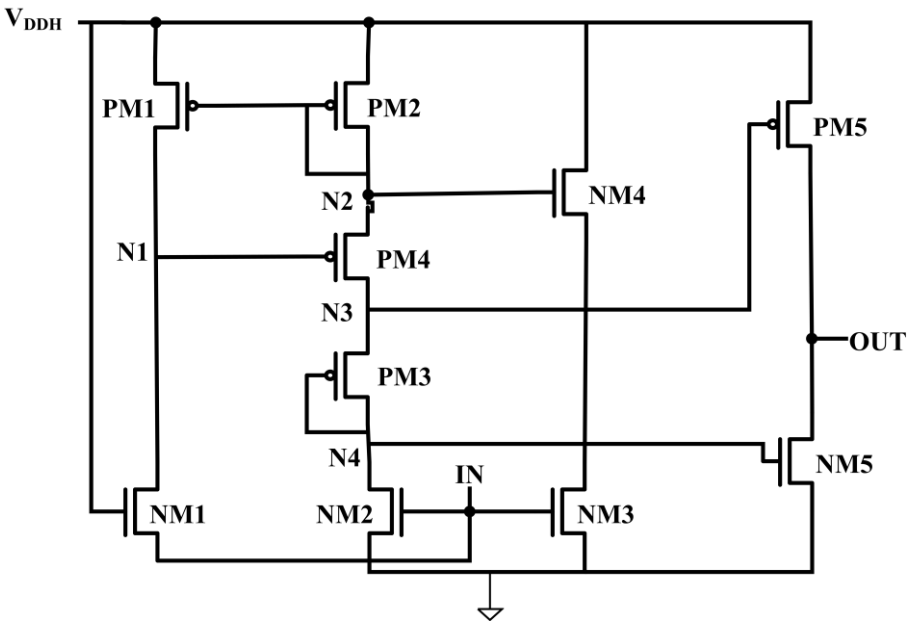

Fig. 4.1: Proposed VLSP2 Structure

4.4. Working of the Proposed Voltage Level Shifter (VLSP2)

Low Input Operation (IN = 0 V)

When the input voltage IN is at 0 V (logic low), the NMOS transistors NM2 and NM3 are both turned OFF. Since these transistors would normally provide a discharge path to ground, their deactivation effectively breaks the conductive path from internal nodes N3 and N4 to ground. As a result, no current flows through the ground path from these nodes.

Simultaneously, the PMOS transistor PM4 is turned ON, as its gate is at a low potential. This activation of PM4 charges nodes N3 and N4 toward the positive supply (V_{DDH} = 1.2 V). The increasing potential at N3 and N4 has cascading effects:

- The high voltage at Node N3 ensures that PM5 remains OFF, as its gate-source voltage is insufficient to turn it on.
- In contrast, the gate of NM5 is now at a high potential (from N4), which turns NM5 ON. This provides a low-resistance path from the output node (OUT) to ground, effectively pulling the output voltage down to 0 V (logic low).

To enhance reliability and prevent short-circuit current (simultaneous conduction of PMOS and NMOS transistors on the output path), PM3 plays a crucial supporting role. Acting as a diode-connected MOS, PM3 ensures a voltage differential between N3 and N4, minimizing overlap in conduction and avoiding excessive short-circuit power dissipation during transitions.

Thus, under low input conditions, the circuit ensures that the output node is firmly pulled to ground while preserving low power consumption.

High Input Operation (IN = 0.5 V)

As the input signal IN rises to 0.5 V (logic high), the behaviour of the circuit changes dramatically to reflect the altered logic state:

- NM2 and NM3 now receive sufficient gate-source voltage to turn ON, providing an efficient discharge path from Node N3 to ground. As a result, N3 and N4 is quickly pulled down to ground.
- The discharge of N3 causes PM4 to turn OFF (due to equalized gate and source potentials), which effectively halts further charging of Node N3. This is a crucial step to prevent continued pull-up action once the logic state changes.

- As N4 is now at 0 V, N3 is connected to N4 via the diode-connected PMOS PM3. PM3 acts as a voltage follower, ensuring that N3 closely tracks the potential at N4 under these conditions.

Now, with N3 at a low voltage, the PM5 transistor is turned ON. This provides a direct charging path from V_{DDH} (1.2 V) to the output node (OUT), allowing the output to rise quickly and efficiently to a logic high level.

At the same time, the gate of NM5 (connected to Node N3) is at low potential, keeping NM5 OFF. This ensures that there is no conflicting discharge path, preventing any short-circuit current and ensuring a clean and unambiguous transition to the high logic state.

4.5. Results

The simulation outcomes of the new voltage level shifter (VLSP2) show robust functionality and improved performance features. The input signal (IN), in red, works at a low voltage level of about 0.5 V. As shown in the Fig.4.2, the output signal (Vout), in blue, effectively switches to a higher logic level of 1.2 V, proving effective level shifting. The output closely tracks the input transitions with crisp and clear edges, signifying superior signal integrity and correct functioning of the circuit.

The propagation delay of the circuit is observed to be 48.41 picoseconds, which verifies its suitability for high-speed applications. The power consumption is read at 22.49 microwatts, which is reasonable for low-power system integration. In addition, the design's energy efficiency is estimated to be 1088.74, reflecting a good tradeoff between power consumption and switching speed. The findings confirm the effectiveness and efficiency of the proposed design and render it very much applicable to high-speed digital systems that necessitate speed along with energy-aware operation.

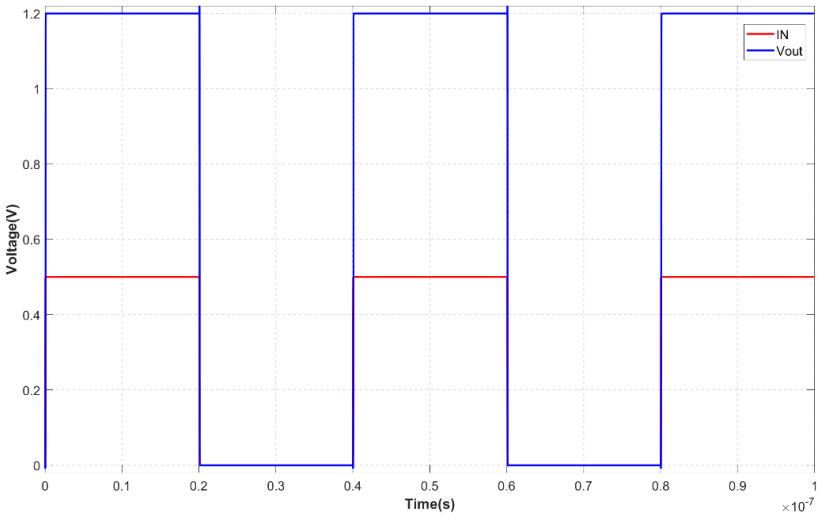

Fig. 4.2: Output of VLSP2

4.6. Conclusion

In this chapter, the performance of the improved low-power, high-speed voltage level shifter was tested using simulation. The waveform outputs confirmed successful voltage level shifting from an input voltage of 0.5 V to an output voltage of 1.2 V, with proper and clean transitions, ensuring the proper functionality of the circuit. The design exhibited a very minimum propagation delay, showing the ability to perform ultra-fast switching. In addition, the circuit consumed a very less power, which made it appropriate for energy-restricted applications. The derived energy efficiency of 1088.74 indicates trade-off between speed and power, supporting the suitability of the circuit for integration into contemporary low-power VLSI systems.

CHAPTER 5

PROPOSED DESIGN OF VOLTAGE LEVEL SHIFTER FOR IOT APPLICATIONS

5.1. Overview

The proposed voltage level shifter (VLSP3) design is introduced with the aim to overcome the shortcomings seen in the earlier structures by consuming less power through a simple single-supply scheme. This chapter discusses the full development of the design, starting from its specifications, and design structure. The adoption of an effective circuit structure enables the proposed voltage level shifter to operate with less power consumption, which makes it well-suited for modern devices like low-voltage battery operated devices.

The chapter provides an elaborate discussion of the circuit working, followed by simulation result, verifying of its operation. Analysis of the input and output waveforms is provided to ensure proper level shifting and general circuit behaviour. The chapter wraps up with a conclusion that reaffirms the appropriateness of the design for integration into energy-efficient VLSI systems.

5.2. Design Specifications

The voltage level shifter is used to cross two different voltage domains: one running at a low 0.5V voltage and the other at a 2V higher voltage. The level shifter supports safe, dependable communication between these realms through logic-level translation without signal integrity compromise or excessive delay introduction.

One of the main characteristics of this design is its single-supply operation, which keeps the power distribution network simple and minimizes the circuit complexity. Avoiding the use of multiple bias voltages or extra regulators, the single-supply mode makes the level shifter suitable for small area and limited resource-based applications, especially when power and area are among important design factors. Besides, the level shifter is also very low-power optimized, both statically and dynamically. It is optimized to reduce leakage current during idle

and dynamic power dissipation during switching activity. This makes the circuit best suited for power-sensitive applications, including portable electronics, IoT devices, and ultra-low-power processors, where power efficiency directly affects battery life and thermal performance.

5.3. Voltage Level Shifter Structure

As shown in the Fig.5.1, the circuit is composed of twelve MOSFETs—six NMOS (NM1 to NM6) and six PMOS (PM1 to PM6). The circuit utilizes complementary NMOS and PMOS pairs to ensure that only one pull path (either to ground or V_{DDH}) is active at any time, minimizing static power dissipation. The circuit establishes a logical sequence of transistor switching that prevents contention and ensures reliable voltage level conversion.

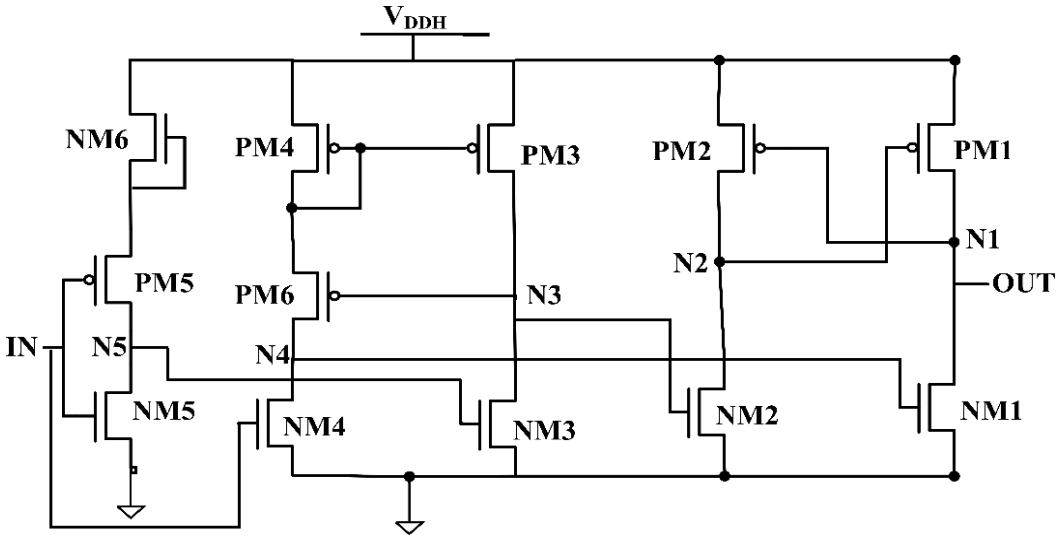

Fig. 5.1: Proposed VLSP3 Structure

5.4. Working of the Proposed Voltage Level Shifter (VLSP3)

The proposed level shifter employs a carefully orchestrated configuration of NMOS and PMOS transistors to enable reliable translation of low-voltage logic levels to higher voltage domains. The circuit operation dynamically adjusts internal nodes and the output state based on the logic level of the input signal. Below is a step-by-step explanation of its functionality in both high and low input conditions.

Case 1: High Input Condition (IN = High)

When the input signal is at a logic high level, the NMOS transistor NM5 is activated (turned ON).

- As NM5 conducts, it provides a path to ground for its connected node N5, which subsequently causes a low voltage to be applied to the gate of NM3, effectively turning NM3 OFF.
- Simultaneously, high input logic state turns ON NM4, allowing Node N4 to discharge to ground through NM4. As a result, N4 reaches a low potential (0 V).
- Since NM3 is OFF, Node N3 is no longer grounded and is allowed to charge high via a pull-up transistor PM3.
- As NM1 receives a low gate voltage from N4, it remains in the OFF state.
- NM2, on the other hand, sees a high gate voltage from N3, turning it ON.

With NM2 ON and NM1 OFF, the output node now connects to the positive supply via a pull-up transistor PM1, resulting in the output being pulled high (logic '1'). Thus, a high input results in a high output.

Case 2: Low Input Condition (IN = Low)

When the input signal transitions to a logic low level, the PMOS transistor PM5 is activated due to the low voltage at its gate terminal.

- As PM5 conducts, it pulls its connected node high, turning NM3 ON and NM4 OFF.
- With NM3 now ON, grounds Node N3.
- And NM4 OFF, Node N4 is disconnected from the ground and starts charging.
- The grounding of Node N3 turns ON PM6, which is a PMOS transistor connected to Node N4.
- As PM6 conducts, Node N4 charges up to the supply voltage (V_{DDH}), attaining a logic high potential.
- The high voltage at N4 now activates NM1 (gate receives high voltage), turning it ON.
- Meanwhile, the low voltage at N3 ensures that NM2 remains OFF.

With NM1 ON and NM2 OFF, the output node is connected to ground via NM1. This creates a logic low output (0 V) corresponding to the low input.

5.5. Results

The simulation result of the proposed voltage level shifter (VLSP3) is shown in Fig.5.2. Analysis show that the level shifter can perform effectively under the aspects of speed and power consumption. The waveform shown in Fig.5.2, clearly

demonstrates the action of the circuit, in which the input signal (IN), shown in red, is at a low voltage level of around 0.5 V. The output signal (Vout), shown in blue, correctly switches to a higher voltage level of 2 V, verifying proper level shifting functionality. The output signal trace closely tracks the input transitions with sharp rising and falling edges, which shows very little delay and excellent signal integrity.

The circuit shows a propagation delay of 128.41 picoseconds. The average power consumption of the circuit is also found to be just 7.95 microwatts, which is reflective of its low-power functionality. The energy efficiency of the design, taken as the product of power consumption and propagation delay, is 1020.8, which represents a very good trade off between power and speed. These findings, coupled with the clean and clear transition of waveforms, confirm the efficacy of the proposed voltage level shifter for application in energy-restricted, high-performance electronic systems.

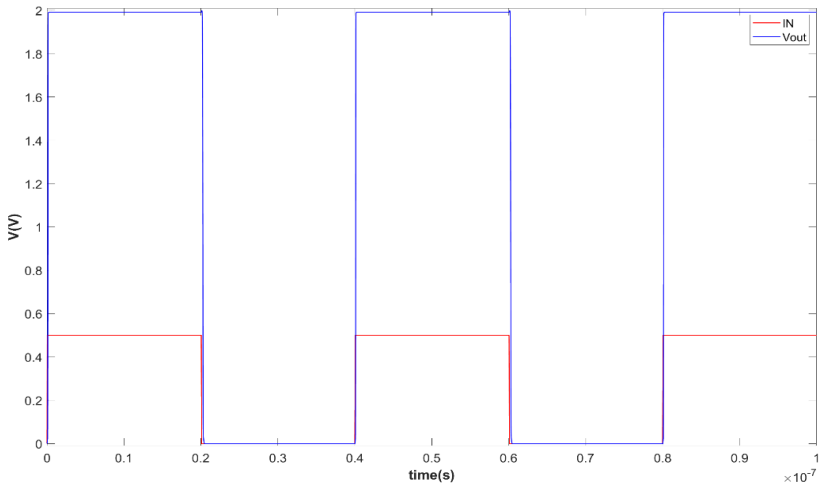

Fig. 5.2: Output of VLSP3

5.6. Conclusion

In this chapter, the proposed voltage level shifter was comprehensively analysed based on the simulation result. The waveform of output guaranteed accurate level shifting from 0.5 V input to 2 V output and ensured proper functionality with smooth and quick transitions. The proposed design had a comparable propagation delay, which shows its suitability for applications in high-speed systems. In addition, the circuit exhibited extremely low power consumption, making it highly efficient for low-power use. The calculated energy efficiency of 1020.8 is a further indication of the optimal speed versus power

trade-off. All these results bear testimony to the effectiveness of the proposed design and verify its suitability for use in modern-day VLSI circuits where high performance and low energy demands are essential.

CHAPTER 6

SIMULATION RESULTS ANALYSIS AND COMPARISON

6.1. Introduction

This chapter describes the simulation setup employed to verify the performance of the proposed low-power, high-speed voltage level shifter designs. The design wereimplemented and tested under different operating conditions, where emphasis was placed on analysing crucial performance parameters including power consumption, propagation delay, and voltage swing. Simulation results are compared to confirm the efficacy of the design. Additionally, the outcomes of the proposed designs were contrasted with the outcomes of the current voltage level shifter designs presented in the literature (as introduced in Chapter 2). Special emphasis lies in the comprehension of the trade-offs between the speed and power consumption.

6.2. Simulation Setup

To validate the operation and efficiency of the proposed designs, severe simulations were performed using the Cadence Virtuoso design tool with 90nm CMOS technology [21]. For evaluating the robustness of the proposed designs, the circuits were simulated at various voltage levels.

6.3. Performance Metrics

The following parameters were simulated to evaluate the performance of the proposed voltage level shifter designs:

- Propagation Delay: The duration for which the input signal travels from the source to the output. It is essential for high-speed applications.
- Power Consumption: The combined power consumption, both dynamic and static power utilized by the level shifter in operation.
- Voltage Swing: The ability of the level shifter to reliably translate the voltage levels between the two domains.

- Energy Consumption: The energy consumption is expressed as a product of propagation delay and average power usage.

6.4. Performance Comparison

To conclusively evaluate the performance of the novel voltage level shifter circuit designs proposed, a detailed comparison was made with previously reported architectures in the literature (as presented in Chapter 2). The comparison points out the relative merits of the proposed circuits under important performance parameters. The table below gives an overall overview of the performance characteristics, facilitating easy assessment of how the designed solutions compare to previous work.

Table 6.1: Comparison of VLS Designs

VLS Design	**Delay (ns)**	**Power (µW)**	**Energy Consumption (Delay × Power)**
Traditional VLS	132.95	4.12	547.8
WCMVLS	50.72	70.74	3587.9
ROWCMLS	69.3	15.1	1046.43
HPVLS	47.9	137.7	6595.83
SSVLS	140.65	24.18	3400.92
Proposed VLSP1 (ch4)	113.97	0.43	49.01
Proposed VLSP2 (ch5)	48.41	22.49	1088.74
Proposed VLSP3 (ch6)	128.41	7.95	1020.8

Through an analysis of the data of the given table, we can determine each design's performance and recognize trade-offs between power efficiency and speed. These observations assist in comprehending the comparative merits and drawbacks of every design, informing the choice of the best VLS for particular application requirements. The minute observations are enumerated below:

- HPVLS achieves the best delay performance (47.9 ns) but at the expense of extremely high power consumption (137.7 μW), causing the worst energy efficiency (6595.83). This renders it less suitable for energy-sensitive applications despite its high speed.
- SSVLS has the largest delay (140.65 ns) and average power consumption (24.18 μW). Its energy efficiency (3400.92) is also poor, and it has a lower voltage swing as well, which can potentially restrict full-swing logic level compatibility.
- WCMVLS and ROWCMVLS have comparatively low delays and acceptable power usage, with respective energy efficiencies of 3587.9 and 1046.43. ROWCMVLS is more energy-efficient because it consumes much less power.
- Conventional VLS has a large delay (132.95 ns) but low power consumption (4.12 μW), and hence good energy efficiency (547.8) compared to the majority of the designs.
- Proposed VLSP1 (ch4) has superior energy efficiency with the minimum value (49.01) among all the designs. This is because it has very low power consumption (0.43 μW), even though its delay (113.97 ns) is moderate. It is thus very well suited for ultra-low-power applications in which speed is not a major issue.
- Proposed VLSP2 (ch5) has a balanced trade-off between power and delay, with low delay (48.41 ns) and moderate power usage (22.49 μW). Therefore, it has a good energy efficiency (1088.74) and thus a good candidate for those applications that call for speed as well as energy efficiency.
- Proposed VLSP3 (ch6) has low power consumption (7.95 μW) but increased delay (128.41 ns), still having good energy efficiency (1020.8). It can be appropriate where power is limited but there can be some delay.

6.5. Conclusion

This chapter provided an extensive evaluation of the simulation outcomes for the novel low-power, high-speed voltage level shifter designs. The performances were evaluated based on critical parameters such as propagation delay, power

usage, energy efficiency, and voltage swinging capability. These designs had individual strengths tailored to particular application areas. VLSP1 was proven to be extremely energy-efficient and bidirectionally operational, thus being suitable for ultra-low-power and energy-restricted applications. VLSP2 possessed the highest switching speed, thereby proving its applicability in speed-critical digital circuits. VLSP3 provided balanced performance with acceptable power consumption and wide voltage operation, hence being suitable for general-purpose mixed-signal applications. The designs are able to meet the key requirements of speed, power efficiency, and functional strength. Trade-offs between the performance parameters were addressed, and the comparison results indicate that these designs are extremely versatile for application in current integrated circuits, especially where reliable voltage level conversion over different domains is needed.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1. Conclusion

This thesis focused on the design and implementation of voltage level shifters for low-power applications, high-speed applications suitable for modern integrated circuit applications. The primary contribution is the designs of a voltage level shifter that simultaneously achieves low power consumption and high-speed operation, making it suitable for modern low-voltage applications. The thesis contains a comparative study of the proposed designs with other level shifter designs presented in the literature, showing its superiority in both power consumption and speed.The proposed designs overcome the problems inherent in traditional level shifters, especially regarding power consumption and propagation delay. By optimizing the circuit design with caution, the developed level shifter succeeded in these results despite changing operating conditions. The main findings of the research are: The designs realized low power dissipation, a considerable advancement over previous designs. The propagation delay was minimal, fitting high-speed applications in today's systems.The output voltage swing was consistent across both the low-voltage and high-voltage domains, ensuring reliable logic level translation. The simulation results validate the effectiveness of the proposed voltage level shifter designs and demonstrate its potential for use in low-power, high-performance systems such as mobile devices, Internet of Things (IoT) devices, and biomedical sensors.

7.2. Future Work

Although the proposed voltage level shifter (VLS) designs have shown encouraging results in low power usage, lower propagation delay, and increased signal integrity, various areas can be explored to better improve their performance and applications. One key research direction is incorporating these designs into more innovative semiconductor process nodes, like 22nm, 16nm, or even FinFET-based technologies. While technology continues to scale, these nodes provide significant benefits in terms of power efficiency, switching speed, and integration density, but also pose new design challenges, such as greater short-channel

effects, greater leakage currents, and process variability. Mitigation of these could allow the VLS circuits to function more reliably in future low-voltage digital systems. In addition, though this work draws upon intensive simulations with 90nm CMOS models, experimental verification by physical implementation is a most important subsequent step. Prototyping the proposed level shifter circuits on silicon and making post-silicon measurements would lend real-world confirmations of key parameters like dynamic and static power consumption, propagation delay, voltage swing, and noise margins. This would also be useful for discovering inconsistencies between simulated and measured behaviour caused by parasitic effects, manufacturing tolerances, and temperature gradients. It would also be possible to include the VLS circuits in an overall system-on-chip (SoC) or field-programmable gate array (FPGA) design so that complete evaluation could be made under realistic operating conditions. Such system-level integration would show the performance of the level shifter in complex, mixed-voltage settings, particularly with interfacing between low-power cores, memory blocks, and high-speed I/O subsystems. It would also allow for the testing of variable workloads, making further optimizations possible for targeted application domains like mobile devices, IoT systems, and wearable electronics. By employing these prolonged explorations, the strengths, effectiveness, and scalability of the devised VLS designs are better comprehensible and can be improved to meet future low-power high-performance VLSI demands.

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