ANALOG UNIVERSAL FILTER DESIGN USING CMOS VDCC AS AN ACTIVE BUILDING BLOCK

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in

CONTROL & INSTRUMENTATION

by

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23/C&I/01

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ABSTARCT

This study validates design and implementation of voltage-mode (VM) triple-input, single-output (TISO) biquad filter that employs a single voltage differencing current conveyor (VDCC) as the core active building block. The research encompasses a comprehensive study of various analog filter responses, including low-pass, high-pass, band-pass, band-stop and all-pass filters, emphasizing the VDCC's versatility and superior performance metrics. The study is structured to include a detailed theoretical analysis and extensive PSPICE simulation of CMOS based VDCC filters. The theoretical analysis entails deriving the design equations and comprehending the operational principles of VDCCs in filter circuits. These models are subjected to rigorous validation through extensive simulations using advanced electronic design automation (EDA) tool like PSPICE. Additionally, the circuit allows for the adjustment of the cutoff frequency (ω_0) and pole quality factor (Q). The configuration was designed and simulated using PSPICE, and the simulation results were cross-verified with theoretical expectations.

In conclusion, this research makes a significant contribution to the domain of analog filter design by presenting VDCC as a robust and efficient alternative to conventional methodologies. The findings substantiate the practical advantages of VDCC, paving the way for future innovations in analog signal processing. This work establishes a solid foundation for further exploration and application of VDCC in various analog circuit designs, promising enhanced performance, reduced power consumption, and increased versatility in modern electronic systems.

LIST OF PUBLICATIONS

Publisher	Name of Paper	Scopus Indexed
Springer RITEEC 2025 (NIT Patna)	VDCC-Based Voltage-Mode Universal Filter	YES
Springer PICS 2025 (NIT Hamirpur)	Single CMOS VDCC-Based Voltage Mode Universal Filter	YES

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CHAPTER 1

1. INTRODUCTION

1.1 ANALOG SIGNAL PROCESSING (ASP):

Analog Signal Processing [1] refers to the manipulation or modification of continuous-time signals using analog circuits and devices. Unlike digital signal processing, which involves discrete-time (sampled and quantized) signals, ASP works directly with natural, real-world signals such as voltage or current waveforms that vary continuously over time.
Examples of analog signals include:

- Audio signals (voice, music)
- Biomedical signals (ECG, EEG)
- Sensor outputs (temperature, pressure, light)

Analog signal processing involves performing operations such as:

- Amplification
- Filtering
- Integration and Differentiation
- Modulation and Demodulation
- Mixing and Oscillation

These operations are performed using analog circuit components that respond in real-time to input signals without converting them to digital form.

Advantages of Analog Signal Processing

- Real-time Operation: Instantaneous response to signal changes
- Low Latency: Minimal delay compared to digital processing
- No Sampling or Quantization Error: Avoids issues inherent in analog-to-digital conversion
- Lower Power in Some Applications: Especially for low-frequency or low-data-rate signals
- Simplicity: Certain operations are easier to implement in analog (e.g., simple filters)

Limitations

- Noise Sensitivity: Analog circuits are more prone to noise and signal degradation
- Limited Flexibility: Reconfiguration requires physical changes to the circuit

- Accuracy and Stability: Can drift over time and with temperature
- Scaling Issues: Complex analog circuits take up more space and are harder to integrate

Applications

- Audio electronics (equalizers, preamplifiers)
- Communication systems (modulation, RF filters)
- Medical instrumentation (EEG, ECG amplifiers)
- Control systems (PID controllers)
- Instrumentation and Measurement (signal conditioning)

1.2 FUNDAMENTALS OF FILTER DESIGN:

Filter design is a critical component in the field of signal processing, electronics, communication systems, and control engineering. Filters are used to remove unwanted components or features from a signal, enhance desired signal characteristics, and shape frequency responses according to specific requirements. The process of filter design involves determining the filter type, selecting appropriate specifications, and implementing the design using either analog or digital techniques. Manipulating signals through filtering is crucial for ensuring optimal performance and functionality in electronic systems. Traditional filter design typically employs standard active and passive components, which can introduce challenges such as increased complexity, higher power consumption, and performance limitations. A filter is essentially a circuit that alters signals based on their frequency content. Filters are commonly classified by their magnitude response into categories such as low-pass (LP), high-pass (HP), band-pass (BP), and band-reject or notch (BR) filters [1]. Additionally, all-pass (AP) filters form another class that adjusts the phase of signals without affecting their magnitude.

In the realm of electronic circuit design, filters serve as indispensable tools for signal processing, allowing engineers to manipulate signals according to specific frequency characteristics. While passive components like resistors, capacitors, and inductors traditionally have been used to construct filters, the emergence of active building blocks has revolutionized filter design by offering enhanced performance, flexibility, and efficiency. This chapter explores the principles, advantages, and methodologies involved in designing filters using active building blocks, shedding light on their significance in modern electronic systems. Filters constitute indispensable elements within electronic circuits used to selectively pass or attenuate signals based on their frequency content. They are utilized across a range

of fields, spanning communication systems, audio manipulation, instrumentation, and control systems.

1.3 CLASSIFICATION OF FILTERS:

Filters can be broadly categorized based on their frequency response characteristics and implementation domain:

- Low-Pass Filter (LPF): Allows low-frequency signals to pass while attenuating those that exceed a certain cutoff frequency.
- High-Pass Filter (HPF): Transmits high-frequency signals above a specified cutoff and reduces the strength of lower-frequency components.
- Band-Pass Filter (BPF): Enables signals within a specific frequency range to pass, while filtering out frequencies outside this range.
- Band-Stop Filter (BSF) or Notch Filter: Blocks or attenuates a select narrow band of frequencies, letting all others pass through with minimal effect.
- All-pass filters (APF): An APF is a signal processing tool that permits all frequencies to travel through it. However, its distinctive feature lies in its ability to modify the phase relationship between the input and output signals, while leaving the amplitude (or magnitude) of those frequencies unchanged.

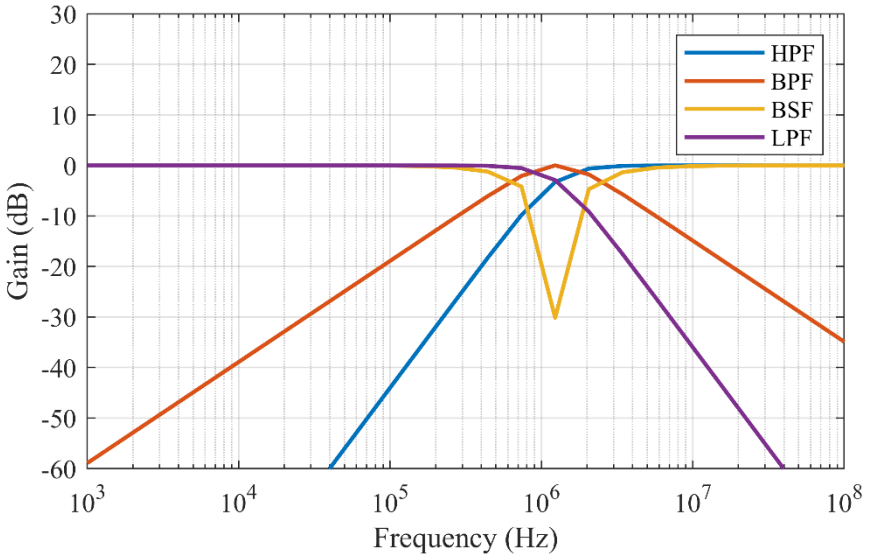

Figure 1.1: Frequency response curves for LPF, HPF, BPF, and BSF.

1.3.1 LOW PASS FILTER (LPF):

A Low-Pass Filter (LPF) is an essential electronic circuit that allows signals with frequencies lower than a certain cutoff frequency to pass through while attenuating higher-frequency components. LPFs are widely used in analog and digital signal processing applications to remove high-frequency noise, smooth waveforms, and extract useful low-frequency signals from mixed-frequency inputs.
An LPF works based on the principle of frequency discrimination. When a composite signal containing multiple frequency components is passed through a low-pass filter, the filter suppresses or attenuates the components above the cutoff frequency (fc) while allowing those below fc to pass with minimal attenuation. The cutoff frequency is defined as the frequency at which the output signal power drops to half of its maximum value, or the output voltage amplitude drops to 0.707 of the input (which corresponds to a -3 dB point in a Bode plot).

Low-pass filters can be implemented in several ways depending on the application:

- Passive LPF: Made using only passive components such as resistors (R), capacitors (C), and inductors (L).
- Active LPF: Incorporates active elements such as operational amplifiers (op-amps) along with R and C components.
- Digital LPF: Implemented via algorithms in digital systems (DSPs or microcontrollers).

The simplest LPF consists of a resistor and a capacitor connected in series, with the output taken across the capacitor. The transfer function of this circuit is

$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{1}{(1 + sRc)} \tag{1.1}$$

where s = jω. The cutoff frequency is given by

$$fc = \frac{1}{(2\pi RC)} \tag{1.2}$$

When the input frequency is well below the cutoff frequency (f_c), the capacitor behaves like an open circuit, allowing the signal to pass through with minimal loss. In contrast, at frequencies significantly above f_c, the capacitor acts almost like a short circuit, causing the output signal to be greatly reduced. For a first-order low-pass filter (LPF), the gain drops at a rate of approximately -20 dB per decade beyond the cutoff frequency.

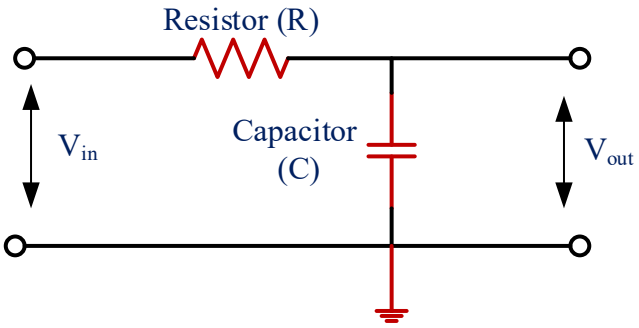

Figure 1.2: RC LPF Circuit

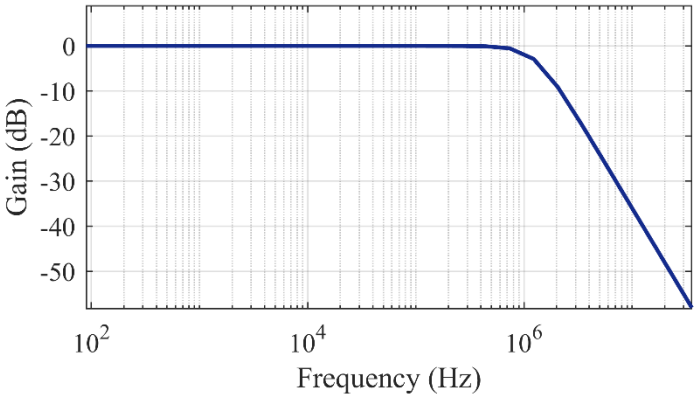

Figure 1.3: Frequency Response of LPF

Applications of LPFs include:

- Audio processing
- Data acquisition
- Communication systems
- Power supplies
- Image processing

Advantages of LPFs:

- Simple to design and implement
- Effective in attenuating high-frequency noise
- Easily tunable by adjusting component values

Limitations:

- Passive LPFs cannot provide gain
- Sharpness of the transition is limited in low-order filters
- May introduce phase shift and time delay

1.3.2 HIGH PASS FILTER (HPF):

A High-Pass Filter (HPF) is an electronic circuit designed to allow signals with frequencies above a specific cutoff point to pass while attenuating those with lower frequencies. These filters are widely applied in areas such as signal processing, communication systems, and control engineering to eliminate low-frequency noise, remove DC offsets, and isolate high-frequency components from complex input signals.

HPFs function by filtering out unwanted low-frequency signals. When a mixed-frequency input is applied, the filter suppresses components below the cutoff frequency (f_c) and permits those above this threshold to pass with little loss.

The cutoff frequency marks the point at which the output power drops to half of the input power. This corresponds to a voltage gain reduction to approximately 70.7% of the original signal, which is recognized as the -3 dB point in the filter's frequency response.

High-pass filters can be categorized based on their design and operational approach:

- Passive High-Pass Filters: Built using resistors and capacitors (RC) or resistors and inductors (RL), these filters do not amplify signals and are mainly used for basic signal conditioning.
- Active High-Pass Filters: Incorporate active components like operational amplifiers along with resistors and capacitors. These filters not only shape signals but can also amplify them, providing improved performance in precision applications.
- Digital High-Pass Filters: Implemented via algorithms in digital signal processors (DSPs) or software, these filters are used for processing digital signals.

The most basic form of a high-pass filter uses a capacitor in series with a resistor, with the output taken across the resistor. The mathematical representation of this configuration is known as its transfer function.

$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{sRc}{(1 + sRc)} \tag{1.3}$$

where s = jω. The cutoff frequency is given by

$$fc = \frac{1}{(2\pi RC)} \tag{1.4}$$

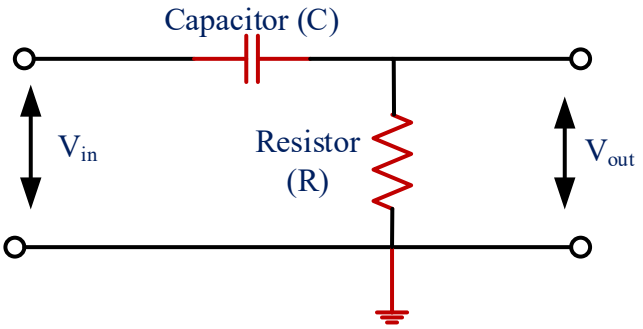

Figure 1.4: RC HPF Circuit

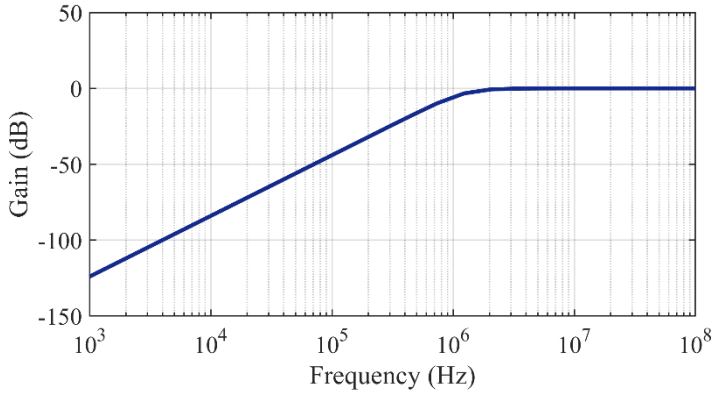

Figure 1.5: Frequency Response of HPF

At frequencies much lower than fc, the capacitor blocks the signal (high impedance), resulting in low output. At frequencies much higher than fc, the capacitor acts like a short circuit, and the signal passes to the output. The filter exhibits a gain increase of +20 dB/decade up to the cutoff point in a first-order HPF.

Applications of High-Pass Filters

- Audio systems: To eliminate low-frequency hum and rumble (e.g., microphone or speaker circuits).
- Data transmission: To remove DC offset in signals.
- Image processing: To enhance edges and details by removing low-frequency components.
- Biomedical devices: To eliminate baseline drift in ECG or EEG signals.
- Communication systems: For separating desired high-frequency signals from mixed sources.

Advantages:

- Simple construction and easy to implement.
- Useful in rejecting unwanted low-frequency noise.
- Passive versions do not require power supply.

Limitations:

- Passive filters cannot provide gain.
- Limited selectivity in first-order designs.
- May introduce phase distortion in time-sensitive applications.

High-pass filters are indispensable in many electronic systems where low-frequency interference needs to be suppressed or where only high-frequency signals are of interest. Understanding their design, implementation, and limitations enables engineers to effectively use them in a wide variety of practical applications.

1.3.3 BAND PASS FILTER (BPF):

A Band Pass Filter (BPF) is an electronic circuit or device that allows signals within a certain frequency range to pass through while attenuating frequencies outside that range. Essentially, it combines the characteristics of both a low pass filter and a high pass filter. Band pass filters are widely used in communication systems, audio processing, instrumentation, and various signal processing applications.

The operation of a band pass filter is based on the principle of frequency selection. It allows frequencies between a lower cutoff frequency f_L and an upper cutoff frequency f_H to pass through, while attenuating frequencies lower than f_L and higher than f_H.

The bandwidth (BW) of the filter is defined as the difference between the upper and lower cutoff frequencies:

$$BW = f_L - f_H \tag{1.5}$$

The center frequency f_C is the geometric mean of the cutoff frequencies:

$$f_c = \sqrt{f_L \cdot f_H} \tag{1.6}$$

Band pass filters can be categorized based on their design:
a) Passive Band Pass Filter

- Composed of passive components such as resistors (R), capacitors (C), and inductors (L).
- Does not require any external power source.
- Simple in design but lacks amplification.

b) Active Band Pass Filter

- Uses active components like operational amplifiers (op-amps) along with R, L, and C.
- Requires external power supply.
- Offers better gain and tuning capabilities.

A basic passive band-pass filter (BPF) can be created by connecting a high-pass RC filter in series with a low-pass RC filter. However, because it lacks an active amplification stage, the overall gain remains limited. The frequency response of a band-pass filter features a peak at the center frequency f_C, with the output gradually decreasing on both sides of the passband.

Important characteristics include:

- Passband: The specific frequency range that the filter allows to pass through with minimal attenuation.
- Stopband: Frequency ranges outside the passband that are significantly reduced or blocked.
- Roll-off Rate: Describes how quickly the filter suppresses signals beyond the passband, typically measured in decibels per decade or per octave.

The Q-factor of a band pass filter describes how "selective" or "sharp" the filter is around its center frequency:

$$Q = \frac{f_C}{BW} \tag{1.7}$$

- A high Q-factor indicates a narrow bandwidth and high selectivity.
- A low Q-factor means a broader bandwidth and lower selectivity.

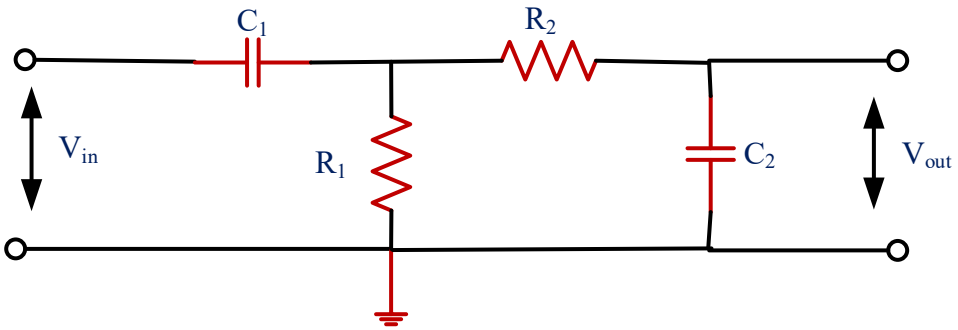

Figure 1.6: RC BPF Circuit

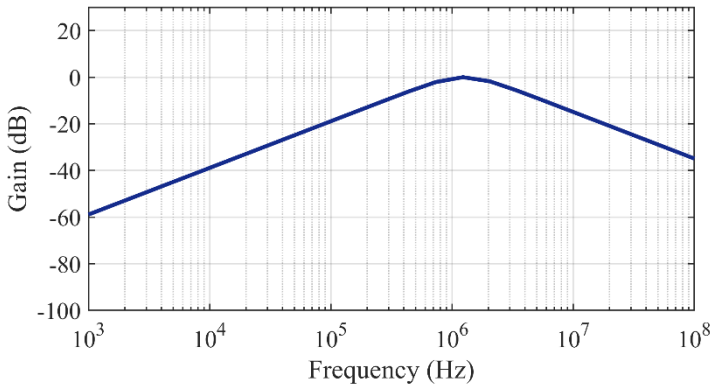

Figure 1.7: Frequency Response of BPF

Applications

- Wireless Communication: Selecting specific frequency bands in radio receivers.
- Audio Systems: Isolating certain frequencies in equalizers.
- Biomedical Devices: Filtering physiological signals (e.g., ECG, EEG).
- Instrumentation: Removing noise from sensor signals.

1.3.4 BAND STOP FILTER (BSF):

A Band Stop Filter (BSF), also known as a Band Reject Filter or Notch Filter, is an electronic filter that attenuates (blocks) signals within a specific frequency range while allowing frequencies outside this range to pass through. It essentially does the opposite of a Band Pass Filter. Band stop filters are used in various applications such as noise suppression, audio processing, instrumentation, and communication systems.

A band stop filter allows signals below a certain lower cutoff frequency f_L and above an upper cutoff frequency f_H to pass with minimal attenuation, but significantly attenuates frequencies between these two values. This blocked range of frequencies is called the stopband.

The bandwidth (BW) of the stopband is calculated as:

$$BW = f_H - f_l \tag{1.8}$$

The center frequency f_C of the filter is given by the geometric mean of the cutoff frequencies:

$$f_c = \sqrt{f_L \cdot f_H} \tag{1.9}$$

Built using passive components such as resistors (R), capacitors (C), and inductors (L). No amplification or external power is required. Typically used for low-frequency applications.

The frequency response of a band stop filter shows a notch or dip at the center frequency, indicating strong attenuation. The response is flat on either side of the notch, meaning that frequencies far below and far above the stopband are passed with minimal loss.

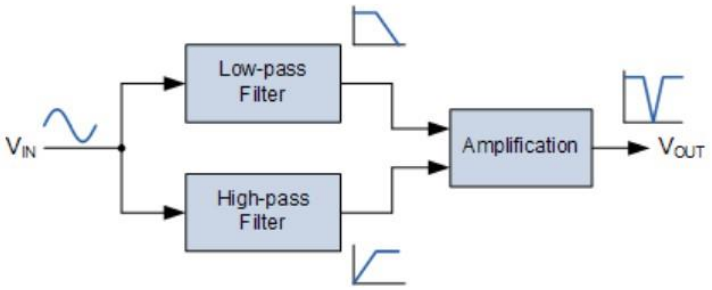

Figure 1.8: Typical BSF Configuration

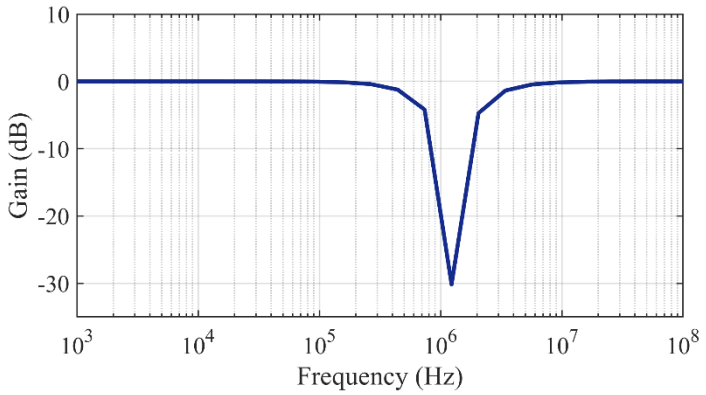

Figure 1.9: Frequency Response of BSF

Key terms:

- Stopband: Range of frequencies that are highly attenuated.
- Passbands: Frequencies outside the stopband that pass through with minimal attenuation.

- Roll-off Rate: The rate at which attenuation increases near the edges of the stopband.

The Q-factor of a band stop filter describes the selectivity or sharpness of the attenuation around the center frequency:

$$Q = \frac{f_C}{BW} \tag{1.10}$$

- A high Q indicates a narrow notch with steep attenuation (useful in notch filters).
- A low Q corresponds to a broader attenuation band.

Applications

- Power Line Noise Rejection: Filtering out 50 Hz or 60 Hz hum from audio signals.
- Communication Systems: Removing unwanted narrowband interference.
- Medical Devices: Eliminating specific interference frequencies in ECG or EEG systems.
- RF Systems: Suppressing spurious emissions or interference signals.
- Audio Processing: Removing undesirable resonant frequencies (feedback or hum).

1.3.5 ALL PASS FILTER (APF):

An All-Pass Filter (APF) is a type of signal processing filter that passes all frequency components of an input signal with equal gain, but alters the phase relationship among various frequencies. Unlike other filters (low-pass, high-pass, band-pass, or band-stop), an all-pass filter does not affect the amplitude of the input signal at any frequency; its primary purpose is phase shifting or phase equalization.

All-pass filters are widely used in audio processing, control systems, communications, and digital signal processing (DSP) for group delay correction, phase compensation, and signal alignment.

The key characteristic of an all-pass filter is:

- Magnitude Response: Constant (unity gain) across all frequencies.
- Phase Response: Varies with frequency.

Mathematically, the magnitude of the transfer function

$|H(j\omega)|=1$

for all ω, but the phase ∠H(jω) is frequency-dependent. This phase shift can be designed to compensate for phase distortion introduced by other system components, aligning signals in time.

A basic first-order analog all-pass filter has the following transfer function:

$$H(s) = \frac{s - a}{s + a} \tag{1.11}$$

Where:

- s=jω (Laplace variable)
- a is a real, positive constant

First-Order All-Pass Filter introduces a phase shift that varies from 0° to −180° (or 180°, depending on design). Has a flat magnitude response

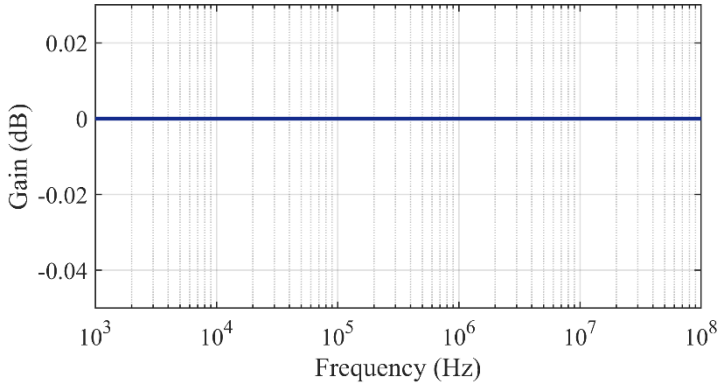

Figure 1.10: Frequency Response of APF

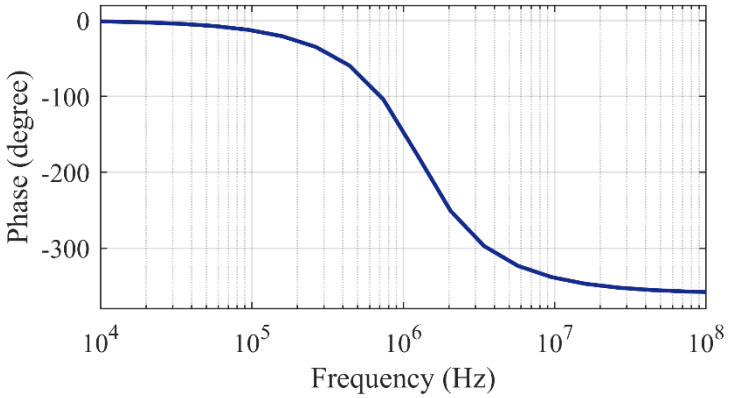

Figure 1.11: Phase Response of APF

1.4 ACTIVE BUILDING BLOCKS:

Active building blocks offer a flexible and effective approach to filter design in electronic circuits, enabling precise signal manipulation and frequency control. Low-pass filters (LPFs), which allow low-frequency signals to pass while attenuating high frequencies, can be constructed using operational amplifiers (op-amps) in combination with resistors and capacitors. Similarly, high-pass filters (HPFs) can be designed with active components to allow high-frequency signals through while suppressing lower ones, offering improved cutoff precision and roll-off characteristics.

Band-pass filters, essential for isolating specific frequency ranges, are often implemented using configurations like multiple feedback (MFB) or state-variable topologies, which allow tuning of center frequencies and bandwidths. Band-stop filters, which reject signals within a specific frequency band while allowing others to pass, also benefit from active component-based designs for enhanced selectivity and performance. Moreover, active building blocks enable the realization of complex filter types such as higher-order filters, elliptic filters, and switched-capacitor filters. These advanced filters offer features like sharp roll-off rates, accurate transition bands, and tunable cutoff frequencies, making them suitable for demanding signal processing applications.

Overall, the use of active building blocks in circuit design provides a robust platform for developing highly customizable and efficient filters. As technology evolves, these components continue to play a pivotal role in advancing electronic system performance across various industries.

Active building blocks refer to electronic components or modules that incorporate active devices such as op-amps, transistors, or voltage/current sources to provide amplification, signal conditioning, or processing capabilities. These building blocks offer distinct advantages over passive components, including:

1. Gain: Active components can provide signal amplification, enabling the design of filters with higher gain levels compared to passive filters.
2. Flexibility: Active building blocks allow for the implementation of complex filter configurations and frequency responses that may be challenging to achieve using passive components alone.
3. Tunability: Active filters provide the flexibility to modify parameters such as cutoff frequency, BW, and gain by adjusting component values or control inputs. This enables easy adaptation to different system demands.
4. Low Sensitivity: Active filters are less sensitive to component variations and parasitic effects, resulting in improved stability and robustness.

5. Integration: Active building blocks can be readily integrated into integrated circuit (IC) technologies, enabling compact and cost-effective solutions for filter design.

The design of various filters using active building blocks typically involves the following steps:

1. Specification: Define the desired filter specifications including frequency response, cutoff frequency, bandwidth, and gain requirements.
2. Topology Selection: Choose a suitable filter topology based on the specified requirements and application constraints. Common filter types include LP, HP, BP and BS.
3. Component Sizing: Determine the component values (resistors, capacitors, etc.) and operating parameters of active devices (op-amps, transistors) based on the selected topology and specifications.
4. Simulation and Optimization: Utilize circuit simulation tools to verify the performance of the designed filter and optimize component values for desired characteristics such as frequency response, passband ripple, and stopband attenuation.
5. Sensitivity Analysis: Conduct sensitivity analysis to examin the impact of component tolerances, temperature variations, and manufacturing variations on filter performance and stability.
6. Prototype Implementation: Build a physical prototype of the designed filter circuit using discrete components or integrated circuits, following best practices for layout and grounding to minimize noise and interference.
7. Performance Evaluation: Test the prototype filter under various operating conditions to evaluate its performance in terms of frequency response, gain, noise, distortion, and stability.
8. Fine-Tuning and Adjustment: Fine-tune the filter circuit parameters if necessary to meet any deviations from the desired specifications, taking into account practical constraints and limitations.

Filters designed using active building blocks find wide-ranging applications across different domains, including:

1. Communication Systems: Active filters are used for frequency shaping, channel selection, and signal conditioning in communication systems such as wireless transceivers, satellite receivers, and base stations.
2. Audio Processing: Active filters are employed in audio equalizers, crossover networks, and tone control circuits for audio processing applications in amplifiers, mixing consoles, and audio recording equipment.

3. Biomedical Instruments: Active filters are utilized in biomedical instrumentation for signal filtering and noise rejection in electrocardiography (ECG), electroencephalography (EEG), and other medical diagnostic systems.
4. Instrumentation and Control: Active filters play a very important role in instrumentation and control systems for signal conditioning, anti-aliasing filtering, and noise reduction in sensors, data acquisition systems, and industrial automation equipment.
5. Automotive Electronics: Active filters are integrated into automotive electronic systems for audio entertainment, engine control, and safety features such as active noise cancellation and adaptive cruise control.
6. Consumer Electronics: Active filters are incorporated into consumer electronic devices such as televisions, smartphones, and portable audio players for audio processing, speaker protection, and noise filtering.

Recent advancements in active building blocks have focused on enhancing performance, efficiency, and integration. These advancements include:

1. High-Speed Op-amps: Op-amps with increased bandwidth and slew rate enable high-speed signal processing in communication and data acquisition systems.
2. Low-Power ICs: Low-power integrated circuits conserve energy and extend battery life in portable electronic devices and IoT applications.
3. Integrated Sensor Interfaces: ICs incorporating sensor interfaces simplify the integration of sensors into electronic systems, enabling IoT, healthcare, and environmental monitoring applications.
4. Programmable Filters: Programmable filter ICs offer configurable filter characteristics, allowing for flexible signal processing in audio, communication, and instrumentation applications.

Analog filters play a vital role in electronics, with widespread applications in high-speed communication, instrumentation, audio systems, control engineering, and electroacoustics [1]. A universal filter is a versatile circuit configuration capable of realizing all five fundamental filter responses: high-pass (HP), low-pass (LP), band-pass (BP), band-stop (BS), and all-pass (AP).

Current-mode active devices have gained significant traction in analog circuit design due to their inherent advantages, including high speed, wide dynamic range, low power consumption, high slew rate, superior linearity, and minimal crosstalk [2]. As a result, numerous universal filter designs based on current-mode active devices have been proposed in the literature. Various current-mode elements have been employed in these designs, such as the differential voltage

current conveyor (DVCC), voltage differencing buffered amplifier (VDBA), extra X current conveyor transconductance amplifier (EXCCTA), current differencing buffered amplifier (CDBA), multiple-output current controlled current conveyor transconductance amplifier (MO-CCCCTA), differential difference current conveyor transconductance amplifier (DDCCTA), four-terminal floating nullor (FTFN), dual X current conveyor differential input transconductance amplifier (DXCCDITA), differential voltage current controlled conveyor transconductance amplifier (DVCCCTA), current controlled differential difference current conveyor transconductance amplifier (CCDDCCTA), operational transconductance amplifier (OTA), second-generation current conveyor (CCII), fully differential second-generation current conveyor (FDCCII), voltage differencing transconductance amplifier (VDTA), differential difference current conveyor (DDCC) [16], extra X current controlled conveyor (EXCCCII), and voltage differencing extra X current conveyor (VD-EXCCII).

In recent years, the Voltage Differencing Current Conveyor (VDCC) has gained attention as a versatile and efficient active building block in analog circuit design. Introduced by Biolek in 2008 [5], the VDCC extends the capabilities of traditional current conveyors by incorporating voltage differencing and electronically tunable transconductance properties within a single device. This enhanced functionality allows the VDCC to serve as a compact and powerful solution for a variety of analog signal processing tasks.

A major advantage of the VDCC is its electronically adjustable transconductance gain, allowing circuit parameters to be tuned in real-time without physically changing components. This capability is especially valuable in adaptive systems and programmable analog circuits that require dynamic control of their response. Moreover, the VDCC features a wide bandwidth, making it well-suited for high-frequency applications such as communication systems and precision instrumentation. Its high accuracy and linearity significantly enhance performance in filter circuits, oscillators, and analog computing devices. Additionally, the VDCC's low power consumption, straightforward design, and compatibility with standard CMOS technology make it an attractive choice for integrated circuit (IC) implementation.

Due to these attributes, the VDCC has been successfully employed in the development of universal filters, oscillators, modulators, and other analog signal processing elements. Its ability to realize all five standard filter responses (low-pass, high-pass, band-pass, band-stop, and all-pass) with minimal component count and high tunability makes it a strong candidate for next-generation analog systems.

1.5 INTRODUCTION TO VDCC:

The Voltage Differencing Current Conveyor (VDCC) is an active versatile building block used in the realization of analog signal processing circuits and analog wave generation [4]. The VDCC represents a specialized type of active device that offers unique advantages over traditional operational amplifiers (op-amps) and other active components. At its core, the VDCC operates based on the concept of voltage differencing, utilizing current conveyor to achieve its functionality. Unlike op-amps which primarily amplify voltage differentials, VDCCs are designed to directly manipulate voltage differences, making them particularly well-suited for applications requiring precise control and manipulation of voltage differentials.

One of the key benefits of utilizing the VDCC as an active component is its ability to enable compact circuit designs in various applications [20]. Unlike many traditional active elements, the VDCC offers dual-value characteristics, which allow it to support a wide range of functions—including biquad filtering, oscillation, inductance simulation, and frequency-dependent negative resistance (FDNR) emulation—using just one or two capacitors [12]. Another significant advantage is its suitability for voltage-mode operations, as it features voltage-driven input terminals and current-driven output terminals [12]. Furthermore, with the growing emphasis on low-power and portable electronic systems, the VDCC stands out as an efficient choice for designers aiming to reduce power consumption without sacrificing analog signal processing performance.

Furthermore, the unique characteristics of VDCCs make them suitable for application in areas such as biomedical instrumentation, sensor interfaces, communication systems, and audio processing. Their ability to accurately process small signals and maintain linearity over a wide dynamic range makes them invaluable in these domains.

In summary, VDCCs represent a significant advancement in active device technology, offering unparalleled versatility, precision, and efficiency in analog signal processing applications. As the demand for high-performance analog circuits continues to grow, VDCCs are poised to play a central role in meeting the evolving needs of the electronics industry. At its heart, the VDCC operates by managing voltage differences, utilizing current conveyor. This sets it apart from op-amps, which primarily focus on amplifying voltage differentials. This unique design makes VDCCs ideal for applications requiring precise manipulation and control of voltage variations.

Their distinctive traits make VDCCs well-suited for diverse applications such as biomedical instrumentation, sensor interfaces, communication systems, and audio processing. Their ability to accurately handle small signals while maintaining linearity across a broad dynamic range positions them as invaluable assets in these fields. In essence, VDCCs signify a substantial leap forward in active device technology, delivering unmatched versatility, precision, and efficiency in analog signal processing. With the continuous growth in demand for high-performance analog circuits, VDCCs are poised to play a pivotal role in addressing the evolving requirements of the electronics industry.

1.6 VDCC HISTORY:

The Voltage Differencing Current Conveyor (VDCC) is a type of current conveyor that has evolved over time as part of the broader development of active circuit elements used in analog signal processing. Here's a brief history of VDCCs and the key milestones leading to their development.

The concept of current conveyors (CC) was introduced by R.J. Elliott (1957), who developed the first current conveyor, which became known as the First-Generation Current Conveyor (CC-1)**.** The CC-1 was primarily used to transfer current between different parts of a circuit while maintaining the voltage at the input terminal. CC-1s were widely used in applications like analog filters and amplifiers. Over time, the need for improved performance led to new types of current conveyors, and eventually the Voltage Differencing Current Conveyor (VDCC) emerged.

The VDCC concept was introduced by Sedra and Smith in the late 1970s and early 1980s as an extension of the earlier current conveyor ideas. The VDCC is designed to handle both voltage and current differently compared to earlier generations of current conveyors. The development of VDCCs continued as research into current-mode analog circuits gained traction, particularly in the fields of active filters**,** oscillators**,** and signal processors. VDCCs became particularly important in designing high-performance analog filters and signal processors due to their ability to operate efficiently with low power and high precision.

Today, research into VDCCs has focused on improving their linearity**,** bandwidth, and power consumption, which is crucial for modern wireless communication and low-power analog systems. Advanced modelling and simulation techniques are used to better understand and optimize VDCC circuits.

- 1957: Introduction of the first current conveyor by R. J. Elliott.
- Late 1970s - 1980s: Development of advanced current conveyor types, including the VDCC, by researchers like Sedra and Smith.
- 1990s - 2000s: Increased use of VDCCs in analog signal processing, especially for filters, oscillators, and communication systems.
- 2010s - Present: Ongoing improvements in VDCC-based circuit design, including low- power, high-performance applications in RF and mixed-signal systems.

The Voltage Differencing Current Conveyor (VDCC) has evolved from the early ideas of current conveyors, becoming an important active element for modern analog and signal processing circuits. Its ability to handle both voltage and current in a highly efficient and scalable manner has made it a valuable tool for a wide range of applications, from telecommunications to biomedical electronics. As technology advances, VDCCs continue to play a key role in the design of more sophisticated, low-power, high-performance analog circuits.

1.7 VDCC SYMBOLIC REPRESENTATION:

As illustrated in Fig. 1, the VDCC is a six-terminal device. Among these, P and N serve as the input terminals, while Z, X, W_N and W_P function as output terminals. Except for the X terminal, all other terminals exhibit high impedance. The behaviour of the VDCC is described by the characteristic equation provided in (1.12).

$$\begin{bmatrix} I_p \\ I_n \\ I_z \\ V_z \\ I_{wp} \\ I_{wn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ I_X \end{bmatrix} \tag{1.12}$$

I_P, I_N, I_Z, I_X, I_{WN} and I_{WP} represents the current at P, N, Z, X, W_P, W_N respectively and V_N, V_P, V_Z, V_X are the voltage at N, P, Z, X respectively. Transconductance gain, represented by g_m, is achieved by modulating the bias current of the VDCC.

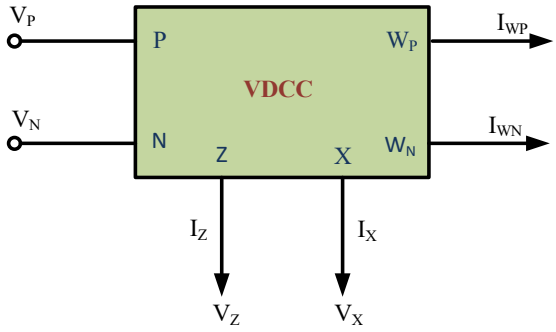

Figure 1.12: Basic symbol of VDCC

The transconductance gain, represented by g_m, is adjustable via electronic control, achieved by modulating the bias current of the VDCC. g_m is defined by equation (1.13).

$$gm = \sqrt{I_{B1}\mu_1 C_{ox}\left(\frac{w}{l}\right)} \quad \ldots (1.13)$$

where μ_n represents the carrier mobility in NMOS transistors, C_{ox} is the gate-oxide capacitance per unit area, W denotes the effective channel width, L is the effective channel length, and I_{B1} is the bias current.

1.8 VDCC ANALYSIS:

The Voltage Differencing Current Conveyor (VDCC) has a number of important characteristics that define its behavior and make it useful in various analog signal processing applications. Below are the key characteristics and their results for the ideal and practical VDCCs:

1. Current Output Proportional to Voltage Difference

The most fundamental characteristic of a VDCC is its ability to produce a current at the output (Z) that is proportional to the difference between the voltages at the two input terminals (N and P).

$$I_Z = g_m (V_P - V_N) \quad (1.14)$$

Where:

- I_Z is the output current at terminal Z.
- V_P is the voltage at terminal P (the positive input).
- V_N is the voltage at terminal N (the negative input).

- g_m is the transconductance gain of an ideal VDCC.

2. High Input Impedance

- The input terminals (P and N) of a VDCC ideally exhibit high impedance. This means the current entering the VDCC from the P and N terminals is ideally zero (no loading on the source).
- This makes the VDCC suitable for interfacing with high-impedance sources, as it does not significantly affect the voltages at the inputs.

- The input current at both terminals I_P and I_N is ideally zero:

$$I_P = I_N = 0 \tag{1.15}$$

- The input impedance of both X and Y is ideally infinite.

3. Output Current Controlled by Voltage Difference

The VDCC has an output current at the Z terminal that is directly influenced by the voltage difference between the X and Y terminals.

The output current is linearly proportional to the input voltage difference $V_P - V_N$, as given by the equation:

$$I_Z = g_m (V_P - V_N) \tag{1.16}$$

4. High Output Impedance

The output terminal (Z) of the VDCC has high output impedance. This means that the current output at Z is relatively independent of the load at the output terminal.

Ideal Output Impedance:

- The output impedance at the Z terminal is ideally infinite, which means the VDCC behaves like a current source, and the output current does not change with varying load resistance at the Z terminal.

Practical Results:

- In real-world VDCCs, the output impedance is large but finite, and there might be some dependence on the load resistance. However, in many applications, this high output impedance is still desirable.

5. Voltage at the Z Terminal

For an ideal VDCC, the voltage at the Z terminal is typically not defined or is considered to be floating since the current is the primary output. The VDCC is a current-mode device, so voltage levels at the Z terminal are not directly controlled by the device itself.

Ideal Behavior:

- The voltage at the Z terminal (denoted as $V_Z$is not determined by the VDCC; it depends on the external load and circuit configuration.
- The current mode of operation allows the VDCC to interface with other current-mode devices or circuits, where voltage levels are not as critical.

6. Bandwidth and Slew Rate

VDCCs can operate over a broad frequency range, making them suitable for high-frequency applications such as active filters and analog signal processing. The frequency response depends on the internal components of the VDCC (e.g., transistors, capacitors), and non-ideal effects may reduce the bandwidth.

Practical Behavior:

- The bandwidth of a VDCC is typically high, but it is limited by the internal bandwidth of the components.
- The slew rate (the rate of change of the output current with respect to time) is also finite and may be influenced by the power supply and design constraints of the VDCC.

7. Linearity and Distortion

For an ideal VDCC, the relationship between the input voltage difference $V_P - V_N$ and the output current I_Z is perfectly linear, meaning there is no distortion. However, in practical VDCCs, nonlinearities and parasitic effects may arise due to the limitations of real components.

Practical Results:

- In practical devices, there may be nonlinearities at very high input voltage differences or large currents, which can lead to distortion in the output current.
- However, VDCCs are designed to minimize these nonlinearities, and the linear region is typically broad enough for most applications.

8. Power Supply Sensitivity

VDCCs, like most analog components, rely on power supplies for proper operation. In real-world VDCCs, the output current and behavior can be affected by the power supply voltage and quality.

Practical Behavior:

- A stable power supply is essential to ensure the VDCC operates correctly, and fluctuations in supply voltage may cause errors or instability in the current output.
- In most cases, VDCCs are designed with rail-to-rail operation or with a wide supply range to accommodate variations in voltage.

Table.1.1. Summary of Key Results for VDCCs:

Characteristic	Ideal VDCC Behaviour	Practical VDCC Behaviour
Input Current	$I_P = I_N = 0$ (High impedance)	High impedance, very small current
Output Current	$I_Z = g_m (V_P - V_N)$	Linear relationship, with some deviations at extremes
Input Voltage	No specific voltage at P or N	Voltage difference $V_P - V_N$ controls current
Output Impedance	Infinite	Large, but finite
Bandwidth	Ideal: Infinite	Dependent on design, may have limits
Slew Rate	Ideal: Infinite	Finite, depending on components
Linearity	Perfectly linear	Some nonlinearity at extremes
Power Supply Sensitivity	Independent of supply voltage	Sensitive to power supply quality and range

1.9 CMOS IMPLEMENTATION OF VDCC:

To validate the operation of the proposed circuit in PSPICE simulation utilizing TSMC 0.18um CMOS technology was performed. The design of a VDCC circuit

utilizing CMOS technology in PSpice is illustrated in fig.3.2. In the fig.3.2, a transconductance amplifier comprised of transistors M_1 to M_8 is also depicted. The current conveyor is composed of transistors M_9 to M_{22} in the fig.3.2. The direct current external bias is represented by I_{B1} and I_{B2}. The power supply voltages were configured as $V_{DD} = -V_{SS}$.

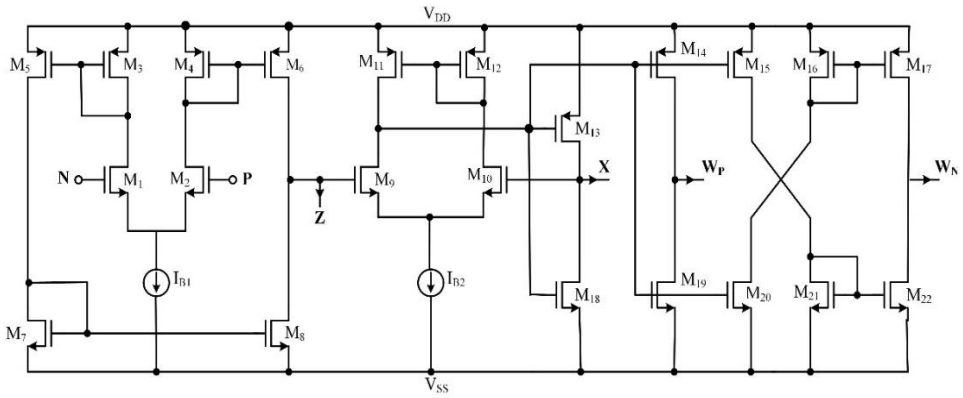

Figure 1.13: CMOS implementation[23] of the VDCC

Finally, a CMOS realization of a VDCC element[23] is shown in Fig. The supply voltages and biasing currents are given by

$$V_{DD}=-V_{SS}=0.9\text{V} \tag{1.17}$$

$$I_{B1}=50\ \mu\text{A} \tag{1.18}$$

$$I_{B2}=100\ \mu\text{A} \tag{1.19}$$

The aspect ratios of the transistors are given[23] in the table below. The MOS transistors are simulated using TSMC CMOS 0.18µm process model parameters.

Table 1.2: Aspect ratios of the CMOS devices.[10]

CMOS Transistor	W(µm)	L(µm)
M1-M4	3.6	1.8
M5, M6	7.2	1.8
M7, M8	2.4	1.8
M9-M10	3.06	1.72
M11, M12	9.0	1.72
M13-M17	14.4	1.72
M18-M22	0.72	0.72

1.10 DC CHARACTERISTICS OF VDCC:

The DC characteristics of a Voltage Differencing Current Conveyor (VDCC) can be illustrated by plotting how various terminal voltages and currents behave under DC conditions. A VDCC is an active building block used in analog signal processing, and its DC behaviour is typically described by its terminal relations and corresponding ideal characteristics.

A typical VDCC has the following terminals:

- V_P and V_N: High-impedance voltage input terminals
- X: A terminal where the current from (V_P - V_N) is conveyed; voltage-controlled current source behaviour
- Z: High-impedance output terminal, which mirrors the current from X

For an ideal VDCC, the relations are:

- $V_X = V_P - V_N$
- $I_P = I_N = 0$ (high-impedance input)
- $I_Z = I_X$

1.10.1. V_X vs $V_P - V_N$

- A straight line with a slope of 1 passing through the origin.
- Represents the voltage difference applied at the input being transferred to node X.

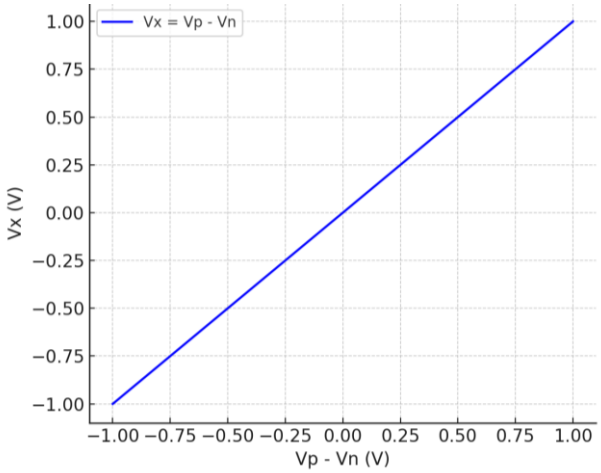

Figure 1.14: DC Characteristic (V_X vs $V_P - V_N$) of the VDCC

1.10.2. Iz vs Vx

- A linear response showing how current at Z changes with voltage at X.
- The slope depends on the transconductance (in practical devices); for an ideal device, the slope is determined by how X controls the current to Z.

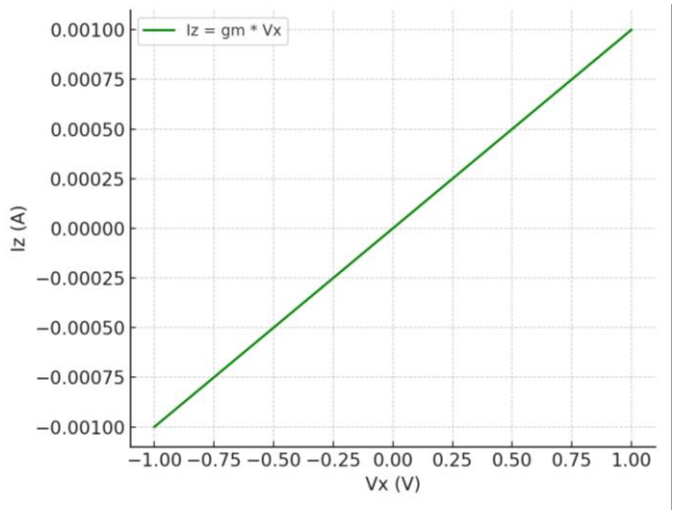

Figure 1.15: DC Characteristic (I_Z vs V_X) of the VDCC

1.10.3 I_X and -I_X vs V_X

- For a linear VDCC, this would be a straight line (ohmic behaviour) if internal resistance exists.
- In ideal case, it's defined by connected load or controlled element.

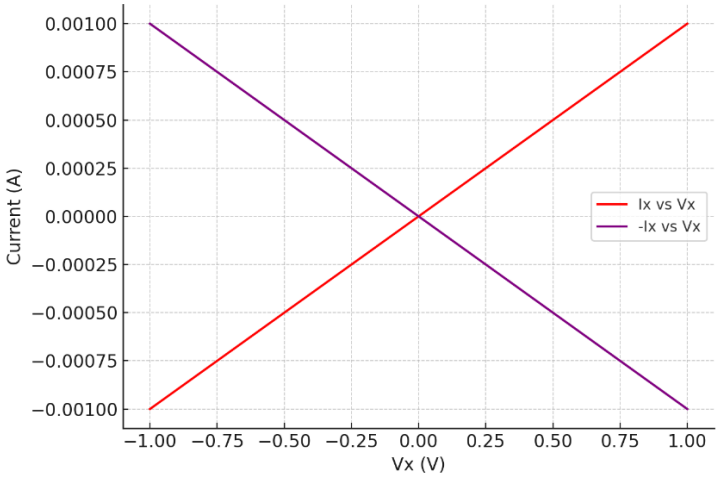

Figure 1.16: DC Characteristic (I_X and $-I_X$ vs V_X) of the VDCC

1.11 SCOPE OF WORK:

The aim of the thesis includes the design, analysis, simulation, and implementation of a voltage-mode multi input single output biquad filter utilizing CMOS based VDCC. The proposed filter configuration offers flexibility and adaptability by providing multiple voltage mode, transadmittance mode, and current mode functions, including low-pass, high-pass, band-pass, band stop and all pass responses.

Key aspects of the scope include:

1. Design: The thesis involves the design of the voltage-mode MISO biquad filter architecture based on VDCC. This includes the selection of appropriate circuit topologies, component values, and operational modes to achieve the desired filter functions and characteristics.
2. Analysis: A comprehensive analysis of the proposed filter configuration is conducted to understand its operational principles, performance characteristics, and feasibility for integration into a single integrated circuit (IC). This involves mathematical analysis, transfer function derivation, and stability analysis of the filter.
3. Simulation: PSPICE simulations are employed to validate the feasibility and performance of the proposed biquad filter configuration. Simulations are performed using the 0.18µm TSMC CMOS process specifications to ensure compatibility with standard semiconductor manufacturing processes.

Overall, the thesis aims to demonstrate the feasibility and effectiveness of the proposed voltage-mode MISO biquad filter based on VDCC through comprehensive design, analysis, simulation, and implementation efforts. A comparative analysis is done of proposed biquad filter with the previously published biquad filters structures. The implementation and analysis of the proposed work is discussed in the following chapters.

CHAPTER 2

2. LITERATURE REVIEW

The Voltage Differencing Current Conveyor (VDCC) is an advanced active building block that has gained considerable attention in analog signal processing since its introduction. VDCC extends the capabilities of the conventional current conveyor (CC) and current differencing buffered amplifier (CDBA) by integrating the functionality of voltage differencing and current conveyance into a single device, enabling enhanced performance in terms of bandwidth, linearity, and design simplicity.

The VDCC was introduced as an improvement over traditional current conveyors (CCI, CCII, CCIII), current differencing transconductance amplifiers (CDTA), and CDBAs, to overcome their limitations in high-frequency operation and design flexibility. As report in [4], VDCCs offer low-input impedance and high-output impedance characteristics, making them well-suited for voltage-mode, current-mode, and mixed-mode applications. The distinguishing feature of VDCCs is their ability to accept two input voltages and convey the difference to the output terminals through a current conveyor mechanism.

A typical VDCC consists of a voltage differencing unit followed by a second-generation current conveyor (CCII). The device has two high-impedance voltage inputs V_P and V_N, which are subtracted internally, and the result appears as a current at the Z terminal. The intrinsic properties of VDCC include high bandwidth, low power consumption, and tunability, which are critical for high-frequency analog design. The performance of VDCCs is highly dependent on the underlying CMOS technology and biasing schemes. Various CMOS implementations have been proposed in literature to optimize linearity, power dissipation, and frequency response [5].

2.1 CIRCUIT TOPOLOGIES UTILIZING VDCCs:

This section delves into the application of Voltage Differencing Current Conveyor (VDCCs) in various analog signal processing circuits, as documented in existing literature [6-13]. These circuits encompass a wide range of functionalities crucial for signal processing, including oscillators, simulators for inductance, capacitance, and resistance, analog computation as well as filters operating in different modes such as VM, CM and TAM.

VDCCs have been widely applied in the design of analog signal processing circuits, including:

- Filters: Numerous voltage-mode and current-mode filters have been developed using VDCCs, offering advantages such as tunability, reduced component count, and electronic controllability. For example, in [6] Jaikla et al. (2010) demonstrated voltage-mode biquad filters with orthogonal tuning capabilities using a single VDCC.
- Oscillators: VDCCs have been used to implement quadrature oscillators and sinusoidal oscillators with minimal component usage and good frequency stability [7].
- Analog computation: Due to their current-mode operation and high-frequency characteristics, VDCCs are suitable for analog computing elements like integrators, differentiators, and analog multipliers.
- Impedance simulators: Several works have demonstrated floating and grounded impedance simulators using VDCCs, which are useful in sensor interface circuits and analog front-end designs.

2.2 ANALYSIS OF CIRCUITS USING VDCC:

This section presents the analysis of various circuits utilizing the Voltage Differencing Transconductance Amplifier (VDTA). In reference [8], three new voltage-mode universal biquad filters are introduced. The filter topology illustrated in Fig. 3.1 represents a compact configuration that employs only the VDCC element. This filter operates as a three-input single-output (TISO) voltage-mode filter, as depicted in Fig. 3.1.

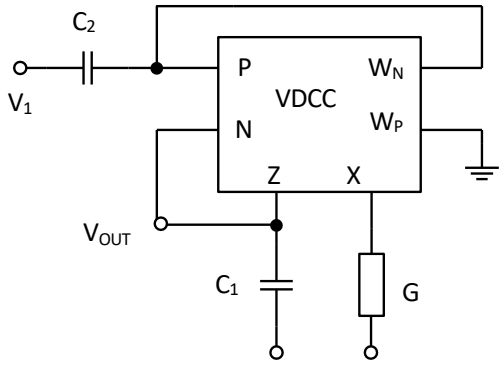

Figure 2.1: TISO biquad filter [8]

Circuit analysis yields the following for the output voltage which can be expressed as:

$$V_{out} = \frac{V_2 s^2 C_1 C_2 + V_1 s C_2 g_m + V_3 g_m G}{s^2 C_1 C_2 + s C_2 g_m + g_m G} \tag{2.1}$$

Depending on the voltage levels of V_1, V_2 and V_3 in the numerator of Eq. (2.1), one of the following five filter functions can be realized:

(i) LP: $V_1 = V_2 = 0$, $V_3 = V_{IN}$
(ii) BP: $V_2 = V_3 = 0$, $V_1 = V_{IN}$
(iii) HP: $V_1 = V_3 = 0$, $V_2 = V_{IN}$
(iv) BS: $V_1 = 0$, $V_2 = V_3 = V_{IN}$
(v) AP: $V_2 = V_3 =$ □ $V_1 = V_{IN}$

The circuit of quality factor (Q) and pole frequency (ω_0) can be given as follows:

$$Q = \sqrt{\frac{GC_1}{g_m C_2}} \tag{2.2}$$

$$w_o = \sqrt{\frac{g_m}{C_1 R_1 C_2}} \tag{2.3}$$

Two other single-input dual-output (SIDO) voltage-mode multifunction filters, each utilizing a single Voltage Differencing Current Conveyor (VDCC), are presented in Fig. 2.2. Both configurations employ two capacitors and two resistors. The first SIDO voltage-mode multifunction filter is illustrated in Fig. 2.2, while the second is shown in Fig. 2.3.

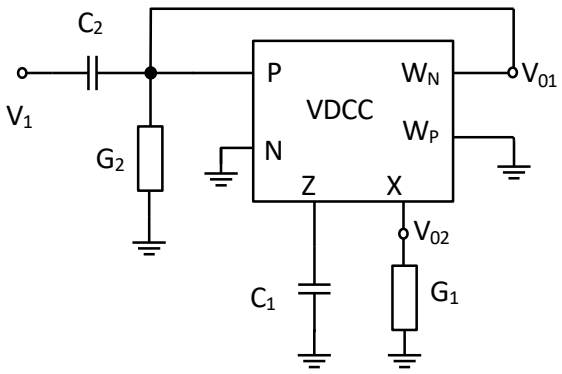

Figure 2.2: SIDO biquad filters [8]

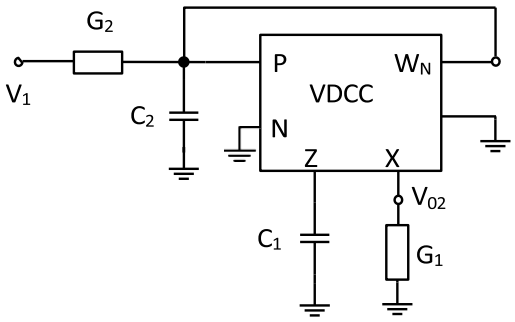

Figure 2.3: SIDO biquad filters [8]

The filter circuit proposed in [9] is shown in Fig. 2.4. It comprises a single VDCC, one resistor, and two capacitors. The circuit has three input voltages V_{in1}, V_{in2} and V_{in3} and a single output voltage V_{out}. A straightforward analysis of the proposed filter, based on Eq. (2.4), yields the following expression for the output voltage:

$$T(s) = \frac{s^2 V_2 + \left(\frac{s}{R_1 C_2}\right) V_3 + \left(\frac{g_m}{R_1 C_1 C_2}\right) V_1}{s^2 + \left(\frac{s}{R_1 C_2}\right) + \left(\frac{g_m}{R_1 C_1 C_2}\right)} \tag{2.4}$$

According to eq. (2.4), the natural frequency and the quality factor is given as

$$w_o = \sqrt{\frac{g_m}{C_1 R_1 C_2}} \tag{2.5}$$

$$Q = \sqrt{\frac{C_2}{g_m C_1 R}} \tag{2.6}$$

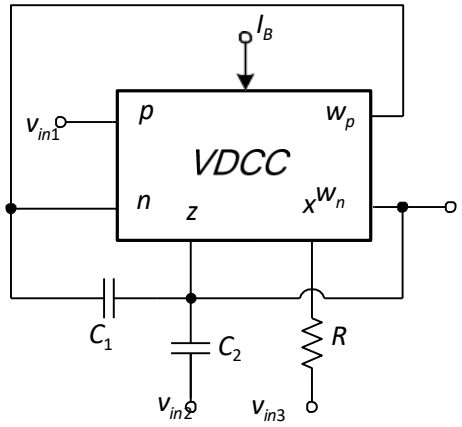

Figure 2.4. TISO Voltage-Mode Biquad universal filter [9]

A single-VDCC-based voltage-mode first-order all-pass filter (APF) with electronic controllability is presented in [11]. The proposed APF consists of one VDCC as the active component, along with two resistors and a grounded capacitor, as shown in Fig. 2.5. The circuit features a single input voltage node (V_{in}) and a single output voltage node (V_{out}). To achieve high input impedance in the proposed voltage-mode first-order APF, the resistance value should be sufficiently large. The voltage transfer function of the proposed filter is given by:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{g_m - sC}{g_m + sC} \tag{2.7}$$

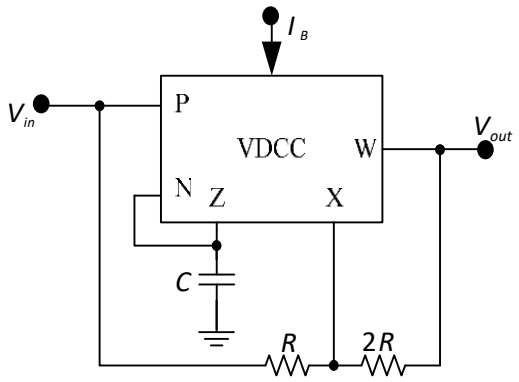

Figure 2.5: The Voltage-Mode first order APF [11]

From (2.7), the proposed circuit yields unit voltage gain. The phase respoinse of the presented APF is obtained by

$$\theta = -2\tan^{-1}\left(\frac{\omega C}{g_m}\right) \tag{2.8}$$

The pole frequency ω0 and voltage gain of the proposed first order all-pass filter are respectively given by

$$\omega_o = \frac{g_m}{C} \tag{2.9}$$

An electronically tunable universal biquad filter using a single active component is proposed in [12]. The universal voltage-mode circuit consists of only one VDCC, two capacitors, and two resistors, as illustrated in Fig. 2.6. A standard analysis of the filter shown in Fig. 2.6 yields the following transfer functions simultaneously:

$$H_{LP}(s) = \frac{V_{o1}}{V_{in}} = \frac{\alpha\mu g_m / R_2 C_1 C_2}{D(s)} \tag{2.10}$$

$$H_{BP}(s) = \frac{V_{o2}}{V_{in}} = \frac{s(\alpha\mu g_m / C_2)}{D(s)} \tag{2.11}$$

$$H_{HP}(s) = \frac{V_{o3}}{V_{in}} = \frac{s^2}{D(s)} \tag{2.12}$$

$$H_{NF}(s) = \frac{V_{o4}}{V_{in}} = \frac{s^2 + \alpha\mu g_m / R_2 C_1 C_2}{D(s)} \tag{2.13}$$

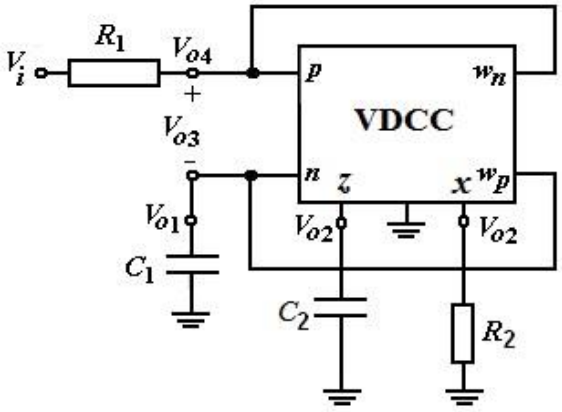

Figure 2.6: Voltage-Mode Universal Filter [12]

A single-VDCC-based notch filter has been implemented in [13], as shown in Fig. 2.7. This design utilizes two capacitors and two resistors as passive components, along with a VDCC serving as the active element. The transfer function of the filter, derived through standard analysis of Fig. 2.7, is given as follows:

$$\frac{V_o}{V_{in}} = \frac{s^2 + \dfrac{g_m}{C_1 C_2 R_1}}{s^2 + s\dfrac{1}{R_1 C_2} + \dfrac{g_m}{C_1 C_2 R_1}} \tag{2.14}$$

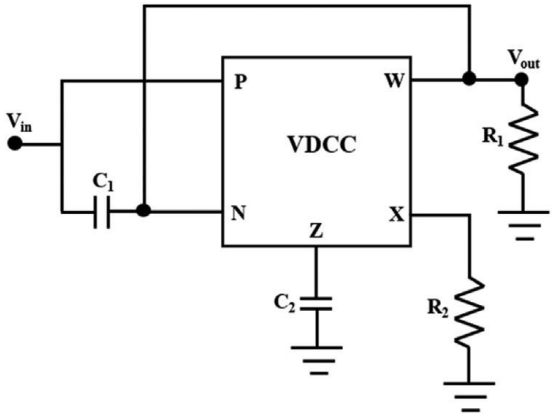

Figure 2.7**:** Circuit of a single VDCC-based notch filter [13]

The notch filter of second-order can be expressed as:

$$H(s) = \frac{s^2 + \omega_o^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} \tag{2.15}$$

From the above equations (2.14 and 2.15), the system parameters of the proposed circuit, namely, ω_o and Q of this notch filter are given by:

$$Q = \sqrt{\frac{g_m R_1 C_2}{C_1}} \tag{2.16}$$

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{2.17}$$

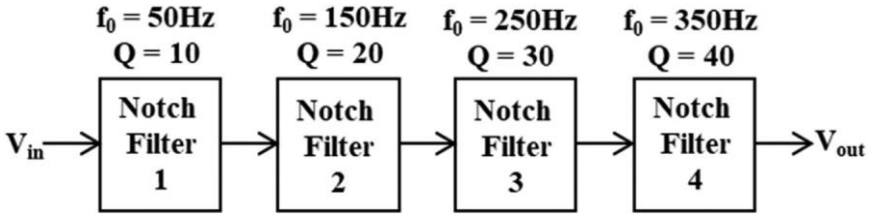

Figure 2.8**:** Methodology to design analog comb filter. [13]

As an application example of the VDCC, the quadrature sinusoidal oscillator described in [11] is considered. The oscillator is constructed by cascading an inverting lossless integrator with a first-order all-pass filter, as depicted in Fig. 2.10. The inverting lossless integrator, shown in Fig. 2.9, employs a single VDCC along with a grounded capacitor. The voltage transfer function for this integrator is derived as follows:

$$\mathrm{T(s)} = \frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{\mathrm{g_{m2}}}{\mathrm{sC_2}} \tag{2.18}$$

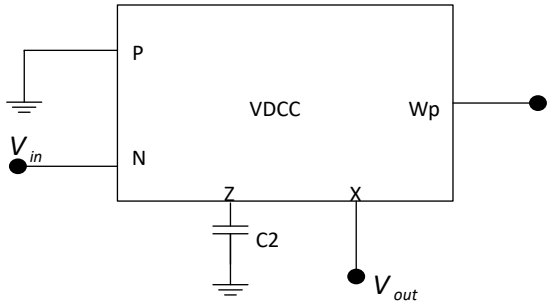

Figure 2.9: The voltage mode non-inverting lossless integrator based on VDCC.[11]

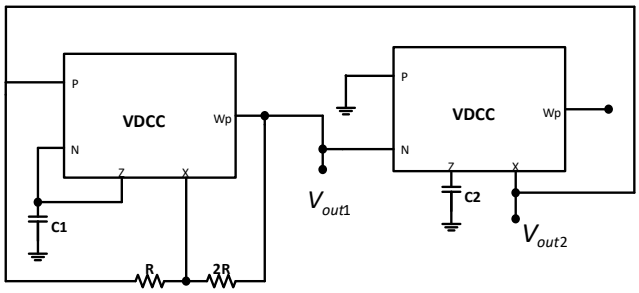

Figure 2.10. The voltage mode quadrature sinusoidal oscillator. [11]

By performing a standard analysis of the voltage-mode quadrature sinusoidal oscillator depicted in Fig. 2.10, the characteristic equation is obtained as follows:

$$s^2C_1C_2 + sC_2g_{m1} - sC_1g_{m2} + g_{m1}g_{m2} = 0 \qquad (2.18)$$

From (2.18), the frequency of oscillation (FO) can be achieved by

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \qquad (2.19)$$

2.3 DIFFERENT METHODS OF IMPLIMENTATION OF VDCC:

The most common implementation of the VDCC is based on CMOS technology. A CMOS realization of the VDCC, as presented in [9], is illustrated in Fig. 2.11. The circuit operates with supply voltages of V_{DD}=−V_{SS}=0.9 V, and biasing currents I_{B1}=50 µA and I_{B2}=100 µA. The transistor aspect ratios are listed in Table 3.1. The MOS transistors have been simulated using the TSMC 0.18 µm CMOS process model parameters.

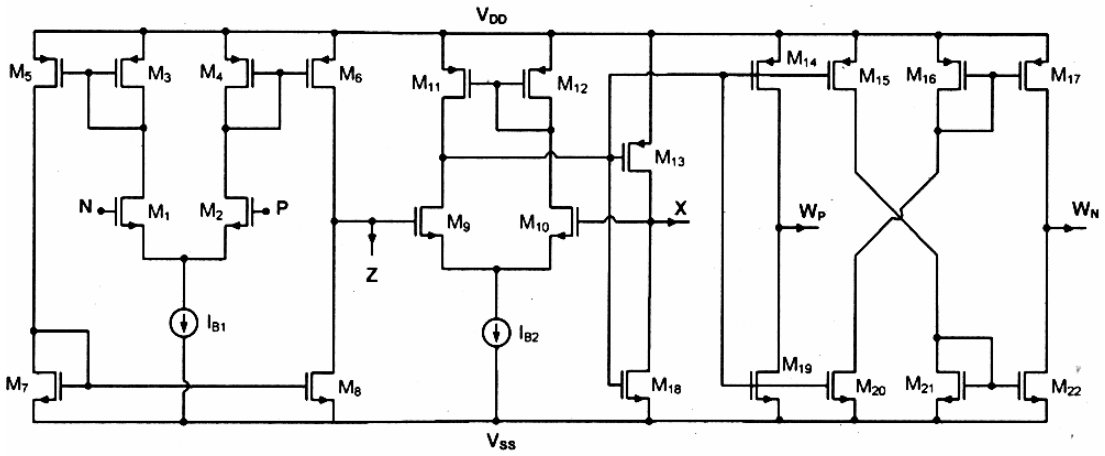

Figure 2.11: CMOS implementation of the VDCC [9]

Table 2.1: Aspect ratios of the CMOS devices.

CMOS Transistor	W(μm)	L(μm)
M1-M4	3.6	1.8
M5, M6	7.2	1.8
M7, M8	2.4	1.8
M9-M10	3.06	1.72
M11, M12	9.0	1.72
M13-M17	14.4	1.72
M18-M22	0.72	0.72

he VDCC in this design [11] is realized using commercially available ICs, specifically the LM13700 and AD844, as illustrated in Fig. 2.11. This setup features only the signal W terminal. The transconductance gain, g_m, for this configuration is given by:

$$g_m = \frac{I_B}{2V_T} \tag{2.20}$$

where VT is the thermal voltage.

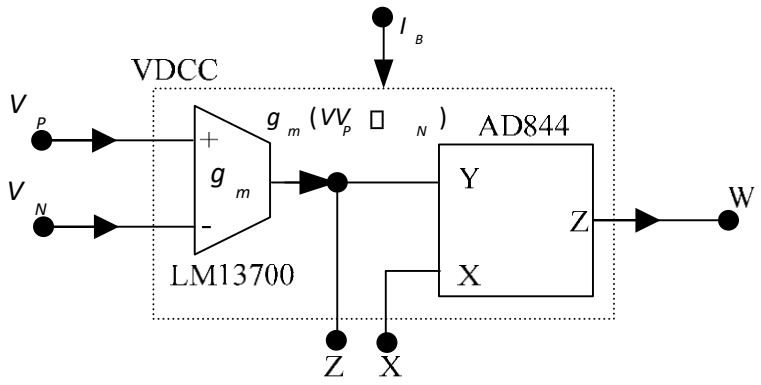

Figure 2.11: VDCC implementation from available ICs, LM13700 and AD844[11].

The BJT implementation of the VDCC, which includes a current-controlled current conveyor and a simple transconductance section, is presented in [12] and shown in Fig. 2.12. This implementation is achieved by properly connecting the outputs of these two sections.

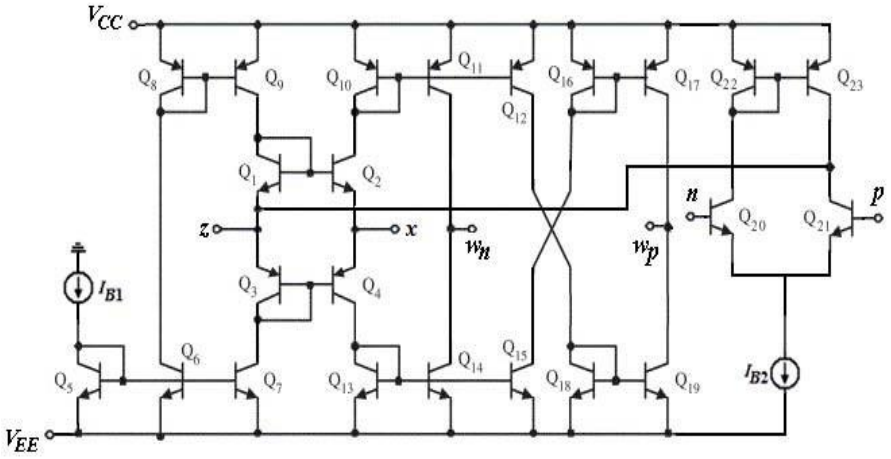

Figure 2.12: BJT implementation of the VDCC [12].

An IC-based Implementation of VDCC using an OTA ICMAX435 and a CFOA IC AD844, as shown in Fig.2.13 is used as hardware implementation also.

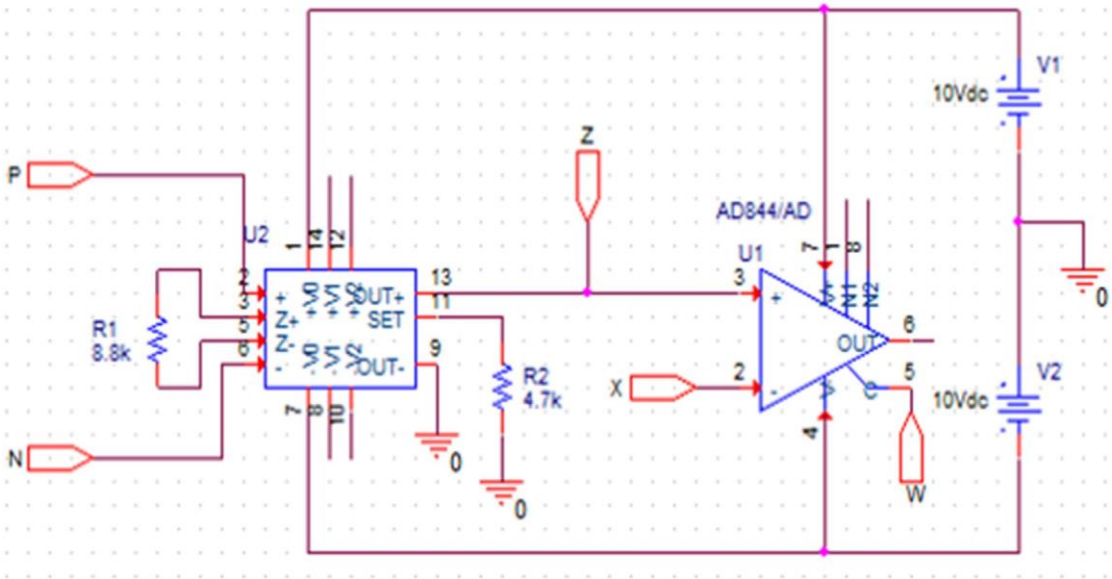

Figure 2.13. VDCC Implementation using ICs MAX435 and AD844 [13].

2.4 COMPARITIVE ANALYSIS:

Voltage Differencing Current Conveyor (VDCC)-based filters have garnered significant attention in analog signal processing due to their numerous advantages over traditional filter designs. However, like any technology, they come with their own set of challenges and trade-offs. A comprehensive understanding of both their strengths and limitations is crucial for effective implementation in various applications.

2.4.1 Advantages of VDCC-Based Filters

1. Broad Frequency Range: VDCC-based filters are capable of operating over a wide frequency spectrum, making them suitable for applications ranging from audio processing to radio frequency (RF) communications.

2. High Linearity: The inherent design of VDCCs ensures a linear relationship between input and output, which is essential for maintaining signal integrity in analog processing.

3. Versatility in Filter Configurations: VDCCs can be configured to realize various filter responses, including low-pass, high-pass, band-pass, band-stop, and all-pass filters. This adaptability allows for the design of multifunctional filter circuits using a single active component.

4. Reduced Component Count: By leveraging the multifunctionality of VDCCs, designers can achieve desired filter responses with fewer active and passive components, leading to simplified circuit layouts and potential cost savings.

5. Electronic Tunability: The transconductance parameter (g_m) of VDCCs can be electronically adjusted, facilitating real-time tuning of filter characteristics such as center frequency and quality factor without the need for physical component changes.

In conclusion, VDCC-based filters offer a compelling solution for modern analog signal processing needs, providing flexibility, efficiency, and adaptability. However, designers must carefully consider the associated challenges, particularly regarding parasitic effects and design complexity, to fully leverage the benefits of VDCCs in practical applications.

Table 2.2: Comparison between Traditional Filter Design and VDCC Filter Design.

Feature	**VDCC-Based Filters**	**Traditional Filters**
Frequency Range	Wide	Moderate
Linearity	High	Variable
Component Count	Low	High
Electronic Tunability	Yes	Limited
Design Complexity	High	Moderate
Susceptibility to Parasitics	High	Lower
Voltage Swing	Limited	Higher

VDCC-based filters offer significant advantages in terms of wide frequency range, high linearity, versatility, and reduced component count compared to traditional approaches. However, they also have limitations and trade-offs, including limited availability, sensitivity to parasitic effects, design complexity, and voltage swing limitations. Understanding these factors is essential for effectively designing and deploying VDCC-based filters in various signal processing applications. A thorough comparison of previously published structures with the presented configuration is provided in Table 2.3.

Table 2.3: Comparison between various multifunction VM biquad filers using VDCC as an active element.

Ref	Mode	Filtering Category	No. of VDCC	Technology	No. of R+C	All grounded passive element only	Filtering Functions
[8]	VM	MISO (Fig. 2)	1	0.18 µm CMOS & ICs	1+2	No	LP, HP, BP, BR, AP
	VM	SIMO (Fig. 3(a)	1	0.18 µm CMOS	2+2	No	HP, BP
	VM	SIMO (Fig. 3(b)	1	0.18 µm CMOS	2+2	No	LP, BP
[9]	VM	MISO	1	0.18 µm CMOS & ICs	1+2	No	LP, HP, BP, BR, AP
[10]	VM	SISO	2	0.18 µm CMOS	5+2	Yes	BP
[11]	VM	SISO	1	0.18 µm CMOS & ICs	2+1	No	AP
[12]	VM	SIMO	1	HFA3127, HFA3128 BJT	2+2	No	LP, HP, BP, BR, AP
[13]	VM	SISO	1	0.18 µm CMOS & ICs	2+2	No	BR
Proposed circuit (1)	VM	MISO	1	0.18 µm CMOS	1+2	No	LP, HP, BP, BR, AP
Proposed circuit (2)	VM	MISO	1	0.18 µm CMOS	2+2	No	LP, HP, BP, BS, AP

CHAPTER 3

3. PROPOSED WORK AND SIMULATION RESULTS

In this thesis, we introduce a novel methodology for analog filter design based on the Voltage Differencing Current Conveyor (VDCC), a modern and highly versatile active building block in analog circuit design. Unlike conventional operational amplifiers, VDCCs exhibit several intrinsic advantages, such as a high gain-bandwidth product, low power consumption, reduced voltage operation, and exceptional flexibility in signal processing tasks. These attributes make VDCCs especially suitable for designing efficient and high-performance analog filters.

The core objective of this research is to explore the design, implementation, and optimization of filter circuits that utilize VDCCs as the primary active components. We propose a comprehensive framework for developing a wide range of filter types, including low-pass (LP), high-pass (HP), band-pass (BP), and band-stop (BS) configurations. By carefully tailoring the circuit topology to leverage the unique properties of VDCCs, we demonstrate how improved frequency selectivity, wider bandwidth, and increased dynamic range can be achieved compared to traditional filter designs.

The thesis delves into both theoretical analysis and practical implementation, providing detailed insights into circuit behaviour, design parameters, and performance characteristics. Furthermore, we highlight the adaptability of VDCC-based filters across various application domains, such as communication systems, audio signal processing, biomedical instrumentation, and other areas where precise and efficient analog filtering is essential.

Overall, this work represents a significant advancement in analog filter design methodology. The proposed VDCC-based circuits not only improve upon existing performance benchmarks but also open new avenues for innovation in analog signal processing. Through this research, we aim to contribute meaningfully to the field of analog electronics and support the wider adoption of VDCC-based architectures in real-world applications.

3.1 REALIZATION OF UNIVERSAL BI-QUAD FILTERS USING FIRST PROPOSED CIRCUIT CONFIGURATION:

The proposed filter used a single VDCC and three passive components (two capacitor and one resistor) is demonstrated in Fig.3.1. The transfer function of the proposed filter is given by:

$$V_o = \frac{s^2 V_{in2} + s\frac{1}{R_1 C_2} V_{in3} + \frac{g_m}{C_1 C_2 R_1} V_{in1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.1}$$

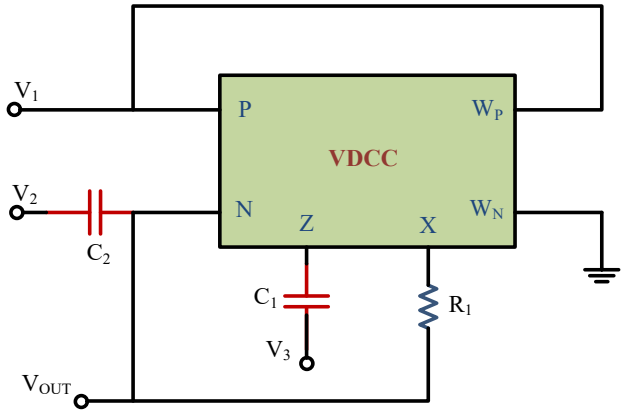

Figure 3.1: Circuit of Realised Universal Filters using VDCC.

Depending upon the voltage status of V_1, V_2 and V_3 in the above equation one of the following five filter functions is realized.

1. For LPF, $V_3 = V_2 = 0$ and $V_1 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{\frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.2}$$

2. For HPF, $V_3 = V_1 = 0$ and $V_2 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.3}$$

3. For BPF, $V_2 = V_1 = 0$ and $V_3 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s\frac{1}{R_1 C_2}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.4}$$

4. For BSF, $V_3 = 0$ and $V_2 = V_1 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2 + \frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.5}$$

5. For APF, $V_2 = V_1 = -V_3 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2 - s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3.6}$$

It is shown from the above equations that selecting the appropriate input voltages allows for the implementation of a four distinct second-order filter function. The filter parameters of the proposed circuit, namely, ω and Q (derived by using 1) of this filter are given by:

$$Q = \sqrt{\frac{g_m R_1 C_2}{C_1}} \tag{3.7}$$

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{3.8}$$

The proposed filter circuit, as indicated that the w_o can be adjusted by C ($C=C_1=C_2$) and maintained the ratio of g_m/R_1 constant while the Q can be adjusted by gmR1 and kept the ratio of C_1/C_2 constant. The novel circuit allows for independent control of ω and Q. Note that for varying the value of C_1 and C_2 simultaneously; it is possible by using capacitor arrays.

3.2 SIMULATION AND EXPERIMENTAL VALIDATION OF FIRST PROPOSED CIRCUIT CONFIGURATION:

To validate the functionality of the proposed universal filter, a comprehensive simulation study was conducted using PSPICE, leveraging the TSMC 0.18µm CMOS technology node. The core component of this filter is the Voltage Differencing Current Conveyor (VDCC), whose CMOS implementation is detailed in Fig. 1.12. This VDCC architecture integrates two primary stages:

1. Transconductance Amplifier Stage: Comprising transistors M1 to M8, this stage converts differential input voltages into output currents.

2. Current Conveyor Stage: Formed by transistors M9 to M22, this stage facilitates the transfer of current while maintaining voltage levels, ensuring accurate signal processing.

The transconductance parameter, g_m, of the VDCC is a critical factor influencing the filter's performance and is mathematically expressed as:

$$gm = \sqrt{I_{B1}\mu_1 C_{ox}\left(\frac{w}{l}\right)} \tag{3.9}$$

Where:

- I_{B1}: External bias current
- μ_n: Electron mobility
- C_{ox}: Gate oxide capacitance per unit area
- W and L: Effective channel width and length of the NMOS transistors.

In the simulation setup, the power supply voltages were set to V_{DD}=+0.9, and VSS=−0.9, with a bias current I_{B2}=100 μA. The transistor dimensions, as specified in Table 1.2, were meticulously chosen to optimize performance.

The universal filter was engineered to realize five fundamental filter responses: LPF, HPF, BPF, BSF and APF. The design targeted a center frequency of 1.44 MHz with a quality factor (Q) of 1. The selected component values were:

- C1=C2=40 pF
- I_{B1}=30 μA
- R_1=2.6 kΩ
- g_m=347 μƱ

Simulation results, depicted in Figures 3.2 through 3.6, illustrate the magnitude responses of the respective filters. The observed center frequency was approximately 1.41 MHz, slightly deviating from the theoretical value, likely due to inherent parasitic elements and non-idealities in the CMOS implementation.

Further analysis of the APF's phase response at 1.44 MHz, conducted using MATLAB and presented in Figure 3.7, confirmed the filter's capability to maintain consistent phase characteristics across the desired frequency range.

To assess the robustness of the filter against component variations, a Monte Carlo simulation with 100 iterations was performed, considering a ±10% tolerance in capacitor values. The

resulting frequency distributions, shown in Figures 3.8 to 3.10, demonstrate the filter's resilience and stability under manufacturing variances.

Transient response analyses, illustrated in Figure 3.11, evaluated the filter's time-domain performance for a 50 mV input signal at various frequencies: 100 kHz for LPF, 1.4 MHz for BPF, and 30 MHz for HPF. These results confirm the filter's efficacy in processing signals across a broad frequency spectrum.

Notably, the total power consumption of the circuit was measured at 4.9 mW, highlighting its suitability for low-power applications in modern electronic systems.

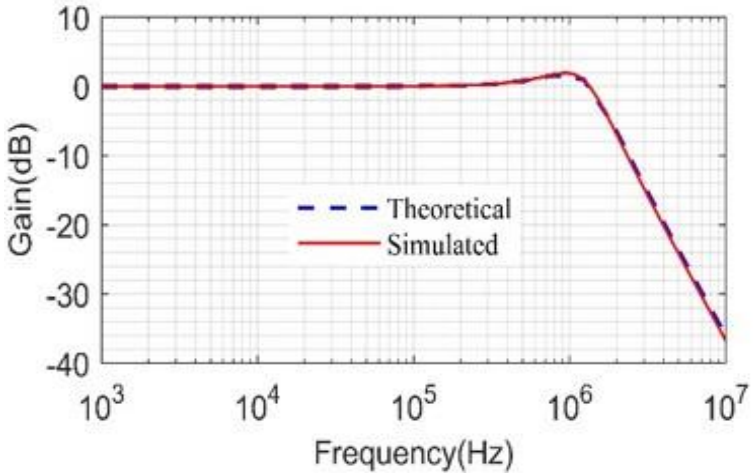

Figure 3.2: Theoretical and Simulation frequency response of LPF

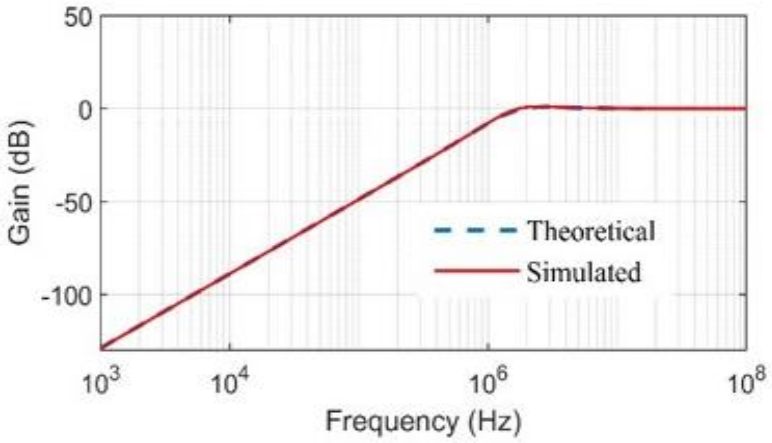

Figure 3.3: Theoretical and Simulation frequency response of HPF

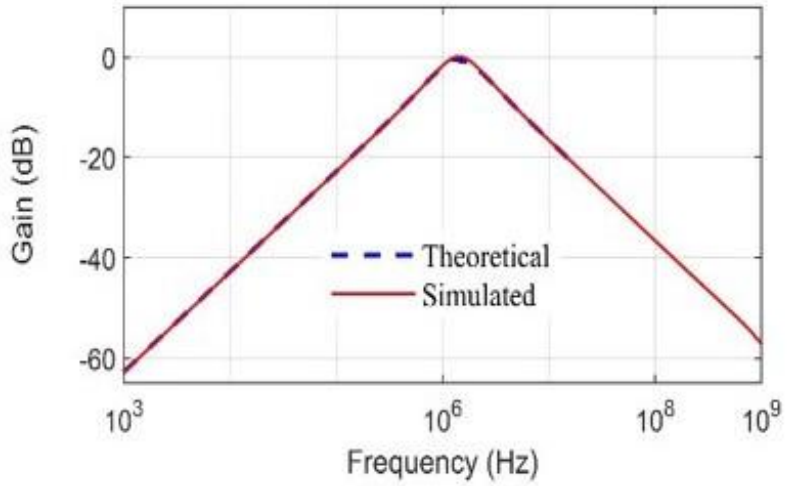

Figure 3.4: Theoretical and Simulation frequency response of BPF

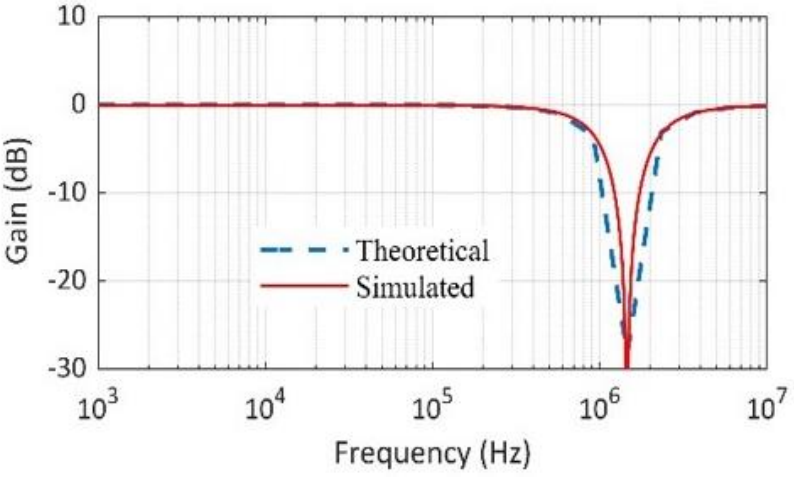

Figure 3.5: Theoretical and Simulation frequency response of BSF

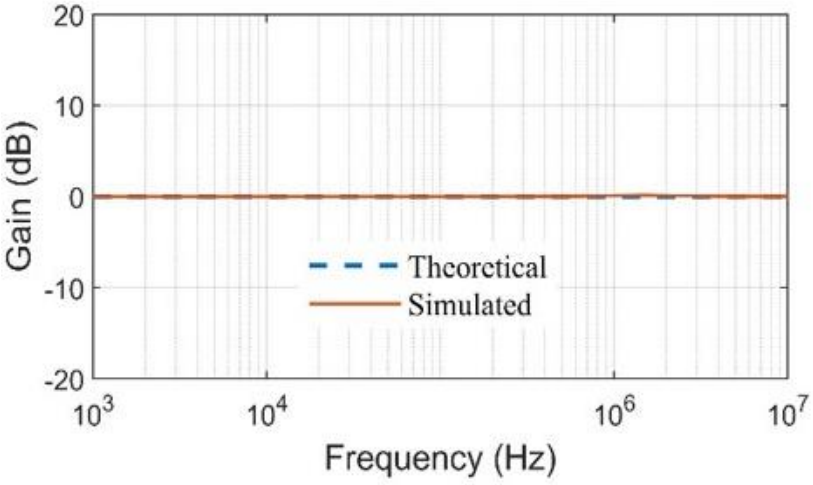

Figure 3.6**:** Theoretical and Simulation frequency response of APF

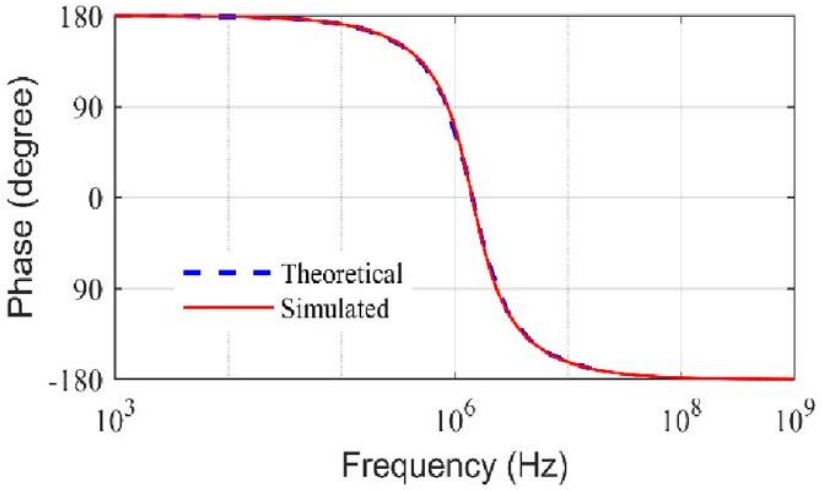

Figure 3.7: Theoretical and Simulation phase response of APF

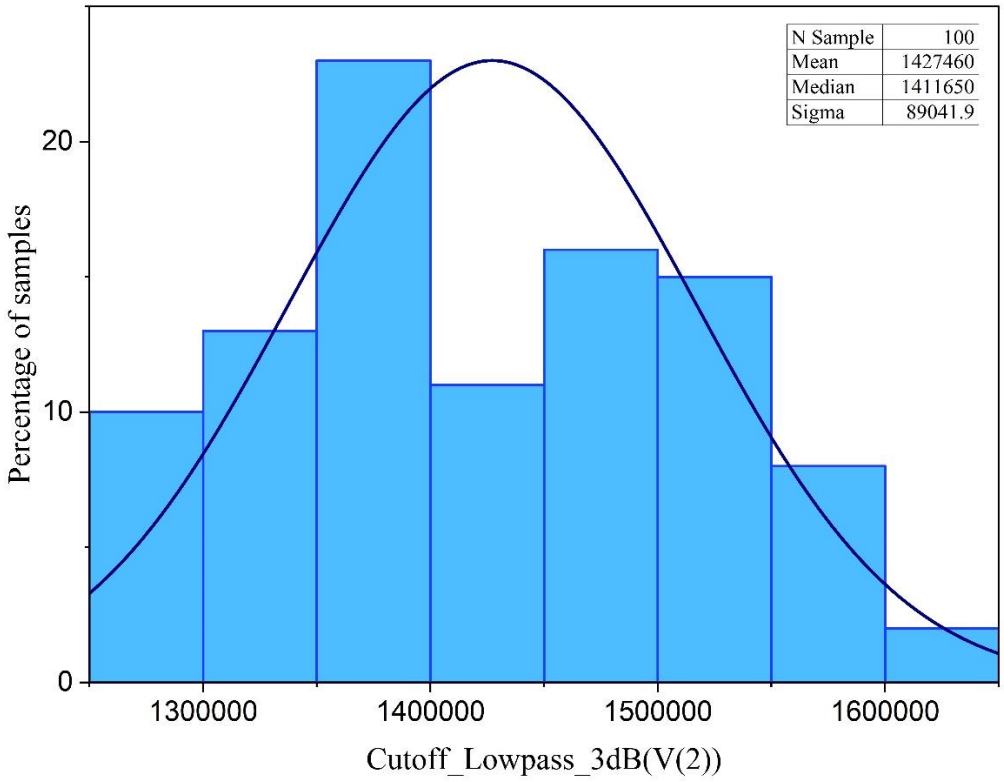

Figure 3.8: Monte Carlo analysis of LPF

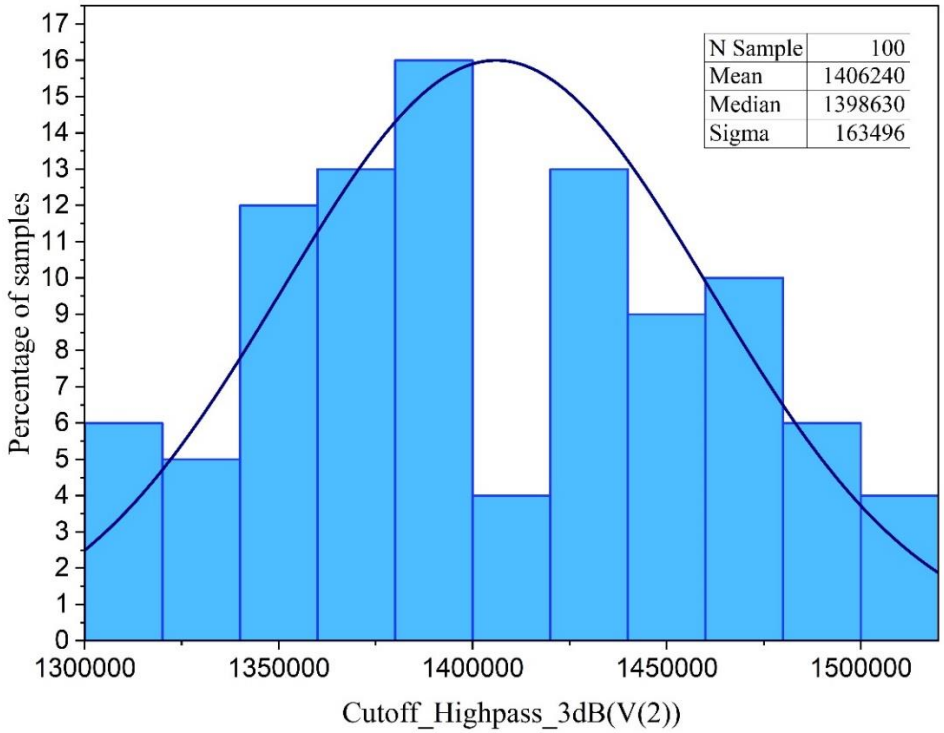

Figure 3.9**:** Monte Carlo analysis of HPF

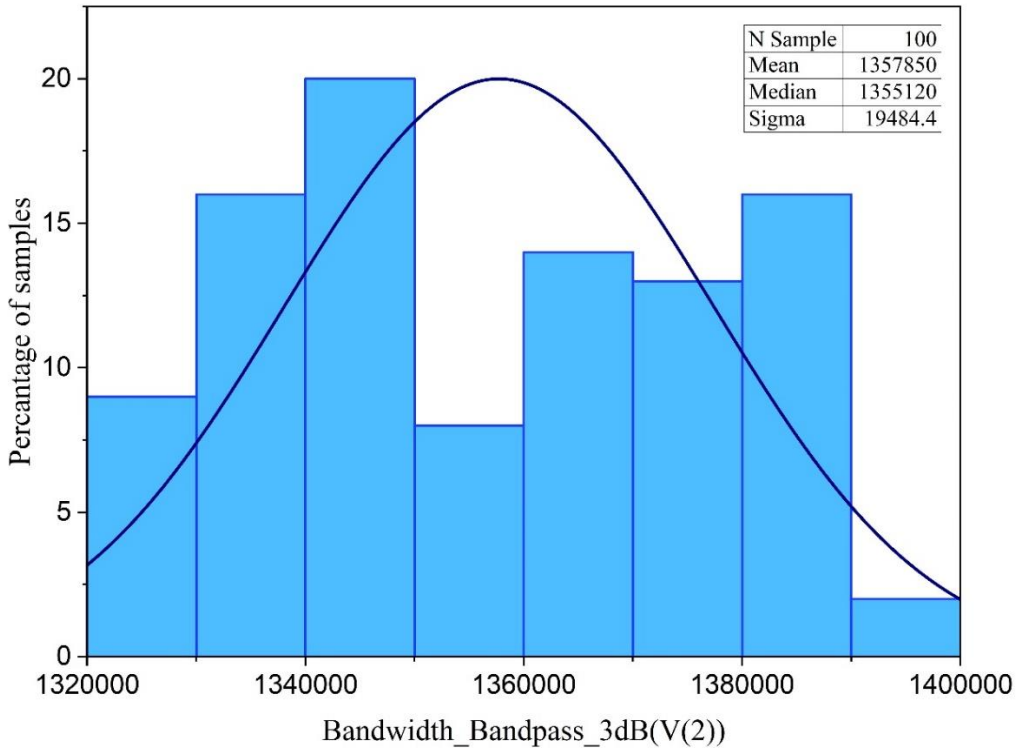

Figure 3.10: Monte Carlo analysis of BPF

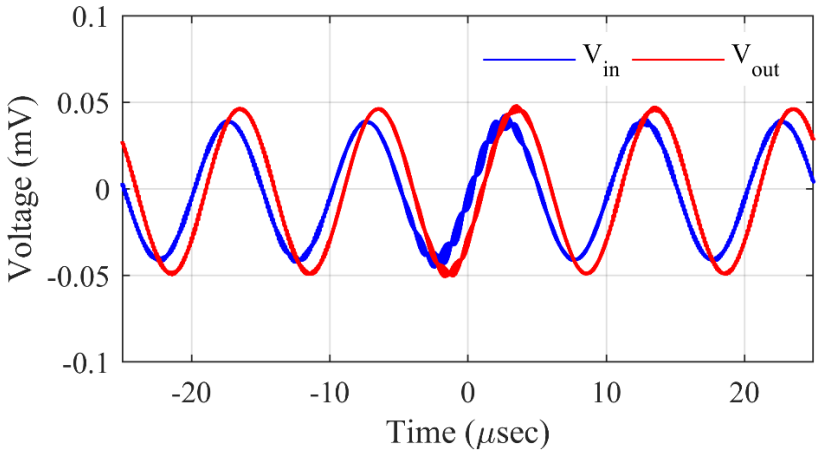

Figure 3.11: Transient analysis of LPF

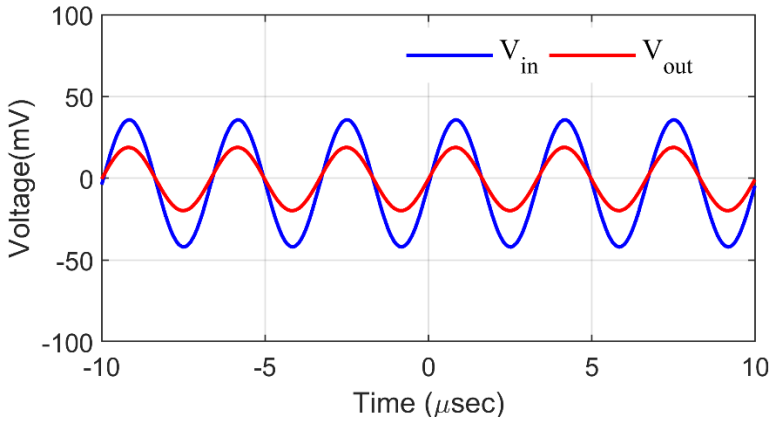

Figure 3.12: Transient analysis of HPF

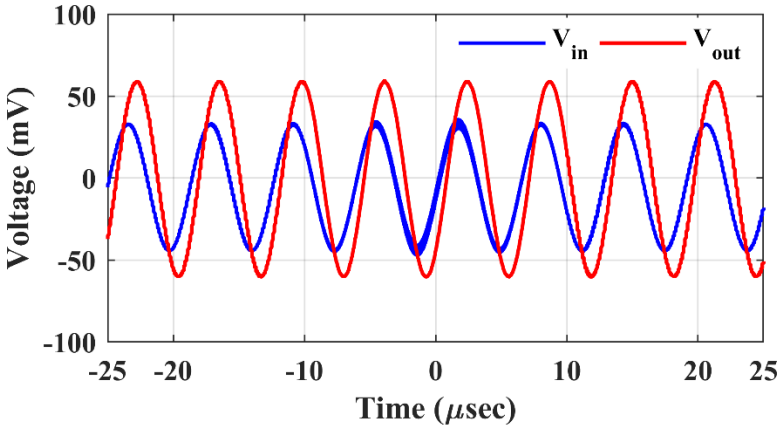

Figure 3.13: Transient analysis of BPF

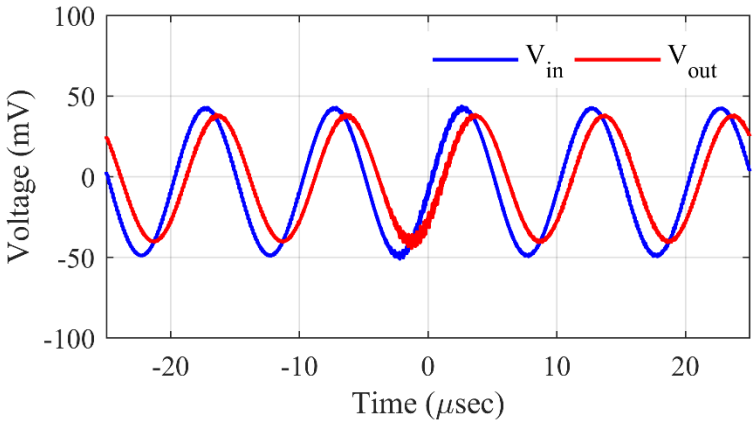

Figure 3.14: Transient analysis of BSF

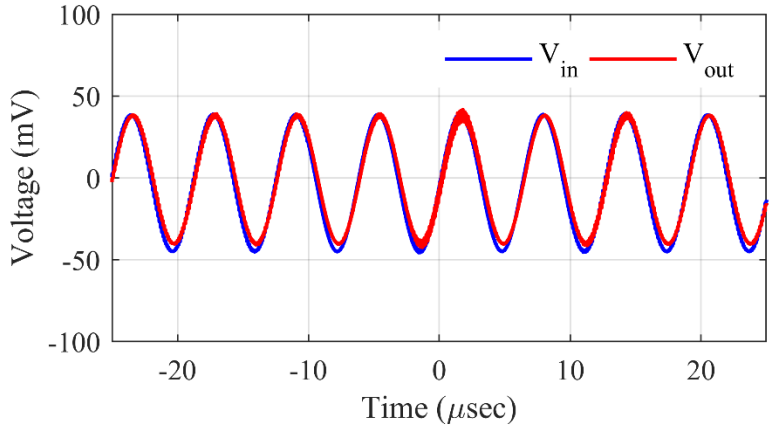

Figure 3.15: Transient analysis of APF

3.3 REALIZATION OF UNIVERSAL BI-QUAD FILTERS USING SECOND PROPOSD CIRCUIT CONFIGURATION:

VDCC based universal biquad filter is proposed in this section. Using a VDCC and four passive elements, the proposed design to achieve LPF, HPF, BPF, APF and BSF is demonstrated in Fig.3.16.

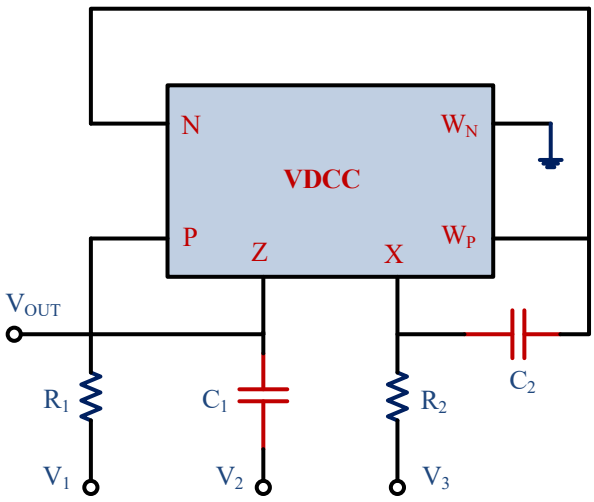

Figure 3.16: Circuit of Realised Universal Filters using VDCC.

A circuit analysis of Fig. 3.16 (assuming ideal VDCC) gives the following transfer function (TF);

$$V_o = \frac{s^2 V_{in2} + s\frac{1}{C_1 R_1} V_{in1} + \frac{g_m}{C_1 C_2 R_2} V_{in3}}{s^2 + s\frac{1}{C_1 R_1} + \frac{g_m}{C_1 C_2 R_2}} \tag{3.10}$$

Case I : For LPF, $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{\frac{g_m}{C_1 C_2 R_2}}{s^2 + s\frac{1}{C_1 R_1} + \frac{g_m}{C_1 C_2 R_2}} \tag{3.11}$$

Case II : For HPF, $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\frac{1}{C_1 R_1} + \frac{g_m}{C_1 C_2 R_2}} \tag{3.12}$$

Case III : For BPF, $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s\frac{1}{C_1R_1}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \tag{3.13}$$

Case IV : For APF, $V_{in2} = V_{in3} = V_{in}$ and $V_{in1} = -V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2 - s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \tag{3.14}$$

Case V : For BSF, $V_{in1} = 0$ and $V_{in2} = V_{in3} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2 + \frac{g_m}{C_1C_2R_2}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \tag{3.15}$$

The parameters such as ω_o and Q of the LPF, HPF, BPF, APF and BSF (derived by using (3.9)) of this filter are given by:

$$\omega_o = \sqrt{\frac{g_m}{C_1C_2R_2}} \tag{3.16}$$

$$Q = \sqrt{\frac{g_mR_1C_1}{C_2}} \tag{3.17}$$

The proposed circuit allows independent tunning of ω and Q. The filter response with desired value of ω_o was obtained by making $C_1=C_2 =C$ in (3.16) Note that it is possible to vary the values of C1 and C2 simultaneously by utilizing capacitor arrays.

3.4 SIMULATION AND EXPERIMENTAL VALIDATION OF SECOND PROPOSED CIRCUIT CONFIGURATION:

To comprehensively validate the functionality of the proposed Voltage-Differential Current Conveyor (VDCC) circuit, a series of simulations were conducted using PSPICE, employing the TSMC 0.18 μm CMOS technology node. The VDCC architecture integrates two primary components: a transconductance amplifier and a current conveyor. The transconductance amplifier is constructed using transistors M1 through M8, while the current conveyor comprises transistors M9 to M22. External bias currents, denoted as I_{B1} and I_{B2}, are applied to facilitate the operation of these components.

The transconductance parameter (gm) of the VDCC is determined by the following equation:

$$gm = \sqrt{I_{B1}\mu_1 C_{ox}\left(\frac{w}{l}\right)} \tag{3.18}$$

In this expression, μ_1 represents the electron mobility, C_{OX} is the oxide capacitance per unit area at the gate, and W and L denote the channel width and length of the CMOS transistors, respectively.

For the simulations, the power supply voltages were set to V_{DD} = +0.9 V and V_{SS} = -0.9 V. The bias currents were configured as I_{B1} = 50 μA and I_{B2} = 100 μA. The transistor dimensions utilized in the design are detailed in Table 3.2 of the original documentation.

The VDCC was employed to design a suite of universal filters, including LPF, HPF, BPF, BSF and APF. These filters were targeted to achieve a center angular frequency (ω_0) of 1.26 MHz and a quality factor (Q) of 0.7. The component values selected for the filter designs were as follows:

- Capacitors: C1 = C2 = 50 pF
- Resistors: R1 = R2 = 1.768 kΩ
- Transconductance: g_m = 277 μ℧

Upon simulation, the filters exhibited a cutoff frequency of approximately 1.21 MHz, which is slightly lower than the theoretical value of 1.26 MHz. This minor deviation is attributed to practical non-idealities inherent in the circuit components and layout.

The magnitude responses of the filters, as obtained from the PSPICE simulations, are illustrated in Figures 3.17 through 3.21. These results confirm the effective operation of the VDCC-based configurations as universal filters. Additionally, the phase response of the APF at 1.21 MHz was evaluated using MATLAB, with the findings presented in Figure 3.22.

To assess the impact of component tolerances on filter performance, a Monte Carlo simulation was performed. This analysis involved 100 samples, considering a 10% tolerance variation in the capacitor values. The outcomes of this simulation are depicted in Figures 3.23 to 3.27, demonstrating the robustness of the filter designs against component variations.

Further analysis was conducted to explore the independent adjustment of the cutoff frequency (ω_0) while maintaining a fixed quality factor (Q). This was achieved by varying the resistance R_2 to values of 1.5 kΩ, 1.75 kΩ, and 2 kΩ. The corresponding effects on the filter responses are shown in Figures 3.28 to 3.32, highlighting the tunability of the filter characteristics through resistor value adjustments.

In summary, the comprehensive simulation studies validate the efficacy of the proposed VDCC circuit in implementing versatile and tunable analog filters, demonstrating its potential for integration into various signal processing applications.

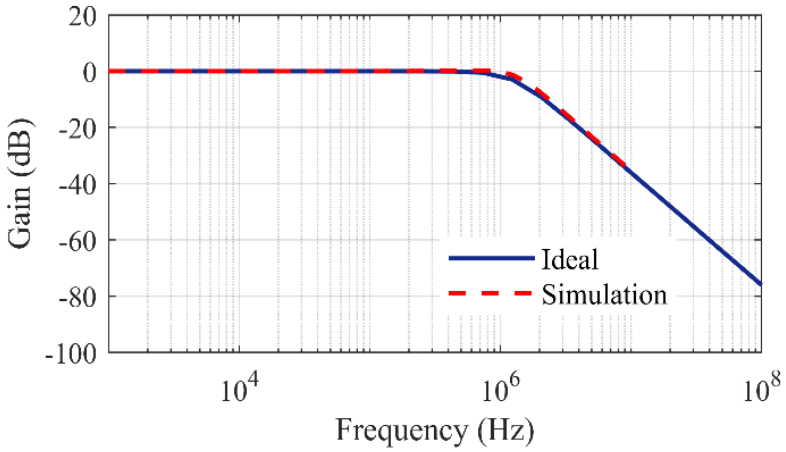

Figure 3.17**:** Ideal and simulated respose of LPF

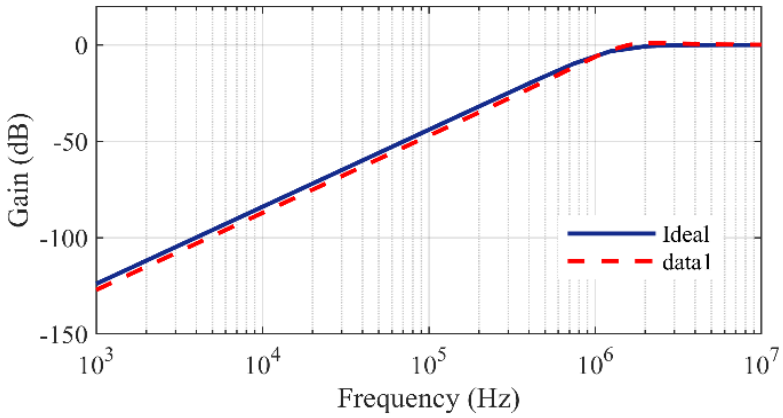

Figure 3.18: Ideal and simulated response of HPF

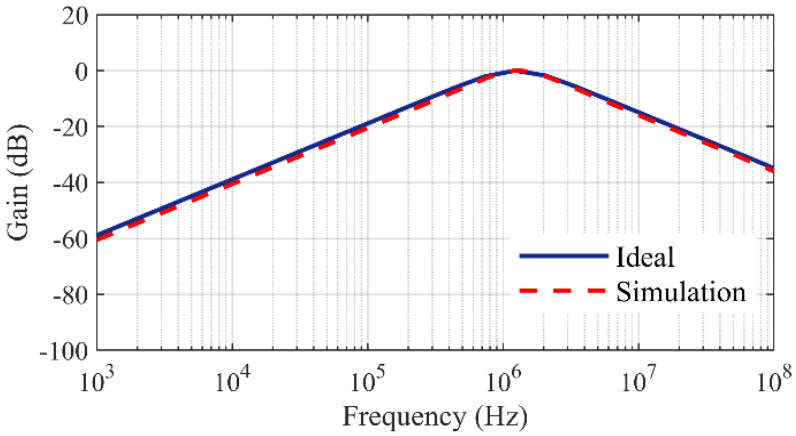

Figure 3.19: Ideal and simultaed response of BPF

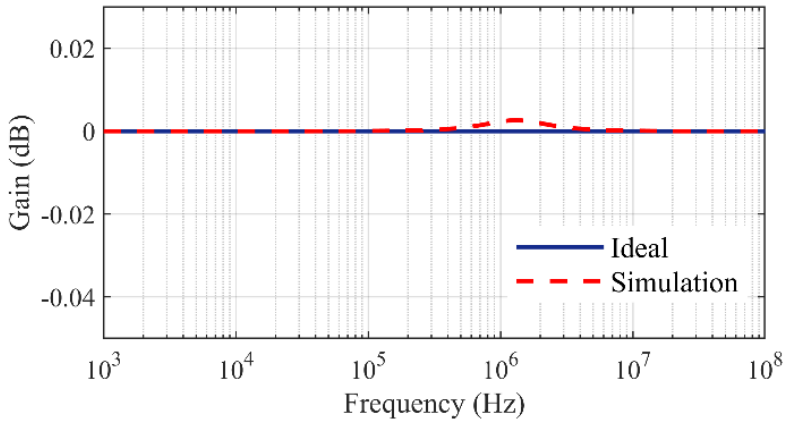

Figure 3.20: Ideal and simulated response of APF

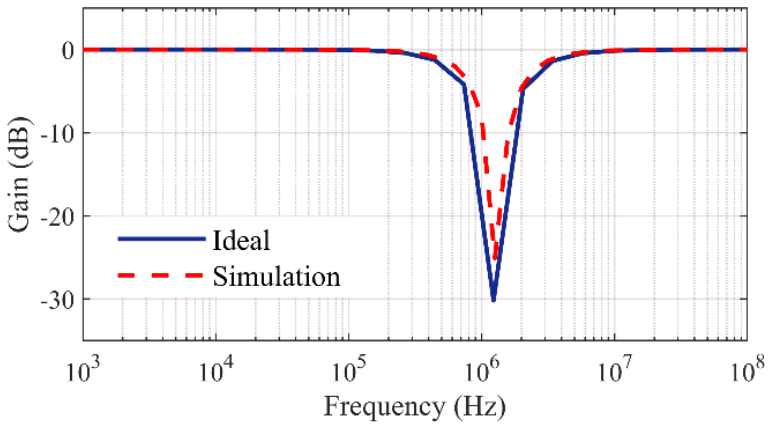

Figure 3.21: Ideal and simulated response of BSF

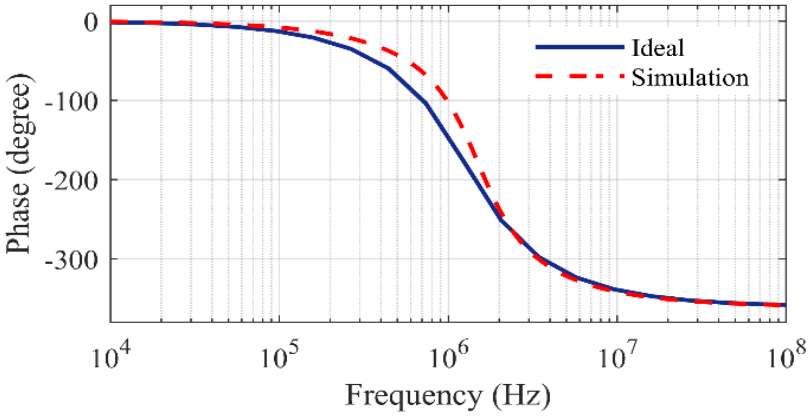

Figure 3.22: Ideal and simulated phase response of APF

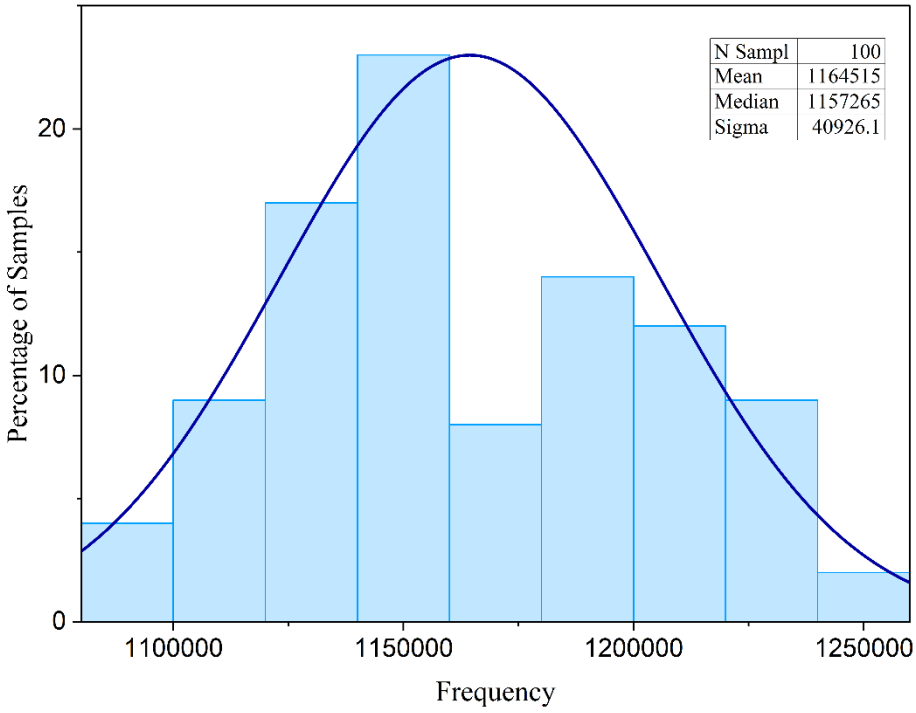

Figure 3.23: Monte Carlo analysis for LPF

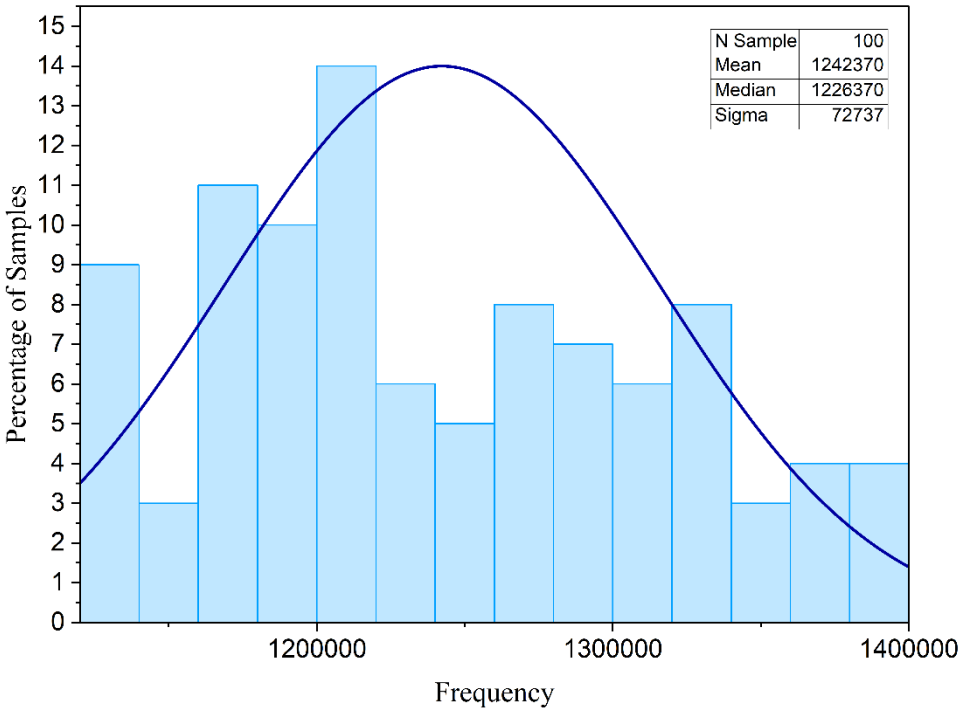

Figure 3.24: Monte Carlo analysis for HPF

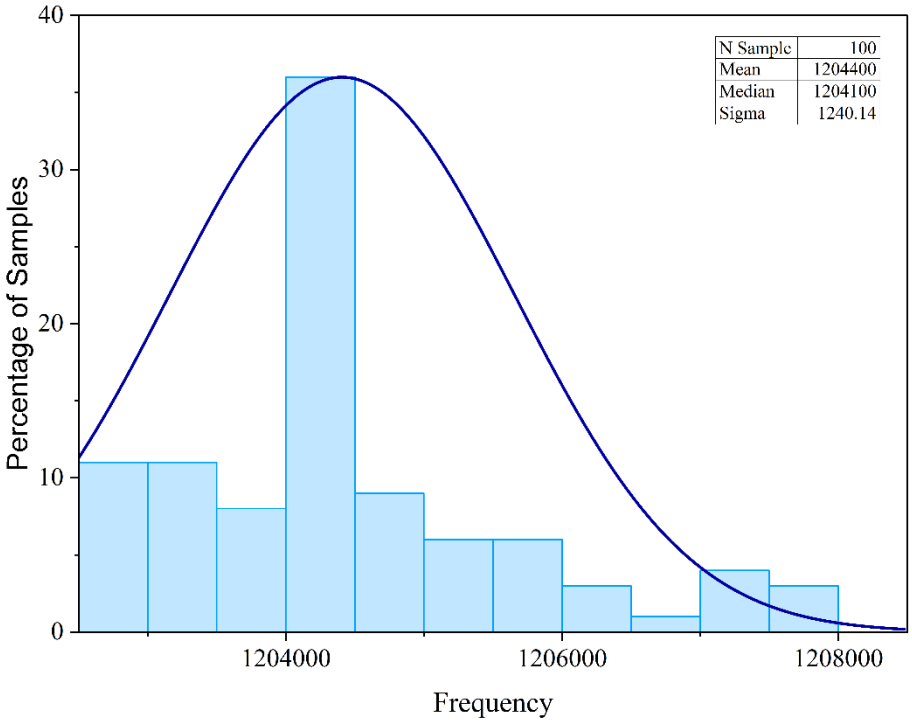

Figure 3.25: Monte Carlo analysis for BPF

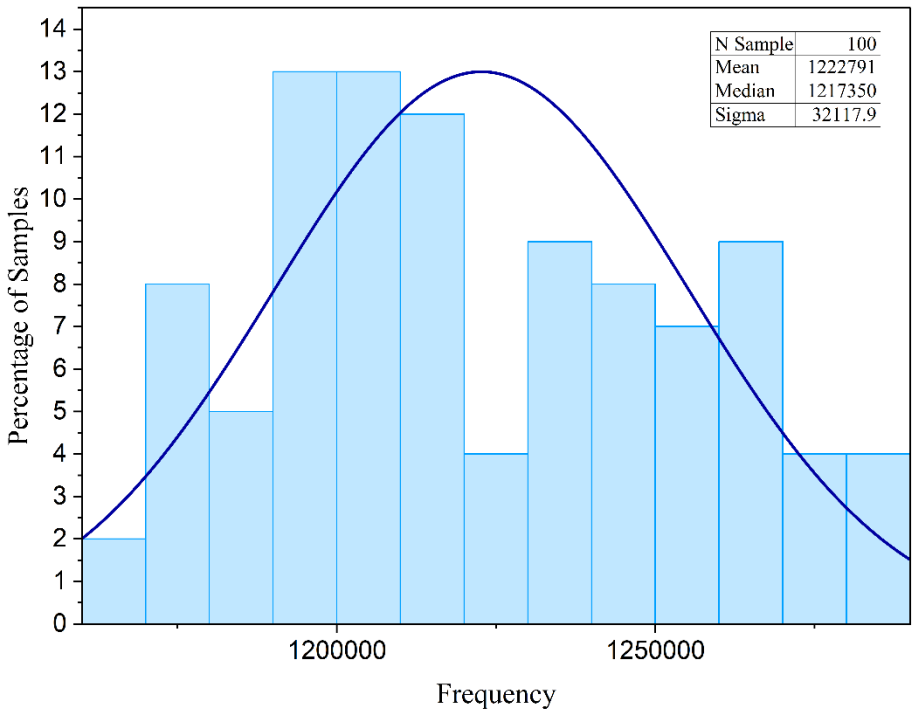

Figure 3.26: Monte Carlo analysis for APF

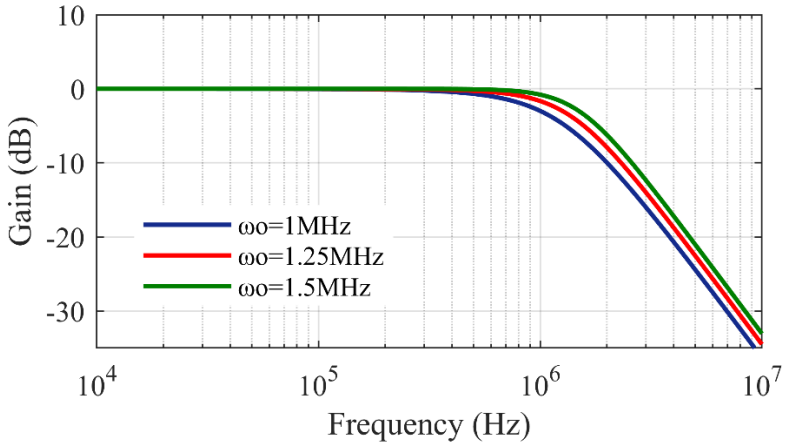

Figure 3.27: Variation of ω_o for LPF (fixed Q)

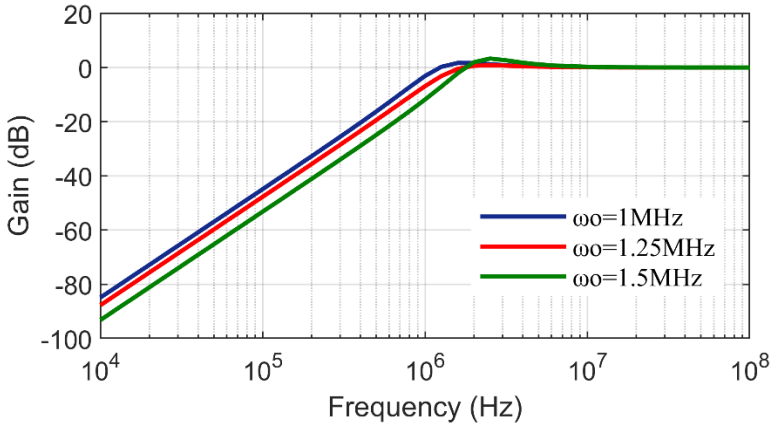

Figure 3.28: Variation of ω_o for HPF (fixed Q)

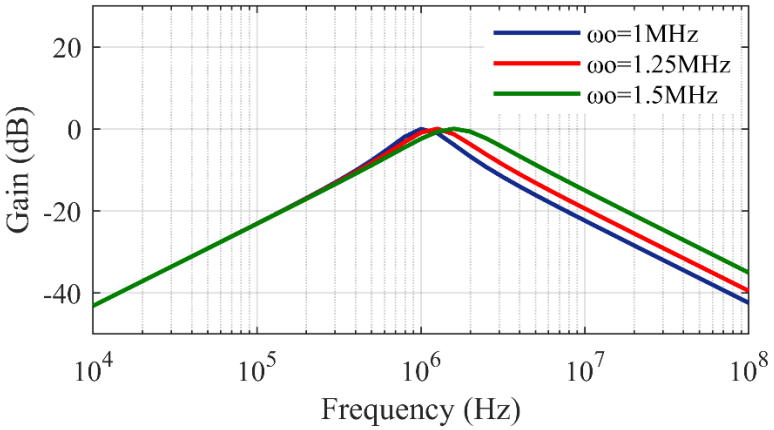

Figure 3.29: Variation of ω_o for BPF (fixed Q)

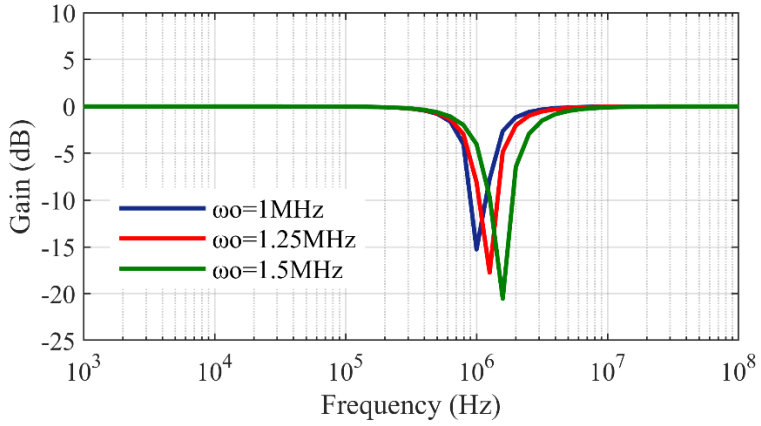

Figure 3.30: Variation of ω_o for BSF (fixed Q)

CHAPTER 4

4. CONCLUSION & FUTURE SCOPE

4.1 CONCLUSION OF THE PRESENTED WORK:

In this thesis, we embarked on a comprehensive exploration of the design, analysis, simulation, and potential applications of filters utilizing Voltage Differencing Current Conveyor (VDCCs). Through our research endeavours, we have meticulously examined the versatility, effectiveness, and promising capabilities of VDCC-based filters across various signal processing domains. By harnessing the unique attributes of VDCCs, including their high gain-bandwidth product, low voltage and power requirements, and flexible signal processing abilities, we have presented novel filter architectures that surpass conventional designs in terms of performance and functionality.

Our proposed filter design has showcased superior performance metrics compared to traditional counterparts. These advancements include enhanced frequency response, improved passband/stopband characteristics, expanded dynamic range, and enhanced linearity. Such improvements are paramount in meeting the evolving demands of modern signal processing applications, where precision, efficiency, and adaptability are crucial. A key highlight of our research lies in the inherent flexibility and adaptability afforded by VDCCs. These characteristics have enabled the realization of filters with multiple modes and functions, thereby facilitating versatile operation and seamless integration into diverse systems. The ability to configure filters to suit specific application requirements underscores the transformative potential of VDCC based designs in addressing a wide array of signal processing challenges. Furthermore, our discussions encompassed optimization techniques, future research directions, and potential applications of VDCC-based filters. By shedding light on these aspects, we 60 have underscored the pivotal role of VDCCs in advancing analog filter design and signal processing technology. The identified future scope encompasses a rich landscape of opportunities, including the exploration of advanced circuit topologies, multi-mode operation, integration into ICs, expansion into wideband/high-frequency

applications, development of adaptive/reconfigurable filters, exploration of integrated sensing capabilities, and investigation of nonlinear signal processing paradigms.

By contributing to the expanding body of knowledge in filter design using VDCCs, this thesis underscores the transformative potential of these devices in diverse fields such as communications, instrumentation, biomedical devices, and beyond. Through continued exploration and innovation in these areas, VDCC-based filters hold the promise of revolutionizing analog signal processing and spearheading the development of groundbreaking solutions in the future. In conclusion, this thesis has explored the design, analysis, simulation, and potential applications of filters using Voltage Differencing Current Conveyor(VDCCs). Throughout this research, we have demonstrated the versatility, effectiveness, and promise of VDCC based filters in various signal processing applications.

The proposed filter design have shown improved performance metrics, including enhanced frequency response, better passband/stopband characteristics, increased dynamic range, and improved linearity compared to conventional filter designs. The flexibility and adaptability of VDCCs have enabled the realization of filters with multiple modes and functions, allowing for versatile operation and seamless integration into different systems. Furthermore, we have discussed optimization techniques, future research directions, and potential applications of VDCC-based filters, highlighting their significance in advancing analog filter design and signal processing technology. The future scope includes exploring advanced circuit topologies, multi-mode operation, IC integration, wideband/high-frequency applications, adaptive/reconfigurable filters, integrated sensing, nonlinear signal processing, and experimental validation in real-world scenarios.

Overall, this thesis contributes to the growing body of knowledge in filter design using VDCCs and underscores their potential for various applications in communications, instrumentation, biomedical devices, and beyond. By continuing to explore these avenues of research and development, VDCC-based filters have the potential to revolutionize analog signal processing and pave the way for innovative solutions in the future.

4.1.1 CONCLUSIVE REAMRKS:

This filter offers several advantages:

a. It uses only one VDCC and three passive components, making it straightforward for integration.

b. It can produce the four standard filter responses without the need for component matching.

c. It allows independent control of the parameters ω_o (natural frequency) and Q (quality factor).

d. Its suitability for low-power applications in modern electronic systems.

4.2 FUTURE SCOPE OF THE PRESENTED WORK:

The future scope outlines potential areas for significant improvement in the capabilities and applicability of these universal bi-quad inverse filters using VDCC technology. By continuing research in these areas, researchers can pave the way for wider adoption of these filters in various signal processing applications.

Enhancing Performance:

- Higher-Order Filters: Future research should explore extending the design to higher-order filters for tackling more complex filtering tasks. These filters would have a more intricate structure than the current bi-quad design.

- Improved Accuracy: Minimizing errors caused by imperfections in VDCC circuits is crucial. Researchers should investigate techniques to achieve greater accuracy in the filter responses.

- Wider Bandwidth: Expanding the operational bandwidth of the filters would allow them to handle a broader range of signal frequencies. This would require further research into design methods.

Advanced Applications:

- Switched-Capacitor Implementations: Investigating the feasibility of implementing these filters using switched-capacitor circuits is necessary. This could potentially allow for integration into CMOS technology, making the filters more widely applicable.

- Programmable Filters: Developing programmable versions of these filters would enable them to dynamically adjust their characteristics based on real time requirements. This would require significant design advancements.

- Nonlinear Filtering Applications: Exploring the potential application of these filters in nonlinear filtering tasks, such as harmonic distortion removal or edge detection in image processing, could open new avenues for their use.

Integration and Miniaturization:

- On-Chip Integration: Researchers should investigate the possibility of incorporating these filters directly onto integrated circuits. This would lead to more compact and efficient signal processing systems.

- Reduced Power Consumption: Minimizing the power consumption of these filters is essential for battery-powered applications. Research on low-power design techniques is needed.

- Microfluidic Integration: Exploring the potential for integrating these filters with microfluidic devices for lab-on-a-chip applications or bio signal processing holds promise for future advancements.

Research into alternative VDCC implementations using different materials or device structures could potentially achieve better performance or wider operating ranges. Exploring the suitability of emerging nano electronic devices for realizing these filters could lead to significant size reduction and improved performance. This would require investigation into the compatibility of these new materials with the filter design.

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LIST OF PUBLICATIONS

Publisher	Name of Paper	Scopus Indexed
Springer RITEEC 2025 (NIT Patna)	VDCC-Based Voltage Mode Universal Filter	YES
Springer PICS 2025 (NIT Hamirpur)	Single CMOS VDCC-based voltage mode universal filter	YES

NIT-PATNA

RITEEC 2025 Electrical Engineering

NITP/EED/RITEEC/2025/C073

Springer

CERTIFICATE OF PAPER PRESENTATION

This is to certify that

AYUSH BHARDWAJ

has presented a paper at the 1st International conference on Recent Innovations and Trends in Electrical & Electronics Engineering and Computing (RITEEC 2025), 22-23rd May 2025, NIT Patna.

Paper title: VDCC-Based Voltage Mode Universal Filter

Authors: Ayush Bhardwaj, Ram Bhagat, Anup Mandpura

Paper Id: 147

DR. RUCHI AGARWAL	DR. G LLOYDS RAJA	DR. AMBARISHA MISHRA
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RENGIE DELIVERING SOLUTION

VDCC-Based Voltage Mode Universal Filter

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Abstract. This paper presents a voltage mode (VM), triple input and single output (TISO) biquad filter using single voltage differencing current conveyor (VDCC) and three passive components. The proposed configuration is capable of realizing second-order high pass filter (HPF), low pass filter (LPF), band pass filter (BPF), band stop filter (BSF) and all pass filter (APF). The proposed biquad configuration has tunability of center frequency (ω), pole quality factor (Q). The proposed filters are implemented in PSPICE and the filter responses are simulated. The simulation results are then verified with theoretical analysis.

Keywords: Biquad, VM, VDCC, Filter, Analog signal processing, TISO, Single input double output.

1. Introduction

Analog filters are essential in many fields, such as electronics, mechatronics, and analog signal processing, as they enhance system functionality by removing noise, interference, and signal distortion. This paper presents an innovative analog filter design utilizing the VDCC. The proposed voltage mode universal filter configuration is designed with a focus on minimizing both equipment size and power consumption, making it an ideal choice for integration into compact systems. Its voltage-mode configuration ensures effective handling of a broad spectrum of AC signals without compromising signal integrity.

First, Over the years, numerous filters utilizing the VDCC as an active building block have been developed and documented in the literature, such as [1]-[13]. These filters are categorized into two primary configurations: voltage mode (where both input and output depend solely on voltage) [1-7], and current mode (where both input and output are determined by current) [7-9]. Furthermore, they can be classified based on their structure as single VDCC-based or multiple VDCC-based filters configuration.

Providing a comprehensive review of VDCC-based voltage-mode (VM) biquad filters introduced by various researchers is essential to establish context and relevance for new developments. This paper focuses on a single VDCC-based VM filter configuration, specifically of the TISO type. A brief overview of previously reported VM filter configurations is presented below to set the stage for this work.

A generalized scheme for the realization of biquad filter has been discussed in [1]. Three different single VDCC circuits has been implemented, one of the TISO type filtering category circuit has been provided, which can allow all types of filtering functions, another circuit were implemented SIDO type filtering category, including four passive components has been provided only HP and BP filtering functions, the last one is SIDO type filtering category, including four passive components (two resistor and two capacitor) has been provided only LPF and BPF filtering functions. ω and Q can be tunable in second and last filtering category. In [2], a MISO type filter configuration employing single VDCC, one resistor and two ungrounded capacitors has been presented with electronic control of ω and Q. A Two Thomas VM filter configuration with two VDCCs, two capacitors and five resistors were provided BP filter configuration in [3]. A voltage mode first-order APF with a SISO type has been implemented using single VDCC, two resistor (both floating) and capacitor (grounded) in [4], while [5] presented SISO type VM second order universal filter with single VDCC based on

BJT structure with four passive components (two capacitors and two resistors) to obtain all five filters function. In [6] a SISO type filter configuration employing single VDCC using two resistors and two capacitors has been provided only BR filtering function and with separate control of ω and Q. Comprehensive study of previously reported VM filter using VDCC have been discussed in table 1.

This paper presents the utilization of the VDCC, a sophisticated active component with electronic tuning capabilities, in the development of a voltage-mode universal biquadratic filters. The VDCC, which integrates a transconductance amplifier and a second-generation current conveyor (CCII), serves as the foundational element of the proposed design. The circuit configuration employs a single VDCC along with three passive components two capacitors and one resistor to achieve versatile functionality The circuit is capable of achieving BPF, HPF, LPF, BSF and AP filter responses within a single configuration. It features a high-impedance output and supports independent tuning of the Q and ω_o. The proposed filter's performance is verified through PSPICE simulations.

Table 1: A comparative analysis of various multifunction voltage-mode (VM) biquad filters using VDCC as active element.

Ref	Mode	Filtering Category	No. of VDCC	Technology	No. of R+C	All grounded passive element only	Filtering Function
[1]	VM	TISO	1	0.18µm CMOS & ICs	1+2	No	LP, HP, BP, BS, AP
[1]	VM	SIDO	1	0.18µm CMOS	2+2	No	HP, BP
[1]	VM	SIDO	1	0.18µm CMOS	2+2	No	LP, BP
[2]	VM	MISO	1	0.18µm CMOS & ICs	1+2	No	LP, HP, BP, BS, AP
[3]	VM	SISO	2	0.18µm CMOS	5+2	Yes	BP
[4]	VM	SISO	1	0.18µm CMOS & ICs	2+1	No	AP
[5]	VM	SIMO	1	HFA3127, HFA3128 BJT	2+2	No	HP, BP, LP, BS, AP
[6]	VM	SISO	1	0.18µm CMOS & ICs	2+2	No	BS
Proposed Circuit	VM	TISO	1	0.18µm CMOS	1+2	No	LP, HP, BP, AP, BS

2. Proposed Voltage Mode filter configuration employing VDCC

2.1 Introduction to VDCC

As illustrated in Fig. 1, the VDCC is a six-terminal device. Among these, P and N serve as the input terminals, while Z, X, W_N and W_P function as output terminals. Except for the X terminal, all other terminals exhibit high impedance. The behaviour of the VDCC is described by the characteristic equation provided in (1).

$$\begin{bmatrix} I_p \\ I_n \\ I_z \\ V_z \\ I_{wp} \\ I_{wn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ I_X \end{bmatrix} \quad (1)$$

I_P, I_N, I_Z, I_X, I_{WN} and I_{WP} represents the current at P, N, Z, X, W_P, W_N respectively and V_N, V_P, V_Z, V_X are the voltage at N, P, Z, X respectively. Transconductance gain, represented by g_m, is achieved by modulating the bias current of the VDCC.

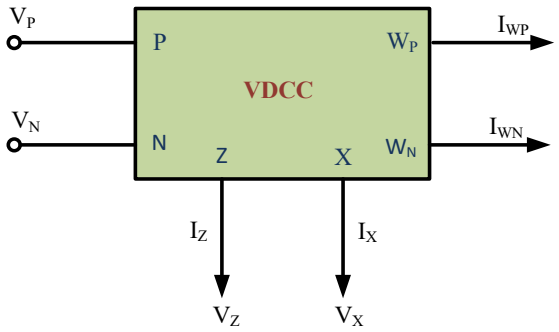

Fig. 1. Basic symbol of VDCC

2.2 Proposed Filter Configuration

The proposed filter with one VDCC, two capacitors and one resistor is demonstrated in Fig. 2. The proposed filter's transfer function V_o is given by:

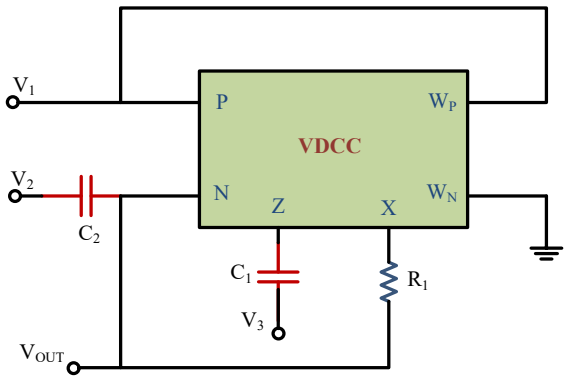

Fig. 2. Proposed Filter

The proposed filter's transfer function V_o is given by:

$$V_o = \frac{s^2 V_{in2} + s\frac{1}{R_1 C_2} V_{in3} + \frac{g_m}{C_1 C_2 R_1} V_{in1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \quad (2)$$

a) For LPF, $V_3 = V_2 = 0$ and $V_1 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{\frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{3}$$

b) For HPF, $V_3 = V_1 = 0$ and $V_2 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{4}$$

c) For BPF, $V_2 = V_1 = 0$ and $V_3 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s\frac{1}{R_1 C_2}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{5}$$

d) For BSF, $V_3 = 0$ and $V_2 = V_1 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2 + \frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{6}$$

e) For APF, $V_2 = V_1 = -V_3 = V_{in}$;

$$\frac{V_o}{V_{in}} = \frac{s^2 - s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}}{s^2 + s\frac{1}{R_1 C_2} + \frac{g_m}{C_1 C_2 R_1}} \tag{7}$$

From the above equations (2-7), it can be observed that by selecting the appropriate input voltages five distinct second-order filter function can be implemented. The system parameters of the proposed circuit, namely, ω and Q (derived by using 1) of this filter are given by:

$$Q = \sqrt{\frac{g_m R_1 C_2}{C_1}} \tag{8}$$

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{9}$$

The novel circuit allows independent control of ω and Q. The filter response with desired value of ω_o was obtained by making C_1=C_2=C in (9) and choosing appropriate value R_1 and C and maintained the ratio of g_m /R_1 constant. Note that it is possible to vary the values of C1 and C2 simultaneously by utilizing capacitor arrays [11]. While the Q can be adjusted by g_m/R_1 and kept the value of C_1, C_2 constant.

3. Simulation Results

To validate the operation of the proposed circuit in Fig. 2 PSPICE simulation utilizing TSMC 0.18um CMOS technology was performed. The design of a VDCC circuit utilizing CMOS technology in PSpice is illustrated in fig.-3. In the fig., a transconductance amplifier comprised of transistors M_1 to M_8 is also depicted. The current conveyor is composed of transistors M_9 to M_{22} in the fig.3. The direct current external bias is represented by I_{B1} and I_{B2}. Using [8], the transconductance parameter g_m of the VDCC is given by,

$$g_m = \sqrt{I_{B1}\mu_1 C_{ox}\left(\frac{w}{l}\right)} \tag{10}$$

where μ_1 indicates the electron mobility, the oxide capacitance per unit area at the gate is represented by C_{OX}, and *w* and *l* denote channel width and length of the CMOS transistor, respectively. The dimensions of the transistors are listed in Table 2. The power supply voltages were configured as V_{DD} = -V_{SS}= 0.9 V, and the bias current of I_{B2} was 100 μA.

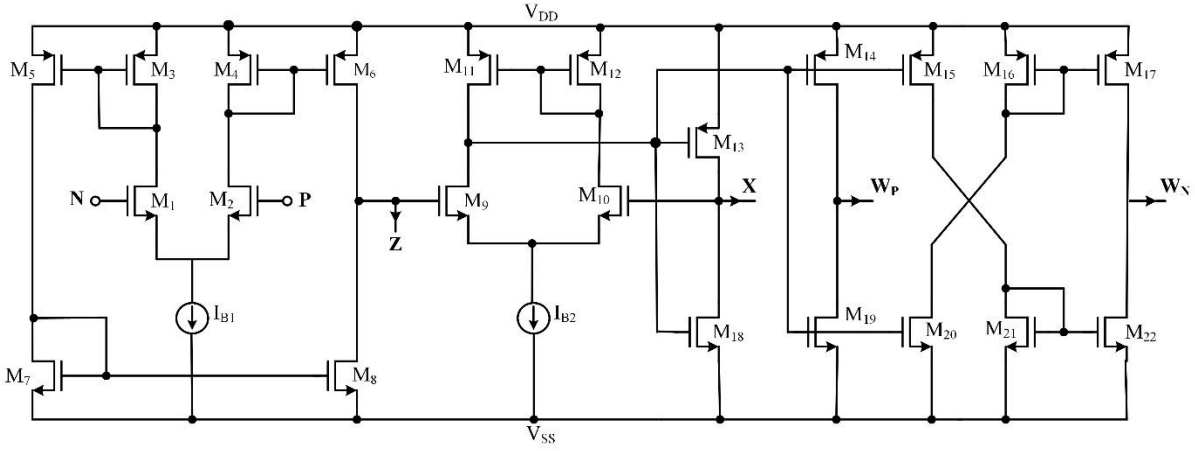

Fig. 3. CMOS implementation of the VDCC [8]

Table:2 Aspect ratios of the CMOS devices [8]

CMOS Transistors	w(μm)	l(μm)
M_1-M_4	3.6	1.8
M_5, M_6	7.2	1.8
M_7, M_8	2.4	1.8
M_9, M_{10}	3.06	0.72
M_{11}, M_{12}	14.4	0.72
M_{13}-M_{17}	0.72	0.72
M_{18}-M_{22}	0.72	0.72

The proposed LPF, HPF, BPF, BRF, and APF filters were designed with a center frequency of 1.44 MHz and a quality factor (Q) of 1. The chosen component values were C1 = C2 =40pF, I_{BI}=30 μA, R_1=2.6 kΩ, and g_m=347 μS. The simulated magnitude responses of the filters, obtained using PSPICE, are illustrated in Figs. 4 to 8. From the analysis of these results, the center frequency was determined to be 1.41 MHz, which is marginally lower than the theoretical value of 1.44 MHz. Fig. 9 presents the simulated phase response of the APF filter at 1.44 MHz, evaluated using MATLAB. The results depicted in Figs. 4 to 9 demonstrate that the proposed circuit effectively operates as a universal filter. Additionally, to evaluate the impact of capacitor tolerance on the center frequency, a Monte Carlo simulation was conducted with 100 samples, considering a 10% tolerance for the capacitors, as shown in Fig. 10. Furthermore, Fig. 11 illustrates the transient responses of the LPF, BPF and HPF filter functions for an input signal of 50 mV at various frequencies: 100 kHz for LPF, 1.4 MHz for BPF and 30 MHz for HPF.Also the total power dissipation of the circuit is 4.9mW which is very low.

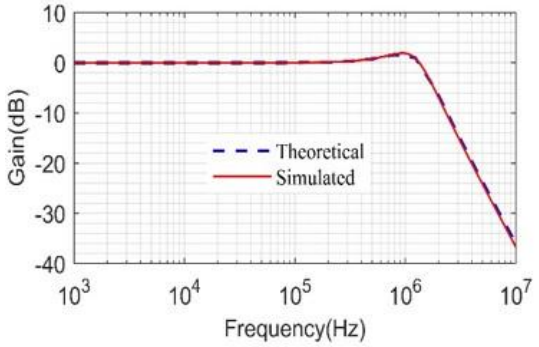

Fig. 4. Theoretical and simulated frequency response of LP Filter

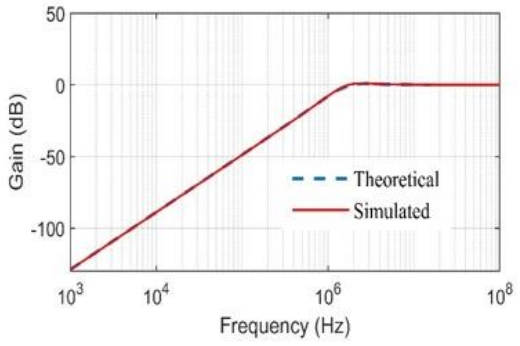

Fig. 5. Theoretical and simulated frequency response of HP Filter

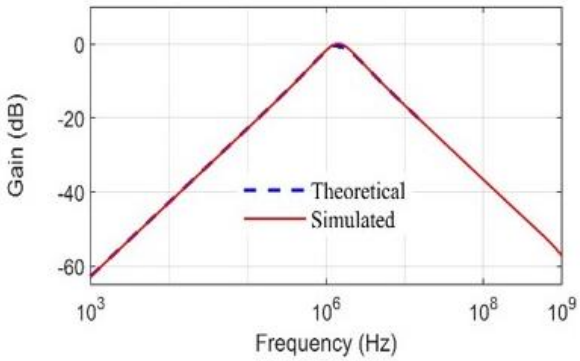

Fig. 6. Theoretical and simulated frequency response of BP Filter

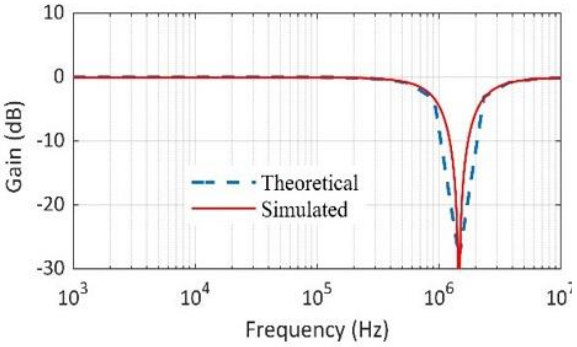

Fig. 7. Theoretical and simulated frequency response of BS Filter

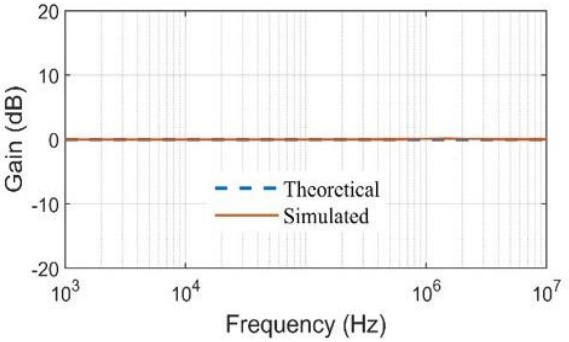

Fig. 8. Theoretical and simulated frequency response of AP Filter

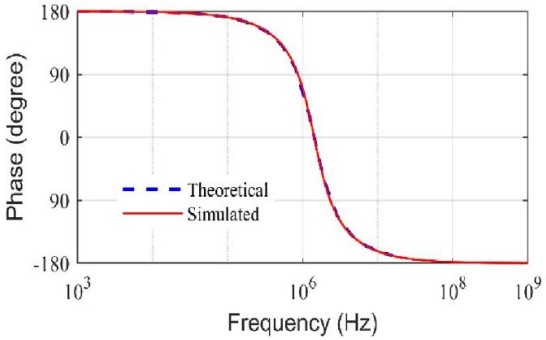

Fig. 9. Phase Response of AP Filter

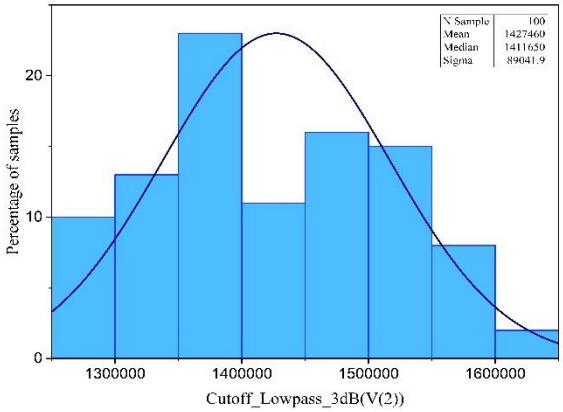

Fig. 10(a). Histogram result of LP Filter

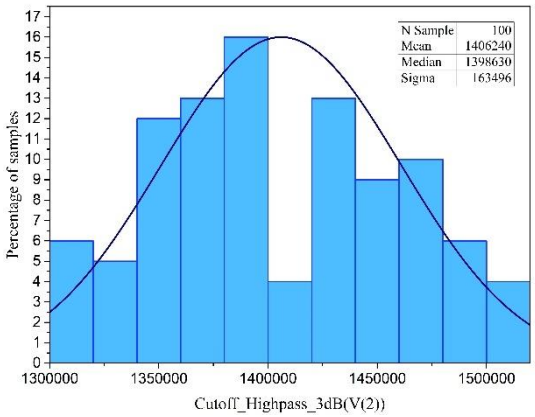

Fig. 10(b). Histogram result of HP Filter

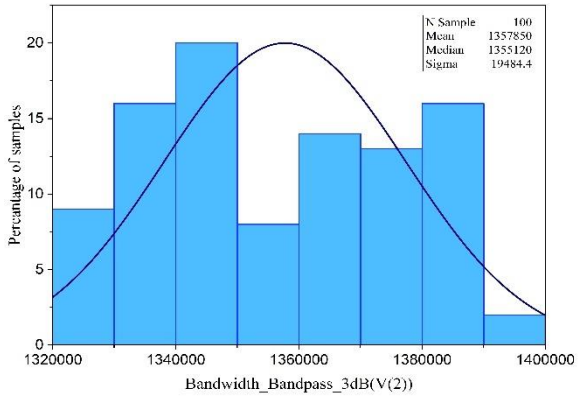

Fig. 10(c). Histogram result of BP Filter

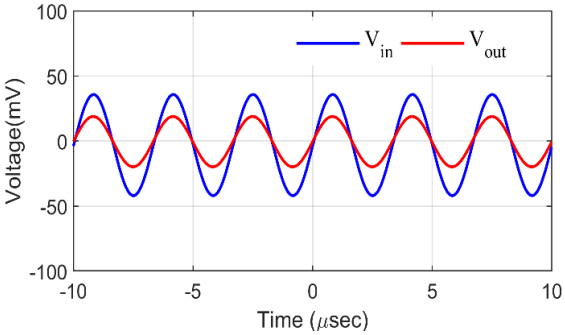

Fig.11(a). Transient Response of LP Filter

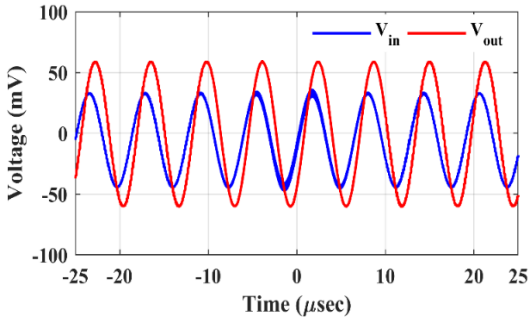

Fig. 11(b). Transient Response of HP Filter

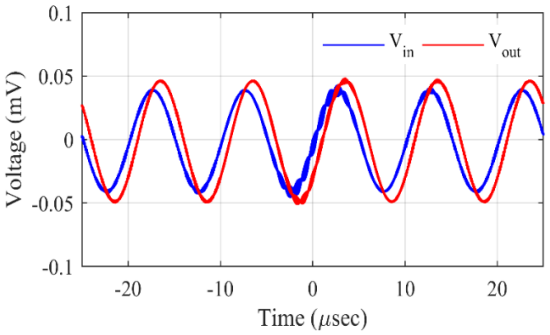

Fig. 11(c). Transient Response of BP Filter

4. Conclusion

This filter configuration offers several advantages: (i) it uses only single VDCC and three passive components, making it straight-forward for integration, (ii) it can produce all the standard filter responses without the need for component matching, (iii) it allows independent control of the parameters ω_o and Q, (iv) the total power dissipation of the circuit is 4.9mW which is very low. The functionality of the proposed circuit was validated through simulation results in PSPICE.

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Status of Conference Paper Submitted to PICS-2025 (Revision)

1 message

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Single CMOS VDCC-based voltage mode universal filter

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***Abstract*— This study validates a voltage-mode (VM) triple-input, single-output (TISO) biquad filter that employs a single voltage differencing current conveyor (VDCC) along with two capacitors and two resisters. The proposed configuration is capable of realizing all five standard biquad filter functions: high-pass filter (HPF), low-pass filter (LPF), band-pass filter (BPF), band-stop filter (BSF), and all-pass filter (APF). Additionally, the circuit allows for the adjustment of the cutoff frequency (ω_0) and pole quality factor (Q). The configuration was designed and simulated using PSPICE, and the simulation results were cross-verified with theoretical expectations.**

Keywords*— Biquad, VM, VDCC, Filter, Analog signal processing, TISO, Single input double output.

INTRODUCTION

In many ways analog filters are essential, such as electronics, mechatronics, and analog signal processing, as they enhance system functionality by removing noise, interference, and signal distortion. This paper presents an innovative analog filter design utilizing the VDCC. The proposed voltage mode universal filter configuration is designed with a focus on minimizing both equipment size and power consumption, making it an ideal choice for integration into compact systems. Its voltage-mode configuration ensures effective handling of a broad spectrum of AC signals without compromising signal integrity.

First, Over the years, numerous filters utilizing the Voltage Differencing Current Conveyor (VDCC) as an active building block (ABB) have been developed and documented in the literature, such as [1]-[13]. These filters are categorized into two primary configurations: voltage mode (where both input and output depend solely on voltage) [1-7], and current mode (where both input and output are determined by current) [7-9]. Furthermore, they can be classified based on their structure as single VDCC-based or multiple VDCC-based filters configuration.

A generalized scheme for the realization of biquad filter has been discussed in [1]. Three different single VDCC circuits has been implemented, one of the TISO type filtering category circuit has been provided, which can allow all types of filtering functions, another circuit were implemented SIDO type filtering category, including four passive components has been provided only HP and BP filtering functions, the last one is SIDO type filtering category, including four passive components (two resistor and two capacitor) has been provided only LP and BP filtering functions. ω and Q can be tunable in second and last filtering category. In [2], a MISO type filter configuration employing single VDCC, one resistor and two ungrounded capacitors has been presented with independent control of ω and Q. A Two Thomas VM filter configuration with two VDCCs, two capacitors and five resistors were provided BP filter configuration in [3]. A voltage mode first-order APF with a SISO type has been implemented using single VDCC, two resistor (both floating) and capacitor (grounded) in [4], while [5] presented SISO type VM second order universal filter with single VDCC based on BJT structure with four passive components to obtain all five filters function. In [6] a SISO type filter configuration employing single VDCC using two resistors and two capacitors has been provided only BR filtering function and with separate control of ω and Q. Comprehensive study of previously reported VM filter using VDCC have been discussed in table 1.

TABLE I. COMPARISON OF VARIOUS VOLTAGE-MODE VDCC BASED BIQUAD FILTERS

Ref.	No. of VDCC	Filtering Category	No. of passive elements	Filters Realized
[1]	1	TISO	1R, 2C	LP, HP, BP, BS, AP
[2]	1	MISO	1R, 2C	LP, HP, BP, BS, AP
[3]	2	SISO	5R, 2GC	BP
[4]	1	SISO	2R, 1C	AP
[5]	1	SIMO	2C, 2R	LP, HP, BP, BS, AP
[6]	1	SISO	2C, 2R	BS
Proposed	1	TISO	2R, 2C	LP, HP, BP, BS, AP

This paper presents the utilization of the VDCC, a sophisticated active component with electronic tuning capabilities, in the development of a voltage-mode universal biquadratic filters. The VDCC, which integrates a transconductance amplifier and a second-generation current conveyor (CCII), serves as foundational element of the proposed configuration. The circuit configuration employs a single VDCC along with four passive components to achieve versatile functionality The circuit is capable of achieving LP, HP, BP, AP and BS filter responses within a single configuration. It features a high-impedance output and supports independent tuning of the quality factor (Q) and cut-off frequency (ω_o). The proposed configuration performance is verified through PSPICE simulations.

OVERVIEW OF VDCC

A VDCC is six terminal device as demonstrated in Fig. 1. Among these, P and N serve as the input terminals, while Z, X, W_N and W_P function as output terminals. The behaviour of the ideal VDCC is described by the characteristic equation (1).

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_Z \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ I_X \end{bmatrix} \quad (1)$$

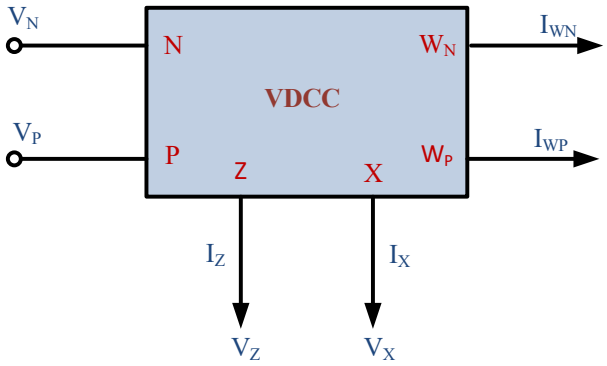

Fig. 1. Representation of VDCC

THE PROPOSED CONFIGURATION

VDCC based universal biquad filter is proposed in this section. Using a VDCC and four passive elements, the proposed design to achieve LPF, HPF, BPF, APF and BSF is demostrated in Fig. 2.

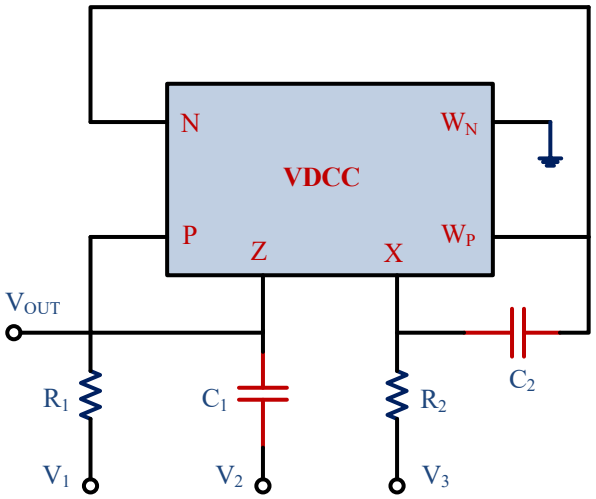

Fig. 2. The proposed filter configuraion

A circuit analysis of Fig. 2 (assuming ideal VDCC) gives the following transfer function (TF);

$$V_o = \frac{s^2 V_{in2} + s\frac{1}{C_1R_1}V_{in1} + \frac{g_m}{C_1C_2R_2}V_{in3}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (2)$$

Case I : For LPF, $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{\frac{g_m}{C_1C_2R_2}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (3)$$

Case II : For HPF, $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (4)$$

Case III : For BPF, $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s\frac{1}{C_1R_1}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (5)$$

Case IV : For APF, $V_{in2} = V_{in3} = V_{in}$ and $V_{in1} = -V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2 - s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (6)$$

Case V : For BSF, $V_{in1} = 0$ and $V_{in2} = V_{in3} = V_{in}$

$$\frac{V_o}{V_{in}} = \frac{s^2 + \frac{g_m}{C_1C_2R_2}}{s^2 + s\frac{1}{C_1R_1} + \frac{g_m}{C_1C_2R_2}} \quad (7)$$

The parameters such as ω_o and Q of the LPF, HPF, BPF, APF and BSF (derived by using (1)) of this filter are given by:

$$\omega_o = \sqrt{\frac{g_m}{C_1C_2R_2}} \quad (8)$$

$$Q = \sqrt{\frac{g_mR_1C_1}{C_2}} \quad (9)$$

The proposed circuit allows independent tunning of ω and Q. The filter response with desired value of ω_o was obtained by making $C_1=C_2 =C$ in (8) Note that it is possible to vary the values of C1 and C2 simultaneously by utilizing capacitor arrays [11].

SIMULATION RESULTS

To validate the operation of the proposed circuit in Fig. 2 PSPICE simulation utilizing TSMC 0.18um CMOS technology was performed. The design of a voltage-differential current-conveyor (VDCC) circuit utilizing CMOS technology in PSpice is illustrated in fig.-3. In the fig., a transconductance amplifier comprised of transistors M_1 to M_8 is also depicted. The current conveyor is composed of transistors M_9 to M_{22} in the fig.3. The direct current external bias is represented by I_{B1} and I_{B2}. Using [8], the transconductance parameter (g_m) of the VDCC is given by:

$$g_m = \sqrt{I_{B1}\mu_1 c_{ox}\left(\frac{w}{l}\right)_1} \quad (10)$$

where μ_1 indicates the electron mobility, the oxide capacitance per unit area at the gate is represented by c_{OX}, and w and l denote channel width and length of CMOS transistor, respectively. The dimensions of the transistors are listed in Table 9. The power supply voltages were configured as $V_{DD} = -V_{SS} = 0.9$ V, and the bias current of I_{B2} was 100 μA.

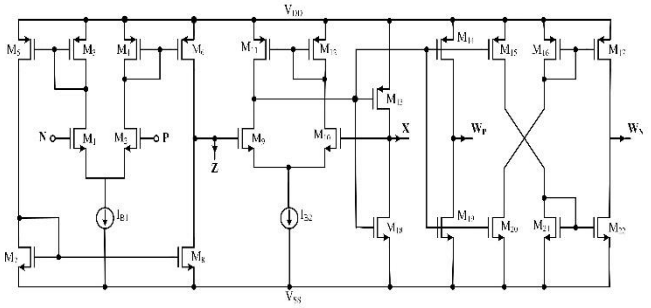

Fig. 3. CMOS implementation of the VDCC [8]

TABLE II. ASPECT RATIO OF THE CMOS DEVICES [8]

Transistor	W (μm)/ L (μm)
M_1 - M_4	3.6/1.8
M_5, M_6	7.2/1.8
M_7, M_8	2.4/1.8
M_9, M_{10}	3.06/0.72
M_{11}, M_{12}	14.4/0.72
M_{13} - M_{17}	0.72/0.72
M_{18} - M_{22}	0.72/0.72

The proposed LPF, HPF, BPF, BSF, and APF filters were designed with ω_o of 1.26 MHz and a Q of 0.7. The chosen component values were $C_1=C_2=50$pF, $I_{B1}=50$ µA, $R_1=R_2=1.768$ kΩ, and $g_m=277$ µ℧. The simulated magnitude responses of the filters, obtained using PSPICE, are illustrated in Figs. 4 to 8. From the analysis of these results, the cut-off frequency was determined to be 1.21 MHz, which is marginally lower than the theoretical value of 1.26 MHz. Fig. 9 presents the simulated phase response of the APF at 1.21 MHz, evaluated using MATLAB. The results depicted in Figs. 4 to 9 demonstrate that the proposed configuration effectively operates as a universal filter. Additionally, to evaluate the impact of capacitor tolerance on the cut-off frequency, a Monte Carlo simulation was conducted with 100 samples, considering a 10% tolerance for the capacitors, as shown in Figs. 10 to 13. The independent adjustment of cut-off frequency ω_o with fixed quality factor is shown in Figs. 14 to 17. To obtain this the value of R_2 is taken as 1.5kΩ, 1.75kΩ and 2kΩ.

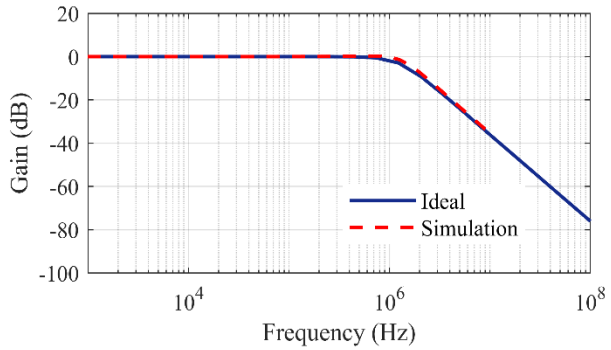

Fig. 4. Ideal and simulated respose of LPF

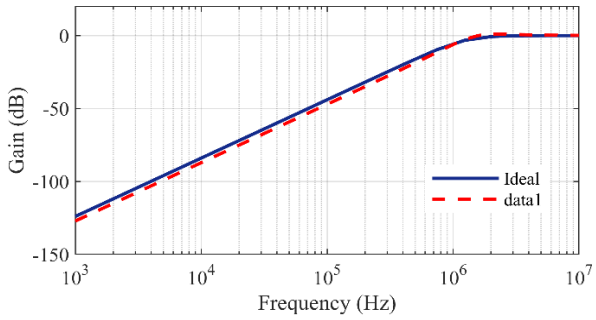

Fig. 5. Ideal and simulated response of HPF

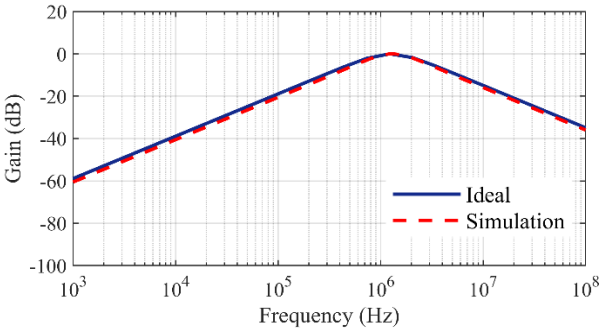

Fig. 6. Ideal and simultaed response of BPF

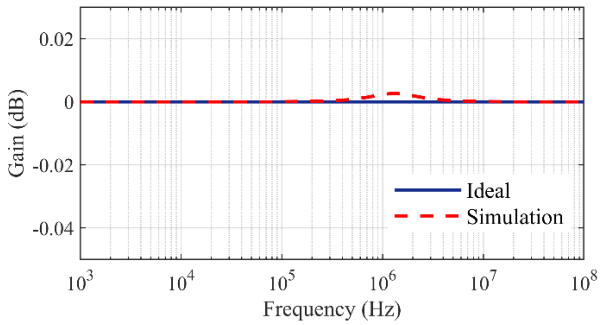

Fig. 7. Ideal and simulated response of APF

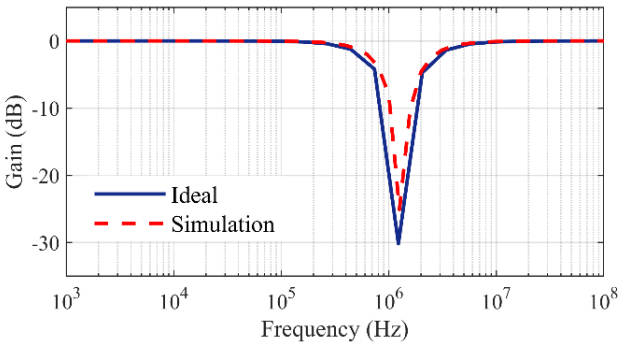

Fig. 8. Ideal and simulated response of BSF

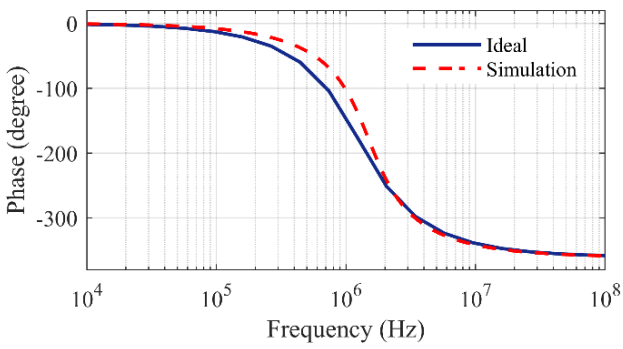

Fig. 9. Ideal and simulated phase response of APF

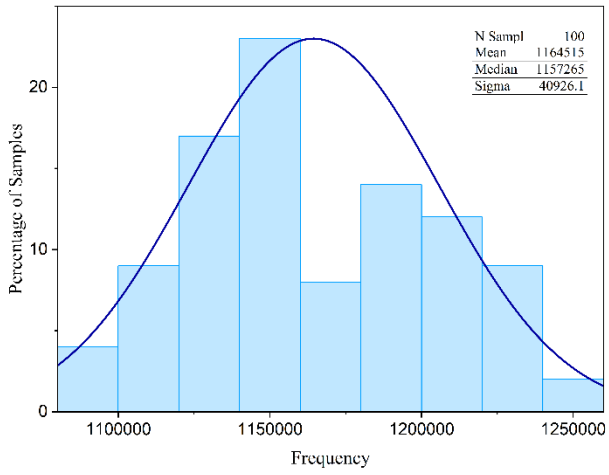

Fig. 10. Monte Carlo analysis for LPF

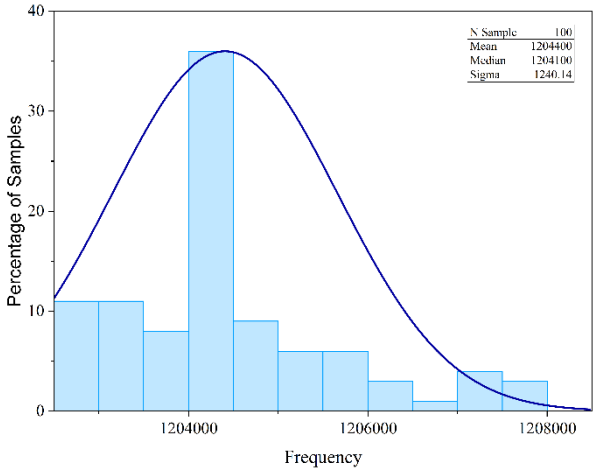

Fig. 12. Monte Carlo analysis for BPF

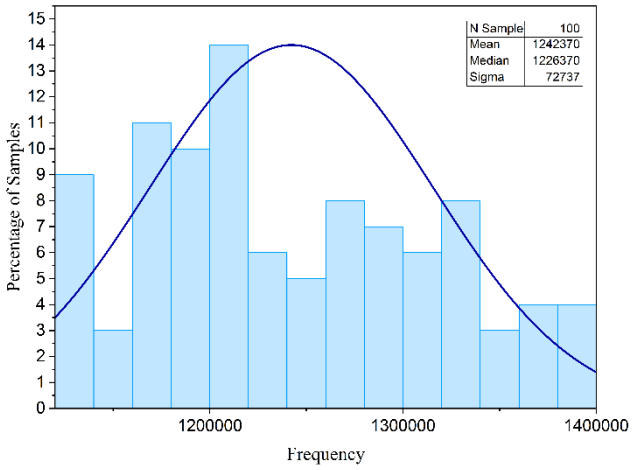

Fig. 11. Monte Carlo analysis for HPF

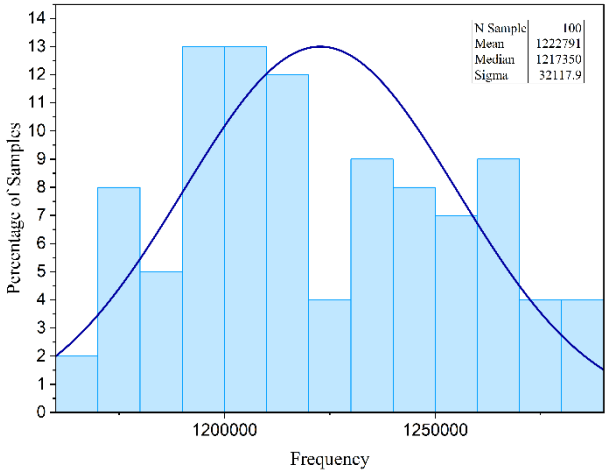

Fig. 13. Monte Carlo analysis for APF

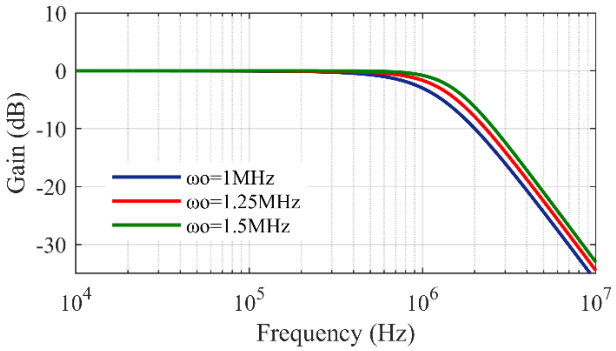

Fig. 14. Variation of ω_o for LPF (fixed Q)

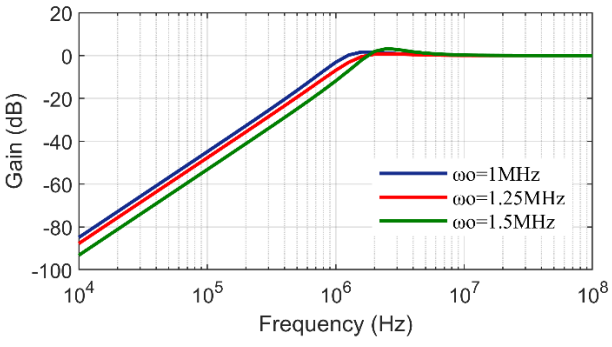

Fig. 15. Variation of ω_o for HPF (fixed Q)

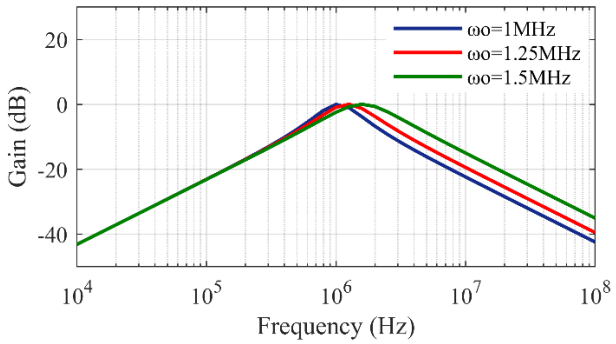

Fig. 16. Variation of ω_o for BPF (fixed Q)

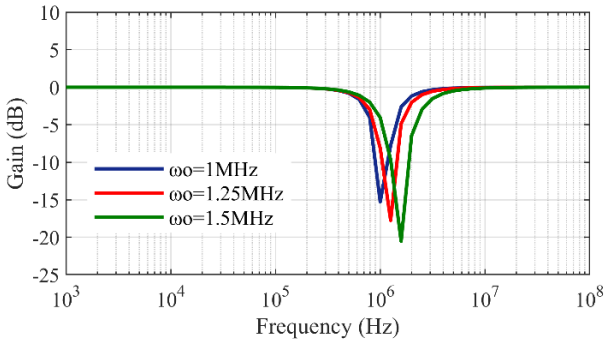

Fig. 17. Variation of ω_o for BSF (fixed Q)

CONCLUDING REMARKS

This paper validates a universal biquad filter design based on a single VDCC. Depending on the passive components used, the suggested design can produce LPF, HPF, BPF, APF and BSF responses. It can produce all the standard filter responses without the need for component matching, simulations of the all five filters were performed using the CMOS VDCC model to verify their performance. Additional validation is performed using Monte Carlo analysis.

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