Realization of various Linear and Non-linear Applications using Current Mode Building Blocks

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by

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CANDIDATE DECLARATION

I hereby certify that the research presented in this thesis, entitled "Realization of various Linear and Non-linear Applications using Current Mode Building Blocks," in fulfilment of the requirements for the award of the degree of Doctor of Philosophy, is an authentic record of my research work carried out under the supervision of Dr. Deva Nand.

The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for awarding any degree.

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CERTIFICATE

This is to certify that the thesis entitled **"Realization of various Linear and Non-linear Applications using Current Mode Building Blocks"** being submitted by Ms. Sweta Kumari (2K18/PHDEC/503) for the award of the degree of Doctor of Philosophy in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, is the record of students own work carried out by her under my supervision. The contents of this research work have not been submitted in part or fully to any other institute or university for the award of any degree.

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ABSTRACT

The rapid evolution of semiconductor technology has enabled the integration of millions of transistors on a single chip, diminishing the gaps between analog and digital domains. This trend has led to the rise of integrated solutions that incorporate both analog and digital subsystems on a single die. Despite a significant shift towards digital circuit design over the past two decades, analog design remains essential, particularly for functions such as signal processing, amplification, filtering, and conversion between analog and digital signals. The demand for high-performance analog interface circuits continues to grow with the emergence of new applications.

Designing analog circuits faces challenges due to the ongoing scaling of device dimensions and power supply voltages. Reduced power supply voltages can limit input common-mode range, linearity, and output voltage swing. Analog circuits can be classified as voltage mode (VM) or current mode (CM) based on whether they process information via nodal voltages or branch currents. Scaling adversely affects VM circuits' performance parameters, including dynamic range, slew rate, and common-mode range. In contrast, CM circuits offer enhanced slew rate, wider bandwidth, and better dynamic range due to smaller time constants and the ability to utilize transistors up to their unity-gain bandwidth. Additionally, CM circuits can be more compact, as current addition is achieved by simply connecting branches.

To leverage the advantages of CM signal processing, various analog building blocks have been developed. Components like Differential Difference Current Conveyors (DDCC), Differential Difference Current Conveyor Transconductance Amplifiers (DDCCTA), and Extra-X Current Controlled Current Conveyor Transconductance Amplifiers (EXCCCCTA) combine the features of current conveyors and current feedback operational amplifiers, with added current outputs to enhance design flexibility. These blocks are well-suited for processing and delivering both current and voltage at appropriate impedance levels, making them invaluable in modern analog circuit design.

A novel voltage-mode First Order Universal Filter (FOUF) utilizing a single DDCC combined with one resistor and one capacitor is presented. The proposed FOUF, designed as a multiple-input single-output (MISO) configuration, provides low-pass, high-pass, and all-pass responses, achieving a pole frequency of Mega Hz. Additionally, the application of the filter in a trans-admittance mode (TAM) controller is presented. This TAM controller employs Proportional-Derivative (PD), Proportional-Integral (PI), and Proportional-Integral-Derivative (PID) configurations, utilizing a DDCCTA with three resistors and three capacitors. Key features include the use of grounded capacitors and independent electronic tuning of control parameters, enabling simultaneous PD, PI, and PID operations. The study explores the impact of DDCCTA non-idealities on the controller and demonstrates an enhanced gain-frequency response. The controller's effect on the step response of a DDCCTA-based second-order filter system is analyzed to validate its practical application.

Two novel designs for wave active filters (WAF) based on voltage mode and current mode configurations are presented. The first design utilizes a DDCC to implement a wave-active filter, with wave quantity processing forming the foundation of its operation. The DDCC serves as the analog building block (ABB) for executing mathematical operations such as lossy integration-subtraction, subtraction, summation, and inversion, which are essential for creating wave-active components like series inductors and shunt capacitors. This design is applied to develop low to high-order low-pass Butterworth filter topologies, with theoretical verification is provided for nth-order low-pass Butterworth filters (n = 2, 3, 4, 5, 6). The second design introduces a current-mode wave active filter employing the EX-CCCCTA. This approach features a simplified design using a single EX-CCCCTA, grounded passive components, and electronic tuning capabilities, making it well-suited for high-frequency applications up to approximately Mega Hz. Compared to passive filters, this current-mode WAF offers advantages such as tunable gain, compatibility with monolithic integration, and optimal input-output impedance. Both filters' performance is validated through Monte Carlo analysis, THD assessment, and noise analysis, demonstrating its efficacy in practical applications.

The CM full-wave rectifiers (FWR) use two distinct analog building blocks: DDCC and DDCCTA. The first design employs a DDCC, two MOS-based diodes, and three grounded resistors to implement CM full-wave positive and negative rectifiers in different topologies, achieving an operating frequency of Mega Hertz. The second design introduces an electronically tunable, dual-output CM FWR using a single DDCCTA, two MOS-based active diodes, and four grounded active resistors. A key advantage of this design is its high output impedance with dual outputs (positive and negative) simultaneously, enabling easy cascading with other circuits. The work thoroughly analyzes the effects of non-idealities, including non-unity transfer gains and parasitic elements, on the circuit's performance. Additionally, Monte Carlo simulations are performed to validate the robustness and practical applicability of the proposed designs.

To evaluate functionality and performance, SPICE and Virtuoso simulators are used with 180 nm TSMC CMOS technology and 180 gpdk parameters, respectively. Various simulations are carried out to demonstrate the effectiveness of all proposed designs.

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Introduction

1.1 Introduction

A system is known as very large scale integration (VLSI) because of involving integration of millions of transistors on a single chip to enable the functioning of highly complex integrated circuits (ICs). Complementary Metal-oxide-semiconductor (CMOS) technology is the heart of modern VLSI systems and a widely used form of Analog circuit design. CMOS technology allows designers to optimize parameters like speed of operation, power dissipation and chip size which leads to more efficient systems-on-chip (SoC) designs [1]. To be familiar with the basics of microelectronic circuits such as how transistors work, and how to build a circuit from those basic components. It allows us to show the extreme difference between properly designed digital logic to analog design [2] which is important for the VLSI design development. Furthermore, the design of analog CMOS integrated circuits is essential for developing interfaces that connect digital components to the analog environment, which improves the capabilities of VLSI systems. This covers a wide range of functionalities, from basic transistor behavior and digital logic design to advanced approaches in analog circuits, demonstrating the scope of VLSI advancements [3].

The operational amplifier (Op-amp) is a useful device, having several applications, nevertheless, it has a limited amplification factor, poor slew rate, and a non-uniform bandwidth product. Furthermore, the op-amp-based designs often require exactly passive components that face challenges such as the need for internal matching and a large number of non-canonical features. To overcome these limitations, researchers and circuit designers have developed various alternatives to analog building blocks (ABBs) over the past decades [4]. Fundamentally, an op-amp operates as a voltage-controlled voltage source (VCVS), producing an output voltage dependent on the differential voltage at its input terminals. Most of the active devices implement one of four types of controlled sources: VCVS, voltage-controlled current source (VCCS), current-controlled voltage source (CCVS), and current-controlled current source (CCCS). These controlled sources enable different modes of circuit operation, namely

voltage mode, current mode, trans-impedance mode, and trans-admittance mode. A comprehensive review provides a unified framework for developing new ABBs with diverse features [5]. In practice, input sources of amplifiers are not ideal; a voltage source has a non-zero output resistance, and a current source has finite output resistance. Similarly, loads driven by an amplifier could vary from very low to very high impedance. Thus, the circuit designers must have the degree of flexibility to select amplifier types appropriate to the needs of the applications.

The open-loop gain for VCVS or Voltage amplifiers, in the case of the input source being of negligible output impedance along with the load impedance being quite high requires the amplifier to have a high (ideally infinite) input impedance and low (ideally zero) output impedance. This class of devices includes traditional op-amp, Differential Difference Amplifiers (DDA), Voltage Differencing Buffered Amplifiers (VDBA), and Voltage Differencing Inverted Buffered Amplifiers (VDIBA), which use voltage for both input and output, leading to high input as well as low output impedance. If the source that is outputting to the amplifier is low, as well as the load that the amplifier drives, the input impedance and output impedance will be high. The VCCS, or trans-conductance amplifiers use an input voltage and output current. These include high input-output resistance, like operational trans-conductance amplifier (OTA), voltage-differential transconductance amplifiers (VDTA), and voltage-differential current conveyors (VDCC), etc. If the input source has a high output impedance and the load impedance is low, the amplifier must have low input impedance (ideally zero) and high output impedance (ideally infinity). This is where the CCCS comes in, current amplifiers meet this need and furnish a controlled current as defined by the input current. This includes Current Conveyor (CC), Current Differential Transconductance Amplifier (CDTA), Current Differential Current Conveyor (CDCC), Dual X Current Conveyor Transconductance Amplifier (DXCCTA), Current Controlled Transconductance Amplifier (CCTA). On the other hand, if both input source output impedance is high, and the load impedance is high, the amplifier would need low input, and output, impedance. This is the domain of the trans-resistance amplifier, or CCVS, which accepts a current input and produces a voltage output. Current difference buffered amplifiers (CDBA), current difference differencing input buffer amplifiers

(CDDIBA), current difference differencing output buffer amplifiers (CDDOBA), and operational trans-resistance amplifiers (OTRA), all with ideally zero input and output impedance [4-5].

A signal in both digital and analog circuitry can be understood better with the help of the two basic design techniques: Voltage mode (VM) and current mode (CM). Using this method, the circuits are built around voltages across components, an approach that is extremely common in CMOS technology because of its robustness, ease of integration, and low power consumption. For the aforementioned reasons, CMOS VLSI design in general utilizes VM circuits in its digital logic functions. On the other hand, the CM design revolves around the idea of current flowing through a circuit to signify a signal and this kind of signal representation provides many benefits including high speed, greater linearity, and better performance on low-power configurations.
Various analog VLSI design blocks have been created to leverage CM signal processing advantages. Op-amps are key components in VM circuits, recognized for their high gain and input impedance. Other important blocks include the current differencing buffer amplifier (CDBA) [34, 75] and voltage differencing buffer amplifier (VDBA) [61]. Current conveyors (CCs) which exist in multiple versions (CCI, CCII, CCIII) [14, 24, 32, 87, 89, 95, 108, 112], are essential in CM designs and frequently used in current mirrors. More sophisticated conveyors like Differential Voltage Current Conveyors (DVCC) [13, 18, 19, 41, 111], Extra-X Current Conveyors (EXCCII) [80], and Dual-X Current Conveyors (DXCCII) [109, 116] support complex applications such as chaotic circuits and analog computation. Operational Floating Current Conveyors (OFCC) [72] and Differential Difference Current Conveyors (DDCCs) [96, 106] broaden the capabilities of CM designs. OTAs, critical for converting input voltage into output current, find widespread use in tunable filters, oscillators, and multipliers. Their tunability is ideal for low-power, programmable circuits. Other significant blocks include the Current Differencing Transconductance Amplifier (CDTA) [20, 26, 67, 69, 71, 123], Voltage Differencing Transconductance Amplifier (VDTA) [59, 60, 124], and Differential-Difference Transconductance Amplifier (DDTA) [63, 129]. Cascading blocks like the Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA) [10], Extra-X Current

Controlled Current Conveyor Transconductance Amplifier (EXCCCCTA) [11], and Dual-X Current Conveyor Transconductance Amplifier (DXCCTA) [109, 116] enhance the flexibility, tunability, and functionality of analog VLSI designs. These advanced building blocks are essential for achieving better precision, enhanced performance, and lower power consumption, making them crucial in current low-power and high-performance analog VLSI circuits.

In VLSI design, analog circuits play a crucial role in facilitating both linear and non-linear applications that are essential for various contemporary systems such as communications, signal processing, and instrumentation. The integration capabilities of VLSI technologies enable the incorporation of multiple analog components onto a single chip, greatly improving performance in terms of area efficiency, power consumption, and operational speed. This thorough analysis explores the design and implementation of these applications, emphasizing how analog components are utilized within the VLSI framework. Linear applications, which include filters, amplifiers, and oscillators, are examined for their potential to maximize key performance metrics. These metrics include bandwidth improvement, power efficiency, and the reduction of circuit area, all of which are vital for creating compact and efficient systems. Filters are crafted to achieve specific frequency responses, amplifiers seek to deliver stable gain with minimal distortion, and oscillators concentrate on producing consistent and reliable frequencies. The design process entails careful consideration of trade-offs among power, speed, and area, guaranteeing that the integrated circuits fulfill the rigorous demands of current applications. Conversely, non-linear applications like rectifiers, multipliers, and waveform generators leverage the inherent non-linear characteristics of analog components to realize high-speed and effective designs. Rectifiers are vital for converting AC signals to DC, multipliers find their use in modulation and demodulation tasks, and waveform generators are essential for producing various signal shapes needed in testing and communication systems. These non-linear applications are specifically designed to enhance operational speed and efficiency, meeting the increasing demand for high-performance analog parts in sophisticated VLSI systems.

In conclusion, the role of analog circuits in VLSI design encompasses a broad use of linear and non-linear applications. The continuous innovation in analog building blocks and their integration into VLSI systems underscores the ongoing significance of analog design in achieving superior performance in contemporary electronic systems. As technology progresses, the exploration and optimization of these analog circuits will remain a cornerstone of VLSI design, driving the development of more advanced and efficient systems.

1.2 Available literature and scope of work

Filters are crucial in signal processing, designed to allow or reduce certain frequency ranges in a signal. They can be categorized as low-pass (LP), high-pass (HP), all-pass (AP), band-pass (BP), or band-stop (BS) [6]. Filters help remove noise, isolate signals, and shape frequency responses. In control systems, they are vital for stable operations, enhancing signal quality, and improving control accuracy by reducing noise and filtering high-frequency interference. This boosts controller performance in applications like robotics, automation, and communication systems. Analog filters (LP, HP, AP) are significant for selecting frequencies and minimizing noise. While early designs using voltage-mode (VM) operational amplifiers (Op-Amps) are effective, they had high-frequency bandwidth limitations. Current-mode (CM) filters, using Current Conveyors (CCs) and Operational Transconductance Amplifiers (OTAs), provide better bandwidth and quicker responses, especially at high frequencies. AP filters are essential for altering phase response while maintaining amplitude, important for phase shifters and oscillators. Studies have introduced various first-order filter topologies utilizing active components like DXMOCCII [12], DVCC [13], CCIII [14], FDCCII [15], MO DXCCTA [16], VDCC [18], CCCDTA [20], and DBTA [21]. Some designs incorporate multiple blocks such as ICCII [23], CCII [24], DO CF [25], CDTA [26], OFCC [27], OTRA [28], and BJT [30]. These are assessed based on operational modes—VM [13, 28], CM [12, 16, 20, 23-26, 29, 30], TAM [27], and mixed-mode [14, 15, 17, 19, 21], and involving grounded or floating passive components [18-20, 23-27, 29]. Many designs aim for high input/output impedances, low total harmonic

distortion (THD), reduced noise, and efficient power usage. Structures that simultaneously provide low-pass, high-pass, and all-pass responses are emphasized [12, 13, 15, 17, 18, 23, 24, 27, 28, 30], especially in VM and CM configurations. Notably, AP filters are commonly used as oscillators [12, 17, 20, 25-27], highlighting the need for single analog building blocks (ABBs) with minimal passive elements.

In control systems, Proportional-Derivative (PD), Proportional-Integral (PI), and Proportional-Integral-Derivative (PID) controllers are widely used for the precise control of dynamic processes [7]. VLSI implementations with CM circuits have shown better dynamic response and low power consumption and are suitable for real-time feedback control applications in robotics and industrial automation. Active block-based controllers are being compared for CCII [31], DO-CCII [32], MO-CCCCTA [33], CCCDBA [34], CFOA [35, 39, 42], FDCCII [37], OTRA [38], DVCCTA [40], VDCC [41], CFTA [43], VCII [46], and CCTA [45]. Their operations in VM, CM, and mixed mode have been demonstrated to possess independent or dependent tunable parameters in terms of PD, PI, and PID configurations [31, 34, 37, 38, 40].

Although first-order and second-order filters are enough for most simple applications, advanced systems often require higher precision and selectivity, which can be achieved with higher-order filters. Higher-order filters have sharper roll-off characteristics and better frequency discrimination, allowing them to handle complex signal environments with closely spaced frequency components [6]. Of the higher-order filters, wave-active filters have the best dynamic range and energy efficiency. Taking advantage of wave propagation principles in the wave, such filters are quite efficient in managing high-frequency signals with variations of operational conditions; hence, it is particularly applicable in high-performance control systems, telecommunications, and power electronics for precision and robustness. Higher-order filters are implemented by cascading multiple first-and second-order stages, which results in an increased complexity of the filter and its improvement in frequency response. A better design for filters involves proper alignments of active circuit components like inductors and capacitors which directly impacts various properties such as the steepness of the cut-off slope, attenuation rate, and selectivity of the filters. Higher-order filters allow better

sharp cutoffs, increase specificity, and maximize attenuations that effectively remove signals without any significance at stopband positions. These features make them indispensable in applications like audio processing, communications, and medical devices, where precise frequency control is crucial. Apart from their noise and interference reduction capabilities, higher-order filters are significant in sensitive applications such as radar, biomedical technology, and RF communication. They also ensure stability and phase control, which are critical in control and communication systems requiring strict phase fidelity. There have been VM-based WAEs reported that incorporate a significant number of analog building blocks in their construction, except [17]. The realization of complex series inductors and shunt capacitors has been elaborated in various works [55, 56, 59, 64]. Second-order [63, 64], third-order [54, 57, 58, 62-64], and fourth-order [55, 56, 59-63] filters have been discussed in many sources. Advanced properties of these filters show their importance in modern electronic systems where high performance and reliability are considered critical.

Rectifiers are basic circuits in signal processing and power conversion. They are very important in the transformation of alternating current (AC) signals into direct current (DC) [8]. The conversion process is essential for the operation of electronic devices, as it guarantees that they obtain a consistent DC supply. Rectifiers are generally categorized into two types: half-wave and full-wave, with full-wave rectifiers providing enhanced efficiency and a more uniform output. This integration is very important in motor drives, power controllers, and audio applications where the absence of ripple on the DC output is considered crucial for achieving the maximum performance output. Full-wave rectifiers have various applications in signal processing, instrumentation, communication systems, radio frequency modulation, and demodulation, measurement of alternating current measurement instruments, detection of signal polarity, peak detection, and frequency doubling. The conventional configurations of the rectifier are primarily based on diodes and operational amplifiers. Such configurations limit the speed and efficiency of their operation. Current designs use CM methodologies and active components such as current conveyors to enhance performance in terms of speed and power consumption. Advanced rectifier topologies involve current-mode components, which include CCII [95], EXCCII [80], DVCC

[74], CDTA [67, 69, 71], OTA [74, 86], OTRA, CFDITA [84], CDBA [75], and OFCC [72]. Most of these utilize active elements and devices like diodes and MOS transistors to offer maximum efficiency for the variable loads due to their sensitivity. Most of these rectification topologies use diodes to rectify while others use MOS transistors [67, 69, 71]; however, most of them are not dual output in one configuration, except [80]. The current configurations of rectifiers portray the changing necessities of today's control and power conversion applications; they are offered greater efficiency and performance within increasingly complex systems.

A comprehensive literature review based on CM-based analog signal processing and generation circuits results in the following shortcomings:

(i) No designs for MISO-type Universal first-order filters using DDCC have been reported.

(ii) Until now, controller circuits involving DDCCTA have not been reported for independent tunability or equivalent resistance preservation.

(iii) Further, no such wave active filter designs involving DDCC and EXCCCCTA are reported, which includes a minimum number of passive components without considering component matching limitations.

(iv) To existing work, no reported work has demonstrated the ability of a DDCC and DDCCTA-based rectifier circuits to simultaneously generate positive and negative rectified outputs.

1.3 Thesis organization

The work presented in the thesis has been organized as follows:

Chapter 1 titled **Introduction**, provides an overview of the fundamental concepts of VLSI technology, focusing on CM blocks and their linear and non-linear applications.

Chapter 2 titled **Description of DDCC, DDCCTA & EXCCCCTA ABBs**, describes an overview of key analog building blocks used in thesis work and their applications in current circuit design. Understanding the functionalities and advantages of DDCC, DDCCTA, and EX-CCCCTA is crucial for developing efficient analog circuits.

Chapter 3 titled **Single ABB-based Filter and Controller Designs**, addresses reducing circuit complexity by employing single analog building blocks (ABB). Simplifying circuit designs is essential for reducing power consumption, lowering fabrication costs, and improving integration in VLSI systems. A Multiple Input Single Output (MISO) VM first-order universal filter using DDCC and TAM-based PD, PI, and PID controllers using a single DDCCTA are discussed.

Chapter 4 titled **VM and CM-based Wave-Active Filters**, focuses on improving the circuit responses in terms of accuracy, stability, and frequency performance. The design of an nth-order wave active low-pass filter using a DDCC and a Simplified Wave Active Filter realized using a single EX-CCCCTA are discussed.

Chapter 5 titled **Design and Analysis of Rectifiers**, addresses designing circuits, an MOS-based electronically tunable CM dual-output full-wave rectifier, utilizing a single DDCCTA and a CM positive and negative rectifier based on DDCC is presented.

Chapter 6, **Conclusion and Future Scope** summarizes the work presented in the thesis and identifies the future scope.

Chapter 2

Description of DDCC, DDCCTA and EX-CCCCTA Blocks

2.1 Differential Difference Current Conveyor (DDCC) Block

DDCC is a DDA cascaded with CCII, with three differential inputs at Y-terminals, one X-terminal, and one Z-terminal [9]. The current at all Y-terminals is shown to be zero as per equation (2.2). The X-terminal voltage is arithmetically proportional to the Y-terminal voltage of the equation (2.3). The Z-terminal current follows the X-terminal current as per equation (2.4), whether inward or outward direction. The X-terminal offers low impedance input, the Y-terminal a high impedance input, and the Z-terminal a high impedance output. The DDCC symbol is presented in Fig. 2.1(a). The terminal relations are shown as matrix characteristics in equation (2.1):

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \tag{2.1}$$

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \tag{2.2}$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \tag{2.3}$$

$$I_Z = \pm I_X \tag{2.4}$$

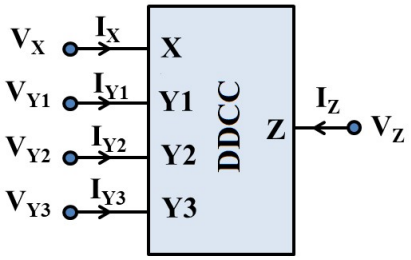


Fig. 2.1: Symbol of DDCC [9]

SPICE simulator with 180 nm TSMC CMOS technology parameters is used. The CMOS schematic of the DDCC block is shown in Fig. 2.2 and respective *W/L* ratios of nMOS and pMOS transistors are shown in Table 2.1. The supply voltages $V_{DD} = V_{SS} = \pm 0.9\ V$ and a bias voltages $V_b = -0.31\ V$ are used. In Fig. 2.2, the two input differential stages *(M1, M2)* and *(M3, M4)*, by considering the large gain phase, a current mirror *(M7 and M8)* transforms the differential current into a single-end output current *(M9)*. The *M10* duplicates the *M9* current.

Table 2.1: Aspect ratio of various transistors of DDCC [9]

Transistors	Aspect ratio W(µm)/L(µm)
All PMOS	10/0.4
All NMOS	05/0.4

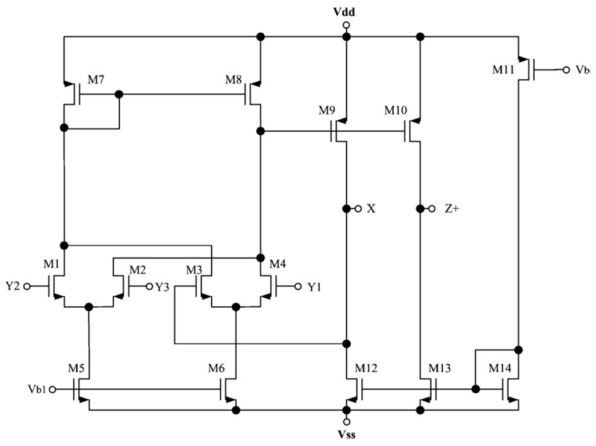


Fig. 2.2: CMOS schematic of DDCC block [9]

2.1.1 AC Characteristics

Fig. 2.3 plots the frequency response of voltage gains *(V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3})*. The cut-off frequencies of the voltage gains obtained without load are about 25 MHz, and the gains are unity at low frequencies.

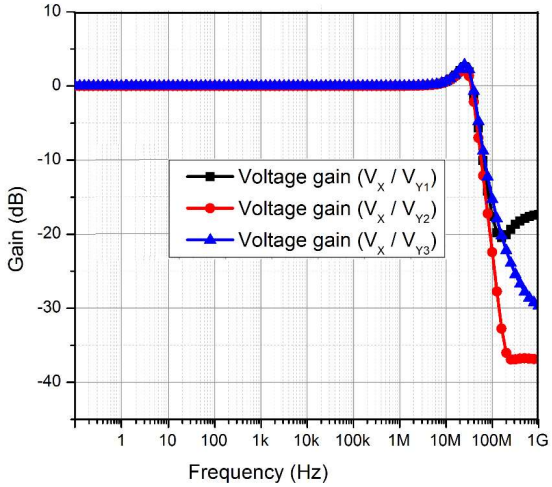


Fig. 2.3: AC response of Voltage at Y-terminals vs. voltage X-terminal

2.1.2 DC Characteristics

The DC voltage characteristics between the Y-terminals and X-terminal are presented in Fig. 2.4. The output voltages obtained to X-terminal V_X according to V_{Y1}, V_{Y2} and V_{Y3} show a common dynamic range extended from -50 mV to 50 mV

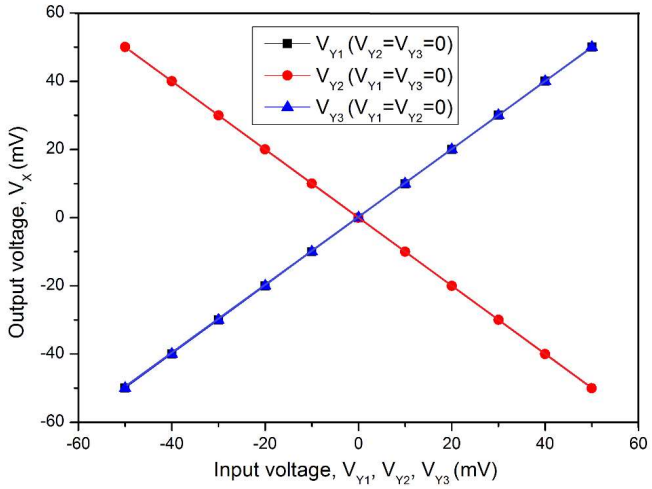


Fig. 2.4: DC response of Voltage at Y-terminals vs. voltage X-terminal

Fig. 2.5 shows the variation of output current I_Z versus the current I_X, with grounded Y terminals and a load resistance of about 1 kΩ, the current follower characteristic with a boundary linear range from -1 mA to 1 mA.

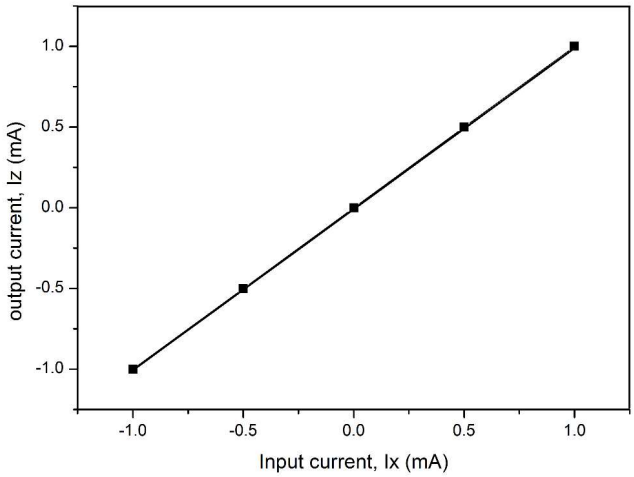


Fig. 2.5: DC response of Current at X-terminal vs. current Z-terminal

2.1.3 Non-ideal Effects

In Fig 2.6, the consideration of the non-ideal values of DDCC, the characteristic matric can be rewritten as:

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha_1 & -\alpha_2 & \alpha_3 & 0 \\ 0 & 0 & 0 & \pm\beta \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (2.5)$$

$$V_X = \alpha_1 V_{Y1} - \alpha_2 V_{Y2} - \alpha_3 V_{Y3} \quad (2.6)$$

$$I_Z = \pm \beta I_X \quad (2.7)$$

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \quad (2.8)$$

Where α_1, α_2 and α_3 are non-ideal voltage-transfer gains from $Y1$ to X, $Y2$ to X and $Y3$ to X-terminal respectively. $\pm\beta$ Is non-ideal current transfer gain from X to Z-terminal.

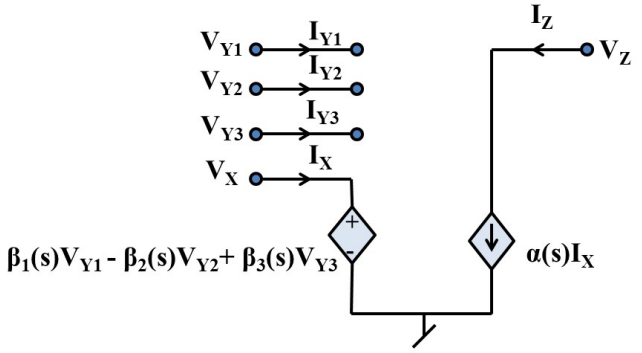


Fig. 2.6: Equivalent circuit of DDCC with frequency-dependent gains

2.1.4 Parasitic Effects

In Fig. 2.7, the parasitic effects of DDCC are characterized by:

- R_X is parasitic resistance that occurs at the X-terminal.
- R_{Y1} // C_{Y1}, R_{Y2} // C_{Y2} and R_{Y3} // C_{Y3} are parasitic impedances at Y_1, Y_2 and Y_3-terminals respectively.
- R_Z // C_Z is parasitic impedance at Z-terminal.

The passive component values including non-ideal parasitic resistances and impedances can be modified as:

$$Z_1 = R_{Y1} // (1/sC_{Y1}) \quad (2.9)$$

$$Z_2 = R_{Y2} // (1/sC_{Y2}) \quad (2.10)$$

$$Z_3 = R_{Y3} // (1/sC_{Y3}) \quad (2.11)$$

$$Z_4 = R_Z // (1/sC_Z) \quad (2.12)$$

$$Z_5 = R_X \quad (2.13)$$

The parasitic at the X-terminal terminal (R_X) is very low, the parasitic at Y-terminal terminals (R_Y, C_Y) is very high, 18 fF, the parasitic at the Z-terminal (R_Z, C_Z) is 200 kΩ, 30 fF. The power consumption of the DDCC circuit is about 2.94 mW.

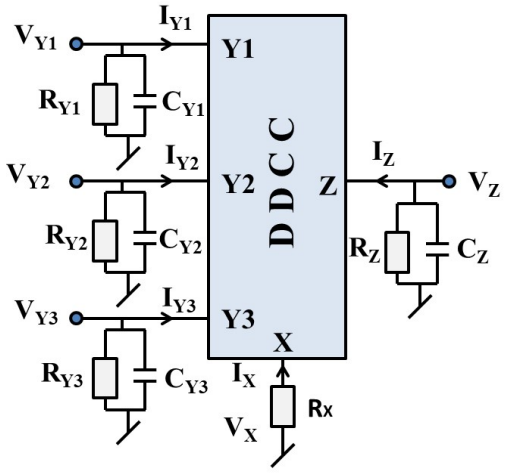


Fig. 2.7: Equivalent circuit showing parasitic elements in DDCC

2.2 Differential Difference Current Conveyor Trans-Conductance Amplifier (DDCCTA) Block

The DDCCTA analog building block is constructed by cascading of DDCC and OTA and its circuit symbol is shown in Fig. 2.8 [10] and its CMOS implementation is shown in Fig. 2.9. To clarify, the DDCCTA provides a single block, unified active component

for proposed circuit design by integrating the advantages of the OTA's transconductance properties with the DDCC's current conveyor characteristics. This integration is essential because it eliminates the need for extra discrete active components while allowing the DDCCTA to perform multiple functions efficiently, including high input and output impedances and enabling electronic tuning. The DDCCTA block has high impedance input Y (*Y1, Y2, Y3*) whereas the X-terminal is low impedance input, and while Z-terminal and O-terminals are the high impedance output terminals. The terminal characteristics are defined by the matrix given below as per equation (2.14):

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_Z \\ I_{O+} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & g_m \\ 0 & 0 & 0 & 0 & -g_m \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \end{bmatrix} \tag{2.14}$$

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \tag{2.15}$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \tag{2.16}$$

$$I_Z = \pm I_X \tag{2.17}$$

$$I_{O\pm} = \pm g_m V_Z \tag{2.18}$$

The trans-conductance (g_m) is electronically controllable by an electronic bias current (I_{bias}) and the value can be calculated as given in equation (2.19):

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_{bias}} \tag{2.19}$$

Where μ is the effective channel mobility, *Cox* is the gate-oxide capacitance per unit area, *W* and *L* correspond to the channel width and length of the MOS transistor (*M15 and M16 in Fig. 2.9*).

SPICE simulations are performed by using 180 nm TSMC CMOS technology. The width and length are mentioned in Table 2.2 for all transistors. The supply voltages are taken $V_{DD} = V_{SS} = \pm$ 0.9 V. The bias voltage V_{bias} and the bias current I_{bias} are taken as - 0.31 V and 50 µA respectively.

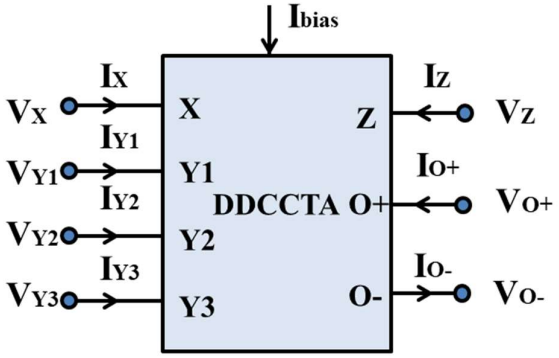


Fig. 2.8: Symbol of DDCCTA [10]

Table. 2.2 Aspect ratio of PMOS and NMOS transistors [10]

Transistors	Aspect ratio W(μm)/L(μm)
M1-M6, M11, M12	4.50/0.36
M7-M10	9.00/0.36
M13, M14	4.32/0.36
M15, M16	11.52/0.36
M17-M20	4.80/0.36
M21-M24	2.88/0.36
N1, N2, M_1R_{i*}, M_2R_{i*}	0.36/0.36

* i = 1,2,3,4

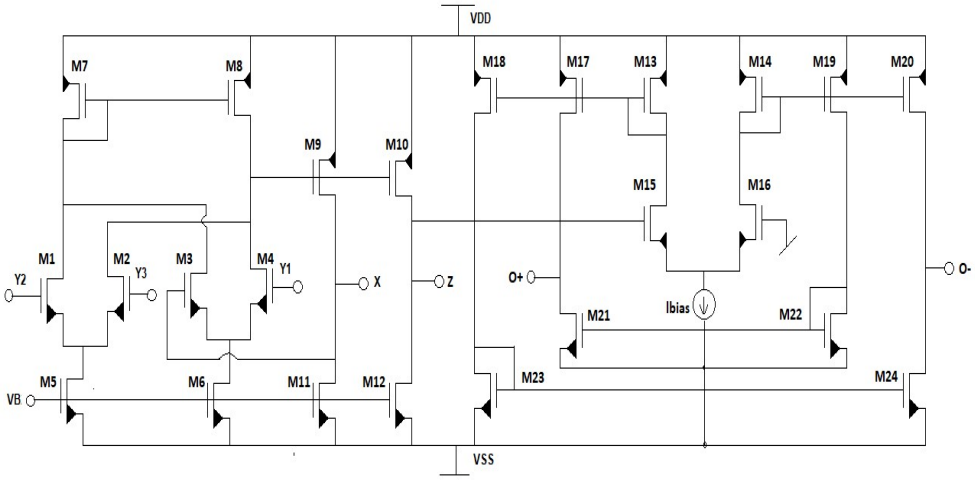


Fig. 2.9: CMOS implementation of DDCCTA [10]

2.2.1 AC Characteristics

Fig. 2.10 plots the frequency response of voltage gains *(V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3})*. The cutoff frequencies of the voltage gains obtained without load are about 45 MHz, and gains are unity at low frequencies. Fig 2.11 shows the OTA gain *($I_{O\pm}/V_Z$)* is 5 MHz when an input voltage of 1 mV is applied at the Z-terminal.

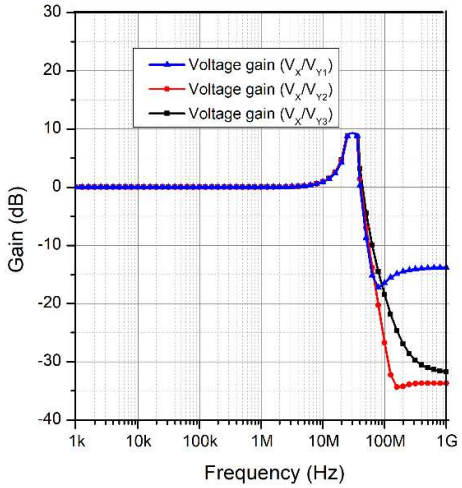


Fig. 2.10: AC response of Voltage at Y-terminals vs. voltage X-terminal

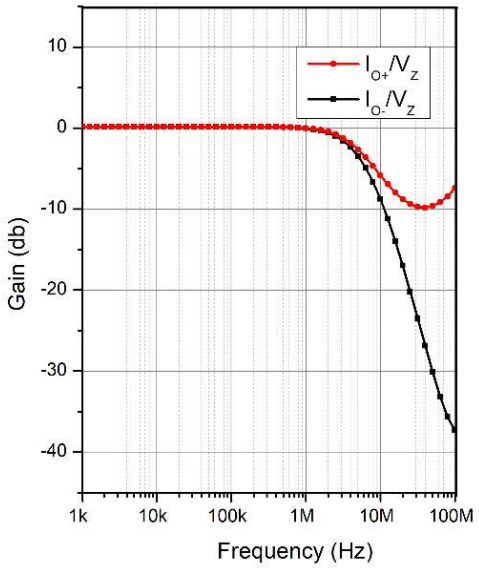


Fig. 2.11: AC response of Voltage at Z-terminal vs. current at O-terminal

2.2.2 DC Characteristics

The DC voltage characteristics between the Y-terminals and X-terminal are presented in Fig. 2.12. The output voltages obtained to X-terminal V_X according to V_{Y1}, V_{Y2} and V_{Y3} show a common dynamic range extended from -300 mV to 300 mV.

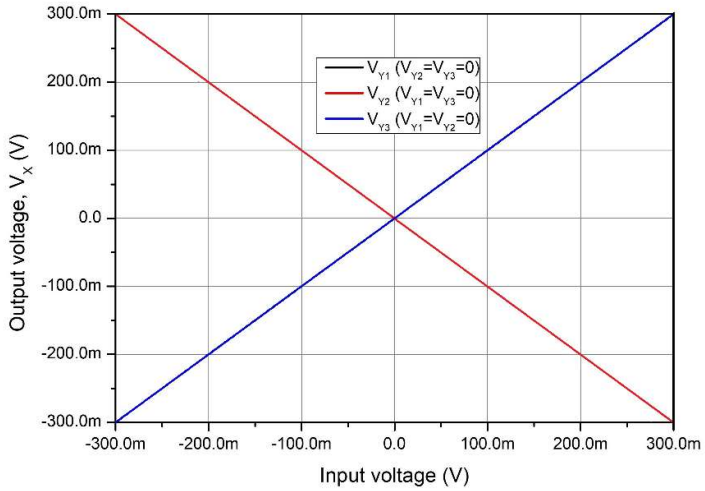


Fig. 2.12: DC response of Voltage at Y-terminals Vs voltage at X-terminal

Fig. 2.13 shows the variation of output current I_Z versus the current I_X, with grounded Y terminals and a load resistance of about 1 kΩ, the current follower characteristic with a boundary linear range from -300 µA to 300 µA .

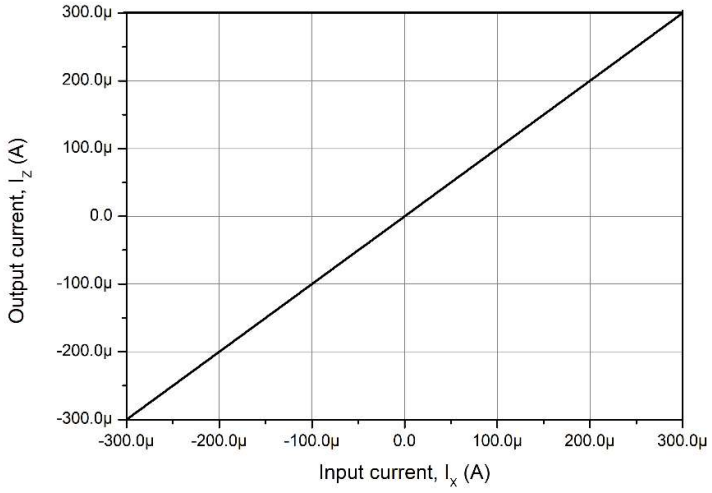


Fig. 2.13: DC response of Current at X-terminal Vs current at Z-terminal

Fig. 2.14 presents the DC voltage characteristics between the Z-terminals and O-terminals. The output current obtained to O-terminal ($I_{O\pm}$) according to voltage at Z-terminal (V_Z) shows a dynamic range extended from -55 µA to 55 µA and -75 mV to 75 mV, respectively.

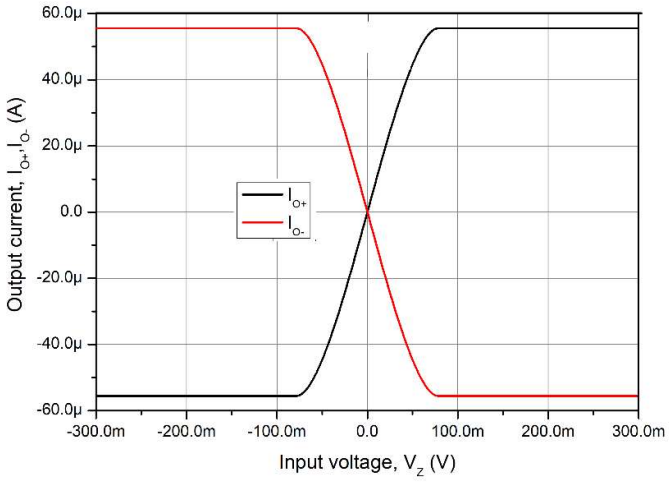


Fig. 2.14: DC response of Current at O-terminal Vs voltage at Z-terminal

The variation of the trans-conductance value by changing I_{bias} from 0 to 500 µA is depicted in Fig. 2.15. The increase in transconductance for larger bias currents. The maximum transconductance is about 3.1 mS.

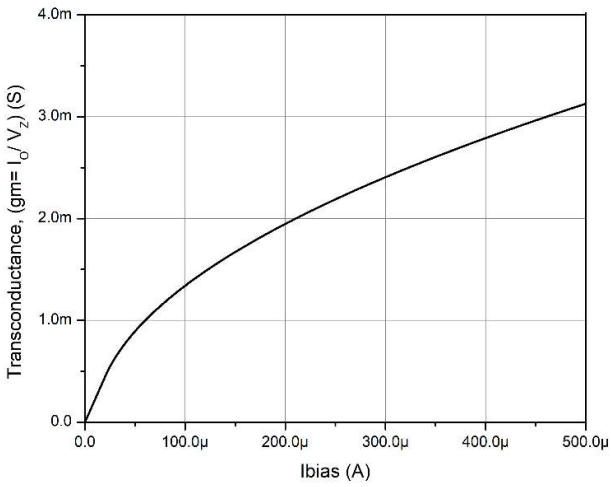


Fig. 2.15: Variation of transconductance with bias current

2.2.3 Non-ideal Effects

In Fig. 2.16, the impact of the non-ideal effect of DDCCTA may be examined by considering non-unity transfer gains and rewritten below in Eq. (2.20):

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_Z \\ I_{O+} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ 0 & 0 & 0 & \alpha & 0 \\ 0 & 0 & 0 & 0 & \gamma g_m \\ 0 & 0 & 0 & 0 & -\gamma g_m \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \end{bmatrix} \tag{2.20}$$

Where, β_1, β_2, *and* β_3 are non-ideal voltage-transfer gains from voltage *Y1, Y2, and Y3* to voltage X-terminal respectively. The α is the non-ideal current transfer gain from current X to current Z-terminal and the γ is the non-ideal trans-admittance transfer gain from voltage Z to current O-terminals.

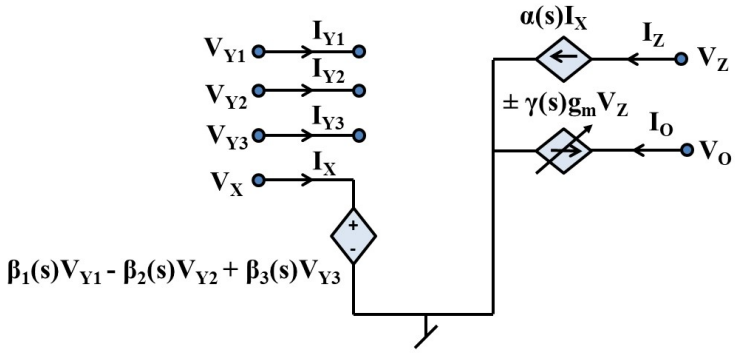


Fig. 2.16: Equivalent circuit of DDCC with frequency-dependent gains

2.2.4 Parasitic Effects

In Fig. 2.17, the parasitic effects of DDCC are characterized by:

- R_X is parasitic resistance that occurs at the X-terminal.
- R_{Y1} // C_{Y1}, R_{Y2} // C_{Y2} and R_{Y3} // C_{Y3} are parasitic impedances at Y_1, Y_2 and Y_3-terminals respectively.
- R_Z // C_Z is parasitic impedance at Z-terminals.
- R_O // C_O is parasitic impedance at O-terminals.

The passive component values including non-ideal parasitic resistances and impedances can be modified as:

$$Z_1 = R_{Y1} // (1/sC_{Y1}) \quad (2.21)$$

$$Z_2 = R_{Y2} // (1/sC_{Y2}) \quad (2.22)$$

$$Z_3 = R_{Y3} // (1/sC_{Y3}) \quad (2.23)$$

$$Z_4 = R_Z // (1/sC_Z) \quad (2.24)$$

$$Z_5 = R_O // (1/Sc_O) \quad (2.25)$$

$$Z_5 = R_X \quad (2.26)$$

The parasitic at the X-terminal terminal (R_X) is very low, the parasitic at Y terminals (R_Y, C_Y) very high, 20 fF, Parasitic at Z terminals (R_Z, C_Z) 218 kΩ, 35 fF, Parasitic at O− terminals (R_O, C_O) 324 kΩ, 20 Ff. The power consumption of the DDCC circuit is about 3.21 mW.

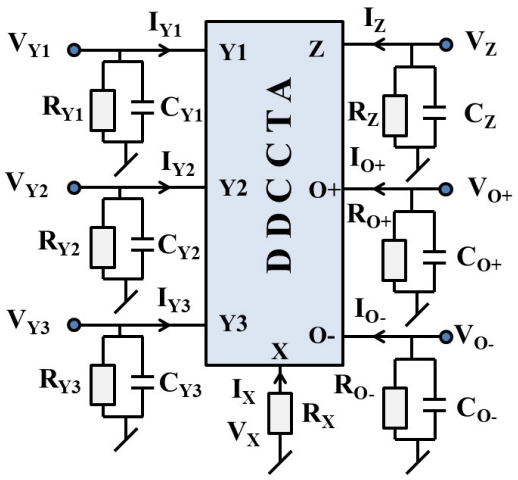


Fig. 2.17: Equivalent circuit showing parasitic elements in DDCCTA

2.3 Extra-X Current Controlled Current Conveyor Trans-Conductance Amplifier (EX-CCCCTA)

The Fig. 2.18 and Fig. 2.19 show the symbol and CMOS implementation of EX-CCCCTA. It has nine terminals. EX-CCCII [11] transistors (M1-M33) comprise the

first stage. At the X_1 and X_2 nodes, the voltage that is applied at the Y node is shown. Nodes $Z_{1\pm}$ and $Z_{2\pm}$ receive the current input from node X_1 and node X_2. The input current from the X_1 node flows to Z_{1+} and Z_{1-}, similarly, the input current from the X_2 node flows to Z_{2+} and Z_{2-} terminal current following operate independently of one another. The trans-conductance amplifier (TA) takes up the second stage and transistors (M34-M47) are used to implement. The voltage Z_{2-} determines the output current of the TA. The output current I_{O+} and I_{O-} of the TA is provided by Eq. (2.27) if all transistors operate in the saturation and transistors M41 and M42 have equivalent W/L ratios. Table 2.3 shows transistor sizes for EX-CCCCTA.

$$\begin{bmatrix} I_Y \\ V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \\ I_{O\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_{X1} & 0 & 0 \\ 1 & 0 & R_{X2} & 0 \\ 0 & \pm 1 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X1} \\ I_{X2} \\ V_{Z1} \end{bmatrix} \tag{2.27}$$

$$R_{X1} = R_{X2} = \frac{1}{\sqrt{8\mu C_{ox} \frac{W}{L} I_O}} \tag{2.28}$$

$$g_m = \sqrt{K_n \frac{W}{L} I_{bias}} \tag{2.29}$$

Where intrinsic resistances R_{X1} and R_{X2} are at terminals X_1 and X_2, I_O and I_{bias} are the bias currents of EX-CCCCTA, and, μ, C_{ox}, W, and L are the usual MOS transistor parameters.

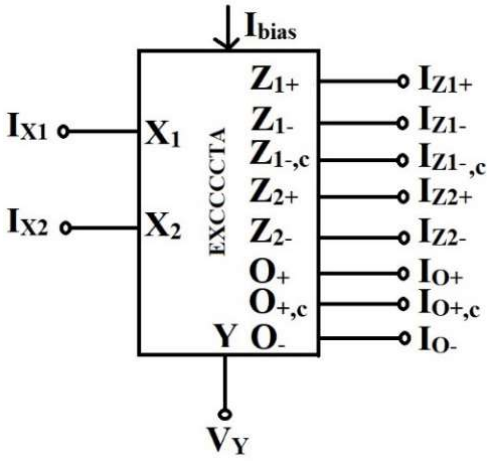


Fig. 2.18. Symbol of EX-CCCCTA [11]

Table 2.3 Transistor sizes for EX-CCCCTA [11]

Transistors	Aspect ratio W (µm)/L (µm)
M1-M3	7.2/0.36
M4-M6	11.52/0.36
All PMOS	4.32/0.36
All NMOS	7.2/0.36

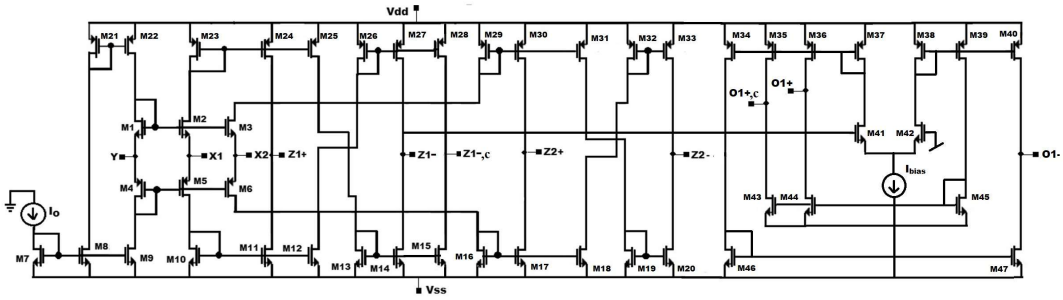


Fig. 2.19: CMOS structure of EX-CCCCTA [11]

The simulation employs 0.18 µm TSMC CMOS technology, with bias currents set at I_o = 10 µA, I_{bias} = 130 µA, and a supply voltage of ±1 V.

2.3.1 AC Characteristics

Fig. 2.20 plots the frequency response of current gains *(I_Z/I_X)*. The cutoff frequencies of the current gains obtained without load are about 2 GHz, and gains are unity at low frequencies.

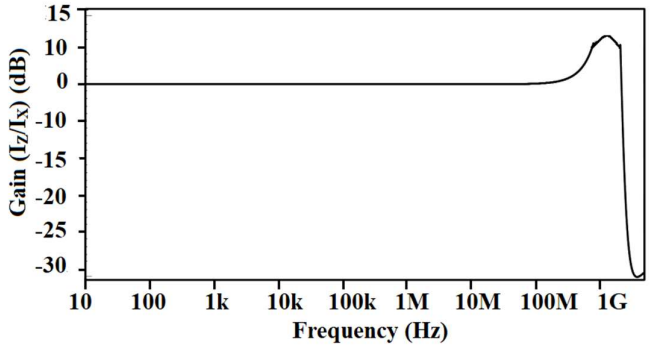


Fig. 2.20: AC response of current at Z-terminals vs. current at X-terminal

The bandwidth of the OTA which is found to be 330 MHz. The Fig. 2.21 gives the value of transconductance when the bias current is set at 100μA which is found to be 984μS.

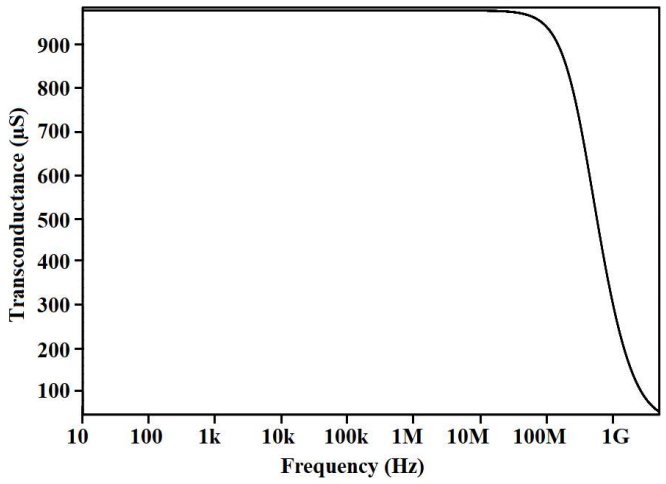


Fig. 2.21: Variation of transconductance with bias current

2.3.2 DC Characteristics

The DC voltage characteristics between the Y-terminals and X-terminal are presented in Fig. 2.22. The output voltages obtained to X-terminal V_X according to V_{Y1}, V_{Y2} and V_{Y3} show a common dynamic range extended from -1 V to 1 V

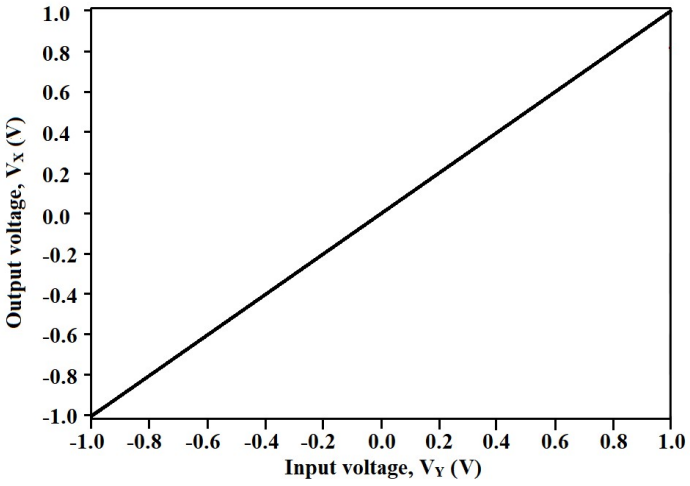


Fig. 2.22: DC response of Voltage at Y-terminals vs. voltage at X-terminal

Fig. 2.23 shows the variation of output current I_Z versus the current I_X, with grounded Y terminals and a load resistance of about 1 kΩ. The current follower characteristic has a boundary linear range from -200 µA to 200 µA.

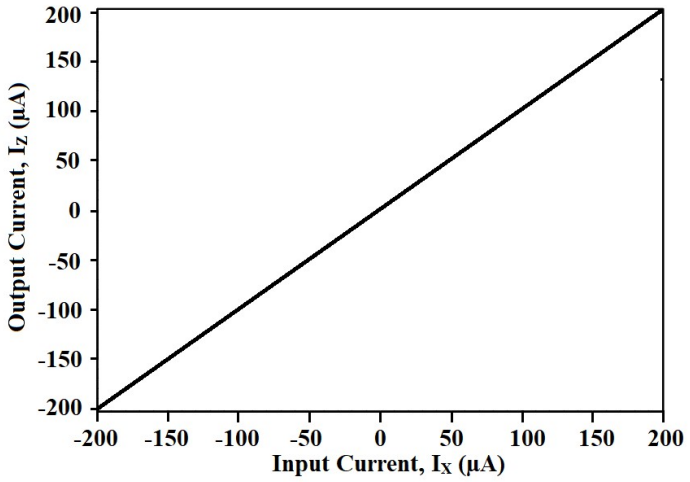


Fig. 2.23: DC response of Current at X-terminal vs. current at Z-terminal

A voltage sweep of ±300mV is applied at the V_{Z1} node and the output current flowing from the O+ and O− nodes is plotted. The linear range of the OTA is ±200 mV after this the output current began to saturate as can be inferred from Fig. 2.24.

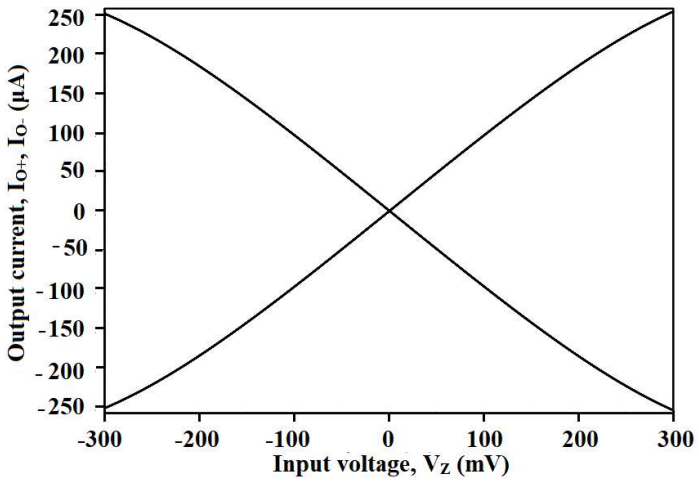


Fig. 2.24: DC response of Current at O-terminal Vs voltage at Z-terminal

2.3.3 Non-ideal Effects

A non-ideal model of EXCCCCTA is provided. Non-ideal frequency-dependent current and voltage transfer gains, $\alpha_i(s)$ and $\beta_i(s)$, are the primary factors leading to deviations in frequency performance. $\alpha_i(s) = \alpha_{0i}/(1 + s/\omega\alpha_i)$, and $\beta_i(s) = \beta_{0i}/(1 + s/\omega\beta_i)$. Ideally, $\alpha_{0i} = \beta_{0i} = 1$, and $\omega_{\alpha i} = \omega_{\beta i} = \infty$. To account for non-ideal gains, modify the EXCCCCTA's V-I relations to $I_Y = 0$, with $V_X = \beta(s)V_Y$. $I_{Z1+} = \alpha(s)I_{X1}$, $I_{Z1-} = -\alpha(s)I_{X1}$, $I_{Z2+} = \alpha(s)I_{X2}$, $I_{Z2-} = -\alpha(s)I_{X2}$, $I_{O+} = \gamma g_m V_{Z1-}$, and $I_{O-} = -\gamma g_m V_{Z1-}$.

2.3.4 Parasitic Effects

Fig. 2.25 shows an equivalent circuit showing parasitic elements in EX-CCCCTA. The performance of the X nodes can be defined as $Z_X = R_X + sL_X$. R_{Z+}, R_{Z-}, and R_Y represent the parasitic resistance and capacitance of the Y and Z nodes, respectively. The corresponding capacitances are C_{Z+}, C_{Z-}, and C_Y. The ideal values are equal to zero. The γ reflects the OTA's transconductance transfer inaccuracy, whereas R_O and C_O are parasitic at the output.

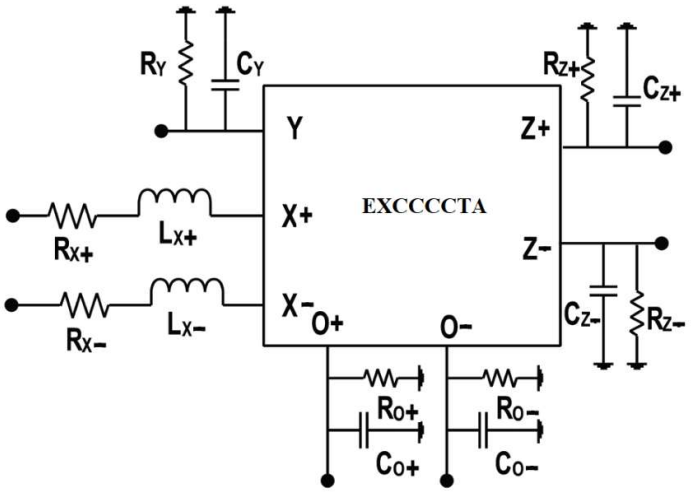


Fig. 2.25: Equivalent circuit showing parasitic elements in EX-CCCCTA [11]

Chapter 3

Single ABB-based Filter and Controller Designs

1. S. Kumari and D. Nand, “DDCC-based MISO type voltage mode First-order Universal Filter,” *2022 2nd International Conference on Intelligent Technologies (CONIT 2022)*, Hubli, India, 2022, pp. 1-6. https://doi.org/10.1109/CONIT55038.2022.9847828.
2. S. Kumari and D. Nand, “Realization of TAM-based PD, PI, PID Controllers Utilizing a Single DDCCTA for Closed-Loop System Applications”, (2024).

3.1 Introduction

Audio amplifiers, equalizers, speaker systems, image processing, integrators, AC coupling, various control systems, radio systems, communication subsystems, and signal generators all demand first-order filters [6]. Some literature can find a dependable method for adjusting the phase of an input signal without disrupting the amplitude against frequency in communications. The applications of controllers are in industrial automation and process control, aerospace and automotive systems, power systems, and renewable energy [7]. PID controllers consist of three terms: The proportional term enhances the device's response time, the integral term improves steady-state error, and the derivative term increases the device's stability. A PD controller can improve the device's timing response. It allows the device to respond quickly while maintaining its steady-state error. A PI controller works effectively when process trends are fundamentally first-order. It can only enhance the device's steady-state response.

This chapter provides an in-depth study of two new circuit designs that use the Differential Difference Current Conveyor (DDCC) and its advanced variant, the Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA). First, a novel voltage-mode first-order universal filter (FOUF) is shown, which uses a single DDCC, one resistor, and one capacitor to accomplish multiple-input, single-output (MISO) capabilities with low-pass, high-pass, and all-pass responses. Second, a novel Trans-admittance Mode (TAM) controller design is proposed, incorporating Proportional-Derivative (PD), Proportional-Integral (PI), and Proportional-Integral-Derivative (PID) control mechanisms via a DDCCTA with grounded capacitors and electronic tuning for control parameters. TAM functionality, the ability to operate PD, PI, and PID controllers simultaneously, and the analysis of non-idealities in DDCCTA performance are all key aspects. The study also investigates how the controller impacts the step response and gain-frequency characteristics with a closed-loop second-order filter system, demonstrating improved performance and practical application.

3.2 Literature review

A literature survey of filters is performed based on a few parameters such as mode of operation, grounded and floated passive components and their count, input/output impedance, total harmonic distortion (THD) [16, 17, 21, 23-26, 28-30], noise [16, 24, 25], power dissipation [16, 17, 23-26, 29, 30], and supply voltages. It is crucial, as it has been reported in [12-30] to use single analog building blocks (ABB) with a minimal number of passive components. Since the input/output impedances are so high [12-16, 20, 21, 27], the industry has recently focused on AABs with cascadable capabilities [15-22, 24-27, 30]. Multiple floating passive components have been employed in the literature [18-20, 23-27, 29]. All first-order filter responses i.e. low pass (LP), high pass (HP) and all-pass (AP) responses have been covered in [12, 13, 15, 17, 18, 23, 24, 27, 28, 30], and APF is frequently utilized as oscillators as reported in [12, 17, 20, 25-27]. A literature review where we have observed the following points: (i) The structures reported in [1,5,9,12-15,18,19] fall under the category of CM, whereas those reported in [2,7,17] belong to VM and TIM/TAM is reported in [14, 15, 17, 19, 21, 22, 27]. (ii) few literatures reported first-order filter topologies using single blocks such as DX MOCCII [12], DVCC [13, 17], CCIII [14, 22], FDCCII [15], MO DXCCTA [16], VDCC [18], CCCCDTA [20], DBTA [21], and some reported multiple blocks such as ICCII [23], CCII [24], DO CF [25], CDTA [26], OFCC [27], OTRA [28], and BJT [29, 30]. A first-order voltage-mode universal filter based on DDCC is proposed to cater above-mentioned limitations. The silent features of the proposed FOUF: (i) Employment of only one AAB. (ii) Used a minimal number of passive components. (iii) Low active or passive sensitivities. (iv) Used for low power and low voltage designs. (v) Used for high pole frequency (in MHz).

In the literature on controllers, a comparison of active block-based controllers such as CCII [31], DO-CCII [32], MO-CCCCTA [33], CCCDBA [34], CFOA [35, 39, 42], FDCCII [37], OTRA [38], DVCCTA [40], VDCC [41], CFTA [43], VCII [44, 46] and CCTA [45]. The PD, PI, and PID parameters can be selected dependently or independently in [31, 34, 37, 38, 40]. The CM-based controllers reported in [31, 32,

34, 36, 42, 46] and VM-based controllers reported in [31, 33, 35, 45], while the mixed mode is given in [36] including TIM and TAM topologies. With the above facts and features of the current mode block in literature, a controller using the DDCCTA block is investigated. This is the first proposal to use DDCCTA to develop a TAM-based PD, PI, and PID controller in one topology. The main highlights of the proposed design: (i) Using only one analog building block. (ii) Grounded capacitors are used. (iii) The PD, PI, and PID controller outputs are achieved in a single proposed topology. (iv) It can be electronically tuned and the output impedance is high.

3.3 Proposed designs using Single ABB

This section includes two proposed structures: The proposed filter circuit comprises of a single DDCC block, a single resistor, and a capacitor. The proposed controller comprises one DDCCTA active block, three resistors, and three grounded capacitors.

3.3.1 Proposed MISO-type VM-based first-order universal filter using DDCC Block

The proposed circuit, shown in Fig. 3.1, consists of a single DDCC block with a single resistor and capacitor. Table 3.1 shows the working principle of MISO-type filter responses. The output voltage obtained from the proposed circuit assuming the ideal DDCC is:

$$V_O = \frac{sRCV_{in2} - V_{in1}}{sRC+1} \tag{3.1}$$

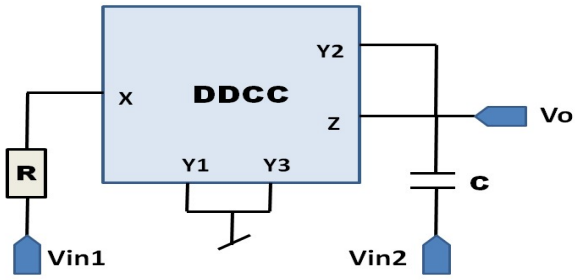


Fig. 3.1: Proposed circuit of the FOUF

Table 3.1: Working principle of MISO type first-order universal filter

Vin1	Vin2	Vo
Vin	0	LPF
0	Vin	HPF
Vin	Vin	APF

From the proposed circuit, various transfer functions are observed as follows:

$$\frac{V_O}{V_{in1}} = -\frac{\left(\frac{1}{RC}\right)}{s+\left(\frac{1}{RC}\right)} \quad \text{For LPF} \tag{3.2}$$

$$\frac{V_O}{V_{in2}} = \frac{s}{s+\left(\frac{1}{RC}\right)} \quad \text{For HPF} \tag{3.3}$$

$$\frac{V_O}{V_{in}} = \frac{s-\left(\frac{1}{RC}\right)}{s+\left(\frac{1}{RC}\right)} \quad \text{For APF} \tag{3.4}$$

$$\omega = \frac{1}{RC}, f = \frac{1}{2\pi RC} \tag{3.5}$$

Phase for APF = $\pi - 2\,tan^{-1}(\omega RC)$ (3.6)

3.3.1.1 Sensitivity Analysis

The first-order filter transfer function may alter as the component's value changes. The sensitivity results show how output responses vary depending on which circuit components are employed. The sensitivities of the proposed filter's output concerning various circuit components have been mathematically computed of APF to R, C.

$$S_R^\omega = S_C^\omega = -1 \tag{3.7}$$

3.3.1.2 Non-idealities Analysis

In consideration of the non-ideal values of DDCC, the characteristic matrix can be rewritten as:

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 \\ 0 & 0 & 0 & \pm\alpha \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (3.8)$$

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} - \beta_3 V_{Y3} \quad (3.9)$$

$$I_Z = \pm \alpha I_X \quad (3.10)$$

Where β_1, β_2 and β_3 are non-ideal voltage-transfer gains from Y1, Y2 and Y3 terminals to X terminal. The non-ideal current transfer gain from X to Z-terminal is ±α. Considering non-idealities, equations are modified as follows:

$$\frac{V_O}{V_{in1}} = \frac{-\left(\frac{\alpha}{RC}\right)}{s+\left(\frac{\beta_2\alpha}{RC}\right)} \quad \text{For LPF} \quad (3.11)$$

$$\frac{V_O}{V_{in2}} = \frac{s}{s+\left(\frac{\beta_2\alpha}{RC}\right)} \quad \text{For HPF} \quad (3.12)$$

$$\frac{V_O}{V_{in}} = \frac{s-\left(\frac{\alpha}{RC}\right)}{s+\left(\frac{\beta_2\alpha}{RC}\right)} \quad \text{For APF } (V_{in1} = V_{in2} = V_{in}) \quad (3.13)$$

$$\omega = \frac{\beta_2\alpha}{RC}, f = \frac{\beta_2\alpha}{2\pi RC} \quad (3.14)$$

$$\text{Phase for APF} = \pi - tan^{-1}\left(\frac{\omega RC}{\beta_2\alpha}\right) - tan^{-1}\left(\frac{\omega RC}{\alpha}\right) \quad (3.15)$$

3.3.1.3 Sensitivity for Non-ideal conditions

The sensitivities of the non-ideal condition of proposed filter outputs to circuit components and non-idealities have been mathematically obtained. The sensitivity of APF to R, C, β_2, α.

$$S_R^\omega = S_C^\omega = -\frac{1}{2} \; ; \; S_\alpha^\omega = S_{\beta_2}^\omega = \frac{1}{2} \quad (3.16)$$

3.3.1.4 Parasitic effects

The parasitic effects of DDCC are characterized by:

- R_X is parasitic resistance that occurs at the X-terminal.

- R_{Y1} // C_{Y1}, R_{Y2} // C_{Y2} and R_{Y3} // C_{Y3} are parasitic impedances at Y_1, Y_2 and Y_3-terminals respectively.
- R_Z // C_Z is parasitic impedance at Z-terminal.

The passive component values including non-ideal parasitic resistances and impedances can be modified as:

$$\frac{V_O}{V_{in1}} = \frac{-\left(\frac{1+sR_ZC+sR_ZC_Z}{C(1+R_ZC_Z)(R+R_X)}\right)}{s+\left(\frac{1+sR_ZC+sR_ZC_Z}{C(1+R_ZC_Z)(R+R_X)}\right)} \quad \text{For LPF} \tag{3.17}$$

$$\frac{V_O}{V_{in2}} = \frac{s}{s+\left(\frac{1+sR_ZC+sR_ZC_Z}{C(1+R_ZC_Z)(R+R_X)}\right)} \quad \text{For HPF} \tag{3.18}$$

$$\frac{V_O}{V_{in}} = \frac{s-\left(\frac{1+sR_ZC+sR_ZC_Z}{C(1+R_ZC_Z)(R+R_X)}\right)}{s+\left(\frac{1+sR_ZC+sR_ZC_Z}{C(1+R_ZC_Z)(R+R_X)}\right)} \quad \text{For APF} \quad V_{in1} = V_{in2} = V_{in} \tag{3.19}$$

$$Z' = \left(\frac{(1+R_ZC_Z)(R+R_X)}{1+sR_ZC+sR_ZC_Z}\right) \tag{3.20}$$

$$\frac{V_O}{V_{in}} = \frac{s-\left(\frac{1}{CZ'}\right)}{s+\left(\frac{1}{CZ'}\right)} \tag{3.21}$$

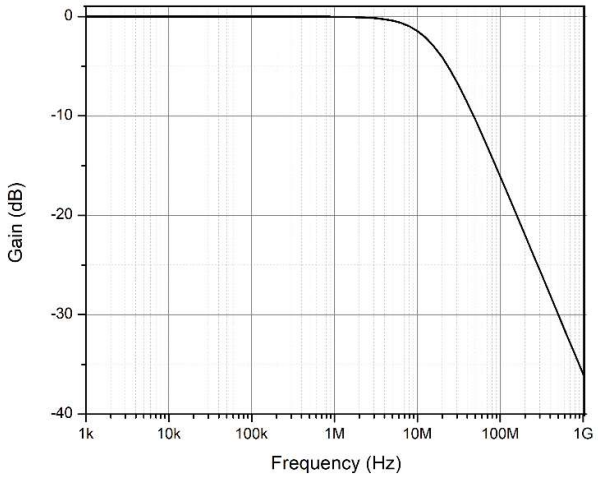
$$\omega = \frac{1}{CZ'} = \frac{(1+sR_ZC+sR_ZC_Z)}{C(1+R_ZC_Z)(R+R_X)} \tag{3.22}$$

$$\text{Phase for APF } = \pi - 2\,tan^{-1}\left(\frac{\omega C(1+R_ZC_Z)(R+R_X)}{(1+sR_ZC+sR_ZC_Z)}\right) = \pi - 2\,tan^{-1}(\omega CZ') \tag{3.23}$$

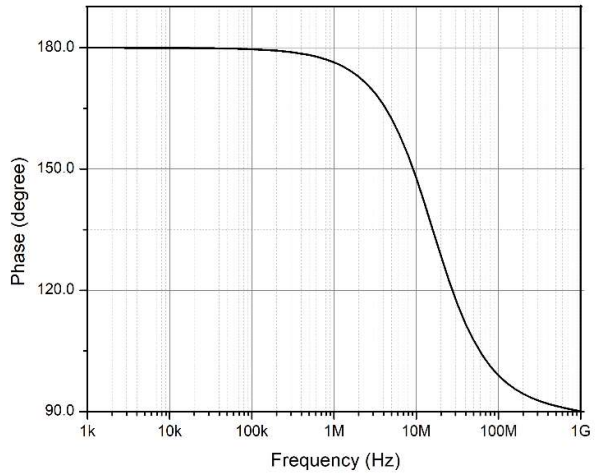
3.3.1.5 Simulation results

The proposed FOUF filter is tested using PSPICE simulations obtained by 180 nm TSMC CMOS technology parameters. The supply voltages $V_{DD} = V_{SS} = \pm$ 0.9 V and a bias voltages V_b = - 0.31 V are used. In the proposed universal filter design input voltage is 3 mV applied, R=1 kΩ, C = 10 pF, angular frequency (ω) is 100 MHz and the pole frequency (fc) is 15.9 MHz. The simulations of the low-pass gain and phase plot with $V_{in1} = V_{in}$ and $V_{in2} = 0$ are shown in Fig. 3.2(a) and Fig. 3.2(b) respectively, where the gain bandwidth of 15.85 MHz at -3dB, the phase of 134.82º are obtained through simulations and the theoretical value of phase is 135º. The high-pass gain and phase plot are simulated in Fig. 3.3(a) and Fig. 3.3(b) respectively, with $V_{in1} = 0$ and $V_{in2} = V_{in}$, where the gain bandwidth of 16 MHz at -3dB, the phase of 44º is obtained

through simulations and theoretical value of phase is 45º. The all-pass gain and phase plot are simulated in Fig. 3.4(a) and Fig. 3.4(b) respectively, with $V_{in1} = V_{in2} = V_{in}$, where the gain bandwidth of 15.85 MHz at 0dB, the phase of 89.21º is obtained through simulations and the theoretical value of phase is 90º. The phase shifter for the all-pass filter response was configured for a 90-phase shift in Fig. 3.4(b) is 15.9 MHz observed.



(a)

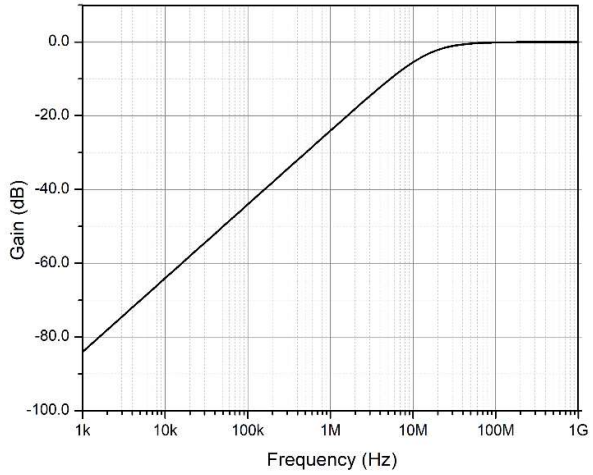


(b)

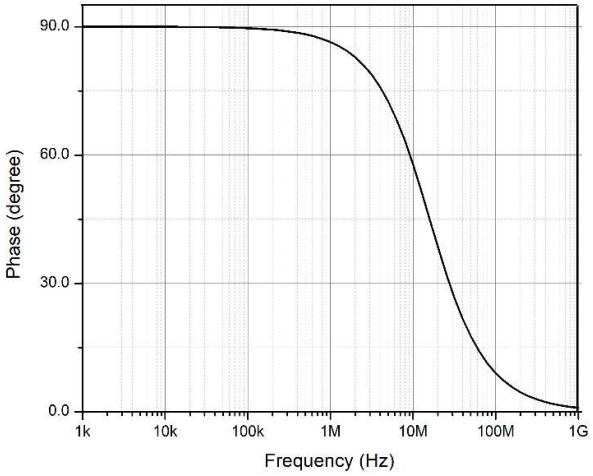
Fig. 3.2: (a) Magnitude (b) Phase vs frequency plot of low-pass filter

Fig. 3.5 shows the output noise is 4.937nV/√Hz. Fig. 3.6 shows the transient response of LPF, HPF, and APF at 15.9 MHz when V_{in} is 3 mV. The generated relationship of waveforms within the LPF, HPF and APF circuit has been verified by the Lissajous

patterns shown in Fig. 3.7(a), Fig. 3.7(b), and Fig. 3.7(c) respectively. Fig. 3.8 shows the deviation in all-pass filter response through Monte Carlo simulations corresponds to ± 3% variation in R and C passive component values. We can observe that the mean value of maximum output voltage MAX(V(OUT) is 2.55mV, for 100 samples and 10 divisions. Fig. 3.9 shows the total harmonic distortions (THDs) of output voltage V_o varies about 3-7% when center frequency varies from 1 MHz to 1 GHz.

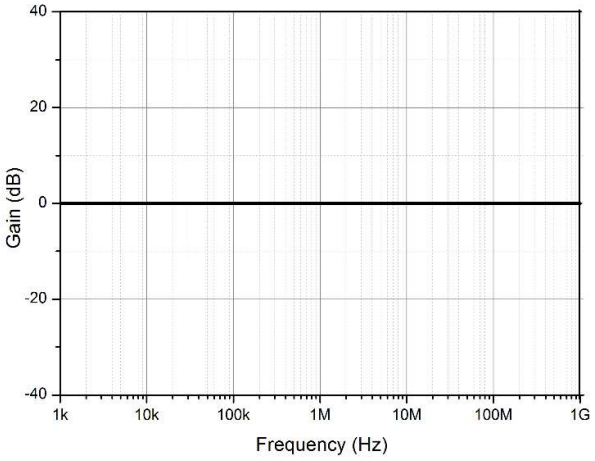


(a)

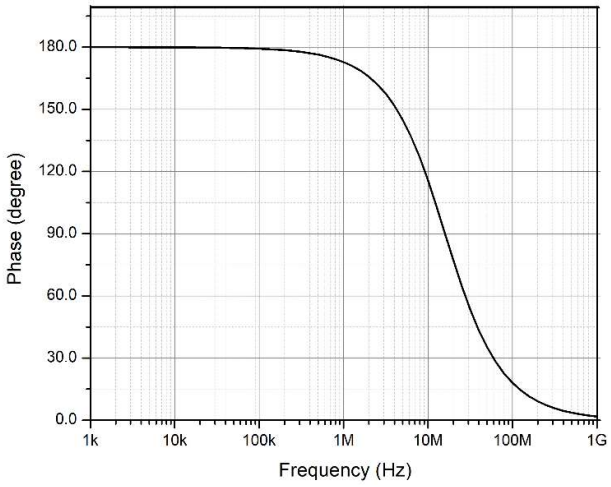


(b)

Fig. 3.3: (a) Magnitude (b) Phase vs frequency plot of high-pass filter



(a)



(b)

Fig. 3.4: (a) Magnitude (b) Phase vs frequency plot of all-pass filter

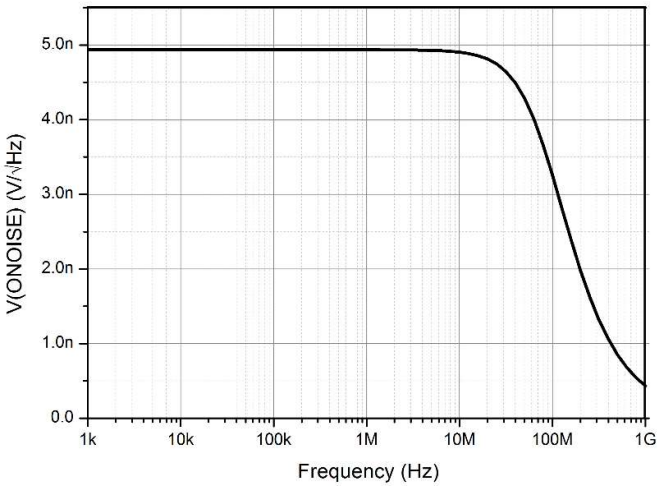


Fig. 3.5: Total output voltage noise

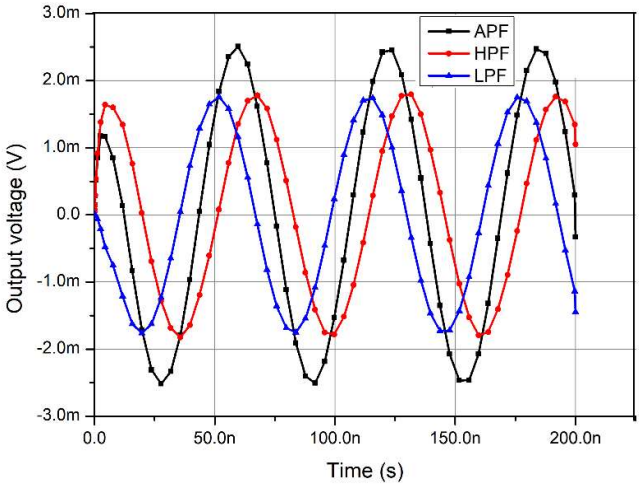
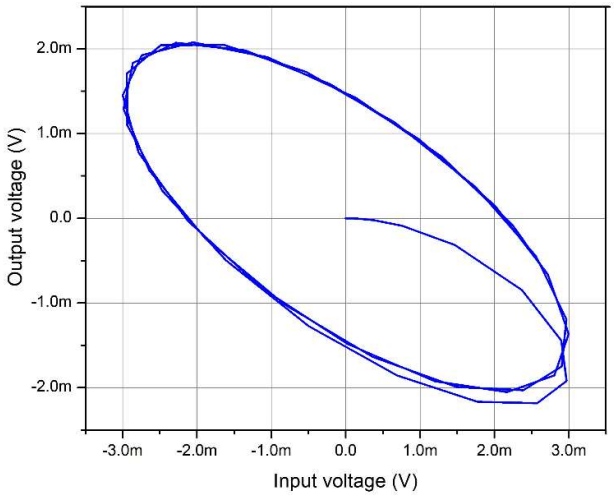
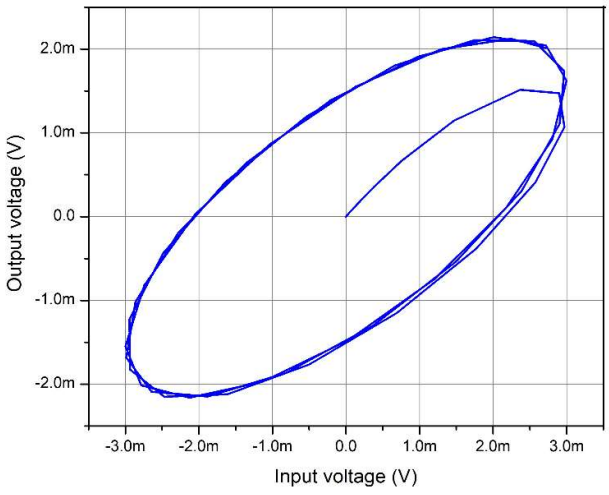


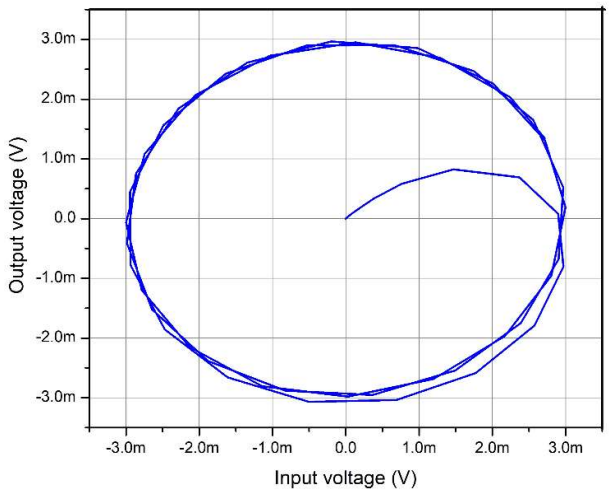
Fig. 3.6: Transient response of LPF, HPF, and APF



(a)

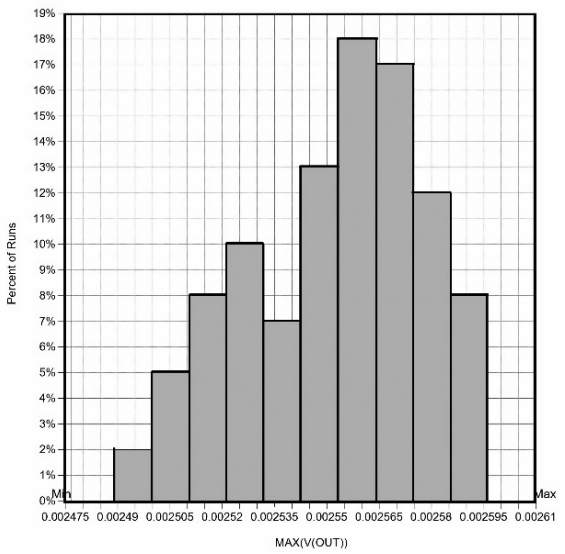


(b)



(c)

Fig. 3.7: Lissajous patterns of (a) LPF (b) HPF (c) APF



n sample	**100**	**min**	**2.4768m**	**mean**	**2.5523m**
n divisions	**10**	**max**	**2.6091m**	**std dev**	**25.1998u**
				median	**2.5560m**

Fig. 3.8: Monte Carlo analysis of max output voltage of APF based on 3% tolerance in R and C components with Vin = 3mV

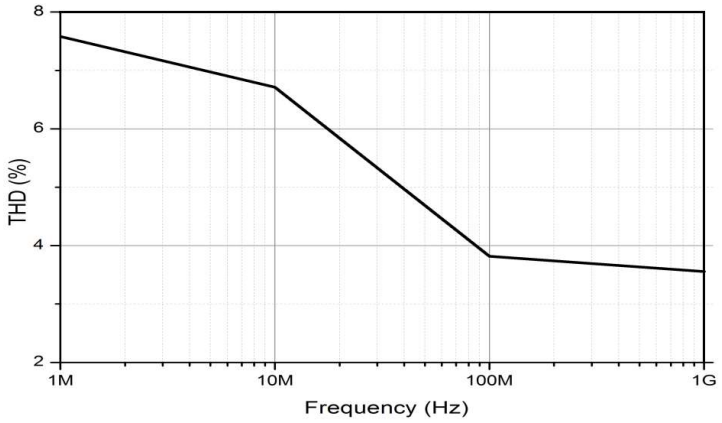


Fig. 3.9: THD against Frequency of APF

3.3.2 Proposed TAM-based PD, PI and PID Controllers using DDCCTA Block

The proposed controller is presented in Fig. 3.10, designed by one DDCCTA active block, three resistors R_1, R_2 and R_3, and three grounded capacitors C_1, C_2 and C_3. The voltage input V_{in} applied through Y_1-terminal and I_{PD}, I_{PI} and I_{PID} are current outputs available through O_1, O_2 and O_3-terminals, which provide high impedance at the input as well at the output terminals, resulting in the cascadable property. Electronically controllable bias currents I_{B1}, I_{B2}, and I_{B3} are available, which give trans-conductance values g_{m1}, g_{m2} and g_{m3} respectively. The common trans-conductance is the g_m for all OTAs.

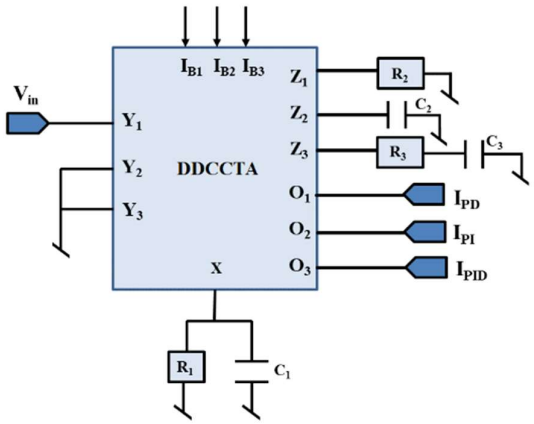


Fig. 3.10: Proposed TAM-based PD, PI, PID controller using DDCCTA

3.3.2.1 PD controller

A proportional-derivative controller has two components: proportional and derivative. It has the potential to improve transient response and is better suited for systems with extremely slow response times. As illustrated in Fig. 3.10, one DDCCTA, two resistors, and are used in the proposed PD controller. The proposed transfer characteristic of the PD controller can be expressed below:

$$\frac{I_{PD}(s)}{V_{in}(s)} = \mathrm{g}_m \frac{R_2}{R_1}(1 + sR_1C_1) \tag{3.24}$$

$$H_{PD}(s) = K_p + sK_d = K_p(1 + sT_d) \tag{3.25}$$

$$K_p = \mathrm{g}_m \frac{R_2}{R_1},\ K_d = \mathrm{g}_m R_2 C_1,\ \ T_d = R_1 C_1 \tag{3.26}$$

The standard transfer characteristic of PD controller and proportional-derivative gains are shown in Eq. (3-5). Furthermore, the sensitivities of control parameters K_p and K_d to R_1, R_2, C_1 and g_m are presented below.

$$-S_{R_1}^{K_p} = S_{R_2}^{K_p} = S_{\mathrm{g}_m}^{K_p} = 1 \tag{3.27}$$

$$S_{R_2}^{K_d} = S_{C_1}^{K_d} = S_{\mathrm{g}_m}^{K_d} = 1 \tag{3.28}$$

3.3.2.2 PI Controller

A proportional-integral controller has two components: proportional and integral. It can only strengthen the steady-state response of the device, when an integral component is present, the offset of proportional action is removed. As illustrated in Fig. 3.10, one DDCCTA, one resistor, and two capacitors are used in the proposed PI controller. The proposed transfer characteristic of the PI controller can be expressed as below:

$$\frac{I_{PI}(s)}{V_{in}(s)} = \mathrm{g}_m \frac{C_1}{C_2}\left(1 + \frac{1}{sR_1C_1}\right) \tag{3.29}$$

$$H_{PI}(s) = K_p + \frac{K_i}{s} = K_p\left(1 + \frac{1}{sT_i}\right) \tag{3.30}$$

$$K_p = \mathrm{g}_m\frac{C_1}{C_2}\ ,\ \ K_i = \frac{\mathrm{g}_m}{R_1C_2}\ ,\ T_i = R_1C_1 \tag{3.31}$$

The standard transfer characteristic of PI controller and proportional-integral gains. Furthermore, the sensitivities of control parameters K_p and K_i to R_1, C_1, C_2, and g_m are presented below.

$$S_{C_1}^{K_p} = -S_{C_2}^{K_p} = S_{\mathrm{g}_m}^{K_p} = 1 \tag{3.32}$$

$$-S_{R_1}^{K_i} = -S_{C_2}^{K_i} = S_{\mathrm{g}_m}^{K_i} = 1 \tag{3.33}$$

3.3.2.3 PID Controller

A PID controller has all three terms, the proportional term increases device speed, the integral term tries to lower the steady-state error, and the derivative term increases device stability. As illustrated in Fig. 3.10, one DDCCTA, two resistors, and two capacitors are used in the proposed PID controller. The proposed transfer characteristic of the PID controller can be expressed as:

$$\frac{I_{PID}(s)}{V_{in}(s)} = \mathrm{g}_m\left(\frac{R_3}{R_1} + \frac{C_1}{C_3}\right).\left[1 + \frac{1}{s(R_1C_3+R_3C_1)} + s\frac{R_1R_3C_1C_3}{(R_1C_3+R_3C_1)}\right] \tag{3.34}$$

$$H_{PID}(s) = K_p + \frac{K_i}{S} + sK_d = K_p\left(1 + \frac{1}{sT_i} + sT_d\right) \tag{3.35}$$

$$K_p = \mathrm{g}_m\left(\frac{R_3}{R_1} + \frac{C_1}{C_3}\right), K_i = \frac{\mathrm{g}_m}{R_1C_3}, K_d = \mathrm{g}_mR_3C_1, T_i = (R_1C_3 + R_3C_1), T_d = \frac{R_1R_3C_1C_3}{(R_1C_3+R_3C_1)} \tag{3.36}$$

The standard transfer characteristic of the PID controller and proportional-integral-derivative gains are shown above. Furthermore, the sensitivities of control parameters K_p, K_i and K_d to R_1, R_3, C_1, C_3 and g_m are presented below.

$$S_{R_1}^{K_p} = -S_{R_3}^{K_p} = \frac{1}{\mathrm{g}_m}\left(\frac{R_3C_3}{R_1C_1+R_3C_3}\right), S_{C_1}^{K_p} = -S_{C_3}^{K_p} = \frac{1}{\mathrm{g}_m}\left(\frac{R_1C_1}{R_1C_1+R_3C_3}\right),\ \ S_{\mathrm{g}_m}^{K_p} = 1 \tag{3.37}$$

$$-S_{R_1}^{K_i} = -S_{C_3}^{K_i} = S_{\mathrm{g}_m}^{K_i} = 1 \tag{3.38}$$

$$S_{R_3}^{K_d} = S_{C_1}^{K_d} = S_{g_m}^{K_d} = 1 \tag{3.39}$$

The controller transfer characteristic may change as the value of the component changes. The sensitivity result demonstrates how output responses differ by available the circuit components used. The sensitivities of the proposed controller output to various circuit components have been calculated mathematically and observed that a low value was achieved.

3.3.2.4 Non-ideal effects

The non-ideal effect on DDCCTA is re-characterized by the matrix below.

$$\begin{bmatrix} I_{Y1,2,3} \\ V_X \\ I_{Z1} \\ I_{Z2} \\ I_{Z3} \\ I_{O1} \\ I_{O2} \\ I_{O3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \gamma_1 g_{m1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \gamma_2 g_{m2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \gamma_3 g_{m3} \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1} \\ V_{Z2} \\ V_{Z3} \end{bmatrix} \tag{3.40}$$

Where β_1, β_2 *and* β_3 are non-ideal voltage gains from Y_1, Y_2 *and* Y_3 terminals to the X terminal. The non-ideal current gain from X to Z_n terminal is α_n for *n=1, 2, 3*. The γ_n is the non-ideal trans-admittance-gain from voltage Z_n to current O_n terminal for *n=1, 2, 3*. Considering the non-idealities of proposed controllers as follows:

For PD controller

$$\frac{I_{PD}(s)}{V_{in}(s)} = \alpha_1\beta_1\gamma_1 g_m \frac{R_2}{R_1}(1 + sR_1C_1) \tag{3.41}$$

$$K_p = \alpha_1\beta_1\gamma_1 g_m \frac{R_2}{R_1}\ ,\ T_d = \alpha_1\beta_1\gamma_1 g_m R_1C_1 \tag{3.42}$$

$$S_{\alpha_1}^{K_p} = S_{\beta_1}^{K_p} = S_{\gamma_1}^{K_p} = 1 \tag{3.43}$$

For PI controller

$$\frac{I_{PI}(s)}{V_{in}(s)} = \alpha_2\beta_1\gamma_2 g_m \frac{C_1}{C_2}\left(1 + \frac{1}{sR_1C_1}\right) \tag{3.44}$$

$$K_p = \alpha_2\beta_1\gamma_2 g_m \frac{C_1}{C_2}\ ,\ T_i = \alpha_2\beta_1\gamma_2 R_1 C_1 \tag{3.45}$$

$$S_{\alpha_1}^{K_p} = S_{\beta_1}^{K_p} = S_{\gamma_1}^{K_p} = 1 \tag{3.46}$$

For PID controller

$$\frac{I_{PID}(s)}{V_{in}(s)} = \alpha_3\beta_1\gamma_3 g_m \left(\frac{R_3}{R_1} + \frac{C_1}{C_3}\right).\ \left[1 + \frac{1}{s(R_1C_3+R_3C_1)} + s\frac{R_1R_3C_1C_3}{(R_1C_3+R_3C_1)}\right] \tag{3.47}$$

$$K_p = \alpha_3\beta_1\gamma_3 g_m \left(\frac{R_3}{R_1} + \frac{C_1}{C_3}\right), T_i = \alpha_3\beta_1\gamma_3(R_1C_3 + R_3C_1)\ ,\ T_d = \alpha_3\beta_1\gamma_3 g_m \frac{R_1R_3C_1C_3}{(R_1C_3+R_3C_1)} \tag{3.48}$$

$$S_{\alpha_3}^{K_p} = S_{\beta_1}^{K_p} = S_{\gamma_3}^{K_p} = 1 \tag{3.49}$$

The mathematical sensitivities of proposed controller outputs to used circuit components of non-ideality conditions have been obtained. The sensitivity of controller K_p to α, β and γ is shown above.

3.3.2.5 Simulation results

Simulations are conducted using the Virtuoso simulator with 180 nm gpdk CMOS technology to validate the results. The circuit operates with supply voltages of V_{DD} = V_{SS} = ±0.9 V, a bias voltage of V_B = -0.62 V, and a bias current of I_B = 100 µA. The total power dissipation is measured at 4 mW. In Fig. 3.11, the variation of g_m is shown for a fixed voltage of V_Z. For a bias current range of 0 to 100µA, the transconductance varies up to 1.21 mS. The voltage input is 50 mV and the corresponding transient responses of PD, PI, and PID controller are simultaneously shown in Fig. 3.12. The parameter values R_1 = 10 kΩ, R_2 = 5 kΩ, R_3 = 2.5 kΩ, C_1 = 2 pF, C_2 = 4 pF and C_3 = 8 pF. The K_p = 0.6 mA/V, T_i = 85 ns, and T_d = 4.7 ns have been determined as PID controllers. For K_p = 0.6 mA/V in PD and PI controller, T_d = 20 ns, and T_i = 20 ns have been determined respectively.

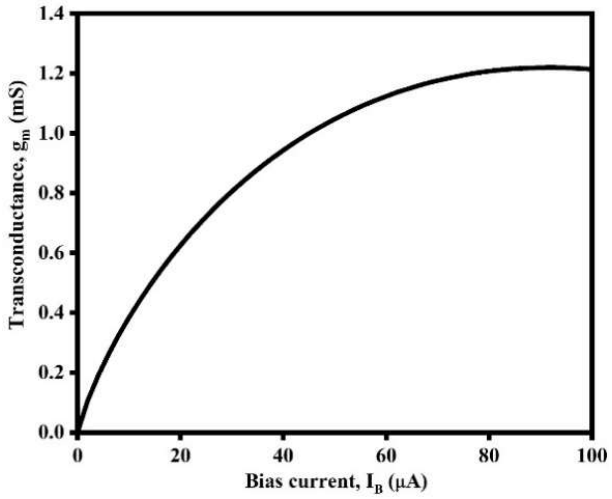
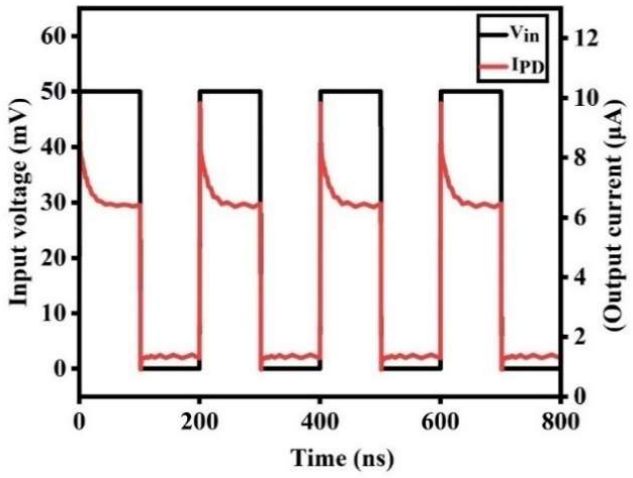
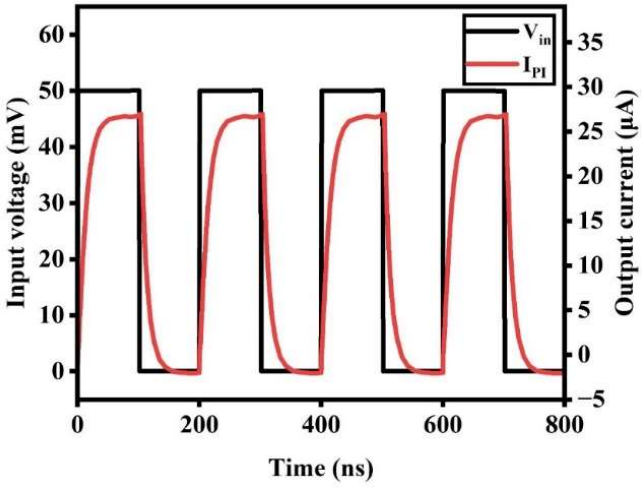


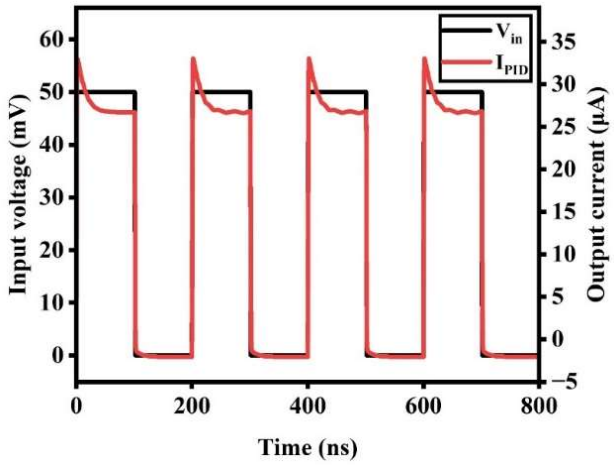
Fig. 3.11: Tunning of trans-conductance by current bias



(a)

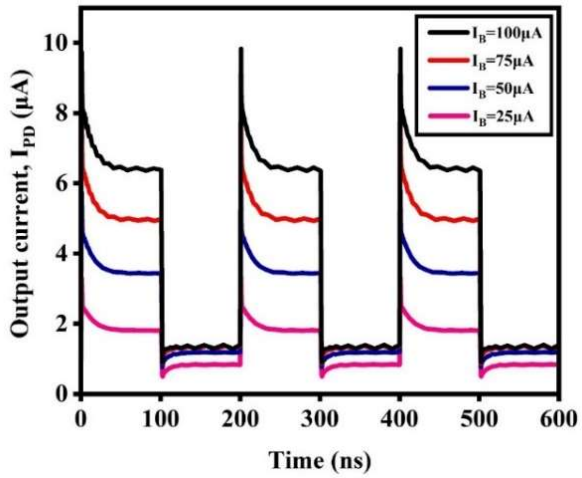


(b)

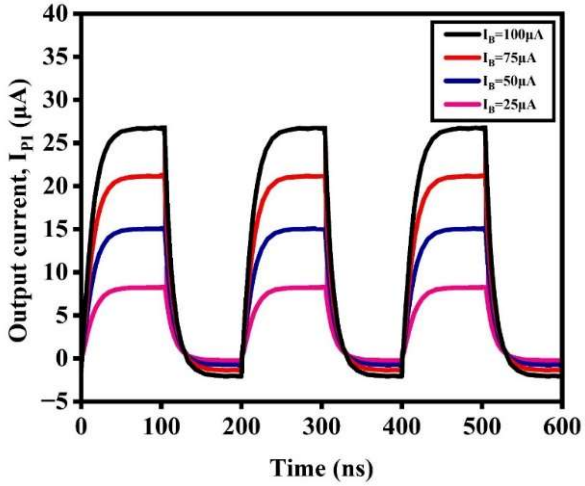


(c)

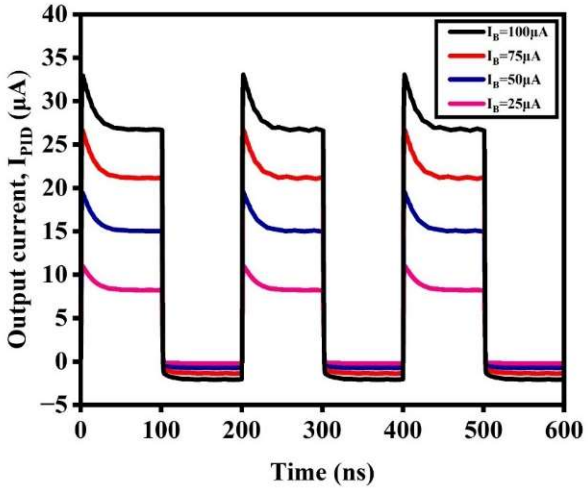
Fig. 3.12: Transient response of the proposed controllers (a) PD (b) PI (c) PID



(a)



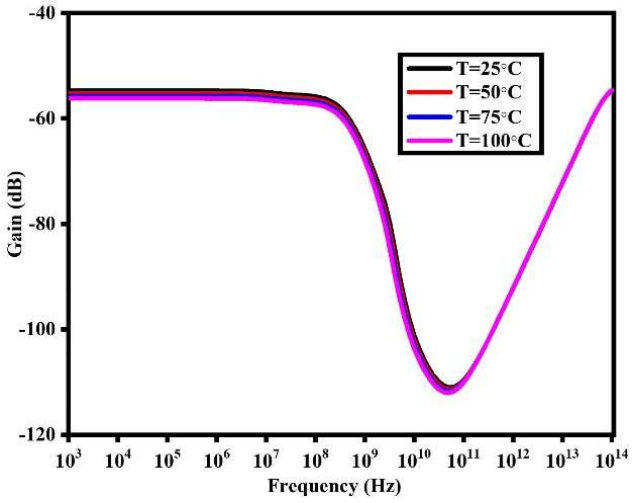
(b)



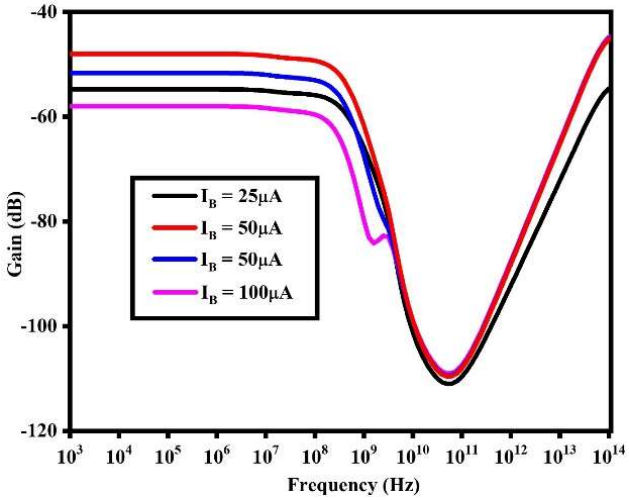
(c)

Fig. 3.13: Transient responses of (a) PD (b) PI (c) PID controller with the tuning of I_B

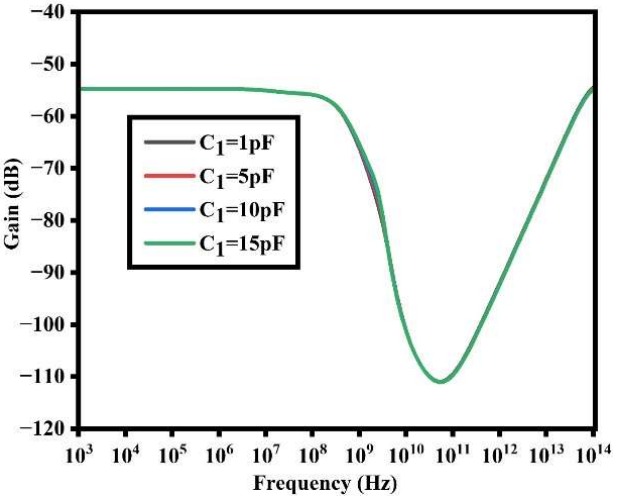
The simulation results of the proposed controller without a closed-loop control system are shown in Fig. 3.13, where $I_{B1} = I_{B2} = I_{B3} = I_B$ vary from 25 µA to 100 µA, with an input signal of 50 mV rectangular waveform. The K_p of the PD controller can be tuned, as shown in Fig. 3.13(a). The derivative conditions vary with I_{B1}, proving that the derivative conditions can be electronically or independently tuned by I_{B1}. The K_p of the PI controller can be tuned, as shown in Fig. 3.13(b). The integral conditions vary with I_{B2}, proving that the integral conditions can be electronically/ independently tuned by I_{B2}. The K_p of the PID controller can be tuned, as shown in Fig. 3.13(c). The derivative and integral conditions vary with I_{B3}, it can be electronically/independently tuned by I_{B3}. The temperature analysis ranges from 25 °C to 100 °C is done using same passive component values as earlier. The gain response of a PID controller varies with temperature, as shown in Fig. 3.14(a). The tuning of bias current I_B in gain response is shown in Fig. 3.14(b), where I_B varies from 25µA to 100µA. The PID controller output response should not be altered as a result of the different values of the passive components. To verify this, the C_1 varies from 1 pF to 15 pF and the respective gain response is shown in Fig. 3.14(c), while the integral part shows some variation for a few values of R_1 as presented in Fig. 3.14(d). When a value of components reaches its minimum and maximum range, the output oscillates.


-40
-60
-80
-100
-120
Gain (dB)
T=25°C
T=50°C
T=75°C
T=100°C
10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10} 10^{11} 10^{12} 10^{13} 10^{14}
Frequency (Hz)

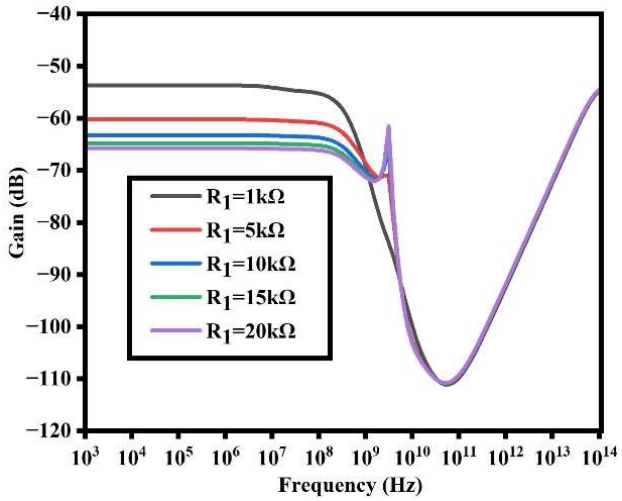
(a)


-40
-60
-80
-100
-120
Gain (dB)
I_B = 25μA
I_B = 50μA
I_B = 50μA
I_B = 100μA
10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10} 10^{11} 10^{12} 10^{13} 10^{14}
Frequency (Hz)

(b)

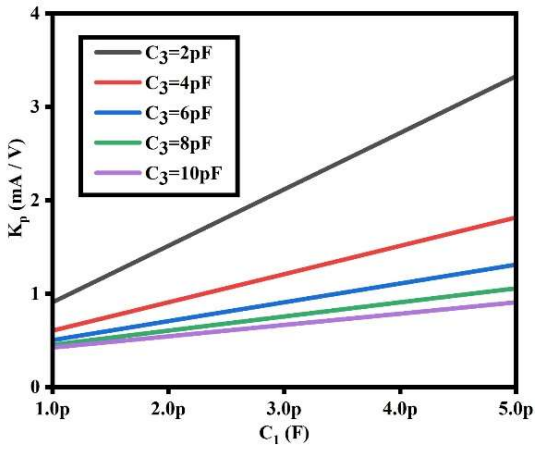

−40
−50
−60
−70
−80
−90
−100
−110
−120
Gain (dB)
C_1=1pF
C_1=5pF
C_1=10pF
C_1=15pF
10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10} 10^{11} 10^{12} 10^{13} 10^{14}
Frequency (Hz)

(c)

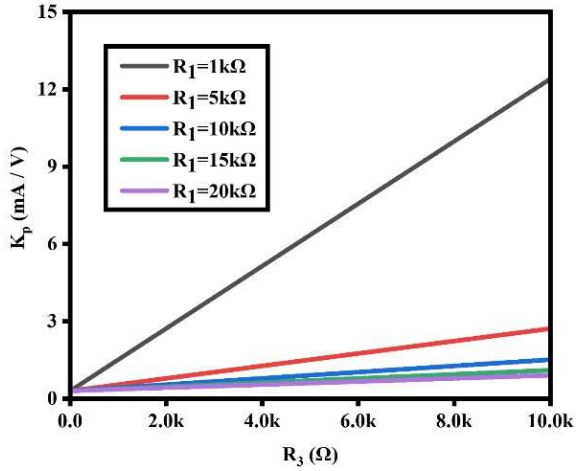


(d)

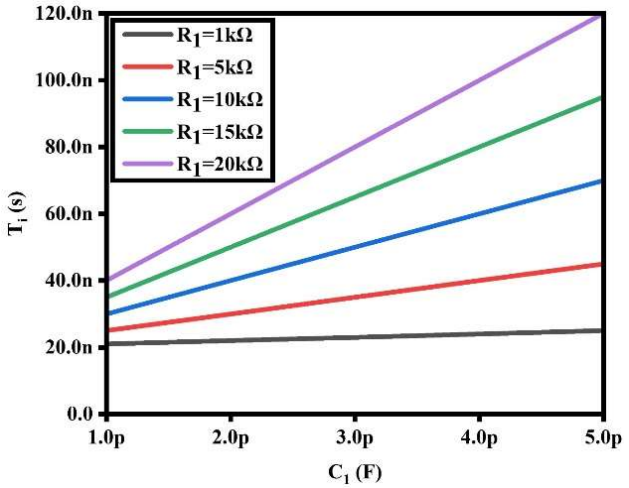
Fig. 3.14: Gain response of PID controller with (a) different temperatures (b) tunning of I_B (c) different values of C_1 (d) different values of R_1



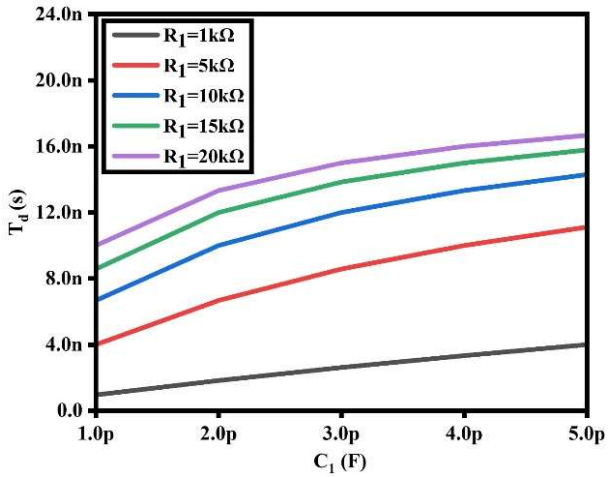
(a)



(b)



(c)



(d)

Fig. 3.15: Gain to passive components control parameter response of PID (a) K_p to C_1 (b) K_p to R_3 (c) T_i to C_1 (d) T_d to C_1

Fig. 3.15 depicts the variations in the controller parameters such as proportionaI gain, derivative time, and integral time to passive components (K_p, T_d, and T_i to R_1, R_3, C_1 and C_3). Fig. 3.15(a) shows the TAM K_p to C_1 for different values of C_3, where K_p vary from 0.6 mA/V to 3.5 mA/V. Fig. 3.15(b) shows the K_p to R_3 for different values of R_1, where K_p vary the K_p to R_3 for different values of R_1, where K_p vary from 0.6 mA/V to 12 mA/V. Fig. 3.15(c) shows the T_i to C_1 for different values of R_1, where T_i varies from 20 ns to 120 ns. Fig. 3.15(d) shows the T_d to C_1 for different values of R_1 where T_d varies from 4 ns to 16 ns.

3.3.2.6 Example as application

The closed-loop system depicted in Fig. 3.16 includes the proposed PID controller operating in TAM, paired with a trans-impedance mode (TIM) low-pass filter (LPF) serving as the plant. This setup demonstrates the practical applications of the TAM mode PID controller. Table 3.2 provides an evaluation of the second-order filter's performance, detailing different metrics.

Table 3.2: Comparison of performance of the second-order filter

Parameters	Without PID controller	With PID controller
Overshoot	10%	2%
Peak output	55 mV	51 mV
Rise time	10.07 ns	5.20 ns
Settling time	49 ns	18 ns

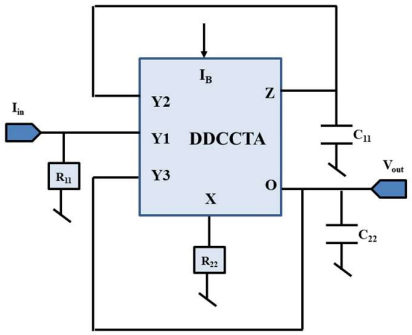
Transfer functions of trans-admittance mode PID controller and trans-impedance mode low pass filter are:

$$H_{PID}(s) = \frac{I_{PID}(s)}{V_{in}(s)} = g_m\left(\frac{R_3}{R_1} + \frac{C_1}{C_3}\right)\left[1 + \frac{1}{s(R_1C_3+R_3C_1)} + s\frac{R_1R_3C_1C_3}{(R_1C_3+R_3C_1)}\right] \quad (3.40)$$

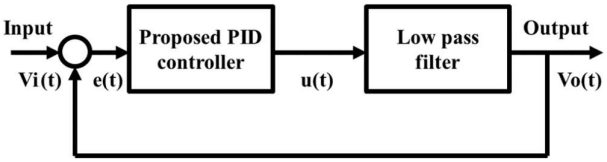
$$H_{LPF}(s) = \frac{V_{out}(s)}{I_{in}(s)} \frac{-\frac{g_mR_{11}}{C_{11}C_{22}R_{22}}}{s^2+s\frac{1}{C_{11}R_{22}}+\frac{g_m}{C_{11}C_{22}R_{22}}} \quad (3.41)$$

The transfer function of the whole close loop system is:

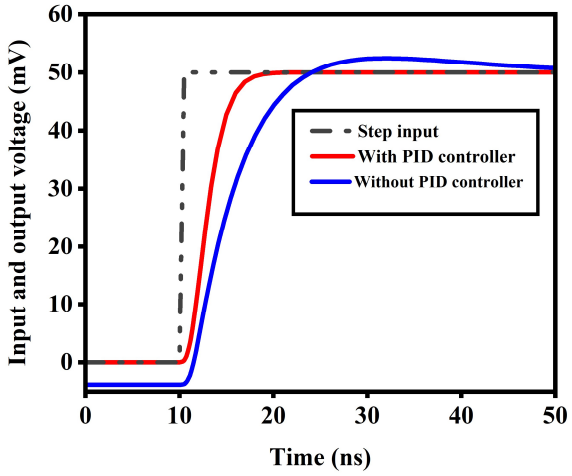
$$H_{CL}(s) = \frac{V_O(s)}{V_i(s)} = \frac{H_{PID}(s)\,H_{LPF}(s)}{1+H_{PID}(s)\,H_{LPF}(s)} \quad (3.42)$$



(a)



(b)



(c)

Fig. 3.16: (a) DDCCTA-based TIM-LPF (b) Closed loop system with proposed TAM-PID controller and TIM-LPF filter (c) Step input and output

This suggests that the study involves creating mathematical models or representations of controllers that are capable of generating high-impedance outputs. High impedance outputs are desirable in certain applications to prevent loading effects and maintain signal integrity. This indicates that the controllers under investigation are based on the TAM architecture. PD, PI, and PID controllers are common types of feedback control systems used in engineering. They consist of proportional, integral, and derivative control actions, respectively, and are widely applied in various control applications. The DDCCTA is in analog signal processing, particularly in control systems and filter design. This indicates that the controllers are intended for use in closed-loop control systems. Closed-loop systems keep feedback, where the output of the system is fed back and matched with a reference input to obtain error signals. The controllers adjust the system inputs based on these error signals to achieve the desired system behavior.

Type of Active Element: The proposed work utilizes a DDCCTA (Differential Difference Current Conveyor Transconductance Amplifier) where others have multiple or more than one block. Number of Passive Elements and Control Actions: The proposed work involves 3 resistors and 3 capacitors and supports PD, PI, and PID control actions simultaneously. Topology/Architecture: The proposed work uses a TAM topology. Existing works use different topologies such as VM, CM, Mixed Mode, and TRM. Performance Metrics: Performance metrics such as power consumption, bandwidth, and tolerance are provided for some of the existing works but not for the proposed work.

3.4 Concluding remarks

A single DDCC-based MISO-type first-order universal filter is presented with a single resistor and single capacitor. This filter offers low pass, high pass and all pass responses from a single topology with higher pole frequency and is suitable for low-power applications. The proposed circuit offers the advantage of higher pole frequency (15.9 MHz), minimum voltage supply (±0.9V), and low power (2.94 mW) dissipation. The theoretical results are well-validated by the SPICE simulations.

A circuit configuration for realizing a TAM controller is presented in this paper. The proposed controllers comprise one DDCCTA and three grounded capacitors with three passive resistors. Because it employs grounded capacitor components, the proposed controller is beneficial for IC implementation. It also has the following features: (1) PD, PI and PID TAM operation without modifying its topology or without matching conditions, (2) electronic parameter (g_{m1}= g_{m2}= g_{m3}= g_m) controllability, and (3) low sensitivity performance. The proportional-integral-derivative gains, derivative time, and integral time constants of the controller can all be adjusted. Virtuoso simulations are used to validate the theoretical analysis.

Chapter 4

VM and CM-based Wave-Active Filters

- S. Kumari and D. Nand, "Realization of *n*th Order Wave Active Low-Pass Filter Using Differential Difference Current Conveyor", *Journal of Circuits, Systems and Computers*, Vol. 33, No. 10, 2450180, (2024). https://doi.org/10.1142/S0218126624501809.
- S. Kumari and D. Nand, "Simplified Wave Active Filter: A Novel design in current mode with single EX-CCCCTA", *Journal of Circuits, Systems and Computers*, Vol. 34, No. 04, 2550091 (2025). https://doi.org/10.1142/S0218126625500914.

4.1 Introduction

Active filters play a pivotal role in signal processing, offering distinct advantages over their passive counterparts. These benefits include tunable gain within pass-band frequencies, compatibility with monolithic integration due to the absence of physical inductors, and adjustable input-output impedance to meet diverse design requirements [4]. While active filters excel in low to medium-frequency applications, their performance may degrade at higher frequencies, where LC ladder-based filters are often preferred. To address this limitation, innovative solutions such as wave-active filters have been developed, exhibiting enhanced sensitivity in very high-frequency ranges. This methodology treats each filter component as a two-port network, deriving its wave-equivalent network and interconnecting these elements to form the wave-active filter [5]. Utilizing scattering matrices, voltage and current parameters are transformed into wave equivalents, enabling high-frequency operation with improved accuracy and stability. Wave-active filters, designed using analog building blocks (ABBs) like DDCC and EXCCCCTA, actively amplify signals while reducing noise and distortion, making them superior to conventional passive filters like LC-ladder filters. These features make wave-active filters particularly advantageous in applications demanding high fidelity and low noise, such as audio and communication systems. The use of analog building blocks in wave-active filter design provides benefits like high precision, minimal distortion, and enhanced noise rejection. Additionally, wave-active filters allow seamless transformations, such as converting a low-pass filter into a high-pass filter using RC-CR transformations, further emphasizing their versatility and practicality [6].

This chapter introduces novel voltage-mode wave active filter (WAF) designs leveraging the Differential Difference Current Conveyor (DDCC) and a current-mode WAF designed with the Extra-X Current Controlled Current Conveyor Transconductance Amplifier (EX-CCCCTA) as an ABBs for efficient wave-based signal processing. The design framework utilizes the wave method to implement basic wave active elements (WAE) of active filters, such as series inductors and shunt

capacitors, through mathematical operations like lossy integration-subtraction, subtraction, summation, and inversion. By employing a CMOS-based DDCC, the proposed approach simplifies the design of low-pass Butterworth filter topologies ranging from lower to higher orders, addressing the challenges typically associated with wave-active filter implementation. This innovative method highlights the versatility of DDCC in achieving high accuracy and stability in analog filter designs. The proposed design minimizes circuit complexity by utilizing a single EX-CCCCTA along with grounded passive components, making it highly suitable for monolithic integration. The inclusion of electronic tuning capabilities further enhances the filter's adaptability, enabling optimal performance across a wide frequency range. This combined approach offers significant advancements in both voltage-mode and current-mode wave active filter topologies, demonstrating their potential for use in current high-performance analog systems.

4.2 Literature review

The low sensitivity is known for inductor-less active filters derived from two network-terminated conventional reactance filtration systems, such as filters based on the FDNR theory and gyrator-capacitor filters [47]. Some methods for getting low-sensitivity RC-active filters are derived from k-ladder filter simulation. One of these approaches is based on the wave-active (WA) approach and incorporates scattering parameters into the generation of waves process [48-50]. The well-known leapfrog approach could be used for developing high-order filters. According to this, an LC ladder prototype is expressed in voltage/current relationships of the passive designs and is used to construct the corresponding Signal Flow Graph (SFG) based on the operational emulation method [51-53]. The wave approach has the following interesting characteristics: The filter structures that result are modular, the availability of a tabular substitution scheme greatly simplifies the design and instead of lossless integrators used in operational emulation or floating capacitors used in topological emulation, only lossy integrators realized using grounded only capacitors are required. The literature review of wave active filters using different ABBs like Current Feedback

Operational Amplifiers (CFOA) [54] in which series inductor and shunt capacitor WAEs are used to design 3rd order LC ladder filters, several ABBs are generated by cascading various current conveyor blocks with transconductance amplifier (TA) blocks in a monolithic device for efficient implementation of signal processing circuits and systems, Differential Voltage Current Conveyor Tans-conductance Amplifier (DVCCTA) [55], Differential Voltage Current Controlled Conveyor Tans-conductance Amplifier (DVCCCTA) [56], Current Controlled Differential Difference Current Conveyor Tans-conductance Amplifier (CCDDCCTA) [57] are an example of such ABBs, Operational Trans-Resistance Amplifier (OTRA) [58] in which series inductor and shunt capacitor WAEs are used to design 3rd order Butterworth filter, Voltage Differential Trans-conductance Amplifier (VDTA) [59,60] in which series inductor and shunt capacitor WAEs are used to design 4th order Butterworth filter, Voltage Differencing Buffered Amplifier (VDBA) [61] in which series inductor and shunt capacitor WAEs are used to design 4th order LC ladder filter, extra X current controlled current conveyor (EX-CCCII) [62] in which series inductor and shunt capacitor WAEs are used to design 3rd order Butterworth filter, Differential Difference Tans-conductance Amplifier (DDTA) [63] in which series/shunt inductor and series/shunt capacitor WAEs are used to design 2nd to 6th order LC ladder filter and Voltage Differencing Differential Input Buffered Amplifier (VDDIBA) [64]. Some important parameters reported in literature like the number of transistors required to form a WAE, higher order of filter i.e., third order [54, 57, 58, 62, 64], fourth order [55, 56, 59-62], and second to sixth order [63]. After a comprehensive literature review, certain limitations are evident in the existing wave active filters as reported in the literature: Use of a floating capacitor [58]. Complex circuit for realization of shunt capacitance and series inductor. except in [52]. Lack of electronic tuning capabilities [54, 58, 62, 64].

This introduces two innovative WAF designs, leveraging advanced ABBs to enhance circuit efficiency and functionality. For the first time, the DDCC is utilized to develop WAEs for implementing nth-order Butterworth filter topologies. Additionally, this work presents a novel wave-active filter employing the EX-CCCCTA. A thorough literature review highlights that EX-CCCCTA-based wave active filters have not been

explored previously, positioning this study as a pioneering effort. The proposed WAF approach stands out due to its minimal use of analog building blocks, employment of grounded resistors and capacitors, and suitability for higher-order filter designs. These features make it a robust solution for efficient and accurate signal processing, grounded passive components for monolithic integration, and series inductor and shunt capacitor wave equivalents. Notable attributes include its ability to operate effectively at very high frequencies and electronic tuning capability for enhanced adaptability. By addressing key challenges in current-mode active filters—such as noise reduction, power efficiency, and resource minimization—this study demonstrates the potential for broader adoption of current-mode technology across various industries.

4.3 Proposed designs VM and CM WAF

This section includes two proposed structures: The proposed VM-based wave active filter circuit comprises of DDCC block. The proposed CM-based wave active filter comprises one EXCCCCCTA active block, a grounded resistor and a capacitor.

4.3.1 Basic Wave Equivalent

Fig. 4.1 shows the two-port network with active wave variables and defines the functionality of such system, incident and reflected waves A_j and B_j, or A_k and B_k, for voltage mode or current mode respectively.

Fig. 4.1: Two-port network with active wave variables

For VM

$$A_j = V_j + I_j R_j \quad (4.1a)$$

$$B_j = V_j - I_j R_j \quad (4.1b)$$

R_j denotes resistance, where j = 1, 2.

For CM

$$A_k = I_k + \frac{V_k}{R_k} \tag{4.2a}$$

$$B_k = I_k - \frac{V_k}{R_k} \tag{4.2b}$$

R_k denotes resistance, where k = 1, 2. Eqs. (4.1 & 4.2) can be stated below in the form of the S-matrix:

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{4.3}$$

In a series inductor L and shunt capacitor C, the scattering parameter (S) is denoted in the following manner:

$$S = \frac{1}{1+s\tau} \begin{bmatrix} s\tau & 1 \\ 1 & s\tau \end{bmatrix} \tag{4.4}$$

$$S = \frac{1}{1+s\tau} \begin{bmatrix} -s\tau & 1 \\ 1 & -s\tau \end{bmatrix} \tag{4.5}$$

Eqs (4.3) and (4.4) can be employed to demonstrate the relationship between the incident wave (A) and the reflected wave (B) for a series inductor.

$$B_1 = A_1 - \frac{1}{1+s\tau_L}(A_1 - A_2) \tag{4.6}$$

$$B_2 = A_2 + \frac{1}{1+s\tau_L}(A_1 - A_2) \tag{4.7}$$

where τ_L the time constant and expressed as

$$\tau_L = \frac{L}{2R} \tag{4.8}$$

At two network ports, L is the required inductance and R is the port resistance. Similarly, Eqs (4.3) and (4.5) can be employed to demonstrate the relationship between the incident wave (A) and the reflected wave (B) for a shunt capacitor.

$$B_1 = -A_1 + \frac{1}{1+s\tau_C}(A_1 - A_2) \tag{4.9}$$

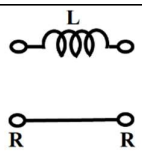
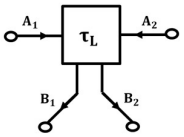
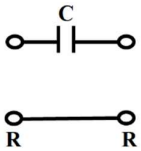
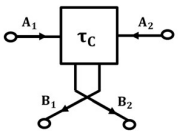
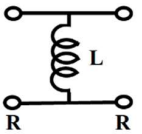
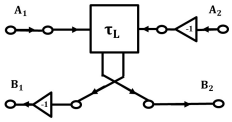
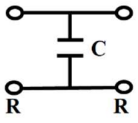
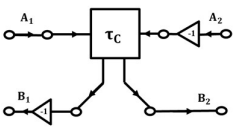
$$B_2 = -A_2 + \frac{1}{1+s\tau_C}(A_1 - A_2) \tag{4.10}$$

where τ_C the time constant and expressed as

$$\tau_C = \frac{RC}{2} \tag{4.11}$$

At two network ports, C is the required capacitance, and R is the port resistance. Table 4.1 shows the relation between the elementary two-port network and wave active elements.

Table 4.1: Wave topologies of series/shunt inductor and capacitor

Type	Elementary two-port network	Wave active element	Value of wave active element	Value of Cd
Series inductor			$L = 2R\tau_L$	$C_{dL} = \frac{L}{2R^2}$
Series capacitor			$C = \frac{\tau_C}{2R}$	$C_{dC} = 2C$
Shunt inductor			$L = \frac{R\tau_L}{2}$	$C_{dL} = \frac{2L}{R^2}$
Shunt capacitor			$C = \frac{2\tau_C}{R}$	$C_{dC} = \frac{C}{2}$

4.3.2 Proposed VM-based Wave Active Filter using DDCC Block

Eqs (4.6), (4.7), (4.9) and (4.10) can be determined using the following operations: (i) Lossy Integration-Subtraction; (ii) Subtraction; (iii) Summation; (iv) Inverter.

4.3.2.1 Lossy Integration-Subtraction operation

Two parallel configurations of resistor and capacitor R_Z and C_d connected on Z-terminals and a resistor R_d connected to the X-terminal in block-1 are used to implement this operation. Each passive component is grounded. Two input voltages A_1 and A_2 applied on Y1 and Y2-terminals, respectively and two output voltages V_{O+} and V_{O-} are obtained from the Z-terminals is shown in Fig. 4.2.

In block 1, the value of the following outputs is obtained:

$$V_{O+} = (A_1 - A_2)\frac{R_Z}{R_d}\frac{1}{(1+sR_ZC_d)} \tag{4.12}$$

$$V_{O-} = -(A_1 - A_2)\frac{R_Z}{R_d}\frac{1}{(1+sR_ZC_d)} \tag{4.13}$$

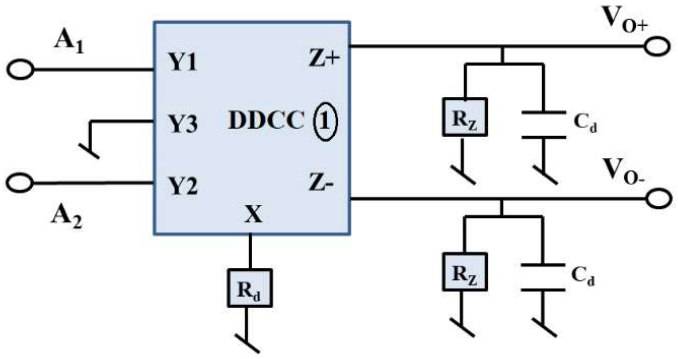


Fig. 4.2: Lossy Integration-Subtraction using DDCC

If $\frac{R_Z}{R_d} = 1$ and $R_ZC_d = \tau$ (4.14)

$$V_{O+} = (A_1 - A_2)\frac{1}{1+s\tau} \tag{4.15}$$

$$V_{O-} = -(A_1 - A_2)\frac{1}{1+s\tau} \tag{4.16}$$

4.3.2.2 Subtraction operation

Two resistors R_Z and R_d connected to the Z-terminals and the X-terminal in block-2, are used to implement this operation. Each passive component is grounded. Two input voltages A_1 and V_{O+} are applied on Y1 and Y2 terminals and output voltage B_1 is obtained from the Z-terminal as shown in Fig. 4.3.

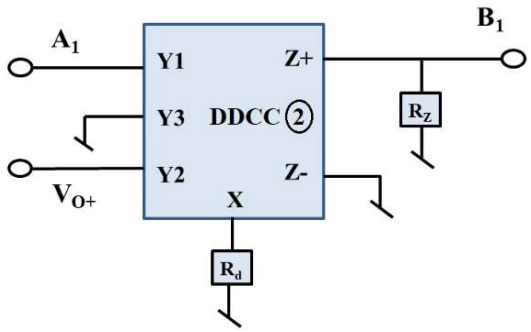


Fig. 4.3: Subtraction operation using DDCC

In block 2, $\frac{B_1}{R_Z} = \frac{A_1 - V_{O+}}{R_d}$ (4.17)

If $\frac{R_Z}{R_d} = 1$ then, $B_1 = A_1 - V_{O+}$ (4.18)

4.3.2.3 Summation operation

Two resistors R_Z and R_d connected to the Z-terminals and the X-terminal in block-3, are used to implement this operation. Each passive component is grounded. Two input voltages A_2 and V_{O-} are applied on Y1 and Y2-terminals and output voltage B_2 is obtained from Z-terminal as shown in Fig. 4.4.

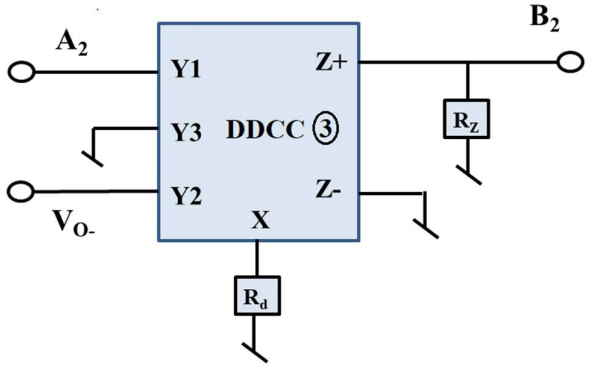


Fig. 4.4: Summation operation using DDCC

From eq. (3) and eq. (4) in block 3

$$\frac{B_2}{R_Z} = \frac{A_1 + V_{O-}}{R_d} \quad (4.19)$$

If $\frac{R_Z}{R_d} = 1$, $B_2 = A_2 + V_{O-}$ (4.20)

4.3.2.4 Inverter

Two resistors R_Z and R_d connected to the Z-terminals and the X-terminal in block-4, are used to implement this operation. Each passive component is grounded. One input voltage V_i is applied on the Y2-terminal and the output voltage V_O is obtained from the Z-terminal as shown in Fig. 4.5.

In block 4, $\frac{-V_i}{R_d} = \frac{V_O}{R_Z}$ (4.21)

If $\frac{R_Z}{R_d} = 1$, then the final output will be $V_O = -V_i$ (4.22)

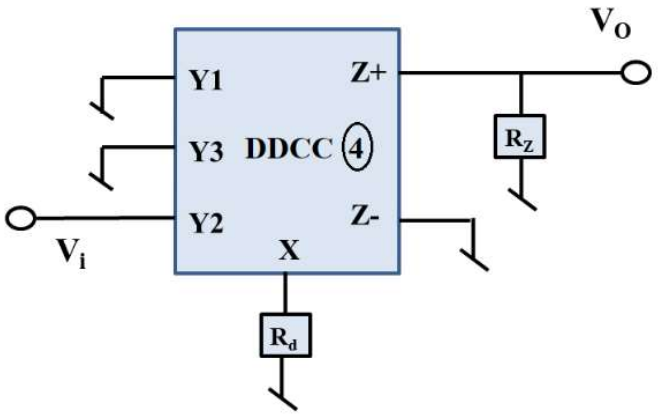


Fig. 4.5: Inverter using DDCC

The capacitance (C_{dL}) required to achieve the wave equivalent of a series inductor 'L' is obtained below. We know,

$\tau = \frac{L}{2R}$, $\tau = R_Z C_d$ and $R_Z = R_d = R$, thus

$$R_Z C_d = \frac{L}{2R} \text{ and } C_{dL} \sim C_d = \frac{L}{2RR_Z} = \frac{L}{2R^2} \quad (4.23)$$

Also, the capacitance (C_{dC}) required to achieve the wave equivalent of a shunt capacitor 'C' is calculated as,

$\tau = \frac{RC}{2}$, $\tau = R_Z C_d$ and $R_Z = R_d = R$, thus

$$R_Z C_d = \frac{RC}{2} \text{ and } C_{dC} \sim C_d = \frac{RC}{2R_Z} = \frac{C}{2} \quad (4.24)$$

From eq. (4.15, 4.16, 4.18, 4.20 and 4.22), the final relation between the incident wave and reflected wave of the proposed series inductor using all combined blocks is obtained below and is shown in Fig. 4.6.

$$B_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2) \quad (4.25)$$

$$B_2 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2) \quad (4.26)$$

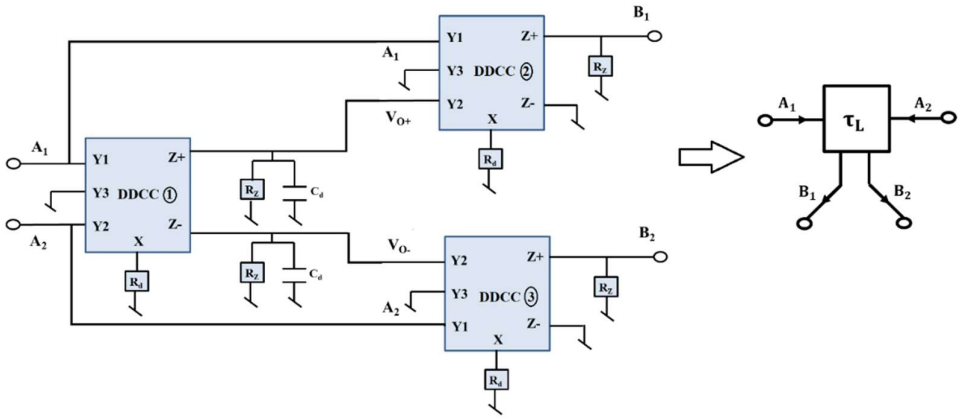


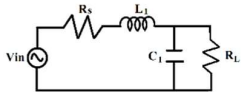
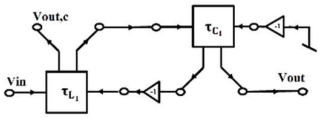
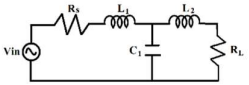
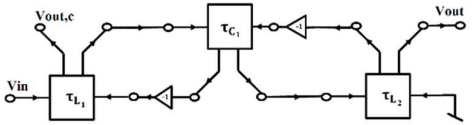
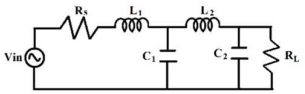
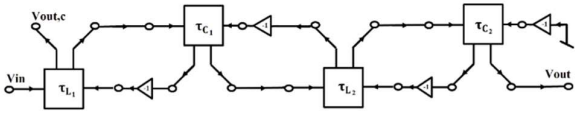
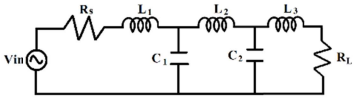
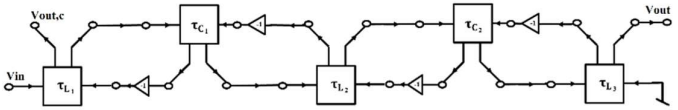
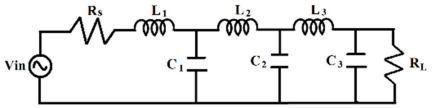
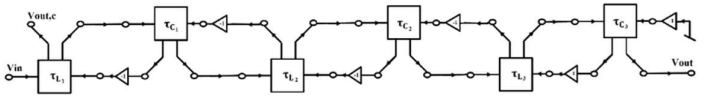
Fig. 4.6: WAE topology for series inductor

4.3.2.5 Simulation results

The SPICE simulator used 0.18 µm TSMC CMOS process parameters with supply voltage $V_{DD} = V_{SS} = \pm$ 0.9 V and a bias voltage of V_b = - 0.31 V to validate all simulation results. The values of all resistors R_d and R_Z are 1 kΩ. The different order of the Butterworth low pass filter synthesis is shown in Table 4.2, where LC ladder passive filters and respective wave active filters are presented.

Fig. 4.7 shows the frequency response of 2nd, 3rd, 4th, 5th and 6th order of LPF. The cut-off frequency at -3 dB gain is 200 kHz. The normalized values of the Butterworth low pass design are $R_s = R_L = 1$, L_{1N}, C_{1N}, L_{2N}, C_{2N}, L_{3N} and C_{3N}.

Table 4.2: Different order of LP Butterworth filter synthesis

Order	LC ladder filter	Wave active filter
2nd		
3rd		
4th		
5th		
6th		

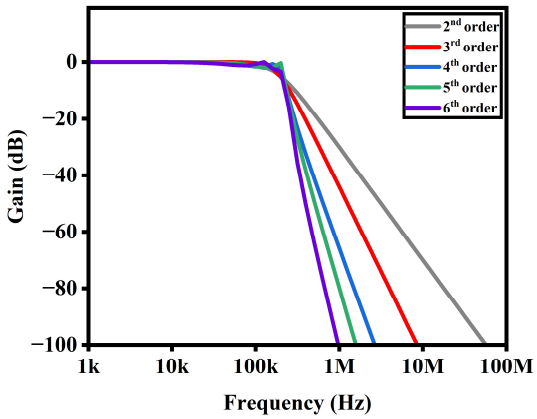
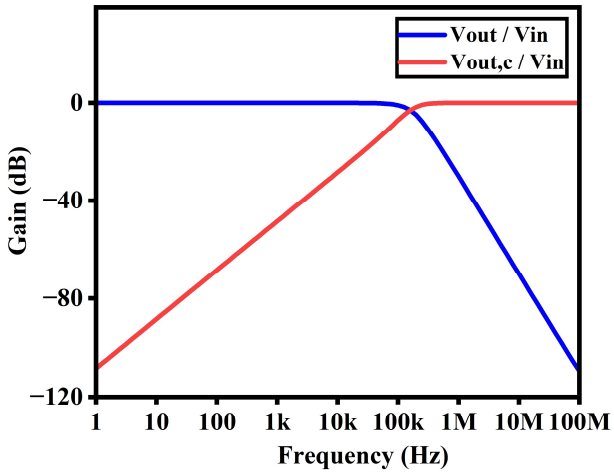


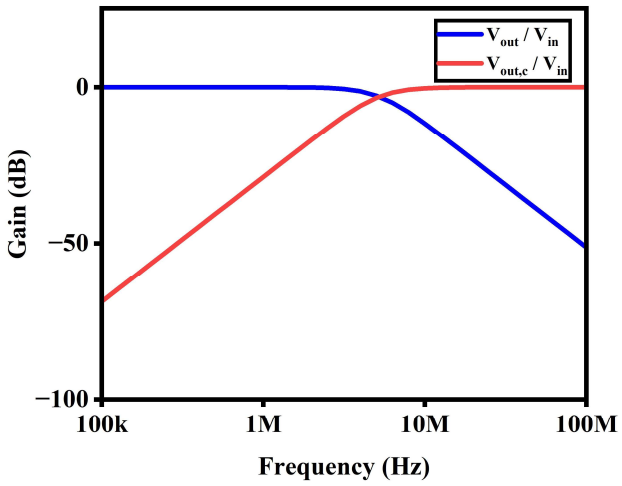
Fig. 4.7: Frequency response of n^{th} order Butterworth filter (n = 2, 3, 4, 5, 6)

Table 4.3: Normalized values and calculated Wave active values for the design of 200 kHz cut-off frequency

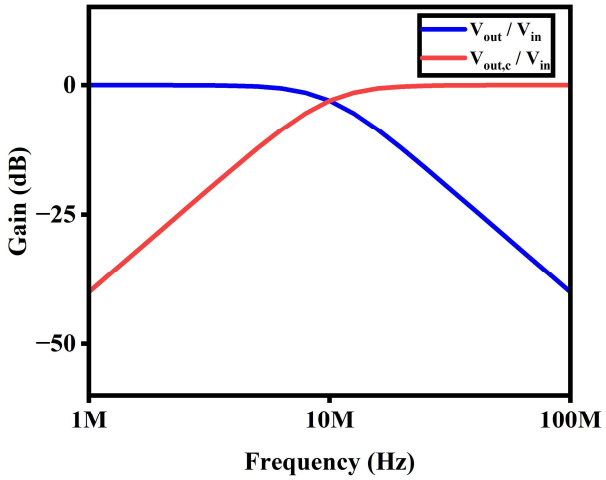
Order	Normalized values (Passive filter)						WAE actual values (Wave active filter)					
	L_{1N}	C_{1N}	L_{2N}	C_{2N}	L_{3N}	C_{3N}	C_{dL1} (nF)	C_{dC1} (nF)	C_{dL2} (nF)	C_{dC2} (nF)	C_{dL3} (nF)	C_{dC3} (nF)
2	1.414	1.414	-	-	-	-	0.562	0.562	-	-	-	-
3	1	2	1	-	-	-	0.397	0.795	0.397	-	-	-
4	0.765	1.848	1.848	0.765	-	-	0.304	0.735	0.735	0.304	-	-
5	0.618	1.618	2	1.618	0.618	-	0.245	0.643	0.795	0.643	0.245	-
6	0.517	1.414	1.932	1.932	1.414	0.517	0.205	0.562	0.767	0.767	0.562	0.205



(a)



(b)

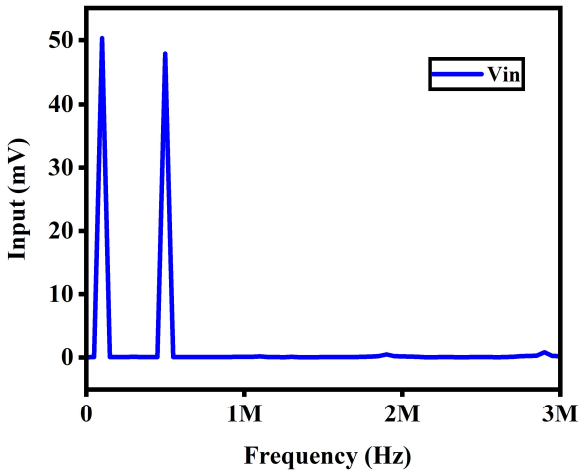


(c)

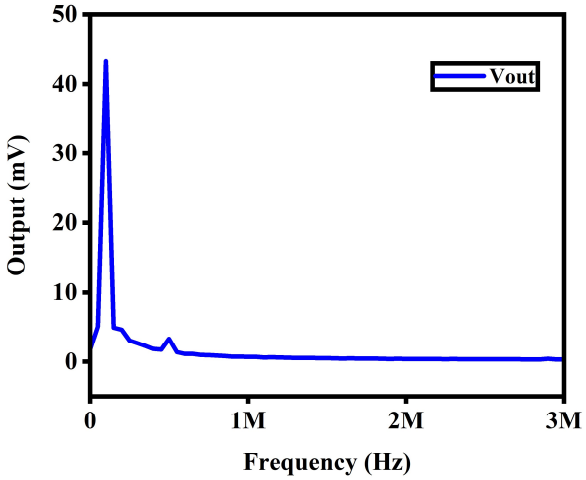
Fig. 4.8: Frequency response of 2nd order LPF and its complementary HPF at (a) 200 kHz (b) 5 MHz (c) 10 MHz frequencies

According to Eqs. (4.23) and (4.24), the capacitance of series inductor (C_{dL1}, C_{dL2}, C_{dL3}) and capacitance of shunt capacitors (C_{dC1}, C_{dC2}, C_{dC3}) are calculated. The port resistance 'R' is set to 1 kΩ. We can observe that as the order of the filter increases, the frequency response becomes an ideal means function that approximates the ideal LP specification in a maximally flat sense.

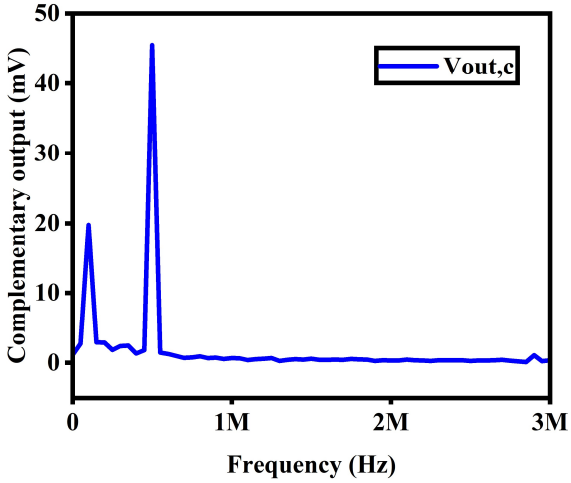
Fig. 4.8 Shows the frequency response of the 2nd order low pass filter and its complementary as high pass filter at different frequencies. For 2nd order LC ladder



(a)



(b)



(c)

Fig. 4.9: Spectrum of 2nd order LPF (a) input (b) output and (c) its complementary

filters $f_c = \frac{1}{2\pi\sqrt{LC}}$ and $\omega = 2\pi f_c$. The theoretical values of f_c are 222 kHz, 5.42 MHz, and 11.06 MHz, whereas simulated values are 200 kHz, 5 MHz and 10 MHz. The value of C_d of L_1 and C_1 are 22.5 pF and 22.5 pF respectively for 5 MHz frequency, and 11.24 pF and 11.24 pF respectively for 10 MHz. The theoretical values of the cutoff frequency of -3 dB gain of this LPF are well matched with simulated values.

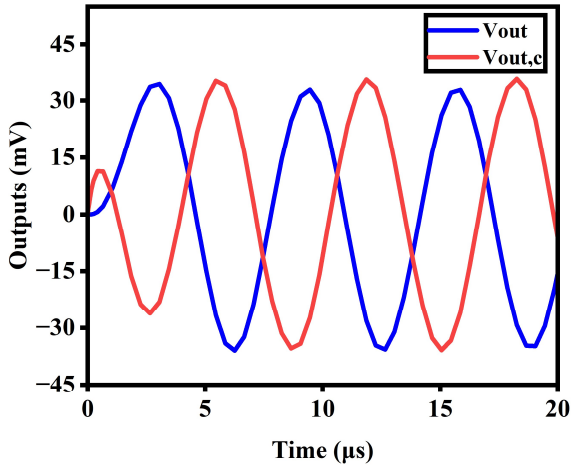
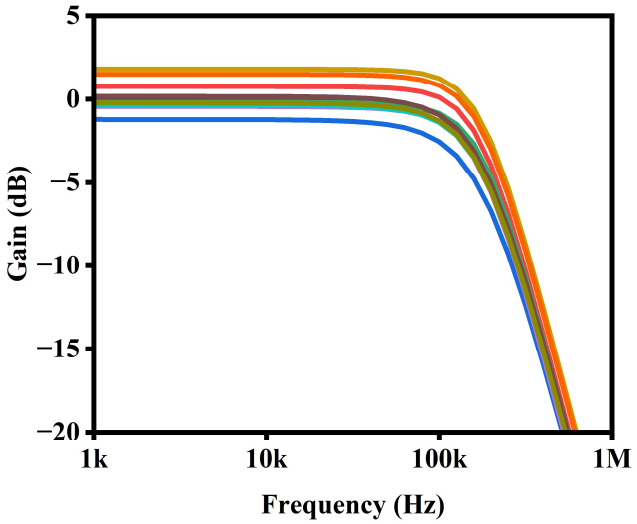
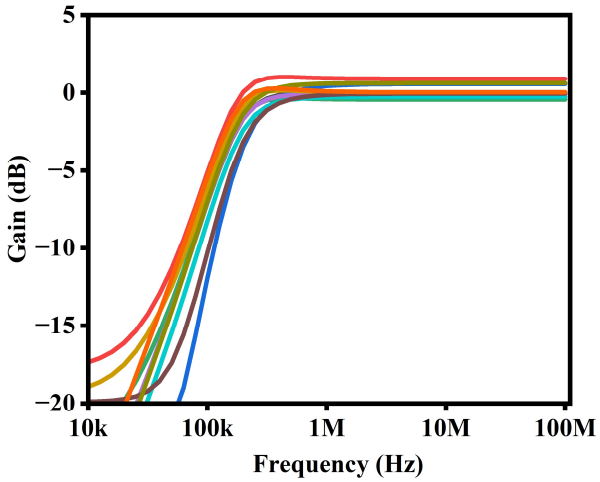


Fig. 4.10: Transient response of 2nd order LPF and its complementary



(a)



(b)

Fig. 4.11: Monte Carlo simulation (a) LPF (b) its complementary as HPF

To investigate the time domain behavior, the input signal of 50 mV amplitude with frequencies of 50 kHz and 300 kHz is applied. Fig. 4.9 and Fig. 4.10 show the spectrum and transient response for input and output, respectively, demonstrating that the 300 kHz signal is significantly attenuated.

It is relatively typical to have device mismatches during the fabrication of analog and digital integrated circuits, which can result in some behavioural variations in the circuit. Statistical analysis can be used to investigate the effect of random variation on circuits. As a result, Monte Carlo simulations (MCS) were used to do the statistical analysis for the proposed second order, which is another measure of the robustness and uncertainty of the proposed design. Fig. 4.11 depicts a random sampling approach for transistor mismatching and process statistical variation generated by setting 100 runs, 5% tolerance in Resistance (R_d) and Capacitance (C_d) at cutoff frequency of -3dB gain of the second-order filter with LPF responses and complementary as HPF responses. The proposed filter is simulated for the cutoff frequency of 200 kHz. The output noise is 5.1738 f V/√Hz as shown in Fig. 4.12 and the %THD obtained from the simulation is within 1.12 % up to 50 mV p–p.

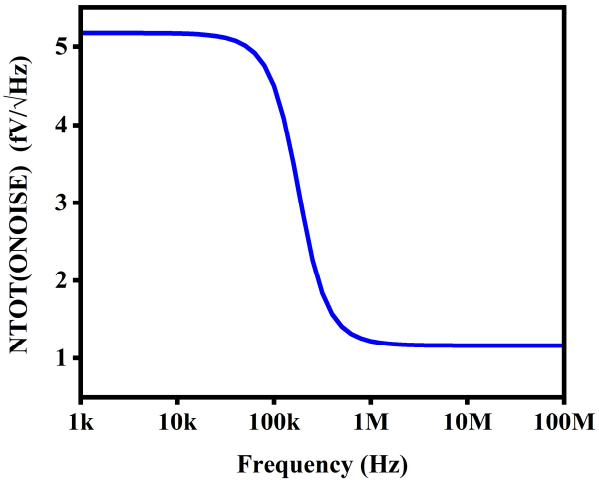


Fig. 4.12: Total output noise voltage

4.3.3 Proposed CM-based Wave Active Filter using EXCCCCTA Block

Eqs (4.6), (4.7), (4.9) and (4.10) can be determined using the following operations: (i) Lossy Integration-Subtraction; (ii) Lossy Integration-Addition.

4.3.3.1 Series inductor

To realize Eq. (4.32) and Eq. (4.33) or implement a series inductor, an EX-CCCCTA, as well as a parallel connection of a resistor and capacitor is utilized. The implementation of this series inductor needs the use of lossy integration techniques, including addition and subtraction operations. The input currents A_1 or A_2 are applied at X_1 or X_2 terminals, and the EX-CCCCTA performs subtraction operation (A_1-A_2) as output terminals Z_{1-} and Z_{2+} are connected at a node. The lossy integration operation is also performed at these terminals and conveys the same to the high-impedance at O_- and O_+ terminals. Fig. 4.13(a) provides a proper circuit of the proposed wave active series inductor employing EX-CCCCTA, and Fig. 4.13(b) reproduces its wave flow diagram as shown in Table 4.1. The standard analysis of the circuit yields two lossy

integrator outputs at the O-terminals: one is inverted (I_{o-}), and the other is non-inverted (I_{o+}).

$$I_{O+} = (A_1 - A_2)\frac{g_m R_d}{1+sR_dC_d} \quad (4.27)$$

$$I_{O-} = -(A_1 - A_2)\frac{g_m R_d}{1+sR_dC_d} \quad (4.28)$$

$$\text{If } \ g_m R_d = 1 \text{ and } R_dC_d = \tau \quad (4.29)$$

$$I_{O+} = (A_1 - A_2)\frac{1}{1+s\tau} \quad (4.30)$$

$$I_{O-} = -(A_1 - A_2)\frac{1}{1+s\tau} \quad (4.31)$$

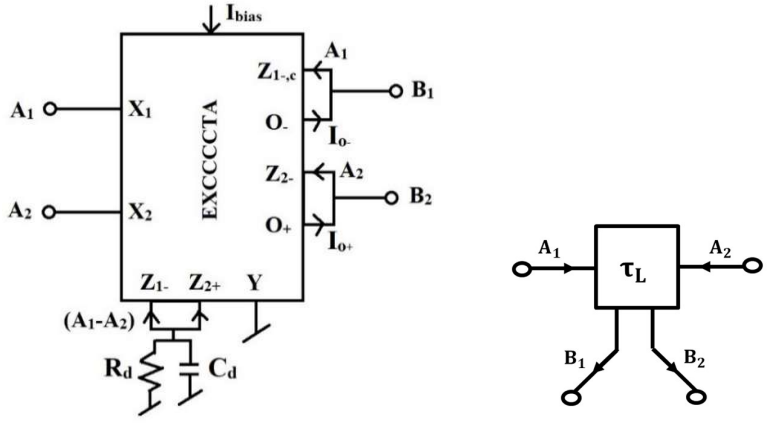
Further, the EX-CCCCTA also performs summation and subtraction operations by connecting the output terminals O_- and O_+ with output terminals ($Z_{1-,c}$) and (Z_{2-}) to realize B_1 and B_2 respectively. According to current at $Z_{1-,c}$ and Z_{2-} terminals provide A_1 and A_2. The ideal relation between the incident and reflected waves of the designed series inductor with the block is shown below.

$$B_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2) \quad (4.32)$$

$$B_2 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2) \quad (4.33)$$

The capacitance (C_{dL}) required to achieve a series inductor 'L' is obtained below:

$$C_{dL} \sim C_d = \frac{L}{2RR_d} = \frac{L}{2R^2} \quad (4.34)$$



(a) (b)

Fig. 4.13: Proposed Wave Active of the series inductor (a) using EX-CCCCTA (b) Wave flow diagram

4.3.3.2 Shunt capacitor

To realize Eq. (4.39) and Eq. (4.40) or implement a shunt capacitor, an EX-CCCCTA, as well as a parallel connection of a resistor and capacitor is utilized. The implementation of this shunt capacitor needs the use of lossy integration techniques, including summation and subtraction operations. The input currents A_1 or A_2 are applied at X_1 or X_2 terminals, and the EX-CCCCTA performs an addition operation (A_1+A_2) as output terminals Z_{1-} and Z_{2-} are connected at a node. The lossy integration operation is also performed at these terminals and conveys the same to the high-impedance at two O_+ terminals. Fig. 4.14(a) provides a proper circuit of the proposed wave active shunt capacitor employing EX-CCCCTA, and Fig. 4.14(b) reproduces its wave flow diagram as shown in Table 4.1. The standard analysis of the circuit yields two lossy integrator outputs at the O-terminals: two non-inverted (I_{o+}) and ($I_{o+,c}$).

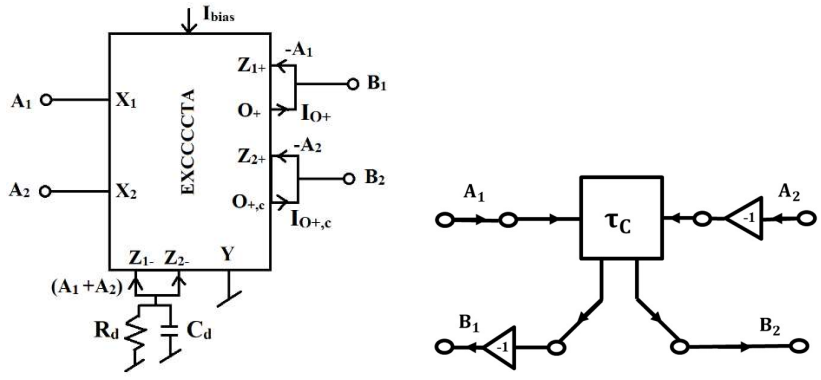
$$I_{O+} = (A_1 + A_2)\frac{g_m R_d}{1+sR_dC_d} \tag{4.35}$$

$$I_{O+,c} = (A_1 + A_2)\frac{g_m R_d}{1+sR_dC_d} \tag{4.36}$$

If $g_m R_d = 1$ and $R_dC_d = \tau$

$$I_{O+} = (A_1 + A_2)\frac{1}{1+s\tau} \tag{4.37}$$

$$I_{O+,c} = (A_1 + A_2)\frac{1}{1+s\tau} \tag{4.38}$$



(a) (b)

Fig. 4.14: Proposed Wave Active of shunt capacitor (a) using EX-CCCCTA (b) Wave flow diagram

Further, the EX-CCCCTA also performs summation operations by connecting the output two terminals O_+ with output terminals (Z_{1+}) and (Z_{2+}) to realize B_1 and B_2 respectively. According to the current Z_{1+} and Z_{2+} terminals provide A_1 and A_2. The ideal relation between the incident and reflected waves of the designed shunt capacitor with the block is shown below.

$$B_1 = -A_1 + \frac{1}{1+s\tau}(A_1 + A_2) \tag{4.39}$$

$$B_2 = -A_2 + \frac{1}{1+s\tau}(A_1 + A_2) \tag{4.40}$$

Also, the capacitance (C_{dC}) required to achieve a shunt capacitor 'C' is calculated as:

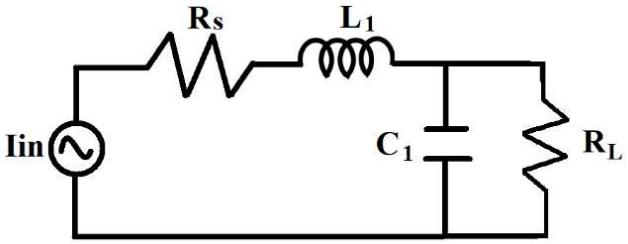
$$R_d C_d = \frac{RC}{2} \text{ and } C_{dC} \sim C_d = \frac{RC}{2R_d} = \frac{C}{2} \tag{4.41}$$

4.3.3.3 Simulation results

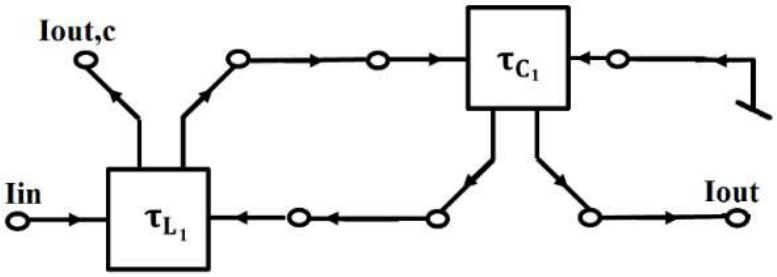
In this section, a 2nd order Butterworth low pass filter is simulated. The component values are normalized to achieve a maximally flat response for the 2nd-order Butterworth filter. These normalized values are as follows: $R_s = 1$, $L_1 = 1.414$, $C_1 = 1.414$, and $R_L = 1$. Fig. 4.15(a) depicts the use of a 2nd order Butterworth low-pass filter. Fig. 4.15(b) shows the equivalent wave flow diagram based on Table 4.2. In this instance, I_{out} represents the desired low pass output, and $I_{out,c}$ denotes its complementary output, resulting in a high pass response.

The simulation employs 0.18 μm TSMC CMOS technology, with bias currents set at $I_o = 10$ μA, $I_{bias} = 130$ μA, and a supply voltage of ±1 V. For an acceptable cut-off frequency (f_c) of 200 kHz, the computed capacitance values for the wave equivalents of the series inductor (L_1) and shunt capacitor (C_1) are both 0.562 nF. Fig. 4.16(a) shows the frequency response at various frequencies (200 kHz, 5 MHz, 10 MHz), as well as the time-domain characteristics of the low-pass and complementary high-pass filters, are shown in Fig. 4.16(b). For attaining a cut-off frequency (f_c) of 5 MHz, the computed capacitance values for the wave equivalents associated with the series inductor (L_1) and shunt capacitor (C_1) are both determined to be 11.24 pF. Likewise, for f_c = 10 MHz, the calculated capacitance values for the wave equivalents

corresponding to the series inductor (L_1) and shunt capacitor (C_1) are both established at 22.5 pF.

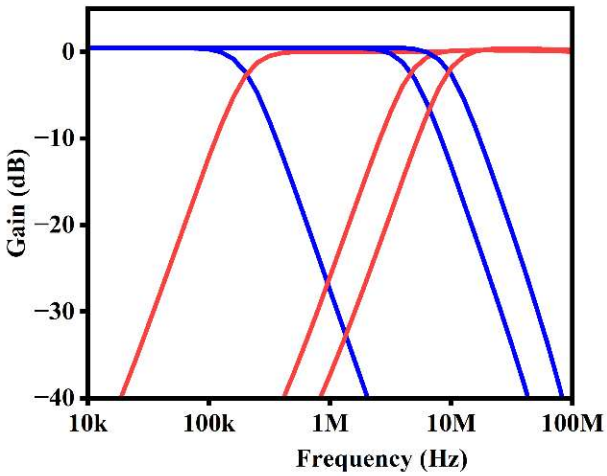


(a)

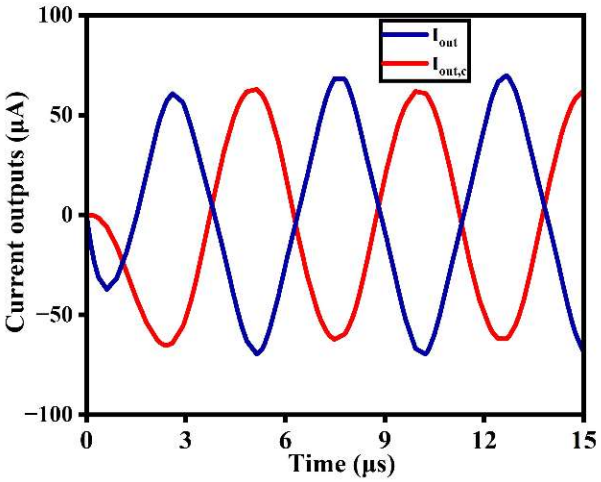


(b)

Fig. 4.15: (a) 2nd order Butterworth low pass filter (b) Wave flow diagram of 2nd order Butterworth low pass filter

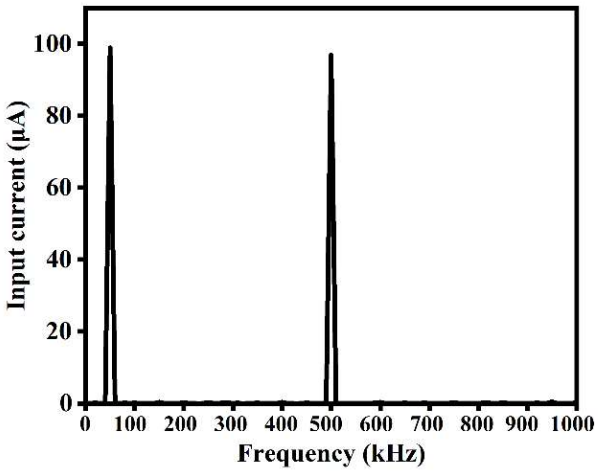


(a)

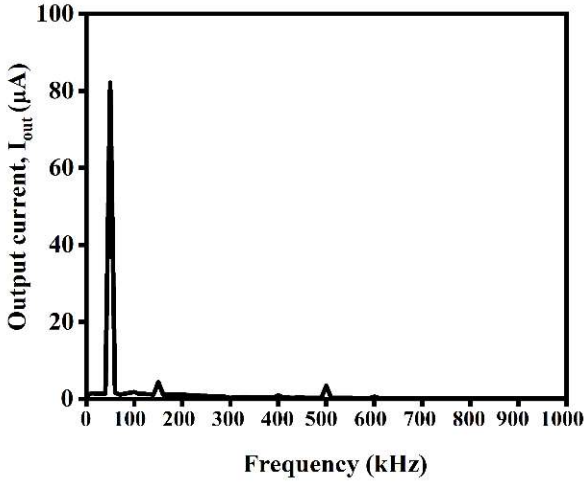


(b)

Fig. 4.16: LPF and HPF (a) Frequency response (b) Transient response



(a)



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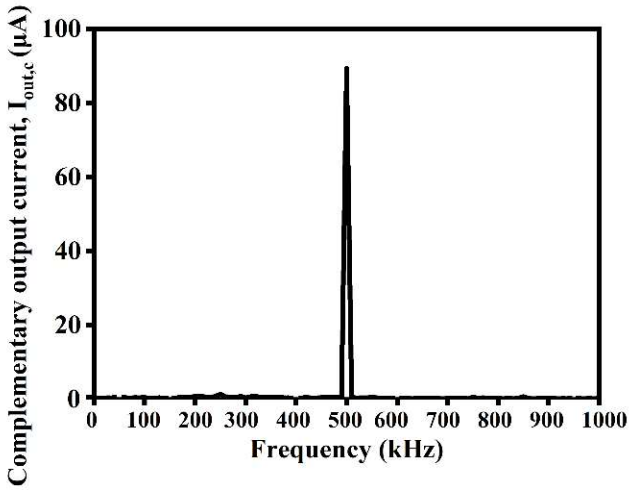


(c)

Fig. 4.17: Spectrum analysis of (a) input current (b) LPF (c) HPF

The spectrum analysis at both the input and output to assess the effectiveness of the filter, we apply a signal consisting of two frequencies, 50 kHz and 500 kHz, each with an amplitude of 100 μA, at the input of the filter and presented in Fig.4.17(a). These results demonstrate the effective elimination of the 500 kHz signal at the output of the low pass filter in Fig. 4.17(b) and the effective attenuation of 50 kHz signal at the output of the high pass filter in Fig. 4.17(c).

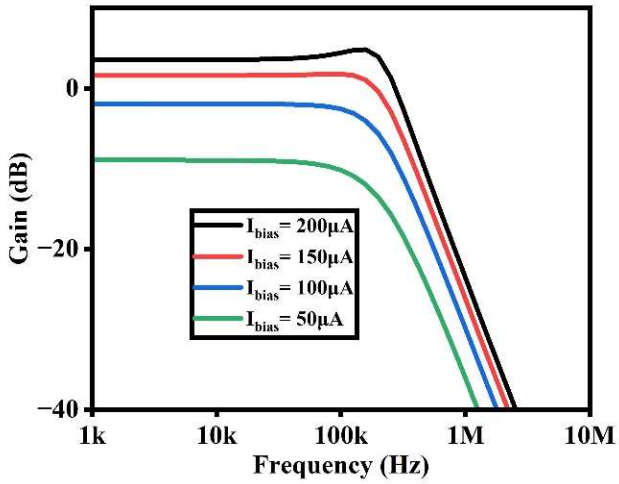


Fig. 4.18: Frequency response of low pass filter at different current bias

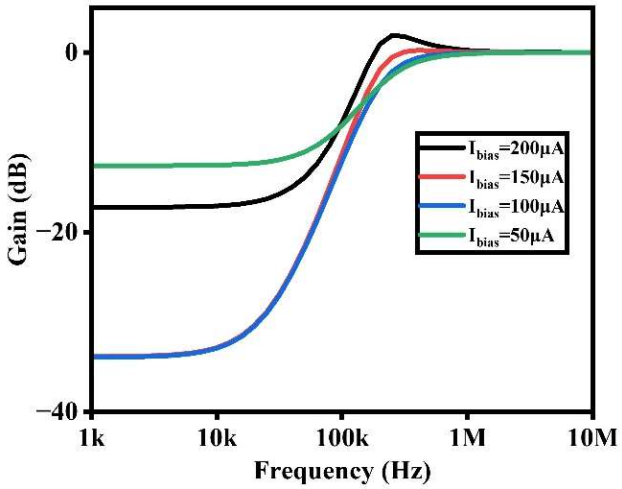


Fig. 4.19: Frequency response of high pass filter at different current bias

The frequency responses illustrated in Fig. 4.18 and Fig. 4.19 highlight the electronic tunability of the cut-off frequency of the filter by adjusting the bias current of EX-CCCCTA for low-pass and high-pass filters, respectively. Calculations reveal the power consumption and noise of the filter to be 2.01 mW and 1.81 nV/Hz, respectively. Fig. 4.20 and Fig. 4.21 present the total output noise voltage and the percentage of total harmonic distortion (% THD). Notably, the THD consistently stays below 7%, indicating that the performance of the filter remains within acceptable limits as the cut-off frequency varies.

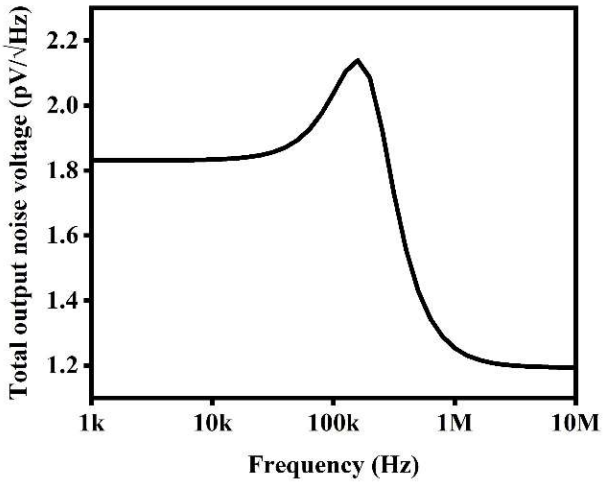


Fig. 4.20: Total output noise voltage

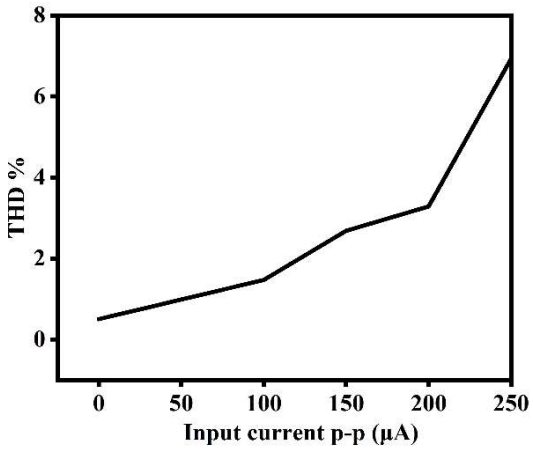
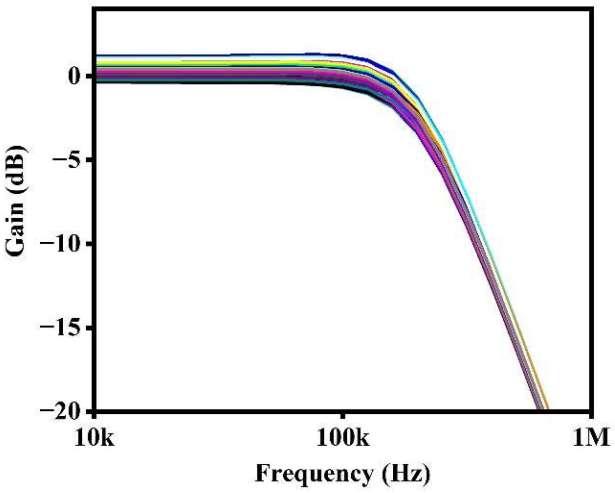
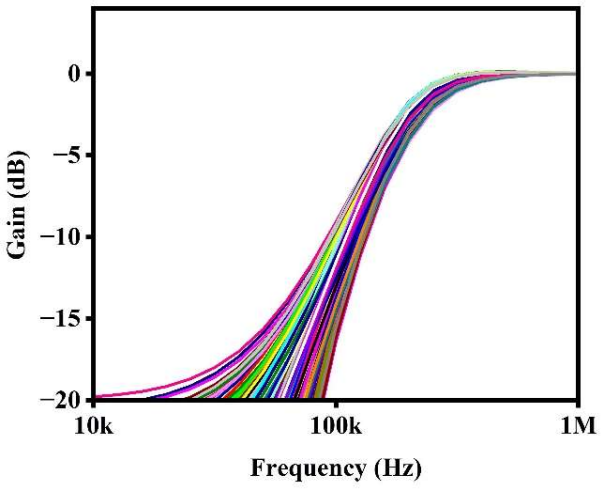


Fig. 4.21: Total harmonic distortion



(a)



(b)

Fig. 4.22: MCS of (a) LPF (b) HPF

Device incompatibilities occur frequently when fabricating analog integrated circuits. This can cause differences in the functioning of the circuit. The use of statistical analysis to study the effects of random variations on circuits is widespread practice. Monte Carlo simulations (MCS) are used to undertake a statistical study of the proposed second-order filter. This approach provides an additional method for assessing the robustness and uncertainty of the proposed design. Fig. 4.22 depicts an MCS technique used to analyse transistor mismatching and process statistical variance. For the second-order filter, 500 runs have been performed with a 5% tolerance in resistance (R_d) and capacitance (C_d), demonstrating both LPF and its complementary HPF responses in Fig. 4.22(a) and Fig. 4.22(b) respectively.

Table 4.4. The performance values of EX-CCCCTA based 2nd order Butterworth filter

Parameters	**Values**
EX-CCCCTA block	1
No. of transistor	47
No. of R, C	1, 1
Cut-off frequency (up to)	10 MHz
Power supply	± 1V
Input current	100 µA
Bias current	130 µA
Power consumption	2.01 mW
Total output noise voltage	1.81 nV/Hz
THD% at 100 µA (p-p)	1.05
Capacitance values of L_1, C_1 for 200 kHz	0.562 nF, 0.562 nF
for 5 MHz	11.24 pF, 11.24 pF
for 10 MHz	22.50 pF, 22.50 pF

Table 4.4 shows the performance of EX-CCCCTA-based WAF of 2nd order. The literature review of existing work and a comparison with the proposed work and brief is presented as below:

- Reduced number of components: The proposed EX-CCCCTA circuit has only 47 transistors, which is significantly lower than the number of transistors in the existing circuits.
- Lower power consumption: The proposed EX-CCCCTA circuit consumes less power than the existing circuits, due to its reduced number of components.
- Higher frequency bandwidth: The proposed EX-CCCCTA circuit has a higher frequency bandwidth (up to 10 MHz) than the existing circuits, making it suitable for high-speed applications.
- Improved robustness: The proposed EX-CCCCTA circuit is more robust to noise and variations in component parameters than the existing circuits.

4.4 Concluding remarks

A new wave-active n^{th}-order low-pass Butterworth filter (n = 2, 3, 4, 5, 6), wave active components and wave active elements based on DDCC are presented. WACs such as lossy integration-subtraction, subtraction, summation, inverter and WAEs such as series inductor and shunt capacitor, are the primary components and elements respectively in realizing a wave-active filter. The wave method is validated by achieving n^{th}-order Butterworth low-pass responses. It should be observed that the complete realization employs all grounded passive components, which is advantageous in terms of IC implementation. The WAF can be operated up to 10MHz. The proposed method is validated for an n^{th}-order low-pass filter using SPICE simulations using 0.18 μm CMOS technology parameters.

The design presents an improved current mode wave active filter based on the EX-CCCCTA that employs fundamental wave elements. Using a single EX-CCCCTA and grounded capacitor, the design provides wave equivalents for series inductors and shunt capacitors, emphasizing its simplicity and effectiveness. This design includes an

electronic tunable for adjusting the cutoff frequency of the filter, offering the system an extensive range of flexibility. Additionally, the significant characteristics of 2^{nd}-order Butterworth low-pass filters are as follows: it has two active building blocks (ABBs), an output noise level of 1.81 nV/Hz, and a power consumption of 2.01 mW. The simulated results well match the theoretical analysis.

Chapter 5

Design and Analysis of Rectifiers

1. S. Kumari, D. Nand and S. Kant, "MOS-based Electronically tunable current-mode dual-output full-wave rectifier using single DDCCTA", *Electrical Engineering Journal*, Vol. **107**, 4203–4213 (2025). https://doi.org/10.1007/s00202-024-02736-7.
2. S. Kumari and D. Nand, "Current mode Positive and Negative Rectifier based on DDCC suitable for Higher Frequency operations", *IOP Conference Series: Materials Science and Engineering, Volume 1084, First International Conference on Circuits, Signals, Systems and Securities (ICCSSS 2020)* 11th-12th December 2020, Tamil Nadu, India 1084 012079. https://doi.org/10.1088/1757-899X/1084/1/012079.

5.1 Introduction

Full-wave rectifiers are essential components widely used in various fields, including signal processing, instrumentation, communications, and measurement systems. Their applications extend to AC voltmeters, ammeters, wattmeters, RF modulators and demodulators, signal polarity detection, peak and average detection, function filtering, absolute value computation, and frequency doubling [8]. Additionally, they play a critical role in RMS-to-DC converters and clipper circuits, finding utility in ultrasonic in-floor detectors and other advanced systems [65]. Despite their versatility, conventional diode-based rectifiers face limitations due to their threshold voltage (~0.3 V for germanium and ~0.7 V for silicon), which restricts their use in high-precision applications requiring low threshold voltages [66]. These challenges emphasize the need for innovative rectifier designs capable of addressing such constraints, thus enabling broader and more accurate applications across diverse fields.

A current-mode (CM) full-wave rectifier (FWR) employs a differential difference current conveyor (DDCC), two MOS diodes, and three grounded resistors. It provides two rectifier proposals: the CM FW positive rectifier and the CM FW negative rectifier. A MOS-based current-mode (CM) full-wave rectifier (FWR) with electronically controllable dual outputs is provided. As an active block, the circuit includes a single differential difference current conveyor transconductance amplifier (DDCCTA), two MOS-based active diodes, and four grounded active resistors.

5.2 Literature review

The brief of the available literature is summarized in this section based on electronic tunability, the number of blocks and the number of diodes required to construct the rectifier etc. It is noted that the structures reported in Ref. [65-91] and Ref. [92-124] are classified as CM and VM respectively. The FWR in [73, 75, 78] possesses electronic tunability. These FWRs employ numerous CM blocks namely Operational Trans-conductance Amplifier (OTA) [75, 86], Current Differencing Transconductance

Amplifier (CDTA) [67, 69, 71], Current Follower Transconductance Amplifier (CFTA) [73], Operational Floating Current Conveyor (OFCC) [72], Differential Voltage Current Conveyor (DVCCTA) [88], Current Differencing Buffer Amplifier (CDBA) [75], Extra-X Current Conveyor (EXCCII) [80]. More than one active block is used in [78] while some reported without any active block where only MOS transistors are used in [65, 66, 68, 70, 78, 79]. Conventional diodes are also used in Ref. [67, 69, 71, 75, 76, 81] and possible hardware realization is done in [73, 75, 88]. Most of the available CM FWRs provide single output except [68, 78, 81]. The DC offset at zero crossing (worst case) is reported in [65, 70, 76, 77, 81]. The DC value transfer (ρ_{DC}) and RMS error (ρ_{RMS}) are computed in [71, 76, 77, 81].

Keeping in view the above-mentioned facts and features of CM blocks, a FWR using the DDCCTA block is proposed and investigated. To the best of our knowledge, this proposal is the first to employ DDCCTA to develop a current-mode dual-output full-wave rectifier in one topology. The key salient features of the proposed design are as follows: (i) It uses a single analog building block and its possible hardware realization is presented. (ii) MOS-based resistors and diodes are used. (iii) It is capable of providing dual outputs (positive and negative FWR) in one proposed topology. The application of dual outputs is to generate dual DC supply voltage. (iv) The outputs are electronic tunable. (v) The output impedance is high causing an easy cascading feature of the design.

5.3 Proposed Designs of Rectifiers

A CM FWR employs a DDCC, two MOS diodes, and three grounded resistors. It provides two rectifier proposals: the CM FW positive rectifier and the CM FW negative rectifier. A MOS-based CM FWR with electronically controllable dual outputs using DDCCTA, two MOS-based active diodes, and four grounded active resistors is provided.

5.3.1 Proposed CM-based rectifier using DDCC Block

The proposed full-wave rectifier is shown in which one DDCC block and two MOS are used. Here, M1 and M2, two MOS-based diodes are behaving like switches. Eq. (5.1) shows the output current of the proposed rectifiers. The working of rectifiers and resulting outputs.

For positive rectifier

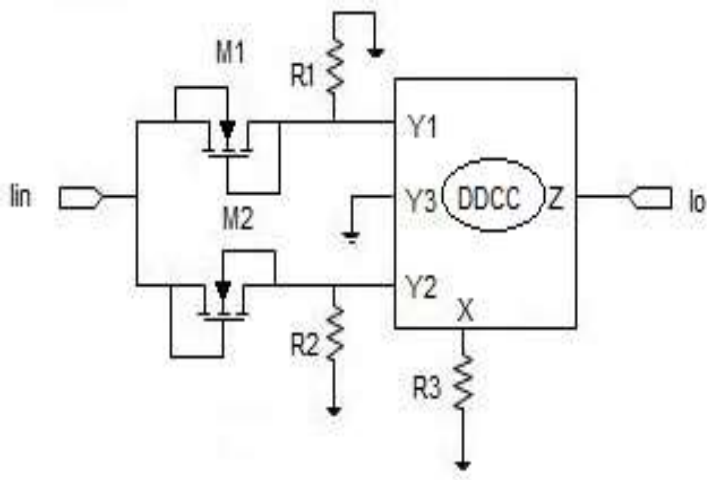
$$I_O(t) = \begin{cases} \frac{R_1}{R_3} I_{in}(t) & \text{For } I_{in}(t) > 0, \text{ M1:ON, M2:OFF} \\ -\frac{R_2}{R_3} I_{in}(t) & \text{For } I_{in}(t) < 0, \text{ M1:OFF, M2:ON} \end{cases}$$

For negative rectifier

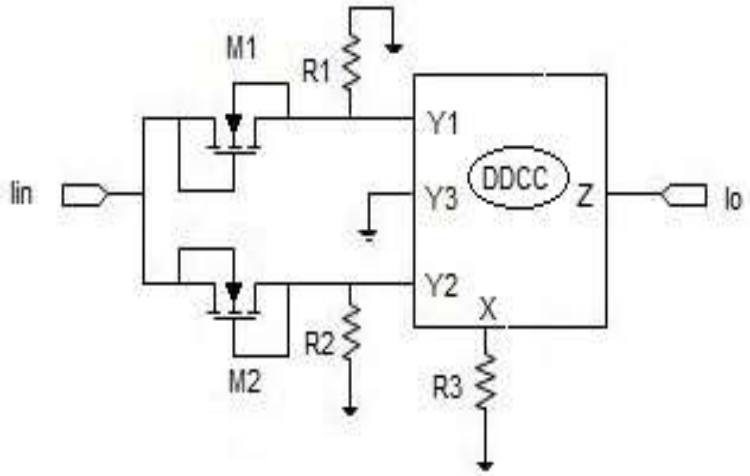
$$I_O(t) = \begin{cases} -\frac{R_1}{R_3} I_{in}(t) & \text{For } I_{in}(t) > 0, \text{ M1:OFF, M2:ON} \\ \frac{R_2}{R_3} I_{in}(t) & \text{For } I_{in}(t) < 0, \text{ M1:ON, M2:OFF} \end{cases}$$

If $R_1 = R_2 = R_{eq}$, then the output current equation of the proposed FWR would be:

$$I_O(t) = \frac{R_{eq}}{R_3} I_{in}(t) \tag{5.1}$$



(a)



(b)

Fig. 5.1: Proposed (a) positive rectifier (b) negative rectifier

5.3.1.1 Simulation results

The PSPICE simulation results using 180 nm TSMC CMOS process parameters with supply voltage $V_{DD} = V_{SS} = \pm$ 0.9 V and two bias voltages of V_B = - 0.1 V and V_{B1} = - 0.31 V. The values of all resistors are 1 kΩ. The power dissipation of the proposed rectifiers is 2.94 mW.

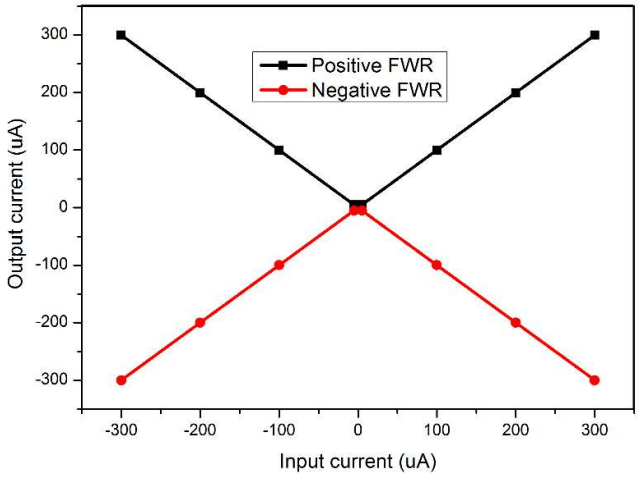
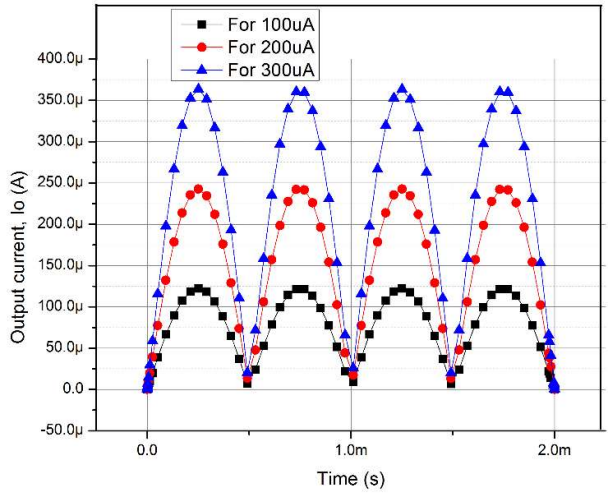
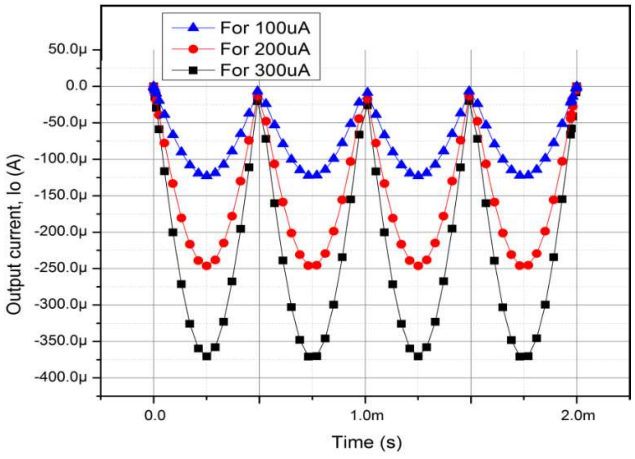


Fig. 5.2: DC response of the proposed FWRs

The DC transfer characteristic of the proposed FWR is shown in Fig. 5.2 with a dynamic current range of -300 µA to 300 µA. Fig. 5.3 shows simulated rectified outputs on the transient response of FWR for different amplitudes 100 µA, 200 µA and 300 µA at 1 KHz. The maximum operating frequency is 200 MHz and the respective simulation result is shown in Fig. 5.4 for positive FWR and negative FWR. Fig. 5.5 shows the transient response of the triangular output current for the peak-to-peak -100 µA to 100 µA triangular input current.

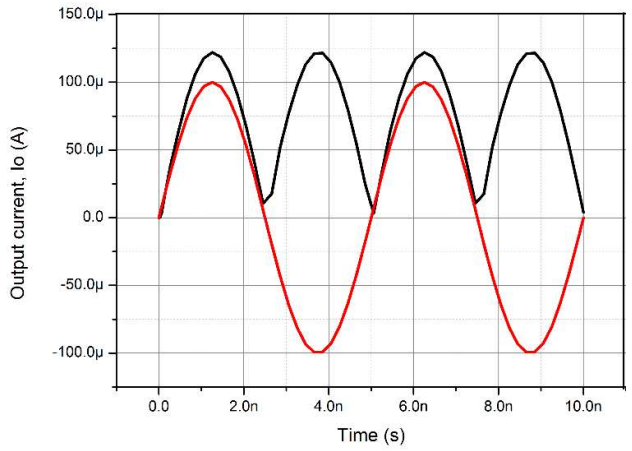


(a)

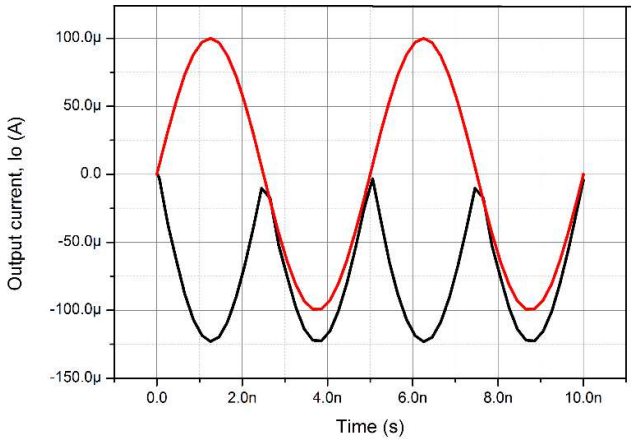


(b)

Fig. 5.3: Transient responses of proposed (a) positive FWR (b) negative FWR

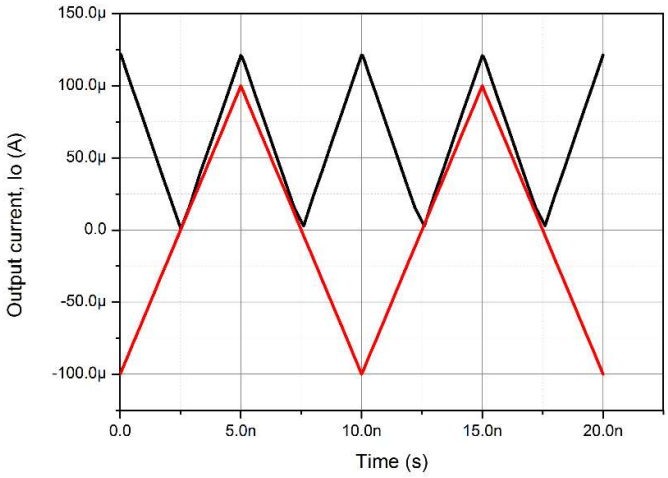


(a)

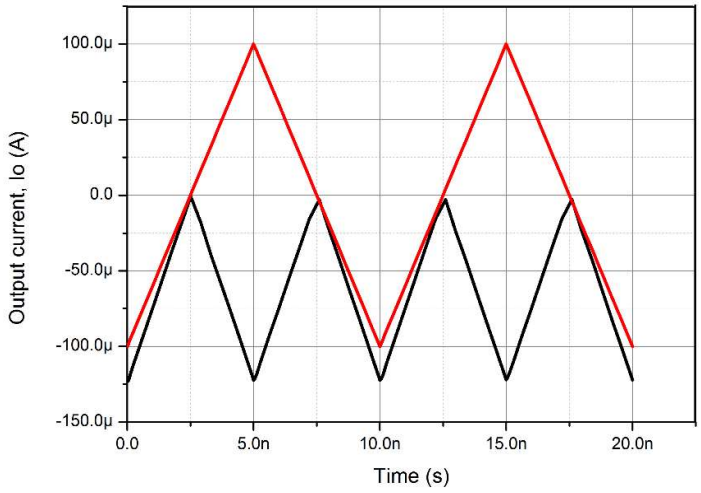


(b)

Fig. 5.4: The output current of (a) Positive FWR (b) Negative FWR at 200 MHz



(a)



(b)

Fig. 5.5: The output current of (a) Positive FWR (b) Negative FWR for triangular input current

5.3.2 Proposed CM-based dual output rectifier using DDCCTA Block

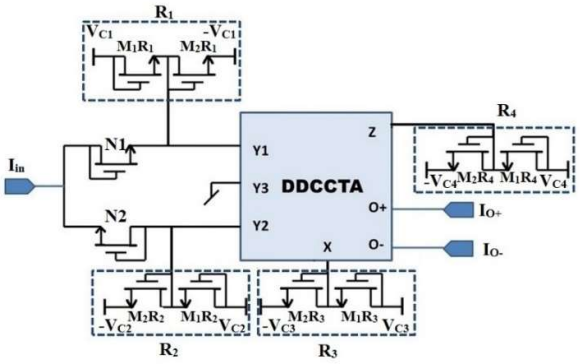
The proposed dual output FWR is shown in Fig. 5.6(a). It utilizes a single DDCCTA, and two MOS diodes N1 and N2 [126]. Additionally, it makes use of four MOS-based resistors [125] R_i (i= *1,2,3,4*) formed by MOS transistors M_1R_i and M_2R_i. The advantages of a MOS-based resistor include its tunability, and ease of integration into integrated circuit designs for a more scalable and potential for increased power efficiency, particularly in low-power applications. Simulations indicate that the FWR using MOS-based resistors has better performance features than the passive resistor, including lower voltage ripple, improved linearity, and better signal-to-noise ratio. The value of resistance R_i is controllable by V_{Cj} (j=*1,2,3,4*) and is given by Eq. (5.2) [24] and shown in Fig. 5.6(b).

$$R_i = \frac{1}{2K(V_{Cj} - V_{TH})} \tag{5.2}$$

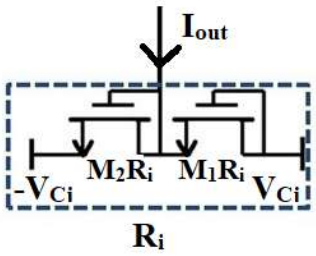
The outputs of the proposed circuit at high impedance are I_{O+} and I_{O-}. Further output currents of positive and negative rectifiers may be obtained in positive and negative cycles as follows in Eq. (5.3) and Eq. (5.4):

$$I_{O+}(t) = \begin{cases} g_m R_1 \frac{R_4}{R_3} I_{in}(t) & \text{For } I_{in}(t) > 0, \text{ N1:ON, N2:OFF} \\ g_m(-R_2) \frac{R_4}{R_3} I_{in}(t) & \text{For } I_{in}(t) < 0, \text{ N1:OFF, N2:ON} \end{cases} \quad (5.3)$$

$$I_{O-}(t) = \begin{cases} -g_m R_1 \frac{R_4}{R_3} I_{in}(t) & \text{For } I_{in}(t) > 0, \text{ N1:ON, N2:OFF} \\ -g_m(-R_2) \frac{R_4}{R_3} I_{in}(t) & \text{For } I_{in}(t) < 0, \text{ N1:OFF, N2:ON} \end{cases} \quad (5.4)$$



(a)



(b)

Fig. 5.6: (a) Proposed dual-output full-wave rectifier (b) MOS-based active resistor

Considering $R_1 = R_2 = R_{eq}$ by analysis of DDCCTA-based dual output FWR gives the following expression.

$$I_{O\pm}(t) = |g_m R_{eq} \frac{R_4}{R_3} |I_{in}(t)|| \quad (5.5)$$

Any mismatch between R_1 *and* R_2 can produce asymmetry in the rectified output, resulting in lower performance and possible distortion.

5.3.2.1 Effect of non-unity gains

The impact of the non-ideal effect of DDCCTA on proposed FWR may be examined by considering non-unity transfer gains and parasitics. In the presence of non-idealities on the port relation, where, β_1, β_2, *and* β_3 are non-ideal voltage-transfer gains from voltage *Y1, Y2, and Y3* to voltage X-terminal respectively. The α is the non-ideal current transfer gain from current X to current Z-terminal and the γ is the non-ideal trans-admittance transfer gain from voltage Z to current O-terminals. Considering $\beta_1=\beta_2=\beta$, the comprehensive transfer function:

$$I_{O\pm}(t) = |\alpha\beta\gamma g_m R_{eq} \frac{R_4}{R_3} |I_{in}(t)|| \tag{5.6}$$

Thus, the non-unity transfer gain changes the transfer function. It is deviation may be accommodated by adjusting g_m or electronically tunable resistors.

5.3.2.2 Effects of parasitic

The parasitics in DDCCTA appear at various ports and are summarized below:

- R_X is a parasitic resistance that occurs at X-terminal.
- $R_{Y1}//C_{Y1}$, $R_{Y2}//C_{Y2}$,and $R_{Y3}//C_{Y3}$ are parasitic impedances at *Y1, Y2, and Y3*-terminals respectively.
- $R_Z//C_Z$ is a parasitic impedance at Z-terminal.
- $R_O//C_O$ is a parasitic impedance at O-terminals.

The passive component values ranging from non-ideal parasite's resistances and capacitances can be improved and which modify R_i to Z_i are given:

$$Z_1 = R_1 // R_{Y1} // (1/sC_{Y1}) \tag{5.7}$$

$$Z_2 = R_2 // R_{Y2} // (1/sC_{Y2}) \tag{5.8}$$

$$Z_3 = R_3 + R_X \tag{5.9}$$

$$Z_4 = R_4 // R_Z // (1/sC_Z) \tag{5.10}$$

$$I_{O+}(s) = g_m\left(R1 // R_{Y1} // (1/sC_{Y1})\right)\frac{R4 // R_Z // (1/sC_Z)}{R3+R_X} I_{in}(s) \quad (5.11)$$

$$I_{O-}(s) = -g_m\left(R2 // R_{Y2} // (1/sC_{Y2})\right)\frac{R4 // R_Z // (1/sC_Z)}{R3+R_X} I_{in}(s) \quad (5.12)$$

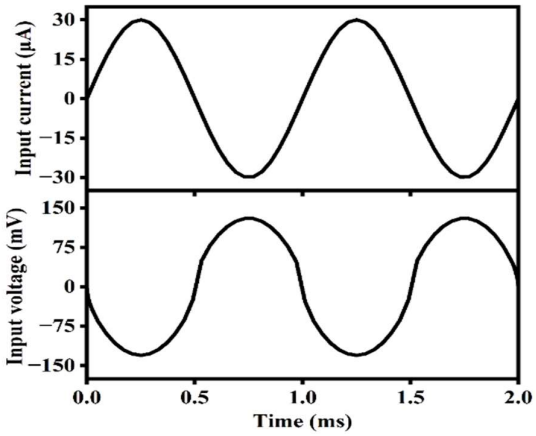
Assuming $Z_1 = Z_2 = Z_{eq}$, in the presence of parasitics, the transfer function:

$$I_{O\pm}(s) = |g_m Z_{eq}\frac{Z_4}{Z_3}|I_{in}(s)|| \quad (5.13)$$

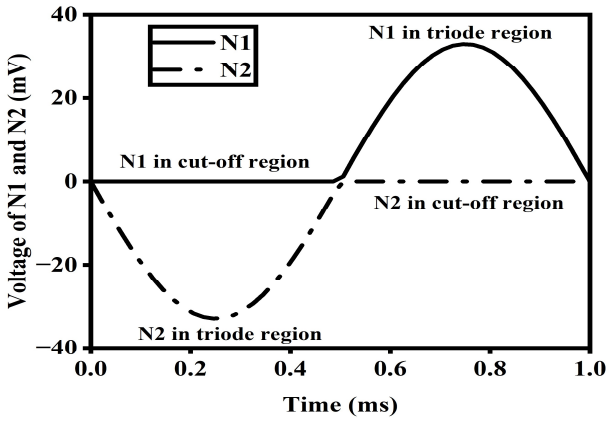
According to Eq. (5.7–5.12), the circuit performance would be partially deviated due to the parasitic resistances and capacitances. Furthermore, the X-terminal of the DDCCTA is connected by the resistor R_3; R_x is in series with R_3. As an outcome, the effect of this parasitic resistance may be accommodated by pre-adjusting R_3 value. The parasitic at Y ports (R_Y , C_Y) very high, 20 fF, Parasitic at Z ports (R_Z , C_Z) 218 kΩ, 35 fF, Parasitic at O− ports(R_{O-}, C_{O-}) 324 kΩ, 20 fF.

5.3.2.3 Simulation results

The proposed FWR is verified for functionality using the DDCCTA SPICE simulations are performed by using 180 nm TSMC CMOS technology. The supply voltages are taken $V_{DD} = V_{SS} = \pm 0.9$ V. The bias voltage V_{bias} and the bias current I_{bias} are taken as - 0.31 V and 50 µA respectively.



(a)



(b)

Fig. 5.7: (a) Input current and its corresponding input voltage (b) Mode of operations of NMOS-based diode

To understand the working principle of the proposed dual-outputs FWR, Fig. 5.7(a) shows the simulated voltage at the input terminal when current input is applied. For a positive half cycle, N1 is in the cut-off region and N2 is in the triode region. When the current input crosses zero and reaches the negative cycle, N1 enters the triode region while N2 enters the cut-off region. Fig. 5.7(b) depicts the mode of operations of N1 and N2. Further, to observe the dynamic range of the proposed FWR in Fig. 5.8, which ranges from -40µA to 40µA when the bias current is 50µA applied.

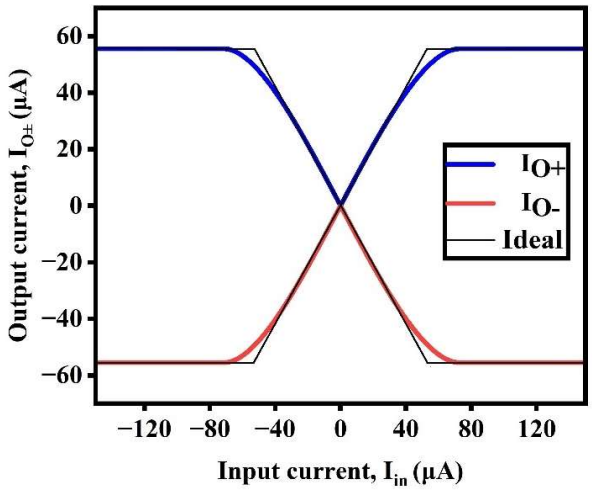
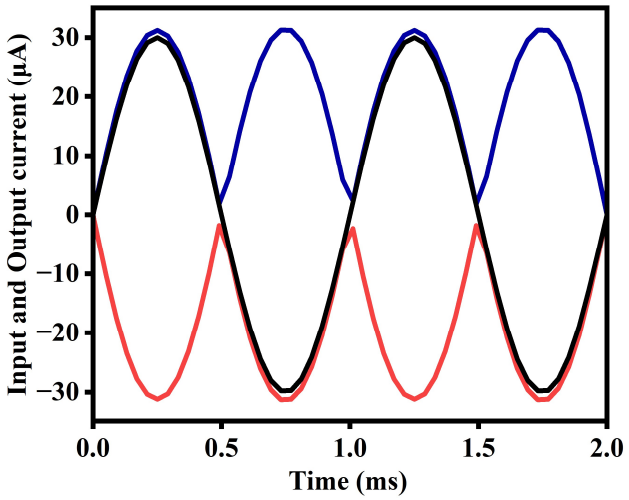


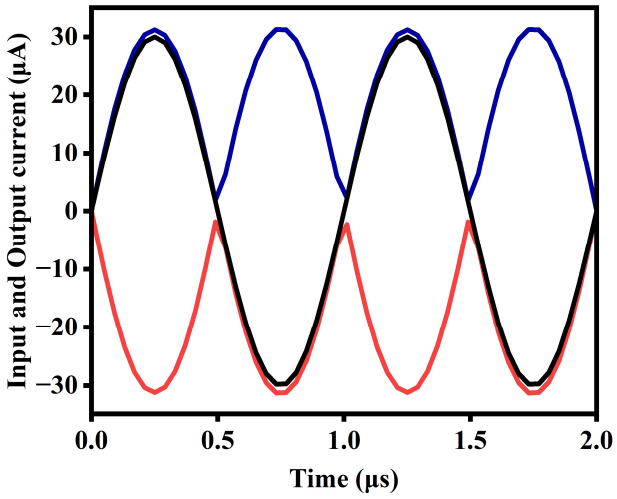
Fig. 5.8: DC response of proposed dual-outputs FWR

In Fig. 5.9, the output current variation is depicted at different operating input frequencies of 1 kHz, 1 MHz, and 10 MHz, using a sinusoidal input current of 30 µA. The output waveform of the proposed rectifier aligns excellently with theoretical expectations at low frequencies (kHz). However, at higher frequencies (MHz), amplitude errors between the input and output signals are observed, mainly due to the rectified low gain in these high-frequency operations. To address this issue, two potential solutions are identified. The first approach involves reducing the W/L ratio of M_1R_i and M_2R_i, thereby increasing the value of R_i to enhance the performance of the rectifier at higher frequencies. Alternatively, the second method entails augmenting the bias current (I_{bias}), leading to a simultaneous increase in the transconductance gain (g_m) of the OTA, which can help improve the capabilities of the rectifier at high frequencies.

We can observe the transient response of FWR in Fig. 5.10(a) with different input current amplitude values of 10 µA, 20 µA and 30 µA at 1 kHz, I_{bias} is 50 µA. The simulations are also performed to demonstrate the tunability of the proposed DDCCTA-based dual-output full-wave rectifier circuit. The input signal is a sinusoidal current signal with a frequency of 1 kHz and a peak value of 30 µA.



(a)



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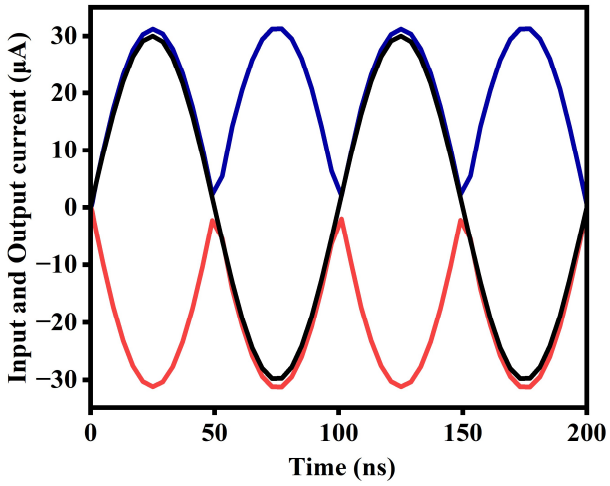
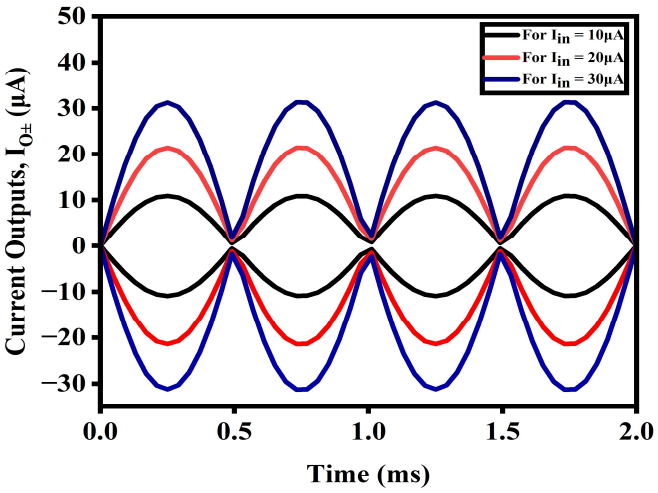


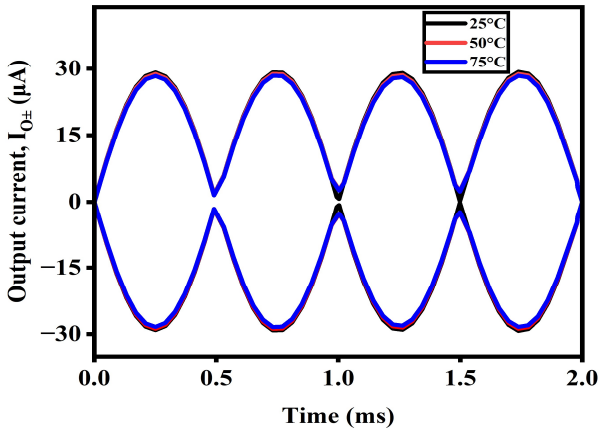
(c)

Fig. 5.9: Transient response of FWR at different frequencies (a) 1 kHz (b) 1MHz (c) 10MHz

To assess the temperature stability of the proposed rectifier, a 30 µA, 1 kHz signal was supplied into the circuit while the simulation temperatures have been varied between 25°C and 75°C. The output waveforms of the proposed rectifier are shown in Fig. 5.10(b) at different temperatures of 25°C, 50°C and 75°C. According to the outcomes, the proposed rectifier has quite good temperature stability.



(a)



(b)

Fig. 5.10: Transient response (a) with different current amplitudes (b) At the different temperature

The electronic tunability of FWR can be observed in Fig. 5.11, where the gain is controlled by bias current (I_{bias}) and the gain increases with an increase in bias current. On the other side, the gain is controlled by a varying control voltage (V_{C1} or V_{C2}) causing variation in values of MOS-based resistors R_1 or R_2 respectively while keeping R_3 and R_4 constant. If the resultant control voltage decreases, the value of the respective resistor increases, and the corresponding gain of the rectifier increases. The robustness of the proposed FWR against the aspect ratio of transistors M_1R_i and M_2R_i is examined through Monte Carlo simulation (MCS). The simulation is done for 100 runs by taking

the 2% Gauss deviation of threshold voltage (*Vth*) and 5% Gaussian deviation under excitation of an input current signal of 30 µA, 10 MHz and an I_{bias} of 50 µA.

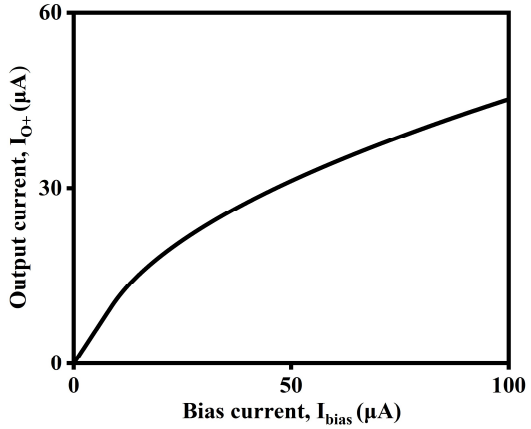
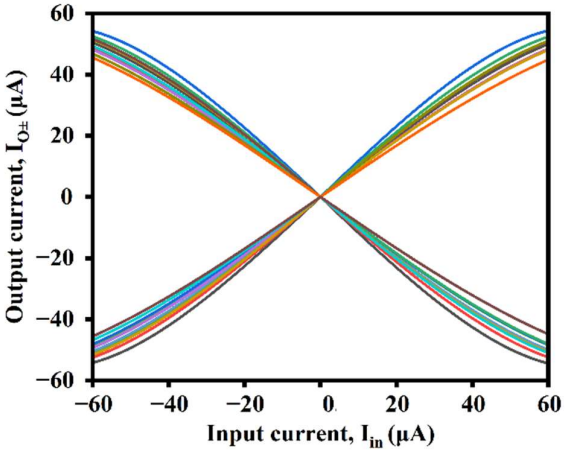
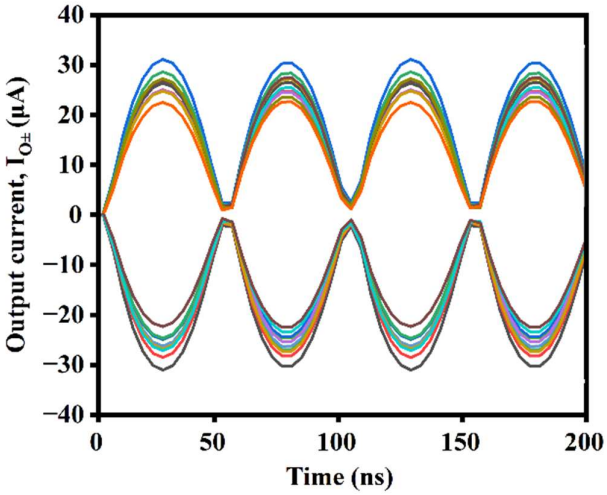


Fig. 5.11: Electronic tuning of rectifier gain through I_{bias}

In the DC characteristics, the percent of the maximum and minimum values that deviated from their nominal value are 112.5% and 95% respectively. In the transient response of the positive and negative rectifier, the percent of the maximum and minimum values that deviated from their nominal value is 100% and 66.67% respectively, are obtained in Fig. 5.12(a) and Fig. 5.12(b) respectively. The total power dissipation from the output window is 3.21mW. The output noise analysis is also performed and the equivalent output noises of the current mode at input operating frequency 10MHz are observed as 17.724 nV/ √Hz and 17.896 nV/ √Hz for positive and negative FWR respectively in Fig. 5.13.



(a)



(b)

Fig. 5.12: Monte-Carlo simulations (a) DC characteristics (b) Rectified output of Positive and Negative FWR

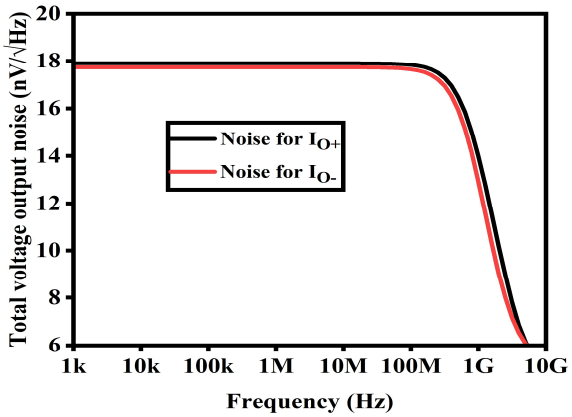
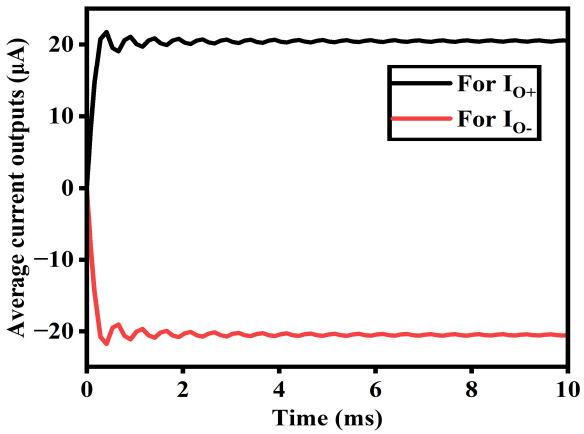
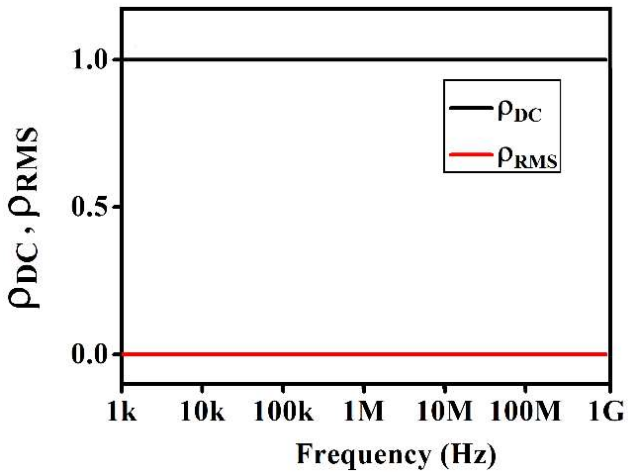


Fig. 5.13: Output voltage noise of proposed rectifiers



(a)



(b)

Fig. 5.14 (a) Dual phase positive (I_{O+}) and negative (I_{O-}) average DC current outputs (b) ρdc and ρrms versus frequency

The average DC outputs I_{O+} and I_{O-} of positive and negative FWRs respectively are shown in Fig. 5.14. The parameters DC value transfer (ρ_{DC})and RMS harmonic factor (ρ_{RMS}) are examined to get the rectifier accuracy mathematically as given expression in Eq. (5.14) and Eq. (5.15):

$$\rho_{DC} = \frac{\int I_{O,sim}(t)dt}{\int I_{O,th}(t)dt} \tag{5.14}$$

$$\rho_{RMS} = \sqrt{\frac{\int [I_{O,sim}(t) - I_{O,th}(t)]^2 dt}{\int I_{O,th}^2(t)dt}} \tag{5.15}$$

Where $I_{O,sim}$ is the simulated value of output and $I_{O,th}$ is the theoretical value of output. To check the frequency dependence of these parameters, a sinusoidal current input signal is applied to verify the effect of frequency variation on ρ_{DC} and ρ_{RMS} through simulations and plot is shown in Fig. 5.14(b). Ideally, the value of $\rho_{DC} = 1$ and $\rho_{RMS} = 0$.

5.4 Concluding remarks

The DDCC based current mode positive and negative types full-wave rectifiers are proposed. The proposed circuits consist of one single active building block, two MOS

based diodes and three grounded resistors suitable from the monolithic implementation point of view. The proposed circuit has a high impedance at the input terminal as well as an output terminal, so best from cascadability point of view. This circuit is useful for a higher frequency, low power consumption, low supply voltage, higher and wider input dynamic range. The PSPICE simulations have been performed using TSMC 180 nm CMOS technology parameters and the supply voltage of ± 0.9V. The full-wave rectifiers output can be achieved for the operating frequency of 200 MHz.

A current-mode dual output rectifier utilizing a single DDCCTA analog building block, two MOS-based diodes, and four MOS-based resistors. This rectifier can provide positive and negative dual outputs simultaneously without altering the topology. The rectifier operates efficiently at frequencies up to 10 MHz. The rectified outputs can be precisely adjusted through either the bias current (Ibias) or a control voltage (Vcj). One of its key advantages is its high output impedance, making it suitable for cascading and IC fabrication using CMOS technology. The proposed rectifier performs exceptionally well in key aspects such as output noise, input dynamic range, temperature stability, and robustness in Monte Carlo analysis. The theoretical proposal is well-supported by SPICE simulation results, utilizing the 0.18 μm technology.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

This thesis presents the design and implementation of novel circuits, including filters, controllers, wave active filters, and rectifiers, utilizing DDCC, DDCCTA, and EX-CCCCTA blocks. This newly developed current-mode (CM) building blocks combine the features of both current conveyors (CC) and operational transconductance amplifiers (OTA). This chapter provides an overview of the key conclusions drawn from the research conducted in the preceding chapters. Below, we summarize the main contributions of the thesis.

Chapter 1 of this thesis begins by discussing VLSI advancements in processing technology and their impact on circuit design. It provides a brief overview of the development of current-mode building blocks in analog circuit design. Additionally, it reviews the existing literature on filters, controllers, wave-active filters, and rectifiers. The chapter concludes with an outline of the thesis structure.

Chapter 2 provides a detailed study of the DDCC, DDCCTA, and EX-CCCCTA building blocks, analyzing their behavior under nonidealities and parasitic effects. The frequency response and current or voltage transfer characteristics are thoroughly validated through SPICE and Virtuoso simulations, confirming their performance and reliability for practical applications.

Chapter 3 presents a single DDCC-based MISO first-order universal filter using one resistor and one capacitor, capable of producing low-pass, high-pass, and all-pass responses from a single topology. The filter achieves a pole frequency (15.9 MHz), operates on a minimal voltage supply (±0.9V), and exhibits low power dissipation (2.94 mW), with theoretical results confirmed by SPICE simulations. Additionally, a TAM controller configuration is introduced, consisting of one DDCCTA, three grounded capacitors, and three passive resistors. The design supports PD, PI, and PID TAM operation without topology modifications, features electronic controllability ($g_{m1} = g_{m2} = g_{m3} = g_m$), and demonstrates low sensitivity, making it suitable for IC

implementation. The controller's proportional-integral-derivative gains, derivative time, and integral time constants are adjustable, with theoretical findings validated through Virtuoso simulations.

Chapter 4 introduces a novel wave-active nth-order low-pass Butterworth filter (n = 2, 3, 4, 5, 6) utilizing wave-active components (WACs) and elements (WAEs) based on DDCC. Key WACs, such as lossy integration-subtraction, subtraction, summation, and inverters, alongside WAEs like series inductors and shunt capacitors, form the foundation for realizing the filter. The design employs only grounded passive components, making it highly suitable for IC implementation, and operates effectively up to 10 MHz. The wave method is validated through SPICE simulations using 0.18 µm CMOS technology, achieving nth-order Butterworth low-pass responses. Additionally, an enhanced current-mode wave-active filter based on EX-CCCCTA is presented, offering wave equivalents for series inductors and shunt capacitors with a single EX-CCCCTA and grounded capacitor. This design features electronic tunability for adjusting the cutoff frequency, providing flexibility. For a 2nd-order Butterworth filter, key characteristics include two active building blocks (ABBs), an output noise level of 1.81 nV/Hz, and a power consumption of 2.01 mW. Simulated results align closely with theoretical predictions.

Chapter 5 proposes DDCC-based current-mode full-wave rectifiers, both positive and negative types in different topologies, designed with a single active building block, two MOS-based diodes, and three grounded resistors, making them suitable for monolithic implementation. The circuits feature high input and output impedance, enhancing cascadability, and are optimized for high-frequency operation, low power consumption, low supply voltage (±0.9V), and a wide input dynamic range. The simulations are achieving full-wave rectification at frequencies up to 200 MHz. Additionally, a current-mode dual-output rectifier is introduced, utilizing a single DDCCTA, two MOS-based diodes, and four MOS-based resistors. This design provides simultaneous positive and negative outputs without topology modification and operates efficiently up to 10 MHz. The rectified outputs can be adjusted via bias current or control voltage, and the high output impedance ensures suitability for

cascading and IC fabrication. The rectifier demonstrates excellent performance in terms of noise, dynamic range, temperature stability, and robustness, as validated by SPICE simulations with 0.18 μm CMOS technology.

6.2 Future scope

This thesis presents several novel analog circuit designs, including filters, controllers, wave active filters, and rectifiers, utilizing DDCC, DDCCTA, and EX-CCCCTA. However, the exploration of this class of circuits is far from complete. The research presented in this thesis can be extended in the following directions:

- Developing a memristor circuit using ABBs.
- Realization of an instrumental amplifier with CM, VM, TAM and TIM Topologies.
- Realizing capacitance multiplier circuits that employ a single ABB with a minimal number of resistors and a grounded capacitor.
- Implementing SIMO-type analog filters with single active and lesser passive components while fully utilizing all output terminals of the ABB.
- Designing a lossless grounded inductor using a single ABB, a single capacitor, and any number of resistors.
- Realizing floating impedances of various types using ABBs.
- Designing a single ABB-based quadrature sinusoidal oscillator with independent control over both CO and FO without requiring passive component matching.

In conclusion, the work presented in this thesis offers ample opportunities for further exploration and development.

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LIST OF PUBLICATIONS

List of journals:

1. S. Kumari and D. Nand, "Realization of *n*th Order Wave Active Low-Pass Filter Using Differential Difference Current Conveyor", *Journal of Circuits, Systems and Computers*, Vol. 33, No. 10, 2450180, (2024). https://doi.org/10.1142/S0218126624501809. **[World Scientific: SCIE Index- Online published]**

2. S. Kumari and D. Nand, "Simplified Wave Active Filter: A Novel design in current mode with single EX-CCCCTA", *Journal of Circuits, Systems and Computers*, Vol. 34, No. 04, 2550091 (2025). https://doi.org/10.1142/S0218126625500914. **[World Scientific: SCIE Index- Online published]**

3. S. Kumari, D. Nand and S. Kant, "MOS-based Electronically tunable current-mode dual-output full-wave rectifier using single DDCCTA", *Electrical Engineering Journal*, Vol. 107, 4203–4213 (2025). https://doi.org/10.1007/s00202-024-02736-7. **[Springer: SCIE Index- Online published]**

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1. S. Kumari and D. Nand, "DDCC-based MISO type voltage mode First-order Universal Filter," *2022 2nd International Conference on Intelligent Technologies (CONIT 2022)*, Hubli, India, 2022, pp. 1-6. https://doi.org/10.1109/CONIT55038.2022.9847828. **[IEEE: Scopus Index- Online published]**

2. S. Kumari and D. Nand, "Current mode Positive and Negative Rectifier based on DDCC suitable for Higher Frequency operations", *IOP Conference Series: Materials Science and Engineering, Volume 1084, First International Conference on Circuits, Signals, Systems and Securities (ICCSSS 2020)* 11th-12th December 2020, Tamil Nadu, India 1084 012079. https://doi.org/10.1088/1757-899X/1084/1/012079. **[IOP: Scopus Index- Online published]**

3. D. Nand and S. Kumari, "Implementation of TAM-Based Fundamental Analog and Arithmetic Operations Using DDCCTA," *2024 First International Conference for Women in Computing (InCoWoCo)*, Pune, India, 2024, pp. 1-5, doi: 10.1109/InCoWoCo64194.2024.10863706. **[IEEE: Scopus Index- Online published]**

Communicated:

1. S. Kumari and D. Nand, “Realization of TAM-based PD, PI, PID Controllers Utilizing a Single DDCCTA for Closed-Loop System Applications”, (2024). [Scopus Index-Communicated]

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