SELF-CONSISTENT LCAO-BASED DFT ANALYSIS OF FERROELECTRIC AND GATE MATERIAL ENGINEERED NEGATIVE CAPACITANCE FET FOR IMPROVED DEVICE-CIRCUIT PERFORMANCE

A Thesis Submitted
In Partial Fulfillment of the Requirements
for the degree of

DOCTOR OF PHILOSOPHY
by

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Dedicated to

My Parents

Mrs. Nirmla Devi

&

Mr. Roshan Mann

"All that I am, and all that I hope to be, I owe to my parent's love, guidance, and support"

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Through my PhD journey, I have learned patience, resilience, and the power of perseverance. I have grown not only as a researcher but as an individual, learning to embrace uncertainty and face challenges head-on. This experience taught me the value of failure—it is in the setbacks that I discovered my strengths and found new ways to approach problems. This journey would have been impossible without the love and support of those around me. My family stood by me, encouraging me when I felt discouraged. My friends offered laughter and perspective when I needed it most. The guidance and mentorship of my supervisor was contributory, not only in my academic development but in navigating the many challenges of the PhD process.

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CANDIDATE'S DECLARATION

I **Rashi Mann** hereby certify that the work which is being presented in the thesis entitled **SELF-CONSISTENT LCAO-BASED DFT ANALYSIS OF FERROELECTRIC AND GATE MATERIAL ENGINEERED NEGATIVE CAPACITANCE FET FOR IMPROVED DEVICE-CIRCUIT PERFORMANCE** in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the **Department of Applied Physics**, Delhi Technological University is an authentic record of my own work carried out during the period from _**2019**_ to **2025**__ under the supervision of **Prof. Rishu Chaujar**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

Signature of Supervisor (s) **Signature of External Examiner**

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CERTIFICATE BY THE SUPERVISOR(s)

This is to certify that the thesis titled "***Self-Consistent LCAO-based DFT Analysis of Ferroelectric and Gate Material Engineered Negative Capacitance FET for Improved Device-Circuit Performance***" is being submitted by ***Ms. Rashi Mann*** with registration number ***2K19/PHD/AP/05*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Physics. The work embodied in this thesis is a record of bonafide research work carried out by me in the Microelectronics Research Lab, Department of Applied Physics, Delhi Technological University (Formerly Delhi College of Engineering), New Delhi, under the guidance of ***Prof. Rishu Chaujar***. It is further certified that this work is original and has not been submitted in part or fully to any other University or Institute for the award of any degree or diploma.

Rashi Mann
Roll No.2K19/PHD/AP/05

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

Self-Consistent LCAO-based DFT Analysis of Ferroelectric and Gate Material Engineered Negative Capacitance FET for Improved Device-Circuit Performance

This thesis explores the challenges associated with Negative Capacitance Field-Effect Transistors (NCFETs), an emerging technology that promises to overcome traditional CMOS devices' fundamental power efficiency limitations. NCFETs, by utilizing a negative capacitance effect in ferroelectric materials, offer a solution for lowering subthreshold swing (SS) beyond the thermionic limit, thus reducing power consumption in next-generation transistors. This research systematically investigates these problems through simulation-based approaches. A detailed analysis of ferroelectric materials used in NCFETs, such as Hafnium-based oxides, is presented to identify performance degradation factors. The study also proposes optimized device architectures and material compositions to mitigate these effects. The findings contribute to understanding NCFET limitations and offer pathways for overcoming these barriers, providing insights for further research in low-power semiconductor technologies.

At this beginning, the effect of ferroelectric material on the substrate region is considered. The ferroelectric material is placed between the high-k HfO_2 layers in the conventional MOSFET's substrate, and this modified structure is termed FE-MOSFET. A study of the analog and RF parameters was investigated. The VISUAL TCAD simulator does all the simulation work. Then, the Quantum ATK simulator examines the reliability of silicon-doped HfO_2 as a ferroelectric material with different concentrations of silicon. The DFT analysis comparison of hafnia and 1Si-HfO_2 and 2Si-HfO_2 is done. DFT analysis contains the band structure and PDOS data corresponding to different materials. The effect of this 2Si-HfO_2 as a ferroelectric material is taken into account on the performance parameters of MOSFET, and the modified device with 2Si-HfO_2 as a ferroelectric in gate stack and high-k HfO_2 in substrate region is termed as Modified NCFET. Further, to ensure the device's

reliability, it is crucial to explore its characteristics, and the temperature variations taken into account. The performance parameter comparison of Modified NCFET is done with the conventional NCFET structure. Moreover, the impact of the high-k spacers on the analog/RF and inverter-based parameter performance of Gate-Stacked NCFET (Modified NCFET) is examined. Spacer materials are HfO_2, SiO_2, and helium (due to the unavailability of air molecule structure in the quantum ATK database, we investigate the structural properties of helium (k=1.000074 at 0^0 C and 1atm), which has nearly the same dielectric constant of air (k=1).) Self-consistent LCAO-based DFT analysis is done for the spacer materials regarding band structure, PDOS, and Hartree potential. Four configurations are simulated for this analysis, defined as GS-NCFET with no spacer (S0), GS-NCFET with AIR spacer (S1), GS-NCFET with SiO_2 spacer (S2), GS-NCFET with HfO_2 spacer (S3). After analyzing the electrical properties of the proposed device (GS-NCFET), the device modelling is done using the VISUALFAB simulator. The Cadence Virtuoso tool creates two symbols corresponding to N-GS-NCFET and P-GS-NCFET. Then, the digital application of GS-NCFET is shown as NAND, NOR, and NOT logic gates. It was found that the digital applications of GS-NCFET in terms of logic gates show the device is working properly with expected input-output curves.

Thus, GS-NCFET can be considered a promising candidate for use in low-power, analog, RF, and high-performance CMOS circuits due to its high switching ratio, lower leakage current, better reliability in terms of temperature, and superior static, analog, and RF performance, suppressed SCEs and parasitic capacitances.

PUBLICATIONS RESULTING FROM THIS THESIS WORK

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3. **R. Mann** and R. Chaujar, "DFT-based Atomic Modeling and Temperature Analysis on the RF and VTC curve of high-k dielectric layer-assisted NCFET," *Physica Scripta* vol. 99, pp. 015029, 2024. **(IF – 2.6)**
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2. **R. Mann,** R. Chaujar, "Electrostatic Analysis of Ferroelectric and High dielectric layer assisted MOSFET"**2021** ***7th International Conference on Signal Processing and Communication (ICSC),*** Noida, India, pp. 321-324, 2021, doi: 10.1109/ICSC53193.2021.9673258.
3. **R. Mann,** R. Chaujar, "Temperature Analysis on Short Channel Effects of Modified NCFET: A Simulation Study," ***8th International Conference on electronics, computing, and communication technologies, IEEE CONECCT***, Banglore, pp. 1-5, doi: 10.1109/CONECCT55679.2022.9865782, 2022.
4. **R. Mann**, R. Chaujar, "Impact of high-k spacers on the switching and VTC characteristics of Gate-Stacked NCFET," ***10th International Conference on 'Microelectronics, Circuits and Systems', MICRO2023,*** Assam, India, 2023.
5. **R. Mann,** R. Chaujar, "Impact of LCAO-DFT analysed Si-HfO_2 on GS-NCFET with its Digital Application," ***19th IEEE International Conference on 'Nano/Micro Engineered and Molecular Systems', NEMS2024***, Kyoto, Japan, pp. 1-4, 2024, doi: 10.1109/NEMS60219.2024.10639839.
6. Y. Pathak, **R. Mann**, B. D. Malhotra and R. Chaujar, "Impact of Temperature on

Negative Capacitance FET: A TCAD Simulation Study," ***2023 2nd Edition of IEEE Delhi Section Flagship Conference (DELCON)***, Rajpura, India, pp. 1-4, 2023, doi: 10.1109/DELCON57910.2023.10127565.

7. **R. Mann,** A. Narwal**,** R. Chaujar, "DFT based analysis of HfO2 layer assisted NCFET for Linearity Performance" ***2024 Asia-Pacific Microwave Conference, APMC 2024,*** Bali, Indonesia, 2024.

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CHAPTER

Introduction

- *This chapter presents a thorough background of the research work, emphasizing the importance of NCFET in the contemporary integrated circuit industry.*
- *Further, the chapter discusses the thesis objectives based on the background of MOSFET technology.*
- *Finally, the chapter provides an overview of the thesis research objectives, followed by a summary of all the chapters.*

1.1 BACKGROUND

In 1958, Jack Kilby, while employed at Texas Instruments, independently developed the concept of the integrated circuit (IC) [1]. Because of this innovation, it is now possible to fabricate several electronic components on a single semiconductor substrate, revolutionizing the electronics industry. On the other hand, Moore's law caused the CMOS technology to downscale, accelerating the development of ICs. The fact that a chip's transistor count doubles every two years is known as Moore's law, after one of Intel's co-founders, Gordon Moore [2]. This observation has been true for over 50 years, as shown by Figure 1.1, and has developed into a core idea in the semiconductor sector [3]. Transistors become smaller and more tightly packed on a single chip, which increases IC performance while lowering cost and power consumption. This trend has made it easier for a variety of electronic devices to be used widely, from cell phones and personal computers to cutting-edge medical technology and driverless cars. Our everyday lives have been miraculously changed by this amazing breakthrough in integrated circuit technology, and further device scaling is necessary to sustain further advancements in IC technology.

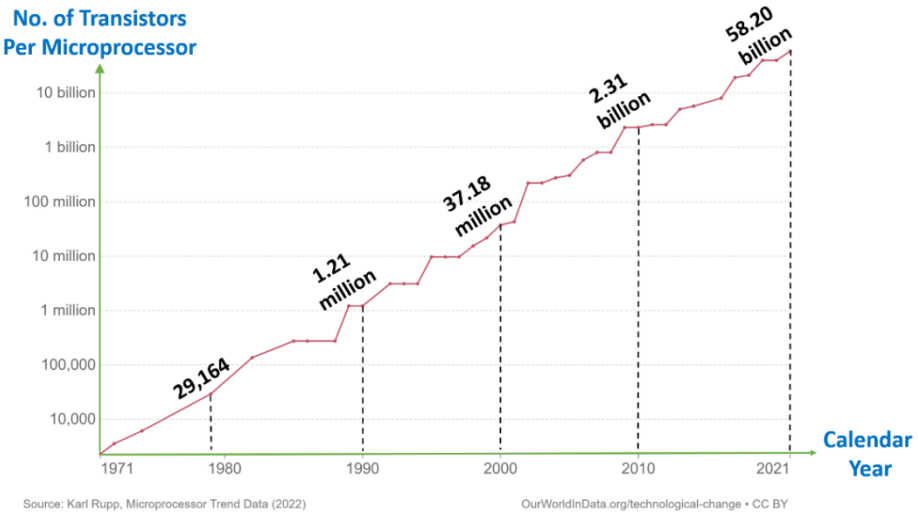

Figure 1.1: Log plot of transistor counts per microprocessor against calendar years [3].

However, maintaining this downscaling in the nanoscale region is challenging because of constraints including higher leakage current, higher power consumption, heat dissipation problems, quantum effects, and short-channel effects (SCEs) [4-6]. In deeply scaled MOSFETs, the drain potential starts to alter the channel's electrostatics, which raises the leakage current between the drain and the source. Furthermore, important SCEs that contribute to power loss in transistors include threshold voltage (V_{th}) roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope (SS) [7–10]. To mitigate these challenges, a variety of device topologies have been proposed, including multi-gate MOSFETs [11], TFETs [12], HEMTs [13, 14], FinFETs [15–17], and NCFETs. NCFET has emerged as the most desirable alternative to MOSFETs and is the driving force behind the current IC industry, which optimizes SCEs to achieve exceptional scalability, augment battery longevity, and minimize power consumption [18, 19].

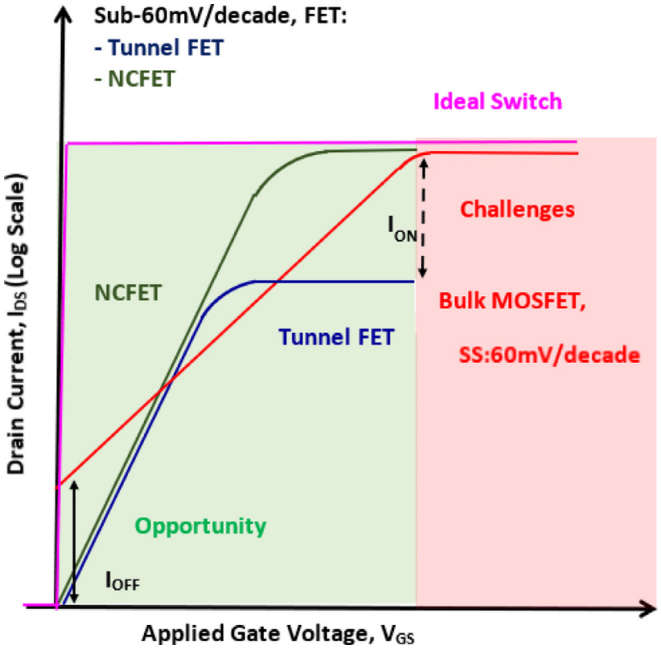

Figure 1.2: Expected steep slope less than 60 mV/dec at room temperature for an NC-FET [20].

Figure 1.2 demonstrates the performance of NCFETs over conventional planar MOSFETs. Leakage current and transistor gate delay have been reduced significantly for the NCFET structure over the planar MOSFET architecture [20]. NCFET ensures superior voltage

amplification with negative capacitance properties. Finally, NCFET offers a larger packing density. With a reduction in device dimensions according to Dennard scaling rules, the capacitances of the devices have reduced promising lesser power consumption. However, the supply voltage (V_D) could not be scaled according to the scaling rules, manifesting itself as a bottleneck in achieving high-speed low-power devices. This is because carriers in the source and drain region of the MOSFET are governed by Boltzmann statistics which limits the rate of increase of drain current for voltage to 60 mV/dec. In this Chapter, we give the thesis objectives, an overview of the thesis chapters, what are the research gaps after doing the literature survey and we explore the idea of negative capacitance in the gate stack of MOSFETs to overcome the Boltzmann limit (SS = 60 mV/dec) to realize high-frequency low-power devices. In this work, we did the step-by-step simulation work on the different architectures of NCFETs and explored the analog/RF parameters to discuss their further assessment of the digital circuits. Firstly, we explored the effect of the ferroelectric material layer as BOX in the substrate of conventional MOSFET and discussed its parameters. After that, the ferroelectric material in the gate stack with the dielectric layer in the substrate region as the BOX layer is explored termed as GS-NCFET, and compared with the conventional NCFET structures. Further, the temperature reliability and spacer's effects of GS-NCFET were discussed. Lastly, the simulated GS-NCFET is converted into the symbol using the VISUALFAB and cadence virtuoso simulator to explore its use in digital circuits like logic gates, amplifiers, etc.

1.2 THESIS OBJECTIVES

The entire work in the present thesis is divided into seven chapters based on the following objectives listed below:

1. To explore the TCAD investigation of ferroelectric-based substrate MOSFET for digital application.
2. To discuss the reliability of Si-doped HfO_2 by its DFT-based atomic calculation and the effect of its Negative Capacitance on SCEs, Analog/RF, and VTC parameters of MOSFET.
3. To explore the impact of temperature on the RF and VTC curve of high-k dielectric layer-assisted NCFET and to discuss DFT-based Atomic Modeling of hafnium oxide.
4. Self-Consistent LCAO-based DFT analysis of high-k spacers and to discuss its assessment on Gate-Stacked NCFET for improved device-circuit performance.
5. To discuss the device and circuit-level assessment of Gate-Stacked NCFET for digital applications.

1.3 SCHEME OF CHAPTERS

This thesis is organized into seven chapters to accommodate all the research objectives. Each chapter is organized to be fundamentally self-contained.

Chapter 1.Introduction

In this chapter, the general introduction to the theory of negative capacitance is discussed with a follow-up of the research objective and the overall organization of the thesis, as well as the importance of the research work presented in this thesis, are discussed.

Chapter 2.Literature Survey

This chapter overviews the basics of nanoscale MOSFET, scaling issues, and short-channel effects. After that, the ways to overcome the short-channel effects are discussed. In this regard, the different engineering schemes and the advanced FET structures, such as SOI MOSFET, FE-MOSFET, and NCFET, reported in different research articles, have been presented. Further, the research gaps found during the literature survey have been explored.

Then, the chapter progresses toward the architecture of NCFET, the basic working principle of NCFET, and its potential advantages and drawbacks.

Chapter 3.TCAD investigation of ferroelectric-based substrate MOSFET for digital application

This chapter presents an investigation on the analog/RF performance of ferroelectric (FE) based substrate metal oxide semiconductor field effect transistor (MOSFET) for digital application as an inverter. Short channel effect (SCEs) reduced significantly with improvement in switching ratio (I_{on}/I_{off}). The simulation shows the immunity towards parameters like transconductance (g_m), transconductance generation factor (TGF), early voltage (V_{EA}), and intrinsic gain (A_V) which allows the device to look into digital applications. Also, the RF performance parameters come out to be superior for the proposed device structure, as the gain frequency product (GFP) and gain bandwidth product (GBP) are enhanced by 100 and 10 folds, respectively. Further, RF investigation shows the enhanced results as attributed to peak values for transconductance frequency product (TFP) and gain transconductance frequency product (GTFP). The transient analysis shows an improvement in the noise margin (NM) for the FE-MOSFET structure. Thus, the proposed architecture can be an attractive alternative for the digital application.

Chapter 4.DFT-based Atomic Calculation of Si-doped HfO_2 and impact of Negative Capacitance on Analog/RF and VTC parameters of MOSFET

Execution grids of developing electronic devices are being examined to find substitutes for MOSFETs in the quest to minimize power dissipation and ease energy efficiency limitations. The innovative architecture of negative capacitance field effect transistors (NCFETs), which offer advantages from the design, performance, and fabrication perspectives, is presented and examined in this chapter. This proposed structure in this chapter is called Modified NCFET. Modification of NCFET includes the Density-

Functional-Theory (DFT) based atomic modelling for Ferroelectric material Hafnium Oxide (FE-HfO_2) with different doping concentrations of silicon (Si). The performance metrics of Modified NCFET are compared with conventional MOSFET designed on the same technology node to draw the effect of Si-doped HfO_2. DFT calculations like Projected Density of States (PDOS) and energy band structure are done using the Quantum Atomistix Tool Kit (ATK) simulator, which is atomic-scale modelling software, and device modelling is done by the Visual Technology-Computer-Aided-Design (TCAD) simulator. The device performance comparison of Modified NCFET and conventional MOSFET is made by the VISUAL TCAD in terms of short-channel effects (SCEs), analog/RF matrices, and FET-based inverter parameters (noise margin (NM), voltage transfer characteristics (VTC)). Additionally, the proposed NCFET is contrasted with the various FOMs' IRDS criteria.

Chapter 5.DFT-based Atomic Modeling and Temperature Analysis on the RF and VTC curve of high-k dielectric layer-assisted NCFET

In this chapter, Density Functional Theory (DFT) based calculation using a Quantum Atomistic Tool Kit (ATK) simulator is done for the hafnia-based ferroelectric material. The band structure, projected density of states (PDOS), and Hartree potential (V_H) are taken into account for hafnium oxide (HfO_2) and silicon-doped hafnium oxide (Si-doped HfO_2). Further, we analyze the temperature variation impact on analog parameters and voltage transfer characteristic (VTC) curve of inverter application of Modified Negative Capacitance Field-Effect-Transistor (NCFET) using the VISUAL Technology-Computer-Aided-Design (TCAD) simulator. The Modified NCFET structure enhances the DC parameters like leakage current (I_{OFF}) and Subthreshold Swing (SS) compared to the conventional NCFET structure. With the temperature impact, the variation in the parameters of Modified NCFET is discussed at 250 K, 275 K, 300 K, 325 K, and 350 K like transconductance (g_m), output conductance (g_d), early voltage (V_{EA}) shows the

increment as we move from 250 K to 350 K. The short channel effects (SCEs) like Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) decrease with the temperature fall at 32.98% and 34.74%, respectively. Further, the VTC curve, Noise Margin (NM), and propagation delay between the input and corresponding output curve of the Modified NCFET-based inverter are discussed, along with the impact of temperature. The propagation delay between the input and corresponding output curve of the Modified NCFET-based inverter for the circuit decreased by 67.94% with the rise in the temperature. These factors show that the Modified NCFET-based inverter provides fast switching performance at high temperatures.

Chapter 6. Self-Consistent LCAO based DFT analysis of high-k spacers on Gate-Stacked NCFET for improved device-circuit performance

This chapter investigates a Gate-Stacked negative capacitance field-effect transistor with a high dielectric material layer in the substrate region (GS-NCFET). Also, the effect of different types of spacers is taken into account. Spacers are differentiated based on their dielectric constant, i.e., GS-NCFET with no spacer is denoted as S_0, with air spacer is denoted as S_1, with SiO_2 specified as S_2, and with HfO_2 noted as S_3 device architecture. Self-consistent LCAO-based DFT analysis is done for the spacer materials in terms of band structure, PDOS, and Hartree potential. Further, the switching ratio (I_{on}/I_{off}) is discussed for S_0, S_1, S_2, and S_3. Further, the short channel effects (SCEs) like subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are extracted at drain-source voltage (V_{ds}) of 0.5 V. In addition, the voltage transfer characteristic (VTC) curve of GS-NCFET with a spacer-based inverter is considered for digital application purposes, and the transition region is drawn out for all the device architecture-based inverters. Essential parameters like propagation time delay between input and corresponding output curve of FET-based inverter and their rise/fall time are evaluated to study the application purposes. In GS-

NCFET, a dielectric layer, which is a buried oxide (BOX), is inserted in the substrate region to reduce the leakage current.

Chapter 7. Device and Circuit-level assessment of Gate Stacked NCFET for digital applications

The work demonstrates a Gate-Stacked Negative Capacitance Field Effect Transistor (GS-NCFET) study. NCFETs have become promising devices in the sub-nano-meter regime. The design possibility of NCFET is explored in this work, and the device modelling is done using the Verilog A code. We will start with the basic analog parameters like transfer characteristics, transconductance (g_m), and transconductance generation factor (TGF), with an improvement of 81.42% (leakage current), 9.97% and 21.54%, respectively, for GS-NCFET. Further, output characteristics and output conductance (g_d) showed a 17.85% decrease in GS-NCFET for the GS-NCFET. Also, the short channel effects for conventional NCFET and GS-NCFET are discussed. Moreover, the authors explored the device-to-circuit modelling using the Verilog A code, which uses the device parameter's "tbl" files. The symbols of N-GS-NCFET and P-GS-NCFET are generated using the Cadence Virtuoso simulator. Further, the digital application of GS-NCFET is shown as NAND, NOR, and NOT logic gates.

Chapter 8. Conclusion and Future Scope

This chapter summarizes the overall research work illustrated in this thesis, along with the concrete conclusions drawn from the results presented in this thesis. This chapter also discusses the future scope of the present work and how this work can be extended and used in future research directions.

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2

CHAPTER

Literature survey

- *This chapter presents a thorough literature survey of NCFETs, emphasizing their importance in the contemporary integrated circuit industry.*
- *The problems related to MOSFET scaling and the different short-channel effects have been comprehensively reviewed in this chapter.*
- *After that, this chapter encompasses an examination of several engineering methods, such as junctionless engineering, gate engineering, and dual-k spacer engineering, as well as advanced FET architectures, including SOI MOSFET, TFET, and CNTFET, as documented in different research publications, for mitigating short-channel effects.*
- *Furthermore, the chapter discusses NCFET as a potential approach to address the limitations. The chapter then progresses toward the fundamental architecture of NCFETs, categorization, basic working principles, possible benefits, and challenges confronted by NCFET technology.*
- *Finally, the research gaps and challenges faced by the NCFET technology is discussed.*

2.1 SCALING OF MOSFET

The development of MOSFETs dates back to the 1960s, with the invention of the first practical metal-oxide-semiconductor transistor by Mohamed Atalla and Dawon Kahng at Bell Labs in 1959. Early MOSFETs were relatively large by today's standards, with gate lengths (the distance between the source and drain under the gate electrode) measured in micrometers (μm). The first commercially viable MOSFETs had gate lengths on the order of 10 μm or more [1].

These early devices were suitable for use in logic circuits and basic memory applications. Still, their size limited the number of transistors that could be integrated onto a single chip, leading to relatively low computing power. The scaling of MOSFETs began in earnest in the 1970s, driven by the realization that reducing the size of transistors could improve performance and energy efficiency [2-6].

As transistors became smaller, they required less power to switch on and off, and they could operate at higher speeds due to the reduced parasitic capacitance and resistance associated with smaller geometries. This marked the beginning of the era of scaling, where each new generation of transistors was designed to be smaller, faster, and more power-efficient than the previous generation.

2.1.1 Dennard Scaling and the Golden Era

The early period of MOSFET scaling was largely guided by a principle known as Dennard scaling, proposed by IBM engineer Robert Dennard in 1974. Dennard's theory stated that as transistors were scaled down in size, their power density would remain constant as long as both the voltage and the current were scaled down proportionally [7-10]. This meant that as transistors got smaller, they would consume less power and produce less heat while switching faster, allowing for higher clock speeds in processors. For several decades,

MOSFET scaling followed this model, with chip manufacturers reducing the size of transistors while maintaining or improving their performance. Throughout the 1980s and 1990s, the semiconductor industry saw rapid improvements in MOSFET technology. Gate lengths shrank from micrometers to nanometers, with the 1 μm barrier being broken in the late 1980s. The transition from aluminium to copper interconnects in the late 1990s also helped reduce resistance and improve the overall speed of circuits, further enhancing the benefits of scaling.

During this time, MOSFET scaling was relatively straightforward, with each new generation of transistors offering better performance, lower power consumption, and increased transistor density. This period, often referred to as the "golden era" of Moore's Law, saw dramatic improvements in computing power and the proliferation of personal computers, mobile phones, and other electronic devices. By the early 2000s, however, the limits of classical MOSFET scaling began to emerge [11]. As gate lengths approached 100 nm and below, several issues became more pronounced, threatening to derail the continued progress predicted by Moore's Law.

- One of the most significant challenges was power dissipation. While Dennard's scaling suggested that power density would remain constant as transistors shrank, in reality, this assumption began to break down as transistors became extremely small.
- Another issue was short-channel effects, which occur when the channel length (the distance between the source and drain) becomes so short that the electric field from the drain begins to influence the behaviour of the channel. This can lead to threshold voltage roll-off, reduced gate control, and increased susceptibility to leakage currents, all of which degrade the performance of the transistor.

2.2 SHORT-CHANNEL EFFECTS

2.2.1 Drain-Induced Barrier Lowering (DIBL)

Drain-induced barrier Lowering (DIBL) is a short-channel effect in MOSFETs where the threshold voltage decreases as the drain voltage increases, as shown in **Figure 2.1**. This occurs because the electric field from the drain penetrates into the channel near the source, lowering the energy barrier for carriers to flow.

As a result, the gate loses some control over the channel, leading to increased leakage currents and degraded device performance [12]. DIBL becomes more pronounced as MOSFETs are scaled to smaller dimensions, negatively affecting power efficiency and off-state behaviour by allowing current to flow even when the device should be off [8,9].

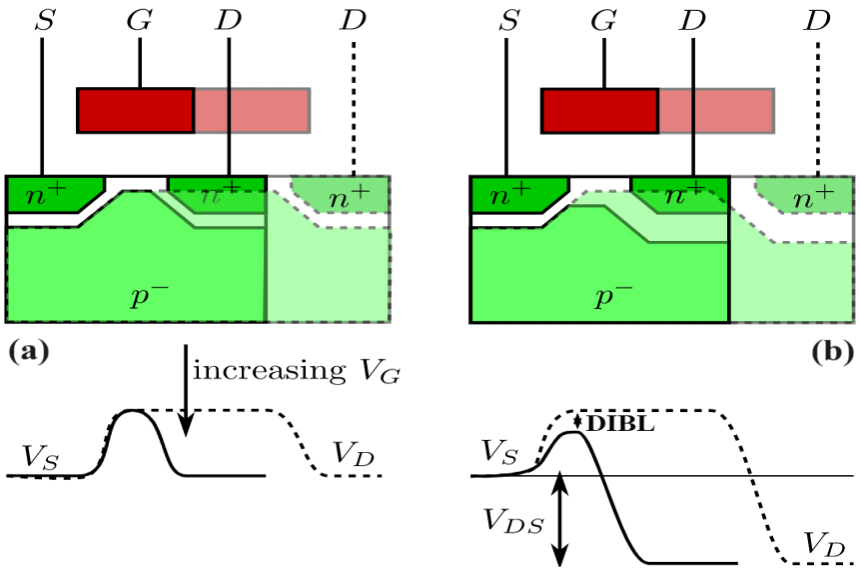

Figure 2.1: Drain-induced barrier lowering [11].

2.2.2 Surface Scattering

Surface scattering occurs in MOSFETs when charge carriers (electrons or holes) move through the channel and collide with the rough surface of the semiconductor-oxide interface expressed in **Figure 2.2**. As MOSFETs are scaled down and the channel becomes thinner, the influence of this surface becomes more pronounced. These collisions scatter the

carriers, reducing their mobility and leading to lower current drive and performance degradation [13]. Surface scattering becomes especially significant in short-channel devices, where the proximity of the channel to the surface is greater, making it a critical factor in limiting device speed and efficiency in advanced semiconductor technologies.

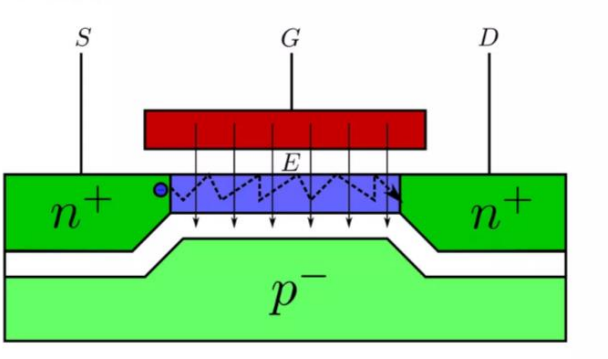

Figure 2.2: Surface Scattering [31].

2.2.3 Threshold Voltage (V_{th}) Roll-off

Threshold voltage roll-off is a short-channel effect in MOSFETs, where the threshold voltage (V_{th}) decreases as the channel length shrinks. In long-channel MOSFETs, the gate has strong control over the channel, keeping the threshold voltage stable. However, in short-channel devices, the electric fields from the drain and source influence the channel potential more significantly, weakening the gate's control. This causes the threshold voltage to decrease with reduced channel length, resulting in an earlier turn-on of the transistor and increased leakage currents. Threshold voltage roll-off negatively impacts performance and power efficiency in highly scaled devices **[14].**

2.2.4 Impact Ionization

Impact ionization occurs in MOSFETs when high electric fields, typically near the drain in short-channel devices, accelerate charge carriers (electrons or holes) to high velocities, as shown in **Figure 2.3.** These energetic carriers can collide with atoms in the semiconductor lattice, generating additional electron-hole pairs **[15].** This process results in an increase in

current beyond what is controlled by the gate voltage and can lead to several adverse effects, such as:

- **Increased leakage current:** Unwanted current due to the creation of extra charge carriers.
- **Hot carrier injection:** Damage to the gate oxide as high-energy carriers are injected into it.
- **Device reliability issues:** Long-term degradation of the MOSFET.

Impact ionization becomes more significant as MOSFETs are scaled down and electric fields intensify.

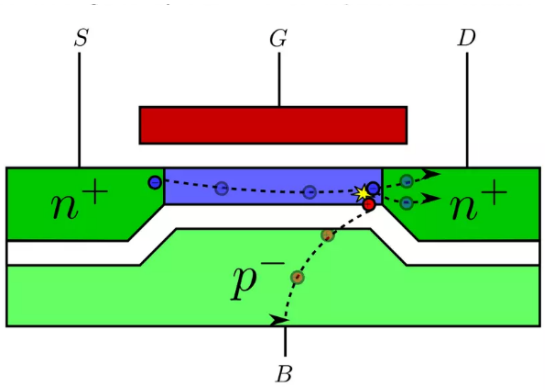

Figure 2.3: Impact Ionization [11].

2.2.5 Hot-Carrier Effects

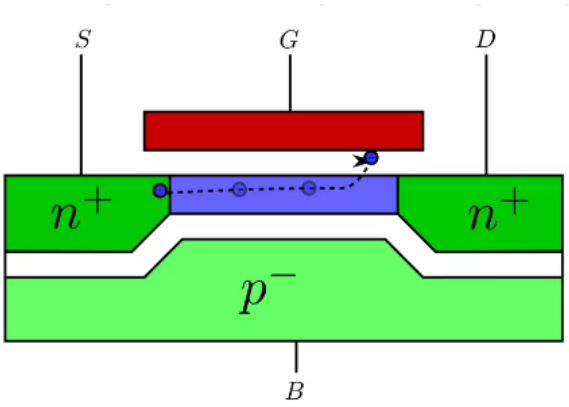

Figure 2.4: Hot Carrier Effects in NMOS [11].

The hot carrier effect in MOSFETs occurs when charge carriers (electrons or holes) gain significant kinetic energy from the electric field within the device, as shown in **Figure 2.4**. This energy can lead to carrier scattering, resulting in increased leakage currents and reduced device performance. As carriers are accelerated through the channel, they may gain enough energy to overcome potential barriers at the oxide-semiconductor interface, leading to impact ionization. This effect can cause device degradation, threshold voltage shifts, and eventual failure, particularly in high-frequency and high-power applications. To mitigate this, device design and fabrication techniques are employed to reduce electric fields and enhance reliability **[16].**

2.3 WAYS TO OVERCOME SHORT-CHANNEL EFFECTS

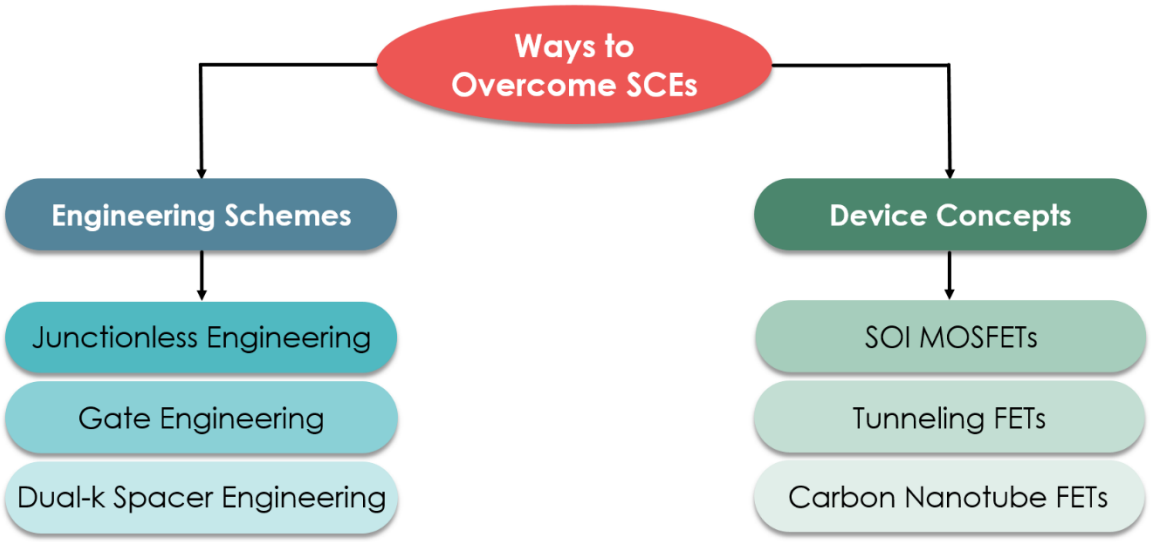

Figure 2.5: Different ways to overcome SCEs in nano-scale MOSFET.

These SCEs should be minimized or eliminated to preserve the electrical long-channel behavior of a physical short-channel device, given that they impede device operation and performance. Literature from recent years suggests that the use of novel device designs and engineering techniques (as presented in **Figure 2.5**) may diminish these short-channel effects.

2.3.1 Engineering Schemes

Researchers have developed various engineering schemes to mitigate the impact of SCEs on transistor performance. Here are some engineering schemes to address SCEs.

2.3.1.1 Junctionless Engineering

A junctionless field effect transistor (JLFET) is a transistor that functions in its channel area without a traditional p-n junction, as depicted in **Figure 2.6** [17]. They use a single-gated silicon nanowire structure instead. This nanowire serves as the current flow channel, and the gate terminal regulates the current flow by controlling the conductivity of the nanowire. When a positive gate voltage is applied, it draws negatively charged carriers (electrons) to the nanowire's surface, forming an accumulation region. This accumulation region improves the nanowire's conductivity, enabling current to pass between the source and drain terminals. When a negative gate voltage is supplied, the negatively charged carriers are repelled, resulting in a depletion zone at the nanowire's surface.

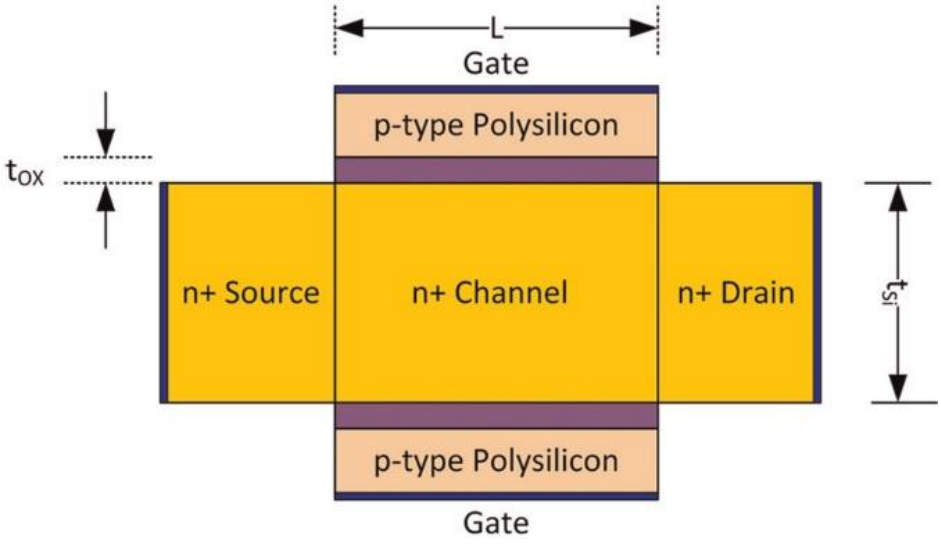

Figure 2.6: Cross-sectional view of junctionless double gate MOSFET [16].

The conductivity of the nanowire is reduced in this depletion zone, essentially limiting current passage between the source and drain terminals. This JL engineering has various benefits over conventional transistors, including easier manufacture, lower production

costs, lower leakage current, and higher energy efficiency. JLFETs alleviate the difficulties related to SCEs by removing the p-n junction, enabling additional scalability and performance benefits [18].

2.3.1.2 Gate Engineering

Long et al. [19] introduced the dual material gate (DMG) MOSFET in 1997, an innovative configuration that effectively mitigates SCEs while concurrently augmenting carrier velocity, as demonstrated in **Figure 2.7**. The gate of the DMG-MOSFET comprises two contacting materials with distinct work functions. The metal near the source has a larger work function, whereas the metal near the drain has a lower work function. Therefore, the threshold voltage $V_{th1} > V_{th2}$ enhances carrier transport efficiency. A metal gate with a lower work function in a DMG-MOSFET diminishes the electric field near the drain, suppressing hot-carrier effects even further. The fringing capacitance issue in DMG-MOSFET is also addressed because two gates are laterally linked into one single gate.

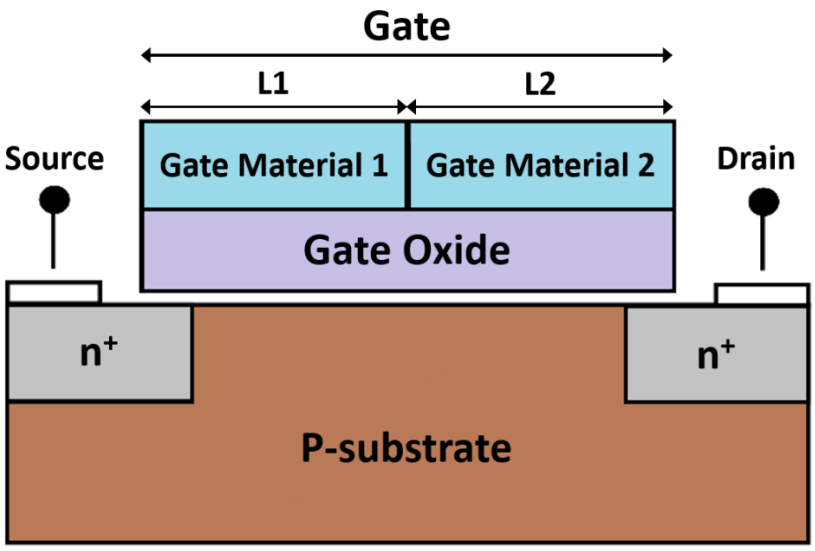

Figure 2.7: Schematic structure of dual material gate MOSFET [19].

2.3.1.3 Dual-k Spacer Engineering

Dual-k spacer engineering uses two dielectric materials with differing relative permittivity (k-values) to build spacers beside the transistor's gate electrode. **Figure 2.8** illustrates that dual-k Spacer engineering combines a high-k spacer on the inside and a low-k spacer on the outside to increase device performance and reduce SCEs [20]. For the inner layer, a high-k dielectric with a higher k-value than typical silicon dioxide (SiO_2) is placed because a high-k spacer enhances electrostatic control, minimizes SCEs, and improves transistor performance.

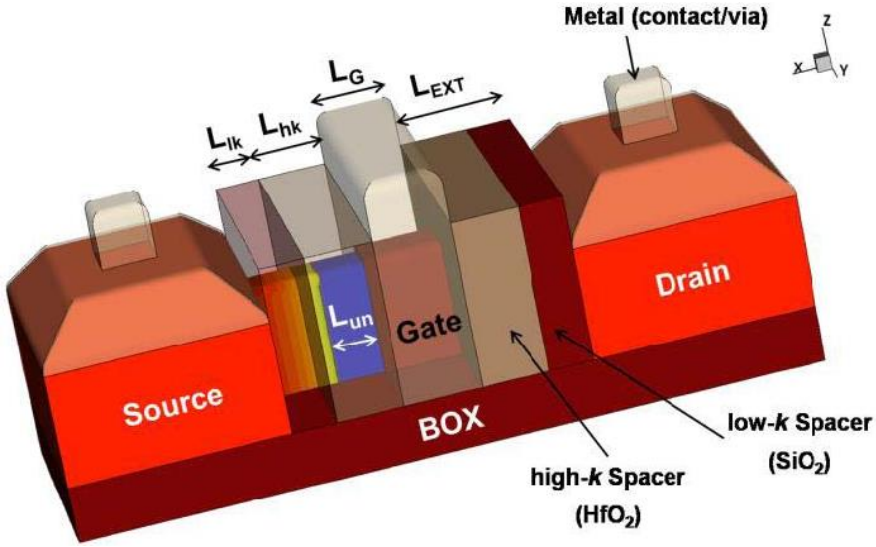

Figure 2.8: Schematic FinFET structure with dual-k underlap spacers [20].

Whereas for the outer layer, a low-k dielectric such as SiO_2 is considered because silicon in SiO_2 makes the silicon channel more flexible, reducing the likelihood of encountering dangling bonds and interface traps, and the low-k spacer reduces parasitic capacitance, minimizing the impact of capacitance and leakage current on transistor performance [21]. Thus, combining high-k and low-k spacers offers greater channel control, reduces SCEs and leakage current, increases threshold voltage stability, and improves overall transistor performance.

2.3.2 Device Concepts

Researchers globally are now working to advance the speed of operation and packing density of ICs by developing novel devices. Here are some devices to address SCEs.

2.3.2.1 Silicon-on-Insulator MOSFET

By sandwiching an entirely depleted silicon-on-insulator (SOI) device [22] between two connected gate electrodes, it is possible to substantially reduce SCEs. As illustrated in **Figure 2.9**, SOI technology utilizes a relatively thick silicon oxide layer to separate a thin silicon layer from a silicon substrate.

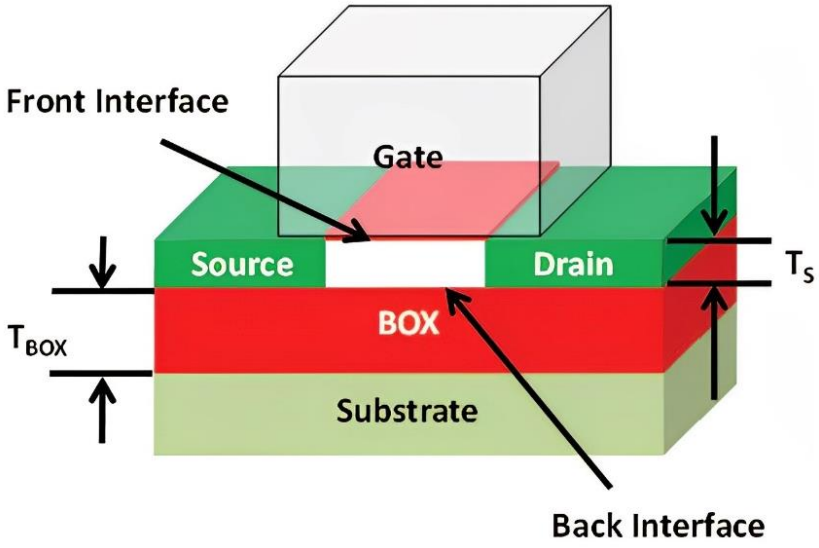

Figure 2.9: Schematic structure of FD-SOI MOSFET [22].

The SOI technology eliminates the possibility of latch-up failures by dielectrically isolating components and reducing various parasitic circuit capacitances in conjunction with lateral isolation. SOI technology provides devices that are exceptionally dense and radiation-resistant. The leakage current is negligible due to the absence of reverse-biased junctions utilized for isolation. Furthermore, the steeper sub-threshold slope of SOI devices makes them more suitable for scaling devices into the deep-submicron regime. This feature enables threshold voltage scaling, which is particularly advantageous for low-voltage, low-power applications. The SOI MOSFET is a highly desirable component for VLSI

applications requiring low power and high performance due to its minimal parasitic capacitances.

2.3.2.2 Tunneling Field Effect Transistor

Figure 2.10 exhibits a lateral structure view of tunnelling field effect transistors (TFETs), another intriguing alternative to traditional MOSFETs [23]. TFETs use the concept of band-to-band tunnelling, in which charge carriers use quantum mechanical phenomena to cross a potential barrier in a semiconductor material.

The capacity of TFETs to function at lower supply voltages is a significant benefit over MOSFETs. This is due to the sharp subthreshold swing characteristic of TFETs, which allows them to attain high on-state current while retaining low off-state leakage current [44].

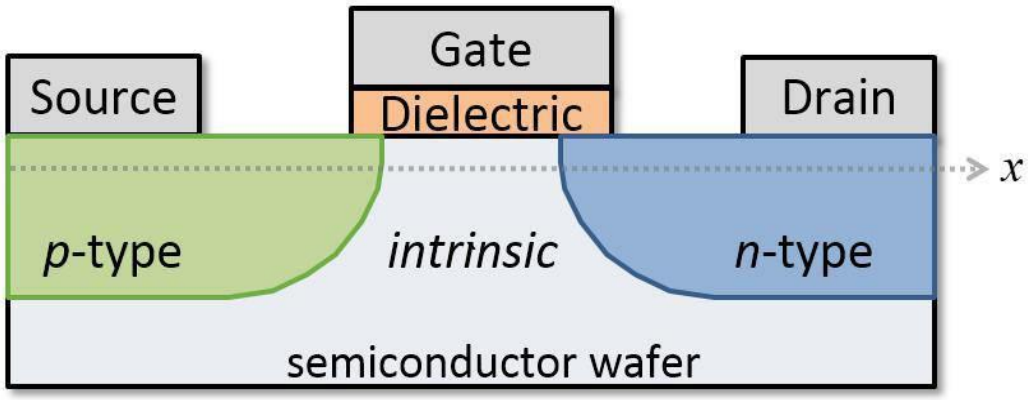

Figure 2.10: Schematic lateral structure of TFET [23].

As a consequence, TFETs have the potential to drastically lower IC power consumption. Another benefit of TFETs is that they are compatible with various semiconductor materials. This offers flexibility when developing TFET devices for multiple applications and performance requirements.

Nevertheless, TFETs encounter certain limitations compared to conventional MOSFETs: their generally lower current densities restrict their applicability in high-power scenarios. Furthermore, fabricating TFETs with the required precision is a substantial task.

2.3.2.3 Carbon Nanotube Field Effect Transistor

Carbon nanotube field effect transistors (CNTFETs) use carbon nanotubes as a conducting channel, as portrayed in **Figure 2.11** [25]. Carbon nanotubes are hexagonally latticed cylindrical structures made of carbon atoms. One of the most significant benefits of CNTFETs is their capacity to function at extremely small scales with reduced power consumption, thus enabling ultra-low-power operation. Furthermore, CNTFETs have high electron mobility, thermal conductivity, and mechanical strength [26]. These properties make CNTFETs capable of operating at high frequencies and high-speed switching applications such as data transmission systems. Another distinguishing aspect of CNTFETs is the ability of carbon nanotubes to be grown on flexible substrates, enabling the development of flexible and wearable electronics.

Despite these potential benefits, there are still hurdles that must be overcome before CNTFETs may be widely used. Controlling the chirality of carbon nanotubes during their production is one of the most challenging tasks. Scalability, device homogeneity, and contact resistance concerns must also be addressed to guarantee the practicality and economic feasibility of CNTFETs.

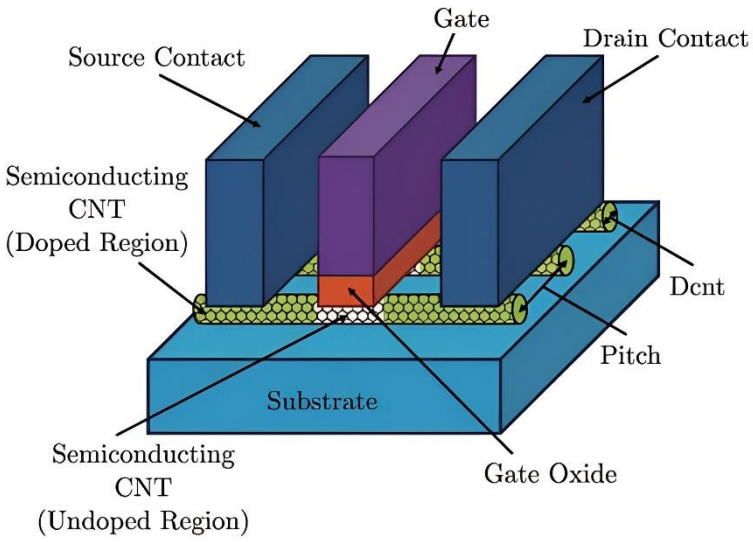

Figure 2.11: Schematic structure of CNTFET device [25].

2.4 RESEARCH GAPS

Research gaps identified after reviewing the literature are as follows, which will be attempted to address via possible solutions.

2.4.1.1 Need to make the device a more cost-effective solution, reduce the complexity of the fabrication process, and offer greater design flexibility.

2.4.1.2 The rise in off-state leakage current with the decreasing gate oxide thickness is another severe issue. This leakage results from quantum mechanical tunnelling, which limits the device scaling and negatively impacts the performance of the device.

2.4.1.3 Densely packed VLSI and ULSI circuits often run at high temperatures due to heat production, and excessive temperatures might harm or influence the functioning of the nanoscaled devices. Therefore, device reliability must be inspected to guarantee long-term endurance and stability.

2.4.1.4 The parasitic capacitance and short channel effects become more significant at the sub-nm range, deteriorating device performance. Thus, thoroughly examining these impacts is essential to improve the device's performance.

2.4.1.5 Due to their many benefits, FET-based electronic devices are widely utilized as bio-sensors, gas-sensors, radiation-sensors, etc. With the advancement of technology towards compact devices, there is a need for new FET-based sensors that cater to different specialized applications.

2.5 POSSIBLE SOLUTION – NCFET

2.5.1 Development and Prospects of NCFETs

Datta and Salahuddin [26] proposed the idea of negative capacitance MOSFETs to achieve SS < 60 mV/dec, wherein a ferroelectric insulator is used as a gate oxide and provides step-up voltage transformation. **Figures 2.12** and **2.13** represent the schematic of NC-FET and capacitive network in the NCFET structure. Further, they argued that for the system to be stable in its totality, the capacitance of the system should be positive.

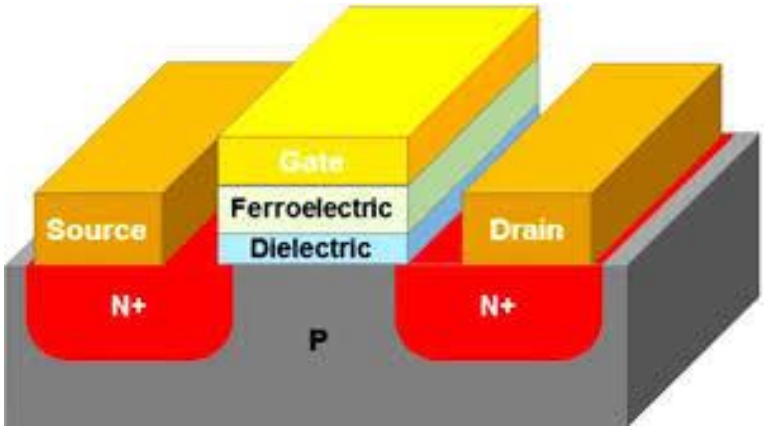

Figure 2.12: Schematic image of an NC-FET with ferroelectric and conventional dielectric as the gate stack [27].

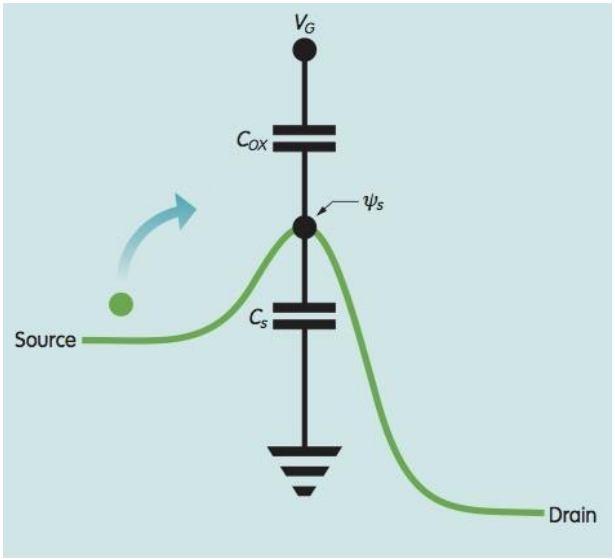

Figure 2.13: Gate is coupled to channel potential ψ_s by a capacitive network [28].

This poses a fundamental limit on the maximum thickness of the ferroelectric for hysteresis-free operation given by $t_{fe} < 1/2|\alpha|C_S$, where α is the material property of the ferroelectric and C_S is the semiconductor capacitance.

Design guidelines for designing NC-MOSFETs show that for stable operation, the total capacitance of the system should be positive, and hence, $C_S^{-1}(Q) > C_{Ox}^{-1}(Q)$ throughout the region of operation of the device. Further, for minimum coupling factor m, C_s, and ferroelectric capacitance $-C_{ox}$ should be as close as possible, since $m = (C_S^{-1} + C_{ox}^{-1})/C_S^{-1}$. In particular, the nanoelectromechanical switch (NEMS) with a suspended gate can also provide a negative capacitance effect, as shown in **Figure 2.14**. As the suspended gate is charged, it is attracted towards the MOSFET, and consequently, the voltage across it decreases. The NEMS switch can then be used in series with the ferroelectric capacitor to provide an ideal logic switch with SS = 0 mV/dec.

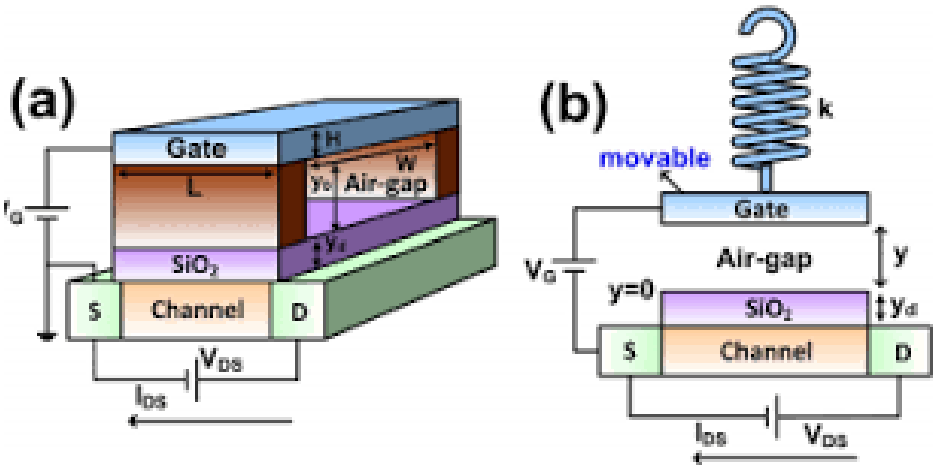

Figure 2.14: Suspended gate and ideal logic switch (a) suspended gate NCMOS with a nanomechanical spring (b)2D view of the suspended gate [29].

2.5.2 Experimental Evidence of Negative Capacitance

Experimental evidence of the NC mechanism was first provided by A. I. Khan and Salahuddin, shown in **Figure 2.15** [30]. In this experiment, they connected a series of ferroelectric capacitors with a high resistor. The flow of screening charges from a battery is then hindered by the resistance, and a transient negative capacitance is observed, where the charge across the ferroelectric decreases even though the voltage across it increases. Experimental evidence of FE-FinFETs has been discussed in [30]. In particular, in 1.5 nm thickness, HZO (Halfnium Zincronium Oxide) was used to achieve a subthreshold swing of about 52 mV/dec.

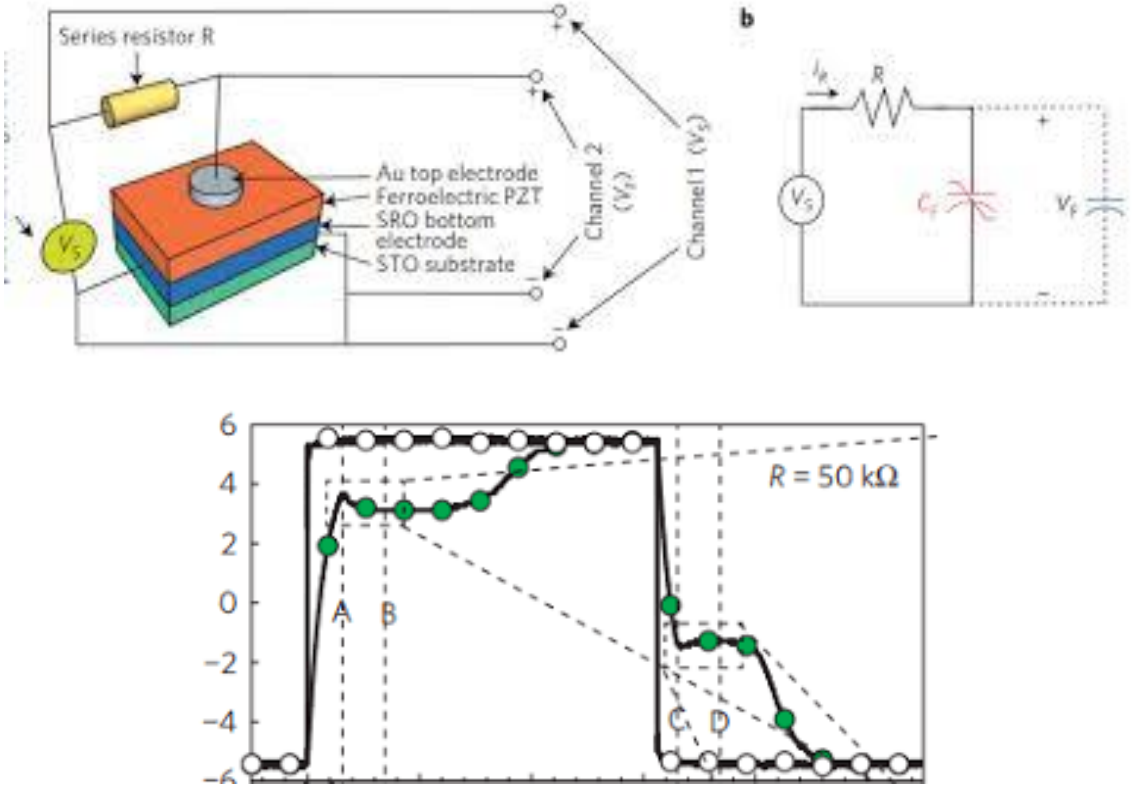

Figure 2.15: Verification of negative capacitance (a) Ferroelectric capacitor connected in series with a resistor to demonstrate NC effect (b) Resistance hinders the flow of screening charges, which results in a transient NC effect between points A and B [30].

2.5.3 NCFET Classification

Ferroelectric-based negative capacitance (NC) transistors, which can enable sub-60-mV/dec switching, are being actively researched for ultralow-power applications. The experimental demonstrations of NCFET have mainly employed two different types of NCFET structures, as shown in **Figure 2.16** [31]. One of the structures involves a metal layer (floating gate) between the ferroelectric and the internal gate oxide (a metal-ferroelectric-metal-insulator semiconductor (MFMIS) FET, as shown in **Figure 2.16(a).**

Each unit in the MFIS equivalent network represents an MFMIS structure. V_{int} denotes internal voltage at the ferroelectric–oxide interface represented in **Figure 2.16(c)**. For MFIS, V_{int} varies along the longitudinal direction when a nonzero drain bias is applied, and hence, it has been modelled by the arrangement shown in **Figure 2.16(d)**. In the other structure shown in **Figure 2.16(b),** the ferroelectric is in direct contact with the oxide layer (a metal-ferroelectric-insulator-semiconductor (MFIS) FET. Recently, Duarte et al. have reported that MFIS provides a higher ON-state current compared with MFMIS. However, we find this not to be true for all the ferroelectric materials.

In this part, an extensive one-to-one comparison between MFMIS and MFIS structures of NCFET using a compact modelling approach is discussed. It shows that the relative value of ON-current is a strong function of remnant polarization of the ferroelectric when comparing MFMIS and MFIS structures.

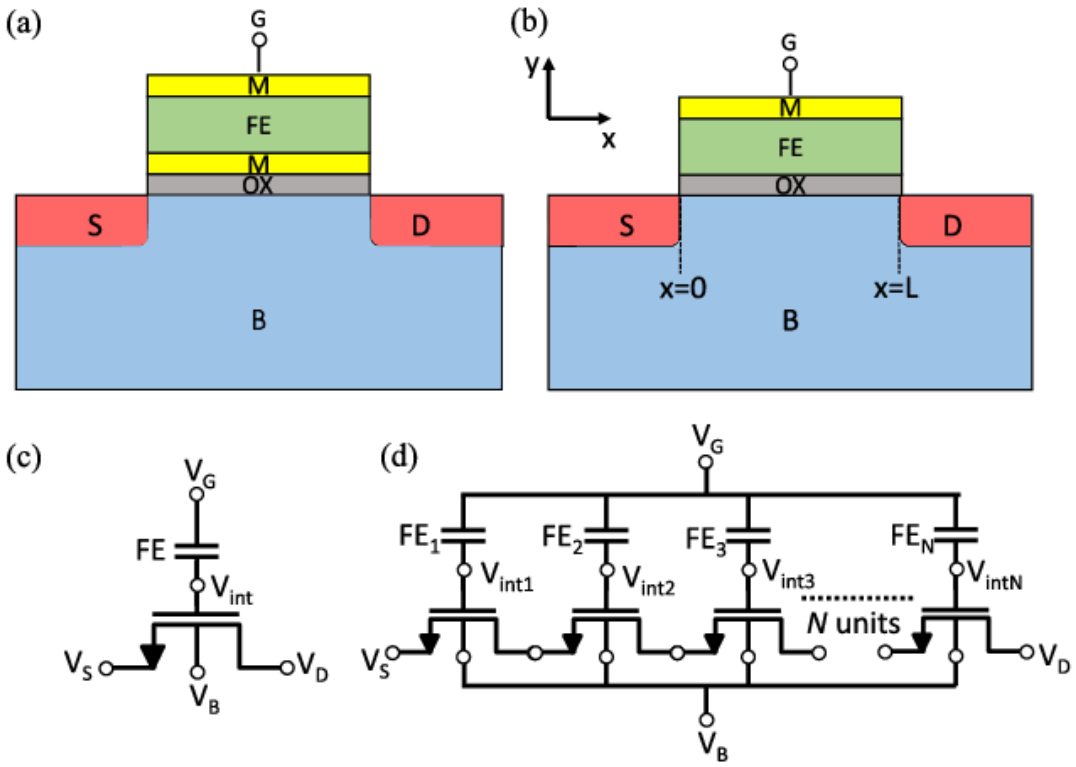

Figure 2.16: Structural comparison between (a) MFMIS and (b) MFIS, (c) MFMIS and (d) MFIS [31].

It also investigates and explains the hysteresis behaviour of the two structures, highlighting the differences in their underlying hysteresis mechanisms for the first time. A compact modelling approach is used to simulate the two types of NCFET structures. For MFMIS, due to the presence of a metal layer, the ferroelectric capacitor and the baseline MOSFET can be considered as two different circuit elements simply connected by a wire, as shown in **Figure 2.16(c).** The MFMIS structure can thus be simulated by a lumped model approach by self-consistently solving the Landau–Devonshire (L–D) model of the ferroelectric with the MOSFET physics, L–D equation relates the voltage drop across the ferroelectric, V_{fe} and the gate charge density, Q_G as $V_{fe} = 2\alpha Q_G + 4\beta Q_G{}^3$, where α and β are the material-dependent parameters. α and β can also be related to the ferroelectric material properties, the remnant polarization (P_r), and the coercive field (E_c) [31].

<u>Comparison of MFIS and MFMIS's transfer characteristics:</u>

ON Condition: $V_G > V_{th}$, V_D = '+' ve, $V_S = 0V$

As we apply a positive voltage to the gate terminal, due to the positivity of the gate and corresponding capacitive effect, minority charge carriers get attracted towards the gate and form a layer of uncovered ions there just below the dielectric layer. When the gate electrode is given a voltage higher than the threshold voltage, the region beneath the gate is inverted and forms a channel, providing a conducting path between the source and the drain. The current flows from the drain to the source in the channel.

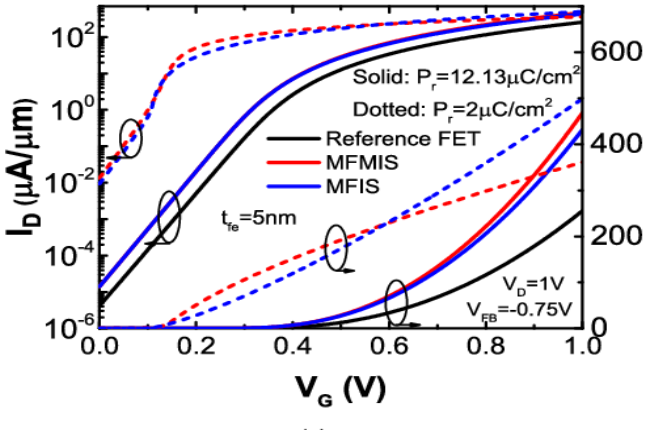

Figure 2.17: Comparison of I_D–V_G of MFMIS and MFIS NCFETs for different remnant polarization values [31].

MFMIS structure shows higher ON-current due to the internal voltage amplification caused by the NC effect, which is present even for $V_G = 0$ as the flat band voltage (V_{FB}) = 0 shown in **Figure 2.17**.

OFF Condition: $V_G < 0V$, V_D = '+' ve, $V_S = 0V$.

The transistor is in OFF condition, and there will be no current flow from drain to source in this state.

2.5.4 Advantages of NCFET

Modern semiconductor manufacturing foundries prefer NCFET technology over traditional planar transistor designs due to its several advantages.

- **Improved Performance:** NCFETs have enhanced electrical performance in comparison to planar transistors. These devices offer enhanced regulation of electron movement, leading to faster switching speeds and improved circuit performance.
- **Reduced Leakage Current:** The foremost benefit of NCFETs is their capacity to mitigate leakage current. When the transistor is not actively switching, the 3D fin structure provides greater control in the transistor's OFF state, lowering power usage.
- **Low Power Consumption:** NCFETs are ideal for applications where power consumption is of the utmost importance, such as mobile devices and IoT devices, due to their exceptional energy efficiency.
- **Scalability:** The scalability of NCFET technology enables its seamless integration into smaller technology nodes such as 15 nm, 10 nm, and beyond. NCFETs have been crucial in preserving Moore's law and enhancing transistor density as semiconductor manufacturers shift towards lower lithography nodes.
- **Improved Heat Dissipation:** The heat dissipation of NCFETs is also helped by their voltage amplification factor. The negative capacitance offered by the ferroelectric material helps in voltage amplification, hence mitigating the potential for overheating in high-performance microprocessors.
- **Better Control Over SCEs:** NCFETs provide superior control over SCEs, including drain-induced barrier lowering (DIBL) and subthreshold slope (SS) degradation, compared to planar transistors.

- **Compatibility:** The integration of NCFET technology into current semiconductor production processes can be facilitated by certain adjustments, simplifying the transition for semiconductor manufacturers towards adopting NCFET technology.
- **Industry Standard:** NCFET technology has emerged as a prevailing standard in advanced semiconductor fabrication, garnering widespread adoption by prominent semiconductor foundries. The extensive use of NCFET-based designs guarantees a diverse range of tools and specialized knowledge inside the ecosystem.

2.5.5 Challenges Confronted by NCFET on the Simulation Level

While NCFET technology offers numerous advantages, it also comes with some challenges. The challenges confronted by the NCFET technology are described as:

Computational Complexity: Coupling ferroelectric materials with conventional MOSFET models requires solving additional differential equations, increasing simulation complexity.

Convergence Issues: Numerical convergence issues arise in TCAD, SPICE, and quantum mechanical simulations, especially when modeling fast switching behavior.

Accurate Material Parameter Extraction: Simulations require precise input parameters like permittivity, polarization coefficients, and domain wall effects, which are often difficult to obtain experimentally. Variability in ferroelectric thickness, doping concentration, and interface properties adds uncertainty to simulation results.

Capturing Temperature and Scaling Effects: Ferroelectric properties vary with temperature, affecting device stability and requiring temperature-dependent modeling. Scaling NCFETs to smaller nodes introduces quantum effects, leakage currents, and variability, which are difficult to simulate accurately.

Reliability Concerns: The ongoing reduction in transistor sizes raises concerns regarding the long-term reliability of NCFET-based devices, such as electro-migration, aging effects, and overall device longevity[32].

By keeping these challenges in view, all the simulation is done on the VISUAL TCAD simulator. This simulator solves the additional differential equations that are required for the use of ferroelectric material in MOSFET architecture. The convergence errors were resolved by taking the fine meshing in the built architecture. Different thickness of ferroelectric material is considered to extract the most suitable results. Also, the temperature analysis is done to check the reliability of the proposed architecture of NCFET. The calibrated transfer characteristics of conventional MOSFET on the VISUAL TCAD simulator and experimental results.

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3

CHAPTER

TCAD investigation of Ferroelectric assisted substrate MOSFET for Digital Application

- *This chapter discusses the analog and RF performance of ferroelectric-assisted substrate MOSFET (FE-MOSFET) and its digital application.*
- *It is found that the switching ratio of the FE-MOSFET increased almost fifty-eight times, thereby improving the analog performance in terms of transconductance, transconductance generation factor, intrinsic gain, and early voltage compared to conventional MOSFET.*
- *The RF performance parameters like GTFP and GFP get enhanced by four decimal points and two decimal points, with an 11 times enhancement in TFP for FE-MOSFET configuration compared to conventional MOSFET due to enhanced value of g_m, TGF, and reduced values of SCEs.*
- *It is also analyzed that the proposed device with a ferroelectric layer-assisted substrate exhibits the most improved static performance compared to the conventional MOSFET configuration. Also, the inverter-based parameters like NM ratio are improved in the case of an FE-MOSFET-based inverter.*
- *Consequently, the proposed FE-MOSFET device with a ferroelectric layer as buried oxide would be an attractive solution for low-power and high-performance CMOS circuits.*

3.1 INTRODUCTION

The current increasing demand to follow the high-performance and ultra-low power circuits has motivated the semiconductor industry to downscale the transistors, as stated by Moore's law. However, with the following trend, CMOS technology is reaching its fundamental limits of scaling down [1-5]. As the size of the transistor scales down, the length of the channel in the device decreases, and the SCEs like channel tunnelling, drain-induced barrier lowering, and subthreshold swing value start dominating and affecting the device's performance. With scaling below 100 nm, the gate control over the device channel becomes poor, so the SCEs start to dominate. Another issue that the device's performance suffers from is the pin-point ultra-sharp S/D junction's formation. Some of these effects are reduced by junctionless field effect transistors in which doping species in all regions are the same. It also provides better protection against SCEs than conventional CMOS devices [6-10].

Another challenge with the decreasing size of the transistor comes from power dissipation. With the reduction of threshold voltage for the same device speed and increasing current exponentially, static power dissipation is a new objective set for transistors. It does not look easy to achieve both things with balance. Still, there is a possible way to maintain the stability between device performance and power dissipation, which is the subthreshold swing value of a device. It represents the amount of applied gate voltage that is required to change the current by one decade and is given by

$$SS = \frac{dlog_{10}I_D}{dV_{gs}} \quad (3.1)\ [11]$$

For a conventional MOSFET, the value of SS is ≥ 60mV/decade. From Equation (3.1), we can say that as the value of SS lowers, the needed applied gate voltage becomes less to switch on the transistor [11-12].

Furthermore, the next challenge is to increase the gate direct tunnelling by reducing gate oxide thickness, which decreases the leakage current. The technical solution for this situation is proved by using high-k dielectric materials like hafnium oxide (HfO_2) (k=25), which can be used in the gate stack of the transistor with a combination of silicon oxide (SiO_2) as the effective oxide thickness (EOT) stays constant. HfO_2 cannot be directly deposited on the Si substrate because it forms the oxide composites at the interface of the gate stack and substrate region, which offers resistance at the interface. So, to maintain the interface quality, HfO_2 is always deposited on top of SiO_2 in the gate stack of the transistor.

In the last several years, there has been a sufficient increase in demand for higher battery backup and portable electronic devices. In addition to the matchup, this demand, along with the addition of speed performance, has been followed by the concept of Moore's law for decades. With the help of this system-on-chip (SoC) concept, we can integrate several independent systems on a single chip. The main challenge in SoC technology is device optimization.

In the past, using ferroelectric material in the gate stack of MOSFET gave better immunity to the device performance because FE material shows the behaviour of negative capacitance, which can be observed from their charge energy curve. So, we can use ferroelectric materials in many possible ways to redefine the architecture of existing MOSFET structures. A suitable example of FE materials is HfO2-based FE (HfO_2FE). We know that HfO_2 is a high-k dielectric material, but its properties show ferroelectric behaviour when it is deposited with chemical vapour deposition.

The use of ferroelectric materials in the substrate for spacer-based FE MOSFETs has an advantage that significantly affects their performance because these materials have the unique property of exhibiting spontaneous polarization, creating a built-in electric field in the channel region of the MOSFET, which results in a reduction in the threshold voltage

(V_{th}) and an improvement in the transconductance (g_m) of the device, which improves the overall performance. The fast polarization switching of ferroelectric materials gives ferroelectric MOSFETs the ability to operate at high speeds.

As a result, they are well suited for use in signal processing circuits, high-speed data transmission systems, and high-frequency RF (radio frequency) devices, all of which require fast switching. The charge energy curve of the FE Material has negative capacitance properties that allow it to be used in gate barrier materials when designing MOSFETs, providing enhanced current, reduced leakage current, and ratio high-speed switching as well as the sub-threshold slope (SS).

The ferroelectric properties of HfO_2 are still subject to investigation, and further studies are needed to understand their properties and potential applications fully. Therefore, when the device is combined with Gate stacks, pads of FE materials become capable of storing large amounts of charge, which can be used for digital, analog/RF applications [12]. In this chapter, we present a new MOSFET architecture that combines a ferroelectric material sandwiched between a high-K dielectric material in the base area and an HfO2 gate compartment used with SiO_2 and is called Ferroelectric assisted substrate MOSFET (FE-MOSFET). Thus, anticipating the combined advantages of the ferroelectric layer with the high-k dielectric layer in the substrate region and gate oxide combination for improved device characteristics, E-mode FE-MOSFET is analyzed and improved accordingly throughout the thesis. The following outline constitutes this chapter's structure: The first section of this chapter provides an overview of the device construction, along with the structural parameters and computational models that were applied throughout this study. The confirmation of the simulation setup is demonstrated in the second portion of the chapter, which details how the models used in the simulation setup were calibrated with the experimental data provided and how this was accomplished. In the following section of

the chapter, the manufacturing possibility of the suggested device will be discussed. The later part of the chapter discusses the results obtained through simulation. These results include the effect of gate and drain bias and the impact of high k gate dielectric; all of these factors affect the electrical and RF performance of E-mode FE-MOSFET. The conclusion of the chapter is presented in the final part of the chapter's summary. Thus, by considering all the conceptions, we designed a new architecture of MOSFET in which we use a ferroelectric material (HfO_2FE) sandwiched in between the high-k dielectric material HfO_2 in the substrate region with the addition of HfO_2 in the gate stack of the device. We named it a ferroelectric-assisted substrate metal-oxide-semiconductor-field-effect-transistor (FE-MOSFET), as shown in **Figure 3.1**[12]. Accordingly, the primary objective of this chapter is to include the ferroelectric layer with a combination of high-k dielectric layer and gate oxide into a single MOSFET. This chapter discusses the ferroelectric layer-assisted substrate MOSFET to acquire an improved device DC and RF performance. These advancements have enhanced the transistor's operational efficiency and opened up new possibilities for various applications in the field of electronics.

3.2 DEVICE DESIGN AND PHYSICAL MODELS

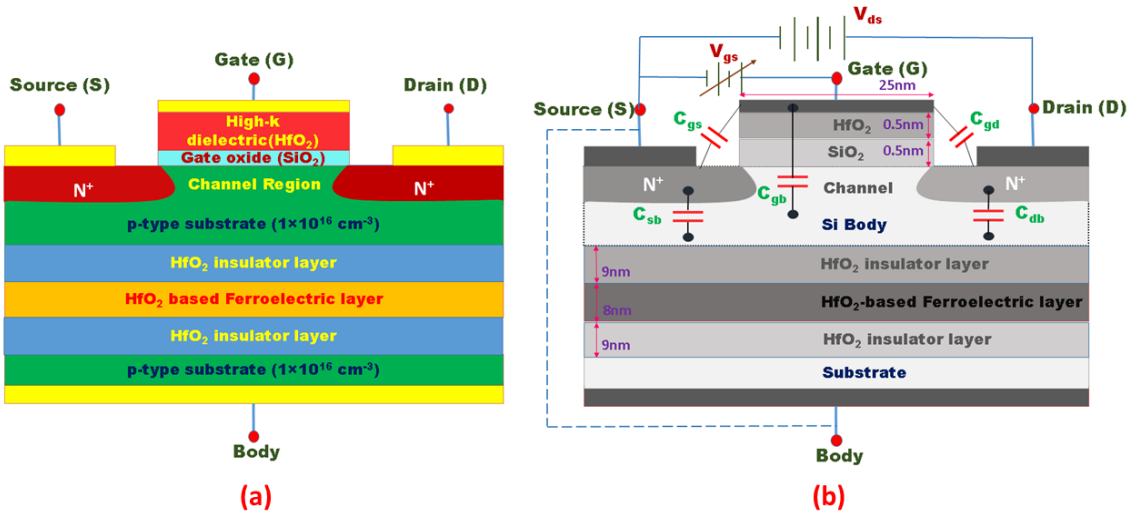

Figure 3.1: (a) Proposed FE-MOSFET structure, (b) Cross-section view and capacitance representation of the device [12].

For a fair comparison, the parameters such as device size, doping profiles, gate work function, etc., are maintained constant for both devices. The distinction is that while SiO_2 is the only gate oxide utilized in the other device, HfO_2 (k = 25) and SiO_2 (k = 3.9) are considered equally in the FE-MOSFET device. Additionally, a combination of insulator and ferroelectric with respective thicknesses of 9 nm and 8 nm is employed in the substrate region. The device's gate length (L_g) is 25 nm, while the S/D regions' ($L_{S/D}$) fixed length is 10 nm. Both devices maintain a constant tox of 1 nm. P-type doping species are equally doped throughout the substrate region. With n-type Gaussian doping, the doping concentration in the source/drain areas ($N_{S/D}$) is 1×10^{19} cm^{-3}, whereas in the channel region (N_{Ch}), it is 1×10^{16} cm^{-3}. The ion-implantation method, a very high-temperature annealing procedure, is used to construct the source and drain region. Metal would melt if it were used as a gate. One of the reasons offered to support the use of polysilicon over metal is its greater melting point. The gate N-Poly-Silicon (N-Poly-Si) has a work function (ϕ_m) of 4.50 eV. It is used because of its high purity, low resistivity, low thermal stability, and compatibility with CMOS processing. The temperature (T) is maintained at 300 K, and

gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) are altered from 0 V to 1.0 V and 0 V to 0.5 V, respectively. In Table 3.1, all the device parameters are tabulated.

Also, silicon material is used as the substrate region for both devices. The following factors make single-crystal silicon a better device substrate material: Its melting temperature is extremely high, approximately 1400 °C [17-19]. It is Young's modulus is comparable to steel's (about 200 GPa), as light as aluminium, and has excellent mechanical stability. Its thermal expansion coefficient is lower than steel and aluminium; its melting point is about double that of aluminium, and its production procedures utilizing silicon substrates are advanced and well-established.

Table 3.1: Different device configurations used for simulation [12].

Parameter	**Conventional MOSFET**	**FE-MOSFET**
L_g (nm)	25	25
$L_{S/D}$ (nm)	10	10
T_{ox} (nm)	1	1(0.5 SiO_2+0.5 HfO_2)
T_{FE} (nm)	0	8
T_{ins} (nm)	0	9
$N_{S/D}$ (cm^{-3})	1×10^{19}	1×10^{19}
N_{ch} (cm^{-3})	1×10^{16}	1×10^{16}
Φ_m (eV)	4.5(Npoly Si)	4.5 (Npoly Si)

The VISUAL TCAD simulator has simulated both configurations. For error-free and useful findings, alternative equations are necessary in addition to Poisson and Continuity equations. Equations (3.2-3.6) are used to describe a range of physical models included in the device simulation.

1. **Shockley-Read-Hall (SRH) recombination model** includes the effect of recombination and generation.

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{E_{Trap}}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-E_{Trap}}{kT_L}\right)\right]} \quad (3.2)\ [13]$$

where T_L is the lattice temperature, E_{TRAP} is the difference between the intrinsic Fermi level and trap energy level, k is the Boltzmann's constant, and τ_n and τ_p stand for the electron and hole lifetimes.

2. **Arora analytical model** correlates the low-field carrier mobility with impurity concentration and temperature.

$$\mu_n = 88\left(\frac{T_L}{300}\right)^{-0.57} + \frac{1252\left(\frac{T_L}{300}\right)^{-2.33}}{1 + \frac{N}{1.432\times10^{17}\left(\frac{T_L}{300}\right)^{2.546}}} \quad (3.3)\ [14]$$

where N is the total local dopant concentration, and T_L is the lattice temperature.

3. **Klaassen band-to-band tunneling model** accounts for the electrons tunneling between the valence and conduction band.

$$G_{BBT} = D \times BB.A \times E^{BB.GAMMA}\exp\left(-\frac{BB.B}{E}\right) \quad (3.4)\ [15]$$

where E signifies the electric field magnitude, D denotes the statistical factor, and BB.A, BB.B, BB.GAMMA are user-definable parameters.

4. **Crowell-Sze impact ionization model** introduces the impact ionization effects.

$$\alpha_{n,p} = \frac{1}{\lambda}\exp[C_0(r) + C_1(r)x + C_2(r)x^2] \quad (3.5)\ [16]$$

where λ denotes the carrier mean free path for optical phonon generation and $C_0(r)$, $C_1(r)$, and $C_2(r)$ are the ionization coefficients.

5. **Fermi-Dirac statistics model** enhances the result accuracy.

$$f(\varepsilon) = \frac{1}{1 + \exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \quad (3.6)\ [17]$$

where E_F indicates the Fermi level and ε is the energy of the available electron state. Additionally, Newton and Gummel's methods are used to achieve a solution.

3.3 CALIBRATION

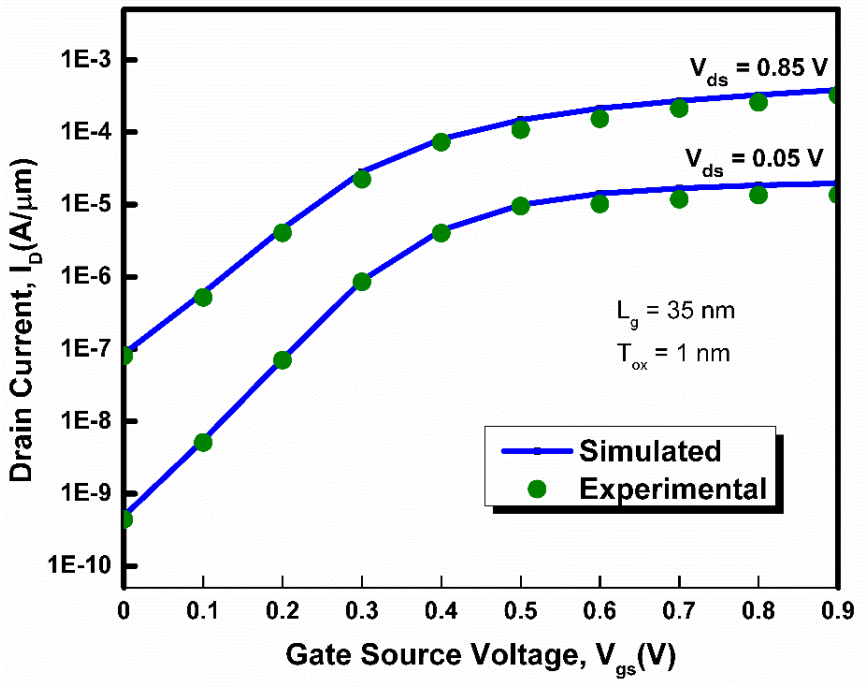

Figure 3.2: Calibrated Experimental and simulated transfer characteristics of the MOSFET [12].

Since experimental or simulated data for NCFET at the 25 nm technology node is not readily available in the literature, we performed a calibration using a conventional 30 nm MOSFET model in the simulator. This calibration process ensures that the baseline device characteristics align with reported results for short-channel MOSFETs, allowing us to extend the study toward NCFET behavior. The calibrated 30 nm MOSFET serves as a reference point to assess the impact of negative capacitance integration at scaled dimensions. The MOSFET is calibrated with the experimental data extracted from G. Roy et al. [20] to validate the above-discussed physical models on the VISUAL TCAD simulator. As mentioned in the paper, the experimental data is calibrated by considering silicon material in the entire substrate region with a fixed device dimension (Lg = 35 nm) to authenticate the simulations.

Figure 3.2 describes the MOSFET's experimental and simulated transfer characteristics at constant V_{ds} of 50 mV and 850 mV. The selection of simulation models is validated due to the close agreement between the experimental and simulated data sets.

3.4 FABRICATION FEASIBILITY

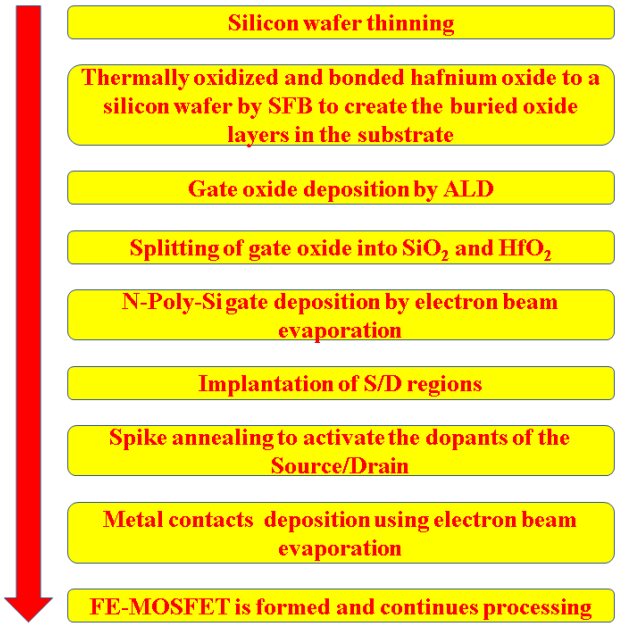

Figure 3.3: FE-MOSFET step-by-step fabrication outline.

To illustrate how the proposed device can be created, a detailed outline of the FE-MOSFET device production process is shown in **Figure 3.3.** The initial step is to thin the silicon film, then thermally oxidize and bond hafnium oxide to the silicon wafer using the silicon fusion bonding (SFB) method. SFB is the process of connecting two silicon wafers without transitional adhesives. The technology has been applied widely in the manufacture of silicon sensors, actuators, and other microstructures, as well as in the creation of silicon-on-insulator (SOI) substrates and silicon power devices. Atomic layer deposition (ALD) deposits the gate dielectric (SiO_2/HfO_2) on the silicon interfacial layer [21]. Next, using electron beam evaporation at room temperature, the N-Poly-Si gate is placed on top of the gate dielectric. The source and drain regions are implanted to activate the source, and the drain area dopants and spike are annealed [21]. Following lift-off, electron beam

evaporation deposits the source/drain metal connections. After forming, the FE-MOSFET proceeds with its processing.

3.5 RESULTS AND DISCUSSION

3.5.1 Device Scalability

Equations (3.7-3.9) provide the current equations used to estimate the device performance in three different regions of operation: the cut-off, linear, and saturation regions.

$$I_d = \left(\frac{\mu C_{ox} W}{L}\right)(\eta - 1)\, V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{\eta\, V_T}\right)\left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \quad \text{(cut-off region)} \quad (3.7)\ [22]$$

$$I_d = \left(\frac{\mu C_{ox} W}{L}\right)(V_{gs} - V_{th} - 0.5\, V_{ds})\, V_{ds} \quad \text{(linear region)} \quad (3.8)\ [22]$$

$$I_d = \left(\frac{\mu C_{ox} W}{2L}\right)\left(V_{gs} - V_{th}\right)^2 (1 + \lambda\, V_{ds}) \quad \text{(saturation region)} \quad (3.9)\ [22]$$

where I_d is drain current, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W is channel width, L is channel length, η is subthreshold swing coefficient, V_T is the thermal voltage, V_{gs} is gate-source voltage, V_{th} is the threshold voltage, V_{ds} is drain-source voltage, and λ is the channel length modulation parameter.

Figure 3.4(a) shows the variation comparison of drain current (I_D) concerning the gate-source voltage (V_{gs}) at constant drain-source voltage (V_{ds}) of 0.5 V in both linear and log scales for both the device structures. From the variation comparison, we can say that I_D increases exponentially with an increase in the $V_{gs,}$ and improvement in I_D is recorded for the FE-MOSFET than for conventional MOSFET.

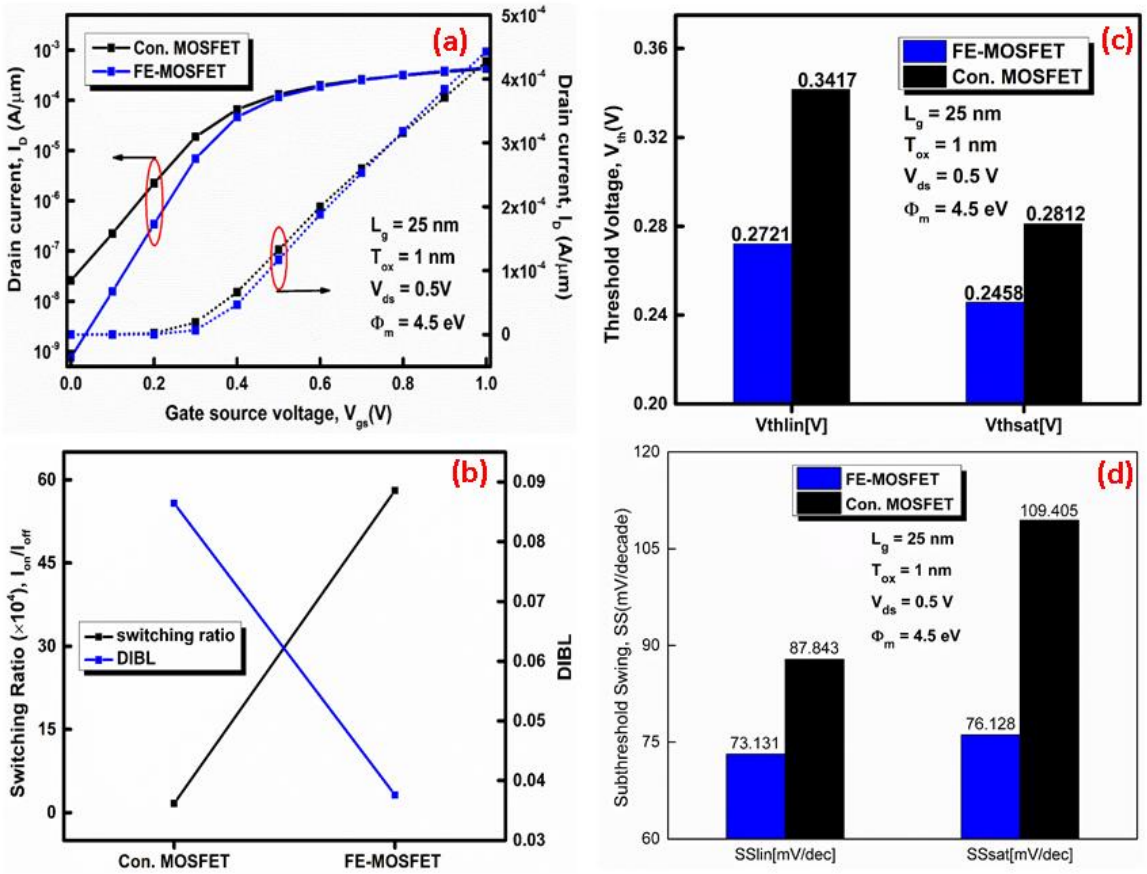

Figure 3.4: (a) Variation of I_d - V_{gs} in linear and log scales, (b) I_{on}/I_{off} ratio and DIBL, (c) V_{th}, and (d) SS comparisons for different configurations [12].

As it is found for the modified configuration, the on-current (I_{on}) improves with the reduction in off current (I_{off}) or leakage current, which gives a higher switching ratio (I_{on}/I_{off}) and enhanced switching speed to the device, as shown in **Figure 3.4(b).** This is attributed to the reduction in tunnelling current and resistance offered by the substrate region modification. Secondly, an essential short channel parameter is DIBL, the second name for channel length modulation[22-25]. DIBL is responsible for increased leakage current at a higher constant drain-source voltage. So, for better device performance, the DIBL effect should be minimized.

The DIBL value for conventional MOSFET and modified FE-FET is displayed in the same **Figure 3.4(b)**. The threshold voltage (V_{th}) comparison for conventional MOSFET and FE-MOSFET is shown in **Figure 3.4(c)**. V_{th} for a device shows the voltage at which the hole

concentration in the substrate region equates to the electron concentration in the channel region so that the current starts to flow to its maximum value [26-29]. The threshold voltage for the modified configuration is less than the conventional device structure, which shows that the device can switch from off to on with less of an applied gate-source voltage value. The subthreshold swing (SS) value for both device configurations is displayed as a bar graph for linear and saturation regions in **Figure 3.4(d).** As discussed in Chapter 2, SS is an important short-channel parameter that should be low for better device performance. From **Figure 3.4(d),** it is clear that the SS in both linear and saturation regions of operation is reduced significantly for FE-MOSFET approaching the ideal value (60mV/dec). This is due to an increase in gate coupling capacitance with an increment in permittivity (k), which improves gate voltage control in the channel region, thus enhancing the SS value[30].

3.5.2 Analog metrics

In this part of the chapter, from the view of analog performance device applications, many critical parameters like transconductance (g_m), Transconductance Generation Factor (TGF), Early Voltage (V_{EA}), and Intrinsic gain (A_V) are described with their explanation. **Figure 3.5(a)** represents the g_m and TGF variation concerning the V_{gs} at constant V_{ds} of 0.5 V for both device structures. Equations (2.10) and (2.11) formulate the g_m and TGF, respectively [20]. **Figure 3.5(a)** shows that the FE-MOSFET shows enhanced results with an improved value of g_m and TGF. Transconductance is an essential analog factor for a device as it estimates its overall gain. It can be evaluated from the transfer characteristics by performing the derivative of I_D to the applied V_{gs} as shown in Equation (3.10) [32-34]. A higher value of g_m shows better control of gate voltage on the channel and hence became the reason for reduced short-channel effects. Also, using ferroelectric material with a combination of high-k dielectric material enhances the mobile electron

concentration and average carrier velocity in the channel region, thus directly increasing the g_m. Ferroelectric materials can improve carrier transport in the channel by: reducing interface traps and scattering and enhancing electric field distribution in the channel.

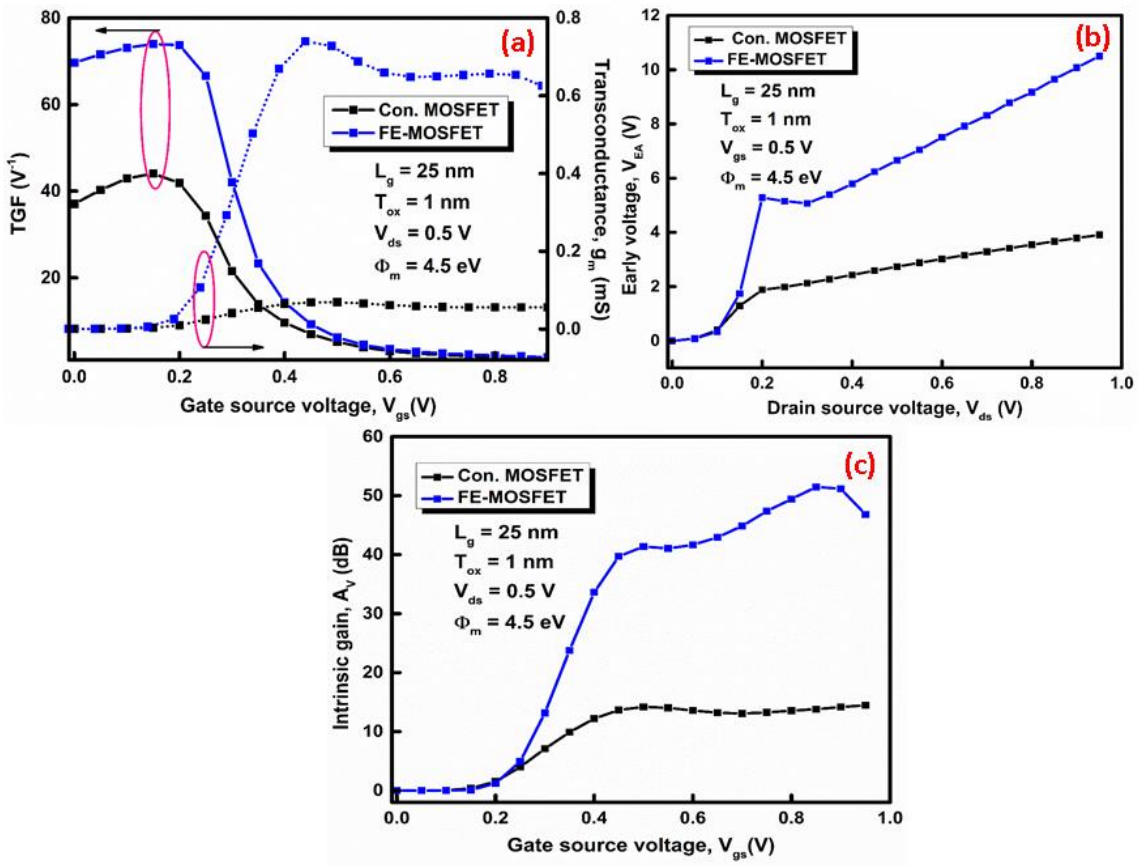

Figure 3.5: (a) g_m and TGF vs. V_{gs}, (b) V_{EA} vs. V_{ds}, and (c) A_v vs. V_{gs} for different structures [12].

$$g_m = \partial I_d / \partial V_{gs} \quad (3.10)\ [12]$$

$$TGF = g_m / I_d \quad (3.11)\ [12]$$

$$V_{EA} = I_d / g_d \quad (3.12)\ [12]$$

$$A_v = g_m / g_d = (g_m / I_d) \times V_{EA} \quad (3.13)[12]$$

This results in higher carrier velocity, further increasing g_m. As the comparison is done with the conventional MOSFET, that is why it shows the 10-fold gap values. Also, TGF shows the net gain generated per unit power loss for a device as formulated in Equation (3.11). A higher value of TGF shows how efficiently a device can work at low supply voltages. FE-

MOSFET configuration reaches the maximum value of TGF. The reason for the higher TGF is the higher drain current and its higher g_m value.

Table 3.2: Summary of electrostatic and analog parameters for different structures [12].

Parameter	Unit	Conv. MOSFET	FE-MOSFET
I_{on}	(A)	4.27×10^{-4}	4.43×10^{-4}
I_{off}	(A)	2.58×10^{-8}	7.62×10^{-10}
I_{on}/I_{off} Ratio	-	1.65×10^{4}	0.58×10^{6}
V_{th}(lin)	(V)	0.34	0.27
V_{th}(sat)	(V)	0.28	0.25
SS(lin)	(mV/dec)	87.84	73.13
SS(sat)	(mV/dec)	109.40	76.13
g_m	(μS)	068	739
TGF	(V^{-1})	44.08	73.98
V_{EA}	(V)	3.91	10.50
A_v	-	13.78	51.48

The V_{EA} variation with the corresponding applied supply voltages are displayed in **Figure 3.5(b)** for the conventional MOSFET and FE-MOSFET structures. This parameter should be as high as possible to improve the analog performance of a device configuration. According to Equation (2.12), the Early voltage can be found. The highest value of early voltage is recorded for the FE-MOSFET configuration compared to the conventional MOSFET structure due to the improved SCEs. **Figure 3.5(c)** displays the variation of A_V concerning the variation of V_{gs} at constant V_{ds} at 0.5 V. These gain values should be high for better-performance devices [35-38]. Also, the maximum value of intrinsic gain is obtained for the FE-MOSFET structure because of the higher V_{EA} and g_m as formulated in Equation (3.13). Intrinsic gain defines the overall voltage gain for a device regardless of its bias point. Table 3.2 summarizes all the electrostatic and analog parameters for different structures.

3.5.3 RF analysis

With keeping the view of RF application, RF parameters play an important role in device performance [39-41]. Some important RF parameters like unity gain frequency (fT), GBP, GFP, TFP, and GTFP are evaluated for conventional MOSFET and FE-MOSFET device structures. The variation of two parasitic capacitances, C_{gs} and $C_{gd,}$ as a function of V_{gs} is displayed in **Figure 3.6(a)**. Both parasitic capacitances are plotted on a linear scale. A small AC signal analysis was simulated at a 1MHz operating frequency with a DC voltage varying from 0 to 1V with 0.05 step size to extract these gate-to-source and gate-to-drain capacitance. In **Figure 3.6(a),** it is shown that both parasitic capacitances increase gradually concerning the V_{gs} showing a higher value for the FE-MOSFET than the conventional MOSFET structure due to the high lateral field, which directly connects to the increment in charge carrier movement from source to drain side. Another reason for high parasitic capacitances is increased gate capacitance and dielectric permittivity. The curve shows less increment behaviour for gate-to-source capacitance than the conventional MOSFET, but FE-MOSFET shows the peak value. Similarly, the curve for the drain-to-source capacitance of FE- MOSFET first indicates a lower value than the conventional MOSFET. However, after the particular value around the threshold voltage, it shows increased behaviour compared to conventional MOSFET.

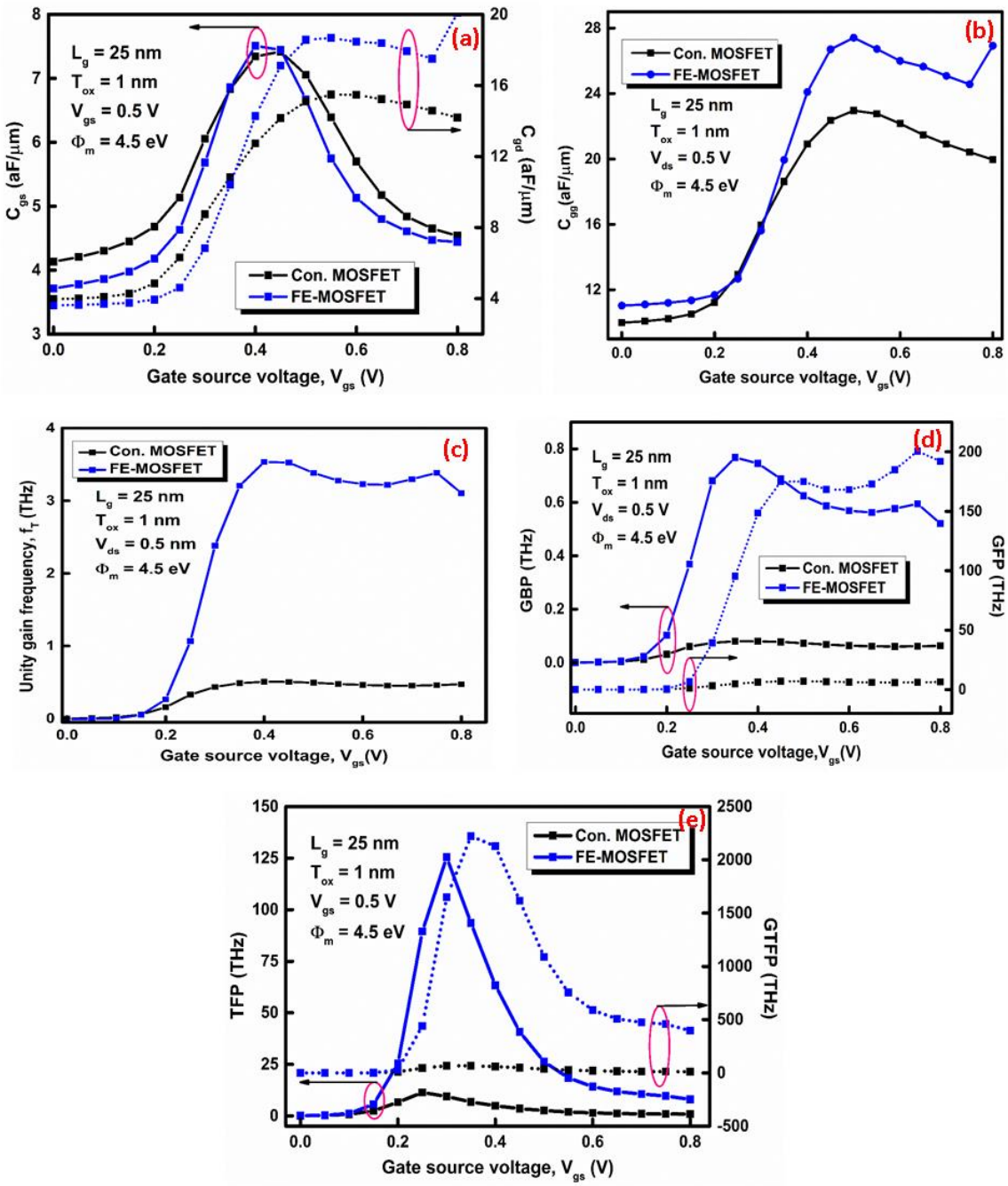

Figure 3.6: Variation of (a) C_{gs} and C_{gd} to V_{gs}, (b) C_{gg} to V_{gs} (c) f_T to V_{gs}, (d) GBP and GFP to V_{gs} (e) TFP and GTFP to V_{gs} for each configuration [12].

$$f_T = g_m/2\pi\left(C_{gs} + C_{gd}\right) \quad (3.14)\ [30]$$

$$\text{GBP} = g_m/\,20\pi(C_{gd}) \quad (3.15)\ [30]$$

$$\text{GFP} = (g_m/g_d) \times f_T \quad (3.16)\ [30]$$

$$\text{TFP} = (g_m/I_d) \times f_T \quad (3.17)\ [30]$$

$$\text{GTFP} = (g_m/g_d) \times (g_m/I_d) \times f_T \quad (3.18)\ [30]$$

In **Figure 3.6(b)**, simulated data of gate capacitance (C_{gg}) is displayed as a function of V_{gs}. The C_{gg} curve shows the same variation as the parasitic capacitances as C_{gg} combines C_{gs} and C_{gd}. So, the FE-MOSFET has a higher gate capacitance value than the conventional MOSFET configuration. **Figure 3.6(c)** displays the variation of unity gain frequency (f_T) as a function of V_{gs} for both device configurations. f_T defines the frequency value at which the device obtains unit current gain [42]. The formula used for the calculation of f_T is shown in Equation (3.14); the maximum value of f_T is demonstrated from the FE- MOSFET structure data compared to conventional MOSFET structure as the g_m is higher for the FE-MOSFET structure. **Figure 3.6(d)** represents the variation of GBP and GFP with V_{gs} at constant V_{ds} of 0.5 V for conventional MOSFET and FE-MOSFET. Gain bandwidth product (GBP) and Gain frequency product (GFP) are the essential performance parameters for high-frequency applications. Both parameters are formulated in Equations (3.15) and (3.16) As the ratio of g_m to C_{gd} is higher and shows the maximum value for the FE-MOSFET in comparison to conventional MOSFET, which shows better device performance, the modified FE-MOSFET shows the enhanced results for GBP than the conventional MOSFET structure. The peak value of GBP indicates the voltage at which the device's gain becomes maximum.

Secondly, the GFP factor is the product of unity frequency gain and intrinsic gain as formulated in Equation (3.16), which are higher for the FE-MOSFET configuration than the conventional one. So, as displayed in **Figure 3.6(d)**, the GFP shows a gradual increase with the increase in gate-source voltage, and the modified FE-MOSFET structure shows the maximum peak value of GFP compared to the conventional MOSFET structure.

Other important RF performance parameters are the transconductance frequency product (TFP) and the gain transconductance frequency product (GTFP), which are formulated in Equations (3.17) and (3.18). **Figure 3.6(e)** illustrates the variation of TFP

and GTFP with an increase in the V_{gs} at constant V_{ds} of 0.5 V for both configurations. The TFP curve shows the gradual increase concerning the V_{gs} at constant V_{ds} of 0.5 V. As TFP is a product of transconductance generation factor and unity gain frequency as formulated in Equation (3.17), which are higher for modified FE- MOSFET configuration in comparison of conventional MOSFET structure. Thus, the FE-MOSFET device structure shows the maximum value for TFP.

Similarly, from Equation (3.18), we can see that the GTFP depends on the intrinsic gain and the TFP factor .so; for the high value of A_V and TFP, GTFP would be high. Consequently, we get a higher GTFP value for the FE-MOSFET configuration than the conventional one. Thus, modified FE-MOSFET is suitable for gain, transconductance, and speed applications. All the RF parameters are tabulated in Table 3.3.

Table 3.3: Summary of RF parameters for different structures [13].

Parameter	Unit	Con. MOSFET	FE-MOSFET
C_{gs}	(aF)	7.34	7.51
C_{gd}	(aF)	15.48	18.67
C_{gg}	(aF)	22.96	27.41
f_T	(THz)	0.51	4.42
GBP	(THz)	0.79	7.67
GFP	(PHz)	0.006	0.200
TFP	(THz/V)	11.35	125.49
GTFP	(PHz/V)	0.07	2.22

3.5.4 Application of FE-MOSFET

For digital applications, combinational circuits are in high demand because of their low power consumption and high switching speed. Several designs are explored to meet the objectives. Using FE-MOSFET is an example of this effort at the device level. Here, the one brief application of FE-MOSFET is defined and presented using the COGENDA VISUAL TCAD simulator. The performance is compared with the conventional MOSFET-based inverter. To show the inverter's application, n-channel and p-channel FE-MOSFET have been designed. A 10 nm silicon oxide spacer is used for electrical isolation between the n-channel and p-channel FE-MOSFET.

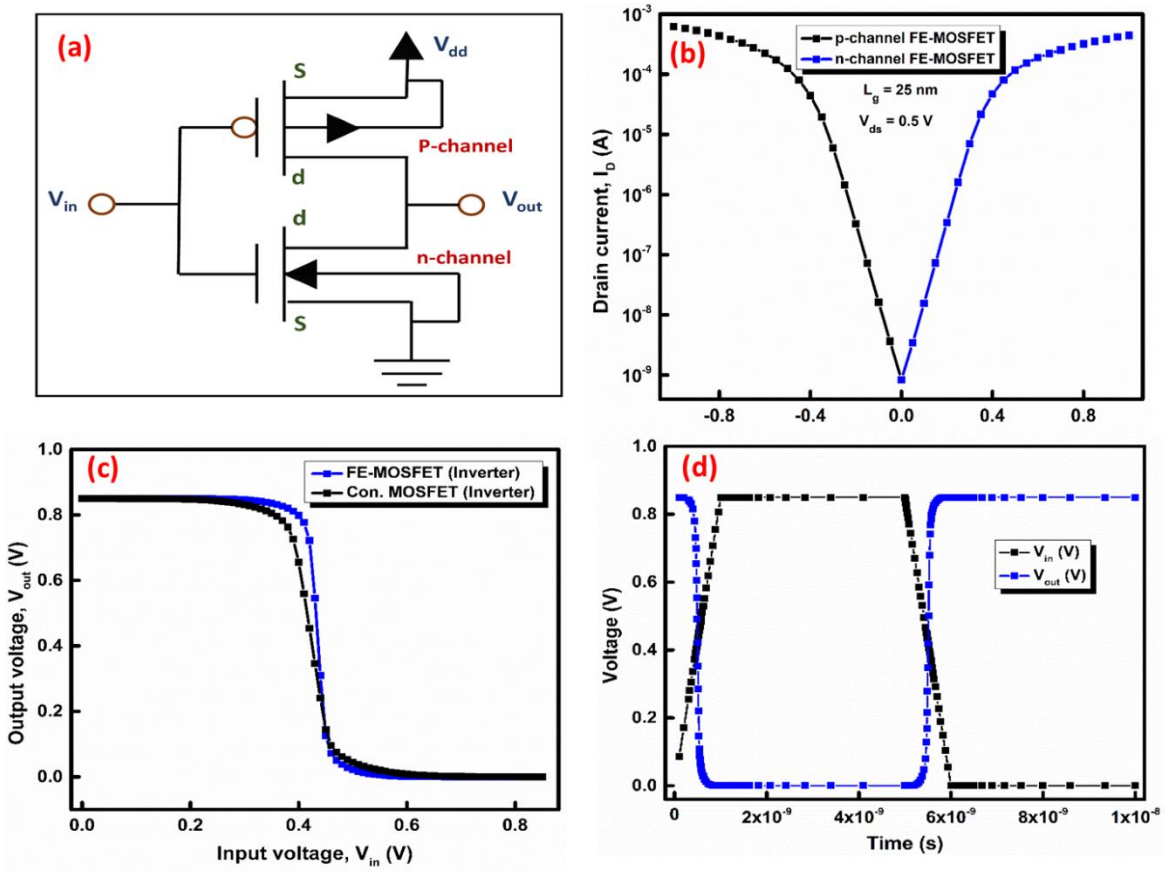

Figure 3.7: (a) Schematic of FE-MOSFET-based inverter, (b) threshold voltage matching of n and p-channel FE-MOSFET to V_{gs} (c) Voltage Transfer Curve (VTC) Characteristics of conventional MOSFET and FE-MOSFET based inverter, (d) Transient curve of FE-MOSFET-based inverter [12].

The gate contact of n-channel and p-channel FE-MOSFET are of N-Poly-Si with a work function of 4.5 eV and 4.95 eV, respectively. For p-channel FE-MOSFET, doping material of n-type is used for the substrate region, and doping material of p-type is used for the source and drain region with a concentration of 1×10^{17} cm^{-3} and 1×10^{20} cm^{-3}, respectively. The general circuit diagram explaining the FE-MOSFET-based inverter is shown in **Figure 3.7(a)**. The I_D-V_{gs} characteristics of both channel configuration devices are plotted together to match the $V_{th,}$ as shown in **Figure 3.7(b)**. The V_{gs} swept from -1 to 1 V at constant V_{ds} 0.5 V with a dual work function metal (DWFM) integration scheme. The voltage transfer characteristics (VTC) of the designed FE-MOSFET inverter and conventional MOSFET-based inverter are displayed in **Figure 3.7(c)**. It shows that the transition range (TR) of an FE-MOSFET-based inverter is sharper compared to a conventional MOSFET inverter, which signifies high speed and fast switching for a device.

The two critical points on the curve where the slope of voltage transfer characteristic becomes -1 correspond to logic 0 and logic 1, denoted as maximum input voltage (V_{IL}) and minimum input voltage (V_{IH}), respectively. The threshold voltage of the inverter configuration is the transition voltage or a voltage point at which $V_{in} = V_{out}$ on the VTC curve. In this case, the switching threshold voltage for the FE-MOSFET inverter is 0.43 V, and for the conventional MOSFET-based inverter is 0.42 V.

3.5.4.1Noise Margin calculation

Noise margin (NM) defines the immunity of noise for a circuit. The noise margin should be as high as possible for better circuit performance. For low signal levels (NM_L) and high signal levels (NM_H), the noise margin is tabulated as in Equations (3.19) and (3.20):

$$NM_L = V_{IL} - V_{OL} \quad (3.19)\ [12]$$

$$NM_H = V_{OH} - V_{IH} \quad (3.20)\ [12]$$

V_{OL} and V_{OH} are the minimum and maximum output voltage when the corresponding output levels are logic 0 and 1, respectively. The parameters required to compute the noise margin (NM) and transition region (TR) are tabulated in Table 3.4.

The transient analysis for the FE-MOSFET-based inverter is displayed in **Figure 3.7(d)**. All the simulations were done at room temperature (300 K) using the drift-diffusion method solver level 1(DDML1) technique [34]. The input pulse and V_{DD} of 0.85 V are standard for both analyses. As in the inverter, the output of the inverter is at logic 1 when n-channel FE-MOSFET is in cut-off mode, and it shows logic 0 in output when the n-channel FE-MOSFET conducts.

Table 3.4: Summary of inverter-based parameters for different structures [12].

Parameter	Unit	Conventional MOSFET	FE-MOSFET
V_{IL}	V	0.27	0.34
V_{IH}	V	0.60	0.54
NM_L	mV	261.7	332.6
NM_H	mV	239.4	298.8
TR	V	0.33	0.20

3.6 SUMMARY

In summary, the effect of ferroelectric material in the substrate region between the high-k HfO_2 layers on the conventional MOSFET structure in terms of the analog and RF parameters using the VISUAL TCAD simulator was investigated. The proposed architecture shows enhanced analog and RF parameters with reduced SCEs. FE-MOSFET structure shows a better switching ratio as the I_{off} decreases by 97.05% with a 3.60% increased I_{on} current. Also, the SCEs, like the subthreshold swing lower by 16.75% and 30.42% in linear and saturation regions, respectively. DIBL is reduced by 56.51% and V_{th} by 20.37% and 12.59% in linear and saturation regions, respectively. For the proposed

architecture, analog parameters like g_m and TGF enhanced with 10-fold and 67.85%, respectively. The V_{EA} and A_V show improved results for the modified configuration, with 2-folds and 3-folds, respectively. These factors are compared with the conventional MOSFET which is why the modified configuration shows a multiple fold improvement but when these results are compared to the conventional NCFET, these shows almost 30 to 40 % increment as discussed in Chapter 4.

Furthermore, RF performance parameters like GBP and GFP increased by a factor of 8 and 31, respectively. The TFP is enhanced by tenfold, and the GTFP improves by 30-fold for the FE-MOSFET structure. For the modified architecture, the unity gain frequency is increased by sevenfold. Furthermore, from the noise margin parameters, it is concluded that the transition range for the proposed device structure is better than the conventional MOSFET structure, as NM_L and NM_H are improved by 27.09% and 24.81%. So, with better NM and TR, the FE-MOSFET-based inverter is a better option for digital applications. Thus, from the above results and discussion, the proposed device structure of FE-MOSFET can be considered an alternate choice for designing analog and RF circuit devices.

After thoroughly examining the FE-MOSFET's analog and RF characteristics, solving the reliability issues related to this suggested device is critical. Therefore, the following chapter's main focus will be investigating the ferroelectric material's Density Functional Theory (DFT) characteristics and how its negative capacitance affects the conventional MOSFET characteristics when used in the gate stack to ensure the device's reliability.

3.7 REFERENCES

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4

CHAPTER

DFT-based Atomic Calculation of Si-HfO_2 and impact of Negative Capacitance on Analog/RF, and VTC parameters of MOSFET

- *This chapter discusses the DFT-based analysis for Si-HfO_2 as a ferroelectric and the effect of its negative capacitance on SCEs, analog and RF performance of MOSFET, and its digital application.*
- *It is found that the switching ratio of the Modified NCFET increased almost eleven times, thereby improving the analog performance in terms of transconductance, transconductance generation factor, intrinsic gain, and early voltage, maximum frequency of oscillation compared to conventional MOSFET.*
- *It is also analyzed that the proposed device with a ferroelectric layer in the gate stack and hafnium oxide as buried oxide exhibits the most improved static performance compared to the conventional MOSFET configuration.*
- *Also, the inverter-based parameters like NM ratio and transition region are improved in the case of a Modified NCFET-based inverter.*
- *Consequently, the proposed NCFET device with a ferroelectric layer in the gate stack and HfO_2 as buried oxide would be an attractive solution for low-power and high-performance CMOS circuits*

4.1 INTRODUCTION

The evolution of semiconductor technology has been driven by the relentless pursuit of higher performance, lower power consumption, and increased device density. In this context, the comparison between buried oxide MOSFETs, particularly those based on SOI technology, and conventional bulk silicon MOSFETs is of critical importance. Buried oxide MOSFETs have emerged as a key technology in modern electronics, offering a range of benefits that address many of the challenges conventional MOSFETs face, especially as device dimensions continue to shrink following Moore's Law [1-4].

The fundamental difference between buried oxide MOSFETs and conventional MOSFETs lies in their structural composition. Conventional MOSFETs are built on bulk silicon substrates, where the active device region is formed directly on the silicon wafer. In contrast, buried oxide MOSFETs are typically constructed using SOI technology, where a thin layer of silicon is separated from the bulk substrate by a buried oxide layer (BOX). This structural difference has profound implications for the electrical and physical characteristics of the devices. The presence of the buried oxide layer in SOI-MOSFETs introduces a range of benefits that enhance device performance, reduce power consumption, and improve isolation, among other advantages [5-9]. These benefits are particularly evident in the context of the challenges posed by device scaling.

One of the most significant advantages of buried oxide MOSFETs is the reduction in parasitic capacitance. In conventional MOSFETs, the active device region is directly in contact with the bulk silicon substrate, leading to capacitance between the source/drain and the substrate. This parasitic capacitance is a major contributor to power consumption and signal delay, particularly as device dimensions shrink. In buried oxide MOSFETs, the BOX layer serves as an insulator between the active silicon layer and the substrate, significantly

reducing parasitic capacitance. This reduction in capacitance translates into several performance benefits. With lower capacitance, the time required to charge and discharge the device during switching operations is reduced, leading to faster signal propagation and higher operating frequencies. This is particularly beneficial in high-speed digital circuits and RF applications, where speed is a critical parameter. Reduced parasitic capacitance also leads to lower dynamic power dissipation. In digital circuits, dynamic power consumption is directly proportional to capacitance, the square of the supply voltage, and the switching frequency. By reducing the capacitance, buried oxide MOSFETs achieve lower power consumption, which is crucial for battery-powered devices and energy-efficient systems. Also, Lowering the subthreshold swing (SS) in BOX-assisted GS-NCFET reduces heat dissipation primarily by improving energy efficiency and reducing power consumption in the following ways:In traditional MOSFETs, reducing SS allows transistors to switch ON at lower voltages. Since dynamic power dissipation (P_{dyn} = α C V_D^2, a lower operating voltage significantly decreases power dissipation. Less power means less heat generation, leading to better thermal management and reduced leakage current lowers standby power A lower SS means the transistor switches off more sharply, reducing leakage current and since leakage power is $P_{leak} = V_D \times I_{leak}$, lowering leakage current reduces static power dissipation. This is particularly crucial for low-power applications like IoT and mobile devices. Another advantage of using BOX is to reduced switching losses. The energy loss per switching cycle is given by E = ½ C V_D^2. Lowering V_D means each switching event consumes less energy, reducing the heat generated during fast transitions in high-frequency circuits. Also, due to the use of ferroelectric material in gate stack enhanced thermal stability of GS-NCFET. In NCFETs, the ferroelectric layer helps stabilize the transistor operation, reducing short-channel effects (SCE). This leads to better electrostatic control, preventing excessive heat buildup due to SCE-related leakage currents. So, the combination

of BOX and ferroelectric layer in GS-NCFET maintains the balance between the operating speed and heat dissipation of the device.

Another key advantage of buried oxide MOSFETs is the superior electrical isolation provided by the BOX layer. In conventional MOSFETs, the active device region is in close proximity to the bulk silicon substrate, which can lead to unwanted interactions between adjacent devices. These interactions, often referred to as crosstalk, can degrade signal integrity and lead to errors in digital circuits. The BOX layer in buried oxide MOSFETs provides a high degree of electrical isolation between the active device region and the substrate. This isolation minimizes crosstalk and other forms of interference, leading to several benefits.

As MOSFETs are scaled down to smaller dimensions, they become increasingly susceptible to short-channel effects (SCEs) [10]. These effects, which include Drain-Induced Barrier Lowering (DIBL) and threshold voltage roll-off, are a major challenge in conventional MOSFETs. SCEs arise due to the proximity of the source and drain regions in short-channel devices, weakening the control that the gate exerts over the channel. Buried oxide MOSFETs, particularly those based on SOI technology, offer superior control over the channel region, mitigating the impact of short-channel effects. The combination of reduced parasitic capacitance, superior electrical isolation, and better control over short-channel effects positions buried oxide MOSFETs as a key technology for the next generation of electronic devices. However, as with any technology, continued innovation and development will be necessary to overcome the challenges associated with scaling and thermal management, ensuring that buried oxide MOSFETs remain at the forefront of semiconductor technology for years to come [11].

On the other hand, a Negative Capacitance Field-Effect Transistor (NCFET) is an advanced type of transistor that leverages the unique properties of ferroelectric materials to

achieve superior performance, particularly in terms of power efficiency and scalability. In a conventional FET, the subthreshold swing, which governs the relationship between the gate voltage and the drain current, is limited to 60 mV/decade at room temperature as discussed in **Chapter 1**. This limit hinders further reduction in operating voltage and power consumption. NCFETs overcome this limitation by incorporating a ferroelectric layer into the transistor's gate stack. This layer exhibits negative capacitance, where the voltage across the ferroelectric material decreases as the charge increases. This amplifies the gate voltage effectively, allowing the transistor to switch at a lower voltage, thus reducing power consumption. The benefits of NCFETs include improved energy efficiency, enabling lower power operation without compromising performance. They are particularly promising for applications in low-power electronics, such as mobile devices and IoT, and for extending Moore's Law by facilitating the scaling of transistors to smaller dimensions [12-15]. The integration of negative capacitance into FETs represents a significant step forward in transistor technology, offering a path to more energy-efficient and powerful electronic devices [16].

By considering the above advantages of BOX and NCFETs, firstly, the density-functional theory (DFT) is done for the Silicon-Hafnium Oxide (Si-HfO_2) with different concentrations of silicon. And further by the use of Si-HfO_2 as a ferroelectric layer in the gate stack and a high-k dielectric layer of HfO_2 as BOX, we created an NCFET structure with BOX called Modified NCFET. The following outline constitutes this chapter's structure: The second section of this chapter provides the device structure of Modified NCFET discussed with computational models that were applied throughout this study. In the second section of this chapter, an overview of the DFT analysis of HfO_2, 1-Si-HfO_2, and 2-Si-HfO_2 along with the structural parameters and DFT parameters like Bandstructure, Projected Density of States (PDOS) is discussed. In the following section of the chapter, the simulation methodology for

device architecture in VISUAL TCAD of the suggested device will be discussed. The later part of the chapter discusses the results obtained through simulation. Results include the effect of BOX and negative capacitance of Si-HfO_2; these factors affect the electrical and RF performance of E-mode conventional MOSFET parameters. The conclusion of the chapter is presented in the final part of the chapter's summary.

4.2 DEVICE DESIGN AND PHYSICAL MODELS

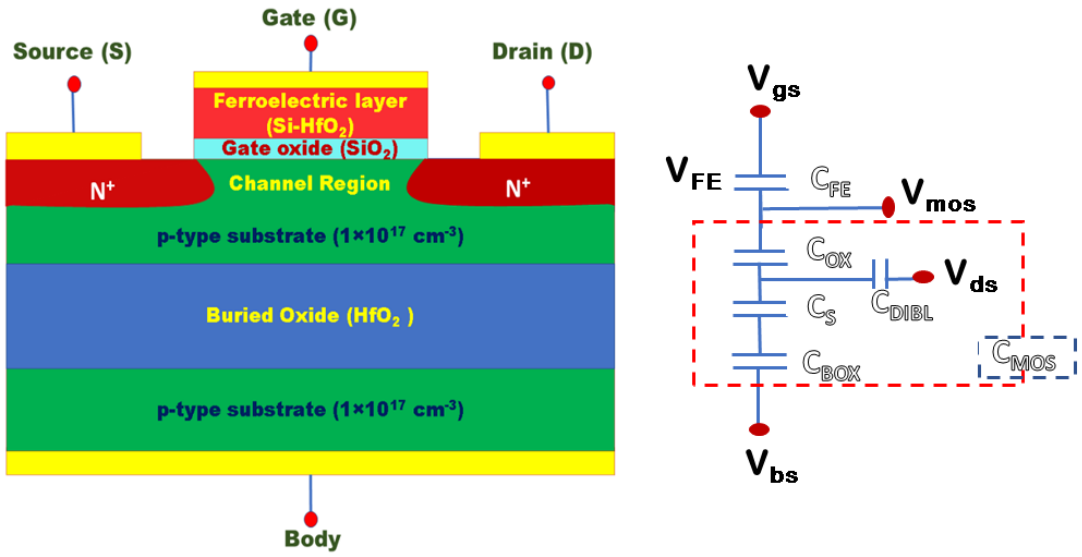


Figure 4.1: Proposed Modified NCFET structure with Si-HfO_2 ferroelectric material and HfO_2 as BOX with equivalent capacitance model [17].

Figure 4.1 represents the proposed Modified NCFET structure with Si-HfO_2 ferroelectric material and HfO_2 as BOX and its equivalent circuits. In device simulation, the parameters are often determined using a hit-and-trial method, where initial values are estimated based on fabrication data, empirical models, or past designs, then iteratively adjusted to match desired performance. This approach involves running multiple simulations with different sets of parameters, such as threshold voltage, mobility, oxide capacitance, and channel length modulation, while comparing the results against measured or expected device characteristics. The adjustments continue until the simulated behavior closely aligns with

experimental results or design specifications. This iterative process helps refine the model for accuracy, especially when dealing with short-channel effects, leakage currents, and other non-idealities that are difficult to predict analytically. For a fair comparison, the parameters such as device size, doping profiles, gate work function, etc., are maintained constant for both devices. The distinction is that while SiO_2 is the gate oxide utilized in the other device, Si-HfO_2 and SiO_2 (k = 3.9) are considered equally as the part of gate stack in the Modified NCFET device. Additionally, a layer of HfO_2 (k=25) as a buried oxide with thicknesses of 20 nm is employed in the substrate region. The device's gate length (L_g) is 25 nm, while the S/D regions' ($L_{S/D}$) fixed length is 10 nm. Both devices maintain a constant t_{ox} of 1 nm. P-type doping species are equally doped throughout the substrate region. With n-type Gaussian doping, the doping concentration in the source/drain areas ($N_{S/D}$) is 1×10^{20} cm^{-3}, whereas in the channel region (N_{Ch}) it is 1×10^{17} cm^{-3}.

Table 4.1: Different device configurations used for simulation.

Parameter	**Unit**	**Conventional MOSFET**	**Modified NCFET**
L_g	nm	25	25
$L_{S/D}$	nm	10	10
T_{ox}	nm	1	1
T_{FE}	nm	0	2.5
$T_{high\text{-}K}$	nm	0	20
$N_{S/D}$	cm^{-3}	1×10^{20}	1×10^{20}
N_{ch}	cm^{-3}	1×10^{17}	1×10^{17}
Φ_m	eV	4.5(N-Poly-Si)	4.5 (N-Poly-Si)

The ion-implantation method, a very high-temperature annealing procedure, is used to construct the source and drain region. Metal would melt if it were used as a gate. One of the reasons offered to support the use of polysilicon over metal is its greater melting point. The gate N-Poly-Silicon (N-Poly-Si) has a work function (ϕ_m) of 4.50 eV. It is used because

of its high purity, low resistivity, low thermal stability, and compatibility with CMOS processing. The temperature (T) is maintained at 300 K, and gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) are altered from 0 V to 1.0 V and 0 V to 0.5 V, respectively. In Table 3.1, all the device parameters are tabulated.

Also, silicon material is used as the substrate region for both devices. The following factors make single-crystal silicon a better device substrate material: Its melting temperature is extremely high, approximately 1400 °C. Its Young's modulus is comparable to steel's (about 200 GPa), as light as aluminum, and has excellent mechanical stability. Its thermal expansion coefficient is lower than steel and aluminum; its melting point is about double that of aluminum, and its production procedures utilizing silicon substrates are advanced and well-established.

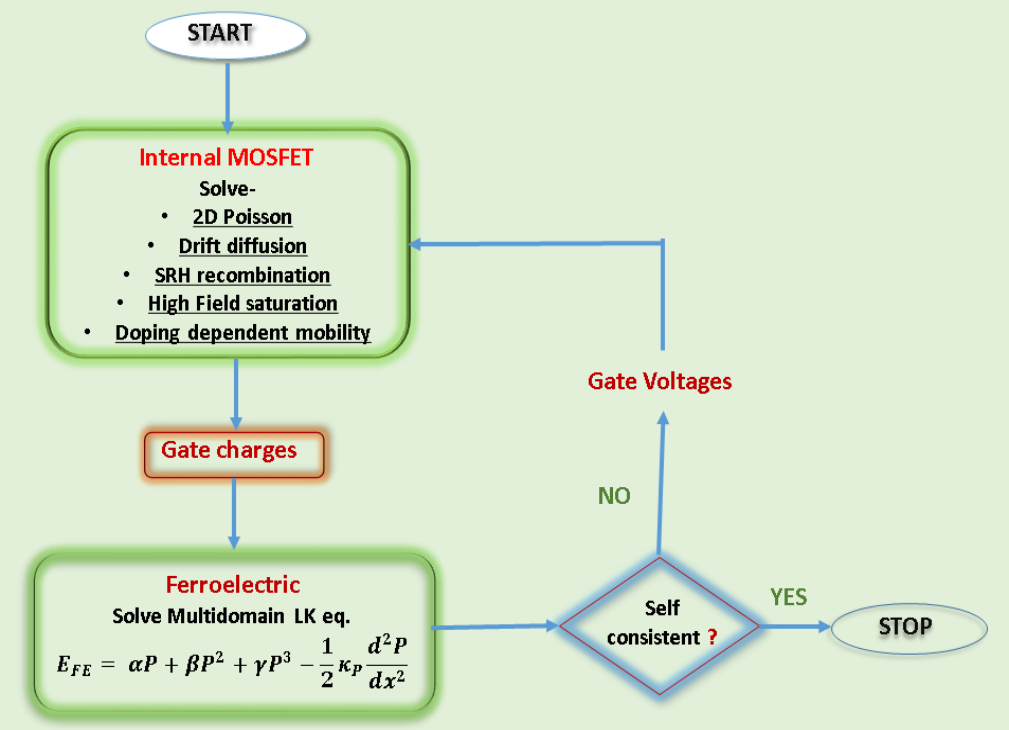


Figure 4.2: Flowchart for the simulation methodology in COGENDA VISUAL TCAD [17].

For the simulation of any semiconductor device, the drift-diffusion (DD) model is widely used and this DD model can be achieved by assuming the various approximations extracted from the hydrodynamic model such as the speed of light is much faster than the speed of charge carriers, collisions are assumed to be elastic collisions and during collisions, band-

gap does not change, degeneration of carriers can be neglected, etc. other more improvements have been done in this DD model which makes it complex but allows it to deal with the real problems. The flowchart of the simulation methodology is shown in **Figure 4.2.** VISUAL TCAD device simulator uses the level 1 drift-diffusion model (DDML1) with constant lattice temperature to solve any procedure. The primary function of DDML1 is to solve the basic electron and hole continuity equations along with Poisson's equations:

$$\nabla.\mathcal{E}\nabla\Psi = -q(p - n + N_D^+ - N_A^-) \tag{4.1}$$

Where Ψ is the electrostatic potential of vacuum level, the concentration of electron and hole is noted by n and p, respectively, $N_D^+ and N_A^-$ defines the ionized impurity concentrations and q is the electron charge magnitude. If $\boldsymbol{\chi}$ defines the electron affinity, $\triangle E_c$and $\triangle E_v$ notes the shift in bandgap due to mechanical strain or heavy doping, and the bandgap of the semiconductor is denoted by E_g. Then, the relation of vacuum level Ψ with the conduction level E_c and valence level E_v is given as

$$E_C = -q\Psi - \chi - \triangle E_C \tag{4.2}$$

$$E_v = E_c - E_g + \triangle E_v \tag{4.3}$$

Further, the intrinsic fermi potential $\Psi_{intrinsic}$ and vacuum level Ψ are connected by the relation given as

$$\Psi = \Psi_{intrinsic} - \frac{\chi}{q} - \frac{E_g}{2q} - \frac{k_b T}{2q} ln\left(\frac{N_c}{N_v}\right) \tag{4.4}$$

In the Genius code, the energy reference 0 eV is taken as the intrinsic Fermi level of the equilibrium state. Continuity equations for electrons and holes are defined as if U is the recombination rate and G is the generation rate for both electrons and holes.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.J_n - (U - G) \tag{4.5}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla . J_p - (U - G) \quad (4.6)$$

Where J_n and J_p are vector quantities and defined as the electron and hole current densities respectively and expressed as

$$J_n = q\mu_n n E_n + qD_n \nabla n \quad (4.7)$$

$$J_p = q\mu_p p E_p + qD_p \nabla p \quad (4.8)$$

Where $\mu_n$and μ_p are mobilities of electrons and holes respectively. $D_n(= \frac{k_b T}{q}\mu_n)$ and $D_p(= \frac{k_b T}{q}\mu_p)$ are the diffusion constants for electron and hole, respectively. E_n and E_p are the effective driving electrical field for electrons and holes and are vector quantities given as

$$E_n = \frac{1}{q} \nabla E_c - \frac{k_b T}{q} \nabla (\ln(N_c) - \ln\left(T^{3/2}\right)) \quad (4.9)$$

$$E_p = \frac{1}{q} \nabla E_v + \frac{k_b T}{q} \nabla (\ln(N_v) - \ln\left(T^{3/2}\right)) \quad (4.10)$$

By using the given values in the above expressions and combining these with Poisson's equations, we obtained the basic equations for DDML1 as follows:

$$\frac{\partial n}{\partial t} = \nabla . (\mu_n n E_n + \mu_n \frac{k_b T}{q} \nabla n) - (U - G) \quad (4.11)$$

$$\frac{\partial p}{\partial t} = -\nabla . (\mu_p p E_p - \mu_p \frac{k_b T}{q} \nabla p) - (U - G) \quad (4.12)$$

$$\nabla . \varepsilon \nabla \Psi = -q(p - n + N_D^+ - N_A^-) \quad (4.13)$$

Equations from Equation (4.1-3.13) are referred to from the VISUAL TCAD simulator manual [18].

4.3 RESULTS AND DISCUSSION

4.3.1 DFT-based Atomic Calculation of Hafnium Oxide (HfO_2)

HfO_2 is a high-k dielectric (k=25) material with a high bandgap, but when the Hafnium (Hf) atom is replaced with the silicon atom by chemical vapor deposition, it revises its electrical properties. Some of these properties are studied by DFT-based calculation of silicon-doped hafnium oxide using the quantum Atomistic Tool Kit (ATK) simulator. In this work, the authors studied the behavior of HfO_2 with a 1-silicon atom and with a 2-silicon atom in terms of its band structure, and projected density of states (PDOS) [19-21]. A simple cubic structure of HfO_2 is taken for calculation and doping of silicon atom is done by replacing one and two hafnium atoms in SC-HfO_2 as shown in **Figure 4.3** and the band structure of these three configurations that is undoped HfO_2, HfO_2 doped with 1 Si-atom, and HfO_2 doped with 2 Si-atom is explained in same **Figure 4.3.**

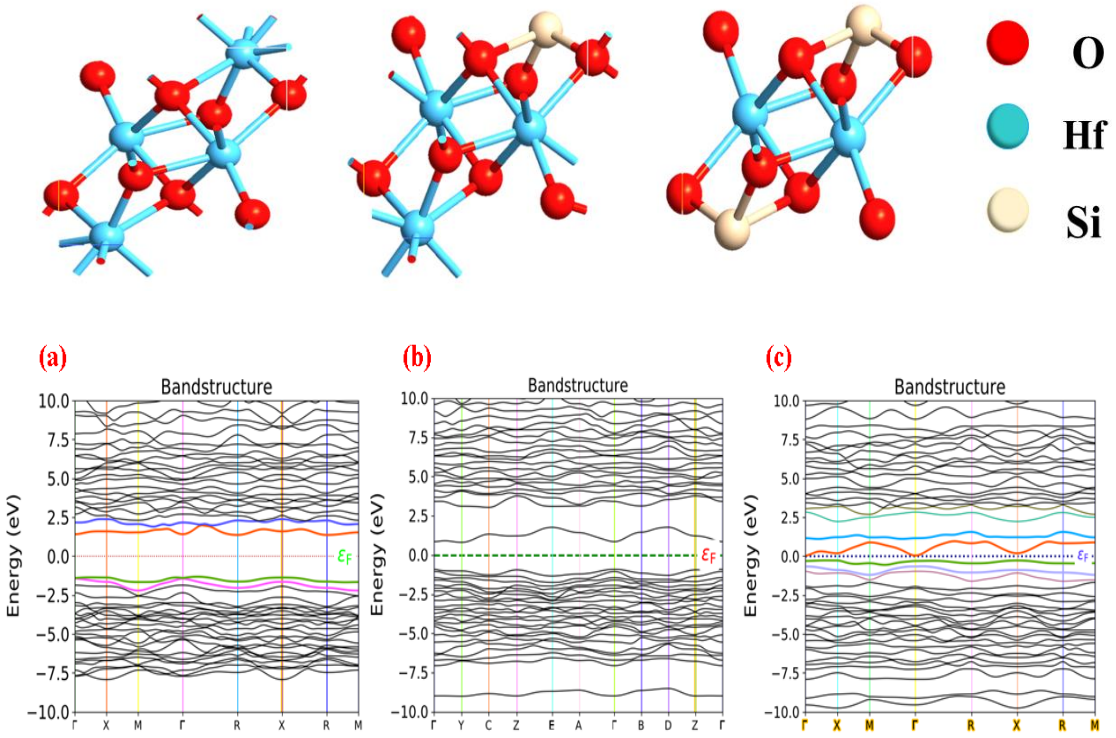


Figure 4.3: The band structure corresponds to (a) HfO_2, (b) 1 Si-atom HfO_2, and (c) 2 Si-atom HfO_2 [17].

From **Figure 4.3**, it is clear that replacing the Hf-atom with Si-atom reduces the bandgap between the conduction band and valence band which is one of the reasons for using the hafnium oxide as ferroelectric. The bandgap for HfO_2 is 2.81 eV, HfO_2 with 1 Si-atom is 1.76eV and reduced to 0.35eV when 2 Si-atom is replaced with an Hf atom.

Further, **Figure 4.4** shows the PDOS for all three configurations. PDOS corresponds to every spin up and spin down configuration which shows the chances of electrons to transfer from VB to CB so that the polarization and charge transfer increases. The highest projected DOS is for the HfO_2 with 2 Si-atom. PDOS gives the projection of a particular orbital of a particular atom on the density of states. So, if you sum over all the projections, you will have the total density of state, or simply, the DOS. PDOS is related to how the energy states are distributed.

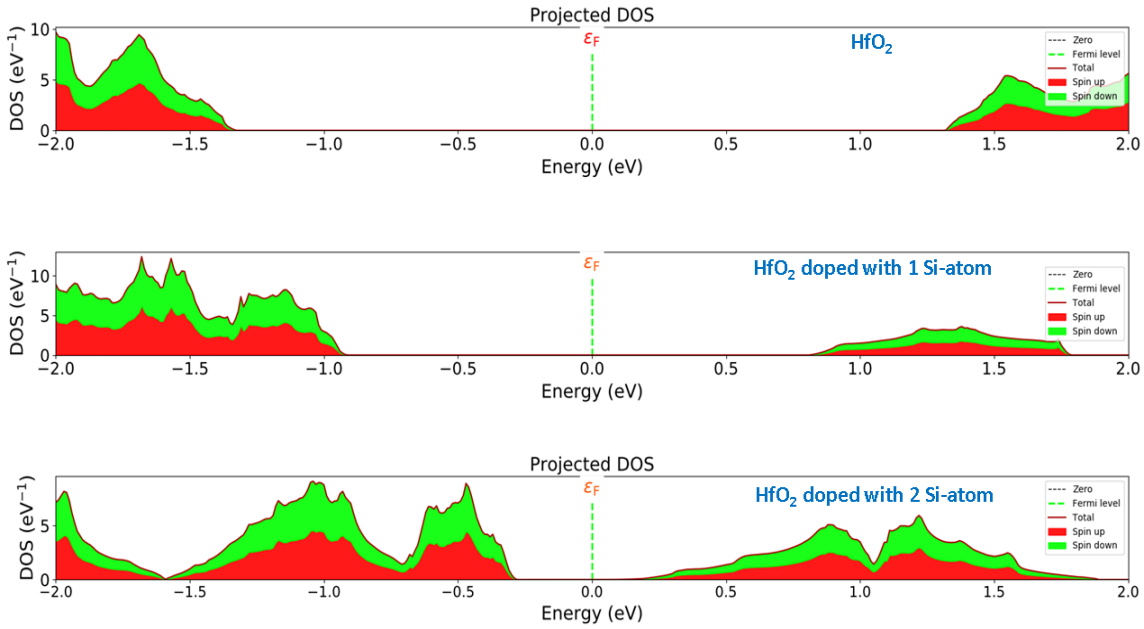


Figure 4.4: The Projected DOS concerning the energy for different configurations of HfO_2 [17].

4.3.2 Voltage Amplification and SCEs in Modified NCFET over MOSFET

Due to the voltage amplification factor in the NCFET structure that is provided by the FE material layer in the gate stack. As we apply the gate-source voltage to turn on the device, there are screening charges (σ) and polarization charges (P) as in **Figure 4.5(a)**. They arrange themselves according to the applied voltage.

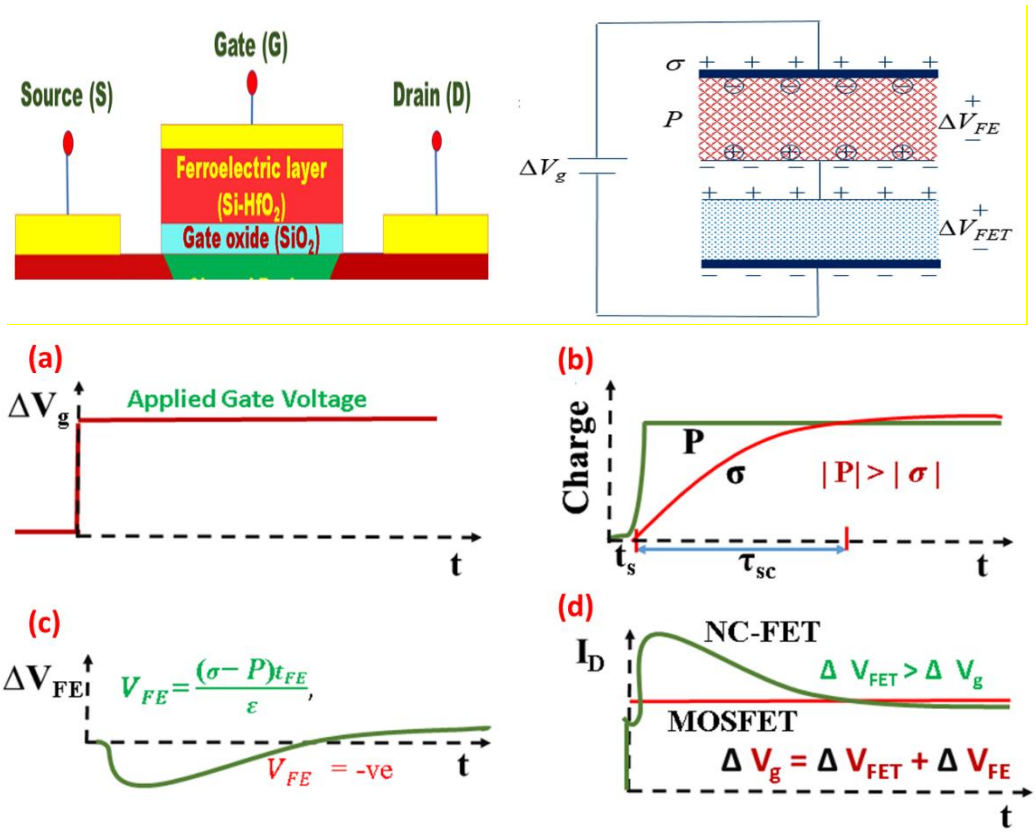


Figure 4.5: The voltage amplification process occurs in the gate stack of NCFET (a) Applied Gate voltage (b) charges in the ferroelectric capacitor (c) negative voltage drop across ferroelectric material (d) voltage amplification in NCFET [17].

The time in which screening charges arrange themselves (T_σ) is much less than the polarization switching time (T_P) shown in **Figure 4.5(b)**, hence the total net voltage drop across the ferroelectric material is negative shown in **Figure 4.5(c)** which results in the voltage amplification in NCFET shown in **Figure 4.5(d). Figure 4.6** shows the transfer

characteristic of conventional MOSFET and the Modified NCFET structure in linear and logarithmic scales. The linear curves show the high I_{ON} for the Modified structure of NCFET due to its negative capacitance phenomenon when compared to the conventional MOSFET. In the logarithmic scale, we can see that the OFF-current or leakage current is almost comparable for both devices which means the switching ratio (I_{ON}/I_{OFF}) becomes high for the Modified NCFET structure [21].

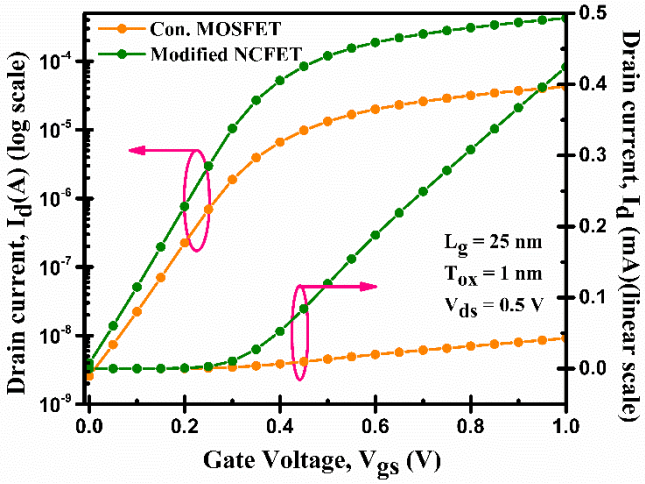


Figure 4.6: Transfer characteristic comparison of conventional MOSFET and Modified NCFET in linear and logarithmic scale [17].

Now talking about the threshold voltage which is the needed voltage to turn on the device, and here for the work, it's less for the Modified NCFET structure than the conventional MOSFET structure shown in **Figure 4.7(a).** Further, the critical SCE is the subthreshold swing value discussed in **Chapter 1**. In this study, we discussed the SS value according to Equation (4.14) we found that the SS value approaches the Boltzmann tranny limit which is 60 mV/dec. The SS value of Modified NCFET is reduced by 8.92% when compared with the conventional MOSFET plotted in **Figure 4.7(a)**. Furthermore, another SCE is DIBL which is responsible for the reduction of threshold voltage and higher leakage current at higher drain bias. When the biasing increases at the drain end, it starts interacting

with the channel region and the source end which results in lower barrier potential and gives the electrons an easy path to travel through the channel.

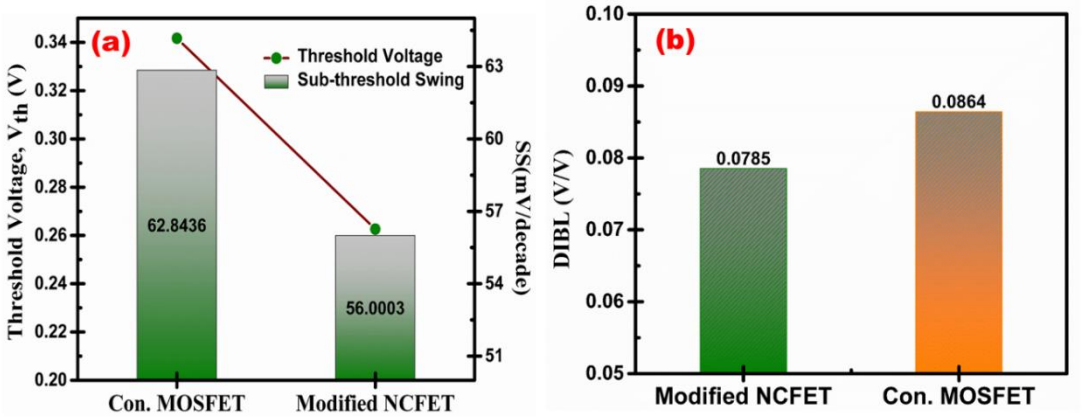


Figure 4.7: Comparison of (a) V_{th} and SS, (b) DIBL comparison of conventional MOSFET and Modified NCFET [17].

Hence, the gate terminal loses the control over channel current. So, this effect should be decreased for better device performance. In **Figure 4.7(b)**, the calculated DIBL data is according to Equation (4.15) [22-25].

$$SS = \frac{k_B T}{q} \frac{d log_{10} I_D}{dV_{gs}} \qquad (4.14)\ [22]$$

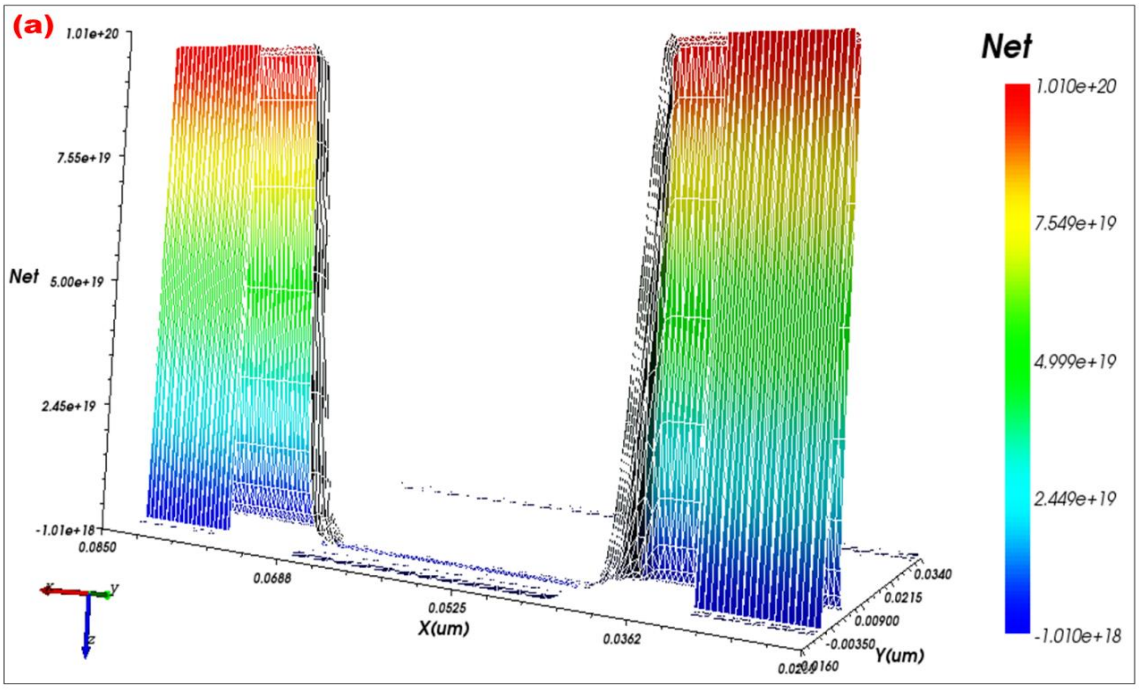
$$DIBL = \frac{V_{th_{V_{ds}=0.9\,V}} - V_{th_{V_{ds}=0.1\,V}}}{V_{ds=0.9\,V} - V_{ds=0.1\,V}} \qquad (4.15)\ [22]$$

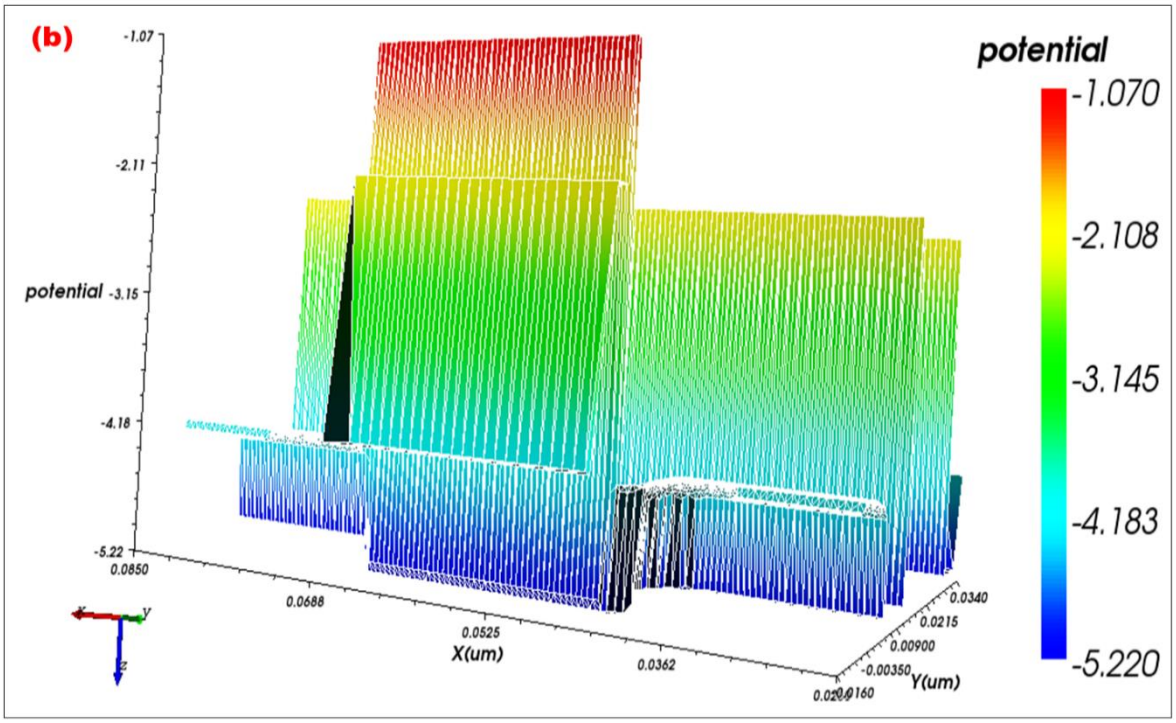
The conventional MOSFET and Modified NCFET structure are shown which shows the lower DIBL value for Modified NCFET over conventional MOSFET. All the extracted values of SCEs are inserted in Table 4.2.

Table 4.2: Comparison of SCEs in conventional MOSFET and Modified NCFET.

Short channel effects	Unit	Conventional MOSFET	Modified NCFET
V_{th}	V	0.34	0.26
DIBL	mV/V	0.086	0.078
SS	mV/dec	62.84	56.00

4.3.3 Analog/RF metrics





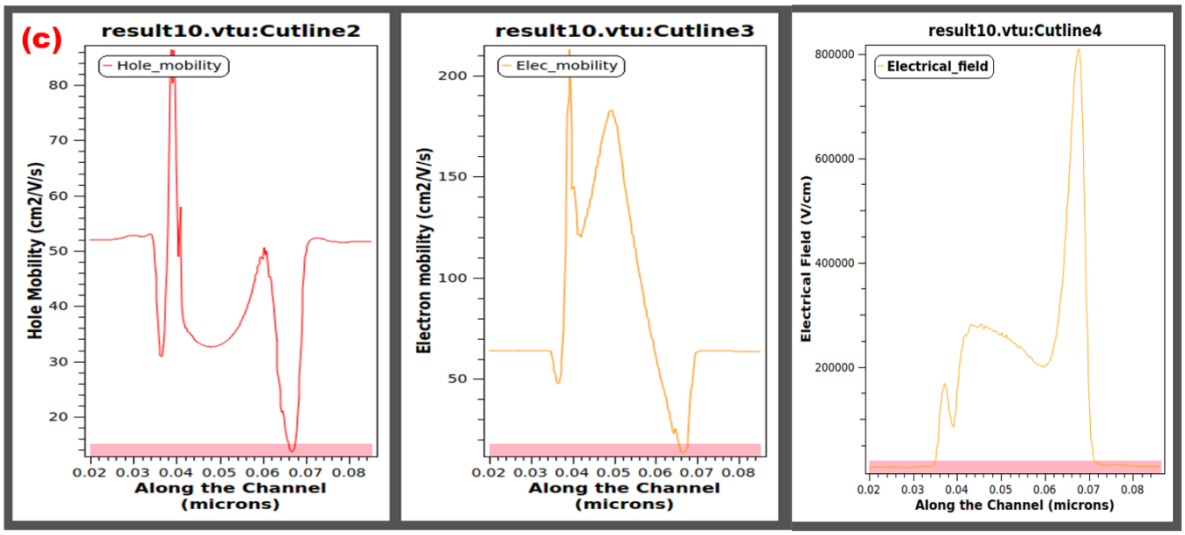


Figure 4.8: (a) Net charge (b) potential, (c) hole, electron mobility, and electric field across the channel region of Modified NCFET structure [17].

. At V_{ds} = 0.5 V and V_{gs} = 0.5 V, **Figure 4.8(a)** shows the net charge across the channel of Modified NCFET. The high intensity of charges is at the source and drain ends. **Figure 4.8(b)** shows the potential across the channel region of Modified NCFET at the same conditions and it indicates that the highest potential is at the channel region in comparison to the source/drain end. **Figure 4.8(c)** shows the electron and hole mobility variation with the cutline starting from the source end and going to the drain end. Again, **Figure 4.8(c)** shows the electrical field generated across the channel region from the source end to the drain end at V_{ds} = 0.5 V and V_{gs} = 0.5 V. Analog parameters and inverter applications are explored in this section of the study to compare the performance of Modified NCFET and traditional MOSFET. The results are simultaneously compared.As **Figure 4.6** makes it clear the Modified NCFET has a higher drain current than the conventional MOSFET device because of the negative capacitance phenomenon in NCFET. Related to drain current, transconductance defines the input conductance which is an essential parameter for the high-performance application[26]. From **Figure 4.9(a)**, it is clear that the g_m calculated according to Equation (4.16) for the Modified NCFET is higher than the conventional

MOSFET as the ON-current for the Modified NCFET is somewhat higher than the conventional MOSFET. Also, the transconductance generation factor (TGF) which is the ratio of gain generated per unit power loss. A high value of TGF calculated from Equation (4.17) indicates a high gain with less power loss which is a valuable factor for reliable application [27-31]. The modified NCFET's TGF value is higher than that of the traditional MOSFET which shows the better device application as expressed in **Figure 4.9(a)**

$$g_m = \partial I_d / \partial V_{gs} \quad (4.16)\ [11,12]$$

$$TGF = g_m / I_d \quad (4.17)\ [11,12]$$

$$QF = g_m / SS \quad (4.18)\ [11,12]$$

$$g_d = \partial I_d / \partial V_{ds} \quad (4.19)\ [11,12]$$

$$V_{EA} = I_d / g_d \quad (4.20)\ [11,12]$$

$$A_v = g_m / g_d = (g_m / I_d) \times V_{EA} \quad (4.21)\ [11,12]$$

$$f_T = g_m / 2\pi [C_{gs} + C_{gd}] \quad (4.22)\ [11,12]$$

$$GFP = (g_m / g_d) \times f_T \quad (4.23)\ [11,12]$$

$$GTFP = (g_m / g_d) \times (g_m / I_d) \times f_T \quad (4.24)\ [11,12]$$

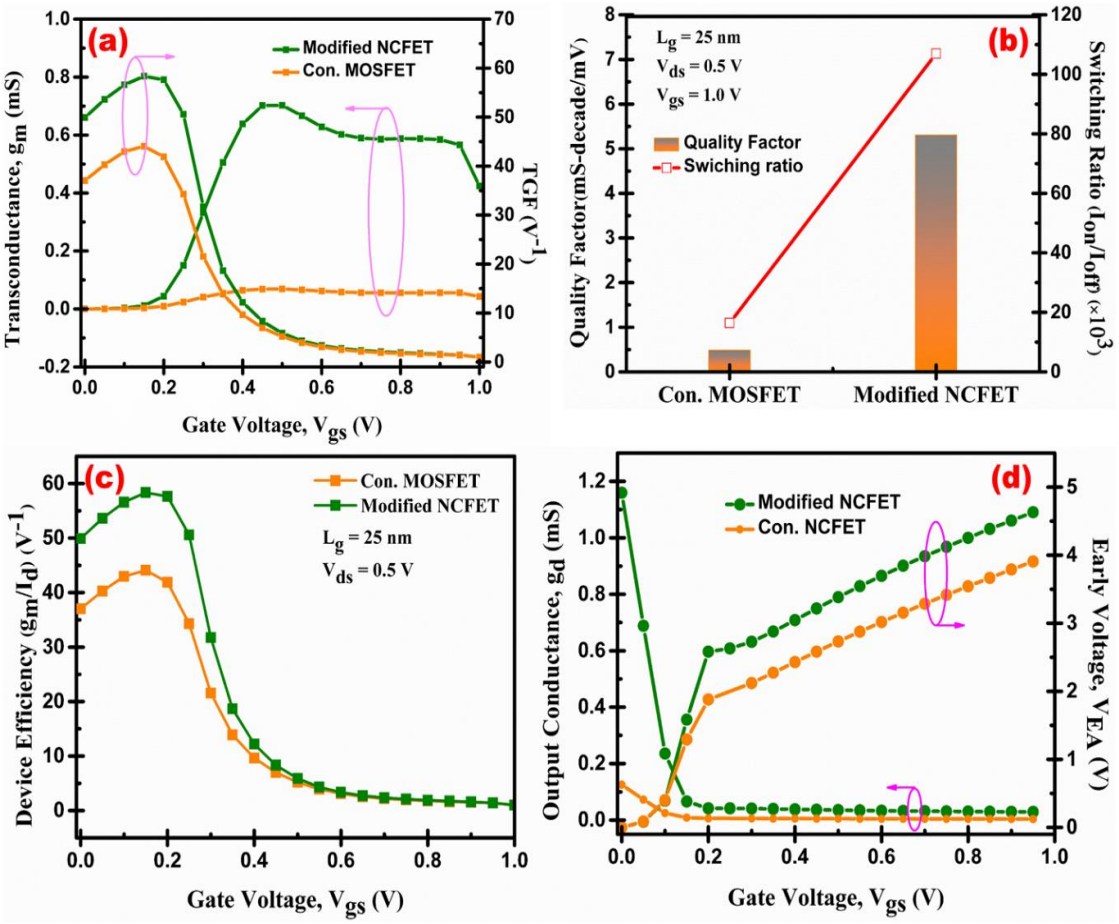
$$f_{max} = f_T / \sqrt{4R_g (g_{ds} + 2\pi f_T C_{gd})} \quad (4.25)\ [11,12]$$

On the other hand, the switching ratio (I_{ON}/I_{OFF}) also increases by one decimal point in the Modified NCFET (1.07×10^5) when compared to the conventional MOSFET (1.64×10^4) calculated from **Figure 4.6.** Also, it is further improved by the use of high-k dielectric material in the substrate region. Further, there is one more essential parameter that gives the device functioning in terms of current and SS called quality factor (QF) [32-35]. QF can be expressed as in Equation (4.18).For Modified NCFET, QF is 5.3 mS-dec/mV and for conventional MOSFET its value is 0.5 mS-dec/mV which is significantly better as shown in **Figure 4.9(b).** It is because of higher g_m in the case of Modified NCFET. Furthermore, another parameter that

connects g_m and I_d is device efficiency (g_m/I_d) which is higher for the Modified NCFET (58.33 V^{-1}) than the conventional MOSFET (44.07 V^{-1}) expressed in **Figure 4.9(c)**. Moving to **Figure 4.9(d)**, the variation of output conductance (g_d) according to Equation (4.19) and early voltage (V_{EA}) according to Equation (4.20) as a function of V_{ds} is shown at V_{gs} = 0.5 V. g_d and V_{EA} should be as high as possible for the gadget to have higher analog performance [33]. Because g_d measures the current driving ability of a device and V_{EA} is the source-drain resistance measurement. In this comparison work, we get these values high for the Modified NCFET structure. Further, we have the variation of cut-off frequency (f_T) with the V_{gs} at constant V_{ds} = 0.5 V in **Figure 4.9(e)**, f_T depends on the transconductance (g_m), gate-source capacitance (C_{gs}), and gate-drain capacitance (C_{gd}) as formulated below in Equation (4.22).

As the g_m is high for the Modified NCFET when compared to the conventional MOSFET, we get the f_T high for the Modified NCFET according to Equation (4.22). Moreover, for the better performance of a device, the intrinsic gain (A_V) should be high [36-38]. No matter what the bias point, A_V is a device's possible maximum voltage gain. The variation of A_V for both the device structures is shown in **Figure 4.9(e)** and it is clear that A_V for Modified NCFET is higher than conventional MOSFET according to Equation (4.21). **Figure 4.9(f)** shows the GFP and GTFP for the conventional MOSFET and Modified NCFET verifying that negative capacitance gives a better improvement to the device's performance according to Equation (4.23) and (4.24) [39-42]. **Figure 4.9(g)** despite the Maximum frequency for oscillation f_{max} for conventional MOSFET and Modified NCFET. It is higher for Modified NCFET in comparison to conventional MOSFET as the overall combination of g_{ds}, f_T, and C_{gd} is low for the previous device in comparison to the conventional device according to Equation (4.25) [43]. All these performance parameters are tabulated in Table 4.3. In NCFETs, the variation of parameters at higher voltage values differs significantly from MOSFETs due to the presence of the ferroelectric layer, which introduces negative

capacitance (NC) effects. At lower voltages, the NC effect amplifies the gate control, reducing the subthreshold swing (SS) and improving energy efficiency. However, at higher voltages, the behavior becomes more complex due to ferroelectric domain switching, saturation effects, and increased depolarization fields. The hysteresis and non-linearity of the ferroelectric material cause greater parameter shifts, leading to variations in threshold voltage, mobility, and capacitance. In contrast, traditional MOSFETs exhibit a more predictable scaling with voltage, primarily governed by oxide capacitance and short-channel effects. Additionally, in NCFETs, increased power dissipation at higher voltages further influence device characteristics, making their parameters more sensitive compared to MOSFETs at elevated operating conditions.



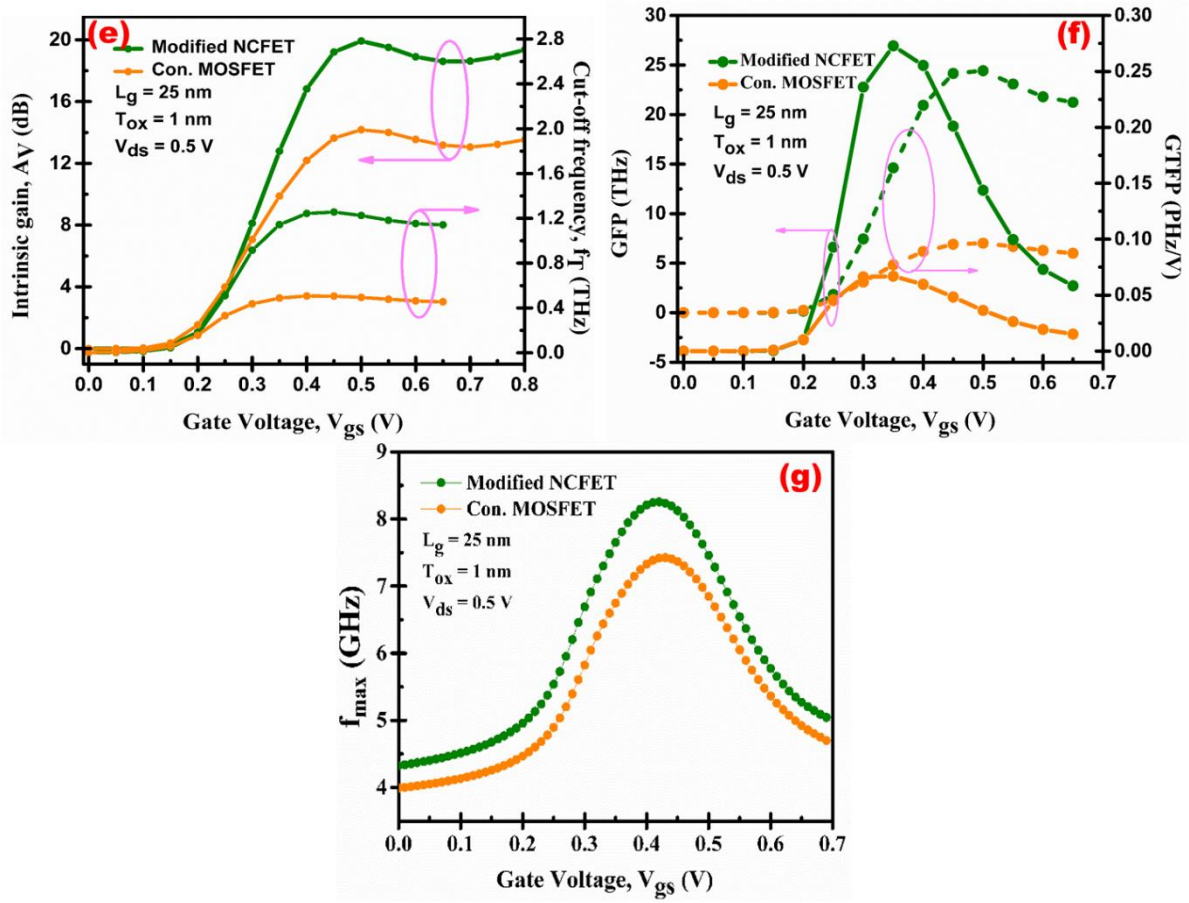


Figure 4.9: Variation of (a) g_m and TGF, (b) QF and I_{on}/I_{off} ratio, (c) device efficiency, (d) g_d and V_{EA}, (e) f_T and A_v, (f) f_{max} to V_{gs} for both configurations.

Table 4.3: Summary of the analog parameter of conventional MOSFET and Modified NCFET.

Parameter	Unit	Conventional MOSFET	Modified NCFET
I_{on}/I_{off}	-	1.64×10^4	1.92×10^5
g_m	mS	0.11	0.71
TGF	V^{-1}	41.07	58.33
QF	mS-dec/mV	0.5	5.1
Device Efficiency	V^{-1}	43	59
g_d	mS	0.13	1.16
V_{EA}	V	3.90	4.63
f_T	THz	0.50	1.25
A_V	dB	14.18	19.92
f_{max}	THz	7.3	8.4

4.3.4 Comparison of Conventional MOSFET-based inverter and Modified NCFET-based inverter

Combinational circuits are in high demand nowadays because of their high switching speed and their low power consumption. For better digital applications, combinational circuits are the first choice. To meet the objectives, several designs of MOSFETs are explored and the Modified NCFET is one of them. In this section of the Chapter, we discuss the voltage-transfer curve of a conventional MOSFET-based inverter and a Modified NCEFT-based inverter. Firstly, **Figure 4.10(a)** shows the schematic structure of a MOSFET-based inverter. So, in this architecture, we need two types of components. One is the n-channel component and the other is the p-channel component, both are connected with the 10 nm SiO_2 spacer. To work as the circuit of the inverter, the components of this structure should be such that their threshold voltage is the same so that there is no break point in the working of the circuit when we change the applied voltage from -1 V to +1 V. As regular CMOS based inverter circuit, V_{gs} = 0 V is the breakpoint for the circuit where the working component changes.

When V_{gs} = -1 to 0 V, at that particular time, p-channel Modified NCFET works and gives the output, and when V_{gs} = 0 to +1 V, then the working component is n-channel Modified NCFET. So, the threshold voltage for both components should be the same so that the complete circuit works smoothly. For matching the V_{th}, we should change the work functions of both gate contacts (Poly-Si) simultaneously. Poly-Si is used as the gate contact with 4.50 eV and 4.95 eV work functions for n-type and p-type channel components respectively. The plot for the threshold match is shown in **Figure 4.10(b).** This architecture is presented using the COGENDA VISUAL TCAD simulator We simulated the results for both compared device-based inverters in the form of VTC plots.

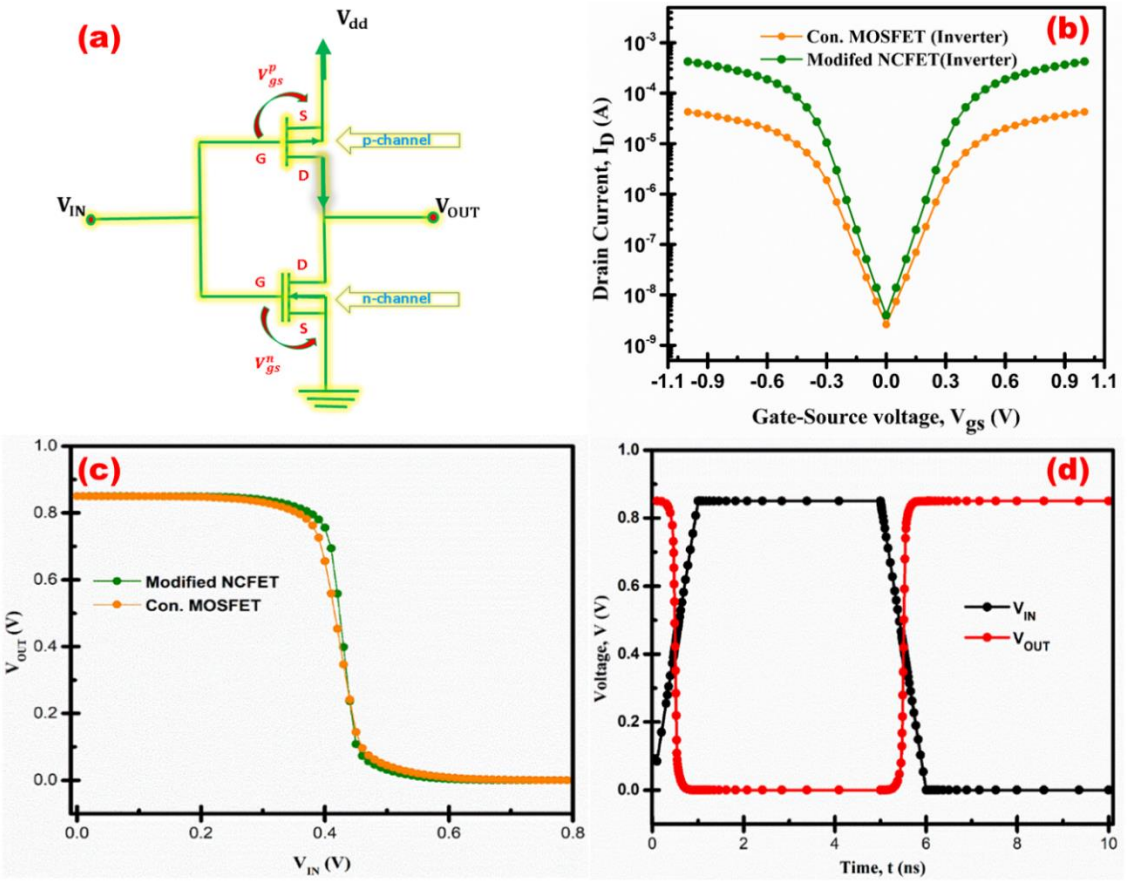


Figure 4.10: (a) Schematic diagram of MOS-based inverter, (b) Threshold voltage matching, (c) VTC curve for both configurations, (d) The transient curve for a Modified NCFET-based inverter [17].

Further, the transfer characteristic curves of conventional MOSFET-based inverter and Modified NCFET-based inverters are shown in **Figure 4.10(b)** to match their threshold voltage. With a dual work function metal (DWFM) integration scheme, V_{gs} varies from -1 V to +1 V at constant V_{ds} = 0.5 V. The VTC comparison curve of the conventional MOSFET-based inverter and Modified NCFET-based inverter is plotted in **Figure 4.10(c)** [44]. From the plot, we can prove that the transition region (TR) for the Modified NCFET-based inverter is significantly sharper than the conventional MOSFET-based inverter which gives it better speed and fast switching.

Noise margin calculation: The transfer region in the VTC curve of a MOSFET-based inverter is a crucial region that plays a significant role in digital logic operation. The VTC

curve represents the relationship between the input voltage (V_{IN}) and the output voltage (V_{OUT}) of the inverter. The transfer region, sometimes referred to as the "active region," is the part of the VTC where the NCFET-based inverter operates as a digital logic gate, it should be low for a quick response of the circuit. On this VTC curve, there are two important critical points where the slope of this curve becomes -1. One point corresponds to logic 0 called maximum input voltage (V_{IL}) and the other corresponds to logic 1 denoted as minimum input voltage (V_{IH}). The threshold voltage in the case of the inverter circuit is the voltage point at which $V_{in} = V_{out}$ or the transition voltage on the VTC curve. In these cases, the V_{th} for conventional MOSFET is 0.41 V and for Modified NCFET, it is 0.43 V. In digital logic circuits, the transfer region corresponds to the range of input voltages where the inverter properly interprets the input as either a logic high (1) or a logic low (0) output. This region is where the inverter performs its primary logic function of signal inversion. The transition region for conventional MOSFET is 0.20 V whereas, for Modified NCFET, it is 0.15 V. The transition from one logic level to another in the transfer region of the NCFET-based inverter is relatively quick. It is important for minimizing the propagation delay between the input and corresponding output curve of the FET-based digital circuits. A well-defined transfer region helps in achieving fast switching times. It is a fundamental characteristic that designers consider when designing and optimizing digital circuits to ensure proper logic operation, noise immunity, and signal integrity. The output signals should be clear from noise signals for better circuit performance. That is why we always calculate the noise margin which gives the extraction of noises from output signals. The noise margin is a crucial parameter in the design and analysis of MOSFET-based inverters and other digital logic gates. It plays a significant role in ensuring the reliability and robustness of digital circuits. And it should be as high as possible. It allows for tolerance in voltage levels so that devices with slightly different voltage levels can still interface

correctly. It is given below for low signal levels (NM_L) and high signal levels (NM_H) in Equation (4.26) and (4.27) [45]:

$$NM_L = V_{IL} - V_{OL} \quad (4.26)\ [12]$$

$$NM_H = V_{OH} - V_{IH} \quad (4.27)\ [12]$$

When input levels are logic 1 and logic 0, respectively, V_{IL} and V_{IH} are the minimum and maximum input voltages.

Table 4.4: Noise margin comparison between inverters using Modified NCFETs and Conventional MOSFETs

Parameter	Unit	Conventional MOSFET	Modified NCFET
V_{IL}	V	0.32	0.35
V_{IH}	V	0.52	0.50
V_{OL}	V	0.022	0.031
V_{OH}	V	0.83	0.82
NM_L	V	0.29	0.32
NM_H	V	0.31	0.32
TR	V	0.20	0.15

Similar to this, when output levels are logic 0 and 1, respectively, V_{OL} and V_{OH} are the minimum and maximum output voltages. The NM_L for a conventional MOSFET-based inverter is 0.29 V and 0.32 V for a Modified NCFET-based inverter. And NM_H for conventional MOSFET and Modified NCFET are 0.31 V and 0.32 V, respectively. Achieving a high noise margin in a MOSFET-based inverter is essential for designing robust digital circuits that can tolerate noise and variations in input voltage levels while maintaining reliable logic operation. A high noise margin implies that the circuit can handle noise and still provide a clear distinction between logic high and logic low levels.

Noise margin is critical for ensuring that different components and devices in a digital system can communicate effectively. It allows for tolerance in voltage levels so that devices with slightly different voltage levels can still interface correctly. Semiconductor

manufacturing processes can result in variations in device characteristics. Noise margin accounts for these process variations, making the circuit more robust and less susceptible to manufacturing-related inconsistencies. **Figure 4.10(d)** shows the transient analysis for the Modified NCFET-based inverter. The drift-diffusion method solver level 1 (DDML1) technique is used for all the simulations which are carried out at room temperature. The calculated and improved values are tabulated in Table 4.4.

4.4 SUMMARY

A Quantum ATK and VISUAL TCAD simulator-based insight for Si-doped HfO_2 NCFET using ferroelectric material is considered. Modified NCFET shows amplified results with high ON-current and a better switching ratio of 1.7×10^5. In addition, Modified NCFET suppresses the short channel effects like threshold voltage decreased by 23.75%, and SS reduced by 8.92% compared to conventional MOSFET. Also, the analog parameters of Modified NCFET over conventional MOSFET show improved results. The transconductance of Modified NCFET increased by 34.75% in comparison to the conventional MOSFET structure. Quality factor and device efficiency of Modified NCFET improved by three decimal points and 32.36%, respectively concerning conventional MOSFET structure. Moreover, the cut-off frequency and intrinsic gain show amplified results with 150 times increment and 40.48% results when compared to conventional MOSFET. Better analog performance parameters and reduced short channel effects make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular MOSFET. Furthermore, when we talk about the digital applications like inverters of both these device structures, the noise margin for Modified NCFET comes out to be high when compared to the conventional MOSFET device structure. Its value is 0.32 V for Modified NCFET and 0.31 V for conventional

MOSFET structure from the VTC plot. Better analog performance parameters, reduced short channel effects, and higher noise margin make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular MOSFET.

Following a comprehensive analysis of the analog and RF characteristics of the Modified NCFET, it is imperative to address the reliability concerns associated with this proposed device. Therefore, to ensure the device's reliability, it is crucial to explore its characteristics, taking into account the temperature variations, which will be the primary focus area of the next chapter.

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5

CHAPTER

DFT-based Atomic Modeling and Temperature Analysis on the RF and VTC curve of high-k dielectric layer-assisted NCFET

- *This chapter discusses the Density Functional Theory (DFT) based atomic modeling of hafnia and silicon-based hafnium oxide.*
- *DFT parameters like Bandgap, Hartree potential, and PDOS for silicon-based hafnium oxide are better than hafnia.*
- *Further, the analog performance comparison of Modified NCFET, and conventional NCFET is discussed.*
- *It was found that the switching ratio of the Modified NCFET increased by almost one decade, thereby improving the Subthreshold swing value compared to the conventional NCFET.*
- *The analog performance in terms of transconductance, transconductance generation factor, output conductance, and early voltage compared to conventional NCFET.*
- *It is also analyzed that the Modified NCFET exhibits the most improved static performance compared to the conventional NCFET configuration. Also, the inverter-based parameters like NM ratio and propagation delay are improved in the case of a Modified NCFET-based inverter.*
- *Consequently, the proposed Modified NCFET device would be an attractive solution for low-power and high-performance CMOS circuits.*

The advantage of using the HfO_2 as BOX and a ferroelectric material in the gate stack of Modified NCFET over the conventional MOSFET structure is discussed in **Chapter 4.** Further, to improve the device's characteristics, the layer of high-k dielectric material (HfO_2) in combination with SiO_2 can be used in the gate stack. Also, temperature analysis is considered in this chapter for the reliability of architecture.

5.1 INTRODUCTION

Continuing Chapter 3, we will further modify the device architecture by adding the high-k dielectric material (HfO_2). Using high-k dielectric materials in the gate stack of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) represents a pivotal advancement in semiconductor technology, particularly as device dimensions continue to shrink following Moore's Law [1]. Traditional gate dielectrics, such as silicon dioxide (SiO_2), face significant limitations as MOSFETs scale down to nanometer dimensions. High-k dielectric materials offer a range of benefits that address these limitations, ensuring that MOSFETs continue to perform efficiently and reliably even as they become smaller. This section explores the benefits of high-k dielectric materials in the gate stack of MOSFETs, highlighting their role in reducing gate leakage current, increasing gate capacitance, enabling scalability, reducing power consumption, enhancing threshold voltage control, and improving overall device reliability [2].

One of the most significant benefits of using high-k dielectric materials in the gate stack is the reduction in gate leakage current. As FET dimensions shrink, the gate oxide layer must also become thinner to maintain the necessary gate capacitance for proper device operation. However, when the gate oxide becomes extremely thin on the order of a few nano-meters quantum tunneling effects become significant, leading to increased leakage currents. This leakage not only causes higher power consumption but also compromises the

reliability and longevity of the device [3]. High-k dielectric materials, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), and aluminum oxide (Al_2O_3), have a dielectric constant significantly higher than that of SiO_2. This property allows for a physically thicker gate dielectric layer while maintaining the same or even higher gate capacitance. A thicker dielectric layer reduces the probability of electron tunneling through the gate, thereby reducing the gate leakage current. The reduction in leakage current is crucial for low-power applications, particularly in mobile and portable devices where battery life and energy efficiency are paramount [4].

Gate capacitance is a critical parameter in MOSFET design, as it directly influences the electrostatic control of the channel, which determines the device's switching speed and drive current. The capacitance of a parallel plate capacitor, which is a good model for the gate structure, is given by Equation (4.1):

$$C = \frac{k\mathcal{E}_0 A}{d} \qquad (5.1)\ [3]$$

Where C is the capacitance, k is the dielectric constant, $\mathcal{E}_0$ is the permittivity of free space, A is the area of the capacitor plates (gate area), and d is the separation between the plates (dielectric thickness). In this Equation, increasing the dielectric constant k allows for a higher capacitance without decreasing the thickness d. High-k dielectrics enable a thicker physical layer, which helps to maintain a high gate capacitance necessary for strong electrostatic control of the channel in scaled devices. This improved gate control leads to higher drive currents and faster switching speeds, enhancing the overall performance of the MOSFET. Furthermore, as semiconductor technology advances, there is a continuous push to scale down the dimensions of MOSFETs to pack more transistors onto a single chip, following Moore's Law. Traditional SiO_2 gate dielectrics, however, face a fundamental

scaling limit due to the issues mentioned above, particularly increased leakage currents as the oxide thickness decreases.

High-k dielectric materials enable continued scaling of MOSFETs by allowing for a thicker physical dielectric layer that still meets the electrical requirements of a scaled device. This scalability is essential for maintaining device performance, power efficiency, and reliability in advanced technology nodes. Without high-k materials, it would be challenging to achieve the levels of integration and performance required for modern electronics. Moreover, power consumption is a critical consideration in the design of modern electronic devices, especially in mobile and portable applications where battery life is a key factor. High-k dielectrics contribute to power savings in several ways [5-8]. First, by reducing gate leakage current, they directly reduce static power consumption, which is a significant portion of the total power budget in nanometer-scale MOSFETs.

As the increased gate capacitance provided by high-k materials improves the electrostatic control of the channel, which can allow the device to operate at a lower threshold voltage (V_{th}) and supply voltage (V_{dd}). Operating at a lower voltage reduces the dynamic power consumption, which is proportional to the square of the supply voltage. This reduction in both static and dynamic power consumption extends battery life and reduces heat generation, which is critical for the reliable operation of densely packed circuits.

High-k dielectric materials, when used in conjunction with metal gates, allow for better tuning of the threshold voltage. The metal gate can be chosen or engineered to have a specific work function that, in combination with the high-k dielectric, sets the desired V_{th}. This capability is particularly important in advanced technologies where multiple threshold voltages may be required across different parts of an integrated circuit to optimize performance and power efficiency.

Also, Temperature has a significant impact on the performance and reliability of transistors, including both MOSFETs and Bipolar Junction Transistors (BJTs). Understanding these effects is crucial for designing reliable electronic circuits, especially in environments where temperature variations are common.

It is concluded from the above discussion, that the integration of high-k dielectric materials in the gate stack of Modified NCFET represents a critical technological advancement that addresses the challenges associated with scaling down transistor dimensions. These materials provide significant benefits, including reduced gate leakage current, increased gate capacitance, enhanced scalability, lower power consumption, improved threshold voltage control, and greater reliability [5,7]. So, this chapter includes the advantage of high-k dielectric (HfO_2) material in the gate stack of Modified NCFET as discussed in **Chapter 4**. The following outline constitutes this chapter's structure: In the second section, the Modified NCFET is discussed with the physical models used in the simulation work. The third section includes the DFT calculation for hafnium oxide and silicon-based hafnium oxide. The later part of the chapter discusses the results obtained through simulation. The temperature analysis of the Modified NCFET is performed with the VISUAL TCAD simulator. The temperature range is taken from 250 K to 350 K. The impact of temperature on the NCFET-based inverter is also discussed in this work with NM calculations. This architecture is based on the practical device design, which can make energy-efficient equipment by regulating material parameters. The conclusion of the chapter is presented in the final part of the chapter's summary.

5.2 DEVICE DESIGN AND PHYSICAL MODELS

Figure 5.1(a) represents the proposed Modified NCFET structure with Si-HfO_2 ferroelectric material with a high-k dielectric layer of HfO_2 in gate stack and HfO_2 as BOX

[9]. A VISUAL TCAD simulator is used to perform all the numerical simulations of temperature analysis presented in this work. For the simulation of silicon regions and the ferroelectric region in n-type architecture, 2D electrostatics is used. The Modified NCFET has buried oxide (HfO_2) with a thickness of 20 nm in the substrate region with the addition of a ferroelectric material layer (HfO_2FE) in the gate stack. In the gate stack, the layers of (SiO_2 + HfO_2) are taken as gate oxide with a thickness of 1nm and the silicon-based ferroelectric layer (HfO_2FE) has a thickness of 2.5 nm. As both the architectures are of n channel type, the substrate regions are doped with the p-type impurities having a concentration of 1×10^{16} cm^{-3}. The extensions of the source/drain with Gaussian doping of 1×10^{19} cm^{-3} are used to reduce the parasitic capacitance. The gate length of 25 nm is used for both the device structure.

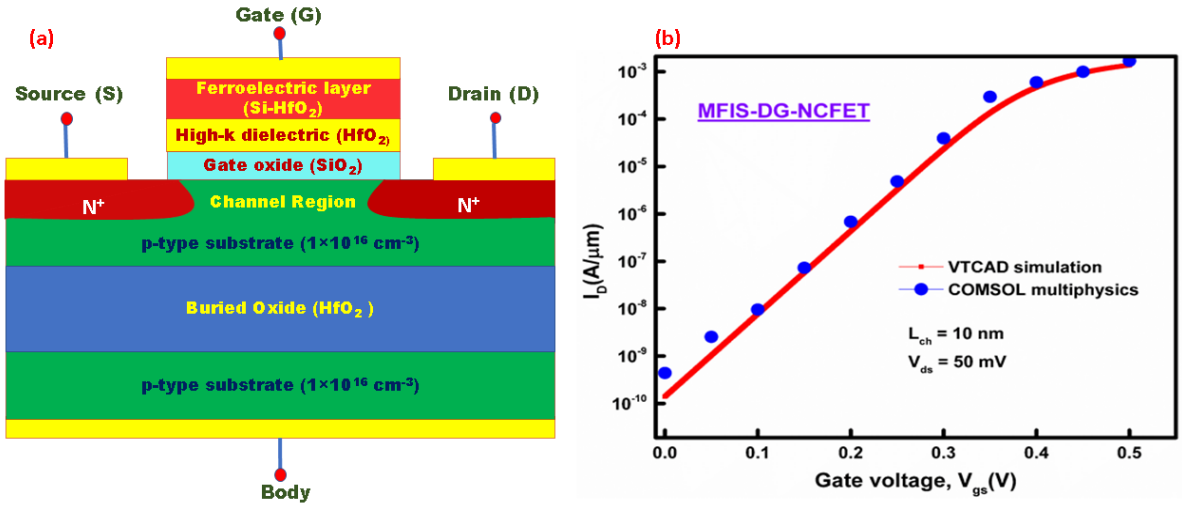


Figure 5.1: (a) The Modified NCFET device schematic architecture. (b) Calibrated I_D-V_{gs} of metal-ferroelectric-insulator-semiconductor double gate NCFET on VTCAD simulator with published results on COMSOL Multiphysics [9].

These device simulation parameters are tabulated in Table 4.1. The drift-diffusion formulation in Fermi-Dirac statistics, which defines the electrical transport in the silicon region of architecture, is explained in **Chapter 4.**

Landau's theory for ferroelectrics provides a phenomenological approach to understanding the phase transition from a paraelectric to a ferroelectric state. The theory

hinges on the concept of an order parameter, which in the context of ferroelectrics is the spontaneous polarization P. The central idea is to express the free energy (F) as a power series expansion in terms of this order parameter, assuming it is small near the phase transition [10, 11]. The free energy (F) near the phase transition can be expressed as Equation (5.2):

$$F(P,T) = F_0 + \frac{\alpha(T)}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - EP \quad (5.2)\ [10,11]$$

Here, F_0 is the free energy of the reference paraelectric phase, (T) is a temperature-dependent coefficient, β and γ are higher-order coefficients, and E represents the applied electric field. The temperature dependence of (T) is critical and is typically modeled as Equation (5.3):

$$(T) = \alpha_0(T-T_c) \quad (5.3)\ [10,11]$$

where α_0 is a positive constant and T_c is the Curie temperature. Above T_c, (T) is positive, leading to a minimum of the free energy at P=0, which corresponds to the paraelectric phase. Below T_c, α(T) becomes negative, causing the free energy to develop minima at non-zero values of P, indicating the presence of spontaneous polarization characteristic of the ferroelectric phase. The spontaneous polarization (P) in the ferroelectric phase can be found by minimizing the free energy with respect to P as Equation (5.4):

$$\frac{dF}{dP} = \alpha(T)P + \beta P^3 + \gamma P^5 - E = 0 \quad (5.4)\ [10,11]$$

In the absence of an external electric field (E=0), this equation shows that below T_c, P takes on non-zero values, indicating a spontaneous polarization. The nature of this phase transition, whether it is first-order (discontinuous) or second-order (continuous), depends on the signs and magnitudes of the coefficients β and γ.

If β>0, the transition is second-order, and P changes continuously from zero at T_c to a non-zero value as the temperature decreases. If β<0 and γ>0, the transition is first-order,

characterized by a discontinuous jump in P at T_c. Landau's theory is particularly valuable for understanding the general features of ferroelectric phase transitions, such as the temperature dependence of polarization and the nature of the transition (first- or second-order). It provides a framework for predicting the behavior of ferroelectrics under various conditions, including temperature changes and applied electric fields. While Landau's theory is phenomenological and does not delve into microscopic details, its simplicity and versatility make it a fundamental tool in the study of ferroelectric materials.

Further, to calculate the energy values of HfO_2 using the Linear Combination of Atomic Orbitals (LCAO) approximation in QATK, the general LCAO approximation to perform such calculations is spin and is unpolarized (not distinguishing between the two possible spin states of electrons), Generalized Gradient Approximation (GGA) exchange-correlation (describe the exchange and correlation effects in terms of electron density gradients.

Table 5.1: Default device dimensions and parameters of conventional NCFET and Modified NCFET structure are taken for the simulation.

Parameter	Unit	Conventional NCFET	Modified NCFET
$\mathbf{L_g}$	nm	25	25
$\mathbf{L_{S/D}}$	nm	10	10
$\mathbf{T_{ox}}$	nm	1	1
$\mathbf{T_{FE}}$	nm	2.5	2.5
$\mathbf{T_{ins}}$	nm	0	20
$\mathbf{N_{S/D}}$	cm^{-3}	1×10^{19}	1×10^{19}
$\mathbf{N_{ch}}$	cm^{-3}	1×10^{16}	1×10^{16}
$\mathbf{\Phi_m}$	eV	4.5(N-Poly-Si)	4.5 (N-Poly-Si)

It is an improvement over the simpler Local Density Approximation (LDA) and adds a dependence on the gradient (or first derivative) of the electron density, Fermi-Dirac occupation (to determine how many electrons occupy each molecular orbital or energy

level), and density mesh cut-off at 125 Hartree (determines the energy range). The supply voltage of 0.5 V is used for all the simulation work [12].

The calibration of simulated work on VISUAL TCAD with the published work on COMSOL Multiphysics by Girish Pahwa et al. **Figure 5.1 (b)** presents the calibrated transfer characteristics of both simulators.

5.3 RESULTS AND DISCUSSION

5.3.1 DFT-based Atomic Calculation of Hafnium Oxide (HfO_2) and Si-HfO_2

Silicon-based hafnia (Si-HfO_2) can exhibit a different bonding nature compared to pristine hafnia due to the introduction of silicon (Si) atoms into the crystal lattice. The exact bonding nature in silicon-doped hafnia can depend on several factors, including the concentration of silicon dopants and the local environment of the dopants. One will find a combination of ionic and covalent bonding in pristine hafnia and silicon-doped hafnia [13]. Hafnia inherently comprises hafnium (Hf) and oxygen (O) atoms. Silicon is also a non-metal. The electronegativity difference between Hf and O leads to ionic bonding, while covalent bonds exist between Hf and O atoms. Introducing silicon into the lattice does not change the basic ionic and covalent bonding characteristics. The dimension of simple cubic HfO_2-based ferroelectric is a=10.23A, b=10.23A, c=10.23A, α =90, β = 90, γ =90. The structure has four hafnium (Hf) atoms and eight oxygen (O) atoms without doping. For silicon (Si) doping, 25% of Si is added, as shown in **Figure 5.2(a).** Using this Si-doped HfO_2 in gate stacking of the device governs the negative capacitance effect.

Quantum Atomistic Tool Kit (QATK) is one such tool kit that can perform electronic structure calculations for molecules and materials. **Figure 5.2(b)** shows the band structure of simple cubic HfO_2 structure (a) and 25% Si-based HfO_2 (b). It was discovered

that the direct bandgap of HfO_2 reduced significantly from 2.81eV to 0.35eV by 25% Silicon doping with two-fold degeneracy.

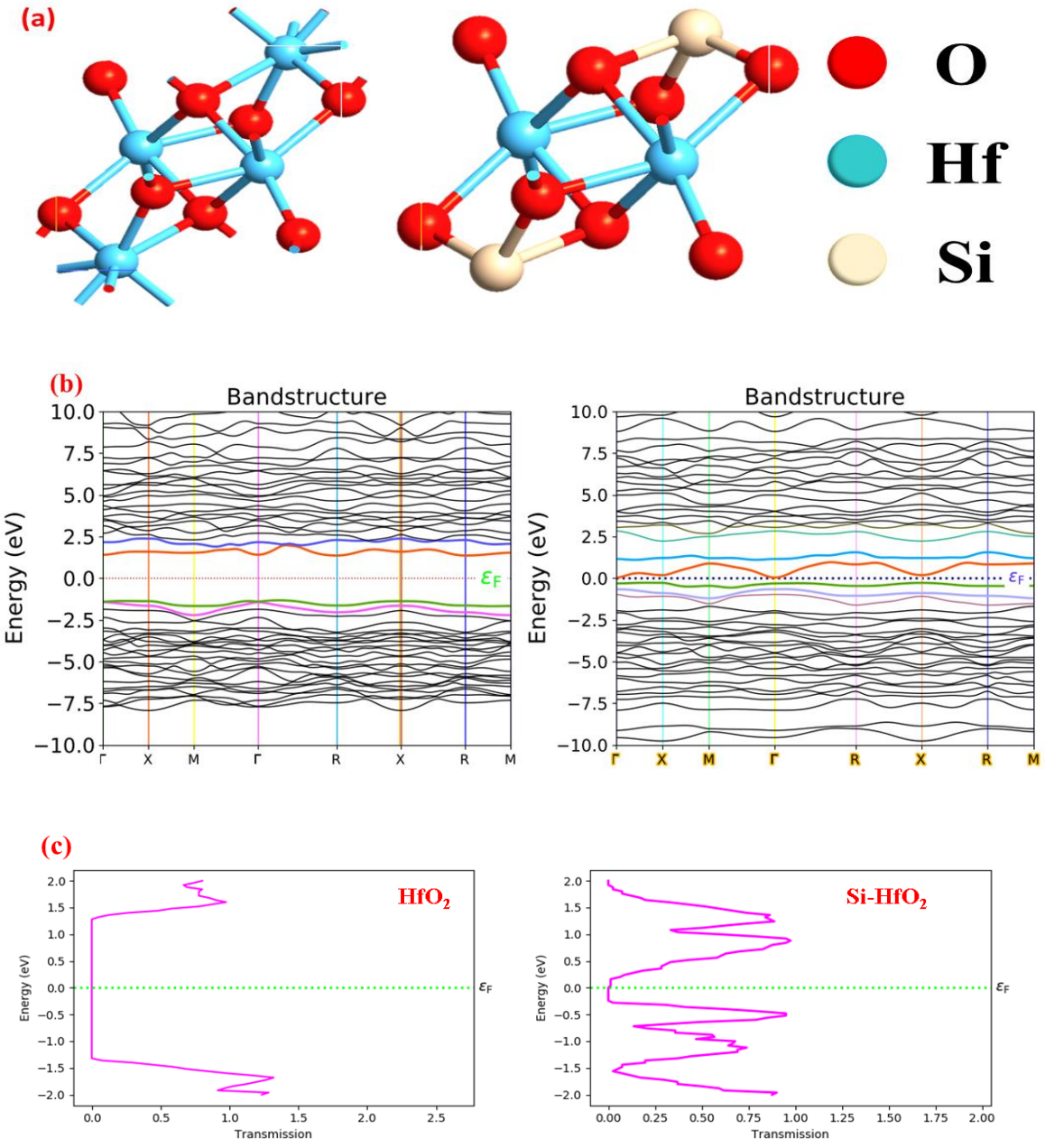


Figure 5.2: (a) Structure, (b) band structure, and (c) transmission spectra with the energy of HfO_2 and Si-HfO_2 [9].

Further, **Figure 5.2(c)** shows the transmission spectra corresponding to hafnium oxide with or without silicon doping. The transmission peaks increase as the doping of silicon increases, which is why the conduction in Si-doped HfO_2 is much higher than the without-

doped HfO_2 [15]. Pure HfO_2 has a wide bandgap. Si doping introduces Si-O bonds, which can alter the electronic structure. Higher Si doping (>10%) can reduce the bandgap due to defect states and oxygen vacancies, leading to lower energy, and longer wavelength. Also, silicon incorporation can transform amorphous HfO_2 into a more stable phase with reduced light scattering. This structural modification enhances the overall transmission of the material. High Si content can introduce localized states within the bandgap. This can create additional absorption peaks, reducing transmission in certain wavelengths. In this case, the author marks the zero-energy level at the Fermi energy level. However, the zero-energy level is a reference point used to measure energies in a system. In contrast, the Fermi energy level is a material-specific concept that describes the highest energy level occupied by electrons at absolute zero temperature. The Fermi energy level is crucial for understanding the behaviour of electrons in materials and their electrical and thermal properties. In-band structure diagrams, specific colours are often used to represent different energy bands or states within a material. The green colour band represents the highest energy valence band, and the red one shows the lowest conduction band. The difference between these two bands is the bandgap for the corresponding structure, which is 2.81 eV in the case of HfO_2 and 0.35 eV for 25% Si-doped HfO_2.

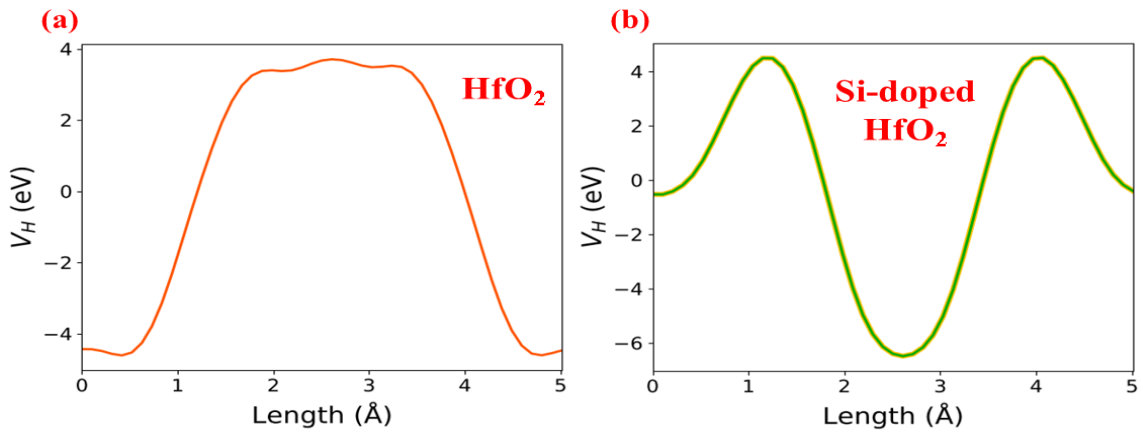


Figure 5.3: The Hartree potential of (a) HfO_2 and (b) Si-doped HfO_2 [9].

Silicon states enhance the bandgap and a comparable bandgap changes along the direction for all the lower concentrations of silicon atoms [16]. Tran Blaha Modified Becke Johnson (TB-mBJ) is used to calculate the electron band structure of the atom accurately.

Figure 5.3 shows the variation of the Hartree potential with length for both atoms. The lower the Hartree potential of an atom, the more stable the atom. So, the Si-doped HfO_2 is more stable than the HfO_2 atom. It takes less time to move from one orbit to another. It reveals the mean electrostatic interaction between the atoms. Poisson's Equation is helpful for the calculation of this electrostatic potential [17]. The Hartree potential curve of hafnium oxide (HfO_2) is not strictly sinusoidal because it is influenced by the complex crystal structure, ionic potentials, and electron distribution rather than a simple periodic function. Unlike an idealized cosine wave, which represents a uniform periodic potential, the actual electrostatic potential in HfO_2 is shaped by:

1. Atomic Potential Asymmetry: HfO_2 has a monoclinic crystal structure, meaning the atomic arrangement is not perfectly periodic like a simple sine wave. Also, Hf and O atoms have different electronegativities, causing asymmetric charge distribution and altering the electrostatic potential.

2. Bond Strength Variation: The Hf-O bonds have different lengths in different crystallographic directions, leading to unequal potential depths across the lattice. This results in a distorted oscillatory potential, rather than a perfect sinusoidal wave.

3. Defects and Localized States: Intrinsic defects, such as oxygen vacancies, introduce local potential wells, further distorting the smooth oscillations expected in an ideal crystal.

Figure 5.4 shows the projected density of states concerning energy levels. It represents the particular density of states like spin-up and spin-down states.

The projected DOS for Si-doped HfO_2 is much more dense and higher than the HfO_2 without doping. The contribution of induced silicon atoms in the lower conduction and valance bands shows the hybridization in the orbits. Hence, the magnitude and peaks increase as the concentration of the silicon atoms increases [18].

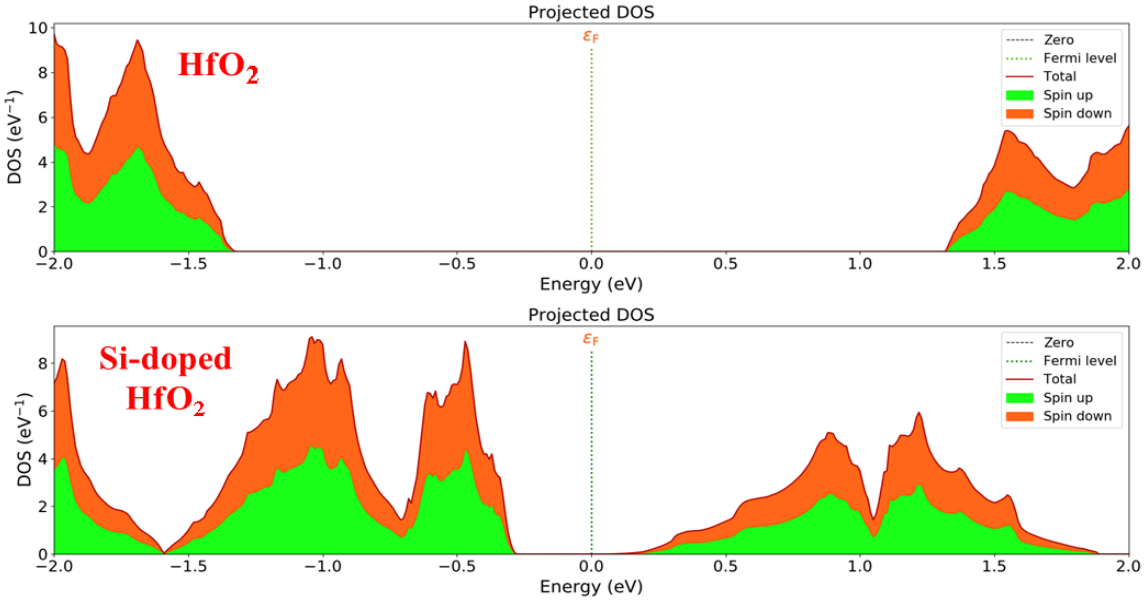


Figure 5.4: The projected DOS of HfO_2 and Si-HfO_2 [9].

5.3.2 SCEs analysis between conventional NCFET and Modified NCFET

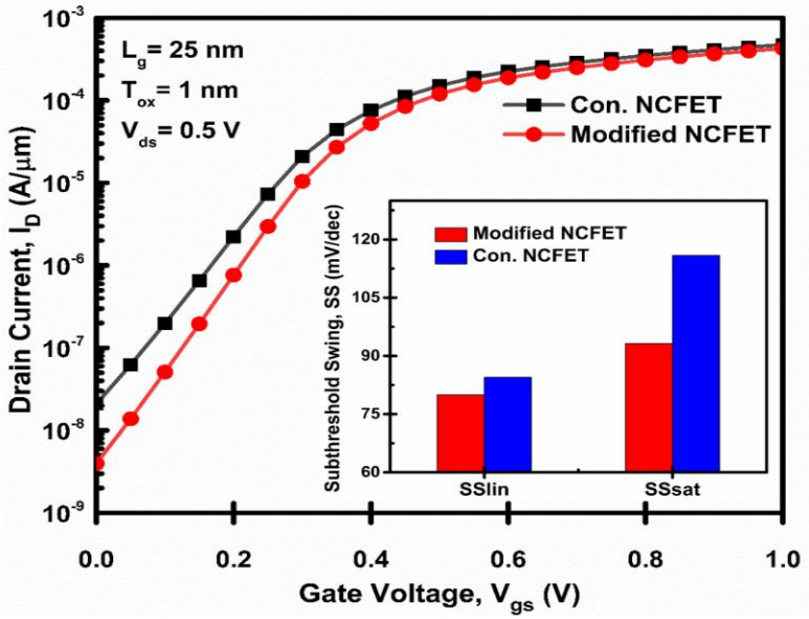


Figure 5.5: Transfer characteristic and Subthreshold Swing (inset) comparison of conventional NCFET and Modified NCFET at a drain-source voltage of 0.5V [9].

The parameters of conventional NCFET and Modified NCFET structures are already discussed in Section 2. **Figure 5.5** shows the performance parameter in the form of drain current (I_D) concerning the gate voltage (V_{gs}). This variation shows that the leakage current (I_{OFF}) is reduced significantly in the Modified NCFET structure. The Modified NCFET contains the BOX part in the substrate region, which acts as the barrier to the mobile electrons in the silicon part of the substrate region. Due to this, the leakage current is reduced, which directly increases the device's switching ratio (I_{ON}/I_{OFF}). Further, as the effect of negative capacitance, the SS value decreased, but more decrement in the SS value happened due to the layer of the BOX layer in the substrate region of the Modified NCFET structure, as shown inset of **Figure 5.5**.

5.3.3 Analog/RF Performance Metrics at different temperatures

The presence of the ferroelectric material introduces an additional capacitance C_{FE} in series with the conventional MOSFET gate capacitance C_{MOS}, leading to negative capacitance (NC) effects that can amplify the gate voltage. In NCFETs, capacitances vary significantly with temperature due to the ferroelectric layer's temperature-dependent properties. The key capacitances in NCFETs include (C_{gs}), gate-to-drain capacitance (C_{gd}), and oxide capacitance (C_{ox}), which are influenced by the ferroelectric capacitance (C_{FE}) as described in **Figure 3.1(b)** and **4.1**. As temperature increases, the permittivity of the ferroelectric material decreases, leading to a reduction in C_{FE}. This affects the total gate capacitance, as the series combination of C_{FE} and C_{ox} determines the device's overall capacitance. A decline in C_{FE} weakens the negative capacitance effect, reducing the subthreshold slope improvement and potentially affecting the threshold voltage. Moreover, temperature variations impact polarization switching dynamics, which can lead to increased leakage currents, and reduced ON-state current. References such as Salahuddin & Datta (2008) and experimental studies on Hafnium-based ferroelectrics highlight that temperature variations must be carefully managed to maintain the performance benefits of NCFETs. Thus, proper thermal stability considerations, such as material engineering and operating condition optimizations, are essential for reliable NCFET operation. The transfer characteristics (I_D-V_{gs}) in linear scale for Modified NCFET for temperatures ranging from 250 K to 350 K are presented in **Figure 5.6(a)(inset)** at a constant supply voltage or drain voltage (V_{ds}) of 0.5 V. From this variation, we can state that with the increase in temperature from 250 K to 350 K, the threshold voltage is reduced down slightly and also gives the high on-current (I_{ON}). At higher temperatures, Ferroelectric permittivity (ε_{FE}) increases, reducing the negative capacitance effect. The voltage amplification weakens, leading to a lower potential

drop across the gate dielectric. As a result, the effective gate voltage seen by the channel decreases, causing a lower threshold voltage [19]. Also, the same variation in the log scale is given in **Figure 5.6**, which shows that the increment in temperature gives a high on-current and slightly high off-current. This variation can be described according to the energy band gap theory. As the temperature increases, the energy band gap starts decreasing, and the passing of electrons from the valence band to the conduction band becomes easy, which results in the rise of the device's off-state current and on-state current [20-24]. The switching ratio (I_{ON}/I_{OFF}) due to transfer characteristics decreases with the temperature rise, as portrayed in **Figure 5.6(b).** Thus, with the temperature rise, the device performance degrades with the concerning switching ratio. The effect of temperature on the short channel effects can be seen in **Figure 5.6(b)** in the form of DIBL value. These effects come because of shortened gate or channel length.

When we shorten the channel length, the source and drain come close to each other, and the supply voltage biasing affects the potential barrier between these terminals. So, the punch-through condition arises between the source and drain terminal, and hence the leakage current increases [25-29]. That is why one should have to minimize these effects. DIBL can be formulated as in Equation (5.5) by taking V_{th} at V_{ds}=0.5 V.

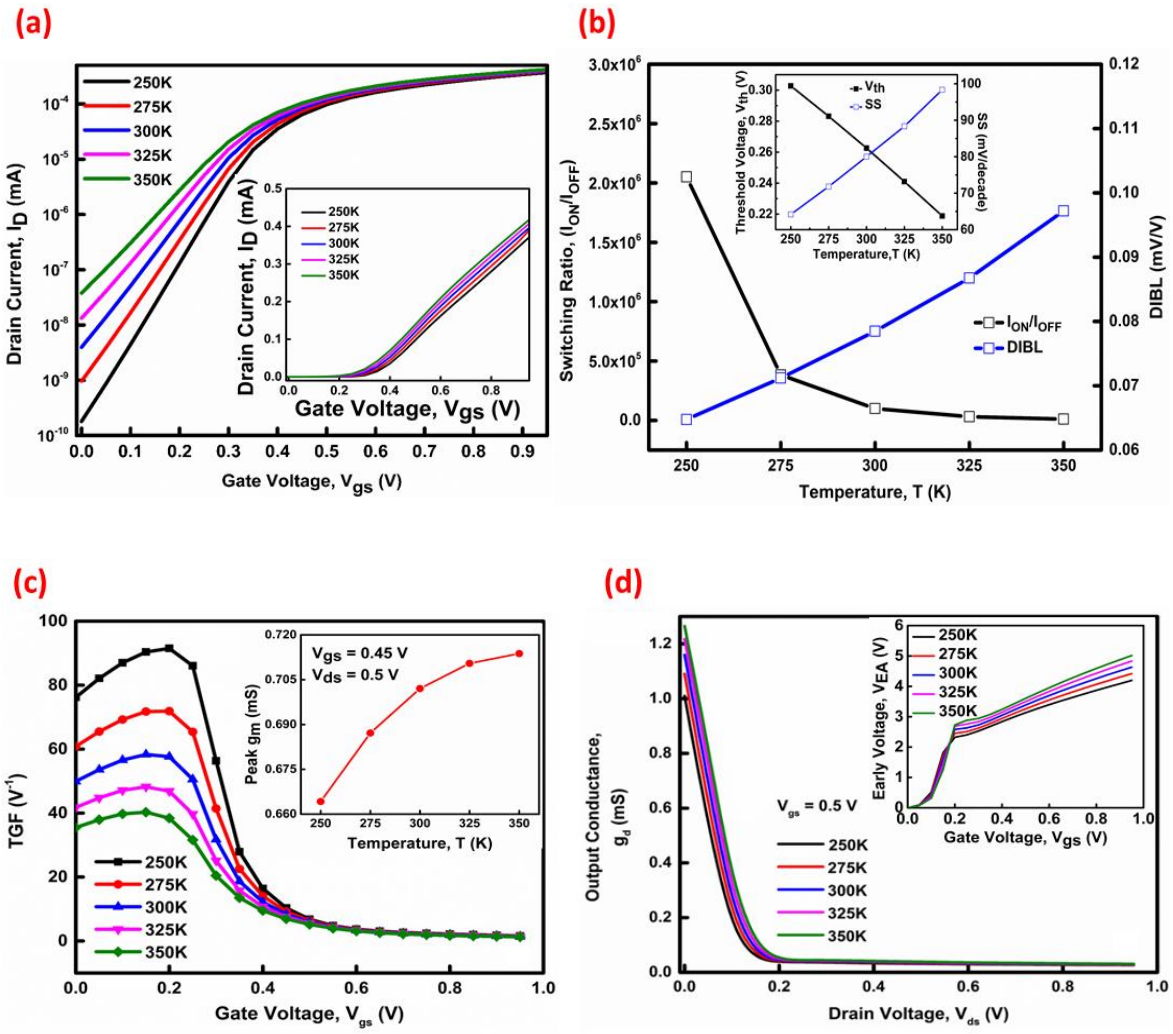


Figure 5.6: Temperature variation impacts (a) I_D-V_{gs} characteristic in logarithm scale and linear scale (inset), (b) I_{ON}/I_{OFF}, DIBL, and V_{th}, SS (inset), (c) TGF, and peak transconductance value (inset), (d) g_d and V_{EA} (inset) with V_{gs} [9].

$$DIBL = \frac{\partial V_{th}}{\partial V_{ds}} \quad (5.5)\ [25]$$

Concerning temperature rise, the DIBL value starts rising, which is unsuitable for the device's performance. At the lower temperature range of 250 K to 300 K, the DIBL value is in a specific range, and it starts increasing linearly with the increase in temperature. Another short channel effect is the subthreshold swing (SS) value [30-32]. The SS variation as a function of temperature is shown inset of **Figure 5.6(b)(inset)**; according to the negative capacitance phenomenon, the SS value becomes low with the use of ferroelectric material in the gate stack. But with the increase in the temperature from 250 K to 350 K,

this value starts increasing, which shows the performance degradation of the device. Another factor in the same **Figure 5.6(b)(inset)** is the threshold voltage (V_{th}) as a function of temperature. For good device performance, the threshold voltage value should be as low as possible because it is the voltage value required for a device to turn on [33]. This behaviour happens due to the use of the insulator layer in the middle of the substrate region, which acts as a barrier for the mobile electrons present in the substrate region to generate the channel region. As the temperature increases, these mobile electrons dominate more, resulting in a lower threshold voltage. All these SCEs are tabulated in Table 5.2.

Moving to analog parameters, **Figure 5.6(c) (inset)** presents the peak transconductance (g_m) observed at V_{gs}= 0.45 V for all the temperatures ranging from 250 K to 350 K. Transconductance can be formulated as Equation (5.6) [34-38].

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \quad (5.6)\ [34]$$

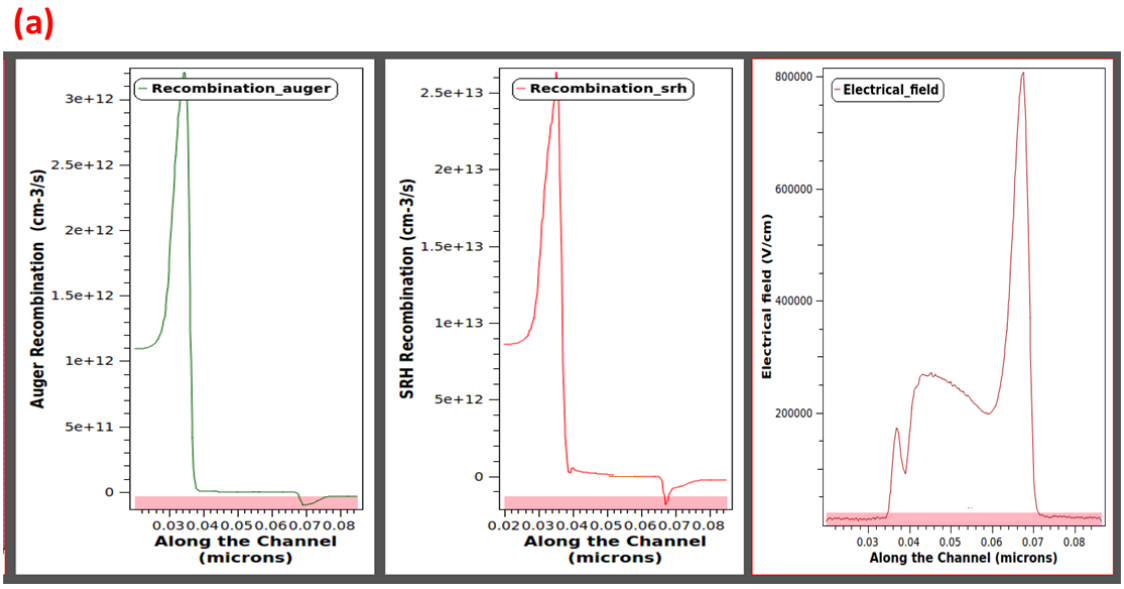
$$TGF = \frac{g_m}{I_D} \quad (5.7)\ [34]$$

$$g_d = \frac{\partial I_D}{\partial V_{gd}} \quad (5.8)\ [34]$$

$$V_{EA} = \frac{I_D}{g_d} \quad (5.9)\ [35]$$

Transconductance tells about the input conductance for a device that describes the drain current change with the gate voltage shift. Graph 5.6(c) (inset) represents the temperature dependence on the peak transconductance. The peak value of transconductance is increasing as the temperature ranges from 250 K to 350 K. This variation shows the improvement of mobility in the electron results in a high value of transconductance with temperature [39-42]. Further, the transconductance generation factor (TGF) variation and the temperature range are given in **Figure 5.6(c).** TGF provides the amount of gain generated per unit of power loss and is given by Equation (5.7). **Figure 5.6(c)** shows the

high values of TGF at low voltages and lower temperatures, which indicates the application in ultra-low-power (ULP) circuits. All the high values of TGF obtained in the subthreshold region illustrate the sustainability of Modified NCFET in ULP applications. With the temperature rise, the rise in the drain current and the lower value of g_m give the lower value of TGF. However, with a further increase in the V_{gs}, this difference in the TGF curves remains insignificant. In addition, **Figure 5.6(d)** shows the behaviour of output conductance (g_d) concerning the drain-source voltage (V_{ds}) for different temperatures and formulated in Equation (5.8). It gives the current driving ability of the device [43]. At low drain-source voltage, g_d decreases with an increase in the temperature range from 250 K to 350 K. The inset of **Figure 5.6(d)** portrays the effect of temperature on the early voltage (V_{EA}). The V_{EA} increases at higher voltages as the temperature rises from 250 K to 350 K. The trend for this can be explained by the expression for the V_{EA}.



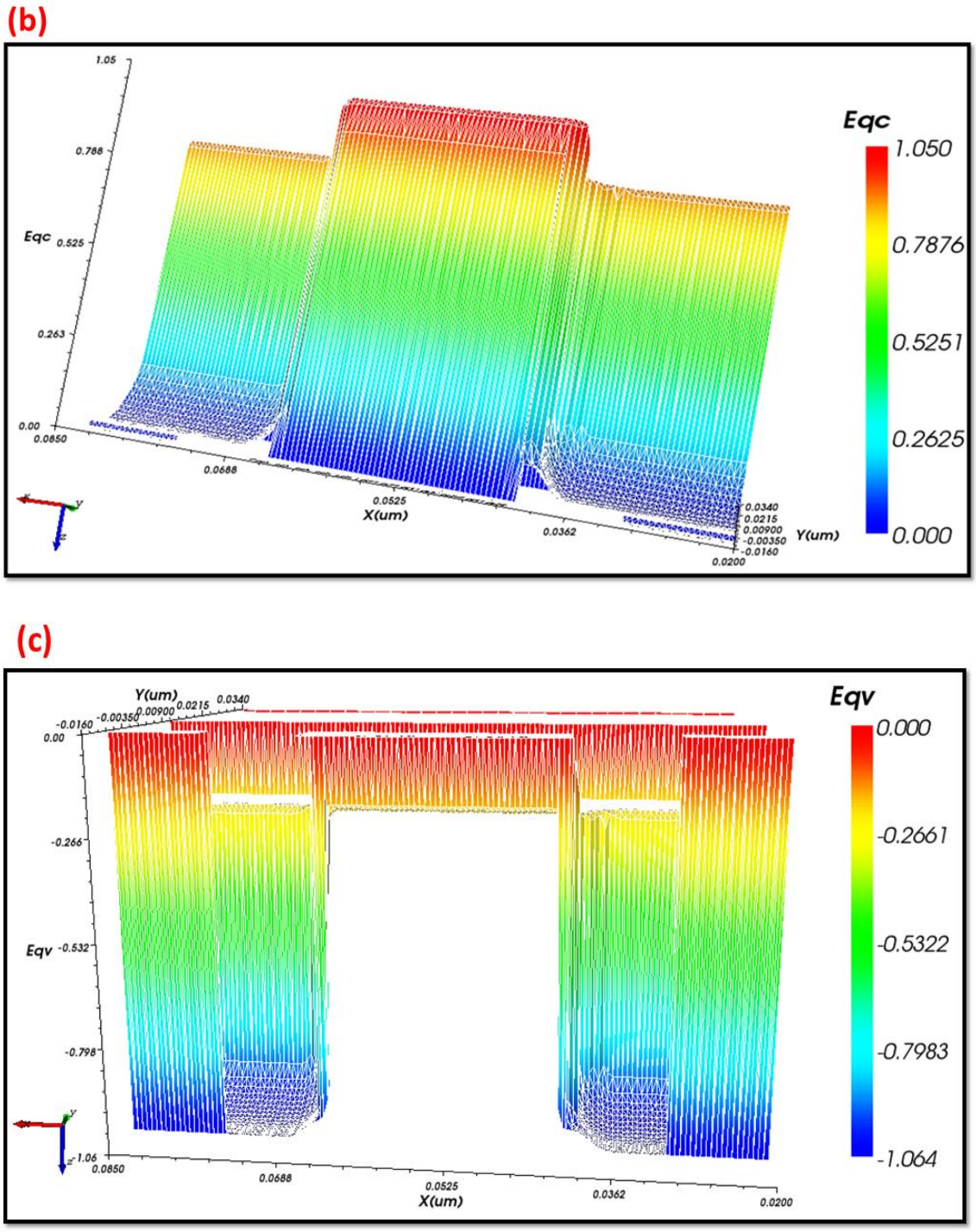


Figure 5.7: (a) Auger, SRH recombination, and Electric Field along the channel length, (b) conduction Band energy (c) Valence Band energy across the architecture [9].

As g_d increases at lower values of voltage and decreases at higher voltage values with the temperature, V_{EA} will increase at higher voltage values with the rise of temperature according to Equation (5.9). All these parameters are tabulated in Table 5.3.

Further, **Figure 5.7** shows the different contour plots across the length of the channel, like **Figure 5.7(a)** shows the Auger and SRH recombination, and electric field in the channel region across the length of the gate. Similarly, **Figure**s **5.7(b)** and **5.7(c)** show the conduction band energy, and valence band energy across the channel length, respectively.

Table 5.2: Variation of SCEs with the impact of temperature.

Short channel effects	**Unit**	**250 K**	**275 K**	**300 K**	**325 K**	**350 K**
V_{th}	V	0.30	0.28	0.26	0.24	0.21
DIBL	(mV/V)	0.065	0.071	0.078	0.086	0.097
SS	(mV/dec)	64.18	71.80	83.34	88.34	98.35

Table 5.3: Summary of analog and RF performance parameters of Modified NCFET with different temperatures.

Parameter	**Unit**	**250 K**	**275 K**	**300 K**	**325 K**	**350 K**
I_{ON}/I_{OFF}	-	2.04×10^{6}	2.61×10^{6}	1.0×10^{5}	3.06×10^{4}	1.10×10^{4}
g_m	mS	0.66	0.68	0.70	0.71	0.72
TGF	V^{-1}	91.49	71.86	57.62	46.84	38.41
g_d	mS	1.01	1.09	1.51	1.21	1.26
V_{EA}	V	4.19	4.41	4.63	4.83	5.01

5.3.4 Temperature impact on the VTC curve of Modified NCFET-based Inverter

To show the temperature impact on the VTC plot of a Modified NCFET-based inverter, we designed a setup with n-channel and p-channel Modified NCFET on the VISUAL TCAD simulator, which is electrically isolated with a 10 nm SiO_2 spacer. N-Poly-Si with a 4.5 eV and P-Poly-Si with a 4.9 eV work function were used for n-channel and p-channel Modified NCFET, respectively. The doping concentration of $1\times10^{16}cm^{-3}$ and $1\times10^{19}cm^{-3}$ is taken for substrate and source/drain of their respective type in n-channel and p-channel Modified NCFET. The schematic circuit diagram of the Modified NCFET-based inverter is shown

in **Figure 5.8(a).** Before any structure-based inverter characteristic, one should match the threshold voltage of an inverter's n-type and p-type components so that the characteristic curve of the inverter from V_{gs}= -1 to 1 V becomes continuous without any breaking point of current [43-47].

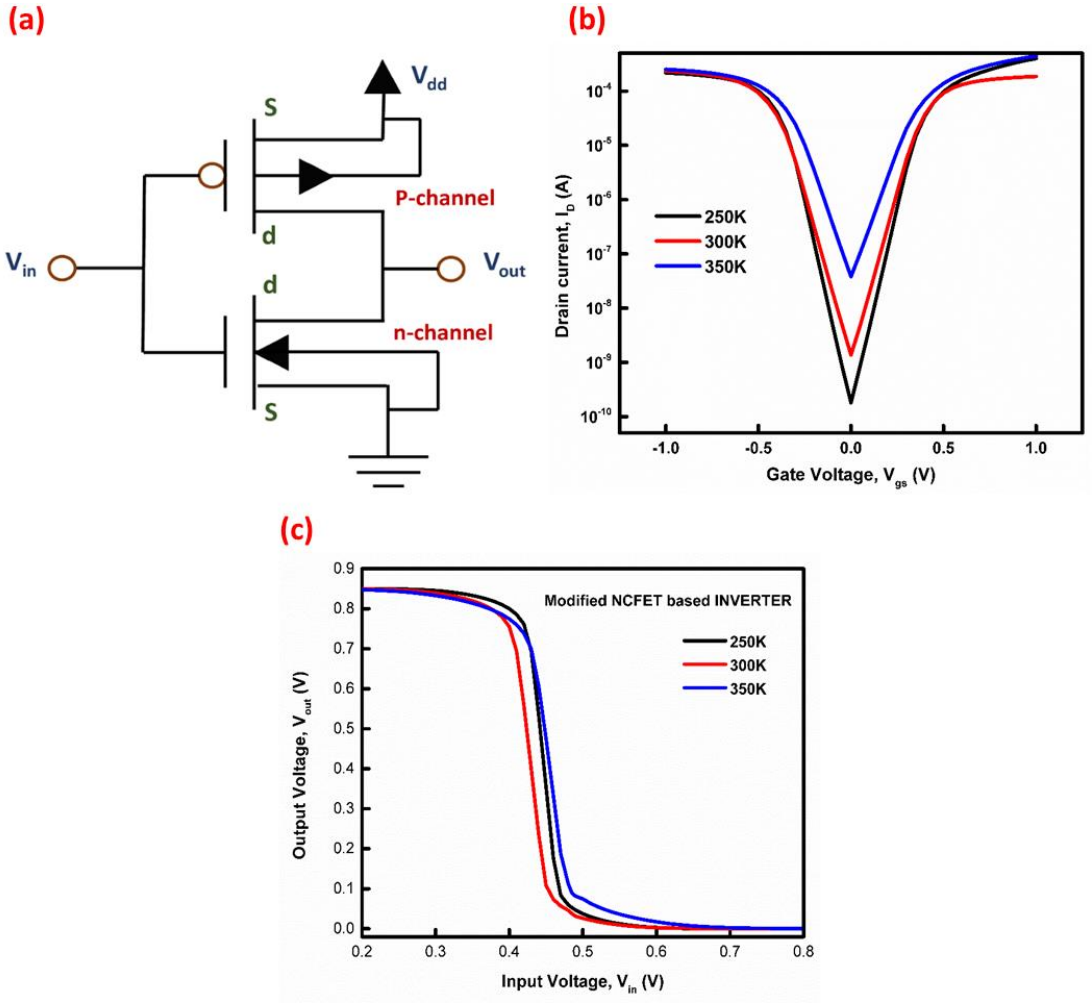


Figure 5.8: (a) Schematic diagram of inverter using Modified NCFET architecture, (b) Threshold voltage matching plot, (c) VTC curve of Modified NCFET-based inverter at temperatures 250K, 300K, and 350K [9].

So, for different temperatures, the V_{th} matching curves are shown in **Figure 5.8(b).** The temperature impact on the voltage transfer characteristic (VTC) curve for a Modified NCFET-based inverter is shown in **Figure 5.8(c).** The variation indicates that the transition region (TR) is getting high with the temperature rise, which delays the device's switching. It shifts from 0.16 V to 0.35 V as the temperature increases from 250 K to 350 K. In the

VTC curve of the inverter, there are two critical points at which the slope of the curve becomes negative. These points correspond to logic 0, called the maximum input voltage (V_{IL}), and logic 1, called the minimum input voltage (V_{IH}).

5.3.4.1 Noise Margin Calculation

The Noise Margin (NM) determines the noise immunity of a device; this value should be high enough to measure the noise components in the device. For low signal levels (NM_L) and high signal levels (NM_H), NM is given as in Equations (5.10) and (5.11) [48].

$$NM_L = V_{IL} - V_{OL} \quad (5.10)\ [48]$$

$$NM_H = V_{OH} - V_{IH} \quad (5.11)\ [48]$$

Where V_{OH} and V_{OL} define the maximum output voltage and minimum output voltage when output levels are logic 1 and logic 0, respectively. All parameters are tabulated in Table 5.4.

5.3.4.2 Propagation Delay and Transition Time

In the case of FETs, there are many non-ideal effects, out of which parasitic capacitance is one. Because of these capacitances, the delay in voltage change is observed, which limits the speed of operation. This work section shows how these capacitances affect the output waveform. With the help of propagation delay and transition delay, we can test the speed performance of the device and how it changes with the temperature variation [49]. We apply a step voltage at the device's input for the propagation delay, and we get the output waveform with a transition delay. The two propagation delays shown in **Figure 5.9(a),** marked as t_{pHL} and $t_{pLH,}$ are known as propagation delay time for High-to-Low and Low-to-High, respectively. The inverter operates between two voltages: output high voltage (V_{OH}) and output low voltage (V_{OL}). The t_{pHL} is the time required for the output to fall from V_{OH} to (V_{OH}+V_{OL})/2.

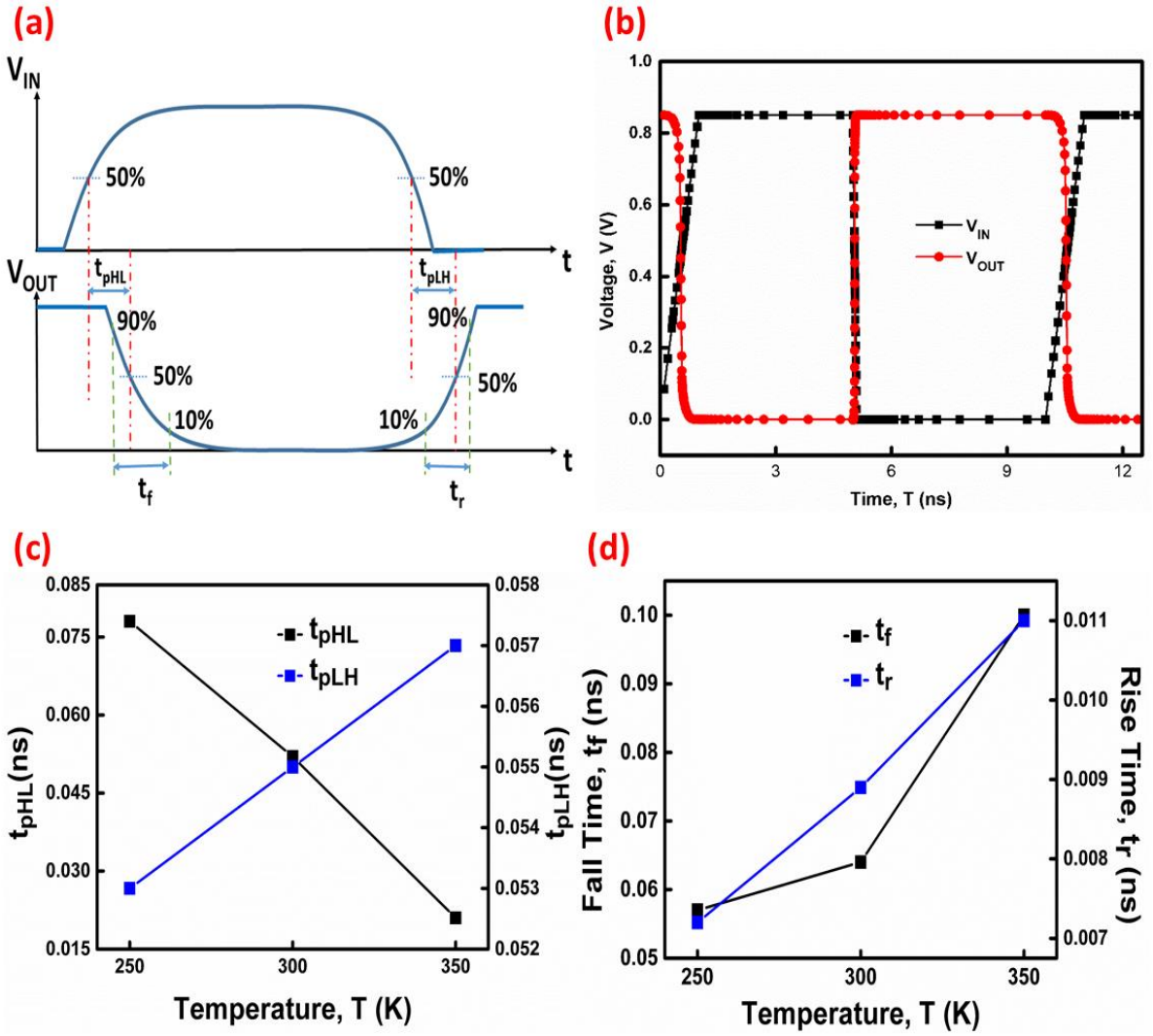


Figure 5.9: (a) Propagation delay and transition time schematic of NCFET-based inverter, (b) Propagation characteristic of Modified NCFET-based inverter at 300K, (c) Variation of t_p, (d) t_{rf} with rise of temperature [9].

Similarly, t_{pLH} is the time required for the output waveform to rise from V_{OL} to $(V_{OH}+V_{OL})/2$. All these parameters are shown in **Figure 5.9(a)** So, the propagation delay is the average of these two given by Equation (5.12).

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} \quad (5.12)\ [48]$$

$$t_{rf} = \frac{t_r+t_f}{2} \quad (5.13)\ [48]$$

Figure 5.9(b) shows the transient curves for the NCFET-based inverter at 300 K. In **Figure**

5.9(c) the propagation characteristic of the Modified NCFET-based inverter at 300K is shown. From **Figure 5.9(d),** we can see the impact of temperature on the propagation delay factors t_{pHL} and $t_{pLH,}$ and it can be concluded that with the temperature rise, t_{pHL} decreases, which indicates the fast switching of the device. And the t_{pLH} increases with the temperature rise [50-52]. Next, the transition time factors are rise time (t_r) and fall time (t_f). Rise time is the time interval when the output signal rises from 10% to 90% of the (V_{OH}-V_{OL}) value, and fall time is the time step in which the output signal falls from 90% to 10% of the (V_{OH}-V_{OL}) value shown in **Figure 5.9(d)** [53-54]. Hence, the transition time is the average of these quantities called Edge rate (t_{rf}) and is given by Equation (5.13). **Figure 5.9(d)** shows that the transition time increases with the rise in the temperature, which shows the slow switching speed.

Table 5.4: Comparison of noise margin and propagation delay for different temperatures of Modified NCFET-based inverters.

Parameter	**Unit**	**250 K**	**300 K**	**350 K**
V_{IL} (V)	V	0.39	0.35	0.30
V_{IH} (V)	V	0.55	0.60	0.65
V_{OL} (V)	V	0.013	0.003	0.007
V_{OH} (V)	V	0.81	0.82	0.83
NM_L (V)	V	O.377	0.347	0.293
NM_H (mV)	mV	0.260	0.220	0.183
TR (V)	V	0.16	0.25	0.35
t_{pHL}(ns)	ns	0.78	0.52	0.21
t_{pLH}(ns)	ns	0.053	0.055	0.057
t_p(ns)	ns	0.416	0.287	0.133
t_r(ns)	ns	0.0072	0.0089	0.0110
t_f(ns)	ns	0.057	0.064	0.100
t_{rf}(ns)	ns	0.0321	0.0364	0.0555

So, the Modified NCFET device should operate at low temperatures for fast-speed performance. All these parameters are tabulated in Table 5.4.

5.4 SUMMARY

It is concluded from this chapter of DFT calculation that Si-doped HfO_2 gives a less direct bandgap, dense projected DOS, high transmission peaks, and lower Hartree potential when compared to the undoped HfO_2 atom. Hence, Si-doped HfO_2 is used as the ferroelectric material in the gate stack of device architecture, which gives us a better industrial application when using natural ferroelectric materials. Further, it is observed that Modified NCFET shows improved factors. I_{OFF} and SS are reduced by 81.17% and 10.28%, respectively, compared to conventional NCFET device architecture. The switching ratio is increased by one decimal point compared to the conventional one. The above study considers the impact of temperature variation on the analog, RF performance, and digital application parameters of the Modified NCFET structure. Simulation results show the variation in different parameters when the temperature rises from 250 K to 350 K with the step size of 25 K. Starting with the basic I_{ON}, which increases by 12.39%, and V_{th} is reduced by 30%.

Further, the impact of temperature variations on SCEs is shown as the DIBL is reduced by 32.98% and SS is reduced by 34.74% as the temperature decreases from 350 K to 250 K. Furthermore, as the temperature rises from 250 K to 350 K, the analog parameters shows the following trends: g_m and g_d is enhanced by 9.09% and 2.75%, respectively and TGF is reduced by 58.02%. Also, V_{EA} is enhanced with 19.57%. In continuation, we examine the effect of temperature on the VTC plot of a Modified NCFET-based inverter. We have taken out three temperature values to extract the variation, which are 250 K, 300 K, and 350 K. If we see the trend with the decreasing temperature, it has been observed that

the transition region (TR) decreases as the temperature drops. It becomes 54 times less when the temperature changes from 350 K to 250 K. The noise margin factors are also increased when the temperature falls. The NM_L and NM_H show improvement with 33.43% and 42.26% increments, respectively. The above results show that the Modified NCFET gives better digital application parameters at lower temperatures. Propagation delay is decreased by 67.94% when the temperature rises from 250 to 350 K, providing better and faster switching performance.

For further device compatibility, ensuring spacer compatibility is essential for the device's efficiency and longevity. Proper testing and selection of spacers will reduce the risk of malfunction and improve overall device performance. So, the Modified NCFET's parameters will be discussed with the different materials spacers.

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6

CHAPTER

Self-Consistent LCAO based DFT analysis of high-k spacers on Gate-Stacked NCFET for improved device-circuit performance

- *This chapter discusses the impact of the high-k spacers on the analog/RF and inverter-based parameter performance of Gate-Stacked NCFET.*
- *Self-consistent LCAO-based DFT analysis is done for the spacer materials regarding band structure, PDOS, and Hartree potential. Maximum PDOS is observed for the HfO2 spacer with minimum Hartree potential.*
- *The switching ratio (I_{on}/I_{off}) is discussed for GS-NCFET with different types of spacers. The leakage current of S3 (GS-NCFET with HfO_2 spacer) is reduced by 25.92 % to S0 (GS-NCFET with no spacer), and three decimal points increase the switching ratio. The short channel effects (SCEs) like subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are extracted at drain-source voltage (V_{ds}) of 0.5 V. Threshold voltage and DIBL value of S3 decreased by 16.66% and 41.17%, respectively, compared with S0.*
- *It is found that the switching ratio of the S3 configuration increased, thereby improving the analog performance in terms of transconductance, device efficiency, intrinsic gain, and early voltage compared to the S0 configuration.*
- *In addition, the voltage transfer characteristic (VTC) curve of GS-NCFET with a spacer-based inverter is considered for digital application purposes, and the transition region is drawn out for all the device architecture-based inverters. Essential parameters like propagation time delay for input and corresponding output curve for FET-based inverters and their rise/fall time are evaluated to study the application purposes.*
- *Consequently, the proposed GS-NCFET device with an HfO_2 spacer would be an attractive solution for low-power and high-performance CMOS circuits.*

In **Chapter 5**, Modified NCFETs' temperature analysis includes threshold voltage, drain current, subthreshold slope, and inverter-based parameters. Understanding these effects is essential for designing any device that maintains consistent performance and reliability under varying thermal conditions. Engineers use empirical data and theoretical models to account for temperature effects in circuit design and system optimization, ensuring that electronic devices operate effectively within their specified temperature ranges. The device uses spacers with different dielectric constants for further reliability tests.

6.1 INTRODUCTION

In MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) technology, spacers play a vital role in ensuring these semiconductor devices' performance, reliability, and scalability. As MOSFETs are used in a wide range of electronic applications, from simple circuits to complex integrated circuits, the precise control of their electrical properties is essential. Spacers contribute significantly to achieving this control [1-3]. Here's a detailed look at why spacers are necessary for MOSFETs: One of the primary functions of spacers is maintaining a proper distance between the gate electrode and the source/drain regions. In MOSFETs, the gate voltage controls the current flowing between the source and drain. Managing the distances between these regions becomes increasingly challenging as devices become smaller. Spacers help precisely define this spacing, which is crucial for controlling the channel length and ensuring that the MOSFET operates within its intended parameters [4]. Further, as MOSFETs scale down to smaller dimensions, short-channel effects become more pronounced. These effects arise when the channel length of the MOSFET becomes comparable to the distance between the source and drain regions, leading to reduced control over the channel and increased leakage currents. Spacers help to mitigate these issues by acting as physical barriers that isolate the gate from the source and drain, thereby improving

the electrostatic control over the channel and reducing leakage currents [5-7]. This is particularly important in advanced technology nodes where short-channel effects are a major challenge. Furthermore, in advanced MOSFET designs, spacers are used to control the extent of the source and drain extension. By adjusting the thickness of the spacers, manufacturers can fine-tune the device's electrical characteristics, such as threshold voltage and drive current. This control is essential for optimizing the performance of the MOSFET, especially in high-speed or low-power applications where precise electrical characteristics are required.

Moreover, gate leakage is a significant issue in modern MOSFETs, particularly as device dimensions continue to shrink. Spacers are crucial in preventing direct contact between the gate and the source/drain regions, which can lead to leakage currents. By providing a robust insulating layer, spacers help to minimize these leakage paths, thereby enhancing the overall efficiency and performance of the MOSFET [8-10]. This is crucial for maintaining the device's reliability and reducing power consumption. In addition to their primary functions, spacers can influence the channel region's mechanical strain. Strain engineering is used to enhance carrier mobility and improve the performance of the MOSFET. By adjusting the spacer thickness and material properties, manufacturers can control the channel's strain, leading to better device performance. This aspect is particularly relevant in high-performance applications where every bit of enhancement can make a significant difference. The dielectric constant of spacer materials is critical in MOSFET design due to its impact on gate-to-source/drain capacitance, short-channel effects, threshold voltage stability, leakage current minimization, and overall device scaling and performance. The appropriate spacer material with the suitable dielectric constant is essential for achieving optimal MOSFET performance, reliability, and efficiency.

In summary, spacers are essential in MOSFETs for maintaining precise gate-source and gate-drain distances, mitigating short-channel effects, controlling source-drain extensions, preventing gate leakage, and enabling strain engineering. As MOSFET technology advances, spacers become increasingly critical in achieving optimal performance and reliability in semiconductor devices. The following outline constitutes this chapter's structure: The second section includes the DFT calculation for the spacer's material. Spacers function as insulators or dielectrics. A computation for spacer materials is conducted using the linear combination of atomic orbital (LCAO)-based density functional theory (DFT). The study analyses the band structure, projected density of states (PDOS), and Hartree potentials of AIR spacers, SiO_2 spacers, and HfO_2 spacers. In the third section, the Gate-Stacked-NCFET (GS-NCFET) is discussed with the physical models used in the simulation work. The later part of the chapter discusses the results obtained through simulation. The impact of different dielectric constant spacers on the parameters of GS-NCFET is discussed. The effect of spacers on the GS-NCFET explores the new approaches for digital applications with improvements in circuit parameters.

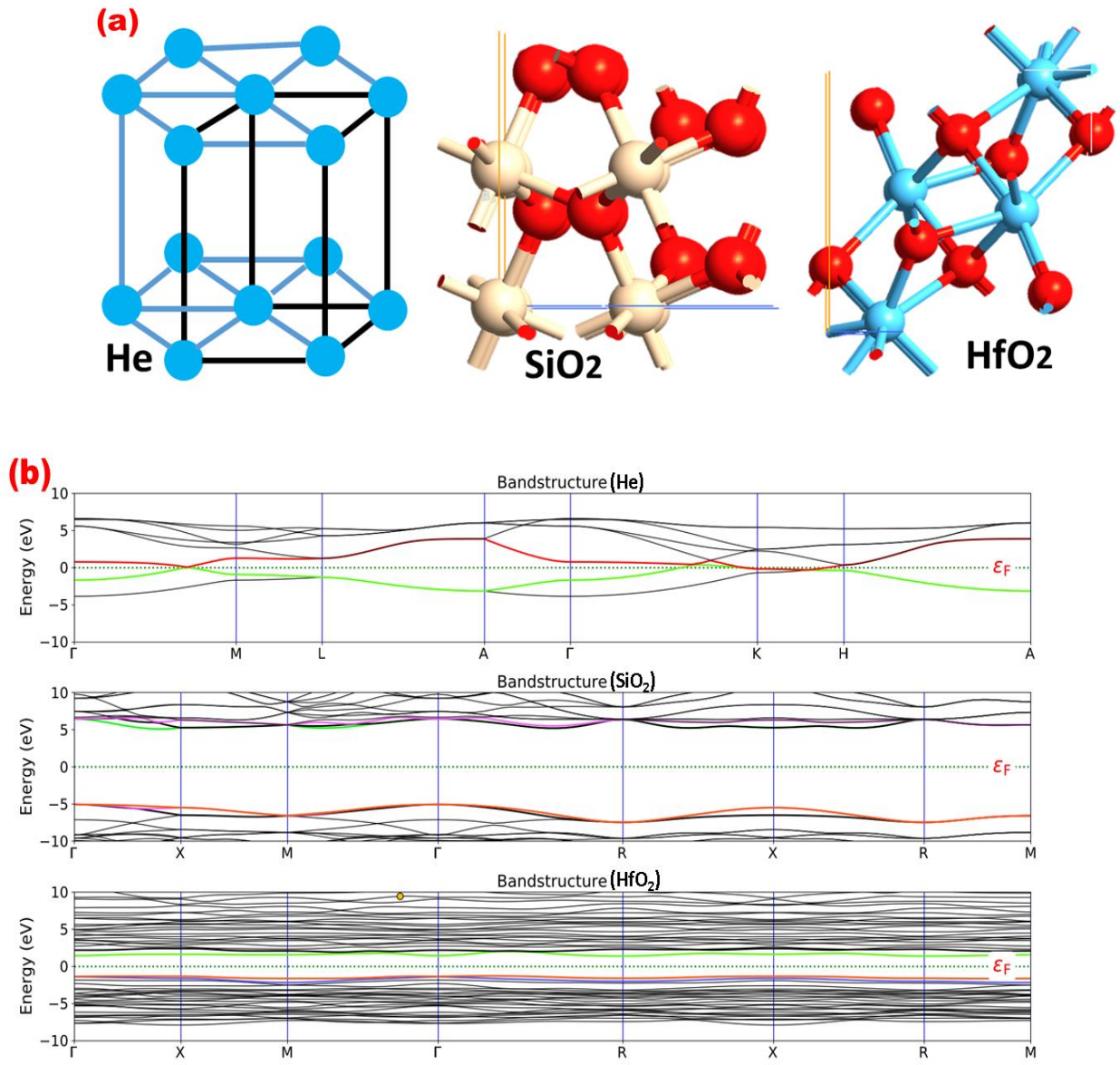
6.2 LCAO-BASED DFT CALCULATION FOR SPACERS

Density Functional Theory (DFT) is a computational quantum-mechanical modeling method used to study the electronic structure of many-body systems like atoms, molecules, non-equilibrium Green's functions linked to electrical devices, and the condensed phases. The properties of many-electron systems can be determined by using a functional that is a function of another function. In DFT, electron density functional are used to investigate the structural properties. DFT calculations predict material behaviour based on quantum mechanical considerations without requiring its fundamental material properties. Atomic modeling using the DFT supports verifying the characteristics of materials. DFT analysis

using the LCAO (Linear Combination of Atomic Orbital) is done to overcome the problem of being unable to solve the Schrodinger equation for a system with more than one electron [11]. In this, the overall wave function is the superposition of individual orbitals. The spacers used in the GS-NCFET have their structural properties, so the device's application must differ. In this work section, the author discussed the structural properties of different spacer materials.

One assumption is taken for this work that due to the unavailability of air molecule structure in the quantum ATK database, we investigate the structural properties of helium (k=1.000074 at 0^0 C and 1atm), which has nearly the same dielectric constant of air (k=1). **Figure 6.1(a)** shows the crystal structure with the respective band structure of He, SiO_2, and HfO_2 in the HCP, SC, and SC lattice, respectively. The lattice parameters are taken for helium are a= 5.1156 Å, b= 5.1156 Å, c= 1.633×a Å, α= 90º, β= 90º, γ= 120º, for SiO_2 are a= 1.25688 Å, b= 1.25688 Å, c= 1.25688 Å, α= 90º, β= 90º, γ= 90º, and for HfO_2 are a= 1.25688 Å, b= 1.25688 Å, c= 1.25688 Å, α= 90º, β= 90º, γ= 90º.The band structure shows the electronic transitions with direct and indirect bandgap between the conduction band and valence band, which defines the actual transition probability in the material. As there is no region without the bands above the fermi energy in the case of helium band structure and the valence band top and conduction band bottom are located at the same Brillouin zone, this would behave like a conductor. In the case of SiO_2 and HfO_2, a region with no bands above the fermi energy level called bandgap shows these materials' insulating properties [12]. The direct and indirect bandgap of He, SiO_2, and HfO_2 is 0 eV, 0 eV, 10.42 eV, 10.14 eV, and 2.80 eV, 2.68 eV, respectively. Also, the valence band and conduction band edge of He is at 0 eV, SiO_2 at -5.07 eV and 5.06 eV, and HfO_2 at -1.32 eV and 1.35 eV shown in **Figure 6.1(b).** Further, **Figure 6.1(c)** defines the projected density of states (PDOS) concerning the energy for Helium, SiO_2, and HfO_2. It gives the projection of a particular

orbital of a specific atom on the density of states. So, if sum over all the projections, one will have the total density of the state, or simply, the DOS. The PDOS for helium is the highest, and for HfO_2, it is lesser, which shows a better spacer quality by enhancing the fringing of the electric field around the gate stack of the device compared to the SiO_2-spacers [13]. Furthermore, the Hartree potential is expressed in **Figure 6.1(d)** for all types of spacer materials. The Hartree potential is defined as the electrostatic potential from the electron charge density and must be calculated from the Poisson's Equation (6.1):



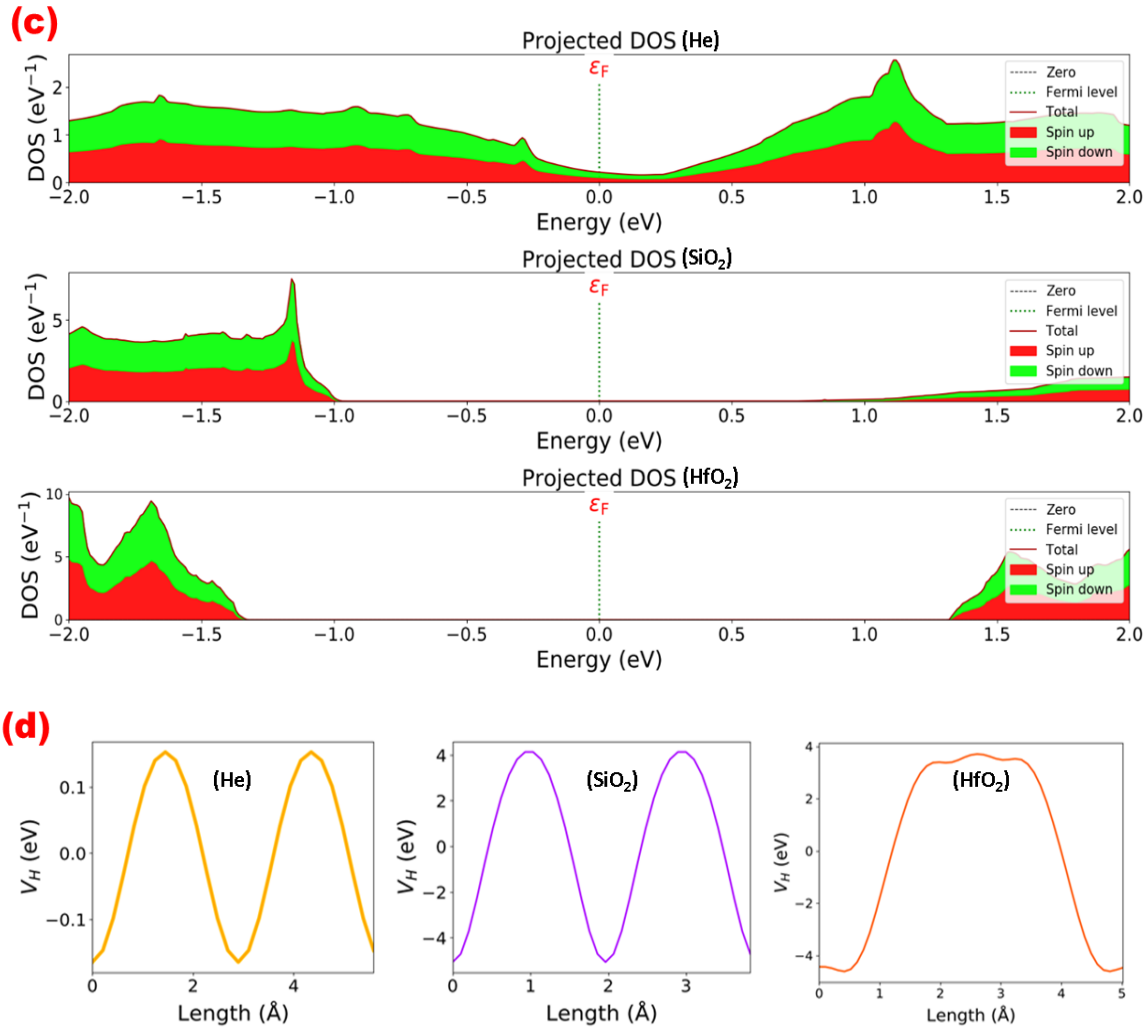


Figure 6.1: (a) Atomic structure (b) Band structure (c) PDOS (d) The Hartree potential corresponding to He (assumed Air molecule), SiO2, and HfO2 [14].

$$\nabla^2 V_H[n](r) = -4\pi n(r) \qquad (6.1)\ [12]$$

Poisson's Equation is a second-order differential equation, and a boundary condition is required to fix the solution. Molecular systems have the boundary condition that the potential goes asymptotically to zero. In bulk systems, the boundary condition is that the potential is periodic. The lower the Hartree potential, the more stable the atomic structure. Atoms take less time to move at lower potential from one orbit to another. HfO_2 has the lowest Hartree potential among all discussed materials [12].

6.3 DEVICE ARCHITECTURE AND PHYSICAL MODELS

As previously discussed in Chapter 4, the architecture of NCFET, a high-k dielectric material (HfO_2) (k=25) layer in the substrate region as Buried Oxide (BOX) as well as in the gate stack is used and is shown in **Figure 6.2** [14]. The device dimensions of both devices are the same as the channel length (L_g) of 25 nm, and extensions of source/drain on both sides of the channel region are taken at 10 nm.

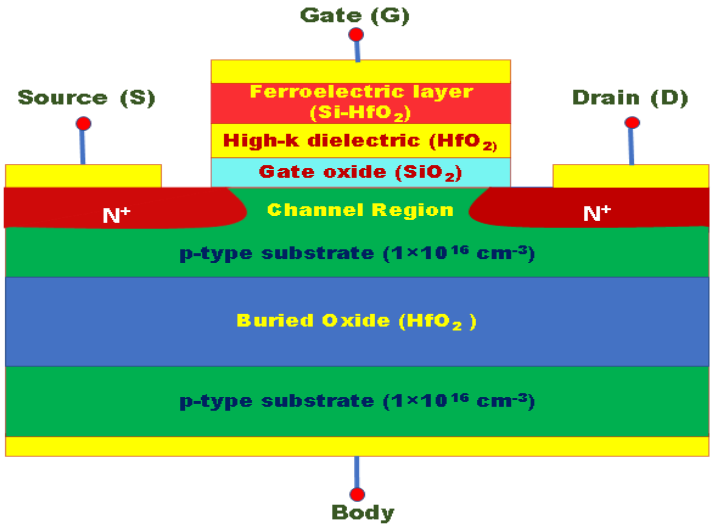


Figure 6.2: Gate-Stacked Negative Capacitance Field Effect Transistor (GS-NCFET) Device architecture [14].

The gate stack's oxide thickness is fixed at 1 nm (0.5 nm SiO_2+0.5 nm HfO_2). The substrate region is doped with a uniform p-type of 1×10^{16} cm^{-3} concentration. The source/drain region is heavily n-type Gaussian doped with 1×10^{20} cm^{-3} concentration. The thickness of high-k dielectric in the substrate region is kept at 5 nm. Further, **Figure 6.3** shows the channel region of GS-NCFET with the attachments of different types of spacers. S0 denotes the GS-NCFET without the spacers, S1 denotes the GS-NCFET with 5 nm length air (k=1) spacers, S2 specifies the GS-NCFET with 5 nm length SiO_2 (k=3.9) spacers, and S3 shows the GS-NCFET with 5 nm length HfO_2 (k=25) spacers around the gate terminal.

In addition, device methodology includes the FE layer set down on the gate dielectric of the baseline MOSFET. The polarization direction of the FE material is parallel

to the gate stack. VISUAL Technology-Computer-Aided-Design (VISUAL TCAD) is capable of solving the Landau-Khalatnikov (L-K) equations of electric field used for the FE layer as a function of polarization (P) given as Equation (6.2):

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\left\langle\frac{dP}{dt}\right\rangle \qquad (6.2)\ [15]$$

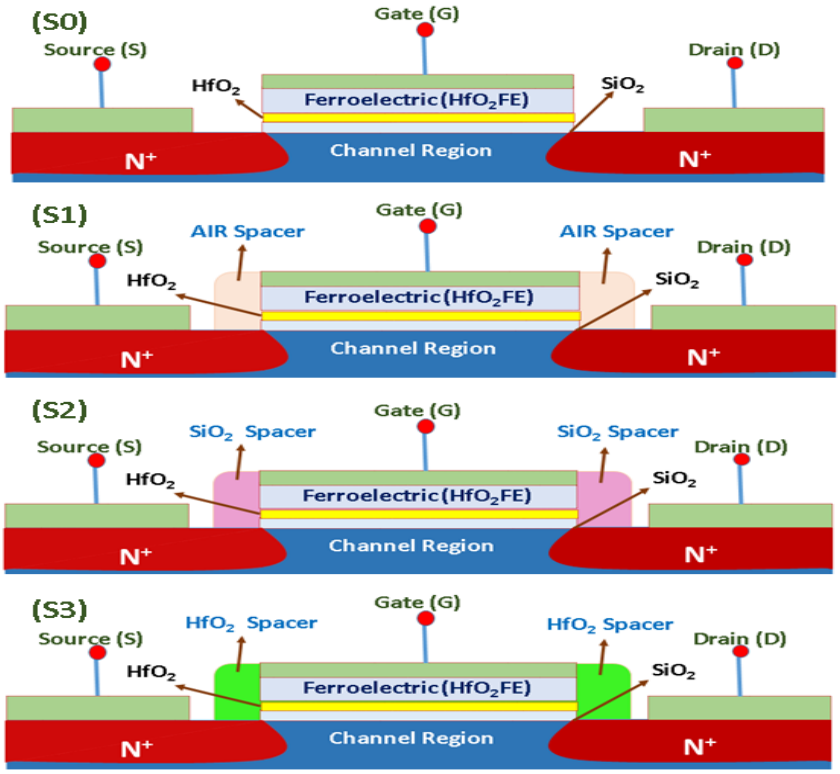


Figure 6.3: GS-NCFET with no spacer (S0) Air spacer (S1) SiO_2 spacer (S2) HfO_2 spacer (S3) [14].

Poisson's Equation and other physical models like impurity scattering, mobility degradation due to surface roughness scattering, and phonon scattering, specific to scaled devices. As the quantum mechanical confinement can be modelled and stabilized by changing the gate work function and oxide thickness, it is not assumed for the simulation work. The viscosity coefficient (ρ) and the domain interaction coefficient (g) in the L-K equation are 0.18 **Ω**cm and 10-10 m^3/F, respectively.

By using the doping technique in HfO_2-based FE, the coercive field (E_C) and remnant polarization (P_r) of 1 MV/cm and 6 μC/cm^2 are achieved, corresponding to L-K

constants α = -2.165× 10^{11} cm/F, β = 3.007 × 10^{21} $cm^5/(FC^2)$, γ = 0.000 cm^9/FC^4. The basic DDML1 equations followed by the simulators are given in Equations (6.3), (6.4), and (6.5).

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n E_n + \mu_n \frac{k_b T}{q} \nabla n) - (U - G) \quad (6.3)\ [15]$$

$$\frac{\partial p}{\partial t} = -\nabla.\left(\mu_p p E_p - \mu_p \frac{k_b T}{q} \nabla p\right) - (U - G) \quad (6.4)\ [15]$$

$$\nabla.\mathcal{E} \nabla \Psi = -q(p - n + N_D^+ - N_A^-) \quad (6.5)\ [15]$$

Where Ψ is the electrostatic potential of vacuum level, the concentration of electron and hole is noted by n and p, respectively, N_D^+ and N_A^- define the ionized impurity concentrations, and q is the electron charge magnitude. E_n and E_p are the effective driving electrical field for electrons and holes. μ_n and μ_p are mobilities of electrons and holes, respectively. U is the recombination rate, and G is the generation rate of both electrons and holes. All other symbols have their specific standard meanings. All other S0, S1, S2, and S3 regions are identical. Simulation work for all the device architectures is carried out on the VISUAL TCAD simulator. All comparison parameters are done on the V_{ds}=0.5 V.

6.4 RESULTS AND DISCUSSIONS

6.4.1 Comparison of Conventional NCFET and GS-NCFET

In this section, the improvement factor of GS-NCFET over the conventional NCFET, followed by the effect of different spacers on the GS-NCFET, is discussed. **Figure 6.4** shows the transfer characteristics of conventional NCFET and GS-NCFET at constant drain-source voltage, V_{ds} = 0.5 V, which shows GS-NCFET has higher on-current and lower leakage current, explaining the improved behaviour of GS-NCFET by the use of high-k dielectric material in gate stack [14].

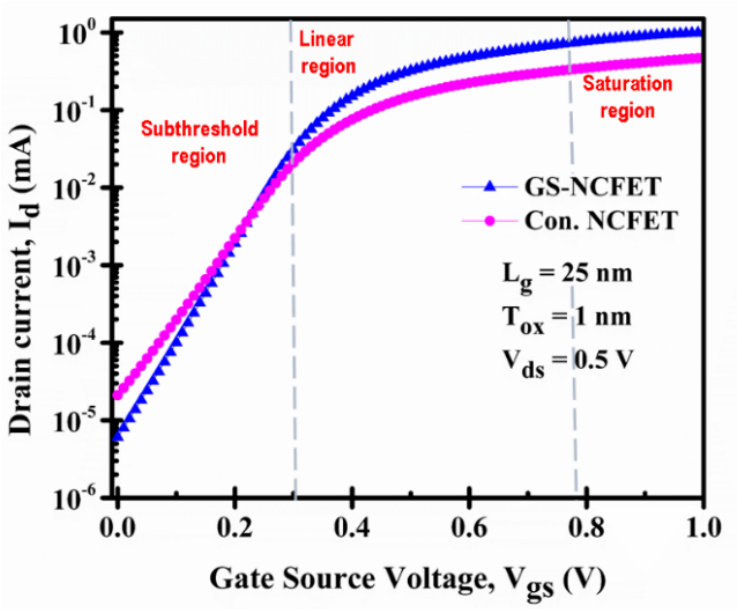


Figure 6.4: Transfer characteristics comparison of conventional NCFET and GS-NCFET [14].

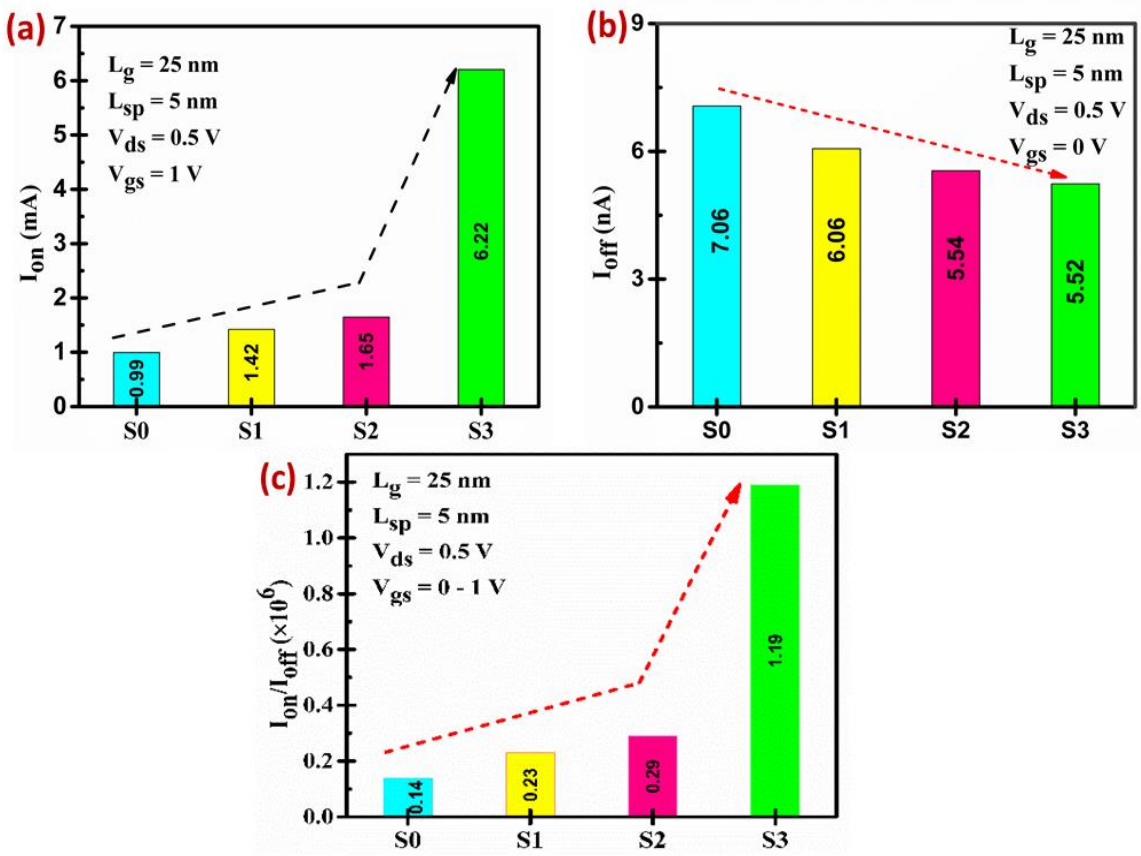


Figure 6.5: Comparison of (a) I_{on} current. (b) I_{off} current. (c) Switching ratio (I_{on}/I_{off}) for S0, S1, S2, and S3 configuration [14].

6.4.2 Effect of spacers on Switching profile and SCEs of GS-NCFET

Figure 6.5(a) shows the comparison of on-current for S0, S1, S2, and S3. S0 has the lowest on-current and increases as the dielectric constant of the spacers increases, i.e. S1, S2, and S3. Also, the leakage current starts decreasing in the same trend shown in **Figure 6.5(b).** The reason for the trend is that the spacers insulate the source and drain region from the gate terminal, which diminishes the gate leakage current and significantly increases the switching ratio of a particular device [15-17]. Another explanation for this trend is the enhancement in the fringing of the electric field due to the application of high-k dielectric constant spacers, i.e. SiO_2 and HfO_2. Thus, it reduces the effective gate voltage that lowers the transverse electric field responsible for carrier tunnelling through the gate oxide. This insulation increases as the dielectric constant of the spacer increases. Here, the Air spacer has the lowest dielectric constant value, 1, and HfO_2 has the highest dielectric constant value (k = 25). So, the S3 has the highest switching ratio, as verified by **Figure 6.5(c).** Furthermore, when the L_g is in the same order of magnitude as the width of the depletion layer, then the MOSFET device is considered to have SCEs. However, at the cost of these SCEs, operation speed and number of components per chip increase [18].

Because of SCEs, two physical phenomena are attributed. One is the limitation imposed on electron drift characteristics in the channel, and the other is modifying the threshold voltage. Two specific SCEs are SS and DIBL. **Figure 6.6(a)** shows the V_{th} and DIBL variation with the different types of spacers. The variation shows the decreasing value of V_{th} and DIBL as the dielectric constant of spacers increases, i.e. S0, S1, S2, and S3. The device S0 has the maximum value of V_{th} and DIBL and starts decreasing for S1, S2, and S3. DIBL is calculated as formulated in Equation (6.6). Reduced DIBL further minimizes the threshold voltage roll-off problem. The drain coupling to the channel through

gate dielectric and spacer reduces as the spacer-k value increases [19]. As discussed in the previous section, the high-k spacers enhance the fringing electric field, directly giving better control over the junction depletion region near the drain side, thus reducing the DIBL effect. Also, as we know, multi-gate structures exhibit good immunity against short channel and degradation effects compared to single-gate FETs. In this case, the immunity to short-channel effects in single-gate FETs is achieved through a combination of material advancements, device structure optimization, and innovative designs, allowing for continued scaling of transistor dimensions and improved performance in integrated circuits. The device structure can be optimized to minimize the influence of the drain on the channel. For example, introducing lightly doped drain (LDD) regions or using halo doping techniques can reduce the electric field at the drain/channel interface, mitigating DIBL. In addition, the SS variation in linear and saturation for S0, S1, S2, and S3 is shown in **Figure 6.6(b).**

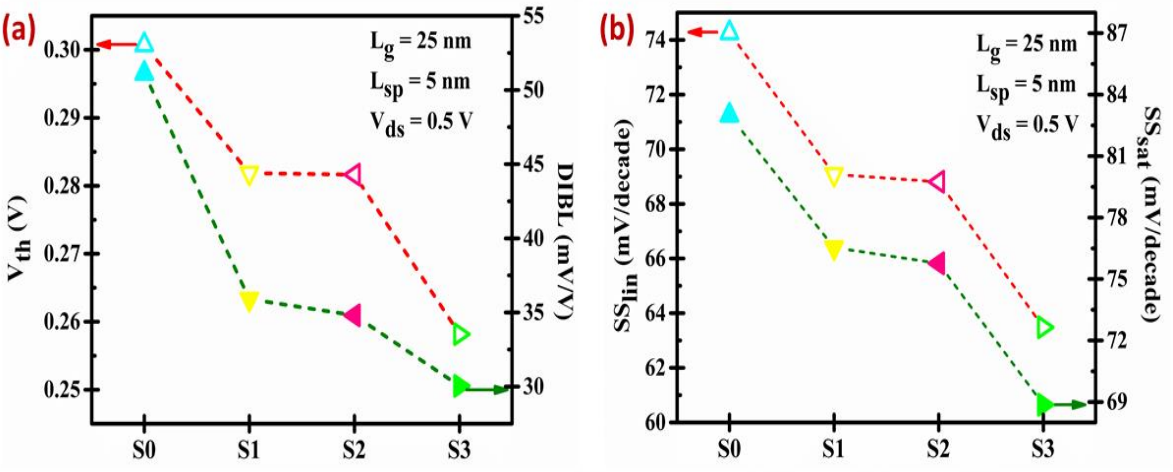


Figure 6.6: Comparison of (a) V_{th} and DIBL. (b) SS in linear and saturation regions for S0, S1, S2, and S3 configurations [14].

The SS value in both regions shows a decreasing trend as we move from S0 to S3. SS in the linear region is extracted at V_{gs} = 0.1 V, SS in the saturation region is extracted at V_{gs} = 1 V, and V_{ds} are kept constant at 0.5 V. Subthreshold swing defines the required gate-

source voltage to change the drain current by one decade. It is clear that the threshold voltage for GS-NCFET with HfO_2 spacer, i.e. S3, has the lowest value. So, the SS value for the S3 is also the lowest and approaches the standard Boltzmann tranny limit, which is 60 mV/dec. S0 has the maximum SS value, and S1 and S2 show the decrement values and can be extracted as given in Equation (6.7).

$$\text{DIBL}=\frac{\partial V_{th}}{\partial V_{ds}} \quad (6.6)\ [20]$$

$$\text{SS}=\frac{\partial V_{gs}}{\partial log I_D} \quad (6.7)\ [20]$$

This variation in SS shows better gate control to channel due to the assistance of high-k dielectric spacers. The higher driving current and lower leakage current achieved using the high-k dielectric spacer effectively enhance the device's performance and reduce power dissipation.

6.4.3 RF/analog parameters of spacers-based GS-NCFET

Analog parameters like transconductance (g_m) and transconductance generation factor (TGF) are discussed for S0, S1, S2, and S3. **Figure 6.7(a)** shows the g_m variation concerning the gate-source voltage at constant V_{ds} = 0.5 V. The curve shows that the peak values of g_m are highest for S3 and lowest for S0 because of an enhanced fringing electric field of HfO_2 spacer. Transconductance is defined by the formula given in Equation (6.8). It depends on the change in drain current with the change in gate-source voltage [20]. Also, Equation (6.9) formulates the TGF of a device. With this help, we can explain the values of TGF shown in **Figure 6.7(b).** The standard value of TGF is 40 V^{-1}, and as we move from S0 to S3, the TGF value increases and approaches the standard value (40 V^{-1}) [21].

$$g_m=\frac{\partial I_D}{\partial V_{gs}} \quad (6.8)\ [11]$$

$$\text{TGF}=\frac{g_m}{I_D} \quad (6.9)\ [11]$$

$$V_{EA}=\frac{I_D}{g_d} \quad (6.10)\ [11]$$

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \quad (6.11)\ [12]$$

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (6.12)\ [12]$$

Another FOM for analog application is early voltage, shown in **Figure 6.7(c).** According to the plot, the GS-NCFET with HfO_2 spacers, i.e., S3 has the highest V_{EA} value of 5 V for 0.95 V of V_{gs} because of high drain current, and S0 has the minimum value of early voltage of around 3 V at 0.95 V of V_{gs}. Early voltage is a parameter to characterize the output resistance and is the inverse of the channel length modulation parameter [22-26]. It can be extracted as formulated in Equation (6.10). Further, Output conductance (g_d) measures the variation of I_d concerning the variation of V_{ds} with constant V_{gs} explicit. Moreover, **Figure 6.7(e)** and Equation (6.12) explain the cut-off frequency variation for the different types of spacers. f_T defines the frequency value when the current gain is unity, and it is the most important parameter for evaluating the RF application of a device [27]. GS-NCFET with HfO_2 spacers (S3) has the highest f_T value among S0, S1, and S2, which shows that RF application is better for this device. These trends can also be explained by the fringing of electric fields by the use of high-k spacers.

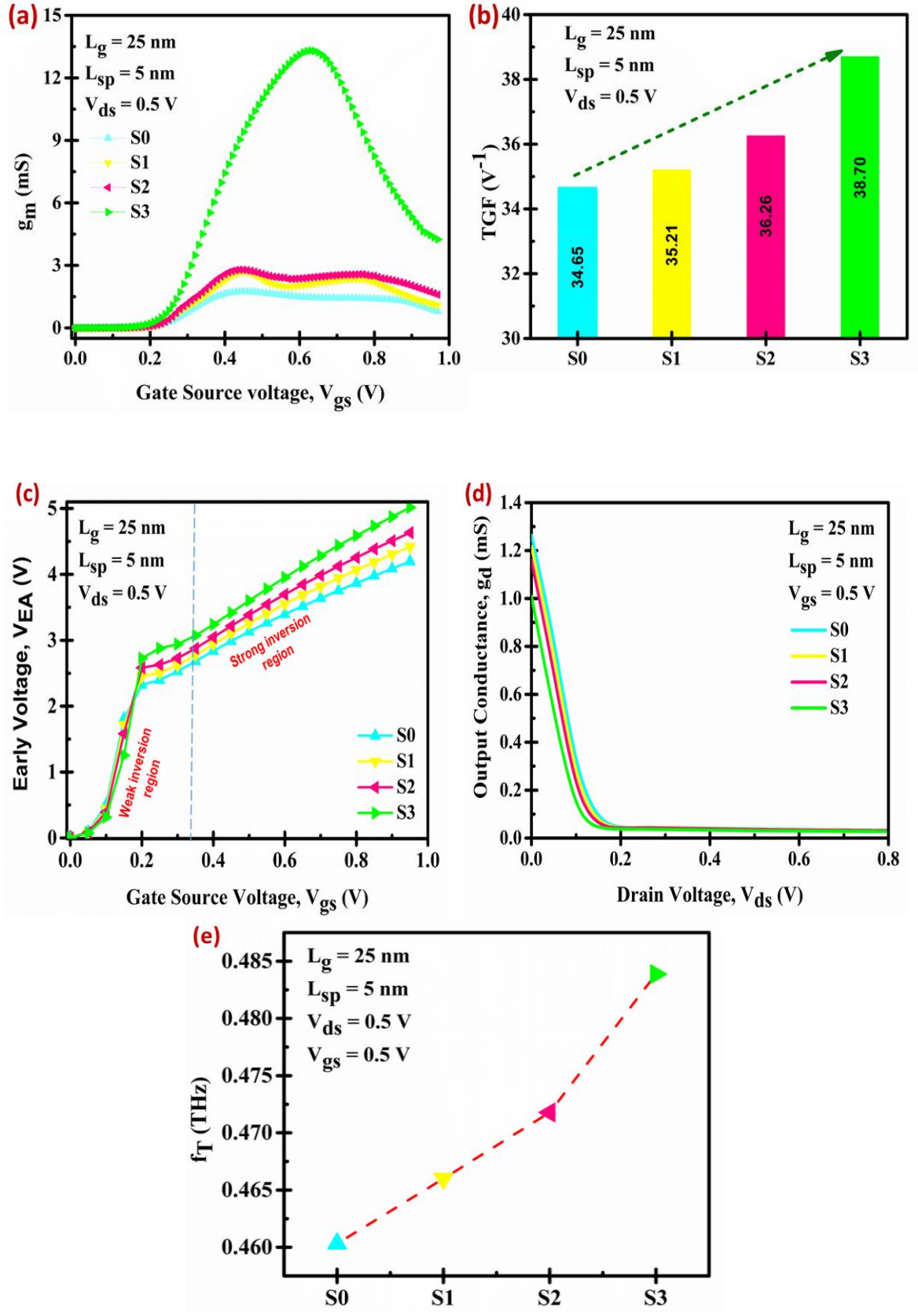


Figure 6.7: Comparison of (a) g_m. (b) TGF. (c) V_{EA}. (d) g_d. (e) f_T curves of GS-NCFET with different types of spacers [14].

6.4.4 Effect of spacers on linearity parameters of GS-NCFET

Figure 6.8(a) gives the combined plots of peak values of GBP and GFP concerning the different types of spacers. As the g_m is higher in the case of S3 configuration, the corresponding GBP is also higher. The gain bandwidth product (GBP) and gain frequency product (GFP) are extracted for device architecture at V_{gs} = 0.5 V and V_{ds} = 0.5 V and formulated as Equation (6.13) and (6.14).

$$GBP = \frac{g_m}{20\pi C_{ds}} \quad (6.13)\ [14]$$

$$GFP = \frac{g_m}{g_d} f_T \quad (6.14)[14]$$

$$TFP = \frac{g_m}{I_d} f_T \quad (6.15)\ [14]$$

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_d} f_T = \frac{g_m}{g_d} \times TFP \quad (6.16)[14]$$

$$g_{m2} = \frac{\partial^2 I_d}{\partial^2 V_{gs}^2} \quad (6.17)[14]$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3} \quad (6.18)\ [14]$$

The parasitic capacitance Cgd (gate-to-drain capacitance) is lower in the case of S3 among other architectures, which is why the ratio of transconductance to Cgd is higher for GS-NCFET with HfO2 spacers (S3) than S0, S1, and S2 [27-34]. Further, in the same **Figure 6.8(a)**, a variation of GFP for all types of spacer devices is shown. Due to the lower value of (g_m/g_d), the total value of GFP of S3 is lesser than S0, S1, and S2. Furthermore, **Figure 6.8(b)** and Equation (6.15) describe the variation of the transconductance frequency product (TFP) concerning V_{gs}. As TGF is high for S3, the TFP value of S3 is also the highest among all S0, S1, and S2 as g_m is higher. Hence, the gain transconductance frequency product (GTFP) is also higher for S3 than S0, S1, and S2, as described in **Figure 6.8(c)** and Equation (6.16). In addition, the linearity parameters like second-order transconductance (g_{m2}) and third-order transconductance (g_{m3}) are shown in **Figure 6.8(d)** and **6.8(e)**, respectively.

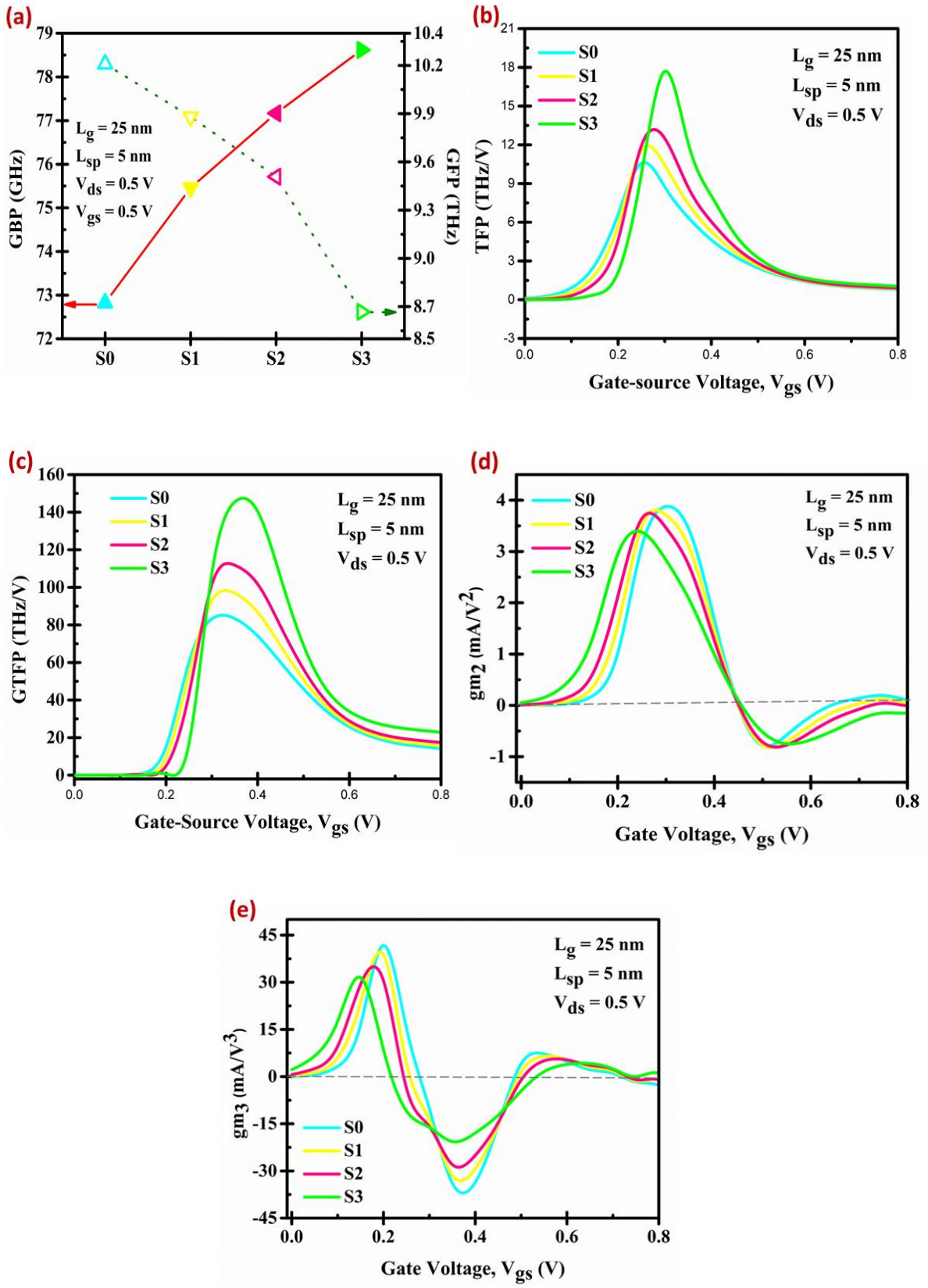
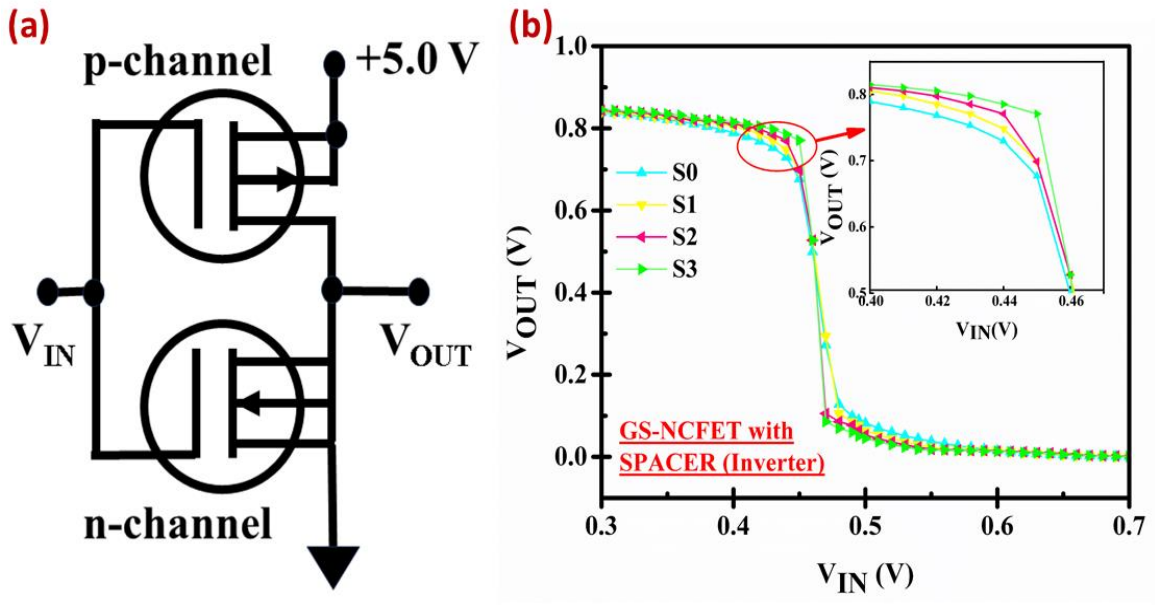


Figure 6.8: Comparison of (a) GBP and GFP. (b) TFP. (c) GTFP. (d) g_{m2}. (e) g_{m3} corresponds toGS-NCFET with different types of spacers [14].

The main reason for non-linearity in RFICs is the non-linearity of devices, as it produces intermodulation and higher-order harmonics in analog/RF circuits [35-40]. These are responsible for wastage in output power. Therefore, minimization of these distortions is a must objective to do. The variation of these parameters is extracted according to Equations (6.17) and (6.18); extracted g_{m2} and g_{m3} of S3 are lowest compared to S0, S1, and S2, which shows the better linearity of a device.

6.4.5 Effect of spacers on parameters of GS-NCFET-based inverter

Figure 6.9(a) demonstrates the GS-NCFET-based inverter schematic. This expresses the requirement for two types of GS-NCFET, n-channel, and p-channel, to work correctly without any delay [41-45]. **Figure 6.9(b)** shows the VTC characteristics of the GS-NCFET-based inverter. Four curves show the corresponding spacer-based inverter plot lines. From the curves, one can conclude that the transition region from high to low output is minimal for the S3-based inverter, which shows the maximum noise margin for the particular circuit. On the other hand, the transition region decreases for S0, S1, and S2 with an increased dielectric constant value, respectively.



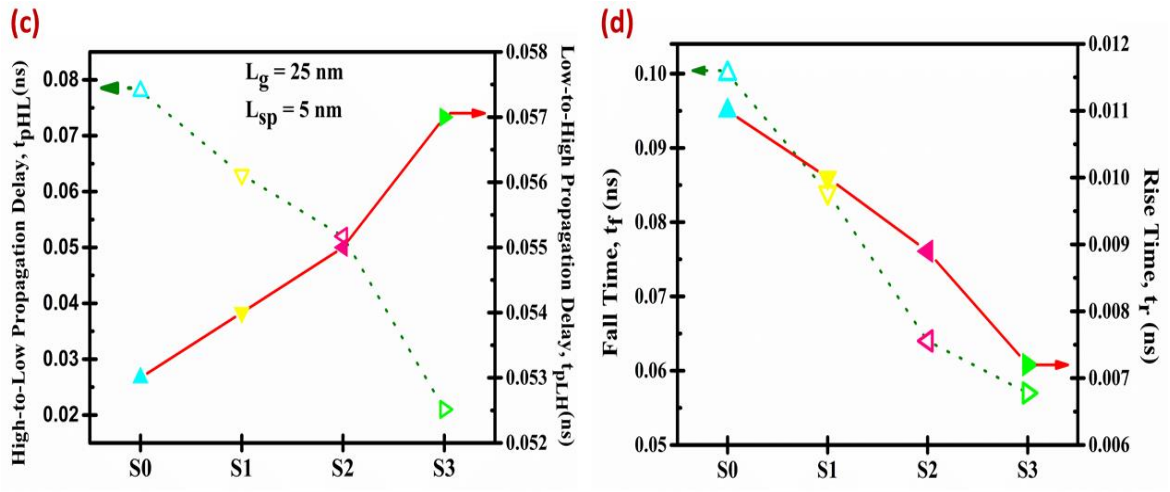


Figure 6.9: (a) Schematics of GS-NCFET-based inverter. (b) VTC curve. (c) propagation delay. (d) rise time and fall time of GS-NCFET-based S0, S1, S2, and S3 inverters [14].

Further, **Figure 6.9(c)** describes the propagation delay low-to-high (t_{pLH}) (and high-to-low (t_{pHL})), which is the delay when output switches from low-to-high (and high-to-low) after input switches from high-to-low (low-to-high). The delay is commonly calculated at 50% input-output switching. The speed of logic is defined by the propagation delays [46-49]. A typical complex system has 20-50 propagation delays per clock cycle. Total propagation delay is calculated with the mean of t_{pHL} and t_{pLH} shown in Equation (6.19).

$$t_p = \langle \frac{t_{pHL} + t_{pLH}}{2} \rangle \qquad (6.19)\ [14]$$

Further, **Figure 6.9(d)** shows the rise (t_r) and fall time (t_f) for concerned device structures, which shows that both parameters have the minimum value for GS-NCFET with HfO_2 spacers, i.e., S3. Rise time (t_r) is defined as the time during a transition when the output switches from 10% to 90%, and fall time (t_f) is referred to as the time taken by the output waveform to switch from 90% to 10% [50-54].

6.5 SUMMARY

This section concludes that GS-NCFET with HfO_2 spacer shows improved results compared to other spacers like air and SiO_2. LCAO-based DFT analysis shows the characteristics of different types of spacers. Maximum PDOS is observed for the HfO_2

spacer with minimum Hartree potential. The band structure shows the allowed transactions for the electrons. The leakage current of S3 is reduced by 25.92 % to S0, and three decimal points increase the switching ratio.

Further, the threshold voltage and DIBL value of S3 decreased by 16.66% and 41.17%, respectively, compared with S0. The SCEs of S3, like SS in linear and saturation, reduced by 14.58% and 17.02% compared to the S0 device architecture. Furthermore, g_m, TGF, g_d, V_{EA}, and f_T improved multiple times more than other device architectures like S0, S1, and S2. Moreover, the linearity parameters like g_{m2} and g_{m3} were minimized in the case of GS-NCFET with HfO_2 spacers. In addition, the VTC characteristics of GS-NCFET are discussed for all types of spacers, and S3 shows the minimum transition region than other device architecture with a 42.85% decrement and better propagation delay with less t_r and t_f. So, the chapter concludes that the GS-NCFET with HfO_2 spacer is a reliable candidate for digital application.

Following a comprehensive analysis of the analog and RF characteristics of the GS-NCFET, it is imperative to address the circuit modeling concerns associated with this proposed device. Therefore, to ensure the device's reliability, it is crucial to explore its device modeling, which will be the primary focus area of the next chapter.

6.6 REFERENCES

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7

CHAPTER

Device and Circuit-level assessment of Gate Stacked NCFET for low-power applications

- *The chapter demonstrates a Gate-Stacked Negative Capacitance Field Effect Transistor (GS-NCFET) study and the device modeling is done using the Verilog A code in the cadence virtuoso tool.*
- *The basic analog parameters like transfer characteristics, transconductance (g_m), and transconductance generation factor (TGF), with an improvement of 81.42% (leakage current), 9.97%, and 21.54%, respectively, for GS-NCFET.*
- *Further, output characteristics and output conductance (g_d) showed a 17.85% decrease in GS-NCFET for the GS-NCFET.*
- *Furthermore, the short channel effects for conventional NCFET and GS-NCFET are discussed.*
- *Moreover, the authors explored the device-to-circuit modeling using the Verilog A code, which uses the device parameter's "tbl" files. The symbols of N-GS-NCFET and P-GS-NCFET are generated using the Cadence Virtuoso simulator.*
- *The digital application of GS-NCFET is shown as NAND, NOR, and NOT logic gates.*
- *It is found that the digital applications of GS-NCFET in terms of logic gates show the proper working of the device with expected input-output curves.*
- *Consequently, the proposed GS-NCFET device would be an attractive solution for low-power and high-performance CMOS circuits.*

7.1 INTRODUCTION

In the realm of electronic circuit design, one of the most important aspects is the representation of devices and components. Whether it is a simple resistor or a complex microcontroller, how these devices are represented in the design process significantly impacts a project's clarity, functionality, and success. Engineers do not work with the physical forms of these devices when designing circuits; instead, they rely on abstract symbols that represent the functionality of each component. This raises an important question: why are device symbols necessary, and why are physical forms inadequate for circuit design? To answer this, it's crucial to delve into the fundamental role that device symbols play in the process and why they offer significant advantages over physical representations [1-3].

Electronic components come in various shapes and sizes, each with unique physical attributes, including pins, packages, and other intricate details. If an engineer were to design circuits using the physical forms of these devices, it would make the design unnecessarily complicated and difficult to interpret. Circuit design is more about the functional behaviour of devices rather than their physical appearance, and symbols offer an abstract representation that focuses on their electrical role within the circuit. Symbols act as a common language for engineers, simplifying what would otherwise be a visually overwhelming and unnecessarily complex process. Also, schematic diagrams serve as the blueprint for electronic circuits, showing how components are interconnected and how signals flow through the system. If these diagrams were created using the physical forms of devices, the result would be cluttered and chaotic. Physical components vary greatly in size, shape, and orientation, making the layout of a circuit diagram cumbersome and difficult to follow [4-6]. Symbols, on the other hand, are standardized and geometrically simple, which ensures that schematics remain clean, organized, and easy to read. The

simplicity of symbols means that a complex circuit can be broken down into digestible parts, with each device represented in a way that communicates its role in the circuit without being bogged down by irrelevant physical details. This clarity is essential for engineers, as they often need to quickly interpret and analyze circuits, troubleshoot problems, or share their designs with others. Moreover, symbols can be arranged in ways that reflect the logical flow of the circuit, whereas physical forms would force the layout to mirror the actual physical constraints of the components, which can be arbitrary and not necessarily conducive to a readable schematic.

Using symbols allows engineers to focus on how the device functions within the circuit without getting distracted by its physical structure. This abstraction is crucial, as it enables engineers to consider the high-level design of a circuit before getting into the details of physical implementation. One of the key benefits of using device symbols is that they provide a standardized method of representing electronic components. In the world of electronics, there are countless different components, each of which may come in different shapes, sizes, and packaging configurations. However, standardized symbols for each type of component ensure that engineers, regardless of their geographical location, language, or the specific brands of components they are using, can understand each other's schematics. Modern circuit design heavily relies on computer-aided design (CAD**)** tools that automate many aspects of the design process. If the design process were based on physical forms instead of symbols, automating would be nearly impossible. CAD tools rely on the abstract nature of symbols to generate netlists (which describe electrical connections) and verify a design's logical correctness. Afterwards, these symbols are associated with physical footprints that describe how the device will be mounted on the PCB. In this way, symbols serve as a bridge between the circuit's abstract logic and the final product's physical reality**.**

This abstraction is essential for enabling modern CAD software's powerful design and verification features [7-9].

In conclusion, converting physical devices into symbols is a fundamental aspect of circuit design because it simplifies the representation of components, enhances the readability of schematics, and focuses on electrical functionality rather than physical appearance. This abstraction, standardization, and clarity are crucial for efficient design, error prevention, and collaboration in the engineering community. Modern electronic design would be far more complicated, error-prone, and less scalable without device symbols. Symbols ensure that circuit design remains a logical, structured, and universally understandable process, paving the way for innovation and effective communication across the global electronics industry.

Device modeling is a critical step in the circuit design process because it allows engineers to predict how components will behave in different scenarios without physically building the circuit [10]. This saves time, reduces costs, and helps optimize the final product's performance. The modeling process involves understanding the device's characteristics, choosing the suitable mathematical representation, implementing it in simulation tools, validating the model against actual data, and refining it for accuracy. Through these steps, engineers can ensure that their designs work as expected, enabling the development of reliable and efficient electronic systems. This chapter uses the Virtuoso tool to model the device for the Gate-Stacked Negative Capacitance Field Effect Transistor (GS-NCFET). The following outline constitutes this chapter's structure: The second section includes the device structure and simulation methodology used. The later part of the chapter discusses the comparison results for conventional NCFET and GS-NCFET obtained through simulation. Then, the next section discusses the device modeling of GS-NCFET using the VISUAL TCAD tool and a symbol generated for n-GS-NCFET and p-GS-

NCFET using the Cadence Virtuoso tool. Lastly, the whole chapter is summarized in the last section.

7.2 DEVICE ARCHITECTURE AND PHYSICAL MODELS

VISUAL TCAD designs and simulates the GS-NCFET discussed in **Chapter 5** and shown in **Figure 7.1** [11]. Meshing is applied to solve the current and voltage equations, leading to the calculation points for equations. A very fine mesh is done in the channel region between the source and drain region to calculate the precise values of current and voltages.

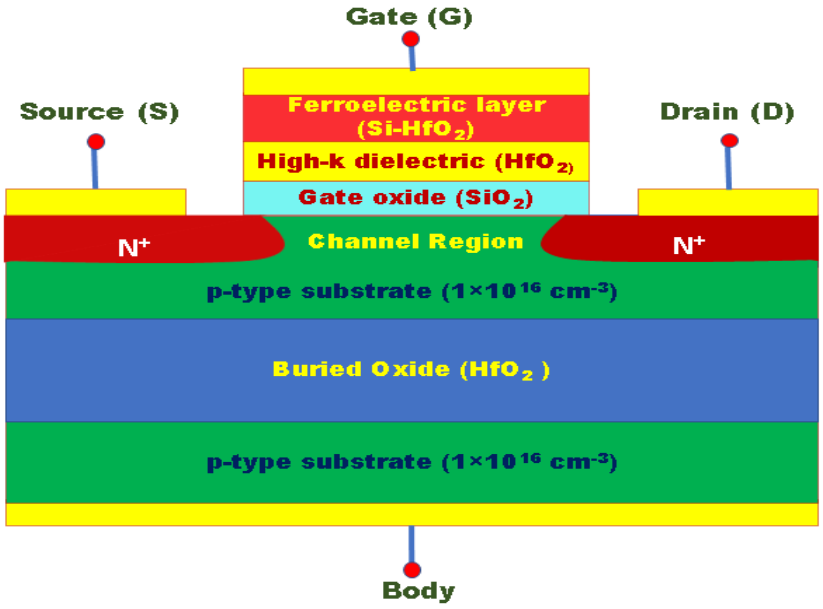


Figure 7.1: Gate-Stacked Negative Capacitance Field Effect Transistor (GS-NCFET) Device architecture [11].

The device simulator includes appropriate models for the effect of standard and high electric fields on mobility, doping dependence mobility, and velocity saturation. The drift-diffusion level 1 equation is used along with Poisson's Equation as solvers in the VISUAL TCAD simulator. The Shockley-Read-Hall recombination (SRH model) and the Fermi-Dirac statistics are discussed in **Chapter 2**. The overall simulation framework is given by the Equations (7.1) – (7.3) [12].

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n E_n + \mu_n \frac{k_b T}{q} \nabla n) - (U - G) \qquad (7.1)\ [12]$$

$$\frac{\partial p}{\partial t} = -\nabla.\left(\mu_p p E_p - \mu_p \frac{k_b T}{q} \nabla p\right) - (U - G) \quad (7.2)\ [12]$$

$$\nabla.\varepsilon \nabla \Psi = -q(p - n + N_D^+ - N_A^-) \quad (7.3)\ [12]$$

Where Ψ is the electrostatic potential of vacuum level, the concentration of electron and hole is noted by n and p, respectively, N_D^+ and N_A^- define the ionized impurity concentrations, and q is the electron charge magnitude. Where μ_n and μ_p are mobilities of electrons and holes, respectively. E_n and E_p are the effective driving electrical fields for electrons and holes and are vector quantities. **Figure 7.2** shows the flowchart of the simulation methodology in the VISUAL TCAD simulator.

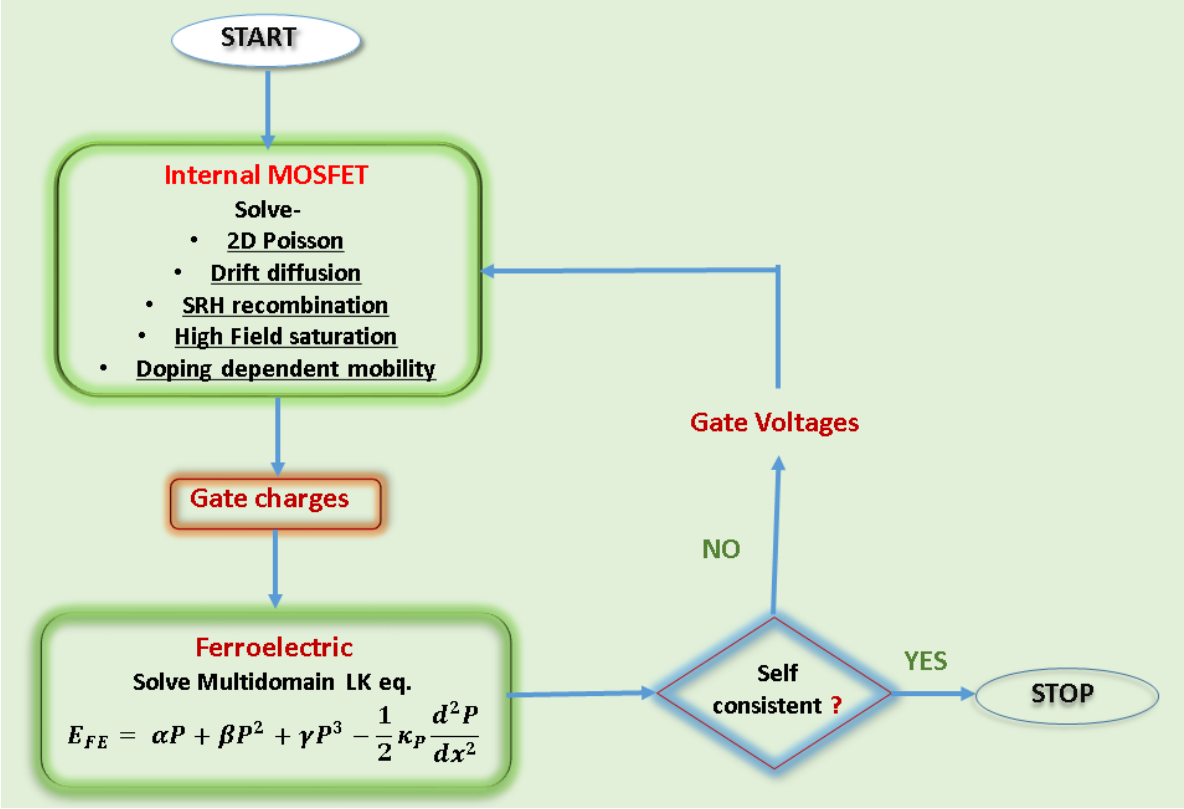


Figure 7.2: Flowchart for the simulation methodology in COGENDA VISUAL TCAD [12].

7.3 RESULTS AND DISCUSSIONS

7.3.1 Comparison of Conventional NCFET and GS-NCFET

A comparison of transfer characteristics of conventional NCFET and modified GS-NCFET is given in **Figure 7.3(a)**, which shows the current leakage improved in the case of GS-NCFET. GS-NCFET shows 3.96 × 10^9 A/μm I_{off} current, whereas conventional NCFET shows 2.10 × 10^8 A/μm leakage current.

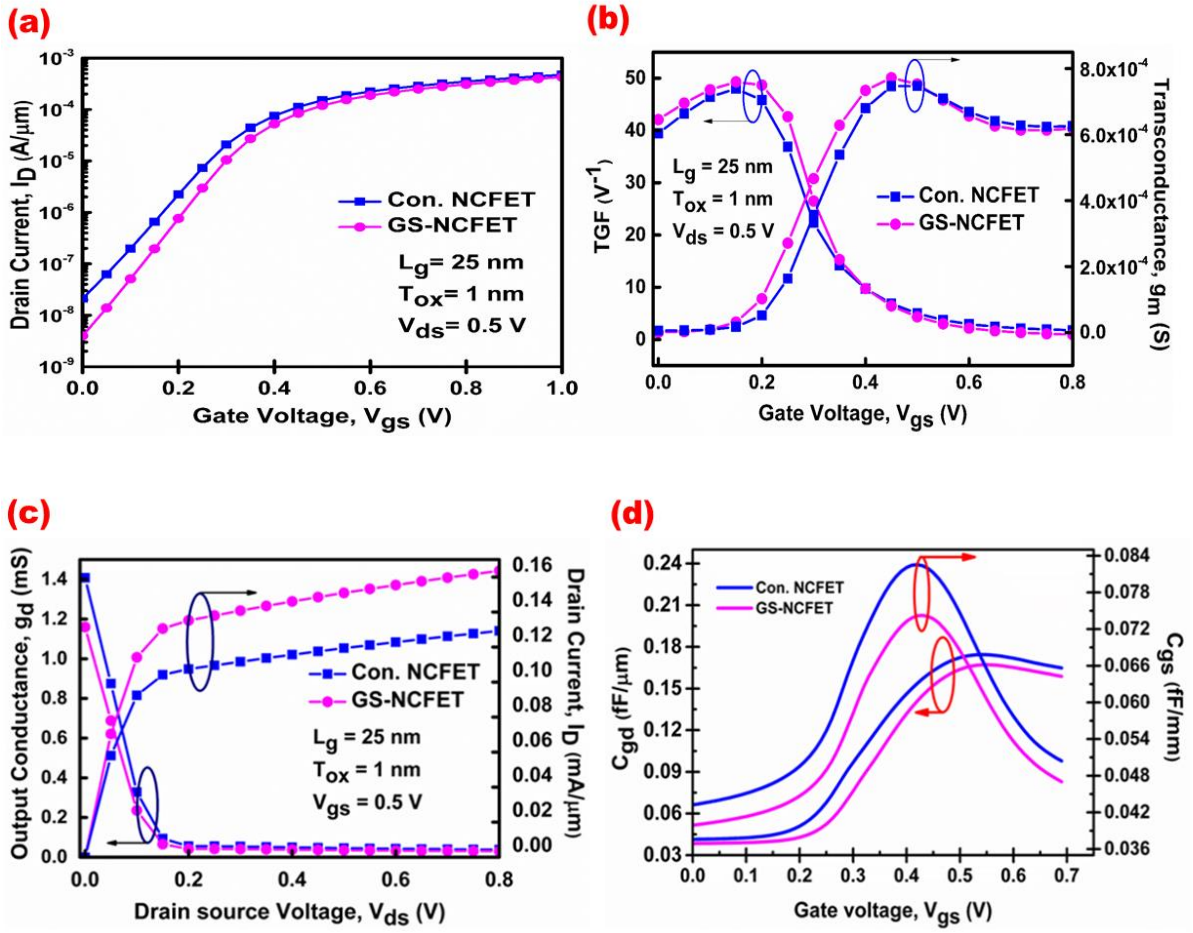


Figure 7.3: Parameter comparison of conventional NCFET and GS-NCFET (a) I_D – V_{gs}. (b) g_m and TGF. (c) I_D – V_{ds} and g_d. (d) C_{gd} and C_{gs} correspond to V_{gs}.

Decreasing the leakage current of GS-NCFET also improves the switching ratio of the device structure, which defines the stability of the device. Further**, Figure 7.3(b)** shows the transconductance (g_m) and transconductance generation factor (TGF) of both device structures. The device's transconductance is a crucial parameter that defines its

amplification capability. It represents the change in the output current (drain current, typically denoted as ΔI_D) concerning a change in the input voltage (gate-source voltage, denoted as ΔV_{gs}). It is mathematically expressed in Equation (7.4) [12]:

$$g_m = \frac{\Delta I_D}{\Delta V_{gs}} \quad (7.4)\ [11]$$

$$\mathrm{TGF} = g_m / I_d \quad (7.5)\ [11]$$

$$g_d = \frac{\Delta I_D}{\Delta V_{ds}} \quad (7.6)\ [11]$$

The peak value of g_m for the GS-NCFET is higher in comparison to the conventional NCFET, which is desirable for higher gain, amplifies the signal more efficiently, and linearity in amplification characteristic, which means the output signal closely resembles the input signal without the significant distortion, etc. and also the higher TGF value of GS-NCFET demonstrates its higher device efficiency and better gain performance at lower voltages values expressed in Equation (7.5). Moreover, **Figure 7.3(c)** shows the higher drain current in output characteristics for GS-NCFET compared to conventional NCFET, which indicates more conductivity and lower resistance, which are desirable for various applications like switching, amplification, etc. Lower output conductance (g_d) ensures the circuit can drive loads efficiently without significant voltage or current variations [13-14]. The mathematical expression for g_d is shown in Equation (7.6). Also, the parasitic capacitances in the device are reduced significantly, as shown in **Figure 7.3(d).**

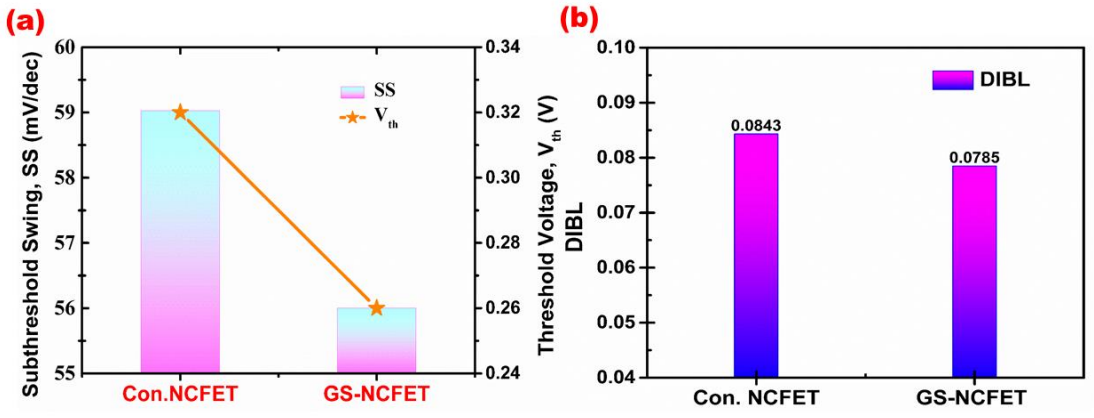


Figure 7.4: Comparison of (a) SS and V_{th} (b) DIBL of conventional NCFET and GS-NCFET.

Other essential factors on which the device's performance depends are short channel effects like drain-induced barrier lowering (DIBL) and subthreshold swing slope (SS), which have to be reduced to get better performance. A small SS value gives better channel control due to less leakage current at the same voltage, or we can say that it provides a better switching ratio (I_{on}/I_{off}) for a device [6-7].

$$SS = \frac{\partial V_{gs}}{\partial log I_D} \quad (7.7)[12]$$

$$DIBL = \frac{\partial V_{th}}{\partial V_{ds}} \quad (7.8)[12]$$

With the help of Equation (7.7), we can find the value of the subthreshold swing, shown in the form of a bar graph and V_{th} in **Figure 7.4(a).** DIBL is the other form of channel length modulation. When the channel length becomes shorter, the source and drain come closer, and the potential barrier between them is affected by the drain-source biasing, so carrier punch-through occurs [15-20]. So, for better performance, the DIBL value should be reduced. The value of DIBL is calculated using the formula given in Equation (7.8) and is done for V_{th} at V_{ds} = 0.5 V. The estimated values of DIBL for both devices are shown in **Figure 7.4(b)**. We can say that the SCEs are reduced in the GS-NCFET architecture.

7.3.2 Device-to-circuit modeling

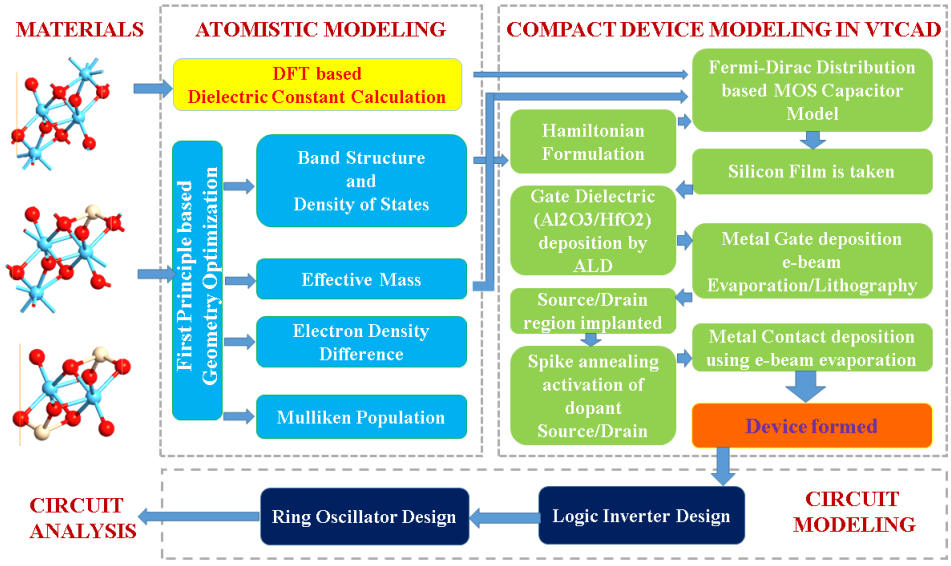
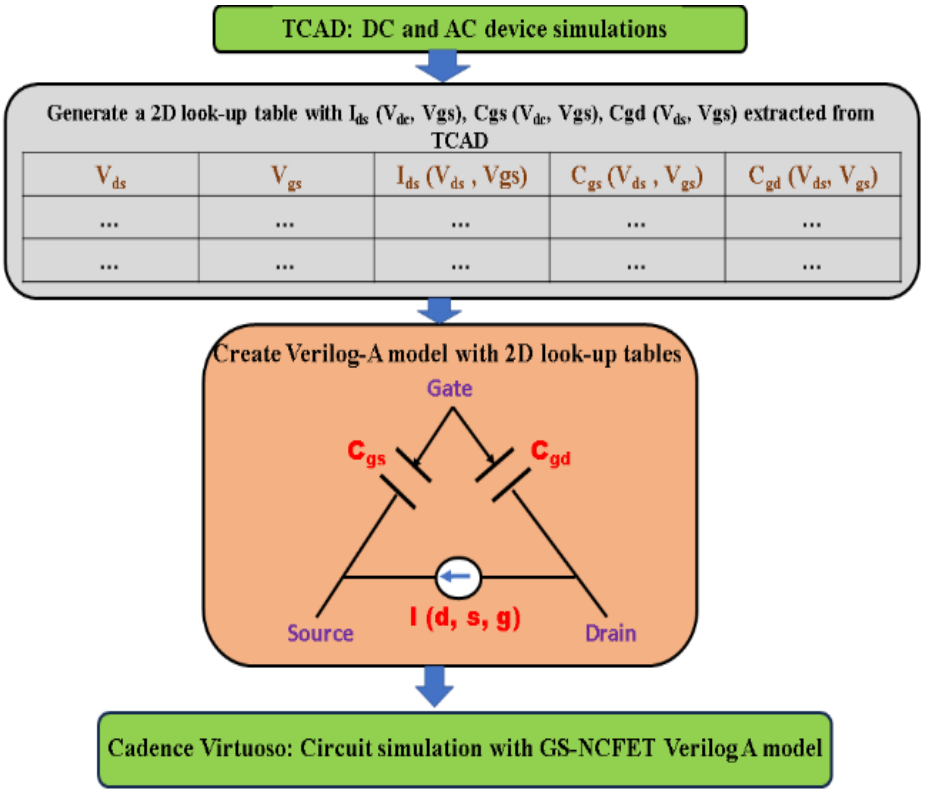


Figure 7.5: Synopsis of "Atom-to-Circuit" Modeling for GS-NCFET structure [12].

Figure 7.5 shows the flowchart for atom-to-circuit modeling for the GS-NCFET structure. The DFT analysis of materials is done and explained in **Chapters 3 and 4**. Since compact SPICE models for NCFETs have not yet been recognized. The authors generate the Verilog-A code for the GS-NCFET device for device-to-circuit modeling.



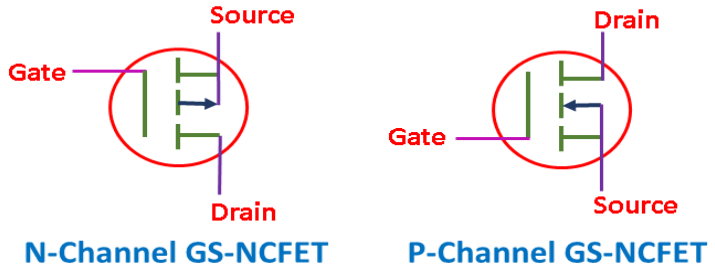


Figure 7.6: Flowchart for the look-up table-based Verilog-A model creation process from TCAD simulations with generated N- and P-GS-NCFET symbols.

This Verilog-A code is based on the two-dimensional look-up tables, including the device characteristics, I_{ds} (V_{ds}, V_{gs}), C_{gs} (V_{ds}, V_{gs}), and C_{gd} (V_{ds}, V_{gs}). Using the VISUAL FAB simulator, the AC and DC simulations yield the current and capacitance characteristics,

respectively. **Figure 7.6** displays the flowchart for the look-up table-based Verilog-A model creation process from TCAD simulations with generated symbols. This Verilog-A code is implemented as a three-terminal device (source, gate, and drain) using the Cadence Virtuoso tool. A sample Verilog-A code for the n-GS-NCFET is displayed in Algorithm 1. The stable model function in this code requires the following three inputs: current or capacitance values (3rd column of the look-up table), V_{ds} (1st column of the look-up table), and V_{gs} (2nd column of the look-up table). The look-up tables in "tbl" assign the values (I_{ds}, C_{gs}, and C_{gd}) based on the terminal voltages. **Figure 7.6** shows the circuit symbols for n- and p-type GS-NCFET generated in the Cadence Virtuoso.

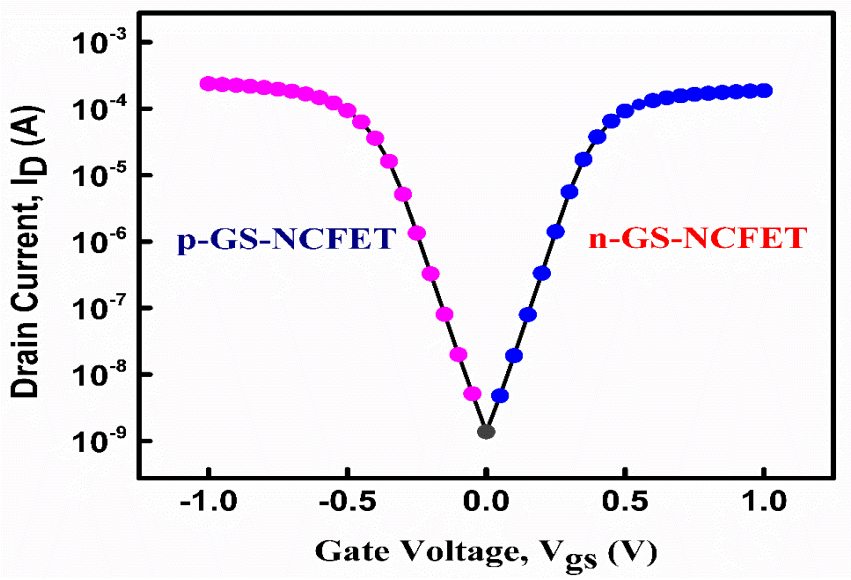


Figure 7.7: Threshold voltage matching for N and P-type GS-NCFET on VISUAL TCAD simulator.

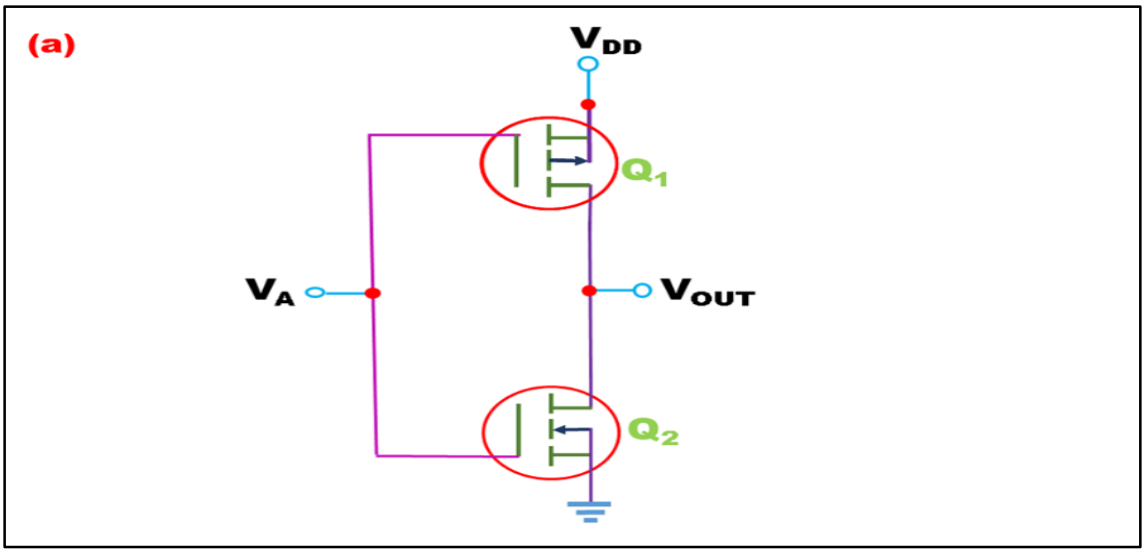
Before modeling a device, one should match N and P-type transfer characteristics so that no dysfunction occurs at V_{gs} = 0 V. This vital parameter is displayed in **Figure 7.7.**

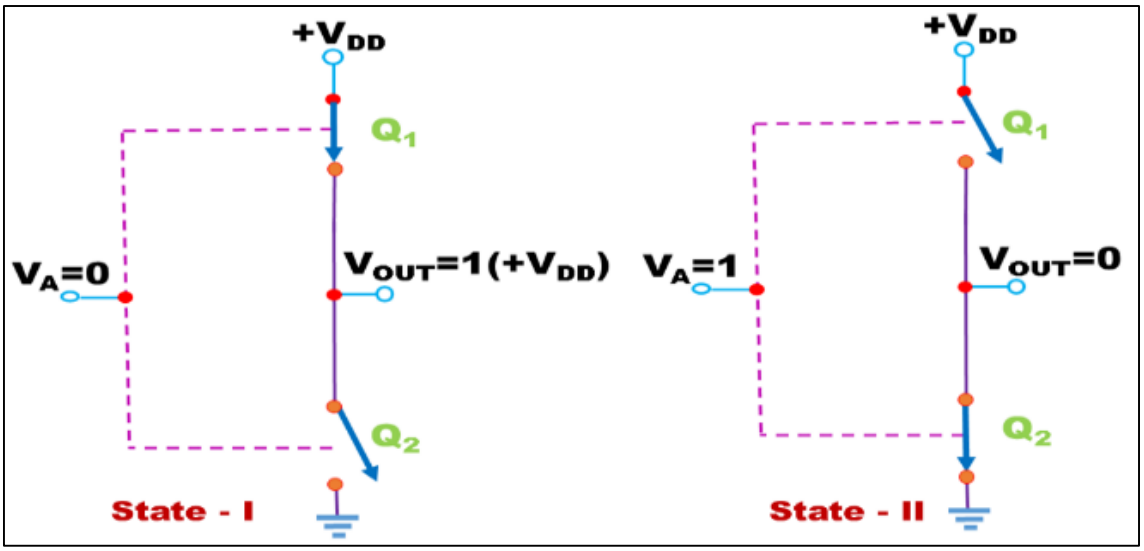
7.3.3 Digital Application of GS-NCFET

7.3.3.1 GS-NCFET-based NOT gate

Any digital circuit's essential building component, the inverter, is utilized to execute a Boolean operation on a single input variable. An NMOS driver transistor and a PMOS load transistor

comprise the complementary MOS (CMOS) inverter. Low-power digital circuits frequently employ CMOS inverters [21-25]. The benefits of CMOS inverter circuits are high output voltage swing, high speed, high noise margin, and low power dissipation. **Figure** 7.8(a) shows that the suggested N-GS-NCFET is a pull-down driver transistor in a CMOS inverter. The pull-up load is the symmetrical P-GS-NCFET. In a CMOS inverter, the output load capacitance determines the delay [26-28]. **Figure 7.8(b)** shows the states according to the input given to the circuit. **Figure 7.8(c)** displays the CMOS inverter's voltage transfer characteristics (VTC) or DC transfer characteristics. The transient and DC analyses of the suggested individual inverter stage are simulated using the numerical simulator Cadence Virtuoso.





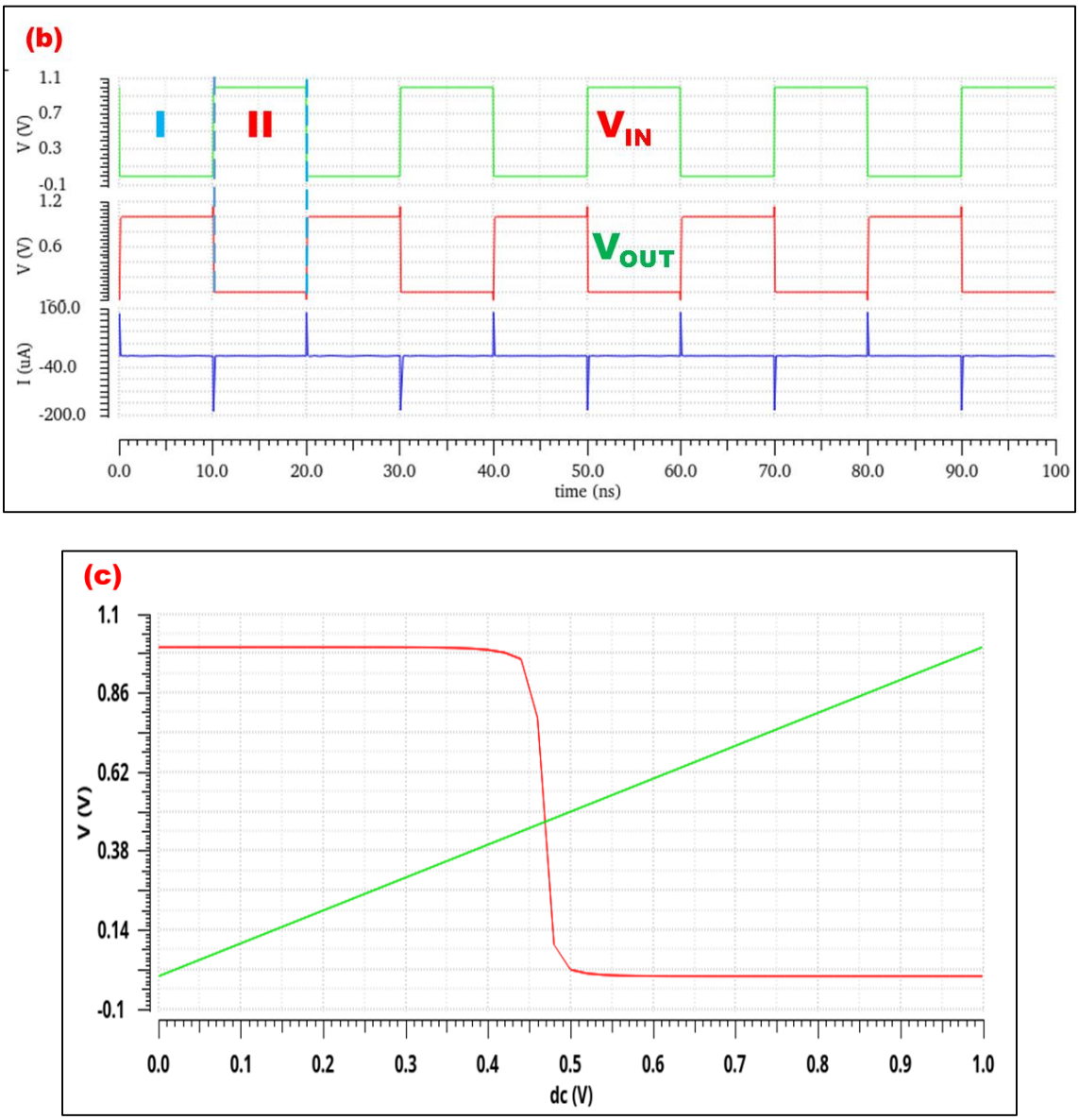


Figure 7.8: (a) schematic diagram of GS-NCFET-based inverter with the possible input-output states. (b) output curve corresponding to GS-NCFET-based inverter. (c) VTC curve of GS-NCFET-based inverter.

The DC transfer characteristics disclose the CMOS inverter's switching threshold and noise margin. The Figure also demonstrates how the practical center of the inverter's characteristics is about $V_{dd}/2$, which is crucial for putting the recommended high-density inverter into practice. The transient analysis of the CMOS inverter is displayed in **Figure 7.8(b).** The inverter's transient analysis provides the output voltage variation concerning the input voltage. This aids in the computation of the output transition delay.

The highest level of noise that a circuit can withstand without causing the logic of the inverter to malfunction is known as the noise margin or NM. The circuit performance and reliability dramatically deteriorate as the noise level rises above this point. Thus, the circuit's noise margin must be maintained as high as feasible [12] [29].

Conversely, Very High NMs result in massive voltage excursions, which lengthen delays and increase power dissipation. There is, therefore, a trade-off between NMs, latency, and power for satisfactory functioning. This implies that a high noise margin impacts the circuit's speed. The period of time a circuit needs to produce an output after an input is applied is known as the propagation delay. The inverter's propagation delay(tp) is determined by averaging the propagation delays (high to low and low to high) that are experienced in the specified circuit [30]. These delays are caused mainly by carrier mobility and device capacitance. Mathematically, tp can be expressed as Equation (7.9)

$$t_p = \frac{t_{LH} + t_{HL}}{2} \quad (7.9)\ [30]$$

Using a GS-NCFET at a 25 nm channel length, the CMOS inverter produced a switching voltage of 0.25 V, a noise margin of 0.283V, and a delay of 0.287n sec, according to the simulation explained in **Chapter 5**.

7.3.3.2 GS-NCFET-based NAND GATE

Two P-GS-NCFETs connected in parallel and two N-GS-NCFETs connected in series comprise this CMOS circuit, which functions as a two-input NAND circuit [31-36]. The quantity of P-GS-NCFETs equals the quantity of N-GS-NCFETs in the NAND circuit 2. To create the two input terminals, the one gate electrode of either P-GS-NCFET is electrically connected to one of the gate electrodes of N-GS-NCFET [37-39]. Additionally, for a symmetrical mode of operation, other gate electrodes of each of the N-GS-NCFET and P-GS-NCFET are electrically connected to each other. **Figure 7.9(a)** displays the design of a 2-input NAND gate utilizing the GS-NCFETs, and it shows the different states

of the NAND gate under the different inputs [40]. The transient analysis of the GS-NCFET-based 2-input NAND gate is displayed in **Figure 7.9(b).**

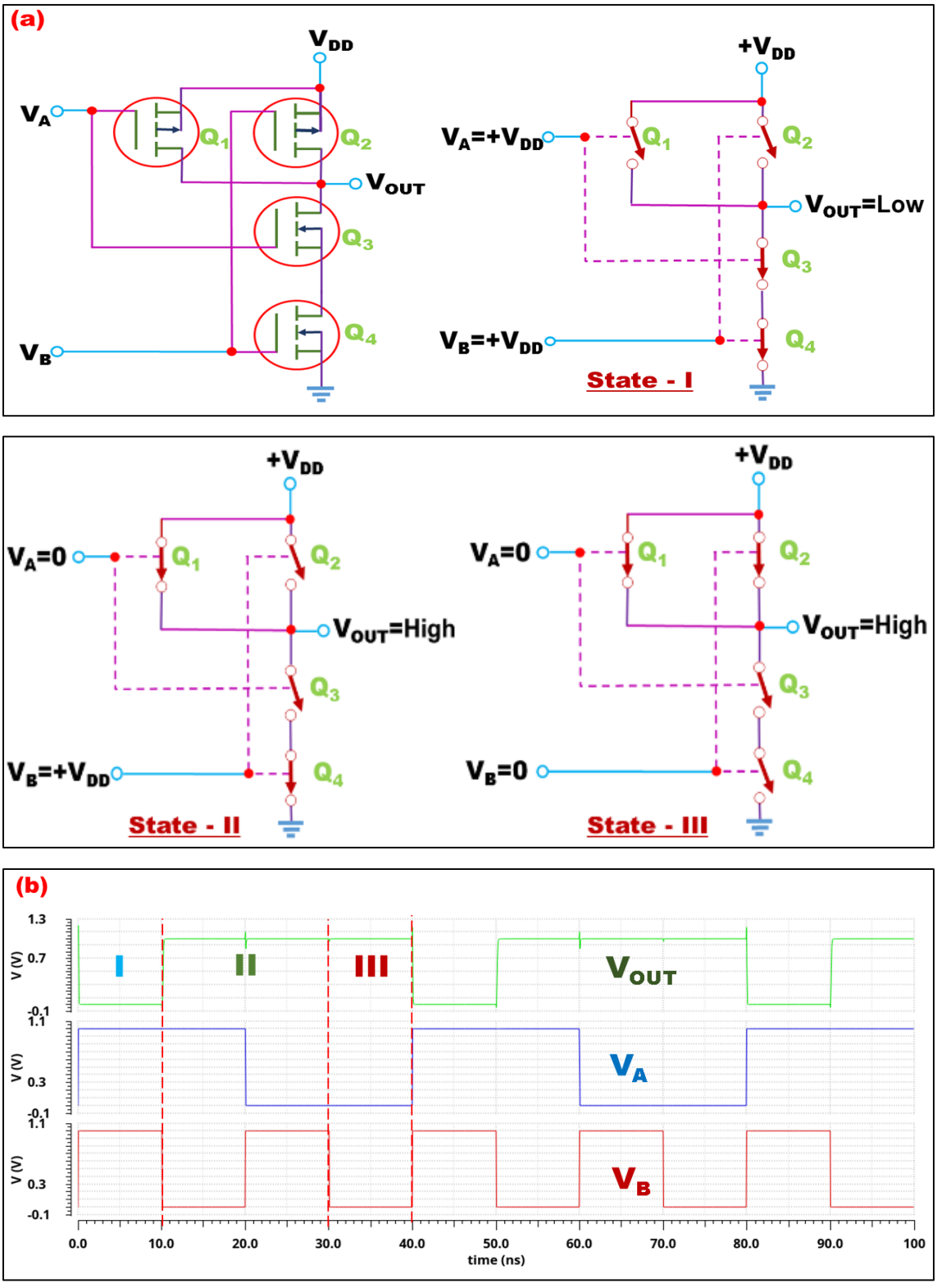
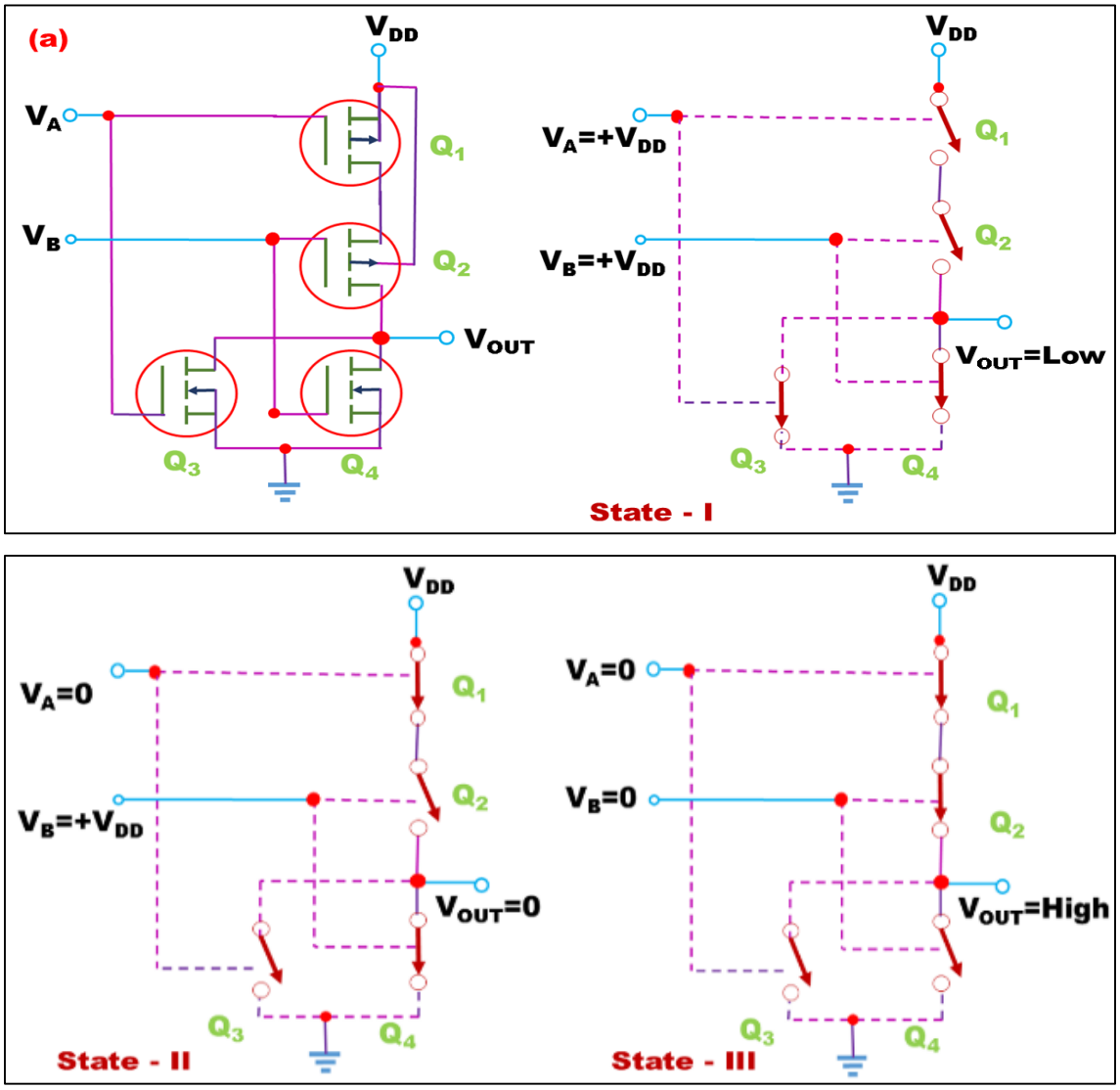


Figure 7.9: (a)Schematic diagram of GS-NCFET-based NAND gate with possible input-output states. (b) Output curve of GS-NCFET-based NAND gate.

7.3.3.3GS-NCFET-based NOR GATE

A number of p-type four terminal GS-NCFETs connected in series and a number of n-type GS-NCFETs connected in parallel make up the CMOS circuit that functions as a multiple-input NOR circuit; the number of P-GS-NCFETs is equal to the number of N-GS-NCFETs [41-44]. To create the same number of input terminals, the two gate electrodes of each of the plurality of P-GS-NCFETs are electrically connected to each other, and one of the gate electrodes of an associated one of the plurality of N-GS-NCFETs [45-47]. Additionally, for the symmetrical mode of operation, the two gate electrodes of each of the plurality of N-GS-NCFETs are electrically connected to each other [48-49].



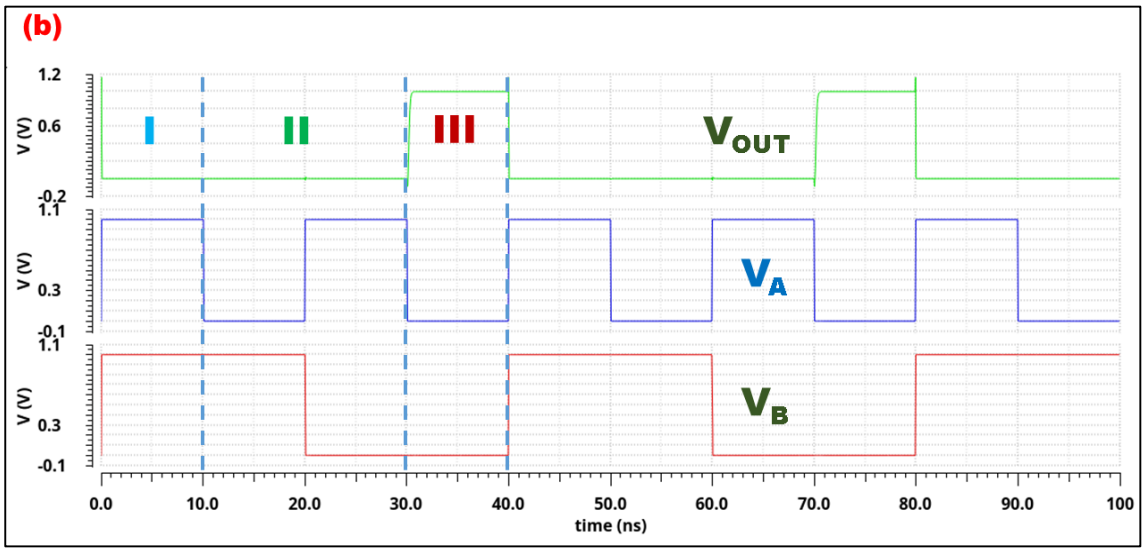


Figure 7.10: (a)Schematic diagram of GS-NCFET-based NOR gate with possible input-output states. (b) Output curve of GS-NCFET-based NOR gate.

The blueprint for the GS-NCFET-based 2-input NOR gate is displayed in **Figure 7.10(a),** and the expected output results are shown in **Figure 7.10(b).**

7.4 SUMMARY

GS-NCFET is a trustworthy digital application architecture with low power consumption and reduced short-channel effects. SCEs for GS-NCFET, like SS, are reduced by 5.11%, and DIBL is improved by 6.88% with a reduced V_{th} of 18.75% compared to conventional NCFET. Further, parasitic capacitances like C_{gs} and C_{gd} are improved by 8.5% and 5.88%, respectively. Circuit modeling using the Verilog-A code is done for VISUAL TCAD simulated GS-NCFET. 25 nm gate length GS-NCFET shows the reduced leakage current, higher transconductance, and TGF with lower parasitic capacitances. Device circuit modeling shows the proper working of logic gates with excellent input-output curves.

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8

CHAPTER

Conclusion and Future Scope

- *This chapter provides a summary of the research conducted throughout this thesis.*
- *Furthermore, the concrete conclusion derived from the presented results is also briefly discussed.*
- *Subsequently, this chapter outlines the potential future scope of work that might be pursued to expand upon the present study.*

8.1 CONCLUSION

This thesis mainly encompasses a Gate-Stack Negative Capacitance Field-Effect-Transistor (GS-NCFET) or Modified NCFET architecture to overcome the challenges faced by conventional NCFET as it provides improved sub-threshold characteristics, suppressed off-state leakage current, extremely high packing density, and reduced fabrication cost and complexity. In this thesis, various scalability and reliability issues of GS-NCFET have been rigorously examined and compared with different architectures. Additionally, approaches such as high-k material-assisted substrate engineering have been used to further increase the performance of GS-NCFET. Starting with a comprehensive study of the analog and RF characteristics of FE-MOSFET has been explored in **Chapter 3,** with the optimization of the ferroelectric material layer in the substrate region of conventional MOSFET at the sub-nano level using extensive simulations. The investigation found that the analog and RF parameters significantly improved for the FE-MOSFET device compared to conventional MOSFET. When compared to conventional MOSFET, a better switching ratio as the I_{off} decreases by 97.05% with a 3.60% increased I_{on} current. Also, the SCEs, like the subthreshold swing lower by 16.75% and 30.42% in linear and saturation regions, respectively. DIBL is reduced by 56.51% and V_{th} by 20.37% and 12.59% in linear and saturation regions, respectively. For the proposed architecture, analog parameters like g_m and TGF enhanced with 977.57% and 67.85%, respectively. The V_{EA} and A_V show improved results for the modified configuration, with 168.81% and 273.60%, respectively.

Furthermore, RF performance parameters like GBP and GFP increased by 864.20%and 3184.02%, respectively. The TFP is enhanced by 1000.69%, and the GTFP improves by 3223.05% for the FE-MOSFET structure. For the modified architecture, the

unity gain frequency is increased by 772.28%. Furthermore, from the noise margin parameters, it is concluded that the transition range for the proposed device structure is better than the conventional MOSFET structure, as NM_L and NM_H are improved by 27.09% and 24.81%. So, with better NM and TR, the FE-MOSFET-based inverter is a better option for digital applications. Thus, from the above results and discussion, the proposed device structure of FE-MOSFET can be considered an alternate choice for designing analog and RF circuit devices. Despite the improved analog and RF performance achieved for the FE-MOSFET device, the reliability of silicon-based hafnium oxide as a ferroelectric material should be considered. Thus, in **Chapter 4**, the DFT-based analysis for Si-HfO_2 as a ferroelectric and the effect of its negative capacitance on SCEs, analog and RF performance of MOSFET, and its digital application is discussed and the structure discussed for this work is termed as Modified NCFET. A quantum ATK and VISUAL TCAD simulator-based insight for Si-doped HfO_2 NCFET using ferroelectric material is considered. Modified NCFET shows amplified results with high ON-current and a better switching ratio of 1.7×10^5. In addition, Modified NCFET suppresses the short channel effects like threshold voltage decreased by 23.75%, and SS reduced by 8.92% compared to conventional MOSFET. Also, the analog parameters of Modified NCFET over conventional MOSFET show improved results. The transconductance of Modified NCFET increased by 34.75% in comparison to the conventional MOSFET structure. Quality factor and device efficiency of Modified NCFET improved by three decimal points and 32.36%, respectively concerning conventional MOSFET structure. Moreover, the cut-off frequency and intrinsic gain show amplified results with 150 times increment and 40.48% results when compared to conventional MOSFET. Better analog performance parameters and reduced short channel effects make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular

MOSFET. Furthermore, when talking about the digital applications like inverters of both these device structures, the noise margin for Modified NCFET comes out to be high when compared to the conventional MOSFET device structure. Its value is 0.32 V for Modified NCFET and 0.31 V for conventional MOSFET structure from the VTC plot. Better analog performance parameters, reduced short channel effects, and higher noise margin make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular MOSFET. Following a comprehensive analysis of the analog and RF characteristics of the Modified NCFET, it is imperative to address the reliability concerns associated with this proposed device. Therefore, to ensure the device's reliability, it is crucial to explore its characteristics. Thus, in **Chapter 5**, the impact of temperature on the static, analog, RF, and wireless performance has been inspected to explore the reliability issues of the Modified NCFET and the proposed device is compared to the conventional NCFET structure. it is observed that Modified NCFET shows improved factors. I_{off} and SS are reduced by 81.17% and 10.28%, respectively, compared to conventional NCFET device architecture. The switching ratio is increased by one decimal point compared to the conventional one. The above study considers the impact of temperature variation on the analog, RF performance, and digital application parameters of the Modified NCFET structure. Simulation results show the variation in different parameters when the temperature rises from 250 K to 350 K with the step size of 25 K. Starting with the basic I_{on}, which increases by 12.39%, and V_{th} is reduced by 30%.

Further, the impact of temperature variations on SCEs is shown as the DIBL is reduced by 32.98% and SS is reduced by 34.74% as the temperature decreases from 350 K to 250 K. Furthermore, as the temperature rises from 250 K to 350 K, the analog parameters shows the following trends: g_m and g_d is enhanced by 9.09% and 2.75%, respectively and TGF is reduced by 58.02%. Also, V_{EA} is enhanced with 19.57%. In continuation, we

examine the effect of temperature on the VTC plot of a Modified NCFET-based inverter. We have taken out three temperature values to extract the variation, which are 250 K, 300 K, and 350 K. If we see the trend with the decreasing temperature, it has been observed that the transition region (TR) decreases as the temperature drops. It becomes 54 times less when the temperature changes from 350 K to 250 K. The noise margin factors are also increased when the temperature falls. The NM_L and NM_H show improvement with 33.43% and 42.26% increments, respectively. The above results show that the Modified NCFET gives better digital application parameters at lower temperatures. Propagation delay is decreased by 67.94% when the temperature rises from 250 to 350 K, providing better and faster switching performance. For further device compatibility, ensuring spacer compatibility is essential for the device's efficiency and longevity. Proper testing and selection of spacers will reduce the risk of malfunction and improve overall device performance. So, **chapter 6** discusses the impact of the high-k spacers on the analog/RF and inverter-based parameter performance of Gate-Stacked NCFET (Modified NCFET). Also, the DFT-based analysis is done for the spacer materials. LCAO-based DFT analysis shows the characteristics of different types of spacers. Maximum PDOS is observed for the HfO_2 spacer with minimum Hartree potential. The band structure corresponding to different spacer materials shows the allowed transactions for the electrons. Four configurations are defined as S0 denotes the GS-NCFET without the spacers, S1 denotes the GS-NCFET with 5 nm length air (k=1) spacers, S2 specifies the GS-NCFET with 5 nm length SiO_2 (k=3.9) spacers, and S3 shows the GS-NCFET with 5 nm length HfO_2 (k=25) spacers around the gate terminal. The leakage current of S3 is reduced by 25.92 % to S0, and three decimal points increase the switching ratio.

Further, the threshold voltage and DIBL value of S3 decreased by 16.66% and 41.17%, respectively, compared with S0. The SCEs of S3, like SS in linear and saturation,

reduced by 14.58% and 17.02% compared to the S0 device architecture. Furthermore, g_m, TGF, g_d, V_{EA}, and f_T improved multiple times more than other device architectures like S0, S1, and S2. Moreover, the linearity parameters like g_{m2} and g_{m3} were minimized in the case of GS-NCFET with HfO_2 spacers. In addition, the VTC characteristics of GS-NCFET are discussed for all types of spacers, and S3 shows the minimum transition region than other device architecture with a 42.85% decrement and better propagation delay with less t_r and t_f. So, the chapter concludes that the GS-NCFET with HfO_2 spacer is a reliable candidate for digital application.

Following a comprehensive analysis of the analog and RF characteristics of the GS-NCFET, it is imperative to address the circuit modeling concerns associated with this proposed device. Therefore, to ensure the device's reliability, it is crucial to explore its device modeling, which is the primary focus area of **Chapter 7.** Circuit modeling using the Verilog-A code is done for VISUAL TCAD simulated GS-NCFET. 25 nm gate length GS-NCFET shows the reduced leakage current, higher transconductance, and TGF with lower parasitic capacitances. Device circuit modeling shows the proper working of logic gates with excellent input-output curves. The ferroelectric materials which can be investigated for the GS-NCFET application are listed below:

Here's a table of ferroelectric materials that have shown improved results in Negative Capacitance Field Effect Transistors (NC-FETs):

Thus, GS-NCFET can be considered a promising candidate for use in low-power, analog, RF, and high-performance CMOS circuits due to its high switching ratio, lower leakage current, better reliability in terms of temperature, and superior static, analog, and RF performance, suppressed SCEs and parasitic capacitances.

Ferroelectric Material	**Crystal Structure**	**Dielectric Constant (εr)**	**Remanent Polarization (μC/cm²)**	**Coercive Field (kV/cm)**	**Key Advantages**
Hafnium Zirconium Oxide (HZO)	Orthorhombic	~20-40	10-30	100-200	CMOS-compatible, Scalable, Low-thermal budget
Hafnium Oxide (HfO_2) (Doped with Si, Zr, or Y)	Orthorhombic	~20-35	5-20	100-250	High stability, Compatible with existing technology
Lead Zirconate Titanate (PZT)	Perovskite	~300-1000	30-50	50-100	High polarization, Established material
Barium Titanate ($BaTiO_3$)	Perovskite	~1000-4000	20-30	5-50	High permittivity, Fast switching
Strontium Bismuth Tantalate (SBT)	Layered Perovskite	~200-400	10-25	50-150	Fatigue resistance,

					Stable ferroelectric properties
Doped Hafnium-based oxides ($Hf_{1-x}Zr_xO_2$, $Hf_{1-x}Al_xO_2$)	Orthorhombic	~25-50	10-25	100-250	Good scalability, CMOS process compatibility

8.2 FUTURE SCOPE

The primary objective of this thesis is to design and optimize a GS-NCFET device that can address the constraints associated with a conventional NCFET structure. The investigation of the proposed device's immunity to temperature variations has been conducted to ascertain the device's reliability. This thesis primarily focuses on the static, analog, RF, and wireless characteristics of the GS-NCFET device. Engineering schemes like high-k material-assisted substrate engineering have been incorporated to improve the device's performance. Another objective of this research work is to assess the suitability of the proposed device to design the low-power circuits. All research objectives have been achieved through extensive numerical simulations. However, there are some objectives that can be explored as potential future elements.

1. The circuit behavior of the GS-NCFET can be explored to make the proposed device suitable for digital circuit applications such as DRAM, SRAM, and other gated logic designs.

2. The investigation of the noise characteristics of GS-NCFET is a valuable endeavor, particularly noise performance metrics such as cross-correlation, auto-correlation,

noise figures, and others. This exploration highlights the potential of GS-NCFET as a compelling solution for the ongoing integration process in analog and digital design technology and for designing low-noise amplifiers.

3. The research conducted in this thesis does not consider the presence of interface trap charges (ITC). Thus, it is crucial to analyze the proposed device for both mobile and stationary ITCs to understand the reliability implications regarding defects.

4. Only silicon is examined as channel material in this thesis work. However, there is potential for further investigation into other materials, including III-V compounds and 2D materials like graphene. These materials exhibit enhanced carrier mobility, and efforts can be made to make the proposed device compatible with high-speed applications, such as high-frequency communication devices.

5. A ferroelectric material as part of its gate structure can be replaced with other ferroelectric materials. The proposed GS-NCFET with different ferroelectric layers can be examined to work better.

6. Moreover, the design of the biosensor device may be engineered to effectively identify and measure other viruses, such as influenza, HIV, and SARS-CoV-2. Alternatively, it can also serve as a gas sensor capable of detecting hazardous chemicals.

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ORIGINAL PAPER

TCAD investigation of ferroelectric based substrate MOSFET for digital application

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Abstract
The present investigation is focused on the analog/RF performance of ferroelectric (FE) based substrate metal oxide semiconductor field effect transistor (MOSFET) for digital application as an inverter. Short channel effect (SCEs) reduced significantly with improvement in switching ratio (I_{on}/I_{off}). The simulation shows the immunity towards the parameters like transconductance (g_m), transconductance generation factor (TGF), early voltage (V_{EA}) and the intrinsic gain (A_V) which allows the device to look into digital application. Also, the RF performance parameters come out to be superior for the proposed device structure, as the gain frequency product (GFP) and gain bandwidth product (GBP) enhanced by 100 and 10 folds, respectively. Further, RF investigation shows the enhanced results as attributed with peak values for transconductance frequency product (TFP) and gain transconductance frequency product (GTFP). The transient analysis shows an improvement in the noise margin (NM) for FE-MOSFET structure. Thus, the proposed architecture can be an attractive alternative for the digital application.

Keywords Ferroelectric material · Subthreshold swing · analog/RF parameters · Transient analysis · Drain induced barrier lowering

1 Introduction

As the situation of current increasing demand to follow the high performance and ultra-low power circuits has motivated the semiconductor industry to downscale the transistors which also states by Moore's law [1]. But with the following of this trend, CMOS technology is getting towards its fundamental limits of scaling down. As the size of the transistor scales down that means the length of the channel in the device decreases, the SCEs like channel tunneling, drain induced barrier lowering, subthreshold swing value start dominating and affect the performance of the device [2–4]. With scaling below 100 nm, the control of the gate over the device channel becomes poor, due to which the SCEs start to dominate. Other issues from which the device performance suffers is pin-point ultra-sharp S/D junction's formation. Some of these effects are reduced by junctionless field effect transistors in which doping species in all regions are the same [5]. Also gives better protection against SCEs in comparison to conventional CMOS devices.

Another challenge with the decreasing size of the transistor comes from power dissipation. Now, with reduction of threshold voltage for same device speed and increasing current exponentially, the static power dissipation is new objective sets for transistors. Whether it looks very difficult to achieve both things with balance but there is a possible way to maintain the stability between device performance and power dissipation which is the subthreshold swing value of a device [6]. It represents the amount of applied gate voltage that is required to change the current by one decade and given by

$$SS = \frac{k_B T}{q} \frac{d\log_{10} I_D}{dV_{gs}} \quad (1)$$

For a conventional MOSFET, the value of SS is ≥ 60mV/decade. From the formula (1), we can say that as the value of SS lowers, this means the needed applied gate voltage becomes less to switch on the transistor [7, 8].

Furthermore, the next challenge is to increase the gate direct tunneling by reducing gate oxide thickness which gives the decrement in leakage current [9, 10]. The technical

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solution for this situation is proved by the use of high-k dielectric materials like hafnium oxide (HfO_2) (k=25). This can be used in the gate stack of the transistor with a combination of silicon oxide (SiO_2) as the effective oxide thickness (EOT) stays constant [11–14]. As HfO_2 cannot be directly deposited on the Si substrate because it forms the oxide composites at the interface of the gate stack and substrate region which offers the resistance at the interface. So, with maintaining the interface quality, HfO_2 always deposited on the top of SiO_2 in the gate stack of the transistor.

In the near past, the use of ferroelectric material in the gate stack of MOSFET gives better immunity to the device performance because FE material shows the behavior of negative capacitance which can be observed from their charge energy curve [15, 16]. So we can use the ferroelectric materials in many possible ways to redefine the architecture of existing MOSFET structures. For that, a suitable example of FE materials is HfO_2 based FE (HfO_2FE) [17]. Basically, we know that the HfO_2 is high-k dielectric material but when it deposited with chemical vapor deposition, its properties show the ferroelectric behavior [18].

Thus, by considering all the conceptions, we designed a new architecture of MOSFET in which we use a ferroelectric material (HfO_2FE) sandwiched in between the high-k dielectric material HfO_2 in the substrate region with the addition of HfO_2 in the gate stack of the device. We named it as ferroelectric based substrate metal oxide semiconductor field effect transistor (FE-MOSFET) as shown in Fig. 1. In the last several years, there is a sufficient increase in demands for higher battery backup and portable electronic devices. And to the matchup, this demand with the addition of speed performance, the concept of Moore's law has been followed for decades. And with help of this system-on-chip (SoC) concept, we can integrate several independent systems on a single chip. The main challenge in the SoC technology is device optimization. Accordingly, the persistence of this work is to consider the structure and performance of the device for the digital application. Analog/RF performance parameters for FE-MOSFET has been examined broadly. In this work, we study the FE-MOSFET with its analog/RF metrics that are significant for RF applications such as GBP, GFP, TFP and GTFP. It is examined from the simulation that modified FE-MOSFET shows the better results in comparison to the conventional MOSFET structure. FE-MOSFET gives the higher switching ratio, lesser leakage current, better subthreshold swing value etc. with the reduction of the threshold voltage value. Starting from the basic introduction of FETs in Section 1, Section 2 briefs the device structure. The simulation methodology is explained in Section 3, Section 4 deals with the analog/RF performance parameter comparison of these two devices. Further, the digital application of FE-MOSFET is discussed and compared with conventional MOSFET in Section 5. Lastly, the concluding remarks are added in Section 6.

2 Device structure

Fig. 1 illustrates the device structure of conventional MOSFET and ferroelectric based substrate MOSFET (FE-MOSFET). The gate length (L_g) for both device structure is 25 nm and the length of source and drain region (S/D) extensions are 10 nm on both side of the gate. The silicon oxide thickness is fixed to 0.5 nm and also the thickness of high-k dielectric material HfO_2 is kept at 0.5 nm in the gate stack of the proposed device structure. In the conventional MOSFET device structure, SiO_2 with a thickness of 1 nm is used as the gate oxide.

Also, silicon material is used as the substrate region for both the device. The modification is done in the substrate region of the proposed device structure or FE-MOSFET structure. A layer of FE material is sandwiched in between the layers of HfO_2. The silicon substrate region in both the device is doped with p-type species of 1×10^{16} cm^{-3}. Also, the doping concentration for the source/drain region is 1×10^{18} cm^{-3} and of n-type. The material used for the gate terminal is Npoly silicon has a work function (φ_m) at 4.5 eV. The Landau's parameters for the FE material are a= - 1e+07 and β = 8.9e+08 [18].These all default dimensions are tabulated in Table 1

3 Simulation methodology

The VISUAL TCAD simulator has been used to simulate both device configurations. In the complete simulation results, the drain-source voltage (V_{ds}) is set at 0.5 V and gate source voltage (V_{gs}) is varying from 0 to 1 V. Temperature is fixed at 300 K for all the simulation work. Also, many physical models are used to explain different concepts in the simulation work like recombination effects, Shockley-Read-Hall (SRH) model briefs the trap charges existence at the interface. Arora model defined the concentration dependent mobility. The Fermi-Dirac statistics are used for accuracy in the results. The calibration on visual TCAD simulator is done for the existing results of 35nm MOSFET as in published work of G. Roy et al. That's why we used the dimension of 35nm only for the calibration part. The calibrated results of 35 nm MOSFET are presented in Fig. 2 with constant V_{ds} of 50 mV and 850 mV [19].

4 Results and discussion

4.1 Device Scalability

Fig. 3 shows the variation comparison of drain current (I_D) with respect to the gate source voltage (V_{gs}) at constant drain source voltage (V_{ds}) of 0.5 V in both linear and log scale for

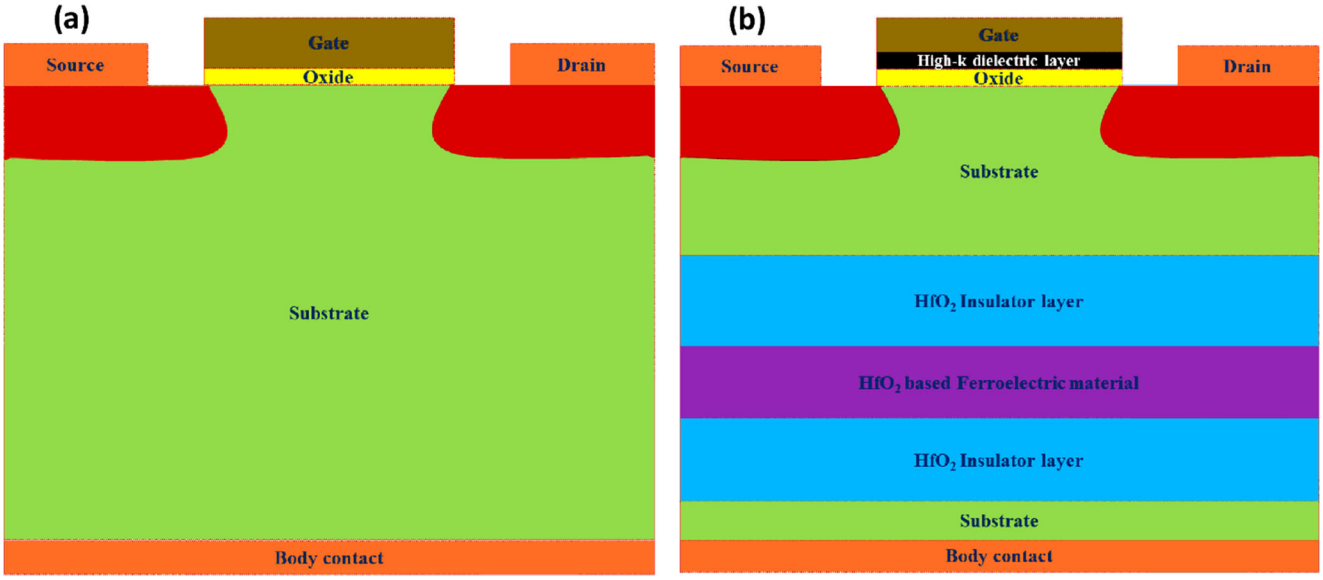

Fig. 1 Systematic architecture of conventional MOSFET (**a**) ferroelectric based substrate MOSFET (**b**)

both the device structures. We can say from the variation comparison that I_D increases exponentially with an increase in the V_{gs} and improvement in I_D is recorded for the modified FE-MOSFET than for conventional MOSFET. As it is found for the modified configuration that the on current (I_{on}) improves with reduction in the off current (I_{off}) or leakage current which gives the higher switching ratio (I_{on}/I_{off}) and enhanced switching speed to the device as shown in Fig. 4. This is attributed due to the reduction in tunneling current and resistance offered by the substrate region modification. Secondly, an important short channel parameter is DIBL which is the second name of channel length modulation. DIBL is responsible for the increase in leakage current at higher constant drain source voltage. So for better device performance, the DIBL effect should be minimized [2–4]. The DIBL value for conventional MOSFET and modified FE-FET is displayed in the same Fig. 4. The threshold voltage (V_{th}) comparison for conventional MOSFET and FE- MOSFET is shown in Fig. 5. V_{th} for a device shows the voltage at which the hole-concentration in the substrate region equate the electron-concentration in the channel region so that the current starts to flow to its maximum value. The threshold voltage for the modified configuration is less than the conventional device structure. This is due to the fact that the ferroelectric material capacitance shows a negative value. This shows that the device can switch from off to on with less value of applied gate source voltage value. The subthreshold swing (SS) value for both the device configuration is displayed in the form of a bar graph for linear and saturation region in Fig. 6. As discussed in Section 1, SS is the important short channel parameter that should be low for better device performance [6]. And from Fig. 6, it is clear that the SS in both linear and saturation region of operation is reduced significantly for FE-MOSFET approaching the ideal value (60mV/dec). It is due to an increase

Table 1 Default device dimension and parameters are taken for the simulation

Parameter	Conventional MOSFET	Modified FE-MOSFET
L_g (nm)	25	25
$L_{S/D}$ (nm)	10	10
T_{ox} (nm)	1	1 (0.5 SiO_2+0.5 HfO_2)
T_{FE} (nm)	0	8
T_{ins} (nm)	0	9
$N_{S/D}$ (cm^{-3})	1×10^{19}	1×10^{19}
N_{ch} (cm^{-3})	1×10^{16}	1×10^{16}
Φ_m (eV)	4.5 (Npoly Si)	4.5 (Npoly Si)

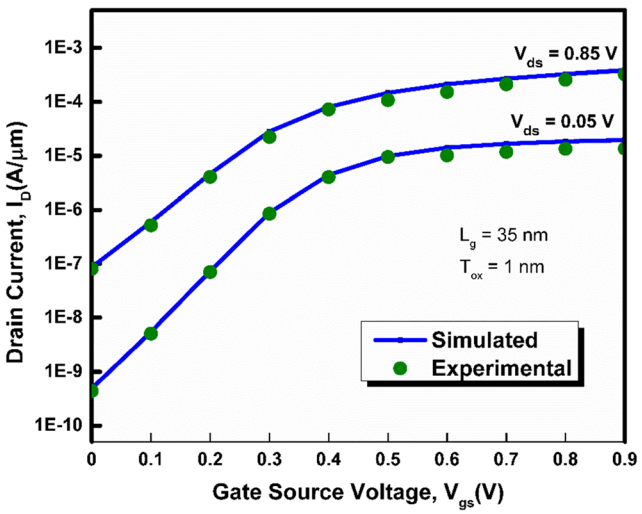

Fig. 2 Calibrated I_D-V_{gs} characteristics of 35nm MOSFET to experimental data

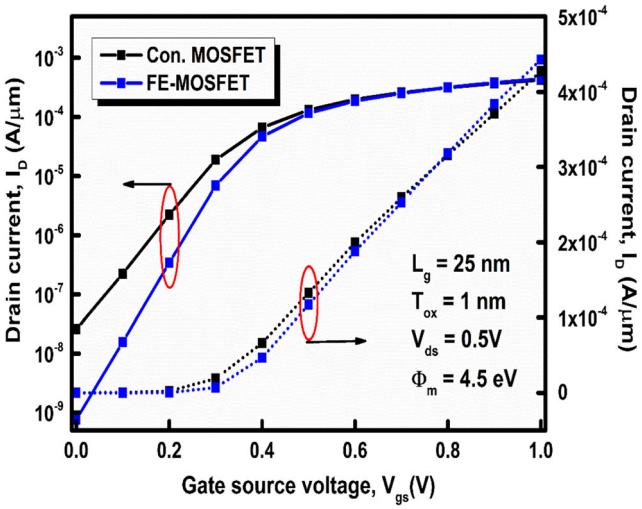

Fig. 3 Variation of I_D with respect to V_{gs} at constant V_{ds} = 0.5 V in logarithmic and linear scale

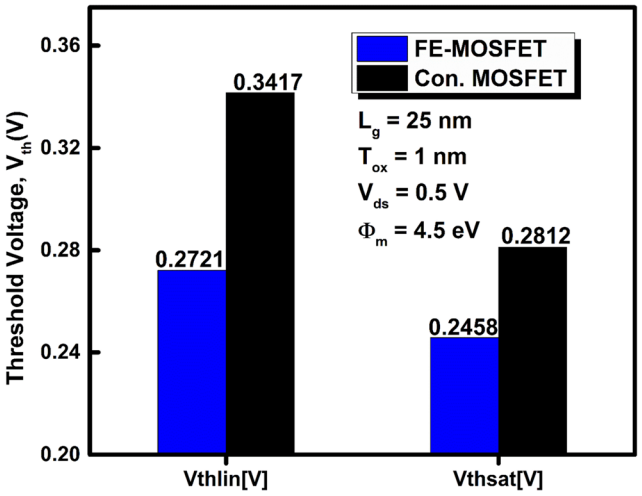

Fig. 5 Threshold voltage comparison for conventional MOSFET and ferroelectric based substrate MOSFET configuration

in gate coupling capacitance with increment in permittivity (k) which improves the gate voltage control on the channel region, thus enhance the SS value.

4.2 Analog metrics

In this part of the paper, from the view of analog performance device application, many important applications like g_m, TGF, V_{EA}, A_V are described with their explanation. Fig. 7 represents the g_m and TGF variation together with respect to the V_{gs} at constant V_{ds} of 0.5 V for both the device structures. Equations (2) and (3) formulates the transconductance and TGF, respectively [20]. From Fig. 7, it is clear that the FE-MOSFET shows the enhanced results with an improved value of g_m and TGF. Transconductance is a very important analog factor for a device as it estimates the overall gain for a device. It can be evaluated from the I_D-V_{gs} characteristics by performing the derivative of I_D with respect to the applied V_{gs} as shown in Eq. (2). Higher value of g_m shows the better control of gate voltage on the channel and hence became the reason of reduced short channel effects [20, 21]. Also, the use of ferroelectric material with a combination of high-k dielectric material enhance the mobile electron concentration and average carrier velocity in the channel region, thus directly increase the g_m. Also, TGF shows the net gain generated per unit power loss for a device as formulated in Eq. (3). A higher value of TGF shows that how efficiently a device can work at low supply voltages. FE-MOSFET configuration reaches the maximum value of TGF. The reason for the higher TGF is the higher drain current and its higher g_m value [22].

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \tag{2}$$

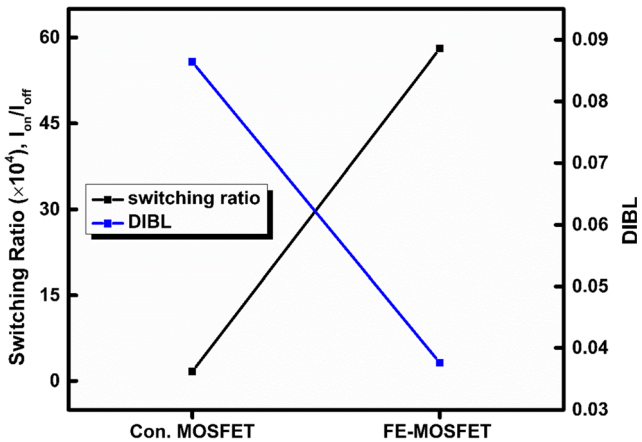

Fig. 4 Comparison of switching ratio and DIBL for conventional MOSFET and ferroelectric based substrate MOSFET structure

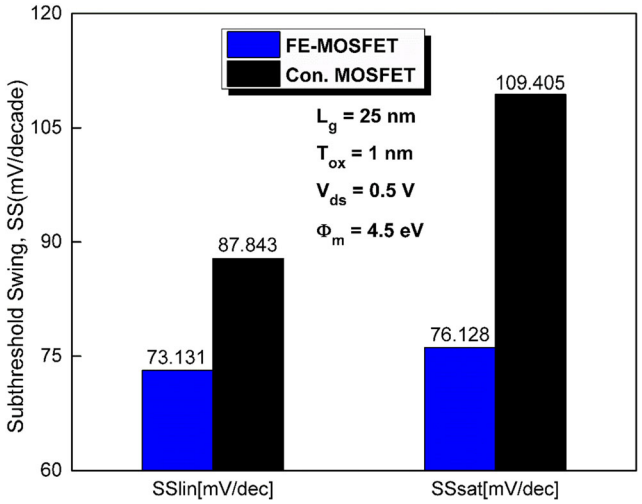

Fig. 6 Subthreshold swing value of conventional MOSFET and FE-MOSFET configuration

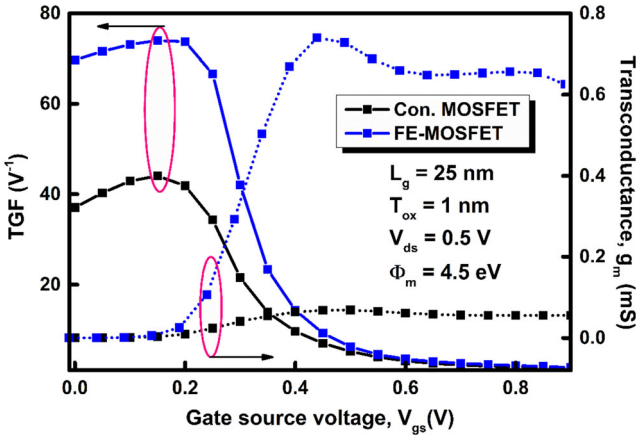

Fig. 7 g_m and TGF variation with V_{gs} for conventional MOSFET and ferroelectric based substrate MOSFET device structure

$$TGF = \frac{g_m}{I_D} \tag{3}$$

$$V_{EA} = \frac{I_D}{g_d} \tag{4}$$

$$A_v = \frac{g_m}{g_d} = \frac{g_m}{I_D} \times V_{EA} \tag{5}$$

The variation of early voltage with the variation of corresponding applied supply voltages is displayed in Fig. 8 for the conventional MOSFET and FE-MOSFET structure. For the improved analog performance of a device configuration, this parameter should be high as possible. Early voltage can find

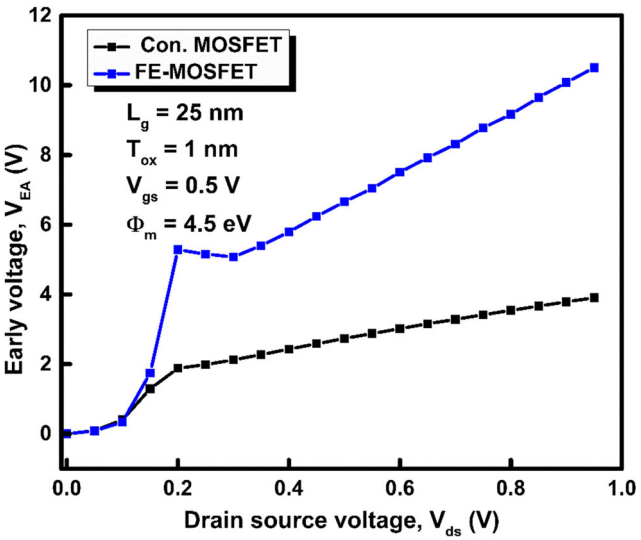

Fig. 8 Comparison of early voltage vs. drain source voltage for conventional MOSFET and ferroelectric based substrate MOSFET structure

out according to Eq. (4) [23, 24]. The highest value of early voltage is recorded for the FE-MOSFET configuration in comparison to conventional MOSFET structure due to the improved SCEs as listed in Table 2. Figure 9 displays the variation of A_V with respect to the variation of V_{gs} at constant V_{ds} at 0.5 V. These value of gain should be high for better performance devices. Also, the maximum value of intrinsic gain is obtained for the FE based substrate MOSFET structure because of the higher V_{EA} and g_m as formulated in Eq. (5). Intrinsic gain defines the overall voltage gain for a device regardless of its bias point [24]. The observed values of SCEs and analog parameters are tabulated in Table 2.

4.3 RF analysis

With keeping the view of RF application, RF parameters play an important role in device performance. Some important RF parameters like unity gain frequency (f_T), GBP, GFP, TFP, and GTFP are evaluated for both conventional MOSFET and ferroelectric based substrate MOSFET device structures. The variation of two parasitic capacitances C_{gs} and C_{gd} as a function of V_{gs} is displayed in Fig. 10. Both the parasitic capacitance plotted in the linear scale. For extraction of these gate to source capacitance and gate to drain capacitance, a small AC signal analysis has been simulated at 1 MHz operating frequency with DC voltage varying from 0 to 1 V with 0.05 step size. In Fig. 10, it is shown that both parasitic capacitances increase gradually with respect to the V_{gs} shows a higher value for the FE-MOSFET than the conventional MOSFET structure due to the high lateral field which directly connects to the increment in charge carrier movement from source to drain side. Another reason for high parasitic capacitances is that there is an increase in gate capacitance with an increase in dielectric permittivity [25, 26]. For gate to source capacitance, the curve shows less increment behavior than the conventional MOSFET but the peak value is shown by FE-MOSFET. Similarly, the curve for drain source capacitance of FE-MOSFET first shows the lower value than the conventional MOSFET but after the certain value around the threshold voltage, it shows the increased behavior in comparison of conventional MOSFET [27].

In next Fig. 11, simulated data of gate capacitance (C_{gg}) is displayed as a function of V_{gs}. The C_{gg} curve shows the same variation as the parasitic capacitances as C_{gg} is a combination of both C_{gs} and C_{gd}. so, a higher value of gate capacitance is shown by the FE-MOSFET than the conventional MOSFET configuration [25–27]. Now, in Fig. 12, the variation of unity gain frequency as a function of V_{gs} is displayed for both the device configuration. Basically, f_T defines the frequency value at which the device obtain unit current gain [28]. The formula used for calculation of f_T is shown in Eq. 6, the maximum value of f_T is shown from the data of FE- MOSFET structure

Table 2 List of analog and electrostatic parameters for conventional MOSFET and ferroelectric based substrate MOSFET

Parameter	Conventional MOSFET	Modified FE-MOSFET
I_{on}(A/ μm)	4.273×10^{-4}	4.427×10^{-4}
I_{off}(A/ μm)	2.587×10^{-8}	7.623×10^{-10}
I_{on}/I_{off}	1.656×10^{4}	0.581×10^{6}
V_{th}(lin) (V)	0.341	0.272
V_{th}(sat) (V)	0.281	0.246
SS_{lin} (mV/dec)	87.844	73.131
SS_{sat} (mV/dec)	109.405	76.128
g_m (mS)	0.068	0.739
TGF (V^{-1})	44.076	73.983
V_{EA} (V)	3.907	10.503
A_V (dB)	13.778	51.477

in a comparison of conventional MOSFET structure as the g_m is higher for the FE-MOSFET structure.

$$f_T = \frac{g_m}{2\pi\left[C_{gs} + C_{gd}\right]} \tag{6}$$

$$GBP = \frac{g_m}{20\pi\left[C_{gd}\right]} \tag{7}$$

$$GFP = [f_T]\frac{g_m}{g_d} \tag{8}$$

$$TFP = \frac{g_m}{I_D} \times f_T \tag{9}$$

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_D} \times f_T = Av \times TFP \tag{10}$$

Figure 13 represents the variation of GBP and GFP with V_{gs} at constant V_{ds} of 0.5 V for conventional MOSFET and FE-MOSFET. GBP and GFP are the essential performance parameter that is used for high-frequency applications [29, 30]. Both parameters are formulated in the Eqs. (7) and (8). As the ratio of g_m to C_{gd} is higher and shows the maximum value for the FE-MOSFET in comparison of conventional MOSFET which shows the better device performance .so, the modified FE-MOSFET shows the enhanced results for GBP than the conventional MOSFET structure. The peak value of GBP indicates the voltage at which the gain of the device becomes maximum [30]. Secondly, the GFP factor is the product of unity frequency gain and intrinsic gain as formulated in Eq. (8) which both are high for the FE-MOSFET configuration than the conventional one. So, as displayed in Fig. 13, the GFP shows a gradual increase with the increase in

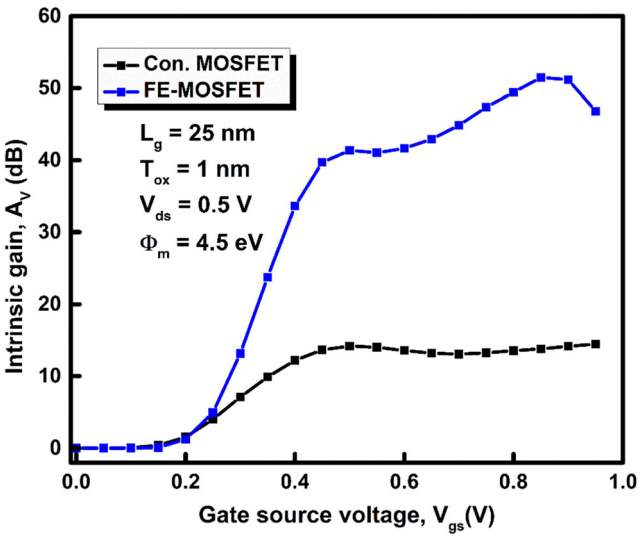

Fig. 9 Variation of A_v with V_{gs} at constant V_{ds} = 0.5 V for conventional MOSFET and ferroelectric based substrate MOSFET structure

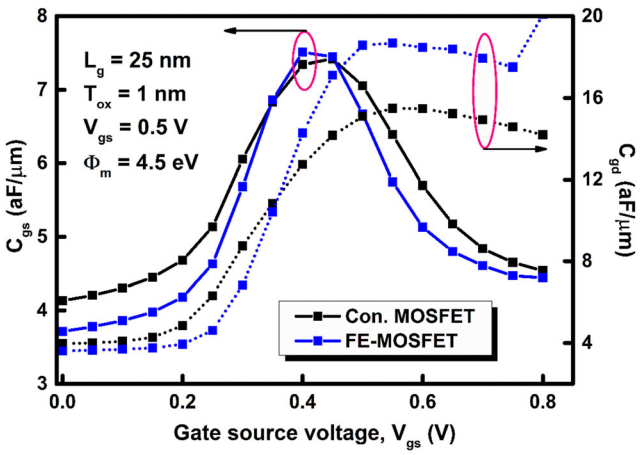

Fig. 10 Variation of parasitic capacitance (C_{gs} and C_{ds}) with V_{gs} at V_{ds} = 0.5 V

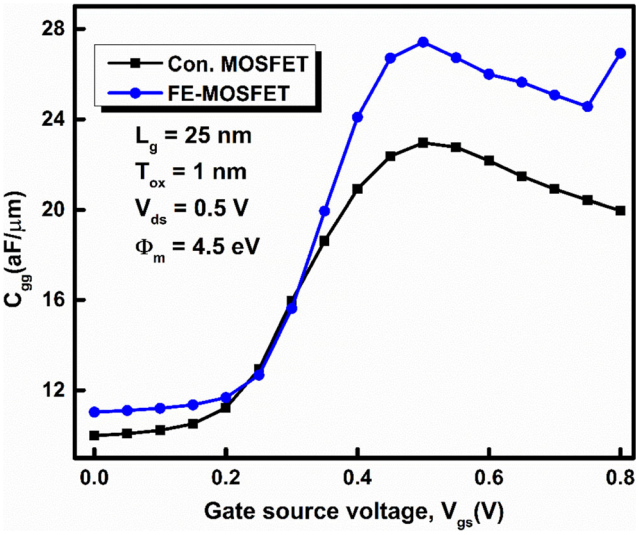

Fig. 11 Variation of gate capacitance with V_{gs} at constant V_{ds} of 0.5 V for conventional MOSFET and FE-MOSFET

gate source voltage and the maximum peak value of GFP is shown by the modified FE-MOSFET structure in a comparison of conventional MOSFET structure.

Other important RF performance parameters are TFP and GTFP as formulated in Eqs. (9) and (10), respectively. Fig. 14 illustrates the variation of TFP and GTFP with an increase in the V_{gs} at constant V_{ds} of 0.5 V for both the configuration. TFP curve shows the gradually increase with respect to the V_{gs} at constant V_{ds} of 0.5 V. As TFP is a product of transconductance generation factor and unity gain frequency as formulated in Eq. (9), which are higher for modified FE-MOSFET configuration in comparison of conventional MOSFET structure. Thus, the maximum value for TFP is shown by the FE-MOSFET device structure.

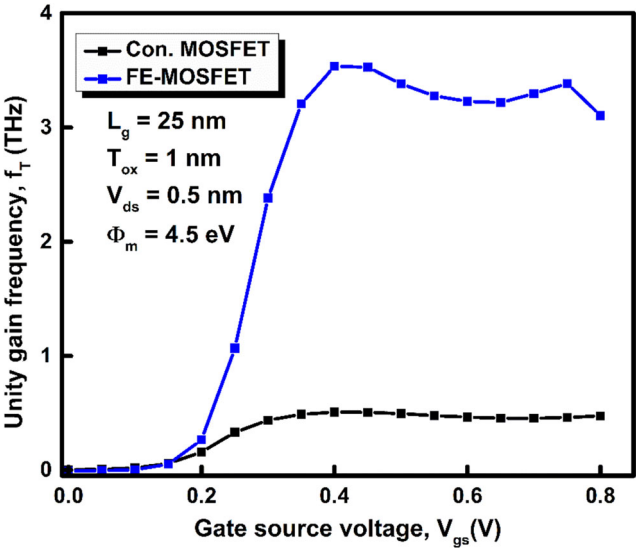

Fig. 12 Comparison of f_T variation vs. V_{gs} at constant V_{ds} = 0.5 V for conventional MOSFET and ferroelectric based substrate MOSFET (FE-MOSFET)

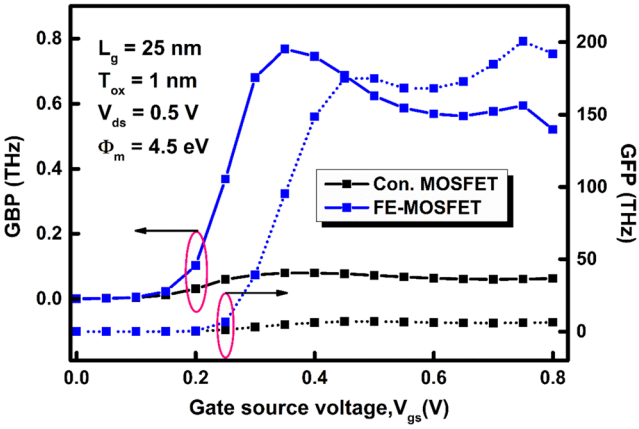

Fig. 13 The GBP and GFP for conventional MOSFET and ferroelectric based substrate MOSFET with V_{gs}

Similarly, from Eq. (10), we can see that the GTFP is dependent on the intrinsic gain and the TFP factor .So, for the high value of A_V and TFP, GTFP would be high. Consequently, we get a higher GTFP value for the FE-MOSFET configuration than the conventional one. Thus, modified FE-MOSFET is a suitable configuration in terms of gain, transconductance and speed applications. All the RF parameters are tabulated in Table 3.

5 Application of ferroelectric based substrate MOSFET

For digital applications, combinational circuits are highly demanded because of their low power consumption and high switching speed. Several designs are explored to meet the objectives. The use of ferroelectric based substrate MOSFET is an example of this effort at the device level. Here, the one brief application of FE-MOSFET is defined and presented using the COGENDA Visual TCAD simulator. And, the performance is compared with conventional MOSFET structure.

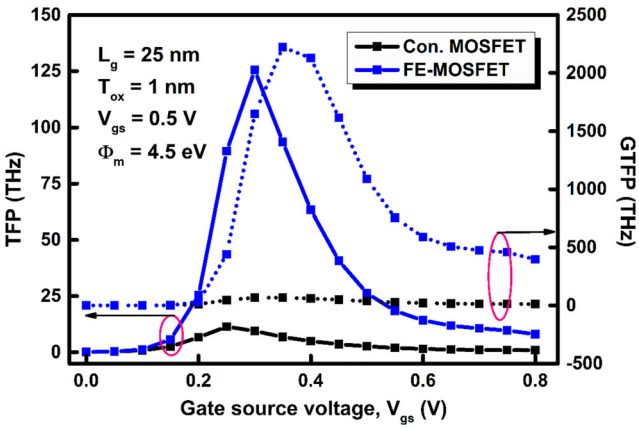

Fig. 14 Variation based comparison of TFP and GTFP with respect to V_{gs} for conventional MOSFET and ferroelectric based substrate MOSFET

Table 3 Summary of RF device performance parameters for conventional MOSFET and FE-MOSFET

Parameter	Conventional MOSFET	Modified FE-MOSFET
C_{gs}(aF/ μm)	7.342	7.507
C_{gd}(aF/ μm)	15.488	18.674
C_{gg}(aF/ μm)	22.959	27.411
f_T(THz)	0.506	4.419
GBP(THz)	0.796	7.675
GFP(PHz)	0.006	0.200
TFP(THz)	11.349	125.490
GTFP(PHz)	0.066	2.221

5.1 Inverter

For showing the application of inverter, n-channel and p-channel FE-MOSFET are designed. For electrical isolation, a spacer of 10 nm silicon oxide is used between the n-channel and p-channel FE-MOSFET. The gate contact of n-channel and p-channel FE-MOSFET are of NpolySi with a work function of 4.5 eV and 4.95 eV, respectively. For p-channel FE-MOSFET, doping material of n-type is used for substrate region and doping material of p-type is used for source and drain region with a concentration of 1×10^{17} cm^{-3} and 1×10^{20} cm^{-3} respectively. The general circuit diagram explaining the FE-MOSFET based inverter is shown in the Fig. 15.

The I_D-V_{gs} characteristics of both channel configuration devices are plotted together to match the V_{th} as shown in Fig. 16. The V_{gs} swept from -1 to 1 V at constant V_{ds} 0.5 V with dual work function metal (DWFM) integration scheme.

The voltage transfer characteristic (VTC) of the designed FE-MOSFET inverter and conventional MOSFET based inverter are displayed in Fig. 17. As from Fig. 17, it is clear that the transition range (TR) of FE-MOSFET based inverter is sharper in comparison to conventional MOSFET inverter which signifies the high speed and fast switching for a device [31].

The two important critical points on the curve where the slope of voltage transfer characteristic becomes -1 are corresponding to logic 0 and logic 1 which are denoted as maximum input voltage (V_{IL}) and minimum input voltage (V_{IH}), respectively [31]. And, the threshold voltage of the inverter configuration is the transition voltage or a voltage point at which $V_{in} = V_{out}$ on the VTC curve. In this case, the switching threshold voltage for the FE-MOSFET inverter is 0.43 V and for the conventional MOSFET based inverter is 0.42 V.

5.2 Noise margin calculation

Noise margin (NM) defines the immunity of noise for a circuit. For a better circuit performance, the noise margin should be high as possible. For low signal level (NM_L) and high signal levels (NM_H), the noise margin is tabulated as:

$$NM_L = V_{IL} - V_{OL} \tag{11}$$

$$NM_H = V_{OH} - V_{IH} \tag{12}$$

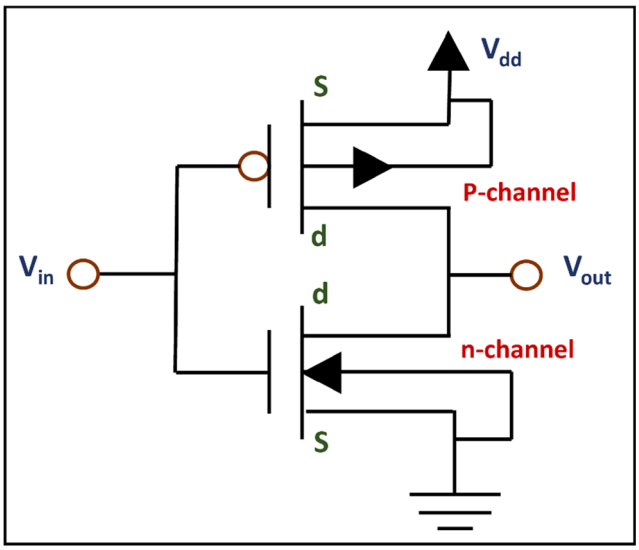

Fig. 15 Circuit diagram of FE-MOSFET based inverter

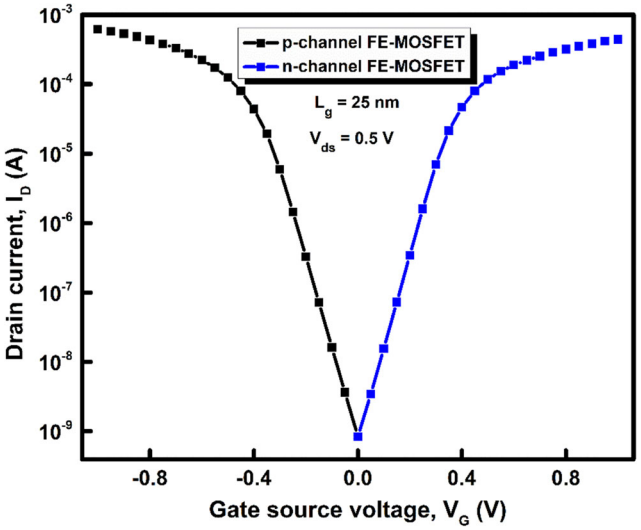

Fig. 16 Threshold voltage matching for n-channel FE-MOSFET and p-channel FE-MOSFET structure

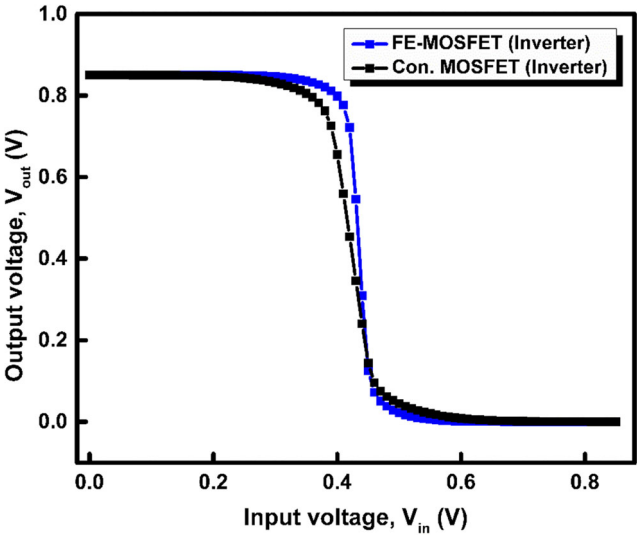

Fig. 17 Voltage Transfer Characteristics of conventional MOSFET and FE-MOSFET based inverter

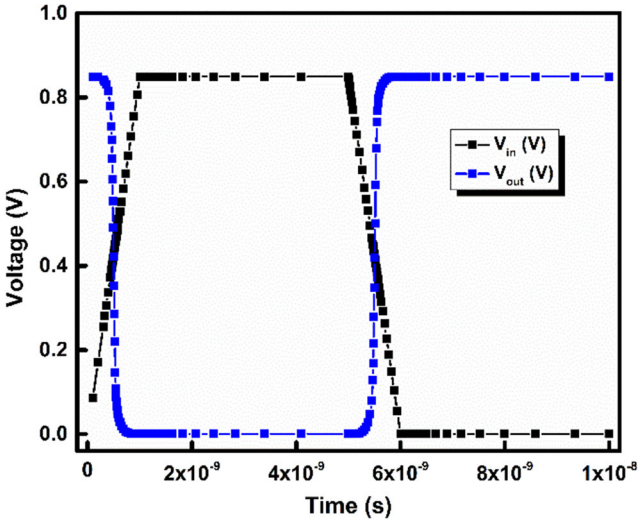

Fig. 18 Transient plot corresponding FE-MOSFET based inverter

Where, V_{OL} and V_{OH} are minimum output voltage and maximum output voltage when corresponding output levels are logic 0 and logic 1, respectively. The parameters that are required to compute the noise margin (NM) and transition region (TR) are tabulated in Table 4.

The transient analysis for FE-MOSFET based inverter is displayed in Fig. 18. All the simulation is done at room temperature (300 K) and using the drift-diffusion method solver level 1(DDML1) technique. The input pulse and V_{DD} of 0.85 V are common for both the analysis. As in inverter, the output of the inverter is at logic 1 when n-channel FE-MOSFET is in cut-off mode and it shows the logic 0 in output when the n-channel FE-MOSFET conducts.

6 Conclusions

In conclusion, the effect of ferroelectric material in the substrate region in between the high-k HfO_2 layers on the conventional MOSFET structure in terms of the analog and RF parameters using the visual TCAD simulator was investigated. The proposed architecture shows the enhanced analog and RF parameters with the reduced SCEs. Modified FE-MOSFET structure shows a better switching ratio as the off current is decreased by 97.05 % with 3.60 % increased I_{on} current. Also, the SCEs like the subthreshold swing is decreased by 16.75 % and 30.42 % in linear and saturation region, respectively. DIBL is reduced by 56.51 % and V_{th} is reduced by 20.37 % and 12.59 % in linear and saturation region, respectively. The analog parameters like g_m and TGF enhanced with 977.57 % and 67.85 %, respectively for the proposed architecture. The V_{EA} and A_V show improved results for the modified configuration with 168.81 % and 273.60 %, respectively.

Furthermore, RF performance parameters like GBP and GFP increased by 864.20 % and 3184.02 %, respectively. The TFP enhanced by 1000.69 % and GTFP gets improved by 3223.05 % for the modified structure. The unity gain frequency (f_T) is increased by 772.28 %. For the modified architecture. Furthermore, from the noise margin parameters, it is concluded that the transition range for the proposed device structure is better than the conventional MOSFET structure as NM_L and NM_H are improved with 27.09 % and 24.81 %. So, with better NM and TR, FE-MOSFET based inverter is a better option for digital applications. Thus, from the above results and discussion, the proposed device structure of FE-MOSFET can be considered as an alternate choice for designing analog and RF circuit devices.

Table 4 Comparison of noise margin for conventional MOSFET and FE-MOSFET based inverters

Parameter	Conventional MOSFET	FE-MOSFET
V_{IL} (V)	0.27	0.34
V_{IH} (V)	0.60	0.54
NM_L (mV)	261.7	332.6
NM_H (mV)	239.4	298.8
TR (V)	0.33	0.20

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Authors' Contribution All authors contributed to the study's conception and design.

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Data Availability The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Declarations

The authors have seen all the Ethical Standards and will supposed to follow them in the future.

Conflict of Interests The authors declare that they have no known conflict of interests or personal relationships that could have appeared to influence the work reported in this paper.

Consent to Participate & for Publication Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consent to the authorities for further processing.

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RESEARCH

DFT-based Atomic Calculation of Si-doped HfO_2 and Effect of its Negative Capacitance on Analog/RF, and VTC Parameters of MOSFET

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Abstract
Execution grids of developing electronic devices are being examined to find substitutes for MOSFETs in the quest to minimize power dissipation and ease energy efficiency limitations. The innovative architecture of negative capacitance field effect transistors (NCFETs), which offer advantages from the design, performance, and fabrication perspectives, is presented and examined in this article. This proposed structure in this work is called Modified NCFET. Modification of NCFET includes the Density-Functional-Theory (DFT) based atomic modelling for Ferroelectric material Hafnium Oxide ($FEHfO_2$) with different doping concentrations of silicon (Si). The performance metrics of Modified NCFET are compared with conventional MOSFET designed on the same technology node to draw the effect of Si-doped HfO_2. DFT calculations like Projected Density of States (PDOS), and energy band structure are done using the Quantum Atomistix Tool Kit (ATK) simulator which is atomic-scale modelling software, and device modelling is done by the Visual Technology-Computer-Aided-Design (TCAD) simulator. The device performance comparison of Modified NCFET and conventional MOSFET is done by the Visual TCAD in terms of short-channel effects (SCEs), analog/RF matrices, and FET-based inverter parameters (noise margin (NM), voltage transfer characteristics (VTC)). Additionally, the proposed NCFET is contrasted with the various FOMs' IRDS criteria.

Keywords DFT atomic modelling · Projected DOS · Short channel effects · Negative Capacitance · VTC · Noise margin

1 Introduction

With the dominance of high-performance, and ultra-low power circuits the IC industry started the trend to reduce the size scale of MOSFETs. But with downscaling below the 100 nm technology node, the prominent concern is the power dissipation and the SCEs. Short channel effects are brought on by the gate terminal's ineffective channel control. However, FINFET does somewhat address this worry. Scaling the supply voltage can lower the power dissipation. However, the device speed is considerably impacted by the lower supply voltage. Lowering the threshold voltage should also be necessary to maintain device speed. Low threshold voltage also causes an exponential increase in the OFF-current, which directly contributes to static power dissipation. Thus, maintaining both, i.e., device performance and power dissipation, appears to be quite difficult [1–9]. After weighing all the goals, we discovered that lowering the device's SS might be one approach to maintain both. Subthreshold swing (SS) is the applied gate voltage (V_{gs}) value that needs to change the drain current by one decade. But, SS value can be reduced to Boltzmann tranny i.e. 60 mV/decade for the conventional MOSFET or we can say that the minimum value of gate voltage is 60 mV to change the drain current (I_d) by one decade in the subthreshold region. The SS of a conventional MOSFET is given in Eq. (1.1) [6].

$$SS_{MOSFET} = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \tag{1.1}$$

The Boltzmann tranny limit is 60 mV/decade because the second term which is body factor i.e. $\left(1 + \frac{C_{dep}}{C_{ox}}\right)$ is always greater than unity. This value reduces below 1 only if the oxide capacitance becomes infinite. So, there is only one possible way to scale down it below 60 mV/decade: to make the oxide capacitance negative. The concept of

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"negative capacitance" in FETs is a relatively new and exciting development in nano-electronics. NCFETs are designed to overcome some of the fundamental limitations of traditional FETs, particularly concerning subthreshold slope (S.S.) and energy efficiency. In NCFETs, the key parameter of interest is the "equivalent oxide capacitance" (C'_{ox}) or "negative capacitance," which is a critical factor in achieving improved subthreshold performance. Here's how the equivalent oxide capacitance works in NCFETs. This objective is given by ferroelectric (FE) materials which inhibit the negative capacitance property, which means that the voltage across the FE decreases as you apply a positive voltage [2, 10]. This effect can counteract the conventional positive capacitance of the gate dielectric. The basic idea behind NCFETs is to incorporate an FE as the gate oxide instead of a conventional dielectric material (e.g., SiO_2). If we use this FE material in the gate terminal layer of conventional MOSFET, then the total oxide capacitance would be the series combination of ferroelectric material capacitance (C_{FE}) and dielectric (C_{ox}) can be expressed as

$$C'_{ox} = \frac{C_{ox}|C_{FE}|}{|C_{FE}| - C_{ox}} \tag{1.2}$$

By connecting an oxide capacitor in series, the instability of negative capacitance caused by the energy barrier can be reduced. A typical ferroelectric material exhibits polarization and hysteresis behavior in the presence of an electric field. A ferroelectric material may only provide an NC state in a specific region ($C_{FE} = 0$), and once this zone is crossed ($C_{FE} > 0$), hysteresis is visible. Figure 1 depicts the related energy-charge landscape at various places. If equivalent oxide capacitance (C'_{ox}) is negative, which is only achievable if $C_{ox} > |C_{FE}|$ according to Eq. (1.2) [6], and SS can be decreased below 60 mV per decade. Equation (1.3) [6] guarantees that with the specified condition, SS can be decreased below the Boltzmann limit. Therefore, the subthreshold swing is modified as

$$SS_{NCFET} = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{dep}}{C'_{ox}}\right) \tag{1.3}$$

The negative value of C'_{ox} is also the reason for the low V_{th} of a device that comes from the NCFET. The negative capacitance effect effectively amplifies the V_{gs}, making it easier to control the channel and achieve steeper subthreshold slopes. This enhanced control allows NCFETs to operate with sub-60 mV/decade SS, potentially breaking the fundamental SS limit of conventional FETs. In summary, the equivalent oxide capacitance (C'_{ox}) in NCFETs is not a static capacitance but rather a dynamic effect arising from the use of FE materials as gate oxides. This negative capacitance property helps overcome the subthreshold performance limitations of traditional FETs, leading to the potential for significantly improved energy efficiency and reduced subthreshold swing in digital and analog circuits.Further, the comparison graph between the conventional MOSFET and NCFET is shown and the SCEs are discussed for both the device structure. Furthermore, the analog performance parameters of conventional

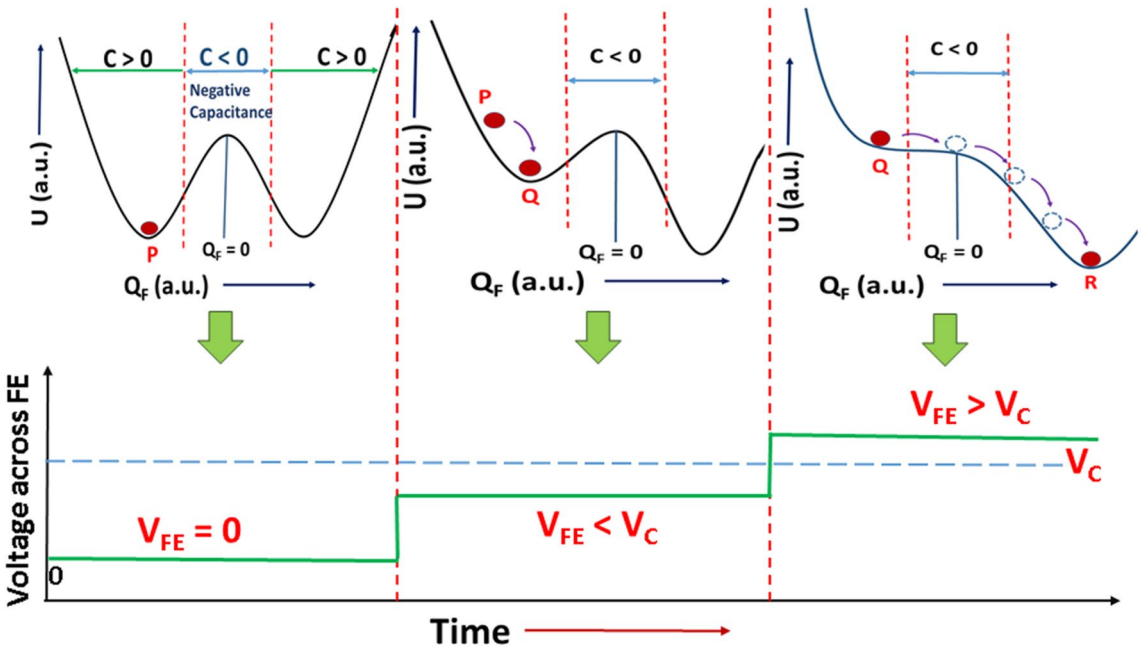


Fig. 1 Energy-charge curvature for a ferroelectric material concerning applied voltage across FE

MOSFET structure and Modified NCFET structure are discussed. An insight into the voltage-transfer curve (VTC) of both the device structure-based inverter is given in the further sections and connection parameters are discussed below.

2 Basic of NCFET

The basic difference between the MOSFET and NCFET is the addition of an FE layer in the gate terminal layer. The property of NC in the FE can be explained by the L.K. equation which is given in terms of charge and voltage in Eq. (2.1) [6].

$$V_F = \alpha Q_F + \beta Q_F^3 + \gamma Q_F^5 \tag{2.1}$$

where Q_F and V_F are the corresponding charge and voltage across the FE in the gate stack. And the constants α, β, and γ are the anisotropy constants for an FE material. Energy-charge curvature of the ferroelectric material showing the negative capacitance phenomenon is drawn in Fig. 1. We begin by pointing out that, by definition, capacitance is a small-signal notion. For example, capacitance C at a given charge Q_{FE} is related to the potential energy U by the formula, $C = \left[d^2U/dQ_{FE}^2\right]^{-1}$. Due to this, we will henceforth refer to "negative differential capacitance" as "negative capacitance." As seen in Fig. 1, the capacitance of a ferroelectric material is exclusively negative in the barrier region surrounding $Q_{FE} = 0$. The energy landscape is tilted as a voltage is placed across the ferroelectric capacitor starting from an initial state P, and the polarization moves to the closest local minimum. This transition at a voltage that is lower than the coercive voltage (V_C). Notably, as the polarization state descends when $V_{FE} > V_C$, it passes through the region where,$C = \left[d^2U/dQ_{FE}^2\right]^{-1} < 0$, i.e., a ferroelectric material switches from one stable polarization to the other while passing through a zone where the differential capacitance is negative. One of the minima vanishes if the voltage exceeds V_C, and Q_{FE} shifts to the remaining minimum of the energy landscape. In the simulated structure, undoped HfO_2 which is a high-k dielectric material (k = 25) when covered with chemical vapor deposition works as the FE material. The model is modified by replacing the existing anisotropy constants with the anisotropy of undoped HfO_2 which are extracted from the expression related to the coercive field (E_C) and remanent polarization (P_r) given in Eq. (2.1a) [6]. The value of E_C and P_r for undoped HfO_2 is taken as 1000 kV/cm and 10 μC/cm2, respectively.

$$\alpha = \frac{-3\sqrt{3}}{2}\frac{V_c}{Q_O} \text{ and } \beta = \frac{3\sqrt{3}}{2}\frac{V_c}{Q_O^3} \tag{2.1a}$$

where, V_C and Q_O are the coercive voltage and remanent polarization charges, respectively in the ferroelectric material. In steady-state conditions, the internal voltage can be expressed as in Eqs. (2.2a), (2.2b), and (2.2c) [6].

$$V_{MOS} = \frac{V_{gs}}{1 - \frac{C_{MOS}}{|C_F|}} + \frac{V_{ds}}{\frac{|C_F| - C_{MOS}}{-C_D}} \tag{2.2a}$$

$$V_{MOS} = A_G \times V_{gs} + A_D \times V_{ds} \tag{2.2b}$$

$$A_G = \frac{|C_F|}{|C_F| - C_{MOS}}; A_D = \frac{-C_D}{|C_F| - C_{MOS}} \tag{2.2c}$$

A_D stands for the drain coupling factor and A_G stands for the amplification factor in the NCFET. V_{MOS} is the internal node voltage and V_{gs}, and V_{ds} are the gate and drain voltages, respectively. C_{MOS} is the total gate capacitance which is the sum of the gate-to-source capacitance (C_S) and gate-to-drain capacitance (C_D). The higher amplification occurs if the difference in the values of C_F and C_{MOS} is negligible [11–14]. That is not possible in the case of MOSFET as discussed in Section 1.

3 Device Architecture and Simulation Methodology

3.1 DFT-based Atomic Calculation of Hafnium Oxide

HfO_2 is a high-k dielectric (k = 25) material with a high bandgap, but when the Hafnium (Hf) atom is replaced with the silicon atom by chemical vapor decomposition, it revises its electrical properties. Some of these properties are studied by DFT-based calculation of silicon-doped hafnium oxide using the quantum ATK simulator. In this work, the authors studied the behavior of HfO_2 with 1 Silicon atom doping and with 2 silicon atom doping in terms of its band structure, and projected density of states. A simple cubic structure of HfO_2 is taken for calculation and doping of silicon atom is done by replacing one and two hafnium atoms in SC-HfO_2 as shown in Fig. 2 and the band structure of these three configurations that is undoped HfO_2, HfO_2 doped with 1 Si-atom, and HfO_2 doped with 2 Si-atom is explained in same Fig. 2. From Fig. 2, it is clear that replacing the Hf-atom with Si-atom reduces the bandgap between the conduction band and valence band which is definitely one of the reasons for using the hafnium oxide as ferroelectric. The bandgap for HfO_2 is 2.8090 eV, HfO_2 with 1 Si-atom doping is 1.7587 eV and

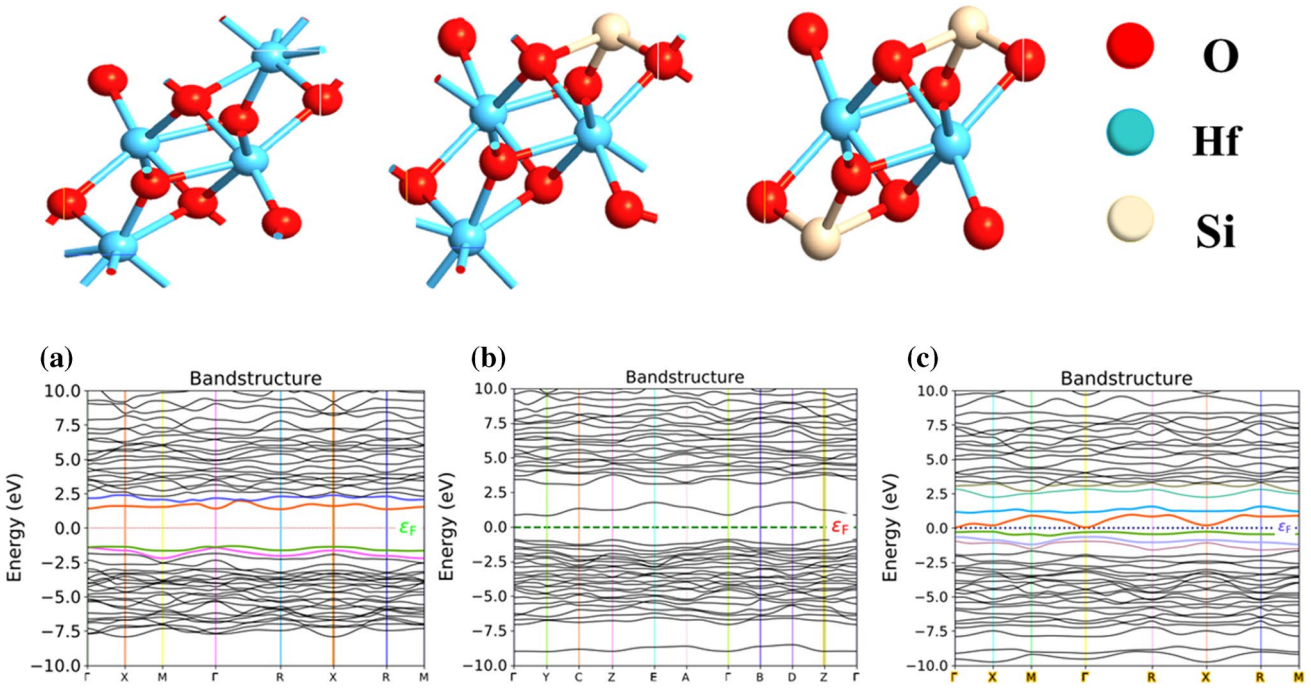


Fig. 2 The band structure corresponds to HfO_2 (**a**) 1 Si-atom doped HfO_2 (**b**) 2 Si-atom doped HfO_2 (**c**)

reduced to 0.3475 eV when 2 Si-atom is replaced with Hf atom.

3.2 Device Architecture and "atom-to-device" Synopsis

Here in this part of the work, the behavior of conventional MOSFET (t_{FE}=0 nm) and a new architecture of NCFET (t_{FE}=0.5 nm) have been compared. In the newly discussed architecture of NCFET, we used a high-k dielectric material layer in the substrate region. All the device dimensions of both devices are the same, like the channel length (L_g) of 25 nm, and extensions of source/drain on both sides of the channel region are taken at 10 nm. The oxide thickness (EOT) in the gate stack is fixed at 1 nm. The substrate region is doped with a uniform p-type of 1×10^{17} cm^{-3} concentration. And source/drain region is heavily n-type doped with 1×10^{20} cm^{-3} concentration and is of Gaussian type. All the device dimensions are tabulated in Table 1 and Fig. 3 shows the architecture of both the device structure.

For the simulation of any semiconductor device, the drift–diffusion (DD) model is widely used and this DD model can be achieved by assuming the various approximations extracted from the hydrodynamic model such as the speed of light is much faster than the speed of charge carriers, collisions are assumed to be elastic collisions and during collisions, band-gap does not change, degeneration of carriers can be neglected, etc. other more improvements have been done in this DD model which makes it complex but allows it to deal with the real problems.

Table 1 For the Visual TCAD simulation, the device dimension and parameters of modified NCFET and traditional MOSFET structures are used

Parameter	Conventional MOSFET	Modified NCFET
L_g (nm)	25	25
$L_{S/D}$ (nm)	10	10
T_{ox} (nm)	1	1
T_{FE} (nm)	0	2.5
$T_{high\text{-}K}$ (nm)	0	20
$N_{S/D}$ (cm^{-3})	1×10^{20}	1×10^{20}
N_{ch} (cm^{-3})	1×10^{17}	1×10^{17}
Φ_m (eV)	4.5(Npoly Si)	4.5 (Npoly Si)

The synopsis for atom to device modelling is explained in Fig. 4(a). The flowchart of the simulation methodology is shown in Fig. 4(b). Visual TCAD device simulator uses the level 1 drift–diffusion model (DDML1) with constant lattice temperature to solve any procedure. The primary function of DDML1 is to solve the basic electron and hole continuity equations along with Poisson's equations:

$$\nabla.\varepsilon\nabla\Psi = -q(p - n + N_D^+ - N_A^-) \tag{3.1}$$

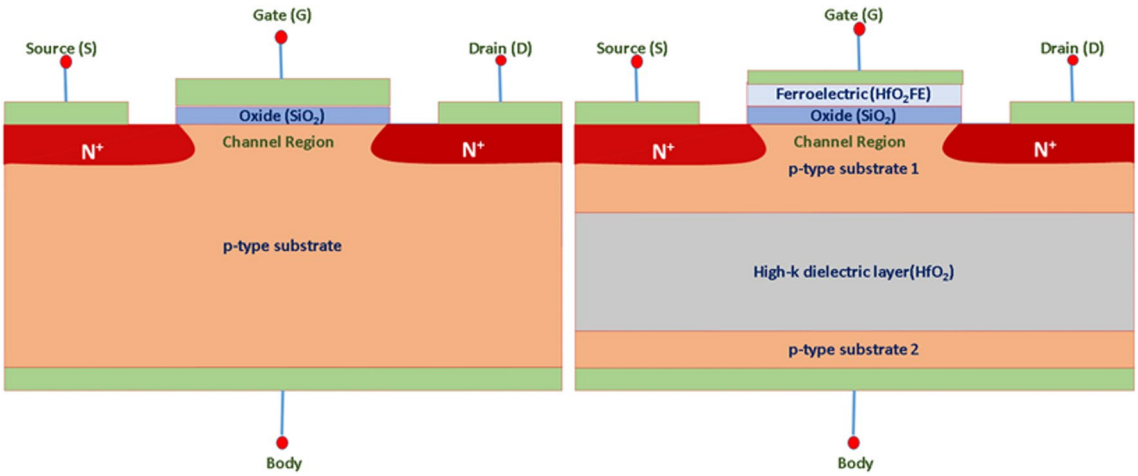


Fig. 3 The schematic architecture of conventional MOSFET and Modified NCFET

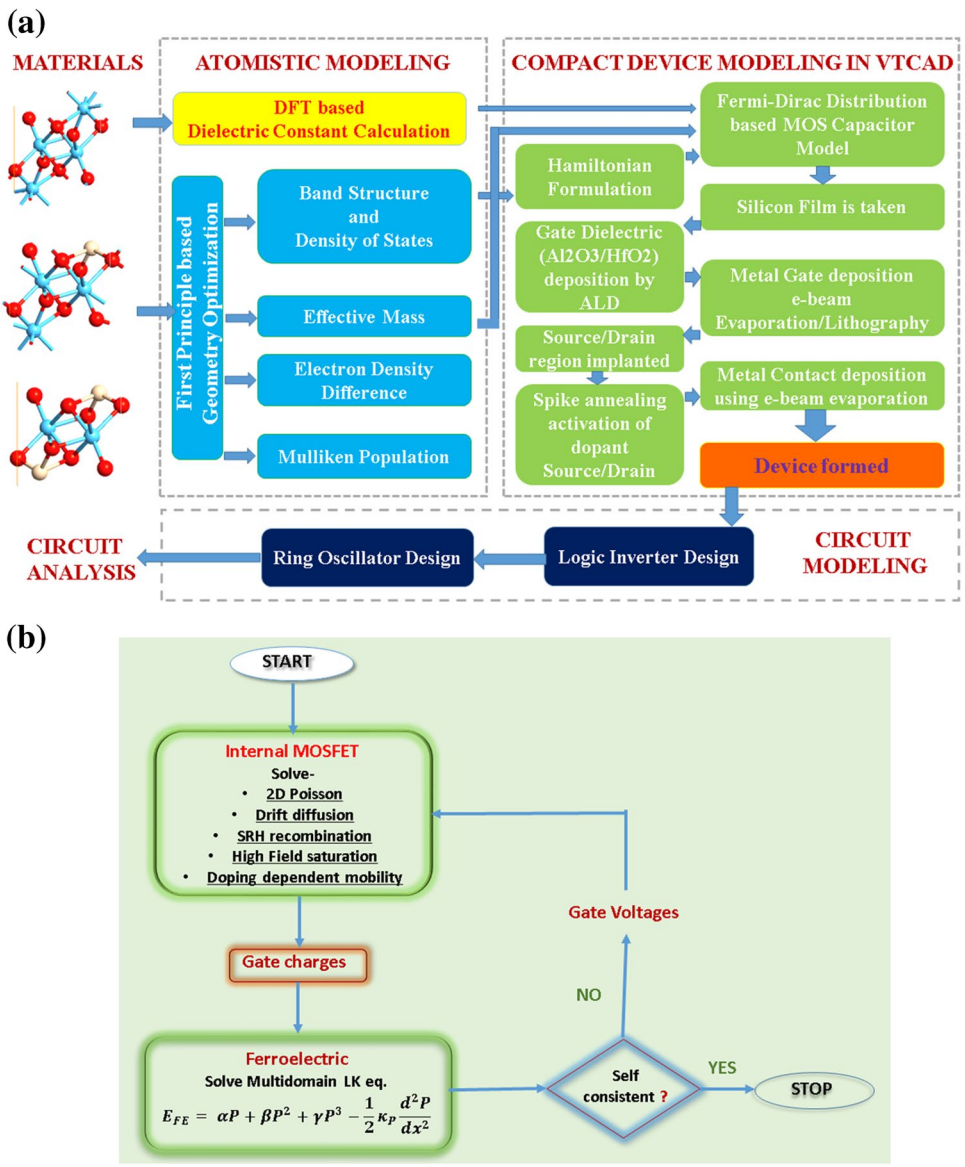


Fig. 4 (**a**) Synopsis of "Atom-to-Circuit" Modelling for Modified NCFET structure. (**b**) Flowchart for the simulation methodology in COGENDA Visual TCAD

where Ψ is the electrostatic potential of vacuum level, the concentration of electron and hole is noted by n and p, respectively, $N_D^+ and N_A^-$ defines the ionized impurity concentrations and q is the electron charge magnitude.

If χ defines the electron affinity, ΔE_c and ΔE_v notes the shift in bandgap due to mechanical strain or heavy doping, and the bandgap of the semiconductor is denoted by E_g then, the relation of vacuum level Ψ with the conduction level E_c and valence level E_v is given as

$$E_C = -q\Psi - \chi - \Delta E_C \tag{3.2a}$$

$$E_v = E_c - E_g + \Delta E_v \tag{3.2b}$$

Further, the intrinsic fermi potential $\Psi_{intrinsic}$ and vacuum level Ψ are connected by the relation given as

$$\Psi = \Psi_{intrinsic} - \frac{\chi}{q} - \frac{E_g}{2q} - \frac{k_b T}{2q} ln\left(\frac{N_c}{N_v}\right) \tag{3.3}$$

In the Genius code, the energy reference 0 eV is taken as the intrinsic Fermi level of the equilibrium state.

Continuity equations for electrons and holes are defined as if U is the recombination rate and G is the generation rate for both electrons and holes.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . J_n - (U - G) \tag{3.4a}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . J_p - (U - G) \tag{3.4b}$$

where J_n and J_p are vector quantities and defined as the electron and hole current densities respectively and expressed as

$$J_n = q\mu_n n E_n + qD_n \nabla n \tag{3.5a}$$

$$J_p = q\mu_p p E_p + qD_p \nabla p \tag{3.5b}$$

where μ_n and μ_p are mobilities of electrons and holes respectively. $D_n\left(=\frac{k_b T}{q}\mu_n\right)$ and $D_p\left(=\frac{k_b T}{q}\mu_p\right)$ are the diffusion constants for electron and hole, respectively. E_n and E_p are the effective driving electrical field for electrons and holes and are vector quantities given as

$$E_n = \frac{1}{q}\nabla E_c - \frac{k_b T}{q}\nabla(\ln(N_c) - \ln\left(T^{3}/2\right)) \tag{3.6a}$$

$$E_p = \frac{1}{q}\nabla E_v + \frac{k_b T}{q}\nabla(\ln(N_v) - \ln\left(T^{3}/2\right)) \tag{3.6b}$$

By using the given values in the above expressions and combining these with Poisson's equations, we obtained the basic equations for DDML1 as follows:

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n E_n + \mu_n \frac{k_b T}{q}\nabla n) - (U - G) \tag{3.7a}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_p p E_p - \mu_p \frac{k_b T}{q}\nabla p) - (U - G) \tag{3.7b}$$

$$\nabla.\varepsilon\nabla\Psi = -q(p - n + N_D^+ - N_A^-) \tag{3.7c}$$

Equations from Eqs. (3.1) to (3.7c) are referred to from the Visual TCAD simulator manual [15].

Figure 4(a) despite the atom-to-circuit modeling for Modified NCFET structure that can be explained with its parameters as.

(a) **Atomistic Modelling**
(b) **DFT-based dielectric constant calculation:** Calculating the dielectric constant (also known as the permittivity) of a material using Density Functional Theory (DFT) is a common theoretical approach in condensed matter physics and materials science. The dielectric constant characterizes a material's ability to store electrical energy in an electric field. DFT can provide valuable insights into the electronic structure and properties of materials, including their dielectric response. DFT calculations can be computationally intensive, and the accuracy of the results depends on various factors, including the choice of exchange–correlation functional, the level of theory, and the convergence criteria.
(c) **First principle-based geometry optimization:** Geometry optimization in Density Functional Theory (DFT) is a fundamental computational technique used to find the most stable atomic positions and lattice parameters for a given material. It's based on the principles of quantum mechanics and aims to minimize the total energy of the system by adjusting the positions of the atoms within the constraints of the chosen DFT method and exchange–correlation functional. Performing a first-principles-based geometry optimization in DFT allows you to obtain accurate structural information for a wide range of materials, enabling you to understand their stability, bonding, and other physical properties from a quantum mechanical perspective.
(d) **Compact device modelling in Visual TCAD**
(e) **Fermi–Dirac distribution-based MOS capacitor model**: FD distribution plays a key role in MOS capacitor modelling by describing the electron energy distribution and determining important parameters such as the flat band voltage and threshold voltage.

These parameters are essential for understanding the operation of MOS devices and designing integrated circuits. The Fermi–Dirac distribution helps model the electron occupancy in energy states within the semiconductor, which in turn affects the device's behaviour and characteristics.

(f) **Substrate Preparation**: Prepare a semiconductor substrate, which is typically a thin wafer of the chosen material. The substrate may be lightly doped or undoped, depending on the type of FET you want to create (e.g., n-channel or p-channel).

(g) **Thin Film Deposition:** Deposit thin films of various materials on the substrate using techniques like chemical vapour deposition (CVD), physical vapour deposition (PVD), or molecular beam epitaxy (MBE). These films are used to create different layers within the FET, including the gate, source, and drain regions.

(h) **Photolithography**: Use photolithography to define the patterns for various FET components. Photomasks are created to define the positions of the gate, source, and drain regions.

(i) **Etching**: Use chemical or plasma etching to remove material in areas not protected by the photoresist. This creates trenches and openings in the thin films, defining the gate, source, and drain regions.

(j) **Doping**: Introduce dopants (impurities) into the semiconductor material to create regions with the desired electrical characteristics. This process is essential for forming the source and drain regions.

(k) **Gate Insulator Formation**: Deposit or grow a thin insulating layer (typically silicon dioxide, SiO2) on top of the semiconductor. This insulating layer will serve as the gate dielectric.

(l) **Gate Electrode Formation**: Deposit a metal (e.g., aluminum or tungsten) or a highly doped semiconductor layer on top of the gate insulator to form the gate electrode.

(m) **Source and Drain Contacts**: Deposit metal layers on top of the source and drain regions to form electrical contacts.

(n) **Annealing**: Subject the device to an annealing process to activate dopants, repair crystal damage, and improve electrical characteristics.

(o) **Circuit Modelling**

Modeling a Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) in a circuit involves representing the device's electrical behaviour using equivalent circuit elements. The MOSFET is a three-terminal semiconductor device commonly used in integrated circuits for amplification, switching, and other functions. There are different levels of complexity for MOSFET models, ranging from simple to highly detailed.

4 Performance Analysis of NCFET Over MOSFET

4.1 Projected DOS for Different HfO_2 Configuration

Further, Fig. 5 shows the projected DOS for all three configurations. Projected DOS corresponds to every spin up and spin down configuration which shows the chances of electrons to transfer from VB to CB so that the polarization and charge transfer increases. The highest projected DOS is for the HfO_2 doped with 2 Si-atom. PDOS (Projected Density of States) gives the projection of a particular orbital of a particular atom on the density of states. So, if you sum over all the projections, you will have the total density of state, or simply, the DOS. PDOS is related to how the energy states are distributed. Due to the voltage amplification factor in the NCFET structure that is provided by the FE material layer in the gate stack. As we apply the gate-source voltage to turn on the device, there are screening charges (σ) and polarization charges (P). They arrange themselves according to the applied voltage. The time in which screening charges arrange themselves (T) is much less than the polarization switching time (T_P), hence the total net voltage drop across the ferroelectric material is negative which results in the voltage amplification in NCFET shown in Fig. 6. Figure 7 shows the transfer characteristic of conventional MOSFET and the Modified NCFET structure in linear and logarithmic scales. The linear curves show the high ON-current for the Modified structure of NCFET due to its negative capacitance phenomenon when compared to the conventional MOSFET. In the logarithmic scale, we can see that the OFF-current or leakage current is almost comparable for both devices which means the switching ratio (I_{ON}/I_{OFF}) becomes high for the Modified NCFET structure.

4.2 Voltage Amplification and SCEs in Modified NCFET over MOSFET

In addition, SCEs like DIBL, SS, and V_{th} become dominant when the technology nodes become shorter than 100 nm. In such a short node, the channel current starts controlled by the drain terminal instead of the gate terminal. So, for the device's performance at such a short channel length we need to suppress these effects [16–18].

Firstly, let's talk about the threshold voltage which is the needed voltage to turn on the device, and here for the work, it's less for the Modified NCFET structure in comparison to the conventional MOSFET structure shown in Fig. 8(a). Further, another SCE is DIBL which is responsible for the reduction of threshold voltage and higher leakage current at higher drain bias. When the biasing increases at the drain end, it starts interacting with the channel region and

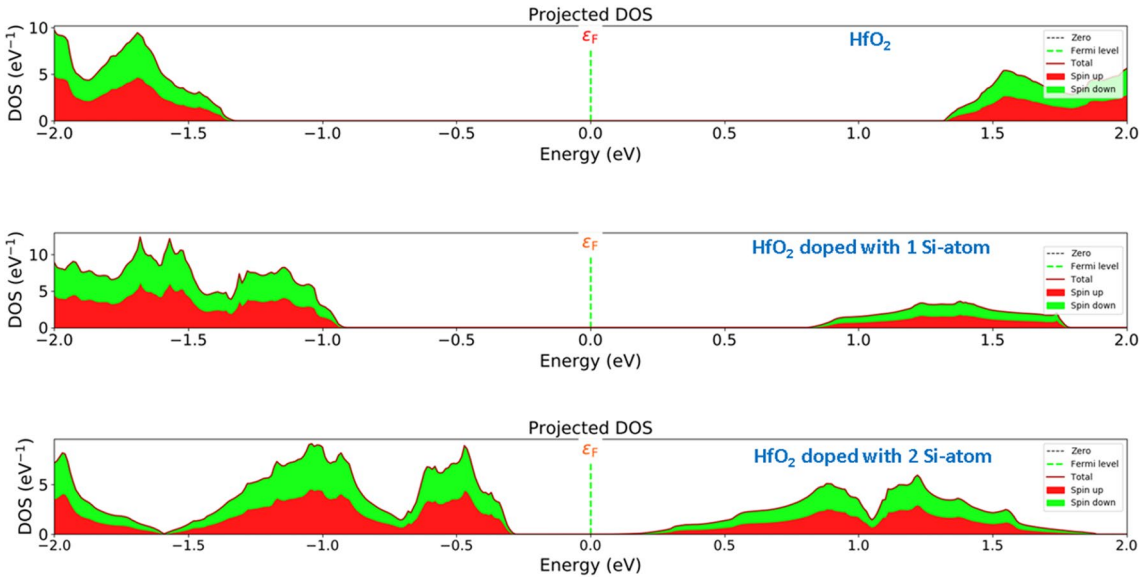


Fig. 5 The Projected DOS concerning the energy for different configurations of HfO_2

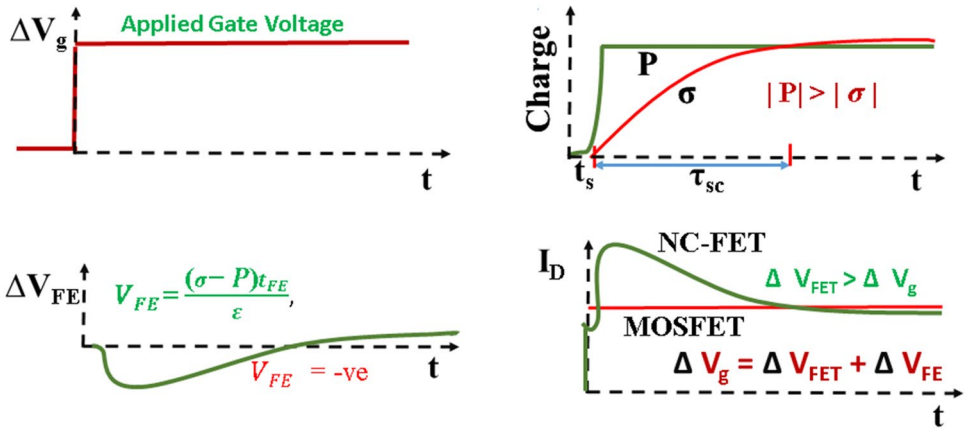


Fig. 6 The voltage amplification process occurs in the gate stack of NCFET

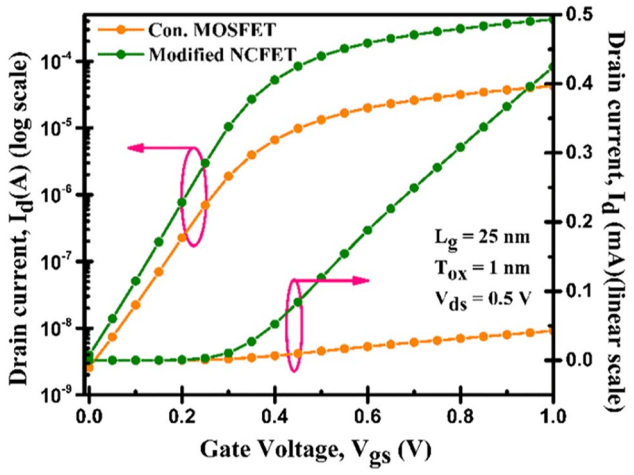


Fig. 7 Transfer characteristic comparison of conventional MOSFET and Modified NCFET

the source end which results in lower barrier potential and gives the electrons an easy path to travel through the channel. Hence, the gate terminal loses the control over channel current. So, this effect should be decreased for better device performance. In Fig. 8(b), the calculated DIBL data is according to Eq. (4.1) [4, 17].

$$DIBL = \frac{V_{th_{V_{ds}=0.9V}} - V_{th_{V_{ds}=0.1V}}}{V_{ds=0.9V} - V_{ds=0.1V}} \tag{4.1}$$

The conventional MOSFET and Modified NCFET structure are shown which shows the lower DIBL value for Modified NCFET over conventional MOSFET. Furthermore, the critical SCE is the subthreshold swing value which is discussed in the introduction section. In this study, we discussed the SS value in the linear and saturation region according to Eq. (1.3).

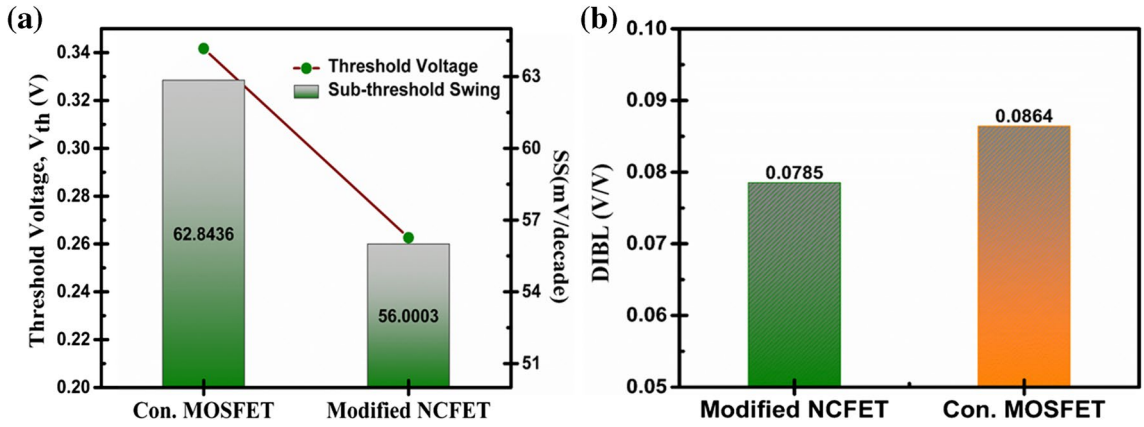


Fig. 8 (**a**) Comparison of V_{th} and SS for conventional MOSFET and Modified NCFET. (**b**) DIBL comparison of conventional MOSFET and Modified NCFET

Table 2 Comparison of SCEs in conventional MOSFET and Modified NCFET

Short channel effects	Conventional MOSFET	Modified NCFET
V_{th} (V)	0.34	0.26
DIBL (mV/V)	0.086	0.078
SS_{lin} (mV/dec)	62.84	56.00

And in both regions, we found that the SS value approaches the Boltzmann tranny limit which is 60 mV/dec [17–19]. In the linear region, the SS value of Modified NCFET is reduced by 8.92% when compared with the conventional MOSFET plotted in Fig. 8(a). All the extracted values of SCEs are inserted in Table 2.

4.3 Analog/RF Parameter Comparison of MOSFET and Modified NCFET

At $V_{ds} = 0.5$ V and $V_{gs} = 0.5$ V, Fig. 9(a) shows the net charge across the channel of Modified NCFET. The high intensity of charges is at the source and drain ends. Figure 9(b) shows the potential across the channel region of Modified NCFET at the same conditions and it indicates that the highest potential is at the channel region in comparison to the source/drain end. Figure 9(c) shows the electron and hole mobility variation with the cutline starting from the source end and going to the drain end. Lastly, Fig. 9(d) shows the Electrical field generated across the channel region from the source end to the drain end at $V_{ds} = 0.5$ V and $V_{gs} = 0.5$ V. Analog parameters and inverter applications are explored in this section of the study to compare the performance of Modified NCFET and traditional MOSFET. The results are simultaneously compared. Figure 7 makes it clear that the Modified NCFET has a higher drain current than the conventional MOSFET device because of the negative capacitance phenomenon in NCFET.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{4.2}$$

$$\mathrm{TGF} = \frac{g_m}{I_d} \tag{4.3}$$

Related to drain current, transconductance defines the input conductance which is an essential parameter for the high-performance application. From Fig. 10(a), it is clear that the g_m calculated according to Eq. (4.2) [4, 12] for the Modified NCFET is higher than the conventional MOSFET as the ON-current for the Modified NCFET is somewhat higher than the conventional MOSFET [20–23]. Also, the "transconductance generation factor is the ratio of gain generated per unit power loss". A high value of TGF calculated from Eq. (4.3) [4, 17] indicates a high gain with less power loss which is a valuable factor for reliable application. The modified NCFET's TGF value is higher than that of the traditional MOSFET which shows the better device application as expressed in Fig. 10(a).

On the other hand, the switching ratio (I_{ON}/I_{OFF}) also increases by one decimal point in the Modified NCFET (1.07×10^5) when compared to the conventional MOSFET (1.64×10^4). Also, it is further improved by the use of high-k dielectric material in the substrate region. Further, there is one more essential parameter that gives the device functioning in terms of current and SS called quality factor (QF). QF can be expressed as in Eq. (4.4) [4].

$$\mathrm{QF} = \frac{g_m}{SS} \tag{4.4}$$

For Modified NCFET, QF is 5.3 μS-dec/mV and for conventional MOSFET its value is 4.8 μS-dec/mV which is

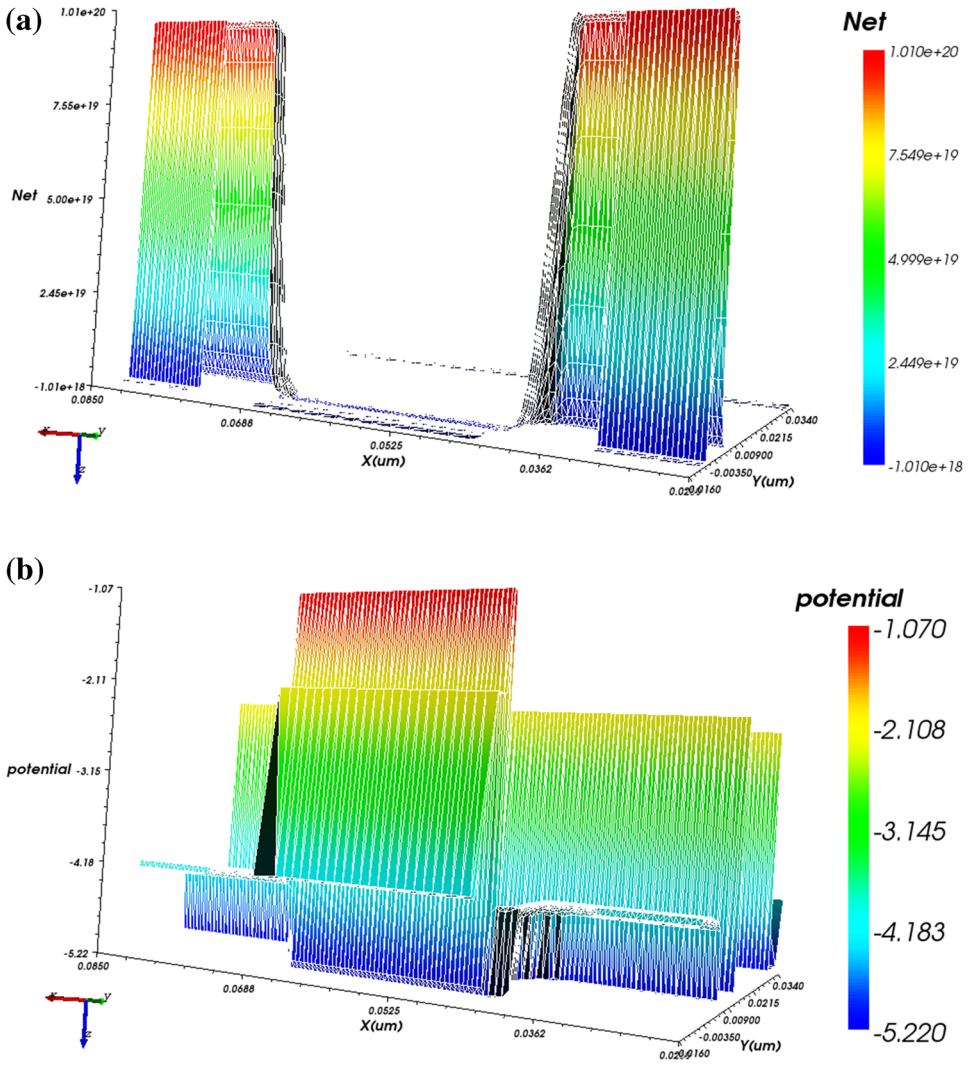


Fig. 9 (**a**) Net charge across the Modified NCFET device. (**b**) The potential across the channel region in Modified NCFET structure. (**c**) Electron and hole mobility across the channel region of Modified NCFET structure. (**d**) The electrical field across the channel region of the Modified NCFET structure

significantly better as shown in Fig. 10(b). It is because of higher g_m in the case of Modified NCFET.

Furthermore, another parameter that connects g_m and I_d is device efficiency which is higher for the Modified NCFET (58.33 V^{-1}) than the conventional MOSFET (44.07 V^{-1}) expressed in Fig. 10(c).

$$g_d = \frac{\partial I_{dsat}}{\partial V_{ds}} \tag{4.5}$$

$$V_{EA} = \frac{I_d}{g_d} \tag{4.6}$$

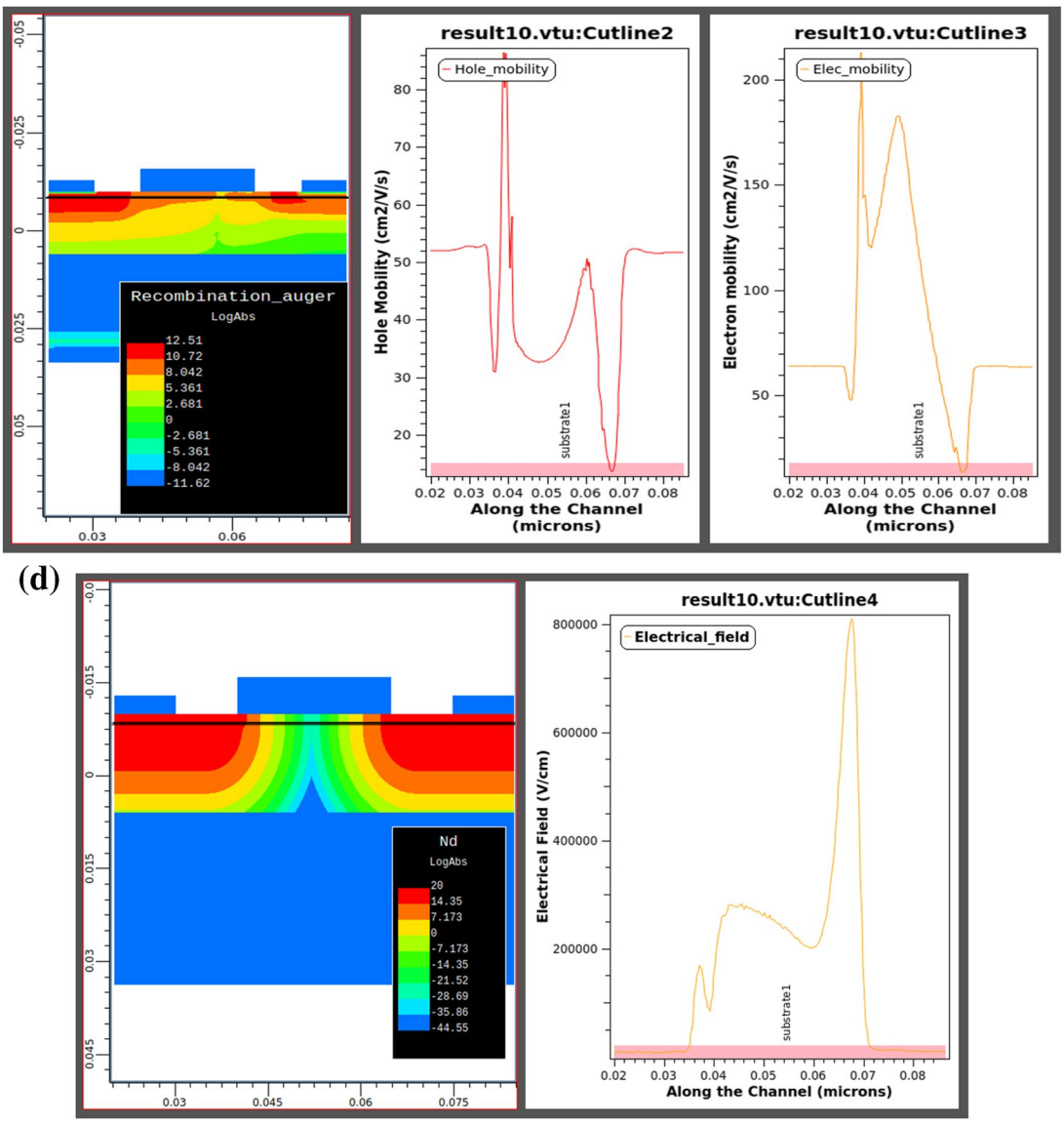
Moving to Fig. 10(d), the variation of output conductance (g_d) according to Eq. (4.5) [4] and early voltage (V_{EA}) according to Eq. (4.6) [4] as a function of V_{ds} is shown at $V_{gs} = 0.5$ V. g_d and V_{EA} should be as high as possible for the gadget to have higher analog performance. Because g_d measures the current driving ability of a device and V_{EA} is the source-drain resistance measurement. In this comparison work, we get these values high for the Modified NCFET structure. Further, we have the variation of cut-off frequency (f_T) with the V_{gs} at constant $V_{ds} = 0.5$ V in Fig. 10(e), f_T depends on the transconductance (g_m), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) as formulated below in Eq. (4.7) [3].

$$f_T = \frac{g_m}{2\pi\left[C_{gs} + C_{gd}\right]} \tag{4.7}$$

$$f_{max} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{4.8}$$

as the g_m is high for the Modified NCFET when compared to the conventional MOSFET, we get the f_T high for the Modified NCFET according to Eq. (4.7). Moreover, for the better performance of a device, the intrinsic gain (A_V) should be

Fig. 9 (continued)

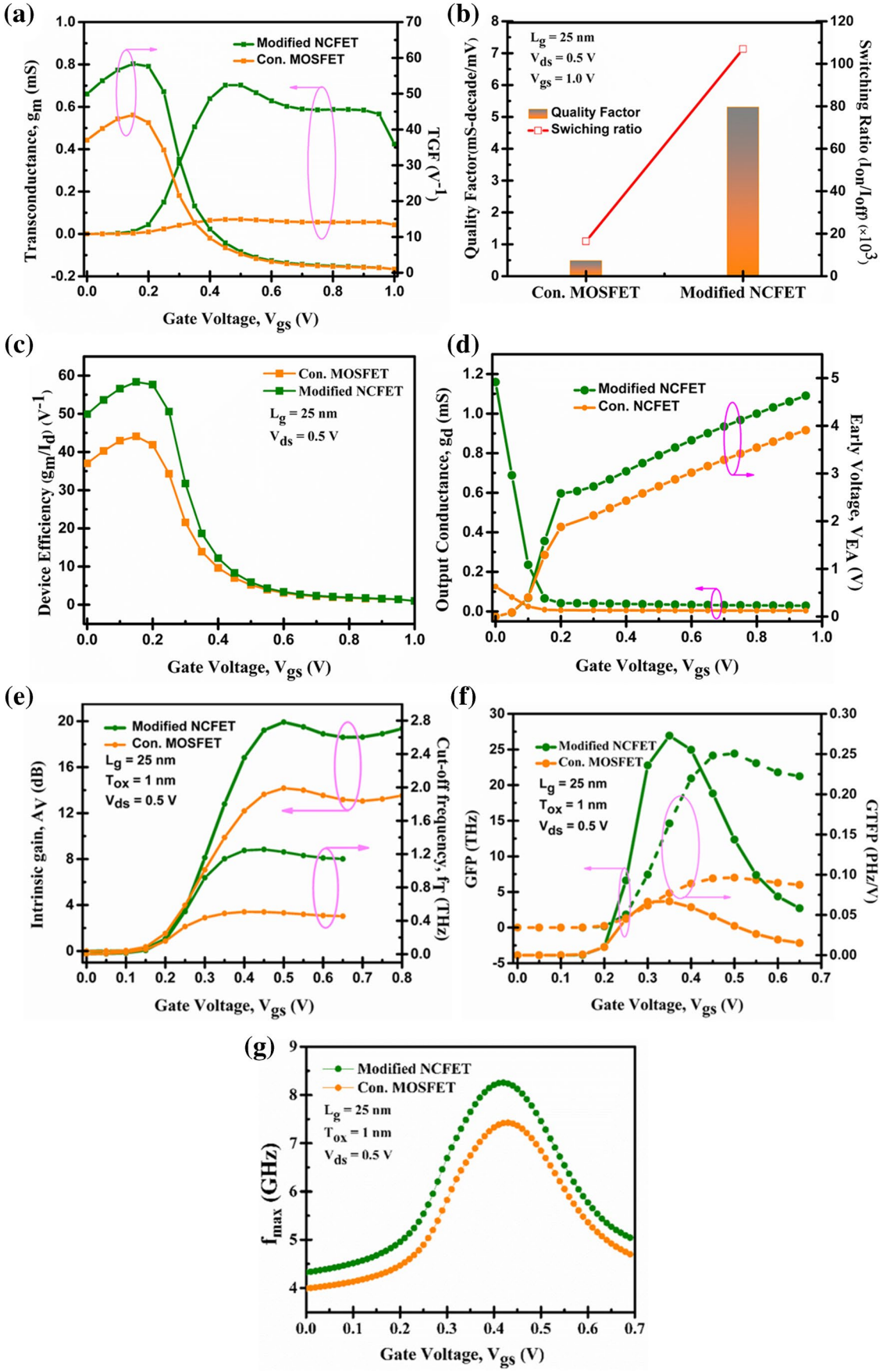


high [24, 25]. No matter what the bias point, A_V is a device's possible maximum voltage gain. The variation of A_V for both the device structures is shown in Fig. 10(e) and it is clear that A_V for Modified NCFET is higher than conventional MOSFET. Figure 10(f) shows the GFP and GTFP for the conventional MOSFET and Modified NCFET verifying that negative capacitance gives a better improvement to the device's performance. Figure 10(g) despite the Maximum frequency for oscillation f_{max} for conventional MOSFET and Modified NCFET. It is higher for Modified NCFET in comparison to con. MOSFET as the overall combination of g_{ds}, f_T, and C_{gd} is low for the previous device in comparison to the conventional device [25].

All these performance parameters are tabulated in Table 3.

5 Comparison of Conventional MOSFET-Based Inverter and Modified NCFET-based Inverter

Combinational circuits are in high demand nowadays because of their high switching speed and their low power consumption. For better digital applications, combinational circuits are the first choice. To meet the objectives, several designs of MOSFETs are explored and the Modified NCFET is one of them. In this section of work, we discuss the voltage-transfer curve of a conventional MOSFET-based inverter and a Modified NCEFT-based inverter. Firstly, Fig. 11(a) shows the schematic structure of a MOSFET-based inverter. So, in this architecture, we need two types of components. One is the n-channel component and the other is the p-channel component, both are connected with the


(a)
Modified NCFET
Con. MOSFET
Transconductance, g_m (mS)
TGF (V^{-1})
Gate Voltage, V_{gs} (V)
(b)
L_g = 25 nm
V_{ds} = 0.5 V
V_{gs} = 1.0 V
Quality Factor
Swiching ratio
Quality Factor(mS-decade/mV)
Switching Ratio (I_{on}/I_{off}) ($\times 10^3$)
Con. MOSFET
Modified NCFET
(c)
Con. MOSFET
Modified NCFET
L_g = 25 nm
V_{ds} = 0.5 V
Device Efficiency (g_m/I_d) (V^{-1})
Gate Voltage, V_{gs} (V)
(d)
Modified NCFET
Con. NCFET
Output Conductance, g_d (mS)
Early Voltage, V_{EA} (V)
Gate Voltage, V_{gs} (V)
(e)
Modified NCFET
Con. MOSFET
L_g = 25 nm
T_{ox} = 1 nm
V_{ds} = 0.5 V
Intrinsic gain, Av (dB)
Cut-off frequency, f_T (THz)
Gate Voltage, V_{gs} (V)
(f)
Modified NCFET
Con. MOSFET
L_g = 25 nm
T_{ox} = 1 nm
V_{ds} = 0.5 V
GFP (THz)
GTFP (PHz/V)
Gate Voltage, V_{gs} (V)
(g)
Modified NCFET
Con. MOSFET
L_g = 25 nm
T_{ox} = 1 nm
V_{ds} = 0.5 V
f_{max} (GHz)
Gate Voltage, V_{gs} (V)

◂**Fig. 10** (**a**) The g_m and TGF variation (**b**) QF and switching ratio for conventional MOSFET and Modified NCFET. (**c**) Variation of device efficiency (**d**) Variation of g_d and V_{EA} for conventional MOSFET and Modified NCFET. (**e**) Variation of the cut-off frequency and intrinsic gain (A_V) to V_{gs}. (**f**) GFP and GTFP to V_{gs} (**g**) f_{max} to V_{gs} for both the architecture

10 nm SiO_2 spacer. To work as the circuit of the inverter, the components of this structure should be such that their threshold voltage is the same so that there is no break point in the working of the circuit when we change the applied voltage from -1 V to + 1 V. As regular CMOS based inverter circuit, $V_{gs} = 0$ V is the breakpoint for the circuit where the working component changes.

When $V_{gs} =$ -1 to 0 V, at that particular time, p-channel Modified NCFET works and gives the output, and when $V_{gs} = 0$ to + 1 V, then the working component is n-channel Modified NCFET. So, the threshold voltage for both components should be the same so that the complete circuit works smoothly. For matching the V_{th}, we should change the work functions of both gate contacts (NpolySi) simultaneously. NpolySi is used as the gate contact with 4.50 eV and 4.95 eV work functions for n-type and p-type channel components respectively. The plot for the threshold match is shown in Fig. 11(b). This architecture is presented using the COGENDA Visual TCAD simulator We simulated the results for both compared device-based inverters in the form of VTC plots. Further, the transfer characteristic curves of conventional MOSFET-based inverter and Modified NCFET-based inverter are shown in Fig. 11(b) to match their threshold voltage. With a dual work function metal (DWFM) integration scheme, V_{gs} varies from -1 V to + 1 V at constant $V_{ds} = 0.5$ V [12, 26, 27]. The VTC comparison curve of the conventional MOSFET-based inverter and Modified NCFET-based inverter is plotted in Fig. 11(c). From the plot, we can prove that the transition region (TR) for the Modified NCFET-based inverter is significantly sharper than the conventional MOSFET-based inverter which gives it better speed and fast switching.

Noise Margin calculation The transfer region in the VTC curve of a MOSFET-based inverter is a crucial region that plays a significant role in digital logic operation. The VTC curve represents the relationship between the input voltage (V_{IN}) and the output voltage (V_{OUT}) of the inverter. The transfer region, sometimes referred to as the "active region," is the part of the VTC where the NCFET-based inverter operates as a digital logic gate, it should be low for a quick response of the circuit. On this VTC curve, there are two important critical points where the slope of this curve becomes -1. One point corresponds to logic 0 called maximum input voltage (V_{IL}) and the other corresponds to logic 1 denoted as minimum input voltage (V_{IH}). The threshold voltage in the case of the inverter circuit is the voltage point at which $V_{in} = V_{out}$ or the transition voltage on the VTC curve. In these cases, the V_{th} for conventional MOSFET is 0.41 V and for Modified NCFET, it is 0.43 V. In digital logic circuits, the transfer region corresponds to the range of input voltages where the inverter properly interprets the input as either a logic high (1) or a logic low (0) output. This region is where the inverter performs its primary logic function of signal inversion. The transition region for conventional MOSFET is 0.2 V whereas, for Modified NCFET, it is 0.15 V. The transition from one logic level to another in the transfer region of the NCFET-based inverter is relatively quick. It is important for minimizing the propagation delay of digital circuits. A well-defined transfer region helps in achieving fast switching times. It is a fundamental characteristic that designers consider when designing and optimizing digital circuits to ensure proper logic operation, noise immunity, and signal integrity. The output signals should be clear from noise signals for better circuit performance. That is why we always calculate the noise margin which gives the extraction of noises from output signals [12, 28]. The noise margin is a crucial parameter in the design and analysis of MOSFET-based inverters and other digital logic gates. It plays a significant role in ensuring the reliability and robustness of digital circuits. And it should be as high as possible. It allows for tolerance in voltage levels so that devices with slightly different voltage levels can still interface correctly. It is given below for low signal levels (NM_L) and high signal levels (NM_H) [12]:

$$NM_L = V_{IL} - V_{OL} \tag{5.1}$$

$$NM_H = V_{OH} - V_{IH} \tag{5.2}$$

When input levels are logic 1 and logic 0, respectively, V_{IL} and V_{IH} are the minimum and maximum input voltages. Similar to this, when output levels are logic 0 and 1, respectively, V_{OL} and V_{OH} are the minimum and maximum output voltages. The NM_L for a conventional MOSFET-based inverter is 0.29 V and 0.32 V for a Modified NCFET-based inverter according to Eqs. (5.1) [12]. And NM_H for conventional MOSFET and Modified NCFET are 0.31 V and 0.32 V, respectively according to Eq. (5.2). Achieving a high noise margin in a MOSFET-based inverter is essential for designing robust digital circuits that can tolerate noise and variations in input voltage levels while maintaining reliable logic operation. A high noise margin implies that the circuit can handle noise and still provide a clear distinction between logic high and logic low levels. Noise margin is critical for ensuring that different components and devices in a digital system can communicate effectively. It allows for tolerance in voltage levels so that devices with slightly different voltage levels can still interface correctly. Semiconductor manufacturing processes can result in variations in device characteristics. Noise margin accounts for these

Table 3 Summary of the analog parameter of conventional MOSFET and Modified NCFET

Parameter	Conventional MOSFET	Modified NCFET
I_{on}/I_{off}	1.64×10^{4}	1.92×10^{5}
g_m (μS)	0.11	3.08
TGF (V^{-1})	41.07	58.33
g_d (mS)	0.13	1.16
V_{EA} (V)	3.90	4.63
f_T (THz)	0.50	1.25
A_V (dB)	14.18	19.92

Table 4 Noise margin comparison between inverters using Modified NCFETs and Conventional MOSFETs

Parameter	Conventional MOSFET	Modified NCFET	% Improvement
V_{IL} (V)	0.32	0.35	9.37 (⬆)
V_{IH} (V)	0.52	0.50	3.84 (⬇)
V_{OL} (V)	0.022	0.031	40.90 (⬆)
V_{OH} (V)	0.83	0.82	1.20 (⬇)
NM_L (V)	0.29	0.32	10.34(⬆)
NM_H (V)	0.31	0.32	3.22(⬆)
TR (V)	0.20	0.15	25(⬇)

process variations, making the circuit more robust and less susceptible to manufacturing-related inconsistencies. Figure 11(d) shows the transient analysis for the Modified NCFET-based inverter. The drift–diffusion method solver level 1 (DDML1) technique is used for all the simulations which are carried out at room temperature. The calculated and improved values are tabulated in Table 4. Table 5 compares this work with the published works.

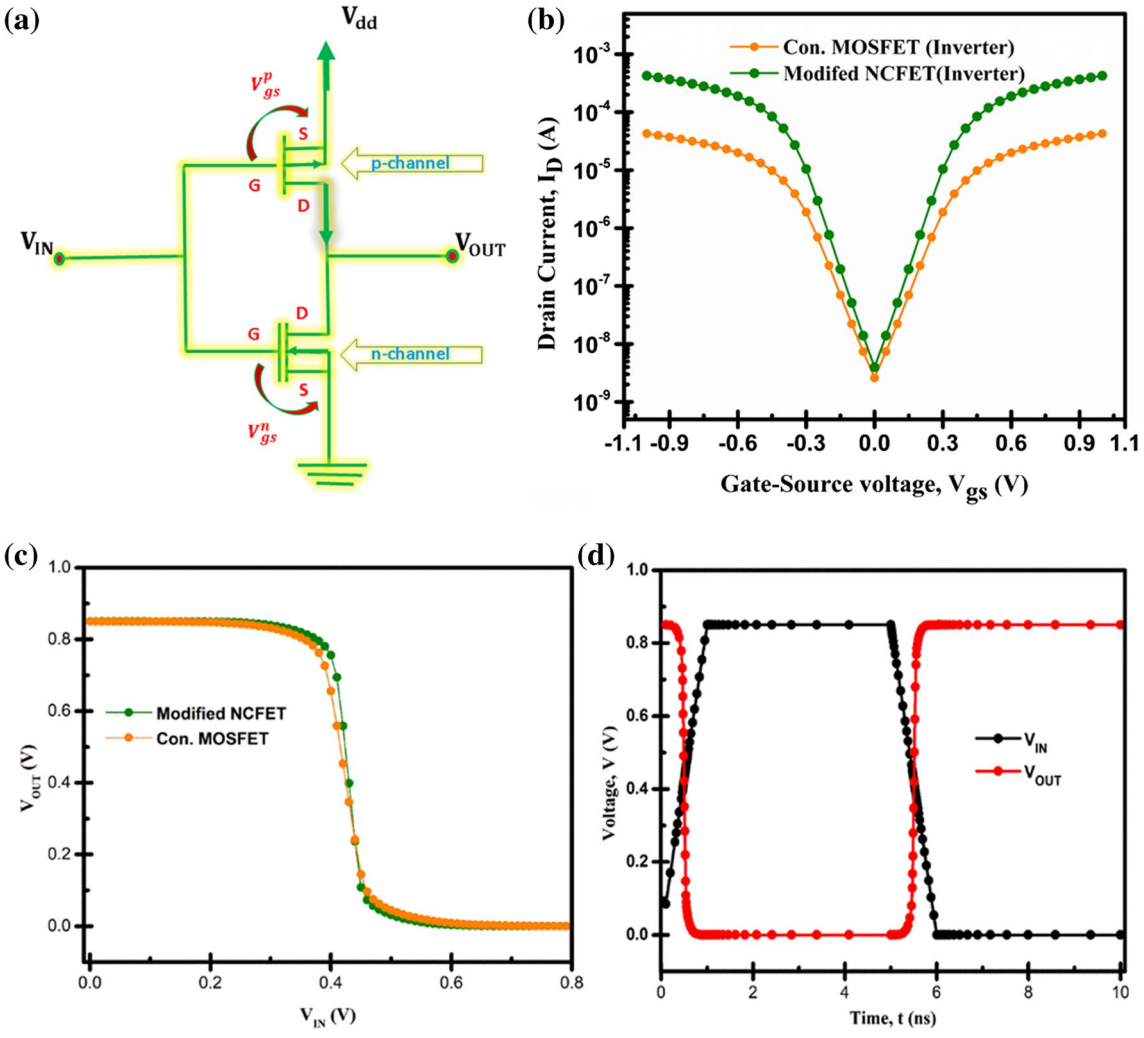


Fig. 11 **a** Schematic diagram of MOS-based inverter **(b).** Threshold voltage matching for Conventional MOSFET-based inverter and Modified NCFET-based inverter. **(c).** VTC curve for conventional MOSFET and Modified NCFET. **(d)** The transient curve for a Modified NCFET-based inverter

Table 5 Comparison of Modified NCFET parameters with other published work

Ref	Year	Device platform	I_{on}/I_{off} ($\times 10^5$)	TGF (V^{-1})	A_v (dB)	V_{EA} (V)	f_T (THz)
[28]	2019	Junctionless Double Gate Vertical MOSFET	NA	26.7	NA	0.59	0.083
[29]	2020	Nano-sheet Transistor	1.90	NA	6.03	2.67	0.585
[30]	2021	SOI Junctionless Nanowire FET	0.82	41.81	NA	NA	0.254
[31]	2022	Tunnel Field Effect Transistor	NA	4.39	0.93	NA	0.940
This work	—-	Modified NCFET	1.92	58.33	19.92	4.63	1.25

6 Conclusion

A quantum ATK and Visual TCAD simulator-based insight for Si-doped HfO_2 NCFET with the use of ferroelectric material is taken into account. Modified NCFET shows amplified results with high ON-current and a better switching ratio of 1.7×10^5. In addition, Modified NCFET suppresses the short channel effects like threshold voltage decreased by 23.75%, and SS reduced by 8.92% compared to conventional MOSFET. Also, the analog parameters of Modified NCFET over conventional MOSFET show improved results. The transconductance of Modified NCFET increased by 34.75% in comparison to the conventional MOSFET structure. Quality factor and device efficiency of Modified NCFET improved by three decimal points and 32.36%, respectively concerning conventional MOSFET structure. Moreover, the cut-off frequency and intrinsic gain show amplified results with 150 times increment and 40.48% results when compared to conventional MOSFET. Better analog performance parameters and reduced short channel effects make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular MOSFET. Furthermore, when we talk about the digital applications like inverters of both these device structures, the noise margin for Modified NCFET comes out to be high when compared to the conventional MOSFET device structure. Its value is 0.29 V for Modified NCFET and 0.31 V for conventional MOSFET structure from the VTC plot. Better analog performance parameters, reduced short channel effects, and higher noise margin make the Modified NCFET (with a high-k dielectric layer in the substrate region) an appealing candidate for digital application in place of regular MOSFET.

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Rishu Chaujar: Writing—review and editing at different stages, supervision.

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Declarations

"The authors have seen all the Ethical Standards and will supposed to follow them in the future."

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PAPER

DFT based atomic modeling and temperature analysis on the RF and VTC curve of high-k dielectric layer-assisted NCFET

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Abstract

In this report, Density Functional Theory (DFT) based calculation using a Quantum Atomistic Tool Kit (ATK) simulator is done for the hafnia-based ferroelectric material. The band structure, projected density of states (PDOS), and Hartree potential (V_H) are taken into account for hafnium oxide (HfO_2) and silicon-doped hafnium oxide (Si-doped HfO_2). Further, we analyze the temperature variation impact on analog parameters and voltage transfer characteristic (VTC) curve of inverter application of Modified Negative Capacitance Field-Effect-Transistor (NCFET) using the Visual Technology-Computer-Aided-Design (TCAD) simulator. The Modified NCFET structure enhances the DC parameters like leakage current (I_{OFF}) and Subthreshold Swing (SS) compared to the conventional NCFET structure. With the temperature impact, the variation in the parameters of Modified NCFET is discussed at 250 K, 275 K, 300 K, 325 K, and 350 K like transconductance (g_m), output conductance (g_d), early voltage (V_{EA}) shows the increment as we move from 250 K to 350 K. The short channel effects (SCEs) like Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) decrease with the temperature fall at 32.98% and 34.74%, respectively. Further, the VTC curve, Noise Margin (NM), and propagation delay of Modified NCFET-based inverter are discussed with the impact of temperature. The propagation delay for the circuit decreased by 67.94% with the rise in the temperature. These factors show that the Modified NCFET-based inverter gives a fast switching performance at high temperatures.

1. Introduction

Silicon-based MOSFETs are knowingly used in microprocessor chips, so they have dominated the IC industry for the past 20 years. The primary goal for such transistors is to fabricate them on small chips [1–5]. Many innovative device structures with small dimensions with better electrostatic control of channels, such as Fin-FETs, dual gates, omega gates, and NCFETs have been proposed. These novel approaches have also been investigated using different materials, such as SiC, III-V semiconductors, II-VI semiconductors, CNT, ferroelectric materials, etc, for power electronics applications. Modern mobile computing demands low power consumption systems, mainly when energy harvesting sources are used for power. I_{ON}/I_{OFF} should be as high as possible at a drain-source voltage (V_{ds}) for energy-efficient performance. The subthreshold slope value should be small to increase the switching ratio (Ion/Ioff). SS can be expressed as

$$SS = \left[\frac{\partial \Psi_s}{\partial V_{gs}}\right]^{-1} \left[\frac{(\partial \log_{10} I}{\partial \Psi_s}\right]^{-1} \tag{1.1}$$

V_{gs} represents the gate-source voltage, and Ψ_s shows the potential of the surface. The first term $\left(\left[\frac{\partial \Psi_s}{\partial V_{gs}}\right]^{-1}\right)$ of equation (1.1) represents the metal oxide semiconductor (MOS) capacitor's electrostatic and the second term $\left(\left[\frac{(\partial \log_{10} I}{\partial \Psi_s}\right]^{-1}\right)$ represents the conductance part of the device [6–9]. Because of the voltage divider between the

silicon channel and gate dielectric, the first term in the formula of the SS does not exceed one in the case of the conventional MOSFET. Also, due to the minority charge diffusion transport in the SS region, the second term remains constant and equivalent to $\frac{2.3kT}{q}$ which is described by the Boltzmann distribution. Therefore, the limit of SS is set to be 60 mV/dec. Many novel devices such as tunneling FET (TFET), Fin-FET, and impact ionization MOSFET (IMOS) are classified in the category of reducing the SS value [10]. However, these drawbacks include complicated process flow and low drive current. Salahuddin *et al* proposed a device structure to overcome the classical limit of 60 mV/dec, which has a steep slope. This device structure, known as the Negative Capacitance Field-Effect-Transistor (NCFET), has the same structure as MOSFET with a difference of the ferroelectric material layer in the gate stack. Experimentally, it is observed that the ferroelectric materials show a negative capacitance value, which, when used in the gate stack of MOSFET, the term $\frac{\partial \Psi s}{\partial Vgs}$ exceeds the value one. Like conventional MOSFET, NCFET devices also have the same diffusion and drift electron transport mechanism, aiming to drive a higher current than tunnel-based FETs because of the greater channel charge thickness brought by intensified Ψ_s at the same off-current. Therefore, NCFET has drawn attention because it can break down the classical minimum limit of Subthreshold Swing, SS = 60 mV/dec with a higher drive current than the conventional MOSFET at the same voltage condition, which is more advantageous while production of new device technology [11–14]. Further, with the advantage of steep slope value, NCFET has many obstacles during its fabrication process. When we fabricate the NCFET device with the use of conventional or existing ferroelectric materials such as Barium Titanate (BTO) and Lead Zirconate Titanate (PZT), the thickness of the gate insulator layer should be such that it balances the large polarization charge density occurred by the ferroelectric material layer and FET channel charge density. It results in hundreds of nanometers, which is a challenging task for fabrication [14–19]. In recent years, ferroelectricity has been found in HfO_2-based thin films that are done by controlling the crystalline phase of the films. For achieving the higher permittivity material for DRAM capacitors, many dopants are introduced in a thin film of HfO_2 to stabilize its tetragonal crystal structure, as this structure has a higher permittivity than the monoclinic structure. Unpredictably, ferroelectricity has been found on the phase boundary between monoclinic and tetragonal structures. 28 nm CMOS technology already shows the use of ferroelectric HfO_2 thin films in the Ferroelectric Random Access Memory (FeRAM). Also, the fabrication of NCFET with the Ferroelectric HfO_2 comes out to be fully compatible with CMOS. NCFET is a very low-cost solution for IoT applications or power requirements without being dependent on the high-cost CMOS technology. NCFET can be manufactured easily by introducing the ferroelectric HfO_2 as a part of the gate stack. For the launch of ferroelectric HfO_2 -based NCFET, one must demonstrate its ultralow supply voltage usage over the existing Ferroelectric based NCFET. A practical guideline for the device design should be followed to achieve fast-speed operations [20–22]. And also, for the process development, material parameters should be properly chosen. Furthermore, it must be calculated theoretically how much switching energy can be reduced by the chosen NCFET.

In this work, the new architecture of Si-doped HfO_2-based NCFET is discussed and compared with the conventional architecture of NCFET. The quantum ATK simulator uses the DFT calculation for hafnium oxide and Si-doped hafnium oxide. Also, the temperature analysis of the architecture is performed with the Visual TCAD simulator. The temperature range is taken from 250 K to 350 K. The impact of temperature on the NCFET-based inverter is also discussed in this work with NM calculations. This architecture is based on the practical device design, which can make energy-efficient equipment by regulating material parameters. These examinations can be done by physical-based simulations like on the ATLAS Visual TCAD. These simulations can involve energy efficiency, material requirement, and operating speed.

2. Device structure and simulation methodology

The Quantum ATK simulator is used for the DFT calculation of the HfO_2 atom, and the Visual TCAD simulator is used for the compact modeling of device architecture. DFT is a quantum-mechanical atomistic modeling approach. DFT is used to verify any materials' energy, structure, and characteristics. The interface engineering in HfO_2-based gate stacks has been done to change the function of the layer. Silicon-doped HfO_2 cubic structure is used as the ferroelectric material in the device architecture to utilize in industrial applications like sensors, fuel cells, and memory devices. The high density of hafnium in HfO_2 results in low lattice thermal conductivity, measured in the range of 0.49 to 0.95 W /m -K .

2.1. Structure of ferroelectric HfO_2-based crystal

Silicon-doped hafnia (Si-doped HfO_2) can exhibit a different bonding nature compared to pristine hafnia due to the introduction of silicon (Si) atoms into the crystal lattice. The exact bonding nature in silicon-doped hafnia can depend on several factors, including the concentration of silicon dopants and the local environment of the dopants. One will find a combination of ionic and covalent bonding in both pristine hafnia and silicon-doped hafnia. Hafnia inherently comprises hafnium (Hf) and oxygen (O) atoms. Silicon is also a non-metal. The electronegativity difference between Hf and O leads to ionic bonding, while covalent bonds exist between Hf and

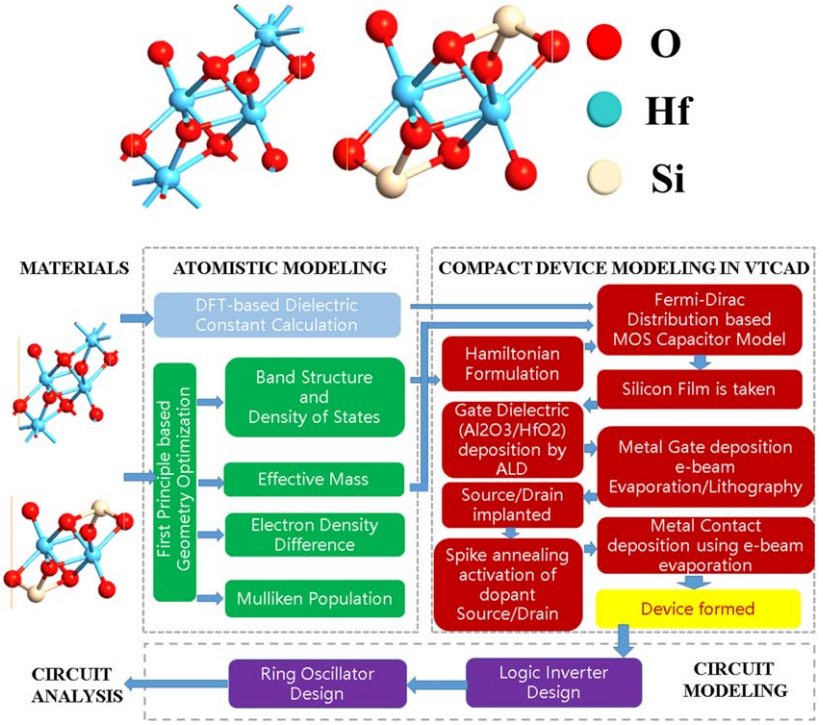

Figure 1. Structure of HfO_2 and Si-doped HfO_2 and synopsis of 'atom-to-circuit' multiscale modeling methodology.

O atoms. Introducing silicon into the lattice does not change the basic ionic and covalent bonding characteristics. The dimension of simple cubic HfO_2-based ferroelectric are a = 10.23 A, b = 10.23 A, c = 10.23 A, $\alpha = 90$, $\beta = 90$, $\gamma = 90$. The structure has four hafnium (Hf) atoms and eight oxygen (O) atoms without any doping [23, 24]. For silicon (Si) doping, 25% of Si is added, as shown in figure 1. Using this Si-doped HfO_2 in gate stacking of the device governs the negative capacitance effect. Quantum Atomistic Tool Kit (QATK) is one such toolkit that can perform electronic structure calculations for molecules and materials.

To calculate the energy values of HfO_2 using the Linear Combination of Atomic Orbitals (LCAO) approximation in QATK, the general LCAO approximation to perform such calculations is spin is unpolarised (not distinguishing between the two possible spin states of electrons), Generalized Gradient Approximation (GGA) exchange–correlation (describe the exchange and correlation effects in terms of electron density gradients. It is an improvement over the simpler Local Density Approximation (LDA) and adds a dependence on the gradient (or first derivative) of the electron density), Fermi–Dirac occupation (to determine how many electrons occupy each molecular orbital or energy level), and density mesh cut-off at 125 Hartree (determines the energy range). Further compact device modeling using the Visual TCAD simulator is done for circuit analysis, as shown in figure 1. A visual TCAD simulator is used to perform all the numerical simulations of temperature analysis presented in this work. For the simulation of silicon regions and the ferroelectric region in n-type architecture, 2D electrostatics is used. The Modified NCFET has an extra layer of high-k dielectric insulator (k = 25) with a thickness of 20 nm in the substrate region with the addition of a ferroelectric material layer (HfO_2FE) in the gate stack shown in figure 2(a). As both the architectures are of n channel type, the substrate regions are doped with the p-type impurities having a concentration of 1×10^{16} cm^{-3}.

The extensions of the source/drain with Gaussian doping of 1×10^{19} cm^{-3} are used to reduce the parasitic capacitance. The gate length of 25 nm is used for both the device structure. In the gate stack, the layers of SiO_2 and HfO_2FE have a thickness of 1 nm and 2.5 nm, respectively. These device simulation parameters are tabulated in table 1. The drift-diffusion formulation in Fermi–Dirac statistics, which defines the electrical transport in the silicon region of architecture, is used. Landau-Khalatnikov equation solves the 2D-electrostatics, which gives Landau's parameters (α, β, γ) for a ferroelectric material. L-K equation is a time-dependent phenomenological equation for ferroelectric material in terms of Landau free energy (G) and characteristics response time (τ) is given as

$$\tau\frac{dP}{dt} = -\frac{dG}{dP}, \text{ And } G(P, E) = \frac{\alpha}{2}p^2 + \frac{\beta}{4}p^4 + \frac{\gamma}{6}p^6 - E.P, \tag{2.1}$$

Out of this equation (2.1), two parameters are $\alpha = -1e+07$ and $\beta = 8.9e+08$. The supply voltage of 0.5 V is used for all the simulation work. The calibration of simulated work on Visual TCAD with the published work on

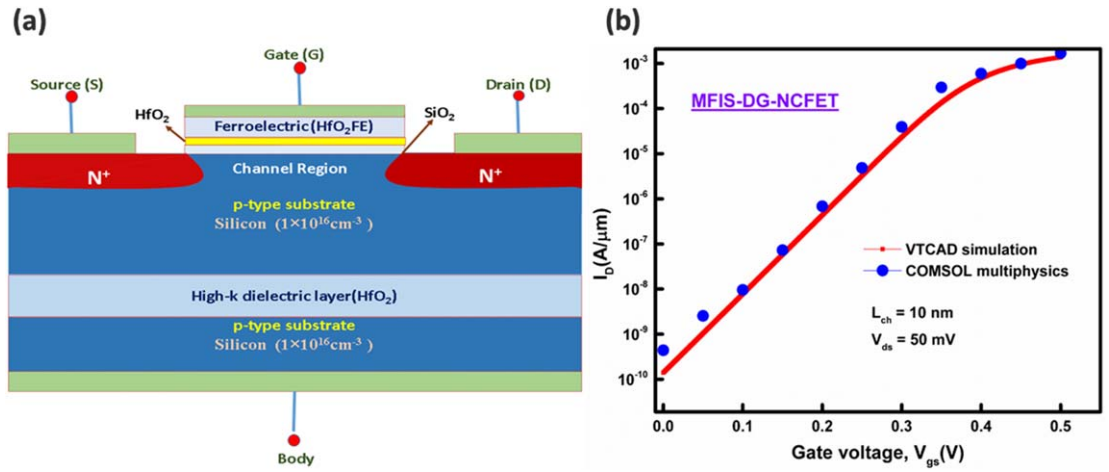

Figure 2. (a) The Modified NCFET device schematic architecture. (b) Calibrated I_D-V_{gs} of metal-ferroelectric-insulator-semiconductor double gate NCFET on VTCAD simulator with published results on COMSOL multiphysics.

Table 1. Default device dimensions and parameters of conventional NCFET and Modified NCFET structure are taken for the simulation.

Parameter	Conventional NCFET	Modified NCFET
L_g (nm)	25	25
$L_{S/D}$ (nm)	10	10
T_{ox} (nm)	1	1
T_{FE} (nm)	2.5	2.5
T_{ins} (nm)	0	20
$N_{S/D}$ (cm^{-3})	1×10^{19}	1×10^{19}
N_{ch} (cm^{-3})	1×10^{16}	1×10^{16}
Φ_m (eV)	4.5(Npoly Si)	(Npoly Si)

COMSOL Multiphysics by Girish Pahwa *et al* [25]. Figure 2(b) presents the calibrated transfer characteristics of both simulators.

3. Results and discussion

3.1. DFT analysis of HfO_2 and Si-doped HfO_2

Figure 3 shows the band structure of simple cubic HfO_2 structure (a) and 25% Si-doped HfO_2 (b). It was discovered that the direct bandgap of HfO_2 reduced significantly from 2.808 eV to 0.347 eV by 25% Silicon doping with two-fold degeneracy. Further, figure 3 shows the transmission spectra corresponding to hafnium oxide with or without silicon doping.

The transmission peaks increase as the doping of silicon increases, which is why the conduction in Si-doped HfO_2 is much higher than the without-doped HfO_2. In this case, the author marks the zero energy level at the Fermi energy level. However, the zero energy level is a reference point used to measure energies in a system. In contrast, the Fermi energy level is a material-specific concept that describes the highest energy level occupied by electrons at absolute zero temperature. The Fermi energy level is crucial for understanding the behaviour of electrons in materials and their electrical and thermal properties. In band structure diagrams, specific colours are often used to represent different energy bands or states within a material. The green colour band represents the highest energy valence band, and the red one shows the lowest conduction band. The difference between these two bands is the bandgap for the corresponding structure, which is 2.808 eV in the case of HfO_2 and 0.347 eV for 25% Si-doped HfO_2.

Silicon states enhances the bandgap and a comparable bandgap changes along the direction for all the lower concentration of silicon atoms. Tran Blaha Modified Becke Johnson (TB-mBJ) is used to calculate the electron band structure of the atom accurately. Figure 4 shows the variation of the Hartree potential with length for both atoms. The lower the Hartree potential of an atom, the more stable the atom. So, the Si-doped HfO_2 is more

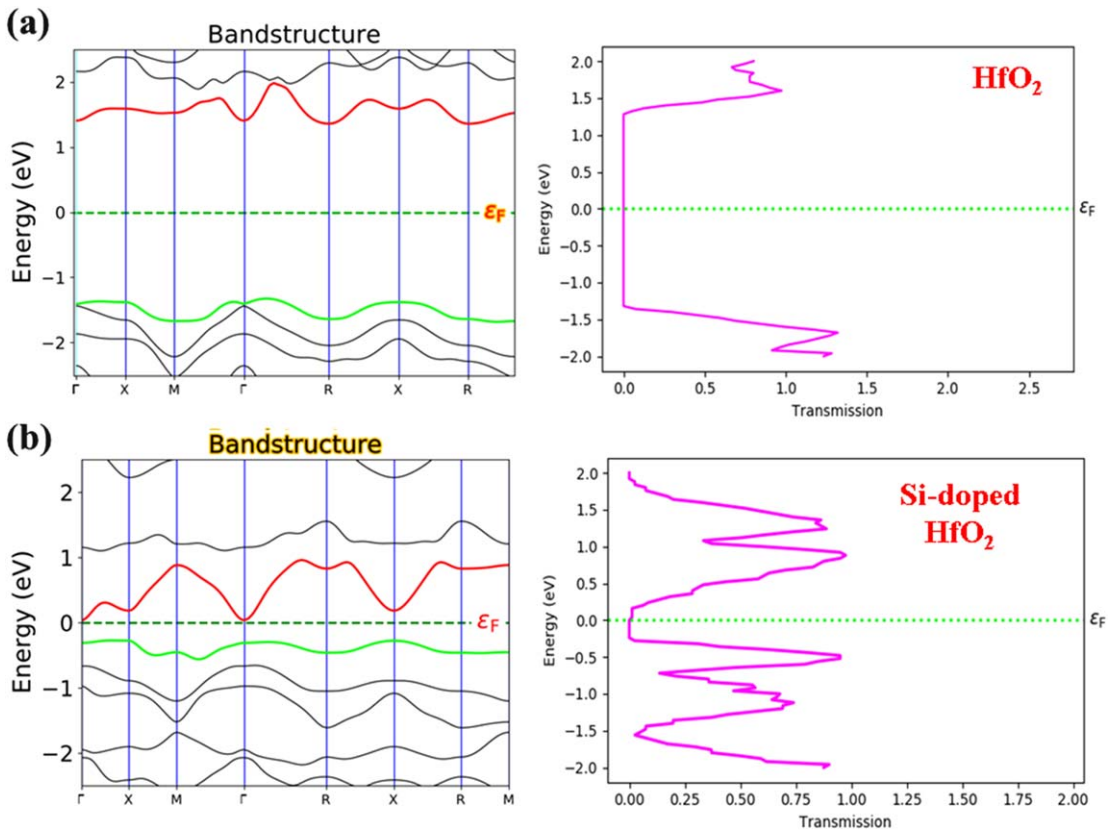

Figure 3. (a) The band structure and corresponding transmission spectra with the energy for (a) HfO_2 and (b) Si-doped HfO_2.

stable than the HfO_2 atom. It takes less time to move from one orbit to another. It reveals the mean electrostatic interaction between the atoms. Poisson's equation is helpful for the calculation of this electrostatic potential [26]. Figure 5 shows the projected density of states concerning energy levels. It represents the particular density of states like spin-up and spin-down states.The projected DOS for Si-doped HfO_2 is much more dense and higher than the HfO_2 without doping. The contribution of induced silicon atoms in the lower conduction and valance bands shows the hybridization in the orbits. Hence, the magnitude and peaks increase as the concentration of the silicon atoms increases.

3.2. SCEs analysis between conventional NCFET and Modified NCFET

The parameters of conventional NCFET and Modified NCFET structures are already discussed in section 2. Figure 6 shows the performance parameter in the form of drain current (I_D) concerning the gate voltage (V_{gs}).

This variation shows that the leakage current (I_{OFF}) is reduced significantly in the Modified NCFET structure. The Modified NCFET contains the insulator part in the substrate region, which acts as the barrier to the mobile electrons in the silicon part of the substrate region. Due to this, the leakage current is reduced, which directly increases the device's switching ratio (I_{ON}/I_{OFF}). Further, as the effect of negative capacitance, the SS value decreased, but more decrement in the SS value happened due to the layer of the high-k dielectric material layer in the substrate region of the Modified NCFET structure, as shown inset of figure 6.

3.3. Analog/RF performance metrics at different temperatures

The transfer characteristics (I_D-V_{gs}) in linear scale for Modified NCFET for temperatures ranging from 250 K to 350 K is presented inset of figure 7(a) at a constant supply voltage or drain voltage (V_{ds}) of 0.5 V. From this variation, we can state that with the increase in temperature from 250 K to 350 K, the threshold voltage is reduced down slightly and also gives the high ON-current (I_{ON}).

Also, the same variation in the log scale is given in figure 7(a), which shows that the increment in temperature gives a high ON-current and slightly high off-current. This variation can be described according to the energy band gap theory. As the temperature increases, the energy band gap starts decreasing, and the passing of electrons from the valence band to the conduction band becomes easy, which results in the rise of the device's off-state current and on-state current. The switching ratio (I_{ON}/I_{OFF}) due to transfer characteristics decreases with the temperature rise, as portrayed in figure 7(b). Thus, with the temperature rise, the device performance

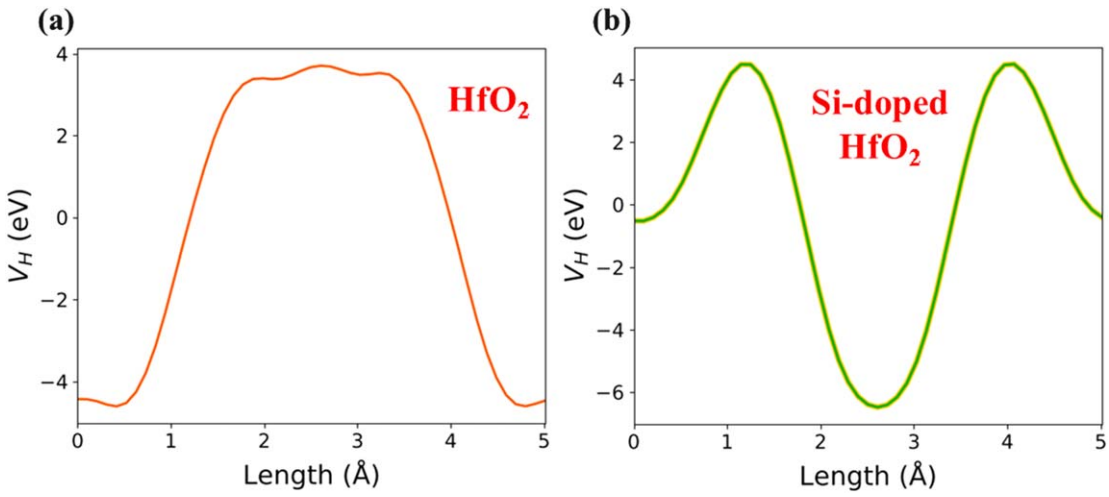

Figure 4. The Hartree potential of (a) HfO_2 and (b) Si-doped HfO_2.

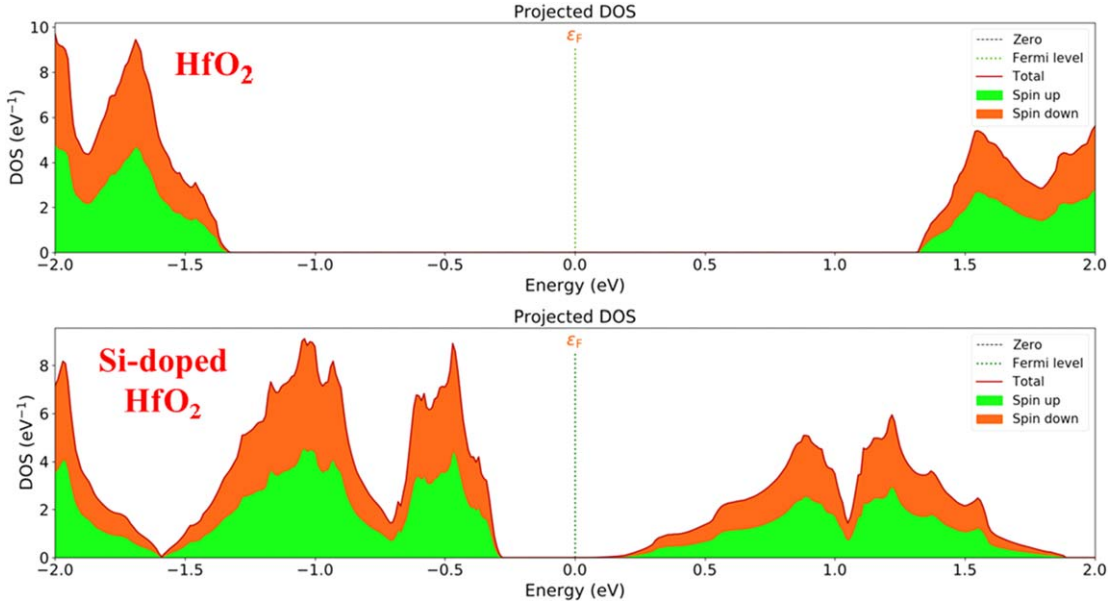

Figure 5. The projected DOS of HfO_2 and Si-doped HfO_2.

degrades with the concerning switching ratio. The effect of temperature on the short channel effects can be seen in figure 7(b) in the form of DIBL value [27, 28]. These effects come because of shortened gate or channel length. When we shorten the channel length, the source and drain come close to each other, and the supply voltage biasing affects the potential barrier between these terminals. So, the punch-through condition arises between the source and drain terminal, and hence the leakage current increases. That is why one should have to minimize these effects. DIBL can be formulated as in equation (3.1) by taking V_{th} at $V_{ds} = 0.5$ V.

$$DIBL = \frac{\partial V_{th}}{\partial V_{ds}} \tag{3.1}$$

Concerning temperature rise, the DIBL value starts rising, which is unsuitable for the device's performance. At the lower temperature range of 250 K to 300 K, the DIBL value is in a specific range, and it starts increasing linearly with the increase in temperature. Another short channel effect is the subthreshold swing value. The SS variation as a function of temperature is shown inset of figure 7(b); according to the negative capacitance phenomenon, the SS value becomes low with the use of ferroelectric material in the gate stack [29]. But with the increase in the temperature from 250 K to 350 K, this value starts increasing, which shows the performance degradation of the device. Another factor in the same figure 7(b) (inset) is the threshold voltage (V_{th}) as a

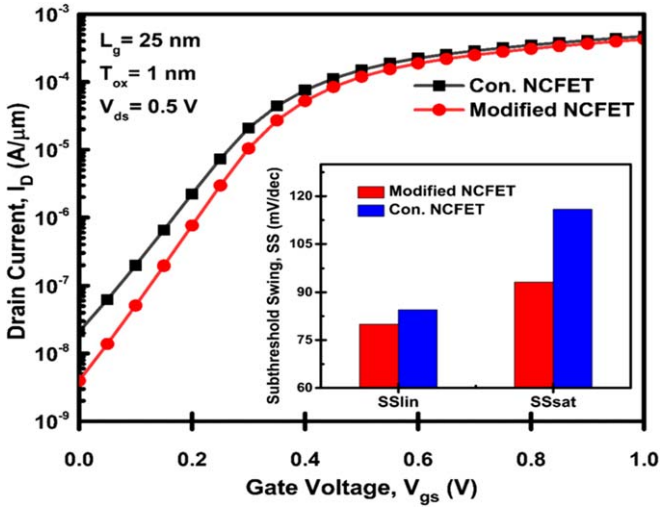

Figure 6. Transfer characteristic and Subthreshold Swing (inset) comparison of conventional NCFET and Modified NCFET at a drain-source voltage of 0.5 V.

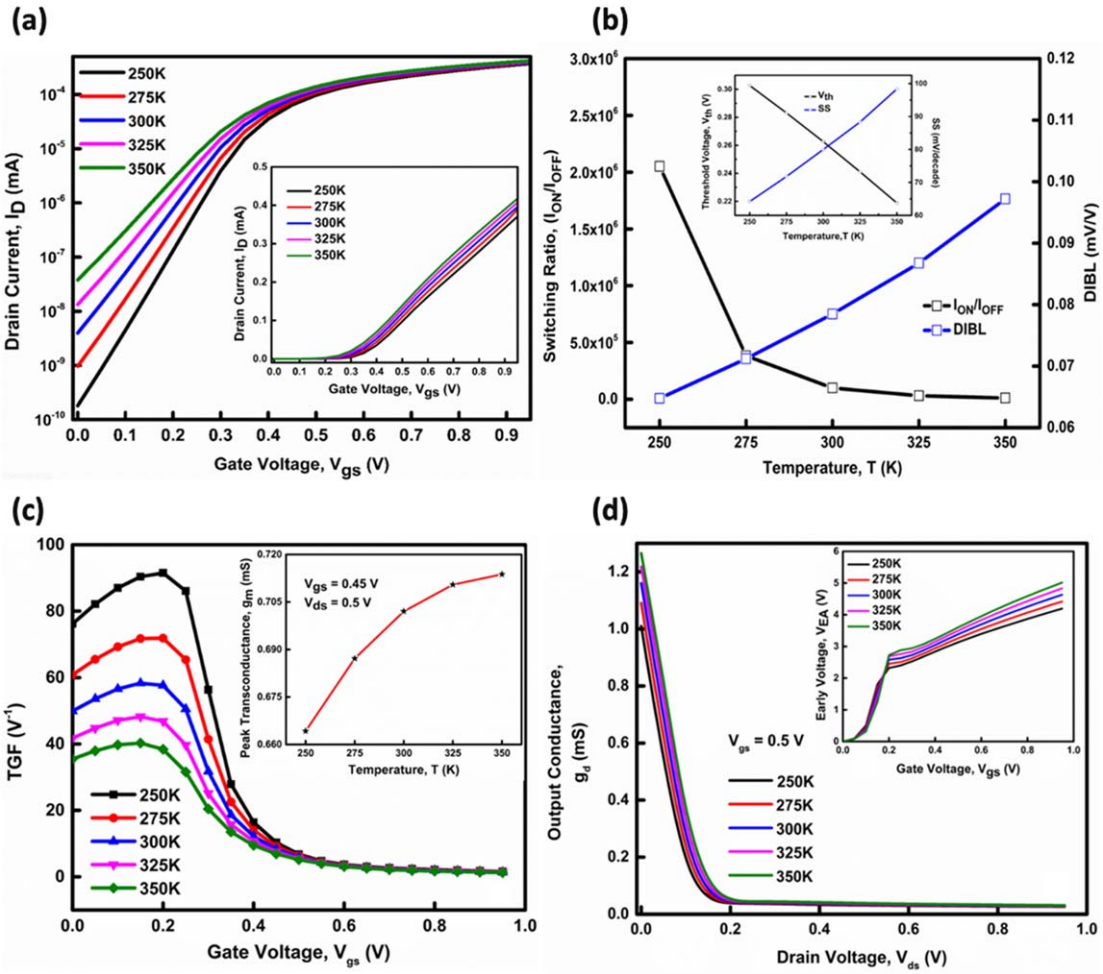

Figure 7. Temperature variation impacts (a) I_D-V_{gs} characteristic in logarithm scale and linear scale (inset). (b) Effect of temperature variation on I_{ON}/I_{OFF}, DIBL and V_{th}, SS (inset). (c) Peak transconductance value (inset) and transconductance generation factor (TGF). (d) Output conductance (g_d) and Early voltage (V_{EA}) (inset) with gate voltage (V_{gs}).

Table 2. Variation of SCEs with the impact of temperature.

Short channel effects	250 K	275 K	300 K	325 K	350 K	% Change (250 K to 350 K)
V_{th} (V)	0.30	0.28	0.26	0.24	0.21	30.00(↓)
DIBL (mV/V)	0.065	0.071	0.078	0.086	0.097	49.23(↑)
SS_{lin} (mV/dec)	64.18	71.80	83.34	88.34	98.35	53.24(↑)

function of temperature. All these SCEs are tabulated in table 2. For good device performance, the threshold voltage value should be as low as possible because it is the voltage value required for a device to turn on. This behaviour happens due to the use of the insulator layer in the middle of the substrate region, which acts as a barrier for the mobile electrons present in the substrate region to generate the channel region. As the temperature increases, these mobile electrons dominate more, resulting in a lower threshold voltage.

Moving to analog parameters, figure 7(c) (inset) presents the peak transconductance (g_m) observed at V_{gs} = 0.45 V for all the temperatures ranging from 250 K to 350 K. Transconductance can be formulated as

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \tag{3.2}$$

$$TGF = \frac{g_m}{I_D} \tag{3.3}$$

$$V_{EA} = \frac{I_D}{g_d} \tag{3.4}$$

Transconductance tells about the input conductance for a device that describes the drain current change with the gate voltage shift as defined in equation (3.2) [30]. Graph 7(c) (inset) represents the temperature dependence on the peak transconductance. The peak value of transconductance is increasing as the temperature ranges from 250 K to 350 K. This variation shows the improvement of mobility in the electron results in a high value of transconductance with temperature. Further, the transconductance generation factor (TGF) variation and the temperature range are given in figure 7(c). TGF provides the amount of gain generated per unit of power loss and is given by equation (3.3). Figure 7(c) shows the high values of TGF at low voltages and lower temperatures, which indicates the application in ultra-low-power (ULP) circuits. All the high values of TGF obtained in the subthreshold region illustrate the sustainability of Modified NCFET in ULP applications. With the temperature rise, the rise in the drain current and the lower value of g_m give the lower value of TGF [20]. However, with a further increase in the V_{gs}, this difference in the TGF curves remains insignificant. In addition, figure 7(d) shows the behaviour of output conductance (g_d) concerning the drain-source voltage (V_{ds}) for different temperatures. It gives the current driving ability of the device. At low drain-source voltage, g_d decreases with an increase in the temperature range from 250 K to 350 K [20].

The inset of figure 7(d) portrays the effect of temperature on the early voltage (V_{EA}). The VEA increases at higher voltages as the temperature rises from 250 K to 350 K. The trend for this can be explained by the expression for the V_{EA} [21]. As g_d increases at lower values of voltage and decreases at higher voltage values with the temperature, V_{EA} will increase at higher voltage values with the rise of temperature according to equation (3.4). All the RF and analog parameters are summerised in table 3. Further, figure 8 shows the different contour plots across the length of the channel, like figure 8(a) shows the Auger and SRH recombination in the channel region across the length of the gate. Similarly, figures 8(b), (c), and (d) show the electric field, conduction band energy, and valence band energy across the channel length, respectively.

3.4. Temperature impact on the VTC curve of Modified NCFET-based inverter

To show the temperature impact on the VTC plot of a Modified NCFET-based inverter, we designed a setup with n-channel and p-channel Modified NCFET on the Visual TCAD simulator, which is electrically isolated with a 10 nm SiO_2 spacer. NpolySi with a 4.5 eV and 4.9 eV work function was used for n-channel and p-channel Modified NCFET, respectively. The doping concentration of $1\times10^{16}cm^{-3}$ and $1\times10^{19}cm^{-3}$ is taken for substrate and source/drain of their respective type in n-channel and p-channel Modified NCFET. The schematic circuit diagram of the Modified NCFET-based inverter is shown in figure 9(a). Before any structure-based inverter characteristic, one should match the threshold voltage of an inverter's n-type and p-type components so that the characteristic curve of the inverter from $V_{gs} = -1$ to 1 V becomes continuous without any breaking point of current. So, for different temperatures, the V_{th} matching curves are shown in figure 9(b).

The temperature impact on the voltage transfer characteristic (VTC) curve for a Modified NCFET-based inverter is shown in figure 9(c). The variation indicates that the transition region (TR) is getting high with the temperature rise, which delays the device's switching. It shifts from 0.16 V to 0.35 V as the temperature increases

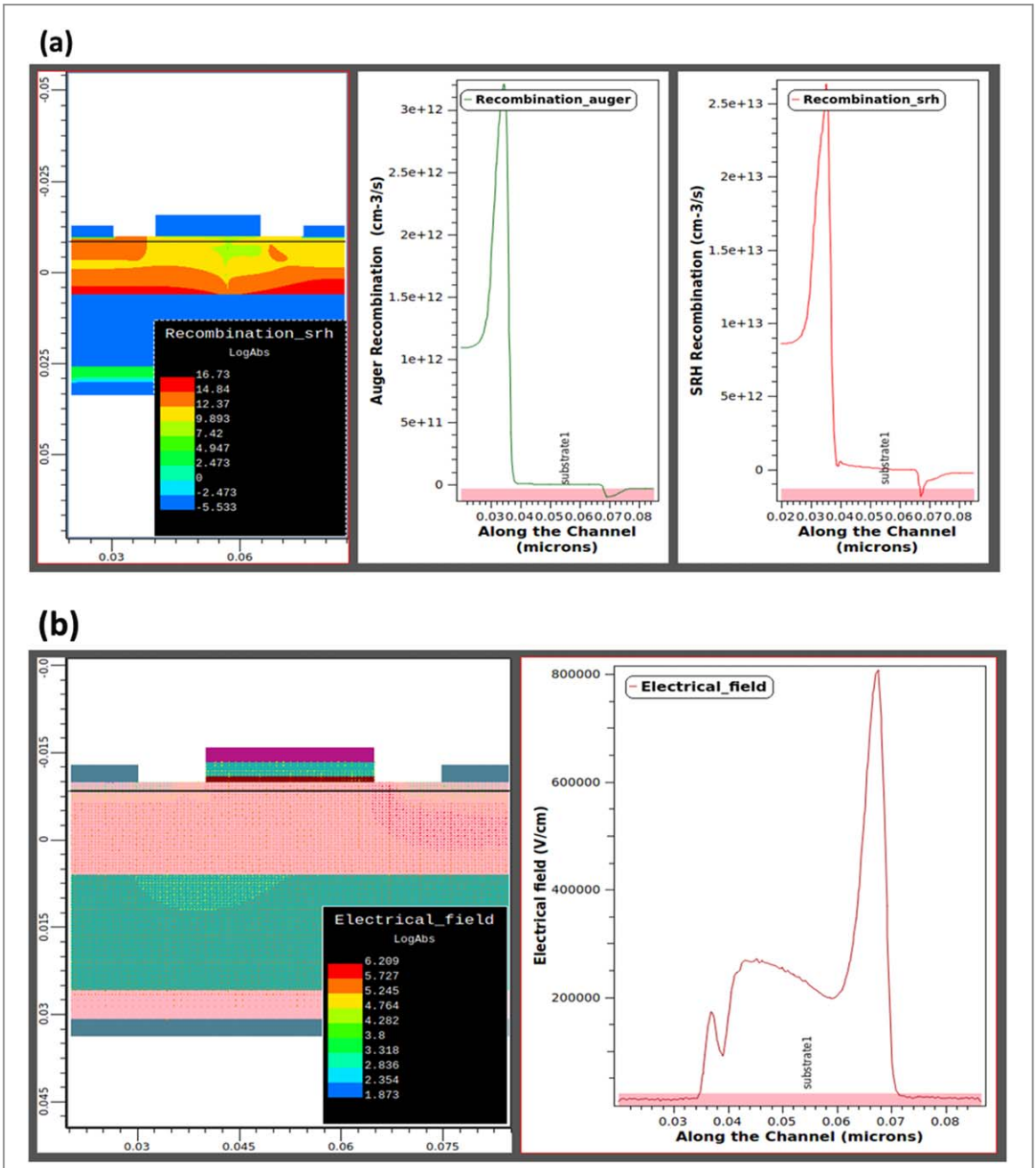

Figure 8. (a) Auger and SRH recombination (b)Electric Field (c) conduction Band energy (d) Valence Band energy across the length of the channel region.

from 250 K to 350 K. In the VTC curve of the inverter, there are two critical points at which the slope of the curve becomes negative. These points correspond to logic 0, called the maximum input voltage (V_{IL}), and logic 1, called the minimum input voltage (V_{IH}) [31–33].

3.4.1. Noise margin calculation

The Noise Margin (NM) determines the noise immunity of a device; this value should be high enough to measure the noise components in the device. For low signal levels (NM_L) and high signal levels (NM_H), NM is given as in equations (3.5) and (3.6).

$$NM_L = V_{IL} - V_{OL} \tag{3.5}$$

$$NM_H = V_{OH} - V_{IH} \tag{3.6}$$

Where V_{OH} and V_{OL} define the maximum output voltage and minimum output voltage when output levels are logic 1 and logic 0, respectively [22], all parameters are tabulated in table 4.

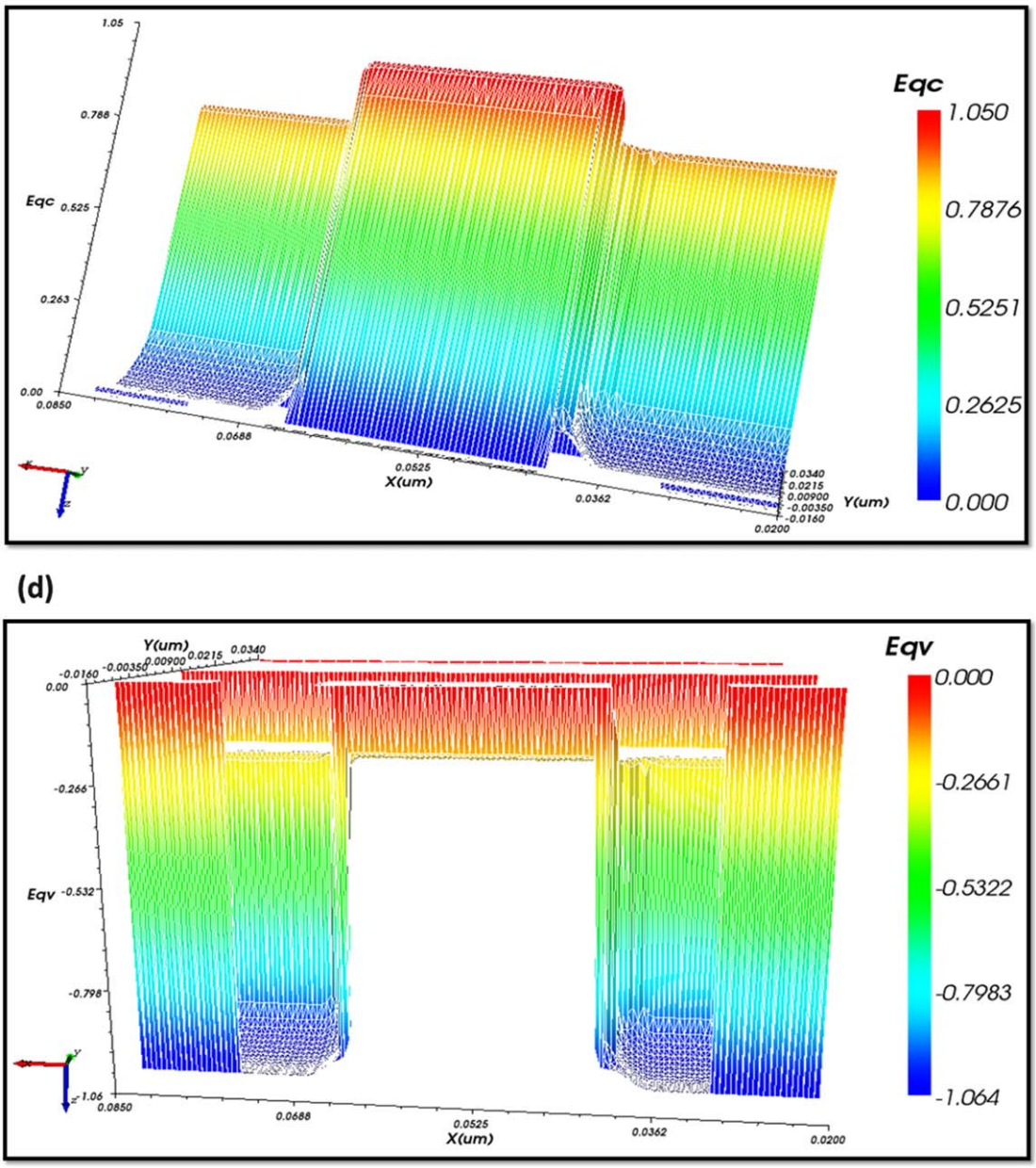

Figure 8. (Continued.)

Table 3. Summary of analog and RF performance parameters of Modified NCFET with different temperatures.

Parameter	250 K	275 K	300 K	325 K	350 K	% change (250 K to 350 K)
I_{on}/I_{off}	2.04×10^{6}	2.61×10^{6}	1.0×10^{5}	3.06×10^{4}	1.10×10^{4}	99.46(↓)
g_m (mS)	0.66	0.68	0.70	0.71	0.72	09.09(↑)
TGF (V^{-1})	91.49	71.86	57.62	46.84	38.41	58.13(↓)
g_d (mS)	1.01	1.09	1.51	1.21	1.26	24.75(↓)
V_{EA} (V)	4.19	4.41	4.63	4.83	5.01	19.57(↑)

3.4.2. Propagation delay and transition time

In the case of FETs, there are many non-ideal effects, out of which parasitic capacitance is one. Because of these capacitances, the delay in voltage change is observed, which limits the speed of operation. This work section shows how these capacitances affect the output waveform. With the help of propagation delay and transition delay, we can test the speed performance of the device and how it changes with the temperature variation. We

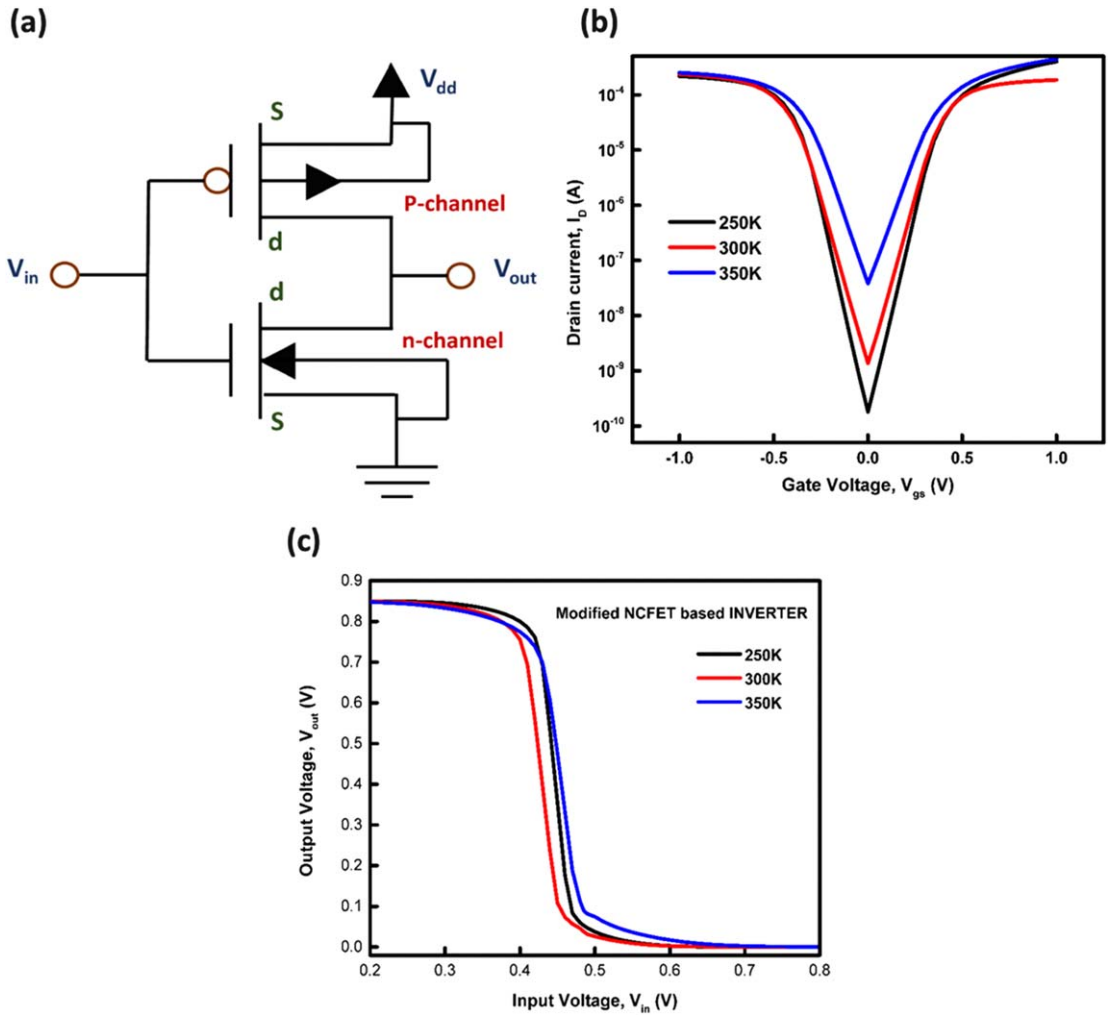

Figure 9. (a) Schematic diagram of inverter using Modified NCFET architecture. (b) Threshold voltage matching plot for Modified NCFET-based inverter for three temperatures: 250 K, 300 K, and 350 K. (c) VTC curve of Modified NCFET-based inverter at temperatures 250 K, 300 K, and 350 K.

apply a step voltage at the device's input for the propagation delay, and we get the output waveform with a transition delay. The two propagation delays shown in figure 10(a), marked as t_{pHL} and $t_{pLH,}$ are known as propagation delay time for High-to-Low and Low-to-High, respectively. The inverter operates between two voltages: output high voltage (V_{OH}) and output low voltage (V_{OL}). The t_{pHL} is the time required for the output to fall from V_{OH} to $(V_{OH} + V_{OL})/2$. Similarly, t_{pLH} is the time required for the output waveform to rise from V_{OL} to $V_{OH} + V_{OL})/2$. All these parameters are shown in figure 10(a). So, the propagation delay is the average of these two given by equation (3.7)

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \tag{3.7}$$

$$t_{rf} = \frac{t_r + t_f}{2} \tag{3.8}$$

In figure 10(b), the propagation characteristic of the Modified NCFET-based inverter at 300 K is shown. From figure 10(c), we can see the impact of temperature on the propagation delay factors t_{pHL} and $t_{pLH,}$ and it can be concluded that with the temperature rise, t_{pHL} decreases, which indicates the fast switching of the device. And the t_{pLH} increases with the temperature rise.

Next, the transition time factors are rise time (t_r) and fall time (t_f). Rise time is the time interval when the output signal rises from 10% to 90% of the (V_{OH}-V_{OL}) value, and fall time is the time step in which the output signal falls from 90% to 10% of the (V_{OH}-V_{OL}) value shown in figure 10(a). Hence, the transition time is the average of these quantities called Edge rate (t_{rf}) and is given by equation (3.8). Figure 10(d) shows that the

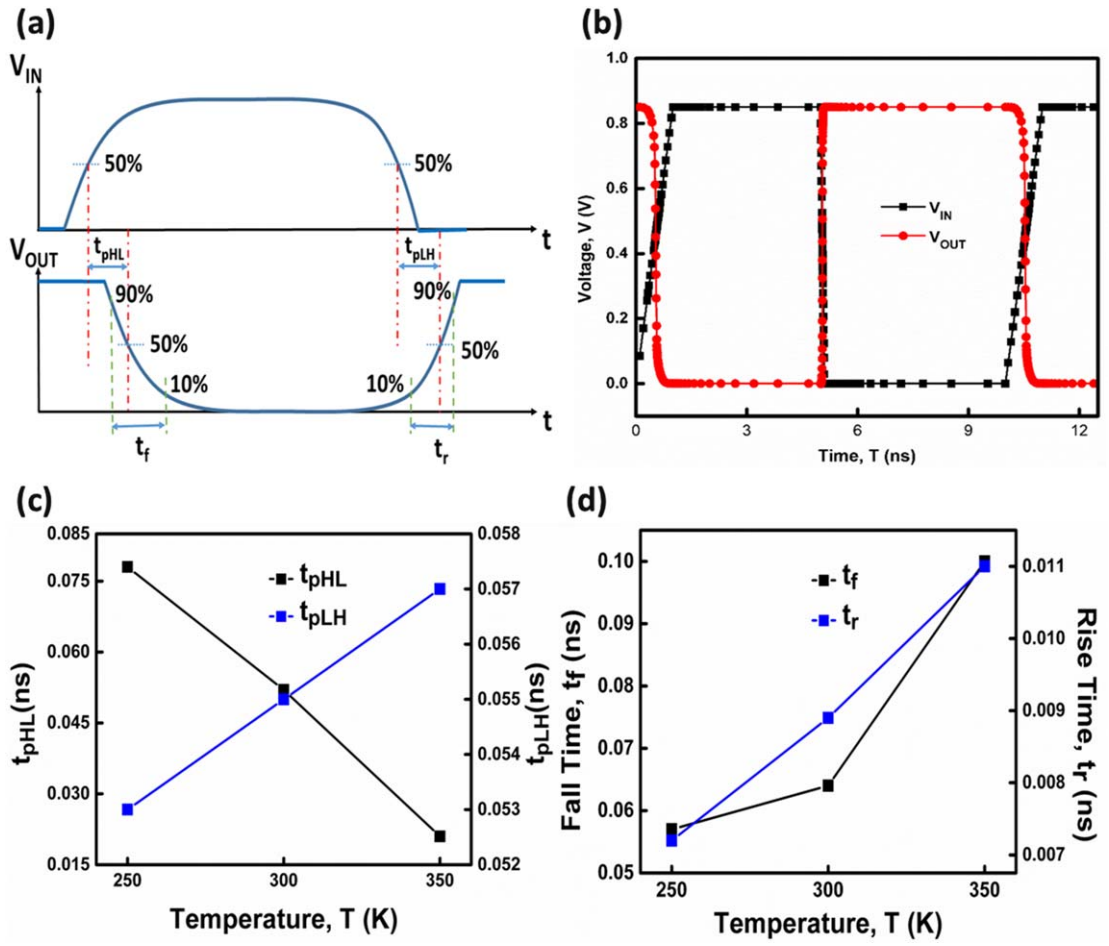

Figure 10. (a) Propagation delay and transition time schematic of NCFET-based inverter. (b) Propagation characteristic of Modified NCFET-based inverter at 300 K. (c) Variation of propagation delay with the temperature. (d) Variation of transition time with the rise of temperature.

Table 4. Comparison of noise margin and propagation delay for different temperatures of Modified NCFET-based inverters.

Parameter	250 K	300 K	350 K	% change (250 K to 350 K)
V_{IL} (V)	0.39	0.35	0.30	23.07(↓)
V_{IH} (V)	0.55	0.60	0.65	18.18(↑)
V_{OL} (V)	0.013	0.003	0.007	46.17(↓)
V_{OH} (V)	0.81	0.82	0.83	02.47(↑)
NM_L (V)	O.377	0.347	0.293	22.28(↓)
NM_H (mV)	0.260	0.220	0.183	29.61(↓)
TR (V)	0.16	0.25	0.35	118.35(↑)
t_{pHL}(ns)	0.78	0.52	0.21	73.07(↓)
t_{pLH}(ns)	0.053	0.055	0.057	07.55(↑)
t_p(ns)	0.416	0.287	0.133	68.02(↓)
t_r(ns)	0.0072	0.0089	0.0110	52.77(↑)
t_f(ns)	0.057	0.064	0.100	75.43(↑)
t_{rf}(ns)	0.0321	0.0364	0.0555	72.89(↑)

transition time increases with the rise in the temperature, which shows the slow switching speed. So, it is better for the Modified NCFET device to operate at low temperatures for fast-speed performance. All these parameters are tabulated in table 4. Comparison of Modified NCFET device with the other published work is tabulated in table 5.

Table 5. Comparison of Modified NCFET parameters at 250 K with other published work.

References	Year	Device platform	I_{on}/I_{off} ($\times 10^5$)	TGF (V^{-1})	A_v (dB)	V_{EA} (V)	f_T (THz)
[34]	2019	Junctionless Double Gate Vertical MOSFET	NA	26.7	NA	0.59	0.083
[35]	2020	Nano-sheet Transistor	1.90	NA	6.03	2.67	0.585
[36]	2021	SOI Junctionless Nanowire FET	0.82	41.81	NA	NA	0.254
[37]	2022	Tunnel Field Effect Transistor	NA	4.39	0.93	NA	0.940
This work	—	Modified NCFET(at 250 K)	20.4	91.49	0.65	4.19	NA

4. Conclusions

It is concluded from the study of DFT calculation that Si-doped HfO_2 gives a less direct bandgap, dense projected DOS, high transmission peaks, and lower Hartree potential when compared to the undoped HfO_2 atom. Hence, Si-doped HfO_2 is used as the ferroelectric material in the gate stack of device architecture, which gives us a better industrial application when using natural ferroelectric materials. Further, it is observed that Modified NCFET shows improved factors. IOFF and SS are reduced by 81.17% and 10.28%, respectively, compared to conventional NCFET device architecture. The switching ratio is increased by one decimal point compared to the conventional one. The above study considers the impact of temperature variation on the analog, RF, wireless performance, and digital application parameters of the Modified NCFET structure. Simulation results show the variation in different parameters when the temperature rises from 250 K to 350 K with the step size of 25 K. Starting with the basic $I_{ON,}$ which increases by 12.39%, and V_{th} is reduced by 30%.

Further, the impact of temperature variations on SCEs is shown as the DIBL is reduced by 32.98% and SS is reduced by 34.74% as the temperature decreases from 350 K to 250 K. Furthermore, as the temperature rises from 250 K to 350 K, the analog parameters shows the following trends: g_m and g_d is enhanced by 9.09% and 2.75%, respectively and TGF is reduced by 58.02%. Also, V_{EA} is enhanced with 19.57%. In continuation, we examine the effect of temperature on the VTC plot of a Modified NCFET-based inverter. We have taken out three temperature values to extract the variation, which are 250 K, 300 K, and 350 K. If we see the trend with the decreasing temperature, it has been observed that the transition region (TR) decreases as the temperature drops. It becomes 54 times less when the temperature changes from 350 K to 250 K. The noise margin factors are also increased when the temperature falls. The NM_L and NM_H show improvement with 33.43% and 42.26% increments, respectively. The above results show that the Modified NCFET gives better digital application parameters at lower temperatures. Propagation delay is decreased by 67.94% when the temperature rises from 250 to 350 K, providing better and faster switching performance.

Acknowledgments

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Data availability statement

The data cannot be made publicly available upon publication because the cost of preparing, depositing and hosting the data would be prohibitive within the terms of this research project. The data that support the findings of this study are available upon reasonable request from the authors.

Declarations

Compliance with ethical standards

The authors have seen all the Ethical Standards and will supposed to follow them in the future.

Consent to participate & for publication

Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

Availability of data & material

The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Conflict of interests

The authors have no relevant financial or non-financial interests to disclose.

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Authors' contribution

Rashi Mann Conceptualization, methodology, software, analysis, data curation, writing-original draft preparation.

Rishu Chaujar

Writing - review and editing at different stages, supervision.

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RESEARCH

Self-Consistent LCAO Based DFT Analysis of High-k Spacers and its Assessment on Gate-Stacked NCFET for Improved Device-Circuit Performance

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Abstract
This work investigates a Gate-Stacked negative capacitance field-effect transistor with a high dielectric material layer in the substrate region (GS-NCFET). Also, the effect of different types of spacers is taken into account. Spacers are differentiated based on their dielectric constant, i.e., GS-NCFET with no spacer is denoted as S0, with air spacer is denoted as S1, with SiO_2 specified as S2, and with HfO_2 noted as S3 device architecture. Self-consistent LCAO-based DFT analysis is done for the spacer materials in terms of band structure, PDOS, and Hartree potential. Further, the switching ratio (I_{on}/I_{off}) is discussed for S0, S1, S2, and S3. Further, the short channel effects (SCEs) like subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are extracted at drain-source voltage (V_{ds}) of 0.5 V. In addition, the voltage transfer characteristic (VTC) curve of GS-NCFET with a spacer-based inverter is considered for digital application purposes, and the transition region is drawn out for all the device architecture-based inverters. Essential parameters like propagation time delay and rise/fall time are evaluated to study the application purposes. In GS-NCFET, a dielectric layer as a buried oxide (BOX) is inserted in the substrate region to reduce the leakage current.

Keywords Negative capacitance · Gate-stacking · Propagation delay · Linearity · Short channel effects · VTC curves

1 Introduction

For almost two decades, the IT industry has been ruled by silicon-based MOSFETs because of their excellent performance, which is why they are commonly used in microprocessor chips, etc. Silicon-based MOSFETs showed their impact on research work and gave new objectives to enhance the overall device performance and minimize the size of these transistors to accommodate small chips. The challenge was fabricating these transistors with scale-down size without compromising their performance. So, researchers started working on new innovative architectures like recessed channels, dual gate technology, TFETs, etc.

One more phenomenon that has been proposed in recent years and drags the attention of researchers is the negative capacitance phenomenon. The researcher has found that the ferroelectric materials exhibit the negative capacitance phenomenon in a specific region of energy-charge curvature [1–5]. If these ferroelectric materials are used in the gate stack of the conventional MOSFET structure, the negative capacitance gives the total voltage amplification to the device as follows in the block diagram shown in Fig. 1. As this is known when applying the gate-source voltage (V_{gs}) to turn on the device, there are two charges, i.e. polarization charges (P) and screening charges (σ) which arrange themselves according to applied V_{gs}. The switching time of polarization charges (t_p) is greater than the time (t_σ) in which screening charges arrange themselves according to the V_{gs}. That is why the voltage drop across the ferroelectric material (FE) will be negative. Hence, according to the voltage drop equation of MOSFET, the total voltage across the device is amplified, as shown in Fig. 1. Due to the voltage amplification, the NCFET structure performs better than the conventional MOSFET.

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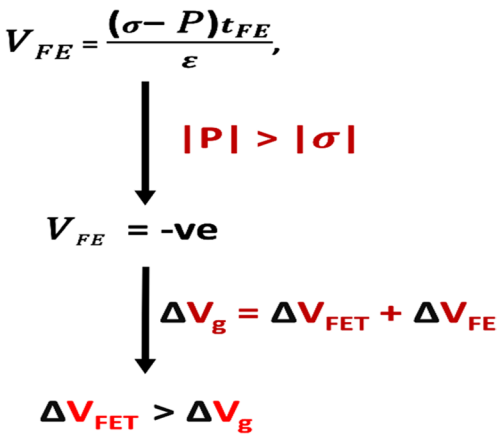


Fig. 1 Flowchart showing the voltage amplification in NCFET

In this work, we analyze the influence of several spacers on the GS-NCFET device, which features a high-k dielectric (HfO_2) gate stacking and BOX-inserted substrate. Our objective is to assess the impact of these spacers on the device's short channel effects, analog/RF parameters, and inverter-based parameters. Spacers are implemented in GS-NCFET to mitigate the gate leakage current by isolating the source and drain regions. Spacers function as insulators or dielectrics. A computation using the linear combination of atomic orbital (LCAO)-based density functional theory (DFT) is conducted for spacer materials. The study focuses on analyzing the band structure, projected density of states (DOS), and Hartree potentials of AIR spacers, SiO2 spacers, and HfO2 spacers. The effect of spacers on the GS-NCFET explores the new approaches for digital applications with improvements in circuit parameters.

2 LCAO-Based DFT Calculation for Spacers

Density Functional Theory (DFT) is a computational quantum-mechanical modelling method used to study the electronic structure of many-body systems like atoms, molecules, non-equilibrium Green's functions linked to electrical devices, and the condensed phases. The properties of many-electron systems can be determined by using a functional that is a function of another function. In DFT, electron density functional are used to investigate the structural properties. DFT calculations predict material behaviour based on quantum mechanical considerations without requiring its fundamental material properties [6–8]. Atomic modelling using the DFT supports verifying the characteristics of materials. DFT analysis using the LCAO (Linear Combination of Atomic Orbital) is done to overcome the problem of being unable to solve the Schrodinger equation for a system with more than one electron [9]. In this, the overall wave function is the superposition of individual orbitals. The spacers used in the GS-NCFET have their structural properties, so the device's application must differ. In this section of the work, the author discussed the structural properties of different materials used as spacers. One assumption is taken for this work that due to the unavailability of air molecule structure in the quantum ATK database, we investigate the structural properties of helium(k = 1.000074 at 0 °C and 1 atm), which has nearly the same dielectric constant of air (k = 1). Figure 2a, b show the crystal structure with the respective band structure of He, SiO_2, and HfO_2 in the HCP, SC, and SC lattice, respectively. The lattice parameters are taken for helium are a = 5.1156 Å, b = 5.1156 Å, c = 1.633 × a Å, α = 90°, β = 90°, γ = 120°, for SiO_2 are a = 1.25688 Å, b = 1.25688 Å, c = 1.25688 Å, α = 90°, β = 90°, γ = 90°, and for HfO_2 are a = 1.25688 Å, b = 1.25688 Å, c = 1.25688 Å, α = 90°, β = 90°, γ = 90°.

The band structure shows the electronic transitions with direct and indirect bandgap between the conduction band and valence band, which defines the actual transition probability in the material. As there is no region without the bands above the fermi energy in the case of helium band structure and the valence band top and conduction band bottom are located at the same Brillouin zone, this would behave like a conductor. In the case of SiO_2 and HfO_2, there is a region with no bands above the fermi energy level called bandgap that shows these materials' insulating properties [10]. The direct and indirect bandgap of He, SiO_2, and HfO_2 is 0 eV, 0 eV, 10.42 eV, 10.14 eV, and 2.80 eV, 2.68 eV, respectively. Also, the valence band and conduction band edge of He is at 0 eV, SiO_2 at -5.07 eV and 5.06 eV, and HfO_2 at -1.32 eV and 1.35 eV.

Further, Fig. 2c defines the projected density of states (PDOS) concerning the energy for Helium, SiO_2, and HfO_2. It gives the projection of a particular orbital of a specific atom on the density of states. So, if sum over all the projections, one will have the total density of the state, or simply, the DOS. The PDOS for helium is the highest, and for HfO_2, it is lesser, which shows a better spacer quality by enhancing the fringing of the electric field around the gate stack of the device compared to the SiO_2-spacers. Furthermore, the Hartree potential is expressed in Fig. 2d for all types of spacer materials. The Hartree potential is defined as the electrostatic potential from the electron charge density and must be calculated from the Poisson Eq. (1):

$$\nabla^2 V_H[n](r) = -4\pi n(r) \tag{1}$$

The Poisson equation is a second-order differential equation, and a boundary condition is required to fix the solution. Molecular systems have the boundary condition that the potential goes asymptotically to zero. In bulk systems, the boundary condition is that the potential is periodic. The

lower the Hartree potential, the more stable the atomic structure. Atoms take less time to move at lower potential from one orbit to another. HfO_2 has the lowest Hartree potential among all discussed materials. All discussed DFT parameters are tabulated in Table 1.

3 Device Architecture and Simulation Methodology

In this section of work, first, Fig. 3i shows the calibrated results of the Visual TCAD simulator with published results of COMSOL Multiphysics by Girish Pahwa et al.[11]. Then, we compare the device architecture of conventional NCFET and GS-NCFET) shown in Fig. 3ii. In the newly discussed architecture of NCFET, we used a high-k dielectric material (HfO_2) (k = 25) layer in the substrate region as Buried Oxide (BOX) as well as in the gate stack [12]. The device dimensions of both devices are the same as the channel length (Lg) of 25 nm, and extensions of source/drain on both sides of the channel region are taken at 10 nm. The gate stack's oxide thickness is fixed at 1 nm (0.5 nm SiO_2 + 0.5 nm HfO_2). The substrate region is doped with a uniform p-type of 1×10^{16} cm^{-3} concentration. The source/drain region is heavily n-type Gaussian doped with 1×10^{20} cm^{-3} concentration. The thickness of high-k dielectric in the substrate region is kept at 5 nm.

Further, Fig. 4 shows the channel region of GS-NCFET with the attachments of different types of spacers. S0 denotes the GS-NCFET without the spacers, S1 denotes the GS-NCFET with 5 nm length air (k = 1) spacers around the gate stacking, S2 specifies the GS-NCFET with 5 nm length SiO_2 (k = 3.9) spacers around the gate terminal and S3 shows the GS-NCFET with 5 nm length HfO_2 (k = 25) spacers around the gate terminal [13]. In addition, device methodology includes the FE layer set down on the gate dielectric of the baseline MOSFET. The polarization direction of the FE material is parallel to the gate stack. Visual Technology-Computer-Aided-Design (VTCAD) is capable of solving the Landau-Khalatnikov (L-K) equations of electric field used for the FE layer as a function of polarization (P) given as Eq. (2):

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\langle\frac{dP}{dt}\rangle \tag{2}$$

with Poisson's Equation and other physical models like impurity scattering, mobility degradation due to surface roughness scattering, and phonon scattering, which are specific to scaled devices. As the quantum mechanical confinement can be modelled and stabilized by changing the gate work function and oxide thickness, it is not assumed for the simulation work. The viscosity coefficient (ρ) and the domain interaction coefficient (g) in the L-K equation are 0.18 Ωcm and 10^{-10} m^3/F, respectively.

By using the doping technique in HfO_2-based FE, the coercive field (E_C) and remnant polarization (P_r) of 1 MV/cm and 6 μC/cm^2 are achieved, corresponding to L-K constants $\alpha = -2.165\times10^{11}$ cm/F, $\beta = 3.007\times10^{21}$ $cm^5/(FC^2)$, $\gamma = 0.000$ cm^9/FC^4. The basic DDML1 equations followed by the simulators are given in Eqs. (3a), (3b), and (3c).

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n E_n + \mu_n \frac{k_b T}{q}\nabla n) - (U - G) \tag{3a}$$

$$\frac{\partial p}{\partial t} = -\nabla.\left(\mu_p p E_p - \mu_p \frac{k_b T}{q}\nabla p\right) - (U - G) \tag{3b}$$

$$\nabla.\varepsilon\nabla\Psi = -q(p - n + N_D^+ - N_A^-) \tag{3c}$$

where Ψ is the electrostatic potential of vacuum level, the concentration of electron and hole is noted by n and p, respectively, $N_D^+ and N_A^-$ defines the ionized impurity concentrations, and q is the electron charge magnitude. E_n and E_p are the effective driving electrical field for electrons and holes. μ_n and μ_p are mobilities of electrons and holes, respectively. U is the recombination rate, and G is the generation rate of both electrons and holes. All other symbols have their specific standard meanings. All other S0, S1, S2, and S3 regions are identical. Simulation work for all the device architectures is carried out on the VISUAL TCAD simulator. All comparison parameters are done on the $V_{ds} = 0.5$ V.

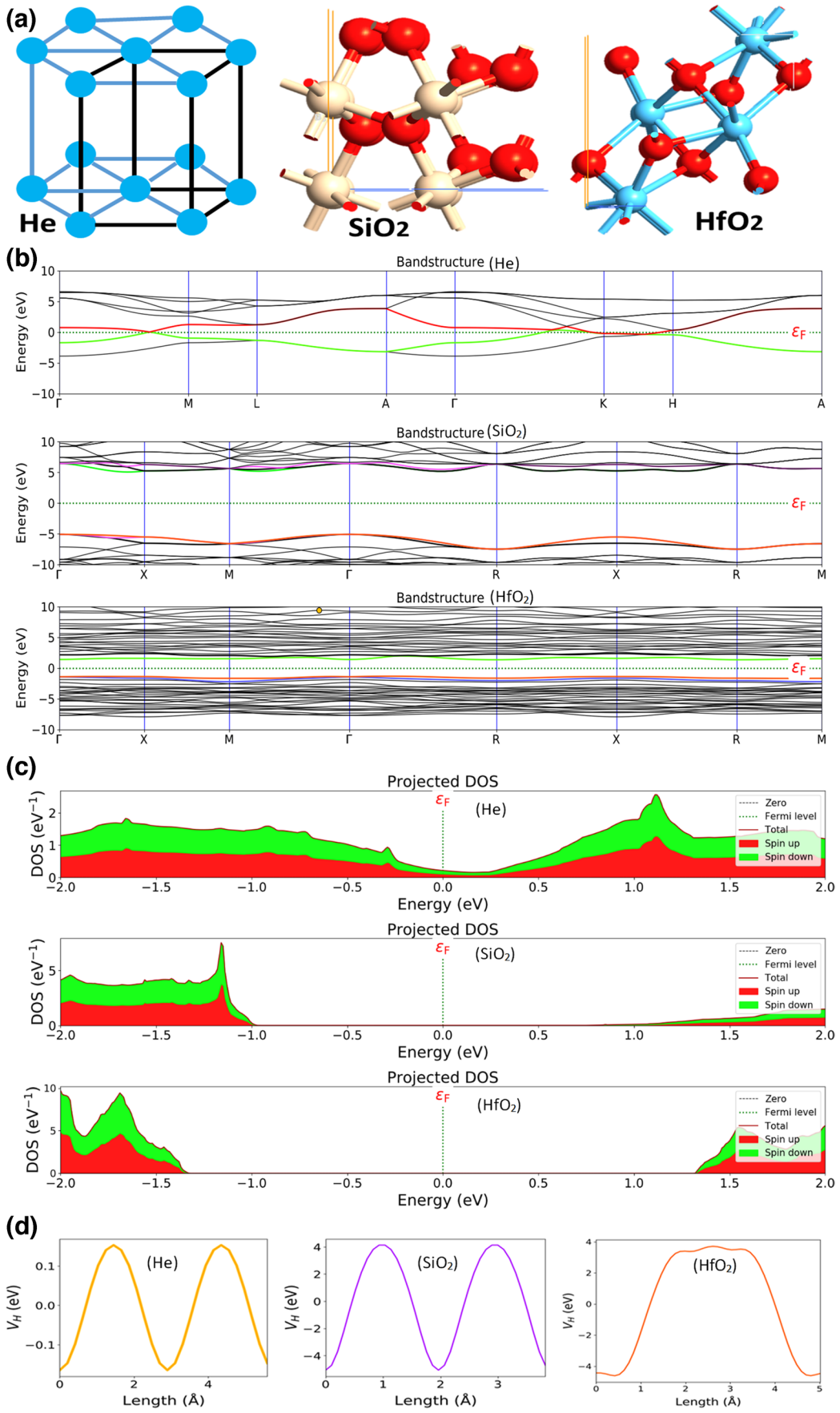
4 Results and Discussions

4.1 Comparison of Conventional NCFET and GS-NCFET

In this work section, we discuss the improvement factor of GS-NCFET over the conventional NCFET, followed by the effect of different spacers on the GS-NCFET. Figure 5 shows the transfer characteristics of conventional NCFET and GS-NCFET at constant drain-source voltage, $V_{ds} = 0.5$ V, which shows GS-NCFET has higher on-current and lower leakage current, explaining the improved behaviour of GS-NCFET.

4.2 Effect of Spacers on Switching Profile and SCEs of GS-NCFET

Figure 6a shows the comparison of on-current for S0, S1, S2, and S3. S0 has the lowest on-current and increases as the dielectric constant of the spacers increases, i.e. S1, S2, and S3. Also, the leakage current starts decreasing in the same trend shown in Fig. 6b. The reason for the trend is



◂**Fig. 2** **a** Atomic structure **b** Band structure **c** PDOS **d** The Hartree potential corresponding to He (assumed Air molecule), SiO2, and HfO2

that the spacers insulate the source and drain region from the gate terminal, which diminishes the gate leakage current and significantly increases the switching ratio of a particular device [13–17]. Another explanation for this trend is the enhancement in the fringing of the electric field due to the application of high-k dielectric constant spacers, i.e. SiO_2 and HfO_2. Thus, it reduces the effective gate voltage that lowers the transverse electric field responsible for carrier tunneling through the gate oxide.

This insulation increases as the dielectric constant of the spacer increases. Here, the Air spacer has the lowest dielectric constant value, 1, and HfO_2 has the highest dielectric constant value (k = 25). So, the S3 has the highest switching ratio, as verified by Fig. 6c. Furthermore, when the L_g is in the same order of magnitude as the width of the depletion layer, then the MOSFET device is considered to have SCEs. However, at the cost of these SCEs, operation speed and number of components per chip increase. Because of SCEs, two physical phenomena are attributed. One is the limitation imposed on electron drift characteristics in the channel, and the other is modifying the threshold voltage. Two specific SCEs are SS and DIBL [18, 19]. Figure 7a shows the V_{th} and DIBL variation with the different types of spacers. The variation shows the decreasing value of V_{th} and DIBL as the dielectric constant of spacers increases, i.e. S0, S1, S2, and S3.

The device S0 has the maximum value of V_{th} and DIBL and starts decreasing for S1, S2, and S3. DIBL is calculated as formulated in Eq. (4a). Reduced DIBL further minimizes the threshold voltage roll-off problem. The drain coupling to the channel through gate dielectric and spacer reduces as the spacer-k value increases. As discussed in the previous section, the high-k spacers enhance the fringing electric field, directly giving better control over the junction depletion region near the drain side, thus reducing the DIBL effect. In addition, the SS variation in linear and saturation for S0, S1, S2, and S3 is shown in Fig. 7b.

The SS value in both regions shows a decreasing trend as we move from S0 to S3. SS in the linear region is extracted at $V_{gs} = 0.1$ V, SS in the saturation region is extracted at $V_{gs} = 1$ V, and V_{ds} are kept constant at 0.5 V. Subthreshold swing defines the required gate-source voltage to change the drain current by one decade.

It is clear that the threshold voltage for GS-NCFET with HfO_2 spacer, i.e. S3, has the lowest value. So, the SS value for the S3 is also the lowest and approaches the standard Boltzmann tranny limit, which is 60 mV/dec. S0 has the maximum SS value, and S1 and S2 show the decrement values and can be extracted as given in Eq. (4b).

$$\text{DIBL} = \frac{\partial V_{th}}{\partial V_{ds}} \tag{4a}$$

$$\text{SS} = \frac{\partial V_{gs}}{\partial log I_D} \tag{4b}$$

This variation in SS shows better gate control to channel due to the assistance of high-k dielectric spacers. The higher driving current and lower leakage current achieved using the high-k dielectric spacer effectively enhance the device's performance and reduce power dissipation. As we know the multigate structures exhibit a good immunity against the short channel and degradation effects in comparison to single-gate FETs. In this case, the immunity to short-channel effects in single-gate FETs is achieved through a combination of material advancements, device structure optimization, and innovative designs, allowing for continued scaling of transistor dimensions and improved performance in integrated circuits. The device structure can be optimized to minimize the influence of the drain on the channel. For example, by introducing lightly doped drain (LDD) regions or using halo doping techniques, the electric field at the drain/channel interface can be reduced, mitigating DIBL [20].

4.3 RF/Analog Parameters of Spacers-Based GS-NCFET

Analog parameters like transconductance (g_m) and transconductance generation factor (TGF) are discussed for S0, S1, S2, and S3. Figure 8a shows the g_m variation concerning the gate-source voltage at constant $V_{ds} = 0.5$ V. The curve shows that the peak values of g_m are highest for S3 and lowest for S0. Transconductance is defined by the formula given in Eq. (5a).

It depends on the change in drain current with the change in gate-source voltage. Also, Eq. (5b) formulates the TGF of a device. With this help, we can explain the values of TGF shown in Fig. 8b. The standard value of TGF is 40 V^{-1}, and as we move from S0 to S3, the TGF value increases and approaches the standard value (40 V^{-1}).

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \tag{5a}$$

$$\text{TGF} = \frac{g_m}{I_D} \tag{5b}$$

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{5c}$$

Table 1 Brief DFT parameters values of helium, silicon oxide, and hafnium oxide

DFT Parameter		Helium (He)	Silicon Dioxide (SiO_2)	Hafnium Oxide (HfO_2)
E_g (eV)	Direct E_g	0	10.42	2.80
	Indirect E_g	0	10.14	2.68
Peak PDOS (eV^{-1})		2.5	8.2	10
V_H (V)		0.14	4	4.1

$$V_{EA} = \frac{I_D}{g_d} \tag{5d}$$

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5e}$$

Further, Output conductance (g_d) measures the variation of I_d concerning the variation of V_{ds} with constant V_{gs} explicit Fig. 8c. It is an essential parameter for device performance as it decides the drive current for a device formulated as Eq. (5c). For better device performance, it should be low as it is the reciprocal of output resistance, which should be high for less power loss [21–25]. In this work, authors observed minimum output conductance for S3 having a high-k dielectric constant spacer and followed the increasing trend with S2, S1, and S0. Another FOM for analog application is early voltage, shown in Fig. 8d. According to the plot, the GS-NCFET with HfO_2 spacers, i.e., S3 has the highest V_{EA} value of 5 V for 0.95 V of $V_{gs,}$ and S0 has the minimum value of early voltage of around 3 V at 0.95 V of V_{gs}. Early voltage is a parameter to characterize the output resistance and is the inverse of the channel length modulation parameter. It can be extracted as formulated in Eq. (5d).

Moreover, Fig. 8e and Eq. (5e) explain the cut-off frequency variation for the different types of spacers. f_T defines the frequency value when the current gain is unity, and it is the most important parameter for evaluating the RF application of a device. GS-NCFET with HfO_2 spacers (S3) has the highest f_T value among S0, S1, and S2, which shows that RF application is better for this device.

4.4 Effect of Spacers on Linearity Parameters of GS-NCFET

Figure 9a gives the combined plots of peak values of GBP and GFP concerning the different types of spacers. The gain bandwidth product (GBP) and gain frequency product (GFP) are extracted for device architecture at $V_{gs} = 0.5$ V and $V_{ds} = 0.5$ V and formulated as Eq. (6a) and (6b).

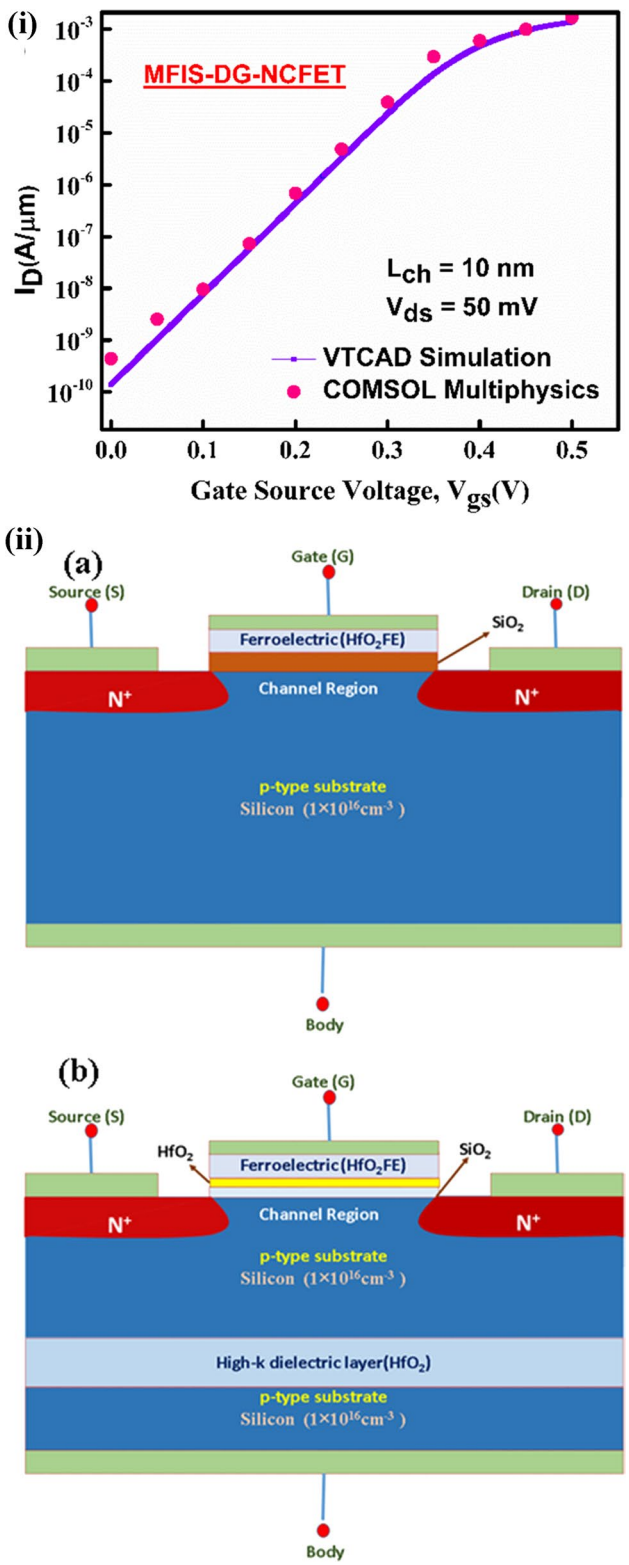


Fig. 3 **i** Calibration of VTCAD simulation with COMSOL Multiphysics and **ii** Device architecture of (**a**) conventional NCFET and (**b**) GS-NCFET

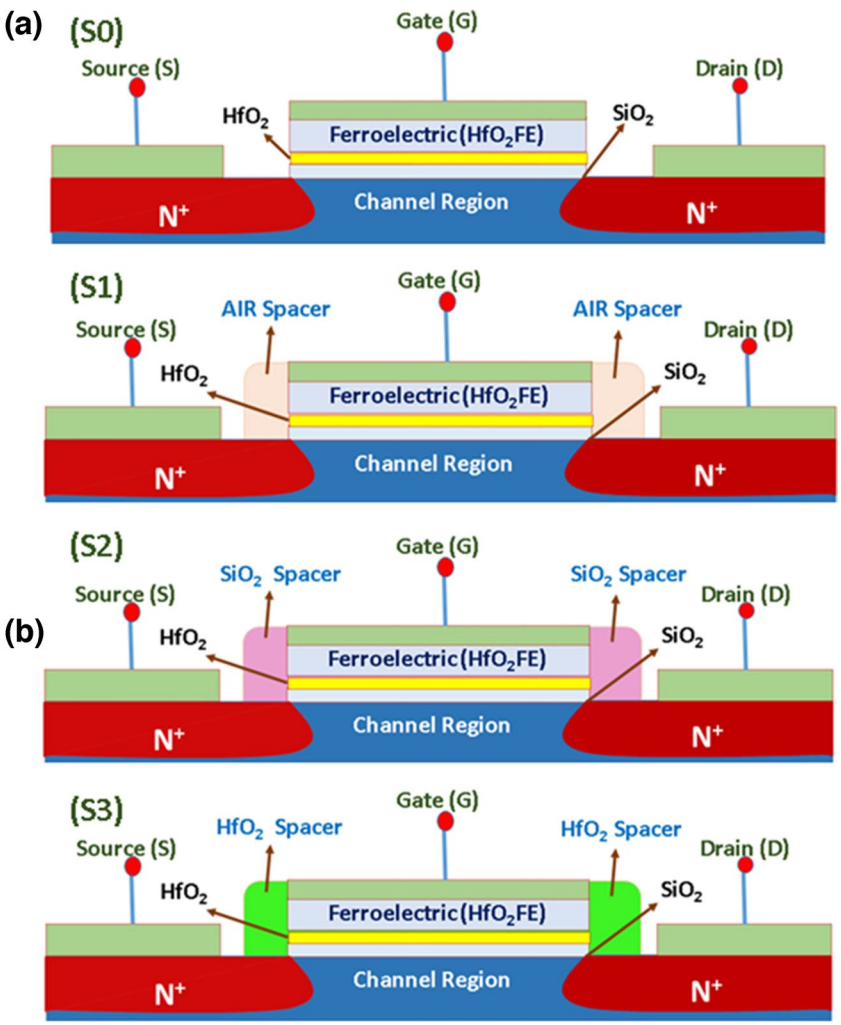


Fig. 4 GS-NCFET with no spacer (S0) Air spacer (S1) SiO_2 spacer (S2) HfO_2 spacer (S3)

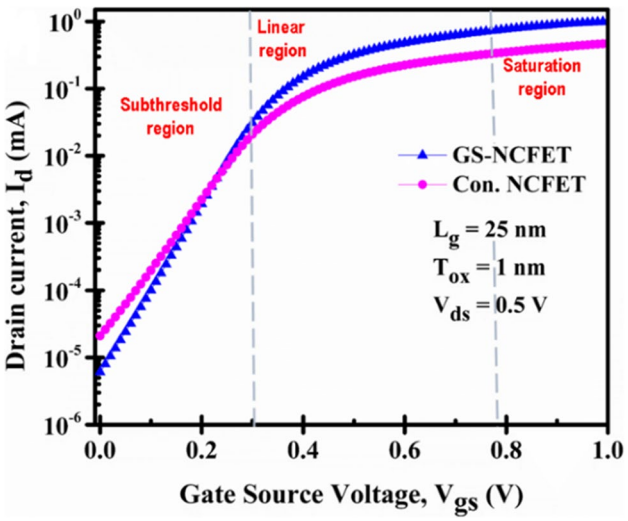


Fig. 5 Transfer characteristics of conventional NCFET and GS-NCFET

$$GBP = \frac{g_m}{20\pi C_{ds}} \tag{6a}$$

$$GFP = \frac{g_m}{g_d} f_T \tag{6b}$$

$$TFP = \frac{g_m}{I_d} f_T \tag{6c}$$

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_d} f_T = \frac{g_m}{g_d} \times TFP \tag{6d}$$

$$g_{m2} = \frac{\partial^2 I_d}{\partial^2 V_{gs}^2} \tag{6e}$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3} \tag{6f}$$

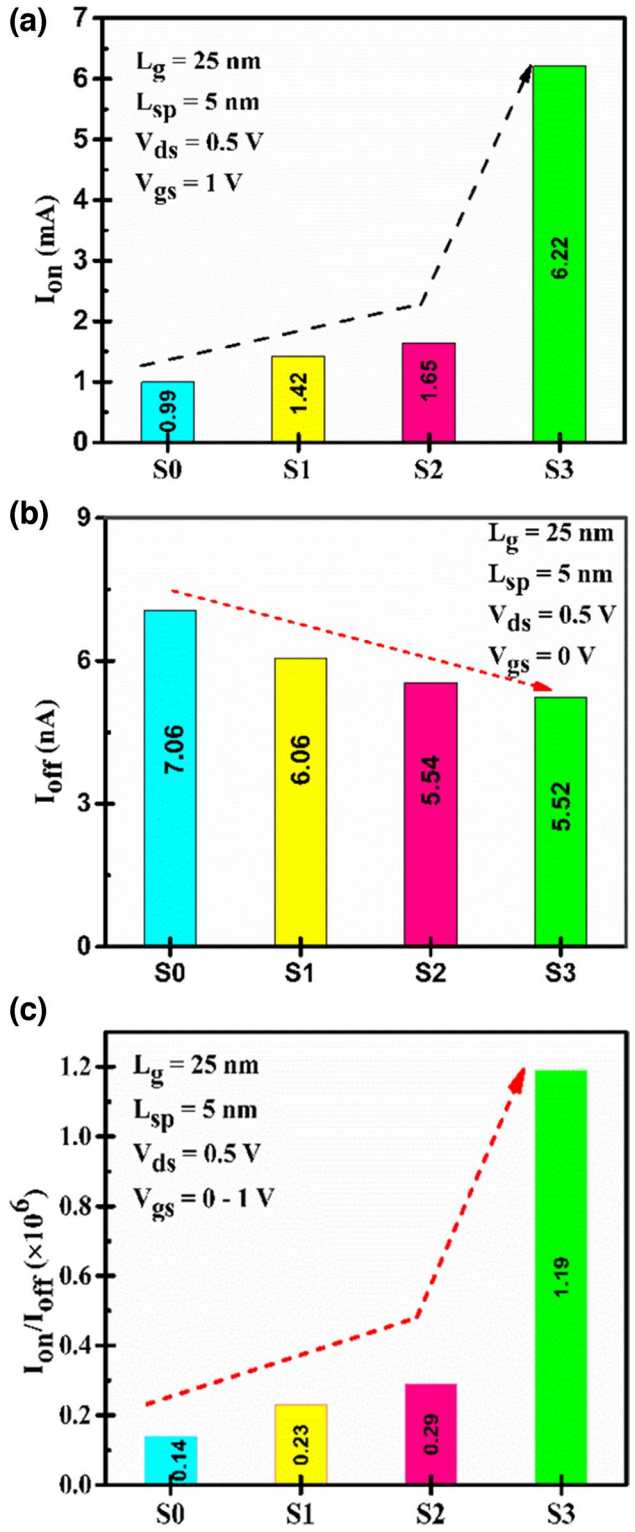


Fig. 6 **a** I_{on} current **b** I_{off} current **c** Switching ratio (I_{on}/I_{off}) comparison of S0, S1, S2, and S3

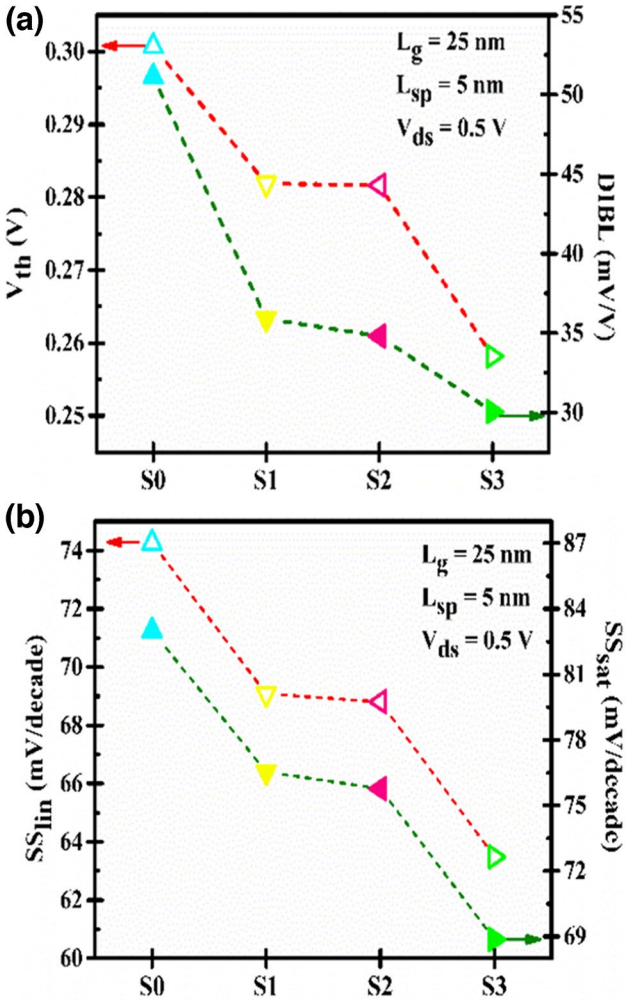


Fig. 7 **a** The V_{th} and DIBL **b** SS in linear and saturation regions for S0, S1, S2, and S3

The parasitic capacitance C_{gd} (gate-to-drain capacitance) is lower in the case of S3 among other architectures, which is why the ratio of transconductance to C_{gd} is higher for GS-NCFET with HfO_2 spacers (S3) than S0, S1, and S2.

Further, in the same Fig. 9a, a variation of GFP for all types of spacer devices is shown. Due to the lower value of (g_m/g_d), the total value of GFP of S3 is lesser than S0, S1, and S2. Furthermore, Fig. 9b and Eq. (6c) describe the variation of the transconductance frequency product (TFP) concerning V_{gs}. As TGF is high for S3, the TFP value of S3 is also the highest among all S0, S1, and S2. Hence, the gain transconductance frequency product (GTFP) is also higher for S3 than S0, S1, and S2, described in Fig. 9c and Eq. (6d). In addition, the linearity parameters like second-order transconductance (g_{m2}) and third-order transconductance (g_{m3}) are shown in Fig. 9d, e, respectively. The main reason for non-linearity in RFICs is the non-linearity of devices, as it produces intermodulation and higher-order

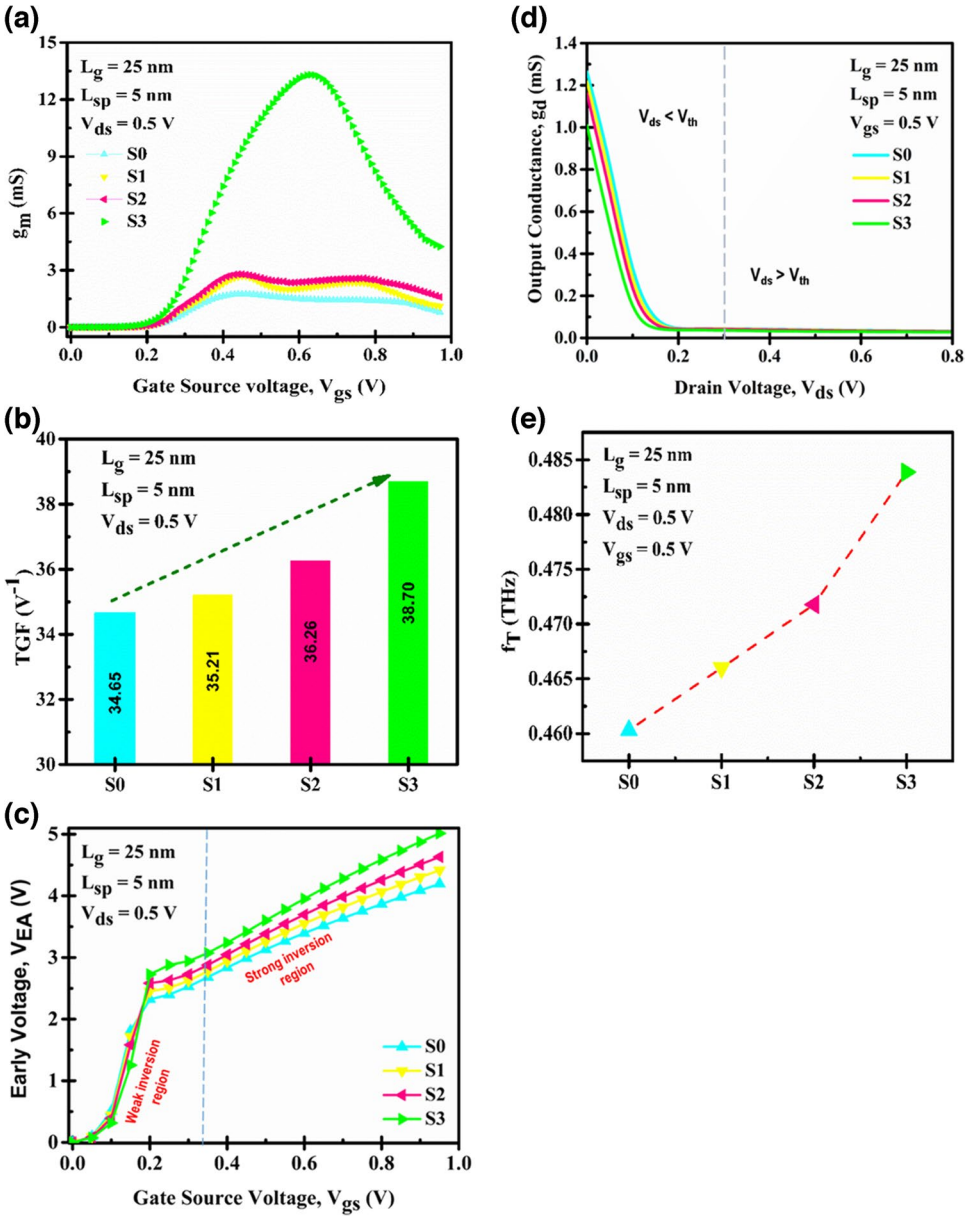


Fig. 8 The **a** g_m **b** TGF **c** g_d **d** V_{EA} **e** f_T curves of GS-NCFET with different types of spacers

harmonics in analog/RF circuits. These are responsible for wastage in output power [12, 26–29]. Therefore, minimization of these distortions is a must objective to do. The variation of these parameters is extracted according to Eq. (6e) and (6f); extracted g_{m2} and g_{m3} of S3 are lowest compared to S0, S1, and S2, which shows the better linearity of a device.

4.5 Effect of Spacers on Parameters of GS-NCFET-Based Inverter

Figure 10a demonstrates the GS-NCFET-based inverter schematic. This expresses the requirement for two types of GS-NCFET, n-channel and p-channel, to work correctly without any delay. Figure 10b shows the VTC characteristics of the GS-NCFET-based inverter [30–33]. Four curves show the corresponding spacer-based inverter plot lines. From the curves, one can conclude that the transition region from high to low output is minimal for the S3-based inverter, which shows the maximum noise margin for the particular circuit. On the other hand, the transition region decreases for S0, S1, and S2 with an increased dielectric constant value, respectively. Further, Fig. 10c describes the propagation delay low-to-high (t_{pLH}) (and high-to-low (t_{pHL})), which is the delay when output switches from low-to-high (and high-to-low) after input switches from high-to-low (low-to-high). The delay is commonly calculated at 50% input-output switching. The speed of logic is defined by the propagation delays. A typical complex system has 20–50 propagation delays per clock cycle. Total propagation delay is calculated with the mean of t_{pHL} and t_{pLH} shown as in Eq. (7)

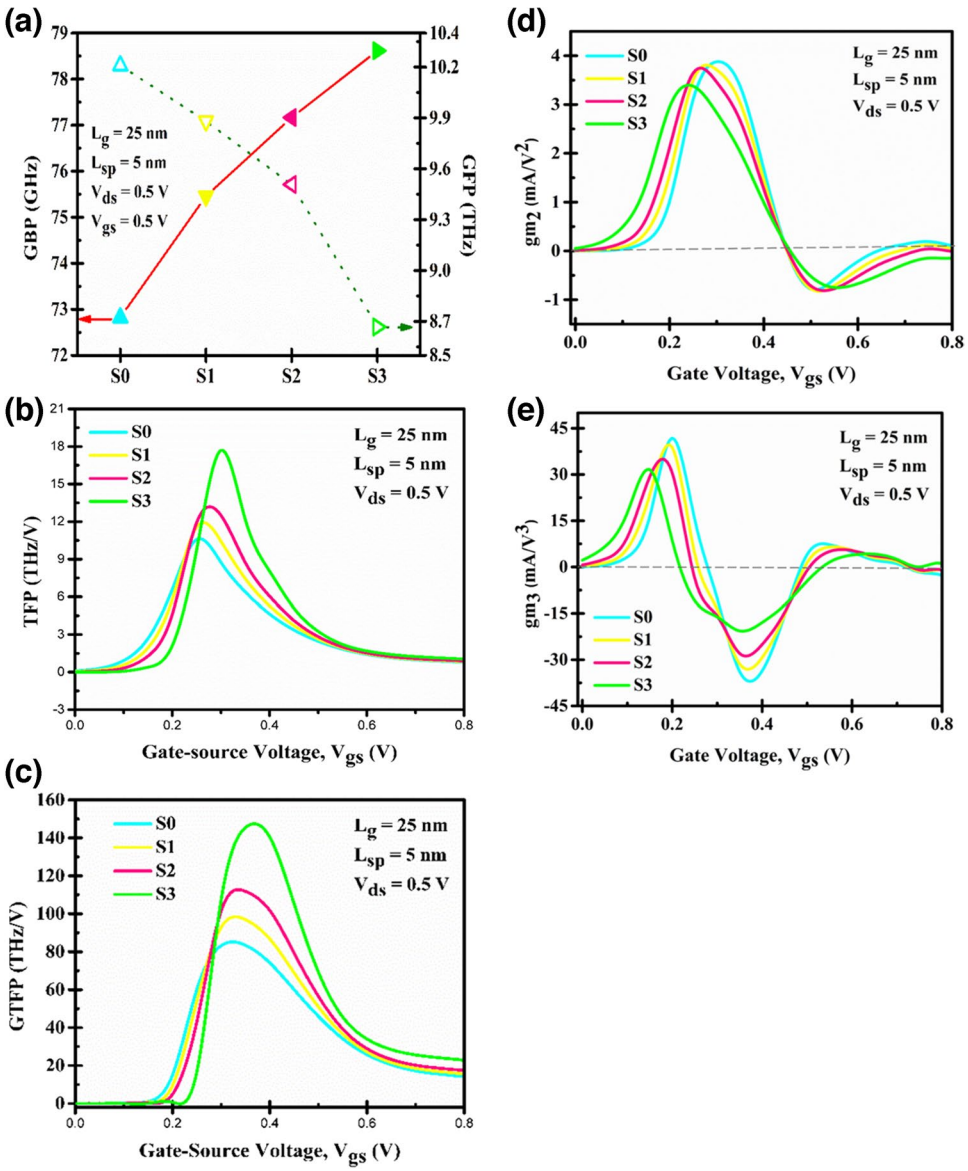


Fig. 9 **a** GBP and GFP **b** TFP **c** GTFP **d** g_{m2} **e** g_{m3} corresponds to different types of spacers

$$t_p = \langle \frac{t_{pHL} + t_{pLH}}{2} \rangle \tag{7}$$

Further, Fig. 10d shows the rise (t_r) and fall time (t_f) for concerned device structures, which shows that both parameters have the minimum value for GS-NCFET with HfO_2 spacers, i.e., S3. Rise time (t_r) is defined as the time during a transition when the output switches from 10 to 90%, and fall time (t_f) is referred to as the time taken by the output waveform to switch from 90 to 10% [34].

So, it is concluded that the GS-NCFET with HfO_2 spacer is a good option for digital applications.

A comparison Table 2 is given to compare this work with the other published works.

5 Conclusion

This paper section concludes that GS-NCFET with HfO_2 spacer shows improved results compared to other spacers like air and SiO_2. LCAO-based DFT analysis shows the characteristics of different types of spacers. Maximum PDOS is observed for the HfO_2 spacer with minimum hartree potential. The band structure shows the allowed transactions

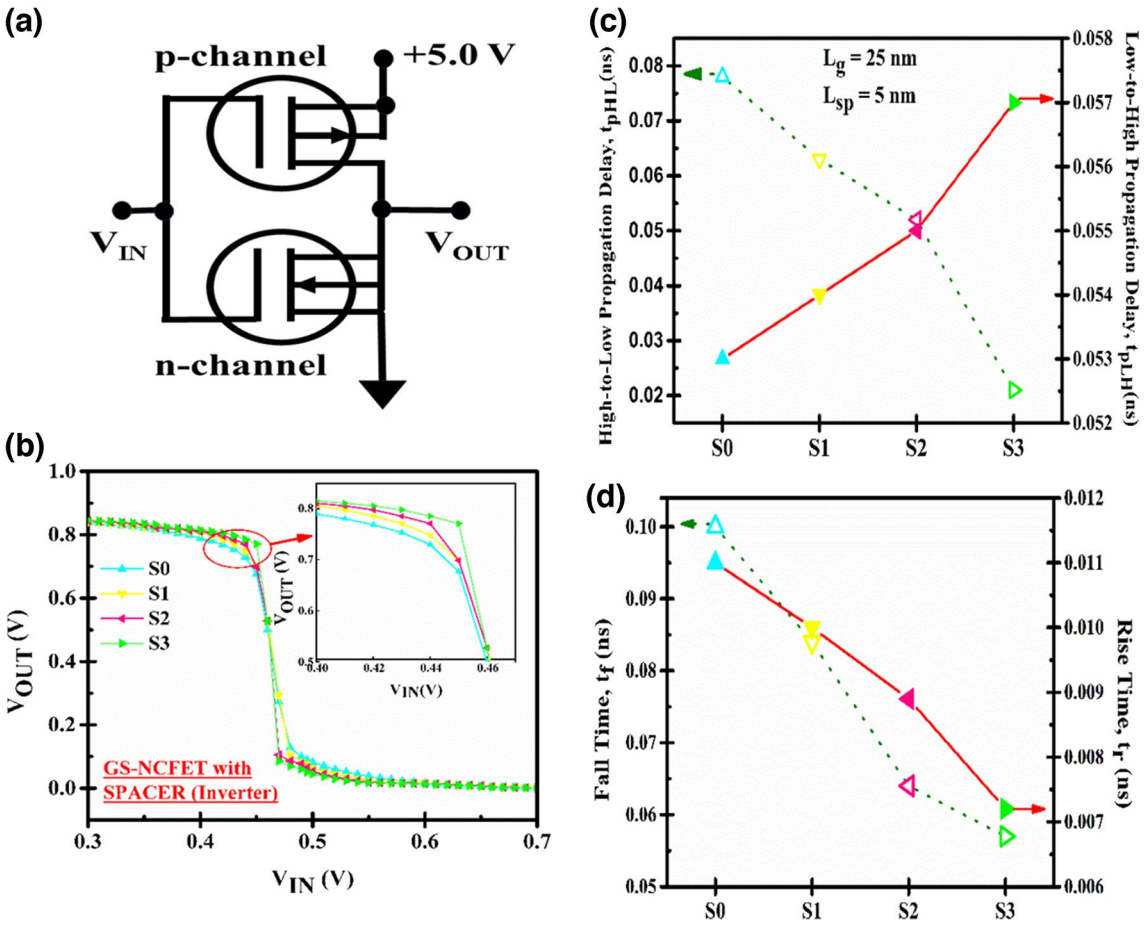


Fig. 10 **a** Schematics of GS-NCFET-based inverter **b** VTC curve **c** propagation delay **d** rise time and fall time of GS-NCFET-based S0, S1, S2, and S3 inverters

Table 2 Comparison of GS-NCFET parameters with other published work

Ref	Year	Device platform	I_{on}/I_{off} ($\times 10^5$)	TGF (V^{-1})	A_v (dB)	V_{EA} (V)	f_T (THz)
[35]	2019	Junctionless Double Gate Vertical MOSFET	NA	26.7	NA	0.59	0.083
[36]	2020	Nano-sheet Transistor	1.90	NA	6.03	2.67	0.585
[37]	2021	SOI Junctionless Nanowire FET	0.82	41.81	NA	NA	0.254
[38]	2022	Tunnel Field Effect Transistor	NA	4.39	0.93	NA	0.940
This work	-----	GS-NCFET(S0)	20.4	91.49	0.65	4.19	NA

for the electrons. The leakage current of S3 is reduced by 25.92% to S0, and the switching ratio is increased by three decimal points.

Further, the threshold voltage and DIBL value of S3 decreased by 16.66% and 41.17%, respectively, compared with S0. The SCEs of S3, like SS in linear and saturation, reduced by 14.58% and 17.02% compared to the S0 device architecture. Furthermore, g_m, TGF, g_d, V_{EA}, and f_T improved multiple times more than other device architectures like S0, S1, and S2. Moreover, the linearity parameters like g_{m2} and g_{m3} were minimized in the case of GS-NCFET with HfO_2 spacers. In addition, the VTC characteristics of GS-NCFET are discussed for all types of spacers, and S3 shows the minimum transition region than other device architecture with a 42.85% decrement and better propagation delay with less t_r and t_f. So, the work concludes that the GS-NCFET with HfO_2 spacer is a reliable candidate for digital application.

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Author Contributions **Rashi Mann**: Conceptualization, methodology, software, analysis, data curation, writing-original draft preparation.

Rishu Chaujar: Writing—review and editing at different stages, supervision.

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Data Availability The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Declarations

The authors have seen all the Ethical Standards and will supposed to follow them in the future.

Consent to Participate & for Publication Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

Competing Interests The authors declare no competing interests.

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