Design and Implementation of Immittance Circuits Using Active Building Blocks

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by

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CANDIDATE'S DECLARATION

I **Navnit Kumar** hereby certify that the research work, which is being presented in the thesis, entitled **Design and Implementation of Immittance Circuits Using Active Building Blocks** in partial fulfillment of requirements of the award of the degree of Doctor of Philosophy, submitted in the Department of **Electronics and Communication,** Delhi Technological University is an authentic record of my own work carried out during the period from **August 2020** to **November 2024** under the supervision of **Dr. Manjeet Kumar** and **Prof. Neeta Pandey**.

The matter presented in the thesis work has not been submitted by me for the award of any other degree or any other Institute.

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Certified that Navnit **Kumar (enrollment no. 2K20/PHDEC/07)** has carried out their search work presented in this thesis entitled "**Design and Implementation of Immittance Circuits Using Active Building Blocks"** for the award of **Doctor of Philosophy** from Department of Electronics and Communication Delhi Technological University, Delhi, under our supervision. The thesis embodies results of original work, and studies are carried out by the student himself, and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

The discipline of analog signal processing has experienced significant growth and development during the past few decades. The literature describes a variety of voltage-mode and current-mode active components for carrying out analog signal processing tasks. Nevertheless, the analog signal processing circuits in the current domain offers advantages such as enhanced bandwidth, less circuit complexity, expanded dynamic, low power consumption, and high speed. Therefore, the current-mode approach is widely recognized as a viable alternative to conventional voltage-mode circuits.

The immittance circuits have numerous applications in microelectronics, communication, analog signal processing, instrumentation, and measurement. There are limitations of realizing traditional components namely inductor and resistor in microelectronics circuits, such as occupying significant chip space, being heavy, expensive, and lacking tunability. It makes the active immittance circuits, a prominent area of study. This thesis deals with design of immittance emulators and their applications.

A variety of integer order immittance emulators have been developed in the literature. However, there is a lean presence of emulators that simultaneously fulfil the following criterions: tunability, no matching constraint, less components, low power consumption, low chip area, and working in positive and negative mode without topological changes. In addition, it is pertinent to mention here that to obtain positive and negative modes the topological change is not possible once the circuit is laid down and fabricated. Also, if two different circuits are realized in IC form for positive and negative immittances, the resulting silicon footprint would require more. Hence, Current Conveyor Transconductance Amplifier (CCTA) based a grounded and floating immittance emulators are developed that provides both positive and negative immittances through appropriate setting of MOS switches. The proposed topology does not require any component matching, thus making it suitable for integration viewpoint. Further, these immittance emulators are tuned electronically via bias current of CCTA. The proposed immittance circuit is used to implement the fifth order low pass filter, and capacitance cancellation circuit.

Nowadays, fractional order circuits gain considerable attention among researchers due to the extra degree of freedom to control the phenomena of the system. The fractional order inductor circuits reported in literature are limited in terms of large number of active and passive components, tunability, slew rate, operating frequency, and high-power dissipation. Hence, Operational Transconductance Amplifier (OTA) based electronically tunable grounded and floating fractional order inductor circuits are also developed. These circuits can flip between positive and negative modes without modifying their architecture. The usefulness of the proposed positive fractional inductor circuit is demonstrated through fractional order band pass filter and fractional order high pass ladder filter. The usefulness of the proposed negative fractional inductance circuit is demonstrated through a fractional inductance cancellation circuit.

The synthetic transformer (ST) circuit or Mutual Coupled Circuit (MCC) is yet another application of immittance circuit. It is frequently used in circuits for instrumentation, measurement, analog communications, and signal processing. It is observed that MCC circuit featuring mutual inductance in four different pairs like passive transformer is not available in open literature. To fill this gap, a CCTA based tunable floating MCC is designed which can be configured in four different pairs of mutual coupled circuits through appropriate setting of MOS switches. The proposed MCC does not require component matching condition. Self-inductance, mutual inductance, and resonant frequency can be tuned by bias current of CCTA. A double tuned band pass filter is shown as an application.

Furthermore, memristor is the fourth fundamental element in circuit theory after resistor, capacitor, and inductor. It is gaining considerable attention among researchers due to its high-density storage property. It is a non-linear device provides relation between electric charge (q) and magnetic flux (φ). A solid state memristor is not available in the market due to its high price and difficult manufacturing process. Hence, charge and flux controlled memristor emulators are developed employing Inverting Current Conveyor Transconductance Amplifier (ICCTA). In addition, both proposed circuits do not include intricate components such as analog multiplier circuits, passive inductors, and analog to digital converter circuits in their design, which is beneficial in terms of integrated circuit implementation point of view. Further, the effectiveness of the developed circuits is validated using meminductor circuits, and memristor-based active filters.

The behavior of the proposed circuits is analyzed in the presence of parasites that may appear in practice. The operation has been examined through SPICE simulations and post-layout simulations are also included in the thesis. Corner and Monte-Carlo analysis is performed to assess the robustness of the various proposals.

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ABBREVIATIONS & NOTATIONS

OTA	Operational Transconductance Amplifier
CCII	Second-Generation Current Controlled Conveyor
CCCII	Second-Generation Current Controlled Current Conveyor
OTRA	Operational Trans resistance Amplifier
CFOA	Current Feedback Operational Amplifier
CDBA	Current Differencing Buffered Amplifier
DDCC	Differential Difference Current Conveyor
VDTA	Differential Difference Current Conveyor
VDCC	Voltage Differencing Current Conveyor
CBTA	Current Backward Transconductance Amplifier
DVCC	Differential Voltage Current Conveyor
DXCCTA	Dual-X Current Conveyor Transconductance Amplifier
CFTA	Current Follower Transconductance Amplifier
CDBA	Current Differencing Buffered Amplifier
DVCC	Differential Voltage Current Conveyor
CDTA	Current Differencing Transconductance Amplifier
MO- CCCCTA	Multiple Output Current Controlled Current Conveyer Transconductance Amplifier
ZC-VDCCC	Z-Copy Voltage Differencing Current Conveyor
DDCCTA	Differential Difference Current Conveyor Transconductance Amplifier
VD-DIBA	Voltage Differencing Differential Input Buffered Amplifier
CCTA	Current Conveyor Transconductance Amplifier
CC-CFA	Current Controlled Current Feedback Amplifier
VDBA	Voltage Differencing Buffered Amplifier
VDIBA	Voltage Differencing Inverting Buffered Amplifier
CFCC	Current Follower Current Conveyor
MDVCC	Modified Differential Voltage Current Conveyor

DXCCDITA	Dual-X Current Conveyor Differential input Transconductance Amplifier
VCII	Second Generation Voltage Conveyor
DO-DVCC	Dual Output Voltage Differential Current Conveyor
MCFOA	Modified Current Feedback Operational Amplifier
MICCI	Minus-Type Modified Inverting First-Generation Current Conveyor
DXCCII	Second-Generation Dual-X Current Conveyor
VCG-CCII	Voltage and Current Gained Second Generation Current Conveyor
D0-CCII	Dual Output Second-Generation Current Controlled Current Conveyor
DDCCTA	Differential Difference Current Conveyor Transconductance Amplifier
MDO-DDCC	Modified Dual Output Differential Difference Current Conveyor
MVDVTA	Modified Voltage Differencing Voltage Transconductance Amplifier
CC-CFA	Current Controlled Current Feedback Amplifier
VDDDA	Voltage Differencing Differential Difference Amplifiers
FTFNTA	Four Terminal Floating Nuller Transconductance Amplifier
DVTCC	Differential Voltage to Current Converters
MICCII	Modified Inverting Second-Generation Current Conveyor
PFTFN	Positive Four Terminal Floating Nuller
ZC-CCCITA	Z-Copy Current Controlled Current Inverting Transconductance Amplifier
OTRA	Operational Transresistance Amplifier
ICFOA	Inverting Current Feedback Operational Amplifier
CCDDCC	Current Controlled Differential Difference Current Conveyor
CCIIITA	Third Generation Current Conveyor Transconductance Amplifier
ICCII	Inverting Second Generation Current Conveyor
DVB	Differential Voltage Buffer
CFDITA	Current Follower Differential Input Transconductance Amplifier
FDNR	Frequency Dependent Negative Resistance
WDA	Weighted Differential Amplifier
WAA	Weight Adder Amplifier

IInV	Inverting Integration Circuit
IWAA	Inverting Weighted Adder Amplifier
ICCTA	Inverting Current Conveyor Transconductance Amplifier
Op-amp	Operational Amplifier
ABB	Active Building Blocks
MCC	Mutually Coupled Circuit
ST	Synthetic Transformer
GIC	General Impedance Convertor
VCR	Voltage-Controlled Resistor
DVCCTA	Differential Voltage Current Conveyor Transconductance Amplifier
VIM	Voltage Inverting Mutator
LDR	Light Dependent Resistor
DTBPF	Double Tuned Band Pass Filter
PHL	Pinch Hysteresis Loop
THD	Total Harmonic Distortion
g_m	Transconductance
μ_n	Electron Mobility
C_{ox}	Gate Oxide Capacitance Per Unit Area
C_α	Fractional Order Capacitor
I_O	Inverter
L_α	Fractional Order Inductor
I_B	Bias Current
Q	Quality Factor
k	Coupling Coefficient
ω_O	Resonant Frequency

CHAPTER 1
INTRODUCTION

1 Introduction

The signals appearing in real life are analog in nature which makes analog signal processing a niche area. Though the thrust is towards digitization of the signal processing, the circuits specially oscillators, rectifiers, amplifiers, analog to digital converters (A/D), and digital to analog converters (D/A) are going to stay and cannot be realized digitally. To elaborate this further, analog signal generated by microphones and other acoustic transducers are appropriately conditioned throughout this procedure utilizing amplifiers and filters. They are then transformed to digital format to allow for further activities such as mixing, editing, and creating special effects. Additionally, digital signals are used for important operations such as transmission, storage, and retrieval. Finally, digital information is converted into analog signal that are transmitted through loudspeakers. The physical environment is ultimately analog, which means that analog circuitry will always be required to modify physical signals, such as those generated by transducers. As a result, analog designers are expected to create interfaces that have superior performance and are compatible with digital circuits to the greatest extent possible. In modern times, VLSI technology has the capability to incorporate millions of transistors into a compact single chip. Further, with scaling down of geometries, it becomes necessary to operate the circuits at reduced supply voltages. The operation of analog circuits at low power supply presents several challenges e.g. decrease in input common mode range, output swing, and linearity. Moreover, it is preferable to use low voltage circuit techniques that are compatible with normal CMOS processes to avoid this clash rather than expensive CMOS technologies with lower thresholds.

The information processed by electronic circuits may be represented by branch current and node voltages of the circuits. An electronic circuit in which performance of the circuit is identified in terms of referred voltage at different input and output nodes known as Voltage-Mode (VM) circuit. An operational amplifier is one of the most predominant devices to develop VM circuits. The VM circuit has high impedance nodes architecture, so the underlying parasitic components present at different nodes get charged and discharged with high voltage swing. Therefore, the VM circuit is not suitable for low power, wide bandwidth, high speed, and high slew rates operation. Current Mode (CM) signal processing circuits have emerged over the past few decades as an alternative design strategy for low power analog signal processing. The concept of the Current Conveyor (CC) was first introduced by Sedra and Smith in 1968 and subsequently

revised in 1970 [1]. An essential component for the formulation and execution of integrated circuits is the Operational Transconductance Amplifier (OTA), which was introduced by Wheatley and Wittlinger in 1969 [2]. The Third-Generation Current Conveyor [3] emerged in 1995 as an improved iteration of the preexisting conveyor. However, another current conveyor, known as the Second-Generation Current Controlled Current Conveyor (CCCII) [4], was documented in 1996. There are a number of functional CM blocks accessible in the scholarly literature such as, Operational Trans resistance Amplifier (OTRA) [5], Current Feedback Operational Amplifier (CFOA) [6], Current Differencing Buffered Amplifier (CDBA) [7], Differential Difference Current Conveyor (DDCC) [8], Differential Difference Current Conveyor (VDTA) [9], Voltage Differencing Current Conveyor (VDCC) [10], Current Backward Transconductance Amplifier (CBTA) [11], Differential Voltage Current Conveyor (DVCC) [12], Dual-X Current Conveyor Transconductance Amplifier (DXCCTA) [13], Current Follower Transconductance Amplifier (CFTA) [14], and many more.

1.1 Literature survey

Active immittance circuit is a prominent area of study within the realm of active circuit design due to the drawbacks associated with incorporating traditional components such as inductors and resistors into microelectronic circuits. These drawbacks include the utilization of significant chip space, increased weight, higher costs, and limited adjustability. The immittance circuits find numerous applications in the domains of microelectronics, communication, analog signal processing, instrumentation, and measurement.

Various implementations of the integer order immittance circuit exist, relying on analog active building blocks. Literature survey on available integer order grounded and floating immittance emulators [15-83] shows that – Refs. [15-61] provide floating immittances. while those reported in Refs. [62-83] furnish grounded immittances. The available floating immittance emulators use single [27,29,35,36,41,43,45,47,51,52,53,56,58-60]/ multiple active block(s) [15-26,28,30-34,37-40,44,46,48-50,54,55,57,61]. These emulators use CCII [15-19], Current Differencing Buffered Amplifier (CDBA) [20], CCCII and Dual Output Second-Generation Current Controlled Current Conveyor (Do-CCCII) [21-22], OTA [23], Dual Output Second Generation Current Conveyor (Do-CII) [24], Second-Generation Dual-X Current Conveyor (DXCCII) and MOS transistors [25], Minus-Type Modified Inverting First-Generation Current Conveyor (MICCI) [26], Modified Current Feedback Operational Amplifier (MCFOA) [27], CCCII [28],

CFOA [29,30], Differential Voltage Current Conveyor (DVCC) and CCII [31], DDCC and CCII [31], DVCC and DDCC [31], CFOA and MOS Transistor [32], OTA and DO-CCII [33], DVCCTA [34,35], DVCC and DDCC [36], Voltage and Current Gained Second Generation Current Conveyor (VCG-CCII) [37], Current Differencing Transconductance Amplifier (CDTA) [38], DVCCC [39], DVCCII [40], Multiple Output Current Controlled Current Conveyer Transconductance Amplifier (MO-CCCCTA) [41], Z-Copy Voltage Differencing Current Conveyor (ZC-VDCCC) [42], Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA) [43], Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA) [44], CBTA [45,46], Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) [47], CFTA [48], VDTA [49], Voltage and Current Follower [50], VDCC [51], Current Conveyor Transconductance Amplifier (CCTA) [52], Modified Voltage Differencing Voltage Transconductance Amplifier (MVDVTA) [53], Current Controlled Current Feedback Amplifier (CC-CFA) [54], Voltage Differencing Buffered Amplifier (VDBA) [55], DXCCTA [56], Voltage Differencing Differential Difference Amplifiers (VDDDA) [57], Four Terminal Floating Nuller Transconductance Amplifier (FTFNTA) [58], DDCC [59-60], and Differential Voltage to Current Converters (DVTCC) [61] Now, grounded immittance emulators available in literature utilize either a single [62,64-77,79,83] or multiple active blocks [63,78,80-82]. These emulators employ Modified Inverting Second-Generation Current Conveyor (MICCII) [62], CCII [63], Positive Four Terminal Floating Nuller (PFTFN) [64], Z-Copy Current Controlled Current Inverting Transconductance Amplifier (ZC-CCCITA) [65], Operational Transresistance Amplifier (OTRA) [66-70], VDCC [71], Inverting Current Feedback Operational Amplifier (ICFOA) [72], DXCCII [73], Voltage Differencing Buffer Amplifier (VDBA) [74], Voltage Differencing Inverting Buffered Amplifier (VDIBA) [75], Current Follower Current Conveyor (CFCC) [76], Modified Differential Voltage Current Conveyor (MDVCC) [77], CFOA [78], Dual-X Current Conveyor Differential input Transconductance Amplifier (DXCCDITA) [79], CCII and Inverting Voltage Buffer (IVB) [80], Second Generation Voltage Conveyor (VCII) [81], Dual Output Voltage Differential Current Conveyor (DO-DVCC) [82], and VDDDA [83]. Moreover, floating and grounded immittance emulator may be further classified as positive and negative immittance emulator. Literature survey on available positive and negative immittance emulators [15-83] shows that – Refs. [15-41,43-65,68,69,71-75,77-83] provide positive

immittances. while those reported in Refs. [22,23,30,32,33,41,45,53,56,59,60,65,66,67,70,71,73] denotes negative immittances.

A detailed study of floating and grounded immittance emulators reveals that – there is limited presence of impedance tunning features in [15-19,24,26,27,29-31,39,40,47,50,59,62,63,66-70,73,77,78,80-82]. Further, component matching is required in [26,30,36,50,60,62,64,66-70,73,77,78,82] for correct functionality which is difficult to achieve in integrated circuits. Also, the circuit in the topological change (interchanging of input terminals, changing components' placement)/different circuit design is required for providing positive and negative immittance in [22,23,30,32,33,41,45,53,59,60,65,71,73,76]. In addition, more than one passive component is required in [15-19,21,22,24-27,30-37,39,40,45-47,50,51-53,55,58,59,60-64,66-74,76-82]. Moreover, Refs. [15,16,24,27,31,47,57,58,72,75,76,78,79] and Refs. [17-19,26,29,30-32,36,37,50,55,59,61,62,64,66-70,73,74,77,80-82] require single floating passive component and multiple floating components respectively. It is clear from above discussion that a limited literature is available immittance emulators that may simultaneously fulfil the following criterions: tunability, no matching constraint and working in positive and negative mode without topological changes. Further, it is pertinent to mention here that the topological change is not possible once the circuit is laid down and fabricated. Also, if two different circuits are realized in IC form for positive and negative immittances, the resulting in larger silicon footprint.

The biomedical signal processing applications require at low frequency operation which require large magnitude of immittance value. An active immittance multiplier is useful in such situations for realizing a substantial magnitude of immittance value from a component of smaller magnitude. In the literature, there have been several reports on the development of active floating [84-97] and grounded immittance multiplier circuits [98-119]. The available floating immittance multiplier use single [91]/ multiple active block(s) [84-90,92-94,96,97]. These floating immittance multiplier employ OTA [84], CCII [85], CCCII [86], CFOA [87,88], CDTA [89], Current Controlled Differential Difference Current Conveyor (CCDDCC) [90], FB-VDBA [91], MODVCC [92], DO-CCII [93,94], FTFN [95], VDCC [96], and VDCCII [97]. Further, floating immittance multiplier available in literature utilize either a single [99,101,105,106,108] or multiple active blocks [98,100,102,103,104,107,109]. These grounded immittance multiplier uses OTA [98], CCII [99], CFOA [100-104], ICFOA [105], DXCCII [106], CFOA and OTA [107], Third Generation Current Conveyor Transconductance Amplifier (CCIIITA) [108],

OTRA [109], VCCII [110,111], Inverting Second Generation Current Conveyor (ICCII) [112], OTA and Differential Voltage Buffer (DVB) [113], CFTA [114,115], Current Follower Differential Input Transconductance Amplifier (CFDITA) [116], VDTA [117,118], and CCCDTA [119].

Nowadays, fractional order circuits gain considerable attention among researcher due to extra degree of freedom to control the phenomena of the system. Fractional calculus is a powerful and widely used tool to demonstrate the characteristics of many systems in the real world such as thermodynamic [120], volcanology [121], human organ [122], biomedicine [123], earthquake [124], modelling of virus [125] and many more. The fractional-order circuits and systems have immense potential in the areas of fractional order controller [126], fractional order signal generating [127,128] and signal processing circuits [129,130,131]. The basic building blocks for the design of a fractional order system are known as fractor having input impedance of $Z(s) = \frac{k_o}{s^\alpha}$ where α ($|\alpha| < 1$) represents order of fractor and k_o is constant. Depending upon the value of α the behavior of the element changes from fractional order inductor to fractional order capacitor. For specific value of α as -1, 0, 1 the fractance turns into classical element capacitor, resistor, inductor respectively, whereas α = -2 corresponds to Frequency Dependent Negative Resistance (FDNR).

Over the years, a limited no. of active block based fractional capacitor is designed. Pacheco et. al [132] developed FC using combinations of Op-amp based Weighted Differential Amplifier (WDA), Weight Adder Amplifier (WAA), Inverting Integration Circuit (IInv), Inverting amplifier (Inv), and Inverting Weighted Adder Amplifier (IWAA). Active realization of first order Continued Fractional Expansion approximation of the fractional capacitor needs three Op-amps, six grounded resistors, seven floating resistors, and one floating capacitor. The order of the Op-amp based fractional capacitor is changed by varying pole frequency of lead/lag phase network. The Op-amp non-idealities such as finite unity gain frequency may reduce the constant phase zone of the fractional order device and deteriorate its constant phase nature [133]. Prommee et al. [134] designed a fractional-order capacitor using OTA-based voltage gain circuit and integrator circuit. The order of OTA based fractional capacitor may be changed by tunning the bias current of the OTA and changing the passive capacitors. An active realization of the fifth order CFE approximation of the fractional capacitor needs 19 OTAs and 5 capacitors. Design of a fractional inductor using large number of OTA-based fractional-order capacitor may result in a

low figure of merit. Therefore, the researchers have made effort in the direction of approximating the fractional order capacitor behavior (Carlson approximation [135], Matsuda approximation [136], Oustaloup approximation [137] Charef approximation [138] and Continued Fractional Expansion [139]) and subsequently designing and developing emulators using appropriate RC ladder.

The fractional order inductor may be designed using a General Impedance Converter (GIC) and fractional order capacitor. These inductors can be classified as positive and negative fractional order inductors. The former is used to design fractional order filter, modeling of the human respiratory system, and fractional order oscillator whereas the latter may find application in parasitic inductance cancellation. Over the years, GIC based fractional inductor simulators [56,140-147] have been presented in the literature. These fractional inductor circuits use OTA and CFOA [56], Op-amp [140-143], CFOA [144,145], OTA and Differential Voltage Buffer (DVB) [146], and OTA [147]. Further, fractional order inductor present in literature is operating either in floating mode [56,146] or grounded mode [140-145,147]. The reported positive fractional inductor circuits are limited in terms large number of active and passive components [56,140-143], tunability [140-144], slew rate [140-143], operating frequency [140-144,147], high power dissipation [146], high chip area [146], and low figure of merit [56,140-147]. Moreover, from the perspective of integration, a single topology positive and negative fractional inductor can be helpful. This type of topology may be referred to as reconfigurable circuit as it provides both positive and negative fractional inductors by varying only the gate voltage of MOS switches and thereby making the circuit user-friendly. Such a reconfigurable circuit benefits from reduced chip area, lower power dissipation, and lower cost. Further, the study of available literature reveals that no circuit is present featuring reconfigurable fractional order positive and negative inductor circuits.

Mutually Coupled Circuit (MCC) is yet another domain of immittance circuits. It is frequently used in circuits for instrumentation, measurement, analog communications, and signal processing. The coupling factor, mutual inductance, primary inductance, and secondary inductance are the primary features of the MCC. The MCC simulator provides a relationship between the voltages and currents of their ports even though they lack real magnetic couplings. By altering the bias current of the active block circuit, the values of the inductances and the coupling coefficient may both be adjustable. Due to the lack of inductive components, the MCC

simulators are easily incorporated. The lack of significant inductive components makes MCC suitable for integrated circuits.

Literature survey reveals that MCCs have been reported [148-164] using different active building blocks. The MCC reported in [148,149] is implemented using large no. of Bipolar Junction Transistor (BJT) and large number of resistors and capacitors. In [150], a MCC is developed using eight OTAs. Moreover, in [151] the MCC topologies are designed using BJT, CCII, and OTAs. Furthermore, the MCC is given in [152] employ six CCIIs. However, four CCIIs based MCC topology is illustrated in [153]. The MCC in [154] realized using three CCCIIs and two DO-CCCIIs. In [155], the reported MCC utilizes four CCCIIs. The topology presented in [156] realizing MCC using two DVCCs and two CCIIs. However, [157] used three CC-CBTAs in implementation of MCC. In [158], the MCC produces using two DVCCTAs. Moreover, in [159] MCC is developed using two CCCCTAs. Further, the MCC is proposed using two CBTAs in [160]. The circuit reported in [161] realizes MCC using four CFOAs. In [162], the reported MCC is developed using two VDDCCs. However, two VDTAs based MCC are mentioned in [163]. Moreover, in [164] the realization of MCC is done using two CCTAs. It is also observed from the above literature survey, the number of active blocks and passive components in available MCCs vary from 2 to 8 and 2 to 11 respectively. The MCCs [150-157,162] use more than two active blocks while those presented in [151-161,164] consist of more than two passive components. The MCCs reported in [151-153,161] do not facilitate tuning feature. The overall transistor counts in [153-158,161,164] is more than 46 transistors and therefore these circuits may require a larger chip area for realization. Further, the study of available MCCs reveals that no circuit is present featuring mutual inductance in four different pairs like passive transformers.

Furthermore, Memristor is the fourth [165] fundamental element in circuit theory after resistors, capacitors, and inductors. It is gaining considerable attention among researchers due to its high-density storage property. It is a non-linear device depending upon the previous history of current. Leon O. Chua developed memristor by giving the relation between electric charge (q) and magnetic flux (φ) in 1971 [166]. The memristor's memristance remains constant even when the input signal is absent, which is referred to as the non-volatile characteristic of the memristor. Since memristor has nonlinear characteristic, non-volatile nature, and high-density storage properties, it is being used in a variety of applications such as programmable gate arrays [167], programmable analog circuits [168], neuromorphic circuits [169], adaptive learning [170,171],

adaptive filters [172], chaotic oscillators [173], and relaxation oscillators [175,176] etc. After 37 years of proposal of the memristor by L O. Chua, Hewlett-Packard (H. P.) lab created the first solid-state memristor in 2008. Due to its high price and difficult manufacturing process, this solid state memristor is not currently accessible. This constraint spurs researchers to create memristor circuits based on Active Building Blocks (ABB). Below is a literature review of an ABB-based memristor emulator.

A variety of memristor emulators have been reported in current literature [177-193]. The programmable analog circuit-based memristor emulator was created by Pershin and Ventra [177]. It is made up of an Analog to Digital Converter (ADC), a microprocessor, and a digital potentiometer. However, the digital potentiometer's finite resolution limits performance. The Voltage-Controlled Resistor (VCR), CCII, and Operational Amplifier (Op-amp) are components of the memristor circuit invented by Hussein and Fouda [178]. Nevertheless, performance is constrained due to the limited linear range of VCR transistors. Arundeepakvel et al. [179] designed Mutator circuit needs one Voltage Inverting Mutator (VIM), two resistors, two diodes and one inductor. The study suggests that passive inductor based memristor circuit requires large chip area. According to the study, passive inductor-based circuits are expensive and large. Three Op-amps, eleven resistors, one Light Dependent Resistor (LDR), one capacitor, and one diode make up the memristor circuit that Fitch et al. [180] showed. The performance of the memristor at higher frequencies was constrained by LDR characteristics. A straightforward and adaptable memristor was created by Abuelama'atti and Khalifa [181] using four CFOA, four resistors, two diodes, and four capacitors. Off-the-shelf floating memristor was introduced by Sozen and Cam [182] and features four CCIIs, three OTAs, six resistors, and one capacitor. A second voltage source is needed to bias the current of one of the OTAs. Some memristor emulators [183-187] call for an extra circuit, such as a multiplier circuit, in addition to active and passive elements. Voltage across a memristor must be multiplied by the flux of the memristor using an analog multiplier circuit. The use of extra circuitry might make the memristor circuit more complicated and lower its operating frequency. One grounded capacitor and two OTAs are present in the floating memristor that is being demonstrated [188] without the need of multiplier circuits. It is nonetheless used up to 400 kHz. However, the floating memristor emulator described in [189] only needs one VDTA, one capacitor, and one resistor, and it can function up to 50 MHz. Additionally, the floating memristor described in [190] has a 10 MHz maximum working

frequency. Three resistors, one grounded capacitor, and one CCTA are used. The literature has a reconfigurable, adjustable grounded memristor emulator [191-193]. The exhibited memristor's maximum operational frequencies in [191], [192], and [193] are 1 MHz, 26.3 MHz, and 9 MHz, respectively. According to the study, grounded memristors are inappropriate for complicated circuits [190]. A floating memristor [194] was developed using OTA and CDTA. The architecture is significantly altered to allow it to work in incremental and decremental mode up to 2 MHz frequency. The memristor emulators shown in [195-197] use different supply voltages, necessitating a high-quality manufacturing architecture [188]. A review of the literature indicates that the reported memristor circuits have limitations in terms of the operating frequency range, mode of operation, supply voltage, number of active and passive components, and additional circuits like multipliers, digital potentiometers, microprocessors, passive inductors, and ADC.

1.2 Research Gaps

The following research gap can be obtained from above literature survey:

a. There is limited presence of impedance tunning features in available immittance emulators. Further, component matching is required for correct functionality which is difficult to achieve in integrated circuits. Also, the circuit in the topological change (interchanging of input terminals, changing components' placement)/different circuit design is required for providing positive and negative immittance. Thus, a limited literature is available immittance emulators that may simultaneously fulfil the following criteria: tunability, no matching constraint and working in positive and negative mode without topological changes. Further, it is pertinent to mention here that the topological change is not possible once the circuit is laid down and fabricated. Also, if two different circuits are realized in IC form for positive and negative immittances, the resulting in larger silicon footprint.
b. No MCC circuit is present featuring mutual inductance in four different pairs like passive transformers is available in open literature.
c. The reported memristor emulators have limitations in terms of their operating frequency range, mode of operation, supply voltage, number of active and passive components, and usage of additional circuits like multipliers, digital potentiometers, microprocessors, passive inductors, and ADC.

1.3 Research Objectives

Research objectives of the thesis are established with consideration of the research gap highlighted in the previous section. The study aims to design different types of immittance circuit such as grounded and floating elements, positive and negative integer order elements using single topology, positive and negative fractional order elements using single topology, mutually coupled circuit, and memristor emulators using suitable ABBs (Active Building Blocks). The primary considerations for these designs include fewer active blocks and passive elements, low power consumption, wide operating frequency, low chip area, and a simple architecture. Thus, there are following objectives are set for the research work:

a. Design of tunable grounded immittance circuit that can work in both positive and negative modes without topological change.
b. Design of tunable floating immittance circuit that can work in both positive and negative modes without topological change.
c. Design of mutually coupled circuit capable of working in all four pairs.
d. Designing of multiplier less mem immittance circuit.

1.4 THESIS Organization

The thesis is structured into seven chapters. Each chapter includes a brief introduction, circuit analysis description, nonideal analysis of the proposed circuit, Monte Carlo analysis, supply voltage variation, temperature variation etc. Furthermore, these chapters present a discussion on simulation results, and a comparison with previously published work, followed by a summary.

Chapter 1 describes evolution and significance of current mode based analog circuit. The constraint of voltage mode ABB is analyzed briefly. A short review of different kinds of current mode ABB is also presented. After words, research gaps in the field of integer and fractional order immittance circuit, synthetic transformer, and memristor circuit are illustrated. Finally, this chapter ends with organization of thesis.

Chapter 2 describes detail illustration of ideal and non-ideal model of current mode analog building blocks such as Operational Transconductance Amplifier (OTA), Current Conveyor Transconductance Amplifier (CCTA), Inverting Current Conveyor Transconductance Amplifier (ICCTA), and Current Feedback Operational Amplifier (CFOA).

Chapter 3 illustrates three positive and negative tunable integer order immittance circuit and their applications. The first positive and negative grounded immittance circuit is designed using

one CCTA, one grounded resistor, one grounded capacitor and two MOS switches. The second positive and negative floating immittance circuit utilizes two CCTAs, two grounded resistors, one floating capacitor, and four MOS switches. Whereas the third positive and negative floating immittance circuit employs two CCTAs, one floating MOS resistor, one floating capacitor and four MOS switches. In addition, Current Feedback Operational Amplifier (CFOA) based lossless grounded negative impedance multiplier circuit is also designed. This circuit is designed by two CFOAs and three passive components. The designed circuit may emulate grounded capacitance multiplier, grounded inductance multiplier, grounded frequency dependent negative resistor and grounded resistance divider circuit. Impact of the parasitic components associated with terminals of CCTA and CFOA on performances of the above designed circuits is mathematically formulated. Transient and frequency response of designed circuits are demonstrated to justify the theoretical prepositions. The applicability of the proposed is demonstrated through active filters.

Chapter 4 describes electronically adjustable floating and grounded fractional order inductor circuits. The developed circuits utilize two OTAs, one fractional order capacitor, one inverter, and four MOS switches. These circuits can operate in both positive and negative modes without any changes to their topology. The behavior of the suggested circuit is further examined in the presence of parasitic elements that may arise in the practical circuit. The efficacy of the suggested positive fractional inductor circuit is showcased by employing it in a fractional order band pass filter and a fractional order high pass ladder filter. The practicality of the suggested negative fractional inductance circuit is showcased with the help of a fractional inductance cancellation circuit.

Chapter 5 investigates electronically tunable mutual coupled circuit employing CCTA. This circuit includes two CCTAs, two capacitors, three resistors and four MOS switches. The designed circuit follows the dot convention of passive transformer and produces all four pairs of mutually coupled circuit like passive transformer by appropriate setting of MOS switches. The proposed MCC does not require component matching condition. Self-inductance, mutual inductance, and resonant frequency can be tuned by bias current of CCTA. Furthermore, non-ideal effects on the proposed MCC are discussed. A double tuned band pass filter is shown as an application.

Chapter 6 presents charge and flux controlled memristor emulators and their application using ICCTA. The flux-controlled floating memristor emulator is implemented using one ICCTA, one

resistor, and one capacitor. Whereas charge controlled floating memristor emulator is composed of one ICCTA, one capacitor, and three resistors. Both emulators are free from additional circuits like ADC, DAC, analog multiplier circuits, passive inductor, light dependent resistor, and diodes. Furthermore, non-ideal analysis of these memristors is mathematically examined. Additionally, the meminductor circuit and memristor-based active filter have been implemented to examine the designed memristor emulators.

Chapter 7 discusses the conclusion and future scope of the work.

CHAPTER 2

ANALOG BUILDING BLOCKS

This chapter describes different analog building blocks used to develop immittance emulator in this work. The port relationships of these blocks and their verification through SPICE is also put forward as background material.

2.1 Operational transconductance amplifier

Operational Transconductance Amplifier (OTA) is a current mode active building block that has various advantages over voltage mode active building blocks for instance high dynamic range, more linearity, wide bandwidth, high slew rate, simple tunning, low chip area, and low power consumption. Due to these benefits, OTA has made a substantial contribution to many analog signal processing and generating circuits including filter [211,212], oscillator [212, 213], and multivibrator [214] etc. The OTA is a differential voltage controlled current source with high input and output impedance. The transconductance of OTA may be controlled by the input bias current (I_B). Circuit symbol of OTA is given in Fig. 2.1(a). The OTA has four terminals namely V_+, V_-, O_+, and O_-. V_+ and V_- are input terminals and O_+ and O_- are output terminals. MOS based circuit realization of OTA is illustrated in Fig. 2.1(b). It is seen from Fig. 2.1(b) that the differential stage consists of transistors M_1-M_4, whereas transistors M_5-M_{12} ensure that the currents at O_+ and O_- terminals of OTA are equal in magnitude. Thus, the difference of the input voltage $(V_+ - V_-)$ is converted to be the output current ($I_{O\pm}$) through transconductance (g_m). The characteristic equation of OTA is given by eq. (2.1) which may be used to add electronic tunning feature to the performance parameters of immittance emulator, filter, oscillator, and multivibrator.

$$I_{O\pm} = g_m(V_+ - V_-) \tag{2.1}$$

Where $V_+$and V_- are input voltages at inverting and non-inverting terminals. The g_m represents transconductance of the OTA, while $I_{O\pm}$ are output currents at O_+ and O_- terminals. Here, the transconductance gain g_m of OTA can be written as:

$$g_m = \sqrt{\mu_n C_{OX} I_B \left(\frac{W}{L}\right)_{3/4}} \tag{2.2}$$

where μ_n, C_{ox}, and $\left(\frac{W}{L}\right)_{3/4}$ are the electron mobility of NMOS, gate oxide capacitance per unit area, and aspect ratio of transistor M_3 or M_4 respectively. It is notable from eq. (2.2) that the value of transconductance can be changed by varying the bias current of OTA.

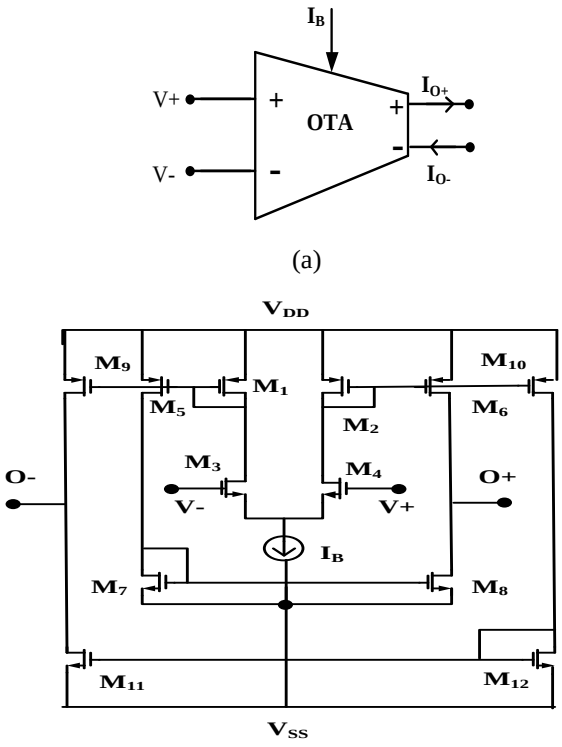


Fig. 2.1 OTA (a) circuit symbol (b) MOS based design.

2.1.1 Non-ideal model of OTA

The parasitic components appear at different terminals of OTA in the form of the parallel combination of resistances and capacitances are depicted in Fig. 2.2. The parasitic components associated with terminals, V_{-}, V_{+}, O_{+}, O_{-} are represented as $R_{V-} \parallel C_{V-}$, $R_{V+} \parallel C_{V+}$, $R_{O+} \parallel C_{O+}$, and $R_{O-} \parallel C_{O-}$ respectively. These parasitic components may lead to deviation in the performance of the device.

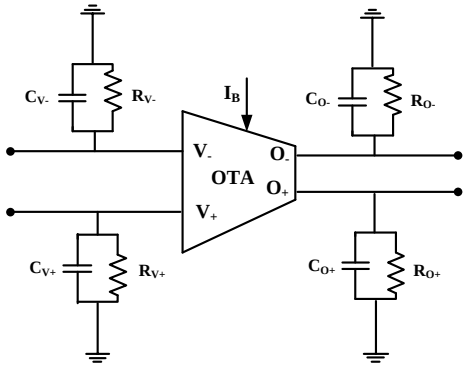


Fig. 2.2 Non-ideal model of OTA.

2.1.2 Verification of OTA

Verification of OTA is carried out using SPICE simulator. CMOS parameter of 90 nm technology is used for the purpose of simulations. Aspect ratios of the transistors employed in Fig. 2.1 are provided in Table 2.1. Supply voltage is chosen to be ±1.2 V, whereas the value of bias current is 120 µA is taken for simulations. The variation of current I_{O+} and I_{O-} against the (V_+ - V_-) is shown in Fig. 2.3. Fig. 2.3 shows that I_{O+} and I_{O-} exhibit a linear variation within the voltage range of -100 mV to 100 mV. Frequency response of OTA is shown in Fig. 2.4. The operating frequency of the OTA for transconductance gain is found to be 200 MHz.

Table 2.1: Aspect ratio of transistors of OTA.

Transistor	W(µm)/ L(µm)
M_1, M_2, M_9, M_{10}, M_5, M_6	2.15/0.7
M_3 - M_4	5.75/0.7
M_7, M_8, M_{11}, M_{12}	1.45/0.7

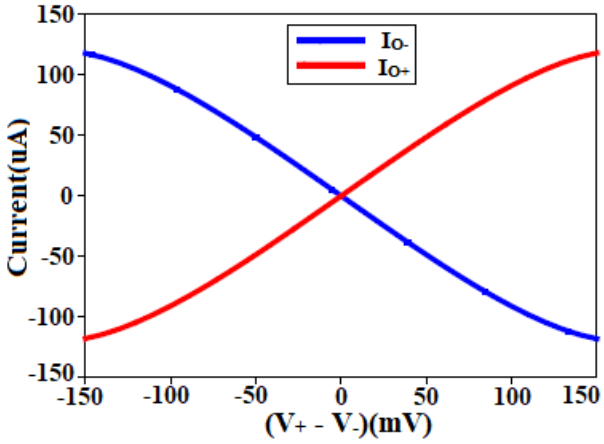


Fig. 2.3 DC characteristic of OTA.

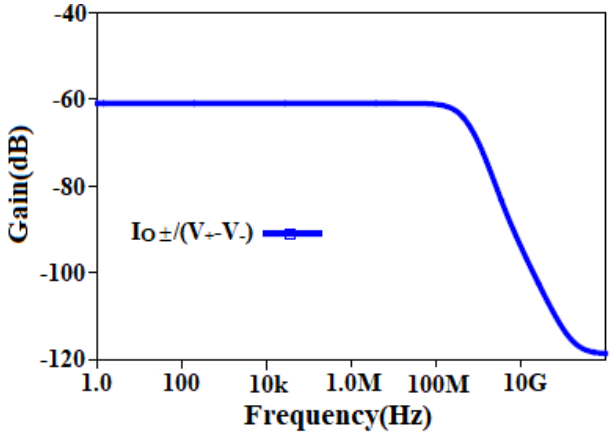


Fig. 2.4 Frequency response of OTA.

2.2 Current conveyor transconductance amplifier

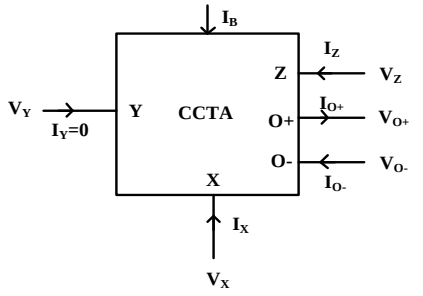
Current Conveyor Transconductance Amplifier (CCTA) comprises of CCII and a dual output Operational Transconductance Amplifier (OTA). Its circuit symbol and MOS based schematic are shown in Fig. 2.5. The current mirror, comprised of transistors M_3 and M_4, ensures that the drain currents of transistors M_8 and M_9 are identical. Hence, the voltage at Y terminal is conveyed to X terminal. The current conveying operation from terminal X to Z is facilitated by selecting transistors M_1 and M_2 with equal aspect ratios. Hence, current fed into X terminal is conveyed to Z terminal. The current flowing out of $O_{\pm}$ terminal is product of transconductance of OTA and Z terminal voltage. The characteristics equations of the CCTA are given by eq. (2.3).

$$I_Y = 0;\ V_X = V_Y;\ I_Z = I_X;\ I_{O\pm} = \pm g_m V_Z \tag{2.3}$$

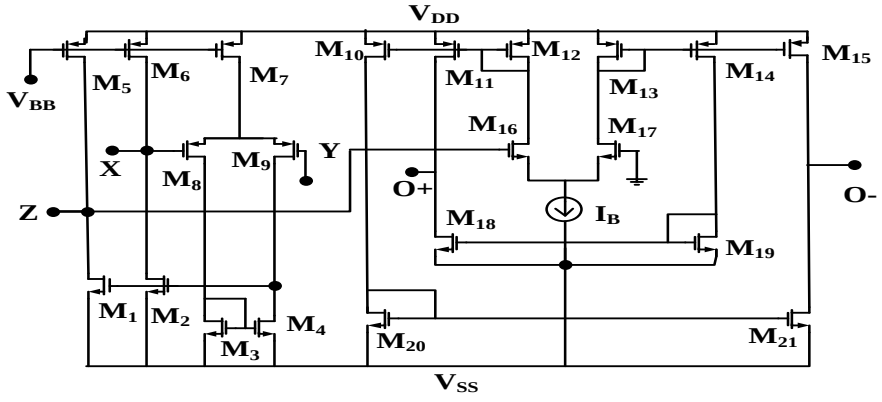
The g_m corresponds to transconductance parameter that can be mathematically defined as:

$$g_m = \sqrt{\mu_n C_{OX} I_B \left(\frac{W}{L}\right)_{16/17}} \tag{2.4}$$

where μ_n is the mobility of charge carrier, C_{OX} is a gate capacitance per unit area, I_B is bias current of CCTA and $(W/L)_{M_{16/M_{17}}}$ is aspect ratio of the MOS transistor M_{16}/ M_{17} respectively.



(a)



(b)

Fig. 2.5 CCTA (a) circuit symbol (b) MOS based implementation of CCTA.

2.2.1 Non-ideal Model of CCTA

In practice, the parasitic components are associated with different ports of CCTA and show their presence in the form of parallel combination of resistances and capacitances at Y, Z, O_+, and O_- ports, and a series resistance at X port. Considering parasitic associated at terminals Y, X_+, Z_+, O_+, and O_-, as $R_Y||C_Y$, R_{X+}, $R_{Z+}||C_{Z+}$, $R_{O+}||C_{O+}$, and $R_{O-}||C_{O-}$ respectively, the CCTA symbol of Fig. 2.5(a) is modified as Fig. 2.6.

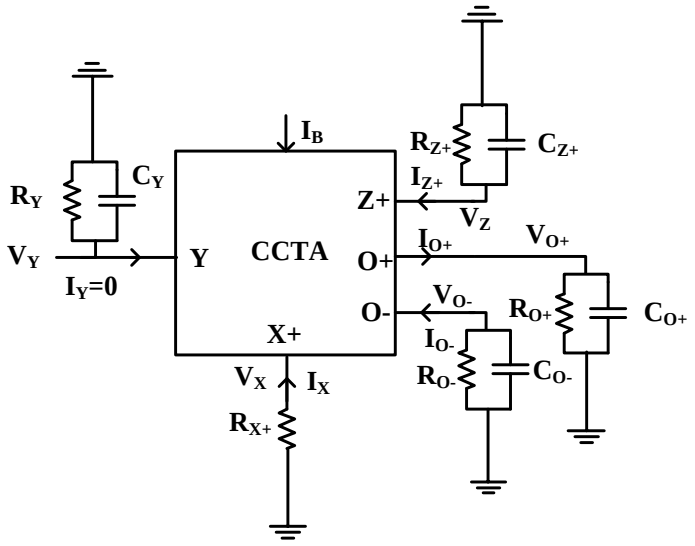


Fig. 2.6 Non-ideal model of CCTA.

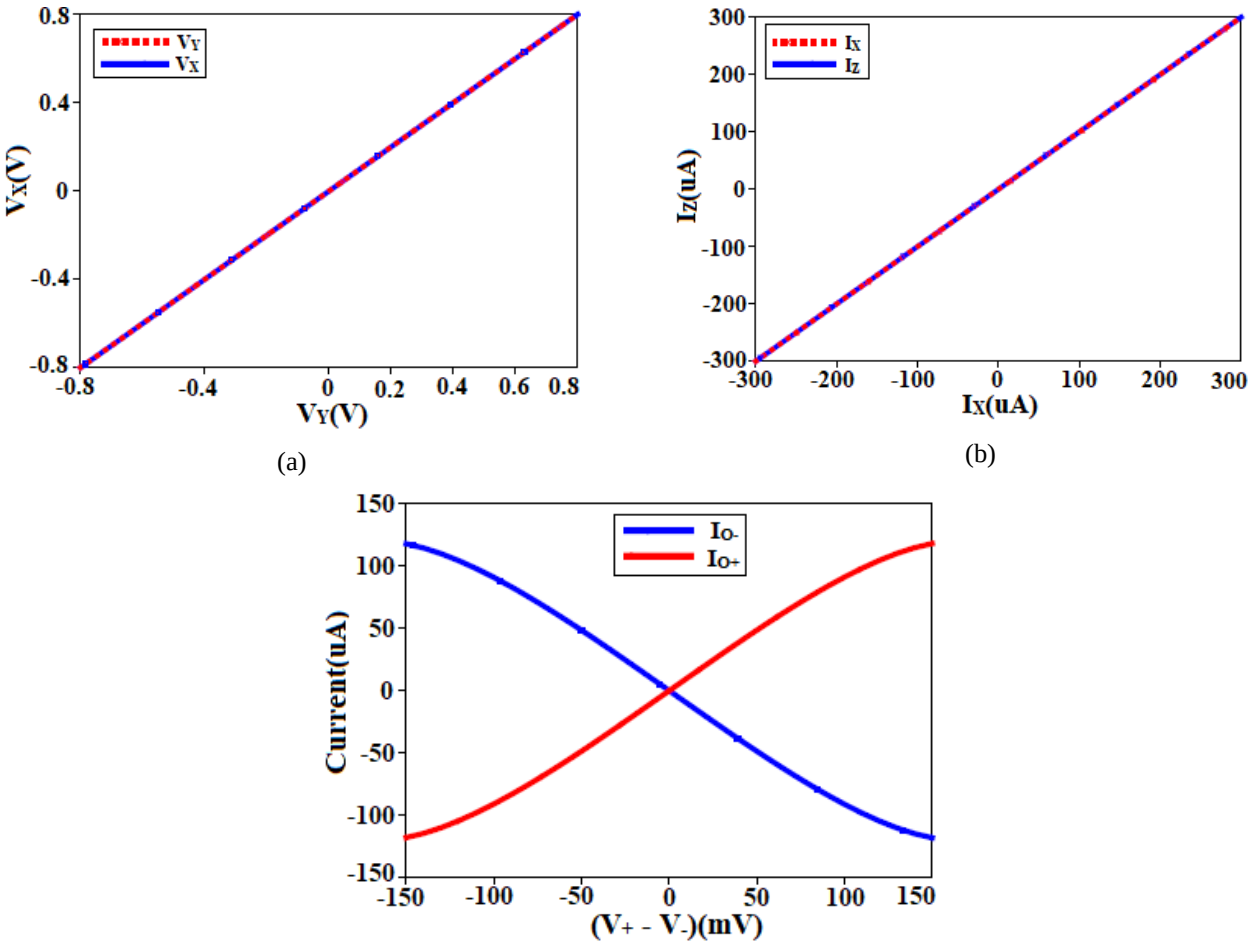
2.2.2 Verification of CCTA

The CMOS implementation of the CCTA is verified through SPICE simulator using 90 nm technology parameter. Table 2.2 enlists the aspect ratios of the MOS transistors utilized in the CMOS implementation of CCTA. The power supply is ± 1.2 V, whereas the bias voltage is set to 0.42 V. The bias current of the CCTA is selected as 120 μA. The DC analysis of the CCTA is displayed in Fig. 2.7. Fig. 2.7(a) illustrates the DC voltage transfer characteristics of V_X in relation to the voltage V_Y. The input voltage dynamic range of CCTA, ranging from V_Y to V_X is -800 mV to 800 mV. Furthermore, Fig. 2.7(b) illustrates the direct current transfer from I_X to I_Z. The input current dynamic range of CCTA, ranging from I_X to I_Z, has been reported to be -300 μA to 300 μA. Fig. 2.7(c) demonstrates the DC transconductance transfer characteristics of the CCTA from voltage V_Z to current I_{O+} and I_{O-}. It is observed from Fig. 2.7(c) I_{O+} and I_{O-} exhibit a linear variation within the voltage range of -100 mV to 100 mV. Now, the frequency response of the CCTA for voltage gain, current gain, and normalized transconductance gain is displayed in

Fig. 2.8. It may be noted from Fig. 2.8 that the operating frequency range of the voltage gain, current gain, and transconductance gain are 3 GHz, 3 GHz, and 200 MHz respectively.

Table 2.2: Aspect ratio of transistors of CCTA.

Transistor	W(μm)/ L(μm)
M_1, M_2, M_5, M_6, M_7	2.4/0.18
M_8, M_9	0.35/0.18
M_3, M_4	0.65/0.18
M_{10} – M_{15}	2.15/0.7
M_{16}, M_{17}	5.75/0.7
M_{18} – M_{21}	1.45/0.7



(a) (b)

(c)

Fig. 2.7 Port relations of CCTA. (a) $V_X = V_Y$, (b) $I_Z = I_X$, and (c) $I_{O\pm} = \pm g_m V_Z$.

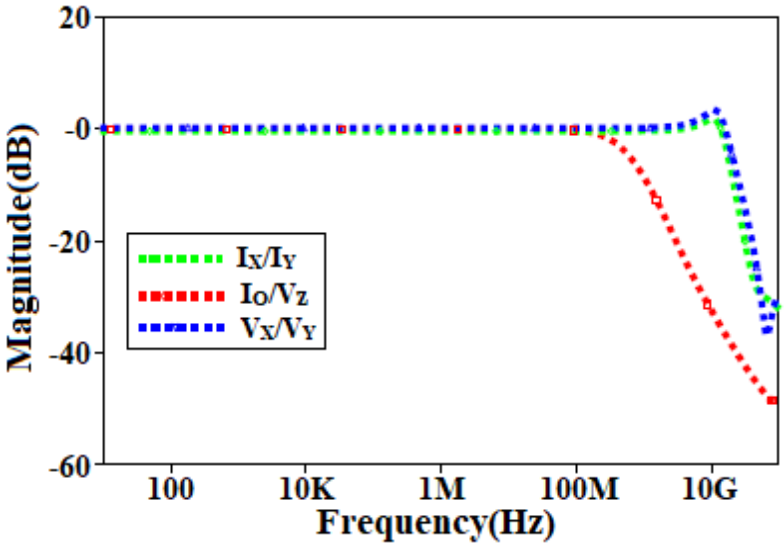


Fig. 2.8 Frequency response of CCTA.

2.3 Inverting current conveyor transconductance amplifier

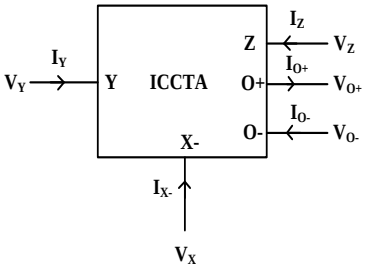
An Inverting Current Conveyor Transconductance Amplifier (ICCTA) is current mode active building block (ABB). This ABB comprises of inverting current conveyor and a dual output operational transconductance amplifier. The schematic symbol and CMOS realization of ICCTA are illustrated in Fig. 2.9. The transistors M_3-M_5 and M_{10}-M_{12} are used to implement an inverting voltage follower. Therefore, the voltage at X- terminal is inverted voltage of the applied voltage to Y terminal. In order to facilitate the current conveying operation from terminal X- to terminal Z, it is recommended to select transistors M_{13} and M_{14} with equal aspect ratios. Thus, the current fed into X- terminal is conveyed to Z terminal. The Y terminal has high input impedance. Hence, current passes through Y terminal will be zero. The current flowing out of O± terminal is transconductance times voltage of Z terminal. The characteristic equations of ICCTA are given by eq. (2.5).

$$I_Y = 0;\ V_Y = -V_{X-};\ I_Z = I_{X-};\ I_{O\pm} = \pm g_m V_Z \tag{2.5}$$

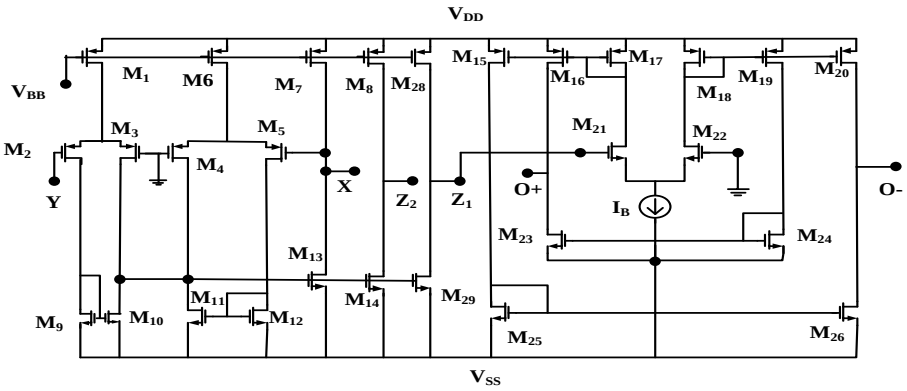
The g_m corresponds to transconductance parameter that can be mathematically expressed as:

$$g_m = \sqrt{\mu_n C_{OX} I_B \left(\frac{W}{L}\right)_{21/22}} \tag{2.6}$$

Where, μ_n, C_{ox}, and $\left(\frac{W}{L}\right)_{21/22}$ are the electron mobility of NMOS, gate oxide capacitance per unit area, and aspect ratio of transistor M_{21} or M_{22} respectively.



(a)



(b)

Fig. 2.9 ICCTA (a) circuit Symbol and (b) CMOS based realization.

2.3.1 Non-ideal Model of ICCTA

Parasitic resistances and capacitances at different terminals of ICCTA may deviate the current and voltage relations of the ICCTA. Figure 2.10 illustrates the parasitic model of ICCTA. It may be observed from Fig. 2.10 that the parasitic components associated with terminals X, Z, Y, O_+ and O_- of ICCTA are R_X, $R_Z||C_Z$, $R_Y||C_Y$, $R_{O+}||C_{O+}$ and $R_{O-}||C_{O-}$ respectively.

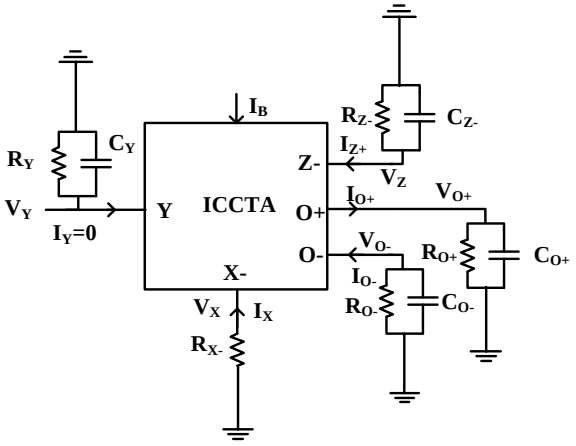


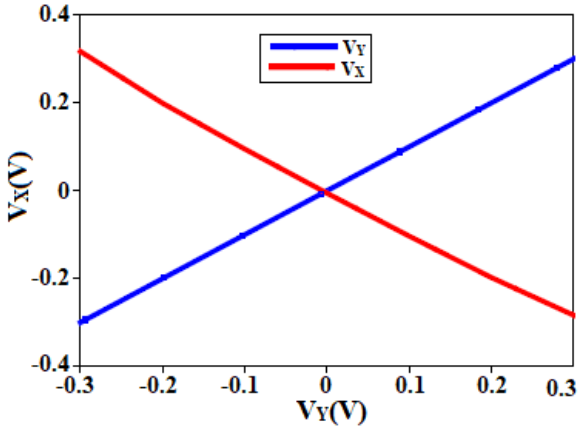
Fig. 2.10 Non-ideal model of ICCTA.

2.3.2 Verification of ICCTA

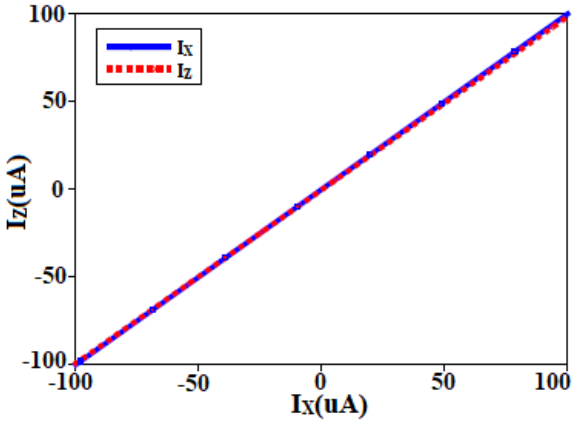
The verification of the CMOS implementation of the ICCTA is conducted using a SPICE simulator with 180 nm technology parameters. Table 2.3 presents the aspect ratios of the MOS transistors used in the CMOS implementation of ICCTA. The power supply voltage is set at ±1.2 V. The bias voltage and bias current of ICCTA are adjusted at 0.42 V and 120 µA respectively. The voltage transfer characteristics of ICCTA from V_Y to V_{X-} are displayed in Fig. 2.11(a). The Fig. 2.11(a) displays the input voltage V_{X-} follows V_Y linearly between -300 mV to 300 mV. Moreover, the direct current transfer from I_{X-} to I_Z is seen in Fig. 2.11(b). It has been observed from Fig. 2.11(b) that the current I_Z follows I_{X-} linearly between -100 µA to 100 µA. Further, The DC transconductance transfer characteristics of the ICCTA from voltage V_Z to currents I_{O+} and I_{O-} are displayed in Fig. 2.11(c). It may be observed in Fig. 2.11(c), current, I_{O+} and I_{O-} is linear for a wide range (-200 mV to 200 mV) of V_Z. Finally, Fig. 2.12 shows the frequency response of the ICCTA for the voltage gain, current gain, and normalized transconductance gain. It can be seen in Fig. 2.12, the voltage gain, current gain, and transconductance gain have constant gain of 1 GHz, 1 GHz, and 200 MHz, respectively.

Table 2.3: Aspect ratio of transistors of ICCTA.

Transistor	W(µm)/ L(µm)
M_1, M_6 - M_8, M_{13}, M_{14}	2.4/0.18
M_2 - M_5	0.67/0.18
M_9 – M_{12}	1.2/0.18
M_{15} – M_{20}	2.15/0.7
M_{21}, M_{22}	5.75/0.7
M_{23} – M_{26}	1.45/0.7



(a)



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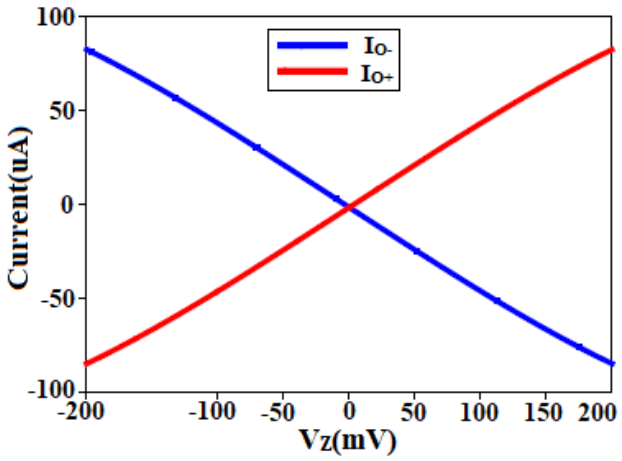


(c)

Fig. 2.11 Port relations of ICCTA. (a) $V_X = -V_Y$, (b) $I_Z = I_X$, and (c) $I_{O\pm} = \pm g_m V_Z$.

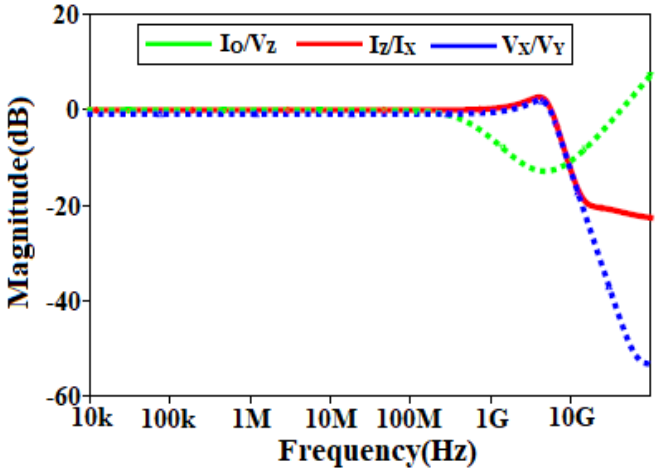


Fig. 2.12 Frequency response of ICCTA.

2.4 Current feedback operational amplifier

Current Feedback Operational Amplifier (CFOA) is one of the most adaptable active elements, has a number of beneficial characteristics such as broad operating frequency range, a high slew rate, and commercial availability (AD844 IC). Additionally, CFOAs with an accessible compensating pin have been found to be highly helpful in implementing circuit solutions with a low component count. The trans linear principle is used for its realization. The idea was described by Barrie Gilbert in 1968. This doctrine states that "Any closed loop that contains an even number of forward-biased junctions arranged such a way that an equal number clockwise facing and anticlockwise facing polarities exist. Then the product of the current densities in both directions must be the same". As a result, there is growing interest in CFOA-based realizations of novel circuits. A wide range of circuits, including filters [215, 216, 217], oscillators [218, 219,

220], square wave generator [221], and PID controller [222] are being built using CFOA. Circuit symbol of CFOA is given in Fig. 2.13. This figure shows that CFOA has four terminals namely Y, X, Z, and W. The voltage at Y terminal is conveyed to X terminal while current fed into X terminal is conveyed to Z terminal. In addition, the voltage at the Z terminal is conveyed to W terminal. The port relations of CFOA are given below as:

$$I_Y = 0; I_X = I_Z;\ V_Y = V_X; \text{and } V_W = V_Z \tag{2.7}$$

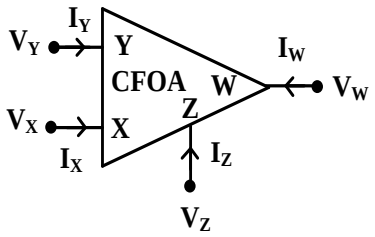


Fig. 2.13 Circuit Symbol of CFOA.

2.4.1 Non-ideal model of CFOA

In practice, the parasitic components are allied with distinct terminals of CFOA show their presence at Y, X, Z and W terminals. Considering parasitic resistance and capacitance associated at terminals Y, X, Z and W as C_Y, R_X, $R_Z \parallel C_Z$ and R_W respectively. The CFOA with parasitic components is shown in the Fig. 2.14 may be expressed as:

$$V_Y = V_Y + R_X I_X; I_Y = sC_Y V_Y; I_Z = I_X + \left(sC_Z + \frac{1}{R_Z}\right) V_Z;\ V_W = V_Z + R_W I_W \tag{2.8}$$

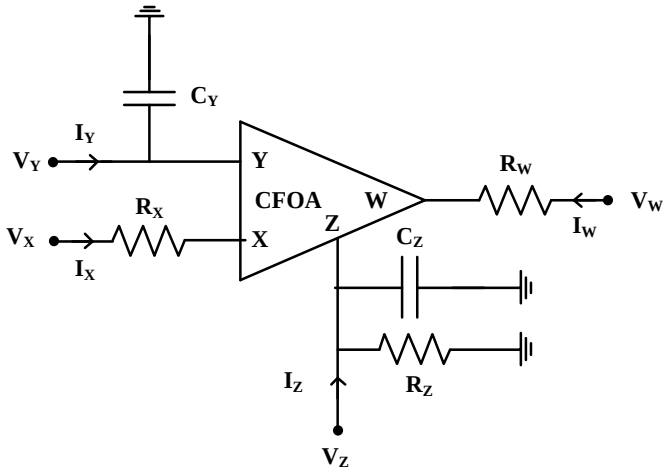
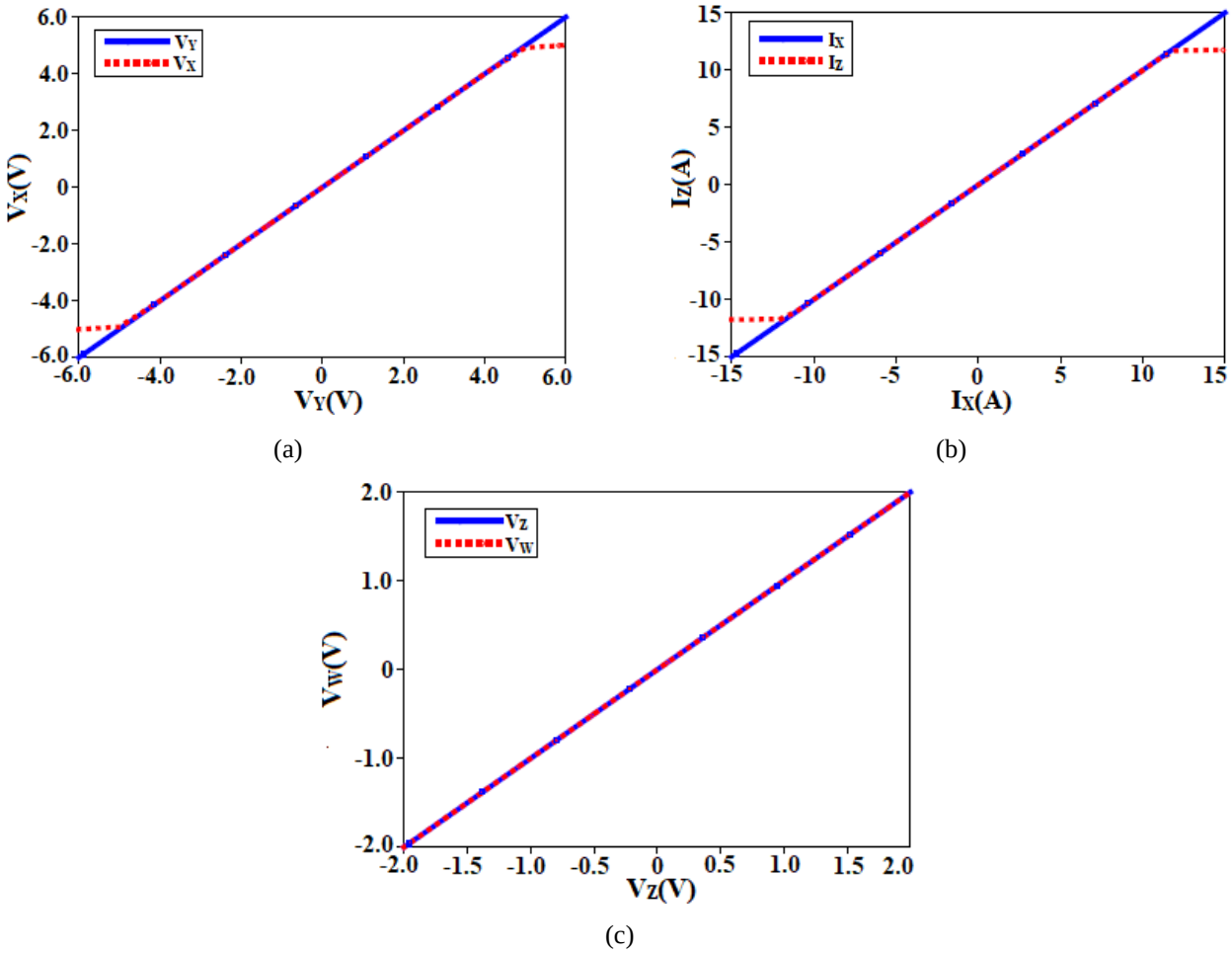


Fig. 2.14 Non-ideal model of CFOA.

2.4.2 Verification of CFOA

The verification of the CFOA is done through SPICE simulator. The power supply of CFOA is selected as ± 5 V. The DC transfer characteristic of CFOA is displayed in Fig. 2.15. Fig. 2.15(a) shows that voltage V_X follows V_Y linearly between -5 V to +5 V.



(a) (b)

(c)

Fig. 2.15 Port relations of CFOA. (a) $V_X = V_Y$, (b) $I_Z = I_X$, and (c) $V_Z = V_W$.

Fig. 2.15(b) displays that current I_Z follows I_X linearly between -11 A to +11 A. Moreover, Fig. 2.15(c) illustrates that voltage V_W follows V_Z linearly between -2 V to +2 V. Next, the frequency response of the CFOA for voltage gain (V_X/V_Y), current gain (I_Z/I_X), and voltage gain (V_W/V_Z) are depicted in Fig. 2.16. It is seen from Fig. 2.16 that the operating frequency range of the V_X/V_Y, I_Z/I_X, and V_W/V_Z are 300 MHz, 300 MHz, and 40 MHz respectively.

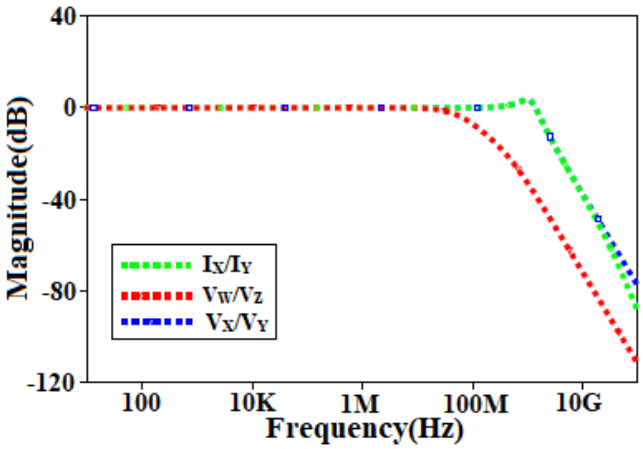


Fig. 2.16 Frequency response of CFOA.

2.5 Summary

This chapter encompasses many commonly used current-mode active building blocks, including the OTA, CCTA, ICCTA, and CFOA. The various analog signal processing circuits presented in chapter 3 to 6 of the thesis are designed using these ABBs. In practice, non-idealities associated with terminals of above ABB deviate the simulated results from theoretical results. Thus, non-idealities associated with OTA, CCTA, ICCTA, and CFOA are also discussed. The CMOS realizations of discussed ABBs will be used throughout the thesis to compare theoretical analysis with simulated results, as was mentioned earlier. In addition, characteristic equations of ABB are verified using SPICE simulator.

CHAPTER 3

INTEGER ORDER IMMITTANCE EMULATORS

In chapter 2, different types of analog building blocks are discussed. This chapter describes proposed grounded and floating immittance emulators based on Current Conveyor Transconductance Amplifier (CCTA). The emulators can realize both positive and negative floating immittances through appropriate setting of switches. These emulators have attractive featuring of electronic tuning of immittance via bias current. Moreover, there is no matching constraint imposed for realizing the functionality. The usefulness proposed immittance circuits is also illustrated with filter, inductance, and capacitance cancellation circuits.

In addition, Current Feedback Operational Amplifier (CFOA) based lossless grounded impedance multiplier circuit is also put forward. Suitable choice of passive components enables proposal to emulate grounded capacitance multiplier, grounded inductance multiplier, frequency dependent negative resistor, and grounded resistance divider circuit. The non-ideal analysis of the proposed circuits is mathematically modelled. In addition, the performance of the proposed circuit examines PVT variation. The Monte Carlo study is also performed to analyze robustness of the proposals against variations in the passive components.

3.1 Proposed grounded integer order immittance circuit

The proposed grounded integer order immittance is shown in Fig. 3.1. It is designed using single CCTA, two impedances (Z_R and Z_Q) and two MOS based switches (S_1 and S_2). The circuit under consideration operates in both positive and negative modes by utilizing PMOS and NMOS switches linked to terminals $0+$ and $0-$ of the CCTAs, respectively.

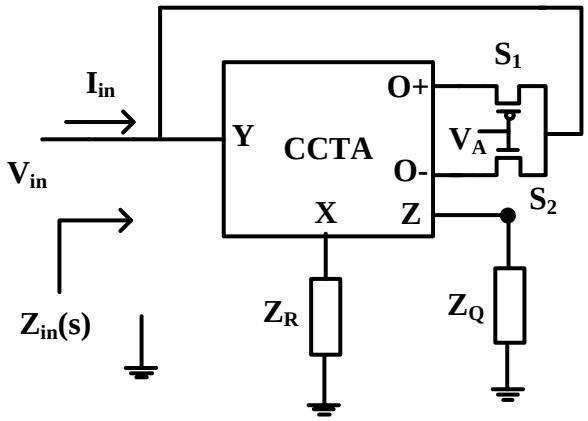


Fig. 3.1 Proposed CCTA based grounded immittance circuit.

The selection of the switch is determined by the voltage (V_A) applied to the gate terminal of the MOS switch. When the voltage V_A is high, the NMOS switch turns on, allowing the establishment of a conducting connection between the O- and Y terminals of the CCTA.

Simultaneously, the PMOS is turned off, thereby disconnecting the connection between O+ and Y terminals of CCTA is disconnected. Consequently, the input impedance of Fig. 3.1 is determined as:

$$Z_{in}(s) = \left(\frac{V_{in}}{I_{in}}\right) = +\left(\frac{Z_R}{Z_Q g_m}\right) \tag{3.1}$$

Equation (3.1) demonstrates that the circuit under consideration operates in positive mode and can offer different impedances with the appropriate selection of components (Z_R and Z_Q). Further, the impedance value can be adjusted by changing g_m.

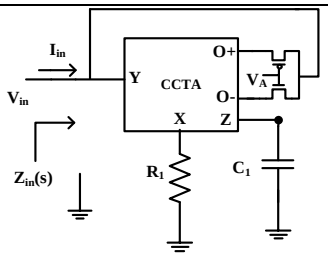
In a similar manner, when the voltage V_A is "low", the PMOS switch (S_1), establishes a conducting pathway between the O+ and Y terminals of CCTA. Simultaneously, the NMOS switch (S_2) is turned off. So, the connection between O- and Y terminals of CCTA does not exist. The expression for the input impedance of the proposed grounded immittance circuit is derived as:

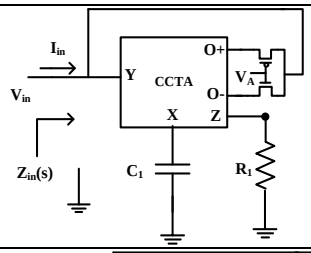
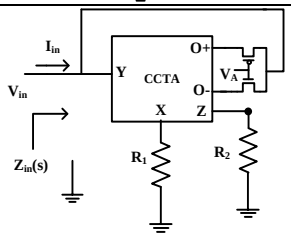
$$Z_{in}(s) = \left(\frac{V_{in}}{I_{in}}\right) = -\left(\frac{Z_R}{Z_Q g_m}\right) \tag{3.2}$$

Equation (3.2) highlights that the circuit under consideration operates in a negative mode and can offer adjustable immittance through the appropriate selection of components (Z_R and Z_Q).

It is clear from eqs. (3.1) and (3.2) that the appropriate choice of Z_R and Z_Q leads to distinct input impedances. Table 3.1 lists the choices of Z_R and Z_Q resulting input impedance and its magnitude. It is worth noting that the input impedance may be altered by modifying the bias current value of the CCTA. Moreover, the magnitude is unity for sensitivity against component variation for all choices of (Z_R and Z_Q).

Table 3.1 Different configurations of the proposed CCTA based grounded immittance**.**

Configuration	Selection of components	Switch Setting	Equivalent Input Impedance ($Z_{in}(s)$)	Equivalent Input Impedance magnitude	Schematic of the Configuration	Sensitivity
Inductor	$Z_Q = \frac{1}{sC_1}$; $Z_R = R_1$	$V_A = H$	$+\frac{sR_1C_1}{g_m}$	$L_{eq} = +\frac{R_1C_1}{g_m}$		$s^{\lvert L_{eq}\rvert}_{C_1} = s^{\lvert L_{eq}\rvert}_{R_1} = -s^{\lvert L_{eq}\rvert}_{g_m} = 1$
		$V_A = L$	$-\frac{sR_1C_1}{g_m}$	$L_{eq} = -\frac{R_1C_1}{g_m}$		

Configuration	Selection of components	Switch Setting	Equivalent Input Impedance ($Z_{in}(s)$)	Equivalent Input Impedance magnitude	Schematic of the Configuration	Sensitivity
Capacitor	$Z_R = \frac{1}{sC_1}; Z_Q = R_1$	$V_A = H$	$+\frac{1}{sR_1C_1g_m}$	$C_{eq} = +R_1C_1g_m$		$S_{C_1}^{\lvert C_{eq}\rvert} = S_{R_1}^{\lvert C_{eq}\rvert} = S_{g_m}^{\lvert C_{eq}\rvert} = 1$
		$V_A = L$	$-\frac{1}{sR_1C_1g_m}$	$C_{eq} = -R_1C_1g_m$		
Resistor	$Z_R = R_1$; $Z_Q = R_2$	$V_A = H$	$+\frac{R_1}{R_2g_m}$	$R_{eq} = +\frac{R_1}{R_2g_m}$		$-S_{R_2}^{\lvert R_{eq}\rvert} = S_{R_1}^{\lvert R_{eq}\rvert} = -S_{g_m}^{\lvert R_{eq}\rvert} = 1$
		$V_A = L$	$-\frac{R_1}{R_2g_m}$	$R_{eq} = -\frac{R_1}{R_2g_m}$		
L- Low; H – High.						

3.1.2 Non-ideal Analysis

Taking non-ideal effects present in CCTA (section 2.2.1) the immittance circuit of Fig. 3.1 may be redrawn as Fig 3.2.

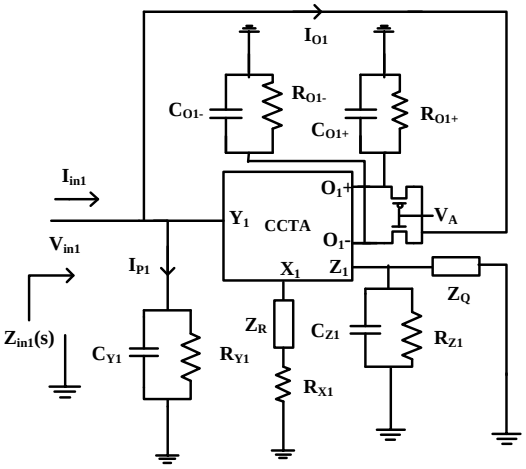


Fig. 3.2 Proposed grounded immittance circuit with parasitic components.

Current flows through terminal X_1 may be expressed as

$$I_{X1} = \frac{-V_{in}}{Z_R + R_{X1}} \tag{3.3}$$

Now, voltage at Z_1 terminal may be written as:

$$V_{Z1} = \frac{V_{in}}{(Z_R + R_{X1})} \left\{ \frac{Z_Q}{Z_Q\left(sC_{Z1} + \frac{1}{R_{Z1}}\right) + 1} \right\} \tag{3.4}$$

Further, input current (I_{in}) may be obtained by applying KCL at Y_1 terminal of Fig. 3.2 as:

$$I_{in} = \frac{V_{in}}{Z_{P1}} \pm g_m V_{Z1} \tag{3.5}$$

where $Z_P = \left(R_{O1-/O1+} \parallel R_Y\right) \parallel \frac{1}{s(C_{O1-/O1+}+C_Y)} = R_P \parallel \frac{1}{sC_P} = \frac{1}{\frac{1}{R_P}+sC_P}$. where $R_P = \left(R_{O1-/O1+} \parallel R_Y\right)$ and $C_P = \left(C_{O1-/O1+} + C_Y\right)$. Substituting the value of V_{Z1} in eq. (3.5), the input admittance of the of Fig. 3.2 is computed as:

$$Y_{in} = \frac{I_{in}}{V_{in}} = \frac{1}{R_P} + sC_P \pm \frac{g_m}{(Z_R+R_{X1})}\left\{\frac{Z_Q}{Z_Q\left(sC_{Z1}+\frac{1}{R_{Z1}}\right)+1}\right\} \tag{3.6}$$

The value of C_P, C_{Z1}, $\frac{1}{R_{Z1}}$, and $\frac{1}{R_P}$ are low, and if the value of $(R_{X1}) \ll (|Z_R|)$. Then, eq. (3.6) is reduced to their corresponding ideal counter parts eq. (3.1) and eq. (3.2).

Positive Immittance: $$Z_{in}(s) = \frac{V_{in}}{I_{in}} = +\frac{Z_R}{g_m Z_Q} \tag{3.7}$$

Negative Immittance: $$Z_{in}(s) = \frac{V_{in}}{I_{in}} = -\frac{Z_R}{g_m Z_Q} \tag{3.8}$$

3.1.3 Results and discussion

To validate the theoretical aspects of proposed grounded immittances, SPICE simulations are carried out with 0.18 µm technology parameter. The aspect ratio of MOS transistors of CCTA (Fig. 2.5(b)) namely M_{1-2}, M_{3-4}, M_{5-7}, M_{8-9}, M_{10-15}, M_{16-17}, and M_{18-21} is $\frac{2.4\ \mu m}{0.18\ \mu m}$, $\frac{0.67\ \mu m}{0.18\ \mu m}$, $\frac{2.4\ \mu m}{0.18\ \mu m}$, $\frac{0.36\ \mu m}{0.18\ \mu m}$, $\frac{40\ \mu m}{1\ \mu m}$, $\frac{40\ \mu m}{0.6\ \mu m}$ and $\frac{40\ \mu m}{1\ \mu m}$ respectively. The supply voltage and bias voltage of CCTA are taken as ±1.5 V and +0.42 V respectively. Post layout simulations are also performed to observe the circuit behavior after fabrication. The CCTA schematic of Fig. 2.5 is laid down using Microwind software is shown in Fig. 3.3. It occupies 51.9 ×55.5 µm^2 area. The frequency response of the proposed immittance emulator is obtained for component values and bias current enlisted in Table 3.2.

Table 3.2 Active grounded immittances value with respect component value and bias current ($I_B = 200\ \mu A$)**.**

S. N.	Nature of immittance	Component Value	Immittance Value	Operating frequency range of immittance; Input Phase
1	Negative resistor	R_1=R_2=1kΩ	Req=-1.1kΩ	NA; -180°
2	Negative integer order inductor	R_1=1kΩ, C_1=1nF	Leq=-1.1mH	10kHz – 10MHz; -90°
3	Positive integer order inductor	R_1=1 kΩ, C_1=1nF	Leq=1.1mH	10kHz – 10MHz; +90°
4	Negative integer order capacitor	C_1=0.5nF, R_1=1 kΩ	Ceq=-1.9nF	3kHz – 1MHz; +90°

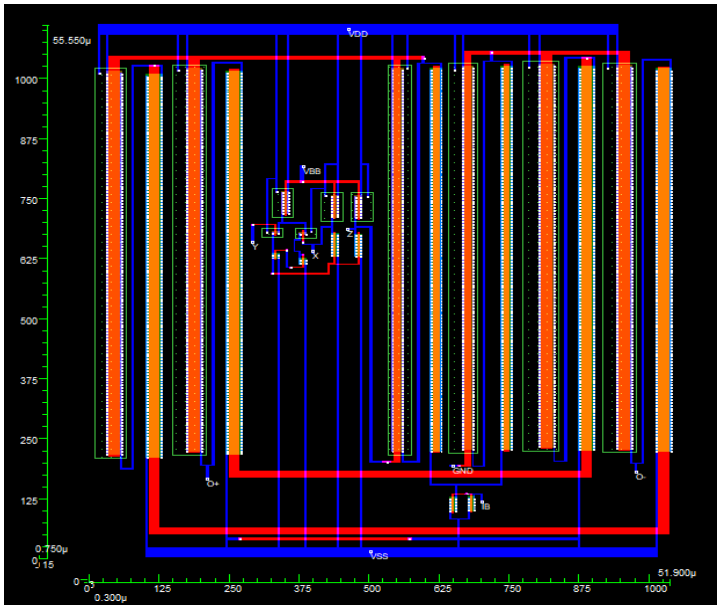
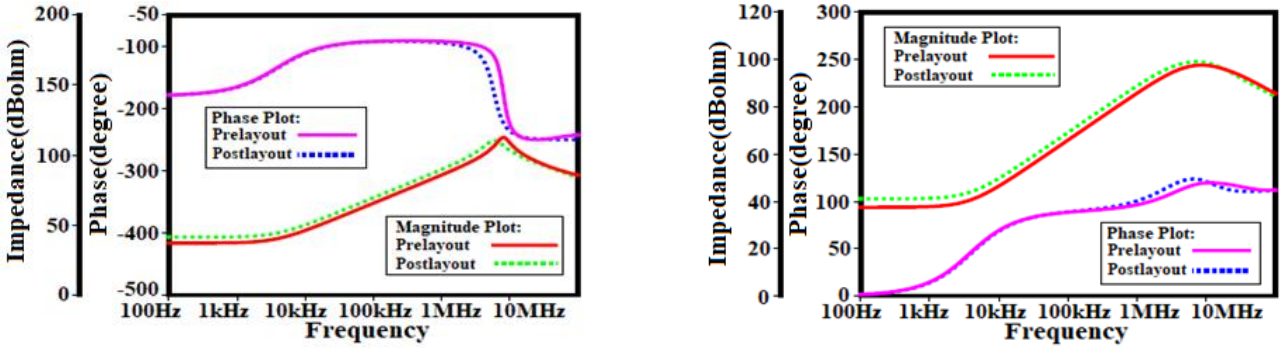


Fig. 3.3 Layout of grounded immittance.

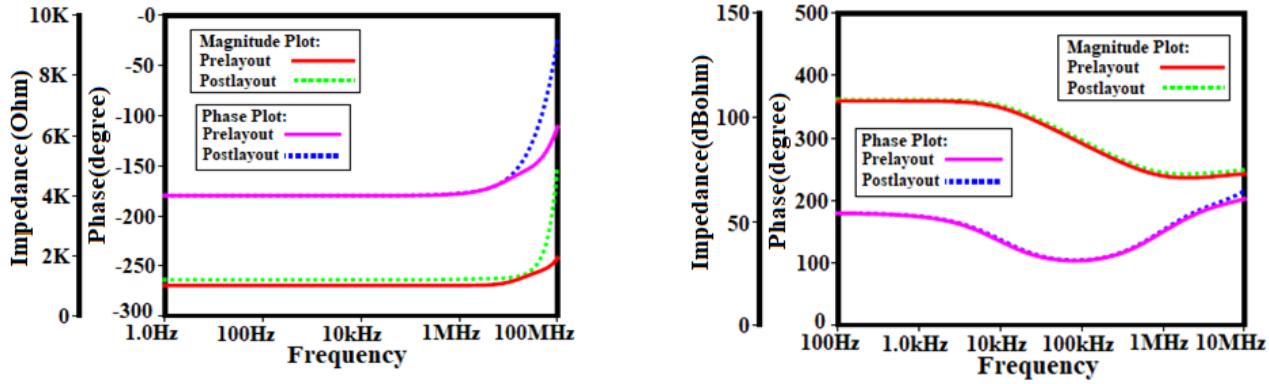
Figures 3.4(a) and 3.4(b) show the frequency responses of the input impedance of the suggested integer order positive and negative inductors respectively. It is noteworthy to mention that there exists a close match between the pre layout and post layout simulations over the frequency spectrum of 10 kHz to 10 MHz. Figure 3.5(a) shows that the circuit works well for the proposed grounded negative resistor. The input resistance and phase don't change when the frequency is changed from 1 Hz to 100 MHz. Further, the input impedance of the proposed grounded negative capacitor is shown in Fig. 3.5(b). Figure 3.5(b) confirms that the circuit exhibits good performance between 3 kHz to 1 MHz for proposed negative capacitor. The observations are summarized in Table 3.2 along with immittance value and input phase. Power dissipation of the grounded immittance circuit is 1.37 mW. A Monte Carlo study is conducted with 500 iterations, where a Gaussian deviation of 10% is applied to the passive component. The purpose is to investigate the impact of the deviation in the passive element on the frequency response of the proposed grounded inductor, as illustrated in Fig. 3.6(a). From Fig. 3.6(a), it is evident that the suggested grounded inductor exhibits a variation in magnitude of ±1.2 dB. Temperature is an environmental factor that affects the mobility of charge carrier, threshold voltage and saturation velocity [205] which affects the drain current in integrated circuit. So, it is necessary to analyses the temperature effect of proposed circuit. Figure 3.6(b) shows frequency response of proposed grounded inductor at different temperature (-45°C to 90°C) that show 5.06 dB change in input impedance effect of temperature. Fluctuation in supply voltage may affect the performance of the

integrated circuit. Hence, Fig. 3.7(a) shows the frequency response of proposed grounded inductor at different supply voltage (±1.35 V to ±1.65 V) that show 6.5 dB variation in input impedance. Corner analysis is conducted to assess the sensitivity characteristics of the proposed grounded inductor circuit. The Fig. 3.7(b) presents the corner analysis of the suggested grounded inductor circuit for the Fast-Fast (FF) corner, Normal-Normal (NN) corner, and Slow-Slow (SS) corner. These responses are achieved by changing the temperature and supply within the range of -45°C to 90°C and ±1.35 V to ±1.65 V correspondingly. Figure 3.7(b) illustrates that the input impedance of a grounded inductor is lower in the FF corner compared to the SS corner due to a larger current flow in the FF corner.



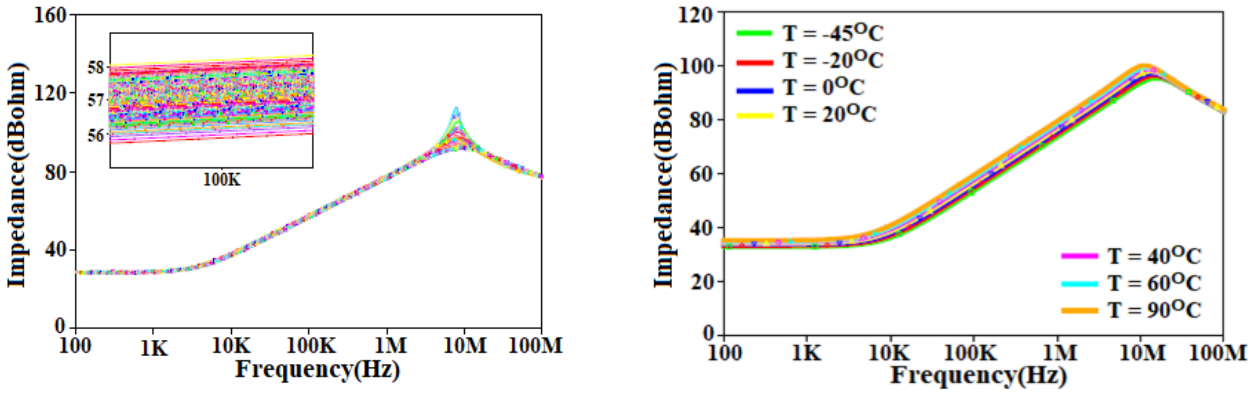
(a) (b)

Fig. 3.4 Frequency response of proposed grounded integer order (a) negative inductor, and (b) positive inductor.



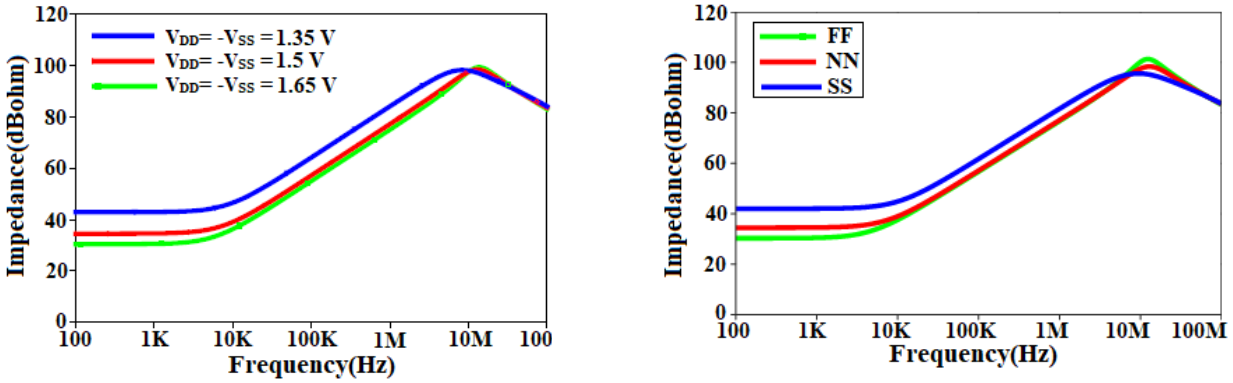
(a) (b)

Fig. 3.5 Frequency response of proposed grounded (a) negative resistor, and (b) negative capacitor.



(a) (b)

Fig. 3.6 Magnitude response of proposed grounded inductor for variation in (a) passive components, and (b) temparatures.



(a) (b)

Fig. 3.7 Magnitude response of proposed grounded inductor for variation in (a) supply voltages, and (b) corner analysis.

3.1.4 Application

A 2nd order current mode multi-function filter circuit is constructed using proposed grounded capacitance circuit, grounded resistance circuit, grounded inductor circuit and the same is depicted in Fig. 3.8.

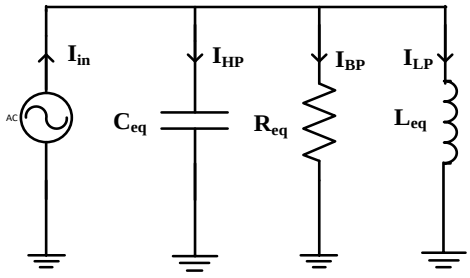


Fig. 3.8 2nd order current mode multi-function filter circuit.

The transfer function for the Band Pass Filter (BPF), Low Pass Filter (LPF) and High Pass Filter (HPF) are given as:

$$\frac{I_{BPF}}{I_{in}} = \frac{\frac{s}{R_{eq}C_{eq}}}{s^2+\frac{s}{R_{eq}C_{eq}}+\frac{1}{L_{eq}C_{eq}}} \quad (3.9)$$

$$\frac{I_{LPF}}{I_{in}} = \frac{\frac{1}{L_{eq}C_{eq}}}{s^2+\frac{s}{R_{eq}C_{eq}}+\frac{1}{L_{eq}C_{eq}}} \quad (3.10)$$

$$\frac{I_{HPF}}{I_{in}} = \frac{s^2}{s^2+\frac{s}{R_{eq}C_{eq}}+\frac{1}{L_{eq}C_{eq}}} \quad (3.11)$$

The angular frequency (ω_o) and quality factor (Q_O) of band pass filter circuit are obtained as:

$$\omega_o = \sqrt{\frac{1}{L_{eq}C_{eq}}} \quad (3.12)$$

$$Q_O = R_{eq}\sqrt{\frac{C_{eq}}{L_{eq}}} \quad (3.13)$$

$$\frac{\omega_o}{Q_O} = \frac{R_{eq}}{L_{eq}} \quad (3.14)$$

It is observed from eq. (3.12) to eq. (3.14) that angular frequency and quality factor may be varied orthogonally via R_{eq}. The functionality of current mode 2nd order band pass filter, low pass filter and high pass filter responses are verified using component values: L_{eq}= 1.1 mH, C_{eq} = 1 nF, and R_{eq}= 1.1 kΩ,. Theoretical and simulated current gain response of multi-function filter is displayed in Fig. 3.9.

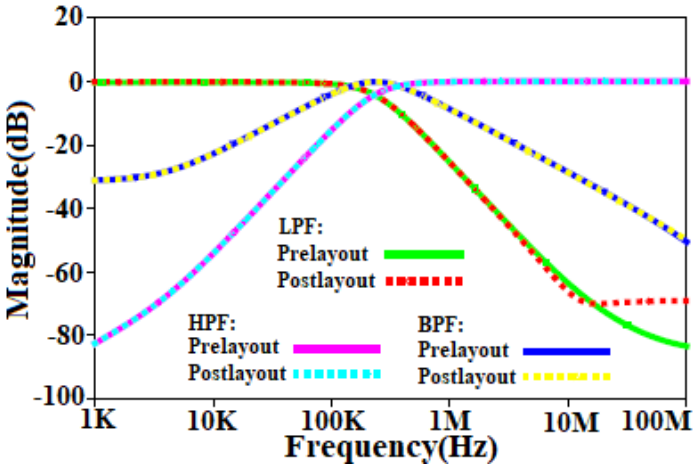


Fig. 3.9 Frequency response of current mode 2nd order multi-function filter.

It is seen from Fig. 3.9 that the center frequency and quality factor of band pass filter is 151.825 kHz and 1.05 respectively. It is also seen from Fig. 3.9 that deviation between pre layout and post layout of filter responses at high frequency due to parasitic components associated with the terminals of CCTA.

3.2 Proposed floating integer order immittance circuits

In this section two floating integer order immittance emulators are proposed. Both circuits use two CCTAs as ABB and four MOS switches. The first circuit uses three passive components while the second circuit employs two passive components.

3.2.1 Proposed floating immittance circuit 1

The proposed floating integer order immittance circuit is depicted in Fig.3.10. The design circuit incorporates a single active block CCTA, together three impedances denoted as Z_1, Z_2 and Z_3. Additionally, four switches based on Metal-Oxide-Semiconductor (MOS) technology, namely S_1, S_2, S_3 and S_4, are included in the design.

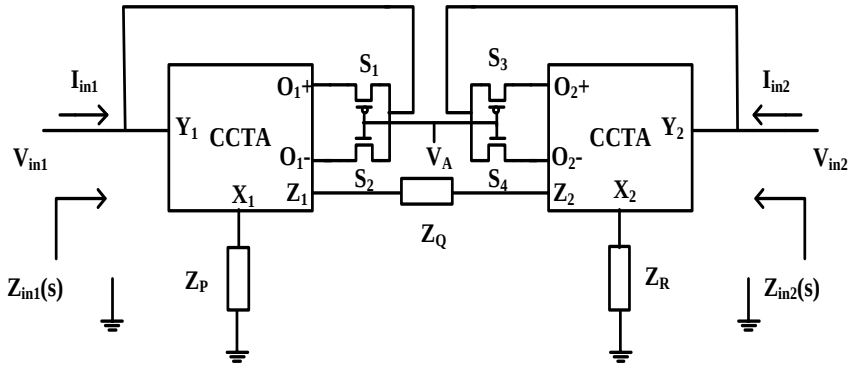


Fig. 3.10 Proposed floating immittance circuit 1.

The choice of the switch is contingent upon the voltage applied to the gate terminal of the MOS switch. When the voltage (V_A) is "high", the switches S_2 and S_4 are activated. This enables the construction of a conductive pathway between the O- and Y terminals of the CCTAs. Concurrently, S_1 and S_3 are deactivated, the linkage between the O+ and Y terminals of the CCTAs is interrupted. Therefore, the input impedance of the proposed floating circuit may be obtained as:

$$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = +\left(\frac{Z_P+Z_R}{Z_Q g_m}\right) \tag{3.15}$$

Equation (3.15) exemplifies the operational characteristics of the analyzed circuit in the positive mode and can offer different impedances with the appropriate selection of components $(Z_P, Z_Q, \text{and}, Z_R)$.

In a comparable fashion, when the V_A is "low", the switches S_1 and S_3 are activated, allowing the establishment of a conducting connection between the O+ and Y terminals of the CCTAs.

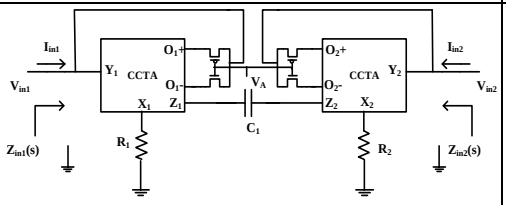
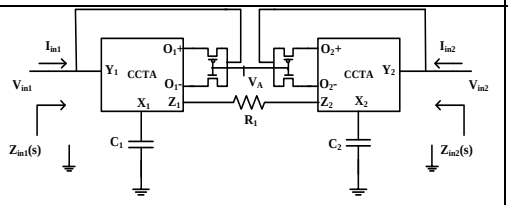
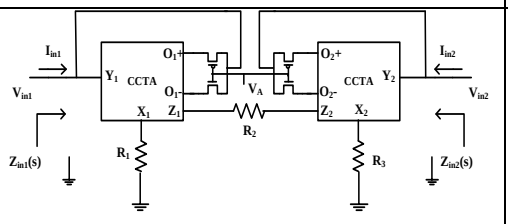
Concurrently, S_2 and S_4 are deactivated, the path between the O- and Y terminals of the CCTAs breaks the input impedance of the floating circuit can be deduced as:

$$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = -\left(\frac{Z_P+Z_R}{Z_Q g_m}\right) \quad (3.16)$$

Equation (3.16) elucidates that the circuit being examined functions in a negative mode and possesses the capacity to provide adjustable immittance by appropriately selection of components $(Z_P, Z_Q, \text{and}, Z_R)$.

Equations (3.15) and (3.16) clearly indicate that selecting the proper values for $Z_P, Z_Q, \text{and}, Z_R$ will result in different input impedances. Table 3.1 lists the choices of Z_R and Z_Q resulting input impedance and its magnitude. It is important to mention that the input impedance may be modified by varying the bias current value of the CCTA. Furthermore, the sensitivity against passive component for all possible choices of $Z_P, Z_Q, \text{and}, Z_R$ is also mentioned in Table 3.3.

Table 3.3 Different configurations of the proposed CCTA based floating immittance circuit**.**

Configuration	Selection of components	Switch Setting	Equivalent Input Impedance $(Z_{in}(s))$	Equivalent Input Impedance magnitude	Schematic of the Configuration	Sensitivity
Inductor	$Z_Q = \frac{1}{sC_1}; Z_P = R_1; Z_R = R_2$	V_A = H	$+\left(\frac{s(R_1+R_2)C_1}{g_m}\right)$	$L_{eq} = +\frac{(R_1+R_2)C_1}{g_m}$		$S_{C_1}^{\lvert L_{eq}\rvert} = -S_{g_m}^{\lvert L_{eq}\rvert} = 1$ $S_{R_{1/2}}^{\lvert L_{eq}\rvert} = \frac{R_{1/2}}{R_1+R_2}$
		V_A = L	$-\left(\frac{s(R_1+R_2)C_1}{g_m}\right)$	$L_{eq} = -\frac{(R_1+R_2)C_1}{g_m}$		
Capacitor	$Z_P = \frac{1}{sC_1}; Z_Q = R_1; Z_R = \frac{1}{sC_2}$	V_A = H	$+\frac{1}{sR_1(C_1+C_2)g_m}$	$C_{eq} = +R_1(C_1+C_2)g_m$		$S_{R_1}^{\lvert C_{eq}\rvert} = S_{g_m}^{\lvert C_{eq}\rvert} = 1$ $S_{C_{1/2}}^{\lvert C_{eq}\rvert} = \frac{C_{1/2}}{C_1+C_2}$
		V_A = L	$-\frac{1}{sR_1(C_1+C_2)g_m}$	$C_{eq} = -R_1(C_1+C_2)g_m$		
Resistor	$Z_P = R_1; Z_Q = R_2; Z_R = R_3$	V_A = H	$+\frac{(R_1+R_3)}{R_2 g_m}$	$R_{eq} = +\frac{(R_1+R_3)}{R_2 g_m}$		$-S_{R_2}^{\lvert R_{eq}\rvert} = -S_{g_m}^{\lvert R_{eq}\rvert} = 1$ $S_{R_{1/3}}^{\lvert R_{eq}\rvert} = \frac{R_{1/3}}{R_1+R_3}$
		V_A = L	$-\frac{(R_1+R_3)}{R_2 g_m}$	$R_{eq} = -\frac{(R_1+R_3)}{R_2 g_m}$		
L- Low; H – High.						

3.2.1.1 Non-ideal analysis

Considering the nonidealities of CCTA given in chapter 2, the circuit of Fig. 3.10 modifies to Fig. 3.11.

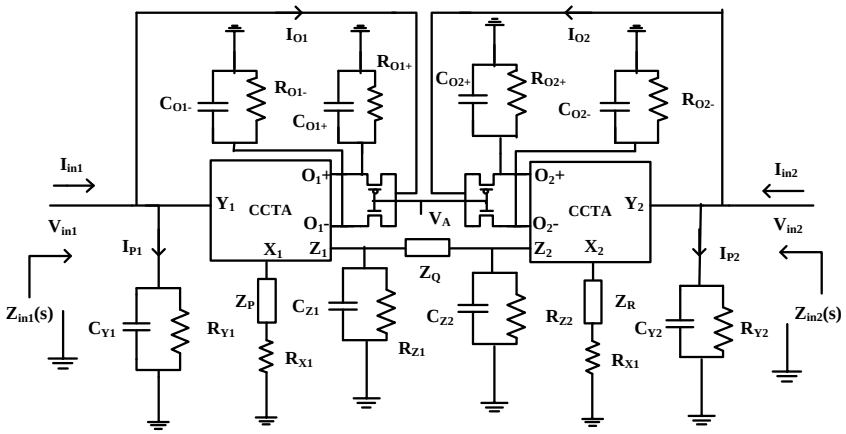


Fig. 3.11 Proposed floating immittance circuit 1 with parasitic components.

Now, input admittance of the floating immittance circuit with parasitic components may be expressed as:

$$Y_{in}(s) = \left(\frac{I_{in1}-I_{in2}}{V_{in1}-V_{in2}}\right) = \frac{1}{R_P} + sC_P \pm \frac{g_m Z_Q}{(R_{X1}+R_{X2}+Z_p+Z_R)} \tag{3.17}$$

where $R_P = \left(R_{O1-/O1+} \parallel R_Y\right)$ and $C_P = \left(C_{O1-/O1+} + C_Y\right)$. The value of C_P, and $\frac{1}{R_P}$ are low, and $(R_{X1} + R_{X2}) \ll \left(|Z_p| + |Z_R|\right)$. Then, eq. (3.17) is reduced to their corresponding ideal counter parts eq. (3.15) and eq. (3.16).

Positive Immittance: $$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = +\left(\frac{Z_P+Z_R}{Z_Q g_m}\right) \tag{3.18}$$

Negative Immittance: $$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = -\left(\frac{Z_P+Z_R}{Z_Q g_m}\right) \tag{3.19}$$

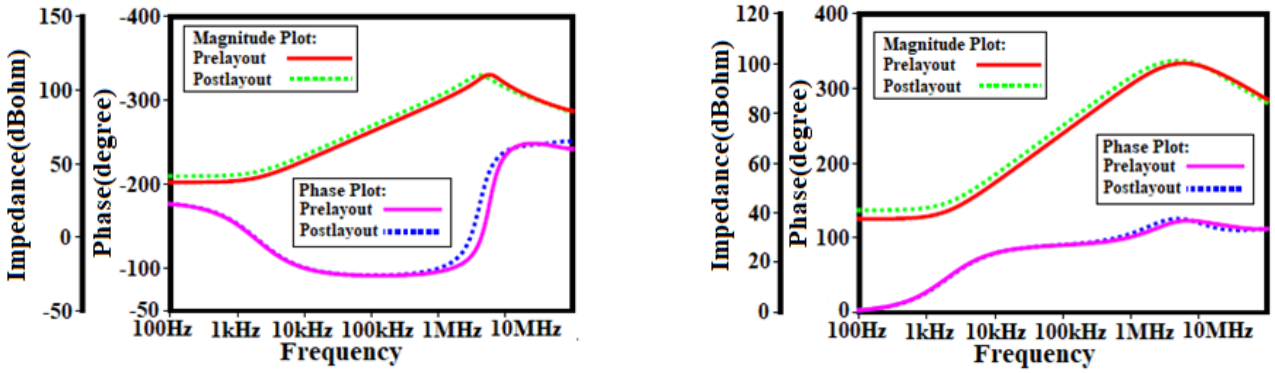
3.2.1.2 Results and discussion

The theoretical aspects of the designed floating immittance circuits are demonstrated using SPICE simulation through 180 nm CMOS technology parameter. The supply voltage and bias voltage of CCTA are taken as ±1.5 V and +0.42 V respectively. The suggested floating immittances are characterized by SPICE simulations using the component values specified in Table 3.4.

Table 3.4 Active floating immittances value with respect component values and bias current ($I_B = 200\mu A$).

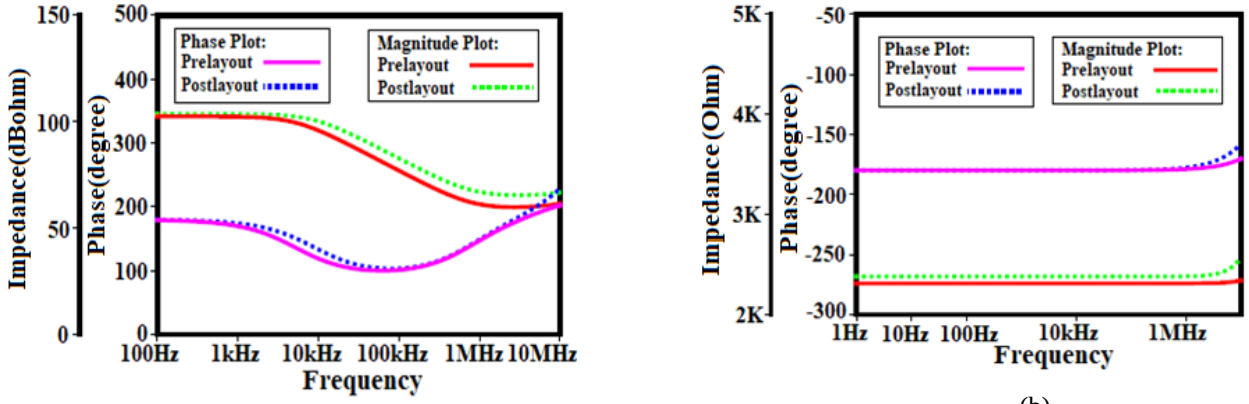
S.N.	Nature of immittance	Component Value	Immittance Value	Operating frequency range of immittance; Input phase
1.	Negative resistor	$R_1=R_2=R_3=1k\Omega$	Req=-2.3kΩ	NA; -180°
2.	Negative integer order inductor	$R_1=R_2=1k\Omega$, $C_1=1nF$	Leq=-2mH	4kHz – 8MHz; -90°
3.	Positive integer order inductor	$R_1=R_2=1k\Omega$, $C_1=1nF$	Leq=2mH	4kHz – 8MHz; +90°
4.	Negative integer order capacitor	$C_1=C_2=1nF$, $R_1=1.8\ k\Omega$	Ceq=-3.6nF	3kHz – 1MHz; +90°

The frequency response of the input impedance of the suggested negative and positive floating inductor is illustrated in Fig. 3.12(a) and Fig. 3.12(b) correspondingly. It is worth noting that theoretical and simulated values closely match within the frequency range of 4 kHz to 8 MHz.



(a) (b)

Fig. 3.12 Frequency response of proposed floating inductor (a) negative, and (b) positive.

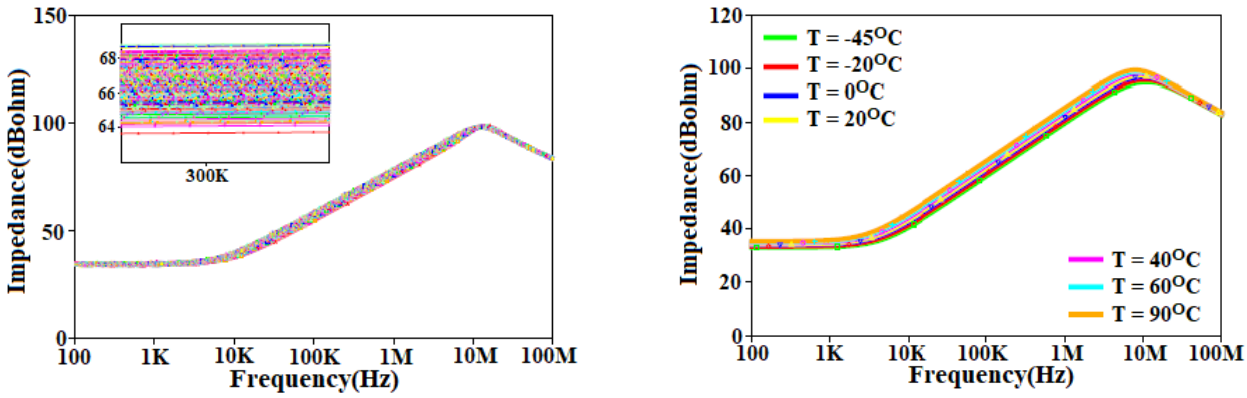


(a) (b)

Fig. 3.13 Frequency response of proposed floating (a) negative capacitor, and (b) negative resistor.

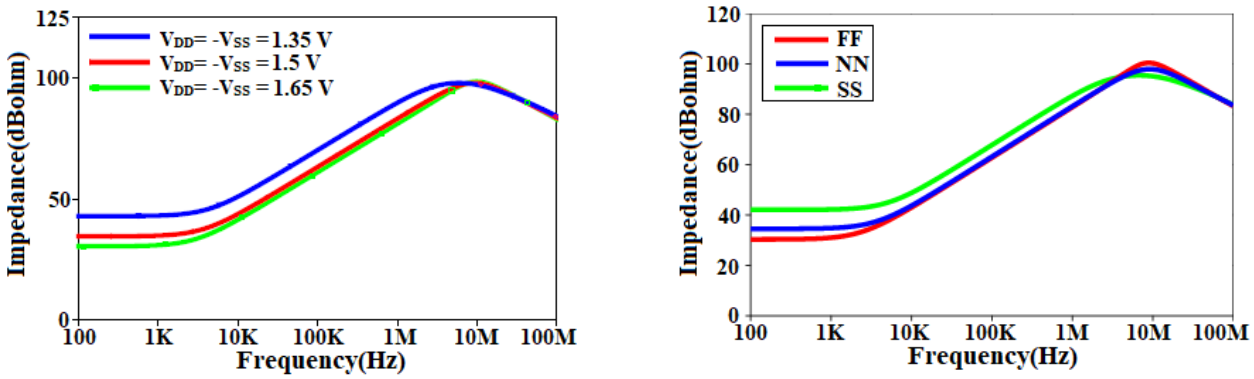
Additionally, the input impedance of the suggested floating negative capacitor is illustrated in Fig. 3.13(a). The results presented in Fig. 3.13(a) provide evidence of the circuit's favorable

performance within the frequency range of 3 kHz to 1 MHz, as observed for the negative capacitor proposed in this study. Fig. 3.13(b) depicts the frequency response of the negative floating resistors. It is noticed that the input impedance and phase remain unaffected by the input frequency within the range of 1 Hz to 20 MHz. The observations are summarized in Table 3.4 along with immittance value and input phase. Power dissipation of the grounded immittance circuit is 3.57 mW Further, the effect of variation in the value of the component on the performance of the floating inductor is displayed in Fig. 3.14(a). This response is obtained by performing Monte Carlo analysis for 500 runs with 10% tolerance in passive components. It is seen from Fig. 3.14(a) that deviation in magnitude response of the proposed inductor is approximately ±2.2 dB. Impact of temperature variations on frequency response of the floating inductor is also studied by varying temperature from -45°C to 90°C and the overall spread in input impedance is found to be within 5.08 dB as shown in Fig. 3.14(b). In practice, the performance of the floating inductor may vary due to supply voltage variations. The frequency response of the floating inductor is plotted in Fig. 3.15(a) by varying supply from ±1.35 V to ±1.65 V and the variation of 6.45 dB is observed in the input impedance. Corner analysis of the floating inductor circuit for Fast-Fast (FF) corner, the Normal-Normal (NN) corner, and the Slow-Slow (SS) corner is depicted in Fig. 3.15(b). It is obtained by changing the temperature and supply from -45°C to 90°C and from ±1.35 V to ±1.65 V. Figure 3.15(b) displays that the input impedance of a floating inductor is lower in the FF corner than in the SS corner.



(a) (b)

Fig. 3.14 Magnitude response of proposed grounded inductor for variation in (a) passive components, and (b) temparatures.



(a) (b)

Fig. 3.15 Magnitude response of proposed grounded inductor for variation in (a) supply voltages, and (b) corner analysis.

3.2.1.3 Application

Application of negative floating inductor can be examined as an inductance compensation, which plays a major role for the cancellation of any unwanted inductance present in electronic circuit. An inductance cancellation circuit using the proposed floating negative inductor ($L_{FLOATING}$=-2mH) and the grounded positive inductor (L=2mH) as shown in Fig. 3.16. Here, the passive component R is chosen as 1kΩ, the circuit is excited with a sinusoidal input signal of amplitude of 40 mV and 10 kHz frequency. The transient response for the circuit shown in Fig. 3.17. It is noted that output is in phase with input signal, thereby confirming the cancelation of positive inductor by using negative inductance and making the circuit resistive.

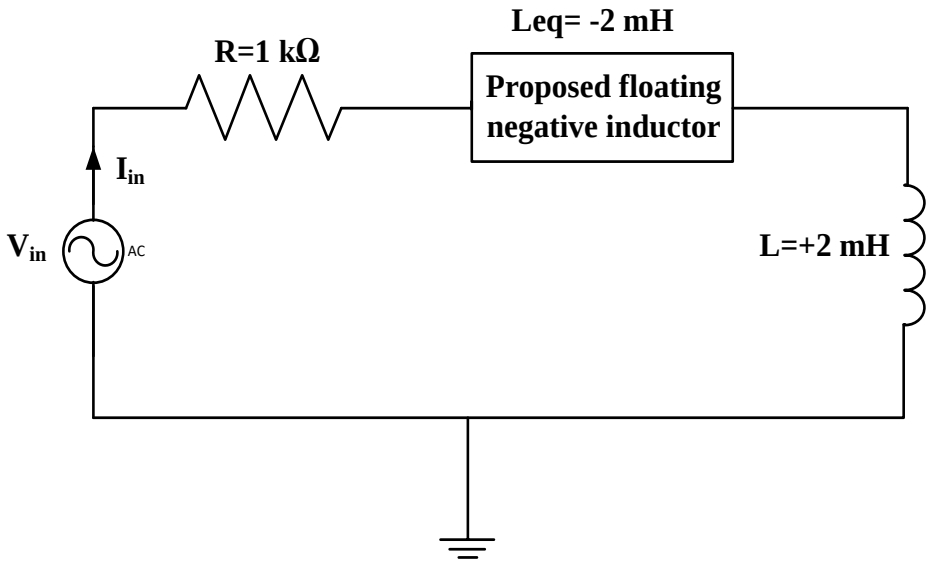


Fig. 3.16 Inductance cancellation using proposed inductor.

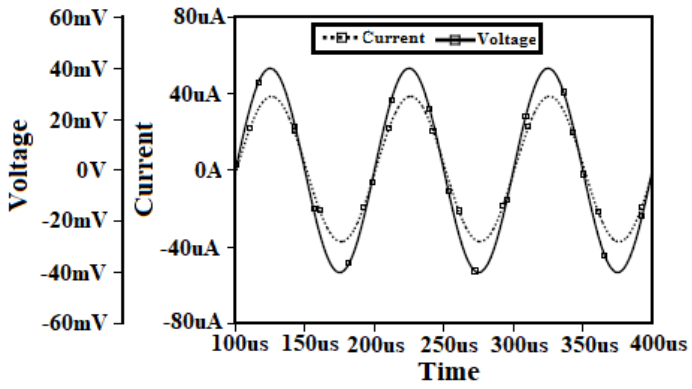


Fig. 3.17 Transient response of the inductance cancellation.

3.2.2 Proposed floating immittance circuit 2

The proposed CCTA based floating immittance topology using two CCTAs, two components (Z_R and Z_Q) and four MOS based switches (S_1, S_2, S_3, and S_4) is shown in Fig. 3.18. The proposed circuit works in positive and negative mode using PMOS and NMOS switch connected at terminal $O+$ and $O-$ terminal of CCTAs, respectively.

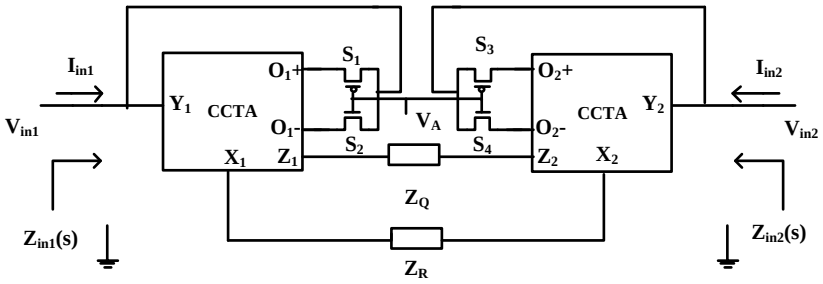


Fig. 3.18 Proposed CCTA based floating immittance circuit 2.

The switch selection is based on the applied voltage (V_A) at gate terminal of MOS switch. When V_A is high, NMOS switches (S_2 and S_4) are turned ON, providing a conducting path between O- and Y terminals of CCTAs. At the same time PMOS switches (S_1 and S_3) are turned OFF, disconnecting the path between O+ and Y terminals of CCTAs. The input impedance of the floating circuit is obtained as:

$$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = -\left(\frac{Z_R}{Z_Q g_m}\right) \tag{3.20}$$

Equation (3.20) shows that the proposed circuit works in negative mode and is capable to provides negative tunable impedances by proper selection of Z_R and Z_Q components. Similarly, when V_A is low, PMOS switches (S_1 and S_3) are turned ON, provides the conducting path between O+ and Y terminals of CCTAs. At the same time NMOS switches (S_2 and S_4) become

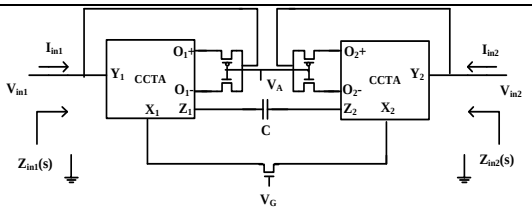
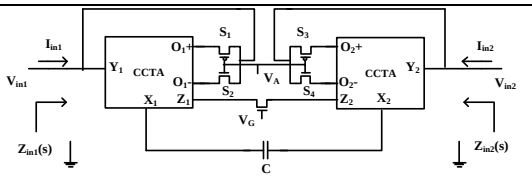
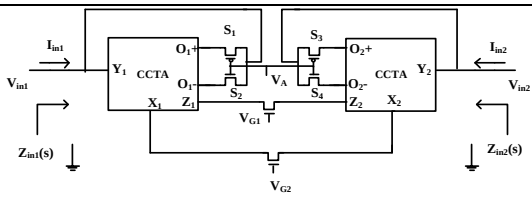
OFF, disconnecting the path between O- and Y terminals of CCTAs. The input impedance of the floating circuit is written as:

$$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = +\left(\frac{Z_R}{Z_Q g_m}\right) \quad (3.21)$$

Equation (3.21) points out that, the proposed circuit works in positive mode and capable to provide tunable positive impedances by proper selection of Z_R and Z_Q components.

Various configuration of the proposed circuit of Fig. 3.18 resulting from the value of V_A, Z_R, and Z_Q. The schematic diagram depicting the resultant topology and the sensitivities of input impedances in relation to the utilized components have been calculated and presented in Table 3.5. It is worth noting that the input impedance may be varied by modifying the bias current value of the CCTA and altering the gate voltage of the MOS resistor. Moreover, sensitivity exhibits a unity value in relation to the variations of all the components.

Table 3.5 Different configurations of the proposed CCTA based floating immittance circuit**.**

Configuration	Selection of components	Switch Setting	Equivalent Input Impedance ($Z_{in}(s)$)	Equivalent Input Impedance magnitude	Schematic of the Configuration	Sensitivity
Inductor	$Z_Q = \frac{1}{sC_1}$; $Z_R = R_1$	V_A = H	$+\frac{sR_1C_1}{g_m}$	$L_{eq} = +\frac{R_1C_1}{g_m}$		$S_{C_1}^{\lvert L_{eq}\rvert} = S_{R_1}^{\lvert L_{eq}\rvert} = -S_{g_m}^{\lvert L_{eq}\rvert} = 1$
		V_A = L	$-\frac{sR_1C_1}{g_m}$	$L_{eq} = -\frac{R_1C_1}{g_m}$		
Capacitor	$Z_R = \frac{1}{sC_1}$; $Z_Q = R_1$	V_A = H	$+\frac{1}{sR_1C_1g_m}$	$C_{eq} = +R_1C_1g_m$		$S_{C_1}^{\lvert C_{eq}\rvert} = S_{R_1}^{\lvert C_{eq}\rvert} = S_{g_m}^{\lvert C_{eq}\rvert} = 1$
		V_A = L	$-\frac{1}{sR_1C_1g_m}$	$C_{eq} = -R_1C_1g_m$		
Resistor	$Z_R = R_1$; $Z_Q = R_2$	V_A = H	$+\frac{R_1}{R_2g_m}$	$R_{eq} = +\frac{R_1}{R_2g_m}$		$-S_{R_2}^{\lvert R_{eq}\rvert} = S_{R_1}^{\lvert R_{eq}\rvert} = -S_{g_m}^{\lvert R_{eq}\rvert} = 1$
		V_A = L	$-\frac{R_1}{R_2g_m}$	$R_{eq} = -\frac{R_1}{R_2g_m}$		

L- Low; H – High, R_1 and R_2 are MOS based resistor.

3.2.2.1 Non-ideal analysis

Considering the parasitic components of CCTA as discussed in chapter 2, the proposed CCTA based floating immittance circuit of Fig. 3.18 is modified as Fig. 3.19.

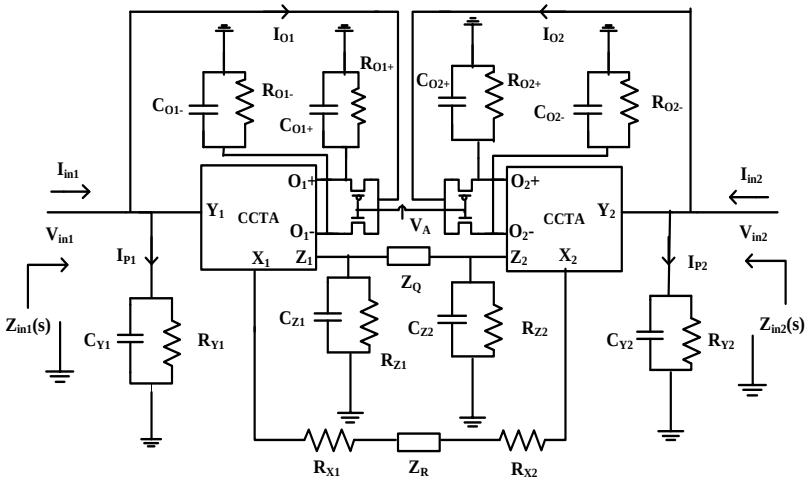


Fig. 3.19 Proposed CCTA based floating immittance circuit 2 with parasitic components.

The parasitic impedance at terminal Y_1 and Y_2 can be obtained by neglecting MOS switch parasitic component as.

$$Z_{Y1} = \left(R_{O1-/O1+} \parallel R_{Y1}\right) \parallel \frac{1}{s\left(C_{O1-/O1+}+C_{Y1}\right)}; Z_{Y2} = \left(R_{O2-/O2+} \parallel R_{Y2}\right) \parallel \frac{1}{s\left(C_{O2-/O2+}+C_{Y2}\right)} \quad (3.22)$$

The parasitic impedance at terminal $Z_1$and Z_2 are obtained as

$$Z_1 = R_{Z1} \parallel \frac{1}{sC_{Z1}}; Z_2 = R_{Z2} \parallel \frac{1}{sC_{Z2}} \quad (3.23)$$

The current flowing through Z_{P1} and Z_{P2} are I_{P1} and I_{P2} respectively can be obtained as

$$I_{P1} = \frac{V_{in1}}{Z_{P1}};\ I_{P2} = \frac{V_{in2}}{Z_{P2}} \quad (3.24)$$

$$I_{P1} = I_{in1} - I_{O1};\ I_{P2} = I_{in2} - I_{O2} \quad (3.25)$$

The proposed immittance circuit with parasitic components as shown in Fig. 3.19 may be defined as:

$$I_{in1}\left[1+\frac{Z_1}{Z_Q}\right] - I_{in2}\left[\frac{Z_1}{Z_Q}\right] = I_{P1}\left[1+\frac{Z_1}{Z_Q}\right] - I_{P2}\left[\frac{Z_1}{Z_Q}\right] \pm \frac{g_m(V_{in1}-V_{in2})Z_1}{R_{X1}+R_{X2}+Z_R} \quad (3.26)$$

Since $Z_1 \gg Z_Q$. So, $\left(1+\frac{Z_1}{Z_Q}\right) \approx \left(\frac{Z_1}{Z_Q}\right)$ and $Z_{P1} = Z_{P2} = Z_P$ then, eq. (3.26) can be rewritten as:

$$I_{in1} - I_{in2} = \left(\frac{V_{in1}-V_{in2}}{Z_P}\right) \pm \frac{g_m(V_{in1}-V_{in2})Z_Q}{R_{X1}+R_{X2}+Z_R} \quad (3.27)$$

Since, $Z_P = \left(R_{O1-/O1+} \parallel R_Y\right) \parallel \frac{1}{s\left(C_{O1-/O1+}+C_Y\right)} = R_P \parallel \frac{1}{sC_P} = \frac{1}{\frac{1}{R_P}+sC_P}$. Thus, eq. (3.27) can be rewritten as:

$$Y_{in}(s) = \left(\frac{I_{in1}-I_{in2}}{V_{in1}-V_{in2}}\right) = \frac{1}{R_P} + sC_P \pm \frac{g_m Z_Q}{(R_{X1}+R_{X2}+Z_R)} \quad (3.28)$$

Since, value of C_P, R_X, and $\frac{1}{R_P}$ are low. So, these values can be neglected from eq. (3.28). Now, the value of magnitude of selected component Z_R is much higher than $(R_{X1} + R_{X2})$. Then, eq. (3.28) is reduced to their corresponding ideal counter parts eq. (3.20) and eq. (3.21).

Positive Immittance: $$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = +\frac{Z_R}{g_m Z_Q} \quad (3.29)$$

Negative Immittance: $$Z_{in}(s) = \left(\frac{V_{in1}-V_{in2}}{I_{in1}-I_{in2}}\right) = -\frac{Z_R}{g_m Z_Q} \quad (3.30)$$

3.2.2.2 Results and discussion

A substantial investigation of the designed floating immittance circuit is evaluated through SPICE simulator using 180 nm process parameter. The aspect ratio of MOS transistors of CCTA is mentioned in chapter 2 (Table 2.2). The supply voltage and bias voltage of CCTA are taken as ±1.2 V and +0.42 V respectively. The Layout of the CCTA circuit is depicted in Fig. 3.20 The area of the layout is 22.8 µm × 67.8 µm. Floating immittances value, input phase of proposed immittance and operating frequency of the proposed floating immittance with respect to component value and bias current of CCTA (I_B) shown in Table 3.6. Now, the frequency response of input impedance of proposed integer order positive and negative inductor is displayed in Fig. 3.21(a) and Fig. 3.21(b) respectively. It is worth mentioning that there is a close match between simulated and theoretical values from 4 kHz to 5 MHz.

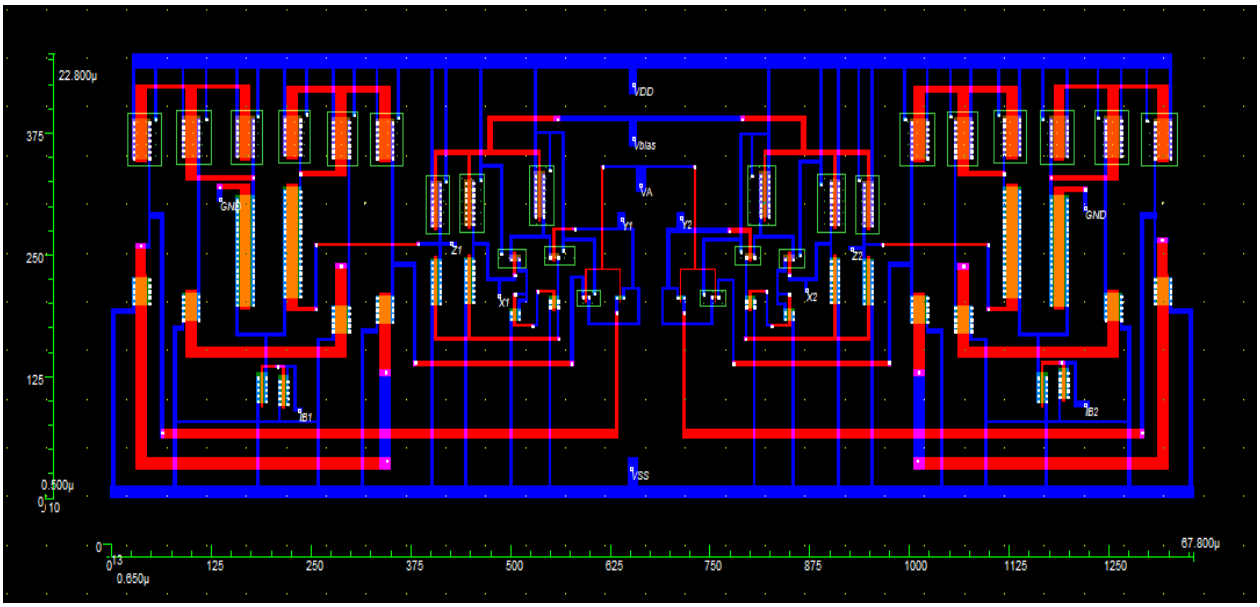
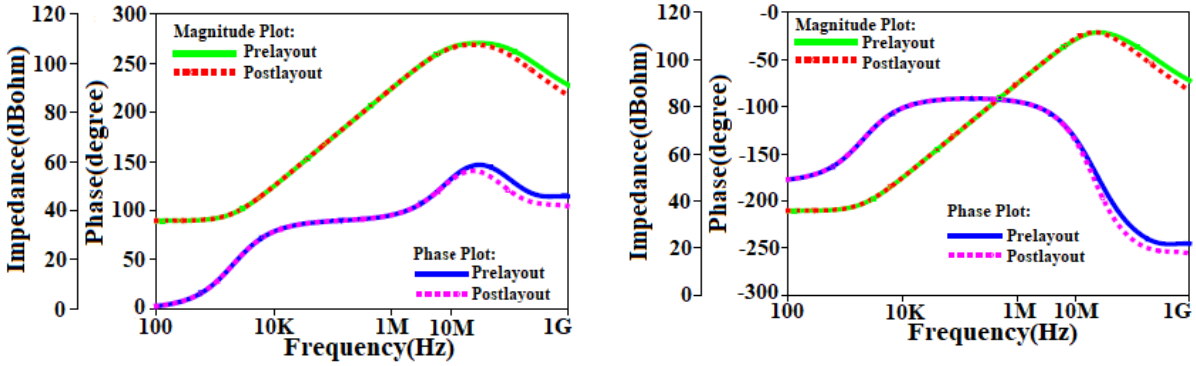


Fig. 3.20 Layout of floating immittance circuit.

Table 3.6 Active floating immittances value with respect component value and bias current ($I_B = 40\ \mu A$).

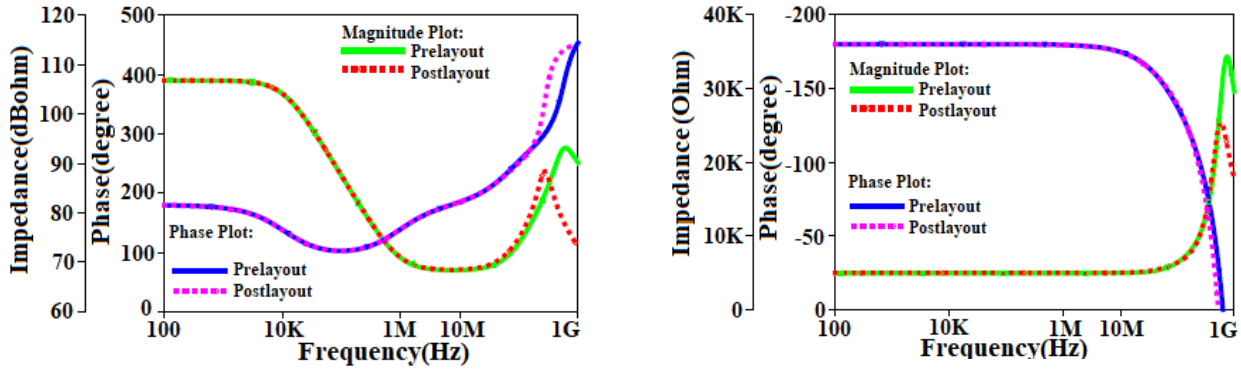
S.N.	Nature of immittance	Component Value	Immittance Value	Operating frequency range of immittance; Input phase
1.	Positive integer order inductor	R_1 =1 kΩ, C_1=1 nF	L_{eq}=+4.96mH	4 kHz -5MHz; +90°
2.	Negative integer order inductor	R_1 =1 kΩ, C_1=1 nF	L_{eq}=-4.96mH	4.23 kHz -6.9 MHz; -90°
3.	Negative integer order Capacitor	R_1 =500 Ω, C_1=0.5 nF	C_{eq}=-50 pF	10 kHz - 1 MHz; +90°
4.	Positive resistor	$R_1 = R_2$=1 kΩ	R_{eq}=+ 5 kΩ	NA; 0°
5.	Negative resistor	$R_1 = R_2$=1 kΩ	R_{eq}=-5 kΩ	NA; -180°

Further, the input impedance of the proposed floating negative capacitor is shown in Fig. 3.22(a). Figure 3.22(a) confirms that the circuit exhibits good performance between 10 kHz to 1 MHz for proposed negative capacitor. Figure 3.22(b) shows frequency response of negative floating resistor in which input impedance and phase are independent of input frequency between 1 Hz to 30 MHz. Power consumption of proposed immittance circuit is 3.47 mW. Further, the effect of variation in the value of the component on the performance of the floating inductor is displayed in Fig. 3.23(a). This response is obtained by performing Monte Carlo analysis for 500 runs with 10% tolerance in passive components. Fig. 3.23(a) demonstrates that deviation in magnitude response of the proposed inductor is approximately ±2.4 dB. In practice, the performance of the the floating immttance emulator may vary due to supply voltage and temperature variations. The frequency response of floating inductor is plotted in Fig. 3.23(b) by varying supply from ±1.0 V to ±1.4 V and the variation of 5.1 dB is observed in the input impedance. Impact of temperature variations on input impedance of floating inductor is also studied by varying temperature from -45°C to 90°C and the overall spread in input impedance is found to be within 4 dB in the observed frequency range as shown in Fig. 3.24(a).



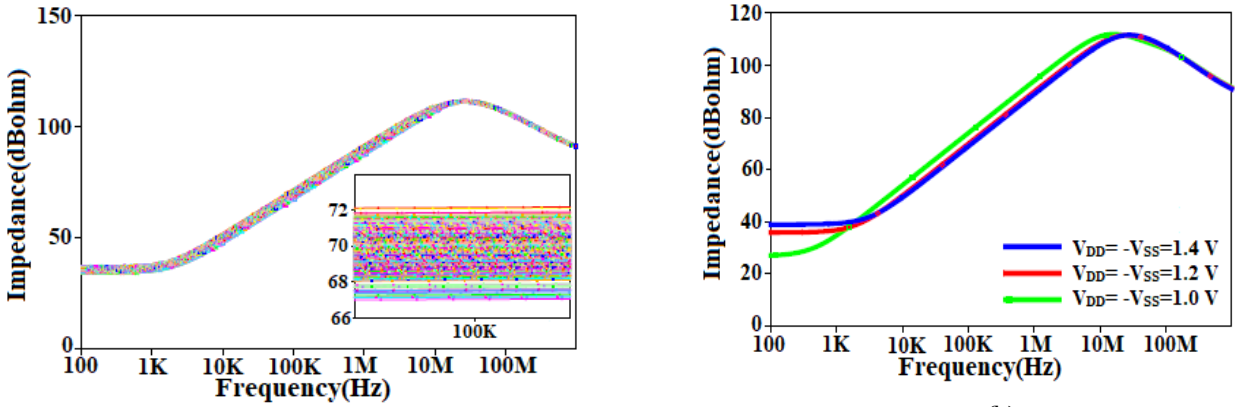
(a) (b)

Fig. 3.21 Frequency response of the proposed floating inductor (a) positive, and (b) negative.



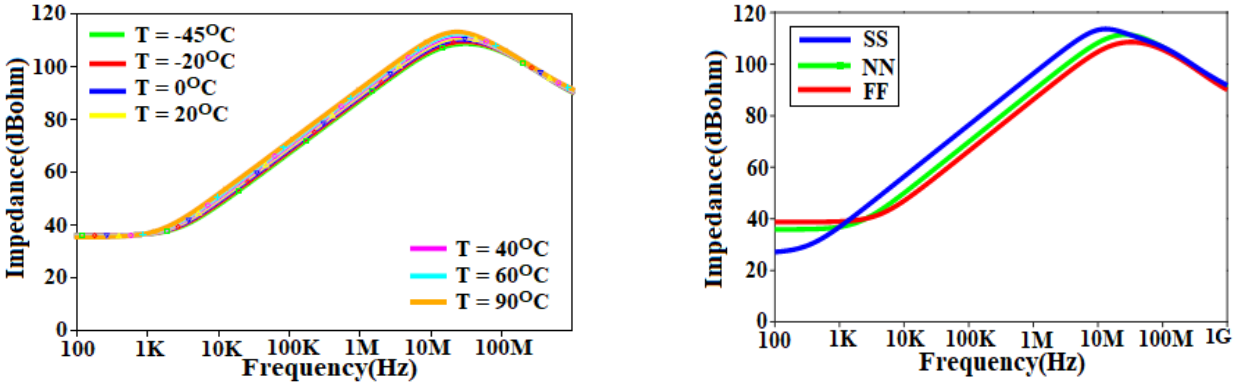
(a) (b)

Fig. 3.22 Frequency response of proposed floating negative (a) capacitor, and (b) resistor.



(a) (b)

Fig. 3.23 Magnitude response of proposed grounded inductor for variation in (a) passive components, and (b) supply voltage.



(a) (b)

Fig. 3.24 Magnitude response of proposed grounded inductor for variation in (a) temparatures, and (b) corner analysis.

The efficiency of the suggested floating immittance circuit is greatly affected by process corner in monolithic integration. The Nominal Nominal (NN), Slow Slow (SS), and Fast Fast (FF) process corners have thoroughly analyzed it. The PHL at various process corners of the given

circuit are shown in Fig. 3.24(b). To accomplish the corner fluctuations, one needs to adjust the supply voltage from ±1 V to ±1.4 V and the temperature from -45˚C to +90˚C, respectively. Figure 3.24(b) indicates that when the floating inductor is in SS mode, the current flowing through it is lower than when it is in FF mode.

3.2.2.3 Applications

The following applications may verify the performance of the proposed floating immittance circuit: (I) Fifth order low pass filter using proposed inductor, and (II) Capacitance cancelation circuit using proposed negative capacitor.

I. Fifth order low pass filter using proposed inductor

The fifth order low pass filter circuit can be used to demonstrate the application of proposed positive integer order inductor, which is shown in Fig. 3.25(a). The transfer function of fifth order low pass filter can be expressed as:

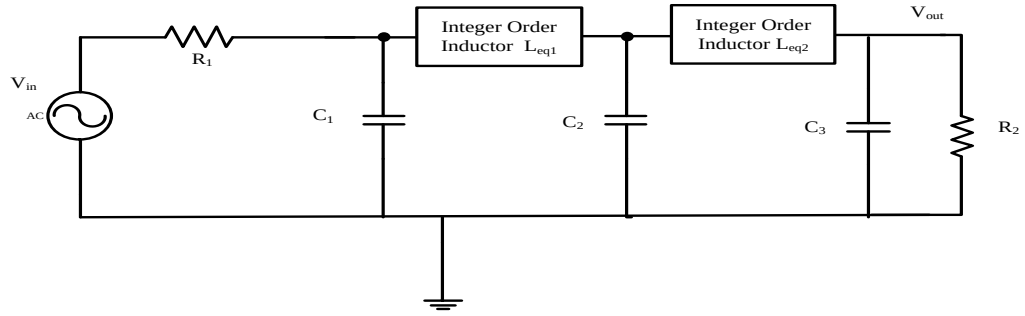
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_o} \tag{3.31}$$

Here, $b_o = R_2; b_1 = R_1 C_1 R_2 + L_{eq2}; b_2 = L_{eq2} R_1 C_1 + L_{eq1} C_2 R_2 + L_{eq2} C_3 R_2;$

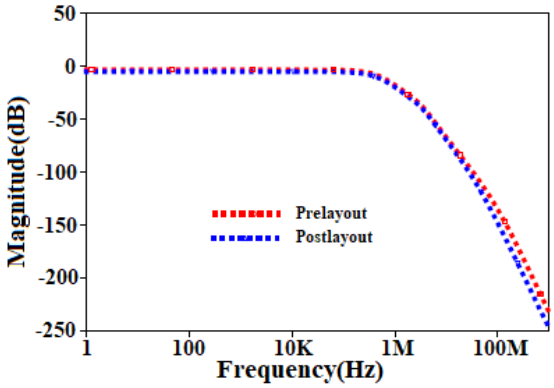
$b_3 = L_{eq1} C_2 R_2 R_1 C_1 + R_2 L_{eq2} C_3 R_1 C_1 + L_{eq1} L_{eq2} C_2; b_4 = R_1 C_1 L_{eq1} L_{eq2} C_2 + R_2 C_3 L_{eq2} L_{eq1} C_2;$

$b_5 = C_1 C_2 C_3 L_{eq1} L_{eq2} R_1 R_2.$ (3.32)

To functionality of the fifth order low pass filter, following components are used: $L_{eq1} = L_{eq2} =$ =+0.125 mH (R=250 Ω, C=0.1 nH, and I_B=40 µA), C_1=C_3=250 pF, C_2=10 pF, R_1=500 Ω and R_2=1000 Ω. The integer order inductors are realized using configuration 1 of Table 3.5. The simulated and theoretical plots of voltage gain of the low pass filter are shown in Fig. 3.25(b). The simulated cutoff frequency and roll-off rate of fifth order low pass filter is observed to be 0.93 MHz and -100 dB/decade respectively. DC gain of the designed low pass filter is -3.5 dB. The power consumption of the low pass filter is 2.73 mW.



(a)

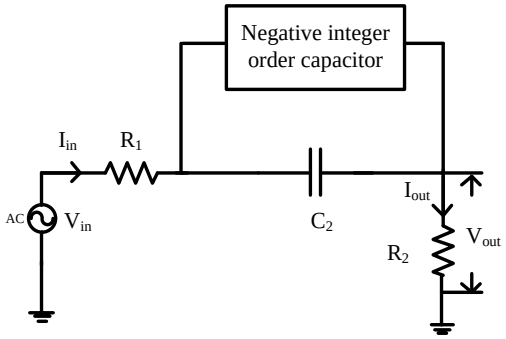


(b)

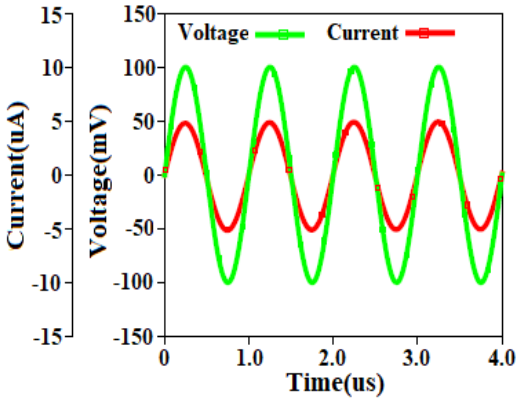
Fig. 3.25 Fifth order low pass filter. (a) Circuit, and (b) response of the fifth order low pass filter.

II. Capacitance cancelation circuit using proposed negative capacitor

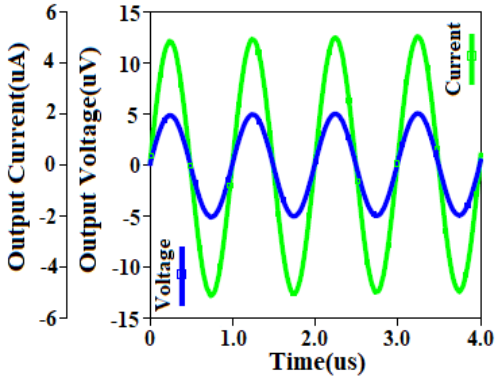
A capacitance cancellation circuit may be used to evaluate the working of the proposed negative integer order capacitor, which is shown in Fig. 3.26(a). To check the performance of the circuit, an input voltage is a sine wave of 100 mV peak to peak, frequency of 1MHz and component values are taken for design are R_1=20 kΩ, R_2=1 Ω, C_{eq1}=-150pF and C_2=+150 pF.



(a)



(b)



(c)

Fig. 3.26 (a) Capacitance cancellation circuit. (b) Input voltage and input current waveform. (c) Output voltage and output current waveform.

The integer order negative capacitances are realized using configuration 2 of Table 3.5 and the component values $R = 1\ k\Omega$, $C = 166$ pF, and $I_B = 200\ \mu A$. The transient responses of the input and output waveform are mentioned in Fig. 3.26(b) and Fig. 3.26(c) respectively. From these figures, it is observed that the input voltage, input current, output voltage and output current are in phase as the positive integer order capacitance circuit has nullified by negative integer order capacitance, making the circuit purely resistive.

3.4 Comparison

The detailed comparisons among the proposed immittance circuits (discussed in section 3.1 to 3.3) with state of art circuits are mentioned in Table 3.7.

Table 3.7 Comparison of positive and negative immittances with the proposed circuit using CCTA.

Ref.	Active block-No.	No. of Passive Compo-nent	Availabi-lity of tuning	Technology	G/F	Matching Require-ment	Nature of immittances		Change in Topology based on		
							±L	±C	Different circuits are used	Interchange input terminal voltage	Change position of components
[21]	DO-CCCCII-1 & CCCCII-3	4	NO	PR100N & NR100N	F	NO	±L	±C	NO	YES	NO
[22]	DO-CCCCII-1 & CCCCII-3	1	YES	NR100N & PR100N	F	NO	±L	±C	YES	NO	NO
[23]	OTA-2	1	YES	PR200N & NR200N	F	NO	±L	-	YES	NO	NO
[30]	CFOA-2	4	NO	-	F	YES	±L	-	YES	NO	NO
[32]	CFOA-4	6	YES	350 nm	F	NO	±L	-	NO	NO	YES
[33]	DO-CCII-1 & OTA-1	2	YES	350 nm	F	NO	±L	±C	NO	YES	NO
[34]	DV-CCTAs-2	3	YES	PR200N & NR200N	F	NO	±L	±C	NO	YES	NO
[41]	MO-CCCCTA-1	1	YES	PR100N & NR100N	F	NO	±L	-	YES	NO	NO
[45]	CBTA-1	2	YES	250 nm	F	NO	±L	±C	NO	YES	NO
[46]	CBTA-2	3	YES	250 nm	F	NO	±L	±C	NO	YES	NO
[53]	VDVTA-1	3	YES	130 nm	F	NO	±L	±C	NO	NO	YES
[59]	DDCC-1	3	NO	130 nm	F	YES	±L	-	YES	NO	NO
[60]	DDCC-1	3	NO	130 nm	G	YES	±L	-	YES	NO	NO
[65]	ZC-CCCITA	1	YES	350 nm	G	NO	±L	-	YES	NO	NO
[71]	VDCC-1	2	YES	180 nm	G	NO	±L	-	YES	NO	NO
[73]	DXCCII-1	3	NO	350 nm	G	YES	±L	-	YES	NO	NO
Proposed	CCTA-1	2	YES	180 nm	G	NO	±L	±C	NO	NO	NO
Proposed	CCTA-2	3	YES	180 nm	F	NO	±L	±C	NO	NO	NO
Proposed	CCTA-2	1	YES	180 nm	F	NO	±L	±C	NO	NO	NO

***List of unspecified abbreviations:** ±L=Positive and Negative Integer Order Inductor, ±C=Positive and negative Integer order Capacitor, G-Grounded, F-Floating.

It should be emphasized that the proposed immittances have following advantageous features: use of less passive component, electronic tunability due to bias current of CCTA, there is no

component matching constraints, working in positive and negative mode without change in topology. Following observations are made from the comparison Table 3.7:

a. More than one passive component is used in [21,30,32,33,34,45,46,53,59,60,71,73].
b. Tunability does not exist in [21,30,59,60,73].
c. Component matching conditions are required in [30,59,60,71].
d. Positive and negative mode of operation is achieved by the different circuits in [22,23,30,41,59,60,65,71,73].
e. Switching from positive mode of operation to negative mode of operation depends upon interchange the input terminal voltage of an active block in [21,33,34,45,46].
f. Switching from positive mode of operation to negative mode of operation depends upon changing the position of components at the different terminals of an active block in [32,53].

3.5 Summary

This chapter described three reconfigurable new CCTA based floating and grounded immittance circuits that can provide both positive and negative type immittance depending upon voltage-controlled switches. Further, non-ideal analysis of all proposed circuits is also mathematically evaluated. Pre layout simulation results of frequency response of all proposed circuits are in good agreement with post layout simulation. Monte Carlo analysis, supply voltage effect analysis, corner analysis, and temperature effect analysis are also done, which show a good performance of the proposed circuits. Finally, the fifth order low pass filter, inductance cancellation, capacitance cancellation, and multi-function filter are demonstrated to illustrate the functionality of the proposed immittances circuits.

CHAPTER 4

FRACTIONAL ORDER INDUCTOR CIRCUIT

In chapter 3, integer order immittance circuits are explained. This chapter introduces electronically adjustable floating and grounded fractional order inductor circuits. The developed circuits utilize two OTAs, one fractional order capacitor, one inverter, and four MOS switches. These circuits can operate in both positive and negative modes without any changes to their topology. The behavior of the suggested circuit is further examined in the presence of parasitic elements that may arise in the practical circuit. The functional evaluation is performed using pre and post layout simulations using a 90 nm technology parameter. The effectiveness of the proposed positive fractional inductor circuit is demonstrated by using it in a fractional order high pass and band pass filters. The practicality of the suggested negative fractional inductance circuit is showcased with the help of a fractional inductance cancellation circuit.

4.1 Proposed grounded fractional order inductor circuit

The proposed tunable positive and negative grounded fractional order inductor circuit is depicted in Fig. 4.1. The grounded inductor circuit is designed using two active blocks (OTA), one grounded fractional order capacitor (C_α), one CMOS inverter (I_O) and four MOS-based switches ($S_1 - S_4$). Fractional order capacitor is also known as fourth quadrant element because it provides phase between 0° to -90°. An RC ladder-based circuit is used to design a fractional order capacitor. Modified Oldman's method may be used to obtain the values of RC ladder circuit. I_O is a CMOS inverter circuit in which pull up network and pull-down network are obtained using PMOS and NMOS respectively.

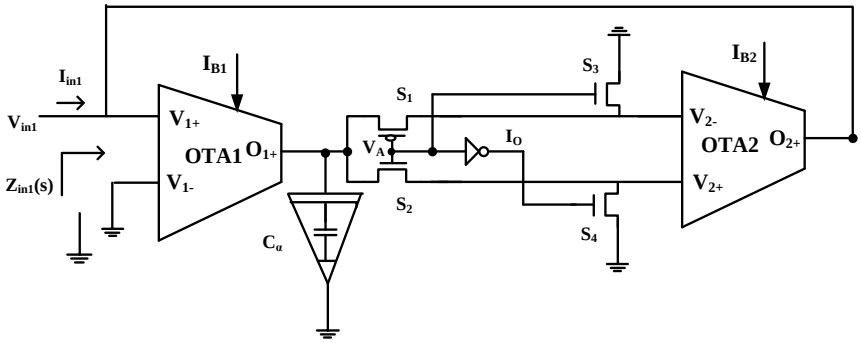


Fig. 4.1 Proposed grounded positive and negative fractional order inductor.

The positive and negative mode of operation of the proposed circuit depends upon the voltage (V_A) applied to the gates of MOS switches S_1, S_2, S_3 and S_4. When V_A is low, switches S_2 and S_3 are OFF, while switches S_1 and S_4 are ON. Then, the input impedance of the proposed circuit may be written as:

$$Z_{in}(s) = \frac{s^{\alpha}C_{\alpha}}{g_{m1}g_{m2}} \quad (4.1)$$

Similarly, with V_A high, switches S_2 and S_3 are ON while switches S_1 and S_2 becomes OFF. Therefore, the input impedance of the presented circuit is written as:

$$Z_{in}(s) = -\frac{s^{\alpha}C_{\alpha}}{g_{m1}g_{m2}} \quad (4.2)$$

Putting $s^{\alpha} = (j\omega)^{\alpha} = \omega^{\alpha}\left(\cos\frac{\pi\alpha}{2} + j\sin\frac{\pi\alpha}{2}\right)$ in eqs. (4.1) and (4.2), then input impedance and input phase of the proposed circuit with V_G low and high can be expressed as:

$$Z_{in}(s) = \frac{\omega^{\alpha}C_{\alpha}}{g_{m1}g_{m2}} \angle\left(+\frac{\alpha\pi}{2}\right) \quad (4.3)$$

$$Z_{in}(s) = \frac{\omega^{\alpha}C_{\alpha}}{g_{m1}g_{m2}} \angle\left(-180° + \frac{\alpha\pi}{2}\right) \quad (4.4)$$

respectively.

It can be seen from eq. (4.3) that the input phase provided by the proposed circuit lies between $0°$ to $90°$ whereas eq. (4.4) shows that the input phase of the proposed circuit lies between $-90°$ to $-180°$. It is observed from eqs. (4.1) to (4.4) that the input impedance of the developed circuits reliant upon bias current of the OTAs and capacitance of the fractional capacitor and there is no passive component matching condition.

4.2 Proposed floating fractional order inductor circuit

The proposed tunable positive and negative floating fractional order inductor circuit is shown in Fig. 4.2. The proposed floating fractional inductor is designed using two active blocks (OTA), one grounded fractional order capacitor (C_{α}), one inverter (I_O) and four MOS-based switches $(S_1 - S_4)$.

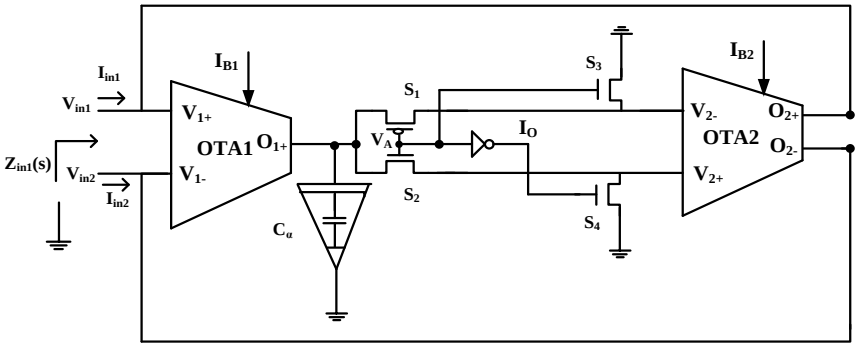


Fig. 4.2 Proposed floating positive and negative fractional order inductor.

The switch selection and working of the proposed floating positive and negative fractional order inductor are the same as the grounded negative and positive fractional order inductor circuit.

Thus, the input impedance of the designed floating fractional order inductor circuit may be written as:

$$Z_{in}(s) = \pm \frac{s^{\alpha} C_{\alpha}}{g_{m1} g_{m2}} \tag{4.5}$$

where '+' sign refers to V_A low and '-' sign is obtained for V_A high.

It can be observed from eq. (4.1) to eq. (4.5), that the proposed grounded and floating fractional order inductance circuit may be varied by changing the bias current (I_B) of OTA. The sensitivity of L_{α} $\left(L_{\alpha} = \pm \frac{C_{\alpha}}{g_{m1} g_{m2}}\right)$ to the variation in passive component and transconductance are obtained as:

$$S_{C_{\alpha}}^{L_{\alpha}} = -S_{g_{m1}}^{L_{\alpha}} = -S_{g_{m2}}^{L_{\alpha}} = 1 \tag{4.6}$$

$$S_{C_{\alpha}}^{-L_{\alpha}} = -S_{g_{m1}}^{-L_{\alpha}} = -S_{g_{m2}}^{-L_{\alpha}} = 1 \tag{4.7}$$

It is observed from eq. (4.6) and eq. (4.7) that the sensitivity of the proposed positive and negative fractional inductor circuit with respect to passive component and transconductance is unit.

4.3 Non-ideal analysis

The parasitic components appear at different terminals of OTA in the form of the parallel combination of resistances and capacitances and may lead to deviation in the performance of the proposed fractional inductor. The parasitic components of the OTA have been addressed in chapter 2. Considering the parasitic components, the proposed circuit of Fig. 4.1 is modified as Fig. 4.3.

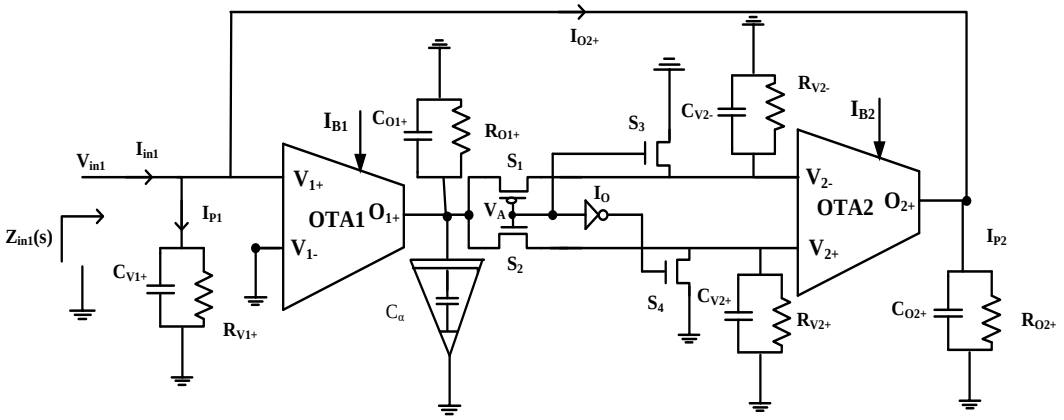


Fig. 4.3 Proposed circuit with parasitic components.

The parasitic resistance and capacitance at terminal V_{1+} can be obtained as:

$$R_P = R_{O2+} \parallel R_{V1+};\ C_P = C_{O2+} \parallel C_{V1+} \tag{4.8}$$

The parasitic impedance at terminal O_{1+} can be obtained by neglecting MOS switch parasitic component as:

$$Z_{O1+} = (R_{O1+} \parallel R_{V2-}) \parallel \left(\frac{1}{s(C_{O1+}+C_{V2-})+s^{\alpha}C_{\alpha}}\right) \tag{4.9}$$

Now, current flowing through O_{2+} terminal can be obtained as:

$$I_{O2+} = \pm g_{m1}g_{m2}V_{in1}Z_{O1+} \tag{4.10}$$

From Fig. 4.3, the input current is the sum of the current at O_{2+} terminal and current through Z_P $\left(Z_P = R_P \parallel \frac{1}{sC_P}\right)$. Thus, the input current can be written as:

$$I_{in} = V_{in}\left(sC_P + \frac{1}{R_P}\right) \pm g_{m1}g_{m2}V_{in1}Z_{o+1} \tag{4.11}$$

Input admittance of the positive fractional order circuit with parasitic components as shown in Fig. 4.3 can be calculated as:

$$\frac{I_{in}}{V_{in}} = sC_P + \frac{1}{R_P} \pm \frac{g_{m1}g_{m2}R_M}{1+(sC_{O1+}+sC_{V2-}+s^{\alpha}C_{\alpha})R_M} \tag{4.12}$$

where, $R_M = R_{O1+} \parallel R_{V2-}$. Now, input admittance (ratio of input current (I_{in}) to input voltage (V_{in})) of the positive fractional order circuit can be obtained by considering $(sC_{O1+} + sC_{V2-} + s^{\alpha}C_{\alpha})R_M \gg 1$ as:

$$\frac{I_{in}}{V_{in}} = sC_P + \frac{1}{R_P} \pm \frac{g_{m1}g_{m2}}{(sC_{O1+}+sC_{V2-}+s^{\alpha}C_{\alpha})} \tag{4.13}$$

Since value of parasitic capacitances (C_P, C_{O1+} and C_{V2-}) and conductance ($1/R_P$) are low, eq. (4.13) reduces to its corresponding ideal counterparts which are given as:

$$Z_{in}(s) = \pm\frac{s^{\alpha}C_{\alpha}}{g_{m1}g_{m2}} \tag{4.14}$$

4.4 Results and discussion

The functional verification of the developed fractional inductance circuits is performed by the SPICE simulator using 90 nm technology node. The aspect ratio of transistor of OTA is mentioned in chapter 2 (Table 2.1). The DC supply voltages are chosen as ±1.2 V. The layout of proposed circuit is illustrated in Fig. 4.4 which encompasses the spatial extent of 783.87 μm^2 (49.3 µm × 15.9 µm). An RC ladder-based circuit is used to design a fractional order capacitor as shown in Fig. 4.5. Modified Oldman's method [142] is used to design fractional order capacitor of capacitance 10 $\mu\Omega^{-1}s^{-0.6}$ for the order of exponent 0.6. The calculated values for Fig. 4.5 fractional capacitor having $\alpha = 0.6$ and C_{α}=+10 $\mu\Omega^{-1}s^{-0.6}$ are R_0=0.1678 MΩ, R_1=28.63 kΩ, R_2=8.44 kΩ, R_3=2.4878 kΩ, R_4=733.3695 Ω, R_5=216.1909 Ω, R_6=63.7312 Ω, R_7=18.784 Ω,

C_0=12.978 µF, C_1=9.9332 µF, C_2=4.3998 µF, C_3=1.9488 µF, C_4=0.86321 µF, C_5=0.38235 µF, C_6=0.16939 µF and C_7=75 nF.

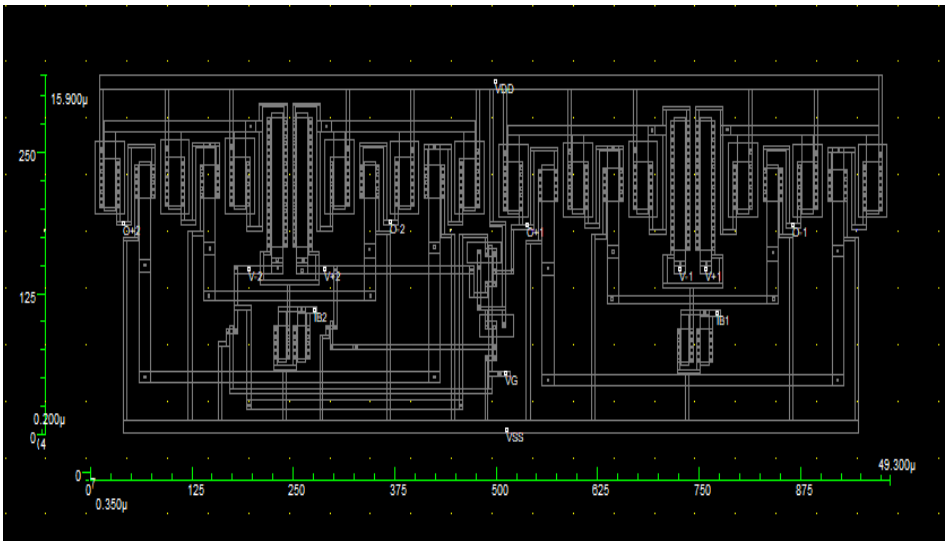


Fig. 4.4 Layout of proposed circuit.

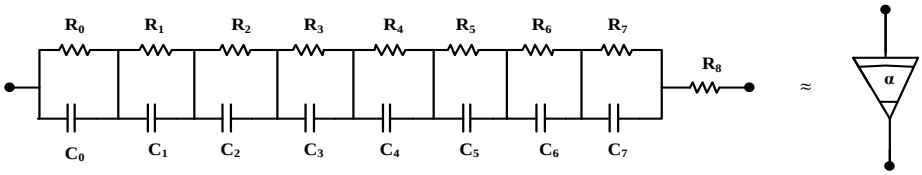
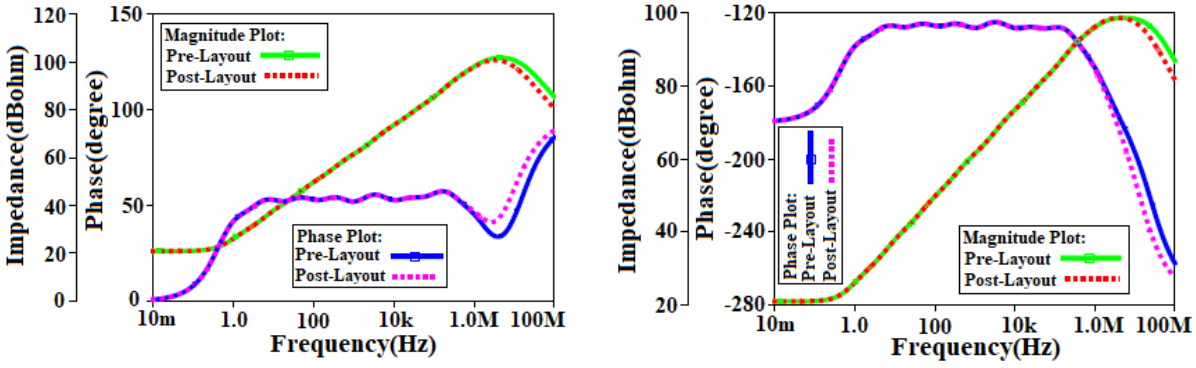
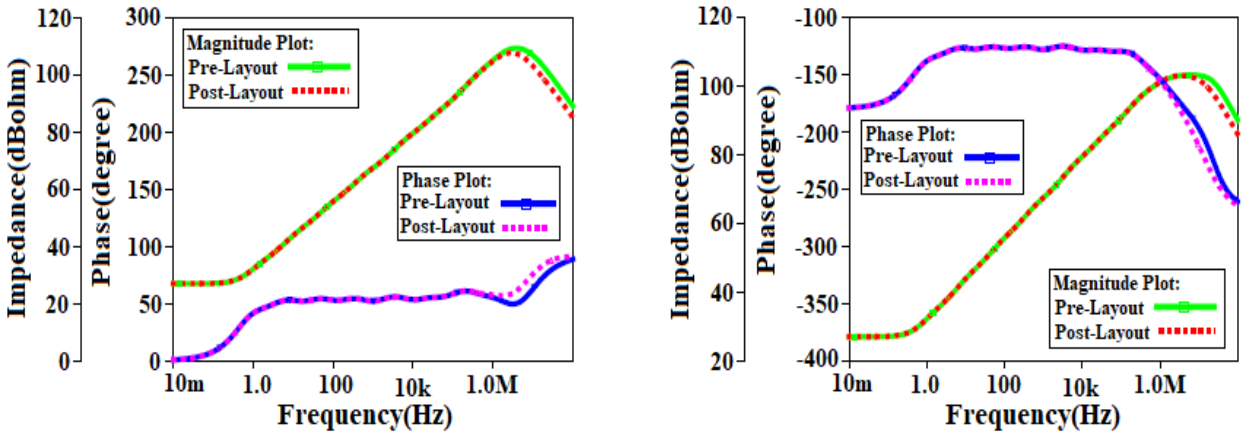


Fig. 4.5 RC ladder structure for fractional capacitor.

The frequency response for the proposed circuits is obtained through pre-layout and post-layout simulations and the results are plotted in Fig. 4.6. This response is obtained by selecting the passive component and bias current as C_α=10 $\mu\Omega^{-1}s^{-0.6}$ and $I_B = +100$ µA respectively, resulting in $L_\alpha = 8.573\ \Omega s^{0.6}$. It may be observed from Fig. 4.6 that there is close matching between, pre and post layout results in the frequency range of 1 Hz to 300 kHz.



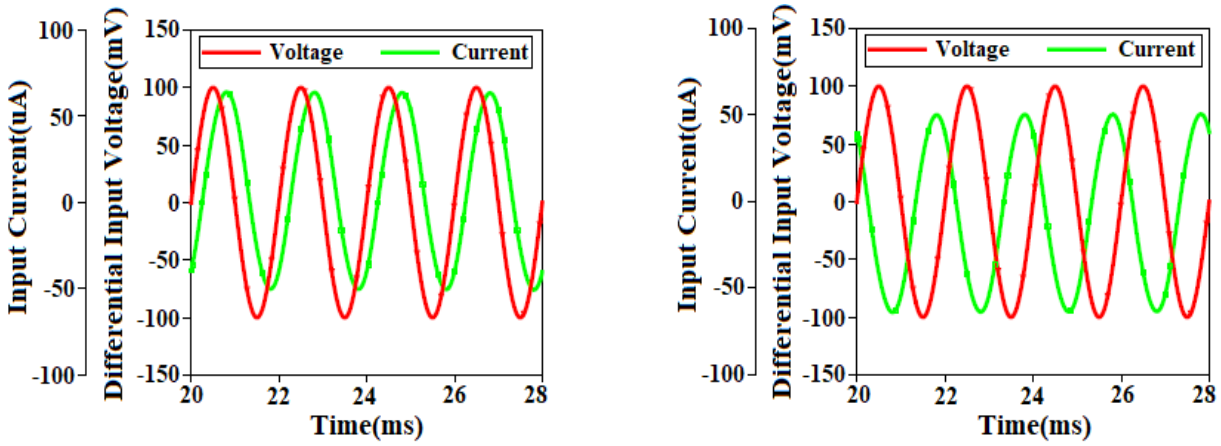
(a) (b)



(c) (d)

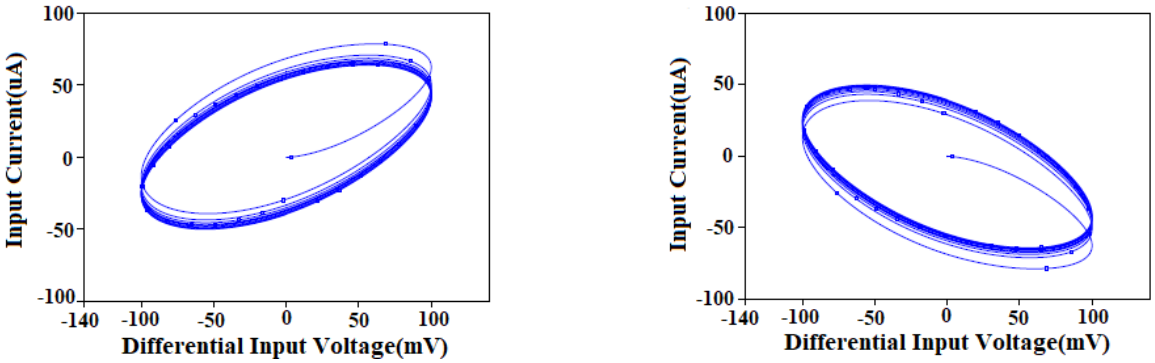
Fig. 4.6 Frequency response of proposed fractional order inductor (a) positive grounded, (b) negative grounded, (c) positive floating, and (d) negative floating.

The transient response of the floating fractional inductors is derived by applying a differential input voltage $(V_1 - V_2)$ of 100 mV peak sinusoidal supply voltage with 500 Hz frequency at input terminals. Figure 4.7 displays the transient responses. It can be noted from Fig. 4.7(a) that voltage leads current by $54°$ $(90° \times \alpha)$ whereas current leads voltage by $126°$ $(-180° + 90° \times \alpha)$ in Fig. 4.7(b). Further, the Lissajous pattern of floating positive fractional inductor and floating negative fractional order inductor are illustrated in Fig. 4.8(a) and Fig. 4.8(b) respectively. Figures 4.8(a) and 4.8(b) reveal the phase shift between differential input voltage (V_1-V_2) and input current of the floating positive fractional inductor and negative fractional inductance circuit respectively.



(a) (b)

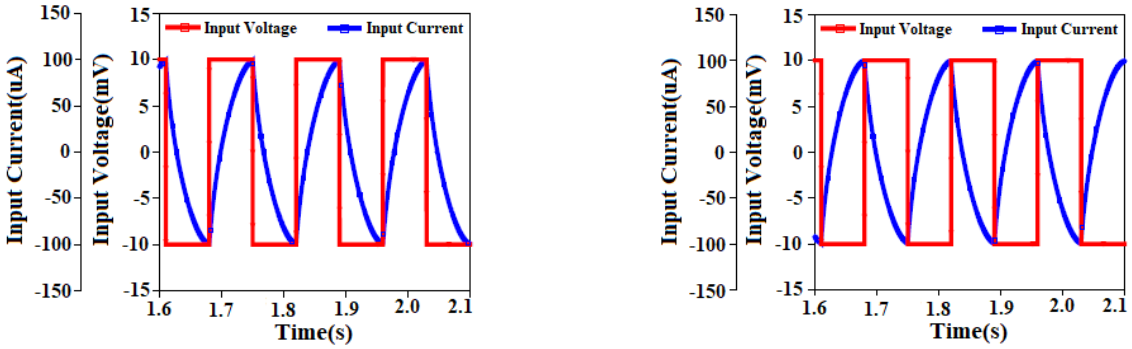
Fig. 4.7 Transient response of floating fractional order inductor (a) positive, and (b) negative.



(a) (b)

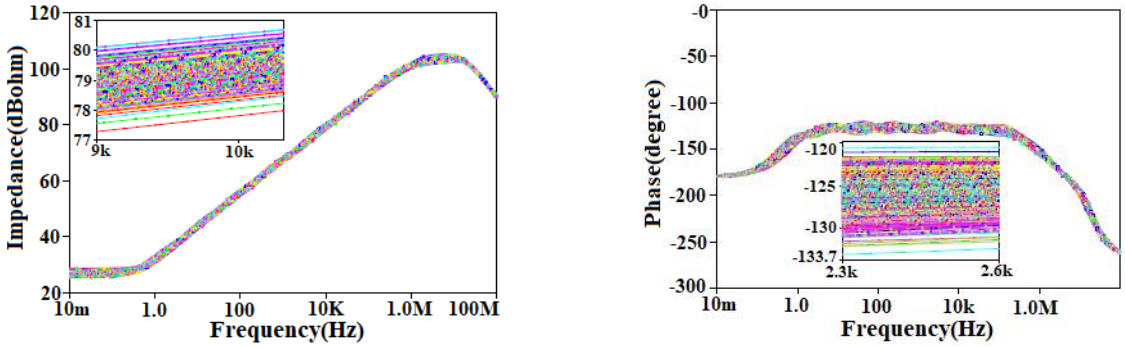
Fig. 4.8 Lissajous pattern of floating fractional order inductor (a) positive, and (b) negative.

To explain the behavior of both positive and negative fractional inductance, a square waveform with a peak value of 10 mV and a frequency of 7 Hz is applied to the input terminal of the proposed circuit. Thus, the current at the input terminal of grounded positive fractional order inductor and negative fractional order inductor are triangular waveforms with the amplitude of 100 µA peak at frequency 7 Hz are illustrated in Fig. 4.9(a) and Fig. 4.9(b) respectively.



(a) (b)

Fig. 4.9 The applied square input voltage and corresponding triangular (for $\alpha = 0.6$) input current response for (a) grounded positive fractional order inductor, and (b) grounded negative fractional order inductor.

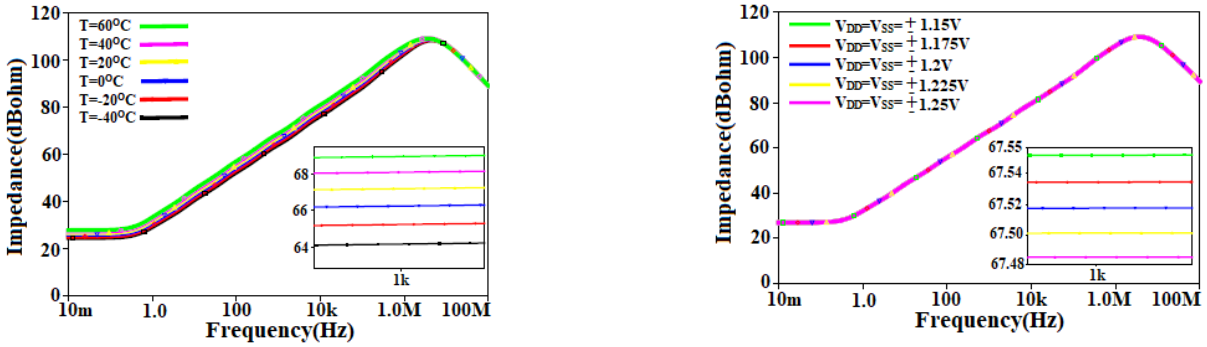


(a) (b)

Fig. 4.10 Monte Carlo analysis for grounded negative fractional inductor (a) magnitude, and (b) phase.

A Monte Carlo study is conducted, consisting of 500 iterations, with a Gaussian deviation of 10% in the passive component. The purpose is to investigate the impact of the deviation in the passive element on the magnitude and phase response of the proposed grounded negative fractional order inductor, as illustrated in Fig. 4.10. It can be noticed from Fig. 4.10 that deviation in magnitude and phase response of proposed grounded negative fractional order inductor are $\pm$ 1.5 dB and $\pm$6° respectively.

The performance of the circuits may deviate due to temperature and supply variations. The impedance magnitude curves for temperature variation -40°C to +60°C and supply variation from supply variations from ± 1.15 V to ± 1.25 V are examined for grounded positive fractional inductor and corresponding plots are displayed in Fig. 4.11(a) and Fig 4.11(b) respectively. A maximum deviation of 7.81% is observed. The electronically controllable feature of proposed circuits is tested by changing the bias current of OTAs from 10 µA to 200 µA. Both theoretical and simulated plots are placed in Fig. 4.12. The % error between theoretical and simulated plots is within 11.85. Power dissipations of the proposed fractional inductor circuit for bias currents 40 µA and 100 µA are 0.86 mW and 1.44 mW respectively.



(a) (b)

Fig. 4.11 Magnitude response of proposed grounded positive fractional inductor for variation in (a) temperatures and (b) supply voltages.

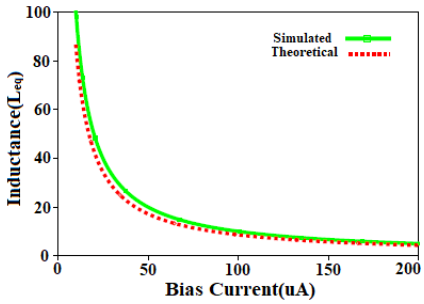


Fig. 4.12 Magnitude response of proposed grounded positive fractional inductor for different bias current of OTA.

Corner analysis is performed to estimate the sensitivity behavior of the proposed fractional inductor circuit. The corner analysis of proposed grounded positive fractional inductor circuit for Fast-Fast (FF) corner, Normal-Normal (NN) corner and Slow-Slow (SS) corner is given in Fig. 4.13. This response is obtained by varying the temperature and supply for the range of -65°C to 65°C and ±1.08 V to ±1.32 V respectively. Figure 4.13 shows that the input impedance of grounded positive fractional inductor in FF corner is lower than input impedance in SS corner because flow of current in FF corner is higher than flow of current in SS.

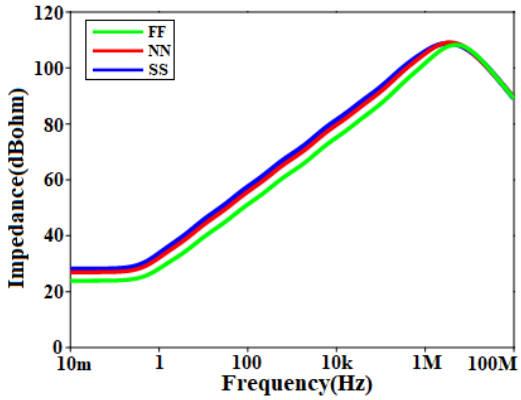


Fig. 4.13 Corner analysis of proposed grounded positive fractional inductor.

4.5 Applications

The following applications have verified the performance of the proposed fractional inductors: (I) Fractional order high-pass ladder filter, (II) Fractional order band-pass filter, and (III) Fractional inductance cancellation circuit.

I. Fractional order high-pass ladder filter

A voltage mode fractional order high-pass ladder filter circuit as presented in Fig. 4.14, which is used to test the functionality of the grounded positive fractional inductor circuit.

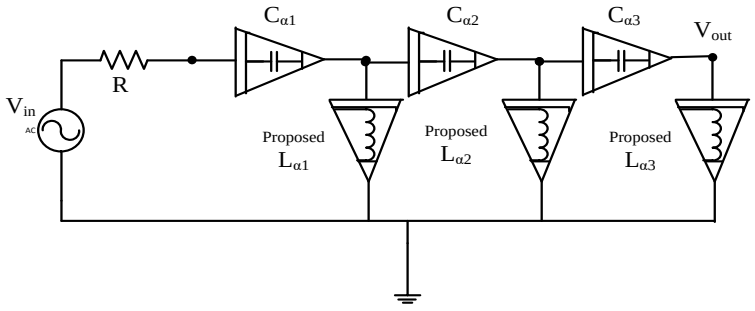


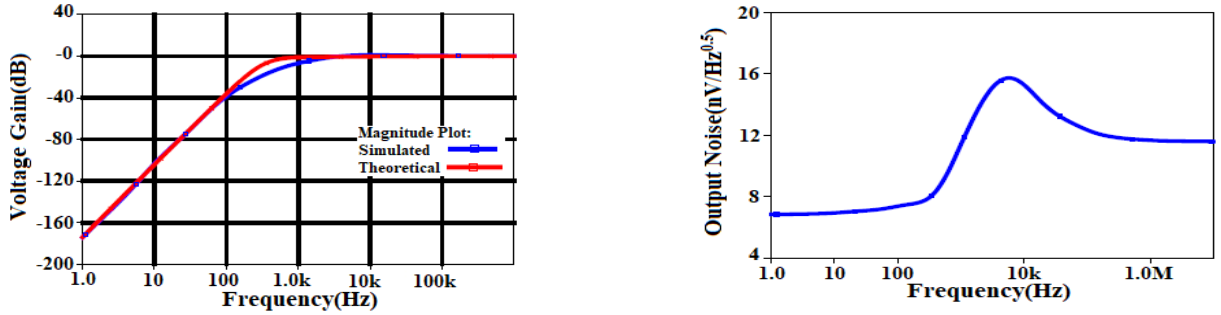
Fig. 4.14 Fractional order high-pass ladder filter.

To design high pass fractional order ladder filter using the proposed grounded positive fractional order inductor having component values are $L_{\alpha1} = L_{\alpha2} = L_{\alpha3} = L_\alpha = 8.57\ \Omega s^{0.6}$, $C_{\alpha1} = C_{\alpha2} = C_{\alpha3} = C_\alpha = 10\ \Omega^{-1}s^{-0.6}$, $R = 1\ k\Omega$ and $I_B = +100\ \mu A$. The voltage gain of fractional high pass filter and its magnitude are computed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s^{6\alpha}}{s^{6\alpha}+s^{5\alpha}\frac{3R}{L_\alpha}+s^{4\alpha}\frac{6}{L_\alpha C_\alpha}+s^{3\alpha}\frac{4R}{L_\alpha^2 C_\alpha}+s^{2\alpha}\frac{5}{L_\alpha^2 C_\alpha^2}+s^{\alpha}\frac{R}{C_\alpha^2 L_\alpha^3}+\left(\frac{1}{L_\alpha C_\alpha}\right)^3} \tag{4.15}$$

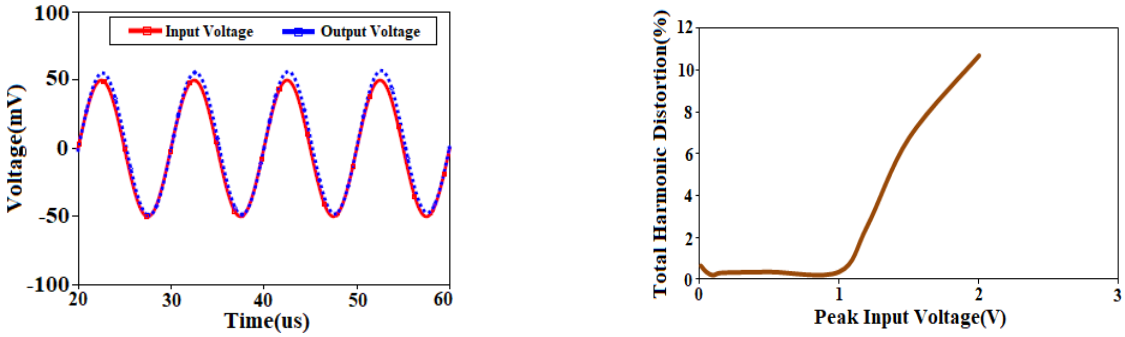
$$\left|\frac{V_{out3}(j\omega)}{V_{in}(j\omega)}\right| \cong \frac{\omega^{6\alpha}}{\sqrt{\begin{bmatrix}\omega^{12\alpha}+\frac{2\omega^{11\alpha}}{RC_\alpha}cos\left(\frac{\alpha\pi}{2}\right)+\omega^{10\alpha}\left\{\frac{6cos(\alpha\pi)}{L_\alpha C_\alpha}+\frac{1}{RC_\alpha}\right\}+\frac{\omega^{9\alpha}cos\left(\frac{\alpha\pi}{2}\right)}{RC_\alpha}\left\{\frac{2}{L_\alpha C_\alpha}+\frac{8cos(\alpha\pi)}{L_\alpha C_\alpha}\right\}+\frac{\omega^{8\alpha}}{L_\alpha^2 C_\alpha^2}\left\{3+12cos^2(\alpha\pi)+\frac{4L_\alpha}{R}cos(\alpha\pi)\right\}\\ +\frac{4\omega^{7\alpha}cos\left(\frac{\alpha\pi}{2}\right)}{RL_\alpha^2 C_\alpha^3}\{1+2cos(\alpha\pi)+2cos^2(\alpha\pi)\}+\frac{2\omega^{6\alpha}}{L_\alpha^3 C_\alpha^3}\left\{4cos^3(\alpha\pi)+\frac{2L_\alpha}{R}cos^2(\alpha\pi)+6cos(\alpha\pi)+\frac{L_\alpha}{R}\right\}+\frac{\omega^{5\alpha}4cos\left(\frac{\alpha\pi}{2}\right)}{RL_\alpha^3 C_\alpha^4}\{1+2cos(\alpha\pi)+2cos^2(\alpha\pi)\}\\ +\frac{\omega^{4\alpha}}{L_\alpha^4 C_\alpha^4}\left\{3+12cos^2(\alpha\pi)+\frac{2L_\alpha}{R}\{1+cos(\alpha\pi)\}\right\}+\frac{\omega^{3\alpha}2cos\left(\frac{\alpha\pi}{2}\right)}{RL_\alpha^4 C_\alpha^5}\left\{1+2cos(\alpha\pi)+\frac{2C_\alpha}{L_\alpha}cos(\alpha\pi)\right\}+\omega^{2\alpha}\left\{\frac{6cos(\alpha\pi)}{L_\alpha^5 C_\alpha^5}+\frac{1}{RL_\alpha^4 C_\alpha^5}\right\}+\omega^{\alpha}\left(2\frac{cos\left(\frac{\alpha\pi}{2}\right)}{RL_\alpha^5 C_\alpha^6}\right)+\left(\frac{1}{L_\alpha C_\alpha}\right)^6\end{bmatrix}}} \tag{4.16}$$

Figure 4.15(a) displays both the simulated and theoretical plots of the voltage gain for the fractional high pass filter. It is noticed from Fig. 4.15(a) that deviation between the simulated and ideal responses due to parasitic component associated with the OTAs. The cut off frequency and roll-off rate of fractional high pass filter is 578 Hz and 72 dB/decade respectively. Output noise of fractional order high pass ladder filter is observed to be 16 $nV/\sqrt{Hz}$ at 9 kHz frequency as shown in Fig. 4.15(b). Power consumption of the designed filter is 4.32 mW. Further, time domain response of the fractional high pass ladder filter is displayed in Fig. 4.16(a). This response is obtained by providing a sinusoidal input voltage of 50 mV peak at 100 kHz input frequency. Percentage of total harmonic distortion of fractional high pass ladder filter is 1% in the peak input voltage range of 10 mV to 1.1 V as shown in Fig. 4.16(b). Apart from this, Monte Carlo analysis of voltage gain of fractional order high pass ladder filter for 10% Gaussian deviation in passive components with 500 runs is shown in Fig. 4.17.



(a) (b)

Fig. 4.15 Response of high pass fractional ladder filter. (a) voltage gain, and (b) output noise ladder.



(a) (b)

Fig. 4.16 Response of fractional order high pass ladder filter. (a) Transient analysis, and (b) total harmonic distortion.

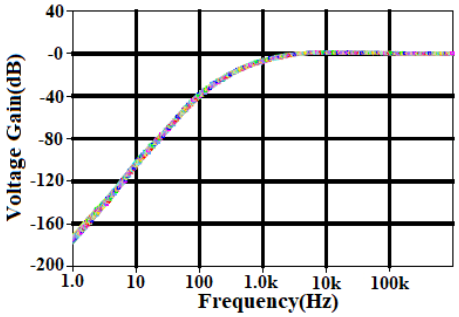


Fig. 4.17 Monte Carlo analysis of voltage gain of fractional order high pass ladder filter.

II. Fractional order band-pass filter

A Fractional Order band pass filter circuit is used to show the functionality of proposed grounded positive fractional order inductor shown in Fig. 4.18(a). The transfer function of the fractional order band pass filter and its magnitude may be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{s^{\alpha}}{RC_{\alpha}}}{s^{2\alpha}+\frac{s^{\alpha}}{RC_{\alpha}}+\frac{1}{L_{\alpha}C_{\alpha}}} \tag{4.17}$$

$$|T(j\omega)|_{FBP} = \left(\frac{\omega^{\alpha}}{RC_{\alpha}}\right)/|D(j\omega)| \tag{4.18}$$

where the value of $|D(j\omega)|$ (denominator of eq. (4.17)) with $L_{\alpha} = \frac{C_{\alpha}}{g_{m1}g_{m2}}$ is given as:

$$|D(j\omega)| = \sqrt{\begin{Bmatrix} \omega^{4\alpha} + \frac{2\omega^{3\alpha}}{RC_{\alpha}}\cos\left(\frac{\alpha\pi}{2}\right) + \omega^{2\alpha}\left\{\frac{2g_{m1}g_{m2}\cos(\alpha\pi)}{C_{\alpha}^2}\right\} \\ + \frac{1}{RC_{\alpha}} + \omega^{\alpha}\left(2\frac{g_{m1}g_{m2}\cos\left(\frac{\alpha\pi}{2}\right)}{RC_{\alpha}^3}\right) + \left(\frac{g_{m1}g_{m2}}{C_{\alpha}^2}\right)^2 \end{Bmatrix}} \tag{4.19}$$

The resonant frequency of the fractional band pass filter may be obtained by differentiating eq. (4.19) with respect to ω^{α} and equating to zero. Thus, following equation is obtained as:

$$\left(\omega_r^{2\alpha} - \frac{g_{m1}g_{m2}}{C_{\alpha}^2}\right)\left\{\omega_r^{2\alpha} + \frac{1}{RC_{\alpha}}\omega_r^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + \frac{g_{m1}g_{m2}}{C_{\alpha}^2}\right\} = 0 \tag{4.20}$$

Now, the resonant frequency of the fractional band pass filter is obtained from eq. (4.20) as:

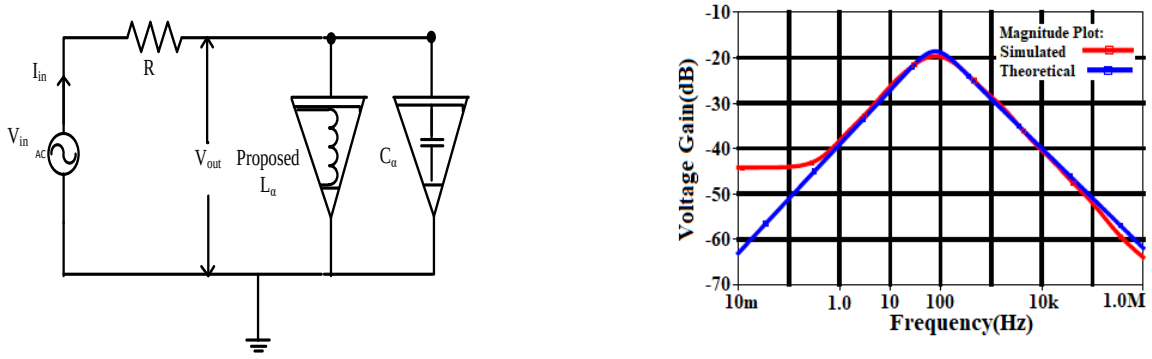
$$f_r = \frac{1}{2\pi}\left(\frac{g_{m1}g_{m2}}{C_\alpha^2}\right)^{\frac{1}{2\alpha}} = \frac{1}{2\pi}\left(\frac{1}{L_\alpha C_\alpha}\right)^{\frac{1}{2\alpha}} \quad (4.21)$$

Quality factor (Q_O) [131] of fractional band pass filter may be written as:

$$Q_O = \frac{-1}{2\cos\left(\frac{\delta}{\alpha}\right)} \quad (4.22)$$

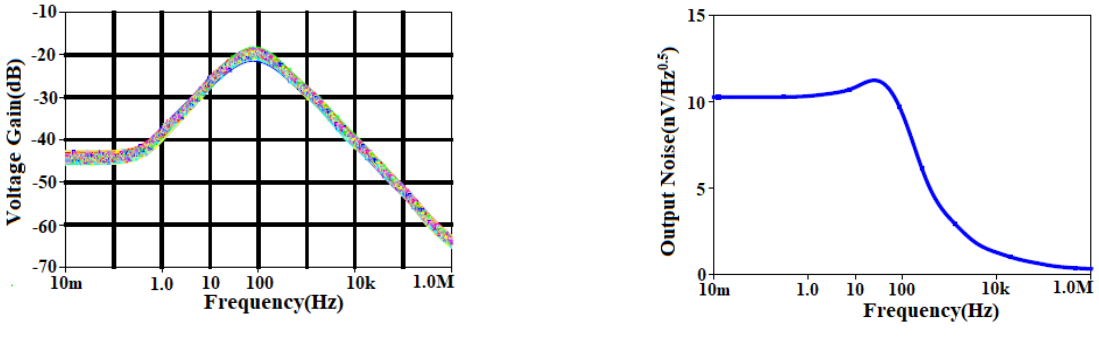
where $\delta = \cos^{-1}\left(-\frac{1}{2R}\sqrt{\frac{L_\alpha}{C_\alpha}}\right) = \cos^{-1}\left(-\frac{1}{2R}\sqrt{\frac{1}{g_{m1}g_{m2}}}\right)$.

It is evident from eqs. (4.17) and (4.22) that resonant frequency and quality factor of fractional band pass filter can be tuned by changing the bias current of OTA. The fractional band pass filter is verified for component values as $C_\alpha = +10\ \mu\Omega^{-1}s^{-0.6}$, $L_\alpha = 57.4\ \Omega^{+1}s^{+0.6}$, $I_B = +15\ \mu A$ and $R = 13.5\ k\Omega$. Figure 4.18(b) displays the simulated and theoretical plots of the fractional order band pass filter. The resonant frequency and quality factor of designed band pass filter are 80 Hz and 0.54 respectively. Monte Carlo analysis of voltage gain of fractional band pass ladder filter for 10 % Gaussian deviation in passive components with 500 runs is displayed in Fig. 4.19(a). The output noise of fractional band pass filter is depicted in Fig. 4.19(b). Power dissipation of the designed band-pass fractional filter is 0.288 mW.



(a) (b)

Fig. 4.18 Fractional order band pass filter. (a) Circuit, and (b) voltage gain.

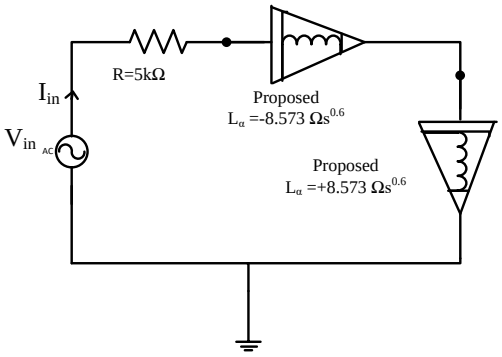


(a) (b)

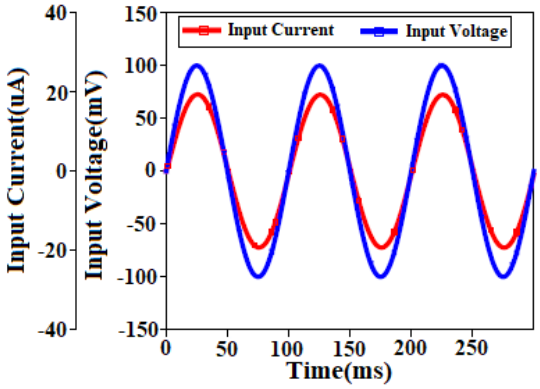
Fig. 4.19 Response of fractional band pass filter. (a) Monte Carlo analysis, and (b) output noise.

III. Fractional inductance cancellation circuit

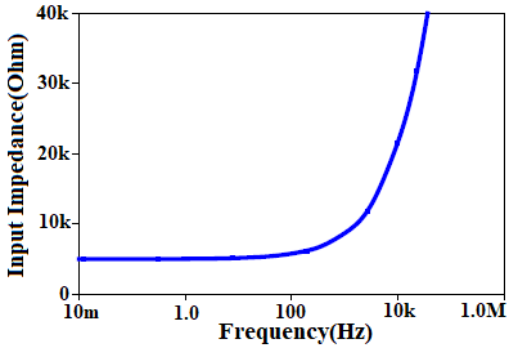
This section examines the utilization of simulated fractional inductance as a circuit for fractional inductance cancellation, as shown in Fig. 4.20(a). It can be observed from Fig. 4.20(a) that a resistor (R) of $5\ k\Omega$, simulated floating negative fractional inductor (L_{eq}) of $-8.573\ \Omega s^{0.6}$, simulated grounded positive fractional inductor (L_{eq}) of $8.573\ \Omega s^{0.6}$ and a sinusoidal input voltage source of amplitude (V_{in}) 100 mV at 10 Hz are connected in series. The time domain analysis of the fractional inductance cancellation circuit as shown in Fig. 4.20(b). Figure 4.20 (b) clearly shows that the input voltage (V_{in}) of 100 mV and input current (I_{in}) of 20 µA are in phase as the simulated floating negative fractional inductor in the circuit has been canceled by the simulated grounded positive fractional inductor and makes the circuit resistive of resistance $5\ k\Omega$. The frequency response of fractional inductance cancellation circuit is shown in Fig. 4.20(c). This figure shows that input impedance of fractional inductance cancellation circuit is $5\ k\Omega$ up to 100 Hz input frequency.



(a)



(b)



(c)

Fig. 4.20 (a) Fractional inductance cancelation circuit. (b) Transient response of fractional Inductance cancellation circuit. (c) Frequency response of fractional inductance cancelation circuit.

4.6 Comparison

The detailed comparisons among the proposed reconfigurable positive and negative fractional inductor circuits (discussed in section 4.2 to 4.4) with state of art circuits are given in Table 4.1. It is emphasized that the immittances being proposed have following advantageous features: use of less passive component, electronic tunability due to bias current of OTA, there is no component matching constraints, working in positive and negative mode without change in topology, low chip area, low power consumption, and high figure of merit.

Table 4.1 Comparison of the developed fractional order inductor with previously published ones.

Reference	Name of Active block	No. of passive component		Grounded/ Floating	Technology (nm)	Transistor count	Tunability	Change in topology	Power dissipation (mW)	Chip area	Mode of operation
		R	C_α								
[56]	CFOA-4, OTA-2	1	1	Floating	-	-	YES	-	NA	NA	Positive
[140]	Op-amp-2	4	1	Grounded	-	-	NO	-	NA	NA	Positive
[141]	Op-amp-2	4	1	Grounded	-	-	NO	-	NA	NA	Positive
[142]	Op-amp-2	4	1	Grounded	-	-	NO	-	NA	NA	Positive
[143]	Op-amp-2	4	1	Grounded	-	-	NO	-	NA	NA	Positive
[144]	CFOA-4	4	1	Floating	-	-	NO	-	NA	NA	Positive
[145]	CFOA-1	2	1	Grounded	-	-	NO	-	NA	NA	Positive
[146]	OTA-1, DVB-1	1	1	Grounded	350	75	YES	-	20	0.23 mm^2	Positive
[147]	OTA-2	0	1	Grounded	-	-	YES	-	NA	NA	Positive
Proposed	OTA-2, MOS switch-4, Inverter-1	0	1	Grounded	90	30	YES	NO	0.863	794.1 μm^2	Positive & Negative
Proposed	OTA-2, MOS switch-4, Inverter-1	0	1	Floating	90	30	YES	NO	0.863	794.1 μm^2	Positive & Negative

A careful examination of Table 4.1 reveals that these circuits:

a. Need two or more passive components for realization [140,141,142,143,144,145,146].
b. Require more than one active block [56,140,141,142,143,144,146,147].
c. Presented in [140,141,142,143,144,145] do not possess tunability.

d. Realize only positive fractional order inductor circuits [56,140,141,142,143,144,145,146,147].
e. Reported in [140,141,142,143] are based on Operational amplifier based and are therefore limited by slew rate. Such limitation does not exist in [56,144,145,146,147] as these are based on CFOA [56,144,145], and OTA [146,147].

4.7 Summary

This chapter presented an electronically tunable grounded and floating fractional-order inductor. It is capable of functioning in both positive and negative modes without any alteration in its topology. Analysis of proposed circuits with parasitic components investigated mathematically. In addition, proposed circuits are free from any components matching constraints. By altering the OTA's bias current, the suggested circuits' input impedance can be adjusted. The post layout of the frequency response of all proposed inductors followed the pre layout. Supply voltage variation analysis, corner analysis, Monte Carlo analysis and temperature effect analysis of the frequency response of the proposed circuit has been conducted, accompanied via supporting results that illustrate the good performance of the circuit. Finally, a fractional order high pass ladder filter, fractional inductance cancelation circuit, and fractional order band pass filter are included to show the applicability of proposed circuits. These fractional filters show lower frequency (Hz range) operation of the designed circuit, which may be useful in biomedical instruments. However, higher frequency (kHz range) operation of designed fractional inductors circuit may be suitable in modelling of different types of tissues.

CHAPTER 5

CCTA BASED MUTUALLY COUPLED CIRCUIT

In the previous chapter, fractional order devices are discussed. This chapter describes a tunable Synthetic Transformer (ST) namely Mutual Coupled Circuit (MCC) based on Current Conveyor Transconductance Amplifier (CCTA). The proposed circuit consists of two CCTAs, two capacitors, three resistors, and four MOS switches and can be configured in four different pairs of mutual coupled circuits through appropriate setting of MOS switch. The proposed MCC does not require component matching condition. Self-inductance, mutual inductance, and resonant frequency can be tuned by bias current of CCTA. Furthermore, non-ideal effects on the proposed MCC are discussed. Performance of proposed circuit is evaluated by pre-layout and post-layout simulation using 90 nm CMOS process technology. A double tuned band pass filter is shown as an application. The impact of supply voltage and temperature variation is examined and a maximum deviation of 3.326% and 16.8% respectively are observed in resonant frequency of DTBPF. The impact of differences in components is also examined by Monte Carlo analysis. The output noise spectral density of DTBPF at resonant frequency is observed to be 102.489 $\mathbf{nV/\sqrt{Hz}}$ whereas the total harmonic distortion is observed within 1.3% for peak input voltage range 0.05V to 3.5 V. The power consumption of DTBPF circuit is 5.16 **mW** at 100 µA bias current of CCTA**.**

5.1 Proposed mutually coupled circuit

The dot convention is used in passive transformers to create four pairs of mutually connected coils [209]. The reference polarity of the mutual voltage in the second coil is positive at the dotted terminal if current flows into the dotted terminal of the first coil. The mutual voltage in the second coil has a reference polarity of negative at the dotted terminal if a current departs the dotted terminal of the first coil. As a result, an MCC may produce four separate pairs of mutually connected circuits.

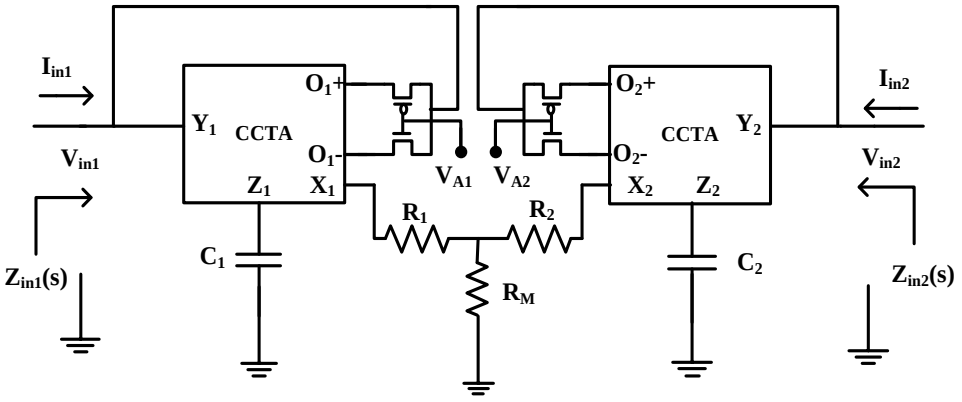


Fig. 5.1 Proposed mutually coupled circuit.

Here, a CCTA-based tunable MCC with a single topology that can function in four distinct MCC pairings is suggested. The circuit is created using the Gorski Popiel Technique [208], which involves embedding a resistive T-shaped network in a conventional impedance converter circuit to create a mutually connected circuit. As seen in Fig. 5.1, the proposed MCC makes use of four MOS-based switches, two CCTAs, two capacitors, and three resistors.

The operation of the circuit depends on voltages applied atV_{A1} and V_{A2}. The Proposed MCC and its equivalent transformer circuit for V_{A1}= V_{A2} = High is illustrated in Fig. 5.2.

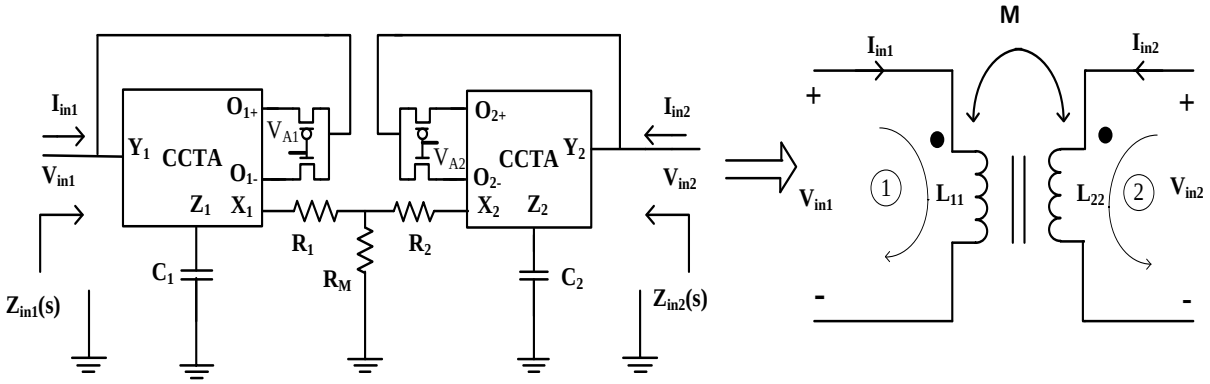


Fig. 5.2 Proposed MCC and its equivalent transformer circuit for V_{A1} = V_{A2} = High.

Currents at X_1 and X_2 terminals of the MCC as mentioned in Fig. 5.2 may be expressed as:

$$I_{X1} = \frac{sC_1}{g_{m1}} I_{in1} \; ; \; I_{X2} = \frac{sC_2}{g_{m2}} I_{in2} \tag{5.1}$$

Now, applying KVL between X_1 and X_2 terminals of CCTAs and grounded terminal of R_M resistor gives V_{in1} and V_{in2} respectively as:

$$V_{in1} = (R_1 + R_M)I_{X1} + R_M I_{X2} \tag{5.2a}$$

$$V_{in2} = (R_2 + R_M)I_{X2} + R_M I_{X1} \tag{5.2b}$$

Substitute the values of $I_{X1}$and I_{X2} from eq. (5.1) into eq. (5.2a-5.2b), we get following equations of port relations of MCC for V_{A1}= V_{A2} = High may be written as:

$$V_{in1} = \frac{sC_1(R_1+R_M)}{g_{m1}} I_{in1} + \frac{sC_2 R_M}{g_{m2}} I_{in2} \tag{5.3a}$$

$$V_{in2} = \frac{sC_1 R_M}{g_{m1}} I_{in1} + \frac{sC_2(R_2+R_M)}{g_{m2}} I_{in2} \tag{5.3b}$$

It is observed from the equivalent circuit of proposed MCC as shown in Fig. 5.2 that currents are entering at dotted terminal. Hence, standard equations of port relations of MCC (for V_{A1}= V_{A2} = High) may be written as:

$$V_{in1} = s(L_{11} + M_{11})I_{in1} + sM_{12} I_{in2} \tag{5.4a}$$

$$V_{in2} = sM_{21}I_{in1} + s(L_{22} + M_{22})I_{in2} \quad (5.4b)$$

Similarly, standard equations of port relations of MCC for other three combinations of gate voltages V_{A1} and V_{A2} may be expressed as:

$$V_{in1} = -s(L_{11} + M_{11})I_{in1} - sM_{12}I_{in2} \quad (5.5a)$$

$$V_{in2} = -sM_{21}I_{in1} - s(L_{22} + M_{22})I_{in2} \quad (5.5b)$$

(forV_{A1}= Low, V_{A2} = Low)

$$V_{in1} = -s(L_{11} + M_{11})I_{in1} + sM_{12}I_{in2} \quad (5.6a)$$

$$V_{in2} = -sM_{21}I_{in1} + s(L_{22} + M_{22})I_{in} \quad (5.6b)$$

(forV_{A1}= Low, V_{A2} = High)

$$V_{in1} = +s(L_{11} + M_{11})I_{in1} - sM_{12}I_{in2} \quad (5.7a)$$

$$V_{in2} = +sM_{21}I_{in1} - s(L_{22} + M_{22})I_{in2} \quad (5.7b)$$

(forV_{A1}= High, V_{A2} =Low)

where $L_{11} = \frac{C_1R_1}{g_{m1}}$; $L_{22} = \frac{C_2R_2}{g_{m2}}$; $M_{11} = M_{21} = \frac{C_1R_M}{g_{m1}}$; $M_{12} = M_{22} = \frac{C_2R_M}{g_{m2}}$.

Like passive transformer, dot convention can be applied in an active transformer by providing high or low gate voltage (V_{A1} and V_{A2}) of MOS switch. If both V_{A1} and V_{A2} are high or low, then voltage and current relation at port 1 and port 2 of the proposed circuit will be like current is entering at the dotted terminal. Similarly, if either V_{A1} or V_{A2} is high or low, then voltage and current relation at port 1 and port 2 of the proposed circuit will be like current is leaving at the dot terminal. Thus, four different combinations of V_{A1} and V_{A2} gate voltage of MOS switch gives four different pairs of mutual coupled circuit. The switch setting, schematic of configuration and its symbol are mentioned in Table 5.1. The generic standard port equations of ST [208] are defined as:

$$V_{in1} = s(\pm L_{11} \pm M_{11})I_{in1} \pm sM_{12}I_{in2} \quad (5.8a)$$

$$V_{in2} = \pm sM_{21}I_{in1} \pm s(L_{22} + M_{22})I_{in2} \quad (5.8b)$$

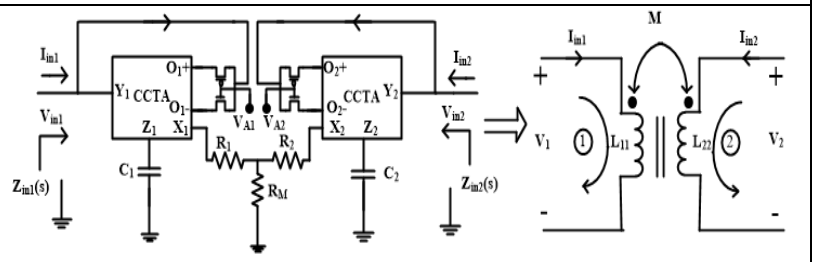
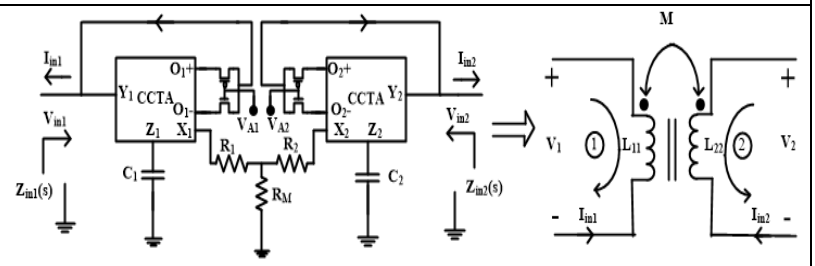
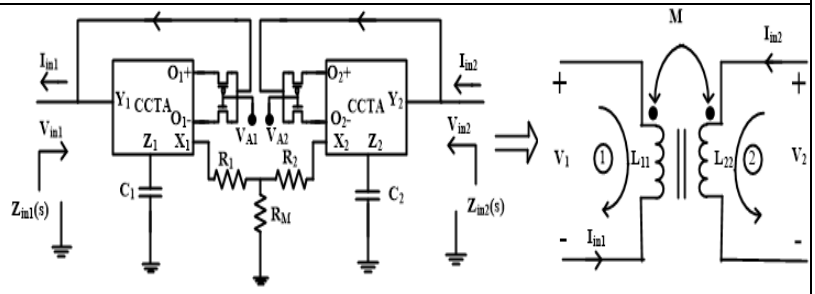
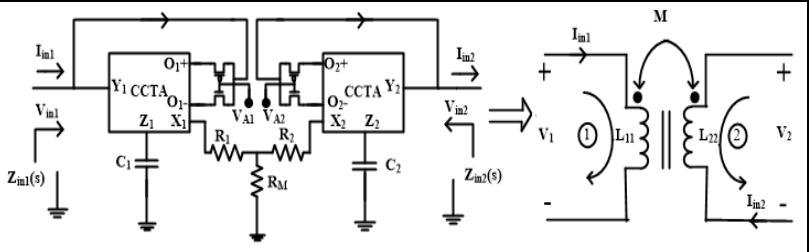
Another way of representation of eqs. (5.8a-5.8b) in term of self and mutual inductance of primary and secondary winding given as:

$$V_{in1} = \pm sL_PI_{in1} \pm sM_{12}I_{in2} \quad (5.9a)$$

$$V_{in2} = \pm sM_{21}I_{in1} \pm L_SI_{in2} \quad (5.9b)$$

where $L_P = L_{11} + M_{11}$; $L_S = L_{22} + M_{22}$ (5.10)

Table 5.1 MCC is configured in four different pairs of mutual coupled circuits.

Configuration	Switch Setting	Self Inductance Components	Mutual Inductance Components	Schematic of the Configuration and its Symbol
1	V_{A1}=H ; V_{A2}=H	$L_{11}=\frac{C_1R_1}{g_{m1}}$ $M_{11}=\frac{C_1R_M}{g_{m1}}$ $L_{22}=\frac{C_2R_2}{g_{m2}}$ $M_{22}=\frac{C_2R_M}{g_{m2}}$	$M_{12}=\frac{C_2R_M}{g_{m2}}$ $M_{21}=\frac{C_1R_M}{g_{m1}}$	
2	V_{A1}=L ; V_{A2}= L	$L_{11}=-\frac{C_1R_1}{g_{m1}}$ $M_{11}=-\frac{C_1R_M}{g_{m1}}$ $L_{22}=-\frac{C_2R_2}{g_{m2}}$ $M_{22}=-\frac{C_2R_M}{g_{m2}}$	$M_{12}=-\frac{C_2R_M}{g_{m2}}$ $M_{21}=-\frac{C_1R_M}{g_{m1}}$	
3	V_{A1}=L ; V_{A2}= H	$L_{11}=-\frac{C_1R_1}{g_{m1}}$ $M_{11}=-\frac{C_1R_M}{g_{m1}}$ $L_{22}=\frac{C_2R_2}{g_{m2}}$ $M_{22}=\frac{C_2R_M}{g_{m2}}$	$M_{12}=\frac{C_2R_M}{g_{m2}}$ $M_{21}=-\frac{C_1R_M}{g_{m1}}$	
4	V_{A1}=H; V_{A2}=L	$L_{11}=\frac{C_1R_1}{g_{m1}}$ $M_{11}=\frac{C_1R_M}{g_{m1}}$ $L_{22}=-\frac{C_2R_2}{g_{m2}}$ $M_{22}=-\frac{C_2R_M}{g_{m2}}$	$M_{12}=-\frac{C_2R_M}{g_{m2}}$ $M_{21}=\frac{C_1R_M}{g_{m1}}$	

L- Low; H – High.

Table 5.1 summarizes various configurations of Fig. 5.1 and corresponding circuit schematics for better visualization. The components (L_{11}, M_{11}) and (L_{22}, M_{22}) represent self-inductance of primary and secondary of transformer respectively. M_{12} and M_{21} refer to mutual inductance of transformer. A close observation of Table 5.1 reveals that self-inductance components and

mutual inductances components depend on transconductance of CCTA. Therefore, electronic tunability of this inductance is possible through bias current of CCTAs. Considering equal capacitance and transconductance values of both CCTAs, the coupling coefficient (k) of MCC may be written as:

$$k = \frac{\pm M}{\sqrt{(\pm L_1 \pm M)(\pm L_2 \pm M)}} \tag{5.11}$$

The values of coupling coefficient for no coupling and perfect coupling are 0 and 1 respectively.

5.2 Non-ideal analysis

In practice, the parasitic components are associated with different ports of CCTA and show their presence in the form of parallel combination of capacitors and resistors at Y, Z, O_+, and O_- ports, and a series resistance at X port. Parasitic components of the CCTA have been discussed in chapter 2. Now, the proposed MCC of Fig. 5.1 is modified as Fig. 5.3.

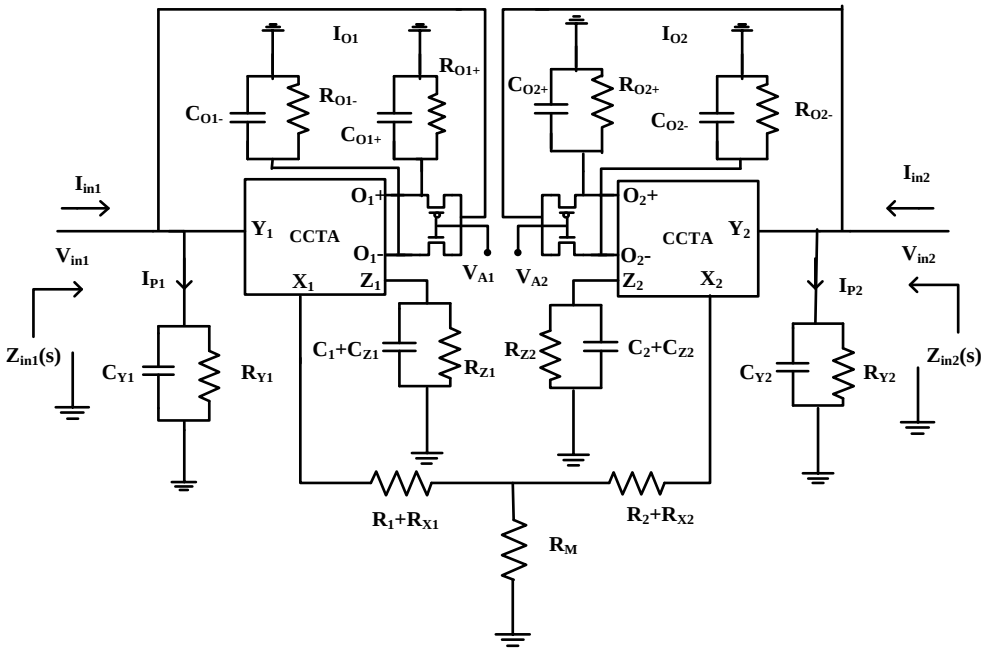


Fig. 5.3 Proposed MCC with parasitic components.

The currents I_{X1} and I_{X2} are flowing through X_1 and X_2 terminals of CCTAs, may be written as:

$$I_{X1} = \mp \frac{s(C_1+C_{Z1})R_{Z1}+1}{R_{Z1}g_{m1}}(I_{in1} - I_{P1}) \tag{5.12}$$

$$I_{X2} = \mp \frac{s(C_1+C_{Z2})R_{Z2}+1}{R_{Z2}g_{m2}}(I_{in2} - I_{P2}) \tag{5.13}$$

The currents I_{P1} and I_{P2} are small in magnitude because impedances seen at Z_1 and Z_2 terminal of CCTAs are high. Thus, these currents can be neglected from eq. (5.12) and eq. (5.13)

respectively. Now, applying KVL between X_1 and X_2 terminals of CCTAs and grounded terminal of R_M resistor gives V_{in1} and V_{in2} respectively as:

$$V_{in1} = -(R_{X1} + R_1 + R_M)I_{X1} - R_M I_{X2} \tag{5.14}$$

and

$$V_{in2} = -R_M I_{X1} - (R_{X2} + R_2 + R_M)I_{X2} \tag{5.15}$$

Using eqs. (5.12) and (5.13), eqs. (5.14) and (5.15) are modified as:

$$V_{in1}=\pm[(R_{X1} + R_1 + R_M)\frac{s(C_1+C_{Z1})+1/R_{Z1}}{g_{m1}}]I_{in1} \pm R_M \frac{s(C_2+C_{Z2})+1/R_{Z2}}{g_{m2}} I_{in2} \tag{5.16}$$

and

$$V_{in2}=\pm R_M \frac{s(C_1+C_{Z1})+1/R_{Z1}}{g_{m1}} I_{in1} \pm [(R_{X2} + R_2 + R_M)\frac{s(C_2+C_{Z2})+\frac{1}{R_{Z2}}}{g_{m2}}]I_{in2} \tag{5.17}$$

respectively.

Since the values of R_{Z1} and R_{Z2} are very large, eq. (5.16) and eq. (5.17) may be rewritten as:

$$V_{in1}=\pm[(R_{X1} + R_1 + R_M)\frac{s(C_1+C_{Z1})}{g_{m1}}]I_{in1} \pm R_M \frac{s(C_2+C_{Z2})}{g_{m2}} I_{in2} \tag{5.18}$$

and

$$V_{in2}=\pm R_M \frac{s(C_1+C_{Z1})}{g_{m1}} I_{in1} \pm [(R_{X2} + R_2 + R_M)\frac{s(C_2+C_{Z2})}{g_{m2}}]I_{in2} \tag{5.19}$$

respectively.

Now, self-inductance and mutual inductance with parasitic components of CCTA for four different pairs mutual coupled circuit can be obtained using eq. (5.18) and eq. (5.19) and are mentioned in Table 5.2. The effect of parasitic components of CCTA on self-inductance and mutual inductance can be minimized by selecting $R_1 >> R_{X1}$, $R_2 >> R_{X2}$, $C_1 >> C_{Z1}$, and $C_2 >> C_{Z2}$. Then eq. (5.18) and eq. (5.19) are reduced to their corresponding ideal eq. (5.4 - 5.7).

Frequency limitation of operation of the proposed circuit at low and high frequency may be obtained by considering parasitic components at Z and X terminals of CCTAs. The inclusion of the parasitic parts at the Z_1 terminal of CCTA necessitates the fulfillment of the subsequent inequality:

$$\left|R_{Z1} \parallel \frac{1}{j\omega C_{Z1}}\right| \gg \left|\frac{1}{j\omega C_1}\right| \Rightarrow \left|R_{Z1} \parallel \frac{1}{j\omega C_{Z1}}\right| \geq 10\left|\frac{1}{j\omega C_1}\right| \tag{5.20}$$

The following expression may be derived by taking the modulus of eq. (5.20) as:

$$\frac{R_{Z1}}{\sqrt{1+\omega^2 R_{Z1}^2 C_{Z1}^2}} \geq \frac{10}{\omega C_1} \tag{5.21}$$

Table 5.2 Self-inductance and mutual inductance with parasitic components of CCTA for four different configurations.

Configuration	Switch Setting	Voltage and Current Relation at Port 1 and Port 2	Self Inductance Components	Mutual Inductance Components
1	V_{A1}=H; V_{A2}= H	$V_{in1}=[(R_{X1}+R_1+R_M)\frac{s(C_1+C_{Z1})}{g_{m1}}]I_{in1}+R_M\frac{s(C_2+C_{Z2})}{g_{m2}}I_{in2}$ $V_{in2}=R_M\frac{s(C_1+C_{Z1})}{g_{m1}}I_{in1}+[(R_{X2}+R_2+R_M)\frac{s(C_2+C_{Z2})}{g_{m2}}]I_{in2}$	$L_{11}=\frac{(C_1+C_{Z1})(R_1+R_{X1})}{g_{m1}}$ $M_{11}=\frac{(C_1+C_{Z1})R_M}{g_{m1}}$ $L_{22}=\frac{(C_2+C_{Z2})(R_2+R_{X2})}{g_{m2}}$ $M_{22}=\frac{(C_2+C_{Z2})R_M}{g_{m2}}$	$M_{12}=\frac{(C_2+C_{Z2})R_M}{g_{m2}}$ $M_{21}=\frac{(C_1+C_{Z1})R_M}{g_{m1}}$
2	V_{A1}=L; V_{A2}= L	$V_{in1}=-[(R_{X1}+R_1+R_M)\frac{s(C_1+C_{Z1})}{g_{m1}}]I_{in1}-R_M\frac{s(C_2+C_{Z2})}{g_{m2}}I_{in2}$ $V_{in2}=-R_M\frac{s(C_1+C_{Z1})}{g_{m1}}I_{in1}-[(R_{X2}+R_2+R_M)\frac{s(C_2+C_{Z2})}{g_{m2}}]I_{in2}$	$L_{11}=-\frac{(C_1+C_{Z1})(R_1+R_{X1})}{g_{m1}}$ $M_{11}=-\frac{(C_1+C_{Z1})R_M}{g_{m1}}$ $L_{22}=-\frac{(C_2+C_{Z2})(R_2+R_{X2})}{g_{m2}}$ $M_{22}=-\frac{(C_2+C_{Z2})R_M}{g_{m2}}$	$M_{12}=-\frac{(C_2+C_{Z2})R_M}{g_{m2}}$ $M_{21}=-\frac{(C_1+C_{Z1})R_M}{g_{m1}}$
3	V_{A1}=L; V_{A2}= H	$V_{in1}=-[(R_{X1}+R_1+R_M)\frac{s(C_1+C_{Z1})}{g_{m1}}]I_{in1}+R_M\frac{s(C_2+C_{Z2})}{g_{m2}}I_{in2}$ $V_{in2}=-R_M\frac{s(C_1+C_{Z1})}{g_{m1}}I_{in1}+[(R_{X2}+R_2+R_M)\frac{s(C_2+C_{Z2})}{g_{m2}}]I_{in2}$	$L_{11}=-\frac{(C_1+C_{Z1})(R_1+R_{X1})}{g_{m1}}$ $M_{11}=-\frac{(C_1+C_{Z1})R_M}{g_{m1}}$ $L_{22}=\frac{(C_2+C_{Z2})(R_2+R_{X2})}{g_{m2}}$ $M_{22}=\frac{(C_2+C_{Z2})R_M}{g_{m2}}$	$M_{12}=\frac{(C_2+C_{Z2})R_M}{g_{m2}}$ $M_{21}=-\frac{(C_1+C_{Z1})R_M}{g_{m1}}$
4	V_{A1}=H; V_{A2}= L	$V_{in1}=[(R_{X1}+R_1+R_M)\frac{s(C_1+C_{Z1})}{g_{m1}}]I_{in1}-R_M\frac{s(C_2+C_{Z2})}{g_{m2}}I_{in2}$ $V_{in2}=R_M\frac{s(C_1+C_{Z1})}{g_{m1}}I_{in1}-[(R_{X2}+R_2+R_M)\frac{s(C_2+C_{Z2})}{g_{m2}}]I_{in2}$	$L_{11}=\frac{(C_1+C_{Z1})(R_1+R_{X1})}{g_{m1}}$ $M_{11}=\frac{(C_1+C_{Z1})R_M}{g_{m1}}$ $L_{22}=-\frac{(C_2+C_{Z2})(R_2+R_{X2})}{g_{m2}}$ $M_{22}=-\frac{(C_2+C_{Z2})R_M}{g_{m2}}$	$M_{12}=-\frac{(C_2+C_{Z2})R_M}{g_{m2}}$ $M_{21}=\frac{(C_1+C_{Z1})R_M}{g_{m1}}$
L- Low; H – High.				

Since, at very low frequency product of $\omega^2 R_{Z1}^2 C_{Z1}^2 \ll 1$, we get following expression of lower frequency condition of the designed circuit.

$$R_{Z1} \geq \frac{10}{\omega C_1} \Rightarrow f \geq \frac{10}{2\pi R_{Z1} C_1} = f_{L1} \tag{5.22}$$

Similar condition of low frequency of the designed circuit may be obtained using parasitic at Z_2 terminal of CCTA as:

$$R_{Z2} \geq \frac{10}{\omega C_2} \Rightarrow f \geq \frac{10}{2\pi R_{Z2} C_2} = f_{L2} \tag{5.23}$$

Now, X terminal of CCTA consists of a parasitic inductor (L_X) in series with parasitic resistor (R_X) at very high frequency. Then following constraint at X_1 terminal of CCTA must be satisfied:

$$R_1 \gg |R_{X1} + j\omega L_{X1}| \Rightarrow R_1 \geq 10 \times |R_{X1} + j\omega L_{X1}| \quad (5.24)$$

The following expression may be derived by expansion of eq. (5.24) as:

$$R_1 \geq 10 \times \sqrt{R_{X1}^2 + \omega^2 L_{X1}^2} \quad (5.25)$$

Since, at very high frequency product of $\omega L_{X1} \gg R_{X1}$, we get following expression of high frequency condition of the designed circuit as:

$$R_1 \geq 10 \times \omega L_{X1} \Rightarrow f \leq \frac{R_1}{20\pi \times L_{X1}} = f_{H1} \quad (5.26)$$

Similar condition of high frequency may be obtained by taking into account parasitic at X_2 terminal of CCTA as:

$$R_2 \geq 10 \times \omega L_{X2} \Rightarrow f \leq \frac{R_2}{20\pi \times L_{X2}} = f_{H2} \quad (5.27)$$

Now, the following frequency limitation of operation at low and high frequencies may be expressed using eqs. (5.22), (5.23), (5.26), and (5.27) as:

$$\frac{1}{2\pi} \max\left\{\frac{10}{R_{Z1}C_1}, \frac{10}{R_{Z2}C_2}\right\} \leq f \leq \frac{1}{2\pi} \min\left\{\frac{R_1}{10L_{X1}}, \frac{R_2}{10L_{X2}}\right\} \quad (5.28)$$

The following conditions can mitigate the effects of parasitic components on the proposed circuit.

a. The proposed circuit may operate properly at high frequency if R_1 and R_2 should meet the condition of $R_1 \geq 10 \times R_{X1}$ and $R_2 \geq 10 \times R_{X2}$.
b. The proposed circuit may operate properly at low frequency if C_1 and C_2 should meet the condition of $C_1 \geq 10 \times C_{Z1}$ and $C_2 \geq 10 \times C_{Z2}$.

The sensitivity of designed MCC might be acquired as the relative change in self-inductance and shared inductance with respect to circuit parameters. The following equations summarize the proposed MCC's sensitivity to passive, parasitic, and transconductance**.**

$$S_{R_1}^{L_{11}} = S_{C_1}^{L_{11}} = -S_{g_{m1}}^{L_{11}} = S_{R_{X1}}^{L_{11}} = S_{C_{Z1}}^{L_{11}} = 1 \quad (5.29)$$

$$S_{R_2}^{L_{22}} = S_{C_2}^{L_{22}} = -S_{g_{m2}}^{L_{22}} = S_{R_{X2}}^{L_{22}} = S_{C_{Z2}}^{L_{22}} = 1 \quad (5.30)$$

$$S_{R_M}^{M_{11}} = S_{C_1}^{M_{11}} = -S_{g_{m1}}^{M_{11}} = S_{C_{Z1}}^{M_{11}} = 1 \quad (5.31)$$

$$S_{R_M}^{M_{12}} = S_{C_2}^{M_{12}} = -S_{g_{m2}}^{M_{12}} = S_{C_{Z2}}^{M_{12}} = 1 \quad (5.32)$$

$$S_{R_M}^{M_{21}} = S_{C_1}^{M_{21}} = -S_{g_{m1}}^{M_{21}} = S_{C_{Z1}}^{M_{21}} = 1 \tag{5.33}$$

$$S_{R_M}^{M_{22}} = S_{C_2}^{M_{22}} = -S_{g_{m2}}^{M_{22}} = S_{C_{Z2}}^{M_{22}} = 1 \tag{5.34}$$

The amount of the sensitivity with regard to passive components, parasitic components, and transconductance is seen from equation (5.29-5.34) to be unity.

5.3 Application

The utility of the suggested MCC is exemplified in Fig. 5.4 by a double tuned band pass filter (DTBPF). One MCC, two capacitors, and two resistors are used in the DTBPF.

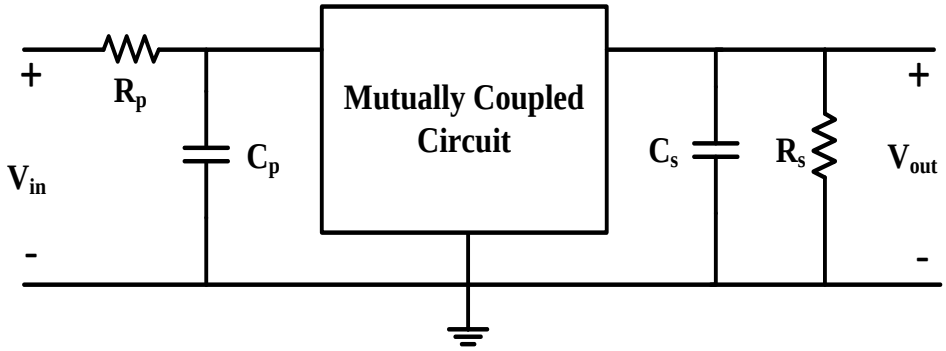


Fig. 5.4 Double tuned band pass filter circuit.

Transfer function of DTBPF as shown in Fig. 5.4 may be written as follows (ω_O, Q, and k denotes angular resonant frequency, quality factor, and coupling coefficient respectively):

$$T(s) = \frac{\frac{ks}{(1-k^2)Q\omega_O}}{\left[\left\{\left(\frac{s}{\omega_o}\right)^2 + \frac{s}{Q\omega_O} + \frac{1}{1-k}\right\}\left\{\left(\frac{s}{\omega_o}\right)^2 + \frac{s}{Q\omega_O} + \frac{1}{1+k}\right\}\right]} \tag{5.35}$$

where,

$$\omega_O = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_S C_S}};\ Q = \omega_P R_P C_P = \omega_S R_S C_S \tag{5.36}$$

The quality factor of the primary winding (Q_P) to the secondary winding (Q_S) of DTBPF can be written as:

$$Q_P = \omega_P R_P C_P \tag{5.37}$$

$$Q_S = \omega_S R_S C_S \tag{5.38}$$

The angular resonant frequency of the primary winding (ω_P) to the secondary winding (ω_S) of DTBPF may be obtained as:

$$\omega_P = \frac{1}{\sqrt{L_P C_P}} \tag{5.39}$$

$$\omega_S = \frac{1}{\sqrt{L_S C_S}} \tag{5.40}$$

5.4 Results and discussion

The verification of the designed circuit is done through PSpice simulator using 90 nm technology node. The aspect ratio of MOS transistors of CCTA is given in chapter 2 (Table 2.2). DC supply voltages and V_{bias} are chosen as ±1.2 V and +0.42 V, respectively. The layout of the CCTA circuit is depicted in Fig. 5.5. The layout of CCTA is designed using 90 nm technology node. The layout area is found to be 666.7 μm^2.

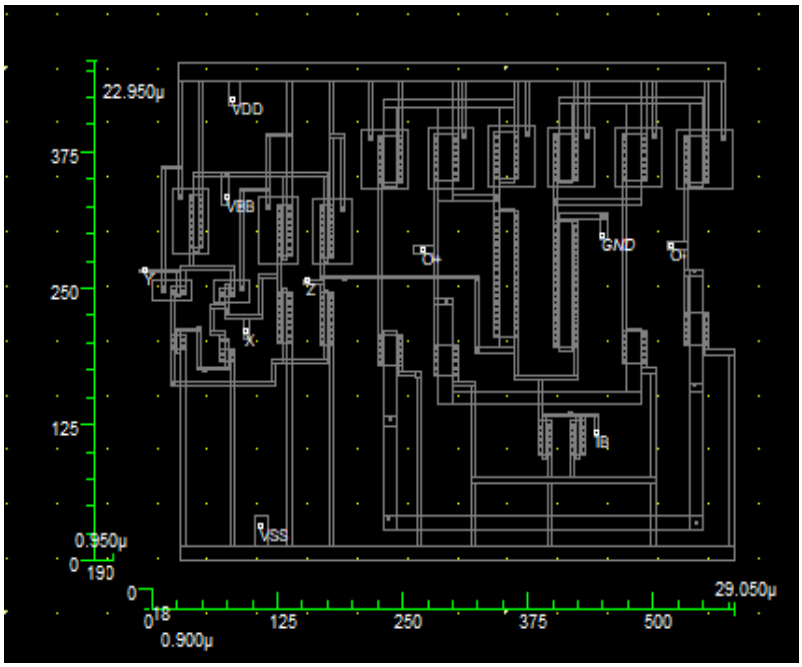
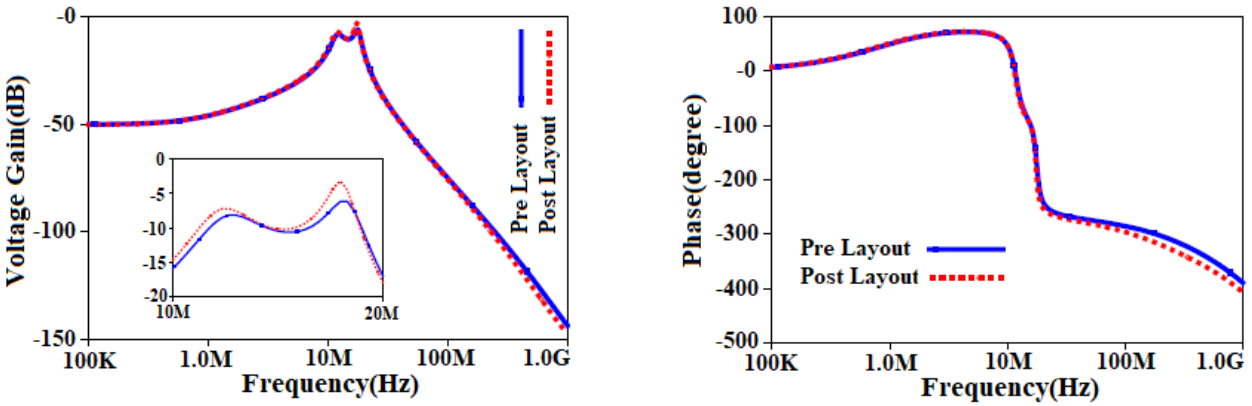


Fig. 5.5 Layout of CCTA.

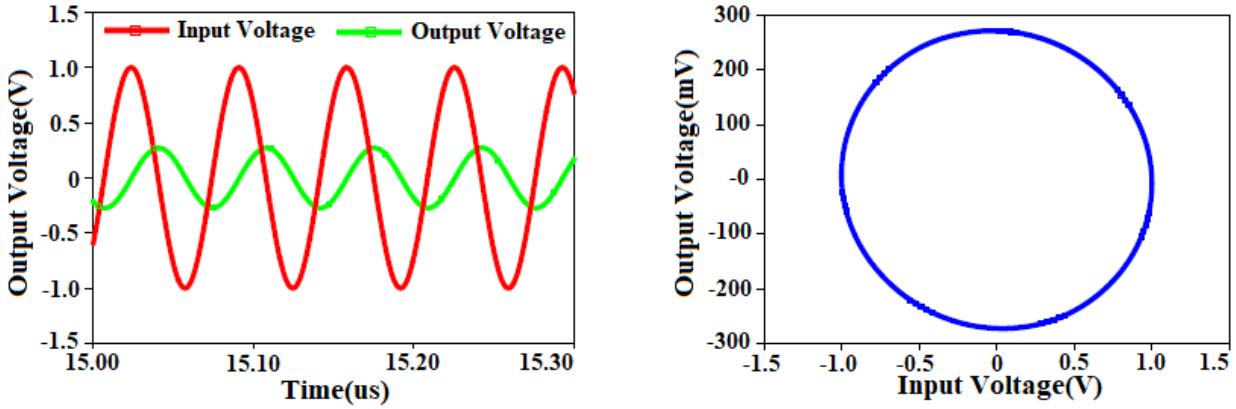
The frequency response of DTBPF is examined with settings of $V_{A1} = V_{A2} = -5V$ in the proposed MCC. The component values for the proposed MCC are chosen as $R_1 = R_2 = 1$ kΩ, $R_{X1} = R_{X2} = 50$ Ω, $R_M = 1.3$ kΩ, $C_1 = C_2 = 37.5$ pF, $C_{Z1} = C_{Z2} = 0.5$ pF, yielding $L_{11}=L_{22}= -24.072$ μH; $M_{11}=M_{12}= M_{21}=M_{22} = -31.294$ μH; $|-L_{11}-M_{11}| = |-L_{22}-M_{22}| = L_P = L_S = 55.366$ μH and k =0.553. The components external to MCC are taken as $R_S = R_P$=40 kΩ, $C_S = C_P$=2 pF which results in $f_P = f_S$= 14.77 MHz, and $Q_P = Q_S$=7.42. Pre-layout and post-layout plots of frequency response of the DTBPF circuit is illustrated in Fig. 5.6. It may be observed that post-layout simulation slightly deviates from pre-layout simulation which may be attributed to parasitics arising from layout.



(a) (b)

Fig. 5.6 Pre-layout and post-layout plot of frequency response of DTBPF circuit (a) magnitude, and (b) phase.

In addition, we examine the time-domain behavior of the DTBPF by applying a sine wave with an amplitude of 1 V and a frequency of 14.77 MHz to the input terminal of the DTBPF. The time domain response of DTBPF is displayed in Fig. 5.7(a) and the corresponding Lissajous pattern is displayed in Fig. 5.7(b). The Lissajous pattern shows a 90° phase shift between the input and output voltages of the DTBPF at a frequency of 14.77 MHz. The power consumption of DTBPF is 5.16 mW with 100 µA bias current from CCTA.



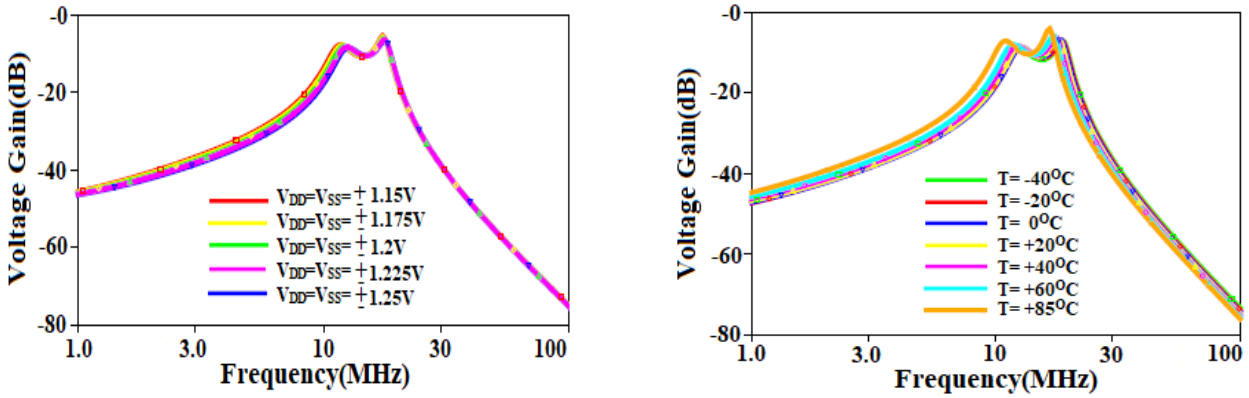
(a) (b)

Fig. 5.7 (a)Time domain response of DTBPF circuit, and (b) corresponding Lissajous pattern.

In practice, the performance of the DTBPF may vary due to supply voltage and temperature variations. The frequency response of DTBPF is plotted in Fig. 5.8(a) by varying supply from ±1.15 V to ±1.25 V and the variation of 3.33% is observed in the resonant frequency. For higher supply voltage the curve shifts toward right which a direct consequence of decrease in inductance value of MCC (larger transconductance for smaller overdrive voltage).

Impact of temperature variations on frequency response is also studied by varying temperature from -40°C to 85°C and the overall spread in resonant frequency is found to be within 14.8% in

the observed ranged frequency as shown in Fig. 5.8(b). The curve shifts towards left with increase in temperature due to increase in inductance value of MCC (lower transconductance due to decrease mobility for higher temperatures).



(a) (b)

Fig. 5.8 Frequency response of DTBPF for different (a) supply voltages, and (b) temperatures.

Further, the component values may drift from their intended values and affect the frequency response. Monte Carlo study is a valuable technique for determining the impact of component drift on the frequency response. The simulated frequency response under 10% Gaussian deviation in the passive components with 500 samples is illustrated in Fig. 5.9. It may be identified from Fig. 5.9 that maximum deviation in magnitude plot of DTBPF at resonant frequency (14.77MHz) is ±1.75 dB.

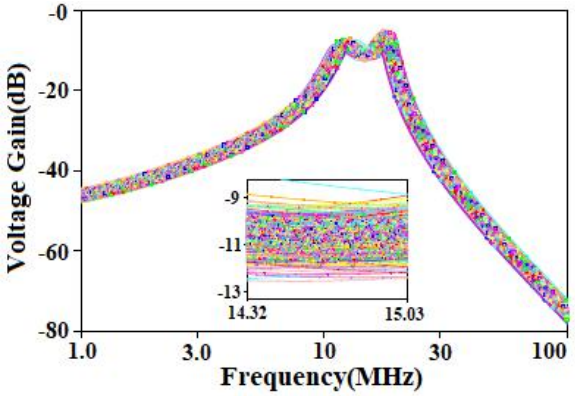


Fig. 5.9 Monte Carlo analysis of frequency response of DTBPF.

The process corner in monolithic integration significantly influences the performance of the proposed circuit. The Slow Slow (SS), Fast Fast (FF), and Nominal Nominal (NN) process corners have undergone thorough examination. The process corner variations of the provided circuit are illustrated in Fig. 5.10. The process, voltage, and temperature (PVT) fluctuations are accomplished by adjusting the supply voltage within the range of ±1.15 V to ±1.25 V and the

temperature within the range of -40˚C to +85˚C. Figure 5.10 illustrates that the current passing through a memristor in SS mode is lower than the current passing through the identical device in FF mode.

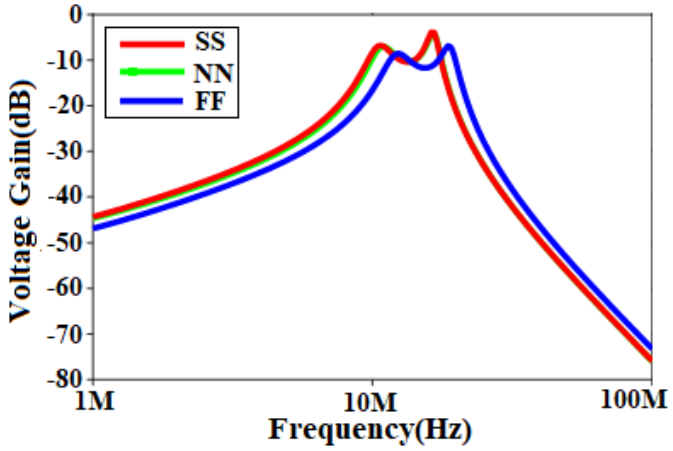


Fig. 5.10 Corner analysis of frequency response of DTBPF.

Coupling coefficient is an important performance parameter of a transformer. In passive transformer, the coupling coefficient (k) is the fraction of total flux emanating from one coil that links the other coil. A passive transformer is classified as loosely coupled, tightly coupled and perfect coupled [209] for the value of k<0.5, k>0.5, and k =1 respectively. Like passive transformer, MCC may also be classified as poor coupled, critical coupled, and over coupled as:

- Poor Coupled: - A MCC is said to be poor coupled when k<1/Q or kQ<1. In poor coupled ST based DTBPF circuit, resonant frequency (f_r=f_p=f_s) and peak frequencies (frequency at which maxima is observed in magnitude response) will be equal and voltage gain of DTBPF is increased at resonant frequency as the value of kQ is increased from 0 to 1.
- Critical coupled: - A MCC is said to be critically coupled when k=1/Q or kQ=1. Resonant frequency and peak frequencies of critically coupled DTBPF will be equal, and the value of voltage gain of the DTBPF at resonant frequency will be the highest.
- Over coupled: - A MCC is said to be over coupled when k>1/Q or kQ>1. In over coupled MCC based DTBPF circuit, resonant frequency and peak frequencies will be different, and voltage gain of the DTBPF at resonant frequency is dipped or decreased as the value of kQ is increased from 1. Relations between resonant frequency and peak frequencies may be obtained from ref. [210] as:

$$f_p = f_s = \sqrt{f_{UPPER}.f_{LOWER}} \tag{5.41}$$

Now, the bandwidth (B) of DTBPF may be obtained as:

$$\text{Bandwidth(B)} = \sqrt{2}(f_{UPPER} - f_{LOWER}) \tag{5.42}$$

Thus, f_{UPPER} and f_{LOWER} can be obtained as:

$$f_{UPPER} = f_r + \frac{B}{2\sqrt{2}} \tag{5.43}$$

$$f_{LOWER} = f_r - \frac{B}{2\sqrt{2}} \tag{5.44}$$

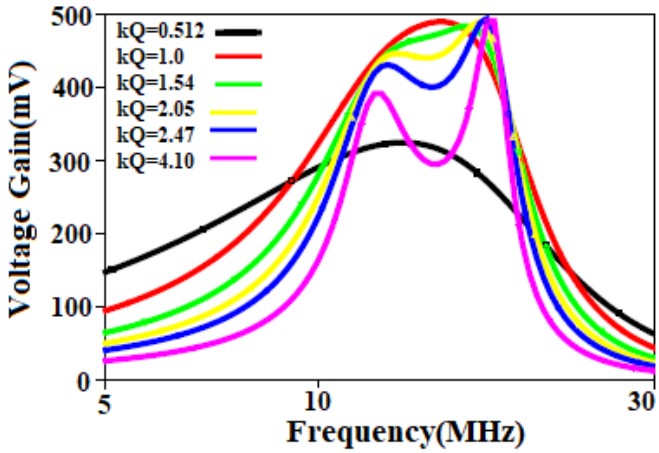


Fig. 5.11 Frequency response of DTBPF for different value of kQ.

Now, study of effect of kQ on frequency response of DTBPF can be obtained by varying the Q and fixed k = 0.553 as shown in Fig. 5.11. Table 5.3 shows the variation of voltage gain at resonant frequency (14.77 MHz) and bandwidth of DTBPF by varying quality factor Q for $R_L = R_S \in [5\ k\Omega, 25\ k\Omega]$. The quality factor Q has been calculated mathematically using eq. (5.37) and eq. (5.38). The following observations can be made from Fig. 5.11 and Table 5.3.

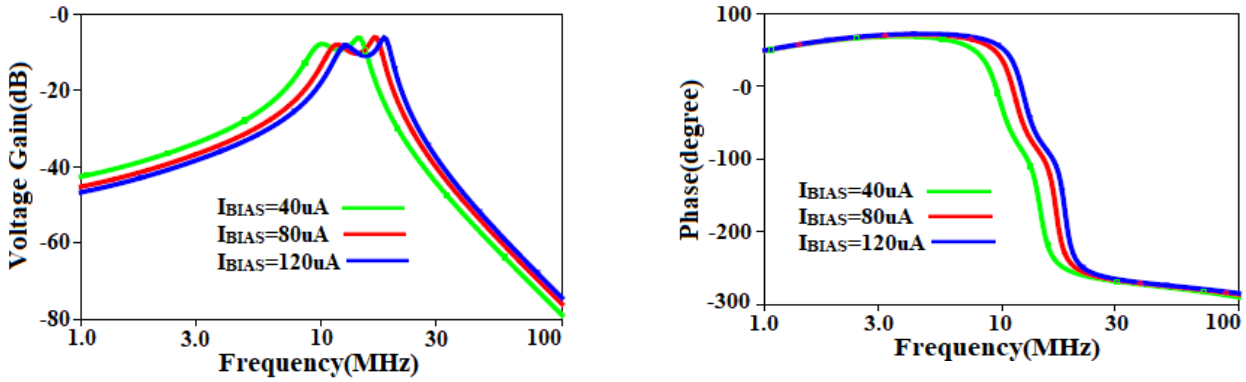
- If kQ< 1, then voltage gain of DTBPF at resonant frequency is increasing by increasing the value of kQ. Resonant frequency and peak frequencies of DTBPF are same i.e., 14.77 MHz. Therefore, DTBPF circuit shows single tune frequency.
- If kQ=1, then voltage gain of DTBPF at resonant frequency is maximum i.e., 500 mV. Resonant frequency and peak frequencies of DTBPF are same i.e., 14.77 MHz, Thus DTBPF circuit shows single tune frequency.
- If kQ>1, then voltage gain of DTBPF at resonant frequency is dipping or decreasing from 500 mV due to splitting of peak frequencies from resonant frequency. Resonant frequency and peak frequencies of DTBPF are different, thus DTBPF circuit shows double tune frequency. Bandwidth of DTBPF will be wider due to splitting of peak frequencies from resonant frequency. Therefore, values of f_{LOWER} and f_{UPPER} are decreased and increased

respectively. However, bandwidth at peak frequencies will be narrow due to increment of the value of Q, which increases selectivity of DTBPF.

Table 5.3 Variation in bandwidth and voltage gain of DTBPF with respect to variation in Q while k is fixed.

Types of Coupling	$R_L = R_S$ (kΩ)	Q	kQ	Voltage Gain at f_r	f_{LOWER}(MHz)	f_{UPPER}(MHz)	B(MHz)
Poor	5	0.93	0.51	0.3	14.77	14.77	-
Critical	9.68	1.79	1	0.5	14.77	14.77	-
Over	15	2.78	1.54	0.48	12.27	17.27	7.08
Over	20	3.71	2.05	0.42	11.99	17.55	7.86
Over	25	4.63	2.47	0.38	11.96	17.58	7.95

Electronic tunability of proposed ST is obtained by varying the bias current of CCTA from 40 µA to 120 µA in step of 40 µA and corresponding magnitude response of DTBPF is shown in Fig. 5.12. An increase in resonant frequency of DTBPF is observed with incrementing bias current which may be attributed to enhancement in transconductance values leading to decrease in inductance value. These facts culminate into increasing resonant frequency of the DTBPF.



(a) (b)

Fig. 5.12 Frequency response of double tuned band pass filter for different bias current. (a) Magnitude, and (b) phase.

The input and output noise response with respect to frequency of DTBPF circuit is obtained using SPICE noise model as shown in Fig. 5.13. This figure shows that the value of output noise spectral density at f_{UPPER}, f_r, and f_{LOWER} are observed to be (-135.30 dB = 171.72×10^{-9}) V/$\sqrt{\text{Hz}}$, (-139.786 dB = 102.489×10^{-9}) V/$\sqrt{\text{Hz}}$, and (-132.46 dB = 238.2×10^{-9}) V/$\sqrt{\text{Hz}}$ respectively.

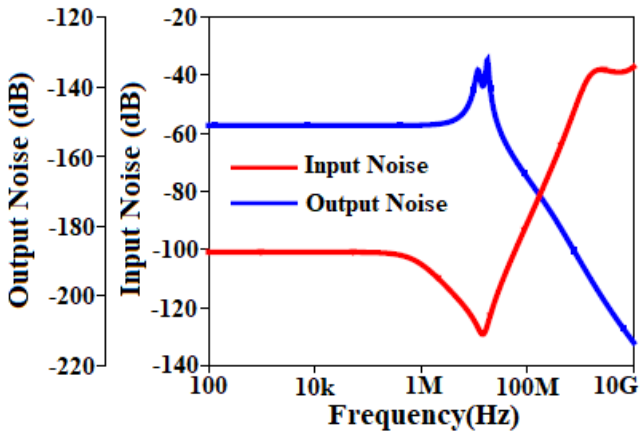


Fig. 5.13 Noise response of proposed synthetic transformer.

Total harmonic distortion (THD) is a crucial to observe the nonlinearity of the circuit. Therefore, the percentage of THD with respect to peak input voltage is displayed in Fig. 5.14. This response is obtained by applying the sinusoidal voltage signal of different peak of 14.77 MHz at the input terminal of the DPTF. Figure 5.14 shows that the output distortion within 1.3% for peak input voltage range 0.05 V to 3.5 V, which is low enough.

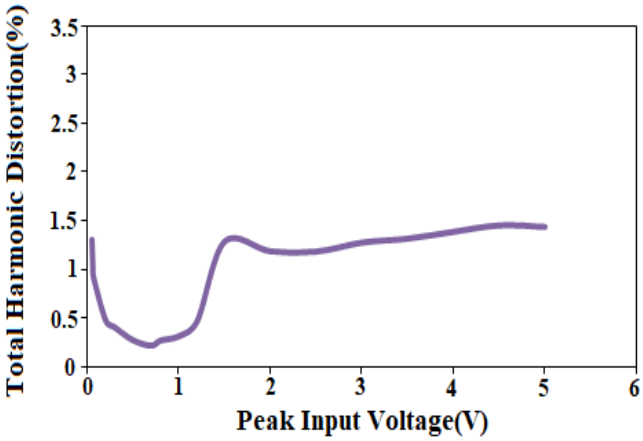


Fig. 5.14 Total harmonic distortion of output voltage of band pass filter circuit.

5.5 Comparison

A comparison table of the performance of DTBPF of the proposed circuit in terms of total harmonic distortion, quality factor, power dissipation, resonant frequency, and output noise is given in Table 5.4. The resonant frequency and quality factor of the designed circuit are 14.77 MHz and 7.42 respectively. The constructed circuit uses 5.16 mW of power, which is less than the amount mentioned in [154,157]. The output noise of the designed circuit at the resonant frequency is 102.489 $nV/\sqrt{Hz}$, which is lower than the output noise described in [155]. When

compared to [157,158,161,162,164], the total harmonic distortion of the proposed circuit at resonance frequency is less than 1.3% for the peak input voltage range of 0.05 V to 3.5 V.

Table 5.4 Comparison of performance of DTBPF of published MCC with DTBPF of the proposed MCC.

Ref.	**[154]**	**[155]**	**[157]**	**[158]**	**[159]**	**[160]**	**[161]**	**[162]**	**[164]**	**Proposed**
Total Harmonic Distortion	NA	NA	Within 3% for peak input voltage 2V	Within 3% for peak input voltage 800mV	NA	NA	Within 2% for peak input voltage range 100 mV to 5.2 V	Within 4.03% for peak input voltage 65 mV	Within 0.08% for peak input voltage 150 mV	Within 1.3% for peak input voltage range 0.05V to 3.5 V
Quality Factor	7.07	7.07	5.77	6.952	5.77	5.77	3.19	5	5	7.42
Power dissipation	38 mW	NA	6 mW	2.77 mW	NA	3.8 mW	NA	NA	NA	5.16 mW
Resonant Frequency (f_r)	112.54 kHz	112.54 kHz	9.2 MHz	5 MHz	95.5 kHz	918.88 kHz	1.69 MHz	1.59 MHz	1.59 MHz	14.77 MHz
Output Noise at f_r	NA	120 $nV/\sqrt{Hz}$	NA	NA	NA	NA	NA	NA	NA	102.489 $nV/\sqrt{Hz}$
NA - NOT Available										

5.6 Summary

This paper reports on a CCTA-based electronically tunable MCC that provides four different pairs of coupled circuits by appropriate setting of MOS switch. The proposed circuit comprises of two CCTAs, two capacitors, three resistors, and four MOS switches. The proposed MCC does not require component matching conditions. In addition, we mathematically investigate the interpretation of the proposed MCC including parasitic components. Moreover, the proposed MCC is used in a double tuned band pass filter to illustrate the performance of the circuit. Studies of power supply voltage fluctuations, temperature fluctuations, Monte Carlo analysis, noise analysis, and THD are examined with supporting outcome. The bias current of CCTA makes resonant frequency and quality factor of DTBPF adjustable. Therefore, the proposed MCC may be suitable in the application of instrumentation, measurement, and analog telecommunication.

CHAPTER 6

FLUX & CHARGE CONTROLLED MERMRISTORS

So far, linear elements such as resistor, capacitor, and inductor are discussed in previous chapters. Resistor is defined by the relationship between voltage and current, inductor is described by the relationship between current and flux, and capacitor is defined by the relation between charge and voltage. This chapter introduces a nonlinear element known as memristor. It provides the relationship between charge and flux. It is controlled by either charge or flux. Hence, this chapter reports ICCTA based charge and flux controlled memristor emulator. Both proposed circuits do not incorporate complex circuits such as analog multiplier circuits, passive inductors, and analog to digital converter circuits in their implementation, which is advantageous in terms of circuit realization. In addition, corner analysis of the developed memristor is also included. Furthermore, the non-ideal explanation of the designed memristors is mathematically examined. Meminductor emulator and memristor-based filter are designed to validate the effectiveness of the proposed circuits.

6.1 Flux controlled memristor emulator

This section discusses flux controlled grounded memristor emulator using ICCTA.

6.1.1 Proposed flux controlled memristor

A flux controlled grounded memristor emulator employing ICCTA is displayed in Fig. 6.1. It consists of a single ICCTA, one grounded resistor, one grounded capacitor, and two MOS switches (NMOS and PMOS). MOS switches are connected between O± and Y terminal of ICCTA. These MOS switches with high gate voltages and low gate voltages may drive the grounded memristor in incremental and decremental modes, respectively.

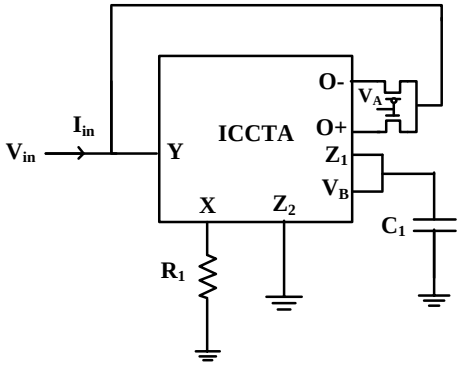


Fig. 6.1 Proposed flux controlled grounded memristor emulator.

Now, current passes across the X terminal of the flux controlled grounded memristor may be written as:

$$I_X = \frac{V_{in}}{R_1} \tag{6.1}$$

Voltage at Z_1 terminal of grounded memristor may be obtained as:

$$V_{z1} = -\frac{1}{C_1}\int \frac{V_{in}}{R_1}\,dt = -\frac{\varphi_{in}}{R_1 C_1} \tag{6.2}$$

Where φ_{in} is known as input flux. Now, input current of grounded memristor for incremental and decremental modes can be derived using port relations of ICCTA as:

$$I_{in} = \mu_n C_{ox}\frac{W}{\sqrt{2}L}\left(\pm\frac{\varphi_{in}}{R_1 C_1} \pm V_{SS} \pm V_{th}\right)V_{in} \tag{6.3}$$

Therefore, memconductance of the proposed grounded memristor may be written as:

$$W(\varphi(t)) = \frac{I_{in}(t)}{V_{in}(t)} = \mu_n C_{ox}\frac{W}{\sqrt{2}L}\left(\pm\frac{\varphi_{in}}{R_1 C_1} \pm V_{SS} \pm V_{th}\right) \tag{6.4}$$

It can be analyzed from eq. (6.4) that memconductance of grounded memristor has one variable term and one fixed term. Fixed term may be controlled by negative dc supply voltage, whereas variable term may be controlled by input flux.

6.1.1.1 Non-ideal analysis

Considering the nonidealities of ICCTA given in chapter 2, the flux controlled memristor emulator of Fig. 6.1 modifies to Fig. 6.2.

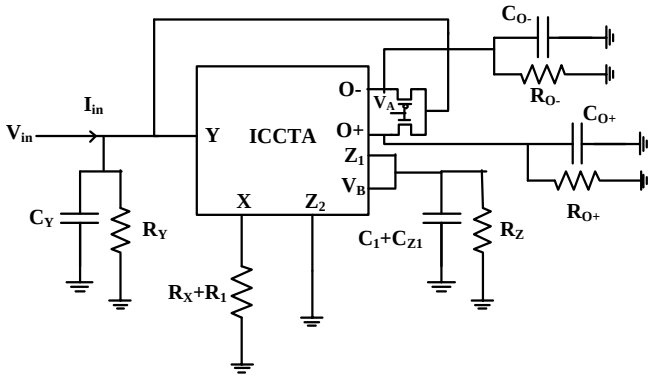


Fig. 6.2 Proposed grounded memristor emulator with parasitic components.

Current passes through the X terminal of the proposed grounded memristor emulator may be written as:

$$I_X = \frac{V_{in}}{(R_1+R_x)} \tag{6.5}$$

Since capacitance at Z_1 terminal of grounded memristor emulator as depicted in Fig. 6.2 is (C_1+C_{Z1}). Therefore, voltage at Z_1 terminal of the grounded emulator can be expressed as:

$$V_{z1} = -\frac{1}{(C_z+C_1)}\int \frac{V_{in}}{(R_1+R_x)}\,dt = -\frac{\varphi_{in}}{(R_1+R_x)(C_{z1}+C_1)} \tag{6.6}$$

Now, input current of the grounded memristor emulator for incremental and decremental modes can be expressed using port relations of ICCTA as:

$$I_{in}(t) = \frac{[\{(R_Y||R_{O\pm})s(C_{O\pm}+C_Y)\}+1]}{(R_Y||R_{O\pm})} V_{in}(t) + \mu_n C_{ox} \frac{W}{\sqrt{2}L} \left(\pm \frac{\varphi_{in}}{(R_1+R_x)(C_{z1}+C_1)} \pm V_{SS} \pm V_{th} \right) V_{in}(t) \tag{6.7}$$

Therefore, memconductance of grounded memristor emulator with parasitic components may be written as:

$$W(\varphi(t)) = \frac{I_{in}(t)}{V_{in}(t)} = \frac{[\{(R_Y||R_{O\pm})s(C_{O\pm}+C_Y)\}+1]}{(R_Y||R_{O\pm})} + \mu_n C_{ox} \frac{W}{\sqrt{2}L} \left(\pm \frac{\varphi_{in}}{(R_1+R_x)(C_{z1}+C_1)} \pm V_{SS} \pm V_{th} \right) \tag{6.8}$$

Equation (6.8) demonstrates how the parasitic components of ICCTA may affect the memconductance of the grounded memristor. By choosing the passive components $R_1 \gg R_{X1}$, and $C_1 \gg C_{Z1}$, one can lessen the impact of these parasitic components on the performance of the designed memristor.

Now, frequency analysis of the proposed memristor may be studied by connecting AC voltage source $V_{in} = V_m \sin(\omega_m t)$ at input terminal of the grounded memristor. Where, ω_m and V_m are known as angular frequency and amplitude of input signal respectively. Now, flux $\varphi(t)$ associated with the proposed grounded memristor emulator may be derived as:

$$\varphi(t) = \int V_{in}\, dt = \frac{V_m \cos(\omega t - \pi)}{\omega} \tag{6.9}$$

Substitute the value of $\varphi(t)$ from eq. (6.9) into eq. (6.8). Expression for memconductance of grounded memristor may be expressed as:

$$W(\varphi(t)) = \frac{I_{in}(t)}{V_{in}(t)} = \frac{[\{(R_Y||R_{O\pm})s(C_{O\pm}+C_Y)\}+1]}{(R_Y||R_{O\pm})} \pm \frac{k}{\sqrt{2}} \left(\frac{V_m \cos(\omega t - \pi)}{\omega\{(R_1+R_x)(C_{z1}+C_1)\}} + V_{SS} + V_{th} \right) \tag{6.10}$$

where $k = \mu_n C_{ox} \frac{W}{L}$. Here, μ_n, C_{ox} and $\frac{W}{L}$ having their usual meaning. Equation (6.10) shows that the expression of memconductance is a combination of time variant and time invariant terms. As a result, the relationship between both terms may be expressed by the amplitude ratio as:

$$\alpha = \frac{V_m}{2\pi f\{(R_1+R_x)(C_{z1}+C_1)\}\left\{\sqrt{2}\left(\frac{[\{(R_Y||R_{O\pm})s(C_{O\pm}+C_Y)\}+1]}{k(R_Y||R_{O\pm})}\right) \pm (V_{SS}+V_{th})\right\}} = \frac{1}{\tau f} \tag{6.11}$$

From eq. (6.11), it can be observed that α relies on the input frequency and time constant of the suggested grounded memristor emulator. The grounded emulator's time constant is now represented as:

$$\tau = \frac{2\pi\{(R_1+R_x)(C_{z1}+C_1)\}\left\{\sqrt{2}\left(\frac{[\{(R_Y||R_{O\pm})s(C_{O\pm}+C_Y)\}+1]}{k(R_Y||R_{O\pm})}\right) \pm (V_{SS}+V_{th})\right\}}{V_m} \tag{6.12}$$

It is seen from eq. (6.11) and eq. (6.12) that the value of α and τ may be deviated from the ideal one due to parasitic components associated with ICCTA.

6.1.1.2 Results and discussion

Theoretical analysis of the grounded memristor emulator is validated by PSPICE simulation using 180 nm TSMC technology. Supply voltage and bias voltage (V_{BB}) of ICCTA are ±1.25 V and 0.42 V respectively. The aspect ratio of MOS transistors of ICCTA is mentioned in Table 2.3 in chapter 2**.** The layout of ICCTA is shown in Fig. 6.3. It occupies 401.41 μm^2 chip area.

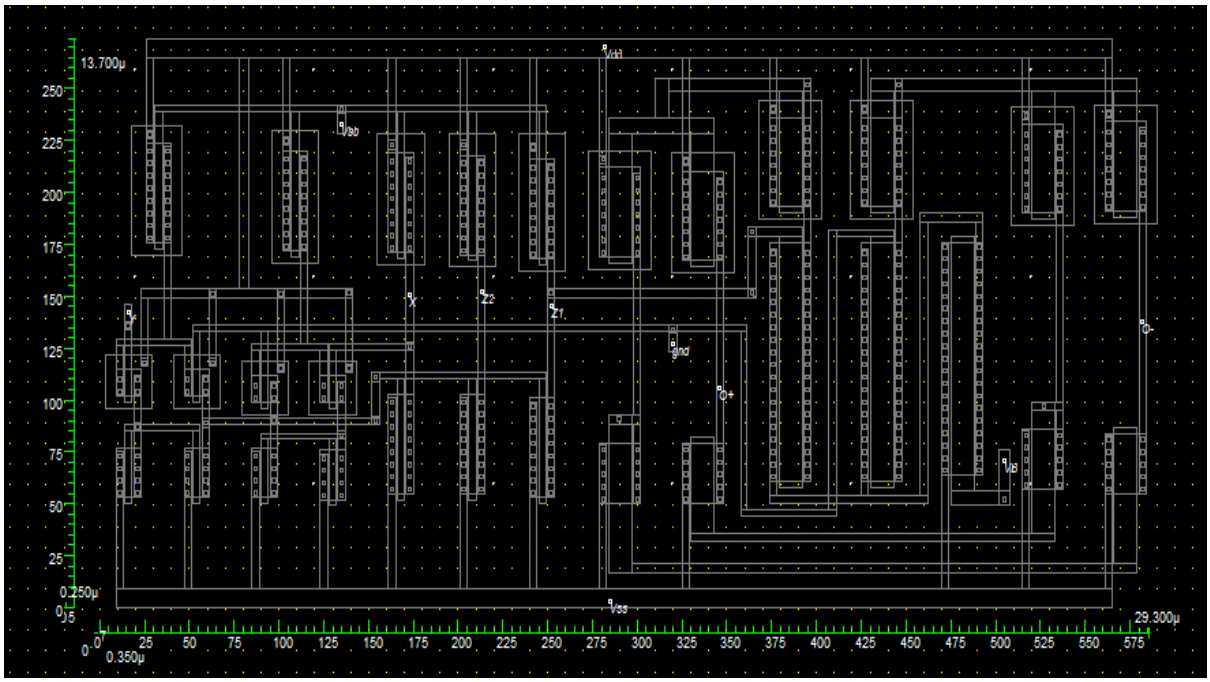
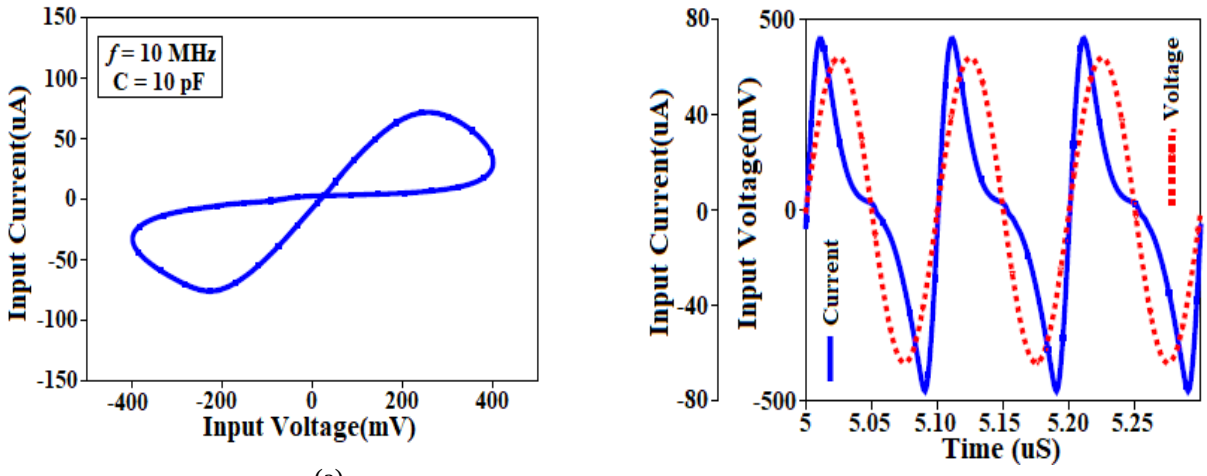


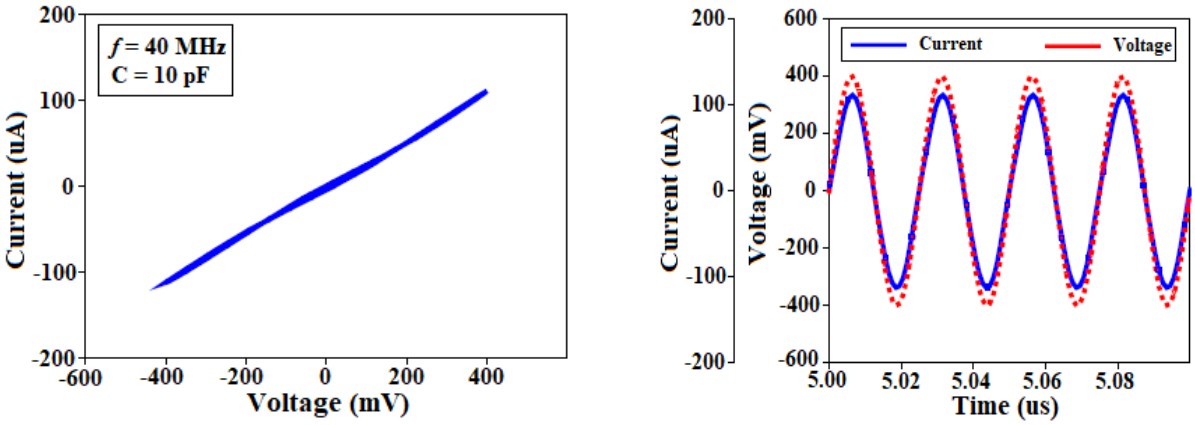
Fig. 6.3 Layout of ICCTA.

Pinch hysteresis curve and time domain response of the grounded memristor at 10 MHz frequency is illustrated in Fig. 6.4. It shows the 1st fingerprint [199] of the proposed memristor emulator. To demonstrate the pinch hysteresis curve at 10 MHz frequency, the value of resistance and capacitance is chosen as R_1=3 kΩ and C_1=10 pF respectively. Figures 6.5(a) and 6.5(b) display PHL and time domain response of the memristor emulator respectively at 40 MHz frequency, while keeping input voltage and value of passive components constant. Figure 6.5 shows that memristance is changed into linear resistor at 40 MHz frequency due to decrement of time varying part of eq. (6.8), which ensures the 2nd and 3rd fingerprints [199] of the proposed memristor.



(a) (b)

Fig. 6.4 Responses of grounded memristor at f=10 MHz. (a) PHL, and (b) time domain response.



(a) (b)

Fig. 6.5 Responses of the grounded memristor at f=40 MHz. (a) PHL, and (b) time domain response.

Moreover, Fig. 6.6 shows pinch hysteresis curve of grounded memristor emulator at different capacitance value of 5 pF, 10 pF, and 15 pF while keeping frequency f=10 MHz and amplitude of input signal Vin=0.4 V constant. Figure 6.6 shows that the lobe area of pinch hysteresis curve is decreased as value of capacitance is increased. Bias voltage of ICCTA may affect the performance of the proposed memristor emulators. Therefore, PHL of the proposed grounded memristor for various bias voltage is illustrated in Fig. 6.7 respectively. It displays that the area of PHL of the designed memristors is increased as the value of the bias voltage of ICCTA is increased.

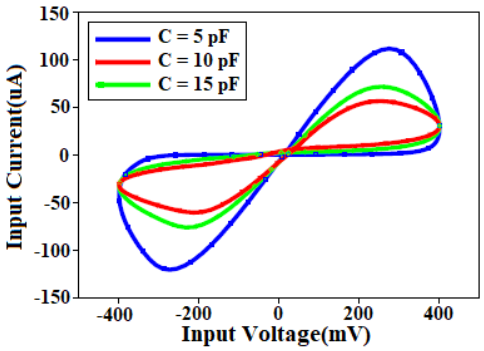


Fig. 6.6 PHL of grounded memristor for different capacitance values.

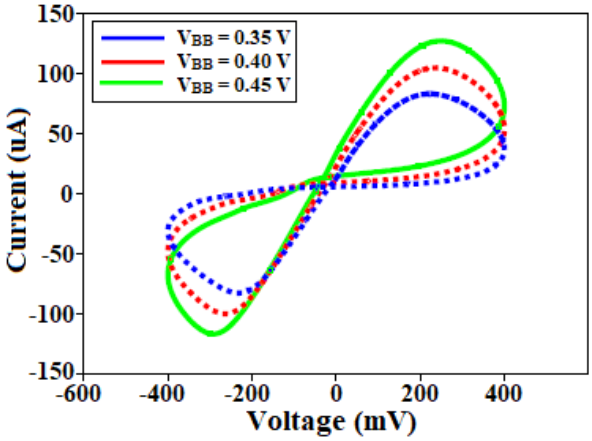
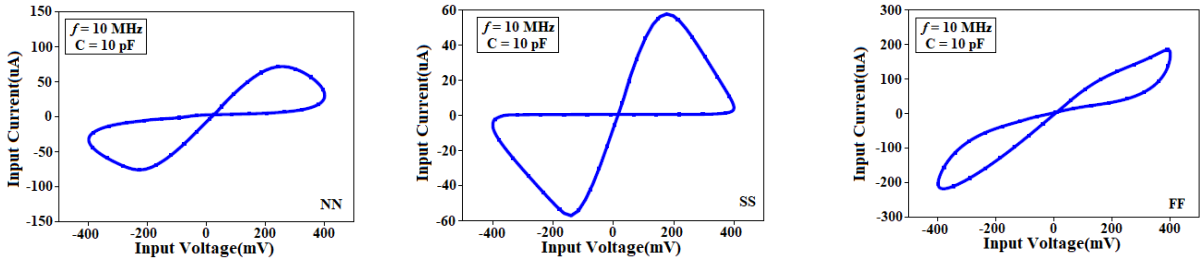


Fig. 6.7 PHL of grounded memristor for different bias voltages.

Further, Fig. 6.8 displays the corner analysis of the V-I curve of the proposed grounded memristor emulator. This response is obtained by selecting the passive components as R_1=3kΩ, and C_1=10 pF, while keeping input voltage and input frequency at 400 mV and 10 MHz respectively. It is noticed from Fig. 6.8 that current flows in SS mode is lower than current flows in FF mode.



(a) (b) (c)

Fig. 6.8 Corner analysis of the grounded memristor. (a) NN, (b) SS, and (C) FF.

Moreover, the grounded memristor emulator may be operated at high frequency by reducing the value of capacitance. V-I characteristic of grounded memristor at 125 MHz input frequency with 400 mV input voltage is illustrated in Fig. 6.9. This response is obtained by selecting the passive

component value as R_1=2 kΩ and C_1=0.5 pF. It is seen from Fig. 6.9 that pinch hysteresis loop slightly deviates from origin because of parasitic components associated with the terminals of ICCTA.

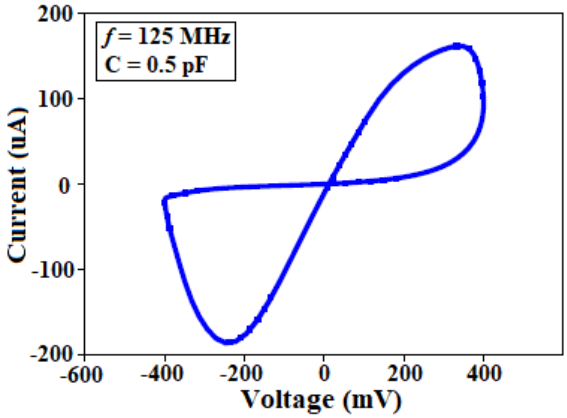


Fig. 6.9 PHL of grounded memristor for 125 MHz frequency.

6.1.1.3 Applications

To demonstrate the viability of the flux controlled grounded memristor, a first order high pass filter may be employed. The first order RC high pass filter is displayed in Fig. 6.10(a). Whereas, incremental and decremental memristor based first order high pass filter is shown in Fig. 6.18(b) and 6.18(c) respectively. The depicted diagram illustrates the substitution of a resistor with a proposed grounded memristor in an RC high pass filter. Equations (6.13) and (6.14) can be used to express the cut off frequency of a memristor-based high pass filter and an RC-based high pass filter circuit, respectively.

$$f = \frac{1}{2\pi C\{R_{AVG} \pm \Delta R_m \sin(2\pi f_m t + \varphi)\}} \tag{6.13}$$

$$f = \frac{1}{2\pi CR} \tag{6.14}$$

Where, R_{AVG} and ΔR_m is known as average value of memristance and variation of memristance due to applied sinusoidal signal respectively. Resistance and capacitance value of RC high pass filter are 2 kΩ, and 1 pF respectively. Components selection for high pass filter using memristor are R_1=3 kΩ, C_1=100 pF and C=1 pF. Magnitude response of voltage gain of RC high pass filter and high pass filter using memristor are illustrated in Fig. 6.11. It is observed from Fig. 6.11, cut off frequency of incremental memristor based high pass filter, RC based high pass filter and decremental memristor based high pass filter are 33.79 MHz, 79.58 MHz, and 165.92 MHz respectively.

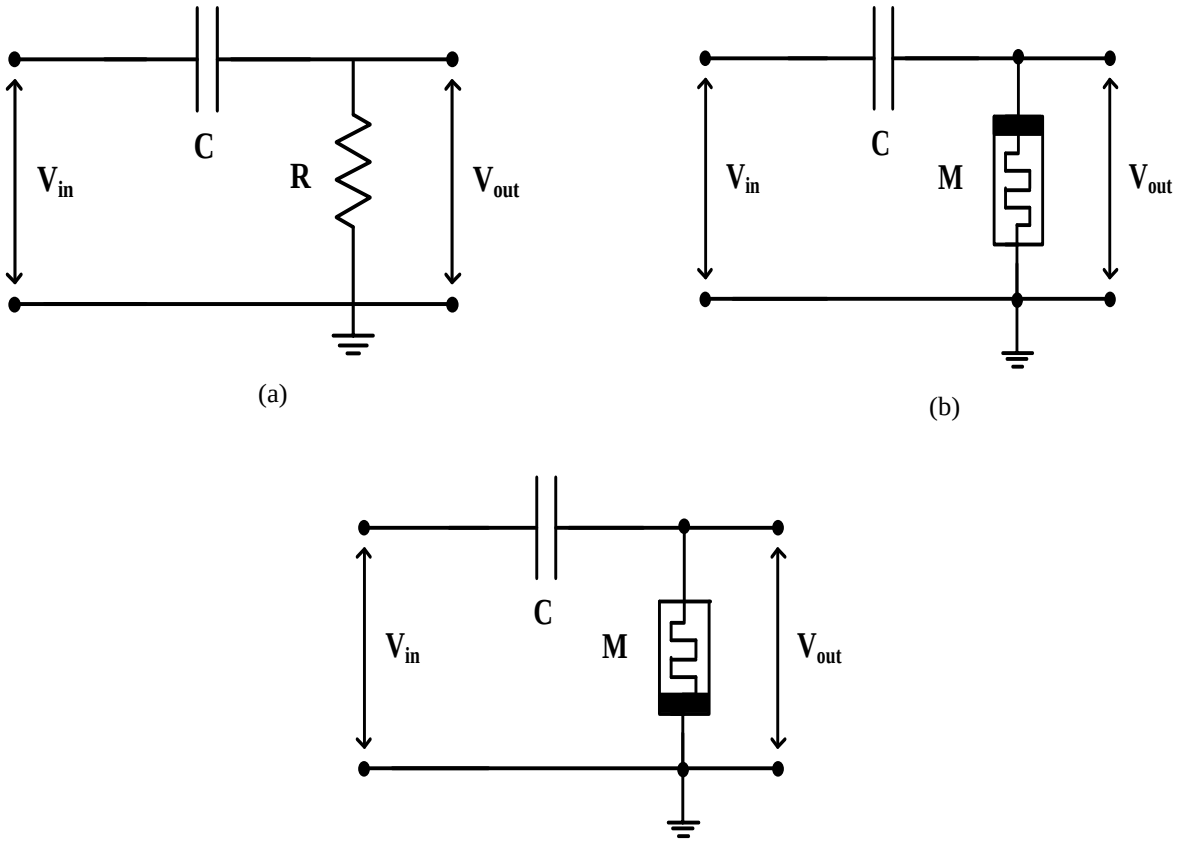


Fig. 6.10 High pass filter based on (a) RC(b) +MC, and (c) -MC.

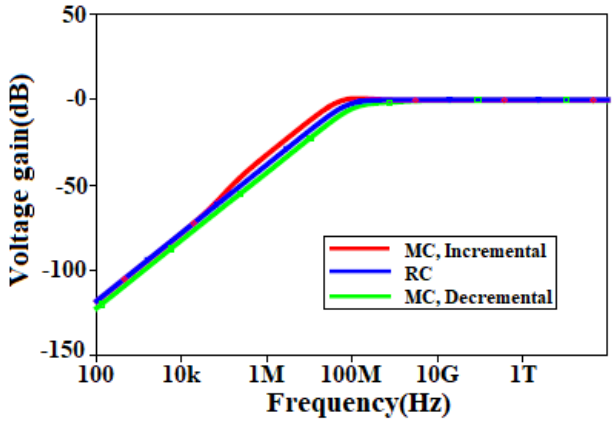


Fig. 6.11. Frequency response of RC and MC high pass filter circuit.

6.2 Charge controlled memristor emulator

This section discusses ICCTA based charge controlled memristor emulator.

6.2.1 Proposed charge controlled memristor

The proposed floating memristor emulator circuit is mentioned in Fig. 6.12. It employs a single ICCTA as ABB, and one capacitor and three resistors as passive elements. There are two MOS

switches (NMOS and PMOS) connected between the O± and Y terminal of ICCTA. MOS switches with high and low gate voltages (V_A) can operate the proposed circuit in incremental and decremental modes, respectively.

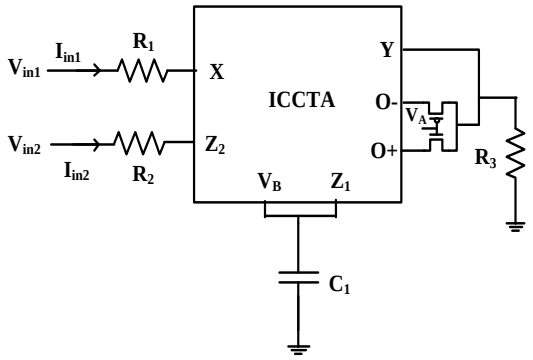


Fig. 6.12 Proposed charge controlled memristor emulator.

Apply KVL at X terminal and Z_2 terminal of the proposed floating memristor emulator. We get following expression of V_{in1} and V_{in2} as:

$$V_{in1} = I_{in1}R_1 - V_Y; V_{in2} = I_{in2}R_2 + V_{Z2} \tag{6.15}$$

Voltage across resistor R_3 of the designed circuit for incremental and decremental modes may be derived using expression of $g_m = 2\mu_n C_{OX}\left(\frac{W}{L}\right)(V_B + V_{ss} - V_T)$ as:

$$V_Y = \pm 2k(V_B + V_{ss} - V_T)V_{Z2}R_3 \tag{6.16}$$

Substitute $V_{Z2} = V_{in2} - I_{in2}R_2$ in equation (6.16), we get following voltage at Y terminal of the floating memristor.

$$V_Y = \pm 2k(V_B + V_{ss} - V_T)(V_{in2} - I_{in2}R_2)R_3 \tag{6.17}$$

Substitution of equation (6.17) into eq. (6.15), we may be obtained following expression of V_{in1} as:

$$V_{in1} = I_{in1}R_1 \mp 2k(V_B + V_{ss} - V_T)(V_{in2} - I_{in2}R_2)R_3 \tag{6.18}$$

Substitute $V_{in1} = \frac{V_{in}(t)}{2}$, $V_{in2} = -\frac{V_{in}(t)}{2}$, $V_B = \frac{q_C(t)}{C_1}$ and $I_{in1} = I_{in2} = I_{in}(t)$ (from port relation) in eq. (6.18), the memristance of the floating memrsitor may be expressed as:

$$M(q_C(t)) = \frac{V_{in}(t)}{I_{in}(t)} = \frac{2R_1 \pm 4k\left(\frac{q_C(t)}{C_1} + V_{ss} - V_T\right)R_3R_2}{1 \mp 2k\left(\frac{q_C(t)}{C_1} + V_{ss} - V_T\right)R_3} \tag{6.19}$$

Select the component value R_3 such that $2k\left(\frac{q_C(t)}{C_1} + V_{ss} - V_T\right)R_3 \ll 1$, then the memristance may be rewritten as:

$$M(q_C(t)) = \frac{V_{in}(t)}{I_{in}(t)} = 2R_1 \pm 4k\left(\frac{q_C(t)}{C_1} + V_{ss} - V_T\right)R_3R_2 \tag{6.20}$$

As one can notice from eq. (6.20) that memristance of floating memristor is composed of time variant resistor and time invariant resistor. Time variant resistor is controlled by charge associate with capacitor C_1, whereas time invariant resistor is controlled by negative supply voltage (V_{ss}) of ICCTA.

6.2.1.1 Non-ideal analysis

Considering the nonidealities of ICCTA given in chapter 2, the charge controlled memristor emulator of Fig. 6.12 modifies to Fig. 6.13.

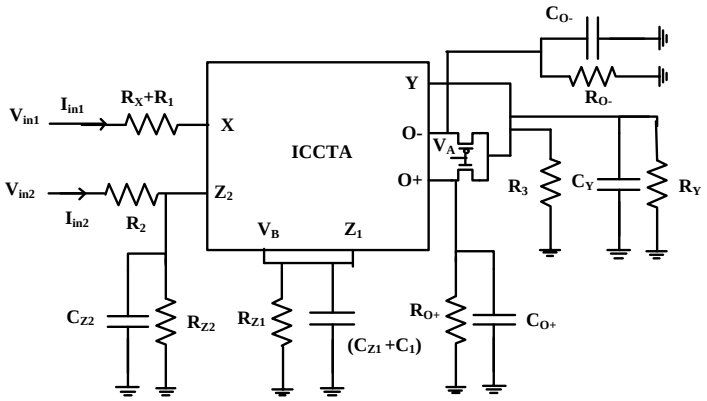


Fig. 6.13 Proposed charge controlled memristor emulator with parasitic components.

Current at X terminal and Z_2 terminal of the proposed floating charge controlled memristor emulator with parasitic components may be written as:

$$I_{in1} = \frac{V_{in1}+V_Y}{(R_1+R_X)};\ I_{in2} = \frac{V_{in2}-V_{Z2}}{R_2} \tag{6.21}$$

Using port relation of ICCTA, voltage at Y terminal for incremental and decremental configurations may be calculated as:

$$V_Y = \pm 2k\frac{R_\theta}{(sR_\theta C_\theta+1)}\left(\frac{q(t)}{C_\delta} + V_{ss} - V_T\right)\left\{V_{in2} - \left(I_{z2} - \frac{V_{Z2}}{Z}\right)R_2\right\} \tag{6.22}$$

where, $C_\theta = C_Y \parallel C_{O\pm}$, $R_\theta = R_Y \parallel R_{O\pm}$, $Z = R_{Z2} \parallel \frac{1}{SC_{Z2}}$ and $C_\delta = C_1 \parallel C_{Z1}$. Now, substitute the eq. (6.22) into eq. (6.21), we get following expression of V_{in1} as:

$$V_{in1} = I_{in1}(R_1 + R_X) \mp 2k\frac{(R_\theta \parallel R_3)}{\{s(R_\theta \parallel R_3)C_\theta+1\}}\left(\frac{q(t)}{C_\delta} + V_{ss} - V_T\right)\left\{V_{in2} - \left(I_{z2} - \frac{V_{Z2}}{Z}\right)R_2\right\} \tag{6.23}$$

Since $V_{in1} = \frac{V_{in}(t)}{2}$, $V_{in2} = -\frac{V_{in}(t)}{2}$, and $I_{in1} = I_{z2} = I_{in}(t)$ (from port relation), therefore memristance of the proposed floating charge controlled memristor emulator with parasitic components may be written as:

$$M(q_C(t)) = \frac{V_{in}(t)}{I_{in}(t)} = R_M = \frac{2R_1+2R_X \pm 4k\frac{(R_\theta \| R_3)}{\{s(R_\theta \| R_3)C_\theta+1\}}\left(\frac{q(t)}{C_\delta}+V_{ss}-V_T\right)R_2}{1\mp 2k\frac{(R_\theta \| R_3)}{\{s(R_\theta \| R_3)C_\theta+1\}}\left(\frac{q(t)}{C_\delta}+V_{ss}-V_T\right)} \quad (6.24)$$

Now, memristance of the proposed floating memristor may be obtained by considering $2k\frac{(R_\theta \| R_3)}{\{s(R_\theta \| R_3)C_\theta+1\}}\left(\frac{q(t)}{C_\delta}+V_{ss}-V_T\right) \ll 1$as:

$$M(q_C(t)) = \frac{V_{in}(t)}{I_{in}(t)} = R_M = 2R_1 + 2R_X \pm 4k\frac{(R_\theta \| R_3)}{\{s(R_\theta \| R_3)C_\theta+1\}}\left(\frac{q(t)}{C_\delta}+V_{ss}-V_T\right)R_2 \quad (6.25)$$

It is seen from eq. (6.25) that memristance of floating memristor may be affected due to parasitic components of ICCTA. Effect of these parasitic components on the performance of the emulator may be reduced by selecting the passive components as $R_1 \gg R_X$, $R_3 \ll (R_Y \parallel R_{O\pm})$, and $C_1 \gg C_{Z1}$. Frequency behavior of the proposed memristor may be studied by connecting AC voltage source $V_{in} = V_m \sin(\omega_m t)$ at input terminal of the proposed circuit. Where, ω_m and V_m are known as angular frequency and amplitude of input signal respectively. Now, charge across the capacitor of the proposed floating emulator can be expressed as:

$$q_C(t) = \frac{1}{R_{DC}}\int V_{in}dt = \frac{V_m \cos(\omega t-\pi)}{\omega\{R_1 \pm 2k(V_{ss}-V_T)R_3R_2\}} \quad (6.26)$$

Substitute the above value of $q_C(t)$ in equation (6.25). We get memristance of the memristor as:

$$M(q_C(t)) = \frac{V_{in}(t)}{I_{in}(t)} = R_M = 2R_1 + 2R_X \pm 4k\frac{(R_\theta \| R_3)}{\{s(R_\theta \| R_3)C_\theta+1\}}\left(\frac{V_m \cos(\omega t-\pi)}{\omega C_\delta\{2R_1 \pm 4k(V_{ss}-V_T)R_{2R_3}\}}+V_{ss}-V_T\right)R_2 \quad (6.27)$$

It is seen from eq. (6.27) that expression of memristance is combination of time variant and time invariant terms. Hence, relationship between both terms may be expressed by the ratio of amplitude as:

$$\alpha = \frac{2kR_2(R_\theta \| R_3)V_m}{\pi f C_\delta\{2R_1 \pm 4k(V_{ss}-V_T)R_{2R_3}\}[\{(2R_1+2R_X)\{s(R_\theta \| R_3)C_\theta+1\}\} \pm 4kR_2(R_\theta \| R_3)(V_{ss}-V_T)]} = \frac{1}{\tau f} \quad (6.28)$$

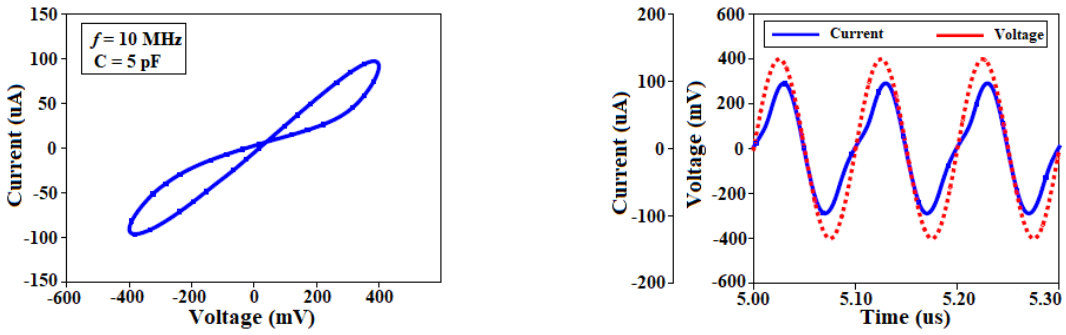
It is observed from eq. (6.28) that α depends upon input frequency and time constant of the grounded circuit. Now, time constant of the memristor emulator can be expressed as:

$$\tau = \frac{\pi f C_\delta\{2R_1 \pm 4k(V_{ss}-V_T)R_{2R_3}\}[(2R_1+2R_X)\{s(R_\theta \| R_3)C_\theta+1\} \pm 4kR_2(R_\theta \| R_3)(V_{ss}-V_T)]}{2kR_2(R_\theta \| R_3)V_m} \quad (6.29)$$

6.2.1.2 Results and discussion

A substantial investigation of ICCTA based charge controlled memristor emulator is done by SPICE simulator using 0.18 μm technology. Bias voltage (V_{BB}) and DC supply voltage of ICCTA are 0.41 V and ±1.2 V respectively. The aspect ratio of MOS transistors of ICCTA is mentioned in chapter 2 (Table 2.3). Pinch Hysteresis Loop (PHL) and its time domain response of charge controlled floating emulator for 10 MHz input frequency are displayed in Fig. 6.14(a)

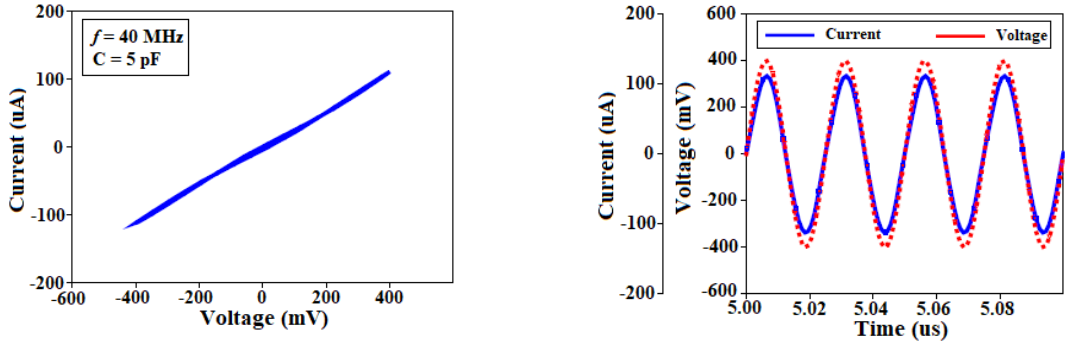
and Fig. 6.14(b) respectively. These responses are obtained by selecting the value of passive components as R_1=R_2=3 kΩ, R_3=300 Ω, C_1=5 pF.



(a) (b)

Fig. 6.14 Responses of the memristor at f=10 MHz. (a) PHL, and (b) time domain response.

Figure 6.14 shows the 1st fingerprint [199] of the proposed memristor emulator. Figures 6.15(a) and 6.15(b) display PHL and time domain response of the memristor emulator respectively at 40 MHz frequency, while keeping input voltage and value of passive components constant. Figure 6.15 shows that memristance is changed into linear resistance at 40 MHz frequency due to decrement of time varying part of eq. (6.27), which ensures the 2nd and 3rd fingerprints [199] of the proposed memristor. It is noticed from Figs. 6.14 to 6.15 that time domain response of the proposed floating and grounded memristor show 0° phase shift between input current and input voltage.



(a) (b)

Fig. 6.15 Responses of the memristor at f=40 MHz. (a) PHL, and (b) time domain response.

In addition, Fig. 6.16 illustrates PHL of the proposed memristor at various capacitance values of 4 pF, 5 pF, and 6 pF while keeping input voltage, input frequency and value of passive components constant. Figure 6.17 displays that the lobe area of PHL decreases as value of capacitance increases. In addition, PHL of the proposed floating memristor for various bias

voltage is displayed in Fig. 6.17. It displays that the area of PHL of the designed memristors is increased as the value of the bias voltage of ICCTA is increased.

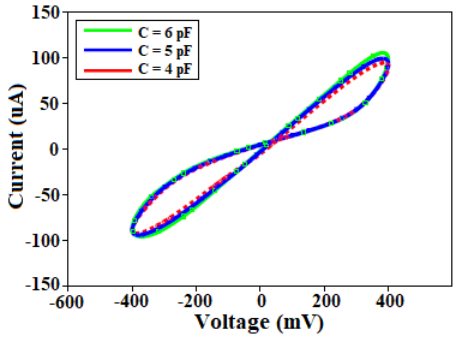


Fig. 6.16 PHL of the memristor for different capacitance values.

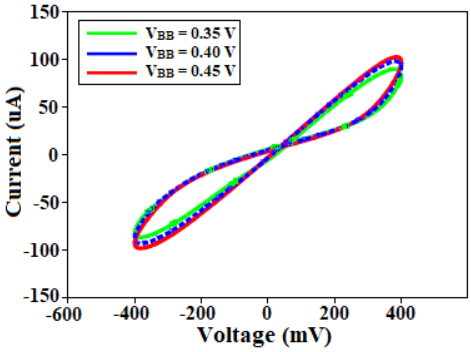
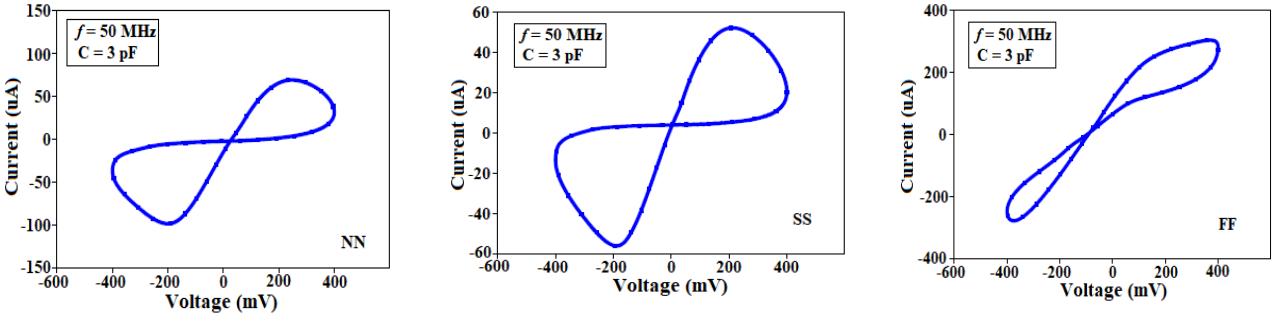


Fig. 6.17 PHL for different bias voltages of the memristor.

Moreover, Fig. 6.18 displays the corner analysis of the PHL of the floating memristor, which is the essential fingerprint of the memristor, at various process corners. This response is obtained by selecting the passive components as R_1=2 kΩ, and C_1=3 pF, while keeping input voltage and input frequency at 400 mV and 50 MHz respectively. It is noticed from Fig. 6.18 that current flows in SS mode is lower than current flows in FF mode.



(a) (b) (c)

Fig. 6.18 Corner analysis of the memristor. (a) NN, (b) SS, and (C) FF.

In addition to the PHL, the non-volatile nature of memristance is another key fingerprint of the memristor emulator. It shows that the memristor may store the final value of memristance for a

longer period without an input signal after it is programmed. Figure 6.19 shows the non-volatile nature of memristance of the floating memristor. It is obtained by providing a pulse signal with amplitude of 600 mV, having a pulse width of 2 ns, and time period of 5 ns has been applied at the input of the floating memristor. A small amount of variation of memristance is observed in ON period of pulse due to non-idealities associated with ICCTA.

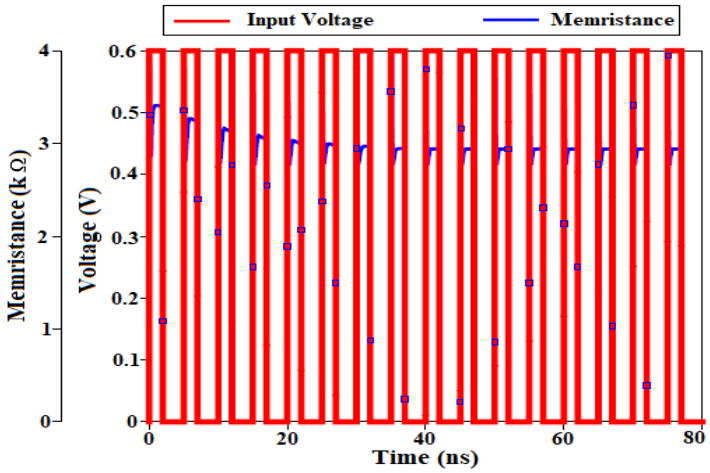


Fig. 6.19 Nonvolatile nature of the memristor.

Further, the proposed memristor emulators can be operated at high frequency by reducing the value of capacitance. The PHL of floating memristor at 100 MHz input frequency with 400 mV input voltage is shown in Fig. 6.20. The value of passive components is selected as R_1=R_2=3 kΩ, R_3=200 Ω, and C_1=0.5 pF to operate at 100 MHz frequency. It is seen from Fig. 6.20 that pinch hysteresis loop slightly deviates from origin because of parasitic components associated with the terminals of ICCTA.

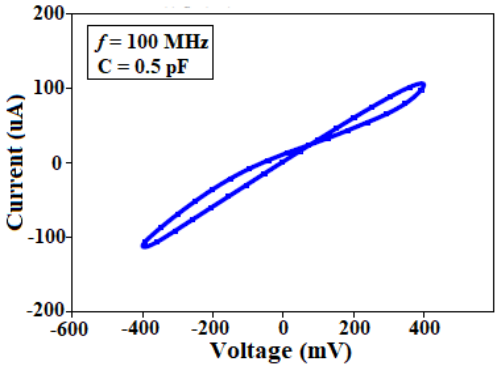


Fig. 6.20 PHL of the proposed memristor for 100 MHz frequency.

6.2.1.3 Application

A meminductor [200,201,202,203,204] emulator may be designed using the proposed charge controlled floating memristor emulator and ICCTA. The developed floating memristor can be

used as grounded memristor by making V_{in2} = 0 V. The meminductor circuit using the designed memristor is illustrated in Fig. 6.21. It consists of one ICCTA, one capacitor, one charge controlled grounded memristor emulator and two MOS switches.

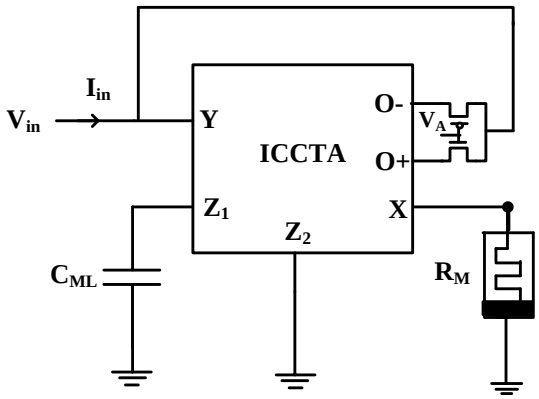


Fig. 6.21 Proposed meminductor circuit using charge controlled memristor.

The meminductor element belongs to the memristor family, provides the relation between flux $(\varphi(t))$ and input current $(I_{in}(t))$, may be expressed as:

$$\frac{\varphi(t)}{I_{in}(t)} = L_M \tag{6.30}$$

where, L_M is known as meminductance of meminductor emulator. Using routine analysis of ICCTA, input current of the proposed meminductor may be written as:

$$I_{in} = \pm g_m V_{z1} \tag{6.31}$$

Voltage at Z_1 terminal of the designed meminductor emulator may be expressed as:

$$V_{Z1} = \frac{1}{C_{ML}} \int \frac{V_{in}(t)}{R_M} dt = \frac{\varphi(t)}{R_M C_{ML}} \tag{6.32}$$

Now, substitute the eq. (6.32) into eq. (6.31), we get following expression of I_{in} as:

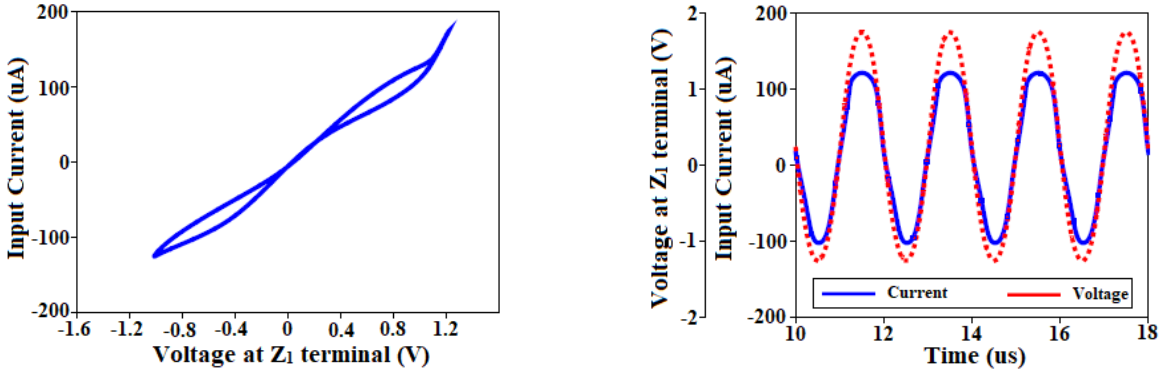
$$I_{in} = \pm g_m \frac{\varphi(t)}{R_M C_{ML}} \tag{6.33}$$

Thus, the meminductance of the proposed meminductor circuit may be obtained as:

$$L_M = \frac{\varphi(t)}{I_{in}(t)} = \pm \frac{R_M C_{ML}}{g_m} \tag{6.34}$$

It is seen from eq. (6.34) that meminductance of the proposed meminductor depends upon memristance (R_M) of memristor, capacitor (C_{ML}), and transconductance (g_m) of ICCTA. Equation (6.34) also shows positive and negative sign; denote positive and negative meminductance value. Positive and negative meminductance of meminductor may be obtained by providing gate voltage of MOS switch (V_A) high and low respectively. The PHL and time domain response of the designed meminductor are obtained between voltage at Z_1 terminal of

ICCTA and input current. The PHL and time domain response of the meminductor for f_{in}=0.5 MHz are depicted in Fig. 6.22(a) and Fig. 6.22(b) respectively. These responses are obtained by selecting the value of components as C_{ML}=1.2 pF, R_1=R_2=3 kΩ, R_3=900 Ω, C_1=4 pF. It is important to mention that flux is not directly measurable electrical quantity [202]. It is observed from port relation of ICCTA that current at Z_1 terminal of ICCTA is directly proportional to input voltage ($I_{Z1} = I_X = \frac{V_{in}(t)}{R_M}$). Hence, voltage across the capacitor (C_{ML}) connected at Z_1 terminal will be proportional to integral of the input voltage known as flux $\varphi(t)$. Hence, the PHL for the proposed meminductor is obtained between voltage at Z_1 terminal of ICCTA and input current ($I_{in}(t)$) instead of $\varphi(t)$ and $I_{in}(t)$.



(a) (b)

Fig. 6.22 Response of meminductor circuit. (a) PHL, and (b) time domain response.

6.3 Comparison

Comparison of performance of ABB-based proposed memristor emulator with existing memristor emulator on the basis of no. of active blocks, no. of passive components, technology node, Layout area, mode of operation, and maximum operating frequency are mentioned in Table 6.1. There are following conclusion may be drawn from Table 6.1 as:

a. The proposed memristor emulator used less no. of active and passive components (except [188]).
b. The designed memristor emulator does not include diodes, inductor, LDR, and multiplier circuits (contrary to [179,180,181,183,184,185,187]).
c. The presented memristor emulators are implemented in incremental and decremental configurations (opposite to [179,180,181,182,184,185,186]).
d. The memristor emulator discussed in [179,180,186,187,190,191,194,196] operates in grounded mode. However, proposed memristors operate in grounded and floating modes.

e. The maximum operating frequency achieved in [179,180,181,182,183,184,185,186,187,188,190,191,194,196] are low. In distinction, maximum operating frequency of the proposed ICCTA based charge and flux controlled memristor is 100 MHz and 120 MHz respectively.

Table 6.1 Comparison of the proposed memristor emulator with existing memristor emulator.

Ref.	No. of Active Block	Passive Elements R and C	All Passive elements are grounded	Parameter (nm)	Floating/ Grounded	Incremental/ Decremental	Flux/ Charge Control	Max. Operating Freq.
[179]	VIM-1, Diode-1, Inductor-1	2 and 1	YES	180	Grounded	Decremental	Flux	10 Hz
[180]	Op-amp-3, LDR-1, Diode-1	11 and 1	NO	-	Grounded	Decremental	Flux	280 Hz
[181]	CFOA-4, Diode-2	4 and 4	NO	-	Floating	Incremental	Charge	2.9 kHz
[182]	CCII-4, OTA-3	6 and 1	NO	-	Floating	Decremental	Flux	10 kHz
[183]	CCII-2, Multiplier-1	4 and 3	NO	-	Grounded	Both	Charge	160 kHz
[184]	CCII-4, Multiplier-1	5 and 1	NO	-	Floating	Incremental	Flux	20.2 kHz
[185]	DDCC-1 Multiplier-1	2 and 1	NO	250	Floating	Incremental	Charge	1 MHz
[185]	DDCC-1 Multiplier-1	2 and 1	NO	250	Floating	Decremental	Charge	1 MHz
[186]	CBTA-1 Multiplier-1	2 and1	NO	180	Grounded	Both	Charge	460 kHz
[187]	VDTA-2, Multiplier-1	2 and1	YES	45	Grounded	Incremental	Flux	53 kHz
[188]	OTA-2	0 and 1	YES	180	Floating	Both	Flux	400 kHz
[189]	VDTA-1	1 and 1	YES	180	Floating	Both	Flux	50 MHz
[190]	CCTA-1	3 and 1	NO	180	Grounded	Both	Charge	10 MHz
[191]	DVCCTA-1	3 and 1	NO	250	Grounded	Both	Charge	1 MHz
[194]	CDTA-1 OTA-1	0 and 1	YES	180	Grounded	Both	Flux	2 MHz
[196]	VDCC-1	2 and 1	YES	180	Grounded	Both	Flux	2 MHz
Proposed	ICCTA-1	3 and 1	NO	180	Floating	Both	Charge	100 MHz
Proposed	ICCTA-1	1 and 1	YES	180	Grounded	Both	Flux	125 MHz
NA- NOT AVAILABLE.								

6.4 Summary

In this chapter, charge and flux-controlled memristor emulator are developed. The flux-controlled floating memristor emulator is implemented using one ICCTA, one resistor, and one capacitor. Whereas charge controlled floating memristor emulator is composed of one ICCTA, one capacitor, and three resistors. Implementation of both proposed emulators does not include complex circuits like analog multiplier circuits, passive inductors, diodes, and ADC circuits. The maximum operating frequency of the proposed charge controlled floating memristor is 100 MHz.

Whereas the maximum operating frequency of flux controlled grounded memristor is 125 MHz. Moreover, the non-ideal analysis of the proposed circuits is also mathematically evaluated. Time domain responses and frequency domain responses of the proposed circuits follow the fingerprints of the memristor. Furthermore, an inspection of the corners has also been conducted to examine the viability and resilience of the designed circuits. Additionally, the meminductor circuit and memristor-based pass filter circuit, are implemented to examine the designed memristor emulators.

CHAPTER 7

CONCLUSIONS & FUTURE SCOPES

7.1 Conclusions

The immittance circuit are used in variety of applications in the field of microelectronics, communication, analog signal processing, instrumentation, and measurement. In integrated circuit design, the active immittance circuits are of prime importance as the inductor and resistances occupy larger chip space. Further, these circuits also add flexibility of tuning of immittance. This chapter provides a concise overview of the research conducted and reported in different chapters of the thesis.

Chapter 2 provides an overview of the active building blocks used to realize immittance emulators. The active blocks namely Operational Transconductance Amplifier (OTA), Current Conveyor Transconductance Amplifier (CCTA), Inverting Current Conveyor Transconductance Amplifier (ICCTA), and Current Feedback Operational Amplifier (CFOA) are described briefly. In reality, the port relations of the active blocks differ from the ideal ones. The discussion on the non-idealities related to OTA, CCTA, ICCTA, and CFOA are also briefly covered.

Chapter 3 presents new grounded and floating immittance emulator based on CCTA. By adjusting the switches, it is possible to achieve both positive and negative floating immittances. The proposed topology does not require any component matching, thus making it suitable for integration viewpoint. Further, the immittance may be tuned electronically via bias current of CCTA. Performance of proposed circuit is evaluated by pre-layout and post-layout simulation using 180 nm CMOS process technology. Power consumption of proposed immittance circuit is 1.35 mW. The proposed immittance circuit is used to implement fifth order low pass filter, and capacitance cancellation circuit. The simulated cutoff frequency and roll-off rate of fifth order low pass filter is observed to be 0.93 MHz and -100 dB/decade respectively. DC gain of the designed low pass filter is -3.5 dB. The power consumption of the low pass filter is 2.73 mW. The effect of parasitic components on operating range frequency of the proposed circuits is mathematically modelled. In addition, temperature sensitivity of designed circuit is also examined. Frequency response of proposed circuits at different temperatures show small effect of temperature. A Monte Carlo study is performed to analyze robustness of the proposal against variations 10% variations in the passive components. To illustrate the applicability of the proposal, voltage mode active filters are constructed.

Chapter 4 presents electronically adjustable floating and grounded fractional order inductor circuits. The suggested circuits utilize OTAs, one fractional order capacitor, one inverter, and

four MOS switches. These circuits can flip between positive and negative modes without modifying their architecture. Additionally, the suggested circuit's behavior is examined in the presence of parasitic components, which could potentially manifest in a real-world circuit. The operational evaluation is conducted using pre and post layout simulations, employing the 90 nm CMOS technology parameter. A close matching between pre and post layout results is observed in the frequency range of 1 Hz to 300 kHz. Power dissipation of the proposed fractional inductor circuit for bias current 40 μA and 100 μA are 0.86 mW and 1.44 mW respectively. Monte Carlo analysis shows the deviation in magnitude and phase response of proposed grounded fractional order inductor are $\pm$ 1.5 dB and $\pm 6°$ respectively. The efficacy of the suggested positive fractional inductor circuit is showcased by its application in a fractional order high pass filter and a fractional order band pass filter. The cut off frequency and roll-off rate of fractional high pass filter is 578 Hz and 72 dB/decade respectively. Output noise of fractional order high pass ladder filter is observed to be 16 $nV/\sqrt{Hz}$ at 9 kHz frequency. Power consumption of the designed high pass filter is 4.32 mW. The resonant frequency and quality factor of designed band pass filter are 80 Hz and 0.54 respectively. Power dissipation of the designed band-pass fractional filter is 0.288 mW. The effectiveness of the suggested negative fractional inductance circuit is showcased by means of a fractional inductance cancellation circuit. The input impedance of fractional inductance cancellation circuit is observed as 5 kΩ between 1mHz to 100 Hz input frequency.

Chapter 5 introduces a tunable Synthetic Transformer (ST) called Mutual Coupled Circuit (MCC), which is based on the CCTA. The circuit under consideration comprises of two CCTAs, three resistors, two capacitors, and four Metal-Oxide-Semiconductor (MOS) switches. By appropriately configuring the MOS switches, the circuit can be set up in four distinct pairs of mutually connected circuits. The proposed solution does not necessitate the condition of matching components. The bias current of CCTA can be used to adjust self-inductance, mutual inductance, and resonant frequency. Performance of proposed circuit is evaluated by pre-layout and post-layout simulation using 90 nm CMOS process technology. A double tuned band pass filter is shown as an application. The impact of supply voltage and temperature variation is examined and a maximum deviation of 3.326% and 16.8% respectively are observed in resonant frequency of DTBPF. The effect of component variations is also studied through Monte Carlo analysis. The output noise spectral density of DTBPF at resonant frequency is observed to be

102.489 **nV**/$\sqrt{\boldsymbol{Hz}}$ whereas the total harmonic distortion is observed within 1.3% for peak input voltage range 0.05V to 3.5 V. The power consumption of DTBPF circuit is 5.16 **mW** at 100 µA bias current of CCTA**.**

Chapter 6 introduces a charge and flux controlled memristor emulator built with an ICCTA. The flux-controlled floating memristor emulator is implemented using one ICCTA, one resistor, and one capacitor. Whereas charge controlled floating memristor emulator is composed of one ICCTA, one capacitor, and three resistors. Both proposed circuits do not include intricate components such as analog multiplier circuits, passive inductors, and analog to digital converter circuits in the design, which is beneficial in terms of circuit implementation. The functional verification is done using 180 nm technology parameter. The maximum operating frequency of the floating and grounded memristors is 100 MHz and 125 MHz respectively. Furthermore, the non-ideal explanation of the developed circuits is mathematically examined. Moreover, corner analysis of the proposed memristor is also included. The effectiveness of the developed circuits is validated using meminductor circuits, and memristor-based low pass filters.

7.2 Future scopes

This thesis makes noteworthy contributions by designing and implementing many immittance circuits employing Active building blocks. There are still other alternatives that remain open for additional study. Thus, the thesis also proposes potential future endeavors that can offer a more holistic exposure to analog designers.

a. The CMOS based ABBs are used in the current exploration. Alternatively, ABBs based on Fin field effect transistor (FINFET)/ Carbon Nano Tube field effect transistor (CNTFET) technology may be examined for performance enhancements of immittance emulators at lower technology nodes.
b. The bulk-driven MOS transistors (BD-MOST) may be used in ABBs for the applications requiring low power consumption.
c. The fractional order inductors are designed using fractional capacitor realized using RC tree. The ABB based fractional capacitor may be used to add extra tunability feature in the fractional order inductor design.
d. Unified MOS only topologies for realizing immittance emulators operating in both positive and negative modes may be looked into.

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LIST OF PUBLICATIONS & THEIR PROOFS

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I. Journal

1 N. Kumar, M. Kumar, and N. Pandey, “Unified Floating Immittance Emulator Based on CCTA,” in *Microelectronics Journal*, vol. 118, pp. 105289, 2021.

2 N. Kumar, M. Kumar, and N. Pandey, “Electronically tunable positive and negative fractional order inductor circuit using single topology,” in *Integration the VLSI Journal*, vol. 88, pp. 379-389, 2023.

3 N. Kumar, M. Kumar, and N. Pandey, “CCTA based four different pairs of mutually coupled circuit using single topology,” in *Integration the VLSI Journal*, vol. 91, pp. 43-53, 2023.

4 N. Kumar, M. Kumar, and N. Pandey, “A Programmable Tunable Active Grounded and Floating Immittance Circuit Using CCTA and Their Applications,” in *International Journal of Electronics*, vol. 110.1, pp.73-106, 2023.

5 N. Kumar, M. Kumar, and N. Pandey, “Grounded and Floating Memristor Emulator Employing ICCTA: Decremental or Incremental Operation,” in *International Journal of Electronics*. (Accepted on 22-04-2024).

II. Conference

1 N. Kumar, M. Kumar, and N. Pandey, "Single DXCCTA based Charge Controlled Floating Incremental/Decremental Memristor Emulator," in *2022 8th International Conference on Signal Processing and Communication (ICSC)*, Noida, India, 2022, pp. 663-668.

2 N. Kumar, M. Kumar, and N. Pandey, "A Grounded Flux Controlled Incremental/Decremental Memristor Emulator," in *2022 5th International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT)*, Aligarh, India, 2022, pp. 1-6.

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Unified floating immittance emulator based on CCTA

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ABSTRACT

In this paper, a unified floating immittace emulator based on Current Conveyor Transconductance Amplifier (CCTA) is put forward. It uses two CCTAs, two additional components (two MOS based resistors/one capacitor and one MOS based resistor) and four MOS switches. It can realize both positive and negative floating immittances through appropriate setting of switches. The proposed topology does not require any component matching, thus making it suitable for integration viewpoint. Further, the immittance may be tuned electronically via bias current of CCTA. Additionally, the operation in fractional domain also investigated. The impact of parasitics of CCTA on the performance of the proposed circuit is mathematically formulated. The functionality of the proposed circuit is verified through post layout simulations carried out using the netlist extraction from the layout and examined through SPICE simulations using 90 nm process parameter. The area of the layout of proposed unified immittance emulator is 67.80 μm × 22.80 μm. The proposed immittance circuit is used to implement notch filter, fifth order low pass filter, and capacitance cancellation circuit.

1. Introduction

The Current Conveyor Transconductance Amplifier (CCTA) is a hybrid active block which enjoys the versatility of current conveyor and adds electronic tunabilty to the application through bias current of inbuilt transconducatnce amplifier. These benefits have attracted researchers' attention in recent past as is evident from the availability of its applications in various analog signal processing applications e. g. memristor [1], FDNR [2], oscillator [3], Filter [4] and few more. The circuit elements such as positive and negative inductor, negative capacitance and resistance cannot be realized directly; therefore, an appropriate interconnection of active building block (ABB) and passive component is used for this purpose. Further, the usefulness of immittance emulators in designing filter, oscillator, multivibrator etc. and cancelling parasitics has attracted researchers' attention leading to presentation of such circuits. The applications may use grounded or floating immittances and the present work addresses floating immittances. Literature survey on available integer order floating immittance emulators shows that – Refs. [5,7–9,11–14,17,19–27,29–32,33,34,37–46,48–51,53–56] provide only positive immittances. while those reported in Refs. [6,10,15,16,18,20,28,35,36,41,45,47,52] furnish both positive and negative immittance by tweaking the topology (changing the components at the different terminals of the active building block (ABB) to achieve a particular mode of operation). A detailed study of these topologies reveals that – impedance tuning is not available in Refs. [5,8,9,11–13,16,17,19,22,23,25,27,37,41–44,49,52,53]; Refs. [5,6,8–13,16,17,22,23,25–31,35–38,41–44,47–55] employ more than one passive components; matching is required in Refs. [5,22,25,30,41,48,49,52], Topological change (interchanging of input terminals, changing components' placement)/different circuit design is required for providing positive and negative immittance [6,10,15,16,20,28,35,36,41,45,47,52]. It is clear from above discussion that a limited literature is available integer order floating immittance emulators that may simultaneously fulfil the following criterions: tunability, no matching constraint and working in positive and negative mode without topological changes. Further, it is pertinent to mention here that the topological change is not possible once the circuit is laid down and fabricated. Also, if two different circuits are realized in IC form for positive and negative immittances, the resulting silicon footprint would require more area. Therefore, it would be beneficial to have a reconfigurable or unified immittance emulator that does not require tweaking of the topology, instead relies on turning on/off a certain set of switches to achieve the desired mode of operation. This paper fills this gap by presenting a CCTA based unified floating immittance emulator topology that inherits electronic tunability; does not impose any restriction on component values and can make both positive and negative immittances available. The proposed topology employs two CCTAs, two additional components (two MOS based resistors, one capacitor and one MOS

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Electronically tunable positive and negative fractional order inductor circuit using single topology

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ABSTRACT

This article presents electronically tunable grounded and floating fractional order inductor circuits. The proposed circuits employ two operational transconductance amplifiers (OTAs), one fractional order capacitor, one inverter and four MOS switches and are capable to work in positive mode and negative mode without change in topology. The behaviour of the proposed circuit is also analyzed in presence of parasites that may appear in the practical circuit. The functional verification is done via pre and post layout simulations at 90 nm CMOS technology parameter. The usefulness of the proposed positive fractional inductor circuit is demonstrated through fractional order band pass filter and fractional order high pass ladder filter. The performance of the proposed negative fractional inductance circuit is demonstrated through a fractional inductance cancellation circuit.

1. Introduction

Fractional calculus is a powerful and widely used tool to demonstrate the characteristics of many systems in the real world such as thermodynamic [1], volcanology [2], human organ [3], biomedicine [4], earthquake [5], modelling of virus [6] and many more. The fractional order system offers an extra degree of freedom to control the phenomena of system. The fractional-order circuits and systems incorporate fractional calculus concepts and have immense potential in the areas of fractional order controller [7], fractional order signal generating [8,9] and signal processing circuits [10–12]. The basic building blocks for the design of a fractional order system are known as fractor having input impedance of $Z(s) = \frac{k_0}{s^\alpha}$ where α ($|\alpha| < 1$) represents order of fractor and k_0 is constant. Depending upon the value of α the behaviour of the element changes from fractional order inductor to fractional order capacitor. There is a lean presence of commercially available fractional order elements in literature [13,14]. Therefore, the researchers have made effort in the direction of approximating the fractional order capacitor behaviour (Carlson approximation [15], Matsuda approximation [16], Oustaloup approximation [17] Charef approximation [18] and Continued Fractional Expansion (CFE) [19]) and subsequently designing and developing emulators using appropriate RC ladder.

The fractional order inductor can be designed using a fractional order capacitor and general impedance converter (GIC) [13,14,20–28]. These inductors can be classified as positive and negative fractional order inductors. The former is used to design fractional order filter, fractional order oscillator, and modelling of the human respiratory system whereas the later may find application in parasitic inductance cancellation. Time domain expressions for the voltage across the fractional order capacitor and fractional order inductor [21] can be expressed as:

$$v^{\alpha}_{C_\alpha}(t) = \frac{1}{C_\alpha \Gamma(\alpha)} \int_0^t \frac{i(\tau)}{(t-\tau)^{1-\alpha}} d\tau \tag{1}$$

$$v^{\alpha}_{L_\alpha}(t) = L_\alpha \frac{d^\alpha i(t)}{dt^\alpha} \tag{2}$$

respectively. Here $\Gamma(.)$ denotes gamma function, $i(t)$ is the current through the fractional order device. The C_α and L_α represents fractional capacitor and fractional inductor respectively with corresponding units of $F/s^{1-\alpha}$ or $\Omega^{-1}s^{-\alpha}$ and $H/s^{1-\alpha}$ or $\Omega^{+1}s^{+\alpha}$.

Over the years, GIC based fractional inductor simulators [13,14,20–28] have been presented in the literature. The features of available fractional inductance simulators are summarized in Table 1. A careful examination of Table 1 reveals that these circuits:

(1) Require more than one active block [13,14,20–23,25].
(2) Need two or more passive components for realization [13,14,21–24].
(3) Presented in Refs. [13,14,21–24] do not possess tunability.

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CCTA based four different pairs of mutually coupled circuit using single topology

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ABSTRACT

This article presents a tunable Synthetic Transformer (ST) namely Mutually Coupled Circuit (MCC) based on Current Conveyor Transconductance Amplifier (CCTA). The proposed circuit consists of two CCTA, three resistors, two capacitors and four MOS switches and can be configured in four different pairs of mutual coupled circuit through appropriate setting of MOS switches. The proposed ST does not require component matching condition. Self-inductance, mutual inductance, and resonant frequency can be tuned by bias current of CCTA. Furthermore, non-ideal effects on the proposed ST are discussed. Performance of the proposed circuit is evaluated by pre-layout and post-layout simulation using 90 nm CMOS process technology. A double tuned band pass filter is shown as an application. The impact of supply voltage and temperature variation is examined and a maximum deviation of 3.326% and 16.8% respectively are observed in resonant frequency of DTBPF. The effect of component variations is also studied through Monte Carlo analysis. The output noise spectral density of DTBPF at resonant frequency is observed to be 102.489 nV/sqrt (Hz) whereas the total harmonic distortion is observed within 1.3% for peak input voltage range 0.05 V–3.5 V. The power consumption of DTBPF circuit is 5.16 mW at 100 μA bias current of CCTA.

1. Introduction

The synthetic transformer (ST) circuit is widely utilized in circuits pertaining to control systems, analog telecommunication, analog signal processing, instrumentation, and measurement. Its design involves active block(s) and their appropriate connection with resistor(s) and capacitors. The STs provide relation between their ports' voltages and currents without actual magnetic couplings. The coupling coefficient (k) of ST is adjusted either by varying the bias current of active block circuit or by changing the values of resistors used therein. The ST does not show magnetic interferences because of absence of inductive components. Absences of bulky inductive components make ST suitable for integrated circuit. However, the performance of ST is limited by parasitic components associated with active block.

Literature survey reveals that STs have been reported [1–16] using different active building blocks. The ST reported in Refs. [1,2] uses Bipolar Junction Transistor (BJT) while those reported in Refs. [3–18] employ active blocks. Moreover, large number of resistors and capacitors utilized in Refs. [1], [2], [3,5,6]. The features of the available active blocks based STs [3–18] are placed in Table 1. It is observed that variety of active blocks namely – Operational Amplifier (Op-amp) [3], Operational Transconductance Amplifier (OTA) [4], Second Generation Current Conveyor (CCII) [5–7], Second Generation Current Controlled Conveyor (CCCII) [8,9], Differential Voltage Current Conveyor (DVCC) [10], Current-Controlled Current Backward Transconductance Amplifiers (CC-CBTA) [11], Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [12], Current-Controlled Current Conveyor Transconductance Amplifier (CC-CCTA) [13], Current Backward Amplifier (CBTA) [14], Current Feedback Operational Amplifier (CFOA) [15], Voltage Differencing Current Conveyor (VDCC) [16] have been used to design the ST. The number of active blocks and passive components in available STs vary from 2 to 8 and 2 to 11 respectively. The STs [3–11], [15] use more than two active blocks while those presented in Refs. [3,5–18] consist of more than two passive components. The STs reported in Refs. [3], [5], [6,7,15] do not facilitate tuning feature. The overall transistor count in Refs. [7–12], [15], [18] is more than 46 transistors and therefore these circuits may require a larger chip area for realization.

Further, the study of available STs reveals that no circuit is present featuring mutual inductance in four different pairs and this forms the

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A programmable tunable active grounded and floating immittance circuit using CCTA and their applications

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ABSTRACT

This article presents a novel grounded and floating immittance circuit. It can simulate any one of the floating and grounded positive and negative inductor circuit, positive and negative capacitor circuit, and positive and negative resistor circuit. The novelty of the proposed circuit is its capability to provide positive and negative immittances without any change of passive component and matching condition. In addition, active realisations of positive and negative fractional order immittance circuits are presented. Thus, this paper presents 16 types of immittances which cover entire two-dimensional phase plane. Grounded immittance circuit uses one active block Current Conveyor Transconductance Amplifier (CCTA), one grounded MOS resistor and one grounded passive component while floating immittance circuit employs two CCTAs and three components. The immittance of the proposed circuits can be tuned by changing the bias current of CCTA and bias voltage of MOS resistor. The frequency responses of the proposed circuits are verified using SPICE simulation based on the 0.18 μm TSMC CMOS technology parameter. The performance of the proposed positive immittance circuits is demonstrated by active filter design using SPICE in conjunction with MATLAB. The performance of the proposed negative immittance circuit is demonstrated through inductance cancellation.

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Grounded and floating immittance circuit; Positive and negative immittance circuit; Integer and fractional order immittance circuit; Active filters; CCTA

1. Introduction

An immittance circuits play an important role in the field of electronics, communication, instrumentation and measurement. It can be classified as positive, negative, grounded, floating, integer and fractional. A positive immittance circuit finds application in areas like active filter, oscillator, chaos circuit whereas negative immittance circuit may be used for cancellation of parasitics. The wide applications of immittance simulators have attracted researchers' interest in the past literature. Numerous active blocks have been used to design the integer order immittance circuit. Some of these active blocks are: First Generation Current Conveyor (CCI) (Arslan et al., 2012), Second Generation Current Conveyor (CCII) (Cicekoglu, 1998), Operational Transresistance Amplifier (OTRA) (Ghosh & Paul, 2014; Kilinc et al., 2006; Nagar & Paul, 2019; Pandey, Pandey, et al., 2011, 2014),

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Grounded and floating memristor emulator employing ICCTA: decremental or incremental operation

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ABSTRACT

This article describes floating and grounded memristor emulator built with an Inverting Current Conveyor Transconductance Amplifier (ICCTA). One ICCTA, one capacitor, and three resistors are used to implement the charge controlled floating memristor emulator. In contrast, a flux controlled grounded memristor emulator consists of one ICCTA, one resistor, and one capacitor. Both presented circuits do not incorporate complex circuits such as analog multiplier circuits, passive inductors, and analog to digital converter circuits in their implementation, which is advantageous in terms of circuit realisation. The designed circuits may be operated in incremental as well as decremental configurations by appropriate setting of MOS switches. In addition, PVT (process, voltage, and temperature) analysis of the proposed memristor is also included. Furthermore, the non-ideal explanation of the proposed circuits is mathematically examined. The proposed emulators are simulated in SPICE simulator using 180 nm technology. Meminductor circuit and memristor-based low pass filter are used to validate the effectiveness of the designed circuits.

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ICCTA; memristor emulator; meminductor emulator; Pinch Hysteresis Loop (PHL); memristor-based active filters

1. Introduction

A memristor is the fourth fundamental element (Tour & He, 2008) in circuit theory after resistor, capacitor, and inductor. It is a non-linear device depending upon the previous history of current. It establishes a relation between charge and flux (Chua, 1971). This relation is first observed by Chua (1971). Memristance of the memristor retains its final value in absence of the input signal, known as the non-volatile nature of the memristor. The non-volatile nature and non-linear properties make memristor suitable for numerous applications like sensors (Adeyemo et al., 2018), memory computing (Thangkhiew et al., 2020), digital circuits (Maruf et al., 2022), neural networks (Abdoli & Safari, 2020), neuromorphic circuits (An et al., 2019), buck-converter (Zhou et al., 2023), relaxation oscillators (Fouda & Radwan, 2014; Yu et al., 2014), and chaotic oscillators (Hua et al., 2021; Kamdem Tchiedjo et al., 2023). The first solid-state memristor is developed by Hewlett-Packard (H.P.) lab employing platinum (Pt) metal and thin titanium dioxide (Tio_2). This solid-state device is not currently accessible in the market due to its high cost and complex fabrication process. This issue may be

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Single DXCCTA based Charge Controlled Floating Incremental/Decremental Memristor Emulator

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***Abstract* - This article offers a charge controlled floating incremental/decremental memristor emulator using Dual-X Current Conveyor Transconductance Amplifier (DXCCTA). The proposed circuit includes one DXCCTA, four resistors, one grounded capacitor and two MOS switches. Incremental and decremental mode of operation depends upon setting of MOS switch. This paper avoids the utilization of analog multiplier circuit. Pinch hysteresis curves of proposed circuit are hold up to 60 MHz. Moreover, two memristor combinations are connected in series and parallel to examine the functionality of the proposed memristor emulator, and the intended results are acquired. Performance of the designed circuit is evaluated, at schematic level 90 CMOS process technology, are presented.**

Keywords- Memristor Emulator, Mem-immittance Circuit, Pinch Hysteresis loop, DXCCTA.

I. INTRODUCTION

Memristor is two terminal passive component that provides connection between electric charge (q) and magnetic flux (φ). It is known as fourth element [1,2] after inductor, capacitor, and resistor. Non-volatile nature of memristor provides various applications such as programmable gate array [3], programmable analog circuit [4], neuromorphic computing circuit [5], adaptive filter [6], hyperchaotic oscillator [7], relaxation oscillator [8,9] and many more. Memristor is conceived by L. O. Chua in 1971.First solid state memristor is fabricated by Hewlett-Packard (H. P.) lab in 2008. This solid state memristor is designed by sandwiching titanium dioxide between two platinum plates. Due to its exorbitant price and challenging fabrication method, this solid state memristor is not easily obtainable. This limitation motivates to researcher to develop active building block (ABB) based memristor circuits. Literature survey of ABB based memristor emulator is given below.

Sozen and cam [10] proposed flux controlled floating memristor circuit. It includes four second generation current conveyor (CCII), three operational transconductance amplifier (OTA), six resistors and one grounded capacitor. 10 kHz is maximum operating frequency of the circuit. Tahir and khalifa [11] introduced a floating memristor circuit. This circuit consist of four AD844 IC, two diodes, four resistors and four capacitors. Lopez et al. [12] designed charge control grounded memristor emulator. This circuit uses two ADD844N IC (integrated circuit), one AD633JN IC, four resistors and three capacitors. Pinch hysteresis curve of the designed circuit maintained up to 160 kHz. Lopez et al. [13] introduced flux controlled floating memristor circuit. This circuit uses four ADD844N IC, one AD633JN IC, five resistor and one capacitor. 20.2 kHz is operating frequency of the designed circuit. Kanyal et al. [14] proposed flux controlled floating memristor emulator. This circuit uses two OTAs and one grounded capacitor. Maximum operating frequency of designed circuit is 400 kHz. Ranjan et al. [15] introduced charge controlled floating memristor emulator. The proposed circuit includes one current conveyor transconductance amplifier (CCTA), three resistors and one capacitor. 10 MHz is maximum frequency of operation of this circuit. A Charge controlled grounded memristor emulator was proposed by Ranjan et al. [16]. One differential voltage current conveyor transconductance amplifier (DVCCTA), three passive resistors, and one capacitor are used in the designed circuit. Operating frequency of this circuit is 1MHz. Yesil et al. [17] designed floating memristor emulator established on differential difference current conveyor (DDCC). This circuit consist of one DDCC, two resistors, one multiplier circuit and one grounded capacitor. Maximum operating frequency of the designed circuit is 1 MHz. Vista and Ranjan [18] proposed flux controlled floating memristor emulator. Proposed circuit includes one voltage difference transconductance amplifier (VDTA), one passive resistor and one grounded capacitor. Operating frequency of designed emulator is reported as 50 MHz. Petrovic [19] introduced flux controlled floating memristor emulator circuit. This circuit is designed with help of one VDTA, one analog multiplier circuit, two passive resistors, one grounded capacitor. Output range of frequency of proposed circuit is 2 MHz. Yadav et al. [20] designed flux controlled floating memristor emulator circuit. This circuit includes one voltage differencing buffered amplifier (VDBA) as an ABB and one capacitor as passive component. 1 MHz is operating frequency of the designed circuit. Yesil et al. [21] introduced flux controlled grounded memristor circuit. This circuit is designed using one voltage differencing current conveyor (VDCC), one grounded capacitor and two MOS resistor. Maximum operating frequency of designed circuit is 2 MHz. Raj et al. [22] introduced flux controlled grounded memristor emulator circuit. This circuit includes one CCII, one OTA, one resistor and one grounded capacitor. 26.3 MHz is maximum operating frequency of this circuit. A grounded memristor circuit is introduced by Ayten et al. [23]. One current backward transconductance amplifier (CBTA), two passive resistors, one analogue multiplier circuit, and one capacitor are used.460 kHz is maximum operating frequency of the designed circuit.

In this study we present charge controlled floating incremental/decremental memristor emulator circuit. The designed circuit consists of one DXCCTA as active

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A Grounded Flux Controlled Incremental/Decremental Memristor Emulator

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Abstract - Single Inverting Current Conveyor Transconductance Amplifier (ICCTA) based flux controlled grounded incremental/decremental memristor emulator is presented in this article. The proposed circuit uses one ICCTA, one grounded resistor, one grounded capacitor. This realization is appropriate for monolithic integration due to the usage of grounded passive devices. Analog multiplier circuit is not required to design the circuit. Additionally, a high pass filter circuit demonstrates how well the suggested memristor emulator works. Using a 180 nm CMOS process, the suggested circuit and its utility are assessed.

Keywords- Memristor Emulator, Mem-immittance Circuit, Pinch Hysteresis loop, ICCTA.

I. INTRODUCTION

The fourth [1-2] fundamental nonlinear element known as memristor is gaining considerable attention among the researchers due to its high-density storage property. Leon O. Chua developed memristor by giving the relation between electric charge and magnetic flux in 1971. Since memristor has nonlinear characteristic, non-volatile nature, and high density storge properties, it is being used in a variety of applications such as programmable gate arrays [3], programmable analogue circuits [4], neuromorphic circuits [5], adaptive learning [6], adaptive filters [7], chaotic oscillators [8], and relaxation oscillators [9-10] etc. After 37 years of proposal of memristor by L O. Chua, Hewlett-Packard (H. P.) lab created the first solid-state memristor in 2008. Due to its high price and difficult manufacturing process, this solid state memristor is not currently accessible on the market. This constraint spurs researchers to create memristor circuits based on active building blocks (ABB). Below is a literature review of an ABB-based memristor emulator.

There are few publications on the realisation of charge and flux controlled memristor circuit, using advance active blocks such as Second Generation Current Conveyor (CCII) [11-14], Operational Transconductance Amplifier (OTA) [15], Current Conveyor Transconductance Amplifier (CCTA) [16], Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [17], Differential Difference Current Conveyor (DDCC) [18], Voltage Difference Transconductance Amplifier (VDTA) [19,20], Voltage Differencing Buffered Amplifier (VDBA) [21], Voltage Differencing Current Conveyor (VDCC) [22], Current Backward Transconductance Amplifier (CBTA) [24]. The reported flux and charge controlled memristor emulator suffer from the following disadvantages:

(1) Memristor emulator reported in [8,9,11,12,13,14,15,26] need more than one active block.
(2) Memristor emulator introduced in [8,9,11-14,16-18,20,25,26] required more than two passive components.
(3) Memristor emulator designed in [8,9,11,12,13,14,16-18,26] need floating passive component.
(4) Memristor emulator presented in [4,8,9,13,14,18,20,24,26] use additional circuit like analog multiplier, Digital to analog converter and analog to digital converter.
(5) Memristor emulator reported in [8,9,11-15,26] operates in low frequency range.
(6) Memristor emulator illustrated in [25] uses passive inductor.

This article presents flux controlled grounded incremental/decremental memristor emulator. The proposed circuit uses one ICCTA as active components, one grounded capacitor and one grounded passive resistor as passive components. The suggested circuit can be designed without the use of additional circuitry, such as an analog multiplier circuit. In addition, Memristor based first order high pass filter circuit shows the usefulness of proposed circuit. Remaining paper is organized as follow: Circuit description of proposed circuit is discussed in section2. Simulation results of proposed memristor is discussed in section 3. The suggested circuit's application is shown in Section 4. The research article is concluded in section 5.

II. CIRCUIT DESCRIPTION

An ICCTA is a versatile active building block. The block symbol and its MOS based block realization is illustrated in Fig.1. The port relation of ICCTA is given in equation (1).

$$I_Y = 0; V_{X-} = -V_Y;\ I_{Z-} = I_{X-};\\ I_{0+} = g_m V_{z-};\ I_{0-} = -g_m V_{z-} \quad (1)$$

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