DEVELOPMENT OF CM CIRCUITS FOR ANALOG SIGNAL PROCESSING AND SIGNAL GENERATION

A Thesis Submitted
In Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

by

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CANDIDATE'S DECLARATION

I Parveen Rani hereby certify that the work which is being presented in the thesis entitled Development of CM Circuits for Analog Signal Processing and Signal Generation in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August, 2016 to December, 2024 under the supervision of Prof. Rajeshwari Pandey.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

This is to certify that the statement made by the candidate is correct to the best of my knowledge.

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CERTIFICATE BY THE SUPERVISOR

Certified that **Parveen Rani** (2K16/PhD/EC/08) has carried out her research work presented in this thesis entitled **"Development of CM Circuits for Analog Signal Processing and Signal Generation"** for the award of **Doctor of Philosophy** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

Signature

(Prof. Rajeshwari Pandey)
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Date: /12/2024

Abstract

Over the past couple of decades, analog signal processing (ASP) has seen a paradigm shift from voltage mode (VM) to current mode (CM) design technique due to inherent merits of the CM processing. Though the design techniques are fundamentally limited by device characteristics; however, for specific applications CM design may provide one or more of the following advantages: higher bandwidth and slew rates, lower power consumption and better signal linearity and accuracy. Additionally, current mode circuits may lead to significant chip area saving also owing to their less complex designs than the voltage mode circuits.

The merits of CM design has led researchers to explore variety of CM analog building blocks (ABBs) and existence of numerous such blocks in literature is a testament of the same. These ABBs find applications in various analog signal processing and generating circuits. The voltage differencing transconductance amplifier (VDTA) is one among the other CM ABBs which is conceptually presented by Biolek et al. in 2008. The VDTA is a voltage input current output ABB having two transconductance gain stages which helps in realization of resistor-less compact CMOS applications. Additionally, the transconductances of the VDTA can be tuned through bias current which facilitates electronic tunability of the system parameters. Thus, VDTA is a preferred choice for designing on-chip high frequency applications. Its first CMOS realization was present by Yesil et al. in 2011.

Further, fractional order (FO) circuits and systems are gaining researcher's increased attention as these provide extra degree of freedom and models natural systems more precisely as compared to their integer order counterparts. Fractional order elements (FOEs) namely fractional capacitors and inductors (FCs and FIs) are the basic building blocks for realizing FO circuits. Though the FCs and FIs are not commercially available as circuit components but a variety of rational approximation methods exists in the open literature to emulate the FCs. The FIs can be derived through classical methods which are used in integer domain for emulating inductors using capacitors.

Thus, combining the advantages of CM processing with fractional order designs researchers have proposed a wide range of signal processing and generation

application using variety of ABBs. This research trend has been explored in context of VDTA having identified the advantages of VDTA based designs in the presented work. Additionally, this work also presents few integer order applications of the VDTA.

Exploring significant avenue of the active inductance emulation, VDTA based compact, resistor-less generic inductance emulator (IE) have been proposed. This emulator can be configured as (i) integer order positive inductance emulator (ii) integer order negative inductance emulator (iii) fractional order positive inductance emulator and (iv) fractional order negative inductance emulator.

Research contribution in the domain of analog filter design is presented in the form of a classical integer order filter and two α-order voltage mode fractional order filters (FOFs) based on VDTA. The integer order filter is a multiple input multiple output biquad filter. Moving on to the fractional order counterparts, first FOF represents voltage mode multiple input single output universal configuration whereas, second FOF topology presents voltage mode single input multiple output multifunction structure.

Further, there is considerable scope for exploring improved design of higher order sinusoidal oscillators. In that attempt, a third order sinusoidal oscillator (TOSO) has been proposed using a single VDTA.

In this work proposition of new CMOS structures of the VDTA are also explored and its outcome has led to the proposition of two new transconductance boosted architectures of the VDTA. The former structure is based on the partial positive feedback whereas the later utilizes the concept of gate to source voltage variation for transconductance enhancement.

The proposed designs are verified either through simulations or combination of simulations and experimental validation. The simulations are carried out either with Cadence tool suite or PSPICE using 180 nm CMOS technology parameters. For experimental purpose, the VDTA is implemented using off the shelf IC LM13700 with ±10V supply voltage.

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List of Abbreviations

Analog Building Blocks	ABBs
Analog Signal Processing	ASP
Current Conveyor	CC
Current Differencing Buffered Amplifier	CDBA
Current Differencing Transconductance Amplifier	CDTA
Current Feedback Operational Amplifier	CFOA
Current Mode	CM
Fractional order Capacitor	FC
Fractional order Inductor	FI
Fractional order All Pass Filter	FAPF
Fractional order Band Pass Filter	FBPF
Fractional order Band Stop/Reject Filter	FBSF/FBRF
Fractional order High Pass Filter	FHPF
Fractional order Low Pass Filter	FLPF
Fractional Order	FO
Fractional Order Elements	FOEs
Fractional Order Filter	FOF
Multiple Input Multiple Output	MIMO
Multiple Input Single Output	MISO
Multiple-output Voltage Differencing Transconductance Amplifier	MO-VDTA
Second-generation Current Conveyor	CCII
Single Input Single Output	SISO
Single Input Multiple Output	SIMO
Sinusoidal Oscillator	SO
Third-generation Current Conveyor	CCIII
Third Order Sinusoidal Oscillator	TOSO
Transadmittance Mode	TAM

Transimpedance Mode	TIM
Voltage Differencing Transconductance Amplifier	VDTA
Voltage Mode	VM
Z-copy Voltage Differencing Transconductance Amplifier	ZC-VDTA

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CHAPTER – 1

INTRODUCTION

1.1 Introduction

Researchers are continuously striving to explore different analog building blocks (ABBs) with attributes like higher bandwidth, higher slew rate, lower power consumption and better linearity. This has led to paradigm shift from voltage mode (VM) to current mode (CM) [1,2] signal processing. Numerous CM ABBs have evolved as presented in [3] and references cited therein. The current conveyor (CC) [4], a hybrid voltage/current circuit, is the most exhaustively explored/utilized block. Since then, three generations of the CC; namely CCI, CCII [5] and CCIII [6], which differ in terms of the terminal characteristics were introduced way back in 1968, 1970 and 1995 respectively. The current feedback operational amplifier (CFOA) [7] has terminal characteristics that resemble those of a CCII followed by a voltage follower. The circuit element operational transresistance amplifier (OTRA) [8] serves/functions as a current controlled voltage source (CCVS). Recently, yet another class of CM blocks having current differencing input stage, has also emerged. Current Differencing Transconductance Amplifier (CDTA) [9] and current differencing buffered amplifier (CDBA) [10] are two notable examples of this class. The voltage differencing transconductance amplifier (VDTA) is yet another versatile CM analog building blocks available in literature. The VDTA is a voltage input current output ABB having two transconductance gain stages which helps in realization of resistor-less compact CMOS applications. Additionally, the transconductances of the VDTA can be tuned through bias current which facilitates electronic tunability of the system parameters. Thus, VDTA is a preferred choice for designing on-chip high frequency applications. This has led to realization of various signal processing [11-43] and generation [44-53] applications based on VDTA. Its CMOS implementation was first proposed by Yesil et al. [11]. Since then, various research efforts are made to propose CMOS implementations [11,15,18,27,110-112] of VDTA with enhanced performance.

On the other hand, fractional order (FO) signal processing which is based on the fundamentals of fractional calculus is an emerging interdisciplinary research area. Fractional calculus is the domain of mathematics concerned with the investigation and application of derivatives and integrals of arbitrary (real or complex) order [54-56]. A fractional derivative of order 'α' may be represented by the Riemann–Liouville definition

$$D^{\alpha} f(t) := \begin{cases} \dfrac{1}{\Gamma(n-\alpha)} \dfrac{\partial^n}{\partial t^n} \displaystyle\int_0^t \dfrac{f(\tau)}{(t-\tau)^{\alpha+1-n}} \partial\tau & ;\mathrm{n}-1<\alpha<n \\ \dfrac{\partial^n}{\partial t^n} f(t) & ;\alpha = n \end{cases} \tag{1.1}$$

The Grunwald–Letnikov approximation gives a more physical interpretation of a fractional derivative

$$D^{\alpha} f(t) \triangleq (\Delta t)^{-\alpha} \sum_{i=0}^{n} \frac{\Gamma(i-\alpha)}{\Gamma(-\alpha)\Gamma(i+1)} f\left((n-i)\Delta t\right) \tag{1.2}$$

where Δt represents the integration step. In order to describe electronic circuits in the complex frequency s-domain, Laplace transform is widely used. Thus, assuming zero initial conditions and applying the Laplace transform to Eqn. (1.2), yields

$$L\left\{ {}_0\partial_t^{\alpha} f(t) \right\} = s^{\alpha} F(s) \tag{1.3}$$

where ${}_0\partial_t^{\alpha} f(t) = \partial f(t)/\partial t$ with zero initial conditions.

Fractional order circuits and systems are gaining researchers' increased attention as these provide extra degree of freedom and models natural systems more precisely [57-59] as compared to their integer order counterparts. These circuits find potential applications pertaining to biomedical, instrumentation and control and analog signal processing and generation. Fractional order elements (FOEs) are the basic building blocks for realizing FO circuits and may be characterized by the generalized impedance function

$$Z_F^{\alpha}(s) = Ks^{\alpha} = K\omega^{\alpha}\exp\left(j\left(\alpha\pi/2\right)\right) \tag{1.4}$$

where '*K*' is termed as fractance and 'α' represents the order of the FOE. The phase of the FOE does not depend on the frequency and remains incessant; hence it can also be termed as a constant phase element (CPE) and the corresponding phase can be referred as the constant phase angle (CPA). The 'α' is a fractional number in the range -n < α < n, where 'n' is an integer number. The generalized impedance function of Eqn. (1.4) represents impedance of a fractional capacitor (FC) if 'α' assumes a negative value and a positive 'α' value corresponds to impedance of fractional inductor (FI) as depicted in Fig. 1.1.

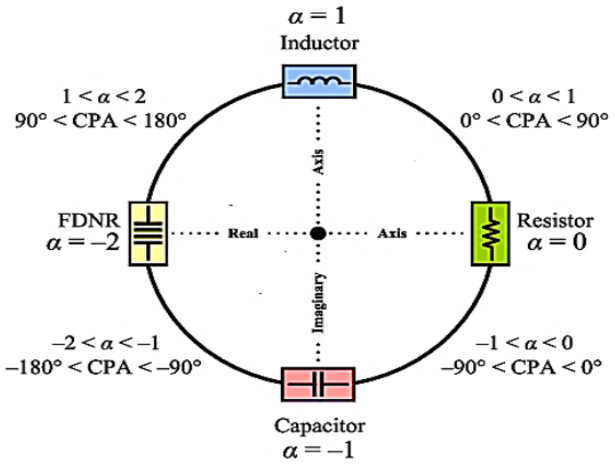


Fig. 1.1 Classification of Fractional Order Elements [60].

The fractional order elements (FOEs) namely FCs and FIs are not commercially available as circuit components. However, the research efforts are being directed towards designing physical FCs [57-59] though, still at very primitive phase. A variety of rational approximation methods [61-69] exists in the open literature to emulate the behaviour of FCs in the range (-1 < α < 0). The FCs so derived can be realized using appropriately configured RC networks depicted in Fig. 1.2.

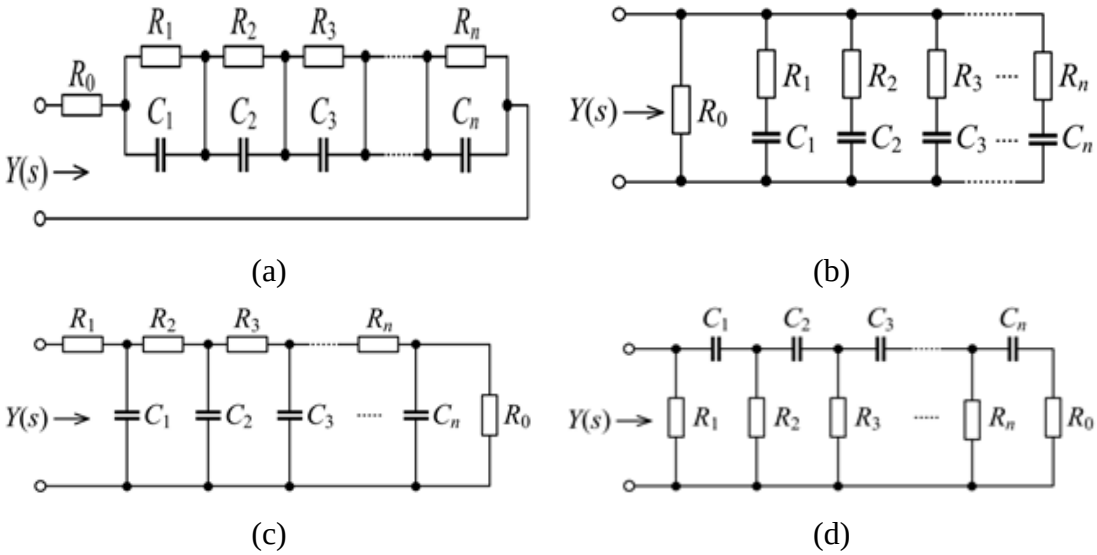


Fig. 1.2 RC Networks for FC Emulation (a) Foster-I (b) Foster-II (c) Cauer-I (d) Cauer-II.

In last few decades analog signal processing has seen a paradigm shift from voltage mode (VM) to current mode (CM) due to inherent advantages of CM processing. Combining the advantages of fractional order designs with CM processing, researchers have proposed a variety of signal processing and generation applications using variety of ABBs. In this work this research trend has been explored in context of VDTA having identified the advantages of VDTA based designs.

1.2 Literature Review

It is observed through comprehensive literature survey that a wide range of electronic circuits using VDTA have been proposed in the literature which broadly include application areas such as grounded inductance simulation [12,13], filter design [11,14-43], signal generation [44-53] and VDTA implementation [11,15,18,27,110-112].

1.2.1 Inductance Emulation

Inductors are an integral part of the electronic circuit design; however, designing an inductor on a chip has issue/challenge in terms of the usage of space, weight, cost and tunability. Thus, it is desired to simulate an inductor using the active components

available thereby saving in chip area. Further, to reap the advantages of fractional order processing; fractional order inductor (FI) realization is equally important. The fractional inductor in the range ($0 < \alpha < 1$) [70-77] can be emulated using various active RC methods similar to their integer order counter parts. These systematic methods include functional block diagram (FBD) approach and generalized impedance converter (GIC) based realization. These methods use large number of active blocks for FI realization. Alternatively, the FI can also be realized using direct intuitive methods using different active blocks and few passive components. An exhaustive review suggests that though VDTA based integer order grounded inductances realizations are available [12,13] in literature but no fractional order inductors are existing. A further exploration suggested that few realizations of FI [69-76] using ABBs other than VDTA are available as enlisted in Table 1.1(a). Additionally, detailed comparison of a few available conventional integer order inductance simulators [12,13,78-86] has been presented in Table 1.1(b) for ready reference.

Table 1.1(a) Literature Summary for Fractional Order Inductance Emulators ($0 < \alpha < 1$).

Ref.	ABB No. Type	Passive Elements		Method Used	Emulator Type (Positive /Negative /Both)	Electronic Tuning
		C/FC	R			
[70]	1 DXCCTA	1C (G)	0	Direct Method	Both	Yes
[71]	1 CCTA	1FC (G)	1R (G)	Direct Method	Both	Yes
[72]	2 Op-Amps	1FC (F)	4R (1G+3F)	GIC	Positive	No
[73]	9 OTAs	2C (G)	0	FBD	Positive	Yes
[74]	1 CFOA	1FC (F)	2R (1G+1F)	Direct Method	Positive	No
[75]	2 Op-Amps	1FC (F)	4R (1G+3F)	GIC	Positive	No
[76]	1 OTA + 10 Op-Amps	3C (F)	17R (F)	FBD	Positive	No
	23 CCIIs	3C (G)	14R (G)	FBD	Positive	No
	10 CFOAs	3C (G)	17R (8G+9F)	FBD	Positive	No
	14 OTAs	3C (G)	0	FBD	Positive	Yes
[77]	3 CFOAs	1FC (G)	3R (2G+1F)	Direct Method	Positive	No

Table 1.1(b) Literature Summary for Integer Order Inductance Emulators.

Ref.	ABB No. Type	Passive Elements		Emulator Type (Positive /Negative /Both)	Electronic Tuning
		C	R		
[78]	1 OTRA	1C (F)	5R (2G+3F)	Negative	No
[70]	1 DXCCTA	1C (G)	0	Both	Yes
[71]	1 CCTA	1C (G)	1R (G)	Both	Yes
[79]	2 CCCDBAs	1C (G)	0	Negative	No
[80]	1 DXCCII	1C (F)	2R (1G+1F)	Both	No
[81]	1 CBTA	1C (G)	1R (1G)	Both	No
[82]	1 ZC-CCCITA	1C (G)	0	Both	No
[83]	1 VDCC	1C (G)	1R (1G)	Both	No
[84]	1 OTRA	1C (F)	4R (4F)	Negative	No
[85]	1 OTRA	1C (F)	3R (3F)	Negative	No
[86]	1 CDBA	1C (G)	3R (1G+2F)	Negative	No
[12]	1 VDTA	1C (G)	0	Positive	Yes
[13]	1 VDTA	1C (G)	0	Positive	Yes

It may be observed from Table 1.1(a) that

- only two topologies [70,71] can emulate both negative and positive fractional order inductance. Further, the topology presented in [71] makes use of resistance
- the emulators of [72,73,75-77] use large number of ABBs
- the existing topologies use large number of resistances [71,72,74-77] and capacitances [73,76]
- Refs. [70,71,74,77] use direct method while [72,75] and [73,76] make use of GIC and FBD based approaches respectively
- Refs [72,74-77] use floating components
- inductance emulators [72,74-77] lack electronic tuning.

Further, inspection of Table 1.1(b) suggests that

- existing designs [71,80,81,83-86] use more number of passive components than the proposed one
- the structure of [79] makes use of more number of ABBs
- Refs. [80,84-86] use floating passive components as against the proposed topology which employs grounded capacitor only.

1.2.2 Analog Filter and Fractional order Filters

Filters are an important class of electronic circuits and widely used for analog signal processing for a wide range of applications. Further, the use of fractional order calculus in analog filter design offers the advantage of better control of the attenuation gradient in stop band as the magnitude response of an (n+α) order filter exhibits a stop-band attenuation of 20*(n+α) dB/decade, as against 20*n dB/decade by integer-order filter where, n represents an integer value. In order to achieve FO behaviour, the fractional order filters (FOFs) either make use of an emulated FOE or deploy a suitable integer-order transfer function, to obtain a fractional order

counterpart, which is subsequently realized using functional block diagram (FBD) approach.

The filter structures on the basis of number of inputs processed and outputs provided can be classified as single-input single-output (SISO), single-input multiple-output (SIMO) and multiple-input single-output (MISO) and multiple-input multiple-output (MIMO).

A detailed review of various VDTA based filters suggests a variety of SISO [14], SIMO [15-30], MISO [18,24,27,31-40] and MIMO [11] integer order VDTA based filters available literature. On the other hand, though a variety of fractional order filters (FOFs) [41-43,87-108] implemented around other ABBs are available but only limited VDTA based fractional order filters (FOFs) are reported [41-43]. Only two FOFs based on VDTA have been reported so far. Both the FOFs are designed using the FBD approach for fractional orders (α = 1.1, 1.5, 1.8). FOFs [41] are designed around three and four VDTAs providing fractional order band pass filter (FBPF) and fractional order band stop/reject filter (FBSF/FBRF) responses respectively. Likewise, [42] provides fractional order low pass filter (FLPF) and fractional order high pass filter (FHPF) responses respectively. A detailed comparison of all available conventional biquads and fractional-order filters has been presented in Tables 1.2(a) and 1.2(b) for ready reference.

Table 1.2(a) Literature Summary for VDTA based Integer Order Biquads.

Ref.	No. of VDTA(s)	Filter Mode Type	Passive Elements		Filter Response(s)
			R	C	
SISO Filters:					
[14]	1 VDTA	VM (SISO)	0	2C (1F+1G)	HP
SIMO Filters:					
[15]	1 VDTA	CM (SIMO)	0	2C (2G)	LP, BP, HP
[16]	2 VDTAs	CM (SIMO)	0	2C (2G)	LP, BP, HP
[17]	2 VDTAs	VM (SIMO)	2 MOS-R (2G)	2C (2G)	LP, BP, HP, BS, AP
[18]	2 VDTAs	TAM (SIMO)	0	2C (1F+1G)	LP, BP, HP
[19]	1 VDTA	CM (SIMO)	1R (G)	2C (2G)	LP, BP, HP, BS, AP
[20]	2 VDTAs	TAM (SIMO)	0	2C (2G)	LP, BP, HP
[21]	2 VDTAs	VM (SIMO)	0	2C (2G)	LP, BP
	2 VDTAs	CM (SIMO)	0	2C (2G)	LP, BP, BR
[22]	1 VDTA	CM (SIMO)	0	2C (2G)	LP, BP
[23]	1 VDTA	TAM (SIMO)	1R (F)	2C (2G)	BP, HP
[24]	2 VDTAs	TAM (SIMO)	0	2C (1F+1G)	LP, BP, HP

continued on page no 12

Table 1.2(a) (continued)

Ref.	No. of VDTA(s)	Filter Mode Type	Passive Elements		Filter Response(s)
			R	C	
SIMO Filters (continued):					
[25]	1 VDTA	TAM (SIMO)	1R (G)	2C (1F+1G)	LP, BP, HP, BR
[26]	1 VDTA	VM & CM (SIMO)	1R (G)	3C (1F+2G)	LP, BP, HP
[27]	2 VDTAs	TAM (SIMO)	0	2C (2G)	LP, BP, HP
[28]	3 VDTAs	VM (SIMO)	0	2C (2G)	LP, BP, HP
	3 VDTAs	TAM (SIMO)	0	2C (2G)	LP, BP, HP, BR, AP
[29]	1 VDTA	TIM (SIMO)	2 MOS-R (2G)	2C (2G)	LP, BP, HP, BR
[30]	2 VDTAs	VM (SIMO)	1R (G)	2C (2G)	LP, BP
MISO Filters:					
[31]	1 VDTA	VM (MISO)	0	2C (2F)	LP, BP, HP, BS, AP
[18]	2 VDTAs	VM (MISO)	0	2C (1F+1G)	LP, BP, HP, BS, AP
	2 VDTAs	TAM (MISO)	0	2C (1F+1G)	LP, BP, HP, BS, AP
[32]	2 VDTAs	CM (MISO)	0	2C (2G)	LP, BP, HP, BS, AP
[33]	1 VDTA	VM (MISO)	1R (G)	2C (2F)	LP, BP, HP, BS, AP

continued on page no 13

Table 1.2(a) (continued)

Ref.	No. of VDTA(s)	Filter Mode Type	Passive Elements		Filter Response(s)
			R	C	
MISO Filters (continued):					
[34]	1 VDTA	VM (MISO)	1R (F)	2C (1F+1G)	LP, BP, HP, BS, AP
[35]	1 VDTA	CM (MISO)	0	2C (2G)	LP, BP, HP, BS, AP
	2 VDTAs	CM (MISO)	0	2C (2G)	LP, BP, HP, BS, AP
[36]	2 VDTAs	CM (MISO)	2R (2G)	2C (2G)	LP, BP, HP, BS, AP
[37]	2 MO-VDTAs	TAM (MISO)	2 MOS-R (2G)	2C (1F+1G)	LP, BP, HP, BR, AP
[38]	1 VDVTA	VM (MISO)	1R (G)	2C (2F)	LP, BP, HP, BR
[24]	2 VDTAs	VM (MISO)	0	2C (1F+1G)	LP, BP, HP, BR, AP
[39]	1 VDTA	CM (MISO)	1R (G)	2C (2G)	LP, BP, HP, BR, AP
[27]	1 VDTA	VM (MISO)	1R (G)	2C (2F)	LP, BP, HP, BS, AP
[40]	1 VDTA	CM (MISO)	1R (G)	2C (2G)	LP, BP, HP, BR, AP
MIMO Filters:					
[11]	1 VDTA	VM (MIMO)	0	2C (1F+1G)	LP, BP, HP

Table 1.2(b) Literature Summary for Fractional Order Filters.

Ref.	ABB No. Type	Passive Elements			FOF Type	FOF Response(s)	Input/Output	Impedance
		R	C	FC				
[87]	1 Op-Amp	4R (3F+1G)	-	2FC (1F+1G)	SISO	Sallen-Key FLPF	Voltage/Voltage	Low
	1 Op-Amp	4R (2F+2G)	-	2FC (2F)	SISO	Sallen-Key FHPF	Voltage/Voltage	Low
	1 Op-Amp	5R (3F+2G)	-	2FC (1F+1G)	SISO	Sallen-Key FBPF	Voltage/Voltage	Low
	3 Op-Amps	6R (6F)	-	2FC (2F)	SIMO	FO-KHN (FLPF, FBPF, FHPF)	Voltage/Voltage	Low
[88]	3 Op-Amps	6R (6F)	1C (1F)	1FC (1F)	SIMO	FO-TT (FLPF, FBPF)	Voltage/Voltage	Low
[89]	3 Op-Amps	6R (6F)	-	2FC (2F)	SIMO	FO-KHN (FLPF, FBPF, FHPF)	Voltage/Voltage	Low
[90]	2 Op-Amps	4R (2F+2G)	2C (2F)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
	4 Op-Amps	7R (7F)	2C (2F)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
	2 Op-Amps	4R (3F+1G)	2C (1F+1G)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
	4 Op-Amps	6R (6F)	2C (2F)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
	2 CCIIs	4R (4F)	2C (2F)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
[91]	2 Op-Amps	3R (2F+1G)	1C (1F)	1FC (1F)	SISO	FLPF, FHPF, FBPF	Voltage/Voltage	Low

continued on page no 15

Table 1.2(b) (continued)

Ref.	ABB No. Type	Passive Elements			FOF Type	FOF Response(s)	Input/Output	Impedance
		R	C	FC				
[92]	3 Op-Amps	6R (6F)	-	2FC (2F)	SIMO	FO-KHN	Voltage/Voltage	Low
[93]	5 CCII (3CCII+ & 2CCII-)	6R (3F+3G)	-	2FC (2G)	SIMO	FO-KHN (FLPF)	Voltage/Voltage	High
	3 CCII+	4R (4G)	-	2FC (2G)	SIMO	FO-TT (FLPF)	Voltage/Voltage	High
[94]	3 Op-Amps	6R (6F)	-	2FC (2F)	SIMO	FO-KHN (FLPF, FBPF, FHPF)	Voltage/Voltage	Low
	1 Op-Amp	4R (3F+1G)	-	2FC (1F+1G)	SISO	FO Sallen-Key	Voltage/Voltage	Low
[95]	5 CCII (3CCII+ & 2CCII-)	7R (3F+4G)	-	2FC (2G)	SIMO	FO-KHN (FLPF, FBPF, FHPF)	Voltage/Voltage	High
[96]	2 Op-Amps	4R (3F+1G)	1C (1F)	-	SISO	FBPF	Voltage/Voltage	Low
	2 Op-Amps	3R (2F+1G)	1C (1F)	1FC (1F)	SISO	FBPF	Voltage/Voltage	Low
[97]	3 Op-Amps	6R (6F)	-	2FC (2F)	SIMO	FO-KHN (FLPF, FBPF, FHPF)	Voltage/Voltage	Low
	1 Op-Amp	4R (3F+1G)	-	2FC (1F+1G)	SISO	FO Sallen-Key	Voltage/Voltage	Low
[98]	3 Op-Amps	6R (6F)	1C (1F)	1FC (1F)	SISO	FO-TT (FLPF)	Voltage/Voltage	Low

continued on page no 16

Table 1.2(b) (continued)

Ref.	ABB No. Type	Passive Elements			FOF Type	FOF Response(s)	Input/Output	Impedance
		R	C	FC				
[99]	5 DDCC	7R (7G)	3C (3G)	-	SISO	FLPF	Voltage/Voltage	High
[100]	2 Op-Amps	3R (2F+1G)	1C (1F)	1FC (1F)	SISO	FBPF, FNF	Voltage/Voltage	Low
[101]	7 OTAs	-	2C (2G)	-	SISO	FLPF, FHPF, FAPF (α)	Voltage/Voltage	High
	11 OTAs	-	4C (4G)	-	SISO	FLPF, FHPF, FBPF, FBSF (α+β)	Voltage/Voltage	High
[102]	3 OTAs + 3 ACAs + 1 CF	-	3C (3G)	-	SISO	FLPF, FHPF (1+α)	Current/Current	High
[103]	3 OTAs	-	-	2FC (2F)	SIMO	FLPF, FBPF (0.5, 0.9)	Current/Current	High
[104]	2 OTAs	-	-	1FC (1F)	SISO	FAPF	Voltage/Voltage	High
[105]	1 CDBA	5R (4F+1G)	-	5FC (4F+1G)	MISO	FLPF, FHPF, FBPF	Voltage/Voltage	Low
[106]	1 CCII+	1R (1G)	-	1FC (1G)	SISO	Current Integrator	Current/Current	High
[107]	3 OTAs	-	-	2FC* (2G)	SIMO	FLPF, FBPF, FHPF	Current/Current	High
[41]	3 VDTAs	7R (3F+4G)	3C (3G)	-	SISO	FBPF (1+α)	Current/Current	High
	4 VDTAs	11R (4F+7G)	3C (3G)	-	SISO	FBRF (1+α)	Current/Current	High

continued on page no 17

Table 1.2(b) (continued)

Ref.	ABB No. Type	Passive Elements			FOF Type	FOF Response(s)	Input/Output	Impedance
		R	C	FC				
[42]	3 VDTAs	7R (3F+4G)	3C (3G)	-	SISO	FLPF (1+α)	Current/Current	High
	4 VDTAs	10R (3F+7G)	3C (3G)	-	SISO	FHPF (1+α)	Current/Current	High
[108]	1 OTRA	4R (4F)	-	4FC (4F)	SISO	FHPF (α+β+γ)	Voltage/Voltage	Low

It may be observed from Table 1.2(a) that

- limited SISO [14] and MIMO [11] type biquads are available
- Ref. [15-30] exhibit SIMO behaviour and MISO type biquads are presented in [18,24,27,31-40]
- structures of [16-18,20,21,24,27,28,30,32,35-37] are designed around large number of active blocks.

Further, inspection of Table 1.2(b) suggests that

- the FOF of [99,101,102,41,42] are designed using the FBD approach while FOEs are employed for obtaining desired functionality in [87-98,100,103-107,108]
- only FCs are employed in [88,90,91,96,100] whereas both capacitors and FCs are used in [87,94,96,97] to obtain desired FO responses
- all structures use large number of ABB except for [105,106,108] and large number of passive components except for [103,104,106,107]
- Ref. [87-101,104,105,108] provide voltage output and [102,103,106,107] are current output circuits
- voltage output is available at high impedance [93,95,99,101,104] thus require a buffer circuit for cascading.

1.2.3 Sinusoidal Oscillators

Sinusoidal oscillators (SOs) are linear electric/electronic circuits and are widely used in various applications pertaining to telecommunications, control systems, signal processing and measurement systems. Based on the order, VDTA based sinusoidal oscillators may be broadly classified as second- and third- order sinusoidal oscillators (TOSOs).

A comparative study for various voltage differencing transconductance amplifier based oscillators [44-53] has been recorded in Table 1.3 for ready reference.

Table 1.3 Literature Summary for VDTA based Sinusoidal Oscillators.

Ref.	ABB No. Type	Passive Elements		Output Type	Order
		R	C		
[44]	1 VDTA	1 (G)	2 (G)	Voltage	Second
[45]	2 VDTAs	0	2 (G)	Current	Second
[46]	1 DDCC + 1 VDTA	1 (G)	3 (G)	Current	Third
[47]	2 VDTAs	0	2 (G)	Voltage	Second
	2 VDTAs	0	2 (G)	Current	Second
[48]	2 VDTAs	0	3 (G)	Current	Third
[49]	2 VDTAs	0	3 (G)	Voltage	Third
	2 VDTAs	0	3 (G)	Current	Third
[50]	2 VDTAs	1 (G)	2 (G)	Voltage	Second
[51]	1 VDTA	0	2 (G)	Voltage	Second
	1 VDTA	0	2 (G)	Current	Second
[52]	1 VDTA	2 (G)	2 (G)	Voltage	Second
[53]	1 VDTA	1 (G)	2 (G)	Current	Second

Based on the inferences made from Table 1.3, it can be drawn that:

- there is lean presence of TOSOs [46,48,49]
- explored TOSOs are designed around two active blocks; either combination of blocks [46] or both VDTAs [48,49]
- the TOSO proposition makes use of single VDTA only
- the proposed structure employs canonical number of grounded capacitors.

1.2.4 VDTA Implementations

It is well known that, transconductance amplifier (TA) with high transconductance gain 'g_m' is essential for designing high performance analog circuits. Most traditionally the g_m can be enhanced by increasing the bias current of the TA stage. However, increased bias current essentially leads to large power dissipation leading to a trade-off between the transconductance gain and the power dissipation. Extensive review suggests that all available CMOS based VDTA implementations [11,15,18,27,110-112] increase the bias current for enhancing the g_m of the TA stages. Thus, it may be summarized that the available VDTA structures do not provide characteristics like low power and high transconductance gain simultaneously. A comparative study of various performance parameters of all available CMOS based VDTA implementations [11,15,18,27,110-112] is given in Table 1.4.

Table 1.4 Literature Summary for VDTA CMOS Implementations.

Ref.	Technology (µm)	Power Supply (V)	No. of Current Sources (Value)	Input Voltage Range (mV)	Transconductance (µS)	BW (MHz)	Power Consumption
[11]	0.18	± 0.9	4 (150 µA)	± 300	636	NA*	NA
[15]	0.35	± 2	2 (40 µA)	NA*	381	NA*	1 mW
[18]	0.18	± 1.5	4 (40 µA)	NA*	150	NA*	NA
[110]	0.045	± 1	-	NA*	NA*	NA*	0.184 mW
[27]	0.18	± 0.7	4 (10 µA)	-80 to 80	415	225	145 µW
[111]	0.18	± 1.8	NA* (Voltage sources for biasing)	NA*	NA*	NA	NA*
[112]	0.25	± 2	8 (70 µA)	± 125	1300	145	NA*

1.3 Research Gaps

Comprehensive literature review suggests that designing and development of FO circuits and systems is still in nascent stage. For designing fractional order circuits FOEs are essential elements. No significant work has been reported in fractional order inductance emulation using VDTA though, other ABBs based designs have been explored. Further, only two topologies are available which can emulate both negative and positive fractional order inductance. Additionally, no structure is existing which provides both integer and fractional order behaviour using a single structure.

Survey on VDTA based integer order filter suggested that only a single structure providing multimode biquad responses is existing. Further, exploring the domain of fractional order filters, it is clearly observed that limited literature is available on VDTA based FOFs. Only three structures are reported [41-43] which make use of large number of active blocks and are the structures are making use of resistive components.

Yet, another research gap that is observed is the lean presence of VDTA based third order sinusoidal oscillators in literature. It is further explored that existing structures are designed around two active blocks. Additionally, only single configuration is reported which provides voltage output.

Exploring further, it is observed that several CMOS VDTA implementations are available in literature; however, scope is always there to enhance its performance parameters namely linearity, transconductance gain, bandwidth etc.

1.4 Research Objectives

Based on the literature survey and research gaps following objectives were formulated:

1) To develop VDTA based generic impedance emulation topology to provide both positive and negative fractional and integer order behaviour.
2) To develop VDTA based integer and fractional order filter topologies.
3) To develop higher order signal generation applications.
4) To design a new VDTA structures with improved performance.

1.5 Organization of the Thesis

The primary objective of this research is on VDTA based conventional integer order and state of the art fractional order circuits for analog signal processing (ASP) and signal generation. The organization of the research work carried out is presented in a chapter-wise format and is as follows:

Chapter 1

This chapter briefs about the background and motivation behind the work carried out in the thesis. Literature review and summary of available analog circuits and/or their fractional order counterparts is put up followed by locating the research gaps to formulating the objectives for the work. The layout of the thesis is described shortly.

Chapter 2

This chapter presents a brief description of fractional order element implementation using Carlson and continued fraction expansion approximations. It also includes characterization of active block used i.e., Voltage Differencing Transconductance Amplifier to develop different analog circuits in the thesis.

Chapter 3

This chapter presents generic impedance emulator with lesser component count which can be configured as (i) integer order positive inductance emulator (ii) integer order negative inductance emulator (iii) fractional order positive inductance emulator and (iv) fractional order negative inductance emulator. Functional validation of the proposition is carried out through simulations as well as experimentally. Further, the applicability of the proposed structure is justified through two application examples namely parasitic fractional order inductance cancellation and fractional order high pass filter.

Chapter 4

This chapter presents an classical analog filter and two α-order voltage mode fractional order filters based on VDTA. Moving on to the fractional order counterparts, first FOF represents voltage mode multiple input single output universal configuration and is based on Carlson approximation. Whereas, second FOF topology presents voltage mode single input single output structure.

Chapter 5

This chapter is devoted to signal generating circuits [i.e. sinusoidal oscillators (particularly, third order SOs)]. A generic TOSO is proposed first followed by two configurations extracted from it by suitably selecting the impedances connected.

Chapter 6

Two transconductance boosted VDTA structures are presented in this chapter. General schemes of the two propositions are discussed, firstly, followed by their CMOS implementations.

Chapter 7

Based on the roadmap outlined above, the work is concluded in **Chapter 7** with a thought on the prospective future scope.

CHAPTER – 2

PRELIMINARIES

2.1 Introduction

Researchers are continuously striving to explore different analog building blocks with attributes like higher bandwidth, higher slew rate, lower power consumption and better linearity. This has led to paradigm shift from voltage mode to current mode signal processing. Hence, numerous current mode active blocks as given in [3] has evolved and references cited therein. The voltage differencing transconductance amplifier (VDTA) is one among those and its CMOS implementation was first proposed by Yesil et al. [11]. Since then, various research efforts are made to propose CMOS implementations [11,15,18,27,110-112] of VDTA with enhanced performance. The VDTA is a voltage input current output ABB having two transconductance gain stages which helps in realization of resistor-less compact CMOS applications. Additionally, the transconductances of VDTA can be tuned through bias current which facilitates electronic tunability of the system parameters. It is well known that, transconductance amplifier (TA) with high transconductance gain 'g_m' is essential for designing high performance analog circuits. Thus, VDTA is a preferred choice for designing on-chip high frequency applications. This has led to realization of various signal processing [12-43] and generation [44-53] applications using VDTA.

The FOE is a fundamental component for designing the fractional order circuits. It is observed from literature that though the efforts are being directed towards physical realization of FC yet these are still in very primitive stage [57-59] and the reported off the shelf FCs are bulky and non-reconfigurable to be used in circuits. On the other hand, various rational approximations [60-68] such as Carlson approximation [60,62,64], Oustaloup recursive approximation [61,62,64], continued fraction expansion (CFE) [62], Matsuda approximation [62,64], Chareff method [62], Modified approximation [63], Halley approximation [65,67], El-Khazali approximation [66] and Laguerre approximation [68] are available to emulate the behaviour of FOE.

This thesis presents realization of integer and fractional order signal processing and generating circuits using VDTA, therefore in this Chapter preliminaries of VDTA and fractional order elements has been presented.

2.2 The VDTA

The VDTA can be modelled as a differential voltage driven current output ABB with two transconductance (TC) gain stages where 'g_{mF}' and 'g_{mS}' represent the transconductance gains of the first and second stages, respectively. The port relations of VDTA are expressed using matrix Eqn. (2.1); that is, two high impedance voltage input terminals 'p' and 'n' and three high impedance current output terminals 'z', 'x+' and 'x-'. The circuit symbol and equivalent model of the VDTA [3] are shown in Fig. 2.1 (a) and (b) respectively.

$$\begin{bmatrix} I_z \\ I_{z-} \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 & 0 \\ -g_{mS} & g_{mS} & 0 & 0 \\ 0 & 0 & g_{mS} & 0 \\ 0 & 0 & -g_{mS} & 0 \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \\ V_{z-} \end{bmatrix} \tag{2.1}$$

The fully differential - flipped voltage follower (FD-FVF) based CMOS structure of VDTA which is used in this work for verification of all propositions, is shown in Fig. 2.1(c). Two dual output OTAs (DO-OTAs) have been used to realize this structure wherein MOSFETs M_1-M_{10}, M_{21} and M_{22} constitute first dual output OTA and M_{11}-M_{20}, M_{23} and M_{24} constitute second dual output OTA.

The transconductance gain of each stage ($g_{mF,}$ g_{mS}) is given by

$$g_{mF,\mathrm{mS}} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{B_{F,S}}} \tag{2.2}$$

where μ_n, C_{ox}, W and L denote the carrier mobility (effective), gate-oxide capacitance (per unit area), effective channel width and length of MOS transistor of differential pair respectively and $I_{BF,BS}$ represent the bias current of the respective transconductance stages.

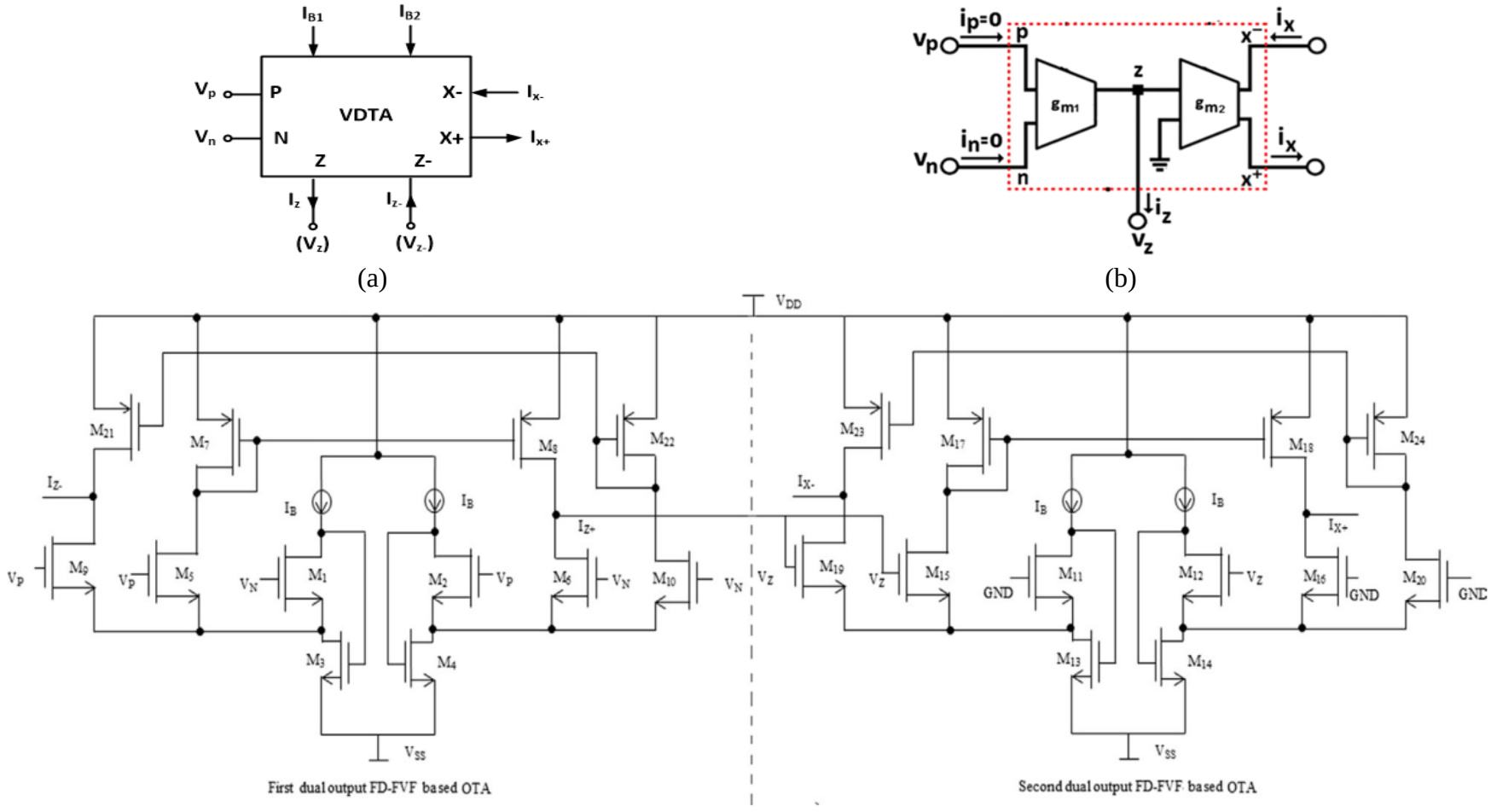


Fig. 2.1 VDTA (a) Symbol (b) Equivalent Model (c) CMOS Implementation [27].

2.2.1 Simulation Results

The functionality of the reproduced CMOS VDTA [27] shown in Fig. 2.1(c), which is used in this work for all proposed realizations, is validated through simulations. Simulations are carried out using Virtuoso from Cadence tool suite using 180 nm generic process design kit (gpdk) CMOS technology parameters. Device dimensions (W/L) are taken as 7.2µm/0.36µm for NMOS, 14.4µm/0.36µm for PMOS transistors and supply voltage of ±0.7 V is used for simulations. The DC characteristics of the VDTA for different values of biasing currents are depicted in Fig. 2.2. Dependence of the transconductance on the biasing current and the supply voltage is illustrated in Fig. 2.3 (a) and (b) respectively. The value of transconductance ($g_{mF} = g_{mS}$) is found to be 400 uA/V for the biasing current and supply voltage of 10 µA and ±0.7 V. Further, from the Fig. 2.2, the linear range is measured to be -150 mV to 150 mV.

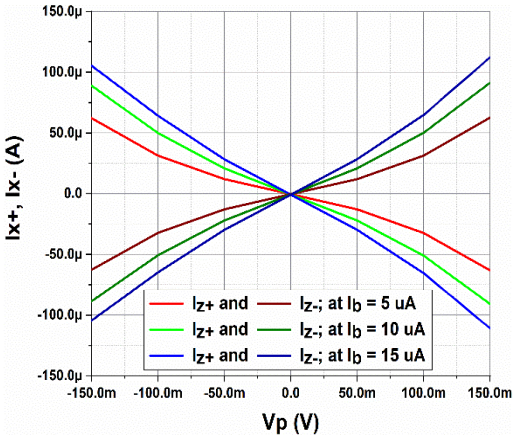
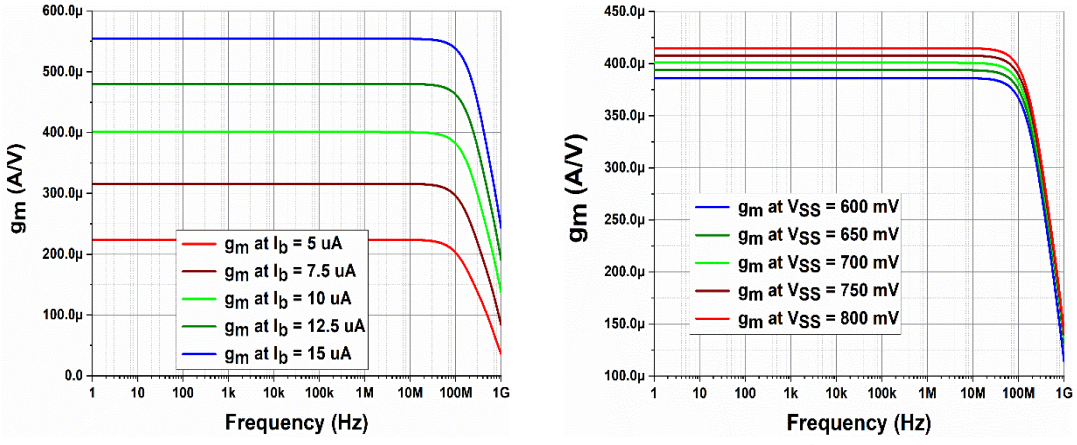


Fig. 2.2 DC Transfer Characteristics of VDTA.



(a) (b)

Fig. 2.3 Transconductance Variation with (a) Bias Current (b) Supply Voltage.

2.3 FC Realization

Comprehensive literature review suggests that various research efforts have been made to perceive a fractional order capacitor. As of now, there are two design techniques to implement:

- Fabrication (i.e. single-component realization) [57-59]
- Emulation (i.e. multi-component realization) [60-68]

The FCs are not commercially available and their physical realization is still in primitive phase [57-59]. However, a number of rational approximations; namely, Carlson approximation [60,62,64], Oustaloup recursive approximation [61,62,64], continued fraction expansion (CFE) [62], Matsuda approximation [62,64], Chareff method [62], Modified approximation [63], Halley approximation [65,67], El-Khazali approximation [66] and Laguerre approximation [68] are available in literature for FOE behaviour emulation.

In this work, Carlson and CFE approximations are used, therefore both these methods have been presented in following subsections.

2.3.1 FC Realization using Carlson Method

Based on the Carlson method, rational integer order approximation function obtained after first iteration for $\alpha = 0.5$ is

$$C^{\alpha}_{1/2\_1st} = \frac{s+3}{3s+1} \tag{2.3}$$

Similarly, post second iteration rational approximation obtained is

$$C^{\alpha}_{1/2\_2nd} = \frac{s^4+36s^3+126s^2+84s+9}{9s^4+84s^3+126s^2+36s+1} \tag{2.4}$$

Likewise, rational approximation obtained after third iteration is

$$C^{\alpha}_{1/2\_3\text{rd}} = \frac{\begin{array}{l} s^{13}+351s^{12}+17550s^{11}+296010s^{10}+2220075s^{9} \\ +8436285s^{8}+17383860s^{7}+20058300s^{6}+13037895s^{5} \\ +4686825s^{4}+888030s^{3}+80730s^{2}+2925s+27 \end{array}}{\begin{array}{l} 27s^{13}+2925s^{12}+80730s^{11}+888030s^{10}+4686825s^{9} \\ +13037895s^{8}+20058300s^{7}+17383860s^{6}+8436285s^{5} \\ +2220075s^{4}+296010s^{3}+17550s^{2}+351s+1 \end{array}} \tag{2.5}$$

It may be observed from Eqn. (2.3) through Eqn. (2.5) that the Carlson based first, second and third iterations result in first, fourth and thirteenth order rational approximation functions respectively. These integer order approximation functions may be used to implement the FC as the impedance of FC is expressed as $Z(s) = 1/Ks^{\alpha}$. The impedance function can be implemented using RC ladder network of Fig. 2.4 thereby emulating the FC. The component values for ladder networks for three iterations are listed in Table 2.1.

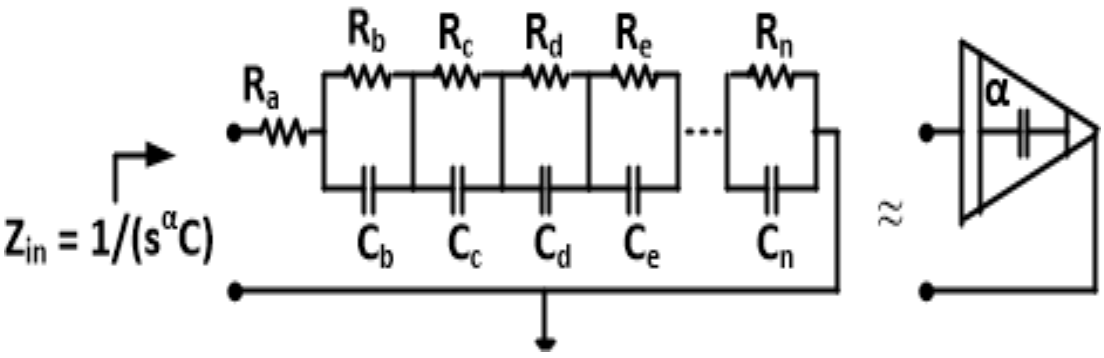


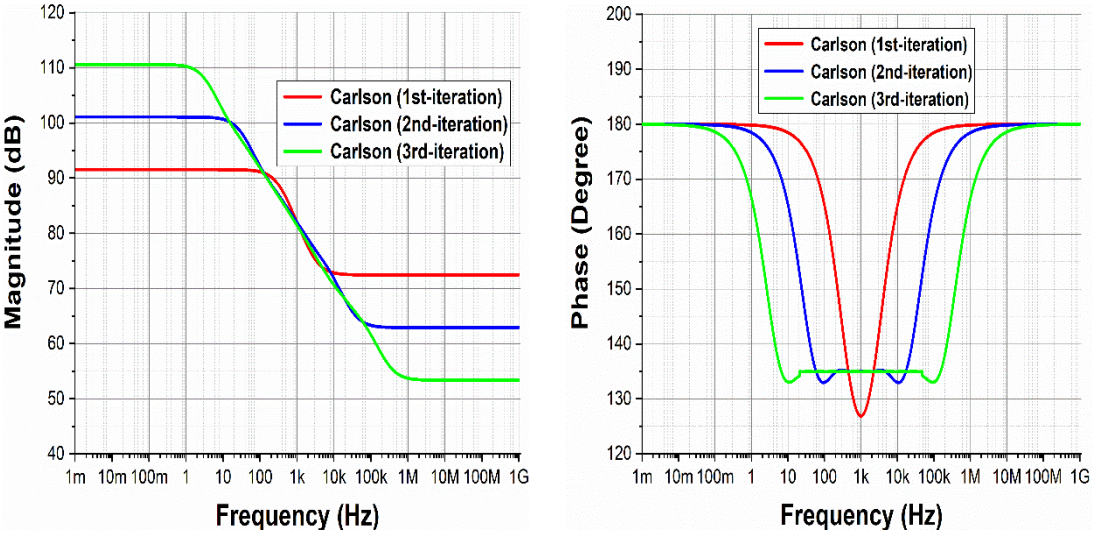
Fig. 2.4 Truncated n^{th} order RC Ladder Circuit.

Table 2.1 Component Values for Carlson based RC Ladder Network with Centre Frequency 1 kHz for FC = 1 μ℧/s^{α}.

	R_a (kΩ)	R_b (kΩ), C_b (nF)	R_c (kΩ), C_c (nF)	R_d (kΩ), C_d (nF)	R_e (kΩ), C_e (nF)	R_f (kΩ), C_f (nF)	R_g (kΩ), C_g (nF)	R_h (kΩ), C_h (nF)	R_i (kΩ), C_i (nF)	R_j (kΩ), C_j (nF)	R_k (kΩ), C_k (nF)	R_l (kΩ), C_l (nF)	R_m (kΩ), C_m(nF)	R_n (kΩ), C_n (nF)
First Iteration	4.21	33.64 14.19	-	-	-	-	-	-	-	-	-	-	-	-
Second Iteration	1.40	3.17 6.64	4.78 23.46	11.21 42.58	92.97 55.06	-	-	-	-	-	-	-	-	-
Third Iteration	0.47	0.95 2.30	0.99 9.06	1.06 19.92	1.17 34.30	1.34 51.43	1.59 70.37	1.98 90.11	2.62 109.58	3.74 127.73	5.96 143.59	11.36 156.30	30.99 165.18	276.41 169.74

2.3.1.1 Simulation Results

It may be observed from Fig. 2.5 that the simulated magnitude and phase values match with ideal values over a larger frequency range as the order of the approximation function is increased. Hence, it can be concluded that, larger the number of iterations, higher is the order of the approximation function and hence better is the performance of the FC.



(a) (b)

Fig. 2.5 Frequency Response for FC of 1 μ℧/s^{α} (a) Magnitude (b) Phase.

2.3.2 The Continued Fraction Expansion Method

The Continued fraction expansion [62] of $(1+x)^{\alpha}$ is given by

$$(1+x)^{\alpha} = \frac{1}{1-}\frac{\alpha x}{1+}\frac{(1+\alpha)x}{2+}\frac{(1-\alpha)x}{3+}\frac{(2+\alpha)x}{2+}\frac{(2-\alpha)x}{5+} \tag{2.6}$$

which has infinite terms. Substituting $x = s - 1$ and retaining only 'n' finite terms the generalized rational approximation for s^{α} can be obtained as

$$s^{\alpha} \cong \frac{a_n s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + a_0}{a_0 s^n + a_1 s^{n-1} + \ldots + a_{n-1} s + a_n} \tag{2.7}$$

where, n is the order of the approximation.

Considering finite number of terms in Eqn. (2.7), the rational approximations of different orders may be obtained for s^{α}. In this work, different orders for s^{α} (α ranging from 0.1 to 0.9 in steps of 0.1) are listed in Table 2.2. It is evident from the Table 2.2 that the order of the approximated transfer function obtained is dependent on the order of the approximation, that is, CFE based n^{th}-order approximation leads to an n^{th}-order transfer function.

Table 2.2 CFE based Approximated Transfer Functions.

	1st-order Approximation	**2nd-order Approximation**	**3rd-order Approximation**	**4th-order Approximation**
α = 0.1	$\frac{9s+11}{11s+9}$	$\frac{57s^2+266s+77}{77s^2+266s+57}$	$\frac{1653s^3+17081s^2+18879s+2387}{2387s^3+18879s^2+17081s+1653}$	$\frac{64467s^4+1174732s^3+2875002s^2+1387932s+97867}{97867s^4+1387932s^3+2875002s^2+1174732s+64467}$
α = 0.2	$\frac{2s+3}{3s+2}$	$\frac{6s^2+33s+11}{11s^2+33s+6}$	$\frac{21s^3+252s^2+308s+44}{44s^3+308s^2+252s+21}$	$\frac{57s^4+1197s^3+3192s^2+1672s+132}{132s^4+1672s^3+3192s^2+1197s+57}$
α = 0.3	$\frac{7s+13}{13s+7}$	$\frac{119s^2+782s+299}{299s^2+782s+119}$	$\frac{1071s^3+15147s^2+20493s+3289}{3289s^3+20493s^2+15147s+1071}$	$\frac{39627s^4+973692s^3+2835162s^2+1610092s+141427}{141427s^4+1610092s^3+2835162s^2+973692s+39627}$
α = 0.4	$\frac{3s+7}{7s+3}$	$\frac{2s^2+16s+7}{7s^2+16s+2}$	$\frac{26s^3+442s^2+663s+119}{119s^3+663s^2+442s+26}$	$\frac{234s^4+6864s^3+21879s^2+13464s+1309}{1309s^4+13464s^3+21879s^2+6864s+234}$
α = 0.5	$\frac{s+3}{3s+1}$	$\frac{s^2+10s+5}{5s^2+10s+1}$	$\frac{s^3+21s^2+35s+7}{7s^3+35s^2+21s+1}$	$\frac{s^4+36s^3+126s^2+84s+9}{9s^4+84s^3+126s^2+36s+1}$
α = 0.6	$\frac{s+4}{4s+1}$	$\frac{7s^2+91s+52}{52s^2+91s+7}$	$\frac{7s^3+189s^2+351s+78}{78s^3+351s^2+189s+7}$	$\frac{119s^4+5474s^3+21114s^2+15249s+1794}{1794s^4+15249s^3+21114s^2+5474s+119}$
α = 0.7	$\frac{3s+17}{17s+3}$	$\frac{13s^2+234s+153}{153s^2+234s+13}$	$\frac{299s^3+11063s^2+22977s+5661}{5661s^3+22977s^2+11063s+299}$	$\frac{9867s^4+618332s^3+2639802s^2+2065932s+266067}{266067s^4+2065932s^3+2639802s^2+618332s+9867}$
α = 0.8	$\frac{s+9}{9s+1}$	$\frac{s^2+28s+21}{21s^2+28s+1}$	$\frac{11s^3+627s^2+1463s+399}{399s^3+1463s^2+627s+11}$	$\frac{22s^4+2112s^3+10032s^2+8512s+1197}{1197s^4+8512s^3+10032s^2+2112s+22}$
α = 0.9	$\frac{s+19}{19s+1}$	$\frac{11s^2+638s+551}{551s^2+638s+11}$	$\frac{77s^3+9009s^2+23751s+7163}{7163s^3+23751s^2+9009s+77}$	$\frac{341s^4+66836s^3+355446s^2+327236s+50141}{50141s^4+327236s^3+355446s^2+66836s+341}$

2.3.2 FC Realization using CFE Method

The CFE for s^{α} presented in Table 2.2 can be used for emulating the FC. The impedance of FC is expressed as $Z(s) = K/s^{\alpha}$ so by substituting s^{α} from Eqn. (2.7) the impedance and admittance of FC using n^{th}-order approximated functions can be respectively be expressed as

$$Z(s) = \frac{1}{C}.\frac{a_0 s^n + a_1 s^{n-1} + ... + a_{n-1} s + a_n}{a_n s^n + a_{n-1} s^{n-1} + ... + a_1 s + a_0} \tag{2.8a}$$

$$Y(s) = C.\frac{a_n s^n + a_{n-1} s^{n-1} + ... + a_1 s + a_0}{a_0 s^n + a_1 s^{n-1} + ... + a_{n-1} s + a_n} \tag{2.8b}$$

The impedance/admittance functions of Eqn. (2.8) can be implemented using well known Foster and Cauer realizations. Thus, the resulting networks will emulate the behaviour of FCs of different orders. This work makes use of FC realization using Foster form I which uses impedance function of Eqn. (2.8a) and can be realized through RC ladder network depicted in Fig. 2.4.

Routine network analysis of Fig. 2.4 yields the impedance function represented by the following Eqn. (2.9)

$$Z(s) = R_a + \sum_{i=1}^{n} \frac{1/C_i}{s + 1/R_i C_i} \tag{2.9}$$

The component values for the arrangement of Fig. 2.4 can be computed by comparing the coefficients of Eqn. (2.8a) and Eqn. (2.9). The RC component values of Foster form I are computed using a MATLAB code for FC (order $\alpha = 0.1$ to 0.9 in steps of 0.1) for first- to fourth- order CFE approximations. It is worth noting that these approximations have been done at center frequency of 1 rad/sec, and thus the FC gives satisfactory performance near 1 rad/sec. Frequency scaling needs to be done to shift the center frequency. To shift frequency from 1 rad/sec to n rad/sec, the

s needs to be replaced by s/n on both side of the impedance function. The component values obtained around 1 rad/sec are not practically realizable and therefore scaling is done as per following relation:

$$R^{'} = RK_m \tag{2.10a}$$

$$C^{'} = \frac{C}{K_f K_m} \tag{2.10b}$$

where K_m and $K_f = \omega^{\alpha}$ are the desired magnitude and scaling factors respectively [62] and $R^{'}$ and $C^{'}$ are post scaled values. Post-scaling component values for RC ladder obtained from first- to fourth- order approximation functions, for FC of value 1 μ℧/s^{α} with a centre frequency of 1 kHz for order α = 0.1 to 0.9 are summarized in Table 2.3.

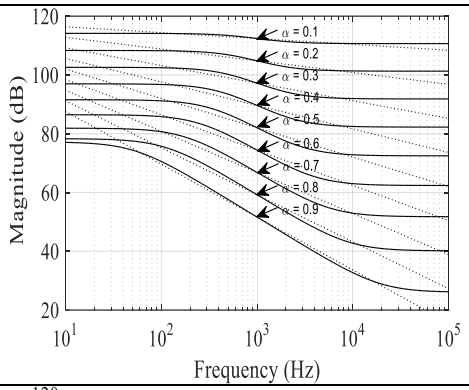
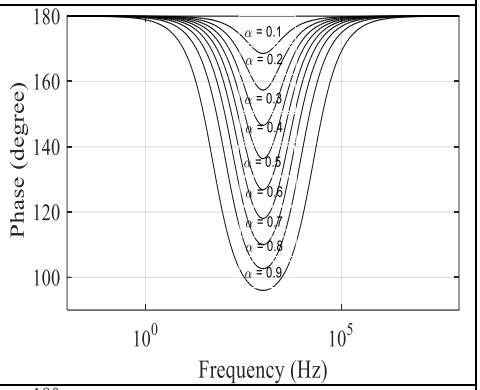
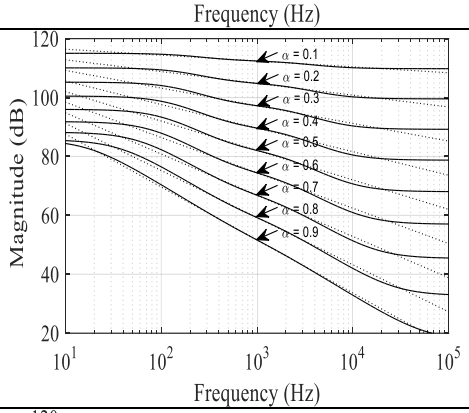
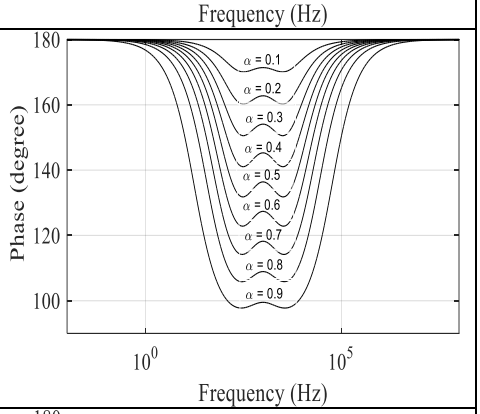
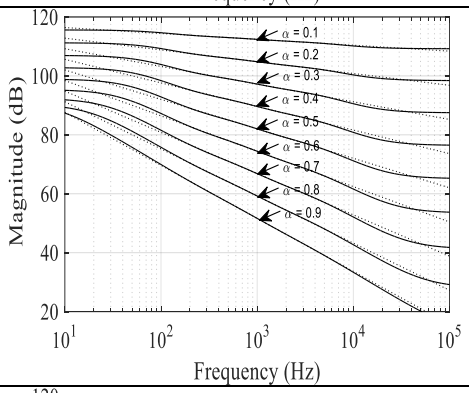
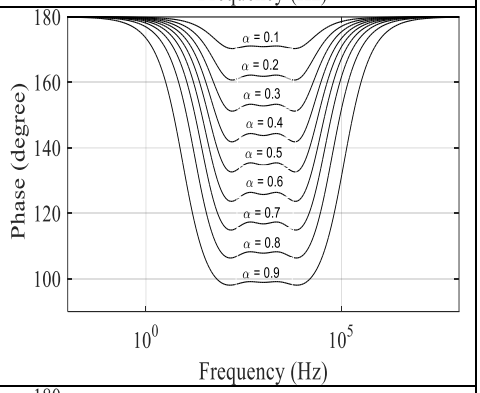
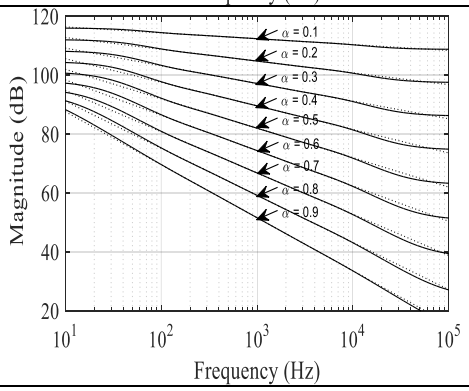
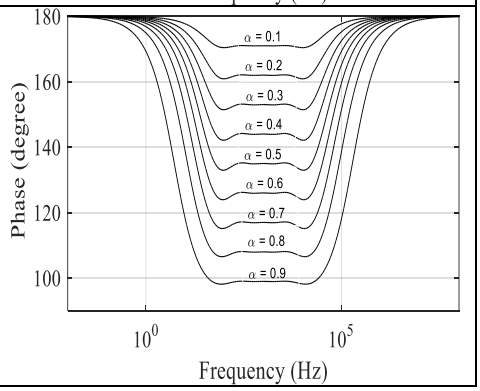
Table 2.3 Component Values for CFE based RC Ladder Network with Centre Frequency 1 kHz for FC = 1 μ℧/s^{α}.

1st-Order Approximation									
	α = 0.1	**α = 0.2**	**α = 0.3**	**α = 0.4**	**α = 0.5**	**α = 0.6**	**α = 0.7**	**α = 0.8**	**α = 0.9**
R_a (kΩ)	341.22	115.95	39.06	12.96	4.21	1.32	0.39	0.10	0.02
R_b (kΩ)	168.50	144.94	95.65	57.62	33.64	19.73	12.05	8.13	7.23
C_b (nF)	1.15	1.65	3.09	6.45	14.19	32.27	74.87	176.10	418.20
2nd-Order Approximation									
	α = 0.1	**α = 0.2**	**α = 0.3**	**α = 0.4**	**α = 0.5**	**α = 0.6**	**α = 0.7**	**α = 0.8**	**α = 0.9**
R_a (kΩ)	308.72	94.87	28.87	8.64	2.52	0.71	0.19	0.04	0.01
R_b (kΩ)	105.41	74.15	38.99	18.06	7.71	3.07	1.12	0.36	0.09
R_c (kΩ)	149.24	149.84	114.39	79.17	52.85	35.31	24.51	18.81	19.02
C_b (nF)	0.47	0.77	1.66	4.09	10.90	31.08	96.14	337.76	1590.19
C_c (nF)	4.65	5.46	8.58	15.15	28.53	55.90	112.46	230.39	477.98
3rd-Order Approximation									
	α = 0.1	**α = 0.2**	**α = 0.3**	**α = 0.4**	**α = 0.5**	**α = 0.6**	**α = 0.7**	**α = 0.8**	**α = 0.9**
R_a (kΩ)	288.80	83.01	23.62	6.61	1.80	0.47	0.12	0.03	0.00
R_b (kΩ)	89.51	57.54	27.53	11.55	4.44	1.58	0.51	0.15	0.03
R_c (kΩ)	73.68	60.28	36.44	19.22	9.27	4.14	1.70	0.61	0.16
R_d (kΩ)	150.24	163.58	135.16	101.07	72.79	52.43	39.22	32.41	35.30
C_b (nF)	0.26	0.46	1.07	2.87	8.31	25.95	88.32	343.64	1805.88
C_c (nF)	2.36	3.16	5.71	11.86	26.99	66.47	179.04	551.81	2293.43
C_d (nF)	9.63	10.35	14.90	24.19	41.97	75.92	141.26	267.98	515.32
4th-Order Approximation									
	α = 0.1	**α = 0.2**	**α = 0.3**	**α = 0.4**	**α = 0.5**	**α = 0.6**	**α = 0.7**	**α = 0.8**	**α = 0.9**
R_a (kΩ)	274.72	75.10	20.32	5.41	1.40	0.35	0.08	0.02	0.00
R_b (kΩ)	81.86	49.60	22.34	8.81	3.17	1.06	0.32	0.08	0.02
R_c (kΩ)	56.13	41.99	23.09	11.02	4.78	1.90	0.69	0.22	0.05
R_d (kΩ)	66.30	58.64	38.21	21.67	11.21	5.36	2.35	0. 90	0.26
R_e (kΩ)	154.10	177.44	154.90	122.32	92.97	70.65	55.73	48.57	55.79
C_b (nF)	0.17	0.31	0.77	2.16	6.64	21.99	79.51	329.30	1846.09
C_c (nF)	1.50	2.16	4.22	9.48	23.46	63.16	187.20	639.51	2972.23
C_d (nF)	5.25	6.40	10.62	20.29	42.58	97.00	242.33	694.26	2687.45
C_e (nF)	15.93	16.12	21.89	33.56	55.06	94.24	165.99	298.30	543.61

2.3.2.1 Simulation Results

It is clear from preceding discussions that the truncated rational approximations just emulate the FC functionality and cannot portray the ideal behaviour. Thus, the accuracy of these approximated FCs is examined through Virtuoso in this subsection. The magnitude and phase behavior of FC of value 1 μ℧/s^{α} with a centre frequency of 1 kHz realized using first, second, third and fourth orders of approximations for different values of α are shown in Table 2.4. The dotted curves represent the ideal behaviour and solid lines represent the simulated responses. Maximum and minimum values of the magnitude and the respective phases for the approximations thus obtained for the orders 'α' 0.1 through 0.9 are tabulated as in Table 2.5 and Table 2.6 respectively with a deviation of ±0.1 dB and ±0.3º for magnitude and phase responses respectively. It is worth noting that higher the order of the approximation function better is the performance of FC over a considerable range of frequency. However, it leads to both computation and circuit complexity.

Table 2.4 Frequency Responses for Approximated FC (1 μƱ/s$^{\alpha}$) based on CFE (a) Magnitude (b) Phase.

Approx Order	Magnitude	Phase
1		
2		
3		
4		

Post scaling, frequency range of operation and phase readings of the emulated FC of value 1 $\mu\text{Ʊ}/s^{\alpha}$ based on the CFE first- to fourth- order approximation for fractional orders 0.1 through 0.9 at the centre frequency of 1 kHz have been recorded in the Table 2.5 and Table 2.6 with a deviation of ± 0.1 dB and ±0.3º for magnitude and phase responses respectively.

Table 2.5 Post-Scaling Frequency Range of Operation of the CFE based Approximated FC.

	1st-order Approximation	**2nd-order Approximation**	**3rd-order Approximation**	**4th-order Approximation**
α = 0.1	169.68 Hz – 5.88 kHz	52.69 Hz – 19.01 kHz	25.94 Hz – 38.58 kHz	15.44 Hz – 64.54 kHz
α = 0.2	113.95 Hz – 8.80 kHz	35.49 Hz – 28.19 kHz	17.48 Hz – 57.26 kHz	10.42 Hz – 95.97 kHz
α = 0.3	85.96 Hz – 11.64 kHz	26.99 Hz – 37.07 kHz	13.31 Hz – 75.17 kHz	7.94 Hz – 125.93 kHz
α = 0.4	66.56 Hz – 15.03 kHz	21.12 Hz – 47.38 kHz	10.44 Hz – 95.86 kHz	6.23 Hz – 160.47 kHz
α = 0.5	51.20 Hz – 19.54 kHz	16.43 Hz – 60.90 kHz	8.14 Hz – 122.92 kHz	4.86 Hz – 205.52 kHz
α = 0.6	38.24 Hz – 26.17 kHz	12.41 Hz – 80.62 kHz	6.16 Hz – 162.31 kHz	3.69 Hz – 271.16 kHz
α = 0.7	26.95 Hz – 37.13 kHz	8.84 Hz – 113.21 kHz	4.40 Hz – 227.35 kHz	2.64 Hz – 379.25 kHz
α = 0.8	16.96 Hz – 58.99 kHz	5.61 Hz – 177.70 kHz	2.80 Hz – 357.35 kHz	1.68 Hz – 595.93 kHz
α = 0.9	8.03 Hz – 124.54 kHz	2.67 Hz – 374.23 kHz	1.34 Hz – 748.94 kHz	0.80 Hz – 1250 kHz

Table 2.6 Post-Scaling Frequency Range of Operation of the CFE based Approximated FC and the Corresponding Phase.

	Ideal	**1st-order Approximation**	**2nd-order Approximation**	**3rd-order Approximation**	**4th-order Approximation**
α = 0.1	171º	1 kHz	317.70 Hz – 3.19 kHz	162.63 Hz – 6.18 kHz	98.63 Hz – 10.17 kHz
α = 0.2	162º	1 kHz	313.55 Hz – 3.16 kHz	162.63 Hz – 6.21 kHz	97.95 Hz – 10.17 kHz
α = 0.3	153º	1 kHz	313.30 Hz – 3.19 kHz	162.63 Hz – 6.27 kHz	95.49 Hz – 10.30 kHz
α = 0.4	144º	1 kHz	309.70 Hz – 3.19 kHz	157.80 Hz – 6.42 kHz	95.72 Hz – 10.47 kHz
α = 0.5	135º	1 kHz	300.79 Hz – 3.27 kHz	155.20 Hz – 6.42 kHz	95.49 Hz – 10.62 kHz
α = 0.6	126º	1 kHz	300.79 Hz – 3.33 kHz	149.00 Hz – 6.58 kHz	92.74 Hz – 10.86 kHz
α = 0.7	117º	1 kHz	300.00 Hz – 3.40 kHz	148.30 Hz – 6.48 kHz	89.74 Hz – 11.10 kHz
α = 0.8	108º	1 kHz	286.40 Hz – 3.42 kHz	142.62 Hz – 6.95 kHz	87.10 Hz – 11.43 kHz
α = 0.9	99º	1 kHz	278.00 Hz – 3.62 kHz	136.51 Hz – 7.19 kHz	82.52 Hz – 11.91 kHz

It may be concluded from simulation results that for a given fractional order, with increasing the order of the approximation the frequency range of operation wherein the FC behaviour is emulated correctly gets enhanced. Moreover, by changing the fractional-order of the FC the slope can be tuned within this specific frequency range.

2.4 Conclusion

In this work, a systematic study of emulation of the FC based on the Carlson and the CFE approximations is presented. The workability of the realized FC is demonstrated through simulations using Cadence Virtuoso. With increasing the order of the approximation, the performance of the emulated FC improves. Workability of the propositions is verified through ADE spectre tool provided by Cadence Virtuoso using 180 nm CMOS technology parameters.

CHAPTER – 3

GENERIC INDUCTANCE EMULATOR

The content and results of the following publication are included in this chapter:

1. Parveen Rani and Rajeshwari Pandey, "VDTA based Unified Grounded Fractional/Integer order Negative/Positive Inductance Emulator", *Journal of Circuits, Systems and Computers*, vol. 32, no. 18, 2350303 (2023).

   DOI: https://doi.org/10.1142/S0218126623503036

   [SCIE, Impact Factor (1.5)]

3.1 Introduction

Inductors are an integral part of the electronic circuit design; however, designing an inductor on a chip has challenge in terms of the usage of space, weight, cost and tunability. Thus, it is desired to simulate an inductor using the active components available thereby saving in chip area. Further, to reap the advantages of fractional order processing; fractional order inductor (FI) realization is equally important. The fractional inductor in the range ($0 < \alpha < 1$) [69-76] can be emulated using various active RC methods similar to their integer order counter parts. These systematic methods include functional block diagram (FBD) approach and generalized impedance converter (GIC) based realization. Further, the FI can also be realized using direct intuitive methods which use different active blocks and few passive components. An exhaustive review suggests that though VDTA based integer order grounded inductance realizations are available [12,13] in literature but no fractional order inductors are in existence. A further exploration suggested that few realizations of FI [69-76] using ABBs other than VDTA are available. It is also observed that only single generic configuration is available to emulate inductance emulator. In this Chapter a generic grounded integer and fractional order positive/negative inductance emulator is presented.

3.2 Proposed Generic Inductance Emulator

The fractional order inductor in the range ($0 < \alpha < 1$) can be emulated using various active RC methods similar to their integer order counter parts. These systematic methods include impedance inverting circuit technique, functional block diagram approach and generalized impedance converter based realization. These methods use large number of active blocks for FI realization. Alternately, the FI can also be realized using direct intuitive methods as detailed in Chapter 1 and Chapter 2. The proposed VDTA based generic grounded integer and fractional order positive/negative inductance emulator is based on an intuitive approach and consists of a single VDTA and a grounded integer/fractional order capacitor only as shown in Fig. 3.1. The conventional integer order capacitor is represented by ‘C’ whereas ‘C^{α}’

denotes the fractional order capacitor. Appropriate switch position selections as specified in Table 3.1 lead to the following four configurations: (i) integer order positive inductance emulator, (ii) integer order negative inductance emulator, (iii) fractional order positive inductance emulator and (iv) fractional order negative inductance emulator. The switches can be implemented using MOS transistors with their gate voltages used for controlling the switch closure.

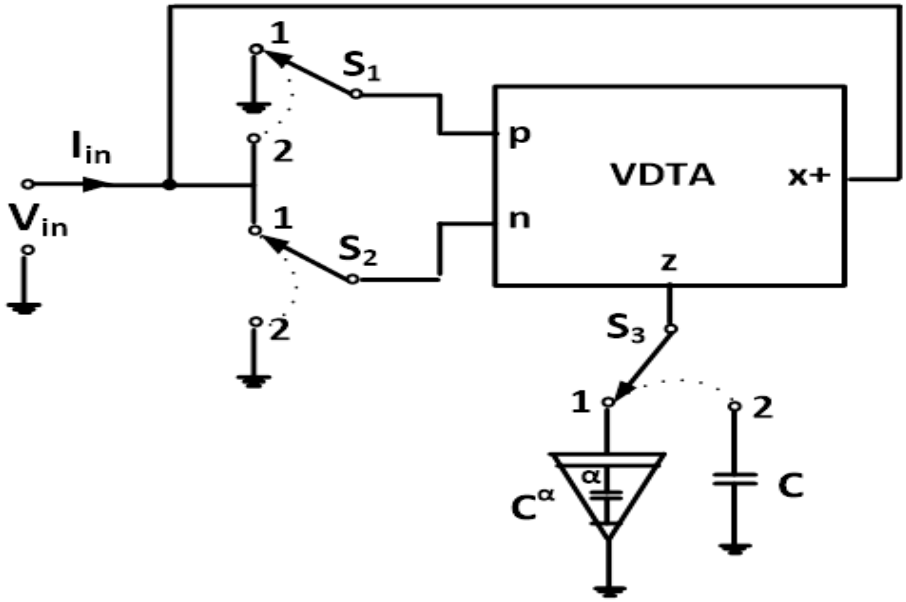


Fig. 3.1 Proposed Generic Inductance Emulator.

Table 3.1 Switch Settings for Emulator Selection.

Emulator Type	Switch 'S_1'	Switch 'S_2'	Switch 'S_3'
IO-PIE	1	1	2
IO-NIE	2	2	2
FO-PIE	1	1	1
FO-NIE	2	2	1

3.2.1 Integer order Inductance Emulator

Routine analysis of the proposition depicted in Fig. 3.1 for switch positions of row 1 and 2 of Table 3.1 yields the following classical integer order impedance functions

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \pm \frac{sC}{g_{mF} g_{mS}} \tag{3.1}$$

where the expressions with positive and negative signs represent the impedance function for integer order positive inductance emulator and integer order negative inductance emulator respectively.

3.2.2 Fractional order Inductance Emulator

Further, for switch positions listed in row 3 and 4 of Table 3.1 which represents the fractional order emulators, routine analysis of the proposed circuit yields the following impedance functions

$$Z_{in}^{\alpha}(s^{\alpha}) = \frac{V_{in}^{\alpha}(s^{\alpha})}{I_{in}^{\alpha}(s^{\alpha})} = \pm \frac{s^{\alpha} C^{\alpha}}{g_{mF} g_{mS}} \tag{3.2}$$

where positive and negative expressions represent the impedance function of the fractional order positive inductance emulator and fractional order negative inductance emulator respectively.

The magnitude and phase functions of integer order positive inductance emulator and integer order negative inductance emulator are derived using Eqn. (3.1) whereas those of fractional order positive inductance emulator and fractional order negative inductance emulator are obtained from Eqn. (3.2) and are tabulated in Table 3.2.

Table 3.2 Impedance Functions of Integer and Fractional Order Positive/Negative Inductance Emulators.

	IO-PIE	IO-NIE	FO-PIE	FO-NIE
Impedance Function	$Z_{in}(s) = sC/g_{mF}g_{mS}$	$Z_{in}(s) = -sC/g_{mF}g_{mS}$	$Z^{\alpha}_{in}(s^{\alpha}) = s^{\alpha}C^{\alpha}/g_{mF}g_{mS}$	$Z^{\alpha}_{in}(s^{\alpha}) = -s^{\alpha}C^{\alpha}/g_{mF}g_{mS}$
Magnitude	$\lvert Z_{in}(\omega)\rvert = \omega C/g_{mF}g_{mS}$	$\lvert Z_{in}(\omega)\rvert = \omega C/g_{mF}g_{mS}$	$\lvert Z^{\alpha}_{in}(\omega^{\alpha})\rvert = \omega^{\alpha}C^{\alpha}/g_{mF}g_{mS}$	$\lvert Z^{\alpha}_{in}(\omega^{\alpha})\rvert = \omega^{\alpha}C^{\alpha}/g_{mF}g_{mS}$
Phase	$\angle Z_{in}(\omega) = \pi/2$	$\angle Z_{in}(\omega) = -\pi/2$	$\angle Z^{\alpha}_{in}(\omega^{\alpha}) = \alpha\pi/2$	$\angle Z^{\alpha}_{in}(\omega^{\alpha}) = -\alpha\pi/2$

It may be observed from the impedance function of a integer and fractional order negative inductor that its magnitude increases with frequency like positive integer and fractional order inductor whereas it provides a negative phase like a integer and fractional order capacitor. Similarly, the magnitude of negative inductor increases with frequency in the same manner as that of an inductor however, it provides a phase of (-π/2) like a capacitor. Further the equivalent inductance value may be electronically tuned through VDTA transconductances in all four cases.

3.3 Non-Ideal Analysis

The analytical expressions presented in the preceding subsection have been obtained considering the VDTA to be ideal and therefore all the input and output terminals of the VDTA have been considered to be having infinite impedances. This section presents the mathematical analysis of the proposed circuit taking into account the parasitics at the input and output terminals of the VDTA. For the sake of brevity the non ideal analysis of the proposed FO-NIE is presented here which can be extended to analyse the non ideal behaviour of all derived configurations. The non-ideal behavioural model of the proposed FO-NIE is depicted in Fig. 3.2 wherein each terminal is represented with a finite impedance Z_i (i = p, n, z, x) consisting of a capacitor C_i in parallel with a resistance R_i.

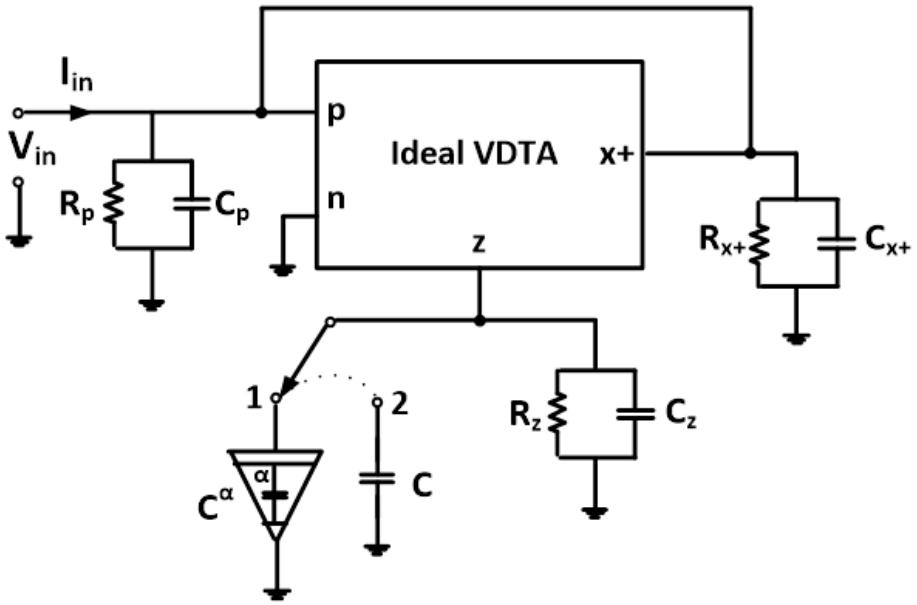


Fig. 3.2 Non Ideal Behavioural Model of the FO-NIE.

Considering current flowing into the ‘p’ terminal of the ideal VDTA as null the nodal equation at node ‘p’ can be expressed as

$$(1/R_{x+} + sC_{x+})V_{in}(s^{\alpha}) - I_{in}(s^{\alpha}) + (1/R_p + sC_p)V_{in}(s^{\alpha}) = g_{mS}V_z \tag{3.3}$$

The nodal equation at ‘z’ terminal can be written as

$$g_{mF}V_{in}(s^{\alpha}) = (1/R_z + sC_z)V_z + s^{\alpha}C^{\alpha}V_z \tag{3.4}$$

From (3.3) and (3.4), overall input current may be obtained as

$$I_{in}(s^{\alpha}) = V_{in}(s^{\alpha})\left[(1/R_{x+} + 1/R_p) + s(C_{x+} + C_p) - \frac{g_{mF}g_{mS}}{(1/R_z + sC_z) + s^{\alpha}C^{\alpha}}\right] \tag{3.5}$$

Thus the impedance function under non ideal conditions can be expressed as

$$Z_{in}(s^{\alpha}) = \frac{V_{in}(s^{\alpha})}{I_{in}(s^{\alpha})} = \frac{(1/R_z + sC_z) + s^{\alpha}C^{\alpha}}{\left[(1/R_z + sC_z) + s^{\alpha}C^{\alpha}\right]\left[(1/R_{x+} + 1/R_p) + s(C_{x+} + C_p)\right] - g_{mF}g_{mS}} \tag{3.6}$$

It may be observed from Eqn. (3.6) that the values of $1/R_x$ and $1/R_p$ being very small may be ignored. Similarly C_z, C_x and C_p being too small in magnitude lead to very high impedance for low operating frequencies ($s << 1/R_zC_z$ and $1/R_pC_p$) which may be treated as open circuit. Thus the parasitics are rendered ineffective under these conditions and Eqn. (3.6) tends to the ideal impedance expression as given in Table 3.2.

3.4 Functional Validation

The performance of the proposed VDTA based generic grounded integer and fractional order positive and negative impedance emulator is validated through simulations as well as experimental work.

3.4.1 Simulation Results

The workability of the proposed VDTA based generic grounded integer and fractional order positive and negative impedance emulator is validated through simulations using Virtuoso from Cadence Spectre tool suite using 180 nm (gpdk) technology node. Results of integer order emulator are presented first followed by fractional order emulator. For all simulations, values of g_{mF} and g_{mS} are considered as 400 uA/V.

3.4.1.1 The FC Implementation

In this work FCs are implemented using RC ladder network of Fig. 2.4 truncated to 12^{th} order. The ladder networks are designed and simulated using Virtuoso for FCs (represented as C^{α}) of value 12.5 $\mu\text{Ʊ}/s^{0.3}$, 3.75 $\mu\text{Ʊ}/s^{0.5}$ and 0.13 $\mu\text{Ʊ}/s^{0.7}$ respectively. The corresponding component values used are as given:

(i) $\alpha = 0.3$ and $C^{\alpha} = 12.5\ \mu\text{Ʊ}/s^{0.3}$

R_a = 47 kΩ, R_b = 20 kΩ, R_c = 12 kΩ, R_d = 7.8 kΩ, R_e = 4.7 kΩ, R_f = 2.7 kΩ, R_g = 1.6 kΩ, R_h = 1 kΩ, R_i = 560 Ω, R_j = 390 Ω, R_k = 220 Ω, R_l = 68 Ω, R_m = 270 Ω, C_a = 22 μF, C_b = 10 μF, C_c = 2.76 μF, C_d = 820 nF, C_e = 270 nF, C_f = 82 nF, C_g = 22 nF, C_h = 7.6 nF, C_i = 2.2 nF, C_j = 680 pF, C_k = 220 pF, C_l = 470 pF;

(ii) $\alpha = 0.5$ and $C^{\alpha} = 3.75\ \mu\text{Ʊ}/s^{0.5}$

R_a = 330 kΩ, R_b = 82 kΩ, Rc = 33 kΩ, R_d = 12 kΩ, R_e = 4.7 kΩ, R_f = 2 kΩ, R_g = 736 Ω, R_h = 270 Ω, R_i = 120 Ω, R_j = 47 Ω, R_k = 8.2 Ω, R_l = 18.2 Ω, C_a = 4.7 μF, C_b = 3.1 μF, C_c = 1 μF, C_d = 470 nF, C_e = 168 nF, C_f = 68 nF, C_g = 27 nF, C_h = 10 nF, C_i = 4.7 nF, C_j = 1 nF, C_k = 2.2 nF;

(iii) $\alpha = 0.7$ and $C^{\alpha} = 0.13\ \mu\text{Ʊ}/s^{0.7}$

R_a = 20 MΩ, R_b = 2 MΩ, R_c = 470 kΩ, R_d = 82 kΩ, R_e = 20 kΩ, R_f = 3.9 kΩ, R_g = 820 Ω, R_h = 150 Ω, R_i = 33 Ω, R_j = 3.3 Ω, R_k = 4.7 Ω, C_a = 150 nF, C_b = 150 nF, C_c = 82 nF, C_d = 33 nF, C_e = 22 nF, C_f = 10 nF, C_g = 5.6 F, C_h = 2.67 nF, C_i = 1.33 nF, C_j = 1.33 nF.

The ideal and simulated magnitude and phase responses for these FCs are shown in Fig. 3.3 (a) and (b) respectively.

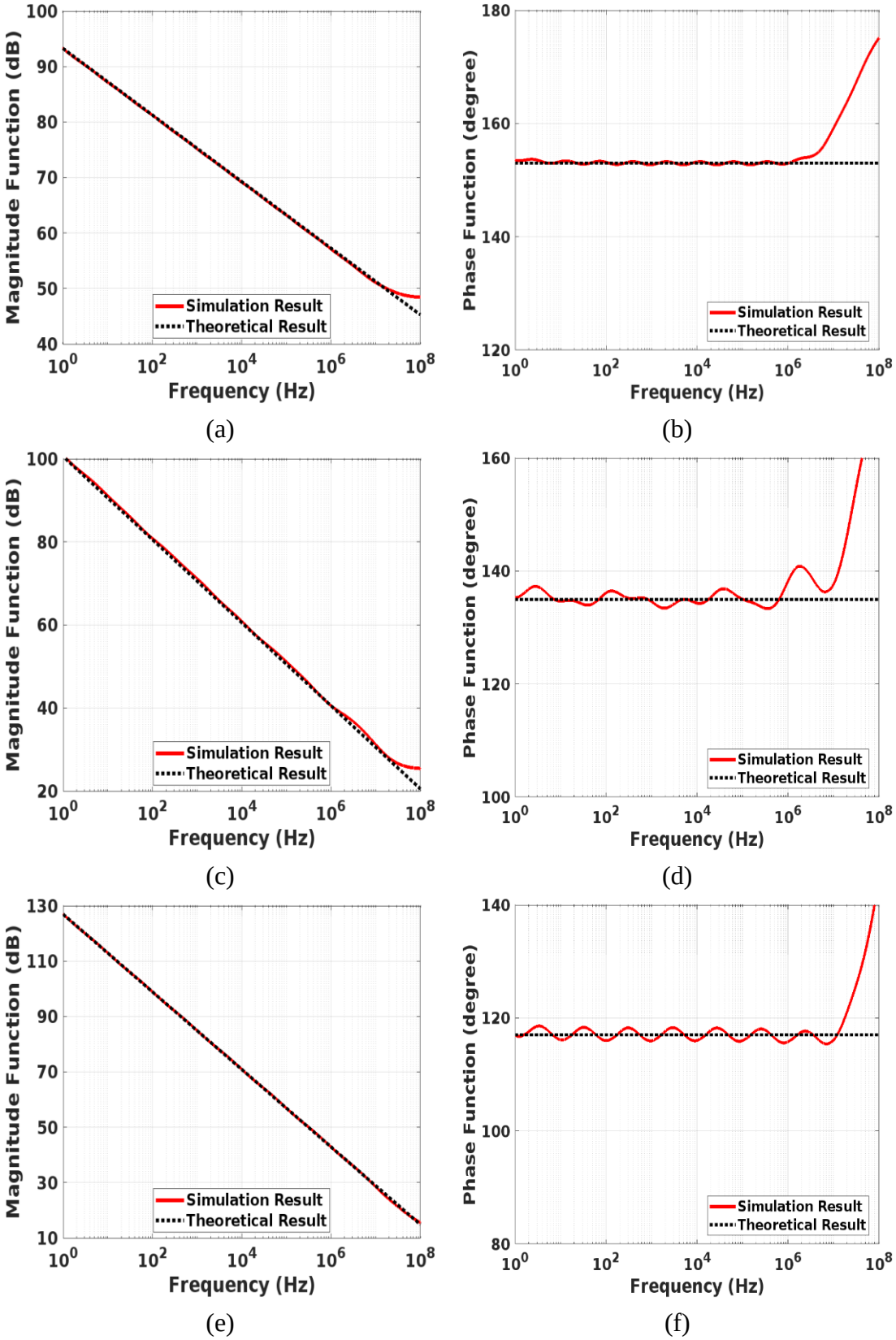
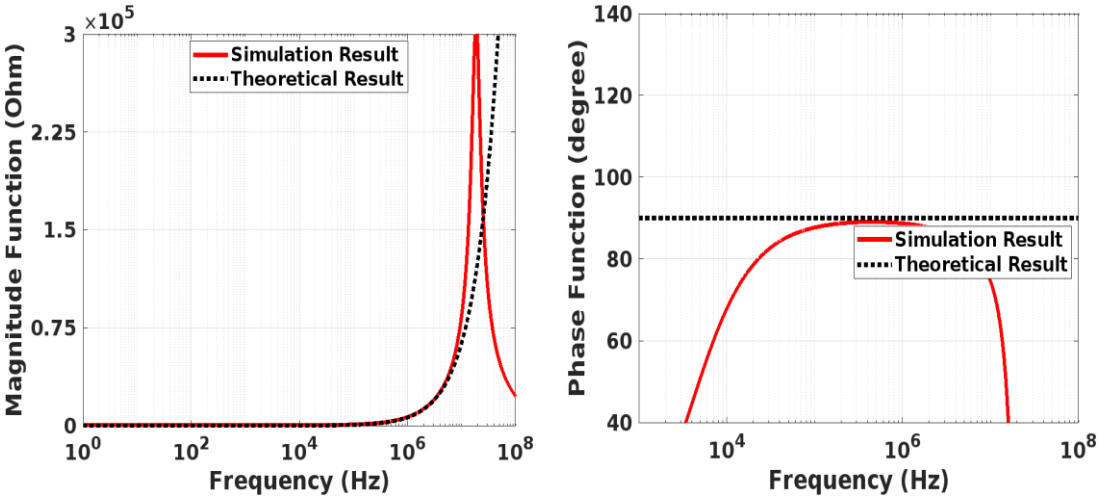


Fig. 3.3 The FC Impedance: (a),(c),(e) Magnitude (b),(d),(f) Phase Response with C^{α} = 12.5 μ℧/$s^{0.3}$, 3.75 μ℧/$s^{0.5}$ and 0.13 μ℧/$s^{0.7}$ respectively.

It may be observed from Fig. 3.3(a) that the magnitude curves follow the ideal response approximately up to 50 MHz. Further, the phase remains constant with a maximum deviation of ±4◦ for all FCs over a frequency range of 50 MHz approximately. Thus, the simulation results verify the functionality of the designed FCs.

3.4.1.2 Integer order Inductance Emulator

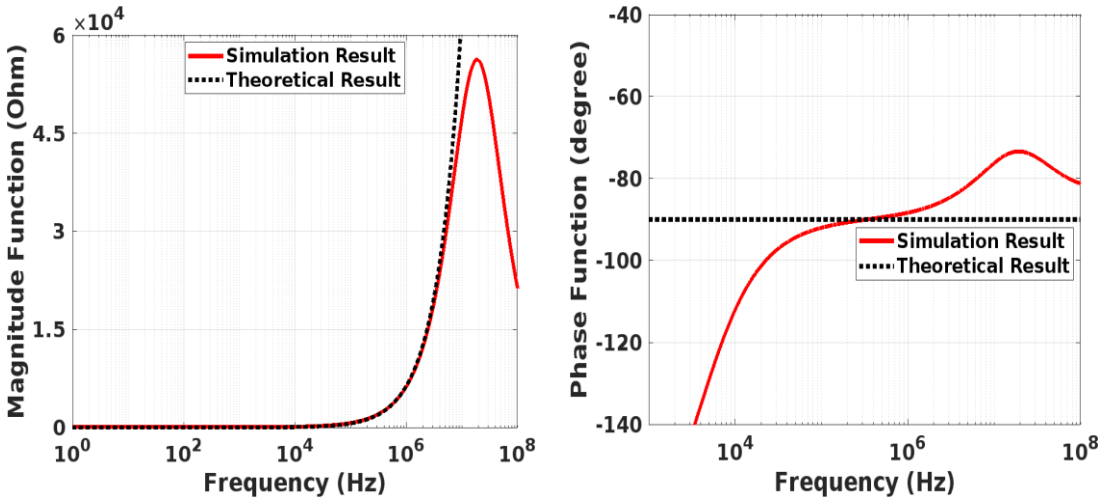
The proposed emulator is configured as a 1 mH positive inductor for which the integer capacitance value is chosen as 0.16 nF. The impedance response so obtained is depicted in Fig. 3.4. It is to be noted from Fig. 3.4(a), the magnitude of the impedance increases with the frequency whereas the phase response of Fig. 3.4(b) suggests that the phase is positive. It is observed that the simulated magnitude response follows the ideal response approximately up to 50 MHz whereas the phase curve follows the ideal value of $\pi/2$ in frequency range of 50 kHz to 30 MHz thereby verifying the positive inductance behaviour in the specified range.



(a) (b)

Fig. 3.4 Positive Impedance: (a) Magnitude (b) Phase Response with L = 1 mH.

The impedance magnitude and phase responses obtained for 1 mH negative inductor are depicted in Fig. 3.5. The magnitude of the impedance increases with the frequency and the phase is a negative value. The magnitude response is in agreement with the ideal curve till 50 MHz and the simulated phase response follows the ideal phase curve in the frequency range of 20 kHz to 20 MHz.



(a) (b)

Fig. 3.5 Negative Impedance: (a) Magnitude (b) Phase Response with L = 1 mH.

3.4.1.3 Fractional order Inductance Emulator

Three instances of fractional order positive inductance are emulated first by selecting FCs of value C^{α} = 12.5 μ℧/$s^{0.3}$, 3.75 μ℧/$s^{0.5}$ and 0.13 μ℧/$s^{0.7}$ respectively and the corresponding values are obtained as 78.13 Ω/$s^{0.3}$, 23.44 Ω/$s^{0.5}$ and 0.78 Ω/$s^{0.7}$ respectively. The impedance responses for the three fractional order positive inductances are depicted in Fig. 3.6 which show that the impedance magnitudes of all the fractional order positive inductances increase with the frequency like a fractional order inductor (FI) whereas their phase values are positive and remain constant for a given ‘α’.

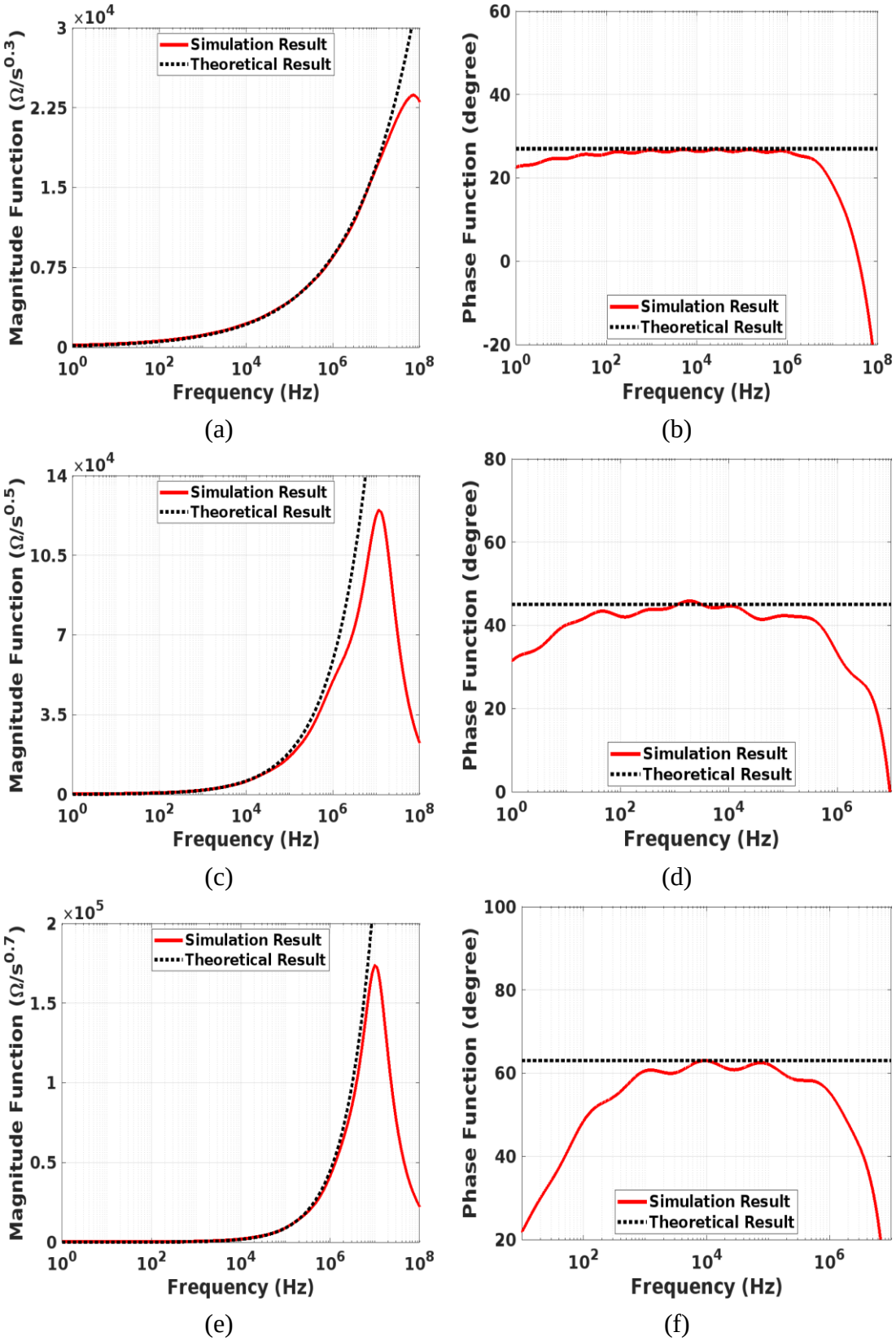


Fig. 3.6 Fractional Positive Impedance: (a),(c),(e) Magnitude (b),(d),(f) Phase Response with L^{α} = 78.13 $\Omega/s^{0.3}$, 23.44 $\Omega/s^{0.5}$ and 0.78 $\Omega/s^{0.7}$ respectively.

It may be observed from Fig. 3.6 (a) that the simulated impedance magnitude curve for fractional order positive inductance emulator of value 78.13 $\Omega/s^{0.3}$ follows the ideal curve up to 10 MHz whereas for fractional order positive inductance emulators of values 23.44 $\Omega/s^{0.5}$ and 0.78 $\Omega/s^{0.7}$ respectively the ideal and simulated curves are in agreement up to 1.3 MHz. It is observed from the corresponding phase responses that the fractional order positive inductance emulators follow ideal phase responses with a deviation of ±5° in the frequency ranges (0 Hz – 50 MHz), (10 Hz – 400 KHz) and (500 Hz – 700 KHz) for 78.13 $\Omega/s^{0.3}$, 23.44$\Omega/s^{0.5}$ and 0.78$\Omega/s^{0.7}$ respectively. Thus, in the given frequency ranges the simulated magnitude and phase responses accord well with the theoretical computations.

Further the impedance responses for the fractional order negative inductances (represented as L^{α}) of values 78.13 $\Omega/s^{0.3}$, 23.44$\Omega/s^{0.5}$ and 0.78$\Omega/s^{0.7}$ are plotted as depicted in Fig. 3.7.

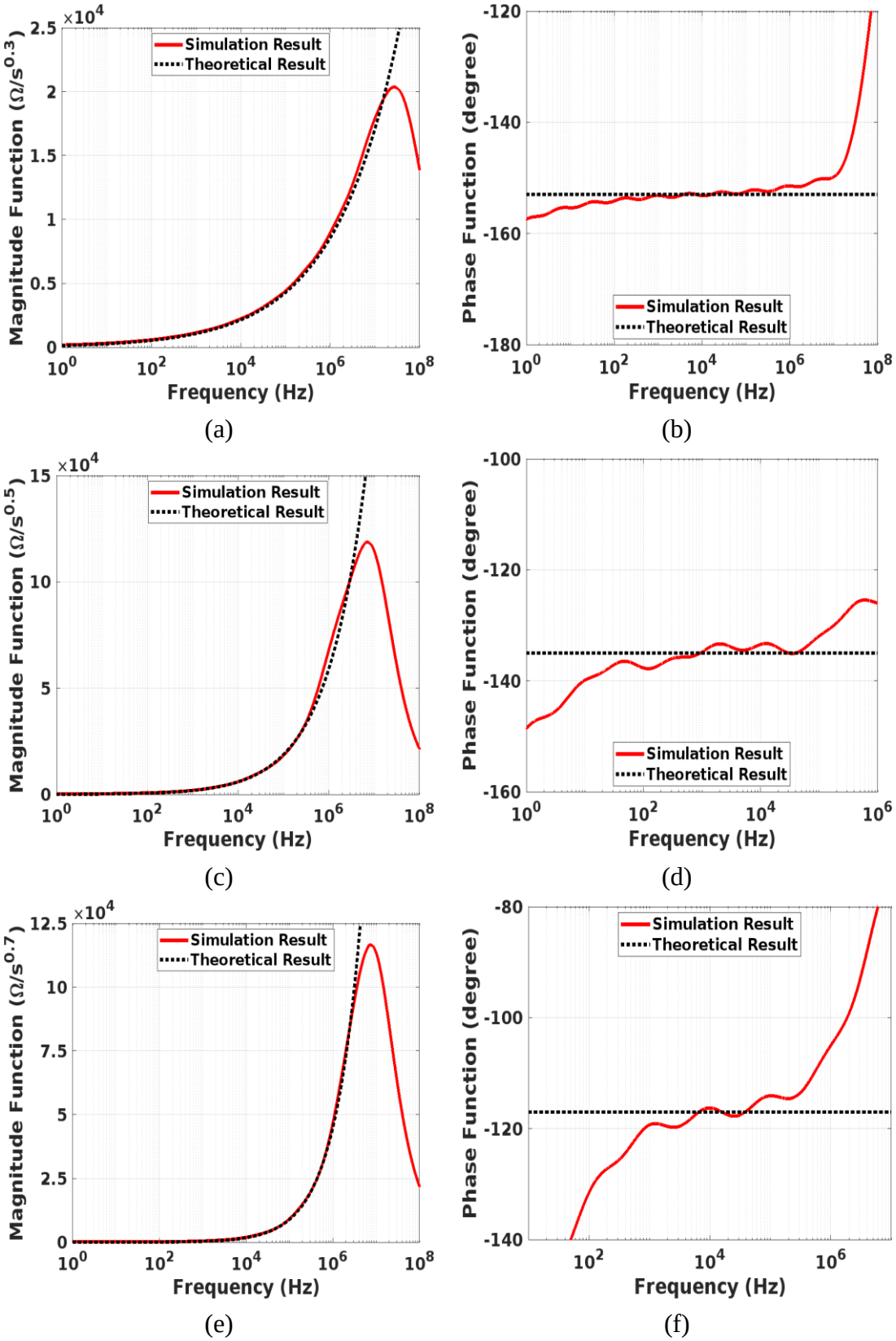


Fig. 3.7 Fractional Negative Impedance: (a),(c),(e) Magnitude (b),(d),(f) Phase Response for Values 78.13 $\Omega/s^{0.3}$, 23.44 $\Omega/s^{0.5}$ and 0.78 $\Omega/s^{0.7}$ respectively.

The magnitude responses shown in Fig. 3.7(a),(c),(e) for fractional order negative inductance emulator are exactly the same as those of the fractional order positive inductance emulators however the phase represents a positive constant value for a given 'α' as shown in Fig. 3.7(b),(d),(f). It may be observed from Fig. 3.7(b) that the phase responses for fractional order negative inductance emulator of value 78.13 $\Omega/s^{0.3}$ follow the ideal curves within frequency range (0 Hz – 50 MHz) and (30 Hz – 200 KHz) for the other two fractional order negative inductance emulators i.e. $23.44\Omega/s^{0.5}$ and $0.78\Omega/s^{0.7}$ with a deviation of ±5°.

Electronic tuning of the proposed fractional inductance emulator is illustrated through variation of inductance with respect to the transconductance of the VDTA. The transconductance of the VDTA is varied from 50 μS to 400 μS resulting in fractional inductance variation as shown in Fig. 3.8.

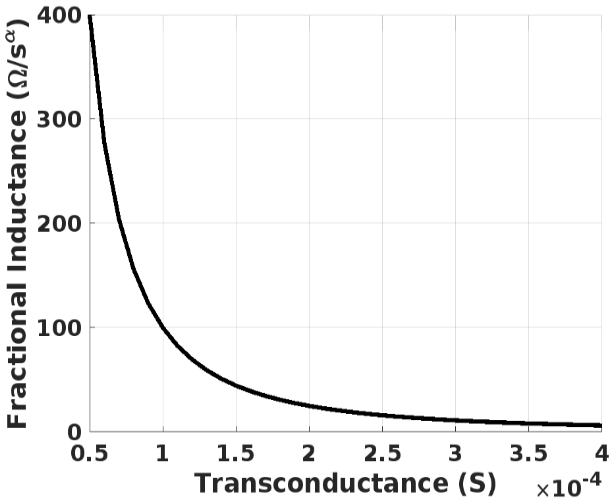


Fig. 3.8 Fractional Inductance Variation with Transconductance.

The proposed generic impedance emulator is also tested for transient behaviour. The transient responses of integer order positive and negative inductance emulators (1 mH) for a 20 mV, 400 kHz sinusoidal signal and corresponding Lissajous patterns are observed. Further, the transient response of integer order positive inductance emulator shown in Fig. 3.9(a) and corresponding Lissajous pattern depicted in Fig. 3.9(b) confirm that the voltage is leading by $\pi/2$ thus confirming the positive inductor behaviour. It may further be observed from transient response of integer order negative inductance emulator and corresponding Lissajous pattern presented in Fig. 3.10(a) and Fig. 3.10(b) respectively that voltage is lagging by $\pi/2$.

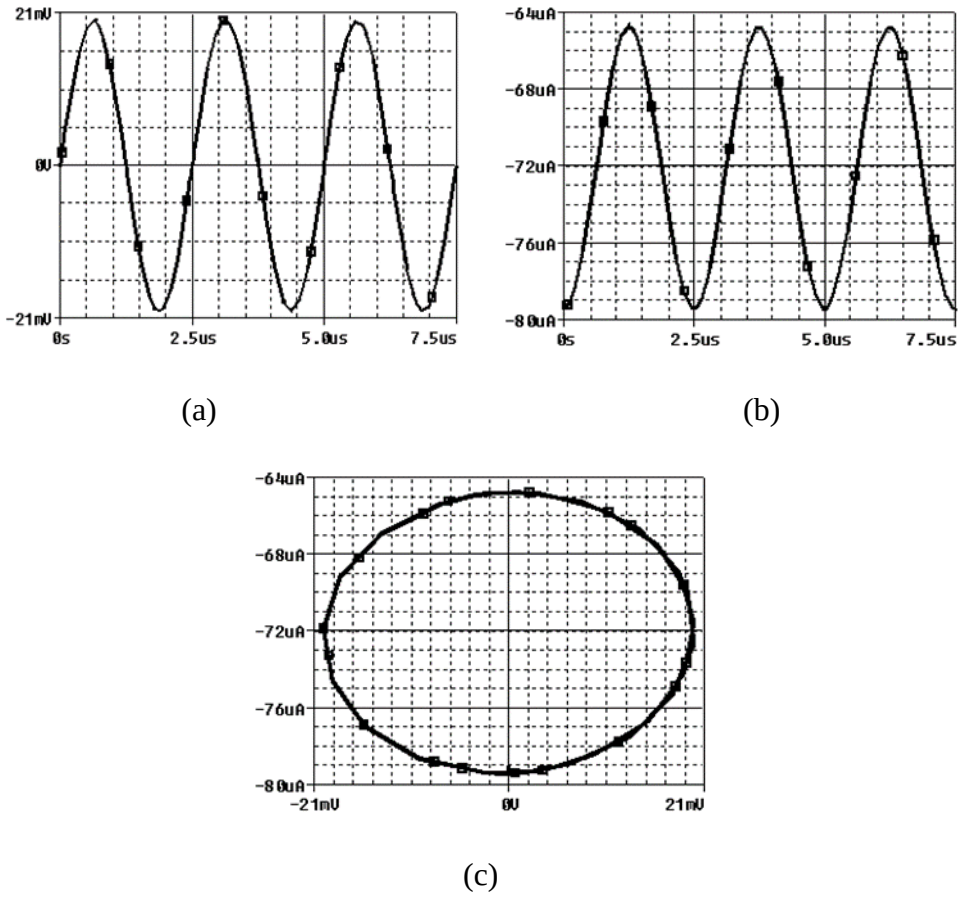
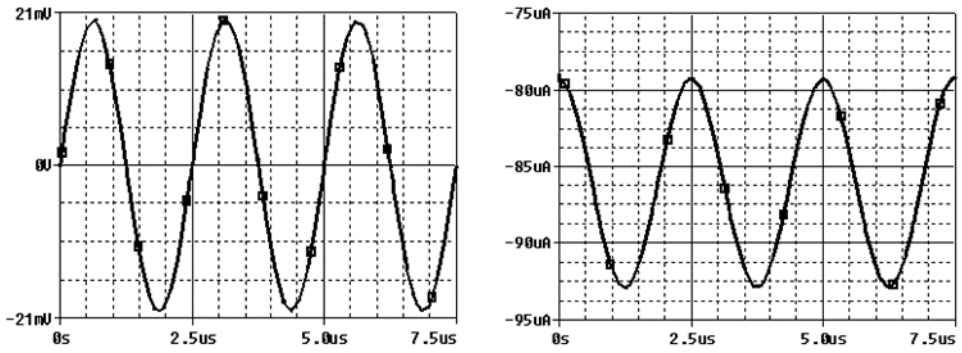
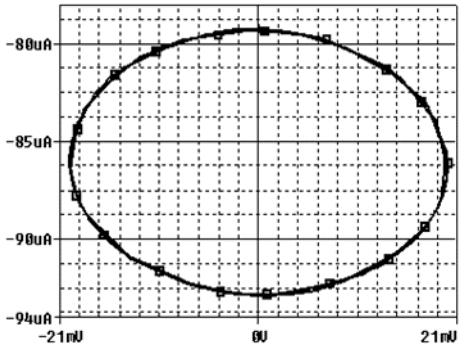


Fig. 3.9 Positive Impedance: (a),(b) Transient Response: Voltage and Current respectively (c) Lissajous.



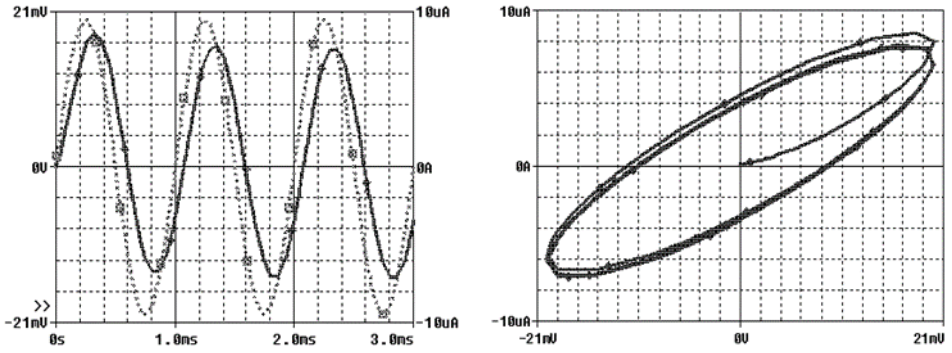
(a) (b)



(c)

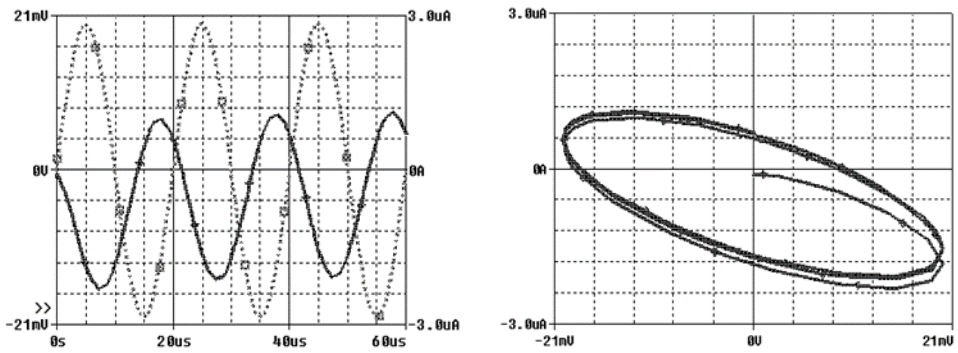
Fig. 3.10 Negative Impedance: (a),(b) Transient Response: Voltage and Current respectively (c) Lissajous.

The transient response of fractional order positive inductance emulator (L^{α} = 23.44 $\Omega/s^{0.5}$) for a 20 mV, 1 kHz sinusoidal signal is shown in Fig. 3.11(a). It may be observed from the transient response that the voltage signal is leading current thus verifying the positive inductance behavior. Further, the corresponding right inclined elliptical Lissajous pattern as depicted in Fig. 3.11(b) verifies the phase dependence on 'α'. Similar results for fractional order negative inductance emulator (L^{α} = 23.44 $\Omega/s^{0.5}$) for a 20 mV, 50 kHz sinusoidal signal are depicted in Fig. 3.12 which verify that the voltage signal is lagging and its phase is dependent on 'α' value.



(a) (b)

Fig. 3.11 Fractional Positive Impedance: (a) Transient (b) Lissajous.



(a) (b)

Fig. 3.12 Fractional Negative Impedance: (a) Transient (b) Lissajous.

3.4.2 Experimental Results

The proposed VDTA based generic grounded integer/fractional positive/negative inductance emulator is validated through experimental results also after verification through simulations for the proof of concept. For experimental purposes, VDTA is being implemented using off the shelf IC LM 13700 with ±10V supply voltage. The transconductance g_{mF} and g_{mS} are set as 3.58 mA/V and the FC is realized using truncated 12^{th} order RC ladder circuit having component values same as taken for simulations. The experimental setup is shown in Fig. 3.13. The inductance emulator is verified for all four cases for following instances and the corresponding results are depicted in Figs. 3.14 to 3.17:

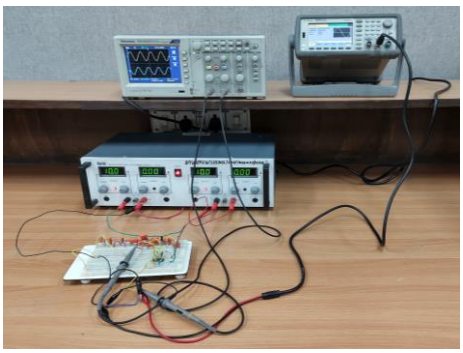
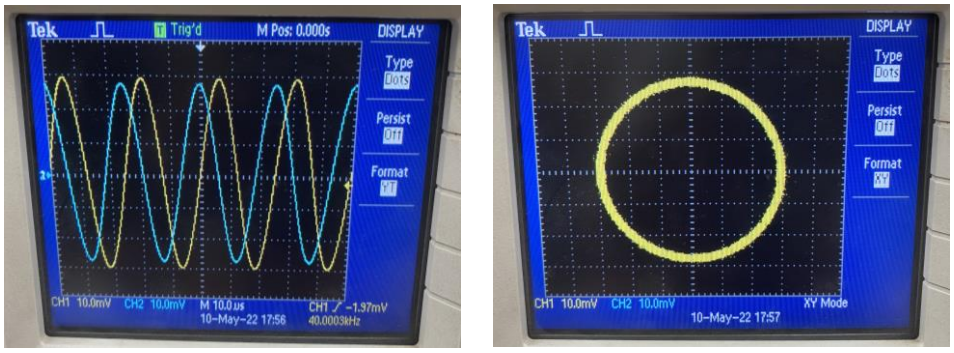


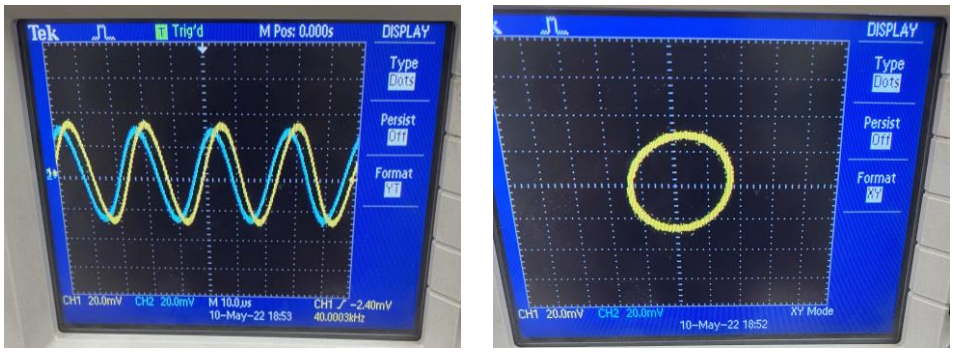
Fig. 3.13 Hardware Setup.

The transient response of the circuit for integer order positive inductance emulator for 1 mH is shown in Fig. 3.14(a) and corresponding Lissajous pattern is presented in Fig. 3.14(b). The transient response of the circuit for integer order negative inductance emulator is presented in Fig. 3.15(a) and its Lissajous pattern is depicted in Fig. 3.15(b). The Lissajous patterns depicted in Figs. 3.14(b) and 3.15(b) respectively confirm the phase shift of $\pi/2$ and hence verify the integer order behaviour.



(a) (b)

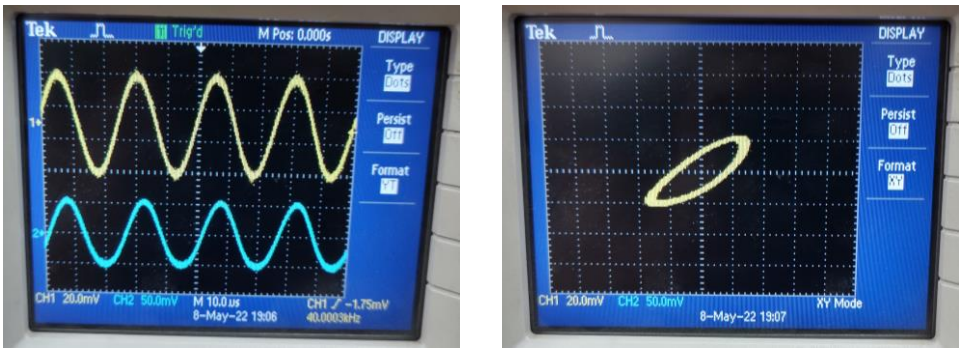
Fig. 3.14 Positive Impedance: (a) Transient Response (b) Lissajous.



(a) (b)

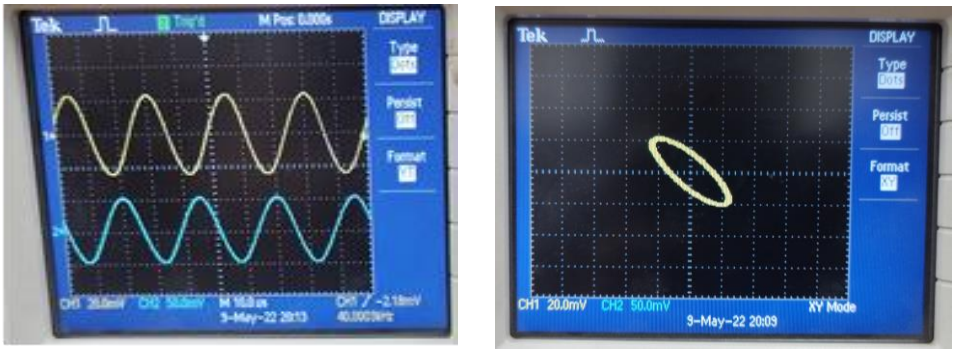
Fig. 3.15 Negative Impedance: (a) Transient Response (b) Lissajous.

Further the experimental transient responses for fractional order positive inductance emulator and fractional order negative inductance emulator of values 23.44 $\Omega/s^{0.5}$ are shown in Fig. 3.16(a) and Fig. 3.17(a) respectively. It may be observed from experimental results that for fractional inductances the phase is dependent on 'α' and phase of fractional order positive inductance emulator and fractional order negative inductance emulator are out of phase with each other.



(a) (b)

Fig. 3.16 Fractional Positive Impedance: (a) Transient Response (b) Lissajous.



(a) (b)

Fig. 3.17 Fractional Negative Impedance: (a) Transient Response (b) Lissajous.

The fractional order ‘α’ adds extra degree of freedom to the impedance. In order to illustrate this fact pictorially the impedance magnitude versus frequency is plotted for different values of ‘α’ while C^{α} was taken as 3.75 $\mu\mho/s^{0.5}$. The magnitude plot shown in Fig. 3.18 clearly indicates that a continuum of impedance values may be achieved by changing ‘α’ in comparison to narrow domain integer impedance.

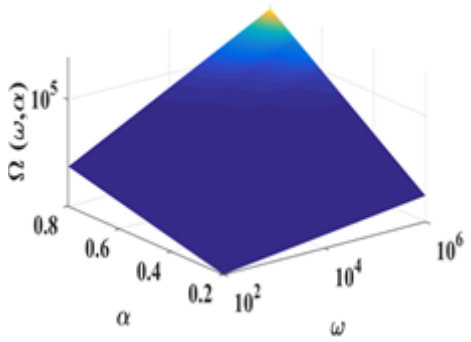


Fig. 3.18 Impedance at different Fractional Orders.

3.5 Applications

Two application examples namely (i) parasitic inductance cancellation using fractional order negative inductance emulator (ii) fractional order high pass RL$^{\alpha}$C filter using fractional order positive inductance emulator are presented for demonstrating the effectiveness of the proposed generic impedance emulator.

3.5.1 Inductance Cancellation

The parasitic cancellation property of the proposed fractional order negative inductance emulator is demonstrated by designing a network as shown in Fig. 3.19 consisting of a resistance in series with a fractional order floating inductance simulator which is treated as parasitic inductance and proposed fractional order negative inductance emulator. When the value of a fractional order inductor is equal to fractional order negative inductance emulator the circuit will be rendered purely resistive. For simulation a VDTA based FO inductor of value $L^{\alpha} = 23.44\ \Omega s^{0.5}$ is designed and placed in series with fractional order negative inductance emulator of the same value. A resistance of 1 kΩ is used in the circuit. It is evident from the simulation result depicted in Fig. 3.20 that the current and voltage are in phase demonstrating the effect of inductance cancellation.

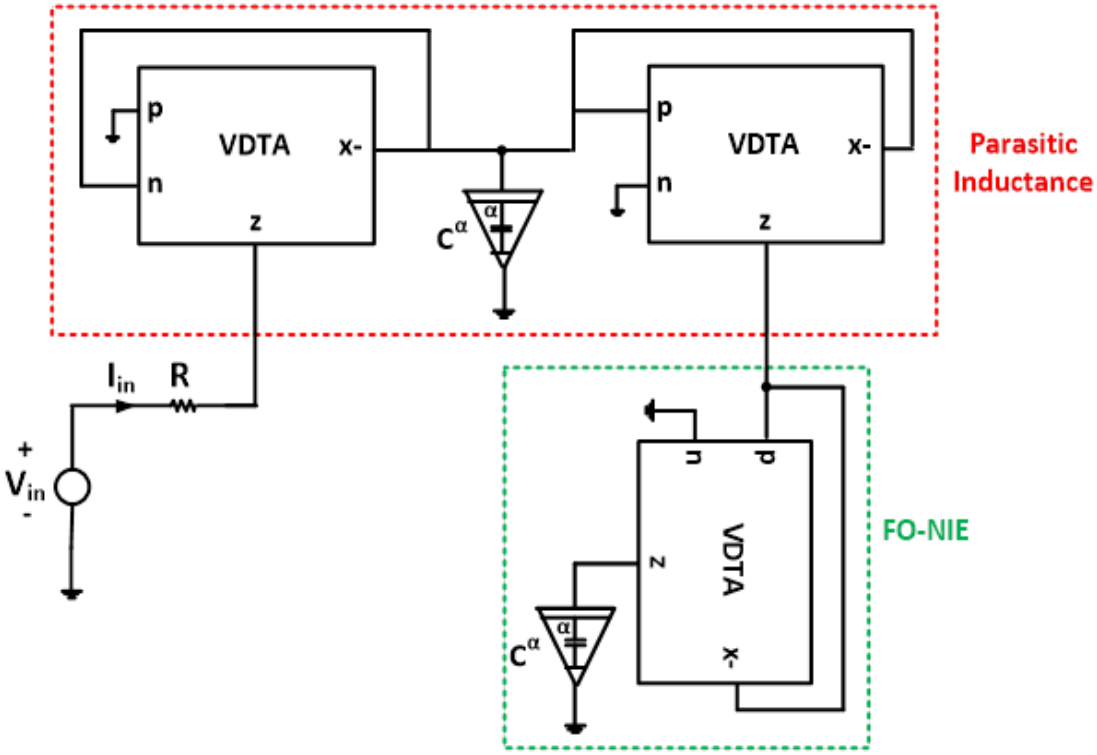
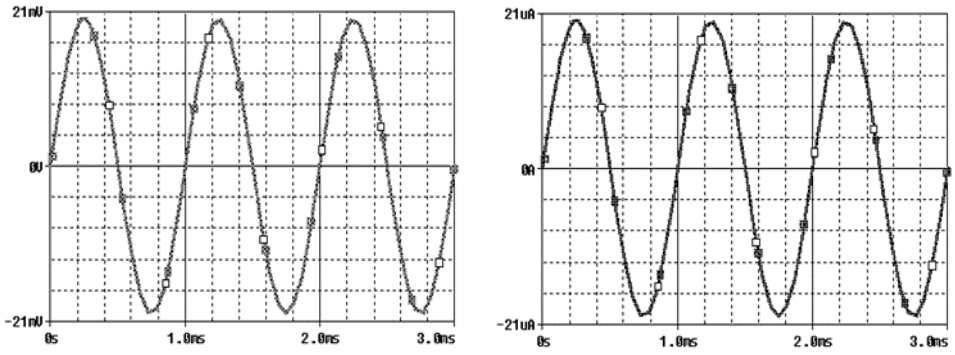


Fig. 3.19 Circuit depicting Inductance Cancellation using Proposed FO-NIE.



(a) (b)

Fig. 3.20 Transient Response: (a) Voltage (b) Current of the Circuit of Fig. 3.19.

3.5.2 Fractional order High Pass RL$^{\alpha}$C Filter

In this subsection a fractional order high pass filter (FO-HP) is designed using RL$^{\alpha}$C circuit as shown in Fig. 3.21.

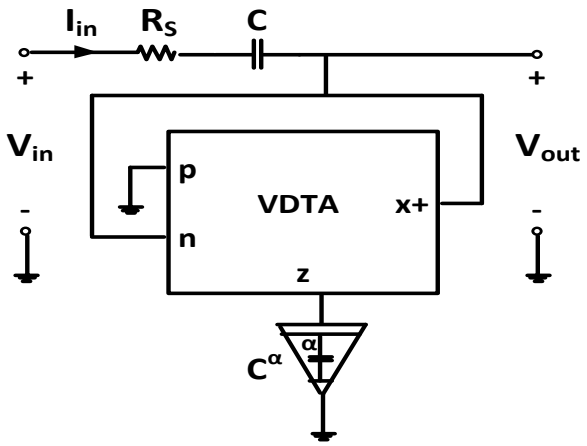


Fig. 3.21 Circuit depicting FO-HP RL$^{\alpha}$C Filter.

where L^{α} is implemented using proposed fractional order positive inductance emulator. Using routine analysis the transfer function of the filter is obtained as

$$H^{\alpha}_{FHPF}(s) = \frac{s^{2\alpha}}{s^{2\alpha} + R_S/L^{\alpha}\, s^{\alpha} + 1/CL^{\alpha}} \tag{3.7}$$

The critical frequencies i.e. 3 dB and right phase frequencies for FHPF may be obtained by deriving magnitude and phase functions from Eqn. (3.7) as given by Eqn. (3.8) and Eqn. (3.9) respectively

$$\left|H^{\alpha}_{FHPF}(\omega)\right| = \frac{\omega^{2\alpha}}{\left[\begin{array}{l}\omega^{4\alpha} + 2R_S/L^{\alpha}\,\omega^{3\alpha}\cos\alpha\pi/2 + \omega^{2\alpha}\left(2/CL^{\alpha}\cos\alpha\pi + R_S^2/L^{2\alpha}\right) \\ +2R_S/L^{\alpha}\,1/CL^{\alpha}\,\omega^{\alpha}\cos\alpha\pi/2 + 1/C^2L^{2\alpha}\end{array}\right]^{1/2}} \tag{3.8}$$

$$\underline{\left|H^{\alpha}_{FHPF}(\omega)\right|} = \tan^{-1}\frac{R_S/L^{\alpha}\,\omega^{\alpha}\sin\alpha\pi/2 + 1/CL^{\alpha}\sin\alpha\pi}{\omega^{2\alpha} + R_S/L^{\alpha}\,\omega^{\alpha}\cos\alpha\pi/2 + 1/CL^{\alpha}\cos\alpha\pi} \tag{3.9}$$

The 3 dB frequency expression of fractional order high pass filter may be expressed as

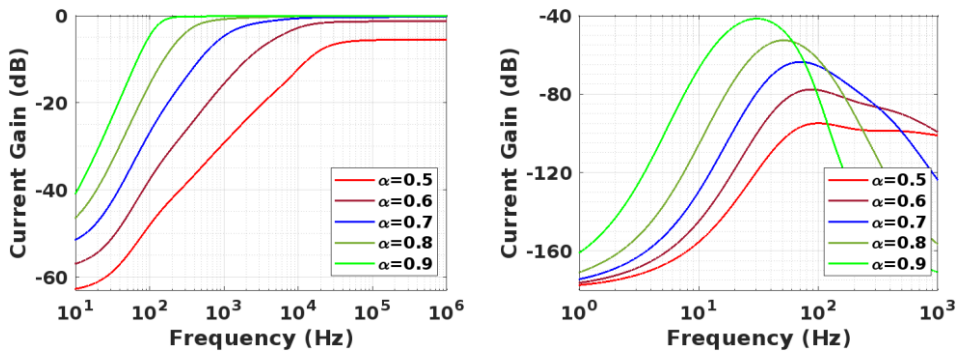
$$\omega_{3dB(FHPF)}^{4\alpha} - 2R_S/L^{\alpha}\,\omega_{3dB(FHPF)}^{3\alpha}\cos\alpha\pi/2 - \omega_{3dB(FHPF)}^{2\alpha}\left(2/CL^{\alpha}\cos\alpha\pi + R_S^2/L^{2\alpha}\right) - 2R_S/L^{\alpha}\,1/CL^{\alpha}\,\omega_{3dB(FHPF)}^{\alpha}\cos\alpha\pi/2 - 1/C^2L^{2\alpha} = 0 \quad (3.10)$$

Right phase frequency may be obtained by equating the phase to ±π/2.

$$\omega_{rp(FHPF)} = \left(\frac{-R_S/2L^{\alpha}\cos\alpha\pi/2 + \sqrt{R_S^2/4L^{2\alpha}\cos^2\alpha\pi/2 - 1/CL^{\alpha}\cos\alpha\pi}}{2}\right)^{1/\alpha} \quad (3.11)$$

It is worth noting that the critical frequencies of the FO-HP filter are dependent on the transconductances of the VDTA, which in-turn can be varied with biasing currents. Thus the critical frequencies of the FO-HP filter are electronically tunable.

The functionality of the fractional order high pass RL$^{\alpha}$C filter is verified through simulations. The magnitude and phase responses for Rs = 1 kΩ, C$^{\alpha}$ = 1 μ℧/s$^{\alpha}$ and L$^{\alpha}$ = 23.44 Ω/s$^{0.5}$ with a centre frequency of 1 kHz using fourth-order approximation for α = 0.5 to 0.9 in steps of 0.1 are illustrated in Fig. 3.22 and the DC gains along with the critical frequencies are recorded in Table 3.3 for quick reference.



(a) (b)

Fig. 3.22 Frequency Response for FO-HP RL$^{\alpha}$C Filter (a) Magnitude (b) Phase.

Table 3.3 Performance Parameters for Fractional Order High Pass Filter.

Fractional Order	DC Gain (dB)		3 dB Frequency (Hz)		Peak Frequency (Hz)		Right Phase Frequency (Hz)	
	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated
0.5	-5.34	-5.52	127.15 k	17.61 k	NA	NA	NA	NA
0.6	-1.14	-1.31	9.80 k	6.27 k	NA	NA	558.21	491.03
0.7	-0.13	-0.29	1.47 k	1.40 k	NA	NA	374.19	360.62
0.8	-0.02	-0.06	345.89	354.16	NA	NA	201.40	198.35
0.9	-0.00	-0.01	114.80	115.99	NA	NA	110.21	111.56

The simulated FO-HP RL$^{\alpha}$C filter parameters are in found to be in close agreement with the theoretical values thus verifying the functionality of proposed FO-PIE.

3.6 Conclusion

A generic grounded impedance emulator based on VDTA is presented in this work which can emulate the behaviour of (i) integer order positive inductor, (ii) integer order negative inductor, (iii) fractional order positive inductor and (iv) fractional order negative inductor. The proposed topology is designed using a single VDTA and a grounded capacitor or FC. Non-ideal behaviour of the proposition is analyzed numerically. Simulations have been carried out using Cadence Virtuoso. The FC is emulated using 12th order approximation based on CFE method. The functionality of all emulators is verified through frequency and time domain responses. Theoretical and simulated results are found to be at par with the proposed theory. Two application examples are presented to show the effectiveness of the emulated fractional order positive/negative inductors.

CHAPTER – 4

INTEGER AND FRACTIONAL ORDER FILTERS

The content and results of the following publications are included in this chapter:

2. Parveen Rani and Rajeshwari Pandey, "Voltage Differencing Transconductance Amplifier based Fractional order Multiple Input Single Output Universal Filter", *Solid State Electronics Letters*, vol. 1, no. 2, pp. 110-118, July 2019. **DOI:** https://doi.org/10.1016/j.ssel.2020.01.006

3. Parveen Rani and Rajeshwari Pandey, "Electronically Tunable Fractional Order Filter based on Single VDTA", *8th International Conference on Signal Processing and Integrated Networks*, pp. 835-838, 2021. **DOI:** https://doi.org/10.1109/SPIN52536.2021.9565975

4. Parveen Rani and Rajeshwari Pandey, "Single VDTA based Multi-Mode MIMO Filter", *IEEE 1st International Conference on Signal Processing, VLSI and Communication Engineering*, 2019. (Paper ID: 151)

5. Parveen Rani and Rajeshwari Pandey, "Single VDTA based CM SIMO fractional order filter". (Communicated)

4.1 Introduction

Analog filters are frequency selective networks and may be broadly classified as first-, second- and higher- order filters. Second-order filters are most popularly known as biquadratic (or biquad) filters. Biquads may be further categorized as single input single output (SISO), single input multiple output (SIMO), multiple input single output (MISO) and multiple input multiple output (MIMO) biquads. Likewise conventional filters, FOFs are also termed as SISO, SIMO, MISO and MIMO fractional order filters.

In this Chapter, voltage differencing transconductance amplifier based integer analog filter and two fractional order filters are presented. Firstly, conventional biquad is presented having multiple inputs and multiple outputs operating in all possible modes (VM, TAM, TIM and CM). Moving on to the state-of-the-art fractional order filters, two topologies are presented. The first proposed fractional order filter represents a multifunction and is based on the continued fraction expansion (CFE) based rational approximation, while the second one is universal in nature and uses Carlson approximation. It is pertinent to mention here that both the proposed fractional order filters make use of the FC implementation which is realized using RC ladder network truncated to fourth order.

4.2 Integer Order Filter

The proposed VDTA based multi-mode MIMO filter is depicted in Fig. 4.1. When the circuit is driven by voltage inputs VM and TAM operation are obtained whereas, CM and TIM modes are outcome of current inputs.

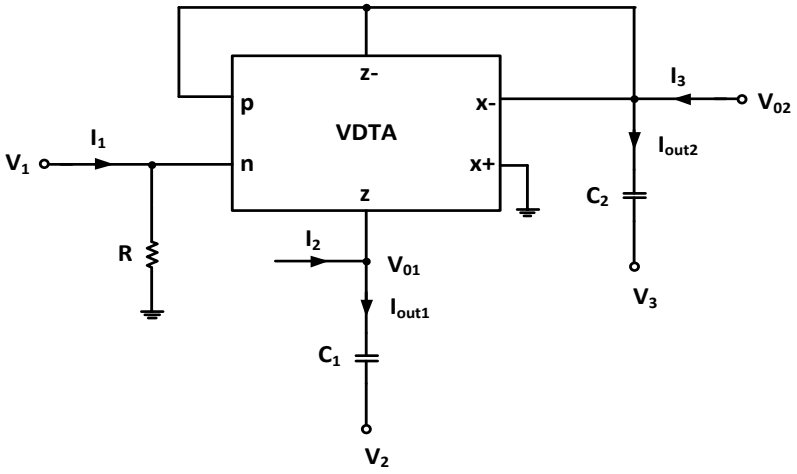


Fig. 4.1 The Proposed Multi-Mode MIMO Filter.

Expression for the voltage outputs obtained by the routine analysis of the proposed circuit are given as

$$V_{01}(s)=\frac{s^2(V_2)+s\left[-(g_{mF}/C_1)V_1+(g_{mF}/C_2)V_2+(g_{mF}/C_1)V_3\right]}{D(s)} \tag{4.1}$$

where, $D(s)=s^2+g_{mF}/C_2\,s+g_{mF}g_{mS}/C_1C_2$ (4.2)

$$V_{02}(s)=\frac{s^2(V_3)+s\left[(g_{mF}/C_2)V_1-(g_{mS}/C_2)V_2\right]+(g_{mF}g_{mS}/C_1C_2)V_1}{D(s)} \tag{4.3}$$

It is evident from Eqn. (4.1) that VM is capable of providing all five filter responses through proper selection of applied input voltages.

Similarly, the current outputs at I_{out1} and I_{out2} for the TAM MIMO configuration respectively can be expressed as

$$I_{out1}(s) = \frac{s^2\left[g_{mF}\left(-V_1 + V_3\right)\right] - s\left(g_{mF}g_{mS}/C_2\right)V_2}{D(s)} \tag{4.4}$$

$$I_{out2}(s) = \frac{s^2\left(g_{mF}V_1 - g_{mS}V_2 - g_{mF}V_3\right) + s\left(g_{mF}g_{mS}/C_1\right)\left(V_1 - V_3\right)}{D(s)} \tag{4.5}$$

Driving circuit with current inputs only results in expressions for V_{01} and V_{02} as given by Eqn. (4.6) and Eqn. (4.7) respectively.

$$V_{01}(s) = \frac{s\left[\left(1/C_1\right)I_2 - \left(g_{mF}/C_1\right)RI_1\right] + \left[\left(g_{mF}/C_1C_2\right) + \left(I_2 + I_3\right)\right]}{D(s)} \tag{4.6}$$

$$V_{02}(s) = \frac{s\left[\left(g_{mF}/C_2\right)RI_1 - \left(1/C_1\right)I_3\right] + \left[\left(g_{mF}g_{mS}/C_1C_2\right)RI_1 - \left(g_{mS}/C_1C_2\right)I_2\right]}{D(s)} \tag{4.7}$$

Likewise, current outputs I_{out1} and I_{out2} for the CM MIMO configuration are given as:

$$I_{out1}(s) = \frac{s^2\left[I_2 - \left(g_{mF}R\right)I_1\right] + s\left[\left(g_{mF}/C_2\right)\left(I_2 + I_3\right)\right]}{D(s)} \tag{4.8}$$

$$I_{out2}(s) = \frac{s^2\left[\left(g_{mF}R\right)I_1 + I_3\right] + s\left[\left(g_{mF}g_{mS}/C_1\right)RI_1 - \left(g_{mS}/C_1\right)I_2\right]}{D(s)} \tag{4.9}$$

The biquadratic and higher order filters are characterized by means of the pass-band gain (H_0), pole frequency (ω_0), the quality factor (Q) which decides the sharpness of the peak and bandwidth (ω_0/Q). The filter parameters may be obtained as

$$\omega_0 = \sqrt{g_{mF}g_{mS}/C_1C_2} \tag{4.10}$$

$$BW = g_{mF}/C_2 \tag{4.11}$$

$$Q = \sqrt{g_{mS}C_2/g_{mF}C_1} \tag{4.12}$$

Since all the filter parameters are dependent on the TC values of the VDTA they may be controlled electronically.

Appropriate input choices, as detailed in Table 4.1, result in various responses in all four modes of operation; namely, the voltage mode (VM), trans-admittance mode (TAM), trans-impedance mode (TIM) and current mode (CM).

Table 4.1 Input Selections for Various Filter Responses.

Mode	**Node 01 Responses**		**Node 02 Responses**	
	Signal Selection	***Transfer Function and Response Type***	***Signal Selection***	***Transfer Function and Response Type***
VM	$V_1 = V_2 = V_{in}$ $V_3 = 0$ $(g_{mF} = g_{mS})$	$\frac{V_{01}(s)}{V_{in}(s)} = \frac{s^2}{D(s)}$ **HP response**	$V_1 = V_2 = V_{in}$ $V_3 = 0$ $(g_{mF} = g_{mS})$	$\frac{V_{02}(s)}{V_{in}(s)} = \frac{g_{mF} g_{mS}/C_1C_2}{D(s)}$ **LP response** $H_0 = 1$
	$-V_1 = V_3 = V_{in}$ $V_2 = 0$	$\frac{V_{01}(s)}{V_{in}(s)} = \frac{2\,g_{mF}/C_1\,s}{D(s)}$ **BP response**	$V_2 = V_{in}$ $V_1 = V_3 = 0$	$\frac{V_{02}(s)}{V_{in}(s)} = \frac{-\,g_{mS}/C_2\,s}{D(s)}$ **Inverting BP response** $H_0 = -\,g_{mS}/g_{mF}$
	NA	NA	$V_3 = V_{in}$ $V_1 = V_2 = 0$	$\frac{V_{02}(s)}{V_{in}(s)} = \frac{s^2}{D(s)}$ **HP response** $H_0 = 1$
	NA	NA	$V_1 = V_2 = V_3 = V_{in}$ $(g_{mF} = g_{mS})$	$\frac{V_{02}(s)}{V_{in}(s)} = \frac{s^2 + g_{mF} g_{mS}/C_1C_2}{D(s)}$ **BS response** $H_0 = 1$
	NA	NA	$V_1 = 2V_2 = V_3 = V_{in}$ $(g_{mF} = g_{mS})$	$\frac{V_{02}(s)}{V_{in}(s)} = \frac{s^2 - g_{mF}/C_2\,s + g_{mF} g_{mS}/C_1C_2}{D(s)}$ **BS response** $H_0 = 1$
TAM	$-V_1 = V_3 = V_{in}$ $V_2 = 0$	$\frac{I_{out1}(s)}{V_{in}(s)} = \frac{2g_{mF}s^2}{D(s)}$ **HP response** $H_0 = 2g_{mF}$	$V_2 = V_{in}$ $V_1 = V_3 = 0$	$\frac{I_{out2}(s)}{V_{in}(s)} = \frac{-s^2 g_{mS}}{D(s)}$ **Inverting HP response** $\lvert H_0 \rvert = g_{mS}$
	$V_2 = V_{in}$ $V_1 = V_3 = 0$	$\frac{I_{out1}(s)}{V_{in}(s)} = \frac{-\,g_{mF} g_{mS}/C_2\,s}{D(s)}$ **Inverting BP response** $\lvert H_0 \rvert = g_{mS}$	$V_1 = -V_3 = V_{in}$ $V_2 = 0$	$\frac{I_{out2}(s)}{V_{in}(s)} = \frac{2\,g_{mF} g_{mS}/C_1\,s}{D(s)}$ **BP response** $H_0 = g_{mS}$

Mode	Node 01 Responses		Node 02 Responses	
	Signal Selection	***Transfer Function and Response Type***	***Signal Selection***	***Transfer Function and Response Type***
TIM	$I_1 = I_{in}$ $I_2 = I_3 = 0$	$\frac{V_{01}(s)}{I_{in}(s)} = \frac{-g_{mF}R/C_1 s}{D(s)}$ **Inverting BP response** $H_0 = R$	$I_3 = I_{in}$ $I_1 = I_2 = 0$	$\frac{V_{02}(s)}{I_{in}(s)} = \frac{1/C_2 s}{D(s)}$ **BP response** $H_0 = 1/g_{mF}$
	$I_3 = I_{in}$ $I_1 = I_2 = 0$	$\frac{V_{01}(s)}{I_{in}(s)} = \frac{g_{mF}/C_1C_2}{D(s)}$ **LP response** $H_0 = 1/g_{mS}$	$I_2 = I_{in}$ $I_1 = I_3 = 0$	$\frac{V_{02}(s)}{I_{in}(s)} = \frac{-g_{mS}/C_1C_2}{D(s)}$ **Inverting LP response** $H_0 = 1/g_{mF}$
CM	$I_1 = I_{in}$ $I_2 = I_3 = 0$	$\frac{I_{out1}(s)}{I_{in}(s)} = \frac{-g_{mF}Rs^2}{D(s)}$ **Inverting HP response** $H_0 = g_{mF}R$	$I_3 = I_{in}$ $I_1 = I_2 = 0$	$\frac{I_{out2}(s)}{I_{in}(s)} = \frac{s^2}{D(s)}$ **HP response** $H_0 = 1$
	$I_3 = I_{in}$ $I_1 = I_2 = 0$	$\frac{I_{out1}(s)}{I_{in}(s)} = \frac{g_{mF}/C_2 s}{D(s)}$ **BP response** $H_0 = 1$	$I_2 = I_{in}$ $I_1 = I_3 = 0$	$\frac{I_{out2}(s)}{I_{in}(s)} = \frac{-g_{mS}/C_1 s}{D(s)}$ **Inverting BP response** $H_0 = 1$

4.2.1 Sensitivity Analysis

Sensitivity analysis is of prime importance as it is a measure to find out the dependence of different filter parameters on the various active and passive components. Filter parameter sensitivities depends on the transconductances of the VDTA as well as the value of the capacitors. Sensitivities of different filter parameters are given by Eqn. (4.13) – Eqn. (4.14) and are found to be low.

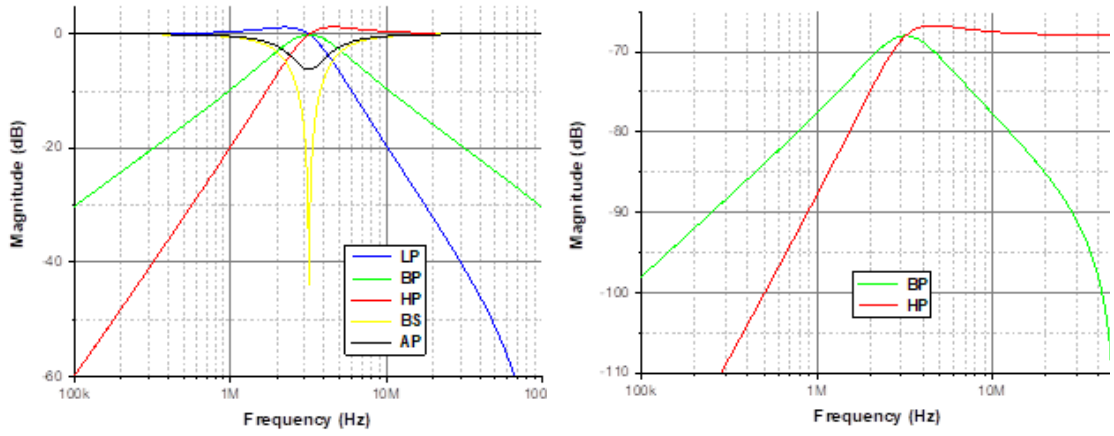
$$S_{g_{mF},g_{mS}}^{\omega_0} = 1/2 \qquad S_{C_1,C_2}^{\omega_0} = -1/2 \tag{4.13}$$

$$S_{g_{mF}}^{BW} = 1 \qquad S_{g_{mS}}^{BW} = 0 \qquad S_{C_1}^{BW} = 0 \qquad S_{C_2}^{BW} = -1 \tag{4.14}$$

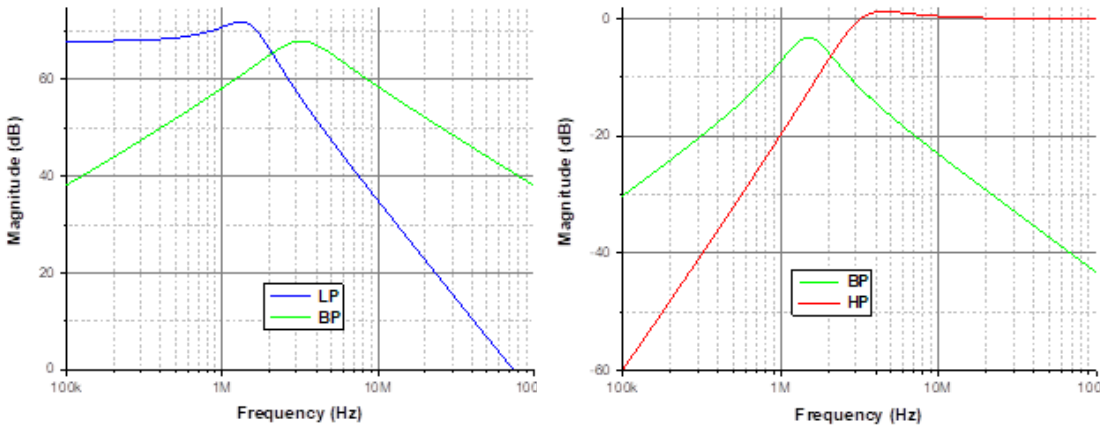
4.2.2 Simulation Results

The functionality of the proposed filter of Fig. 4.1 is validated through simulations using Cadence Virtuoso and gpdk180 nm CMOS process parameters. The CMOS structure of VDTA [27] as given in Fig 2.1(c) was used and the aspect ratios of the MOS transistors are taken as 7.2 µm/0.36 µm for NMOS and 14.4 µm/0.36 µm for PMOS. The supply voltage and the biasing current are considered to be ±0.7 V and 10 µA respectively. The resistor and capacitor values are chosen as R = 1 kΩ and C_1 = C_2 = 20 pF. Transconductance values are found to be gm1 = gm2 = 400 µA/V.

The magnitude responses of the proposed filter are shown in Fig. 4.2. The VM responses are depicted in Fig. 4.2(a) and TAM responses in Fig. 4.2(b). Driving circuit with appropriate current signals the TIM and CM responses are obtained and are shown in Figs. 4.2(c) and (d) respectively. The simulated value of f_0 in various modes of operation is observed to be in the range of 2.5 MHz - 3.3 MHz as against theoretical value of 3.18 MHz.



(a) (b)



(c) (d)

Fig. 4.2 Magnitude Responses of (a) LP, BP, HP, BS and AP in VM; (b) LP, BP in TAM, (c) LP, BP in TIM (d) HP, BP in CM.

To show the electronic tunability of proposed filter biasing current is varied from 5 µA to 15 µA in steps of 5 µA and corresponding BP responses in VM mode are shown in Fig. 4.3. It may clearly be observed that changing the bias current results in change in frequency. Similar tuning for other modes can also be obtained.

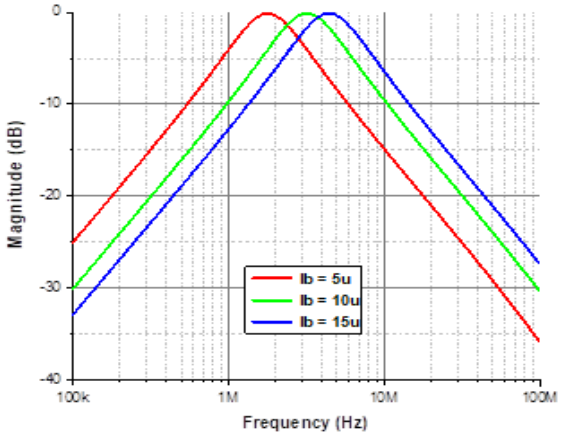


Fig. 4.3 Electronic Tuning of BP Filter Frequency in VM Mode.

Natural phenomena can be modelled more precisely using fractional calculus [54-56]. For instance, first- order and biquadratic filters provides -20 dB/Decade and -40 dB/decade stopband attenuation respectively, but what if in-between value is desired. So, in order to bridge that gap, focus has been shifting to the fractional order filters.

4.3 Proposed FOF-I

The first proposed voltage mode multiple input single output is universal in nature and is capable of providing all the five filter responses simultaneously; namely, fractional order low pass filter, fractional order band pass filter, fractional order high pass filter, fractional order band stop/reject filter and fractional order all pass filter. The proposition is based on a single VDTA and two fractional order capacitors as shown in Fig. 4.4.

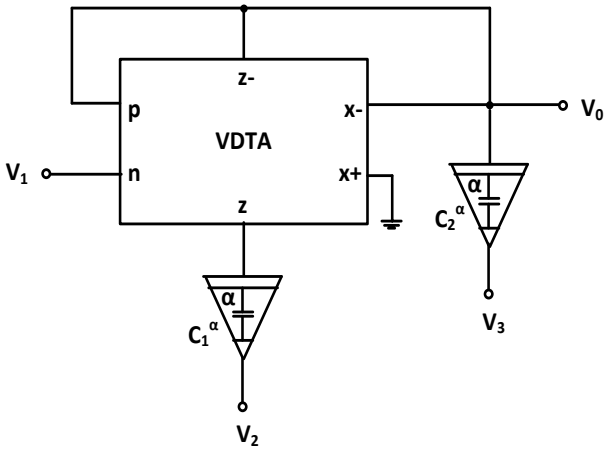


Fig. 4.4 Proposed FOF-I.

Routine analysis of the circuit in Fig. 4.4 leads to the following voltage output expression

$$V_O(s) = \frac{s^{2\alpha}(V_3) + s^{\alpha}\left[\left(g_{mF}/C_2^{\alpha}\right)V_1 - \left(g_{mS}/C_2^{\alpha}\right)V_2\right] + \left(g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\right)V_1}{D(s)} \qquad (4.15)$$

where, $D(s) = s^{2\alpha} + g_{mF}/C_2^{\alpha}\, s^{\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}$ (4.16)

The requisite input selections and the corresponding voltage transfer functions for all five FOFs are listed in Table 4.2.

Table 4.2 Input Selections for Various FOF Responses and Corresponding Transfer Functions.

FOF Response	**Signal Selection**	**Voltage Transfer Function**
FLPF	$V_1 = V_2 = V_{in}$ $V_3 = 0$ $(g_{mF} = g_{mS})$	$\frac{V_0(s)}{V_{in}(s)} = \frac{g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}}{D(s)}$
FBPF	$V_2 = V_{in}$ $V_1 = V_3 = 0$	$\frac{V_0(s)}{V_{in}(s)} = \frac{-g_{mS}/C_2^{\alpha}\, s^{\alpha}}{D(s)}$
FHPF	$V_3 = V_{in}$ $V_1 = V_2 = 0$	$\frac{V_0(s)}{V_{in}(s)} = \frac{s^{2\alpha}}{D(s)}$
FBSF	$V_1 = V_2 = V_3 = V_{in}$ $(g_{mF} = g_{mS})$	$\frac{V_0(s)}{V_{in}(s)} = \frac{s^{2\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}}{D(s)}$
FAPF	$V_1 = 2V_2 = V_3 = V_{in}$ $(g_{mF} = g_{mS})$	$\frac{V_0(s)}{V_{in}(s)} = \frac{s^{2\alpha} - g_{mF}/C_2^{\alpha}\, s^{\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}}{D(s)}$

A fractional order filter is characterized by means of the following critical frequencies [86]:

- the 3 dB frequency; where power drops down to $1/\sqrt{2}$
- the peak frequency; corresponding to the point at which $|T(j\omega)|$ is maximum/minimum
- the right phase frequency at which phase corresponds to ± π/2

The expression for 3 dB frequency for any of the fractional order filter responses may be obtained by equating the corresponding magnitude function to 0.707 and peak frequency may be determined by differentiating the magnitude of function with respect to ω^{α} and equating it to zero. On the other hand, the right phase frequency may be computed by equating the phase function to $\pm\pi/2$.

4.3.1 The Fractional Order Low Pass Filter

The transfer function of the fractional order low pass filter is expressed as:

$$T(s)\big|_{FLPF} = \frac{V_O(s)}{V_{in}(s)}\bigg|_{FLPF} = \frac{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha} + g_{mF}/C_2^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.17}$$

The magnitude and phase functions of Eqn. (4.17) can be expressed by Eqn. (4.18) and Eqn. (4.19) respectively.

$$\left|T(j\omega)\right|_{FLPF} = \frac{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{\left[\begin{array}{l}\omega^{4\alpha} + 2\,g_{mF}/C_2^{\alpha}\,\omega^{3\alpha}\cos\alpha\,\pi/2 + \omega^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right. \\ \left. + g_{mF}^2/C_2^{2\alpha}\right) + 2\,g_{mF}/C_2^{\alpha}\; g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\;\omega^{\alpha}\cos\alpha\,\pi/2 \\ + g_{mF}^2 g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}} \tag{4.18}$$

$$\underline{\left|T(j\omega)\right|_{FLPF}} = -\tan^{-1}\frac{\sin\alpha\pi\omega^{2\alpha} + g_{mF}/C_2^{\alpha}\omega^{\alpha}\sin\alpha\pi/2}{\cos\alpha\pi\omega^{2\alpha} + g_{mF}/C_2^{\alpha}\omega^{\alpha}\cos\alpha\pi/2 + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.19}$$

Analogous to conventional integer order filters, the 3 dB frequency is obtained by equating the magnitude to 0.707 and is given as:

$$\begin{array}{l}\omega_{3dB(FLPF)}^{4\alpha} + 2\,g_{mF}/C_2^{\alpha}\,\omega_{3dB(FLPF)}^{3\alpha}\cos\pi/4 + \omega_{3dB(FLPF)}^{2\alpha}\left[g_{mF}^2/C_2^{2\alpha} + 2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\right. \\ \left.\cos\pi/2\right] + 2\,g_{mF}/C_2^{\alpha}\;g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\;\omega_{3dB(FLPF)}^{\alpha}\cos\pi/4 - g_{mF}^2 g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha} = 0\end{array} \tag{4.20}$$

The peak frequency corresponds to the point where magnitude is maximum/minimum and is determined by equating the derivative of magnitude function to zero. The ω_m for FLPF is thus computed as:

$$\omega_{p(FLPF)}^{3\alpha} + 3/2\, g_{mF}/C_2^{\alpha} \cos\pi/4\, \omega_{p(FLPF)}^{2\alpha} + \omega_{p(FLPF)}^{\alpha}\left[1/2\, g_{mF}^2/C_2^{2\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha} \cos\pi/2\right] + 1/2\, g_{mF}/C_2^{\alpha}\, g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha} \cos\pi/4 = 0 \tag{4.21}$$

The frequency at which the phase value of the function is $\pi/2$ corresponds to right phase frequency. The ω_{rp} for proposed FLPF may be computed from Eqn. (4.19) as:

$$\omega_{rp(FLPF)} = \left(\frac{-1/2\, g_{mF}/C_2^{\alpha} \cos\pi/4 \pm \sqrt{1/4\, g_{mF}^2/C_2^{2\alpha} \cos^2\pi/4 - g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha} \cos\pi/2}}{\cos\pi/2} \right)^2 \tag{4.22}$$

4.3.2 The Fractional Order Band Pass Filter

The transfer function of the fractional order band pass filter is expressed as:

$$T(s)\big|_{FBPF} = \frac{V_O(s)}{V_{in}(s)}\bigg|_{FBPF} = \frac{-g_{mS}/C_2^{\alpha}\, s^{\alpha}}{s^{2\alpha} + g_{mF}/C_2^{\alpha}\, s^{\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}} \tag{4.23}$$

The magnitude and phase functions for the fractional order band pass filter may be obtained from Eqn. (4.23) and are given by Eqn. (4.24) and Eqn. (4.25) respectively.

$$\left|T(j\omega)\right|_{FLPF} = \frac{g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}}{\left[\begin{array}{l} \omega^{4\alpha} + 2\, g_{mF}/C_2^{\alpha}\, \omega^{3\alpha} \cos\pi/4 + \omega^{2\alpha}\left(2\, g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha} \cos\pi/2 \right. \\ \left. + g_{mF}^2/C_2^{2\alpha}\right) + 2\, g_{mF}/C_2^{\alpha}\, g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}\, \omega^{\alpha} \cos\pi/4 \\ + g_{mF}^2 g_{mS}^2/C_1^{2\alpha} C_2^{2\alpha} \end{array}\right]^{1/2}} \tag{4.24}$$

$$\underline{\left|T(j\omega)\right|_{FLPF}} = -\tan^{-1} \frac{\sin\alpha\pi\omega^{2\alpha} + g_{mF}/C_1^{\alpha}\omega^{\alpha} \sin\alpha\pi/2}{\cos\alpha\pi\omega^{2\alpha} + g_{mF}/C_1^{\alpha}\omega^{\alpha} \cos\alpha\pi/2 + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}} \tag{4.25}$$

The 3 dB frequency of fractional order band pass filter may be derived as:

$$\begin{aligned}&\omega_{3\mathrm{dB}(FBPF)}^{4\alpha}+2\,g_{mF}/C_2^{\alpha}\,\omega_{3\mathrm{dB}(FBPF)}^{3\alpha}\cos\pi/4+\omega_{3\mathrm{dB}(FBPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\&\left.-g_{mF}^2/C_2^{2\alpha}-8\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos^2\pi/4-g_1/C_2\sqrt{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}\cos\pi/4\right)\\&+2\,g_{mF}/C_2^{\alpha}\,2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3\mathrm{dB}(FLPF)}^{\alpha}\cos\pi/4+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{aligned}\tag{4.26}$$

The peak frequency of the fractional order band pass filter may be obtained from Eqn. (4.24).

$$\begin{aligned}&\omega_{\mathrm{p}(FBPF)}^{4\alpha}+g_{mF}/C_2^{\alpha}\cos\pi/4\,\omega_{\mathrm{p}(FBPF)}^{3\alpha}-g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\omega_{\mathrm{p}(FBPF)}^{\alpha}\cos\pi/4\\&-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{aligned}\tag{4.27}$$

The right phase frequency for the fractional order band pass filter can be expressed as

$$\omega_{rp(FBPF)}=\left(\frac{-1/2\,g_{mF}/C_2^{\alpha}+\sqrt{1/4\,g_{mF}^2/C_2^{2\alpha}-g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos^2\pi/4}}{\cos\pi/4}\right)^2\tag{4.28}$$

4.3.3 The Fractional Order High Pass Filter

The transfer function of the fractional order high pass filter is expressed as:

$$T(s)\big|_{FHPF}=\frac{V_O(s)}{V_{in}(s)}\bigg|_{FHPF}=\frac{s^{2\alpha}}{s^{2\alpha}+g_{mF}/C_2^{\alpha}\,s^{\alpha}+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}\tag{4.29}$$

The 3 dB, peak and right phase frequencies for fractional order high pass filter may be obtained by deriving magnitude and phase functions from Eqn. (4.29) as given by Eqn. (4.30) - Eqn. (4.31) respectively

$$\left|T\left(j\omega\right)\right|_{FHPF}=\frac{\omega^{2\alpha}}{\left[\begin{array}{l}\omega^{4\alpha}+2\,g_{mF}/C_2^{\alpha}\,\omega^{3\alpha}\cos\pi/4+\omega^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\ \left.+g_{mF}^2/C_2^{2\alpha}\right)+2\,g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega^{\alpha}\cos\pi/4\\ +g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}} \tag{4.30}$$

$$\underline{\left|T\left(j\omega\right)\right|_{FHPF}}=\tan^{-1}\frac{g_{mF}/C_2^{\alpha}\omega^{\alpha}\sin\alpha\pi/2+\sin\alpha\pi\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{1+g_{mF}/C_2^{\alpha}\omega^{\alpha}\cos\alpha\pi/2+\cos\alpha\pi g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.31}$$

The 3 dB frequency expression of the fractional order high pass filter may be expressed as

$$\begin{array}{l}\omega_{3\mathrm{dB}(FHPF)}^{4\alpha}-2\,g_{mF}/C_2^{\alpha}\,\omega_{3\mathrm{dB}(FHPF)}^{3\alpha}\cos\pi/4-\omega_{3\mathrm{dB}(FHPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\ \left.+g_{mF}^2/C_2^{2\alpha}\right)-2\,g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3\mathrm{dB}(FHPF)}^{\alpha}\cos\pi/4-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{array} \tag{4.32}$$

The peak frequency for the fractional order high pass filter may be determined as

$$\begin{array}{l}g_{mF}/C_2^{\alpha}\cos\pi/4\,\omega_{p(FHPF)}^{4\alpha}+\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2+g_{mF}^2/C_2^{2\alpha}\right)\omega_{p(FHPF)}^{3\alpha}\\ +3\,g_{mF}/C_2^{\alpha}\,2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{p(FHPF)}^{2\alpha}+2\,g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\,\omega_{p(FHPF)}^{\alpha}=0\end{array} \tag{4.33}$$

The right phase frequency may be obtained by equating the phase to ±π/2.

$$\omega_{rp(FHPF)}=\left(\frac{-1/2\,g_{mF}/C_2^{\alpha}\cos\pi/4+\sqrt{1/4\,g_{mF}^2/C_2^{2\alpha}\cos^2\pi/4-g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2}}{2}\right)^2 \tag{4.34}$$

4.3.4 The Fractional Order Band Stop/Reject Filter

The transfer function of the fractional order band stop/reject filter is expressed as:

$$T\left(s\right)\Big|_{FBSF}=\left.\frac{V_O\left(s\right)}{V_{in}\left(s\right)}\right|_{FBSF}=\frac{s^{2\alpha}+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha}+g_{mF}/C_2^{\alpha}\,s^{\alpha}+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.35}$$

The magnitude and phase functions using Eqn. (4.35) may be expressed as:

$$\left|T\left(j\omega\right)\right|_{FLPF}=\frac{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{\left[\begin{array}{l}\omega^{4\alpha}+2g_{mF}/C_2^{\alpha}\,\omega^{3\alpha}\cos\pi/4+\omega^{2\alpha}\left(2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\\left.+g_{mF}^2/C_2^{2\alpha}\right)+2g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega^{\alpha}\cos\pi/4\\+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}} \tag{4.36}$$

$$\underline{\left|T\left(j\omega\right)\right|_{FLPF}}=-\tan^{-1}\frac{\sin\alpha\pi\omega^{2\alpha}+g_{mF}/C_1^{\alpha}\omega^{\alpha}\sin\alpha\pi/2}{\cos\alpha\pi\omega^{2\alpha}+g_{mF}/C_1^{\alpha}\omega^{\alpha}\cos\alpha\pi/2+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.37}$$

Equating Eqn. (4.36) to 0.707 the expression for 3 dB frequency of fractional order band stop filter may be obtained as:

$$\begin{array}{l}\omega_{3\mathrm{dB}(FBSF)}^{4\alpha}-2g_{mF}/C_2^{\alpha}\,\omega_{3\mathrm{dB}(FBSF)}^{3\alpha}\cos\pi/4+\omega_{3\mathrm{dB}(FBSF)}^{2\alpha}\left(2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\\left.-g_{mF}^2/C_2^{2\alpha}\right)-2g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3\mathrm{dB}(FBSF)}^{\alpha}\cos\pi/4+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{array} \tag{4.38}$$

Similarly, peak frequency corresponding to point where magnitude is maximum/minimum may be determined by differentiating and equating the magnitude to zero.

$$\begin{array}{l}\cos\pi/4\,\omega_{p(FBSF)}^{6\alpha}+g_{mF}/C_2^{\alpha}\,\omega_{p(FBSF)}^{5\alpha}+\left(3g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/4\right.\\\left.-2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\cos\pi/4\right)\omega_{p(FBSF)}^{4\alpha}+\left(-3g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\cos\pi/4\right.\\\left.+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\cos\alpha\pi\cos\pi/4\right)\omega_{p(FBSF)}^{2\alpha}-g_{mF}/C_2^{\alpha}\,g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\\\omega_{p(FBSF)}^{\alpha}-3g_{mF}^3g_{mS}^3/C_1^{3\alpha}C_2^{3\alpha}\cos\pi/4=0\end{array} \tag{4.39}$$

4.3.5 The Fractional Order All Pass Filter

The transfer function of the fractional order all pass filter is expressed as:

$$T\left(s\right)\Big|_{FAPF}=\frac{V_O\left(s\right)}{V_{in}\left(s\right)}\Bigg|_{FAPF}=\frac{s^{2\alpha}-g_{mS}/C_2^{\alpha}\,s^{\alpha}+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha}+g_{mF}/C_2^{\alpha}\,s^{\alpha}+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.40}$$

The magnitude and phase functions using Eqn. (4.40) may be expressed as:

$$\left|T(j\omega)\right|_{FAPF}=\frac{\left[\begin{array}{l}\omega^{4\alpha}-2\,g_{mS}/C_2^{\alpha}\,\omega^{3\alpha}\cos\alpha\,\pi/2+\omega^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.\\ \left.+g_{mS}^2/C_2^{2\alpha}\right)-2\,g_{mS}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega^{\alpha}\cos\alpha\,\pi/2\\ +g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}}{\left[\begin{array}{l}\omega^{4\alpha}+2\,g_{mF}/C_2^{\alpha}\,\omega^{3\alpha}\cos\alpha\,\pi/2+\omega^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.\\ \left.+g_{mF}^2/C_2^{2\alpha}\right)+2\,g_{mF}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega^{\alpha}\cos\alpha\,\pi/2\\ +g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}} \tag{4.41}$$

$$\underline{\left|T(j\omega)\right|_{FLPF}}=-\tan^{-1}\frac{\sin\alpha\pi\omega^{2\alpha}+g_{mF}/C_1^{\alpha}\omega^{\alpha}\sin\alpha\pi/2}{\cos\alpha\pi\omega^{2\alpha}+g_{mF}/C_1^{\alpha}\omega^{\alpha}\cos\alpha\pi/2+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.42}$$

Equating Eqn. (4.41) to 0.707 the expression for 3 dB frequency of fractional order band stop filter may be obtained as:

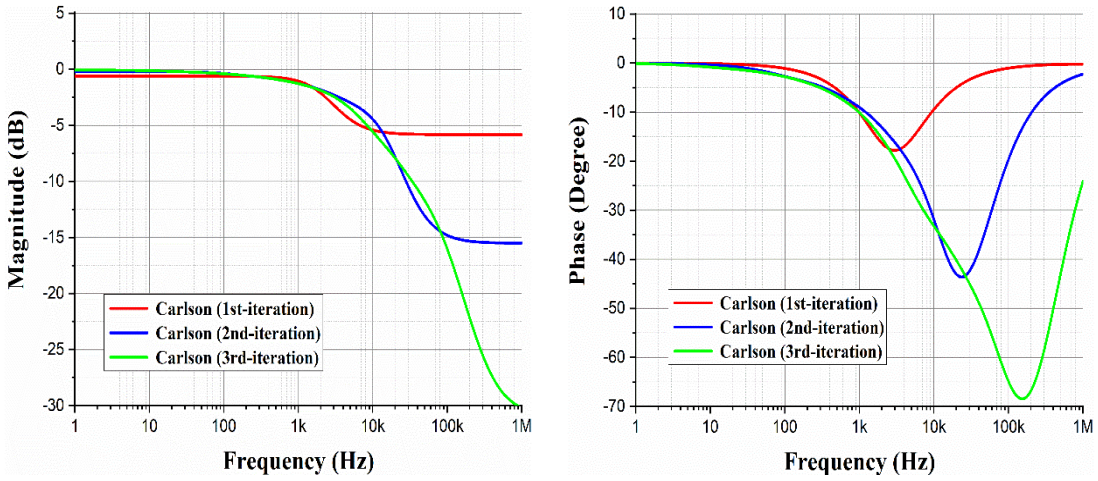
$$\begin{array}{l}\omega_{3\mathrm{dB}(FAPF)}^{4\alpha}+2\,g_{mS}/C_2^{\alpha}\,\omega_{3\mathrm{dB}(FAPF)}^{3\alpha}\cos\pi/4+\omega_{3\mathrm{dB}(FAPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\pi/2\right.\\ \left.+g_{mS}^2/C_2^{2\alpha}\right)+2\,g_{mS}/C_2^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3\mathrm{dB}(FAPF)}^{\alpha}\cos\pi/4+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{array} \tag{4.43}$$

4.3.6 Simulation Results

Functionality of the presented VDTA based FOF is justified through simulations using Cadence Virtuoso. The CMOS based implementation of VDTA [27] is used for simulations with 0.18 μm CMOS process parameters. The VDTA is characterized for bias current of 10 μA and the supply voltages are considered to be ± 0.7 V. The aspect ratios of NMOS and PMOS transistors are set to be 7.2μm/3.6μm and 14.4μm/3.6μm respectively.

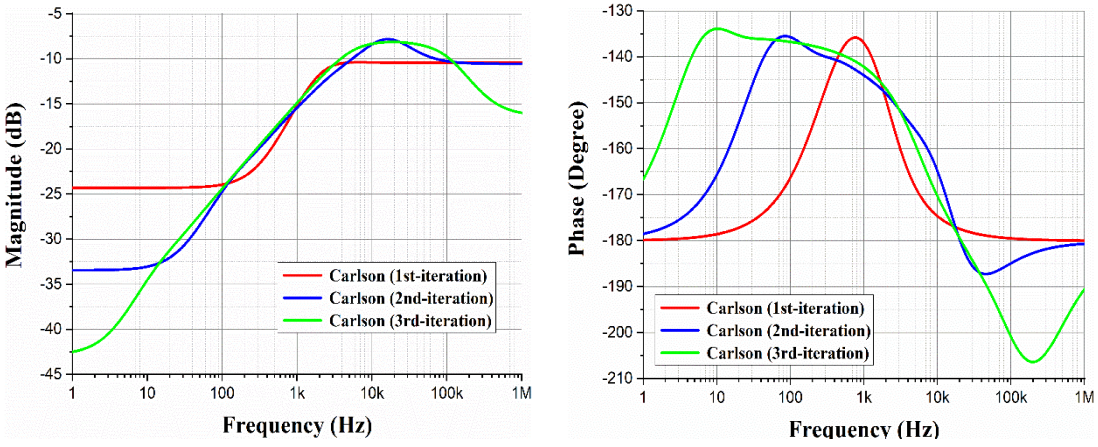
Using the emulated FCs of 1 μ℧/s^{α} with α = 0.5 all the five filter functions namely fractional order low pass filter, fractional order band pass filter, fractional order high pass filter, fractional order band stop filter and fractional order all pass filter are simulated and their corresponding magnitude and phase functions are depicted in Fig. 4.5 through Fig. 4.9 respectively. The simulated filter parameters for all five

responses have been recorded in Table 4.3. For the sake of comparison, the theoretical values, as presented in Table 4.3, are computed for fractional order α = 0.5 using mathematical relations of filter parameters. It is pertinent to mention that some of the critical frequencies are not observable (NO) for α = 0.5 as theoretical results lead to negative/complex frequencies.



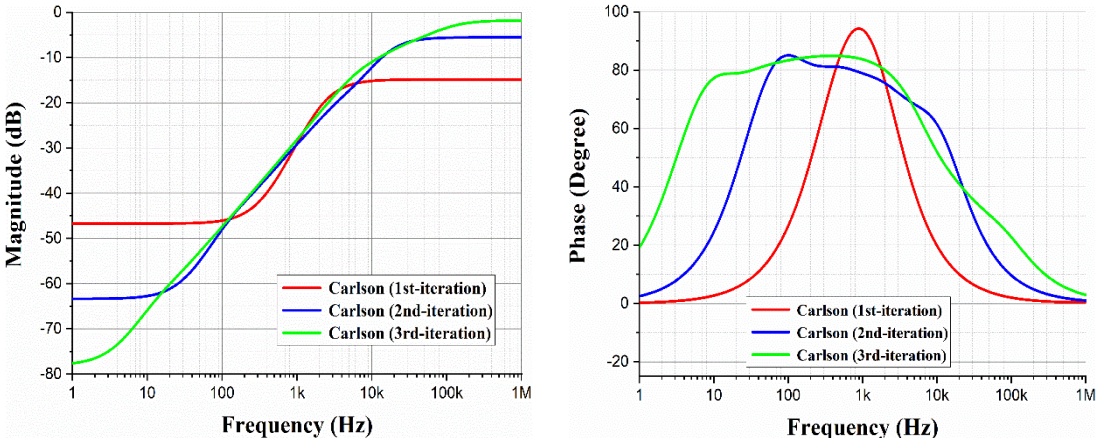
(a) (b)

Fig. 4.5 Frequency Response for FLPF (a) Magnitude (b) Phase.



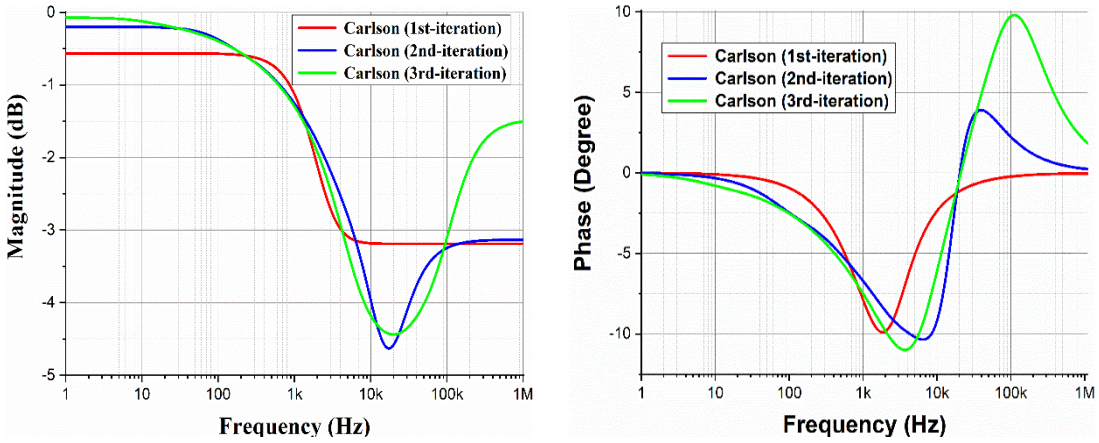
(a) (b)

Fig. 4.6 Frequency Response for FBPF (a) Magnitude (b) Phase.



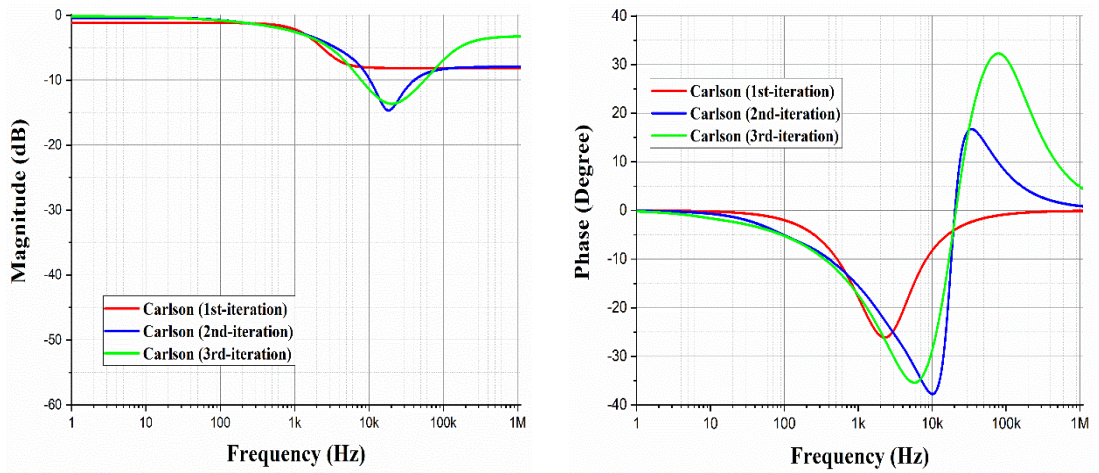
(a) (b)

Fig. 4.7 Frequency Response for FHPF (a) Magnitude (b) Phase.



(a) (b)

Fig. 4.8 Frequency Response for FBSF (a) Magnitude (b) Phase.



(a) (b)

Fig. 4.9 Frequency Response for FAPF (a) Magnitude (b) Phase.

Table 4.3 Performance Parameters for FOFs for 1 μ℧/s^{α} ($\alpha = 0.5$).

Filter Response	Parameters	Theoretical Results	Simulated Results		
			Carlson 1st-Iteration	Carlson 2nd-Iteration	Carlson 3rd-Iteration
FLPF	DC Gain (dB)	0	-0.60	-0.20	-0.07
	3 dB Frequency (kHz)	5.10	3.50	5.81	4.19
	Peak Frequency (kHz)	Not defined	NO	NO	NO
FBPF	DC Gain (dB)	-7.66	-10.39	-7.82	-8.13
	Lower 3 dB Frequency (kHz)	4.00	1.38	4.05	2.69
	Centre Frequency (kHz)	25.46	7.05	16.44	19.41
	Higher 3 dB Frequency (kHz)	162.22	NO	NO	151.82
FHPF	DC Gain (dB)	0	-14.86	-5.53	-1.8
	3 dB Frequency (kHz)	127.15	3.16	17.64	59.83
	Peak Frequency (Hz)	Not defined	NO	NO	NO
FBSF	DC Gain (dB)	- 4.65	-4.95	- 4.63	-4.44
	Lower 3 dB Frequency (kHz)	5.76	1.93	6.57	4.39
	Centre Frequency (kHz)	16.70	NO	18.41	20.42
	Higher 3 dB Frequency (kHz)	112.54	NO	131.07	101.79

It is evident from the Table 4.3 that as the number of iterations is increased, the filter parameters such as gain, 3 dB and/or center frequency right phase frequency as applicable for a given configuration approach the theoretical values.

4.4 Proposed FOF-II

The second proposed voltage mode single input single output fractional order filter comprises of a single VDTA and two grounded fractional order capacitors only as shown in Fig. 4.10.

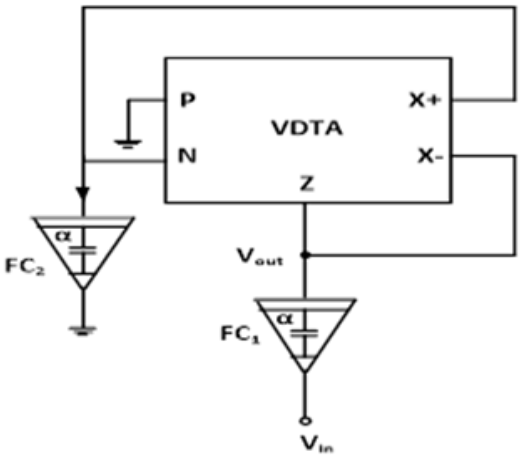


Fig. 4.10 Proposed FOF-II.

Routine analysis of the proposed circuit suggests that it provides fractional order low pass filter, fractional order band pass filter and fractional order high pass filter responses simultaneously.

$$T(s)\big|_{FHPF} = \frac{V_{out}(s)}{V_{in}(s)}\bigg|_{FHPF} = \frac{s^{2\alpha}}{D(s)} \tag{4.44}$$

where, $D(s) = s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF} g_{mS}/C_1^{\alpha} C_2^{\alpha}$ (4.45)

represents the characteristic equation of the filter and α is the fractional order of the capacitor.

The 3 dB, peak and right phase frequencies for fractional order high pass filter may be obtained by deriving magnitude and phase functions from Eqn. (4.44) as given by Eqn. (4.46) - Eqn. (4.47) respectively

$$\left|T\left(j\omega\right)\right|_{FHPF}=\frac{\omega^{2\alpha}}{\left[\begin{array}{l}\omega^{4\alpha}+2g_{mS}/C_1^{\alpha}\,\omega^{3\alpha}\cos\alpha\pi/2+\omega^{2\alpha}\left(2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi+\right.\\ \left.g_{mS}^2/C_1^{2\alpha}\right)+2\omega^{\alpha}g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,g_{mS}/C_1^{\alpha}\cos\alpha\pi/2\\ +g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\end{array}\right]^{1/2}} \tag{4.46}$$

$$\underline{\left|T\left(j\omega\right)\right|_{FHPF}}=\tan^{-1}\frac{g_{mS}/C_1^{\alpha}\omega^{\alpha}\sin\alpha\pi/2+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\sin\alpha\pi}{\omega^{2\alpha}+g_{mS}/C_1^{\alpha}\omega^{\alpha}\cos\alpha\pi/2+g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi} \tag{4.47}$$

The 3 dB frequency of fractional order high pass filter may be expressed as

$$\begin{array}{l}\omega_{3dB(FHPF)}^{4\alpha}-2g_{mS}/C_1^{\alpha}\,\omega_{3dB(FHPF)}^{3\alpha}\cos\alpha\pi/2-\omega_{3dB(FHPF)}^{2\alpha}\left(2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi+\right.\\ \left.g_{mS}^2/C_1^{2\alpha}\right)-2g_{mS}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3dB(FHPF)}^{\alpha}\cos\alpha\pi/2-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0\end{array} \tag{4.48}$$

Peak frequency for the fractional order high pass filter may be determined as

$$\begin{array}{l}g_{mS}/C_1^{\alpha}\cos\alpha\pi/2\,\omega_{p(FHPF)}^{4\alpha}+\omega_{p(FHPF)}^{3\alpha}\left(2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi+g_{mS}^2/C_1^{2\alpha}\right)\\ +3g_{mS}/C_1^{\alpha}\,2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{p(FHPF)}^{2\alpha}+2\,g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\,\omega_{p(FHPF)}^{\alpha}=0\end{array} \tag{4.49}$$

Right phase frequency may be obtained by equating the phase to ±π/2.

$$\omega_{rp(FHPF)}=\frac{\left(-0.5g_{mS}/C_1^{\alpha}\cos\alpha\pi/2+0.5\sqrt{g_{mS}^2/C_1^{2\alpha}\cos^2\alpha\pi/2-4g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi}\right)^{1/\alpha}}{2} \tag{4.50}$$

It is worth noting that various critical frequencies of all fractional order filter responses are dependent on the transconductances of the VDTA, which in-turn can be varied as per the biasing currents. Hence critical frequencies of proposed fractional order filter are electronically tunable.

4.4.1 Sensitivity Analysis

Sensitivity analysis is a measure to find out the relative change in filter responses with change in circuit parameters; that is the external passive components, transconductance values which further depends on the biasing currents.

Transfer function sensitivities of the proposed fractional order high pass filter have been computed with respect to capacitors used in the circuit and the transconductances of VDTA are computed and expressed as Eqn. (4.51) - Eqn. (4.55). Transfer function sensitivities are dependant of value of the fractional order capacitors and transconductances of the VDTA.

$$S_{\alpha}^{T(s)|_{FHPF}} = \frac{\alpha ln(s)\left(g_{mS}/C_1^{\alpha}\, s^{\alpha} + 2g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\right)}{s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.51}$$

$$S_{C_1^{\alpha}}^{T(s)|_{FHPF}} = \frac{g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.52}$$

$$S_{C_2^{\alpha}}^{T(s)|_{FHPF}} = \frac{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.53}$$

$$S_{g_{mF}}^{T(s)|_{FHPF}} = \frac{-\left(g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\right)}{s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.54}$$

$$S_{g_{mS}}^{T(s)|_{FHPF}} = \frac{-g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{s^{2\alpha} + g_{mS}/C_1^{\alpha}\, s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}} \tag{4.55}$$

4.4.2 Stability Analysis

The fractional order filters have an extended stability region based on the location of the roots [96,109], in contrast to integer order filters. In this work, roots of the characteristic equation Eqn. (4.45) are positive and are located at $r_{1,2} = \frac{-g_{mF}/C_1 \pm \sqrt{g_{mF}^2/C_1^2 - 4\left(g_{mF}g_{mS}/C_1C_2\right)}}{2} = g_{1,2}e^{j\pi}$ and $r_{1,2} = \sqrt{g_{mF}g_{mS}/C_1C_2} = g_{1,2}e^{\pm j\Delta}$ respectively, hence proposed fractional order filter is stable for $|\Delta| > \alpha\pi/2$ region in w plane for α ranging from 0.5 to 0.9. Corresponding pole frequencies are given by $g_{1,2}^{1/\alpha}$ and $(g_{mF}g_{mS}/C_1C_2)^{1/2\alpha}$ respectively. The resulting quality factors are $\frac{-1}{2\cos\pi/\alpha}$ and $\frac{-1}{2\cos\Delta/\alpha}$ respectively. Pictorial representation of stable and unstable regions is depicted in Fig. 4.11 for α ranging from 0.5 to 0.9.

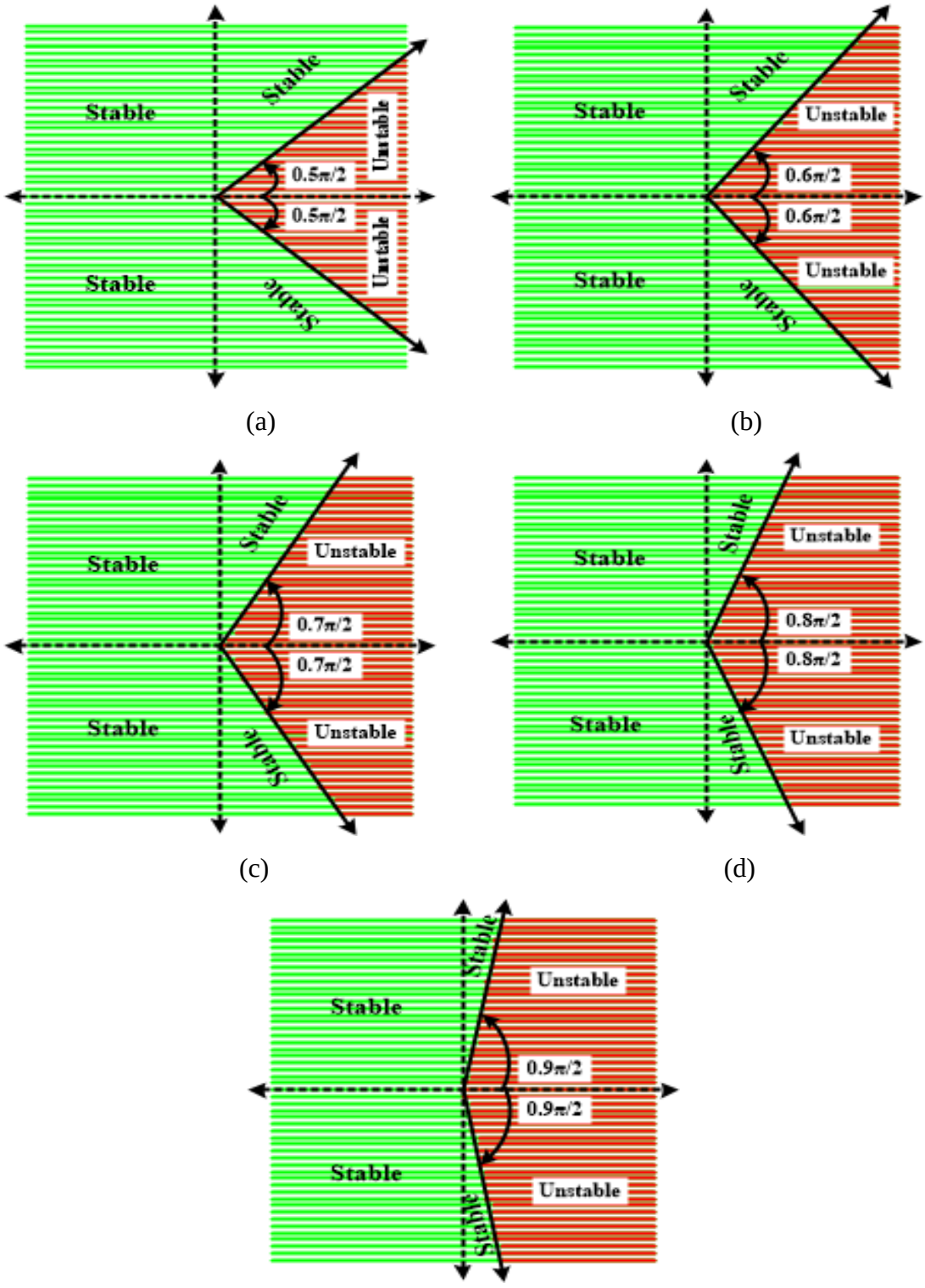


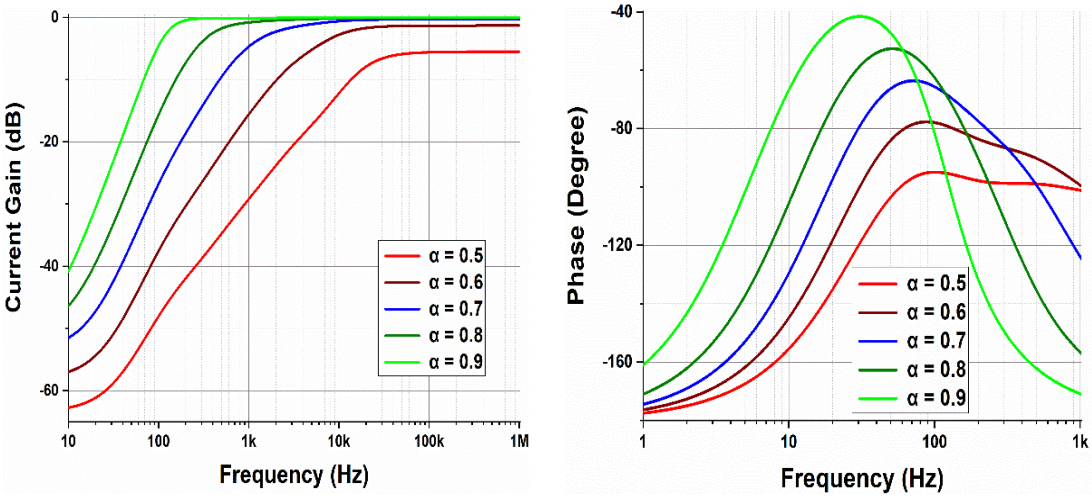
Fig. 4.11 Stability Region in w Plane for α = (a) 0.5 (b) 0.6 (c) 0.7 (d) 0.8 (e) 0.9.

4.4.3 Simulation Results

Proposed VDTA based FOF-II topology has been tested for its functionality through simulations carried out by Virtuoso from Cadence Spectre tool suite using 180 nm (gpdk) technology node.

Using the FCs simulated in Section 2.3.2 magnitude and phase responses of the FHPF for the orders ranging from 0.5 to 0.9 are obtained as shown in Fig. 4.12. It may be observed from the magnitude response that likewise conventional integer order filters, as the order of the fractional order capacitor increases, fractional order high pass filter approaches the ideal brick wall response. Furthermore, 3 dB frequency tends to reduce as the order of the FC increases. It may be further noted from the phase response that higher the fractional order, lower is the right phase frequency. These results are summarized in Table 4.4. All the critical frequencies are observed to be in close agreement with theoretical values.

The magnitude and phase responses of FHPF are illustrated in Fig. 4.12 and the critical frequencies are listed in Table 4.4.



(a) (b)

Fig. 4.12 Frequency Response for FHPF (a) Magnitude (b) Phase.

Table 4.4 Performance Parameters for Fractional Order High Pass Filter.

Fractional Order	DC Gain (dB)		3 dB Frequency (Hz)		Peak Frequency (Hz)		Right Phase Frequency (Hz)	
	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated
0.5	-5.34	-5.52	127.15 k	17.61 k	NA	NA	NA	NA
0.6	-1.14	-1.31	9.80 k	6.27 k	NA	NA	558.21	491.03
0.7	-0.13	-0.29	1.47 k	1.40 k	NA	NA	374.19	360.62
0.8	-0.02	-0.06	345.89	354.16	NA	NA	201.40	198.35
0.9	-0.00	-0.01	114.80	115.99	NA	NA	110.21	111.56

The FHPF displays a reduction in the 3 dB frequency and enhancement in the gain as the order of the fractional order capacitor increases. Furthermore, right phase frequency reduces with increase in order of the filter. The simulated fractional order filter parameters are in found to be in close agreement with the theoretical values except for $\alpha = 0.5$ and 0.6.

4.5 Proposed FOF-III

The third proposed current mode single input multiple output is multifunction in nature and is capable of providing; fractional order low pass filter, fractional order band pass filter, fractional order high pass filter responses simultaneously. The proposition is based on a single VDTA and two grounded fractional order capacitors as shown in Fig. 4.13.

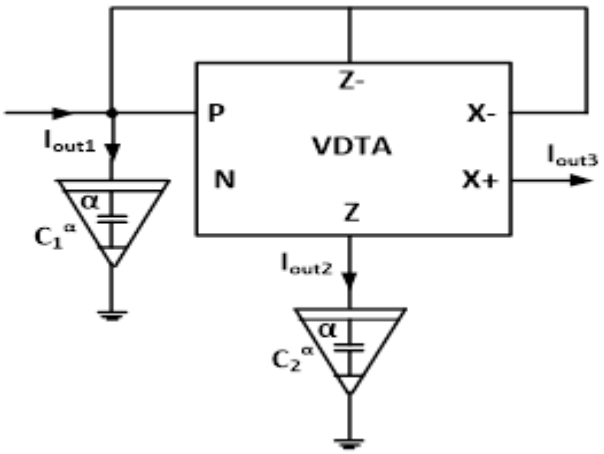


Fig. 4.13 Proposed FOF-III.

The proposed CM SIMO FOF comprises of a single VDTA and two grounded FCs only as shown in Fig. 4.13. Routine analysis of the proposed circuit suggests that it provides FLPF, FBPF and FHPF responses simultaneously.

$$T(s)\big|_{FLPF} = \frac{I_{out3}(s)}{I_{in}(s)}\bigg|_{FLPF} = \frac{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}{D(s)} \tag{4.56}$$

$$T(s)\big|_{FBPF} = \frac{I_{out2}(s)}{I_{in}(s)}\bigg|_{FBPF} = \frac{g_{mF}/C_1^{\alpha}\,s^{\alpha}}{D(s)} \tag{4.57}$$

$$T(s)\big|_{FHPF} = \frac{I_{out1}(s)}{I_{in}(s)}\bigg|_{FHPF} = \frac{s^{2\alpha}}{D(s)} \tag{4.58}$$

where, $D(s) = s^{2\alpha} + g_{mF}/C_1^{\alpha}\,s^{\alpha} + g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}$

represents the characteristic equation of the filter and α is the fractional order of the capacitor.

The mathematical relations for critical frequencies for the responses namely, FLPF, FBPF and FHPF are presented in Table 4.5.

Table 4.5 Critical Frequencies for Various FOF-III Responses.

FLPF	$\omega_{3dB(FLPF)}^{4\alpha}+2g_{mF}/C_1^{\alpha}\,\omega_{3dB(FLPF)}^{3\alpha}\cos\alpha\pi/2+\omega_{3dB(FLPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.$ $\left.+g_{mF}^2/C_1^{2\alpha}\right)+2g_{mF}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3dB(FLPF)}^{\alpha}\cos\alpha\pi/2-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0$ $\omega_{p(FLPF)}^{3\alpha}+1.5g_{mF}/C_1^{\alpha}\cos\alpha\pi/2\,\omega_{p(FLPF)}^{2\alpha}+\omega_{p(FLPF)}^{\alpha}\left(g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.$ $\left.+0.5g_{mF}^2/C_1^{2\alpha}\right)+0.5g_{mF}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi/2=0$ $\omega_{rp(FLPF)}=\left(\dfrac{-1/2\,g_{mF}/C_1^{\alpha}\cos\alpha\pi/2+\sqrt{1/4\,g_{mF}^2/C_1^{2\alpha}\cos^2\alpha\pi/2-g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi}}{\cos\alpha\pi}\right)^{1/\alpha}$
FBPF	$\omega_{3dB(FBPF)}^{4\alpha}+2g_{mF}/C_1^{\alpha}\,\omega_{3dB(FBPF)}^{3\alpha}\cos\alpha\pi/2+\omega_{3dB(FBPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.$ $\left.-g_{mF}^2/C_1^{2\alpha}-8g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos^2\alpha\pi/2-g_{mF}/C_1^{\alpha}\sqrt{g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}}\cos\alpha\pi/2\right)$ $+2g_{mF}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3dB(FLPF)}^{\alpha}\cos\alpha\pi/2+g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0$ $\omega_{p(FBPF)}^{4\alpha}+g_{mF}/C_1^{\alpha}\cos\alpha\pi/2\,\omega_{p(FBPF)}^{3\alpha}-g_{mF}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\omega_{p(FBPF)}^{\alpha}\cos\alpha\pi/2$ $-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0$ $\omega_{rp(FBPF)}=\left(\dfrac{-1/2\,g_{mF}/C_1^{\alpha}+\sqrt{1/4\,g_{mF}^2/C_1^{2\alpha}-g_{mF}g_{mS}/C_1C_2\cos^2\alpha\pi/2}}{\cos\alpha\pi/2}\right)^{1/\alpha}$
FHPF	$\omega_{3dB(FHPF)}^{4\alpha}-2g_{mF}/C_1^{\alpha}\,\omega_{3dB(FHPF)}^{3\alpha}\cos\alpha\pi/2-\omega_{3dB(FHPF)}^{2\alpha}\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi\right.$ $\left.+g_{mF}^2/C_1^{2\alpha}\right)-2g_{mF}/C_1^{\alpha}\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{3dB(FHPF)}^{\alpha}\cos\alpha\pi/2-g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}=0$ $g_{mF}/C_1^{\alpha}\cos\alpha\pi/2\,\omega_{p(FHPF)}^{4\alpha}+\left(2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi+g_{mF}^2/C_1^{2\alpha}\right)\omega_{p(FHPF)}^{3\alpha}$ $+3g_{mF}/C_1^{\alpha}\,2\,g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\,\omega_{p(FHPF)}^{2\alpha}+2\,g_{mF}^2g_{mS}^2/C_1^{2\alpha}C_2^{2\alpha}\,\omega_{p(FHPF)}^{\alpha}=0$ $\omega_{rp(FHPF)}=\left(\dfrac{-1/2\,g_{mF}/C_1^{\alpha}\cos\alpha\pi/2+\sqrt{1/4\,g_{mF}^2/C_1^{2\alpha}\cos^2\alpha\pi/2-g_{mF}g_{mS}/C_1^{\alpha}C_2^{\alpha}\cos\alpha\pi}}{2}\right)^{1/\alpha}$

4.6 Conclusion

A Single-VDTA based MIMO Filter is presented in this paper which provides various responses in all four modes of operation with appropriate input choices. The transfer functions for all four modes of operations are derived and are tabulated. Filter parameters' sensitivities too are computed and found to be well within unity. To prove the workability of the proposition, the biquad is simulated using Cadence Virtuoso and 180 nm gpdk process parameters are used. Electronic tunability of parameters is also established by varying bias current. The theoretical and simulated values obtained are found to be in accordance with each other.

Further, a VDTA based FO-MISO universal filter is presented in this work which is designed using a single VDTAs and two FCs. Detailed mathematical formulations for FLPF response are presented. An FC of order 0.5 and value 1 $\mu\mho/s^{\alpha}$ is used for illustrating the proposal. The FC is emulated for three different instances obtained after first, second and third iterations based on Carlson method. Physical realization of FC is done using RC ladder network. Simulations have been carried out using Cadence Virtuoso. Theoretical and simulated results are found to be in close agreement. The proposed designs offer precise control of various filter parameters due to additional degree of freedom hence may be used for biomedical applications.

Moreover, a VDTA based voltage mode fractional order SISO filter; providing FHPF response, is presented. Workability of the proposed filter is verified through industry-standard tool Virtuoso from Cadence tool suite using gpdk180 foundry; for fractional-orders (α = 0.5-0.9). Performance of the proposed circuit is analysed by virtue of sensitivity and stability analysis. The simulated results are at par with theoretical ones, thereby validating the functionality of the proposed FOF-II.

CHAPTER – 5
SINUSOIDAL OSCILLATORS

The content and results of the following publication(s) are included in this chapter:

6. Parveen Rani and Rajeshwari Pandey, "Electronically Tunable Third Order Sinusoidal Oscillator based on VDTA", *Springer 8th International Conference on Nanoelectronics, Computational Intelligence & Communication Systems (NCCS-2022)*, 2022. (Paper ID: NCCS22015)

5.1 Introduction

Sinusoidal oscillators (SOs) are linear electric/electronic circuits and are widely used in various applications pertaining to telecommunications, control systems, signal processing and measurement systems. Sinusoidal oscillators may be broadly classified as second- and third- order sinusoidal oscillators (TOSO) [44-53]. It is pertinent to mention that for such applications, the third order sinusoidal oscillators are a apposite choice over second order oscillators, as they provide better frequency response. Further, sinusoidal oscillators are sub-categorized as single phase (SPs), quadrature oscillators (QOs) and multiple/multi-phase sinusoidal oscillators (MSOs). Comparative study for various voltage differencing transconductance amplifier based oscillators has been recorded in Table 1.3 for ready reference.

Comprehensive literature survey suggests that there is lean presence of third order sinusoidal oscillators. Further, explored TOSOs are designed around two active blocks; either combination of blocks [44] or both VDTAs [47,48]. In this Chapter, voltage differencing transconductance amplifier based two voltage mode third order sinusoidal oscillators based on single VDTA are presented.

5.2 TOSO-I

The first proposed structure to realize third order sinusoidal oscillator is shown in Fig. 5.1 and is designed around a single VDTA.

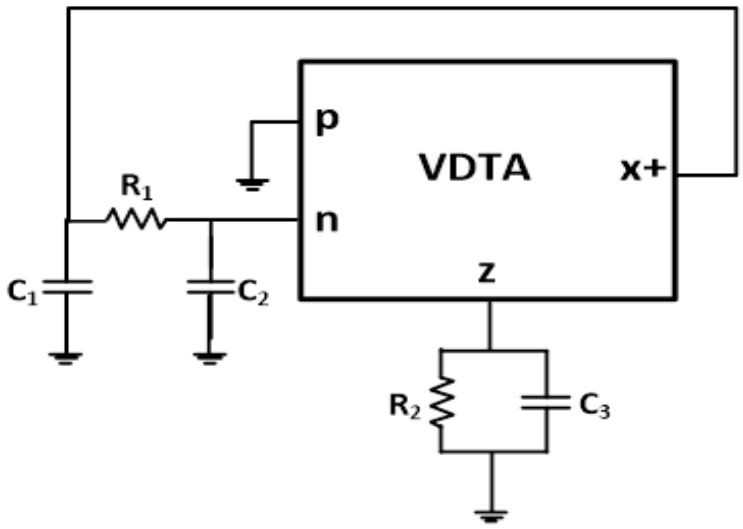


Fig. 5.1 Proposed Circuit (TOSO-I).

Using routine circuit analysis and considering current flowing into the ‘n’ terminal of the ideal VDTA as null the nodal equation at node ‘n’ can be expressed as

$$\left(1+sC_2R_1\right)V_n\left(s\right)=V_0\left(s\right) \tag{5.1}$$

The nodal equation at ‘z’ terminal can be written as

$$-g_{mF}R_2V_n\left(s\right)=\left(1+sC_3R_2\right)V_z\left(s\right) \tag{5.2}$$

The nodal equation at ‘x+’ terminal can be written as

$$\left(1/R_1+sC_1\right)V_0\left(s\right)-V_n\left(s\right)/R_1=g_{mS}V_z\left(s\right) \tag{5.3}$$

Thus, the generalized characteristic equation of the proposed third order sinusoidal oscillator is derived as

$$C_1C_2C_3R_1R_2s^3+\left(C_1C_2R_1+C_2C_3R_2+C_3C_1R_2\right)s^2+\left(C_1+C_2\right)s+g_{mF}g_{mS}R_2=0 \quad (5.4)$$

The corresponding frequency of oscillation (FO) and condition of oscillation (CO) are obtained as

$$f_o=\frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{C_1C_2C_3R_1R_2}} \quad (5.5)$$

$$\text{and } \left(C_1+C_2\right)\left(C_1C_2R_1+C_2C_3R_2+C_3C_1R_2\right)=g_{mF}g_{mS}R_1R_2^2C_1C_2C_3 \quad (5.6)$$

Assuming $C_1 = C_2 = C$, $C_3 = C'$, $R_1 = R_2 = R$, the characteristic equation simplifies to

$$C^2C'R^2s^3+\left(C^2R+2CC'R\right)s^2+2Cs+g_m^2R=0 \quad (5.7)$$

The simplified corresponding FO and CO are

$$f_o=\frac{1}{2\pi R\sqrt{CC'}} \quad (5.8)$$

$$\text{and } g_m^2R^2C'=2\left(C+2C'\right) \quad (5.9)$$

From Eqn. (5.8) and Eqn. (5.9), it is clear that CO can be tuned using g_m without affecting FO. Transconductances (g_{mF} and g_{mS}) may be varied by changing the bias currents (I_{BF} and I_{BS}) of the VDTA. Thus, the proposed third order sinusoidal oscillator is electronically tunable.

5.2.1 Non-Ideal Analysis

The analytical expressions presented in the preceding subsection have been obtained considering the VDTA to be ideal and therefore all the input and output terminals of the VDTA have been considered to be having infinite impedances. This section presents the mathematical analysis of the proposed circuit taking into account the parasitic at the input and output terminals of the VDTA. The non-ideal behavioural model of the proposed TOSO-I is depicted in Fig. 5.2 wherein each terminal is represented with a finite impedance Z_i (i = p, n, z, x) consisting of a capacitor C_i in parallel with a resistance R_i.

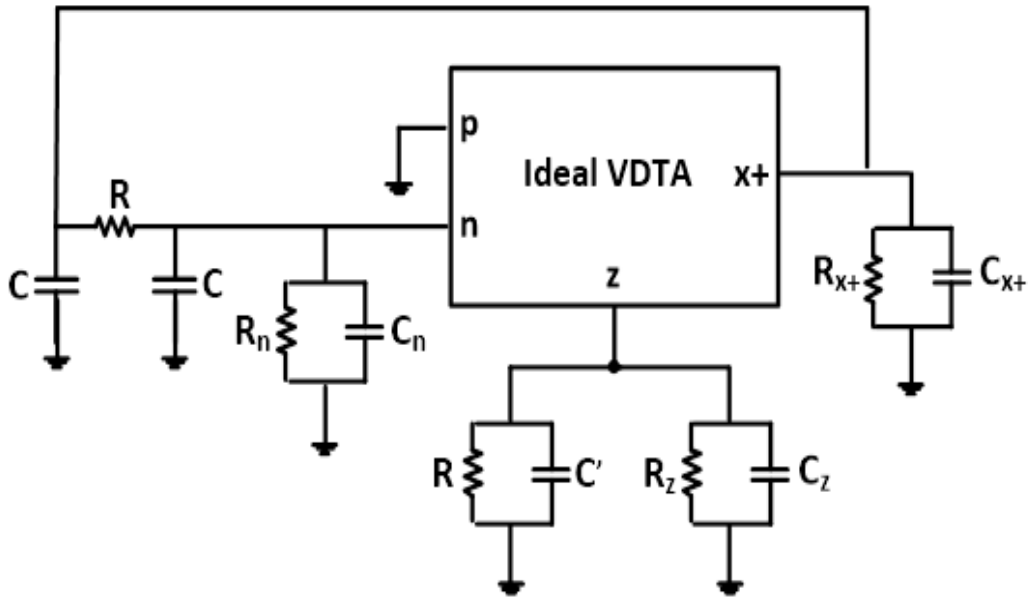


Fig. 5.2 Non Ideal Behavioural Model of the TOSO-I.

Considering current flowing into the ‘n’ terminal of the ideal VDTA as null the nodal equation at node ‘n’ can be expressed as

$$(1/R+sC)V_n(s)+(1/R_n+sC_n)V_n(s)=V_0(s) \tag{5.10}$$

The nodal equation at 'z' terminal can be written as

$$-g_{mF}V_n(s)=(1/R_z+sC_z)V_z(s)+(1/R+sC')V_z(s) \tag{5.11}$$

The nodal equation at 'x+' terminal can be written as

$$(1/R+sC)V_0(s)+(1/R_{x+}+sC_{x+})V_0(s)-V_n(s)/R=g_{mS}V_z(s) \tag{5.12}$$

Thus, the characteristic equation under non ideal conditions can be expressed as

$$\begin{aligned}
&C^2C'R^2s^3+\left[CC'R+CC'R^2(1/R_n+sC_n)+CR^2\left\{\left(C+C'/R\right)+C'(1/R_{x+}+sC_{x+})+C(1/R_z+sC_z)\right\}\right]s^2\\
&+\left[R\left\{\left(C+C'/R\right)+C'(1/R_{x+}+sC_{x+})+C(1/R_z+sC_z)\right\}\right.\\
&+R^2(1/R_n+sC_n)\left\{\left(C+C'/R\right)+C'(1/R_{x+}+sC_{x+})+C(1/R_z+sC_z)\right\}\\
&+CR^2\left\{1/R^2+1/R\left\{(1/R_{x+}+sC_{x+})+(1/R_z+sC_z)\right\}+(1/R_{x+}+sC_{x+})(1/R_z+sC_z)\right\}\Big]s\\
&+R\left[1/R^2+1/R\left\{(1/R_{x+}+sC_{x+})+(1/R_z+sC_z)\right\}+(1/R_{x+}+sC_{x+})(1/R_z+sC_z)\right]\\
&+R^2(1/R_n+sC_n)\left[1/R^2+1/R\left\{(1/R_{x+}+sC_{x+})+(1/R_z+sC_z)+(1/R_{x+}+sC_{x+})(1/R_z+sC_z)\right\}\right]=0
\end{aligned} \tag{5.13}$$

It is pertinent to mention here that the proposed oscillator circuit (TOSO-I) depicted in Fig. 5.1 comprises of grounded passive components only thereby making it capable of mitigating the effects of the parasitic impedance; which is fairly an advantage.

5.2.2 Sensitivity Analysis

The sensitivity is a significant performance criterion of any circuit. The sensitivity of frequency of oscillation 'f_0' for the circuit shown in Fig. 5.1 with respect to passive components; that is, R and C are given as

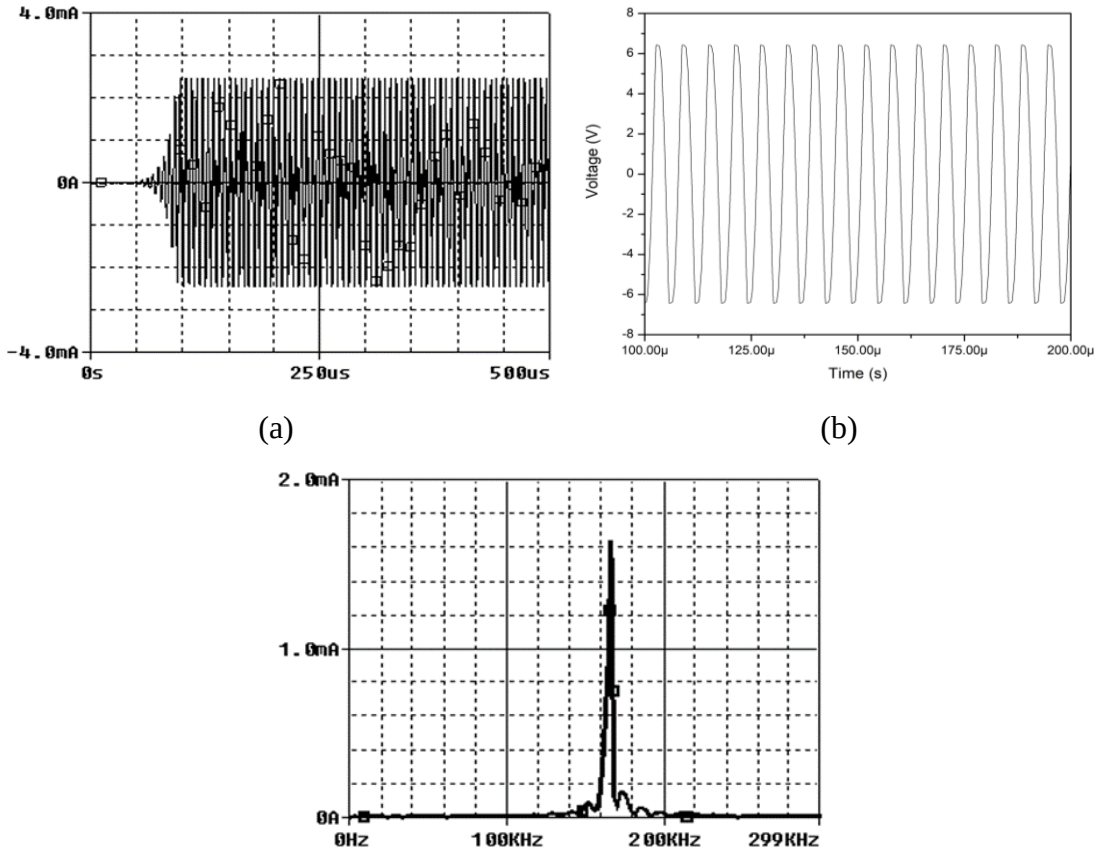
$$S_C^{f_0}=1/2 \qquad S_{C'}^{f_0}=1/2 \tag{5.14}$$

$$S_R^{f_0}=1 \tag{5.15}$$

From Eqn. (5.14) and Eqn. (5.15), it may be observed that all passive sensitivities are below or equal to unity in magnitude.

5.2.3 Simulation Results

The performance of the proposed third order sinusoidal oscillator is verified through Pspice simulations using AD844 IC model. The supply voltages are taken as ±10 V. The values of the resistors are taken as 10 kΩ. whereas the capacitors (C and C') are taken as 250 pF and 100 pF respectively. The simulated transient response, sustained oscillations and the corresponding FFT are shown in Fig. 5.3 (a), (b) and (c) respectively. The simulated value of f_0 is observed to be 169 kHz. The theoretical and simulated results are in mutual agreement with each other.



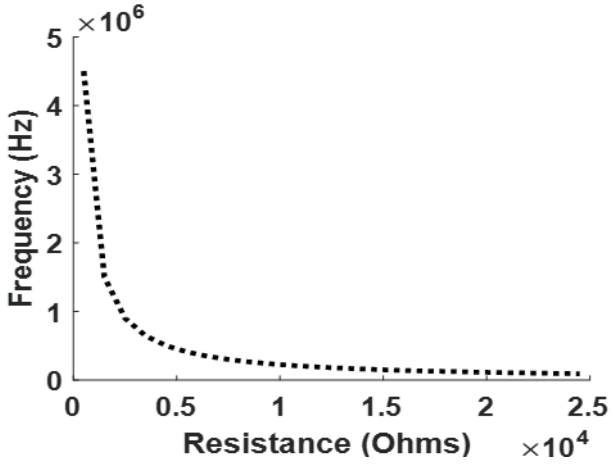
(a) (b)

(c)

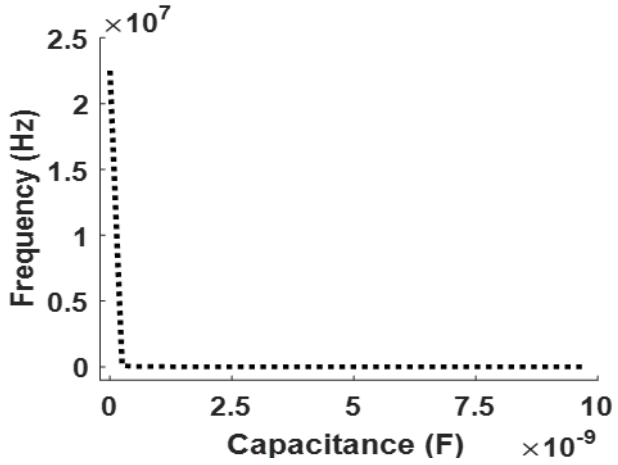
Fig. 5.3 TOSO-I (a) Transient Output (b) Sustained Oscillations (c) Frequency Spectrum.

The FO variation with respect to R and C are shown in Fig. 5.4(a) and (b) respectively. In Fig. 5.4(a) capacitor value is set at 100 pF and R is varied from 0.5

kΩ to 25 kΩ. For 5.4(b) resistor value is fixed at 10 kΩ and capacitor is varied from 1 pF to 10 nF.



(a)



(b)

Fig. 5.4 Frequency Tuning with (a) Resistance (b) Capacitance.

Thus, it is evident that the proposed third order sinusoidal oscillator relishes the benefits of frequency tuning.

5.3 TOSO-II

By connecting a resistance in shunt with the input capacitor, one more TOSO configuration is obtained and is shown in Fig. 5.5.

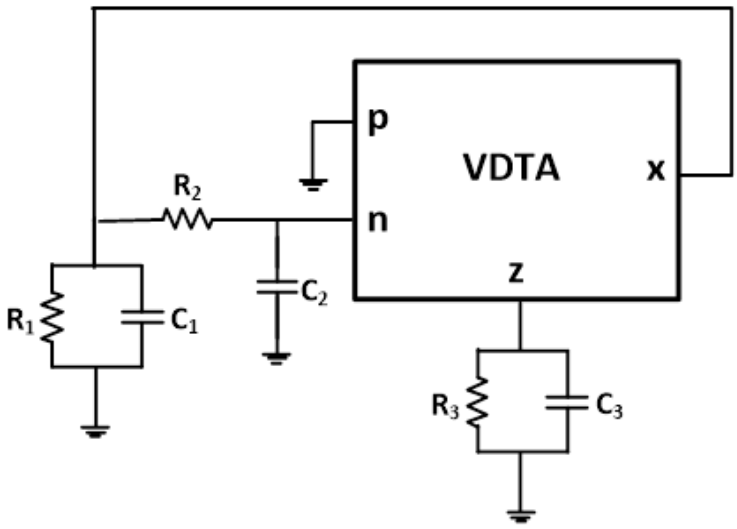


Fig. 5.5 Proposed Circuit (TOSO-II).

Using routine circuit analysis and considering current flowing into the ‘n’ terminal of the ideal VDTA as null the nodal equation at node ‘n’ can be expressed as

$$\left(1+sC_2R_2\right)V_n\left(s\right)=V_0\left(s\right) \tag{5.16}$$

The nodal equation at ‘z’ terminal can be written as

$$-g_{mF}R_3V_n\left(s\right)=\left(1+sC_3R_3\right)V_z\left(s\right) \tag{5.17}$$

The nodal equation at ‘x+’ terminal can be written as

$$\left[\left(1/R_1+sC_1\right)+1/R_2\right]V_0\left(s\right)-V_n\left(s\right)/R_2=g_{mS}V_z\left(s\right) \tag{5.18}$$

Thus, routine analysis of the second TOSO configuration, yields the following generalized characteristic equation

$$\begin{aligned} &C_1C_2C_3R_1R_2R_3s^3+\left[C_1C_2R_1R_2+C_3R_3\left(C_2R_1+C_2R_2+C_1R_1\right)\right]s^2 \\ &+\left[\left(C_2R_1+C_2R_2+C_1R_1\right)+C_3R_3\right]s+\left(1+g_{mF}g_{mS}R_1R_3\right)=0 \end{aligned} \tag{5.19}$$

The corresponding frequency of oscillation (FO) and condition of oscillation (CO) are obtained as

$$f_o=\frac{1}{2\pi}\sqrt{\frac{\left[\left(C_2R_1+C_2R_2+C_1R_1\right)+C_3R_3\right]}{C_1C_2C_3R_1R_2R_3}} \tag{5.20}$$

and $$\begin{aligned} &\left[\left(C_2R_1+C_2R_2+C_1R_1\right)+C_3R_3\right]\left[C_1C_2R_1R_2+C_3R_3\left(C_2R_1+C_2R_2+C_1R_1\right)\right] \\ &=C_1C_2C_3R_1R_2R_3\left(1+g_{mF}g_{mS}R_1R_3\right) \end{aligned} \tag{5.21}$$

Assuming $C_1 = C_2 = C$, $C_3 = C'$, $R_1 = R_2 = R_3 = R$, the characteristic equation becomes

$$C^2C'R^3s^3+\left(C^2R^2+3CC'R^2\right)s^2+\left(3CR+C'R\right)s+\left(1+g_m^2R^2\right)=0 \tag{5.22}$$

Further simplification (Considering $C_1 = C_2 = C_3 = C$, $R_1 = R_2 = R_3 = R$) leads to the following characteristic equation

$$R^3C^3s^3+3R^2C^2s^2+3RCs+\left(1+g_m^2R^2\right)=0 \tag{5.23}$$

The simplified corresponding FO and CO are

$$f_o=\frac{\sqrt{3}}{2\pi RC} \tag{5.24}$$

$$\text{and } g_mR=2\sqrt{2} \tag{5.25}$$

From Eqn. (5.24) and Eqn. (5.25), it is clear that CO can be tuned using g_m without affecting FO. Transconductances (g_{mF} and g_{mS}) may be varied by changing the bias currents (I_{B1} and I_{B2}) of the VDTA. Thus, the proposed third order sinusoidal oscillator is electronically tunable.

5.3.1 Sensitivity Analysis

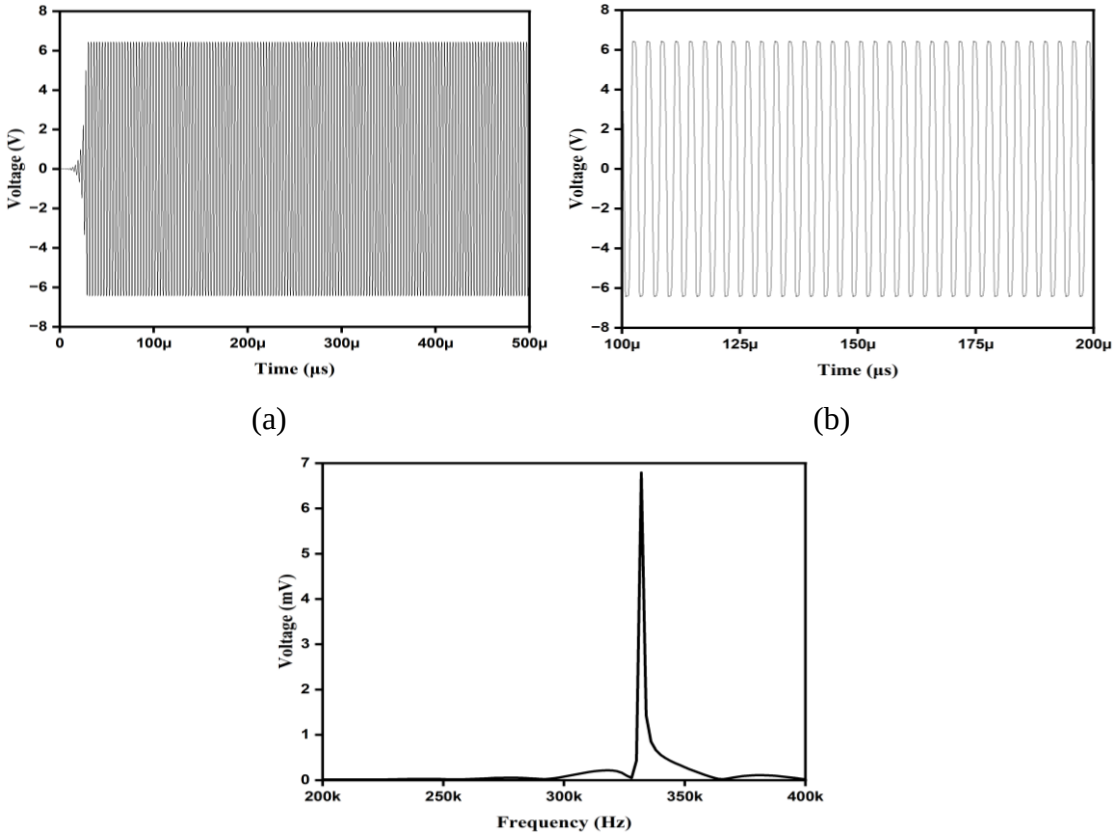
The passive component sensitivities of frequency of oscillation 'f_0' for the circuit shown in Fig. 5.5 are

$$S_R^{f_0} = S_C^{f_0} = 1 \tag{5.26}$$

Thus, from Eqn. (5.26), it may be observed that all passive sensitivities are equal to unity in magnitude.

5.3.2 Simulation Results

The performance of the second proposed third order sinusoidal oscillator is verified through Cadence simulations. The values of the resistors are taken as 15 kΩ. whereas the capacitors are taken as 75 pF respectively. The simulated transient response, sustained oscillations and the corresponding FFT are shown in Fig. 5.6 (a), (b) and (c) respectively. The simulated value of f_0 is observed to be 332 kHz. The theoretical and simulated results are in mutual agreement with each other.



(a) (b)

(c)

Fig. 5.6 TOSO-II (a) Transient Output (b) Sustained Oscillations
(c) Frequency Spectrum.

5.4 Conclusion

This chapter presented two new voltage differencing transconductance amplifier based third order sinusoidal oscillators. The characteristic equation and hence corresponding frequency and condition of oscillation are derived for both the configurations. To prove the workability, the oscillator is simulated on Pspice. Electronic tunability of parameters is also established by varying g_m. The theoretical and simulated values obtained are found to be in accordance with each other.

CHAPTER – 6
VDTA STRUCTURES

The content and results of the following publication are included in this chapter:

7. Parveen Rani, Priyanka Gupta, Gurumurthy Komanapalli and Rajeshwari Pandey, "New Approaches for Realizing Transconductance-Boosted VDTA Structures", *Journal of Circuits, Systems and Computers*, vol. 33, no. 12, 2450209 (2024).

   DOI: https://doi.org/10.1142/S0218126624502098

   [SCIE, Impact Factor (1.5)]

6.1 Introduction

Commercial portable devices having variety of features with extended battery life have become essential part of life. Owing to an upsurge in this demand the research focus of circuit designers has been directed towards low voltage, low power and high speed circuits, in past few decades. This has led to the proposition of several low voltage device techniques such as floating gate, bulk driven and sub threshold operations etc. and circuit techniques such class AB operation, self-cascode, adaptive biasing and current mode (CM) operations. Further, circuits designed using CM techniques offer numerous merits over voltage mode (VM) counterparts; such as larger dynamic range, reduced power consumption and wider bandwidth. As a result, various CM analog building blocks are reported over the past three decades which are summarized in [3]. The voltage differencing transconductance amplifier (VDTA) [11] is one such versatile block which is an appropriate choice for designing integrated analog applications [11-53] with electronic tunability of circuit parameters. The suitability of VDTA for integrated circuit applications has resulted in numerous VDTA implementation as is evident from the available literature [11,15,18,27,110-112].

It is well known that, transconductance amplifier (TA) with high transconductance gain 'g_m' are essential for designing high performance analog circuits. Most traditionally the g_m can be enhanced by increasing the bias current of the TA stage. However, increased bias current essentially leads to large power dissipation leading to a trade-off between the transconductance gain and the power dissipation. Extensive review suggests that all available CMOS based VDTA implementations [11,15,18,27,110-112] increase the bias current for enhancing the g_m of the TA stages. Thus, it may be summarized that the available VDTA structures do not provide characteristics like low power and high transconductance gain simultaneously.

In this chapter two new VDTA structures with enhanced transconductance gain have been proposed which are presented in following section.

6.2 Proposed Circuits

This work contributes two new VDTA propositions which make use of additional circuitry for enhanced transconductance gain. The first proposed structure relies on the positive partial feedback technique which makes use of a cross coupled NMOS transistor pair. While to boost the transconductance gain, the second structure implements an inverting amplifier each between the gate and source terminals of the differential pair transistors in the TA stage.

The following subsection presents a brief on conventional VDTA which is further modified to develop two new VDTA propositions with increased transconductance gain.

6.2.1 Conventional VDTA

Conventionally, the VDTA is designed by cascading two transconductance amplifier (TA) stages. A typical CMOS implementation is depicted in Fig. 6.1 which will be referred to as conventional VDTA hereafter. It may be observed that the TA1 stage comprises of differential pair transistors M_1, M_2 and active load transistors M_3 and M_4. Similarly, stage TA2 consists of M_9, M_{10}, M_{11} and M_{12}. The transconductance gain of TA1 and TA2 can only be enhanced by increasing the bias current $I_{b1,2}$ which results in high power dissipation.

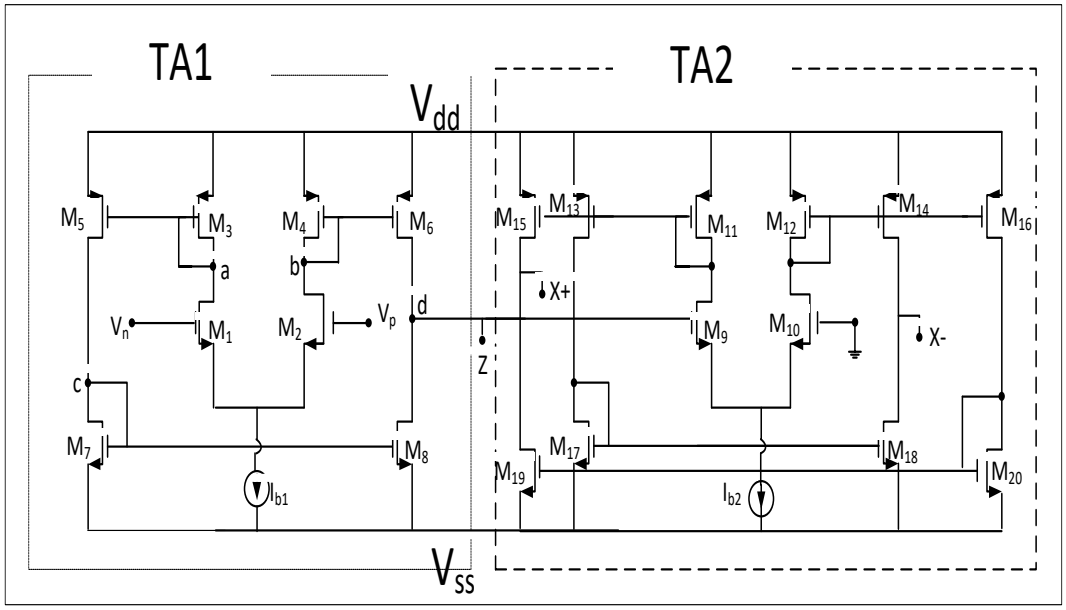


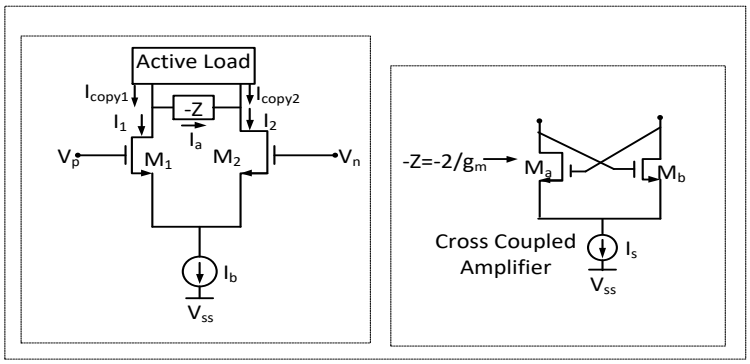
Fig. 6.1 Conventional scheme for designing VDTA.

6.2.2 Proposed VDTA-I

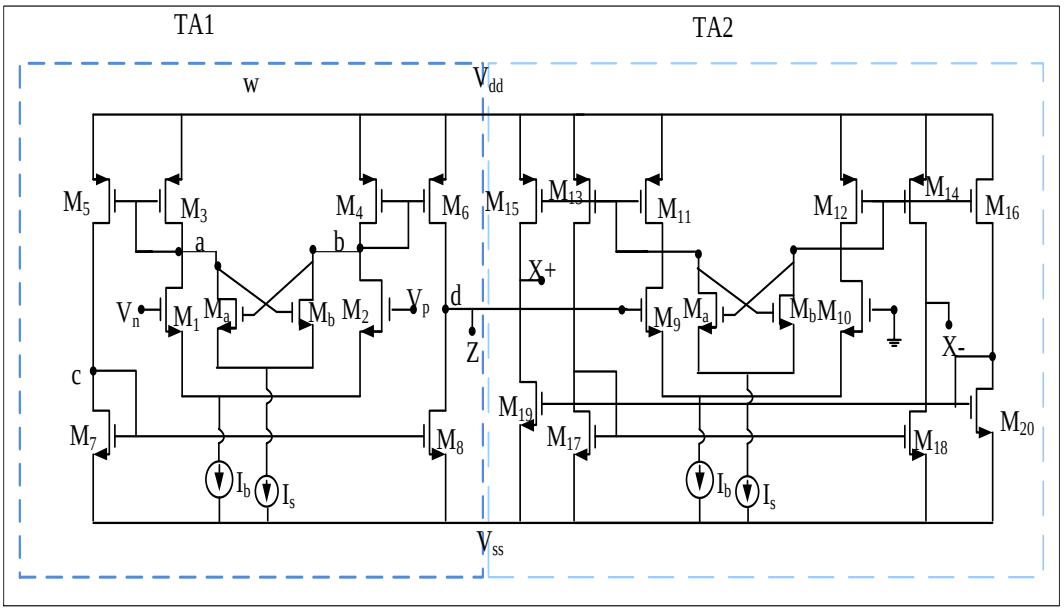
The proposed first structure VDTA-I, which is a modification over conventional VDTA, makes use of well-known partial positive feedback technique [113] for gain enhancement. The transconductance gain of the proposed VDTA-I, is enhanced by connecting positive feedback through active loads of both the TA stages.

The concept of partial positive feedback [113] is shown in Fig. 6.2(a) where a negative impedance Z is connected between the drain terminals of the differential pair (formed by M_1 and M_2). It is evident that the resulting currents I_{copy1}/I_{copy2} will be the summation/difference of I_1/I_2 and I_a respectively. Thus, the overall differential current (I_2 - I_1) will be raised by the factor $2*I_a$ resulting in increased transconductance gain computed as $(I_2 - I_1)/(V_p - V_n)$. The negative impedance Z may be realized using cross coupled NMOS transistors (M_a and M_b) which provide positive feedback. It is pertinent to mention that the impedance of this cross coupled pair can be controlled through the bias current of the cross coupled amplifier I_s.

The complete CMOS implementation of the proposed VDTA-I is depicted in Fig. 6.2(b) wherein, for stage TA1 transistors M_3, M_4 act as active load, M_{3-5}, M_{4-6} are the corresponding current mirrors along with M_{7-8}. The cross coupled M_a, M_b pair serves as negative impedance for positive feedback. The respective functions for stage TA2 are served by transistors M_{11} M_{12}, M_{11-13}, M_{12-14} along with M_{17-18}. The I_b represents the bias currents for the respective TA stages whereas the Is is the bias currents for the cross coupled amplifiers.



(a)



(b)

Fig. 6.2 Proposed VDTA-I (a) Scheme (b) CMOS Implementation.

The small signal high frequency model for TA1 is depicted in Fig. 6.3. For the sake of clarity of presentation $r_{oa}||r_{01}||r_{03}$, $C_{gs3}+C_{gs5}+C_{gsb}$, $r_{ob}||r_{02}||r_{04}$, $C_{gs4}+C_{gs6}+C_{gsa}$, $r_{o7}||r_{05}$ and $C_{gs7}+C_{gs8}$ are represented by R_A, C_A, R_B, C_B and R_C and C_C respectively.

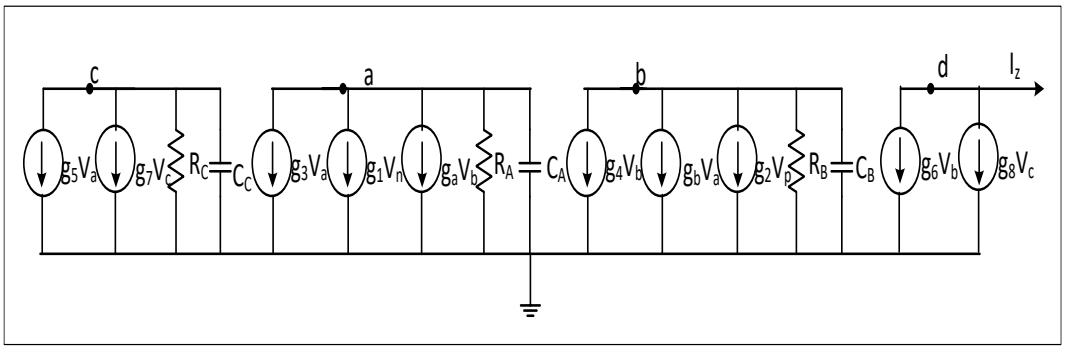


Fig. 6.3 Small-signal high-frequency model of TA1 stage of the proposed VDTA-I.

The nodal equations at nodes ‘a’, ‘b’ and ‘c’ can be represented by Eqn. (6.1), Eqn. (6.2) and Eqn. (6.3) respectively.

$$\left(g_3+\frac{1}{R_A}+sC_A\right)V_a+g_aV_b=-g_1V_n \tag{6.1}$$

$$g_bV_a+\left(g_4+\frac{1}{R_B}+sC_B\right)V_b=-g_2V_p \tag{6.2}$$

$$V_c=\frac{-g_5V_a}{\left(g_7+\frac{1}{R_C}+sC_C\right)} \tag{6.3}$$

Considering $g_7=g_5$ and keeping in view that ($g_7/Cc+1/R_CCc$) is not the dominant pole, Eqn. (6.3) results in

$$V_c=-V_a \tag{6.4}$$

Applying KCL at node ‘d’ gives

$$-g_6V_b-g_8V_c=I_Z \tag{6.5}$$

$$-g_6V_b+g_8V_a=I_Z \tag{6.6}$$

Assuming $g_a = g_b$, $g_1 = g_2$, $g_3 = g_4$, $g_6 = g_8$, $R_A = R_B$, $C_A = C_B$ and solving Eqn. (6.1), Eqn. (6.2) leads to

$$V_a - V_b = \frac{-g_1(V_p - V_n)}{\left(-g_a + g_3 + \frac{1}{R_A} + sC_A\right)} \tag{6.7}$$

Substituting Eqn. (6.7) in Eqn. (6.6) results in

$$I_z = \frac{g_1 g_6 (V_p - V_n)}{\left(-g_a + g_3 + \frac{1}{R_A} + sC_A\right)} \tag{6.8}$$

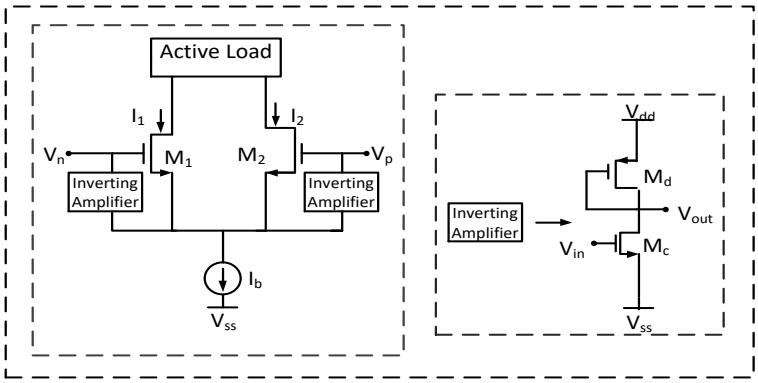
$$g_{m1} = \frac{I_z}{(V_p - V_n)} = \frac{g_1 g_6}{(-g_a + g_3)\left((1 + \frac{1}{(-g_a + g_3)R_A}) + \frac{sC_A}{(-g_a + g_3)}\right)} \tag{6.9}$$

It may be observed that the transconductance gain (g_{m1}) is modified by a factor *(1/(1- η))* where η represents the ratio g_a/g_3. If η is set as $0 < \eta < 1$, then the factor $1/(1 - \eta)$ will be greater than 1 and hence the transconductance gain will be enhanced. Further, the gain bandwidth product of the proposed structure increases though it leads to the reduction in the bandwidth of the proposed structure.

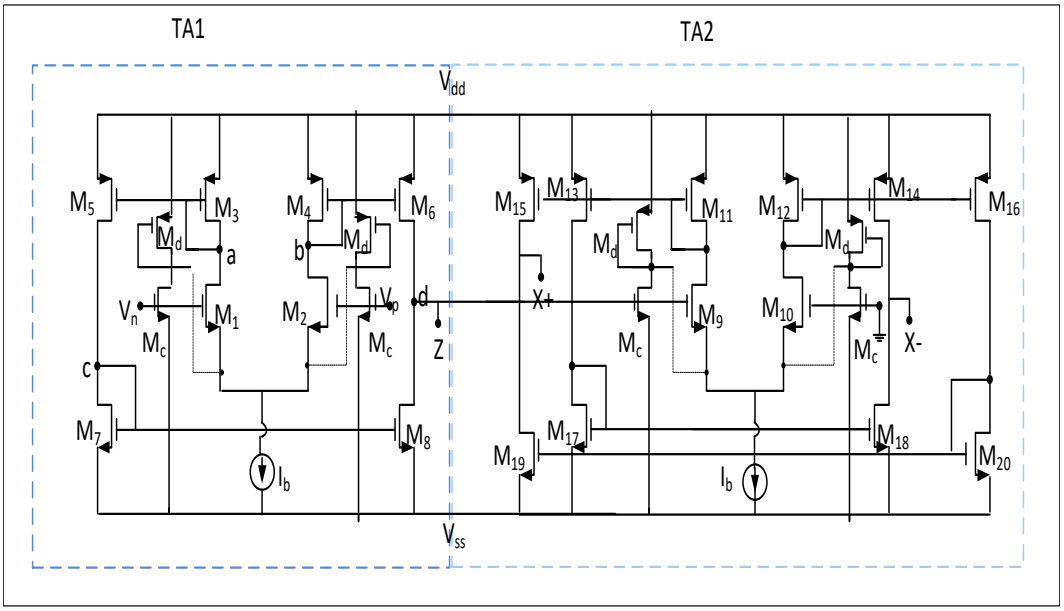
6.2.3 Proposed VDTA-II

It is well known that transconductance of a differential pair is proportional to $\sqrt{I_b}$ or V_{GS} where I_b represents the bias current and V_{GS} is gate to source voltage of the MOSFET. The open literature suggests that to enhance g_m bias current method is used most widely. However, it leads to limited transconductance variation and at a cost of large power dissipation [114]. In the proposed VDTA-II the V_{GS} variation method is used. The V_{GS} variation topology is shown in Fig. 6.4(a) wherein inverting amplifiers are used to enhance the V_{GS} of each transistor (M_1 and M_2) of the differential pair. The inverting amplifiers are placed between the gate and the source terminals of the differential pair (M_1 and M_2) and their output terminals are tied to the source terminals of differential pair transistors, while keeping the differential pair transistors and inverting amplifiers at the same input voltages, respectively. Phase

reversal between inputs and outputs produced by inverting amplifiers increases the potential differences between the gate and source terminals of differential pair transistors. This increase in V_{GS} is proportional to the gain of the inverting amplifier configuration which in turn increases the transconductance of the differential pair. The complete CMOS implementation of the proposed VDTA-II based on the outlined method is depicted in Fig. 6.4(b).



(a)



(b)

Fig. 6.4 Proposed VDTA-II (a) Scheme (b) CMOS Implementation.

The small signal high frequency model for TA1 of proposed VDTA-II is shown in Fig. 6.5. For the sake of clarity $r_{01}||r_{03}$, $r_{02}||r_{04}$ and $r_{o7}||r_{05}$ are represented as R_A, R_B and R_C respectively while $C_{gs3}+C_{gs5}$, $C_{gs4}+C_{gs6}$ and $C_{gs7}+C_{gs8}$ are termed as C_A, C_B and Cc respectively. The gain of the inverting amplifier given by g_c/g_d is represented by 'G'.

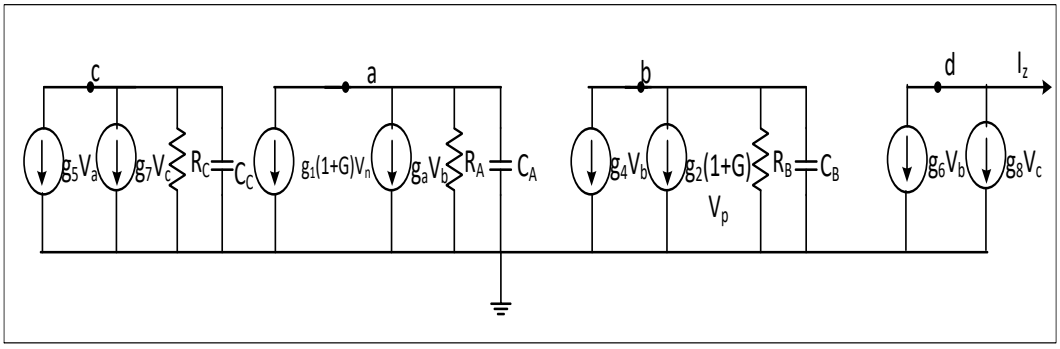


Fig. 6.5 Small-signal high-frequency model of proposed VDTA-II.

Applying KCL at nodes 'a', 'b' and 'c' result in Eqn. (6.10), Eqn. (6.11) and Eqn. (6.12) respectively.

$$V_a = \frac{-g_1(1+G)V_n}{\left(g_3 + \frac{1}{R_A} + sC_A\right)} \tag{6.10}$$

$$V_b = \frac{-g_2(1+G)V_p}{\left(g_4 + \frac{1}{R_B} + sC_B\right)} \tag{6.11}$$

$$V_c = \frac{-g_5V_a}{\left(g_7 + \frac{1}{R_C} + sC_C\right)} \tag{6.12}$$

Keeping in view that the pole ($g7/Cc+1/R_CCc$) cannot be dominant pole and considering $g_7=g_5$, results in Eqn. (6.13)

$$V_c = -V_a \tag{6.13}$$

Applying KCL at node ‘d’

$$-g_6V_b - g_8V_c = I_Z \tag{6.14}$$

$$-g_6V_b + g_8V_a = I_Z \tag{6.15}$$

Considering $g_3=g_4$, $R_A=R_B$ and $C_A=C_B$ and $g_a= g_b$, the (V_a-V_b) from Eqn. (6.10) and Eqn. (6.11) may be expressed as Eqn. (6.16)

$$V_a - V_b = \frac{-g_1(1+G)(V_p - V_n)}{\left(g_3 + \frac{1}{R_A} + sC_A\right)} \tag{6.16}$$

Using Eqn. (6.13), Eqn. (6.14) and Eqn. (6.15), I_z can be written as

$$I_z = \frac{g_1g_6(1+G)(V_p - V_n)}{\left(g_3 + \frac{1}{R_A} + sC_A\right)} \tag{6.17}$$

Thus the transconductance g_m can be expressed as

$$g_m = \frac{I_z}{(V_p - V_n)} = \frac{g_1g_6(1+G)}{g_3\left((1+ 1/g_3R_A) + sC_A\right)} \tag{6.18}$$

It may be observed from Eqn. (6.18) that the transconductance will be increased by a factor of $(1+G)$ without affecting the bandwidth.

6.3 Simulation Results

This Section presents the simulation results of the proposed structures (VDTA-I and VDTA-II). The SPICE simulations are performed using 0.18 µm technology parameters. The aspect ratios of the transistors are presented in Table 6.1. The power supply used is ±0.9 V and the bias currents are set to 50 µA. The simulations have been carried out with z node terminated by 1 kΩ.

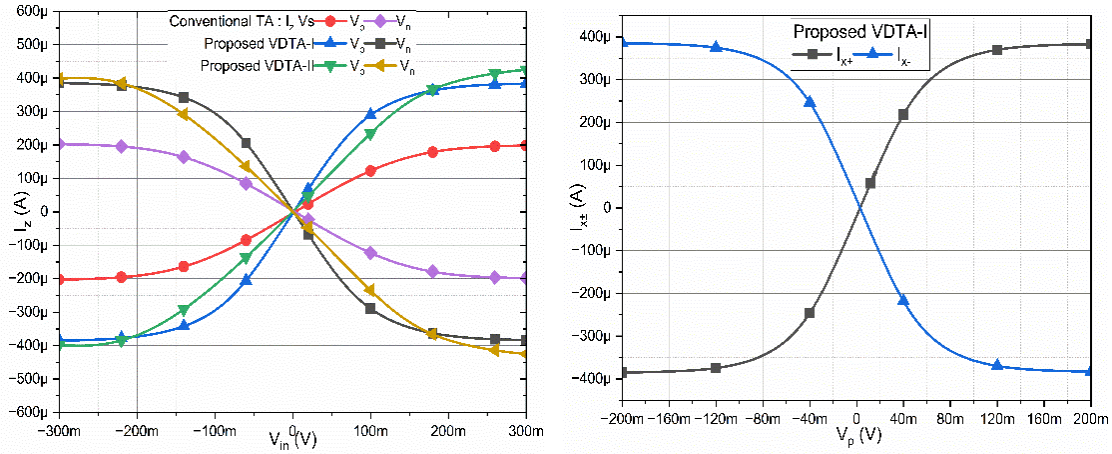
Table 6.1 Device Dimensions.

Transistor	Aspect Ratio
M_1-M_4, M_9-M_{12}	3.6 µm/0.36 µm
M_5-M_6, M_{13}-M_{16}	14.4 µm/0.36 µm
M_7-M_8, M_{17}-M_{20}	7.2 µm/0.36 µm
M_a - M_b	0.72 µm/0.36 µm
M_c	7.2 µm/0.9 µm
M_d	1.8 µm/1.8 µm

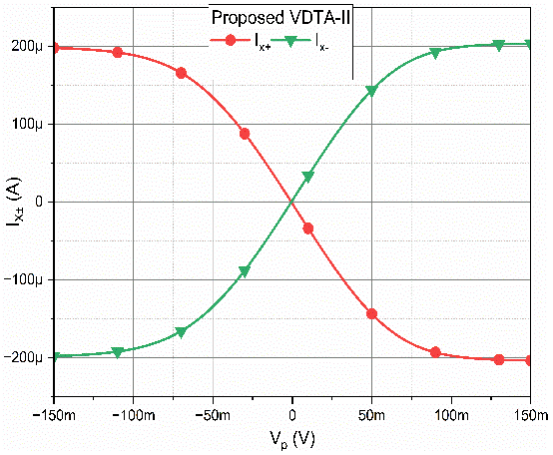
6.3.1 DC Characteristics

The DC transfer characteristics of the VDTA-I and VDTA-II are depicted in Fig. 6.6. The variations of I_z with respect to the input voltage V_{in} (applied across p and n terminals) for both the proposed structures are depicted in Fig. 6.6(a). The linear input voltage ranges are observed to be ±150 mV and ±200 mV for the proposed VDTA-I and the proposed VDTA-II respectively. The DC transfer characteristic of conventional VDTA is also depicted in Fig. 6.6(a) for the sake of comparison.

The Fig. 6.6(b) and Fig. 6.6(c) depict the variation of $I_{x\pm}$ with respect to change in V_p for VDTA-I and VDTA-II respectively. From Fig. 6.6(b) and Fig. 6.6(c), the overall linear ranges are observed as ±50 mV and ±80 mV for proposed VDTA-I and VDTA II respectively.



(a) (b)



(c)

Fig. 6.6 The DC Transfer Characteristics (a) I_z versus V_{in} (b) $I_{x\pm}$ versus V_p for VDTA-I (c) $I_{x\pm}$ versus V_p for VDTA-II.

6.3.2 AC Characteristics

The AC responses of the proposed VDTAs are depicted in Fig. 6.7. The AC responses for transconductance g_{m1} for the conventional VDTA and the proposed structures are shown in Fig. 6.7(a). The g_{m1} values are observed to be 1.4 mS, 3.6 mS and 2.3 mS respectively for the conventional, proposed VDTA-I and VDTA-II and corresponding 3dB frequencies are recorded to be 370 MHz, 160 MHz and 630 MHz. It is observed that in comparison to the conventional circuit, the g_m values for VDTA-I and VDTA-II are increased by 140% and 53% respectively. The current at x_+ terminal is observed to be 1.28 mA with a bandwidth of 80 MHz for the proposed

VDTA-I, and 0.318 mA with the bandwidth of 225 MHz for the proposed VDTA-II, as shown in Fig. 6.7(b) and Fig. 6.7(c) respectively, whereas for conventional VDTA, it is 0.194 mA with 54 MHz bandwidth.

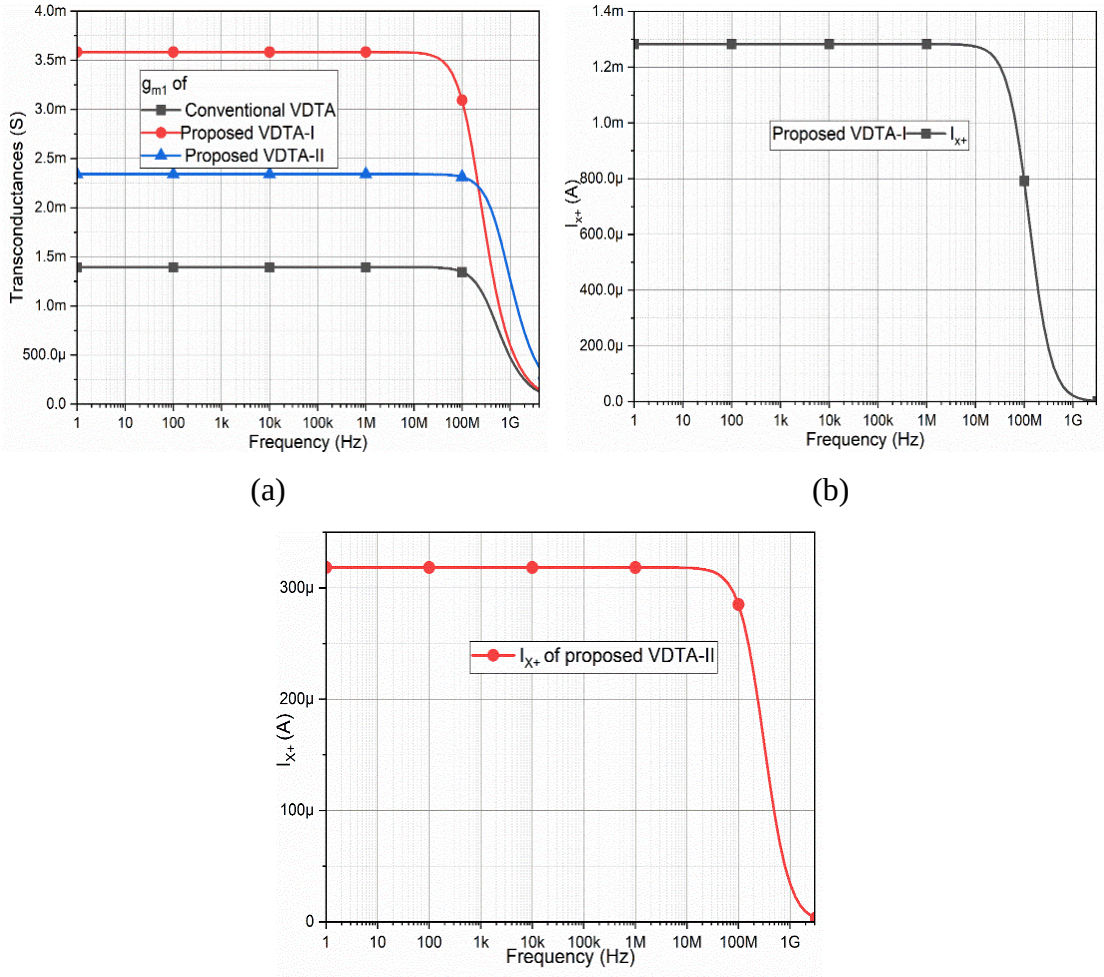


Fig. 6.7 Frequency Response (a) Transconductance Gain (g_{m1}) (b) I_{x+} of VDTA-I (c) I_{x+} of VDTA-II.

The transconductance (g_{m1}) of the proposed VDTA-I is also observed to be increasing with the increase in bias currents 'I_b' and 'I_s' and the same is depicted in Figs. 6.8 (a) and (b) respectively. Similarly, the variation of the transconductance (g_{m1}) of the proposed VDTA-II is plotted in Fig. 6.8(c) for 'I_b' variation. It may be

observed from Eqn. (6.18) that g_{m1} is a function of gain of inverter (G), therefore the variation of g_{m1} is observed with variation of W/L of M_c (G is proportional to g_c) and the same is shown in Fig. 6.8(d).

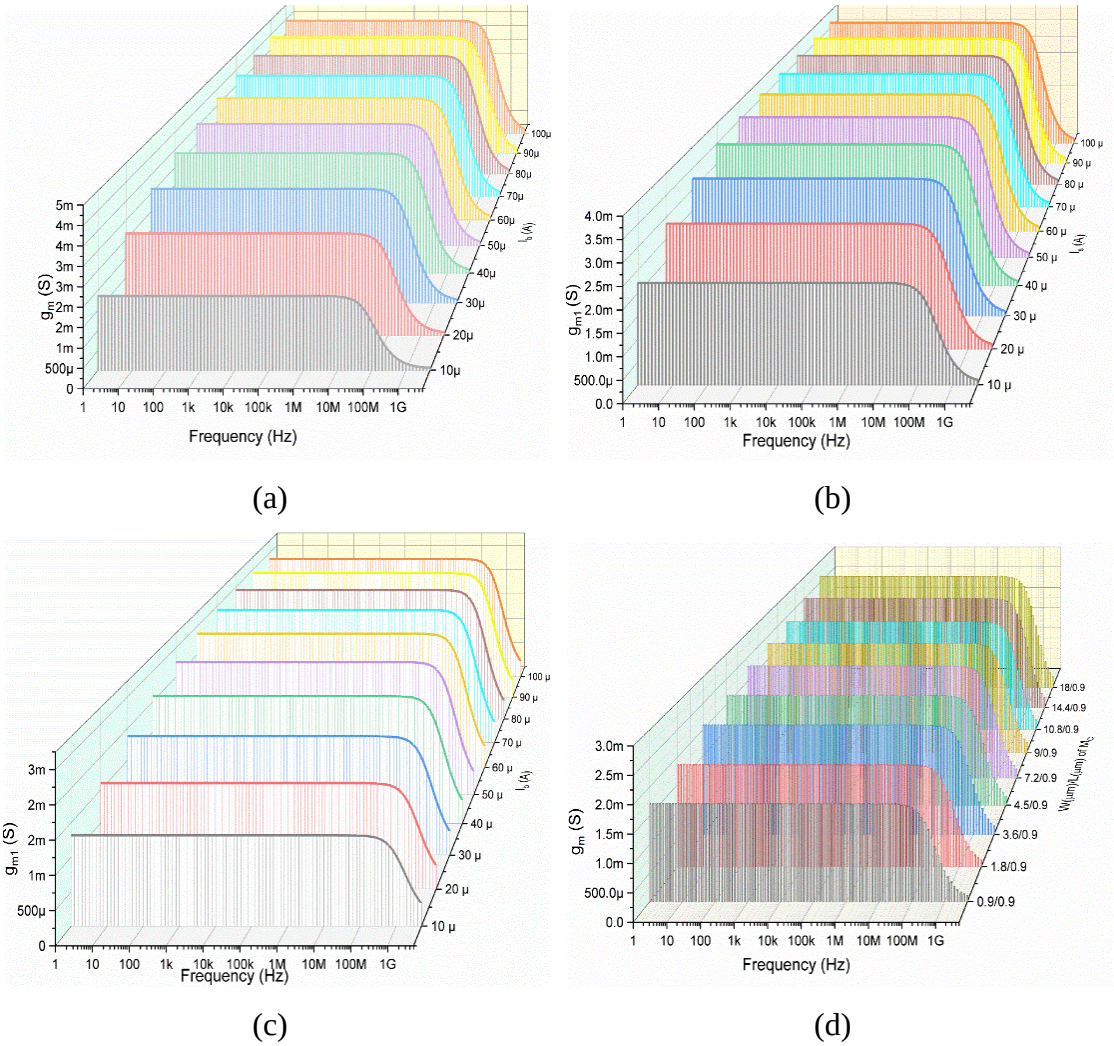
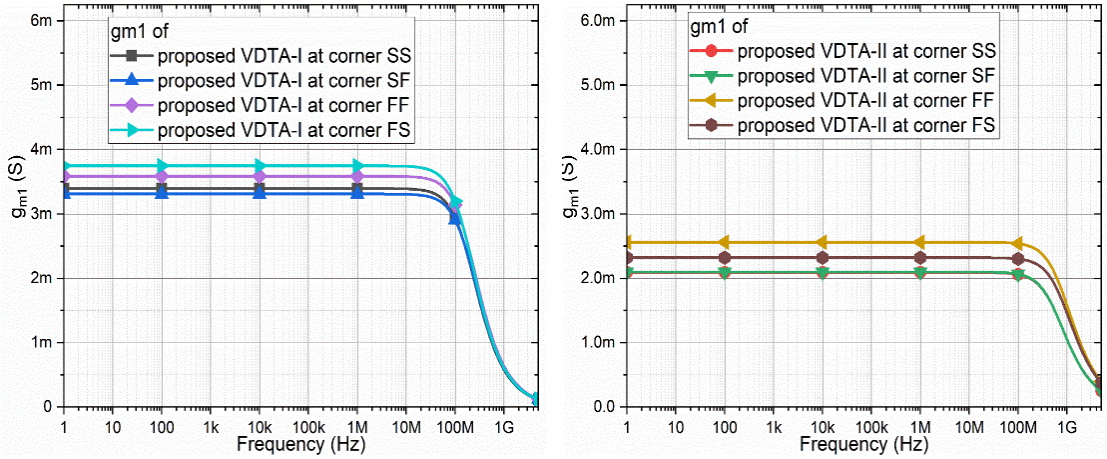


Fig. 6.8 AC Response of Transconductance (g_{m1}) with variation in (a) I_b for VDTA-I (b) I_s for VDTA-I (c) I_b for VDTA-II (d) Gain of Inverters for VDTA-II.

6.3.3 PVT Analysis

The behavior of both the proposed structures is also studied under Process, Voltage and Temperature (PVT) variation as depicted in Figs. 6.9, 6.10 and 6.11 respectively. The extreme process corners may vary from slow (S) to fast (F) and both NMOS and PMOS are being used in the proposed structure, therefore four possible corner

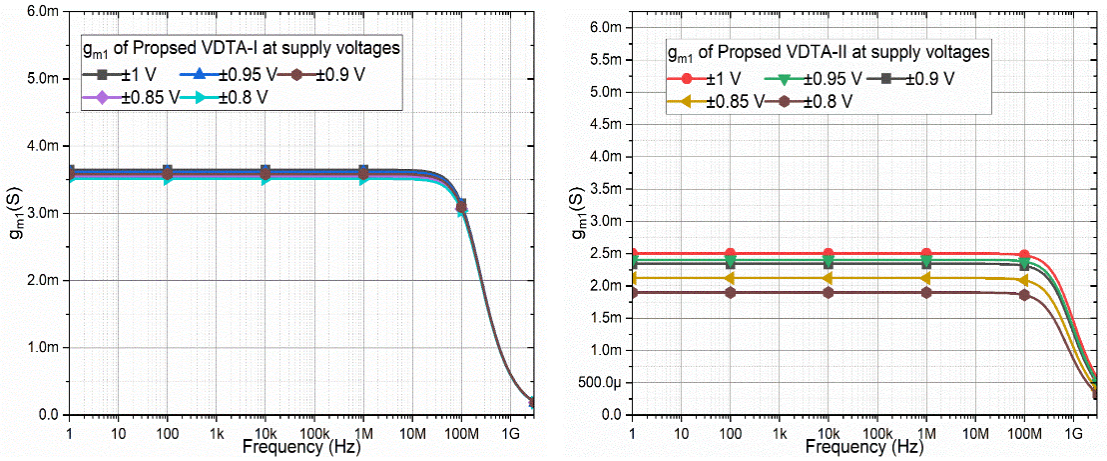
analyses are presented which are SS, SF, FS and FF. The variation of the transconductance (g_{m1}) for proposed VDTA-I and VDTA-II are depicted in Fig. 6.9 (a) and (b) respectively.



(a) (b)

Fig. 6.9 Transconductance for different Process Corners (SS, SF, FS and FF) (a) VDTA-I (b) VDTA-II.

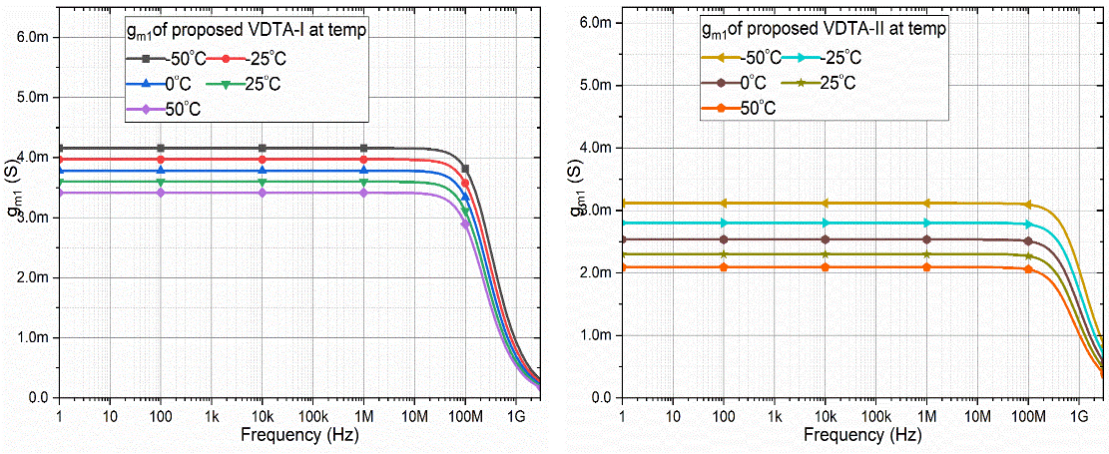
The proposed configurations are also tested for variation in supply voltages. The variation of the transconductance (g_{m1}) with change in supply voltages from ± 0.8 V to ± 1 V in steps of 0.05 V for VDTA-I and VDTA-II, are presented in Fig. 6.10 (a) and (b) respectively.



(a) (b)

Fig. 6.10 Transconductances for different Supply Voltages for proposed (a) VDTA-I (b) VDTA-II.

The effect of temperature variation in transconductance is also observed through simulations for both the proposed structures. The variations in g_{m1} for the change in temperature from -50 ˚C to 50 ˚C in the steps of 25 ˚C are depicted in Fig. 6.11 (a) and (b) for VDTA-I and VDTA-II respectively.

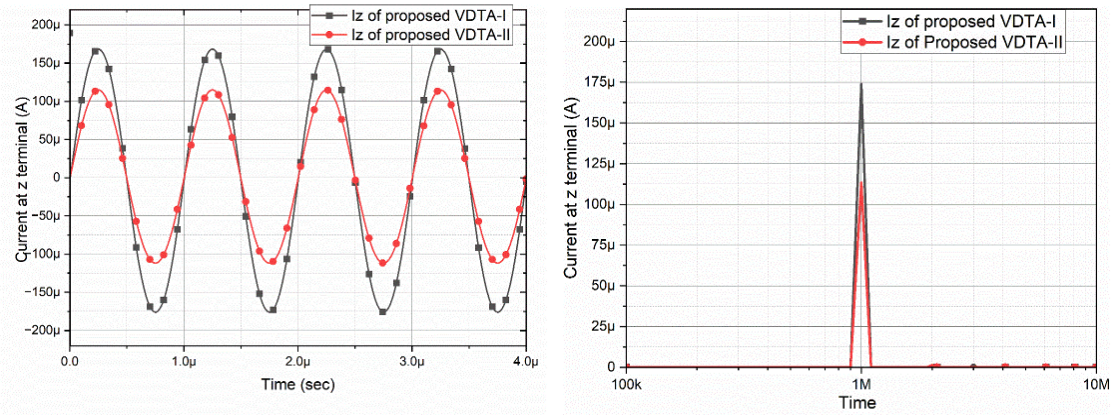


(a) (b)

Fig. 6.11 Variations in Transconductance with respect to Temperature for (a) VDTA-I and (b) VDTA-II.

6.3.4 Transient Response

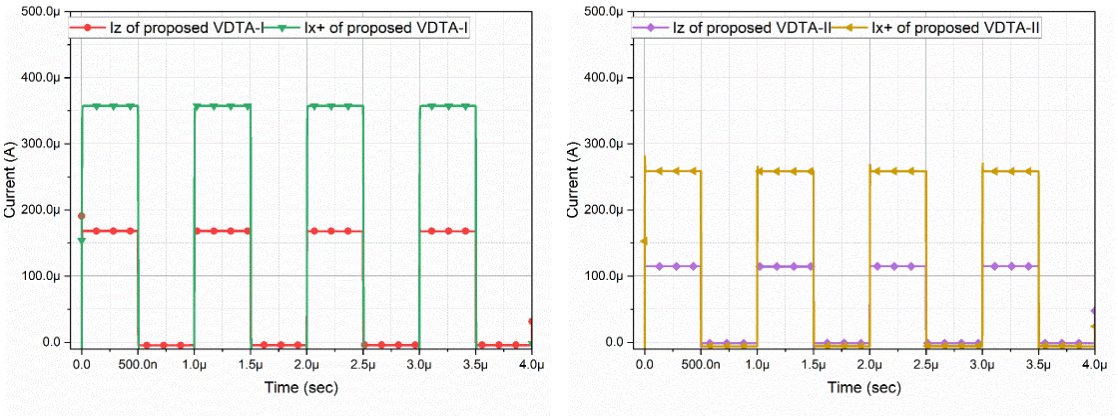
The time domain behavior of the proposed VDTAs is studied in this subsection. The circuits are excited with a 50 mV Vpp/1MHz input source, and the output currents at the z terminals are plotted. The transient responses for the proposed structures are shown in Fig. 6.12(a) and their respective spectrums are depicted in Fig. 6.12(b). Further, the total harmonic distortion (THD), which is the measure to estimate the degree to which a system is non-linear, is also observed for both circuits. The THDs for VDTA-I and VDTA–II are observed to be 0.9% and 1.3% respectively and are quite low.



(a) (b)

Fig. 6.12 Current I_{x+} for VDTA-I and VDTA-II (a) Time domain (b) FFT, for Sinusoidal inputs.

The pulse input responses of the proposed VDTAs are shown in Fig. 6.13. The input is excited with 50 mV /1MHz pulse signal. The currents at z and x+ terminals are shown in Fig. 6.13(a) and Fig 6.13(b) respectively. The slew rates are obtained as 0.08639825 A/µs and 0.123165 A/µs for proposed VDTA-I and VDTA-II respectively.



(a) (b)

Fig. 6.13 Current at Z and X+ Terminal for (a) Proposed VDTA-I (b) Proposed VDTA-II.

A comparative study of various performance parameters of all available CMOS based VDTA implementations [11,15,18,27,110-112], conventional VDTA, VDTA-I and VDTA-II is given in Table 6.2.

Table 6.2 Summary of Existing CMOS VDTA Implementations.

Ref.	Technology (μm)	Power Supply (V)	No. of Current Sources (Value)	Input Voltage Range (mV)	Transconductance (μS)	Bandwidth (MHz)	Power Consumption
[11]	0.18	± 0.9	4 (150 μA)	± 300	636	NA*	NA
[15]	0.18	± 2	2 (40 μA)	NA*	381	NA*	1 mW
[18]	0.18	± 1.5	4 (40 μA)	NA*	150	NA*	NA
[27]	0.18	± 0.7	2 (10 μA)	-80 to 80	415	225	145 μW & 102 μW
[110]	0.18	± 1	-	NA*	NA*	NA*	0.184 mW
[111]	0.18	± 1.8	8 Voltage sources for biasing (NA*)	NA*	NA*	NA	NA*
[112]	0.25	± 2	8 (100 μA)	± 100	1250	145	NA*
Conventional VDTA	0.18	± 0.9	2 (50 μA)	± 60	1400	370	3.2 mW
Proposed VDTA-I	0.18	± 0.9	3 (50 μA)	± 50	2400	160	1.5 mW
Proposed VDTA-II	0.18	± 0.9	2 (50 μA)	± 80	3600	630	2.67 mW

[a]NA* Not available.

It may be observed from the Table 6.2 that the proposed VDTA-I and VDTA-II offer much higher value of gm as compared to the conventional VDTA. Further, the VDTA-I outperforms in terms of transconductance, GBW product and the %THD among all the three structures. Further, drawing comparison with existing structures, it may be inferred that transconductances of the proposed VDTA-I and VDTA-II are much higher than the existing structures even at lower bias currents.

6.4 Conclusion

In this chapter, two new VDTA structures using the concept of transconductance boosting are presented. The first approach is based on a negative impedance realized using cross coupled amplifier while the later architecture incorporates an inverting amplifier. The functionality of the circuits is tested through Spice simulations using TSMC 0.18 μm technology node. The proposed VDTA-I provides high transconductance gain and lower power consumption at compromised bandwidth in comparison to conventional VDTA. The VDTA-II provides high gain and large bandwidth and consumes less power as compared to conventional VDTA. The VDTA-I consumes least power thereby making itself a potential candidate for low power high performance applications whereas the VDTA-II is more suitable for high frequency applications.

CHAPTER – 7

CONCLUSION AND FUTURE SCOPE

In this work VDTA based integer and fractional order circuits have been presented.

The VDTA comprises of two transconductance gain stages, so resistorless applications can be developed [11-53], which seems to be fairly a good advantage as all those problems which are associated with a resistor can be eliminated. Further, most of the applications can be realized using grounded capacitors; which is a suitable choice from integrated circuit view point. Additionally, electronic tuning can be achieved by controlling the DC bias currents.

Further, the application of the fractional order calculus in modelling physical processes and systems is gaining momentum due to its inherent ability to provide an additional/extra degree of freedom for better control mechanism. This approach offers for more accurate modelling of real-world phenomena and natural processes.

This Chapter presents a concise summary of the contributions and significant findings of the propositions presented in this thesis.

7.1 Summary of Work done

The introductory chapter of the thesis presents evolution of the analog building blocks; particularly, state of the art current mode blocks followed by the fractional order dynamics. Further, literature review/summary on VDTA based CMOS implementations and various integer and fractional order analog signal processing and generating applications has also been presented. This survey aided to identify significant research gaps in the domain which led to the potential areas where further research could be carried out. Lastly, organization of the thesis was also provided.

Chapter 2 presented preliminaries of the active block used in this work; that is, the VDTA. The functionality of the same is validated through simulations using Virtuoso from Cadence Spectre tool suite using 180 nm (gpdk) technology node. Additionally, the Chapter also presented detailed study and the implementation of the emulated fractional order capacitor, specifically focusing on the application of the Carlson and the continued fraction expansion based rational approximations. Further,

three ‘2α-order’ fractional order filters were designed, former is based on the Carlson method (first- till third- iteration with $\alpha = 0.5$) while the latter two are developed using fourth order CFE approximation for 0.5 to 0.9 in steps of 0.1.

In Chapter 3, an ‘α-order’ generic inductance emulator is proposed which based on the appropriate switch selection could be configured as (i) integer order positive inductor emulator (ii) integer order negative inductor emulator (iii) fractional order positive inductor emulator (iv) fractional order negative inductor emulator. Effect of non-ideal behaviour of the VDTA also been studied and specific case of the fractional order negative inductance has been presented in thesis for the sake of brevity. The workability of the generic inductance emulator is tested through simulations and experimentally. Further, the applicability of the proposed structure is verified through two application examples namely parasitic fractional order inductance cancellation and fractional order high pass filter.

In succession, in Chapter 4 design of a conventional second order filter which is followed by three ‘2α-order’ fractional order filter configurations is presented. The proposed classical analog filter is multi mode multiple input single output, providing multifunction responses. The first fractional order filter is a voltage mode MISO configuration which provides all five responses. The validation of the structure is done using Virtuoso where FC is emulated through Carlson approximation. The second and third fractional order filters are designed using CFE approximation.

In Chapter 5, two third order sinusoidal oscillators based on a single VDTA have been presented. Post deriving the characteristic equation, the corresponding frequency and condition of oscillation has been computed theoretically. In order to verify its performance, time domain analysis and its frequency spectrums are plotted for both the circuits using Pspice.

Lastly, in an attempt to present VDTA structures with improved gm, two transconductance boosted structures were proposed in Chapter 6. The former is based on well known partial positive feedback approach while the later is based on the gate to source voltage variation method for gain enhancement. Detailed high frequency small signal mathematical formulations has been computed for both the configurations. Further, in order to validate the performance, both the structures are characterized via DC and AC analyses and PVT (Process corners, supply voltages and temperature) variation.

Summary of the work presented in this thesis is placed in tabular manner in Table 7.1.

Table 7.1 Summary of the Work Presented in the Thesis.

Chapter	Structure/Topology/Configuration	ABB No. Type	Passive Elements	Analysis
1	Introduction (Background of the ABBs) Literature Review Thesis Organization			
2	Fundamentals of the Fractional Order Methods (FC Emulation): Carlson Approximation / Newton Method (first- till third- iteration) CFE Method (first- till fourth- order approximation)			
	VDTA (Port Relations & Impedance Properties, Characterization)			
3	Generic Inductance Emulator	1 VDTA	1 C/FC (Grounded)	Theoretical (Non-ideal) Simulations (Frequency Response, Transient) Experimental (Transient)
4	Analog Filter / Biquad (Multi-Mode MIMO)	1 VDTA	2C + 1R(G)	Sensitivity
	FOF-I [Carlson (0.5)]	1 VDTA	2FC	
	FOF-II [Carlson (0.5-0.9)]	1 VDTA	2FC (1G+1F)	Sensitivity
5	TOSO-I	1 VDTA	3C(G) + 2R(1G+1F)	Transient Output & Frequency Spectrum Frequency Tuning
	TOSO-II	1 VDTA	3C(G) + 3R(2G+1F)	Transient Output & Frequency Spectrum
6	VDTA-I	N.A.	N.A.	
	VDTA-II	N.A.	N.A.	
7	Conclusion and Future Scope			

7.2 Future Scope

In this thesis signal processing and generating applications have been explored in integer and fractional order domains using VDTA as a building block. Additionally, a new VDTA is also proposed. The proposed work may be extended further to address some of the following points:

1) Most of the fractional order designs have been explored using CFE approximation. Some other available approximations / new approximations may be explored for optimum realization of FOE.
2) The FO circuits designed may be used for different applications such as sensing low frequency signals and control application.
3) The concept of fractional calculus in signal generating applications may be explored.
4) FO domain inverse filters may be explored to nullify the noise introduced due to channel characteristics.
5) Further, VDTA structures may be explored using newer devices such as CNTFET, FinFET etc to leverage their advantages.

Research is an unending journey and always opens doors for further exploration. The presented work is a drop in vast ocean of knowledge created by other researchers in the field.

In the end the candidate would like to express gratitude to all learned reviewers of the proposed work, as their constructive comments have helped shape the presented thesis.

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