Analysis and Design of CMOS Multistage Amplifiers

A Thesis Submitted

In Partial Fulfilment of the Requirements

For the Degree of

DOCTOR OF PHILOSOPHY

in

Department of Electronics & Communication Engineering

by

Om Krishna Gupta
2K18/PhD/EC/513

Under the Supervision of

Prof. Neeta Pandey
Dept. of ECE
Delhi Technological University,
Delhi –110042

Prof. Maneesha Gupta
Dept. of ECE
Netaji Subhas University of Technology,
Delhi –110078

Department of Electronics & Communication Engineering,
Delhi Technological University,
Shahbad Daulatpur, Main Bawana Road
Delhi-110042
December 2024

CERTIFICATE

This is to certify that the thesis entitled "**Analysis and Design of CMOS Multistage Amplifiers"** submitted by Om Krishna Gupta (2K18/PhD/EC/513) to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi, for the award of the degree of Doctor of Philosophy is based on the original research work carried out by him under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirement of the regulations relating to the degree. It is further certified that the work presented in this thesis is not submitted to any other university or institution for the award of any other degree or diploma.

Prof. Neeta Pandey
Supervisor
Department of Electronics &
Communication Engineering,
Delhi Technological University,
Delhi –110042

Prof. Maneesha Gupta
Co-Supervisor
Department of Electronics &
Communication Engineering,
Netaji Subhas University of Technology,
Delhi –110078

DECLARATION

I hereby declare that the work presented in this thesis entitled "**ANALYSIS AND DESIGN OF CMOS MULTISTAGE AMPLIFIERS"** has been carried out by me under the supervision of **Prof. Neeta Pandey**, Department of Electronics & Communication Engineering, Delhi Technological University, Delhi and **Prof. Maneesha Gupta**, Department of Electronics & Communication Engineering, Netaji Subhas University of Technology, Delhi and is hereby submitted for the award of the degree of Doctor of Philosophy in Department of Electronics & Communication, Delhi Technological University, Delhi.

I further undertake that the work embodied in this thesis has not been submitted for the award of any other degree or diploma elsewhere.

Om Krishna Gupta

2K18/PhD/EC/513

ACKNOWLEDGMENT

It is indeed a great pleasure to thank all those who guided, supported and helped me in completing this research work. The grace of almighty God, blessings of my teachers and elders, strengthen my courage in the course of my research.

First and foremost, I express my deepest gratitude to my supervisors Prof. Neeta Pandey, Professor, Electronics and Communication Engineering Department, Delhi Technological University, New Delhi and Prof. Maneesha Gupta, Professor, Electronics and Communication Engineering Department, Netaji Subhas University of Technology, New Delhi for their valuable suggestions, guidance and encouragement during the research work.

I would like to acknowledge the reviewers of the research publications and conferences for their valuable suggestions.

Finally, I would like to express my sincere appreciation to all my family members and friends who helped me directly or indirectly for the successful completion of this research work.

Om Krishna Gupta

ABSTRACT

A multistage amplifier is an essential component of analog signal processing. Although it provides high gain but the complexity of the amplifier increases with the number of stages. Moreover, a multistage amplifier produces a large number of comparable poles and zeros, which causes the phase margin to deteriorate. As a result, the stability of the amplifier is reduced. Consequently, the frequency compensation techniques become crucial when designing multistage amplifiers in order to improve the stability of the amplifier. However, in addition to addressing the amplifier's stability, the frequency compensation technique should enhance the gain bandwidth product (GBW), phase margin, and slew rate of the amplifier. The key objective of this thesis is to propose improved three stage amplifiers using different frequency compensation techniques.

One of the conventional frequency compensation techniques called Reversed Nested Miller Compensation (RNMC) is widely used in three stage amplifiers. However, RNMC suffers with the problem of Right Half Plane (RHP) zero, which reduces the phase margin of the amplifier. In order to address the RHP zero problem of RNMC, the proposed amplifier 1 utilizes Flipped Voltage Follower (FVF) in the inner compensation loop of RNMC. Moreover, it improves the frequency response of the amplifier. Further, a feed forward path is employed to enhance the transient response of the amplifier.

Another variant of voltage follower called Folded Flipped Voltage Follower (FFVF) is exploited in the inner compensation loop of RNMC in the proposed amplifiers 2-5. It resolves the RHP zero issue and improves the Gain Bandwidth Product (GBW) of the amplifiers. Moreover, the proposed amplifiers 3-5 also make use of a resistor in the outer compensation loop. It results in double pole-zero cancellation, which enhances the phase margin.

Additionally, the proposed amplifiers 4 and 5 employ the self cascode structure and DTMOS transistors in the input stage, respectively. This results in better GBW of the amplifiers. The proposed amplifiers 2-5 also take advantage of the feed forward path to improve the transient response.

Further, an active LHP zero circuit is employed in the proposed amplifiers 6-9 to cancel the parasitic pole of the second stage. It enhances the GBW of the amplifiers. Additionally, a Miller capacitor with resistor ensures the stability of the amplifiers. Moreover, a self cascode structure and self cascode with DTMOS are used in the input stage of the proposed amplifiers 6 and 7, respectively. It results in better GBW of the amplifiers. The GBW is further enhanced by employing a modified self cascode structure in the first stage of the proposed amplifiers 8 and 9. Moreover, a feed forward path is exploited to improve the transient response of the proposed amplifiers 6-9.

To further enhance the frequency response of three stage amplifiers, a class AB FVF is utilized in the inner compensation loop of RNMC in the proposed amplifiers 10 and 11. Additionally, a slew rate enhancer circuit and a feed forward path are exploited to improve the transient response.

In this thesis, the small signal analysis is performed for all proposed amplifiers to find out the transfer function, which helps in evaluating the GBW and the stability of the amplifiers. Further, the performance of all proposed amplifiers is compared with their counterparts. The functionality of the proposed amplifiers is verified using TSMC 0.18 μm CMOS technology parameters in Tanner tool. Corner analysis, supply voltage variation, and Monte Carlo analysis are carried out to confirm the robustness of the proposed amplifiers.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

1.1 Motivation

The amplifiers are essential building blocks of cutting-edge integrated systems and are used in reference circuits, data converters, and linear regulators. Further, it is imperative to use amplifiers as front end in the applications where data sensed from the environment is to be processed. The data so sensed is very small in magnitude and need to be amplified before it can be processed. The amplifier design has become increasingly more challenging with the scaling down of the feature size and supply voltages. With a reduction in channel length, the unity gain bandwidth of the amplifier improves, whereas the open loop gain deteriorates. Therefore, it becomes difficult to achieve large gain and wide bandwidth using single stage amplifiers in sub-micron technologies, pushing researchers to switch to an alternative route to multistage designs.

1.2 Multistage Amplifiers

Multistage amplifiers rely on cascading of gain stages for improving the gain. In addition to providing gain, the input stage is usually required to provide a high input resistance in order to avoid loss of signal level when the amplifier is fed from a high resistance source and to combat the effect of noise. To achieve it, a differential amplifier is used in the input stage, which must provide large common mode rejection. The function of the middle stages of a multistage amplifier is to provide the bulk of voltage gain. In addition, the middle stages provide other functions, such as the conversion of the signal from differential mode to single-ended mode and the shifting of the DC level of the signal in order to allow the output signal to swing both positive and negative. Finally, the main function of the last or output stage of an amplifier is to provide a low output resistance in order to avoid loss of gain. Also, the output stage should be able to supply the current required by the load in an efficient manner [1].

Moreover, multistage OTA gives high DC gain, but it also gives high number of comparable poles and zeros, which exhibits low phase margin, leading to stability issues.

The multiple-pole nature of the multistage amplifiers causes closed loop stability issues. It is pertinent to mention that the phase crossover point is moved closer to the origin as a result of further negative phase shift caused by a zero in the right half plane. According to Bode approximations, the zero pushes the gain crossover away from the origin by slowing down the magnitude drop. Consequently, the stability is reduced considerably. Necessary measures are required so that the gain crossover point moves towards the origin. To achieve this, the

dominant pole frequency may simply be lowered by increasing the load capacitance, but due to the presence of the non-dominant pole, which is near the dominant pole, the gain cross over point moves away from the origin, which is a big threat to stability [2-3]. To ensure closed loop stability, frequency compensation is mandatory. Various frequency compensation techniques are proposed in the literature for multistage amplifiers.

1.3 Frequency Compensation Technique

A two-stage amplifier with Miller compensation [2] is depicted in Fig. 1.1, which uses a compensation capacitor C_C. Here, the voltage gains of the first stage and second stage are denoted by A_{v1} and A_{v2}. The idea of Miller compensation is to move the low frequency pole (dominant pole) towards the origin and the other pole away from the origin. It makes the gain cross over frequency less than the phase crossover frequency, which enhances the stability of the amplifier. The compensation capacitor C_c creates a large capacitance at the input of the second stage (node E), equal to $(1 + A_{v2})\ C_c$. It effectively moves the dominant pole to $\frac{1}{R_{out1}\left[C_E + \left(1 + A_{v2}\right) C_C\right]}$, where C_E denotes the capacitance at node E before C_c is added, and R_{out1} is the output resistance of the first stage. As a result, a low frequency pole can be established with a moderate capacitor value, saving considerable chip area. In addition to lowering the required capacitor value, Miller compensation moves the output pole away from the origin. This effect is called pole splitting (Fig. 1.2). Since the Miller loop should exhibit a negative gain for stability, therefore, the second stage is the inverting amplifier in order to create favorable condition for Miller's effect.

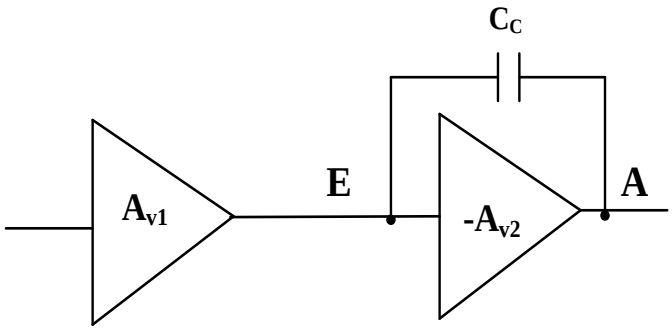


Fig. 1.1 Miller compensation of two-stage op amp

Fig. 1.2 Pole Splitting as a result of Miller compensation

1.4 Literature review of frequency compensation techniques

Since single stage amplifiers do not provide sufficient gain for many applications, it is imperative to use multistage amplifiers. Due to high number of comparable poles and zeros, multistage amplifiers need to be compensated for stability. In the literature, various frequency compensation techniques are proposed for multistage amplifiers for different capacitive loads. A brief description of frequency compensation techniques for two stage & three stage amplifiers is given below.

Frequency Compensation Techniques for Two Stage Amplifier:

The implementation of a simple Miller compensation scheme is accountable for a RHP zero due to the forward path to the output through the compensation capacitor. This RHP zero degrades the stability. In order to address the RHP zero problem, frequency compensation using nulling resistor, voltage buffer and current buffer are proposed in the literature [4-5]. Ref. [4] uses a simple Miller compensation with a resistor R_c along with a capacitor C_c to break

the forward path (Fig. 1.3). Additionally, the block diagram of a two-stage amplifier that improves the GBW and PM by using the voltage buffer and current buffer in the Miller compensation loop is displayed in Figs. 1.4–1.5 [4-5].

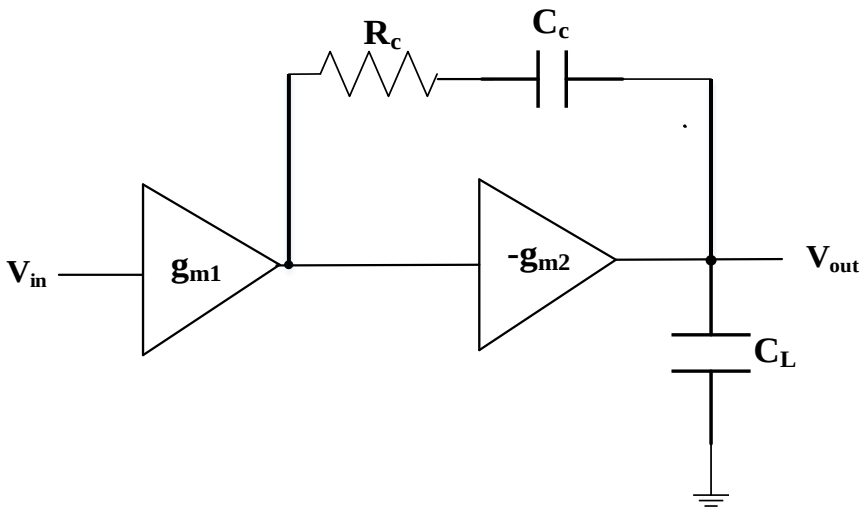


Fig. 1.3 Miller Compensation with Nulling Resistor

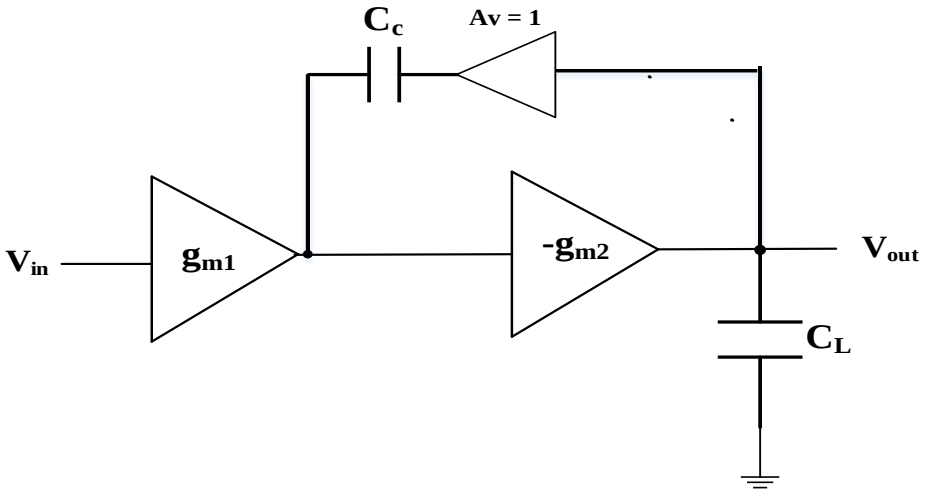


Fig. 1.4 Miller Compensation with Voltage Buffer

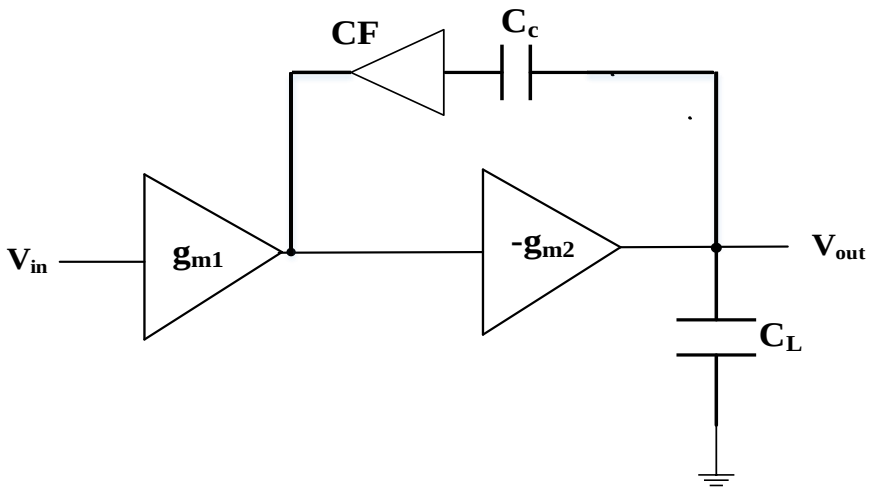


Fig. 1.5 Miller Compensation with Current Buffer

Moreover, voltage buffer compensation using flipped voltage follower (FVF) and folded flipped voltage follower (FFVF) improves the performance of two stage amplifier in terms of GBW [6]. Frequency compensation using negative capacitance and a flipped voltage follower is proposed, which improves GBW and PM [7]. In Ref. [7], negative capacitance reduces the parasitic capacitance of a particular stage, which enhances GBW. Further, the pole-zero cancellation is achieved with the help of FVF, which improves phase margin. Ref. [8] offers feed forward compensation in two stage amplifiers, which creates a LHP zero, resulting in higher GBW and PM.

Frequency compensation using positive feedback, positive capacitive feedback, and positive resistive-capacitive feedback gives an extra LHP zero to cancel a pole, which improves GBW [9-11]. Furthermore, in the positive feedback compensation technique, the amplifier's stability is less sensitive to the capacitive load. Compared to Miller compensation with the same compensation capacitance, pseudo cascode compensation improves GBW and large signal settling response [12]. Moreover, a bulk-biasing technique has been employed in [12] to increase the two stage op-amp's DC gain without changing the output voltage swing and without requiring more power. Gain-boosting and indirect current feedback frequency compensation performed by regulated cascode amplifier is suggested in [13], which enhances the low frequency gain and phase margin with a reduction in settling time. Further, one of the low voltage lower technique (LVLP), Quasi-Floating Gate MOSFET (QFGMOS) is employed

in [13] to reduce the power supply requirement. In Ref. [14], a hybrid class A/AB two stage OTA has been presented, which includes a folded cascode in the first stage and active current mirrors in the second stage in order to increase the speed of the amplifier. In order to achieve class-AB operation, the Class AB-AB Miller op-amp described in [15] uses a transconductance boosting technique based on local common-mode feedback. This leads to improved open-loop gain, GBW, and slew rate without appreciably raising the quiescent power consumption. Further, Miller and phase-lead compensation provide the stability over wide range of capacitive loads in [15].

The compensation capacitor is simply reconnected in [16] to enhance the bandwidth without requiring additional power dissipation. Moreover, improvements in power-supply rejection ratio (PSRR) and slew rate are obtained in [16]. A two-stage fully differential CMOS amplifier includes inverters as input structures with self-biasing technique is put forward in [17], which results in high energy efficiency and low power consumption. Embedded capacitor multiplier frequency compensation technique is suggested in [18] to improve the stability and slew rate with lesser area and power consumption.

Since the gain requirement is high for many applications, such a high gain has not been achieved by two stage amplifiers in the literature. So, the need for three stage amplifiers arises.

Frequency Compensation Techniques for Three Stage Amplifier:

There are two conventional frequency compensation techniques for three stage amplifiers in the literature. One of the conventional frequency compensation technique is Nested Miller Compensation (NMC) [19]. Figure 1.6 dispalys the block diagram of NMC. It uses simple Miller compensation in both of its inner compensation loop and outer compensation loop with the help of two compensation capacitors. However, both the compensation capacitors load the output node, which results in a reduction in bandwidth. Further, NMC suffers with the problem of RHP zero. To address the RHP zero problem of NMC, a resistor R_c is connected in series with compensation capacitors, which is used to break the feed forward path [20]. It is shown in Fig. 1.7. It improves the phase margin by cancelling the RHP zero while keeping the LHP zero, thus resulting in higher stability of the circuit. Using an extra feed forward path, Multipath NMC (MNMC) increases the bandwidth of the original NMC structure [21]. Figure 1.8 displays the block diagram of MNMC. In contrast to the NMC structure, it provides an extra LHP zero.

This LHP zero can be used to cancel out the second non-dominant pole of the amplifier, which enhances the gain-bandwidth product of the amplifier.

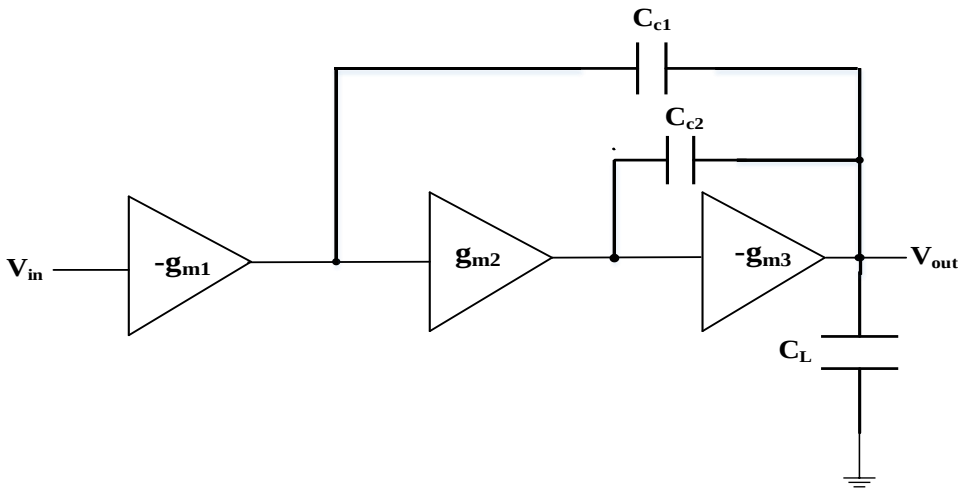


Fig. 1.6 Nested Miller Compensation

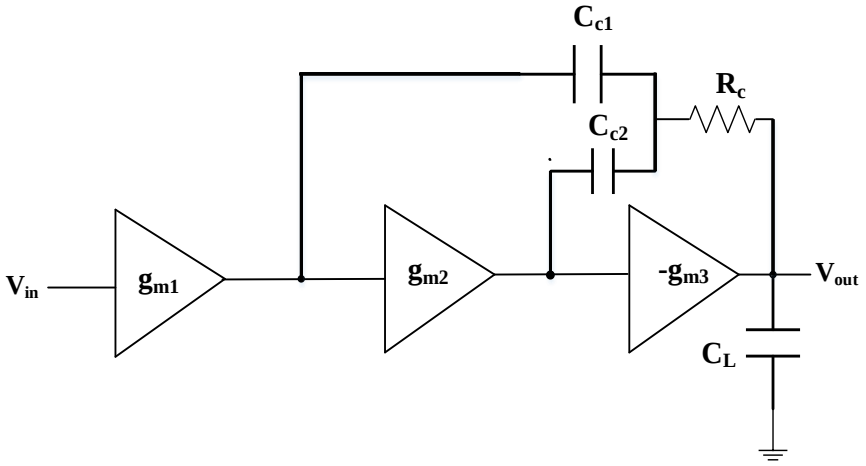


Fig. 1.7 NMC with Nulling Resistor

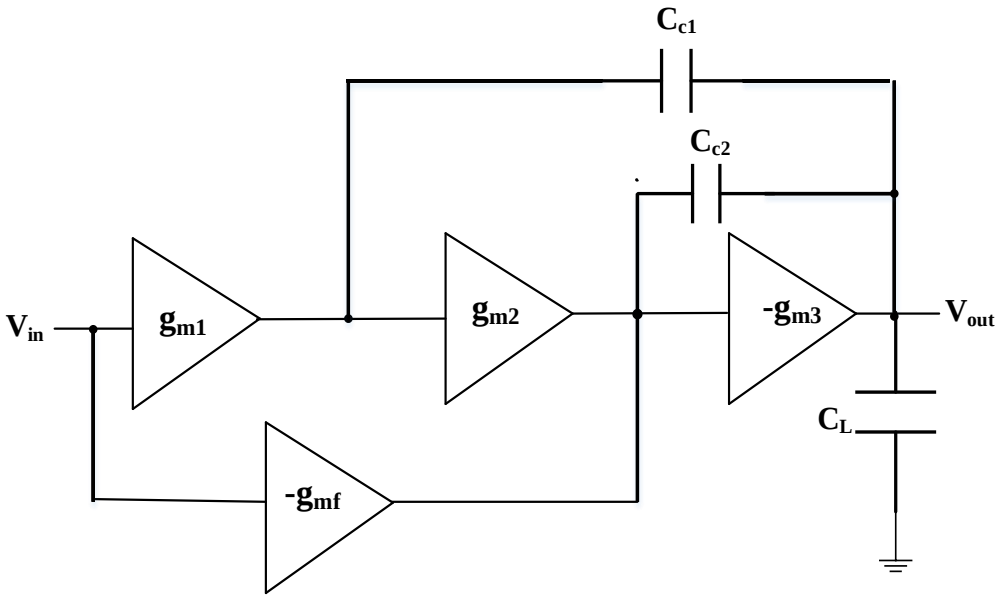


Fig. 1.8 Multipath NMC

Further, Nested Transconductance-Capacitance Compensation (NGCC) is proposed, which offers better GBW than NMC [22]. Moreover, NMC with feed forward stage (NMCF) and damping-factor-control frequency compensation (DFCFC) are employed to improve the frequency response and transient response [23]. Ref. [24] adds a Nested feed-forward transconductance stage and a nulling Resistor to NMC, which enhances GBW, phase margin and slew rate of three stage amplifier.

Figure 1.9 shows the block diagram of another conventional technique, Reversed Nested Miller Compensation (RNMC) [25]. OTA based on RNMC shows higher GBW and better performance compared to NMC due to the independence of inner compensation capacitor from output. Further, RNMC has RHP zero in its transfer function. This RHP zero degrades the stability of the amplifier. To cancel this RHP zero, various techniques have been proposed by the authors in the literature, such as RNMC with nulling resistor, voltage follower and current follower [25], and are shown in Figs. 1.10-1.12. These techniques break the feed forward path, while maintaining the LHP zero and shift the RHP zero to a very high frequency, which results in higher phase margin of the circuit. Further, Ref. [26] results in double pole-zero cancellation by using a resistor in the outer compensation loop and a voltage buffer in the inner

compensation loop of RNMC, which further enhances the phase margin (Fig. 1.13). A feed forward path is added to improve the transient response in [26].

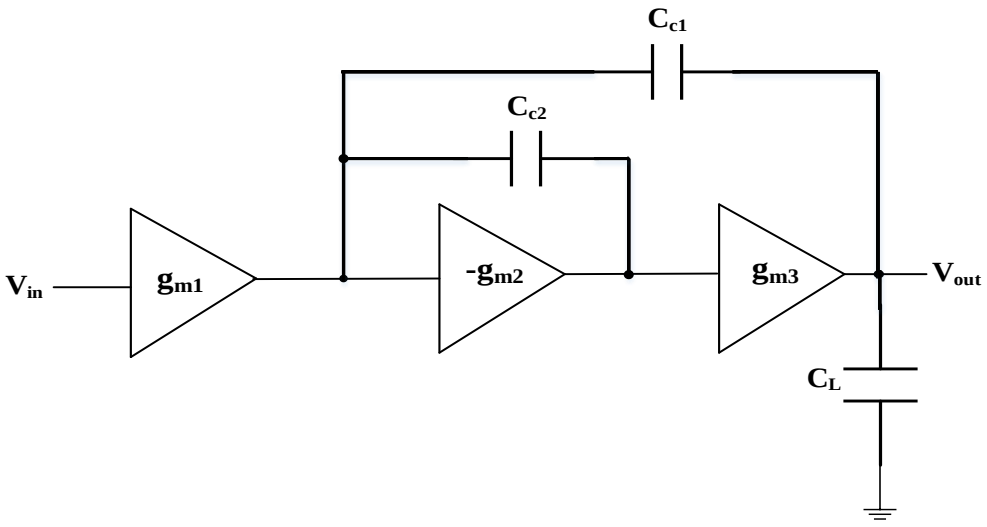


Fig. 1.9 Reversed Nested Miller Compensation

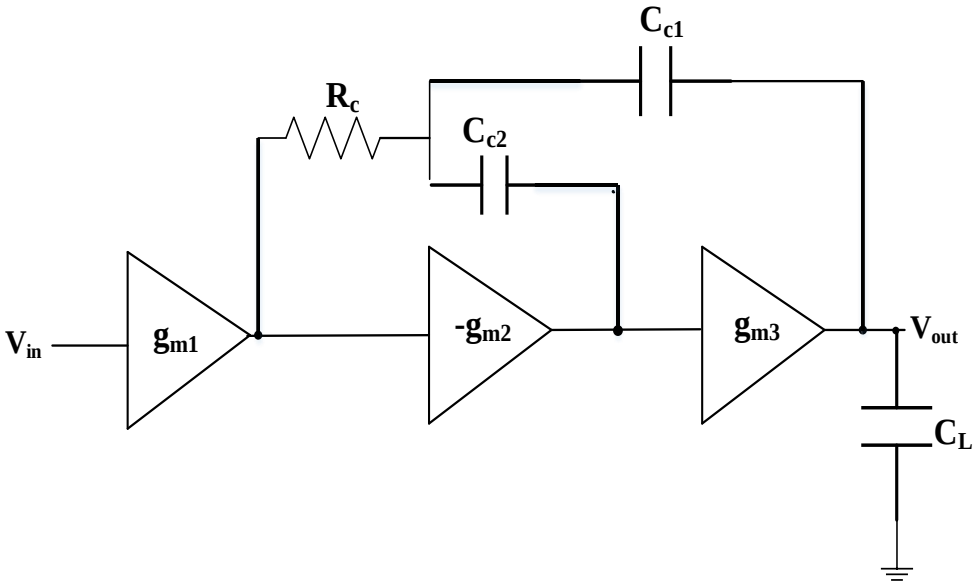


Fig. 1.10 RNMC with Nulling Resistor

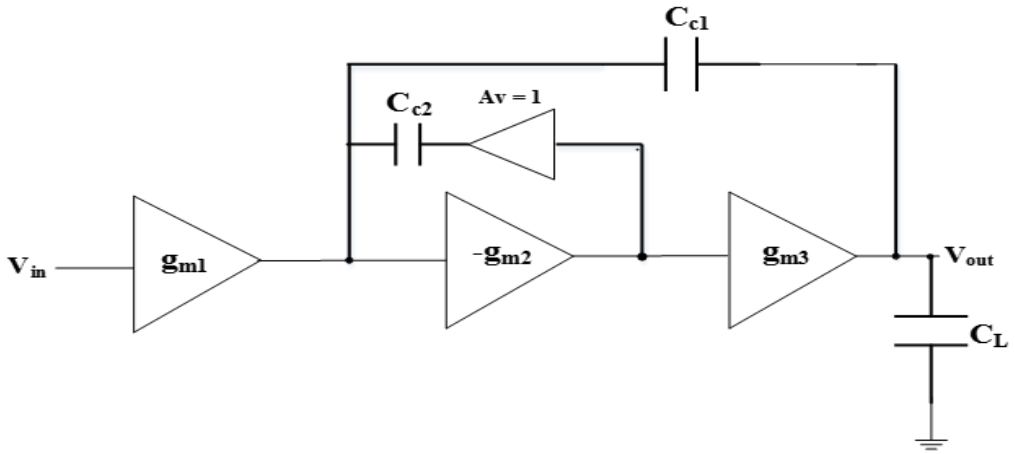


Fig. 1.11 RNMC with Voltage Buffer

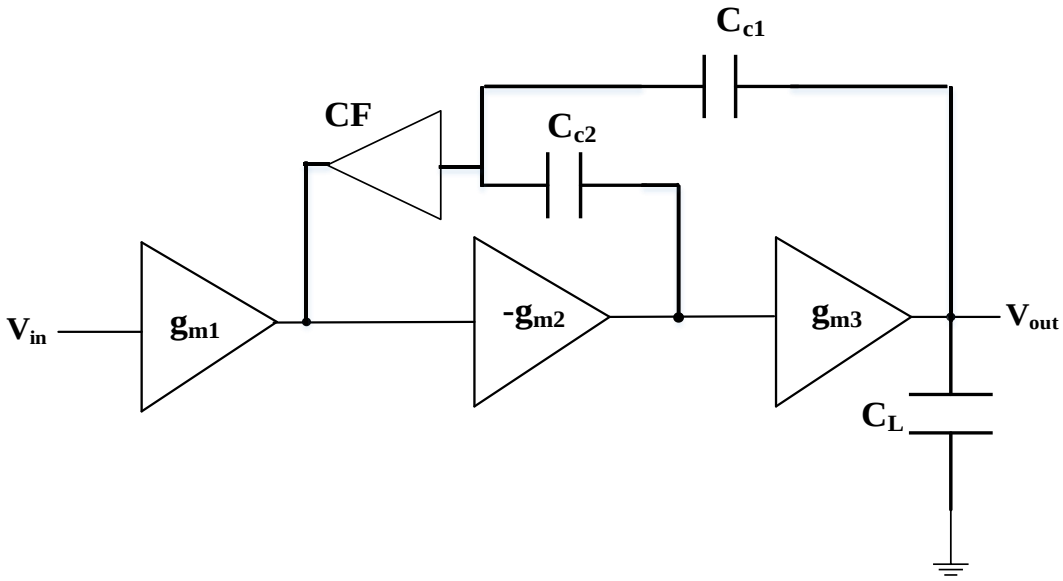


Fig. 1.12 RNMC with Current Buffer

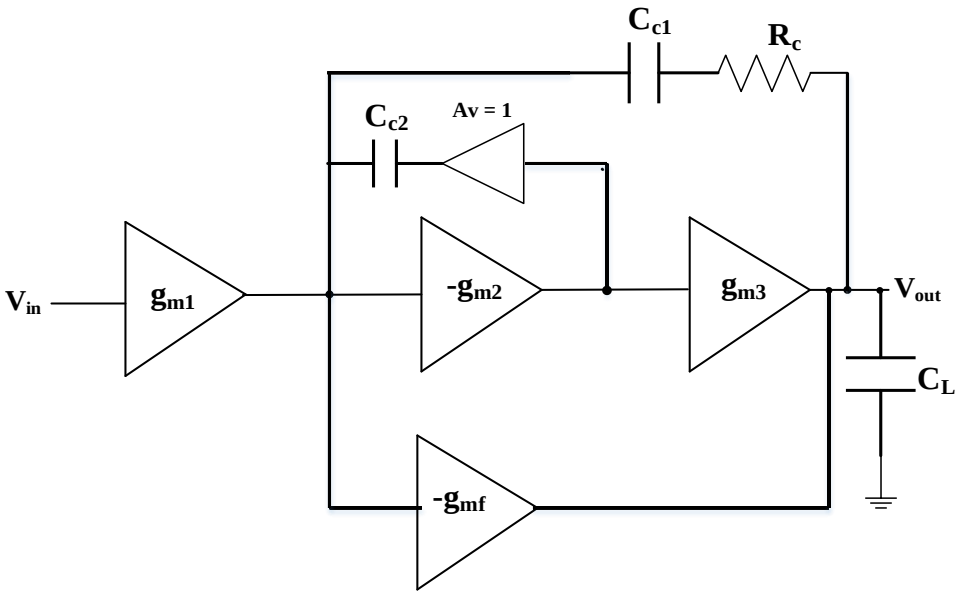


Fig. 1.13 RNMC with Voltage Buffer and Resistor

Reversed Active Feedback Frequency Compensation (RAFFC) employs the current buffer in the outer compensation loop [27]. Figure 1.14 displays the block diagram of RAFFC. In RAFFC, the removal of zero is more reliable because it does not demand matching between resistance and transconductances. Further, the feed forward path has been added to enhance the large signal response.

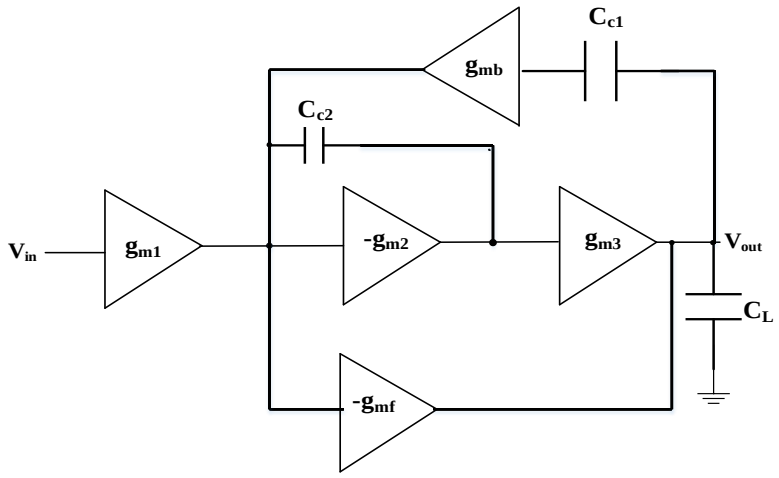


Fig. 1.14 Reversed Active Feedback Frequency Compensation

Many other frequency compensation techniques using RNMC have been proposed for high capacitive load in the literature. Ref. [28] utilizes a current subtractor in the common node of Miller capacitors of RNMC to remove the feed forward path and RHP zero. RNMC with a current comparator in the feedback path is presented in [29] to achieve higher GBW and phase margin. A Second generation Differential Current Conveyor (DCCII) in the feedback path from output of the second and third stage to the output of first stage is suggested in [30] to remove the feed forward path and RHP zero, resulting in enhanced GBW and PM. Further, by using a single compensation capacitor and differential amplifier in third stage, adverse effects of feedback and feed forward paths are reduced simultaneously [31]. So, it removes the need of using voltage or current buffer. Further, [28-31] suffers with low figure of merits. In Ref. [32], analytical formulation of various RNMC based topologies has been elucidated. Moreover, [32] compares RNMC based topologies on the basis of figure of merits, which shows that RNMC with feed forward, voltage buffer, and two resistors offers a better FOM than other RNMC topologies. Apart from these, a dual complex pole-zero cancellation frequency compensation scheme employing one pair of complex zeros to cancel one pair of complex poles is suggested in [33] to improve bandwidth and phase margin. Further, a current buffer along with Miller capacitor is connected between output of first and third stage to improve the figure of merits [34]. Moreover, [34] utilizes the feature of an active LHP zero circuit to enhance the frequency response. Embedded capacitor-multiplier compensation and active parallel compensation are put forward in [35] to enhance the area efficiency. Further, GBW is improved due to transconductance boosting technique in [35]. Negative capacitance circuit is utilized in [36] to minimize the parasitics capacitance of the critical node, which moves the non-dominant pole to higher frequency. It results in higher GBW. However, [34-36] endures low FOM. The local feedback enhanced compensation scheme is suggested in [37] for improving GBW. Some other techniques used for this purpose are - dual active capacitive feedback compensation under the variation of the load capacitance [38], cross feed forward cascode compensation [39], and active single Miller capacitor compensation with inner half-feed forward stage [40]. A slew rate enhancer circuit is also used in [40] to improve large signal performance. Damping-Factor-Control frequency compensation presented in [41] enhances the GBW and improves the transient response of amplifier for large capacitive load. Active-Feedback frequency compensation is put forward in [42], which simultaneously

enhances gain and GBW. Further stability and transient response are also improved due to the presence of LHP zero. An AC Boosting compensation scheme presented in [43] adds ac path to the internal stage of three stage amplifier to improve GBW and slew rate. Ref. [44] uses a serial R-C branch and current buffer to enhance the frequency response of three stage amplifier. In Ref. [45], the frequency of non-dominant complex pole is boosted using cascode Miller compensation. Moreover, the step response is enhanced using a feed forward transconductance stage and the stability is improved with the help of LHP zero. Hybrid active Miller enhancement compensation is used in [46] to increase GBW and PM. Additionally, [46] employs a slew rate enhancement method to further improve the transient response. Single Miller capacitor frequency compensation techniques are analytically compared in [47]. Ref. [48] offers multistage amplifiers, which can drive a wide range of capacitive loads using low-frequency zeros. Further, [49] suggests a three stage amplifier with a Miller capacitor and a small feed forward capacitor to improve the stability of the amplifier for a wide range of load capacitors. The frequency compensation using cascade zero is employed in [50] to enhance the gain of three stage amplifier. Moreover, [51] presents folded cascode OTA at lower supply voltage by using current driven bulk technique, while design techniques to operate OTA at low supply voltage are proposed in [52]. A feed forward transconductance stage and indirect compensation capacitor combined with a resistor are suggested in [53] to improve the stability of the amplifier. In Ref. [54], the complex-pole frequency of the amplifier is extended by eliminating the inner Miller capacitor and utilizing cascode Miller compensation in the outer compensation loop, which results in higher GBW. Further, an optimized trade-off between the frequency and the quality factor of the complex pole is achieved by using a local impedance attenuation block in [54]. In Ref. [55], second-stage bypass compensation scheme for three stage amplifier is presented, in which the second stage is bypassed using a capacitive feed forward path, thus reducing the amplifier to a two-stage. Further, unity closed loop gain stability of [55] is ensured using a conventional two-stage compensation technique.

Ref. [56] employs a nonlinear current mirror in the input stage to realize class AB operation, which enhances the slew rate of the amplifier. Auxiliary feedback is used in [57] to reduce the total compensation capacitance, resulting in higher GBW and slew rate. A three gain stage topology with class AB output stage is put forward in [58] to improve the driving capability of the amplifier. Further, Reversed Nested Indirect Compensated (RNIC) topology is

employed in [59], which reduces the settling time of the amplifier. Ref. [60] increases the slew rate of the amplifier by providing more current to the output node while avoiding an excessively high increase in power consumption. In Ref. [61], the transconductance stage in the internal feedback loop of NMC is utilized to improve GBW and the stability of the amplifier. Further, the feed forward stage in [61] improves the large signal performance of the amplifier. A single Miller capacitor with a resistor and feed forward path is introduced in [62] to improve the frequency response and transient response. Moreover, [63] employs a single Miller capacitor with current buffer and slew rate enhancer circuit, which improves the figure of merits of three stage amplifier. In Ref. [64], GBW is improved by using an attenuator in the path of Miller compensation capacitor. Moreover, a feed forward path is employed to deal with the LHP zero in [64]. It cancels out the first non-dominant pole. Another feed forward path in [64] forms push-pull output stage, which enhances the transient response. Further, sensitivity and robustness analysis of different three stage amplifiers are performed in [65].

Ref. [66] utilizes one of the low voltage low power (LVLP) technique, called Floating Gate MOS (FGMOS), to reduce the power supply requirement of the three stage amplifier. It reduces the power consumed by the circuit. Further in [66], an active LHP zero circuit and a resistor are used to improve GBW.

Further, following Figure of Merits (FOMs) are used to compare the results obtained from different frequency compensation techniques [43]. Eqs. 1.1-1.4 describe the four figures of merits.

$$\mathrm{FOM_S} = \frac{GBW \times C_L}{Power}\left(\frac{Hz \times F}{W}\right) \tag{1.1}$$

$$\mathrm{FOM_L} = \frac{SR \times C_L}{Power}\left(\frac{1}{V}\right) \tag{1.2}$$

$$\mathrm{IFOM_S} = \frac{GBW \times C_L}{I_B}\left(\frac{Hz \times F}{A}\right) \tag{1.3}$$

$$\mathrm{IFOM_L} = \frac{SR \times C_L}{I_B} \tag{1.4}$$

In the above equations, index S and L denote the small-signal mode and large-signal mode, respectively. I_B is the total bias current. A higher value of the figure of merits is desirable for any amplifier.

1.5 Research gaps

There is a range of performance metrices to be taken into account while designing multistage amplifiers, such as GBW, stability, power consumption, DC gain, noise, CMRR, slew rate, etc. It is desirable to have high gain, large GBW, optimum phase margin, high slew rate, high CMRR and less power consumption for wide range of capacitive loads for any multistage amplifier. Following are the observations from the literature review:

(i) There are many applications which require the ability to drive large capacitive loads, e.g. low dropout regulators (LDO), peak detectors, MEMS devices, LCD drivers etc. [63]. In the literature, various multistage amplifiers are proposed for high capacitive load, however, GBW is limited for high capacitive load. Also, there is a scope for improvement in GBW for multistage amplifiers for low and moderate value of capacitive load.

(ii) Slew rate defines how quickly the output changes with time. It should be high for any amplifier. In the literature, slew rate is limited for multistage amplifiers at high capacitive load. There is a scope for further improvement in slew rate for multistage amplifiers to increase the speed of the circuit for different capacitive loads.

(iii) Figure of merits (FOM) are used to compare the results obtained from different frequency compensation techniques. It should be high for any multistage amplifier. In the literature, figure of merits (FOM) are limited for multistage amplifier. There is a scope of further improvement in figure of merits for multistage amplifier.

(iv) The use of Low-Voltage Low-Power (LVLP) techniques such as Bulk Driven technique, Dynamic Threshold Voltage MOSFET (DTMOS), Floating Gate MOS (FGMOS), and Quasi Floating gate MOS (QFGMOS) is limited in the literature. These techniques can be further explored for three stage amplifiers.

1.6 Research objectives

On the basis of the research gaps, the following objectives are formulated:

(i) Develop compensation technique for better frequency response of multistage amplifiers.

(ii) Design of multistage amplifiers with improved transient response and/or figure of merits.

(iii) Apply low voltage/low power techniques to improve performance of multistage amplifiers.

1.7 Key contributions

This thesis discusses different frequency compensation techniques applied in a three stage amplifier to enhance the performance of the amplifier. The key contributions are listed below.

(i) A Flipped Voltage Follower (FVF) is utilized in the inner loop of Reversed Nested Miller Compensation (RNMC) to address the RHP zero problem. This compensation technique enhances the GBW. Moreover, the push pull output stage is used to enhance the slew rate.

(ii) The frequency response of three stage amplifier is improved with the help of Folded Flipped Voltage Follower (FFVF) in the inner loop of RNMC. Further, the transient response is enhanced using feed forward path.

(iii) RNMC makes use of FFVF and resistor in the inner and outer compensation loop, which results in double pole-zero cancellation. It improves the frequency response of the amplifier. Additionally, the transient response gets better due to feed forward path.

(iv) In order to refine the frequency response and transient response of three stage amplifier, Dynamic Threshold Voltage MOSFET (DTMOS) and self cascode structure are employed along with FFVF with resistor and feed forward path.

(v) An active LHP zero circuit is used to cancel the parasitic pole of the second stage to improve GBW of the amplifier. Moreover, a self cascode structure in the input stage and a Miller capacitor with resistor make the frequency response better. Additionally, a self cascode structure with DTMOS in the input stage and a Miller capacitor with resistor further enhance the GBW.

(vi) Modified self cascode with active LHP zero circuit and a single Miller capacitor with resistor improve the GBW of three stage amplifier.

(vii) Enhanced frequency compensation of a three stage amplifier is achieved by employing class AB FVF, a slew rate enhancer circuit, and push pull output stage in RNMC.

1.8 Organization of the thesis

This research focuses on enhanced frequency compensation of three stage amplifier. This thesis is organized into seven chapters, which are briefly explained below.

Chapter 1: This chapter outlines multistage amplifiers and frequency compensation techniques. Moreover, the frequency compensation techniques available in the literature are reviewed and classified on the basis of performance parameters. After the review of available compensation techniques, research gaps are identified, and research objectives are formulated.

Chapter 2: This chapter describes the different frequency compensation techniques used in the proposed work, such as Reversed Nested Miller Compensation (RNMC), Flipped Voltage Follower (FVF), class AB FVF, folded FVF, push pull output stage, slew rate enhancer circuit, self-cascode structure, Dynamic Threshold Voltage MOSFET (DTMOS), self-cascode with DTMOS, modified self-cascode, and active LHP zero circuit. The significance of these techniques to enhance the performance of the amplifier is discussed throughout the chapter.

Chapter 3: Frequency compensation using FVF along with one of the conventional compensation techniques, RNMC, is elaborated in this chapter. FVF is used to break the forward path of RNMC to resolve the RHP zero issue. This technique also utilizes the feed forward path to improve the transient response. Small signal analysis of the amplifier has been performed in this chapter. Moreover, simulation results are discussed to verify the performance of the amplifier.

Chapter 4: This chapter proposes the amplifiers, which utilize folded FVF (FFVF) to break the forward path of RNMC to solve the RHP zero problem. Moreover, a resistor along with FFVF has been exploited in the compensation loops of RNMC, which results in double pole-zero cancellation. This technique offers better frequency response. Further, DTMOS and self cascode structures are employed in the input stage of the amplifier to improve GBW.

Additionally, the feed forward path makes the transient response better. Moreover, this chapter examines the small signal analysis and simulation results of the proposed amplifiers.

Chapter 5: This chapter presents the frequency compensation of three stage amplifiers using an active LHP zero circuit to cancel the parasitic pole of second stage, which improves GBW. Additionally, self cascode structure, self cascode with DTMOS, modified self cascode and a Miller capacitor with resistor enhance the frequency response of the proposed amplifiers. Small signal analysis of the circuits is performed, and simulation results are shown to verify the effectiveness of the proposed circuits.

Chapter 6: Frequency compensation using class AB FVF, along with RNMC, is presented in this chapter. Class AB FVF is used to break the forward path of RNMC to address the RHP zero issue. This technique also utilizes the feed forward path to enhance the transient response. Further, a slew rate enhancer circuit is employed along with class AB FVF to improve the large signal response. Small signal analysis of the amplifiers has been performed in this chapter. Moreover, simulation results are discussed to verify the performance of the amplifiers.

Chapter 7: It concludes all the proposed three stage amplifiers to improve the frequency response and transient response. All simulations are performed using TSMC 0.18 μm CMOS process in Tanner tool to examine the functionality and performance of the proposed amplifiers. It is illustrated that the simulation results of the proposed amplifiers match up with the theoretical results. Additionally, this chapter also suggests possible future work.

Chapter 2

Various frequency compensation techniques used in proposed amplifiers

2.1 Introduction

The improvement in the performance of amplifiers is required continuously due to the rapid advancement in technology and the scaling down of the supply voltage. In this regard, single stage amplifiers suffer from low gain and low bandwidth. Therefore, multistage amplifiers become mandatory. Further, multistage amplifiers come with frequency compensation to address the stability problem. Researchers have proposed various frequency compensation techniques over the last few decades. However, there is still scope for improving the frequency compensation techniques. In this thesis, eleven three stage amplifiers are proposed with enhanced performance. This chapter briefly describes the techniques employed in the proposed amplifiers to improve the performance of the amplifiers The organization of this chapter is as follows: Section 2.2 describes one of the conventional frequency compensation techniques, Reversed Nested Miller Compensation (RNMC), while Sections 2.3 to 2.5 include Flipped Voltage Follower (FVF), class AB FVF, and folded FVF. Moreover, the push pull output stage and slew rate enhancer circuit are elucidated in Sections 2.6 and 2.7, respectively. Dynamic Threshold Voltage MOSFET (DTMOS), self cascode structure, self cascode with DTMOS, modified self cascode, and active LHP zero circuit are detailed in Sections 2.8 to 2.12. Section 2.13 provides the summary of the chapter.

2.2 Reversed Nested Miller Compensation (RNMC) [25]

The main difficulty in the design of multistage amplifiers is performing frequency compensation due to increased high impedance nodes. Also, it is required to fulfill the stability criterion for a multistage amplifier with adequate GBW and phase margin of the amplifier. To deal with it, RNMC technique (shown in Fig. 2.1) can be used due to its independency of the inner compensation capacitor from the output. It helps in improving the GBW of the amplifier. This technique is widely used due to its simplicity of design and no extra power consumption. However, it has RHP zero in its transfer function, which degrades the phase margin.

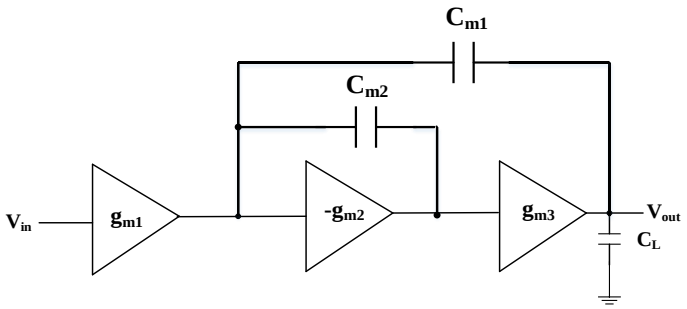


Fig. 2.1 Reversed nested Miller compensation technique

Figure 2.2 shows the circuit diagram of a three stage amplifier with RNMC. In Fig. 2.2, transistors M1-M4 and M6 form the differential amplifier for the first stage. Transistors M7-M8 form the second stage, which is a common source amplifier; followed by a non-inverting stage, which constitutes the third stage (M9-M12). Apart from this, two Miller capacitors, C_{c1} and C_{c2}, are connected in the feedback loop.

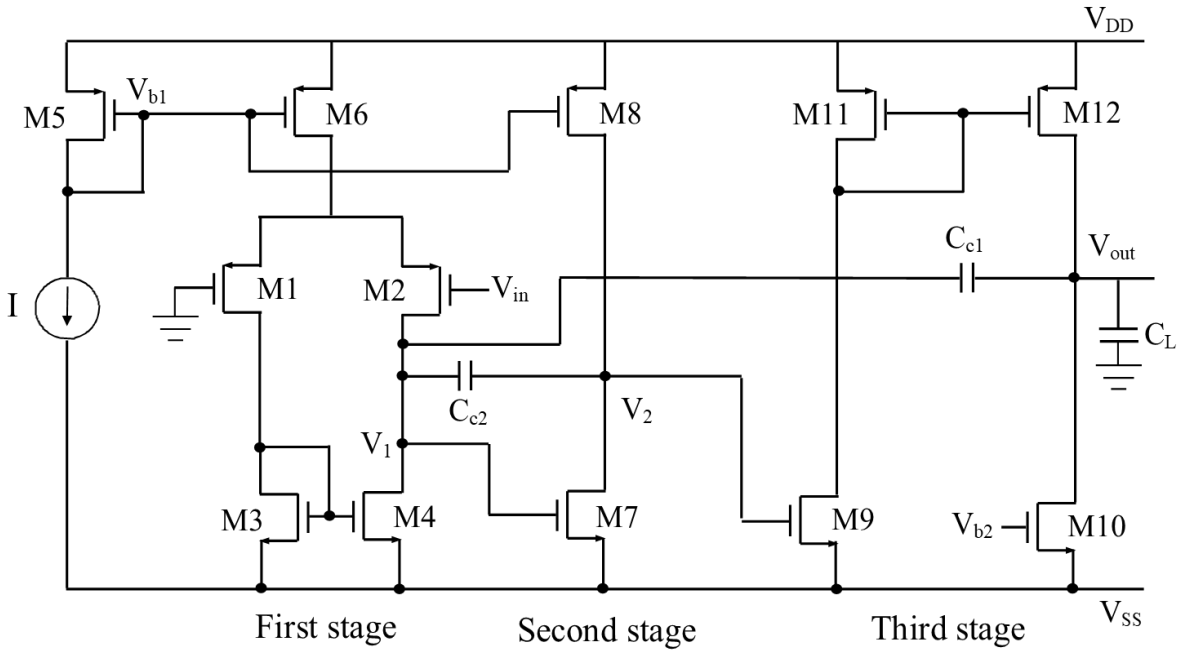


Fig. 2.2 Circuit Diagram of three stage amplifier with RNMC

A small signal equivalent circuit of a three stage amplifier using RNMC is described in Fig. 2.3. In this figure, the input stage has output resistance r_{o1}, output capacitance $C_{1,}$ transconductance g_{m1}, and output voltage V_1. The second stage has output resistance, output

capacitance, and output voltage of $r_{o2,}$ C_2, and V_2 with transconductance g_{m2}. Final stage possesses output resistance r_{o3}, transconductance g_{m3}, total equivalent load capacitance C_L, and output voltage V_{out}. Apart from this, two Miller capacitors, C_{c1} and C_{c2}, are connected in the feedback loop. The compensation capacitor C_{c1} is connected between the output of the third stage and the first stage, while C_{c2} is connected between the output of the second stage and the first stage.

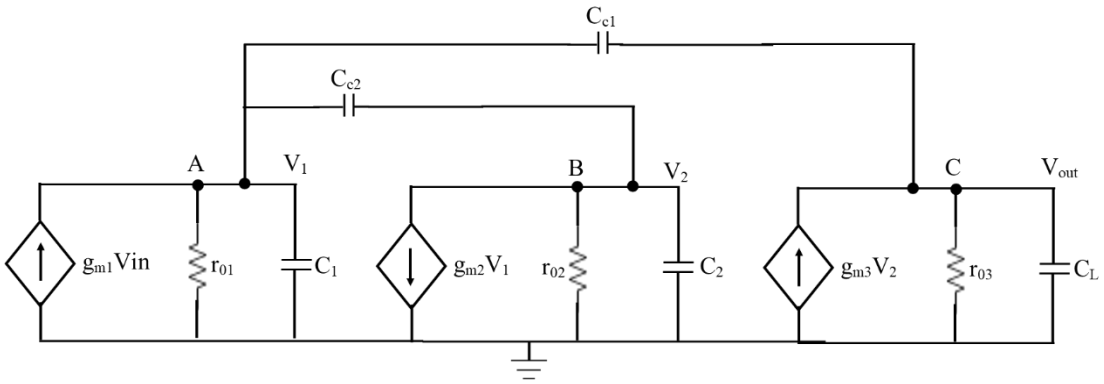


Fig. 2.3 Small signal equivalent circuit of RNMC

The transfer function of RNMC can be obtained by analyzing the small signal equivalent circuit.

To simplify the calculations, following assumptions are made,

$g_{m1}r_{o1}, g_{m2}r_{o2}, g_{m3}r_{o3} >> 1$ (2.1)

$C_L, C_{c1,} C_{c2} >> C_1, C_2$ (2.2)

The following equations are obtained by applying nodal analysis at nodes A, B, and C in Fig. 2.3,

$$g_{m1}V_{in} - V_1(\frac{1}{r_{o1}} + sC_1) - (V_1 - V_2)sC_{c2} - (V_1 - V_{out})\,\mathrm{s}\,C_{c1} = 0 \quad (2.3)$$

$$(V_1 - V_2)sC_{c2} - g_{m2}V_1 - V_2(\frac{1}{r_{o2}} + sC_2) = 0 \quad (2.4)$$

$$g_{m3}V_2 + (V_1 - V_{out})\,\mathrm{s}\,C_{c1} - V_{out}(\frac{1}{r_{o3}} + sC_L) = 0 \quad (2.5)$$

Taking Eqs. 2.3-2.5 into considerations, the transfer function of RNMC is calculated as,

$$A(s) = \frac{A_{dc}}{(1+\frac{s}{\omega_{p1}})} \frac{[1-(\frac{C_{c2}}{g_{m2}}+\frac{C_{c1}}{g_{m2}g_{m3}r_{o2}})s-(\frac{C_{c1}C_{c2}}{g_{m2}g_{m3}})s^2]}{[1+(\frac{C_{c2}C_L}{g_{m3}C_{c1}}+\frac{C_{c2}}{g_{m3}}-\frac{C_{c2}}{g_{m2}})s+\frac{C_{c2}C_L}{g_{m2}g_{m3}}s^2]} \quad (2.6)$$

where A_{dc} is the low frequency gain, and given by, $A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$ (2.7)

According to the denominator of the open loop transfer function (Eq. 2.6), the amplifier contains the dominant pole ω_{p1}, which is defined as,

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{c1}} \quad (2.8)$$

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1}}{C_{c1}} \quad (2.9)$$

Moreover, Eq. 2.6 provides two non-dominant poles and two zeros. Since the coefficients of the s and s^2 terms in the numerator are negative, a right half plane zero is created that is located at a lower frequency than the other left half plane zero. This degrades the stability of the amplifier. Consequently, the right half plane zero should be eliminated.

2.3 Flipped Voltage Follower [67]

The schematic of FVF is shown in Fig. 2.4. It is basically a source follower circuit with shunt feedback, which is very useful in low voltage low power analog design. It consists of PMOS input transistor M9, transistor M10 with shunt feedback, and transistor M11 acting as a current source. FVF has high current sourcing capability and provides low output impedance. The internal feedback loop helps in reducing the output impedance, which helps in shifting the first non-dominant pole away from the origin. It results in improving the GBW.

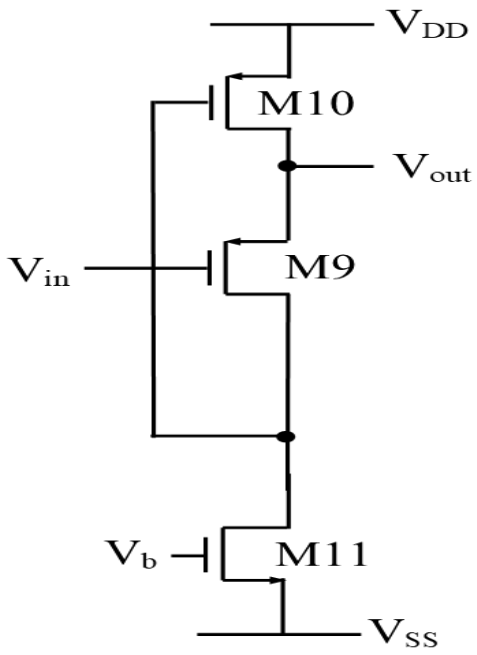


Fig. 2.4 Flipped Voltage Follower

2.4 Class AB Flipped Voltage Follower [68]

Figure 2.5 shows the circuit of class AB FVF. The transistor M9 is the input transistor, which acts as a voltage follower. Transistors M11 and M12 provide large sinking and sourcing currents, respectively, while the transistor M10 is acting as a current source. The resistor R is connected between the gates of the transistors M11 and M12 to adjust the biasing point of the respective transistors. Further, due to this resistor R, a voltage V is developed between the gates of the transistors M11 and M12. The voltage V acts as the battery conventionally utilized in class AB operation. Further, the internal feedback loop reduces the output resistance of class AB FVF, which shifts the first non-dominant pole away from the origin. It leads to an increase in GBW.

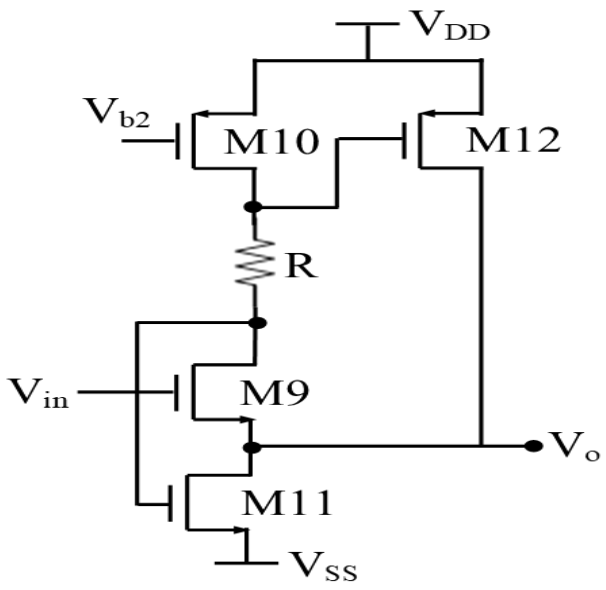


Fig. 2.5 Class AB Flipped Voltage Follower

2.5 Folded Flipped Voltage Follower [67]

The schematic of FFVF is shown in Fig. 2.6. The PMOS version of FFVF consists of PMOS input transistor M9 and NMOS feedback transistor M16. In order to eliminate the voltage clamping issue as in FVF, the feedback transistor is folded. Transistors M10 and M11 are acting as a current source. FFVF has ultra low output impedance and does not suffer from a limited operating voltage range.

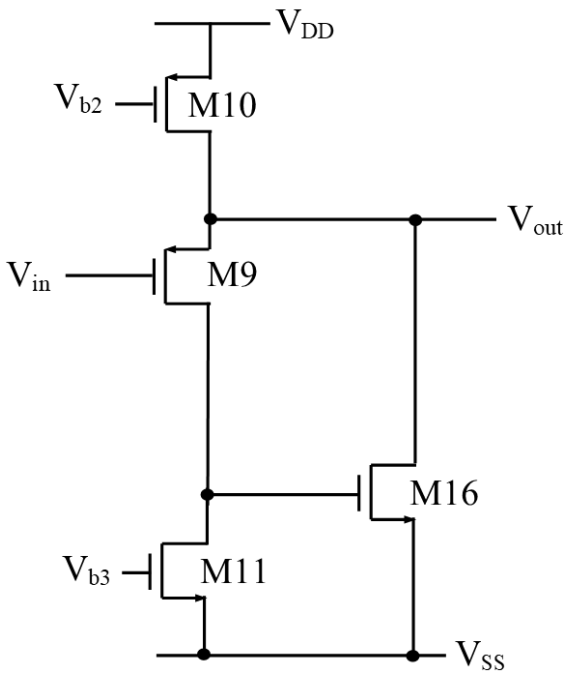


Fig. 2.6 Folded Flipped Voltage Follower

2.6 Push pull class AB output stage [26]

The RNMC structure with the feed forward path in a three-stage amplifier is depicted in Fig. 2.7. The push pull class AB output stage has been realized using the feed forward transconductance stage (g_{mf}). Further, Fig. 2.8 shows the transistor level circuit diagram of a three stage amplifier with RNMC and feed forward path. The feed forward transconductance stage is formed by connecting the output of the first stage to the gate terminal of transistor M14. The push pull class AB output stage enhances the current driving capability of the amplifier, which improves the large signal response.

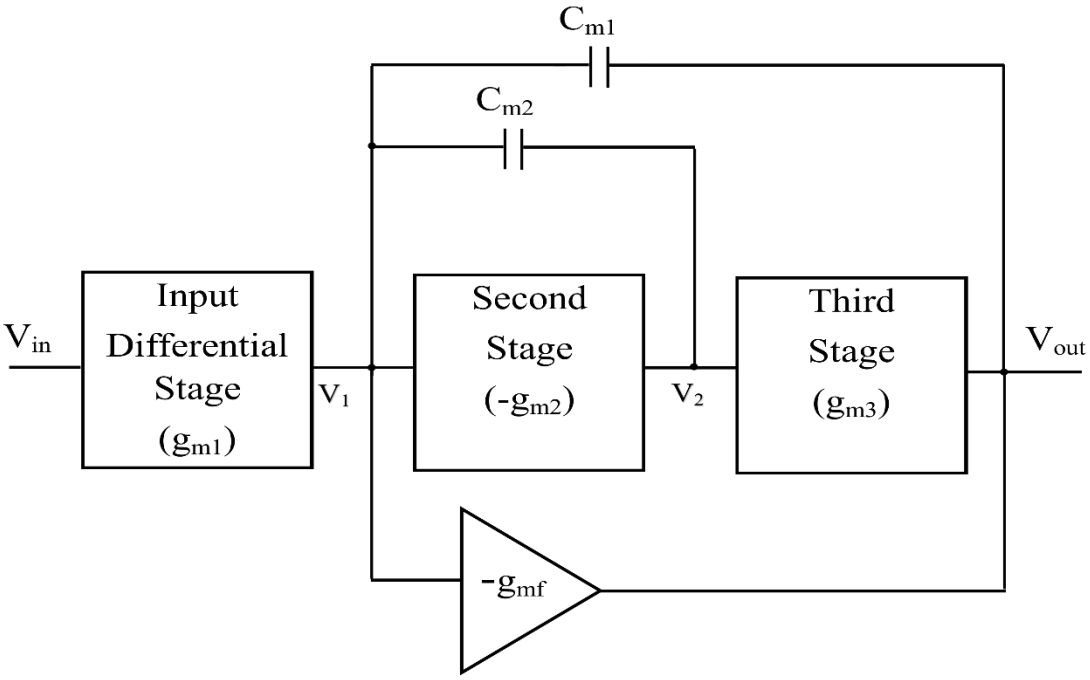


Fig. 2.7 Reversed Nested Miller Compensation with feed forward path

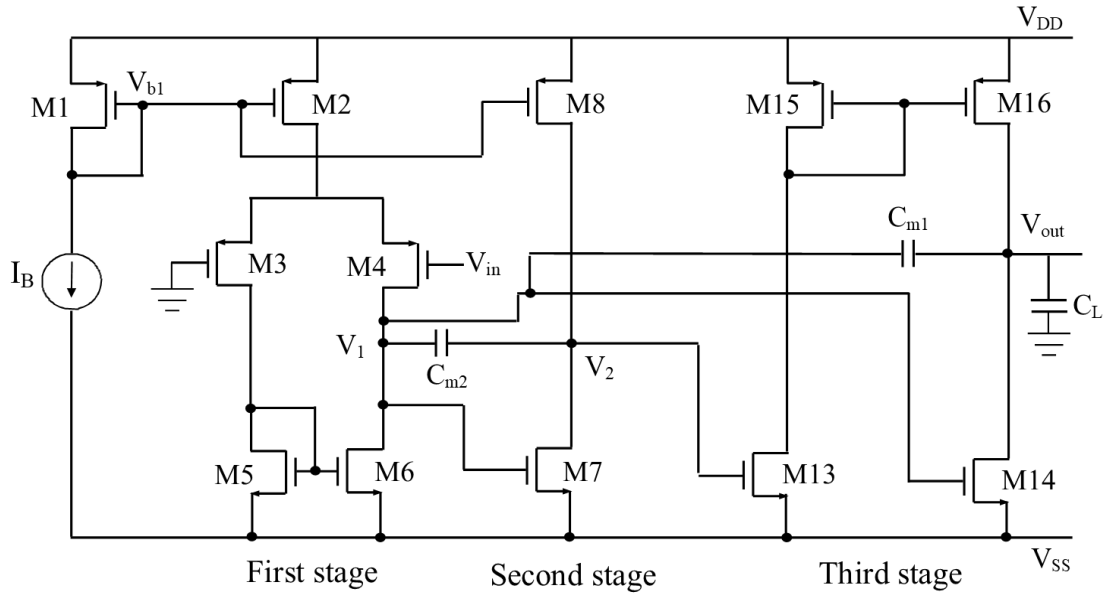


Fig. 2.8 Circuit diagram of Reversed Nested Miller Compensation with feed forward path

2.7 Slew Rate Enhancer Circuit [69]

The schematic of the slew rate enhancer circuit is shown in Fig. 2.9. It increases the slew rate of the amplifier by providing more current to the output node while avoiding an excessively high increase in power consumption. Transistors M18 and M19 form a current comparator that identifies the input voltage transients by observing the output voltage of the first stage and the second stage. As a result, the transistor M20 supplies the additional current. So, the driving capability of the amplifier is enhanced.

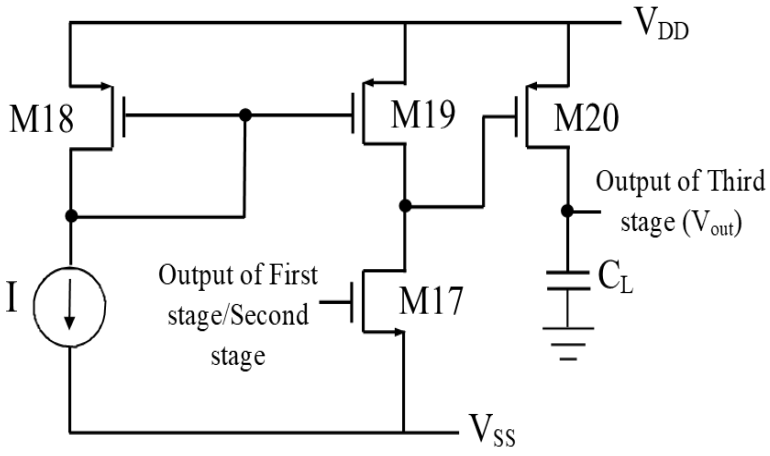


Fig. 2.9 Slew Rate Enhancer Circuit

2.8 Dynamic Threshold Voltage MOSFET (DTMOS) technique [70]

For low voltage low power design, several approaches have been described in the literature. The key objective behind these techniques is to decrease the threshold voltage of the transistor to improve transconductance. One of those methods is bulk driven, in which the input signal is applied at the body terminal rather than the gate terminal. Unfortunately, the transconductance of a bulk driven MOS transistor is substantially smaller, which results in a lower gain bandwidth product. The basic DTMOS structure suggests providing the signal input to both the body and the gate terminal. This approach enhances the transconductance of transistor, which improves the GBW. The schematic of the DTMOS (M1) transistor is shown in Fig. 2.10.

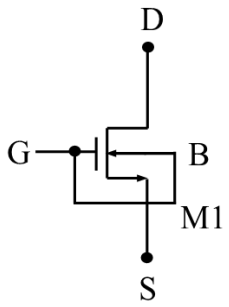


Fig. 2.10 DTMOS

2.9 Self Cascode Structure [71]

Figure 2.11 displays the self cascode structure. It comprises, two transistors M1 and M2. For optimal operation, transistor M1 always operates in the saturation region, while transistor M2 operates in the linear region. Further, the aspect ratio (W/L) of transistor M1 should be N times larger than transistor M2, which helps in increasing the output resistance R_{out} of the self cascode structure. Eq. 2.10 shows the relation of R_{out} with the factor N, where r_{o1} is the output resistance of transistor M1.

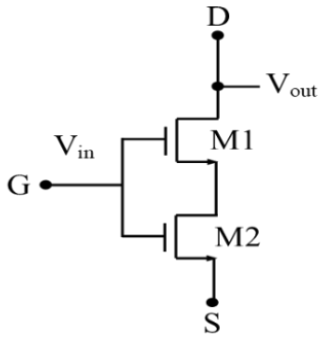


Fig. 2.11 Self cascode structure

$$Rout = (N+1)ro1 \quad (2.10)$$

2.10 Self Cascode Structure with Dynamic Threshold Voltage MOSFET technique [72]

Various conventional and non-conventional techniques have been proposed for low voltage low power design in the literature. The self cascode structure and DTMOS are two of the low voltage low power techniques. Both the techniques can be combined to enhance the transconductance of

the transistor. It results in enhancing the GBW of the amplifier. Fig. 2.12 depicts the self cascode structure with DTMOS. Transistors M1 and M2 construct the self cascode structure. The upper transistor M1 is a DTMOS transistor.

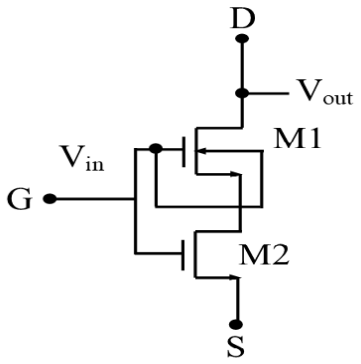


Fig. 2.12 Self Cascode Structure with DTMOS

2.11 Modified Self Cascode Structure

The modified self cascode structure is displayed in Fig. 2.13. Here, the self cascode transistors M1-M2 are placed in parallel with transistor M5 to achieve higher transconductance. For optimal operation, transistor M1 always works in the saturation region while transistor M2 functions in the linear region. This arrangement enhances the GBW of the amplifier. Additionally, because of the very low voltage that exists between source and drain terminal of transistors M2, this structure can be utilized in low voltage applications.

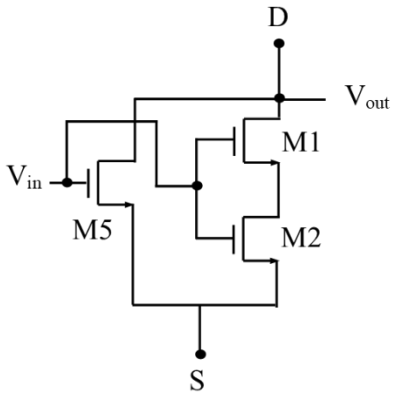


Fig. 2.13 Modified self cascode structure

2.12 Active LHP Zero Circuit [34]

This circuit is highly helpful for eliminating a parasitic pole of any particular stage. This technique has been used at the second stage of the amplifier. Active LHP zero circuit only serves as the second stage's load and does not short out the last stage, therefore, no additional power is consumed. Figure 2.14 shows the structure of an active LHP zero circuit, which comprises transistors M8 and M9 along with a resistor R_z and capacitor C_z. Further, the active LHP zero block provides one active zero Z_1 and two poles P_1 and P_2, which are evident from Eqs. 2.11-2.13. The active LHP zero Z_1 cancels the parasitic pole P_{b2} (Eq. 2.14) of the second stage, which helps in improving GBW.

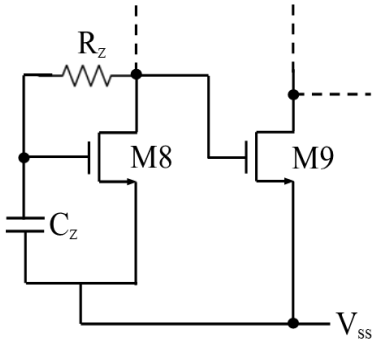


Fig. 2.14 Active LHP Zero Circuit

$$Z_1 = \frac{1}{RzCz} \tag{2.11}$$

$$P_1 = \frac{g_{ma}}{Cz} \tag{2.12}$$

$$P_2 = \frac{g_{ma}}{RzC_{pa}} \tag{2.13}$$

$$P_{b2} = \frac{g_{m2}}{C_2} \tag{2.14}$$

The transconductance and parasitic capacitance of the active LHP block are g_{ma} and C_{pa}, respectively, whereas g_{m2} denotes the transconductance of the second stage.

2.13 Summary

In this chapter, various techniques have been discussed to improve the performance of three stage amplifiers. One of the conventional frequency compensation techniques, RNMC, has the advantage of better GBW, but it has the RHP zero problem. Moreover, FVF, class AB FVF, and folded FVF are utilized to address the RHP zero problem. Further, the frequency response of the amplifier is enhanced using these techniques. The push pull class AB output stage and slew rate enhancer circuit make the slew rate of the amplifier better. DTMOS and self-cascode structure enhance the GBW of the amplifier. Additionally, the GBW is improved with the help of self-cascode with DTMOS and modified self-cascode structure. The active LHP zero circuit increases the GBW by cancelling the parasitic pole of the amplifier.

Chapter 3

Reversed Nested Miller Compensation with Flipped Voltage Follower

The contents of this chapter are published in:

[1] Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, **"Improved reversed nested Miller frequency compensation techniques using flipped and folded flipped voltage follower with resistor for three stage amplifier"**, AEU-International Journal of Electronics and Communications, vol. 142, pp. 1-14, 2021. **(SCI-Expanded)**

3.1 Introduction

This chapter presents Flipped Voltage Follower (FVF) in inner feedback loop of RNMC for frequency compensation. The FVF breaks the forward path and resolve the RHP zero problem. The input stage of the proposed amplifier 1 is the differential amplifier, while the second stage is common source amplifier. The non-inverting amplifier constitute the third stage. To enhance the transient response, an additional feed forward stage has been used to realize the push pull output stage.

The organization of this chapter is as follows: Section 3.2 gives the circuit description and small signal analysis of the proposed amplifier 1. To verify the functionality of the amplifier, simulation results are also given in Section 3.2. Moreover, process corner analysis has been done to examine the robustness of the amplifier over process variations. Further, the effect of supply voltage variations on the proposed amplifier 1 is studied, and observations are comprehended in Section 3.2. Additionally, Monte Carlo analysis has been done and included in Section 3.2. The performance of the proposed amplifier 1 is compared with its existing counterparts in Section 3.3. The chapter is summarized in Section 3.4.

3.2 Proposed amplifier 1

The block diagram of proposed amplifier 1 is shown in Fig. 3.1. It can be seen from Fig. 3.1 that the three gain stages are connected in series, and the input of the FVF has been connected to the output of the second stage to break the forward path. Since the Miller loop should exhibit a negative gain, therefore the second stage is the inverting amplifier in order to create favorable condition for Miller's effect. A non-inverting amplifier constitutes the third stage. Further, an additional feed forward stage has been used to realize the push pull output stage.

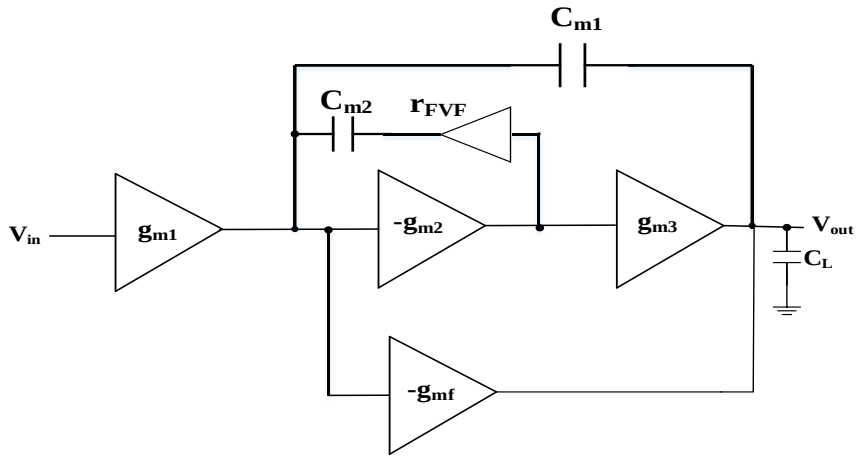


Fig. 3.1 Block diagram of proposed amplifier 1

3.2.1 Circuit description of proposed amplifier 1

The transistor level implementation of the proposed amplifier 1 is given in Fig. 3.2. Transistors M1-M4 and M6 form the differential amplifier for the first stage. Transistors M7-M8 form the second stage, which is a common source amplifier; followed by a non-inverting stage which constitutes the third stage (M12-M15). Transistors M9-M11 form the FVF circuit. Apart from this, two Miller capacitors, C_{m1} and C_{m2}, are connected in the feedback loop. The compensation capacitor C_{m2} is independent of the output node, so it helps in increasing the GBW. Compensation capacitor C_{m1} is connected between the output of third stage and the first stage, while C_{m2} is connected between the output of the FVF and the first stage. It can be seen that transistor M13 is connected to the output of the differential stage, thus implementing the push pull output stage with improved slew rate performance. However, it only affects the large signal performance and does not alter the small-signal open-loop transfer function.

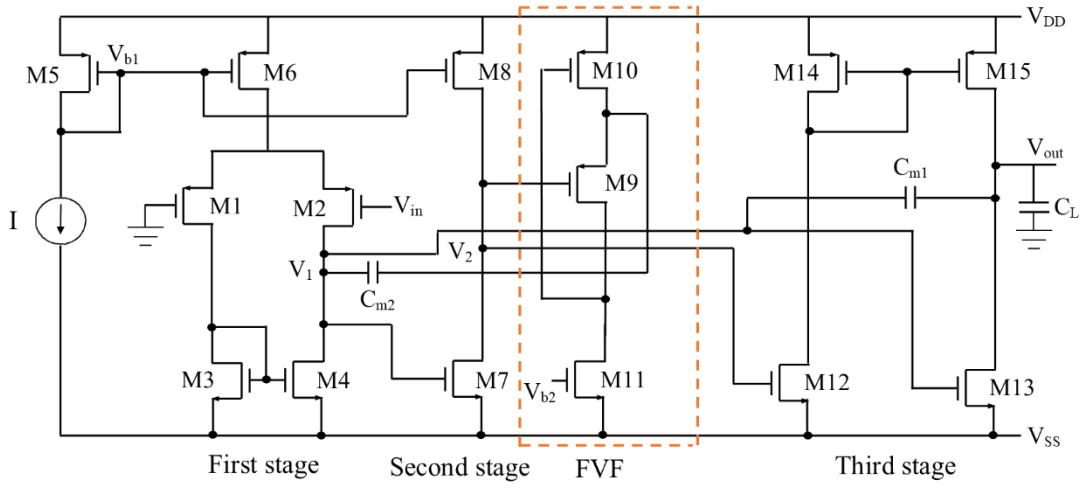


Fig. 3.2 Transistor level implementation of proposed amplifier 1

3.2.2 Small signal analysis of proposed amplifier 1

The transfer function of the proposed amplifier 1 can be obtained by analyzing the small signal equivalent circuit of the proposed amplifier 1 of Fig. 3.2, as shown in Fig. 3.3.

To simplify the calculations, following assumptions are made,

$$g_{m1}r_{o1},\ g_{m2}r_{o2},\ g_{m3}r_{o3} >> 1 \tag{3.1}$$

$$C_L,\ C_{m1},\ C_{m2} >> C_1,\ C_2 \tag{3.2}$$

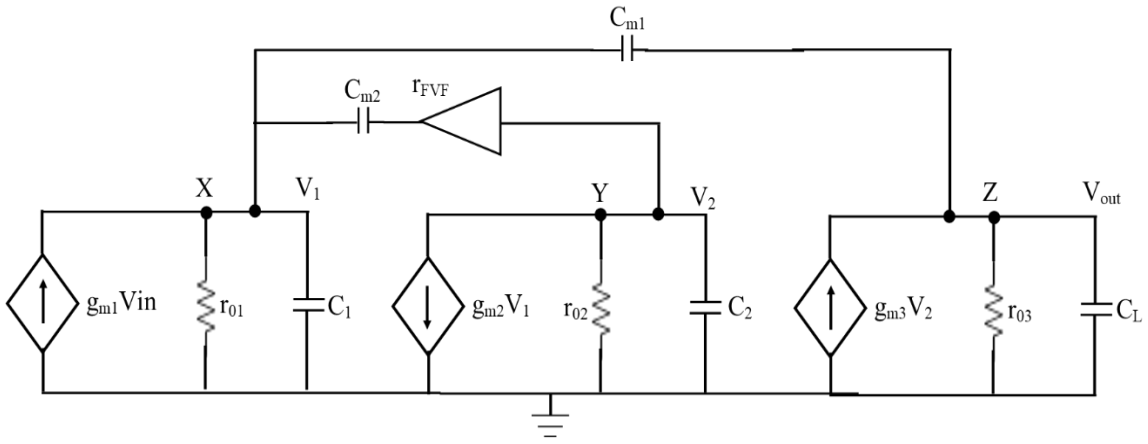


Fig. 3.3 Small signal model of proposed amplifier 1

The small signal transfer function of the proposed amplifier 1 can be obtained by a third order expression, which is given by,

$$A(s) = \frac{A_{dc}}{(1+\frac{s}{\omega_{p1}})} \frac{[1+(r_{FVF}C_{m2} - \frac{C_{m1}}{g_{m2}g_{m3}r_{FVF}})s - (\frac{C_{m1}C_{m2}r_{FVF}}{g_{m2}g_{m3}r_{o2}})s^2]}{[1+\frac{C_{m2}(C_L+C_{m1}+g_{m3}r_{FVF}C_{m1})}{g_{m3}C_{m1}}s + \frac{r_{FVF}C_{m2}C_L}{g_{m2}g_{m3}r_{o2}}s^2]} \quad (3.3)$$

where A_{dc} is the low frequency gain and given by, $A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$ (3.4)

The input stage has output resistance r_{o1}, output capacitance C_1, and transconductance g_{m1}. The second stage has output resistance and output capacitance of r_{o2} and C_2, respectively with transconductance g_{m2}. The final stage possesses output resistance r_{o3}, transconductance g_{m3}, and total equivalent load capacitance C_L. The output resistance of FVF is r_{FVF}.

According to the denominator of the open loop transfer function (Eq. 3.3), the amplifier contains the dominant pole ω_{p1} and non-dominant poles ω_{p2} and ω_{p3}, which are defined as,

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}} \quad (3.5)$$

$$\text{First non-dominant pole, } \omega_{p2} = \frac{g_{m3}C_{m1}}{C_{m2}(C_L+C_{m1}+g_{m3}r_{FVF}C_{m1})} \quad (3.6)$$

$$\text{Second non-dominant pole, } \omega_{p3} = \frac{g_{m2}r_{o2}(C_L+C_{m1}+g_{m3}r_{FVF}C_{m1})}{C_{m1}C_Lr_{FVF}} \quad (3.7)$$

Further, from the numerator of the open loop transfer function (Eq. 3.3), it can be seen that there are one LHP zero and a RHP zero, which are given by,

$$\text{LHP zero, } \omega_{z1} = \frac{g_{m2}g_{m3}r_{FVF}}{g_{m2}g_{m3}r^2_{FVF}C_{m2} - C_{m1}} \quad (3.8)$$

$$\text{RHP zero, } \omega_{z2} = -\frac{g_{m2}r_{o2}g_{m3}r^2_{FVF}C_{m2} - r_{o2}C_{m1}}{C_{m1}C_{m2}r^2_{FVF}} \quad (3.9)$$

The value of the GBW can be obtained by multiplying dc gain A_{dc} with dominant pole frequency ω_{p1}, i.e.

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1}}{C_{m1}} \quad (3.10)$$

It is evident from Eqs. 3.5-3.7, that the proposed amplifier 1 has no RHP pole. So, it is unconditionally stable. From Eq. 3.9, it can be observed that the RHP zero ω_{z2} is now shifted to a very high frequency since it is multiplied with the second stage gain $g_{m2}r_{o2}$. Therefore, this RHP zero will not upset the phase margin, which leads to higher stability of the circuit. Though, the system is more stable for larger phase margins, the time response of such system slows down. A phase margin of 60° is typically considered as the optimum value [2].

Stability Analysis

Phase margin (PM) can be calculated as [2],

$$PM=180°+\angle\beta H\ (\omega = \omega_{GBW)} \quad (3.11)$$

where ω_{GBW} denotes the gain-bandwidth product, which is also called unity gain frequency, and βH is the loop gain.

A measure of stability is given by the value of the phase when gain is unity i.e. 0 dB. In order to ensure the stability of the circuit, the PM should be positive. From the small signal analysis of the proposed amplifiers 1, it is clear that it has no RHP pole. Also RHP zero is at very high frequency. Thus, the proposed amplifier exhibits sufficient phase margin, which leads to higher stability of the circuit.

3.2.3 Simulation results and discussions

The functionality of the proposed amplifier 1 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 1 is enlisted in Table 3.1.

Table 3.1 Design parameters of proposed amplifier 1

Parameters	**Value**
Transistor dimensions	M1, M2: W=100 µm, L=0.35 µm; M3, M4, M7: W=60 µm, L=0.35 µm M5, M6, M14, M15: W=20 µm, L=1 µm; M8: W=10 µm, L= 1 µm; M9, M10: W=15 µm, L= 1 µm; M11: W=35 µm, L= 1 µm; M12: W=12 µm, L= 0.35 µm; M13: W=150 µm, L= 0.35 µm;
C_{m1}, C_{m2}	12.5 pF, 2.2 pF
Biasing current (I)	10 µA
C_L	100 pF

The frequency response of the proposed amplifier 1 is displayed in Fig. 3.4. Proper selection of element values leads to a maximally flat magnitude response with a significant improvement in the bandwidth of the amplifier. From the frequency response, it can be seen that the GBW of the proposed amplifier 1 is 20 MHz. Further, the phase margin is 64°, which ensures good stability of the amplifier. Also, it has a DC gain of more than 100 dB. Figure 3.5 shows the transient response in unity gain configuration. The slew rate of the proposed amplifier 1 is 10 V/µS, and 1 % settling time is 0.1 µs. Figure 3.6 shows the frequency response of CMRR. The CMRR is found to be 86 dB. Further, Fig. 3.7 displays the PSRR of the proposed amplifier 1. It is observed to be 78 dB.

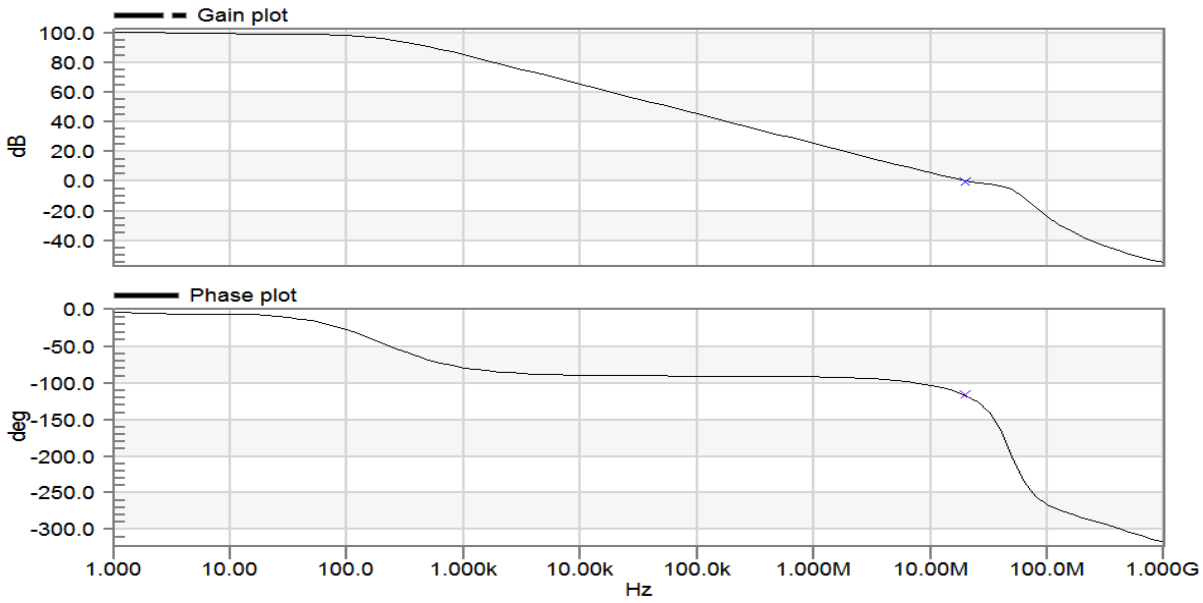


Fig. 3.4 Frequency response of proposed amplifier 1

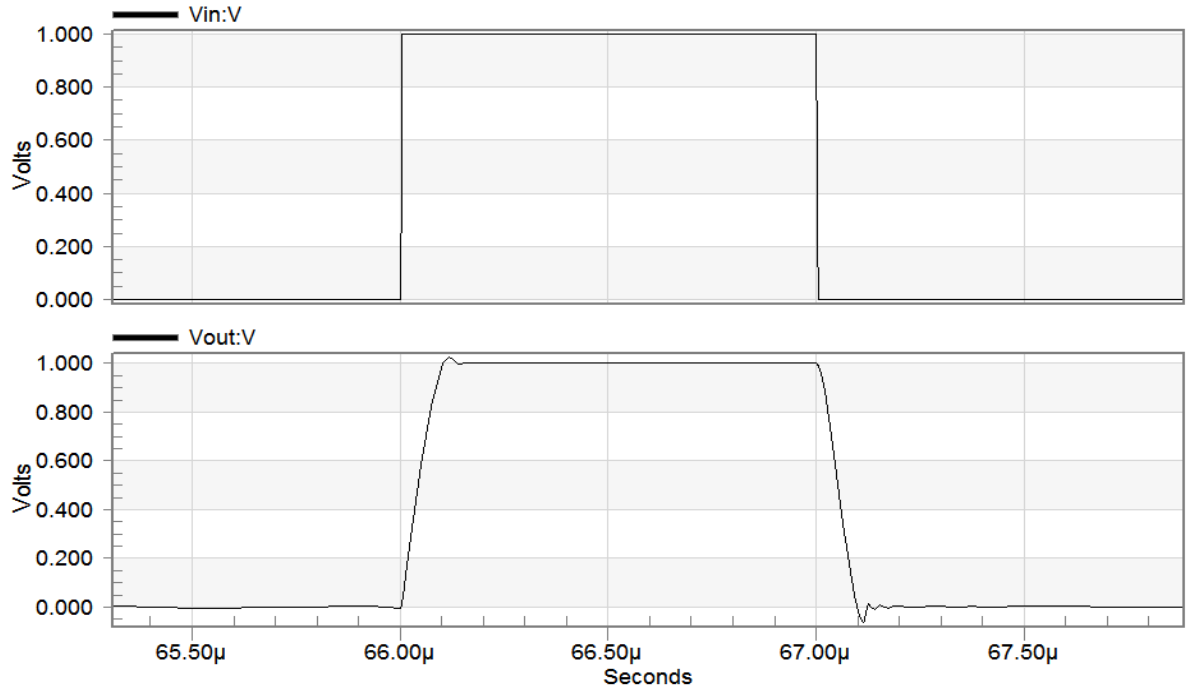


Fig. 3.5 Transient response of proposed amplifier 1

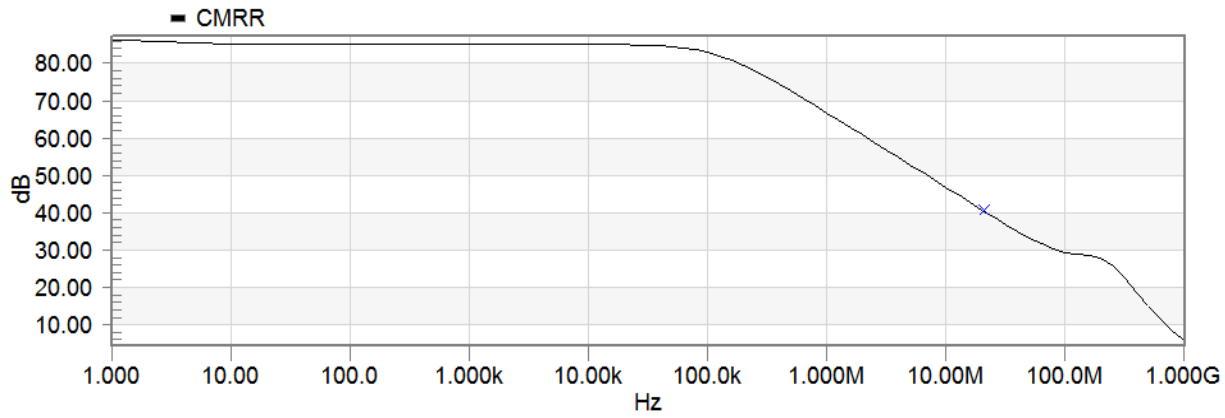


Fig. 3.6 Frequency response of CMRR of proposed amplifier 1

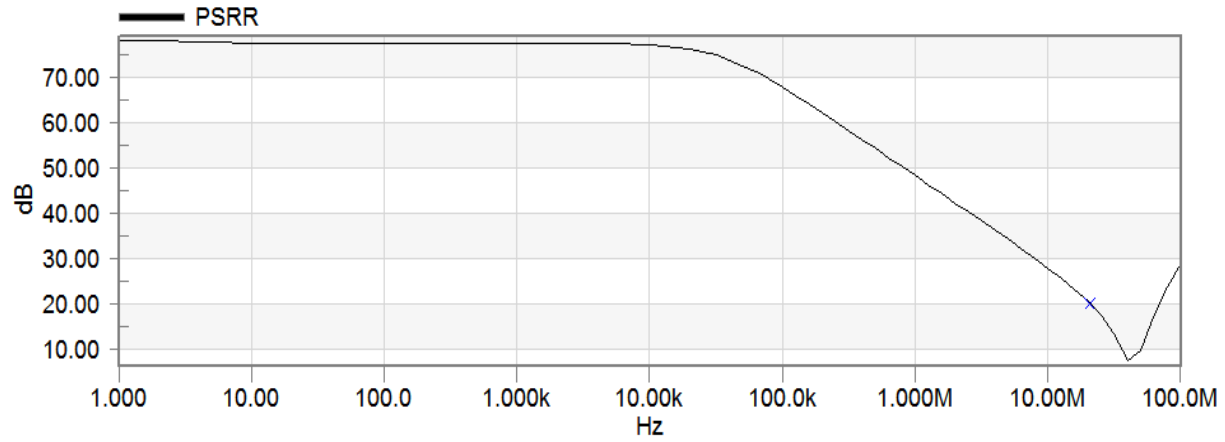


Fig. 3.7 Frequency response of PSRR of proposed amplifier 1

Process corner analysis (Fig. 3.8) has been done to prove the robustness of the proposed amplifier 1 over process variations that statistically occur during wafer production. Different process corners are Typical NMOS Typical PMOS (TT), Slow NMOS Fast PMOS (SF), Fast NMOS Slow PMOS (FS), Slow NMOS Slow PMOS (SS), Fast NMOS Fast PMOS (FF). These corners are based on the carrier mobility, threshold voltage etc. of NMOS and PMOS. Table 3.2 shows the variation of gain, GBW and PM for various process corners. It can be seen that the maximum variations in (Gain, GBW, PM) with respect to TT process corner are within 20%.

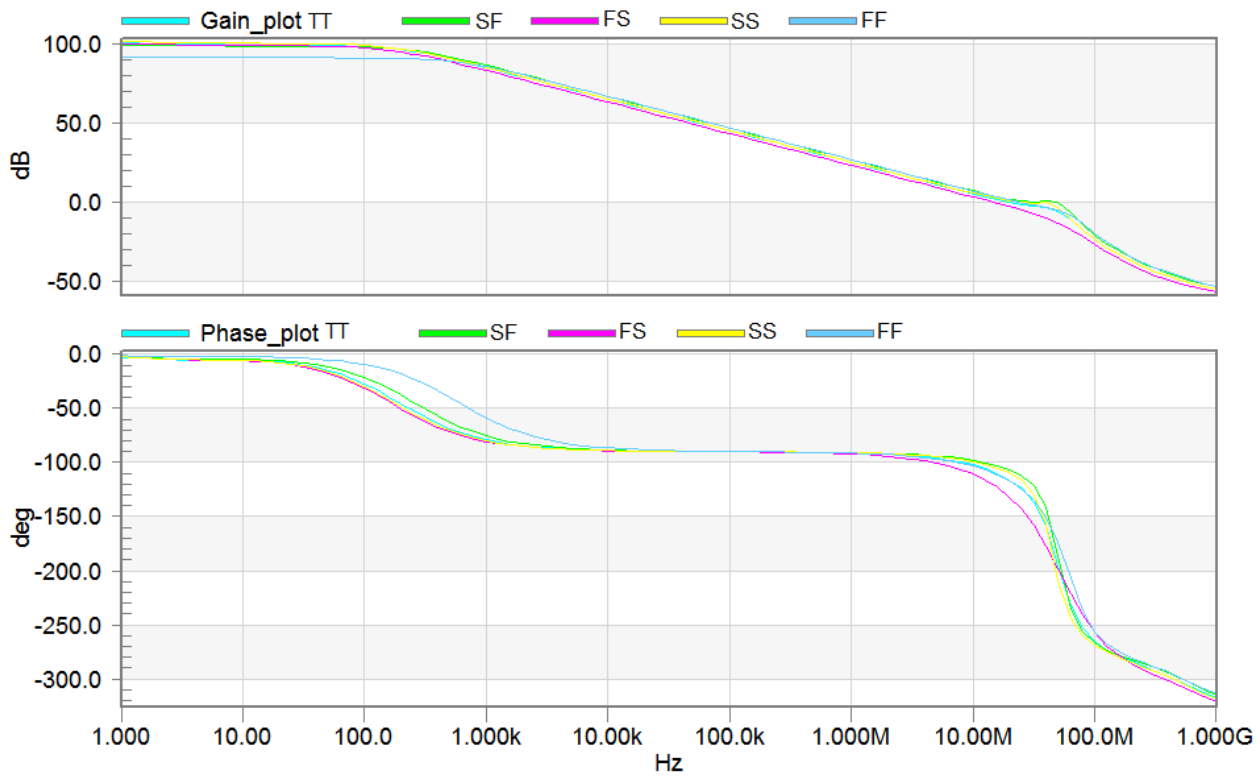


Fig. 3.8 Frequency response of proposed amplifier 1 at different process corners

Further, the supply voltage variation of ±5% is considered, and the observe frequency response of the proposed amplifier 1 is shown in Fig. 3.9. The corresponding results are placed in Table 3.2. It has been noted that the maximum variations in (Gain, GBW, PM) for proposed amplifier 1 is (0.99%, 14%, 12.3%). Thus, the maximum variation with respect to the supply voltage is 14%.

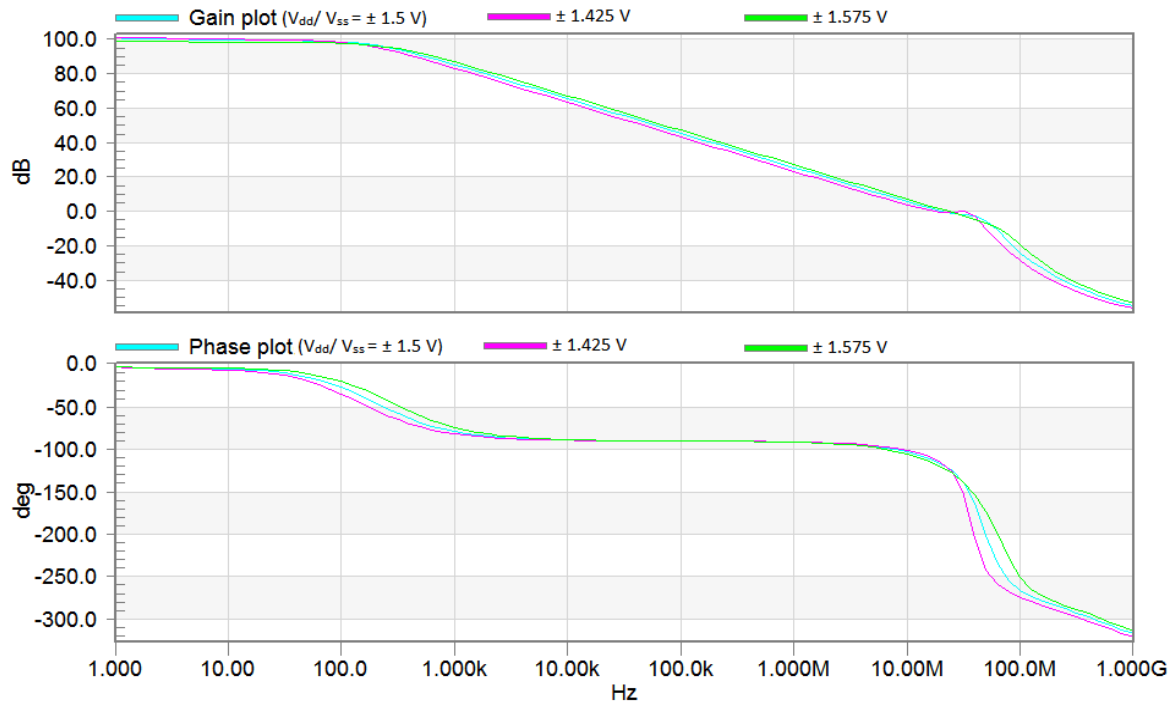


Fig. 3.9 Frequency response of proposed amplifier 1 with variations in supply voltage

Table 3.2 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 1

(viii) Performance parameter	Corner					Supply Voltage variation (1.5V ± 5% of 1.5V)	
	TT	SF	FS	SS	FF	1.425V	1.575V
Gain (dB)	101	101	100	102	93.6	101.3	100
GBW (MHz)	20	22.3	16	21.6	23.3	21.1	22.8
PM (°)	65	69	60	68	60	62	57

Further, Monte-Carlo simulations (100 runs) are carried out for 5% Gaussian distribution of power supply. The corresponding gain and phase plots are shown in Fig. 3.10. The (mean, standard deviation) in gain for proposed amplifier 1 is (100.25 dB, 3.75 dB).

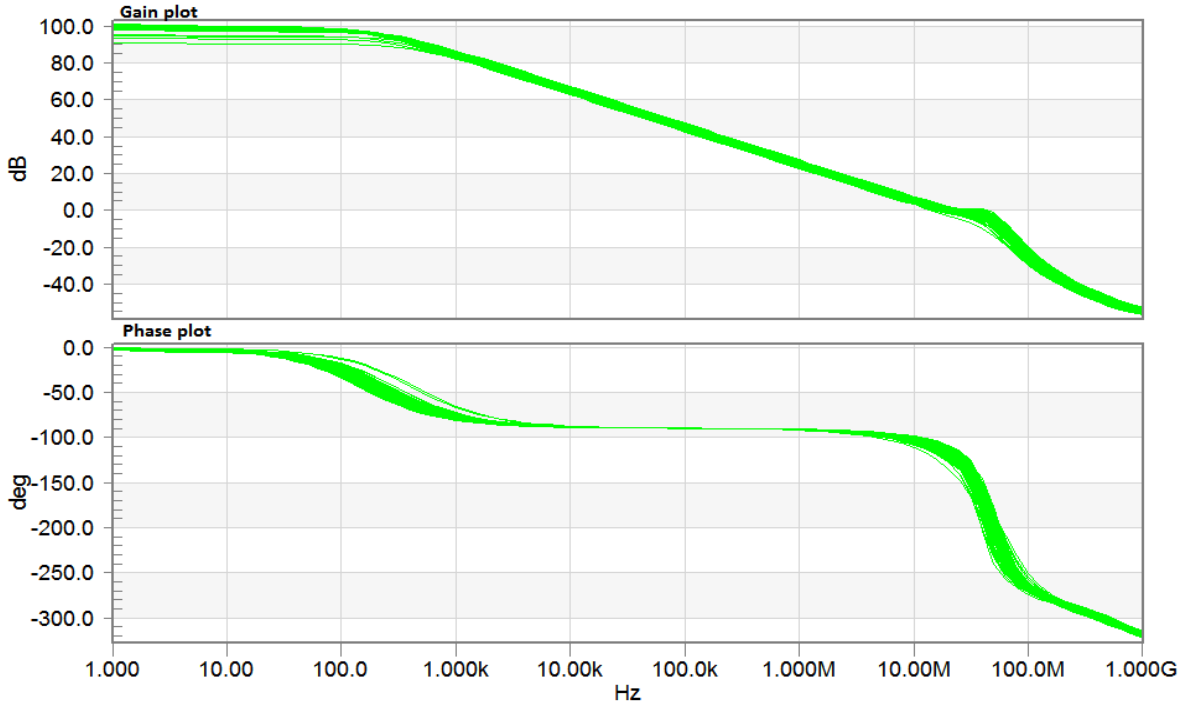


Fig. 3.10 Monte-Carlo analysis for frequency response of the proposed amplifier 1 against supply voltage variations

3.3 Comparison

Table 3.3 compares the proposed amplifier 1 with other amplifiers at 100 pF load. It is evident that the proposed amplifier 1 offers better GBW with phase margin more than 60°. Further, the slew rate of the proposed amplifier 1 is superior to its counterparts. Few of the figure of merits are found to be good. FOM_L of the proposed amplifier 1 is comparable to Refs. [28-29] and [31], while $IFOM_L$ is higher than Refs. [28-29] and [31].

Table 3.3: Performance comparison of proposed amplifier 1 with its counterparts

Parameters	**[28]**	**[29]**	**[30]**	**[31]**	**Proposed amplifier 1**
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Supply (V)	1.8	1.8	1.8	1.8	1.5
C_L (pF)	100	100	100	100	100
GBW (MHz)	4.75	14	9.63	9.08	20
PM (°)	63.3	86	85	83	64
DC Gain (dB)	110	112	115	110	101
Power (mW)	0.32	0.28	0.31	0.54	3.8
SR (V/µS)	1.2	0.8	7.01	2.23	10
FOM_L (V^{-1})	0.38	0.35	2.26	0.41	0.26
$IFOM_L$	0.7	0.61	5.18	0.73	0.8
FOM_S (Hz.F/W)	1.51	6	3.11	1.65	0.51
$IFOM_S$ (Hz.F/A)	2.72	10.76	5.6	2.97	1.52

3.4 Summary

In this chapter, a frequency compensated three stage amplifier is proposed. The proposed amplifier 1 utilizes RNMC with FVF to enhance the GBW and phase margin of the amplifier. Additionally, the push pull output stage enhances the transient response. Moreover, the transfer function of the proposed amplifier 1 is determined with the help of small signal analysis. The transfer function provides the poles and zeros, which helps in evaluating the DC gain, stability, and GBW of the amplifier. The proposed amplifier 1 offers the GBW of 20 MHz, which is better than its counterparts. The phase margin is 64°, which indicates the good stability of the amplifier. Further, the DC gain is more than 100 dB. The slew rate of the proposed amplifier 1 is 10 V/µs, and it is better than other amplifiers. Further, the effectiveness of the proposed amplifier 1 is verified with the help of various simulations, including corner analysis, supply voltage variation, and Monte Carlo analysis.

Chapter 4

Reversed Nested Miller Compensation with Folded Flipped Voltage Follower, Self Cascode structure and DTMOS

The contents of this chapter are published in:

[1] Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, **"Improved reversed nested Miller frequency compensation techniques using flipped and folded flipped voltage follower with resistor for three stage amplifier"**, AEU-International Journal of Electronics and Communications, vol. 142, pp. 1-14, 2021. **(SCI-Expanded)**

[2] Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, **"Refining RNMC compensation for Three Stage Amplifier using DTMOS Transistor and FFVF"**, 14th International Conference on Computing, Communication and Networking Technologies (ICCCNT), July 2023.

[3] Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, **"Enhancing Reversed Nested Miller Compensation of Three Stage Amplifier using Self Cascode and Folded Flipped Voltage Follower"**, Fifth International Conference on Advances in Electronics, Computers and Communications (ICAECC), Sep 2023.

4.1 Introduction

In chapter 3, FVF is introduced with RNMC to address the RHP zero problem. This chapter explores the impact of introducing Folded Flipped Voltage Follower (FFVF) in the inner compensation loop of RNMC to resolve the RHP zero problem. Four variants are presented are presented and are called proposed amplifiers 2-5. Further, the proposed amplifiers 3, 4, and 5 also utilize a resistor in the outer compensation loop of RNMC for double pole-zero cancellation. The input stage of the proposed amplifiers 2 and 3 is same whereas the proposed amplifier 4 uses the self cascode structure. The proposed amplifier 5 makes use of DTMOS transistor in the input stage to improve the GBW of the amplifiers. Moreover, the feed forward path is exploited in all amplifiers to improve the transient response.

The organization of this chapter is as follows: Section 4.2 gives the circuit description, small signal analysis, and simulation results of the proposed amplifier 2. Section 4.3 describes the proposed amplifier 3. Moreover, the small signal analysis, and simulation results of the proposed amplifier 3 are also included in Section 4.3. Further, the description of the proposed amplifiers 4 and 5 is given in Sections 4.4 and 4.5, respectively. Additionally, Sections 4.4 and 4.5 comprise the small signal analysis and simulation results of the proposed amplifiers 4 and 5, respectively. Process corner analysis of all proposed amplifiers has been done to ascertain the robustness of the circuits over process variations, and results are compiled in the respective sections. Further, the effect of supply voltage variations on the performance of proposed amplifiers is studied, and observations are comprehended in the respective sections. Moreover, Monte Carlo analysis has been done for all amplifiers and results are included in the respective sections. The performance of the proposed amplifiers in this chapter are compared with their existing counterparts in Section 4.6. Further, Section 4.7 includes the summary of the findings.

4.2 Proposed amplifier 2

The block diagram of proposed amplifier 2 is shown in Fig. 4.1. It can be seen from Fig. 4.1 that FFVF has been introduced in the inner loop to address the RHP zero problem. By using FFVF in the inner loop, the output swing is completely preserved. Also, the proposed amplifier 2 utilizes the advantage of FFVF i.e. ultra low output impedance. It can be seen from Fig. 4.1 that the three gain stages are connected in series and input of FFVF has been connected to the output of the second stage to break the forward path. Second stage is the inverting amplifier in order to create

favorable condition for Miller's effect. A non-inverting amplifier constitutes the third stage. Further, an additional feed forward stage has been used to realize push pull output stage.

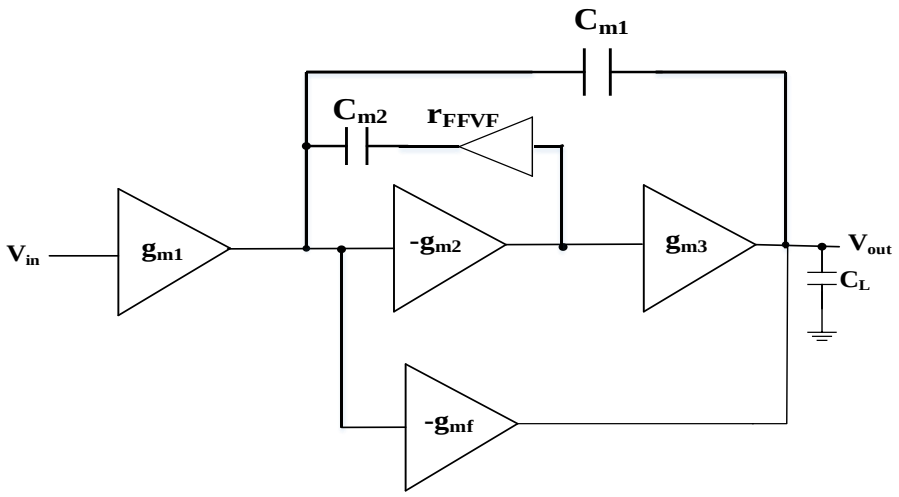


Fig. 4.1 Block diagram of proposed amplifier 2

4.2.1 Circuit description of proposed amplifier 2

Figure 4.2 shows the circuit diagram of the proposed amplifier 2. Transistors M1-M4 and M6 form the differential amplifier for the first stage. Transistors M7-M8 form the second stage, which is a common source amplifier; followed by a non-inverting stage, which constitutes the third stage (M12-M15). Transistors M9-M11 and M16 form the FFVF circuit. Apart from this, two Miller capacitors, C_{m1} and C_{m2}, are connected in the feedback loop. The compensation capacitor C_{m2} is independent of the output node, so it helps in increasing the GBW. The compensation capacitor C_{m1} is connected between the output of third stage and the first stage, while C_{m2} is connected between the output of FFVF and the first stage. It can be seen that transistor M13 is connected to the output of differential stage thus implementing a push pull output stage with improved slew rate performance.

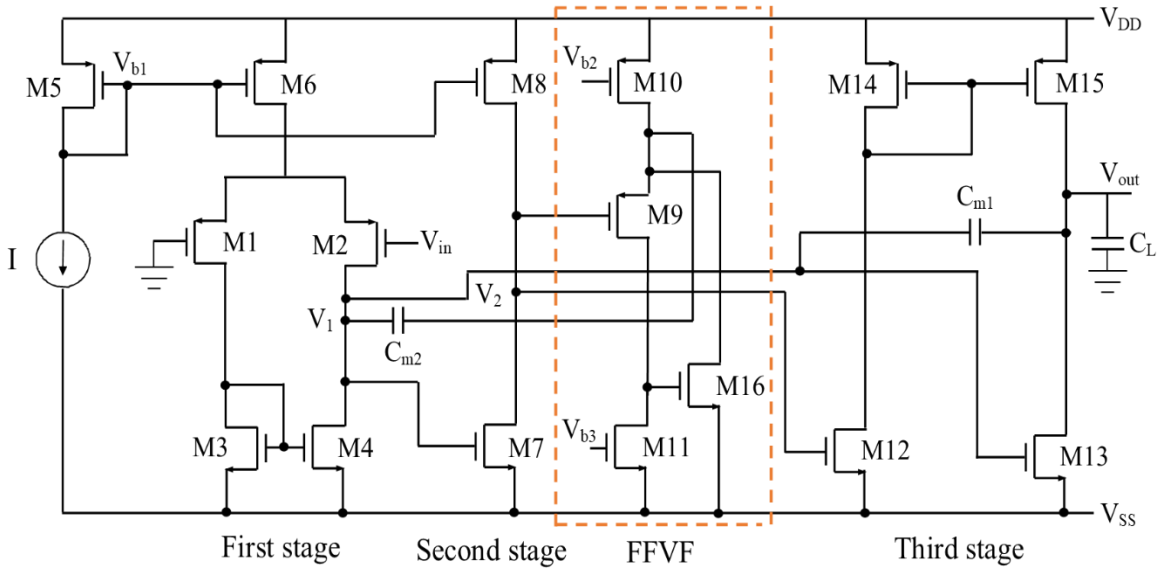


Fig. 4.2 Transistor level implementation of proposed amplifier 2

4.2.2 Small signal analysis of proposed amplifier 2

The transfer function of the proposed amplifier 2 can be obtained by analyzing the small signal equivalent circuit of the amplifier, as shown in Fig. 4.3.

To simplify the calculations, following assumptions are made,

$$g_{m1}r_{o1},\ g_{m2}r_{o2},\ g_{m3}r_{o3} >> 1 \tag{4.1}$$

$$C_L,\ C_{m1},\ C_{m2} >> C_1,\ C_2 \tag{4.2}$$

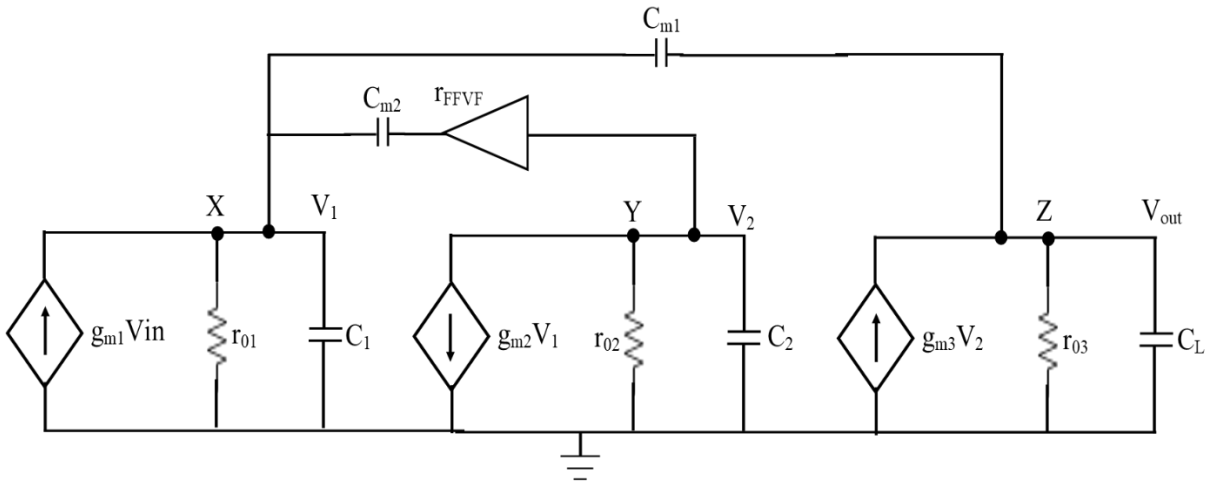


Fig. 4.3 Small signal model of proposed amplifier 2

The small signal transfer function of the proposed amplifier 2 can be obtained by a third order expression, which is given by,

$$A(s) = \frac{A_{dc}}{\left(1+\frac{s}{\omega_{p1}}\right)} \frac{\left[1+\left(r_{FFVF}C_{m2}-\frac{C_{m1}}{g_{m2}g_{m3}r_{FFVF}}\right)s-\left(\frac{C_{m1}C_{m2}r_{FFVF}}{g_{m2}g_{m3}r_{o2}}\right)s^2\right]}{\left[1+\frac{C_{m2}(C_L+C_{m1}+g_{m3}r_{FFVF}C_{m1})}{g_{m3}C_{m1}}s+\left(\frac{C_LC_{m2}r_{FFVF}}{g_{m2}g_{m3}r_{o2}}\right)s^2\right]} \quad (4.3)$$

The input stage has output resistance r_{o1}, output capacitance C_1, and transconductance g_{m1}. The second stage has output resistance and output capacitance of r_{o2} and C_2, respectively with transconductance g_{m2}. The final stage possesses output resistance r_{o3}, transconductance g_{m3}, and total equivalent load capacitance C_L. The output resistance of FFVF is r_{FFVF}.

According to the denominator of the open loop transfer function (Eq. 4.3), the amplifier contains the dominant pole ω_{p1} and non-dominant poles ω_{p2} and ω_{p3} which are defined as,

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}} \quad (4.4)$$

$$\text{First non-dominant pole, } \omega_{p2} = \frac{g_{m3}C_{m1}}{C_{m2}(C_L + C_{m1} + g_{m3}r_{FFVF}C_{m1})} \quad (4.5)$$

$$\text{Second non-dominant pole, } \omega_{p3} = \frac{g_{m2}r_{o2}(C_L + C_{m1} + g_{m3}r_{FFVF}C_{m1})}{C_{m1}C_Lr_{FFVF}} \quad (4.6)$$

Further from numerator of open loop transfer function (Eq. 4.3), it can be seen that the amplifier contains one LHP zero and a RHP zero which are given by,

$$\text{LHP zero, } \omega_{z1} = \frac{g_{m2}g_{m3}r_{FFVF}}{g_{m2}g_{m3}r^2_{FFVF}C_{m2} - C_{m1}} \quad (4.7)$$

$$\text{RHP zero, } \omega_{z2} = -\frac{g_{m2}r_{o2}g_{m3}r^2_{FFVF}C_{m2} - r_{o2}C_{m1}}{C_{m1}C_{m2}r^2_{FFVF}} \quad (4.8)$$

The value of the GBW can be obtained by multiplying dc gain A_{dc} with dominant pole frequency ω_{p1} i.e.

$$\text{GBW} = A_{dc}.\omega_{p1} = \frac{g_{m1}}{C_{m1}} \quad (4.9)$$

From Eqs. 4.4-4.6, it is evident that the proposed amplifier 2 has no RHP pole. So, it is unconditionally stable. Since the output resistance of FFVF is lower, so the first non-dominant pole, ω_{p2}, moves away from the origin, resulting in improved performance of compensation using FFVF in comparison with FVF. Also from Eq. 4.8, it can be observed that RHP zero ω_{z2} is now shifted to a very high frequency since it is multiplied with the second stage gain $g_{m2}r_{o2}$. So this RHP zero will not upset the phase margin, which leads to higher stability of the circuit.

4.2.3 Simulation results and discussions

The functionality of the proposed amplifier 2 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 2 is enlisted in Table 4.1.

Table 4.1 Design parameters of proposed amplifier 2

Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M2: W=100 µm, L=0.35 µm; M3, M4, M7: W=60 µm, L=0.35 µm M5, M6, M14, M15: W=20 µm, L=1 µm; M8: W=10 µm, L= 1 µm; M9: W=15 µm, L= 1 µm; M10: W=5 µm, L= 1 µm; M11: W=60 µm, L= 1 µm; M12: W=12 µm, L= 0.35 µm; M13: W=150 µm, L= 0.35 µm; M16: W=40 µm, L= 1 µm
C_{m1} C_{m2}	12.5 pF 0.4 pF
Biasing current (I)	10 µA
C_L	100 pF

Figure 4.4 displays the frequency response of the proposed amplifier 2. Proper selection of element values leads to a maximally-flat magnitude response with a significant improvement in bandwidth for the amplifier. From the frequency response, it can be seen that GBW is 26 MHz for the proposed amplifier 2 with the optimum value of phase margin. It ensures good

stability of the amplifier. Also, it has a DC gain of more than 100 dB. Figure 4.5 displays the transient response of the proposed amplifier 2. The slew rate and and 1 % settling time are observed as 10 V/µS and 0.1µs respectively. Figure 4.6 depicts the frequency response of CMRR for the proposed amplifier 2 and its value is found to be 86.1 dB. Further, Fig. 4.7 displays the PSRR of the proposed amplifier 2. The PSRR is observed to be 78 dB.

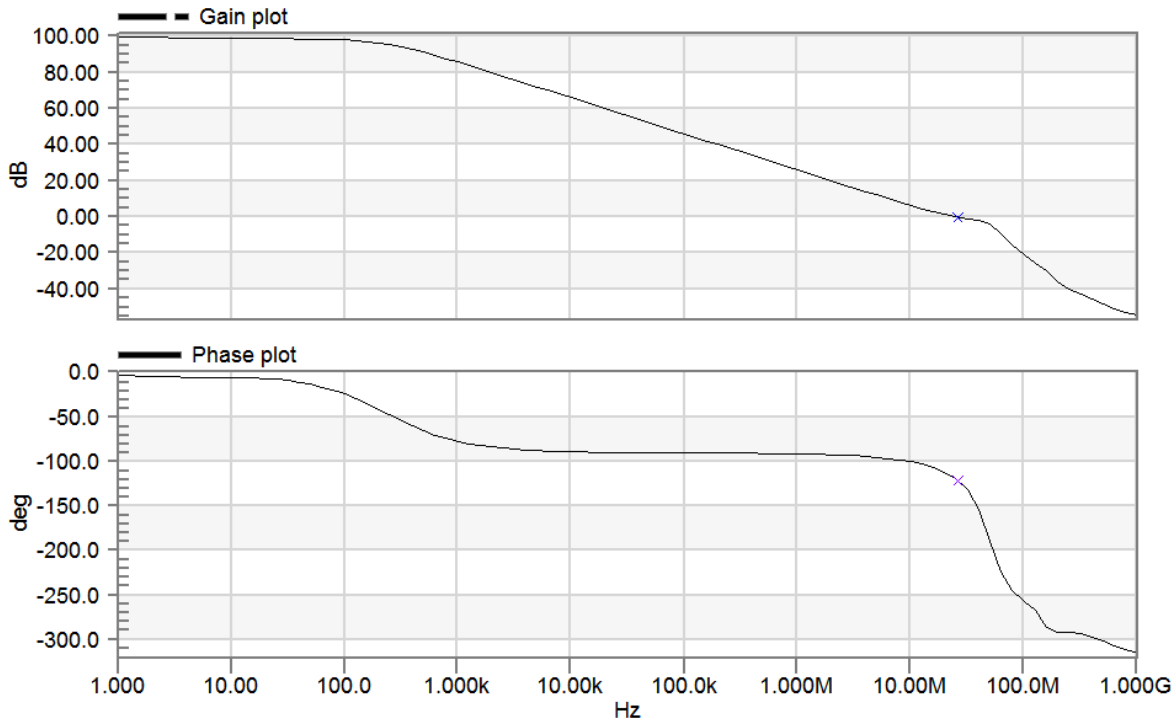


Fig. 4.4 Frequency response of proposed amplifier 2

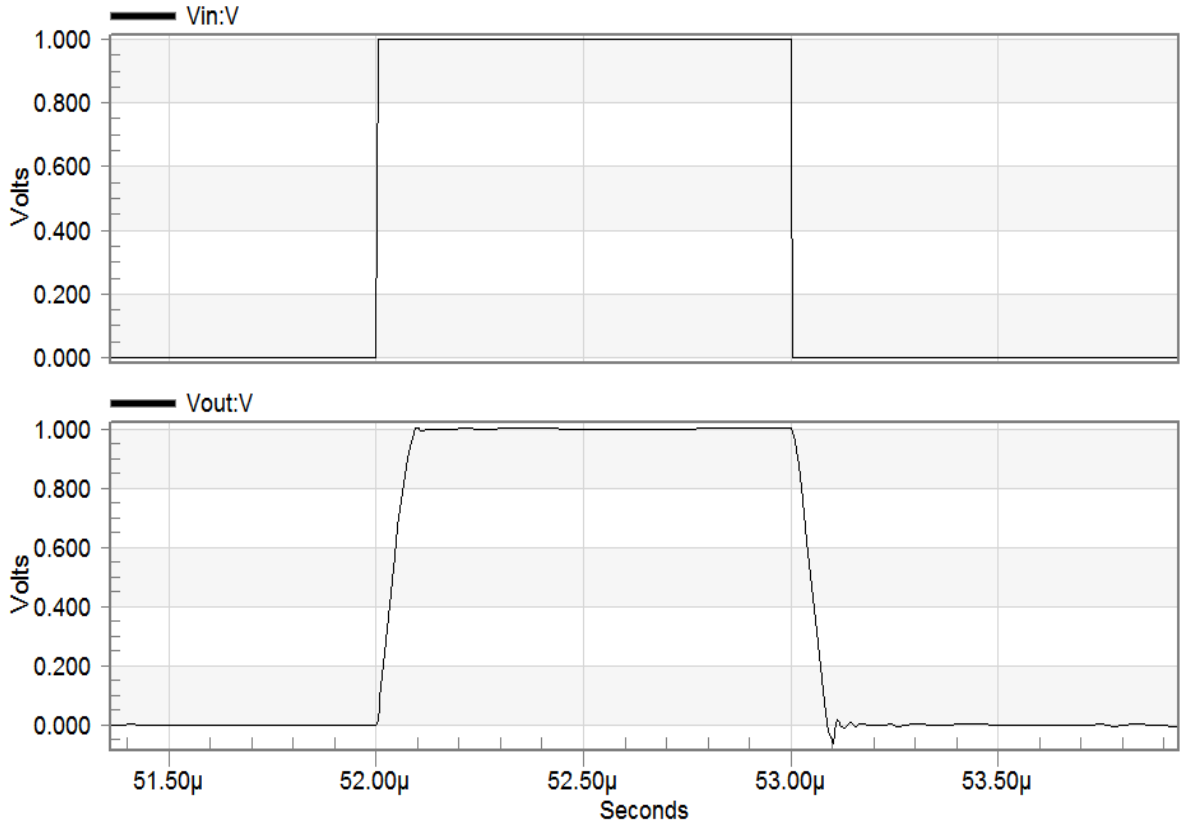


Fig. 4.5 Transient response of proposed amplifier 2

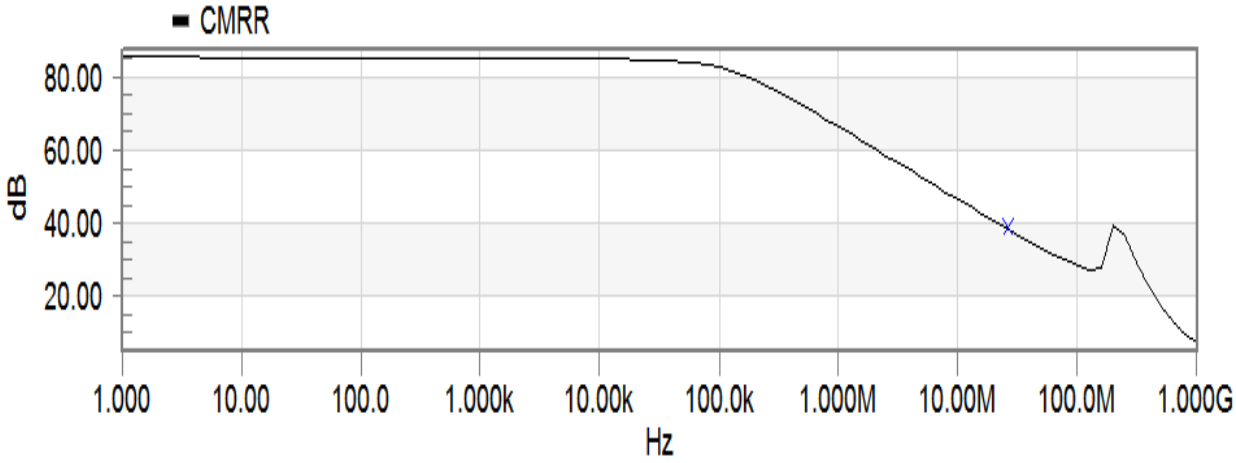


Fig. 4.6 Frequency response of CMRR of proposed amplifier 2

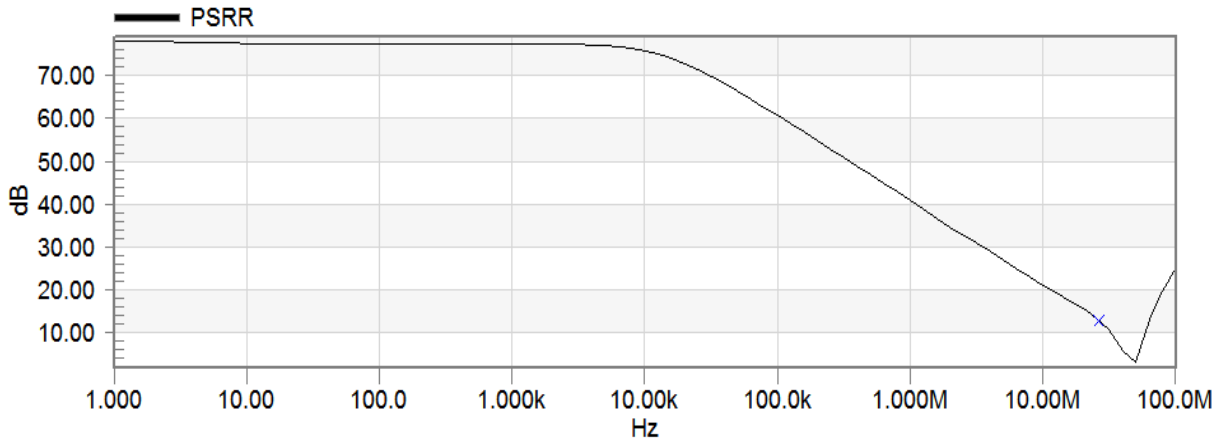


Fig. 4.7 Frequency response of PSRR of proposed amplifier 2

Process corner analysis (Fig. 4.8) has been done to examine the robustness of the proposed amplifier 2 over process variations that statistically occur during wafer production. Table 4.2 shows the variation of gain, GBW and PM for various process corners. It can be seen that the maximum variations in (Gain, GBW, PM) with respect to TT process corner are within 20%.

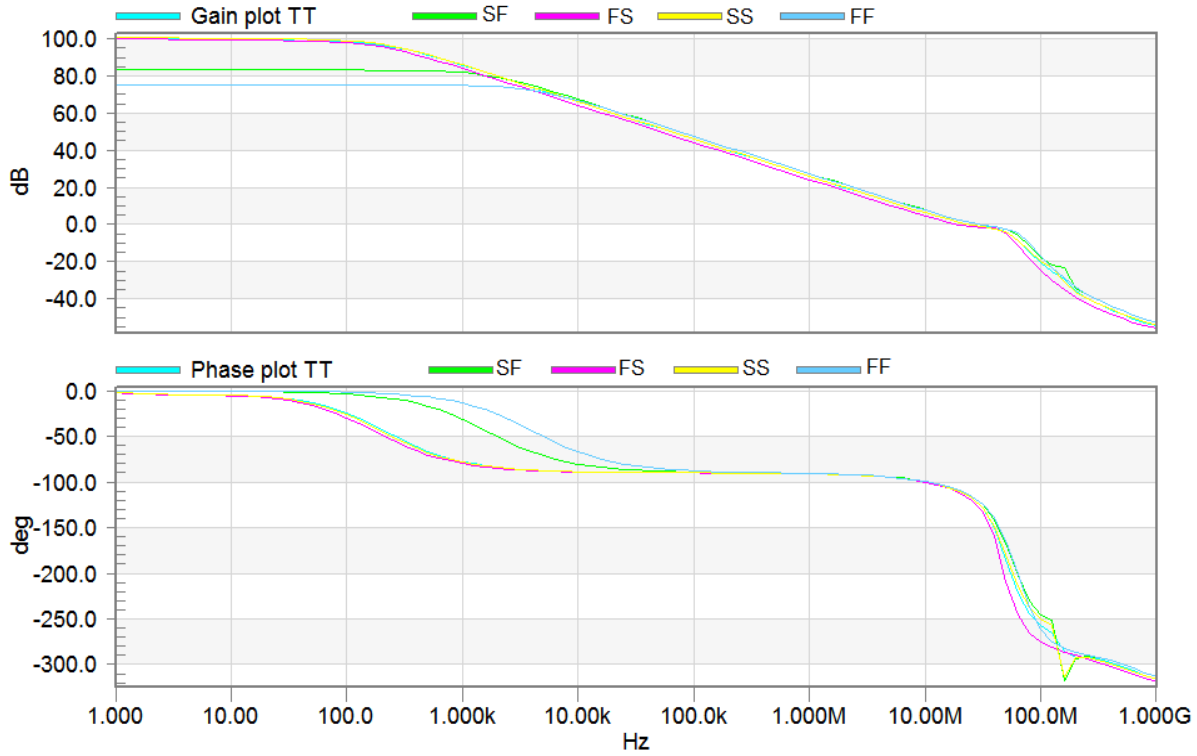


Fig. 4.8 Frequency response of proposed amplifier 2 at different process corners

Further, a supply voltage variation of ±5% is considered, and the frequency response of the amplifier is given in Fig. 4.9. Additionally, the corresponding results are placed in Table 4.2. It is noted that the maximum variations in (Gain, GBW, PM) for the proposed amplifier 2 are (10%, 10.6%, 6.45%). Thus, the overall maximum variation with respect to supply voltage is within 11%.

Further, Monte-Carlo simulations (100 runs) are carried out for 5% Gaussian distribution of power supply; and the gain and phase plots for the proposed amplifier 2 is shown in Fig. 4.10. The (mean, standard deviation) in gain for the proposed amplifier 2 is (92.75 dB, 14.43 dB).

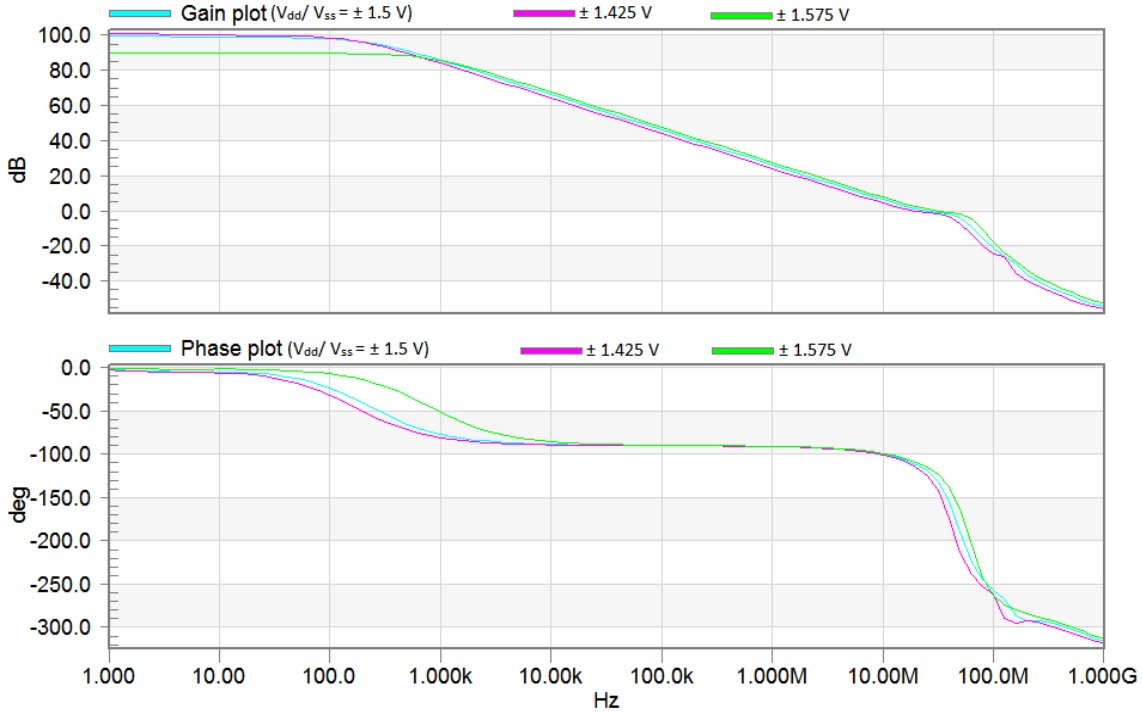


Fig. 4.9 Frequency response of proposed amplifier 2 with variations in supply voltage

Table 4.2 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 2

Performance parameter	Corner					Supply Voltage variation (1.5V ± 5% of 1.5V)	
	TT	SF	FS	SS	FF	1.425V	1.575V
Gain (dB)	101	85	101	101	77	102	90.9
GBW (MHz)	26.3	27.7	27	29	25.1	25.7	29.1
PM (°)	62	67	59	59	69	58	61

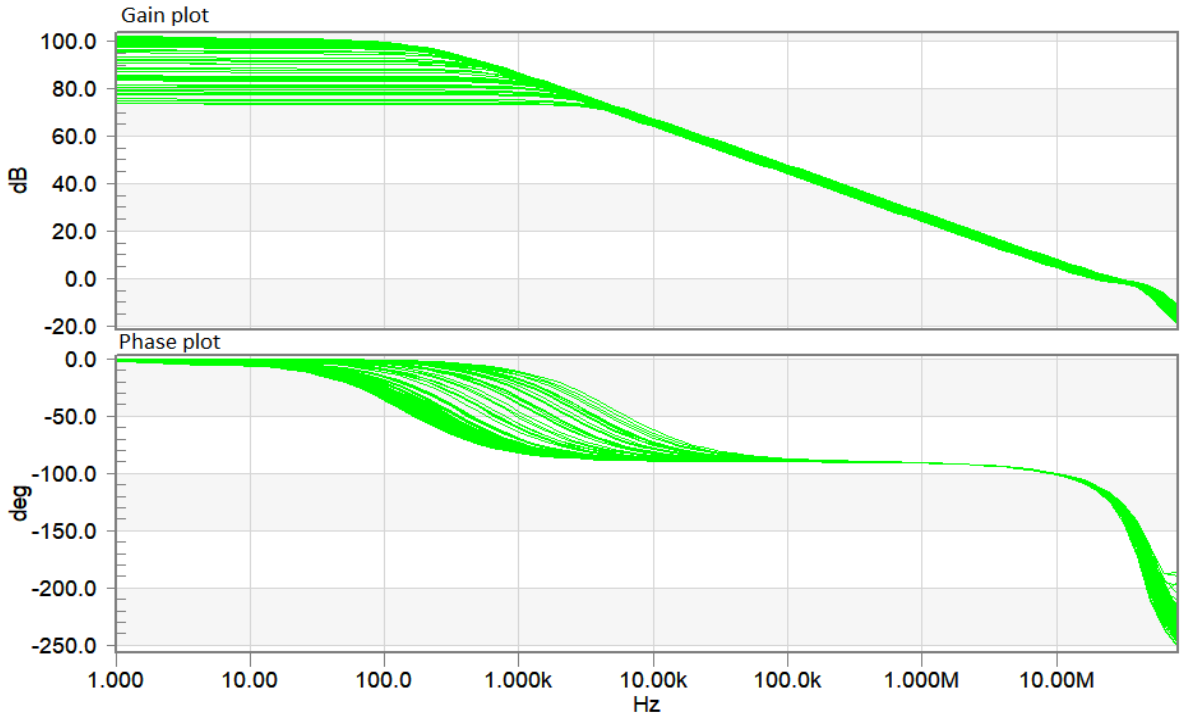


Fig. 4.10 Monte-Carlo analysis for frequency response of the proposed amplifier 2 against supply voltage variations

4.3 Proposed amplifier 3

The block diagram of the proposed amplifier 3 is shown in Fig. 4.11. The circuit utilizes FFVF in the inner loop of RNMC similar to proposed amplifier 2, and a resistor R_m in the outer compensation loop to achieve double pole-zero cancellation that occurs beyond gain-bandwidth product (GBW). In the proposed amplifier 3, the compensation structure includes Miller capacitors

$C_{m1,}$ $C_{m2,}$ feed forward stage g_{mf}, resistor R_m, and folded flipped voltage follower (FFVF), whose output resistance is r_{FFVF}.

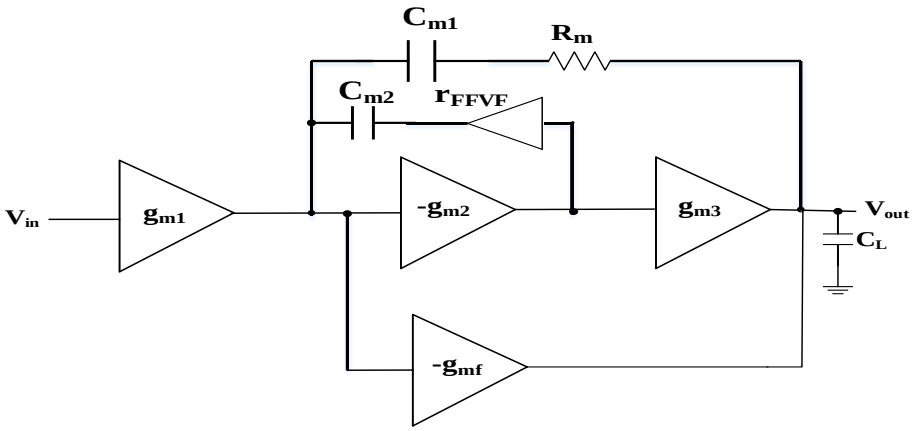


Fig. 4.11 Block diagram of proposed amplifier 3

4.3.1 Circuit description of proposed amplifier 3

Figure 4.12 shows the transistor level diagram of the proposed amplifier 3. The input stage is the differential amplifier, which consists of transistors M1-M4 and M6. The second stage is a common source amplifier (transistors M7-M8). The third stage is a non-inverting stage, which is formed by transistors M12-M15. Transistors M9-M11 and M16 form the FFVF circuit. Further, two Miller capacitors, C_{m1} and C_{m2}, are connected in the feedback loop of RNMC. The compensation capacitor C_{m1} and a resistor R_m are connected between the output of the third stage and the first stage, while C_{m2} is connected between the output of FFVF and the first stage. Moreover, transistor M13 is connected to the output of differential stage, resulting in a push pull output stage with better slew rate performance.

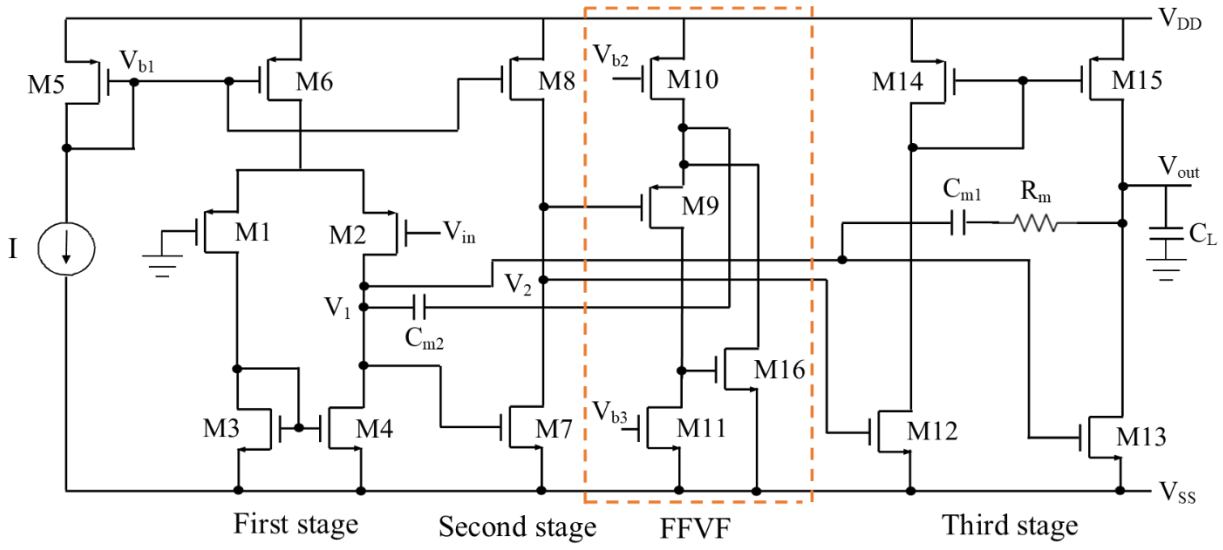


Fig. 4.12 Transistor level implementation of proposed amplifier 3

4.3.2 Small signal analysis of proposed amplifier 3

The small signal analysis is performed to find out the transfer function of the proposed amplifier 3. The small signal model of the amplifier is shown in Fig. 4.13. To simplify the calculations, following assumptions are made,

$$g_{m1}r_{o1},\ g_{m2}r_{o2},\ g_{m3}r_{o3} >> 1 \tag{4.10}$$

$$C_L,\ C_{m1},\ C_{m2} >> C_1,\ C_2 \tag{4.11}$$

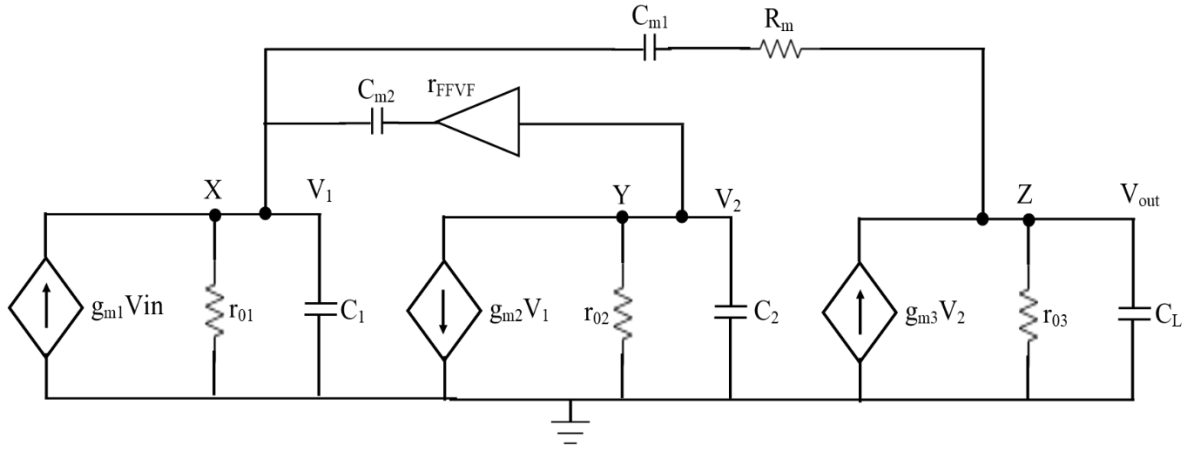


Fig. 4.13 Small signal model of proposed amplifier 3

Equation 4.12 gives the transfer function of the proposed amplifier 3.

$$A(s) = \frac{A_{dc}}{(1+\frac{s}{\omega_{p1}})} \frac{[1+(R_m C_{m1} + r_{FFVF} C_{m2})s + r_{FFVF} R_m C_{m1} C_{m2} s^2]}{[1+\frac{C_{m2}(C_L + C_{m1} + g_{m3} r_{FFVF} C_{m1})}{g_{m3} C_{m1}} s + \frac{R_m C_{m2} C_L}{g_{m3}} s^2]} \quad (4.12)$$

where A_{dc} is the low frequency gain and given by, $A_{dc} = g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3}$ (4.13)

According to the denominator of the open loop transfer function (Eq. 4.12), the amplifier contains the dominant pole ω_{p1} which is defined as,

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} C_{m1}} \quad (4.14)$$

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1}}{C_{m1}} \quad (4.15)$$

The transfer function of the proposed amplifier 3 exhibits two high frequency intermediate poles and two zeros, which are allocated in the left half plane (LHP) by a suitable choice of the components of the compensation structure. These two LHP zeros can cancel out the two high frequency non-dominant poles. It can be achieved by equating the coefficients of second order polynomials of Eq. 4.12. After doing so, we get the equations for R_m and r_{FFVF}.

$$R_m = \frac{C_{m2}}{C_{m1}} \left(1 + \frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.16)$$

$$r_{FFVF} = \left(\frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.17)$$

After double pole-zero cancellation, Eq. 4.12 is reduced to a single pole transfer function, and the phase margin is 90° (neglecting the effect of the parasitic pole). Also, Eqs. 4.16-4.17 require the matching between a resistance and two transconductance values, so process variations may lead to incomplete elimination of the poles and zeros. Eq. 4.16 helps in selecting the value of R_m. Further, the condition for the first dominant pole-zero doublet to be placed beyond the unity gain frequency (Eq. 4.18) of the open loop amplifier gain, can be obtained from Eqs. 4.12 and 4.15.

$$\left(\frac{1}{R_m C_{m1} + r_{FFVF} C_{m2}} \right) > \frac{g_{m1}}{C_{m1}} \tag{4.18}$$

4.3.3. Simulation results and discussions

The functionality of the proposed amplifier 3 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 3 is enlisted in Table 4.3.

Table 4.3 Design parameters of proposed amplifier 3

Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M2: W=100 µm, L=0.35 µm; M3, M4, M7: W=60 µm, L=0.35 µm M5, M6, M14, M15: W=20 µm, L=1 µm; M8: W=10 µm, L= 1 µm M9: W=15 µm, L= 1 µm; M10: W=5 µm, L= 1 µm; M11: W=60 µm, L= 1 µm; M12: W=12 µm, L= 0.35 µm; M13: W=150 µm, L= 0.35 µm; M16: W=40 µm, L= 1 µm
C_{m1} C_{m2}	12.5 pF 0.5 pF
R_m	150 Ω
Biasing current (I)	10 µA
C_L	100 pF

Figure 4.14 displays the frequency response of the proposed amplifier 3. From the frequency response, it can be observed that GBW is 30 MHz with an optimum phase margin for the proposed amplifier 3. Moreover, the DC gain is more than 100 dB. Figure 4.15 shows the transient response of the proposed amplifier 3. The slew rate is observed as 10 V/µS, and 1 % settling time is 0.1 µs. Figures 4.16 and 4.17 depict the frequency responses of CMRR and PSRR, respectively. The CMRR is noted as 86.1 dB whereas the PSRR is found as 78 dB.

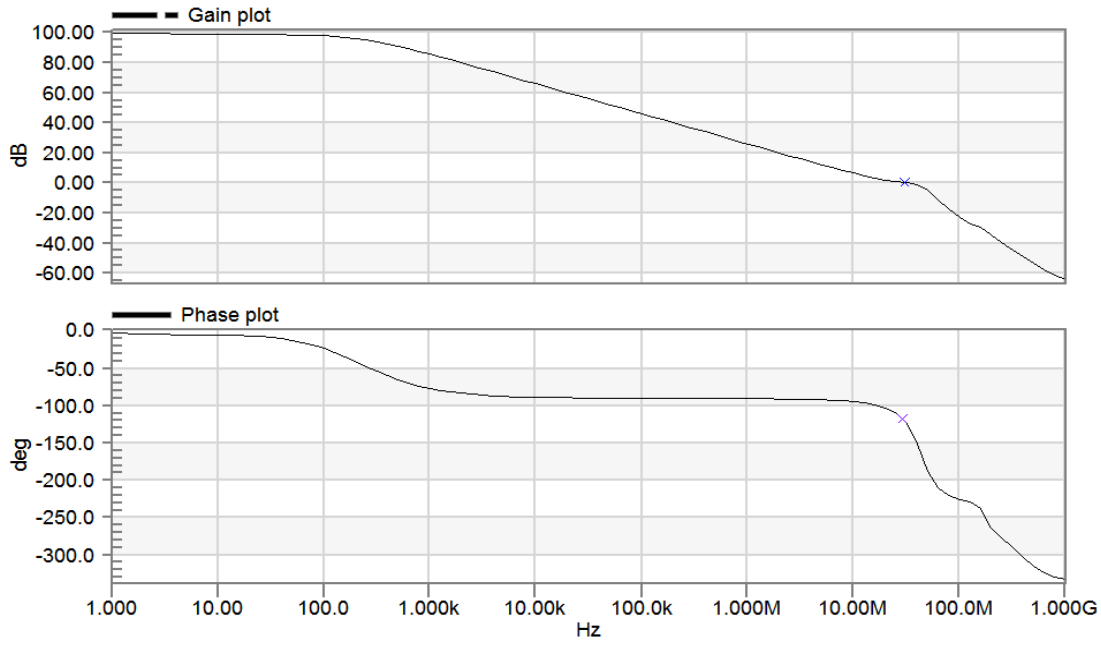


Fig. 4.14 Frequency response of proposed amplifier 3

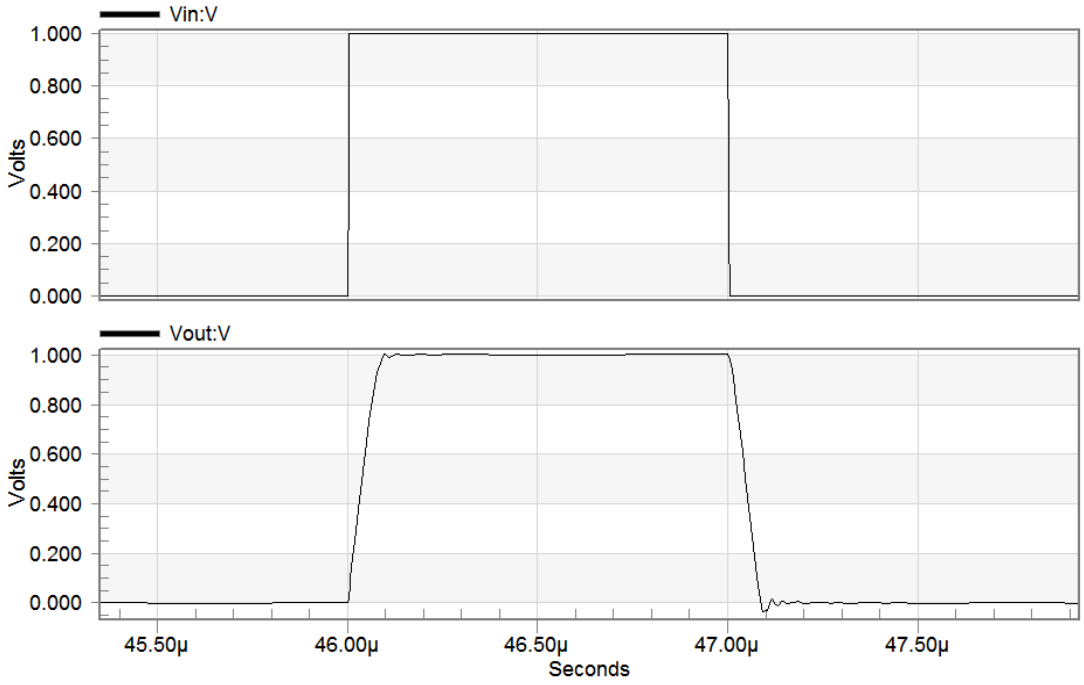


Fig. 4.15 Transient response of proposed amplifier 3

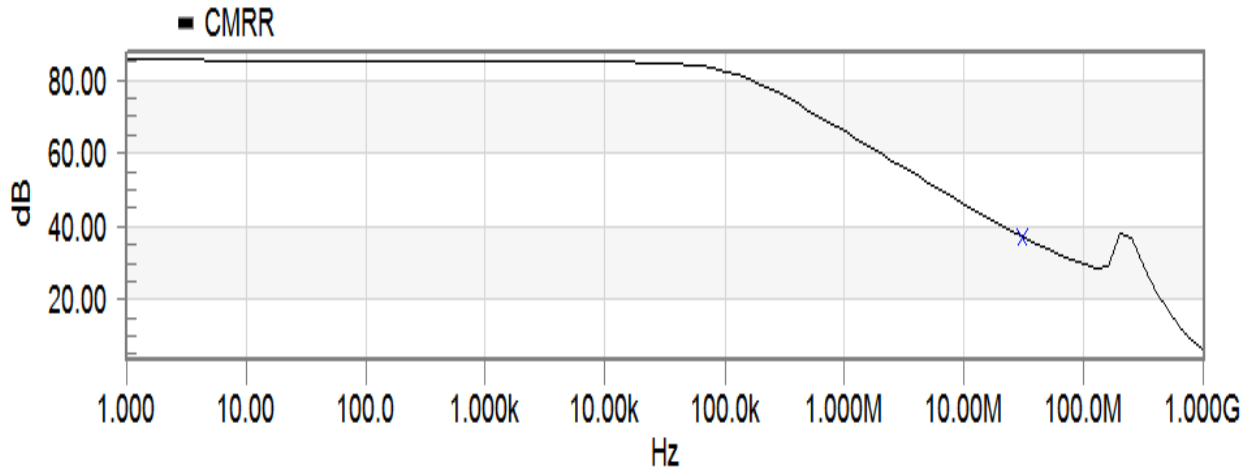


Fig. 4.16 Frequency response of CMRR of proposed amplifier 3

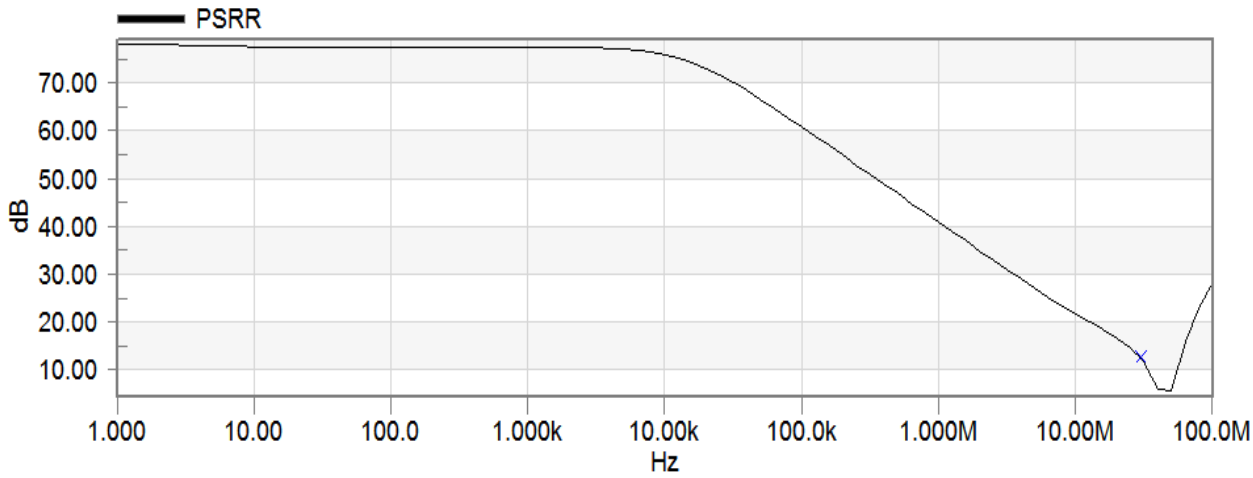


Fig. 4.17 Frequency response of PSRR of proposed amplifier 3

The robustness of the proposed amplifier 3 over process variations is ensured by the process corner analysis, which is shown in Fig. 4.18. Table 4.4 shows the results for various process corners. It is observed that the maximum variations in (Gain, GBW, PM) with respect to TT process corner are within 20%. Figure 4.19 displays the frequency response of the proposed amplifier 3 for the supply voltage variation of ±5%. The corresponding results are included in Table 4.4. The maximum variations in (Gain, GBW, PM) for the proposed amplifier 3 are found to be (9.9%, 12.3%, 3.33%) with respect to supply voltage. So, the overall maximum variation with respect to supply voltage is within 13%. Further, Monte-Carlo simulations (100 runs) are carried out for 5% Gaussian distribution of power supply,

and the frequency response for the proposed amplifier 3 is displayed in Fig. 4.20. The (mean, standard deviation) in gain for the proposed amplifier 3 is (92.75 dB, 14.43 dB).

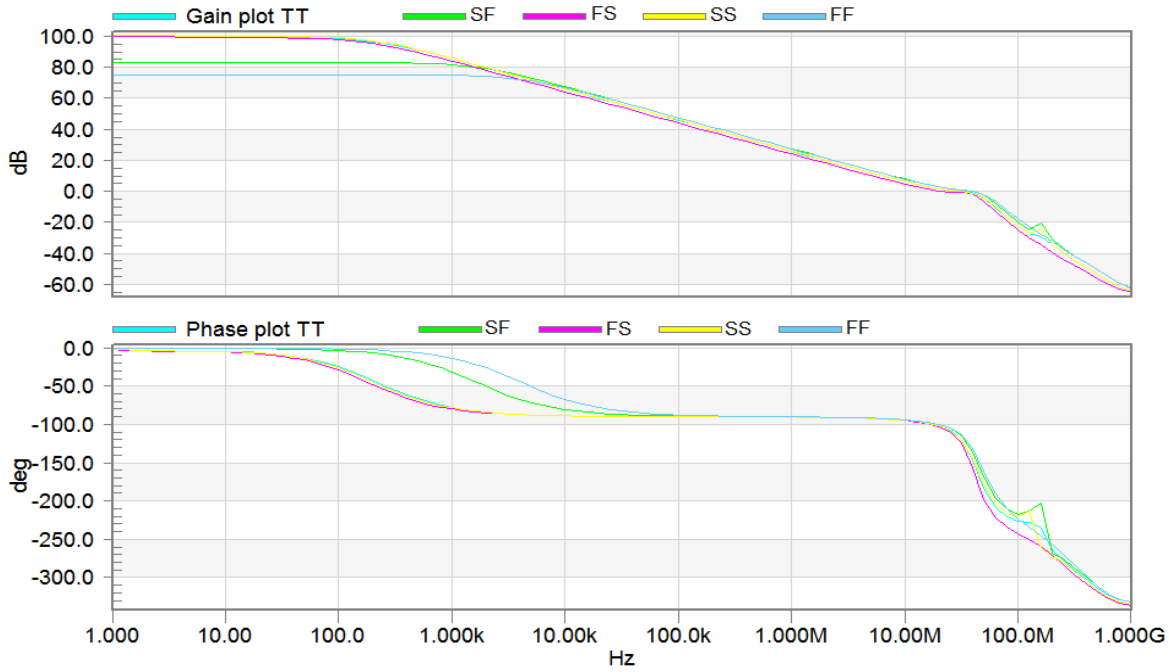


Fig. 4.18 Frequency response of proposed amplifier 3 at different process corners

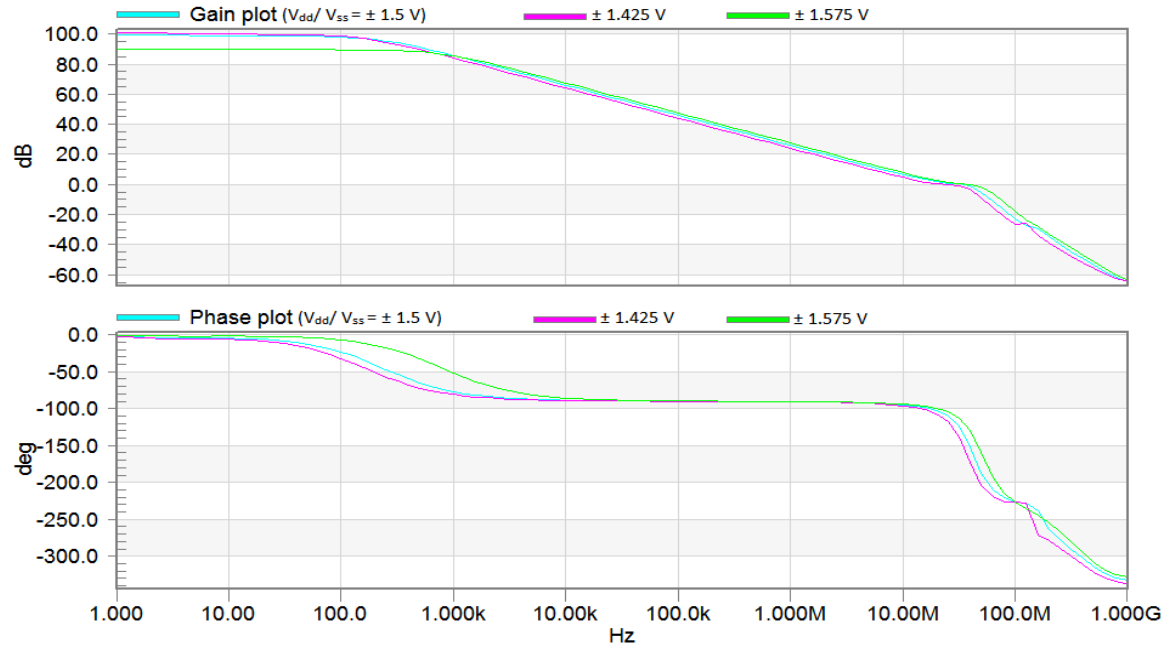


Fig. 4.19 Frequency response of proposed amplifier 3 with variations in supply voltage

Table 4.4 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 3

Performance parameter	Corner					Supply Voltage variation (1.5V ± 5% of 1.5V)	
	TT	SF	FS	SS	FF	1.425V	1.575V
Gain (dB)	101	86	101	101	77.5	102	91
GBW (MHz)	31.6	29.8	29.1	31.4	28.4	28.4	35.5
PM (°)	60	66	62	59	68	58	59

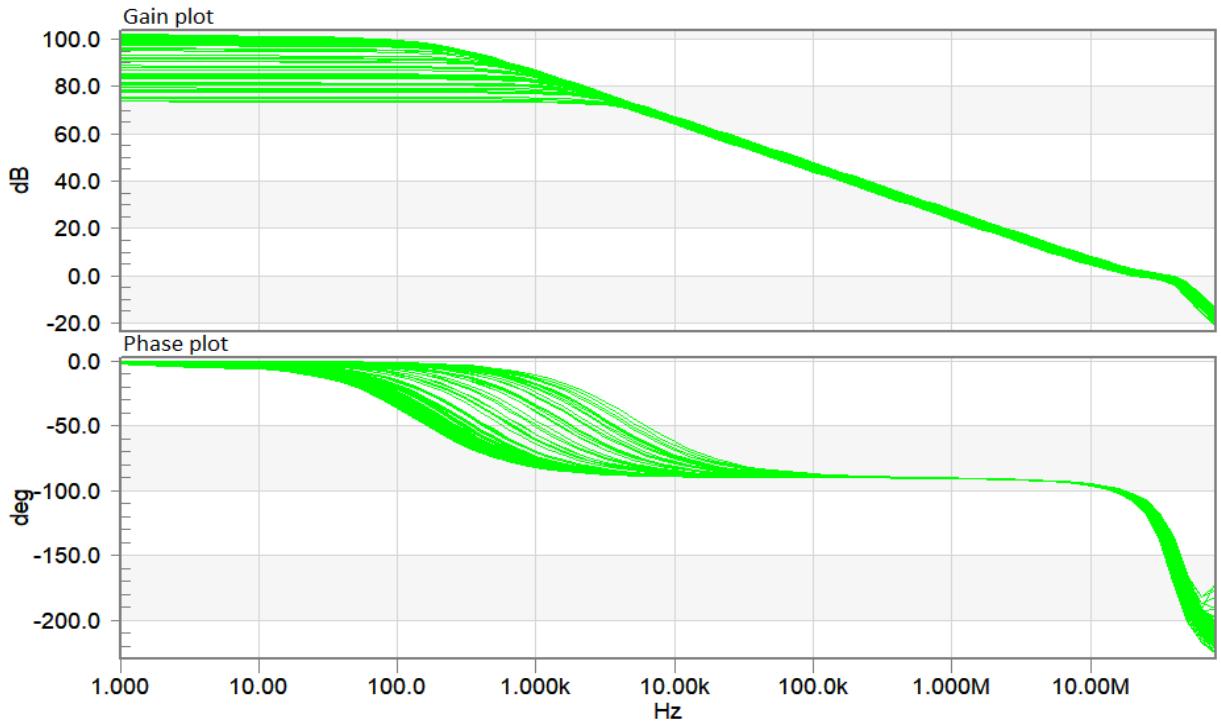


Fig. 4.20 Monte-Carlo analysis for frequency response of the proposed amplifier 3 against supply voltage variations

4.4 Proposed amplifier 4

The block diagram of the proposed amplifier 4 is shown in Fig. 4.21. A self cascode structure has been utilized in the input stage to improve the GBW of the proposed amplifier 4. Further, the compensation structure of the proposed amplifier 4 includes the FFVF in the inner loop of the RNMC, and a resistor in the outer compensation loop. It results in double pole-zero cancellation that occurs beyond the gain-bandwidth product (GBW). Moreover, the feed forward path is employed to enhance the large signal response of the amplifier.

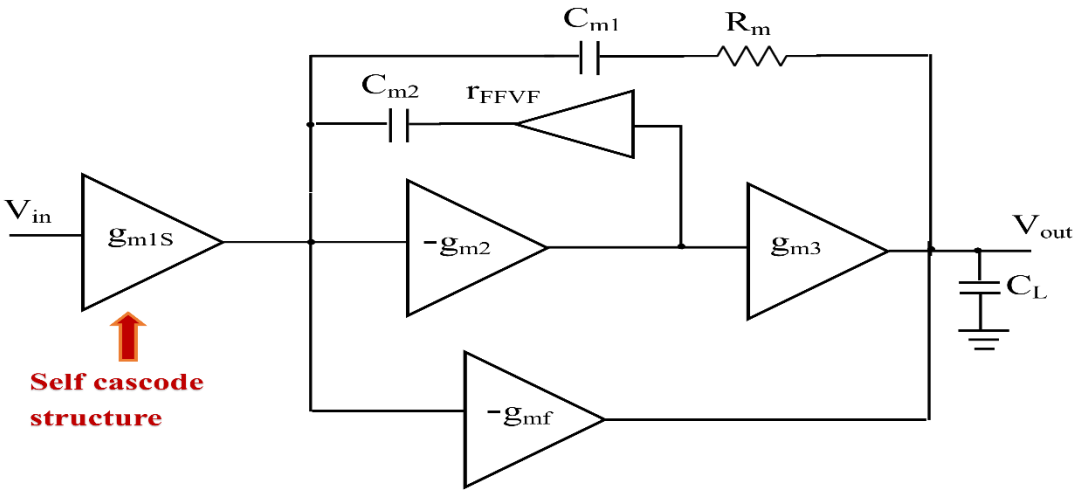


Fig. 4.21 Block diagram of proposed amplifier 4

4.4.1 Circuit description of proposed amplifier 4

Figure 4.22 displays the transistor level implementation of proposed amplifier 4. Transistors M1-M6 and M8 constitute the differential amplifier (first stage) based on the self cascode structure. A common source amplifier comprising the transistors M9 and M10 is used as the second stage. A non-inverting stage (M14-M17) is employed as the third stage to make the gain of the Miller's loop negative. Transistors M11-M13 and M18 form the FFVF circuit. The output of FFVF is connected to the compensation capacitor C_{m2}. It deals with the RHP zero issue. FFVF has the benefit of very low output resistance. The outer loop consists of a resistor R_m and compensation capacitor C_{m1}. To make the large signal response better, a transistor M15 is additionally connected to the first stage's output.

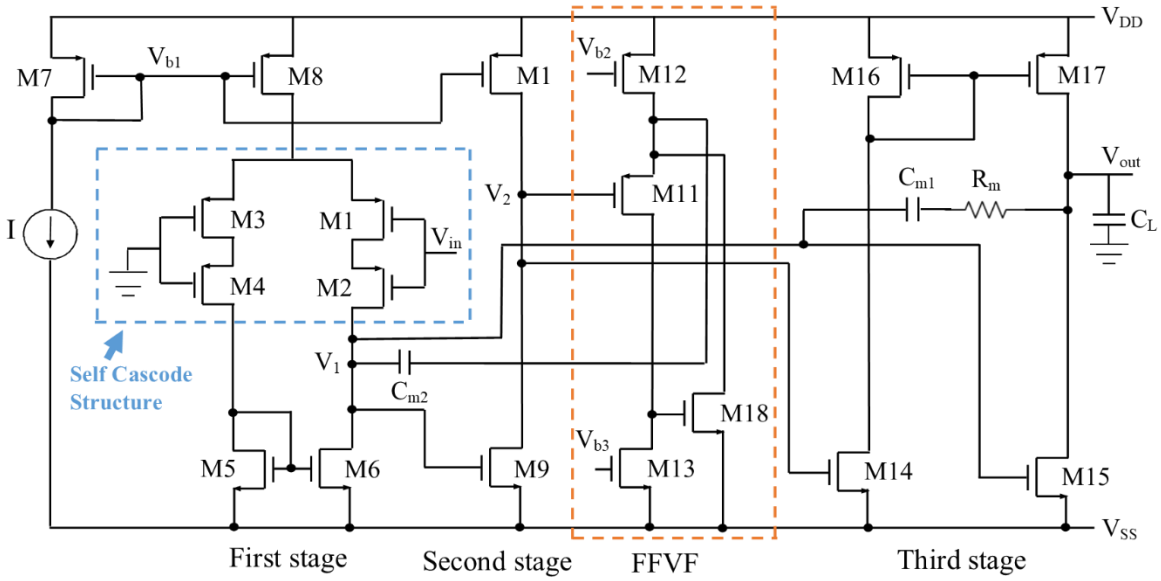


Fig. 4.22 Transistor level implementation of proposed amplifier 4

4.4.2 Small signal analysis of proposed amplifier 4

To find out the transfer function, the small signal analysis is performed. Figure 4.23 displays the small signal model of the proposed amplifier 4. To simplify the calculations, following assumptions are made,

$$g_{m1S}r_{o1},\ g_{m2}r_{o2},\ g_{m3}r_{o3} >> 1 \tag{4.19}$$

$$C_L,\ C_{m1},\ C_{m2} >> C_1,\ C_2 \tag{4.20}$$

where g_{m1S} represents the transconductance of the first stage.

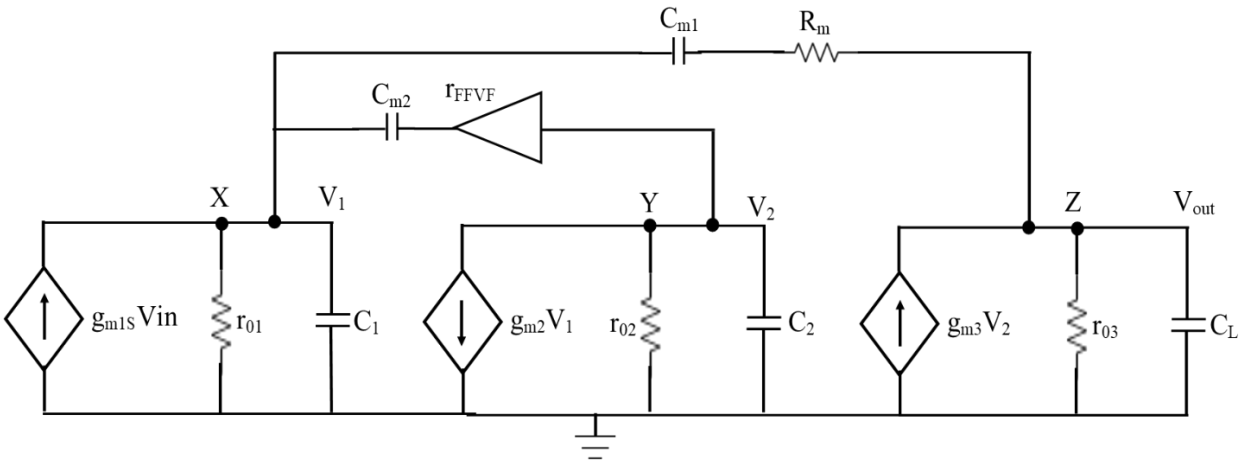


Fig. 4.23 Small signal model of proposed amplifier 4

The transfer function of the proposed amplifier 4 is provided by Eq. 4.21.

$$A(s) = \frac{A_{dc}}{(1+\frac{s}{\omega_{p1}})} \frac{[1+(R_m C_{m1} + r_{FFVF} C_{m2})s + r_{FFVF} R_m C_{m1} C_{m2} s^2]}{[1+\frac{C_{m2}(C_L + C_{m1} + g_{m3} r_{FFVF} C_{m1})}{g_{m3} C_{m1}} s + \frac{R_m C_{m2} C_L}{g_{m3}} s^2]} \quad (4.21)$$

where A_{dc} is the DC gain and given by, $A_{dc} = g_{m1S} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3}$ (4.22)

Eq. 4.21 gives the dominant pole ω_{p1}, which is provided by Eq. 4.23.

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} C_{m1}} \quad (4.23)$$

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1S}}{C_{m1}} \quad (4.24)$$

Equation 4.21 gives two high frequency intermediate poles and two zeros, which are allocated in the LHP by a suitable choice of the components of the compensation structure. These two LHP zeros can cancel out the two high frequency non-dominant poles. It can be achieved by equating the coefficients of second order polynomials of Eq. 4.21. After doing so, we get the equations for R_m and r_{FFVF}.

$$R_m = \frac{C_{m2}}{C_{m1}} \left(1 + \frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.25)$$

$$r_{FFVF} = \left(\frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.26)$$

After double pole-zero cancellation, Eq. 4.21 is reduced to a single pole transfer function, and the phase margin is 90° (neglecting the effect of the parasitic pole). Also, Eqs. 4.25-4.26 require the matching between a resistance and two transconductance values, so process variations may lead to incomplete elimination of the poles and zeros. Equation 4.25 helps in selecting the value of R_m. Further, the condition for the first dominant pole-zero doublet to be placed beyond the unity gain frequency (Eq. 4.27) of the open loop amplifier gain, can be obtained from Eqs. 4.21 and 4.24.

$$\left(\frac{1}{R_m C_{m1} + r_{FFVF} C_{m2}}\right) > \frac{g_{m1S}}{C_{m1}} \quad (4.27)$$

4.4.3 Simulation results and discussions

The functionality of the proposed amplifier 4 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 4 is enlisted in Table 4.5.

Table 4.5 Design parameters of proposed amplifier 4

Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M3, M15: W=150 µm, L=0.35 µm; M2, M4: W=300 µm, L=0.35 µm; M5, M6, M9: W=60 µm, L=0.35 µm; M7, M8, M16, M17: W=20 µm, L= 1 µm; M10: W=10 µm, L= 1 µm; M11: W=15 µm, L= 1 µm; M12: W=5 µm, L= 1 µm; M13: W=60 µm, L= 1 µm; M14: W=12 µm, L= 0.35 µm; M18: W=40 µm, L= 0.35 µm
C_{m1} C_{m2}	11 pF 0.5 pF
R_m	150 Ω
Biasing current (I)	10 µA
C_L	100 pF

Figure 4.24 depicts the frequency response of the proposed amplifier 4. From the frequency response, it can be seen that GBW is 31.3 MHz with sufficient phase margin, ensuring the better stability of the amplifier. Moreover, the minimum phase margin should be 45° for the amplifier to be stable. For the proposed amplifier 4, phase margin is more than 45°. Further, the DC gain is 103 dB. Figure 4.25 shows the transient response of the proposed amplifier 4. The slew rate is 9.71 V/µS, and 1 % settling time is 0.1 µs. The frequency responses of CMRR and PSRR are shown in Figs. 4.26-4.27 and the corresponding values are found as 89 dB and 81 dB.

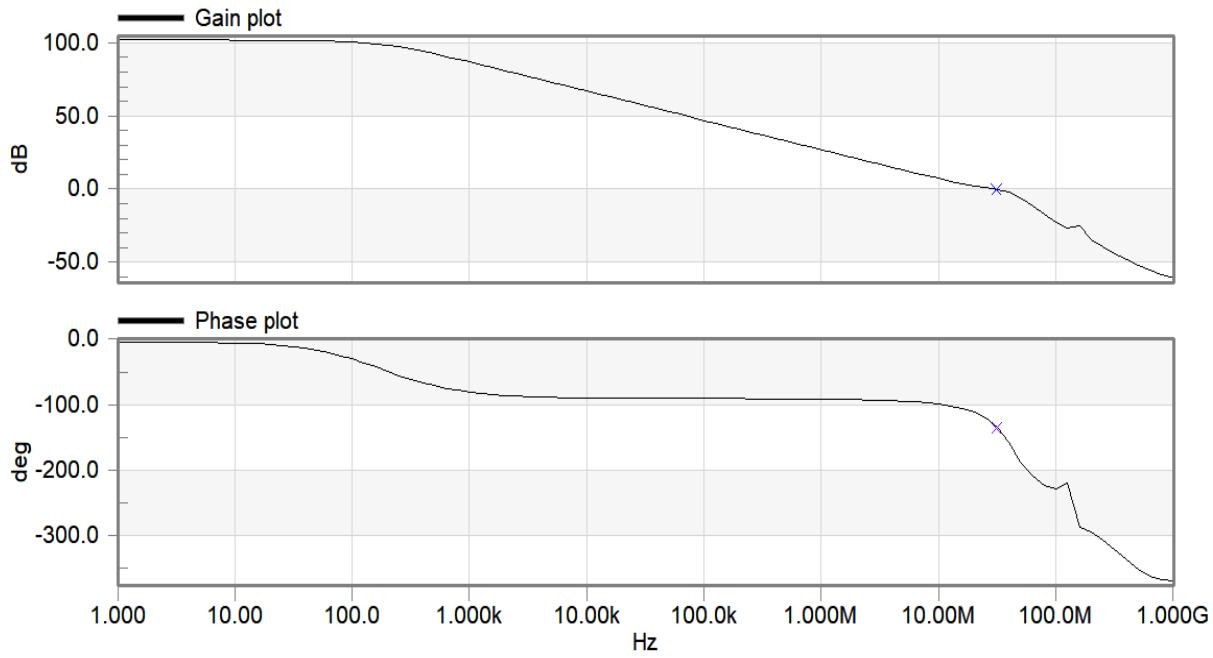


Fig. 4.24 Frequency response of proposed amplifier 4

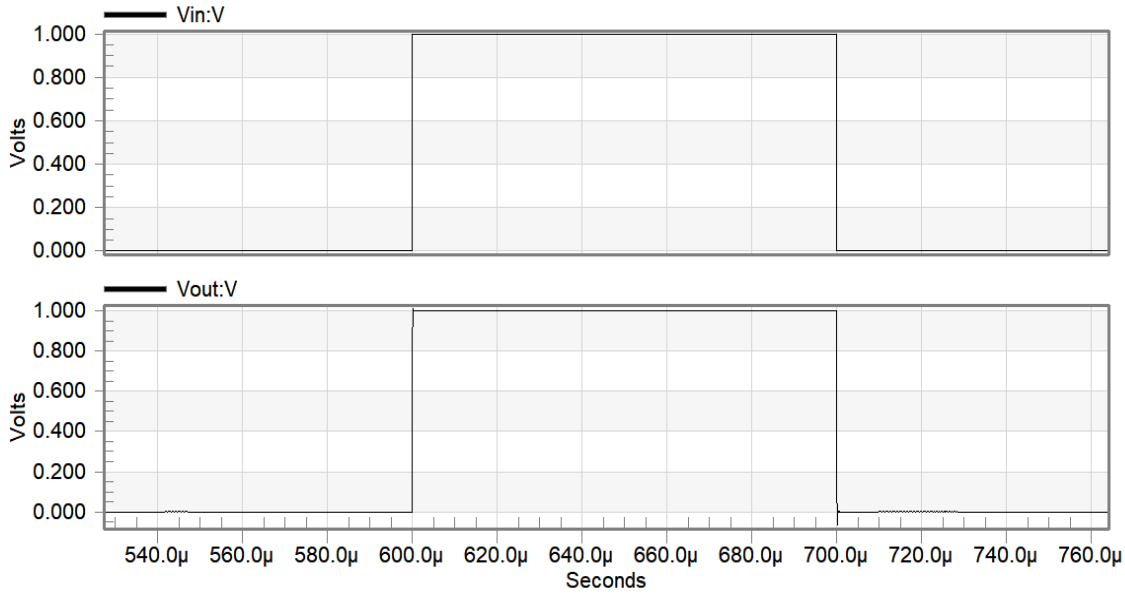


Fig. 4.25 Transient response of proposed amplifier 4

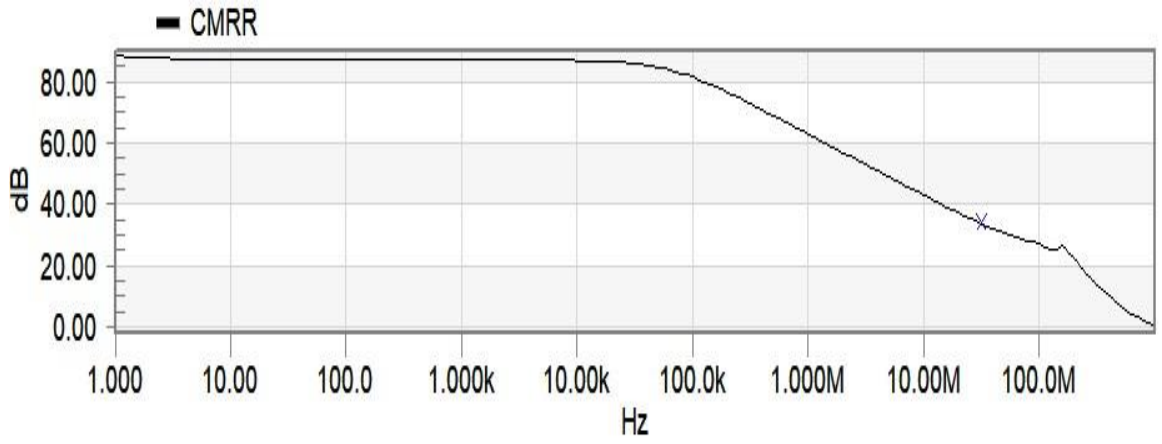


Fig. 4.26 Frequency response of CMRR of proposed amplifier 4

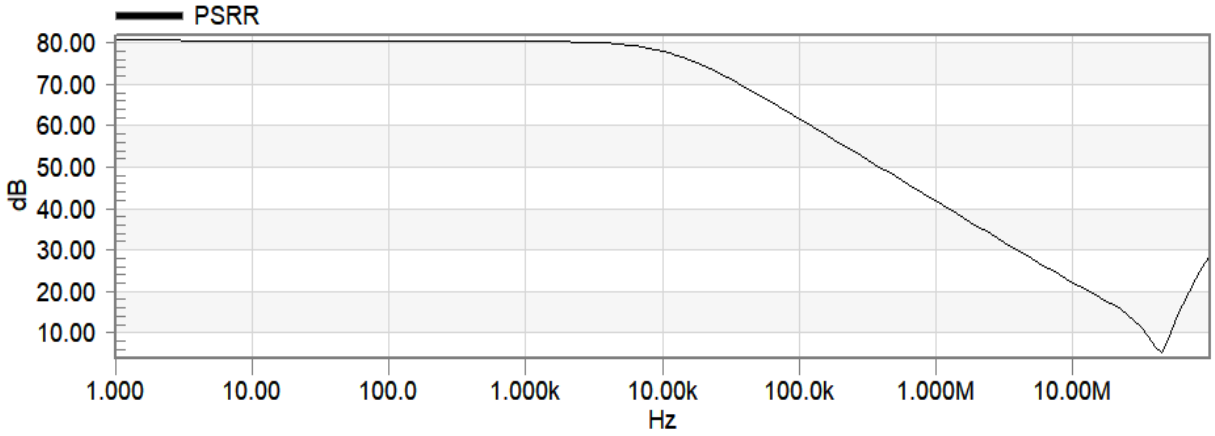


Fig. 4.27 Frequency response of PSRR of proposed amplifier 4

The robustness of the proposed amplifier 4 over process variations is ensured by the process corner analysis, which is shown in Fig. 4.28. Table 4.6 shows the results for various process corners. It is observed that the maximum variations in (Gain, GBW, PM) with respect to TT process corner are within 20% except for the variation in gain for FF process corner, for which the variation is 22.2%. Figure 4.29 displays the frequency response of the proposed amplifier 4 for the supply voltage variation of ±5%. The corresponding results are included in Table 4.6. The maximum variations in (Gain, GBW, PM) for the proposed amplifier 4 are (10.39%, 13.74%, 8%). So, the overall maximum variation with respect to supply voltage is within 14%. Further, Monte-Carlo simulations (100 runs) are carried out for 5% Gaussian distribution of power supply, and the frequency response for the proposed

amplifier 4 is displayed in Fig. 4.30. The (mean, standard deviation) in gain for the proposed amplifier 4 is noted as (97.18 dB, 18.1 dB).

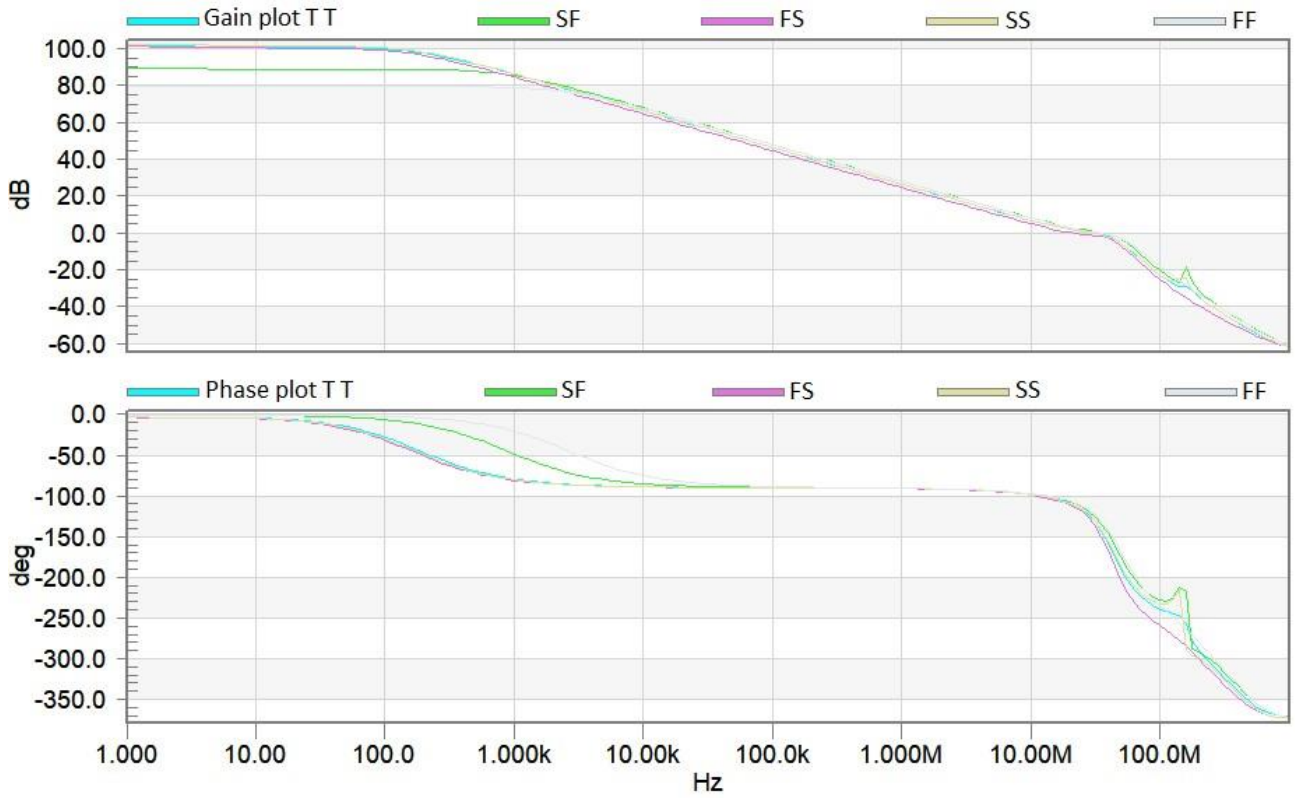


Fig. 4.28 Frequency response of proposed amplifier 4 at different process corners

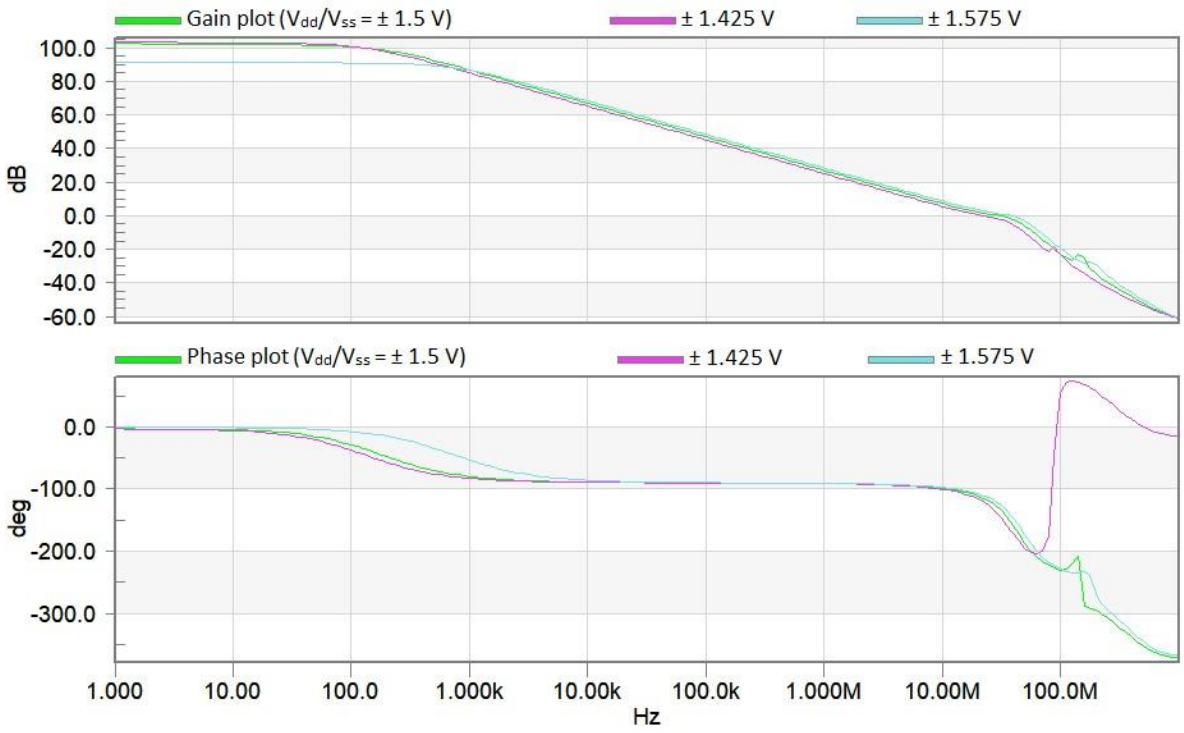


Fig. 4.29 Frequency response of proposed amplifier 4 with variations in supply voltage

Table 4.6 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 4

Performance parameter	Corner					Supply Voltage variation (1.5V ± 5% of 1.5V)	
	TT	SF	FS	SS	FF	1.425V	1.575V
Gain (dB)	103	89.4	102.3	103.5	80.1	104	92.3
GBW (MHz)	31.4	32.2	25.7	33	34.6	27	35.1
PM (°)	52	53	58	48	50	51	46

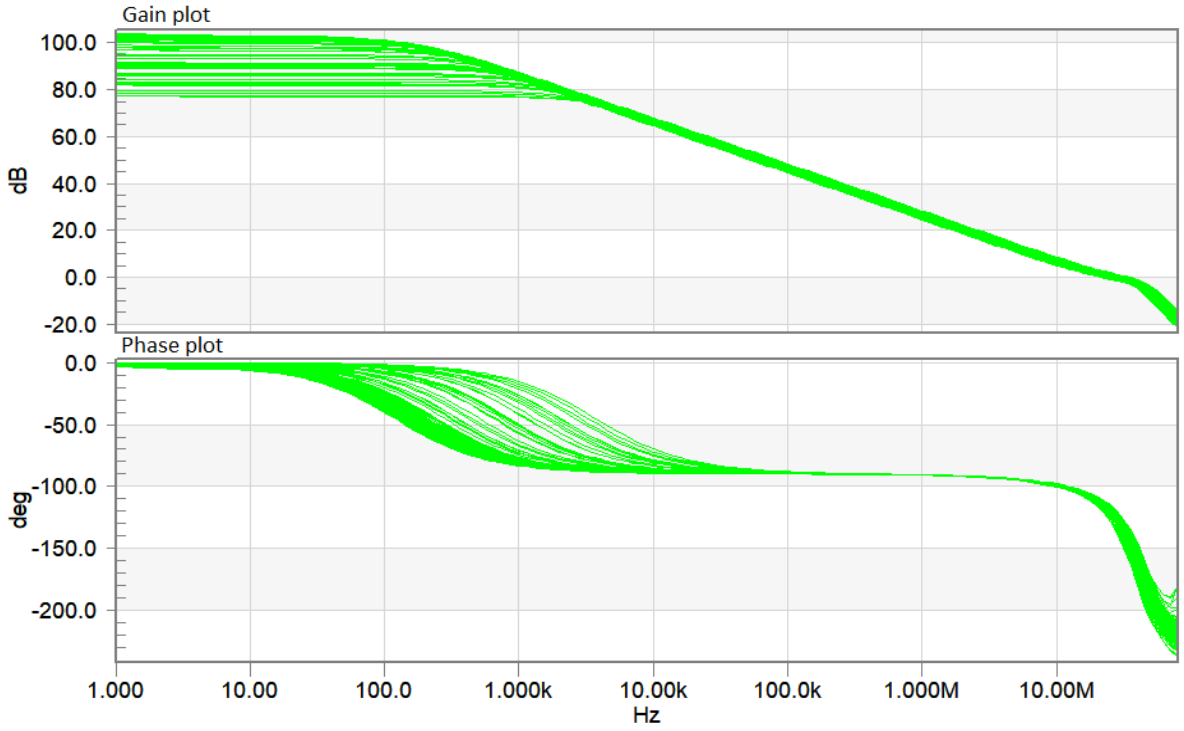


Fig. 4.30 Monte-Carlo analysis for frequency response of the proposed amplifier 4 against supply voltage variations

4.5 Proposed amplifier 5

The block diagram of the proposed amplifier 4 is shown in Fig. 4.31. A DTMOS structure has been utilized in the first stage to improve the GBW of the proposed amplifier 5. Further, FFVF is employed in the inner compensation loop of the RNMC, while a resistor is used in the outer compensation loop. Consequently, double pole-zero cancellation occurs. Moreover, the large signal response of the amplifier is enhanced with the help of the feed forward path.

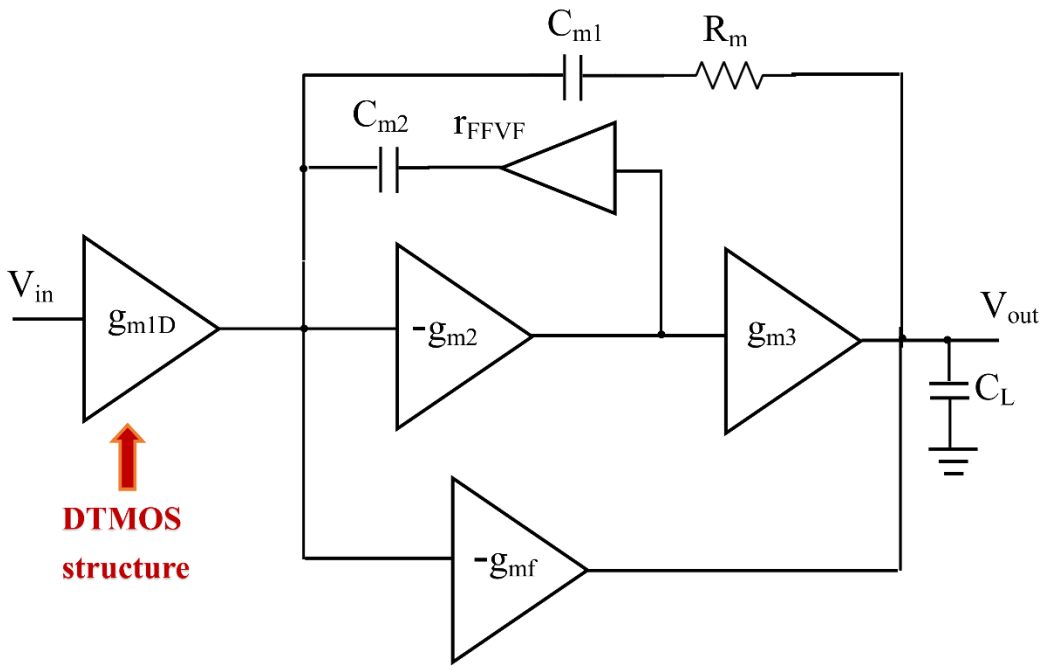


Fig. 4.31 Block diagram of proposed amplifier 5

4.5.1 Circuit description of proposed amplifier 5

The proposed amplifier 5 uses three stages, and the complete schematic is displayed in Fig. 4.32. The input stage of the proposed amplifier is a differential amplifier (M1-M4, M6) wherein input transistors M1 and M2 are DTMOS. The common source amplifier (M7-M8) makes up the second stage, which is an inverting stage, and keeps Miller loop gain negative. Further, the third stage is a non-inverting amplifier (M12-M15). The transistor M13 is further connected to the input stage's output to create a push-pull output stage, which enhances the transient response. In order to break the forward path, FFVF circuit is utilized along with C_{m2} in the inner loop. The FFVF circuit includes the transistors M9-M11, and M16. The outer compensation loop consists of the capacitor C_{m1} along with the resistor R_m. The use of FFVF and a resistor can cause double pole-zero cancellation, which enhances the phase margin of the amplifier.

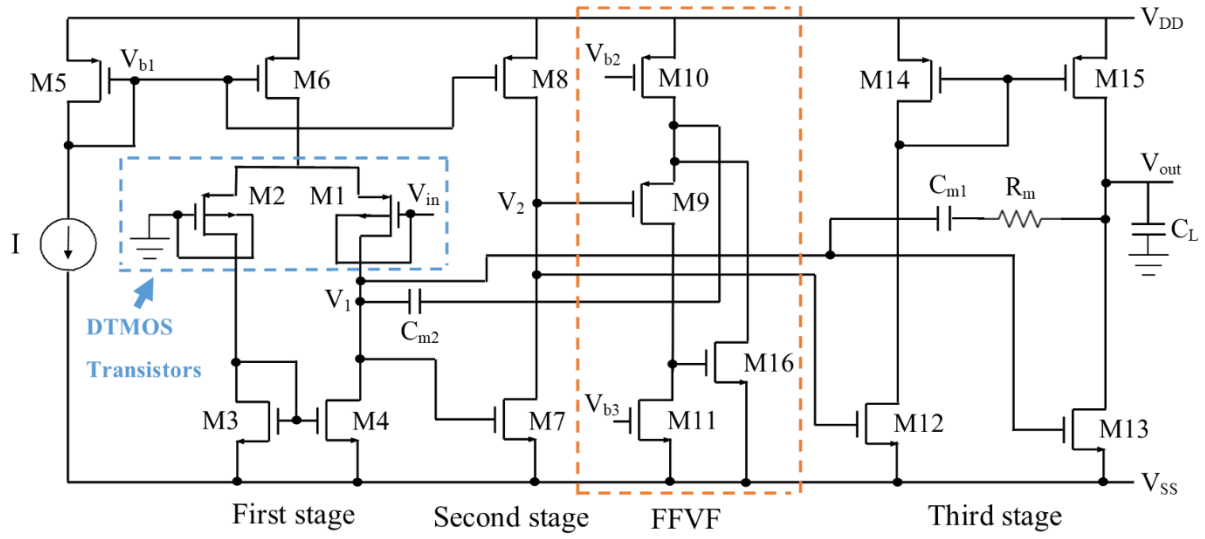


Fig. 4.32 Transistor level implementation of proposed amplifier 5

4.5.2 Small signal analysis of proposed amplifier 5

To find out the transfer function, the small signal analysis is performed using the small signal model of proposed amplifier 5 depicted in Fig. 4.33. To simplify the calculations, following assumptions are made,

$$g_{m1D}r_{o1},\ g_{m2}r_{o2},\ g_{m3}r_{o3} >> 1 \tag{4.28}$$

$$C_L,\ C_{m1},\ C_{m2} >> C_1,\ C_2 \tag{4.29}$$

where g_{m1D} represents the transconductance of the first stage.

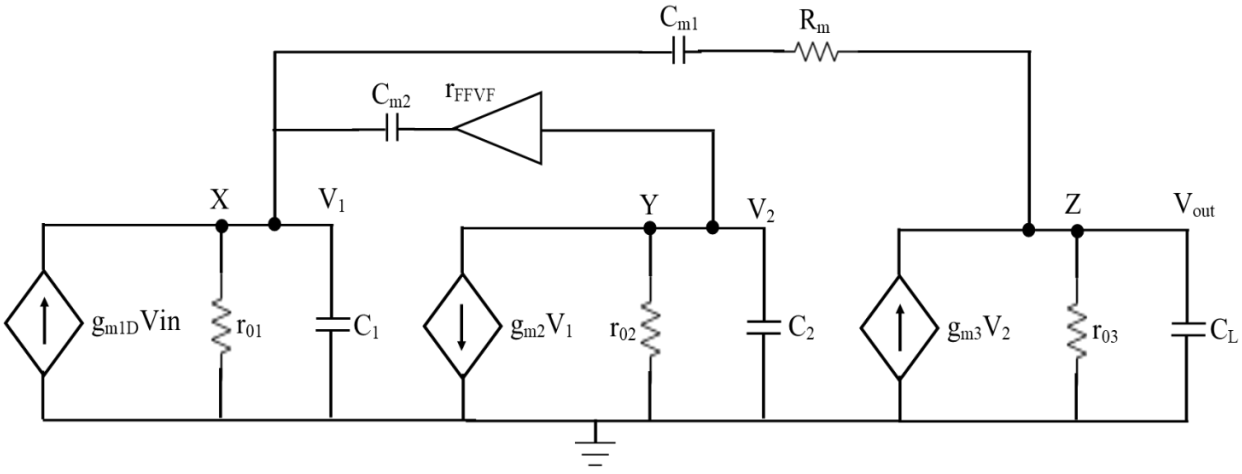


Fig. 4.33 Small signal model of proposed amplifier 5

The transfer function of the proposed amplifier 5 is provided by Eq. 4.30.

$$A(s) = \frac{A_{dc}}{(1+\frac{s}{\omega_{p1}})} \frac{[1+(R_m C_{m1} + r_{FFVF} C_{m2})s + r_{FFVF} R_m C_{m1} C_{m2} s^2]}{[1+\frac{C_{m2}(C_L + C_{m1} + g_{m3} r_{FFVF} C_{m1})}{g_{m3} C_{m1}} s + \frac{R_m C_{m2} C_L}{g_{m3}} s^2]} \quad (4.30)$$

where A_{dc} is the DC gain and given by, $A_{dc} = g_{m1D} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3}$ (4.31)

Equation 4.30 gives the dominant pole ω_{p1}, which is provided by Eq. 4.32.

$$\text{Dominant pole, } \omega_{p1} = \frac{1}{r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} C_{m1}} \quad (4.32)$$

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1D}}{C_{m1}} \quad (4.33)$$

Equation 4.30 gives two high frequency intermediate poles and two zeros, which are allocated in the LHP by a suitable choice of the components of the compensation structure. These two LHP zeros can cancel out the two high frequency non-dominant poles. It can be achieved by equating the coefficients of second order polynomials of Eq. 4.30. After doing so, we get the equations for R_m and r_{FFVF}.

$$R_m = \frac{C_{m2}}{C_{m1}} \left(1 + \frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.34)$$

$$r_{FFVF} = \left(\frac{C_L}{C_{m1}}\right) \frac{1}{g_{m3}} \quad (4.35)$$

After double pole-zero cancellation, Eq. 4.30 is reduced to a single pole transfer function, and the phase margin is 90° (neglecting the effect of the parasitic pole). Also, Eqs. 4.34-4.35 require the matching between a resistance and two transconductance values, so process variations may lead to incomplete elimination of the poles and zeros. Equation 4.30 helps in selecting the value of R_m. Further, the condition for the first dominant pole-zero doublet to be placed beyond the unity gain frequency (Eq. 4.36) of the open loop amplifier gain, can be obtained from Eqs. 4.30 and 4.33.

$$\left(\frac{1}{R_m C_{m1} + r_{FFVF} C_{m2}}\right) > \frac{g_{m1D}}{C_{m1}} \quad (4.36)$$

4.5.3 Simulation results and discussions

The functionality of the proposed amplifier 5 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 5 is enlisted in Table 4.7.

Table 4.7 Design parameters of proposed amplifier 5

Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M2: W=100 µm, L=0.35 µm; M3, M4, M7: W=60 µm, L=0.35 µm; M5, M6, M14, M15: W=20 µm, L= 1 µm; M8: W=10 µm, L= 1 µm; M9: W=15 µm, L= 1 µm; M10: W=5 µm, L= 1 µm; M11: W=60 µm, L= 1 µm; M12: W=12 µm, L= 0.35 µm M13: W=120 µm, L= 0.35 µm M16: W=40 µm, L= 1 µm
C_{m1} C_{m2}	14 pF 0.5 pF
R_m	100 Ω
Biasing current (I)	10 µA
C_L	100 pF

Figure 4.34 depicts the frequency response of the proposed amplifier 5. It is evident that the proposed circuit's GBW is 33.3 MHz, the highest of any three stage amplifiers currently in use. The proposed three stage amplifier also provides enough phase margin to stabilize the circuit with a DC gain of greater than 100 dB. The transient response of the amplifier is displayed in Fig. 4.35 by considering the unity gain configuration. It is illustrated by applying an input pulse of 1 V_{p-p}. The proposed amplifier has a slew rate of 9.71 V/µS. Further, 1% settling time is 0.1 µs. The frequency responses of CMRR and PSRR are shown in Figs. 4.36-4.37. The CMRR is 89 dB for the proposed amplifier 5. Further, the PSRR is 81.5 dB.

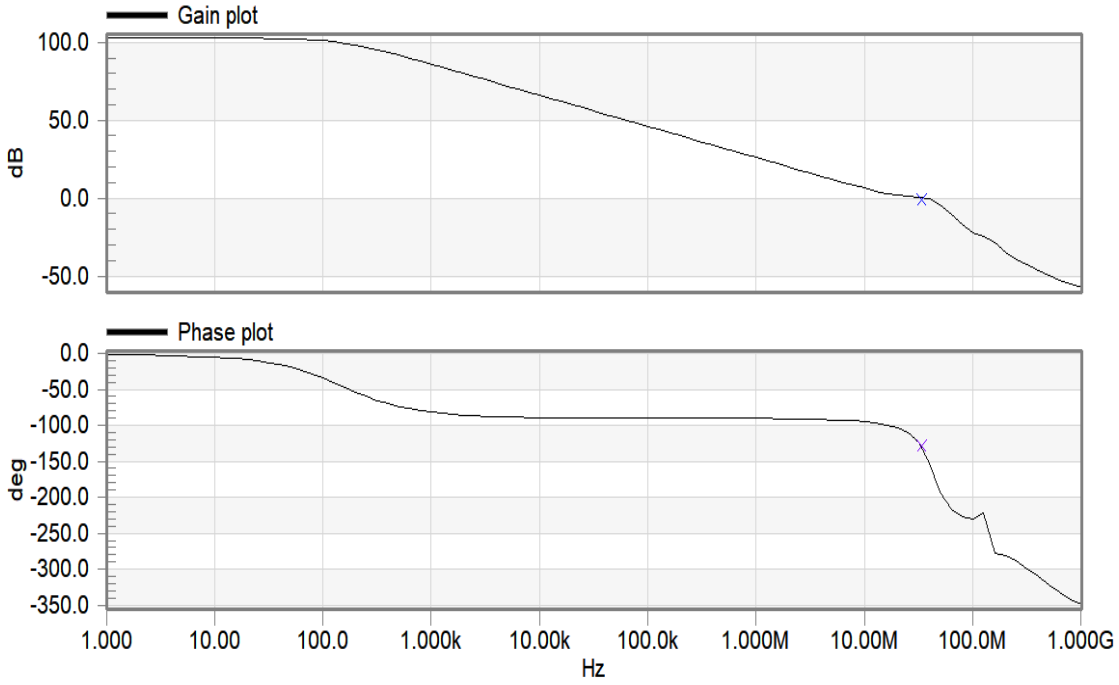


Fig. 4.34 Frequency response of proposed amplifier 5

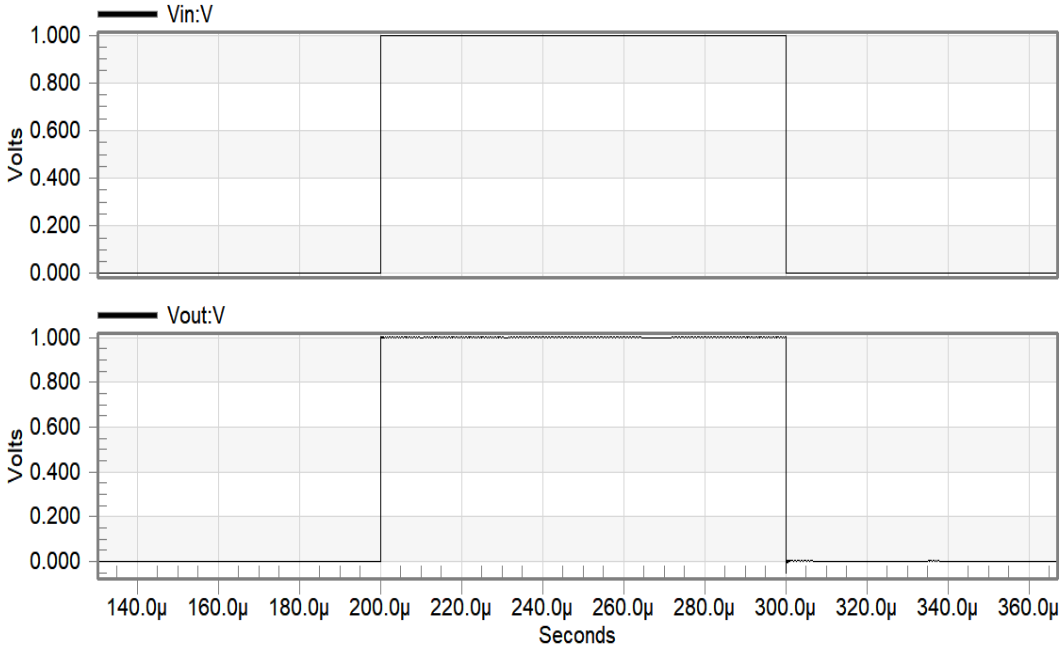


Fig. 4.35 Transient response of proposed amplifier 5

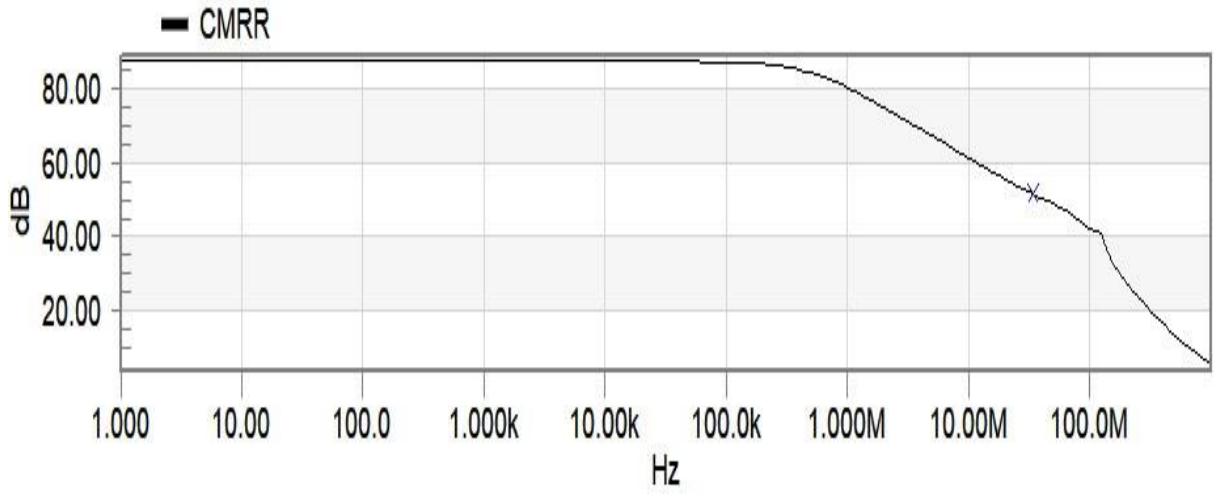


Fig. 4.36 Frequency response of CMRR of proposed amplifier 5

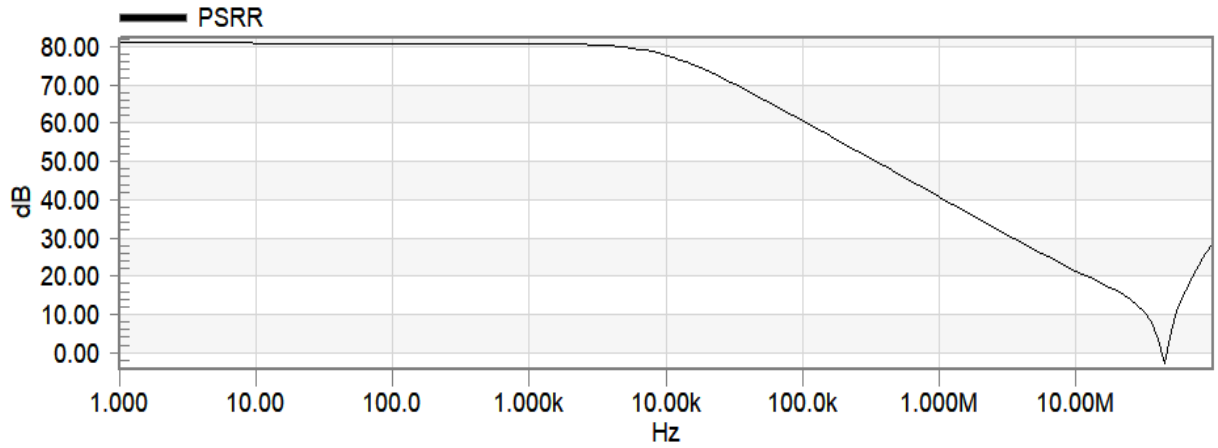


Fig. 4.37 Frequency response of PSRR of proposed amplifier 5

The robustness of the proposed amplifier 5 over process variations is ensured by the process corner analysis, which is displayed in Fig. 4.38. Table 4.8 shows the results for various process corners. It is found that the maximum variations in (Gain, GBW, PM) with respect to TT process corner are within 20%. Figure 4.39 displays the frequency response of the proposed amplifier 5 for the supply voltage variation of ±5%. The corresponding results are included in Table 4.8. The maximum variations in (Gain, GBW, PM) for the proposed amplifier 5 are (0.96%, 15%, 14.8%). So, the overall maximum variation with respect to supply voltage is 15%. Further, Monte-Carlo simulations (100 runs) are carried out for 5% Gaussian distribution of power supply, and the frequency response for the proposed

amplifier 5 is displayed in Fig. 4.40. The (mean, standard deviation) in gain for the proposed amplifier 5 is (105.14 dB, 8.73 dB).

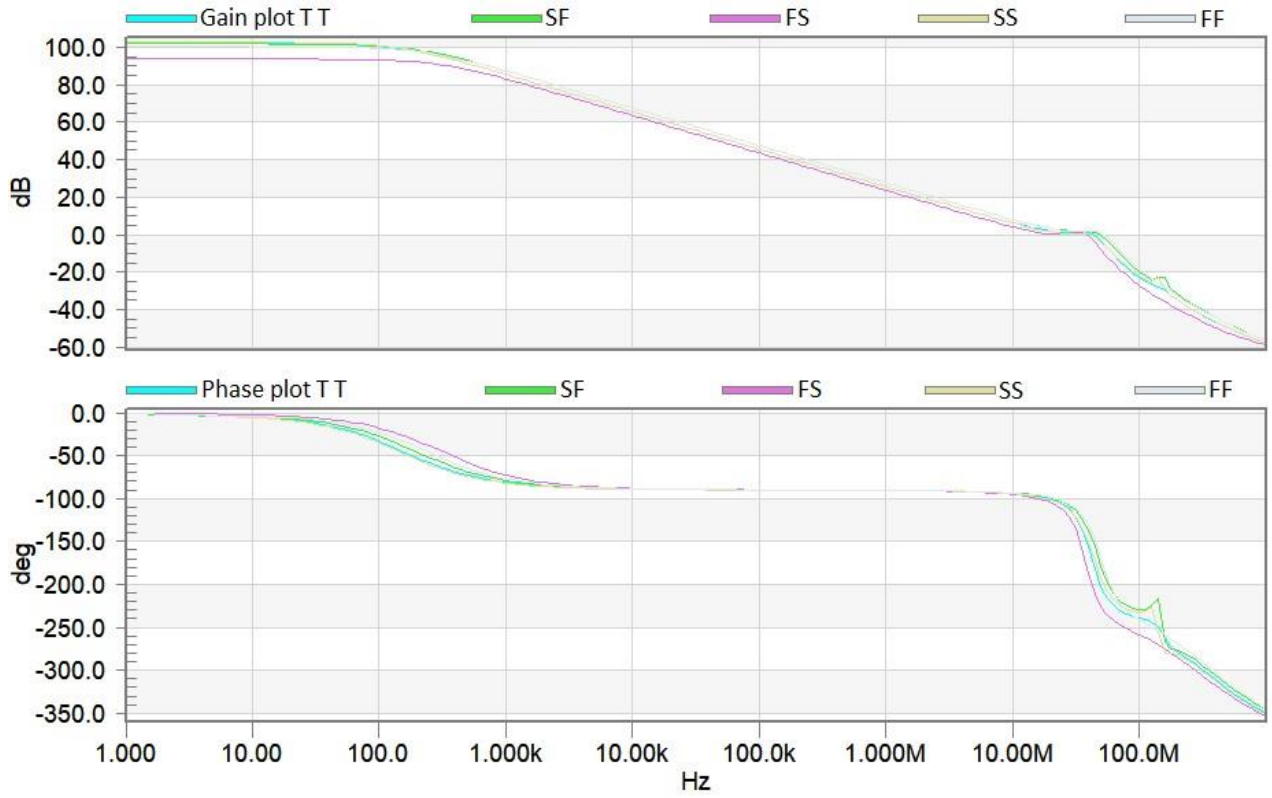


Fig. 4.38 Frequency response of proposed amplifier 5 at different process corners

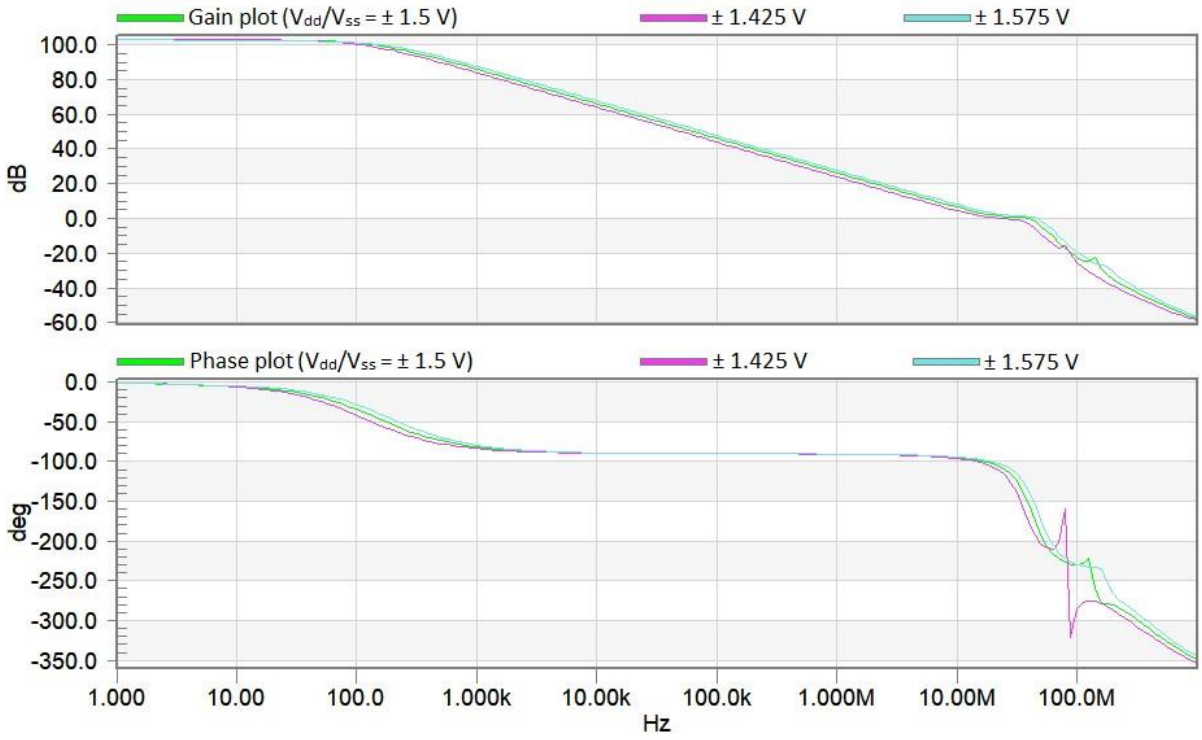


Fig. 4.39 Frequency response of proposed amplifier 5 with variations in supply voltage

Table 4.8 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 5

Performance parameter	Corner					Supply Voltage variation (1.5V ± 5% of 1.5V)	
	TT	SF	FS	SS	FF	1.425V	1.575V
Gain (dB)	104	103.5	94.1	103.5	102	103.4	103
GBW (MHz)	33.8	39.2	31.4	35.5	39.8	30.6	38.3
PM (°)	52	45	46	47	51	46	48

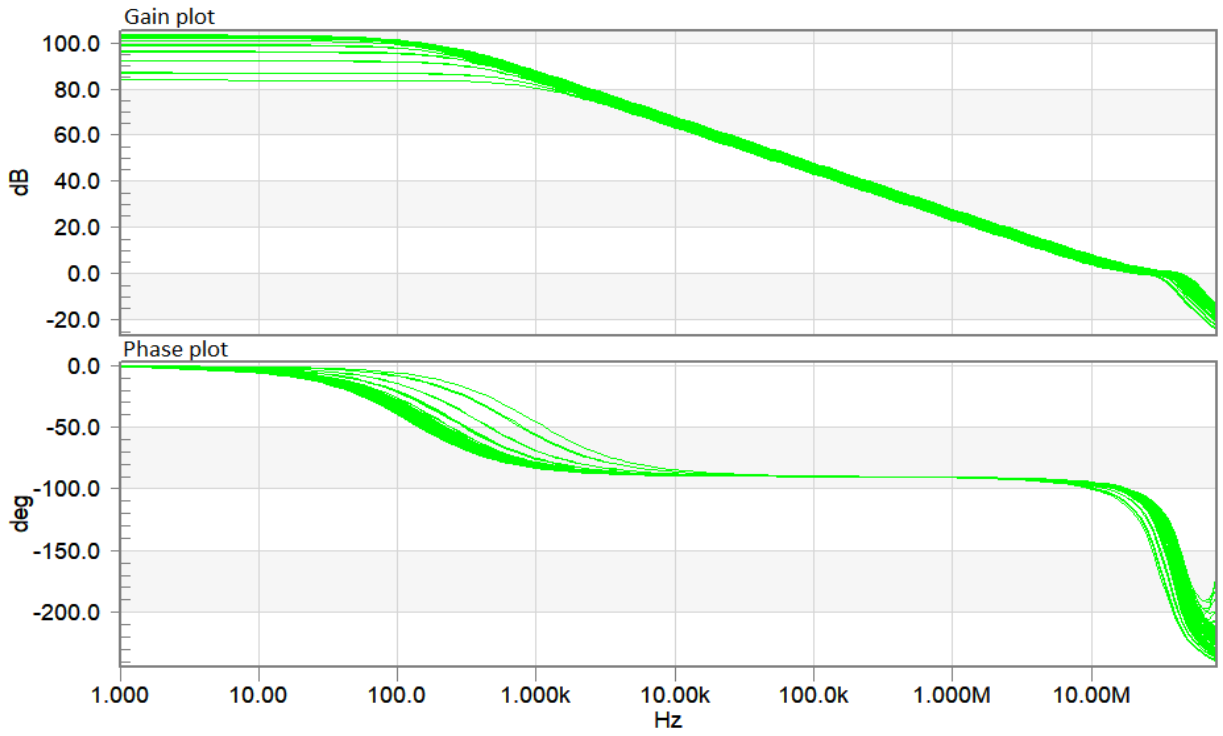


Fig. 4.40 Monte-Carlo analysis for frequency response of the proposed amplifier 5 against supply voltage variations

4.6 Comparison

The proposed amplifiers are compared with their counterparts in Table 4.9. It is clear that the proposed amplifiers offer better GBW than other amplifiers. Further, the proposed amplifiers provide the DC gain of more than 100 dB. Additionally, the phase margin is 60° for the proposed amplifiers 2 and 3, while it is more than 50° for amplifiers 4 and 5. It shows the good stability of the proposed amplifiers. Further, the slew rate is better for the proposed amplifiers than its counterparts. The proposed amplifiers 2 and 3 give the highest slew rate of 10 V/µs. Few of the figure of merits are found to be good. FOM_L of the proposed amplifiers is comparable to Refs. [28-29] and [31], while $IFOM_L$ is better than Refs. [28-29] and [31]. Moreover, $IFOM_S$ of the proposed amplifier 5 is better than Refs. [28, 31].

Table 4.9: Performance comparison of proposed amplifiers 2-5 with their counterparts

Parameters	**[28]**	**[29]**	**[30]**	**[31]**	**Proposed amplifier 2**	**Proposed amplifier 3**	**Proposed amplifier 4**	**Proposed amplifier 5**
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply (V)	1.8	1.8	1.8	1.8	1.5	1.5	1.5	1.5
C_L (pF)	100	100	100	100	100	100	100	100
GBW (MHz)	4.75	14	9.63	9.08	26	30	31.3	33.3
PM (°)	63.3	86	85	83	60	60	50	54
DC Gain (dB)	110	112	115	110	101	101	103	104
Power (mW)	0.32	0.28	0.31	0.54	3.36	3.36	3.46	3.21
SR (V/µS)	1.2	0.8	7.01	2.23	10	10	9.71	9.71
FOM_L (V^{-1})	0.38	0.35	2.26	0.41	0.3	0.3	0.28	0.3
$IFOM_L$	0.7	0.61	5.18	0.73	0.9	0.9	0.84	0.91
FOM_S (Hz.F/W)	1.51	6	3.11	1.65	0.8	0.9	0.9	1.04
$IFOM_S$ (Hz.F/A)	2.72	10.76	5.6	2.97	2.32	2.7	2.72	3.12

4.7 Summary

In this chapter, four amplifiers (proposed amplifiers 2, 3, 4, and 5) are presented, which utilize FFVF in the inner compensation loop of RNMC to resolve the RHP zero problem. Further, the proposed amplifiers 3, 4, and 5 also use a resistor in the outer compensation loop, resulting in double pole-zero cancellation. The push pull output stage is exploited in all proposed amplifiers to

improve the transient response. Additionally, a self cascode structure is employed in the input stage of the proposed amplifier 4 to improve the GBW of the amplifier. The proposed amplifier 5 makes use of the DTMOS structure in the input stage to enhance the GBW. Further, the small signal analysis is performed for all amplifiers to find out the transfer function, which determines the stability and GBW of the amplifiers. The proposed amplifier 5 offers the highest GBW and DC gain of 33.3 MHz and 104 dB, respectively. Moreover, the proposed amplifiers 2 and 3 provide the optimum phase margin of 60°. Additionally, the highest slew rate of 10 V/μs is achieved by the proposed amplifiers 2 and 3. The efficacy of the proposed amplifiers is verified with the help of various simulations, such as corner analysis, supply voltage variation and Monte Carlo analysis.

Chapter 5

Frequency compensation using Active LHP Zero Circuit with Self Cascode structure and DTMOS

5.1 Introduction

In analog design domain, the capacity to drive large capacitive loads is required for many applications. A few of these include LCD drivers, MEMS devices, and low dropout regulators (LDO) [63]. In this context, three-stage amplifiers are beneficial for large capacitive loads in low voltage low power applications.

This chapter presents the proposed amplifiers 6-9 that may be used at higher capacitive load of 1 nF. The proposed amplifiers utilize the active LHP zero circuit at the output of the second stage to cancel the parasitic pole. To resolve the RHP zero problem, a Miller capacitor and resistor are also connected between the output of the third stage and the second stage in the proposed amplifiers 6, 7, and 8, while in the proposed amplifier 9, it is connected between the output of the third stage and the first stage to improve the GBW. The feed forward path is employed in all proposed amplifiers to improve the transient response. Further, the proposed amplifier 6 uses the self cascode structure in the first stage, while a self cascode with DTMOS is utilized in the first stage of the proposed amplifier 7. A modified self cascode structure is employed in the first stage of the proposed amplifiers 8 and 9.

The organization of this chapter is as follows: Section 5.2 discusses the proposed amplifier 6 with its small signal analysis and simulation results. The circuit description, small signal analysis, and simulation results of the proposed amplifier 7 are given in Section 5.3. Further, Section 5.4 describes the proposed amplifier 8. The small signal analysis and simulation results of the proposed amplifier 8 are also included in Section 5.4. The proposed amplifier 9 is presented in Section 5.5 with its small signal analysis and simulation results. The performance of the proposed amplifiers 6-9 is compared in Section 5.6. Finally, the chapter is concluded in Section 5.7.

5.2 Proposed amplifier 6

The block diagram of the proposed amplifier 6 is shown in Fig. 5.1. It employs a cascade of three gain stages. An active LHP zero block is placed at the output of the second stage. The active LHP zero block cancels the parasitic pole of this particular stage. A Miller capacitor C_m and resistor R_m are connected in a feedback loop between the output of the third stage and the second stage to overcome the RHP zero problem. The input stage consists of the self cascode structure. The third stage is an inverting amplifier to comply with the condition of negative gain in the Miller loop. Further, a push pull output stage has been realized by employing an additional feed forward stage.

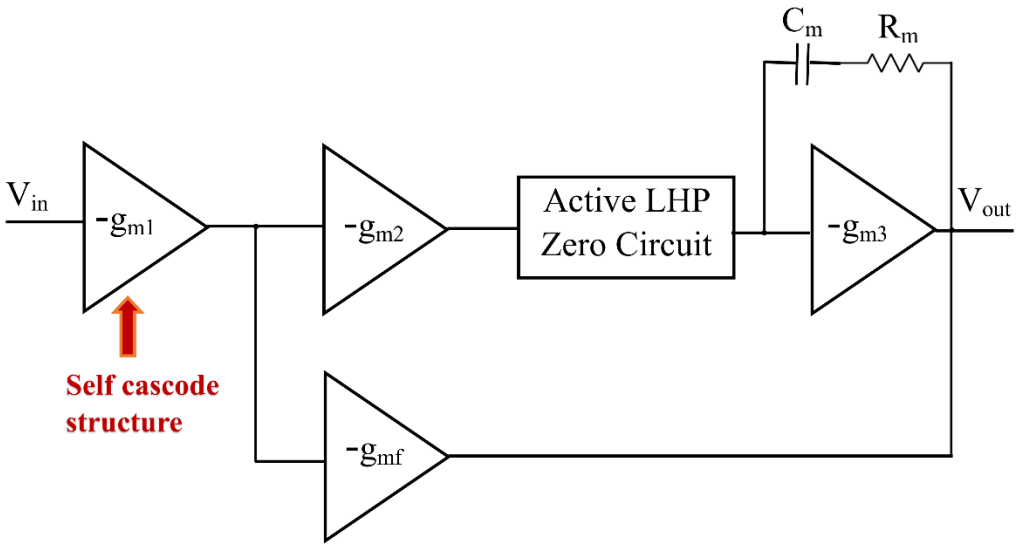


Fig. 5.1 Block diagram of proposed amplifier 6

5.2.1 Circuit description of proposed amplifier 6

Figure 5.2 shows the transistor level schematic of the proposed amplifier 6. Transistors M1-M6 with a current source (I) constitute a differential amplifier which is the first stage. Self cascode structure (M1-M2, M3-M4); current mirror load (M5-M6) and a current source (I) form the differential amplifier. The transistor M7 is employed as a common source amplifier. Moreover, an active LHP zero circuit (transistors M8-M9; resistor R_z, and capacitor C_z) is connected in the second stage. Here, transistor M10 acts as a current source. The third stage is again a common source amplifier (M11-M12). The transistor M12 implements the push pull output stage and improves the large signal performance.

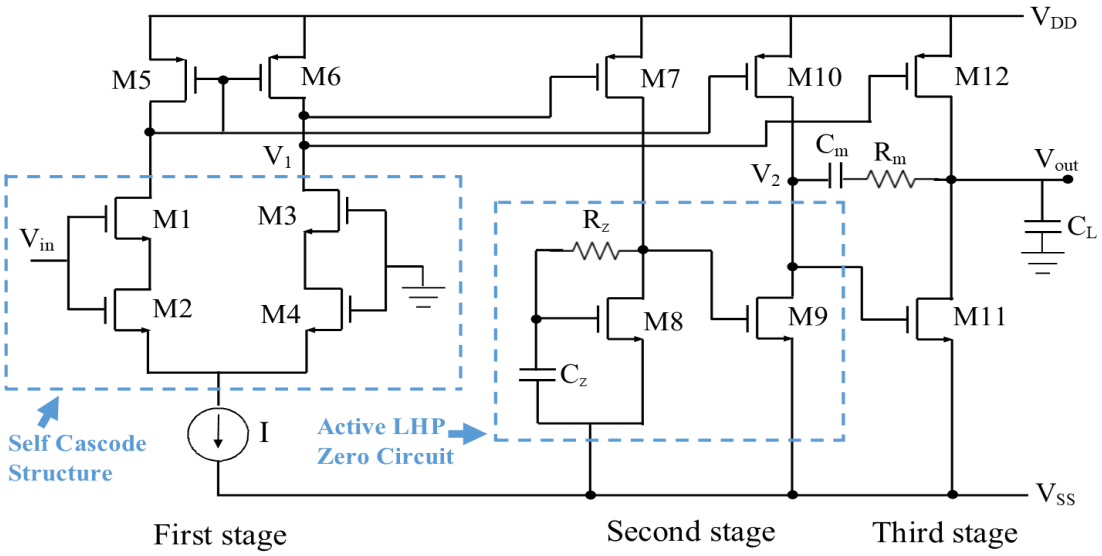


Fig. 5.2 Transistor level implementation of proposed amplifier 6

5.2.2. Small signal analysis of proposed amplifier 6

The small signal model of the proposed amplifier 6 is shown in Fig. 5.3. Let the (transconductance, output resistance and capacitance) of first, second and third stage be represented as (g_{m1}, r_{o1}, C_1), (g_{m2}, r_{o2}, C_2) and (g_{m3}, r_{o3}, C_L).

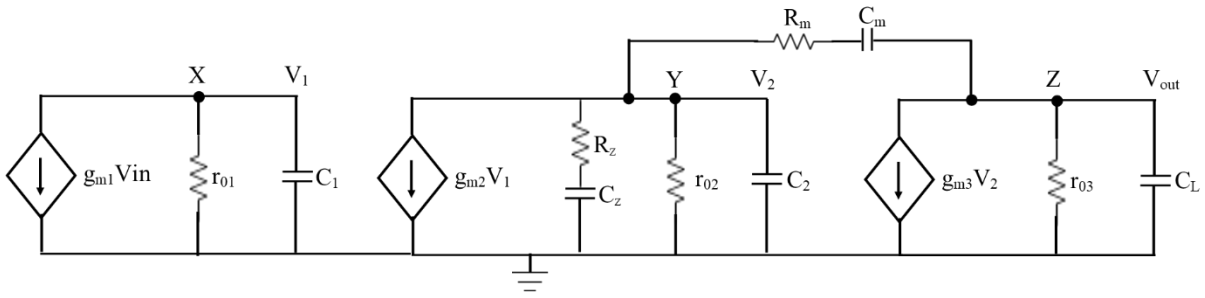


Fig. 5.3 Small signal model of proposed amplifier 6

To simplify the small signal analysis, following assumption is made:

$$g_{m1}r_{o1} >> 1,\ g_{m2}r_{o2} >> 1,\ g_{m3}r_{o3} >> 1 \tag{5.1}$$

and following transfer function is obtained for the proposed amplifier 6,

$$A(s) = \frac{A_{dc}(1+sC_mR_m)}{1 + a_1s + b_1s^2 + c_1s^3 + d_1s^4} \tag{5.2}$$

where A_{dc} is the low frequency gain of proposed amplifier 6 and is given by,

$$A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3} \tag{5.3}$$

and the coefficients a_1, b_1, c_1 and d_1 are given by Eqs. 5.4-5.7.

$$a_1 = C_L r_{o3} + C_m r_{o2} g_{m3} r_{o3} + C_z r_{o2} + C_1 r_{o1} + C_m(R_m + r_{o2}) \tag{5.4}$$

$$b_1 = C_L C_m r_{o2} r_{o3} + C_m C_1 g_{m3} r_{o1} r_{o2} r_{o3} + C_L r_{o3}(C_1 r_{o1} + C_2 r_{o2}) \tag{5.5}$$

$$c_1 = C_L C_m R_m r_{o3}(C_1 r_{o1} + C_2 r_{o2}) + C_L C_1 r_{o1} r_{o2} r_{o3}(C_m + C_2) \tag{5.6}$$

$$d_1 = C_m C_1 C_2 R_m r_{o1} r_{o2} \tag{5.7}$$

Eq. 5.2 contains a dominant pole ω_{P1}, three non-dominant poles ω_{P2}, $\omega_{P3,}$ ω_{P4} and one LHP zero ω_z, which are given by Eqs. 5.8-5.12.

$$\omega_{p1} = \frac{1}{C_L r_{o3} + C_m r_{o2} g_{m3} r_{o3} + C_z r_{o2} + C_1 r_{o1} + C_m(R_m + r_{o2})} \tag{5.8}$$

$$\omega_{p2} = \frac{C_L r_{o3} + C_m r_{o2} g_{m3} r_{o3} + C_z r_{o2} + C_1 r_{o1} + C_m(R_m + r_{o2})}{C_L C_m r_{o2} r_{o3} + C_m C_1 g_{m3} r_{o1} r_{o2} r_{o3} + C_L r_{o3}(C_1 r_{o1} + C_2 r_{o2})} \tag{5.9}$$

$$\omega_{p3} = \frac{C_L C_m r_{o2} r_{o3} + C_m C_1 g_{m3} r_{o1} r_{o2} r_{o3} + C_L r_{o3}(C_1 r_{o1} + C_2 r_{o2})}{C_L C_m R_m r_{o3}(C_1 r_{o1} + C_2 r_{o2}) + C_L C_1 r_{o1} r_{o2} r_{o3}(C_m + C_2)} \tag{5.10}$$

$$\omega_{p4} = \frac{C_L C_m R_m r_{o3}(C_1 r_{o1} + C_2 r_{o2}) + C_L C_1 r_{o1} r_{o2} r_{o3}(C_m + C_2)}{C_m C_1 C_2 R_m r_{o1} r_{o2}} \tag{5.11}$$

$$\omega_z = \frac{1}{R_m C_m} \tag{5.12}$$

The GBW can be represented as the product of DC gain and the dominant pole frequency and is given by Eq. 5.13.

$$GBW = A_{dc.}\omega_{p1} = \frac{g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3}}{C_L r_{o3} + C_m r_{o2} g_{m3} r_{o3} + C_z r_{o2} + C_1 r_{o1} + C_m(R_m + r_{o2})} \tag{5.13}$$

It is evident that the RHP pole does not exist for the proposed amplifier 6, therefore, it is unconditionally stable. Moreover, the proposed amplifier 6 does not have any RHP zero, which signifies that the proposed amplifier is highly stable. We can improve the stability of the system

by enhancing the phase margin, but it slows down the time response. In this context, the optimum value of PM is considered as 60 degrees [2].

5.2.3 Simulation results and discussions

The functionality of the proposed amplifier 6 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 6 is enlisted in Table 5.1.

Table 5.1 Design parameters of proposed amplifier 6

Parameters	Value
Transistor dimensions	M1, M3: W/L = 1.5 µm/1 µm M2, M4: W/L = 0.75 µm/1 µm M5, M6: W/L = 3.9 µm/1 µm M7, M10: W/L = 3.1 µm/1 µm M8, M9, M11: W/L = 1.6 µm/0.6 µm M12: W/L = 2.9 µm/1 µm
R_m, Rz	1 kΩ, 500 kΩ
C_m, Cz, C_L	1 fF, 50 fF, 1 nF
Biasing current (I)	50 µA

The frequency response of the proposed amplifier 6 is placed in Fig. 5.4. The GBW of 4.8 MHz is observed for the proposed amplifier 6. The phase margin is found to 62° and is indicative of good stability. The DC gain is more than 80 dB. The unity gain step response of the proposed amplifier 6 is observed, and is depicted in Fig. 5.5. The slew rate and 1 % settling time are found to be 0.1 V/µs and 2.5 µs, respectively. The frequency response of CMRR is shown in Fig. 5.6. The CMRR is found to be 225 dB for the proposed amplifier 6. The PSRR plot is displayed in Fig. 5.7. It can be checked that the PSRR for the proposed amplifier 6 is 84.4 dB.

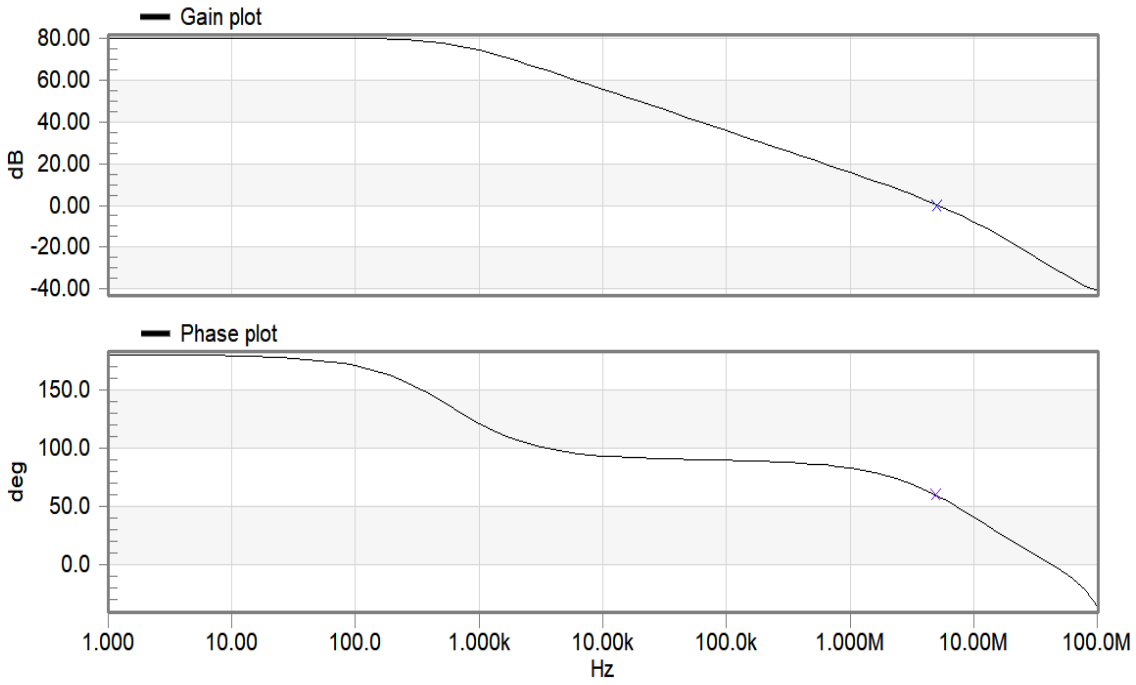


Fig. 5.4 Frequency response of proposed amplifier 6

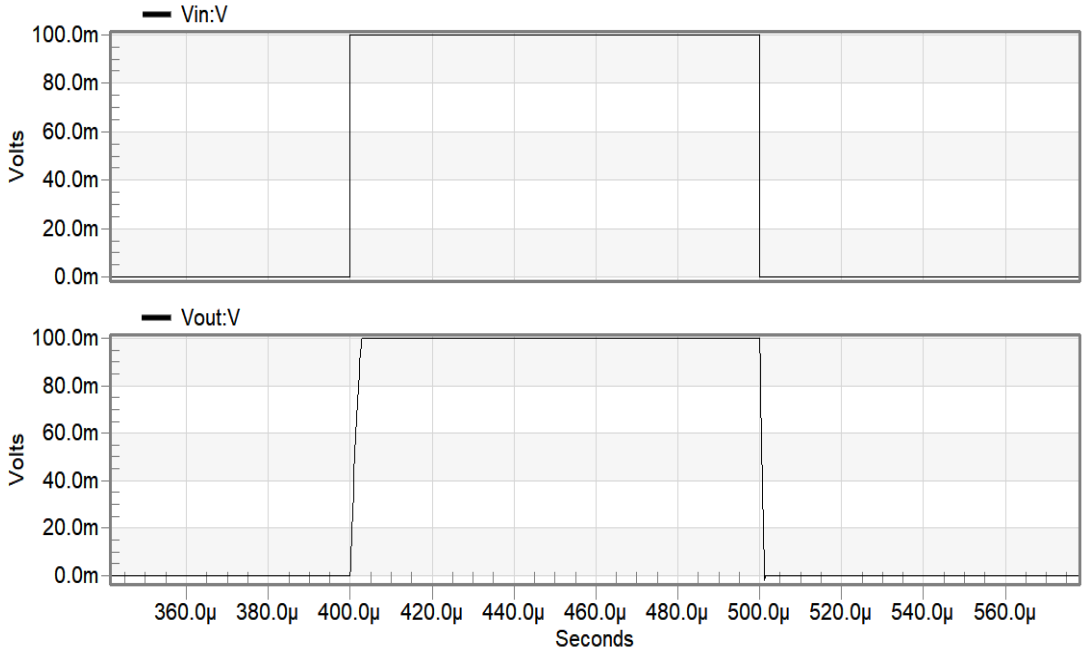


Fig. 5.5 Transient response of proposed amplifier 6

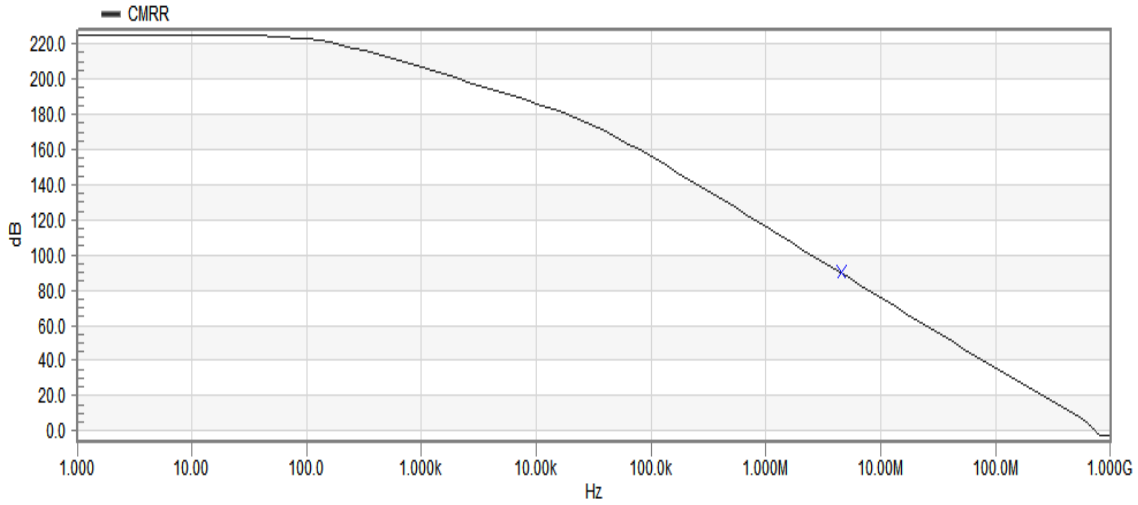


Fig. 5.6 Frequency response of CMRR for proposed amplifier 6

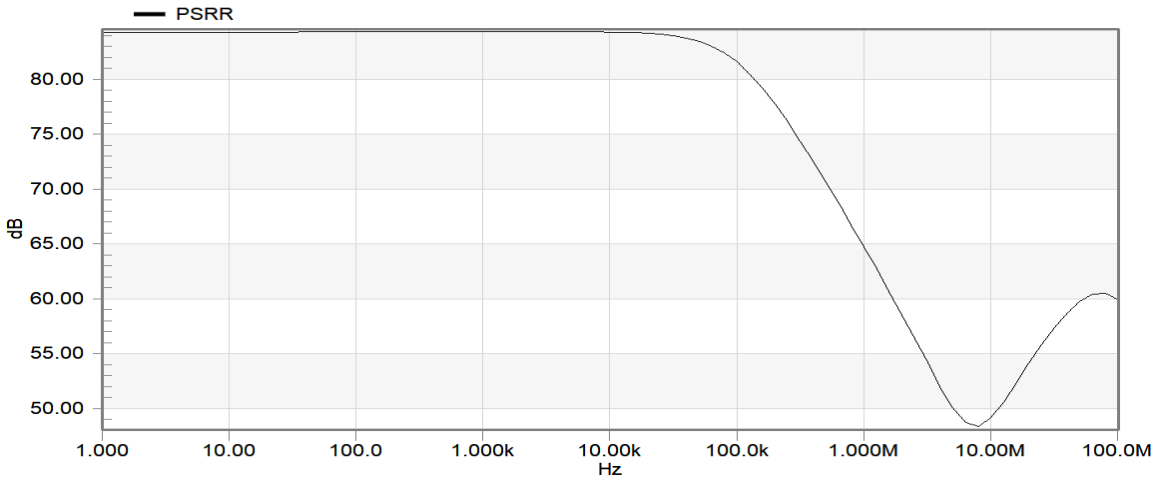


Fig. 5.7 Frequency response of PSRR for proposed amplifier 6

To examine the impact of process variations on gain, GBW and PM, corner analysis is performed. The findings are presented and comprehended in Fig. 5.8 and Table 5.2 respectively. It is noted that the maximum deviations in gain, GBW, and PM are within 25%, except for FS process corner, for which variations in GBW and PM are higher. Deviations are calculated with reference to TT process corner. To assess the performance of the proposed amplifier 6 with supply voltage variation of ±2.5%, the frequency response has been checked (Fig. 5.9), and the results are placed in Table 5.2. The maximum variations in gain, GBW, and PM are observed to be 2.47%, 20.8% and 17.9% respectively. This results in a maximum total variation of 20.8% with reference to the supply voltage. Additionally, Monte-Carlo simulations are performed for a power supply with an 8% Gaussian distribution (200 runs), and the frequency response for the proposed amplifier 6 is

depicted in Fig. 5.10. The proposed amplifier 6 offers the (mean, standard deviation) in gain as (78.8 dB, 11.4 dB).

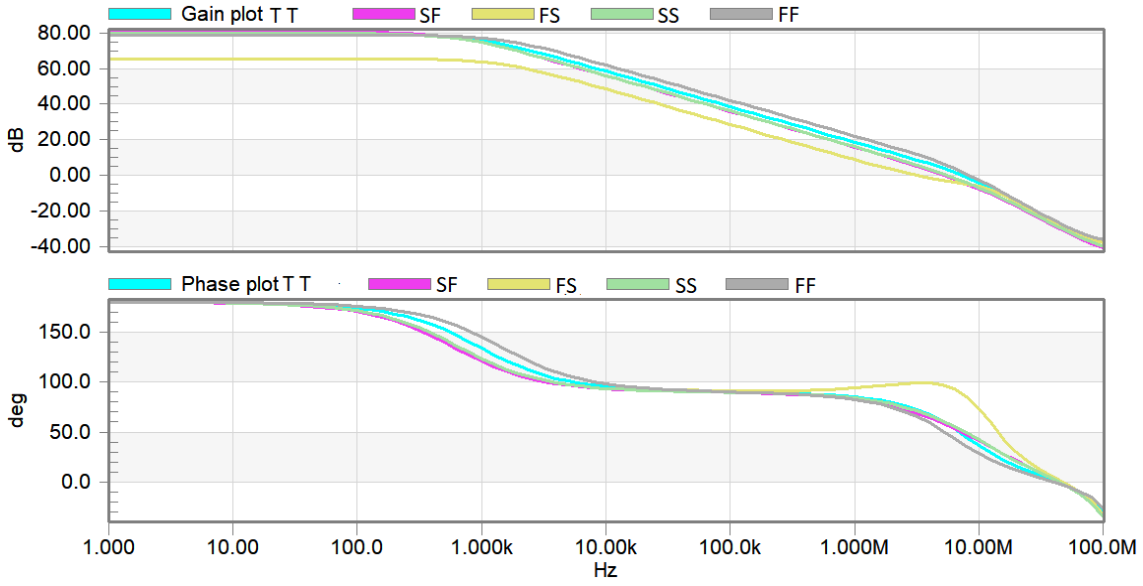


Fig. 5.8 Frequency response of proposed amplifier 6 at different corners

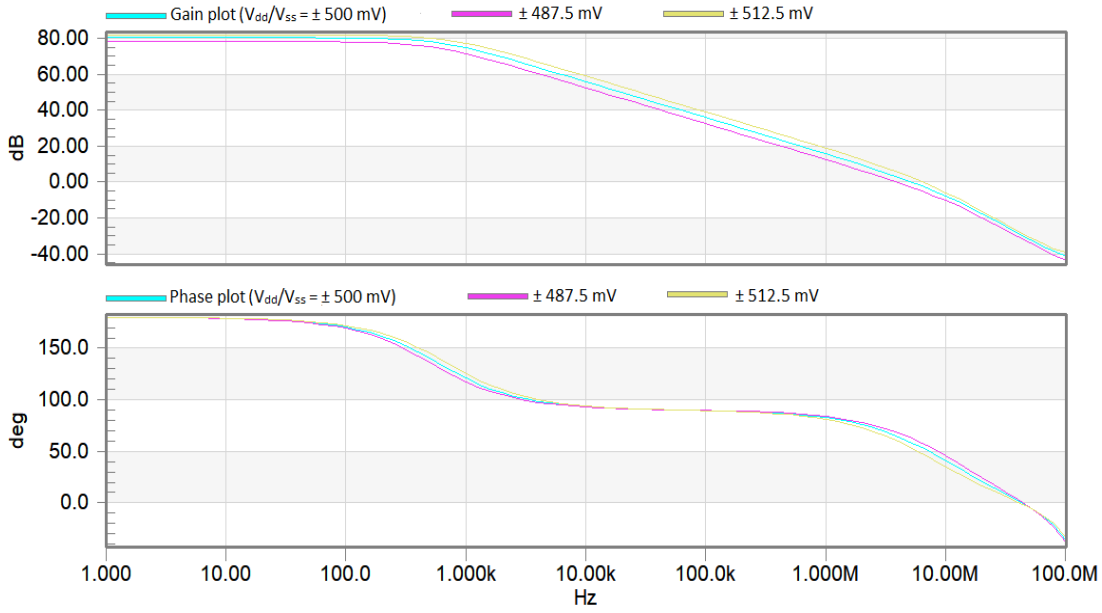


Fig. 5.9 Frequency response of proposed amplifier 6 against variations in supply voltage

Table 5.2 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 6

AC response metrics	Process Corner					V_{DD} variation (500 mV ± 2.5% of 500 mV)	
	TT	SF	FS	SS	FF	487.5 mV	512.5 mV
Gain (dB)	79.8	81.4	66.1	80.6	79.7	79	82.7
GBW (MHz)	6.6	5	3.1	5.2	7.6	4.2	5.8
PM (°)	52.7	61.8	99	61.4	39.6	67.6	50.9

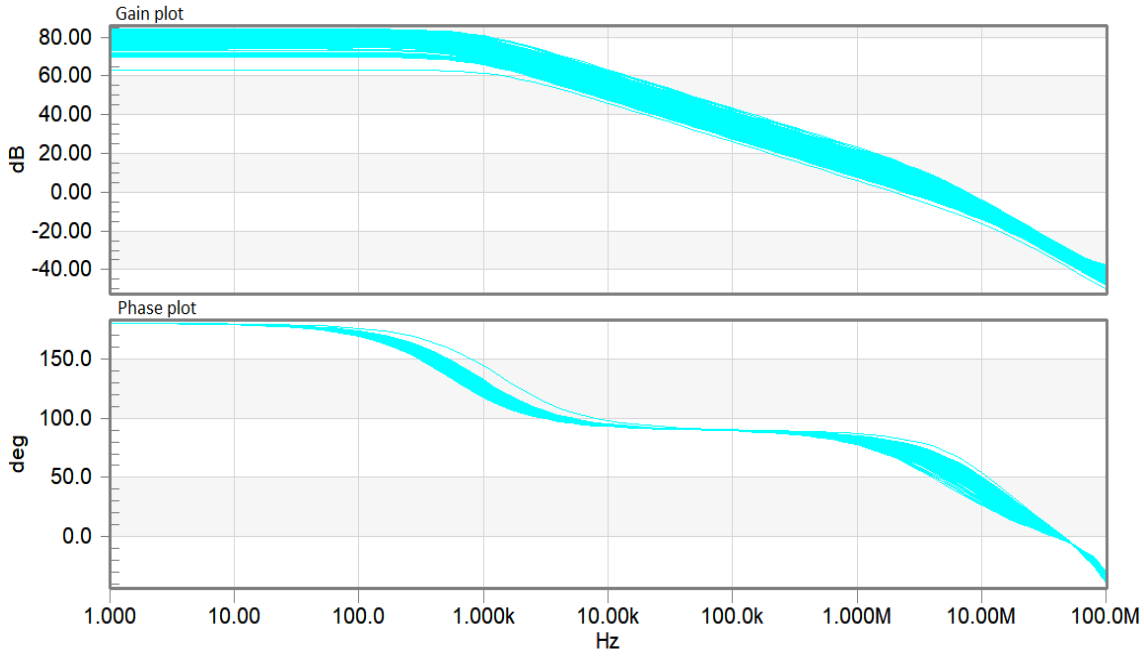


Fig. 5.10 Monte-Carlo simulation for gain and phase response of the proposed amplifier 6 with V_{DD} deviations

5.3 Proposed amplifier 7

Figure 5.11 depicts the block diagram of the proposed amplifier. In this amplifier, an active LHP zero block is placed at the output of the second stage to cancel the parasitic pole of this particular stage. A Miller capacitor C_m and resistor R_m are connected in a feedback loop between the output of the third stage and the second stage to address the RHP zero problem. The first stage includes the self cascode structure with DTMOS transistor. The third stage is an inverting amplifier to comply with the condition of negative gain in the Miller loop. Further, a feed forward path is utilized to enhance the transient response.

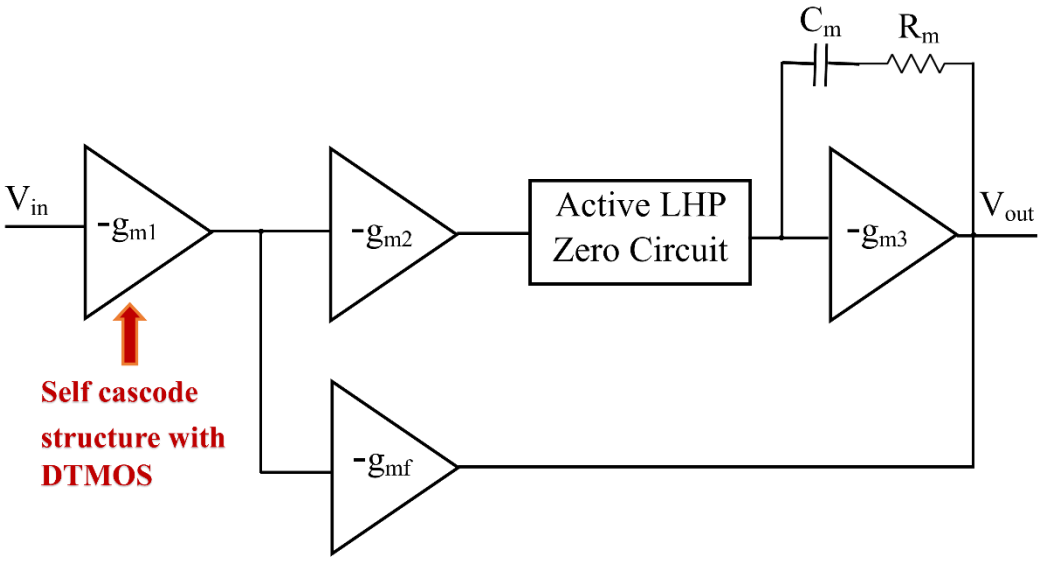


Fig. 5.11 Block diagram of proposed amplifier 7

5.3.1 Circuit description of proposed amplifier 7

Figure 5.12 manifests the transistor level schematic of the proposed amplifier 7. It uses dynamically body biased self cascode structure in the first stage to have better transconductance and output resistance to improve the GBW of the amplifier. Transistors M1-M2 and M3-M4 form the self cascode structure. Moreover, the transistors M1 and M3 are DTMOS. The input stage is comprised of the transistors M1-M6 with a current source (I). The transistor M7 is employed as a common source amplifier. Moreover, an active LHP zero circuit (transistors M8-M9; resistor R_z, and capacitor C_z) is connected in the second stage. Here, transistor M10 acts as a current source. The third stage is again a common source amplifier (M11-M12). The transistor M12 implements the push pull output stage and improves the large signal performance.

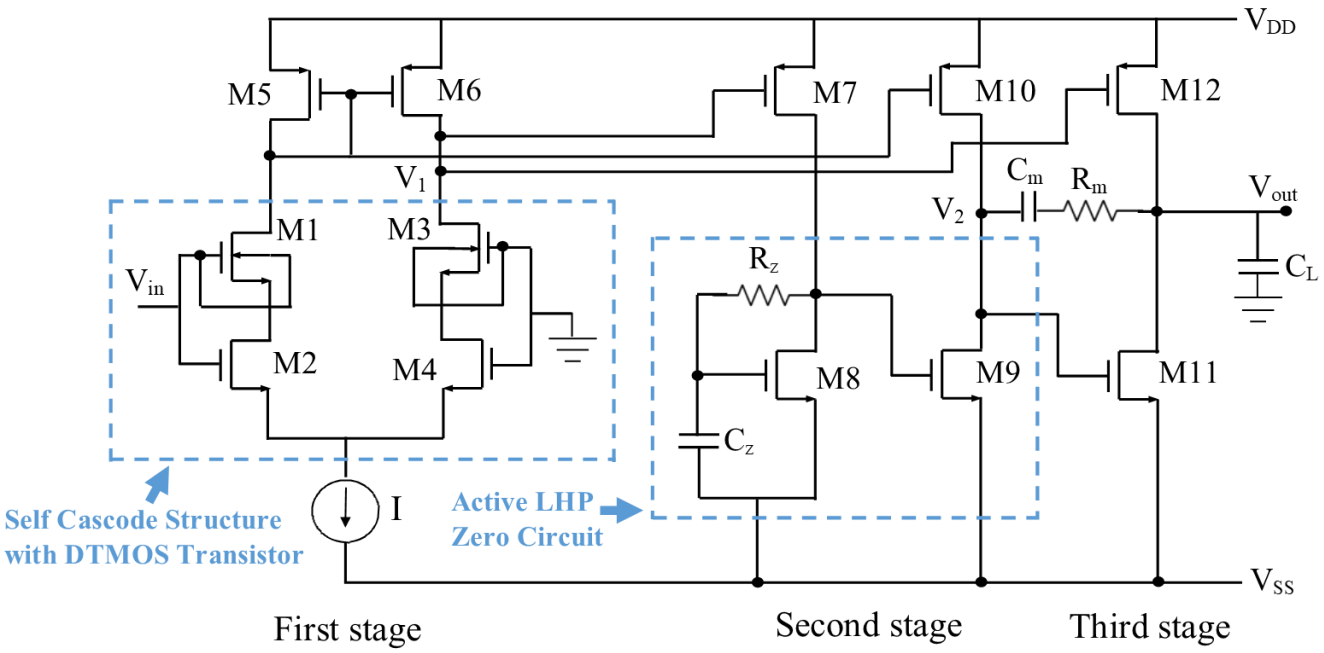


Fig. 5.12 Transistor level implementation of proposed amplifier 7

5.3.2 Small signal analysis of proposed amplifier 7

Figure 5.13 describes the small signal model of the proposed amplifier 7. Let the (transconductance, output resistance and capacitance) of first, second and third stage be represented as (g_{m1D}, r_{o1D}, C_{1D}), (g_{m2D}, r_{o2D}, C_{2D}) and (g_{m3D}, r_{o3D}, C_L).

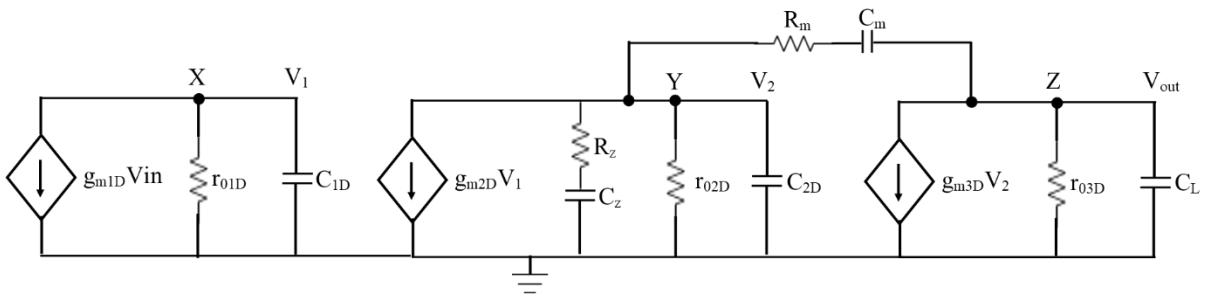


Fig. 5.13 Small signal model of proposed amplifier 7

To simplify the small signal analysis, following assumption is made:

$$g_{m1D}r_{o1D} >> 1,\ g_{m2D}r_{o2D} >> 1,\ g_{m3D}r_{o3D} >> 1 \qquad (5.14)$$

and following transfer function is obtained for the proposed amplifier 7,

$$A(s) = \frac{A_{dc}(1+sC_mR_m)}{1 + a_2s + b_2s^2 + c_2s^3 + d_2s^4} \quad (5.15)$$

where A_{dc} is the low frequency gain of proposed amplifier 7 and is given by,

$$A_{dc} = g_{m1D}r_{o1D}g_{m2D}r_{o2D}g_{m3D}r_{o3D} \quad (5.16)$$

and the coefficients a_2, b_2, c_2 and d_2 are given by Eqs. 5.17-5.20.

$$a_2 = C_Lr_{o3D} + C_mr_{o2D}g_{m3D}r_{o3D} + C_zr_{o2D} + C_{1D}r_{o1D} + C_m(R_m + r_{o2D}) \quad (5.17)$$

$$b_2 = C_LC_mr_{o2D}r_{o3D} + C_mC_{1D}g_{m3D}r_{o1D}r_{o2D}r_{o3D} + C_Lr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D}) \quad (5.18)$$

$$c_2 = C_LC_mR_mr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D}) + C_LC_{1D}r_{o1D}r_{o2D}r_{o3D}(C_m + C_{2D}) \quad (5.19)$$

$$d_2 = C_mC_{1D}C_{2D}R_mr_{o1D}r_{o2D} \quad (5.20)$$

Eq. 5.15 contains a dominant pole ω_{P1}, three non-dominant poles ω_{P2}, $\omega_{P3,}$ ω_{P4} and one LHP zero ω_z, which are given by Eqs. 5.21-5.25.

$$\omega_{p1} = \frac{1}{C_Lr_{o3D} + C_mr_{o2D}g_{m3D}r_{o3D} + C_zr_{o2D} + C_{1D}r_{o1D} + C_m(R_m + r_{o2D})} \quad (5.21)$$

$$\omega_{p2} = \frac{C_Lr_{o3D} + C_mr_{o2D}g_{m3D}r_{o3D} + C_zr_{o2D} + C_{1D}r_{o1D} + C_m(R_m + r_{o2D})}{C_LC_mr_{o2D}r_{o3D} + C_mC_{1D}g_{m3D}r_{o1D}r_{o2D}r_{o3D} + C_Lr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D})} \quad (5.22)$$

$$\omega_{p3} = \frac{C_LC_mr_{o2D}r_{o3D} + C_mC_{1D}g_{m3D}r_{o1D}r_{o2D}r_{o3D} + C_Lr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D})}{C_LC_mR_mr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D}) + C_LC_{1D}r_{o1D}r_{o2D}r_{o3D}(C_m + C_{2D})} \quad (5.23)$$

$$\omega_{p4} = \frac{C_LC_mR_mr_{o3D}(C_{1D}r_{o1D} + C_{2D}r_{o2D}) + C_LC_{1D}r_{o1D}r_{o2D}r_{o3D}(C_m + C_{2D})}{C_mC_{1D}C_{2D}R_mr_{o1D}r_{o2D}} \quad (5.24)$$

$$\text{LHP zero } (\omega_{z1}) = \omega_z = \frac{1}{R_mC_m} \quad (5.25)$$

The GBW can be represented as the product of DC gain and dominant pole, which is given by Eq. 5.26.

$$GBW = A_{dc.}\omega_{p1} = \frac{g_{m1D}r_{o1D}g_{m2D}r_{o2D}g_{m3D}r_{o3D}}{C_Lr_{o3D} + C_mr_{o2D}g_{m3D}r_{o3D} + C_zr_{o2D} + C_{1D}r_{o1D} + C_m(R_m + r_{o2D})} \quad (5.26)$$

It is clear that the proposed amplifier 7 does not offer any RHP pole; therefore, it is unconditionally stable. Moreover, the proposed amplifier 7 does not have any RHP zero, which signifies that the proposed amplifier is highly stable.

5.3.3 Simulation results and discussions

The functionality of the proposed amplifier 7 is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool. The design parameters of the proposed amplifier 7 is tabulated in Table 5.4.

Table 5.3 Design parameters of proposed amplifier 7

Parameters	Value
Transistor dimensions	M1, M3: W/L = 1.5 µm/1 µm M2, M4: W/L = 0.75 µm/1 µm M5, M6: W/L = 3.9 µm/1 µm M7, M10: W/L = 3.1 µm/1 µm M8, M9, M11: W/L = 1.6 µm/0.6 µm M12: W/L = 2.9 µm/1 µm
R_m, Rz	1 kΩ, 500 kΩ
C_m, Cz, C_L	1 fF, 50 fF, 1 nF
Biasing current (I)	50 µA

The frequency response of the proposed amplifier 7 is depicted in Fig. 5.14. The GBW is 5.2 MHz, and the phase margin is 60°, which is indicative of good stability. Further, the DC gain is more than 80 dB. The unity gain step response of the proposed amplifier 7 is shown in Fig. 5.15. The slew rate and 1 % settling time are found as 0.1 V/µs and 2.5 µs, respectively. The frequency response of CMRR for the proposed amplifier 7 is displayed in Fig. 5.16. The CMRR is found as 236 dB for the proposed amplifier 7. The PSRR plot is shown in Fig. 5.17. It can be checked that the PSRR is 84.8 dB for the proposed amplifier 7.

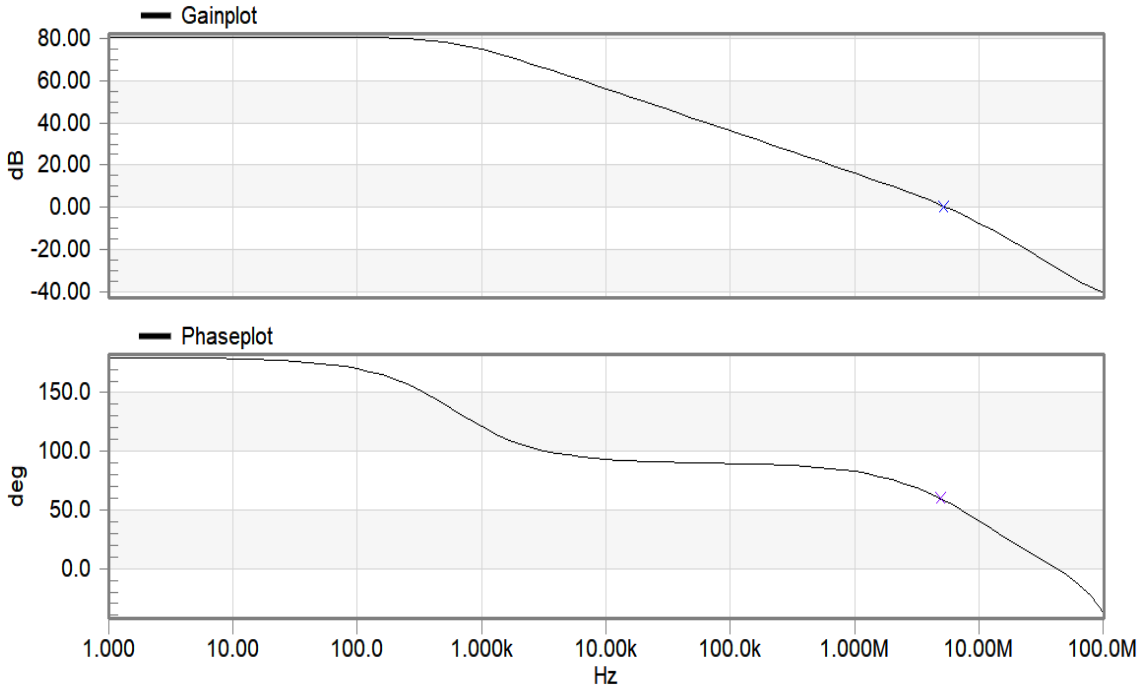


Fig. 5.14 Frequency response of proposed amplifier 7

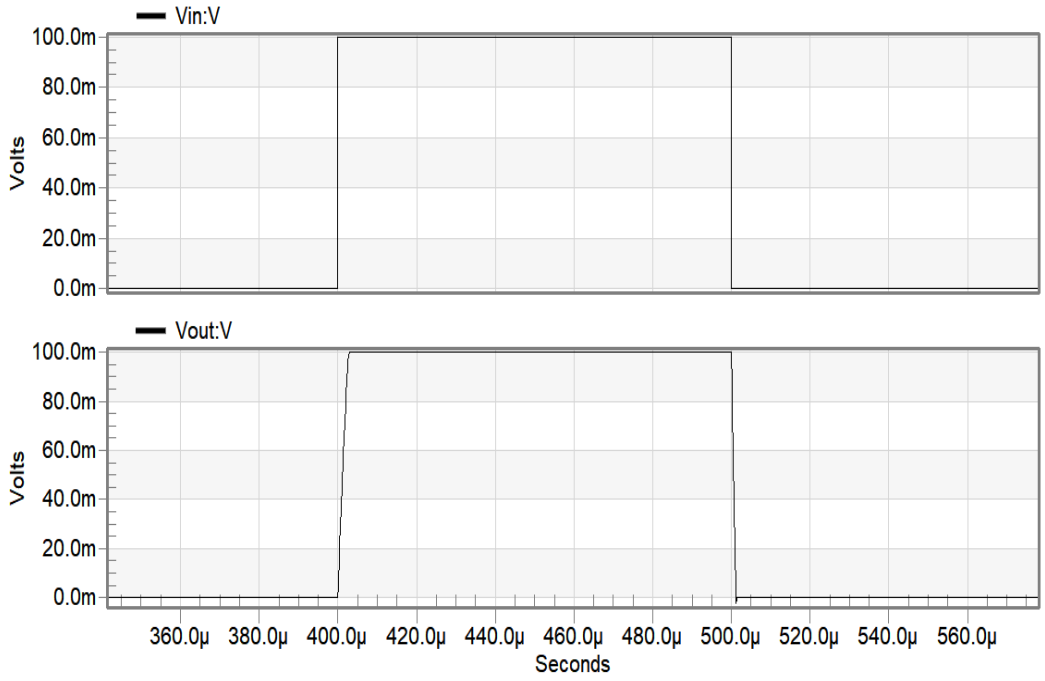


Fig. 5.15 Transient response of proposed amplifier 7

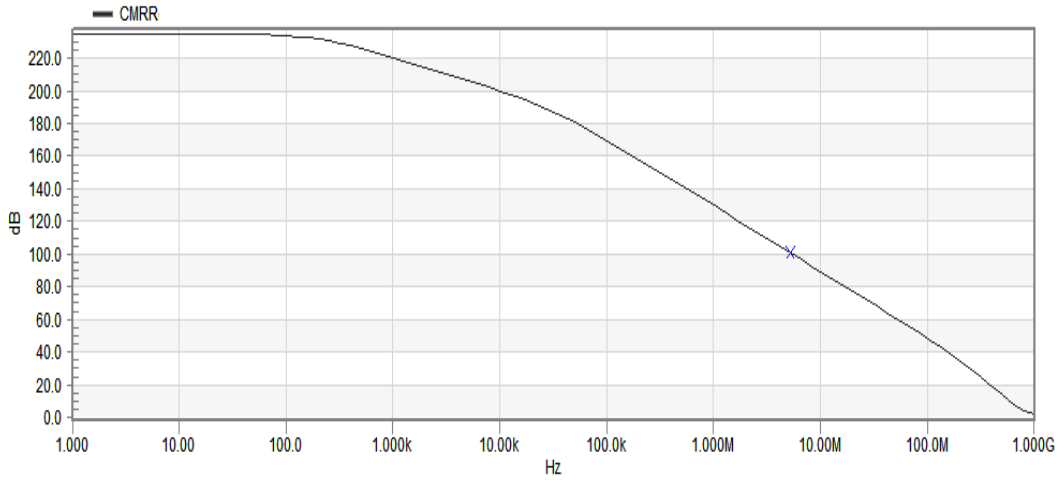


Fig. 5.16 Frequency response of CMRR for proposed amplifier 7

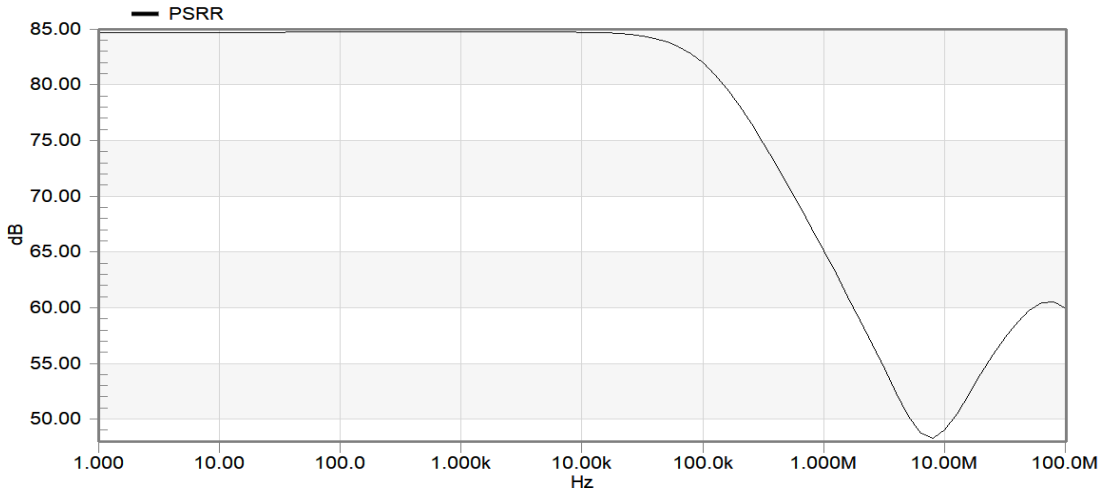


Fig. 5.17 Frequency response of PSRR for proposed amplifier 7

The corner analysis of the proposed amplifier 7 is performed to investigate the impact of process variations (Fig. 5.18). Table 5.4 reveals that the maximum deviations in gain, GBW, and PM are within 25%, except for FS process corner, for which variations in GBW and PM are higher. Deviations are calculated with reference to TT process corner. To assess the performance of the proposed amplifier 7 with supply voltage variation of ±2.5%, the frequency response has been checked (Fig. 5.19), and results are tabulated in Table 5.4. The proposed amplifier 7 has maximum variations in gain, GBW, and PM of 3.2%, 19.2%, 17% respectively. This results in a maximum total variation of 19.2 % with reference to supply voltage. Additionally, Monte-Carlo simulations are performed for a power supply

with an 8% Gaussian distribution (200 runs), and the frequency response for the proposed amplifier 7 is depicted in Fig. 5.20. The proposed amplifier 7 offers the (mean, standard deviation) in gain as (80.32 dB, 11.4 dB).

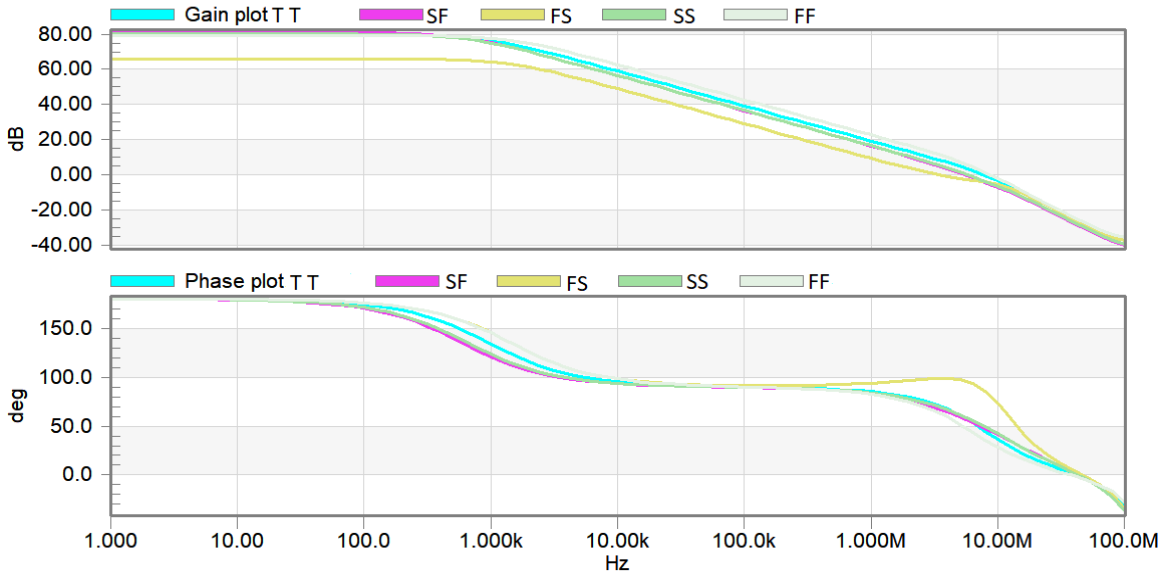


Fig. 5.18 Frequency response of proposed amplifier 7 at different process corners

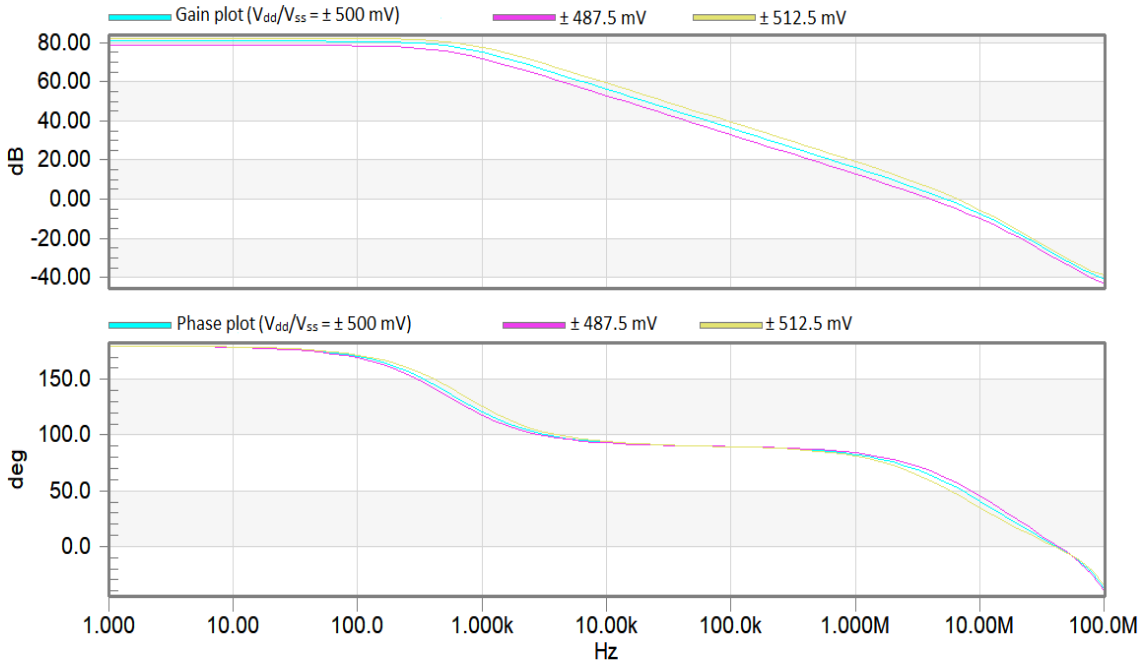


Fig. 5.19 Frequency response of proposed amplifier 7 against variations in supply voltage

Table 5.4 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 7

AC response metrics	Process Corner					V_{DD} variation (500 mV ± 2.5% of 500 mV)	
	TT	SF	FS	SS	FF	487.5 mV	512.5 mV
Gain (dB)	80.3	81.8	66.6	81	80.2	79.4	83.1
GBW (MHz)	7.1	5.7	3.6	6.1	8.2	4.3	6.2
PM (°)	50	56.2	98.8	56.7	37.6	67.7	49.8

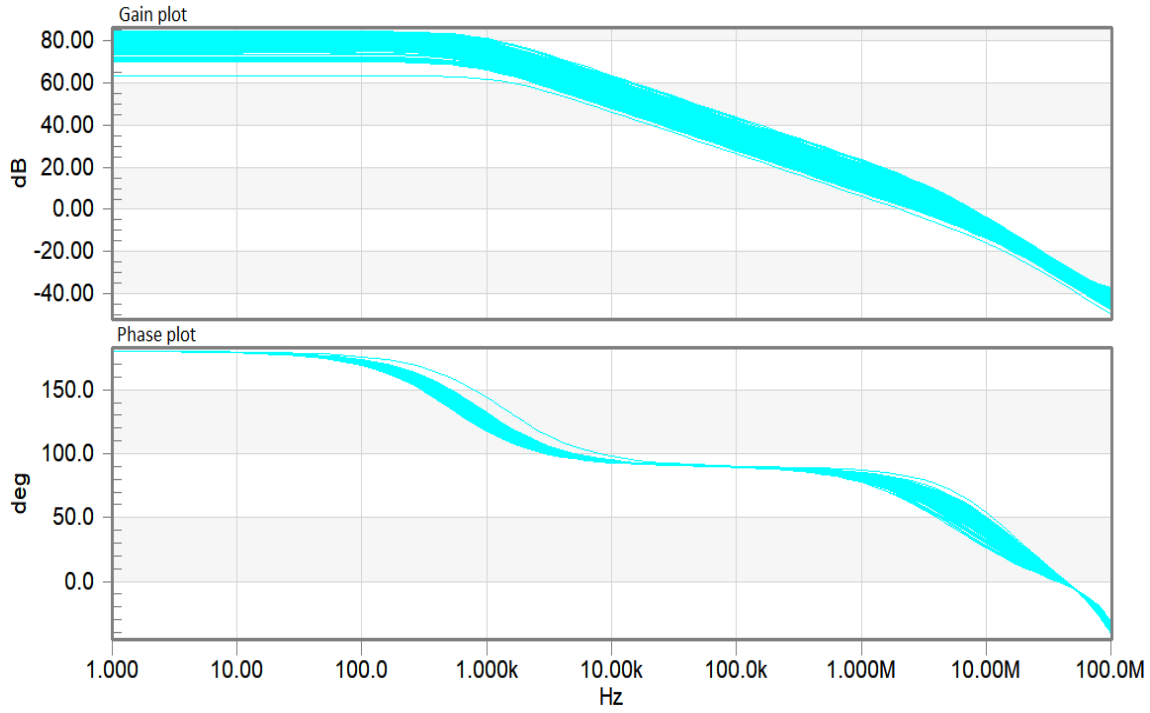


Fig. 5.20 Monte-Carlo simulation for gain and phase response of the proposed amplifier 7 with V_{DD} deviations

5.4 Proposed amplifier 8

Figure 5.21 shows the block diagram of the proposed amplifier 8. It consists of three stages, which are connected in a cascade. An active LHP zero block is placed at the output of the second stage. The active LHP zero block cancels the parasitic pole of this particular stage. A Miller capacitor C_m and resistor R_m are connected in a feedback loop between the output of the third stage and the second stage to overcome the RHP zero problem. The first stage consists of a modified self cascode

structure. The third stage is an inverting amplifier to comply with the condition of negative gain in the Miller loop. Further, the feed forward path implements a push pull output stage.

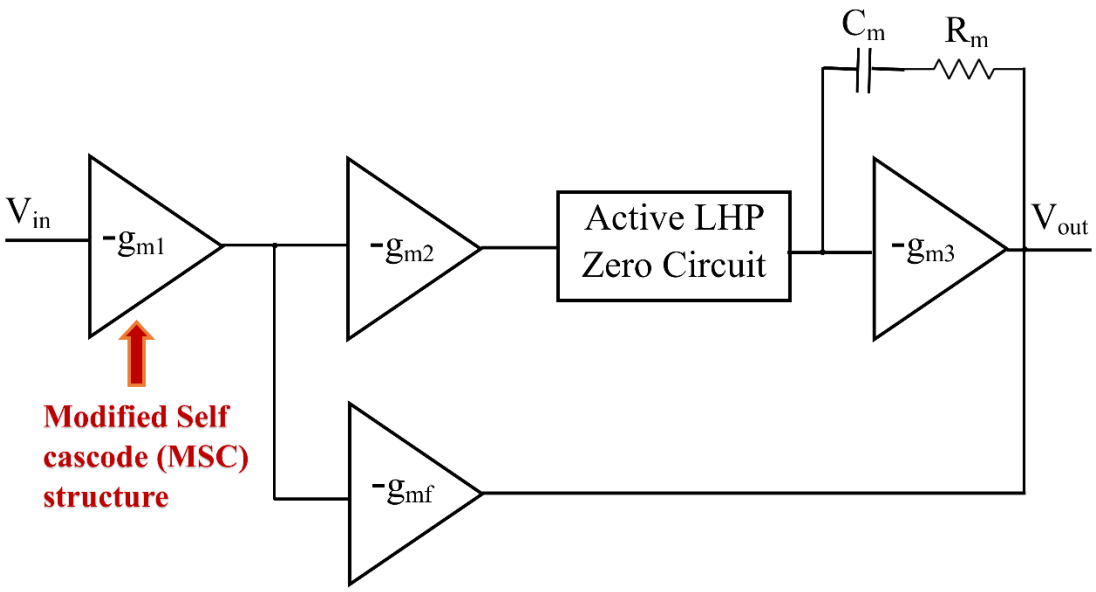


Fig. 5.21 Block diagram of proposed amplifier 8

5.4.1 Circuit description of proposed amplifier 8

Figure 5.22 shows the circuit diagram of the proposed amplifier 8. First stage is the differential amplifier, which consists of Modified Self Cascode (MSC) circuit (M1-M6), current mirror load (M7-M8) and current source I_B. The input transistors are the modified self-cascode circuits in which self-cascode transistors M1-M2 and M3-M4 are placed in parallel with transistors M5 and M6 in order to achieve higher transconductance. For optimal operation, transistors M1-M3 always works in the saturation region, while transistor M2-M4 functions in the linear region. This arrangement enhances the GBW of the amplifier and is therefore adopted in the proposed amplifier 8. Additionally, because of the very low voltage that exists between the source and drain terminals of transistors M2-M4, this structure can be utilized in low voltage applications. Further, the proposed three stage amplifier utilizes the active LHP zero block at the output of the second stage to cancel the parasitic pole of this particular stage. Moreover, a feedback loop comprising of a Miller capacitor C_m and resistor R_m is placed between the output of the third stage and the second stage to get over the RHP zero issue. A common source amplifier (transistor M9) with an active LHP zero circuit (transistors M10-M11; resistor R_a and capacitor C_a) is used as the second stage.

Transistor M12 works as a current source. The third stage is again a common source amplifier (M13-M14) with a push pull output stage (transistor M14), which affects the large signal performance only. A feed forward stage is used to implement the push pull output stage. As a result, the slew rate is enhanced while maintaining the same small-signal open-loop transfer function.

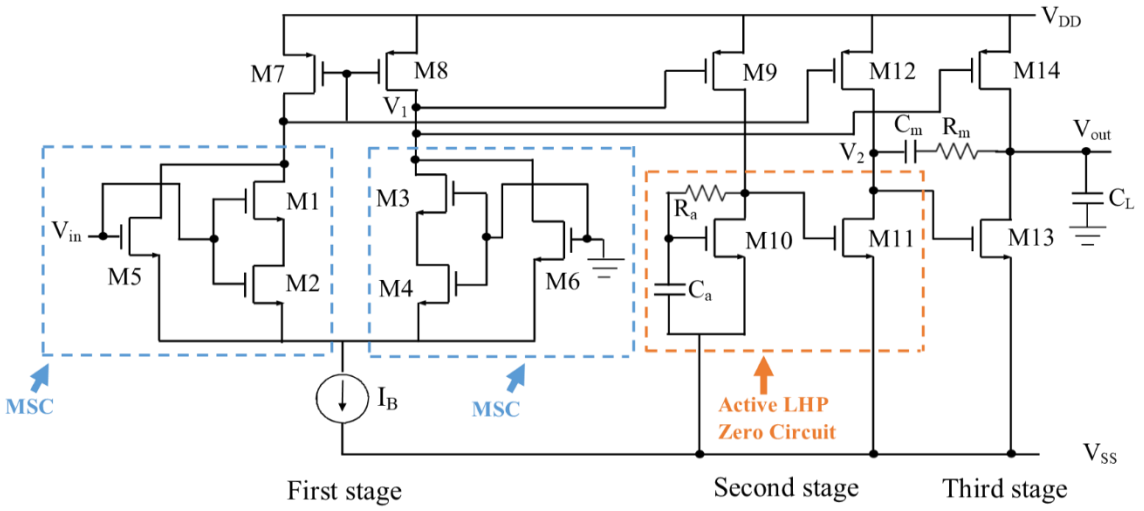


Fig. 5.22 Transistor level implementation of proposed amplifier 8

5.4.2 Small signal analysis of proposed amplifier 8

In order to find out the GBW and stability of the proposed amplifier 8, the open loop transfer function is required. To find out the transfer function, the small signal model of the proposed amplifier 8 is drawn and the same is shown in Fig. 5.23. Let the transconductance and output resistance of the first, second, and third stage are expressed as g_{miA} and r_{oiA}, where i = 1, 2, and 3, while the output capacitance is C_{1A}, C_{2A}, and C_L, respectively.

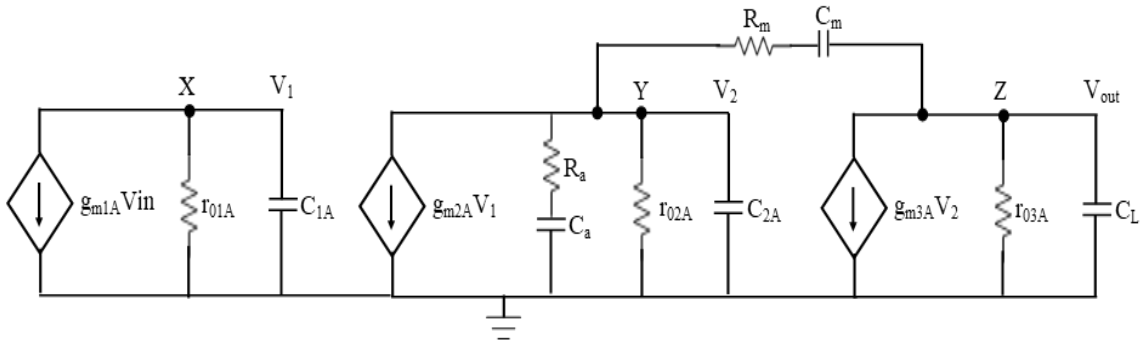


Fig. 5.23 Small signal model of proposed amplifier 8

To simplify the analysis, following assumption is made.

$g_{m1A}r_{o1A} >> 1,\ g_{m2A}r_{o2A} >> 1,\ g_{m3A}r_{o3A} >> 1$ (5.27)

The transfer function of the proposed amplifier 8 is given by Eq. 5.28.

$$A(s) = \frac{A_{dc}(1+sC_mR_m)}{1 + a_1s + b_1s^2 + c_1s^3 + d_1s^4} \quad (5.28)$$

where A_{dc} represents the low frequency gain of proposed amplifier 8 and is given by,

$$A_{dc} = g_{m1A}r_{o1A}g_{m2A}r_{o2A}g_{m3A}r_{o3A} \quad (5.29)$$

and the coefficients a_1, b_1, c_1 and d_1 are given by Eqs. 5.30-5.33.

$$a_1 = C_Lr_{o3A} + C_mr_{o2A}g_{m3A}r_{o3A} + C_ar_{o2A} + C_{1A}r_{o1A} + C_m(R_m + r_{o2A}) \quad (5.30)$$

$$b_1 = C_LC_mr_{o2A}r_{o3A} + C_mC_{1A}g_{m3A}r_{o1A}r_{o2A}r_{o3A} + C_Lr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A}) \quad (5.31)$$

$$c_1 = C_LC_mR_mr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A}) + C_LC_{1A}r_{o1A}r_{o2A}r_{o3A}(C_m + C_{2A}) \quad (5.32)$$

$$d_1 = C_mC_{1A}C_{2A}R_mr_{o1A}r_{o2A} \quad (5.33)$$

Eq. 5.28 contains a dominant pole ω_{P1}, three non-dominant poles ω_{P2}, $\omega_{P3,}$ ω_{P4} and one LHP zero ω_z, which are given by Eqs. 5.34-5.38.

$$\omega_{P1} = \frac{1}{C_Lr_{o3A} + C_mr_{o2A}g_{m3A}r_{o3A} + C_zr_{o2A} + C_1r_{o1A} + C_m(R_m + r_{o2A})} \quad (5.34)$$

$$\omega_{P2} = \frac{C_Lr_{o3A} + C_mr_{o2A}g_{m3A}r_{o3A} + C_zr_{o2A} + C_{1A}r_{o1A} + C_m(R_m + r_{o2A})}{C_LC_mr_{o2A}r_{o3A} + C_mC_{1A}g_{m3A}r_{o1A}r_{o2A}r_{o3A} + C_Lr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A})} \quad (5.35)$$

$$\omega_{P3} = \frac{C_LC_mr_{o2A}r_{o3A} + C_mC_{1A}g_{m3A}r_{o1A}r_{o2A}r_{o3A} + C_Lr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A})}{C_LC_mR_mr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A}) + C_LC_{1A}r_{o1A}r_{o2A}r_{o3A}(C_m + C_{2A})} \quad (5.36)$$

$$\omega_{P4} = \frac{C_LC_mR_mr_{o3A}(C_{1A}r_{o1A} + C_{2A}r_{o2A}) + C_LC_{1A}r_{o1A}r_{o2A}r_{o3A}(C_m + C_{2A})}{C_mC_{1A}C_{2A}R_mr_{o1A}r_{o2A}} \quad (5.37)$$

$$\omega_z = \frac{1}{R_mC_m} \quad (5.38)$$

The GBW can be represented as the multiplication of DC gain and the dominant pole frequency and is given by Eq. 5.39.

$$GBW = A_{dc}.\omega_{P1} = \frac{g_{m1A}r_{o1A}g_{m2A}r_{o2A}g_{m3A}r_{o3A}}{C_L r_{o3A} + C_m r_{o2A}g_{m3A}r_{o3A} + C_z r_{o2A} + C_{1A}r_{o1A} + C_m(R_m + r_{o2A})} \quad (5.39)$$

It may be observed from Eqs. 5.34-5.37 that RHP pole does not exist for the proposed amplifier 8, therefore, it is unconditionally stable. Moreover, the proposed amplifier does not have any RHP zero, which signifies that the proposed amplifier is highly stable.

5.4.3 Simulation results and discussions

The functional verification of proposed amplifier 8 is performed through simulations using 0.18 µm technology parameters. The design parameters of the proposed amplifier 8 is tabulated in Table 5.5.

Table 5.5 Design parameters of proposed amplifier 8

Parameters	Value
Transistor dimensions	M1, M3, M5, M6: W/L = 1.5 µm/1 µm M2, M4: W/L = 0.75 µm/1 µm M7, M8: W/L = 3.9 µm/1 µm M9, M12: W/L = 3.1 µm/1 µm M10, M11, M13: W/L = 1.6 µm/0.6 µm M14: W/L = 2.9 µm/1 µm
R_m, Rz	1 kΩ, 500 kΩ
C_m, Cz, C_L	1 fF, 37 fF, 1 nF
Biasing current (I)	50 µA

Figure 5.24 shows the frequency response of the proposed amplifier 8. For the proposed amplifier 8, the GBW is observed to be 7.2 MHz. Moreover, the proposed amplifier also provides the phase margin of optimum value, which suggests good stability. The DC gain is 84 dB for the amplifier.

Figure 5.25 displays the unity gain step response for an input pulse of 100 mV_{pp}. The 1 % settling time and slew rate of the proposed amplifier are found to be 2.5 µs, and 0.1 V/µs, respectively. The frequency responses of CMRR is presented in Fig. 5.26. The CMRR is found as 271 dB at low frequencies. The PSRR graph is shown in Fig. 5.27 for the proposed amplifier 8. It can be confirmed that the PSRR is 88.8 dB.

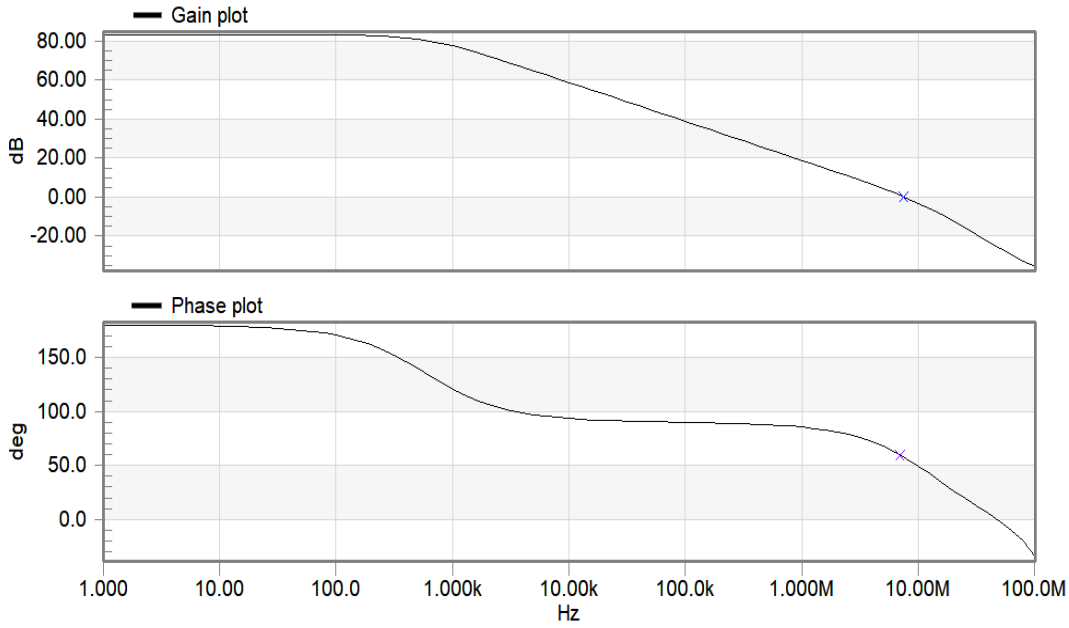


Fig. 5.24 Frequency response of proposed amplifier 8

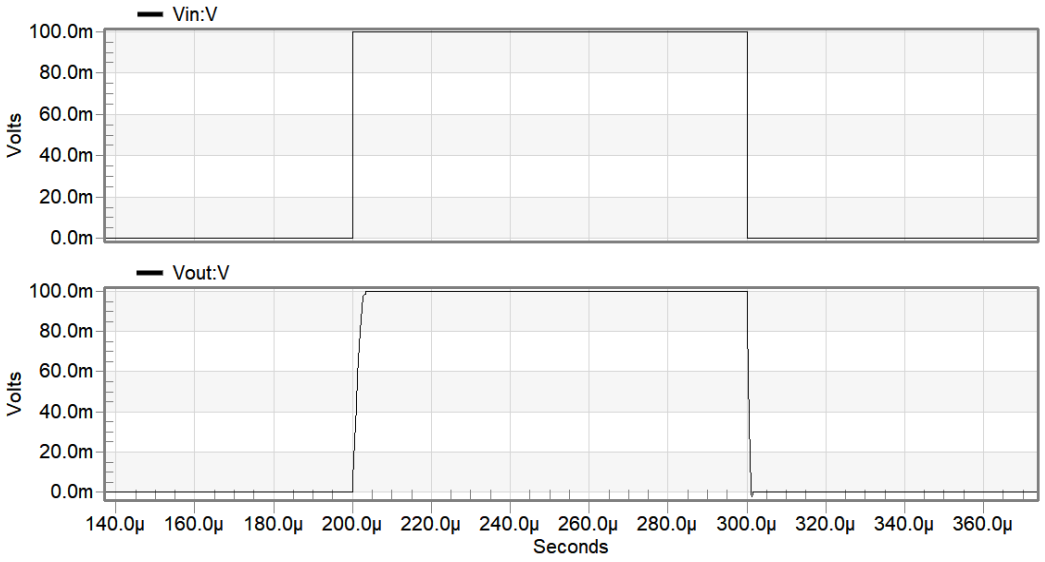


Fig. 5.25 Transient response of proposed amplifier 8

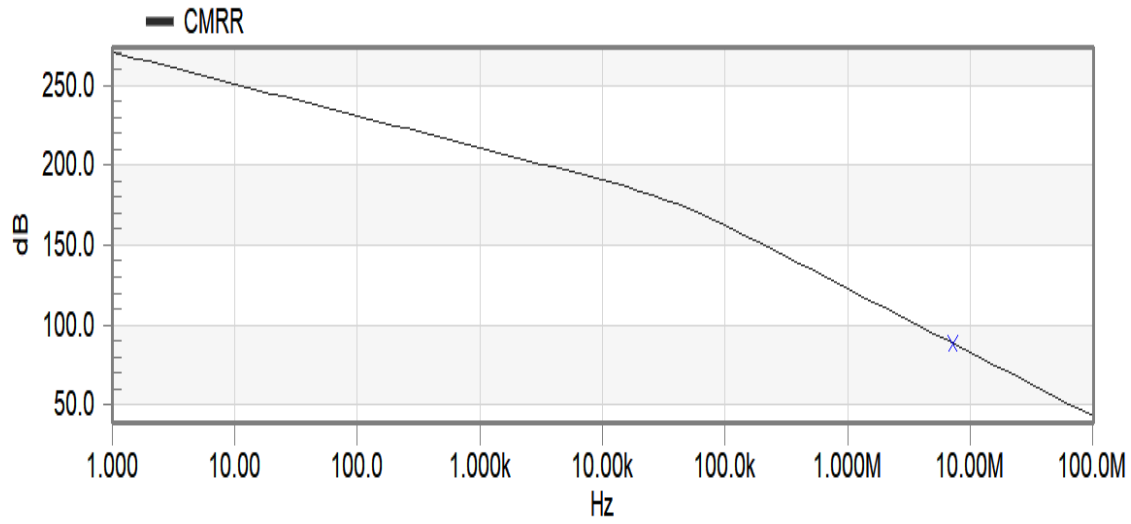


Fig. 5.26 Frequency response of CMRR for proposed amplifier 8

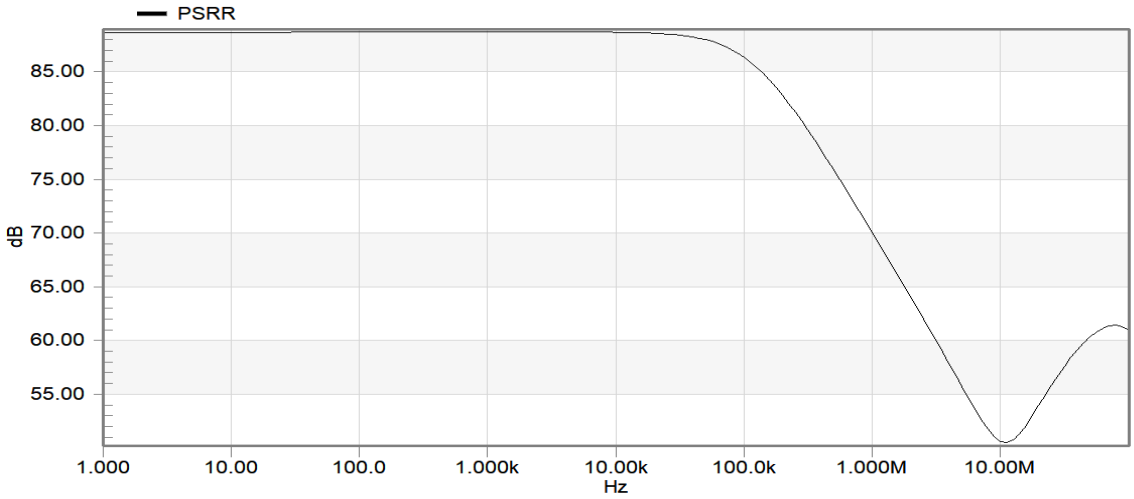


Fig. 5.27 Frequency response of PSRR for proposed amplifier 8

Corner analysis has been done to find out the process variations and the frequency response of the proposed amplifier at all five corners (TT, SF, FS, SS and FF). The corresponding graph is shown in Fig. 5.28. It can be seen that the highest deviations in Gain, GBW and PM are within 25%, except FS process corner, for which the variations in PM are higher. Deviations are assessed with reference to TT process corner. Further, the gain and phase plots of proposed amplifier with supply voltage variation of ±2.5% have been shown in Fig. 5.29. Table 5.6 summarizes the results. It has the maximum variations in gain, GBW, and PM of (2.5%, 16.7%, 18.3%). So, the maximum overall deviation with reference to supply voltage is 18.3%. Additionally, the impact of power supply variation is examined through Monte-Carlo simulations with 5% Gaussian distribution and

200 runs. The frequency response is depicted in Fig. 5.30. The mean and standard deviations in gain are observed to be 92.44 dB and 5.16 dB for the proposed amplifier 8.

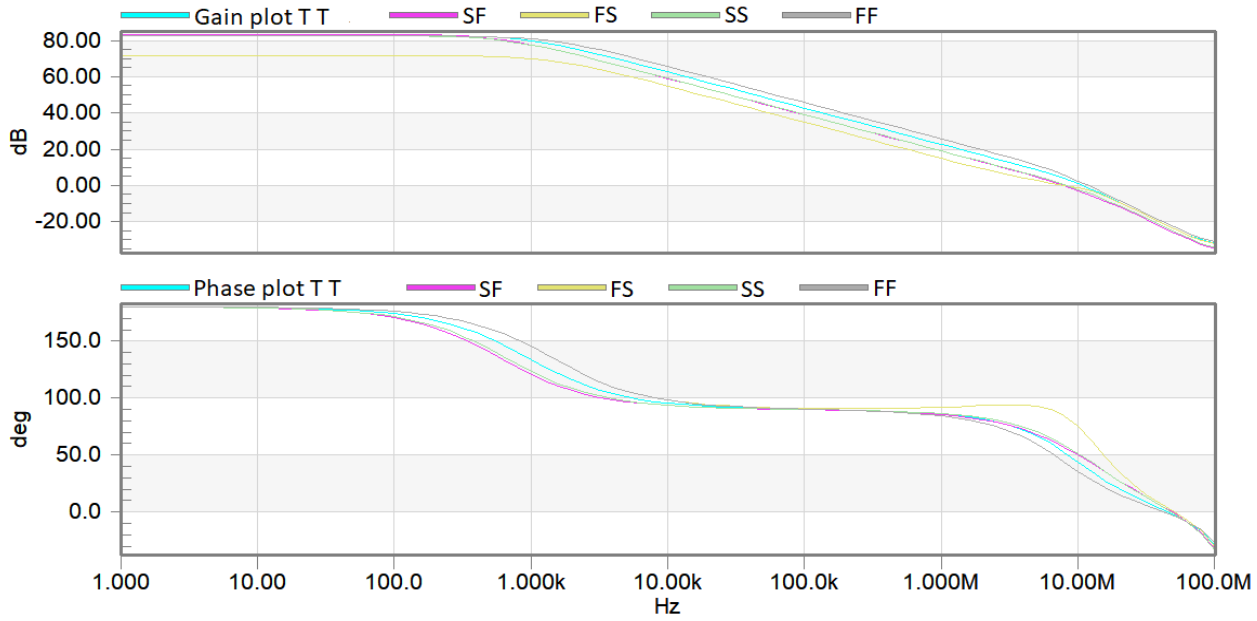


Fig. 5.28 Corner analysis of proposed amplifier 8

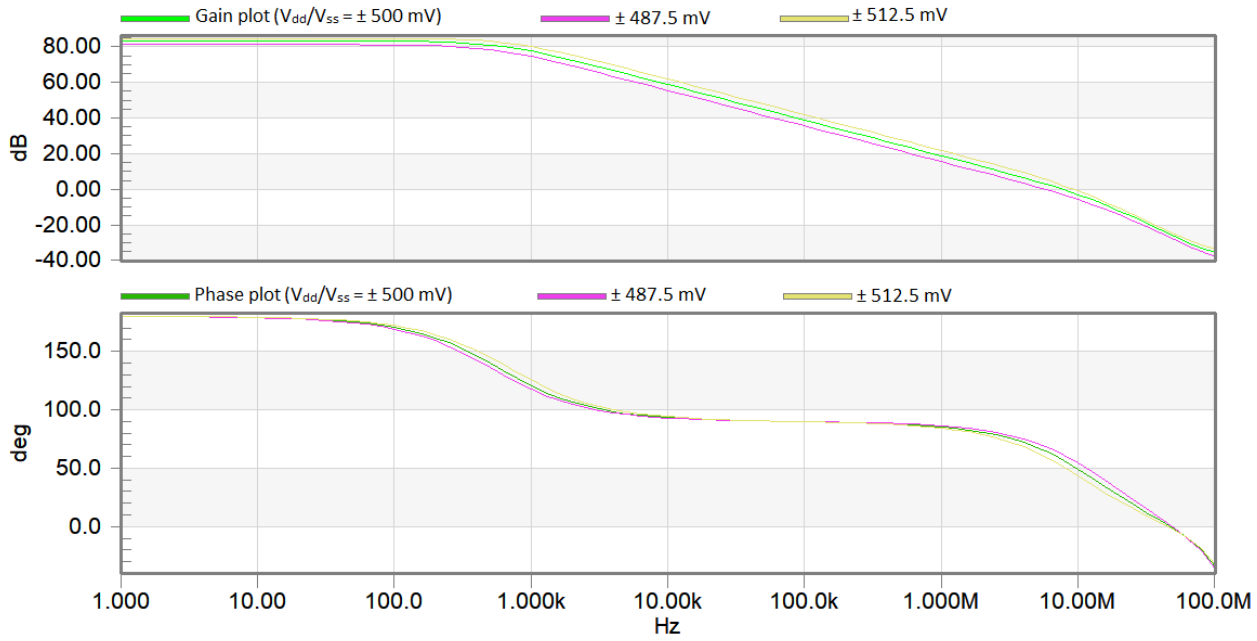


Fig. 5.29 Impact of supply voltage variations on proposed amplifier 8

Table 5.6 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 8

Performance parameter	Corner					Supply Voltage variation (500 mV ± 2.5% of 500 mV)	
	TT	SF	FS	SS	FF	487.5 mV	512.5 mV
Gain (dB)	83.7	84.2	72.3	83.4	83.2	81.9	85.5
GBW (MHz)	10.3	8.2	8.1	8.6	11.2	6.4	8.4
PM (°)	45.1	55.6	83.2	56.3	35.1	66.8	49

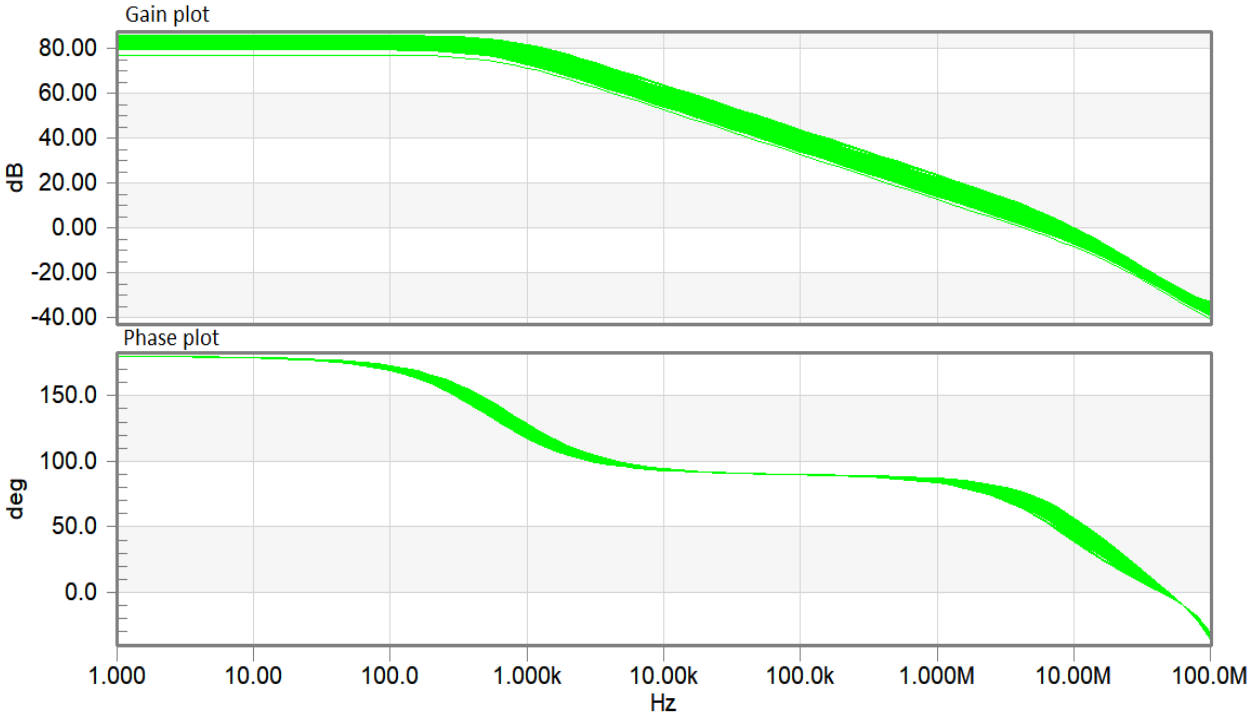


Fig. 5.30 Monte-Carlo simulation for frequency response of proposed amplifier 8 against V_{DD} deviations

5.5 Proposed amplifier 9

The block diagram of the proposed amplifier 9 is shown in Fig. 5.31. It consists of three stages, which are connected in a cascade. An active LHP zero block is placed at the output of the second stage. The active LHP zero block cancels the parasitic pole of this particular stage. A Miller capacitor C_m and a resistor R_m are connected in a feedback loop between the output of the third stage and the first stage to overcome the RHP zero problem. The first stage consists of a modified

self cascode structure. The second and third stages are inverting amplifiers. Further, the feed forward path implements a push pull output stage.

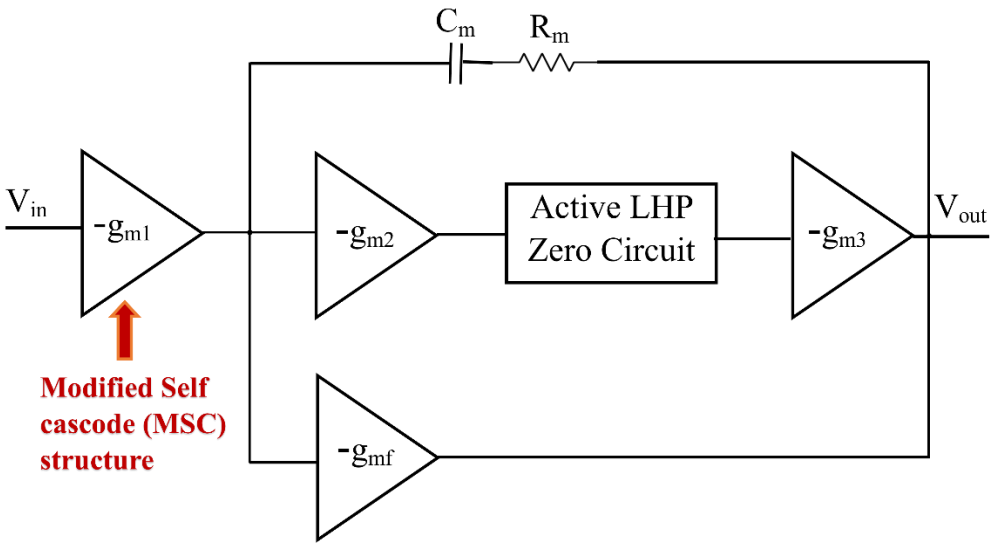


Fig. 5.31 Block diagram of proposed amplifier 9

5.5.1 Circuit description of proposed amplifier 9

Figure 5.32 displays the circuit schematic of the proposed amplifier 9. The input stage is the differential amplifier, which consists of Modified Self Cascode (MSC) circuit (M1-M6), current mirror load (M7-M8) and current source I_B. The input transistors are the modified self-cascode circuits in which self-cascode transistors M1-M2 and M3-M4 are placed in parallel with transistors M5 and M6 in order to achieve higher transconductance. For optimal operation, transistors M1-M3 always works in the saturation region, while transistor M2-M4 functions in the linear region. This arrangement enhances the GBW of the amplifier. Further, the proposed three stage amplifier utilizes the active LHP zero block at the output of the second stage to cancel the parasitic pole of this particular stage. Moreover, a feedback loop comprising of a Miller capacitor C_m and resistor R_m is placed between the output of the third stage and the first stage to get over the RHP zero issue. A common source amplifier (transistor M9) with an active LHP zero circuit (transistors M10-M11; resistor R_a and capacitor C_a) is used as the second stage. Transistor M12 works as a current source. The third stage is again a common source amplifier (M13-M14) with a push pull output stage (transistor M14), which affects the large signal performance only. A feed forward path is employed to implement the push pull output stage, resulting in improved transient response.

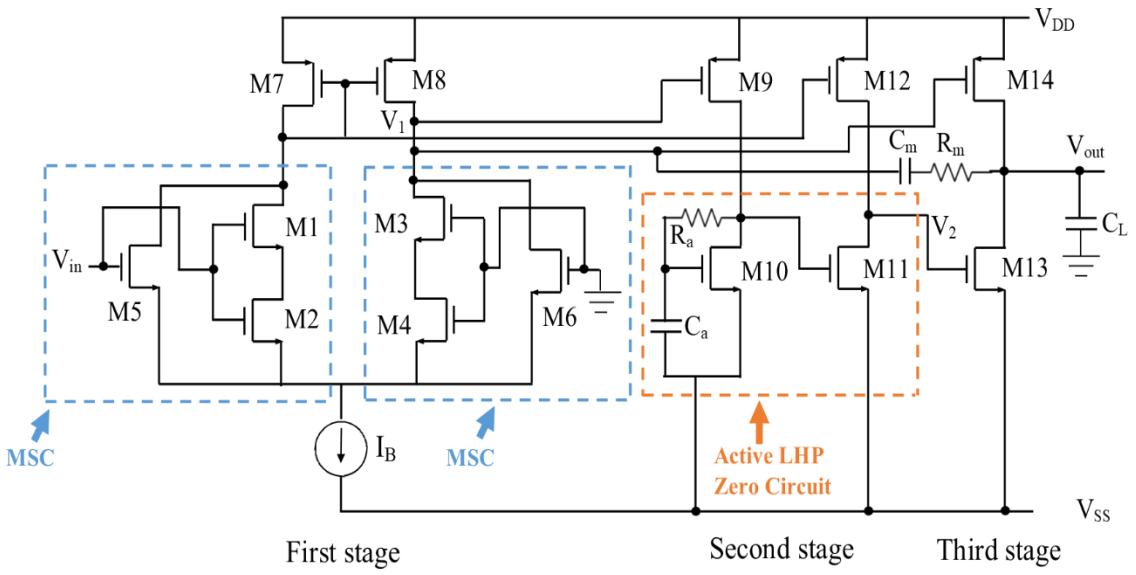


Fig. 5.32 Transistor level implementation of proposed amplifier 9

5.5.2 Small signal analysis of proposed amplifier 9

The small signal model of the proposed amplifier 9 is shown in Fig. 5.33. Let the transconductance and output resistance of the first, second and third stages are expressed as g_{miB} and r_{oiB}, where i = 1, 2, and 3, while the output capacitance is C_{1B}, C_{2B} and C_L, respectively.

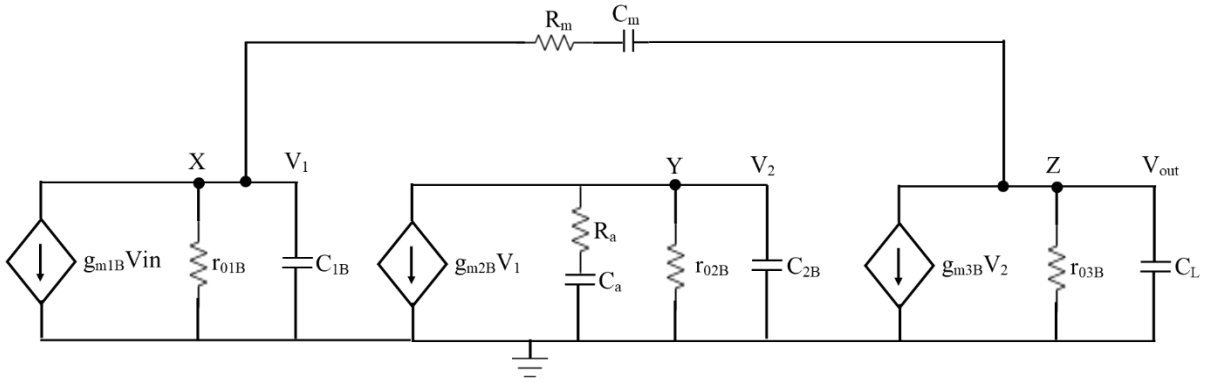


Fig. 5.33 Small signal model of proposed amplifier 9

The transfer function of the proposed amplifier 9 is given by Eq. 5.40.

$$A(s) = \frac{A_{dc}(1+sC_mR_m)}{1 + a_2s + b_2s^2 + c_2s^3 + d_2s^4} \tag{5.40}$$

where A_{dc} is the low frequency gain of proposed amplifier 9 and is given by,

$$A_{dc} = g_{m1B}r_{o1B}g_{m2B}r_{o2B}g_{m3B}r_{o3B} \tag{5.41}$$

and the coefficients a_2, b_2, c_2 and d_2 are given by Eqs. 5.42-5.45.

$$a_2 = C_m r_{o1B} g_{m2B} r_{o2B} g_{m3B} r_{o3B} - C_L r_{o3B} - C_m(R_m + r_{o1B}) \tag{5.42}$$

$$b_2 = C_L r_{o3B}(C_m r_{o1B} + C_m R_m + C_{1B} r_{o1B} + C_{2B} r_{o2B}) + C_{2B} r_{o1B} r_{o2B}(C_m + C_{1B}) \tag{5.43}$$

$$c_2 = C_L r_{o3B}(C_m R_m C_{1B} r_{o1B} + C_m R_m C_{2B} r_{o2B} + C_m C_{2B} r_{o1B} r_{o2B} + C_{1B} C_{2B} r_{o1B} r_{o2B}) \tag{5.44}$$

$$d_2 = C_L C_m R_m C_{1B} C_{2B} r_{o1B} r_{o2B} r_{o3B} \tag{5.45}$$

Eq. 5.40 contains a dominant pole ω_{P1}, three non-dominant poles ω_{P2}, $\omega_{P3,}$ ω_{P3} and one LHP zero ω_z, which are given by Eqs. 5.46-5.50.

$$\omega_{P1} = \frac{1}{C_m r_{o1B} g_{m2B} r_{o2B} g_{m3B} r_{o3B} - C_L r_{o3B} - C_m(R_m + r_{o1B})} \tag{5.46}$$

$$\omega_{P2} = \frac{C_m r_{o1B} g_{m2B} r_{o2B} g_{m3B} r_{o3B} - C_L r_{o3B} - C_m(R_m + r_{o1B})}{C_L r_{o3B}(C_m r_{o1B} + C_m R_m + C_{1B} r_{o1B} + C_{2B} r_{o2B}) + C_{2B} r_{o1B} r_{o2B}(C_m + C_{1B})} \tag{5.47}$$

$$\omega_{P3} = \frac{C_L r_{o3B}(C_m r_{o1B} + C_m R_m + C_{1B} r_{o1B} + C_{2B} r_{o2B}) + C_{2B} r_{o1B} r_{o2B}(C_m + C_{1B})}{C_L r_{o3B}(C_m R_m C_{1B} r_{o1B} + C_m R_m C_{2B} r_{o2B} + C_m C_{2B} r_{o1B} r_{o2B} + C_{1B} C_{2B} r_{o1B} r_{o2B})} \tag{5.48}$$

$$\omega_{P4} = \frac{C_m R_m C_{1B} r_{o1B} + C_m R_m C_{2B} r_{o2B} + C_m C_{2B} r_{o1B} r_{o2B} + C_{1B} C_{2B} r_{o1B} r_{o2B}}{C_m R_m C_{1B} C_{2B} r_{o1B} r_{o2B}} \tag{5.49}$$

$$\omega_z = \frac{1}{R_m C_m} \tag{5.50}$$

The GBW can be represented as the multiplication of Eqs. 5.41 and 5.46, which is given by Eq. 5.51.

$$GBW = A_{dc}.\omega_{P1} = \frac{g_{m1B}r_{o1B}g_{m2B}r_{o2B}g_{m3B}r_{o3B}}{C_m r_{o1B} g_{m2B} r_{o2B} g_{m3B} r_{o3B} - C_L r_{o3B} - C_m(R_m + r_{o1B})} \tag{5.51}$$

It is evident from Eqs. 5.46-5.47 that the dominant pole ω_{P1} moves towards the origin and the first non-dominant pole ω_{P2} shifts away from the origin. As a result, the GBW of the proposed amplifier 9 is enhanced.

5.5.3 Simulation results and discussions

The functional verification of proposed amplifier 9 is performed through simulations using 0.18 µm technology parameters. The design parameters of the proposed amplifier 8 is given in Table 5.7.

Table 5.7 Design parameters of proposed amplifier 9

Parameters	Value
Transistor dimensions	M1, M3, M5, M6: W/L = 1.5 µm/1 µm M2, M4: W/L = 0.75 µm/1 µm M7, M8: W/L = 3.9 µm/1 µm M9, M12: W/L = 3.1 µm/1 µm M10, M11, M13: W/L = 1.6 µm/0.6 µm M14: W/L = 2.9 µm/1 µm
R_m, Rz	1 kΩ, 500 kΩ
C_m, Cz, C_L	5 fF, 50 fF, 1 nF
Biasing current (I)	50 µA

Figure 5.34 shows the frequency response of the proposed amplifier 9. For the proposed amplifier 9, the GBW is observed to be 8 MHz. Moreover, the proposed amplifier also provides the phase margin of the optimum value, which suggests good stability. Further, the DC gain is 84 dB. Figure 5.35 displays the unity gain step response for an input pulse of 100 mV_{pp}. The 1 % settling time and slew rate are found to be 2.5 µs and 0.1 V/µs, respectively. The frequency response of CMRR is presented in Fig. 5.36. The CMRR is found as 271 dB at low frequencies. The PSRR graph is shown in Fig. 5.37. It can be confirmed that the PSRR is 88.8 dB for the proposed amplifier 9.

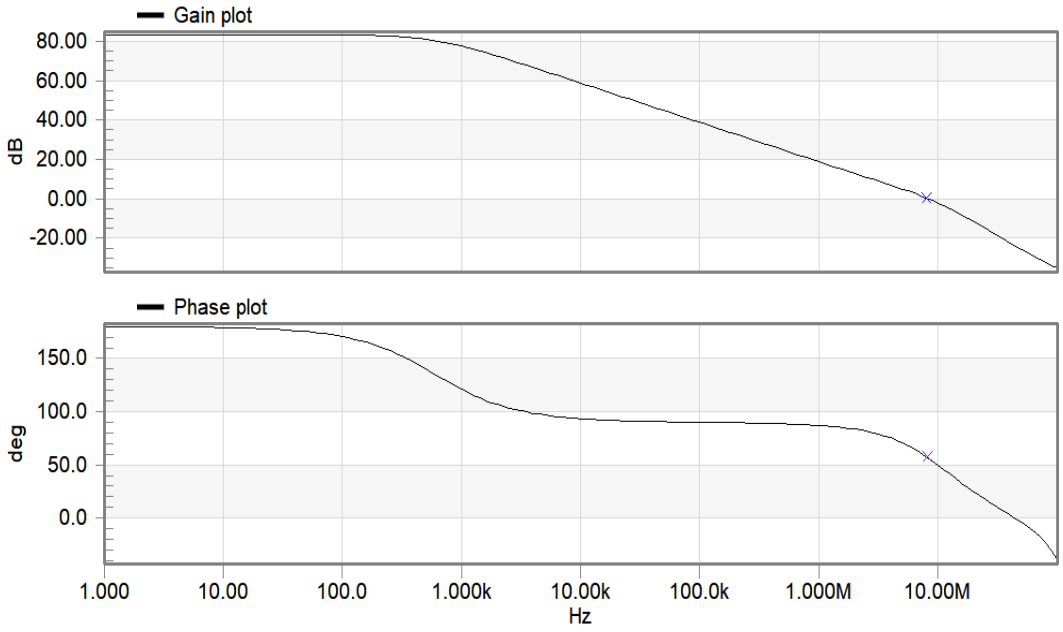


Fig. 5.34 Frequency response of proposed amplifier 9

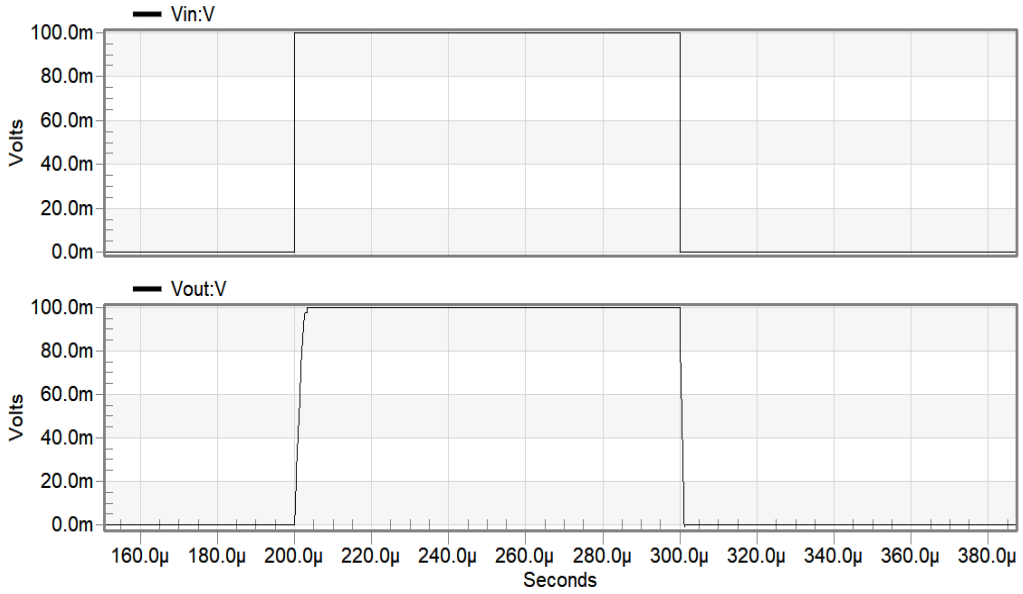


Fig. 5.35 Transient response of proposed amplifier 9

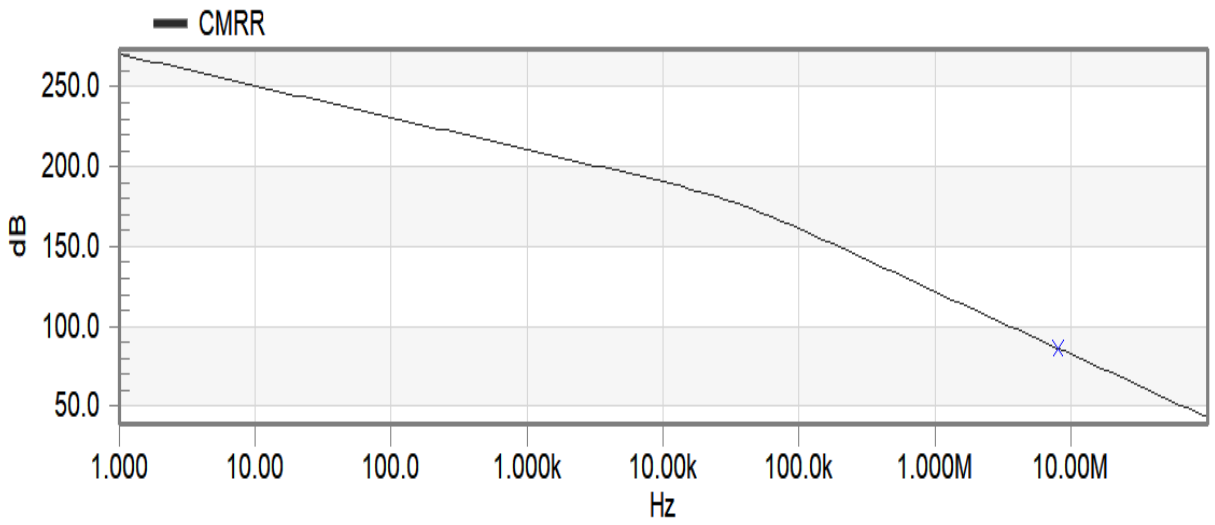


Fig. 5.36 Frequency response of CMRR for proposed amplifier 9

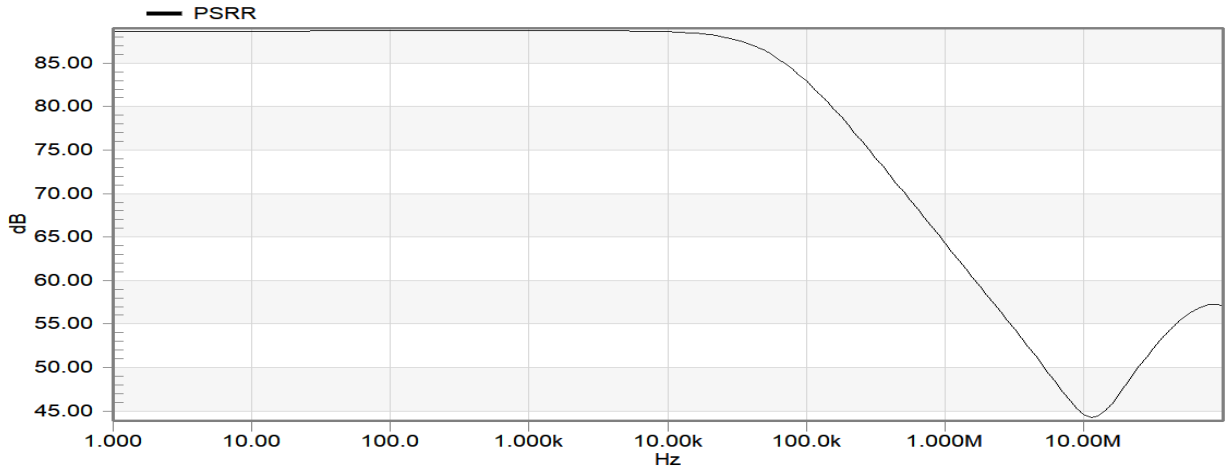


Fig. 5.37 Frequency response of PSRR for proposed amplifier 9

The frequency response of the proposed amplifier 9 is displayed in Fig. 5.38 at all five corners (TT, SF, FS, SS, and FF). It can be seen that the highest deviations in Gain, GBW, and PM are within 25%, except FS process corner, for which variations in PM are higher. Deviations are assessed with reference to TT process corner. Further, the gain and phase plots of the proposed amplifier with supply voltage variation of ±2.5% have been shown in Fig. 5.39. Table 5.8 summarizes the results. The proposed amplifier has maximum variations in gain, GBW, and PM of 2.5%, 21.3% and 20.7% respectively. So, the maximum overall deviation with reference to supply voltage is 21.3%. Additionally, the impact of power supply variation is studied through Monte-Carlo simulations with 5% Gaussian distribution and 200 runs. The frequency response is

depicted in Fig. 5.43. The mean and standard deviations in gain for the proposed amplifier 9 are observed to be 92.44 dB and 5.16 dB respectively.

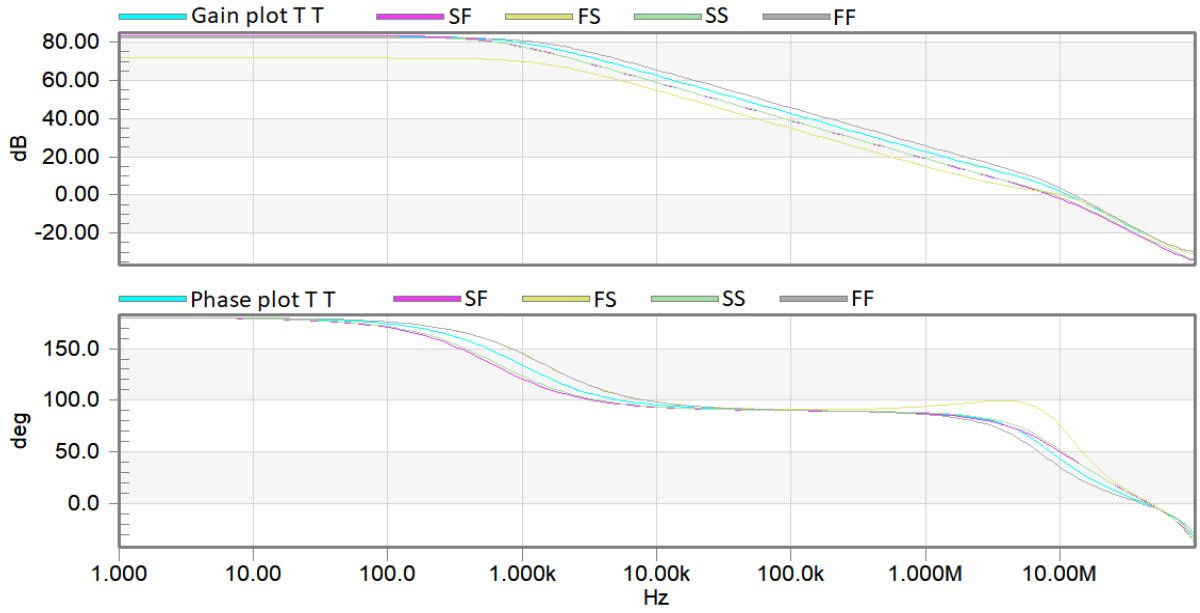


Fig. 5.38 Corner analysis of proposed amplifier 9

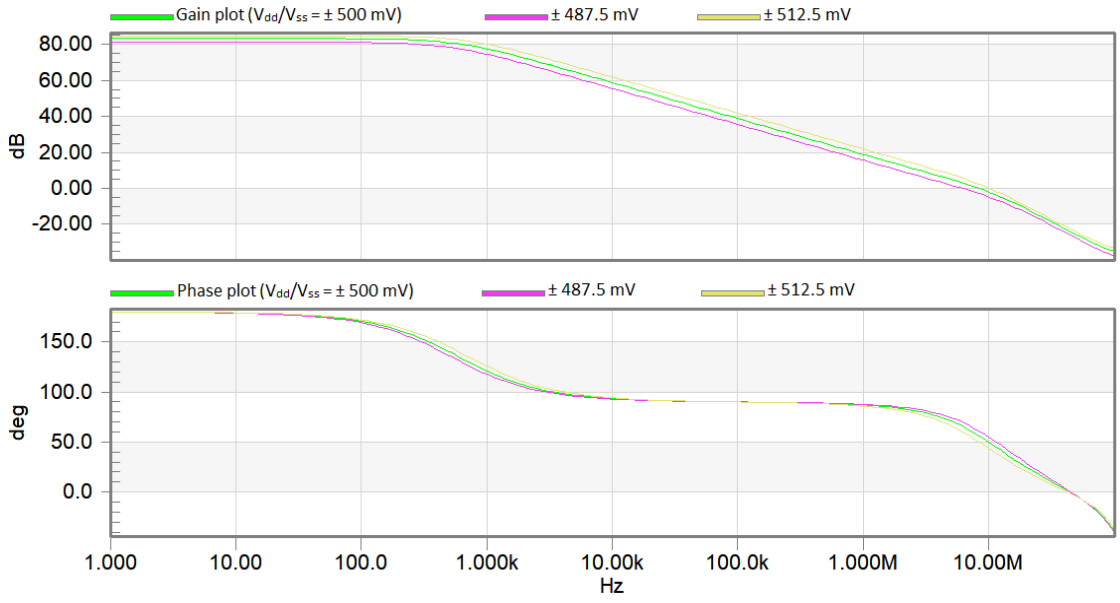


Fig. 5.39 Impact of supply voltage variations on proposed amplifier 9

Table 5.8 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 9

Performance parameter	Corner					Supply Voltage variation (500 mV ± 2.5% of 500 mV)	
	TT	SF	FS	SS	FF	487.5 mV	512.5 mV
Gain (dB)	83.7	84.2	72.3	83.4	83.2	81.9	85
GBW (MHz)	10.6	8.4	9.9	9	11.2	6.5	9.7
PM (°)	44.7	55.8	75.1	55.5	34.2	69.6	47.6

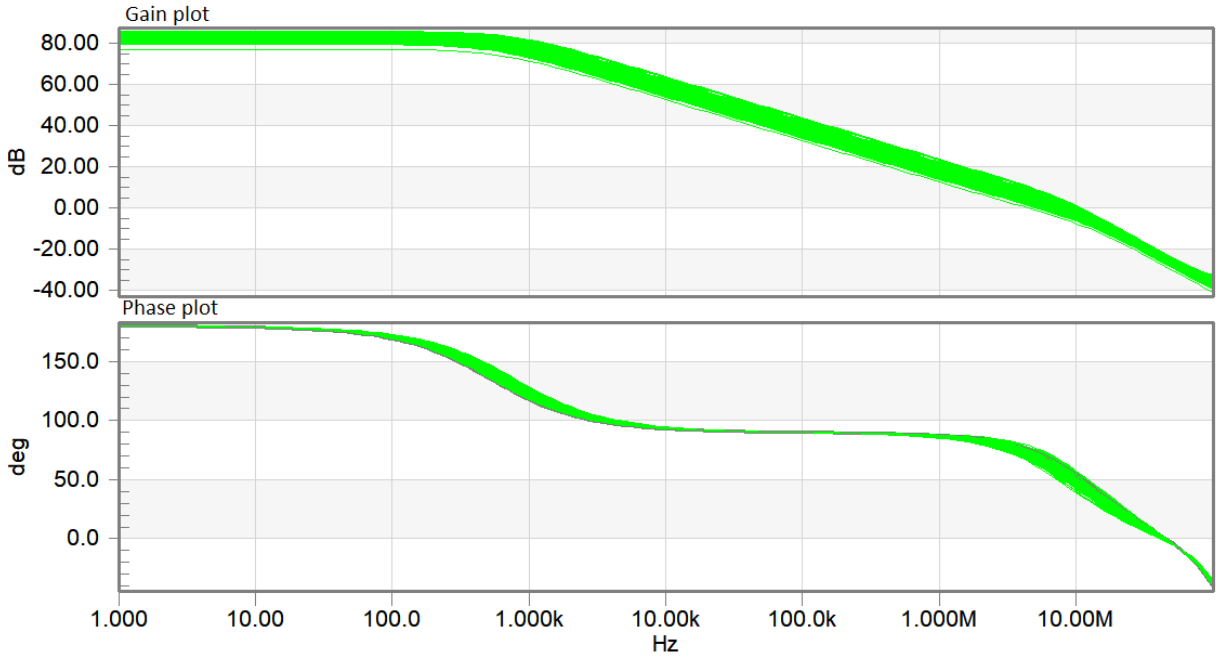


Fig. 5.40 Monte-Carlo simulation for frequency response of proposed amplifier 9 against V_{DD} deviations

5.6 Comparison

The performance of the proposed amplifiers 6-9 is compared in Table 5.9. It can be seen that the proposed amplifiers offer better GBW in comparison with their counterparts at 1 nF load. The phase margin is 62° for the proposed amplifier 6, while it is 60° for the proposed amplifiers 7-9. It indicates the good stability of the amplifiers. Further, the power consumption of the proposed amplifiers is less than Ref. [34]. Moreover, FOM_S of the proposed amplifier 9 is better than other amplifiers, while $IFOM_S$ is higher than Refs. [34, 36].

Table 5.9: Performance comparison of proposed amplifiers 6-9 with their counterparts

Parameters	**[34]**	**[35]**	**[36]**	**Proposed amplifier 6**	**Proposed amplifier 7**	**Proposed amplifier 8**	**Proposed amplifier 9**
Technology (nm)	350	180	180	180	180	180	180
Supply voltage (V)	± 2	± 1.2	1.8	± 0.5	± 0.5	± 0.5	± 0.5
C_L (nF)	1	1	1	1	1	1	1
GBW (MHz)	1.37	1.13	3	4.8	5.2	7.2	8
PM (°)	83.2	56.2	82	62	60	60	60
DC Gain (dB)	>100	>100	>100	81	82	84	84
Power (µW)	144	15.8	75	106.4	106.4	106.4	106.4
SR (V/µS)	0.59	0.41	1.4	0.1	0.1	0.1	0.1
FOM_S [(MHz . pF)/mW]	9,514	71,518.99	40,000	45,112.78	48,872.18	67,669.17	75,187.97
$IFOM_S$ [(MHz . pF)/mA]	19,028	88,627.45	71,994.24	45112.78	48,872.18	67,669.17	75,187.97
FOM_L [(V/µs . pF)/mW]	4,097	25,949.37	18,666.67	939.85	939.85	939.85	939.85
$IFOM_L$ [(V/µs . pF)/mA]	8,194	32,156.86	33,597.31	939.85	939.85	939.85	939.85

5.7 Summary

In this chapter, four amplifiers (proposed amplifiers 6, 7, 8, and 9) are presented, which employ an active LHP zero block at the output of the second stage to cancel the parasitic pole. A Miller capacitor and a resistor are connected in a feedback loop between the output of the third stage and the second stage in the proposed amplifiers 6, 7, and 8, while they are connected between the output of the third stage and the first stage in the proposed amplifier 9 to overcome the RHP zero problem. The input stage of the proposed amplifier 6 consists of the self cascode structure, while a self cascode with DTMOS is utilized in the input stage of the proposed amplifier 7. Further, a modified self cascode structure is employed in the first stage of the proposed amplifiers 8 and 9 to improve the GBW. The push pull output stage is exploited in all proposed amplifiers to improve the transient response. Moreover, the small signal analysis is performed for all amplifiers to find out the transfer function, poles, and zeros. It determines the stability and GBW of the amplifiers. The proposed amplifiers offer better GBW than other amplifiers. In this regard, the proposed amplifier 9 offers the highest GBW of 8 MHz. Further, the proposed amplifier 6 provides the phase margin of 62°, while the proposed amplifiers 7-9 give the phase margin of 60°. It shows the good stability of the amplifiers presented in this chapter. Additionally, various simulations, such as corner analysis, supply voltage variation, and Monte Carlo analysis are performed to confirm the effectiveness of the proposed amplifiers.

Chapter 6

Reversed Nested Miller Compensation with Class AB Flipped Voltage Follower and Slew Rate Enhancer Circuit

The contents of this chapter are published in:

[1] Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, **"Improved frequency compensation technique of three stage amplifier using class AB flipped voltage follower and slew rate enhancer circuit"**, AEU-International Journal of Electronics and Communications, vol. 177, pp. 1-15, 2024. **(SCI-Expanded)**

6.1 Introduction

In continuation with the FVF and FFVF deployment in the inner compensation loop of RNMC to resolve the RHP zero issue, this chapter investigate the use of class AB Flipped Voltage Follower (FVF) for the same purpose. Further, a slew rate enhancer circuit is utilized between the output of the third stage and the first stage in the proposed amplifier 10, while it is connected between the output of the third stage and the second stage in the proposed amplifier 11. The slew rate enhancer circuit, along with a push pull output stage improves the transient response of the proposed amplifiers.

This chapter is organized as follows: Section 6.2 gives the circuit description of the proposed amplifier 10. Moreover, small signal analysis and simulation results are also discussed in Section 6.2. The circuit of proposed amplifier 11 is discussed in Section 6.3 with its small signal analysis and simulation results. Process corner analysis of both proposed amplifiers has been done to prove the robustness of the amplifiers over process variations, and results are compiled in the respective sections. Further, the effect of supply voltage variations on the performance of the proposed amplifiers is studied, and observations are comprehended in the respective sections. Moreover, Monte Carlo analysis has also been done for both amplifiers. Section 6.4 compares the performance of the proposed amplifiers with their existing counterparts. Finally, the chapter is concluded in Section 6.5.

6.2 Proposed amplifier 10

Figure 6.1 shows the block diagram of the proposed amplifier 10. The input stage is the differential stage. The second and third stages are the inverting and non-inverting amplifier, respectively, to make suitable arrangements for RNMC. Further, the structure of RNMC consists of two compensation capacitors, C_{m1} and C_{m2}. The compensation capacitor C_{m1} is connected between the output of third stage and first stage, while another compensation capacitor C_{m2} is connected between the output of class AB FVF and first stage. It is evident that the inner compensation capacitor C_{m2} is not connected to the output, which helps in increasing the GBW of the amplifier. A class AB FVF is employed in the inner loop to break the forward path to resolve the RHP zero issue. The feed forward path and slew rate enhancer circuit are employed to increase the transient response of the amplifier.

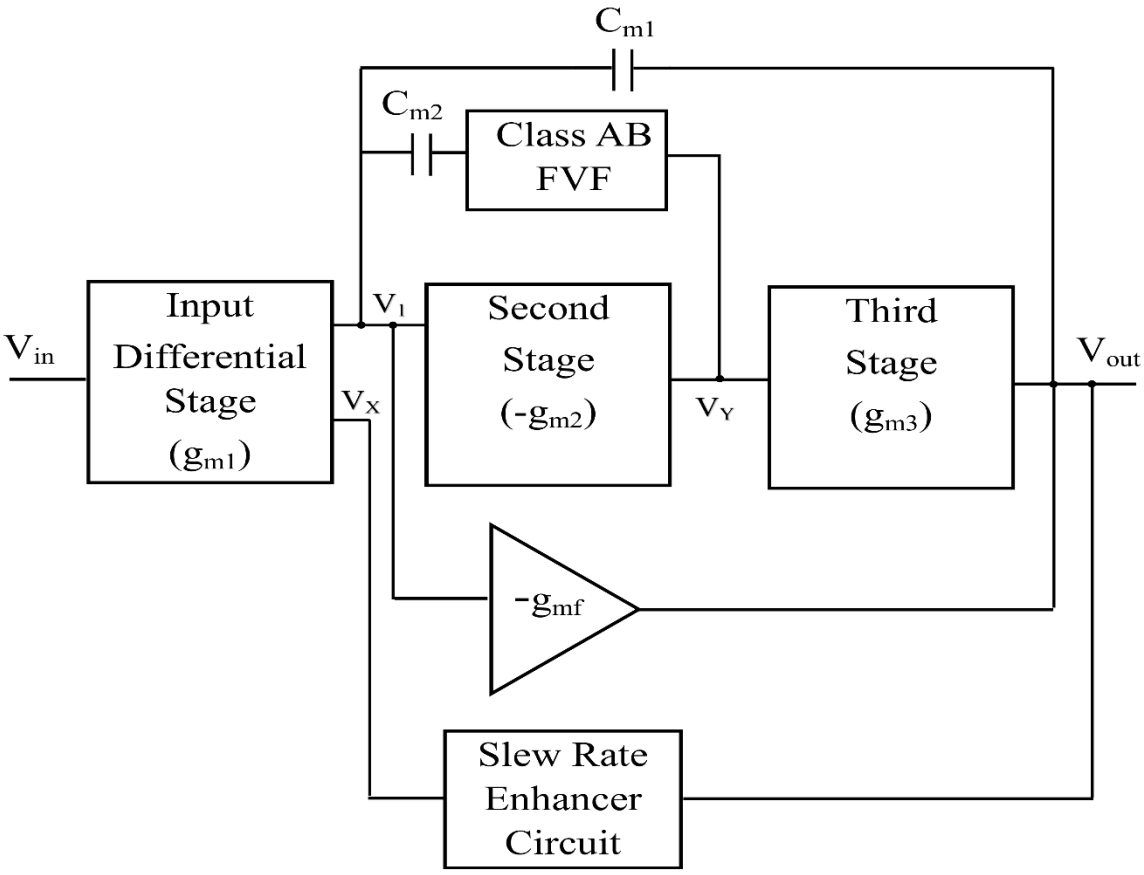


Fig. 6.1 Block diagram of proposed amplifier 10

6.2.1 Circuit description of proposed amplifier 10

The transistor level circuit of the proposed amplifier 10 is shown in Fig. 6.2. Transistors M2 and M3-M6 form the first stage, which is the differential amplifier. The second stage is the common source amplifier (transistors M7-M8). Further, class AB FVF is made up of transistors M9-M12. The third stage is the non-inverting stage, which is formed by the transistors M13-M16. Further, the feed forward path is implemented by connecting the output of the first stage to the gate terminal of the transistor M14. It forms the push pull output stage. Additionally, the slew rate enhancer circuit is connected between the nodes V_X and V_{out}. The push pull output stage and slew rate enhancer circuit improve the transient response of the amplifier.

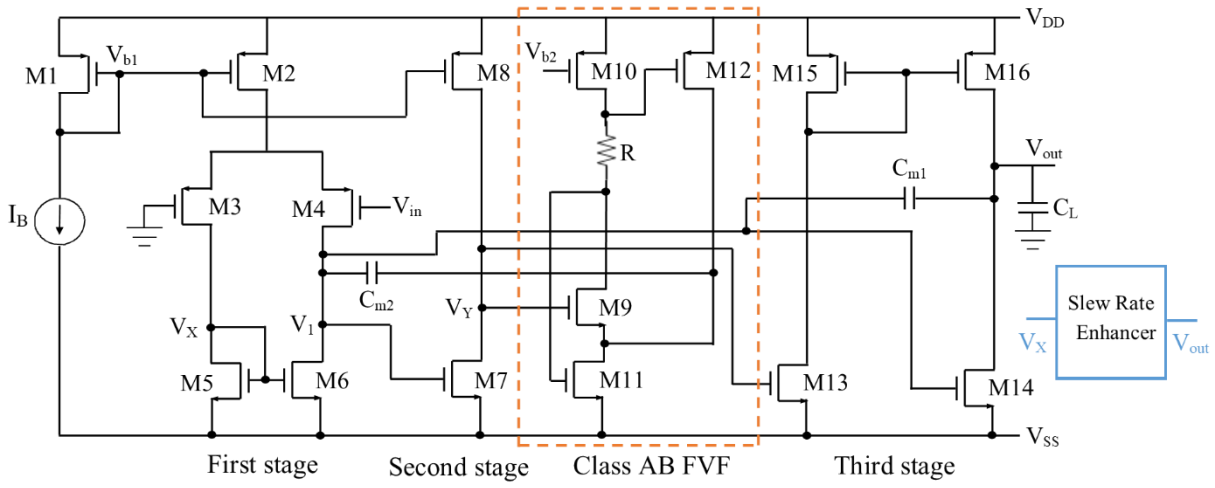


Fig. 6.2 Transistor level implementation of proposed amplifier 10

6.2.2 Small signal analysis of proposed amplifier 10

To perform the small signal analysis, a small signal model of the proposed amplifier 10 is shown in Fig. 6.3. It helps in finding the poles, zeros, DC gain, and GBW. The following assumptions are made to simplify the calculations.

$$g_{mi}r_{oi} >> 1 \tag{6.1}$$

$$C_L, C_{m1}, C_{m2} >> C_1, C_2 \tag{6.2}$$

Where g_{mi} and r_{oi} are the transconductance and output resistance of the i^{th} stage; i = 1, 2, and 3. C_1 and C_2 represent the output capacitance of the first stage and second stage, respectively, whereas C_L is the load capacitance.

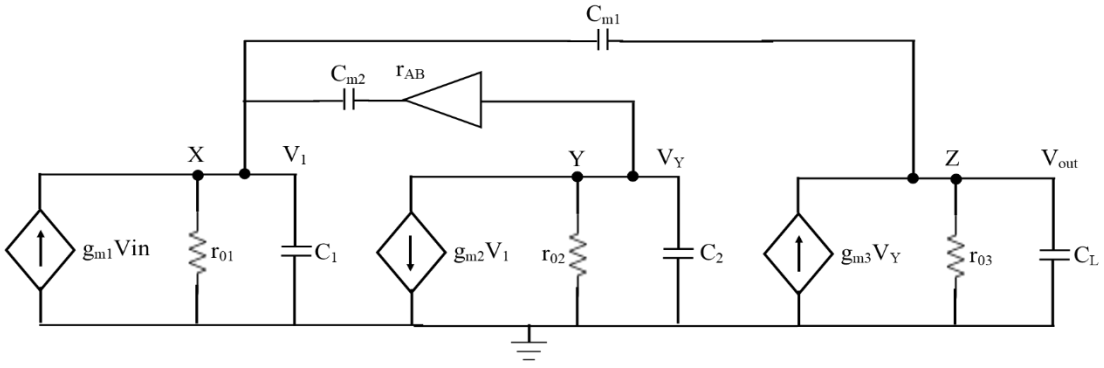


Fig. 6.3. Small signal model of proposed amplifier 10

Eq. 6.3 represents the transfer function of the proposed amplifiers 1 and 2.

$$A(s) = \frac{A_{dc}}{\left(1+\frac{s}{\omega p1}\right)} \frac{\left[1+\left(r_{AB}C_{m2}-\frac{C_{m1}}{r_{AB}g_{m2}g_{m3}}\right)s-\left(\frac{r_{AB}C_{m1}C_{m2}}{r_{O2}g_{m2}g_{m3}}\right)s^2\right]}{\left[1+\frac{C_{m2}(r_{AB}g_{m3}C_{m1}+C_L+C_{m1})}{g_{m3}C_{m1}}s+\left(\frac{r_{AB}C_LC_{m2}}{r_{O2}g_{m2}g_{m3}}\right)s^2\right]} \quad (6.3)$$

A_{dc} denotes the DC gain of the amplifier and is given by Eq. 6.4.

$$A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3} \quad (6.4)$$

The denominator of Eq. 6.3 gives a dominant pole ω_{P1} and two non-dominant poles ω_{P2}, ω_{P3}. Moreover, one LHP zero ω_{z1} and one RHP zero ω_{z2} are provided by the numerator of Eq. 6.3. All poles and zeros are described by Eqs. 6.5-6.9.

$$\omega_{P1} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}} \quad (6.5)$$

$$\omega_{P2} = \frac{g_{m3}C_{m1}}{C_{m2}(C_L + C_{m1} + r_{AB}g_{m3}C_{m1})} \quad (6.6)$$

$$\omega_{P3} = \frac{g_{m2}r_{o2}(C_L + C_{m1} + r_{AB}g_{m3}C_{m1})}{r_{AB}C_{m1}C_L} \quad (6.7)$$

$$\omega_{z1} = \frac{g_{m2}g_{m3}r_{AB}}{g_{m2}g_{m3}r^2_{AB}C_{m2} - C_{m1}} \quad (6.8)$$

$$\omega_{z2} = -\frac{g_{m2}r_{o2}g_{m3}r^2_{AB}C_{m2} - r_{o2}C_{m1}}{C_{m1}C_{m2}r^2_{AB}} \quad (6.9)$$

Equation 6.10 gives the value of GBW, which is the multiplication of dc gain A_{dc} and dominant pole frequency ω_{P1}.

$$GBW = A_{dc}.\ \omega_{P1} = \frac{g_{m1}}{C_{m1}} \quad (6.10)$$

It is pertinent to mention that any circuit is unconditionally stable only when it does not have any RHP pole. In this context, the proposed amplifier 10 is unconditionally stable since it does not have any RHP pole. Further, RHP zero reduces the phase margin of the circuit, but for the proposed amplifier 10, the RHP zero ω_{z2} is shifted to a very high frequency since it is multiplied with the

second stage gain $g_{m2}r_{o2}$. As a result, this RHP zero will not disturb the phase margin. As a consequence, the stability of the proposed amplifier improves.

6.2.3 Simulation results and discussions

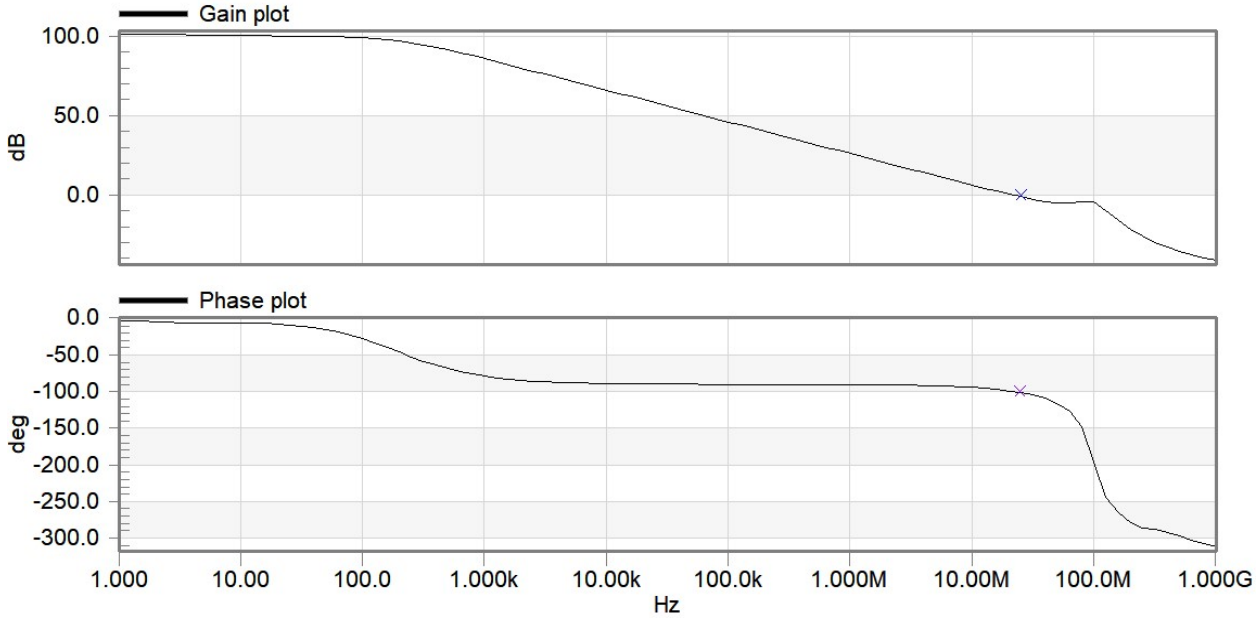
The proposed amplifier 10 is functionally verified through simulations using 0.18 µm technology parameters. Table 6.1 gives the design parameters for the proposed amplifiers 10.

Table 6.1 Design parameters of proposed amplifier 10

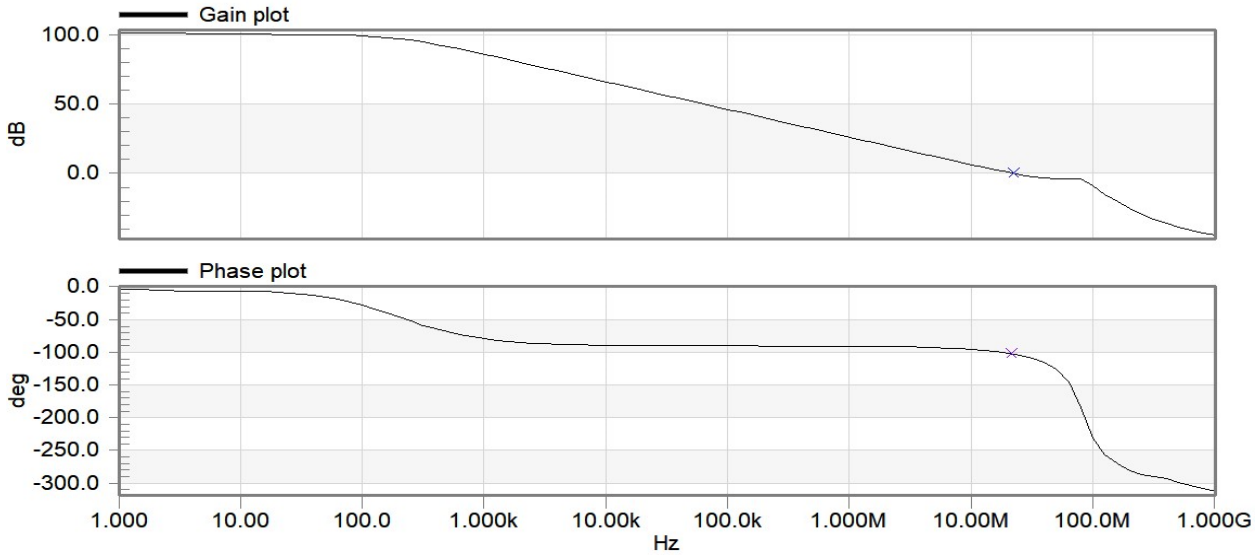
Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M2, M15, M16: W= 20 µm, L=1 µm; M3, M4: W= 100 µm, L=0.35 µm M5, M6, M7: W= 60 µm, L=0.35 µm; M8: W= 10 µm, L= 1 µm M9: W= 60 µm, L= 1 µm; M10, M12: W= 5 µm, L= 1 µm; M11: W= 35 µm, L= 1 µm; M13: W= 12 µm, L= 0.35 µm; M14: W= 150 µm, L= 0.35 µm; M17: W= 5 µm, L= 0.35 µm M18, M19: W= 25 µm, L= 1 µm M20: W= 1 µm, L= 1 µm
C_{m1} C_{m2}	12.5 pF 0.5 pF
R	13.5 KΩ
Biasing current (I_B)	10 µA
C_L	20 pF/ 30 pF

Figure 6.4 shows the frequency response of the proposed amplifier 10 at 20 pF and 30 pF load, respectively. The GBW is observed to be 25 MHz at 20 pF load, while it is 22 MHz at 30 pF load for the amplifier. Further, the DC gain is 102 dB. Moreover, the proposed amplifier also provides the phase margin of 82° and 79° at 20 pF and 30 pF load, respectively, which suggests good stability. Figure 6.5 displays the unity gain step response for an input pulse of 1 V_{pp}. The slew rate

is found to be 10.42 V/µs at 20 pF load, whereas it is 10.1 V/µs at 30 pF load. Further, the proposed amplifier has a 1% settling time of 0.1µs. The frequency response of CMRR and PSRR at 20 pF and 30 pF load are presented in Fig. 6.6 and Fig. 6.7, respectively. The corresponding CMRR and PSRR are observed to be 87.6 dB and 85.6 dB .

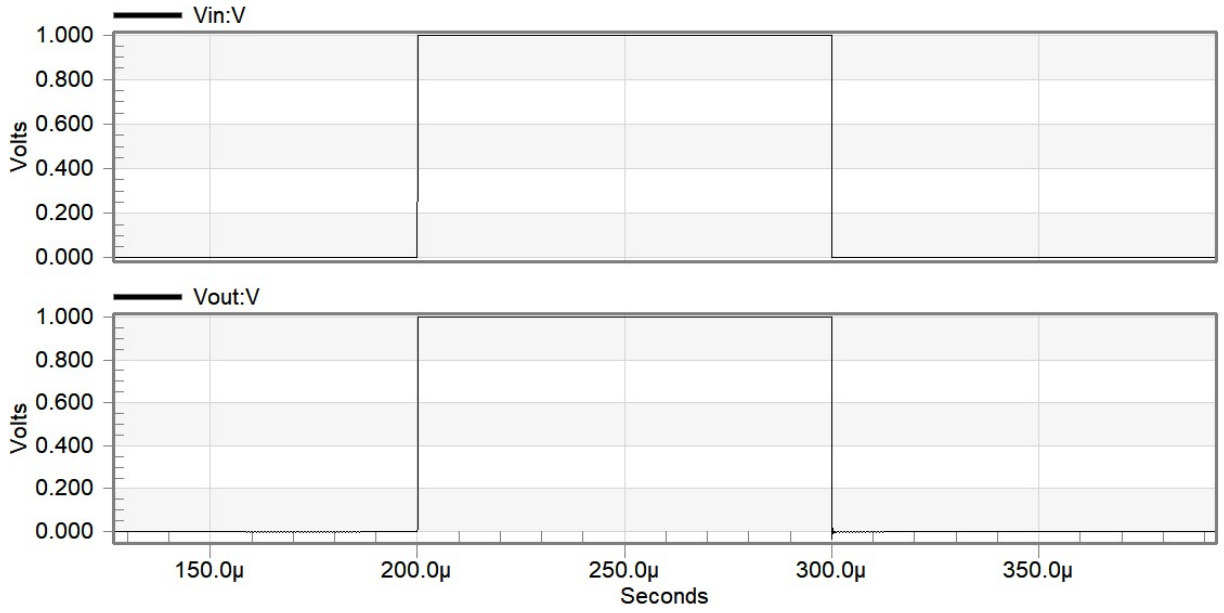


(a)

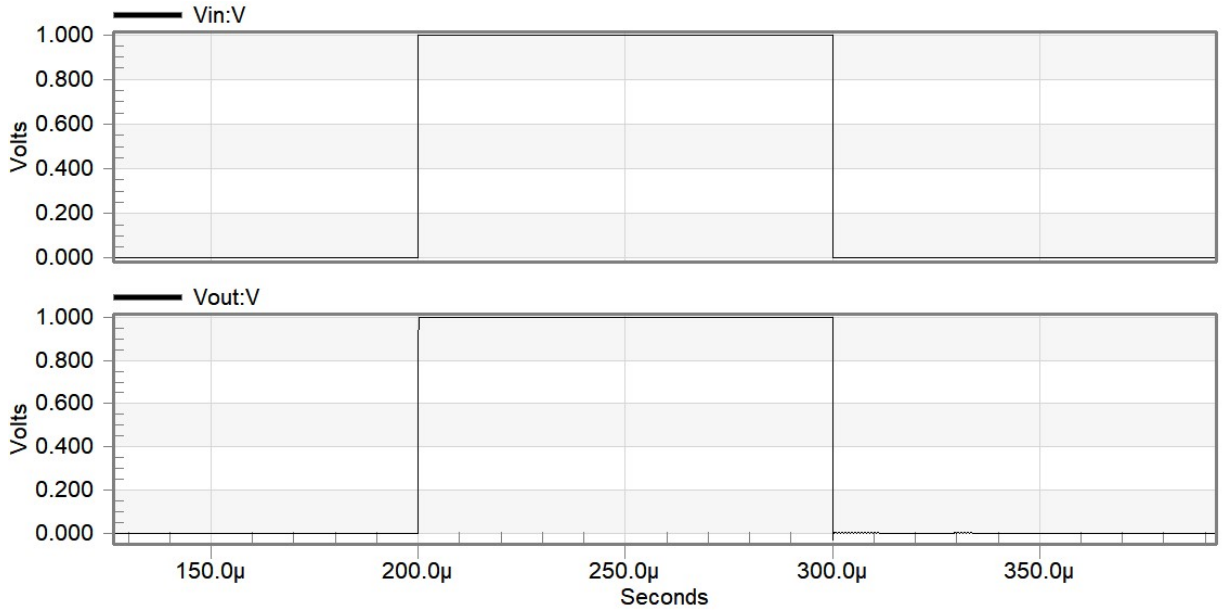


(b)

Fig. 6.4 Frequency response of proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load

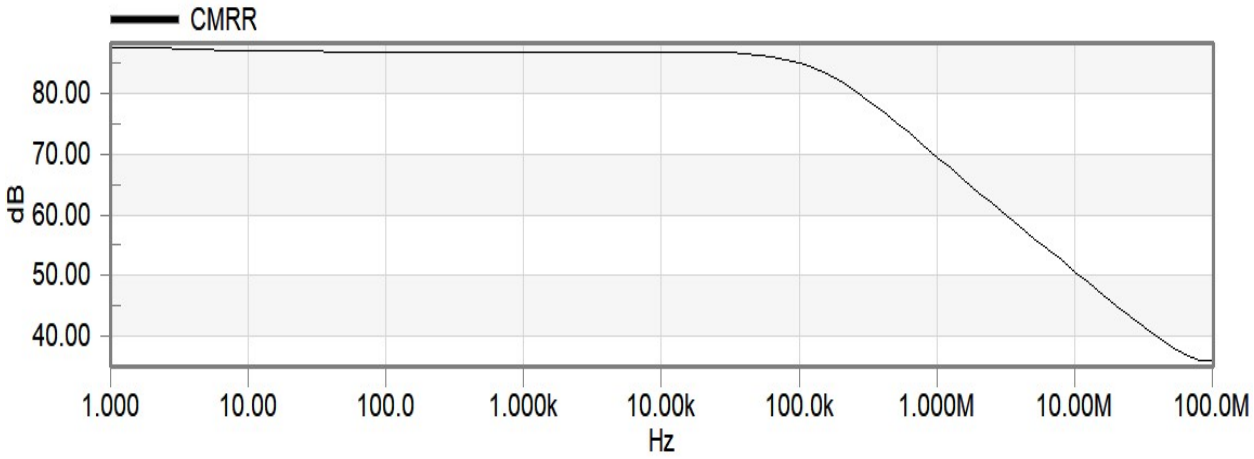


(a)

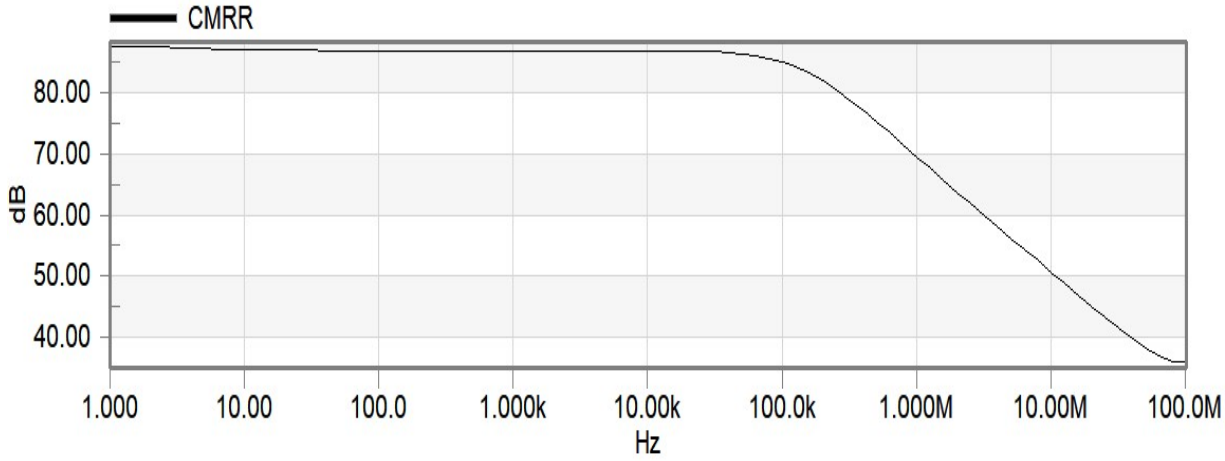


(b)

Fig. 6.5 Transient response of proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load

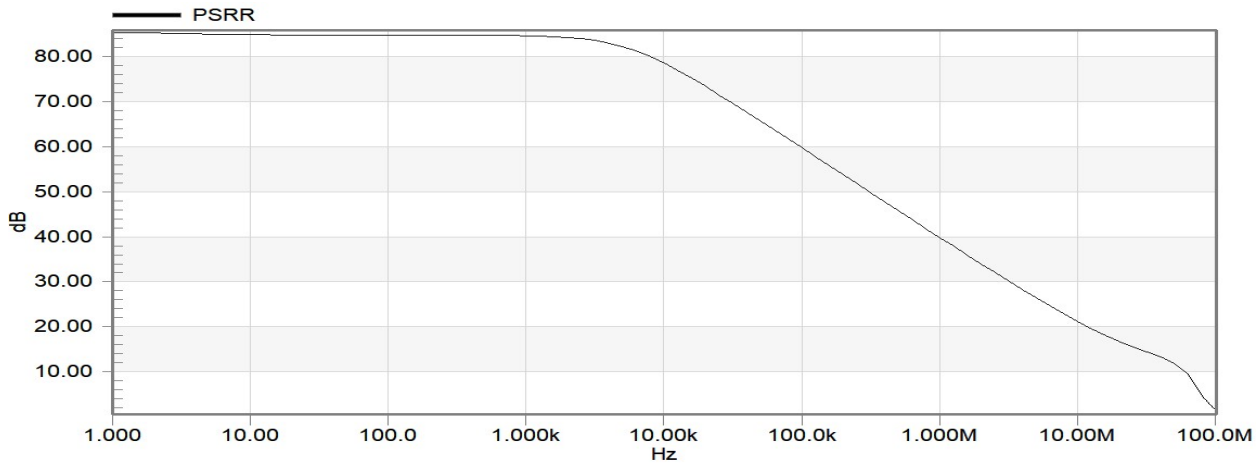


(a)

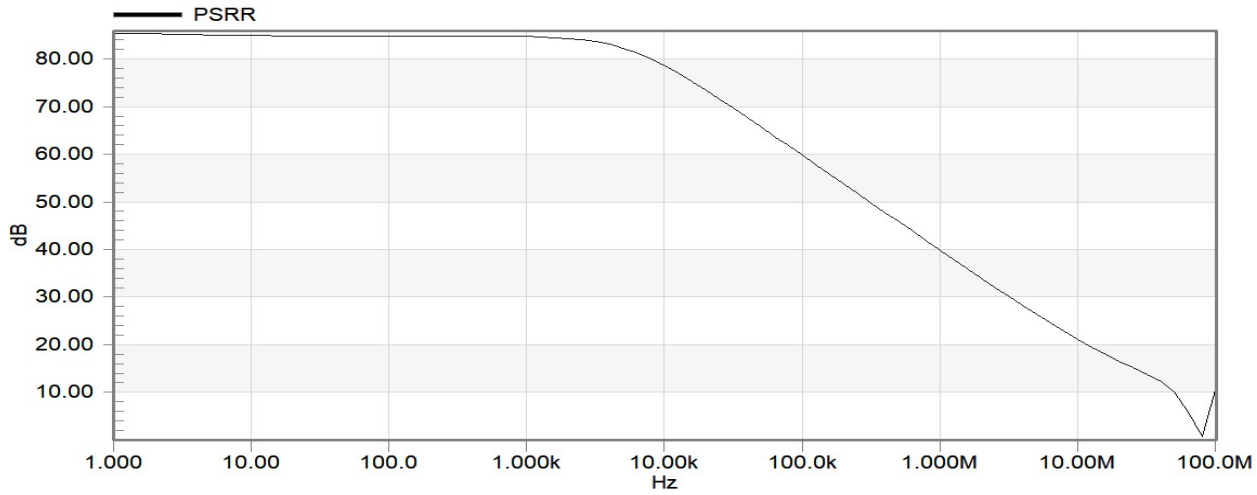


(b)

Fig. 6.6 Frequency response of CMRR for proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load



(a)

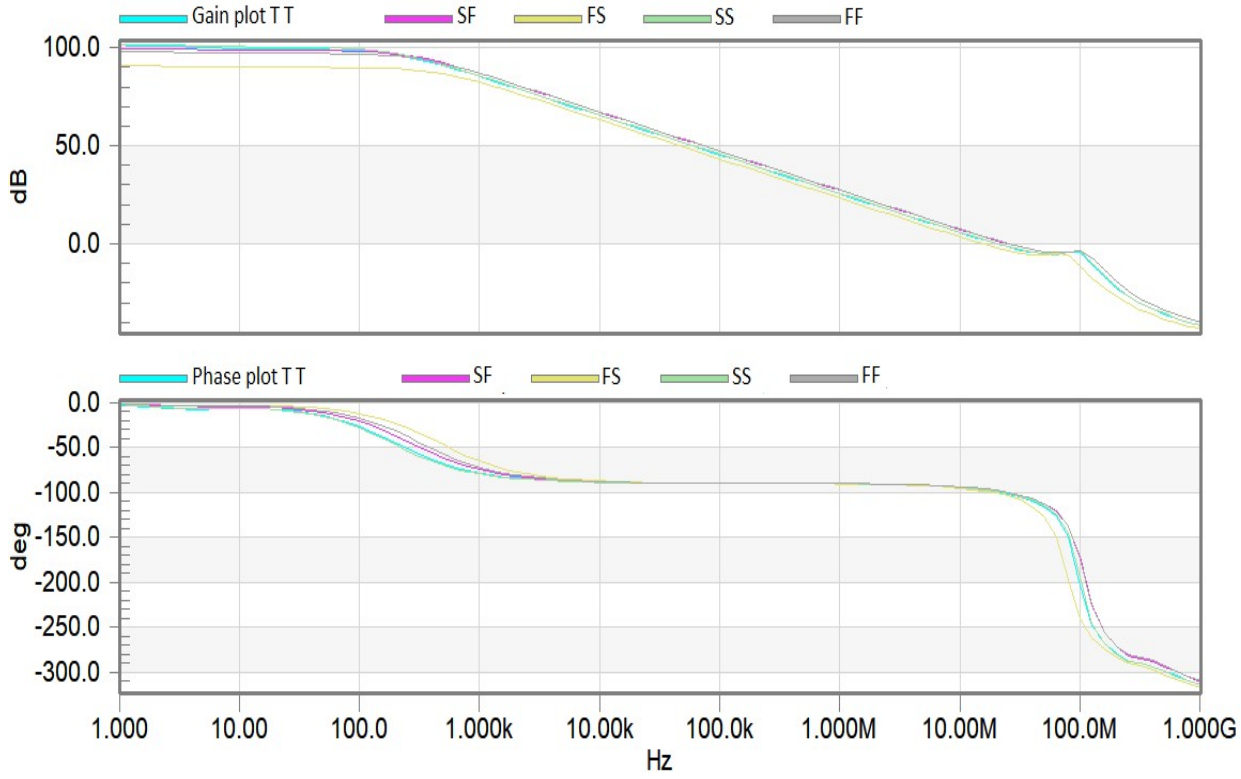


(b)

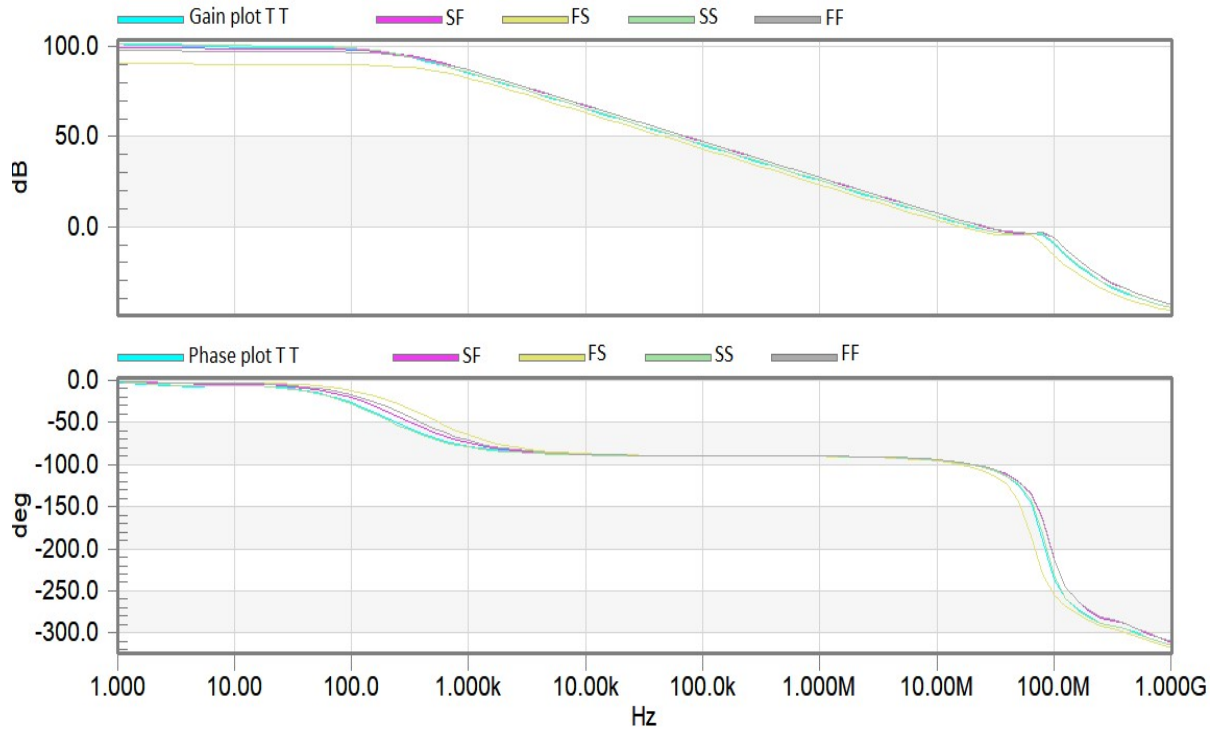
Fig. 6.7 Frequency response of PSRR for proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load

The impact of process variations on frequency response of the proposed amplifier 10, corner analysis has been performed at all five corners (TT, SF, FS, SS, and FF) and the findings are placed in Fig. 6.8 for 20 pF and 30 pF load. It can be seen that the highest variations in Gain, GBW, and PM are within 20%, except FS process corner of the proposed amplifier at 20 pF load, for which variations in GBW are 21.7 %. Variations are evaluated with reference to TT process corner. Additionally, the gain and phase plots of the amplifier with a supply voltage variation of ± 5 % have been shown in Fig. 6.9 The results are summarized in Table 6.2. The proposed amplifier 10

has maximum variations in gain, GBW, and PM of (1.96%, 20%, 2.1%). So, the maximum overall variation with respect to supply voltage is 20%. Moreover, the effect of power supply variation is examined through Monte-Carlo simulations with 5% Gaussian distribution and 200 runs. Figure 6.10 shows the frequency response of the amplifier at 20 pF and 30 pF load, respectively. The mean and standard deviations in gain are observed to be 102.33 dB and 6.13 dB for the proposed amplifier 10.

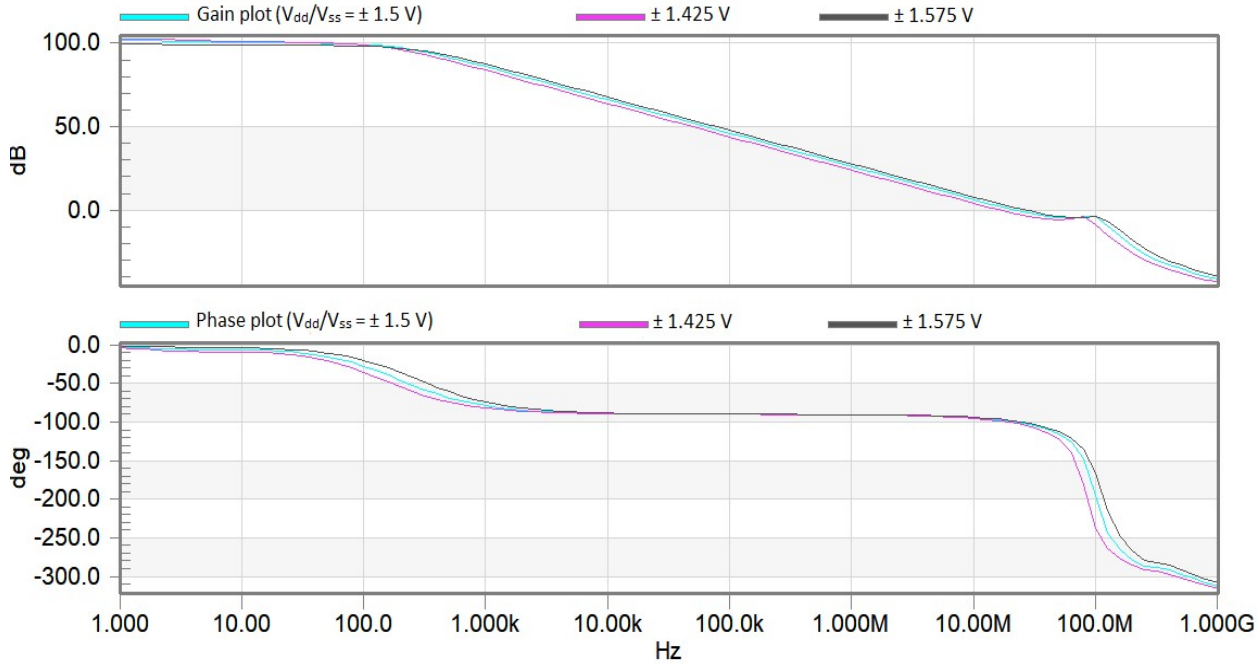


(a)

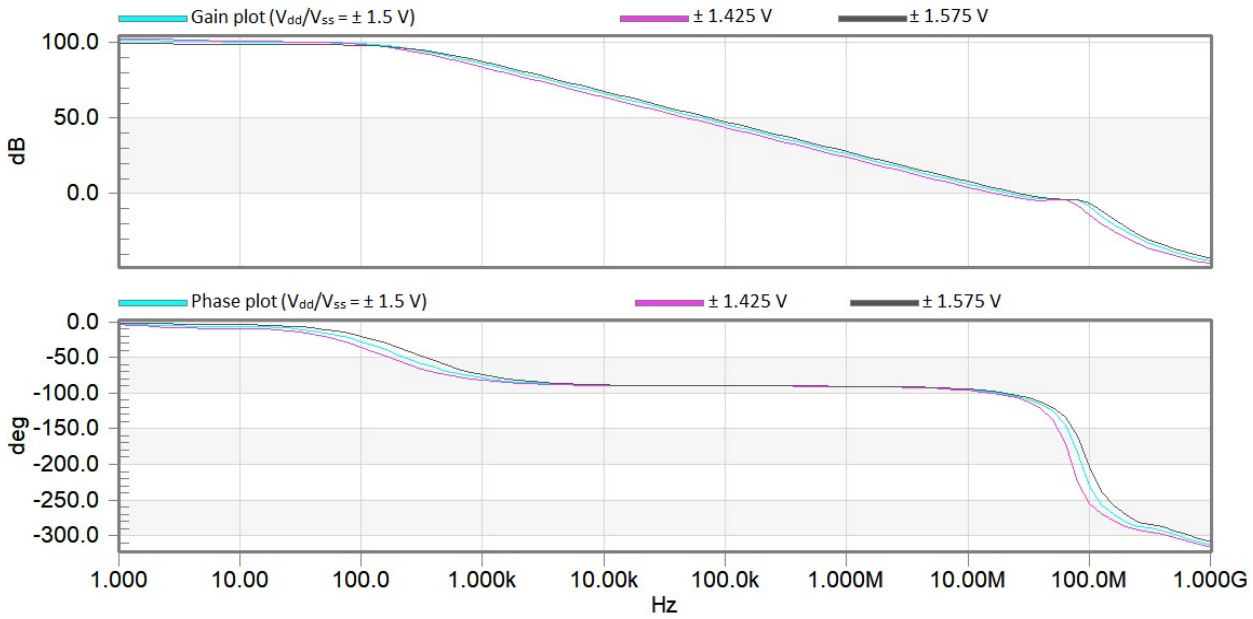


(b)

Fig. 6.8 Corner analysis of proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load



(a)

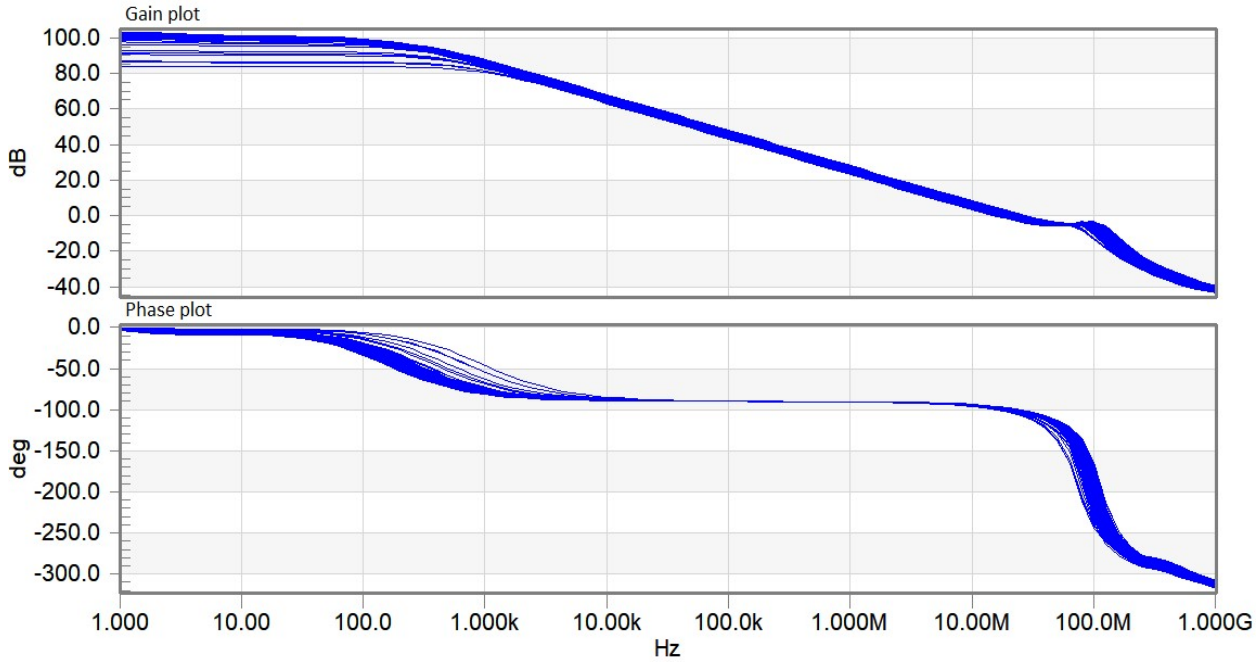


(b)

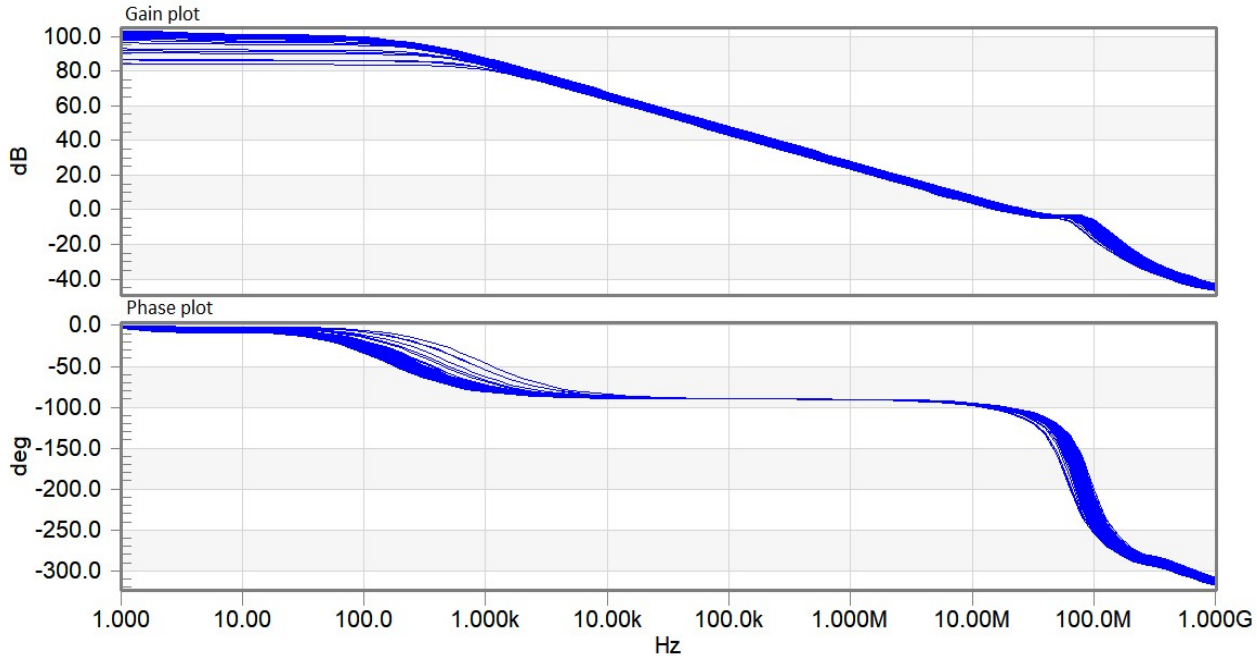
Fig. 6.9 Impact of supply voltage variations on proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load

Table 6.2 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 10

C_L	AC response metrics	Process Corner					V_{DD} variation (1.5 V ± 5% of 1.5 V)	
		TT	SF	FS	SS	FF	1.425V	1.575V
20 pF	Gain (dB)	102	100	91.5	103	98.7	104	100
	GBW (MHz)	23	26.1	18	20.8	26.1	20	26.1
	PM (°)	80.1	80.8	80.3	83.4	81.2	82	80.3
30 pF	Gain (dB)	102	100	91.5	103	98.7	104	100
	GBW (MHz)	20.8	24	17.3	21.2	24.5	17.6	26.1
	PM (°)	80	79	80.1	80.1	79	80.3	78



(a)



(b)

Fig. 6.10 Monte-Carlo simulation for frequency response of proposed amplifier 10 (a) at 20 pF load (b) at 30 pF load against V_{DD} variations

6.3 Proposed amplifier 11

The block diagram of the proposed amplifier 11 is shown in Fig. 6.11. The three stages are connected in a cascading manner. The proposed amplifier 11 utilizes RNMC, in which two compensation capacitors, C_{m1} and C_{m2}, are connected in the outer and inner compensation loops, respectively. Further, the proposed amplifier 11 makes use of class AB FVF in the inner loop to break the forward path, which resolves the RHP zero issue. The feed forward path and slew rate enhancer circuit are exploited to improve the transient response of the amplifier.

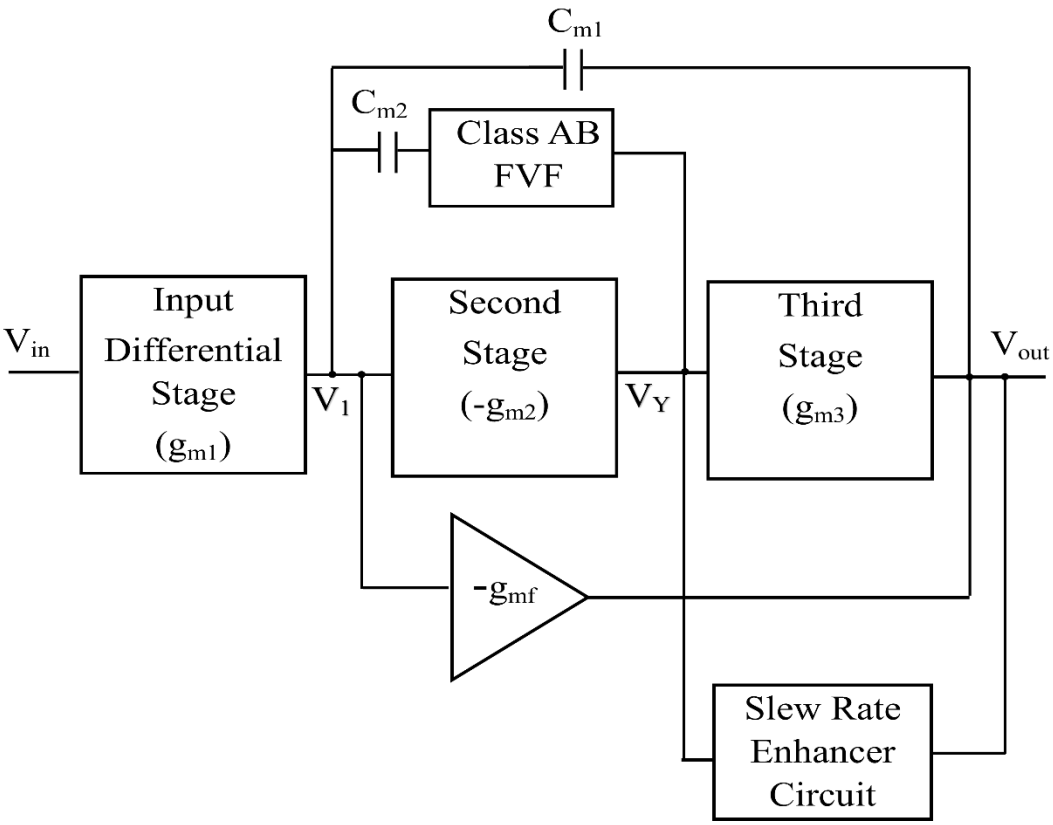


Fig. 6.11 Block diagram of proposed amplifier 11

6.3.1 Circuit description of proposed amplifier 11

Figure 6.12 describes the transistor level circuit of the proposed amplifier 11. Transistors M2 and M3-M6 form the first stage, which is the differential amplifier. The second stage is the common source amplifier (transistors M7-M8). Further, class AB FVF is made up of transistors M9-M12. The third stage is the non-inverting stage, which is formed by the transistors M13-M16. Further, the feed forward path is implemented by connecting the output of the first stage to the gate terminal

of the transistor M14. It forms the push pull output stage. The slew rate enhancer circuit is connected between the output of the second stage (V_Y) and the third stage. The push pull output stage and slew rate enhancer circuit improve the transient response of the amplifier. The advantage of the proposed amplifier 11 is its enhanced slew rate.

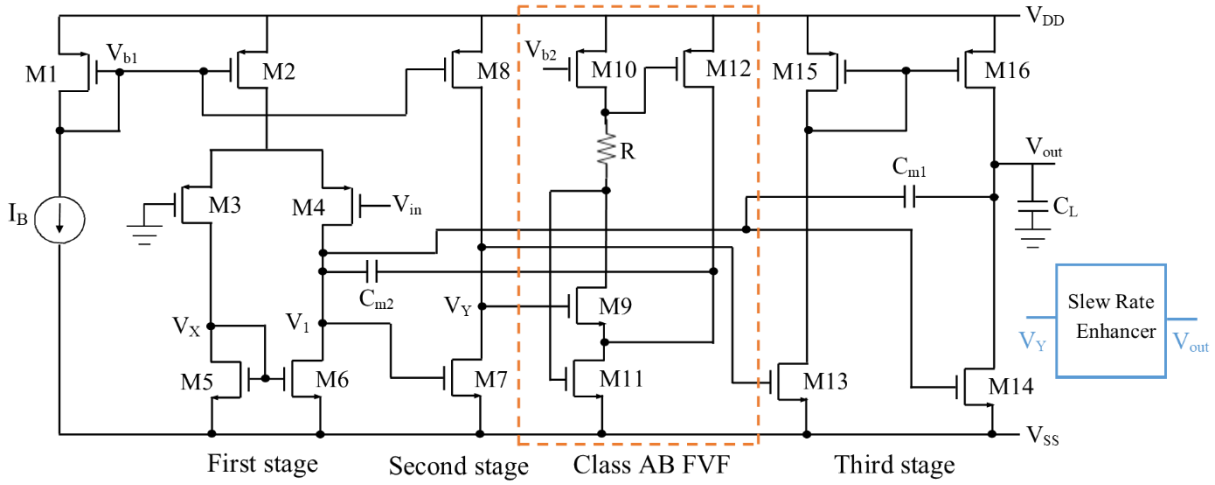


Fig. 6.12 Transistor level implementation of proposed amplifier 11

6.3.2 Small signal analysis of proposed amplifier 11

To perform the small signal analysis, a small signal model of the proposed amplifier 11 is shown in Fig. 6.13. It helps in finding the poles, zeros, DC gain, and GBW. The following assumptions are made to simplify the calculations.

$$g_{mi}r_{oi} >> 1 \tag{6.11}$$

$$C_L, C_{m1}, C_{m2} >> C_1, C_2 \tag{6.12}$$

Where g_{mi} and r_{oi} are the transconductance and output resistance of the i^{th} stage; i = 1, 2, and 3. C_1 and C_2 represent the output capacitance of the first stage and second stage, respectively, whereas C_L is the load capacitance.

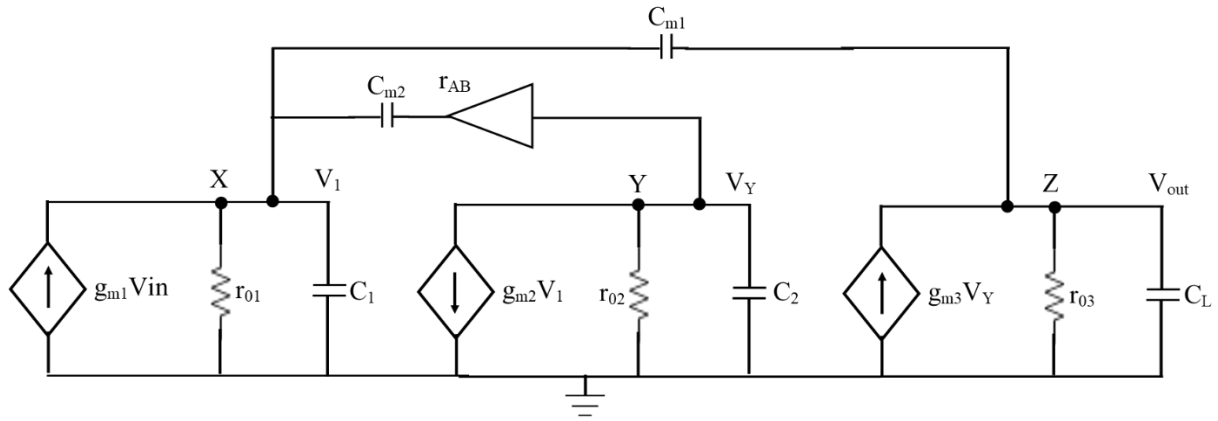


Fig. 6.13 Small signal model of proposed amplifier 11

Eq. 6.13 represents the transfer function of the proposed amplifiers 11.

$$A(s) = \frac{A_{dc}}{\left(1+\frac{s}{\omega p1}\right)} \frac{\left[1+\left(r_{AB}C_{m2}-\frac{C_{m1}}{r_{AB}g_{m2}g_{m3}}\right)s-\left(\frac{r_{AB}C_{m1}C_{m2}}{r_{o2}g_{m2}g_{m3}}\right)s^2\right]}{\left[1+\frac{C_{m2}(r_{AB}g_{m3}C_{m1}+C_L+C_{m1})}{g_{m3}C_{m1}}s+\left(\frac{r_{AB}C_LC_{m2}}{r_{o2}g_{m2}g_{m3}}\right)s^2\right]} \quad (6.13)$$

A_{dc} denotes the DC gain of the amplifier and is given by Eq. 6.14.

$$A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3} \quad (6.14)$$

The denominator of Eq. 6.13 gives a dominant pole ω_{p1} and two non-dominant poles $\omega_{p2,}$ ω_{p3}. Moreover, one LHP zero ω_{z1} and one RHP zero ω_{z2} are provided by the numerator of Eq. 6.13. All poles and zeros are described by Eqs. 6.15-6.19.

$$\omega_{p1} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}} \quad (6.15)$$

$$\omega_{p2} = \frac{g_{m3}C_{m1}}{C_{m2}(C_L + C_{m1} + r_{AB}g_{m3}C_{m1})} \quad (6.16)$$

$$\omega_{p3} = \frac{g_{m2}r_{o2}(C_L + C_{m1} + r_{AB}g_{m3}C_{m1})}{r_{AB}C_{m1}C_L} \quad (6.17)$$

$$\omega_{z1} = \frac{g_{m2}g_{m3}r_{AB}}{g_{m2}g_{m3}r^2_{AB}C_{m2} - C_{m1}} \quad (6.18)$$

$$\omega_{z2} = - \frac{g_{m2} r_{o2} g_{m3} r^2_{AB} C_{m2} - r_{o2} C_{m1}}{C_{m1} C_{m2} r^2_{AB}} \quad (6.19)$$

Equation 6.20 gives the value of GBW, which is the multiplication of dc gain A_{dc} and dominant pole frequency ω_{p1}.

$$GBW = A_{dc}.\omega_{p1} = \frac{g_{m1}}{C_{m1}} \quad (6.20)$$

It is pertinent to mention that any circuit is unconditionally stable only when it does not have any RHP pole. In this context, the proposed amplifier 11 is unconditionally stable since it does not have any RHP pole. Further, RHP zero reduces the phase margin of the circuit, but for the proposed amplifier 11, the RHP zero ω_{z2} is shifted to a very high frequency since it is multiplied with the second stage gain $g_{m2}r_{o2}$. As a result, this RHP zero will not disturb the phase margin. As a consequence, the stability of the proposed amplifier improves.

6.3.3 Simulation results and discussions

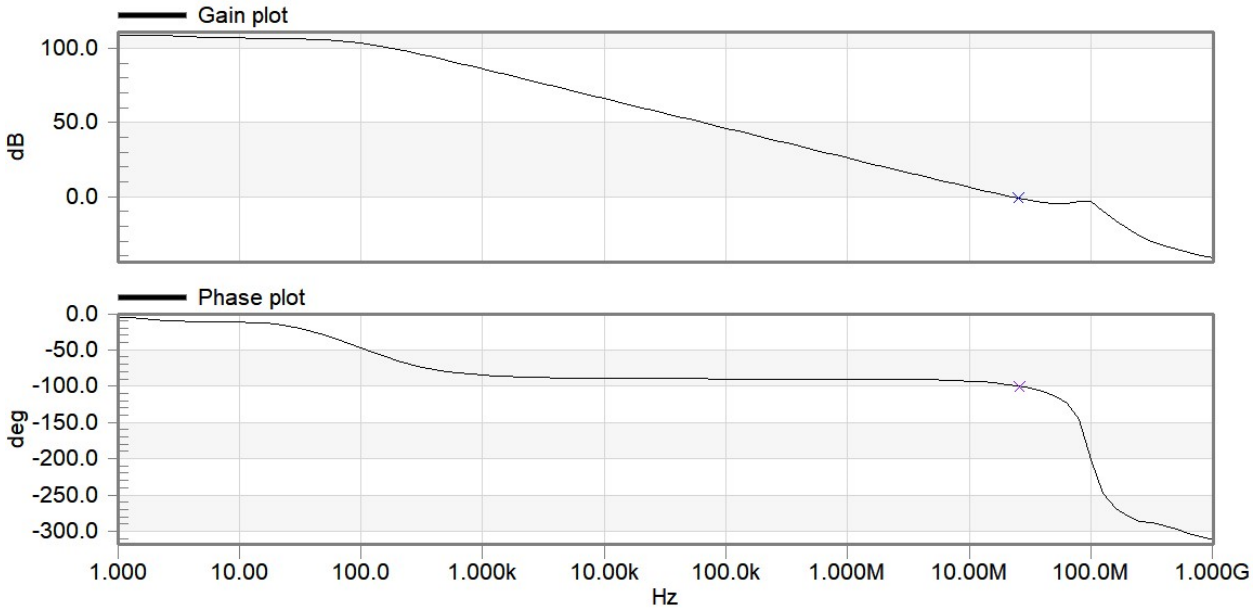
The proposed amplifier 11 is functionally verified through simulations using 0.18 µm technology parameters. Table 6.3 gives the design parameters for the proposed amplifiers 11.

Table 6.3 Design parameters of proposed amplifier 11

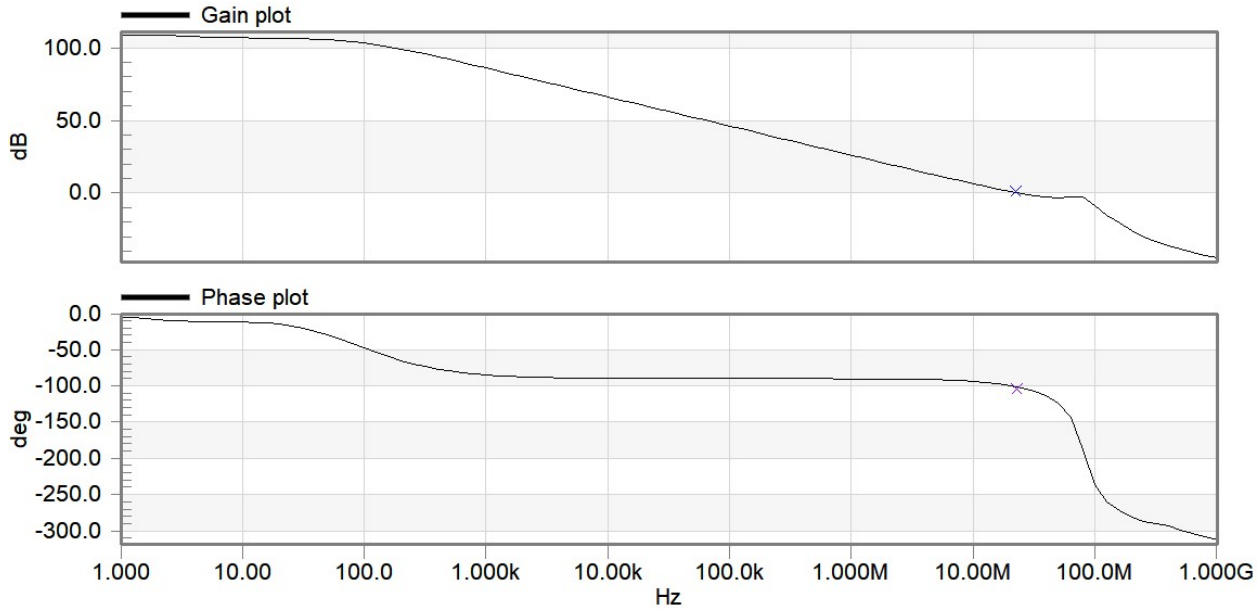
Parameters	**Value**
Technology	0.18 µm
Transistor dimensions	M1, M2, M15, M16: W= 20 µm, L=1 µm; M3, M4: W= 100 µm, L=0.35 µm M5, M6, M7: W= 60 µm, L=0.35 µm; M8: W= 10 µm, L= 1 µm M9: W= 60 µm, L= 1 µm; M10, M12: W= 5 µm, L= 1 µm; M11: W= 35 µm, L= 1 µm; M13: W= 12 µm, L= 0.35 µm; M14: W= 150 µm, L= 0.35 µm; M17: W= 0.5 µm, L= 0.35 µm M18, M19: W= 25 µm, L= 1 µm

	M20: W= 1 µm, L= 1 µm
C_{m1} C_{m2}	12.5 pF 0.5 pF
R	13.5 KΩ
Biasing current (I_B)	10 µA
C_L	20 pF/ 30 pF

Figure 6.14 shows the frequency response of the proposed amplifier 11 at 20 pF and 30 pF load. For the proposed amplifier 11, the GBW is observed to be 25 MHz at 20 pF load, while it is 22 MHz at 30 pF. Further, the DC gain is 110 dB for the proposed amplifier 11. Moreover, the proposed amplifier also provides the phase margin of 82° and 79° at 20 pF and 30 pF load, respectively, which suggests good stability. Figure 6.15 displays the unity gain step response at 20 pF and 30 pF load for an input pulse of 1 V_{pp}. The slew rate is found to be 10.8 V/µs at 20 pF load, whereas it is 10.56 V/µs at 30 pF load. Further, the proposed amplifier has a 1% settling time of 0.1 µs. The frequency response of CMRR is presented in Fig. 6.16 at 20 pF and 30 pF load. The CMRR is 87.8 dB for the proposed amplifier 11. The PSRR graph is shown in Fig. 6.17. It can be confirmed that the PSRR for the proposed amplifier 11 is 87.4 dB.

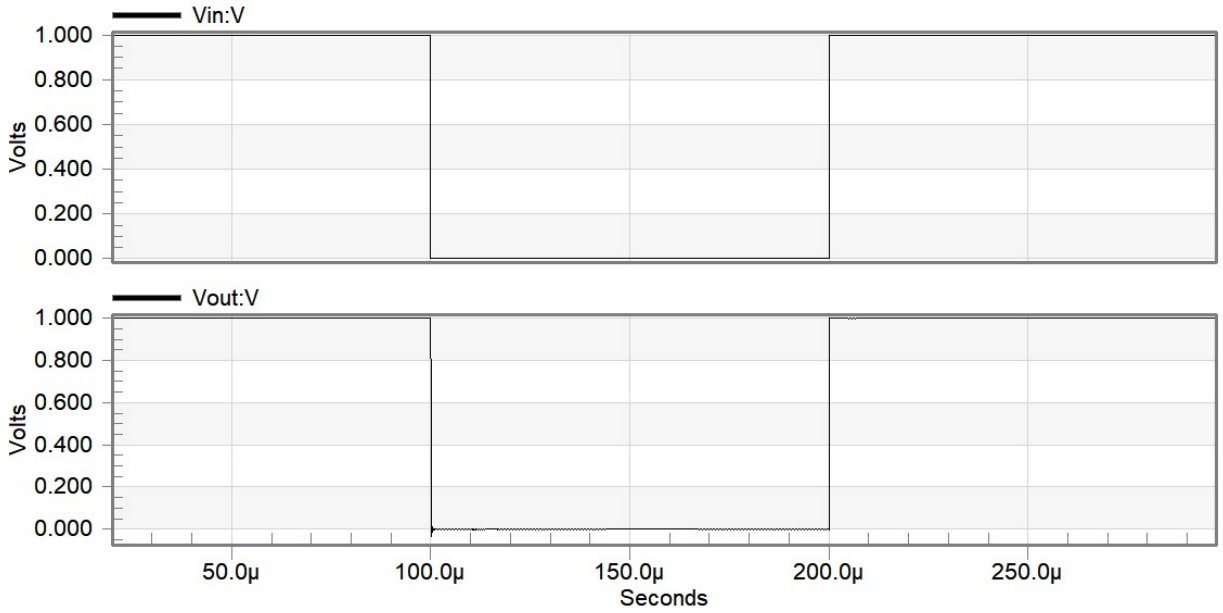


(a)

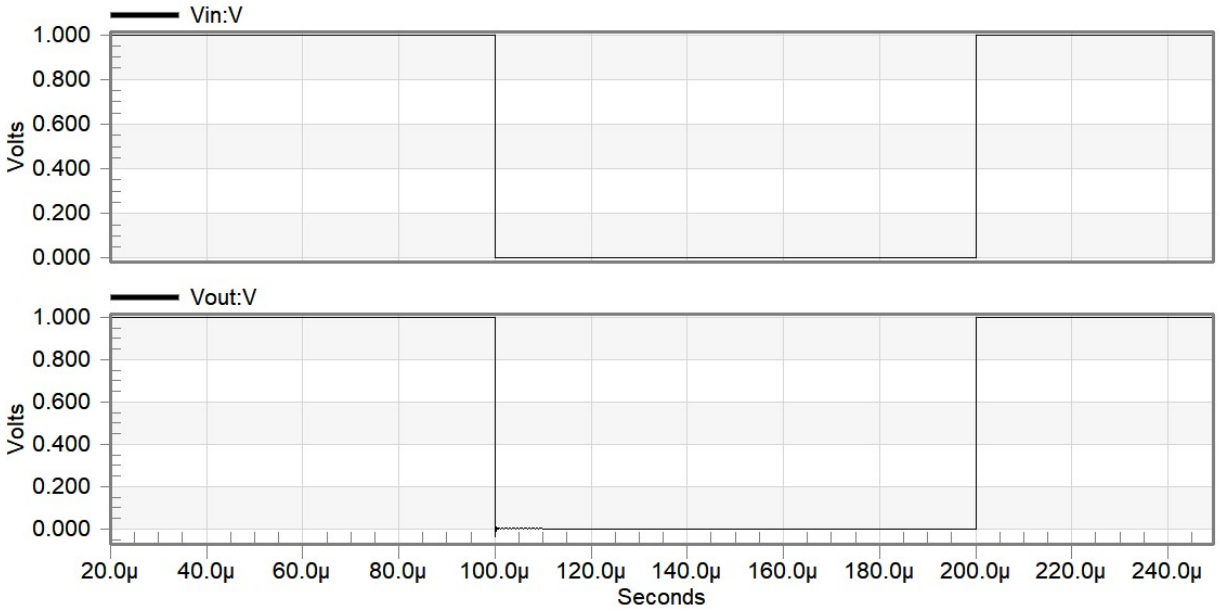


(b)

Fig. 6.14 Frequency response of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load

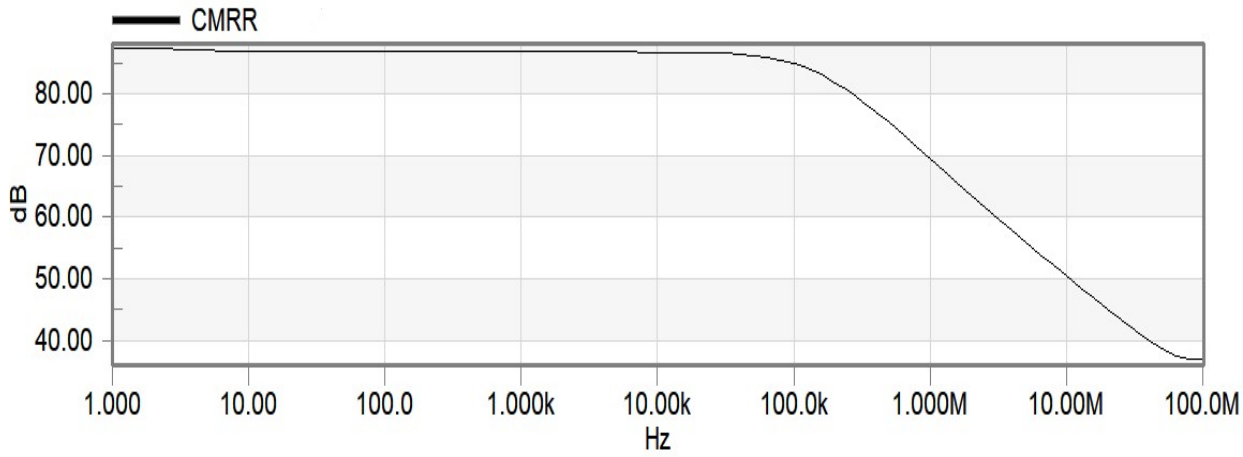


(a)

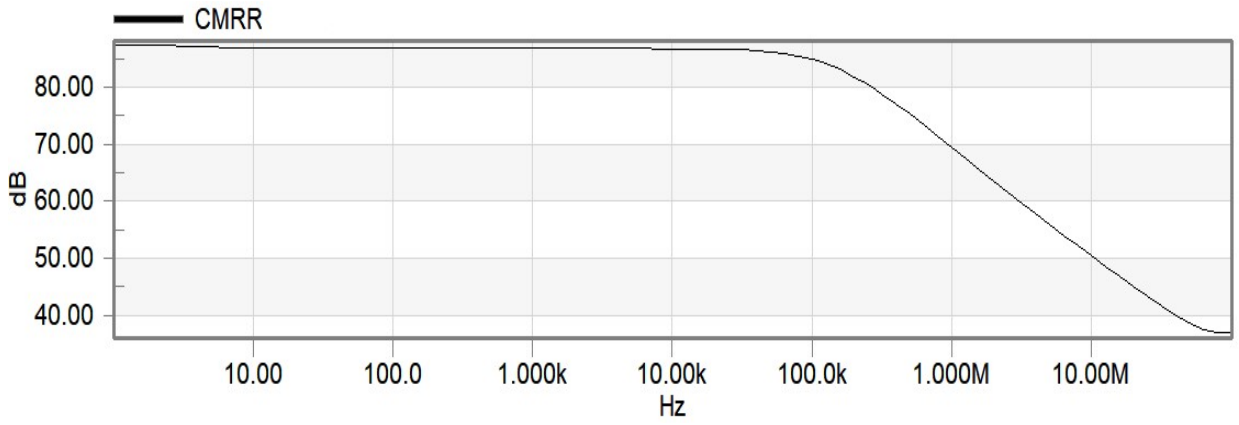


(b)

Fig. 6.15 Transient response of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load

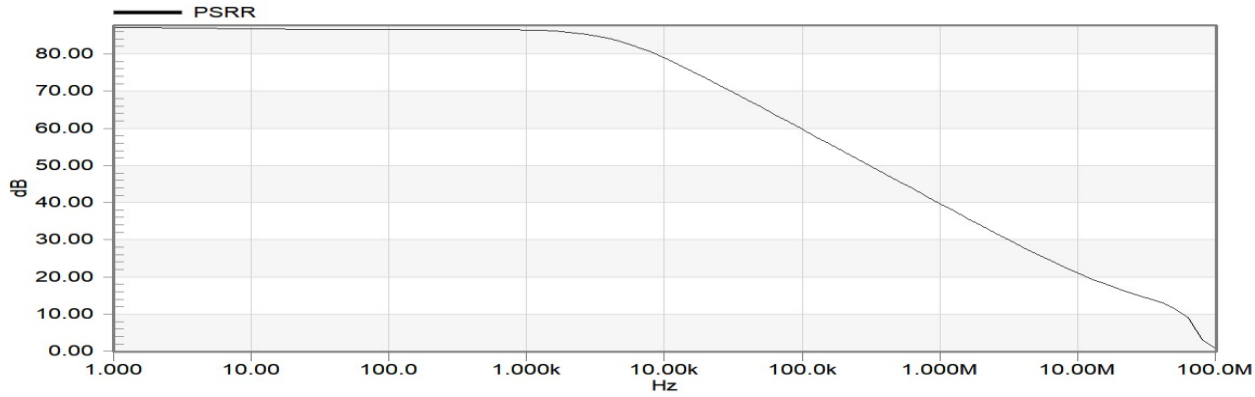


(a)

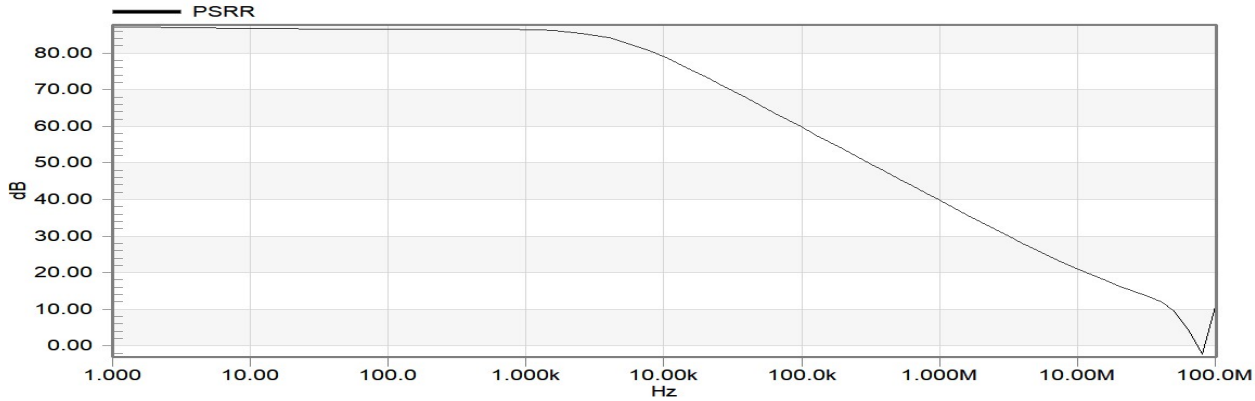


(b)

Fig. 6.16 Frequency response of CMRR of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load



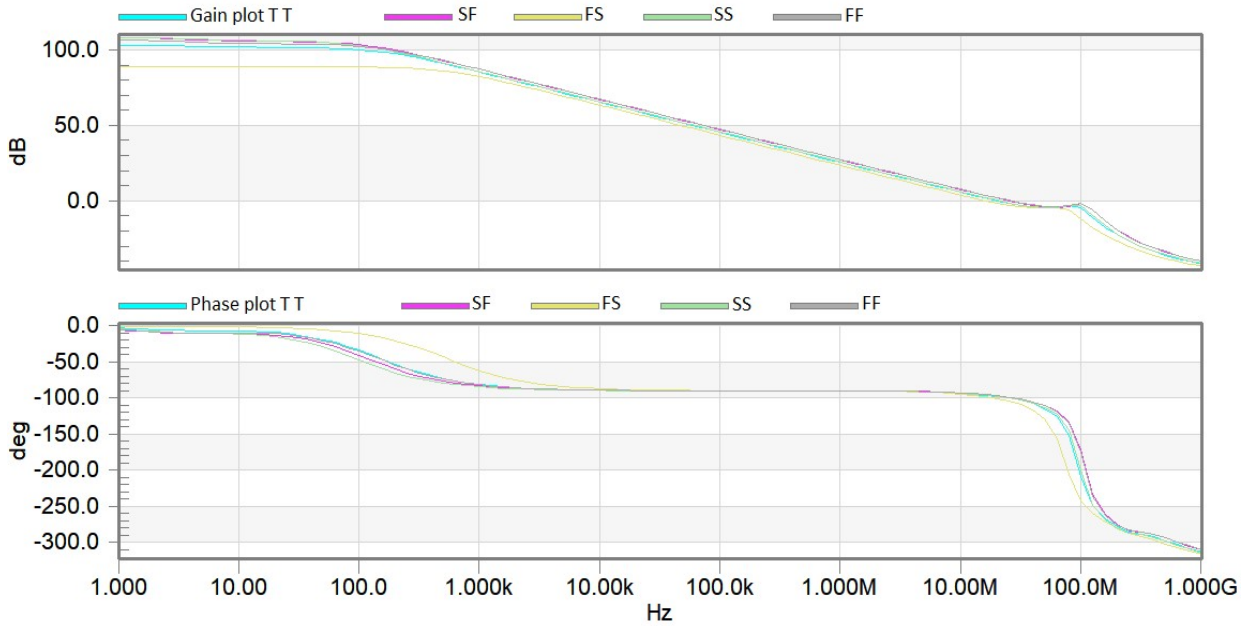
(a)



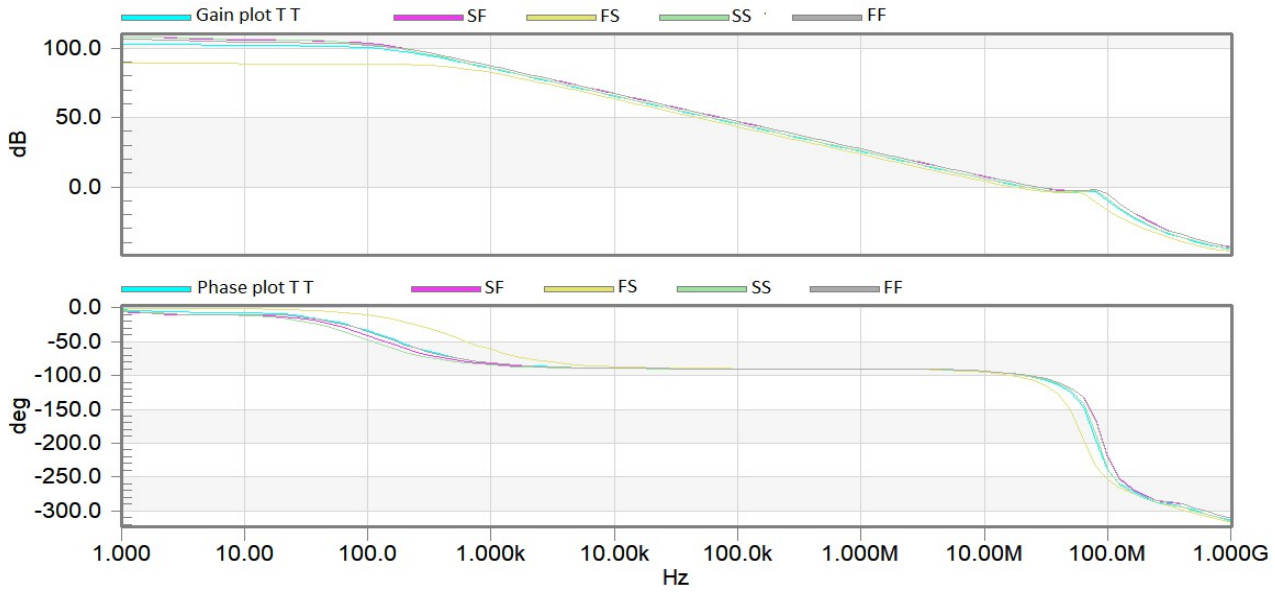
(b)

Fig. 6.17 Frequency response of PSRR of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load

To determine the frequency response of the proposed amplifier 11 under variations in process parameters, corner analysis has been performed at all five corners (TT, SF, FS, SS, and FF). Figure 6.18 displays the corner analysis at 20 pF and 30 pF load. It can be seen that the highest variations in Gain, GBW, and PM are within 20%, except FS process corner at 20 pF load, for which variations in GBW are 21.7 %. These variations are evaluated with reference to TT process corner. Additionally, the gain and phase plots of the proposed amplifier with a supply voltage variation of ± 5 % have been shown in Fig. 6.19. The results are summarized in Table 6.4. The proposed amplifier 11 has maximum variations in gain, GBW, and PM of (3.64%, 20.9%, 1.59%). So, the maximum overall variation with respect to supply voltage is 20.9%. Moreover, the effect of power supply variation is examined through Monte-Carlo simulations with 5% Gaussian distribution and 200 runs. Figure 6.20 shows the frequency response at 20 pF and 30 pF load. The mean and standard deviations in gain are observed to be 113.98 dB and 13.85 dB for the proposed amplifier 11.

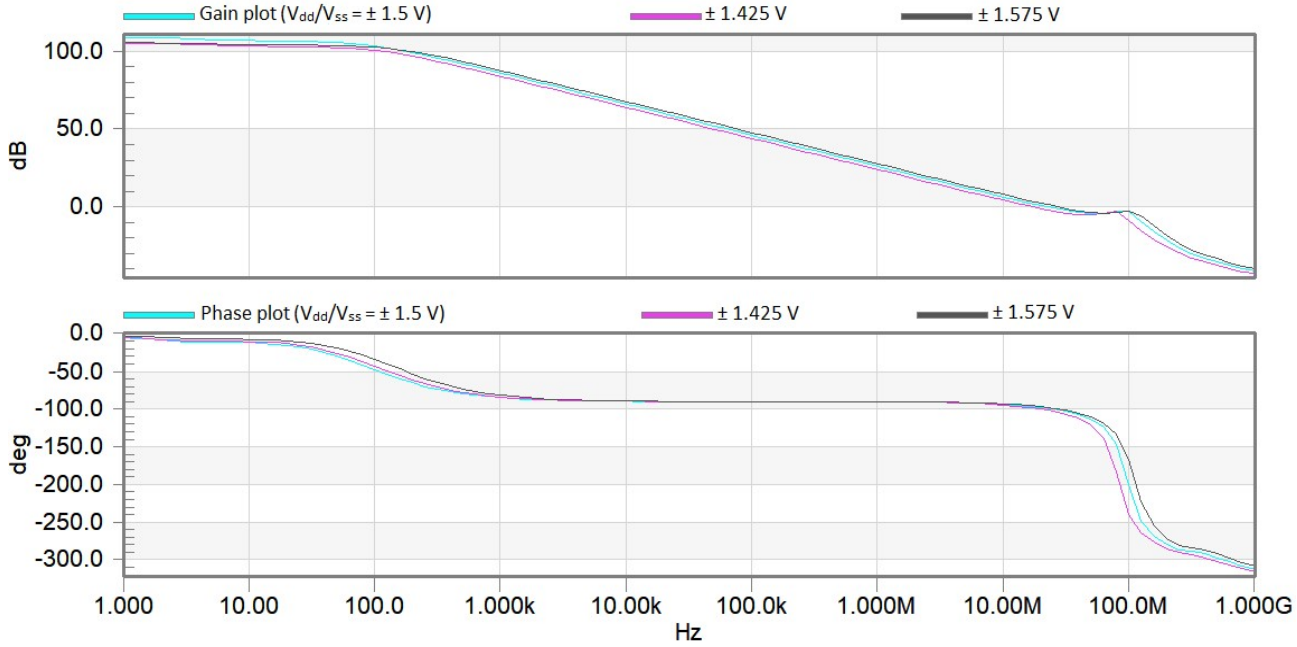


(a)

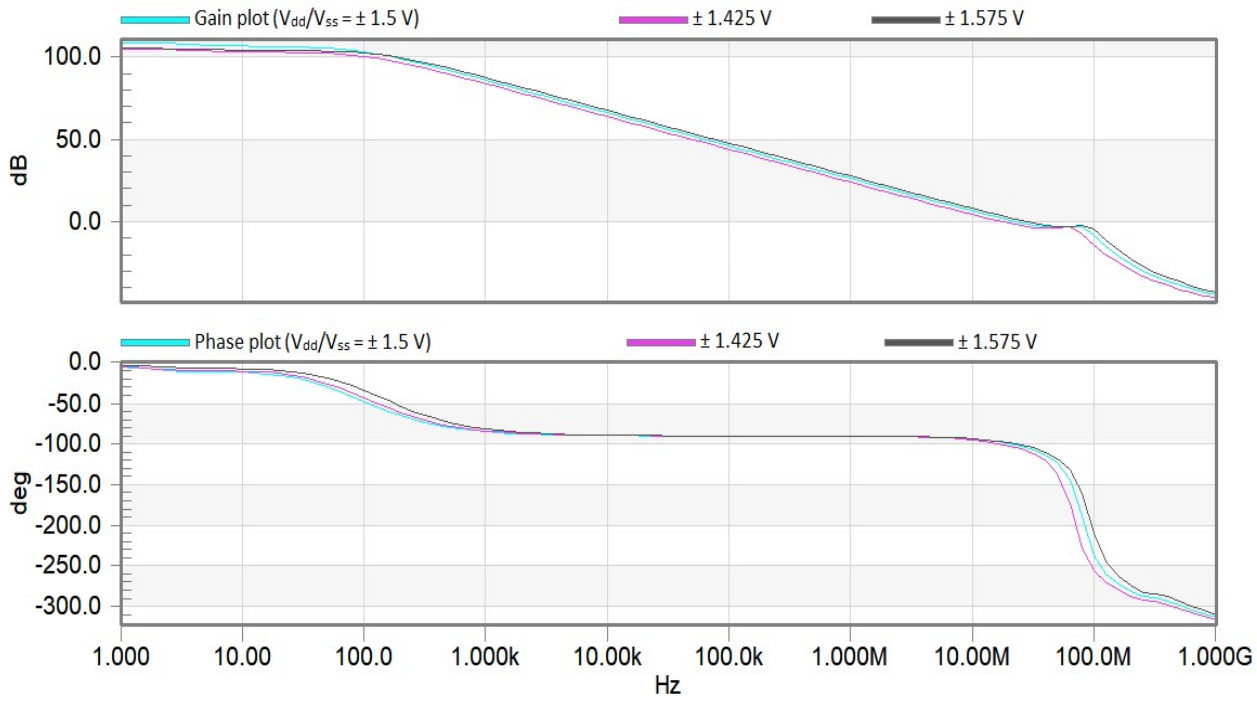


(b)

Fig. 6.18 Corner analysis of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load



(a)

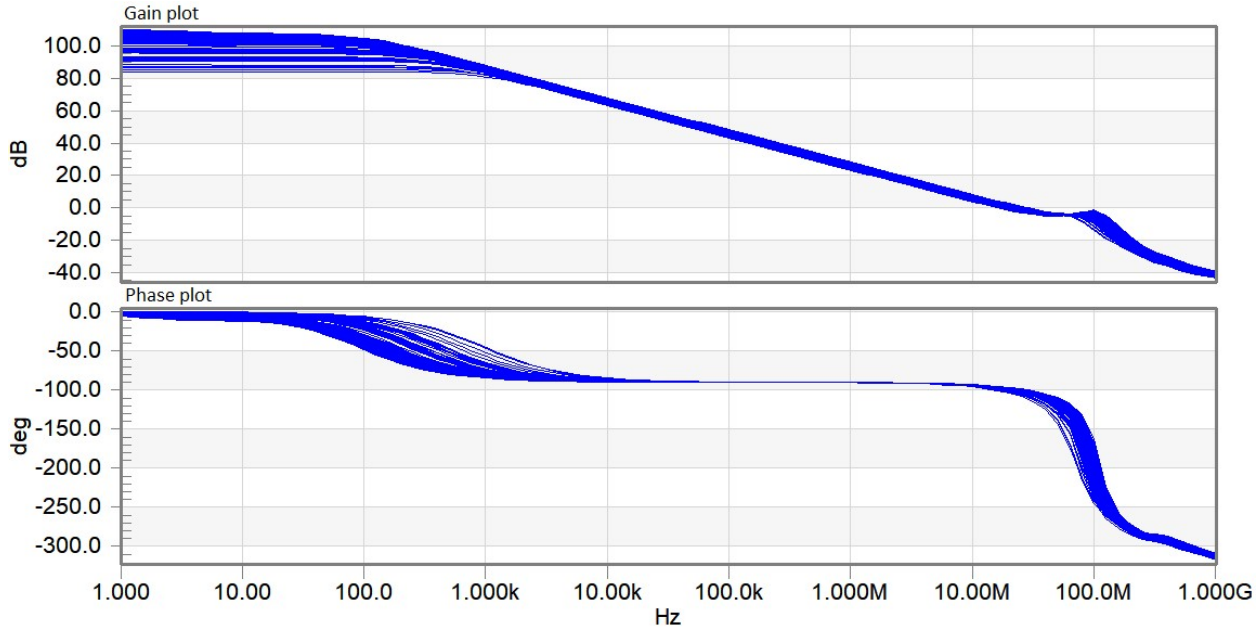


(b)

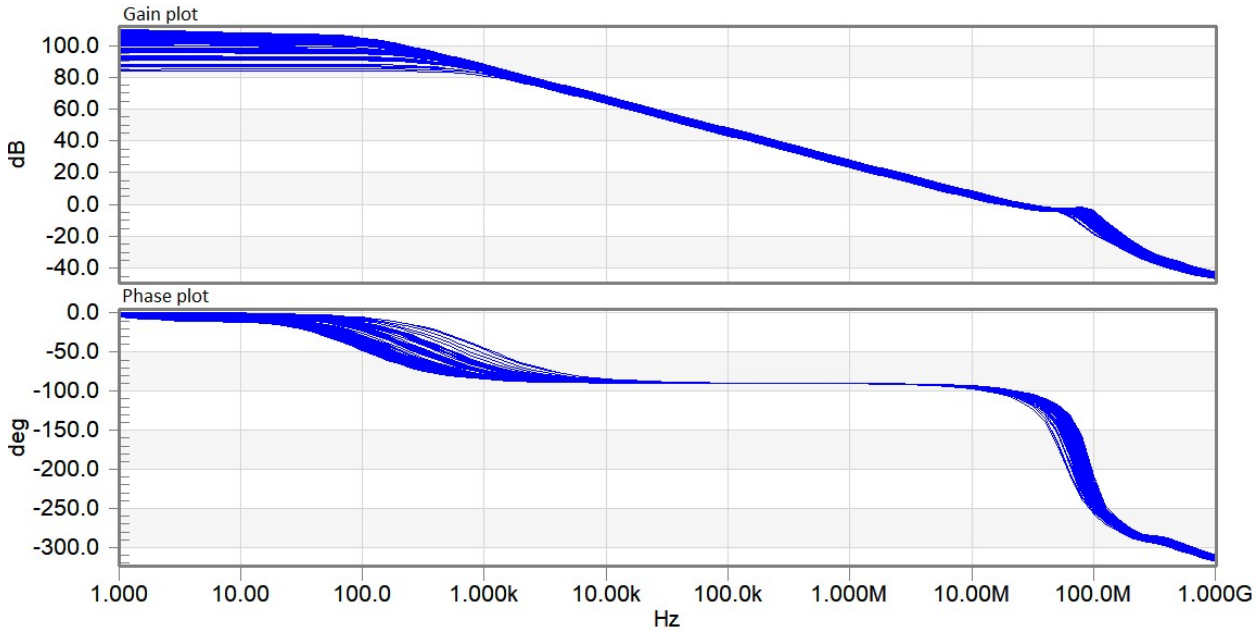
Fig. 6.19 Impact of supply voltage variations on proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load

Table 6.4 Summary of simulation results at different process corners and supply voltage variation for proposed amplifier 11

C_L	AC response metrics	Process Corner					V_{DD} variation (1.5 V ± 5% of 1.5 V)	
		TT	SF	FS	SS	FF	1.425V	1.575V
	PM (°)	80	79	80.1	80.1	79	80.3	78
20 pF	Gain (dB)	104	109	89.7	109	107.4	106	106.3
	GBW (MHz)	22.1	26.5	17.3	20.8	25.5	20.4	28.8
	PM (°)	83.7	81.4	81.2	83.7	81.7	83.3	80.7
30 pF	Gain (dB)	104	109	89.7	109	107.4	106	106.3
	GBW (MHz)	21.6	24.5	18.4	22.5	25	18	26.6
	PM (°)	81.9	81.1	79	82	80	80.1	79



(a)



(b)

Fig. 6.20 Monte-Carlo simulation for frequency response of proposed amplifier 11 (a) at 20 pF load (b) at 30 pF load against V_{DD} variations

6.4 Comparison

Table 6.5 compares the proposed amplifiers 10 and 11 with other work at 20 pF and 30 pF loads. It can be seen that the proposed amplifiers offer the highest GBW and DC gain in comparison with other amplifiers. Further, the proposed amplifiers provide good phase margin, ensuring better stability of the amplifiers. Moreover, the slew rate of the proposed amplifiers 10 and 11 is highest at 20 pF and 30 pF load. FOM_S of the proposed amplifiers is comparable to Ref. [59], and $IFOM_S$ is better than Ref. [52]. Additionally, FOM_L and $IFOM_L$ are comparable to Refs. [51, 59] and [51, 52], respectively.

Table 6.5 Performance comparison of proposed amplifiers 10-11 with their counterparts

Parameters	**[51]**	**[52]**	**[58]**	**[59]**	**Proposed Amplifier-10**		**Proposed Amplifier-11**	
Technology (nm)	500	180	180	500	180	180	180	180
Supply voltage (V)	± 1	± 0.5	± 0.7	3	± 1.5	± 1.5	± 1.5	± 1.5
C_L (pF)	20	20	20	30	20	30	20	30
GBW (MHz)	2	2.5	3	12	25	22	25	22
PM (°)	57	-	60	85	82	79	82	79
DC Gain (dB)	69	52	57.5	82	102	102	110	110
SR (V/μS)	0.5	2.89	2.8	10	10.42	10.1	10.8	10.56
Power (mW)	0.08	0.11	0.05	1.2	3.57	3.57	3.6	3.6
FOM_S	0.5*	0.45*	1.2*	0.3*	0.14	0.2	0.14	0.2
$IFOM_S$	1*	0.23*	1.65*	0.9*	0.42	0.6	0.4	0.6
FOM_L	0.13*	0.53*	1.12*	0.25*	0.13	0.1	0.1	0.1
$IFOM_L$	0.25*	0.26*	1.54*	0.75*	0.25	0.25	0.18	0.26

*FOM is calculated with the help of data given in the paper.

6.5 Summary

In this chapter, two frequency compensated three stage amplifiers are discussed, which employ class AB FVF in the inner compensation loop of RNMC to resolve the RHP zero issue. Additionally, a slew rate enhancer circuit is utilized between the output of the first stage and the third stage in the proposed amplifier 10, while it is connected between the second stage and the third stage in the proposed amplifier 11. A feed forward path along with the slew rate enhancer

circuit improves the transient response of the amplifiers. Further, the small signal analysis is performed to find out the transfer function, which gives the poles and zeros of the amplifiers. It helps in determining the stability of the amplifiers. The proposed amplifiers offer the highest GBW and DC gain of 25 MHz and 110 dB, respectively. The phase margin is 82° and 79° for the proposed amplifiers at 20 pF and 30 pF load, respectively. Moreover, the presented amplifiers in this chapter provide the highest slew rate of 10.8 V/µs. Additionally, a number of simulations, such as corner analysis, supply voltage variation, and Monte Carlo analysis are carried out to confirm the effectiveness of the proposed amplifiers.

Chapter 7

Conclusion and Future Scope

In this thesis, the performance of a three stage amplifier is enhanced with the help of various frequency compensation techniques. Section 7.1 highlights the important features and key findings of this thesis. The scope for future work is discussed in Section 7.2.

7.1 Summary of work done

One of the conventional techniques, such as RNMC, is employed with other methods to improve the frequency response and the transient response of the amplifier. Moreover, an active LHP zero circuit has been utilized with other techniques to enhance the performance of a three stage amplifier.

The first chapter of this thesis provides an overview of the multistage amplifiers and frequency compensation techniques. Further, different frequency compensation techniques available in the literature are reviewed in this chapter. Additionally, the research gaps are identified and research objectives are formulated.

Chapter 2 describes the different techniques to enhance the performance of a three stage amplifier such as RNMC, FVF, class AB FVF, folded FVF, push pull output stage, slew rate enhancer circuit, self cascode structure, DTMOS, self cascode with DTMOS, modified self cascode and active LHP zero circuit. The comprehension of these techniques provides sound justification for their use in the various circuits of this thesis.

A frequency compensated proposed amplifier 1 is presented in chapter 3. It utilizes RNMC with FVF to improve the GBW and phase margin of the amplifier. Additionally, the feed forward path enhances the transient response. The small signal analysis of the amplifier is done to find out the transfer function. It helps in evaluating the DC gain, stability, and GBW of the amplifier. The proposed amplifier 1 provides the GBW and phase margin of 20 MHz and 64°, respectively. Further, the DC gain is more than 100 dB and the slew rate is 10 V/µs.

Further, FFVF has been used in the inner loop of RNMC of the proposed amplifiers 2-5 to address the RHP zero issue in chapter 4. Moreover, a resistor is used in the outer loop of the proposed amplifiers 3-5 for double pole zero cancellation to further enhance the performance of the amplifiers. Additionally, the proposed amplifiers 4 and 5 make use of self cascode structure and DTMOS in the input stage to improve the GBW of the amplifiers. All the proposed amplifiers in chapter 4 employ the feed forward path to improve the

transient response. The small signal analysis of the amplifiers is done to find out the GBW and stability of the amplifiers. The proposed amplifier 5 offers the highest GBW and DC gain of 33.3 MHz and 104 dB, respectively. Moreover, the proposed amplifiers 2 and 3 provide the optimum phase margin of 60°. Further, the highest slew rate of 10 V/µs is achieved by the proposed amplifiers 2 and 3.

Chapter 5 presents the proposed amplifiers 6-9, which utilize an active LHP zero circuit to cancel the parasitic pole of the second stage. It enhances the GBW of the amplifiers. Further, a Miller capacitor with resistor ensures the stability of the amplifiers. Additionally, a self cascode structure and self cascode with DTMOS are incorporated in the input stage of the proposed amplifiers 6 and 7, respectively. It results in higher GBW of the amplifiers. The proposed amplifiers 8 and 9 employ a modified self cascode structure in the first stage to further improve the GBW. The amplifiers presented in this chapter make use of the feed forward path to make the transient response better. Further, the small signal analysis of the amplifiers is done to find out the transfer function, which helps in evaluating the GBW. The proposed amplifier 9 offers the highest GBW of 8 MHz. Further, the proposed amplifier 6 provides the phase margin of 62°, while the proposed amplifiers 7-9 give the phase margin of 60°. It shows the good stability of the amplifiers presented in this chapter.

The performance of a three stage amplifier is further improved with the help of Class AB FVF with RNMC in the proposed amplifiers 10 and 11 in chapter 6. The class AB FVF is employed in the inner loop of RNMC to resolve the RHP zero issue and improve the frequency response. Additionally, the feed forward path and slew rate enhancer circuit are employed to improve the transient response of the proposed amplifiers. The small signal analysis is carried out to find out the GBW of the amplifiers. The proposed amplifiers give the highest GBW and DC gain of 25 MHz and 110 dB, respectively. The maximum phase margin is 82°, which shows the higher stability of the amplifiers. Moreover, the presented amplifiers in this chapter provide the highest slew rate of 10.8 V/µs.

Additionally, the robustness of all proposed amplifiers is verified with the help of various simulations, such as corner analysis, supply voltage variation, and Monte Carlo analysis. The functionality of the proposed amplifiers is verified using TSMC 0.18 µm CMOS technology parameters in Tanner tool.

7.2 Scope for future work

There are various ways in which this work can be expanded. The following are some possible options to further explore the work.

(i) The frequency compensation techniques applied in this thesis can be employed on four stage amplifiers to improve the performance of these amplifiers.

(ii) The proposed amplifiers can be utilized to implement various circuits such as oscillators, active filters, peak detectors, etc.

(iii) The amplifiers presented in this thesis can be further designed at lower technology nodes such as 45 nm and 90 nm.

(iv) Different technologies such as CNTFET and FinFET can be applied to the proposed amplifiers to enhance the performance of the amplifiers.

(v) To break the forward path of RNMC, various voltage followers are implemented in the proposed amplifiers of chapters 3, 4, and 6. It is possible to explore more advanced voltage followers in RNMC to further enhance the performance of the amplifiers.

(vi) An active LHP zero circuit is employed in the proposed amplifiers of chapter 5 to cancel the parasitic pole. The active LHP zero circuit can be further utilized along with RNMC to improve the frequency response of the amplifier.

(vii) The proposed amplifiers in chapter 6 make use of the slew rate enhancer circuit to improve the transient response. Various other slew rate enhancer circuits can be tried out to enhance the transient response of the amplifier.

References

1. A.S. Sedra and K.C. Smith, “Microelectronics Circuits: Theory and Applications”, Sixth edition, Oxford University Press, New York, 2015.
2. B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, New York, 2001.
3. P.E. Allen and D.R. Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, New York, 2011.
4. A.D. Grasso, G. Palumbo and S. Pennisi, “Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs”, IEEE Transactions on Circuits and Systems II, Express Briefs, vol. 55, pp. 1099-1103, 2008.
5. W. Aloisi, G. Palumbo and S. Pennisi, “Design methodology of Miller frequency compensation with current buffer/amplifier”, IET Circuits Devices Systems, vol. 2, pp. 227–233, 2008.
6. S.H. Pakala, M. Manda, P. Surkanti, A. Garimella and P. Furth, “Voltage Buffer Compensation using Flipped Voltage Follower in a Two-Stage CMOS Op-amp”, IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), 2015.
7. U. Bansal, M. Gupta and U. Singh, “Frequency compensation of two stage CMOS circuit using negative capacitance and flipped voltage follower”, Analog Integrated Circuits and Signal Processing, vol. 90, pp. 175-188, 2016.
8. P.K. Chan and Y.C. Chen, “Gain-Enhanced Feedforward Path Compensation Technique for Pole–Zero Cancellation at Heavy Capacitive Loads”, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, pp. 933-941, 2003.
9. M. Abdulaziz, M. Tormanen and H. Sjoland, “A Compensation Technique for Two-Stage Differential OTAs”, IEEE Transactions on Circuits and Systems II, Express Briefs, vol. 61, pp. 594-598, 2014.
10. A. Mesri, M.M. Pirbazari, K. Hadidi and A. Khoei, “High gain two-stage amplifier with positive capacitive feedback compensation”, IET Circuits Devices Systems, vol. 9, pp. 181–190, 2015.
11. A. Mesri, J. Javidan and M.M. Pirbazari, “Analysis and design of a two-stage amplifier with enhanced performance”, Microelectronics Journal, vol. 46, pp. 1304-1312, 2015.

12. M.T. Sani and A. Hamoui, “A 1-V Process-Insensitive Current-Scalable Two-Stage Op amp With Enhanced DC Gain and Settling Behavior in 65-nm Digital CMOS”, IEEE Journal of Solid-State Circuits, vol. 46, pp. 660-668, 2011.
13. J.L. Lopez, A.D. Sanchez, C.M. Montero, J.R. Angulo, J.M.R. Perez, L.A.S. Gaspariano, “High Gain Amplifier with Enhanced Cascoded Compensation”, Radio Engineering, vol. 23, pp. 504-511, 2014.
14. M. Yavari and O. Shoaei, “Very Low-Voltage, Low-Power and Fast-Settling OTA for Switched-Capacitor Applications”, IEEE 14th International Conference on Microelectronics, 2003.
15. S. Pourashraf, J.R. Angulo, A.J.L. Martin and R.G. Carvajal, “A Highly Efficient Composite Class-AB–AB Miller Op-Amp With High Gain and Stable From 15 pF Up To Very Large Capacitive Loads”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, pp. 2061-2072, 2018.
16. J.M.A. Miguel, J.R. Angulo, E. Mirazo, A.J.L. Martin and R.G. Carvajal, “A Simple Miller Compensation With Essential Bandwidth Improvement”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, pp. 3186-3192, 2017.
17. M. Figueiredo, R. Tavares, E. Santin, J. Ferreira, G. Evans and J. Goes, “A Two-Stage Fully Differential Inverter-Based Self-Biased CMOS Amplifier With High Efficiency”, IEEE Transactions on Circuits and Systems I:Regular Papers, vol. 58, pp. 1591-1603, 2011.
18. Z. Yan, W. Wang, P.I. Mak, M.K. Law and R.P. Martins, “A 0.0045-mm^2 32.4-μW Two-Stage Amplifier for pF-to-nF Load Using CM Frequency Compensation”, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, pp. 246-250, 2015.
19. K.N. Leung and P.K.T. Mok, “Nested Miller compensation in low-power CMOS design”, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, pp. 388–394, 2001.
20. K.N. Leung, P.K.T. Mok and W.H. Ki, “Right-Half-Plane Zero Removal Technique for Low-Voltage Low-Power Nested Miller Compensation CMOS Amplifier”, IEEE International Conference on Electronics, Circuits and Systems, pp. 599-602, 1999.

21. R.G.H. Eschauzier, L.P.T. Kerklaan and J.H. Huijsing, “A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure”, IEEE Journal of Solid State Circuits, vol. 27, pp. 1709-1717, 1992.
22. F. You, S.H.K. Embabi and E.S. Sinencio, “Multistage Amplifier Topologies with Nested Gm-C Compensation”, IEEE Journal of Solid-State Circuits, vol. 32, pp. 2000-2011, 1997.
23. K.N. Leung and P.K.T. Mok, “Analysis of Multistage Amplifier–Frequency Compensation”, IEEE Transactions on Circuits & Systems I”, vol. 48, pp. 1041-1056, 2001.
24. X. Peng and W. Sansen, “Nested feed-forward Gm-stage and nulling Resistor plus Nested-Miller Compensation for Multistage Amplifiers”, IEEE Custom Integrated Circuits Conference, 2002.
25. R. Mita, G. Palumbo and S. Pennisi, “Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers”, IEEE Transactions on Circuits and Systems II, Analog and Digital Signal Processing, vol. 50, pp. 227-233, 2003.
26. A.D. Grasso, D. Marano, G. Palumbo and S. Pennisi, “Improved Reversed Nested Miller Frequency Compensation Technique with Voltage Buffer and Resistor”, IEEE Transactions on Circuits and Systems II, Express Briefs, vol. 54, pp. 382-386, 2007.
27. A.D. Grasso, G. Palumbo and S. Pennisi, “Advances in reversed nested Miller compensation”, IEEE Transactions on Circuits & Systems I, vol. 54, pp. 1459-1470, 2007.
28. S. Biabanifard, S. Mehdi Largani, M. Akbari, S. Asadi and C.E. Yagoub Mustapha, “High performance reversed nested Miller frequency compensation”, Analog Integrated Circuits and Signal Processing, vol. 85, pp. 223–233, 2015.
29. M. Zaherfekr and A. Biabanifard, “Improved reversed nested miller frequency compensation technique based on current comparator for three-stage amplifiers”, Analog Integrated Circuits and Signal Processing, vol. 98, pp. 633-642, 2019.
30. S. Shahsavari, S. Biabanifard, S. Mehdi Hosseini Largani and O. Hashemipour, “DCCII based frequency compensation method for three stage amplifiers”, International Journal of Electronics and Communications, vol. 69, pp. 176–181, 2015.

31. S. Mehdi Hosseini Largani, S. Shahsavari, S. Biabanifard and A. Jalali, “A new frequency compensation technique for three stages OTA by differential feedback path”, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 28, pp. 381–388, 2015.
32. A.D. Grasso, D. Marano, G. Palumbo and S. Pennisi, “Analytical comparison of Reversed Nested Miller Compensation Techniques”, International Journal of Circuit Theory and Applications, vol. 38, pp. 709-737, 2010.
33. Q. Li, J. Yi, B. Zhang and Z. Li, “A dual complex pole-zero cancellation frequency compensation with gain-enhanced stage for three-stage amplifier”, Analog Integrated Circuits and Signal Processing, vol. 48, pp. 175–180, 2006.
34. Z. Yan, P.I. Mak, M.K. Law and R.P. Martins, “A 0.016-mm 144-µW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW”, IEEE Journal of Solid State Circuits, vol. 48, pp. 527-540, 2013.
35. Z. Yan, P.I Mak, M.K Law, R.P Martins, “0.0045 mm^2 15.8 µW three-stage amplifier driving 10×-wide (0.15–1.5 nF) capacitive loads with >50° phase margin”, Electronics Letters, vol. 51, pp. 454-456, 2015.
36. A. Rasekh and M.S. Bakhtiar, “Compensation Method for Multi Stage Opamps with High Capacitive Load Using Negative Capacitance”, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, pp. 919-923, 2016.
37. W. Qu, J.P. Im, H.S. Kim and G.H. Cho, “A 0.9 V 6.3 µW Multistage Amplifier Driving 500 pF Capacitive Load with 1.34 MHz GBW”, IEEE International Solid-State Circuits Conference, pp. 290-292, 2014.
38. S. Guo and H. Lee, “Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers”, IEEE Journal of Solid-State Circuits, vol. 46, pp. 452-464, 2011.
39. S.S. Chong and P.K. Chan, “Cross Feedforward Cascode Compensation for Low-Power Three-Stage Amplifier with Large Capacitive Load”, IEEE Journal of Solid-State Circuits, vol. 47, pp. 2227-2234, 2012.
40. D. Marano, A.D. Grasso, G. Palumbo and S. Pennisi, “Optimized Active Single-Miller Capacitor Compensation with Inner Half-Feedforward Stage for Very High-Load

Three-Stage OTAs", IEEE Transactions on Circuits & Systems I, vol. 63, pp. 1349-1359, 2016.

41. A.K.N. Lenug, P.K.T. Mok, W.H. Ki and J.K.O. Sin, "Damping-Factor-Control Frequency Compensation Technique for Low-Voltage Low-Power Large Capacitive Load Applications", IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC, pp. 158–159, 1999.
42. H. Lee and P.K.T. Mok, "Active-Feedback Frequency-Compensation Technique for Low- Power Multistage Amplifiers", IEEE Journal of Solid-State Circuits, vol. 38, pp. 511–520, 2003.
43. X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers", IEEE Journal of Solid-State Circuits, vol. 39, pp. 2074–2077, 2004.
44. H. Aminzadeh, A. Ballo and A.D. Grasso, "Frequency Compensation of Three-Stage OTAs to Achieve Very Wide Capacitive Load Range", IEEE Access, vol. 10, pp. 70675-70687, 2022.
45. Q. Cheng, W. Li, X. Tang and J. Guo, "Design and Analysis of Three-Stage Amplifier for Driving pF-to-nF Capacitive Load Based on Local Q-Factor Control and Cascode Miller Compensation Techniques", Electronics Journal, vol. 8, pp. 1-18, 2019.
46. S. Dong, C. Liu, X. Xin and X. Tong, "A three-stage OTA with hybrid active miller enhanced compensation technique for large to heavy load applications", Microelectronics Journal, vol. 115, pp. 1-10, 2021.
47. A.D. Grasso, D. Marano, G. Palumbo and S. Pennisi, "Single miller capacitor frequency compensation techniques: Theoretical comparison and critical review, International Journal of Circuit Theory and Applications, vol. 50, pp. 1462-1486, 2022.
48. M.A. Mohammed and G.W. Roberts, "Scalable Multi-Stage CMOS OTAs With a Wide C_L-Drivability Range Using Low-Frequency Zeros", IEEE Transactions on Circuits and Systems I, vol. 70, pp. 74-87, 2023.
49. P. Manikandan, "Miller compensated three-stage OTA for a wide range of load capacitors (1pF to 1nF)", International Journal of Electronics, 2023.

50. Y. Jin, Y. Seo, S. Kim and S. Cho, “Three-Stage Operational Amplifier with Frequency Compensation Using Cascade Zero”, Circuit and Signal Processing, vol. 12, pp. 1-17, 2023.
51. T. Lehmann and M. Cassia, “1-V Power Supply CMOS Cascode Amplifier”, IEEE Journal of Solid-State Circuits, vol. 36, pp. 1082-1086, 2001.
52. S. Chatterjee, Y. Tsividis and P. Kinget, “0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design”, IEEE Journal of Solid-State Circuits, vol. 40, pp. 2373-2387, 2005.
53. S. Liu, Z. Zhu, J. Wang, L. Liu and Y. Yang, “A 1.2-V 2.41-GHz Three-Stage CMOS OTA With Efficient Frequency Compensation Technique”, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, pp. 20-30, 2018.
54. M. Tan and W.H. Ki, “A Cascode Miller-Compensated Three-Stage Amplifier With Local Impedance Attenuation for Optimized Complex-Pole Control”, IEEE Journal of Solid-State Circuits, vol. 50, pp. 440-449, 2015.
55. U. Dasgupta, G.T. Ong, J.M. Cao and S.L. Chew, “A Versatile Three-stage Operational Amplifier with Second-stage Bypass Compensation”, IEEE International Symposium on Integrated Circuits (ISIC), pp. 232-235, 2014.
56. F.A. Arand and M. Yavari, “A three-stage NMC operational amplifier with enhanced slew rate for switched-capacitor circuits”, Analog Integrated Circuits Signal Processing, vol. 106, 697–706, 2021.
57. A.R. Loera, A. Veerabathini, L.A.F. Oropeza, L.A.C. Martinez and D.M. Frias, “Improved Frequency Compensation Technique for Three-Stage Amplifiers”, Journal of Low Power Electronics and Applications, vol. 11, pp. 1-12, 2021.
58. E.C. Bernal, S. Pennisi, A.D. Grasso, A. Torralba and R.G. Carvajal, “0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier”, IEEE Transactions on Circuits and Systems I, vol. 63, pp. 1807-1815, 2016.
59. V. Saxena and R.J. Baker, “Indirect Compensation Techniques for Three-Stage Fully-Differential Op-amps”, IEEE 53rd International Midwest Symposium on Circuits and Systems (MWSCAS), 2010.

60. D. Marano, G. Palumbo and S. Pennisi, “Step-response optimisation techniques for low-power, high-load, three-stage operational amplifiers driving large capacitive loads”, IET Circuits, Devices & Systems, vol. 4, pp. 87-98, 2010.
61. X. Peng and W. Sansen, “Transconductance With Capacitances Feedback Compensation for Multistage Amplifiers”, IEEE Journal of Solid-State Circuits, vol. 40, pp. 1514-1520, 2005.
62. G.D. Cataldo, A.D. Grasso, G. Palumbo and S. Pennisi, “Improved single-miller passive compensation network for three stage CMOS OTAs”, Analog Integrated Circuits and Signal Processing, vol. 86, pp. 417-427, 2016.
63. A.D. Grasso, D. Marano, G. Palumbo and S. Pennisi, “High-Performance Three-Stage Single Miller CMOS OTA with no Upper Limit of C_L”, IEEE Transactions on Circuits & Systems vol. 65, pp. 1529-1533, 2017.
64. I. Chaharmahal, S. Asadi, B. Dorostkar, M.M. Bosra and M. Abedini “A New Method Modifying Single Miller Feedforward Frequency Compensation to Drive Large Capacitive Loads: Putting an Attenuator in the Path”, Analog Integrated Circuits and Signal Processing, vol. 93, pp. 61-70, 2017.
65. E. Ranjbar and M. Danaie, “Frequency compensation of three-stage operational amplifiers: Sensitivity and robustness analysis”, Microelectronics Journal, vol. 66, pp. 155-166, 2017.
66. U. Bansal, P. Gupta and R. Tayal, “A high gain and high bandwidth three stage amplifier using FGMOS and 0.5 V dual supply”, Analog Integrated Circuits and Signal Processing, vol. 103, pp. 247–258, 2020.
67. S.H. Pakala, M. Manda, P.R. Surkanti, A. Garimella and P.M. Furth, “Voltage Buffer Compensation using Flipped Voltage Follower in a Two-Stage CMOS Op-amp”, IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), 2015.
68. I.P. Cantoya, J.E.M. Solis and J.R. Angulo, “Class AB flipped voltage follower with very low output resistance and no additional power”, IEICE Electronics Express, vol. 15, pp. 1-7, 2018.
69. D. Marano, G. Palumbo and S. Pennisi, “Step-response optimisation techniques for low-power, high-load, three-stage operational amplifiers driving large capacitive loads”, IET Circuits, Devices & Systems, vol. 4, pp. 87-98, 2010.

70. F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P.K. KO and C. Hu, “A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation”, IEEE Proceedings of International Electron Devices Meeting, pp. 809-812, 1994.
71. M.T. Sanz, S. Celma, B. Calvo and D. Flandre, “Self-cascode SOI versus graded-channel SOI MOS transistors”, IEEE proceedings-Circuits Devices and Systems, vol. 153, pp. 461-465, 2006.
72. V. Niranjan, A. Kumar and S.B. Jain, “Composite Transistor Cell Using Dynamic Body Bias For High Gain and Low-Voltage Applications”, Journal of Circuits, Systems, and Computers, vol. 23, pp. 1-18, 2014.

Publications

List of Journal Papers (Published):

1. Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, "Improved reversed nested Miller frequency compensation techniques using flipped and folded flipped voltage follower with resistor for three stage amplifier", AEU-International Journal of Electronics and Communications, vol. 142, pp. 1-14, 2021. **(SCI-Expanded)**

2. Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, "Improved frequency compensation technique of three stage amplifier using class AB flipped voltage follower and slew rate enhancer circuit", AEU-International Journal of Electronics and Communications, vol. 177, pp. 1-15, 2024. **(SCI-Expanded)**

List of International Conference Papers:

1. Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, "Refining RNMC compensation for Three Stage Amplifier using DTMOS Transistor and FFVF", 14th International Conference on Computing, Communication and Networking Technologies (ICCCNT), July 2023.

2. Om Krishna Gupta, Neeta Pandey and Maneesha Gupta, "Enhancing Reversed Nested Miller Compensation of Three Stage Amplifier using Self Cascode and Folded Flipped Voltage Follower", Fifth International Conference on Advances in Electronics, Computers and Communications (ICAECC), Sep 2023.

Appendix A

Impact of temperature variation on the performance of the proposed amplifiers

Tables A1-A5 show the variations of Gain, GBW, and phase margin for a temperature variation of 75°C. It is found that the maximum variation in gain, GBW and PM for the proposed amplifiers 1-5 is 25%.

Table A1: Summary of variations in Performance parameter with temperature for proposed amplifier 1

Performance Parameter	Temperature		
	27° C	70° C	-5° C
Gain (dB)	101	98.3	100.5
GBW (MHz)	20	18.6	23.4
PM (°)	64	55	63

Table A2: Summary of variations in Performance parameter with temperature for proposed amplifier 2

Proposed amplifier	Performance Parameter	Temperature		
		27° C	70° C	-5° C
2	Gain (dB)	101	78.6	99.8
	GBW (MHz)	26	19.1	29.3
	PM (°)	60	58	62

Table A3: Summary of variations in Performance parameter with temperature for proposed amplifier 3

Performance Parameter	Temperature		
	27° C	70° C	-5° C
Gain (dB)	101	78.6	99.6
GBW (MHz)	30	24.4	36.7
PM (°)	60	51	62

Table A4: Summary of variations in Performance parameter with temperature for proposed amplifier 4

Performance Parameter	Temperature		
	27° C	70° C	-5° C
Gain (dB)	103	80.9	103.3
GBW (MHz)	31.3	23.5	35.5
PM (°)	50	45	53

Table A5: Summary of variations in Performance parameter with temperature for proposed amplifier 5

Performance Parameter	Temperature		
	27° C	70° C	-5° C
Gain (dB)	104	105	103.3
GBW (MHz)	33.3	25.1	39.2
PM (°)	54	48	55

Further, the effect of temperature on the performance of the proposed amplifiers 6-9 has been investigated at 27°C, 45°C, and -5°C. It is found that the variations are within an acceptable range for 27°C and 45°C, while they are higher for -5°C.

Tables A6-A7 show the variations of Gain, GBW, and phase margin for a temperature variation of 95°C. It is found that the variations in gain, GBW and PM for the proposed amplifiers 10-11 are within acceptable range.

Table A6: Summary of variations in Performance parameter with temperature for proposed amplifier 10

C_L	Performance Parameter	Temperature		
		27° C	70° C	-25° C
20 pF	Gain (dB)	102	103	93.4
	GBW (MHz)	25	19	28.8
	PM (°)	82	80.4	81.6
30 pF	Gain (dB)	102	103	93.4
	GBW (MHz)	22	18	27.1
	PM (°)	79	77	80

Table A7: Summary of variations in Performance parameter with temperature for proposed amplifier 11

C_L	Performance Parameter	Temperature		
		27° C	70° C	-25° C
20 pF	Gain (dB)	110	103	88.6
	GBW (MHz)	25	18.8	30.7
	PM (°)	82	81.5	79
30 pF	Gain (dB)	110	103	88.6
	GBW (MHz)	22	18.4	27.1
	PM (°)	79	77	80.1