Studies on Technology Computer Aided Design of Double Metal Negative Capacitance FET using DFT and Machine Learning Approach for Analog/Sensing Applications

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Under the Supervision of

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Dedicated

to

My Loving Family

DECLARATION

I declare that the research work presented in this thesis titled "**Studies on Technology Computer Aided Design of Double Metal Negative Capacitance FET using DFT and Machine Learning Approach for Analog/Sensing Applications**" for the attainment of the degree of ***Doctor of Philosophy in Physics*** has been conducted by me, under the guidance of ***Prof. Rishu Chaujar*** from the Department of Applied Physics, and co-guidance of ***Prof. Bansi Dhar Malhotra*** from the Department of Biotechnology, Delhi Technological University, Delhi, India. This work has not been previously submitted, either partially or in its entirety, to any other academic institution for any degree or diploma.

I declare that this thesis reflects my ideas expressed in my own words. Wherever the ideas or words of others have been incorporated, appropriate citation and referencing have been provided to acknowledge the sources. I also confirm that I have upheld the principles of academic honesty and integrity and that I have not misrepresented, fabricated, or falsified any information, data, fact, or source in the content of my submission.

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CERTIFICATE

This is to certify that the thesis titled **Studies on Technology Computer Aided Design of Double Metal Negative Capacitance FET using DFT and Machine Learning Approach for Analog/Sensing Applications** , submitted by **Mr. Yash Pathak**, to the Delhi Technological University, Delhi, for the award of the degree of **Doctor of Philosophy**, is a bonafide record of the research work done by him under our supervision and guidance. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Studies on Computer Aided Design Technology of Double Metal Negative Capacitance FET using DFT and Machine Learning Approach for Analog/Sensing Applications.

The exponential growth in transistor density has been the driving force behind advancements in computing power, energy efficiency, and cost reduction for decades. As transistor dimensions shrink, the gate loses control over the channel, causing issues such as threshold voltage roll-off, increased leakage currents, drain-induced barrier lowering (DIBL) etc, higher transistor densities increase power consumption per unit area. Shrinking device dimensions exacerbate parasitic capacitance, parasitic resistance, heat dissipation etc. The primary issue with conventional integrated circuits and systems based on CMOS technology is increasing power consumption. Due to the ability to reduce supply voltages using steep-subthreshold swing Field Effect Transistor devices, they have been proposed as a viable option for future circuits and systems that prioritize energy efficiency. The scientific and academic communities have shown significant interest in Negative Capacitance Field Effect Transistors (NCFETs). NCFETs offer numerous notable benefits compared to conventional FETs, primarily due to unique characteristics of the ferroelectric material used in their gate stack. The advantages of NCFETs include low power consumption, increased drive current, reduced subthreshold swing, and higher energy efficiency.

The property of NCFETs that allows them to achieve low off-current (I_{off}) and comparable on-current (I_{on}) at low supply voltages means that they work effectively at low switching voltage and with less power consumption. Different types of NCFETs depending on their structural integration with ferroelectric materials and engineering such as Planar NCFET, NC FinFET, Nanowire NCFET, NC Tunnel FET, etc have been analysed in various literature, each configuration has

distinct benefits but also poses various obstacles in their functioning like ferroelectric material stability, control of ferroelectric properties, power-performance trade-offs, temperature sensitivity, and overall device reliability. To counter these challenges, a new device structure, DM NCFET (Double Metal NCFET) is proposed and examined in this thesis. It comprises two metallic layers below the ferroelectric material with stacked insulator in between, resulting in MFMIMIS (Gate Metal-Ferroelectric-Metal-Insulator-Metal-Insulator-Semiconductor) configuration. The idea behind the inclusion of metal layers in the structure is due to its several benefits. The metal layer helps in redistributing the electric field across the ferroelectric and insulator layers. The metal layer also acts as a barrier, preventing direct tunnelling currents between the semiconductor and ferroelectric layers, thus enhances device reliability by minimizing leakage. The metal layer also provides better control over the interface properties, which reduces hysteresis effects in the ferroelectric layer. The metal layer can act as a heat sink, dissipating heat generated during device operation, thus improves the thermal stability and longevity of the device. Further, by isolating the ferroelectric and insulator layers, the metal layer minimizes defects at their interface, thus enhances the overall performance and reliability of the device. Subsequently, spacer technology is also incorporated in the DM NCFET configuration to form DM-NCFET (spacer) to further improve device performance and scalability. Spacers are typically insulating materials, such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2), formed on the sidewalls of the gate stack. They reduce hot-carrier injection (HCI), thereby improves device reliability and reduces electric field peaks at the drain junction. Spacers electrically isolate the gate electrode from the source/drain regions, thus prevent parasitic capacitance and any associated leakage paths. Spacers also help in achieving self-aligned source and drain regions during fabrication. So, by providing precise control over doping, isolation, and stress, spacers in general enhance the reliability and efficiency of the device. Thus, this proposed structure presents a promising direction for overcoming the limitations of conventional NCFETs, especially as technology nodes scale down. It provides a pathway to achieve a more promising device for meeting the demands of modern electronics.

Initially, the analog and RF (Radio Frequency) performance of the ferroelectric Field Effect Transistor device, specifically the DM-NCFET with and without a spacer were studied. The proposed DM-NCFET (spacer) improves the ON-current (I_{on}) by 25% as compared to the DM-NCFET without a spacer, reduces leakage current (I_{off}) by approximately 37%, enhances the switching ra-

tio (I_{on}/I_{off}) by 99%, increases the threshold voltage (V_{th}) by 0.29%, and lowers drain-induced barrier lowering (DIBL) by 17.6%. We also examined various analog parameters to improve the performance of the DM-NCFET with a spacer at 300K, including transconductance generation factor (TGF), transconductance (g_m), intrinsic gain (A_v), early voltage (V_{ea}), intrinsic delay (T_i), and some RF parameters like gain transconductance frequency product (GTFP), cut-off frequency (F_t), and gain frequency product (GFP). At 300K, the DM-NCFET(spacer) shows improved performance for these parameters compared to higher temperatures (400K and 500K). Simulated results using Visual TCAD confirm the high compatibility and enhanced performance of DM-NCFET(spacer) at room temperature (300K). Additionally, the gate electrode work function was varied using materials like Palladium, Chromium, and Tungsten. Palladium with a work function of 5.3eV, showed the best performance with improvement in leakage current by 106 times and switching ratio by 107 times compared to Chromium.

Furthermore, the DM-NCFET is explored for biosensing applications, analyzing the effects of nano cavity gaps with biomolecules like proteins, cholesterol oxidase (ChO_x), streptavidin, and uricase. Electrical characteristics such as threshold voltage and switching ratio (I_{on}/I_{off}) are higher with biomolecules compared to without biomolecules. Protein sensitivity is improved by 1.11 times, and the detection limit is higher by 1.012 times. The biosensor's sensitivity is increased with increase in dielectric parameter of the biomolecules, and modulation of the cavity gap length (from 8nm to 12nm). Visual TCAD software was used for all the simulations, showing that the DM-NCFET biosensors are highly sensitive with low-power consumption, thus suitable in numerous applications like checking infections, food investigation, crime detection, ecological monitoring, and biomedical field.

Moreover, the analog/RF and linearity parameters of Single Metal Double Gate NCFET (SM-DGNCFET) and Double Metal Double Gate NCFET (DM-DGNCFET) are observed using Cogenda Visual TCAD and Quantum ATK tool. SM-DGNCFET demonstrated better performance with a 279 times higher switching ratio, 54% lower DIBL, reduced SS, and improved transconductance, TGF, and RF parameters like TFP, confirming the enhanced device's reliability and stability. Linearity parameters such as second and third-order transconductance (g_{m2}, g_{m3}) and voltage intercept points for 2nd and 3rd order are also improved. The Tran-Blaha modified Becke-Johnson (TB-mBJ) approximation provided accurate band gap calculations, and DFT-based atomic studies

with 12.5% Si doping in HfO_2 crystals showed better conductivity for the device.

Further, the machine learning approach for predicting key analog and RF parameters of NCFETs is also explored using Visual TCAD and Python. The algorithm of an artificial neural network effectively predicted multi-input to single-output relationships, reducing computational costs. Simulations demonstrated that DM-DGNCFETs performed optimally at T=300K, T_{ox}=0.8nm, and T_{sub}=3nm, improving the switching ratio and reducing leakage current. Notably, at $T = 300K$, the switching ratio is higher and the leakage current is 84 times lower compared to $T = 500K$. Similarly, at ferroelectric thicknesses $T_{Fe} = 4nm$, the switching ratio improves by 5.4 times compared to $T_{Fe} = 8nm$. Furthermore, at substrate thicknesses $T_{sub} = 3nm$, switching ratio increases by 81% from $T_{sub} = 7nm$. For oxide thicknesses at $T_{ox} = 0.8nm$, the switching ratio increases by 41% compared to $T_{ox} = 0.4nm$. The analysis reveals that $T_{Fe} = 4nm$, $T = 300K$, $T_{ox} = 0.8nm$, and $T_{sub} = 3nm$ represent the optimal settings for DM DGNCFET, resulting in significantly improved performance.

Additionally, experimental circuit designs of Ion-Sensitive FETs (ISFETs) for pH sensing are investigated. The gate electrode work function on ISFETs was rigorously studied using Cogenda Visual TCAD, with molybdenum showing better results than aluminum. Based on its I-V characteristics, it may deduce that molybdenum, with a work function of 4.75eV, has a larger threshold voltage, switching ratio (10^4) and lower leakage current (10^{-3}) than aluminium at 300K. Comparative studies of ISFET sensing layers (Al_2O_3, Si_3N_4, SiO_2) indicated that Al_2O_3 displayed the best results for switching ratio, leakage current, sensitivity, and transconductance. The enhancement in pH sensing is also demonstrated experimentally with proper circuit designing of ISFET. ISFET display instability, often referred to as drift, in the form of a gradual, monotonic, temporal increase in the device's threshold voltage. The validation of the observations is done by increasing the value of the pH as follows: 4.67, 5.9, 7.5, 8.57, and 9.3, which were checked by pH meter.

In conclusion, DM-NCFET shows great potential for low-power, analog, RF, and sensing applications along with its compatibility with DFT and machine learning approaches as discussed comprehensively in this research work.

Contents

DECLARATION **i**

CERTIFICATE **iii**

ACKNOWLEDGEMENTS **v**

ABSTRACT **viii**

List of figures **xviii**

List of tables **xix**

List of publications **xx**

1 Introduction **1**

1.1 Background 2

1.2 Theory of NCFET 4

1.2.1 Basic Structure of NCFET 4

1.2.2 Ferroelectric Material 5

1.2.3 Operation of NCFET 7

1.2.4 NCFET Device Engineering 9

1.3 Advantages of NCFET 12

1.4 Challenges Confronted by NCFET 14

1.5 Proposed Device 16

1.6 Research Objectives 17

1.7 Thesis Organisation 18

2 Effect of Temperature and Work Function Variation on Double Metal NCFET with Spacer Engineering **22**

2.1 Introduction 23

2.2 Device Architecture 24
2.3 Method of Simulation 25
2.4 Result & Discussion 26
2.4.1 Device Scalability 26
2.4.2 Analog Analysis 27
2.4.3 RF (Radio Frequency) Analysis 30
2.4.4 Effect of Variation of Temperature on the performance of DM-NCFET . . 33
2.4.5 Effect of Variation of Work Function on the performance of DM-NCFET . 35
2.5 Summary 40

3 Detection of Biomolecules in Dielectric Modulated Double Metal NCFET with Improved Sensitivity 42

3.1 Introduction 43
3.2 Device Structure 44
3.3 Simulation Methodology 45
3.4 Result and Discussion 46
3.4.1 Impact of Various Biomolecules on DM-NCFET 46
3.4.2 Effect of Length Modulation in Cavity Gap 51
3.5 Summary 53

4 DFT Based Atomic Modeling and Optimization of Double Metal Double Gate NCFET 54

4.1 Introduction 55
4.2 Device Design and Atomic Study 56
4.2.1 Device Structure 56
4.2.2 Structure of Ferroelectric HfO_2-Based Crystal 58
4.3 Methodology and Theoretical Details 59
4.3.1 Device Methods 59
4.3.2 Method for HfO_2 Crystal 59
4.3.3 Flowchart for Fabrication Feasibility from Atomic Modeling to Device Fabrication 60
4.4 Result and Discussion 61
4.4.1 Comparative Study of NCFET Device 61
4.4.2 DFT Analysis of Ferroelectric HfO_2 based Crystal 67

4.5 Summary . . . 70

5 Artificial Neural Network based Modelling for Variational Effect on Double Metal Double Gate Negative Capacitance FET **71**

5.1 Introduction . . . 72

5.2 Device Architecture and Simulation Methodology . . . 73

5.3 Artificial Neural Network (ANN) Implementation . . . 74

5.4 Result and Discussion . . . 76

5.5 Summary . . . 82

6 Experimental Circuit Design and TCAD Analysis of Ion Sensitive Field Effect Transistor (ISFET) for pH Sensing **84**

6.1 Introduction . . . 85

6.2 Device Structure and Circuit Designing . . . 86

6.2.1 Device Structure of ISFET . . . 86

6.2.2 Experimental Circuit Designing of ISFET based pH Sensor . . . 88

6.3 Simulation Study of ISFET and Circuit based pH Sensor . . . 89

6.3.1 Simulation Study of ISFET Device . . . 89

6.3.2 Techniques for Experimental Circuit Designing . . . 89

6.3.3 Fabrication Feasibility of ISFET based pH Sensor . . . 90

6.4 Result and Discussion . . . 91

6.4.1 Comparative Study of ISFET for Different Gate Electrode Material . . . 91

6.4.2 Experimental Circuit Design Result of ISFET . . . 95

6.4.3 Effect of Variation of Sensing Layer on ISFET performance . . . 97

6.5 Summary . . . 100

7 Summary and Future Scope **101**

7.1 Summary . . . 101

7.2 Future Work . . . 104

References **116**

Reprints of Journal Publication **117**

List of Figures

1.1 The plot of (a) No. of Transistor per Microprocessor vs Year (hpm) (b) MOSFET Gate Length vs Year (Rad13). 2

1.2 (a) The advancement of semiconductor FET vs SS (RTU21) (b)The graph of drain current vs gate voltage for MOSFET and NCFET (LSH+23). 3

1.3 Schematic diagram for (a) NCFET with MFIS configuration (Pah20) (b) NCFET with MFMIS configuration (PDAC18) 5

1.4 The plot of polarisation vs electric field for (a) paraelectric and (b) ferroelectric (DDVK22). Atomic structure of $Pb^{2+}Ti^{4+}{O_3}^{6-}$ for (c) paraelectric (d) ferroelectric with up polarisation (e) ferroelectric with down polarisation (WYSK15). 6

1.5 (a) Schematic diagram for equivalent capacitance model of NCFET and (b) Device structure of NCFET (Pah20). 9

1.6 (a) The plot of polarisation vs electric field for NC (Kha15) (b) Drain current vs gate voltage graph for MFIS vs MFMIS (CB20) (c) Energy vs charge graph (MCM22) (d) Hystresis curve for NC. 10

1.7 The schematic diagram of device engineering for (a) Planar NCFET (TWW+18) (b) NC FinFET (TWW+18)(c) Fe-Ins-FET (LKSH16) (d) Nanowire NCFET (SHH20) (e) GAA NCFET (SHH20) (f) NC-TFET (TWW+18). 11

2.1 The two different DM-NCFET schematics structure (a) DM-NCFET with spacer (b) DM-NCFET (PMC22b). 25

2.2 (a) The curve of drain current vs gate voltage in linear and log scale (b) comparison of V_{th} (V) and switching ratio at V_d=0.3V for DM-NCFET(spacer) and DM-NCFET (PMC22b). 27

2.3 The curve of different structures at V_d=0.3V (a) transconductance and transconductance generation factor vs gate voltage (b) drain current and output conductance vs drain voltage (PMC22b). 28

2.4 Graph of different structures at V_d=0.3V showing (a) drain induced barrier lowering (b) Variation of early voltage and intrinsic gain vs gate voltage at T=300K (PMC22b). 29

2.5 Variation of (a) gate capacitance vs gate voltage and cutoff frequency vs gate voltage (b) intrinsic delay vs gate voltage for different structures with V_d=0.3V and L_g = 20nm at T=300K (PMC22b). 31

2.6 Electric field contour with (a) DM-NCFET (spacer) from 0 to 8.661E+06 and (b) DM-NCFET from 0 to 8.404E+06 at V_d=0.3V and T=300K.(PMC22b). 32

2.7 Graph for different structures at V_d=0.3 showing (a) Variation of gain frequency product and gain transconductance frequency gain product vs gate voltage at T=300K, (b) Variation of drain current in linear and log scale vs gate voltage for different temperature of DM-NCFET (spacer) at V_d=0.3 (PMC22b). 33

2.8 The graph showing variation of (a) threshold voltage and switching ratio vs gate voltage (b) transconductance and transconductance generation factor vs gate voltage for DM-NCFET (spacer) at different temperature, T=300K, 400K and 500K at V_d=0.3 (PMC22b). 34

2.9 The contour plot of electric field for (a) palladium (b) tungsten (c) chromium (d) Variation of electric field vs position along the channel for various gate electrode of DM-NCFET(spacer) at V_d=0.4V, V_{gs}=0.4V, and T=300k (PMC22b). 36

2.10 (a) The impact on electric field vs position along channel for palladium gate electrode at different gate voltage (b) Variation of drain current vs gate voltage of DM-NCFET(spacer) for various gate electrode at V_d=0.4V and T=300k (PMC22b). . 36

2.11 Variation of (a) potential vs position along channel (b) maximum electric field and maximum potential of DM-NCFET(spacer) with various gate electrode materials at V_d=0.4V and T=300K (PMC22b). 38

2.12 (a) The effect on quasi fermi potential vs position along channel and (b) The impact on energy band structure (conduction band (E_c) and valence band (E_v)) vs position along channel for DM-NCFET(spacer) with palladium, tungsten, and chromium as gate elctrode materials at V_d=0.4V and T=300K (PMC22b). 39

3.1 (a) The Schematic diagram of DM-NCFET for detection of biomolecule (b) Magnified view of cavity with biomolecules(PMC22c). 45

3.2 Transfer characteristic of different biomolecules for DM-NCFET at drain voltage =0.4V. (PMC22c). 46

3.3 Variation of (a) Transconductance, (g_m) (b) Threshold voltage (V_{th}) versus gate voltage of different biomolecules for DM-NCFET at $V_d = 0.4V$. (PMC22c). . . . 47

3.4 (a) Switching ratio (I_{on}/I_{off}) (b) Sensitivity of DM-NCFET for different biomolecules at drain voltage =0.4V. (PMC22c). 47

3.5 Contour plot for Electronic concentration of DM-NCFET for different biomolecules with dielectric constant (a) K=8 (b) K=3.5 (c) K=2.1 (d) K=1.5 (e) K=1 and (f) Variation of electronic concentration vs distance along channel for various biomolecules (PMC22c). 48

3.6 Contour plot for Potential of DM-NCFET for different biomolecules with dielectric constant (a) K=8 (b) K=3.5 (c) K=2.1 (d) K=1.5 (e) K=1. (f) Variation of potential vs distance along channel at drain voltage = 0.4V for different biomolecules (PMC22c). 49

3.7 Variation of (a) drain current vs drain voltage (b) output conductance vs drain voltage of DM-NCFET at gate voltage = 0.4V for different biomolecules (PMC22c). 50

3.8 Variation of (a) drain current vs gate voltage (b) Sensitivity of DM-NCFET for various biomolecules with different cavity length, L_{bio} = 8nm, 10nm, and 12nm at drain voltage = 0.4V (PMC22c). 51

3.9 Variation of (a) switching ratio of DM-NCFET (b) limit of detection (LOD) for various biomolecules with different cavity length, L_{bio} = 8nm, 10nm, and 12nm at drain voltage = 0.4V (PMC22c). 52

4.1 Structural diagram of (a) Double Metal Double Gate NCFET(DM DGNCFET) and (b) Single Metal Double Gate NCFET device (SM DGNCFET) (PMC23). . . . 57

4.2 Structural diagram of HfO_2 ferroelectric based simple cubic crystal (a) without doping (b) with Si doping (PMC23). 58

4.3 Fabrication process flowchart from atomic modelling to device modelling (PMC23). 60

4.4 Plot of (a) drain current and log drain current vs gate voltage (b) transconductance and TGF vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05V (PMC23). 61

4.5 Plot of (a) DIBL and subthreshold swing vs gate voltage (b) switching ratio and threshold voltage vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage= 0.05V (PMC23). 63

4.6 Plot of (a) drain current and output conductance vs drain voltage (b) gate capacitance and unity gain cutoff frequency vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage =0.05V (PMC23). 63

4.7 (a) The curve of maximum frequency vs gate voltage (b) GFP and TFP vs gate voltage at ferroelectric thickness =7nm, temperature =300K, drain voltage = 0.05V (PMC23). 65

4.8 (a) Plot of second and third order transconductance vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage =0.05V, (b) The calibration curve between drain current vs gate voltage curve at drain voltage =0.2V from reference (LFT+16) (PMC23). 66

4.9 The curve of drain current vs gate voltage for (a) variation of ferroelectric thickness (b) different substrate thickness (c) variation of temperature (PMC23). 67

4.10 Band structure for (a) Si doping (b) without doping (PMC23). 68

4.11 (a) Curve of Hartree potential vs length of atom, (b) Curve of electron density vs length of atom for without doping and Si doping (PMC23). 69

4.12 Curve of density of state vs energy for (a) Si doping and (b) without doping at centre of fermi energy (PMC23). 69

5.1 The 2D schematic diagram of Double Metal Double Gate NCFET (PMC23). . . 73

5.2 The figure shows the DM DGNCFET Artificial Neural Network (ANN) with one input, one output, and three hidden layers. There are 256 neurons in the first and third hidden layers, and 512 neurons in the middle layer V_{ds} (KLK+19a) 74

5.3 Algorithm for DM DGNCFET Artificial Neural Network (ANN) (KLK+19a). . . 75

5.4 The graph of drain current vs gate voltage for predicted and simulated data of DM DGNCFET for different variations of temperature, oxide thickness, ferroelectric thickness, and substrate thickness at V_{ds}=0.05V (KLK+19a; PMC23). 76

5.5 The graph of drain current vs gate voltage DM DGNCFET for different variations of temperature, oxide thickness, ferroelectric thickness, and substrate thickness at V_{ds}=0.05V (PMC23). 77

5.6 Artificial Neural Network Model for DGNCFET 79

5.7 The plot of transconductance and TGF vs V_{gs} for various temperature and thicknesses at V_{ds}=0.05V (PMC23). 81

5.8 The spider chart of leakage current, switching ratio, threshold voltage for different temperature and thicknesses at V_{ds}=0.05V (PMC23). 82

6.1 Sketch diagram for ISFET structure by TCAD tool (PMS+24). 87

6.2 (a) Circuit diagram of ISFET based pH sensor (b) Experimental setup (c) MP008v2 ISFET (PMS+24). 88

6.3 The flowchart of fabrication feasibility of ISFET based pH Sensor from ISFET to circuit designing (PMS+24). 91

6.4 (a) I_{ds} - V_g characteristics on the left side and log drain current on the right side (b) g_m - V_g characteristics on left side and TGF on the right side for different materials of electrode used in ISFET designing at V_{ds}=0.5V and T=300K (PMS+24). . . 92

6.5 (a) I_{ds} - V_{ds} characteristics in the left side and output conductance on the right side (b) The plot of switching ratio on the left side and leakage current on the right side for different materials of electrode used in ISFET designing T=300K (PMS+24). 93

6.6 (a) The plot of threshold voltage on the left side and subthreshold swing on the right side (b) V_e - V_g characteristics on the left side and intrinsic gain on the right side for different materials of electrode used in ISFET designing at V_{ds}=0.5V, T=300K (PMS+24). 94

6.7 The calibration of ISFET from (a) reference (KZH07) (b) reference (KZP+15). . 95

6.8 The graph of (a) pH value vs output voltage in pH capsule solution (b) Sensitivity vs pH value in pH capsule solution (c) pH value vs output voltage in PBS solution (d) Sensitivity vs pH value in PBS solution for pH based ISFET device (PMS+24). 96

6.9 The curve of (a) drain current vs gate voltage for different sensing layer (b) sensitivity and leakage current for various sensing layer (PMS+24). 97

6.10 The variation of (a) limit of detection and SS for varous sensing layer (b) transconductance and device efficiency vs gate voltage (PMS+24). 98

6.11 Contour plot of electric field for various sensing layer (a) Al_2O_3 (b) Si_3N_4 (c) SiO_2 (d) variation of electric field along the channel for various sensing layer (PMS+24). 98

List of Tables

2.1 Parameters used for the simulation of DM-NCFET (spacer) and DM-NCFET . . 24

2.2 Comparison of different performance parameters for different configurations at T_{ox}=1nm, T=300K and L_g=20nm . . . 31

2.3 Comparison of different performance parameters for DM-NCFET (spacer) at various temperature with T_{ox}=1nm, and L_g=20nm. . . . 34

2.4 Performance comparison of DM-NCFET (spacer) and DM-NCFET for different gate electrode materials such as palladium, chromium, and tungsten. . . . 37

3.1 Comparison of different performance parameters for various biomolecules in DM-NCFET at $T_{ox} = 1nm$ and cavity length of $10nm$ . . . 50

4.1 The Device parameters for SM DGNCFET and DM DGNCFET used for the simulation . . . 57

4.2 The parameters of leakage current, subthreshold swing, DIBL, and others for SM DGNCFET and DM DGNCFET . . . 62

4.3 Brillouin Zone (BZ) of the specific position of ferroelectric HfO_2 based crystal for band stucture . . . 68

5.1 The Device parameters for DM DGNCFET are used for the simulation . . . 74

5.2 DM DGNCFET comparison for different temperature, substrate thickness, ferroelectric, oxide thickness. . . . 80

6.1 ISFET device parameter by TCAD simulation. . . . 87

6.2 Performance comparison of ISFET for different gate electrode materials such as molybdenum, chromium, and aluminium . . . 92

6.3 Comparison of output voltage and sensitivity of this ISFET device with previously reported results . . . 95

List of publications

Publication Result from this thesis work

Article in International Refereed Journal (5):

1. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer", ***Silicon***. vol. 14, pp. 12269–12280, 2022 (**SCIE index, Impact Factor: 2.8**).
2. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Detection of biomolecules in dielectric modulated double metal below ferroelectric layer FET with improved sensitivity", ***Journal of Materials Science: Materials in Electronics***. vol. 33, no. 17, pp. 13558–13567, 2022 (**SCIE index, Impact Factor: 2.4**).
3. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "DFT based atomic modeling andAnalog/RF analysis of ferroelectric HfO2based improved FET device", ***Physica Scripta***. vol. 98, no. 8, pp. 1-15, 2023 (**SCIE index, Impact Factor: 2.8**).
4. **Yash Pathak**, Piyush Mishra, Megha Sharma, Shipra Solanki, Ved Varun Agarwal, Bansi Dhar Malhotra, and Rishu Chaujar "Experimental circuit design and TCAD analysis of ion sensitive field effect transistor (ISFET) for pH sensing", ***Materials Science and Engineering: B***. vol. 299, no. , pp. 116951, 2024 (**SCIE index, Impact Factor: 3.9**).
5. **Yash Pathak**, Kajal Verma, Bansi Dhar Malhotra, and Rishu Chaujar "Impact of Work function and Effect of Electric Field across the Channel on Gate Staked NCFET for Analog/Switching Performance", ***Physica Scripta***. 2024 (**SCIE index, Impact Factor: 2.8**).

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Advanced Nanoscale MOSFET architectures: Current Trends and Future Perspectives (pp. 113-123), Wiley, 2023.

2. **Yash Pathak**, Anshul, Bansi Dhar Malhotra, and Rishu Chaujar "Dielectric-modulated Gate Engineered NCFET as a label-free biosensor", ***LNEE Proceedings, Scopus indexed,*** Springer, 2024. (Accepted).

3. **Yash Pathak**, Rashi Mann, Bansi Dhar Malhotra, and Rishu Chaujar "Numerical Study on Impact of Sensing Film on modified ISFET for improved analog performance", ***LNEE Proceedings, Scopus indexed,*** Springer, 2024. (Accepted).

Article in International Conferences (4):

1. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Tcad analysis and simulation of double metal negative capacitance fet (dm ncfet)", ***2021 Devices for Integrated Circuit (DevIC)***. Kalyani, India, pp. 224–228, 2021.

2. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "A numerical study of analog parameter of negative capacitance field effect transistor with spacer", ***2021 7th International Conference on Signal Processing and Communication (ICSC)***. Noida, India, pp. 277–281, 2021.

3. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Linearity Performance of Double Metal Negative Capacitance Field-Effect Transistors: A Numerical Study", ***2022 IEEE VLSI Device Circuit and System (VLSI DCS)***. Kolkata, India, pp. 19–23, 2022.

4. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Impact of Temperature on Negative Capacitance FET: A TCAD Simulation Study", ***2023 2nd Edition of IEEE Delhi Section Flagship Conference (DELCON)***. Rajpura, India, pp. 1–4, 2023.

Communicated Journal Paper (2):

1. **Yash Pathak**, Laxman Prasad Goswami, Bansi Dhar Malhotra, and Rishu Chaujar "Artificial Neural Network based Modelling for Variational Effect on Double Metal Double Gate Negative Capacitance FET using Machine Learning Approach", ***IEEE Transactions on Electron device***. 2024.

2. **Yash Pathak**, Bansi Dhar Malhotra, and Rishu Chaujar "Synthesis of SnO2 based study using DFT and Experimental result", ***IEEE Transaction Nanotechnology, IEEE***. 2024.

Chapter 1

Introduction

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* This chapter provides a comprehensive overview of the research work, focusing primarily on the significance of NCFET in the low power memory device and the modern integrated circuit industry.
* Following that, this chapter includes a review of several engineering techniques for reducing short channel effects(SCEs), such as planar NCFET, junctionless engineering, NC FinFET, NC TFET, and Fe-Ins-FET as reported in various research articles.
* Moreover, NCFET is covered in the chapter as a possible solution to the issues. The chapter then goes on to discuss the basic design of NCFETs, their classification, their basic operation, potential advantages, and the technological difficulties incurred in NCFETs.
* The chapter concludes with a summary of all the chapters and an outline of the research objectives for the thesis.

1.1 Background

Jack Kilby independently developed the concept of the integrated circuits (ICs) while employed at Texas Instruments in 1958, which transformed the electronic world (Sax09). Moore's law served to reduce Complementary Metal-Oxide-Semiconductor (CMOS) technology, which in turn fueled the development of ICs. Moore's Law, named after Gordon Moore, an Intel co-founder, is credited with coining the Moore's Law, which states that a chip's transistor count doubles every two years (Moo98). Figure 1.1 reveals (a) the curve showing increase in number of transistors per microprocessor with the increasing time (hpm), and (b) trend of decreasing length of gate for mosfet with time along with exponential scaling trend of transistors according to International Technology Roadmap for Semiconductors (ITRS) target (Rad13). The performance of ICs has greatly enhanced as transistor's size has been reduced and more densely integrated on a chip, resulting in reduced cost and power consumption. This tendency has enabled the extensive use of diverse range of electronic devices, including personal computers, cellphones, and modern medical equipment, as well as autonomous vehicles (Kum24).

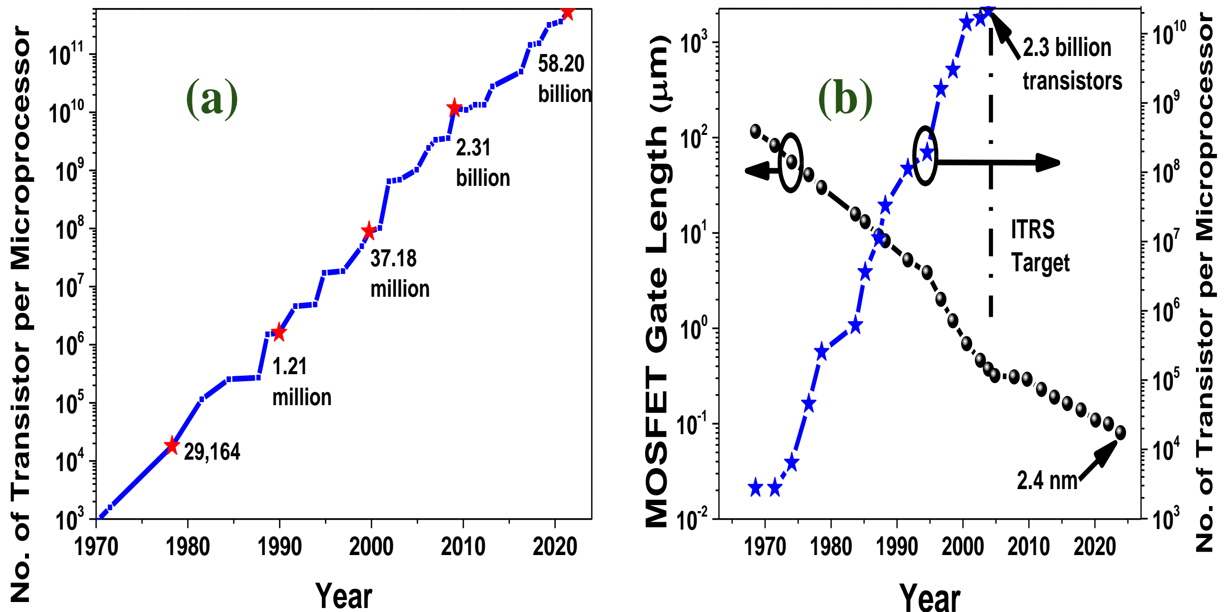

Figure 1.1: The plot of (a) No. of Transistor per Microprocessor vs Year (hpm) (b) MOSFET Gate Length vs Year (Rad13).

Nevertheless, achieving this reduction in size to the nanoscale is very challenging owing to constraints such as higher leakage current, elevated power consumption, SCEs, quantum phenomena, and heat dissipation problems, etc (Kuh11; RMMM03). The drain potential starts to impact the electrostatics of the channel in highly scaled MOSFETs, leading to an increased leakage current between the drain and the source. Furthermore, transistors are prone to significant SCEs, including threshold voltage (V_{th}) roll-off, which contribute to power dissipation, drain induced barrier lowering, and subthreshold slope (XLX+13; CK04). The primary issue with conventional integrated circuits and systems based on CMOS technology is increasing power consumption. Due to the ability to reduce supply voltages using steep-subthreshold swing Field Effect Transistor devices, they have been proposed as a viable option for future circuits and systems that prioritize energy efficiency (RTU21).

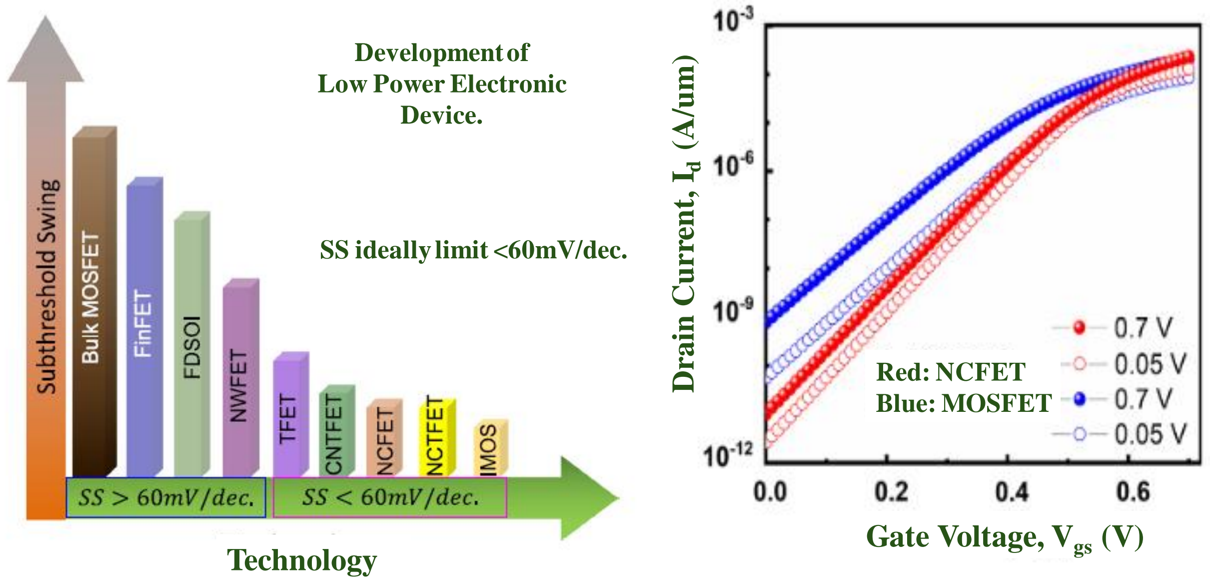

Figure 1.2: (a) The advancement of semiconductor FET vs SS (RTU21) (b)The graph of drain current vs gate voltage for MOSFET and NCFET (LSH+23).

The scientific and academic communities have shown significant interest in NCFETs. The notion of negative capacitance in a FET involves increasing the internal potential without changing the transport phenomenon of conventional MOSFETs. NCFETs have successfully achieved comparable switching at a lower supply voltage, V_{DD}, than conventional MOSFETs. The SS of NCFET is ideally less than 60mV/dec. as illustrated in Figure 1.2(a) (RTU21). The property of NCFETs that allows them to achieve low off-current (I_{off}) and comparable on-current (I_{on}) at low supply

voltages means that they work effectively at low switching voltage and with less power consumption as exhibited in Figure 1.2(b) (LSH+23). This can be accomplished by making minor adjustments to ordinary CMOS devices, i.e. by incorporating a small layer of ferroelectric material into the gate stack. This small change to a conventional MOSFET is aimed at NC, which is a distinctive feature of FE materials. Materials with non-linear dielectric behaviour are called FE materials. These materials exhibit a phenomenon called pre-existing polarization, which undergoes a reversal in direction when an external electric field is applied.

1.2 Theory of NCFET

1.2.1 Basic Structure of NCFET

The negative capacitance FET is a sophisticated variation of the FET that incorporates a ferroelectric material into the gate stack in order to attain a negative capacitance phenomenon. The presence of negative capacitance may address the drawbacks of traditional FETs by effectively decreasing the subthreshold swing to a level below the 60 mV/decade threshold. This, in turn, improves the performance and energy efficiency of the device.

Figure 1.3 reflects the schematic diagram for (a) NCFET with Metal Ferroelectric Insulator Semiconductor (MFIS) configuration (Pah20), and (b) NCFET with Metal Ferroelectric Metal Insulator Semiconductor (MFMIS) configuration (PDAC18). The NCFET is characterized by its specific structure:

1. Substrate refers to the underlying substance, often silicon or another semiconductor, that serves as the basis for a transistor.
2. The source and drain of the FET are heavily doped areas in the substrate that facilitate the injection and extraction of charge carriers, which may be either electrons or holes.
3. The channel is the area located between the source and drain, where the charge carriers flow. The gate voltage regulates the conductivity of the channel.
4. The gate oxide, also known as the dielectric layer, is a thin insulating layer that separates the gate from the channel. Typically, in an NCFET, this layer consists of a high-k dielectric material, which enhances gate control and minimizes leakage currents.

5. The ferroelectric layer is the crucial element that distinguishes NCFETs from regular FETs. The ferroelectric layer, typically composed of hafnium oxide (HfO_2) doped with dopants such as zirconium, silicon and aluminium, which has been proved to possess ferroelectricity, is positioned above the gate oxide. The ferroelectric material demonstrates a negative capacitance phenomenon, which augments the total gate capacitance and decreases the subthreshold swing.

6. The gate electrode refers to the uppermost layer of a device, often composed of metal or polycrystalline silicon. The gate electrode is used to administer a voltage that regulates the conductivity of the channel.

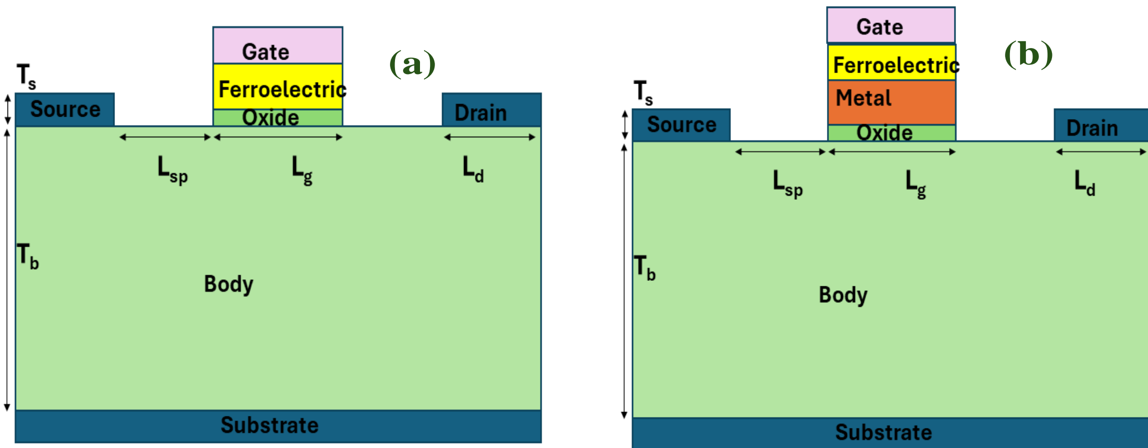

Figure 1.3: Schematic diagram for (a) NCFET with MFIS configuration (Pah20) (b) NCFET with MFMIS configuration (PDAC18)

1.2.2 Ferroelectric Material

While discussing the materials exhibiting nonlinear polarization under the influence of electric field, there are two categories: one is paraelectric materials, which give enhanced nonlinear polarization and no polarisation occurs even in absence of electric field as shown in Figure 1.4(a), while the other is ferroelectric materials, which give non zero spontaneous polarization that exhibit two possible states of polarization even in the absence of electric field as illustrated in Figure 1.4(b). The polarization is directly proportional to an electric field applied in the ferroelectric material. Even when the electric field is no longer present in the ferroelectric material, the remnant polarisation remains as depicted in the hysteresis loop owing to the material's inherent spontaneous polarization.

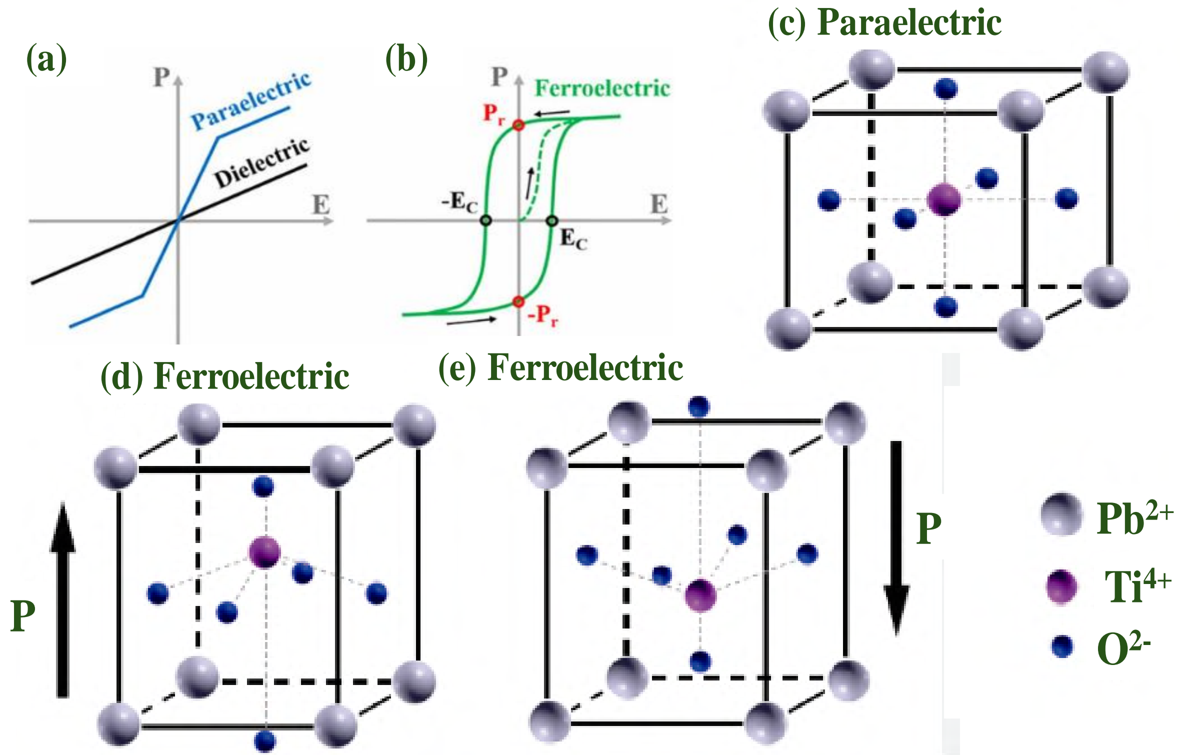

Figure 1.4: The plot of polarisation vs electric field for (a) paraelectric and (b) ferroelectric (DDVK22). Atomic structure of $Pb^{2+}Ti^{4+}{O_3}^{6-}$ for (c) paraelectric (d) ferroelectric with up polarisation (e) ferroelectric with down polarisation (WYSK15).

Figure 1.4 reveals the atomic structure of lead titanate ($PbTiO_3$) for (c) paraelectric and (d) ferroelectric with up polarisation (e) ferroelectric with down polarisation (WYSK15). The centrosymmetric property and linear dielectric are in paraelectic material. The non-centrosymmetric property and non-linear dielectric are in ferroelectric material (RAT07; Kha15).

The L-K and Miller models are often used to elucidate the polarisation (P) and voltage across ferroelectric (FE) materials (SDG18; LK54; Son05). However, L-K has received greater recognition. This section has focused on the L-K model. The Landau–Khalatnikov (L–K) equation is a dynamic formulation of the Landau–Devonshire theory as shown in Eq. 1.1. The L–K equation is a very useful tool for comprehending the ferroelectric switching features in the development of NCFET technology (SDG18; SD08). The Landau theory of nonlinear dielectric is given below:

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP, \alpha = \alpha_0[T - T^0] \tag{1.1}$$

Here, G is free energy density, α, β, γ are landau coefficients, P is polarization, and E is an electric

field.

The concept of negative capacitance is explained using the L–K equation, which describes the relationship between polarisation (P) and voltage (V) in a steady-state condition. In this equation, there is a region where the derivative of polarisation with respect to voltage is negative. The L-K model describes the temporal changes in the polarisation of a ferroelectric material. The L–K model also describes the charge–voltage characteristic of the ferroelectric material as depicted in Eq. 1.2. The landau Khalanikov (L-K) theory is given below:

$$\delta \frac{\partial P}{\partial t} = -\frac{\partial G}{\partial P} \tag{1.2}$$

here, δ is polarisation damping factor, P is polarization. On differentiating the Eq. 1.1 w.r.t. P, we get the electric field (E) by Eq. 1.3,

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \tag{1.3}$$

If E=0 means polarisation for paraelectric is zero (P=0) as shown in Figure 1.4(a) and (c), but polarisation for ferroelectric (P) =0, + P_r, - P_r. The two state of polaristion is formation for ferroelectric material by Eq. 1.4.

$$P_{\mathrm{r}} = +- \sqrt{(\sqrt{\beta^2 - 3\alpha\gamma} - \beta)/3\gamma} \tag{1.4}$$

1.2.3 Operation of NCFET

The NCFET's ferroelectric layer demonstrates a phenomenon known as negative capacitance, which can be comprehended using the Landau-Khalatnikov theory of ferroelectrics. The voltage is applied to the gate causes the ferroelectric layer to polarise, resulting in an amplification of the gate voltage. This amplification reduces the voltage needed to turn on and off of the transistor. Consequently, this leads to a more pronounced subthreshold slope and enhanced switching properties in comparison to conventional FETs.

The subthreshold swing (SS) is becoming the primary characteristic for low-power devices, as it determines their behavior in the subthreshold region using the equivalent capacitance model and device structure of NCFET as reveals in Figure 1.5(a) and (b) respectively. In conventional MOSFETs, the subthreshold slope is mathematically defined as the ratio of the logarithm of the change in drain current to the change in gate-source voltage. The logarithm of the drain current ratio represents the rate of change of the drain current. The SS of a FET device is the inverse of the subthreshold slope. Classical MOS devices experience a voltage sag of about 60 mV per decade at a temperature of 300 K, often referred as the "Boltzmann tyranny" (BCBD19; ZLH+19). To address these restrictions, researchers have created and improved a number of field-effect transistor devices that have a sharp subthreshold swing characteristic. The steady-state behavior of classical MOS devices is represented by the following model to show the SS by Eq. 1.5, Eq. 1.6, and Eq. 1.7:

$$SS = \frac{\partial V_{\mathrm{g}}}{\partial \log_{10}(I_{\mathrm{d}})} \tag{1.5}$$

$$SS = \frac{\partial V_{\mathrm{g}}}{\partial V_{\mathrm{int}}} \times \frac{\partial V_{\mathrm{int}}}{\partial \psi_{\mathrm{s}}} \times \frac{\partial \psi_{\mathrm{s}}}{\partial \log_{10}(I_{\mathrm{d}})} \tag{1.6}$$

$$SS = \frac{1}{A_{\mathrm{v}}} \times \frac{1}{m} \times \frac{\partial \psi_{\mathrm{s}}}{\partial \log_{10}(I_{\mathrm{d}})} \tag{1.7}$$

$$A_{\mathrm{v}} = \frac{\partial V_{\mathrm{int}}}{\partial V_{\mathrm{g}}} = \frac{C_{\mathrm{fe}}}{C_{\mathrm{fe}} + C_{\mathrm{int}}} \tag{1.8}$$

here, m is body factor, A_v is amplification factor, and A_v is greater than 1 in Eq. 1.8, C_s is negative, then body factor is always less than 1 as shown in Eq. 1.9.

$$m = \frac{\partial \psi_{\mathrm{s}}}{\partial V_{\mathrm{int}}} = (1 + \frac{C_{\mathrm{s}}}{C_{\mathrm{ox}}})^{-1} \tag{1.9}$$

The negative capacitance might be used to get high on the current and steep subthreshold swing. Recently, the phenomena of negative capacitance have been demonstrated in different systems experimentally: (i) superlattice, (ii) ferroelectric dielectric bilayer, and (iii) isolated ferroelectric

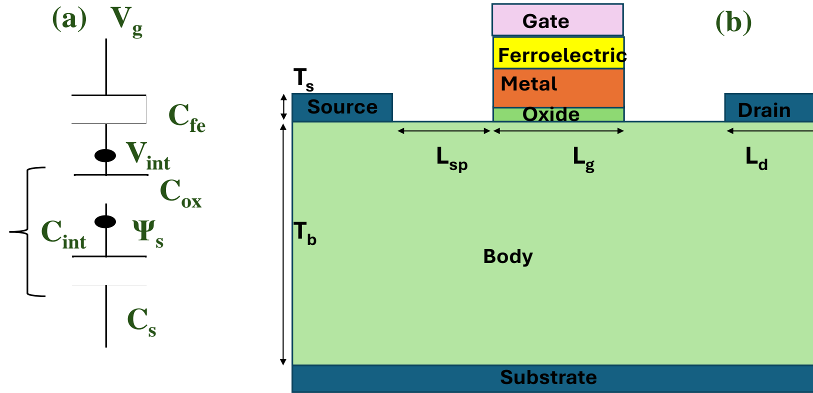

Figure 1.5: (a) Schematic diagram for equivalent capacitance model of NCFET and (b) Device structure of NCFET (Pah20).

film. The ferroelectric material is exploited to obtain the phenomenon of negative capacitance with negative slope of the curve as depicted in Figure 1.6(a). The steeper slope of negative capacitance is shown in Figure 1.6(b), which illustrates the curve of drain current and gate voltage for conventional MFIS vs MFMIS. MFMIS structure shows lower subthreshold swing as compared to MFIS. When we work on ferroelectric materials to exploit the property of negative capacitance, The unstable point on ferroelectric material gives negative capacitance phenomenon thus NCFET. It is difficult to reach the atom from left stable state to right stable state, also shown in Figure 1.6(c). So, the applied voltage should be higher than the coercive voltage, which can be defined as the voltage at which the net polarization of ferroelectric is zero, resulting in the creation of the metastable state that facilitates the negative capacitance phenomenon. Figure 1.6(d) illustrates the curve of polarisation vs electric field to represent the hysteresis loop for forward and backward sweeps. It also shows remnant polarisation and coercive field.

1.2.4 NCFET Device Engineering

NCFETs exist in several forms, distinguished by the precise manner in which the ferroelectric material is incorporated into the device structure. The following are the main categories of NCFETs as shown in Figure 1.7(a)-(f):

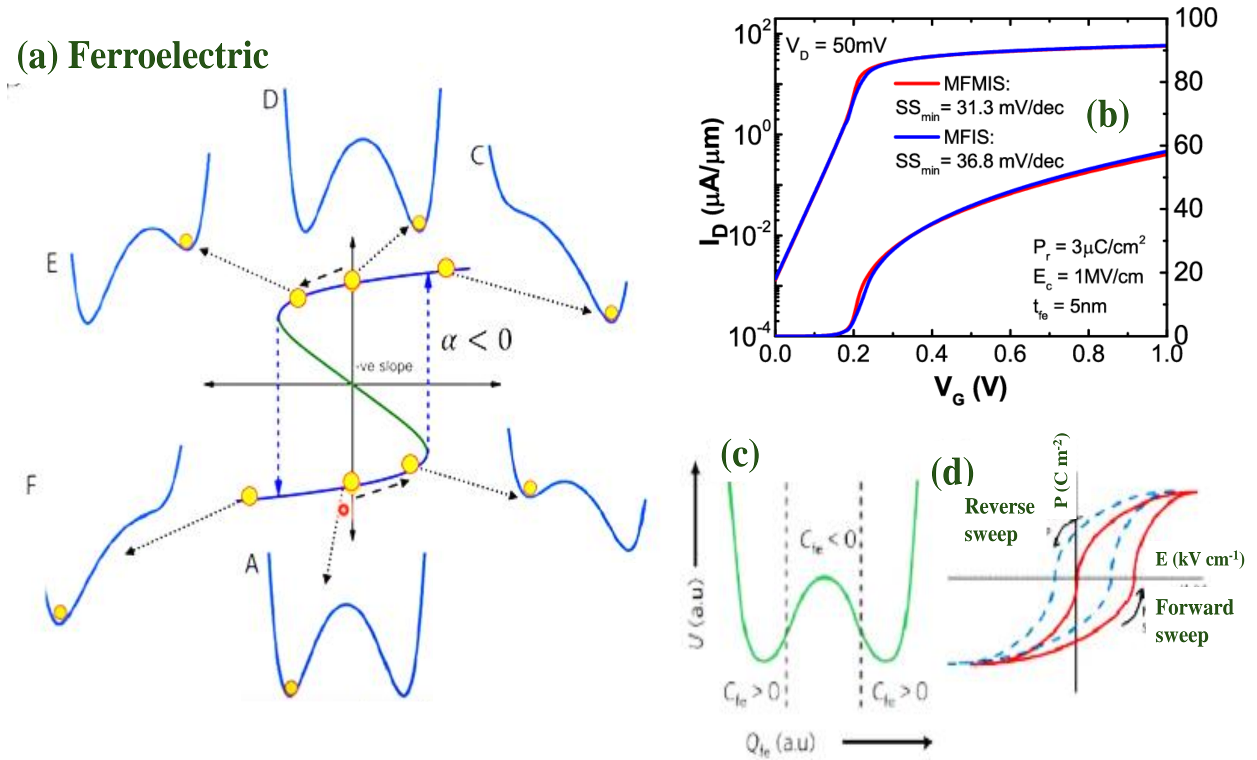

Figure 1.6: (a) The plot of polarisation vs electric field for NC (Kha15) (b) Drain current vs gate voltage graph for MFIS vs MFMIS (CB20) (c) Energy vs charge graph (MCM22) (d) Hystresis curve for NC.

1. Planar NCFET (Two-dimensional Nanoscale Channel NCFET): In planar NCFETs, the ferroelectric material is included into the gate stack of a conventional planar FET device. This variant is similar to traditional planar MOSFETs, except it has an extra ferroelectric layer as reveals in Figure 1.7(a).

Composition: The gate stack comprises a metallic gate, a ferroelectric layer, and a high-k dielectric layer, usually positioned above a silicon channel. It is well-suited for planar technology nodes and provides a more straightforward integration route with current planar CMOS processes.

2. NC FinFET: NC FinFET refers to a kind of transistor known as a Fin FET (FinFET) that integrate the ferroelectric layer into the gate stack of FinFETs, which are three-dimensional devices with channel as fins as shown in Figure 1.7(b).

Configuration: The ferroelectric layer is encased around the vertical fins that create the channel, together with a high-k dielectric and metal gate. It enhances electrostatic control in the channel, making it ideal for advanced technology nodes that use FinFETs to mitigate short-channel effects.

3. Fe-Ins-FET: The Ferroelectric-Insulator-FET (Fe-Ins-FET) is a kind of field-effect transistor that utilizes a ferroelectric insulator material. In Fe-Ins-FETs, the ferroelectric layer is integrated with an insulating layer instead of being directly connected to the semiconductor channel as shown in Figure 1.7(c).

Composition: The gate stack consists of a ferroelectric layer positioned above a conventional high-k dielectric, which is then followed by the metal gate. This engineering combines the advantageous characteristics of ferroelectric materials with the insulating capabilities of high-k dielectrics. It is well-suited for a range of applications that need both high performance and low power consumption.

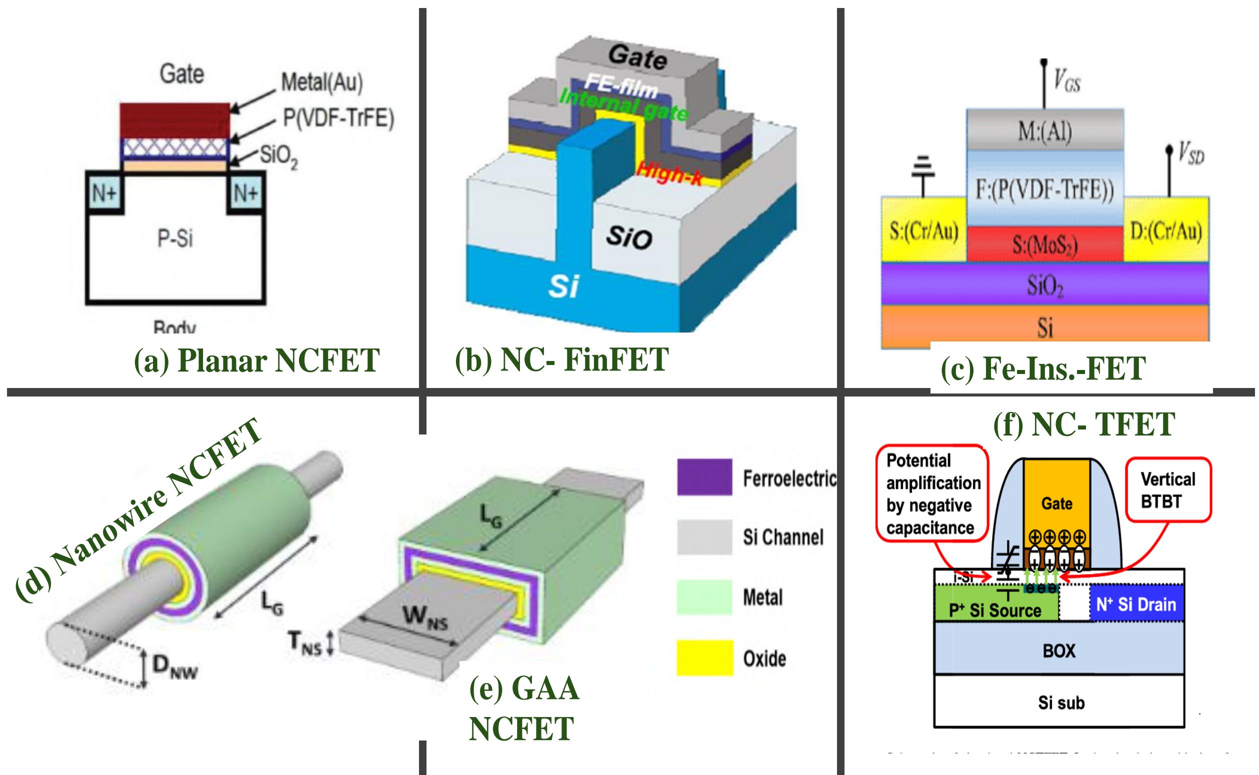

Figure 1.7: The schematic diagram of device engineering for (a) Planar NCFET (TWW+18) (b) NC FinFET (TWW+18)(c) Fe-Ins-FET (LKSH16) (d) Nanowire NCFET (SHH20) (e) GAA NCFET (SHH20) (f) NC-TFET (TWW+18).

4. Nanowire NCFET (Junctionless Nanowire Channel NCFET): Junctionless NCFETs distinguish themselves from conventional FETs by lacking a clearly defined source and drain junction as shown in Figure 1.7(d).

Structure: The channel area has a uniform distribution of dopants, and the flow of current is regulated by the voltage applied to the gate. Negative capacitance is achieved by integrating

a ferroelectric layer into the gate stack of nanowired channel FET. Its advantage is streamlined manufacturing by removing the need for accurate connection creation, which might be beneficial for reducing device size.

5. GAA NCFET (Gate-All-Around (GAA) NCFET): GAA NCFETs use a gate-all-around architecture, whereby the gate completely encloses the channel from all directions, therefore including the ferroelectric material in this arrangement as shown in Figure 1.7(e).

Composition: The channel is often constituted by nanowires or nanosheets, encased by a ferroelectric layer, high-k dielectric, and metal gate. Its advantage is providing superior electrostatic control, making it ideal for cutting-edge technological nodes and future iterations of highly miniaturized transistors.

6. NC-TFET (Negative Capacitance Tunnel FET): It is a type of field-effect transistor that combines the principles of negative capacitance and tunneling to achieve enhanced performance characteristics. This device leverages the unique properties of a ferroelectric material to provide negative capacitance, which help in further reducing the steep subthreshold characteristics of TFET thus give the super steep subthreshold swing as shown in Figure 1.7(f).

As different types of NCFETs depending on their structural integration with ferroelectric materials and engineering have been discussed above, each configuration has distinct benefits but also poses various obstacles on the incorporation of materials. Thus thorough and detailed engineering and optimisation are necessary to properly exploit the capabilities of NCFETs in different applications and technology nodes.

1.3 Advantages of NCFET

NCFETs provide numerous notable benefits compared to ordinary FETs, principally attributable to the distinctive characteristics of the ferroelectric material used in their gate stack. The following are the primary benefits:

1. Steep Subthreshold Swing:

    - Lower SS: NCFETs can achieve a subthreshold swing of less than 60 mV/decade,

which is the minimum limit for standard FETs at normal temperature. This enables quicker transitions between the activated and deactivated conditions by means of smaller changes in voltage.

- Lower operating voltage: Reduced subthreshold slope allows NCFETs to function at lower voltages without compromising performance, resulting in substantial use for low power applications.

2. Enhanced Energy Efficiency:

   - Lower Power Consumption: The capacity to function at lower voltages results in less dynamic power. This is essential for devices that rely on batteries and for applications that need significant computational power.
   - Reduce Leakage current: NCFETs have the ability to reduce leakage currents by effectively managing the channel at lower voltages. This capability aids in minimizing static power usage.

3. Increased Drive Current and Transconductance:

   - Higher I_{on}: The negative capacitance effect may amplify the driving current (I_{on}) of the transistor, hence improving its performance. Increasing the driving current enhances the transistor's speed.
   - Higher transconductance: The negative capacitance leads to an enhancement in the transconductance of the FET, resulting in enhanced amplification at quicker switching rates.

4. Compatibility with Existing Technology:

   - CMOS Compatibility: NCFETs may be seamlessly incorporated into current CMOS production methods with few modifications. This makes them a viable choice for the semiconductor industry seeking to improve existing technology without the need for a total restructuring of fabrication facilities.
   - Use of high-k dielectric: The use of high-k dielectric materials is prevalent in NCFETs since they are already widely used in modern CMOS processes, making integration more convenient.

5. Possibility for Innovative Applications:

- Low power logic and memory device: NCFETs provide significant benefits for low-power applications, including as portable electronics, IoT devices, and other power-sensitive applications.
- High performance computing: NCFETs are well-suited for high-performance computing workloads because to their enhanced performance characteristics, which are crucial for achieving both speed and power efficiency.

NCFETs have a significant benefit in a way that they can overcome the limitation of 60 mV/decade subthreshold swing barrier. This enables them to operate at lower voltages and achieve improved performance. NCFETs provide substantial energy efficiency, enhanced drive current, increased transconductance, and greater electrostatic control, positioning them as a very promising technology for forthcoming low-power and high-performance electronic devices.

1.4 Challenges Confronted by NCFET

Although NCFETs have certain benefits, they also encounter several problems that must be resolved in order to fully exploit their potential in practical applications. The NCFETs face many significant challenges such as:

1. Stability of Ferroelectric Materials:
    - Material degradation: Material degradation refers to the deterioration of ferroelectric materials, particularly when exposed to electric fields and heat conditions often seen in semiconductor devices. It is important to guarantee the enduring stability and dependability of these materials.
    - Fatigue and Hysteresis: Ferroelectric materials display hysteresis, resulting in device performance fluctuations. Fatigue, which refers to the progressive deterioration of ferroelectric characteristics due to repetitive cycling, is also a matter of concern.
2. Incorporation with CMOS Technology:
    - Process Compatibility: The use of ferroelectric materials into current CMOS production methods might provide difficulties. The deposition and patterning of these materials must be compatible with existing semiconductor production procedures.

- Thermal Budget: Ferroelectric materials sometimes need precise thermal treatments to get the appropriate characteristics. In order to prevent any harm to other components of the device, it is essential that these treatments be consistent with the temperature budget of the CMOS process.

3. Manipulation of Ferroelectric Characteristics:

   - Uniformity: It is difficult to achieve consistent ferroelectric characteristics across a wafer. Differences in device configurations might result in unreliable device functionality.
   - Scaling: As devices are reduced in size, it becomes more challenging to preserve the ferroelectric characteristics. Precise control is required for both the thickness of the ferroelectric layer and its contact with other materials.

4. Modelling and Simulation of Devices:

   - Complex behaviour: The behaviour of NCFETs is intricate compared to regular FETs because of the non-linear and hysteresis properties of the ferroelectric layer. Precise modelling and simulation techniques are necessary to predict device performance and provide guidance for design.
   - Parameter Extraction: Parameter extraction for NCFETs from experimental data is difficult owing to the intricate interaction between the ferroelectric layer and the underlying FET structure.

5. Balancing Power and Performance:

   - Optimization: To optimise the NCFETs, one must carefully balance the advantages of power and performance with the possible disadvantages of greater variability and hysteresis. This involves meticulous optimisation of both device designing and operating circumstances.
   - Energy Efficiency: Energy efficiency is a crucial consideration when using NCFETs to lower the power consumption. It is necessary to prevent any rise in leakage currents or other inefficiencies that might inhibit the advantages achieved.

6. Ferroelectric Layer Material:

   - Material Selection: It is essential to choose the appropriate ferroelectric material with sufficient characteristics for integration into NCFETs. Materials such as hafnium oxide

(HfO_2) that have been modified with dopants to show potential, but more investigation is required to enhance their characteristics.

- Ferroelectric Layer Thickness: The thickness of the ferroelectric layer is of utmost importance. The material should have a sufficiently small thickness to demonstrate negative capacitance, while yet being thick enough to preserve its ferroelectric characteristics.

7. Temperature Sensitivity:

   - Thermal stability: Thermal stability refers to the extent to which the performance of ferroelectric materials is influenced by temperature. It is crucial to guarantee the reliable operation of NCFETs over a broad range of temperature for practical purposes.

8. Variability and Reliability:

   - Device-to-Device Variability: Ensuring consistent performance across various devices on a chip is a significant challenge. Inconsistencies in device properties might arise from variations in the ferroelectric layer or its contact with other materials.
   - Long-Term Reliability: It is crucial to establish that NCFETs can sustain their performance and advantages over prolonged periods of use in order to facilitate their acceptance in commercial applications.

Summary Although NCFETs show potential benefits, there are still notable obstacles regarding material stability, integration with current CMOS processes, control of ferroelectric properties, device modelling, power-performance trade-offs, ferroelectric layer engineering, temperature sensitivity, and overall device reliability. To ensure the effective integration of NCFET technology in future electronic devices, it is crucial to address these problems by conducting more research and development.

1.5 Proposed Device

Different types of NCFETs depending on their structural integration with ferroelectric materials and engineering such as Planar NCFET, NC FinFET, Nanowire NCFET, NC Tunnel FET, etc have been analysed in various literature, each configuration has distinct benefits but also poses various obstacles in their functioning like ferroelectric material stability, control of ferroelectric

properties, power-performance trade-offs, temperature sensitivity, and overall device reliability. To counter these challenges, a new device structure, DM NCFET (Double Metal NCFET) is proposed and examined in this thesis. It comprises two metallic layers below the ferroelectric material with stacked insulator in between, resulting in MFMIMIS (Gate Metal-Ferroelectric-Metal-Insulator-Metal-Insulator-Semiconductor) configuration. The idea behind the inclusion of metal layers in the structure is due to its several benefits. The metal layer helps in redistributing the electric field across the ferroelectric and insulator layers. The metal layer also acts as a barrier, preventing direct tunnelling currents between the semiconductor and ferroelectric layers, thus enhances device reliability by minimizing leakage. The metal layer also provides better control over the interface properties, which reduces hysteresis effects in the ferroelectric layer. The metal layer can act as a heat sink, dissipating heat generated during device operation, thus improves the thermal stability and longevity of the device. Further, by isolating the ferroelectric and insulator layers, the metal layer minimizes defects at their interface, thus enhances the overall performance and reliability of the device. Subsequently, spacer technology is also incorporated in the DM NCFET configuration to form DM-NCFET (spacer) to further improve device performance and scalability. Spacers are typically insulating materials, such as silicon nitride (SiN) or silicon dioxide (SiO), formed on the sidewalls of the gate stack. They reduce hot-carrier injection (HCI), thereby improves device reliability and reduces electric field peaks at the drain junction. Spacers electrically isolate the gate electrode from the source/drain regions, thus prevent parasitic capacitance and any associated leakage paths. Spacers also help in achieving self-aligned source and drain regions during fabrication. So, by providing precise control over doping, isolation, and stress, spacers in general enhance the reliability and efficiency of the device. Thus, this proposed structure presents a promising direction for overcoming the limitations of conventional NCFETs, especially as technology nodes scale down. It provides a pathway to achieve a more promising device for meeting the demands of modern electronics.

1.6 Research Objectives

1. Dual Material Double Gate (DM-DG) engineering can be implemented on the proposed device to improve the SCEs and carrier transport efficiency.

2. Direct Source to Drain Tunneling (DSDT), SCEs and Analog Figures of Merit (FOM) can be further improved by applying spacer on the proposed device.

3. To analyze the linearity performance and high frequency RF performance of the proposed device structure.

4. To analyze the Effect of Temperature on Double Metal NCFET (DM NCFET).

5. To design a bio-chemical sensor by introducing a nano-cavity gap above the gate dielectric, which can sense both harmful as well as bio-molecules such as proteins, DNA, glucose or in cancer detection.

1.7 Thesis Organisation

To summarize, the NCFET structure utilizes a ferroelectric layer to exploit negative capacitance phenomenon, resulting in significant advantages such as reduced power consumption and improved performance. This makes it a highly promising technology for future electronic industry.

Chapter 1 explains the drawbacks of MOSFETs and the need for NCFETs. It provides an overview of subthreshold swing (SS), short-channel effects (SCEs), and MOSFET scaling issues. The chapter covers methods for overcoming SS and SCEs, introducing various engineering schemes such as Planar NCFET, Junctionless Engineering, NC FinFET, NC TFET, and Fe-Ins-FET, as documented in research publications. It then discusses the design, classification, basic operation, potential benefits, and challenges of NCFETs. Further, it gives a brief idea of the proposed device formed with the amalgamation of several technologies to overcome the limitations of conventional NCFETs. The chapter concludes by outlining the thesis's structure and objectives, emphasizing the importance of this research.

Chapter 2 explores the analog and radio frequency (RF) performance of ferroelectric layer-enhanced field-effect transistor devices, specifically DM-NCFET with and without spacers. The proposed DM-NCFET (spacer) shows a 25% increase in ON-current (I_{on}), a 37% reduction in leakage current (I_{off}), a 99% enhancement in the switching ratio (I_{on}/I_{off}), a 0.29% increase in threshold voltage (V_{th}), and a 17.6% decrease in drain-induced barrier lowering (DIBL) compared to DM-NCFET without spacers. The analog parameters such as transconductance generation

factor (TGF), transconductance (g_m), intrinsic gain (A_v), early voltage (V_{ea}), intrinsic delay (T_i), and RF parameters like gain transconductance frequency product (GTFP), cut-off frequency (F_t), and gain frequency product (GFP) are also examined. The study finds that the DM-NCFET (spacer) performs better at room temperature (300K) compared to higher temperatures (400K and 500K). Additionally, the variation in gate electrode work functions—Palladium, Chromium, and Tungsten—is analyzed, with Palladium showing the most improved performance. These results indicate that DM-NCFET (spacer) with Palladium gate material offers enhanced performance for nanoelectronic devices and IC design.

Chapter 3 investigates the application of DM-NCFET for biosensing, focusing on the impact of nano-cavity gaps with biomolecules like proteins, Cholesterol oxidase (ChO_x), streptavidin, and uricase. The electrical characteristics and neutral biosensing capabilities, including threshold voltage and switching ratio (I_{on}/I_{off}), show significant improvement with biomolecules. The sensitivity of the device increases by 1.11 times for protein, and the limit of detection improves by 1.012 times compared to without biomolecules. The study examines the effect of cavity length (from 8nm to 12nm) on sensitivity, finding that increased cavity length enhances biosensor sensitivity. Visual TCAD software is used for all the simulations. The results suggest that DM-NCFET biosensors offer high sensitivity at low drain voltage (0.4V), making them suitable for low-power, high-density, and high-speed biosensor applications to detect various infections.

Chapter 4 investigates the analog/RF and linearity parameters of SM DGNCFET (Single Metal Double Gate NCFET) and DM DGNCFET (Double Metal Double Gate NCFET) using the Cogenda Visual TCAD simulator. It also demonstrates the enhancement in electronic and optical properties of Si-doped bulk structures using Quantum ATK. The analog parameters for SM DGNCFET show significant improvements: the switching ratio is 279 times better, DIBL is 54% lower, SS swing is improved, and other parameters like transconductance, TGF, and RF performance are enhanced. The transconductance frequency product (TFP) improves the reliability and stability of the device. Linearity parameters such as second-order and third-order transconductance (g_{m2}, g_{m3}) and voltage intercept points for 2nd order and 3rd order are also examined. The Tran Blaha modified Becke Johnson (TB-mBJ) approximation provides an accurate band gap of the crystal. In a DFT-based atomic study, 12.5% Si doping in a bulk structure reveals better results for ferroelectric HfO_2 based crystals, with a zero direct band gap and improved density of states

(DOS) for conductivity. Hence, Si doping in the crystal structure enhances conductivity.

Chapter 5 explores an accurate machine-learning approach for predicting various key analog and RF parameters of NCFETs Visual TCAD simulator and Python were employed for the simulations, though the computational cost was high. This machine-learning approach is a novel method for predicting the effects of different sources on NCFETs while reducing the computational costs. An artificial neural network algorithm effectively predicts multi-input to single-output relationships, enhancing existing techniques. The analog parameters of Double Metal Double Gate Negative Capacitance FETs (DM DGNCFET) are demonstrated across various temperatures (T), oxide thicknesses (T_{ox}), substrate thicknesses (T_{sub}), and ferroelectric thicknesses (T_{Fe}). Notably, at $T = 300K$, the switching ratio is higher, and leakage current is 84 times lower compared to $T = 500K$. Similarly, at $T_{Fe} = 4nm$, the switching ratio improves by 5.4 times compared to $T_{Fe} = 8nm$. Furthermore, at $T_{sub} = 3nm$, the switching ratio increases by 81% compared to $T_{sub} = 7nm$. For oxide thicknesses at $T_{ox} = 0.8nm$, the ratio increases by 41% compared to $T_{ox} = 0.4nm$. The analysis reveals that $T_{Fe} = 4nm$, $T = 300K$, $T_{ox} = 0.8nm$, and $T_{sub} = 3nm$ represent optimal settings for DM DGNCFET, resulting in significantly improved performance. These findings can be very useful for various applications in nanoelectronic devices and integrated circuit (IC) design.

Chapter 6 investigates the experimental circuit designing of FET, based on the basic structure of an ion-sensitive FET (ISFET), for pH sensing. After analyzing the ISFET design, further work was conducted on DM-NCFET for enhanced pH sensing. Both theoretical and experimental studies were performed, focusing on the analog characteristics of ISFETs and their circuit designing for pH sensing. The gate electrode work function in ISFET was rigorously examined for analog/RF applications using the Cogenda Visual TCAD tool. Based on the I-V characteristics, it was deduced that molybdenum, with a work function of 4.75 eV, exhibits a higher threshold voltage, a better switching ratio (10^4), and lower leakage current (10^{-3}) than aluminum at 300K. Comparative studies of ISFET sensing layers (Al_2O_3, Si_3N_4, SiO_2) indicated that Al_2O_3 showed the best results for switching ratio, leakage current, sensitivity, and transconductance. The enhancement in pH sensing was also demonstrated experimentally with the proper circuit design of ISFET. However, ISFETs display instability, often referred to as drift, characterized by a gradual, monotonic increase in the device's threshold voltage over time. The validation of these observations was conducted by

increasing the pH values to 4.67, 5.9, 7.5, 8.57, and 9.3, as measured by a pH meter.

Chapter 7 offers a comprehensive summary of the research conducted for this thesis, highlighting the key conclusions and results. It also explores the potential future applications of the present study and considers how to build on and utilize this research in other projects.

Chapter 2

Effect of Temperature and Work Function Variation on Double Metal NCFET with Spacer Engineering

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* This chapter discusses the impact on analog and RF parameters of Double Metal NCFET with spacer (DM-NCFET(spacer)) to achieve the better performance of the device.
* It is found that the switching ratio is enhanced for DM-NCFET(spacer) by 99% in comparison to DM-NCFET without spacer engineering, along with significant improvements in some other analog and RF parameters such as transconductance, TGF, early voltage, unity gain cut off frequency etc.
* In addition, the variation of temperature and gate electrode material for DM-NCFET(spacer) is also explored for optimizing the device to show better performance.
* Consequently, the DM-NCFET(spacer) shows the improved analog/RF performance with low power consumption. Also the analysis done for variation of temperature and impact of gate electrode material will aid engineers in designing the device for various high performance applications.

2.1 Introduction

Achieving faster speed in line with Moore's law, which predicts the doubling of transistor density approximately every eighteen months, has been realized with minimal power dissipation through adaption of several engineering and technologies. Power dissipation (P) scales with the supply voltage ($P = V_d^2$), where V_d is typically constrained by the minimum subthreshold swing (SS = 60mV/dec) of a thermally activated Boltzmann switch (KJMA15). Gordon E. Moore's observation highlights the exponential growth of transistor count in a given space (Wal16; PMC22b). Recently, ferroelectric field-effect transistors (Fe-FETs) have garnered significant attention for their potential in both memory and switching applications (LCL+15; MBP+08). Size and power consumption are critical metrics for modern electronic devices, driving ongoing research toward developing aggressively scaled devices that consume ultra-low power (LFT+16). To meet these challenges, there has been considerable interest in alternative devices that operate on fundamentally different mechanisms, allowing a more efficient transition between the off and on states of an electronic switch (MBP+08).

Ferroelectric layer-enhanced performance field-effect transistors, particularly NCFETs, can achieve sub-60-mV/decade SS and high ON current. Recently, the negative capacitance phenomenon has been experimentally demonstrated in various systems: 1) isolated ferroelectric layers, 2) ferroelectric-dielectric bilayers, 3) superlattices, and 4) ferroelectric-gated transistors (LKSH16; BLH+18). However, NCFET research has not fully addressed the impact of channel length scaling. Additionally, the Landau model is applied only to the out-of-plane polarization component, with Landau parameters for the ferroelectric material being $\alpha = -1.0 \times 10^{+7}$ and $\beta = 8.9 \times 10^{+8}$ (AKYU21), which are not suitable for thicker ferroelectric layers. Previous studies have analyzed the performance of NCFETs with long channels using analytical modeling (VRPS17). While NCFETs typically provide higher ON-state currents compared to other configurations, this is not always the case for all ferroelectric materials. Moreover, a comprehensive understanding of the behavior and performance of these structures is still lacking in the literature.

In this study, we conduct a thorough comparative analysis between DM-NCFET (spacer) and other NCFET structures. In the DM-NCFET structure, metal layers are inserted between the

ferroelectric layer and the gate insulator, creating an equipotential surface at the inner gate. This allows the ferroelectric and the underlying MOSFET to be managed as two separate circuit elements connected by a wire (PDAC17). Further spacer engineering is incorporated in the DM-NCFET to further improve the device performance. This chapter discusses the impact on analog and RF parameters of Double Metal NCFET with spacer (DM-NCFET(spacer)) to achieve the better performance of the device. Simultaneously a comparison between DM-NCFET (spacer) and DM-NCFET without spacer engineering have been made for all the discussed parameters. In addition, the variation of temperature and gate electrode material for DM-NCFET(spacer) is also explored for optimizing the device to show better performance. So the detailed analysis done on the device to know the impact of spacer engineering, variation of temperature and impact of gate electrode material will aid engineers in designing the device for various high performance applications.

2.2 Device Architecture

There are two schematics represented as Figure 2.1(a), showing metal ferroelectric metal insulator metal oxide transistor with spacer as DM-NCFET (spacer), and Figure 2.1(b) showing metal ferroelectric metal insulator metal oxide transistor without spacer as DM-NCFET.

Table 2.1: Parameters used for the simulation of DM-NCFET (spacer) and DM-NCFET

Parameter	DM-NCFET (spacer)	DM-NCFET
Gate length (L_g)	20 nm	20 nm
Oxide Thickness (T_{ox})	1 nm	1 nm
Drain/Source length ($L_{d/s}$)	10 nm	10 nm
Drain/ Source thickness ($T_{d/s}$)	3 nm	3 nm
Body thickness (T_b)	50 nm	50 nm
Ferroelectric thickness (T_{fe})	1 nm	1 nm
Insulator thickness (T_{ins})	2.2 nm	2.2 nm
Concentration of Body (N_b)	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Concentration of Drain/ Source ($N_{d/s}$)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Length of Spacer1/Spacer2 ($L_{sp1/sp2}$)	10nm	10nm

The Body length (L_b) is 60nm, Drain/Source length ($L_{d/s}$) is 10nm, the Spacer1/Spacer2 length ($L_{sp1/sp2}$) is 10nm, Body thickness (T_b) is 50nm, Drain/Source thickness ($T_{d/s}$) is 3nm, Oxide thickness (T_{ox}) is 1nm, Ferroelectric thickness (T_{fe}) is 1nm, Gate/Metal2 ($T_{g/m2}$) thickness is

2nm, Insulator thickness (T_{ins}) is 2.2nm as depicted in Table 2.1. The total gate length (L_g) is 20nm for DM-NCFET (spacer) and DM-NCFET. The thickness of the total gate (T_{gt}) is 10nm DM-NCFET (spacer) and DM-NCFET.

As shown in Figure 2.1(a) and (b), the material of the Body is Si (silicon), the material of Drain/Source/Substrate/Gate is Al (Aluminium), the material of Spacer1/Spacer2 is Silicon Nitride, the material of Oxide is SiO_2 (silicon dioxide) and material of ferroelectric is HfO_2FE (silicon doped hafnium dioxide). A proposed device DM-NCFET (spacer) involves a gate, ferroelectric, metal, insulator, metal, silicon dioxide, and silicon from top to bottom along with the adaptation of spacer engineering between gate dielectrics and source/drain. The doping concentration of Body (N_b) is 1×10^{16} cm^{-3} with Uniform profile and acceptor type, the doping concentrating of Drain /Source ($N_{d/s}$) is 1×10^{20} cm^{-3} with Gaussian profile and donor type.

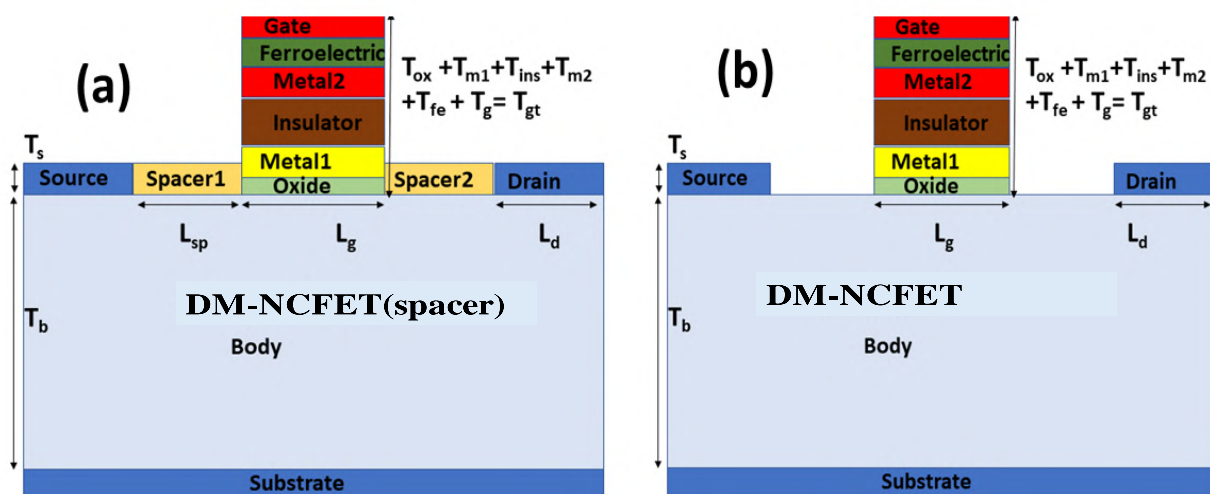

Figure 2.1: The two different DM-NCFET schematics structure (a) DM-NCFET with spacer (b) DM-NCFET (PMC22b).

2.3 Method of Simulation

All simulations are conducted using the Visual TCAD simulator. A comparison is made between two devices: DM-NCFET (spacer) and DM-NCFET. The drain voltage, V_d, is fixed at 0.3V throughout the process, while the gate voltage, V_{gs}, is varied from 0V to 3V. The temperature (T) is held constant at 300K for the first case of device simulation . In the second case, the temperature variation on the DM-NCFET (spacer) is examined. Different boundary conditions are applied to

implement the DM-NCFET (spacer) and DM-NCFET designs. In the DM-NCFET structure, the continuity of normal components of displacement vectors is used at the oxide/spacer ferroelectric boundaries(HPC+16a; SKW+17). To encounter key phenomena in the device, various models are used in the simulation. The Shockley-Read-Hall (SRH) model is used to account the generation and recombination of the carriers while the Lombardi surface mobility model is used to account for carrier mobility, complemented by Fermi-Dirac statistics. The Arora model considers the effects of temperature and impurity concentration on carrier mobility along with Crowell Sze that accounts for impact ionization. Different boundary conditions were applied to implement the designs of the DM-NCFET(spacer) and DM-NCFET. The congruence of typical sections of translation vectors are used at the oxide-ferroelectric interfaces in the DM-NCFET structure. The internal metal gate serves as a floating terminal in the DM-NCFET structure (HPC+16b; MPAS15).

2.4 Result & Discussion

2.4.1 Device Scalability

Figure 2.2(a) shows the variation of drain current (I_d(mA)) with gate voltage (V_{gs}(V)) for DM-NCFET (spacer) and DM-NCFET in linear scale and in log scale at V_d=0.3V. The drain current of DM-NCFET (spacer) is better than the DM-NCFET configurations along with reduced leakage current I_{off} as shown in the left side of the graph. The spacer on DM-NCFET enhances the formation of the inversion layer at the interface, allowing more carriers to contribute to the current (GC16; SFZ+18). With an increase in gate voltage, more carriers are available, resulting in a higher drain current (SN21).

Figure 2.2(b) shows that the threshold voltage (V_{th}(V)) of DM-NCFET (spacer) is enhanced as compared to DM-NCFET device configurations at V_d =0.3V due to increased gate control over the channel. It also indicates that structure DM-NCFET (spacer) is the better shield of drain-side potential that has improved the characteristics of the threshold voltage. The spacer acts as an insulating layer between the gate and the drain/source regions, which helps in reducing the electric field coupling from these regions to the channel. This reduces short-channel effects where the drain voltage can influence the channel. By minimizing these effects, the threshold voltage becomes

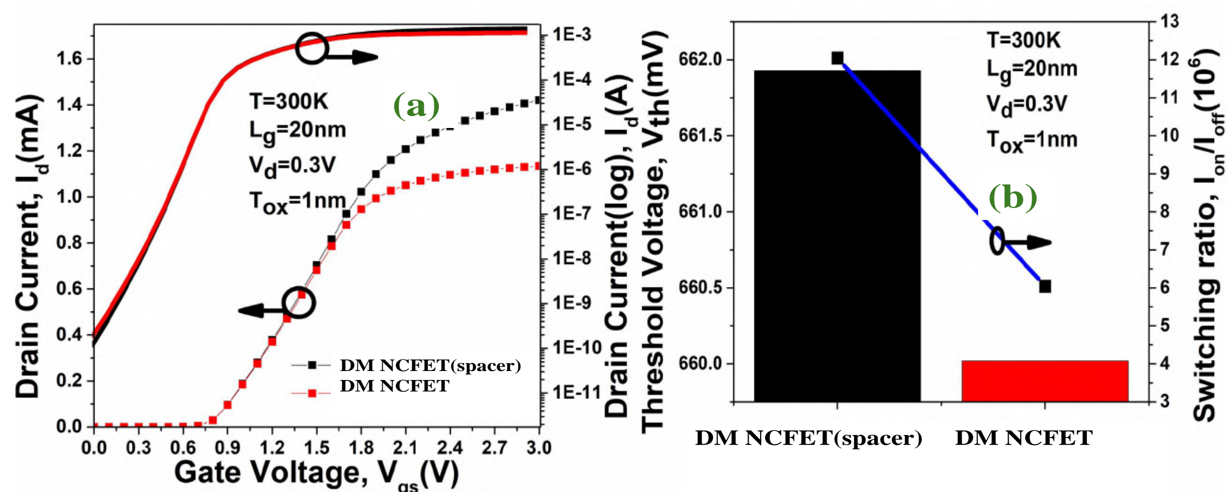

Figure 2.2: (a) The curve of drain current vs gate voltage in linear and log scale (b) comparison of V_{th} (V) and switching ratio at V_d=0.3V for DM-NCFET(spacer) and DM-NCFET (PMC22b).

more stable and increases for DM-NCFET (spacer). The switching ratio, I_{on}/I_{off} of DM-NCFET (spacer) is higher than the other DM-NCFET structure at V_d=0.3V, ensuring high switching speed for DM-NCFET (spacer) structure, as also depicted in Table 2.2. The spacer on DM-NCFET helps in reducing the leakage current by isolating the gate from the drain/source. This allows for a better distinction between the "on" and "off" states, leading to a higher switching ratio. This enhances the device's efficiency in digital applications by improving its ability to switch between states with less leakage in the off-state (P^+24).

2.4.2 Analog Analysis

In this subsection, analog performance metrics are discussed in terms of transconductance (g_m), transconductance generation factor (TGF), output conductance, early voltage (V_{ea}), intrinsic gain (A_v).

Here, transconductance (g_m) is a parameter that quantifies the shift in drain current to shift in gate voltage at drain voltage of 0.3V and at T=300K, as given by Eq. 2.1. The transconductance peak of DM-NCFET(spacer) is higher than the DM-NCFET structures as revealed by Figure 2.3(a). The spacer improves gate control over the channel, allowing for better modulation of the channel's conductivity with changes in gate voltage(MPAS15). This results in higher transconductance,

meaning that the device can generate more current for a given change in gate voltage, enhancing overall performance (NG18).

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} \tag{2.1}$$

$$TGF = \frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} \tag{2.2}$$

$$g_{\mathrm{d}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{d}}} \tag{2.3}$$

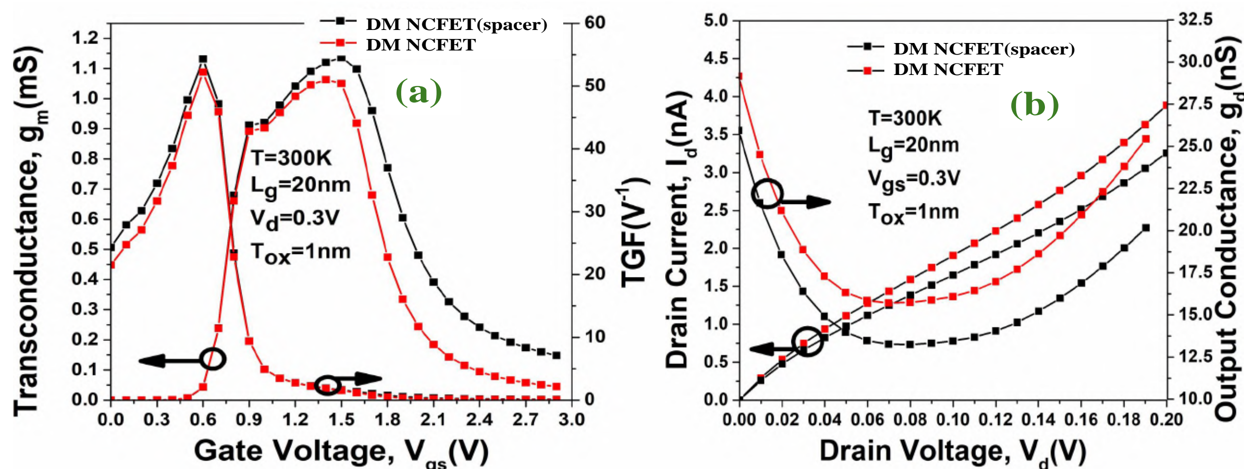

Figure 2.3: The curve of different structures at V_d=0.3V (a) transconductance and transconductance generation factor vs gate voltage (b) drain current and output conductance vs drain voltage (PMC22b).

Transconductance generation factor (TGF) is gain generated per unit power loss. TGF of DM-NCFET(spacer) is increased as compared to DM-NCFET configuration, close to ideally $50\mathrm{V}^{-1}$ as shown in right side Figure 2.3(a). The device operation at low supply voltage shows more efficiency with a high value of TGF as calculated using Eq. 2.2. The change in TGF between two configurations is observed in the subthreshold region. With the spacer in DM-NCFET reduces the leakage current and improves the transconductance, which results in enhancement of TGF. A higher TGF indicates that the device maintains efficient gate control while minimizing power

losses, leading to more energy efficient operation. Figure 2.3(b) represents the graph of drain current (I_d(A)) and output conductance ($g_d(nS)$) vs drain voltage, V_d(V) at gate voltage V_{gs} of 0.3V. Output conductance is the driving capacity of the device as characterized by Eq. 2.3 mirrors the locale of device activity.

$$V_{\text{ea}} = \frac{I_{\text{d}}}{g_{\text{d}}} \tag{2.4}$$

$$A_{\text{v}} = \frac{g_{\text{m}}}{g_{\text{d}}} \tag{2.5}$$

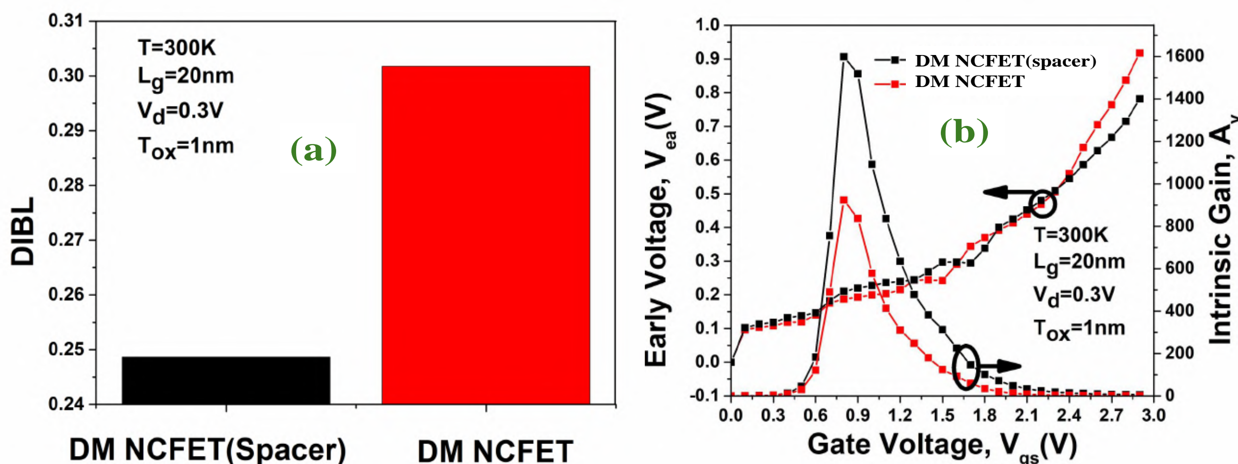

Figure 2.4: Graph of different structures at V_d=0.3V showing (a) drain induced barrier lowering (b) Variation of early voltage and intrinsic gain vs gate voltage at T=300K (PMC22b).

At first, a high output conductance in the linear region is observed with increasing drain voltage beyond pinch-off voltage owing to DIBL as well as channel length modulation (CLM) (AS15). The g_d twist of DM-NCFET (spacer) is lower than DM-NCFET that shows upgraded gate controllability in the device as portrayed in Figure 2.3(b). The spacer on DM-NCFET helps to isolate the gate from the drain/source, which reduces the impact of the drain voltage on the channel, ultimately results in lower output conductance.

Figure 2.4(a) shows that the bar graph of drain induced barrier lowering for different configuration at T=300K. It is one of the type of short channel effects that occurs in devices with short

channel. DIBL of DM-NCFET (spacer) is lower than DM-NCFET structure. Without the spacer on DM-NCFET, there is a stronger interaction between the drain and the channel, leading to higher output conductance. The spacer minimizes this interaction, resulting in less dependence of the drain current on the drain voltage. Also the spacer acts as a buffer that reduces the drain's control over the channel, thereby reducing DIBL and improving the performance of DM-NCFET (spacer).

Figure 2.4(b) reveals the variation of early voltage and intrinsic gain vs gate voltage for different configurations at V_d=0.3V, oxide thickness of 1nm, and channel length of 20nm. These parameters are evaluated by using Eq. 2.4 and Eq. 2.5. The higher value of intrinsic gain is resulted from the high value of transconductance and lower output conductance due to better controlling of the channel potential. The higher early voltage for DM-NCFET (spacer) as depicted in Figure 2.4(b), is resulted due to reduced DIBL and better output resistance, which makes the device crucial for various analog applications(MGC17b; KTC18; MGC17a).

2.4.3 RF (Radio Frequency) Analysis

In the RF analysis, various RF parameters are considered such as gate capacitance, gate charge (Q_g), unity gain cutoff frequency (F_t), gain frequency product (GFP), and gain transconductance frequency product (GTFP). Figure 2.5(a) represents the variation of gate capacitance (C_{gg}(F/um)) vs gate voltage for all configurations at V_d=0.3V, channel length of 20nm, and oxide thickness of 1nm. The gate capacitance of DM-NCFET (spacer) is higher than that of other structures, which reflects an enhanced amount of stored charges at a particular voltage. With the introduction of spacer in DM-NCFET (spacer), the electric field lines from the gate do not only go straight down through the ferroelectric layer but also curve around, passing through the spacer. These are called fringing fields, and they increase the effective area through which the electric field interacts with the channel, leading to higher gate capacitance. Figure 2.5(a) also indicates that cut off frequency of DM-NCFET (spacer) is higher than that for DM-NCFET configuration due to larger enhancement in transconductance in comparison to rise in gate capacitance as depicted in Eq. 2.6.

Figure 2.5(b) indicates the curve of intrinsic delay vs gate voltage. The intrinsic delay of DM-NCFET (spacer) is lower than other structures as calculated by Eq. 2.7 (PMC21b). It is the time

interval taken by the device to give output after applying input thus low value reflects less input power consumption (MPAS15). The spacer provides better isolation between the gate and the drain, reducing the impact of drain voltage variations on the gate control. This leads to faster switching and reduced delay. The gate charge of DM-NCFET (spacer) is higher than other structures that is reflected in higher gate capacitance for DM-NCFET (spacer). The improved electrostatic control from the spacer reduces carrier scattering and accelerates charge carriers through the channel, thus lowering the transit time which is directly linked to the intrinsic delay.

$$F_{\mathrm{t}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gg}})} \tag{2.6}$$

Table 2.2: Comparison of different performance parameters for different configurations at T_{ox}=1nm, T=300K and L_g=20nm

Parameter	DM-NCFET (spacer)	DM-NCFET
I_{on} (A)	0.001421	0.001135
I_{off} (A)(10^{-10})	1.18	1.88
DIBL	0.248673	0.30171177
$I_{on}/I_{off}(10^{-6})$	12.0424	6.0372
$V_{th}(mV)$	661.929	660.0196

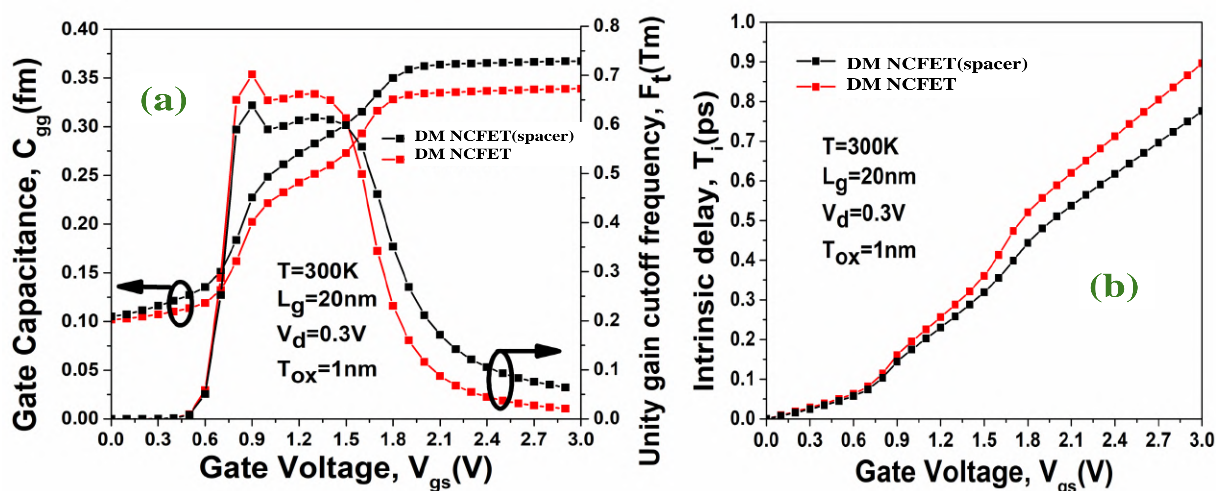

Figure 2.5: Variation of (a) gate capacitance vs gate voltage and cutoff frequency vs gate voltage (b) intrinsic delay vs gate voltage for different structures with V_d=0.3V and L_g = 20nm at T=300K (PMC22b).

$$T_{\mathrm{i}} = \frac{C_{\mathrm{gg}} \times V_{\mathrm{d}}}{(I_{\mathrm{on}})} \tag{2.7}$$

$$GFP = (\frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}) \times F_{\mathrm{t}} \tag{2.8}$$

$$GTFP = (\frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}) \times (\frac{g_{\mathrm{m}}}{I_{\mathrm{d}}}) \times F_{\mathrm{t}} \tag{2.9}$$

Figure 2.6 shows the Electric field contour with (a) DM-NCFET (spacer) from 0 to 8.661E+06 and (b) DM-NCFET from 0 to 8.404E+06 at V_d=0.3V, T=300K. The electric field is higher in the area of contour from gate to drain side for DM-NCFET (spacer). The spacer in DM-NCFET improves the distribution of the electric field within the channel, focusing it in the active region between the source and drain. This increases the overall electric field strength in the channel, which helps to accelerate charge carriers thus improving both the drive current and switching speed.

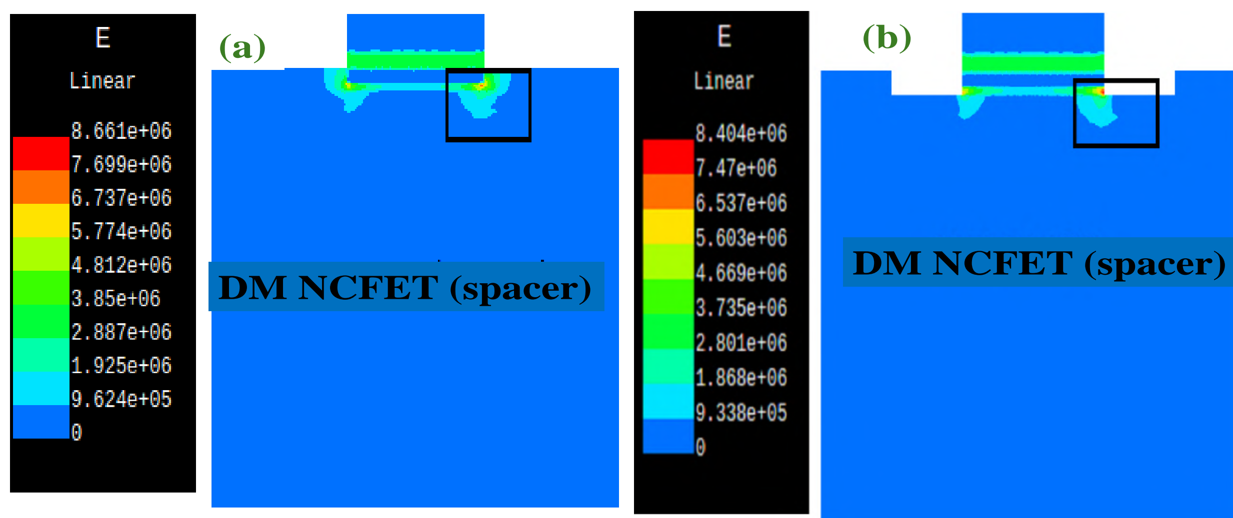

Figure 2.6: Electric field contour with (a) DM-NCFET (spacer) from 0 to 8.661E+06 and (b) DM-NCFET from 0 to 8.404E+06 at V_d=0.3V and T=300K.(PMC22b).

Figure 2.7(a) reflects the variation of gain frequency product (GFP) and gain transconductance frequency product (GTFP) vs gate voltage for different structures at V_d=0.3 and T=300K. GFP represents the trade-off between the gain (amplification) of the device and its operating frequency as determined by Eq. 2.8(MPAS15). It is seen from Figure 2.7(a), GFP increments as the gate voltage increases and afterward accomplishes a greatest top prior to tumbling to a constant value in the saturation locale. DM-NCFET (spacer) records the higher value of GFP because of higher transconductance with small rise in cut-off frequency. The spacer on DM-NCFET reduces signal loss due to parasitics, ensuring that the gain remains stable even at higher operating frequencies.

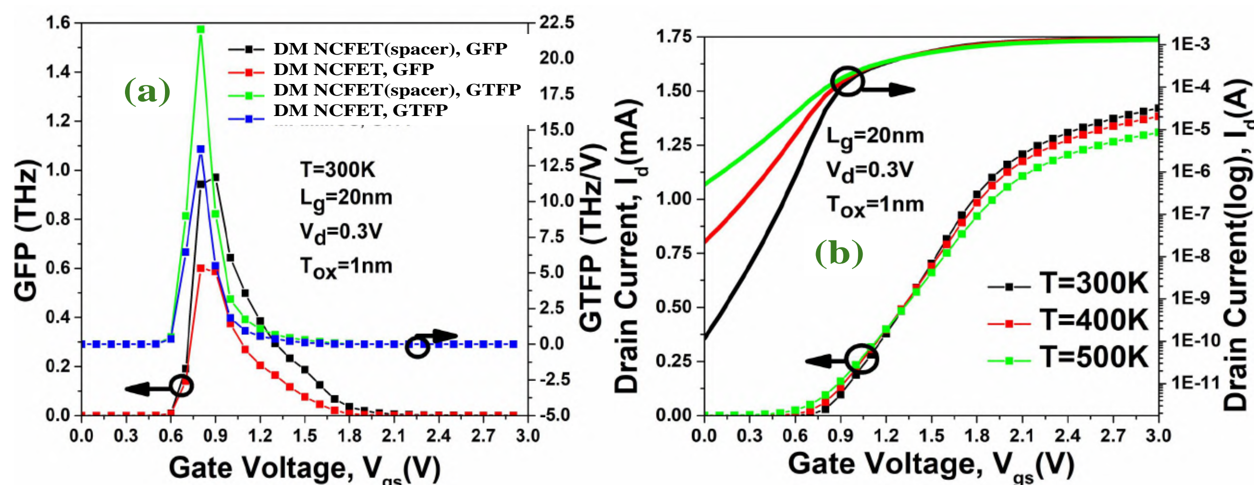

Figure 2.7: Graph for different structures at V_d=0.3 showing (a) Variation of gain frequency product and gain transconductance frequency gain product vs gate voltage at T=300K, (b) Variation of drain current in linear and log scale vs gate voltage for different temperature of DM-NCFET (spacer) at V_d=0.3 (PMC22b).

GTFP, as calculated by Eq. 2.9, acquired higher value for DM-NCFET (spacer) structure because of rise in g_m and TGF with fall in g_d at practically comparable F_t. In this manner, DM-NCFET (spacer) is the best appropriate design as far as speed, efficiency, and gain are considered for various high performance analog and RF applications.

2.4.4 Effect of Variation of Temperature on the performance of DM-NCFET

In this section, we observed the variation of temperature on DM-NCFET (spacer) such as T=300K, 400K and 500K with drain voltage of 0.3V, gate length of 20nm and oxide thickness of 1nm. Figure 2.7(b) exhibits the variation of drain current vs gate voltage for DM-NCFET (spacer) at V_d=0.3 in linear and log scale. The drain current of DM-NCFET (spacer) at temperature T=300K is higher in comparison to other temperatures with increase in gate voltage V_{gs} (V) that reflects the improved gate coupling capacitance at lower temperature. The left side of the graph shows less leakage current I_{off} at T=300K. At lower temperatures, phonon activity in the semiconductor material decreases. Phonons (lattice vibrations) are a major source of scattering for charge carriers, which impede their motion. With fewer phonons at lower temperatures, charge carriers can travel more freely through the channel, resulting in higher mobility. This increased mobility directly contributes

to a higher drain current at T=300K.

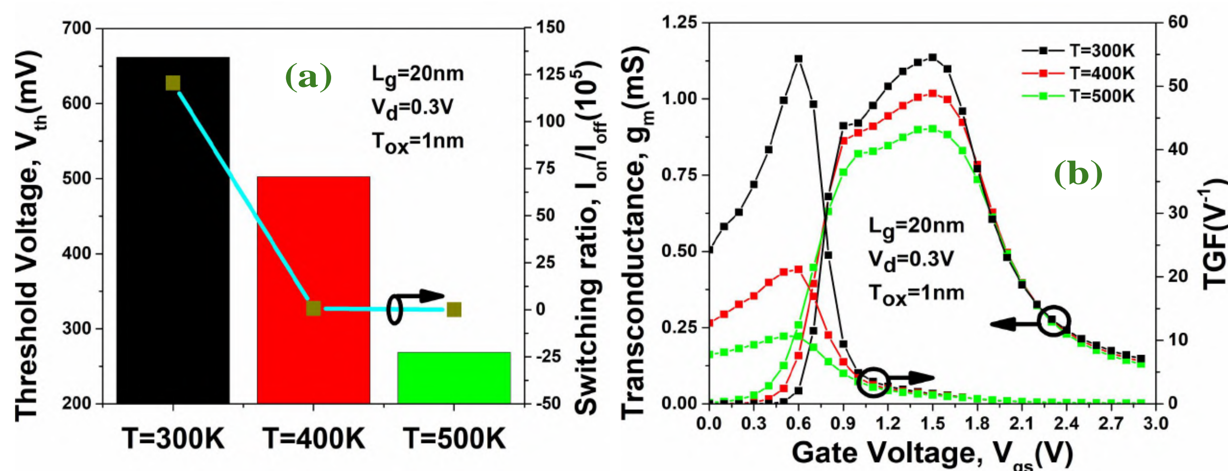

Figure 2.8: The graph showing variation of (a) threshold voltage and switching ratio vs gate voltage (b) transconductance and transconductance generation factor vs gate voltage for DM-NCFET (spacer) at different temperature, T=300K, 400K and 500K at V_d=0.3 (PMC22b).

Table 2.3: Comparison of different performance parameters for DM-NCFET (spacer) at various temperature with T_{ox}=1nm, and L_g=20nm.

Parameter	T=300K	T=400K	T=500K
I_{on} (A)	0.001421	0.001383	0.001309
I_{off} (A)(10^{-10})	1.18	220	5040
$I_{on}/I_{off}(10^{-6})$	12.0424	00.0629	0.002597
$V_{th}(mV)$	661.929	502.534	268.78

Figure 2.8(a) shows that the threshold voltage (V_{th} (V)) of DM-NCFET (spacer) at temperature of 300K is enhanced than other temperature T=400K and T=500K configurations at V_d =0.3V. At lower temperature, the intrinsic carrier concentration in the semiconductor decreases due to reduced thermal excitation. This shift requires a higher gate voltage to create enough charge carriers in the channel to turn the device on, which leads to an increase in the threshold voltage.

The switching ratio (I_{on}/I_{off}) of DM-NCFET (spacer) at T=300K is higher than the other temperatures such as T=400K and T=500K at T_{ox}=1nm, and V_d=0.3V, ensuring high switching speed for DM-NCFET (spacer) structure as also summarized in Table 2.3. Lower temperature reduce thermally generated carriers, leading to even lower off-state current. Meanwhile, the on-state current remains high due to the improved mobility and gate control at lower temperatures,

resulting in a higher switching ratio.

Figure 2.8(b) shows the variation of transconductance with gate voltage for both the structures. It is a parameter that is showing shift in drain current to shift in gate voltage at drain voltage of 0.3V. The transconductance curve of DM-NCFET (spacer) at T=300K is higher than the other temperatures. Thus, g_m has been analysed with the help of transfer characteristics of the the device that reflects enhanced carrier mobility and reduced thermal noise (NG18). Carrier mobility improves at lower temperatures because phonon scattering (caused by lattice vibrations) is reduced. At higher temperatures, phonon scattering increases, slowing down carrier movement. Transconductance generation factor is gain generated per unit power loss (PMMC23; MPC22; VC23). TGF of DM-NCFET (spacer) at T=300K is increased as compared to T=400K and T=500K configurations, close to ideally $50V^{-1}$ as shown in Figure 2.8(b). With less scattering and thermal noise at lower temperatures, the conductance of the channel improves, which increases the current response for a given change in gate voltage. This leads to higher TGF and improved device efficiency.

2.4.5 Effect of Variation of Work Function on the performance of DM-NCFET

In this section, we have varied the work function of gate electrode to improve the device performance for DM-NCFET(spacer). The varying work function (ϕ) for different materials considered for gate electrode are given as, for palladium (ϕ=5.3eV), tungsten (ϕ=4.55eV), and chromium (ϕ=4.3eV).

In this section, an extensive analysis for the electric field distribution over channel is done. Figure 2.9 shows the contour plot of electric field for (a) palladium (Pd) (b) tungsten (W) (c) chromium (Cr) and (d) the variation of electric field vs position along channel for various gate electrodes of DM-NCFET(spacer) at V_d=0.4V, V_{gs}=0.4V, and T=300k. The electric field distribution across the channel exhibits almost homogeneous distribution, when device is in linear region. When the device is in saturation region, the electric field took M-shape. The electric field (E) at drain side is higher for palladium than at source side as depicted in Figure 2.9(d), which reflects the better control at channel in linear region. The curve of E near drain is better than the channel which makes the potential difference higher, thus increases the electric field (E) as shown in Figure 2.9(d). The stronger electric field near the drain side due to higher work function of palladium helps in accelerating the charge carriers more efficiently, contributing to a higher drain current for

palladium. Thus, electric field effectively drives carriers through the channel while reducing the effect of unwanted carrier's scattering, ultimately enhancing the current flow in the device.

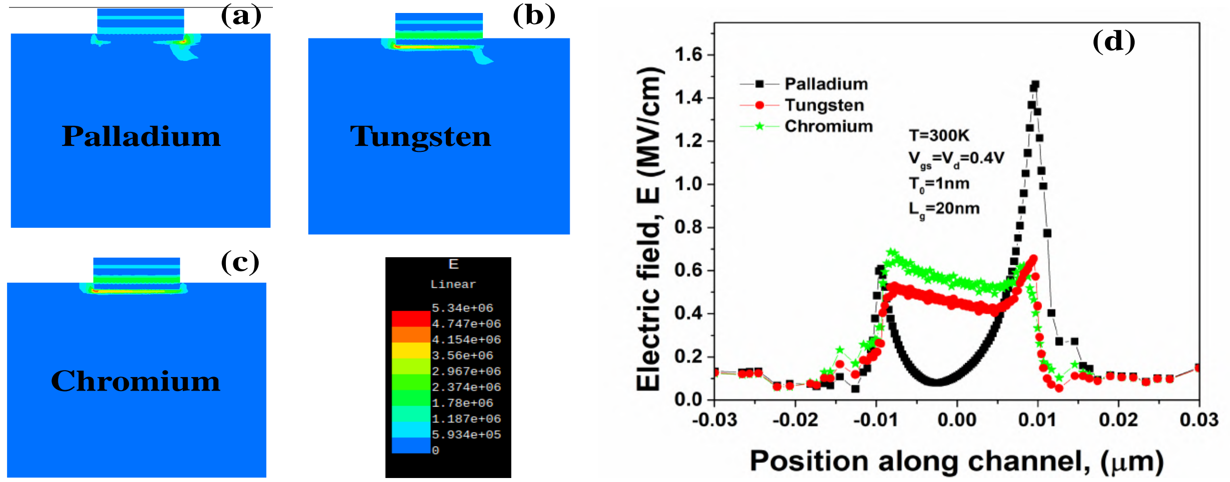

Figure 2.9: The contour plot of electric field for (a) palladium (b) tungsten (c) chromium (d) Variation of electric field vs position along the channel for various gate electrode of DM-NCFET(spacer) at V_d=0.4V, V_{gs}=0.4V, and T=300k (PMC22b).

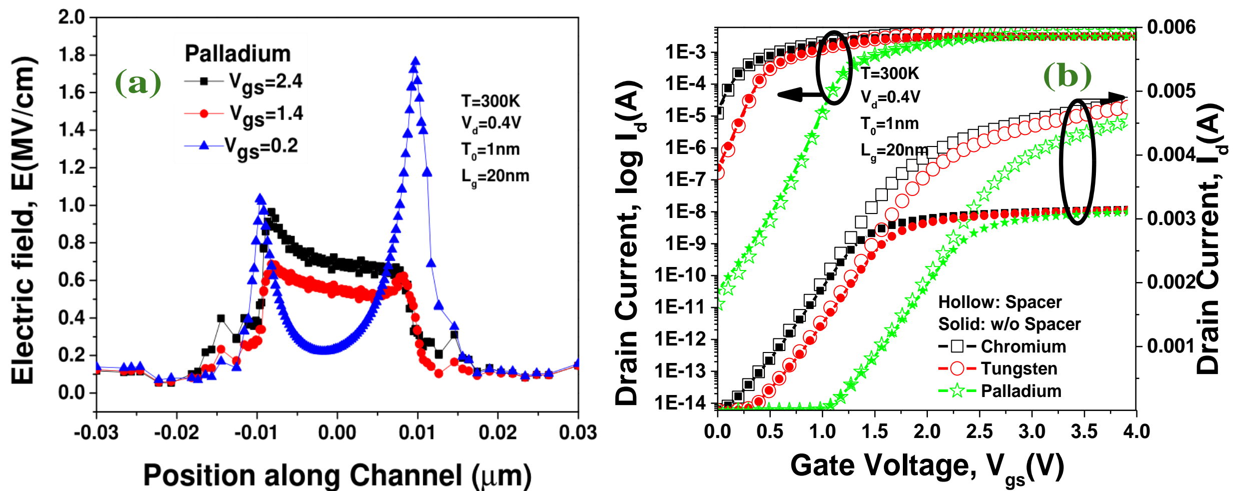

Figure 2.10: (a) The impact on electric field vs position along channel for palladium gate electrode at different gate voltage (b) Variation of drain current vs gate voltage of DM-NCFET(spacer) for various gate electrode at V_d=0.4V and T=300k (PMC22b).

Figure 2.10(a) shows the variation of electric field along the channel with variation in gate voltage when palladium gate electrode is considered in DM-NCFET (spacer). By controlling the electric field more effectively, the spacer also minimizes short-channel effects as discussed in previous section, which ultimately results in improved device performance at low gate voltage. Figure 2.10(b) reflects

the variation of drain current vs gate voltage at V_d=0.4 V for various work function of DM-NCFET (spacer) and DM-NCFET structures. The drain current for DM-NCFET (spacer) with palladium is higher than the others such as chromium and tungsten. Also DM-NCFET (spacer) shows decreased leakage current than DM-NCFET for all the considered work functions, that reveals enhanced gate effect to control the channel for the spacer configuration. The higher work function of Pd as gate electrode leads to better electrostatic control over the channel, increasing the carrier concentration and enhancing the current flow between the source and drain. As a result, the drain current is higher for Palladium based devices than for devices with chromium and tungsten as gate electrodes.

Table 2.4: Performance comparison of DM-NCFET (spacer) and DM-NCFET for different gate electrode materials such as palladium, chromium, and tungsten.

Parameter	DM-NCFET (spacer) Chromium (Cr)	DM-NCFET (spacer) Tungsten (W)	DM-NCFET (spacer) Palladium (Pd)	DM-NCFET Chromium (Cr)	DM-NCFET Tungsten (W)	DM-NCFET Palladium (Pd)
I_{off}(nA)	12200	169.0	0.013	14800	240.0	0.0338
$I_{on}/I_{off}(10^6)$	0.000394	0.0281	348	0.000212	0.013	91.8
$V_{th}(V)$	-0.28	0.201	0.9504	-0.324	0.188	0.938
TGF (V^{-1})	42.89	49.5	50.6	39.9	46.2	47.3

Transconductance Generation factor of DM-NCFET (spacer) for palladium is enhanced as compared to other work functions (ϕ), which reflects improved device efficiency that is close to ideally $50V^{-1}$. The higher value of TGF and switching ratio along with other improved parameters for palladium are summarized in Table 2.4. The variation of potential along channel is shown in Figure 2.11(a) for various gate materials considered for DM-NCFET at V_{gs}=V_d=0.4V. The potential of palladium is lower at the channel side than that for the other gate electrodes . The difference in work function between the gate electrode and the semiconductor channel creates stronger band bending in the semiconductor. This bending reduces the potential in the channel, lowering it for palladium as compared to gates with chromium and tungsten material. The increased band bending helps to form a conductive channel more easily, thus enhancing the device's switching characteristics and reducing the overall channel potential for palladium gate electrode (SC22). Also, When device is in biased or active condition, the max. potential and max. electric field of DM-NCFET (spacer) with

palladium is higher at drain side in comparison to other gate electrodes as shown in Figure 2.11(b). The potential is higher at drain side, which reveals better flow of current and smooth amplification of signal in ON state (conducting). The stronger electrostatic coupling between the Pd gate electrode and the channel, due to its higher work function, leads to more significant electric potential at the drain side (SC22). This enhanced potential allows for better control of the channel's conduction properties, particularly in short channel devices, thus improving overall device efficiency.

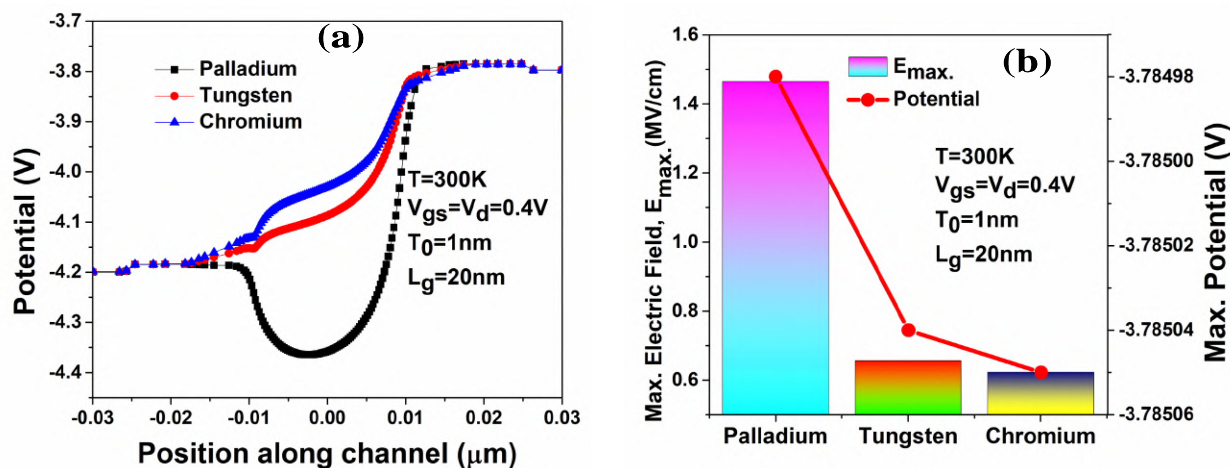

Figure 2.11: Variation of (a) potential vs position along channel (b) maximum electric field and maximum potential of DM-NCFET(spacer) with various gate electrode materials at V_d=0.4V and T=300K (PMC22b).

For digital circuit, the operation of transistor takes place in linear region, while for analog circuit, the operation of transistor is in saturation region (V_d=V_{gs}=0.4V) (Raz05; SGM10). The electric field distribution is studied by tuning V_{gs} for different operating situations. The breakdown time of channel is lower at higher electric field. The time dependent breakdown (t_b) equation is given below by Eq. 2.10:

$$t_{\mathrm{b}} = Aexp(-\gamma E_{\mathrm{o}})\frac{E_{\mathrm{a}}}{K_{\mathrm{b}}T} \tag{2.10}$$

where A is electric field acceration, γ is proportionality constant, T is absolute temperature, E_a is thermal activation energy, E_o is oxide electric field, and K_b is Boltzmann constant (Raz05; SGM10).

Figure 2.12(a) shows the effect on quasi fermi potential vs position along channel for DM-NCFET(spacer) with different gate electrode materials at V_{gs}=V_d=0.4V and T=300K. The quasi

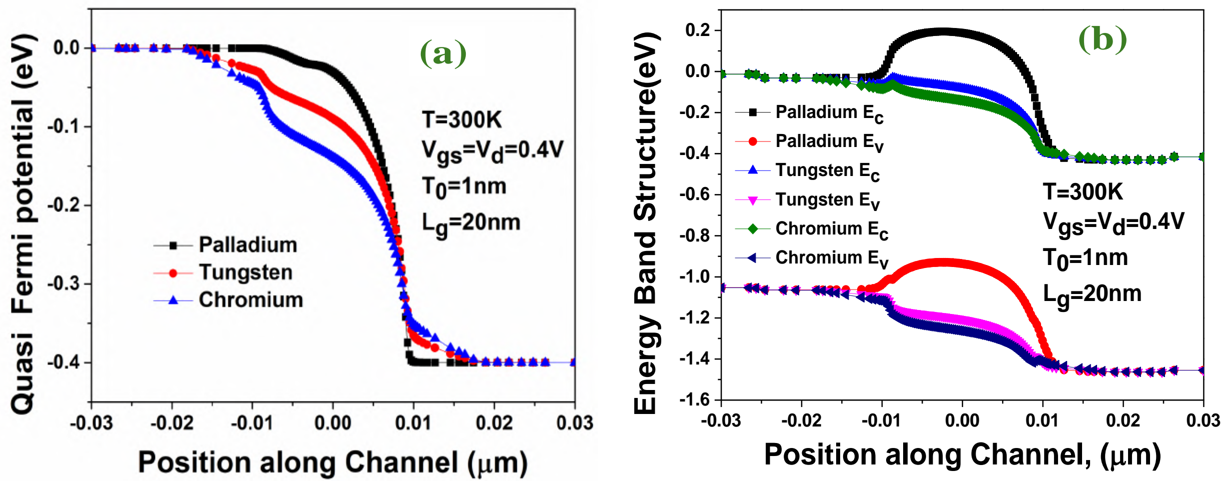

Figure 2.12: (a) The effect on quasi fermi potential vs position along channel and (b) The impact on energy band structure (conduction band (E_c) and valence band (E_v)) vs position along channel for DM-NCFET(spacer) with palladium, tungsten, and chromium as gate elctrode materials at V_d=0.4V and T=300K (PMC22b).

fermi potential of palladium is higher than others electrode, when FET is in equilibrium and biased condition. The quasi fermi potential for holes and electrons may shift from equilibrium position on applying the external bias (PMM85; CDS15). A higher quasi-Fermi potential means more available carriers for conduction. With Pd as the gate electrode, the higher work function raises the quasi-Fermi potential, leading to increased carrier density and improved device performance (CJZ16). Figure 2.12(b) exhibits the variation in energy band structure vs position along channel for DM-NCFET(spacer) at V_{gs}=V_d=0.4V and T=300K with various gate electrode materials. The band gap of palladium is 1.1eV, which is lower than that for chromium (1.12eV). The higher work function of Pd also results in more significant band bending near the semiconductor interface, which effectively lowering the barrier for the electron flow (DGA+17). This reduces the effective band gap of the device, allowing for easier charge carrier injection, thus ultimately leading to improved device characteristics.

2.5 Summary

In this work, we proposed a ferroelectric layer-enhanced FET device, specifically the DM-NCFET with spacer and without a spacer. All simulations were conducted using a Visual TCAD simulator. The DM-NCFET (spacer) configuration demonstrated significantly improved analog results as compared to DM-NCFET without a spacer. Specifically, the switching ratio is increased by approximately 2 times, the subthreshold swing was reduced by 1.06 times, and DIBL decreased by 1.21 times, indicating reduced short channel effects and lower leakage current for DM-NCFET (spacer) in comparison to DM-NCFET. The DM-NCFET (spacer) structure also show enhancement in other analog parameters such as g_m, TGF, A_v, and V_{ea}. Furthermore, RF parameters showed significant improvements with the DM-NCFET (spacer) configuration, including reduced F_t, improved C_{gg}, GFP, and GTFP. Further, the analysis done on DM-NCFET (spacer) at various temperatures revealed improved performance at T=300K as compared to T=400K and T=500K. The device showed more favorable results with enhancements in switching ratio and transconductance while reduction in leakage current at T=300K. Thus, this study suggests that DM-NCFET (spacer) at T=300K is an improved device structure for analog performance compared to its conventional counterpart, making it suitable for high-speed IC applications.

Additionally, a comparative study of DM-NCFET (spacer) and DM-NCFET with different gate electrode materials showed that palladium, with a work function of 5.3eV, provided better results than chromium and tungsten. Palladium demonstrated 10^{-6} times lower leakage current compared to chromium along with higher switching ratio and reduced subthreshold swing. The increasing work function (ϕ) correlated with improved device performance. The electric field across the channel was also studied for various work functions, and palladium exhibited enhanced electric field as compared to other gate electrodes. Thus, DM-NCFET (spacer) design has shown significant improvements in terms of various measured parameters, showing greater efficiency in terms of energy and speed. Consequently, the findings of this research can assist engineers in designing nanoelectronic devices to further meet the requirements for high performance Analog/RF applications.

After thoroughly examining the analog and RF properties of the DM-NCFET along with studying the effects of variation of temperature and work function of the gate electrode to ensure improved

performance and reliability, the proposed device has the potential to be explored for further enhancement in DM-NCFET's performance with a special focus on the detection of biomolecules using the DM-NCFET for improved sensitivity in multiple areas of applications such as disease monitoring, food analysis, forensic investigations,and environmental monitoring. This will be the main area of emphasis in the next chapter.

Chapter 3

Detection of Biomolecules in Dielectric Modulated Double Metal NCFET with Improved Sensitivity

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* This chapter investigates the Double metal below ferroelectric layer FET that is DM-NCFET for biosensing application with the help of extensive analysis for different biomolecules at varying cavity length.

* It is observed that switching ratio of the device with protein biomolecules is higher than the device without biomolecules by 1.52 times, sensitivity of protein is enhanced by 1.11 times over device without biomolecule.

* In addition, decrement in the cavity length from 12nm to 8nm altogether upgraded the sensitivity of the proposed biosensor along with other performance metrics.

* Consquently, Double Metal NCFET is empowering its utilization for biosensor applications to analyze different infections with enhanced speed and sensitivity along with low power consumption, making them a reliable biosensor.

3.1 Introduction

The recent COVID-19 pandemic has highlighted the crucial importance of microelectronic biosensors in detecting biomolecules and biological warfare agents. These electronic biosensors can be deployed for continuous monitoring of airborne biomolecules in environments such as airplanes, metro systems, hospitals, schools, and clinics. This has created an urgent need to design and develop fast and accurate biosensors. These sensors detect biochemical compounds like antibodies, enzymes, nucleic acids, and proteins through chemical reactions, making them invaluable in various applications, including disease monitoring, food analysis, forensic investigations, environmental monitoring, and the study of biomolecular interactions (AC+20; KRG+20; PMC22c).

Numerous methods have been developed for biomolecule detection, including the chemical-linked immunosorbent assay (WJT+13), which is used for conditions such as Alzheimer's disease, coronary artery disease, and ovarian cancer. However, many of these methods are complex and time consuming due to the need for sophisticated modeling techniques (LSC+15). In recent years, field-effect transistor (FET) based biosensors have gained significant attention due to their high scalability, extreme sensitivity, rapid electrical detection, low power consumption, linear electrical response, and cost-effective mass production, making them superior to other methods like surface plasmon resonance, microcantilevers (Ber86), and various fluorescence devices (IHGC07). Low-cost, highly sensitive, reliable, user-friendly, and rapid diagnostic biosensing devices are essential for a wide range of biological and biomedical applications (VES+09). Sensitivity is a critical parameter for MOSFET-based biosensors (KRG+20).

Ferroelectric FETs (Fe-FETs) have garnered considerable attention due to their potential in both memory and switching applications (MBP+08). The size and power consumption are key factors in the field of modern electronic devices, with ongoing research aimed at developing aggressively scaled devices that consume ultra-low power (LKSH16). However, NCFETs did not account for the effects of channel length scaling, and they employed the Landau model only for the out-of-plane polarization component, which is unsuitable for thick ferroelectric layers (AKYU21). In many literatures, researchers has examined and analyzed the performance of NCFETs with extended channels using analytical modeling (PAC18). But, a thorough understanding of the behavior of

dual metal structures and comprehensive performance analysis remains scarce in the literature (PMC22c; PMC21a; PMC22a).

In this study, Double metal below ferroelectric layer FET (DM-NCFET) is explored for various biomolecules like protein, uricase, streptavidin, cholesterol oxidase (ChO_x), and its performance is compared and analysed to find the device suitability for various biomolecules in terms of various analog metrics such as sensitivity, lower leakage current, threshold voltage, etc. Further, DM-NCFET is also analysed for various cavity lengths to find the optimum length for giving the most improved performance, makes it suitable with high sensitivity and high speed biosensing for detecting various diseases.

3.2 Device Structure

Figures 3.1(a) depict the schematic diagram of a DM-NCFET and (b) magnified view of the cavity with biomolecules, respectively. Biomolecules are immobilized in the Bio1 and Bio2 regions. The regions between the source and gate (L_{bio1}) and between the drain and gate (L_{bio2}) correspond to the cavity gap, which is a crucial characteristic that determines the impact of biomolecules on DM-NCFET.

The channel length (L_c) is 20nm, the body length (L_b) is 60nm, and the drain/source length ($L_{d/s}$) is 10nm. The Bio1/Bio2 length ($L_{bio1/bio2}$) is 10nm, the body thickness (T_b) is 50nm, and the drain/source thickness ($T_{d/s}$) is 3nm. Additionally, the oxide thickness (T_o) is 1nm, the ferroelectric layer thickness (T_f) is 1nm, the thickness of Metal1 (T_{m1}) is 2nm, the insulator thickness (T_i) is 2.3nm, and the thickness of Metal2 (T_{m2}) is 1.7nm. The thickness of Bio1/Bio2 is 3nm, and the gate thickness is 2nm. The total gate thickness (T_{gt}) is the sum of the oxide, Metal2, insulator, Metal1, ferroelectric layer, and gate thickness.

The body is made of silicon (Si), while the drain, source, substrate, and gate are made of aluminum (Al). The insulator is composed of silicon nitride, the oxide is silicon dioxide (SiO_2), Metal1 is gold (Au), and the ferroelectric material is silicon doped hafnium dioxide (HfO_2FE). The doping concentration of the drain/source ($N_{d/s}$) is $1 \times 10^{20} cm^{-3}$ with a Gaussian profile and donor type. The work function for the Metal1 gate is set at a high value of 5.4eV.

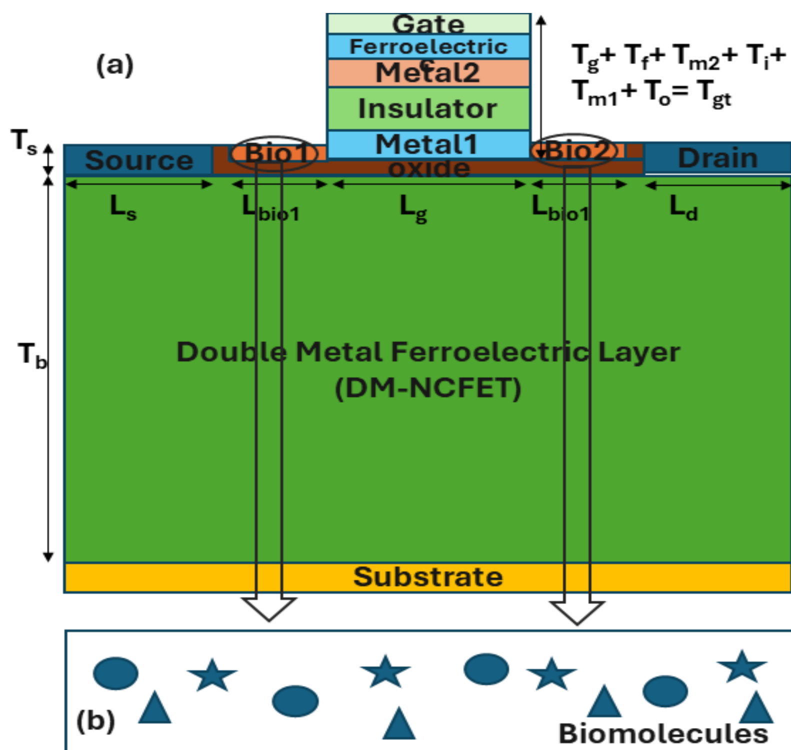

Figure 3.1: (a) The Schematic diagram of DM-NCFET for detection of biomolecule (b) Magnified view of cavity with biomolecules(PMC22c).

3.3 Simulation Methodology

The Visual TCAD system is used to simulate all the results. Biomolecules are introduced and identified within the confined Bio1 and Bio2 regions. In this study, neutral biomolecules such as streptavidin, protein, uricase, and ChO_x are simulated within the cavity gap. The drain voltage, V_d, is fixed at 0.4V throughout the process, and the gate voltage, V_{gs}, varies from 0V to 4V. The temperature is maintained at 300K during the entire device simulation. The design utilizes concentration-dependent mobility (CONMOB) model, field-dependent drift velocity (FLDMOB) model, the Shockley–Read–Hall (SRH) recombination model, and Landau Khalatnikov model for considering the polarization of the ferroelectric material.

The absorption of various biomolecules is modeled by introducing a non-conductive material with the same dielectric constant as the specific biomolecule into the cavity gap. The empty cavity (without biomolecules) is represented by an insulator with a dielectric constant of K=1, while the dielectric constants of the different studied biomolecules are as follows: protein (K=8) (KHCP12), uricase (K=1.5), ChO_x (K=3.5), and streptavidin (K=2.1) (BSMM02)(DMSB86). This method

has been adopted in concurrence with experimental results (IHGC07).

3.4 Result and Discussion

3.4.1 Impact of Various Biomolecules on DM-NCFET

Figure 3.2 illustrates the variation of drain current (both in linear and logarithmic scales) versus gate voltage for different biomolecules in double metal NCFET at $V_d = 0.4$ V, with a channel length of 20 nm and oxide thickness of 1 nm. The drain current for protein (K = 8) is higher than that for other biomolecules along with reduced leakage current as shown in left side of the graph. This is due to the increase in dielectric constant which results into improved gate coupling capacitance A higher dielectric constant (K) also results in greater capacitance for the biomolecule-modulated region of the device. This increased capacitance enhances the ability of the gate to control the channel, leading to a stronger electric field and improved charge carrier accumulation in the channel.

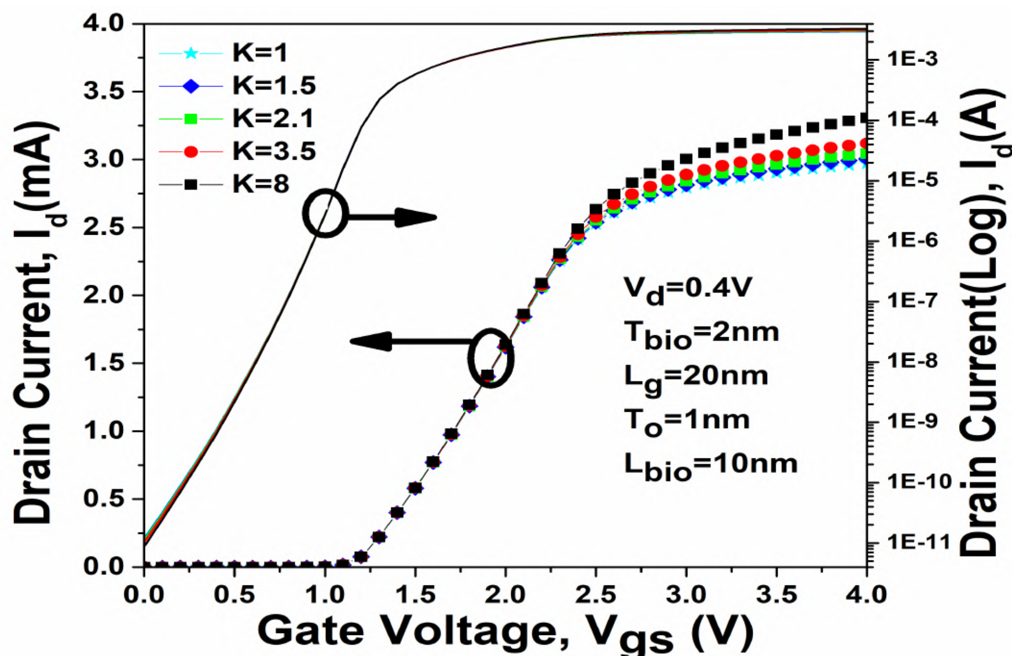

Figure 3.2: Transfer characteristic of different biomolecules for DM-NCFET at drain voltage $=0.4V$. (PMC22c).

Figure 3.3(a) shows that transconductance, which is the ratio of the change in drain current to the change in gate voltage at a drain voltage of 0.4 V, is higher for protein as compared to streptavidin, uricase, ChO_x, and the case without molecules. A higher dielectric constant increases the gate capacitance, which enhances the control of the gate over the channel. The increased

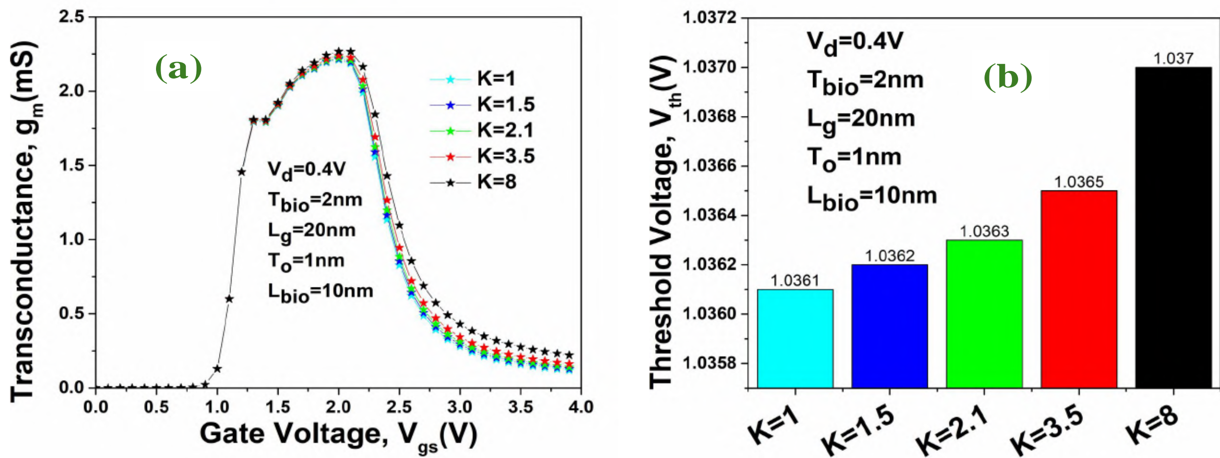

Figure 3.3: Variation of (a) Transconductance, (g_m) (b) Threshold voltage (V_{th}) versus gate voltage of different biomolecules for DM-NCFET at $V_d = 0.4V$. (PMC22c).

average carrier velocity and improved electron mobility with higher dielectric constant for protein, results in a stronger current response for a given gate voltage, and enhanced g$_m$(NG18).

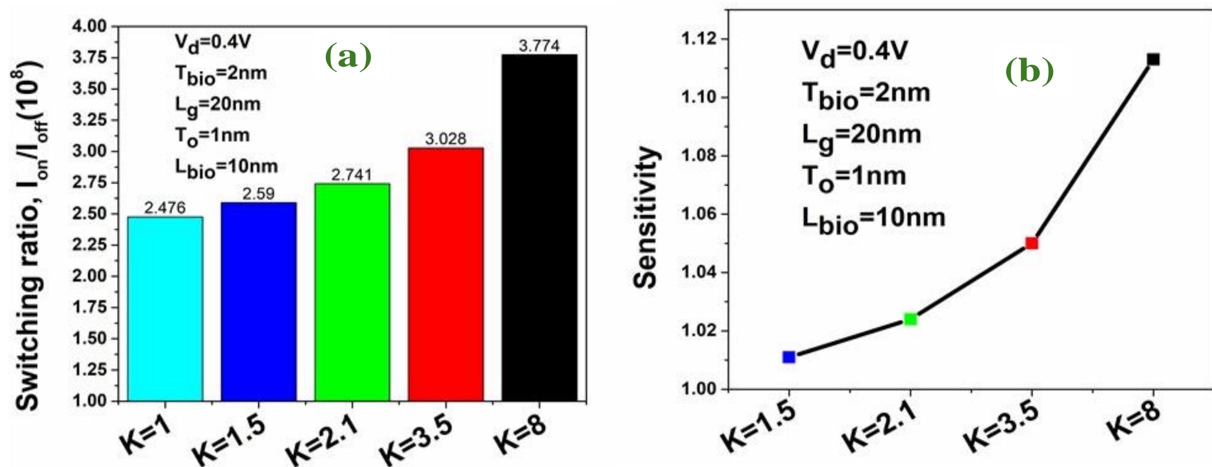

Figure 3.4: (a) Switching ratio (I_{on}/I_{off}) (b) Sensitivity of DM-NCFET for different biomolecules at drain voltage =0.4V. (PMC22c).

Figure 3.3(b) demonstrates that the threshold voltage for protein is higher than that for the other biomolecules at V_d = 0.4 V. Protein molecules provide better shielding of the drain-side potential, enhancing the threshold voltage characteristics. The threshold voltage is directly related to the dielectric constant and is applied as a sensing parameter for biomolecule recognition. a higher dielectric constant in a DM-NCFET improves the electrostatic control of the gate over the

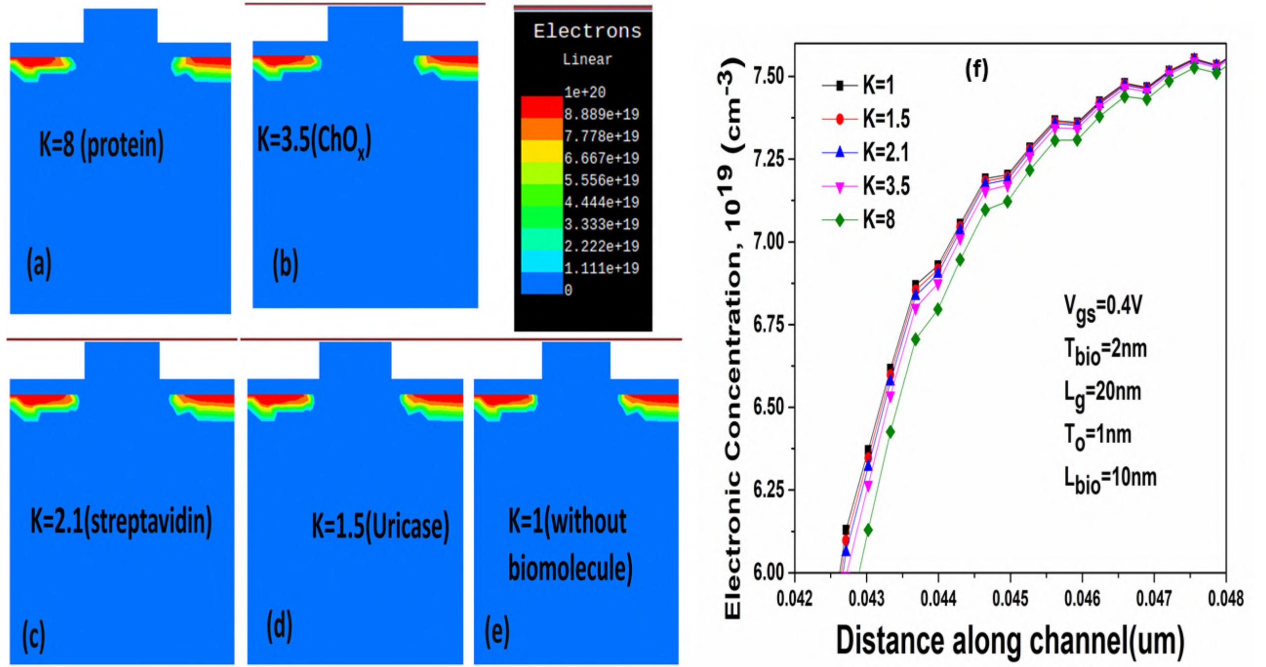

Figure 3.5: Contour plot for Electronic concentration of DM-NCFET for different biomolecules with dielectric constant (a) K=8 (b) K=3.5 (c) K=2.1 (d) K=1.5 (e) K=1 and (f) Variation of electronic concentration vs distance along channel for various biomolecules (PMC22c).

channel, leading to enhanced device performance with increased threshold voltage.

Figure 3.4(a) depicts the switching ratio for protein, which is higher than that for the other biomolecules at $L_g = 20$ nm, $T_o = 1$ nm, $L_{bio} = 10$ nm, and $V_d = 0.4$ V. The reduced leakage current for protein as shown in Figure 3.2, results in higher switching ratio, as also shown in Table 3.1. A rise in dielectric constant increases the gate capacitance, allowing for faster switching between on and off states. This leads to reduced switching time, thus increasing the switching speed of the NCFET which is critical for high-speed applications. Figure 3.4(b) illustrates the sensitivity of various biomolecules, including protein, streptavidin, uricase, ChO$_x$, and the case without biomolecules, at a drain voltage of 0.4 V. If the cavity gap is fully filled with the biomolecules, then the sensitivity is calculated using the formula provided in Eq. (3.1). The increased dielectric constant allows for more precise detection of variations in the channel, and results in higher sensitivity as showcased by the protein biomolecule.

$$S = \frac{I_{on}\,(K > 1)}{I_{on}\,(K = 1)} \tag{3.1}$$

Figure 3.5(a)-(e) presents contour plots of the electronic concentration along the channel from source to drain for different biomolecules with dielectric constant: (a) K = 8, (b) K = 3.5, (c) K = 2.1, (d) K = 1.5, and (e) K = 1. Figure 3.5(a) shows that when a biomolecule is introduced, additional charges are generated in the channel from source to drain beneath the cavity. Figure 3.5(f) reflects variation of the electronic concentration across the channel at L_{bio} =10nm. The quantity of these charges depends on the specific biomolecule. With a higher dielectric constant, the electric field required to accumulate electrons in the channel is distributed more effectively. This can lead to reduced electron concentration in the off state, minimizing leakage current and improving the power efficiency of the device.

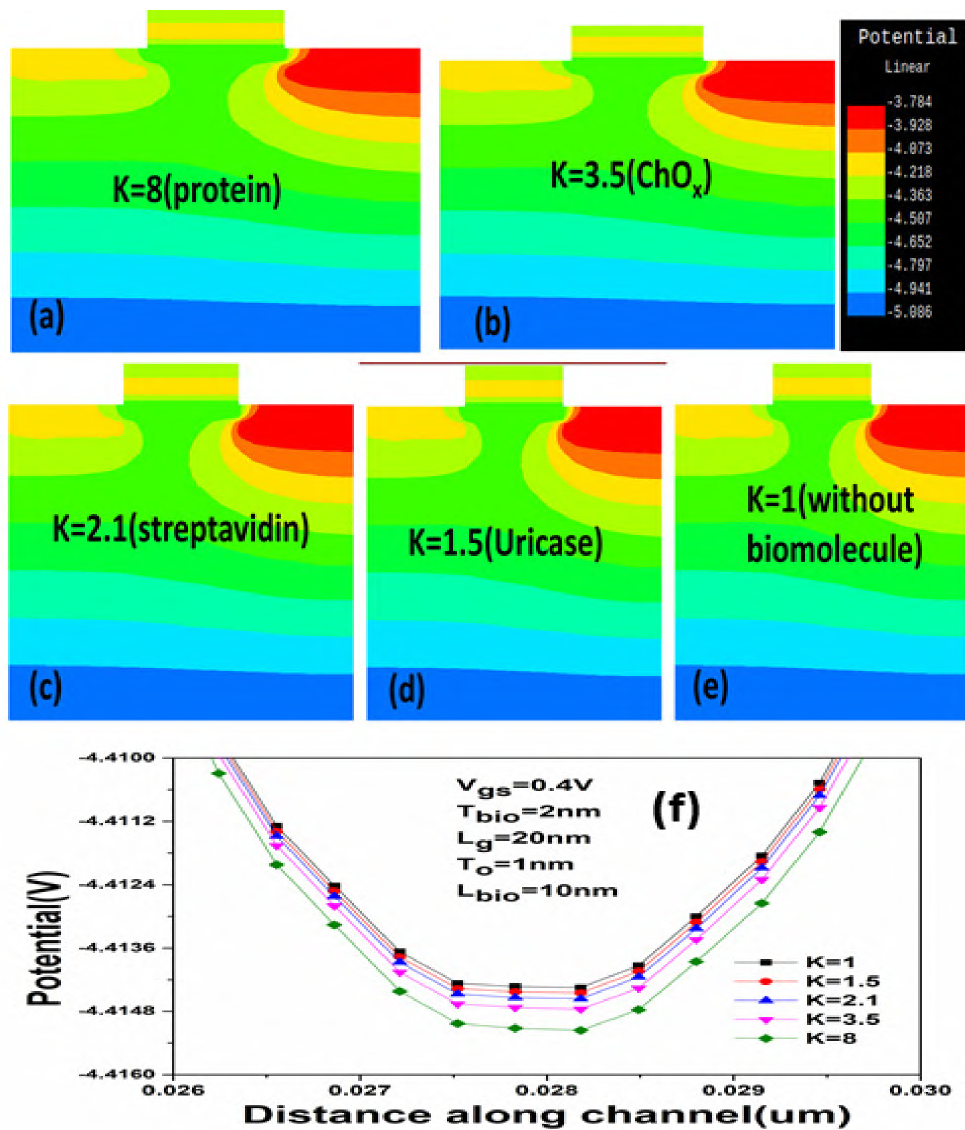

Figure 3.6: Contour plot for Potential of DM-NCFET for different biomolecules with dielectric constant (a) K=8 (b) K=3.5 (c) K=2.1 (d) K=1.5 (e) K=1. (f) Variation of potential vs distance along channel at drain voltage = 0.4V for different biomolecules (PMC22c).

Figure 3.6(a)-(e) presents contour plots of the potential along the channel from source to drain for different biomolecules with dielectric constant: (a) K = 8, (b) K = 3.5, (c) K = 2.1, (d) K = 1.5, and (e) K = 1. It also reflects the electrical performance of the DM-NCFET. Changes in potential across the channel occur on the drain side beneath the cavity region as shown in Figure 3.6(f). When the cavity gap is occupied by biomolecules, a potential deformation is observed due to the shift in dielectric constant caused by the biomolecules(NKJ^{+}20). This change in potential can be used to detect the presence of biomolecules in the cavity gap area. With a higher dielectric constant, the electric field is more effectively modulated, reducing the potential barrier for charge carriers. This leads to higher carrier mobility and consequently, a larger drain current in the device.

Table 3.1: Comparison of different performance parameters for various biomolecules in DM-NCFET at $T_{ox} = 1nm$ and cavity length of $10nm$

Parameter	$K = 8$	$K = 3.5$	$K = 2.1$	$K = 1.5$	$K = 1$
I_{on} (mA)	3.58	3.34	3.21	3.14	3.07
I_{off} (pA)	4.76	8.14	9.77	10.6	11.3
I_{on}/I_{off} (10^8)	7.52	4.1	3.28	2.96	2.71
V_{th} (V)	0.802	0.794	0.792	0.791	0.79
g_m (mS)	2.34	2.3	2.27	2.25	2.23
g_d (nS)	0.473	0.596	0.638	0.656	0.674

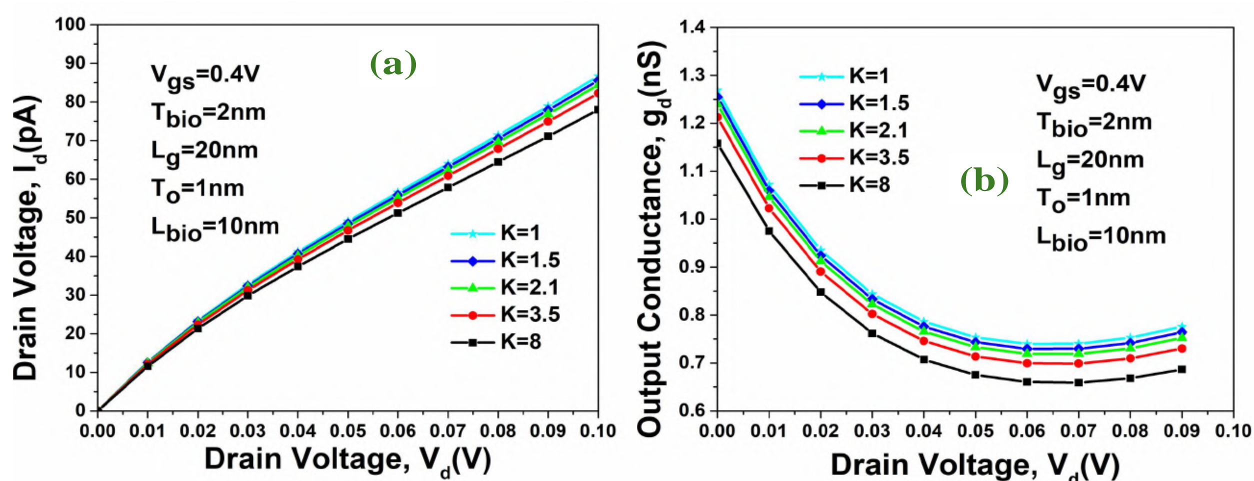

Figure 3.7: Variation of (a) drain current vs drain voltage (b) output conductance vs drain voltage of DM-NCFET at gate voltage = 0.4V for different biomolecules (PMC22c).

Figure 3.7(a) presents the plot of drain current versus drain voltage at a gate voltage of 0.4 V, oxide thickness of 1 nm, cavity gap of 10 nm, and channel length of 20 nm. The output conductance

which reflects the driving capability of the device, characterizes the region of device operation, as depicted in Figure 3.7(b). Initially, a high output conductance in the linear region is observed as the drain voltage increases beyond the pinch-off voltage due to drain-induced barrier lowering and channel length modulation (AS15). The g_d for protein is lower as compared to other biomolecules as shown in Figure 3.7(b), indicating enhanced gate controllability and suppressed short-channel effects. A higher dielectric constant increases the gate capacitance, which enhances the gate-channel coupling between the gate and the channel, thus reduces the variation of drain current with drain voltage. This is very well reflected in decreasing value of output conductance for protein.

3.4.2 Effect of Length Modulation in Cavity Gap

Figure 3.8(a) displays the variation of drain current versus gate voltage for various cavity length (L_{bio} = 8 nm, 10 nm, and 12 nm) with different biomolecules, including ChO_x, protein, streptavidin, and uricase. The drain current for protein at a cavity length of L_{bio} = 8nm is enhanced compared to the other lengths. A lower cavity length contributes to higher drain current by reducing the distance between the gate and the channel, which strengthens the gate's influence on the channel and enhances current conduction.

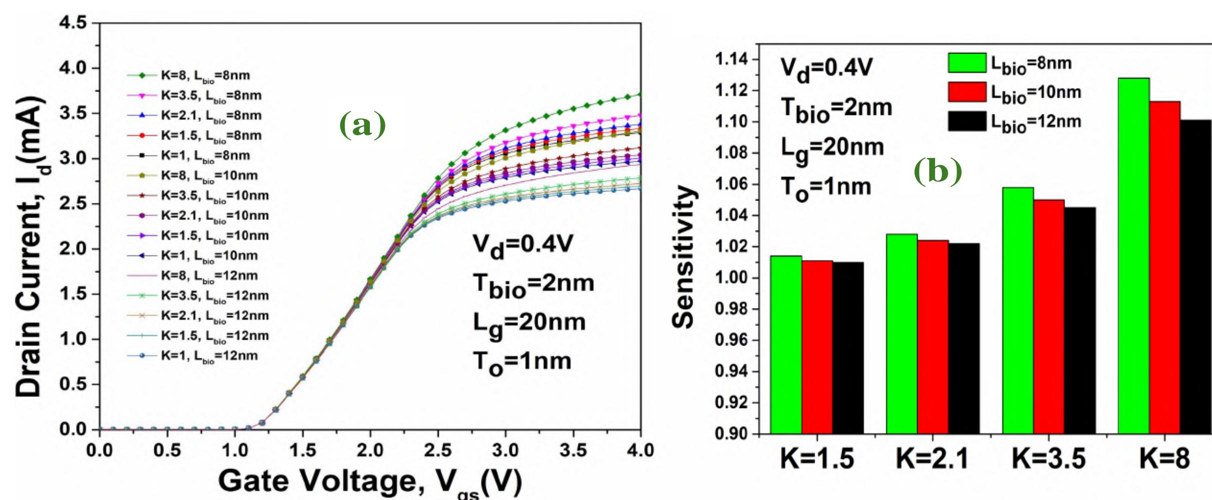

Figure 3.8: Variation of (a) drain current vs gate voltage (b) Sensitivity of DM-NCFET for various biomolecules with different cavity length, L_{bio} = 8nm, 10nm, and 12nm at drain voltage = 0.4V (PMC22c).

The sensitivity of the DM-NCFET biosensor with varying cavity gap length is also evaluated,

revealing a significant improvement as the cavity length, L_{bio} decreases for all the biomolecules as shown in Figure 3.8(b). Specifically, the sensitivity improves for a biomolecule with higher dielectric constant for the given L_{bio}. At a cavity length of L_{bio} = 8 nm, the nanogap-inserted on DM-NCFET biosensor demonstrated enhanced sensitivity for proteins (K = 8) as compared to other biomolecules. In sensing applications, the higher dielectric constant improves the device's sensitivity by increasing the responsiveness of the channel to changes in the gate voltage. Further, a lower cavity length enhances the device's sensitivity by improving the electrostatic control of the channel, making the device more responsive to small variations in external conditions and allows for more precise detection of external stimuli.

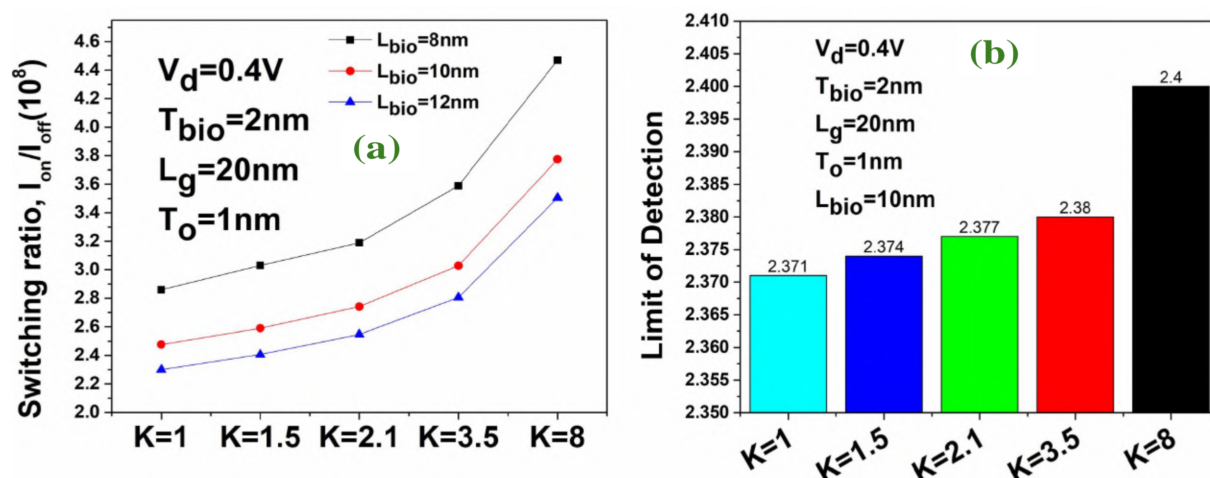

Figure 3.9: Variation of (a) switching ratio of DM-NCFET (b) limit of detection (LOD) for various biomolecules with different cavity length, L_{bio} = 8nm, 10nm, and 12nm at drain voltage = 0.4V (PMC22c).

Figure 3.9(a) shows the variation of switching ratio for different biomolecules with various cavity length, indicating that protein exhibits the highest improvement with shorter cavity length as compared to other biomolecules. The higher dielectric constant enhances the device's ability to switch between the on and off states, which results in a higher switching ratio. Also, a shorter cavity length reduces the impact of drain voltage on the channel and its related modulation, thus contributing to a clearer distinction between the on and off states and improving the switching ratio.

Figure 3.9(b) shows the variation of limit of detection (LOD) against different K values associated with different biomolecules. The standard deviation considered for LOD is 0.000737 for K=1,

0.000739 for K=1.5, 0.000741 for K=2.1, 0.000749 for K=3.5, and 0.000765 for K=8. The LOD for protein is lower than that for the other biomolecules, indicating the ability to detect lower concentrations of analytes, though not necessarily quantifying them (MB19). A lesser limit of detection for COVID-19 suggests that it may miss more infected cases. The combination of a higher dielectric constant and a lower cavity length allows for finer detection of small variations. The device can more accurately detect changes in the environment or analyte concentration, resulting in a higher limit of detection as shown by protein in this study.

3.5 Summary

This study has explored the biosensing capabilities of the DM-NCFET device. The electrical performance are assessed under different conditions for the detection of various biomolecules. The threshold voltage shift for proteins is improved by 0.28% as compared to the DM-NCFET without biomolecules. Sensitivity for protein detection with K=8 is increased by 1.167 times over K=1, and the switching ratio for proteins is 177% higher than that for without biomolecules. At a cavity length of 10 nm, the surface potential showed 13% improvement for proteins as compared to that for without biomolecules. The DM-NCFET device exhibited notable improvements with better sensitivity for biomolecules having higher K values. The proposed device showed enhanced sensitivity for protein detection (K=8) as compared to other biomolecules. Additionally, the impact of cavity length on V_{th}, sensitivity, and the I_{on}/I_{off} ratio of the DM-NCFET biosensor was analyzed. The results indicated that sensitivity increases with smaller cavity lengths along with other performance metrics. So optimizing the cavity length to 8 nm enhances overall performance, making it suitable for high-sensitivity and high-speed biosensors for detecting various diseases.

In conclusion, the study confirms that DM-NCFET devices are well-suited for biosensing applications, offering improved speed and sensitivity for infection analysis. Consequently, the proposed device has the potential to be explored for further enhancement in DM-NCFET's performance through DFT-based atomic modeling and optimization for improved analog/RF performance, which will be the main focus of the next chapter.

Chapter 4

DFT Based Atomic Modeling and Optimization of Double Metal Double Gate NCFET

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* This chapter discusses the investigated Analog/RF and linearity parameters of SM DGNCFET and DM DGNCFET to achieve the better performance.
* It is found that SM DGNCFET showed better performance with switching ratio being 279 times better, and DIBL being 54% lower as compared to DM DGNCFET.
* In addition, DFT analysis is done for the enhancement in the electronic and optical properties of Si-doping bulk structure by using the Quantum ATK.
* Consequently, the proposed device shows better electronic and optical properties along with improved analog/RF and linearity performance.

4.1 Introduction

Power dissipation (P) varies with the supply voltage, following the relationship as P proportional to V_{ds}^2, where V_{ds} is the drain-source voltage. This dissipation is typically controlled by the minimum subthreshold swing (SS = 60 mV/decade) of a Boltzmann switch, which is regulated by barriers (KJMA15). Recently, ferroelectric FETs (Fe-FETs) have gained significant attention for their reliability in memory and switching applications (LCL+15; PMC23; AC24). Key factors in advanced electronic devices include power consumption and space efficiency, with past and ongoing research focusing on developing aggressively scaled devices that utilize ultralow power (LFT+16). To overcome current limitations, there has been growing interest in alternative devices that operate through fundamentally different mechanisms to switch an electronic device from OFF to ON (PMC23).

Enhancements in ferroelectric layer devices with NCFETs include Single Metal Double Gate NCFET and Double Metal Double Gate NCFET configurations (PAC18; PAC19). NCFETs are field-effect transistors that exhibit a subthreshold swing below 60 mV/decade and a high ON-current. Recently, negative capacitance effects have been experimentally demonstrated in various systems, including 1) isolated ferroelectric films, 2) ferroelectric-dielectric bilayers, and 3) ferroelectric-gated transistors using superlattices (LKSH16). However it is found that SM DGNCFET does not account for channel length scaling (PAC19; SJSI16; YS18), and the Landau model is applied only in the out-of-plane polarization section of the device (AKYU21).

Moreover, FeFETs offer advantages such as non-destructive read capabilities, rapid operation, and application in memory devices, marking a new era of FET technology (KCJ21). The FE material exhibits negative capacitance behavior, as evidenced by its charge-energy curve (KPK+16). Incorporating a ferroelectric material in the gate stack of MOSFETs enhances device performance and reliability.

Density Functional Theory (DFT) is a quantum-mechanical, atomistic modeling approach for calculating the properties of atomic systems, including surfaces, crystals, molecules, and electronic devices when coupled with Non-Equilibrium Green's Functions (NEGF). DFT is crucial for validating the energy, structure, and properties of materials, nanosystems, and molecules. In HfO_2-based

gate stacks, atomic dopants can alter the work function (KPK+16). At 2800 degrees Celsius, HfO_2 exists in a cubic phase (ZRR13; KGA+17). Yttrium doping stabilizes the cubic phase at lower temperatures (KVS22). The cubic phase of HfO_2 is used in various industrial applications, including random access memory devices, fuel cells, sensors, and optical coatings. HfO_2 thin films have low lattice thermal conductivity, measured between 0.49 and 0.95 W/m-K (LXZ+17).

Achieving ferroelectricity in thin films has long been a research goal due to its potential applications in ferroelectric FET (FEFET) and ferroelectric random-access memory (FERAM) (DGMIB19; MWC01; HPR+10). Ferroelectric-based technology offers several advantages over current non-volatile memory technologies, including low power consumption, controllability over variability, and high switching speed (MH02). However, the lack of ferroelectric materials that meet all the practical requirements for memory technology—scalability, CMOS compatibility, and memory retention—has limited widespread application. HfO_2 remains one of the most widely used dielectric gate oxides in current field-effect transistor devices (GM16; CPN+16). The performance of the SM DGNCFET with long channels using analytical modeling has been evaluated in the literature (PAC18). While the SM DGNCFET shows a higher ON-state current than the DM DGNCFET, this is not consistent across all ferroelectric materials.

Thus performance of SM DGNCFET and DM DGNCFET for thin channel with silicon doped hafnium oxide ferroelectric material has been explored in this chapter for various possible variations of scaling in dimension such as ferroelectric layer, substrate, temperature (PMMC23). A brief DFT analysis is also done for the enhancement in the electronic and optical properties of Si-doping bulk structure that will further improve the device performance.

4.2 Device Design and Atomic Study

4.2.1 Device Structure

Figure 4.1 illustrates two device structures: (a) Double Metal Double Gate NCFET (DM DGNCFET) and (b) Single Metal Double Gate NCFET (SM DGNCFET). The dimensions of these two devices are nearly identical, except for the Metal2-Top and Metal2-Bottom ($T_{m2T/m2B}$) layers, which vary in the SM DGNCFET. In the DM DGNCFET, the thickness of $T_{m2T/m2B}$ is 5 nm and made up

of aluminium.

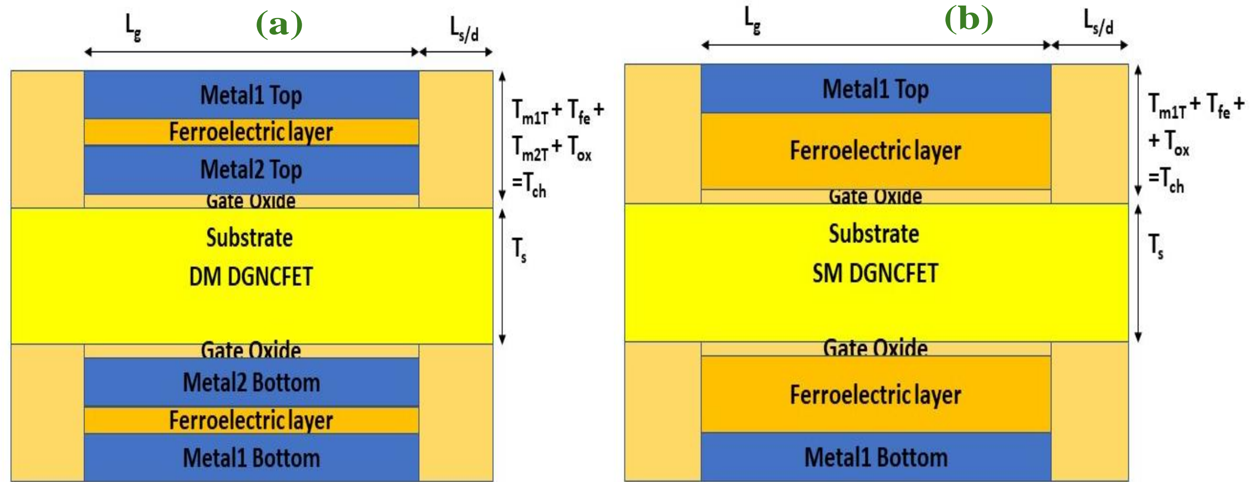

Figure 4.1: Structural diagram of (a) Double Metal Double Gate NCFET(DM DGNCFET) and (b) Single Metal Double Gate NCFET device (SM DGNCFET) (PMC23).

Table 4.1: The Device parameters for SM DGNCFET and DM DGNCFET used for the simulation

Parameter	SM DGNCFET	DM DGNCFET
Oxide Thickness (T_{ox})	0.6 nm	0.6 nm
Gate length (L_g)	50 nm	50 nm
Substrate thickness (T_{sub})	05 nm	05 nm
Ferroelectric thickness (T_{fe})	07 nm	07 nm
Source/Drain length ($L_{s/d}$)	05 nm	05 nm
Metal1 Top/Metal1 bottom thickness ($T_{m1T/m1b}$)	10 nm	10 nm
Doping concentration of Drain/ Source ($N_{d/s}$)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}

The channel length (L_{ch}) is 60 nm, the Drain/Source length ($L_{d/s}$) is 50 nm, the Drain/Source thickness ($T_{d/s}$) is 5 nm, and the oxide thickness (T_{ox}) is 0.6 nm. The SM DGNCFET features a T_{ox} of 7 nm, with Metal1 having top and bottom layers each 10 nm thick as detailed in Table 4.1.

Both SM DGNCFET and DM DGNCFET have a total gate length (L_g) of 50 nm. The entire gate thickness (T_{ch}) of the SM DGNCFET is 10 nm. The materials used include aluminium for Metal1 Top and Metal1 Bottom, Metal2 Top and Metal2 Bottom. The gate oxide is composed of SiO_2 and the ferroelectric material is HfO_2FE (silicon doped hafnium dioxide). The substrate is made with silicon. The doping concentration of the Drain/Source is 1×10^{20} cm^{-3}, with a Gaussian profile, as shown in Table 4.1. The work function of the aluminium used in the dual gate

is 4.2 eV.

4.2.2 Structure of Ferroelectric HfO_2-Based Crystal

The ferroelectric HfO_2 structure is formed in a simple cubic crystal lattice with dimensions a = 10.23 Å, b = 10.23 Å, c = 10.23 Å, and angles $\alpha = 90°$, $\beta = 90°$, $\gamma = 90°$. The crystal structure consists of eight hafnium (Hf) atoms and sixteen oxygen (O) atoms in its undoped state. Figure 4.2 shows the HfO_2 structure: (a) without doping, and (b) with 12.5% silicon (Si) doping. The cartesian coordinates for Si doping are [0.7677, 2.621, 3.128] Å. This research has demonstrated that HfO_2 films doped with 12.5% Si, grown to a thickness of 7 nm between dual-gate metal electrodes, and annealed, may exhibit ferroelectricity. Some studies indicate that the ferroelectric behavior of TiN/HfO_2/TiN stacks is significantly inhibited when the film is annealed before deposition of the top electrode, suggesting that the confinement provided by the top electrode during annealing is crucial for ferroelectricity (GCMK+11).

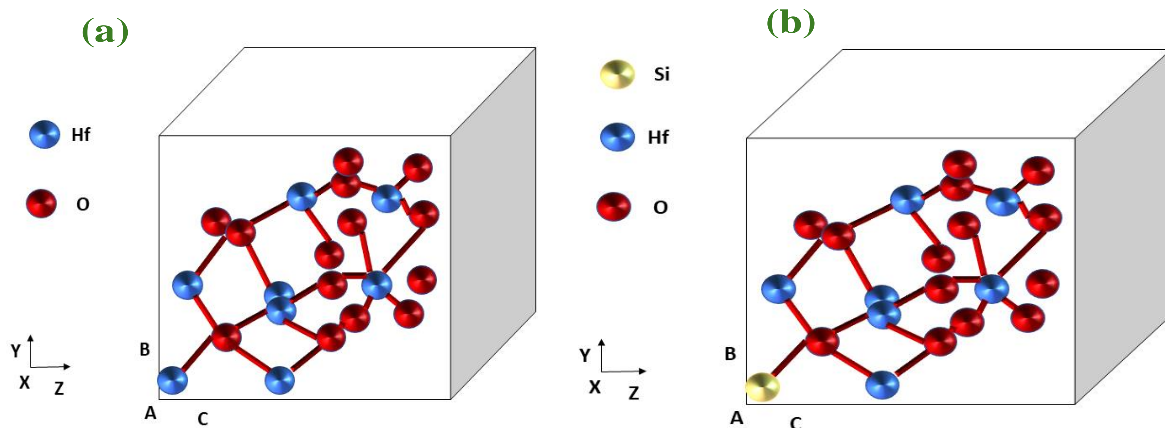

Figure 4.2: Structural diagram of HfO_2 ferroelectric based simple cubic crystal (a) without doping (b) with Si doping (PMC23).

4.3 Methodology and Theoretical Details

4.3.1 Device Methods

All numerical simulations were performed using the Cogenda Visual TCAD Multiphysics tool. A comparative analysis is performed between two devices: DM DGNCFET and SM DGNCFET. During operation, the drain voltage is fixed at 0.05V, while the gate voltage was varied between 0 and 0.5 volts. The temperature (T) was maintained constant at 300K throughout all the simulations. To encounter key phenomena in the device, various models are used in the simulation. The Shockley-Read-Hall (SRH) model to account the generation and recombination of the carriers while the Lombardi surface mobility model accounts for carrier mobility, complemented by Fermi-Dirac statistics. The Arora model considers the effects of temperature and impurity concentration on carrier mobility along with Crowell Sze that accounts for impact ionization. Different boundary conditions were applied to implement the designs of the SM DGNCFET and DM DGNCFET. The congruence of typical sections of translation vectors was used at the oxide-ferroelectric interfaces in the SM DGNCFET structure. The internal metal gate serves as a coating terminal in the DGNCFET structure (HPC$^+$16b; MPAS15).

4.3.2 Method for HfO_2 Crystal

The Quantum ATK (Atomistix ToolKit) simulator was employed for atomic-level studies using DFT. We utilized DFT within the Perdew-Burke-Ernzerhof Generalized Gradient Approximation (PBE GGA) framework (PBE96) with ultrasoft pseudo-potentials to compute the minimal energy structures. The Tran-Blaha modified Becke-Johnson (TB-mBJ) approximation was used to accurately determine the band gap of the crystal. To eliminate the effect of electric fields in the vacuum, a fictional dipole was introduced in the cell's vacuum area, canceling out the electric field. The forces on all atoms were relaxed until they were less than 10^{-4} Ry/Bohr in magnitude in all axial directions (BV00; DGMIB19).

4.3.3 Flowchart for Fabrication Feasibility from Atomic Modeling to Device Fabrication

The process of modeling from the atomic scale to device fabrication for SM DGNCFET is summarized in Figure 4.3. We begin with an atomic model to calculate band energy in vander waals heterostructures (vdWH) at an interfacial charge. First-principle calculations provide the carrier mobility and dielectric constant of the material (DM18). These material properties are then applied in physics-based device models to understand the electronic and optical configuration using the Quantum ATK simulator. The process starts with the thinning of the silicon film, followed by the deposition of HfO_2, and SiO_2 layers on the silicon interface layer through atomic layer deposition (ALD) (CMY20). The metal gate is fabricated on the gate dielectric using the electron beam evaporation process. The source and drain regions are doped through spike annealing activation, and electron beam evaporation is applied to the surface of the source and drain. This process results in the formation of the SM DGNCFET device.

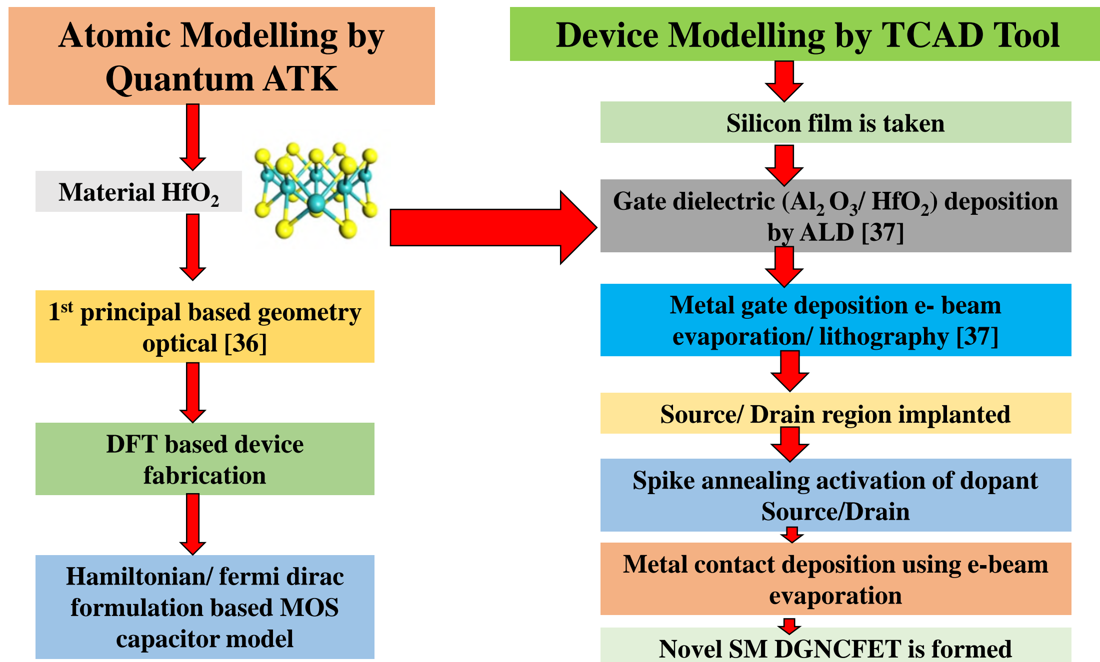

Figure 4.3: Fabrication process flowchart from atomic modelling to device modelling (PMC23).

4.4 Result and Discussion

4.4.1 Comparative Study of NCFET Device

Analog Performance

Figure 4.4(a) presents the drain current, I_d (A), plotted on both linear scale and logarithmic scale against the gate voltage, V_g (V), for SM DGNCFET and DM DGNCFET at $V_{ds} = 0.05$V, with channel length of 50 nm at temperature of 300K. The figure shows that under low gate bias, the off-state current of the SM DGNCFET is lower. As the gate voltage increases, the drain current in the SM DGNCFET design surpasses that of the DM DGNCFET, and indicating better gate coupling capacitance. In SM DGNCFET structure, the simplified gate material and reduced complexity contribute to better control of the channel, leading to an enhanced drain current. The single metal interface minimizes potential mismatch between different metals, resulting in more efficient electron flow.

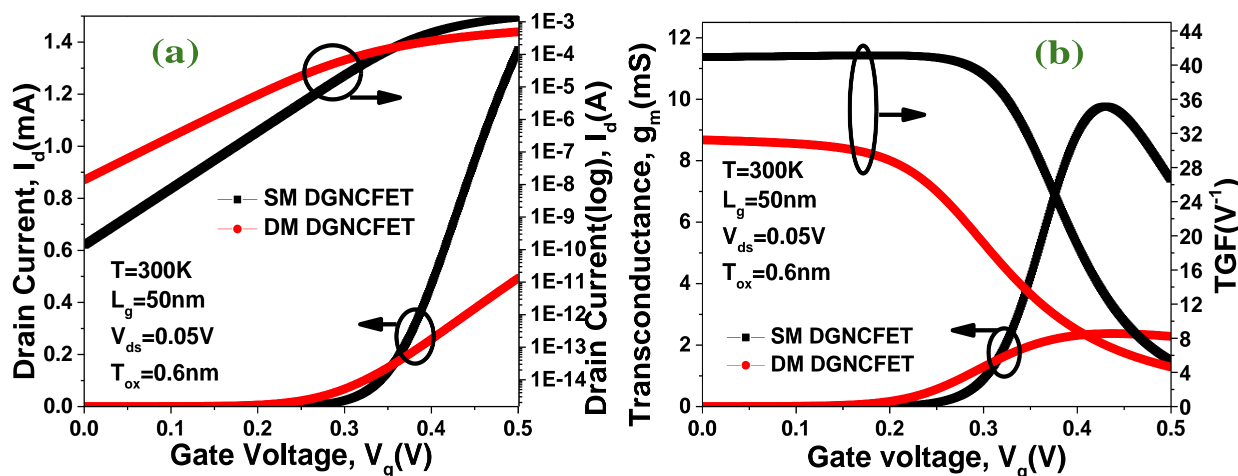

Figure 4.4: Plot of (a) drain current and log drain current vs gate voltage (b) transconductance and TGF vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05V (PMC23).

Transconductance measures the ratio of change in drain current with change in gate voltage at a drain voltage of 0.05V and a temperature of 300K, as shown in Figure 4.4(b). The SM DGNCFET exhibits higher transconductance compared to the DM DGNCFET. This improvement in g_m reflects

a stronger correlation between drain current and gate voltage (NG18), indicating strong coupling between the gate and channel, and increased average carrier's mobility(LHL+22). The transconductance generation factor is also higher for SM DGNCFET, as shown in Figure 4.4(b), due to improved g_m.

Table 4.2: The parameters of leakage current, subthreshold swing, DIBL, and others for SM DGNCFET and DM DGNCFET

Parameter	SM DGNCFET	DM DGNCFET
I_{on} (A) (10^{-3})	1.37	0.493
$V_{th}(mV)$	180.72	86.687
SS (mV/dec)	57.322	59.6
I_{off} (A)(10^{-10})	1.4	1.41
DIBL	0.0462	0.2187
$I_{on}/I_{off}(10^5)$	97.85	0.3496

Figure 4.5(a) shows the plot of DIBL for different configurations. DIBL is a short-channel effect that allows electrons to travel more easily from source to drain as the channel length decreases. The DIBL in the SM DGNCFET structure is lower than in the DM DGNCFET structure, due to better gate control and a more uniform electric field along the channel in SM DGNCFET stucture, indicating reduced short-channel effects and low power consumption. Subthreshold swing is also crucial, with an optimal limit of 60 mV/decade as per Boltzmann limitation at room temperature in conventional MOS devices. The SM DGNCFET achieves lower SS than the DM DGNCFET, ensuring high speed and efficient switching of SM DGNCFET between OFF and ON states.

The threshold voltage, V_t (V), of the SM DGNCFET at a drain voltage of 0.05V is more in comparison to DM DGNCFET design, as illustrated in Figure 4.5(b). This is attributed to better drain-side potential shielding in SM DGNCFET. Additionally, at a gate length (L_g) of 50 nm and T_{ox} of 0.6 nm, the SM DGNCFET structure demonstrates higher switching ratio as compared to DM DGNCFET, due to the uniform work function and electrostatic potential lead to strong gate control in SM DGNCFET structure. Thus, SM DGNCFET achieves faster switching speed with reduced leakage current, and overall better performance in comparison to DM DGNCFET at T = 300K and V_{ds} = 0.05V, as also summarized in Table 4.2.

Figure 4.6(a) illustrates the output characteristics of both the devices, highlighting the variation

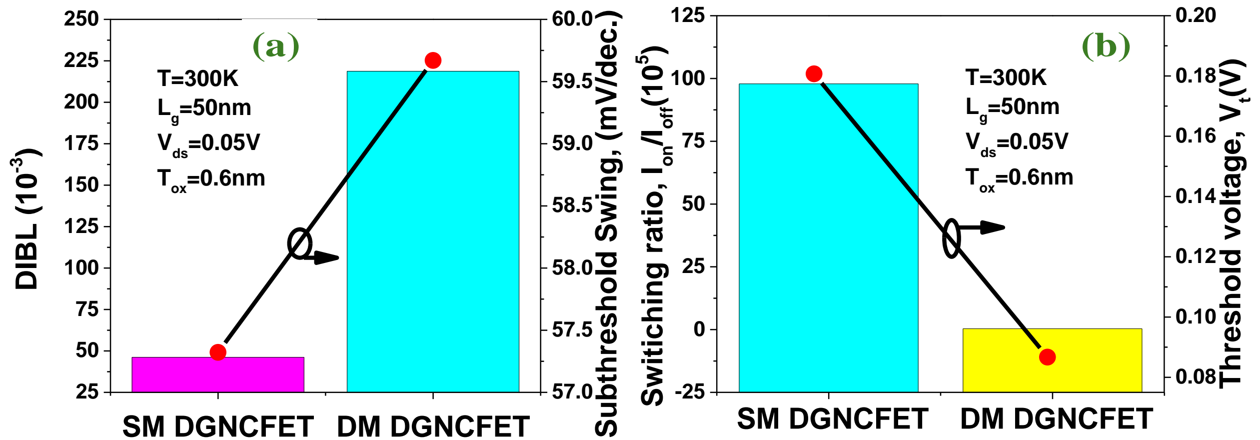

Figure 4.5: Plot of (a) DIBL and subthreshold swing vs gate voltage (b) switching ratio and threshold voltage vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage= 0.05V (PMC23).

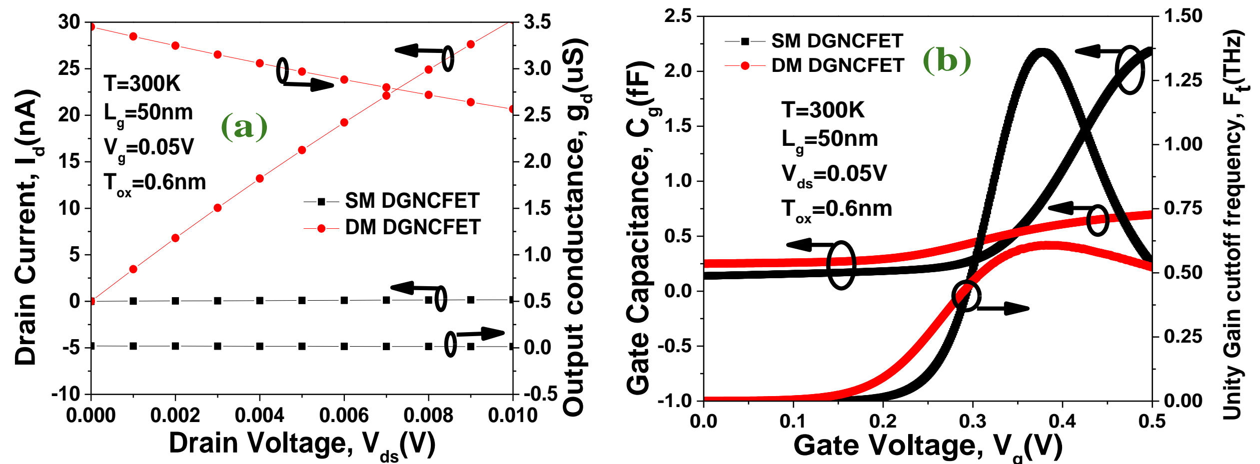

Figure 4.6: Plot of (a) drain current and output conductance vs drain voltage (b) gate capacitance and unity gain cutoff frequency vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage =0.05V (PMC23).

of drain current and output transconductance with changes in drain voltage. Due to DIBL and channel length modulation, a high output conductance is initially observed in the linear region as the drain voltage increases beyond the pinch-off voltage (AS15). The g_d slope of the SM DGNCFET is less steep than that of the DM DGNCFET, indicating superior gate controllability and better suppression of short-channel effects, as shown in Figure 4.6(a). In the SM DGNCFET, the uniform electrostatic control provided by the single gate metal ensures that the drain current remains more

stable with changes in the drain voltage, resulting in a lower output conductance and improved output resistance.

Radio Frequency Analysis

Figure 4.6(b) shows the variation of gate capacitance and unity gain cutoff frequency with the gate voltage. F_t represent the frequency at which unilateral current gain drop to unity (0 dB) and related by Eq. 4.1. It is visible from the figure that the SM DGNCFET configuration exhibits higher gate capacitance and cutoff frequency as compared to the DM DGNCFET configuration, ensuring its capability of better amplification without significant distortion, leading to better overall signal integrity and fidelity. The SM DGNCFET has also higher gate charge than other designs which is reflected in its increased gate capacitance, allowing the device to operate efficiently at higher frequencies.

F_{max} represent the frequency at which unilateral power gain drop to unity (0 dB). The F_{max} values for the SM DGNCFET is higher than those for the DM DGNCFET, indicating superior frequency gain response at a drain voltage of 0.05V as shown in Figure 4.7(a). The higher F_{max} value reflects increased electron mobility for SM DGNCFET, higher overdrive voltage to enhance g_m, and suitability for minimum gate length applications.

$$F_{\mathrm{t}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gd}} + C_{\mathrm{gs}})} \tag{4.1}$$

$$GFP = (\frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}) \times F_{\mathrm{t}} \tag{4.2}$$

The maximum frequency power gain (F_{max}) is directly proportional to the cutoff frequency (F_t). F_{max} and F_t represent the frequencies at which unilateral power gain and current gain respectively drop to unity (0 dB). The F_{max} and F_t values for the SM DGNCFET are higher than those for the DM DGNCFET, indicating superior frequency gain response at a drain voltage of 0.05V as shown in Figure 4.7(a). The higher F_{max} and F_t values reflect increased electron mobility for SM DGNCFET, higher overdrive voltage to enhance g_m, and suitability for minimum gate length

applications (BS21).

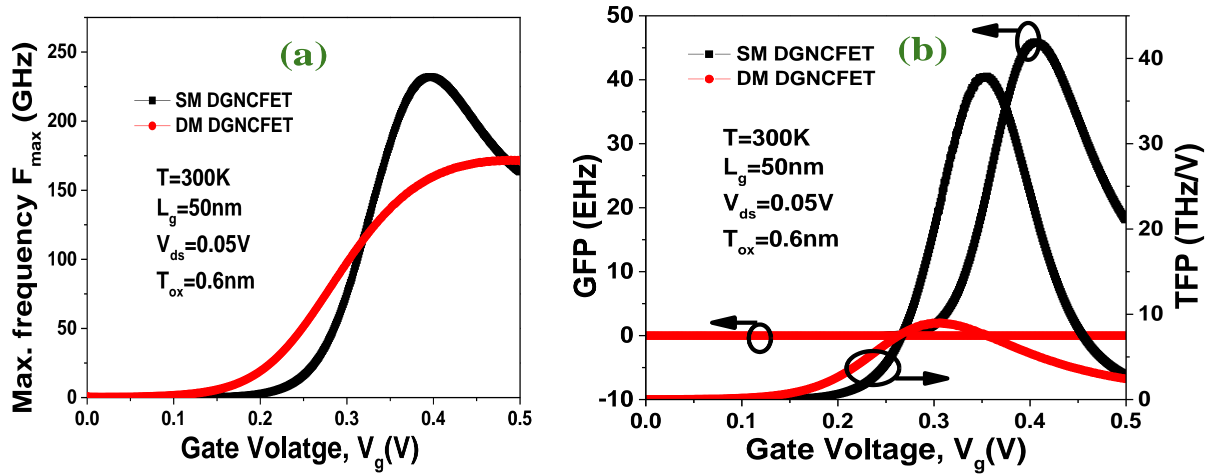

Figure 4.7: (a) The curve of maximum frequency vs gate voltage (b) GFP and TFP vs gate voltage at ferroelectric thickness =7nm, temperature =300K, drain voltage = 0.05V (PMC23).

Figure 4.7(b) shows the variation of gain frequency product (GFP) and transconductance frequency product (TFP) versus gate voltage for various architectures at T = 300K and V_{ds} = 0.05V. The gain frequency product is a key parameter for high-frequency applications, as defined by Eq. 4.2. As shown in Figure 4.7(b), the GFP increases with rising gate voltage, reaching a peak before stabilizing at a constant value in the saturation region. The SM DGNCFET design exhibits the highest GFP value due to its improved output transconductance and transconductance with minimal reduction in cutoff frequency. Conversely, TFP as related by Eq. 4.3, decreases as V_g increases due to the rise in C_g, and once V_g reaches a saturation point, it remains at a minimal constant value. In terms of speed, transconductance, and TFP, the SM DGNCFET is the most suitable structure.

$$TFP = (\frac{g_{\rm m}}{I_{\rm d}}) \times F_{\rm t} \tag{4.3}$$

Linearity Parameter

Figure 4.8(a) displays the second-order and third-order transconductance, (g_{m2} and g_{m3}) versus gate voltage for both SM DM DGNCFET and DM DGNCFET at drain voltage of 0.05V. Nonlinear

characteristics are significant source of distortion and must be carefully examined. To achieve high linearity, nonlinear parameters should be minimized. The nearly identical values of these

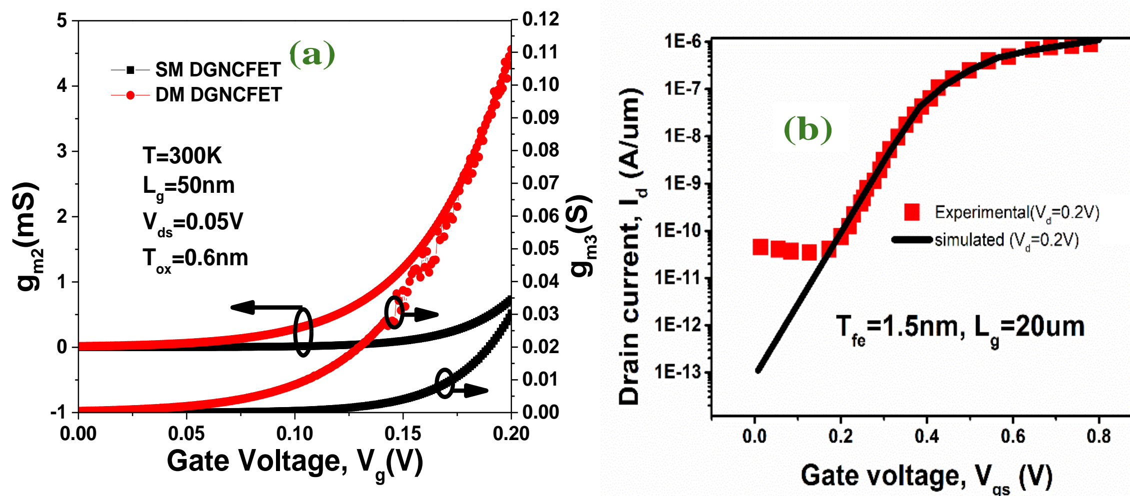

Figure 4.8: (a) Plot of second and third order transconductance vs gate voltage for SM DGNCFET and DM DGNCFET at drain voltage =0.05V, (b) The calibration curve between drain current vs gate voltage curve at drain voltage =0.2V from reference (LFT+16) (PMC23).

parameters at high gate voltage indicate that increasing gate bias, the SM DGNCFET has minimal impact on them. Figure 4.8(b) shows the calibration of the NCFET based on experimental data with a gate length of 20 µm, a ferroelectric thickness of 1.5 nm, and a drain voltage of 0.2V. The experimental data, referenced from (LFT+16), validates the physical models used in the study. The close agreement between simulated and experimental results confirms the accuracy of the simulation models.

Impact of Ferroelectric Thickness, Substrate Thickness, and Temperature

Figure 4.9(a) compares the performance of SM DGNCFET and DM DGNCFET structures with varying ferroelectric material thickness (T_{fe}) at 5 nm, 6 nm, and 7 nm. The performance of the SM DGNCFET improves more significantly than that of the DM DGNCFET as T_{fe} increases. At T_{fe} = 7 nm, the SM DGNCFET exhibits lower leakage current and better switching ratio. Figure 4.9(b) shows the effect of varying substrate thickness (T_{fe}) at 4 nm, 5 nm, and 6 nm, where the device performance is optimized at 4 nm. Figure 4.9(c) illustrates the impact of different temperatures

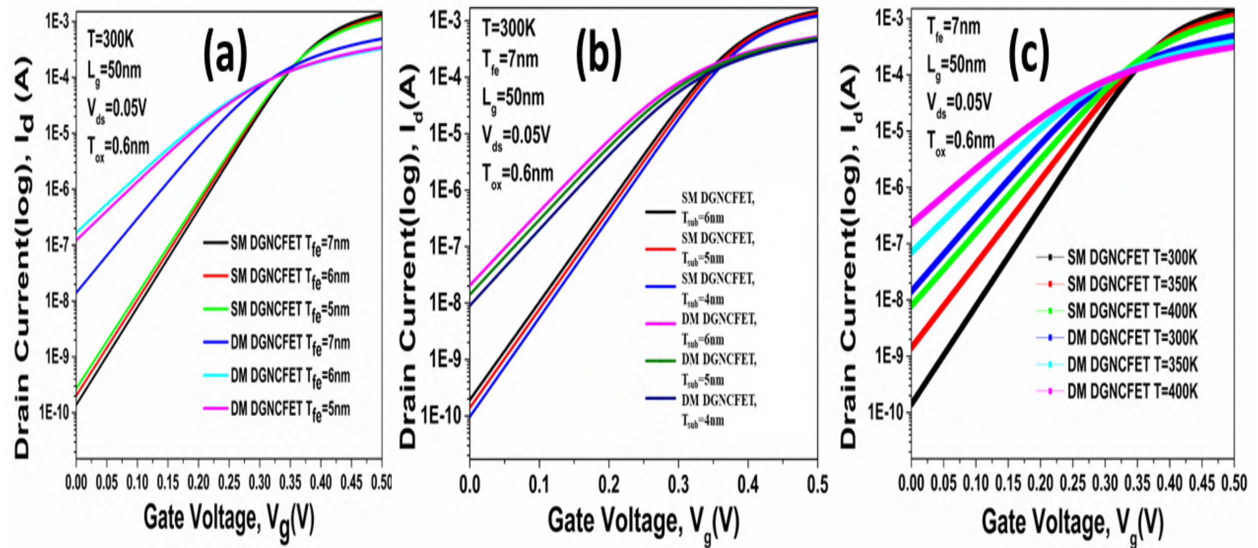

Figure 4.9: The curve of drain current vs gate voltage for (a) variation of ferroelectric thickness (b) different substrate thickness (c) variation of temperature (PMC23).

on device performance with drain voltage maintained at 0.05V throughout the simulation. The temperatures considered are 300K, 350K, and 400K. The SM DGNCFET performs best at 300K, showing reduced leakage current with higher switching ratio ensuring better gate controllability and lower power consumption.

4.4.2 DFT Analysis of Ferroelectric HfO_2 based Crystal

Figure 4.10 illustrates the band structure for (a) Si doping and (b) without doping. It was observed that 12.5% Si doping significantly altered the band gap of HfO_2, reducing the direct band gap to 0.20 eV and the indirect band gap to 0.193 eV, with two-fold degeneracy as shown in Figure 4.10(a) and (b). The narrowing of the band gap can be attributed to the presence of Si states. Table 4.3 provides the Brillouin zone values, including their coordinates and symmetry K points used for the DFT analysis.

Figure 4.11(a) shows the Hartree potential versus the length of atom for both the doped and undoped samples, revealing the mean field electrostatic interaction between atoms. The electrostatic potential from the electron density is calculated using the Poisson equation. Additionally, Figure 4.11(b) depicts the electron density versus the length of atom for both the Si-doped and undoped samples, showing a proportional relationship to the square magnitude of the wave function and the

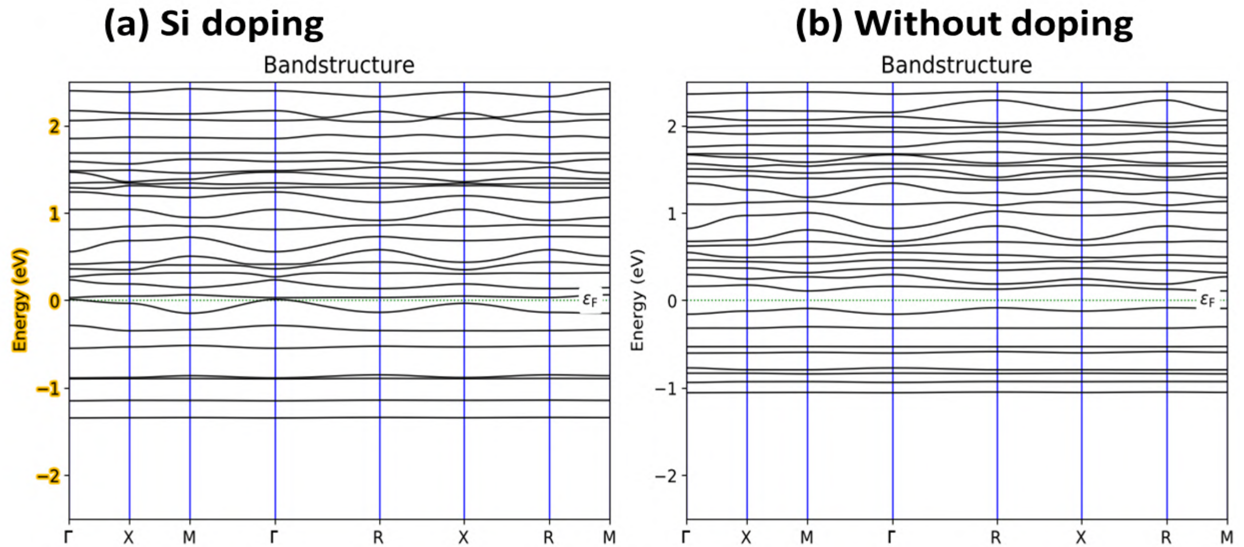

Figure 4.10: Band structure for (a) Si doping (b) without doping (PMC23).

probability of electron presence in a given space. Si doping results in a shorter collision time due to higher electron density.

Table 4.3: Brillouin Zone (BZ) of the specific position of ferroelectric HfO_2 based crystal for band stucture

Value	Fractional, [K_x,K_y,K_z]	Cartesian(A^{-1})	Position along bandstructure, x
Gamma G	[0 , 0 , 0]	[0.0000, 0.0000, 0.0000]	0.0000e+00
X	[1/2, 0 , 0]	[0.3071, 0.0000, 0.0000]	1.1142e-01
M	[1/2, 1/2, 0]	[0.3071, 0.3071, 0.0000]	2.2285e-01
G	[0 , 0 , 0]	[0.0000, 0.0000, 0.0000]	3.8043e-01
R	[1/2, 1/2, 1/2]	[0.3071, 0.3071, 0.3071]	5.7342e-01
X	[1/2, 0 , 0]	[0.3071, 0.0000, 0.0000]	7.3100e-01
R	[1/2, 1/2, 1/2]	[0.3071, 0.3071, 0.3071]	8.8858e-01
M	[1/2, 1/2, 0]	[0.3071, 0.3071, 0.0000]	1.0000e+00

Figure 4.12 presents the density of states (DOS) versus energy for (a) Si doping and (b) without doping. At the Fermi energy (E_f), the enhanced conductivity is associated with increased DOS,

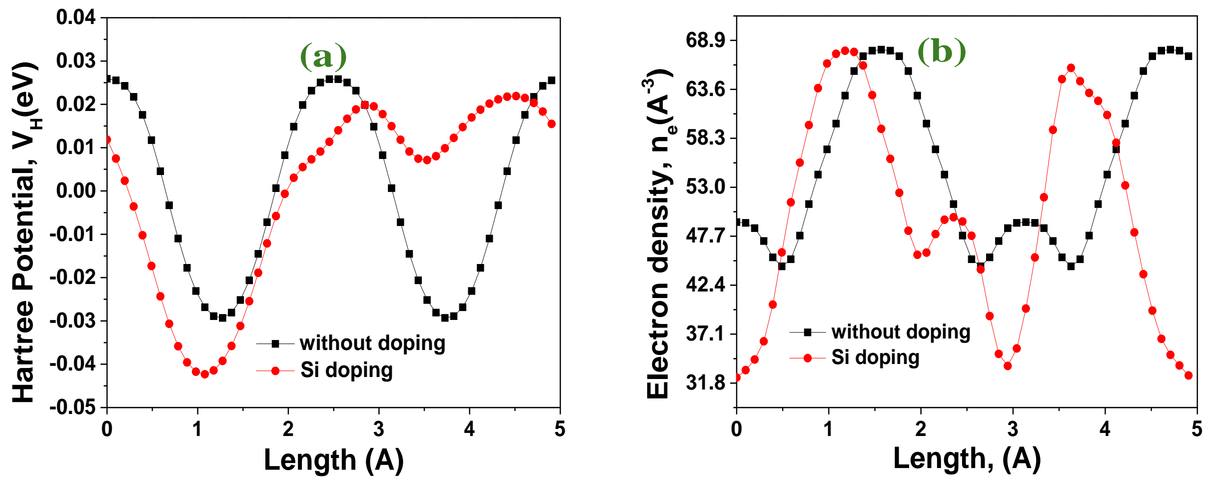

Figure 4.11: (a) Curve of Hartree potential vs length of atom, (b) Curve of electron density vs length of atom for without doping and Si doping (PMC23).

indicating that more states are available for occupation. The DOS for all doping levels was examined to understand the impact of different atomic species on electronic structures as shown in Figure 4.12(a) and (b). In all doped structures, the contribution of different atoms to the valence bands (VB) is similar to that in pure c-HfO_2. However, the Si states in the lower conduction band (CB) appear between 0 and 0.5 eV. At 0 eV, Si states dominate over Hf and O states, reflecting the extent of hybridization. As the doping concentration of Si in HfO_2 increases, the DOS magnitude grows proportionally due to the increased number of Si atoms.

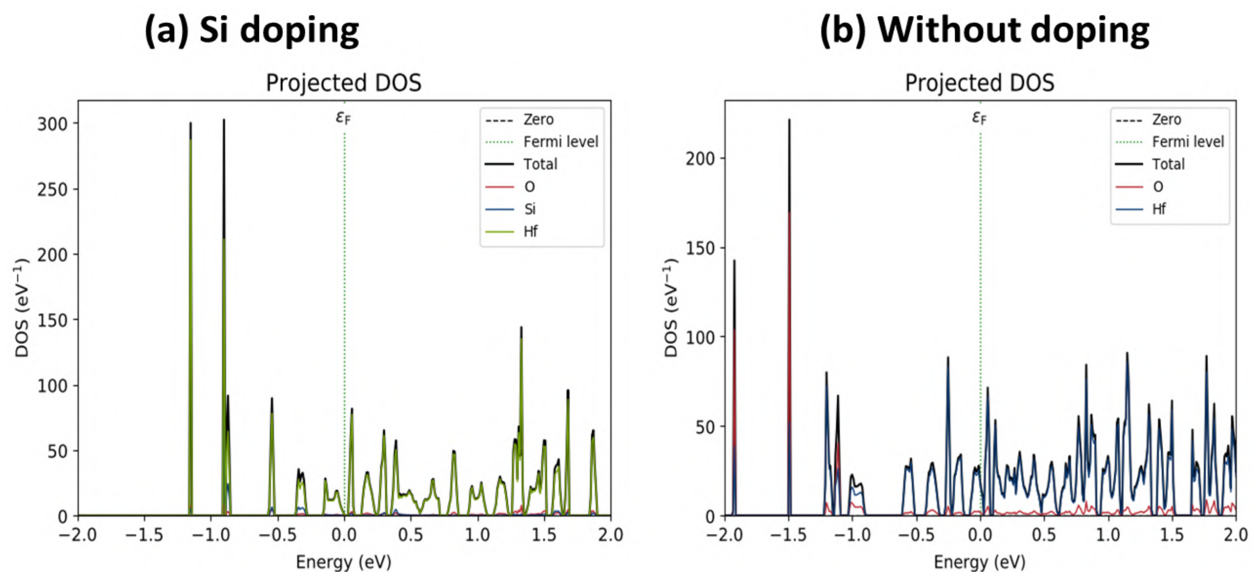

Figure 4.12: Curve of density of state vs energy for (a) Si doping and (b) without doping at centre of fermi energy (PMC23).

4.5 Summary

This paper presents a comparative study of DM DGNCFET and SM DGNCFET. The SM DGNCFET demonstrates superior performance in terms of analog/RF and linearity parameters, including DIBL, SS, transconductance, TFP, GFP, g_{m2}, and g_{m3}. Atomic modeling advancements in quantum theory are explored using DFT, which helps in determining the energy, band structure, and other properties of materials at atomic level. The Tran-Blaha modified Becke-Johnson (TB-mBJ) approximation accurately predicts the band gap of crystals. The DFT analysis of hafnia (HfO_2)-based simple cubic crystals, for both undoped and with 12.5% Si doping, shows improved results for Si doping with the band structure approaching zero band gap and enhanced DOS, ensuring better conductivity.

The present chapter of this thesis has focused on the extensive analysis of DGNCFET with single and double metal configurations for analog/RF and linearity parameters, following the DFT-based atomic modeling of silicon doped HfO_2, which can be very useful for high performance applications. Consequently, the proposed device has the potential to be explored for accurate prediction of device's characteristics through the application of machine learning techniques involving artificial neural network based modelling. This will be the main area of emphasis in the next chapter.

Chapter 5

Artificial Neural Network based Modelling for Variational Effect on Double Metal Double Gate Negative Capacitance FET

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* This chapter investigated the Artificial Neural Network based Modelling for prediction of the different key analog parameters of negative capacitance FET by using Machine Learning Approach for Double Metal Double Gate NCFET (DM DGNCFET).
* Analog parameters of DM DGNCFET are analysed for various temperature (T), oxide thickness (T_{ox}), substrate thickness (T_{sub}), and ferroelectric thickness (T_{Fe}) and it is found that DM DGNCFET exhibits higher switching ratio due to reduction in leakage current at T=300K by 84 times in comparison to T=500K, at T_{Fe}=4nm by 5.4times in comparison to T_{Fe}=8nm, at T_{sub}=3nm by 81% in comparison to T_{sub}=7nm, at T_{ox} =0.8nm by 41% in comparison to T_{ox}=0.4nm.
* Consequently, All the results analysed reveals that T_{Fe}=4nm, T=300K, T_{ox} =0.8nm, and T_{sub}=3nm reflects most improved performance for the DM DGNCFET, and can further be used for various applications with nanoelectronic devices and IC designing.

5.1 Introduction

Since the four decades in the semiconductor industry, the size of FET devices has been decreased to attain better efficiency and performance, in possession with Moore's law (KLK+19a; WCR+15; WCB+13; GAA+13). The new trend of VLSI is governing the variability issue, such as global variability (GV) and local variability (LV) sources for both planar and gate-all-around (GAA) devices. In the case of LV source, a high-k/metal gate device with various work functions, which is vital for statistical variability, would be at extreme risk for device performance because of the random occupied grain orientation of gate material (WBCA11; DEDB10). Additionally, in the case of the GV source, the impact of critical dimension is variability in varying the device performance, and as device size is reduced, this effect cannot be ignored.

The power and thermal management of integrated circuits are vital aspects of the transistor industry. Although with engineering technology and material science advancement, power dissipation in transistors has been decreased a lot. However, the ICs have millions of transistors on the chip, which generate huge amounts of heat. Due to its lesser supply voltage, tunnel FETs have also been cited by many research organizations in the semiconductor world as the ideal FET over traditional MOSFETs for future low-power applications. But dealing with TFET can lead to low I_{on}, so to get the amalgamation of improved I_{on} and subthreshold swing, the NC technology is an apt candidate to meet the demand of future electronics. (RTU21).

However, the variability focuses on the accurate prediction of correlation among different sources. Cogenda Visual TCAD and Python are proven tools for doing complicated analysis. However, a large number of samples is required for better performance. Hence, a large computational budget is inevitable for precise prediction. In this study, a method of variability analysis is proposed for modeling at device level with minimum error (HLC+20; KLK+19b; WG21). Consequently, we propose a new method of machine learning (ML) algorithm with a precise match of the TCAD simulator for improved efficiency. This article consists of an analysis of analog parameters of DM DGNCFET for different oxide thicknesses, ferroelectric thickness, temperature, and substrate thickness, which results in reduced subthreshold swing ensuring low input power consumption, reduced leakage current, and reduced DIBL, ensuring better controllability of the device.

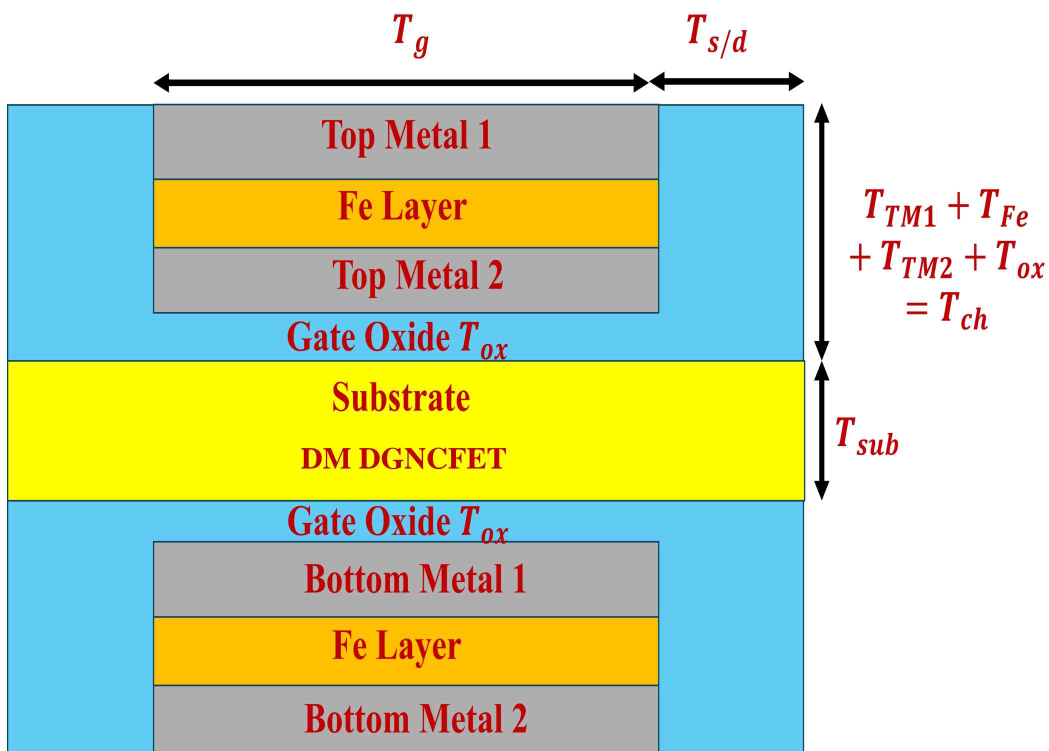

Figure 5.1: The 2D schematic diagram of Double Metal Double Gate NCFET (PMC23).

5.2 Device Architecture and Simulation Methodology

Figure 5.1 shows the schematic diagram of the Double Metal Double Gate NCFET (PDAC18). The parameters of DM DGNCFET are summarized in Table 5.1. The channel is made with silicon material and has a length of $L_g = 60nm$. The drain and source are made with aluminium which has length $L_{d/s} = 50nm$. The thickness of the substrate (T_{sub}), oxide (T_{ox}), top metal1/bottom metal1 (T_{TM1}/T_{TB1}), top metal2/bottom metal2 (T_{TM2}/T_{TB2}) are $5nm$, $0.6nm$, $10nm$, $5nm$ respectively. The total thickness of channel (T_{ch}) is $10nm$ as illustrated in Table-5.1. The material of top metal1/bottom metal1, top metal2/bottom metal2 is Aluminium. The material taken for ferroelectric material and gate oxide are silicon doped hafnium oxide (HfO_2FE), and SiO_2 respectively. The work function (ϕ) of aluminium material is fixed at $4.2eV$ for the double gate. The concentration of the doping profile for Source/Drain ($N_{s/d}$) is $1.0 \times 10^{20} cm^{-3}$.

The entire simulation is done by Cogenda Visual TCAD and Python high-level language. The gate voltage (V_{gs}) is varied from $0 - 0.5V$, with drain voltage fixed at $0.05V$. The various physical models are used in this work, such as Shockley Read Hall (SRH) which includes generation and

Table 5.1: The Device parameters for DM DGNCFET are used for the simulation

Parameter	Symbol	DM DGNCFET
Substrate thickness	T_{sub}	$5nm$
Ferroelectric thickness	T_{fe}	$7nm$
Oxide Thickness	T_{ox}	$0.6nm$
Gate length	L_g	$50nm$
Concentration of Source/Drain	$N_{s/d}$	$10^{20}cm^{-3}$
Source/Drain length	$L_{s/d}$	$5nm$
Top/Bottom Metal thickness	T_{m1}/T_{m1b}	$10nm$

recombination effects associated with carriers, the Arora model which incorporates the effects on carrier mobility due to temperature and impurities concentration, complemented by Fermi-Dirac statistics, Crowell Sze for considering the effects associated with the impact ionization on the carriers.

5.3 Artificial Neural Network (ANN) Implementation

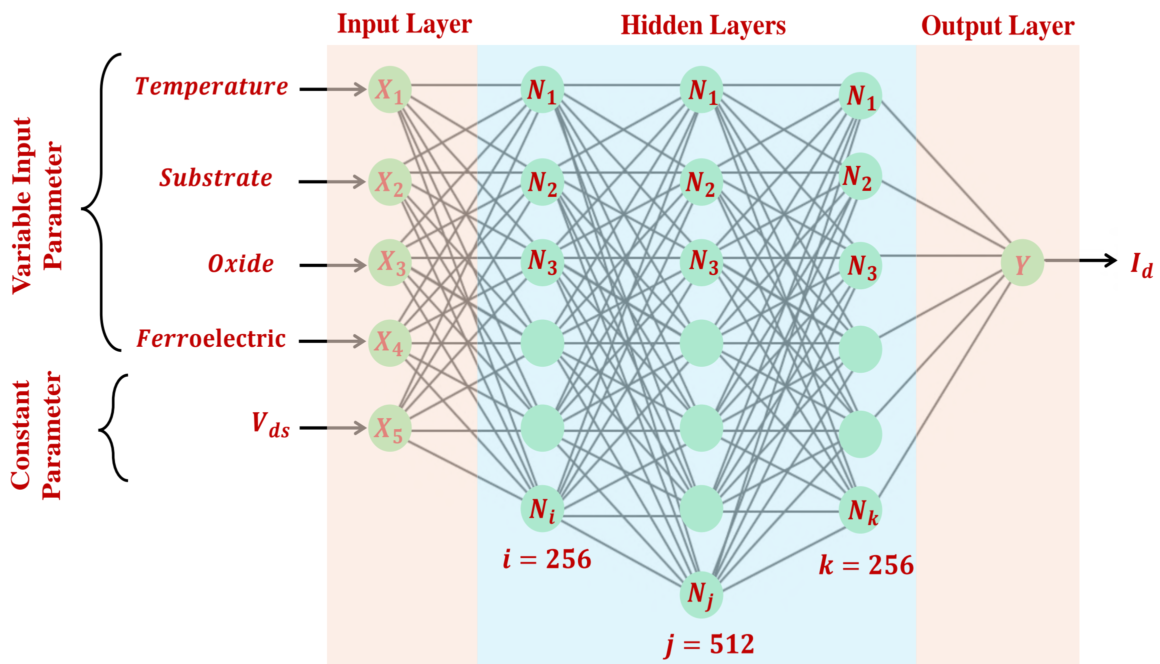

Figure 5.2: The figure shows the DM DGNCFET Artificial Neural Network (ANN) with one input, one output, and three hidden layers. There are 256 neurons in the first and third hidden layers, and 512 neurons in the middle layer V_{ds} (KLK+19a)

We constructed a tensor flow-based ANN model with a Rectified Linear Unit (ReLU) activation function (HSS15; DST+23; KDM17) for DM DGNCFET. The architecture of the ANN model is shown in Figure 5.2. The input to the input layer is an array of size 5 for each variable taken such as temperature, substrate thickness, oxide thickness, ferroelectric thickness, and the drain voltage. The output layer provides the ANN prediction for the drain current. Further, we consider three hidden layers in our ANN model. The first and third layers have 256 neurons while there are 512 neurons in the middle layer. The output of each neuron in the Neural Network (NN) is given as:

$$a_p^{[q]} = g\left(\vec{W}_p^{[q]} \cdot \vec{a}^{[q-1]} + b_p^{[q]}\right) \tag{5.1}$$

where, q represents the layers of the neural network (NN), and p is the node number such that $a_p^{[q]}$ is the output of pth node from q^{th} layer. g is the activation function. $\vec{W}$ and b are the weight and biasing parameters for each node.

This function is repeated and runs up to the Taylor series to get the precise result. The input value put in ANN does not exclude work function variation (WFV) due to WFV impact and its effect on the variability of T_{ox}, T, T_{sub}, and T_{Fe}. The algorithm of the implemented DM DGNCFET ANN is illustrated in Figure 5.3.

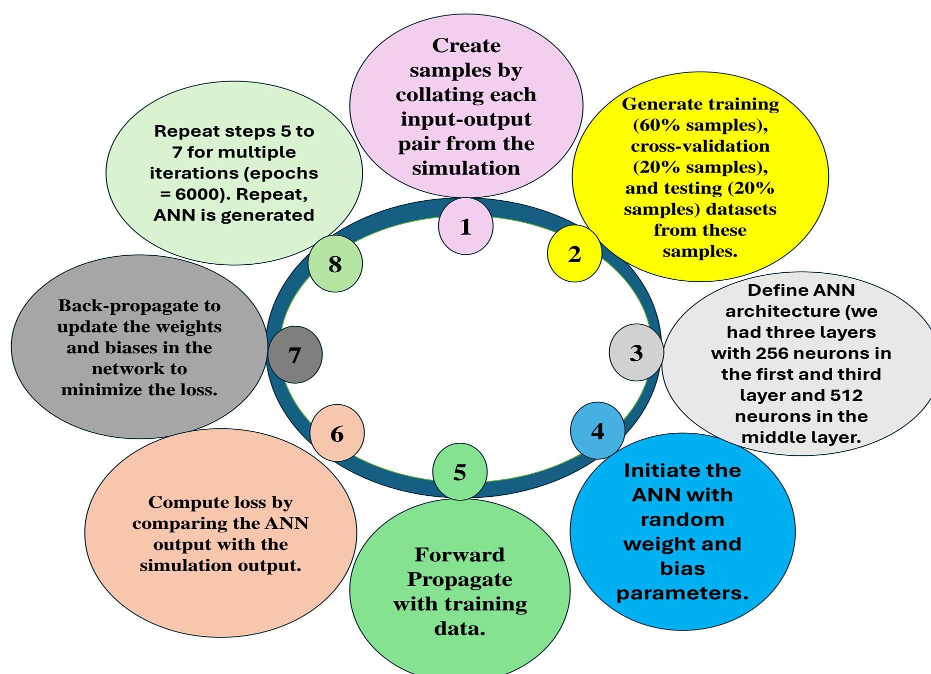

Figure 5.3: Algorithm for DM DGNCFET Artificial Neural Network (ANN) (KLK+19a).

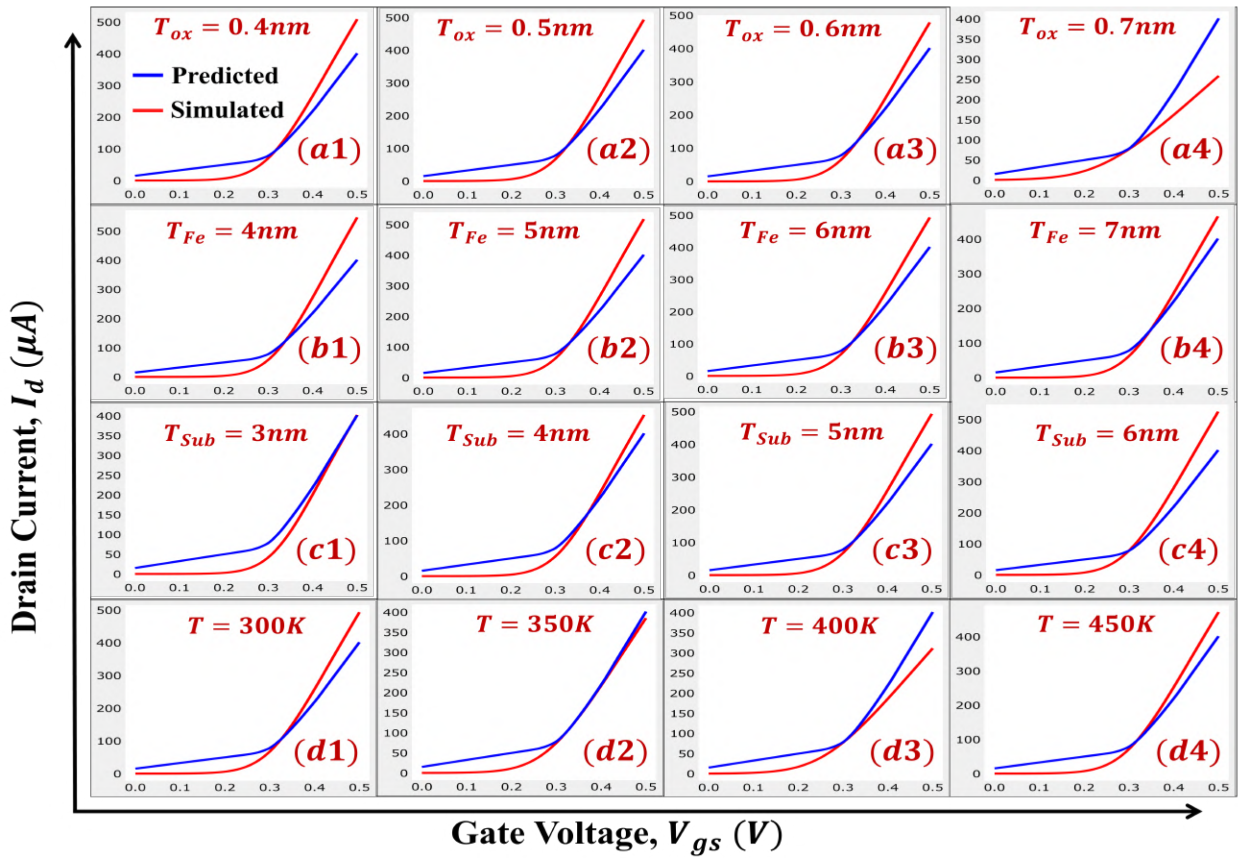

Figure 5.4: The graph of drain current vs gate voltage for predicted and simulated data of DM DGNCFET for different variations of temperature, oxide thickness, ferroelectric thickness, and substrate thickness at V_{ds}=0.05V (KLK+19a; PMC23).

5.4 Result and Discussion

Figure 5.4 represents the drain current (I_d) vs gate voltage (V_{gs}) of the TCAD simulation study (in red dash line) and predicted data (blue dash line) by ANN model for DM DGNCFET at $V_{ds} = 0.05V$. The variation with oxide thickness (T_{ox}) are displayed in subplots (a1)-(a4) at $T_{Fe} = 7nm$, $T = 300K$, and $T_{sub} = 5nm$. The predicted and simulated data shows a precise match at $T_{ox} = 0.6nm$, which reflects the lower error at $0.3V$ of gate voltage. The variation with ferroelectric thickness (T_{Fe}) is shown in subplots (b1)-(b4) at $T_{ox} = 0.6nm$, $T = 300K$, and $T_{sub} = 5nm$. The precise data of predicted and simulated is matched at $T_{Fe} = 8nm$, reflecting the lower error after $0.3V$ of gate voltage. The variation with substrate thickness (T_{sub}) is illustrated in subplots (c1)-(c4) at $T_{ox} = 0.6nm$, $T = 300K$, and $T_{Fe} = 7nm$. The precise data of predicted and simulated is matched at $T_{sub} = 4nm$, which reflects the lower error at $0.3V$ of gate voltage. The variations with temperature is shown in subplots (d1)-(d4) at $T_{ox} = 0.6nm$, $T_{Fe} = 7nm$, and

$T_{sub} = 5nm$. The predicted and simulated data are matched at $T = 300K$, which reflects the minimum error at $0.3V$ of gate voltage. The different variations of all data variables turned out to coincide at gate voltage at 0.3V. The trainer of predicted data works successfully as a transfer characteristics start from off current to linear current.

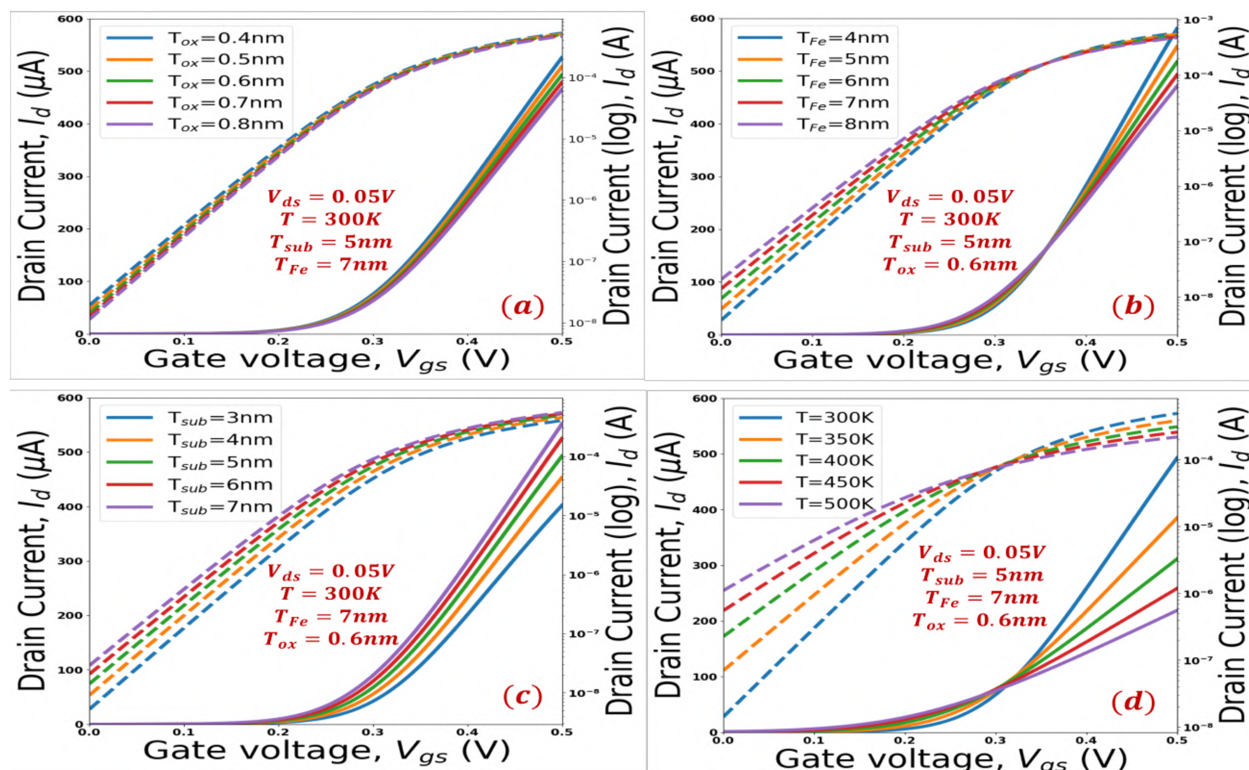

Figure 5.5: The graph of drain current vs gate voltage DM DGNCFET for different variations of temperature, oxide thickness, ferroelectric thickness, and substrate thickness at V_{ds}=0.05V (PMC23).

Figure 5.5 shows the curve of transfer characteristics of DM DGNCFET in linear and log scales for various temperatures and thicknesses. The device characteristics with variation in oxide thickness (T_{ox}) are shown in Figure 5.5(a) at fixed $V_{ds} = 0.05V$, $T = 300K$, $T_{Fe} = 7nm$, $T_{sub} = 5nm$. The better performance of the device is represented at $T_{ox} = 0.8nm$, which has a lower leakage current, higher drain current, and better switching ratio, confirming the improved gate controllability. The improving trend of drain current for DM DGNCFET for higher oxide thickness is due to the negative capacitance effect provided by the ferroelectric material, which compensates for the increased gate thickness. It allows for the retention of strong gate control over the channel, while the increased oxide thickness reduces leakage pathways. Thus, this results in lower leakage currents, especially in the off-state, and higher drain current. The impact of variation of ferroelectric thickness(T_{Fe}) is shown in Figure 5.5(b) at fixed $V_{ds} = 0.05V$, $T = 300K$, $T_{ox} = 0.6nm$, and

$T_{sub} = 5nm$. The better performance of the device is represented at $T_{Fe} = 4nm$ with lower leakage current and higher drain current, resulting in a better switching ratio with low power consumption. The drain current of DM DGNCFET is improved with lesser ferroelectric thickness because a thinner ferroelectric layer facilitates the capacitance matching between the ferroelectric and gate oxide layer. This helps in maintaining strong gate control over the channel and thus reducing leakage current in the device.

The effect of variation of substrate thickness (T_{sub}) is shown in Figure 5.5(c) at fixed $V_{ds} = 0.05V$, $T = 300K$, $T_{ox} = 0.6nm$, and $T_{Fe} = 7nm$. The better performance of the device is exhibited at $T_{sub} = 3nm$, which shows higher drain current, and lower leakage current resulting better switching ratio. It shows that the drain current for DM DGNCFET is improved with lesser substrate thickness. With a thinner substrate, the double gate design helps to confine the carriers in the channel more effectively, thus providing tighter control over channel and minimizing the leakage paths, resulting in a more efficient device. The influence of variation in temperature (T) is shown in Figure 5.5(d) at fixed $V_{ds} = 0.05V$, $T_{Fe} = 7nm$, $T_{ox} = 0.6nm$, and $T_{sub} = 5nm$ with all the results summarized in Table 5.2. The better performance of the device is represented at $T = 300K$, which has a lower leakage current and a higher drain current, thus ensuring a better switching ratio. The drain current of DM DGNCFET is improved at low temperatures due to the combination of strong gate control and reduced thermal generation of carriers at low temperature. Also, drain current is influenced by factors such as mobility and threshold voltage, both of which improve at lower temperatures, making the device more efficient at low temperature.

The simulation and ANN prediction results are compared in Figure 5.6. The linear relation between the prediction and the TCAD simulation results signifies the accuracy of our ANN model as depicted in subplot Figure 5.6(a). We further computed the losses during each epoch of training the ANN model. The loss reduces by increasing the number of epochs as shown in subplot Figure 5.6(b).

Figure 5.7 shows the plot of transconductance and TGF as a function of gate voltage for various temperatures, and different thicknesses at $V_{ds} = 0.05V$. The subplot (a) shows the transconductance (g_m) and transconductance gain factor (TGF) of DM DGNCFET at $T_{ox} = 0.8nm$ is higher than other oxide thickness, which reflects better gain generated per unit cell at $T_{Fe} = 7nm$,

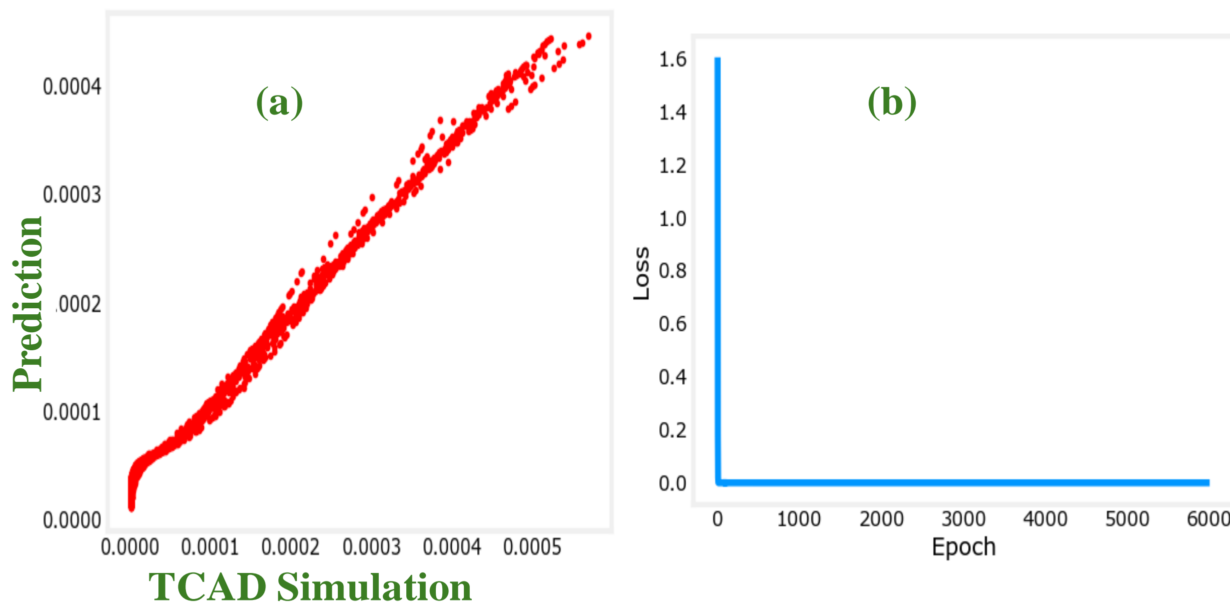

Figure 5.6: The figure shows the comparison of TCAD simulated output and the output predicted by ANN model. (a) The graph of predicted versus simulated data and (b) model loss at each epoch during the training of ANN model (KLK+19a).

$T = 300K$, and $T_{sub} = 5nm$. With higher oxide thickness, the gate capacitance is optimized for the negative capacitance effect in the ferroelectric material. This improves the overall gate control over the channel, allowing for more efficient charge transport and better current modulation. As a result, g_m and TGF increases, leading to higher device performance. The subplot (b) shows the transconductance and transconductance gain factor of DM DGNCFET at T_{Fe}=4nm is higher than other thickness of ferroelectric layer, which reveals better gain generated per unit cell at T=300K, T_{ox}=0.6nm, and T_{sub}=5nm. A thinner ferroelectric layer enhances the negative capacitance effect, which boosts the effective gate voltage amplification. This leads to stronger modulation of the channel with small changes in gate voltage, increasing g_m. The enhanced coupling between the gate and the channel due to the reduced ferroelectric thickness ensures that the device is more responsive, improving the transconductance and TGF significantly.

The subplot (c) The transconductance and transconductance gain factor of DM DGNCFET at T_{sub}=3nm is higher than other thickness of substrate, which reflects better gain generated per unit cell at T_{Fe}=7nm, T_{ox}=0.6nm, and T=300K. Higher substrate thickness can reduce the fringing electric fields from the drain, which helps in maintaining strong gate control over the channel. This improved gate control allows for better current modulation, resulting in higher g_m.

Table 5.2: DM DGNCFET comparison for different temperature, substrate thickness, ferroelectric, oxide thickness.

No.	Parameter	I_{off} $(10^{-8}A)$	I_{on}/I_{off} (10^5)	V_{th} (mV)
$(a1)$	$T = 300k,\ T_{ox} = 0.4nm,\ T_{sub} = 5nm,\ T_{Fe} = 7nm$	1.92	0.273	77.23
$(a2)$	$T = 300k,\ T_{ox} = 0.5nm,\ T_{sub} = 5nm,\ T_{Fe} = 7nm$	1.62	0.314	82.278
$(a3)$	$T = 300k,\ T_{ox} = 0.7nm,\ T_{sub} = 5nm,\ T_{Fe} = 7nm$	1.25	0.383	89.52
$(a4)$	$T = 300k,\ T_{ox} = 0.8nm,\ T_{sub} = 5nm,\ T_{Fe} = 7nm$	1.13	0.412	92.18
$(b1)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 5nm,\ T_{Fe} = 4nm$	0.382	1.52	118.2
$(b2)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 5nm,\ T_{Fe} = 5nm$	0.605	0.89	107.77
$(b3)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 5nm,\ T_{Fe} = 6nm$	0.935	0.55	97.2
$(b4)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 5nm,\ T_{Fe} = 8nm$	2.08	0.227	76.065
$(c1)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 3nm,\ T_{Fe} = 7nm$	0.523	0.768	115.107
$(c2)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 4nm,\ T_{Fe} = 7nm$	0.906	0.5	99.462
$(c3)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 6nm,\ T_{Fe} = 7nm$	2.06	0.2548	74.58
$(c4)$	$T = 300k,\ T_{ox} = 0.6nm,\ T_{sub} = 7nm,\ T_{Fe} = 7nm$	2.88	0.192	63.84
$(d1)$	$T = 300k,\ T_{sub} = 5nm,\ T_{Fe} = 7nm,\ T_{ox} = 0.6nm$	1.41	0.347	86.68
$(d2)$	$T = 350k,\ T_{sub} = 5nm,\ T_{Fe} = 7nm,\ T_{ox} = 0.6nm$	6.96	0.0553	40.23
$(d3)$	$T = 400k,\ T_{sub} = 5nm,\ T_{Fe} = 7nm,\ T_{ox} = 0.6nm$	0.225	0.0138	-5.21
$(d4)$	$T = 450k,\ T_{sub} = 5nm,\ T_{Fe} = 7nm,\ T_{ox} = 0.6nm$	0.55	0.0047	-50.04
$(d5)$	$T = 500k,\ T_{sub} = 5nm,\ T_{Fe} = 7nm,\ T_{ox} = 0.6nm$	0.011	0.0012	-94.86

A thicker substrate also helps in reducing unwanted leakage paths through the bulk, ensuring that more of the applied gate voltage is used to control the channel, further enhancing g_m and TGF. The subplot (d) The transconductance and transconductance gain factor of DM DGNCFET at T=300K is higher than the other temperatures, which reflects better gain generated per unit cell T_{Fe}=7nm, T_{ox}=0.6nm, and T_{sub}=5nm. This is due to increased carrier mobility and reduced phonon interactions (vibrations in the lattice) at lower temperature. The increased carrier mobility allows for a larger change in drain current with a small change in gate voltage, boosting g_m and TGF.

Figure 5.8 shows the spider chart of leakage current, switching ratio, and threshold voltage for

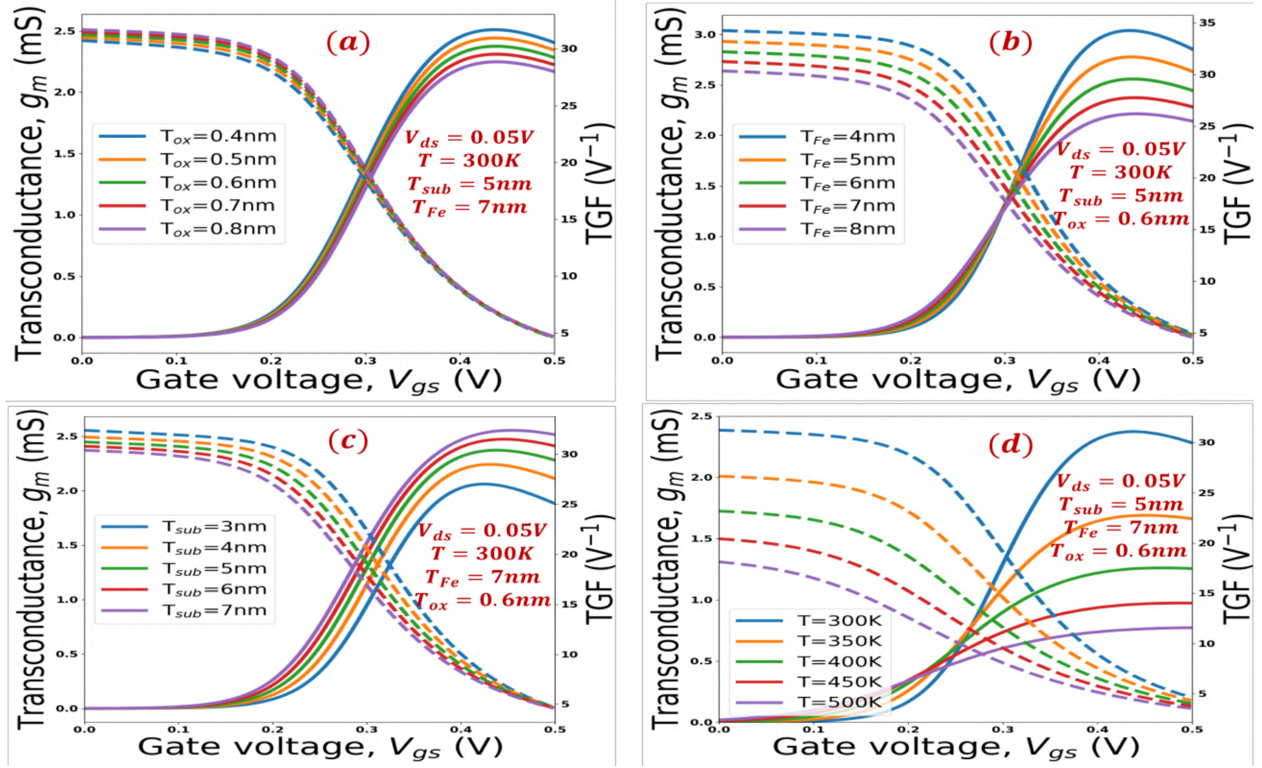

Figure 5.7: The plot of transconductance and TGF vs V_{gs} for various temperature and thicknesses at V_{ds}=0.05V (PMC23).

different temperatures and thicknesses of different variable sets. (a) The oxide thickness of 0.8nm shows higher switching ratio, lower leakage current, and higher threshold voltage at V_{ds}=0.05V, $T_{Fe} = 7nm$, $T_{sub} = 5nm$, and $T = 300K$. Oxide thickness plays a key role in controlling gate leakage current. A thicker oxide increases the distance between the gate and the channel, which reduces tunneling current. This is crucial for suppressing gate leakage, particularly in ultra-scaled devices where leakage current is a major concern. (b) The ferroelectric thickness of $4nm$ results in higher switching ratio, lower leakage current, and higher threshold voltage at $V_{ds} = 0.05V$, $T_{ox} = 0.6nm$, $T_{sub} = 5nm$, and $T = 300K$. Since leakage current is typically caused by the inability to properly control the channel in the off-state, a thinner ferroelectric layer enhances gate modulation and keeps the leakage current low. (c) The substrate thickness of $3nm$ showcases higher switching ratio, lower leakage current, and higher threshold voltage at $V_{ds} = 0.05V$, $T_{Fe} = 7nm$, $T_{ox} = 0.6nm$, $T = 300K$. This occurs due to reduced substrate thickness, which reduces the parasitic resistance in the device and improves the drive current in the on-state. Also the ferroelectric layer in an NCFET is responsible for the negative capacitance effect, which enhances the overall device performance by reducing the effective gate capacitance and improving gate control. A thinner substrate enhances

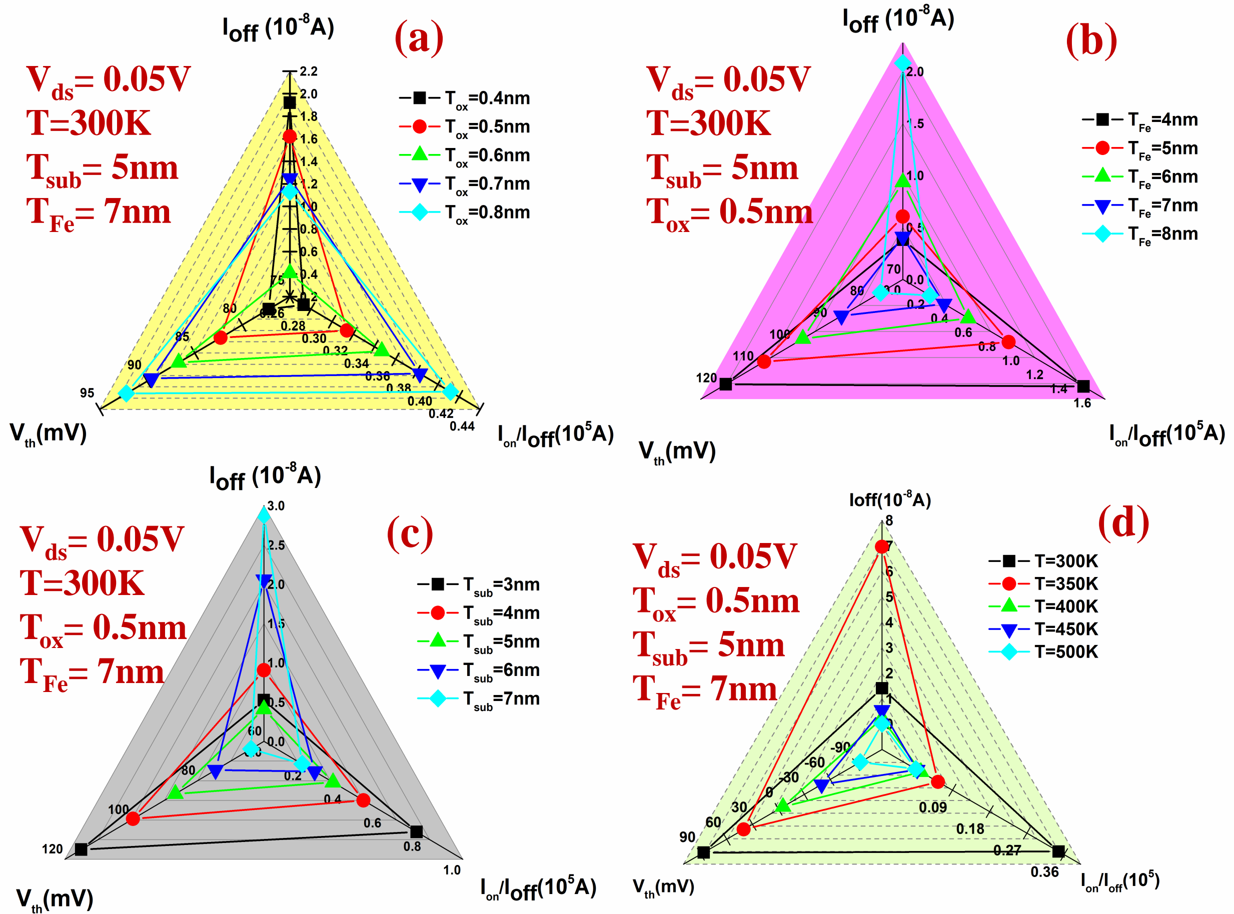

Figure 5.8: The spider chart of leakage current, switching ratio, threshold voltage for different temperature and thicknesses at V_{ds}=0.05V (PMC23).

the ability of the negative capacitance to influence the channel by bringing the channel closer to the gate. (d) The temperature of 300K reflects higher switching ratio, lower leakage current, and higher threshold voltage at $V_{ds} = 0.05V$, $T_{Fe} = 7nm$, $T_{sub} = 5nm$, $T_{ox} = 0.6nm$. In NCFETs, although the negative capacitance effect in the ferroelectric layer enhances gate control, but leakage current still depends on thermal effects. Lower temperatures reduce the intrinsic carrier concentration in the semiconductor, leading to a decrease in off-state leakage currents. This makes the device more efficient, especially when it comes to switching between the on and off states.

5.5 Summary

In this study, we analyzed the application of ANN-based machine learning to explore the variability in the device performance. The Cogenda Visual TCAD simulator and Python programming

language were employed throughout the process. ANN-based ML significantly reduces the computational cost while providing precise calculations and efficiency. This method of investigating variability processes aids in better optimization and design, which is beneficial for various applications. The analog parameters of DM DGNCFET were studied for various oxide thicknesses, substrate thicknesses, temperatures, and ferroelectric thicknesses. Notable results include a lower leakage current resulting in higher switching ratio which is, 3000 times better at $T = 300K$ as compared at $T = 500K$, improved by 588% at $T_{Fe} = 4nm$ as compared at $T_{Fe} = 8nm$, enhanced by 300% at $T_{sub} = 3nm$ as compared at $T_{sub} = 7nm$, and improved by 50% at $T_{ox} = 0.8nm$ as compared at $T_{ox} = 0.4nm$. These results indicate that $T_{Fe} = 4nm$, $T = 300K$, $T_{ox} = 0.8nm$, and $T_{sub} = 3nm$ are the optimal variable sets for DM DGNCFET, leading to the most improved performance. This analysis can aid the engineers in device designing for various applications with nanoelectronic devices.

After successfully investigating the accurate Machine Learning Approach and Artificial Neural Network based Modelling for predicting the different key analog and RF parameters for DM DGNCFET, the device has showcased its potential and its wide usage in the field of Artificial Intelligence (AI). Further to experimentally explore some work, the research has been further carried out for pH Sensing as Ion Sensitive Field Effect Transistor (ISFET) based sensor and its implementation on TCAD simulator for analysing various device's performance metrics. This will be the main area of emphasis in the next chapter.

Chapter 6

Experimental Circuit Design and TCAD Analysis of Ion Sensitive Field Effect Transistor (ISFET) for pH Sensing

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* This chapter describes the impact of analog and RF parameters for Ion Sensitive FET (ISFET) (added a sensing layer in Double Metal FET by removing ferroelectric layer) to achieve the better performance.

* It is found that the switching ratio is enhanced for Molybednum ISFET by an order of 10^4 as compared to Aluminium. Subsequently, some other analog parameters, such as transconductance, TGF, etc, are also explored.

* It is also found that the switching ratio is enhanced when Al_2O_3 is used as sensing layer in ISFET, along with improvement in some other analog and electrical parameters.

* In addition, the experimental circuit is designed for a pH sensor consisting of ISFET, capsule solution, PBS (Phosphate Buffered Saline), and op-amp components for sensing different pH values.

* Consequently, Molybdenum based ISFETs, which contain molybdenum as gate electrode, show superior performance for various analog metrics along with Al_2O_3 as sensing layer, giving the most desirable performance as pH sensor.

6.1 Introduction

Bergveld first unveiled the Ion Sensitive FET in 1970 (Ber70), which is sometimes referred to as a solid state device that incorporates the chemical sensitivity displayed by semiconductors, a membrane and a FET's field-sensing capacity. The benefits of ISFETs go beyond their small form factor, resilience, as well as relatively affordable production costs, but enable the implementation of advanced smart CMOS-based integrated circuit-based sensor systems. However, threshold voltage instability is also a result of drift, ISFET-based biosensors have not gained popularity and a leading position in the industry. Drift is distinguished by a unidirectional, slowly changing temporal pattern in the threshold voltage, and consequently, the concentration of the provided ion does not bring any change in the drain current of ISFET(EFJ18).

The MOSFET idea provides the foundation of ISFET. The metal gate of the MOSFET is replaced in the ISFET construction with a pH sensor layer. This film is used to monitor the activity of ions in the analyte while being in direct contact with the electrolyte. The ion concentration in the electrolyte controls the current passing through the transistor's channel (CSS+17). The gate area and dimensions of the sensor film affect the device's sensitivity. The study of the ISFET is more interesting for the researchers, and they have looked at numerous insulators as a sensing layer, including Silicon Dioxide (SiO_2), Tantalum Pentoxide (Ta_2O_5), Silicon Nitride (Si_3N_4), and other dielectrics including Aluminium Oxide (Al_2O_3) as sensing film (SDL07).

The chemical interactions between the ISFET gate dielectric on one side and the electrolyte on the other side creates the surface charge density that makes the ISFET sensitive to pH value (VHEB96; DZS+19). In a standard ISFET structure, a sensor membrane known as gate oxide is in direct contact with the solution. This location is relative to the area of the total sensor and alters the ISFET electrical behavior because the measurements of the ISFET's sensitivity are hampered by the presence of the parasitic capacitance feature. The surface charge potential at the surface of an ISFET is activated by protonation and deprotonation processes between the surface and the floating gate, to develop the coupling capacitance. The floating gate of ISFET is modulated by this potential, threshold voltage for chemical and biological sensing (CCC+00). The development and description of the ISFET's sensitivity are very well explained by site-dissociation model given

by Yates (DZS[+]19).

In the article, initially Si_3N_4 is used as sensing film to reflect the sensitivity for different materials of gate electrodes such as Molybdenum, Aluminium, Chromium with its work function 4.75eV, 4.3eV, 4.1eV. Also, the sensing layer of the ISFET is paid more attention by the researchers because the sensing film monitors the activity of existing ions in the analyte after coming in direct contact with electrolyte. To further enhance the sensitivity and improve the stability of the device, an extensive analysis of ISFET with different sensing materials is done. This paper also presents the comparative study of sensing layer of ISFET with sensing film (Al_2O_3, Si_3N_4, SiO_2) for analog and electrical performance.

Further, ISFET also used for measuring the ion concentration in solution. The updated value of pH and the fluid of body indicates the medical issue. The important component for detection of any disease demands high sensitivity, fast respond, robustness, ability to collect and transmit data in real time(Kel00; BMK13). For circuit design, the apparatus is utilized, such as ISFET, op-amp, power supply, resistor, pH value capsule, PBS solution, and multimeter. To create a circuit design that enables the preservation of constant drain current by giving a feedback voltage to the electrolyte at room temperature. ISFET drift data was collected in the feedback mode. In the absence of back bias, the drain current was set at I_d = 100 mA using a constant drain to source voltage. Using a commercial Calomel reference electrode dipped in a phosphate buffer saline with a pH of 7, the ISFET gate voltage was applied. The validation of observation was done by increasing the voltage with a higher value of pH 4.67, 5.9, 7.5, 8.57, and 9.3.

6.2 Device Structure and Circuit Designing

6.2.1 Device Structure of ISFET

Figure 6.1 shows the sketch diagram of the ISFET made by using TCAD tool. The drain current equation is same for both MOSFET and ISFET as exhibited by Eq. 6.1. The structure of ISFET is designed with bulk silicon region having length of 500nm and thickness of 400nm. Drain/Source consists of aluminium with length 30nm and thickness 100nm, reference layer consists of aluminium with length 500nm and thickness 20nm, oxide layer consists of SiO_2 with length 180nm and thickness

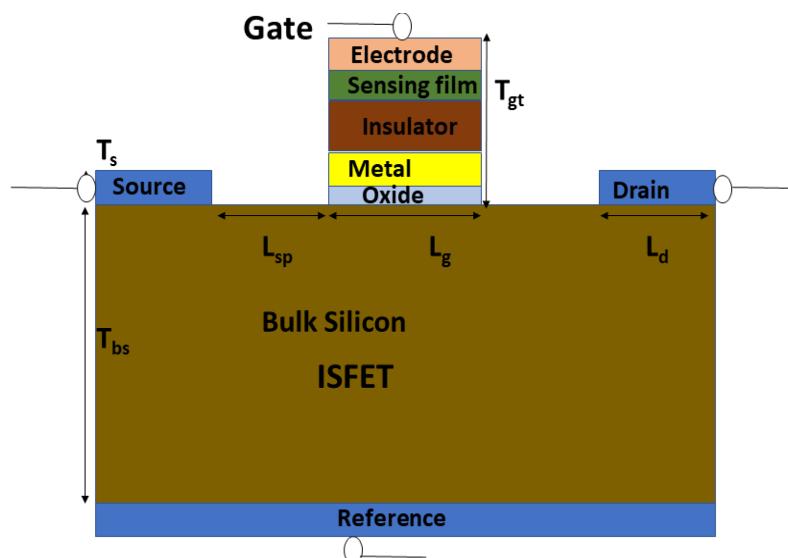

Figure 6.1: Sketch diagram for ISFET structure by TCAD tool (PMS+24).

10nm, electrode region consists of aluminium with length 180nm and thickness 40nm, sensing film consists of Si_3N_4 with length 180nm and thickness 10nm (AS15).

$$I_{\rm d} = \frac{\mu \times C_{\rm ox} \times W}{L} \times [(V_{\rm g} - V_{\rm th}) - \frac{(V_{\rm ds})^2}{2}] \tag{6.1}$$

Here, the threshold voltage is V_{th}, and the width and length of the channel are W and L, respectively.

Table 6.1: ISFET device parameter by TCAD simulation.

Parameter	ISFET
Temperature	300k
Channel length (L_c)	180nm
Oxide thickness (T_{ox})	10nm
Length of drain/ source ($L_{d/s}$)	100nm
Thickness of drain/source ($T_{d/s}$)	30nm
Doping concentration of drain/source	$1 \times 10^{20}\ cm^{-3}$
Width of gate (T_{gt})	130nm

The mobility model is used as an analytical tool in the bulk silicon area as described by Shockley-Read-Hall theory for trap charges (CCC+00). Lombardi surface mobility model is used for accounting carriers's mobility along with Fermi-Dirac models. The gaussian doping concentration is $1 \times 10^{20}\ cm^{-3}$ for drain and source with the donor type along with other device parameters as shown in Table 6.1.

6.2.2 Experimental Circuit Designing of ISFET based pH Sensor

Figure 6.2 (a) shows the circuit diagram of ISFET based pH sensor (b) demonstrating experimental setup (c) showcasing the MP008v2 ISFET. The apparatus utilized for circuit designing are as follows: sodium monohydrate phosphate (Na_2HPO_4) and sodium dihydrogen phosphate (NaH_2PO_4) which were purchased from Sigma Aldrich. ISFET which was purchased from LioniX international site, three 8 pin operational amplifier, wires, multimeter, 9V power supply, voltage divider, 22uf capacitor, 3 resistors as R1-100 Ω, R2-1 KΩ, R3-100 Ω, op 07CN (an operational amplifier).

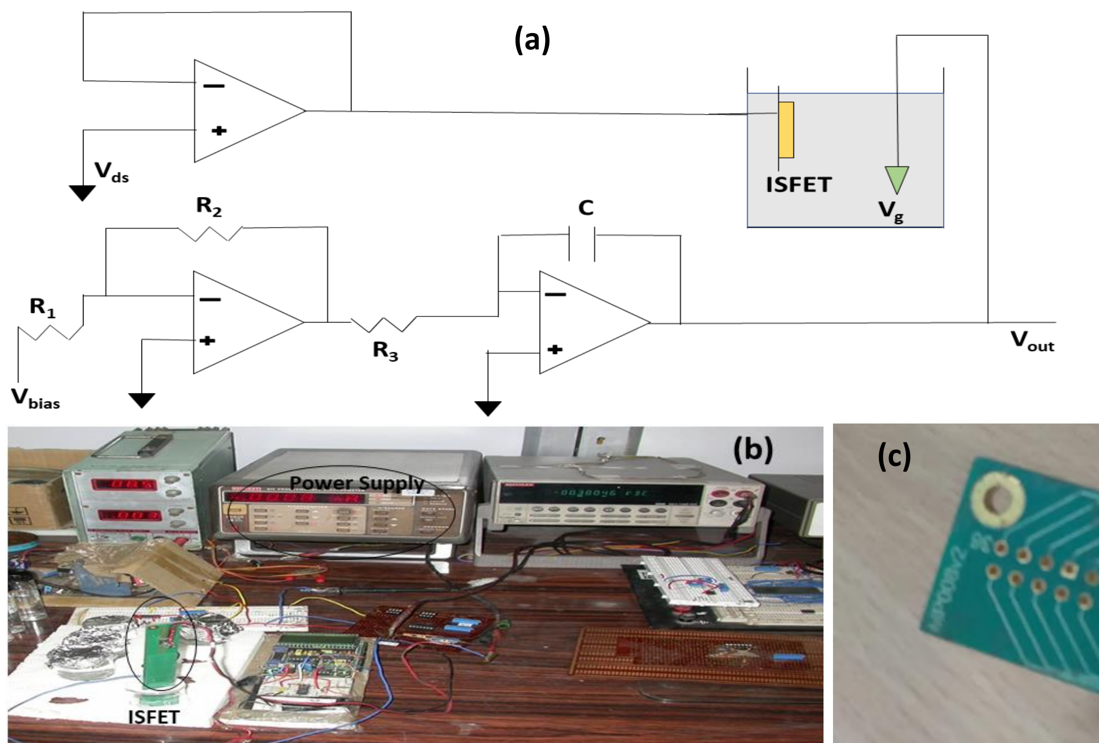

Figure 6.2: (a) Circuit diagram of ISFET based pH sensor (b) Experimental setup (c) MP008v2 ISFET (PMS+24).

This section reveals the ISFET drift in context of the inversion layer's constant, temporal decline of charge density to support the drift counteraction, depending specifically on the closed shape. We shall create a relation for the gate voltage drift (SPK+21), and change in the charge density at the insulator interface, which can be used to create a useful gadget for a way of counteracting drift mobility (EFJ18).

6.3 Simulation Study of ISFET and Circuit based pH Sensor

6.3.1 Simulation Study of ISFET Device

The Visual TCAD tool is used to make ISFET device. We have optimized the device by doing the comparison study of different materials of the gate electrode for ISFET such as Molybdenum(Mo), Chromium(Cr), and Aluminium(Al) with its different work functions 4.75eV, 4.3eV, and 4.1eV respectively. The drain voltage is maintained constant at 0.5V, the gate voltage varies from 0 to 3V. The temperature (T) is maintained at 300K in all circumstances throughout the process of the device simulation. SiO_2 layer is used as gate dielectric in ISFET passivation of silicon, which reduces the charge recombination, protects semiconductor from chemical corrosion. SiO_2 as gate dielectric supports electric field and invert the type of charge carrier in the channel and turn the device ON. To further enhance the sensitivity and improve the stability of the device, an extensive analysis of ISFET with different sensing materials (Al_2O_3, Si_3N_4, SiO_2) of sensing film is studied with Aluminium as gate electrode material.

Although the extent of chemical modification of the Al_2O_3 surface as determined by the thickness of the modified surface layer can be significantly less than that of the Si_3N_4 surface, it is still thought that chemical modification of the insulator surface is the cause of the drift observed in Si_3N_4-gate pH-sensitive ISFETs. The dielectric constant of the changed surface layer will be different from that of the bulk insulator as a result of chemical alteration of the insulator surface. As a result, the total insulator capacitance will gradually decrease over time as surface modification continues. This capacitance is defined by the series combination of the capacitance of the changed surface layer and that of the underlying insulator (EFJ18; MSD20; UKF$^+$00).

6.3.2 Techniques for Experimental Circuit Designing

When the ISFET is replaced with a equilibrium reference electrode ions mixture, they bind the passivation or decay charge recombination thus protect semiconductor from chemical corrosion. This cause an accumulation of charge which in turn bias V_{th} of the device (Ber03). V_{th} of ISFET is dependent on pH of the device which shifts as related in Eq. 6.2. Here the term E_{ref} is reference

potential, x_{sol} is potential for dipole moment in existing solution, ψ_0 is chemical potential of pH. All the terms of the chemical reaction grouped in potential ($V_{chem.}$) are represented in Eq. 6.3. The chemical potential is depicted in Eq. 6.4, γ is potential for non chemical grouping, and α range from 0 to 1 (GT09).

$$V_{\text{th(ISFET)}} = E_{\text{ref}} - \psi_0 + x_{\text{soi}} - \frac{\phi_{\text{m}}}{q} + V_{\text{th(mosfet)}} \tag{6.2}$$

$$V_{\text{chem.}} = E_{\text{ref}} - \psi_0 + x_{\text{soi}} - \frac{\phi_{\text{m}}}{q} \tag{6.3}$$

$$V_{\text{chem.}} = \gamma + \frac{2.3\alpha kT}{q} pH \tag{6.4}$$

The apparatus used for this purpose of experimental circuit designing are: pH capsules, PBS solution for different pH values, wire, operational amplifiers, resistors, capacitors, pH meter, and multimeter. The Faradaic process on electrochemistry helps the electron transfer across the metal (electrode) to solution interface. There is also the process of oxidation and reduction occurring depending on the flow of charge from the electrode. The pH capsule solution is made by applying a power supply of 9V and 1A while dissolving a capsule with pH 4 in 50ml deionized water to make the solution pH 4.67 in 5 minutes. Similarly dissolve the second capsule of pH 4 in 50ml deionized water to make the solution of pH 5.9, dissolve a capsule of pH 7 in 50ml deionized water to make the solution of pH 7.5. and dissolve a capsule of PH 9 in 50ml deionized water to make the solution of pH 9.3. For making the phosphate buffer saline solution, mix the solution of sodium monohydrate phosphate (Na_2HPO_4) and sodium dihydrogen phosphate (NaH_2PO_4) along with adding Ferro and Ferri in 100ml solution.

6.3.3 Fabrication Feasibility of ISFET based pH Sensor

Figure 6.3 shows the device fabrication feasibility of ISFET based pH Sensor with step by step procedure from ISFET to circuit designing for pH sensor. Visual TCAD simulator has reported on the viability of fabricating ISFET. First, silicon film deposition is thinning out. The atomic

layer deposition (ALD) on silicon substrate, and Al_2O_3/Si_3N_4 layer has been created on the metal interface layer (CMY20). The gate metal is created by utilizing the electron beam evaporation method on the gate dielectric. The activation of the spike annealing dopant is inserted in the source and drain regions by lift-off process. With these steps, ISFET is made and then the circuit is designed by using the ISFET device.

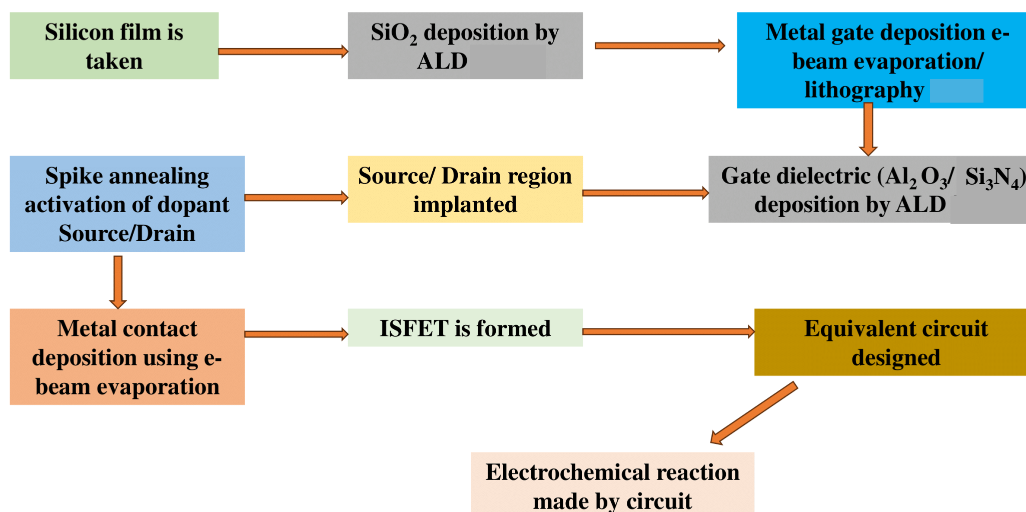

Figure 6.3: The flowchart of fabrication feasibility of ISFET based pH Sensor from ISFET to circuit designing (PMS+24).

6.4 Result and Discussion

Firstly, we have seen the analog and RF parameter of pH-ISFET for various work function (ϕ) to improve the performance of leakage current, subthreshold swing, DIBL etc. Then, an extensive analysis of ISFET with different sensing materials (Al_2O_3, Si_3N_4, SiO_2) of sensing film is done with Aluminium as gate electrode material. The performance is discussed in terms of various static and analog parameters to optimized the device for improved performance as pH sensor.

6.4.1 Comparative Study of ISFET for Different Gate Electrode Material

Figure 6.4 (a) reflects the graph of drain current vs gate voltage in linear and log scale for different materials of gate electrode of ISFET at V_{ds}=0.5V, T=300K. The molybdenum (Mo) with work

function 4.75eV has showed the most improved result in comparison to aluminium, and chromium. Mo showcased better results with substantial reduction in leakage current (I_{off}) on the left side of the graph and also illustrated in Table 6.2. A higher work function in the gate electrode enhances the electric field across the electrolyte and semiconductor interface, leading to more efficient ion modulation in the sensing region. This improves the ability to control charge carriers, resulting in reduced leakage current (SP22).

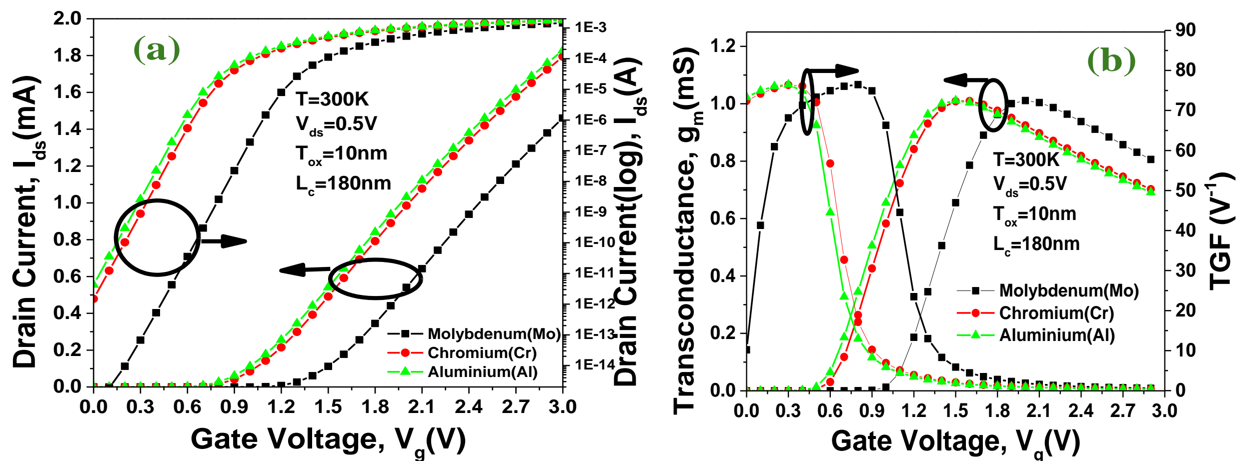

Figure 6.4: (a) I_{ds} - V_g characteristics on the left side and log drain current on the right side (b) g_m - V_g characteristics on left side and TGF on the right side for different materials of electrode used in ISFET designing at V_{ds}=0.5V and T=300K (PMS+24).

Table 6.2: Performance comparison of ISFET for different gate electrode materials such as molybdenum, chromium, and aluminium

Parameter	Molybdenum (Mo)	Chromium (Cr)	Aluminium (Al)
I_{on} (A)	0.00146	0.00179	0.00183
I_{off}(pA)	0.000919	1.4911	4.266
$I_{on}/I_{off}(10^{10})$	158.86	0.12004	0.04289
$V_{th}(mV)$	1	0.6	0.5
SS $(mV/dec.)$	104.8	106.78	107

The transconductance, g_m is defined as shift in drain current vs gate voltage (NG18). Transconductance of Molybdenum as gate electrode is higher than others gate electrodes. Molybdenum is more chemically stable and less prone to oxidation or corrosion than aluminum and chromium. This stability ensures consistent device performance in terms of drain current in response to applied gate

voltage, especially in sensitive environments like biochemical sensing applications, contributing to better overall transconductance as shown in Figure 6.4 (b). TGF is shown on the right side of the figure, demonstrating that it is higher for Mo. Molybdenum's stable interface properties also helps in reducing leakage current for ISFET. Lower leakage current translates into higher TGF, as it maintains a better ratio between transconductance and drain current (SDL07).

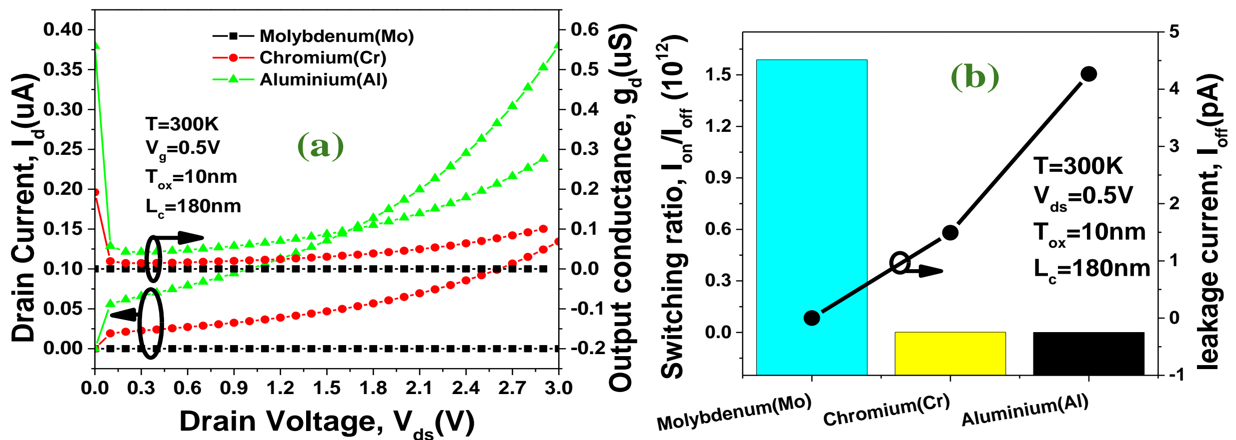

Figure 6.5: (a) I_{ds} - V_{ds} characteristics in the left side and output conductance on the right side (b) The plot of switching ratio on the left side and leakage current on the right side for different materials of electrode used in ISFET designing T=300K (PMS+24).

Figure 6.5 (a) exhibits the graph of drain current vs drain voltage on the left side and output conductance (g_d) on the right side for different materials of gate electrode used in ISFET designing at V_g=0.5V and T=300K. The performance of output conductance for the molybdenum is better in comparison to others. The rise in drain voltage beyond pinch-off voltage results in high output conductance in the linear region due to channel length modulation. As demonstrated in Figure 6.5(a), for molybdenum, g_d twist is less as compared to Al and Cr, indicating better gate controllability and capacity to inhibit short direct strikes.

Figure 6.5 (b) reveals the plot of switching ratio on the left side and I_{off} on the right side for different materials of gate electrode ISFET design at V_{ds}=0.5V, T=300K. For Molybdenum, the device gives lower leakage current and higher switching ratio. The higher work function creates a stronger energy barrier at the gate, reducing unwanted carrier leakage when the device is in its off state. This minimizes leakage current and improves the device's drain current, enhances power efficiency.

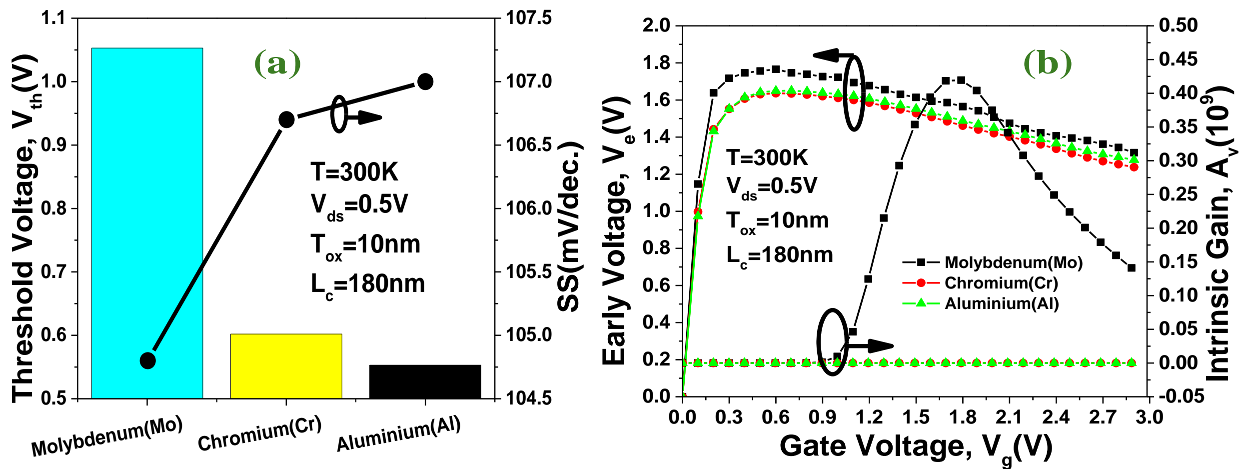

Figure 6.6: (a) The plot of threshold voltage on the left side and subthreshold swing on the right side (b) V_e - V_g characteristics on the left side and intrinsic gain on the right side for different materials of electrode used in ISFET designing at V_{ds}=0.5V, T=300K (PMS+24).

Figure 6.6 (a) reveals the plot of threshold voltage (V_{th}) on primary axis and subthreshold swing (SS) on secondary axis for different materials of gate electrode used in ISFET designing at V_{ds}=0.5V, T=300K. The enhanced threshold voltage and lower SS for Molybdenum in comparison to other materials, depicting its enhanced gate channel coupling with enhanced gate capacitance due to increased work function, also shown in Table 6.2. Figure 6.6 (b) reveals the graph of Early voltage (V_e) vs gate voltage on left side and intrinsic gain (A_v) on the right side for different materials of gate electrode at V_{ds}=0.5V, T=300K. The greater transconductance and lower output conductance for Molybdenum result in higher intrinsic gain for the device. The previous data of reference (MML05) are compared with present work in term of output voltage and sensitivity. For sake of briefing, the sensitivity and output voltage of ISFET in present work are improved than the reference literatures at pH 5, 6 (MML05) as presented in Table 6.3.

The calibration of ISFET is validated in Figure 6.7 (a) and 6.7 (b). Figure 6.7 (a) exhibits the validation of ISFET between TCAD simulation study and reference (KZH07). The drain current of this validation is -1.5V at gate length 10 um and width 100um. It is an p-type ISFET and observed with gate voltage range varying from 0 to -8V. Figure 6.7 (b) reveals the calibration study of ISFET between TCAD simulation and reference (KZP+15). The drain voltage of this validation is 0.1V at temperature of 300K. It is an n-type ISFET and observed with gate voltage range varying from

Table 6.3: Comparison of output voltage and sensitivity of this ISFET device with previously reported results

Reference	Year	Device platform	pH	V_{out}	Sensitivity
(MML05)	2005	ISFET based Microsystem	6	0.042	1.4
(MML05)	2005	Aluminium-gate-FET (ALUFET) ISFET	5	1.25	Na
(VSL+97)	1997	Diamond like carbon (DLC) gate ISFET	5	0.035	Na
(PL08)	2008	Electrolyte insulator semi-conductor (EIS) device	4	-0.4	Na
This work	Present	Silicon Nitride ISFET	6	0.051	1.7
This work	Present	Silicon Nitride ISFET	5	0.045	1.5

0 to 2.5V.

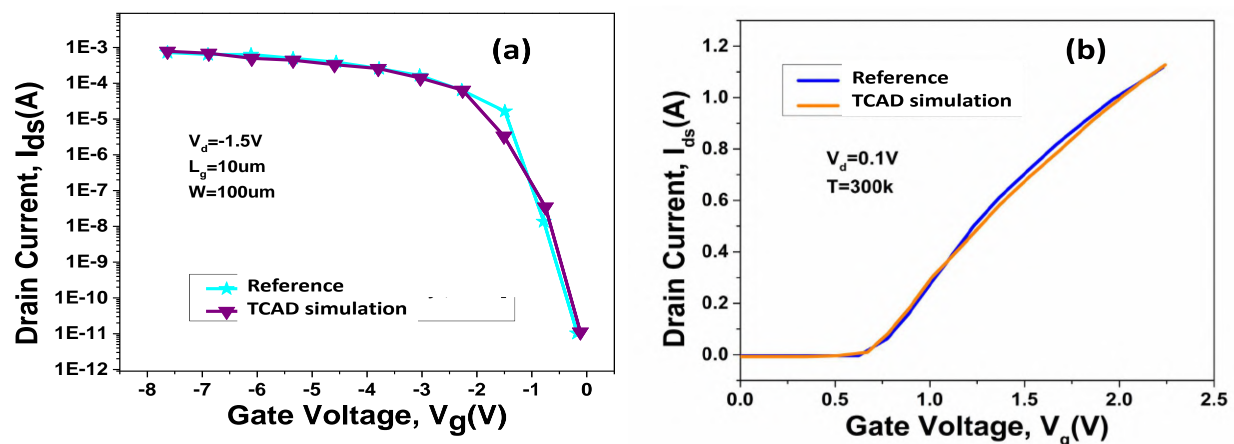

Figure 6.7: The calibration of ISFET from (a) reference (KZH07) (b) reference (KZP+15).

6.4.2 Experimental Circuit Design Result of ISFET

The Levenburg-Marquardt nonlinear extraction procedure was used to determine the parameter's extracted values, which offer a very excellent match to the recorded drift data and are contained within their physically appropriate ranges. But some of these characteristics must be determined independently through experiments for a more thorough validation of the drift model. Modern surface characterization methods, for instance, may be used to determine the ultimate thickness of the changed surface layer after exposing the pH-sensitive insulator to an electrolyte for a sizable

amount of time. The unique circuit architecture involving the ISFET were also provides the counter drift through simple adjustment of voltage and reduce flicker noise (MAR+23). A flicker noise is charge carrier trapped and released between the interface of materials.

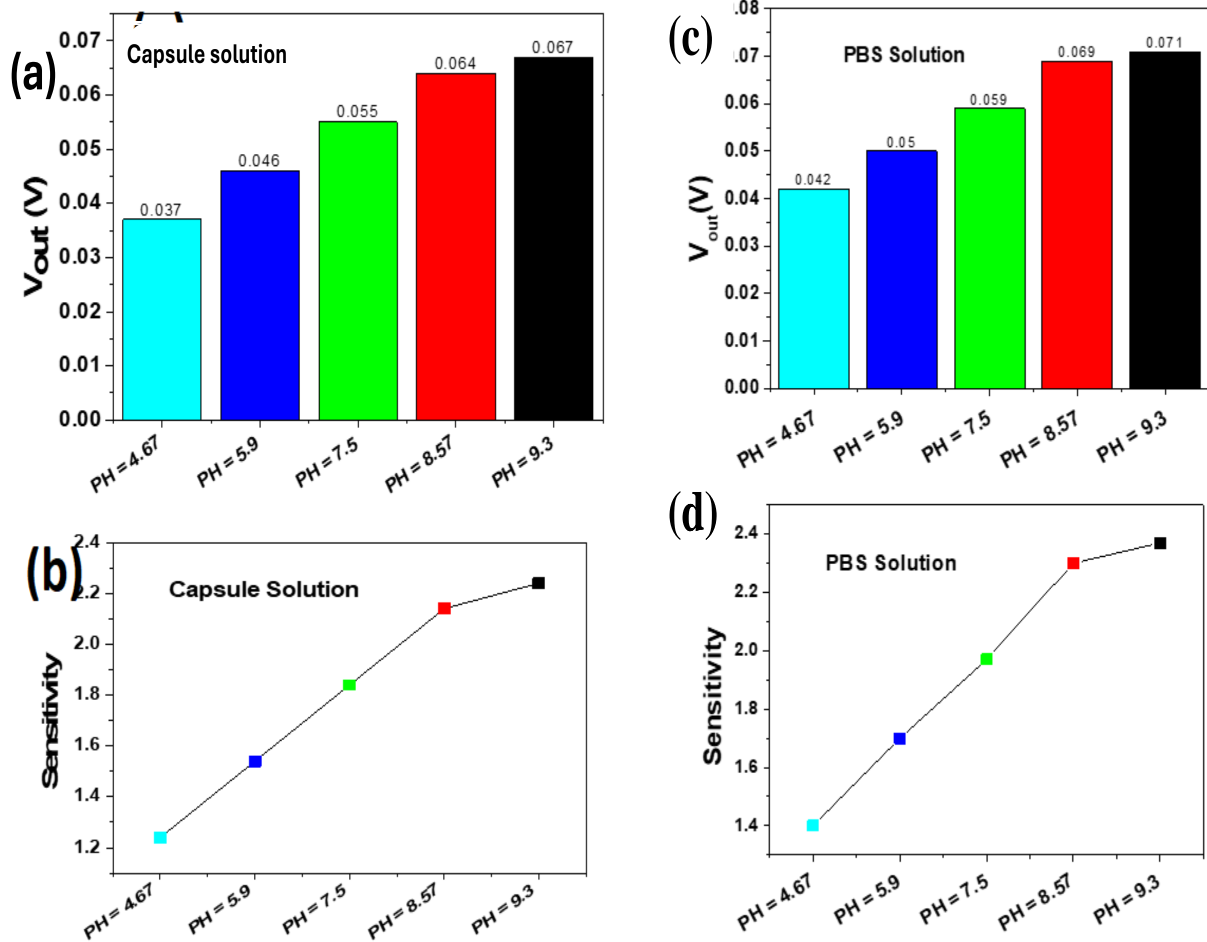

Figure 6.8: The graph of (a) pH value vs output voltage in pH capsule solution (b) Sensitivity vs pH value in pH capsule solution (c) pH value vs output voltage in PBS solution (d) Sensitivity vs pH value in PBS solution for pH based ISFET device (PMS+24).

Figure 6.8 (a) reflects the curve of pH value vs output voltage in pH capsule solution done for pH based ISFET. Voltage is improved with increasing pH value. The different value of pH capsule solution taken are pH 4.67, 5.9, 7.5, 8.57, 9.3. Figure 6.8(b) exhibits the curve of sensitivity vs pH value in pH capsule solution for pH based ISFET. The unit of sensitivity is dimensionless. In this work, a typical ISFET device's electrostatic behavior (transfer characteristics) is modeled. To provide the 9V voltage, initially convert it into 7V and 2V by using voltage divider. 2V voltage was supplied to make the current in 3mA by using 10uf capacitor and resistor. The operational amplifier is used to amplify the signal from 3mV to 1V. Drain to source current I_d vs reference gate voltage

$V_{Ref.}$ for sensing film gate oxide layer has been measured at varied pH values (YLW[+]22; NSTK21; SMS[+]19). It is noted that sensitivity is improved at higher pH value. As pH value increases, the shift in surface potential becomes larger. This results in stronger modulation of the source-drain current in the channel, enhancing the device's overall sensitivity (MPM[+]23).

Figure 6.8 (c) exhibits the variation of pH value vs output voltage in PBS (phosphate buffer saline) solution for pH based ISFET device. The applied voltage is 9V and the current is 1A in the circuit, it lead to divide the voltage by voltage divider and stored some current in 10μF capacitor to further pass the current operational amplifier. At higher pH, the concentration of hydrogen ions (H^+) decreases, which alters the surface charge at the gate insulator of the ISFET. This change shifts the threshold voltage, resulting in an increase in the output voltage of the device at higher pH value as shown in Figure 6.8 (c). The PBS solution enhanced the sensitivity at higher pH value as shown in Figure 6.8 (d), which illustrated the sensitivity of different pH value for PBS solution. ISFETs exhibit greater sensitivity to ion concentration variations at higher pH values. The circuit responds more effectively to small changes in ion concentration, enhancing the overall sensitivity of the device.

6.4.3 Effect of Variation of Sensing Layer on ISFET performance

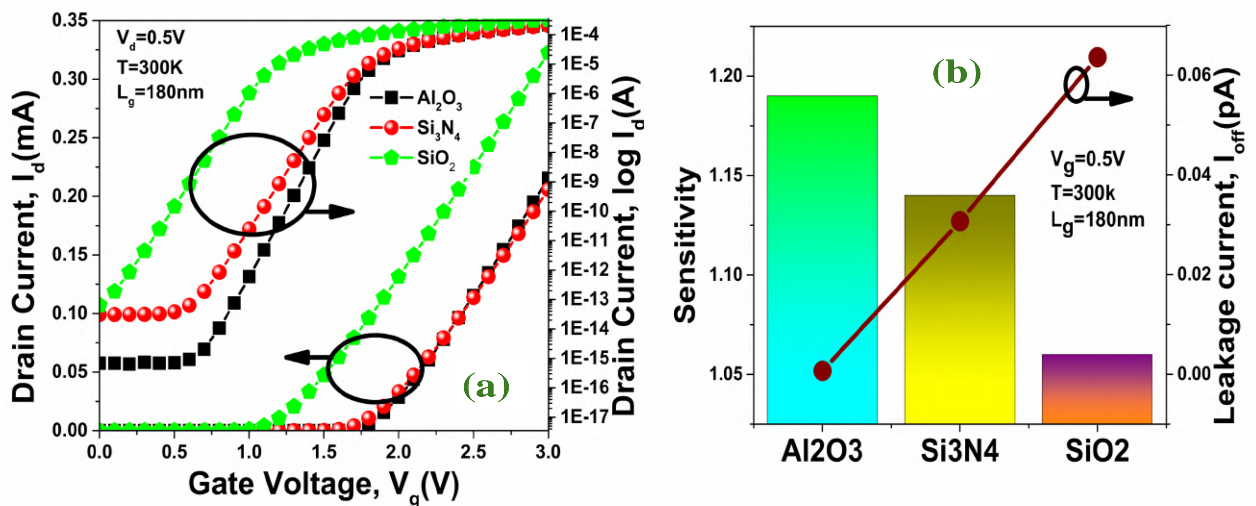

Figure 6.9: The curve of (a) drain current vs gate voltage for different sensing layer (b) sensitivity and leakage current for various sensing layer (PMS[+]24).

Firstly, we have seen analog performance of ISFET for different sensing layer to obtain better

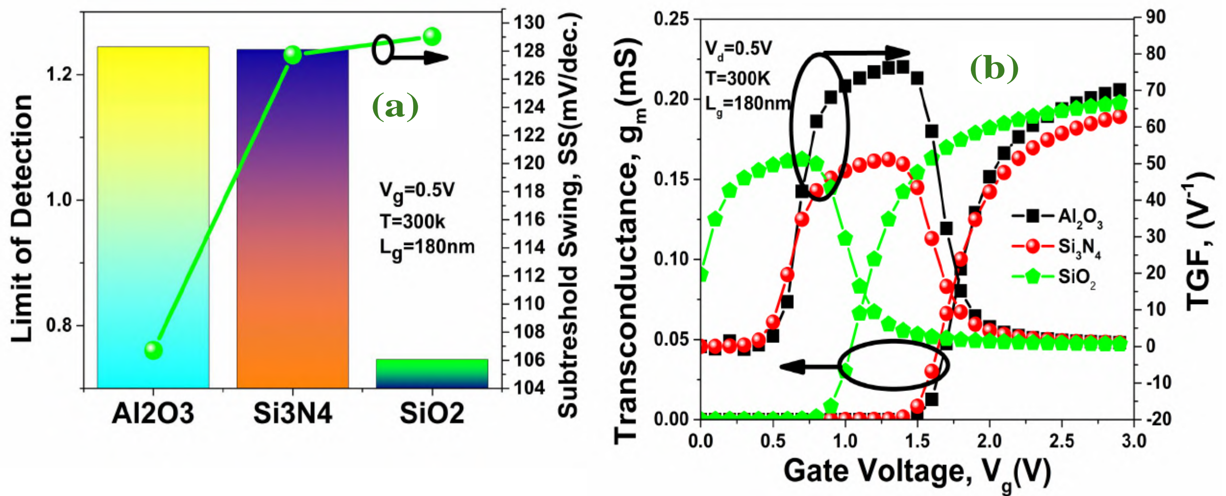

Figure 6.10: The variation of (a) limit of detection and SS for varous sensing layer (b) transconductance and device efficiency vs gate voltage (PMS+24).

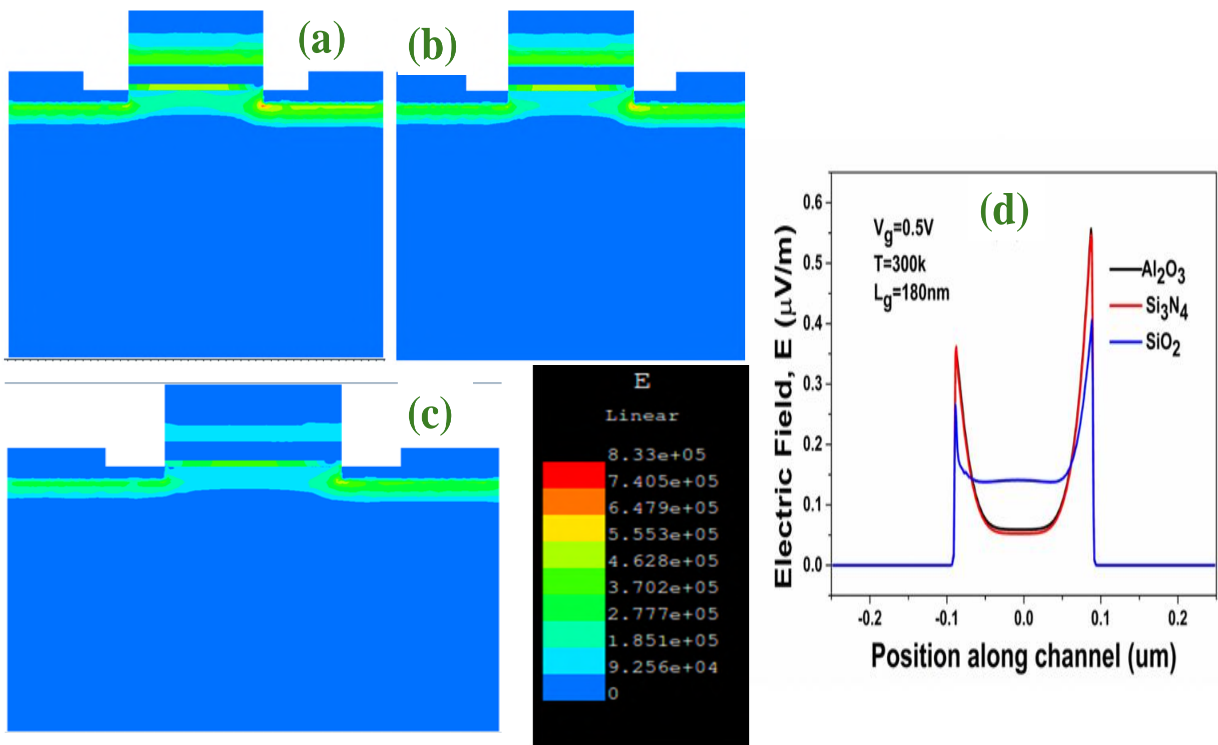

Figure 6.11: Contour plot of electric field for various sensing layer (a) Al_2O_3 (b) Si_3N_4 (c) SiO_2 (d) variation of electric field along the channel for various sensing layer (PMS+24).

results for short channel effect, SS, leakage current etc. Figure 6.9 (a) reflects the drain current (I_d) vs gate voltage (V_g) of ISFET for different sensing layer at T=300K, V_d=0.5V. The drain current of aluminium oxide is better than silicon oxide and silicon nitrite with the lower I_{off}, depicts its better sensitivity to sense any change in the analyte. Al_2O_3 offers better surface properties with higher

surface charge density due to its ability to interact more effectively with ions in the electrolyte. This results in stronger modulation of the channel and allowing for higher drain current (CR15).

Figure 6.9 (b) illustrates sensitivity and leakage current on the left side and right side of graph respectively for different sensing layers of ISFET at T=300K and V_d=0.5V. Al_2O_3 has superior sensitivity to pH changes compared to SiO_2 and Si_3N_4, which contributes to an increased ion interaction and enhanced drain current in ISFET devices. Also Al_2O_3 as sensing layer creates a stronger energy barrier at the gate. This reduces unwanted carrier leakage when the device is in off state and resulting in lower leakage current. Figure 6.10 (a) exhibit the limit of detection and SS for different sensing layer of ISFET at T=300K, V_d=0.5V. The limit of detection is higher for Al_2O_3, that showcases improved detection of any variation in the solution thus better sensitivity. The SS of Al_2O_3 is also lower as compared to other two sensing layers (PMC22b). Al_2O_3 tends to have a lower interface trap density compared to SiO_2, and Si_3N_4, resulting in reduced scattering and recombination at the interface. This further contributes to the lowering of SS.

Figure 6.10 (b) shows variation of g_m with variation in gate voltage and the result showcases that g_m of Al_2O_3 is improved as compared to SiO_2 and Si_3N_4 layer, depicting lower short channel effects and better gate controllability with Al_2O_3 as sensing layer. Al_2O_3 has a higher dielectric constant compared to SiO_2, and Si_3N_4, which results in a stronger capacitive coupling between the gate and the channel. This enhances the transconductance and making the device more sensitive to variations in ion concentrations. Effective performance of the device is also reflected by transconductance generation factor on right side of Figure 6.10 (b). TGF of the device with Al_2O_3 as sensing layer is better than as compared to other two layers. Al_2O_3 has a higher dielectric constant compared to SiO_2 and Si_3N_4. A higher dielectric constant enhances the electric field coupling between the gate and the channel, thus improving the TGF of the device and its efficiency of detecting any change in the analyte.

Figure 6.11 reflects the contour plot of electric field for (a) Al_2O_3, (b) Si_3N_4, (c) SiO_2 (d) comparison of electric field along the channel for all the three sensing layers at T=300K and V_d=0.5V. The electric field of Al_2O_3 is enhanced at drain side as compared to other layers. This leads to stronger capacitive coupling between the gate and the channel, generating a more intense electric field within the device. A stronger electric field enhances the control of the gate over the

channel, leading to better current modulation and improving the performance of the device.

6.5 Summary

This work addresses the comparative study of various materials for gate electrode of ISFET with their varying work function and subsequently a circuit is designed experimentally for ISFET based sensor. Molybdenum with work function 4.75eV shows the most improved results than the other gate electrodes like aluminium and chromium. Molybdenum has reduced the leakage current by 10^{-3} times in comparison to aluminium. It also enhanced the switching ratio, improved the sub-threshold swing along with some others enhanced analog parameters like transconductance, TGF and g_d. Theoretically, we concluded that molybdenum has proved to be an efficient material for gate electrode in the fabrication of ISFET using silicon nitride as sensing layer.

Subsequently comparative study for sensing layer of ISFET with sensing film (Al_2O_3, Si_3N_4, SiO_2) for analog and electrical performance is also investigated. The dependent parameters are evaluated with variation in sensing material such as switching ratio that is enhanced by 3.5 times and leakage current which is reduced by 63% for Al_2O_3 in comparison to SiO_2 as sensing layer in ISFET. Consequently, the findings of this research can assist engineers in designing ISFET based sensors to meet their requirements in various fields of applications.

Now, the subsequent chapter represents the conclusion of the study conducted in the thesis and offers a perspective on prospective future advancements that can be explored for further research.

Chapter 7

Summary and Future Scope

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* ∗ The summary of the research done for this thesis is given in this chapter.
* ∗ In addition, a brief discussion of specific conclusions drawn from the given findings is also included.
* ∗ The chapter then describes potential future research that could be conducted to further explore the current study.

7.1 Summary

This thesis primarily focuses on the double metal negative capacitance field-effect transistor (DM-NCFET) architecture, developed to overcome the limitations of conventional NCFETs. The DM-NCFET offers significant improvements in packing density, sub-threshold properties, off-state leakage current, and reduced manufacturing cost and complexity. This study thoroughly investigates and compares the scalability and reliability of the DM-NCFET with other designs. Additionally, methods such as double metal double gate NCFET spacer engineering have been implemented to enhance the performance of DM-NCFET with the indepth TCAD analysis along with DFT and Machine Learning based Artificial Neural Network Modelling for various applications as already discussed in detail.

Chapter 2 provides an in-depth study of DM-NCFET for analog and RF performance. The DM-NCFET (spacer) configuration demonstrates significantly improved analog performance compared to other DM-NCFET configurations. It shows a switching ratio approximately twice that of the standard DM-NCFET, a subthreshold swing reduced by 1.06 times, and a DIBL decreased by 1.21 times, indicating better short-channel effects and reduced leakage current. The DM-NCFET (spacer) structure enhances other analog properties such as transconductance (g_m), transit frequency gain (TGF), voltage gain (A_v), and early voltage (V_{ea}). Furthermore, RF applications also see improvements, with a reduced transit frequency (F_t), and better performance in terms of gate capacitance (C_{gg}), gain frequency product (GFP), and gain transit frequency product (GTFP). When examining the temperature effects on DM-NCFET (spacer) at T=300K, the results are superior compared to T=400K and T=500K, showing enhanced performance in terms of leakage current, switching ratio, and transconductance. Thus, the study suggests that DM-NCFET (spacer) at T=300K is an improved variant for analog and RF parameters compared to its conventional counterpart, making it highly suitable for high-speed IC applications. A comparative study of DM-NCFET (spacer) with different gate electrodes reveals that palladium with a work function of 5.3 eV provides better results than other materials like chromium and tungsten. Palladium shows a leakage current lower by a factor of 10^{-6} compared to chromium, a higher switching ratio, and a reduced subthreshold swing. The increasing work function (ψ) correlates with improved device performance. The electric field across the channel has also been studied for various work functions, with palladium showing an enhanced electric field compared to other gate electrodes. The DM-NCFET (spacer) design has already achieved significant advancements in accuracy, component count reduction, downsizing, cost reduction, and efficiency. Consequently, the findings of this research can assist engineers in designing nanoelectronic devices that meet these requirements.

Chapter 3 investigates the use of DM-NCFET for high-sensitivity biomolecule detection, specifically for medical diagnostics. The biosensing application of DM-NCFET has been explored for recognizing various biomolecules. The electrical performance was evaluated, showing a 0.28% shift in threshold voltage for protein compared to without a biomolecule. The sensitivity of protein detection improved by a factor of 1.167 over K=1, and the switching ratio increased by 177% compared to without a biomolecule. The surface potential at a cavity length of 10 nm was measured, and the lower limit of detection for protein improved by approximately 13% compared to without

molecules. The DM-NCFET device showed significant enhancements, indicating better sensitivity for biomolecules with a higher value of K. The proposed device demonstrated that sensitivity was greater for protein recognition (K=8) compared to various other biomolecules. Additionally, the impact of cavity length on threshold voltage (V_t), sensitivity, and the switching ratio (I_{on}/I_{off}) of the DM-NCFET biosensor was analyzed. The results revealed that sensitivity increased with the rise in cavity length, although the overall biosensor operation was slightly reduced. Thus, optimizing the cavity length to 8 nm enhances performance, making it suitable for high-sensitivity, high-speed biosensors for detecting various associated diseases.

Now, it is vital to further improve the performance of the DM-NCFET device through density functional theory (DFT) atomic modeling, as detailed in **Chapter 4**. A comparative study was conducted on the double metal double gate negative capacitance FET (DM-DGNCFET) and the single metal double gate negative capacitance FET (SM-DGNCFET). The SM-DGNCFET demonstrated superior performance in analog/RF and linearity parameters, such as reduced DIBL and subthreshold swing (SS), enhanced transconductance (g_m), improved transit frequency product (TFP) and gain frequency product (GFP), and higher second and third order transconductance (g_{m2}, g_{m3}). In the realm of atomic modeling for quantum theory advancements, density functional theory (DFT) is pivotal for determining the energy, structure, and characteristics of materials, nanosystems, and molecules. The Tran-Blaha modified Becke-Johnson (TB-mBJ) approximation provides accurate band gap calculations for crystals. A DFT study was performed on hafnia (HfO_2) based simple cubic crystals, both undoped and with 12.5% silicon doping. The results indicated that silicon doping improves the band structure by reducing the band gap to near zero and enhancing the density of states (DOS), leading to better conductivity.

Chapter 5 investigates a machine learning-based approach for accurate prediction of DM-NCFET performance. ANN-based machine learning techniques are explored to enhance variability in the ULSI domain. The Cogenda Visual TCAD simulator and Python high-level language were employed throughout the process. The computational cost is substantially reduced by using ANN-based ML, providing precise calculations and efficiency. This method aids in optimizing and designing applications for ULSI technology. The analog parameters of DM DGNCFET were studied for various oxide thicknesses, substrate thicknesses, temperatures, and ferroelectric thicknesses, revealing improvements such as lower leakage current and higher switching ratios. Specifically, at

$T = 300K$, the switching ratio increased by 3000 times compared to $T = 500K$, at $T_{Fe} = 4nm$, the switching ratio improved by 588% compared to $T_{Fe} = 8nm$, at $T_{sub} = 3nm$, the switching ratio increased by 300% compared to $T_{sub} = 7nm$, and at $T_{ox} = 0.8nm$, the switching ratio improved by 50% compared to $T_{ox} = 0.4nm$. These findings suggest that $T_{Fe} = 4nm$, $T = 300K$, $T_{ox} = 0.8nm$, and $T_{sub} = 3nm$ are the most optimal parameters for DM DGNCFET, leading to enhanced performance and suitability for various nanoelectronic devices and IC designs.

Chapter 6 delves into the experimental circuit design based on the basic structure of ion-sensitive FET (ISFET). A comparative study of materials for various gate electrification of ISFETs, focusing on their work functions and circuit design, was conducted. Molybdenum, with a work function of 4.75 eV, demonstrated superior performance compared to other materials such as aluminum and chromium. Molybdenum reduced leakage current by 10^{-3} times compared to aluminum, increased the switching ratio, decreased the subthreshold swing, and enhanced analog parameters like transconductance, TGF, and g_d. Theoretically, it was concluded that molybdenum is an efficient material for fabricating ISFETs using silicon nitride as a sensing layer with different gate electrodes. The ISFET design showed significant progress in accuracy, component count reduction, size reduction, cost efficiency, and overall performance. Additionally, a comparative study of ISFET sensing layers (Al_2O_3, Si_3N_4, SiO_2) for analog and electrical performance was conducted. The results showed that the switching ratio was enhanced by 3.5 times, and leakage current decreased by 63% for Al_2O_3 compared to other materials. A 6-pin ISFET was successfully manufactured to enhance voltage at various pH levels (4.67, 5.9, 7.5, 8.57, 9.3) as measured by a pH meter.

7.2 Future Work

The main goal of this thesis is to create a double metal NCFET device that can overcome the constraints of conventional MOSFETs. Yet all goals are largely achieved through the use of sophisticated numerical simulations. Nevertheless, given the existing work, it may be worthwhile to explore and refine the following elements as future directions.

1. It is possible to investigate the double metal NCFETs circuit behavior to optimize the suggested device for digital circuit applications such as gated logic circuits, CMOS inverters, and

SRAM.

2. Further research into other materials, such as III-V compounds, GaAs and 2D materials like graphene, may be explored. It is possible to make the suggested device suitable for high-speed and high-frequency communication devices.

3. The study conducted for this thesis have not taken interface trap charges (ITCs) into account. Therefore, in order to understand the reliability implications associated with the device, it is necessary to analyze the suggested device for both mobile and stationary ITCs.

4. In particular, noise performance measures like noise figures, cross-correlation, auto-correlation, and others are useful in examining the noise characteristics of the double metal NCFET. This investigation demonstrates how the double metal NCFET presents itself as a strong contender for the current analogue and digital design technology integration process as well as for the development of low-noise amplifier designs, thus can be explored further.

5. Various environmental based sensors such as hydrogen, oxygen and various gas sensor may also be made to measure and identify potentially dangerous substances floating in the environment.

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ORIGINAL PAPER

Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer

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Abstract

In this article, we investigated the analog performance and RF(Radio Frequency) performance of ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor (MFMIMOS) with spacer and without spacer. A proposed device MFMIMOS (spacer) with spacer enhances the ON-current (I_{on}) by 25% as compared to a without spacer device MFMIMOS, leakage current (I_{off}) reduces by almost 37%, switching ratio (I_{on}/I_{off}) enhanced by 99%, threshold voltage (V_{th}) increased by 0.29%, subthreshold swing (SS) reduced by almost 5.6% and drain induced barrier lowering (DIBL) lowed by 17.6% over MFMIMOS. We also examined the analog parameters for improving the performance of the proposed device MFMIMOS with a spacer at temperature (T) 300K such as a transconductance generation factor (TGF), transconductance (g_m), intrinsic gain (A_v), early voltage (V_{ea}), intrinsic delay (T_i), and some RF parameters gain transconductance frequency product (GTFP), cut off frequency (F_t), and gain frequency product(GFP). In the variation of temperature on MFMIMOS(spacer) we observed improved assessment at room temperature rather than other temperatures T=400K and T=500K such as threshold voltage higher by 2.4 times over temperature T=500K, switching ratio (I_{on}/I_{off}), transconductance (g_m), transconductance generation factor (TGF). All the simulated result is taken by Visual TCAD simulator with high compatibility of MFMIMOS (spacer) with spacer. Thus, the proposed device MFMIMOS (spacer) with spacer shows significantly improved analog performance than its conventional counterpart and improved performance at room temperature (T=300K) rather than other temperatures T=400K and T=500K.

Keywords MFMIMOS(spacer) · Subthreshold swing (SS) · Intrinsic Delay (T_i) · Visual TCAD · Short channel effects (SCEs)

1 Introduction

Accomplishing better speed of objective of Moore's law of transistor scaling has been the stabled at small power dissipation. The power dissipation (P) ranges with the inventory voltage(P $\tilde{V}^2$ D), with V_d generally restricted by the base subthreshold swing (SS = 60mV/dec) of an obstruction monitored Boltzmann switch [1]. As indicated by Gordon E.Moore, at almost every one of eighteen months will being twice the number of transistors in a presented unit of space [2–4] . As of late, ferroelectric (Fe-FETs) have pulled in improved consideration because of their guarantee in both memory and exchanging applications [5, 6]. Size and power consumption are the main figures of value of any advanced electronic device and the objective of past and present research endeavors is to devise forcefully scaled devices that consume ultralow power [7]. To conquer this drawback, there has been extraordinary interest in elective devices dependent on a very basic level diverse activity systems that bring about a change between the off and on condition of an electronic switch [6].

Ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor (MFMIMOS) with spacer and without spacer is

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known as NEGATIVE capacitance FETs (NCFETs) could work at a sub-60-mV/decade subthreshold swing and a high ON-current. Presently a day [7, 8], negative capacitance marvels have been experimentally shown in various frameworks:1) isolated ferroelectric images 2) ferroelectric-dielectric bilayers 3) superlattices and ferroelectric gated transistors [9, 10]. MFMIMOS did exclude the effect of channel length scaling. Additionally, the last utilizes the Landau model just in the outside-of-plane polarization part, The Landau's parameters for the FE material are $\alpha = -1.0 \times 10^{+7}$ and $\beta = 8.9 \times 10^{+8}$ [11], which is not reasonable for huge ferroelectric thicknesses [12]. In our previous works, we examined and analyzed the execution of the MFMIMOS with lengthy channels, utilizing logical displaying [13]. MFMIMOS gives a higher ON-state flow contrasted and MFMIMOS; be that as it may, we discover this not to be the case for all the ferroelectric materials. Moreover, a definite actual understanding of the conduct of the two constructions and general performance analysis is yet missing in the writing.

In this essay, we perform a broad coordinated correlation between MFMIMOS (spacer) and MFMIMOS constructions of NCFET utilizing a conservative demonstrating approach [12]. In the MFMIMOS structure, the metal layer insert between the ferroelectric layer and the gate insulator gives an equipotential side at the interior gate [14, 15], consequently empowering the management of the ferroelectric and the fundamental MOSFET as two separate circuit elements associated by a wire [16–18].

Further, ferroelectric field effect transistors (FeFETs) stand out for new era of FET devices in view of low power loss, non-volatile read ability as a memory device, and quick operation speed [19–21]. The utilization of ferroelectric material in the gatestack of MOSFET gives better resistance to the device execution since FE material shows the conduct of negative capacitance which can be seen from their charge energy bend [22–24]. So we can utilize the ferroelectric materials in numerous potential ways to reclassify the engineering of existing MOSFET structures. For that, an appropriate illustration of FE materials is HfO_2 based FE (HfO_2FE). Essentially, we know that the HfO_2 is high-k dielectric material however when it is deposited with chemical vapor deposition, its properties show the ferroelectric conduct [11].

In this article, Ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor with spacer (MFMIMOS (spacer)) at room temperature (T=300K) enhanced the performance of the device in comparison to other MFMIMOS devices such as lower subthreshold swing, lower leakage current, lower drain induced barrier lowering, low input power consumption and control over gate channel device. A new concept of a ferroelectric layer with dielectric constant (K=33.5) has been introduced. The matrix of device performance has been extracted by using visual TCAD simulator. In this MFMIMOS (spacer), the I_{off} is lying in the request for 10^{-9} A and thus has less releasing capacity from a battery point of view, which is useful for superior performance. The MFMIMOS has upgraded the sum of Ion and great depletion channel at off-state (i.e., at $V_{gs} = 0$). From this examination, we become more acquainted with the device that has phenomenal execution of analog and power amplification at the point when having an analogy and RF of simulation between MFMIMOS(spacer), MFMIMOS.

In this article, We have also observed ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor with spacer (MFMIMOS (spacer)) at temperature T=300K enhanced the performance of the device in comparison to other temperatures such as T=400K and T=500K of MFMIMOS (spacer) devices such as lower subthreshold swing, lower leakage current.

2 Device Architecture

In Fig. 1(a) shows the proposed device MFMIMOS (spacer) with spacer. There are also two schematics represented by the names as Fig. 1(a) represents metal insulator metal oxide transistor with spacer (MFMIMOS (spacer)), Fig. 1 (b) shows metal insulator metal oxide transistor without spacer (MFMIMOS).

The Body's Gate length (L_b) is 60nm, Drain's / Source's length ($L_{d/s}$) is 10nm, the Spacer1's /Spacer2's length ($L_{sp1/sp2}$) is 10nm, Body's thickness (T_b) is 50nm, Drain's/ Source's thickness ($T_{d/s}$) is 3nm, Oxide's thickness (T_{ox}) is 1nm, Ferroelectric's thickness (T_{fe}) is 1nm, Gate's / Metal2's ($T_{g/m2}$) thickness is 2nm, Insulator's thickness (T_{ins}) is 2.2nm. As depicted in Table 1, the total gate length (L_g) is 20nm for MFMIMOS (spacer) and MFMIMOS. The thickness of the total gate (T_{gt}) is 10nm MFMIMOS (spacer) and MFMIMOS. Numerous classical models are utilized to clarify various ideas in the simulation work like Shockley-Read-Hall (SRH) model briefs the trap charges presence at the point of interaction, recombination impacts. The Fermi-Dirac insights are utilized for precision in the outcomes. Arora model characterized the concentration dependent mobility.

The material of nitride is used silicon nitride (Si_3N_4). These compounds have high melting points, are extremely hard, and are usually opaque materials that have metallic lustre and high conductivities. Silicon nitride offers a number of benefits, such as high temperature capability, low friction, high wear and chemical resistance, and high electrical resistivity. It is nonmagnetic, has low specific

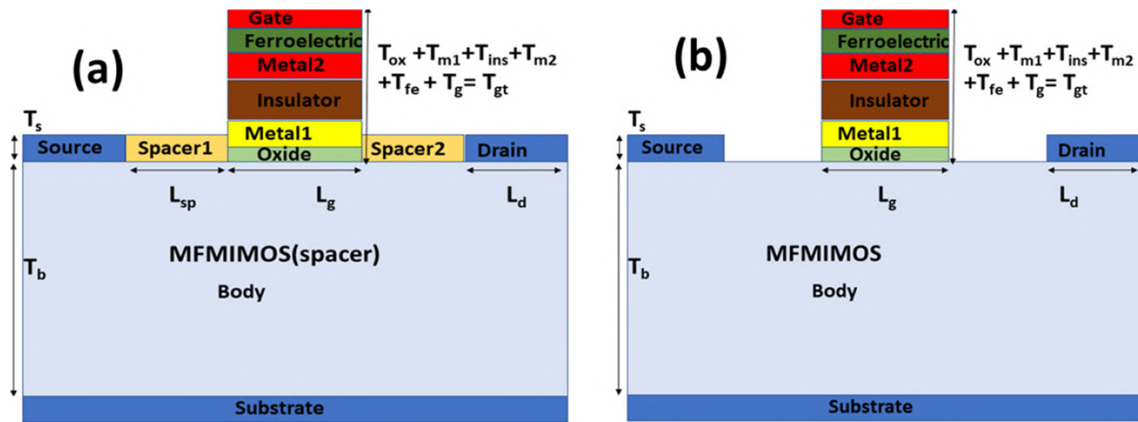


Fig. 1 The two different MFMIMOS schematics structure with using new concept of ferroelectric layer (a) MFMIMOS (spacer) with spacer (b) MFMIMOS

weight, and offers long service life. Detection of nitride is vital for human and environmental protection [25]. As shown in Fig. 1, the material of the Body is Si (silicon), the material of Drain / Source /Substrate/Gate is Al (aluminum), the material of Spacer1 /Spacer2 is Nitride, the material of Oxide is SiO_2 (silicon dioxide), Material of Ferroelectric is HfO_2FE (a new idea of a ferroelectric layer with hafnium dioxide), and material used for Metal1, Metal2 and Insulator is Au, NPoly Si and HfO_2 respectively. A proposed device MFMIMOS (spacer) involve of gate, ferroelectric, metal, insulator, metal, silicon dioxide, silicon from top to bottom. The doping concentration of Body (N_b) and silicon substrate is 1×10^{16} cm^{-3} with Uniform profile and acceptor type, the doping concentrating of Drain /Source ($N_{d/s}$) is 1×10^{20} cm^{-3} with Gaussian profile and type of donor and the doping concentration of threshold voltage (N_{vt}) is 1×10^{18} cm^{-3} with Gaussian profile and acceptor type. The work function is retained at $4.5eV$ for a gate of metal.

3 Method of Simulation

All the simulations are taken by Visual TCAD simulator. Comparison of two devices i.e MFMIMOS (spacer), and MFMIMOS have been carried out. Drain voltage, V_d (V) is fixed in the entire process at 0.3V. Gate voltage, V_{gs} is different from 0V to 3V. temperature (T) is fixed during the the first case device simulation at 300K (room temperature). In the second case variation of temperature on MFMIMOS (spacer). We have disregarded the connection among ferroelectric dipoles, which is a sensible suspicion for g_d: HfO_2 material [26, 27]. Distinctive limit conditions are applied to carry out the MFMIMOS and MFMIMOS designs. In the MFMIMOS structure, congruity of typical parts of displacement vectors is utilized at the oxide/spacer ferroelectric limits. For the MFMIMOS structure, the inside metal gate goes about as a coasting terminal. We utilize visual TCAD Multiphysics to play out every single mathematical reproduction.

Table 1 These parameters are used for the simulation of MFMIMOS (spacer)

Parameter	MFMIMOS (spacer)	MFMIMOS
Gate length (L_g)	20 nm	20 nm
Oxide Thickness (T_{ox})	1 nm	1 nm
Drain/Source length ($L_{d/s}$)	10 nm	10 nm
Drain/ Source thickness ($T_{d/s}$)	3 nm	3 nm
Body thickness (T_b)	50 nm	50 nm
Ferroelectric thickness (T_{fe})	1 nm	1 nm
Insulator thickness (T_{ins})	2.2 nm	2.2 nm
Concentration of Body (N_b)	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Concentration of Drain/ Source ($N_{d/s}$)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Concentration of threshold voltage (N_{vt})	1×10^{18} cm^{-3}	1×10^{18} cm^{-3}
Length of Spacer1/Spacer2 ($L_{sp1/sp2}$)	10nm	10nm

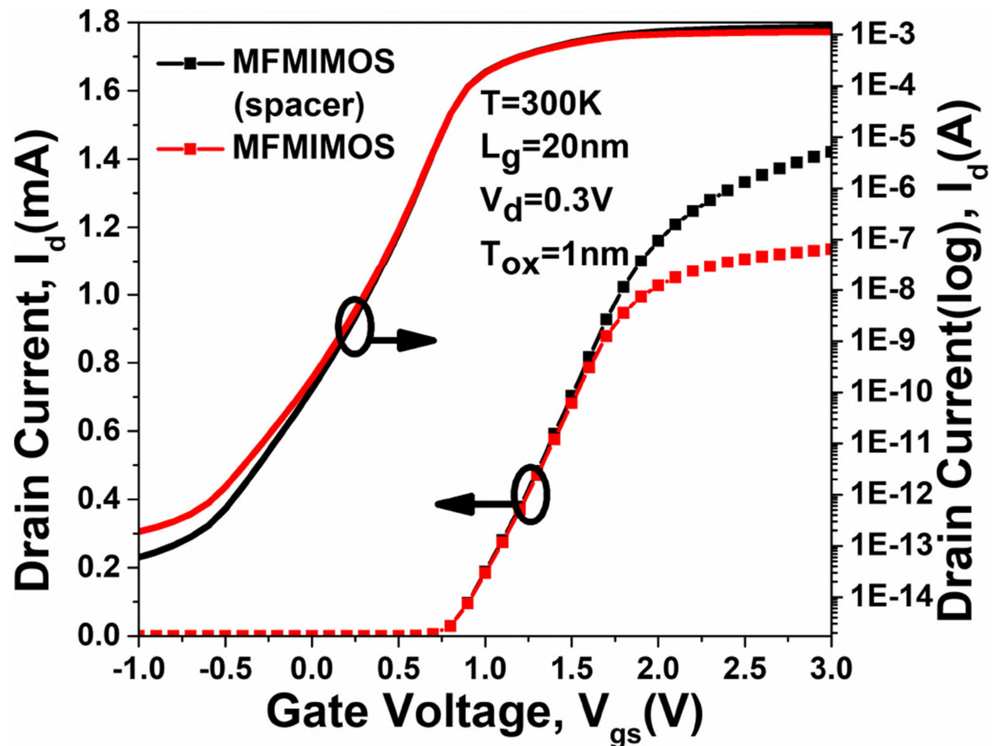


Fig. 2 The curve of drain current vs gate voltage on the left side of the graph and right side of the y-axis is log scale drain current for MFMIMOS (spacer), MFMIMOS at $V_d = 0.3V$

4 Result & Discussion

4.1 Device Scalability

Figure 2 reveals the curve between drain current, I$_d$ (A) in linear scale and drain current [28, 29], I$_d$ (A) in log scale vs gate voltage, V$_{gs}$ (V) for ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor with spacer (MFMIMOS (spacer)) at temperature T=300K, and MFMIMOS at V$_d$=0.3V, channel length, L$_g$=20nm, T=300K, and oxide thickness T$_{ox}$=1nm. It reveals thet Off state current lower for MFMIMOS (spacer) in the log drain current in negative bias also. The drain current of MFMIMOS (spacer) is better than the MFMIMOS configurations with increase in gate voltage V$_{gs}$ (V) that reflects the Superior gate coupling capacitance and reduced leakage current I$_{off}$ in the left side of the graph.

Figure 3 shows that the threshold voltage, V_{th} (V) of MFMIMOS (spacer) is enhanced than other MFMIMOS device configurations at drain voltage, V$_d$ =0.3V due to increased gate control over the channel and structure MFMIMOS (spacer) is the better shield of drain-side potential so that improved the character of the threshold voltage. The switching ratio, I_{on}/I_{off} of MFMIMOS (spacer) is higher than the other MFMIMOS structures at $L_g = 20nm$, $T_{ox} = 1nm$, $T = 300K$, and $V_d = 0.3V$, decreased leakage current, I_{off} (A), and high switching speed for MFMIMOS (spacer) structure is also obtained. The log current for measuring of V_{th} (I_{th}) is fixed $1 \times 10^{-7}A$. The formula is used for calculating V_{th} here, V_1, I_2, I_1, V_2 is log (v_2) , $\log(i_2 \times W/L)$, $\log(i_1 \times W/L)$, $\log(v_2)$. The expression $V_g = v_2 - -(I_2 - \log(I_{th})) \times (v_2 - v_1)/(I_2 - I_1)$.

4.2 Analog Analysis

In this subsection, analog performance metrics are discussed in terms of transconductance (g$_m$), transconductance generation factor (TGF), output conductance [30], early voltage (V$_{ea}$), intrinsic gain (A$_v$). Transconductance, transconductance generation factors are higher for MFMIMOS (spacer).

Figure 4 reveals that transconductance is a parameter of the shift in drain current (I$_d$) to shift in gate voltage (V$_{gs}$) at drain voltage (0.3V) at T=300K. The transconductance curve of MFMIMOS (spacer) is higher than the MFMIMOS structures. Thus, g$_m$ has taken from the curve drain current vs gate voltage that reflects enhanced gate control and lowered short channel effects (SCEs) and also increases average carrier velocity, upgraded electron mobility with increase transconductance [31].

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} \tag{1}$$

$$TGF = \frac{\partial g_{\mathrm{m}}}{\partial I_{\mathrm{d}}} \tag{2}$$

$$g_{\mathrm{d}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{d}}} \tag{3}$$

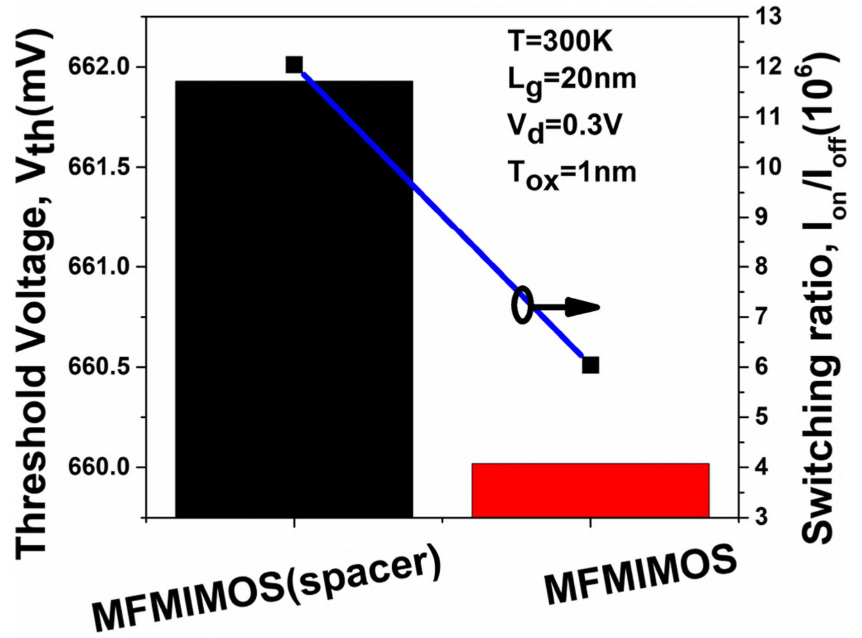


Fig. 3 The bar graph indicates for two configurations at V_d=0.3V (a) threshold voltage, V_{th} (V) (b) switching ratio

$$V_{\mathrm{ea}} = \frac{\partial I_{\mathrm{d}}}{\partial g_{\mathrm{d}}} \tag{4}$$

$$A_{\mathrm{v}} = \frac{\partial g_{\mathrm{m}}}{\partial g_{\mathrm{d}}} \tag{5}$$

Transconductance generation factor (TGF) is gain generated per unit power loss. TGF of MFMIMOS (spacer) is increased than MFMIMOS configurations, close to ideally 50V^{-1} and subthreshold swing ideally close to 60mV/decade. The device operation at low supply voltage performs more efficiency for a high value of TGF. (b) reflects the output characteristics for different drain current at constant gate voltage= 0.7V it gives us better than other gate voltage such as V_{gs}=0.75V and 0.8V. The changes of TGF occur in the subthreshold region. The region for high TGF and g_m due to high drain current. Figure 5 represents the graph of drain current, I_d (A) and output conductance, g_d (nS) vs drain voltage, V_d (V) at gate voltage V_{gs} (0.8) oxide thickness 1nm and channel length 20nm. Output conductance is the driving capacity of the device as characterized in (3) [32] mirrors the locale of device activity.

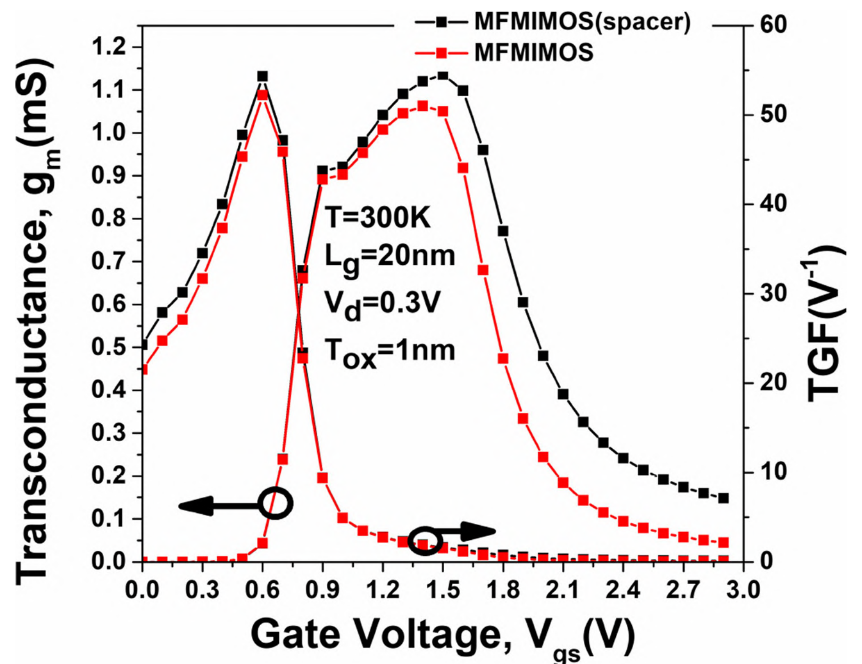


Fig. 4 The curve of different structures at V_d=0.3V (a) transconductance and gate voltage (b) transconductance generation factor vs gate voltage

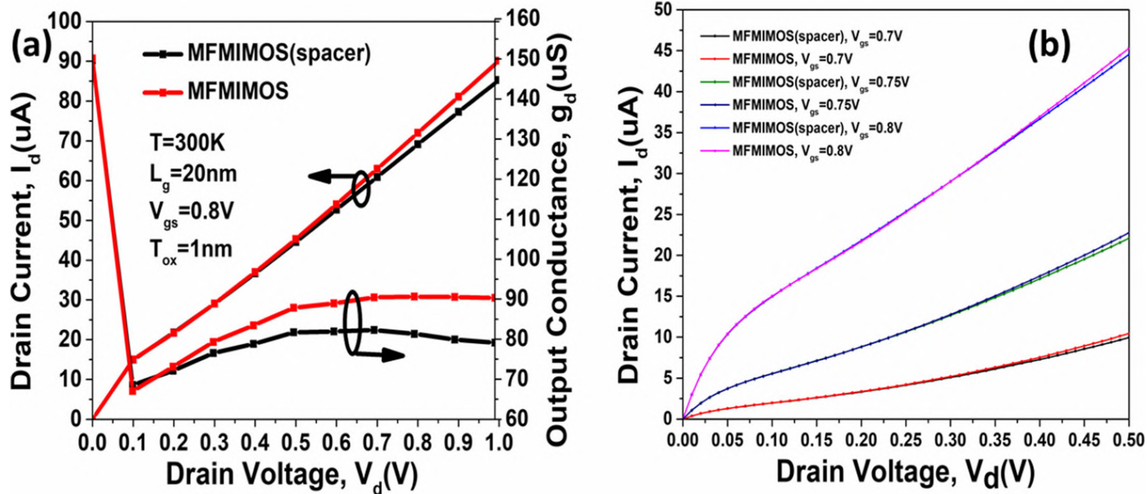


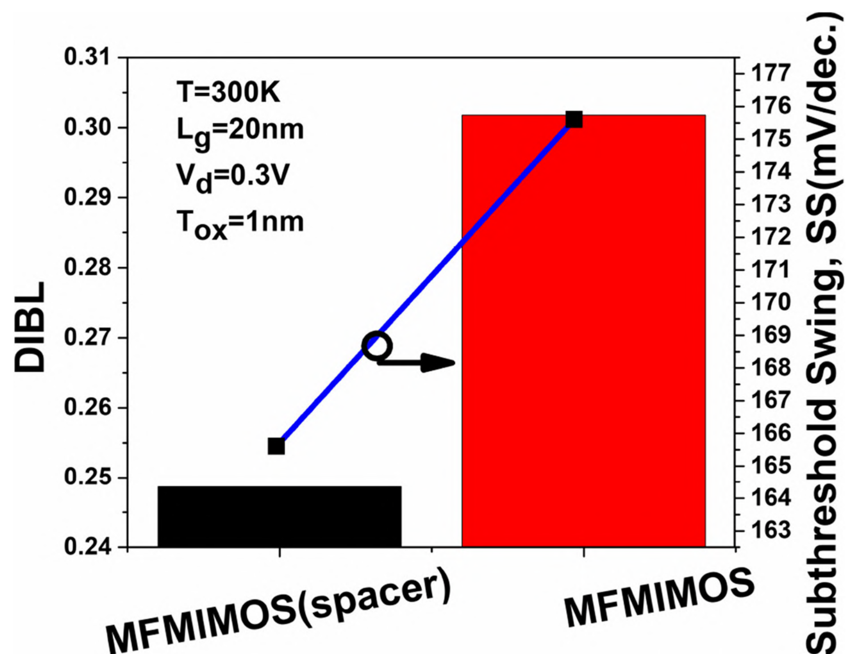
Fig. 5 (a)The curve of drain current and output conductance vs drain current for different structures at V_{gs}=0.8V.(b) Plot for various constant gate voltage

At first, a high output conductance in the linear region is observed with increasing drain voltage beyond pinch-off voltage owing to drain induced barrier lowering (DIBL) as well as channel length modulation (CLM) [33]. The g_d twist of MFMIMOS (spacer) is lower than MFMIMOS that shows upgraded gate controllability and stifle short direct impacts as portrayed in Fig. 5 that reflects improved output obstruction.

Figure 6 shows that the bar graph of drain induced barrier lowering (DIBL) for a different configuration at T=300K. It is a short channel effect (SCEs), the length of the channel decreasing means electrons easily move from source to drain. DIBL of MFMIMOS (spacer) is lower than MFMIMOS structure that reflects reduced leakage current, improved SCEs. Subthreshold swing (SS) is also a vital parameter of SCEs, ideally SS 60mV/decade. SS of MFMIMOS (spacer) is lowering than MFMIMOS that reflect enhanced gate coupling capacitance with high permittivity (K), increase gate control over the channel.

Figure 7(a) reveals that the curve of early voltage and intrinsic gain vs gate voltage for different configurations at V_d=0.8, oxide thickness 1nm, channel length 20nm [34–37]. These formulae are evaluated by using (4) and (5). The proposed device MFMIMOS (spacer) metrics are higher

Fig. 6 Graph of different structures at V_d=0.3V (a) drain induced barrier lowering, DIBL in the left side (b) Subthreshold swing in right side



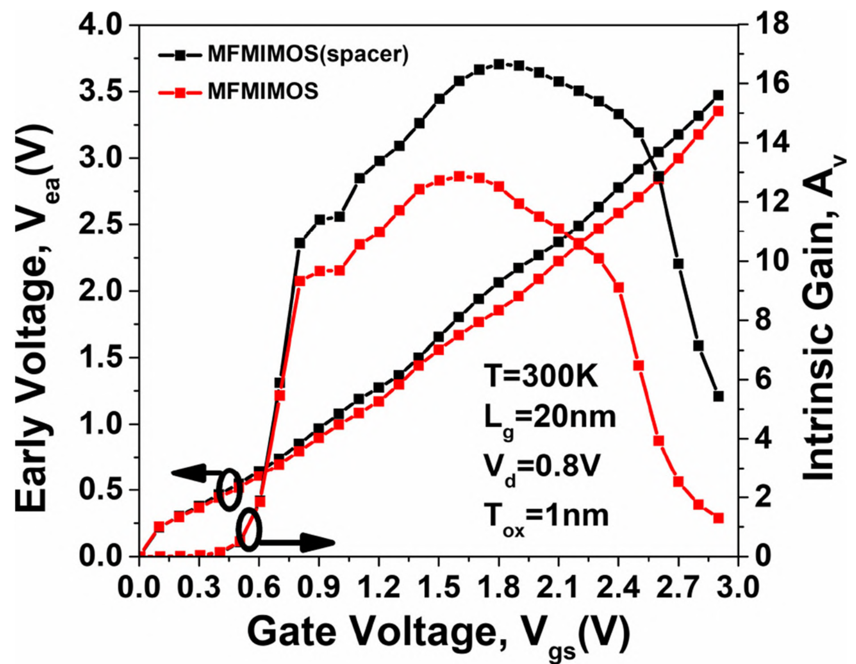


Fig. 7 Graph for different structures at V_d=0.8v (a) Variation of early voltage and intrinsic gain vs gate voltage at T=300K

than other conventional devices that indicate short channel effects (SCEs). The higher value of intrinsic gain is obtained from the high value of transconductance, and lower output conductance as depicted in Table 2.

4.3 RF Analysis

In the RF (Radio Frequency) application, the parameter of RF is gate capacitance (C_{gg}), gate charge (Q_g), unity gain cutoff frequency (F_t), gain frequency product (GFP), and gain transconductance frequency product (GTFP). etc. Fig. 8(a). represents the variation of gate capacitance, C_{gg} (F/um) vs gate voltage for all configurations at drain voltage (0.3V), channel length (20nm), and oxide thickness (1nm). The gate capacitance curve of MFMIMOS (spacer) is higher than other structures that reflect an enhanced number of stored charges.

Figure 8 indicates that gate capacitance and cutoff frequency [21, 29] of MFMIMOS (spacer) is lower than MFMIMOS configuration that reveals enhanced gate capacitance and increased transconductance as depicted in (6). Intrinsic delay of MFMIMOS (spacer) is lower than other structures by using the (7) on the right side of the graph [32]. It is the time interval carried by the device to gives output after applying input that reflects less input power consumption [32–39]. The gate charge of MFMIMOS (spacer) is higher than other structures that reflects high gate capacitance.

$$F_{\mathrm{t}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gg}})} \tag{6}$$

$$T_{\mathrm{i}} = \frac{C_{\mathrm{gg}} \times V_{\mathrm{d}}}{(I_{\mathrm{on}})} \tag{7}$$

$$GFP = \left(\frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}\right) \times F_{\mathrm{t}} \tag{8}$$

$$GTFP = \left(\frac{g_m}{g_d}\right) \times \left(\frac{g_m}{I_d}\right) \times F_t \tag{9}$$

Figure 9 shows that the electric field I contour Electric field contour with MFMIMOS (spacer) from 0 to 8.661E+06 and MFMIMOS from 0 to 8.404E+06 at $V_d = 0.3V$, T=300K, channel length 20nm, oxide thickness 1nm.

Table 2 Parameter and value of leakage current, SS, DIBL for different configuration, T_{ox}=1nm, T=300K and L_g=20nm

Parameter	MFMIMOS (spacer)	MFMIMOS
I_{on} (A)	0.001421	0.001135
I_{off} (A)(10^{10})	1.18	1.88
DIBL	0.248673	0.30171177
SS (mV/dec)	165.607	175.606
I_{on}/I_{off}(10^6)	12.0424	6.0372
V_{th}(mV)	661.929	660.0196

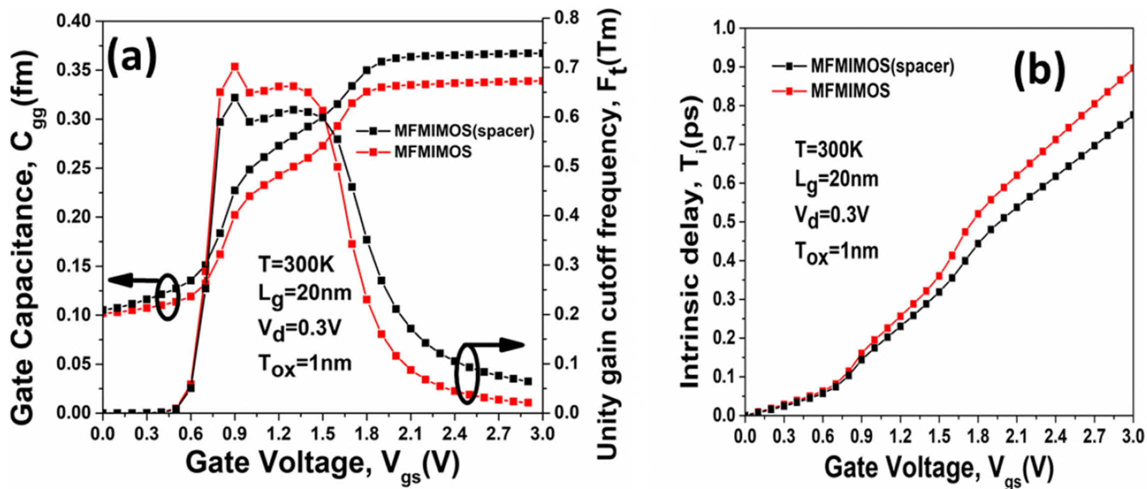


Fig. 8 Variation for different structures with V_d=0.3V and L_g = 1GHz (a) Curve of gate capacitance vs gate voltage and Curve of cutoff frequency vs gate voltage (b) Curve of intrinsic delay vs gate voltage at T=300K

The electric field is high in the area of contour from gate to drain. Area of electric field contour is higher than other structure that reflects reduced leakage current I_{off}.

Figure 10 reflects the graph for different structures at V_d=0.8 (a) Variation of gain frequency product and gain transconductance frequency gain product vs gate voltage at T=300K. Gain frequency Product is a fundamental boundary utilized in high-recurrence applications, as determined in (8) [40, 41]. It is seen from Fig. 10, GFP increments as the gate voltage higher and afterward accomplishes a greatest top prior to tumbling to a consistent worth in the saturation locale. MFMIMOS (spacer) design records the most elevated worth of GFP because of the further developed worth of output transconductance and transconductance with an insignificant abatement in cut-off frequency. GTFP most noteworthy worth is acquired for MFMIMOS (spacer) structure because of the upgraded worth of g_m, TGF, and decreased worth of g_d with practically comparable F_t. In this manner, MFMIMOS (spacer) is the best appropriate design as far as speed, transconductance, and gain.

4.4 Effect of temperature on MFMIMOS (spacer)

In this section, we observed the variation of temperature on MFMIMOS (spacer) such as T=300K, 400K and 500K drain voltage 0.3V, gate length 20nm and oxide thickness 1nm. In Fig. 11 exhibits graph for different temperature such that T=300K, 400K and 500K at V_d=0.3 (a) Drain current and log drain current vs gate voltage for MFMIMOS (spacer). The drain current of MFMIMOS (spacer) at temperature T=300K is higher than the other temperature with increase in gate voltage V_{gs} (V) that reflects the improved gate coupling capacitance and less leakage current

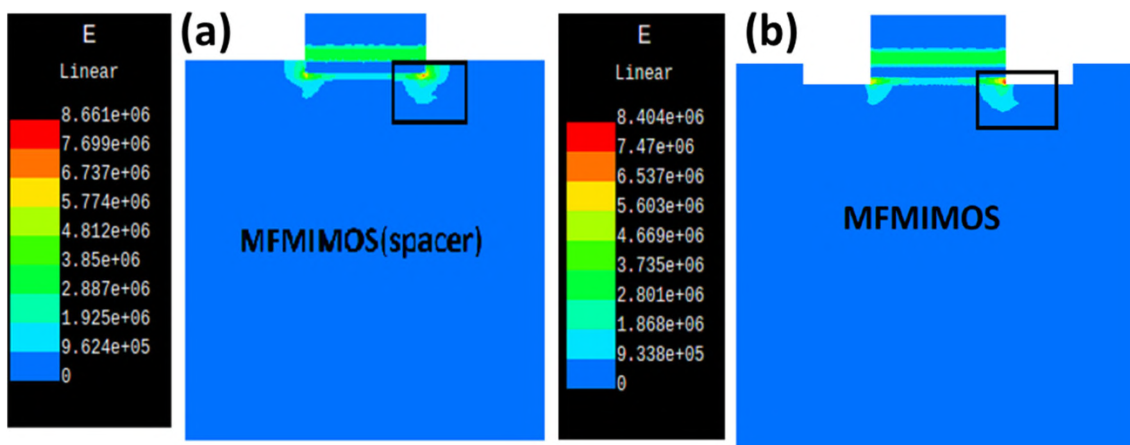


Fig. 9 Electric field contour with MFMIMOS (spacer) from 0 to 8.661E+06 and MFMIMOS from 0 to 8.404E+06 at V_d=0.3V and T=300K. (a) MFMIMOS (spacer) (b) MFMIMOS

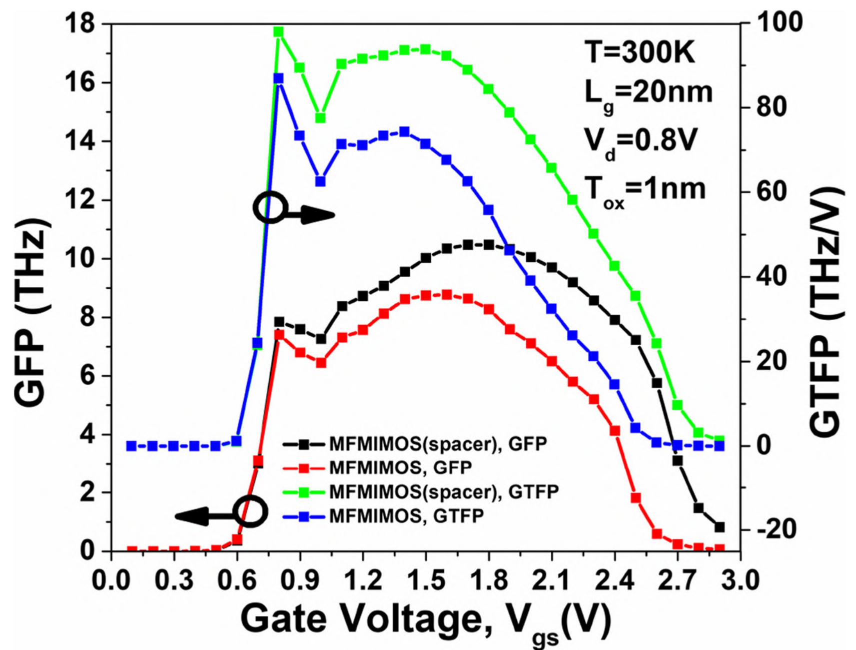


Fig. 10 Graph for different structures at V_d=0.8v (a) Variation of gain frequency product and gain transconductance frequency gain product vs gate voltage at T=300K

I_{off} in the left side of the graph. Figure 12 shows that the threshold voltage, V_{th} (V) of MFMIMOS (spacer) at temperature T=300K is enhanced than other temperature T=400K and T=500K configurations at drain voltage, V_d =0.3V due to increased gate control over the channel and structure MFMIMOS (spacer) at temperature T=300K is the better shield of drain-side potential so that improved the character of the threshold voltage. The switching ratio, I_{on}/I_{off} of MFMIMOS (spacer) temperature T=300K is higher than the other temperature T=400K and T=500K structures at L_g=20nm, T_{ox}=1nm, and V_d=0.3V, decreased leakage current, I_{off} (A), and high switching speed for MFMIMOS (spacer) structure is also obtained as depicted in Table 3.

Figure 13 reveals that transconductance is a parameter of the shift in drain current (I_d) to shift in gate voltage (V_{gs}) at drain voltage (0.3V). The transconductance curve of MFMIMOS (spacer) at temperature T=300K is higher than other temperature T=400K and T=500K structures. Thus, g_m has taken from the curve drain current vs gate voltage that reflects enhanced gate control and lowered short channel effects (SCEs) and also increases average carrier velocity, upgraded electron mobility with increase transconductance [31]. Transconductance generation factor

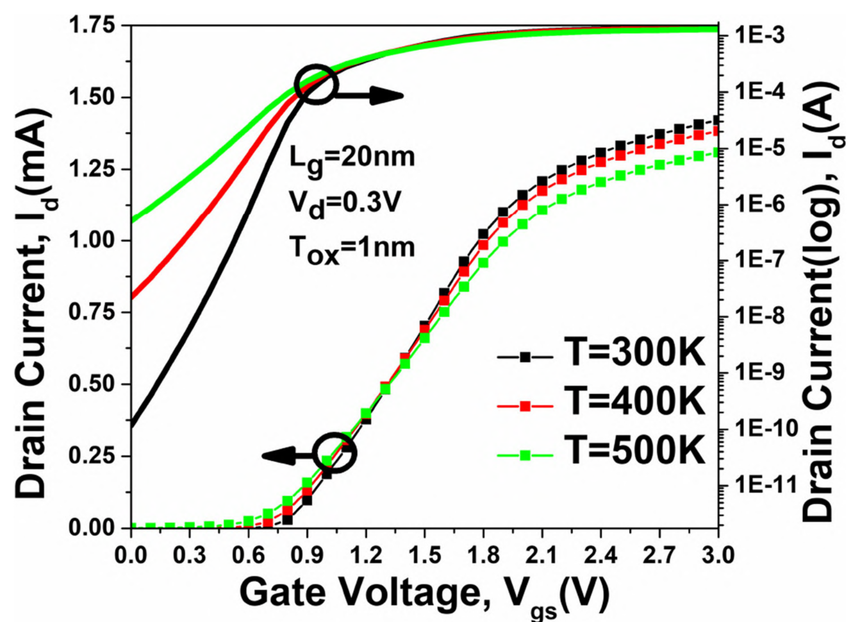


Fig. 11 Graph for different temperature such that T=300K, 400K and 500K at V_d=0.3 (a) Drain current and log drain current vs gate voltage for MFMIMOS (spacer)

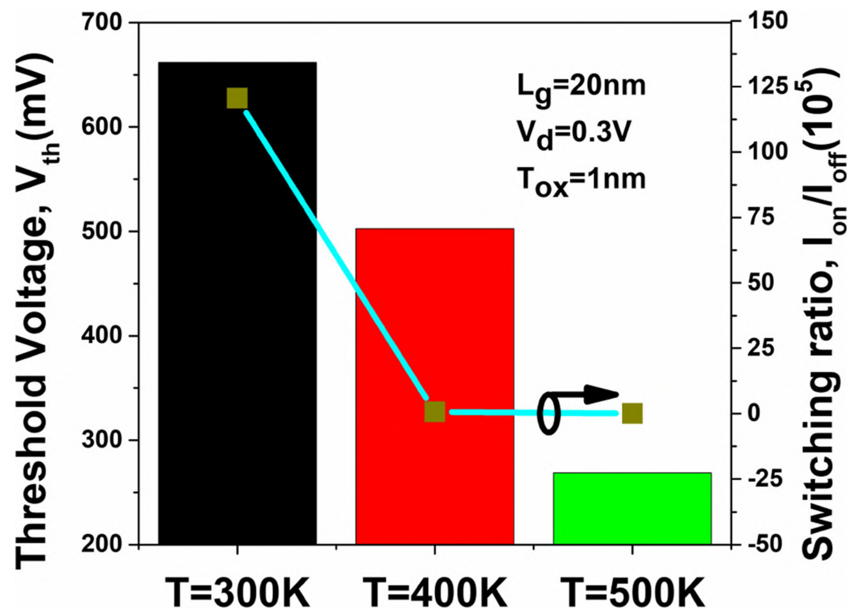


Fig. 12 Graph for different temperature such that T=300K, 400K and 500K at V_d=0.3 (a) threshold voltage and switching ratio vs gate voltage for MFMIMOS (spacer)

Table 3 Parameter and value of leakage current for different temperature at MFMIMOS (spacer) T_{ox}=1nm, and L_g=20nm

Parameter	T=300K	T=400K	T=500K
I_{on} (A)	0.001421	0.001383	0.001309
I_{off} (A)(10^{10})	1.18	220	5040
$I_{on}/I_{off}(10^6)$	12.0424	00.0629	0.002597
$V_{th}(mV)$	661.929	502.534	268.78

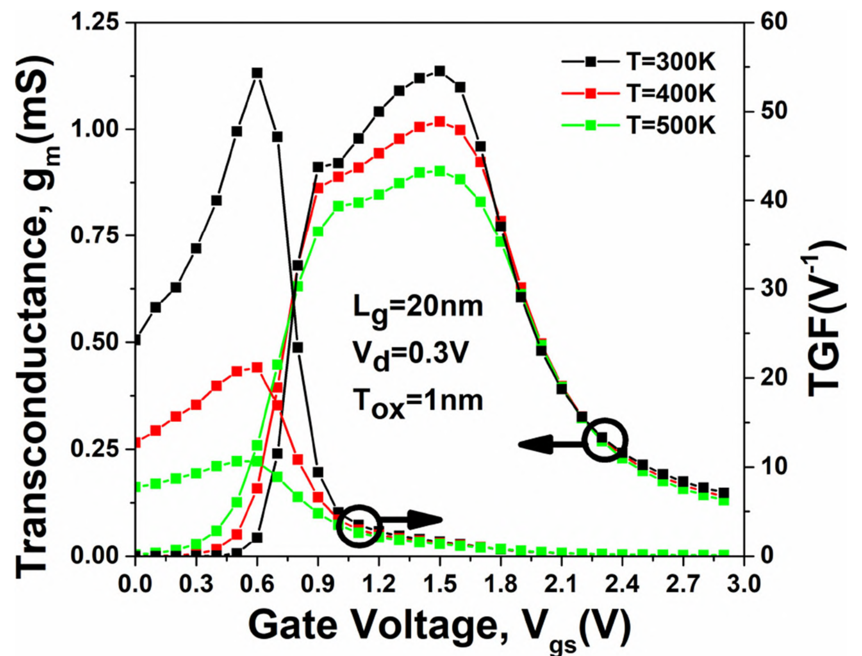


Fig. 13 Graph for different temperature such that T=300K, 400K and 500K at V_d=0.3 (a) transconductance and transconductance generation factor vs gate voltage for MFMIMOS (spacer)

(TGF) is gain generated per unit power loss. TGF of MFMIMOS (spacer) at temperature T=300K is increased than temperature T=400K and T=500K configurations, close to ideally $50V^{-1}$ and subthreshold swing ideally close to 60mV/decade. The device operation at less supply voltage performs high efficiency for a high value of TGF. The changes of TGF occur in the subthreshold region. The region for high TGF and g_m due to high drain current.

5 Conclusion

In this work, we proposed ferroelectric layer improved Field Effect Transistor device that is metal ferroelectric metal insulator metal oxide transistor (MFMIMOS) with spacer and without spacer. All the simulations are brought by a visual TCAD simulator. MFMIMOS (spacer) indicates significantly improved analog results than MFMIMOS configurations such as switching ratio increased by around 2 times of MFMIMOS, subthreshold swing reduced by 1.06 times of MFMIMOS, DIBL decreased by 1.21 times of MFMIMOS that parameters reflect a short channel effect and reduced leakage current. The structure of MFMIMOS (spacer) enhanced the properties of other analog application such as g_m, TGF, A_v, and V_{ea} increases, respectively. Furthermore. RF application is also improved such as F_t reduces, C_{gg}, GFP and GTFP. In the case of effect on temperature of MFMIMOS (spacer) at T=300K reveals more improved result than other temperature such that T=400K and T=500K. At temperature T=300K enhanced performance such as leakage current, switching ratio, transconductance TGF. Thus, this article indicates MFMIMOS (spacer) at temperature T=300K can be considered as an improved variant of analog and RF parameters in analogy to its conventional counterpart. The device has a wide variety of applications to high speed ICs.

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Author Contributions All authors added to the study's understanding and design.

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Availability of Data & Material The creators expressed above have every one of the suitable data associated with this examination work and will be dedicated to uncovering that they will be addressed to do as such future.

Declarations

The authors have found all the Moral Standards and will intended to follow them in the future.

Consent for Publication Since the related research document is created on the 'no-life science journal.' Therefore, 'Non Applicable' at this point. Still, the authors have turned over all journal guidelines and consent to the agencies for additional processing.

Conflict of Interests The writers broadcast that they have no known dispute of individual connections or interests that might have arisen to impact the work depicted in this article.

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Detection of biomolecules in dielectric modulated double metal below ferroelectric layer FET with improved sensitivity

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ABSTRACT

In this work, we examined the double metal below ferroelectric layer FET that is double metal below negative capacitance field-effect transistor (DM-below-NCFET) for biosensing application and change in nanocavity gap with biomolecules as protein, ChO_x (cholesterol oxidase), streptavidin, and uricase. For measuring the electrical characteristic and neutral biosensing such as threshold voltage, switching ratio (I_{on}/I_{off}) of the device which is higher than one without molecules by 1.52 times, sensitivity of protein enhanced by 1.11 over without biomolecule, limit of detection of protein is higher by 1.012 times over without molecule, shift in potential have been researched for cavity length 10 nm. The biosensor indicated improved sensitivity for biomolecules with the rise in their dielectric parameter. Moreover, modulation of the length of the gap of cavity was too examined, exposing that its increment (from 8 to 12 nm) altogether upgraded the sensitivity of the proposed biosensor. Visual TCAD (Technology Computer-Aided Design) software is used for simulating all results. In general, the consequences of this examination represent that such DM-below-NCFET biosensors can display extreme sensitivity (1.11) at small drain voltage (0.4 V), empowering their utilization for biosensor applications to analyze different infections which involve low power, extreme density, and enhanced speed.

1 Introduction

The new COVID-19 epidemic has once more gained a bleeding edge on the impact of microelectronic biosensors in recognition of biomolecules and biological fighting specialists. The applications might be discovered by electronic biosensors uninterruptedly observing inflight biomolecules in conveyance contexts like airplanes and metro rail and midway cooled structures like hospitals, schools, clinics, and so forth. Consequently, the requirement of great importance is to plan and foster quick and precise biosensors. Biosensors utilize chemical responses to distinguish the biochemical mixtures like antibodies,

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enzymes, nucleic acids, proteins, and so forth. So they are broadly utilized in numerous applications like checking of infections, food investigation, crime detection, ecological field observing, and for the investigation of biomolecules cooperation [1, 2].

Various strategies have been created for recognizing of biomolecules such that the chemical connected immunosorbent measure [3], for Alzheimer's illness, coronary vein infection, and ovarian cancer. In any case, numerous of these methodologies are convoluted and tedious caused by the necessity for modeling procedures [4]. Field-effect transistor (FET) constructed biosensors have drawn in much consideration from late years inferable from their great versatility, extreme sensitivity, quick electrical identification, small force utilization, straight electrical display, and minimal expense large-scale manufacturing in correlation with different strategies, for example, surface plasmon resonance [5], microcantilevers [5], and varieties of fluorescence devices [6, 7]. Minimal expense, profoundly touchy, dependable, easy to use, and speedy symptomatic biosensing gadgets are fundamental for various organic and biomedical applications [8]. For biosensing functions, the main component of key for a MOSFET is sensitivity [9].

Ferroelectric FETs (Fe-FETs) have pulled in improved consideration because of their guarantee in both memory and exchanging applications [10]. Size and power consumption are the main figures of value of any advanced electronic device and the objective of past and present research endeavors is to devise forcefully scaled devices that consume ultralow power [11]. The effect of channel length scaling was excluded by NCFET. Additionally, the last utilizes the Landau model just in the outside-of-plane polarization part, which is not reasonable for huge ferroelectric thicknesses [12]. In our previous works, we examined and analyzed the execution of the double NCFETs with lengthy channels, utilizing logical displaying [13]. The Landau's parameters for the FE material is $\alpha = -1.0 \times 10^{+7}$ and $\beta = 8.9 \times 10^{+8}$ [14]. Double metal below negative capacitance FET (DM-below-NCFET) for protein biomolecule gives a higher ON-state flow contrasted to other biomolecule; be that as it may, we discover this not to be the case for all the ferroelectric materials. Moreover, a definite actual understanding of the conduct of the dual constructions and general execution analysis is yet disappeared in the writing [15–20].

In this article, double metal below negative capacitance FETs (DM-below-NCFETs) for protein biomolecule enhanced the performance of the device in comparison with uricase, streptavidin, ChO_x (Cholesterol oxidase), without biomolecules such as higher sensitivity, lower leakage current, low input power consumption, and control over gate channel device. A new concept of a ferroelectric layer with a dielectric constant (K = 33.5) has been introduced. The matrix of device performance has been extracted by using visual TCAD (Technology Computer-Aided Design) software. In this DM-below-NCFET, the I_{off} is lying in the request for 10^{-12} A and thus has less releasing capacity from a battery point of view, which is useful for superior performance. The DM-below-NCFET has upgraded the sum of I_{on} and great depletion channel at off-state (i.e., at V_{gs} = 0). From this examination, we become more acquainted with the device that has phenomenal execution of analog and power amplification at the point when having an analogy and electrical stimulation between various biomolecules.

A proposed device has been utilized as a biosensor for detecting different biomolecules. The main use of the device is to comprehend different biomolecules, which is done when biomolecule ties to the gate of the device and modifies its surface charge. In the proposed DM-below-NCFET device (biosensor), the device's channel limit gets improved with the electrical curve of biomolecules from which they can be distinguished. In the traditional MOSFET, the current through channel flow when the gate voltage transcends the threshold voltage (V_{TH}) [2, 21, 22]. With a general high doping concentration, the DM-below-NCFET acts as a resistor. At the point when the quantity of charged analyte changes on the sensor surface, the conductance of the resistor changes likewise. Following recently talked about detecting instruments, the charges from analytes influence the conductivity of the device channel due to attractive or repulsion electrostatic force. All in all, the level of depletion inside channel changes because of charges from analytes in the arrangement [23].

2 Structure of device and method of simulation

Figure 1a reveals the structure of Double Metal below ferroelectric layer FET that is double metal below negative capacitance FET and Fig. 1b represent the spacer has biomolecules. For immobilization of biomolecules in the area of Bio1 and Bio2, the region between area source and gate (L_{bio1}) or drain and gate (L_{bio2}) is the same as cavity gap. Since the determining region is the most important characteristic and behavior of DM-below-NCFET, rhe channel's length (L_c) is 20 nm, body's length (L_b) is 60 nm, drain's/-source's length ($L_{d/s}$) is 10 nm, the Bio1/Bio2 length ($L_{bio1/bio2}$) is 10 nm, body's thickness (T_b) is 50 nm, drain's/source's thickness ($T_{d/s}$) is 3 nm, oxide's thickness (T_o) is 1 nm, Ferroelectric's thickness (T_f) is 1 nm, Metal1's (T_{m1}) thickness is 2nm, insulator's thickness (T_i) is 2.3 nm, Metal2's thickness (T_{m2}) is 1.7 nm, the thickness of Bio1/Bio2 is 2 nm, and the thickness of gate is 2 nm. The total gate thickness (T_{gt}) is the addition of thickness oxide, Metal2, insulator, Metal1, ferroelectric layer, and gate. The material of the body is Si (silicon), the material of drain/source/substrate/gate is Al (aluminum), the material of Insulator is nitrite, the material of oxide is SiO_2 (silicon dioxide), the material of Metal1 is Au and Material of ferroelectric is HfO_{2FE} (an innovative idea of a ferroelectric layer with hafnium dioxide). A proposed device DM-below-NCFET contains metal, insulator, metal, ferroelectric, intermediate gate, silicon dioxide, and silicon from top to bottom. The doping concentration of body (N_b) is 1×10^{16} cm^{-3} with uniform profile and acceptor type, the doping concentrating of drain/source ($N_{d/s}$) is 1×10^{20} cm^{-3} with Gaussian profile and type of donor and the doping concentration of threshold voltage (N_{vt}) is 1×10^{18} cm^{-3} with Gaussian profile and acceptor type. The work function is very high kept at 5.4 eV for a Metal1 gate.

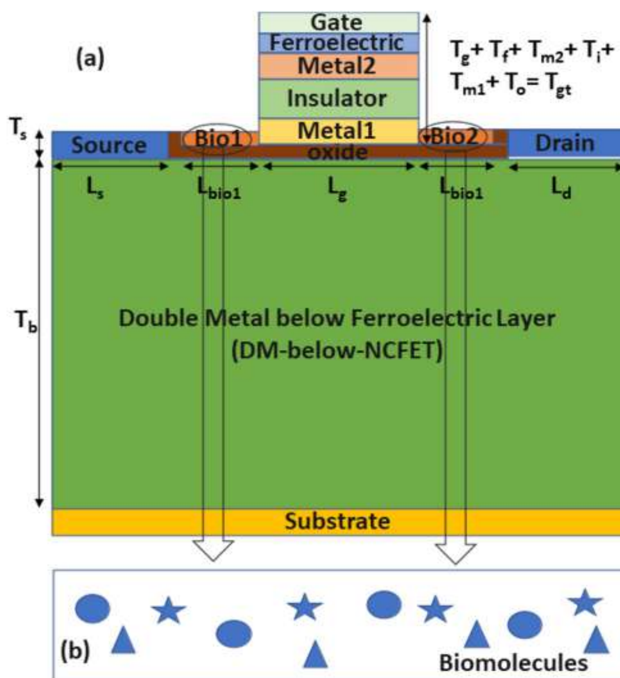

Fig. 1 Schematic diagram of double metal below ferroelectric layer FET (DM-below-NCFET) for biomolecules

3 Simulation methodology

Visual TCAD system is used for simulating all results. This region is confined to Bio1 and Bio2 to introduce and identify biomolecules. In this work, impartial(neutral) biomolecules, for example, streptavidin, protein, uricase, and ChO_x are created in the gap of the cavity. Drain voltage, V_d (V) is fixed in the entire process at 0.4 V. Gate voltage, V_{gs} is different from 0 to 4 V. temperature (T) is fixed during the entire device simulation at 300 K (room temperature). So, the existence of impartial biomolecules can be patterned by initiating substance with a dielectric constant related to impartial biomolecules. This method has been calibrated with the outcomes of the experiments [6, 21].

The design is used in concentration-dependent mobility (CONMOB), field-dependent drift velocity (FLDMOB) model, Shockley–Read–Hall (SRH) recombination model, and polarization model. We utilize visual TCAD multiphysics to play out every single mathematical reproduction. Bioelectronics is focused on straightforwardly coupling biomolecular work units of high-atomic weight and incredibly confounded subatomic construction (chemicals, receptors, or entire, cells, and so on just as tissues, cell clusters, and organisms) with electronic or optical transducer device. Elective and new ideas are constantly emerged and proposed for future data advancements to address, control, read, and use data, requiring the improvement of constructions for signal take-up, transduction, enhancement, handling, and change [24, 25].

The absorption of various biomolecules is patterned by the initiation of an non-conductor having the identical dielectric constant such as a specific biomolecule into the cavity's gap. The void cavity (i.e., without biomolecules present) is demonstrated by applying an insulator with dielectric constant (K = 1), although the dielectric constant of the diverse studied biomolecules is like this as shown in Table 1: protein (K = 8) [26], uricase (K = 1.5), ChO_x (K = 3.5), and streptavidin (K = 2.1) [27]. Streptavidin is utilized to distinguish Marek's disease virus (MDV) applying an enzyme-linked immunosorbent assay (ELISA) method [28, 29].

The essential thought behind a MD simulation is clear. Given the places of the multitude of atom in a biomolecular framework (e.g., a protein encompassed by water and maybe a liquid bilayer), one can compute the force applied on every particle by the wide range of various molecules. One can hence utilize Newton's laws of movement to foresee the spatial place of every molecule as an element of time. Specifically, one stages through time, more than once ascertaining the force on every iota and afterward utilizing those force to refresh the position and speed of every particle. The subsequent direction is, basically, a three-layered film that depicts the nuclear level setup of the framework at each point during the simulated time interval [30].

4 Results and discussion

4.1 Impact of dielectric modulation for cavity gap 10 nm

Figure 2 shows the curve between drain current, I_d (A) in linear scale and log scale vs gate voltage, V_{gs} (V) of different biomolecules for double metal below negative capacitance field-effect transistor (DM-below-NCFET) at V_d = 0.4 V, channel length, L_c = 20 nm, and oxide thickness T_o = 1 nm. The drain current of protein (K = 8) is higher than the others biomolecules, as enhanced drain current with an increase in dielectric constant that reflects the improved gate coupling capacitance and lowered leakage current I_{off} in the left side of the graph.

Table 1 The value of dielectric constant for biomolecule

Biomolecules	Dielectric constant
Uricase	1.5
Streptavidin	2.1
ChO_x	3.5
Protein	8

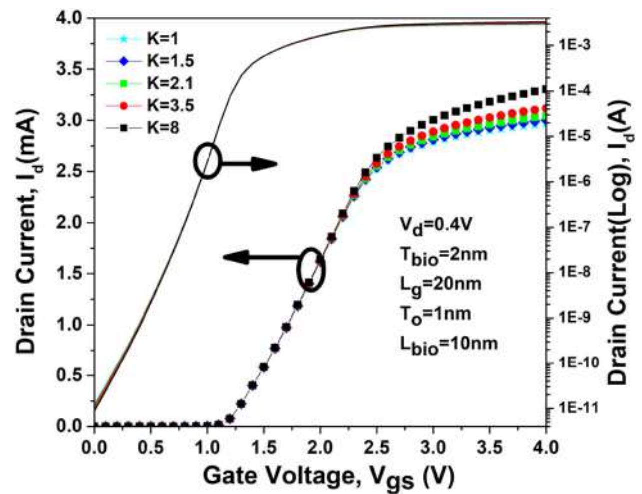

Fig. 2 Transfer characteristic of DM-below-NCFET for different biomolecules at drain voltage 0.4 V

Figure 3 reveals that transconductance is a factor of the shift in drain current (I_d) to shift in gate voltage (V_{gs}) at drain voltage (0.4 V). The transconductance curve of protein is higher than the streptavidin, uricase, ChO_x, without molecules. Thus, the g_m has taken from the curve drain current vs gate voltage that reflects enhanced gate control and lowered short channel effects (SCEs) and also increases average

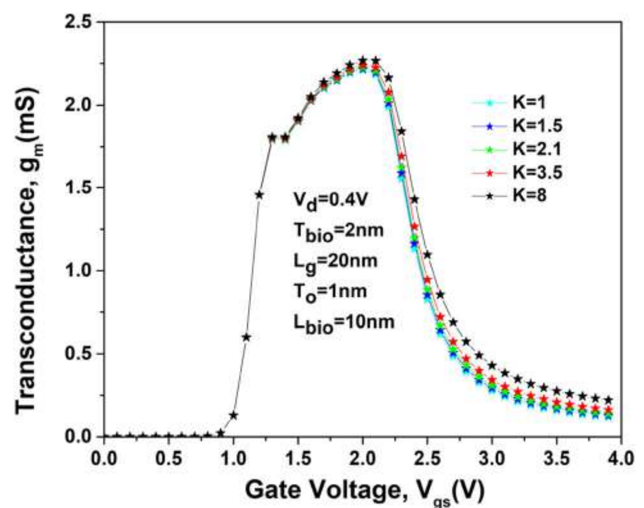

Fig. 3 Transconductance (g_m) of DM-below-NCFET for different biomolecules at V_d 0.4 V

carrier velocity, upgraded electron mobility with increase transconductance [31].

Figure 4 shows the threshold voltage, V_{th} (V) of protein is enhanced than other biomolecules configuration at drain voltage, V_d = 0.4 V because of enlarged gate control over the channel and biomolecule of protein is the better shield of drain-side potential so that improved the character of the threshold voltage. The threshold voltage is directly related to the dielectric constant was applied as a sensing application for recognition. Figure 5a shows the switching ratio, I_{on}/I_{off} of protein is higher than the different biomolecules at L_g = 20 nm, T_o = 1 nm, L_{bio} = 10 nm, and V_d = 0.4 V, decreased leakage current, I_{off} (A/um), and high switching speed for protein molecules (K = 8) is also obtained. Figure 5b implies the sensitivity of various biomolecules for instance protein, streptavidin, uricase, ChO_x, and without biomolecules at drain voltage 0.4 V as shown in Table 2. The cavity gap is completely filled with dielectric constant. The formula for sensitivity is given in Eq. (1).

$$S = \frac{I_{on}(K > 1)}{I_{on}(K = 1)} \quad (1)$$

Figure 6a–e represents the contour plot of electronic concentration of channel from source to drain for various dielectric constant Fig. 6a implies biomolecule is created, the extra charges become caused in the channel from source to drain in the region beneath the cavity. Charge quantity caused hangs on the various biomolecules. The electronic

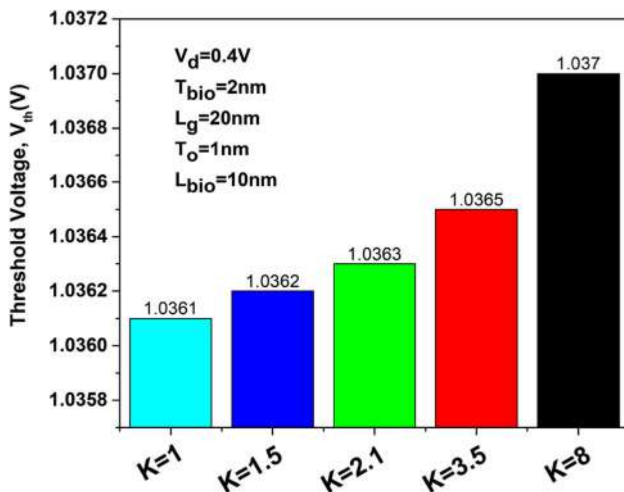

Fig. 4 The threshold voltage (V_{th}) of DM-below-NCFET for different biomolecules at V_d 0.4 V

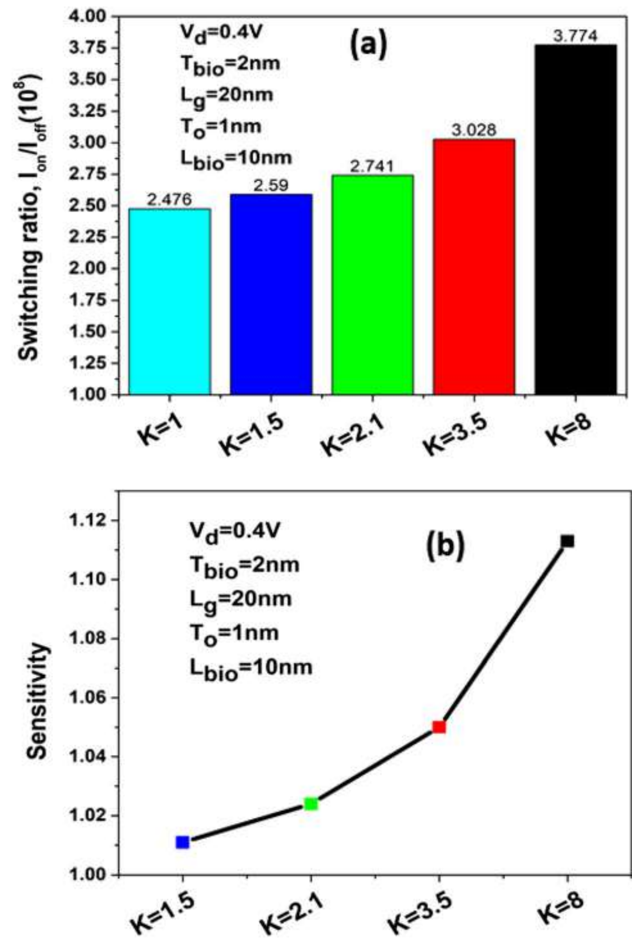

Fig. 5 **a** Switching ratio (I_{on}/I_{off}), **b** sensitivity of DM-below-NCFET for different biomolecules at drain voltage 0.4 V

Table 2 Value and parameter of DM-Below-NCFET for different biomolecules at T_o = 1 nm and cavity length 10 nm

Parameter	$K = 8$	$K = 3.5$	$K = 2.1$	$K = 1.5$	$K = 1$
I_{on} (mA)	3.31	3.12	3.04	3.01	2.97
I_{off} (pA)	8.76	10.3	11.1	11.6	12
I_{on}/I_{off} (10^8)	3.77	3.03	2.74	2.59	2.48
V_{th} (V)	1.037	1.0365	1.0363	1.0362	1.0361
g_m (mS)	2.27	2.23	2.21	2.2	2.19
g_d (nS)	0.662	0.698	0.718	0.731	0.744

concentration of protein at drain is worked at lower concentration. Due to the smallest value of the dielectric constant of without molecules, extra charges are created in the channel as shown in Fig. 6f that is deducted from the increase of drain current.

Figure 7a–e reflects the contour plot of the potential of the channel for diverse biomolecules. It is also

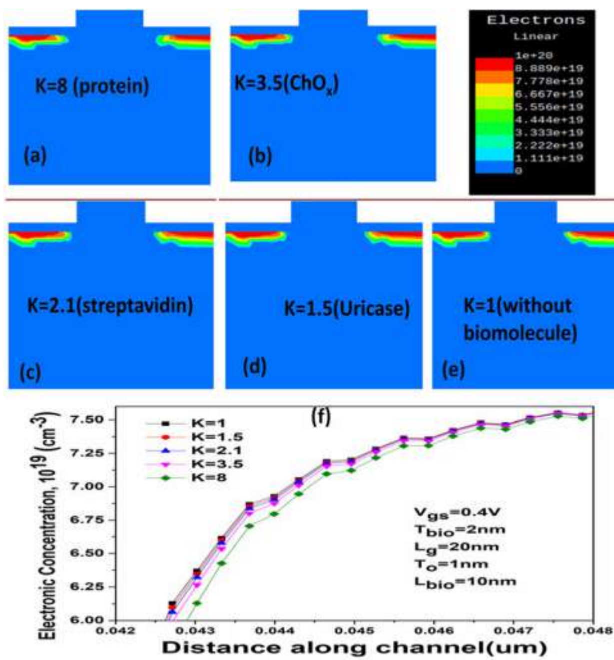

Fig. 6 **a**–**e** Electronic concentration contour plot of DM-below-NCFET at V_d 0.4 V for different biomolecules, for example, **a** $K = 8$, **b** $K = 3.5$, **c** $K = 2.1$, *d* $K = 1.5$, *e* $K = 1$, and **f** graph of electronic concentration vs distance along channel

the electrical performance of DM-below-NCFET. Changes of the potential occur (at the drain side) under the cavity region. When the cavity gap is immobilized by biomolecules [32], a deformation in potential is detected because of the shift in the dielectric constant caused by the biomolecules as shown in Fig. 7f. This change in potential can as well be applied to identify the existence of biomolecules in the cavity gap area.

Figure 8 signifies the plot of drain current, I_d (A) vs drain voltage, V_d (V) at gate voltage V_{gs} (0.4) oxide thickness of 1 nm, cavity gap of 10 nm, and channel length of 20 nm. Output conductance is the driving capacity of the device as characterized mirrors the locale of device activity as shown in Fig. 9. At first, a high-output conductance in the linear region is observed with increasing drain voltage beyond pinch-off voltage owing to drain-induced barrier lowering (DIBL) as well as channel length modulation (CLM) [33]. The g_d

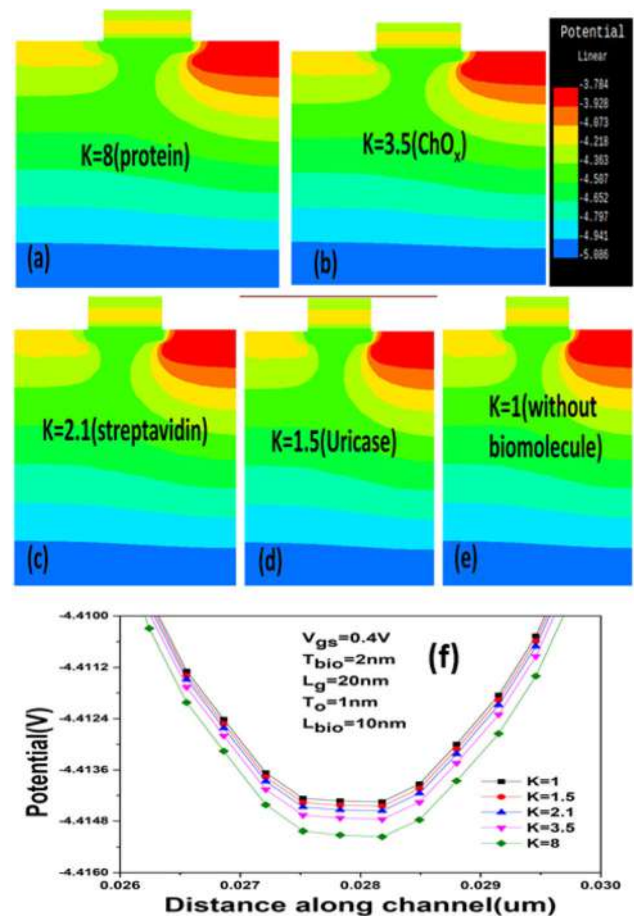

Fig. 7 Potential contour plot of DM-below-NCFET at V_d 0.4 V for different biomolecules for example **a** $K = 8$, **b** $K = 3.5$, **c** $K = 2.1$, **d** $K = 1.5$, **e** $K = 1$, **f** Potential graph of DM-below-NCFET at drain voltage 0.4V for different biomolecules

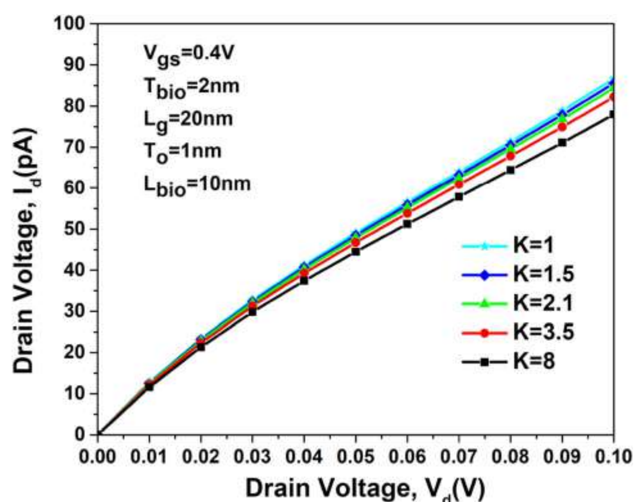

Fig. 8 Graph of drain current vs drain voltage of DM-below-NCFET at gate voltage 0.4 V for different biomolecules

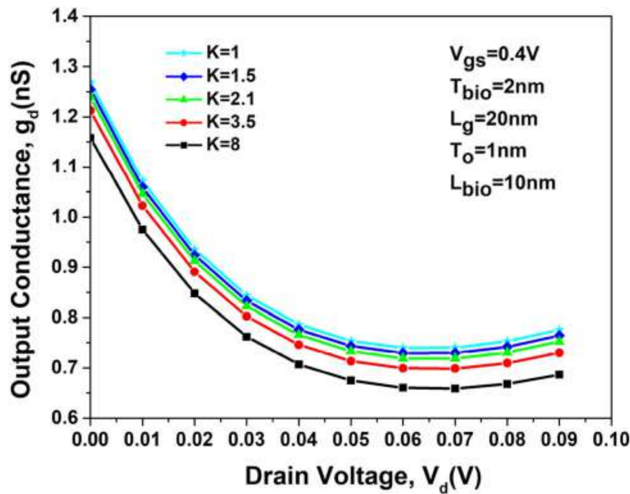

Fig. 9 Graph of output conductance vs drain voltage of DM-below- NCFET at gate voltage 0.4 V for different biomolecules

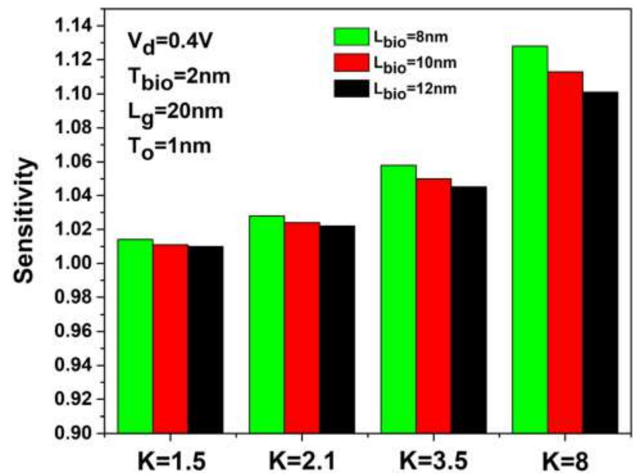

Fig. 11 Sensitivity of DM-below-NCFET at drain voltage 0.4 V for various biomolecules with different cavity length L_{bio} = 8 nm, 10 nm, and 12 nm

4.2 Effect of length modulation in cavity gap

Figure 10 shows graph of drain current vs gate voltage for various cavity length L_{bio} = 8 nm, 10 nm, and 12 nm with various biomolecules for instance ChO_x, protein, streptavidin, uricase, and without biomolecules. The drain current of protein with cavity length (L_{bio} = 8 nm) is enhanced over others as the dielectric constant increases with lower cavity reflects to improve drain current.

Figure 11 implies that the switching ratio was obviously lowered due to a rise in the leakage current subsequent from greater capacitance with the rise in the cavity gap length. Furthermore, the sensitivity of the DM-below-NCFET biosensor with distinct cavity gap lengths was too calculated, exposing that it improved meaningfully with the rise in L_{bio} (Fig. 12). Since this figure, it is stated that the sensitivity enhanced with a dielectric constant for offered L_{bio}. Thus, for L_{bio} = 12 nm, the nanogap-inserted DM-below-NCFET biosensor indicated improved sensitivity for protein (K = 8) in analogy with the additional biomolecules.

Figure 13 gives the plot of limit of detection (LOD) vs different K values with standard deviation 0.000719 for K = 1, 0.000719 for K = 1.5, 0.00072 for K =

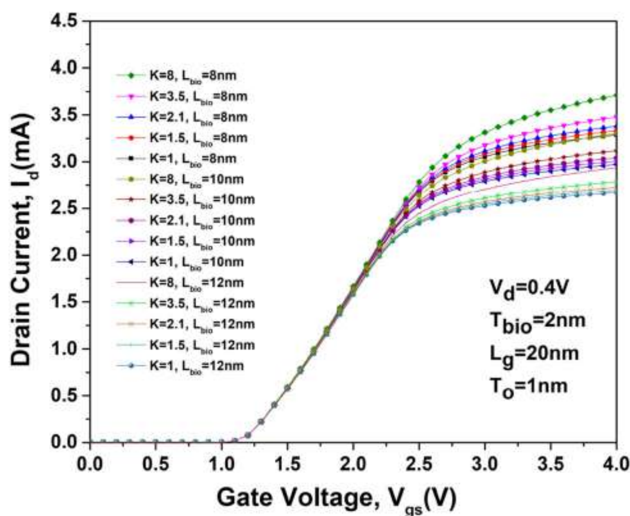

Fig. 10 Plot of drain current vs gate voltage of DM-below-NCFET at drain voltage 0.4 V for various biomolecules with different cavity length L_{bio} = 8 nm, 10 nm, and 12 nm

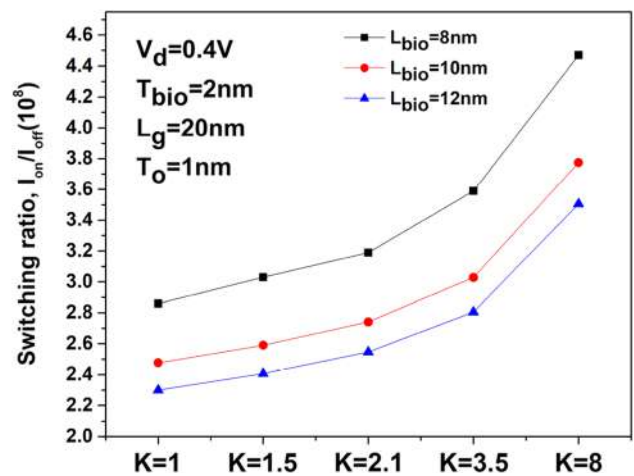

Fig. 12 Switching ratio of DM-below-NCFET at drain voltage 0.4 V for various biomolecules with various cavity length L_{bio} = 8 nm, 10 nm, and 12 nm

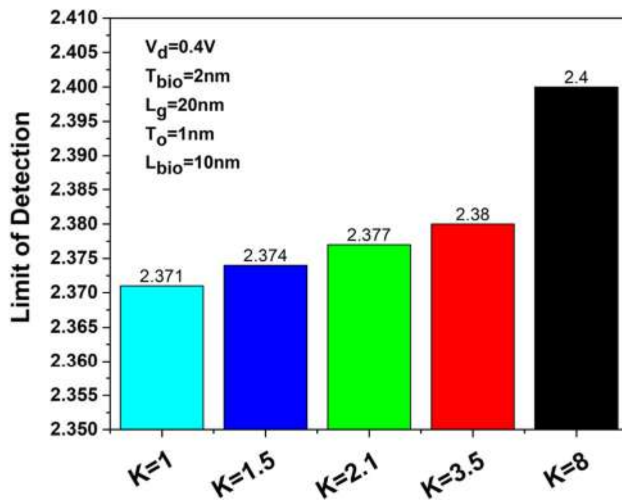

Fig. 13 Plot of limit of detection (LOD) vs different K values with standard deviation 0.000719 for $K = 1$, 0.000719 for $K = 1.5$, 0.00072 for $K = 2.1$, 0.000722 for $K = 3.5$, and 0.000727 for $K = 8$

2.1, 0.000722 for K = 3.5, and 0.000727 for K = 8. LOD of protein is higher than without molecule that indicating higher concentration of analyte in the sample that can be detected but not necessarily quantified [34]. It is determined by the response of standard deviation and slope. At the lower limit of detection in COVID-19 reflects it can miss more infected cases. These outcomes give understanding into the significance of controlling properties for amplifying sensitivity and limiting execution variety across device when planning and manufacturing nano-FET biosensors [35, 36].

Figure 14 shows the experimental data and simulated result with some parameters and reveals the curve of drain current and gate voltage at drain voltage is 0.1 V, ferroelectric thickness is 5 nm, and the channel length is 30 um for negative capacitance field-effect transistor (NCFET), and data of experiment are taken from reference [7].

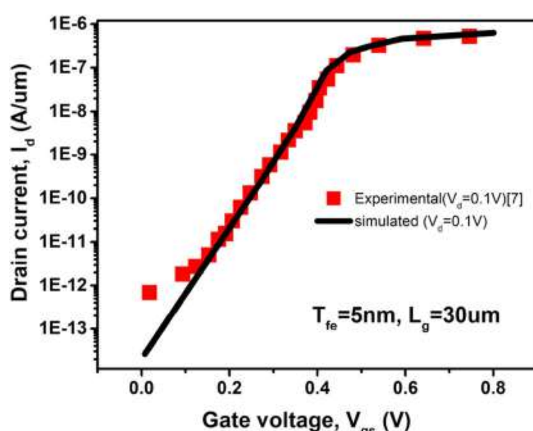

Fig. 14 Calibration results of experimental data and simulated data curve of drain current vs gate voltage at V_d = 0.1 and the channel length is 30 um

Organic FETs have formed into an astonishing area of examination and innovation to supplant exemplary inorganic semiconductors. Light-emitting diodes, organic photovoltaics, and thin-film transistors are as of now very much evolved and are at present being marketed an assortment of application for DM-below-NCFET. All the more as of late, organic FET has tracked down new applications in the field of biosensors [37, 38]. The FET-based biosensor turns into a promising contender for applications requiring ultra-sensitivity and fast reaction time. Moreover, new era complementary metal-oxide semiconductor (CMOS)-producing methods give advantages of scaling down, parallel detecting (for example, detecting clusters), and abilities to be coordinated with electronic circuits and frameworks. This would be a significant benefit for strong state-based biosensors to compete with other bio-detecting mechanism later on [23].

5 Conclusion

In this work, we examined the biosensing application of a double metal below negative capacitance FET (DM-below-NCFET). For the recognition of different biomolecules, the electrical performance was calculated in conditions of the shift of threshold voltage for protein enhanced by 0.09% over without biomolecule, the sensitivity of protein improved by 1.11 by times over $K = 1$, switching ratio of protein higher by 52% over to without biomolecule, the surface potential at cavity length of 10nm, as shown in Table 2, and measured higher limit of detection for protein by around 1.18% over without molecules. The DM-below-NCFET device was significantly improved, indicating better sensitivity for biomolecules with a large value of K. The proposed device realized that the sensitivity was greater for the recognition of protein ($K = 8$) in analogy with the various biomolecules. Moreover, the impacts of the gap of cavity length on the V_{vt}, sensitivity, and switching ratio(I_{on}/I_{off}) of the DM-below-NCFET biosensor were too analyzed, exposing that the sensitivity enhanced with the rise in the gap size although the whole biosensor

operation was marginally reduced. So, the gap of cavity length is well improved for improved execution, which will authorize the utilization of such cavity length of 8 nm high sensitivity, high-speed biosensors for recognition of several associated diseases.

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Author contributions

All authors added to the study's understanding and design.

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Data availability

The creators expressed above have every one of the suitable data associated with this examination work and will be dedicated to uncovering that they will be addressed to do as such future.

Declarations

Conflict of interest The writers broadcast that they have no known dispute of individual connections or interests that might have arisen to impact the work depicted in this article.

Ethical standards The authors have found all the moral standards and will intended to follow them in future.

Consent to participate and publication Since the related research document is created on the 'no-life science journal.' Therefore, 'Non-Applicable' at this point. Still, the authors have turned over all journal guidelines and consent to the agencies for additional processing.

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PAPER

DFT based atomic modeling and Analog/RF analysis of ferroelectric HfO_2 based improved FET device

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Abstract

In this study, we systematically investigated the Analog/RF and linearity parameter of SM DGNCFET (single metal double gate negative capacitance field effect transistor) and DM DGNCFET (double metal double gate negative capacitance Field effect transistor) with the help of Cogenda Visual TCAD simulator, and also demonstrated the enhancement in the electronic and optical properties of Si-doping bulk structure by using the Quantum ATK. The analog parameters are enhanced for SM DGNCFET such better performance of switching ratio 279 times better, DIBL 54% lower, SS decay, and some other improved parameter transconductance, TGF and Radio frequency parameter is also enhanced, transconductance frequency product (TFP) for improving reliability and stability of device. Linearity parameters like that second and third order transconductance (g_{m2}, g_{m3}), voltage intercept point for 2nd, 3rd. Tran Blaha modified Becke Johnson (TB-mBJ) approxiamation gives the accurate band gap of crystal. In DFT based atomic study, 12.5% of Si doping in bulk structure reveals better results for ferroelectric HfO_2 based crystal in the direct band gap of bandstructure is zero, Density of state (DOS) is also improved conductivity for Si doping crystal. Hence, Si doping in crystal structure is also better for conductivity.

1. Introduction

The power dissipation (P) varies with the inventory voltage ($P \sim V_d^2$), V_{ds}. It is typically controlled by the obstacle monitored Boltzmann switch's base subthreshold swing (SS = 60 mV/dec) [1]. Ferroelectric (Fe-FETs) transistors have recently gotten plenty of attention due to their reliability in memory and switching applications [2–4]. The key factors of any sophisticated electronic device are power, size utilisation, the goal of previous and current research attempts, which has been to create aggressively updated devices that utilize ultralow power [5]. Towards conquer this constraint, there has been a lot of concern in selective devices that are based on a variety of activity systems that alter the state of an electrical switch from off to on device [4].

Improvements of the ferroelectric layer device with a Negative capacitance FET in single metal double gate and double metal double gate negative capacitance field effect transistor (DM DGNCFET) [6, 7]. NEGATIVE capacitance FETs (NCFETs) are field effect transistors with a sub-60mV/decade subthreshold swing and a large ON-current. Negative capacitance wonders have recently demonstrated experimentally in a variety of contexts [5]: (1) ferroelectric pictures separated from the rest of the world (2) Bilayers of ferroelectric and dielectric (3) Ferroelectric gated transistors using superlattices [8, 9]. Channel length scaling was not taken into account by SM DGNCFET [7, 10, 11]. Furthermore, the Landau model is merely used in the knocked out polarisation section of the last. The Landau factors for the FE substance are $\beta = 8.9 \times 10^8$ and $\alpha = 1.0 \times 10^7$ [12], which are insufficient for large ferroelectric thicknesses [13]. By using logical displaying, we evaluated the implementation of the SM DGNCFET with long channels in prior work [6]. SM DGNCFET has a larger ON-state flow than DM DGNCFET; however, we found that it is not the case for all ferroelectric materials.

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Furthermore, due to their capacity requirements down, non-destructive read capabilities as rapid operating speed, and memory device in ferroelectric field effect transistors (FeFETs) hold out for a modern age of FET devices [14, 15]. FE substance displays the supervise of negative capacitance, which can be detected from their charge energy bend [16], ferroelectric substance in the gatestack of MOSFETs provides superior endurance to device accomplishment.

The SM DGNCFET device has lowered the leakage current, higher switch ratio, low power consumption, better device controllability over channel than DM DGNCFET. The impact of ferroelectric thickness and temperature has been studied. The impact of ferroelectric thickness and temperature of device has been also studied for improving the performance of SM DGNCFET as increases the ferroelectric thickness, decreases substrate thickness and decreases temperature [17, 18].

DFT (density functional theory) is a quantum-mechanical atomistic modelling approach for computing features of nearly any atomic system, including surfaces, crystals, molecules, and even electrical devices when linked with non-equilibrium Green's functions (NEGF). Atomic modeling of the significant developments in quantum theory is the density functional theory (DFT), which aids in verifying the energy, structure, and characteristics of materials, nanosystems, and molecules. The interface engineering in HfO2-based gate stacks, atomic dopants have been demonstrated to alter the work function [19]. At 2800 degrees Celsius of HfO_2 is in the cubic phase [20, 21]. At lower temperatures of yttrium doping affords HfO_2 cubic phase stability [22]. Random access memory devices, fuel cells, sensors, optical and protective coatings, laser mirrors, and other industrial applications all utilise the cubic HfO_2 phase. Low lattice thermal conductivity results from the high density of Hafnium in HfO_2. The lattice thermal conductivity of HfO_2 thin films has been measured in the range of 0.49 to 0.95 W/m-K [21].

The possible technology uses, such as ferroelectric field effect transistors (FEFET) and ferroelectric random-access memory(FERAM), achieving ferroelectricity in thin films has been a decades-long research quest [23–25]. Low power consumption, controllability over variability, and high switching speed are all benefits of ferroelectric-based technology over the current non-volatile memory technology. However, due to a dearth of ferroelectric materials that meet all of the conditions for a practical memory technology: scalability, CMOS compatibility, and memory retention, this promising technology has not been extensively applied [26]. In today's field effect transistor devices, HfO_2 is one of the most extensively utilised dielectric gate oxides [27, 28].

2. Design for device and atom

2.1. Structure of device

Figure 1 reveals two device structures (a) Double metal double gate negative capacitance Field effect transistor (DM DGNCFET) and (b) single metal double gate negative capacitance FET (SM DGNCFET). The dimension of these two devices almost same except Metal2-Top and Metal2-bottom ($T_{m2T/m2B}$) are varing from SM DGNCFET. The thickness of $T_{m2T/m2B}$ is 5 nm with aluminum metal for DM DGNCFET.

The length of the channel(L_{ch}) is 60 nm, the Drain/Source length ($L_{d/s}$) is 50 nm, the Drain/Source thickness ($T_{d/s}$) is 5 nm, and the Oxide thickness(T_{ox}) is 0.6 nm. T_{ox} is 7 nm, and Metal1 has a top and bottom thickness of 10 nm as illustrates table 1. SM DGNCFET and DM DGNCFET have 50 nm length of total gate channel size (L_g). The entire gate channel thickness (T_{ch}) of an SM DGNCFET is 10 nm. To explain key concepts in the book, a variety of classical models are used. Shockley-Read-Hall (SRH) classical describes the trap charges, while Lombardi model surface mobility model for electron mobility in a basic MOSFET Recombination influences, presence at the site of contact Fermi–Dirac equation is a mathematical formula that describes the relationship between two particles. Precision is achieved by the use of insights. The Arora model mobility is influenced by focus. The material for metal1 Top and bottom, metal2 Top and metal2 bottom is aluminium. Gate oxide material is used SiO_2, Material of ferroelectric is HfO_2FE (a latest thought of a ferroelectric coating with hafnium dioxide), substrate substance is Silicon easily available in anywhere. The doping concentrating of Drain/Source ($N_{d/s}$) is 1×10^{20} cm^{-3} with Gaussian profile. The workfunction of aluminium metal is 4.2 eV for dual gate.

2.2. Structure of ferroelectric HfO_2 based crystal

The ferroelectric HfO_2 based structure is created in crystal Simple cubic structure with dimension a = 10.23A, b = 10.23A, c = 10.23A, $\alpha = 90$, $\beta = 90$, $\gamma = 90$. The structure of crystal atoms have eight Hf (hafnium) and sixteen Oxygen(O) for without doping. For Si doping, 12.5% of Si is added in crystal structure as shown in figure 2. The cartesian coordinate for Si doping is [0.7677, 2.621, 3.128] A. This research have revealed that HfO_2 films doped with a few percent of a variety of dopants or 12.5 per cent Si, grown to be 7 nm thick between dual gate metal electrodes, and annealed may exhibit ferro-electricity. The ferroelectric behavior of TiN/HfO_2/TiN stacks is dramatically inhibited when the film is annealed before the top electrode is deposited, according to

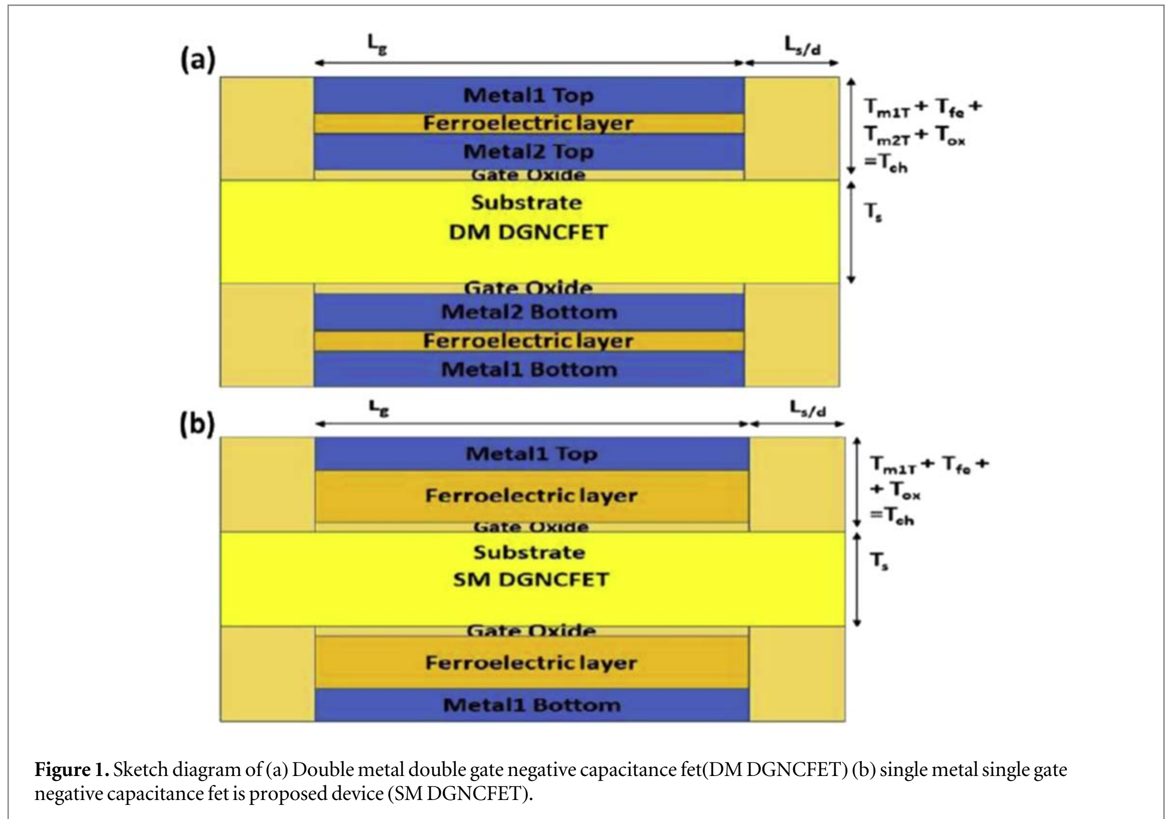

Figure 1. Sketch diagram of (a) Double metal double gate negative capacitance fet(DM DGNCFET) (b) single metal single gate negative capacitance fet is proposed device (SM DGNCFET).

Table 1. The Device parameters for SM DGNCFET and DM DGNCFET are used for the simulation.

Parameter	SM DGNCFET	DM DGNCFET
Oxide Thickness (T_{ox})	0.6 nm	0.6 nm
Gate length (L_g)	50 nm	50 nm
Substrate thickness (T_{sub})	05 nm	05 nm
Ferroelectric thickness (T_{fe})	07 nm	07 nm
Source/Drain length ($L_{s/d}$)	05 nm	05 nm
Metal1 Top/Metal1 bottom thickness ($T_{m1T/m1b}$)	10 nm	10 nm
Concentration of Drain/Source ($N_{d/s}$)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}

certain investigations, indicating that the confinement provided by the top electrode during annealing is critical for ferroelectricity [23, 29].

3. Methodology and theoretical details

3.1. Device methods

Cogenda Visual TCAD simulator is used for all simulations. A comparison of two devices the DM DGNCFET and the SM DGNCFET was performed. Throughout the operation the drain voltage, V_{ds} (V) is kept constant at 0.05 V. The gate voltage, V_g (V) varies between 0 and 0.5 volts. During the device simulation, the temperature (T) is kept constant at 300 K in all scenarios (room temperature). We ignored the ferroelectric dipole connection, depolarization fields in HfO_2-based ferroelectrics, on the other hand, we can reach the coercive field's order of magnitude and so cannot be ignored [30, 31]. To carry out the SM DGNCFET and DM DGNCFET designs, distinct limit conditions are used. Congruency of usual sections of translation vectors is used at the oxide ferroelectric restrictions in the SM DGNCFET structure. The interior metal gate serves as a coating terminal for the DGNCFET structure. Every mathematical recreation is performed using Cogenda visual TCAD Multiphysics [32].

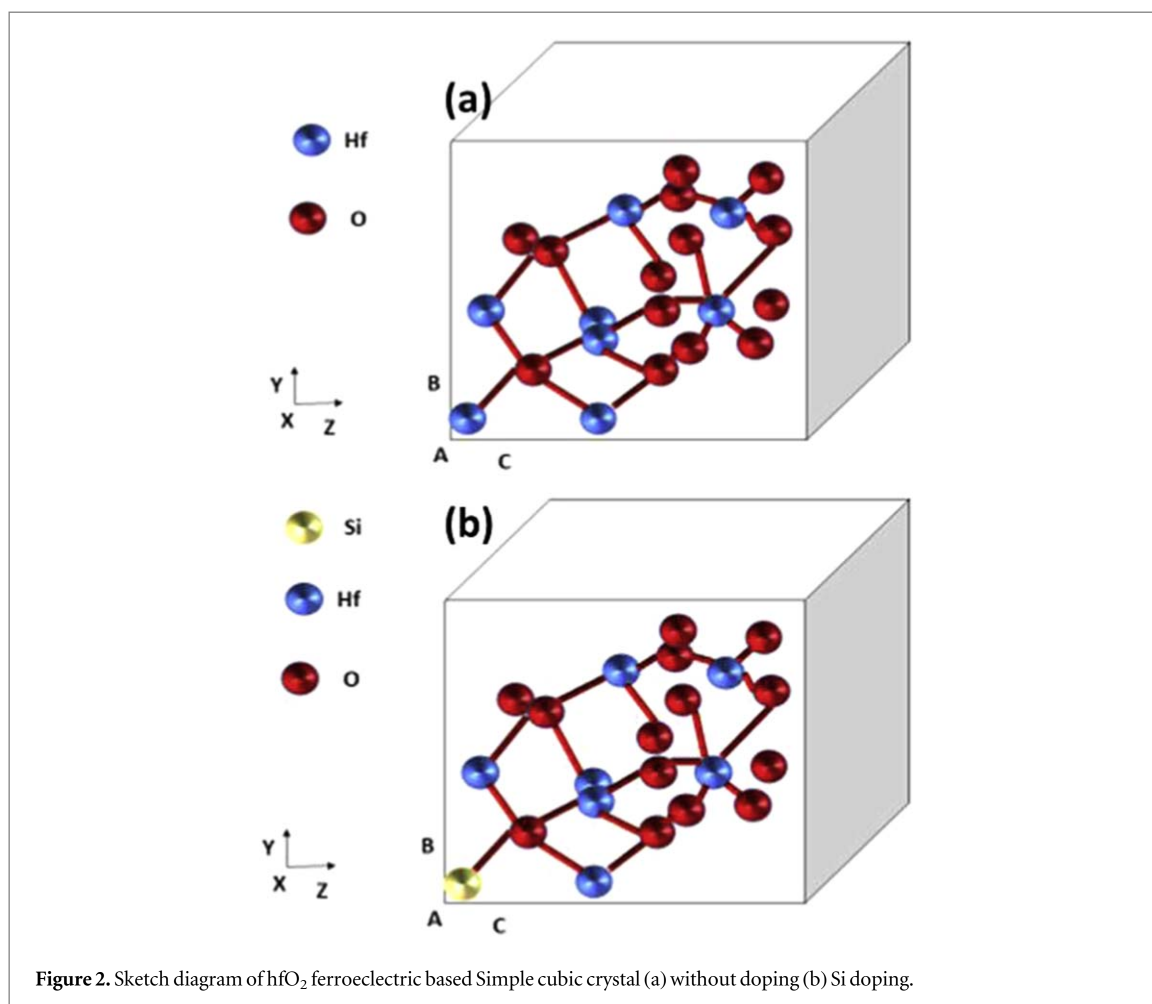

Figure 2. Sketch diagram of hfO_2 ferroeclectric based Simple cubic crystal (a) without doping (b) Si doping.

3.2. Method for HfO_2 crystal

Quantum ATK (Atomic tool kit) simulator is used for atomic study of density function theory. We use DFT in the Perdew–Burke–Ernzerhof Generalized Gradient Approximation (PBE GGA) [33] with ultrasoft pseudopotentials to compute minimal energy structures. Tran Blaha modified Becke Johnson (TB-mBJ) approxiamation gives the accurate band gap of crystal. This effect is eliminated by placing a fictional dipole in the cell's vacuum area, which cancels out the electric field in vacuum. The forces on all atoms are loosened until they are less than 104 Ry/Bohr in magnitude in all axial directions [23, 34].

3.3. The flowchart from atomic modelling to device fabrication feasibility

The framework modelling from atomic to device has been synopsized in figure 3. We start with atomic model for band energy in Vander wall heterostructure (vdWH) at interfacial charge. 1st principal calculation gives the carrier mobility and dielectric constant value of material [35]. The material attributes are used for physics based device models to obtain the knowledge of FET and MOS properties by Quantum ATK simulator. The feasibility fabrication of SM DGNCFET has been reported by Visual TCAD simulator. The deposition of silicon film is thinning first. The deposition of Al_2O_3/HfO_2 layer has developed on silicon interfacing layer by using atomic layer deposition (ALD) [36]. The metal gate is fabricated on gate dielectric using electron beam evaporation process. The dopant of source and drain region implanted by spike annealing activation. Evaporation of the electron beam is made on the surface of the source and drain. SM DGNCFET has been formed.

4. Result and discussion

4.1. Comparative study of FET device

4.1.1. Analog performance

Figure 4 shows the drain current, I_d (A) in linear scale and log drain current scale versus gate voltage, V_g (V) for a ferroelectric film better Field Effect Transistor device that is a single metal double gate negative capacitance FET SM DGNCFET at constant room temperature T = 300 K, DM DGNCFET at V_{ds} = 0.05 V, channel length,

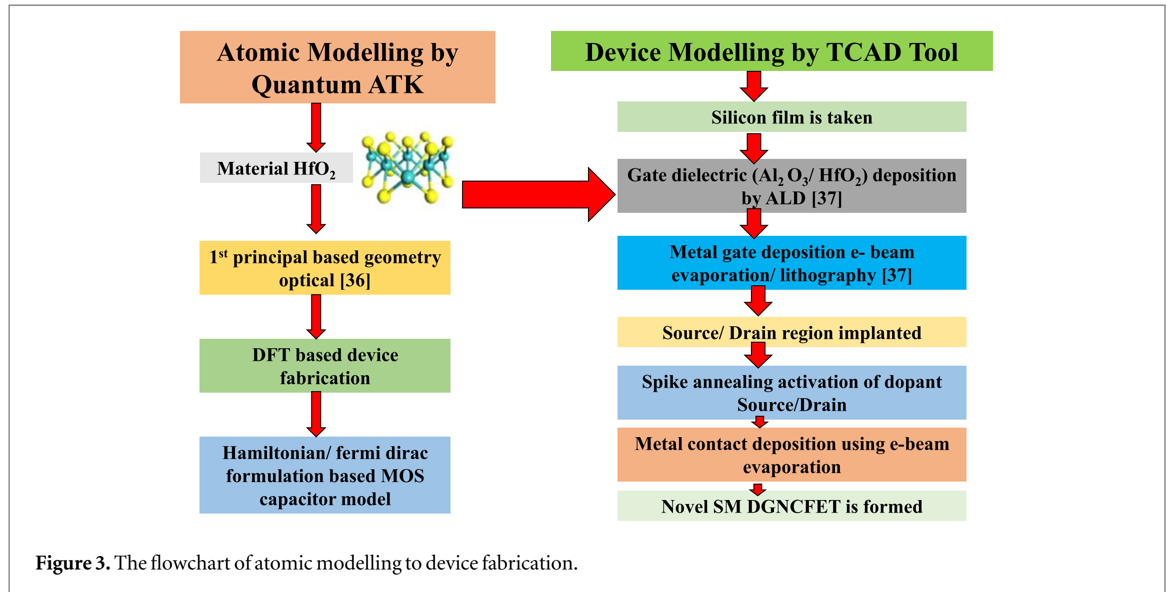

Figure 3. The flowchart of atomic modelling to device fabrication.

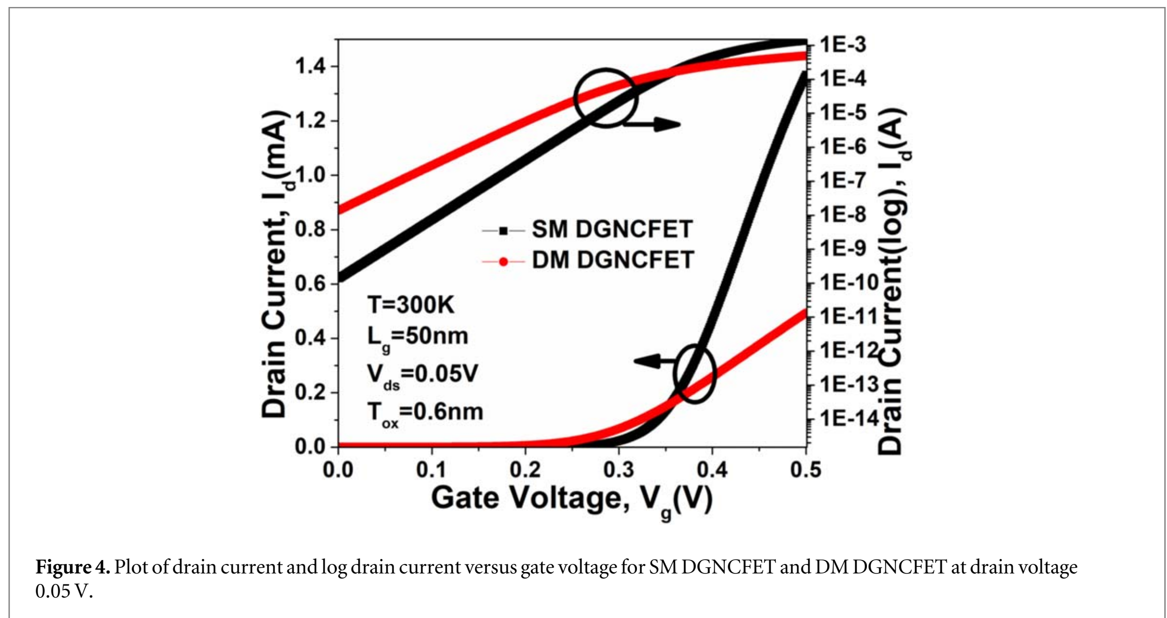

Figure 4. Plot of drain current and log drain current versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

$L_g = 50$ nm, T = 300 K It also shows that under negative bias, the off state current for SM DGNCFET is smaller. With increased gate voltage V_g (V), the drain current of SM DGNCFET designs is better than DM DGNCFET configurations, indicating superior gate coupling capacitance and lower leakage current I_{off} on the left side of the graph.

Transconductance is a measure of the ratio of drain current (I_d) to gate voltage (V_g) at drain voltage (0.05 V), T = 300 K, as shown in figure 5 SM DGNCFET has a greater transconductance curve than DM DGNCFET. As a result, g_m has adopted the shift in drain current versus gate voltage [37], which indicates improved gate control and reduced short channel effects (SCEs) [38, 39], as well as increased average carrier velocity and improved electron mobility with increased transconductance. Transcoductance generation factor (TGF) is also improved for SM DGNCFET because of g_m enhanced.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{g}}.} \tag{1}$$

$$TGF = \frac{\partial g_{\mathrm{m}}}{\partial I_{\mathrm{d}}} \tag{2}$$

The plot of drain induced barrier lowering (DIBL) for a different setup is shown in figure 6. It's a short channel effect (SCE), which implies electrons may readily travel from source to drain when the channel length decreases. The DIBL of the SM DGNCFET structure is lower than that of the DM DGNCFET structure, indicating lower leakage current and enhanced SCEs. The subthreshold swing (SS) of SCEs is also important,

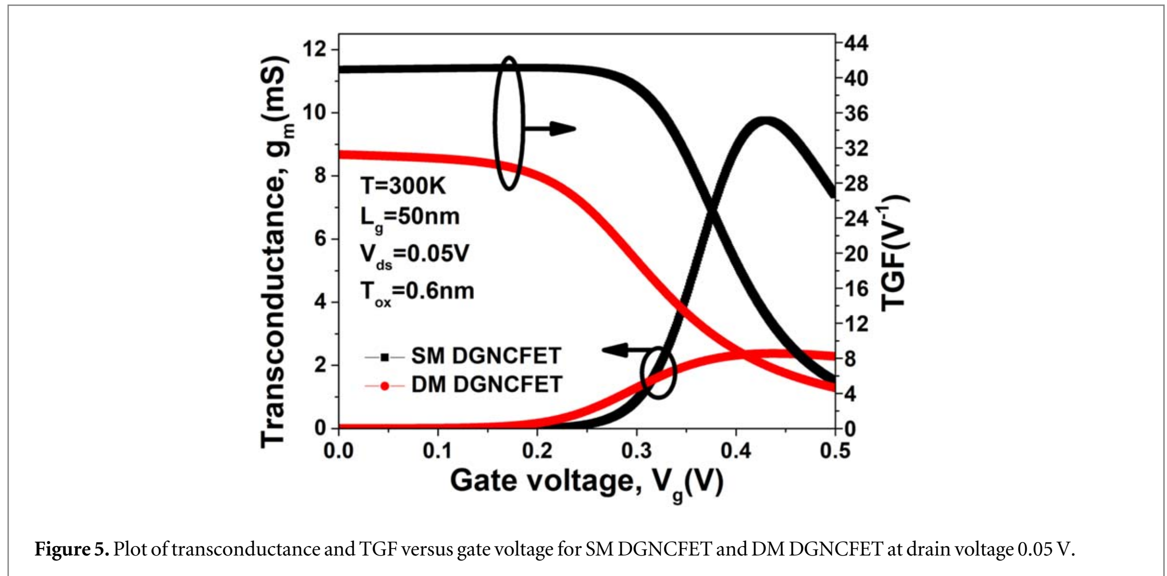

Figure 5. Plot of transconductance and TGF versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

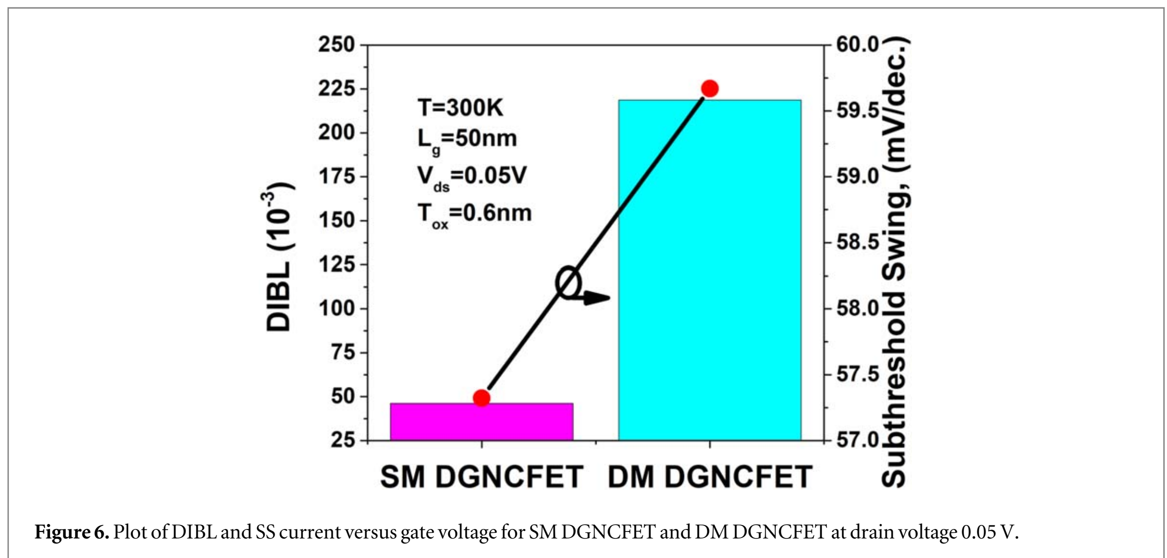

Figure 6. Plot of DIBL and SS current versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

with an optimum SS of 60 mV/decade. SM DGNCFET has a lower SS than DM DGNCFET, which is due to increased gate coupling capacitance with high permittivity (K), which improves gate control over the channel.

The threshold voltage, V_t (V) of SM DGNCFET at drain voltage, $V_{ds} = 0.05$ V is better than other DM DGNCFET device designs as illustrated in figure 7.

due to greater drain-side potential shielding and higher gate control over the channel. The threshold voltage's nature at $L_g = 50$ nm, $T_{ox} = 0$, the switching ratio I_{on}/I_{off} of SM DGNCFET is larger than the other DM DGNCFET structures. Reduced leakage current I_{off}(A), and rapid switching speed for the SM DGNCFET structure are also achieved at T = 300 K, and $V_{ds} = 0.05$ V as depicted in table 2.

Due to drain induced barrier lowering (DIBL) and channel length modulation (CLM), a high output conductance in the linear area is initially noticed with rising drain voltage beyond pinch-off voltage [40]. The g_d twist of the SM DGNCFET is smaller than that of the DM DGNCFET, indicating superior gate controllability and the ability to suppress brief direct hits, as shown in figure 8, indicating improved output obstruction.

$$g_{\mathrm{d}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{ds}}.} \tag{3}$$

$$F_t = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gd}} + C_{\mathrm{gs}})} \tag{4}$$

$$GFP = \left(\frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}\right) \times F_{\mathrm{t}} \tag{5}$$

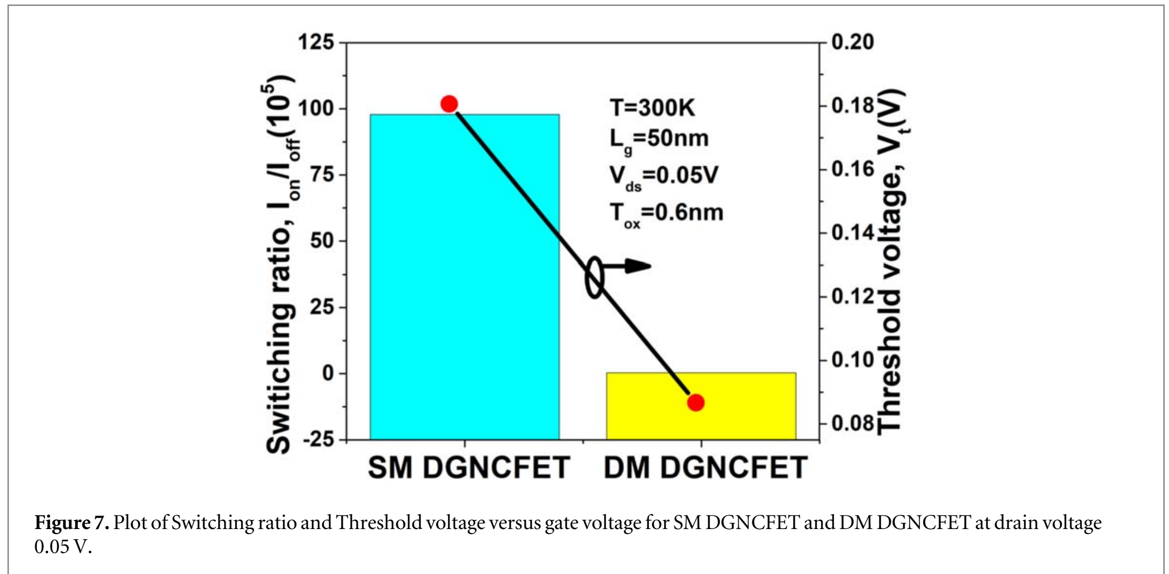

Figure 7. Plot of Switching ratio and Threshold voltage versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

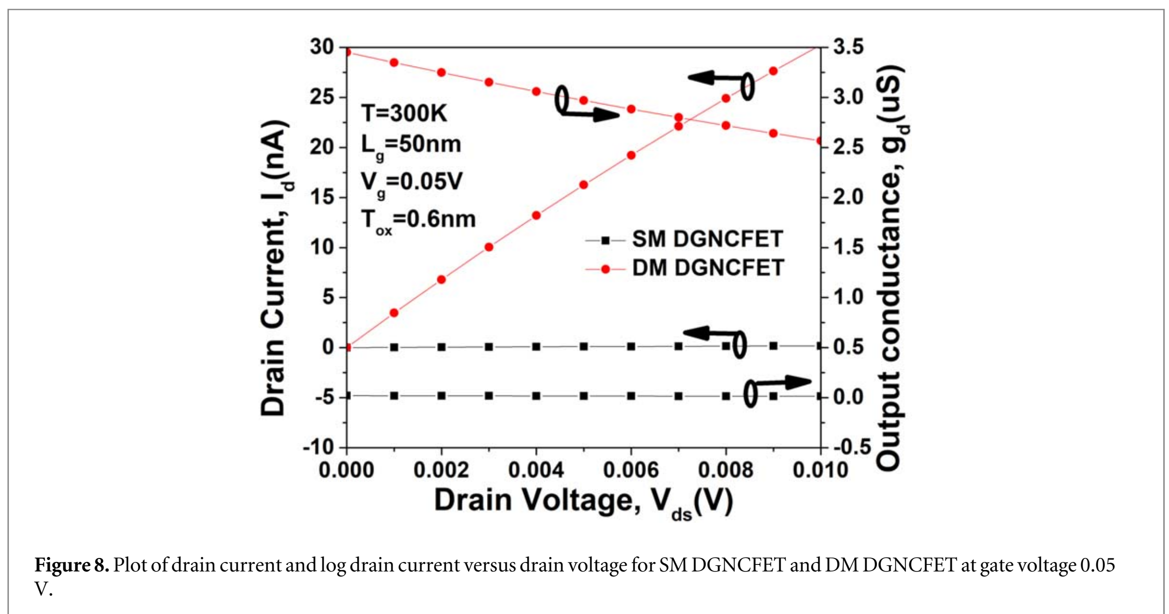

Figure 8. Plot of drain current and log drain current versus drain voltage for SM DGNCFET and DM DGNCFET at gate voltage 0.05 V.

Table 2. The data point of Leakage current, Subthreshold swing, Drain barrier induced lower for SM DGNCFET and DM DGNCFET.

Parameter	SM DGNCFET	DM DGNCFET
I_{on} (A) (10^{-3})	1.37	0.493
$V_{th}(mV)$	180.72	86.687
SS (mV/dec)	57.322	59.6
I_{off}(A)(10^{-10})	1.4	1.41
DIBL	0.0462	0.2187
$I_{on}/I_{off}(10^5)$	97.85	0.3496

4.1.2. Radio frequency analysis

According to figure 9, the SM DGNCFET configuration has a greater gate capacitance and cutoff frequency [41–43] than the DM DGNCFET configuration, revealing enhanced gate capacitance and increased transconductance as shown in equation (4) The device's time interval for producing output after receiving input shows lower input power consumption [44, 45]. The SM DGNCFET has a greater gate charge than other architectures, which reflects the high gate capacitance.

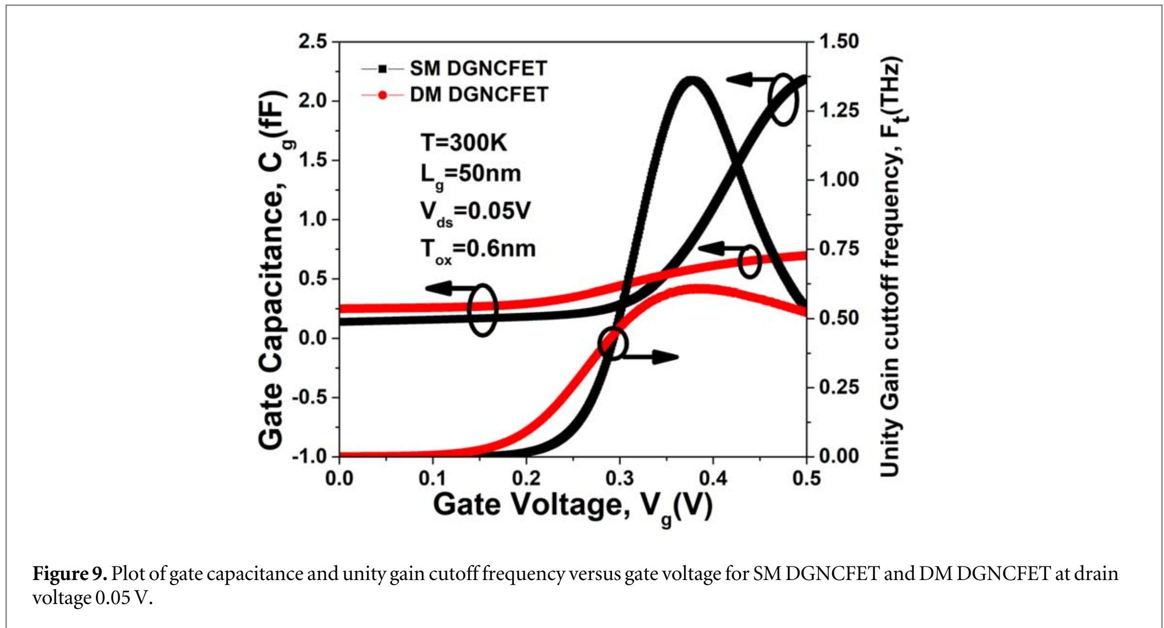

Figure 9. Plot of gate capacitance and unity gain cutoff frequency versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

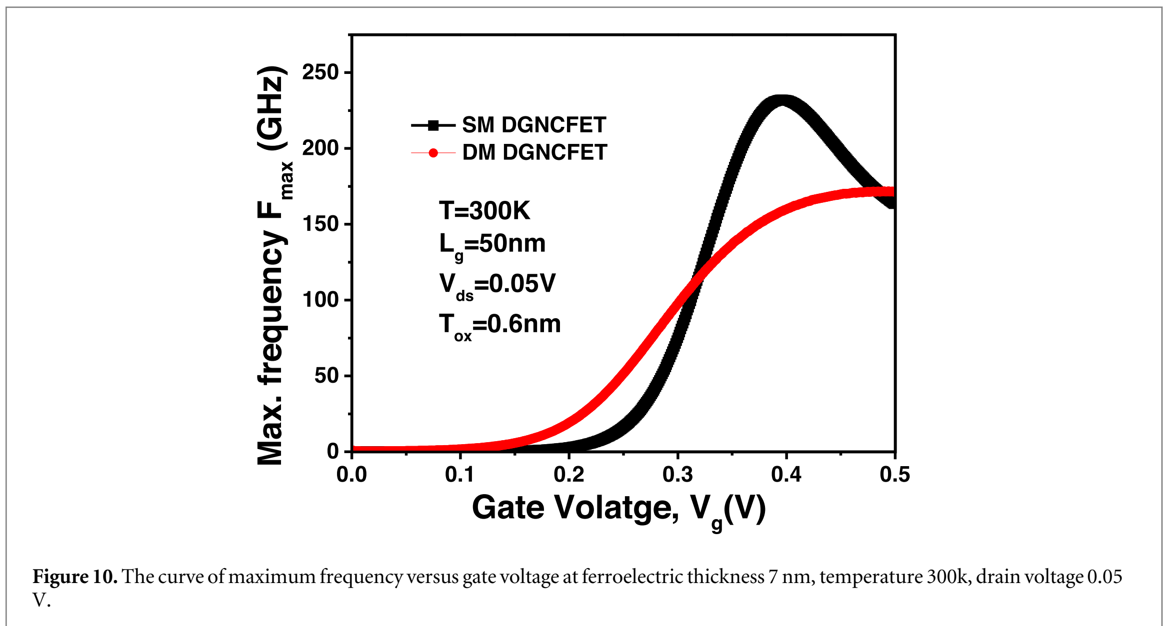

Figure 10. The curve of maximum frequency versus gate voltage at ferroelectric thickness 7 nm, temperature 300k, drain voltage 0.05 V.

The maximum frequency power gain ($F_{max.}$) is proportional to cut off frequency (F_t) as shown in figure 10. The $F_{max.}$ and F_t of SM DGNCFET is higher than DM DGNCFET which reveals the frequency gain and response at drain voltage 0.05 V. The $F_{max.}$ and F_t are the frequency of unilateral power gain and current gain becomes unity (0 dB). The F_t and $F_{max.}$ is higher which reflects the higher electron mobility in nmos than pmos, higher overdrive voltage to boost g_m, and use for minimum gate length [46, 47].

Variation of gain frequency product and transconductance frequency product versus gate voltage at T = 300 K and V_{ds} = 0.05 V is depicted in figure 10 for various architectures. The boost frequency product is a fundamental boundary used in high-recurrence applications as defined by equation (5). As we can be observed in figure 11, GFP increases as the gate voltage rises, reaching a maximum peak before dropping to a constant value in the saturation region. Because of the further developed worth of output transconductance and transconductance with a negligible reduction in cut-off frequency, the SM DGNCFET design has the highest GFP value. TFP reduces as V_g increases due to a rise in C_g, and when V_g reaches a saturation point, it maintains a minimal constant value. In terms of speed, transconductance, and gain, the SM DMNCFET is the best appropriate structure for TFP.

$$TFP = \left(\frac{g_{\rm m}}{I_{\rm d}}\right) \times F_{\rm t} \tag{6}$$

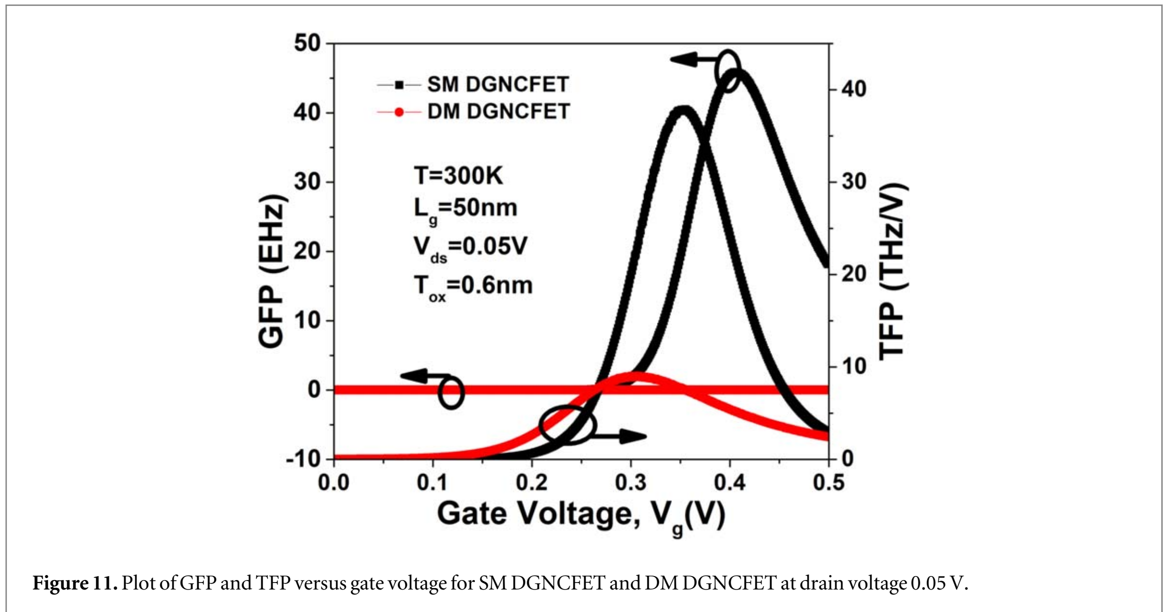

Figure 11. Plot of GFP and TFP versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

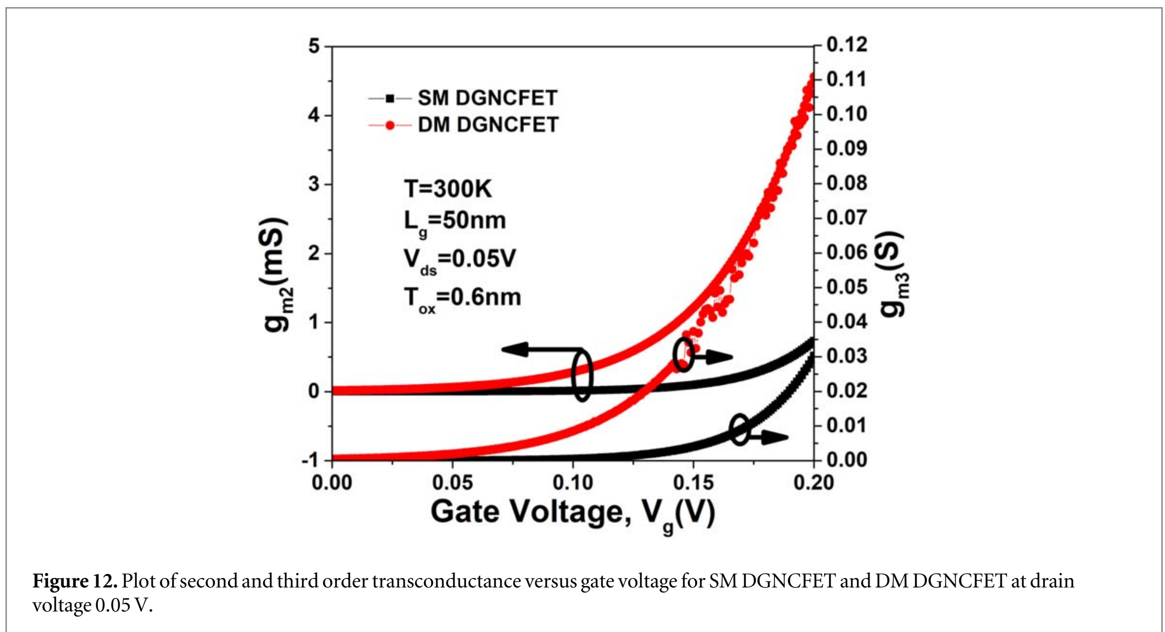

Figure 12. Plot of second and third order transconductance versus gate voltage for SM DGNCFET and DM DGNCFET at drain voltage 0.05 V.

$$VIP2 = \frac{4 \times g_m}{g_{\mathrm{m2}}} \tag{7}$$

$$VIP3 = \sqrt{\frac{24 \times g_{\mathrm{m}}}{g_{\mathrm{m3}}}} \tag{8}$$

4.1.3. Linearity parameter

Figure 12 exhibits second and third order transconductance versus gate voltage for SM and DM DGNCFETs at 0.05V drain voltage. Nonlinear characteristics are the major source of distortion, hence they must be investigated thoroughly. Nonlinear parameters should be kept to a minimum to attain high linearity. The nonlinear parameters (g_{m2}, g_{m3}) are for second- and third-order transconductance. The nonlinear parameters are nearly identical, indicating that increasing SM DGNCFET has little effect on them [31, 44]. The extrapolated gate voltage amplitude at which second- and third-order harmonics match the fundamental tone in device current is designated as VIP2 and VIP3 (I_{ds}). The distortion features of these FOMs may be precisely investigated using DC parameters. These values should be as high as feasible in order to achieve excellent linearity and minimum distortion.

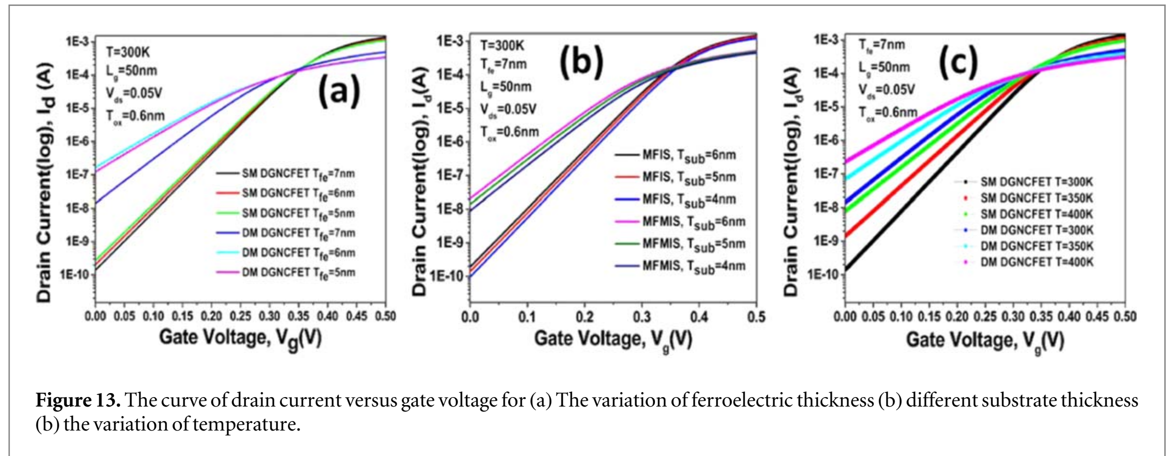

Figure 13. The curve of drain current versus gate voltage for (a) The variation of ferroelectric thickness (b) different substrate thickness (b) the variation of temperature.

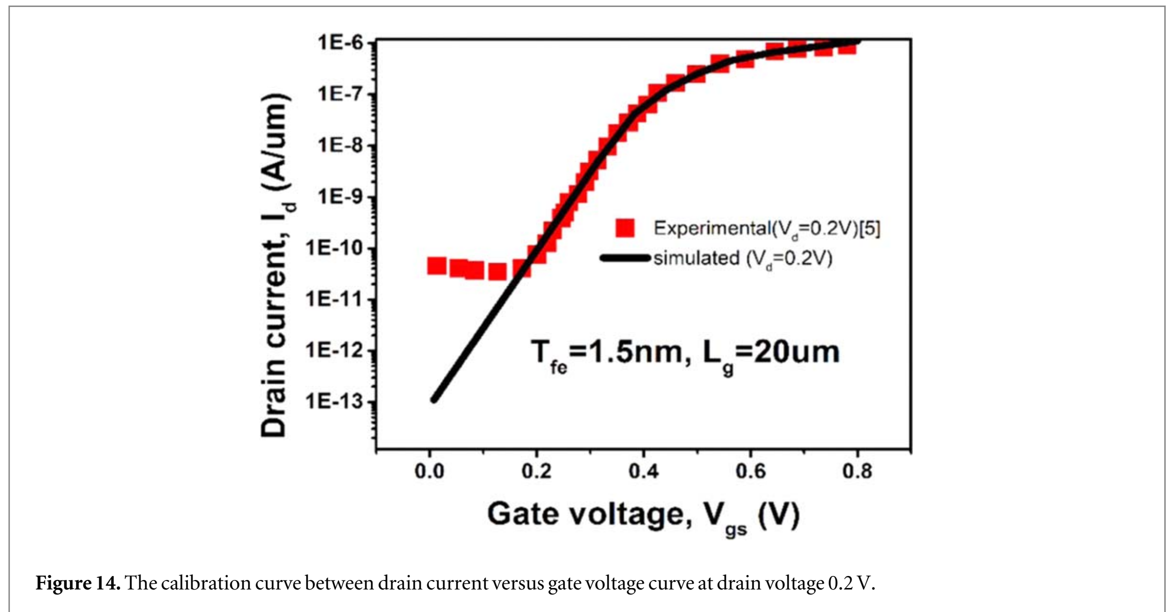

Figure 14. The calibration curve between drain current versus gate voltage curve at drain voltage 0.2 V.

4.1.4. Impact of variation of ferroelectric thickness, substrate thickness, and temperature

The comparison of two structures that is SM DGNCFET and DM DGNCFET. The variation of ferroelectric material thickness (T_{fe}) has been exhibits in figure 13 (a). The SM DGNCFET performance is higher improved than DM DGNCFET as increases the T_{fe}. The leakage current, switching ratio is better for SM DGNCFET at T_{fe} = 7 nm. The various substrate thickness (T_{sub}) is 6 nm, 5 nm, 4 nm where the leakage current lowered, switching ratio enhanced with decreases the substrate thickness(T_{sub} = 4 nm). The varing ferroelectric thickness T_{fe} is 5 nm, 6 nm, 7 nm where the performance of proposed device is improved at 7 nm. The various temperature has been exhibited in figure 13 (b). The drain voltage is same in entire simulation which is 0.05 V. The varying temperature (T) is 300 K, 350 K, 400 K where as the device performance of the SM DGNCFET is improved at 300 K due to reduced leakage current, increased gate controllability, low power consumption, higher switching ratio [17, 18].

Figure 14, represents the calibration of NCFET from the experimental data at gate length 20 um, ferroelctric thickness 1.5 nm and drain voltage 0.2 V. The experimental data extraction has taken from reference [5] to validate the physical model. The simulation models is validated due to the nearly agreement between the simulated and experimental results.

4.2. Impact of ferroelectric HfO_2 based crystal

In figure 15 exhibits the band structure for (a) Si doping (b) without doping. In the instance of HfO_2, it was discovered that 12.5% Si doping significantly altered the band gap along the direction, reducing the direct band gap to 0.20 eV and the indirect band gap to 0.193 eV with two-fold degeneracy (figure 15). The Si states may be blamed for the narrowing of the band gap. For all lower concentrations of Si, a comparable band gap changes along the direction, and the amplitude of the band gap grows monotonically as we proceed from x = 0.125 to

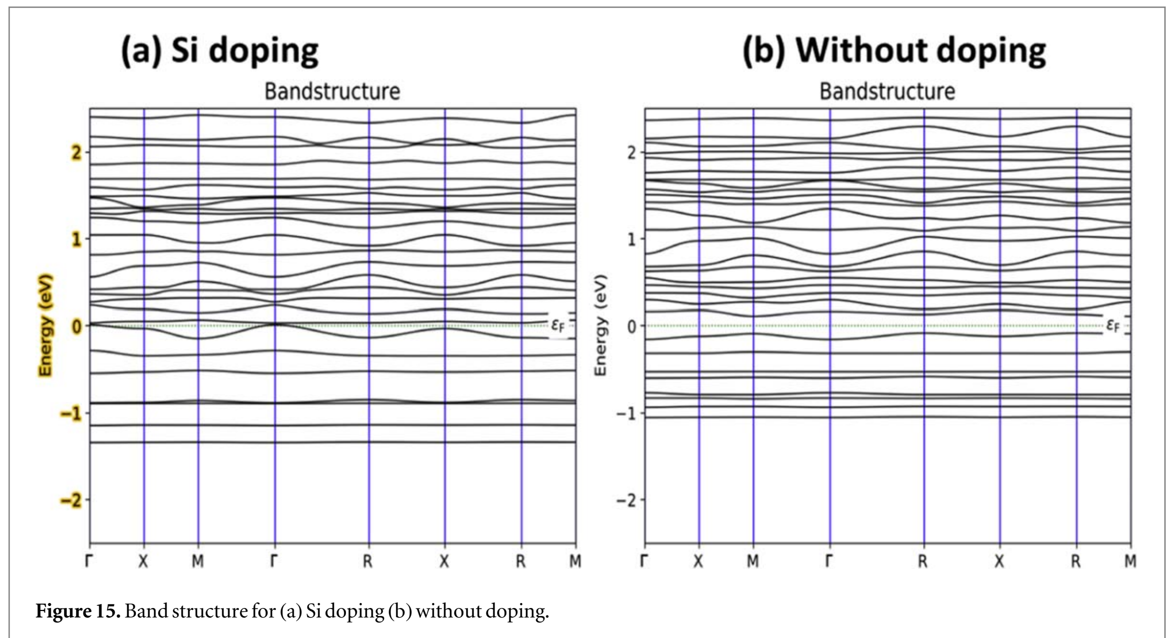

Figure 15. Band structure for (a) Si doping (b) without doping.

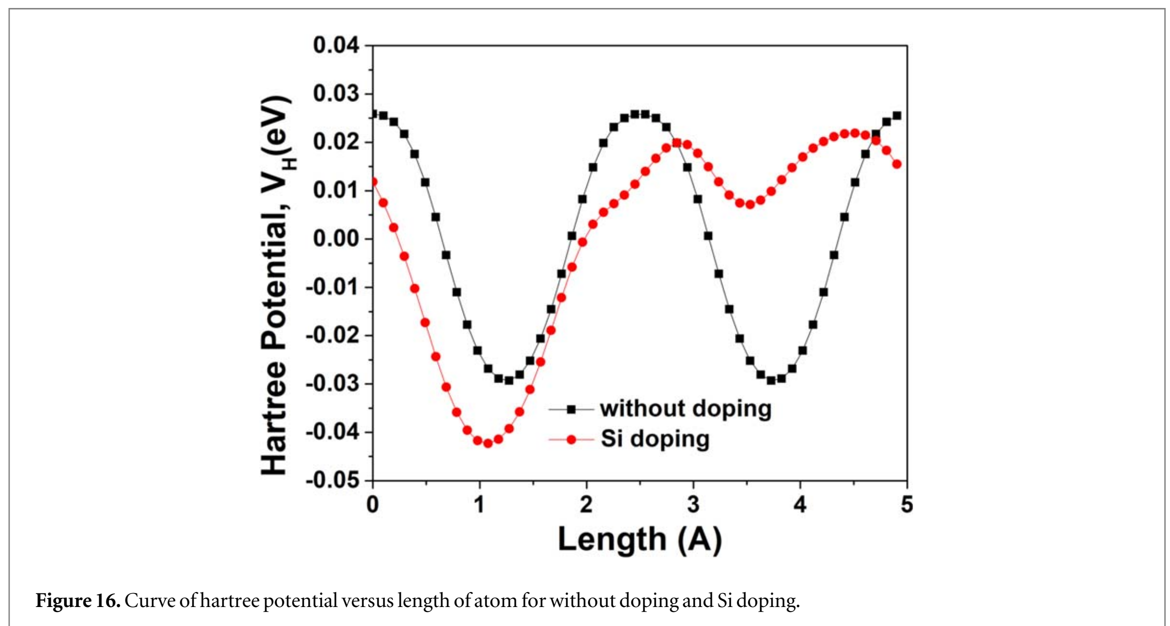

Figure 16. Curve of hartree potential versus length of atom for without doping and Si doping.

Table 3. Brillouin Zone (BZ) of specific path of ferroelectric HfO_2 based crystal for band stucture.

Value	Fractional, [K_x, K_y, K_z]	Cartesian(A^{-1})	Position along bandstructure, x
Gamma G	[0 , 0 , 0]	[0.0000, 0.0000, 0.0000]	0.0000e+00
X	[1/2, 0 , 0]	[0.3071, 0.0000, 0.0000]	1.1142e-01
M	[1/2, 1/2, 0]	[0.3071, 0.3071, 0.0000]	2.2285e-01
G	[0 , 0 , 0]	[0.0000, 0.0000, 0.0000]	3.8043e-01
R	[1/2, 1/2, 1/2]	[0.3071, 0.3071, 0.3071]	5.7342e-01
X	[1/2, 0 , 0]	[0.3071, 0.0000, 0.0000]	7.3100e-01
R	[1/2, 1/2, 1/2]	[0.3071, 0.3071, 0.3071]	8.8858e-01
M	[1/2, 1/2, 0]	[0.3071, 0.3071, 0.0000]	1.0000e+00

lower doping concentrations. Table 3 lists the Brillouin zone values along with their coordinates and symmetry K points for density function theory(DFT) study.

Figure 16 shows the curve examining the Hartree potential versus length for without doping and Si doping that revealed mean field electrostatic interaction between atoms. Electrostatic potential from electron density

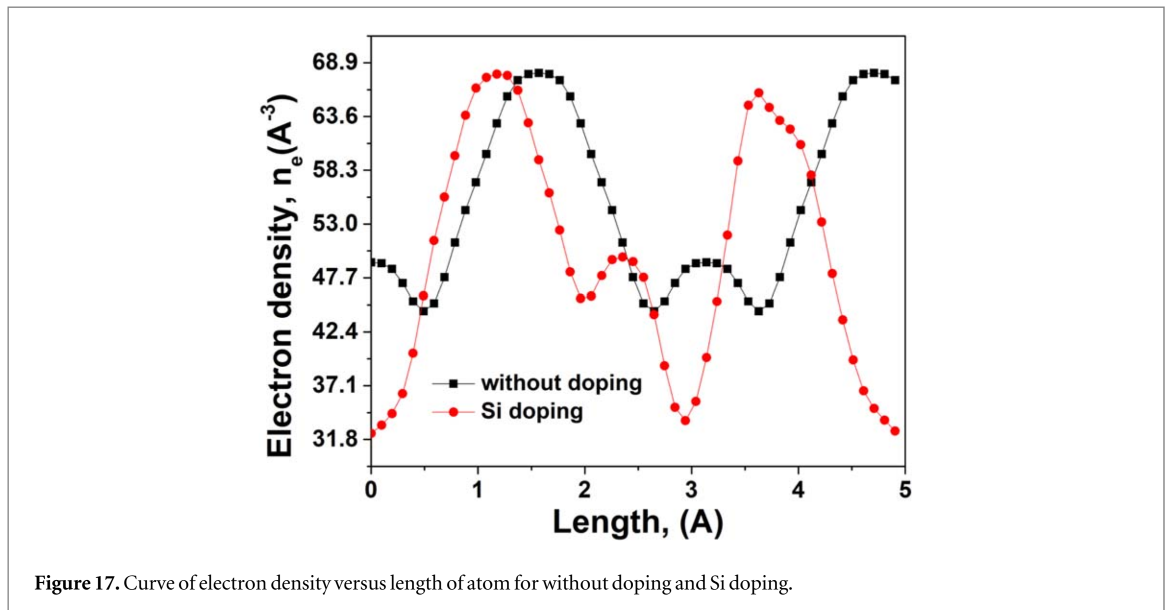

Figure 17. Curve of electron density versus length of atom for without doping and Si doping.

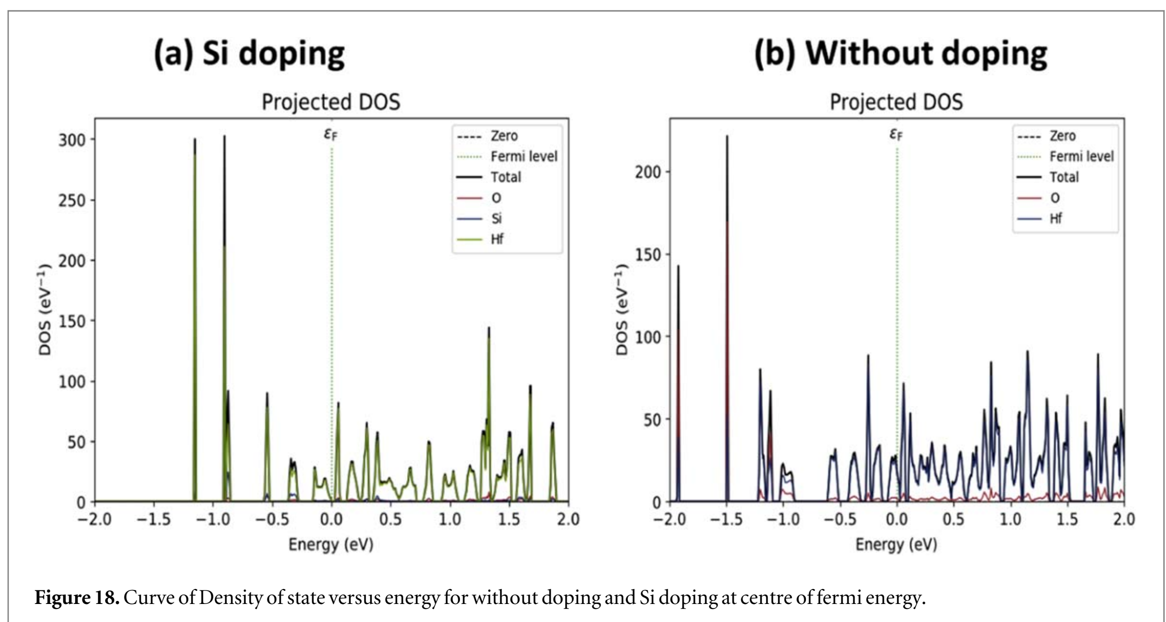

Figure 18. Curve of Density of state versus energy for without doping and Si doping at centre of fermi energy.

must be calculated using Poisson equation. Further, figure 17 exhibits the curve of electron density versus length for without doping and Si doping reflects proportional to square magnitude of wavefunction and the probability of electron or electron density being present at infinitesimal element of space. The collision time of Si doping is less for higher electron density.

In figure 18 reveals the curve examined the DOS(density of state) versus energy for without doping and Si doping at Fermi energy(E_f) reflects the conductivity enhanced with DOS increases and dispersion relation of properties of many system is available for occupation. We also examined the DOS(density of state) for all values of x to determine the influence of distinct atomic species on electronic structures (figure 18). In all doped structures, the contribution of different atoms in VBs(Valence bands) is found to be the same as in the pure c-HfO_2 phase, but the induced Si-states in lower CB occur between 0 and 0.5 eV. Si-states dominate over Hf and O-states at 0 eV, indicating the amount of hybridization. Because the number of atoms in the cell is exactly proportional to the doping concentration of Si in HfO_2, the magnitude of DOS grows as the doping concentration of Si in HfO_2 increases.

5. Conclusion

This paper addresses a comparative study of double metal double gate negative capacitance FET (DM DGNCFET) and single metal double gate negative capacitance FET (SM DGNCFET). SM DGNCFET reveals the better performance of Analog/RF and linearity such that DIBL, SS, transconductance, TFP, GFP, second and

third order of tranconductance (g_{m2}, g_{m3}). Atomic modeling for developments in quantum theory is the density functional theory (DFT), which aids to determine the energy, structure, and characteristics of materials, nanosystems, and molecules. Tran Blaha modified Becke Johnson (TB-mBJ) approxiamation gives the accurate band gap of crystal. The DFT study of hafnia(HfO_2) based Simple cubic crystal for without doping and 12.5% of Si doping. For improved results of Si the bandstructure better with band gap tends to zero, DOS enhanced for better conductivity.

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Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

Declarations

Funding statement

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Conflict of interests

The authors declare that they are not aware of any disagreements regarding personal ties or interests that might have impacted the work represented in this publication.

Authors' contribution

The comprehension and design of the study were improved by all writers.

Compliance with ethical standard

The authors have located all of the moral standards and intend to adhere to them going forward.

Consent to participate and for publication

Since that the relevant study paper was produced in the 'no-life science magazine'. Therefore, at this time, it is 'Non Applicable'. However, the authors have provided the agencies with all journal policies and their permission for additional processing.

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Experimental circuit design and TCAD analysis of ion sensitive field effect transistor (ISFET) for pH sensing

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ABSTRACT

In this work, we have investigated, both theoretically and experimentally, the analog study of the ion-sensitive field effect transistor (ISFET) and the circuit design for pH sensing. The gate electrode work function engineered on ISFET has been rigorously investigated for the analog/RF applications by using the Cogenda Visual TCAD tool. Based on its I–V characteristics, we may deduce that molybdenum, with a work function of 4.75 eV, has a larger threshold voltage, switching ratio (10^4) and lower leakage current (10^{-3}) than aluminum at 300 K. In addition, we experimentally investigated the enhancement in pH sensing. ISFET display instability, often referred to as drift, in the form of a gradual, monotonic, temporal increase in the device's threshold voltage. The validation of the observations was done by increasing the value of the pH as follows: 4.67, 5.9, 7.5, 8.57, and 9.3 which was checked by pH meter.

1. Introduction

Bergveld first unveiled the Ion Sensitive FET in 1970 [1], which is sometimes referred to as a solid state device that incorporates the chemical sensitivity displayed by semiconductors, a membrane and a FET's field-sensing capacity. The benefits of ISFETs go beyond their small form factor, resilience, as well as relatively affordable production costs, but enable the implementation of advanced smart CMOS-based integrated circuit-based sensor systems. However, threshold voltage instability is also a result of drift, ISFET-based biosensors have not gained popularity and a leading position in the industry. Drift is distinguished by a unidirectional, slowly changing temporal pattern in the threshold voltage, and consequently, the concentration of the provided ion does not change in the drain current of ISFET [2].

The MOSFET idea provides the foundation of ISFET. The metal gate of the MOSFET is replaced by the ISFET construction with a pH sensor layer. This film is used to monitor the activity of ions in the analyte while being in direct contact with the electrolyte. The ion concentration in the electrolyte modulates the current that passes through the transistor's channel [3]. The gate area dimensions and the sensor film both affect the device's sensitivity. The sensing layer of the ISFET is more interesting for the researchers, and they have looked at numerous insulators including Silicon Dioxide (SiO_2), Tantalum Pentoxide (Ta_2O_5), Silicon Nitride (Si_3N_4), and other dielectrics including Aluminum Oxide (Al_2O_3) as sensing film [4].

The chemical interactions between the ISFET gate dielectric on one side and the electrolyte on the other side which creates the surface charge density that makes the ISFET sensitive to pH value [5,6]. In a standard ISFET structure, a sensor membrane known as gate oxide is in direct contact with the solution. This location is relative to the area of the total sensor and alters the ISFET electrical behavior because the measurements of the ISFET's sensitivity are hampered by the presence of the parasitic capacitance feature. The surface charge potential at the surface of an ISFET is activated by protonation and deprotonation processes between the surface and the floating gate, to develop the coupling capacitance. The floating gate of ISFET is modulated by this potential, threshold voltage V_T for chemical, biological sensing [7]. The development and description of the ISFET sensitivity are on website dissociation models by Yates [6].

In the article, the silicon nitride is used as sensing film to reflect the sensitivity for different materials of gate electrode such as Molybdenum, Aluminum, Chromium with their work function 4.75 eV, 4.3 eV,

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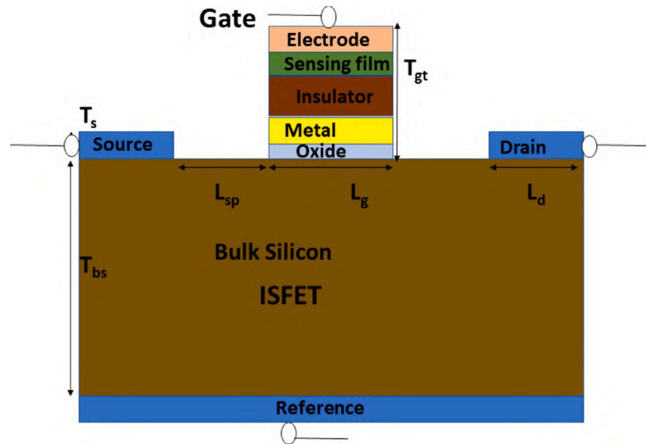

Fig. 1. Sketch diagram for TCAD design of ISFET structure.

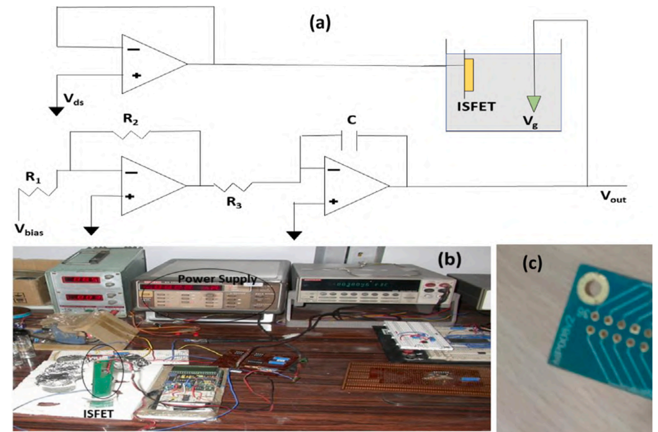

Fig. 2. (a) The experimental Circuit diagram of pH sensor-based structure by using 3 op amp A1, A2, A3. (b) experimental setup (c) MP008v2 ISFET.

4.1 eV as given in Table 2. The work function (4.75 eV) electrode, the smaller leakage current, lower subthreshold swing [8], lower input power, decreased drain-induced barrier lowering usage, and management of the gate channel device [9–12]. The transistor channel's source and drain diffusion's extended 100 nm. The double-layer insulator was made up of a film of thermally generated SiO_2 that was 10 nm thick, on top of which a layer of 65 nm thick, Si_3N_4 was produced using the usual chemical vapour deposition process, which relied on the reaction between aluminum bromide and water vapour. There was no threshold-setting ion implantation. The drift characteristics of n-channel were measured on gate pH sensitive ISFETs creating a technique described above.

ISFET is FET to apply for measuring the ion concentration in solution. The updated value of pH, the fluid of body indicates the medical issue. The important component for detection of pH disease such as high sensitivity, fast respond, robustness, very small disease, ability to collect & transmit data in real time [13,14]. For circuit design, the apparatus is utilized such as ISFET, op amp, power supply, resistor, pH value capsule, PBS solution, multimeter. By using the circuit design as shown in Fig. 2, which enables the preservation of a constant drain current by delivering a feedback voltage to the electrolyte, room temperature. ISFET drift data was gathered in the feedback mode. In the absence of back bias, the drain current was set at I_d = 100 mA using a constant drain to-source voltage. Using a commercial Calomel reference electrode dipped in a phosphate buffer saline with a pH of 7, the ISFET gate voltage was applied. The validation of observation was done by increasing the voltage with a higher value of pH 4.67, 5.9, 7.5, 8.57, and 9.3.

2. Design for device and circuit

2.1. Device architecture of ISFET

Fig. 1 shows the sketch diagram of the ISFET by using the TCAD tool. The drain current equation is same for both MOSFET and ISFET as exhibited in (1).

$$I_{\mathrm{d}} = \frac{\mu \times C_{\mathrm{ox}} \times W}{L} \times V_{\mathrm{ds}} \times [(V_{\mathrm{g}} - V_{\mathrm{t}}) - \frac{(V_{\mathrm{ds}})}{2}] \quad (1)$$

Here, the threshold voltage is V_t, width, and length of the channel are W, L respectively (see Table 2).

The dimension of ISFET is designed in Fig. 1, bulk silicon region consists of silicon with a length of 500 nm and thickness of 400 nm. Drain/ Source consists of aluminum with length 30 nm and thickness 100 nm, reference consists of aluminum with length 500 nm and thickness 20 nm, oxide layer consists of SiO_2 with length 180 nm and thickness 10 nm, electrode consists of aluminum with length 180 nm and thickness 40 nm, sensing film consists of Si_3N_4 with length 180 nm and thickness 10 nm [15]. The mobility model is used as an analytical tool in the bulk silicon area as described by Shockley–Read–Hall (SRH) theory for trap charge [7,16–19]. MOSFET's Lombardi surface mobility model for electron mobility influences recombination and it is presence at the point of contact and the connection between two particles is described by the Fermi-Dirac mathematical formula. The usage of insights leads to precision. Focus affects the mobility of the Arora model. The gaussian doping concentration is 1×10^{20} cm^{-3} for drain and source with the donor as shown in Table 1.

Table 1
ISFET device parameter for TCAD simulation.

Parameter	ISFET
Temperature	300 K
Channel length (L_c)	180 nm
Oxide thickness (T_{ox})	10 nm
Length of drain/ source ($L_{d/s}$)	100 nm
Thickness of drain/source ($T_{d/s}$)	30 nm
Doping concentration of drainsource	1×10^{20} cm^{-3}
Width of gate (T_{gt})	130 nm

Table 2
The table used for the work function of different materials on electrode.

Material	Work function ϕ (eV)
Molybdenum	4.75
Chromium	4.3
Aluminum	4.1

2.2. Structure for experimental circuit design

The apparatus utilized for circuit design is as follow: sodium monohydrate phosphate (Na_2HPO_4) and sodium dihydrogen phosphate (NaH_2PO_4) were purchased from Sigma Aldrich. ISFET was purchased from LioniX international site, three 8 pin operational amplifier, wires, 3 resistors, capacitor, multimeter, 9 V power supply, a voltage divider. MP008v2 ISFET as shown in Fig. 2(c), 22uf capacitor, R1 100 Ω,R2 1 KΩ, R3 100 Ω, op 07CN an operational amplifier as shown in Fig. 2.

This section reveals the ISFET drift in context of the inversion layer's constant, temporal decline charge density to support the drift counteraction, depending specifically on the closed shape. We shall create an equation for the gate voltage drift [20–22], changing the charge density at the insulator interface, which can be used to create a useful gadget for way of counteracting drift [2].

3. Simulation study of ISFET and circuit design

3.1. Simulation study of ISFET device

The Visual TCAD tool is used to make ISFET device theoretically. We have optimized the comparison study of different materials of the gate electrode for ISFET such as Molybdenum, Chromium, and Aluminum with their different work functions 4.75 eV, 4.3 eV, 4.1 eV respectively. The drain voltage, V_{ds}(V), is maintained constant at 0.5 V, the gate voltage, V_g(V) ranges from 0 to 3 V. The temperature (T) is maintained at 300 K in all circumstances throughout the process for the device simulation. SiO_2 is used as gate dielectric in ISFET passivation of silicon, which reduces the charge recombination, increase water oxidation, protects semiconductor from chemical corrosion. Gate dielectric as SiO_2 supports electric field invert the type of charge carrier in MOSFET channel and turn the device ON.

Although the extent of chemical modification of the aluminum oxide surface as determined by the thickness of the modified surface layer can be significantly less than that of the silicon nitride surface, it is still thought that chemical modification of the insulator surface is the cause of the drift observed in Si_3N_4-gate pH-sensitive ISFETs [16,17]. The dielectric constant of the changed surface layer will be different from that of the bulk insulator as a result of chemical alteration of the insulator surface. As a result, the total insulator capacitance will gradually decrease over time as surface modification continues. This capacitance is defined by the series combination of the capacitance of the changed surface layer and that of the underlying insulator [2,23].

Interface trap affects the device performance. It is a trap between oxide layer and semiconductor (e.g. silicon). This effect is a defect and imperfection at the interface. It may release and capture the charge carrier and cause changes in the transistor behavior. The trap at interface is localized at oxide and semiconductor interface. It is nearly mid gap area of energy band structure of Si. The energy level may be at edge of band gap and within band gap that affects the threshold voltage control and the carrier transport. During semiconductor manufacturing and device design, strategies are used to minimize the negative consequences of traps in MOSFETs. To reduce mesh density and energy levels, they include process passivation layers, optimization, and the use of premium materials [24].

3.2. Technique for experimental circuit design

When the ISFET is replaced with a equilibrium reference electrode ions mixture, they bind the passivation or decay charge recombination, protect semiconductor from chemical corrosion, causing an accumulation of charge which in turn bais the threshold voltage of the device [25]. ISFET threshold voltage is dependent on pH of the device which shifts as manifested in Eq. (2). Here the term E_{ref} is reference potential, x_{sol} is potential for dipole moment in existing solution, ψ_0 is chemical potential of pH. All the terms of the chemical reaction grouped in potential are represented in Eq. (3). In Eq. (4), γ is potential for non chemical grouping, and α range from 0 to 1 [26].

$$V_{\mathrm{th(ISFET)}} = E_{\mathrm{ref}} - \psi_0 + x_{\mathrm{soi}} - \frac{\phi_{\mathrm{m}}}{q} + V_{\mathrm{th(mosfet)}} \tag{2}$$

$$V_{\mathrm{chem.}} = E_{\mathrm{ref}} - \psi_0 + x_{\mathrm{soi}} - \frac{\phi_{\mathrm{m}}}{q} \tag{3}$$

$$V_{\mathrm{chem.}} = \gamma + \frac{2.3\alpha kT}{q} pH \tag{4}$$

The apparatus used for this purpose of experimental circuit design is: pH capsules, PBS solution for different pH values, wire, operational amplifier, resistor, capacitor, pH meter, and multimeter. The Faradaic process on electrochemistry helps the electron transfer across the metal (electrode) to solution interface. There is also the process of oxidation and reduction occurring as per which charge will flow from the electrode. The procedure for making the pH capsule solution, is applied a power supply of 9 V and 1 A, and dissolving a capsule with pH 4 in 50 ml deionized water to make the solution pH 4.67 at 5 min. Dissolve the second capsule of pH 4 in 50 ml deionized water to make the solution of pH 5.9. Dissolve a capsule of pH 7 in 50 ml deionized water to make the solution of pH 7.5. Dissolve a capsule of PH 9 in 50 ml deionized water to make the solution of pH 9.3. For making the phosphate buffer saline solution, mix the solution of sodium monohydrate phosphate (Na_2HPO_4) and sodium dihydrogen phosphate (NaH_2PO_4) for making the solution, add Ferro and Ferri in 100 ml solution as reflected in Fig. 2.

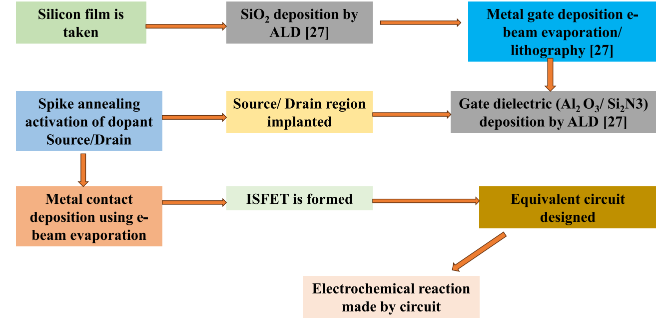

Fig. 3. The flowchart of device feasibility from ISFET to circuit design.

3.3. Fabrication feasibility from ISFET to circuit design

Fig. 3 shows the device fabrication feasibility from ISFET to circuit design. Visual TCAD simulator has reported on the viability of fabricating ISFET. First, silicon film deposition is thinning out. The atomic layer deposition (ALD) on silicon substrate, and Al_2O_3/Si_3N_4 layer has been created on the metal interface layer [27]. The gate metal is created by utilizing the electron beam evaporation method on the gate dielectric. The activation of the spike annealing dopant is inserted in the source and drain regions by lift-off process. Hence, defines the ISFET fabrication process. The circuit is designed by using the ISFET device.

4. Result and discussion

Firstly, we have seen the analog and RF parameter of pH-ISFET for various work function (ϕ) to improve the performance of leakage current, subthreshold swing, DIBL etc. ISFET is used for pH sensing circuit enhanced compatible CMOS technology. ISFET circuit for biosensing at low power supply when brought in weak inversion. ISFET circuit can merge with MOSFET and standard transistor of integrated circuits.

4.1. Comparative study of ISFET for different work function

Fig. 4 reflects the graph of gate voltage vs. drain current on primary axis and log drain current on secondary axis for different materials of gate electrode with their work function of ISFET design at drain voltage, V_{ds} = 0.5 V, temperature T = 300 K. The molybdenum with work function 4.75 eV has improved result than aluminum, and chromium. Mo has better results which indicated superior gate coupling capacitance and lower leakage current (I_{off}) on the left side of the graph.

The transconductance is a ratio of drain current vs. gate voltage, V_g as shown in Fig. 5 to show the better performance of transconductance for molybdenum. The g_m is defined as shift in drain current vs. gate voltage [28], which indicates improved gate control and reduced short channel effects, as well as increased average carrier velocity and improved electron mobility with increased transconductance. TGF is

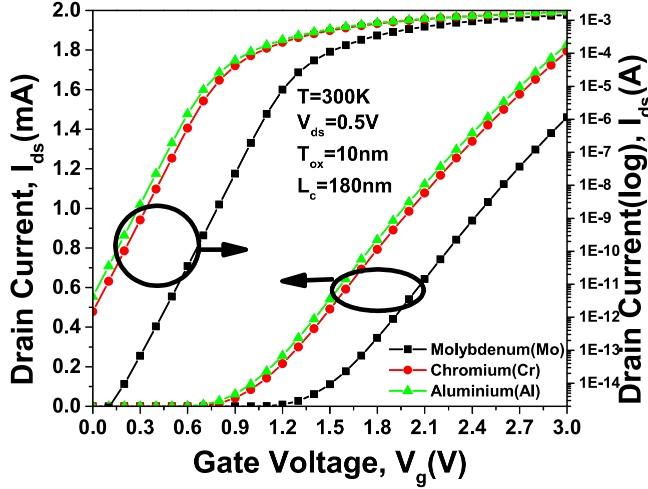

Fig. 4. I_{ds} - V_g characteristics on the left side and log drain current on the right side for different materials of electrode ISFET design at Vds = 0.5 V, T = 300 K.

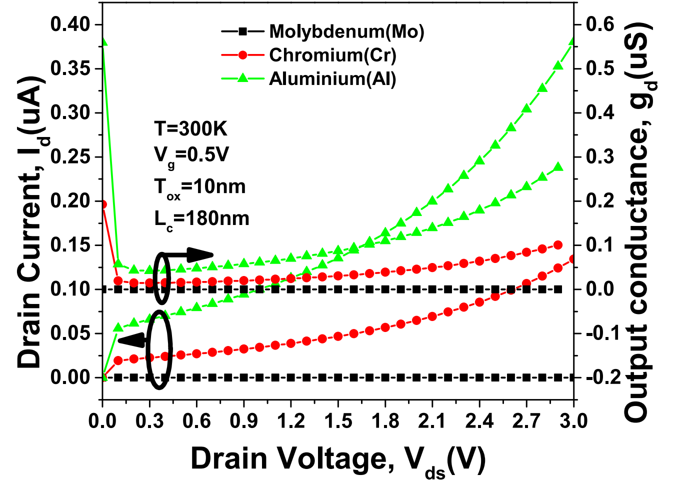

Fig. 6. I_{ds} - V_{ds} characteristics in the left side and output conductance on the right side for different materials of electrode ISFET design at Vg = 0.5 V, T = 300 K.

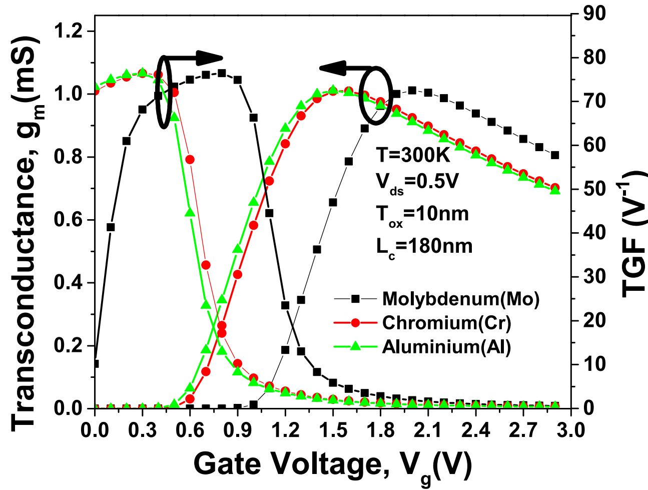

Fig. 5. g_m - V_g characteristics in left side and TGF on the right side for different materials of electrode ISFET design at Vds = 0.5 V, T = 300 K.

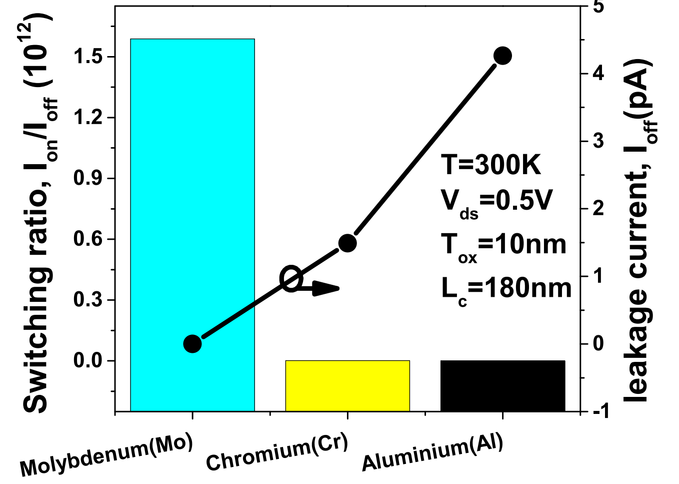

Fig. 7. The plot of switching ratio on the left side and leakage current on the right side for different materials of electrode ISFET design at Vds = 0.5 V, T = 300 K.

Table 3
ISFET comparison for different work function materials such as molybdenum, chromium, and aluminum.

Parameter	Molybdenum (Mo)	Chromium (Cr)	Aluminum (Al)
I_{on} (A)	0.00146	0.00179	0.00183
I_{off}(pA)	0.000919	1.4911	4.266
$I_{on}/I_{off}(10^{10})$	158.86	0.12004	0.04289
V_{th} (mV)	1	0.6	0.5
SS (mV/dec.)	104.8	106.78	107

shown on the right side of figure which is ratio of g_m and I_{ds}, It also shows better effective performance of device in case of molybdenum.

$$g_m = \frac{\partial I_{ds}}{\partial V_g} \tag{5}$$

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{6}$$

Fig. 6 exhibits the graph of drain voltage vs. drains current on the left side and output conductance (g_d) on the right side for different materials of gate electrode ISFET design at V_g = 0.5 V, and T = 300 K. The performance of output conductance for the molybdenum is better than others such as aluminum, chromium. The rise at drain voltage beyond pinch-off voltage, a high output conductance in the linear region is first seen due to drain induced barrier lowering (DIBL) and channel length modulation (CLM) [15,29]. As demonstrated in Fig. 6, the molybdenum's g_d twist is less than Al and Cr, indicating better gate controllability and the capacity to inhibit short direct strikes.

$$V_e = \frac{I_{ds}}{g_d} \tag{7}$$

$$A_v = \frac{g_m}{g_d} \tag{8}$$

Fig. 7 reveals the plot of switching ratio (I_{on}/I_{off}) on the left side and leakage current (I_{off}) on the right side for different materials of gate electrode ISFET design at V_{ds} = 0.5 V, T = 300 K. For Molybdenum lower leakage current and higher switching ratio, which is inversely proportional to leakage current gives better performance of the short channel effect and is directly proportional to ON current.

Fig. 8 reveals the plot of threshold voltage (V_{th}) on primary axis and subthreshold swing (SS) on secondary axis for different materials of gate electrode ISFET design at V_{ds} = 0.5 V, T = 300 K. The enhanced threshold voltage and lower SS for Molybdenum than other materials such as Aluminum, Chromium which means to enhance gate controllability and reduce short channel effect, which suggests that

Table 4
Comparison of output voltage and sensitivity from previous data.

Reference	Year	Device platform	pH	V_{out}	Sensitivity
[30]	2005	ISFET based Microsystem	6	0.042	1.4
[30]	2005	Aluminum-gate-FET (ALUFET) ISFET	5	1.25	Na
[31]	1997	Diamond like carbon (DLC) gate ISFET	5	0.035	Na
[32]	2008	Electrolyte insulator semiconductor (EIS) device	4	−0.4	Na
This work	Present	Silicon nitride ISFET	6	0.051	1.7
This work	Present	Silicon nitride ISFET	5	0.045	1.5

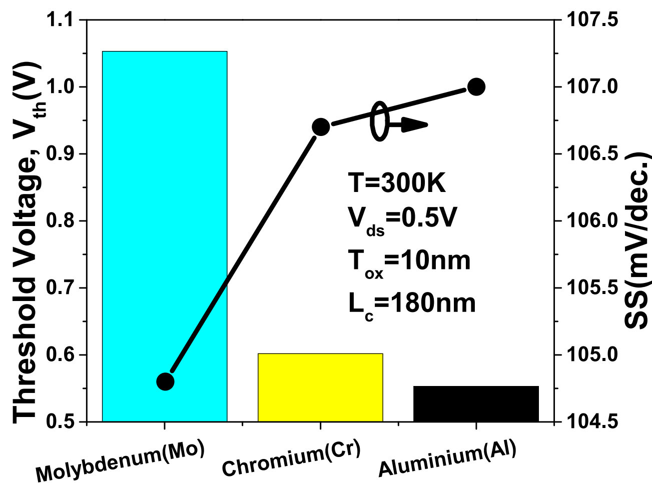

Fig. 8. The plot of threshold voltage on the left side and subthreshold swing on the right side for different materials of electrode ISFET design at Vds = 0.5 V, T = 300 K.

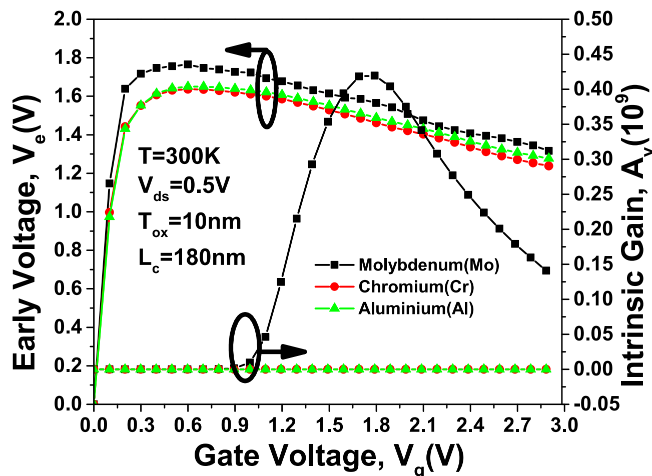

Fig. 9. V_{ea} - V_g characteristics on the left side and intrinsic gain on the right side for different materials of electrode ISFET design at Vds = 0.5 V, T = 300 K.

when the channel length is reduced, electrons can move easily from source to drain. For lower SS, it shows a result of an improved gate control over the channel and enhanced gate coupling capacitance with work function (ϕ). Fig. 9 reveals the graph of gate voltage vs. Early voltage (V_e) on left side and intrinsic gain (A_v) on the right side for different materials of gate electrode ISFET design at V_{ds} = 0.5 V, T = 300 K. Molybdenum material reflects the which show declined short channel effects. The greater transconductance values and lower output conductance result in higher intrinsic gain values.

Gate control over the channel has enhanced drain-side potential barrier. The switching ratio I_{on}/I_{off} of molybdenum is greater than that of the other structures due to the nature of the threshold voltage at L_c = 180 nm, T_{ox} = 10 nm. At T = 300 K and V_{ds} = 0.5 V, the molybdenum with work function 4.75 eV structure similarly achieves reduced leakage current I_{off} (A) and quick switching speed, as shown in Table 3. The previous data of reference [30–32] are compared with present work in term of output voltage and sensitivity. For sake of briefing, the sensitivity and output voltage of ISFET in present work is improved than reference at pH 5, 6 [30] as presented in Table 4.

The calibration of ISFET is validated in Fig. 10(a), (b). Fig. 10(a) exhibits the validation of ISFET between TCAD simulation study and reference [33] . The drain current of this validation is −1.5 V at gate length 10 um and width 100um. It is an p-type ISFET at gate voltage range 0-(−8)V. Fig. 10(b) reveals the calibration study of ISFET between TCAD simulation and reference [34]. The drain voltage of this validation is 0.1 V at temperature of 300 K. It is an N-type ISFET with gate voltage range 0–2.5 V

4.2. Experimental circuit of ISFET

The Levenberg–Marquardt nonlinear extraction procedure was used to determine the parameters' extracted values, which offer a very excellent match to the recorded drift data and are contained within their physically appropriate ranges. But some of these characteristics must be determined independently through experiments for a more thorough validation of the drift model. Modern surface characterization methods, for instance, may be used to determine the ultimate thickness of the changed surface layer after exposing the pH-sensitive insulator to an electrolyte for a sizable amount of time. The unique circuit architecture involving the ISFET is also provide the counter drift through simple adjustment of voltage and reduce flicker noise [35–37]. A flicker noise is charge carrier trapped and released between the interface of materials.

Fig. 11(a) reflects the curve of pH value vs. output voltage in pH capsule solution for pH based ISFET. Voltage is improved with increasing pH value, the different value of pH capsule solution pH 4.67, 5.9, 7.5, 8.57, 9.3. Fig. 11(b) exhibits the curve of sensitivity vs. output voltage in pH capsule solution for pH based ISFET. The unit of sensitivity is dimensionless. A typical ISFET device's electrostatic behavior (transfer characteristics) is modeled. To provide the 9 V voltage convert into 7 V and 2 V by using voltage divider. 2 V voltage was supplied to make the current in 3 mA by using 10 μf capacitor and resistor. The operational amplifier is used to amplify the signal 3 mV to 1 V. Draining to source current I_d vs. reference gate voltage $V_{Ref.}$ for sensing film gate oxide layer has been measured at varied pH values. Sensitivity is improved at higher pH value [38–40].

Fig. 12(a) exhibits the variation of pH value vs. output voltage in PBS (phosphate buffer saline) solution for pH based ISFET device. Applied voltage 9 V and current 1 A cross through the breadboard circuit, it lead to divide the voltage by voltage divider and stored some current in 10 μF capacitor to pass the current operational amplifier as shown in Fig. 3. The phosphate buffer saline solution enhanced the sensitivity at higher pH value shown in Fig. 12(b).

5. Conclusion

This work addresses the comparative study of materials for various gate electrification progress of ISFET with their work function and circuit design experimentally. Molybdenum with work function 4.75 eV

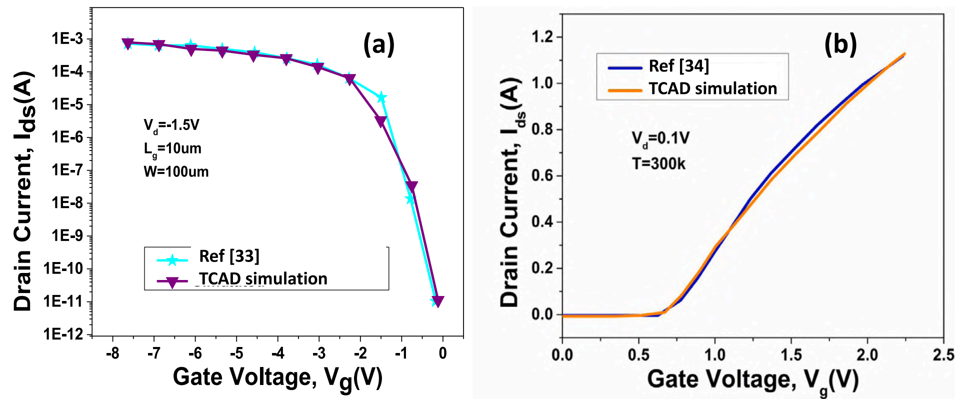

Fig. 10. The calibration of ISFET from references.

Fig. 11. (a) The graph of pH value vs. output voltage in pH capsule solution for pH based ISFET (b) The curve of sensitivity vs. output voltage in pH capsule solution for pH based ISFET.

Fig. 12. (a). The variation of pH value vs. output voltage in PBS(phosphate buffer saline) solution for pH based ISFET device (b) The variation of Sensitivity vs. output voltage in PBS (phosphate buffer saline) solution for pH based ISFET device.

shows improved results than others like aluminum, chromium. Molybdenum has reduced the leakage current 10^{-3} times from aluminum, higher the switching ratio, decayed the subthreshold swing, and enhanced some analog parameters found in ISFET like transconductance, TGF, g_d. Theoretically, we concluded that molybdenum has proved to be an efficient material for fabrication of ISFET using silicon nitride as sensing layer at different gate electrode. ISFET design has shown significant progress in terms of accuracy, and reduction in component count in size, lower cost, more efficiency. 6-pin ISFET is being successfully manufactured for enhancing voltage at high pH 4.67, 5.9, 7.5, 8.57, 9.3 checked by pH meter. Consequently, the findings of this research can assist engineers in designing nanoelectronic devices that meet their requirements.

CRediT authorship contribution statement

Yash Pathak: Conceptualization, Methodology, Software, Material preparation, Data collection and analysis, Writing - original draft, Writing - review & editing. **Piyush Mishra:** Data curation, Visualization, Writing - review & editing. **Megha Sharma:** Data curation, Visualization, Writing - review & editing. **Shipra Solanki:** Data curation,

Visualization, Writing - review & editing. **Ved Varun Agarwal:** Supervision, Writing - original draft. **Rishu Chaujar:** Supervision, Writing - original draft. **Bansi Dhar Malhotra:** Supervision, Writing - original draft.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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Compliance with ethical standard

The authors have located all of the moral standards and intend to adhere to them going forward.

Consent to participate & for publication

Since that the relevant study paper was produced in the "no-life science magazine". Therefore, at this time, it is "Non Applicable". However, the authors have provided the agencies with all journal policies and their permission for additional processing.

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PAPER

Performance evaluation of gate engineered ferroelectric MIMOS for analog/electrical IC applications

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Abstract

This work examines various materials for gate electrode for enhancing the performance of M-Fe-MIMOS (Metal Ferroelectric Metal Insulator Metal Oxide Semiconductor Field Effect Transistor (MOSFET)). The device is analysed for different analog, electrical and RF parameters with gate materials such as chromium, tungsten and palladium. The gate stacked attached to MOSFET device consists ferroelectric layer sandwiched with insulator for focusing on reliability and stability of M-Fe-MIMOS. The palladium gate material for M-Fe-MIMOS(spacer) shows better analog parameters such as improvement in leakage current by 106 times that results 107 times higher switching ratio as compare to chromium. Also with higher threshold voltage by 428% and lower subthreshold swing by 340% as compare to chromium, M-Fe-MIMOS(spacer) shows better immunity towards various noise distortions. The electrical properties of the device are analysed in terms of electric field , electric potential and energy band structure.All the analysed results indicate that palladium as a gate material for the M-Fe-MIMOS shows most improved electrical performance and can further be used for various applications in nanoelectronic devices and integrated circuit (IC) design.

1. Introduction

The power and thermal management of integrated circuits (ICs) are more vital aftercare for transistor industry. Although with engineering technology and material science advancement transistor generates the low amount of heat. However, the ICs have millions of transistors on chip which generate huge amount of heat. Thus, the reduction of supply voltage (V_{dd}) is vital technique to solve the problem. Power factor depends upon square of supply voltage ($P_{dyn} \alpha V_{dd}^2$). The scaling of supply voltage for conventional MOSFET reached 60mV/dec. (fundamental limit) and cannot be lowred using methods that is known as Boltzmann Tyranny [1]. The negative capacitance might work to provide high on current and subthreshold swing lower than 60mV/dec. Recently the phenomena of negative capacitance has been demonstrated in different systems experimentally such as (i) superlattice (ii) ferroelectric dielectric bilayer (iii) isolated ferroelectric film [2, 3].

Due to its lower supply voltage, tunnel FETs have also been cited by many research organizations in the semiconductor world as the ideal replacement for traditional MOSFETs for future low-power applications. In order to fulfill the needs of ultra-low power ICs, the idea of NC has been adopted and used in MOS devices [4, 5]. According to the literature available , NCFET technology has the ability to address the drawbacks of traditional MOS technology. Additionally, it offers superior characteristics particularly SS in compare to other devices like TFET and IMOS. Because NCFET devices operate at lower supply voltage than IMOS and do not suffer from low on-state drain current [6, 7].

Channel length scaling does not cause much degration M-Fe-MIMOS due to negative capacitance phenomena well accommodated in the ferroelectric layer of device. Furthermore, the final model merely applies the Landau parameters to the outside-of-plane polarisation component, which is unreasonable for materials

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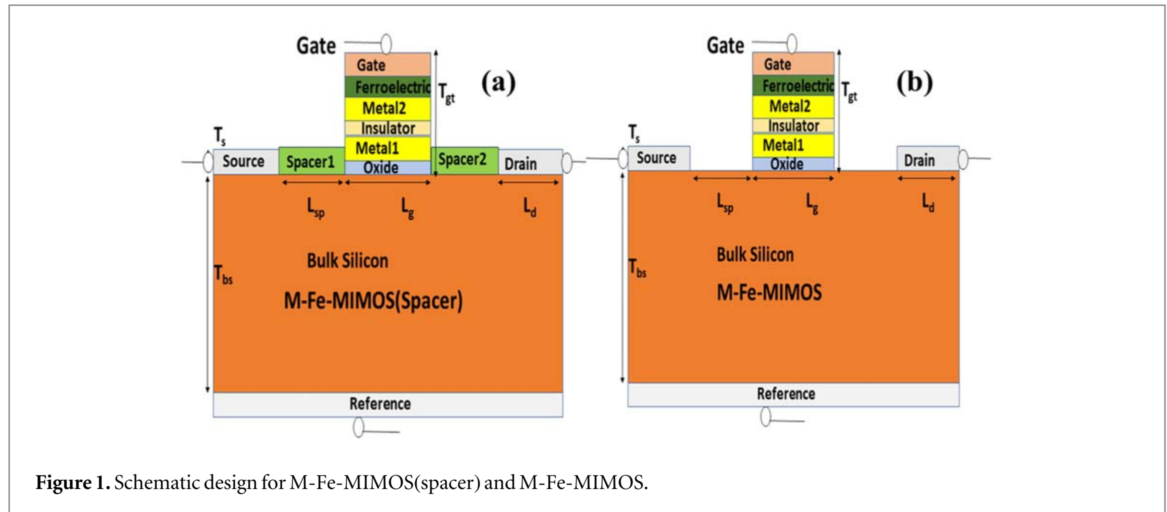

Figure 1. Schematic design for M-Fe-MIMOS(spacer) and M-Fe-MIMOS.

with large ferroelectric thicknesses [8], $\alpha = 1.0 \times 10^{+7}$, $\beta = 8.9 \times 10^{+8}$ and $\gamma = 0$ [9]. The L-K and Miller models are often used to elucidate the polarisation (P) and voltage across ferroelectric (FE) materials. However, L-K has received greater recognition. This section has focused on the L-K model. The LandauKhalatnikov (LK) equation is a dynamic formulation of the LandauDevonshire theory as shown in equation (1). The LK equation is a very useful tool for comprehending the ferroelectric switching features in the development of NCFET technology. The landau theory of non linear dielectric is given below in equation (1):

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP,\ \alpha = \alpha_0[T - T^0] \quad (1)$$

Here, G is free energy density, α, β, γ are landau coefficients, P is polarisation, E is electric field [10, 11].

In our earlier studies, we have done extensive investigation to analyse how the M-Fe-MIMOS with long channels work [12, 13], giving the degradation of the device in terms of low switching speed, high leakage current, high power consumption. M-Fe-MIMOS(spacer) provides a greater ON-state flow compared to M-Fe-MIMOS, however we have found that it is not true for all ferroelectric materials. Additionally, the text still lacks for clear explanation of the real conduct of the two structures and a general performance analysis.

The energy required to transfer an electron from the Fermi level to the vacuum is known as the work function. In FETs, the work function of the gate material influences the threshold voltage, thereby improving channel control. A double metal NCFET device uses two distinct metals for the gate electrode. This structure allows for more accurate fine-tuning of the work function and optimization of the threshold voltage for enhanced performance [14]. Optimizing the performance of double metal NCFETs for both analog and digital applications necessitates an understanding of the variations in work function. By carefully selecting materials and designing the gate stack, it is possible to significantly enhance transconductance, threshold voltage, subthreshold slope, and overall device efficiency [15, 16].

This article describes an improved field effect transistor with a ferroelectric layer that operates at room temperature (T = 300 K) with several performance advantages over other MFMIMOS transistors, including low input power consumption, reduced drain induced barrier lowering, reduced subthreshold swing, reduced leakage current, and better control over gate channel device[17]. Visual TCAD simulator was used to derive the device performance matrix. The I_{off} in this M-Fe-MIMOS (spacer) is lying in the realm of 10^{-11}A, means less leakage and more working life of device, which is the requirement for better performance. At off-state (i.e., at $V_{gs} = 0$), the M-Fe-MIMOS has improved both Ion and depletion channel width. Through this investigation, we learn more about the device for better analog execution and power amplification performance, when M-Fe-MIMOS(spacer) and M-Fe-MIMOS are compared analogically and virtually.

2. Device Structure

Figure 1 shows schematic diagram of the proposed device, metal ferroelectric metal insulator mosfet with spacer (M-Fe-MIMOS (spacer)) and conventional device, M-Fe-MIMOS. The length of bulk silicon (L_b), Drain/Source ($L_{d/s}$), Spacer1/Spacer2 (L_{sp}) are 60 nm, 10 nm, 8 nm respectively. The thickness of Drain/Source ($T_{d/s}$), Bulk Silicon (T_{bs}), oxide layer (T_o), ferroelectric layer, metal1, metal2, insulator layer are 3 nm, 50 nm, 1 nm, 1 nm, 2 nm, 1.7 nm, 2.3 nm respectively. The total gate thickness is denoted by T_{gt}. The material of bulk silicon, source/drain/gate, metal1, oxide layer, ferroelectric layer is Silicon (Si), Aluminum (Al), Au, Silicon dioxide (SiO_2), HfO_2FE, respectively. M-Fe-MIMOS (spacer) and M-Fe-MIMOS have similar architecture except 2 layers of spacers. The material of spacer1/spacer2 is NpolySi. The uniform doping concentration of bulk silicon

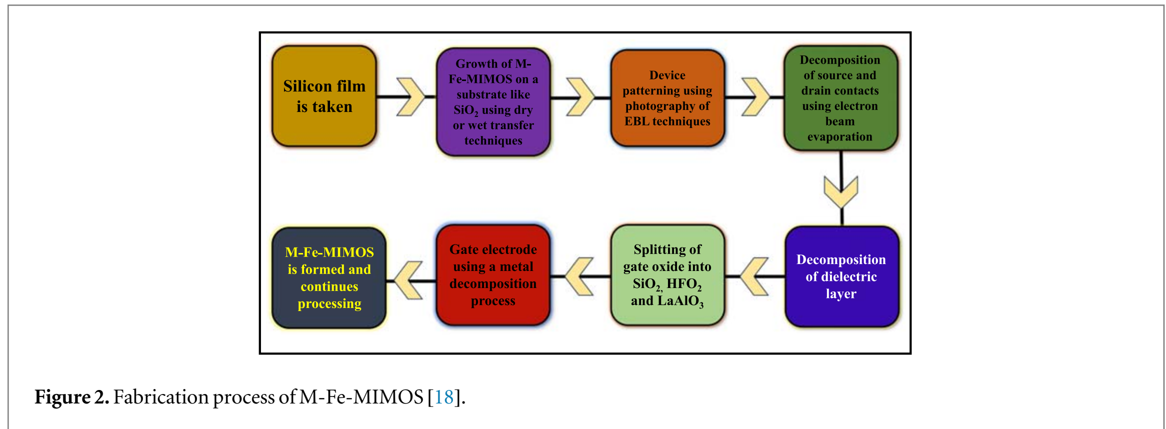

Figure 2. Fabrication process of M-Fe-MIMOS [18].

Table 1. M-Fe-MIMOS device parameter for TCAD simulation.

Parameter	M-Fe-MIMOS (Spacer)
Temperature	300 k
Channel length (L_g)	20 nm
Oxide thickness (T_o)	1 nm
Length of drain/ source ($L_{d/s}$)	12 nm
Thickness of drain/source ($T_{d/s}$)	3 nm
Doping concentration of drainsource	1×10^{21} cm^{-3}
Total width of gate (T_{gt})	130 nm

Table 2. The various material with its work function.

Material	Work function ϕ (eV)
Chromium	4.3
Tungsten	4.55
Paladium	5.3

is 1×10^{16} cm^{-3} with acceptor type. The gaussian doping concentration of drain/source ($N_{d/s}$) and threshold voltage (N_v) is 1×10^{21} cm^{-3} with donor type, 1×10^{18} cm^{-3} with acceptor type correspondingly as shown in table 1. The metal1 work function is maintained at 5.3 eV.

The equation of drain current equation of MOSFET is exhibited in equation (2).

$$I_{\rm d} = \frac{\mu \times C_{\rm ox} \times W}{L} \times [(V_{\rm g} - V_{\rm t}) - \frac{(V_{\rm ds}) \times (V_{\rm ds})}{2}] \quad (2)$$

Here, the threshold voltage is V_t, and width, length of the channel are W, L respectively, μ is mobility of n type, C_{ox} is capacitance of oxide, V_g, V_t, V_{ds} are the gate, threshold, drain voltage [19, 20].

3. Simulation study of M-Fe-MIMOS(spacer)

Cogenda Visual TCAD(Technology Computer Aided Design) system is used for entire validation. In this study, the variation of work function for palladium, chromium, tungsten has been analyzed in gate material. The voltage of drain (V_d) and temperature (T) is secured at 0.4V and 300 K. The range of gate voltage (V_{gs}) is different from 0 to 4V. he L-K and Miller models are often used to elucidate the polar- isation (P) and voltage across ferroelectric (FE) materials [10, 11]. The field dependent mobility model (FLDMOB) is used for computing the mobility, concentration-dependent mobility (CONMOB) [21, 22], polarization model, Shockley-ReadHall (SRH) recombination model [23, 24]. We have explored the various work function (ϕ) such as 4.3 eV for aluminum, 4.55 eV for Chromium, 5.3 eV for palladium as shown table 2.

The fabrication process is shown in figure 2. The visual TCAD simulator has reported the feasibility of fabricating M-Fe-MIMOS. Firstly, the silicon film is thinned. Next, the Al_2O_3/HfO_2 layer is deposited on the silicon interfacing layer via atomic layer deposition (ALD) [18]. Finally, the metal gate is formed on the gate

dielectric via electron beam evaporation process. The dopants of the source and drain region are implanted by spike annealing activation. Finally, the electron beam is evaporated on the surface of the source and drain, resulting in the formation of M-Fe-MIMOS.

4. Result and discussion

4.1. Effect of electrical performance on M-Fe-MIMOS

We have explored the electrical parameter of M-Fe-MIMOS such as electric field distribution over the channel, max. electric field, potential across channel, quasi fermi potential, band structure for all gate electrodes. We studied the electric field distribution over channel means the electric field is in vertical direction. The drain voltage is fixed at 0.4V with variation in gate voltage. The electric field distribution across channel exhibits almost homogeneous distribution, when device is in linear region. The device is in saturation region, when the electric field took M-shape. The electric field (E) at drain side is higher for palladium as depicted in figure 3 than source area, which reflect the better control at channel in linear region[17]. The curve of E near source is better than channel due to the electron collected under oxide layer to make the reverse bais, leads the potential difference higher thus, increases the electric field (E). The peak of E is higher at drain side for better voltage stress as shown in figure 4. The plot of potential versus position along channel are shown in figure 5 for various gate layer of M-Fe-MIMOS at $V_{gs} = V_d = 0.4$ V. The potential and electric field of palladium is higher than other gate electrode at drain side as shown in figure 5(b), when device is in biased or active condition. The max. electric field and potential for palladium gate electrode are improved by 141% and 0.002% as compared to chromium gate electrode. The potential is higher at drain side, which reveals better flow of current and smooth amplification of signal in ON state (conducting).

The maximum and 'M' shaped electric field profile in M-Fe-MIMOS (spacer) devices for the palladium gate electrode arises from the combined effects of gate-channel interactions, channel potential variations, ferroelectric material mobility, short channel effects, and design/material heterogeneities. These factors create a complex electric field distribution that enhances device performance by optimizing control over the channel and improving transconductance [25–28]. Figure 6 reflects the quasi fermi potential versus position along channel for different gate electrode at $V_{gs} = V_d = 0.4$ V and T = 300 K. The quasi fermi potential of palladium is higher than others electrode, when FET is in non equilibrium and biased condition. The quasi fermi potential for hole and electron may shift from equilibrium position on applying the external bias. The ntype FET is observed for rising the electrons by applying quasi fermi level [29, 30]. Figure 7 exhibits the energy band structure versus position along channel at $V_{gs} = V_d = 0.4$ V and T = 300 K for various gate electrode. The band gap of palladium is 1.1 eV, which is lower than chromium 1.12 eV. Valence band gap (E_v) and conduction band gap (E_c) are extracted along channel as depicted in figure 7. The device performance and static parameter is improved for palladium.

4.2. Analog and switching parameter

Figure 8 reflects the drain current, I_d versus gate voltage, V_{gs} at constant $V_d = 0.4$ V for various work function of M-Fe-MIMOS (spacer) and M-Fe-MIMOS. The drain current for M-Fe-MIMOS (spacer) with palladium is higher than others such as chromium, tungsten. The M-Fe-MIMOS (spacer) represents decreased leakage current than M-Fe-MIMOS in linear drain current graph, that reveals enhanced the gate effect to control the channel. Figure 9 shows the gate voltage versus transconductance on left side of graph and device efficiency on right side of graph at $V_d = 0.4$ V. Transconductance (g_m) is ratio of drain current and gate voltage. The g_m of M-Fe-MIMOS (spacer) for palladium is improved than chromium, tungsten. Also, the g_m of M-Fe-MIMOS (spacer) is higher than M-Fe-MIMOS, which reveals upgraded electron mobility, better gate controllability, increase average carrier velocity, reduced short channel effect (SCEs). TGF is gain generated by power loss. Transconductance Generation factor (TGF) of M-Fe-MIMOS (spacer) for palladium is enhanced as compare to other work functions (ϕ) [31–33], which reflects improved device efficiency tht is close to ideally 50 V^{-1}. The TGF is higher that shows the more g_m [34]. The high transconductance and device efficiency of M-Fe-MIMOS arise from their strong gate control over the channel, high carrier mobility, and material/structural enhancements. These factors collectively enable NCFET to achieve significant changes in drain current with small changes in gate voltage, making them highly efficient and effective for a wide range of electronic applications [35, 36].

For digital circuit, the operation of transistor takes place in linear region, while for analog circuit, the operation of transistor is in saturation region ($V_d = V_{gs} = 0.4$ V) [37, 38]. The electric field distribution is studied by tuning V_{gs} for different operating situation. The breakdown time of channel is lower at higher electric field. The breakdown of time dependent equation (t_b) is given below in equation (3):

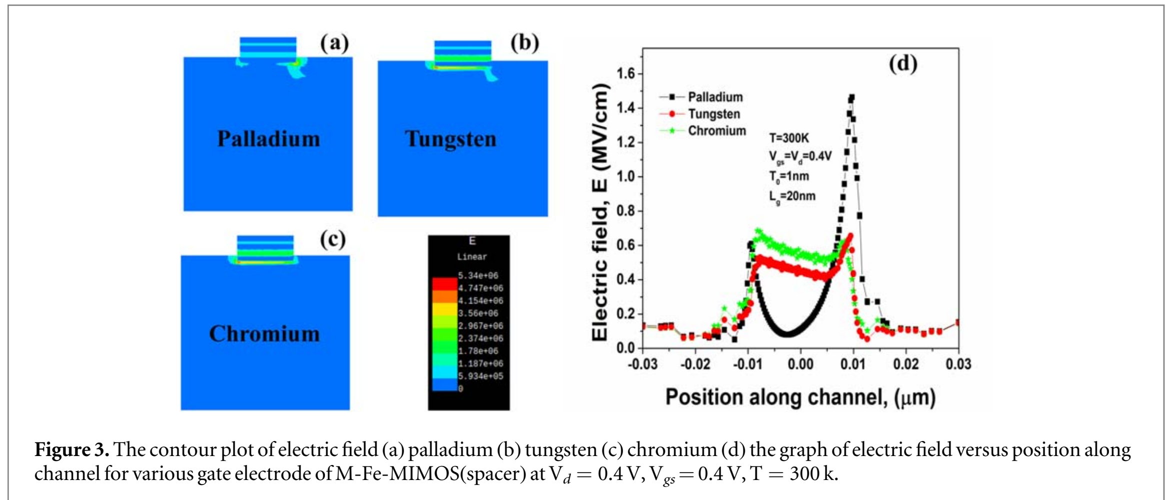

Figure 3. The contour plot of electric field (a) palladium (b) tungsten (c) chromium (d) the graph of electric field versus position along channel for various gate electrode of M-Fe-MIMOS(spacer) at $V_d = 0.4$ V, $V_{gs} = 0.4$ V, T = 300 k.

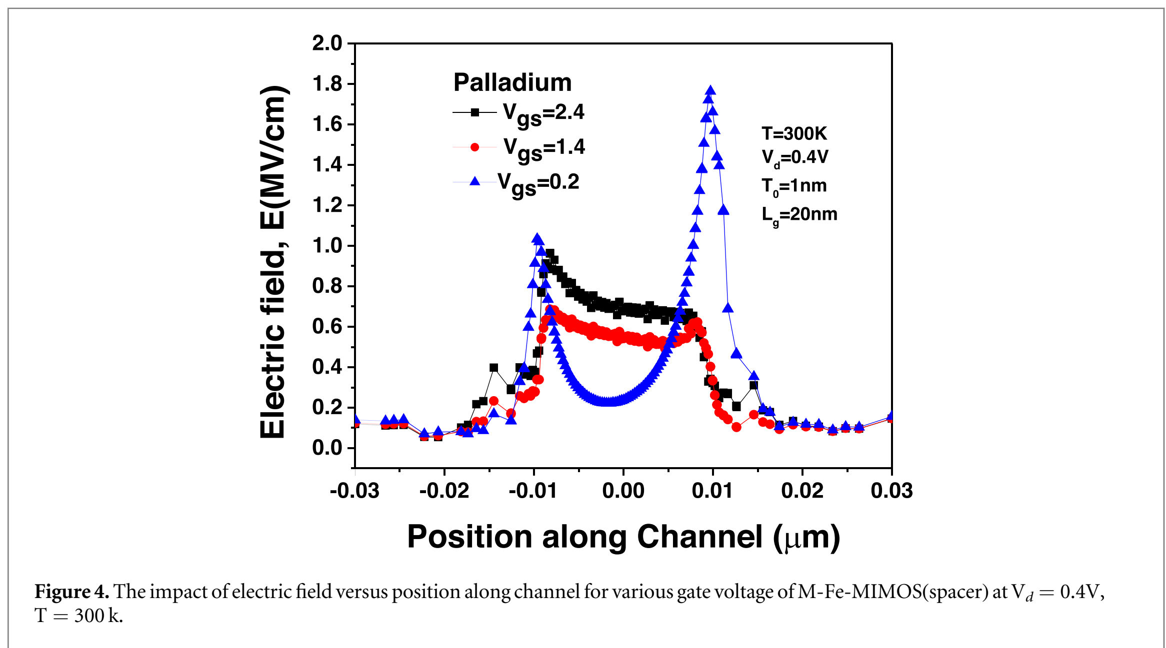

Figure 4. The impact of electric field versus position along channel for various gate voltage of M-Fe-MIMOS(spacer) at $V_d = 0.4$V, T = 300 k.

$$t_b = Aexp(-\gamma E_o)\frac{E_a}{K_b T}. \tag{3}$$

Here, A is electric field acceration, γ is proportionality constant, T is absolute temperature, E_a is thermal activation energy, E_o is oxide electric field, K_b is Boltzmann constant [17, 39].

Figure 10 shows the gate voltage versus leakage current (I_{off}) on left side of graph and switching ratio (I_{on}/I_{off}) on right side of graph at $V_d = 0.4$ V for various work function.The I_{off} of M-Fe-MIMOS (spacer) for palladium is lower than chromium, tungsten. The I_{off} of M-Fe-MIMOS (spacer) is also decreased as compare to M-Fe-MIMOS, that exhibits the lower leakage current. The Y axis has two sides of the plot. The left part of the arrow represents the leakage current and the right part of the arrow represents the switching ratio. The I_{on}/I_{off} of M-Fe-MIMOS (spacer) for palladium is better than chromium, tungsten. The I_{on}/I_{off} of M-Fe-MIMOS (spacer) is higher than M-Fe-MIMOS, that affect the switching speed of device and lower leakage current as shown in table 3. Figure 11 shows the gate voltage versus threshold voltage (V_t) on left side of plot and subthreshold swing (SS) on right side of plot at T = 300K, $V_d = 0.4$ V for different work function. The threshold voltage (V_t) of M-Fe-MIMOS (spacer) for palladium is better than chromium, tungsten. The V_t of M-Fe-MIMOS (spacer) is also higher than M-Fe-MIMOS, which reveals better potential shield at drain side better potential shield, increased gate controllability over channel. The subthreshold swing (SS) of M-Fe-MIMOS (spacer) for palladium is less than chromium, tungsten. The SS of M-Fe-MIMOS also reflects decrement as compare to M-Fe-MIMOS, which shows lower short channel effect i.e. drain barrier induced lowering (DIBL).

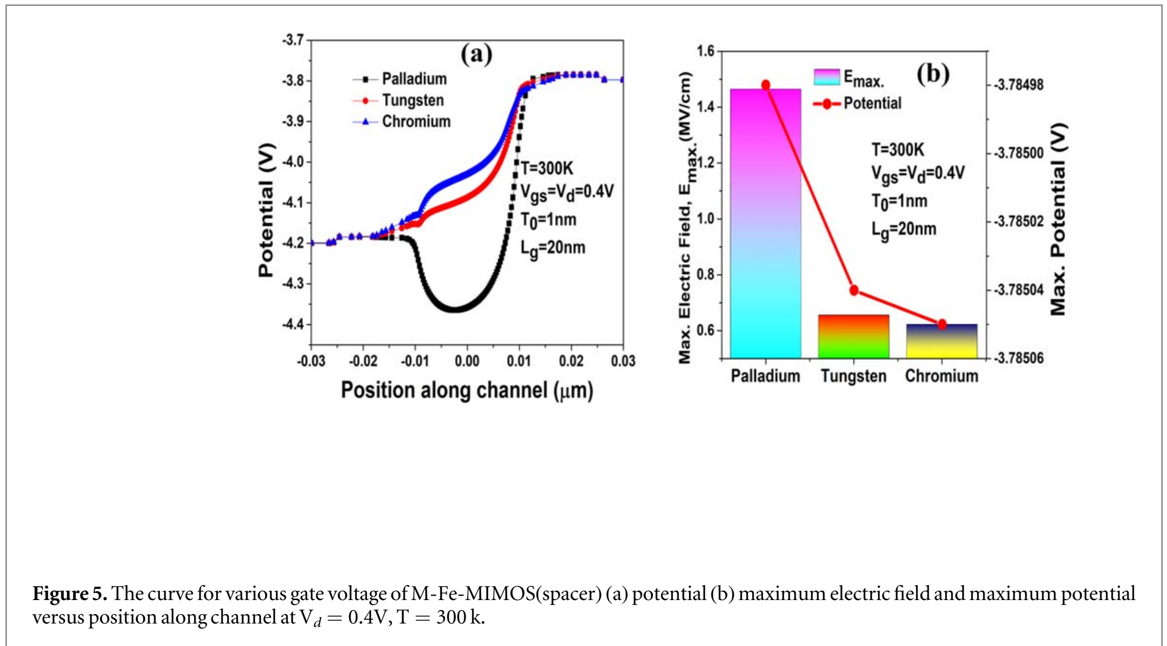

Figure 5. The curve for various gate voltage of M-Fe-MIMOS(spacer) (a) potential (b) maximum electric field and maximum potential versus position along channel at $V_d = 0.4V$, $T = 300$ k.

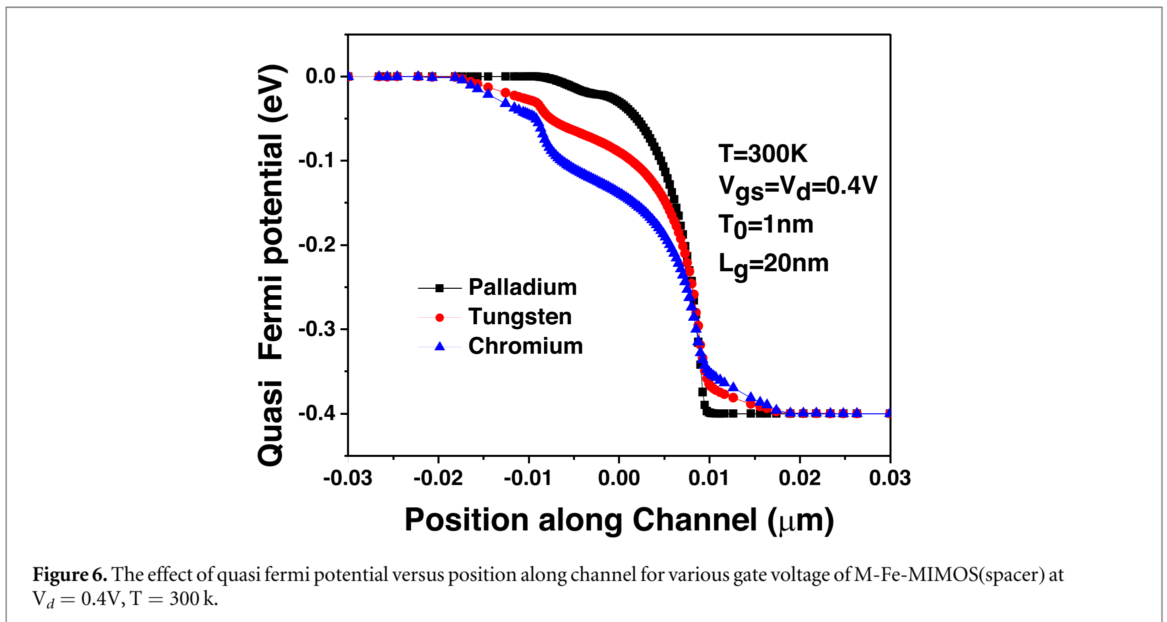

Figure 6. The effect of quasi fermi potential versus position along channel for various gate voltage of M-Fe-MIMOS(spacer) at $V_d = 0.4V$, $T = 300$ k.

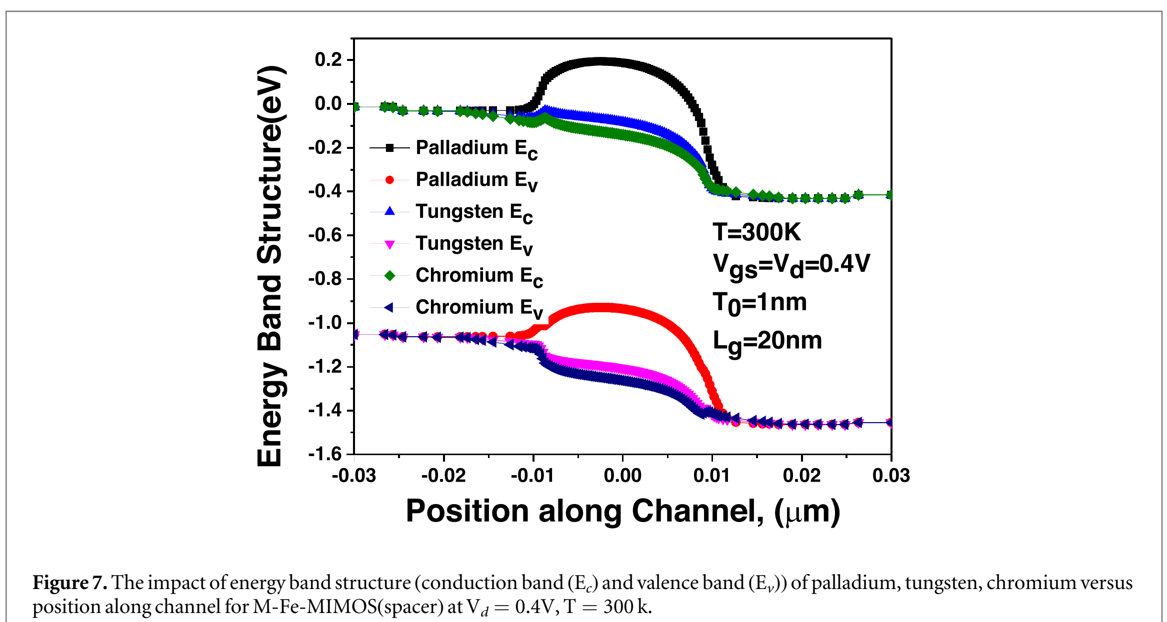

Figure 7. The impact of energy band structure (conduction band (E_c) and valence band (E_v)) of palladium, tungsten, chromium versus position along channel for M-Fe-MIMOS(spacer) at $V_d = 0.4V$, $T = 300$ k.

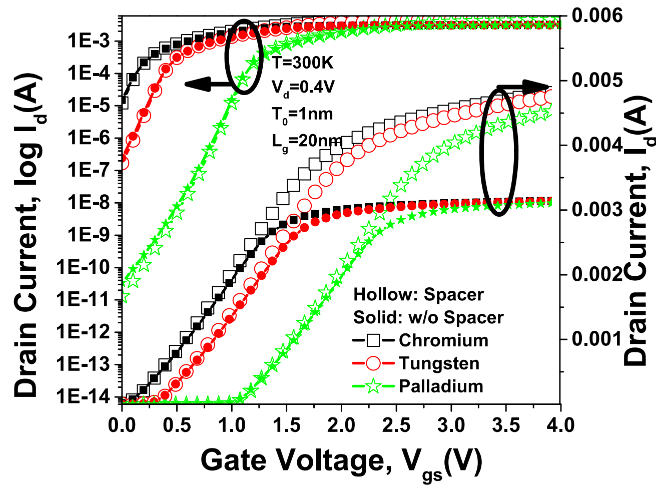

Figure 8. The Plot of I_d versus V_{gs} for 3 work function of M-Fe-MIMOS at $V_d = 0.4$ V.

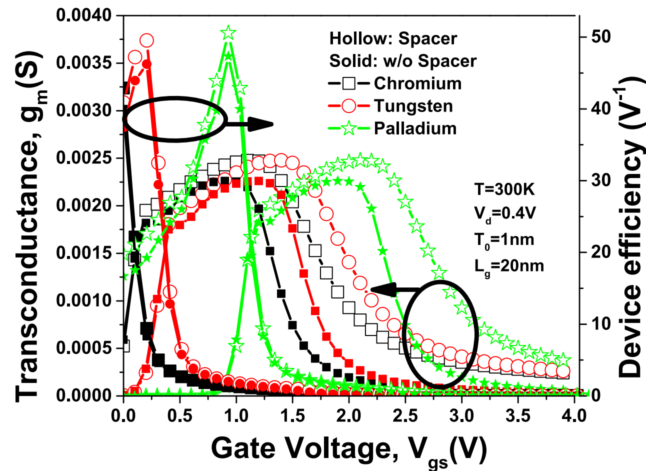

Figure 9. The graph of transconductance and device efficiency versus V_{gs} for 3 work function of M-Fe-MIMOS at $V_d = 0.4$V.

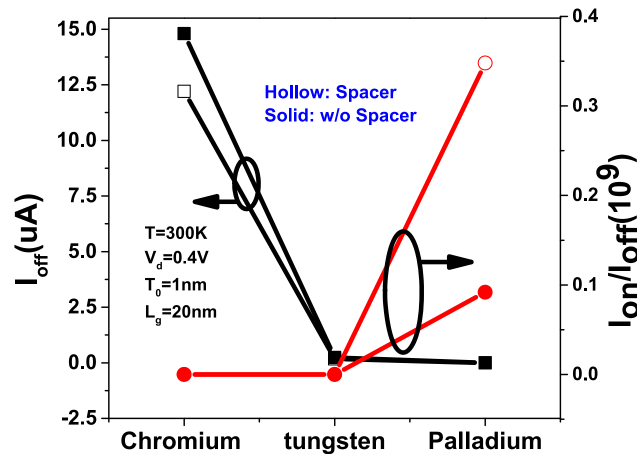

Figure 10. The Plot of gate voltage versus leakage current and switching ratio for different work function of M-Fe-MIMOS(spacer) at $V_d = 0.4$ V, T = 300 k.

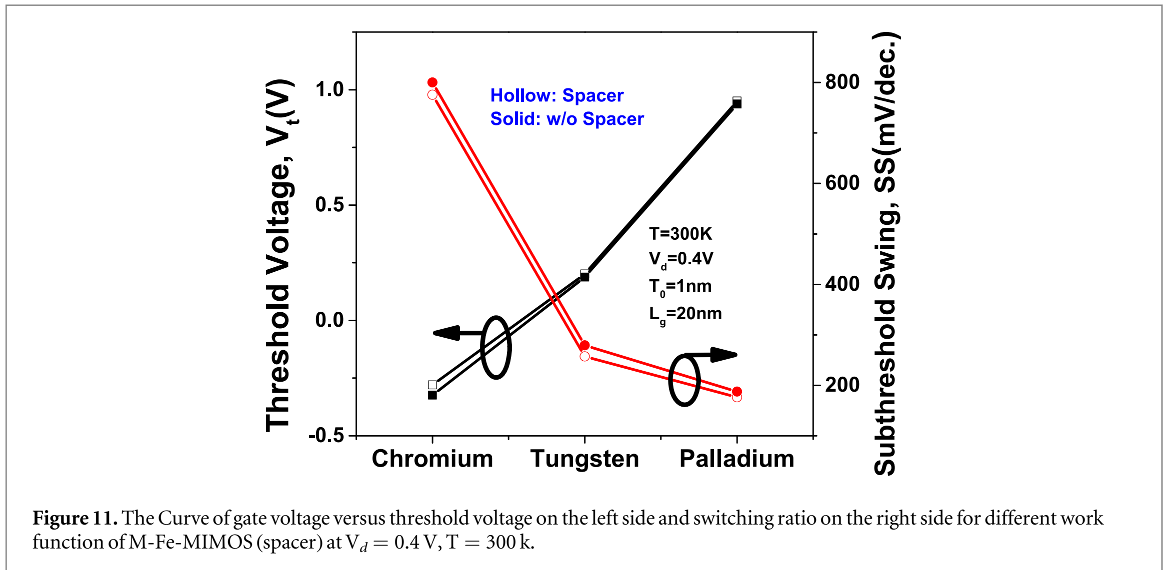

Figure 11. The Curve of gate voltage versus threshold voltage on the left side and switching ratio on the right side for different work function of M-Fe-MIMOS (spacer) at $V_d = 0.4$ V, T = 300 k.

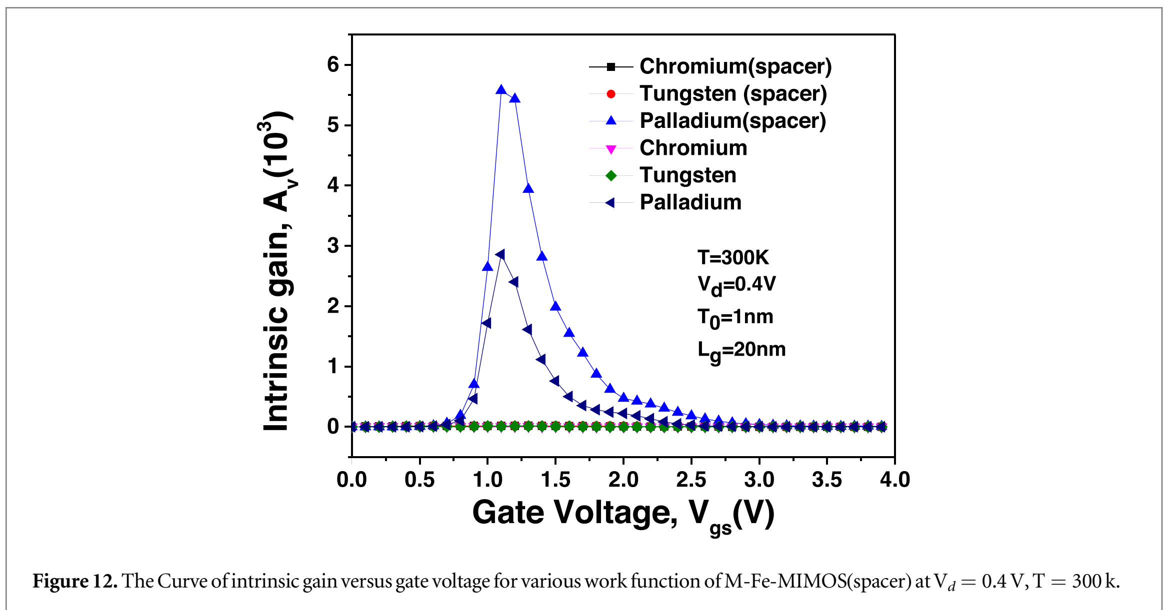

Figure 12. The Curve of intrinsic gain versus gate voltage for various work function of M-Fe-MIMOS(spacer) at $V_d = 0.4$ V, T = 300 k.

Table 3. M-Fe-MIMOS comparison for different work function materials such as palladium, chromium, and tungsten.

Parameter	M-Fe-MIMOS (spacer) Chromium (Cr)	M-Fe-MIMOS (spacer) Tungsten (T)	M-Fe-MIMOS (spacer) Palladium (Pd)	M-Fe-MIMOS Chromium (Cr)	M-Fe-MIMOS Tungsten (T)	M-Fe-MIMOS Palladium (Pd)
I_{off}(nA)	12200	169.0	0.013	14 800	240.0	0.0338
$I_{on}/I_{off}(10^6)$	0.000 394	0.0281	348	0.000 212	0.013	91.8
$V_{th}(V)$	−0.28	0.201	0.9504	−0.324	0.188	0.938
SS ($mV/dec.$)	775.5	257.1	176.4	800.24	279	187.3
TGF (V^{-1})	42.89	49.5	50.6	39.9	46.2	47.3

$$g_m = \frac{\partial I_{ds}}{\partial V_g} \tag{4}$$

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{5}$$

$$V_e = \frac{I_{ds}}{g_d} \tag{6}$$

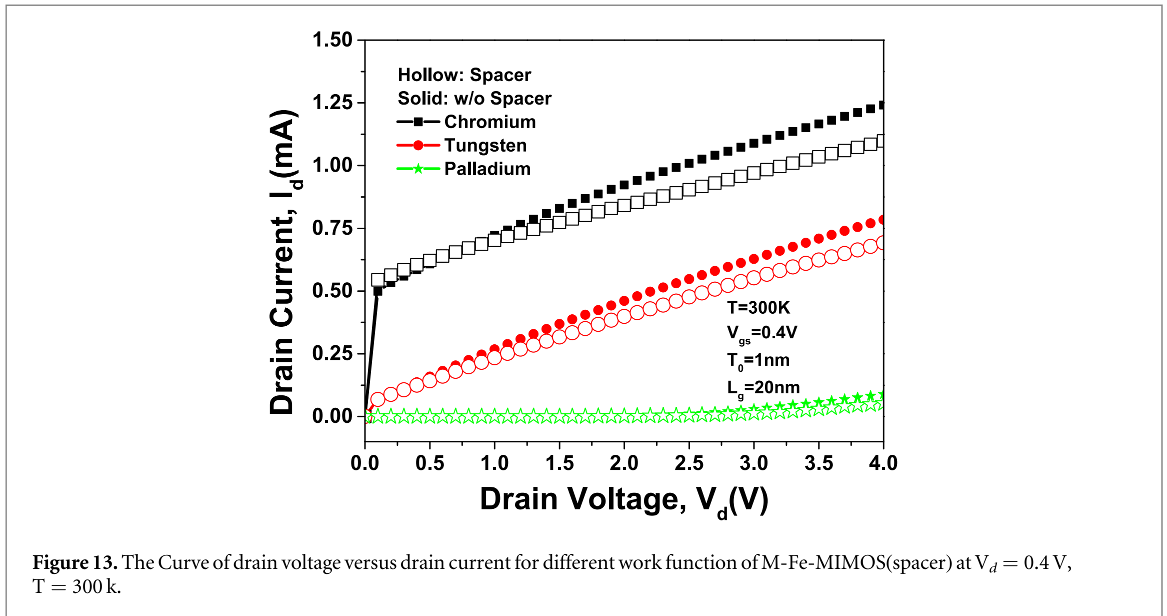

Figure 13. The Curve of drain voltage versus drain current for different work function of M-Fe-MIMOS(spacer) at $V_d = 0.4$ V, T = 300 k.

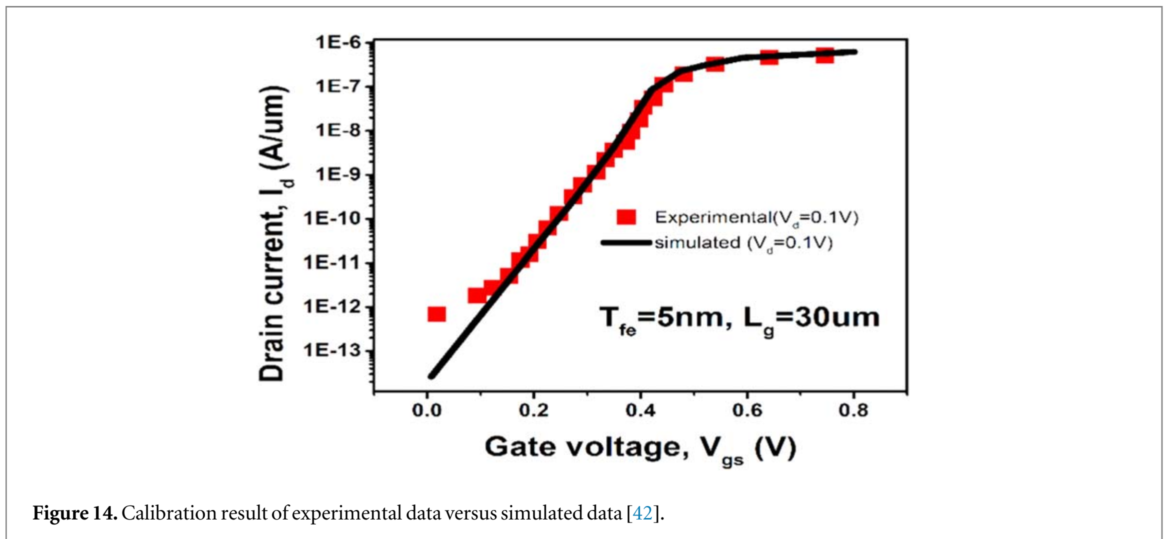

Figure 14. Calibration result of experimental data versus simulated data [42].

$$A_v = \frac{g_m}{g_d} \tag{7}$$

Figure 12 exhibits the gate voltage versus intrinsic gain (A_v) plot at T = 300 K, $V_d = 0.4$ V for different work function. The intrinsic gain (A_v) of M-Fe-MIMOS (spacer) for palladium is better than chromium, tungsten. The A_v of M-Fe-MIMOS (spacer) is higher than M-Fe-MIMOS, which indicates lower output conductance and higher transconductance. It is ratio of transconductance and output conductance [40, 41]. Figure 13 exhibits the drain voltage versus drain current (I_d) of plot at T = 300 K, V_{gs}=0.4 V for different work function. The drain current (I_d) of M-Fe-MIMOS (spacer) for palladium is better than chromium, tungsten. The drain current (I_d) of M-Fe-MIMOS (spacer) is less than M-Fe-MIMOS, which shows the lower output conductance (g_d), lower DIBL as well as channel length modulation (CLM), thus, upgraded the control on gate.

The experiment data is taken from [42]. Figure 14 shows the drain current and gate voltage curves at a drain voltage of 0.1V, a ferroelectric thickness of 5nm and a channel length of 30um for a negative capacitance field effect transistor (NCFET). To verify the physical model, experimental data extraction was taken from [42]. The approximate match between the simulated and experimental data validates the simulation model.

5. Conclusion

This work addresses the comparative study of M-Fe-MIMOS (spacer) and M-Fe-MIMOS for different gate electrodes, and reveals that the palladium with work function 5.3 eV reflects improved result than others like chromium, tungsten. The palladium reveals 10^{-6} times lower the leakage current as compare to chromium, higher switching ratio, decayed the subthreshold swing. Also, some analog parameters found in M-Fe-MIMOS like transconductance, TGF, g_d. Theoretically, we concluded that palladium proved to be a potential material for fabrication of M-Fe-MIMOS with palladium as gate electrode. The increasing work function (ϕ) indicates improved performance of the device. The electric field across channel has also been studied for various work function thus, electric field of palladium is enhanced than other gate electrodes. The M-Fe-MIMOS (spacer) design has already seen significant advances in terms of accuracy, and component count reduction leading to downsizing, lower cost, and greater efficiency. Consequently, the findings of this research can assist engineers in designing such nanoelectronic devices that meet their requirements.

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Data availability statement

The data cannot be made publicly available upon publication because the data can be misused by the third party. The data that support the findings of this study are available upon reasonable request from the authors. The data cannot be made publicly available upon publication because no suitable repository exists for hosting data in this field of study. The data that support the findings of this study are available upon reasonable request from the authors.

Declarations

Funding statement

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Conflict of interests

The authors declare that they are not aware of any disagreements regarding personal ties or interests that might have impacted the work represented in this publication.

Availability of data and material

The creators mentioned above possess the necessary information related to this examination work, and they are committed to revealing it in the event that they are asked to do so in the future.

Authors' contribution

The comprehension and design of the study were improved by all writers.

Compliance with ethical standard

The authors have located all of the moral standards and intend to adhere to them going forward.

Consent to participate and for publication

Since that the relevant study paper was produced in the 'no-life science magazine.' Therefore, at this time, it is 'Non Applicable.' However, the authors have provided the agencies with all journal policies and their permission for additional processing.

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