M.Tech (Power Electronics and Systems)

INTEGERATED CONTROL STRATEGIES FOR CUK CONVERTER

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OF

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Submitted by:

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DECLARATION

I, Praanshu Srijan Shandilya, Roll No. 2K22/PES/10 student of M.Tech (Power Electronics and Systems), hereby declare that the project Dissertation titled **"Integrated Control Strategies for Cuk Converter"** which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original work and not previously used for the award of any Degree.

Place: Delhi **PRAANSHU SRIJAN SHANDILYA**
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CERTIFICATE

This is to certify that the dissertation entitled ***"Integrated Control Strategies for Cuk Converter"*** being submitted by PRAANSHU SRIJAN SHAND IL YA (2K22/PES/10) in partial fulfillment of the requirements for the award of Master of Technology degree in "ELECTRICAL ENGINEERING" with specialization of "POWER ELECTRONICS & SYSTEMS" at the Delhi Technological University is an authentic work carried out by him under my supervision and guidance. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/ Institute for the award of any degree or diploma.

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ABSTRACT

This thesis explores the design, analysis, modeling, and control of DC-DC converters, which are essential components in contemporary electronic systems valued for their efficiency, compactness, and reliability. With their wide range of uses in various industries like computer power supplies, aerospace, medical, and telecommunications, it is crucial for these converters to deliver a stable DC output voltage even in the face of fluctuating input voltage and varying load currents.

Within the parameters of this study, particular focus is made to the Cuk converter in both ideal and non-ideal forms. Starting with important design issues, the paper improves the duty cycle, inductor, and capacitor calculations by including actual non-ideal factors. Especially in the performance of capacitors, a thorough study of output voltage ripple emphasizes even more the importance of the equivalent series resistances (ESRs). The thesis discusses the development of a comprehensive mathematical model that encompasses all aspects of the converter, including both ideal and non-ideal elements. Through the utilization of advanced techniques like state-space averaging and averaged switch modeling, a highly accurate model is created that closely resembles the dynamic and steady-state characteristics of real converters.

Comparative study of the ideal model and the one with non-ideal components confirms the better accuracy of the latter, more precisely reflecting what practitioners could expect from real-world operations of DC-DC converters.

This work investigates improving the performance of both ideal and non-ideal Cuk converters by means of several control techniques including sliding mode controllers, PI-lead controllers, and PI controllers in the final part. Furthermore, it evaluates the sliding mode controller's performance against the conventional two-loop PI controller configuration, therefore providing insightful analysis on how to maximize converter efficiency using sophisticated control techniques.

All things considered, this study holistically covers the essential characteristics of DC-DC converters and provides important new perspectives on their optimization achieved with creative control strategies. The result opens the path for improved performance in electronic systems where such converters are essentially supporting.

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CHAPTER 1
INTRODUCTION

1.1. Overview

In modern times, the availability of electrical power has become an essential requirement for both household appliances and industrial operations. There are diverse uses that necessitate electric power in distinct forms such as AC (Alternative current) or DC (direct current), constant or variable voltage, set or variable frequency, and so on. Typically, electrical power is provided to consumers in the form of AC with a consistent voltage magnitude and frequency (either 50 or 60 Hz). To be able to cater to the needs of diverse consumers, a wide range of power electronic converters have been developed. They have the ability to transform electrical power from one form to another as needed. It is crucial to acknowledge the extensive uses of power electronic converters across diverse industries, in addition to comprehending their complex workings. These converters play a crucial role in many advanced technologies, allowing for the efficient and dependable transformation of electrical power to fulfil a wide range of requirements. Power electronic converters are essential components in renewable energy systems as they transform energy from sources such as solar panels and wind turbines into electricity that can be used by households and businesses.

Similarly, converters in electric vehicles enable the transformation of battery electricity into the necessary energy to drive motors, ensuring a seamless and effective functioning. Furthermore, in portable electronic devices such as smartphones and laptops, DC-DC converters are used to control voltage levels to supply power to delicate electronic parts, hence enhancing battery life and overall performance. Researchers can improve the efficiency and reliability of existing systems and enable new applications in upcoming technologies by comprehending the principles and control mechanisms of power electronic converters.[1]-[5] There are four main categories of power electronic converters that play a crucial role in transforming electrical power to meet various demands: [6]-[9]:

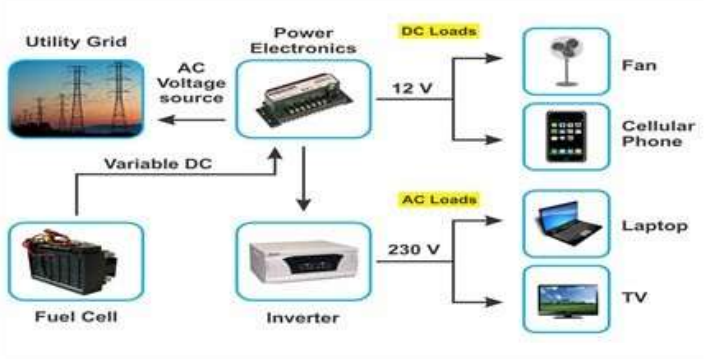


Fig 1.1Application of Power Electronics Converter Systems

1. **AC-DC Converters:** These converters transform AC voltage into either fixed or variable DC voltage in a precise and efficient manner. For example, diode rectifiers are highly efficient at converting AC into fixed DC. On the other hand, phase-controlled rectifiers are more advanced and allow for the regulation of variable DC voltage by modulating the conduction angle.
2. **DC-AC Converters (Inverters)**: Responsible for converting DC input into AC output, inverters ensure the provision of the desired voltage and frequency by precisely adjusting the switch-on time of the components. This allows them to efficiently operate a wide range of loads, including motors and appliances.
3. **AC-AC converter:** A class of converters known as an AC-AC converter skilfully modifies fixed AC voltage to produce variable AC voltage, frequently with the option to change the frequency. While cyclo-converters have the special capacity to modify both voltage and frequency, making them appropriate for applications, AC voltage regulators, for example, maintain voltage levels without changing frequency.
4. **DC-DC Converters:** With specialization in modifying fixed DC voltage to variable DC voltage, these converters employ precise control over switch-on time to achieve the desired output. There are various types of converters available that are designed to efficiently adjust voltage levels for a wide range of applications. These converters are commonly used in portable electronics and renewable energy systems.

1.2. Introduction to DC - DC Converters

The search for effective and flexible power conversion in the always changing field of electronics has never ended. DC-DC converters are now a mainstay of technology that have revolutionized the way power is controlled and used in a wide range of applications. Innovations sparked by these converters have allowed devices to be made smaller while maintaining great efficiency and flexibility that linear regulators could not match on their own[6]-[8]. Before DC-DC converters became widely used, linear regulators were commonly used for voltage regulation tasks. Although linear regulators are known for their simplicity in design and ability to deliver clean, stable output with minimal noise, their operational inefficiency in certain situations prompted the exploration of alternative solutions. Because linear regulators dissipate extra power as heat to regulate voltage, they have a poor energy conversion efficiency by design, particularly in applications where the input and output voltages range significantly. This constraint led to the creation and acceptance of DC-DC converters[9]-[15].

Unlike linear regulators, DC-DC converters employ a distinct method for power conversion. They utilize switch-mode technology, where power switches efficiently convert input voltage to a desired output voltage through high-frequency switching. The energy is stored temporarily in inductors or capacitors and then released at the desired output voltage, greatly reducing energy waste. Making the switch to DC-DC converters instead of traditional linear regulators offers clear advantages, mainly because of their higher efficiency. These converters are well-known for their impressive efficiency rates, often exceeding 90%. This efficiency proves crucial, especially when modern power supplies systems are taken into consideration. Since DC-DC converters are flexible and efficient, they have established essential positions in many different industries. In portable electronics, they effectively control battery life in anything from computers to cell phones. They improve device uptime by guaranteeing constant voltages across various circuit components, which is essential in our world going more and mobile.

For maximum efficiency, the renewable energy industry—which is typified by fuel cells and solar panels—uses DC-DC converters. They skilfully change output voltage to suit the requirements of the grid or storage system, so promoting more seamless energy integration [20]-[23]. The topologies of DC-DC converters are classified in the literature according to several criteria. Still, two basic groups can be distinguished among the important DC-DC converters which is shown in Fig.1.2.:

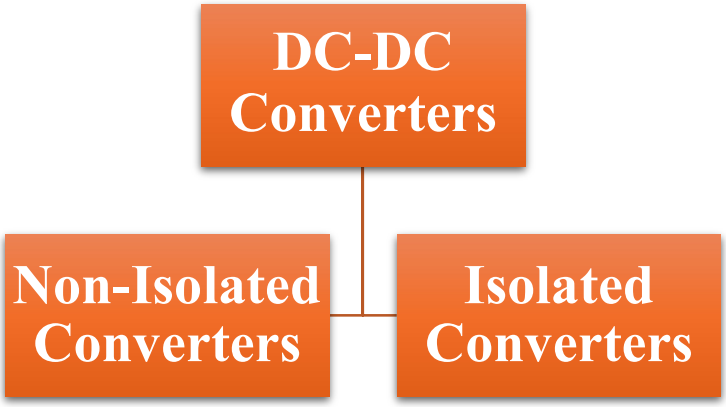


Fig 1.2 Classification of DC-DC Converters

1. **Non-Isolated Converters:** These converters enable seamless energy transfer without any isolative barrier, resulting in cost-effective construction and compact design while ensuring dependable performance in different environments. Among the many topologies covered are the Buck, Boost, Buck-boost, Cuk, Zeta, and SEPIC converters.
2. **Isolated Converters:** Isolated converters use high-frequency transformers to overcome situations that need electrical isolation between the input and output. They play a crucial role in reducing noise and protecting delicate components. Some examples of these types are the forward converter, flyback converter, push-pull converter, half-bridge converter, and full-bridge converter, among other types, are commonly used in power electronics.

   In addition, DC-DC converters can be classified according to their output characteristics, such as having single or multiple outputs. They can also be categorized based on the nature of inductor current flow, which can be either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode

(DCM). Furthermore, the output voltage magnitude is another factor that determines the classification, typically seen in buck, boost, and buck-boost configurations. CCM maintains a stable inductor current above zero throughout the switching cycle, ensuring reliable operation. On the other hand, DCM experiences a drop in the inductor current to zero during a portion of this cycle, which can lead to size reduction benefits for the inductor. To meet a wide range of power management needs, converters like the buck, which steps down input voltage, the boost, which raises it, and the buck-boost, which can do both, use different operational strategies. Adaptive and efficient power supply designs, which serve a wide variety of electronic devices and systems, rely on these converters. Additionally, there are fourth-order converters such as cuk, sepic, and zeta that are based on buck boost topology.

1.3. Motivation for the research

Modern electronics infrastructure would not be complete without DC-DC converters, which have recently come under increased scrutiny in the race for more efficient and effective electronic gadgets. The exact regulation of direct current (DC) power supplied to different circuits from a single source relies heavily on such converters. The many DC-DC converter topologies, which are designed to meet the needs of individual applications by carefully selecting and rating their components, have been previously covered. Several variables impact this complex selection process. These include, but are not limited to, input and output voltages, input current ripple, output voltage ripple, output power, and switching frequency. In particular, the design details cover passive components like inductors and capacitors and active components like semiconductor devices, which are crucial to the efficiency of the converter. To achieve performance goals including improving the converter's efficiency and dependability and reducing voltage and current ripples, their ratings are crucial. Inductors play a crucial role in converter design [24]. Their value has a direct impact on ripple current, where higher inductance results in decreased ripple but at the trade-off of larger size and

potentially higher cost. The shift towards higher switching frequencies indicates a way to reduce the size of the inductor, although it does pose difficulties in terms of managing heat and electromagnetic interference (EMI). In high-frequency applications, the efficiency of inductors can be affected by their inherent resistance. To minimize these losses, it is important to use high-quality inductors with low resistance, often achieved through the use of ferrite cores. However, a careful analysis of scholarly discussions uncovers a lack of consideration for non-idealities in the design equations of inductors and capacitors. This research is driven by the observation that there are gaps in the current understanding of DC-DC converter design processes and aims to fill them by incorporating the effects of non-idealities. Improved converter designs are expected as a result of thorough analysis and consideration of less-than-ideal factors, such as capacitor equivalent series resistance (ESR), inductor core losses, and semiconductor switching and conduction losses. The ultimate goal of this study is to help designers create smaller, more dependable, and more efficient converters by creating a complete model that takes these imperfections into account. Another important part of this study is the modelling of DC-DC converters, which requires a delicate balancing act between being accurate and making models as simple as possible. By filling a critical void in current modelling approaches, this study intends to tackle the problem of modelling converter non-idealities in a way that produces more accurate and useful models[25]-[30].

With the aim of keeping output steady under a range of changing conditions, such as input voltage fluctuations and load variability, the development of improved and adaptive control techniques for DC-DC converters is recognized as an important research avenue. The purpose of this study is to investigate the feasibility of using pulse width modulation (PWM) and other advanced control techniques to reliably stabilize the output voltage.

Because Cuk converters and other higher-order systems are inherently complex, this study is also keen to investigate how non ideal study techniques can simplify control strategy design. While maintaining the control system's

efficacy, this strategy seeks to reduce the computing cost. By combining theoretical analysis with practical innovation, this project seeks to address the stated issues and make a meaningful contribution to the field. This work aims to improve DC-DC converter design and control mechanisms by bridging the gap between theoretical models and real-world application demands, setting new standards for efficiency and effectiveness [31]-[39].

In short, any DC-DC converter must be built through a series of crucial stages, starting with the first one of identifying design parameters to accomplish user-defined goals. After that, one has to work on creating an exact mathematical model of the system [40]-[50]. The final step in this approach is to design a skilful control plan that will guarantee output voltage regulation over a range of operating circumstances. As such, the following three essential aspects of DC-DC converters are the focus of this dissertation:

1. Developing and personalizing DC-DC converter settings.
2. Creating thorough mathematical models of these converters.
3. The integration of control strategies for DC-DC voltage regulation

This thesis focuses on these topics for both non-ideal and ideal models of the Cuk converter in recognition of the variety of DC-DC converter topologies. Through this narrowly focused perspective, the study seeks to provide light on a route toward improved converter dependability and efficiency.

1.4. Contribution of the author

Even if DC-DC converter design, modelling, and control have been studied extensively, this thesis attempts to go deeper into these fields. Both the voltage drops in diodes and the resistances in inductors, capacitors, diodes, and MOSFETs were frequently ignored by earlier studies. These errors are included into this paper, which offers a more precise analysis. With the introduction, there are six chapters in all to the thesis. Chapters that follow describe the contributions to this work. With its concise synopsis of the work done, each chapter advances our knowledge of DC-DC converters.

Incorporating the consequences of imperfections, Chapter 2 presents improved duty cycle calculations for both ideal and non-ideal Cuk converters. These revised design formulae for inductor and capacitor values show how input voltage, defects, and load resistances affect the duty cycle. These converters also have a comprehensive capacitor voltage ripple study done. The maximum ESR value to sustain specified output voltage ripple and inductor current ripple at a given frequency is determined by this analysis. The validation of these theoretical conclusions by means of simulation data closes this chapter.

The emphasis in Chapter 3 moves to using state-space averaging and averaged switch modelling approaches to develop a mathematical model for both the ideal and non-ideal DC-DC Cuk converter. This improved model includes diode voltage dips and parasitic resistances. An evaluation of the mathematical models of the ideal and non-ideal converters is given. This comparison shows that assuming the converter functions perfectly misses important insights into the physical behaviour of the converter that are provided by modelling the converter with its non-ideal features.

Drawing on their transfer function models; Chapter 4 investigates several conventional control techniques for the ideal and non-ideal DC-DC Cuk converters. This section of the work describes the stability boundary locus technique and a predefined phase margin-based PID controller architecture for each kind of Cuk converter. A PI controller reduces steady-state voltage errors well, but it is not very good at maximizing transient responsiveness, the chapter notes.

The chapter presents a dual loop control technique to improve DC-DC converter voltage response. An external voltage and an internal current PI controller are integrated in this novel method. A new approach to modify the parameters of both PI controllers is presented with the intention of achieving particular gain crossover frequency and phase margin targets. This algorithm's power is in its simultaneous fulfilment of the crossover frequency and best phase margin requirements.

A real-world fourth order Cuk converter is then subjected to this recently

developed control approach. The performance of this real application is shown to be rather good, almost matching the performance obtained with the PI controller that was first modelled.

For the DC-DC Cuk converter, Chapter 5 explores the sliding mode control method. It describes how to derive several transfer functions that look at the converter's closed-loop behaviour under sliding mode control. Within the chapter is suggested a simple approach for calibrating the controller's parameters. We present simulation results to show how well the developed controller works.

Chapter 6, which summarises the whole thesis and addresses future study directions, closes the thesis.

At the end of the thesis comes supporting material, which includes appendices and a thorough list of references that support the study carried out throughout.

CHAPTER 2
DESIGN OF DC-DC CONVERTERS

2.1 Introduction

Important parts of the electronics industry, DC-DC converters are essential for managing and modifying voltage levels in a wide range of devices. Through the provision of the necessary voltage for electronic circuits, these converters guarantee the effective operation of a wide range of applications, from portable devices like laptops and cell phones to renewable energy systems and automobile electronics. There exist three basic topologies of DC-DC converters, each with unique properties and uses. These are the converters for buck, boost, and buck-boost.

The buck converter reduces the input voltage to a lower output value. It is distinguished by its capacity to deliver a consistent output current with few voltage fluctuations, making it very efficient for applications that necessitate a reliable power supply. However, there is a problem to consider: the input current is not continuous, which means that an input filter must be included in order to guarantee smooth functioning.

Conversely, the boost converter amplifies the input voltage to a greater output voltage. The most notable characteristic of this is its uninterrupted input current flow, which eliminates the requirement for an input filter. Nevertheless, similar to the buck converter, it also has drawbacks. In the boost topology, the output current is not continuous, which means that it is not constant over time. To reduce the amount of fluctuation in the output voltage, a significant amount of capacitance is needed.

The flexible buck-boost converter offers output voltage levels that can be greater, lower, or equal to the input voltage by combining the features of both buck and boost converters. Because it flips the polarity of the output voltage with respect to the input and has discontinuous input and output currents, like a boost converter, its implementation presents special problems.

With clever integration of their benefits, the Cuk converter appears as a smart development of these three fundamental topologies. It can be set to provide continuous

current at the input and output sides and to vary the output voltage to be either equal to, less than, or higher than the input voltage. In comparison to the input voltage, its output voltage is inverted, though.

A fourth-order system, the Cuk converter gains stability and efficiency by adding two inductors and capacitors.

Beyond the Cuk converter, the Zeta and SEPIC converters are also part of the DC-DC converter arena; they both keep the output voltage polarity equal to the input voltage. Though the Zeta converter has discontinuous input current, like the buck topology, the SEPIC converter has discontinuous output current, which is a drawback of the boost architecture. In keeping with their intricacy and degree of control over voltage conversion procedures, both are likewise categorised as fourth-order systems.

When it comes to applications that depend on DC-DC converters, finding the perfect combination of inductance and capacitance is crucial. Achieving the optimal inductance and capacitance configuration is critical for applications depending on DC-DC converters, as several research and scholarly sources [references] demonstrate. Although real-world situations show otherwise, theoretical analysis and design approaches usually presume the components of these converters to be faultless [references]. DC-DC converters' real components are faulty and not at all like the ideal model {List of references}. These imperfections manifest as equivalent series resistances (ESRs) in inductors and capacitors, additional resistances encountered in MOSFETs and diodes during their operational phase, and the diodes' inherent forward voltage drop. Such non-ideal factors can significantly influence the performance and design specifics of DC-DC converters, posing challenges for crafting precise and high-quality power supplies. For instance, when theoretically modelling the duty cycle formulas for a Cuk converter in continuous conduction mode (CCM) as shown in Eqn. (2.1), these real-world discrepancies must be accounted for to ensure accuracy and efficiency in design.

$$\frac{V_o}{V_s} = D_{ideal} \tag{2.1}$$

Where V_o is the output voltage and V_s is the input voltage of the Cuk converter.

The conventional assumptions for the Cuk converter's operation are based on the ideal performance of every component in the system. Nevertheless, practical implementations of the Cuk converter may not achieve the desired output voltage V_O when compared to the idealised expressions, due to encountered losses. This phenomenon occurs when there are voltage reductions or energy dissipation across components that deviate from the ideal model.

One must use a duty cycle that is higher than the one anticipated by the ideal formulations Eqn. (2.1) in order to counteract these energy losses. Accurate design and parameter adjustment of the converter also become essential to achieve the performance targets. This demands that the converter's circuitry and operation be thoroughly examined. Here we go into great detail on the non-ideal behaviour of the Cuk converter, which results in the development of improved design equations for the relevant inductors and capacitors. This chapter also provides a thorough analysis and performance review of the Cuk converter, comparing the theoretical ideal models with their real-world, less ideal equivalents.

2.2 Analysis of Ideal Cuk DC- DC Converter

The schematic diagram of a Cuk DC-DC converter as shown in Fig.2.1 reveals a unique arrangement designed to regulate voltage levels efficiently. It consists of two inductors, two capacitors, a semiconductor diode, and a switch, usually a transistor. Using this configuration, energy is transferred effectively between its input and output sides while the polarity of the output voltage is reversed w.r.t the input voltage. Inductors and capacitors, two energy storage components, play a crucial role in smoothing out voltage and current transitions, making sure a stable output happens. What sets the Cuk converter apart is its versatility, demonstrated by its capability to work in two modes: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). For the purpose of this study, the focus is narrowed to its operation in CCM. This mode is critical for understanding how the converter performs under steady conditions, with particular emphasis on the duty cycle (D) and the switching frequency (f_s). The duty cycle, which is the ratio of the switch's active time to the total cycle time, plays a pivotal role in controlling the converter's output, making it a key factor in our analysis.

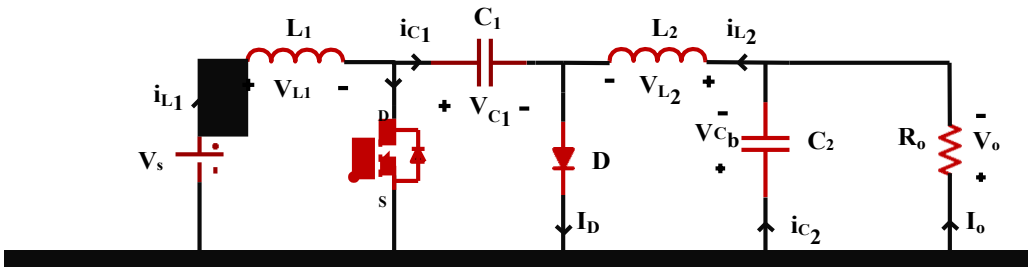


Fig 2.1 Schematic Diagram of Cuk Converter

Mathematically,

$$D = \frac{t_{on}}{t_{on} + t_{ooooo}} = \frac{t_{on}}{T_S} = t_{on}f_s \tag{2.2}$$

Where t_{on} is the interval of time when the MOSFET is turned ON, and t_{ooooo} is the time interval when the MOSFET is turned OFF.

From Eqn. (2.2), we get,

$$t_{on} = DT_S \text{ (When the MOSFET is turned ON)} \tag{2.3}$$

$$t_{ooooo} = (1 - D)T_S = D'T_S \text{ (When the MOSFET si turned OFF)} \tag{2.4}$$

Where $D' = (1 - D)$

Cuk converter is controlled by MOSFET switching mechanisms. In CCM mode it has two switching mode (a) When the MOSFET is ON and the Diode is turned OFF, or (b) When the MOSFET is turned OFF and the Diode Conducts.

2.2.1 Mode 1 of operation ($00 < t < DT_S$)

In a Cuk DC-DC converter, Mode 1 refers to the phase where the MOSFET, is turned on and the diode, D is non-conducting. As the MOSFET is turned on in Mode 1, the current flows through an inductor, L_1, the MOSFET, and then to the ground. Because of the applied voltage V_s, across inductor L_1, the current through it increases linearly with time. Due to the input voltage source's energy, inductor L_1 stores more energy. During this time, the capacitor C_1 starts to discharge through the closed MOSFET since it's storing energy from the previous cycle. Thus, the voltage across C_1 drops. In this mode, the current flowing through capacitor C_1 contributes to the current flowing through inductor L_2, which also provides power to the load, so energy is transferred.

Using Kirchoff's Voltage and current law, the voltage across the inductor L_1 and L_2, current across the capacitor C_1 and C_2, and the output voltage is given by:

$$V_{L_{1,on}} = L_1 \frac{d\ddot{\imath}_{L_1}}{dt} = V_s \tag{2.5}$$

$$V_{L_{2,on}} = L_2 \frac{d\ddot{\imath}_{L_2}}{dt} = V_{C_1} - V_{C_2} \tag{2.6}$$

$$\ddot{\imath}_{C_{1,on}} = C_1 \frac{dV_{C_1}}{dt} = -\ddot{\imath}_{L_2} \tag{2.7}$$

$$\ddot{\imath}_{C_{2,on}} = C_2 \frac{dV_{C_2}}{dt} = \ddot{\imath}_{L_2} - \frac{V_{C_2}}{R_o} \tag{2.8}$$

$$V_o = V_{C_2} \tag{2.9}$$

2.2.2 Mode 2 of operation ($DT_s < t < (\mathbf{1} - D)T_s$)

In the Cuk converter's second stage, when the MOSFET turns off, the dynamics of the system change. The inductor L_1, which had been building up current, now pushes that current through a diode that starts to conduct because of the MOSFET's inactivity. This current goes on to charge capacitor C_1. and the energy stored in L_2 is transferred to the output capacitor C_2 and the load. Both modes of operation are shown in Fig.2. Using Kirchoff's Voltage and current law, the voltage across the inductor L_1 and L_2, current across the capacitor C_1 and C_2, and the output voltage is given by:

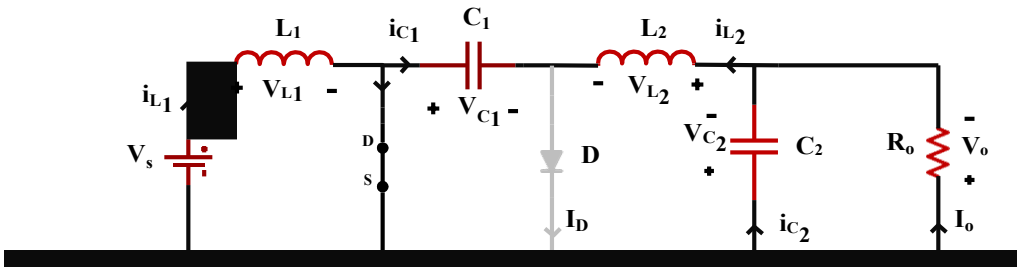
$$V_{L_{1,ooooo}} = L_1 \frac{d\ddot{\imath}_{L_1}}{dt} = V_s - V_{C_1} \tag{2.10}$$

$$V_{L_{2,ooooo}} = L_2 \frac{d\ddot{\imath}_{L_2}}{dt} = -V_{C_2} \tag{2.11}$$

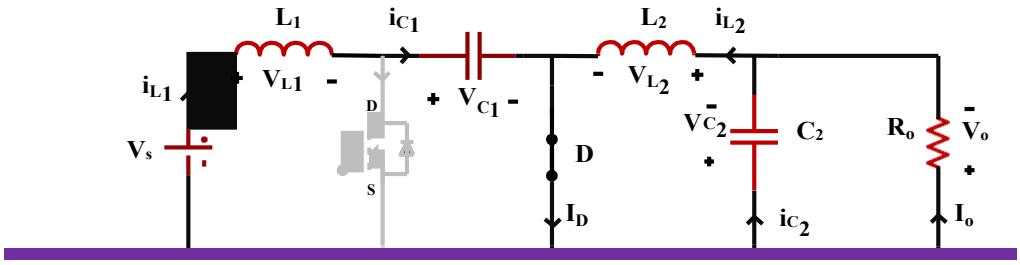
$$\ddot{\imath}_{C_{1,o0000}} = C_1 \frac{dV_{C_1}}{dt} = -\ddot{\imath}_{L_1} \tag{2.12}$$

$$\ddot{\imath}_{C_{2,O0000}} = C_2 \frac{dV_{C_2}}{dt} = \ddot{\imath}_{L_2} - \frac{V_{C_2}}{R_o} \tag{2.13}$$

$$V_{OO} = V_{C_2} \tag{2.14}$$



(a)



(b)

Fig 2.2 Mode of operation (a) Mode 1 (b) Mode 2

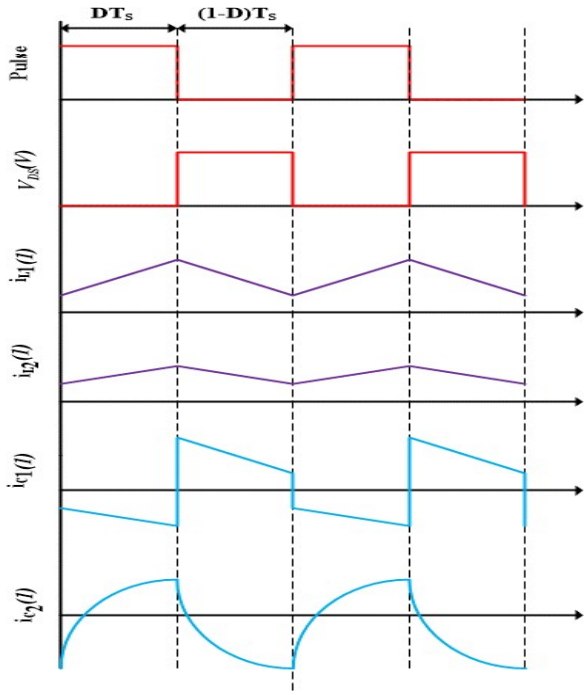


Fig 2.3 Switching Waveforms of Cuk DC-DC Converter

2.2.3 Steady state analysis

In the context of steady-state analysis, the mean value of a current and voltage variable, denoted as X can be described as follows:

$$XX = \frac{1}{T}\int_0^T x(t)dt = \frac{1}{T}\int_0^{DT} x_{on}(t)dt + \frac{1}{T}\int_{DT}^T x_{ooooo}(t)dt \tag{2.15}$$

Where x_{on} and x_{off} denotes the variable x(t) when switch is on and off respectively.

According to the principle of volt-second balance for an inductor, over a full cycle of a switched-mode power supply, the cumulative voltage applied to an inductor equals zero i.e,

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^{DT} v_{L,on}(t)dt + \frac{1}{T}\int_{DT}^T v_{L,ooooo}(t)dt = 0 \tag{2.16}$$

Similarly, as per the Ampere-Second balance for a capacitor, over a complete switching cycle, the net charge transferred to and from a capacitor equals zero, signifying a state of dynamic equilibrium. This is given by:

$$I_C = \frac{1}{T}\int_0^T i_C(t)dt = \frac{1}{T}\int_0^{DT} i_{C,on}(t)dt + \frac{1}{T}\int_{DT}^T i_{C,ooooo}(t)dt \tag{2.17}$$

Also, the average output voltage of the ideal Cuk converter is given by:

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = \frac{1}{T}\int_0^{DT} v_{o,on}(t)dt + \frac{1}{T}\int_{DT}^T v_{o,ooooo}(t)dt \tag{2.18}$$

2.2.3.1 Expression for output voltage

The expression of the output voltage of the ideal Cuk Converter can be derived from applying volt sec balance to the inductor L_1. Substituting Eqn. (2.5) and Eqn. (2.10) into Eqn. (2.16) we get:

$$\frac{1}{T}\int_0^{DT} V_S dt + \frac{1}{T}\int_{DT}^T (V_S - V_{C_1})dt = 0 \tag{2.19}$$

On simplifying the Eqn. (2.19) we get,

$$V_S D + (1-D)(V_S - V_{C_1}) = 0 \tag{2.20}$$

$$V_S - (1-D)V_{C_1} = 0 \tag{2.21}$$

The average Voltage of capacitor C_1 can be calculated by applying KVL from voltage source to the output voltage, i.e.,

$$V_{C_1} = V_s + V_o - V_{L_1} + V_{L_2} \quad (2.22)$$

Since the average voltage of inductors is zero as per volt sec balance, therefore,

$$V_{C1,avaa} = V_s + V_o \quad (2.23)$$

Substituting the value from Eqn. (2.23) to Eqn. (2.21), we get

$$V_o = \frac{DV_s}{1-D} \quad (2.24)$$

As shown by this equation, the converter is capable of producing an inverted output voltage relative to its input voltage. When the duty cycle is less than 0.5, the converter generates a reduced magnitude of inverted output voltage. Conversely, when the duty cycle is greater than 0.5, the inverted output voltage increases in magnitude, enabling the converter to respond to situations involving higher voltage levels from lower voltage sources in particular.

Table 2.1 Ideal Cuk Converter Specifications

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1	0.384µH
Inductance L_2	0.768µH
Decoupling Capacitor,C_1	38.58µF
Filter Capacitor, C_2	2µF
Switching Frequency, f_{sss}	50kHz
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\%I_{L_1}$/ $10\%I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\%V_{c_1}/1\%\ V_{c_2}$

For constant input voltage V_s, the variation of output voltage with respect to duty cycle is shown in figure. At a load resistance R_o = 12, the input voltage is kept constant at 24V, and the duty cycle varies from D = 0.1 to D = 0.85. As shown in Figure, for duty cycles less than 0.5, output voltages are less than input voltages. However, for duty cycles greater than 0.5, output voltages rise sharply and exceed input voltages.

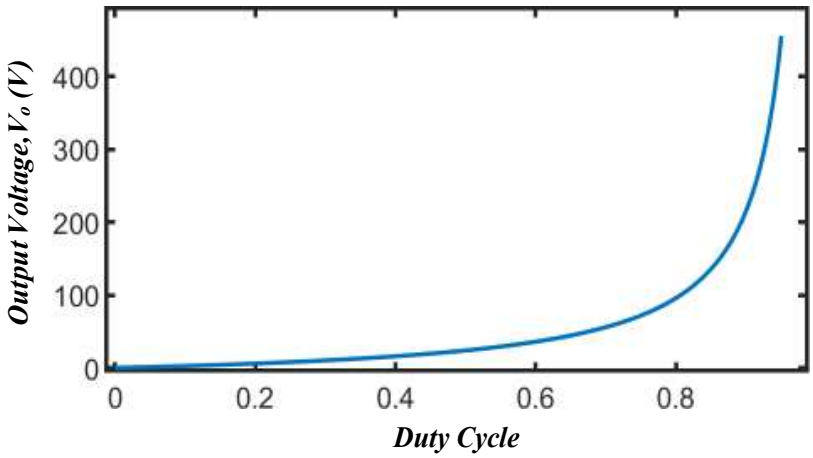


Fig 2.4 Output Voltage Variation with Duty Cycle

2.2.4 Inductor current ripple and Inductor design

The design of inductors plays a key role in the effectiveness of DC-DC converters. It influences their efficiency, size, and the control over voltage fluctuations. Inductors are central to how energy is stored and transferred, shaping the converter's overall performance. Thus, focusing on innovating inductor design is essential for achieving more efficient, smaller, and robust DC-DC converters.

Let Δi_{L_1} *and* Δi_{L_2} be the desired ripple in inductor current (ICR) and x_{L_1} *and* x_{L_2} be the desired inductor current ripple factor (ICRF) for both the inductors. The relationship between the ICR and ICRF is given by:

$$x_{L_1} = \frac{\Delta i_{L_1}}{I_{L_1}}$$

Similarly, (2.25)

$$x_{L_2} = \frac{\Delta i_{L_2}}{I_{L_2}}$$

Where, I_{L_1} *and* I_{L_2} are the average currents flowing through inductor L_1 and L_2.

Now, under steady state, using Eqn. (2.5), it can be written as,

$$L_1 \frac{di_{L_1}}{dt} = V_s \quad (2.26)$$

By substituting the switch on duration, dt = DTs, we get,

$$L_1 = \frac{V_S * DT_s}{\Delta\Delta i_{L_1}} \tag{2.27}$$

Since $T_s = 1/f_s$, therefore Eqn. (2.27) can be rewritten as,

$$L_1 = \frac{V_S * D}{\Delta\Delta i_{L_1} * f f_s} \tag{2.28}$$

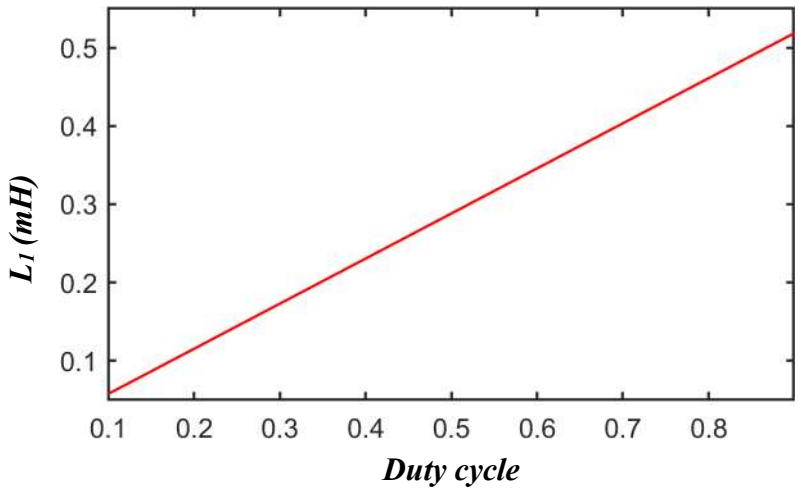
For inductor L_2, using the Eqn. (2.11) i.e. when the switch is off, it can be written as

$$L_2 \frac{d i_{L_2}}{dt} = -V_o \tag{2.29}$$

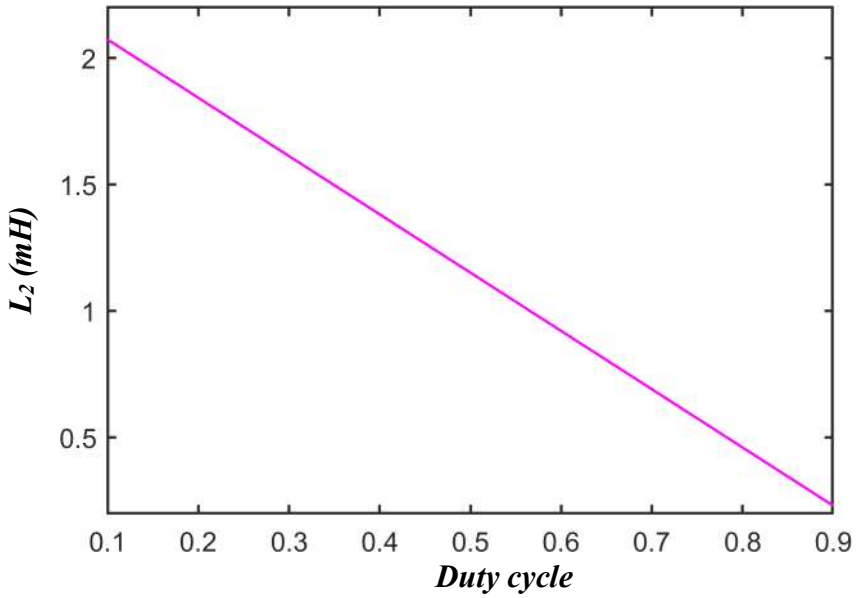
By substituting the switch off duration, $dt = (1-D)T_s$ and $T_s = 1/f_s$, we get

$$L_2 = \frac{V_o * (1 - D)}{\Delta\Delta i_{L_2} * f f_s} \tag{2.30}$$

Fig.2.4 masterfully showcases the contrasting dynamics between two inductors, L_1 and L_2, within the framework of varying duty cycles in a Cuk converter setup. It intriguingly reveals that as we dial up the duty cycle, the inductance of inductor L_1 experiences an upward trajectory, necessitating higher inductance to efficiently manage the system's energy storage and minimize current ripple. As opposed to the narrative when observing inductor L_2 within the same graph, an increase in duty cycle intriguingly leads to a reduction in inductance. Based on this inverse relationship, L_2 demands less inductance as the duty cycle intensifies, suggesting a unique, adaptive behaviour as opposed to L_1. Moreover, this nuanced interplay emphasizes the delicate balance and precise tuning required for the smooth and efficient operation of Cuk converters, taking into account L_1 and L_2's distinct functions and requirements.



(a)



(b)

Fig 2.5 Variation of inductance with Duty Cycle (a) L_1 (b) L_2

2.2.5 Output voltage ripple and capacitor design

The capacitor plays a pivotal role in determining the system's overall efficiency and performance. An optimally designed capacitor ensures the seamless transfer of energy between circuits, minimizing voltage ripples and enhancing power stability. This critical component acts as a buffer, storing and releasing electrical energy, thereby smoothing the output voltage, and reducing electromagnetic interference. The design parameters of the capacitor, including its capacity, voltage rating, and physical size,

must be meticulously tailored to meet the specific requirements of the converter. It allows for the achievement of high-efficiency levels, operational reliability, and longevity of the converter, underscoring the necessity for precise capacitor design in crafting an ideal Cuk DC converter.

In steady state, let ΔV_{C_1} *and* ΔV_{C_2} be the desired voltage ripple across the capacitor C_1 and C_2.

Considering the Eqn. (2.7), and also considering the average value of inductor current i_{L_2} we get,

$$i_{C_1,avg} = I_{00} \tag{2.31}$$

$$C_1 \frac{dV_{C_1}}{dt} = \frac{V_o}{R_o} \tag{2.32}$$

$$C_1 = \frac{V_o * D}{R_o * \Delta V_{C_1} * f_s} \tag{2.33}$$

The output capacitor is like a buck converter, so using the definition of capacitor,

$$\Delta\Delta\Delta = C\Delta\Delta V \tag{2.34}$$

So for the output capacitor the relationship shown in Eqn. (2.34) can be written as,

$$\frac{1}{2}\left(\frac{T_s}{2}\right)\left(\frac{\Delta\Delta i_{L_2}}{2}\right) = C_2 \Delta V_{C_2} \tag{2.35}$$

$$C_2 = \frac{T_S * \Delta\Delta i_{L_2}}{8V_{C_2}} \tag{2.36}$$

Using Eqn. (2.29) and substituting the value of Δi_{L_2} into Eqn. (2.36) we get,

$$C_2 = \frac{V_o * (1 - D)}{8 * f_s^2 * \Delta V_{C_2} * 2} \tag{2.37}$$

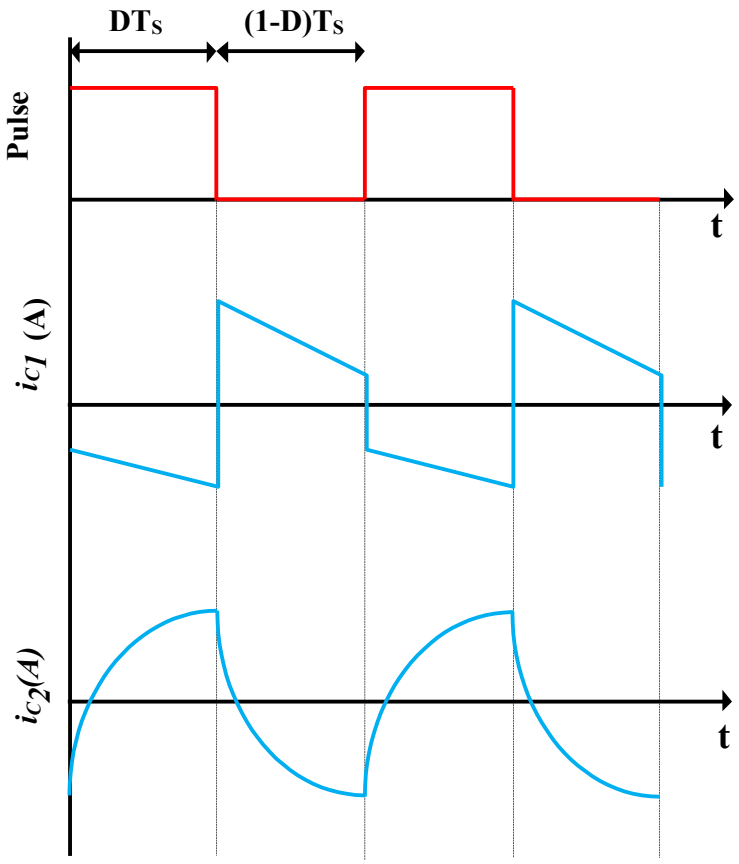


Fig 2.6 Charging and Discharging behaviour of Capacitor $C_1 and C_2$

2.2.6 Results and discussions

The theoretical study of the ideal Cuk converter was simulated using MATLAB Simulink, with parameters specified in Table 2.1. The simulation aimed to analyse the output voltage response under varying conditions. Results indicated that the output voltage closely followed the expected behaviour predicted by theoretical models. Specifically, as the duty cycle increased, the output voltage also rose, exhibiting a linear relationship. Conversely, decreasing the duty cycle led to a reduction in output voltage.

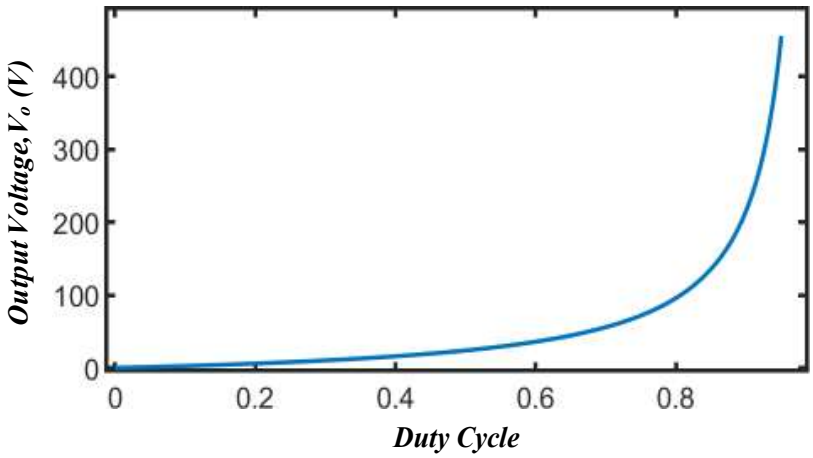


Fig 2.7 Duty Cycle Vs Output Voltage

With a carefully calculated duty cycle of 0.66, based on Eqn.(2.1), and inductance values set at 0.384mH for L_1 and 0.768mH for L_2, the converter was tasked with transforming a 24V input to a 48V output, as dictated by Eqn (2.2). Throughout the simulation, the performance of the Cuk converter was exemplary, achieving a steady and stable 48V output under open loop conditions.

This capability to maintain a precise output voltage, especially notable in an open-loop system, emphasizes the converter's efficiency and the accuracy of its design and component selection.

A fascinating aspect captured in Fig 2.9 is the relationship between the output voltage ripple and the switching frequency. The trend is clear and consistent: as the switching frequency climbs, the ripple within the output voltage shows a marked decline. This inverse relationship is critical for applications demanding a smooth DC output, as it suggests that increasing the switching frequency can enhance the output quality.

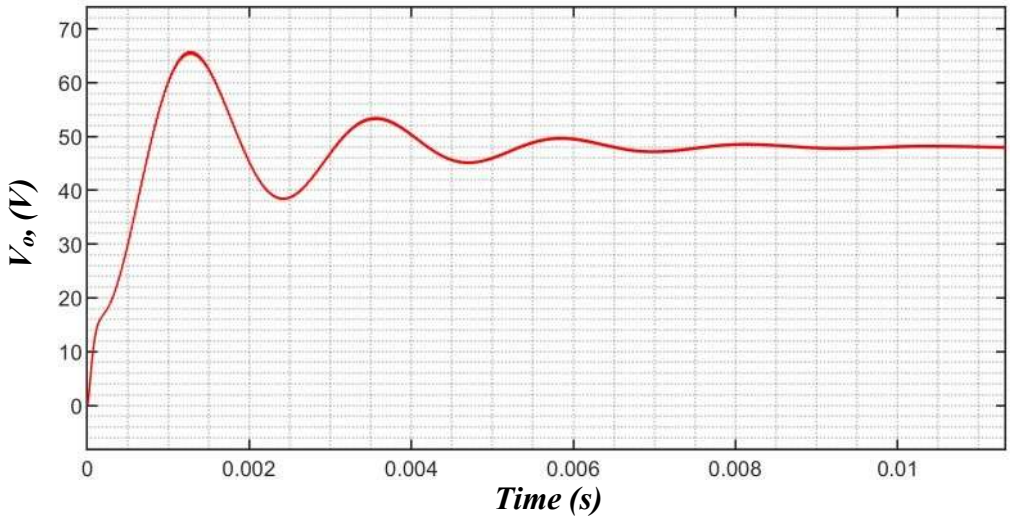
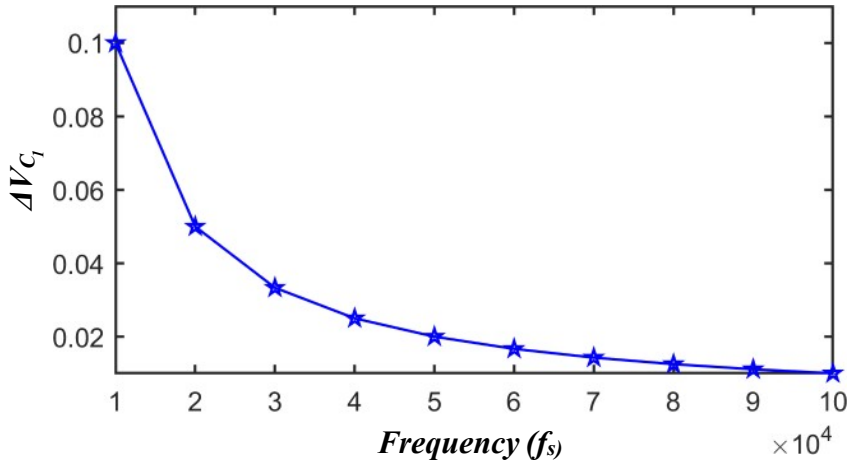
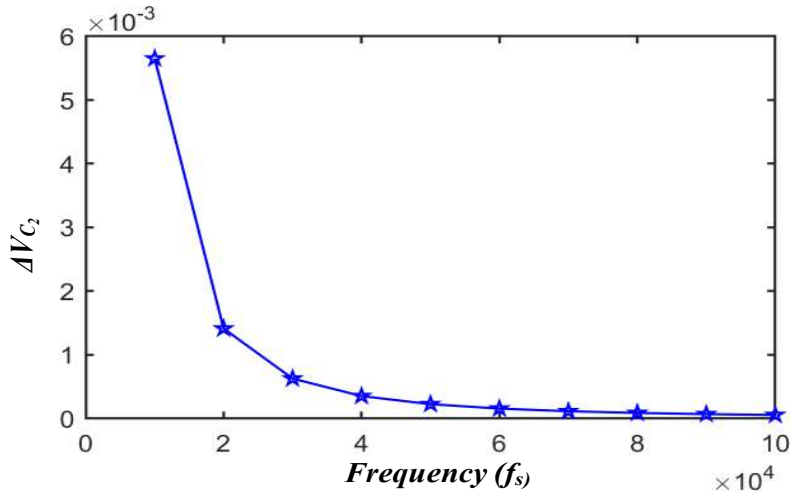


Fig 2.8 Output Voltage response at rated conditions



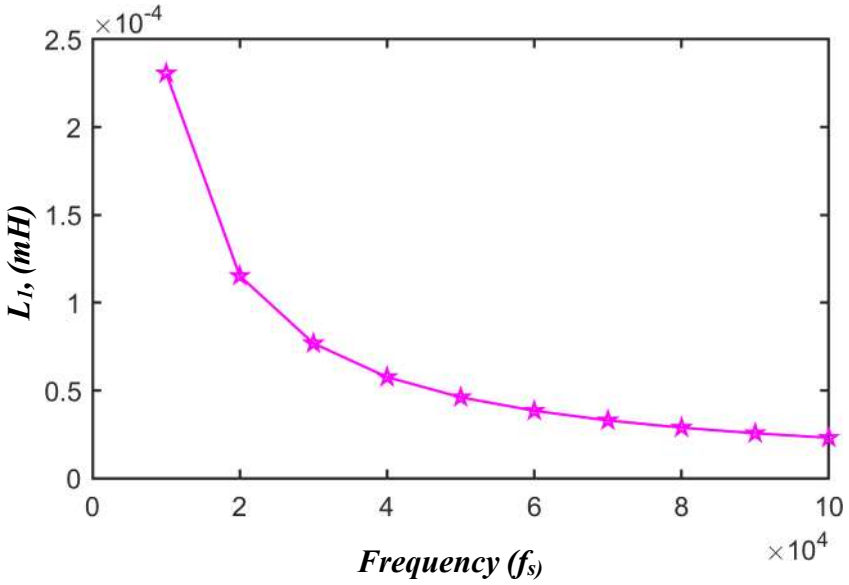
(a)



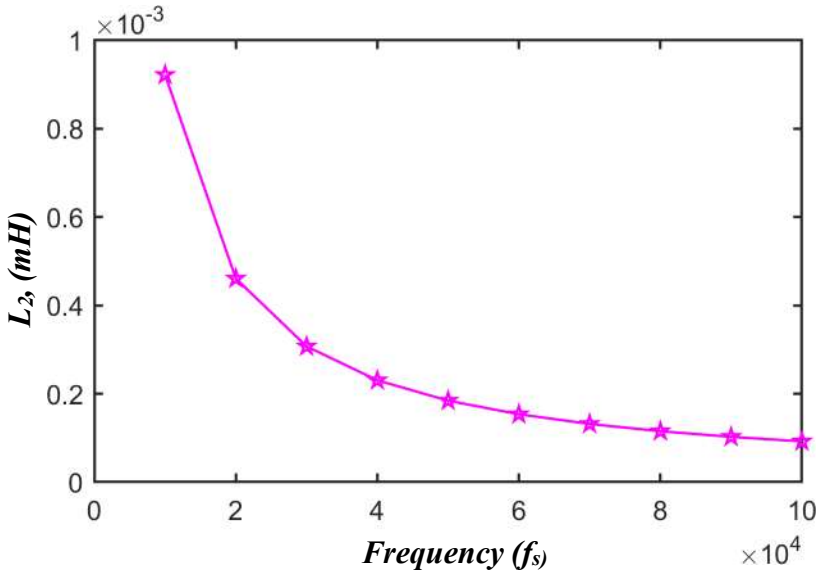
(b)

Fig 2.9 Ripple Voltage variation with switching frequency for (a) C_1 (b) C_2

Simultaneously, Fig 2.10 illustrates another interesting correlation between the inductance values and switching frequency. The captured data demonstrates a decrease in the required inductance value as the switching frequency rises. This finding has practical implications for the design of compact Cuk converters; higher switching frequencies allow the use of smaller inductors, which can lead to size and cost reductions without sacrificing performance.



(a)



(b)

Fig 2.10 Relation of frequency with inductance (a) L_1 (b) L_2

2.3 Analysis of Non ideal Cuk converter

In the schematic of a non-ideal Cuk DC-DC converter, several components critical to its operation must be accounted for beyond the ideal theoretical model. The converter characteristically includes two inductors, $L_1$and L_2, essential for energy storage and smoothing input and output current fluctuations respectively. Between these inductors, a capacitor (C_1) is pivotal in transferring energy via a switching mechanism controlled by a pulse-width modulated (PWM) signal. This switching element, typically a MOSFET, orchestrates the charge and discharge cycles of (C_1) by alternating its state. Complementing this switch, a diode is strategically placed to provide a pathway for current during the non-conductive states of the transistor, maintaining continuity of operation. Additionally, the output capacitor (C_2) plays a vital role in mitigating voltage ripple, thereby stabilizing the output. The schematic is shown in Fig.2.9.

In the realm of non-ideal components, the Equivalent Series Resistance (ESR) of both capacitors and inductors introduces inefficiencies such as heat generation and voltage drop, factors that significantly affect converter performance and efficiency. This intricate configuration of the non-ideal Cuk converter, complexified by real-world component imperfections, provides a robust framework for understanding the challenges in optimizing converter design to balance efficiency, cost, and performance

in practical power supply applications. This detailed examination not only advances the comprehension of the operational principles but also aids in the empirical evaluation and enhancement of DC-DC converter systems. In the comprehensive study of the non-ideal Cuk DC-DC converter, a critical aspect similar to its ideal counterpart is the operation across two distinct modes of conduction: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

The Cuk converter employs MOSFET switching mechanisms for control. In Continuous Conduction Mode (CCM), it operates in two switching modes: (a) when the MOSFET is in the ON state and the diode is turned OFF, or (b) when the MOSFET is turned OFF and the diode conducts.

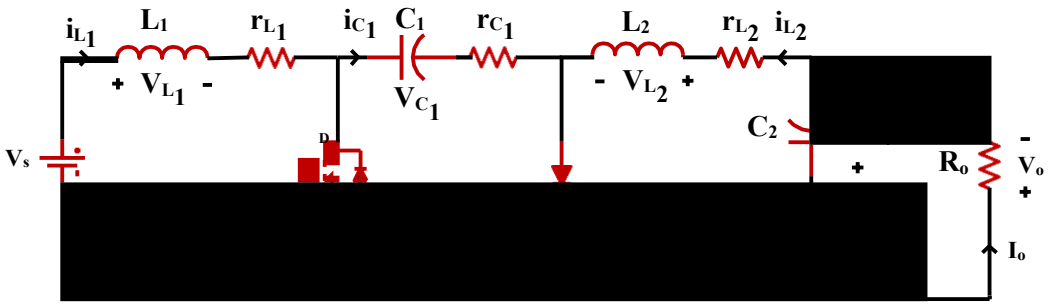


Fig 2.11 Schematic diagram of Non- Ideal Cuk Converter

2.3.1 Mode 1 of operation ($00 < t < DT_S$)

The operational dynamics of the non-ideal Cuk converter, as delineated in Fig.2, can be dissected into two principal stages that are critical to understanding its steady-state behaviour. During the initial stage, the MOSFET, denoted as S, is in a closed state, catalysing a notable increment in the current through the inductor (L_1). This increment is indicative of the inductor (L_1) charging, storing energy derived from the input source. Concurrently, the coupling capacitor (C_1) commences its discharge process, whereby it serves a dual role: it provides the necessary energy to power the load, and at the same time, facilitates the transferal of energy to inductor (L_2). Throughout this phase, the diode remains in an OFF state due to the reverse bias induced by the potential difference across it, sustained by the energy transfer dynamics governed by the closed MOSFET.

Using Kirchoff's voltage and current equation, the system dynamics under steady state can be written as:

$$V_{L_{1,on}} = L_1 \frac{d\ddot{\imath}_{L_1}}{dt} = V_s - \blacklozenge r_{L_1} + R_{ds}\blacklozenge\ddot{\imath}_{L_1} - R_{ds}\ddot{\imath}_{L_2} \tag{2.38}$$

$$V_{L_{2,on}} = L_2 \frac{d\ddot{\imath}_{L_2}}{dt}$$

$$= -R_{ds}\ddot{\imath}_{L_1} - \blacklozenge R_{ds} + r_{C_1} + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}\blacklozenge\ddot{\imath}_{L_2} + V_{C_1} \tag{2.39}$$

$$- \blacklozenge \frac{R_o}{R_o + r_{C_2}} \blacklozenge V_{C_2}$$

$$\ddot{\imath}_{C_{1,on}} = C_1 \frac{dV_{C_1}}{dt} = -\ddot{\imath}_{L_2} \tag{2.40}$$

$$\ddot{\imath}_{C_{2,on}} = C_2 \frac{dV_{C_2}}{dt} = \frac{R_o}{R_o + r_{C_2}} \ddot{\imath}_{L_2} - \frac{V_{C_2}}{R_o + r_{C_2}} \tag{2.41}$$

$$V_o = \frac{R_o r_{C_2}}{R_o + r_{C_2}} \ddot{\imath}_{L_2} + \frac{R_o}{R_o + r_{C_2}} \tag{2.42}$$

2.3.2 Mode 2 of operation ($DT_s < t < (\mathbf{1} - D)T_s$)

In the operational process of the non-ideal Cuk DC converter during stage 2, there's a detailed explanation of its inner workings. As the MOSFET S switches to an open state and the diode takes over conduction, a significant transformation occurs within the converter's setup. Essentially, the energy previously stored in the inductor L_1 is discharged, initiating a transfer of power to the capacitor C_1. This phase is marked by the simultaneous charging of C_1, which acts as a repository for accumulated energy. At the same time, the discharge of the previously charged inductor L_2 begins, facilitating the delivery of power to the load.

The system dynamics under steady state can be written as Using Kirchoff's voltage and current equation:

$$V_{L_{1,o0000}} = L_1 \frac{d\ddot{\imath}_{L_1}}{dt} = V_s - \blacklozenge r_{L_1} + r_{C_1} + R_D\blacklozenge\ddot{\imath}_{L_1} - R_D\ddot{\imath}_{L_2} - V_{C_1} \tag{2.43}$$

$$V_{L2,ooooo} = L_2 \frac{d\ddot{\imath}_{L_2}}{dt}$$

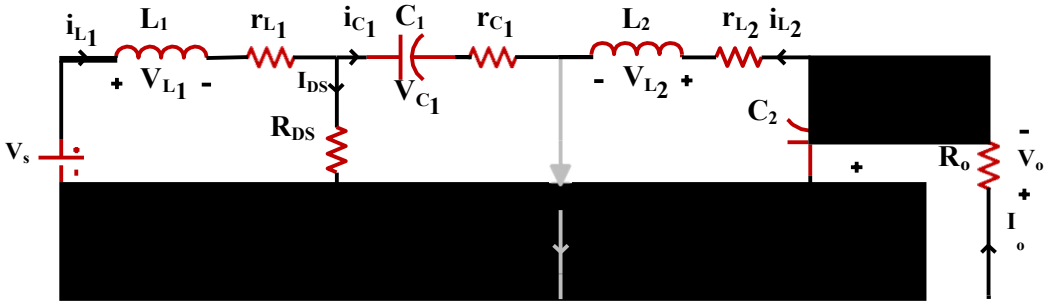
$$= -R_D \ddot{\imath}_{L_1} - \left(R_D + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}\right) \ddot{\imath}_{L_2} \quad (2.44)$$

$$- \left(\frac{R_o}{R_o + r_{C_2}}\right) V_{C_2}$$

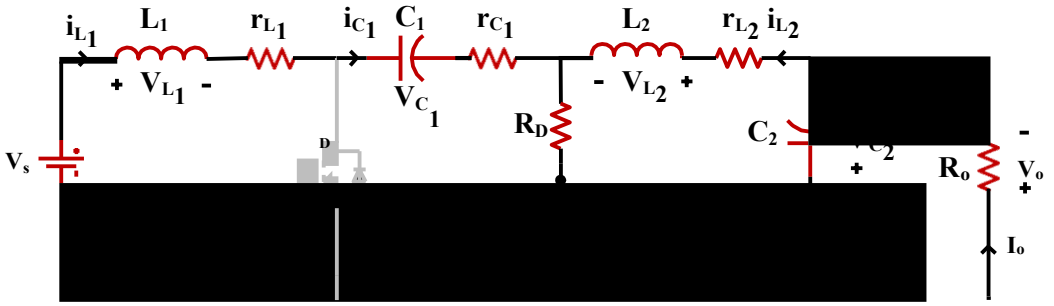
$$\ddot{\imath}_{C_1,oooo} = C_1 \frac{dV_{C_1}}{dt} = \ddot{\imath}_{L_1} \quad (2.45)$$

$$\ddot{\imath}_{C_2,oooo} = C_2 \frac{dV_{C_2}}{dt} = \frac{R_o}{R_o + r_{C_2}} \ddot{\imath}_{L_2} - \frac{V_{C_2}}{R_o + r_{C_2}} \quad (2.46)$$

$$V_o = \frac{R_o r_{C_2}}{R_o + r_{C_2}} \ddot{\imath}_{L_2} + \frac{R_o}{R_o + r_{C_2}} \quad (2.47)$$



(a)



(b)

Fig 2.12 Modes of operation (a) Mode 1 (b) Mode 2

2.3.3 Steady state analysis

In the context of steady-state analysis, the mean value of a current and voltage variable, denoted as X can be described as follows:

$$XX = \frac{1}{T}\int_0^T x(t)dt = \frac{1}{T}\int_0^{DT} x_{on}(t)dt + \frac{1}{T}\int_{DT}^T x_{ooooo}(t)dt \tag{2.48}$$

Where x_{on} and x_{off} denotes the variable $x(t)$ when switch is on and off respectively. According to the principle of volt-second balance for an inductor, over a full cycle of a switched-mode power supply, the cumulative voltage applied to an inductor equals zero i.e.,

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^{DT} v_{L,on}(t)dt + \frac{1}{T}\int_{DT}^T v_{L,ooooo}(t)dt = 0 \tag{2.49}$$

Similarly, as per the Ampere-Second balance for a capacitor, over a complete switching cycle, the net charge transferred to and from a capacitor equals zero, signifying a state of dynamic equilibrium. This is given by:

$$I_C = \frac{1}{T}\int_0^T i_C(t)dt = \frac{1}{T}\int_0^{DT} i_{C,on}(t)dt + \frac{1}{T}\int_{DT}^T i_{C,ooooo}(t)dt \tag{2.50}$$

Now using eq. (2.50) for capacitor C1 and C2 we get

$$I_{C_1} = \frac{1}{T}\int_0^T i_{C_1}(t)dt = \frac{1}{T}\int_0^{DT} i_{C_1,on}(t)dt + \frac{1}{T}\int_{DT}^T i_{C_1,ooooo}(t)dt \tag{2.51}$$

$$I_{C_1,avg} = D(-i_{L_2}) + (1-D)(i_{L_1}) = 0 \tag{2.52}$$

$$i_{L_1} = \frac{D}{D'} i_{L_2} \tag{2.53}$$

Now for capacitor C2,

$$I_{C_2} = \frac{1}{T}\int_0^T i_{C_2}(t)dt = \frac{1}{T}\int_0^{DT} i_{C_2,on}(t)dt + \frac{1}{T}\int_{DT}^T i_{C_2,ooooo}(t)dt \tag{2.54}$$

$$I_{C_2,avg} = D\left(i_{L_2} - \frac{V_o}{R_o}\right) + (1-D)\left(i_{L_2} - \frac{V_o}{R_o}\right) = 0 \tag{2.55}$$

$$i_{L_2} = \frac{V_o}{R_o} \tag{2.56}$$

Also, the average output voltage of the ideal Cuk converter is given by:

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = \frac{1}{T}\int_0^{DT} v_{o,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{o,ooooo}(t)dt \quad (2.58)$$

$$V_o = D\left(V_{C_2} + r_{C_2} i_{C_2}\right) + (1-D)\left(V_{C_2} + r_{C_2} i_{C_2}\right) \quad (2.59)$$

$$V_o = V_{C_2} \quad (2.60)$$

2.3.3.1 Expression for output Voltage

Applying KVL in the outer loop from the input voltage source to the output voltage gives us:

$$V_{C_1} = V_s - i_{L_1} r_{L_1} + i_{L_2} r_{L_2} + V_o \quad (2.57)$$

Applying volt-sec balance in inductor L_1 using Eqn. (2.49) we get,

$$V_S - i_{L_1}\left(r_{L_1} + DR_{ds} + D' r_{C_1} + D' R_D\right) - i_{L_2}\left(D r_{L_2} + D' R_D\right) - D' V_{C_1} = 0 \quad (2.58)$$

Substituting the value of $V_{C_1}, i_{L_1} and\ i_{L_2}$ from Eqn. (2.60), Eqn. (2.54) and Eqn. (2.57) we get the expression for output voltage as:

$$V_o = \frac{\frac{D}{D'} V_s}{1 + \frac{1}{R_o}\left(\frac{D}{D'}\right)^2 r_{L_1} + r_{L_2} + \frac{D r_{C_1}}{D'} + \frac{r_{eq}}{D'^2}} \quad (2.59)$$

Where $r_{eq} = DR_{ds} + D'R_D$

Table 2.2 Non-Ideal Cuk Converter Specifications

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1/r_{L_1}	0.384µH /0.1 Ω
Inductance L_2/r_{L_2}	0.768µH/0.1 Ω
Decoupling Capacitor,C_1/r_{C_1}	38.58µF/1 µΩ
Filter Capacitor, C_2/r_{C_2}	2µF/1 µΩ
Switching Frequency, f_{sss}	50kHz
Diode Resistance,R_D	0.1Ω
MOSFET Resistance, R_{ds}	0.25Ω
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\% I_{L_1}$/ $10\% I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\% V_{c_1}$/1% V_{c_2}

It's clear that the output voltage from a non-ideal Cuk DC-DC converter is influenced by more than just the duty cycle (D) and the input voltage (V_s). It also varies with the load resistance (R_o), as well as other parasitic resistances that are not ideal. These additional factors are crucial in understanding and predicting the behaviour of the

converter in real-world applications. Figure 2.9 illustrates how the output voltage of a non-ideal Cuk DC-DC converter varies with the duty cycle under different load resistances. The input voltage is set at 24V, and the load resistance is adjusted to 16Ω, 10Ω, and 5Ω. The additional effects of parasitic resistances, which can be referenced in Table 2.2, also play a significant role in this relationship.

In contrast to an ideal converter, where the output voltage linearly depends on the duty cycle, the non-ideal converter exhibits a more complex behaviour. Initially, as the duty cycle increases, the output voltage rises. This increase continues up to a certain point, after which the output voltage reaches a peak. Upon surpassing this peak, further increases in the duty cycle lead to a decrease in the output voltage. This characteristic curve is due to several non-ideal factors inherent in real components. Parasitic resistances, as indicated, along with other losses like those from non-ideal switch behaviour and diode forward voltage, introduce inefficiencies. These factors cause the energy transfer to be less effective at higher duty cycles beyond the optimal point, thus reducing the output voltage.

Understanding this behaviour is crucial for effectively utilizing Cuk converters in practical applications, where achieving maximum efficiency often requires operating at or near this optimum duty cycle.

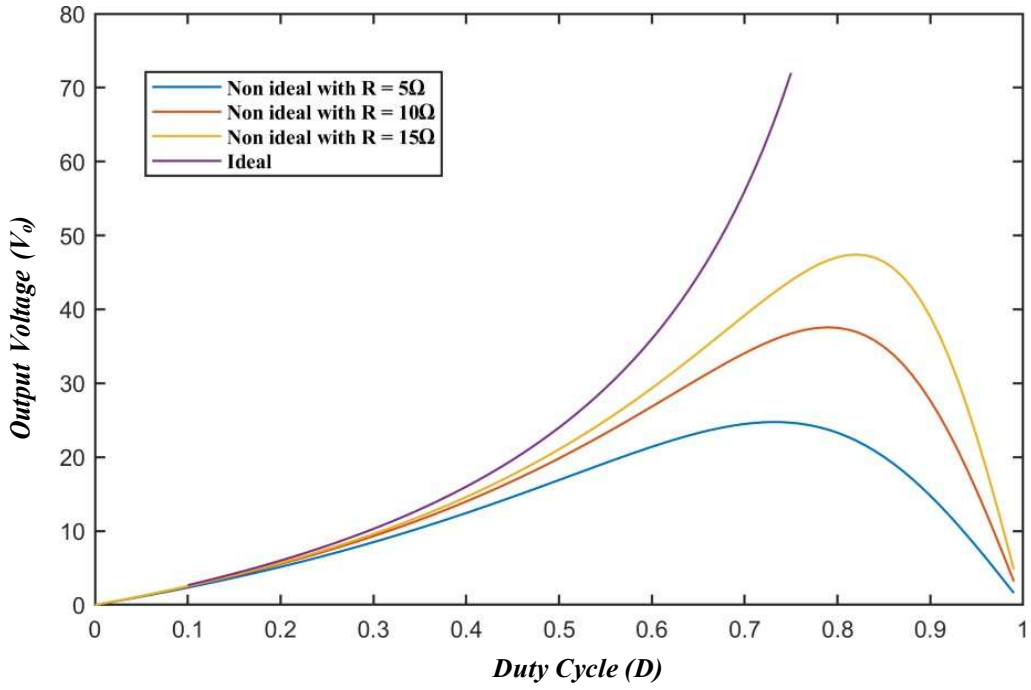


Fig 2.13 Output voltage of Non-ideal Cuk converter as a function of duty cycle

2.3.4 Inductor current ripple and inductor design

In a non-ideal Cuk converter, the design of inductors is a pivotal element that significantly impacts the converter's performance. These components are integral to energy storage and transfer within the system, directly affecting its efficiency, physical dimensions, and voltage regulation capabilities.

Let Δi_{L_1} *and* Δi_{L_2} be the desired ripple in inductor current (ICR) and x_{L_1} *and* x_{L_2} be the desired inductor current ripple factor (ICRF) for both the inductors. The relationship between the ICR and ICRF is given by:

$$x_{L_1} = \frac{\Delta i_{L_1}}{I_{L_1}}$$

Similarly,

$$x_{L_2} = \frac{\Delta i_{L_2}}{I_{L_2}} \tag{2.60}$$

Where, I_{L_1} *and* I_{L_2} are the average currents flowing through inductor L_1 and L_2.

2.3.4.1 Designing of inductor L_1

Under steady state using Eqn. (2.38), it can be written as:

$$\frac{\Delta i_{L_1}}{\Delta t} = \frac{V_s - r_{L_1} + R_{ds} i_{L_1} - R_{ds} i_{L_2}}{L_1} \tag{2.61}$$

When the MOSFET is on, $\Delta t = DT_s$, therefore the above equation becomes:

$$\Delta i_{L_1} = \frac{V_s - r_{L_1} + R_{ds} i_{L_1} - R_{ds} i_{L_2}}{L_1} DT_s \tag{2.62}$$

Substituting the value of i_{L_1} *and* i_{L_2} from Eqn. (2.54) and Eqn .(2.57) we get,

$$\Delta i_{L_1} = \frac{1}{L_1} V_s - r_{L_1} + R_{ds} \frac{DV_o}{D'R} - \frac{R_{ds} V_o}{R} DT_s \tag{2.63}$$

Simplifying the above equation yields,

$$\Delta i_{L_1} = \frac{DV_o}{L_1 f_s} \frac{V_s}{V_o} - \frac{1}{RD'} D r_{L_1} + R_{ds} \tag{2.64}$$

Now substituting the value of V_s/V_o from Eqn. (2.62) into Eqn. (2.67) we get,

$$\Delta i_{L_1} = \frac{D' V_o}{L_1 f_s}\left(1 + \frac{1}{R}\left(r_{L_2} + \frac{D r_C}{D'}\right) + \frac{R_d}{D'}\right) \quad (2.65)$$

Now from Eqn. (2.63) $\Delta i_{L_1} = x_{L_1} I_{L_1} = \frac{x_{L_1} D V_o}{D' R}$, we get,

$$L_1 = \frac{D'^2 R}{x_{L_1} f_s D}\left(1 + \frac{1}{R}\left(r_{L_2} + \frac{D r_C}{D'}\right) + \frac{R_d}{D'}\right) \quad (2.66)$$

2.3.4.2 Designing of inductor L_2

For inductor L_2, using the Eqn. 2.44 i.e. when the switch is off, it can be written as

$$\frac{\Delta i_{L_2}}{\Delta t} = \frac{-R_D i_{L_1} - r_{L_2} + R_D i_{L_2} - V_o}{L_2} \quad (2.67)$$

For the period when the MOSFET is turned of $\Delta t = (1 - D)T_s = D'T_s$. Therefore,

$$\frac{\Delta i_{L_2}}{\Delta t} = \frac{R_D i_{L_1} + r_{L_2} + R_D i_{L_2} + V_o}{L_2} D' T_s \quad (2.68)$$

Substituting the value of i_{L_1} and i_{L_2} from Eqn. (2.54) and Eqn. (2.57) we get,

$$\Delta i_{L_2} = \frac{D' V_o}{f_s L_2}\left(1 + \frac{1}{R}\left(r_{L_2} + \frac{R_D}{D'}\right)\right) \quad (2.69)$$

Now from Eqn. (2.63) $\Delta i_{L_2} = x_{L_2} I_{L_2} = \frac{x_{L_2} V_o}{R}$, we get,

$$L_2 = \frac{D' R}{x_{L_2} f_s}\left(1 + \frac{1}{R}\left(r_{L_2} + \frac{R_D}{D'}\right)\right) \quad (2.70)$$

Eqn. (2.69) and Eqn. (2.73) provides improved calculation of inductor when there are parasitic components are involved.

2.3.5 Capacitor design

In a non-ideal Cuk DC-DC converter, the additional resistances found in capacitors necessitate a careful approach to their design. These resistances can lead to energy losses, decreasing the overall efficiency of the system. Therefore, selecting the right capacity, voltage tolerance, and size for the capacitors is crucial to combat these energy losses. When designing capacitors for non-ideal Cuk DC-DC converters, one critical factor that must be considered is the Equivalent Series Resistance (ESR) of the capacitor. The ESR represents the internal resistance within the capacitor that can affect the converter's performance. High ESR can lead to significant energy losses,

heat generation, and reduced efficiency of the power conversion process. Therefore, choosing capacitors with low ESR is essential to enhance the system's overall performance. Low ESR capacitors improve energy transfer efficiency, minimize heating, and ensure a stable power output. By carefully selecting capacitors with appropriate ESR values, designers can effectively mitigate potential performance issues, leading to more reliable and efficient converter operations. This nuanced approach to capacitor selection underscores the importance of considering ESR in the design process for optimized circuit performance.

2.3.5.1 Capacitor C_1 &C_2

Let the ripple voltage across the capacitor C_1 and C_2 are ΔV_1 and ΔV_2. The ripple voltage is the sum of ripple voltage due to capacitor itself $\Delta V_{C_1} and\ \Delta V_{C_2}$ and the ripple voltage induces by the ESRs of the capacitor $\Delta v_{rc_1} and\ \Delta v_{rc_2}$.

$$\Delta V_1 \cong \Delta V_{C_1} + \Delta v_{rc_1} \tag{2.71}$$

Let rc_1 be the effective series resistance of the Capacitor C1. Therefore,

$$\Delta v_{rc_1} = rc_1 \Delta i_{C_1} \tag{2.72}$$

Now the change in capacitor current C_1 can be written as:

$$\Delta i_{C_1} = i_{L_1} + i_{L_2} + \frac{1}{2}(\Delta i_{C_2} - \Delta i_{C_1}) \tag{2.73}$$

Substituting the value of $i_{L_1}, i_{L_2}, \Delta i_{C_1} and\ \Delta i_{C_2}$ from Eqn. (2.54). Eqn. (2.57), Eqn.(2.67), Eqn. (2.72) into the above equation

$$\Delta i_{C_1} = \frac{V_o}{RD'} + \frac{D'V_o}{2f_s}\left(1 + \frac{1}{R}\right)\left(r_{L_2} + \frac{R_D}{D'}\right)\left(\frac{1}{L_2} - \frac{1}{L_1}\right) - \frac{rc_1 DV_o}{2fL_1} \tag{2.74}$$

Therefore substituting the value of eq.(2.77) in eq.(2.75) we get ,

$$\Delta v_{rc_1} = r_{c_1}\left(\frac{V_o}{RD'} + \frac{D'V_o}{2f_s}\right)\left(1 + \frac{1}{R}\right)\left(r_{L_2} + \frac{R_D}{D'}\right)\left(\frac{1}{L_2} - \frac{1}{L_1}\right) - \frac{rc_1 DV_o}{2fL_1}\Big) \tag{2.75}$$

Considering the Eqn. (2.70) , and also considering the average value of inductor current i_{L_2} we get,

$$i_{C_1,avg} = I_{00} \tag{2.76}$$

$$C_1 \frac{dV_{C_1}}{dt} = \frac{V_o}{R_o} \tag{2.77}$$

$$C_1 = \frac{V_o * D}{R_o * \Delta V_{C_1} * f_s} \tag{2.78}$$

$$C_1 = \frac{\frac{D}{R f_s (\Delta V_1 - \Delta v_{rc_1})}}{V_o} \tag{2.79}$$

This Eqn. (2.82) shows the minimum required value of capacitance.

Similarly, the minimum value of capacitance C_2 can be calculated as shown:

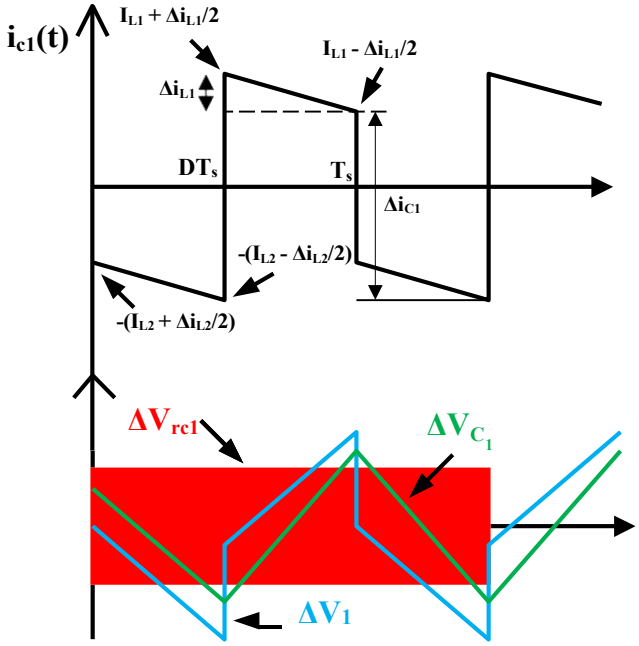


Fig 2.14 Current and ripple voltage waveforms associated with capacitor C_1

$$C_2 = \frac{V_o * (1 - D)}{8 * f_s^2 * \Delta V_{C_2} * L_2} \tag{2.80}$$

$$C_2 = \frac{\frac{1 - D}{8 f_s^2 L_2 (\Delta V_2 - \Delta v_{rc_2})}}{V_o} \tag{2.81}$$

2.3.6 Results and discussions

The results from simulations were conducted to corroborate the findings from the analytical research. These simulations were executed using the MATLAB/Simulink software suite.

The numerical values for the various parameters that were employed in both the simulation and the experimental phases are consistent with those presented in Table 2.2. Based on these parameters and referring to Eqn. (2.24), the ideal duty cycle was determined to be approximately 0.666. However, when accounting for the complexities introduced by non-ideal conditions, the duty cycle was recalculated and found to be slightly higher, at 0.725 based on Eqn. (2.62).

In terms of the simulations, the current waveforms for the inductor and the capacitor within the Cuk converter were depicted in Fig 2.15. Specifically, the average current values for the first and second inductors, denoted as i_{L_1} and i_{L_2} , respectively, reached 7 A and 3.473 A. Meanwhile, the ripples observed in the inductor currents, represented as Δi_{L_1} and Δi_{L_2}, were measured at 0.7176 A and 0.3605 A, respectively. Looking at the capacitor currents, their peak-to-peak values stood at 11.02 A for the first capacitor (C_1) and at 0.3605 A for the second capacitor (C_2).

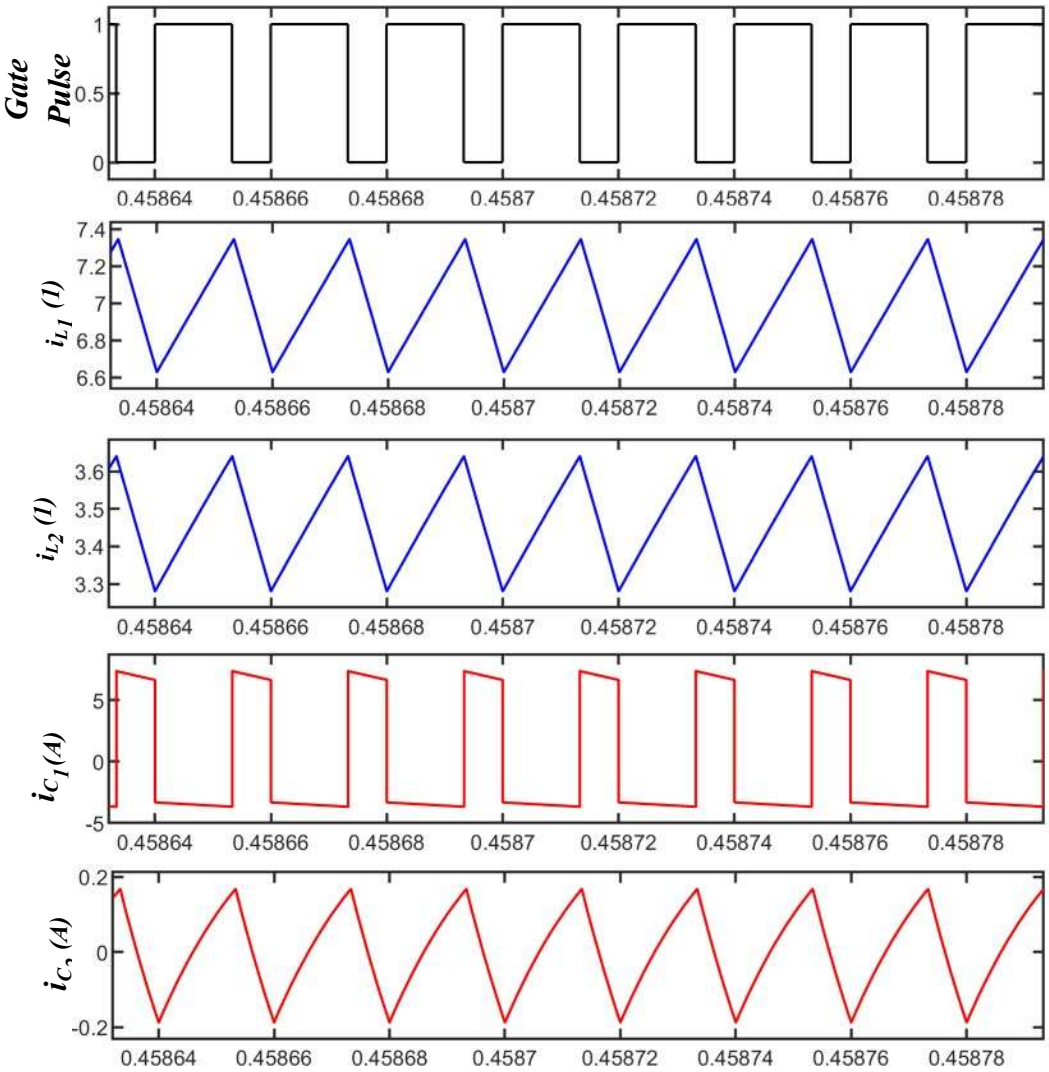


Fig 2.15 Current profiles of energy storing elements

The results of the simulated output voltage for the Cuk converter, employing the ideal duty cycle of D=0.666, are illustrated in Figure 2.23. During steady-state conditions, the output voltage stabilized at a value of 39.88 V, which fell short of the intended target of 48 V. Conversely, when the duty cycle was adjusted to the recalculated value of 0.725, in light of the relationship proposed, the desired steady-state output voltage of 48 V was successfully achieved. This finding is visually supported by the simulation data presented in Figure 2.16.

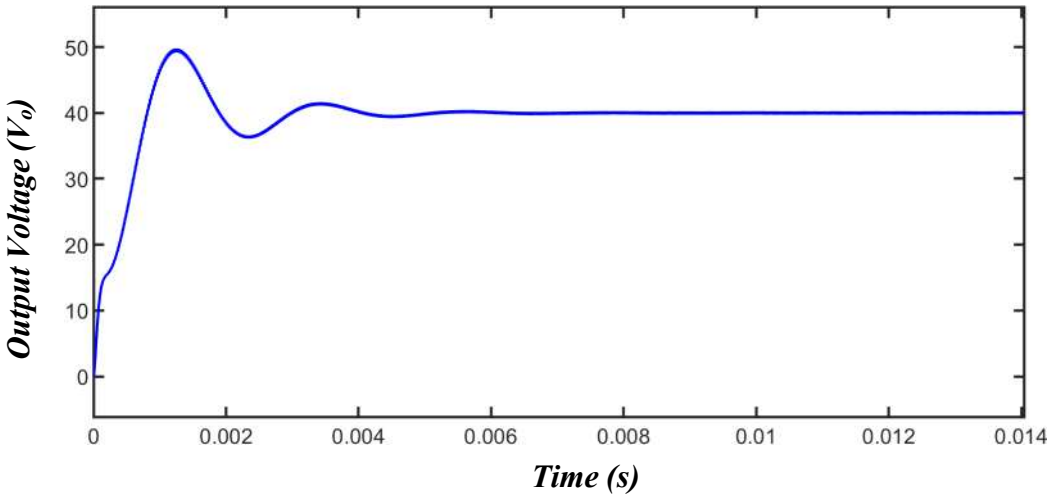


Fig 2.16 Output voltage response of ideal cuk converter at D = 0.66

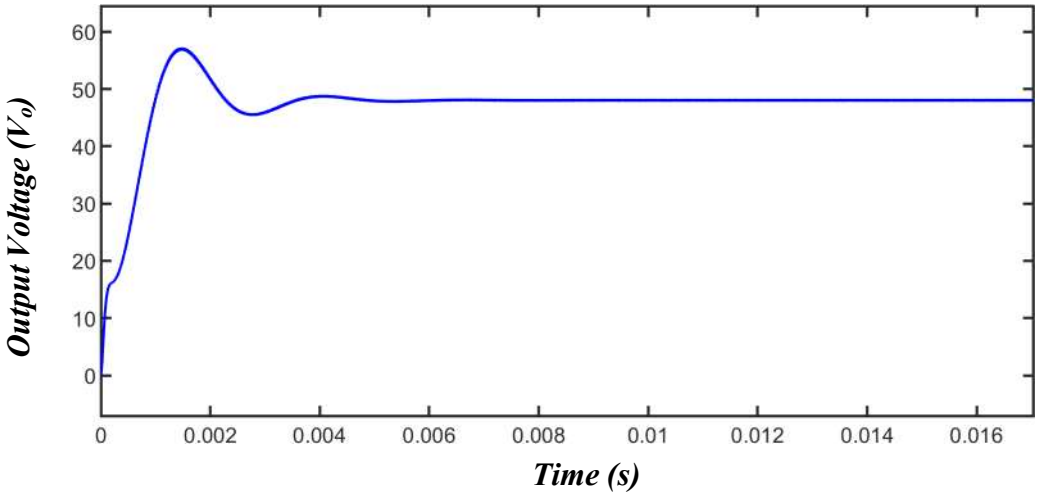


Fig 2.17 Output voltage response of Non-ideal Cuk converter at D = 0.725

The simulation's fidelity in capturing the behaviour of the converter with the implemented duty cycle adjustments demonstrates a solid agreement with the theoretical expectations, highlighting the accuracy of the model's predictions under different scenarios. It becomes evident that factoring in non-ideal elements is critical for refining the control strategy and achieving the specified performance outcomes of the Cuk converter.

2.4 Conclusion

In the comparison between ideal and non-ideal Cuk DC-DC converters, marked differences primarily emerge in terms of output voltage response and the design requirements for inductors and capacitors. In an ideal Cuk converter, the assumption is that there is no energy loss and components such as inductors and capacitors are considered perfect, which leads to a stable and predictable output voltage. However, in non-ideal converters, various non-idealities like the ESR (Equivalent Series Resistance) in capacitors and parasitic resistances in inductors introduce efficiency losses and voltage ripples in the output.

The presence of ESR in capacitors in non-ideal converters can significantly affect the transient response and stability of the output voltage. It demands a meticulous selection of low-ESR capacitors to minimize losses and improve efficiency. Similarly, the design of inductors must consider parasitic elements that can lead to undesirable effects such as higher ripple currents and reduced effectiveness in energy storage.

Therefore, designers must carefully optimize the characteristics of both inductors and capacitors, keeping in mind the specific challenges posed by the non-ideal factors in Cuk DC-DC converters. By focusing on these aspects, one can better manage the discrepancies in performance between ideal and non-ideal systems, aiming to enhance reliability and efficiency in practical applications.

CHAPTER 3
MODELLING OF DC-DC CONVERTER

3.1 Introduction

Modelling of both ideal and non-ideal DC-DC converters is a fundamental step in the design and development of efficient power conversion systems. This process is crucial because it allows engineers and designers to predict the behaviour of converters under various operating conditions. By understanding how these converters respond to different loads, input voltages, and other environmental factors, it becomes possible to optimize their performance, increase their efficiency, and ensure their reliability in practical applications.

Moreover, modelling plays a pivotal role in the design of controllers for these converters. A precise model helps in designing a controller that can accurately regulate the output voltage or current, maintain stability under dynamic conditions, and respond effectively to disturbances. This is particularly important in applications where power efficiency and response time are critical, such as in renewable energy systems, portable electronics, and automotive applications.

The state-space averaging technique is frequently employed in the thesis to model the converters due to its effectiveness in providing a simplified yet accurate representation of the system dynamics. This technique bridges the gap between complex electrical systems and the practical necessity for simplified models that can be easily analysed and used for control design.

3.2 State space averaging modelling technique

The state-space averaging technique is a method used to model and analyse the dynamic behaviour of power converters. This approach simplifies the inherently switched, nonlinear nature of DC-DC converters into linear time-invariant (LTI) systems over a switching period. By doing so, it enables the use of linear control theory for the design and analysis of converter controllers, which is significantly more straightforward and less time-consuming than dealing directly with nonlinear systems.

The technique involves several steps. First, it identifies the different states of the converter (e.g., on and off states) and models each state's circuit equations in state-space form. Next, it calculates the average of these state-space equations over one switching period, considering the duty cycle of the converter. This results in a set of averaged state-space equations that describe the converter's dynamics over time.

One of the key benefits of the state-space averaging technique is that it provides a detailed insight into the converter's behaviour by encompassing both the electrical characteristics and the control system dynamics in a unified framework. This holistic view is invaluable for optimizing converter design, improving performance, and enhancing reliability.

By using the state-space averaging technique, engineers can develop models that accurately reflect the real-world operation of both ideal and non-ideal DC-DC converters, thereby facilitating the design of efficient, robust power conversion systems and their controllers.

The state-space averaging technique simplifies the analysis and design of power electronic converters by converting their inherently nonlinear behaviour into linear time-invariant (LTI) models. The generalised state space averaging modelling technique is shown in the below steps:

Step 1: Identify System States

The first step involves identifying the different operational states of the converter. For a typical switched-mode power supply, these states correspond to the switching components (such as MOSFETs or diodes) being in either an 'on' or 'off' state.

In the analysis of DC-DC converters, each operational state of the converter is described through its own set of system equations. Generally, the state variables selected for modelling are the currents flowing through inductors and the voltages across capacitors. Thus, the total count of state variables is directly based on the number of inductors and capacitors present in the circuit. These state variables are encapsulated within a state variable vector, denoted as *x(t)*. For Continuous Conduction Mode (CCM), the state equations for the two operational circuit states can be expressed as follows:

(a) When the MOSFET is on during the switching interval$0 < t < DT_S$, the state equation is given as:

$$\frac{dx(t)}{dt} = A_1x(t) + B_1u(t) \quad (3.1)$$

$$y(t) = E_1x(t) + F_1u(t) \quad (3.2)$$

When the MOSFET is off during the switching interval DT < t < T, the state equation is given as:

$$\frac{dx(t)}{dt} = A_2x(t) + B_2u(t) \quad (3.3)$$

$$y(t) = E_2x(t) + F_2u(t) \quad (3.4)$$

Where $x(t)$ is the state variable vector, including inductor currents and capacitor voltages, among others, controlled input denoted as $u(t)$, and output vector denoted as $y(t)$. The state matrix is denoted as A, the input matrix as B, the output matrix as E, and the output coupling matrix as F.

Step 2: State Space Averaging equation

For each state variable, average the state equations over one switching period, taking into account the duty cycle. To remove the switching ripple component from the circuit equations, averaging over one switching period is done. This involves multiplying the state equations for the 'on' state by (D) and the equations for the 'off' state by (1-D), and then summing these results. This step effectively linearizes the model, making it amenable to analysis and design using linear control theory.

$$\frac{d\bar{x}(t)}{dt} = A\bar{x}(t) + B\bar{u}(t) \quad (3.5)$$

$$\bar{y}(t) = C\bar{x}(t) + D\bar{u}(t) \quad (3.6)$$

Where,

$$A = A_1 * d(t) + A_2 * (1 - d(t)) \quad (3.7)$$

$$B = B_1 * d(t) + B_2 * (1 - d(t)) \quad (3.8)$$

$$E = E_1 * d(t) + E_2(1 - d(t)) \quad (3.9)$$

$$F = F_1 * d(t) + F_2(1 - d(t)) \quad (3.10)$$

In the context of the averaged state-space model, the overline symbol (-) denotes the average value of a variable over the entirety of a switching period. The equations

presented as Eqn. (3.5) and eqn. (3.6) exhibit nonlinearity, which arises from the multiplication of quantities that vary with time.

Step 3: Perturbation and Linearisation of averaged state space model

To analyse and control systems with nonlinear dynamics, as seen in the averaged state-space models, we often employ perturbation and linearization methods. These involve small deviations around a steady operational point to yield a linear approximation of the system's behaviour. This process simplifies the design of control strategies and system analysis, especially within power electronics domains.

The small ac perturbation introduced around steady state values are as follows:

$$\bar{x}(t) = \mathrm{X} + \hat{x}(t) \ , \bar{y}(t) = Y + \hat{y}(t) \tag{3.11}$$

$$d(t) = D + \hat{d}(t), \quad d'(t) = 1 - d(t) = 1 - D - \hat{d}(t) = D' - \hat{d}(t)$$

It is to note that $\mathrm{X} \gg \hat{x}(t), Y \gg \hat{y}(t), U \gg \hat{u}(t) and\ D \gg \hat{d}(t)$. (3.12)

By substituting the Eqn.(3.11) into Eqn. (3.5)-(3.6) we get,

$$\dot{\mathrm{X}} + \dot{\hat{x}}(t) = \{A_1 \{D + \hat{d}(t)\} + A_2 \{1 - D - \hat{d}(t)\}\}\mathrm{X} + \hat{x}(t)\} + \{B_1 \{D + \hat{d}(t)\} + B_2 \{1 - D - \hat{d}(t)\}\}U + \hat{u}(t)\}$$

On simplifying we get,

$$\begin{aligned}\dot{\mathrm{X}} + \dot{\hat{x}}(t) = \{&A_1 D + A_2(1 - D) + (A_1 - A_2)\hat{d}(t)\}\mathrm{X} + \hat{x}(t)\} \\ &+ \{B_1 D + B_2(1 - D) + (B_1 - B_2)\hat{d}\}U + \hat{u}(t)\}\end{aligned} \tag{3.13}$$

Similarly,

$$Y + \hat{y}(t) = \{E_1 \{D + \hat{d}(t)\} + E_2 \{1 - D - \hat{d}(t)\}\}\mathrm{X} + \hat{x}(t)\} + \{F_1 \{D + \hat{d}(t)\} + F_2 \{1 - D - \hat{d}(t)\}\}U + \hat{u}(t)\} \tag{3.14}$$

Simplifying the above equation yields, (3.15)

$$\begin{aligned}Y + \hat{y}(t) = \{&E_1 D + E_2(1 - D) + (E_1 - E_2)\hat{d}(t)\}\mathrm{X} + \hat{x}(t)\} \\ &+ \{F_1 D + F_2(1 - D) + (F_1 - F_2)\hat{d}\}U + \hat{u}(t)\}\end{aligned}$$

To derive the linear model, we overlook the second-order nonlinear terms, which involve the multiplication of two small AC perturbed signals, as mentioned in equations (3.13) to (3.15). As a result, we obtain:

$$\dot{X} + \hat{x}(t) = \left(A_1 D + A_2(1-D)\right)X + \left(A_1 D + A_2(1-D)\right)\hat{x}(t) + (A_1 - A_2)X\hat{d}(t) + \left(B_1 D + B_2(1-D)\right)U + \left(B_1 D + B_2(1-D)\right)\hat{u}(t) + (B_1 - B_2)U\hat{d}(t) \quad (3.16)$$

$$Y + \hat{y}(t) = \hat{E_1}D + E_2(1-D)\hat{X} + \hat{E_1}D + E_2(1-D)\hat{x}(t) + (E_1 - E_2)X\hat{d}(t) + \hat{F_1}D + F_2(1-D)\hat{U} + \hat{F_1}D + F_2(1-D)\hat{u}(t) + (F_1 - F_2)U\hat{d}(t) \quad (3.17)$$

Now the above equations can be written as:

$$\dot{X} + \hat{x}(t) = AX + BU + A\hat{x}(t) + B\hat{u}(t) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(t) \quad (3.18)$$

$$Y + \hat{y}(t) = EX + FU + E\hat{x}(t) + F\hat{u}(t) + [(E_1 - E_2)X + (F_1 - F_2)U]\hat{d}(t) \quad (3.19)$$

$$WWhere\ , A = A_1D + A_2(1-D), B = B_1D + B_2(1-D), E = E_1D + E_2(1-D), F = F_1D + F_2(1-D) \quad (3.20)$$

3.2.1 Small signal Ac model

Separating out the small signal ac terms from Eqn. (3.18) - (3.19), we get

$$\hat{x} = A\hat{x}(t) + B\hat{u}(t) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(t) \quad (3.21)$$

$$\hat{y}(t) = E\hat{x}(t) + F\hat{u}(t) + [(E_1 - E_2)X + (F_1 - F_2)U]\hat{d}(t) \quad (3.22)$$

To determine the different transfer functions, we apply the Laplace transform to the aforementioned state-space model, yielding the following expression:

$$s\hat{x}(s) = A\hat{x}(s) + B\hat{u}(s) + [(A_1 - A_2)X(s) + (B_1 - B_2)U(s)]\hat{d}(s) \quad (3.23)$$

$$\hat{y}(s) = E\hat{x}(s) + F\hat{u}(s) + [(E_1 - E_2)X(s) + (F_1 - F_2)U(s)]\hat{d}(s) \quad (3.24)$$

Eqn. (3.23) and Eqn. (3.24) serve as the basis for extracting a range of transfer functions specific to DC-DC converters. Within the context of a DC-DC converter, the variable (x) is associated with the fluctuations in inductor current and capacitor voltage, while (u) corresponds to variations in input voltage and load current. The symbol (d) is linked with changes in the duty cycle, and (y) signifies adjustments in the output voltage. By analysing these equations, we can formulate the transfer functions that map the relationship between these perturbations as detailed in Eqn. (3.25) -(3.26).

The transfer functions that link the duty cycle (d) and input variables (u) to the state variables (x) are expressed as follows:

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (sI - A)^{-1}[(A_1 - A_2)X(s) + (B_1 - B_2)U(s)] \quad (3.25)$$

$$\frac{\hat{x}(s)}{\hat{u}(s)} = (sI - A)^{-1}B \tag{3.26}$$

The relationships between the duty cycle (d) and the input parameters (u) to the output response (y) are characterized by a set of transfer functions.

$$\frac{\hat{y}(s)}{\hat{d}(s)} = E(sI - A)^{-1}[(A_1 - A_2)X(s) + (B_1 - B_2)U(s)] + [(E_1 - E_2)X + (F_1 - F_2)U] \tag{3.27}$$

$$\frac{\hat{y}(s)}{\hat{u}(s)} = E(sI - A)^{-1}B + F \tag{3.28}$$

In the following subsections, we will derive the transfer functions for both ideal and non-ideal Cuk converters, taking into account all non-ideal characteristics. These characteristics encompass the equivalent series resistances (ESRs) of inductors and capacitors, as well as the parasitic resistances inherent to the diode and MOSFET when they are in the conduction state.

3.2.2 Modelling of Ideal Cuk converter

The Cuk converter, a type of DC-DC converter, features a distinct circuit structure that includes two inductors, two capacitors, a switch (typically a MOSFET), and a diode. This setup helps in providing a stable output voltage or current by transferring energy through the capacitors, thereby enhancing the stability of power delivery even under varying load conditions.

Modelling the ideal Cuk converter involves understanding this basic circuit design, which remains consistent with the discussion in the previous chapter. The circuit is characterized by instantaneous currents and voltages, which vary over time. Notably, at the output stage, an additional current source, denoted as ($i_z(t)$), is incorporated. This modification aims to assess the dynamic effects that variations in the load current have on the output voltage response.

In this section, we shift our focus to the modelling of an ideal DC-DC Cuk converter. This analysis assumes the converter operates in Continuous Conduction Mode (CCM). During CCM operation, a DC-DC Cuk converter transitions between two distinct states: (a) when the MOSFET switch is active (conducting) and the diode is inactive

(not conducting), and (b) when the MOSFET switch is inactive (not conducting) and the diode takes over (conducting). We derive the state-space equations for these two circuit states to understand the dynamics of the converter under ideal conditions better:

Step 1: Identifying System States and obtain the state space equations.

State 1: Switch ON duration ($0 < t < DT_s$)

In the ideal Cük converter operation, the initial state involves the switch, usually a MOSFET, being closed. This action allows energy transfer from the input source, through the inductors, and into the capacitors. Using Kirchhoff's voltage and current law, the inductor voltage, capacitor current and output voltage equation is given by:

$$V_{L_1}(t) = L_1 \frac{di_{L_1}(t)}{dt} = V_s(t) \tag{3.29}$$

$$V_{L_2}(t) = L_2 \frac{di_{L_2}(t)}{dt} = V_{C_1}(t) - V_{C_2}(t) \tag{3.30}$$

$$i_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = i_{L_2}(t) \tag{3.31}$$

$$i_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = i_{L_2}(t) - \frac{V_{C_2}(t)}{R_o} \tag{3.32}$$

$$V_o(t) = V_{C_2}(t) \tag{3.33}$$

Equations Eqn. (3.29)-Eqn. (3.33) can be written in state space representation as:

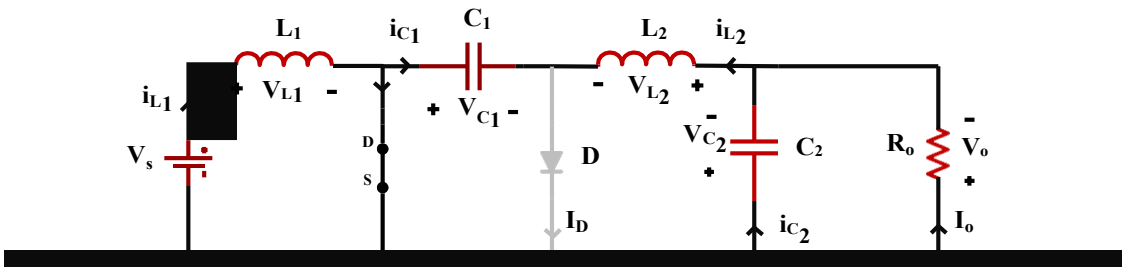
$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = A_1 \begin{matrix} i_{L_1} \\ i_{L_2} \\ V_{C_1} \\ V_{C_2} \end{matrix} + B_1 [V_s] \tag{3.34}$$

$$[V_o] = E_1 \begin{matrix} i_{L_1} \\ i_{L_2} \\ V_{C_1} \\ V_{C_2} \end{matrix} + F_1[V_s] \tag{3.35}$$

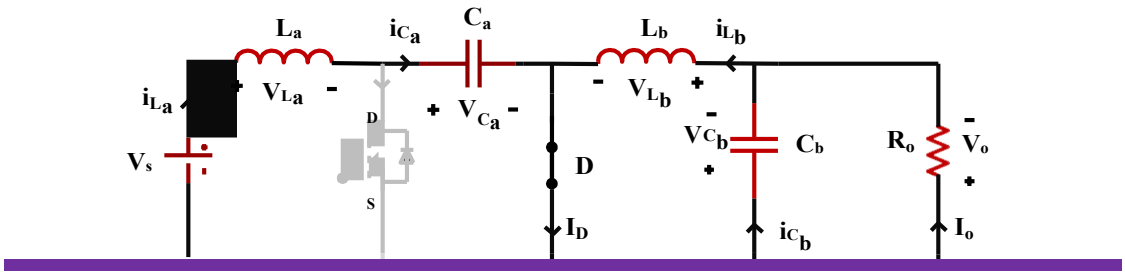
Where,

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -\frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 1 & 0 & -\frac{1}{R_o C_2} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$E_1 = [0 \quad 0 \quad 0 \quad 1], F_1 = [0] \tag{3.36}$$



(a)



(b)

Fig 3.1 Circuit diagram of ideal Cuk converter (a) equivalent circuit during switch-on (b) equivalent circuit during switch-off

State 2: Switch OFF duration ($DT_s < t < T_s$):

During the subsequent state, the MOSFET switch is opened, allowing the diode to conduct. This transition enables a steady flow of energy from the capacitors to the output load. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltages, capacitor currents and output voltage equations are given as:

$$V_{L_1}(t) = L_1 \frac{d\ddot{\imath}_{L_1}(t)}{dt} = V_s(t) - V_{C_1}(t) \tag{3.37}$$

$$V_{L_2}(t) = L_2 \frac{d\ddot{\imath}_{L_2}(t)}{dt} = -V_{C_2}(t) \tag{3.38}$$

$$\ddot{\imath}_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = -\ddot{\imath}_{L_1}(t) \tag{3.39}$$

$$\ddot{\imath}_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = \ddot{\imath}_{L_2}(t) - \frac{V_{C_2}(t)}{R_o} \tag{3.40}$$

$$V_{OO}(t) = V_{C_2}(t) \tag{3.41}$$

Equations Eqn. (3.37)-Eqn. (3.41) can be written in state space representation as:

$$\begin{bmatrix} \frac{d\ddot{\imath}_{L_1}}{dt} \\ \frac{d\ddot{\imath}_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = A_2 \begin{matrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{matrix} + B_2 [V_s] \tag{3.42}$$

$$[V_o] = E_2 \begin{matrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{matrix} + F_2[V_s] \tag{3.43}$$

Where,

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 1 & 0 & \frac{-1}{R_o C_2} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.44}$$

$$E_2 = [0 \quad 0 \quad 0 \quad 1], F_2 = [0]$$

Step2: State Space Averaging equation

According to the discussion in section 3.2.1, the large-signal non-linear averaged state-space model of ideal Cuk converter can be given as:

$$\begin{bmatrix} \frac{d\bar{i}_{L_1}}{dt} \\ \frac{d\bar{i}_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = \bar{A} \begin{bmatrix} \bar{i}_{L_1} \\ \bar{i}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + \bar{B}[V_s] \tag{3.45}$$

$$[V_o] = \bar{E} \begin{bmatrix} \bar{i}_{L_1} \\ \bar{i}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + \bar{F}[V_s] \tag{3.46}$$

Where

$$\bar{A} = A_1 * D + A_2 * (1 - D), \bar{B} = B_1 * D + B_2 * (1 - D)$$
$$\bar{E} = E_1 * D + E_2 * (1 - D), \bar{F} = F_1 * d + F_2 * (1 - D) \tag{3.47}$$

Step 3: Perturbation and Linearisation of averaged state space model

In this context, we introduce small variations to certain variables, relative to their normal, constant (DC) values. These changes are made to examine how the system behaves around its equilibrium or steady-state condition.

$$\bar{i}_{L_1}(t) = I_{L_1} + \hat{i}_{L_1}(t), \bar{i}_{L_2}(t) = I_{L_2} + \hat{i}_{L_2}(t)$$
$$V_s(t) = V_s + \hat{v}_s(t), d(t) = D + \hat{d}(t) \tag{3.48}$$
$$V_{C_1}(t) = V_{C_1} + \hat{v}_{C_1}(t), V_{C_2}(t) = V_{C_2} + \hat{v}_{C_2}(t), V_o(t) = V_o + \hat{v}_o(t)$$

By introducing these perturbation, and ignoring the higher order ac terms we can obtain the small signal ac model of an ideal Cuk converter which will be given as:

$$\begin{bmatrix} \frac{d\hat{i}_{L_1}}{dt} \\ \frac{d\hat{i}_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = A \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + B[V_s] \tag{3.49}$$

$$[\hat{v}_o] = E \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C1} \\ \hat{v}_{C_2} \end{bmatrix} + F[\hat{v}_s] \tag{3.50}$$

Step 4: Derivation of Transfer Function

Now, by taking the Laplace transform and using Eqn. (3.25) and Eqn. (3.28), We can calculate various transfer function

1. **Line to Output voltage transfer function:** The transfer function of input voltage to output voltage in an ideal Cuk converter describes how the output voltage changes in response to variations in the input voltage.

$$\frac{\hat{v}_o(s)}{\hat{v}_s(s)} = G_{vvv}(s) = C(sI - A)^{-1}[B]_{first\ coloumn} \tag{3.51}$$

$$G_{vvv}(s) = \frac{\frac{DD'}{L_1L_2C_1C_2}}{s^4 + \frac{1}{RC_2}s^3 + \left(\frac{D'^2}{L_1C_1} + \frac{D^2}{L_2C_1} + \frac{1}{L_2C_2}\right)s^2 + \frac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \frac{D'^2}{L_1L_2C_1C_2}} \tag{3.52}$$

2. **Load Current to output voltage transfer Function:** The load current to output voltage transfer function for an ideal Cuk converter characterizes how the voltage supplied to the load is affected as the amount of current the load draws vary, demonstrating the output regulation capabilities of the converter. This function is essential for assessing the response of the converter when facing different load conditions, ensuring it can provide a consistent output voltage despite fluctuations in load current. Understanding this relationship helps in optimizing the converter design to achieve better performance and reliability in practical applications.

$$\frac{\hat{v}_o(s)}{\hat{i}_z(s)} = G_{vz}(s) = C(sI - A)^{-1}[B]_{second\ coloumn} \tag{3.53}$$

$$G_{vz}(s) = \frac{-\frac{1}{L_1L_2C_1C_3}(L_1L_2C_2s^3 + (D^2L_1 + D'^2L_2)s)}{s^4 + \frac{1}{RC_2}s^3 + \left(\frac{D'^2}{L_1C_1} + \frac{D^2}{L_2C_1} + \frac{1}{L_2C_2}\right)s^2 + \frac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \frac{D'^2}{L_1L_2C_1C_2}} \tag{3.54}$$

3. **Control to Output Transfer Function:** The duty cycle to output voltage transfer function in an ideal Cuk converter describes how changes in the duty cycle influence the output voltage. This relationship is critical for controlling and adjusting the voltage output to meet specific requirements of the load, ensuring efficient power delivery across varying operating conditions

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_{vd}(s) = C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \quad (3.55)$$

$$G_{vd}(s) = \frac{-\frac{1}{L_1L_2C_1C_2}\left(L_1C_1V_{C_1}s^2 - L_1I_{L_1}s + D'V_{C_1}\right)}{s^4 + \frac{1}{RC_2}s^3 + \left(\frac{D'^2}{L_1C_1} + \frac{D^2}{L_2C_1} + \frac{1}{L_2C_2}\right)s^2 + \frac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \frac{D'^2}{L_1L_2C_1C_2}} \quad (3.56)$$

3.2.3 Modelling of Non-Ideal Cuk converter

When modelling a non-ideal Cuk converter, it's important to incorporate various real-world imperfections to enhance the accuracy of the predictions regarding its behaviour. This includes considering the finite on-resistance of switches, which leads to power losses, and that affects efficiency. Additionally, components like inductors and capacitors have an equivalent series resistance (ESR), introducing losses that impact output ripple and stability. In the continuous conduction mode (CCM) of operation, the Cuk converter operates through two distinct circuit states: firstly, when the MOSFET switch is engaged and the diode is not conducting, and secondly, when the MOSFET is turned off, allowing the diode to conduct. To establish both the steady-state and small-signal models of the Cuk converter, the averaged-switch model technique is employed, which can be broken down into a series of steps as described below:

Step 1: Identifying System States and obtain the state space equations.

State 1: Switch ON duration $(0 < t < DT_s)$:

In the non-ideal Cük converter operation, the initial state involves the switch, usually a MOSFET, being closed. This action allows energy transfer from the input source, through the inductors, and into the capacitors. Using Kirchhoff's voltage and current law, the inductor voltage, capacitor current and output voltage equation is given by:

$$V_{L_1}(t) = L_1 \frac{d\ddot{\imath}_{L_1}(t)}{dt} = V_s(t) - \blacklozenge r_{L_1} + R_{ds}\blacklozenge\ddot{\imath}_{L_1}(t) - R_{ds}\ddot{\imath}_{L_2}(t) \tag{3.57}$$

$$V_{L_2}(t) = L_2 \frac{d\ddot{\imath}_{L_2}(t)}{dt}$$

$$= -R_{ds}\ddot{\imath}_{L_1}(t) - \blacklozenge R_{ds} + r_{C_1} + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}\blacklozenge\ddot{\imath}_{L_2}(t) + V_{C_1}(t) \tag{3.58}$$

$$- \blacklozenge\frac{R_o}{R_o + r_{C_2}}\blacklozenge V_{C_2}(t)$$

$$\ddot{\imath}_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = -\ddot{\imath}_{L_2}(t) \tag{3.59}$$

$$\ddot{\imath}_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = \frac{R_o}{R_o + r_{C_2}}\ddot{\imath}_{L_2}(t) - \frac{V_{C_2}(t)}{R_o + r_{C_2}} \tag{3.60}$$

$$V_o(t) = \frac{R_o r_{C_2}}{R_o + r_{C_2}}\ddot{\imath}_{L_2}(t) + \frac{R_o}{R_o + r_{C_2}} V_{C_2}(t) \tag{3.61}$$

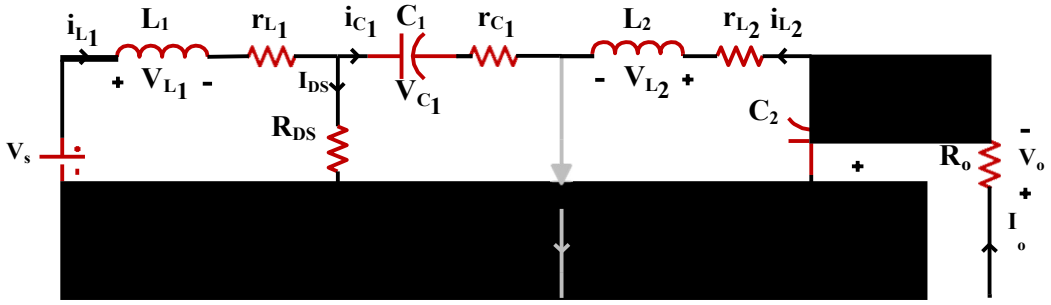
The above equations can be represented in state space form as follows:

$$\begin{bmatrix} \frac{d\ddot{\imath}_{L_1}}{dt} \\ \frac{d\ddot{\imath}_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = A_1 \begin{bmatrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + B_1 [V_s] \tag{3.62}$$

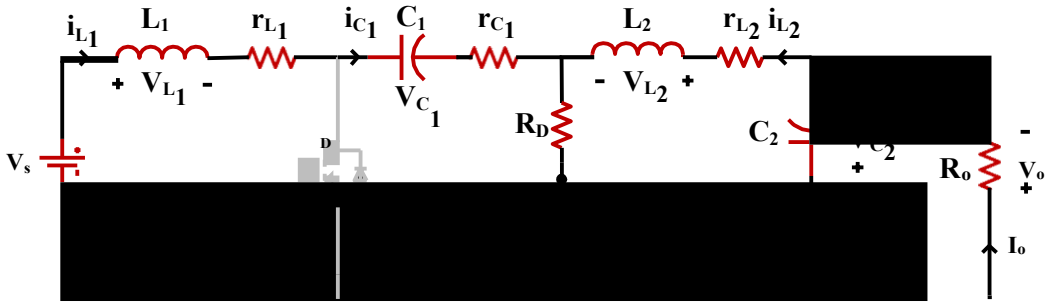
$$[V_o] = E_1 \begin{bmatrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + F_1[V_s] \tag{3.63}$$

$$A_1 = \begin{bmatrix} -\frac{r_{L_1} + R_{ds}}{L_1} & -\frac{R_{ds}}{L_1} & 0 & 0 \\ -\frac{R_{ds}}{L_2} & -\frac{R_{ds} + r_{C_1} + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}}{L_2} & \frac{1}{L_2} & -\frac{\frac{R_o}{R_o + r_{C_2}}}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{\frac{R_o}{R_o + r_{C_2}}}{C_2} & 0 & -\frac{\frac{1}{R_o + r_{C_2}}}{C_2} \end{bmatrix} \quad (3.64)$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, E_1 = \begin{bmatrix} 0 & \frac{R_o r_{C_2}}{R_o + r_{C_2}} & 0 & \frac{R_o}{R_o + r_{C_2}} \end{bmatrix}, F_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$



(a)



(b)

Fig 3.2 Circuit diagram of non-ideal DC-DC Cuk converter (b) equivalent circuit during switch-on (c) equivalent circuit during switch of

State 2: Switch OFF duration($DT_s < t < T_s$):

During the subsequent state, the MOSFET switch is opened, allowing the diode to conduct. This transition enables a steady flow of energy from the capacitors to the output load. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltages, capacitor currents and output voltage equations are given as:

$$V_{L_1}(t) = L_1 \frac{d\ddot{\imath}_{L_1}(t)}{dt} = V_s(t) - \left(r_{L_1} + r_{C_1} + R_D\right)\ddot{\imath}_{L_1}(t) - R_D\ddot{\imath}_{L_2}(t) - V_{C_1}(t) \tag{3.65}$$

$$\begin{aligned} V_{L_2}(t) &= L_2 \frac{d\ddot{\imath}_{L_2}(t)}{dt} \\ &= -R_D\ddot{\imath}_{L_1}(t) - \left(R_D + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}\right)\ddot{\imath}_{L_2}(t) - \left(\frac{R_o}{R_o + r_{C_2}}\right)V_{C_2}(t) \end{aligned} \tag{3.66}$$

$$\ddot{\imath}_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = \ddot{\imath}_{L_1}(t) \tag{3.67}$$

$$\ddot{\imath}_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = \frac{R_o}{R_o + r_{C_2}}\ddot{\imath}_{L_2}(t) - \frac{V_{C_2}(t)}{R_o + r_{C_2}} \tag{3.68}$$

$$V_o(t) = \frac{R_o r_{C_2}}{R_o + r_{C_2}}\ddot{\imath}_{L_2}(t) + \frac{R_o}{R_o + r_{C_2}}V_{C_2}(t) \tag{3.69}$$

The above equations can be represented in state space form as follows:

$$\begin{bmatrix} \frac{d\ddot{\imath}_{L_1}}{dt} \\ \frac{d\ddot{\imath}_{L_2}}{dt} \\ \frac{dV_{C_1}}{dt} \\ \frac{dV_{C_2}}{dt} \end{bmatrix} = A_2 \begin{bmatrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + B_2 [V_s] \tag{3.70}$$

$$[V_o] = E_2 \begin{bmatrix} \ddot{\imath}_{L_1} \\ \ddot{\imath}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + F_2[V_s] \tag{3.71}$$

Where,

$$A_2 = \begin{bmatrix} -\frac{r_{L_1} + r_{C_1} + R_D}{L_1} & -\frac{R_D}{L_1} & -1 & 0 \\ -\frac{R_D}{L_2} & -\frac{R_D + r_{L_2} + \frac{R_o r_{C_2}}{R_o + r_{C_2}}}{L_2} & 0 & -\frac{\frac{R_o}{R_o + r_{C_2}}}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{\frac{R_o}{R_o + r_{C_2}}}{C_2} & 0 & -\frac{\frac{1}{R_o + r_{C_2}}}{C_2} \end{bmatrix} \quad (3.72)$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, C_2 = \begin{bmatrix} 0 & \frac{R_o r_{C_2}}{R_o + r_{C_2}} & 0 & \frac{R_o}{R_o + r_{C_2}} \end{bmatrix}, D_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

Step2: State Space Averaging equation

According to the discussion in section 3.2.1, the large-signal non-linear averaged state-space model of ideal Cuk converter can be given as:

$$\begin{bmatrix} \frac{d\bar{i}_{L_1}}{dt} \\ \frac{d\bar{i}_{L_2}}{dt} \\ \frac{d\bar{v}_{C_1}}{dt} \\ \frac{d\bar{v}_{C_2}}{dt} \end{bmatrix} = \bar{A} \begin{bmatrix} \bar{i}_{L_1} \\ \bar{i}_{L_2} \\ \bar{v}_{C_1} \\ \bar{v}_{C_2} \end{bmatrix} + \bar{B}[\bar{v}_s] \quad (3.73)$$

$$[\bar{v}_o] = \bar{E} \begin{bmatrix} \bar{i}_{L_1} \\ \bar{i}_{L_2} \\ V_{C_1} \\ V_{C_2} \end{bmatrix} + \bar{F}[\bar{v}_s] \quad (3.74)$$

Where

$$\bar{A} = A_1 * D + A_2 * (1 - D), \bar{B} = B_1 * D + B_2 * (1 - D)$$
$$\bar{E} = E_1 * D + E_2 * (1 - D), \bar{F} = F_1 * d + F_2 * (1 - D) \quad (3.75)$$

Step 3: Perturbation and Linearisation of averaged state space model

In this context, we introduce small variations to certain variables, relative to their normal, constant (DC) values. These changes are made to examine how the system behaves around its equilibrium or steady-state condition.

$$\bar{\imath}_{L_1}(t) = I_{L_1} + \hat{\imath}_{L_1}(t), \bar{\imath}_{L_2}(t) = I_{L_2} + \hat{\imath}_{L_2}(t)$$
$$\bar{v}_s(t) = V_s + \hat{v}_s(t), d(t) = D + \hat{d}(t) \tag{3.76}$$
$$\bar{v}_{C_1}(t) = V_{C_1} + \hat{v}_{C_1}(t), \bar{v}_{C_2}(t) = V_{C_2} + \hat{v}_{C_2}(t), \bar{v}_o(t) = V_o + \hat{v}_o(t)$$

By introducing these perturbation, and ignoring the higher order ac terms we can obtain the small signal ac model of an ideal Cuk converter which will be given as:

$$\begin{bmatrix} \frac{d\hat{\imath}_{L_1}}{dt} \\ \frac{d\hat{\imath}_{L_2}}{dt} \\ \frac{d\hat{v}_{C_1}}{dt} \\ \frac{d\hat{v}_{C_2}}{dt} \end{bmatrix} = A \begin{bmatrix} \hat{\imath}_{L_1} \\ \hat{\imath}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix} + B[\hat{v}_s] \tag{3.77}$$

$$[\hat{v}_o] = E \begin{bmatrix} \hat{\imath}_{L_1} \\ \hat{\imath}_{L_2} \\ \hat{v}_{C1} \\ \hat{v}_{C_2} \end{bmatrix} + F[\hat{v}_s] \tag{3.78}$$

Step 4: Derivation of Transfer Function

Now, by taking the Laplace transform and using Eqn. (3.25) and Eqn. (3.28), We can calculate various transfer function:

1. **Line to Output Transfer Function**: This transfer function illustrates the impact of fluctuations or disruptions in the input voltage on the output voltage. To derive this transfer function, the influences of variations in the duty cycle and the output current are presumed to be negligible. Therefore, employing Eqn. (3.28) allows us to establish the relationship between changes in input voltage and their effects on output voltage within this specific context.

$$\frac{\hat{v}_o(s)}{\hat{v}_s(s)} = G_{vvv}(s) = C(sI - A)^{-1}[B]_{first\ coloumn} \tag{3.79}$$

$$G_{vvv}(s) = \frac{K_{vvv}(sz + 1)(z_{v1}s + z_{vv0})}{s^4 + p_3 s^3 + p_2 s^2 + p_1 s^1 + p_o} \tag{3.80}$$

Where $K_{vvv} = \frac{R}{L_1 L_2 C_1 C_2 (R + r_{C_2})}, z = r_{C_2} C_2, z_1 = -r_{eq} C_1, z_o = DD'$

Also,

$$p_3 = \frac{r_{eq} + r_{L_1} + D' r_{C_1}}{L_1} + \frac{1}{L_2}\left(r_{eq} + r_{L_2} + D r_{C_1} + \frac{r_{C_2} R_o}{R_o + r_{C_2}}\right) + \frac{1}{C_2}\left(\frac{1}{R_{oo} + r_{C_2}}\right)$$

$$p_2 = \frac{D'^2}{L_1 C_1} + \frac{(r_{eq} + r_{L_1} + D' r_{C_1})}{L_1 C_2 (R_o + r_{C_2})} + \frac{D^2}{L_2 C_1} + \frac{(R + r_{eq} + r_{L_2} + D r_{C_1})}{L_2 C_2 (R + r_{C_2})}$$

$$p_1 = \frac{(r_{eq} + r_{L_1} + D' r_{C_1})(R_{oo} + r_{L_2} + D r_{C_1}) + r_{eq} r_{L_1} + D' r_{C_1}}{L_1 L_2 C_2 (R_o + r_{C_2})} + \frac{D^2 L_1 + D'^2 L_2}{L_1 L_2 C_1 C_2 (R_o + r_{C_2})}$$

$$p_0 = \frac{D'^2 R_o + D^2 r_{L_1} + D'^2 r_{L_2} + DD' r_{C_1} + r_{eq}}{L_1 L_2 C_2 (R_o + r_{C_2})}$$

2. **Load current to output voltage transfer function:** The load current to output voltage transfer function is essential for understanding the dynamics of power converters as it helps to predict how variations in the load, which can occur due to changes in the connected devices or the system demand, will affect the stability and regulation of the output voltage. By analysing this transfer function, engineers can design control systems to maintain a stable output voltage despite fluctuations in load current, ensuring the reliable operation of electronic devices and systems that rely on consistent power delivery.

$$\frac{\hat{v}_o(s)}{\hat{\imath}_z(s)} = G_{vz}(s) = C(sI - A)^{-1}[B]_{second\ coloumn} \tag{3.81}$$

$$G_{vz}(s) = \frac{K_{vz}(sz + 1)(z_{z3}s^3 + z_{z2}s^2 + z_{z1}s + z_{z0})}{s^4 + p_3 s^3 + p_2 s^2 + p_1 s^1 + p_o} \tag{3.82}$$

Where, $K_{vz} = -\frac{R}{L_1 L_2 C_1 C_2 (R + r_{C_2})}, z = r_{C_2} C_2, z_{z3} = L_1 L_2 C_2$

$$z_{z2} = L_1 C_1 (r_{eq} + r_{L_2} + D r_{C_1}) + L_2 C_1 (r_{eq} + r_{L_1} + D' r_{C_1}),$$

$$z_{z1} = D^2 L_1 + D'^2 L_2 + C_1 (r_{eq} + r_{L}^{1} + D' r_{C} (r_{L}^{1} + r_{L}^{2}) + D' r_{C}^{1})$$

$$z_{z0} = D^2 r_{L_1} + D'^2 r_{L}^{2} + D D' r_{C}^{1} + r_{eq}$$

3. **Control to output transfer Function:** The transfer function relating duty cycle to output voltage primarily illustrates how changes in the duty cycle influence the output voltage under conditions where disturbances in input voltage and output current are considered.

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_{vd}(s) = E(sI - A)^{-1}[(A_1 - A_2)\mathrm{X}(s) + (B_1 - B_2)U(s)] + [(E_1 - E_2)\mathrm{X} + (F_1 - F_2)U] \quad (3.83)$$

$$G_{vd}(s) = \frac{K_{vd}(zs + 1)^2 (z_{d2} s^2 + z_{d1} s + z_{d0})}{s^4 + p_3 s^3 + p_2 s^2 + p_1 s^1 + p_o} \quad (3.84)$$

Where

$$K_{vd} = -\frac{R}{L_1 L_2 C_1 C_2 (R + r_{C_2})}, z = r_{C_2} C_2$$

$$z_{d1} = (r_{L_1} + D r_{C_1}) C_1 - L_1 I_{L_1} - (r_{L_1} + D r_{C_1}) C_1 + \left(\frac{R_{ds}}{D'^2} - \frac{r_{L_1} r_{eq}}{D'^2}\right) C_1 I_{L_2}$$

$$z_{d2} = L_1 C_1 (V_{C_1} - I_{L_2} r_{C_1} + \frac{R_{ds} - R_D}{D'})$$

$$z_{d0} = D' V_{C_1} - \left(\frac{D}{D'} r_{L_1} + D r_{C_1} + \frac{R_{ds}}{D'}\right) I_{L_2}$$

3.3 Comparison of ideal and Non-ideal Cuk Converter Models

3.3.1 Steady state model

Comparing the steady-state models of ideal and non-ideal Cuk converters reveals

significant differences in their performance outcomes. In the ideal model, assumptions

lead to simplified calculations and predictions that may fall short of real-life complexities. Conversely, the non-ideal model incorporates practical imperfections, such as component losses and nonlinearities, offering a more accurate reflection of actual performance. This comparison underscores the importance of considering non-ideal factors in the design and analysis of Cuk converters, ensuring more reliable and efficient energy conversion in practical applications.

Table 3.1 Steady state parameters for Ideal Cuk converter

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1	0.384µH
Inductance L_2	0.768µH
Decoupling Capacitor,C_1	38.58µF
Filter Capacitor, C_2	2µF
Switching Frequency, f_{sss}	50kHz
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\%I_{L_1}$/ $10\%I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\%V_{c_1}$/1% V_{c_2}

Table 3.2 Steady state parameters for Non-Ideal Cuk converter

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1/r_{L_1}	0.384µH /0.1 Ω
Inductance L_2/r_{L_2}	0.768µH/0.1 Ω
Decoupling Capacitor,C_1/r_{C_1}	38.58µF/1 µΩ
Filter Capacitor, C_2/r_{C_2}	2µF/1 µΩ
Switching Frequency, f_{sss}	50kHz
Diode Resistance,R_D	0.1Ω
MOSFET Resistance, R_{ds}	0.25Ω
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\%I_{L_1}$/ $10\%I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\%V_{c_1}$/1% V_{c_2}

In the steady-state analysis for both the ideal and non-ideal Cuk converters, as described in chapter 2. Upon substituting these values, the steady-state parameters for the Cuk converter are detailed in Table 3.3. The findings highlight lower steady-state currents and voltages in the non-ideal model compared to the ideal one due to power losses in non-ideal elements—a topic thoroughly examined in the preceding chapter

Table 3.3 Comparison between steady state values of Ideal and Non- Ideal Cuk Converter

Steady state parameters	Ideal Case	Non -ideal Case
Inductor current, i_{L_1}	8.33 A	7 A
Inductor current i_{L_2}	4.166 A	3.473 A
Capacitor voltage V_{C_1}	72 V	63.58 V
Output voltage V_{C_2}	48 V	39.96 V
Dc voltage gain factor $\frac{V_o}{V_s}$	2	1.665

3.3.2 Small Signal Model

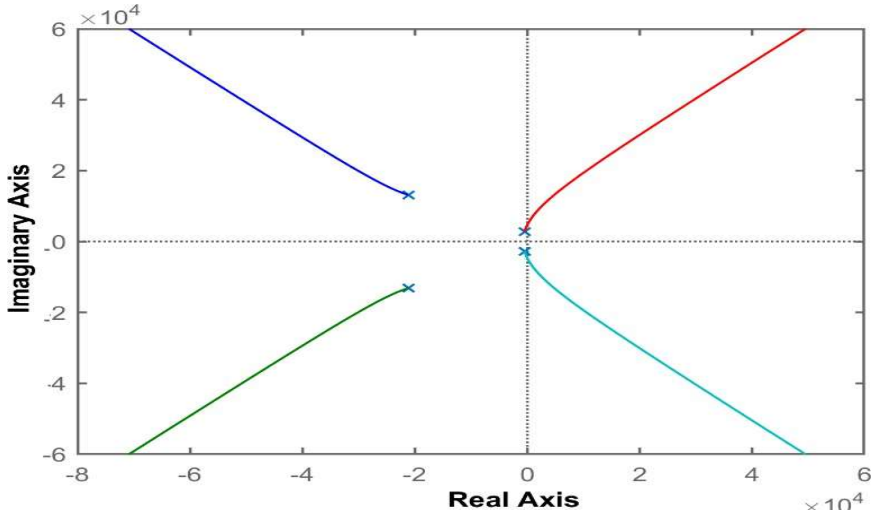
3.3.2.1 Line to Output transfer function

We obtain by entering the converter parameter values in Eqn. (3.52) and Eqn. (3.80), respectively,

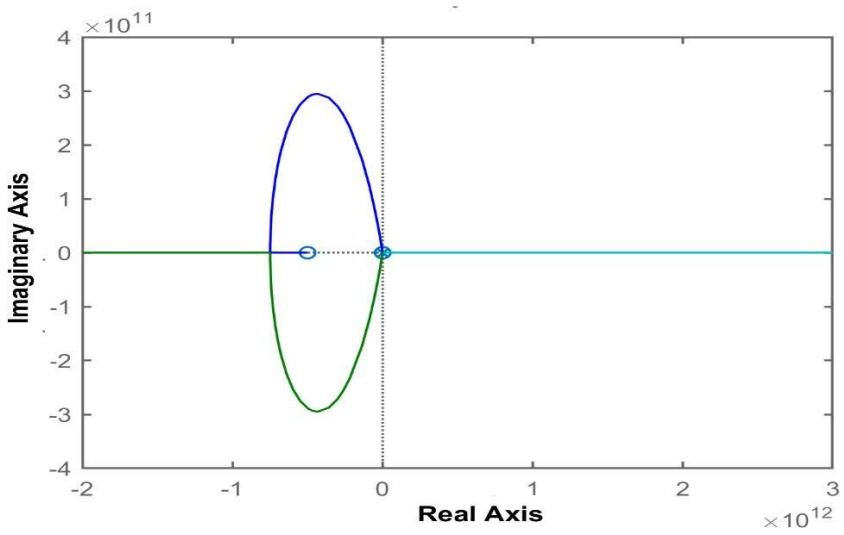
$$G_{vv,ideal} = \frac{9.7754 \times 10^{15}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \quad (3.85)$$

$$G_{vv,nonideal} = \frac{-0.6778\, s^2 - 3.389 \times 10^{11}\, s + 9.775 \times 10^{15}}{s^4 + 4.457 \times 10^4\, s^3 + 7.246 \times 10^8\, s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (3.86)$$

The ideal Cuk converter is characterised by the presence of four complex conjugate poles, specifically located at $(-2.1185 \pm 1.3156i) \times 10^4$ and $(-0.0517 \pm 0.2760i) \times 10^4$, while having no zero. On the other hand, the non-ideal Cuk converter is characterised by four complex conjugate poles located at $(-2.1411 \pm 1.3488i) \times 10^4$ and $(-0.0876 \pm 0.2900i) \times 10^4$, as well as two real zeros positioned at -5×10^{11} and 0 .



(a)



(b)

Fig 3.3 Root locus plot of Line to output transfer function (a) Ideal (b) Non-Ideal

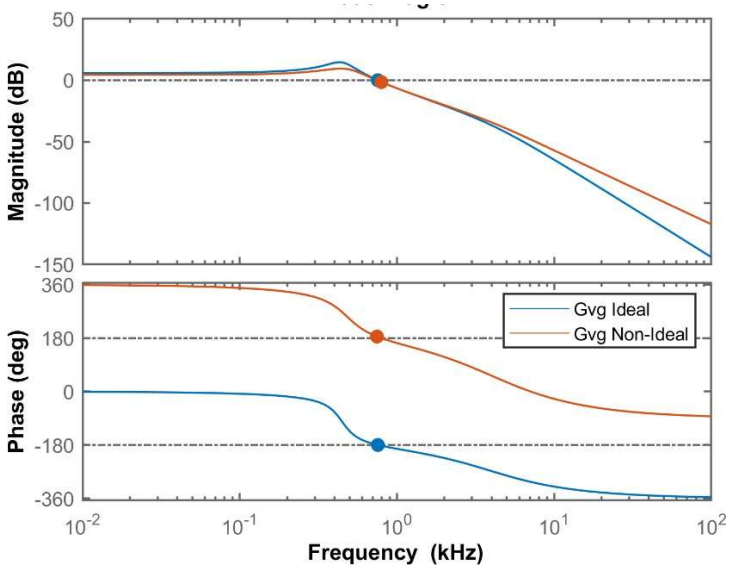


Fig 3.4 Frequency response of Ideal and Non ideal line to output transfer function

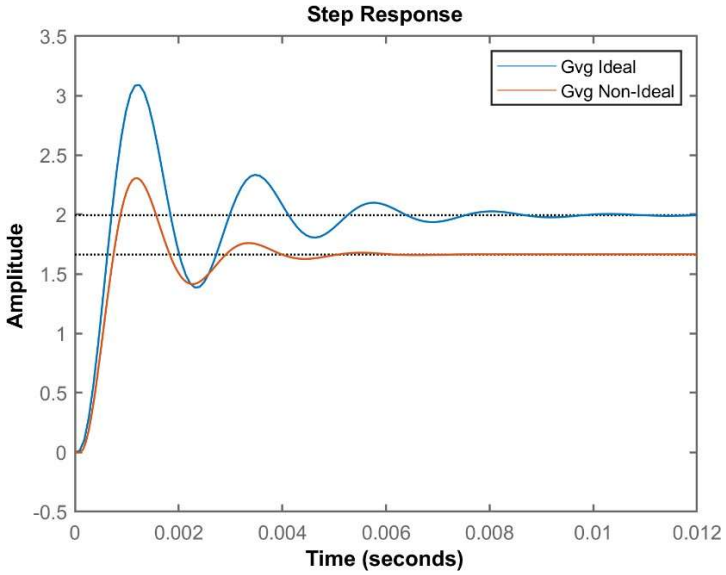


Fig 3.5 Step response comparison of Ideal and Non ideal line to output transfer function

In evaluating the performance of ideal versus non-ideal Cuk converters, the distinctions in their behaviour become evident through the analysis of both Bode and step responses, particularly concerning the input voltage to output voltage transfer function. For the ideal Cuk converter, the analysis points to a gain margin recorded at -0.206dB at a frequency of 0.755kHz, accompanied by a phase margin of -0.0562

degrees at 0.756kHz. These parameters suggest a certain level of stability and frequency response under ideal conditions.

Transitioning to the non-ideal Cuk converter, the gain and phase margins undergo notable shifts. The gain margin tightens to 1.49dB at a frequency of 0.795kHz, while the phase margin increases to 5.41 degrees, observed at a significantly elevated frequency of 0.747kHz. This adjustment in margins highlights the impact of real-world imperfections on the converter's performance metrics, emphasizing a more delicate balance between gain and phase in the presence of non-ideal elements.

An additional layer of comparison is offered through the step response analysis. Here, the non-ideal Cuk converter demonstrates a less oscillatory behavior compared to its ideal counterpart. This characteristic indicates a potential enhancement in operational stability for the non-ideal converter, especially in scenarios of varying load conditions. The dampened oscillatory response suggests that despite the losses and non-idealities present, the system may be more adept at handling abrupt changes in input or load, ultimately contributing to a smoother transition and potentially more reliable performance over time.

3.3.2.2 Line to output transfer function

We obtain by substituting the values of various parameters in (3.56) and (3.84) accordingly,

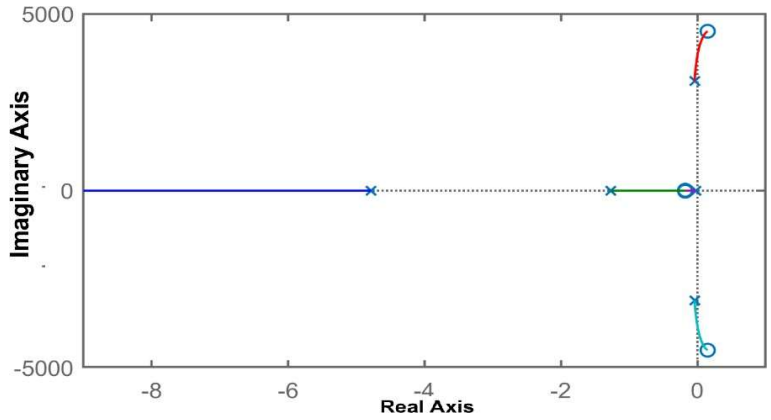
$$G_{vd,ideal} = \frac{4.688 \times 10^{10}\, s^2 - 1.404 \times 10^{14}\, s + 1.057 \times 10^{18}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \quad (3.87)$$

$$G_{vd,non\text{-}ideal} = \frac{0.08074\, s^3 + 4.037 \times 10^{10}\, s^2 - 1.072 \times 10^{14}\, s + 7.875 \times 10^{17}}{s^4 + 4.457 \times 10^4\, s^3 + 7.246 \times 10^8\, s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (3.88)$$

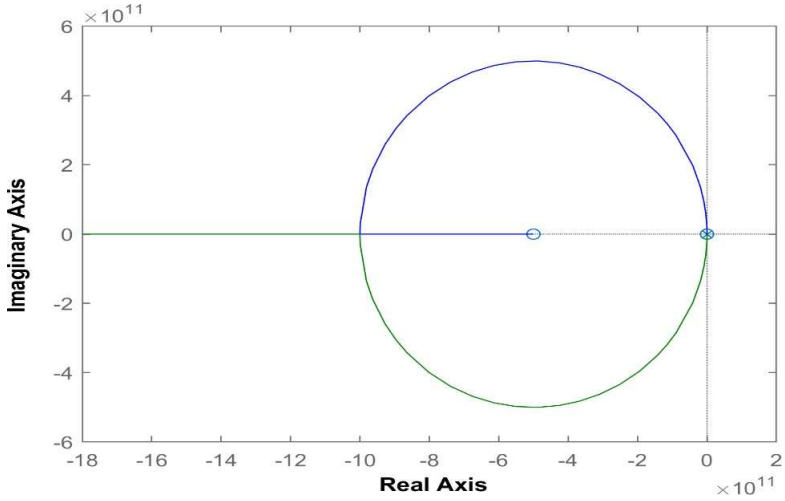
The ideal and non-ideal Cuk converters exhibit different characteristics in their duty cycle to output voltage transfer functions, as seen through their poles and zeroes. The ideal Cuk converter has four complex conjugate poles situated at $(-2.1185 \pm 1.3156ii) \times 10^4$ and $(-0.0517 \pm 0.2760ii) \times 10^4$, and two right half-plane zeros at $(1.4980 \pm 4.5057ii) \times 10^3$. This configuration signifies a non-minimum phase system, indicating an initial response in the output voltage that may be contrary to the

input's intended effect .

Contrastingly, the non-ideal Cuk converter's transfer function reveals a minimum phase system, with four complex conjugate poles at $(-2.1411 \pm 1.3488ii) \times 10^4$ *and* $(-0.0876 \pm 0.2900ii) \times 10^4$, alongside three zeros located at $(-5.0000 + 0.0000ii) \times 10^{11}$ *and* $(0.0000 \pm 0.0000ii)$. The absence of right half-plane zeros implies a more intuitive, direct relationship between input changes and output responses. This differentiation between the ideal and non-ideal systems underscores the practical considerations required in designing and controlling Cuk converters effectively.



(a)



(b)

Fig 3.6 Root locus plot of Line to output transfer function (a) Ideal (b) Non-Ideal

In comparing the ideal and non-ideal Cuk converters concerning their duty cycle to output voltage transfer function, significant differences are noted in their Bode and

step responses. The ideal Cuk converter displays a gain margin of -48.6dB at 0.517kHz, coupled with a phase margin of 12.3 degrees at 3.44kHz. This configuration suggests a certain level of stability but indicates potential challenges in maintaining control over a wide frequency range.

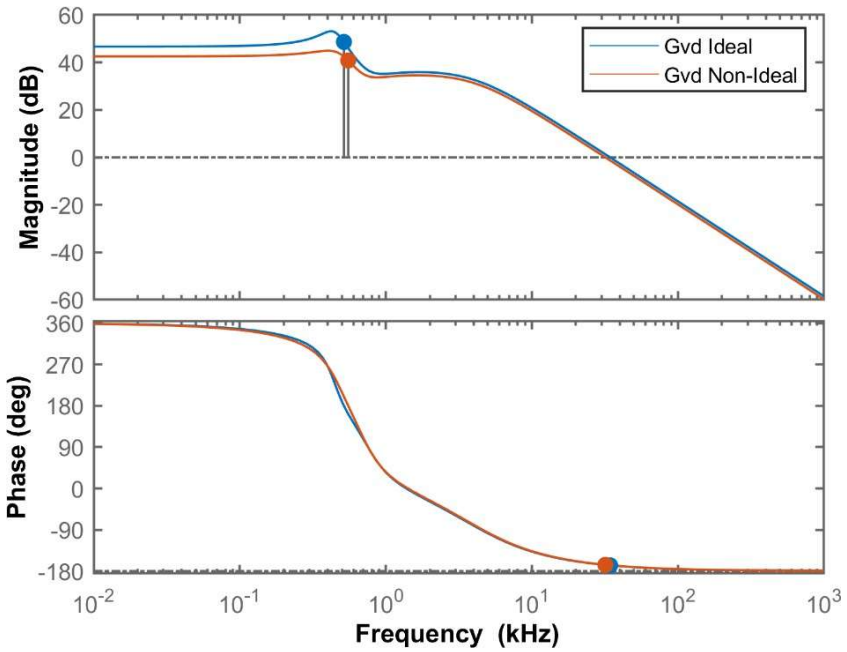


Fig 3.7 Frequency response comparison of $G_{vd}(s)$ for ideal and non ideal case

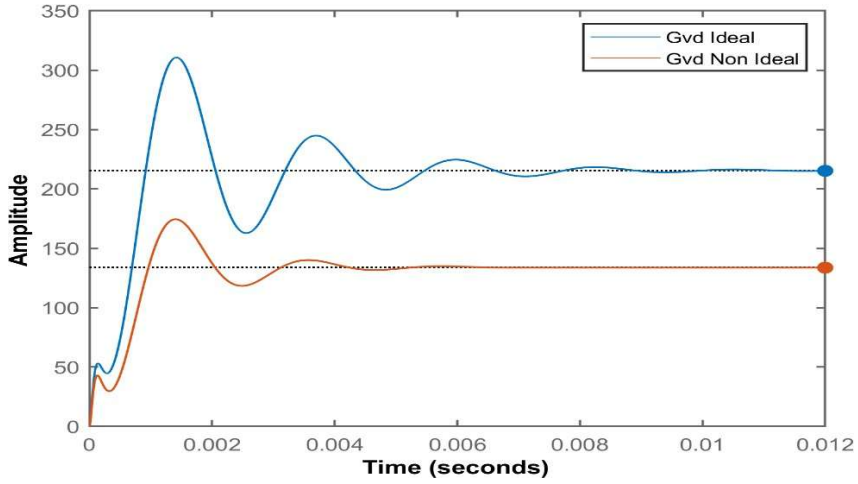


Fig 3.8 Comparison of step responses of $G_{vd}(s)$ for ideal and non-ideal case

On the other hand, the non-ideal Cuk converter exhibits a much-improved gain margin of -4.08dB at 0.553kHz and a phase margin of 13.5 degrees at a substantially higher

frequency of 31.9kHz. This enhancement in the phase margin, despite a close gain margin value, implies a slightly increased robustness against oscillations and a better overall response to changes.

Crucially, the examination of the open-loop step response reveals that the parasitic resistances present in the non-ideal converter play a pivotal role in dampening the system. This dampening effect leads to an improved transient response, showcasing a more stable behavior under dynamic conditions compared to the ideal converter. The incorporation of parasitic elements, often deemed detrimental under many circumstances, thus proves advantageous in this context by providing natural damping that aids in steadying the converter's performance during rapid changes

3.3.2.3 Load current to output voltage transfer function

We obtain by substituting the corresponding parameter values in (3.274) and (3.265), respectively,

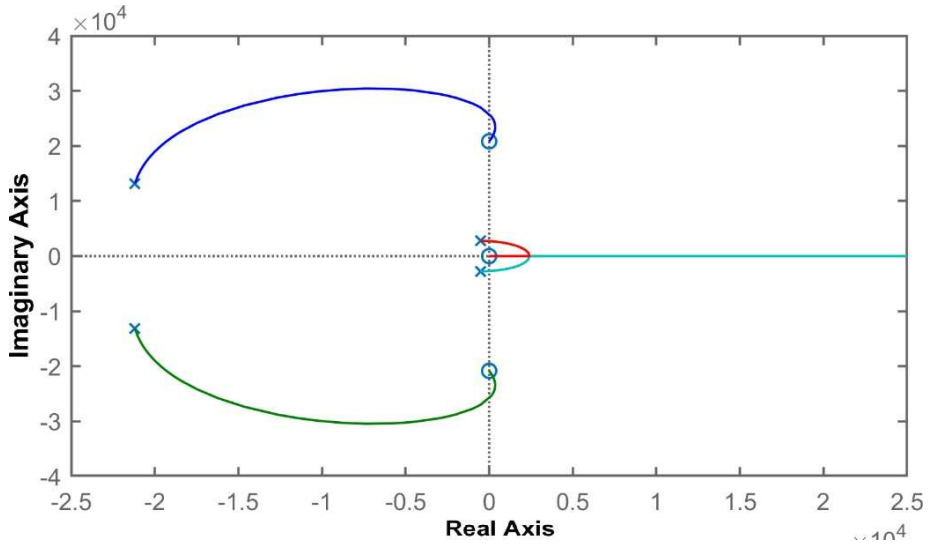
$$G_{iiz,iideal} = \frac{-2.592 \times 10^4\, s^3 - 1.125 \times 10^{13}\, s}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \quad (3.89)$$

$$G_{iiz,noniideal} = \frac{-0.1089\, s^4 - 2392\, s^3 - 8.163 \times 10^5\, s^2 - 1.225 \times 10^9 s - 2.029 \times 10^{11}}{s^4 + 584.5\, s^3 + 1.8 \times 10^6\, s^2 + 2.897 \times 10^8\, s + 1.372 \times 10^8} \quad (3.90)$$

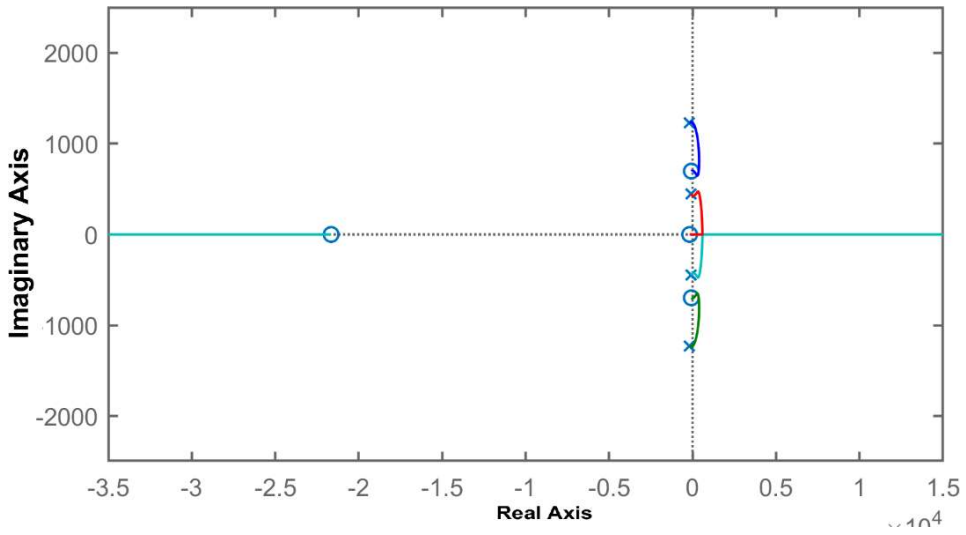
In examining the load current to output voltage transfer functions of both ideal and non-ideal Cuk converters, distinct characteristics emerge through their poles and zeros. The ideal Cuk converter features four complex conjugate poles at($-2.1185 \pm 1.3156ii) \times 10^4\ and\ (-0.0517 \pm 0.2760ii) \times 10^4$, accompanied by three zeros located at $0\ and \pm 2.0833ii \times 10^4$. This configuration underscores a dynamic response influenced by both the oscillatory nature of the poles and the initial system response directed by these zeros .

Meanwhile, the non-ideal Cuk converter presents a slightly different landscape with its four complex conjugate poles positioned at $(-2.1090 + 1.3365ii) \times 10^4\ and -0.2394$, *and at oriigiin* alongside four zeros, one of which is real at -2.16x10^4, and the others being -175.07 and a complex conjugate pair at $-73.77 \pm 697.75ii$. This arrangement indicates a comprehensive response heavily shaped by the non-idealities such as component tolerances and losses, which contribute to a more intricate output

behavior in response to load current variations. These differences between ideal and non-ideal models highlight the importance of considering real-world factors in the design and operational strategies of Cuk converters.



(a)



(b)

Fig 3.9 Root locus plot for $G_{vz}(s)$ for ideal and non-ideal case

When analysing and comparing the Bode and step responses related to the load current to output voltage transfer function of ideal and non-ideal Cuk converters, several key differences emerge.

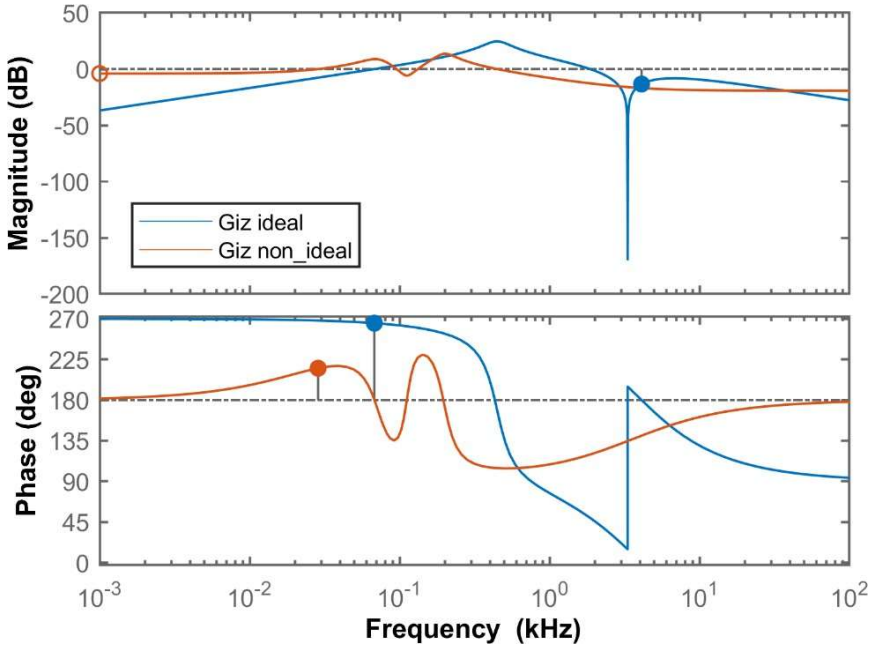


Fig 3.10 Comparison of Bode plots of $G_{vz}(s)$ for ideal and non-ideal case

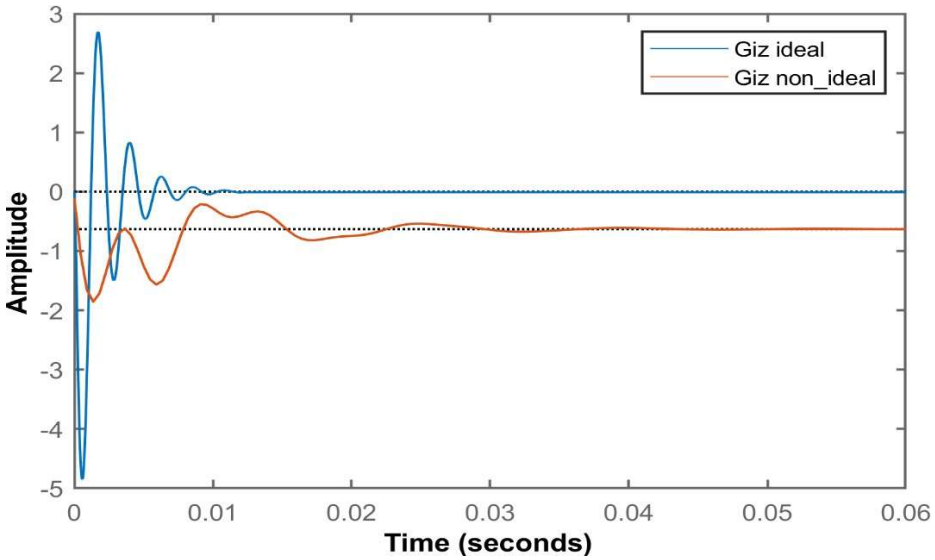


Fig 3.11 Comparison of step responses of $G_{vz}(s)$for ideal and non-ideal case

In the ideal Cuk converter scenario, the gain margin is presented as 13.3dB at a frequency of 4.11kHz, while the phase margin is notably high at 85 degrees, observed at a lower frequency of 0.0679kHz. These values suggest a robust system with significant stability margins, capable of dealing with a wide range of operational conditions without risk of instability. The high phase margin, in particular, indicates a system that is highly resistant to overshooting and capable of settling into its steady state quickly after disturbances.

3.4 Conclusions

In conclusion, the application of the state space averaging technique in modelling both ideal and non-ideal Cuk converters has yielded significant advancements in understanding their behaviour. This method facilitated the development of an enhanced model for the non-ideal Cuk converter, offering greater accuracy in steady-state and transient analysis. By examining the transfer functions related to input voltage to output voltage and load current to output voltage, along with carrying out frequency analysis for each, a comprehensive understanding of these converters' dynamics was achieved.

One of the pivotal findings is the distinction between the ideal and non-ideal Cuk converters concerning the phase system of their duty cycle to output voltage transfer functions. Under ideal assumptions, the system exhibits non-minimum phase behaviour. However, by incorporating non-ideal elements, the system can transition to a minimum phase system, though this is subject to the specific non-ideal elements and their values. Therefore, the non-minimum phase property is not intrinsic but conditional upon the modelling parameters, which highlights the critical role of accurate modelling in predictive analysis and control strategy development.

Furthermore, comparing the step responses of both ideal and non-ideal converters for each transfer function emphasized the practical implications of these findings. The refined transfer functions obtained are instrumental for controller design, offering insights that ensure the robust performance and reliability of Cuk converters in real-world applications. Thus, adopting state space averaging for modelling illuminates the nuances of converter behaviours, bridging the gap between theoretical assumption and practical application, which is invaluable for advancing power electronics design and analysis.

CHAPTER 4
CONTROL OF DC-DC CONVERTERS

4.1 Introduction

The effectiveness of DC-DC converters is crucial in modern power electronics, supporting a wide range of applications from mobile devices to advanced automotive systems. Implementing robust control systems is crucial for maximizing the performance of these converters. These systems are responsible for maintaining consistent output, ensuring high-quality responses, and being able to handle different levels of load and input conditions. This chapter explores the essentials of closed-loop control systems for DC-DC converters, emphasizing the importance of advanced control strategies through theoretical exposition and simulation validation.

Unavoidable deviations include variations in input voltage, variations in load, and intrinsic non-linearities of the components like resistors, capacitors, and inductors make closed-loop systems necessary. Potential instability and inefficiencies may result from these changes having a big effect on the converters' performance. Effectively correcting for these variations and ensuring stable operation is a closed-loop control that continuously modifies the output to meet the given reference value.

Stability, accuracy, responsiveness, and efficiency are among the main criteria that a control system for DC-DC converters should satisfy in its design. Irrespective variations in input or load, the control system ought to stabilise the voltage or current output. Reactivity is the speed at which the control system fixes any deviations; accuracy is the ability to reach and maintain the set output value. Operational effectiveness without unduly high expenses or complexity should likewise be the goal of the control design.

Several control methodologies are utilized to address the distinct challenges presented by various DC-DC converter applications. One approach to control is voltage mode control, which adjusts the duty cycle solely based on the output voltage. This method provides a simpler and more straightforward way of adjusting the duty cycle. Additionally, current mode control effectively monitors and regulates both the output

current and voltage, resulting in a more rapid response to load changes and enhancing the converter's transient response. This control method combines voltage and current mode controls to create a more reliable solution that is essential for applications requiring high precision and stability. It offers comprehensive monitoring and faster corrective actions, ensuring optimal performance.

The wide range of applications and strong performance features of PID (Proportional-Integral-Derivative) and PI (Proportional-Integral) controllers make them widely used in industrial environments. These controllers quickly settle transients and efficiently temper overshoots. Easy application with adjustable parameters to suit particular application requirements is made possible by the straightforward mathematical formulations.

Frequency domain measurements including bandwidth (or gain crossover frequency, GCF) and phase margin (PM) are also often used to assess the robustness and performance of DC-DC converters. These measurements are important since they show how the converter will react to external disturbances and in dynamic situations. Therefore, it is suggested that developing controllers with these frequency domain measures in mind frequently leads to improved dynamic performance and system stability.

There are special difficulties in the details of managing ideal versus non-ideal Cuk converters. Because capacitors and inductors have Equivalent Series Resistance (ESR), which adds more dynamics that a controller must control, non-ideal converters show inefficiencies. Among these are output ripple and response time variations, which are less of a problem in ideal converters without these non-ideal features. Realistic applications need control systems that take these non-ideal components into account.

Significant modelling experiments have shown the effectiveness of closed-loop controls in both ideal and non-ideal Cuk converters. These investigations confirm that different control techniques work well to manage normal deviations and enhance performance in a range of operational environments. Therefore, the application of advanced control techniques in DC-DC converters guarantees the operational dependability and improves the effectiveness of these essential components in contemporary electronic systems.

PULSE WIDTH MODULATOR

An essential feature of power electronics, especially in the functioning of DC-DC converters, is a pulse width modulator (PWM). Controlling power supplied to a load without appreciable energy loss is the fundamental purpose of PWM. In a pulse train, this is accomplished by varying the pulse width, which regulates the average power applied to the load. The process is the interaction of a sawtooth waveform $V_{sss}(t)$with a control signal $V_c(t)$.

Controller made especially for the DC-DC converter produces the control signal V_c (t). Depending on the output needs of the converter, such the intended voltage or current level, this controller modifies the control signal. The control signal next becomes an input to the PWM.

Within the PWM (Pulse Width Modulation) system, the control signal is subjected to a comparison with a sawtooth waveform using a comparator. The sawtooth waveform is defined by its constant switching frequency (ƒs) and its peak-to-peak amplitude (V_{sss}). Crucially, the frequency of this waveform is coordinated with the switching frequency of the converter, guaranteeing optimal and efficient operation of the converter.

$$d(t) = \frac{V_c(t)}{V_{sss}} \tag{4.1}$$

Hence, we get the mathematical model of the pulse width modulator as:

$$\frac{d(t)}{V_c(t)} = \frac{1}{V_{sss}} \tag{4.2}$$

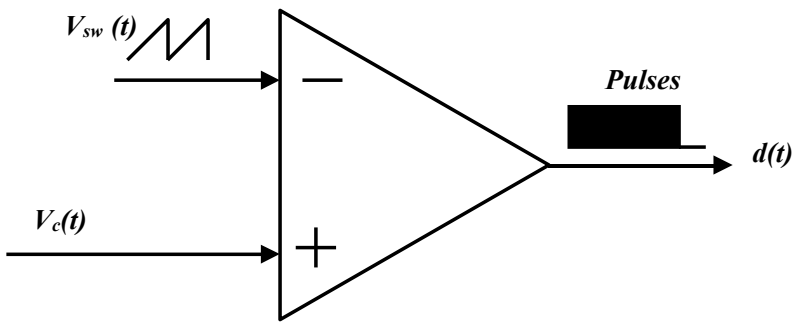


Fig 4.1 Pulse width modulator circuit

The functionality of the PWM relies on this comparison. When the control signal surpasses the sawtooth waveform in magnitude, the output of the comparator switches to a high state. On the other hand, if the magnitude of the sawtooth is increased, the output of the comparator will stay low. This adjustment leads to the creation of a pulse train, with each pulse's width being determined by the control signal's magnitude in relation to the sawtooth waveform.

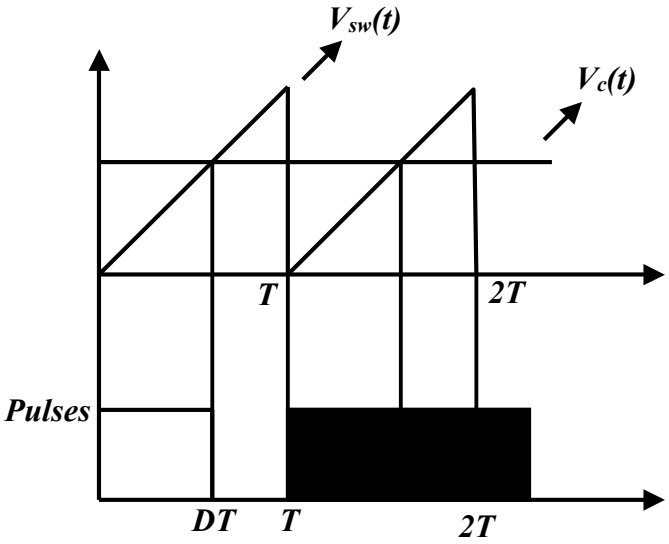


Fig 4.2 Waveforms of Pulse Width Modulator

4.2 Control of DC-DC Cuk Converter

The effective functioning of both ideal and non-ideal Cuk converters relies on the adoption of efficient control methods. Three primary control systems, namely Proportional-Integral (PI) control, Proportional-Integral-Derivative (PID) control, and Dual Loop control, are utilized to meet specific performance needs and rectify any inherent inefficiencies. These control systems can be divided into Voltage Mode Control and Current Mode Control, each of which emphasizes different aspects of the converter's performance.

4.2.1 PI CONTROLLER DESIGN FOR IDEAL CUK CONVERTER

In power electronics, efficient voltage and current control depends critically on the Proportional-Integral (PI) controller design for a perfect Cuk converter. Renowned for

its ability to keep an output steady over a wide variety of inputs, the Cuk converter needs exact management to maintain both stability and efficiency. Presenting the PI controller, which modifies the duty cycle of the converter according to the difference between the intended and actual outputs. This dynamic adjustment guarantees that, in spite of changes in load or input voltage, the output voltage and current closely follow preset values.

Table 4.1 Controller Design parameters for an Ideal Cuk Converter

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1	0.384µH
Inductance L_2	0.768µH
Decoupling Capacitor,C_1	38.58µF
Filter Capacitor, C_2	2µF
Switching Frequency, f_{sss}	50kHz
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\% I_{L_1}$/ $10\% I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\% V_{c_1}/1\%\ V_{c_2}$

Optimizing the performance of the PI controller requires a thorough analysis of the gain and phase margin. Here is where the Ziegler-Nicholas method becomes useful, providing a systematic approach for determining the optimal proportional and integral gain values. Through deliberate manipulation of a controlled oscillation and careful analysis of the converter's response, one can determine the essential parameters for setting the PI controller gains. This guarantees a harmonious combination of swift response time and minimal overshoot.

4.2.1.1 VOLTAGE MODE CONTROL

A typical method for controlling the output voltage in an ideal Cuk converter is voltage mode control, which is independent of variations in input voltage or load conditions. Through modification of the duty cycle—the ratio of the on-time to the entire switching period of the converter's switch—this control technique aims to maintain a preset voltage level. Measurement of the output voltage and comparison with a reference voltage are the fundamental concepts. When these values diverge, an error signal is produced that a controller—a Proportional-Integral (PI) controller—processes to modify the duty cycle as shown in Fig.4.3

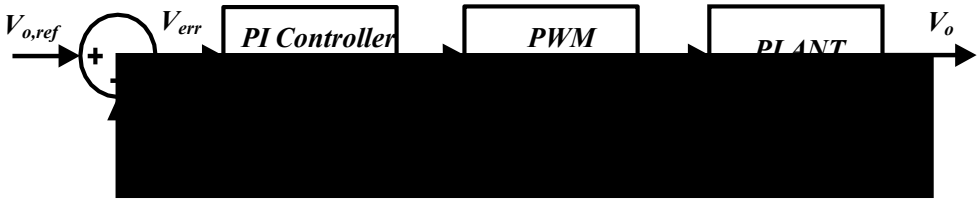


Fig 4.3 Voltage mode control algo using PI controller

The duty cycle to output voltage transfer functions of DC-DC Converter and PWM Modulation are:

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.3}$$

$$G_{PWM} = \frac{1}{V_{sss}} \tag{4.4}$$

In this chapter, sawtooth peak voltage $V_{sss} = 1$ is taken,

The loop transfer function of an uncompensated system will thus be

$$T(s) = G_{PWM}(s) G_{vd}(s) = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.5}$$

Now, a PI controller whose transfer function is designed to enhance this converter's phase margin and steady-state performance is

$$G_c(s) = \left(k_p + \frac{k_{ii}}{s}\right) \tag{4.6}$$

The parameters of the Cuk converter under study are listed in Table 4.1. They are the same as those applied to its modelling in chapter 3.

Section (3.254) of the earlier chapter has the duty-cycle to output-voltage transfer function derived. By replacing V_s =16 V and R_o = 11Ω together with other Cuk converter values, we obtain

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{4.688 \times 10^{10}\, s^2 - 1.404 \times 10^{14}\, s + 1.057 \times 10^{18}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \tag{4.7}$$

The uncompensated loop transfer function of Cuk converter will be

$$T(s) = G_{PWM}(s)G_{vd}(s) = \frac{1}{V_{sss}} G_{vd}(s) \tag{4.8}$$

$$T(s) = \frac{4.688 \times 10^{10}\, s^2 - 1.404 \times 10^{14}\, s + 1.057 \times 10^{18}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \tag{4.9}$$

When analysing the behaviour of an uncompensated Cuk converter, as shown in Fig,4.4 we can identify a few important points in its frequency response. First, the converter demonstrates an poor gain margin, and secondly, it boasts a phase margin of 12.3° at a gain crossover frequency of 34.4 kHz. This relatively low phase margin indicates a compromised transient response, which is characterized by significant overshooting. In addition, the constant gain seen at lower frequencies suggests that the system will experience a steady-state error when confronted with unexpected disruptions. This behaviour is characteristic of a type-0 system, which, when uncompensated, is not well-suited to efficiently handle step disturbances.

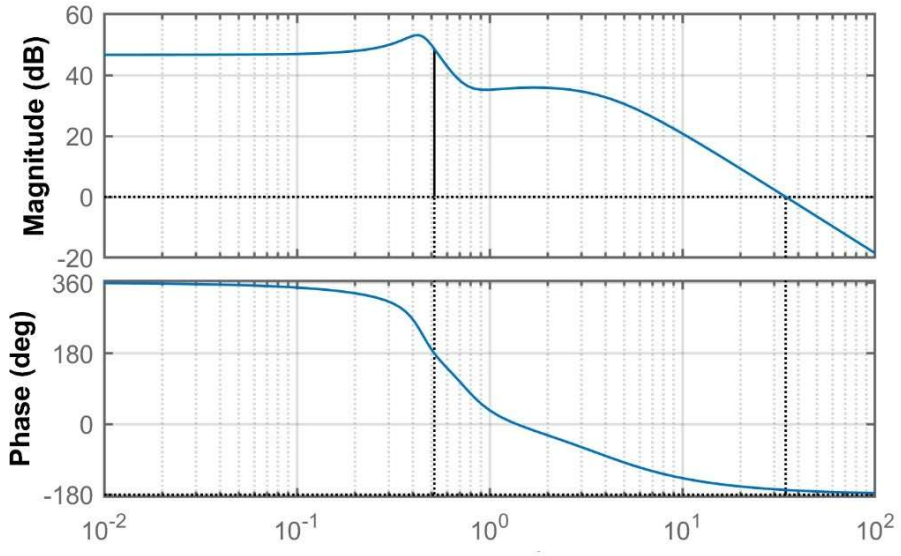


Fig 4.4 Bode plot of Uncompensated Transfer function

Two strategic changes are suggested in order to address these problems and improve the performance of the system. First, lowering the gain crossover frequency would help to advance the phase margin and, thus, enhance the system's transient response. The second suggestion is to add a single pole at the origin, which will help the system better react to step disturbances and hence address the problem of steady-state inaccuracy.

These improvements are put into practice by means of a Proportional-Integral (PI) controller. Finding the crossover frequencies is possible with frequency response techniques like Bode plot analysis if the transfer function is known. The phase margins and gain satisfies the stability and responsiveness requirements at these frequencies. The phase and gain margins of the converter are then shaped by adjusting the gain $K_p$and integral time K_{ii} of the PI controller. Through this tuning, the system is made stable and has no overshoot, allowing for a quick reaction to variations in input or load circumstances.

We select $K_p = 1.5 \times 10^{-4}\ and\ K_{ii} = 2.9711$. With these values, the PI controller transfer function is:

$$G_c(s) = 1.5 \times 10^{-4} + \frac{2.9711}{s} \tag{4.10}$$

Therefore, the loop transfer function of compensated Cuk converter is given by:

$$G_c(s)T(s) = \frac{8.789 \times 10^6\, s^3 + 1.53 \times 10^{11}\, s^2 - 2.191 \times 10^{14}\, s + 3.925 \times 10^{18}}{s^5 + 4.34 \times 10^4\, s^4 + 6.735 \times 10^8\, s^3 + 9.766 \times 10^{11}\, s^2 + 4.902 \times 10^{15}\, s} \tag{4.11}$$

Fig.4.5 illustrates the significant changes to the performance characteristics of the enhanced Cuk converter in its frequency response. For the closed-loop system, the adjustment has effectively increased the phase margin to 78.9°. This large phase margin increase implies a more stable reaction to changes by greatly reducing overshoot. But as seen by the gain crossover frequency drop to 106 Hz, this enhancement has a cost. With a slower response speed shown by this lower crossover frequency, the system may respond to changes in command or load more slowly. A noticeable modification in the system's performance at lower frequencies is also the addition of a -20 dB/decade gain slope. Because it tackles and successfully removes the steady-state error, this particular modification helps to guarantee that the Cuk converter produces consistent output throughout time even in the presence of noise.

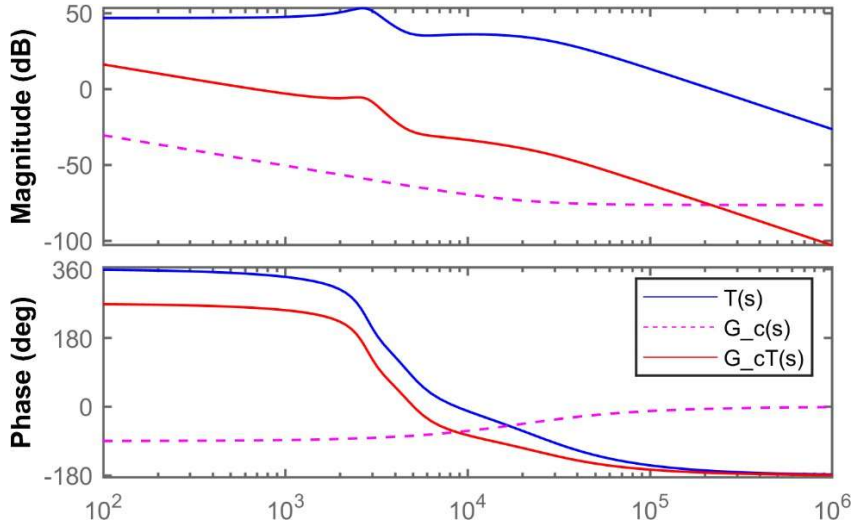


Fig 4.5 Frequency response of PI controlled DC-DC Cuk Converter

4.2.1.2 CURRENT MODE CONTROL

Current mode control integrates the regulation of the output voltage with direct control over the inductor current. To achieve optimal performance in a Cuk converter with current mode control, it is crucial to have direct control over the current that flows through the inductor. The initial step requires detecting the electrical current passing through the inductor of the converter. Current sensing is accomplished by utilizing a current sensor that is positioned in series with the inductor. The current is then compared with a reference current in a precise manner. The discrepancy between these currents represents the error signal, indicating the difference between the actual and desired current levels. This error signal is inputted into a PI controller, which is commonly used in professional settings. The controller adjusts the duty cycle of the switch within the converter based on the error as shown below:

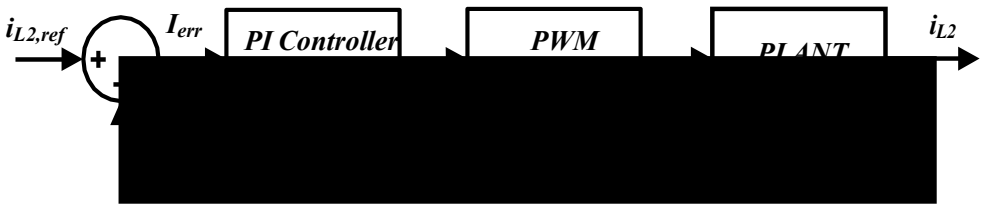


Fig 4.6 Current mode control algo using PI control

Let the duty cycle to Inductor current transfer function for the ideal Cuk converter be:

$$G_{iid}(s) = \frac{\hat{\imath}_{L_2}}{\hat{d}}$$
$$= \frac{93750\,s^3 + 3.788 \times 10^9\,s^2 - 1.008 \times 10^{13}\,s + 9.174 \times 10^{16}}{s^4 + 4.34 \times 10^4\,s^3 + 6.735 \times 10^8\,s^2 + 9.766 \times 10^{11}\,s + 4.902 \times 10^{15}} \quad (4.12)$$

The uncompensated loop transfer function of the Cuk converter is as follows:

$$T(s) = G_{PWM}(s)G_{iid}(s)$$
$$= \frac{93750\,s^3 + 3.788 \times 10^9\,s^2 - 1.008 \times 10^{13}\,s + 9.174 \times 10^{16}}{s^4 + 4.34 \times 10^4\,s^3 + 6.735 \times 10^8\,s^2 + 9.766 \times 10^{11}\,s + 4.902 \times 10^{15}} \quad (4.13)$$

Where $G_{PWM}(s) = \frac{1}{V_{sss}}$ and $V_{sss} = 1$ for this compensator design.

The phase margin of 93.2° for the uncompensated DC-DC Cuk converter is shown in Figure 4.7 at a gain crossover frequency of 15.8 kHz. A steady-state error can also arise from the converter's consistent gain in the low-frequency spectrum when a step disturbance occurs in the system. A PI (Proportional-Integral) controller is implemented to address these problems with phase margin and steady-state error in the Cuk converter. The Ziegler Nicholas method is used in the parameter tuning of this PI controller with the goal of improving the converter's dynamic response as well as its steady-state performance.

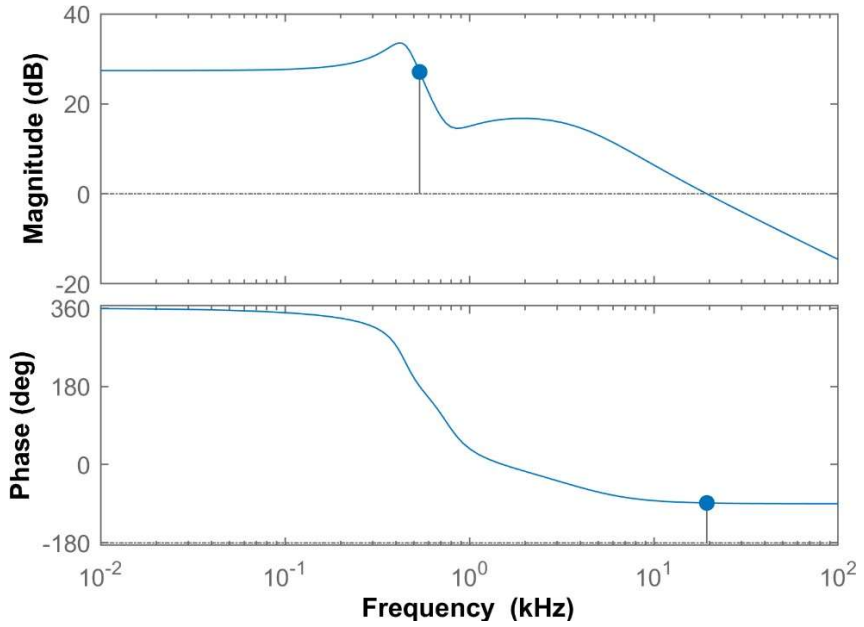


Fig 4.7 Frequency response of uncompensated Cuk Converter

The Bode plot for a PI-compensated Cuk converter, presented in Figure 4.8, demonstrates an increase in the phase margin to 79.7°, while the gain crossover

frequency drops to 107 Hz. This enhancement in phase margin is beneficial for reducing overshoots, albeit at the cost of a slower response due to the lower crossover frequency. Additionally, the gain at low frequencies now shows a slope of -20 dB/decade, a change that significantly contributes to the elimination of steady-state errors in the system.

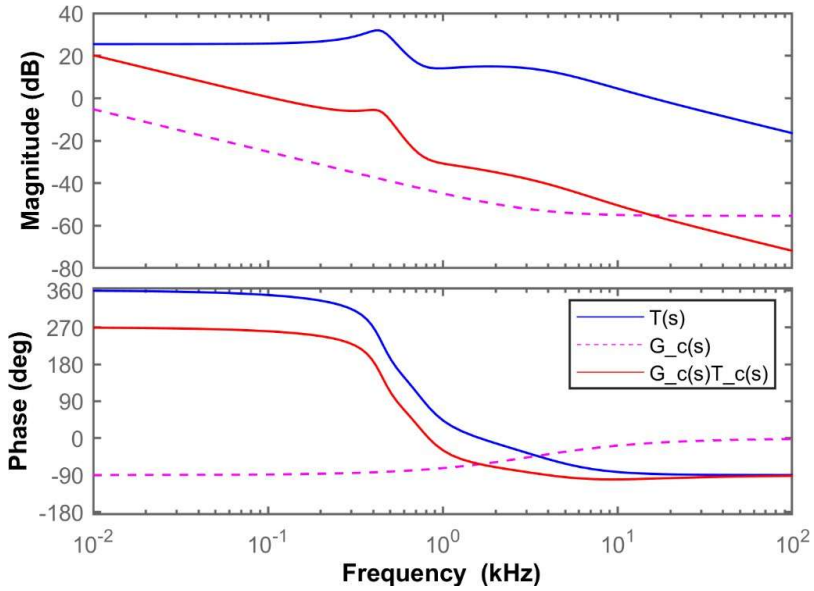


Fig 4.8 Frequency response of PI controlled DC-Dc Cuk converter

4.2.1.3 RESULTS AND DISCUSSION

To evaluate the performance of the PI controller described in (4.23), simulations were conducted on a closed-loop DC-DC Cuk converter. The parameters used for the simulations are consistent with those listed in Table 4.1. MATLAB/Simulink software was employed to obtain the simulation results. These results were then compared and analysed under three distinct conditions: (a) changes in the reference output voltage, (b) changes in input voltage, and (c) changes in load current.

4.2.1.3.1 Voltage Mode Control

4.2.1.3.1.1 Reference Voltage Variation

The performance of the PI controller designed for the Cuk converter is evaluated for a step change in the reference output voltage $V_{o,rerr}$ The input voltage V_s and load resistance $R_o$are maintained at constant values of 24V and 11.52 Ω, respectively. Simulation results, depicted in Fig. 4.9, show the response to a reference voltage

change from 14V to 30V. It is observed that, in both scenarios, the output voltage reaches the new desired value within 13.96 ms, without any overshoot or oscillations. Since the load resistance is constant at 11.52 Ω, the load current adjusts to the new output voltage, resulting in a load current of 4.166A

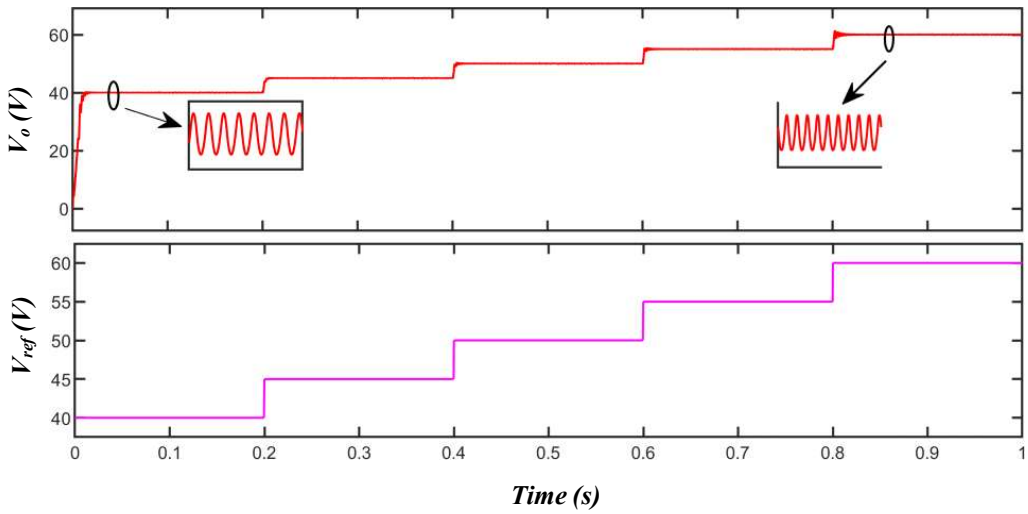


Fig 4.9 Simulation results for reference variation from 40V to 60V

4.2.1.3.1.2 Variation in Input Voltage

Results of simulation were achieved for step changes in input voltage under constant load conditions. R_o was set at 11.52 Ω and the input voltage V_s was ranged from a minimum of 14V to a maximum of 30V. The output voltage stabilises back to its steady-state value of 48V within 13 ms when the input voltage rises from 14V to 30V. Still, the output voltage undergoes notable oscillations and overshoot in the transient phase as shown in Fig.4.10

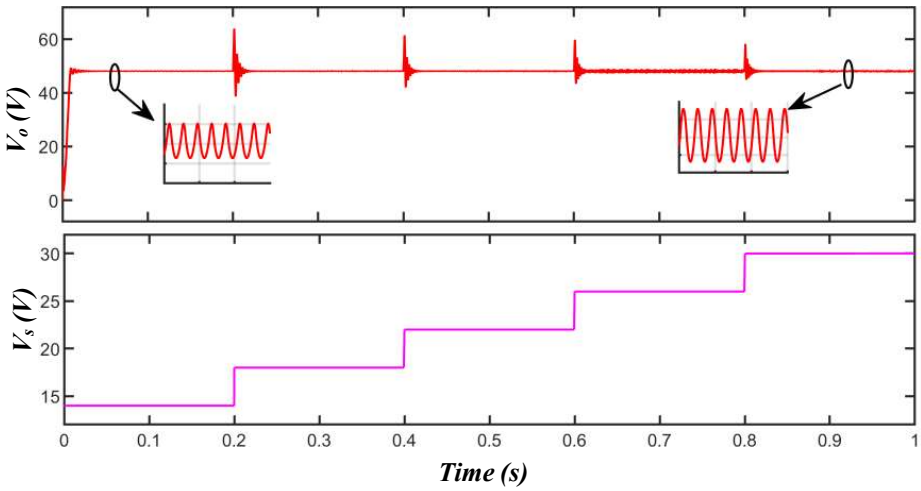


Fig 4.10 Line voltage variation from 14V to 30V

4.2.1.3.2 Variation in Load Resistance

Under changing load conditions, the closed-loop Cuk converter's performance is also investigated while maintaining constant input voltage. From 16Ω, the lowest load current of 3A, the load resistance (R) is changed to 7.5Ω, the maximum load current of 6.5A. The output voltage shows an undershoot of 4V before settling back to 48V within 13 ms when the load resistance varies from 16Ω to 7.5Ω.

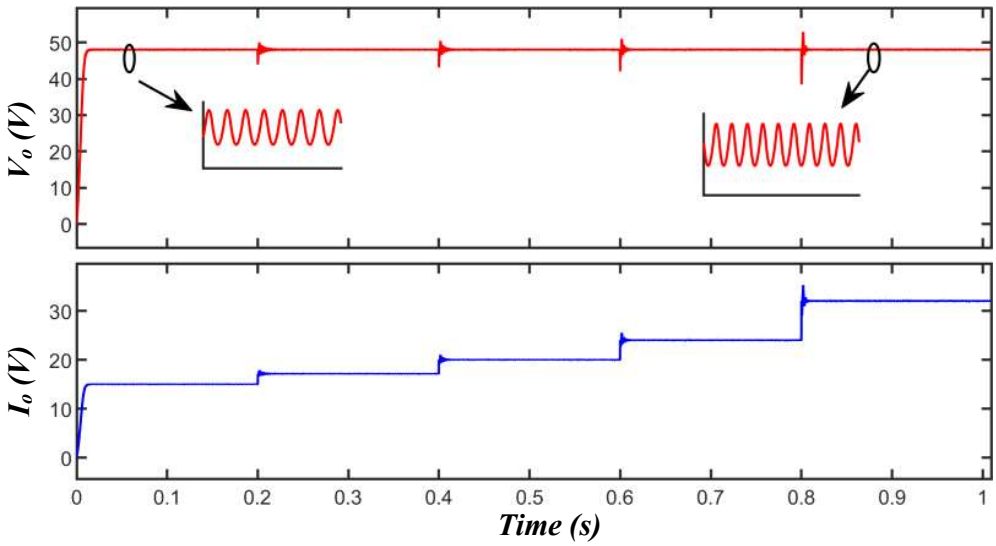


Fig 4.11 Load variation from 16 Ω to 7.5 Ω

4.2.1.4 Current Mode Control

4.2.1.4.1 Reference Current tracking

The reference current tracking performance was evaluated for Cuk converters under dual-loop PI control in Fig.4.12. The reference current was dynamically changed in steps, starting from 3.5A and incrementing up to 5.5A. The Current Mode Control exhibited exceptional precision with a small steady-state error of 0.72%, implying a superior capability in maintaining output voltage with high accuracy across the given range.

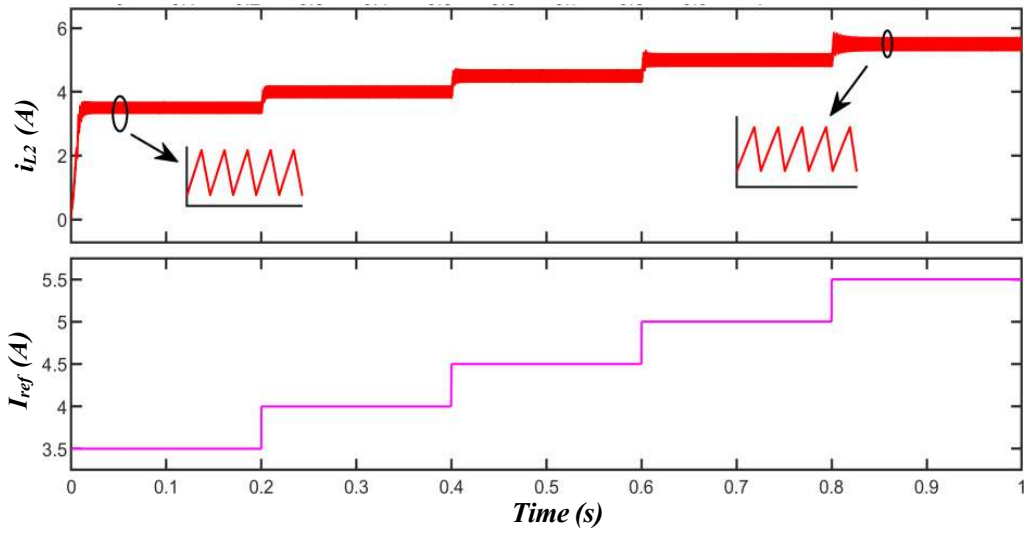


Fig 4.12 Simulation result for reverence current variation from 3.5A to 5.5A

4.2.1.4.2 Line voltage tracking

Several simulations assessed the current-controlled Cuk converter's line regulation capabilities. The converter model was tested with 14V to 30V input voltages. These situations tested the converter's output current stability despite input voltage swings. Fig. 20 shows that the Cuk converter regulates output current well. Output current remained at 4.166A regardless of input voltage. The robust current control system of the Cuk converter design ensured stability.

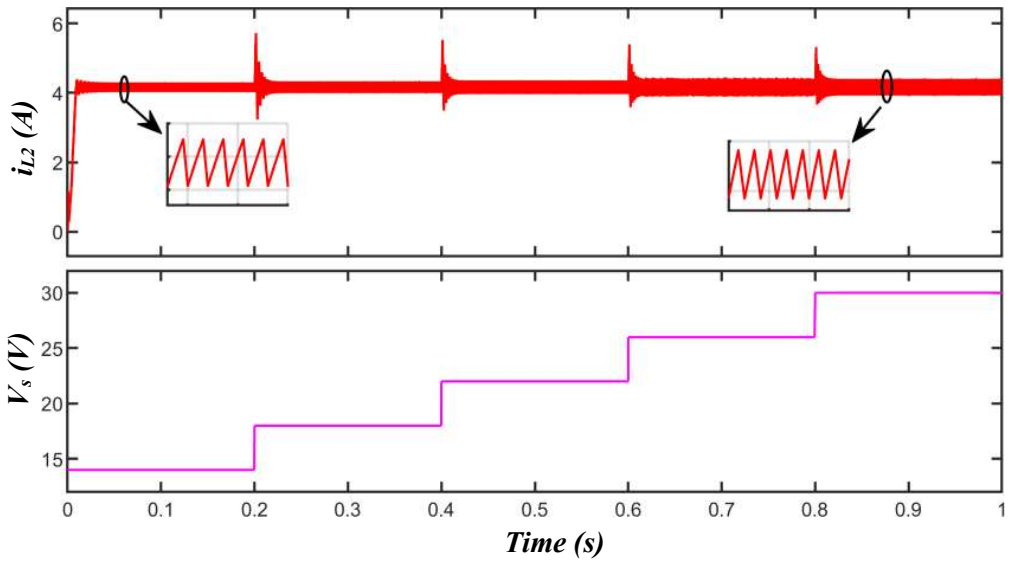


Fig 4.13Simulation results for line voltage variation from 14V to 30V

4.2.1.4.3 Variation in load current

The closed-loop current-controlled Cuk converter's performance was assessed while the load resistance circumstances were changed. The load resistance was changed from 16Ω, resulting in a minimum load current of 3A, to 7.5Ω, resulting in a maximum load current of 6.5A. During these fluctuations, the output current remained consistently at a constant value of 4.166A.

While changing from a resistance of 16Ω to 7.5Ω, the output current saw a small decrease below the desired level. Nevertheless, it rapidly stabilised at the intended magnitude of 4.166A in just 13ms.

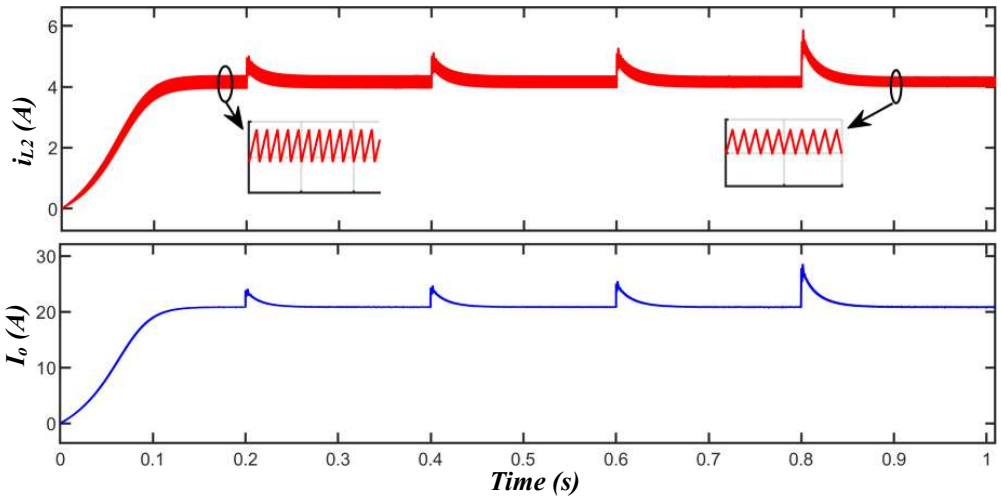


Fig 4.14Simulation of results for load resistance variation from 16 Ω to 7.5 Ω

4.2.2 PID CONTROLLER DESIGN OF IDEAL CUK CONVERTER

As was previously discussed, the uncompensated Cuk converter showed steady-state inaccuracy and poor phase margin in the low-frequency band. An initial implementation of a PI controller intended to improve these performance features. Phase margin and low-frequency gain of this PI controller were successfully increased. But it also resulted in a better phase margin at a lower gain crossover frequency, which because of the slower reaction, prolonged the settling time of the output voltage.

Based on these observations, it would be wise to incorporate a derivative component into the PI controller in order to enhance system performance. By incorporating the derivative action, the controller gains the ability to anticipate future errors by analysing the current rate of change. This level of foresight enables a greater ability to make proactive adjustments, effectively minimizing errors before they become significant. This derivative term introduced by the PID controller improves the dynamic response of the system as a whole, especially its bandwidth and phase margin around the gain crossover frequency. Fundamentally, by dampening oscillations and lowering overshoot, the PID controller not only accelerates response time but also quickly stabilises the output. The PID is a priceless enhancement from the simpler PI setup in managing an ideal Cuk converter since this improvement is essential in applications that require great accuracy and precision under changing operating conditions.

The transfer function of PID controller is:

$$G_c(s) = K_p + \frac{K_{ii}}{s} + K_D s \tag{4.14}$$

Where K_p, K_{ii} and K_D are PID controller parameters.

4.2.2.1 Voltage Mode Control

When operating an ideal Ćuk converter with voltage mode control, a highly effective method is utilized to efficiently regulate the converter's output voltage. Central to this approach is the use of a PID controller, which is essential for achieving the desired performance characteristics, including increased stability, decreased steady-state error, and improved dynamic response. Nevertheless, the progression towards more sophisticated control schemes has resulted in the integration of a PI-lead controller to tackle distinct challenges and meet performance requirements.

The difference between the converter's real output voltage and the intended setpoint is represented by the voltage error, or V_{err} in this modified approach. Then a PI-lead controller is used to route this error signal. The major job of the PI-lead controller is to carefully alter the error signal to produce a control voltage, denoted as V_c. After the control voltage V_c is generated, it is then compared to a reference signal. This reference signal is a sawtooth waveform with a fixed frequency and magnitude. This comparison leads to the generation of gate pulses, which in turn modulate the energy transfer between the converter's input and output to maintain a stable output voltage at the desired level.

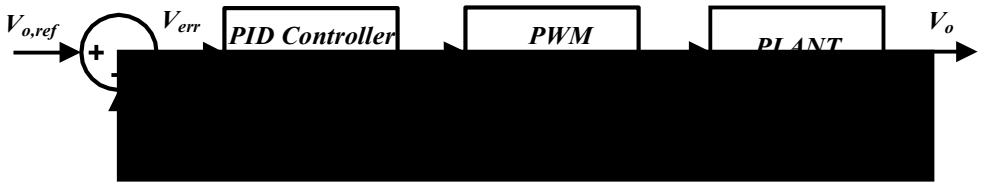


Fig 4.15Voltage mode control using PID Controller

Cuk converter uncompensated loop transfer function stays equal to that in (4.9). It is rewritten below just for clar0ity:

$$T(s) = G_{PWM}(s)G_{vd}(s) = \frac{1}{V_{sss}} G_{vd}(s) \tag{4.15}$$

$$T(s) = \frac{4.688 \times 10^{10}\, s^2 - 1.404 \times 10^{14}\, s + 1.057 \times 10^{18}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \quad (4.16)$$

The design algorithm covered in the previous part is followed in the construction of the PI-lead controller for the Cuk converter. A particular set of criteria—a gain crossover frequency (GCF) of 0.5 kHz and a desired phase margin (PM) of 30 degrees—is used to demonstrate this design technique. This approach shows the flexibility and adaptability of the design process for optimizing the performance of the Cuk converter according to different operational criteria since it is consistent and applicable to other specification sets as well.

We select $K_p = 5.9813 \times 10^{-4}$, $K_{ii} = 3.6728$, and, $K_d = 2.43 \times 10^{-8}$With these values, the PID controller transfer function is:

$$G_c(s) = K_p + \frac{K_{ii}}{s} + K_d s \quad (4.17)$$

$$G_c(s) = 5.9813 \times 10^{-4} + \frac{3.6728}{s} + 2.43 \times 10^{-8} s \quad (4.18)$$

Therefore, the loop transfer function of compensated Cuk converter is given by:

$$G_c(s)T(s) = \frac{1427\, s^4 + 3.163 \times 10^7 s^3 + 1.634 \times 10^{11}\, s^2 + 2.743 \times 10^{14}\, s + 4.852 \times 10^{18}}{s^5 + 4.34 \times 10^4 s^4 + 6.735 \times 10^8 s^3 + 9.766 \times 10^{11}\, s^2 + 4.902 \times 10^{15}\, s} \quad (4.19)$$

A DC-DC Ćuk converter with PID (Proportional-Integral-Derivative) control optimized is shown in Figure 4.16 with its frequency response. Accurately meeting the intended performance standards, the system achieves a desirable phase margin of 74.1° at a gain crossover frequency of 0.133 kHz. The gain has been modified, notably with a slope of -20 dB/decade and an increase in the low-frequency range presently. Since it eliminates the steady-state inaccuracy in reaction to any abrupt disruptions, this particular modification is essential. Furthermore, an increased response speed brought about by the gain crossover frequency increase indicates a general improvement in the dynamic behaviour and stability of the system.

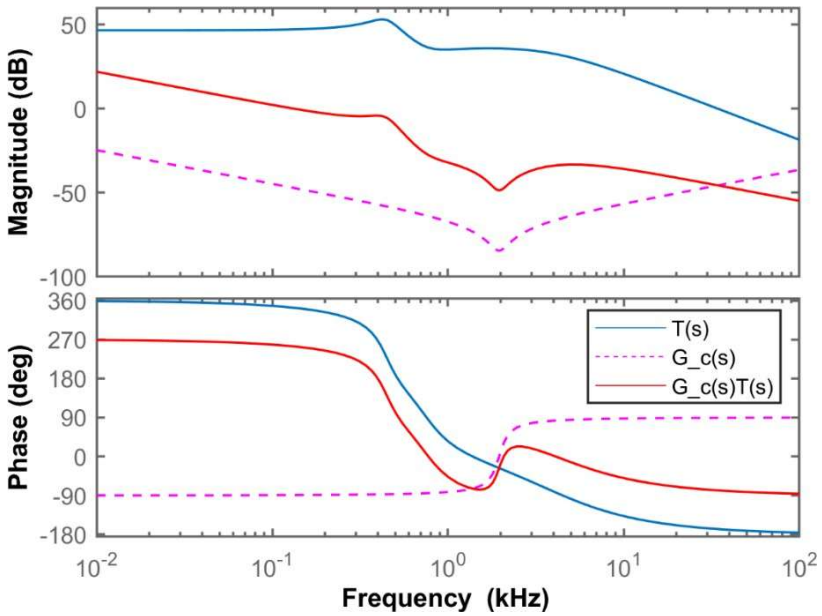


Fig 4.16Frequency response of PID Controlled Cuk Converter

4.2.2.2 Current Mode Control

Implementing current mode control in an ideal Ćuk converter with a PID control provides numerous benefits for optimizing and improving the converter's performance. Current mode control is a technique that focuses on regulating the operation of the converter by primarily considering the current flowing through it, rather than solely focusing on regulating the output voltage. This approach to control offers a precise grip on the power being transferred, resulting in faster response times and enhanced stability when dealing with different load conditions.

Combining PID control with current mode control has special advantages because of its derivative feature. It reacts to the rate of change of the error to predict system disturbances and enables pre-emptive corrections before significant deviations arise. A more steady and dependable system results from the significant decrease in overshoot and settle times.

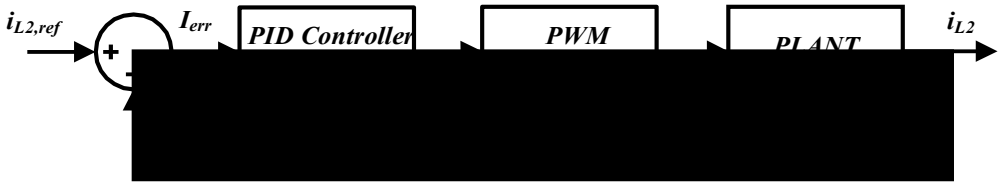


Fig 4.17 Current mode control using PID Controller

In discussing the behaviour of the ideal Cuk converter, we reference its duty cycle to inductor current transfer function detailed as Eqn. 4.12.

Let the duty cycle to Inductor current transfer function for the ideal cuk converter be:

$$G_{iid}(s) = \frac{\hat{\imath}_{L_2}}{\hat{d}} = \frac{93750\,s^3 + 3.788 \times 10^9\,s^2 - 1.008 \times 10^{13}\,s + 9.174 \times 10^{16}}{s^4 + 4.34 \times 10^4\,s^3 + 6.735 \times 10^8\,s^2 + 9.766 \times 10^{11}\,s + 4.902 \times 10^{15}} \quad (4.20)$$

Along with this, the converter's loop transfer function without compensation is identified as 4.13, incorporating specific constants for this design.

$$T(s) = G_{PWM}(s)G_{iid}(s) \quad (4.21)$$

$$T(s) = \frac{93750\,s^3 + 3.788 \times 10^9\,s^2 - 1.008 \times 10^{13}\,s + 9.174 \times 10^{16}}{s^4 + 4.34 \times 10^4\,s^3 + 6.735 \times 10^8\,s^2 + 9.766 \times 10^{11}\,s + 4.902 \times 10^{15}} \quad (4.22)$$

Where $G_{PWM}(s) = \frac{1}{V_{sss}}$ and $V_{sss} = 1$ for this compensator design.

The phase margin of the unaltered Cuk converter is initially 93.2°, as seen in Fig 4.18. This happens at 15.8 kHz, the gain crossover frequency. Furthermore, the tendency for steady-state errors is found, which is caused by the converter's ongoing gain at lower frequencies in the presence of step disturbances in the system.

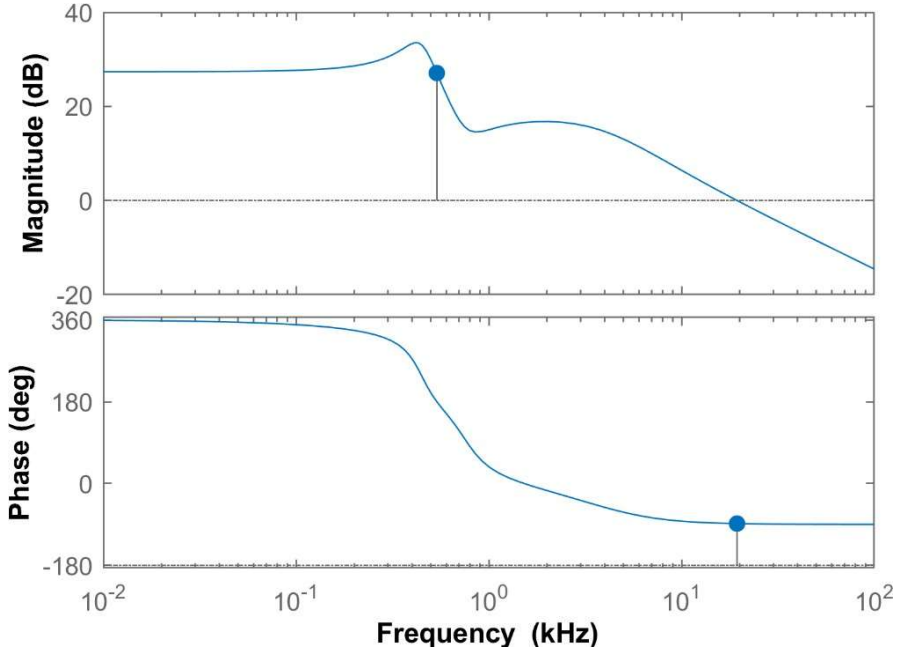


Fig 4.18 Frequency response of Uncompensated Cuk Converter

After the PID controller is installed, as the Bode plot Fig.4.19 shows, a happy story starts. There is an amazing rise to 80° in the phase margin. But along with this climb, the gain crossover frequency falls, now at a modified 125 Hz. Unquestionably, the higher phase margin helps to prevent overshoots, but the lowered crossover frequency causes a slower reaction to start. Though it is a big trade-off, better system stability requires it. Even more so, a crucial change is shown with the gain at lower frequencies, showing a -20 dB/decade decline.

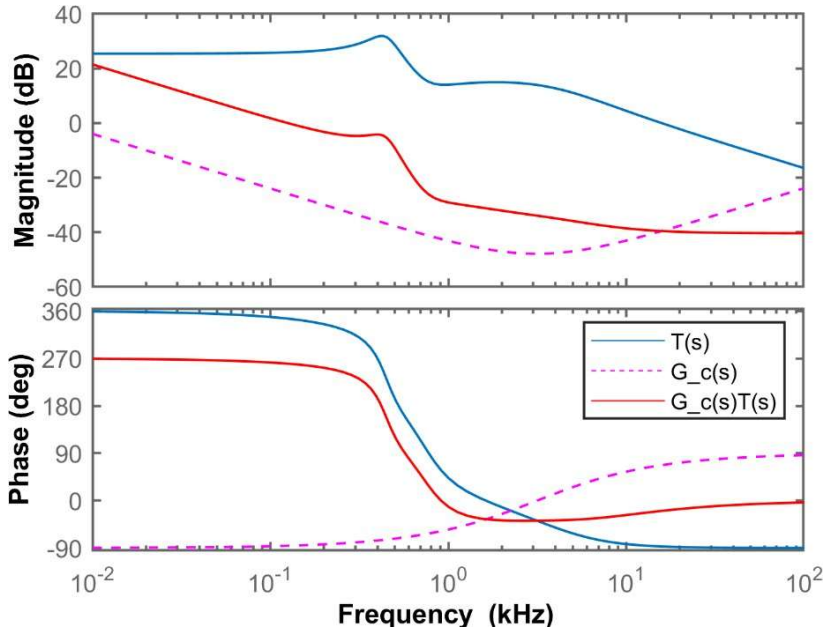


Fig 4.19 Frequency response of PID controlled Cuk Converter

This particular change is essential in eliminating steady-state mistakes and represents a significant step in improving the accuracy and stability of the system throughout a wide range of operating situations.

4.2.2.3 Results and Discussion

In order to assess the effectiveness of the PID controller as outlined in equation (4.23), software simulations were carried out on a closed-loop DC-DC Cuk converter. The parameters utilised for the simulations are in accordance with the ones specified in Table 4.1. The simulation results were obtained using the MATLAB/Simulink software. The results were subsequently compared and examined under three specific conditions: (a) variations in the reference output voltage, (b) variations in the input voltage, and (c) variations in the load current.

4.2.2.3.1 Reference Voltage tracking

The performance of the PID controller designed for the Cuk converter is assessed for a step change in the reference output voltage $V_{o,rerr}$ The input voltage V_s and load resistance R_o are kept at constant values of 24V and 11.52 Ω, respectively. The simulation results, shown in Figure 4.20, illustrate the response to a change in the reference voltage from 14V to 30V. In both scenarios, the output voltage quickly reaches the desired value of 20ms, without any overshoot or oscillations. Given the constant load resistance of 11.52 Ω, the load current adapts to the new output voltage, resulting in a load current of 4.166A.

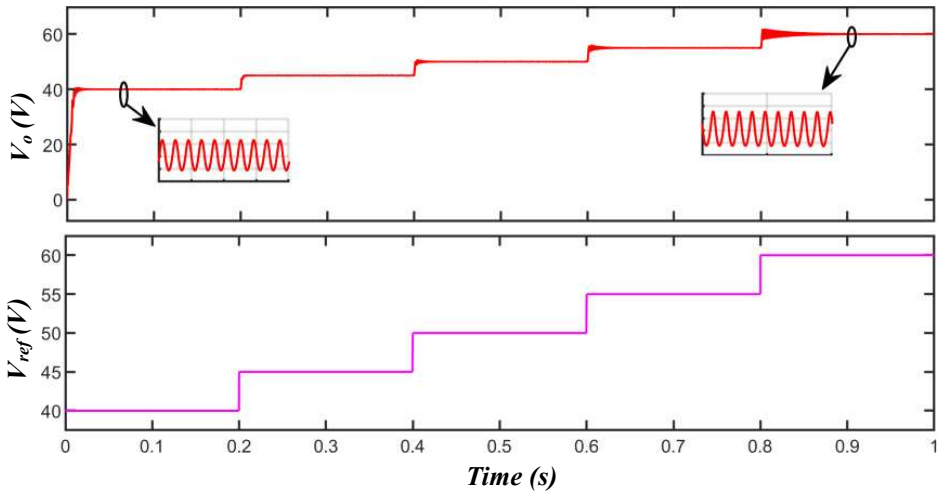


Fig 4.20 Simulation results for reference voltage tracking from 40V to 60V

4.2.2.3.2 Line Voltage Variation

Simulation results were obtained for step changes in input voltage while maintaining a constant load. The value of R_o was 11.52 Ω and the input voltage V_s varied from 14V to 30V. The output voltage quickly returns to its stable value of 48V within 13 ms when the input voltage increases from 14V to 30V. However, there are significant fluctuations and excessive overshooting in the output voltage during the transient phase, as illustrated in Fig.4.21.

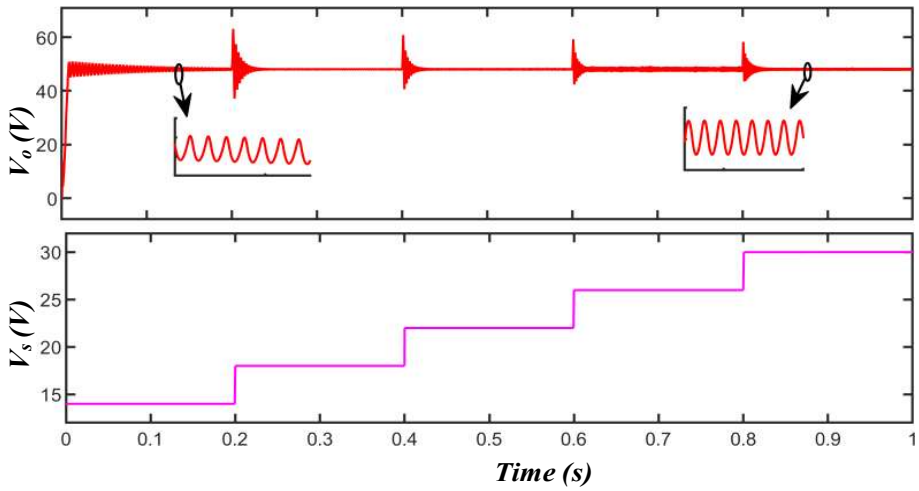


Fig 4.21 Simulation results for line voltage variation from 14V to 30V

4.2.2.3.3 Variation in Load Resistance

Investigating the performance of the closed-loop Cuk converter under varying load conditions, while keeping the input voltage constant. Starting with a load resistance of 16 Ω and a lowest load current of 3A, the load resistance R_o is then adjusted to 7.5Ω, resulting in a maximum load current of 6.5A. The output voltage exhibits a brief decrease of 4V before stabilising at 48V within a time span of 20 ms, in response to changes in the load resistance from 16Ω to 7.5Ω.

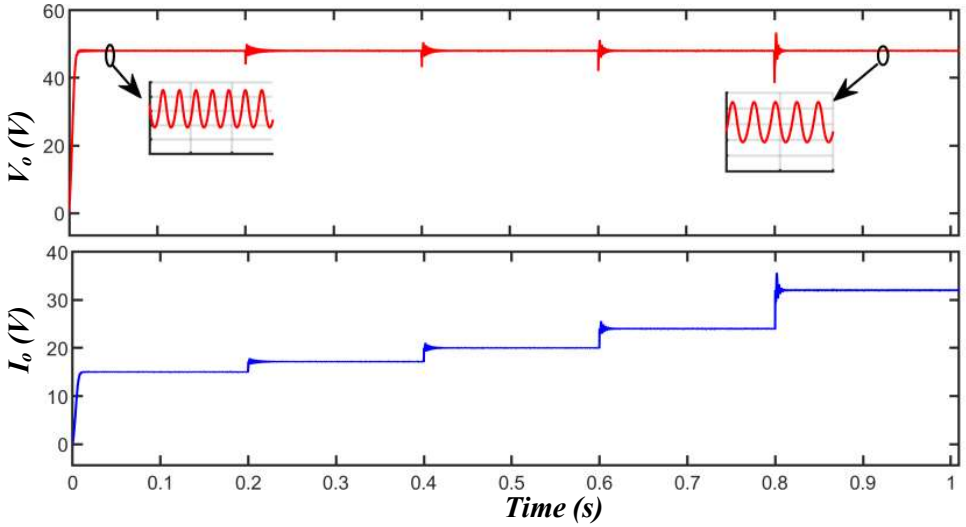


Fig 4.22 Simulation results for load variation from 16 Ω to 7.5 Ω

4.2.2.4 Current Mode Control

4.2.2.4.1 Reference Current tracking

Fig.4.23 illustrates the evaluation of the reference current tracking performance for Cuk converters under closed loop PID control. The reference current was adjusted gradually, starting from 3.5A and increasing up to 5.5A. The Current Mode Control demonstrated remarkable precision, with a minimal steady-state error of 0.72%. This indicates its exceptional ability to maintain output voltage with utmost accuracy throughout the specified range.

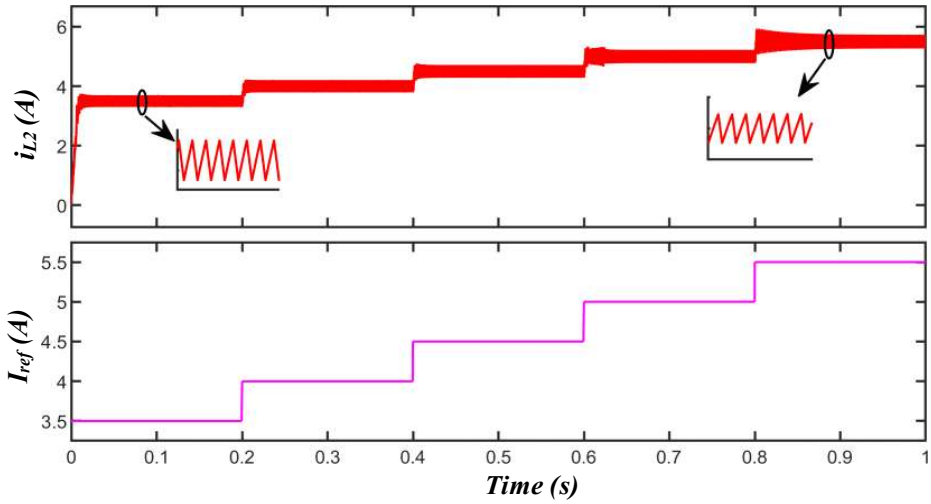


Fig 4.23 Simulation results for reference current variation from 3.5A to 5.5A

4.2.2.4.2 Line voltage tracking

Multiple simulations were conducted to evaluate the line regulation capabilities of the current-controlled Cuk converter. The converter model underwent testing using input voltages ranging from 14V to 30V. These situations challenged the converter's ability to maintain stable output current, even when there were fluctuations in the input voltage. Fig.4.24 demonstrates the excellent regulation of output current by the Cuk converter. The current output remains steady at 4.166A, unaffected by changes in the input voltage.

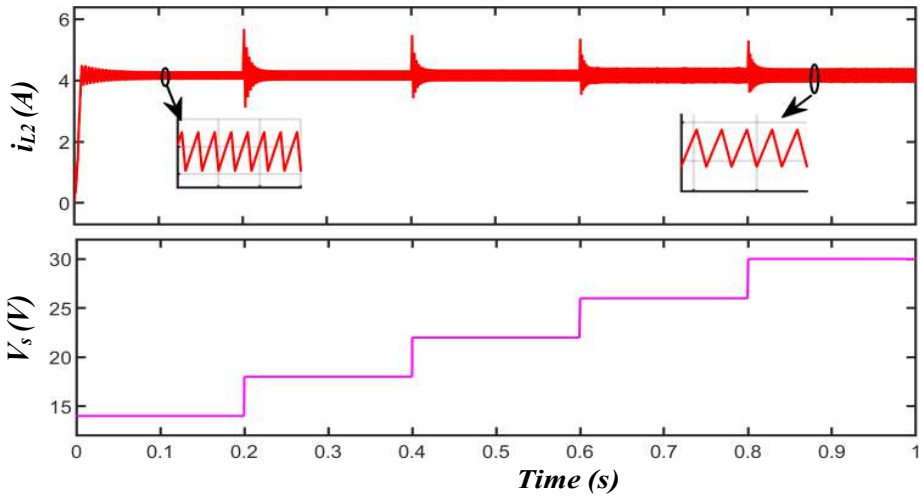


Fig 4.24 Simulation results for line voltage variation from 14V to 30V

4.2.2.4.3 Variation in load current

Performance of the closed-loop current-controlled Cuk converter was evaluated under varying load resistance conditions. From 16Ω, the load resistance was altered to provide a minimum load current of 3A and a maximum load current of 6.5A. The output current stayed always at a constant amount of 4.166A during these variations. The output current dropped somewhat below the intended amount as one moved from a resistance of 16Ω to 7.5Ω. Still, it quickly settled at the planned 4.166A in just 20 ms.

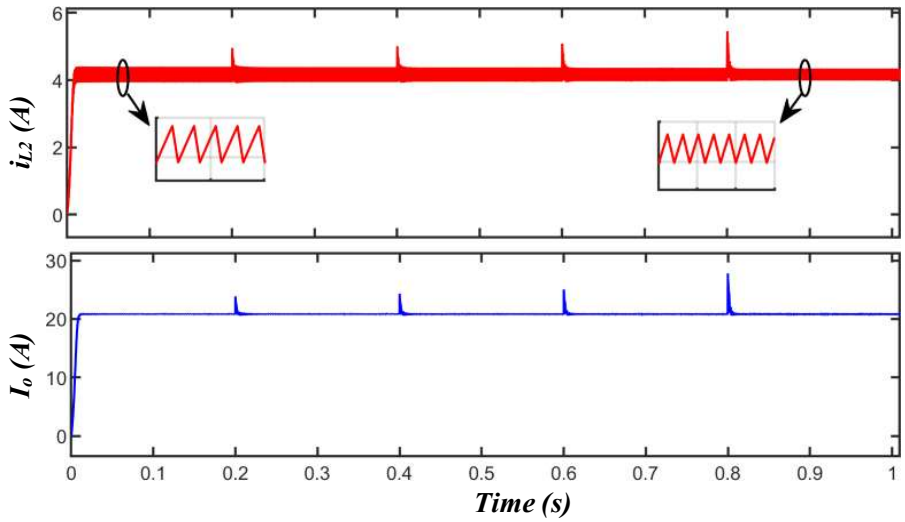


Fig 4.25 Simulation results for load resistance variation from 16 Ω to 7.5 Ω

4.2.3 PI CONTROLLER DESIGN FOR AN NON-IDEAL CUK CONVERTER

This part focuses on the design of PI control specifically for the DC-DC Cuk converter. Simulation results are displayed to demonstrate the performance of the PI controller.

Table 4.2 Controller design parameters for Non-Ideal Cuk Converter

Parameters	Values
Input Voltage, V_S	24V
Output Voltage, V_o	48V
Load Resistance,R_o	11.52Ω
Inductance L_1/r_{L_1}	0.384µH /0.1 Ω
Inductance L_2/r_{L_2}	0.768µH/0.1 Ω
Decoupling Capacitor,C_1/r_{C_1}	38.58µF/1 µΩ
Filter Capacitor, C_2/r_{C_2}	2µF/1 µΩ
Switching Frequency, f_{sss}	50kHz
Diode Resistance,R_D	0.1Ω
MOSFET Resistance, R_{ds}	0.25Ω
Desired Inductor current ripple $\Delta i_{L_1}/\Delta i_{L_2}$	$10\%I_{L_1}$/ $10\%I_{L_2}$
Desired Output voltage ripple, $\Delta V_{c_1}/\Delta V_{c_2}$	$1\%V_{c_1}$/1% V_{c_2}

4.2.3.1 Voltage Mode Control

The closed-loop PI (Proportional-Integral) control mechanism for a DC-DC Cuk converter is depicted in Figure 4.47, with a more comprehensive diagram available in Figure 4.48. This design mirrors that of the ideal Cuk converter with PI control. Here, the actual output voltage V_o,is measured and compared against a predefined reference output voltage,V_{rerr}. The difference between these voltages, known as the voltage error $V_{err}$is routed through a PI controller $G_c(s)$. This process yields a control voltage $V_c$which is then set against a constant peak and frequency sawtooth waveform. The comparator's output delivers the switch pulses necessary to achieve the desired duty cycle, effectively regulating the DC output voltage of the Cuk converter. This ensures that the system can maintain stable output under varying conditions.

Table 4.2 contains the Cuk converter under analysis's parameters. These are the same values applied in Chapter 3's Cuk converter modelling. With certain operational conditions assumed: an input voltage ($V_s = 20V$) and a maximum load current, corresponding to a minimum load resistance ($R_o = 11.52\ \Omega$), in this chapter we construct the mathematical model for the controller design of the Cuk converter.

We already covered the duty-cycle to output-voltage transfer function for the Cuk converter in Chapter 3—more especially, in equation 3.281. Applying the Table 4.2 parameters results in

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{0.09137s^3 + 4.569 \times 10^{10}s^2 - 1.248 \times 10^{14}s + 8.875 \times 10^{17}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}s + 5.877 \times 10^{15}} \quad (4.23)$$

The uncompensated loop transfer function of Cuk converter will be

$$T(s) = G_{PWM}(s)G_{vd}(s) = \frac{0.09137s^3 + 4.569 \times 10^{10}s^2 - 1.248 \times 10^{14}s + 8.875 \times 10^{17}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}s + 5.877 \times 10^{15}} \quad (4.24)$$

Where $G_{PWM} = \frac{1}{V_{sSS}}$ is the transfer function of PWM Modulator and $V_{sss} = 1$ for this modulator design.

Indicating a phase margin of 22.1° at a gain crossover frequency of 1.09 kHz, figure 4.26 shows the Bode curve for an uncompensated DC-DC Cuk converter. This somewhat low phase margin produces undesirable transient behavior marked by large overshoots. Furthermore, in the low-frequency band, the Cuk converter's gain stays constant, which results in constant steady-state errors should the system suffer a step disturbance.

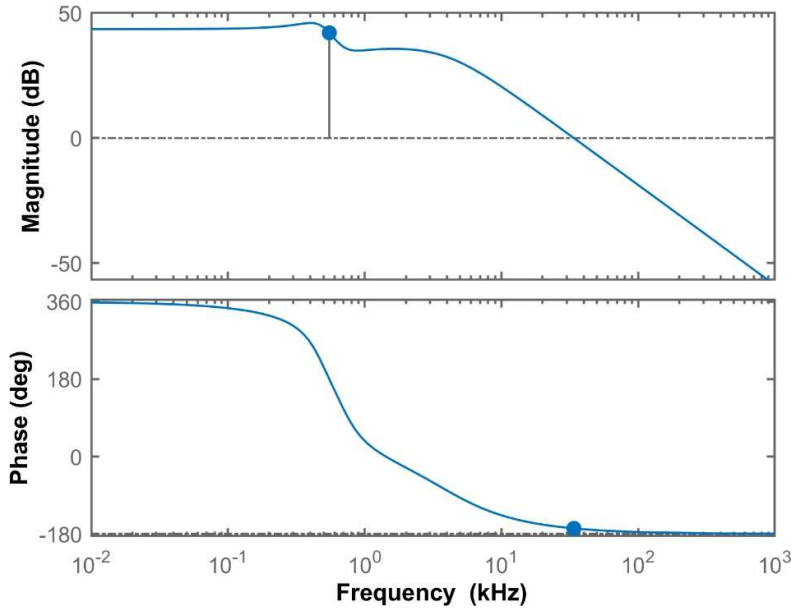


Fig 4.24 Frequency response of Uncompensated Cuk Converter

A PI (Proportional-Integral) controller has been developed to tackle the challenges at hand, namely the steady-state errors and inadequate phase margin. We have optimized the parameters of this PI controller using the Ziegler-Nicholas method, resulting in enhanced performance which is given below:

$$G_c(s) = K_p + \frac{K_{ii}}{s} \tag{4.25}$$

$$G_c(s) = 2.1 \times 10^{-4} + \frac{5.1032}{s} \tag{4.26}$$

Figure 4.27 depicts the Bode plot for the Cuk converter with PI compensation. Based on the data provided, it is evident that the phase margin of the Cuk converter in its closed-loop configuration has experienced a substantial increase, reaching 73°. Nevertheless, there is a clear decrease in the gain crossover frequency, which drops to 127 Hz. The improved phase margin helps reduce overshoots and enhances the stability of the system. However, the decrease in crossover frequency results in a slower response time, indicating that the system's ability to respond rapidly to changes is somewhat compromised. Remarkably, the gain at low frequencies now shows a -20 dB/decade slope. This adjustment eliminates the problem of steady-state error, guaranteeing that the output remains precise and stable over time, even when disturbances are present.

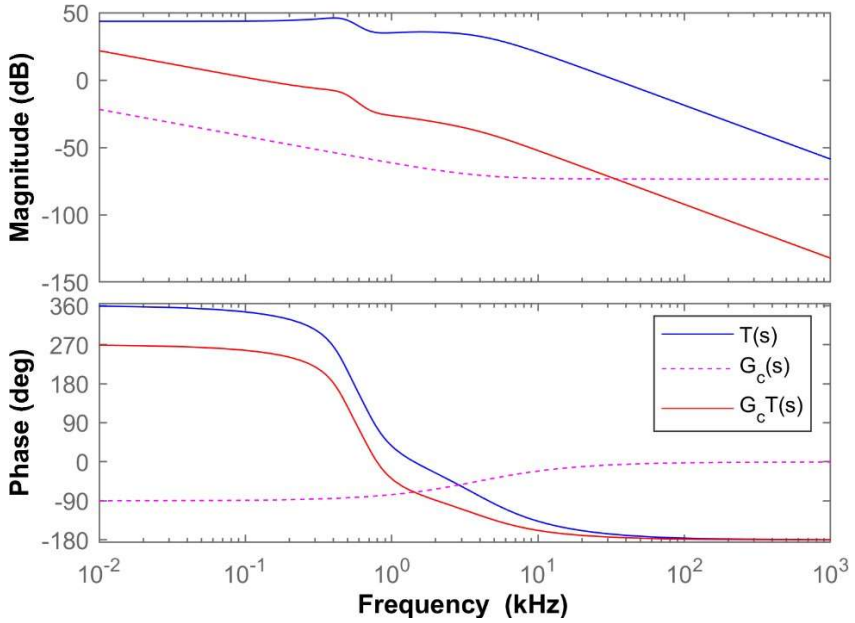


Fig 4.25 Frequency response of PI controlled Non-Ideal Cuk converter

4.2.3.2 Current Mode Control

In the previous section, we discussed the principles of current mode control and its implementation in converter systems. Building on that foundation, we can now consider the application of current mode control to a non-ideal Cuk converter.

The Cuk converter, in real-world scenarios, presents certain challenges that need to be addressed. These challenges include component non-linearities and parasitic effects, which can have an impact on the overall performance and stability of the system. Through the implementation of current mode control, the converter's capacity to handle fluctuations in input voltage and load conditions is improved, ensuring stable operation by directly regulating the inductor currents.

Let the duty cycle to Inductor current transfer function for the ideal cuk converter be:

$$G_{iid}(s) = \frac{\hat{\imath}_{L_2}}{\hat{d}} = \frac{9.137 \times 10^4 s^3 + 3.716 \times 10^9 s^2 - 9.061 \times 10^{12} s + 7.704 \times 10^{16}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (4.27)$$

The uncompensated loop transfer function of the Cuk converter is as follows:

$$T(s) = G_{PWM}(s) G_{iid}(s) = \frac{9.137 \times 10^4 s^3 + 3.716 \times 10^9 s^2 - 9.061 \times 10^{12} s + 7.704 \times 10^{16}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (4.28)$$

Where $G_{PWM}(s) = \frac{1}{V_{SSS}}$ and $V_{sss} = 1$ for this compensator design.

The phase margin of 93.9° for the uncompensated DC-DC Cuk converter is shown in Fig 4.28 at a gain crossover frequency of 15.4 kHz.. A steady-state error can also arise from the converter's consistent gain in the low-frequency spectrum when a step disturbance occurs in the system. A PI (Proportional-Integral) controller is implemented to address these problems with phase margin and steady-state error in the Cuk converter. The Ziegler Nicholas method is used in the parameter tuning of this PI controller with the goal of improving the converter's dynamic response as well as its steady-state performance.

The Bode plot for a PI-compensated Cuk converter, presented in Figure 4.29, demonstrates an increase in the phase margin to 73.3°, while the gain crossover frequency drops to 129 Hz. This enhancement in phase margin is beneficial for

reducing overshoots, albeit at the cost of a slower response due to the lower crossover frequency. Additionally, the gain at low frequencies now shows a slope of -20 dB/decade, a change that significantly contributes to the elimination of steady-state errors in the system.

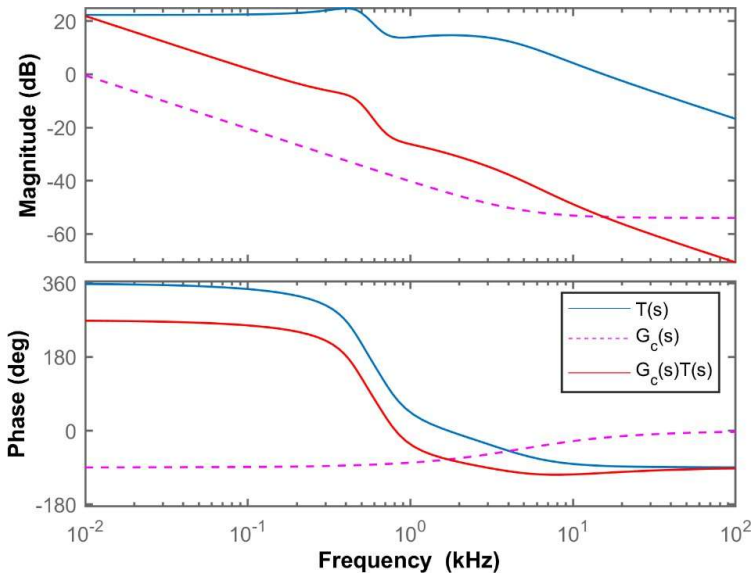


Fig 4.26 Frequency response of PI controlled Non-Ideal Cuk converter

4.2.3.3 Result and discussion

Simulations on a closed-loop non-ideal DC-DC Cuk converter were carried out to assess the PI controller specified in equation (4.23). The simulation parameters matched those shown in Table 4.2. Results were acquired and examined under three conditions—variations in reference output voltage, variations in input voltage, and variations in load current—using MATLAB/Simulink.

4.2.3.3.1 Reference Voltage tracking

The performance of the PI controller for the non-ideal Cuk converter was evaluated for a step change in reference output voltage$V_{o,rerr}$. The input voltage $V_s$and load resistance R_o were kept constant at 24V and 11.52Ω, respectively. The simulation results, presented in Figure 4.29, demonstrate the response to a reference voltage change from 40V to 60V. The output voltage quickly stabilizes at the desired value within 5.493ms, without any overshoot or oscillations. With the load resistance constant at 11.52Ω, the load current adjusts accordingly, resulting in a steady-state current of 4.166A.

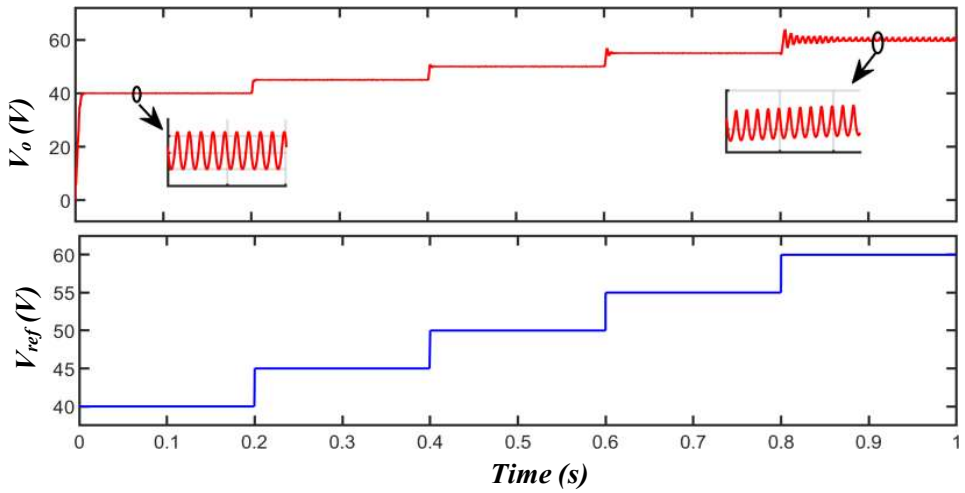


Fig 4.27 Simulation results for reference voltage tracking from 40V to 60V

4.2.3.3.2 Line Voltage Variation

Simulation results were obtained for step changes in input voltage while maintaining a constant load with R_o set at 11.52Ω. The input voltage V_s ranged from 20V to 40V. When the input voltage increased from 20V to 40V, the output voltage swiftly returned to its stable value of 48V within 5.4ms. However, significant fluctuations and excessive overshooting were observed in the output voltage during the transient phase, as depicted in Fig. 4.30.

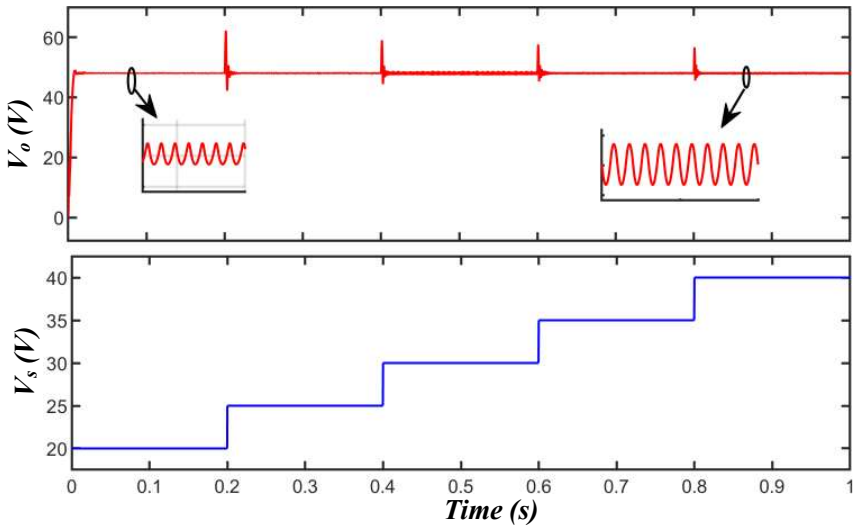


Fig 4.28 Simulation results for line voltage variation from 20V to 40V

4.2.3.3.3 Variation in Load Resistance

The performance of the closed-loop Non-ideal Cuk converter was studied under varying load conditions while maintaining a constant input voltage. Starting with a load resistance of 16Ω and a minimum load current of 3A, the load resistance $R_o$was then adjusted to 7.5Ω, resulting in a maximum load current of 6.5A. In response to these changes, the output voltage experienced a brief decrease of 4V before stabilizing at 48V within a time span of 10ms.

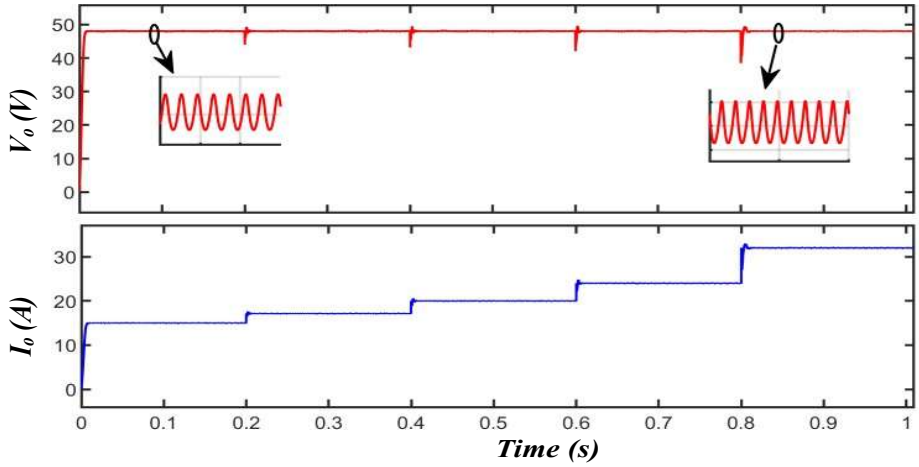


Fig 4.31 Simulation results for load resistance variation from 16 Ω to 7.5 Ω

4.2.3.4 Current Mode Control

4.2.3.4.1 Reference Current tracking

Figure 4.32 shows under closed-loop PI control the assessment of reference current tracking performance for Cuk converter. From 3.5A to 5.5A the reference current was gradually changed. With a minimum steady-state inaccuracy of 0.435%, Current Mode Control shown extraordinary accuracy.

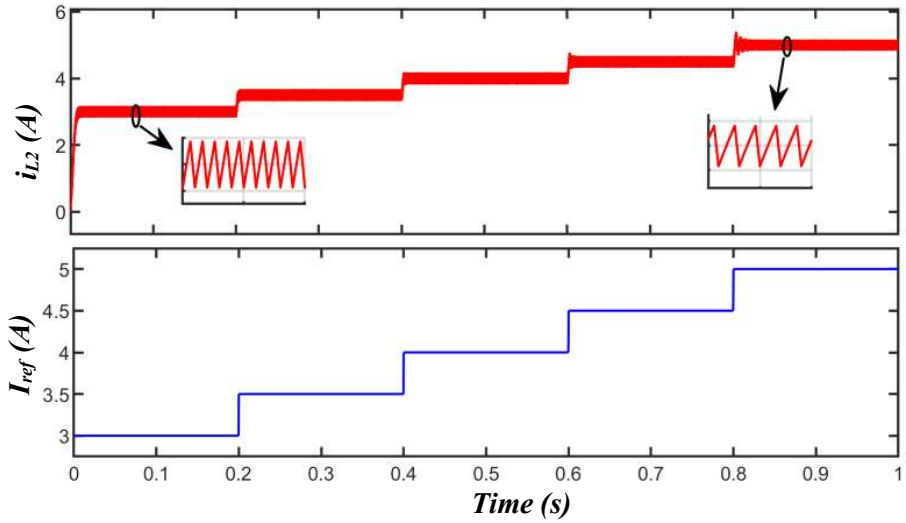


Fig 4.29 Simulation results for reference current variation from 3A to 5A

4.2.3.4.2 Line voltage tracking

To evaluate the current-regulated Cuk converter's line control capacity, several simulations were run. Testing included 20 to 40V input voltages to assess the converter's capacity to sustain a constant output current in spite of changes in input voltage. Fig. 4.33 shows the Cuk converter's extraordinary control of output current. Changes in input voltage have no effect on the constant output of 4.166A.

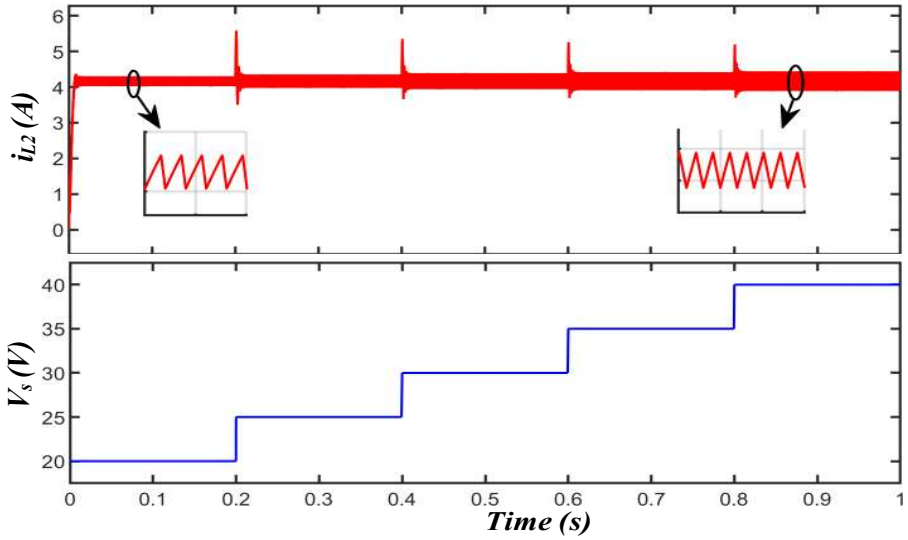


Fig 4.30 Simulation results for line voltage variation from 20V to 40V

4.2.3.4.3 Variation in load current

The closed-loop current-controlled Cuk converter's performance was assessed under varying load resistance conditions. Starting from 16Ω, the load resistance was adjusted to provide minimum and maximum load currents of 3A and 6.5A, respectively. Throughout these variations, the output current remained consistently at 4.166A. While transitioning from a resistance of 16Ω to 7.5Ω, the output current briefly dropped below the intended value. However, it quickly stabilized at 4.166A within a mere 20ms.

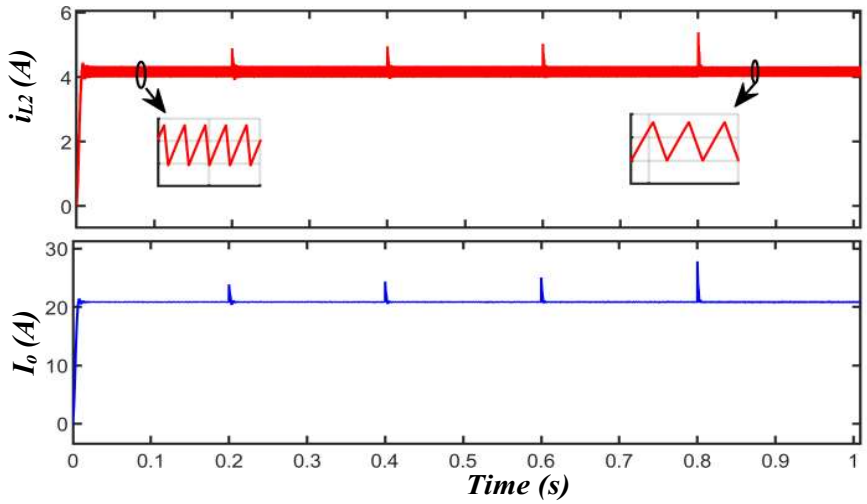


Fig 4.31 Simulation results for load resistance variation from 16 Ω to 7.5 Ω

4.2.4 PID controller design for a Non-Ideal Cuk converter

4.2.4.1 Voltage mode control

Proceeding from our analysis of voltage mode control using PID controllers for ideal Cuk converters, the application to non-ideal Cuk converters similarly uses this strategy but with subtle changes to address the effects of non-ideal components such parasitic resistances, leakage inductances, and capacitor ESRs (Equivalent Series resistances). Both dynamic performance and voltage control quality can be much affected by these non-idealities. We can improve the duty cycle adjusting response of the Cuk converter by including a PID controller in the voltage mode control system, so optimizing it to minimize the effect of these flaws.

Cuk converter uncompensated loop transfer function stays equal to that in (4.9). It is rewritten below just for clarity:

$$T(s) = G_{PWM}(s)G_{vd}(s) = \frac{1}{V_{sss}} G_{vd}(s) \tag{4.29}$$

$$T(s) = \frac{4.688 \times 10^{10}\, s^2 - 1.404 \times 10^{14}\, s + 1.057 \times 10^{18}}{s^4 + 4.34 \times 10^4\, s^3 + 6.735 \times 10^8\, s^2 + 9.766 \times 10^{11}\, s + 4.902 \times 10^{15}} \tag{4.30}$$

The design algorithm covered in the previous part is followed in the construction of the PI-lead controller for the Cuk converter. A particular set of criteria—a gain crossover frequency (GCF) of 0.551 kHz and a desired phase margin (PM) of 30°—is used to demonstrate this design technique. This approach shows the flexibility and adaptability of the design process for optimizing the performance of the Cuk converter according to different operational criteria since it is consistent and applicable to other specification sets as well.

We select $K_p = 5.01 \times 10^4$, $K_{ii} = 6.1956$, *and* K_d =With these values, the PID controller transfer function is:

$$G_c(s) = K_p + \frac{K_{ii}}{s} + K_d s \tag{4.31}$$

$$G_c(s) = 5.01 \times 10^{-4} + \frac{6.1956}{s} + 1.016 \times 10^{-8} \tag{4.32}$$

Therefore, the loop transfer function of compensated Cuk converter is given by:

$$G_c(s)T(s) = \frac{9.286 \times 10^{-10} s^5 + 464.3\, s^4 + 2.16 \times 10^7 s^3 + 2.294 \times 10^{11} s^2 - 3.28 \times 10^{14} s + 5.4 \times 10^{18}}{s^5 + 4.457 \times 10^4 s^4 + 7.246 \times 10^8 s^3 + 1.515 \times 10^{12} s^2 + 5.877 \times 10^{15}\, s} \tag{4.33}$$

A DC-DC Ćuk converter with PID (Proportional-Integral-Derivative) control optimized is shown in Fig 4.35 with its frequency response. Accurately meeting the intended performance standards, the system achieves a desirable phase margin of 70.6° at a gain crossover frequency of 0.157 kHz. The gain has been modified, notably with a slope of -20 dB/decade and an increase in the low-frequency range presently. Since it eliminates the steady-state inaccuracy in reaction to any abrupt disruptions, this

particular modification is essential. Furthermore, an increased response speed brought about by the gain crossover frequency increase indicates a general improvement in the dynamic behavior and stability of the system.

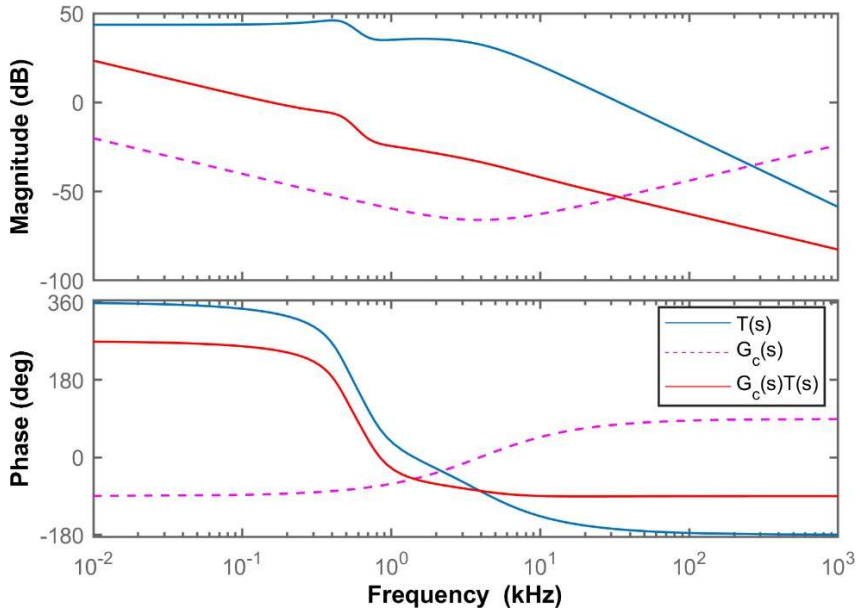


Fig 4.32 Frequency response of PID controlled Non-Ideal Cuk converter

4.2.4.2 Current Mode Control

Following the discussion on the application of current mode control using a PID controller for ideal Cuk converters, this method's adaptation to non-ideal converters necessitates a tailored approach to handle additional complexities. Non-ideal aspects such as inductor losses, capacitor ESR, and voltage drops across switches can influence the current waveform, thereby affecting overall performance. The PID controller in a current mode setup for a non-ideal Cuk converter effectively adjusts to these variations, aiding in maintaining consistent current regulation despite these non-ideal characteristics. This ensures more accurate control over the inductor currents, which is critical for the efficiency and reliability of the converter under fluctuating operating conditions.

In discussing the behaviour of the ideal Cuk converter, we reference its duty cycle to inductor current transfer function detailed as 4.12.

Let the duty cycle to Inductor current transfer function for the ideal cuk converter be:

$$G_{iid}(s) = \frac{\hat{\imath}_{L_2}}{\hat{d}} = \frac{9.137 \times 10^4 s^3 + 3.716 \times 10^9 s^2 - 9.061 \times 10^{12} s + 7.704 \times 10^{16}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (4.34)$$

Along with this, the converter's loop transfer function without compensation is identified as 4.13, incorporating specific constants for this design.

$$T(s) = G_{PWM}(s) G_{iid}(s) = \frac{9.137 \times 10^4 s^3 + 3.716 \times 10^9 s^2 - 9.061 \times 10^{12} s + 7.704 \times 10^{16}}{s^4 + 4.457 \times 10^4 s^3 + 7.246 \times 10^8 s^2 + 1.515 \times 10^{12}\, s + 5.877 \times 10^{15}} \quad (4.35)$$

Where $G_{PWM}(s) = \frac{1}{V_{sss}}$ and $V_{sss} = 1$ for this compensator design.

The phase margin of the unaltered Cuk converter is initially 93.9°, as seen in Fig 4.36. This happens at 15.4 kHz, the gain crossover frequency. Furthermore, the tendency for steady-state errors is found, which is caused by the converter's ongoing gain at lower frequencies in the presence of step disturbances in the system.

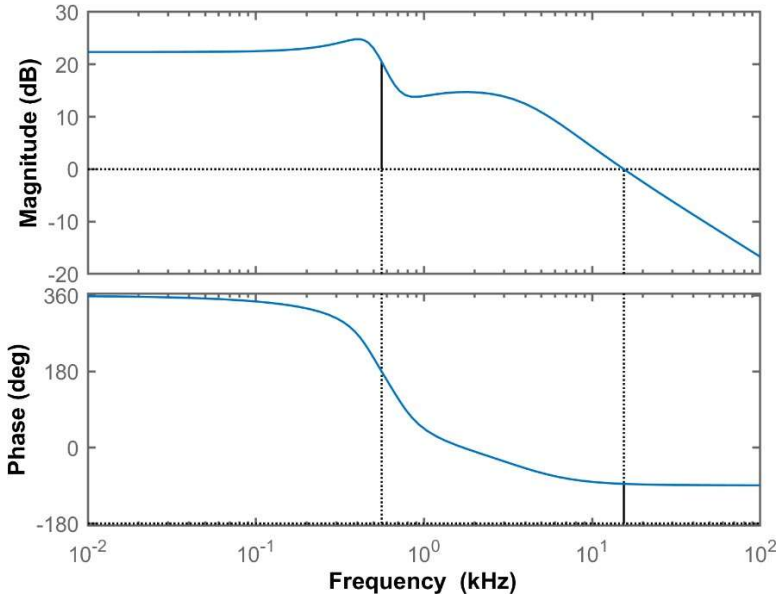


Fig 4.33 Frequency response of Uncompensated Cuk Converter

After the PID controller is installed, as the Bode plot Fig.4.37 shows, a happy story starts. There is an amazing rise to 72.4° in the phase margin. But along with this climb, the gain crossover frequency falls, now at a modified 154 Hz. Unquestionably, the higher phase margin helps to prevent overshoots, but the lowered crossover frequency causes a slower reaction to start. Though it is a big trade-off, better system stability

requires it. Even more so, a crucial change is shown with the gain at lower frequencies, showing a -20 dB/decade decline. This particular change is essential in eliminating steady-state mistakes and represents a significant step in improving the accuracy and stability of the system throughout a wide range of operating situations.

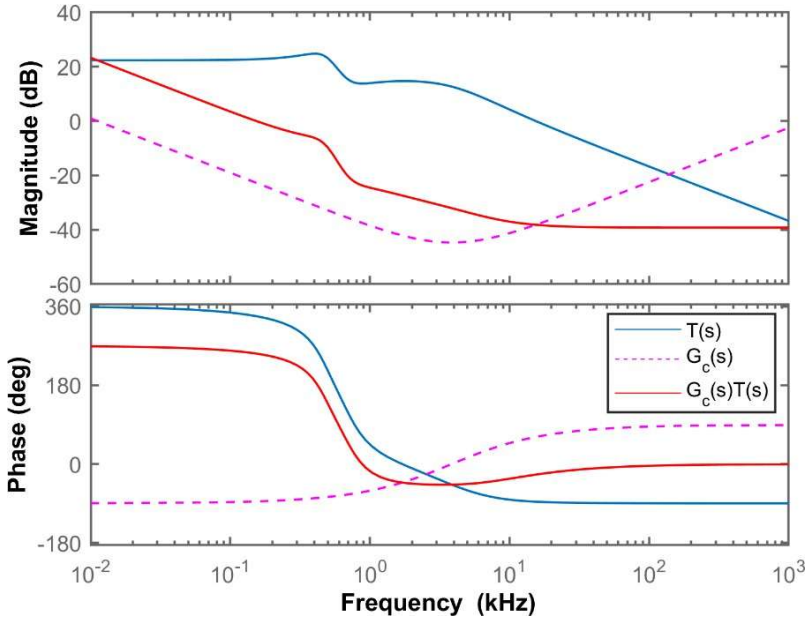


Fig 4.34 Frequency response of PID controlled Non-Ideal Cuk converter

4.2.4.3 Results and Discussion

Simulations on a closed-loop, non-ideal DC-DC Cuk converter let one assess the PID controller's efficacy as stated in equation (4.23). The criteria applied matched those in Table 4.2. The simulation results were obtained using MATLAB/Simulink and examined under three conditions: (a) variations in reference output voltage; (b) variations in input voltage; and (c) variations in load current.

4.2.4.3.1 Reference Voltage tracking

The PID controller's performance for the non-ideal Cuk converter was assessed for a step change in reference output voltage $V_{o,rerr}$. Held constant at 24V and 11.52Ω respectively, the input voltage V_s and load resistance $R_o$remained constant. Figure 4.38 displays the reaction from a reference voltage change from 40V to 60V. Without oscillations or overshoot, the output voltage arrived at the intended level in 2.62ms. The load current changed to match the increased output voltage, therefore producing a steady-state current of 4. 166A from a constant load resistance of 11.52Ω.

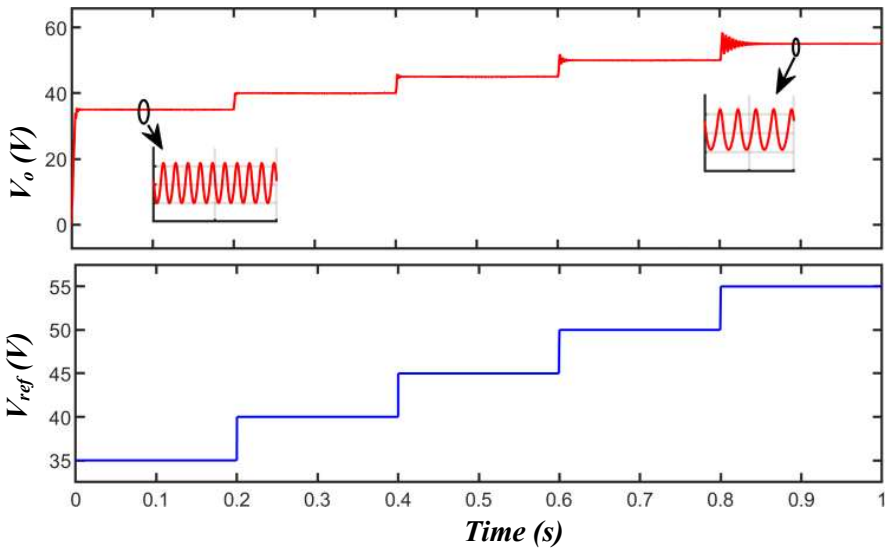


Fig 4.35 Simulation results for reference voltage tracking from 35V to 55V

4.2.4.3.2 Line Voltage Variation

Maintaining a constant load with R_o =11.52Ω, simulation results for step changes in input voltage were acquired. The input voltage,V_s ranged in value from 20V to 40V. When the input voltage rose from 20V to 40V, the output voltage promptly reverted to its steady value of 48V within3 ms. But as Fig. 4.39 shows, during the transitory phase there were notable swings and too much overshooting.

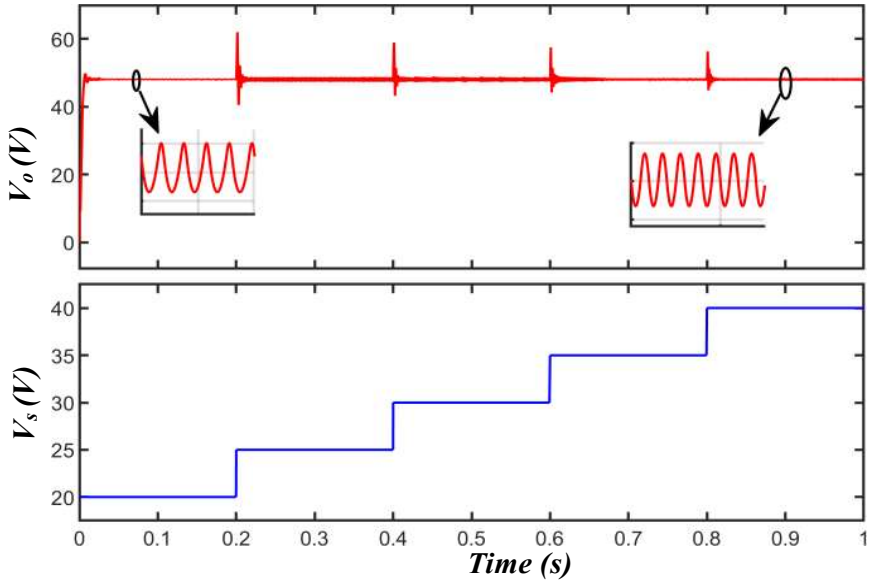


Fig 4.36 Simulation results for line voltage variation from 20V to 40V

4.2.4.3.3 Variation in Load Resistance

Closed-loop Cuk converter performance under different load circumstances with a constant input voltage was tested. Beginning with a load resistance of 16Ω and a load current of 3A, the resistance Ro was changed to 7.5Ω, therefore producing a load current of 6.5A. The change in load resistance from 16Ω to 7.5Ω caused the output voltage to momentarily decrease by 3V then stabilise at 48V within 20 ms.

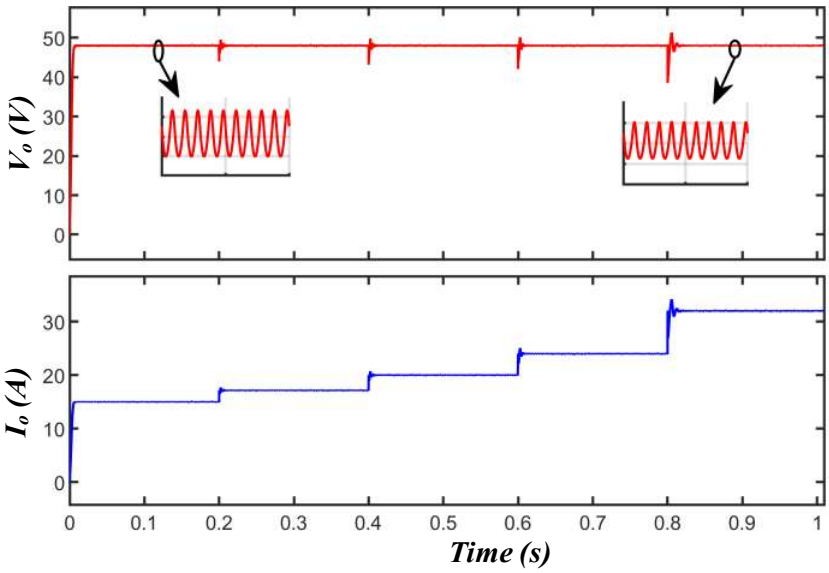


Fig 4.37 Simulation results for load resistance variation from 16 Ω to 7.5 Ω

4.2.4.4 Current Mode Control

4.2.4.4.1 Reference Current tracking

Figure 4.41 displays under closed-loop PID control the reference current tracking performance for Cuk converters. From 3.5A to 5.5A the reference current was progressively changed. With a minimum steady-state error of 0.72%, the Current Mode Control shown amazing accuracy and great capacity to sustain output voltage accuracy over the designated range.

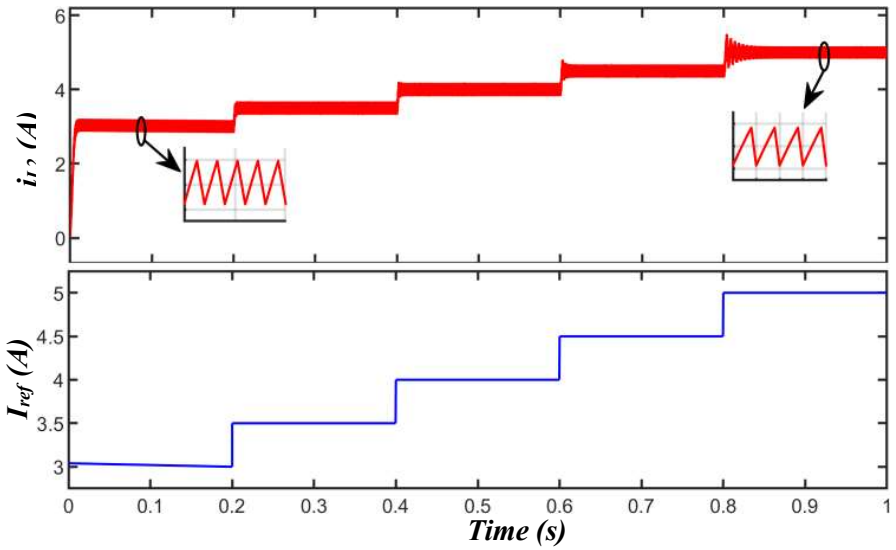


Fig 4.38 Simulation results for reference current variation from 3A to 5A

4.2.4.4.2 Line voltage tracking

Several simulations were performed to assess the line regulation of the current-controlled Cuk converter. The input voltages varied between 20V and 40V, assessing the converter's capacity to uphold a consistent output current in the face of voltage fluctuations. Figure 4.42 showcases exceptional output current regulation, maintaining a steady current of 4.166A regardless of any fluctuations in input voltage.

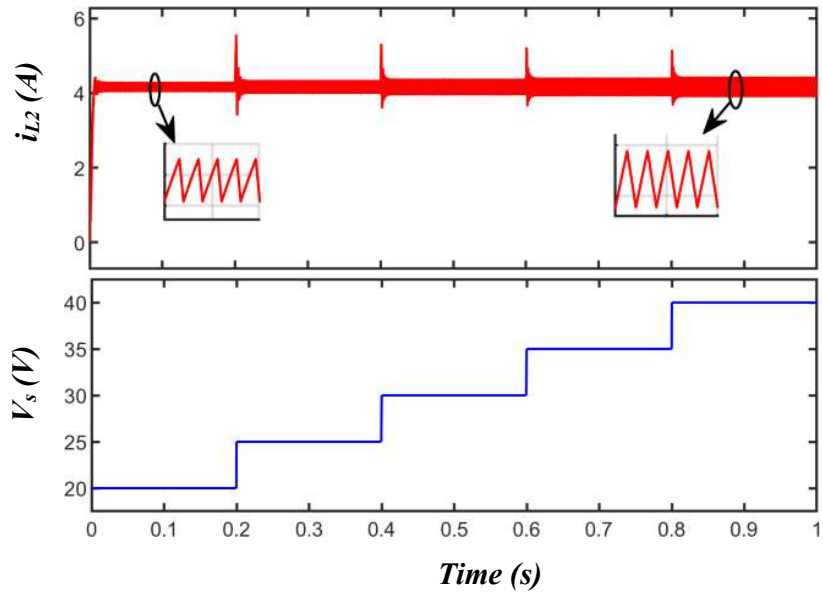


Fig 4.39 Simulation results for line voltage variation from 20V to 40V

4.2.4.4.3 Variation in load current

The closed-loop current-controlled Cuk converter was tested to assess its performance across different load resistance conditions. Beginning at 16Ω, the load resistance was fine-tuned to achieve load currents ranging from 3A to 6.5A. The output current remained consistent at 4.166A throughout these variations. The output current experienced a temporary decrease during the transition from 16Ω to 7.5Ω, but it rapidly settled at 4.166A within a mere 19ms.

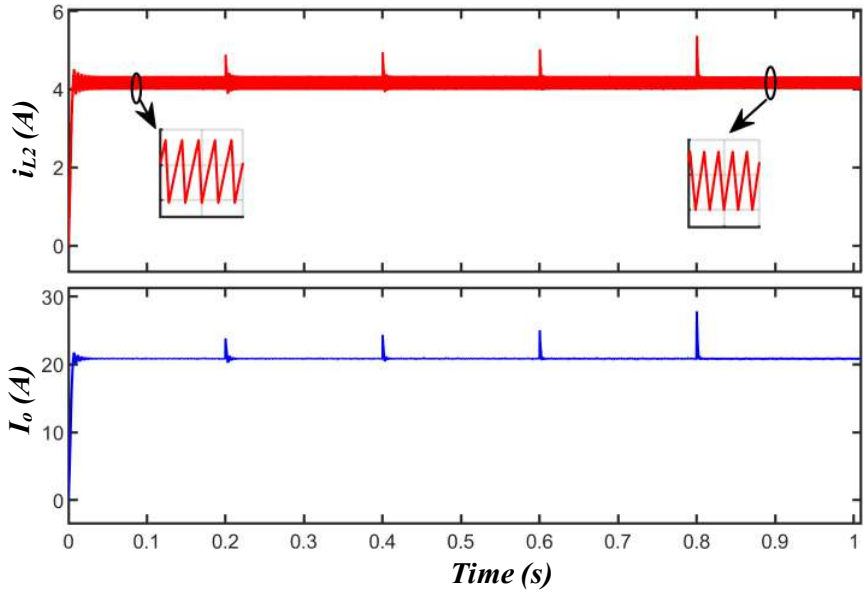


Fig 4.40 Simulation results for load resistance variation from 16 Ω to 7.5 Ω

4.3 Conclusions

This chapter investigated several control strategies to control the output voltage of both ideal and non-ideal DC-DC converters. The process of controller design started using the enhanced transfer functions gained in the last chapter

First, the desired phase margin drove the development of a PI controller. Simulation findings showed that although the PI controller produced longer settling periods and greater overshoots, it efficiently controlled the output voltage. Later on, a PI-led controller was developed with an algorithm for parameter adjustment to handle these problems. The controller showed enhanced performance by decreasing both the settling time and overshoots. Nevertheless, when the gain crossover frequencies were

increased, the PI-lead controller caused the output voltage to be affected by noise, as shown by the simulation results.

Ultimately, creating closed-loop control systems for both ideal and non-ideal Cuk converters necessitates thoughtful deliberation regarding the types of controllers and tuning methods to employ. The PI controller offers a standard level of regulation, but it is prone to experiencing noticeable overshoots and delays in settling time. The PI-lead controller improves performance by minimising overshoots and settling times, although it does introduce some noise at higher frequencies. Thus, it is crucial to adopt a well-rounded strategy that maximises both stability and performance. Future work could explore advanced control strategies to address noise concerns while ensuring rapid and precise voltage regulation.

CHAPTER 5
SLIDING MODE CONTROL OF CUK CONVERTER

5.1. Introduction

In control theory, there's a shift towards stronger and more flexible methods, showcased by the emergence of Sliding Mode Control (SMC). This approach is quite different from older control techniques often talked about before in this thesis, which mostly relied on transfer functions. While these traditional methods are crucial for understanding linear systems, they face challenges when dealing with systems that are inherently nonlinear, like DC-DC converters. The non-linearity of these systems makes things more complicated, causing traditional control strategies to struggle in ensuring effective management and resulting in performance shortcomings.

One of the primary shortcomings of these earlier approaches lies in their assumption of linearity and time-invariance, which fails to hold true in the face of the dynamic and nonlinear nature of many real-world systems. This discrepancy can result in reduced control accuracy and reliability due to the sensitivity of these methods to parameter variations and external disturbances. Additionally, the traditional techniques often do not adequately address the high switching frequencies characteristic of modern power electronics, which can result in less-than-optimal performance and responsiveness.

Against this backdrop, Sliding Mode Control presents itself as a highly effective alternative, specifically engineered to tackle the complexities of nonlinear systems. SMC distinguishes itself through a robust design that is inherently insensitive to system parameter variations and external disruptions. This resilience is achieved through a unique control strategy that forces the system states to conform to a specifically defined sliding surface, ensuring optimal operation despite the presence of disturbances or system parameter changes.

The process of designing a sliding mode control system involves several carefully orchestrated steps. Initially, it necessitates the definition of a sliding surface – a critical component that represents the desired state trajectory of the system. This surface is

judiciously designed to ensure that, once the system's state reaches it, the system will continue to evolve within this prescribed dynamic regime. Following this, the development of a reaching law is essential. This law outlines the control actions required to drive the system's state to the sliding surface in finite time, starting from any initial condition. The final step involves the actual implementation of the control law, which includes the activation of the control inputs necessary to maintain the system's state on the sliding surface, thus ensuring the desired system behaviour.

The advantages offered by Sliding Mode Control are manifold and significant. Most notably, its robustness to various types of disturbances and insensitivity to system parameter variations guarantee a high degree of reliability and performance consistency across a wide range of operating conditions. This makes SMC particularly suited for applications involving complex, nonlinear systems where traditional control strategies falter. Moreover, the ability of SMC to cope with high switching frequencies endows it with remarkable responsiveness and efficiency, further solidifying its position as a preferred control strategy in contemporary engineering challenges

In conclusion, Sliding Mode Control stands out as a sophisticated control strategy that effectively addresses the limitations encountered by traditional transfer function-based methods, especially in the context of nonlinear systems. Through its robust and adaptive design philosophy, encapsulated in the steps of defining a sliding surface, developing a reaching law, and implementing a control law, SMC offers a compelling advantage in terms of performance reliability and robustness against disturbances and uncertainties. As such, it represents a pivotal advancement in control theory, offering enhanced capabilities for managing the complexities of modern engineering systems.

5.2 Cuk Converter

The schematic of an ideal Ćuk converter features a unique configuration with two inductors, a diode, an output capacitor, and a switch, such as a transistor, to facilitate both step-up and step-down voltage regulation while providing an inverted output. The inclusion of two inductors supports efficient energy storage and transfer, and the output capacitor smooths the supply to maintain stable voltage levels at the load. The switch is operated with the duty cycle d and switching frequency f_s

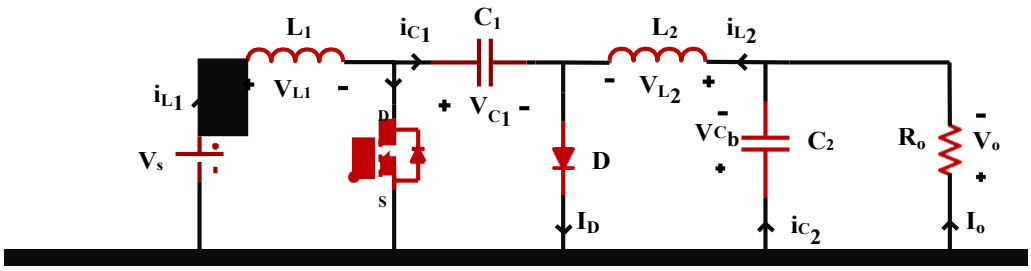


Fig 5.1 Schematic Diagram of Ideal Cuk Converter

5.2.1 Dynamic Equations of CUK Converter

In the continuous conduction mode (CCM) of operation, the Ćuk converter navigates through two primary switching states as discussed below:

Interval I: Interval 1 of the Cuk converter operation, as shown in Fig.5.3(a), the switch S is closed, and the input voltage is delivered to the inductor L_1. This causes the input current to pass through inductor L_1, resulting in a gradual and steady increase in the current across L_1. During this stage, diode D maintains a reverse bias, allowing the transmission of energy stored in coupling capacitor C_1 to output capacitor C_2 and the load through inductor L_2. Thus,

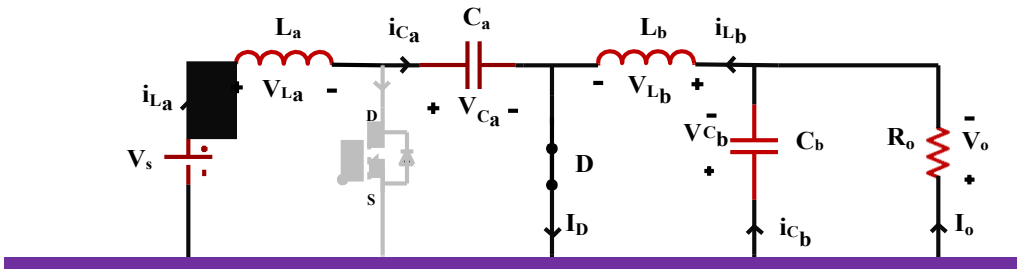
$$V_{L_1}(t) = L_1 \frac{d\ddot{\imath}_{L_1}(t)}{dt} = V_s(t) \tag{5.1}$$

$$V_{L_2}(t) = L_2 \frac{d\ddot{\imath}_{L_2}(t)}{dt} = V_{C_1}(t) - V_{C_2}(t) \tag{5.2}$$

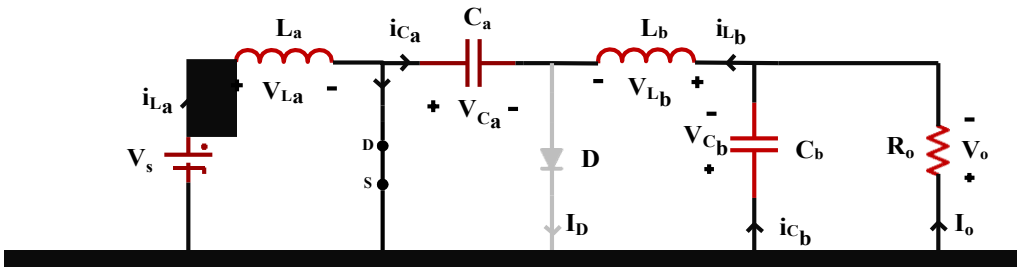
$$\ddot{\imath}_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = -\ddot{\imath}_{L_2}(t) \tag{5.3}$$

$$\ddot{\imath}_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = \ddot{\imath}_{L_2}(t) - \frac{V_{C_2}(t)}{R_o} \tag{5.4}$$

$$V_o(t) = V_{C_2}(t) \tag{5.5}$$



(a)



(b)

Fig 5.2 Mode of Operation (a) Interval I (b) Interval II

Interval II: During Interval 2, as shown inf Fig.2(b) the switch S is in an open position, causing the inductor L_1 to be connected in series with the coupling capacitor C_1. At the same time, the diode D is in a forward-biased condition. This arrangement enables the efficient transfer of energy from the L_1 storage to the C_1 storage, while simultaneously transferring the energy from the L_2 storage to both the output capacitor C_2 and the load. During this interval we have:

$$V_{L_1}(t) = L_1 \frac{d\ddot{\imath}_{L_1}(t)}{dt} = V_s(t) - V_{C_1}(t) \tag{5.6}$$

$$V_{L_2}(t) = L_2 \frac{d\ddot{\imath}_{L_2}(t)}{dt} = -V_{C_2}(t) \tag{5.7}$$

$$\ddot{\imath}_{C_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} = -\ddot{\imath}_{L_1}(t) \tag{5.8}$$

$$\ddot{\imath}_{C_2}(t) = C_2 \frac{dV_{C_2}(t)}{dt} = \ddot{\imath}_{L_2}(t) - \frac{V_{C_2}(t)}{R_o} \tag{5.9}$$

$$V_{OO}(t) = V_{C_2}(t) \tag{5.10}$$

The equations governing the dynamics when the switch is turned on and off can be merged in the following manner:

$$\frac{di_{L_1}(t)}{dt} = \frac{1}{L_1}\left(V_s(t) - \bar{d}V_{C1}(t)\right) \tag{5.11}$$

$$\frac{di_{L_2}(t)}{dt} = \frac{1}{L_2}\left(dV_{C1}(t) - V_o(t)\right) \tag{5.12}$$

$$\frac{dV_{C_1}(t)}{dt} = \frac{1}{C_1}\left(\bar{d}i_{L1}(t) - di_{L2}(t)\right) \tag{5.13}$$

$$\frac{dV_{C_2}(t)}{dt} = \frac{1}{C_2}\left(i_{L2}(t) - \frac{V_o(t)}{R_o}\right) \tag{5.14}$$

Where $\bar{d} = 1 - u$ and represents a binary switching signal that takes the value of 1 when the switch is on, and 0 when it is off.

5.3 Design of sliding mode control for Cuk converter

The design of a sliding mode control for a Cuk converter represents a structured approach to managing its performance through two distinct, yet interrelated, control loops. The block diagram delineated in Fig. 5.3 demonstrates the ingenuity behind this scheme, consisting of an outer voltage control loop and an inner current control loop. The outer loop utilizes a Proportional-Integral (PI) controller to manage the voltage, ensuring that the output consistently aligns with the desired setpoint through corrective adjustments that mitigate both steady-state and transient errors. Alternatively, the inner loop makes use of a sliding mode controller, a robust technique known for its outstanding disturbance rejection properties and strong resilience in the face of system parameter variations .

In particular, for the Cuk converter's sliding mode control, the primary inductor current (iL1) and the output voltage (vo) are selected as the controlled state variables. These variables are continuously monitored, and their real-time values are fed back into the control system. This feedback mechanism enables the system to dynamically adjust and maintain the output voltage within specified tolerances. By sensing and instantly responding to fluctuations in iL1 and vo, the sliding mode controller within the inner current loop can swiftly counteract any disruptions, providing stabilized converter behaviour and enhanced reliability in the delivered power quality.

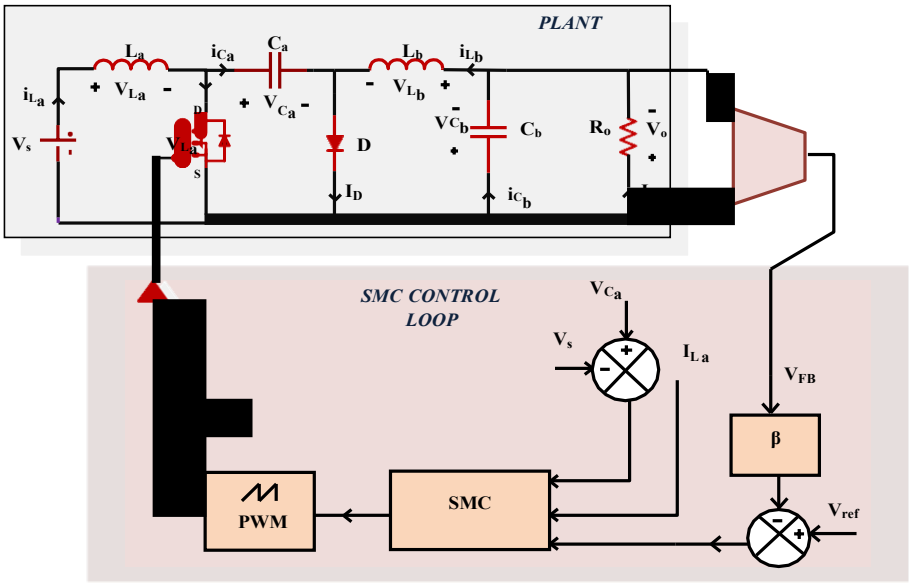


Fig 5.3 Block diagram for sliding mode control of Cuk Converter

a) Outer voltage loop controller: The primary function of the outer voltage loop within a Cuk converter control system is to mitigate and ideally eliminate the steady-state error in the output voltage. To achieve this level of precision and stability, a Proportional-Integral (PI) controller is strategically incorporated into the loop. The workings of a PI controller make it exceptionally suited for this task, as it combines the immediate responsiveness of proportional control to output voltage deviations with the integral action's ability to diminish residual steady-state errors over time. The output from this PI controller doesn't directly modify the converter's settings. Instead, it provides a reference target for the primary inductor current (i_{rerr}).

$$i_{rerr} = K_{prop}e(t) + \int K_{int}e(t)dt \tag{5.15}$$

$$e(t) = V_{rerr} - \beta V_o \tag{5.16}$$

This reference serves as a bridge between the desired output voltage stabilization objectives and the dynamic operational adjustments executed by the inner current control loop.

b) Inner current loop controller: The inner current loop's purpose is fundamentally distinct from that of the outer voltage loop, focusing on regulating the actual inductor current (i_{L_1}) to match a predetermined reference current (i_{rerr}), which has been set by the outer loop. This is where the choice of a sliding mode controller becomes pivotal.

By continuously comparing the actual and reference inductor currents, the controller dynamically adjusts the semiconductor switches' states within the converter. It employs a specifically defined sliding surface to discern the optimal moments for toggling these switches, thereby ensuring that the actual inductor current consistently aligns with its reference. This process not only supports the outer loop's voltage stabilization goal but also enhances the overall efficiency and performance reliability of the Cuk converter by maintaining precise current control under varying load conditions.

5.3.1 Defining of Control equivalent model

Sliding mode control functions by altering the system's dynamics to forcefully drive the system's state to a predefined sliding surface, and then maintains it on this surface despite disturbances or uncertainties in the system. The sliding surface is crucial as it defines the desired system behaviour in the control process. Choosing an appropriate sliding surface is essential for ensuring robust performance and stability of the overall control system, making it responsive to changes and disturbances in a predictable manner. To achieve this control, sliding mode control switches between different control laws, aiming for precision and reliability in reaching the system's desired state. The establishment of an optimal sliding surface is a pivotal step, as it not only dictates the path towards the target state but also significantly influences the system's response time and efficiency. This careful selection ensures the system navigates through disturbances with minimal deviation from its course, underscoring the importance of tailoring the sliding surface to the system's specific needs and characteristics.

Deriving a simplified equivalent control rule requires obtaining a control-oriented model, which is fundamental. This model represents the error dynamics of the DC-DC Cuk converter while it is working in Continuous Conduction Mode (CCM).

Sliding-mode current control involves the selection of a certain reference current signal, i_{rerr} to guide the operation of the system as follows:

$$i_{rerr} = K_c\,(V_{rerr} - \beta V_o) \tag{5.17}$$

For developing the control-centric model of the DC-DC Cuk converter, selecting the appropriate control state variables is crucial. In this context, the control state variable is identified as:

$$x_1 = i_{rerr} - i_{L_1} \tag{5.18}$$

$$x_2 = \int (V_{rerr} - \beta V_o) dt \tag{5.19}$$

$$x_3 = \int x_1 dt \tag{5.20}$$

$$x_4 = \int x_2 dt \tag{5.21}$$

The system under consideration includes four state variables, namely(x_1, x_2, x_3 and x_4), which serve distinctive purposes in representing the system's dynamics. The variable (x_1), is responsible for capturing the discrepancy in the input inductor current from its desired value. Meanwhile, (x_2) is the cumulative sum, or integral, of the difference in the output voltage from its intended target, offering a sense of how this error evolves over time.

Delving further, (x_3) represents the integral of (x_1), which could be seen as a secondary measure of the current error's long-term behavior. (x_4)extends this concept by being the integral of (x_2)effectively becoming the double-integral of the output voltage error. The significance of (x_4) lies in its role in the control system— it is instrumental in addressing and mitigating any persistent discrepancy in the output voltage, thereby working to secure a steady-state output with minimal error.

In reference to source [1], it's articulated that a switched power converter's ideal model, as captured in equation (5.4-5.14), can be accurately depicted through these control state variables. These variables encapsulate the converter's control dynamics, offering a precise representation that's essential for effective management and control of the system's behaviour as shown below:

$$\dot{x_1} = -K_c \beta \frac{dV_o}{dt} - \frac{di_{L_1}}{dt} \tag{5.22}$$

$$\dot{x_2} = V_{rerr} - \beta V_o \tag{5.23}$$

$$\dot{x_3} = i_{rerr} - i_{L_1} \tag{5.24}$$

$$\dot{x_4} = \int V_{rerr} - \beta V_o \tag{5.25}$$

In alignment with averaging theory, the control-oriented model of the DC-DC Cuk converter, as derived from Eqn. (5.11) -(5.14), is delineated by the following equation:

$$\dot{x_1} = -\frac{K_c \beta i_{C_2}}{C_2} - \frac{\blacklozenge V_s - V_{C_1} \underline{D} \blacklozenge}{L_1} \tag{5.26}$$

$$\dot{x_2} = V_{rerr} - \beta V_o \tag{5.27}$$

$$\dot{x_3} = i_{rerr} - i_{L_1} \tag{5.28}$$

$$\dot{x_4} = \int V_{rerr} - \beta V_o \tag{5.29}$$

5.3.2 Derivation of equivalent control law

The application of sliding mode control (SMC) to ćuk converters necessitates a well-designed switching control input to achieve the essential hitting condition. Initially, determining an adequate sliding surface is a crucial step in a practical smc implementation as shown below:

$$\epsilon\epsilon(x) = m_1 x_1 + m_2 x_2 + m_3 x_3 + m_4 x_4 \tag{5.30}$$

Where $m_1, m_2, m_3 \; and \; m_4$ are sliding coefficients.

To meet the criteria outlined in reference [1], a control input that operates through switching mechanisms must fulfil a specific requirement, known as the hitting condition. This condition is essential for the control strategy to be effective, ensuring that the system's response aligns with predetermined performance parameters. To fulfil this condition, the control input is manipulated to induce a switching action, guiding the system towards the sliding surface as described by equation:

$$d_{eq} = \frac{1}{2}(1 + sign(\epsilon\epsilon)) \tag{5.31}$$

According to the hitting condition in SMC, the derivative of the sliding surface $(\epsilon\epsilon(x))$ along the system trajectories should be zero or negative definite, formally expressed as:

$$\dot{\epsilon\epsilon}(x) = m_1 \dot{x_1} + m_2 \dot{x_2} + m_3 \dot{x_3} + m_4 \dot{x_4} \tag{5.32}$$

In accordance with the principles of invariance, the error dynamics associated with the dc-dc Cuk converter are reduced to zero upon reaching the sliding surface. The

following step entails the integration of the model, which is averaged and tailored towards control objectives, into Eqn. (5.30). This integration facilitates a deeper insight into the converter's performance when subjected to the defined operational conditions.

$$m_1 \left(-\frac{K_c \beta}{C_2} i_{C_2} - \frac{V_s - V_{C_1} d_{eq}}{L_1} \right) + m_2 \left(V_{rerr} - \beta V_o \right) + m_3 \left(\dot{V}_{rerr} - i_{L_1} \right) \quad (5.33)$$

$$+ m_4 \left(\int (V_{rerr} - \beta V_o) dt \right) = 0$$

During the steady-state operation, the average current through the capacitor, is effectively zero. Moreover, this element does not substantially influence the sliding-mode control approach, especially when compared with the impact of other control state variables. Therefore,

$$m_1 \left(-\frac{V_s - V_{C_1} d_{eq}}{L_1} \right) + m_2 \left(V_{rerr} - \beta V_o \right) + m_3 \left(\dot{V}_{rerr} - i_{L_1} \right) \quad (5.34)$$

$$+ m_4 \left(\int (V_{rerr} - \beta V_o) dt \right) = 0$$

In a Cuk converter, the switching control input (u) typically involves the alternation between two state scenarios—engaging and disengaging the switch, contingent on the status of $\epsilon\epsilon(x)$. This leads to the expression of the control law as:

$$d_{eq} = \frac{1}{V_{C_1}} \left(V_{C_1} - V_S \right) - K_c I_{L_1} + K_{prop} \left(V_{rerr} - \beta V_o \right) \quad (5.35)$$

$$+ K_{int} \left(\int \left(V_{rerr} - \beta V_o \right) dt \right))$$

Where $K_c, K_{prop}, K_{int} = \frac{m_3}{m_1}, \frac{K_c m_3 + m_2}{m_1} L_1, \frac{m_4}{m_1} L_1$

5.3.3 Existence and stability conditions

In sliding mode control (SMC), a critical prerequisite for achieving desired dynamic and steady-state performance involves ensuring the closed-loop system attains and retains sliding mode (SM) operation. One vital requirement in this context is the hitting condition, which guarantees that the system's state trajectory invariably approaches the sliding surface, regardless of the starting conditions. For the Cuk converter specifically, the hitting condition is effectively met by appropriately defining the

sliding surface.

5.3.3.1 Hitting Conditions

The hitting condition is pivotal as it ensures that regardless of initial discrepancies, the system state trajectory consistently aligns towards the predefined sliding surface. This is crucial for the control system to engage effectively. Ina Cuk converter using SMC, the hitting condition is fulfilled by determining a sliding surface that governs the switching behaviour as shown below:

$$u = \begin{cases} 1, ffor\ S > 0 \\ 0, ffor\ S < 0 \end{cases} \tag{5.36}$$

Setting the control variable (u) to 1 when the sliding variable ($\epsilon\epsilon$) is positive ($\epsilon\epsilon > 0$) and to 0 when negative ($\epsilon\epsilon < 0$) This methodical switching ensures that the system's trajectory steers back to the desired path, a necessity for maintaining control accuracy.

5.3.3.2 Existence Condition

The existence condition, meanwhile, complements the hitting condition by ensuring that once the system's trajectory reaches the sliding surface, it stays there despite any system disturbances or parameter variations. This condition is essential for the robustness of SMC, as it maintains the desired system behavior under diverse operational conditions and external influences, ultimately enhancing system stability and performance reliability.

The local reachability condition is mathematically expressed as the product of the sliding function $\epsilon\epsilon(x)$ and its time derivative ($\epsilon\dot{\epsilon}(x)$) being negative definite. So, the existence condition can be written as:

$$\lim_{g\to 0} \epsilon\epsilon\dot{\epsilon} < 0 \quad \begin{cases} \epsilon\epsilon < \cup, \epsilon\epsilon > \cup \\ -\epsilon\dot{\epsilon} > 0. \epsilon\epsilon < 0 \end{cases} \tag{5.37}$$

Differentiating $\epsilon\epsilon(x)$ with respect to time, we get,

$$K_{prop}V_{rerr} - \beta V_o - K_c i_{L_1} + K_{int} x_2 < V_S \tag{5.38}$$

$$K_{prop}V_{rerr} - \beta V_o - K_c i_{L_1} + K_{int} x_2 > V_S - V_{C_1} \tag{5.39}$$

5.3.3.3 Stability conditions

In the study of sliding mode control for power electronics, particularly in the context of Cuk converters, stability criteria play a critical role in ensuring reliable operation. At the heart of sliding mode control lies the principle of guiding system state

trajectories towards a predefined equilibrium point, ensuring that the system's response remains predictable and robust against perturbations

Focusing on the Cuk converter, a popular choice for its efficiency in converting DC voltage levels, we define its operation in terms of steady-state values: V_s (input voltage), V_o (output voltage), V_{C_1}(voltage across the energy transfer capacitor), i_{L_1} (current through the input inductor), i_{L2} (current through the output inductor), and R_o (value of the load resistor). These parameters anchor our analysis, setting the stage for scrutinizing the converter's behaviour under closed-loop control.

$$V_{C_1} = V_S + V_o \tag{5.40}$$

$$I_{L_2} = i_{L_2,avaa} = \frac{V_o}{R_o} \tag{5.41}$$

$$I_{L_1} = i_{L_1,avaa} = \frac{V_o^2}{V_s R_o} \tag{5.42}$$

To achieve stability and desirable performance, one integrates the equivalent control law into a simplified model of the Cuk converter operating in Continuous Conduction Mode (CCM) as shown below:

$$\frac{di_{L_1}(t)}{dt} = \frac{1}{L_1}(V_s(t) - dV_{C_1}(t)) \tag{5.43}$$

$$\frac{di_{L_2}(t)}{dt} = \frac{1}{L_2}(dV_{C_1}(t) - V_o(t)) \tag{5.44}$$

$$\frac{dV_{C_1}(t)}{dt} = \frac{1}{C_1}(di_{L_1}(t) - di_{L_2}(t)) \tag{5.45}$$

$$\frac{dV_{C_2}(t)}{dt} = \frac{1}{C_2}(i_{L_2}(t) - \frac{V_o(t)}{R_o}) \tag{5.46}$$

The ideal closed-loop Cuk converter dynamics in (17) can be linearized around the equilibrium point, which gives:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \\ \dot{x}_5 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} \tag{5.47}$$

The Jacobian matrix is given as :

$$M_{jjac} = \begin{bmatrix} -\frac{K_c}{L_1} & 0 & 0 & \frac{K_{pppop}\beta}{L_1} & -\frac{K_{jint}\beta}{L_1} \\ \frac{K_c V_o}{V_s R_o C_1} + \frac{V_s}{C_1 V_{CC_1}} & 0 & -\frac{V_o}{C_1(V_s+V_o)} & -\frac{K_{pppop}\beta}{V_s R_o C_1} & -\frac{K_{jint}\beta}{V_s R_o C_1} \\ -\frac{K_c}{L_2} & \frac{1}{L_2} & 0 & -\left(\frac{K_{pppop}\beta}{L_2} + \frac{1}{L_2}\right) & -\frac{K_{jint}\beta}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{R_o C_2} & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \quad (5.48)$$

The characteristic equation of the Jacobian matrix is given by:

$$s^5 + K_1 s^4 + K_2 s^3 + k_3 s^2 + K_4 s + K_5 = 0 \quad (5.49)$$

where,

$$\begin{aligned} P_1 &= -(j_{11} + j_{44}) \\ P_2 &= j_{11}j_{44} - j_{23}j_{32} - j_{34}j_{43} \\ P_3 &= -j_{35}j_{43} + j_{11}j_{23}j_{32} + j_{11}j_{34}j_{43} - j_{14}j_{31}j_{43} + j_{23}j_{32}j_{44} - j_{24}j_{32}j_{43} \\ P_4 &= j_{11}j_{35}j_{43} - j_{15}j_{31}j_{43} - j_{25}j_{32}j_{43} - j_{11}j_{23}j_{32}j_{44} + j_{11}j_{24}j_{32}j_{43} \\ &\quad - j_{14}j_{21}j_{32}j_{43} \\ P_5 &= j_{11}j_{25}j_{32}j_{43} - j_{15}j_{21}j_{32}j_{43} \end{aligned} \quad (5.50)$$

For the DC-DC Cuk converter operating under closed-loop conditions, achieving stability around its equilibrium point is crucial. This stability is ensured when all the Eigenvalues from the Jacobian Matrix have negative real parts. In simpler terms, this means that the system will naturally settle into a stable state over time if these conditions are met. Utilizing the Routh–Hurwitz stability criterion, we can further define these stability conditions. By applying this criterion to equation (20), we obtain specific conditions that underpin the converter's stable operation. This approach offers a clear path to verify the system's robustness and its ability to maintain consistent performance:

$$\begin{aligned} K_1 &> 0 \\ K_2 &> \frac{K_3}{K_1} \end{aligned} \quad (5.51)$$

$$K_3 > \frac{K_1K_4 - K_5}{K_2 - \frac{K_3}{K_1}}$$

$$K_4 > \frac{K_4\left(\frac{K_5}{K_1} + K_2 K_2 - \frac{K_3}{K_1}\right)}{2K_5 - K_1K_4 + K_3\left(K_2 - \frac{K_3}{K_1}\right)}$$

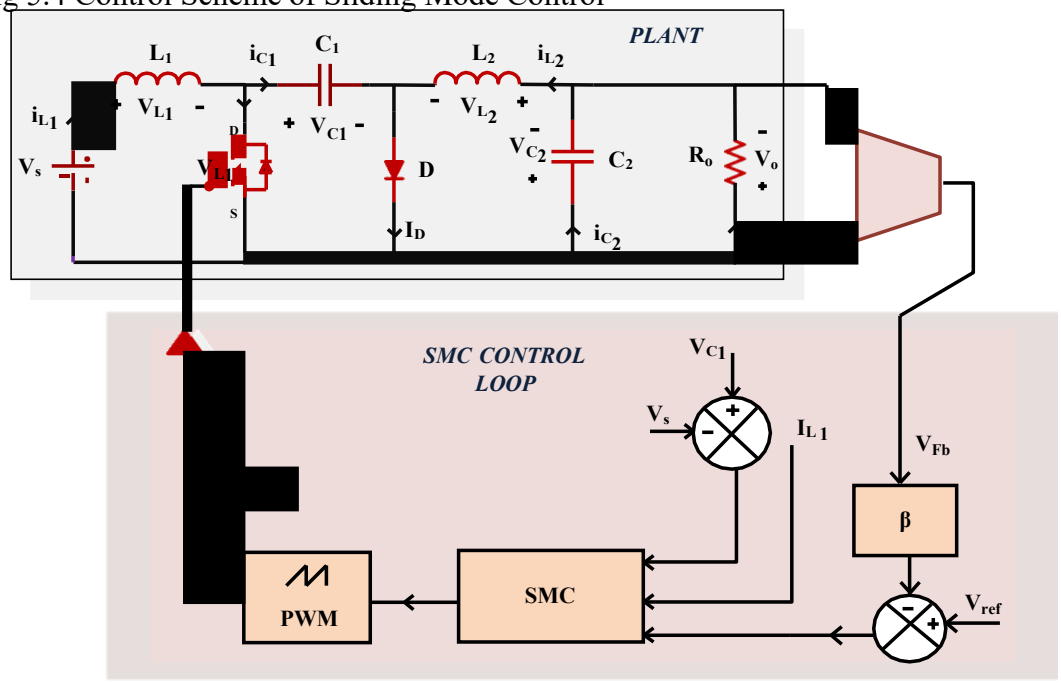
$$K_5 > 0$$

Thus, Eqn. (5.51) can be solved numerically to determine the controller gains that guarantee the stability of the system.

5.4 Comparison Between A PI Controller and Sliding Mode Controller

In this experiment, a comparative analysis was conducted on stability and transient analysis of CUK converter using two different control methods: Dual Loop PI Control and Sliding Mode Control via MATLAB SIMULINK as shown in Fig.

Fig 5.4 Control Scheme of Sliding Mode Control



5.4.1 Output voltage comparison

Fig. 6 illustrates the comparative analysis of output voltage between Cuk DC-DC converter employing dual-loop PI control and Sliding Mode Control (SMC). With a

66.66% duty cycle, both control settings maintained a stable output of 48V. However, significant differences were evident in their dynamic responses. The Sliding Mode Control exhibited a superior performance with a quicker settling time of 77ms, compared to the 130ms of the Dual Loop PI Control, indicating a faster system response. Furthermore, it achieved a notably lower maximum peak overshoot at 0.6%, whereas the Dual Loop PI Control recorded a higher overshoot of 1.5%. These results highlight the Sliding Mode Control's enhanced stability and efficiency in managing the Cuk converter's output voltage.

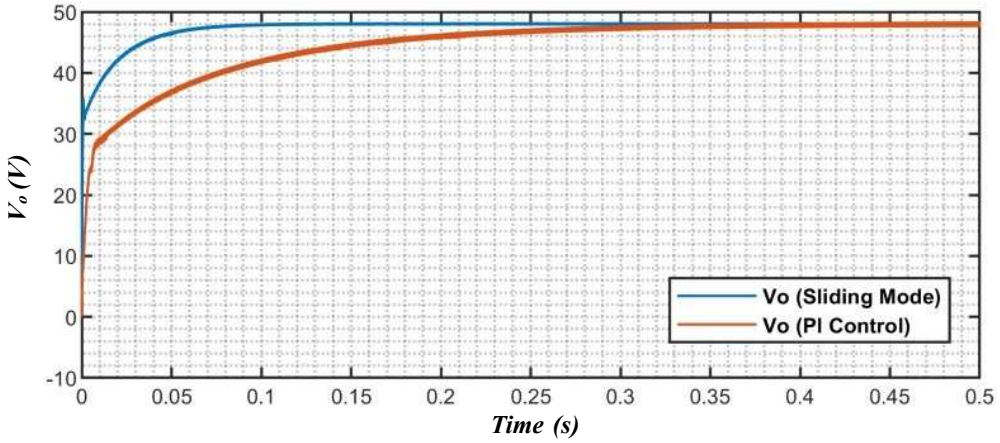
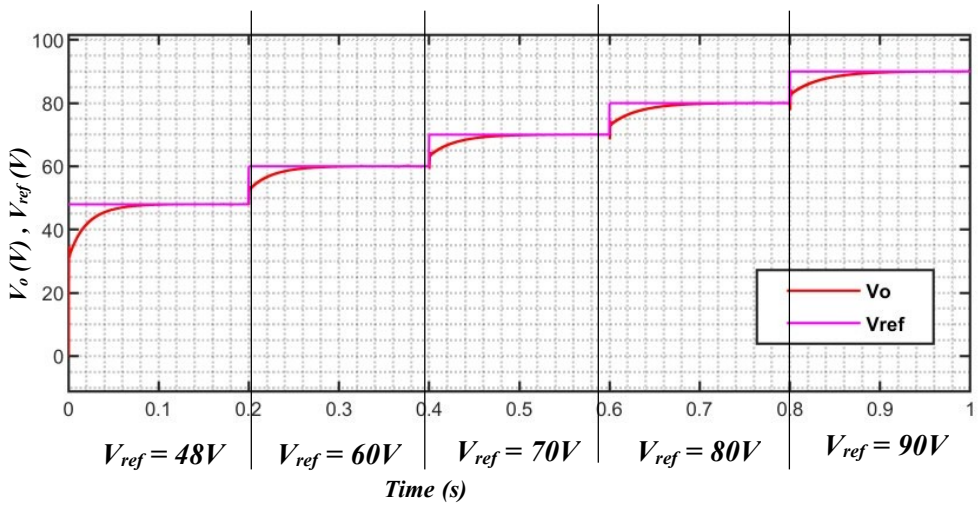


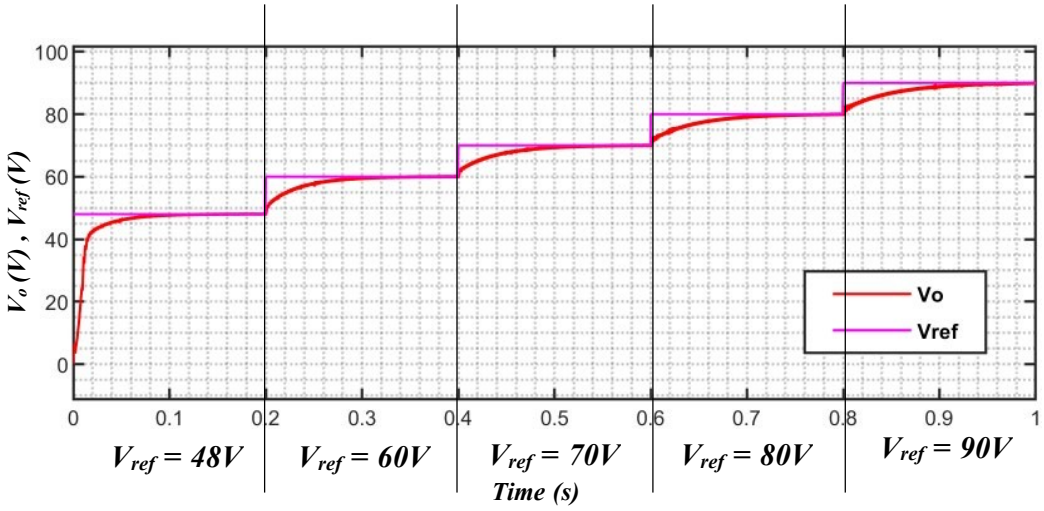
Fig 5.5 Output Voltage Comparison between Sliding Mode Control and PI Control

5.4.2 Reference voltage tracking

The reference voltage tracking performance was evaluated for Cuk converters under dual-loop PI control and Sliding Mode Control (SMC) in Fig.7. The reference voltage was dynamically changed in steps, starting from 48V, and incrementing up to 90V. The Sliding Mode Control exhibited exceptional precision with a small steady-state error of 0.14%, implying a superior capability in maintaining output voltage with high accuracy across the given range. Conversely, the Dual Loop PI Control, though effective, showed less precision with a steady-state error of 0.3%.



(a)

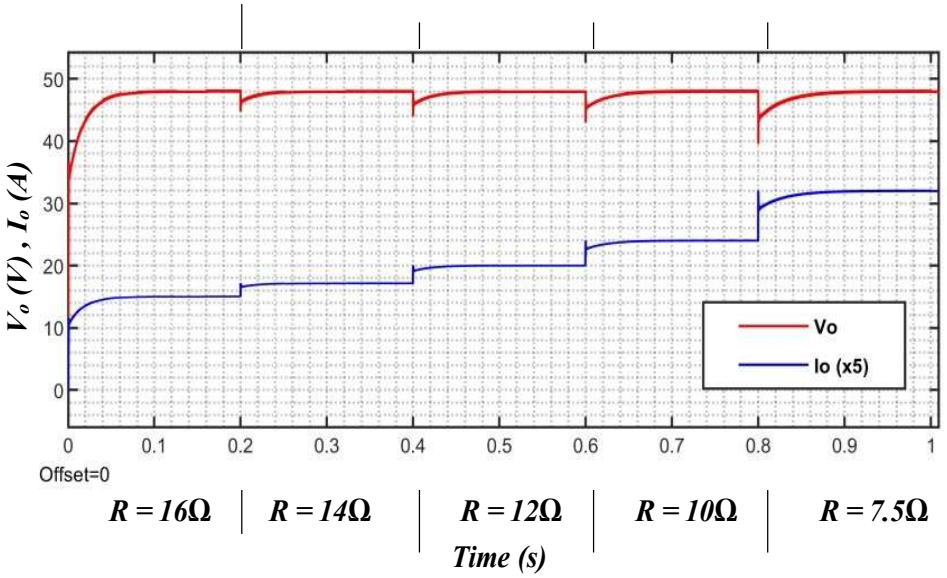


(b)

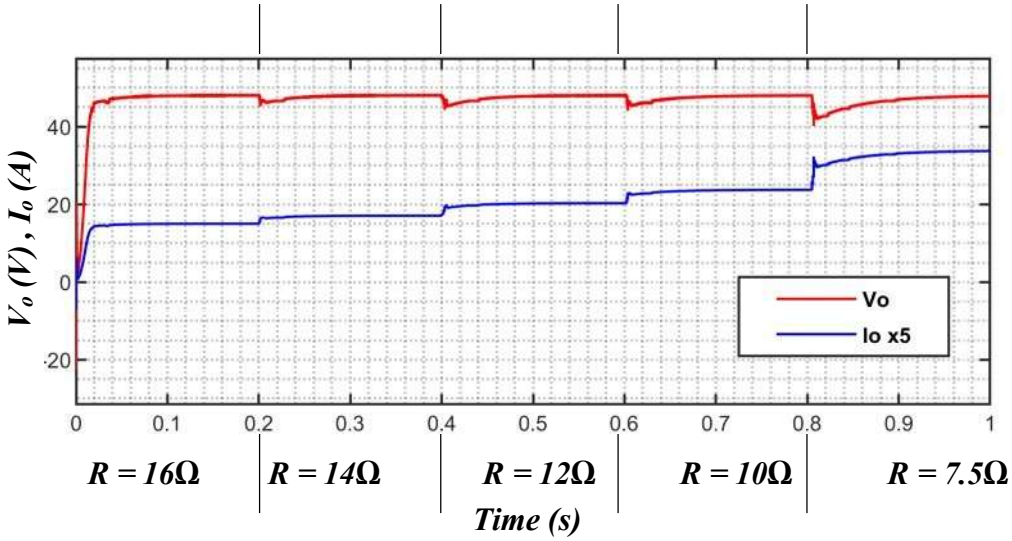
Fig 5.6 Reference Voltage tracking for : (a) SMC control (b) PI Control

5.4.3 Load Variation Transients

The Fig.8 shows the load variation response in a Closed Loop Cuk Converter, illustrating the ability of both Dual Loop PI Control and Sliding Mode Control to maintain a stable output voltage of 48V.However, while Dual Loop PI exhibits some ringing and oscillations upon load change from 16 ohms to 7.5 ohms, Sliding Mode Control demonstrates a clean, stable output without such disturbances. This visual evidence points to Sliding Mode Control's enhanced stability during load fluctuations.



(a)



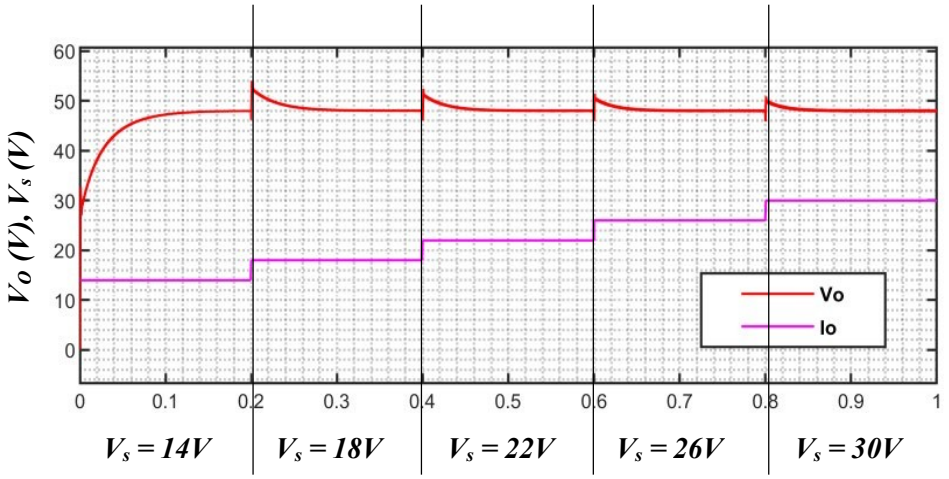
(b)

Fig 5.7 Response of the Cuk converter under step variation of the load Resistance (a)SMC Control (b) PI Control

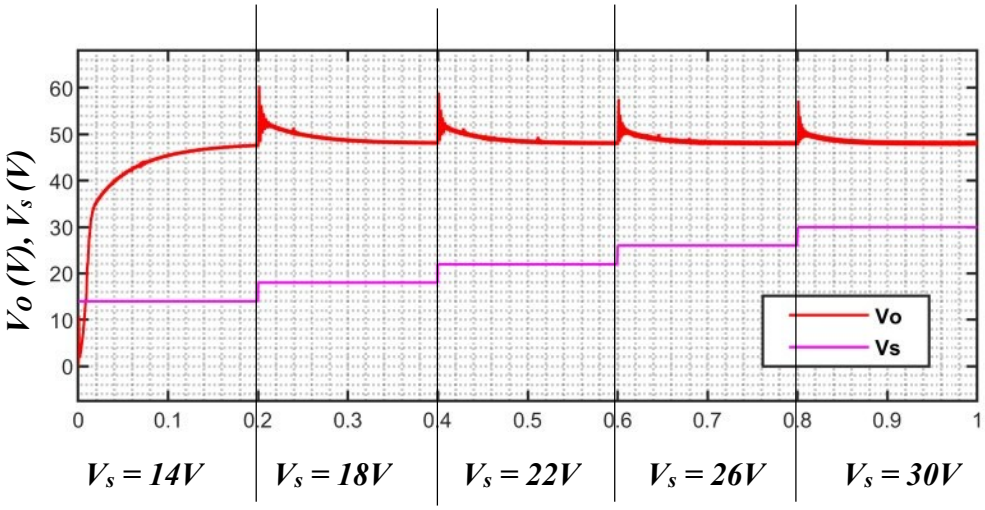
5.4.4 Input voltage variation transients

Fig.9 shows a Closed Loop Cuk Converter that experiences input voltage fluctuations ranging from 14V to 30V. Both Dual Loop PI Control and Sliding Mode Control successfully maintained a stable output of 48V.However, at lower voltages, the PI Control suffered from a 25% overshoot with significant ringing, while the Sliding Mode Control exhibited a more controlled 12% overshoot and quickly stabilized to

48V. This demonstrates the superior efficiency of Sliding Mode Control in handling input voltage fluctuations with minimal disturbances.



(a)



(b)

Fig 5.8 Response of the Cuk converter under step variation of the Line Voltage (a) SMC control (b) PI Control

5.5 Conclusions

The performance attributes of the Closed Loop Cuk Converter using Dual Loop PI Control and Sliding Mode Control are highlighted through a comparison under varying input voltage, load, and reference voltage tracking conditions. Sliding Mode Control demonstrated reduced overshoot and minimal disturbance in comparison to PI Control at lower input voltages. During load and line fluctuations, Sliding Mode Control

exhibited an improved reaction in maintaining the 48V output, characterized by reduced oscillations and faster settling time.

Furthermore, when it comes to tracking a reference voltage, Sliding Mode Control has demonstrated superior accuracy and speed, effectively adapting to rapid fluctuations in reference signals. Sliding Mode Control consistently shows better stability than PI Control under changing conditions.

The Cuk converter stands out among other 4th Order converters like the SEPIC and Zeta, chiefly because it ensures continuous currents at both input and output, which lessens electromagnetic interference (EMI) and boosts efficiency.

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

This thesis has thoroughly investigated the design, mathematical modelling, and control challenges related to both ideal and non-ideal Cuk converters. During the study, it became clear that although ideal models offer fundamental insights and a theoretical framework, practical applications frequently involve addressing the complications presented by non-perfect behaviours. The findings of this research study on design, modelling, and control matters can be succinctly summarized as follows:

1. During the investigation of design-related difficulties, it was discovered that when assuming an optimal converter, the computed duty cycle resulted in a voltage that was lower than anticipated. The decrease in voltage is ascribed to power dissipation across different resistive elements in the converter. In response to this issue, novel and precise equations were constructed to determine the duty cycle of both ideal and non ideal Cuk converters. These calculations consider the typical non-ideal characteristics of converter components. Similarly, the formulas for calculating the dimensions of inductors and capacitors were improved to more accurately accommodate situations where these non-ideal conditions exist. It has been found that non-ideal systems necessitate bigger component values in order to satisfy design specifications. Furthermore, an analysis of the fluctuation in output voltage, known as voltage ripple, was carried out for both ideal and non-ideal systems. The investigation's findings, backed by simulation data, validate the precision of the improved theoretical models, underscoring the significance of accounting for non-ideal component behavior in design calculations.

2. The state-space averaging technique was employed to analyze the relationships between input voltage and output voltage, load current and output voltage, and duty cycle and output voltage for both ideal and non-ideal Cuk converters. A more comprehensive model of the converters was built by considering factors such as equivalent series resistances (ESRs) of inductors and capacitors, as well as the resistances from switches and diodes. This improved the understanding of both the dynamic and steady-state behaviour. It has been found that transfer functions under non-ideal conditions have distinct steady-state and transient tendencies in comparison to their ideal counterparts. The specific non-ideal factors evaluated in this work

showed that the duty cycle to output voltage transfer function, which is crucial for control design, behaved as a minimum phase system. Conversely, assuming perfect conditions, this function typically exhibits non-minimum phase behavior, with zeros located in the right-half plane. This distinction emphasizes that the phase features of the transfer function depend on the individual non-ideal parameters involved, while ideally, it tends to be non-minimum phase. By utilizing these enhanced transfer functions, superior controller designs were accomplished for both the ideal and non-ideal Cuk converters.

3. Using the transfer function models including both non-ideal and ideal components, several control strategies were devised to control the output voltage of both ideal and non-ideal Cuk converters across several operational conditions. For both types of the Cuk converter, the controllers developed were Proportional-Integral (PI), PI-Lead, and a dual-loop PI controller. The PI controller parameters were optimized using the Ziegler-Nicholas technique. Though with more overshoot and longer settling periods, simulation results underlined the PI controller's capacity to manage output voltage under different scenarios. Using this PI controller on a real-world Cuk converter produced similar performance traits. We introduced a PI-Lead controller to improve the converters' performance. Targeting a specified phase margin and gain crossover frequency, an original algorithm was chosen to calibrate the PI-Lead controller's characteristics, so exactly meeting the design specifications. Better settling times and less overshoot followed from this change. As per simulation studies, nevertheless, pushing for a higher gain crossover frequency using the PI-Lead controller caused noise into the output voltage. Therefore, a dual-loop PI control method was used for both the ideal and non-ideal Cuk converters to improve the bandwidth of the system even more without sacrificing performance. This method stabilizing the output voltage combined an inner current PI controller with an outer voltage PI controller. Based on the suggested approach, these controllers' design sought to concurrently achieve the required phase margin and gain crossover frequency. Simulation results showed that this two-loop arrangement exceeded the performance of both the stationary PI and PI-Lead controllers by efficiently improving settling times and minimizing overshoots under different operating situations.

4. In the final section of the thesis, the focus is on the implementation of sliding mode control for the DC-DC Cuk converter. The derivation and study of the transfer functions provided a novel viewpoint in comparison to previous investigations. The calibration of the controller settings was performed using a direct method that was influenced by the Routh-Hurwitz stability criterion. The simulation experiments demonstrated that the effectiveness of the sliding mode control was comparable to that of the two-loop PI control system. Sliding

mode control offers the advantage of just needing to tune a single PI controller, instead of the two controllers required for the two-loop system. Furthermore, this technique eliminates the requirement for a PWM modulator to generate switching signals, simplifying the whole control procedure.

6.2 Future Scope

The research presented in this thesis paves the way for additional exploration and expansion:

1. The methodologies used for the design, modelling, and control of DC-DC buck and Cuk converters can be easily adapted and modified for other types of DC-DC converters.
2. Although the small-signal averaged model used in this thesis provides valuable insights, it falls short in capturing the complete influence of converter switching frequency on system dynamics. Further research could be dedicated to the development of mathematical models that explicitly consider the impact of converter switching frequency.
3. In this thesis, control techniques were developed with the consideration of consistent converter parameters. However, further improvements can be made to these techniques by considering the variations in converter parameters.
4. The control design methodologies developed have great potential for implementation in a wide range of applications, such as battery-operated electric vehicles, photovoltaic systems, DC microgrids, and more. Further exploration of these applications could lead to valuable insights and practical implementations.

LIST OF PUBLICATIONS

1. P. S. Shandilya, A. Gupta and D. Joshi, "Voltage and Current Regulation in Cuk DC-DC Converters having Enhanced Closed-Loop Control using PID Controller," *2023 11th National Power Electronics Conference (NPEC)*, Guwahati, India, 2023, pp. 1-6, doi: 10.1109/NPEC57805.2023.10385025.
2. P. S. Shandilya, A. Gupta. Joshi and Narendra Kumar “Modelling of PID-based Closed-Loop Voltage Mode Control for Cuk Converter with Circuit Parasitics” 2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (IEEE SeFeT 2024) (Accepted)

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