Analytical Modeling, Simulation and Characterization of Junctionless Accumulation Mode MOSFET for Analog and RF Circuit Applications

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

by

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Dedicated to,

My beloved family and my loved ones, without whose endless love and support, I wouldn't have achieve this.

ACKNOWLEDGEMENTS

I am delighted that the day has come that I have completed my research work for my Ph.D. journey and today I am writing my thesis. This Ph.D. journey was very admirable, memorable and knowledgeable for me. Before proceeding towards the work, I would like to express my gratitude and appreciation towards everyone who has been my pillar of strength and support throughout this journey. I feel so blessed and fortunate to have all these people in my life who help me to make this journey a remarkable one.

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CANDIDATE'S DECLARATION

I **Sumedha Gupta** hereby certify that the work which is being presented in the thesis entitled **Analytical Modeling, Simulation and Characterization of Junctionless Accumulation Mode MOSFET for Analog and RF Circuit Applications** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **July'2019 to May'2024** under the supervision of **Prof. Neeta Pandey and Prof. R S Gupta**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

Signature of Supervisor (s) **Signature of External Examiner**

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CERTIFICATE BY THE SUPERVISOR(s)

Certified that **Sumedha Gupta** (Enrollment No.: 2K19/PHDEC/19) has carried out her research work presented in this thesis entitled "**Analytical Modeling, Simulation and Characterization of Junctionless Accumulation Mode MOSFET for Analog and RF Circuit Applications"** for the award of Doctor of Philosophy from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under our supervision. The thesis embodies results of original work and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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Abstract

The persistent demand of the market for area- efficient and low power dissipating devices leads to continuous reduction in device size. It persuades the device engineers to develop such Integrated Circuits (ICs) with less fabrication complexity. Integrated circuit industry has revolutionized over the past few decades. Scaling has lead towards the compactness of these physical devices. The density of the transistors present over the chip doubles itself after every 18 months. This factor of scaling has given rise to many novel structures and devices. But as this dimension enters into nanometer regime, it brings about many difficulties known as Short- Channel Effects (SCEs) and Hot-Carrier Effects (HCEs). SCEs include Drain Induced Barrier Lowering (DIBL) effect, threshold voltage roll- off, velocity saturation effect, etc. These effects can alter the device characteristics severely and needs to be minimized. Therefore, to overcome these complications, several novel device architectures involving device engineering techniques have been proposed to maintain the functioning and capabilities of the device inspite of scaling.

Multiple gate transistors are becoming prevalent these days because of their scaling capabilities, complete depletion of the channel and more control of the gate over the channel region. These structures also help in reduction of the leakage currents and the SCEs to a greater extent. Nowadays, a new structure called Cylindrical Surrounding Gate (CSG) MOSFET has emerged, in which the gate wraps all around the silicon pillar. Thus, provides superior gate controllability, finer scalability, excellent compatibility with Complementary Metal-Oxide-Semiconductor (CMOS) technology, much reduced SCEs, low leakage current and steep Subthreshold Slope (SS). These characteristics make CSG MOSFET as the ultimate short channel device for the future device technology. However, when the device dimensions are extremely scaled (below 22nm technology), higher source/drain resistance is formed due to the formation of abrupt source/drain p-n junctions. This in turn increases the fabrication complexity of the device and therefore, from the fabrication point of view, it is difficult to have control over these metallurgical p-n junctions. Hence, to endure with the future Ultra Large Scale Integration (ULSI) design, progressive changes in the elementary device design needs to be incorporated. A novel device structure called as Junctionless Transistor

(JLT) was then proposed to overcome this problem of the increased source/drain resistance. JLT is uniformly heavily doped throughout the source, channel and drain regions either with n^+- n^+- n^+ or p^+- p^+- p^+. Hence, there is no formation of p-n junctions between the source/drain and the channel regions. Due to elimination of junctions, JLT is easy to fabricate and also offers improved electrical properties. But because of the high doped channel, the mobility of the carriers gets degraded in the JLT. This problem of Carrier Mobility Degradation (CMD) leads to lower drain current and lower transconductance. So, another structure, junctionless accumulation-mode (JAM) MOSFET was introduced. In JAM MOSFET, the channel region's doping is done slightly less than that of source and drain. The carriers get accumulated at the source-channel-drain boundaries similar to an ohmic contact. On account of the higher doping present in the source and drain regions, it avoids high parasitic resistance. Also, due to lower doping present in channel region, it also overcomes the problem of CMD. Thus, provides more conductivity and better characteristics than JLT.

JAM has reduced SCEs but they are still not negligible, so in this research work, techniques of gate metal engineering and gate stack engineering are therefore incorporated in JAM MOSFET and a new structure was proposed named Dual-Metal Gate Stack Engineered JAM-CSG (DMGSE-JAM-CSG) MOSFET. In a MOS device, a high electric field at the drain side causes impact ionization and tunnelling of the carriers, which are responsible for hot- carrier effect. In order to address this problem, high-k gate stack have been implemented in our proposed device architecture. Thus, use of gate stack helps eliminate the problem of leakage currents. Also, the implementation of dual metal gates of different work- functions enhances the gate transport efficiency resulting in excellent gate control, which further leads to high drain current and high transconductance. Hence, our proposed device, DMGSE-JAM-CSG MOSFET possesses better electrical characteristics as compared to the JAM-CSG MOSFET. This has been verified by both using both the analytical and simulation method. 2-D analytical modeling of DMGSE-JAM-CSG MOSFET has also been proposed to address center potential, electric field, subthreshold current, transconductance and various SCEs. Furthermore, the analysis is also done using different high- k gate stack materials. The exactness of this developed model is then established by comparing with the simulated outcomes.

The change in temperature varies the performance of the MOSFET, therefore, it becomes important to examine the impact of temperature upon the various characteristic aspects of the MOSFET. Therefore, to study the influence of temperature on our structure i.e., DMDG-JAM-CSG MOSFET, we have developed this structure's temperature- dependent physics- based analytical model using the applicable boundary conditions. The characterization of the device is also studied at cryogenic temperatures. In addition to this, we have also performed the linearity assessment of our device by determining various figure of merits. Our research also proposes analytical modeling for Junctionless Accumulation-Mode Cylindrical Surrounding Gate (JAM- CSG) MOSFET-based biosensor used for label free electrical detection of the biomolecules (enzymes, cells, DNA, etc.). In this work, non-uniform doping in the channel of DMGAA-JAM-NWFET is also considered and improved characteristics over the uniformly doped channel were observed. Also, the influence of the straggle length parameter and peak doping concentration upon the device behaviour was also examined.

All the device designs discussed above are elaborated in the dissertation. Also, the contribution of the research to the field of Nano Electronics is also discussed herewith.

LIST OF PUBLICATIONS

INTERNATIONAL JOURNALS

1. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Analytical modeling of dual-metal gate stack engineered junctionless accumulation-mode cylindrical surrounding gate (DMGSE-JAM-CSG) MOSFET." *Applied Physics A* 127, no. 7 (2021): 1-10. **DOI:** 10.1007/s00339-021-04652-0 **(SCIE indexed, Impact Factor: 2.584)**

2. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Temperature dependency and linearity assessment of dual-metal gate stack junctionless accumulation-mode cylindrical surrounding gate (DMGS-JAM-CSG) MOSFET." *Physica Scripta* 96, no. 12 (2021): 124055. DOI: 10.1088/1402-4896/ac33fd **(SCIE indexed, Impact Factor: 2.487)**

3. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Analytical model for junctionless accumulation-mode cylindrical surrounding gate (JAM-CSG) MOSFET as a biosensor." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* (2023): e3095. **DOI:** 10.1002/jnm.3095 **(SCIE Indexed**, **Impact Factor: 1.436).**

4. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Modeling of Dual- Metal Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DM-JAM-CSG) MOSFET for Cryogenic temperature Applications." *Microelectronics Journal vol.* 139, (2023). **DOI:** 10.1016/j.mejo.2023.105880 **(SCIE Indexed**, **Impact Factor: 1.992).**

5. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. (2024). "Non-uniform doping dependent electrical parameters of dual-metal gate all around junctionless accumulation-mode nanowire FET (DMGAA-JAM-NWFET)." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 37*(2), e3203, (2024). **DOI:** 10.1002/jnm.3203 **(SCIE indexed, Impact Factor: 1.436)**

INTERNATIONAL CONFERENCES

1. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Investigation of dual-material double gate junctionless accumulation-mode cylindrical gate all around (DMDG-JLAM-CGAA) MOSFET with High-k gate stack for low power digital applications." In *2020 IEEE 17th India Council International Conference*

(INDICON), pp. 1-4. IEEE, 2020. **DOI:** 10.1109/INDICON49873.2020.9342380

2. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Analog Performance of Dual-Metal Gate Stack Architecture of Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSA-JAM-CSG) MOSFET." In *2021 Devices for Integrated Circuit (DevIC)*, pp. 1-5. IEEE, 2021. **DOI:** 10.1109/DevIC50843.2021.9455896

3. **Sumedha Gupta**, Neeta Pandey, and R. S. Gupta. "Comparative study of Compound Semiconductors/Silicon-based Cylindrical Surrounding Dual-Metal Gate Junctionless Accumulation-Mode (CS-DMG-JAM) MOSFET for High Frequency and Switching Applications." In *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)*, pp. 486-490. IEEE, 2022. **DOI:** 10.1109/EDKCON56221.2022.10032896

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A_v	Voltage gain
C_{ox}	Capacitance per unit area
I_{ds}	Drain Current
I_{lin}	Linear Current
I_{sat}	Saturation Current
I_{sub}	Subthreshold Current
N_D^+	Partial Ionization
$S_{I_{ds}}$	Drain Current Sensitivity
V_{EA}	Early Voltage
V_T	Thermal Voltage
k_B	Boltzmann's constant
t_{si}	Substrate's Thickness
ε_{hk}	Dielectric Constants of HfO_2 layer
ε_{ox}	Dielectric Constants of SiO_2 layer
ε_{si}	Dielectric Constant of Si
θ_{short}	Subthreshold Slope Factor
ϕ_{bi}	Built- in Voltage
AM	Accumulation-Mode
BJT	Bipolar Junction Transistor
BTBT	Band-to-Band Tunneling
C_G	gate capacitance
CGAA	Cylindrical Gate All Around
CLM	Channel Length Modulation
CMD	Carrier Mobility Degradation
CMOS	Complementary Metal Oxide Semiconductor
CONMOB	Concentration Dependent Mobility model
CSG	Cylindrical Surrounding Gate
DG	Double Gate
DIBL	Drain-Induced Barrier Lowering

DM-FET	Dielectric Modulated-FET
DMGAA	Dual-Metal Gate All Around
DMGSE	Dual- Material Gate Stack Engineered
DSG	Double Surrounding Gate
E_c	Critical Electric Field
E_D	Ionization Energy of the Donor Dopant
EOT	Effective Oxide Thickness
FET	Field- Effect Transistor
FLDMOB	Field Dependent Mobility Model
FOMs	Figure of Merits
GAA	Gate All Around
g_d	Output Conductance
GIDL	Gate-Induced Drain Leakage
g_m	Transconductance
GME	Gate Material Engineering
HCEs	Hot Carrier Effects
ICs	Integrated Circuits
I_{DSS}	Maximum Drain Current
I_{gidl}	GIDL current
IIP3	Third-order Intercept Input Power
IM	Inversion-Mode
IMD3	Third-order Intermodulation Distortion
I_{ON}	ON current
JAM	Junctionless Accumulation Mode
JLT	Junctionless Transistor
k	Dielectric Constant
L	Channel Length
LGAA	Lateral Gate All Around
LSP	Low Standby Power
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N_D	Channel Doping
N_D**(peak)**	Peak Doping Concentration

N_D^+	Source/Drain Doping
N_f	Charge of the Biomolecules
NWFET	Nanowire FET
PPA	Parabolic Potential Approximation
q	Electronic Charge
RF	Radio Frequency
SCEs	Short- Channel Effects
SELBOX	Selective Buried Oxide
SS	Subthreshold Slope
T	Temperature
t_{bio}	Thickness of the Nanogap Cavity
TG	Tri-Gate
TGF	Transconductance Generation Factor
t_{ox}	Thickness of oxide layer
ULSI	Ultra Large Scale Integration
V_{DD}	drain voltage
V_{ds}	Voltage across Drain and Source
V_{fb}	Flatband Voltage
VGAA	Vertical Gate All Around
V_{GS}	Gate Voltage
VIP2	Second-order Voltage Intercept Point
VIP3	Third-order Voltage Intercept Point
V_p	Pinch-off Voltage
v_s	Saturation Velocity
V_{th}	Threshold Voltage
z	Co-ordinates for Horizontal Axis
ΔV_{th}	Sensitivity of the device
μ	Mobility of the carrier
μ_n	Low- Field Mobility
σ	Straggle Length Parameter
τ	Switching Speed
E	Electric Field

r	Co-ordinates for Vertical Axis
v	Electron Velocity
ΔV_{fb}	Change of the Flat Band Voltage
λ	Characteristic Length
ψ	Potential
$\psi(r,z)$	Potential Distribution
ϕ	Work-function

CHAPTER 1

Introduction

1.1 Background

The development of Integrated Circuits (ICs) and Complementary Metal- Oxide-Semiconductor (CMOS) has revolutionized our daily life needs including, televisions, laptops, mobile phones, etc. as well as transformed the industrial applications comprising, robotics, sensors, amplifiers, etc. The fundamental element of the ICs and CMOS technology is the Metal Oxide Semiconductor Field Effect Transistors (MOSFET). Gorden Moore predicted that with the growth in these technologies, after every 18 months, the number of transistors assembled on a chip would nearly get doubled. This compactness of the transistors lead towards the scaling of the MOSFET's size at nanometer scale along with minimum Short- Channel Effects (SCEs). Fabrication complication also arises in the devices with shorter channel. Therefore, in order to suppress these issues and keep up with the proper functioning, advanced materials and innovative device structures are required.

Various device designs with shorter channel lengths have been proposed which possesses lesser SCEs. Multi- gate MOSFETs are augmenting the scaling dimensions of the device because of their upraised control of the gate over the channel. Double Gate (DG) MOSFETs introduced by Sekigama [1] in 1984 and Balestra [2] in 1987, possesses dual gates, one above and one below the channel. The presence of dual gates leads to better gate control and reduced surface leakage path between the source and drain. Hence, offers higher scalability and more exemption from the SCEs as contrasted with the conventional MOSFETs. To reduce these SCEs further, Huang [3] proposed FinFET in the year 1999. FinFET consists of a thin silicon fin which is surrounded by a metal gate. This structure exercises a higher gate command over the channel and minimizes the SCEs.

To extend the scalability and electrostatic control, another structure named, Cylindrical Surrounding Gate (CSG) MOSFET was proposed [4-9]. In CSG MOSFET, the channel

is entirely wrapped by the metal gate which provides much more escalated gate control over the channel. Therefore, augments the charge carrier density and the overall performance of the MOSFET. CSG MOSFET progressed by implementing double gate MOSFET on CSG structure, thus, evolving a Double Surrounding Gate (DSG) MOSFET. DSG MOSFET exhibits a considerable escalation of the gate control over the channel due to the presence of two cylindrical double gates implemented on a surrounding gate structure. Chen [10] demonstrated experimentally and analytically, research on the DSG MOSFET. DSG MOSFET shows much lower ON resistance, higher drain currents and energy storage capacity (~1.4 times of conventional MOSFETs). All the above- stated devices exhibits the problem of source/drain resistance. In order to eliminate this problem, Colinge [11] introduced a Junctionless Transistor (JLT), which has uniformly doped source (N^+), channel (N^+) and drain (N^+). As the transistors have scaled upto deca nanometres range, it is becoming difficult to reproduce ultra sharp doping concentration gradients along with the thermal budget requirement and costly annealing techniques. Therefore, elimination of junctions due to uniform doping in JLT MOSFET poses a favourable situation. As, there is no change in the doping gradient, hence the fabrication process also becomes simpler. However, the presence of higher doping in the channel region causes the problem of Carrier Mobility Degradation (CMD), which lowers down the ON-state current. To overcome this problem another transistor Junctionless Accumulation Mode (JAM) MOSFET was introduced. In this MOSFET, the doping of the channel is slightly lesser than the source/drain, which reduces the CMD problem and also avoids high- parasitic resistance. Thus, increases the drain current and transconductance with lowered SCEs.

To further mitigate these issues, Device Engineering has been introduced. Dual Metal Gate Engineering [12-15] is considered as one of the solution. This technique employs two metal gates of different work functions, keeping the lower work function metal gate at the drain end [14-19]. This reduces the impact of the high speed electrons at the drain end and thus, elevating the carrier efficiency. Moreover, subthreshold leakage current is a predominant phenomenon in multigate devices and it is prevalent as the gate oxide leakage current. It can be subsided by employing Gate Dielectric Engineering [20-21], which exhibits a high- k dielectric layer in addition to the SiO_2 layer. This helps to

easily subsides the gate leakage current. In this work, two engineering approaches are proposed to make device more efficient.

1.2 MOSFET Scaling

There is spectacular increase in the device density due to continous decrease in minimum feature size. Figure 1.1 depicts the traditional MOSFET device and the scaled MOSFET device, where the MOSFET is scaled by a factor of 'S' (S>1).

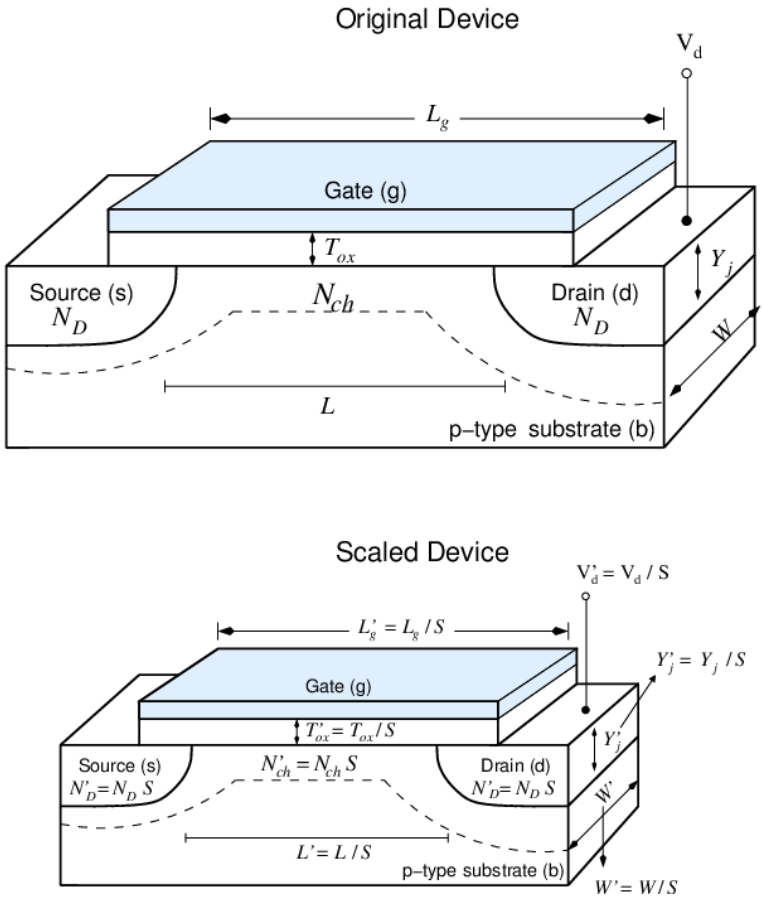


Figure 1.1 Traditional and Scaled MOSFET device structure [22].

As the device size is reduced, more functionality may be added in same size. Apart from this, MOSFET scaling also offers reduction in power consumption and cost of Integrated Circuit (IC). Scaling also leads to increased switching speed because of the decrement in the transit time of the carriers. The MOSFET scaling has been a fundamental driving force behind the continuous improvement in integrated circuit (IC) performance and integration density for several decades.

The concept of MOSFET scaling is rooted in Moore's Law. In 1969, Gordon Moore anticipated that the number of transistors on an IC would get twice approximately after every 18 months as shown in Figure 1.2. Over the years, his law has proved to be true because of the continuous efforts from the semiconductor device design engineers to push the limits of technology. Scaling of MOS devices improves the power density and speed performance of IC but also results in several SCEs. The SCEs dominate in reduced size devices and degrade the performance of the device significantly.

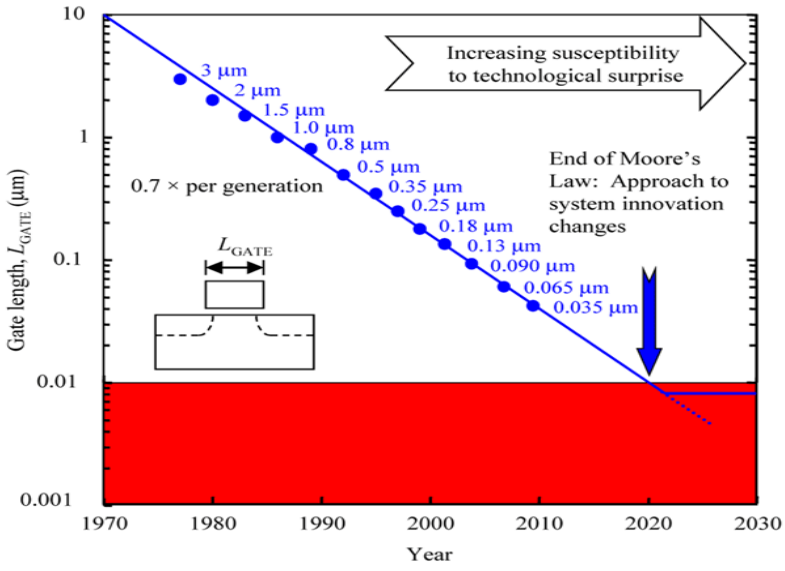


Figure 1.2 MOSFET scaling [*23*].

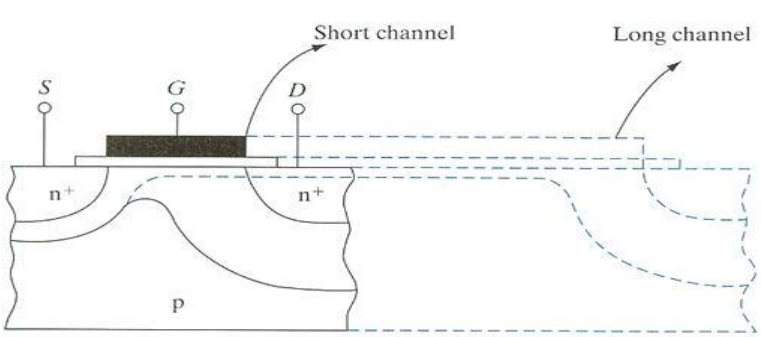
1.3 Short Channel Effects (SCEs)

These are the phenomena that occur in MOSFET when the length of the channel is down- sized to the nanometer range. As the channel length reduces, traditional MOSFET face several challenges that can degrade transistor performance and reliability. Scaling the dimensions of the MOSFET device has made the depletion region comparable with the channel length. This makes the gate lose all its control over the channel, thus, instigating various kinds of SCEs which hamper the effective working of the MOSFET by altering its input and output characteristics. The main SCEs are described as follows:

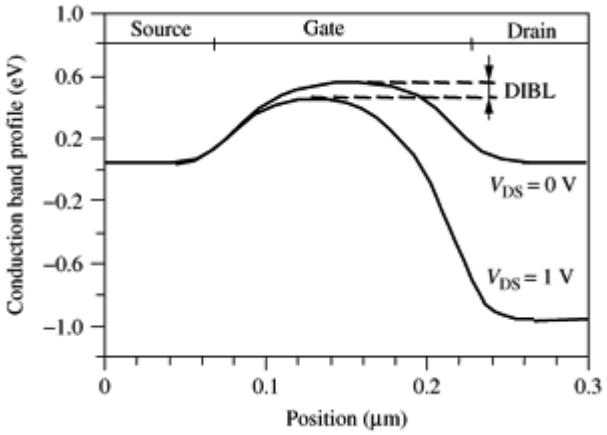
1.3.1 Drain Induced Barrier Lowering (DIBL)

DIBL [24, 25] can be described as the lowering of the threshold voltage of a MOSFET when the drain is connected at higher voltages. The threshold voltage is the gate voltage

required to invert the surface of the channel and to make a conductive path between the source to drain. Figure 1.3(a) illustrates the depletion region in the channel for long and short channel devices and Figure 1.3(b) represents the conduction band profile versus position across the channel length at V_{ds}= 0 V and 1.0 V. In the long channel devices, the potential barrier is dependent only on the gate voltage. However, in short channel devices, the potential barrier is also dependent upon the drain bias as well. This is because the source and drain sections lie in close proximity in the case of short channel devices. It is observed that if the drain bias is increased in short channel devices, the potential barrier decreases. This also changes and reduces the threshold voltage. This deduction in the threshold voltage in short channel devices owing to the applied drain bias is termed as DIBL.



(a)



(b)

Figure. 1.3 Elucidation of (a). long channel and short channel device and (b). DIBL [26].

1.3.2 Threshold Voltage Roll-off

In short channel devices, charge sharing takes place between source and drain regions and it further instigates field penetration from drain to source region [26] as depicted in Figure 1.4. Field penetration lowers the potential barrier at the source end, consequently, increasing the charge carriers flow and causing decrement in threshold voltage and higher sub-threshold drain current.

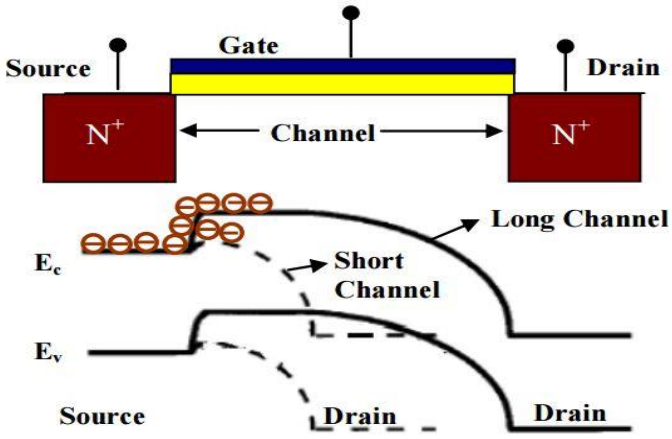


Figure 1.4 Threshold- Voltage Roll- off illustration using Conduction Band and Valance Band diagram.

1.3.3 Channel Length Modulation

With the increase in the drain bias, the channel region is pinched off at the drain end, reducing the channel length (L) by ΔL as shown in Figure 1.5. This decrease in the effectual channel length of the MOSFET is termed as Channel Length Modulation. Tise pinch off at the drain side alters the drain current and threshold voltage for the device. However, in long channel devices the threshold voltage does not depends upon ΔL. Hence, the effective channel length will be L-ΔL.

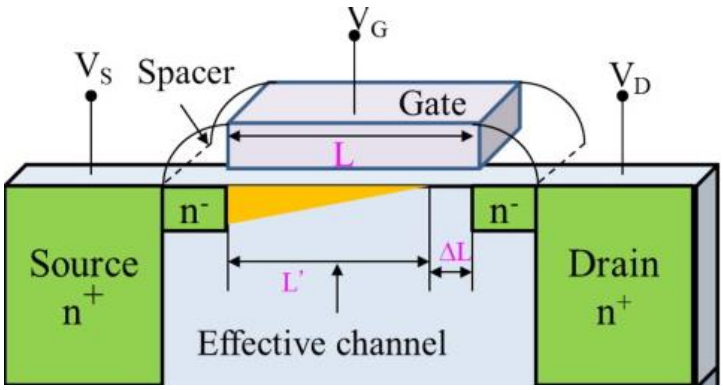


Figure 1.5 Schematic illustration of Channel Length Modulation [27].

1.3.4 Punchthrough

Punchthrough effect in MOSFET takes place when the depletion region encompassing the drain-body junction stretches in the direction of the source-body junction, with the result that the both the depletion regions meet with each other and form a single depletion region. This effect is well depicted in Figure 1.6. At this point, gate loses its control over the channel. Consequently, the current cannot be regulated with the gate voltage and increases rapidly with drain bias [28]. The prime cause behind this punchthrough effect is that the current transport occurs deeper in the bulk and distant from the gate. Thus, increasing the subthreshold leakage current, which further results into an increment in the power consumption. Punchthrough effect can be lowered down by increasing the substrate doping [29]. This technique reduces the depletion regions surrounding the source and drain. Thus, no parasitic current path formation takes place. But this also leads to the increment in the subthreshold swing, which makes this approach not to be suggested to minimize punchthrough effect. Other techniques to diminish punchthrough can be using narrower oxides, shallower junctions and of course, by employing longer channel lengths.

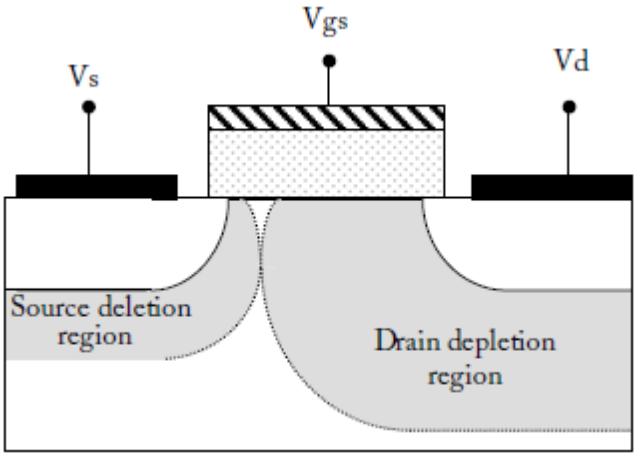


Figure 1.6 Schematic diagram for punchthrough effect [30].

1.3.5 Impact Ionization and Hot Carriers Effects

When electric field is enhanced in the short channel length devices, the carriers acquire excessive kinetic energy greater than their thermal energy, and then they are referred to as “hot carriers”. These carriers can follow three possible phenomenons: (i). these hot carriers can multiply themselves owing to impact ionization, leading to high substrate current. (ii). Carriers possessing energy more than the dielectric conduction band energy

may cause conduction current towards the gate. (iii). Carriers with very high energy can get introduced towards the inside of the gate oxide layer and may destroy the dielectric interface. This can also alter the threshold voltage and drain current of the device. These three phenomenons portraying hot carrier injection mechanism are displayed in Figure 1.7.

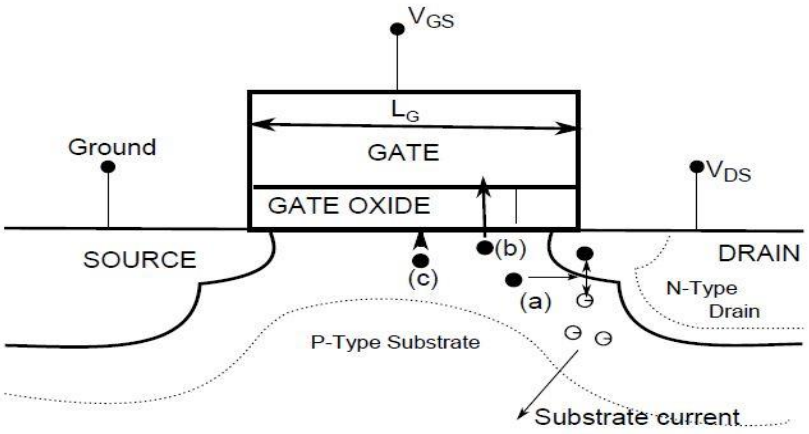


Figure 1.7 Diagrammatic representation for hot carrier injection mechanism [31].

1.3.6 Band- to- Band- Tunneling (BTBT) Leakage

Another challenge that arises in heavily doped transistors is the BTBT Leakage mechanism. MOSFETs working in the volume depletion mode in the OFF- state behaviour possesses an overlapping between the valence and the conduction bands in the channel and drain regions respectively [32, 33]. Because of the higher doping present inside the channel, band overlap results in the tunnelling of electrons arising out of valence band of the channel towards the conduction band of the drain region [32] (for n- channel junctionless transistor). This tunnelling leakage mechanism is depicted in Figure 1.8, which further brings about the escalation of the drain leakage current during the OFF- state. This augmentation in the drain current is unenviable and brings about large amount of static power dissipation. Therefore, BTBT is a prime difficulty encountered in the case of low standby power (LSP) applications.

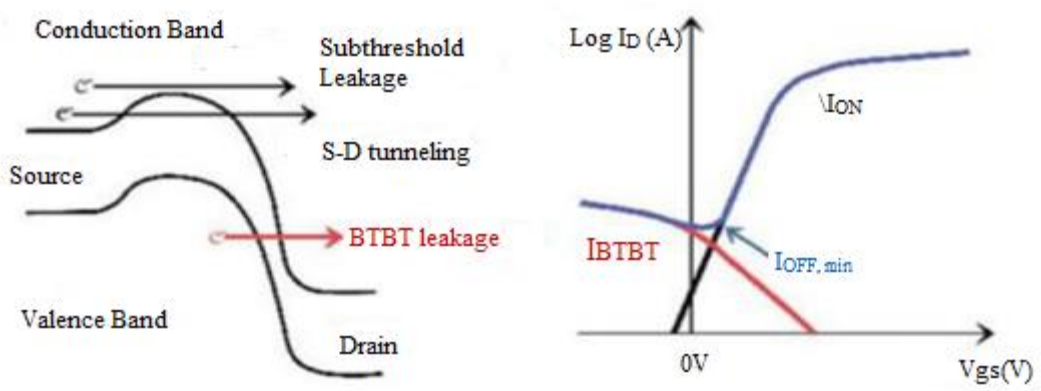


Figure 1.8 Schematic diagram of various leakage mechanisms [34].

1.3.7 Velocity Saturation

This effect also influences the functioning of the short-channel MOSFET devices. The velocity of the electrons is directly proportional to the electric field. With the increase in the electric field, the velocity of the carriers also rises. At elevated electric field, this velocity attains a maximum critical value and at this value, the electron velocity starts to saturate. Beyond the saturation velocity, further increase in the electric field will bring about the decrease in the mobility of the electrons, thus, causing minimization of the drain current and transconductance. With the aim of avoiding such situation, employment of constant field scaling is done; this would retain the identical electric field. The variation of electron velocity with electric field is well represented in Figure 1.9.

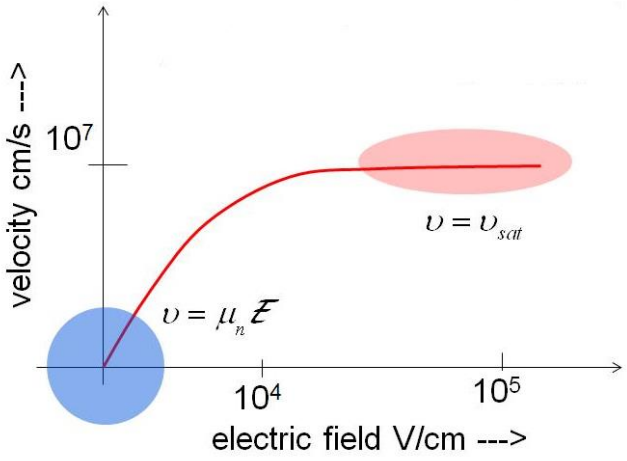


Figure 1.9 Velocity of the electron versus electric field for silicon.

1.3.8 Gate Oxide Leakage

When the width of the gate oxide is reduced to 3nm or 2nm or less than this in the MOSFET devices, tunnelling of the carriers occurs. This in turn increases the gate oxide leakage current, which deteriorates the functioning of the device. This may be eliminated by implementing a gate stack within the device. The gate stack is a combination of a low- k oxide accompanied by a high- k oxide layer, this administers towards the decrement in the leakage current to some extent.

1.4 Literature Survey

In order to compensate for the SCEs upon the device significantly, several device topologies [21, 36-40, 53-55] have been introduced. Such device topologies are enumerated as:

1.4.1 Double Gate (DG) MOSFET

It consists of two gates existing on both sides of the channel called as a front gate and a back gate [33] and is shown in Figure 1.10. Thus, controls the channel very effectively by employing dual gate contacts and shorter channel width. This assists in subduing the short channel effects and further directing towards higher drain current [35]. T. Sekigawa and Y. Hayashi introduced DG MOSFET in 1984 [36] stating the robustness of this device over single- gate MOSFET. This happens since the gate guards the channel from both the sides, thus quelling the electric field penetration through the gate and helps in lowering down the SCEs. There can be two alignments for the case of DG MOSFETs: Asymmetric or Symmetric DG MOSFET. Asymmetrical DG MOSFET has distinct biasing applied on both the gates, whereas in symmetrical DG MOSFET, the two gates are connected to a common bias. Also, the thickness of the two oxides is different for the instance of asymmetrical DG MOSFET and similar thickness for the symmetrical DG MOSFET instance.

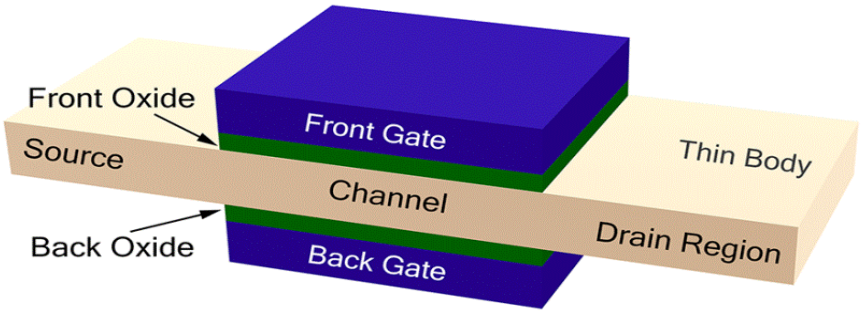


Figure 1.10 Structure of Double Gate MOSFET [37].

1.4.2 Fin-FET

As the number of interconnected gate leads to increment in the control of the gate over the channel, electrostatic potential increases. So the further improvement in DG MOSFET resulted in Tri- Gate or Fin- FET MOSFET structure. In Fin- FET, gate surrounds the narrow silicon pillar from three sides, called as "fin" which builds up the gate control over the channel. Consequently, lowering down the SCEs encountered by deep submicron transistors, such as DIBL and threshold voltage roll- off. It also minimises the leakage current. This device topology was proposed by Huang et al in 1999 [38] and is depicted in Figure 1.11. As, it is gated on three sides of the channel, hence is named "Tri- Gate".

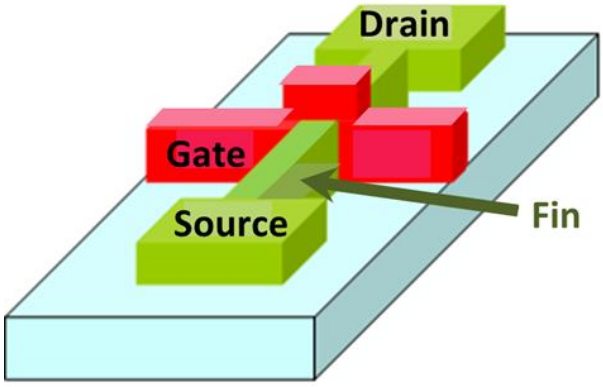


Figure 1.11 Schematic view of Fin-FET structure [39].

1.4.3 Gate All-Around (GAA) MOSFET

In GAA MOSFET [40-42], the gate wraps all over the beam of silicon pillar. The gate may have any type of orientation like broad or thin, rectangular, triangular, or

circular. GAA MOFET is also known as Surrounding Gate MOSFET [43, 44] or Wrap Around Gate MOSFET [45]. As a consequence of the existence of gate all around the channel, better electrostatic control is provided by GAA MOSFET. It offers 50% more scalability than DG FET [43, 45]. The major benefit of the GAA perspective is immensely inflated packing density in the event of vertical structures; on the other hand, the major drawback is the extremely confined current-carrying potential per device which acts as an utmost constraint for rapid logic applications [46].

1.4.3.1 Rectangular GAA MOSFET

Figure 1.12 depicts the 3D and cross-sectional structure of Rectangular GAA MOSFET. In this, a gate of rectangular shape completely wraps around the rectangular substrate. Rectangular GAA MOSFET provides magnificent electrostatic control of the channel, elevated current drivability, favourable subthreshold swing, strengthening of mobility and also possesses reduced SCEs as compared with the DG and Fin-FET structures.

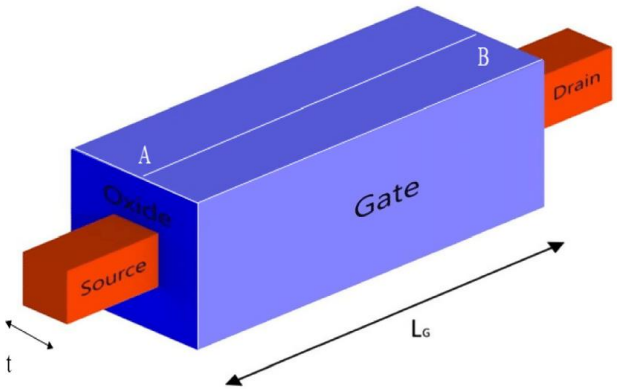
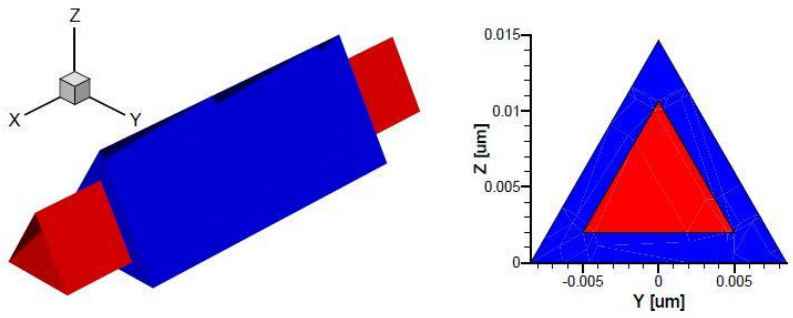


Figure 1.12 Rectangular GAA MOSFET [47].

1.4.3.2 Triangular GAA MOSFET

Figure 1.13 shows the 3D and cross-sectional structure of triangular GAA MOSFET. Here the gate is of triangular shape, completely surrounding the triangular substrate material. The local volume inversion in corners, called as corner effect increments the low field mobility in these type of MOSFET. It also helps to enhance the conduction across the sharp corners of the triangular GAA MOSFET.

In addition, a substantial strengthening of the carrier mobility (around ~1000cm^2/Vs) is noticed for the triangular cross-sectional MOSFETs.

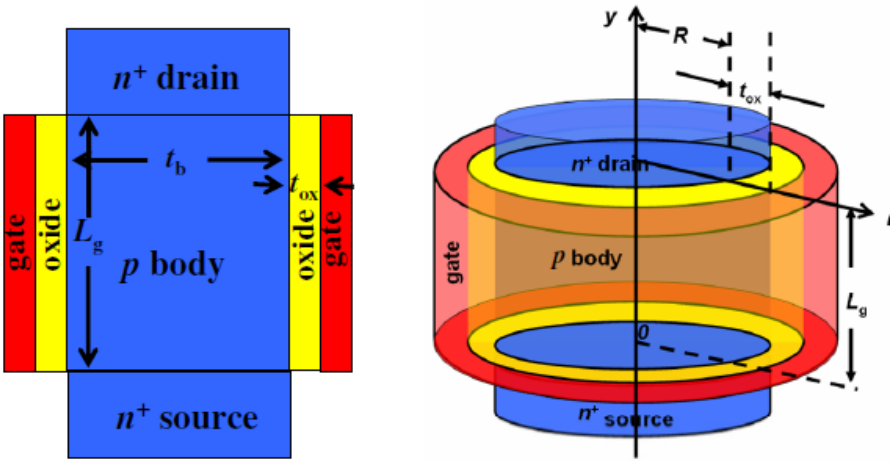


(a) (b)

Figure 1.13 Triangular GAA MOSFET **(a)** 3D view **(b)** cross sectional view [48]**.**

1.4.3.3 Cylindrical GAA MOSFET

Figure 1.14 shows the cylindrical GAA MOSFET. In Cylindrical GAA (CGAA) MOSFET [49-53], the gate completely wraps around a cylindrical shaped semiconductor substrate material. The sidewalls of the pillar are utilized as the channel region. CGAA MOSFET offers much more robustness towards SCEs, excellent controllability of gate, improved transport property and compatibility with CMOS technology [54, 55]. Thus, stands out to be one of the most favourable structure for future technology.



(a) (b)

Figure 1.14 (a) 2-D and (b) 3-D structure of Cylindrical GAA MOSFET [56].

1.4.4 Gate Electrode Engineering

Gate transport efficiency is related to the average electron velocity traversing through the channel that is further related to the electric field distribution across the channel. In FET, the electrons enter with a small initial velocity inside the channel and gradually accelerate when moving near the drain end. The electrons move expeditiously near the drain section as the utmost electron drift velocity is attained nearby the drain and is relatively slow around the source region. Hence, the device's speed gets influenced by the slow electron drift velocity inside the channel close to the source region. To enhance the gate transport proficiency and to reduce the SCE's, Gate Material Engineering (GME), was suggested by Long *et al*. [57] in *1997* as illustrated in Figure 1.15.

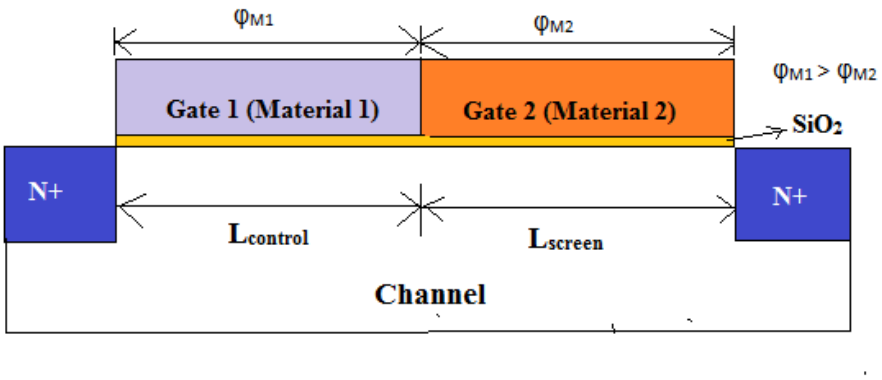


Figure 1.15 The Dual Material Gate FET (DMGFET) structure [57].

Gate-material engineering involves metal gates possessing distinct work-functions to establish a field discontinuity along the channel, thereby elevating the transport efficiency and leading to reduction in SCE*s*. The work function of the metal present at the source side (ϕ_{M1}) is higher than the metal employed at the drain side (ϕ_{M2}). This adjusts the channel electric field profile such that enhanced field occurs at the source end. Consequently, this enhances the velocity of the carriers to screen drain potential variations and therefore minimizes the CLM effect. Electric field also gets reduced near the drain end, thereby diminishing the HCEs. This enhanced carrier transport efficacy also leads in improvement of drain current and transconductance.

1.4.5 Gate Dielectric Engineering

Silicon dioxide (SiO_2) is being used as a conventional oxide layer in the MOSFETs

since 1960s. Reduction of oxide layer thickness is important for the purpose of MOSFET scaling. This layer has been reduced from the value of 300 nm upto 1.2 nm. This scaling down of the oxide layer will in turn provide greater gate capacitance and hence higher ON current for the device. The high ON current provides improved transconductance and switching capability. Also, reduction of the oxide thickness controls the threshold voltage roll off which helps in suppression of the subthreshold leakage current. For oxide thickness lesser than 2 nm, tunneling of the carriers through this oxide layer becomes a serious issue generating gate leakage current. Additional restrain is the long term operation at higher fields, particularly at higher temperature ranges, when the breaking down of the weak atomic bonds takes place at the silicon-oxide interface leading to creation of oxide charge and shift in the threshold voltage. Thus, a gate stack as shown in Figure 1.16, comprising of a layer of material possessing higher dielectric constant in addition to the SiO_2 layer is used to subdue this problem. This layer of high-k material allows achieving this smaller oxide thickness with suppressed leakage current. Let the thickness of high- k material be t_{hk} with dielectric constant ε_{hk} and thickness of SiO_2 layer be t_{ox} with dielectric constant ε_{ox}, then the Effective Oxide Thickness (EOT) for the gate stack can be calculated as:

$$EOT = t_{ox} + \frac{\varepsilon_{ox} t_{hk}}{\varepsilon_{hk}} \quad (1)$$

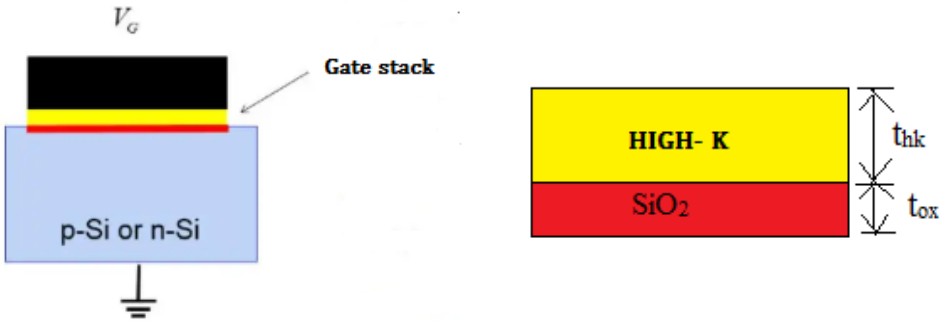


Figure 1.16 Schematic diagram for Gate stack engineering [58].

1.4.6 Junctionless Nanowire Transistor (JLT)

The MOSFETs require abrupt source/drain junctions which makes fabrication process very challenging. In inversion mode MOSFET, two p-n junctions are connected back to back. Below 22 nm technology node, the device length is almost

equal to the depletion region length of the p-n junctions. Then from the perspective of fabrication, it becomes very difficult to manage these p-n junctions. Also below this regime, SCEs and HCEs increase to a greater extent. Therefore, to maintain future of Ultra Large Scale Integration (ULSI) design, elementary changes in the device needs to be incorporated. Thus, a new structure known as Junctionless Transistor was introduced by Colinge et al. [11] to subdue the problems possessed by the junction based transistor. It is a heavily doped transistor in which uniform doping is present through all the regions (source, channel and drain). This uniform doping thus eliminates the development of junctions, by that means getting rid of the difficulty related to the diffusion of the impurities. This structure reduces the effects of various parasitic resistance and capacitances. To improve the gate controllability in junctionless transistor, cylindrical gate structure has been proposed [59, 60].

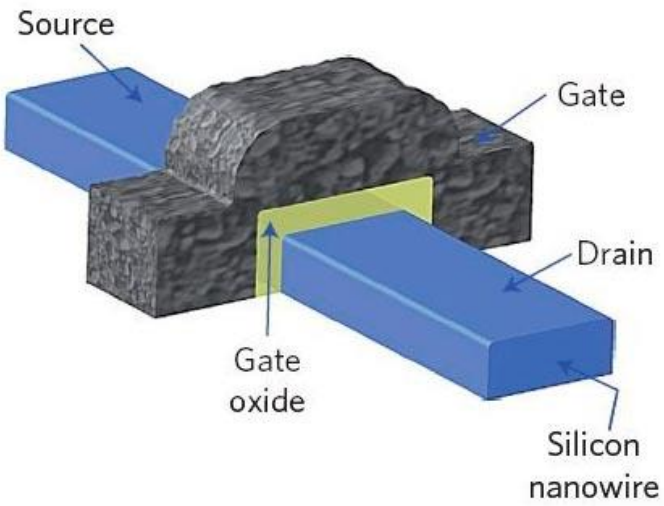


Figure 1.17 Junctionless Transistor [11].

The fundamentals of the JLT are quite dissimilar compared to the traditional MOSFET, as shown in Figure 1.18. Below the threshold voltage, a large electric field gets created which is perpendicular to the direction of the current flow due to the depletion of the heavily doped transistor. However, beyond the threshold voltage, the electric field slides to zero. The mentioned mechanism is the converse of the operation with the inversion-mode (IM) and accumulation-mode (AM) transistors, in which the electric field reaches maximum during the time the device

is switched ON [61]. From the Figure 1.18, below threshold voltage, the mobile carriers in channel region are depleted. Therefore, no conduction path lies between the source and drain regions. When sufficient amount of gate voltage is applied, conduction path starts forming and the carriers start to flow across the center of the semiconductor film.

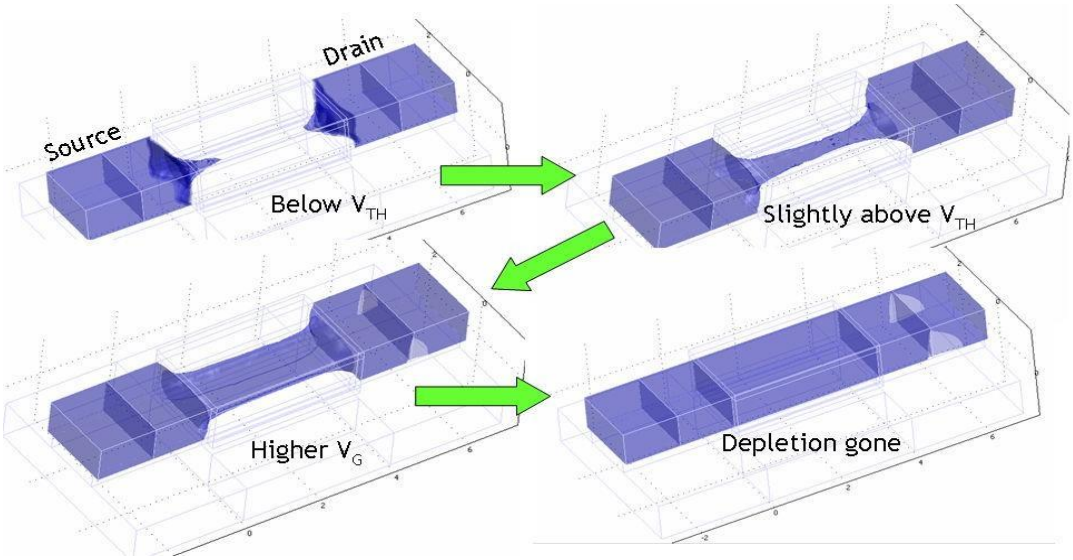
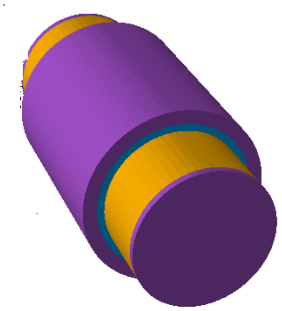


Figure 1.18 Operation mechanism of junctionless transistor [62].

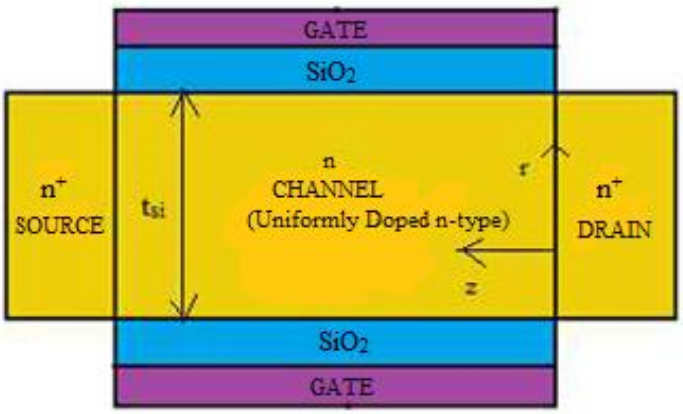
1.4.7 Junctionless Accumulation Mode (JAM) MOSFET

Junctionless Transistor has numerous advantages as discussed in previous section. However, the mobility of the carriers gets degraded in the Junctionless Transistor due to the highly doped channel; this phenomenon is known as Carrier Mobility Degradation (CMD). This CMD causes lower drain current and lower transconductance. Also, in JLT the current is confined in the middle of the channel and a variation of current is also present moving from center to the surface. Furthermore, metal gate with higher workfunction is needed in order to fully deplete the channel. These shortcomings can be overcomed by the newly introduced structure called as Junctionless Accumulation Mode (JAM) MOSFET [63-65]. JAM MOSFET is a homogeneously doped structure, in which the channel is slightly less doped as compared to source/drain regions (N^+- N- N^+). This lesser doped channel helps in overcoming the problem of CMD and leads to improvement in the drain current and transconductance. Also, metal with lower workfunction is required in

JAM MOSFET to fully deplete the channel. Figures 1.19(a) and 1.19(b) illustrates the 3-dimensional and 2- dimensional view of the JAM-CSG MOSFET.



(a)



(b)

Figure 1.19(a) 3-D and **(b)** 2-D cross-section view of JAM-CSG MOSFET.

1.4.7.1 Conduction Mechanism in Junctionless Accumulation Mode Transistor

Figure 1.20 depicts various modes of operation for the MOSFET, i.e., i) inversion-mode ii) accumulation and iii) junctionless.

i) Inversion- mode: Let us consider an n-channel device having p-type substrate. Here, the flatband voltage (V_{fb}) lies below the threshold voltage (V_{th}). Subthreshold region exist between these two voltages, V_{fb} and V_{th}. In this region, the silicon is depleted. Further increasing the gate voltage, i.e., above V_{th}, the silicon surface gets inverted and is shown in Figure 1.20(a).

ii) Accumulation- mode: Taking into account an n-channel device with a lightly doped n-type substrate, the silicon is depleted below V_{th}. As the silicon becomes neutral, threshold voltage is reached. At V_{th}, bulk current starts flowing. When the entire silicon becomes neutral, flatband voltage (V_{fb}) is reached. In the middle of V_{th} and V_{fb}, there is partial depletion and additional increase of gate voltage, lead to the formation of surface accumulation layer. This is illustrated in Figure 1.20(b).

iii) Junctionless: In this mode, a heavily- doped n-type substrate is present in an n-channel device. Below V_{th} or in subthreshold region, the silicon is depleted. When the silicon becomes neutral, i.e., no longer depleted, threshold voltage is reached and bulk current starts to flow. The amount of current in this mode is much higher than in the case of accumulation- mode. With the increase in the gate voltage, the device becomes partially depleted. When the channel becomes neutral, the device reaches flatband voltage. By increasing the gate voltage further, an accumulation layer is created and is shown in Figure 1.20 (c).

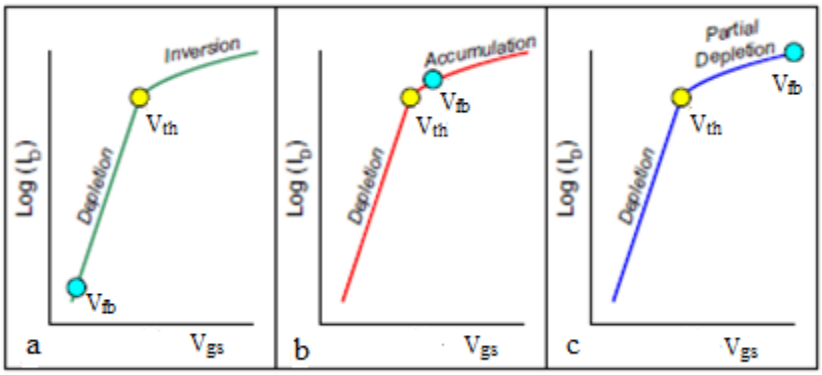


Figure 1.20 Conduction Mechanism in (a). Inversion Mode Transistor, (b). Accumulation Mode and (c) Junctionless transistor [62].

1.5 Device Simulation

Before carrying out expensive and time consuming fabrication processes, device simulation provides speedy results for the device under consideration. Thus, device simulation plays a very important role for designing the device. The simulations can compute various parameters like terminal currents, voltages, charges, etc. build on a set of device equations– Poisson's and continuity equations. Semiconductor device simulation ATLAS developed by Silvaco International, is widely used by semiconductor engineers and researchers for simulating the conduct of several

semiconductor devices, including MOSFETs, BJTs, diodes, and more. ATLAS offers a powerful platform for analyzing device characteristics, optimizing device designs, and predicting device performance under different operating conditions. A brief description of ATLAS capabilities is as under:

- It allows users to simulate the fabrication process concerned with the semiconductor device manufacturing, such as doping, oxidation, and deposition. It also enables simulation of device operation and performance, including DC characteristics, small-signal behavior, and transient responses.
- It incorporates a wide range of physical models that describe the functioning of semiconductor devices grounded on fundamental principles such as semiconductor physics, carrier transport, and electrostatics. These models enable accurate simulation of device behavior at various length scales and operating conditions.
- It supports the simulation of a variety of semiconductor device structures, including planar MOSFETs, FinFETs, nanowire FETs, bipolar junction transistors (BJTs), diodes, and more. It also allows users to define custom device structures and geometries for specialized applications.
- It provides built-in material databases with parameters for commonly used semiconductor materials. Users can also define custom material properties and models for simulating novel materials and device structures.
- It generates a computational mesh for simulating semiconductor devices based on user-defined device geometries and meshing parameters. The mesh generation process ensures accurate representation of device structures and enables efficient numerical simulation.
- It offers tools for visualizing simulation results, including current-voltage characteristics, charge distributions, electric field profiles, and more. Users can analyze simulation data to gain insights into device behavior and performance and optimize device designs accordingly.

- It supports the study of the environmental conditions as well like temperature, pressure, etc. to notice the device functioning in such domain.

Table 1.1

Various Models available in ATLAS

Category	**Models Available**
Statistics	Boltzman, Fermi-Dirac, Incomplete ionization, Bandgap narrowing
Mobility	Concentration dependent mobility (Standard, Analytic, Arora Model), Carrier-Carrier scattering model, Field dependent mobility model, Surface scattering mobility model, CVT model, Yamaguchi model.
Recombination	Shockley-Read-Hall (SRH) recombination model with fixed lifetime and with concentration dependent lifetime, Auger recombination model
Impact ionization	Crowell and Sze model, Grant's model, Selberherr model
Tunneling	Fowler-Nordheim tunneling model, Band to Band tunneling model, Direct quantum tunneling model, Hot carrier injection model, Concannon's Injection Model
Energy transport	Energy balance model, Hydrodynamic model.
Quantum	Self-Consistent Coupled Schrodinger Poisson Model, Density Gradient (Quantum Moments Model), Bohm Quantum Potential (BQP), Quantum Correction Models, General Quantum Well Model, Quantum Transport: Non-Equilibrium Green's Function Approach, Drift-Diffusion Mode-Space Method (DD_MS).

Overall, ATLAS is a versatile and powerful tool for semiconductor device simulation, offering comprehensive capabilities for modeling, simulating, and analyzing the behavior of various semiconductor devices. It is extensively utilized in both academic research and industrial applications for advancing semiconductor technology and developing next-generation electronic devices. In this thesis, ATLAS 3-D device simulator from Silvaco [66] has been utilized. Table 1.1 indicates the various models

available in ATLAS to model the device mechanism.

1.6 Thesis Organization

The thesis is categorized into seven chapters and each chapter is organized to be largely self-contained. A brief depiction of chapters is as follows:

Chapter 1: Introduction

This chapter includes the fundamental invention of MOSFET and is discussed along with Moore's law which explains the scaling of MOSFET and the potential issues that may arise with it. Further in this chapter, the overview of various short-channel effects has been described. The various conventional and non-conventional structures have also been discussed stating their advantages and disadvantages. Additionally, the historical background of the previous work done in this field is also covered.

Chapter 2: Dual‑metal gate stack engineered junctionless accumulation‑mode cylindrical surrounding gate (DMGSE‑JAM‑CSG) MOSFET

This chapter proposes a dual- material gate stack engineered junctionless accumulation-mode cylindrical surrounding gate (DMGSE-JAM-CSG) MOSFET. The physics-based 2-D analytical model using 2-D Poisson's equation in cylindrical co-ordinate system is also put forward. It is seen that this device possesses enhanced drain current, higher transconductance, lower output conductance and high I_{on}/I_{off} ratio as compared to the JAM-CSG MOSFET, which leads to its usage for low power and high speed switching applications. The electrical characteristics and short channel effects of this device are also examined for different gate stack materials. It is observed that the device characteristics improve when permittivity of the gate stack is increased. Further, the results acquired using analytical modeling is mapped with the simulated data results to affirm and validate the device model structure.

Chapter 3: Temperature dependency and linearity assessment of dual-metal gate stack junctionless accumulation-mode cylindrical surrounding gate (DMGS-JAM-CSG) MOSFET

A physics-based temperature-dependent analytical model for a Dual- Metal Gate Stack Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGS-JAM-CSG) MOSFET has been presented in this chapter by solving the 2D Poisson's equation utilizing the suitable boundary conditions. The device performance is examined at various temperatures (T=100K, 300K and 500K) by observing several parameters like potential, electric field, electron concentration and electron velocity. The obtained analytical outcomes are also contrasted with the outcomes acquired after simulation. Lastly, to check the relevancy of the device for RFIC applications, linearity assessment is performed by evaluating its several figure of merits (FOMs) like second-order and third-order Voltage Intercept Points (VIP2, VIP3), third-order Intercept Input Power (IIP3), third-order Intermodulation Distortion (IMD3) and various higher order transconductances.

Chapter 4: Analytical model for junctionless accumulation-mode cylindrical surrounding gate (JAM-CSG) MOSFET as a biosensor

This chapter proposes analytical modeling for Junctionless Accumulation-Mode Cylindrical Surrounding Gate (JAM- CSG) MOSFET-based biosensor used for label free electrical detection of the biomolecules (enzymes, cells, DNA, etc.). Modeling has been performed using the Poisson's equation and considering parabolic potential profile. A nanogap cavity is being created for providing a binding site for the biomolecules. Influence of both the neutral and charged biomolecules immobilized in the nanogap cavity has been studied. The change in the threshold voltage is being utilized as a measure for detecting the existence of the biomolecules inside the cavity region. The sensitivity parameter has also been found considering different cavity heights. Furthermore, the analytical model outcomes are validated with the simulated ones.

Chapter 5: Non-Uniform Doping Dependent Electrical Parameters of Dual- Metal Gate All Around Junctionless Accumulation-Mode Nanowire FET (DMGAA-JAM-NWFET)

This chapter presents an analytical analysis of a Dual-Metal Gate All Around Junctionless Accumulation- Mode Nanowire FET (DMGAA-JAM-NWFET) possessing a horizontal-like non-uniform doping profile. The 2-D electrostatic potential distribution is evaluated using Poisson's equation under the applicable boundary conditions. Also,

the impact of straggle length parameter and the peak doping concentration upon the device behaviour is also examined. The analytical outcomes are authenticated through TCAD simulations. Both the results were contrasted and found to be in good agreement. The outcomes obtained for non-uniform doped DMGAA-JAM-NWFET are also compared with that of uniformly doped DMGAA-JAM-NWFET and finer electrical characteristics were noticed for non-uniformly doped device.

Chapter 6: Modeling of Dual- Metal Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DM-JAM-CSG) MOSFET for Cryogenic temperature Applications

This chapter introduces the characterization of the Dual- Metal Junctionless Accumulation-Mode Nanowire FET (DM-JAM-NWFET) at cryogenic temperatures. Mathematical model has been developed by using the 2-D Poisson's equation under the relevant boundary conditions. It is perceived from the study that at cryogenic temperatures, the performance of the considered FET does not differ by a significant amount when compared to that at room temperature. By varying the temperature from 50K to 300K, it is noticed that the variation in center potential, electric field, transconductance, output conductance, drain current are almost minimum. The TCAD results were achieved by deploying ATLAS 3-D device simulator and were also contrasted along with the numerical results.

Chapter 7: Conclusion and Future Scope of research work

This chapter concludes the entire work based on the results presented. Additionally, it discusses about the future scope of the presented research work and explores further expansion of this work to be utilized in future for enhancing the device performance.

1.7 References

[1] T. Sekigawa and Y. Hayashi, "Calculated Threshold-Voltage Characteristics of an XMOS Transistor Having an Additional Bottom Gate", *Solid-State Electronics*, vol. 27, pp. 827-828, 1984.

[2] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double Gate silicon-on Insulator Transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Letter*, vol. 8, no. 9, pp. 410-412, 1987.

[3] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, and L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V Subramaniam, T. J. King, J. Bokor anf C. Hu, "Sub 50-nm FinFET: PMOS" *In Proceeding of International Electron Devices Meeting Technical Digest*, p. 67, December, 5–8, 1999.

[4] C. Li, Z. Yiqi, and Han Ru, "New analytical threshold voltage model for halo-doped cylindrical surrounding-gate MOSFETs," *Journal of Semiconductor*, vol. 32, no.7, pp. 1–8, 2011.

[5] R. Gautam, M. Saxena, R. S. Gupta, M. Gupta, "Two Dimensional Analytical Subthreshold Model of Nanoscale Cylindrical Surrounding Gate MOSFET Including Impact of Localised Charges," *J. of Com. and Theoretical Nanoscience*, vol. 9, pp. 1-9, 2012.

[6] Kranti, S. Haldar and R. S. Gupta, "Analytical model for threshold voltage and I-V characteristics of fully depleted short channel cylindrical/surrounding gate MOSFET," *Microelectronic Engineering*, Vol. 56, no. 3-4, pp. 241-259, 2001.

[7] Y. Pratap, P. Ghosh, S. Haldar, R.S Gupta, and M. Gupta "An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering," *Microelectronics Journal*, vol. 45, no. 4, pp. 408–415, April 2014.

[8] D. Sharma, S. K. Vishvakarma, "Precise analytical model for short channel Cylindrical Gate (CylG) Gate-All-Around (GAA) MOSFET," *Solid-State Electronics*, vol.86, pp.68-74, 2013.

[9] L. Zhang, C. Ma, J. He, X. Lin, M. Chan, "Analytical solution of subthreshold channel potential of gate underlap cylindrical gate-all-around MOSFET," *Solid-State Electronics*, vol. 54, pp. 806–808, 2010.

[10] Y. Chen and W. Kang, "Experimental study and modeling of double–surrounding gate and cylindrical silicon–on-nothing MOSFETs," *Microelectron Engineering*. vol. 97, pp. 138-143, 2012.

[11] Jean-Pierre Colinge, Chi-Woo Lee, Aryan Afzalian†, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi, Brendan O'Neill, Alan Blake, Mary White, Anne-Marie Kelleher, Brendan McCarthy and Richard Murphy," Nanowire transistors without junctions" Nature Nanotechnology, DOI: 10.1038/nnano.2010.15, pp. 1-5, 2010.

[12] M. T. Bohr, R. S. Chau, T. Ghani, and K. Mistry, "Intel's High-k Dielectric and Metal Gate Process Solution" *IEEE Spectrum*, Nov. 2007.

[13] T.K Chiang, M. L. Chen "A new analytical threshold voltage model for symmetrical double-gate MOSFETs with high-k gate dielectrics" *Solid-State Electronics*, Vol. 51, pp 387-393, 2007.

[14] Z. Zhang, S.C. Song, C. Huffman, M. Hussain, J. Barnett, N. Moumen, H. Alshareef, P. Majhi, J.H. Sim, S. Bae, B.H. Lee, "Inte. of dual metal gate CMOS on high-k dielectrics utilizing a metal wet etch pro., Electro- chem." *Solid-State Lett.*, vol.8, pp. 271–274, 2005.

[15] X. Zhuy, J.Zhu, A.Li, Z.Liu, N.Ming, Challenges in atomic- scale characterization of high-k dielectrics and metal gate electrodes for advanced CMOS gate stacks, *J. Material Science :Mater. Electron.*, vol. 25, no. 3, pp. 289–313, 2009.

[16] P. Razavi and Ali A. Orouji, "Nanoscale Triple Material Double Gate (TM-DG) MOSFET for Improving Short Channel Effects". *ICAEM conference proceeding*, 2008.

[17] H. K. Wang, T. K. Chiang and M. S. Lee, "A New Two-Dimensional Analytical Threshold Voltage Model for Short-Channel Triple-Material Surrounding-Gate Metal–Oxide–Semiconductor Field-Effect Transistors". *J.J.A.P*, vol. 51, pp-054301, 2012.

[18] M. J. Kumar, Ali A. Orouji and H. Dhakad, "New Dual-Material SG Nanoscale MOSFET: Analytical Threshold-Voltage Model" *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp 920 – 923, 2006.

[19] Aouaj, A . Bouziane and A. Nouaçry, "Dual Material Gate-Graded Channel-Gate Stack (DMG-GC-Stack) surrounding gate MOSFET: Analytical threshold

voltage (VTH) and subthreshold swing (S) models", *IEEE Electron Device Letters*, pp. 1 – 4, 2011.

[20] Pravin, J. Charles, D. Nirmal, P. Prajoon, and J. Ajayan. "Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications." *Physica E: Low-dimensional systems and nanostructures, vol.* 83,pp 95-100, 2016.

[21] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Gate-material-engineered junctionless nanowire transistor (JNT) with vacuum gate dielectric for enhanced hot-carrier reliability." *IEEE Transactions on Device and Materials Reliability*, *vol.* 16, no. 3, pp 360-369, 2016.

[22] Jaramillo-Ramirez, Rodrigo, Javid Jaffari, and Mohab Anis. "Variability-aware design of subthreshold devices." In *2008 IEEE International Symposium on Circuits and Systems*, pp. 1196-1199. IEEE, 2008.

[23] F. J. Levi, "Towards Quantum Engineering", *Proceedings of the IEEE,* vol. 96, no. 02, pp. 335-342, Feb. 2008.

[24] E. S. Yang, "Microelectronic Devices", *McGraw-Hill*, New York, 1988, pp. 285-294.

[25] K.K. Young, "Short Channel Effect in Fully Depleted SOI MOSFET", *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 399-402, 1989.

[26] Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices," *Cambridge University Press*, New York, 1998. http://dc311.4shared.com/doc/iVXChT-k/preview.html

[27] Tuan, Fu-Yuan, Chii-Wen Chen, Mu-Chun Wang, Wen-Shiang Liao, Shea-Jue Wang, Shou-Kong Fan, and Wen-How Lan. "Thermal stress probing the channel-length modulation effect of nano n-type FinFETs." *Microelectronics Reliability* 83 (2018): 260-270.

[28] W. Lee, T. Osakama, K. Asada, and T. Sugano, "Design Methodology and Size Limitations of Submicrometer MOSFET's for DRAM Application", *IEEE Transactions on Electron Devices*, vol. 35, pp. 1876-1884, 1988.

[29] Y. Taur, Y.-J. Mii, D. J. Frank, H.-S. Wong, D. A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasz, E. J. Nowak, "CMOS Scaling into the 21st Century: 0.1 μm and Beyond", *IBM Journal Research and Development*, vol. 39, pp. 245-259, 1995.

[30] D. K. Slisher, R. G. Filippi, Jr., D. W. Storaska and A. H. Gay, "Scaling of Si MOSFETs for Digital Applications", *Project report Advanced Concepts in Electronic and Optoelectronic Devices*, 1999.

[31] S. Gundapaneni, M. Bajaj, R. K. Pandey, KVRM Murali, S. Ganguly and A. Kottantharayil. "Effect of band-to band tunneling on junctionless transistors," *IEEE Trans. on Electron Devices,* vol. 59, no. 4, pp. 1023–1028, April 2012.

[32] M. Wu, X. Jin, H-I Kwon, R. Chuai, X. Liu and J-H Lee, "The optimal design of junctionless transistors with double-gate structure for reducing the effect of band-to-band tunneling." *Journal of Semiconductor Technology and Science*, vol. 13, no. 3, pp. 245-251, June 2013.

[33] A. Sarkar, A.K Das, S. De, C.K. Sarkar, "Effect of gate engineering in double-gate MOSFETs for analog/RF applications," *Microelectronics Journal*, vol. 43 pp. 873–882, 2012.

[34] Taur, Yuan, and Tak H. Ning. *Fundamentals of modern VLSI devices*. Cambridge university press, 2021.

[35] H.-S.P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann and J. J. Welser, "Nanoscale CMOS**",** *Proceedings of The IEEE,* vol. 87, no. 4, pp. 537-570, 1999.

[36] T. Sekigawa and Y. Hayashi, "Calculated Threshold-Voltage Characteristics of an XMOS Transistor Having an Additional Bottom Gate", *Solid-State Electronics*, vol. 27, pp. 827-828, 1984.

[37] Paydavosi, Navid, Sriramkumar Venugopalan, Yogesh Singh Chauhan, Juan Pablo Duarte, Srivatsava Jandhyala, Ali M. Niknejad, and Chenming Calvin Hu. "BSIM—SPICE models enable FinFET and UTB IC designs." *IEEE Access* 1 (2013): 201-215.

[38] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, and L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V Subramaniam, T. J. King, J. Bokor anf C. Hu, "Sub 50-nm FinFET: PMOS" *In Proceeding of International Electron Devices Meeting Technical Digest*, p. 67, December, 5–8, 1999.

[39] Chau, Robert S. "" Integrated CMOS tri-gate transistors: Paving the way to future technology generations," Technology Intel Magazine." *http://www. intel. com/technology/silicon/integrated_cmos. htm* (2006).

[40] J. M. Colinge, M. Gao, A. R. Rodriguez, H. Maes, and C. Claeys, "Silicon-on-Insulator 'Gate-All-Around Device'," in *Proceedings of International Electron Devices Meeting,* pp. 595-598, 1990.

[41] Y. Pratap, P. Ghosh, S. Haldar, R.S Gupta, and M. Gupta "An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering," Microelectronics Journal, vol. 45, no. 4, pp. 408–415, April 2014.

[42] Y. Pratap, S. Haldar, R.S. Gupta, and M. Gupta "Performance Evaluation and Reliability Issues of Junctionless CSG MOSFET for RFIC Design" IEEE Trans. Device and Material Reliability, vol. 14, no. 1, pp. 418–425, March 2014.

[43] C. P. Auth, and J. D. Plummer, "Scaling Theory For Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's", IEEE Electron Device Letters, vol. 18, no. 2, pp. 74-76, 1997.

[44] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, Fumio Horiguchi, and Fujio Masuoka, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI' s", IEEE Transactions On Electron Devices, vol. 38, no. 3, pp. 573-578, 1991.

[45] E. Leobandung, J. Gu, L. Guo, and S. Chou, "Wire-Channel And Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with Significant Reduction in Short-Channel Effects," Journal of Vaccuum Science and Technology, vol. B-15, pp. 2791-2794, 1997.

[46] H.-S.P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann and J. J. Welser, "Nanoscale CMOS", Proceedings of The IEEE, vol. 87, no. 4, pp. 537-570, 1999.

[47] Razavi, Pedram, and Giorgos Fagas. "Electrical performance of III-V gate-all-around nanowire transistors." *Applied Physics Letters* 103, no. 6 (2013).

[48] Moselund, Kirsten E., Didier Bouvet, Lucas Tschuor, Vincent Pott, Paolo Dainesi, and Adrian M. Ionescu. "Local volume inversion and corner effects in triangular gate-all-around MOSFETs." In *2006 European Solid-State Device Research Conference*, pp. 359-362. IEEE, 2006.

[49] C. Li, Z. Yiqi, and Han Ru, "New analytical threshold voltage model for halo-doped cylindrical surrounding-gate MOSFETs," Journal of Semiconductor, vol. 32, no.7, pp. 1–8, 2011.

[50] R. Gautam, M. Saxena, R. S. Gupta, M. Gupta, "Two Dimensional Analytical Subthreshold Model of Nanoscale Cylindrical Surrounding Gate MOSFET Including Impact of Localised Charges," J. of Com. and Theoretical Nanoscience, vol. 9, pp. 1-9, 2012.

[51] D. Sharma, S. K. Vishvakarma, "Precise analytical model for short channel Cylindrical Gate (CylG) Gate-All-Around (GAA) MOSFET," Solid-State Electronics, vol.86, pp.68-74, 2013.

[52] A Tsormpatzoglou1, D. H. Tassis1, C A Dimitriadis, G Ghibaudo,G Pananakakis and R Clerc "A compact drain current model of short-channel cylindrical gate-all-around

[53] L. Zhang, C. Ma, J. He, X. Lin, M. Chan, "Analytical solution of subthreshold channel potential of gate underlap cylindrical gate-all-around MOSFET," Solid-State Electronics, vol. 54, pp. 806–808, 2010.

[54] P. Ghosh, S. Haldar, R.S. Gupta and M. Gupta, "An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET", Microelectronics Journal, vol. 43, pp.17 – 24, 2012.

[55] R. Wang, J. Zhuge, R. Huang, Y. Tian, Z. Xiao, L. Zhang, C. Li, X. Zhang and Y. Wang, "Analog/RF Performance of Si Nanowire MOSFETs and the Impact of Process Variation", IEEE Tran. On Electron Devices, vol. 54, no. 6, pp 1288 – 1294, 2007.

[56] Jin, Xiaoshi, Xi Liu, Meile Wu, Rongyan Chuai, Jung-Hee Lee, and Jong-Ho Lee. "A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration." *Semiconductor science and technology* 28, no. 1 (2012): 015002.

[57] W. Long and K. K. Chin, "Dual Material Gate Field Effect Transistor (DMGFET)," International Electron Devices Meeting Technical Digest, pp. 549-552, 1997.

[58] Cheng, Baohong, Min Cao, Ramgopal Rao, Anand Inani, P. Vande Voorde, Wayne M. Greene, Johannes MC Stork, Zhiping Yu, Peter M. Zeitzoff, and Jason CS Woo. "The impact of high-/spl kappa/gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs." *IEEE Transactions on Electron Devices* 46, no. 7 (1999): 1537-1544.

[59] J. P. Duarte, S-J Choi, D-I Moon, and Y-K Choi, "A Nonpiecewise Model for Long-Channel Junctionless Cylindrical Nanowire FETs" IEEE Electron Device Letters, vol. 33, no. 2, pp. 155–157, Feb. 2012.

[60] T. Wang, L. Lou, and C. Lee, "A Junctionless Gate-All-Around Silicon Nanowire FET of High Linearity and Its Potential Applications", IEEE Transactions on Electron Devices, vol. 34, no.4, pp.478-484, May 2013.

[61] Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. Dehdashti Akhavan, P. Razavi, JP Colinge,"Junctionless nanowire transistor (JNT): Properties and design guidelines," Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 357–360, 2010.

[62] Colinge, Jean-Pierre, Abhinav Kranti, Ran Yan, Chi-Woo Lee, Isabelle Ferain, Ran Yu, N. Dehdashti Akhavan, and Pedram Razavi. "Junctionless nanowire transistor (JNT): Properties and design guidelines." Solid-State Electronics, vol. 65, pp. 33-37, 2011.

[63] J. H. Choi et al., "Origin of Device Performance Enhancement of Junctionless Accumulation-Mode (JAM) Bulk FinFETs With High- κ Gate Spacers," in IEEE Electron Device Letters, vol. 35, no. 12, pp. 1182-1184, Dec. 2014.

[64] T. K. Kim et al., "First Demonstration of Junctionless Accumulation-Mode Bulk FinFETs With Robust Junction Isolation," in IEEE Electron Device Letters, vol. 34, no. 12, pp. 1479-1481, Dec. 2013.

[65] Zebhbroeck, B. V. "Principal of semiconductor devices.", 2011, online.

[66] ATLAS User's Manual: 3-D Device Simulator, SILVACO International, Version 5.14.0.R, 2014.

CHAPTER 2

Dual- Metal Gate Stack Engineered Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSE-JAM-CSG) MOSFET

2.1 Introduction

In conventional MOSFETs, when scaling of the device dimensions is performed, some short channel and hot carrier effects (SCEs and HCEs) arise [1-2]. These effects result in the performance degradation of the device. Therefore, to suppress this problem, various topologies were presented such as Double- gate (DG) MOSFETs, Triple- gate MOSFET, Cylindrical Surrounding Gate (CSG) MOSFET [3-5]. All these devices exhibit better performance in comparison with the conventional MOSFET. Due to superior gate control, CSG MOSFET offers high short channel immunity, but they also possess a drawback of the development of extremely- sharp source- drain junctions. So, to overcome this issue, Junctionless Transistor (JLT) was proposed by Colinge in 2010 [6]. This transistor has uniform doping in source, channel and drain, therefore, no junction is present and no doping concentration gradient is there. The JLT offers improved electrical properties [7] and is also easy to fabricate. However, the high doped channel leads to degradation in the mobility of the carriers in the JLT and hence lower drain current and lower transconductance. So, another structure, Junctionless Accumulation Mode (JAM) MOSFET [8-9] was introduced. In JAM MOSFET, the channel region's doping is slightly less than that of source and drain. On account of the higher doping present in the source and drain regions, it avoids high parasitic resistance; therefore, providing more conductivity and better characteristics than JLT [10]. The techniques such as Gate- Metal Engineering and Gate Stack Engineering are introduced in order to further improve the SCEs [11-15].

2.1.1 Gate Metal Engineering

In MOSFETs, the electrons travel from the source region towards the drain region. They enter the channel region with a low initial velocity and accelerate its speed as it

progresses towards the drain side. Electron drift velocity is high near the drain region and low near the source region. Thus, the electrons travels slow near the source end and relatively fast towards the drain end. This average electron transport velocity specifies the gate transport efficiency. Now, to improve this gate transport efficiency, Gate Material Engineering was proposed by Long et al [16] in 1997. This engineering involves use of gate materials possessing distinct work- functions, placed side-by-side as shown in Figure 1.15. This placement is such that the metal gate placed near the source side possesses higher metal work-function (ϕ_{M1}) as compared to the work-function of the metal placed at the drain side (ϕ_{M2}), *i.e.*, $\phi_{M1} > \phi_{M2}$. This enhances the electric field at the source side and thus, increases the carrier velocity and due to the presence of lower metal work-function at the drain end, reduces the electric field. Therefore, use of these distinct work-function metals tunes the channel electric field profile such that it results in the reduction of the hot carrier effect. Gate Electrode Engineering offers suppression in SCEs in nanoscale regime, thus providing improved scaling options.

2.1.2 Gate Oxide Engineering

Since 1960s, Silicon Dioxide (SiO_2) has been used as the typical gate insulator in the MOSFETs. The gate dielectric layer thickness has been reducing over the decades from micrometers to 2 nm. The idea behind this reduction in the oxide thickness is that the thinner oxide offers higher gate capacitance and thereby higher ON current of the device. Gate oxide engineering, already mentioned under section *1.4.5* employs a high-k material layer stacked with the SiO_2 layer and is known as gate stack model. This gate stack model helps in reduction of the leakage currents. It basically employs two layer gate oxide stack, shown in Figure 1.16 and the Effective Oxide Thickness (EOT), t_{oxeff} is given by equation (1) mentioned under section *1.4.5*. Various high- k materials can be commonly employed while designing the gate stack model and are listed in Table 2.1 along with their respective permittivities.

Table 2.1

Various High- k Materials with their respective dielectric constants

Material	Si_3N_4	Al_2O_3	Y_2O_3	Ta_2O_5	HfO_2	La_2O_3	TiO_2
K	7.5	10	15	22	25	30	40

2.1.3 Dual- Metal Gate Stack Engineered JAM-CSG (DMGSE-JAM-CSG) MOSFET

Now, using both the techniques of Gate- Metal Engineering and Gate Oxide Engineering, we have proposed a novel structure named, Dual- Metal Gate Stack Engineered JAM-CSG (DMGSE-JAM-CSG) MOSFET in 2020. A physics- based analytical model has also been developed for this proposed structure. In this device, use of dual metal gates and a high-k gate stack is leading towards the enhancement of the device's performance. Simulation of this device has been accomplished and the results are also compared with JAM-CSG MOSFET. This proposed structure possesses improved characteristics and lower SCEs. This has been verified in this chapter by comparing the results with the analogous structures. The investigation has also been carried out by employing different high- k materials in the gate stack. The simulated results have also been compared with the analytical results.

2.2 Device Structure

Figure 2.1 represents the 3- dimensional structure view and Figure 2.2 represents the 2-dimensional cross- section view of DMGSE-JAM-CSG MOSFET. Let the gates towards the source and drain side be represented as gate1 and gate2; with corresponding work functions as ϕ_1 and ϕ_2 (provided $\phi_1 > \phi_2$). In this structure, a high- k gate oxide layer is stacked with the SiO_2 layer. Analysis of the device is carried out by varying the gate stack material. Table 2.2 enlists various parameters utilized in carrying out the simulation. The device will also be investigated for various high-k gate stack materials as listed in Table 2.1.

Figure 2.1 3-Dimensional structural view of DMGSE-JAM-CSG MOSFET.

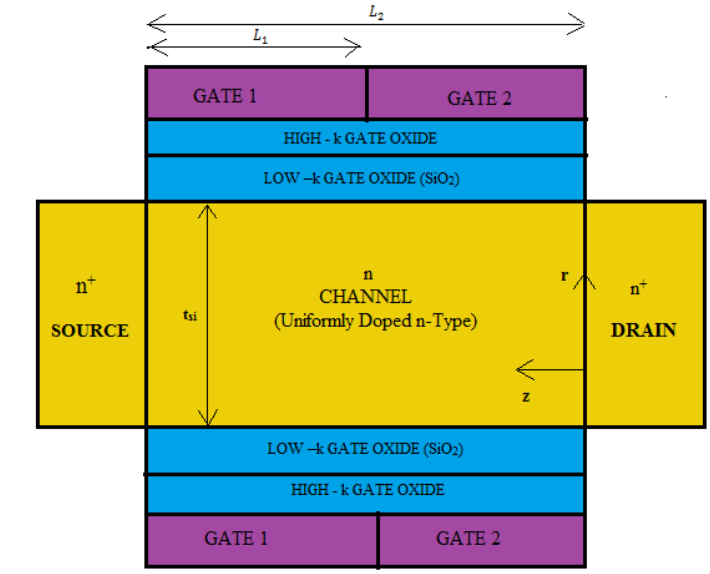


Figure 2.2 2-Dimensional Cross-Section view of DMGSE-JAM-CSG MOSFET.

Table 2.2

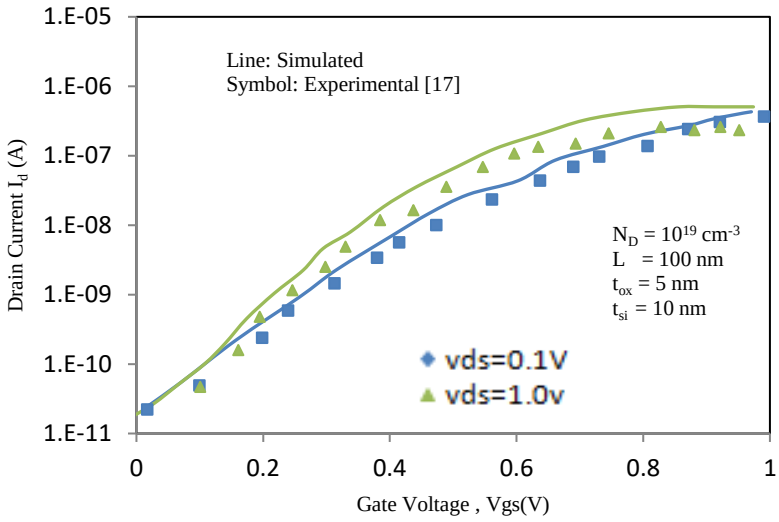
Parameters Employed for the DMGSE-JAM-CSG MOSFET structure

Parameter	**DMGSE-JAM-CSG**
Channel Length	40 nm
Channel Doping	$10^{18}/cm^3$
Source/Drain Doping	$10^{20}/cm^3$
Work- Function (ϕ_1)	5.0 eV
Work- Function (ϕ_2)	4.7 eV
Low- k Gate Oxide	SiO_2
Thickness of Low- k Gate Oxide	1 nm
Thickness of high- k gate oxide	1 nm
Thickness of Silicon Pillar	20 nm
Permittivity of SiO_2	3.9

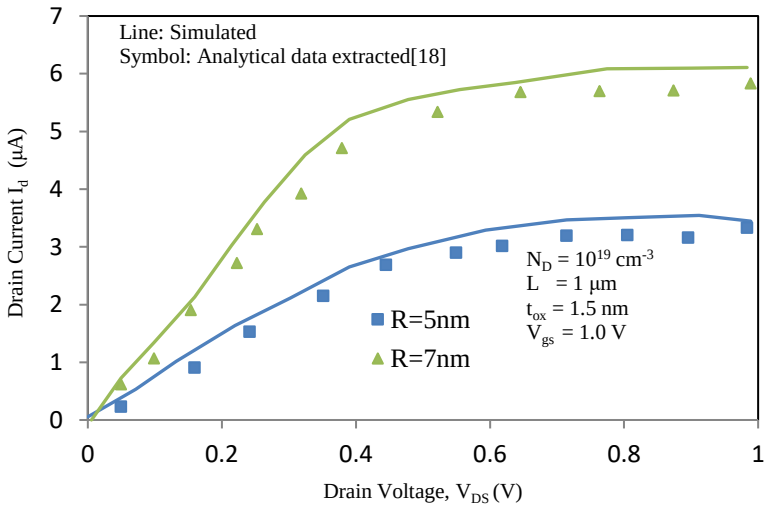
2.2.1 Device Calibration

Figures 2.3 (a) and (b) illustrate the calibration results. For verification of the models, utilized for the device simulation, calibration has been performed with an experimental work of M. Najmzadeh et al. [17] and analytical work of J. Xiao-shi et al. [18]. Figure

2.3 (a) indicates the drain current as a function of gate voltage and Figure 2.3 (b) indicates the drain current as a function of drain voltage. These graphs demonstrate the effectiveness of our model as the simulation data agrees well with the published experimental results and also with the analytical/ theoretical results.



(a)



(b)

Figure 2.3(a) Calibration with M. Najmzadeh et al. [17] experimental work. **(b)** Calibration with J. Xiao-shi et al. [18] analytical data.

2.2.2 Simulation Setup

The simulation is performed using ATLAS- 3D simulator with the help of the models mentioned in Table 2.3 [19].

Table 2.3
Physical Models used for Simulation

Physical Models	Description
Recombination Model	The Shockley– Read– Hall recombination model (with carrier lifetime $1x10^{-7}$ s) is included in simulation to incorporate minority recombination effects.
Concentration Dependent Mobility Model	The Concentration Dependent Mobility model (CONMOB) is invoked to relate the low-field mobility at 300K to the impurity concentration.
Field Dependent Mobility Model	High-field mobility reduction model (FLDMOB) has been used in simulation.
Band To Band Tunneling (BTBT) Model	Standard Band-to Band- Tunneling model has been used in the analysis to inculcate tunnelling effect of the charge carriers.
Statistics	Boltzmann Model because it considers the Carrier Statistics.
Methods	The Newton and Gummel methods are simultaneously invoked for the numerical solution

2.3 Model Derivation

Analytical analysis of DMGSE-JAM-CSG MOSFET is done using parabolic potential approximation by solving 2-D Poisson's equation [20-22] in cylindrical co-ordinates. The model has been developed within appropriate boundary conditions to obtain the center potential, electric field, sub-threshold current, transconductance, output conductance and subthreshold slope.

2.3.1 Electrostatic Potential

Considering that the channel region is fully depleted under sub-threshold conditions, the impact of mobile charge carriers is negligible. The 2-D Poisson's equation in the cylindrical co-ordinates [20-22] is stated as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z)}{\partial r}\right)+\frac{\partial^2 \psi_i(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}},\quad i=1,2 \tag{2.1a}$$

or it can be written as:

$$\frac{\partial^2 \psi_i(r,z)}{\partial r^2}+\frac{1}{r}\left(\frac{\partial \psi_i(r,z)}{\partial r}\right)+\frac{\partial^2 \psi_i(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}} \tag{2.1b}$$

where, $\psi(r,z)$ is potential distribution, r is radial co-ordinate, z is channel length co-ordinate, q is electronic charge, N_D is channel doping concentration and ε_{si} is the permittivity of SiO_2.

Solving equation (2.1), the potential along the radial or z- direction can be estimated using a parabolic profile function as:

$$\psi_j(r,z) = P_{j0}(z) + P_{j1}(z)\, r + P_{j2}(z)\, r^2, \quad 0 \leqslant z \leqslant L \tag{2.2}$$

where, P_{j0}, P_{j1} and P_{j2} are coefficients and their values are obtained by using appropriate boundary conditions.

By substituting $r = 0$ in equation (2.2), the center potential is obtained as:

$$\psi_j(r,z)|_{r=0} = \psi_j(0,z) = \psi_{cj}(z) = P_{j0}(z) \tag{2.3}$$

Equation (2.2) may be written for the two different materials as:

$$\psi_1(r,z) = P_{10}(z) + P_{11}(z)\, r + P_{12}(z)\, r^2, \quad 0 \leqslant z \leqslant L_1 \qquad (Region\ 1) \tag{2.4a}$$

$$\psi_2(r,z) = P_{20}(z) + P_{21}(z)\, r + P_{22}(z)\, r^2, \quad L_1 \leqslant z \leqslant L_2 \qquad (Region\ 2) \tag{2.4b}$$

where, L_1 is the length of gate 1 and L_2 is the total channel length.

The Poisson's equation is interpreted distinguishably for both the regions (region 1 and region 2) with the help of the following boundary conditions [20-22]:

(1). Channel's center potential is given by:

$$\psi(r,z)|_{r=0} = \psi_c(z) \tag{2.5}$$

(2). Surface potential of the channel towards source end is represented as:

$$\psi(r, z=0) = \psi_s(r)|_{z=0} = \phi_{bi} \tag{2.6}$$

where, ϕ_{bi} is the built- in potential and is given as:

$$\phi_{bi} = V_T ln\left(\frac{{N_D}^+}{N_D}\right)$$

V_T is the thermal voltage and is given by, $V_T = \frac{k_B T}{q}$, where, k_B is the Boltzmann's constant and T is the temperature. N_D^+ is the source/ drain doping and N_D is the channel doping concentration.

(3). Surface potential of channel towards drain end is:

$$\psi(r, z = L) = \psi_s(r)|_{z=L} = \phi_{bi} + V_{ds} \tag{2.7}$$

(4). Electric field in center of silicon substrate is zero:

$$E = \frac{\partial \psi(r,z)}{\partial r}|_{r=0} = 0 \tag{2.8}$$

(5). Electric field at interface of silicon and stacked oxide layer is:

$$\frac{\partial \psi(r,z)}{\partial r}|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\psi_{gs} - \psi_{si}\left(r=\frac{t_{si}}{2}, z\right)}{\frac{t_{si}}{2} ln\left(1+\frac{2t_{oxeff}}{t_{si}}\right)}\right] \tag{2.9}$$

where, ψ_{gs} is the gate potential (= $V_{gs} - V_{fb}$) , V_{gs} is the gate-source voltage, $V_{fb}$is flat band voltage (= $\phi_m - \phi_s$), ϕ_m and ϕ_s are work functions for metal and semiconductor respectively, t_{si} is thickness of silicon region, t_{oxeff} is effective thickness of two oxide layers present in the gate stack and is given as:

$$t_{oxeff} = t_{ox} + \frac{\varepsilon_{ox} \,.\, t_{hk}}{\varepsilon_{hk}}$$

here, t_{ox} and t_{hk} are the thicknesses of SiO_2 and HfO_2 layer respectively, ε_{ox} and ε_{hk} are the permittivities of SiO_2 and HfO_2 respectively.

(6). At the interface of two distinct metals (metal 1 and metal 2), surface potential is continuous:

$$\psi_{s_1}(r, L_1)|_{r=\frac{t_{si}}{2}} = \psi_{s_2}(r, L_1)|_{r=\frac{t_{si}}{2}} \tag{2.10}$$

(7). Electric flux is also continuous at the interface of the metals:

$$\frac{\partial \phi_{s_1(R,z)}}{\partial z}|_{z=L_1} = \frac{\partial \phi_{s_2(R,z)}}{\partial z}|_{z=L_2} \tag{2.11}$$

On applying the above boundary conditions, the coefficients $P_{0i}(z)$, $P_{1i}(z)$ and $\mathrm{P_{2i}(z)}(i = 0, 1, 2)$ are computed as:

$$P_{10}(z) = \psi_{c_1}(z) \tag{2.12a}$$

$$P_{20}(z) = \psi_{c_2}(z) \tag{2.12b}$$

$$P_{11}(z) = 0 \tag{2.12c}$$

$$P_{21}(z) = 0 \tag{2.12d}$$

$$P_{12}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \tag{2.12e}$$

$$P_{22}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \tag{2.12f}$$

where, C_{ox} is the capacitance per unit area and is given by:

$$C_{ox} = \frac{2\varepsilon_{ox}}{t_{si}\ln\left(1 + \frac{2t_{oxeff}}{t_{si}}\right)}$$

Now, using the above coefficient values, the center potential specified by equation (2.4) is rewritten as:

$$\psi_1(r, z) = \psi_{c_1}(z) + r^2\frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \tag{2.13a}$$

$$\psi_2(r, z) = \psi_{c_2}(z) + r^2\frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \tag{2.13b}$$

At $r = \frac{t_{si}}{2}$, $\psi\left(r = \frac{t_{si}}{2}, z\right) = \psi_{si}(r = \frac{t_{si}}{2}, z)$, so the equation (2.13) for ψ_{si_1} and ψ_{si_2} becomes:

$$\psi_{si_1}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_1(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)}{\varepsilon_{si}t_{si}}\right) \tag{2.14a}$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)}{\varepsilon_{si}t_{si}}\right) \tag{2.14b}$$

Rearranging the terms in equation (2.14) yields

$$\psi_{si_1}(r=\frac{t_{si}}{2},z)=\left[\frac{4\varepsilon_{si}\psi_{c_1(z)}+t_{si}C_{ox}\psi_{gs_1}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \quad (2.15a)$$

$$\psi_{si_2}(r=\frac{t_{si}}{2},z)=\left[\frac{4\varepsilon_{si}\psi_{c_2(z)}+t_{si}C_{ox}\psi_{gs_2}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \quad (2.15b)$$

The JLT works on bulk to source conduction mechanism, therefore, the center potential is to be calculated for $r = 0$. Center potential for two different metals is solved and is given as:

$$\frac{\partial^2\psi_{c_1}(z)}{\partial z^2}=\frac{1}{\lambda^2}\left[\psi_{c_1(z)}-\eta_1\right], \qquad 0\leqslant z\leqslant L_1 \quad (2.16a)$$

$$\frac{\partial^2\psi_{c_2}(z)}{\partial z^2}=\frac{1}{\lambda^2}\left[\psi_{c_2(z)}-\eta_2\right], \qquad L_1\leqslant z\leqslant L_2 \quad (2.16b)$$

where, the characteristic length (λ), η_1 and η_2 are respectively given by

$$\frac{1}{\lambda^2}=\frac{16\,C_{ox}}{4\varepsilon_{si}t_{si}+{t_{si}}^2C_{ox}} \quad (2.17)$$

$$\eta_1=\psi_{gs_1}+\frac{qN_Dt_{si}}{4C_{ox}}+\frac{qN_D{t_{si}}^2}{16\varepsilon_{si}} \quad (2.18a)$$

$$\eta_2=\psi_{gs_2}+\frac{qN_Dt_{si}}{4C_{ox}}+\frac{qN_D{t_{si}}^2}{16\varepsilon_{si}} \quad (2.18b)$$

General solution of equation (2.15a and 2.15b) comes out as:

$$\psi_{C1}(z)=A\,e^{z/\lambda}+Be^{-z/\lambda}+\eta_1 \quad (2.19a)$$

$$\psi_{C2}(z)=C\,e^{z/\lambda}+De^{-z/\lambda}+\eta_2 \quad (2.19b)$$

where, the coefficients *A*, *B*, *C* and *D* we obtained are given by,

$$A=\frac{e^{-L_1/\lambda}\,(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{-L_1/\lambda}-e^{L_1/\lambda})} \quad (2.20a)$$

$$B=\frac{e^{L_1/\lambda}\,(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{L_1/\lambda}-e^{-L_1/\lambda})} \quad (2.20b)$$

$$C=\frac{e^{-L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{-L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_1-L_2)/\lambda}-e^{(L_2-L_1)/\lambda}} \quad (2.20c)$$

$$D = \frac{e^{L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_2-L_1)/\lambda}-e^{(L_1-L_2)/\lambda}} \quad (2.20d)$$

2.3.2 Electric Field

Electric field distribution of this device along channel length can be found by taking differentiation of center potential (2.19a and 2.19b).

$$E = \begin{cases} -\dfrac{d\psi_{C1}(z)}{dz}, & for \quad 0 \leqslant z \leqslant L_1 \\ -\dfrac{d\psi_{C2}(z)}{dz}, & for \quad L_1 \leqslant z \leqslant L_2 \end{cases} \quad (2.21)$$

2.3.3 Subthreshold Drain Current

It is the current between source and drain when the transistor is operating in subthreshold region [22]. It is given as:

$$I_d(V_{gs}, V_{ds}, z) = \frac{\left[2\pi N_D \mu\left\{1-e^{\frac{-(qV_{ds})}{(k_B T)}}\right\}\right]}{\int_0^{L_1+L_2+L_3} \frac{1}{\int_0^r r.e\left(\frac{q\psi(V_{gs},V_{ds},z)}{k_B T}\right)dr} dz} \quad (2.22)$$

where, μ is carrier's mobility.

2.3.4 Subthreshold Slope (SS)

It is change in gate voltage, V_{GS} for every one decade change in drain current, I_{DS}, i.e.,

$$SS = \left[\frac{d \log (I_{DS})}{d(V_{GS})}\right]^{-1} \quad mV/decade \quad (2.23)$$

2.3.5 Transconductance (g_m) and Output Conductance (g_d)

Transconductance (g_m) is defined as the rate of change in drain current with respect to gate voltage while keeping the drain voltage constant and is given by,

$$g_m = \left(\partial I_d / \partial V_{gs}\right)|_{V_{ds=constant}} \quad (2.24)$$

Output Conductance is rate of change in drain current with respect to drain voltage while keeping the gate voltage constant and is given by,

$$g_d = (\partial I_d / \partial V_{ds})|_{V_{gs=constant}} \quad (2.25)$$

2.3.6 Switching Speed (τ)

Switching speed of a MOSFET gives the measure of the rate of change of the output in response to changes at the input. It is given by,

$$\tau = \frac{C_G V_{DD}}{I_{ON}} \quad (2.26)$$

where, C_G is the gate capacitance, V_{DD} is the drain voltage and I_{ON} is the ON current of the MOSFET.

2.4 Results and Discussion

The simulations have been carried out on ATLAS-3D simulator and the acquired results are also verified with the proposed developed analytical model.

2.4.1 Analysis of the device for different high- k materials

To discover the impact of *k* variation on behaviour of the device, the device is analyzed for different high- *k* materials, i.e., *k*= 7.5, 15 and 22.. Figure 2.4 indicates the center potential of the device across the channel length for various stack materials (*k*= 7.5, 15 and 22) for 40 nm channel length. It is observed from the graph that as permittivity of the material is increased, center potential gets lowered down. This decrease in potential distribution reflects decrease in SCEs [23]. It is also noticed that the simulation results agree well with the analytical model. Due to the higher work function of the metal present near the source end, the charge carriers existing in the channel region experiences an acceleration force and the other gate material that is near the drain end possessing lower work function brings about screening, which results in the lowering down of DIBL and channel length modulation (CLM) effect. This yields in more immunity towards SCEs and HCEs.

Figure 2.5 displays graph indicating electric field across channel of length equal to 40nm for numerous materials (*k*= 7.5, 15, 22). It is noticed from the figure that near the drain side, the peak electric field is lowered. This is due to the presence of lower work function at the drain side which results in reduced HCEs, lowered impact ionization and improved breakdown voltage. Also the presence of the gate stack increases the gate controllability over the channel. From the figure, it is noted that as the material's

permittivity increases, electric field towards the source end increases. Thus, the carrier transport efficiency is increased or there is rise in mean electron velocity. Further, there is close agreement between numerical and simulated results.

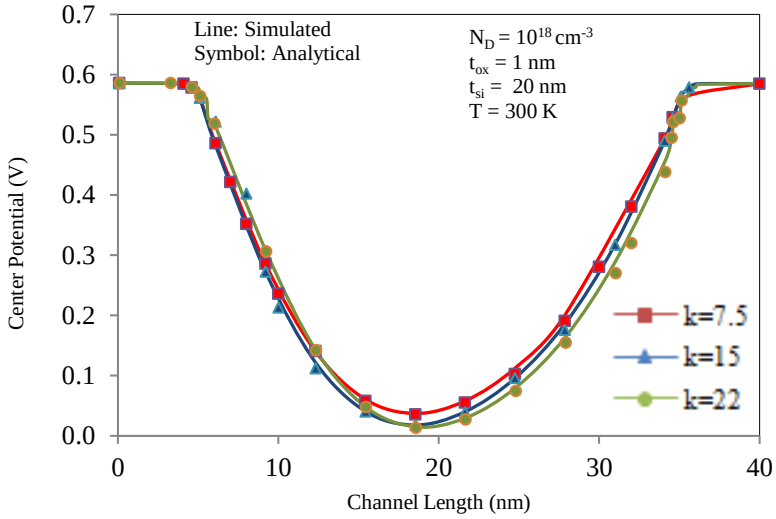


Figure 2.4 Center potential over the channel length of DMGSE-JAM-CSG MOSFET for various gate stack materials (*k*= 7.5, 15, 22).

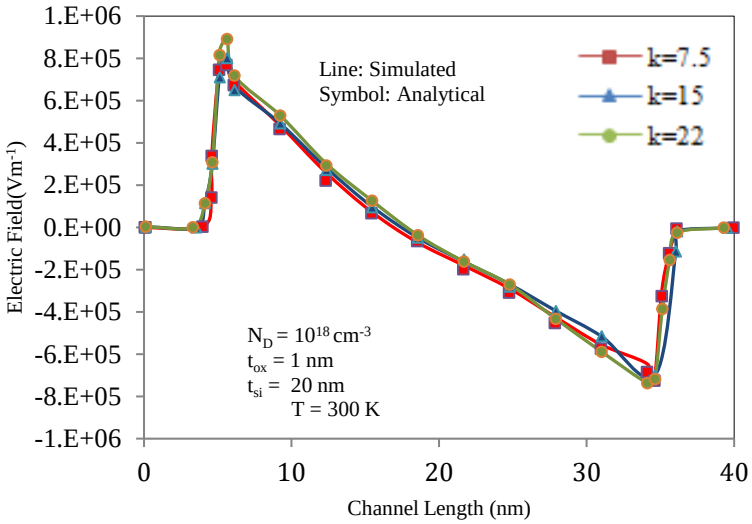


Figure 2.5 Electric field over the channel length of DMGSE-JAM-CSG MOSFET for various gate stack materials (*k*= 7.5, 15, 22).

Leakage current has become a major issue in recent CMOS technology. Various machanisms exists to study this leakage current. Subthreshold leakage [24] is one among these and is a measure of the drain-to-source current that flows when MOSFET

operates in the subthreshold region. Figure 2.6 shows graph of sub-threshold current with gate voltage for various gate stack materials (k= 7.5, 15, 22). It is noticed that when dielectric constant is increased, subthreshold current reduces. This indicates improved device performance. Also, simulated data agrees well with the analytical data.

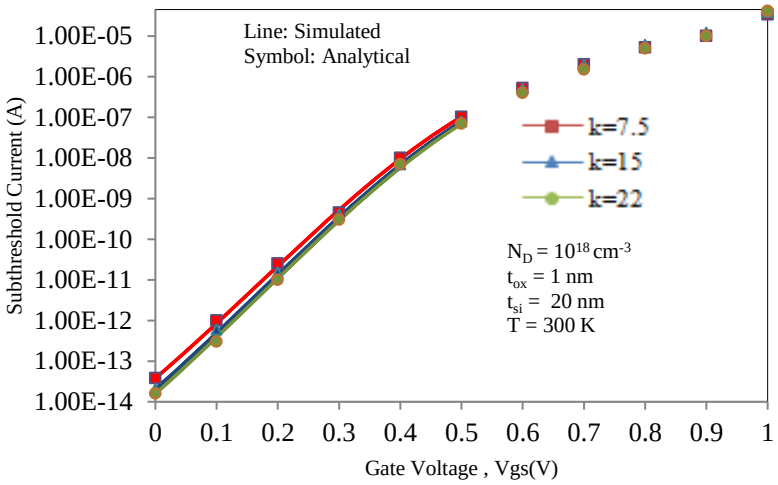


Figure 2.6 Subthreshold current vs. gate voltage of DMGSE-JAM-CSG MOSFET for various gate stack materials (k= 7.5, 15, 22).

Another mechanism for leakage current is Gate-Induced Drain Leakage (GIDL) [25] which is an attribute of presence of high electric field at the drain. This causes band-to-band tunneling current in the gate-to-drain overlap region. Figure 2.7 shows GIDL current (I_{gidl}) with respect to gate voltage for various dielectrics, k= 7.5, 15 and 22. It is seen that the value of I_{gidl} is quite low and its value reduces with increasing dielectric constant. At V_{gs}= 0.4V, I_{gidl} reduces from 5.23E-18A to 4.45E-19A when k moves from 7.5 to 22. The reduced sub-threshold current and GIDL current implies lowering of SCEs and marking the device more efficient.

Figure 2.8 presents graph displaying drain current against gate voltage at drain voltage, V_{ds} = 0.2 for different materials [26-27]. It is noticed from this figure that I_{on} is much higher due to existence of gate stack architecture. It is seen that the drain current is initially almost same for all the three cases but at higher gate voltages, the current rises with the increment in dielectric constant. This effect is due to higher inversion charge resulting from increasing dielectric constant. It is also seen that the simulation results correspond well with the analytical results, thus verifying our model.

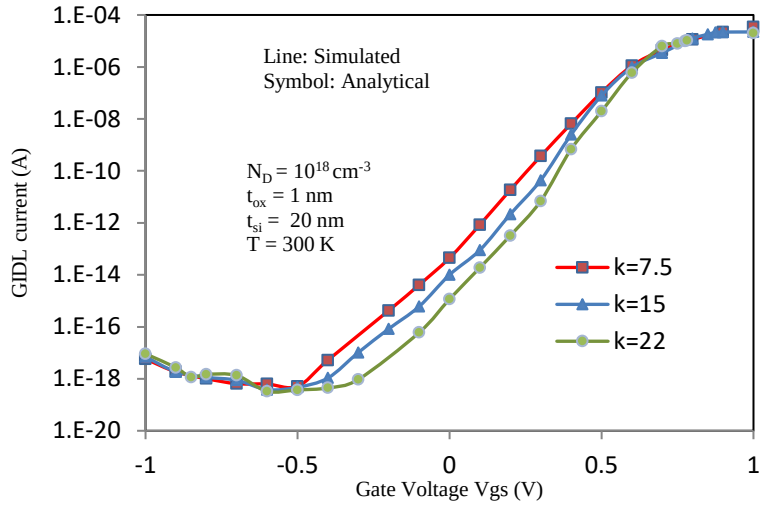


Figure 2.7 GIDL current vs. gate voltage of DMGSE-JAM-CSG MOSFET for various gate stack materials (*k*= 7.5, 15, 22).

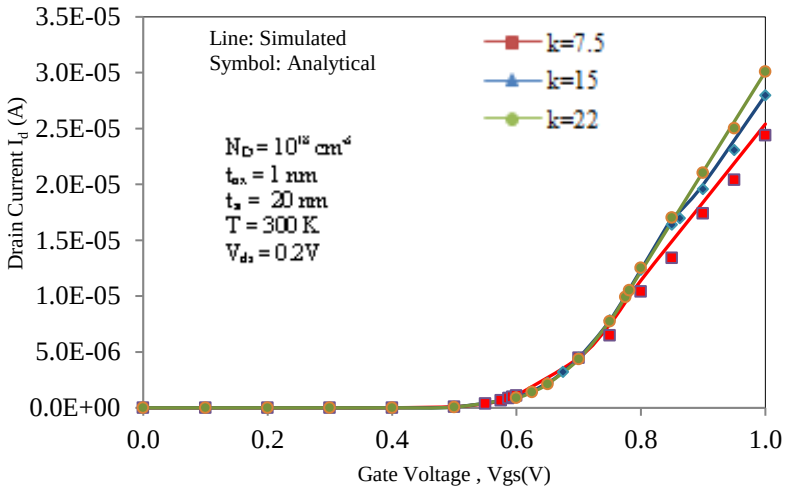


Figure 2.8 Drain current vs. gate voltage of DMGSE-JAM-CSG MOSFET at V_{ds}= 0.2V for various gate stack materials (*k*= 7.5, 15, 22).

Figure 2.9 display drain current as a function of the drain voltage at V_{gs}= 0.1V for various stack materials (*k*= 7.5, 15, 22) for *L*= 40nm. Drain currents for all the three gate stack materials are almost equal in the linear region, whereas, in the saturation region, device with higher *k* exhibits higher drain current. So, there is a rise in the drain current with increase in material's dielectric constant, the reason is same, i.e., higher inversion charge due to increased dielectric constant. The simulated results match well with the analytical ones.

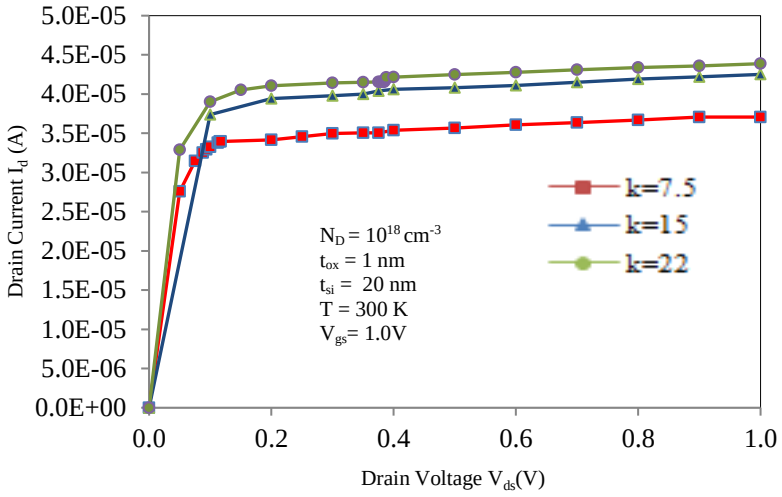


Figure 2.9 Output Characteristics of DMGSE-JAM-CSG MOSFET at V_{gs}= 1V for various gate stack materials (k= 7.5, 15, 22).

Transconductance (g_m) is a vital specification. It determines the potential of the device to drive the load. Another important parameter is output conductance (g_d). Both these terms are already defined in section 2.3.5. Voltage gain of MOSFET is defined as the ratio of the above two parameters, i.e., $A_v = (g_m/g_d)$. This means for higher gain, transconductance should be higher and output conductance should be lower. Figure 2.10 depicts the transconductance (g_m) against the gate voltage (V_{gs}) for several gate stack materials. As seen from the figure that transconductance is higher for k= 22 as compared to k= 7.5 and 15. So, for the higher dielectric constant material, transconductance increases. This indicates its suitability for high frequency and high gain amplifier applications.

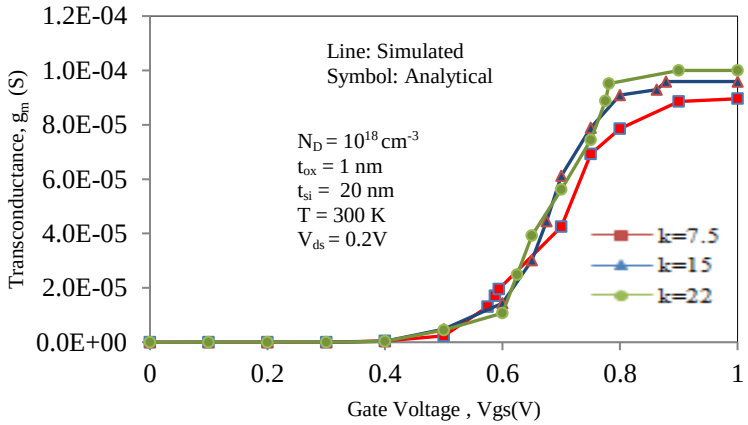


Figure 2.10 Transconductance (g_m) with respect to gate voltage of DMGSE-JAM-CSG MOSFET at V_{ds}= 0.2V for numerous gate stack materials (k= 7.5, 15, 22).

Further, Figure 2.11 indicates output conductance (g_d) with drain voltage (V_{ds}) for several stack materials (k= 7.5, 15, 22). It can be noted from the Figure 2.11 that as dielectric constant increases, output conductance reduces, thus, results in increased voltage gain of the device. Also, increase in the dielectric constant of the stack will lead to increase in the gain of the device. Also, early voltage which is given as, $V_{EA} = (I_d/g_d)$ will also become high due to this lowered output conductance.

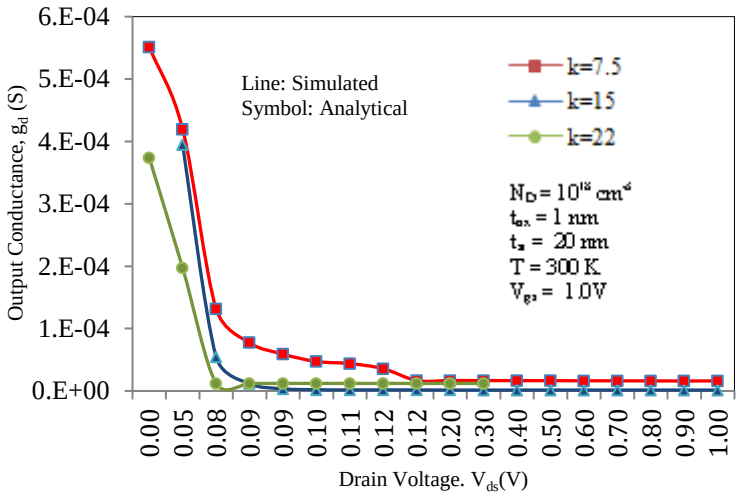


Figure 2.11 Output Conductance (g_d) with drain voltage, V_{ds} of DMGSE-JAM-CSG MOSFET at V_{gs}= 1.0V for different gate stack materials (k= 7.5, 15, 22).

Another important criterion for verifying the device's performance is its switching speed as it provides an estimation of the delay experienced by the output in responding the input change. Using equation (2.26), switching speed is also computed for this device, i.e., DMGSE-JAM-CSG MOSFET for dielectrics, k= 7.5, 15 and 22. Figure 2.12 shows the transient response [28] of this device i.e., DMGSE-JAM-CSG MOSFET for various dielectrics, k= 7.5, 15 and 22. From the graph, it is seen that when the device is turned ON, initially the drain current rises and after some time, it attains a saturated value (ON current). The time at which it attains this ON current is the switching time of the device.

Figure 2.13 shows the variation of switching time with dielectric constant. It is observed that the device is switched ON approximately at the same time irrespective of the dielectric constant. The switching time is nearly at 1ns which authenticates that our device is useful for faster switching applications.

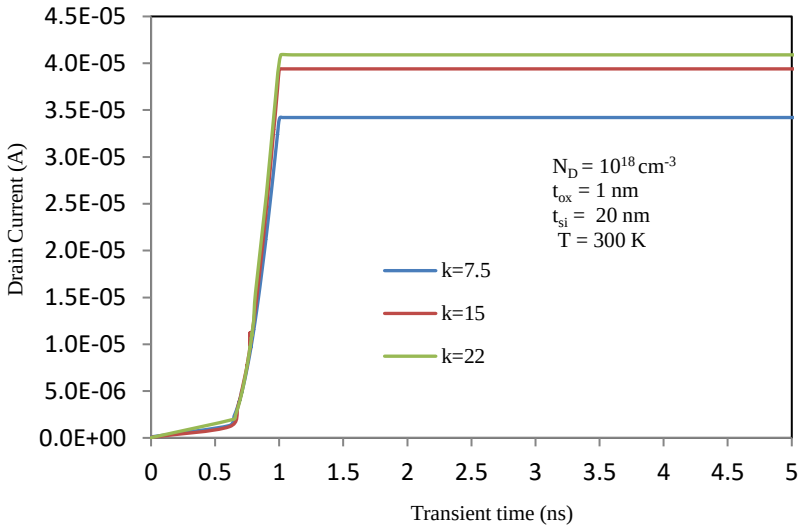


Figure 2.12 Transient time response of DMGSE-JAM-CSG MOSFET for *k*= 7.5, 15 and 22.

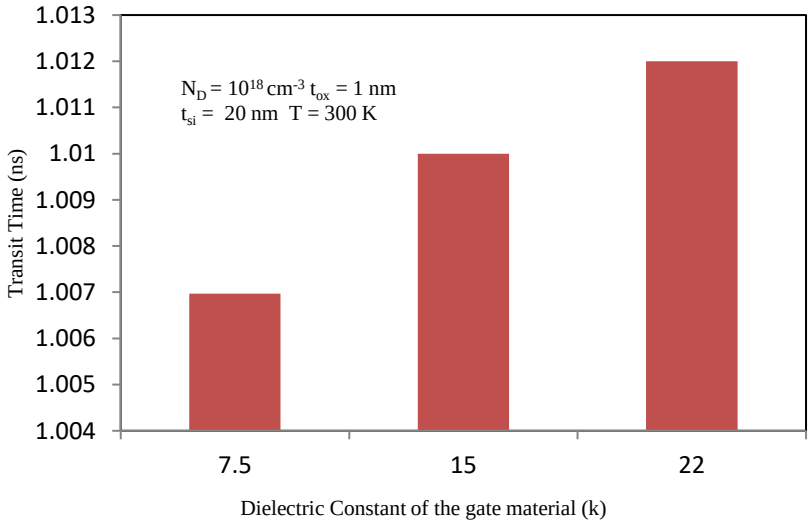


Figure 2.13 Switching time of DMGSE-JAM-CSG MOSFET for the various gate stack materials used.

Also, the operating speed can also be analyzed by computing the I_{on}/I_{off} ratio for this device. Figure 2.14 displays I_{on}/I_{off} ratio of this device when distinct gate stack materials are used. This figure shows that the device possesses very high and improved I_{on}/I_{off} ratio with increase in material's dielectric constant. Numerically, the I_{on}/I_{off} ratio improves from 9.00E+08 (*k*= 7.5) to 3.48E+09 (*k*= 40) indicating its better switching capability. This improvement is caused by the elevated vertical effect of the fringing electric field.

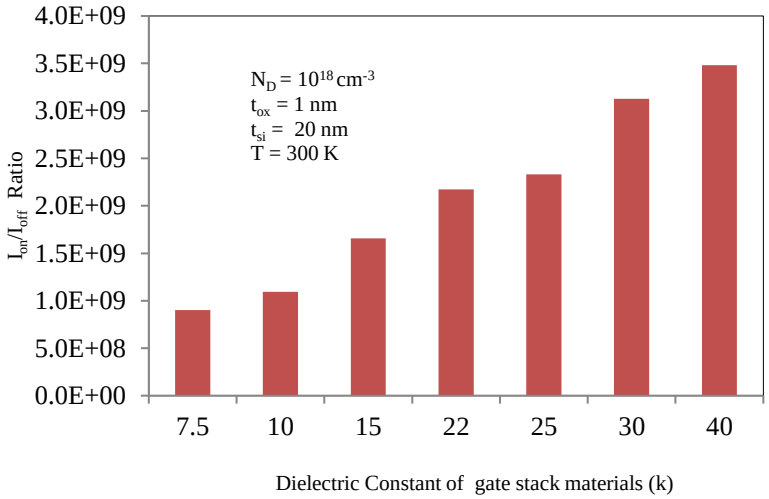


Figure 2.14 I_{on}/I_{off} ratio of DMGSE-JAM-CSG MOSFET considering various gate stack materials possessing distinct dielectric constants.

Subthreshold Slope (SS) [29, 30] is another parameter to measure device performance. Its value should be low, approximately equal to 60 mV/decade. Figure 2.15 depicts variation of SS of the device with *k*. The value of SS is observed to be 74 mV/decade for *k*= 7.5 which reaches approximately 71 mV/ decade for *k*= 30. Thus, the device has better subthreshold slope with increasing dielectric constant. This indicates increased gate controllability over the channel. Hence, the overall device's performance is augmented with the increasing value of *k* of the gate stack material.

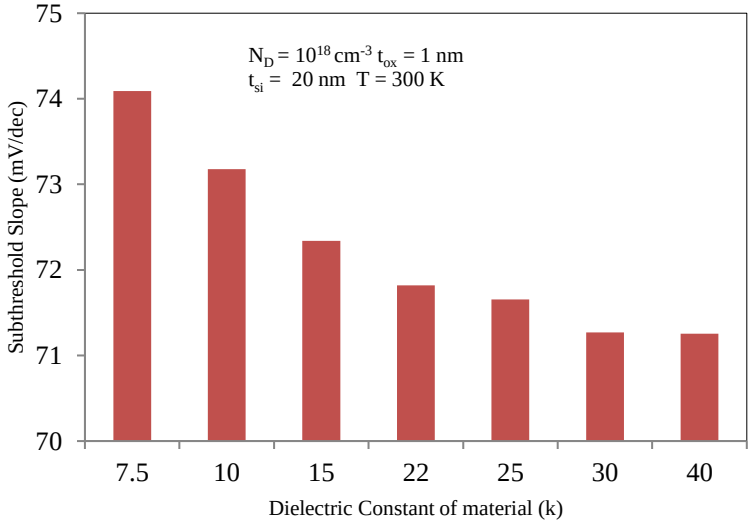


Figure 2.15 Subthreshold slope of DMGSE-JAM-CSG MOSFET for the various gate stack materials used.

2.4.2 Comparison with Analogous Devices

Various electrical characteristics have been evaluated for this device and results are also compared with JAM-CSG MOSFET. Figure 2.16 represents drain current (I_d) w.r.t gate voltage (V_{gs}) at V_{ds} = 0.1V and 1.0V for JAM-CSG MOSFET and DMGSE-JAM-CSG MOSFET. As, can be seen from the graph, DMGSE-JAM-CSG MOSFET possesses improved transfer characteristics. Also, when the value of drain voltage is increased from 0.1V to 1.0V, the threshold voltage is decreasing. This lowering in threshold voltage at higher V_{ds} is due to the DIBL effect [31, 32]. Further, Figure 2.17 depicts drain current (I_d) with respect to drain voltage (V_{ds}) at V_{gs} = 1V. DMGSE-JAM-CSG MOSFET acquires higher drain current in comparison with the JAM-CSG MOSFET

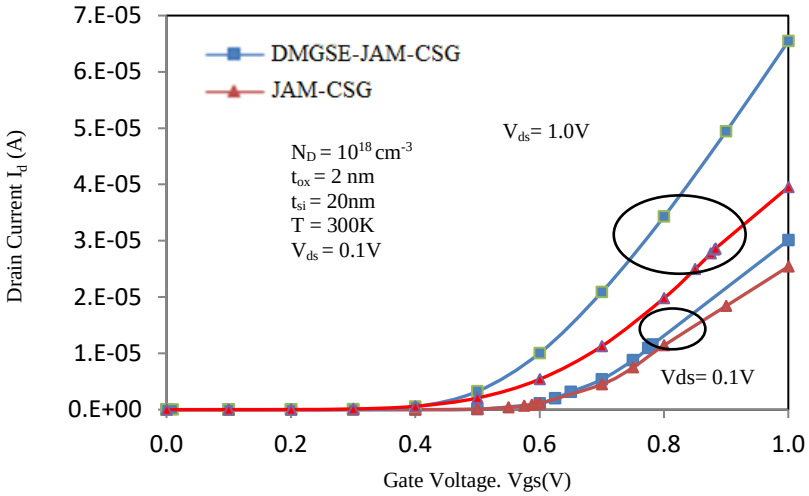


Figure 2.16 Transfer Characteristics for DMGSE-JAM-CSG and JAM-CSG MOSFET at V_{ds} = 0.1V and 1.0V.

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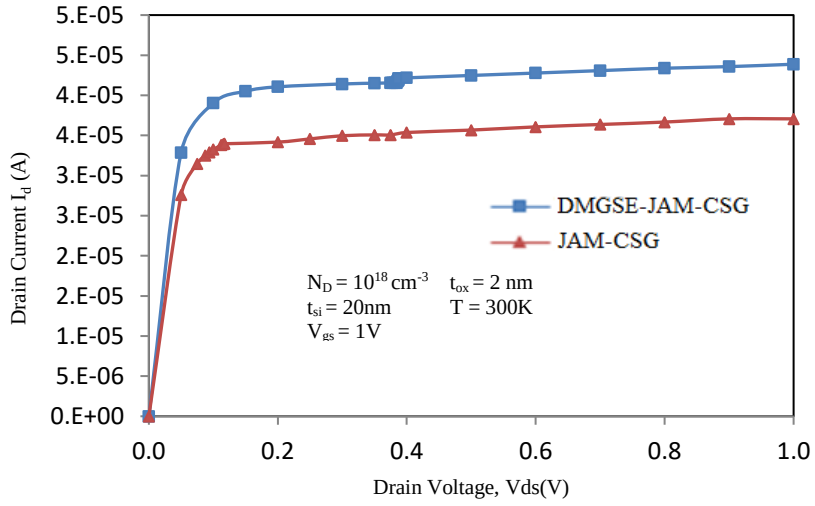


Figure 2.17 Output Characteristics of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

Figure 2.18 shows transconductance with respect to V_{gs} at V_{ds} = 0.1 V. Transconductance is higher for DMGSE-JAM-CSG MOSFET which indicates that this device is more appropriate for high gain amplifier applications. Transconductance Generation Factor (TGF) is calculated as g_m/I_d. Figure 2.19 indicates TGF with respect to gate voltage. DMGSE-JAM-CSG MOSFET shows higher TGF. Higher TGF specifies higher capacity of the MOSFET to amplify a signal.

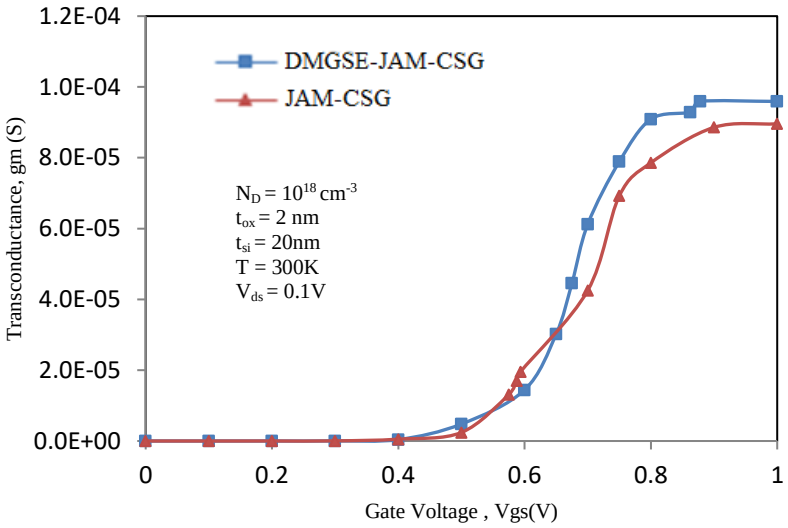


Figure 2.18 Transconductance (g_m) with gate voltage, $V_{gs.}$ of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

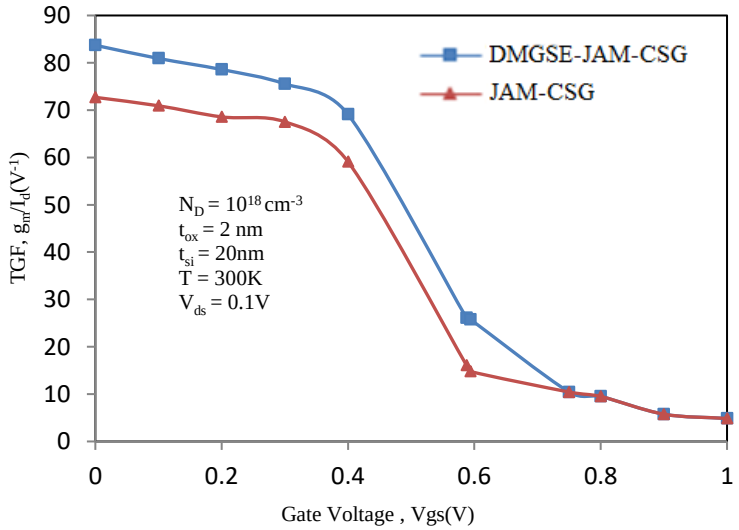


Figure 2.19 Variation of TGF with gate voltage, V_{gs} of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

Figure 2.20 depicts output conductance, g_d with V_{ds}. From figure, it is seen that DMGSE-JAM-CSG MOSFET owns higher output conductance than JAM-CSG MOSFET.

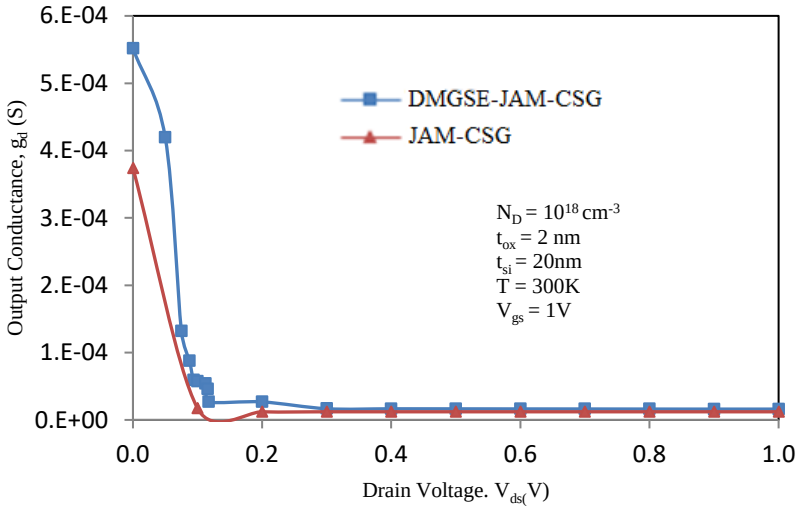


Figure 2.20 Variation of Output Conductance, g_d with drain voltage, V_{ds} of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

Early voltage is a dominant specification of a MOSFET and is given by $V_A = I_d/g_d$. Figure 2.21 represents early voltage with drain voltage. Figure indicates that DMGSE-JAM-CSG MOSFET has improved early voltage.

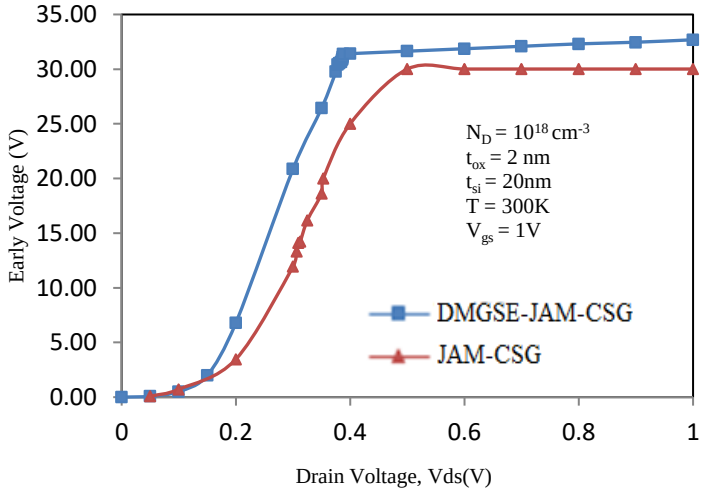


Figure 2.21 Early voltage with drain voltage, V_{ds} of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

Figure 2.22 shows intrinsic gain ($A_v = g_m/g_d$) with respect to V_{gs}. DMGSE-JAM-CSG MOSFET has higher gain. This is because of higher transconductance [33, 34] possessed by DMGSE-JAM-CSG MOSFET as shown in Figure 2.18.

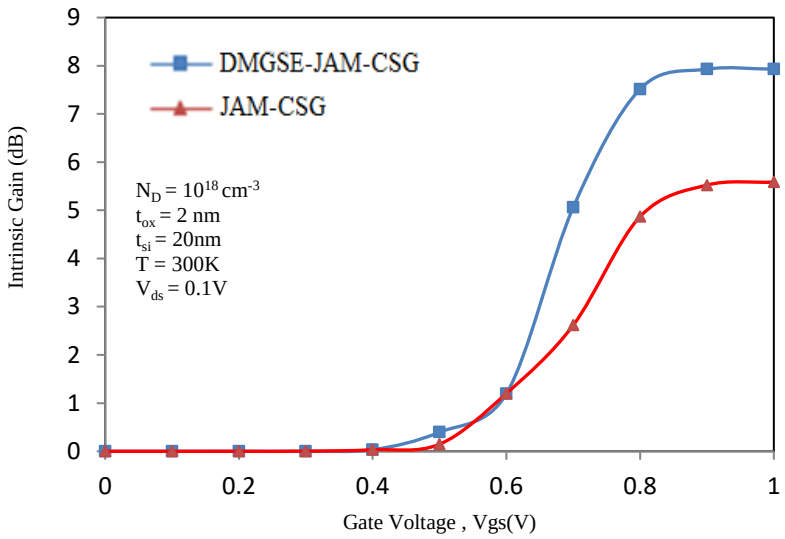


Figure 2.22 Intrinsic Gain with gate voltage, V_{gs} of DMGSE-JAM-CSG MOSFET and JAM-CSG MOSFET.

Figure 2.23 shows Subthreshold Slope (SS) [29, 30] for JAM-CSG and DMGSE-JAM-CSG MOSFETs. SS of a MOSFET is given by equation (2.23), mentioned under section *2.3.4.*). From the figure 2.23, it is observed that the SS of DMGSE-JAM-CSG MOSFET is 67mV/decade, that is more near to the ideal SS value (60 mV/decade).

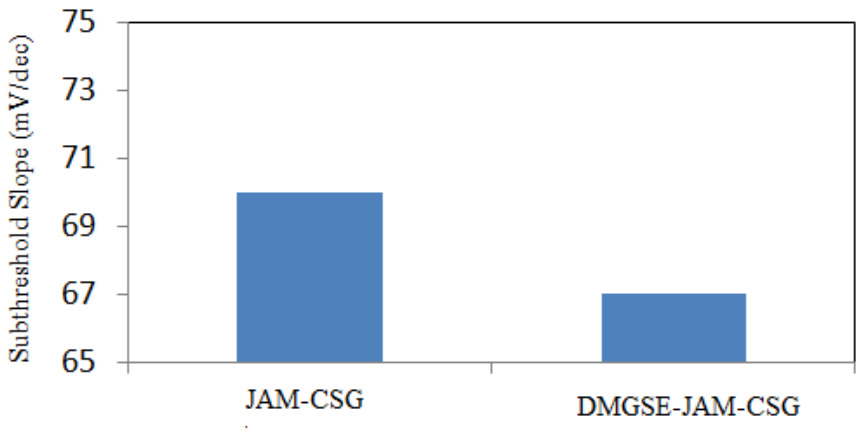


Figure 2.23 Subthreshold Slope for JAM-CSG and DMGSA-JAM-CSG MOSFET.

Figure 2.24 shows I_{on}/ I_{off} ratio for both the devices. This ratio is much higher for DMGSE-JAM-CSG MOSFET. All these parameters verify the excellence of DMGSE-JAM-CSG MOSFET over JAM-CSG MOSFET.

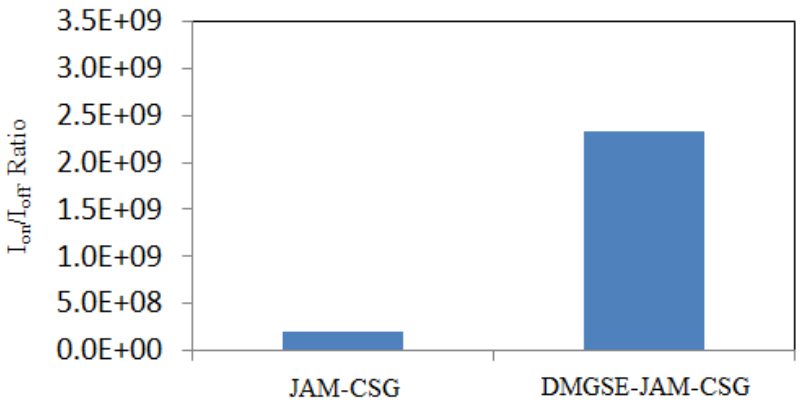


Figure 2.24 I_{on}/I_{off} ratio for JAM-CSG and DMGSE-JAM-CSG MOSFET.

The performance parameters of DMGSE-JAM-CSG MOSFET are compared with two available analogous devices namely Junctionless (JL) -CSG MOSFET and JAM-CSG MOSFET [35]. The I_{on}/I_{off} ratio and peak transconductance values of these devices for various dielectric constants (k= 3.9, 10 and 25) are listed in Table 2.4.

Table 2.4

Comparison of DMGSE-JAM-CSG MOSFET with Analogous Devices

Performance Parameter		**I_{on}/I_{off}**	**Peak g_m (S)**
JL-CSG	K=3.9	3.85E+06	2.13E-05
	K=10	1.33E+07	2.03E-05
	K=25	7.89E+07	1.98E-05
JAM-CSG	K=3.9	7.43E+07	4.27E-05
	K=10	1.04E+08	3.96E-05
	K=25	2.00E+08	3.80E-05
DMGSE-JAM-CSG	K=3.9	9.00E+08	8.96E-05
	K=10	1.09E+09	8.88E-05
	K=25	2.33E+09	9.73E-05

The table shows an improvement in parameters for over JL -CSG MOSFET and JAM-CSG MOSFET for various dielectric constants. As can be seen from the Table 2.4, there is a significant improvement in I_{on}/I_{off} ratio for DMGSE-JAM-CSG MOSFET as compared to the other two devices (JL-CSG and JAM-CSG). It has increased by 12, 10 and 11 times in context to JAM-CSG MOSFET for the dielectrics, k= 3.9, 10 and 25 respectively. Also, there is an increase in the value of transconductance (g_m) for the case of DMGSE-JAM-CSG MOSFET as compared to JL-CSG and JAM-CSG MOSFET. These values indicate the device is more robust and better suited for switching and high-frequency applications.

2.5 Summary

Utilizing 2-D Poisson's equation in cylindrical co-ordinates, an analytical model of DMGSE-JAM-CSG MOSFET is introduced. Influence of dual- gates and stack engineering on JAM MOSFET for analog/ RF applications has been examined for 40 nm channel length. The mathematical formulation for center potential, electric field, subthreshold current, transconductance and output conductance is put forward. The capability of the device has been observed by varying the gate stack materials. As, the dielectric constant increases, improvement in the device performance has also been observed. Results obtained reveals high I_{on}/I_{off} ratio, low subthreshold slope, high transconductance and low output conductance for the device when permittivity of the stack layer is increased. Also, the numerical results follow simulation results very closely. The device DMGSE-JAM-CSG MOSFET offers improvement in SCEs and HCEs. Results are also compared with JAM-CSG MOSFET and JL-CSG MOSFET. From the simulation results, it has been seen that the proposed structure, DMGSE-JAM-CSG MOSFET possesses better electrical properties than JAM-CSG and JL-CSG MOSFET. The subthreshold slope of this device is reduced and I_{on}/I_{off} ratio has increased, thus making the overall performance of this device much more powerful and more useful for high frequency and high amplification applications.

2.6 References

[1] Wong, H-S. Philip. "Beyond the conventional MOSFET." In *31st European Solid-State Device Research Conference*, pp. 69-72. IEEE, 2001.

[2] Fahad, Hossain M., and Muhammad M. Hussain. "High-performance silicon nanotube tunneling FET for ultralow-power logic applications." *IEEE transactions on electron devices* 60, no. 3 (2013): 1034-1039.

[3] Hong, Chuyang, Jun Zhou, Jiasheng Huang, Rui Wang, Wenlong Bai, James B. Kuo, and Yijian Chen. "A general and transformable model platform for emerging multi-gate MOSFETs." *IEEE Electron Device Letters* 38, no. 8 (2017): 1015-1018.

[4] Kumar, Manoj, Subhasis Haldar, Mridula Gupta, and R. S. Gupta. "Impact of gate material engineering (GME) on analog/RF performance of nanowire Schottky-barrier gate all around (GAA) MOSFET for low power wireless applications: 3D T-CAD simulation." *Microelectronics journal* 45, no. 11 (2014): 1508-1514.

[5] Sharma, Rupendra Kumar, Charalabos A. Dimitriadis, and Matthias Bucher. "A comprehensive analysis of nanoscale single-and multi-gate MOSFETs." *Microelectronics journal* 52 (2016): 66-72.

[6] Colinge, Jean-Pierre, Abhinav Kranti, Ran Yan, Chi-Woo Lee, Isabelle Ferain, Ran Yu, N. Dehdashti Akhavan, and Pedram Razavi. "Junctionless nanowire transistor (JNT): Properties and design guidelines." *Solid-State Electronics* 65 (2011): 33-37.

[7] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design." *IEEE Transactions on Device and Materials Reliability* 14, no. 1 (2014): 418-425.

[8] Holtij, Thomas, Michael Graef, Franziska Marie Hain, Alexander Kloes, and Benjamn Iñíguez. "Compact model for short-channel junctionless accumulation mode double gate MOSFETs." *IEEE Transactions on Electron Devices* 61, no. 2 (2013): 288-299.

[9] Choi, Ji Hun, Tae Kyun Kim, Jung Min Moon, Young Gwang Yoon, Byeong Woon Hwang, Dong Hyun Kim, and Seok-Hee Lee. "Origin of Device Performance Enhancement of Junctionless Accumulation-Mode

(JAM) Bulk FinFETs With High-$\kappa $ Gate Spacers." *IEEE Electron Device Letters* 35, no. 12 (2014): 1182-1184.

[10] Trivedi, Nitin, Manoj Kumar, Subhasis Haldar, S. S. Deswal, Mridula Gupta, and R. S. Gupta. "Analytical modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG)." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 29, no. 6 (2016): 1036-1043.

[11] Zeghbroeck, B. V. "Principles of semiconductor devices (2011)." URL http://ecee. colorado. edu/~ bart/book (2015).

[12] Darwin, S., and TS Arun Samuel. "A holistic approach on Junctionless dual material double gate (DMDG) MOSFET with high k gate stack for low power digital applications." *silicon* 12, no. 2 (2020): 393-403.

[13] Amin, S. Intekhab, and R. K. Sarin. "Charge-plasma based dual-material and gate-stacked architecture of junctionless transistor for enhanced analog performance." *Superlattices and Microstructures* 88 (2015): 582-590.

[14] Chebaki, E., F. Djeffal, H. Ferhati, and T. Bentrcia. "Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions." *Superlattices and Microstructures* 92 (2016): 80-91.

[15] Sarkar, A., Das, A. K., De, S., & Sarkar, C. K. (2012). Effect of gate engineering in double-gate MOSFETs for analog/RF applications. *Microelectronics Journal*, *43*(11), 873-882.

[16] W. Long and K. K. Chin, "Dual Material Gate Field Effect Transistor (DMGFET)," *International Electron Devices Meeting Technical Digest*, pp. 549-552, 1997.

[17] Najmzadeh, Mohammad, Didier Bouvet, Wladyslaw Grabinski, J-M. Sallese, and A. M. Ionescu. "Accumulation-mode gate-all-around Si nanowire nMOSFETs with sub-5 nm cross-section and high uniaxial tensile strain." *Solid-state electronics* 74 (2012): 114-120.

[18] Xiao-Shi, Jin, Liu Xi, Kwon Hyuck-In, and Lee Jong-Ho. "A continuous current model of accumulation mode (junctionless) cylindrical surrounding-gate nanowire MOSFETs." *Chinese Physics Letters* 30, no. 3 (2013): 038502.

[19] ATLAS, Device Simulator. "Silvaco International. Santa Clara." (2015).

[20] Roy, Nirmal Ch, Abhinav Gupta, and Sanjeev Rai. "Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra low-power analog/RF circuits." *Microelectronics Journal* 46, no. 10 (2015): 916-922.

[21] Holtij, Thomas, Mike Schwarz, Alexander Kloes, and Benjamin Iniguez. "Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region." *Solid-state electronics* 90 (2013): 107-115.

[22] Gautam, Rajni, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localised charges." *Journal Of Computational and Theoretical Nanoscience* 9, no. 4 (2012): 602-610.

[23] Jiang, Chunsheng, Renrong Liang, Jing Wang, and Jun Xu. "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs." *AIP Advances* 5, no. 5 (2015): 057122.

[24] Li, Cong, Yiqi Zhuang, Ru Han, and Gang Jin. "Subthreshold behavior models for short-channel junctionless tri-material cylindrical surrounding-gate MOSFET." *Microelectronics Reliability* 54, no. 6-7 (2014): 1274-1281.

[25] Goel, Anubha, Sonam Rewari, Seema Verma, and R. S. Gupta. "Physics-based analytic modeling and simulation of gate-induced drain leakage and linearity assessment in dual-metal junctionless accumulation nano-tube FET (DM-JAM-TFET)." *Applied Physics A* 126, no. 5 (2020): 1-14.

[26] Gnudi, A., S. Reggiani, E. Gnani, and G. Baccarani. "Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs." *IEEE Electron Device Letters* 33, no. 3 (2012): 336-338.

[27] Duarte, Juan Pablo, Sung-Jin Choi, and Yang-Kyu Choi. "A full-range drain current model for double-gate junctionless transistors." *IEEE transactions on electron devices* 58, no. 12 (2011): 4219-4225.

[28] Ahmadivand, Arash, Burak Gerislioglu, and Zeinab Ramezani. "Gated graphene island-enabled tunable charge transfer plasmon terahertz metamodulator." *Nanoscale* 11, no. 17 (2019): 8091-8095.

[29] Wouters, Dirk J., J-P. Colinge, and Herman E. Maes. "Subthreshold slope in thin-film SOI MOSFETs." *IEEE Transactions on Electron Devices* 37, no. 9 (1990): 2022-2033.

[30] Colinge, J-P. "Subthreshold slope of thin-film SOI MOSFET's." *IEEE Electron Device Letters* 7, no. 4 (1986): 244-246.

[31] E. S. Yang, "Microelectronic Devices", *McGraw-Hill*, New York, 1988, pp. 285-294.

[32] K.K. Young, "Short Channel Effect in Fully Depleted SOI MOSFET", *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 399-402, 1989.

[33] Pravin, J. Charles, D. Nirmal, P. Prajoon, and J. Ajayan. "Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications." *Physica E: Low-dimensional systems and nanostructures* 83 (2016): 95-100.

[34] Rewari, Sonam, Subhasis Haldar, Vandana Nath, S. S. Deswal, and R. S. Gupta. "Numerical modeling of Subthreshold region of junctionless double surrounding gate MOSFET (JLDSG)." *Superlattices and Microstructures* 90 (2016): 8-19.

[35] Trivedi, Nitin, Manoj Kumar, Mridula Gupta, Subhasis Haldar, S. S. Deswal, and R. S. Gupta. "Investigation of analog/RF performance of High-k spacer junctionless accumulation-mode cylindrical gate all around (JLAM-CGAA) MOSFET." In *2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON)*, pp. 201-205. IEEE, 2016.

CHAPTER 3

Temperature Dependency and Linearity Assessment of Dual- Metal Gate Stack Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGS-JAM-CSG) MOSFET

3.1 Introduction

As already mentioned, MOSFETs are approaching nanometer scale and due to scaling, a problem called as Short Channel Effects (SCEs) arises. SCEs brings about the degradation in the performance of the MOSFETs [1-2]. To overcome this problem, several multigate MOSFET topologies, that is, Double-Gate (DG), Tri-Gate (TG), Cylindrical Surrounding Gate (CSG) MOSFETs [3-5] were introduced. These topologies provide improved behavior when compared with the conventional one. The CSG is the superior among all these because of the presence of gate all over the silicon film, which offers extended gate control. But it also holds a drawback of development of sharp source-drain junctions. For elimination of the above-stated problem, Junctionless Transistor (JLT) was introduced in 2010 [6]. In JLT, uniform doping is done all over the MOSFET, because of which no source-channel and drain-channel junctions are formed. This makes the fabrication process simpler and less expensive. But JLT also possesses lower drain current and transconductance because of the Carrier Mobility Degradation (CMD) [7]. So, for improved drain current and transconductance, another MOSFET called Junctionless Accumulation Mode (JAM) MOSFET was proposed. In this MOSFET, non-uniform doping is done, i.e., channel is slightly less doped as compared to source/drain [8-9]. The JAM MOSFET possesses better electrical characteristics, more conductivity and less SCEs in contrast to JLT. To decrease the SCEs further, double gates and a gate stack [10-12] are introduced to JAM MOSFET, proposing a new structure called Dual- Metal Gate Stack (DMGS) JAM- CSG MOSFET.

Temperature is one of the important parameter which influences the characteristics of the MOSFET [13]. Therefore, dependency of temperature upon our proposed structure,

introduced in chapter 2, needs to be examined. Therefore, in this chapter the temperature is varied and the changes upon the electrical characteristics of our proposed device have been studied. Thus, it is inferred in this chapter whether the device will be able to work at other temperatures as well with good efficiency or not. This also defines the applicability of the device in different environmental conditions. Also, whether the device is suitable for various RF applications i.e., wireless, radio networking, etc., linearity of the device needs to be assessed. For this, various Linearity Assessment Parameters for our proposed device have been evaluated in this chapter to see if the device possesses high linearity and is suitable for numerous RF applications. Influence of temperature and linearity assessment of the device is now being studied in detail in the forthcoming sections.

3.1.1 Temperature Dependency Phenomenon

When MOSFET is utilized for the applications including space communication, satellite communication, infrared detectors, etc., temperature plays a significant role. As, the change in temperature varies the performance of the MOSFET, therefore, it becomes important to examine the impact of temperature upon the various characteristic aspects of the MOSFET [14]. Therefore, to study the influence of temperature [15] on our proposed structure i.e., DMDG-JAM-CSG MOSFET, we have developed this structure's temperature- dependent physics- based analytical model using the applicable boundary conditions. Also, we have examined the improved performance of DMGS-JAM- CSG MOSFET over JAM-CSG MOSFET by analyzing its various analog performance parameters.

3.1.2 Linearity Assessment Phenomenon

In addition to the analog performance analysis, we have also performed the linearity assessment of the device. Nowadays, semiconductors are being utilized for numerous RF applications [16-18] including wireless networks, radio broadcasting, navigation, etc. For improved performance of these applications, they require intermodulation and higher order harmonics to be minimum because if distortion is present, then it will lead to the generation of undesirable (noise) signals which may alter the output signal [17]. Therefore, linearity analysis is very essential for RF systems. Various techniques are there to confirm high linearity. Determination of linearity characteristics is also performed through experiments but this is a high cost and time consuming affair.

Another method which is very effective and less time consuming is by evaluating several Figure of Merits (FOMs). The FOMs includes second-order and third-order Voltage Intercept Points (VIP2, VIP3), third-order Intercept Input Power (IIP3), third-order Intermodulation Distortion (IMD3) and higher order transconductances. So, we have performed the linearity analysis of the device by determining these various FOMs.

3.2 Device Description, Simulation Methodology and Calibration

3.2.1 Device Description

Figure 3.1 represents the 2-D structural view of proposed DMGS-JAM-CSG MOSFET. The channel is slightly less doped in comparison to source/drain with n-type doping. It consists of dual gates (gate1 and gate2) of different workfunctions, ϕ_1 and ϕ_2 respectively such that $\phi_1 > \phi_2$. Also, a high-*k* material HfO_2 along with SiO_2 is also present as a gate stack.

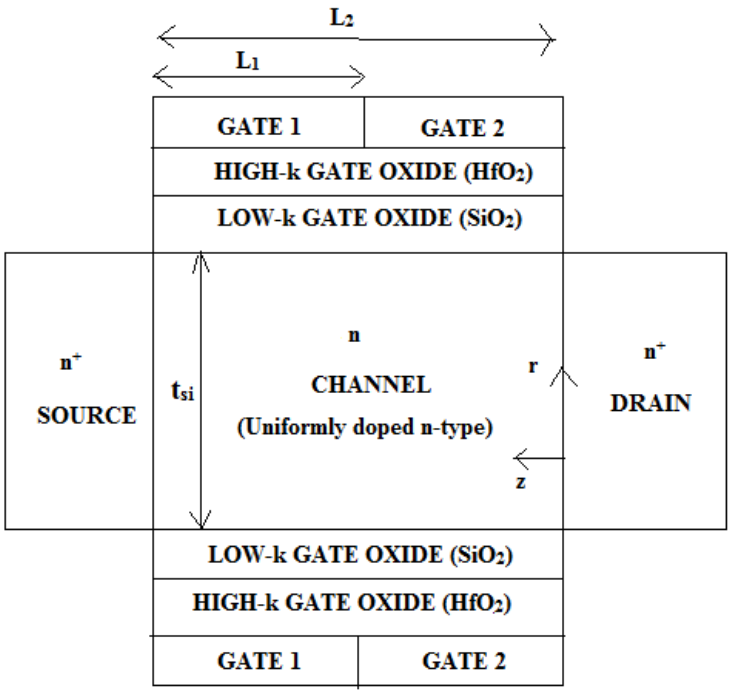


Figure 3.1 2-D view of DMGS-JAM-CSG MOSFET.

Here, thickness of SiO_2, t_{ox} is 1nm and thickness of HfO_2, t_{hk} is 1nm. Thus, the effective oxide thickness, t_{oxeff} is calculated as:

$$t_{oxeff} = t_{ox} + \frac{\varepsilon_{ox} \cdot t_{hk}}{\varepsilon_{hk}} \tag{3.1}$$

where, ε_{ox}, ε_{hk} are the permittivities of SiO_2 and HfO_2 respectively and are equal to 3.9 and 25 respectively. Table 3.l summarizes the various structural parameters employed for proposed DMDG-JAM-CSG MOSFET and JAM-CSG MOSFET.

Table 3.1

Structural Parameters of JAM-CSG and DMGS-JAM-CSG MOSFET

Parameter	**JAM-CSG**	**DMGS-JAM-CSG**
Channel Length	50 nm	50 nm
Channel Doping	$10^{18}/cm^3$	$10^{18}/cm^3$
Source/Drain Doping	$10^{20}/cm^3$	$10^{20}/cm^3$
Gate Oxide Material	SiO_2	SiO_2 AND HfO_2
Gate Stack Oxide Thickness	SiO_2- 2 nm	SiO_2- 1 nm
Silicon Pillar Thickness	20 nm	20 nm
Work- Function	Φ = 4.8 eV	$\phi_1 = 5.0$ eV (Rhodium) $\phi_2 = 4.8$ eV (Ruthenium)

3.2.2 Models Utilized

For performing the simulation, ATLAS-3D device simulator has been employed with the following models: Recombination Model for considering minority recombination effects, Concentration Dependent Mobility Model for relating the low-field mobility to the impurity concentration, Band To Band Tunneling Model for inclusion of tunnelling effect, Boltzmann Model is used to consider the Carrier Statistics, Newton and Gummel methods for the numerical solution. Table 3.2 enumerates several physical models and methods utilized while performing simulation on ATLAS 3-D simulator [19].

3.2.3 Device Calibration

Figure 3.2 shows the calibration of the simulation data of our model with the experimental work carried out by Choi et al. [20], considering the same cross-sectional area. Extraction of the experimental data [20] has been carried out by utilizing the Graph Digitizer tool and then using the extracted data, the experimental graph has been

plotted. It may be noticed the Figure 3.2 that both the simulated and experimental results match closely with each other.

Table 3.2

Physical Models Used

Physical models	**Description**
Recombination Model	The Shockley– Read– Hall recombination model (with carrier lifetime $1x10^{-7}$ s) is included in simulation to incorporate minority recombination effects. The SRH model considers carrier lifetimes.
Concentration Dependence Model	Considers SRH recombination along with their lifetimes. CONMOB relates the low-field mobility to the impurity concentration.
Band To Band Tunneling (BTBT) Model	For direct transitions. Required with very high fields. BTBT model inculcates tunnelling effect of the charge carriers.
Mobility Model	Field-Dependent Mobility Model (FLDMOB) has been used in the analysis to accommodate the velocity saturation effect.
Statistics	Boltzmann Model is used because it considers the Carrier Statistics.
Methods	The Newton and Gummel methods are simultaneously invoked for the numerical solution.

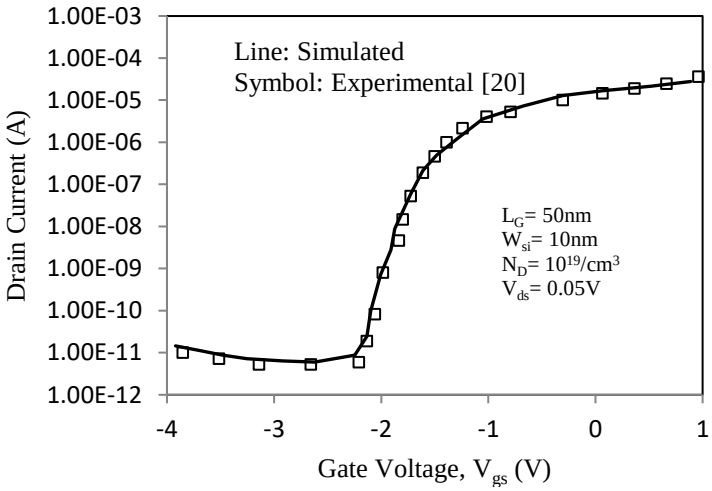


Figure 3.2 Calibration of simulated data of our model with the experimental data [20].

3.3 Analytical Model

For investigating the effect of temperature variation upon various device characteristics, potential distribution model of the device is developed using the 2-D Poisson's equation, stated as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\psi_i(r,z,T)}{\partial r}\right)+\frac{\partial^2\psi_i(r,z,T)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}},\quad i=1,2 \tag{3.2}$$

where, T be the temperature measured in Kelvin (K), $\psi_i(r,z,T)$ represents the potential distribution, r and z are the distances across the radial and vertical axis respectively, q is the electronic charge, N_D be the channel doping and ε_{si} is the permittivity of SiO_2.

Using parabolic potential approximation (PPA) technique, the potential is calculated as:

$$\psi_i(r,z,T)=P_{i0}(z)+P_{i1}(z)\,r+P_{i2}(z)\,r^2,\quad 0\leqslant z\leqslant L_2 \tag{3.3}$$

Solution of the above potential equation is acquired by administering the subsequent boundary conditions:

(1) Center potential :

$$\psi_i(r=0,z,T)=\psi_c \tag{3.4}$$

(2) Field is zero at the center:

$$\frac{\partial\psi_i(r,z,T)}{\partial r}\Big|_{r=0}=0 \tag{3.5}$$

(3) Surface potential:

$$\psi_i\left(r=\frac{t_{si}}{2},z,T\right)=\psi_s\left(\frac{t_{si}}{2},z,T\right) \tag{3.6}$$

(4) Surface field:

$$\frac{\partial\psi_i\left(\frac{t_{si}}{2},z,T\right)}{\partial r}=\frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs}-V_{fb}-\psi_i\left(\frac{t_{si}}{2},z,T\right)\right] \tag{3.7}$$

(5) Potential present towards source side:

$$\psi_1(r,0,T)=V_{bi} \tag{3.8}$$

(6) Potential present towards drain side:

$$\psi_2(r, L_2, T) = V_{bi} + V_{ds} \tag{3.9}$$

(7) Potential is continous at the interface of both the gates:

$$\psi_{s_1}(r, L_1, T) = \psi_{s_2}(r, L_1, T) \tag{3.10}$$

(8) Continuity of electric field at the interface:

$$\frac{\partial \psi_{s_1(r,L_1,T)}}{\partial r} = \frac{\partial \psi_{s_2(r,L_1,T)}}{\partial r} \tag{3.11}$$

where, capacitance per unit area, $C_{ox} = \frac{2\varepsilon_{ox}}{t_{si} \ln\left[1+\left(\frac{2t_{oxeff}}{t_{si}}\right)\right]}$ (3.12)

V_{bi} represents the built-in potential; t_{si} be the width of the silicon film and V_{ds} be the drain to source voltage.

On applying the above boundary conditions, the coefficients $P_{0i}(z)$, $P_{1i}(z)$ and $\mathrm{P_{2i}(z)}(i = 0, 1, 2)$ we obtained are:

$$P_{10}(z) = \psi_{c_1}(z) \tag{3.12a}$$

$$P_{20}(z) = \psi_{c_2}(z) \tag{3.12b}$$

$$P_{11}(z) = 0 \tag{3.12c}$$

$$P_{21}(z) = 0 \tag{3.12d}$$

$$P_{12}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z, T)\right] \tag{3.12e}$$

$$P_{22}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z, T)\right] \tag{3.12f}$$

Now, using the above coefficient values, the center potential specified by equation (3.3) is rewritten as:

$$\psi_1(r, z, T) = \psi_{c_1}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z, T)\right] \tag{3.13a}$$

$$\psi_2(r, z, T) = \psi_{c_2}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z, T)\right] \tag{3.13b}$$

where, ψ_{gs_1}, ψ_{gs_2} are the gate to source potentials across gate1 and gate2 respectively.

At $r = \frac{t_{si}}{2}$, $\psi_i\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{si_i}(r = \frac{t_{si}}{2}, z, T)$, so the equations (3.13a) and (3.13b) for ψ_{si_1} and ψ_{si_2} becomes:

$$\psi_{si_1}\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{c_1(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_1} - \psi_{si_1}(r=\frac{t_{si}}{2}, z, T)}{\varepsilon_{si} t_{si}}\right) \tag{3.14a}$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r=\frac{t_{si}}{2}, z, T)}{\varepsilon_{si} t_{si}}\right) \tag{3.14b}$$

Rearranging the terms in (3.14a) and (3.14b) yields

$$\psi_{si_1}(r = \frac{t_{si}}{2}, z, T) = \left[\frac{4\varepsilon_{si}\psi_{c_1(z)} + t_{si} C_{ox}\psi_{gs_1}}{4\varepsilon_{si} + t_{si} C_{ox}}\right] \tag{3.15a}$$

$$\psi_{si_2}(r = \frac{t_{si}}{2}, z, T) = \left[\frac{4\varepsilon_{si}\psi_{c_2(z)} + t_{si} C_{ox}\psi_{gs_2}}{4\varepsilon_{si} + t_{si} C_{ox}}\right] \tag{3.15b}$$

The JLT works on bulk to source conduction mechanism, therefore, the center potential is to be calculated for *r* = 0. Center potential for two different metals is solved as:

$$\frac{\partial^2 \psi_{c_1}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_1(z)} - \eta_1\right], \qquad 0 \leqslant z \leqslant L_1 \tag{3.16a}$$

$$\frac{\partial^2 \psi_{c_2}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_2(z)} - \eta_2\right], \qquad L_1 \leqslant z \leqslant L_2 \tag{3.16b}$$

where, the characteristic length (λ), η_1 and η_2 are respectively given by

$$\frac{1}{\lambda^2} = \frac{16\, C_{ox}}{4\varepsilon_{si} t_{si} + {t_{si}}^2 C_{ox}} \tag{3.17}$$

$$\eta_1 = \psi_{gs_1} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{3.18a}$$

$$\eta_2 = \psi_{gs_2} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{3.18b}$$

General solution of center potential, $\psi_{ci}(r, z, T)$ was obtained as:

$$\psi_{ci}(r, z, T) = \begin{cases} \psi_{c1}(r, z, T) \;\; for\; 0 \leqslant z \leqslant L_1 \\ \psi_{c2}(r, z, T) for\; L_1 \leqslant z \leqslant L_2 \end{cases} \tag{3.19}$$

$$\psi_{C1}(r, z, T) = A\, e^{z/\lambda} + B e^{-z/\lambda} + \eta_1 \tag{3.20a}$$

$$\psi_{C2}(r, z, T) = C\, e^{z/\lambda} + D e^{-z/\lambda} + \eta_2 \tag{3.20b}$$

where, the coefficients *A*, *B*, *C* and *D* we obtained are given by,

$$A = \frac{e^{-L_1/\lambda}(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{-L_1/\lambda}-e^{L_1/\lambda})} \tag{3.21a}$$

$$B = \frac{e^{L_1/\lambda}(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{L_1/\lambda}-e^{-L_1/\lambda})} \tag{3.22b}$$

$$C = \frac{e^{-L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{-L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_1-L_2)/\lambda}-e^{(L_2-L_1)/\lambda}} \tag{3.23c}$$

$$D = \frac{e^{L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_2-L_1)/\lambda}-e^{(L_1-L_2)/\lambda}} \tag{3.24d}$$

Temperature affects the parameters and performance of the device [21, 22]. Various temperature sensitive parameters are:

Band Gap Energy (E_g):

$$E_g(T) = Eg(0) - \frac{\alpha T^2}{T+\beta} \tag{3.25}$$

where, $Eg(0) = 1.166\ eV, \alpha = 4.73 \text{ x } 10^{-4} eV/K, \beta = 636K$..

Intrinsic carrier concentration (n_i):

$$n_i(T) = 1.706 \text{ x } 10^{25} \left(\frac{T}{300}\right)^{3/2} exp\left(\frac{-qE_g(T)}{kT}\right) \tag{3.26}$$

Permittivity of silicon:

$$\varepsilon_{si}(T) = 11.4 + (1 + 1.2 \text{ x } 10^{-4}T) \tag{3.27}$$

Fermi Potential:

$$\phi_f(T) = \frac{kT}{q} ln\left(\frac{N_D}{n_i(T)}\right) \tag{3.28}$$

Flat- band voltage:

$$V_{fb}(T) = \phi_m - \phi_s(T) \tag{3.29}$$

where, work-function of the semiconductor, $\phi_s(T)$ is given as:

$$\phi_s(T) = \frac{E_g(T)}{2} + \chi - q\phi_f(T) \tag{3.30}$$

Another important parameter affected due to temperature is mobility. Caughey and Thomas function [23] for modelling mobility, considering the effect of temperature is expressed as:

$$\mu_{Caug} = \mu_1 + \frac{\mu_2\left(\frac{T}{300}\right)^{\beta} - \mu_1}{1+\left(\frac{T}{300}\right)^{\gamma}\left(\frac{N_a}{N_{crit}}\right)^{\delta}} \tag{3.31}$$

where, μ_1= 55.24 cm^2/Vs, μ_2= 240 cm^2/Vs, β= -2.3, γ=- 3.8, N_{crit}= 1.072 x 10^{17} cm^{-3}.

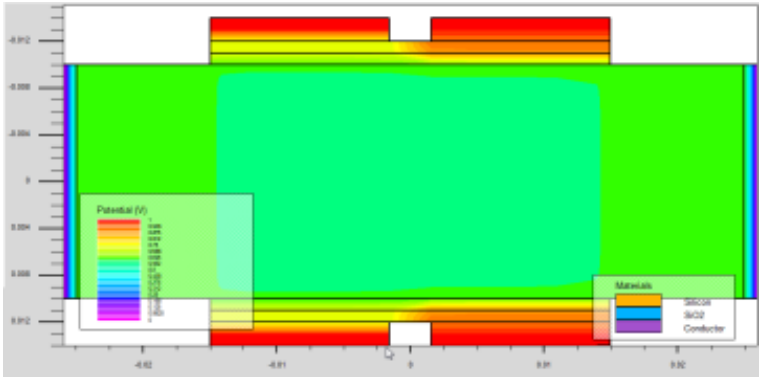
Electric Field distribution is given as:

$$E_i(r,z,T) = -\frac{d\psi_i(r,z,T)}{dz} \tag{3.32}$$

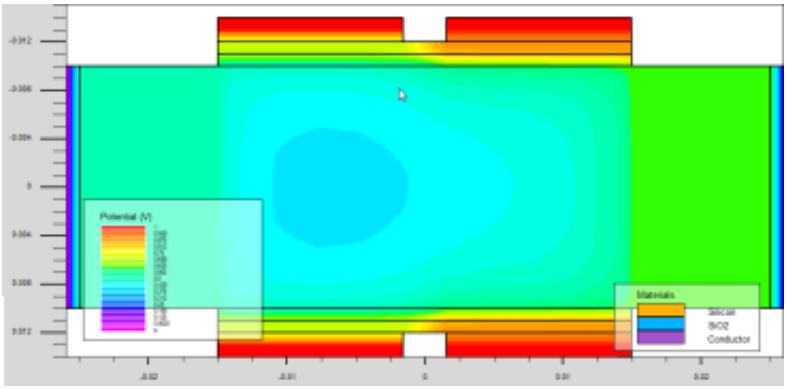
3.4 Results and Discussion

3.4.1 DMGS-JAM-CSG MOSFET Model

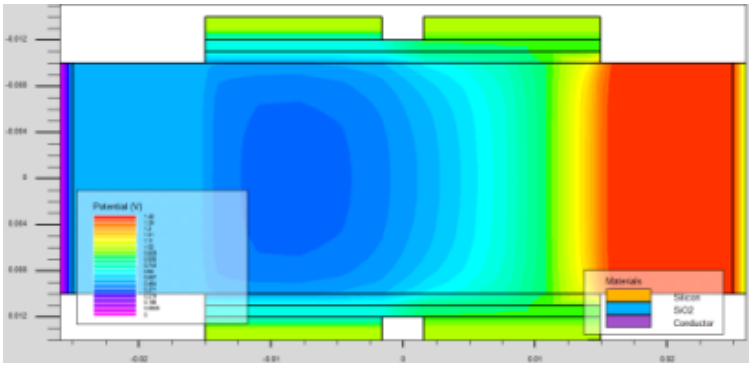
Figures 3.3(a), (b) and (c) displays the contour plots of the potential for DMGS-JAM-CSG MOSFET with V_{gs}= 1.0V and V_{ds}= 0.1V at T= 100K, 300K and 500K respectively. From the figure, it is seen that as the temperature is increasing from 100K to 500K, the potential is getting lowered down. With the rise in temperature, the intrinsic carrier concentration increases which results in the reduction of the potential across the channel [24]. This is due to increase in the mobility of the carriers because of the Fermi level shift towards the bandgap.



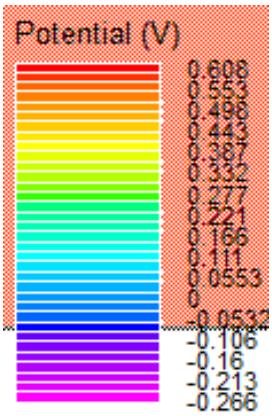
(a)



(b)



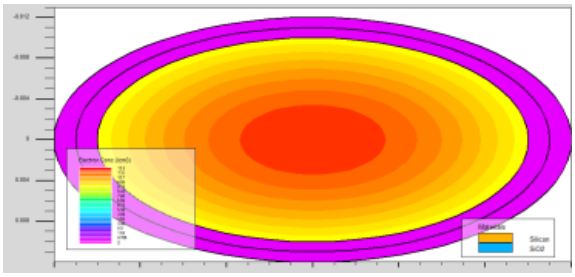
(c)



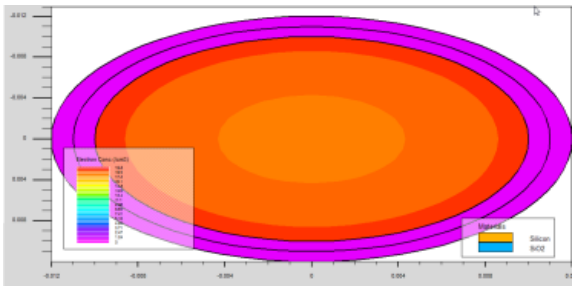
(d)

Figure 3.3 Potential contour plot for DMGS-JAM-CSG MOSFET at V_{gs}= 1.0V and V_{ds}= 0.1V for various temperatures (a) 100K (b) 300K (c) 500K and (d) color coding scale.

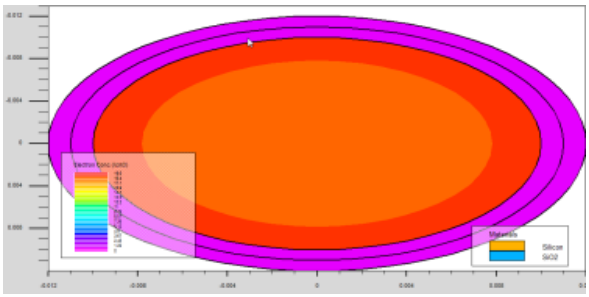
Contour plots for electron concentration for DMGS-JAM-CSG MOSFET when V_{gs}= 1.0V and V_{ds}= 0.1V at (a) T= 100K (b) T= 300K and (b) T= 500K is depicted in Figures 3.4(a), (b) and (c) respectively.



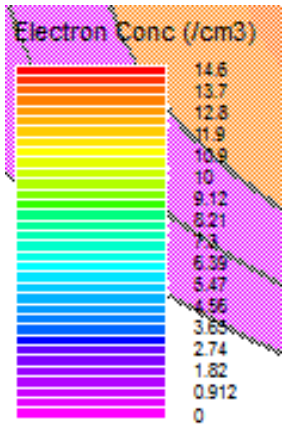
(a)



(b)



(c)



(d)

Figure 3.4 Contour plot for electron concentration of DMGS-JAM-CSG MOSFET at the channel's surface at V_{gs}= 1.0V and V_{ds}= 0.1V for various temperatures (a) 100K (b) 300K (c) 500K and (d) color coding scale.

From the Figure 3.4, it is noted that when temperature is increasing from 100K to 500K, the concentration of the electrons is also increasing [24]. The increase in temperature brings about movement of Fermi level towards the bandgap. This results in increase in the mobility of the carriers and thus, increment in electron concentration.

Figure 3.5 depicts the electron velocity for DMGS-JAM-CSG MOSFET across the channel length at distinct temperatures (*T*= 100K, 300K and 500K). It is noted that as the temperature is increased, the electron velocity decreases. For *T*= 100K, the electron velocity reaches the maximum value of 1.88E+07 cm/s and for *T*= 500K, it reaches 1.29E+07 cm/s. The reason behind this is that the mobility of the electrons increases due to the increment in temperature. Thereby, the number of collisions of electrons increases, leading towards the decrease of electron velocity.

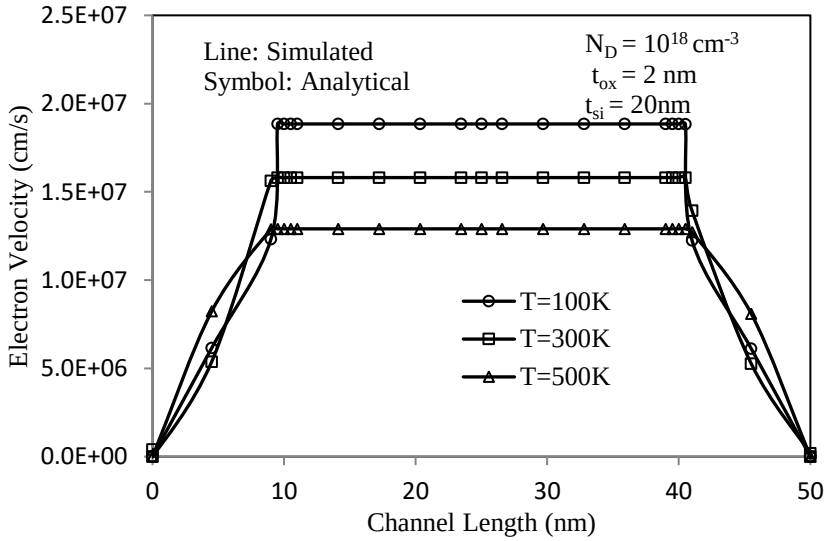


Figure 3.5 Electron velocity variation in DMGS-JAM-CSG MOSFET with channel length at *T*= 100K, 300K and 500K.

Variation of the potential for DMGS-JAM-CSG MOSFET across the channel at various temperatures (*T*= 100K, 300K and 500K) is depicted in Figure 3.6. It is observed that as the temperature is incremented, the center potential is lowered down. The potential is lowered down from 25 mV (at *T*= 100K) to -23 mV (at *T*= 500K). This lowering down of potential is owing to the increase in the carrier concentration with the increment in temperature. This reduction in potential indicates lowering down of the threshold voltage, which makes the device to turn ON faster.

Electric field along the channel at distinct temperatures (*T*= 100K, 300K and 500K) for DMGS-JAM-CSG MOSFET is depicted in Figure 3.7. It is observed that as the increment in the temperature takes place, an elevation in the electric field occurs towards the source side and decrease towards the drain side. This leads to minimized SCEs and Hot Carrier Effects. The reason behind this is the increment in the amount of charge carriers, when there is a rise in temperature.

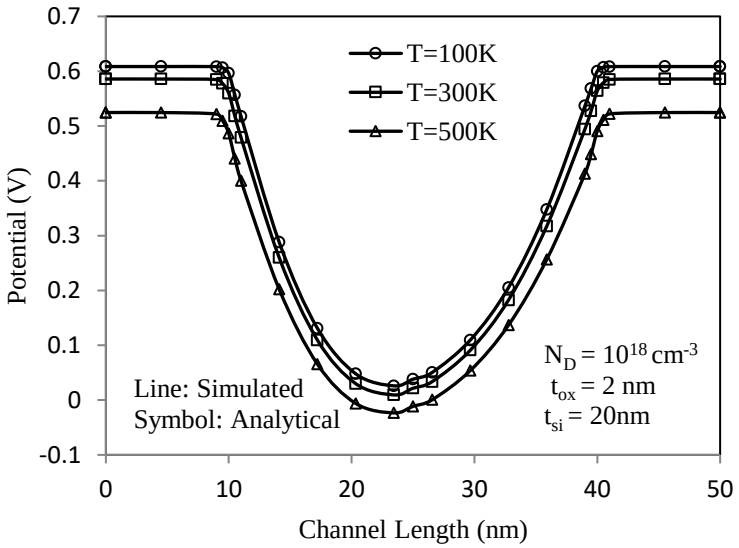


Figure 3.6 Potential variation in DMGS-JAM-CSG MOSFET with channel length at different temperatures (*T*= 100K, 300K and 500K).

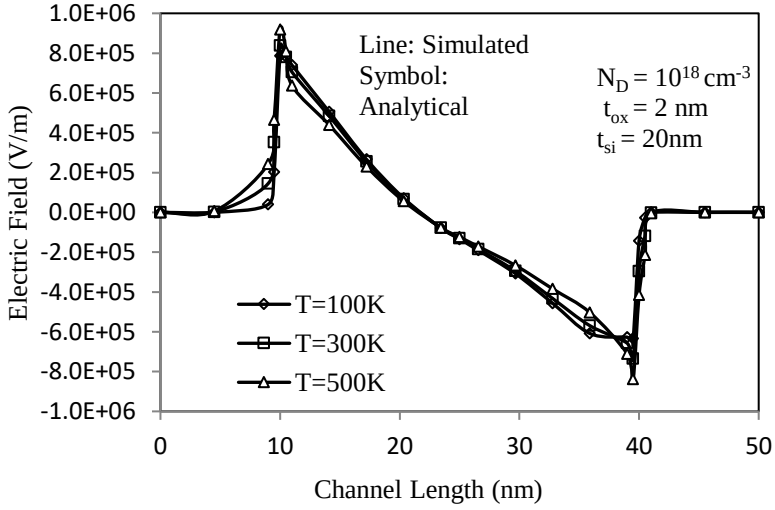


Figure 3.7 Electric field variation in DMGS-JAM-CSG MOSFET with channel length at different temperatures (*T*= 100K, 300K and 500K).

3.4.2 Comparison with analogous device

Transfer characteristics (I_{ds} vs V_{gs}) [25-26] for DMDG-JAM-CSG and JAM-CSG MOSFET at V_{ds}= 0.1V and 1.0V is shown in Figure 3.8. From the figure, we can make out that DMGS-JAM-CSG MOSFET owns better transfer characteristics. Further, from the Figure 3.8, it is visible that when V_{ds} is changed from 0.1V to 1.0 V, threshold voltage is getting lowered down. This indicates the DIBL effect.

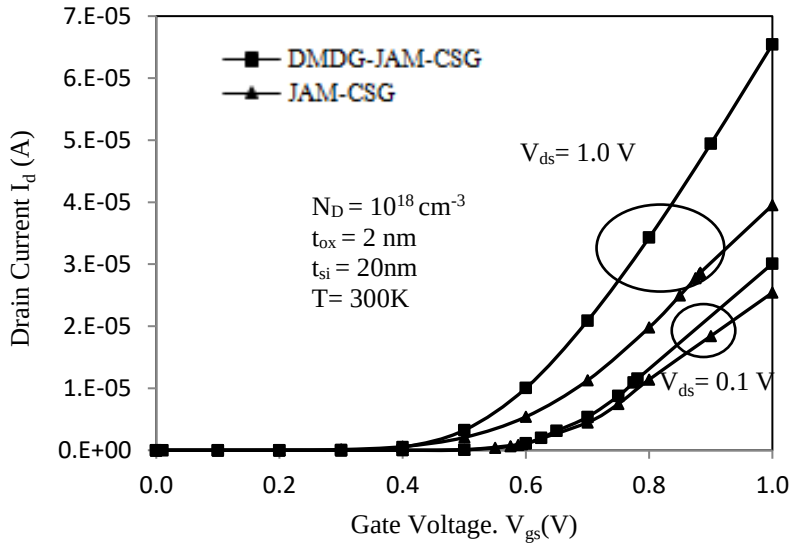


Figure 3.8 Transfer characteristics (I_d vs V_{gs}) curve for DMDG-JAM-CSG and JAM-CSG MOSFET.

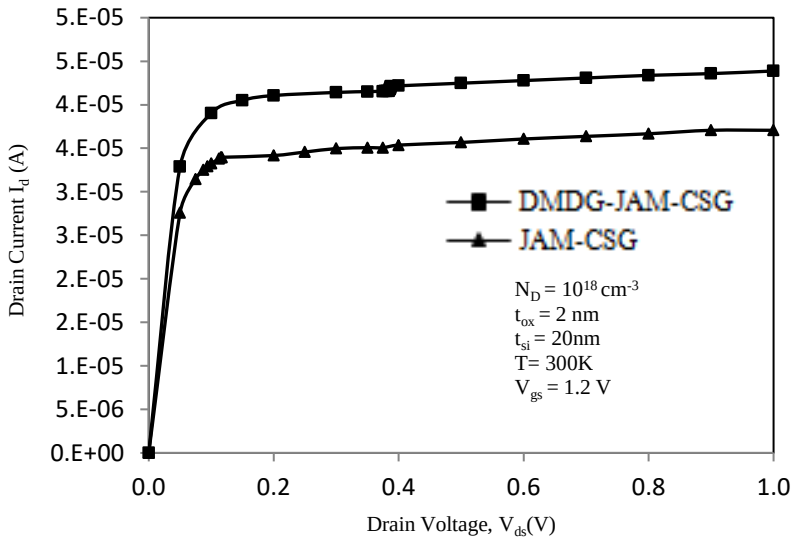


Figure 3.9 Output characteristics (I_d vs V_{ds}) curve for DMDG-JAM-CSG and JAM-CSG MOSFET.

Output characteristics (I_{ds} vs V_{ds}) for DMGS-JAM-CSG and JAM-CSG at V_{gs} = 1.2 V is depicted in Figure 3.9. This figure shows that the DMGS-JAM-CSG MOSFET obtains

higher drain current compared to JAM-CSG MOSFET. The reason behind this increased drain current is that when gate voltage is applied, an electric field is produced inside the channel and when this applied voltage overruns the flat band voltage, the charge carriers starts accumulating which makes the current to pass through the center of the channel. DMGS-JAM-CSG MOSFET possesses increased gate control over the channel, thereby resulting in faster accumulation of the charge carriers causing high flow of drain current.

Transconductance (g_m) [27] is another vital parameter given by:

$$g_m = \left(\Delta I_{ds}/\Delta V_{gs}\right)|_{V_{ds=constant}} \tag{3.33}$$

Figure 3.10 represents the g_m with respect to V_{gs} at V_{ds} = 0.2 V. It is noted that this parameter is higher for the DMDG-JAM-CSG MOSFET. Therefore, it can be used for applications requiring high gain amplification.

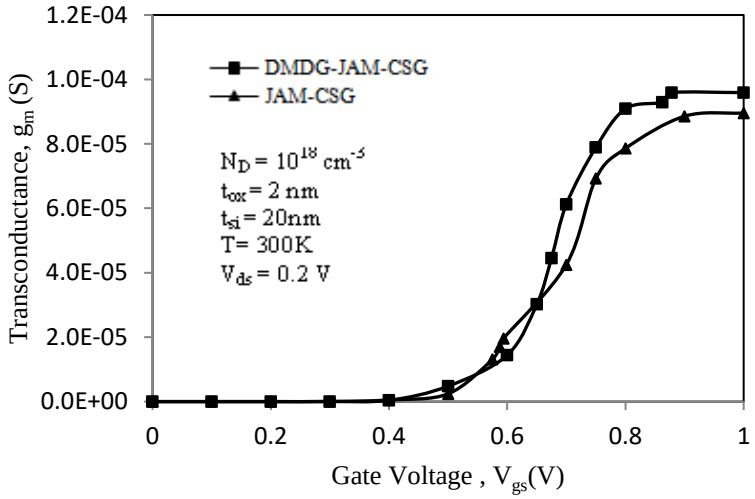


Figure 3.10 Variation of Transconductance, g_m with gate voltage, V_{gs} for DMDG-JAM-CSG and JAM-CSG MOSFET.

Next parameter is Transconductance Generation Factor (TGF) [28] or device efficiency, given by:

$$\text{TGF} = g_m/I_{ds} \tag{3.34}$$

TGF with respect to gate voltage is indicated in Figure 3.11. From the Figure 3.11, higher TGF is seen for DMGS-JAM-CSG MOSFET, signifying its capability to amplify

a signal more effectively. Thus, DMGS-JAM-CSG MOSFET proves to be more suitable for high amplification applications.

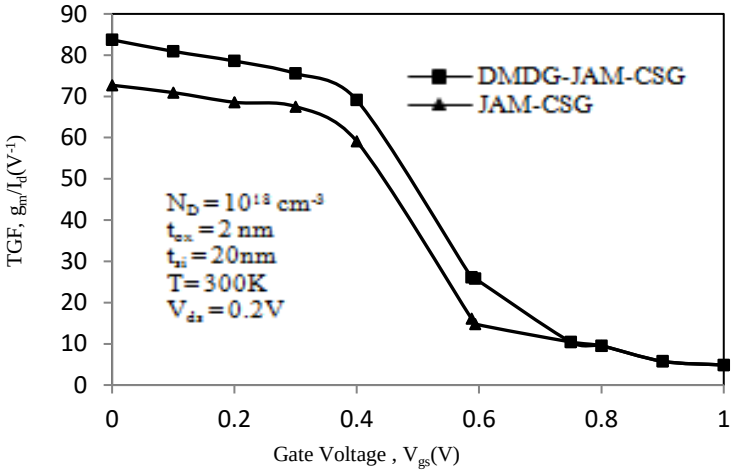


Figure 3.11 Variation of TGF with gate voltage, V_{gs} for DMDG-JAM-CSG and JAM-CSG MOSFET.

Output conductance is given as [27]:

$$g_d = (\Delta I_{ds}/\Delta V_{ds})|_{V_{gs=constant}} \tag{3.35}$$

Figure 3.12 represents the variation of output conductance, g_d with V_{ds} for both the devices. Output conductance is more for DMGS-JAM-CSG MOSFET in comparison to JAM-CSG MOSFET.

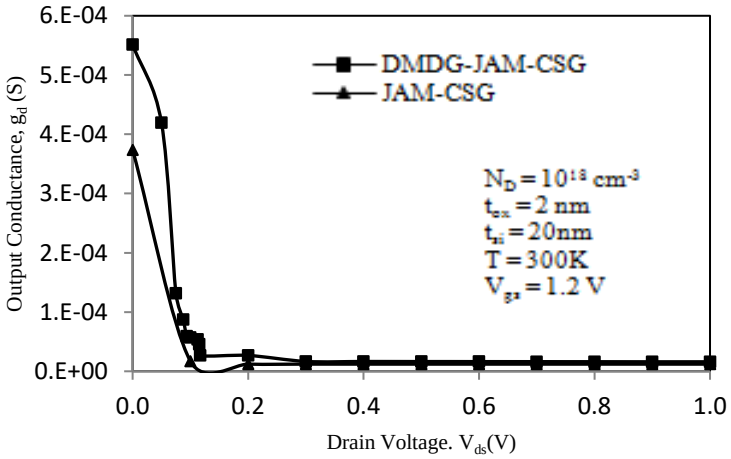


Figure 3.12 Variation of Output Conductance with Drain Voltage for DMDG-JAM-CSG and JAM-CSG MOSFET

Early voltage [28] is also major parameter for a MOSFET. It refers to the immunity of the MOSFET towards the Channel Length Modulation (CLM) effect and is stated as:

$$V_A = I_d / g_d \tag{3.36}$$

Early voltage with respect to V_{ds} is depicted in Figure 3.13. For DMGS-JAM-CSG MOSFET, the increase in the drain current is more as compared to the decrease in the output conductance. Therefore, from the Figure 3.13 also, it can be seen that early voltage for DMGS-JAM-CSG MOSFET has been improved and thus is more immune towards CLM effect, which is dominant in short-channel MOSFETs.

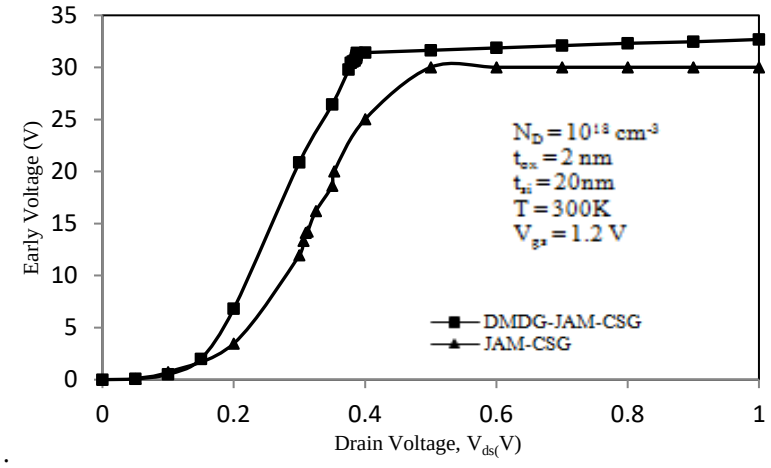


Figure 3.13 Variation of Early voltage with Drain Voltage, V_{ds} for DMDG-JAM-CSG and JAM-CSG MOSFET.

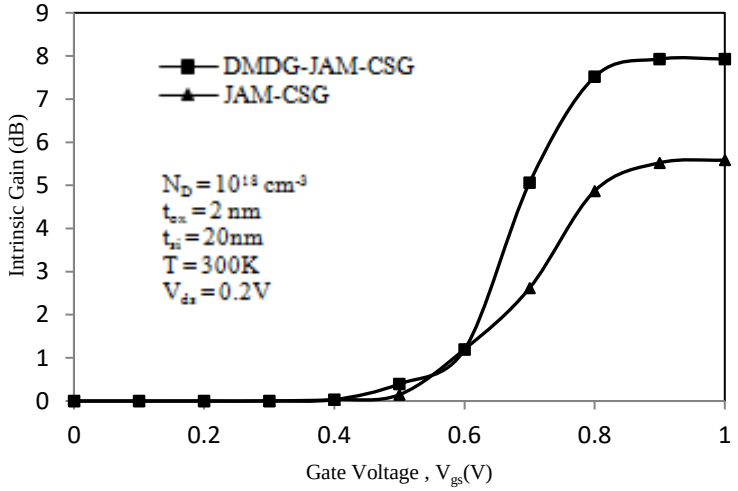
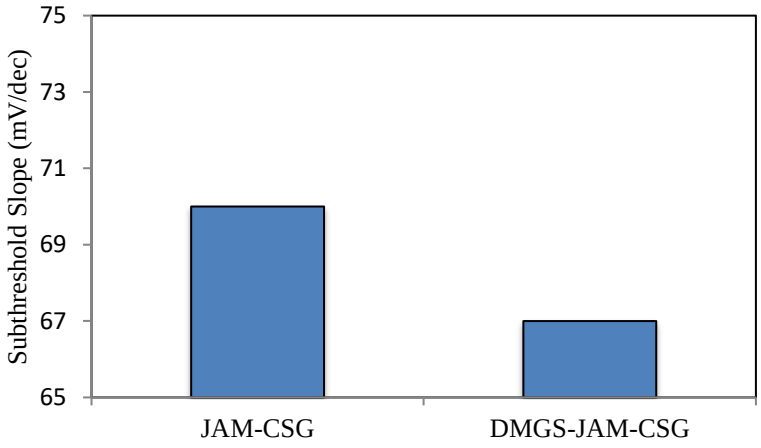


Figure 3.14 Variation of Intrinsic Gain with Gate Voltage for DMDG-JAM-CSG and JAM-CSG MOSFET.

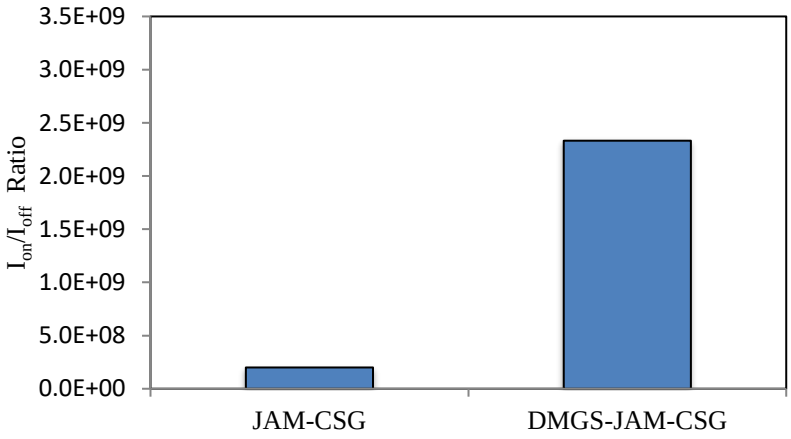
Intrinsic gain (A_v) [28] is stated as:

$$A_v = g_m / g_d \tag{3.37}$$

Intrinsic gain (A_v) w.r.t V_{gs} is shown in Figure 3.14. DMGS-JAM-CSG MOSFET is having higher intrinsic gain than JAM-CSG MOSFET due to the higher transconductance and early voltage [26]. Thus, DMGS-JAM-CSG MOSFET is more relevant for applications requiring high-gain amplification.



(a)



(b)

Figure 3.15 (a) Subthreshold Slope and **(b)** I_{on}/I_{off} ratio for DMDG-JAM-CSG and JAM-CSG MOSFET.

Subthreshold slope (*SS*) [29] is given by:

$$SS = 2.3\, V_T \left[\frac{d\psi(r,z)_{min}}{dV_{GS}}\right]^{-1} \tag{3.38}$$

here, V_T represents the threshold voltage, $\psi(r,z)_{min}$ represents the minimum potential distribution of MOSFET. *SS* for both the MOSFETs is depicted in Figure 3.15(a).

Better subthreshold slope can be seen for DMGS-JAM-CSG MOSFET from the Figure 3.15(a) as compared to the JAM-CSG MOSFET.

I_{on}/ I_{off} ratio defines the digital performance of the MOSFET and is given as:

$$\frac{I_{on}}{I_{off}} = \frac{I_{ds}(on)\ at\ V_{gs}=1.0V}{I_{ds}(off)\ at\ V_{gs}=0.0V} \tag{3.39}$$

I_{on}/ I_{off} ratio is depicted in Figure 3.15(b) for both the devices. From the Figure 3.15(b), DMGS-JAM-CSG MOSFET is noticed to be having higher $I_{on}/\ I_{off}$ ratio, thereby making it more useful for high- switching applications. This also indicates lower leakage current for DMGS-JAM-CSG MOSFET. Thus, all the above results infers that the DMGS-JAM-CSG MOSFET possesses overall better performance and enhanced capability for digital applications as well when contrasted with JAM-CSG MOSFET, thus verifying the excellence of the device.

3.4.3 Linearity Assessment

Minimum signal distortion is a very important requirement for the device for performing various analog/ RF applications with more accuracy. For this, linearity and various intermodulation parameters are evaluated [17]. These parameters are higher-order transconductances (g_{m2} and g_{m3}) and several FOMs namely second-order and third-order Voltage Intercept Points (VIP2, VIP3), third-order Intercept Input Power (IIP3), third-order Intermodulation Distortion (IMD3). Mathematically, these parameters are given by:

$$g_{mn} = \frac{\partial^n I_d}{\partial {V_{gs}}^n} \tag{3.40}$$

$$\text{VIP2} = 4 \text{ x } \frac{g_{m1}}{g_{m2}} \tag{3.41}$$

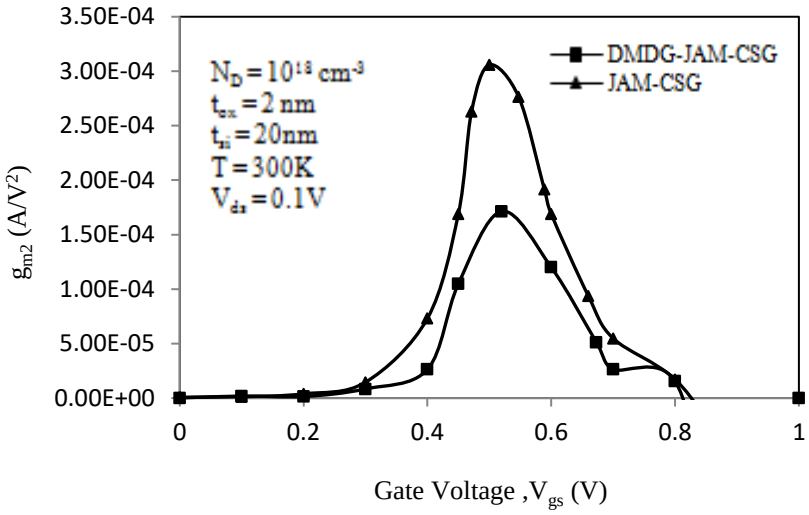
$$\text{VIP3} = \sqrt{24 \text{ x } \frac{g_{m1}}{g_{m3}}} \tag{3.42}$$

$$\text{IIP3} = \frac{2}{3} \text{ x } \frac{g_{m1}}{g_{m3} \text{ x } R_s} \tag{3.43}$$

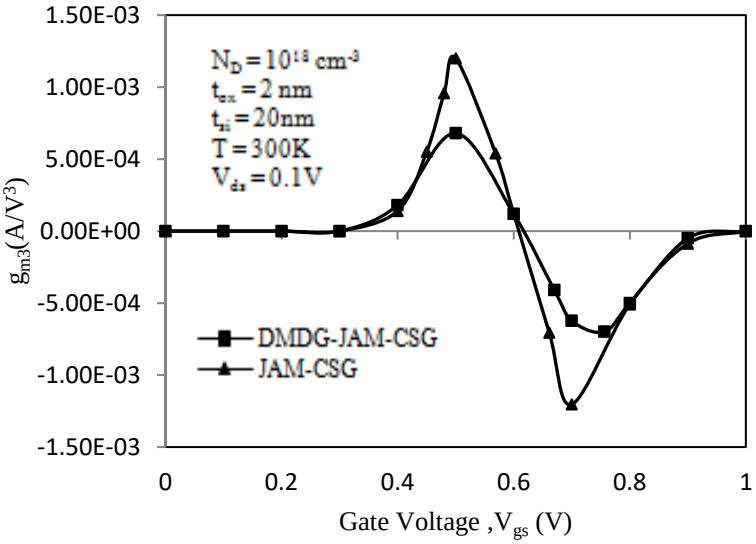
$$\text{IMD3} = \left[\frac{9}{2} \text{ x } (\text{VIP3})^2 \text{ x } g_{m3}\right]^2 \text{ x } R_s \tag{3.44}$$

where, R_s= 50Ω during RF designs [16].

Figures 3.16(a) and (b) represents the higher order transconductances, g_{m2} and g_{m3} variation against the V_{gs}, respectively. These coefficients should be ideally zero or of minimal value for the device to be of high-linearity.



(a)



(b)

Figure 3.16 Variation of Higher-order transconductances for DMDG-JAM-CSG and JAM-CSG MOSFET **(a)** g_{m2} with respect to gate voltage **(b)** g_{m3} with respect to gate voltage.

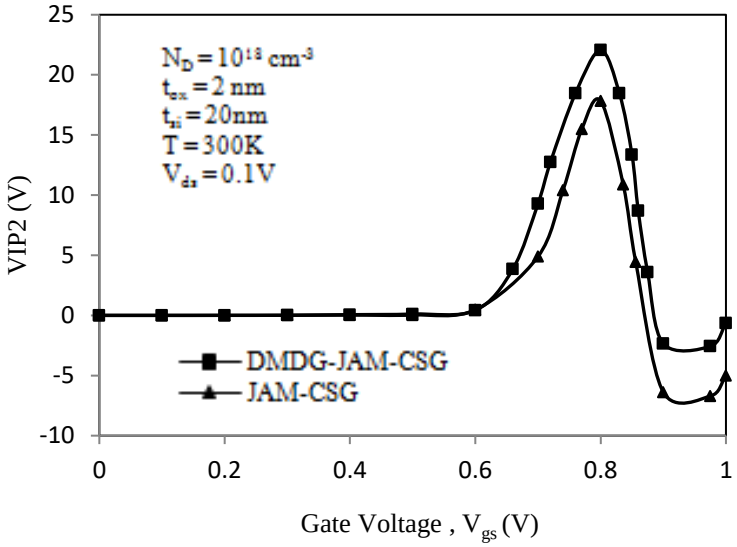
From the figure, it can be seen that DMGS-JAM-CSG MOSFET possesses lower higher- order transconductances as compared to JAM-CSG MOSFET, which indicates the lowered harmonic distortions and improved linearity behaviour. The reason is the increased gate control provided in the case of DMGS-JAM-CSG MOSFET.

Figures 3.17 (a) to (d) represents the numerous FOMs (VIP2, VIP3, IIP3 and IMD3). The VIP2 is the extrapolated input voltage at which first order harmonic voltage is equal to the second order harmonic voltage. Likewise, VIP3 is the extrapolated input voltage at which first order harmonic is equal to the third order harmonic voltage. For improved linearity of the device, elevated values of VIP2 and VIP3 is preferable. Figure 3.17(a) represents the VIP2 against V_{gs} and higher value of VIP2 is being observed for DMGS-JAM-CSG as contrasted to the JAM-CSG MOSFET, which indicates its lower distortion and better linearity characteristics over JAM-CSG MOSFET.

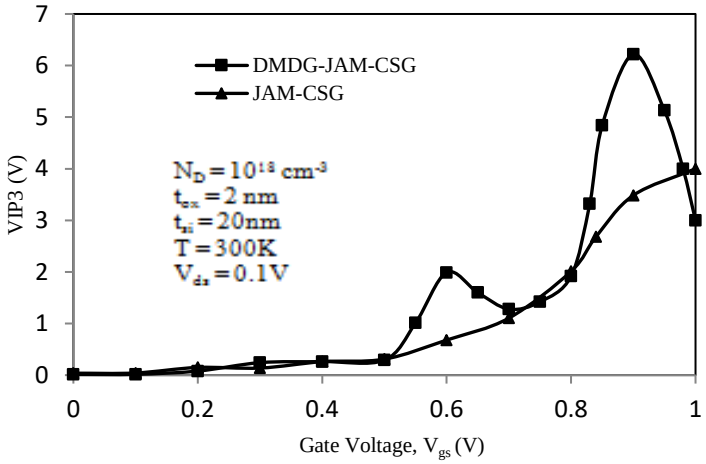
Figure 3.17(b) shows the variation of VIP3 against the gate voltage for both the devices under consideration. A peak of VIP3 at lower gate bias for DMGS-JAM-CSG MOSFET is observed. This peak of VIP3 indicates cancellation of 3rd order non-linear coefficient around second order non-linear coefficient by internal feedback of the device. This occurs on account of the lower metal work function gate present towards the drain side.

The IIP3 is the extrapolated input power at which third order intermodulation voltage and the first order harmonic voltage are equal. The IIP3 for the device must be high for better linearity characteristics [30]. Figure 3.17(c) shows IIP3 against the gate bias voltage for DMGS-JAM-CSG and JAM-CSG MOSFET. The DMGS-JAM-CSG MOSFET possesses higher value of IIP3 which indicates its better linearity as compared to JAM-CSG MOSFET. This enhancement in IIP3 for DMGS-JAM-CSG MOSFET is due to the dual-metal architecture which provides distinct work functions for the two metal gates. Thus, providing a step- profile for the device's potential. This higher IIP3 yields better gate control and also provides higher carrier transport over the channel.

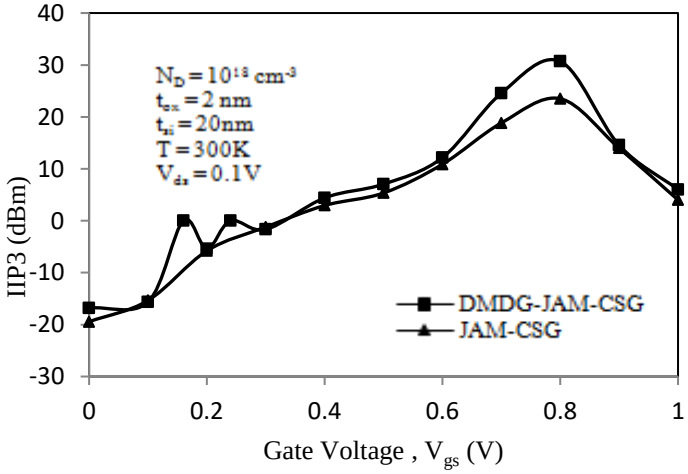
Next relevant linearity specification is IMD3 (Third- order Intermodulation Distortion). It is the extrapolated intermodulation power at which the first order harmonic power and third order intermodulation harmonic power are equal. Figure 3.17(d) shows IMD3 for DMGS-JAM-CSG MOSFET and JAM-CSG MOSFET. For any device to be distortionless, this parameter should be low [30]. From the Figure 3.17(d), we can make out that the DMGS-JAM-CSG MOSFET possesses lower value of IMD3 as compared to JAM-CSG MOSFET. This indicates superior linearity of DMGS-JAM-CSG MOSFET and its higher efficiency.


$N_D = 10^{18}$ cm^{-3}
$t_{ox} = 2$ nm
$t_{si} = 20$nm
T = 300K
$V_{ds} = 0.1$V
DMDG-JAM-CSG
JAM-CSG
VIP2 (V)
Gate Voltage , V_{gs} (V)

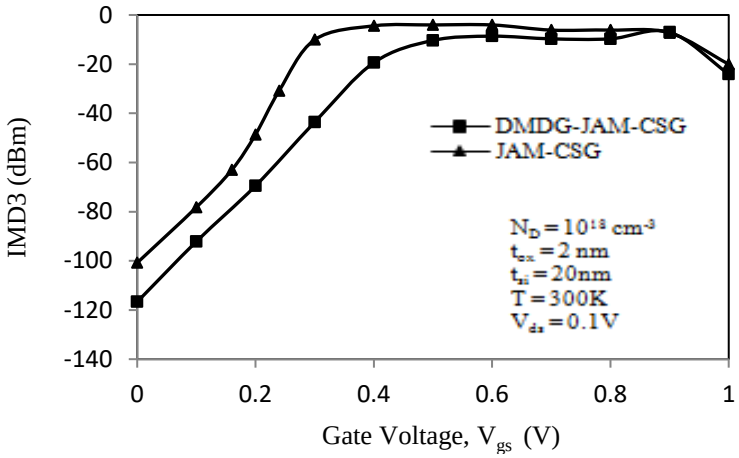
(a)


DMDG-JAM-CSG
JAM-CSG
$N_D = 10^{18}$ cm^{-3}
$t_{ox} = 2$ nm
$t_{si} = 20$nm
T = 300K
$V_{ds} = 0.1$V
VIP3 (V)
Gate Voltage, V_{gs} (V)

(b)


$N_D = 10^{18}$ cm^{-3}
$t_{ox} = 2$ nm
$t_{si} = 20$nm
T = 300K
$V_{ds} = 0.1$V
DMDG-JAM-CSG
JAM-CSG
IIP3 (dBm)
Gate Voltage , V_{gs} (V)

(c)



(d)

Figure 3.17 Variation of various FOMs **(a)** VIP2 **(b)** VIP3 **(c)** IIP3 **(d)** IMD3 with respect to the Gate Voltage, V_{gs} for DMDG-JAM-CSG and JAM-CSG MOSFET.

3.5 Summary

An analytical model has been developed in this chapter to study the influence of temperature upon DMGS-JAM-CSG MOSFET. As the temperature increases, an improvement has been observed in all the parameters of the DMGS-JAM-CSG MOSFET. It is observed that the potential and electron velocity are lowered by 48 mV and 59 cm/s respectively, indicating reduction of SCEs and HCEs, as the temperature is increasing from 100K to 500K. Also, analytical results agree well with the simulated ones. Further, the device has been examined for its analog performance and higher values for drain current, transconductance, output conductance, early voltage and intrinsic gain is noticed for the DMGS-JAM-CSG MOSFET. Thus, the device stands out to be more applicable for high-frequency and high-gain amplification applications. I_{on}/ I_{off} ratio has also increased by 11.6 times in comparison to JAM-CSG MOSFET, thus, the device possesses lower leakage current and more useful for high-switching applications. Linearity metrics g_{m2}, g_{m3}, VIP2, VIP3, IMD3 and IIP3 were also examined and found to be improved for DMGS-JAM-CSG MOSFET, thus, marking the device to be more distortion free and applicable for RFIC applications.

3.6 References

[1] Jimenez, David, J. J. Saenz, Benjamin Iniguez, Jordi Sune, Lluis F. Marsal, and Josep Pallares. "Modeling of nanoscale gate-all-around MOSFETs." *IEEE Electron device letters* 25, no. 5 (2004): 314-316.

[2] Wang, Runsheng, Jing Zhuge, Ru Huang, Yu Tian, Han Xiao, Liangliang Zhang, Chen Li, Xing Zhang, and Yangyuan Wang. "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation." *IEEE transactions on Electron Devices* 54, no. 6 (2007): 1288-1294.

[3] Colinge, Jean Pierre. "Multi-gate soi mosfets." *Microelectronic Engineering* 84, no. 9-10 (2007): 2071-2076.

[4] Sarkar, Angsuman, Aloke Kumar Das, Swapnadip De, and Chandan Kumar Sarkar. "Effect of gate engineering in double-gate MOSFETs for analog/RF applications." *Microelectronics Journal* 43, no. 11 (2012): 873-882.

[5] Wu, Yu-Sheng, and Pin Su. "Sensitivity of gate-all-around nanowire MOSFETs to process variations—A comparison with multigate MOSFETs." *IEEE transactions on electron devices* 55, no. 11 (2008): 3042-3047.

[6] Colinge, Jean-Pierre, Chi-Woo Lee, Aryan Afzalian, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi et al. "Nanowire transistors without junctions." *Nature nanotechnology* 5, no. 3 (2010): 225-229.

[7] Cho, Seongjae, Kyung Rok Kim, Byung-Gook Park, and In Man Kang. "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs." *IEEE Transactions on Electron Devices* 58, no. 5 (2011): 1388-1396.

[8] Kim, Tae Kyun, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong-Il Moon, Gi Seong Lee et al. "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation." *IEEE electron device letters* 34, no. 12 (2013): 1479-1481.

[9] Holtij, Thomas, Michael Graef, Franziska Marie Hain, Alexander Kloes, and Benjamn Iñíguez. "Compact model for short-channel junctionless accumulation mode double gate MOSFETs." *IEEE Transactions on Electron Devices* 61, no. 2 (2013): 288-299.

[10] Chau, Robert, Suman Datta, Mark Doczy, Brian Doyle, Jack Kavalieros, and Matthew Metz. "High-/spl kappa//metal-gate stack and its MOSFET characteristics." *IEEE Electron Device Letters* 25, no. 6 (2004): 408-410.

[11] Dhiman, Gaurav, Rajeev Pourush, and P. K. Ghosh. "Performance analysis of high-κ material gate stack based nanoscale junction less double gate MOSFET." *Materials Focus* 7, no. 2 (2018): 259-267.

[12] Darwin, S., and TS Arun Samuel. "A holistic approach on Junctionless dual material double gate (DMDG) MOSFET with high k gate stack for low power digital applications." *silicon* 12, no. 2 (2020): 393-403.

[13] Ji, Shiqi, Sheng Zheng, Fei Wang, and Leon M. Tolbert. "Temperature-dependent characterization, modeling, and switching speed-limitation analysis of third-generation 10-kV SiC MOSFET." *IEEE Transactions on Power Electronics* 33, no. 5 (2017): 4317-4327.

[14] Skotnicki, Thomas, James A. Hutchby, Tsu-Jae King, H-SP Wong, and Frederic Boeuf. "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance." *IEEE Circuits and Devices Magazine* 21, no. 1 (2005): 16-26.

[15] Gautam, Rajni, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "Temperature dependent subthreshold model of long channel GAA MOSFET including localized charges to study variations in its temperature sensitivity." *Microelectronics Reliability* 54, no. 1 (2014): 37-43.

[16] Saha, Rajesh, Brinda Bhowmick, and Srimanta Baishya. "Temperature effect on RF/analog and linearity parameters in DMG FinFET." *Applied Physics A* 124, no. 9 (2018): 1-10.

[17] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design." *IEEE Transactions on Device and Materials Reliability* 14, no. 1 (2014): 418-425.

[18] Kaya, Savas, and Wei Ma. "Optimization of RF linearity in DG-MOSFETs." *IEEE Electron Device Letters* 25, no. 5 (2004): 308-310.

[19] ATLAS, Device Simulator. "Silvaco International. Santa Clara." (2015).

[20] Choi, Sung-Jin, Dong-Il Moon, Sungho Kim, Juan P. Duarte, and Yang-Kyu Choi. "Sensitivity of threshold voltage to nanowire width variation in

junctionless transistors." *IEEE Electron Device Letters* 32, no. 2 (2010): 125-127.

[21] Goel, Anubha, Sonam Rewari, Seema Verma, and R. S. Gupta. "Temperature-dependent gate-induced drain leakages assessment of dual-metal nanowire field-effect transistor—analytical model." *IEEE Transactions on Electron Devices* 66, no. 5 (2019): 2437-2445.

[22] Narang, Rakhi, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "Impact of temperature variations on the device and circuit performance of tunnel FET: a simulation study." *IEEE transactions on Nanotechnology* 12, no. 6 (2013): 951-957.

[23] Caughey, D. Mo, and R. E. Thomas. "Carrier mobilities in silicon empirically related to doping and field." *Proceedings of the IEEE* 55, no. 12 (1967): 2192-2193.

[24] Hasanuzzaman, Md, Syed K. Islam, and Leon M. Tolbert. "Effects of temperature variation (300–600 K) in MOSFET modeling in 6H–silicon carbide." *Solid-State Electronics* 48, no. 1 (2004): 125-132.

[25] Gnudi, A., S. Reggiani, E. Gnani, and G. Baccarani. "Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs." *IEEE Electron Device Letters* 33, no. 3 (2012): 336-338.

[26] Duarte, Juan Pablo, Sung-Jin Choi, and Yang-Kyu Choi. "A full-range drain current model for double-gate junctionless transistors." *IEEE transactions on electron devices* 58.12 (2011): 4219-4225.

[27] Arora, Narain D. *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media, 2012.

[28] Rewari, Sonam, Vandana Nath, Subhasis Haldar, S. S. Deswal, and R. S. Gupta. "Improved analog and AC performance with increased noise immunity using nanotube junctionless field effect transistor (NJLFET)." *Applied Physics A* 122, no. 12 (2016): 1-10.

[29] Colinge, J-P. "Subthreshold slope of thin-film SOI MOSFET's." *IEEE Electron Device Letters* 7, no. 4 (1986): 244-246.

[30] Wang, Tao, Liang Lou, and Chengkuo Lee. "A junctionless gate-all-around silicon nanowire FET of high linearity and its potential applications." *IEEE Electron Device Letters* 34, no. 4 (2013): 478-480.

CHAPTER 4

Analytical Model for Junctionless Accumulation-Mode Cylindrical Surrounding Gate (JAM-CSG) MOSFET as a Biosensor

4.1 Introduction

A Biosensor, i.e., a biological sensor, is a device which helps detecting the biological and chemical substances (for example, DNA, biotin, protein, etc.) by producing the signals corresponding to the analyte. Thus, the biosensor can help in monitoring the disease, detection of various micro- organisms, pollutants, etc. and therefore, holds an important application in the field of biomedical. So, in this chapter MOSFET has been utilized to work as a biosensor. Various electrical characteristics of the proposed biosensor and its sensitivity towards the biomolecules have been examined in detail.

Nowadays, the dimensions of the MOSFET are getting shrinked which brings about a trouble called as short- channel effects (SCEs) [1, 2]. Therefore, in order to tackle with these SCEs, numerous multi- gate (Double gate, Fin-FETs, Surrounding Gate) MOSFETs [3-6], silicon- on selective buried oxide (SELBOX) MOSFETs [7] were introduced and found to be more superior compared to the conventional MOSFETs. These topologies offer lesser SCEs and thus, improved characteristics. However, reduction in the MOSFET dimensions also makes the fabrication process difficult and a costly phenomenon due to the ultra-sharp doping profiles formed between the source/drain and channel regions. Thus, Junctionless Transistor (JLT) [8] was then proposed to solve this problem. It contains same type of doping throughout the MOSFET; therefore, no abrupt junction exists in JLTs. Thus, fabrication process becomes simpler and economical. Also, JLT provides better immunity towards SCEs as well as better overall characteristics. JLT MOSFETs also finds potential applications in the area of optical communication as ultrasensitive photodetectors [9] and also significant for performing analog/ RF applications [10-12] with low cost and high performance. Besides all these advantages, it possesses a drawback of lesser drain current and transconductance [13]. Thus, to tackle with this drawback, another

MOSFET, named Junctionless Accumulation Mode (JAM) MOSFET [14-15] was proposed. The doping present in the channel region of this MOSFET is a bit lesser than the source and drain, which makes this MOSFET to possess better electrical properties and more conductivity as compared to JLT. So, in this chapter, application of JAM MOSFET as a biosensor is being developed.

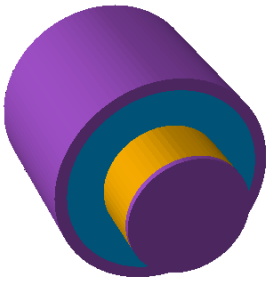
4.1.1 MOSFET as a Biosensor

Biosensor provides applications to detect various biological parameters [16-18]. FET-based biosensors have several advantages over other techniques such as high sensitivity, direct transduction, mass production and compatibility with CMOS technology. Ion-sensitive FET (ISFET) [19] was the first biosensor using FET and was introduced in 1970. It gave good results but also had limited capability to detect neutral biomolecules and was also not compatible with CMOS technology. Then to solve this problem, biosensor based on dielectric modulated FET (DM-FET) [20] was proposed. Now, to further improve the sensitivity, JAM- CSG MOSFET has been utilized to work as a biosensor in this current work. The investigation of this JAM MOSFET based biosensor is done by building an analytical model and analyzing the influence of both the neutral and charged biomolecules upon the MOSFET characteristics. The sensitivity criterion for biomolecule detection used is the threshold voltage change of the MOSFET. For carrying out this work, we have considered dry environment conditions due to its several advantages. Dry environment offers high degree of freedom which in turn provides better characteristics for biosensor [21]. Also, under this condition, electric signal is independent of the Debye length parameter [22]. Debye length depends upon the ionic concentration present in the sample and in the case of humans; this concentration is difficult to control. Therefore, Debye length independent sensing technique is also an advantage when working under dry environment conditions. Hence, utilizing these dry environment conditions, a biosensor based upon JAM MOSFET is proposed in this chapter to perform various biosensor applications.

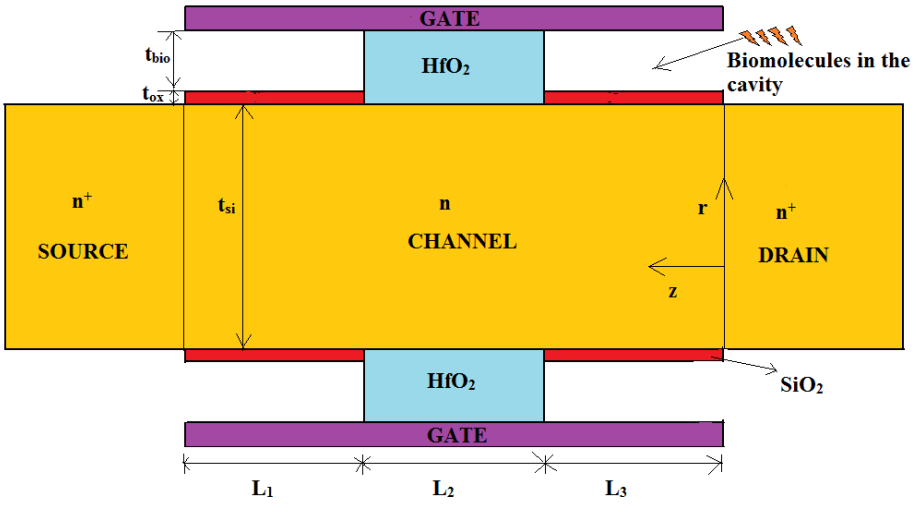
4.2 Device Description

Figures 4.1(a) and (b) illustrates the 3-D and 2-D device architectures for JAM MOSFET based biosensor respectively. The structure consists of nanogap cavities created at the source side and drain side (of lengths L_1 and L_3 respectively) by etching

the oxide layer from both the ends of the channel. t_{bio} is the thickness of these nanogap cavities. In between the cavities is the gate oxide (HfO_2) of length L_2. Also, t_{si} and t_{ox} are the widths of the silicon pillar and SiO_2 layer respectively.



(a)



(b)

Figure 4.1(a) 3-D and **(b)** 2-D architectures of JAM-CSG MOSFET based biosensor.

The fabrication process for this biosensor is as follows, firstly, an N-type Si bulk is taken as the starting substrate material. Then, channel doping of $10^{18}/cm^3$ is carried out by ion implantation method and with the help of Bosch process, Si nanowire is developed. After this, the procedure for channel stop implantation is performed, followed by sacrificial oxidation and formation of Shallow Trench Isolation. Next, oxide etching is executed to form nanogap cavities. Thereafter, gate stack deposition on the substrate and then N^+ polysilicon deposition by isotropic method takes place. Gate patterning is then implemented and S/D doping of $10^{20}/cm^3$ is accomplished by employing ion implantation technique. Finally, a process named as gas annealing is conducted [23, 24].

Nanogap cavity regions are functionalized for immobilization of biomolecules, thus, acting as the sensing region for detecting the biomolecules. The neutral biomolecules are simulated by inserting a material with dielectric constant, $\kappa > 1$ in the nanogap cavity under the assumption that the cavity is entirely occupied with the biomolecules. Firstly, we consider the nanogap cavity to be unoccupied by the biomolecules and completely filled with air, having permittivity equal to one. Then, a layer of oxide possessing different dielectric constants (like, κ = 3, 5, 7, 9) is defined in the cavity region for detecting the existence of the neutral biomolecules. Table 4.1 lists the various biomolecules alongwith their dielectric constants [25-27].

Table 4.1

Biomolecules and their dielectric constants

Biomolecule	DNA	Biotin	Protein	APTES	Hydroprotein
Dielectric Constant	8.7	2.63	2.50	3.57	5

Table 4.2

Structural Parameters of JAM-CSG MOSFET based biosensor

Parameter	**Value**
Length of Channel (L)	30 nm
Channel Doping (N_D)	$10^{18}/cm^3$
Source/Drain Doping N_D^+)	$10^{20}/cm^3$
Gate Oxide Materials	SiO_2 (κ = 3.9) & HfO_2 (κ = 25)
Width of SiO_2 (t_{ox})	1 nm
Nanogap Cavity Thickness (t_{bio})	5 nm
Silicon Pillar Thickness (t_{si})	20 nm
Length of Nanogap Cavities (L_1 and L_3)	10 nm
Length of HfO_2 Layer (L_2)	10 nm
Work- Function of Gate Material (Φ)	4.8 eV

The influence of the charged biomolecules is taken into account by examining positive and negative fixed oxide charges (N_f) at the SiO_2- air interface. N_f is varied from -7x10^{11} Cm^{-2} to 7x10^{11} Cm^{-2} to study its influence on the device. Table 4.2 lists the several structural parameters and Table 4.3 summarizes the various physical models employed during the simulation process using ATLAS 3-D simulator [28].

Table 4.3

Physical Models used in simulation

Physical models	**Description**
Recombination Model	The Shockley– Read– Hall model examines minority recombination effects.
Field- Dependent Mobility Model	FLDMOB to accommodate the velocity saturation effect.
Concentration- Dependent Mobility Model	CONMOB to refer to the low-field mobility.
Statistics	Boltzmann Model takes into account the Carrier Statistics.
Methods	Newton and Gummel methods are concurrently evoked to perform the numerical solution.

4.3 Analytical Model

4.3.1. Center Potential

For acquiring the potential distribution model for the JAM-CSG MOSFET based biosensor, analytical modeling has been done by utilizing 2-D Poisson's equation in cylindrical co-ordinate system considering Parabolic Potential Approximation (PPA). The model has been evolved taking into consideration suitable boundary conditions.

Also, the channel region of proposed device has been splitted into three sections, i.e.:

Section I: $0 \leqslant x \leqslant t_{si}; 0 \leqslant y \leqslant L_1$

Section II: $0 \leqslant x \leqslant t_{si}; L_1 \leqslant y \leqslant L_1 + L_2$

Section III: $0 \leqslant x \leqslant t_{si}; L_1 + L_2 \leqslant y \leqslant L_1 + L_2 + L_3$

The analysis is performed in each of the three sections under the assumption that the channel region is fully depleted when the subthreshold condition is prevailing and the effect of mobile charge carriers is almost negligible. The Poisson's equation [29, 30] is expressed as:

$$\frac{\partial^2\psi_i(r,z)}{\partial r^2}+\frac{1}{r}\left(\frac{\partial\psi_i(r,z)}{\partial r}\right)+\frac{\partial^2\psi_i(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}} \tag{4.1}$$

where, $i = 1$, 2 and 3 corresponding to the respective sections I, II and III, $\psi_i(r,z)$ is the potential variation, r is the co-ordinate for radial direction, z is the co-ordinate for channel length direction, q denotes electronic charge and ε_{si} be the permittivity of Si.

The Potential across r and z directions is calculated using parabolic potential function [31]:

$$\psi_i(r,z)=P_{i0}(z)+P_{i1}(z)\,r+P_{i2}(z)\,r^2 \tag{4.2}$$

The coefficients $P_{i0},(z), P_{i1}(z)$ and $P_{i2}(z)$ are calculated with the help of the successive boundary conditions:

(1) Center Potential:

$$\psi_i(r=0,z)=\psi_c \tag{4.3}$$

(2) Electric Field at the center:

$$\frac{\partial\psi_i(r,z)}{\partial r}\Big|_{r=0}=0 \tag{4.4}$$

(3) Potential present at the surface:

$$\psi_i\left(r=\frac{t_{si}}{2},z\right)=\psi_s\left(\frac{t_{si}}{2},z\right) \tag{4.5}$$

(4) Electric Field at the surface:

$$\frac{\partial\psi_i\left(\frac{t_{si}}{2},z\right)}{\partial r}=\frac{C_i}{\varepsilon_{si}}\left[V_{gs}-V_{fbi}-\psi_i\left(\frac{t_{si}}{2},z\right)\right] \tag{4.6}$$

(5) Potential near source end:

$$\psi_1(r,0)=V_{bi} \tag{4.7}$$

(6) Potential near drain end:

$$\psi_2(r, L_1 + L_2 + L_3) = V_{bi} + V_{ds} \tag{4.8}$$

where, V_{bi} be the built-in potential and C_{ox} is given by $C_{ox} = \frac{2\varepsilon_{ox}}{t_{si} \ln\left[1+\left(\frac{2t_{ox}}{t_{si}}\right)\right]}$ (4.9)

The flat band voltages in section I (V_{fb1}), II (V_{fb2}) and III (V_{fb3}) are given by:

$$V_{fb1} = V_{fb3} = V_{fb2} - \frac{qN_f}{C_{gap}}; \tag{4.10}$$

$$\text{where, } C_{gap} = \frac{\varepsilon_{bio}}{t_{bio}} \tag{4.11}$$

Here N_f and ε_{bio} correspond to charge density and permittivity of the biomolecules respectively.

Let C_i be the gate capacitance for all the three sections and is given as:

$$C_1 = C_3 = C_{eff} \tag{4.12}$$

$$C_{eff} = \frac{\varepsilon_{bio}\varepsilon_{ox}}{\varepsilon_{bio}t_{ox}+\varepsilon_{ox}t_{bio}} \tag{4.13}$$

$$C_2 = C_{ox} \tag{4.14}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.15}$$

On applying the above boundary conditions, the coefficients $P_{0i}(z)$, $P_{1i}(z)$ and $P_{2i}(z)(i = 0, 1, 2)$ are obtained as:

$$P_{10}(z) = \psi_{c_1}(z) \tag{4.16a}$$

$$P_{20}(z) = \psi_{c_2}(z) \tag{4.16b}$$

$$P_{30}(z) = \psi_{c_3}(z) \tag{4.16c}$$

$$P_{11}(z) = 0 \tag{4.16d}$$

$$P_{21}(z) = 0 \tag{4.16e}$$

$$P_{31}(z) = 0 \tag{4.16f}$$

$$P_{12}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \tag{4.16g}$$

$$P_{22}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \quad (4.16h)$$

$$P_{32}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \quad (4.16i)$$

where, C_{ox} is the capacitance per unit area and is given by:

$$C_{ox} = \frac{2\varepsilon_{ox}}{t_{si}\ln\left(1+\frac{2t_{oxeff}}{t_{si}}\right)} \quad (4\backslash.17)$$

Now, using the above coefficient values, the center potential specified by equation (4.2) is rewritten as:

$$\psi_1(r,z) = \psi_{c_1}(z) + r^2\frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \quad (4.18a)$$

$$\psi_2(r,z) = \psi_{c_2}(z) + r^2\frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \quad (4.18b)$$

$$\psi_3(r,z) = \psi_{c_3}(z) + r^2\frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_3} - \psi_{si_3}(r = \frac{t_{si}}{2}, z)\right] \quad (4.18c)$$

At $r = \frac{t_{si}}{2}$, $\psi\left(r = \frac{t_{si}}{2}, z\right) = \psi_{si}(r = \frac{t_{si}}{2}, z)$, so the equation (4.18) for ψ_{si_1}, ψ_{si_2} and ψ_{si_3} becomes

$$\psi_{si_1}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_1(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_1} - \psi_{si_1}(r=\frac{t_{si}}{2},z)}{\varepsilon_{si}t_{si}}\right) \quad (4.19a)$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r=\frac{t_{si}}{2},z)}{\varepsilon_{si}t_{si}}\right) \quad (4.19b)$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r=\frac{t_{si}}{2},z)}{\varepsilon_{si}t_{si}}\right) \quad (4.19c)$$

Rearranging the terms in (4.19) yields

$$\psi_{si_1}(r = \frac{t_{si}}{2}, z) = \left[\frac{4\varepsilon_{si}\psi_{c_1(z)} + t_{si}C_{ox}\psi_{gs_1}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \quad (4.20a)$$

$$\psi_{si_2}(r = \frac{t_{si}}{2}, z) = \left[\frac{4\varepsilon_{si}\psi_{c_2(z)} + t_{si}C_{ox}\psi_{gs_2}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \quad (4.20b)$$

$$\psi_{si_3}(r = \frac{t_{si}}{2}, z) = \left[\frac{4\varepsilon_{si}\psi_{c_2(z)} + t_{si}C_{ox}\psi_{gs_2}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \quad (4.20c)$$

The JLT works on bulk to source conduction mechanism, therefore, the center potential is to be calculated for r = 0. Center potential for two different metals is solved and is given as:

$$\frac{\partial^2\psi_{c_1}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_1(z)} - \eta_1\right], \qquad 0 \leqslant z \leqslant L_1 \tag{4.21a}$$

$$\frac{\partial^2\psi_{c_2}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_2(z)} - \eta_2\right], \qquad L_1 \leqslant z \leqslant L_1 + L_2 \tag{4.21b}$$

$$\frac{\partial^2\psi_{c_3}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_3(z)} - \eta_3\right], \qquad L_1 + L_2 \leqslant z \leqslant L_1 + L_2 + L_3 \tag{4.21c}$$

where, the characteristic length (λ), η_1, η_2 and η_3 are respectively given by

$$\frac{1}{\lambda^2} = \frac{16\, C_{ox}}{4\varepsilon_{si}t_{si} + {t_{si}}^2 C_{ox}} \tag{4.22}$$

$$\eta_1 = \psi_{gs_1} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{4.23a}$$

$$\eta_2 = \psi_{gs_2} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{4.23b}$$

$$\eta_3 = \psi_{gs_3} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{4.23c}$$

Center potential, $\psi_{ci}(r,z)$ is thus obtained for all the three sections as:

$$\psi_{ci}(r,z) = \begin{cases} \psi_{c1}(r,z) \text{ for } 0 \leqslant z \leqslant L_1 \\ \psi_{c2}(r,z) \text{for } L_1 \leqslant z \leqslant L_1 + L_2 \\ \psi_{c3}(r,z) \text{for } L_1 + L_2 \leqslant z \leqslant L_1 + L_2 + L_3 \end{cases} \tag{4.24}$$

where, $\psi_{Ci}(r,z) = A_i\, e^{z/\lambda} + B_i e^{-z/\lambda} + \eta_i$ (4.25)

The coefficients A_i and B_i are calculated by employing the aforementioned boundary conditions and are given as:

$$A_1 = \frac{e^{-L_1/\lambda}(\phi_{bi} - \eta_1) - \psi_1 + \eta_1}{(e^{-L_1/\lambda} - e^{L_1/\lambda})} \tag{4.26a}$$

$$B_1 = \frac{e^{L_1/\lambda}(\phi_{bi} - \eta_1) - \psi_1 + \eta_1}{(e^{L_1/\lambda} - e^{-L_1/\lambda})} \tag{4.26b}$$

$$A_2 = \frac{e^{-L_2/\lambda}(\psi_1 - \eta_2) - \psi_2 + \eta_2}{e^{(L_1 - L_2)/\lambda} - e^{(L_1 + L_2)/\lambda}} \tag{4.26c}$$

$$B_2 = \frac{e^{L_2/\lambda(\psi_1-\eta_2)-\psi_2+\eta_2}}{e^{-(L_1-L_2)/\lambda}-e^{-(L_1+L_2)/\lambda}} \quad (4.26d)$$

$$A_3 = \frac{e^{-L_3/\lambda(\psi_2-\eta_3)-V_{ds}-\phi_{bi}+\eta_3}}{e^{(L_1+L_2-L_3)/\lambda}-e^{(L_1+L_2+L_3)/\lambda}} \quad (4.26e)$$

$$B_3 = \frac{e^{L_3/\lambda\,(\psi_2-\eta_3)-V_{ds}-\phi_{bi}+\eta_3}}{e^{-(L_1+L_2-L_3)/\lambda}-e^{-(L_1+L_2+L_3)/\lambda}} \quad (4.26f)$$

where, ψ_1 and ψ_2 are the potentials at the intermediate points.

4.3.2. Threshold Voltage

It is used as an index for measuring the sensing parameter useful for determining the efficiency of the biosensor. It is expressed as:

$$V_{th} = V_{fb} + 2\phi_{bi} + \frac{q(\pm N_f)}{C_{eff}} \quad (4.27)$$

where, $\phi_{bi} = V_T ln\left(\frac{{N_D}^+}{N_D}\right)$ (4.28)

V_T is the thermal voltage.

4.3.3. Subthreshold Current

It is given by the following expression:

$$I_d(V_{gs}, V_{ds}, z) = \frac{\left[2\pi N_D \mu\left\{1-e^{\frac{-(qV_{ds})}{(k_B T)}}\right\}\right]}{\int_0^{L_1+L_2+L_3} \frac{1}{\int_0^r r.e\left(\frac{q\psi(V_{gs},V_{ds},z)}{k_B T}\right)dr} dz} \quad (4.29)$$

where, μ be the mobility of the carrier and k_B be the Boltzmann's constant.

4.3.4. Sensitivity

To determine the sensitivity of the device (ΔV_{th}) towards the existence of biomolecules (both neutral and charged) in the cavity region, mathematical expressions [30] used are:

(i). when neutral biomolecules are present:

$$\Delta V_{th} = V_{th}(\kappa = 1) - V_{th}(\kappa > 1) \quad (4.30)$$

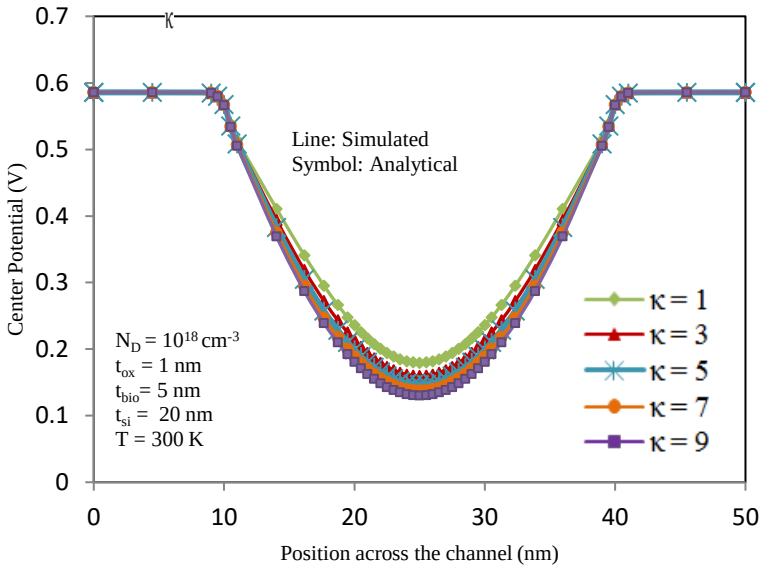
(ii). when charged biomolecules are present:

$$\Delta V_{th} = V_{th}(neutral\ biomolecule) - V_{th}(charged\ biomolecule) \qquad (4.31)$$

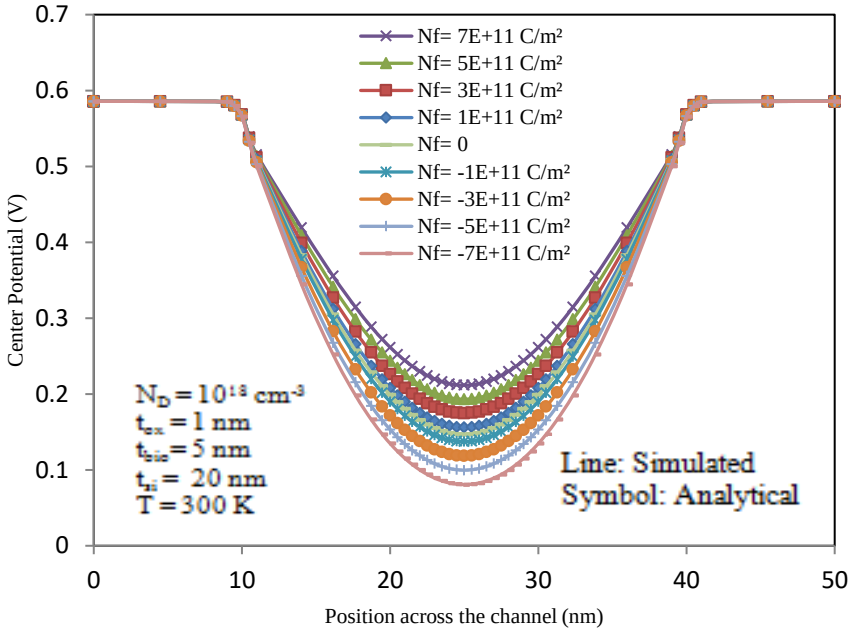
4.4 Results and Discussion

4.4.1 Center Potential

Figure 4.2 illustrates the center potential variation [32] along the channel length for the two cases: (i). when nanogap region is infused with materials possessing distinct permittivities (κ = 1, 3, 5, 7, and 9) corresponding to the neutral biomolecules and (ii). when filled by positive and negative charged biomolecules. Figure 4.2 (a) illustrates the center potential curve for the first case. When κ = 1, it means that the cavity is infused with air and no biomolecules are present. When κ is changed to higher values i.e., κ = 3, 5, 7, 9 then, it implies that the cavity is being simulated by the neutral biomolecules. From Figure 4.2 (a), it is noticed that as the permittivity of the material introduced in the cavity increments from κ = 1 to κ = 9, center potential decreases for JAM-MOSFET. Figure 4.2 (b) displays the center potential distribution for the case (ii), when the cavity is simulated with positive and negative fixed oxide charges, where the charge has been varied from -7x10^{11} Cm^{-2} to 7x10^{11} Cm^{-2}. From this figure, it is perceived that the minimal center potential decreases when the negatively charged biomolecules are simulated in the cavity. In contrast, center potential increases when the positive charged biomolecules are introduced.



(a)



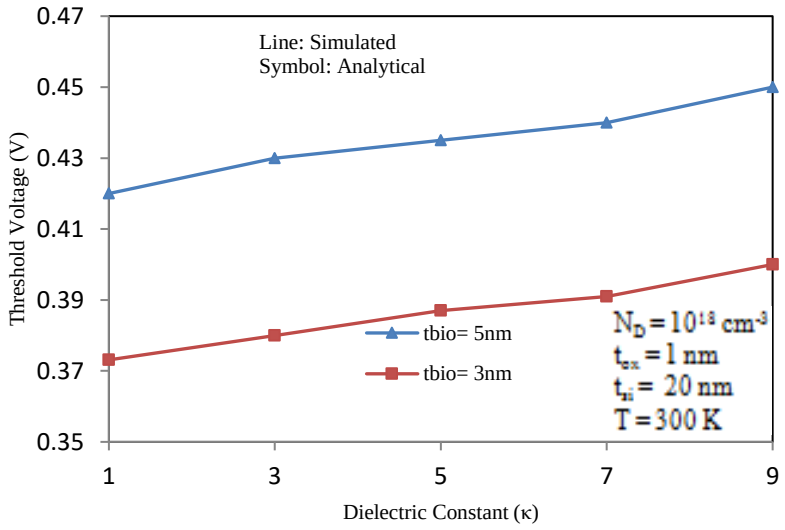
(b)

Figure 4.2 Center Potential variation of JAM-CSG MOSFET based biosensor **(a)** when neutral biomolecules (κ = 1, 3, 5, 7, 9) are present in the nanogap cavity and **(b)** when charged biomolecules (N_f = 7E+11 Cm^{-2} to -7E+11 Cm^{-2} when κ = 5) are filled in the nanogap cavity.

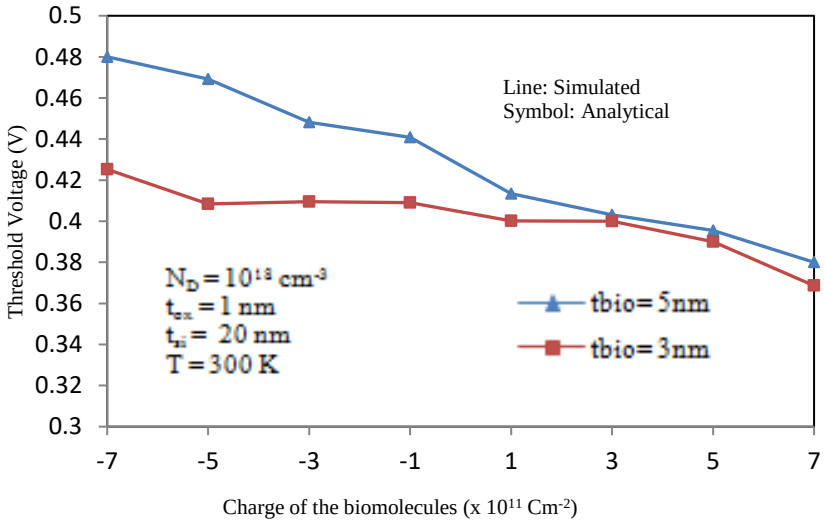
4.4.2 Threshold Voltage

Threshold Voltage is the most important parameter and it is utilized as the sensing parameter for the MOSFET- based sensors. It is utilized to detect the biomolecules interacting with the device by the change in the value of threshold voltage i.e., the difference between threshold voltage with biomolecules and without biomolecules. Figure 4.3 depicts the threshold voltage variability [33] across the channel length for the JAM- MOSFET due to the influence of the neutral and charged biomolecules for different cavity heights (t_{bio} = 3 nm and 5 nm). Neutral biomolecules (for instance, protein, biotin, streptavidin) possesses distinct dielectric constants. So, in order to examine such biomolecules, dielectric constant of the material is varied from κ = 1 to 9. Figure 4.3 (a) depicts this threshold voltage variation due to the existence of neutral biomolecules and is noticed that there is an increase in threshold voltage as the dielectric constant is incremented. It can also be noted that as the cavity height is increasing from t_{bio} = 3nm to 5nm, threshold voltage also increases for all the dielectric constants. Figure 4.3 (b) depicts the influence of positively and negatively charged (for

example, DNA) biomolecules upon the device's threshold voltage. When cavity region is occupied by the positively charged biomolecules, then the threshold voltage is decreasing and when filled with negatively charged biomolecules, an increment in the threshold voltage is noticed. Further, when cavity height is increasing, an increase in threshold voltage is also noticed for all the charged biomolecules (positive or negative).



(a)

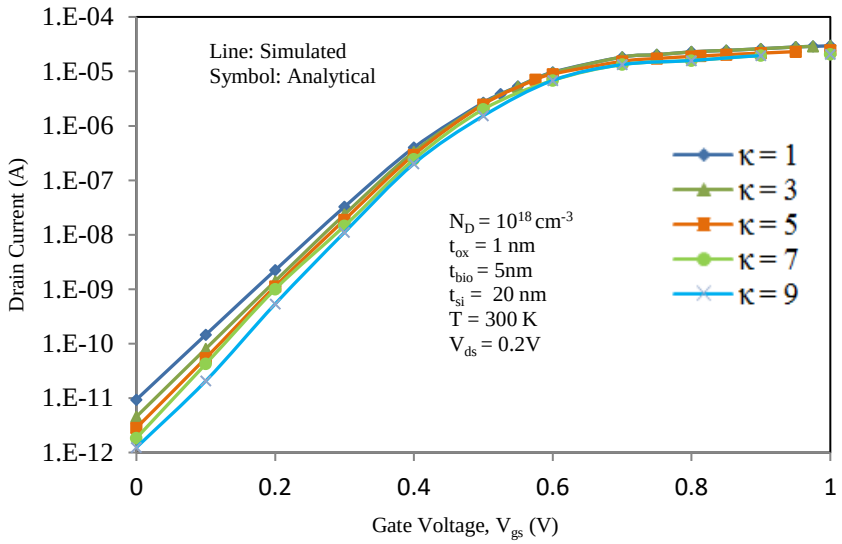


(b)

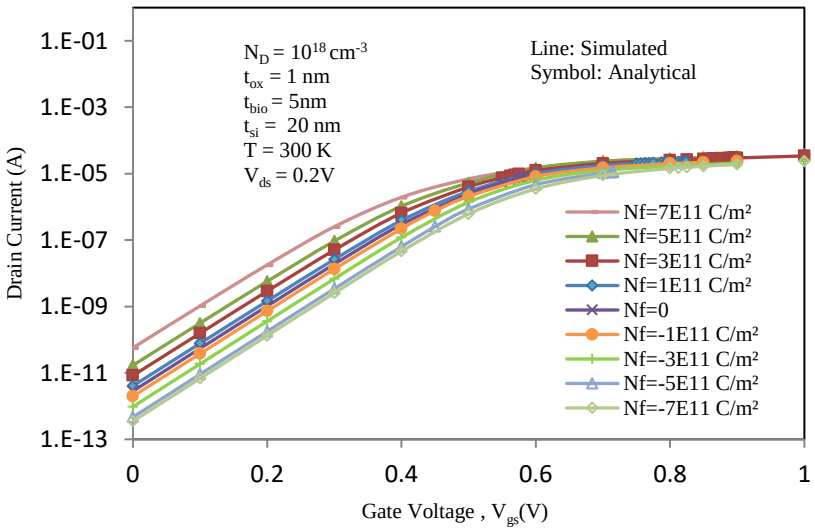
Figure 4.3 Threshold voltage variation for distinct cavity heights in JAM-CSG MOSFET based biosensor (t_{bio}) **(a)** when neutral biomolecules (for κ = 1, 3, 5, 7, 9) are present in the nanogap cavity and **(b)** when charged biomolecules (N_f = 7E+11 Cm^{-2} to -7E+11 Cm^{-2} when κ = 5) are filled in the nanogap cavity.

4.4.3 Drain Current

Transfer characteristics curve (drain current vs. gate voltage) [34, 35] also gets influenced owing to the existence of neutral and charged biomolecules and this happens because of the change in the flat band voltage, stated as:$\Delta V_{fb} = qN_f/C_{gap}$; where, $C_{gap} = \varepsilon_{bio}/t_{bio}$ [28].



(a)



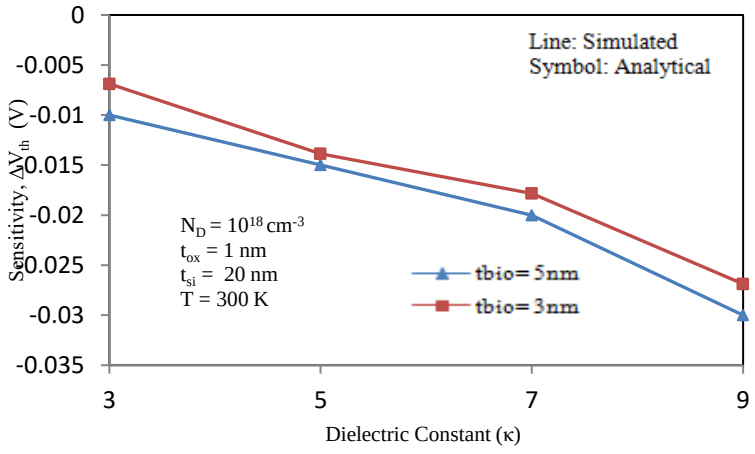
(b)

Figure 4.4 Transfer characteristics of JAM-CSG MOSFET based biosensor **(a)** when neutral biomolecules (for κ = 1, 3, 5, 7, 9) are present in the nanogap cavity and **(b)** when charged biomolecules (N_f = 7E+11 Cm^{-2} to -7E+11 Cm^{-2} when κ = 5) are present.

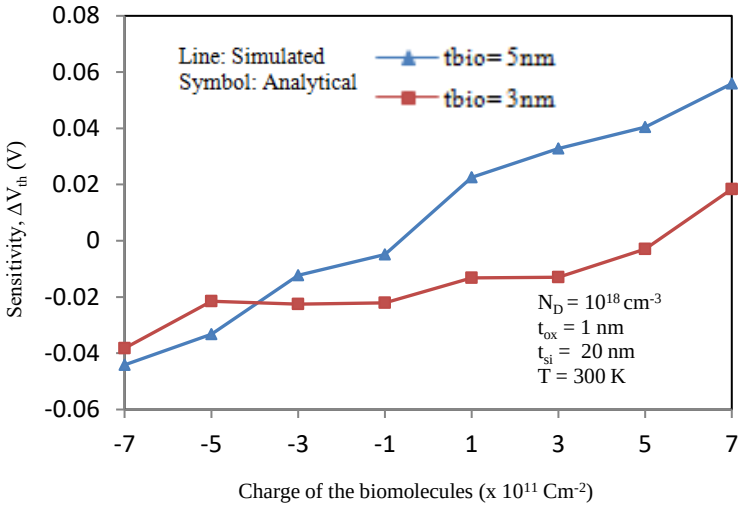
Figure 4.4 (a) represents the impact of neutral biomolecules upon the transfer characteristics and to study this effect, permittivity of the neutral biomolecules is varied (κ = 1, 3, 5, 7, 9). It is noticed that with the increment in the dielectric constant, OFF current is decreasing and the ON current remains almost same for all the values of dielectric constant considered. Figure 4.4 (b) portrays the influence of charged biomolecules upon the transfer characteristics of the MOSFET. During the interaction of the positively charged biomolecules, an increase in the OFF current is noticed and when interacting with the negatively charged biomolecules, OFF current decrements. I_{on} current remains almost constant for positively as well as negatively charged biomolecules.

4.4.4 Sensitivity

Figure 4.5 depicts the device's sensitivity [36, 37] under the situation during which the nanogap cavity is being simulated with the biomolecules (neutral and charged) considering distinct cavity heights. The sensitivity parameter due to the interaction of neutral biomolecules is illustrated in Figure 4.5 (a) and is noticed that with the rise in the dielectric constant (κ = 1, 3, 5, 7, 9), the sensitivity parameter decreases. Also, the rate at which it is decreasing is high, which reveals the higher sensitivity of the device when neutral biomolecules interact. Also, with the increment in the cavity height, there is a rise in the sensitivity factor. Figure 4.5 (b) displays the device's sensitivity when charged biomolecules are simulated. During the presence of positively charged biomolecules, the sensitivity parameter increases and when negatively charged biomolecules are there, then this parameter decreases.



(a)



(b)

Figure 4.5 Variation of Sensitivity factor ΔV_{th} in JAM-CSG MOSFET based biosensor **(a)** when neutral biomolecules (for κ = 1, 3, 5, 7, 9) are present in the nanogap cavity and **(b)** when charged biomolecules (N_f = 7E+11 Cm^{-2} to -7E+11 Cm^{-2} when κ = 5) are present.

As, t_{bio} is increasing from 3nm to 5nm, a good variation in sensitivity factor can be noted for all the charged biomolecules. The change in sensitivity corresponding to charged biomolecules is very high and thus, from the Figure 4.5, it is verified that the device exhibits good sensitivity towards the biomolecules (both neutral and charged).

4.4.5 Comparison with analogous devices

Comparison of our proposed device has been conducted with the other published works. Table 4.4 contrasts our proposed device, JAM-CSG MOSFET based biosensor with the dielectrically modulated FET (DM-FET) and Source-Engineered Schottky- FET (SE-SB- FET) as a label-free biosensor [38]. The parameter taken for comparison is drain current sensitivity ($S_{I_{ds}}$), which is given by:

$$S_{I_{ds}} = \left(\frac{I_{ON}^{bio} - I_{ON}^{air}}{I_{ON}^{air}}\right) \tag{4.32}$$

The values of $S_{I_{ds}}$ have been obtained for all of the FETs under comparison, when charged biomolecules interacts in the nanogap cavity (considering, dielectric constants, κ = 5 and 7). From the Table 4.4, it is noticed; in general, that JAM-CSG MOSFET is possessing improved drain current sensitivity.

Table 4.4

Comparison Based Upon Sensitivity Parameter

	Drain Current Sensitivity, ($S_{I_{ds}}$)					
	κ = 5			**κ = 7**		
Biomolecules Concentration (Cm^{-2})	**DM-FET**	**SE-SB-FET**	**JAM-CSG MOSFET**	**DM-FET**	**SE-SB-FET**	**JAM-CSG MOSFET**
-1E11	0.60	1.60	1.90	0.80	2.30	1.40
-5E11	0.25	0.50	0.69	0.50	1.15	1.20
-1E12	0.10	0.25	0.44	0.20	0.20	0.41

4.5 Summary

A biosensor based JAM- CSG MOSFET has been introduced in this chapter for the purpose of label- free detection of the biomolecules. Analytical modeling for this device has also been proposed utilizing the Poisson's equation under the relevant boundary constraints. The influence of the biomolecules (both neutral and charged) upon the various device's performance characteristics, like center potential, drain current, threshold voltage, sensitivity have been examined. Analytical and simulated results obtained are corresponding well with each other. Threshold voltage change has been used as the sensitivity parameter for detecting the biomolecules and from the outcomes we noticed that the threshold voltage is changing at a very remarkable rate for both the neutral and charged biomolecules. So, it concludes that our proposed device, JAM-CSG MOSFET based biosensor functions as an outstanding device for diagnosing the biomolecules (both neutral and charged) with very high sensitivity and thereby proves to be more applicable as a biosensor.

4.6 References

[1] Fahad, Hossain M., and Muhammad M. Hussain. "High-performance silicon nanotube tunneling FET for ultralow-power logic applications." *IEEE transactions on electron devices* 60, no. 3 (2013): 1034-1039.

[2] Wang, Runsheng, Jing Zhuge, Ru Huang, Yu Tian, Han Xiao, Liangliang Zhang, Chen Li, Xing Zhang, and Yangyuan Wang. "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation." *IEEE transactions on Electron Devices* 54, no. 6 (2007): 1288-1294.

[3] Colinge, Jean Pierre. "Multi-gate soi mosfets." *Microelectronic Engineering* 84, no. 9-10 (2007): 2071-2076.

[4] Wu, Yu-Sheng, and Pin Su. "Sensitivity of gate-all-around nanowire MOSFETs to process variations—A comparison with multigate MOSFETs." *IEEE transactions on electron devices* 55, no. 11 (2008): 3042-3047.

[5] Sarkar, Angsuman, Aloke Kumar Das, Swapnadip De, and Chandan Kumar Sarkar. "Effect of gate engineering in double-gate MOSFETs for analog/RF applications." *Microelectronics Journal* 43, no. 11 (2012): 873-882.

[6] Kumar, Manoj, Subhasis Haldar, Mridula Gupta, and R. S. Gupta. "Impact of gate material engineering (GME) on analog/RF performance of nanowire Schottky-barrier gate all around (GAA) MOSFET for low power wireless applications: 3D T-CAD simulation." *Microelectronics journal* 45, no. 11 (2014): 1508-1514.

[7] Loan, Sajad A., S. Qureshi, and S. Sundar Kumar Iyer. "A novel partial-ground-plane-based MOSFET on selective buried oxide: 2-D simulation study." *IEEE Transactions on Electron Devices* 57, no. 3 (2010): 671-680.

[8] Colinge, Jean-Pierre, Chi-Woo Lee, Aryan Afzalian, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi et al. "Nanowire transistors without junctions." *Nature nanotechnology* 5, no. 3 (2010): 225-229.

[9] Ferhati, H., and F. Djeffal. "Planar junctionless phototransistor: A potential high-performance and low-cost device for optical-communications." *Optics & Laser Technology* 97 (2017): 29-35.

[10] Doria, Rodrigo Trevisoli, Marcelo Antonio Pavanello, Renan Doria Trevisoli, Michelly de Souza, Chi-Woo Lee, Isabelle Ferain, Nima Dehdashti Akhavan et

al. "Junctionless multiple-gate transistors for analog applications." *IEEE Transactions on Electron Devices* 58, no. 8 (2011): 2511-2519.

[11] Chebaki, E., F. Djeffal, H. Ferhati, and T. Bentrcia. "Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions." *Superlattices and Microstructures* 92 (2016): 80-91.

[12] Djeffal, F., H. Ferhati, and T. Bentrcia. "Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions." *Superlattices and Microstructures* 90 (2016): 132-140.

[13] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design." *IEEE Transactions on Device and Materials Reliability* 14, no. 1 (2014): 418-425.

[14] Trivedi, Nitin, Manoj Kumar, Subhasis Haldar, S. S. Deswal, Mridula Gupta, and R. S. Gupta. "Analytical modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG)." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 29, no. 6 (2016): 1036-1043.

[15] Kim, Tae Kyun, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong-Il Moon, Gi Seong Lee et al. "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation." *IEEE electron device letters* 34, no. 12 (2013): 1479-1481.

[16] Narang, Rakhi, KV Sasidhar Reddy, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "A dielectric-modulated tunnel-FET-based biosensor for label-free detection: Analytical modeling study and sensitivity analysis." *IEEE transactions on electron devices* 59, no. 10 (2012): 2809-2817.

[17] Chen, Kuan-I., Bor-Ran Li, and Yit-Tsong Chen. "Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation." *Nano today* 6, no. 2 (2011): 131-154.

[18] Baek, David J., Juan P. Duarte, Dong-Il Moon, Chang-Hoon Kim, Jae-Hyuk Ahn, and Yang-Kyu Choi. "Accumulation mode field-effect transistors for improved sensitivity in nanowire-based biosensors." *Applied Physics Letters* 100, no. 21 (2012): 213703.

[19] Bergveld, Piet. "Thirty years of ISFETOLOGY: What happened in the past 30 years and what may happen in the next 30 years." *Sensors and Actuators B: Chemical* 88, no. 1 (2003): 1-20.

[20] Im, Hyungsoon, Xing-Jiu Huang, Bonsang Gu, and Yang-Kyu Choi. "A dielectric-modulated field-effect transistor for biosensing." *Nature nanotechnology* 2, no. 7 (2007): 430-434.

[21] Kim, Jee-Yeon, Jae-Hyuk Ahn, Sung-Jin Choi, Maesoon Im, Sungho Kim, Juan Publo Duarte, Chang-Hoon Kim, Tae Jung Park, Sang Yup Lee, and Yang-Kyu Choi. "An underlap channel-embedded field-effect transistor for biosensor application in watery and dry environment." *IEEE transactions on nanotechnology* 11, no. 2 (2011): 390-394.

[22] Siu, William M., and Richard SC Cobbold. "Basic properties of the electrolyte—SiO 2—Si system: physical and theoretical aspects." *IEEE Transactions on Electron Devices* 26, no. 11 (1979): 1805-1815.

[23] Kim, Tae Kyun, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong-Il Moon, Gi Seong Lee et al. "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation." *IEEE electron device letters* 34, no. 12 (2013): 1479-1481.

[24] Dwivedi, Praveen, and Abhinav Kranti. "Dielectric modulated biosensor architecture: Tunneling or accumulation based transistor?." *IEEE Sensors Journal* 18, no. 8 (2018): 3228-3235.

[25] Kim, Sungho, David Baek, Jee-Yeon Kim, Sung-Jin Choi, Myeong-Lok Seol, and Yang-Kyu Choi. "A transistor-based biosensor for the extraction of physical properties from biomolecules." *Applied Physics Letters* 101, no. 7 (2012): 073703.

[26] Busse, Stefan, Volker Scheumann, Bernhard Menges, and Silvia Mittler. "Sensitivity studies for specific binding reactions using the biotin/streptavidin system by evanescent optical methods." *Biosensors and Bioelectronics* 17, no. 8 (2002): 704-710.

[27] Narang, Rakhi, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "Dielectric modulated tunnel field-effect transistor—A biomolecule sensor." *IEEE Electron Device Letters* 33, no. 2 (2011): 266-268.

[28] ATLAS, Device Simulator. "Silvaco International. Santa Clara." (2015).

[29] Chakraborty, Avik, and Angsuman Sarkar. "Analytical modeling and sensitivity analysis of dielectric-modulated junctionless gate stack surrounding gate MOSFET (JLGSSRG) for application as biosensor." *Journal of Computational Electronics* 16, no. 3 (2017): 556-567.

[30] Narang, Rakhi, Manoj Saxena, and Mridula Gupta. "Investigation of dielectric modulated (DM) double gate (DG) junctionless MOSFETs for application as a biosensors." *Superlattices and Microstructures* 85 (2015): 557-572.

[31] Jazaeri, Farzan, Lucian Barbut, Adil Koukab, and J-M. Sallese. "Analytical model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime." *Solid-State Electronics* 82 (2013): 103-110.

[32] Jaiswal, Nivedita, and Abhinav Kranti. "Modeling short-channel effects in core–shell junctionless MOSFET." *IEEE Transactions on Electron Devices* 66, no. 1 (2018): 292-299.

[33] Trevisoli, Renan Doria, Rodrigo Trevisoli Doria, Michelly de Souza, and Marcelo Antonio Pavanello. "Threshold voltage in junctionless nanowire transistors." *Semiconductor Science and Technology* 26, no. 10 (2011): 105009.

[34] Arora, Narain D. *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media, 2012.

[35] Ortiz-Conde, Adelmo, FJ Garcıa Sánchez, Juin J. Liou, Antonio Cerdeira, Magali Estrada, and Yaxing Yue. "A review of recent MOSFET threshold voltage extraction methods." *Microelectronics reliability* 42, no. 4-5 (2002): 583-596.

[36] Parihar, Mukta Singh, and Abhinav Kranti. "Enhanced sensitivity of double gate junctionless transistor architecture for biosensing applications." *Nanotechnology* 26, no. 14 (2015): 145201.

[37] Chakraborty, Avik, and Angsuman Sarkar. "Analytical modeling and sensitivity analysis of dielectric-modulated junctionless gate stack surrounding gate MOSFET (JLGSSRG) for application as biosensor." *Journal of Computational Electronics* 16, no. 3 (2017): 556-567.

[38] Hafiz, Syed Adeebul, M. Ehteshamuddin, and Sajad A. Loan. "Dielectrically modulated source-engineered charge-plasma-based Schottky-FET as a label-free biosensor." *IEEE Transactions on Electron Devices* 66, no. 4 (2019): 1905-1910.

CHAPTER 5

Non-Uniform Doping Dependent Electrical Parameters of Dual- Metal Gate All Around Junctionless Accumulation-Mode Nanowire FET (DMGAA-JAM-NWFET)

5.1 Introduction

Shrinking of device dimensions has brought the advancement in the semiconductor industry and leads to various unwanted problems like short channel and hot carrier effects (SCEs and HCEs) [1-3]. To tackle with these problems, various structures namely, double-gate FET, triple-gate, GAA MOSFET, etc. [4-6] have been proposed. Among these, GAA MOSFET provides better control of the gate across the channel. GAA MOSFET can have vertical structure (VGAA) or horizontal (lateral) structure (LGAA) [7]. Channel in the case of VGAA is a vertical nanopillar and a nanowire in the case of LGAA. Due to the unfavourable electrical characteristics caused by VGAA over LGAA [7], we have incorporated LGAA in our device structure. Also, development of sharp junctions across the source and drain takes place in nanowire FETs. So, to deal with this issue, another device, junctionless transistor (JLT) [8-11] was introduced, in which absence of junctions provides improved electrical properties, lower leakage current and easy fabrication. But, JLT also possesses decaying carrier's mobility leading to decreased drain current and transconductance [12-14]. To eliminate these problems, Junctionless Accumulation Mode (JAM) MOSFET was proposed [15-17]. In this MOSFET, the doping of the channel is done moderately lower than the source/drain, providing increased conductivity and better performance than JLT. However, SCEs are not negligible in JAM, so, a dual-metal with gate stacked [18-20] JAM MOSFET was proposed. Dual- Metal gates provide enhanced carrier injection effect, gate transport efficiency and better gate control [21, 22].

5.1.1 Non- Uniform Doping

All the above stated devices have considered channel to be uniformly doped. But it is quite tough to achieve uniform doping during the fabrication process due to several steps involved such as heating and annealing steps performed after ion implantation [23]. This issue may lead to the fabrication of a MOSFET with peak doping done at the channel's surface and lesser doping done at the bottom surface, i.e., a non-uniform doping profile [24, 25]. Adan *et al.* [26] and Goto *et al.* [27] reported the fabrication of such a graded channel JLFET with non-uniform doping profile. Also, longitudinal non-uniform doping through graded-channel devices can also be achieved [28]. Such type of non-uniform doping profile is possible for devices possessing channel length upto 50nm. However, the application of such a doping profile could be impeditive for shorter devices/lower-doped devices due to the small number of dopant atoms. Improvements in the MOSFET characteristics were also reported for the non-uniformly doped channel [29, 30].

Thus, this chapter presents an analytical analysis of a Dual-Metal Gate All Around Junctionless Accumulation- Mode Nanowire FET (DMGAA-JAM-NWFET) possessing a horizontal-like non-uniform doping profile. The 2-D electrostatic potential distribution is evaluated using Poisson's equation under the applicable boundary conditions. Also, the impact of straggle length parameter and the peak doping concentration upon the device behaviour is also examined. For authenticating the obtained analytical outcomes, TCAD simulations were also performed. Both the results were contrasted and found to be in good agreement. The outcomes obtained for non-uniform doped DMGAA-JAM-NWFET are also compared with that of uniformly doped DMGAA-JAM-NWFET and finer electrical characteristics were noticed for non-uniformly doped device.

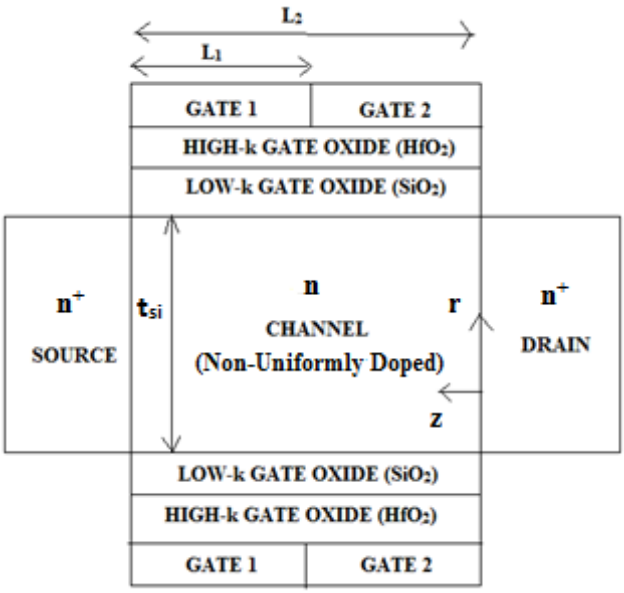
5.2 Schematic Description and Simulation Approach

5.2.1 Schematic Description

Figures 5.1 (a) and (b) illustrates the respective 3- D and 2-D schematic of the non-uniformly doped DMGAA-JAM-NWFET with dual metal gates placed side-by-side [31-33], i.e., gate1 present towards the source end and gate2 present towards the drain end, possessing work-functions ϕ_1 and ϕ_2 respectively (where, $\phi_1 > \phi_2$). High-k gate oxide material HfO_2 is also used as a gate stack with the SiO_2 layer. The channel is non-

uniformly doped with a horizontal-like profile with the peak doping concentration, N_D(peak) = 10^{19} /cm^3. Such desired doping profile can be reached as discussed by Adan *et al.* [26]. The simulated results for various straggle parameters have been obtained and are compared with the analytical results and are in good agreement, thus showing the validity of our proposal model. The structural specifications utilized are presented in Table 5.1.

(a)



(b)

Figure 5.1 (a) 3-D and (b) 2-D schematic of DMGAA-JAM-NWFET.

Table 5.1

Structural Specifications for DMGAA-JAM-NWFET

Specification	DMGAA-JAM-NWFET
Channel Length (L_G)	50 nm
Channel Doping (N_D)	N_D(peak) = 10^{19}/cm^3
Source/Drain Doping (N_D^+)	10^{20}/cm^3
Gate Stack Oxide Materials	SiO_2 (k = 3.9) and HfO_2 (k = 25)
Gate Stack Oxide Thickness	SiO_2- 1 nm and HfO_2- 1nm
Silicon Pillar Width (W_{si})	10 nm
Gate Work- Functions	ϕ_1= 5.0 eV and ϕ_2 = 4.8 eV

5.2.2 Simulation Approach

Simulations have been performed by making use of ATLAS-3D device simulator [34]. The models employed during the simulation are all described in Table 5.2.

Table 5.2

Description of Models

Models	Description
Recombination Model	The SRH– recombination model is incorporated for the analysis of the minority recombination effects.
Mobility Models	Concentration and Field Dependent Mobility models (CONMOB and FLDMOB) are incorporated for correlating the low-field mobility at 300K.
Statistics	Boltzmann Model is employed during simulation for examining the Carrier Statistics.
Methods	For the numerical solution, Newton and Gummel methods are called concurrently.

5.3 Analytical Analysis

5.3.1 Electrostatic Potential

The 2-D Poisson's equation [36-38] in the cylindrical co-ordinates is given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\psi_i(r,z)}{\partial r}\right)+\frac{\partial^2\psi_i(r,z)}{\partial z^2}=-\frac{qN_D(z)}{\varepsilon_{si}},\quad i=1,2 \tag{5.1a}$$

or

$$\frac{\partial^2\psi_i(r,z)}{\partial r^2}+\frac{1}{r}\left(\frac{\partial\psi_i(r,z)}{\partial r}\right)+\frac{\partial^2\psi_i(r,z)}{\partial z^2}=-\frac{qN_D(z)}{\varepsilon_{si}} \tag{5.1b}$$

where, $\psi(r,z)$ denotes the potential distribution, r and z denotes the co-ordinates for vertical and horizontal axis respectively, q be the electronic charge, ε_{si} be the dielectric constant of Si. $N_D(z)$ corresponds to the horizontal-type non-uniform doping profile distribution over the channel and is stated as:

$$N_D(z)=N_{D(peak)}\exp\left[-\frac{(z-\mu)^2}{2\sigma^2}\right] \tag{5.2}$$

where, $N_{D(peak)}$ be the peak doping concentration, μ be the position for peak doping and σ be the straggle length parameter.

The parabolic profile function used to solve equation (5.1) is given as:

$$\psi_j(r,z)=P_{j0}(z)+P_{j1}(z)\,r+P_{j2}(z)\,r^2,\quad 0\leqslant z\leqslant L \tag{5.3}$$

where, the coefficients P_{j0} (z), P_{j1} (z), P_{j2} (z) are computed by applying appropriate boundary conditions.

For dual metal gate materials, employing parabolic profile [39], equation (5.1) is solved for to get:

$$\psi_1(r,z)=P_{10}(z)+P_{11}(z)\,r+P_{12}(z)\,r^2,\quad 0\leqslant z\leqslant L_1 \qquad (Region\ 1)$$

$$\psi_2(r,z)=P_{20}(z)+P_{21}(z)\,r+P_{22}(z)\,r^2,\quad L_1\leqslant z\leqslant L_2 \qquad (Region\ 2) \tag{5.4}$$

where, L_1 and L_2 be the gate1 length and total channel length respectively.

Boundary conditions used during the analytical modeling are:

(1). Center potential:

$$\psi(r,z)|_{r=0} = \psi_c(z) \tag{5.5}$$

(2). Surface potential existing near to the source side:

$$\psi(r,z=0) = \psi_s(r)|_{z=0} = \phi_{bi} \tag{5.6}$$

where, ϕ_{bi} be the built- in voltage.

(3). Surface potential existing near to the drain side:

$$\psi(r,z=L) = \psi_s(r)|_{z=L} = \phi_{bi} + V_{ds} \tag{5.7}$$

where, V_{ds} be the voltage across drain and source.

(4). Central Electric field:

$$E = \frac{\partial\psi(r,z)}{\partial r}|_{r=0} = 0 \tag{5.8}$$

(5). Electric field existing at the intersection of the substrate and oxide:

$$\frac{\partial\psi(r,z)}{\partial r}|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{V_{gs}-\psi_{si}\left(r=\frac{t_{si}}{2},z\right)}{\frac{t_{si}}{2}ln\left(1+\frac{2t_{oxeff}}{t_{si}}\right)}\right] \tag{5.9}$$

where, V_{gs} denotes the gate potential, t_{si} denotes the substrate's thickness, t_{oxeff} denotes the effective oxide thickness, stated as:

$$t_{oxeff} = t_{ox} + \frac{\varepsilon_{ox}\ .\ t_{hk}}{\varepsilon_{hk}}$$

where, ε_{ox} and ε_{hk} indicates the dielectric constants; t_{ox} and t_{hk} indicates the thicknesses of SiO_2 layer and HfO_2 layer respectively.

(6). Continuity of Surface Potential at the intersection of the gates (gate 1 and gate 2):

$$\psi_{s_1}(r,L_1)|_{r=\frac{t_{si}}{2}} = \psi_{s_2}(r,L_1)|_{r=\frac{t_{si}}{2}} \tag{5.10}$$

(7). Continuity of Electric flux at the intersection of the gates:

$$\frac{\partial\phi_{s_1(R,z)}}{\partial z}|_{z=L_1} = \frac{\partial\phi_{s_2(R,z)}}{\partial z}|_{z=L_2} \tag{5.11}$$

On applying the above boundary conditions, the coefficients $P_{0i}(z)$, $P_{1i}(z)$ and $P_{2i}(z)(i=0,1,2)$ were obtained as:

$$P_{10}(z) = \psi_{c_1}(z) \tag{5.12a}$$

$$P_{20}(z) = \psi_{c_2}(z) \tag{5.12b}$$

$$P_{11}(z) = 0 \tag{5.12c}$$

$$P_{21}(z) = 0 \tag{5.12d}$$

$$P_{12}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \tag{5.12e}$$

$$P_{22}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \tag{5.12f}$$

where, ψ_{gs_1}, ψ_{gs_2} are the gate to source potentials across gate1 and gate2 respectively and C_{ox} is the capacitance per unit area and is given by:

$$C_{ox} = \frac{2\varepsilon_{ox}}{t_{si}\ln\left(1 + \frac{2t_{oxeff}}{t_{si}}\right)}$$

Now, using the above coefficient values, the center potential specified by equation (5.4a and 5.4b) is rewritten as:

$$\psi_1(r, z) = \psi_{c_1}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)\right] \tag{5.13a}$$

$$\psi_2(r, z) = \psi_{c_2}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)\right] \tag{5.13b}$$

At $r = \frac{t_{si}}{2}$, $\psi\left(r = \frac{t_{si}}{2}, z\right) = \psi_{si}(r = \frac{t_{si}}{2}, z)$, so the equation (5.13) for ψ_{si_1} and ψ_{si_2} becomes:

$$\psi_{si_1}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_1(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z)}{\varepsilon_{si} t_{si}}\right) \tag{5.14a}$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z)}{\varepsilon_{si} t_{si}}\right) \tag{5.14b}$$

Rearranging the terms in (14) yields

$$\psi_{si_1}(r = \frac{t_{si}}{2}, z) = \left[\frac{4\varepsilon_{si}\psi_{c_1(z)} + t_{si}C_{ox}\psi_{gs_1}}{4\varepsilon_{si} + t_{si}C_{ox}}\right] \tag{5.15a}$$

$$\psi_{si_2}(r = \frac{t_{si}}{2}, z) = \left[\frac{4\varepsilon_{si}\psi_{c_2(z)} + t_{si}C_{ox}\psi_{gs_2}}{4\varepsilon_{si} + t_{si}C_{ox}}\right] \tag{5.15b}$$

The JLT works on bulk to source conduction mechanism, therefore, the center potential is to be calculated for $r = 0$. Center potential for two different metals is solved and is given as:

$$\frac{\partial^2 \psi_{c_1}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_1(z)} - \eta_1\right], \qquad 0 \leqslant z \leqslant L_1 \tag{5.16a}$$

$$\frac{\partial^2 \psi_{c_2}(z)}{\partial z^2} = \frac{1}{\lambda^2}\left[\psi_{c_2(z)} - \eta_2\right], \qquad L_1 \leqslant z \leqslant L_2 \tag{5.16b}$$

where, the characteristic length (λ), η_1 and η_2 are respectively given by

$$\frac{1}{\lambda^2} = \frac{16\, C_{ox}}{4\varepsilon_{si} t_{si} + {t_{si}}^2 C_{ox}} \tag{5.17}$$

$$\eta_1 = \psi_{gs_1} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{5.18a}$$

$$\eta_2 = \psi_{gs_2} + \frac{qN_D t_{si}}{4C_{ox}} + \frac{qN_D {t_{si}}^2}{16\varepsilon_{si}} \tag{5.18b}$$

General solution of equation (5.15a and 5.15b) comes out as:

$$\psi_{C1}(z) = A\, e^{z/\lambda} + B e^{-z/\lambda} + \eta_1 \tag{5.19a}$$

$$\psi_{C2}(z) = C\, e^{z/\lambda} + D e^{-z/\lambda} + \eta_2 \tag{5.19b}$$

where, the coefficients *A*, *B*, *C* and *D* are computed as:

$$A = \frac{e^{-L_1/\lambda}(\phi_{bi} - \eta_1) - V_{DS}/2 + \eta_1}{(e^{-L_1/\lambda} - e^{L_1/\lambda})} \tag{5.20a}$$

$$B = \frac{e^{L_1/\lambda}(\phi_{bi} - \eta_1) - V_{DS}/2 + \eta_1}{(e^{L_1/\lambda} - e^{-L_1/\lambda})} \tag{5.20b}$$

$$C = \frac{e^{-L_2/\lambda}\left(\frac{V_{DS}}{2} - \eta_2\right) - e^{-L_1/\lambda}(\phi_{bi} + V_{DS} - \eta_2)}{e^{(L_1 - L_2)/\lambda} - e^{(L_2 - L_1)/\lambda}} \tag{5.20c}$$

$$D = \frac{e^{L_2/\lambda}\left(\frac{V_{DS}}{2} - \eta_2\right) - e^{L_1/\lambda}(\phi_{bi} + V_{DS} - \eta_2)}{e^{(L_2 - L_1)/\lambda} - e^{(L_1 - L_2)/\lambda}} \tag{5.20d}$$

5.3.2 Electric Field

Differentiating the center potential (5.19a and 5.19b) gives the distribution of the electric field:

$$E = -\frac{d\psi_{C1}(z)}{dz}, \qquad 0 \leqslant z \leqslant L_1$$

$$E = -\frac{d\psi_{C2}(z)}{dz}, \qquad L_1 \leqslant z \leqslant L_2$$

(5.21)

5.3.3 Drain Current

Drain current corresponding to various regions is specified as:

$$I_{ds} = \begin{cases} I_{sub}, 0 \leq V_{gs} \leq V_{th} \\ I_{lin}, V_{th} \leq V_{gs} \leq V_{sat} \\ I_{sat}, V_{sat} \leq V_{gs} \leq 1.0V \end{cases} \tag{5.22}$$

During the operation of the transistor in the subthreshold region, the current flowing across the source and drain is known as the subthreshold drain current [39, 40] and is stated as:

$$I_d(V_{gs}, V_{ds}, z) = \frac{\left[2\pi N_D \mu \left\{1 - e^{\frac{-(qV_{ds})}{(k_B T)}}\right\}\right]}{\int_0^{L_1+L_2+L_3} \frac{1}{\int_0^r r.e\left(\frac{q\psi(V_{gs}, V_{ds}, z)}{k_B T}\right) dr} dz} \tag{5.23}$$

where, μ is the electron mobility equal to 1300 cm^2/Vs, k_B is the Boltzmann constant having value equal to1.38 × 10^{-23} J/K and T is the temperature considered as 300 K.

For linear region,

$$I_{lin} = \frac{\pi t_{si} \mu C_{oxeff1} E_c}{(E_c L + V_{ds})} \left[(V_{gs} - V_{th})^{\frac{\alpha}{2}} V_{ds} - \frac{\theta_{short} {V_{ds}}^2}{2} \right] \tag{5.24}$$

E_c is the critical electric field, $\theta_{short}$is the subthreshold slope factor, given as

$$\theta_{short} = 0.1/(\partial\varphi(0, z_{min})/\partial V_{gs} \; at \; V_{gs} = V_{th}) \tag{5.25}$$

$$V_{ths} = V_{th}(1 - \theta_{short}) \tag{5.26}$$

$$C_{oxeffi} = \frac{2\varepsilon_{oxi}}{t_{si} ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)} \tag{5.27}$$

α and β are the fitting parameters and here there values considered are 1.24 and 0.756 respectively.

For saturation region,

$$I_{sat} = \frac{\pi t_{si}\mu C_{oxeff2}}{\left(1+\frac{V_{dsat}}{E_C L}\right)(L-L_{sat})}\left[\beta\left(V_{gs}-V_{th}\right)^{\frac{\alpha}{2}}V_{ds} - \frac{\theta_{short}{V_{ds}}^2}{2}\right] \quad (5.28)$$

5.3.4 Subthreshold Slope (SS)

It is given as the change in gate voltage, V_{gs} for every one decade change in drain current, I_{ds}:

$$SS = \left[\frac{d\log(I_{ds})}{d(V_{gs})}\right]^{-1} \qquad mV/decade \quad (5.29)$$

5.3.5 Transconductance (g_m) and Output Conductance (g_d)

Transconductance (g_m) is the change in drain current with respect to the change in gate voltage, keeping the drain voltage constant and is given by,

$$g_m = \left(\partial I_d/\partial V_{gs}\right)|_{V_{ds=constant}} \quad (5.30)$$

At a particular value of gate voltage (V_{gs}), transconductance (g_m) is maximum. Also before and after this value, transconductance decreases. This maximum value of g_m is called as peak transconductance, g_{mo}.

$$g_m = g_{m_o}\left(1-\frac{V_{gs}}{V_p}\right) \quad (5.31)$$

where, $g_{m_o} = \frac{2I_{DSS}}{|V_P|}$, V_p is the pinch-off voltage equal to $V_p = V_{gs}$-V_{th} and I_{DSS} is the maximum drain current.

Output Conductance (g_d) is the change in drain current with respect to the change in drain voltage when gate voltage is kept constant and is given by,

$$g_d = (\partial I_d/\partial V_{ds})|_{V_{gs=constant}} \quad (5.32)$$

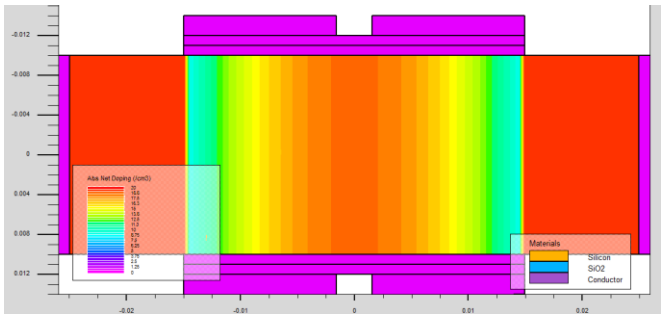
5.4 Results and Discussion

5.4.1 DMGAA-JAM-NWFET Device Model

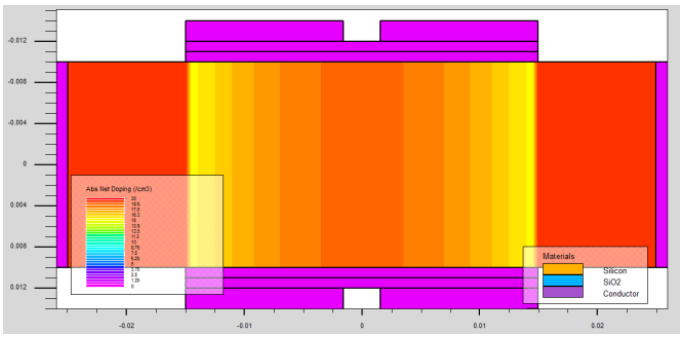
The device simulation for the considered device, DMGAA-JAM-NWFET has been carried out using ATLAS-3D simulator and the obtained outcomes are then contrasted with the analytical outcomes obtained from the model developed. Further, the device is

also simulated for various straggle length and peak doping concentration to study their influence upon the device's behavior [24, 40].

Figures 5.2 and 5.3 corresponds to the contour plots and doping profile curve respectively for doping concentration of DMGAA-JAM-NWFET at various straggle lengths i.e., σ = 3nm, 5nm and 7nm. It is noticed from these figures that the doping is high across the center of the channel and is decreasing towards both the sides of the channel i.e., a non-uniform doping profile is observed. Also, as straggle length is varying from σ = 3nm to 7nm, change in the profile can be noticed and is getting broadened.



(a)



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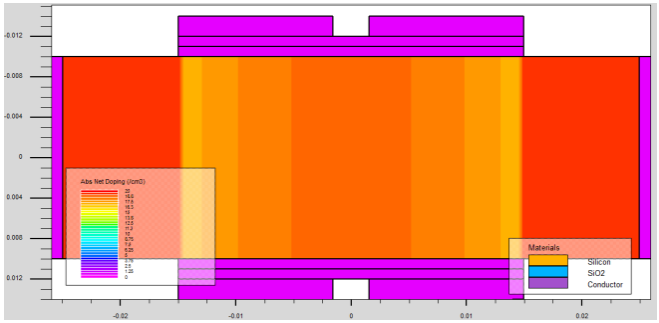

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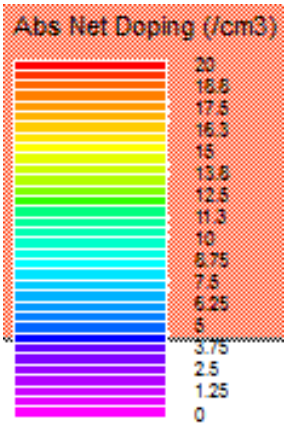


(d)

Figure 5.2 Contour Plots for Doping Concentration for DMGAA-JAM-NWFET at V_{gs} = 1.0V and V_{ds} = 0.2V for different straggle lengths, σ = (a) 3nm (b) 5nm (c) 7nm and (d) color coding scale used.

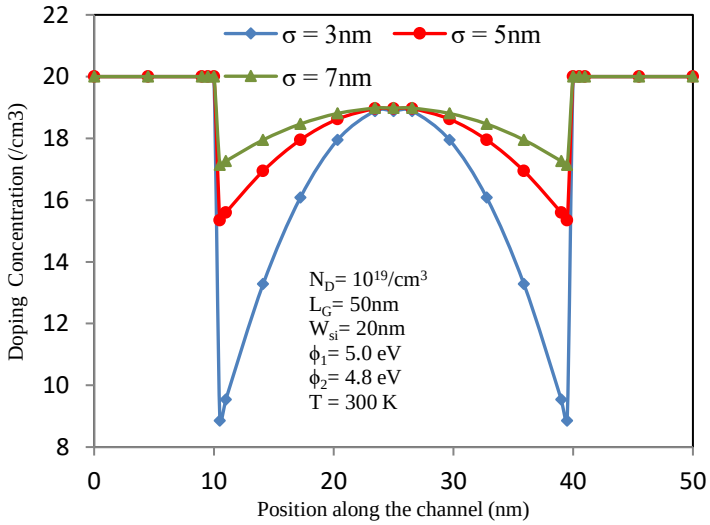
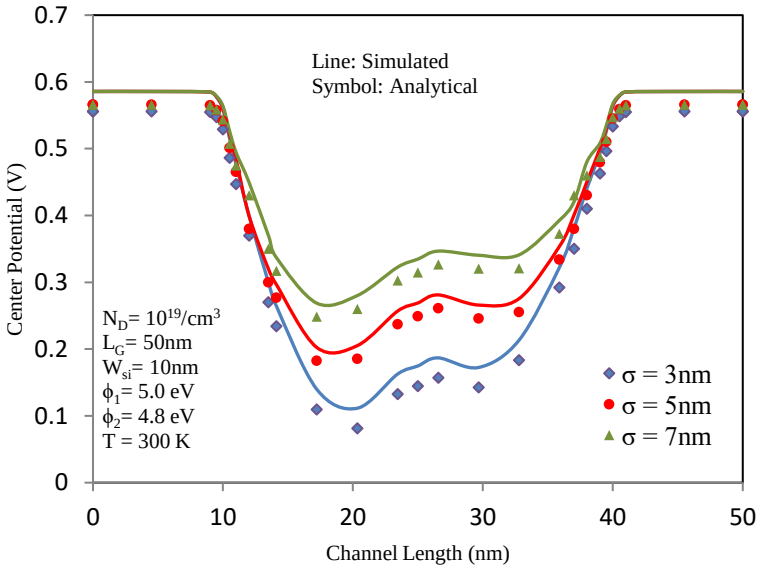


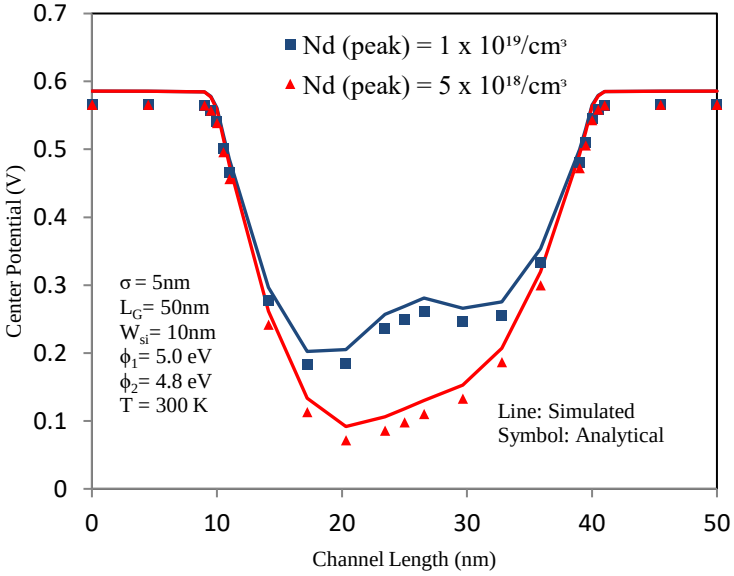
Figure 5.3 Doping profile curve for DMGAA-JAM-NWFET with straggle lengths, σ = 3nm, 5nm and 7nm.

Figures 5.4(a) and 5.4(b) illustrates the center potential against the length of the channel [41] for the considered device for different straggle lengths and peak doping concentrations respectively. Figure 5.4(a) indicates the center potential for straggle lengths, σ = 3nm, 5nm and 7nm. From this figure, it is seen that when there is decrease in the straggle length parameter (σ), the center potential is pulled down. This happens because the decrease in straggle length leads to more dominance of the gate across the channel, thereby enhancing the subthreshold characteristics and threshold voltage. Figure 5.4(b) indicates the center potential for different peak doping concentrations,

N_d(peak) = 1 x 10^{19}/cm^3 and 5 x 10^{18} /cm^3. Figure 5.4(b) displays the reduction in the potential barrier, owing to the SCEs, is balanced out by incrementing the channel's doping concentration [42]. Also, the simulated and analytical outcomes are observed to be matching well with each other.



(a)



(b)

Figure 5.4 Center potential variation of DMGAA-JAM-NWFET for different (a) straggle lengths (σ= 3nm, 5nm, 7nm) and (b) peak doping concentration (N_d (peak) =1 x 10^{19}/cm^3 and 5x10^{18}/cm^3)

Figure 5.5 indicates electric field across the channel against various straggle length parameter (σ = 3nm, 5nm and 7nm). The electric field peak is observed to be lower towards the drain side. This happens because of the lower work-function gate present at that side leading to reduced impact ionization. Also, as the straggle length parameter is decreasing, the electric field increases which means higher carrier transport efficiency or higher electron velocity.

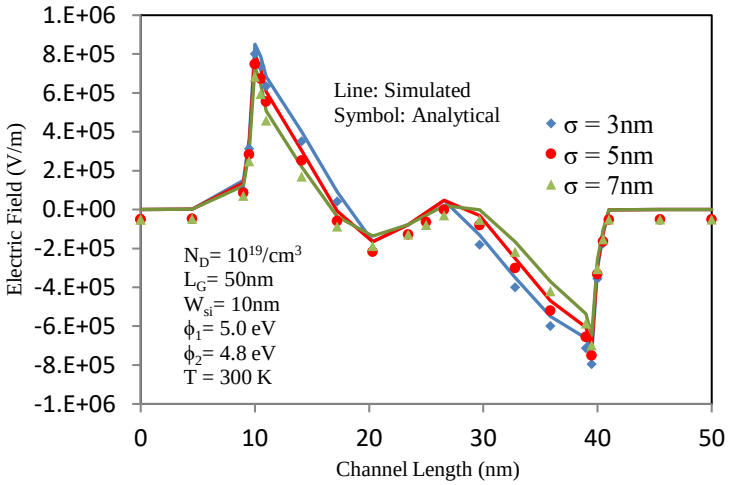
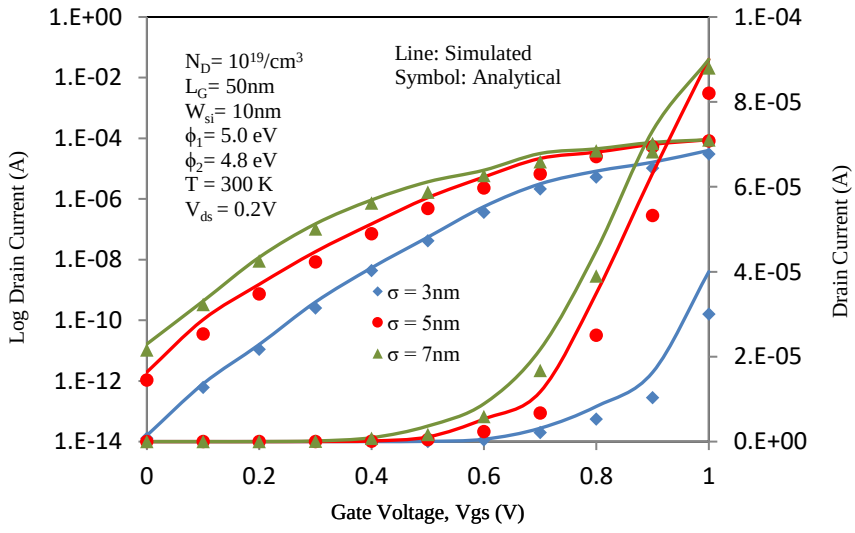
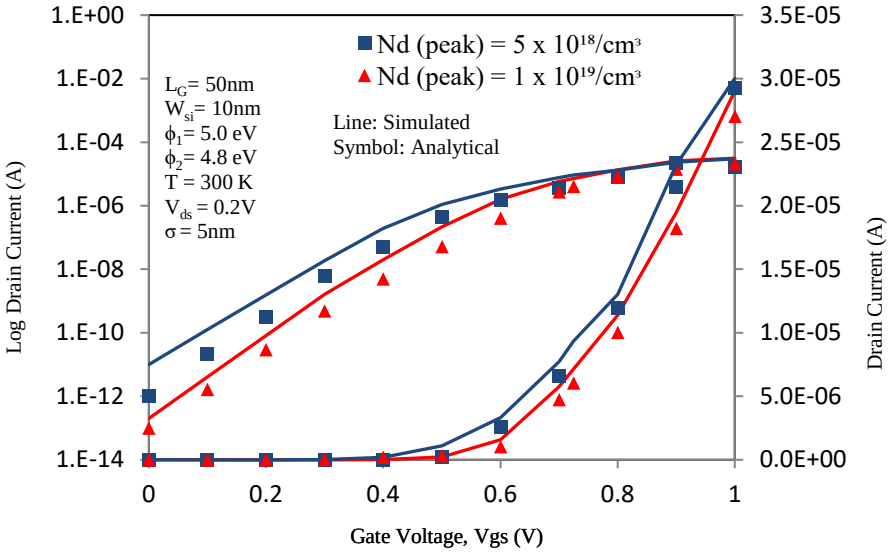


Figure 5.5 Electric field variation of DMGAA-JAM-NWFET for different straggle lengths, σ= 3nm, 5nm and 7nm.

Transfer characteristics (Drain current vs. V_{gs}) [43, 44] at V_{ds}= 0.2 V for various straggle lengths (σ = 3nm, 5nm and 7nm) are shown in Figure 5.6(a).



(a)



(b)

Figure 5.6 Drain current vs. gate voltage of DMGAA-JAM-NWFET for various (a) straggle lengths (σ= 3nm, 5nm, 7nm) and (b) peak doping concentration (N_d (peak) = 1 x 10^{19}/cm³ and 5x10^{18}/cm³).

From Figure 5.6(a), an increase in I_{on}/I_{off} can be observed with the reduction in the straggle length. This occurs because the gate controllability of the device becomes better at the lower straggle lengths, leading towards the reduction in the leakage current. I_{on}/I_{off} for σ = 3nm is observed to be almost hundred times to that for σ = 5nm, which indicates its usefulness for high switching speed applications. Figure 5.6(b) illustrates the transfer characteristics for peak doping concentrations, N_d(peak)= 1 x 10^{19}/cm^3 and 5 x 10^{18} /cm^3. From the figure, we can notice the change in I_{on}/I_{off} at different peak doping concentration levels. Simulated and analytical results are in good agreement.

Figure 5.7 denotes the transfer characteristics curve for different drain to source voltages (V_{ds} = 0.2, 0.4, 0.6, 0.8 and 1.0V). From this figure, we observe that the threshold voltage is almost same for every value of V_{ds} considered. This can also be seen in Figure 5.8, where threshold voltage value is nearly equal to 0.35V for every V_{ds} (= 0.2, 0.4, 0.6, 0.8 and 1.0V) considered.

Transconductance, already defined in section 3.5, is another important parameter for analysis of the device [45]. Figure 5.9 shows the variation of transconductance with gate to source voltage at different straggle lengths. It is observed, that the maximum transconductance is observed for σ = 7nm, making it more suitable for high gain applications. Greater the straggle length, lesser will be the effective channel length (L_{eff})

of the device, thus, leading to the increased drain current. Transconductance depends upon I_{ds} and V_{gs}, thus, an increase in I_{ds} for higher σ, exhibits higher transconductance.

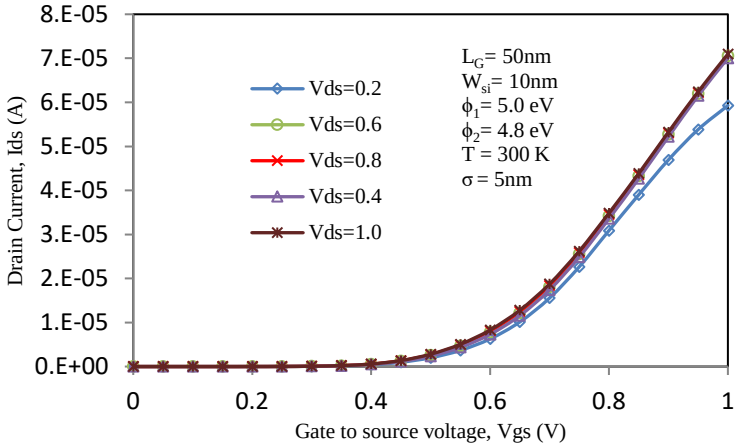


Figure 5.7 Transfer characteristics of DMGAA-JAM-NWFET for different drain to source voltages (V_{ds} = 0.2, 0.4, 0.6, 0.8 and 1.0V).

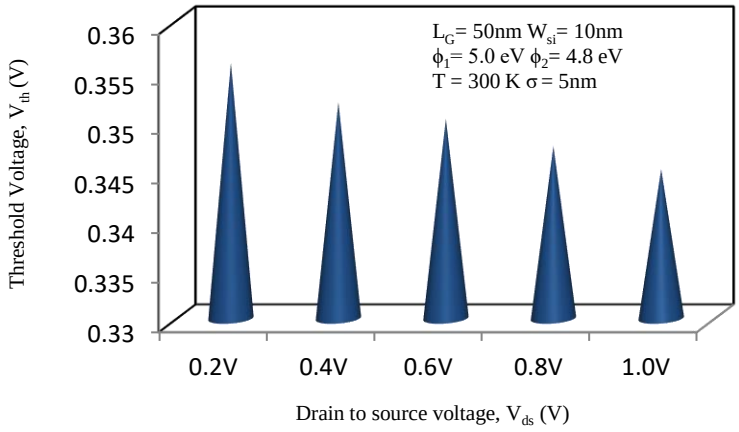


Figure 5.8 Threshold voltage of DMGAA-JAM-NWFET at various drain to source voltages, V_{ds}.

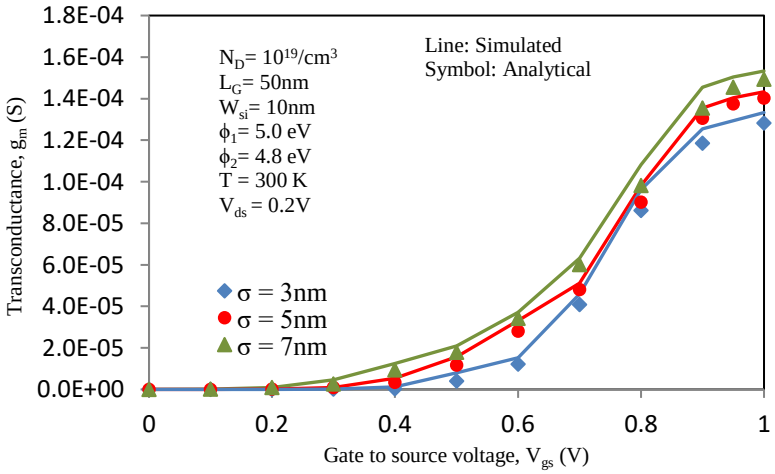


Figure 5.9 Transconductance of DMGAA-JAM-NWFET for different straggle lengths, σ= 3nm, 5nm and 7nm.

Output characteristic (Drain current vs. drain voltage) curve at gate voltage, V_{gs} = 1V is shown in Figure 5.10 for various straggle lengths. As seen from Figure 5.10, the drain current is almost same for all the three straggle lengths (σ = 3nm, 5nm and 7nm), but slightly higher for σ = 7nm as compared to current for lower straggle values. This happens due to the reduction in the effective channel length (L_{eff}) with the increase in the σ parameter, leading to increase in the drain current. Figure 5.11 gives the output conductance, g_d with respect to the drain voltage for different straggle lengths. From Figure 5.11, it is observed that the output conductance is more for σ = 3nm and gets reduced for σ = 5nm and 7nm.

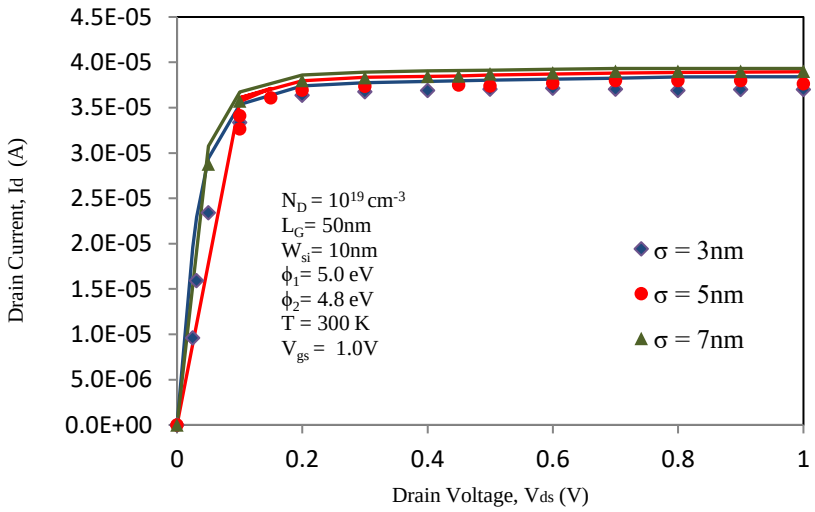


Figure 5.10 Output characteristics of DMGAA-JAM-NWFET for different straggle lengths, σ = 3nm, 5nm and 7nm.

Next key parameter is Subthreshold Slope (*SS*) of the device [46] given by equation (5.29). This parameter is ideally equal to 60mV/ decade at 300K. Figure 5.12 shows the *SS* for DMGAA-JAM-NWFET considering different straggle lengths, σ = 3nm, 5nm and 7nm. Straggle length for a non-uniform distribution, considered in Figure 5.12, is the distance from the peak density where its value is 1/exp(0.5) ~ 0.606 of the peak density The value of *SS* for σ = 7nm is approximately 71mV/decade and reaches to approximately 66mV/ decade for σ = 3nm. Thus, it can be inferred that the *SS* is getting better at lower straggle lengths. At higher straggle lengths, there is decrement in the channel length. This leads to increase in the SS significantly due to the severe increase

in the short channel effects. Hence, better *SS* is obtained at lower values of σ, meaning better command of the gate across the channel.

Further, it is noticed that SS is better for lower value of σ, while various other parameters acquired are better at higher σ, σ= 7nm. So, a compromise can be made, we can use an intermediate value of σ (σ= 5nm), to get the optimum results of the device in all respects.

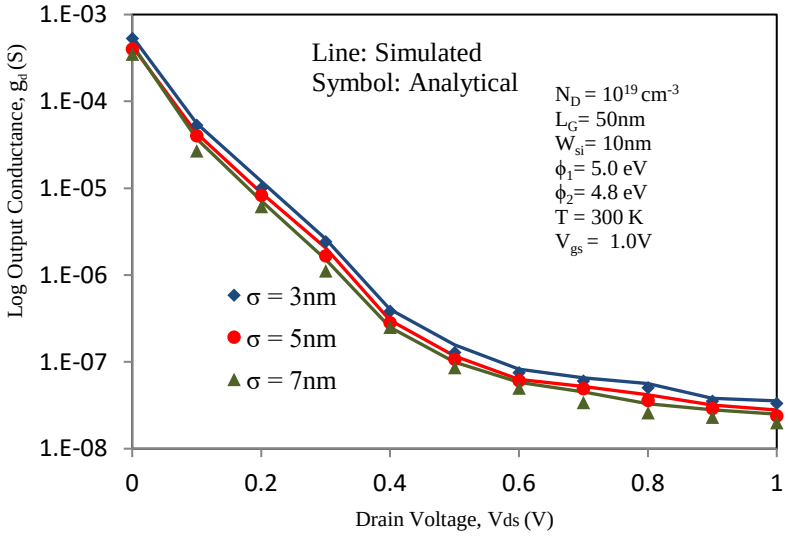


Figure 5.11 Output Conductance of DMGAA-JAM-NWFET for different straggle lengths, σ= 3nm, 5nm and 7nm.

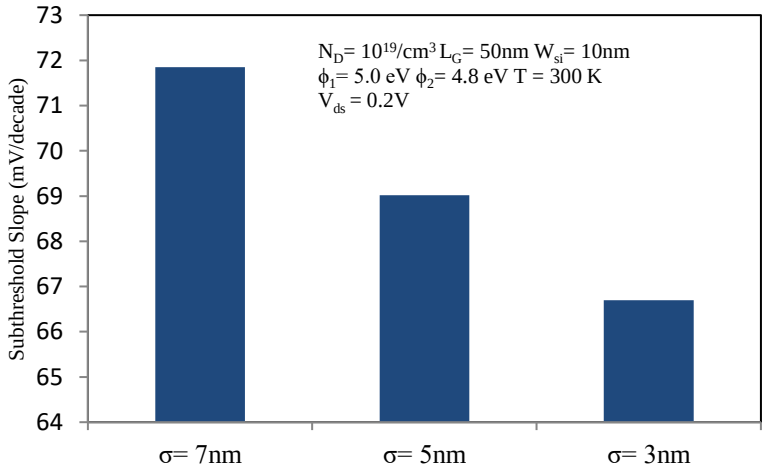


Figure 5.12 Subthreshold slope of DMGAA-JAM-NWFET for different straggle lengths, σ = 3nm, 5nm and 7nm.

5.4.2 Comparison with other devices

5.4.2.1. Comparison with analogous devices with and without junctions

This section gives the comparison of our considered device, DMGAA-JAM-NWFET with an analogous device possessing junction, i.e., GAA-NWFET and another device that is junctionless, GAA-JAM-NWFET (considering each device to be non-uniformly doped). Figures 5.13 and 5.14 give the Transfer and Output characteristic curves for these three devices (GAA, GAA-JAM and DMGAA-JAM NWFET) respectively. It can be deduced from the Figure 5.13 that the Transfer characteristics are better for DMGAA-JAM-MOSFET as compared to the other devices. This indicates the better gate control and higher ON current for DMGAA-JAM-NWFET. From Figure 5.14, it is observed that the drain current is also higher for the case of DMGAA-JAM-NWFET.

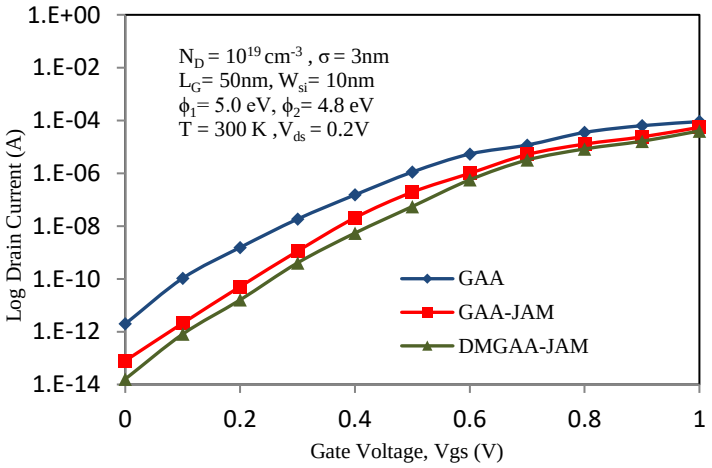


Figure 5.13 Transfer characteristics for GAA, GAA-JAM and DMGAA-JAM-NWFET.

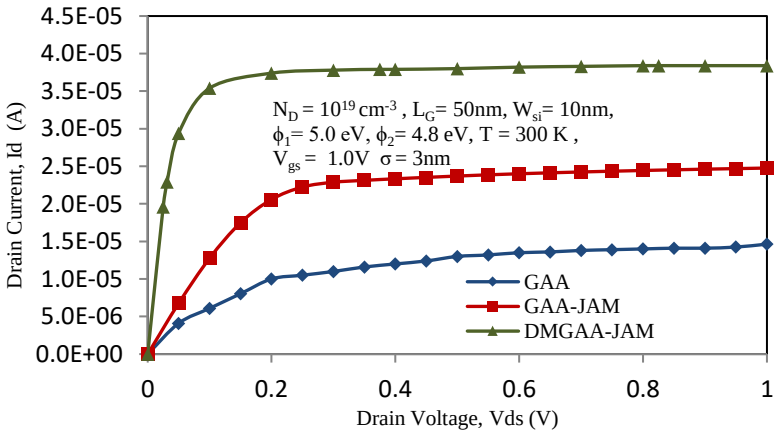


Figure 5.14 Output characteristics for GAA, GAA-JAM and DMGAA-JAM-NWFET.

Table 5.3 specifies various SCE parameters for these related devices. Highest I_{ON}/ I_{OFF} ratio (approx. 10^9) and finer subthreshold slope is noted for DMGAA-JAM-NWFET device, marking the device possessing better performance over the device having junctions and present single-gate junctionless device.

Table 5.3

GAA vs. GAA-JAM vs. DMGAA-JAM-NWFET

Performance Parameter	**I_{on}/ I_{off}**	**Subthreshold Slope (mV/decade)**
GAA-NWFET	4.59E+07	69.80
GAA-JAM-NWFET	6.93E+08	68.44
DMGAA-JAM-NWFET	2.51E+09	66.70

5.4.2.2. Comparison with Uniformly doped device

Further, the performance of non-uniformly doped DMGAA-JAM-NWFET is also contrasted versus the uniformly doped DMGAA-JAM-NWFET [38]. Comparison is done on the grounds of various performance parameters like I_{on}/I_{off} ratio, peak transconductance value, subthreshold slope and is shown in Table 5.4.

Table 5.4

Non- Uniformly doped vs. Uniformly doped DMGAA-JAM-NWFET

Performance Parameter	**I_{on}/ I_{off}**	**Peak g_m (S)**	**Subthreshold Slope (mV/decade)**
Uniformly-doped DMGAA-JAM-NWFET	2.33E+09	9.73E-05	71.65
Non-Uniformly-doped DMGAA-JAM-NWFET	2.51E+09	1.50E-04	66.70

It is infered from this table, that non-uniformly –doped DMGAA-JAM-NWFET shows significant improvement over the uniformly-doped device. I_{on}/I_{off} ratio has increased and peak g_m value is also more for the case of non-uniformly –doped device.

Subthreshold slope has also improved for non-uniformly –doped DMGAA-JAM-NWFET and is more near to 60mV/decade. These values infers that the non-uniformly-doped DMGAA-JAM-NWFET is more powerful device and is more suitable for applications demanding high-frequnecy and high-speed.

5.5 Summary

Analytical modeling for DMGAA-JAM-NWFET possessing non-uniform doping has been proposed using the Poisson's equation employing suitable boundary conditions. Various electrical parameters like center potential, electric field, transconductance, etc. were inferred. The device is also examined for various straggle lengths and channel's peak doping concentrations. It was noticed that both these parameters can be further optimized for additional escalation in the performance of this device. Analytical and simulated outcomes correspond well with each other. Also, the device was compared with the uniformly- doped DMGAA-JAM-NWFET and was deduced that the non-uniformly doped DMGAA-JAM-NWFET possesses better electrical properties, i.e., I_{on}/I_{off} ratio, peak g_m, subthreshold slope and thus, is more beneficial for applications requiring elevated frequency and switching capability.

5.6 References

[1] Oh, Sang-Hyun, Don Monroe, and Jack M. Hergenrother. "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs." *IEEE electron device letters* 21, no. 9 (2000): 445-447.

[2] Xie, Qian, Chia-Jung Lee, Jun Xu, Clement Wann, Jack Y-C. Sun, and Yuan Taur. "Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs." *IEEE Transactions on Electron Devices* 60, no. 6 (2013): 1814-1819.

[3] Jimenez, David, Juan J. Saenz, Benjamin Iniguez, Jordi Sune, Lluis F. Marsal, and Josep Pallares. "Modeling of nanoscale gate-all-around MOSFETs." *IEEE Electron device letters* 25, no. 5 (2004): 314-316.

[4] Colinge, Jean Pierre. "Multi-gate soi mosfets." *Microelectronic Engineering* 84, no. 9-10 (2007): 2071-2076.

[5] Hong, Chuyang, Jun Zhou, Jiasheng Huang, Rui Wang, Wenlong Bai, James B. Kuo, and Yijian Chen. "A general and transformable model platform for emerging multi-gate MOSFETs." *IEEE Electron Device Letters* 38, no. 8 (2017): 1015-1018.

[6] Sharma, Rupendra Kumar, Charalabos A. Dimitriadis, and Matthias Bucher. "A comprehensive analysis of nanoscale single-and multi-gate MOSFETs." *Microelectronics journal* 52 (2016): 66-72.

[7] Ye, Shujun, Kikuo Yamabe, and Tetsuo Endoh. "Ultimate vertical gate-all-around metal–oxide–semiconductor field-effect transistor and its three-dimensional integrated circuits." *Materials Science in Semiconductor Processing* 134 (2021): 106046.

[8] Colinge, Jean-Pierre, Abhinav Kranti, Ran Yan, Chi-Woo Lee, Isabelle Ferain, Ran Yu, N. Dehdashti Akhavan, and Pedram Razavi. "Junctionless nanowire transistor (JNT): Properties and design guidelines." *Solid-State Electronics* 65 (2011): 33-37.

[9] Jazaeri, Farzan, and Jean-Michel Sallese. *Modeling nanowire and double-gate junctionless field-effect transistors*. Cambridge University Press, 2018.

[10] Jazaeri, Farzan, Lucian Barbut, and Jean-Michel Sallese. "Modeling asymmetric operation in double-gate junctionless FETs by means of symmetric devices." *IEEE Transactions on Electron Devices* 61, no. 12 (2014): 3962-3970.

[11] Sahay, Shubham, and Mamidala Jagadesh Kumar. *Junctionless field-effect transistors: design, modeling, and simulation*. John Wiley & Sons, 2019.

[12] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design." *IEEE Transactions on Device and Materials Reliability* 14, no. 1 (2014): 418-425.

[13] Koukab, Adil, Farzan Jazaeri, and J-M. Sallese. "On performance scaling and speed of junctionless transistors." *Solid-state electronics* 79 (2013): 18-21.

[14] Jazaeri, Farzan, Lucian Barbut, and Jean-Michel Sallese. "Trans-capacitance modeling in junctionless symmetric double-gate MOSFETs." *IEEE transactions on electron devices* 60, no. 12 (2013): 4034-4040.

[15] Holtij, Thomas, Michael Graef, Franziska Marie Hain, Alexander Kloes, and Benjamn Iñíguez. "Compact model for short-channel junctionless accumulation mode double gate MOSFETs." *IEEE Transactions on Electron Devices* 61, no. 2 (2013): 288-299.

[16] Kim, Tae Kyun, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong-Il Moon, Gi Seong Lee et al. "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation." *IEEE electron device letters* 34, no. 12 (2013): 1479-1481.

[17] Trivedi, Nitin, Manoj Kumar, Subhasis Haldar, S. S. Deswal, Mridula Gupta, and R. S. Gupta. "Analytical modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG)." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 29, no. 6 (2016): 1036-1043.

[18] Darwin, S., and TS Arun Samuel. "A holistic approach on Junctionless dual material double gate (DMDG) MOSFET with high k gate stack for low power digital applications." *silicon* 12, no. 2 (2020): 393-403.

[19] Amin, S. Intekhab, and R. K. Sarin. "Charge-plasma based dual-material and gate-stacked architecture of junctionless transistor for enhanced analog performance." *Superlattices and Microstructures* 88 (2015): 582-590.

[20] Sarkar, Angsuman, Aloke Kumar Das, Swapnadip De, and Chandan Kumar Sarkar. "Effect of gate engineering in double-gate MOSFETs for analog/RF applications." *Microelectronics Journal* 43, no. 11 (2012): 873-882.

[21] Pravin, J. Charles, D. Nirmal, P. Prajoon, and J. Ajayan. "Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications." *Physica E: Low-dimensional systems and nanostructures* 83 (2016): 95-100.

[22] Aggarwal, Sonal, and Rajbir Singh. "Dual metal gate and conventional MOSFET at sub nm for analog application." *International Journal of VLSI Design & Communication Systems* 3, no. 1 (2012): 111.

[23] Dubey, Sarvesh, Pramod Kumar Tiwari, and S. Jit. "A two-dimensional model for the potential distribution and threshold voltage of short-channel double-gate metal-oxide-semiconductor field-effect transistors with a vertical Gaussian-like doping profile." *Journal of Applied Physics* 108, no. 3 (2010): 034518.

[24] Singh, Balraj, Deepti Gola, Kunal Singh, Ekta Goel, Sanjay Kumar, and Satyabrata Jit. "Analytical modeling of channel potential and threshold voltage of double-gate junctionless FETs with a vertical Gaussian-like doping profile." *IEEE Transactions on Electron Devices* 63, no. 6 (2016): 2299-2305.

[25] Cheng, Kangguo, Bruce B. Doris, Ali Khakifirooz, Pranita Kulkarni, and Tak H. Ning. "Method for fabricating junctionless transistor." U.S. Patent Application 13/618,054, filed March 28, 2013.

[26] Adan, Alberto O. "Semiconductor device with a non-uniformly doped channel." U.S. Patent 5,401,994, issued March 28, 1995.

[27] Goto, Ken-Ichi, and Zhiqiang Wu. "Non-uniform channel junction-less transistor." U.S. Patent 8,487,378, issued July 16, 2013.

[28] Mondal, Partha, Bahniman Ghosh, and Punyasloka Bal. "Planar junctionless transistor with non-uniform channel doping." *Applied Physics Letters* 102, no. 13 (2013): 133505.

[29] Mondal, Partha, Bahniman Ghosh, Punyasloka Bal, M. W. Akram, and Akshaykumar Salimath. "Effects of non-uniform doping on junctionless transistor." *Applied Physics A* 119, no. 1 (2015): 127-132.

[30] Tsai, Meng-Ju, Kang-Hui Peng, Chong-Jhe Sun, Siao-Cheng Yan, Chieng-Chung Hsu, Yu-Ru Lin, Yu-Hsien Lin, and Yung-Chun Wu. "Fabrication and

characterization of stacked poly-Si nanosheet with gate-all-around and multi-gate junctionless field effect transistors." *IEEE Journal of the Electron Devices Society* 7 (2019): 1133-1139.

[31] Dehzangi, Arash, A. Makarimi Abdullah, Farhad Larki, Sabar D. Hutagalung, Elias B. Saion, Mohd N. Hamidon, Jumiah Hassan, and Yadollah Gharayebi. "Electrical property comparison and charge transmission in p-type double gate and single gate junctionless accumulation transistor fabricated by AFM nanolithography." *Nanoscale research letters* 7 (2012): 1-9.

[32] Kim, Hyeong-Jin, Chul-Ho Lee, Dong-Wook Kim, and Gyu-Chul Yi. "Fabrication and electrical characteristics of dual-gate ZnO nanorod metal–oxide semiconductor field-effect transistors." *Nanotechnology* 17, no. 11 (2006): S327.

[33] Jang, Hyun-June, and Won-Ju Cho. "Fabrication of high-performance fully depleted silicon-on-insulator based dual-gate ion-sensitive field-effect transistor beyond the Nernstian limit." *Applied Physics Letters* 100, no. 7 (2012): 073701.

[34] ATLAS, Device Simulator. "Silvaco International. Santa Clara." (2015).

[35] Roy, Nirmal Ch, Abhinav Gupta, and Sanjeev Rai. "Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra low-power analog/RF circuits." *Microelectronics Journal* 46, no. 10 (2015): 916-922.

[36] Holtij, Thomas, Mike Schwarz, Alexander Kloes, and Benjamin Iniguez. "Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region." *Solid-state electronics* 90 (2013): 107-115.

[37] Gautam, Rajni, Manoj Saxena, R. S. Gupta, and Mridula Gupta. "Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localised charges." *Journal Of Computational and Theoretical Nanoscience* 9, no. 4 (2012): 602-610.

[38] Singh, Balraj, Deepti Gola, Kunal Singh, Ekta Goel, Sanjay Kumar, and Satyabrata Jit. "Analytical modeling of channel potential and threshold voltage of double-gate junctionless FETs with a vertical Gaussian-like doping profile." *IEEE Transactions on Electron Devices* 63, no. 6 (2016): 2299-2305.

[39] Kaushal, S., & Rana, A. K. (2022). Analytical model of subthreshold drain current for nanoscale negative capacitance junctionless FinFET. *Microelectronics Journal*, *121*, 105382.

[40] Kumari, Vandana, Ayush Kumar, Manoj Saxena, and Mridula Gupta. "Study of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) transistor including source drain depletion length: Model for sub-threshold behavior." *Superlattices and Microstructures* 113 (2018): 57-70.

[41] Pradhan, K. P., M. R. Kumar, S. K. Mohapatra, and P. K. Sahu. "Analytical modeling of threshold voltage for Cylindrical Gate All Around (CGAA) MOSFET using center potential." *Ain Shams Engineering Journal* 6, no. 4 (2015): 1171-1177.

[42] Jiang, Chunsheng, Renrong Liang, Jing Wang, and Jun Xu. "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs." *AIP Advances* 5, no. 5 (2015): 057122.

[43] Gnudi, A., S. Reggiani, E. Gnani, and G. Baccarani. "Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs." *IEEE Electron Device Letters* 33, no. 3 (2012): 336-338.

[44] Duarte, Juan Pablo, Sung-Jin Choi, and Yang-Kyu Choi. "A full-range drain current model for double-gate junctionless transistors." *IEEE transactions on electron devices* 58, no. 12 (2011): 4219-4225.

[45] Arora, Narain D. *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media, 2012

[46] Colinge, J. P., J. W. Park, and W. Xiong. "Threshold voltage and subthreshold slope of multiple-gate SOI MOSFETs." *IEEE Electron Device Letters* 24, no. 8 (2003): 515-517.

CHAPTER 6

Modeling of Dual- Metal Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DM-JAM-CSG) MOSFET for Cryogenic temperature Applications

6.1 Introduction

Certain applications including space, terrestrial and satellite communication requires semiconductor devices as the prime component in their circuits. The operating temperature plays an important role in these above-stated applications [1-3]. Although, the device exhibits effective characteristics at room temperature, it also requires investigation in its behavior at higher and lower temperature conditions. At extreme low temperatures, the properties of the material changes [1-3], this makes the topic relevant to be discussed upon.

Also, scaling of the device brings about various Short Channel and Hot Carrier Effects (SCEs and HCEs), thereby worsening the device functioning [4-7]. To deal with these effects, various gate engineering techniques, double-gate, tri-gate, quadruple- gate, cylindrical surrounding gate (CSG) MOSFETs, etc. were employed [8-11]. Amongst these, CSG MOSFET provides improved characteristics due to the extended gate control present all around the silicon film with no corner effect [12]. Apart from these benefits, CSG owns a limitation of formation of abrupt source-drain junctions.

This complication was overcome by the origination of the Junctionless Transistor (JLT) [13-15], which includes consistent doping, all over the source, drain and channel. Uniform doping leads to absence of source-drain junctions making the fabrication process easier and less costly. Besides this, drain current is lower in the case of JLTs leading to degradation of the carrier's mobility. Therefore, to curb this drawback, one more MOSFET, in which doping of channel was done slightly less than the source/drain was introduced and is known as Junctionless Accumulation Mode (JAM) MOSFET [16-17]. It possesses better conductivity and lesser SCEs when compared with the JLT. In order to further reduce these SCEs, an improved structure of JAM-MOSFET was introduced i.e., Dual- Metal JAM- CSG (DM-JAM-CSG) MOSFET, employing Dual-

Metal Gate and Dielectric Engineering. Dual Metal Gate Engineering employs two metal gates of different work functions, keeping the lower function metal gate at the drain end [18-21]. This lessens the influence of the high speed electrons at the drain end and thus, elevating the carrier efficiency. Gate Dielectric Engineering [22-23] employs using a high- k dielectric layer in addition to the SiO_2 layer. This helps to easily subsides the gate oxide leakage current, which is predominant phenomenon in the MOSFET devices. Thus, these two engineering approaches make our proposed device more efficient.

Utilizing gate engineering techniques, device dimensions can be scaled down. Apart from this, the effect of temperature upon the device's behavior also plays an important role [24-25]. Therefore, this chapter introduces the characterization of the Dual- Metal Junctionless Accumulation-Mode Nanowire FET (DM-JAM-NWFET) at cryogenic temperatures.

6.1.1 Cryogenic Analysis

Cryogenic refers to the branch of physics and engineering that deals with the production and effects of very low temperatures. The term is commonly used to describe temperatures below -150 ^{0}C (-238 ^{0}F) or even colder, often approaching absolute zero (-273.15 ^{0}C or -459.67 ^{0}F). Cryogenic technology involves the study and application of materials and processes at extremely low temperatures, typically using liquefied gases such as nitrogen, oxygen, hydrogen, and helium. Some common applications of cryogenic technology include:

- **Medical:** Cryogenics is used in medical applications such as cryopreservation, where biological samples (such as sperm, eggs, or tissues) are preserved at very low temperatures for future use.
- **Industrial**: In industries, cryogenics is used for processes like liquefied natural gas (LNG) production, metal treatment, and superconductivity applications.
- **Space Exploration:** Cryogenic fuels, such as liquid oxygen and liquid hydrogen, are used in rockets for space exploration.
- **Superconductivity:** Some materials exhibit superconductivity at extremely low temperatures, and cryogenics is essential for maintaining these temperatures in applications like maglev trains and certain medical devices.

- **Transportation:** Cryogenic technology is used in the transportation and storage of liquefied gases, such as LNG or compressed natural gas (CNG).

Cryogenic technology plays a crucial role in various scientific, industrial, and medical fields, enabling the study and manipulation of materials and processes at extremely low temperatures. Here are some common cryogenic temperatures and their corresponding values in both Celsius and Fahrenheit:

1. **Liquid Nitrogen:** Boils at around -196^{0}C (-321 ^{0}F).
2. **Liquid Oxygen:** Boils at approximately -183^{0}C (-297 ^{0}F).
3. **Liquid Hydrogen:** Boils at around -253^{0}C (-423 ^{0}F).
4. **Liquid Helium:** Boils at approximately -269^{0}C (-452 ^{0}F).

6.2 Cryogenic Analysis of MOSFETs

Cryogenic analysis of MOSFETs involves studying the behavior and performance of these electronic devices at extremely low temperatures, typically in the cryogenic range. This analysis is particularly important in applications such as low-temperature electronics, superconducting circuits, and quantum information processing. Here are some aspects of cryogenic analysis for MOSFETs:

- **Electrical Performance:** MOSFETs are semiconductor devices, and their electrical characteristics can be significantly influenced by temperature. Cryogenic analysis assesses parameters such as threshold voltage, mobility, and subthreshold slope at low temperatures to understand how MOSFETs behave in these extreme conditions.
- **Threshold Voltage Shift:** It determines the point at which the device turns on, can shift at cryogenic temperatures. This shift is crucial for designing circuits that operate reliably in low-temperature environments.
- **Subthreshold Behavior:** Cryogenic analysis examines the subthreshold characteristics of MOSFETs. This is essential for low-power applications and understanding leakage currents.
- **Transconductance and Output Conductance:** These are the key parameters of MOSFET that impact the device performance. Cryogenic analysis helps evaluate how these parameters change with temperature.

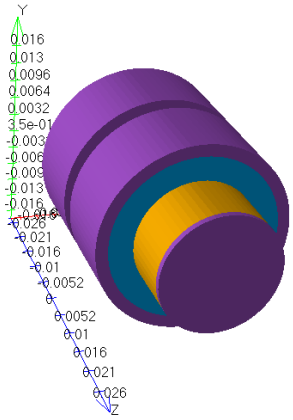
- **Noise Performance:** Cryogenic temperatures can affect the noise performance of electronic devices. Analyzing MOSFET noise at low temperatures is important for applications where minimizing noise is critical, such as in sensitive measurements or quantum computing.
- **Reliability and Longevity:** Understanding how MOSFETs perform at cryogenic temperatures is essential for assessing the reliability and longevity of electronic circuits in environments where low temperature is a factor.
- **Quantum Effects**: At extremely low temperatures, quantum effects become more pronounced. Cryogenic analysis of MOSFETs may involve exploring quantum mechanical phenomena and their impact on device performance, especially in the context of quantum computing or quantum information processing.

Cryogenic analysis of MOSFETs contributes to the development of electronic systems that can operate effectively in extreme conditions, enabling advancements in fields like space exploration, astrophysics, and quantum technologies. Thus, this chapter examines our proposed device at Cryogenic temperature. Mathematical model has also been developed by using the 2-D Poisson's equation under the relevant boundary conditions. It is perceived from the study that at cryogenic temperatures, the performance of the considered FET does not differ by a significant amount when compared to that at room temperature. By varying the temperature from 50K to 300K, it is noticed that the variation in center potential, electric field, transconductance, output conductance, drain current are almost minimum. The TCAD results were achieved by deploying ATLAS 3-D device simulator and were also contrasted along with the numerical results.

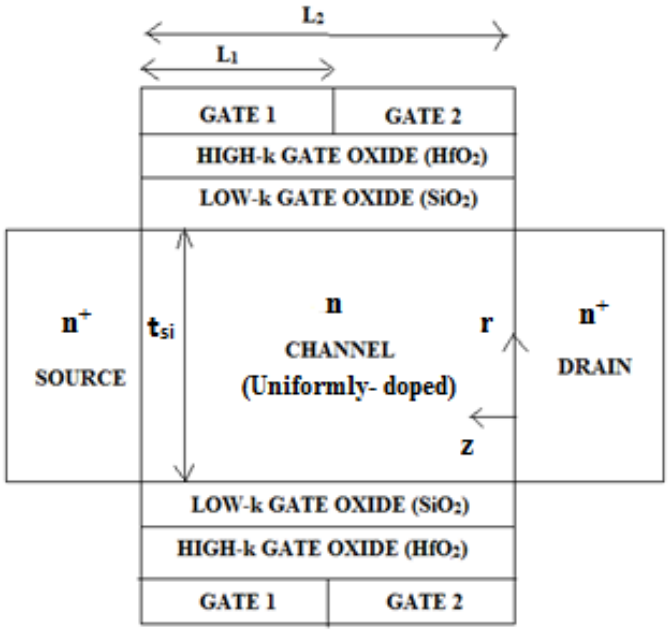
6.2 Device Design, Simulation Methodology and Device Calibration

6.2.1 Device Design

3-D and 2-D view of DM-JAM-CSG MOSFET is depicted in figure 6.1(a) and (b) respectively. The considered MOSFET comprises of dual metal gates, namely gate1 and gate2 with respective work- functions ϕ_1 and ϕ_2, where $\phi_1 > \phi_2$.



(a)



(b)

Figure 6.1 (a) 3-D and (b) 2-D view of DM-JAM-CSG MOSFET.

In this device, a gate stack is also present consisting of a high-k material HfO_2 together with a layer of SiO_2, such that the effective oxide thickness, t_{oxeff} becomes:

$$t_{oxeff} = t_{ox} + \frac{\varepsilon_{ox} \cdot t_{hk}}{\varepsilon_{hk}} \tag{6.1}$$

where, t_{ox} and t_{hk} are the respective thicknesses of SiO_2 and HfO_2 layers equal to 1nm each and ε_{ox}, ε_{hk} are the dielectric constants for SiO_2 and HfO_2 with the values of 3.9 and 25 respectively. For accumulation mode, the doping of channel is done a bit lower

than the source/drain regions. Various parametric values employed while designing the DM-JAM-CSG MOSFET are tabulated in Table 6.1.

Table 6.1

Parametric Values Employed for DM-JAM-CSG MOSFET

Parameters	**DM-JAM-CSG MOSFET**
Channel Length (L)	50 nm
Channel Doping (N_D)	10^{18}/cm^3
Source/Drain Doping (N_D^+)	10^{20}/cm^3
Thickness of the Gate Stack (t_{ox})	SiO_2- 1 nm HfO_2- 1nm
Thickness of the Silicon Pillar (t_{si})	20 nm
Work- Functions (ϕ_1 and ϕ_2)	$\phi_1 = 5.0$ eV (Rhodium) $\phi_2 = 4.8$ eV (Ruthenium)

6.2.2 Simulation Methodology

Device simulation is crucial for understanding, designing, and optimizing the performance of electronic devices. It is a computational technique used in semiconductor engineering to model the behaviour of electronic devices. Device simulation for DM-JAM-CSG MOSFET at various temperatures has been accomplished on the ATLAS 3-D device simulator [30] by taking into account the various physical models. Various models used during simulating this structure are: SRH recombination model, Concentration and Mobility Dependent models, Boltzmann Statistics model and Newton- Gummel methods. All these models are described in Table 6.2.

6.2.3. Device Calibration

Simulation data has been calibrated with the experimental results performed by Choi et al [31] and is illustrated in Figure 6.2. Both the experimental and simulated results are seen to be present in good correspondence with each other.

Table 6.2

Physical Models Used

Physical models	Description
Recombination Model	The SRH model considers carrier lifetime to be $1x10^{-7}$ s and incorporates minority recombination effects.
Concentration Dependent Model	CONMOB associates mobility with the doping concentration at 300K.
Mobility Model	FLDMOB is utilized to assist the impact of velocity saturation.
Statistics	Boltzmann Model is applied for examining the Carrier Statistics.
Methods	Newton Gummel method is called simultaneously for carrying out the numerical solution.

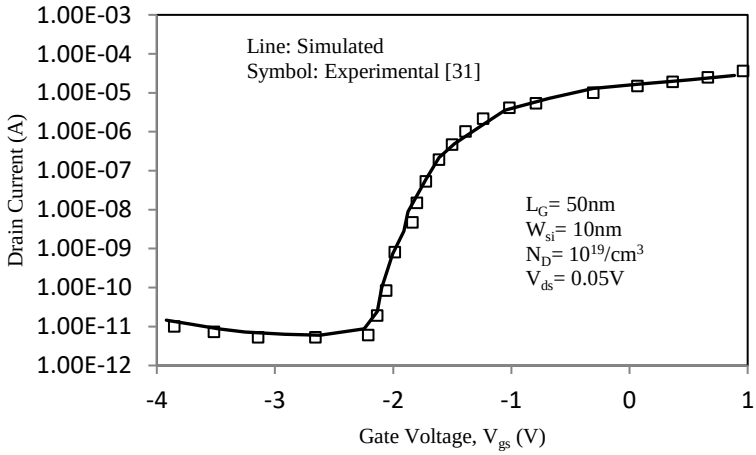


Figure 6.2 Calibration result.

6.3 Analytical Model

Considering the symmetry and the fully depleted silicon channel, potential distribution model has been developed for the device DM-JAM-CSG MOSFET to inspect it at the cryogenic temperatures by employing Poisson's equation in two-dimensions [32-34], given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z,T)}{\partial r}\right)+\frac{\partial^2 \psi_i(r,z,T)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}},\quad i=1,2 \tag{6.2}$$

where, $\psi_i(r,z)$ be the potential distribution, r and z be the respective lengths over horizontal and vertical axes, q be the charge of an electron, N_D is the doping concentration of the channel and ε_{si} is the permittivity of SiO_2.

For solving the above mentioned Poisson's equation, we have considered Parabolic Potential Approximation (PPA) assumption as the potential obtained inside the channel is of parabolic nature [35]. Now, applying the technique of PPA, the potential can be computed as:

$$\psi_i(r,z,T) = P_{i0}(z) + P_{i1}(z)\, r + P_{i2}(z)\, r^2, \quad 0 \leqslant z \leqslant L \tag{6.3}$$

Equation (6.3) is solved by considering the following boundary conditions:

(1) Center potential :

$$\psi_i(r=0,z,T) = \psi_c \tag{6.4}$$

(2) Field is zero at the center:

$$\frac{\partial \psi_i(r,z,T)}{\partial r}\Big|_{r=0} = 0 \tag{6.5}$$

(3) Surface potential:

$$\psi_i\left(r=\frac{t_{si}}{2},z,T\right) = \psi_s\left(\frac{t_{si}}{2},z,T\right) \tag{6.6}$$

(4) Electric field at the surface:

$$\frac{\partial \psi_i\left(\frac{t_{si}}{2},z,T\right)}{\partial r} = \frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs} - V_{fb} - \psi_i\left(\frac{t_{si}}{2},z,T\right)\right] \tag{6.7}$$

(5) Potential present towards source side:

$$\psi_1(r,0,T) = V_{bi} \tag{6.8}$$

(6) Potential present towards drain side:

$$\psi_2(r,L_2,T) = V_{bi} + V_{ds} \tag{6.9}$$

(7) Potential is continous at the interface of both the gates:

$$\psi_{s_1}(r,L_1,T) = \psi_{s_2}(r,L_1,T) \tag{6.10}$$

(8) Continuity of electric field at the interface:

$$\frac{\partial \psi_{s_1(r,L_1,T)}}{\partial r} = \frac{\partial \psi_{s_2(r,L_1,T)}}{\partial r} \tag{6.11}$$

where, capacitance per unit area, $C_{ox} = \frac{2\varepsilon_{ox}}{t_{si} \ln\left[1+\left(\frac{2t_{oxeff}}{t_{si}}\right)\right]}$ (6.12)

V_{bi} represents the built-in potential; t_{si} be the width of the silicon film and V_{ds} be the drain to source voltage.

On applying the above boundary conditions, the coefficients $P_{0i}(z)$, $P_{1i}(z)$ and $P_{2i}(z)(i = 0, 1, 2)$ we obtained are:

$$P_{10}(z) = \psi_{c_1}(z) \tag{6.12a}$$

$$P_{20}(z) = \psi_{c_2}(z) \tag{6.12b}$$

$$P_{11}(z) = 0 \tag{6.12c}$$

$$P_{21}(z) = 0 \tag{6.12d}$$

$$P_{12}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z, T)\right] \tag{6.12e}$$

$$P_{22}(z) = \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z, T)\right] \tag{6.12f}$$

Now, using the above coefficient values, the center potential specified by equation (6.3) is rewritten as:

$$\psi_1(r, z, T) = \psi_{c_1}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_1} - \psi_{si_1}(r = \frac{t_{si}}{2}, z, T)\right] \tag{6.13a}$$

$$\psi_2(r, z, T) = \psi_{c_2}(z) + r^2 \frac{C_{ox}}{\varepsilon_{si}.t_{si}}\left[\psi_{gs_2} - \psi_{si_2}(r = \frac{t_{si}}{2}, z, T)\right] \tag{6.13b}$$

where, ψ_{gs_1}, ψ_{gs_2} are the gate to source potentials across gate1 and gate2 respectively.

At $r = \frac{t_{si}}{2}$, $\psi_i\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{si_i}(r = \frac{t_{si}}{2}, z, T)$, equations (6.13a) and (6.13b) for ψ_{si_1} and ψ_{si_2} becomes:

$$\psi_{si_1}\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{c_1(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_1} - \psi_{si_1}(r=\frac{t_{si}}{2}, z, T)}{\varepsilon_{si} t_{si}}\right) \tag{6.14a}$$

$$\psi_{si_2}\left(r = \frac{t_{si}}{2}, z, T\right) = \psi_{c_2(z)} + \left(\frac{t_{si}}{2}\right)^2 C_{ox}\left(\frac{\psi_{gs_2} - \psi_{si_2}(r=\frac{t_{si}}{2}, z, T)}{\varepsilon_{si} t_{si}}\right) \tag{6.14b}$$

Rearranging the terms in (6.14a) and (6.14b) yields

$$\psi_{si_1}(r=\frac{t_{si}}{2},z,T)=\left[\frac{4\varepsilon_{si}\psi_{c_1(z)}+t_{si}C_{ox}\psi_{gs_1}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \tag{6.15a}$$

$$\psi_{si_2}(r=\frac{t_{si}}{2},z,T)=\left[\frac{4\varepsilon_{si}\psi_{c_2(z)}+t_{si}C_{ox}\psi_{gs_2}}{4\varepsilon_{si}+t_{si}C_{ox}}\right] \tag{6.15b}$$

The JLT works on bulk to source conduction mechanism, therefore, the center potential is to be calculated for $r = 0$. Center potential for two different metals is solved as:

$$\frac{\partial^2\psi_{c_1}(z)}{\partial z^2}=\frac{1}{\lambda^2}\left[\psi_{c_1(z)}-\eta_1\right], \qquad 0\leqslant z\leqslant L_1 \tag{6.16a}$$

$$\frac{\partial^2\psi_{c_2}(z)}{\partial z^2}=\frac{1}{\lambda^2}\left[\psi_{c_2(z)}-\eta_2\right], \qquad L_1\leqslant z\leqslant L_2 \tag{6.16b}$$

where, the characteristic length (λ), η_1 and η_2 are respectively given by

$$\frac{1}{\lambda^2}=\frac{16\,C_{ox}}{4\varepsilon_{si}t_{si}+{t_{si}}^2C_{ox}} \tag{6.17}$$

$$\eta_1=\psi_{gs_1}+\frac{qN_Dt_{si}}{4C_{ox}}+\frac{qN_D{t_{si}}^2}{16\varepsilon_{si}} \tag{6.18a}$$

$$\eta_2=\psi_{gs_2}+\frac{qN_Dt_{si}}{4C_{ox}}+\frac{qN_D{t_{si}}^2}{16\varepsilon_{si}} \tag{6.18b}$$

General solution of center potential, $\psi_{ci}(r,z,T)$ was obtained as:

$$\psi_{ci}(r,z,T)=\begin{cases}\psi_{c1}(r,z,T)\ \ for\ 0\leqslant z\leqslant L_1\\ \psi_{c2}(r,z,T) for\ L_1\leqslant z\leqslant L_2\end{cases} \tag{6.19}$$

$$\psi_{C1}(r,z,T)=A\,e^{z/\lambda}+Be^{-z/\lambda}+\eta_1 \tag{6.20a}$$

$$\psi_{C2}(r,z,T)=C\,e^{z/\lambda}+De^{-z/\lambda}+\eta_2 \tag{6.20b}$$

where, the coefficients *A*, *B*, *C* and *D* we obtained are given by,

$$A=\frac{e^{-L_1/\lambda}(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{-L_1/\lambda}-e^{L_1/\lambda})} \tag{6.21a}$$

$$B=\frac{e^{L_1/\lambda}(\phi_{bi}-\eta_1)-V_{DS}/2+\eta_1}{(e^{L_1/\lambda}-e^{-L_1/\lambda})} \tag{6.22b}$$

$$C=\frac{e^{-L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{-L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_1-L_2)/\lambda}-e^{(L_2-L_1)/\lambda}} \tag{6.23c}$$

$$D=\frac{e^{L_2/\lambda}\left(\frac{V_{DS}}{2}-\eta_2\right)-e^{L_1/\lambda}(\phi_{bi}+V_{DS}-\eta_2)}{e^{(L_2-L_1)/\lambda}-e^{(L_1-L_2)/\lambda}} \tag{6.24d}$$

Various device parameters get influenced due to the change in temperature [36]. At room temperature, doping concentration is presumed to be completely ionized, whereas at low temperature, partial ionization [37, 38] is there and is given by:

$$N_D^+ = \frac{N_D}{1+2\,exp\left(\frac{E_{fn}-E_D}{kT}\right)} \tag{6.25}$$

where, T be the temperature in Kelvin (K), E_D be the ionization energy of the donor dopant. The value of $(E_C - E_D)$ is equal to 0.054eV for Arsenic, 0.045eV for phosphor, 0.039eV for antimony and 0.045eV for Boron.

Subthreshold Current is also dependent upon temperature, given by:

$$I_{ds}(V_{gs}, V_{ds}, z) = \frac{\left[2\pi N_D \mu\left\{1-e^{\frac{-(qV_{ds})}{(k_B T}}\right\}\right]}{\int_0^{L_1+L_2} \frac{1}{\int_0^r r.e^{\left(\frac{q\psi(r,z}{k_B T}\right)dr}} dz} \tag{6.26}$$

Mobility component dependent upon temperature is expressed by Caughey and Thomas function [39], given as:

$$\mu_{Caug} = \mu_1 + \frac{\mu_2\left(\frac{T}{300}\right)^{\beta} - \mu_1}{1+\left(\frac{T}{300}\right)^{\gamma}\left(\frac{N_D}{N_{crit}}\right)^{\delta}} \tag{6.32}$$

where, μ_1= 55.24 cm^2/Vs, μ_2= 240 cm^2/Vs, β= -2.3, γ=- 3.8, N_{crit}= 1.072 x 10^{17} cm^{-3}.

Electron velocity [40] can be calculated using the equation:

$$v = \frac{\mu_n E_i(r,z)}{[1+(\mu_n E_i(r,z)/v_s)^n]^{1/n}} \tag{6.33}$$

where, μ_n is the low- field mobility, v_s is the saturation velocity and is equal to 1 x 10^7 cm/sec at room temperature for silicon, n= 2 for electrons and n= 1for holes in silicon.

Temperature dependent built- in voltage, V_{bi} is given by:

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_D^+}{N_D}\right) \tag{6.34}$$

where, k_B is the Boltzmann's constant.

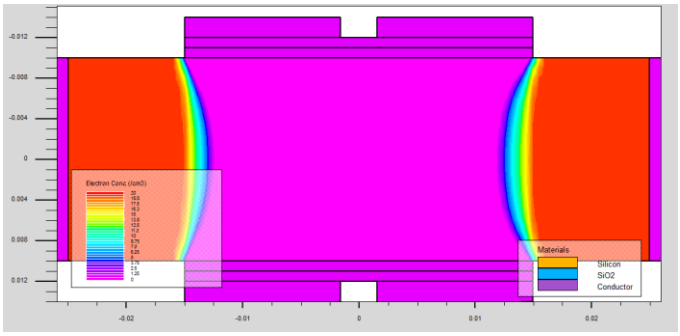
Transconductance (g_m) is given by:

$$g_m = \left(\partial I_{ds}/\partial V_{gs}\right)|_{V_{ds=constant}}$$

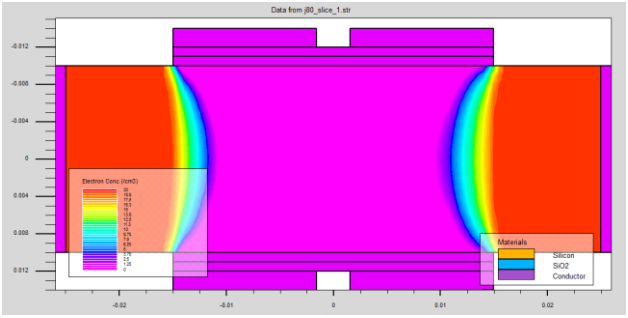
(6.35)

6.4 Results and Discussion

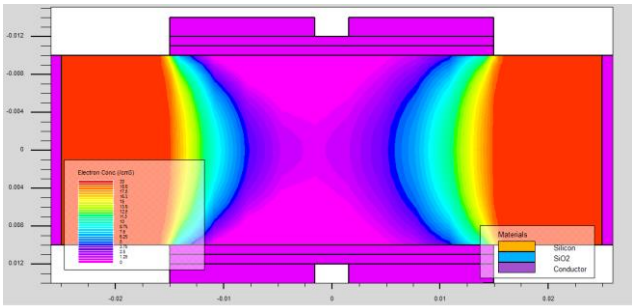
The electron concentration in a MOSFET is a critical parameter that determines the device's electrical characteristics. Temperature influences the electron concentration in the channel. Contour plots depicting the concentration of the electrons for DM-JAM-CSG MOSFET at *T*= 50K, 77K, 120K and 300K are depicted in Figures 6.3(a), (b), (c) and (d) respectively. The contour plots are obtained by taking a horizontal cut- line across the middle of the channel for V_{gs}= 1.0V and V_{ds}= 0.1V. It is perceived from these contour plots that as the temperature is increasing from 50K to 300K, the color of the channel in the contour plots is changing from pink to green, indicating that there is rise in the electron concentration in the considered device. The concentration of the electrons is observed to be very low at 50K and is increasing rapidly as the temperature is rising. This happens because the rise in temperature leads to the shifting of the Fermi level near the bandgap. Thus, resulting in the increase in the mobility of the carriers and bringing about increment in the electron concentration [41].



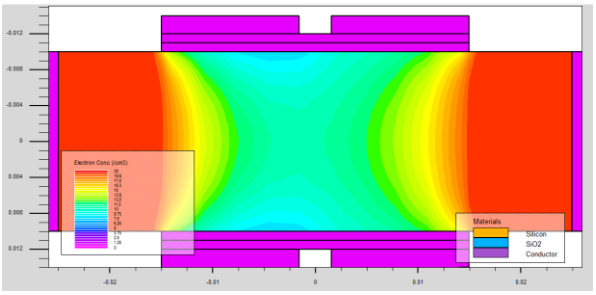
(a) T= 50K



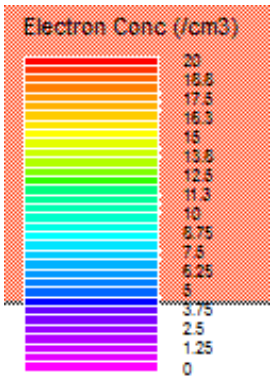
(b) T= 77K



(c) T= 120K



(d) T= 300K



(e) Color coding scale

Figure 6.3 Electron concentration contour plot for DM-JAM-CSG MOSFET at T= (a) 50K (b) 77K (c) 120K (d) 300K and (e) scale for the color coding.

The electron velocity in a MOSFET [42] is influenced by temperature due to its impact on various semiconductor properties. Electron velocity for DM-JAM-CSG MOSFET is depicted in Figure 6.4 (at T= 50K, 77K, 120K and 300K). When the temperature is lowered down, the velocity of the electron escalates. This is because the mobility of the electrons decreases with the decrease in the temperature. So, there is less number of collisions, bringing about increase in electron velocity. For T= 300K, electron velocity

is noticed to be 1.58E+07 cm/s and for T= 50K, it is equal to 1.96E+07 cm/s. Thus, the electron velocity is higher at lower temperature.

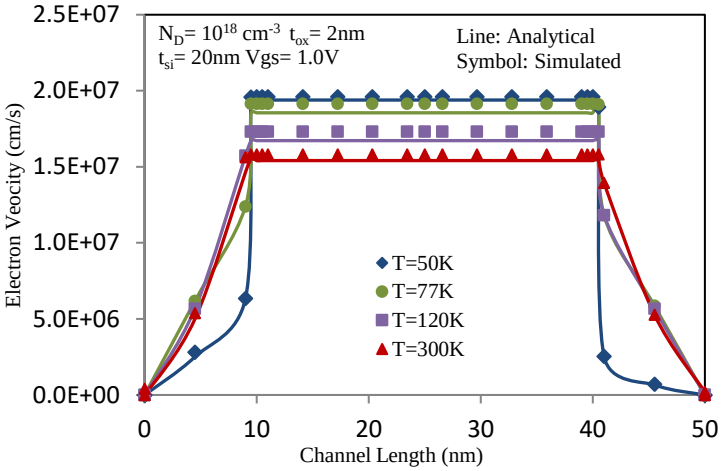


Figure 6.4 Electron velocity at T= 50K, 77K, 120K and 300K for DM-JAM-CSG MOSFET.

Figure 6.5 illustrates the center potential [43] across the channel length for distinct temperatures. It is perceived that with the decrease in temperature, the center potential is pulled up. This pull up is due to the decrease in the electron concentration at low temperature. But this pull up is so small, almost negligible; signifying the device potential does not have a considerable difference at cryogenic temperatures when compared with room temperature.

The MOSFET behaviour changes with temperature due to temperature-dependent parameters, such as threshold voltage, mobility, and other factors. The transfer characteristics for DM-JAM-CSG MOSFET is shown in Figure 6.6 for different temperatures at V_{ds}= 0.1V [44, 45]. From the figure, it is perceived that the drain current decreases with the decrease in temperature, due to the slower accumulation of the charge carriers at lower temperatures. This decrement in drain current is small in magnitude, i.e., at T= 300K, I_{ds}= 4.75 x 10^{-5}A and at T= 120K, I_{ds}= 3.88 x 10^{-5} A, thus, a decrease of 8.7 μA is observed when temperature is changing from room temperature (300K) to cryogenic (120K). So, at low temperature also, the characteristics of the device do not vary much. This small change in the drain current at 50K, 77K, and 120K indicates the usability of the device at cryogenic temperatures as well.

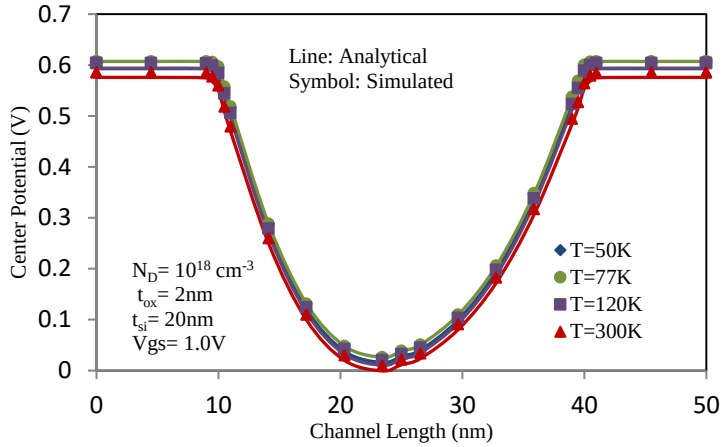


Figure 6.5 Center Potential variation at T= 50K, 77K, 120K and 300K for DM-JAM-CSG MOSFET.

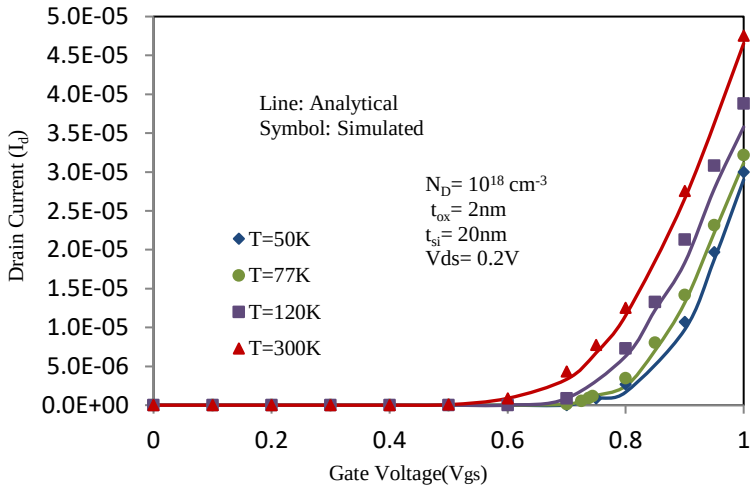


Figure 6.6 Transfer characteristics at T= 50K, 77K, 120K and 300K for DM-JAM-CSG MOSFET.

Output characteristics for DM-JAM-CSG MOSFET at *T*= 50K, 77K, 120K and 300K is displayed in Figure 6.7. From the figure, it is inferred that the output current remains almost same at cryogenic temperatures as well. At 120K, the output current is 4.02 x 10^{-} 5 A and at 300K, it is equal to 4.20 x 10^{-5} A, giving a difference of 1.8μA, which is not relevant much. Thus, concluding that the device at cryogenic temperatures gives almost similar output current as that at room temperature conditions.

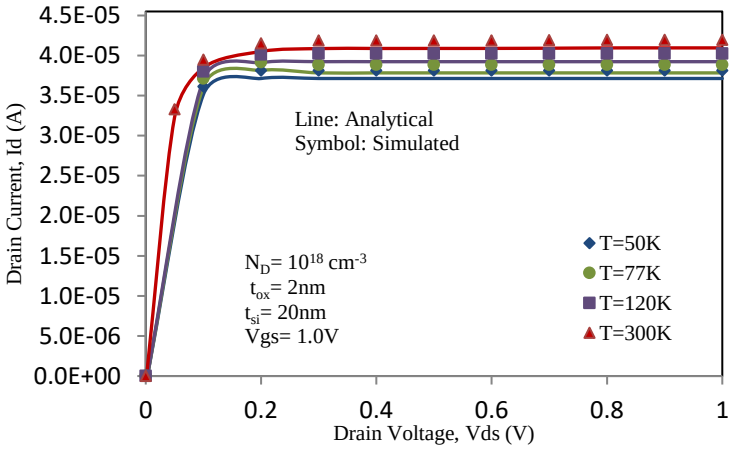


Figure 6.7 Output characteristics at T= 50K, 77K, 120K and 300K for DM-JAM-CSG MOSFET.

The transconductance (g_m) of a MOSFET [46], which represents the rate of change of drain current (I_{ds}) with respect to gate-to-source voltage (V_{gs}), is influenced by temperature. The key factor contributing to the temperature dependence of transconductance is the mobility of charge carriers. Figure 6.8 depicts the transconductance variation with respect to the gate to source voltage at room temperature and cryogenic temperatures at V_{ds}= 0.1V. As observed from the Figure 6.8, as the temperature is getting lowered down, the transconductance decreases. At T= 120K, it is equal to 1.95 x 10^{-4} S and at T= 300K, it is 2.20 x 10^{-4} S. So, a change of 0.25 x 10^{-4} S is observed in transconductance at these two temperatures. This difference is not substantial; denoting the device to work at cryogenic temperatures as well.

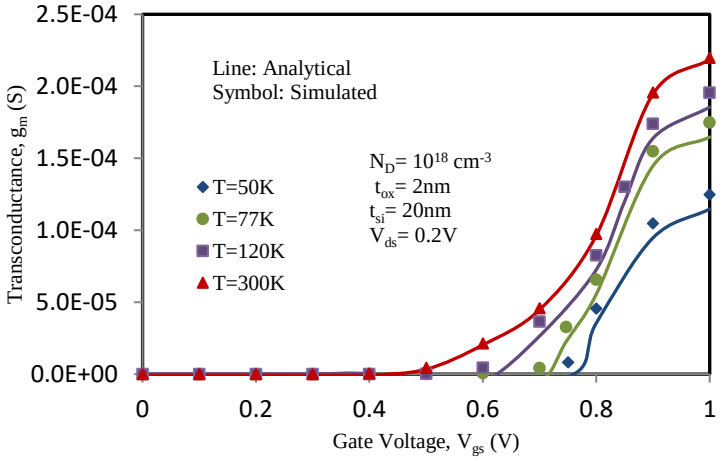


Figure 6.8 Transconductance (g_m) variation with V_{gs} at T= 50K, 77K, 120K and 300K for DM-JAM-CSG MOSFET.

The Subthreshold Slope (*SS*) of a MOSFET is a crucial parameter that characterizes the device's performance in the subthreshold region. The SS is related to the efficiency of turning the MOSFET on and off. Subthreshold slope (*SS*) [47] is defined as:

$$SS = 2.3\, V_{th} \left[\frac{d\psi(r,z)_{min}}{dV_{gs}}\right]^{-1} \tag{6.36}$$

where, V_{th} be the threshold voltage and $\psi(r,z)_{min}$be the minimal surface potential distribution. Figure 6.9 gives the SS for the device at several temperatures, *T*= 50K, 77K, 100K, 120K, 200K, 250K and 300K. It is noticed from Figure 6.9, that as the temperature is decreasing, *SS* is observed to become more robust. Such as, at *T*= 120K, it is 38 mV/decade and at *T*= 50K (at cryogenic temperature), it is equal to 18 mV/decade. Therefore, it can be inferred that at cryogenic temperatures, the subthreshold slope of the device becomes much more enhanced.

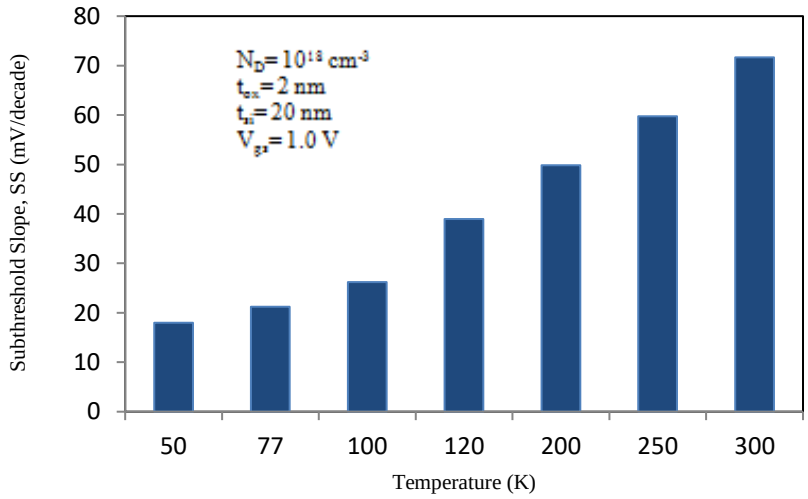


Figure 6.9 Subthreshold Slope for DM-JAM-CSG MOSFET at various Cryogenic temperatures.

Comparison of proposed device, DM-JAM-CSG MOSFET is performed with an analogous device, Junctionless Nanowire (JNT-NW) MOSFET [48] at cryogenic temperatures. Table 6.3 lists this comparison between the two devices, inferring that the drain current and peak transconductance, g_m are much more improved for DM-JAM-CSG MOSFET at cryogenic temperatures (*T*= 80K, 120K) as compared to JNT Nanowire MOSFET.

Table 6.3

Comparison of DM-JAM-CSG MOSFET with analogous device [48]

Parameter	**JNT-NW MOSFET [48]**	**DM-JAM-CSG MOSFET**	**JNT-NW MOSFET [48]**	**DM-JAM-CSG MOSFET**
	T= 80K		**T= 120K**	
Drain Current, I_d (µA)	1.75	33.0	1.90	38.8
Peak g_m (S)	1.85E-05	1.77E-04	1.35E-05	1.95E-04

The proposed device performance is also compared with another similar device, Junctionless (JNT) MOSFET [49] at T= 50K and 77K. Table 6.4 shows this contrast between the two devices on the basis of the various characteristics. From the table, it is observed that the drain current is much more enhanced for the presented device. Similarly, peak transconductance and subthreshold slope is also improved appreciably for the case of proposed device, DM-JAM-CSG MOSFET. Hence, it validates to exhibit more applicability under cryogenic temperature conditions.

Table 6.4

Comparison of DM-JAM-CSG MOSFET with another device [49]

Parameter	**JNT MOSFET [49]**	**DM-JAM-CSG MOSFET**	**JNT MOSFET [49]**	**DM-JAM-CSG MOSFET**
	T= 50K		**T= 77K**	
Drain Current, I_d (µA)	0.8	30.0	1.2	32.1
Peak g_m (S)	3.0E-08	1.25E-04	6.0E-08	1.75E-04
Subthreshold Slope (mV/dec)	25.7	18.0	54.1	21.2

6.5 Summary

MOSFETs are commonly used in electronic devices at room temperature, their behaviour changes significantly at extremely low temperatures. Using MOSFETs at

cryogenic temperatures, typically below -150 degrees Celsius, introduces several challenges and considerations. Using MOSFETs at cryogenic temperatures is a specialized application and is typically reserved for specific scientific and research purposes, such as experiments in quantum computing or astrophysics. Researchers and engineers working in these fields often need to address the unique challenges associated with cryogenic electronics and carefully design their circuits to operate effectively in extreme temperature conditions. Thus, in this chapter, analytical modeling has been performed to study the DM-JAM-CSG MOSFET under cryogenic temperature conditions. Various electrical characteristics regarding center potential, electric field, drain current, transconductance for the device has been attained at T= 50K, 77K, 120K and 300K and found to be almost same as that at room temperature. Also, subthreshold slope is much better at cryogenic temperatures. Thus, it can be concluded that low temperature does not vary the performance of the DM-JAM-CSG MOSFET by substantial amount. Thus, signifies its use for applications including space, terrestrial and satellite communication as well. Analytical and simulated results also agree well with each other.

6.6 References

[1] Gutierrez-D, E. A., Deen, J., & Claeys, C. (Eds.). (2000). *Low temperature electronics: physics, devices, circuits, and applications*. Elsevier.

[2] Ghibaudo, G., Aouad, M., Cassé, M., Martinie, S., Poiroux, T., & Balestra, F. (2020). On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature. *Solid-State Electronics*, *170*, 107820.

[3] Goryachev, M., Galliou, S., & Abbé, P. (2010). Cryogenic transistor measurement and modeling for engineering applications. *Cryogenics*, *50*(6-7), 381-389.

[4] Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability*, *4*(1), 99-109.

[5] D'Agostino, F., & Quercia, D. (2000). Short-channel effects in MOSFETs. *Introduction to VLSI design (EECS 467)*, *70*, 71-72.

[6] Xie, Q., Lee, C. J., Xu, J., Wann, C., Sun, J. Y. C., & Taur, Y. (2013). Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs. *IEEE Transactions on Electron Devices*, *60*(6), 1814-1819.

[7] Xie, Q., Wang, Z., & Taur, Y. (2017). Analysis of short-channel effects in junctionless DG MOSFETs. *IEEE Transactions on Electron Devices*, *64*(8), 3511-3514.

[8] Sarkar, A., Das, A. K., De, S., & Sarkar, C. K. (2012). Effect of gate engineering in double-gate MOSFETs for analog/RF applications. *Microelectronics Journal*, *43*(11), 873-882.

[9] Mohankumar, N., Syamal, B., & Sarkar, C. K. (2010). Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. *IEEE transactions on Electron Devices*, *57*(4), 820-826.

[10] Colinge, Jean Pierre. "Multi-gate soi mosfets." *Microelectronic Engineering* 84, no. 9-10 (2007): 2071-2076.

[11] Jazaeri, F., & Sallese, J. M. (2018). *Modeling nanowire and double-gate junctionless field-effect transistors*. Cambridge University Press.

[12] Li, C., Zhuang, Y., Di, S., & Han, R. (2013). Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs. *IEEE Transactions on Electron Devices*, *60*(11), 3655-3662.

[13] Colinge, J. P., Kranti, A., Yan, R., Lee, C. W., Ferain, I., Yu, R., ... & Razavi, P. (2011). Junctionless nanowire transistor (JNT): Properties and design guidelines. *Solid-State Electronics*, *65*, 33-37.

[14] Barbut, L., Jazaeri, F., Bouvet, D., & Sallese, J. M. (2013). Transient off-current in junctionless FETs. *IEEE transactions on electron devices*, *60*(6), 2080-2083.

[15] Jazaeri, F., Barbut, L., & Sallese, J. M. (2014). Generalized charge-based model of double-gate junctionless FETs, including inversion. *IEEE Transactions on Electron Devices*, *61*(10), 3553-3557.

[16] Kim, T. K., Kim, D. H., Yoon, Y. G., Moon, J. M., Hwang, B. W., Moon, D. I., ... & Lee, S. H. (2013). First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation. *IEEE electron device letters*, *34*(12), 1479-1481.

[17] Holtij, T., Graef, M., Hain, F. M., Kloes, A., & Iñíguez, B. (2013). Compact model for short-channel junctionless accumulation mode double gate MOSFETs. *IEEE Transactions on Electron Devices*, *61*(2), 288-299.

[18] Nigam, Kaushal, Pravin Kondekar, and Dheeraj Sharma. "High frequency performance of dual metal gate vertical tunnel field effect transistor based on work function engineering." *Micro & Nano Letters* 11, no. 6 (2016): 319-322.

[19] Sarkar, A., Das, A. K., De, S., & Sarkar, C. K. (2012). Effect of gate engineering in double-gate MOSFETs for analog/RF applications. *Microelectronics Journal*, *43*(11), 873-882.

[20] Srivastava, V. M., Yadav, K. S., & Singh, G. (2011). Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch. *Microelectronics Journal*, *42*(3), 527-534.

[21] Kasturi, P., Saxena, M., Gupta, M., & Gupta, R. S. (2007). Dual material double-layer gate stack SON MOSFET: A novel architecture for enhanced analog performance—Part I: Impact of gate metal workfunction engineering. *IEEE transactions on electron devices*, *55*(1), 372-381.

[22] Chau, R., Datta, S., Doczy, M., Doyle, B., Kavalieros, J., & Metz, M. (2004). High-/spl kappa//metal-gate stack and its MOSFET characteristics. *IEEE Electron Device Letters*, *25*(6), 408-410.

[23] Dhiman, G., Pourush, R., & Ghosh, P. K. (2018). Performance analysis of high-κ material gate stack based nanoscale junction less double gate MOSFET. *Materials Focus*, *7*(2), 259-267.

[24] Tayal, S., & Nandi, A. (2018). Study of temperature effect on junctionless Si nanotube FET concerning analog/RF performance. *Cryogenics*, *92*, 71-75.

[25] Oproglidis, T. A., Karatsori, T. A., Barraud, S., Ghibaudo, G., & Dimitriadis, C. A. (2018). Effect of temperature on the performance of triple-gate junctionless transistors. *IEEE Transactions on Electron Devices*, *65*(8), 3562-3566.

[26] Beckers, A., Jazaeri, F., & Enz, C. (2018). Cryogenic MOS transistor model. *IEEE Transactions on Electron Devices*, *65*(9), 3617-3625.

[27] Luo, C., Li, Z., Lu, T. T., Xu, J., & Guo, G. P. (2019). MOSFET characterization and modeling at cryogenic temperatures. *Cryogenics*, *98*, 12-17.

[28] Jazaeri, F., Beckers, A., Tajalli, A., & Sallese, J. M. (2019, June). A review on quantum computing: From qubits to front-end electronics and cryogenic MOSFET physics. In *2019 MIXDES-26th International Conference" Mixed Design of Integrated Circuits and Systems"* (pp. 15-25). IEEE.

[29] Balestra, F., & Ghibaudo, G. (2017). Physics and performance of nanoscale semiconductor devices at cryogenic temperatures. *Semiconductor Science and Technology*, *32*(2), 023002.

[30] ATLAS, D. S. (2015). Silvaco International. Santa Clara.

[31] Choi, S. J., Moon, D. I., Kim, S., Duarte, J. P., & Choi, Y. K. (2010). Sensitivity of threshold voltage to nanowire width variation in junctionless transistors. *IEEE Electron Device Letters*, *32*(2), 125-127.

[32] Roy, N. C., Gupta, A., & Rai, S. (2015). Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra low-power analog/RF circuits. *Microelectronics Journal*, *46*(10), 916-922.

[33] Holtij, T., Schwarz, M., Kloes, A., & Iniguez, B. (2013). Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region. *Solid-state electronics*, *90*, 107-115.

[34] Gautam, R., Saxena, M., Gupta, R. S., & Gupta, M. (2012). Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localised charges. *Journal of Computational and Theoretical Nanoscience*, *9*(4), 602-610.

[35] Pradhan, K. P., Kumar, M. R., Mohapatra, S. K., & Sahu, P. K. (2015). Analytical modeling of threshold voltage for Cylindrical Gate All Around (CGAA) MOSFET using center potential. *Ain Shams Engineering Journal*, *6*(4), 1171-1177.

[36] Lu, Juejing, Kai Sun, Hongfei Wu, Yang Xing, and Lipei Huang. "Modeling of SiC MOSFET with temperature dependent parameters and its applications." In *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 540-544. IEEE, 2013.

[37] Donato, N., & Udrea, F. (2018). Static and dynamic effects of the incomplete ionization in superjunction devices. *IEEE Transactions on Electron Devices*, *65*(10), 4469-4475.

[38] Trevisoli, R. D., Doria, R. T., de Souza, M., Ferain, I., Das, S., & Pavanello, M. A. (2012, October). The role of the incomplete ionization on the operation of Junctionless Nanowire Transistors. In *2012 IEEE International SOI Conference (SOI)* (pp. 1-2). IEEE.

[39] Gautam, R., Saxena, M., Gupta, R. S., & Gupta, M. (2014). Temperature dependent subthreshold model of long channel GAA MOSFET including localized charges to study variations in its temperature sensitivity. *Microelectronics Reliability*, *54*(1), 37-43.

[40] Roldan, J. B., Gamiz, F., Lopez-Villanueva, J. A., & Carceller, J. E. (1997). Modeling effects of electron-velocity overshoot in a MOSFET. *IEEE Transactions on Electron Devices*, *44*(5), 841-846.

[41] Hasanuzzaman, M., Islam, S. K., & Tolbert, L. M. (2004). Effects of temperature variation (300–600 K) in MOSFET modeling in 6H–silicon carbide. *Solid-State Electronics*, *48*(1), 125-132.

[42] Fischetti, M. V., Wang, L., Yu, B., Sachs, C., Asbeck, P. M., Taur, Y., & Rodwell, M. (2007, December). Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation. In *2007 IEEE International Electron Devices Meeting* (pp. 109-112). IEEE.

[43] Jazaeri, F., Barbut, L., Koukab, A., & Sallese, J. M. (2013). Analytical model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime. *Solid-State Electronics*, *82*, 103-110.

[44] Gnudi, A., Reggiani, S., Gnani, E., & Baccarani, G. (2012). Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs. *IEEE Electron Device Letters*, *33*(3), 336-338.

[45] Duarte, J. P., Choi, S. J., & Choi, Y. K. (2011). A full-range drain current model for double-gate junctionless transistors. *IEEE transactions on electron devices*, *58*(12), 4219-4225.

[46] Arora, N. D. (2012). *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media.

[47] Colinge, J. P. (1986). Subthreshold slope of thin-film SOI MOSFET's. *IEEE Electron Device Letters*, *7*(4), 24.

[48] Sasank, T. S., Ganesh, P. R., Kumar, N. P., Jena, B., & Obaid, A. J. (2021, May). Cryogenic analysis of junctionless nanowire MOSFET during underlap in lower technology nodes. In *Journal of Physics: Conference Series* (Vol. 1879, No. 3, p. 032124). IOP Publishing.

[49] Trevisoli, R., De Souza, M., Doria, R. T., Kilchtyska, V., Flandre, D., & Pavanello, M. A. (2016). Junctionless nanowire transistors operation at temperatures down to 4.2 K. *Semiconductor Science and Technology*, *31*(11), 114001.

CHAPTER 7

Conclusion and Future Scope of the Work

7.1 Conclusion

As already discussed in the previous chapters, as the scaling of the MOSFETs reaches the nanometer regime, Short- Channel Effects (SCEs) arises. This makes the conventional planar MOSFETs approach the near end of the technology road map. Therefore, in order to subside these effects, various devices with different geometries (Double- gate (DG) MOSFETs, Triple- gate MOSFET, Cylindrical Surrounding Gate (CSG) MOSFET) have been proposed and demonstrated. CSG MOSFET shows perfection with rampant scaling and increased short channel immunity under 22nm channel length. But for extremely scaled devices, Junctionless MOSFET and Junctionless Accumulation Mode (JAM) MOSFET were proposed which deal with the high parasitic resistance due to the development of extremely- sharp source- drain junctions. SCEs got lowered down to some extent in these topologies. In order to further minimize these SCEs, with the help of various Device Engineering techniques, we have proposed a new device structure in **Chapter 2.** Using Gate Metal Engineering and Gate Oxide Engineering, a novel structure named, Dual- Metal Gate Stack Engineered JAM-CSG (DMGSE-JAM-CSG) MOSFET was introduced. This structure possesses improved electrical characteristics such as high I_{on}/I_{off} ratio, low subthreshold slope, high transconductance and low output conductance than the previously introduced structures. Utilizing 2-D Poisson's equation in cylindrical co-ordinates, an analytical model of DMGSE-JAM-CSG MOSFET is also put forward for center potential, electric field, subthreshold current, transconductance and output conductance. The simulated results are compared with the analytical results and are found to be in good agreement. The proficiency of the device has also been examined by altering the gate stack materials and it is found that as the dielectric constant of the material increases, device performance upgrades. Thus, the overall performance of our proposed structure is much more dynamic as compared to the analogous devices. These enhanced properties make

this structure more pertinent for applications where high frequency and high amplification is significant.

Temperature is the prime factor which impacts the attributes of the MOSFET. The effect of temperature upon proposed structure is also studied in **Chapter 3** Dual- Metal Gate Stack (DMGS) JAM- CSG MOSFET. The device has been examined at various temperatures ranging from 100K to 500K. As the temperature is increasing an improvement is seen in all the parameters such as potential, electric field, electron velocity and electron concentration. A temperature-based analytical model has also been developed to inspect the model at various temperatures. It was observed that these analytical results agree well with the simulated ones. Further, to check the acceptability of the device for various RF applications i.e., wireless, radio networking, etc., Linearity of the device needs the investigated. Linearity characteristics are inspected by estimating numerous Figure of Merits (FOMs) including VIP2, VIP3, IIP3, IMD3 and higher order transconductances. FOMs for DMGS-JAM-CSG MOSFET are found to be improved and higher order harmonics are also reduced in compared to the other analogous devices. Thereby, making the proposed device DMGS-JAM-CSG MOSFET is found to be more immune towards distortion and also relevant for RFIC applications.

In **Chapter 4** a biosensor based JAM- CSG MOSFET to perform label- free detection of the biomolecules (for example, DNA, biotin, protein, etc.) is proposed. The impact of both the neutral and charged biomolecules upon the device has been inspected in this chapter. Additionally, analytical model for this device has been introduced employing the Poisson's equation within the boundary conditions and the results obtained are corresponding well with the simulated results. The sensitivity criterion considered in our study for detecting the biomolecules is the threshold voltage change. The sensitivity parameter and various other electrical characteristics of the biosensor have been explored and explained comprehensively in this chapter. A prominent change is noticed in the threshold voltage of proposed device for both the neutral and charged biomolecules. Thus, JAM- CSG MOSFET based biosensor as desired for detecting the biomolecules with appreciable sensitivity and hence confirms its relevancy to work as a biosensor.

All the stated devices in the literature survey have considered channel to be uniformly doped. As, it is fairly difficult to attain uniform doping in the course of the fabrication process, therefore, a Dual-Metal Gate All Around Junctionless Accumulation- Mode Nanowire FET (DMGAA-JAM-NWFET) possessing a horizontal-like non-uniform doping profile is put forward in **Chapter 5**. An analytical model of the proposed structure has also been presented to obtain the 2-D electrostatic potential distribution. This is evaluated using Poisson's equation under the pertinent boundary conditions. Both the analytical and simulated results were contrasted and found to be in good agreement. Furthermore, the effect of straggle length parameter and the peak doping concentration upon the device behaviour is inspected. The non-uniformly doped DMGAA-JAM-NWFET is also compared with the uniformly doped DMGAA-JAM-NWFET and we observe finer electrical characteristics for non-uniformly doped device i.e., improved I_{on}/I_{off} ratio, peak g_m, subthreshold slope. Thus, we can conclude that the non-uniformly doped DMGAA-JAM-NWFET is appreciably more favourable where upgraded frequency and switching speed is a requirement.

The device manifests efficacious aspects at room temperature. Further study is required to monitor device performance at other temperature conditions as well. So, investigation is needed to check its behavior at higher and lower temperature conditions. Analysis of a device at very low temperature is termed as Cryogenic analysis. An analytical model to analyze the DM-JAM-CSG MOSFET under cryogenic temperature conditions is presented in **Chapter 6**. Various electrical characteristics concerning center potential, electric field, drain current, transconductance are acquired at several low temperature conditions (T= 50K, 77K, 120K and 300K) and it was perceived that the characteristics are almost similar as that at room temperature. Consequently, it can be inferred that the DM-JAM-CSG MOSFET performs well at low temperatures. Therefore, declaring its utility for space, terrestrial and satellite communication.

7.2 Future Scope of the Work

With the scaling of the MOSFET device in nanometer regime, Short- Channel Effects (SCEs) and Hot Carrier Effects (HCEs) show presence. The main aim of this thesis is to improve the performance of the devices utilizing various Device Engineering Mechanisms. and For this we have proposed various devices using Gate Metal

Engineering and Gate Oxide Engineering.The research work performed proved that the proposed structure is more immune towards SCEs and HCEs. Objective of the thesis have been fulfilled through analytical formulations and extensive simulations. However, certain aspects related to performance improvement can be done. There is always scope of improvement in performane of the existing devices. The candidate has identified the following problems that may be looked into the future.

1. Further compact modeling of the Dual- Metal Gate Stack Engineered Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSE-JAM-CSG) MOSFET with detailed analysis of all the electrical characteristics of the MOSFET can be performed.
2. Noise Analysis of Dual- Metal Gate Stack Engineered Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSE-JAM-CSG) MOSFET also needs to be done by evolving its noise model.
3. Designing of different circuits using Dual- Metal Gate Stack Engineered Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSE-JAM-CSG) MOSFET can be taken up for future investigation for low power and RF applications.
4. A Junctionless Accumulation-Mode Cylindrical Surrounding Gate (JAM-CSG) MOSFET as a Biosensor has been developed in this work. This device can be further inspected for different sensor applications also.