LOW POWER, DUAL MODE OPERATIONAL 7T SRAM BIT CELL AND SENSE AMPLIFIER FOR PERFORMANCE ENHANCEMENT

A Thesis Submitted

In Partial Fulfillment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

by

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CERTIFICATE

Certified that **Bhawna Rawat** **(2K19/PHDEC/501**) has carried out their search work presented in this thesis entitled **"Low Power, Dual Mode Operational 7T SRAM Bit Cell and Sense Amplifier for Performance Enhancement"** for the award of **Doctor of Philosophy** from Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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CANDIDATE'S DECLARATION

I, **Bhawna Rawat** (**Roll No. 2K19/PHDEC/501)** student of Ph.D., hereby declare that the Dissertation titled "**Low Power, Dual Mode Operational 7T SRAM Bit Cell and Sense Amplifier for Performance Enhancement**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of **Doctor of Philosophy**, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: DTU, Delhi **BHAWNA RAWAT**

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ABSTRACT

Cache memory is a key component for most microprocessors in embedded system. The increasing processing load has resulted in an upsurge in the demand for low power, high performance SRAM bit cells. The memory is formed by an array of bit cells for data storage, and its peripheral circuits. The peripheral circuit comprises of SA, row-column decoders, write drivers, and pre-charge circuitry. The 6T bit cell was the industry standard, but with decreasing technology node and V_{DD} scaling the performance for the 6T cell is deteriorating. This has motivated researchers to design other bit cells. Altering the bit cell design mandates re-designing the sense amplifier topology as well to make it compatible with the modified cell design.

In keeping with the same, four designs (7TP1, 7TP2, 7TP3, and 7TP4) of single ended, single port 7T bit cells are proposed. The cells differ from each other in terms of the number of multi-threshold devices and the read port topology adopted by the cell. The performance of the proposed of the four proposed cells is compared to identify the best design topology. Based on the comparison the 7TP3 cell is identified as the best topology amongst the four designs. Its HSNM and RSNM are high at 90 mV; the WM value is slightly high. While, the write time is considerably low at 10 ns. Additionally, its area is also towards the lower end in comparison to others and the design is also nearly square. Thus, 7TP3 cell design is accepted as the best design topology amongst the four proposed 7T bit cells. All the cells are designed at 32 nm technology node and simulated for 300 mV supply voltage.

Thereafter, the performance of the proposed 7TP3 bit cell is compared against pre-exiting bit cells to validate its performance. The major highlights for the 7TP3 cell are - its read port which is designed to exclude the data node from read discharge current path and it use of a high performance transistor to improve write ability for the cell. Collectively, they help improve the read and write stability for the cell. The hold, read, and write noise margin for the cell are 90, 90, and 180 mV respectively for supply voltage of 300 mV. It requires a 10 ns pulse-width to perform a successful write operation.

The robustness of 7TP3 cell is analyzed using its resilience to global variation analysis and temperature variation anlsyis. For the Monte Carlo analysis 6σ variation around the mean threshold value are taken for performance analysis, whereas for temperature variation

analysis the environment temperature for the simulation is varied from -10 ºC to 80 ºC. When subjected to global variations, the cell maintains read as well as hold SNM of 75 mV, while the WM is 215 mV. While for temperature variation analysis, the HSNM and RSNM are reduced by 0.1 mV/ºC and the WM changes 0.2 mV/ºC. This validates the performance of the proposed 7TP3 cell against both global and temperature variation analysis. This helps validate the reliability of the cell.

The performance for the 7TP3 cell is compared against other 5T, 6T, 7T, 8T, 9T, 10T cells and is found to be superior. Its leakage current is low, while the ON current is high. Thereby, resulting in high current ratio value of 783 for the cell in comparison to its other pre-existing bit cells in comparison. The power consumption of the proposed bit cell is also found to minimal for all modes of operation. The standby power of the cell is calculated to be 8.4 and 1.05 pW for Q = '0' and '1', respectively. Moreover, the improvement in the performance is obtained for area as low as 0.539 μm^2. The area of 5T, 6T, 7T-1, 7T-2, 7T-4, 7T-5, 8T, 9T and 10T cell is greater than 7TP3 bit cell area by 22.17 %, 51.8 %, 35.8 %, 13.9 %, 30.4 %, 6.78%, 56.6 %, 63.3 % and 75.5 %.

The design for the proposed single ended, single port 7T cells can operate only in this configuration. But, the growing popularity of hyper-personalized devices and round the clock connectivity has generated the need for a bit cell that can switch between low power and high speed operation. Thus, concept for a dual mode operational bit cell is proposed. The concept for the proposed dual mode operation cell describes a bit cell that has the capability to operate in two different design configurations. The selection of mode of configuration for the cell is dependent on the control signals for the cells. The control signals of the cell can steer into from one configuration into the other. To design the dual mode operational bit cell, one mode of operation is the single ended, single port mode of the 7TP3. To determine the second mode of operation for the cell, another 7T cell with single ended, dual port configuration is proposed.

Thus, a single ended, dual port 7T cell is also proposed. The memory core and write port for the proposed dual port cell is similar the memory core and write port for the single ended, single port 7TP3 cell proposed in. The difference between the two topologies lie in their respective read port design. The read port and write port for 7TP3 are connected to a common bitline. Whereas, the read and write port for the dual port 7T cell are isolated and

do not share a common bitline for operation. The cell is designed at 32 nm and its performance is compared against other pre-existing 7T bit cells. The cell is simulated for 800 mV as, various pre-existing bit cells performed reliability at this voltage.

The stability analysis for the hold, read, and write operation for the proposed dual port 7T cell yields the noise margin for the three operations as 324, 324, and 488 mV, respectively. For a successful read and write operation pulse-width of 5 ps and 0.14 ns respectively are required. Temperature variation analysis yields 0.15, 0.15, and 0.24 mV/ºC variation in hold, read, and write noise margin values, respectively. The leakage power consumption for the cell is 256 pW, while the read, and write power consumption for the cell are 6 µW and 1.9 µW, respectively. All the aforementioned merits for the proposed dual port 7T cell are achieved with a minimal layout area of 0.553 μm^2.

Once the design for the single ended, single port 7T cell and the single ended, dual port 7T cell is finalized, the dual mode operational cell is designed. The dual mode operational cell is a versatile amalgamation of the aforementioned two cells with the capability to function in two different single ended configurations – single port and dual port. The bit cell is composed of eight transistors and is grouped into three sub-parts – single bit memory core, reading port and writing port. The single bit memory core of the reconfigurable memory is the part that stores the desired information. The read and the write port are the access circuitry that enable the device to read and write into the cell, respectively. The single port cell is more suitable for low power applications and the dual port cell is better for high speed operation. Therefore, as per the requirement of the circuit at a given instant, the different configurations for the cell may be used.

All the proposed cells are of single ended nature owing to their better performance at lower supply voltage and high area density. This growing demand for single ended cells has also generated the need for a single ended sense amplifier topology that is compatible with the array of single ended cell. Conventionally, sense amplifiers were designed with differential ended topology. This SA topology is usually voltage based in nature owing to their low area footprint and low operational V_{DD}. But delay and current for current mode topology are higher. Thus, generating need for a single ended SA that has low power consumption, smaller area footprint, and faster operation. The convenient sensing topology deemed reliable for single ended SRAM is inverter based.

Thus, a single ended switching NMOS based sense amplifier is proposed for 32 nm technology node. It operates in two phases – the pre-charge phase and the evaluation phase. This two-phase functioning for the proposed sense amplifier ensures there is minimal power consumption for the topology when the memory is not executing the read operation. Its pulse-width requirement of 0.32 ns is significantly lower in comparison to its counterparts. While its leakage power is least amongst the different SA topologies at 4 nW. The additional advantage the proposed SA has its lower area footprint of 7.65 μm^2.

A bit cell is a small peg in a wide m×n matrix that forms the memory core for data storage. Conventionally, a bit cell is replicated to create the entire array. But, in a typical multimedia application the lower order bits may be more vulnerable to noise than higher order bits. Hence, appreciable performance and minimal image quality degradation can be achieved by using two different bit cells for array formation.

A hybrid array configuration using two different 7T bit cells topologies is proposed. The best results are obtained when six dual port and ten single port cells are used to design the array. The static and dynamic power values obtained for the design are 0.29 µW and 23 µW, respectively. These values are 3.5% and 20.7% lower than the static and dynamic power values obtained for memory array designed using only dual port cells. Also, the error tolerance for this partition is approximately 0.015, which is fairly low, making this hybrid array design low power and error resistant.

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude and sincere appreciation to all those who have contributed in the completion of my doctoral thesis. Their guidance, support, and encouragement have been invaluable throughout this journey.

First and foremost, I am immensely grateful to my supervisor, Prof. Poornima Mittal, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India. I am greatly thankful for her unwavering commitment, patience, and expertise. Ma'am's guidance and insightful feedback have been instrumental in shaping the direction of my research and enhancing the quality of my work. I am truly fortunate to have had such a dedicated mentor who consistently challenged and inspired me to reach new heights.

I express my gratitude towards the distinguished faculty members who have time and again helped us at different avenues. I extend my sincere regards to HoD sir, for his constant support. I wish to express my gratitude towards the DRC chairperson, the distinguished DRC members. Their expertise, constructive criticism, and valuable suggestions have significantly contributed to the refinement of my thesis. I am deeply grateful for the time and effort they invested in reviewing and evaluating my work.

I am indebted to the esteemed faculty members of Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, who provided me with a rich academic environment and facilitated my intellectual growth. Their lectures, seminars, and discussions have expanded my horizons and shaped my research interests.

I express my deepest regards for Prof. Brijesh Kumar, Department of Information Technology, Indira Gandhi Delhi Technical University, Delhi, India, for investing his valuable time and efforts for providing deep and insightful remarks.

I am also grateful to all my colleagues and seniors of the Electronics and Communication department, especially Mr. Sachin Tyagi, Mr. Mohit Tyagi, Mr. Paritosh Chamola, Mr. Ashish Raturi, Ms. Sugandha, Ms. Yogita Chopra, Mr. Ayush, and Ms. Bharti. I am thankful

to them as they have generously contributed their time and shared their insights, without whom my study would not have been possible. Their willingness to participate and engage in meaningful discussions enriched my research and provided me with valuable data. I also express my thanks all the staff members of the department for their continuous support in our academic activities.

Lastly, I would like to thank my family for their kindness, support, and patience thought my journey. Their belief in me has kept my spirits and motivation high during this process. Their understanding, love, and encouragement have been a constant source of motivation, and I am truly grateful for their presence in my life.

Finally, I would like to acknowledge the financial support provided by Delhi Technological University, Delhi. Their assistance enabled me to carry out my research effectively and ensured that I had the necessary resources to complete my thesis.

To all those who have directly or indirectly contributed to my doctoral thesis, I extend my deepest gratitude. Your support, whether big or small, has played a significant role in shaping my academic and personal growth. I am profoundly grateful for your presence in my life and for the impact you have had on my journey as a researcher.

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List of Symbols and Abbreviations

Symbol/Abbreviation	Full Form
ACSS	AC Coupled Sensing Scheme
BCC	Butterfly Curve Collapse
BER	Bit Error Rate
BI	Bit Interleaving
BL	Bitline
BLB	Bitline Bar
BTI	Bias Temperature Instability
C_{BL}	Bitline Capacitance
C_L	Load Capacitance
C_{OX}	Oxide Capacitance
C_{RBL}	Read Bitline Capacitance
C_{RL}	Readline Capacitance
C_{WBL}	Write Bitline Capacitance
C_{WL}	Wordline Capacitance
C_{WLB}	Wordline Bar Capacitance
DP	Dual Pulse
f_{clk}	Clock Frequency
FF	Fast, Fast
FS	Fast, Slow
GBL	Global Bitline
HS	Half Select
HSD	Half Select Disturbance
HSNM	Hold Static Noise Margin
HV_{TH}	High Threshold Voltage
I_{D_l}	Leakage Current for Dual Port 7T Cell
IoT	Internet of Things
I_{S_l}	Leakage Current for Single Port 7T Cell
j	Number of Rows
k	Number of Columns

kT	Thermal Noise = 26 mV
L	Length
LBL	Local Bitline
LSB	Least Significant Bit
LV_{TH}	Low Threshold Voltage
MC	Monte Carlo
MSB	Most Significant Bit
n	Partition for the Array
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
P_{D_Hold}	Hold Power for Proposed Dual Port 7T Cell
P_{D_Read}	Read Power for Proposed Dual Port 7T Cell
P_{D_Write}	Write Power for Proposed Dual Port 7T Cell
P_{Read}	Read Probability
P_{S_Hold}	Hold Power for Proposed Single Port 7T Cell
P_{S_Read}	Read Power for Proposed Single Port 7T Cell
P_{S_Write}	Write Power for Proposed Single Port 7T Cell
P_T	Total Power Consumption for Hybrid Array
P_{TD}	Total Power for Array formed by Dual Port Cells
P_{Ts}	Total Power for Array formed by Single Port Cells
P_{Write}	Write Probability
PVT	Process, Voltage, and Temperature
Q	Data Node
QB	Data Node Bar
RBL	Read Bitline
RBL1	Read Bitline 1
RBL2	Read Bitline 2
RL	Readline
RP1	Read Port 1
RP2	Read Port 2
RSNM	Read Static Noise Margin
SA	Sense Amplifier
SD	Standard Deviation

SNM	Static Noise Margin
SNSS	Switching NMOS Sensing Scheme
SoC	System on Chip
SPSS	Switching PMOS Sensing Scheme
SRAM	Static Random Access Memory
SF	Slow, Fast
SS	Slow, Slow
ST	Schmitt Trigger
T	Clock Pulsewidth
T_{crit}	Write Pulse Width
TG	Transmission Gate
T_S	Read Time
V_{DD}	Supply Voltage
V_{OH}	High Level of Output Voltage
V_{OL}	Low Level of Output Voltage
V_{TH}	Threshold Voltage
W	Width
WBL	Write Bitline
WL	Wordline
WLB	Wordline Bar
WM	Write Margin
WWL	Write Wordline
WWLB	Write Wordline Bar
α	Activity Factor
ϕ	Enable signal
μ_m	Mean
μ_n	Mobility of Electrons
6σ	Six Sigma Standard Deviation

CHAPTER – 1

INTRODUCTION

The growing depends of the civilization on digital devices has opened up a new world of processing and data. This plethora of data and its processing is dependent on various types of powerful digital devices. These devices comprise of a microprocessor or a group of microprocessors. An essential component of these microprocessors is the cache memory circuit that enables its fast operation. In this chapter, a detailed introduction to the cache memory and its building blocks are presented. It is essential to understand the different components of cache so as identify the different aspects that can be worked upon to improve its performance.

This chapter is divided into six different sections, including introduction, section 1.1. It is followed by section 1.2, which is dedicated to the essential components that together comprise the SRAM. Based on the brief introduction of the different components of SRAM, the identified problem statement is described in section 1.3. Thereafter in section 1.4, objectives are formulated to rectify the identified problems. The methodology used to achieve each desired objective is explained in section 1.5. Finally in section 1.6, the thesis organization is summarized.

1.1 INTRODUCTION

The electronics industry is progressing towards artificial intelligence and internet of things due to the increased popularity of hyper-personalized system on chip (SoC) devices. Also, the increase in demand for round the clock digital connectivity, and the explosion of everyday personal data has increased the processing demand for embedded systems. A mandatory element for most SoC devices is an on-die embedded cache memory, also referred to as the static random access memory (SRAM). These memories occupy more than 90% of the die surface [1] and thereby dominate power consumption and area footprint of SoC [2]. With the increasing demand for light weight portable devices with longer battery life it has become essential to identify techniques that will help in improving performance for the SoC. As highlighted previously, that area, and power consumption for SRAM makes

up for most of the total proportion. It is mandatory to uplift the performance of the memory while simultaneously lowering its area footprint.

Conventionally the data core for SRAM is formed by bit cells organized in an array. These bit cells store data in forms of single bit value, whereas the task of reading and writing into the cell is facilitated by peripheral circuitry formed by row-column decoders, bit-lines, pre-charge circuitry and sense amplifier (SA). In its most crude form, memory core along with the peripheral circuit consumes about 30% of the total power for the system and 50% chip area [3-4]. The total power consumption for an SRAM circuit can be divided into two distinct components – static power consumption and dynamic power consumption. Static power has a linear dependence on supply voltage (V_{DD}), whereas the latter has a quadratic dependence on V_{DD} [5].

The most trivial method for lower power consumption is to lower its operational V_{DD} [6]. But this is limited by process, voltage, and temperature (PVT) variations in the nanometer vicinity [7]. In keeping with the Moore's Law, the technology node for circuit design has scaled drastically. This when coupled with V_{DD} lowering for power consumption reduction makes the circuit highly susceptible to variations, errors, and other vulnerabilities. Another pitfall of the declining trends for V_{DD} is that, the static power for the circuit starts dominating the dynamic power component [8]. This is further augment by increased leakage current values for lower technology node that further adds to the static power consumption factor.

Another major limitation that restricts reduction of V_{DD} for a digital circuit is that it also limits its operational speed [9]. Thereby diminishing the operational frequency for memory [10]. Thus, if the operational frequency for the circuit is lowered, its clock pulse width is widened. This increase in operational time for the circuit increases the power consumption for each operation, even though the total power consumed by the cell decreases [11]. Consequently, resulting in high power consumption for the SRAM, which in turn lowers the battery life for the portable SoC. Thus, it may be inferred that designing a bit cell operational at low levels of V_{DD} is a mammoth task for designers [12].

Another aspect that limits the performance of SRAM is the slow-fast corner. In general, if NMOS and PMOS transistor are equally sized, the performance for the CMOS circuit is skewed. This is caused by the vast gap between the mobility of charge carries for the NMOS and PMOS transistors. This gap between the charge carriers mobility gets extenuated

because of the skewed corner. At this corner, even if the V_{DD} for the circuit is maintained in the super-threshold region the performance of the circuit suffers drastically. Then, for low levels of V_{DD} the impact on cell performance at the skewed corner are highly unreliable.

Besides, apart from V_{DD}, another factor that highly influence error propensity of SRAM is its total area footprint. Memories with larger area footprint are more prone to reliability issues and failure events [13]. The collective influence of these aforementioned factors increases vulnerability [14] of memory towards read, write, and access time failures. Thus, if the performance of the memory is to be improved, it is essential to modify cell design, along with SA and their array configuration. In keeping with the same, cell and its peripheral circuit are the main focus of this thesis. In this chapter, the SRAM design and its essential circuit components are briefly introduced to highlight the key theme pursued in this thesis.

1.2 SRAM AND ITS COMPONENTS

The increase in demand for round the clock digital connectivity, and the explosion of personal data has increased the processing loas for embedded systems. A major component of efficient embedded system is SRAM; formed by bit cells organized in an array and its peripheral circuitry. Bit cell stores data, whereas read and write operation for the cell are facilitated by its peripheral circuitry; composed of decoders, bitlines, pre-charge circuit, and SAs [15]. A block diagram to represent the SRAM memory is depicted in Fig. 1.1.

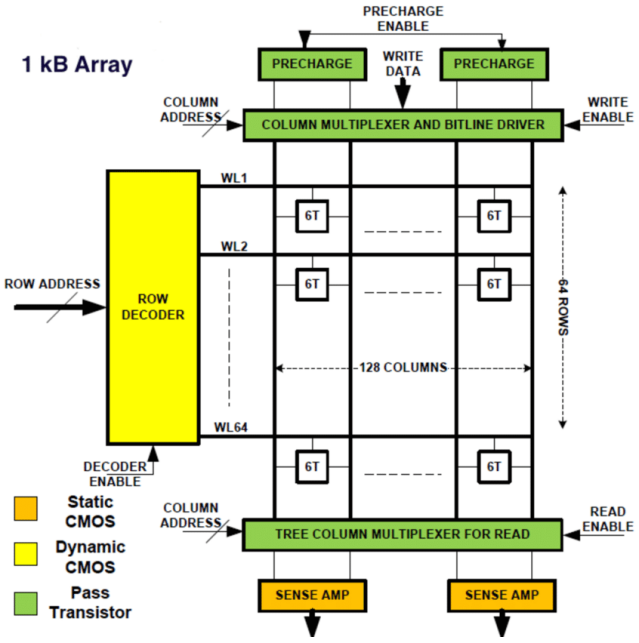


Fig. 1.1 Block diagram for SRAM based memory

The pre-charge circuit charges the bitlines to high or low potential as per the need of the cell, during the read and hold operation. The read operation in general requires both the bitline to have the same potential. Whereas the write operation deems it necessary to have alternating data on the bitlines. Therefore, during the write operation the bitlines are controlled by the write driver circuit and not the pre-charge circuit.

The row and column based decoders are utilized to identify the exact cell in which read or write operation is to be performed. They are highly useful circuits when creating large memories. Another peripheral circuit that is highly important is the SA. This circuit enables a fast read operation for the memory. The SA is a circuit that senses a small differential voltage that develops on the bitlines to amplify it, to yield correct output for the read operation. It also helps reduce the read access time for the memory.

1.2.1 SRAM Bit Cell

The bit cell is the heart for SRAM circuit. It is the singular unit in which information is stored in the form of a bit. A bit cell can store a single bit of data, and the same bit cell is replicated to create the array for the SRAM. Conventionally, the bit cell design comprised of six transistors (6T), with two complementary bitlines that were common for the read as well as the write operation. But, the performance for bit cell has suffered drastically due to technology node scaling and V_{DD} reduction. The 6T cell is unable to perform for lower technology node due to the inherent read-write conflict. Other 6T cells designed to eliminate the inherent read-write conflict resulted in high power requirement, thereby making it unfit for low power application. The most trivial method to eliminate the inherent read-write conflict for a cell is to isolate its read and write port. Thus, based on the port configuration a bit cell can be categorized as single port or dual port cell.

A. Single Port Cells

A bit cell relies on either a pair of bitlines or a single bitline for its operation. If the cell utilizes the same bitline pair or bitline for both read as well as the write operation, the cell is referred to as a single port cell. Conventionally cells are single port in nature, but this results in the inherent read-write conflict. This results in a trade-off between the read and write performance for the bit cell. The improvement in one come at the cost of the other. A major advantage for having a single port cell is that it reduces the power consumption, and

capacitance for the cell, as common signals are used for controlling the different operations.

At higher technology node, the vulnerabilities due to the read-write conflict were not that significant and did not possess any threat to the circuit. But with the decrease in technology node, lowering of V_{DD} and minimal sizing of transistor for high area density, the impact of this conflict is becoming apparent. It limits the designing of the bit cell and also dramatically impacts the performance of the bit cell. Thus, isolating the read and write port is the only alternative at the disposal of memory designers.

B. Dual Port Cells

When a bit cell is designed to have separate ports for read and write operation it is referred to as a dual port cell. The scaling technology node and lowering trends of V_{DD} have resulted in this being a preferred configuration for a bit cell. This configuration is very efficient in eliminating the contradictory sizing requirements for the read and write operation. It makes the cell more stable, increases the speed of operation, and lately is a preferred choice for cell designing for low transistor count cells.

But, the isolation of ports for the cell mandates the use of different control signals to steer the cell into different operations (hold, read and write). Increase in signals implies increase in capacitance for the cell. This also mandates designing additional circuitry to control these signals. Thereby poorly impacting the power consumption and area footprint for the cell.

1.2.2 Sense Amplifier

Additional to the bit cell, a cache memory also comprises of peripheral circuitry. Amongst the different peripheral units, the SA is the most crucial component as the read operation for the cache depends on it. In the array arrangement of the cache, each column culminates in an SA (as illustrated in Fig. 1.1). Conventionally, SA detects a small differential voltage on the bitline, to produce a full swing data output [16-17]. Therefore, it is highly critical for performance of cache memory. It helps in determining the operational frequency, power consumption, and minimum operating point, for cache memory [18-19].

Various SA designs have been reported in literature by researchers. These different SA topologies reported in literature can be categorized into either voltage mode or current mode. The latter is quickly able to amplify a small differential signal at the bitlines to a full swing

voltage output [20-21]. But its higher transistor count and larger area occupancy makes it economically unfeasible. An area efficient SA topology is the latch based voltage mode SA. They are also popular owing to their high speed sensing mechanism and low power consumption [22-23]. Conventionally, both the topologies were differential in nature, but presently single ended bit cells are gaining popularity, therefore single ended SA designs are also in demand.

The efficiency of the SA determines the read operation efficiency for the memory. The operation for the SA is to detect a small differential potential difference that develops on the bitline to sense the data present in the bit cell. The less time it takes, the faster the read operation for the memory. But the decreasing technology node has taken its toll on the performance of SA, making them vulnerable to variability and for credible function occupying high area footprint. Therefore, designing an SA at scaled technology with area efficiency and reduced V_{DD} is turning out to be a real bottleneck for memory designers.

1.2.3 Array Design

Different bit cells and their implementation techniques have been described in literature to improve their performance and achieve various design objectives [24-29]. But, in an attempt to improve and optimize cache memory performance, most designers usually restrict themselves to bit cell design. All the different bit cells described in literature improve performance in terms of one parameter or the other. But a bit cell is only a foundational stone in the design of SRAM. It is a small peg that gets replicated multiple times to form the array that actually acts as the memory core. Thus, designing and optimizing the array configuration for memory is equally essential. Improving the performance for the memory implies collectively improving the performance of the cell when it is placed in an array. In an array arrangement, the cells in the same row and column share control signals. Therefore, performance of the cell gets impacted by its neighboring cell. Thus, deeming it necessary to analyze the performance of a cell in array. Also, for lowering power consumption for memory most researchers focus on lowering the operational V_{DD} for a cell. But SA in general is a circuit that is not operationally at V_{DD} as low as the cell. Thus, an alternative for power saving for memory may be optimizing the array power consumption, but very few research works have explored this arena.

1.3 PROBLEM STATEMENT

Cache memory is an integral part for most microprocessors and SoC circuits. Additionally, with the increasing dependence of hyper-personalized portable devices, and internet of things, the demand for low power, high density, and faster memories is increasing. A method to increase density of cells per unit area is lowering the technology node, while for power reduction the orthodox method is to reduce the V_{DD}. But, with the decreasing technology node, the performance of the conventional bit cells is deteriorating. This is further augmented by lowering the V_{DD}. Therefore, there is need to design a cell that is operational for low voltage and is designed with low transistor count to keep its area under check.

The conventional mechanism to design a cell is to identify the specifications that it has to cater to, and then design its topology. But, in doing so designers have accepted certain trade-offs. But with the growing technological needs, new mechanisms need to be designed to tackling these trade-offs. One such accepted notion is that a cell can operate in a single mode configuration only. But most dynamic devices that are round the clock connected require cells that can cater to low power as well as high speed operations. Thus, generating need for a cell that can operate in low power mode, and when needed switch to high speed mode.

Another circuit essential for proper functioning of a cache memory is the SA. As the bit cells for the memory are being redesigned, there is a need for a SA that is compatible with these modified cell topologies. Thus, once the bit cell topology is finalized, it is essential to design an SA compatible with its design. Also, the shift of cell design from differential ended to single ended configurations, has generated the need for a single ended SA as well.

Also, a bit cell is a small peg in a large array used to form the cache memory. Therefore, it is essential to analyze performance of a cell in array configuration to check the influence of bit cells on each other. When cells are replicated multiple times to form an array configuration, the half select disturbance (HSD) starts hampering cell performance. Also, it is essential to check for impact of bit error on the overall performance of the array.

1.4 OBJECTIVES

The growing demand for faster memory with higher integration density has generated the need for re-designing memory and its peripheral components for performance enhancement.

Also, the cumulative aftermath of reduction in technology node, scaling V_{DD}, and increased process variation may result in augmented memory failure. Thus, the following four objectives were formulated to improve the performance for SRAM.

Objective 1:

Design and analysis of an area efficient, low power 7T SRAM bit cell at 32 nm technology node, resilient to process variation.

Objective 2:

Design a dual mode operational SRAM bit cell with the capability to switch between different configurations.

Objective 3:

Design and performance analysis of a sense amplifier to club the merits of voltage based and current based topologies for performance enhancement.

Objective 4:

Analyzing the proposed array arrangement to reduce vulnerability towards half select issues and bit error.

The detailed methodology followed to achieve each the aforementioned objectives is explained in the following section.

1.5 OBJECTIVE-WISE METHODOLOGY

The methodology adopted to achieve the formulated objectives regarding single ended bit cell, dual mode operational bit cell, SA, and array design is as follows -

Methodology for Objective 1

The foremost objective is to design a bit cell that has a low area footprint, low power applications, and is resilient to process variations. Based on the review of pre-existing bit cells, four possible designs using different port topologies and multi-threshold transistors, for a single ended 7T SRAM cell are proposed. Then, the performance for the different

proposed cell topologies is compared to identify the best design amongst the proposed designs. Once the best performing bit cell is identified, its performance is validated against the performance of the pre-existing cells for various parameters. The performance of the proposed 7T cell for process variation is also compared against other pre-existing cells.

Methodology for Objective 2

Conventionally, cells are designed to operate in a single configuration, but low power and high speed operation are two highly desired attributes for a bit cell. But these two attributes are complementary in nature. One is generally achieved at the cost of the other. Thus, it is essential to conceptualize a dual mode operational cell for low power and high speed operation. Before a dual mode operation cell is designed, it is paramount to design a single ended, dual port 7T bit cell. Once the design for dual port cell is finalized, its performance is validated against other pre-existing 7T bit cells. Thereafter, the design for the dual mode operational cell using proposed single port and dual port cells is finalized and its performance is analyzed.

Methodology for Objective 3

Along with the bit cell, the SA is also an essential circuit for SRAM. With the growing popularity of single ended bit cells, it is essential to design a modified single ended SA topology for faster sensing and low power consumption. The performance for the proposed single ended SA is analyzed to ensure its fast operation. Next, its performance is analyzed for PVT variations. Thereafter, the performance for the proposed SA is validated against other single ended SA designs.

Methodology for Objective 4

Along with the bit cell it is also essential to analyze the performance of the proposed single port and dual port bit cells in the conventional array arrangement. The performance of the array is analyzed to propose a hybrid array configuration using the proposed single ended, single port and single ended, dual port cells. The proposed hybrid array configuration is analyzed for half-select disturbance. Thereafter, the proposed hybrid array configuration is analyzed for bit error and power consumption.

1.6 THESIS ORGANIZATION

The thesis is organized into seven chapters, beginning with the first chapter dedicated to introduction. In the second chapter, an overview of different bit cell topologies, their designs, and categorizations, along with the different SA topologies and array configurations is presented. Chapters three to six are dedicated to the four objectives identified based on the technical gaps. Finally, in chapter seven the key findings are summarized and the future for the work is presented. A brief overview of contents of each chapter is as follows -

Chapter 1: In this chapter, the SRAM circuit comprising of the bit cell array and its peripherals is explained. The different topics addressed in the thesis – memory bit cell, SAs, and array design, are briefly introduced in this section. Their significance and the present trends are also highlighted in this chapter.

Chapter 2: In this chapter, a detailed literature review of the different topologies for bit cell, SAs, and array configurations is presented. The different bit cells reported in literature are described and analyzed to categorize them on the basis of the number of transistors used to design the bit cell. This is done to analyze the different properties and attributes of the bit cells. Based on the analysis the seven transistor topology is identified as the most probable and suitable successor for the conventional bit cell. Therefore, different 7T cells reported in literature are then categorized based on the port topology and sensing scheme used by the cell.

Additional to the bit cells, details of the different sensing amplifier topologies and their categorizations based on sensing scheme are also detailed in this chapter. The characteristic of voltage based, and current based SA is also presented to identify the scope of improvement in the SA design. Thereafter, the different array configurations reported in literature are reviewed.

Chapter 3: In this chapter, four different configurations for a single ended, single port 7T bit cell are proposed. The different bit cells are designed based on the learning from the review presented in chapter 2. The proposed cells differ in terms of their read port topology or the utilization of high performance, low threshold voltage transistor to boost bit cell performance. The performance of the different 7T bit cells proposed in this chapter are then compared to identify the best configuration.

Chapter 4: In this chapter, firstly the concept and method of a dual mode operational bit cell is proposed. This is followed by explaining the design of the proposed single ended, dual port 7T bit cell. The proposed dual port 7T cell is then evaluated for its performance against the pre-existing 7T cells. Thereafter, the best identifies single ended, single port cell from chapter 3 and the single ended, dual port 7T cell proposed in this chapter are used to design a dual mode operational 7T bit cell.

Chapter 5: In this chapter, a single ended SA topology is proposed. The proposed SA is designed based on the learning of the review of pre-existing SA topologies in literature. The proposed design is voltage mode in operation but uses an NMOS switching transistor to uplift its performance. The performance of the proposed SA is validated against pre-existing design.

Chapter 6: In this chapter, a new array configuration is proposed using the single ended single port cell proposed in chapter 3 and single ended, dual port cell proposed in chapter 4. Conventionally, when aiming to reduce power consumption, most researchers target bit cell power reduction. But, in this paper an unconventional technique to lower power consumption by changing the array design for the memory is proposed. The proposed array configuration is based on the concept that not all bits in a word are of the same importance. The lower order bits in a word may be more vulnerable to noise than higher order bits. For analysis, an 8kb memory is considered with 512 rows and 16 columns. The best results are obtained when six dual port and ten single port cells are used to design the array.

Chapter 7: In this chapter the key findings of each chapter are summarized point-by-point to explain how each objective is achieved and their key features are reiterated. In the future scope section, the different aspects that can be worked upon are highlighted. Also, different possible aspects for further memory improvement are listed.

The chapters are followed by the list of publications and references. All the patents/papers published, submitted and under progress for the completion of this work are listed in – List of Publications. While all the books and papers that were referred to during the study to form the basis for this work are listed in the reference section.

CHAPTER – 2

LITERATURE REVIEW

Memory has been the center of attention for performance enhancement for a very long time. Researchers have proposed various techniques and designs for improving performance of single or multiple components of memory. Bit cell design have received special attention from researchers, as bit cell is the heart of SRAM. Attempts have also been made to modify SA designs for better compatibility. While, array configuration optimization is a fairly recent domain. Thus, a detailed review of pre-existing designs, configurations, and topologies is essential to understand the different challenges that need to be overcome, while designing a new modified and improved cell, SA, and array for performance enhancement. Thus, in this chapter, a detailed review of the different memory cells, SA, and array designs is presented.

The chapter is divided into six different sections, starting with introduction, section 2.1. It is followed by section 2.2 dedicated to different bit cells based on transistor count and their performance analysis. This section helps identify 7T cell as the most suitable transistor count for cell design. Thus, the next section 2.3 is devoted to different 7T cells, their characterization based on port topology, and performance analysis. Further in section 2.4, the different SA topologies are explained, and their performance is commented upon. While in section 2.5, different approaches for array implementations are explained. Finally, based on the literature review the identified technical gaps are elaborated upon in section 2.6.

2.1 INTRODUCTION

The key feature for a microprocessor is its multi-core architecture and fast operation. The optimal functioning for a processor is reliant on the performance of the internal cache memory. This internal memory for the processor is formed by a matrix of SRAM bit cells. Consequently, improving the performance metric for a single bit cell has a multi-fold impact on the performance of the memory array. Additionally, with the increasing demand for high density memory blocks, area footprints have become a key parameter.

Presently, SRAM accounts for approximately 30% of the overall power consumption for a system [30] and as for the near future, it is predicted that SRAM may occupy nearly 90% of the total processor area [31]. Therefore, while designing a bit cell it is mandatory to keep the area footprint in check, while reducing the power appetite of the cell. The primary technique to reduce power appetite for a cell is to lower the V_{DD}, to decrease leakage and dynamic power [32]. But, in short channel devices V_{DD} lowering is restricted by PVT variations [33] and static noise margin (SNM) degradation. The SNM degradation is an implication of exponential relation between SNM and threshold voltage (V_{TH}) of the device [34].

The overall power consumption for a cell is the sum of its static and dynamic power components, the charging and discharging event accounts for 60% of the latter component [35]. Therefore, limiting the charging/discharging event for a cell reduces its dynamic power consumption. Consequently, to reduce switching power consumption, single-ended cell topologies are gaining popularity [36-39]. Various other researchers have also reported other cell configurations to rectify the abovementioned problems [40-46]. Therefore, in this chapter a detailed review of different bit cells, SAs, and array designs is presented to understand the different topologies, and techniques reported over time to improve the performance for each SRAM component. It is essential to develop a deep understanding of the different techniques so as to design and develop new modified SRAM components to improve performance.

2.2 COMPARATIVE ANALYSIS OF DIFFERENT SRAM CELLS BASED ON TRANSISTOR COUNT

There are numerous bit cells that have been described in literature; a conventional method to categorize cells is on the basis of the number of transistors. The characteristics and schematic diagram for different bit cells categorized based on transistor count are summarized in this section. Major design objectives for a bit cell are – low area footprint, operational at low V_{DD}, reduced power consumption, faster operation, and high bit density.

2.2.1 Schematic Designs for Different SRAM Bit Cells Based on Transistor Count

The conventional SRAM cell was a six transistor (6T1) bit cell, as depicted in Fig. 2.1 (a). Its speedy operation along with smaller area footprint made it the “de facto” model for

implementation. But at lower technology nodes the high value of leakage current, increases the static power consumed by cell [47-48]. Its performance also suffers majorly because of the inherent read-write conflict and HSD. Its high power consumption for enlarged transistor sizing is also a troublesome parameter for scaled technology node.

In an attempt to lower power consumption, by reducing the discharging event, a single ended, dual port 6T (6T2) cell was described in 2019 [49]. The transistor based diagram for the cell is presented in Fig. 2.1 (b). This cell increases the number of control signals, leading to an increment in the overall capacitance of the memory. This increases the dynamic power for the memory and also designing complexity for the SA. This cell outperforms the 6T1 bit cell in terms of leakage, but the overall energy consumption and area for the embedded memory is quite large.

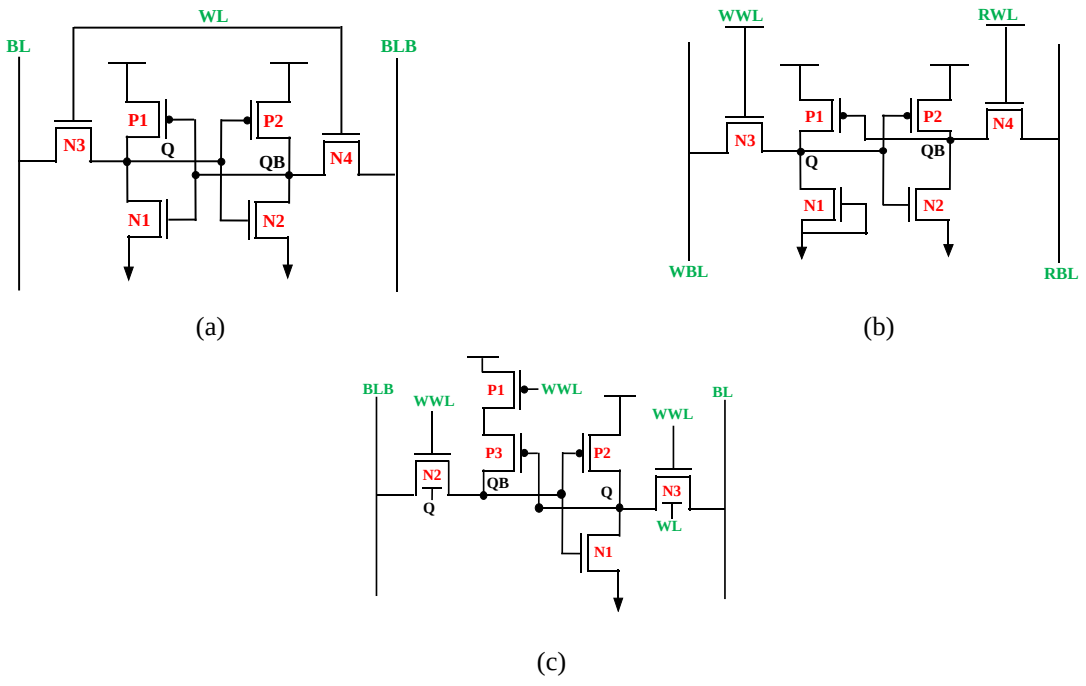


Fig. 2.1 Schematic design for (a) 6T1, (b) 6T2, and (c) 6T3 bit cell.

Another 6T cell was designed by Asli and Taghipour [50] in 2019. It is an asymmetrical 6T (6T3) cell with resilience to soft error, it performs reliably against ageing effects and enhances read performance. The cell employs back gate biasing technique to achieve the desired results. The schematic diagram for 6T3 cell is depicted in Fig. 2.1 (c). It eliminates the left pull down transistor to weaken the positive feedback between the latch inverters to facilitate write '1' operation.

To uplift the performance of the 6T cells, other designers have reported different 7T cell topologies. One such 7T design - 7T1, was presented by Aly and Bayoumi [51] in 2007. The circuit diagram for the bit cell is given in Fig. 2.2 (a). Its memory element is alike 6T1, with an additional N5 transistor added in the feedback connection. The utility of N5 is to establish/break the feedback connection between the inverter pair. It uses a single bitline for the write operation to yield better results. It was designed for 180 nm technology node and 1.8 V V_{DD}. Therefore, at scaled technology node and lower V_{DD}, its performance deteriorates.

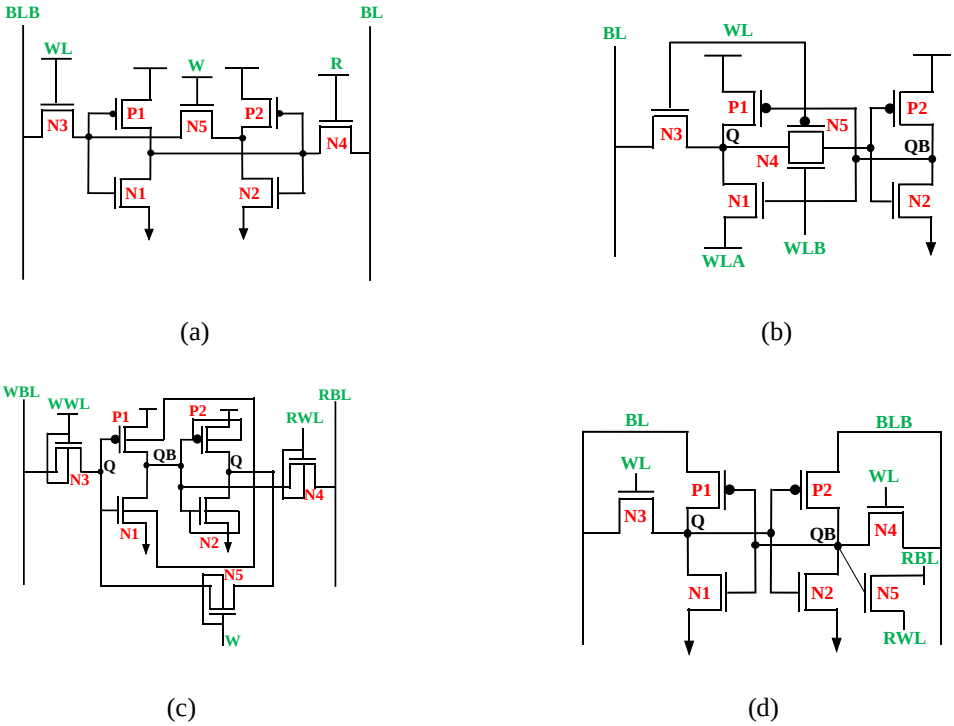


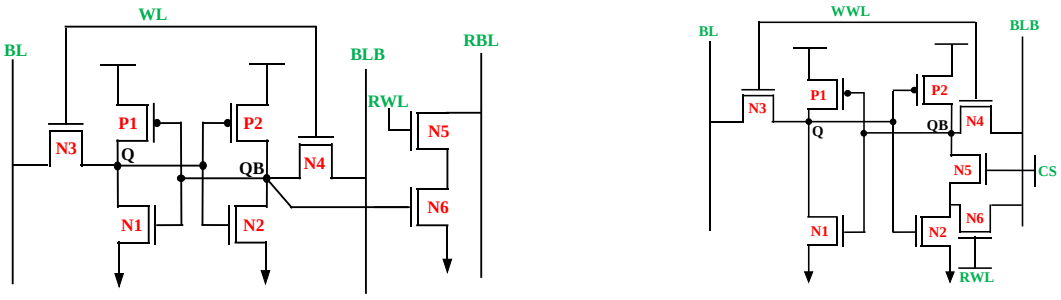
Fig. 2.2 Schematic design for (a) 7T1, (b) 7T2, (c) 7T3, and (d) 7T4 SRAM bit cell.

Another 7T cell - 7T2, was proposed by Yang *et al.* [52] in 2016. It uses a single ended approach for both read and write operations. The circuit diagram for this 7T2 cell is given in Fig. 2.2 (b). It is dependent on transmission gates for disconnection of node Q from input node for the right inverter. The cell has four control signals which are used to steer the bit cell into different modes of operations. It is dependent on two pulses to perform the write operation, thereby reducing its speed. Also, the use of additional control signals increases its complexity, overall footprint, and power consumption of the cache memory.

To uplift cell stability, another 7T cell (7T3) was reported by Sanapala *et al.* [53] in 2018. This cell utilizes Schmitt Trigger (ST) for performance enhancement. Schematic for 7T3 cell is shown in Fig. 2.2 (c). It relies on dynamic body bias that allows altering the switching

voltage by varying the V_{TH} of the transistors in keeping with direction of input transition.

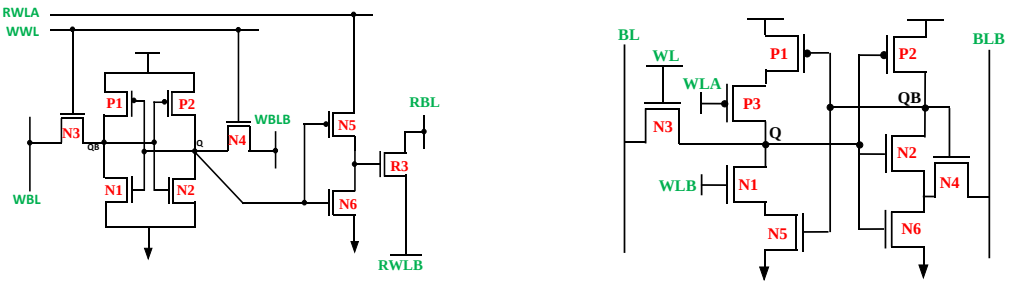
Another recent schematic for 7T cell (7T4) was proposed by Ahmed *et al*. [54] in 2018. This cell is an improvement of the cell presented by Liu *et al*. [55]. The schematic for 7T4 is depicted in Fig. 2.2 (d). This cell has an isolated read port structure, that does not upset the value stored in the memory core. But, to rectify the write fail for low voltage, its V_{DD} assist is modified. The pull up devices for the cell are powered by the bitline pair. This method provides a data dependent supply collapse during the write operation.



(a) (b)

Fig. 2.3 Schematic design for (a) 8T1, and (b) 8T2 SRAM bit cell.

In an attempt to improve performance, researchers have designed 8T cells for read and write port isolation. An eight transistor (8T1) cell was reported by Wen *et al*. [56]. The schematic diagram for 8T1 cell is represented in Fig. 2.3 (a). The read port and its stacked configuration aids in leakage reduction [57]. Another eight transistor (8T2) cell was reported by Singh and Vishvakarma [58]. The schematic diagram for the circuit of 8T2 cell is shown in Fig. 2.3 (b). The cell uses an extra transistor (N5) to disconnect the QB node from the ground rail to boost the single ended read stability. This cell depends on an XOR gate common to a row for its functioning. This requirement for each row has multifold impact on density and overall power consumption for the cache.



(a) (b)

Fig. 2.4 Schematic design for (a) 9T1, and 9T2 SRAM bit cell.

A cell with nine transistors – 9T1 is depicted in Fig. 2.4 (a) [59]. An additional inverter connected to the node Q is used for its read port design. This cell has a notable increase in sensing delay [59]. Another 9T designed with a modified inverter topology is 9T2. It also uses an ST based inverter for memory core designing [60], as it has the ability to manipulate switching voltage subject to the direction of input transition [61]. The schematic for the 9T2 is illustrated in Fig. 2.4 (b). But, for this cell the increased number of control signals causes routing complexity and increased area footprint.

Other ST inverter based cells reported by J. P. Kulkarni [62] and K. Roy [63] are – 10T1, and 10T2 cells. The schematic for the 10T cells is depicted in Fig 2.5 (a), and (b), respectively. They are designed to improve cell stability with lowering V_{DD} [62]. Thus, 10T1 cell has a built-in feedback mechanism for improved process variation tolerance. The 10T1 cell is modified to design this 10T2 cell. The two ST based bit cells have similar schematic with an exception that, 10T2 bit cell relies on an additional control signal to control the feedback transistor.

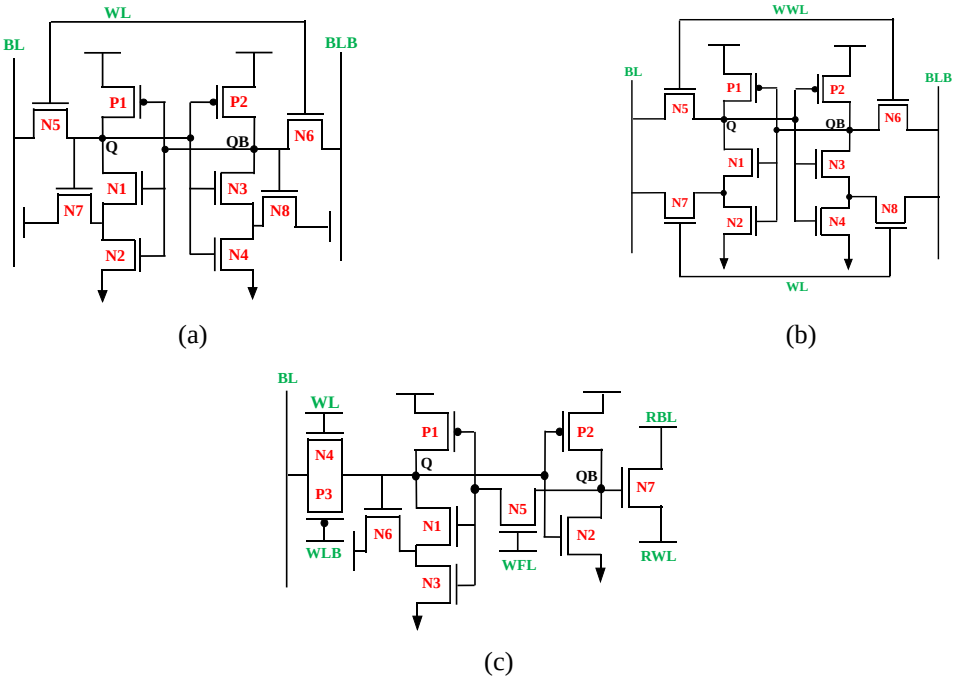
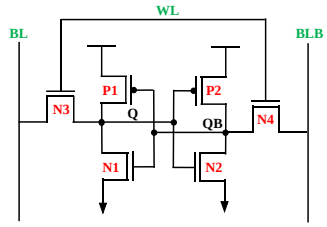
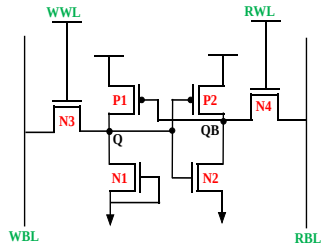
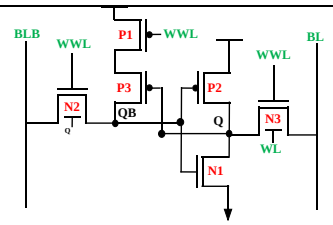
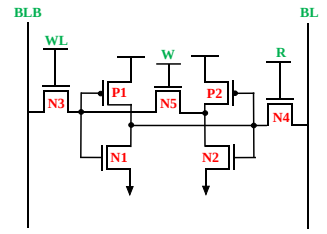
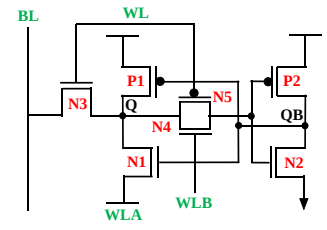


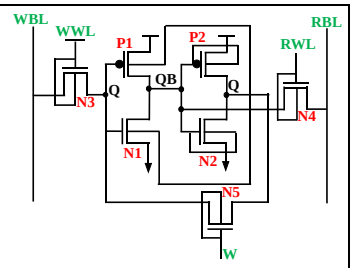
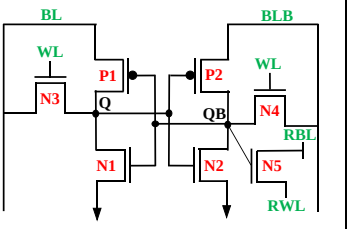
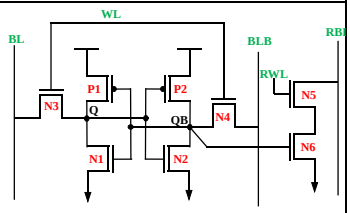
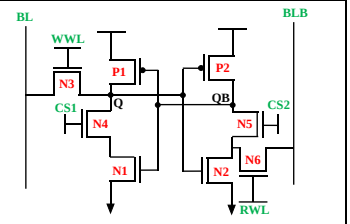
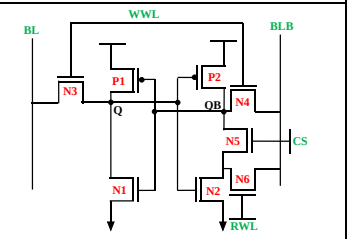
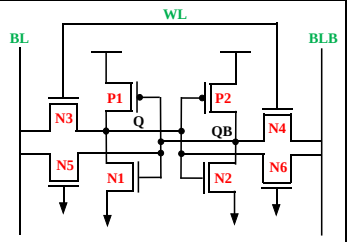
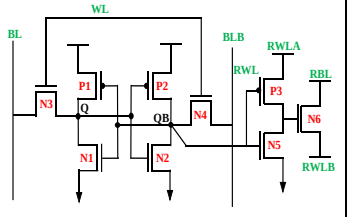
Fig. 2.5 Schematic design for (a) 10T1, (b) 10T2, and (c) 10T3 SRAM bit cell.

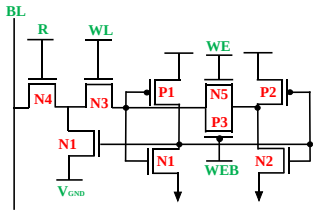
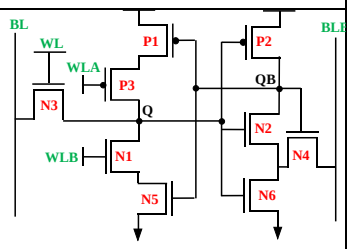
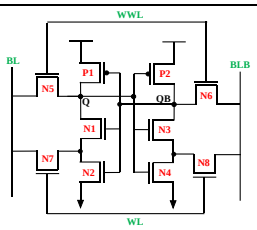
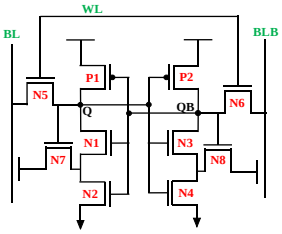
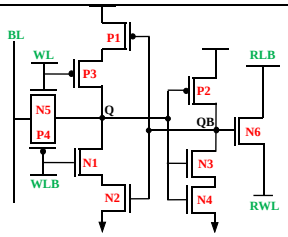
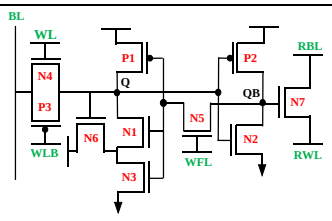
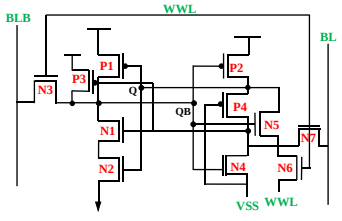
Another 10T cell – 10T3 was reported by Shakouri *et al.* [64] in 2021. It also uses an ST based inverter and a conventional inverter for its memory core. The schematic diagram for 10T3 cell is shown in Fig. 2.5 (c). The transmission gate enables single ended write operation, whereas the N7 transistor facilitates the read operation. It is prone to HSD during

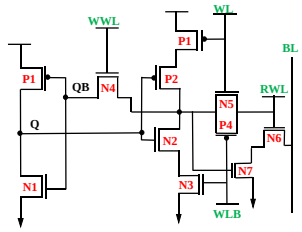
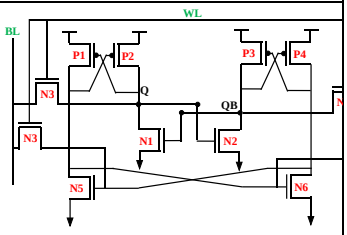
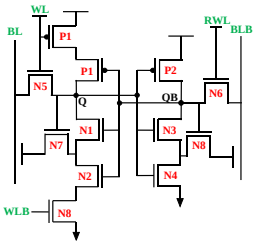
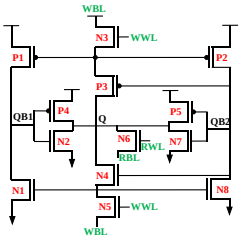
the write operation. Therefore, it requires an internal write back mechanism to resolve the same [65]. For ease of comparison and understanding, the key findings of the different pre-existing bit cells based on transistor count are summarized and presented in Table 2.1.

Table 2.1 Summarized key features of different pre-existing SRAM bit cells based on transistor count

S. No.	Cell Description	Schematic Design
1.	**6T – Arnaud *et al.* [48], 2003.** • The de-facto memory cell. • Single port, differential read and write. • Decrease in technology node, leads to poor performance. • Large area footprint.	
2.	**6T-Surana and Mikie [49], 2019.** • Differential ended read and single ended write. • Uses a LV_{TH} MOS for better noise margin. • Modifies the inverter core the memory. • Large power consumption.	
3.	**6T-Asli and Taghipour [50], 2019** • Asymmetrical design for the memory core. • Eliminates the pull down network for inverter. • Differential write and single ended read.	
4.	**7T-Aly *et al.* [51], 2007.** • Reported for 180 nm and V_{DD} of 1V. • Differential ended read and single ended write. • Poor performance at lower technology node. • Cascaded inverter configuration for write operation.	
5.	**7T-Yang *et al.* [52], 2016.** • Single ended read and write operations. • Dependent on two pulses to perform the write operation. • Reduces the speed of write operation	

6.	**7T-Sanapala *et al.* [53], 2018.** • Schmitt Trigger based memory core. • Disconnects the mutual feedback between the coupled inverter pair. Low hold and read noise margins. • The layout design for the cell is complex.	
7.	**7T-Ahmad *et al.* [54], 2019.** • Isolated read port improves read stability. • Modified V_{DD} assist, bolsters write operation for low V_{DD}. • Data dependent supply collapse during write operation.	
8.	**8T-Wen *et al.* [56], 2016.** • Single ended read, and differential ended write. • Improves read isolation, low OFF current. • Increases area, and power consumption.	
9.	**8T-Kushwah and Vishwakarma [66], 2016.** • Single ended read and write. • Reduces differential switching power. • Improves read stability, and immunity to PVT variations.	
10.	**8T-Singh and Vishwakarma [58], 2017.** • A stable and low voltage cell. • Single ended read and differential ended write. • Reduces leakage current and increases area, and power.	
11.	**8T-Gitermann *et al.* [67], 2018.** • Symmetrical design. • Gate for N5 and N6 are always grounded. They are always in cut-off mode. • For hold mode, the leakage current distribution is even for the cell.	
12.	**9T-Yang *et al.* [59] 2015.** • Utilizes a read buffer circuit. • RWLA and RWLB are forced to V_{SS} and V_{DD} for read operation. • The read port improves delay and current ratio.	

13.	**9T-Pal *et al.* [68], 2019** • Transmission gate (TG) is used to break feedback. • For write operation V_{GND} is set to V_{DD}, and TG is OFF. • TG is ON during hold and read operation.	
14.	**9T-Cho *et al.* [61], 2020.** • A ST based inverter is used to design the memory core. • Uses WLA and WLB to control P3 and N1, respectively. • Improves hold stability but increases area.	
15.	**10T-Kulkarni *et al.* [62], 2007.** • Additional feedback resolves inherent read-write conflict. • Reduces the control signals. • Larger power consumption and area footprint.	
16.	**10T-Kulkarni *et al.* [63], 2012.** • Schmitt Trigger based inverter core. • Improves read stability. • Power consumption and area footprint are high. • The transistor count is also very high.	
17.	**10T-Eslami *et al.* [69] 2020.** • Memory core formed by stacked inverters. • The write port uses TG, read port is SNM free. • Suffers in terms of dynamic ability and high area overhead.	
18.	**10T-Shakouri *et al.* [64], 2021.** • Uses transmission gate for write operation. • Single ended read port. • N5 transistor is used to improve write stability. • Prone to HSD during the write operation.	
19.	**11T-He *et al.* [70], 2019.** • Additional transistors to improve read stability. • Uses virtual ground to charge/discharge data node. • But the area increases significantly.	

20.	**11T-Lorenzo and Pailly [71], 2020.** • Uses read SNM free port with stacked transistor. • Single ended, single port cell, with improved stability. • Leakage current is low. • Decoupling transistor solves the half-select issue.	
21.	**12T-Jiang *et al.* [72], 2019.** • The cell has four data nodes. • Differential ended cell, therefore power consumption is high. • Two discharge paths for read operation, faster read.	
22.	**12T-Sachdeva and Tomar [73], 2020.** • The memory core for the cell is designed using Schmitt Trigger based inverter. • Single ended read and differential ended write operation. • The P1 and N8 transistor are turned off during the read operation.	
23.	**13T-Atias *et al.* [74], 2016.** • Designed for ultra-low power operation in space application. • Uses dual feedback to overcome vulnerabilities. • The cell has two stable states and five separate data nodes.	

A major design issue in the bit cells is the conflict between the read and write stability. Bit cells requires a high cell ratio for a stable read operation. On the contrary, this degrades the write ability due to reduction in the strength of access transistors that in turn raises the write access time. Similarly, the pull-up ratio should be small enough to increase the write ability, but it deteriorates the read performance. Another key drawback of previously reported bit cells is that they often focus on improvement of one of the three – hold/read/write – operations. Generally, this improvement in one parameter is attained at the cost of the other.

2.2.2 Performance Comparison for SRAM Bit Cells Based on Transistor Count

In this section, cells up to ten transistors are simulated and compared. Cells with transistor count greater than ten are not included, as the demerit of area increment outweigh the enhancement in performance for the cell. All the cells are designed for 32 nm technology node and were simulated for 300 mV V_{DD}. Each cell is evaluated for stability, dynamic

analysis, process variation, temperature variation, and area footprint. This performance comparison for cells based on transistor count is performed to identify the most suitable transistor count for designing a new bit cell topology.

A. Static Noise Margin Analysis

The conventional method to measure the stability of a cell is the SNM; it is the maximum noise level a cell may withstand before an erroneous flip in the data of the bit cell is registered [75, 76]. It is obtained by graphically superimposing the transfer characteristics of the inverter core resulting in a two lobe based curve [77], called the butterfly curve. The SNM is the measure of side of the largest square that fits perfectly inside the smaller lobes of the butterfly curve [78]. The hold SNM (HSNM) values for the pre-existing cells based on transistor count are compared in Fig. 2.6. The 10T cells – 10T1, and 10T2, have the highest HSNM values at 117, and 100 mV. It is closely followed by 8T1 with HSNM of 96 mV. While the 6T1, 6T3, 7T1, 7T2, 7T4, 8T2, 9T2, and 10T3 cells register HSNM value higher than 75 mV. The remaining cells have fairly low hold stability.

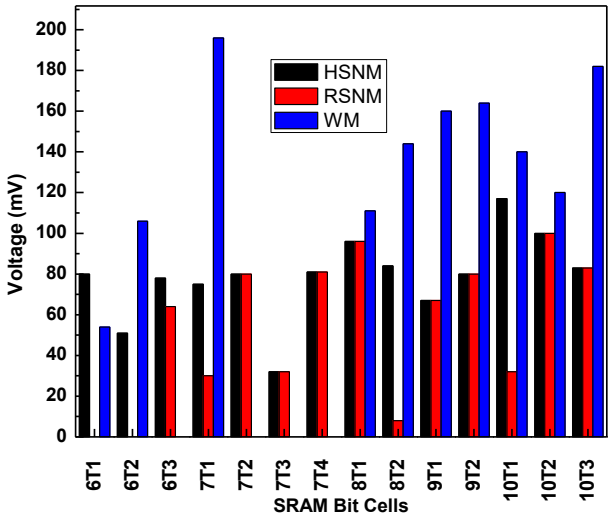


Fig. 2.6 Graphical comparison for HSNM, RSNM, and WM values obtained for the different SRAM bit cells.

The resilience of the cell during read mode is quantified as read SNM (RSNM). A differential read operation always has poor performance in comparison to single ended read [79]. The RSNM values obtained for different bit cells based on transistor count are depicted in Fig. 2.6. Based on the RSNM values, the read operation is highly stable for 7T2, 7T4, 8T1, 9T2, 10T2, and 10T3, as their RSNM is higher than 80 mV. The 6T1, 6T2, and 8T2

cells are extremely vulnerable to read noise as their RSNM values are obtained to be less than 5 mV.

Write margin (WM) is a reliable parameter to determine a cell's write ability [80]. It is estimated as the difference between the voltage level of V_{DD} and wordline signal when the bit stored in the cell flips [81]. WM is measured using the methodology recommended by Islam and Hasan [82]. The WM values for all bit cells except 7T2, 7T3, and 7T4 are compared in Fig. 2.6. The write operation for these cells is divided into two pulses thus; the comparison is avoided to not project them as pseudo poor. The cells with nearly ideal WM values are 8T2, 9T1, 9T2, and 10T1 at 144, 160, 164, and 140 mV, respectively. The 6T1 cell has an extremely low values at 54 mV, while 6T2, and 10T2 register values of 106, and 120 mV. Whereas, extremely high values of WM are obtained for 7T1, and 10T3 cells at 196, and 182 mV, respectively.

B. Dynamic Write Analysis

During static analysis, the pulse width for the write control signal is assumed to be infinite. While, for real time operations the pulse width for write operation is finite. The write time is defined as the least possible pulse width required to alter the bit value stored in the cell. If it is less than that, then the data in the cell will not change, causing a write failure. The cells with the least time requirement for the write operation are 8T1, and 9T1, with values of 30, and 35 ns.

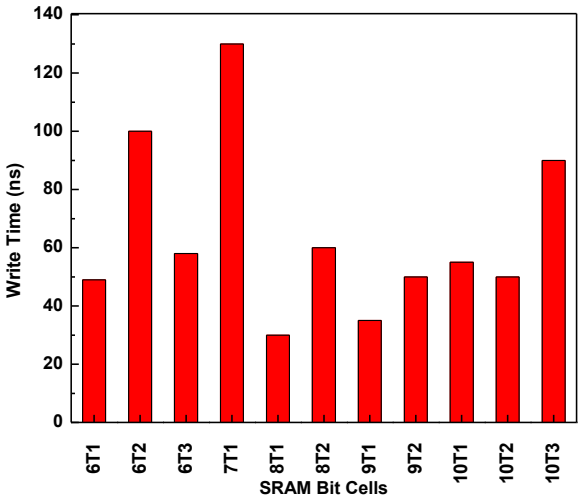


Fig. 2.7 Graphical comparison of dynamic write time required for the different SRAM bit cells.

The write time vales obtained for the different bit cells are compared in Fig. 2.7. The write

operation for the 6T2, 7T1, and 10T3 is significantly slow as their pulse width is greater than 90 ns. The 7T2, 7T3, and 7T4 were not included in this comparison owing to their dual pulse write operation. The write operation for the 6T cells, 7T1, and 10T3 is fairly slow. Also, it may be inferred that write operation for the 7T1 cell needs to be improved, and for the other 7T cells need to be modified to have a single pulse write operation.

C. Process Variation Analysis

The sharp decline in technology node has resulted in serious variability issues at the circuit level [83]. Whereas, the increasing size of cache memory has resulted in an upsurge in process variation among cells. This causes degradation in performance of adjacent bit cell due to asymmetrical characteristics [84]. Therefore, statistical methods are utilized to detect this degree of variation in the performance of all the cells. Inter-die V_{TH} mismatch is taken as the main statistical parameter for evaluation.

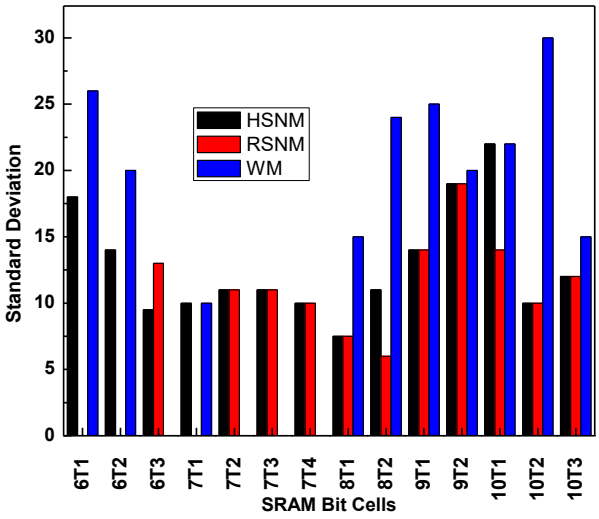


Fig. 2.8 Graphical comparison of standard deviation in SNM values of each cell due to process variations.

The factors responsible for process variation are line edge roughness, chemical-mechanical polishing, random dopant fluctuation, and lithography effects [85]. Most of these parameters are neither predictable nor can they be controlled. But the location and distribution of these factors influences the V_{TH} [85]. Therefore, in this work, V_{TH} is used as the primary source to predict the variability tolerance of a cell. The impact of process variation on the SNM values is explained in terms of standard deviation. The standard deviation values of each SNM for all the cells are compared in Fig. 2.8. The cells that register low variation in their SNM

values due to process variation are the 7T cells and the 8T cell. The cells with 9T and higher transistor count register a high variation in performance. Also, the 6T cells are also highly susceptible to process variations.

D. Temperature Variation Analysis

SRAM circuits are required to function under a wide range of temperatures. Device temperature may surge due to relentless operation or environmental circumstances. Therefore, to account for the temperature variation encountered by the cache memory, a temperature variation analysis is performed for all the pre-existing cells explained previously.

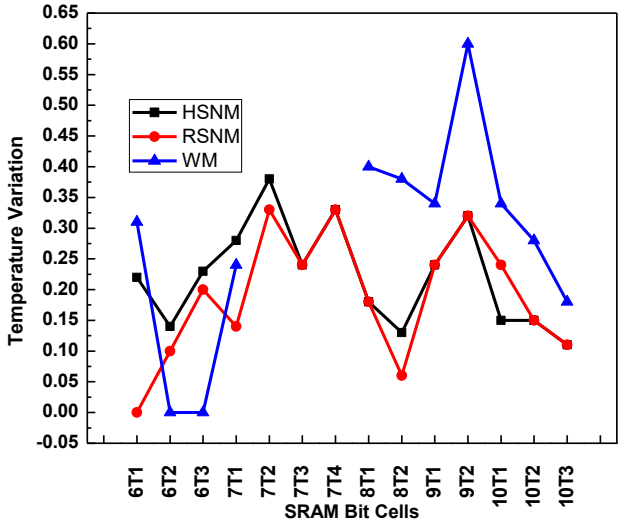


Fig. 2.9 Graphical comparison of variation in SNM values for all the pre-existing cells.

This is accomplished to ensure the performance reliability of the cell. The analysis is performed for temperature varying from -10 ºC to 110 ºC. The result for the analysis is presented in Fig. 2.9. With variation in temperature, a deviation in performance of static parameters for the cell is observed. The cells with a balanced variation in performance due to temperature variation is the 7T1 cell. The hold and read SNM values for other 7T cells are also balanced. The highest variation in performance is recorded for the 9T2 cell. The 6T cell performs poorly; a collapse in butterfly curve for read operation is registered for 6T1 cell, whereas the write stability suffers for 6T2 and 6T3. Thus, based on this performance evaluation also, the 7T cells may be deemed the most superior in performance.

E. Area Footprint Analysis

SRAM cells are arranged into large array to form cache memory. Thus, in order to integrate a large number of bit cells into the cache memory, it is imperative to have minimal area for a bit cell. The length (µm), width (µm) and area (µm^2) for all the pre-existing cells are compared in Fig. 2.10. The minimal area footprint is observed for 7T3, 6T3, 6T1 7T2, 7T4, and 7T1 bit cell at 0.474, 0.565, 0.574, 0.614, 0.703, and 0.733 µm^2, respectively. The layout for the 8T, 9T, and 10T3 cells is moderate, whereas a very high area footprint is observed for the 10T1 and 10T2 bit cell.

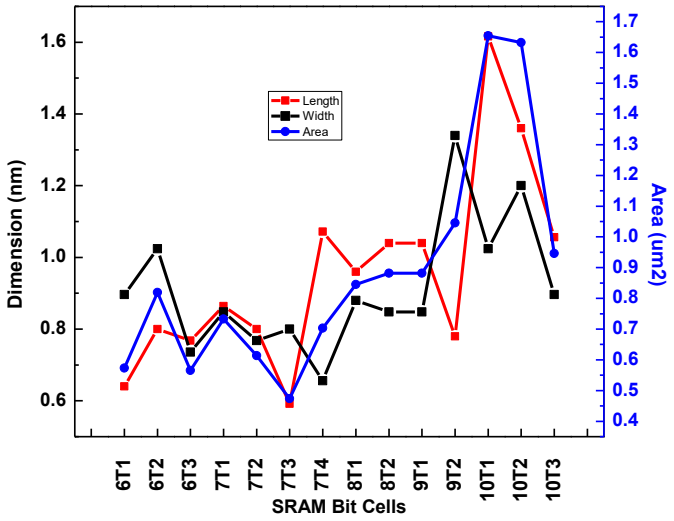


Fig. 2.10 Graphical comparison for the length, width, and area for the pre-existing cells.

Based on the performance assessment for the different bit cells based on transistor count, the 7T transistor bit cell is identified as the most optimal transistor count for cell design. The 7T cells register a reasonable stability towards hold, read, and write operation. They are fairly tolerant towards process and temperature variation. The area footprint for the cells is also low, thereby making them economically feasible. Thus, in the subsequent section a detailed review of different 7T bit cell designs reported in literature is presented.

2.3 COMPARATIVE ANALYSIS OF DIFFERENT 7T SRAM CELLS

Various 7T bit cells have been reported in literature, all these 7T cell topologies for ease of understanding can be characterized based on the methodology they utilize for read and write operation. If a cell utilizes both – bitline (BL) and bitline bar (BLB) for read as well as write operation, it is referred to as differential cell. Whereas, if the cell relies on single bitline configuration to perform its operations, then the cell is referred to as single ended cell. If a

common bitline or bitline pair is used for performing both the operations then, the cell is categorized as single port bit cell. Whereas, if the bitlines used for write and read operation are isolated from one another, then the cell is said to have a dual port architecture. So based on the configuration, a cell can be grouped into one of the following four categories - 1) Differential ended, single port, 2) Differential ended with isolated read port, 3) Single ended, dual port and 4) Single ended, single port.

2.3.1 Differential Ended, Single Port 7T SRAM Bit Cells

When a cell utilizes complementary bitlines for an operation, it is referred to as a differential ended cell. If the same set of bitlines are used for both read and write operations, then the cell is a single port cell. Conventionally, cells were designed with this configuration, and it is still a preferred choice for cell design.

A. Schematic Designs of Differential Ended, Single Port 7T SRAM Bit Cells

Aly and Bayoumi [51] in 2007 reported a differential ended, single port 7T cell (7TA). The mutual feedback connection between the memory core is dependent on an NMOS transistor – N5, controlled by signal; W. Its ability to connect and disconnect the feedback connection facilitates the write operation. Once the write operation is complete, N5 is turned back ON. This is done to maintain stability though the course of read as well as hold operation. The transistor level circuit diagram for 7TA is presented in Fig. 2.11 (a).

In 2015, a 7T bit cell (7TAn) was reported by Ansari *et al.* [86] that uses a combination of low threshold voltage (LV_{TH}) and high threshold voltage (HV_{TH}) transistors. The schematic for 7TAn is illustrated in Fig. 2.11 (b). Transmission gate formed by LV_{TH} NMOS (N3) and HV_{TH} NMOS (N4) provides access to the data core of the cell. This cell has difficulty in storing '0' at QB because of the presence of HV_{TH} NMOS (N2).

A modified version for the preceding bit cell was reported by Asli and Taghipour [87] in 2017. The schematic for the cell (7TAs) is depicted in Fig. 2.11 (c). It improves speed and stability for read operation, while maintaining write characteristics as 7TAn. The additional HV_{TH} PMOS (P3), aids in uplifting its write performance. The specification for MOS used in the memory core is given in Table 2.2. The major drawback for cells reported in [86] and [87] is that their schematics are a combination of multiple HV_{TH} and LV_{TH} MOS transistors.

This will result in design and synthesis problems. As conventional synthesis tools allow only a single type of device in library [88]. Also, the fabrication for these two multi-V_{TH} bit cells is bound to experience fabrication errors due to multi-masking process.

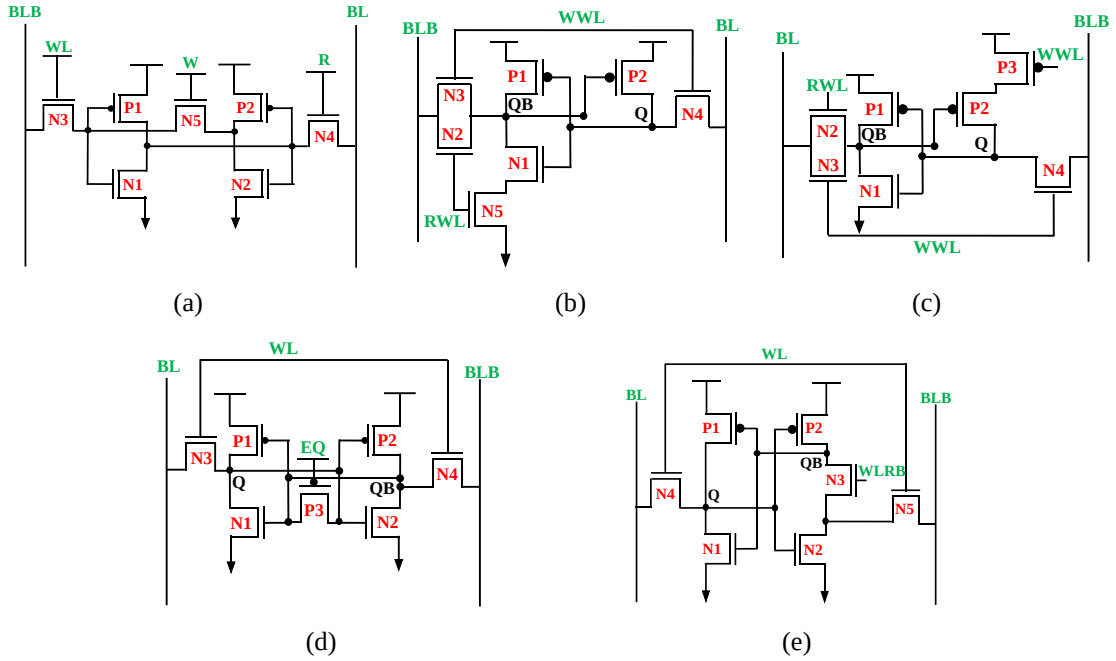


Fig. 2.11 Schematic diagram for (a) 7TA, (b) 7TAn, (c) 7TAs, (d) 7TGi, and (e) 7TO, SRAM bit cell topologies.

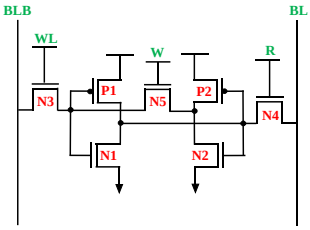
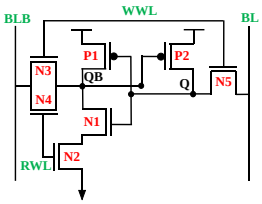
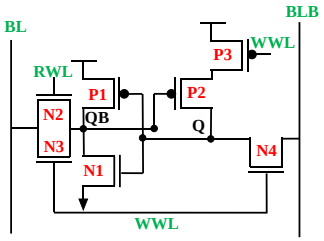
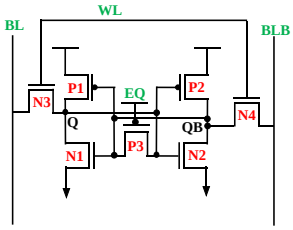
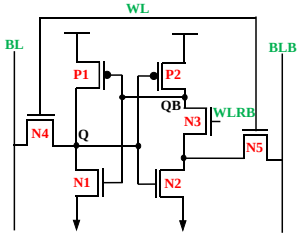
Table 2.2 MOS characteristic for SRAM cells given in Fig. 2.11 (b), (c) and 2.13 (a).

	Fig. 2.11 (b)	**Fig. 2.11 (c)**	**Fig. 2.13 (a)**
P1	HV_{TH}	LV_{TH}	HV_{TH}
N1	LV_{TH}	LV_{TH}	HV_{TH}
P2	LV_{TH}	HV_{TH}	HV_{TH}
N3/N4	LV_{TH}	LV_{TH}	--
N2	HV_{TH}	HV_{TH}	--
N2	--	--	LV_{TH}

In 2018, Giterman *et al.* [89] reported a bit cell (7TGi) with an additional PMOS transistor for equalization during the write operation. The write operation of the cell is performed in two phases. During the first phase V_{DD} is cut off and EQ is high. Thus, by charge sharing process, voltage equalization happens between node Q and QB. Thereby, reducing power consumption during the first phase of operation. The access transistor is then turned ON, only during the second phase. The transistor level circuit diagram for 7TGi is given in Fig. 2.11 (d). This cell reduces the power consumption and correlation between write operation and the data stored.

In 2021, another 7T cell (7TO) was described by Oh *et al.* [90]. This cell relies on additional transistor - N3, to form a stacked inverter configuration. It turns OFF N3 to improve read stability. Its timing is strictly controlled for write operation; or it may result in write failure event. It also increases power consumption and reduces read current due to stacked configuration. Fig. 2.11 (e) depicts the schematic for 7TO cell. The key findings of differential ended, single port cells are summarized in Table 2.3.

Table 2.3 Summarized key features of 7T SRAM bit cells with differential ended, single port configuration.

S. No.	Cell Description	Schematic Design
1.	**7T-Aly *et al.* [51], 2007.** • Reported for 180 nm and V_{DD} of 1V. • Differential ended read and single ended write. • Performance deteriorates with reduction in technology node. • Cascaded inverter configuration for write operation.	
2.	**7T-Ansari *et al.* [86], 2015.** • Uses a combination of H_{VT} and L_{VT} MOS. • Single ended read and a differential ended write. • BL and BLB maintained '0' during hold. • The fabrication is extremely complex.	
3.	**7T-Asli *et al.* [87], 2017.** • Improves speed and stability for read operation. • HV_{TH} transistor, uplifts write performance. • Multi-V_{TH} transistors lead to design and synthesis problems. • Fabrication is complex.	
4.	**7T-Gitermann *et al.* [89], 2019.** • Dual phase write operation. • An additional transistor is used for equalization. • Reduces correlation between write operation and data in cell. • Increases the write time operation.	
5.	**7T-Oh *et al.* [90], 2021.** • Turns OFF R1 to improve read stability. • Timing has to be strictly controlled with reference to WL or may result in write failure. • Increases power consumption and reduces read current.	

All the aforementioned cells are designed at 32 nm technology node for performance analysis. The cells are simulated for V_{DD} of 800 mV. The results obtained for each cell with differential ended, single port configuration are compared in the following sub-section.

B. Performance Analysis of Differential Ended, Single Port 7T SRAM Bit Cells

All the cells were originally proposed for either higher technology node or higher V_{DD}, therefore, in this analysis only their technology node is reduced and not the V_{DD}. Additionally, though the technology node is reduced, the aspect ratios for the cells are maintained as given in their original literature.

Table 2.4 Results obtained for SNM, temperature variation analysis, global variation analysis and power consumption for the differential ended, single port 7T SRAM bit cells.

Bit Cells	Stability Analysis (mV)			Temperature Variation (mV/ºC)			Global Variation (mV)			Power Consumption (pW), (µW), (µW)		
	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write
7TA	304	184	440	0.723	0.23	0.425	18	37	90	166	18	0.053
7TAn	139	92	-	0.21	0.275	-	-	-	-	456	14	5.44
7TAs	319	102	551	0.16	0.23	0.14	-	-	-	540	31	7.84
7TGi	314	46	-	0.23	0.225	-	60	60	-	292	26	2.46
7TO	324	70	266	0.16	0.35	0.26	60	32	101	240	18	4.32

Table 2.5 Results obtained for timing, current ratio, and area footprint for the differential ended, single port 7T SRAM bit cells.

Bit Cells	Timing Analysis		Current Ratio	Area Analysis		
	Write (ns)	Read (ps)		Length (µm)	Width (µm)	Area (µm^2)
7TA	0.4	6	6371	0.864	0.848	0.733
7TAn	-	-	19377	0.976	1.008	0.984
7TAs	0.16	20	11	1.008	0.816	0.823
7TGi	-	-	10821	0.960	0.768	0.737
7TO	0.25	13	566	0.720	0.800	0.576

All the cells are assessed for SNM, temperature variation, process variation, power consumption, time required for read and write operation, current ratio and area footprint. The results obtained for the different performance parameters are tabulated in Table 2.4 and 2.5. The 7TA cell is found to be the most stable cell, owing to its high HSNM, RSNM, and WM values in comparison to the other cells. The 7TGi, 7TAn, and 7TAs cells have high

HSNM but suffer with low RSNM values. The 7TA cell also has a reasonable performance for temperature and global variation. At the same time, its power consumption is also lower in comparison to the other bit cell designs in the same category. Global variation analysis for the 7TAn and 7TAs cells is not performed owing to the non-availability of process corner files for both LV_{TH} and HV_{TH} transistors.

The timing analysis demonstrates that the write time for 7TA is slower than other cells, but its read time is high owing to its differential nature. In terms of current ratio, the 7TAn cell performs the best, followed by the 7TGi cell. Whereas, in terms of area the 7TO cell is the best, with least area footprint of 0.576 μm^2.

2.3.2 Differential Ended with Isolated Read Port 7T SRAM Bit Cells

In the past few years, it is observed that the isolated read port topology is gaining popularity due to its ability to operate at lower V_{DD} [91]. Additionally, this configuration eliminates the inherent read-write conflict in a conventional cell. The most trivial method to isolate ports for a cell is to incorporate an additional read port into a conventional 6T cell.

A. Schematic Design of Differential Ended with Isolated Read Port 7T SRAM Bit Cells

Chun *et al.* [92] in 2012 reported a bit cell with this configuration. This bit cell (7TC) uses PMOS transistors as access transistors to perform the write operation. The schematic for 7TC is depicted in Fig. 2.12 (a). It reduces power dissipation for the write operation. But PMOS transistors require application of negative bias voltage which results in greater variability than NMOS transistors. Moreover, application of a negative bias requires a large charge pump which consumes a significant silicon area [93]. Thus, use of PMOS transistors as access transistors is generally avoided.

Another similar configuration was reported by researchers Liu *et al.* [55] in 2017. It has an asymmetrical 7T bit cell (7TL) with an additional read port connected at the QB node. This additional NMOS transistor is labelled N5 in the schematic shown in Fig. 2.12 (b). The additional read path eliminates the read stability problem, but this significantly reduces the drive current resulting in a poor write performance for the bit cell.

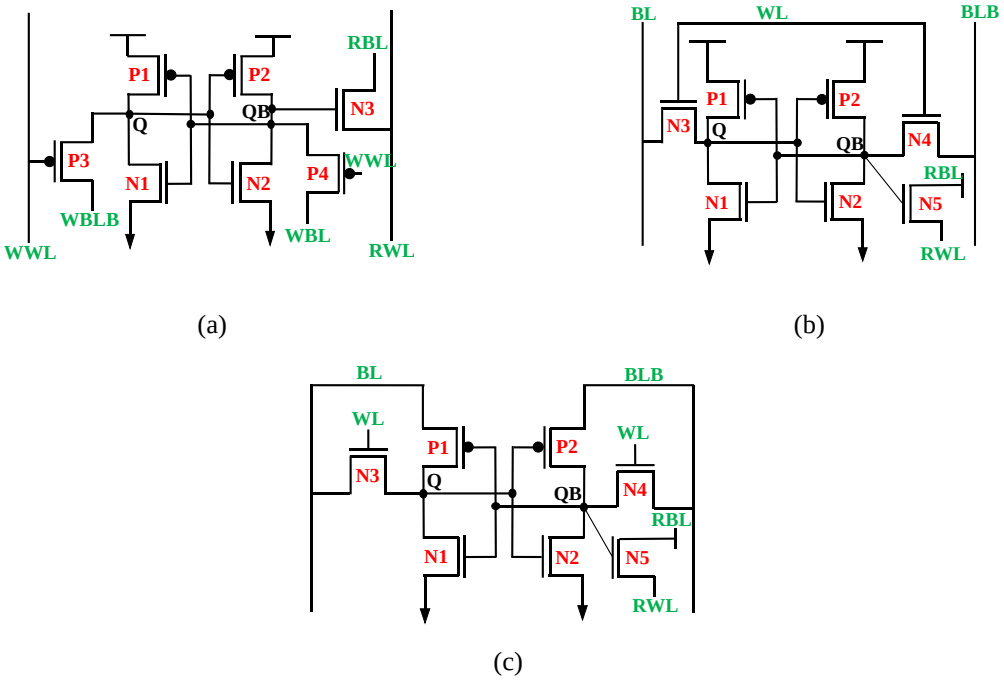
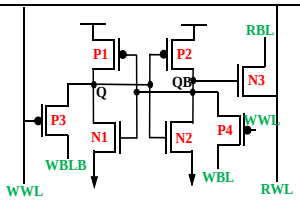
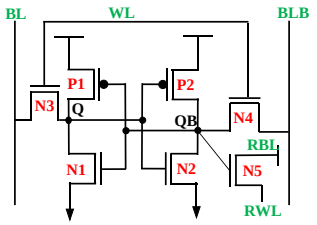
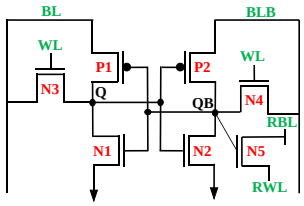


Fig. 2.12 Schematic diagram for (a) 7TC, (b) 7TL, and (c) 7TAh SRAM bit cell topologies

To rectify the shortcomings of 7TL, a modified 7T cell (7TAh) was reported by Ahmed *et al.* [54] in 2018. The schematic for 7TAh cell is illustrated in Fig 2.12 (c). The read operation is performed via an additional port formed by N5. The read operation is similar to decoupled read operation for 7TL [55, 94]. Hence, when the read operation is executed, the access transistors (N3-N4) are not operational, thereby preserving the data and ensuring read stability for bit cell. To remedy the failure in write caused by low V_{DD}, the pull up devices, (P1-P2), are driven by respective bit-lines. But at scaled V_{DD}, this may threaten the data stability of the cell. The key findings of differential ended with isolated read port cells are summarized in Table 2.6.

Table 2.6 Summarized key features of 7T SRAM bit cells with differential ended with isolated read port configuration.

S. No.	Cell Description	Schematic Design
1.	**7T-Chun *et al.* [92], 2012.** • PMOS transistor is used for access mechanism. • Requires negative bias for PMOS operation. • Consumes large area footprint.	

2.	**7T-Liu *et al.* [55], 2017.** • Isolated read port structure. • Increases power consumption. • Weakens the cell during the write operation. • Improve the read stability for the bit cell.	
3.	**7T-Ahmad *et al.* [54], 2019.** • Isolated read port improves read stability. • Modified V_{DD} assists to bolster write for low V_{DD}. • Data dependent supply collapse during write operation.	

All the aforementioned cells are designed at 32 nm technology node for performance analysis. The cells are simulated for V_{DD} of 800 mV. The results obtained for each cell with differential ended, isolated read port configuration are compared in the following sub-section.

B. Performance Analysis of Differential Ended with Isolated Read Port 7T SRAM Bit Cells

The read port for all the cells in this topology are designed to not include the data node in the read discharge current path. Therefore, the HSNM, and RSNM values for the three cells are the same. The WM value for the 7TL cell is more balanced than 7TC, while the 7TAh cell has dual pulse write operation. In terms of temperature and global variation analysis the 7TC cell has better performance for former and 7TL is good in latter. The hold and read power for 7TL is low, while in terms of write power, the 7TAh cell is the best.

Table 2.7 Results obtained for SNM, temperature variation analysis, global variation analysis and power consumption for the differential ended with isolated read port 7T SRAM bit cells.

Bit Cells	**Stability Analysis (mV)**			**Temperature Variation (mV/ºC)**			**Global Variation (mV)**			**Power Consumption (pW), (µW), (µW)**		
	Hold	**Read**	**Write**	**Hold**	**Read**	**Write**	**Hold**	**Read**	**Write**	**Hold**	**Read**	**Write**
7TC	310	310	340	0.275	0.275	0.34	55	55	82	865	36	3.6
7TL	310	310	390	0.3	0.3	0.275	42.5	42.5	79	846	30	1.76
7TAh	310	310	-	0.275	0.275	-	110	32.4	-	1128	30	0.24

Table 2.8 Results obtained for timing, current ratio, and area footprint for the differential ended with isolated read port 7T SRAM bit cells.

Bit Cells	Timing Analysis		Current Ratio	Area Analysis		
	Write (ns)	Read (ps)		Length (µm)	Width (µm)	Area (µm^2)
7TC	0.3	9	5.7	0.88	0.832	0.73216
7TL	0.22	10	3800	0.704	0.8	0.5632
7TAh	0.3	18	9.72	1.072	0.656	0.703232

The results discussed above are tabulated in Table 2.7. While the results for timing analysis, current ratio, and area footprint are tabulated in Table 2.8. In terms of time required to execute an operation, the 7TL cell is best, write time of 0.22 ns, while 7TC is better at read with 9 ps. But the 7TL cell has an edge in terms of current ratio and area with values of 3800, and 0.5632 µm^2, respectively. The 7TC cell suffers the most in terms of area footprint, with highest layout area of 0.732 µm^2.

2.3.3 Single Ended, Dual Port 7T SRAM Bit Cells

As the demand for portable devices has exploded, the need for circuits having ultra-low power consumption has taken the center stage. The two major alternatives for power reduction are 1) lowering V_{DD}, and 2) reducing the activity factor. Reduction in the activity factor of the cell can be achieved via reduction in the number of bitlines. Consequently, the most obvious method after isolating the read port is to use a single ended approach for the write operation. This topology has multi fold advantages – 1) the read-write isolation helps eliminate the conflicting design requirement inherent to bit cell, 2) reduction in silicon overhead, thereby reduction in cost and 3) divided word and bit line reduces the wire delay [80].

A. Schematic Design for Single Ended, Dual Port 7T SRAM Bit Cells

In 2008, Tawfik and Kursun [95] reported a dual V_{TH} SRAM bit cell (7TT). The transistor level schematic for 7TT is illustrated in Fig. 2.13 (a). The memory core is formed by a combination of three HV_{TH} and an LV_{TH} MOS. The information pertaining to the nature of MOS used is given in Table 2.2 This cell has two mutually exclusive controls signals to control the read and write operation. The read port of the bit cell is formed by stacked transistor, N4-N5.

Another 7T cell (7TS) with the similar topology as 7TT was reported by Suzuki *et al.* [96] in 2008. The transistor level schematic diagram for 7TS is depicted in Fig 2.13 (b). A major flaw with this design is maintaining a strong write ability for '1' with a pass transistor based single ended port [36]. Subsequently, to remedy the glitches, Gupta *et al.* [97] in 2017 reported 7TG as a modified version of 7TT. Dual-port architecture of the cell helps resolve the read–write conflict and enables the cell to execute the write operation in the sub-threshold region [97]. The transistor level schematic for 7TG is presented in Fig. 2.13 (c). The cell has improved write stability but registers a decrease in its read stability. Thereby, mandating the use of a read assist circuit for the cell [98].

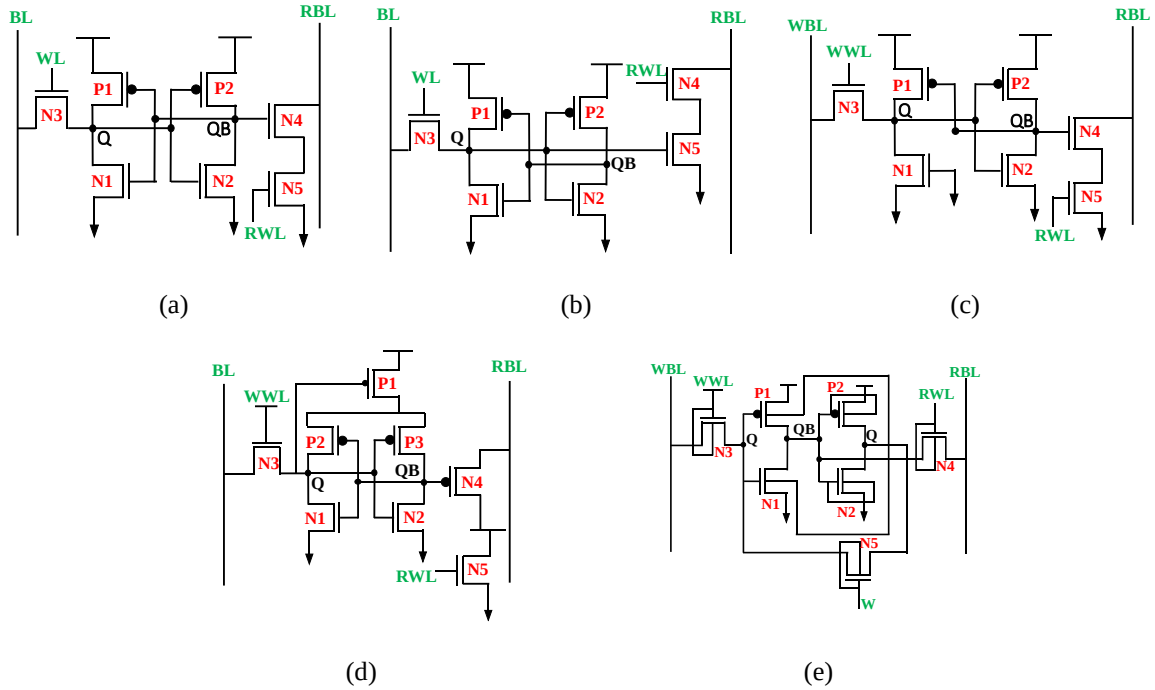
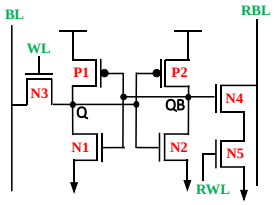
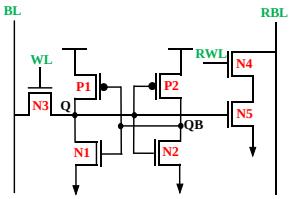
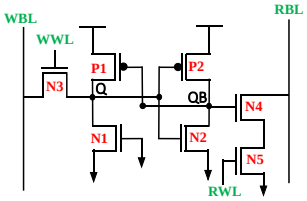
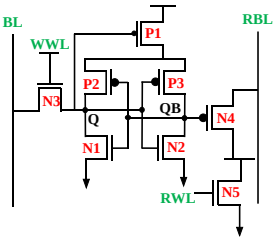
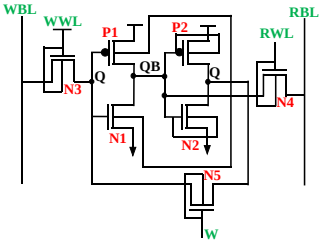


Fig. 2.13 Schematic diagram for (a) 7TT, (b) 7TS, (c) 7TG, (d) 7TR, and (e) 7TSa, SRAM bit cell topologies

Another cell (7TR), that improves dynamic power performance was reported by Roy *et al.* [99] in 2017. The transistor-based schematic for 7TR is depicted in Fig. 2.13 (d). To enhance read stability, the read path does not include either of the data nodes of the cell. A PMOS and an NMOS transistor, N4 and N5 respectively form the read port for the cell. Here N4 is connected to the bit cell memory core, but N5 is common to the entire row. PMOS is used in the read access port owing to its immunity to soft errors, and during the write operation, the supply feedback weakens the pull-up path. As an implication, the write power consumption for 7TR is diminished [100]. But, the cell has to deal with the trade-off of high silicon, due to the need of a charge pump need for a negative bias PMOS.

Using the same configuration another cell 7T was reported in 2018, (7TSa) using ST configuration by Sanapala *et al*. [53]. The transistor-based diagram for 7TSa is illustrated in Fig. 2.13 (e). It employs the second inverter to act as a body biasing circuit for the first inverter. This allows faster operations and better write ability by disconnecting the feedback connection between the inverter pair via transistor (N5) and control signal, W. A major shortcoming of the cell is that its node Q has lower strength as compared to QB. The key findings of differential ended with isolated read port cells are summarized in Table 2.9.

Table 2.9 Summarized key features of 7T SRAM bit cells with single ended, dual port configuration.

S. No.	Cell Description	Schematic Design
1.	**7T-Tawfik *et al.* [95], 2008.** • Isolated read port enhances the read stability. • Increases power consumption, but reduces leakage • Weakens the write operation for low V_{DD}.	
2.	**7T-Suzuki *et al.* [96], 2008.** • Poor write due to no assist circuit. • Stacked NMOS transistors based read port. • Low read current, reduces cell count per column.	
3.	**7T-Gupta *et al.* [97], 2017.** • N1 is always biased in cutoff region. • V_{DD} assist, bolster write operation for low V_{DD} • L_{VT} NMOS makes it vulnerable to variability issues.	
4.	**7T-Roy *et al.* [99], 2017.** • Improves dynamic power performance by reducing charging/discharging events. • Read and hold noise margin are equal. • N5 is common to the entire row. • Requires a charge pump for PMOS bias.	
5.	**7T-Sanapala *et al.* [53], 2018.** • Schmitt Trigger based memory core. • Disconnects mutual feedback between inverter pair. • Low hold and read noise margins. • The layout design for the cell is complex.	

All the aforementioned cells are designed for performance analysis at 32 nm technology node. The cells are simulated for V_{DD} of 800 mV. The results obtained for each cell with single ended, dual port configuration are compared in the following sub-section.

B. Performance Analysis of Single Ended, Dual Port 7T SRAM Bit Cells

The SNM performance analysis for the cells reveals that the 7TT cells have the most balanced performance. It is closely followed by the 7TG cell. The cells with the most inferior performance are the 7TR and 7TSa cell, their HSNM, and RSNM values are fairly low, while the WM value for 7TR is high, while for 7TSa the curve collapses.

Table 2.10 Results obtained for SNM, temperature variation analysis, global variation analysis and power consumption for the single ended, dual port 7T SRAM bit cells.

Bit Cells	Stability Analysis (mV)			Temperature Variation (mV/ºC)			Global Variation (mV)			Power Consumption (pW), (µW), (µW)		
	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write
7TT	324	324	398	0.23	0.23	0.36	37	37	80	240	12	2.97
7TS	314	314	312	0.275	0.275	0.34	56	56	105	259	30	2.74
7TG	324	324	336	0.275	0.275	0.375	37	37	110	652	5	2
7TR	166	166	551	0.19	0.19	0.14	18.5	18.5	50	880	14	3.76
7TSa	84	69	-	0.17	0.17	-	43	43	-	952	3	12.96

Table 2.11 Results obtained for timing, current ratio, and area footprint for the single ended, dual port 7T SRAM bit cells.

Bit Cells	Timing Analysis		Current Ratio	Area Analysis		
	Write (ns)	Read (ps)		Length (µm)	Width (µm)	Area (μm^2)
7TT	-	-	5233	0.96	0.768	0.737
7TS	0.5	27	117470	0.944	0.8	0.755
7TG	0.2	24	6557	0.96	0.848	0.814
7TR	0.7	28	26.64	0.768	0.896	0.688
7TSa	0.4	15	197.5	0.592	0.8	0.474

The results for temperature variation analysis showcase the 7TT cell as most resilient to variation. Though, the variation results for 7TR and 7TSa are lower, but since their typical values are very low, the variation values are bound to be lower. But, they may not be used to declare them – 7TR and 7TSa, as variation resilient. In terms of power consumption also,

the 7TT cell has the best performance, closely followed by 7TS cell. All the results for SNM, temperature analysis, global variation, and power consumption for the single ended, dual port cells are tabulated in Table 2.10.

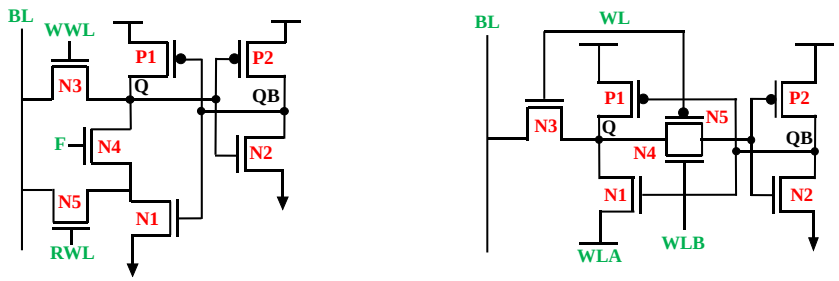
The results for the timing, current ratio, and area footprint for the cells are tabulated in Table 2.11. The best timing results - write and read, are obtained best for 7TG at 0.2 ns and 24 ps, respectively. It is closely followed by 7TSa at 0.4 ns and 15 ps for write and read, respectively. It is also the cell with the smallest area footprint of 0.474 μm^2.

2.3.4 Single-Ended, Single Port 7T SRAM Bit Cells

In certain applications, the chief objective of the circuit is to decrease power and parallelism is not a priority. Then use of multi-port bit cell will only consume more area and power. In such a case the single ended, single port bit cell is more effective as, it has 1) smaller on chip area, 2) reduced activity factor, and 3) decreased circuit capacitance, thereby limiting the total power consumed by the cell.

A. Schematic Design for Single Ended, Single Port 7T SRAM Bit Cells

In 2015, a 7T cell with this configuration was presented by Kushwah *et al.* [66]. This bit cell (7TK) is dependent on single bitline (BL) and feedback disconnection to write '1' through a single NMOS pass transistor. The transistor based diagram for 7TK is given in Fig. 2.14 (a). The write wordline (WWL) controls the NMOS transistor (N3), to enable the write operation, while the NMOS transistor (N5) is used for the read operation. The two operations are mutually exclusive. The control signal, F controls NMOS (N4) and is exerted during the write operation for disconnection of the left inverter to increase the write ability. But when N4 is OFF, the Q node for the bit cell is floating and thereby increases the possibility for a write '0' error. This condition also subjects the cell to HSD.

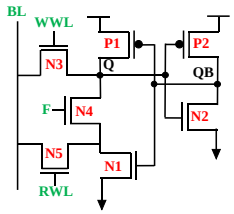
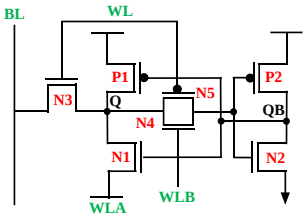


(a) (b)

Fig. 2.14 Schematic diagram for (a) 7TK, and (b) 7TY, SRAM bit cell topologies

Yet another 7T cell (7TY) with single ended, single port configuration was described by Yang *et al.* [52] in 2016. The transistor level diagram for 7TY is illustrated in Fig. 2.14 (b). The cell employs a transmission gate to disconnect node Q from input of right inverter. Transistor – N3 is used to access the memory core of the cell and four control signals navigate the cell to operate in different modes. The cell has single ended, dual pulse write operation that causes the speed of write operation to decrease. Furthermore, the utilization of multiple control signals increases the complexity of the peripheral circuitry. Resulting in power consumption and overall footprint of the cache memory to increase. The key findings of differential ended, isolated read port cells are summarized in Table 2.12.

Table 2.12 Summarized key features of 7T SRAM bit cells with single ended, single port configuration.

S. No.	Cell Description	Schematic Design
1.	**7T-Kushwah *et al.* [66], 2016.** • Stacked inverter configuration facilitates feedback disconnection to increase stability. • Prone to write '1' error as Q is floating during write operation.	
2.	**7T-Yang *et al.* [52], 2016.** • Single ended read and write operations. • Dependent on two pulses to perform the write operation. • Reduces the speed of write operation	

All the aforementioned cells are designed at 32 nm technology node for performance analysis. The cells are simulated for V_{DD} of 800 mV. The results obtained for each cell with single ended, single port configuration are compared in the following sub-section.

B. Performance Analysis of Single Ended, Single Port 7T SRAM bit cells

Both the single ended, single port cells are designed to include the data node in the read discharge path. Thus, the RSNM values for both the cells are poor. In terms of temperature variation, the 7TK cell performs better in comparison to the 7TY cell. Since the 7TY cells are designed to have a dual pulse write operation, its write mode is not compared with a cell with single ended write. In terms of power consumption, this cell is better than 7TK. All the results for SNM, temperature analysis, global variation, and power consumption for the

single ended, single port cells are tabulated in Table 2.13.

Table 2.13 Results obtained for SNM, temperature variation analysis, global variation analysis and power consumption for the single ended, single port 7T SRAM bit cells.

Bit Cells	Stability Analysis (mV)			Temperature Variation (mV/ºC)			Global Variation (mV)			Power Consumption (pW), (µW), (µW)		
	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write	Hold	Read	Write
7TK	310	138	330	0.32	0.15	0.084	194	97	279	780	1	5.6
7TY	287	89	-	0.46	0.23	-	64	64	-	196	1.68	2.14

The results for the timing, current ratio, and area footprint for the cells are tabulated in Table 2.14. The two cells – 7TK and 7TY, owing to a similar topology and read mechanism have similar current ratio values of 5818, and 5692, respectively. But the area parameter is a differentiator, as the area footprint for 7TY is significantly lower than that for 7TK cell at 0.6 and 0.798 μm^2, respectively.

Table 2.14 Results obtained for timing, current ratio, and area footprint for the single ended, single port 7T SRAM bit cells.

Bit Cells	Timing Analysis		Current Ratio	Area Analysis		
	Write (ns)	Read (ps)		Length (µm)	Width (µm)	Area (μm^2)
7TK	0.15	25	5818.2	0.96	0.832	0.7987
7TY	-	-	5691.7	0.8	0.752	0.6016

Thus, based on the aforementioned analysis it is identified that single ended, single port cells are a valid topology for lowing power consumption. But, for enhanced read stability, it is essential to ensure that the read discharge current does not pass through the data node for the cell.

2.4 COMPARATIVE ANALYSIS OF DIFFERENT SENSE AMPLIFIER TOPOLOGIES

The read operation for cell is dependent on an essential memory peripheral circuit - SA. As cells have evolved over the years, different SA topologies have been reported in literature. These different topologies can be pre-dominantly categorized as voltage based or current based SAs. Amongst the two SA topologies the voltage based SA has low transistor count, and low power consumption. While, the current mode SA is quickly able to amplify a small

differential signal at the bitlines to a full swing voltage output [20-21]. But, its higher transistor count and larger area occupancy makes it economically unfeasible. Therefore, owing to its area efficiency, voltage mode SA are more popular. Other merits that add to the qualities of voltage mode SA are high speed sensing mechanism and low power consumption [22-23]. Another mechanism, for categorization for SA is based on the number of input lines – differential ended SA and single ended SA. Thus, the two topologies are discussed below for a detailed understanding of the two topologies.

2.4.1 Differential Ended Sense Amplifier Topologies

The differential SA circuit is solely responsible for detection of a small differential signal on the bitline, to yield a full swing signal at the output [16]. The performance of an SA is highly critical for an SRAM as it determines the minimum operating point, operational frequency, and power consumption for an SRAM based memory [101]. Conventionally, the most important performance metric for an SA includes - sensing delay, minimum differential input voltage, and power consumption during the read operation [102]. Some of the popular SA topologies reported in literature are as follows –

A. Schematic Design for Differential Ended Sense Amplifier Topologies

The most common and conventional design for an SA (SA-1) [103-104] is depicted in Fig. 2.15 (a). The cross coupled nature of the inverter pair helps reduce the delay for the circuit. The core for the SA is accessed via transistors M5 and M6. The M7 transistor at the bottom acts as the current driver and ensures high drive current. It is enabled only after a detectable voltage difference is created between the bitlines. The essential aspect of this design is that during the evaluation phase, it decouples the input and output nodes. Therefore, it achieves higher speed, while maintaining lower energy consumption. But a major limitation for this topology is the use of pass-gate transistors that reduces the available input voltage, thereby poorly impacting its noise margin [23].

An alternative SA (SA-2) that removes the pass transistor gate from the input node was reported in [105]. The optimal functioning of this SA is dependent on the positive feedback of the cross coupled inverter pair. The schematic diagram for SA-2 is depicted in Fig. 2.15 (b). This topology is differential in nature and therefore, depending on the polarity of input differential voltage, the output is determined. The disadvantage of this topology is that input

and output node are the same, therefore it cannot be directly connected to the memory bitlines. If it is directly connected, the delay and power for the circuit will increase significantly. It may also poorly impact the stability of the cells connected to the SA.

An alternative to isolate the input and output nodes for a SA topology (SA-3) was reported in [106]. The schematic diagram for SA-3 is presented in Fig. 2.15 (c). In this SA, the sensing operation begins by turning the M7 transistor ON. The utility of M8 and M9 transistor is to maintain the BL and BLB at equal potential. This also forces the output nodes of SA-3 to equal potential. As its sensing node impedance is very small, the read discharge current from the memory can be directly injected into the SA [107]. It has demonstrated commendable performance for higher values of V_{DD}. But, as V_{DD} is decreasing, its performance is declining.

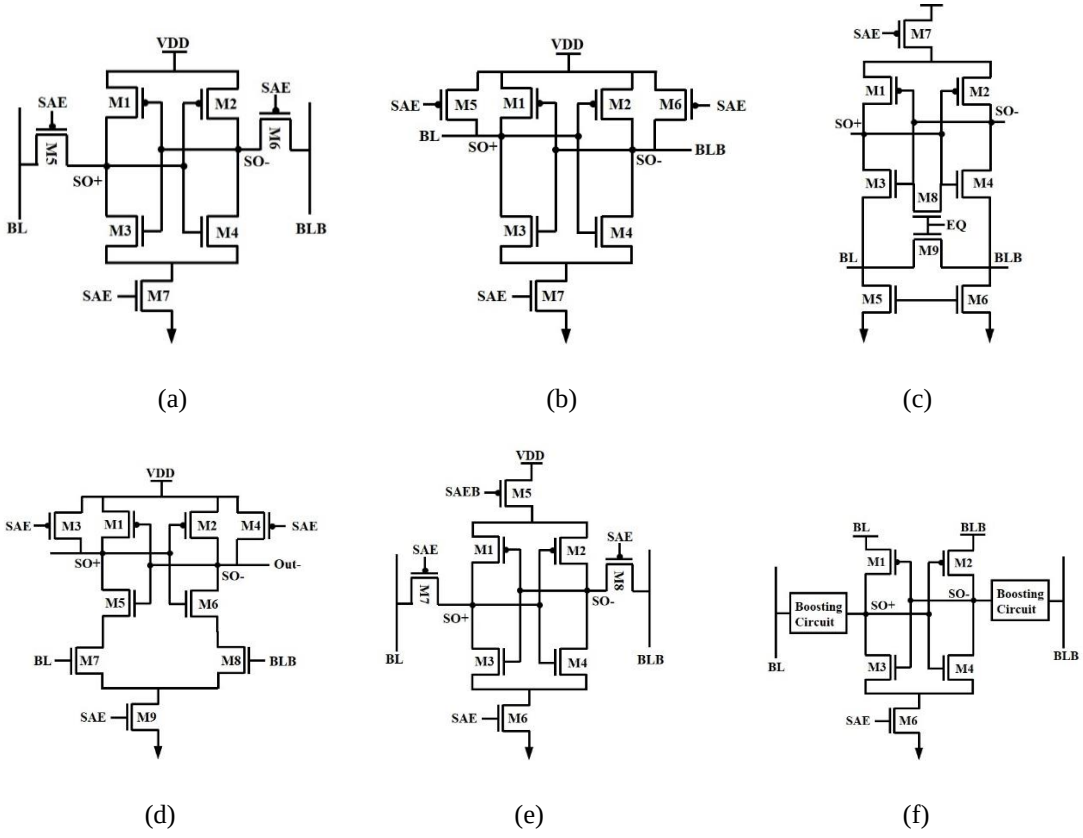


Fig. 2.15 Schematic diagram for (a) SA-1, (b) SA-2, (c) SA-3, (d) SA-4, (e) SA-5, and (f) SA-6.

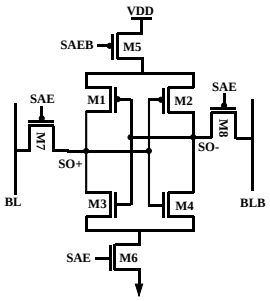
Another SA topology (SA-4) that isolates the input and output node was reported by Kobayashi *et al.* [108]. The schematic diagram for SA-4 is depicted in Fig. 2.15 (d). It combines the strong positive feedback of cross-coupled inverter pair with high resistive input. Therefore, this SA does not require decoupling at its input [109-111]. The enable

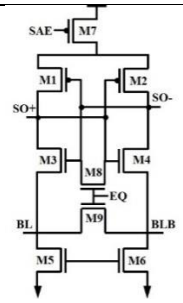
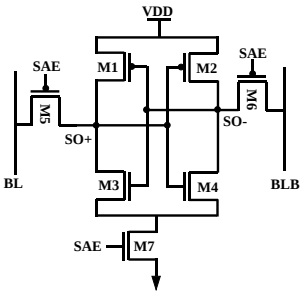
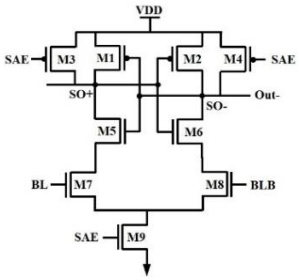
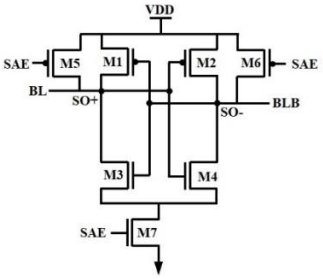
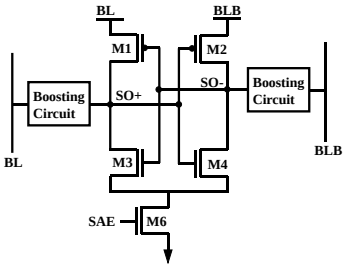
signal starts the operation by activating M7. Immediately, current begins to flow and pulls down the source terminal of M5 and M6. Successively, the input transistor pair M5, M6 starts to discharge the cross-coupled invertors. When the output voltage reaches V_{DD}-V_{TH} level, strong positive feedback enhances the output voltage difference.

A similar SA topology (SA-5) was reported in [112] and is depicted in Fig. 2.15 (e). It uses two sleep transistors to lower static power dissipation. Initially, the SAE signal is low and the PMOS transistors are ON and the differential input voltage gets transferred to the internal nodes of the SA. Then, the SAE signal is turned high, and the access transistors are cut off, thereby activating SA-5. Only when the SAE signal is high, the V_{DD} and the ground rail are connected with the inner core of the topology, thereby enabling it to function correctly. This also ensures that SA-5 works only when it's required and does not detect each time a voltage difference is generated on the bitline pair.

Another SA topology (SA-6) was reported by Patel *et al*. [113] in 2018. The schematic diagram for SA-6 is depicted in Fig. 2.15 (f). Apart from using the boosting circuit to improve the performance of the SA, the other fundamental difference between SA-1 and SA-6 is that of V_{DD}. SA-1 is driven using V_{DD}, while the pull up network of the inverter core for SA-6 circuit is designed with a bitline based supply. SA-2 was initially designed for 65 nm technology node. Lowering the technology node poorly impacts its performance. But the aspect ratio for the circuit is maintained to not bias it unfairly. The output swing and delay performance for the SA-6 is fairly good, but its major drawback is the increased area footprint, that makes it economically unfeasible. The key learning based on the review of the differential ended SA topologies are summarized in Table 2.15.

Table 2.15 Summarized key features of differential ended sense amplifier topologies.

S. No.	Sense Amplifier	Schematic for the sense amplifier
1.	**Sasaki *et al.* [112], 1990.** • Double Tail topology. • Isolates input and output node via pass transistor. • Voltage mode latch type SA. • Low leakage power dissipation.	

2.	**Blalock and Jaeger [106], 1991.** • M8 and M9 perform equalization, force bitlines and outputs to same voltage. • Inverter core acts as a high gain positive feedback. • Current based operation. • High power consumption by the circuit.	
3.	**Seki *et al.* [104], 1993.** • The cross coupled inverter core senses the data. • The bitlines are decoupled from output using pass transistor M5 and M6. • High speed, low energy operation. • SAE signal is high only for read operation.	
4.	**Kobayashi *et al.* [108], 1993.** • Doesn't require decoupling circuit. • SAE signal activates the circuit. • M9 transistor determines the sensing current. • Strong positive feedback enhances performance. • Improves the drive current and read time.	
5.	**Hill and Lachman [105], 2001.** • Removes the pass transistor from input terminal. • M5 and M6 are OFF during read operation. • M7 increases drive current. • Input and output at the same terminal.	
6.	**Patel *et al.* [113], 2018** • Uses boosting circuit is added to improve performance. • Isolates input and output node. • The supply is bitline based, this helps save power.	

The aforementioned differential SAs are designed at 32 nm for performance analysis. The cells are simulated for V_{DD} of 1 V. The results obtained for the SA topologies are compared in the following sub-section.

B. Performance Analysis for Differential Ended Sense Amplifier Topologies

The most important aspect for an SA is the ON and OFF current for the topology. In general, higher ON current ensures faster operation, whereas the OFF current is required to be as low as possible. The lower the OFF current, the lower is the leakage power, and higher are the chances of not registering a false read operation. The ON and OFF current values obtained for the pre-existing SA topologies are compared in Fig. 2.16 (a), and (b) respectively.

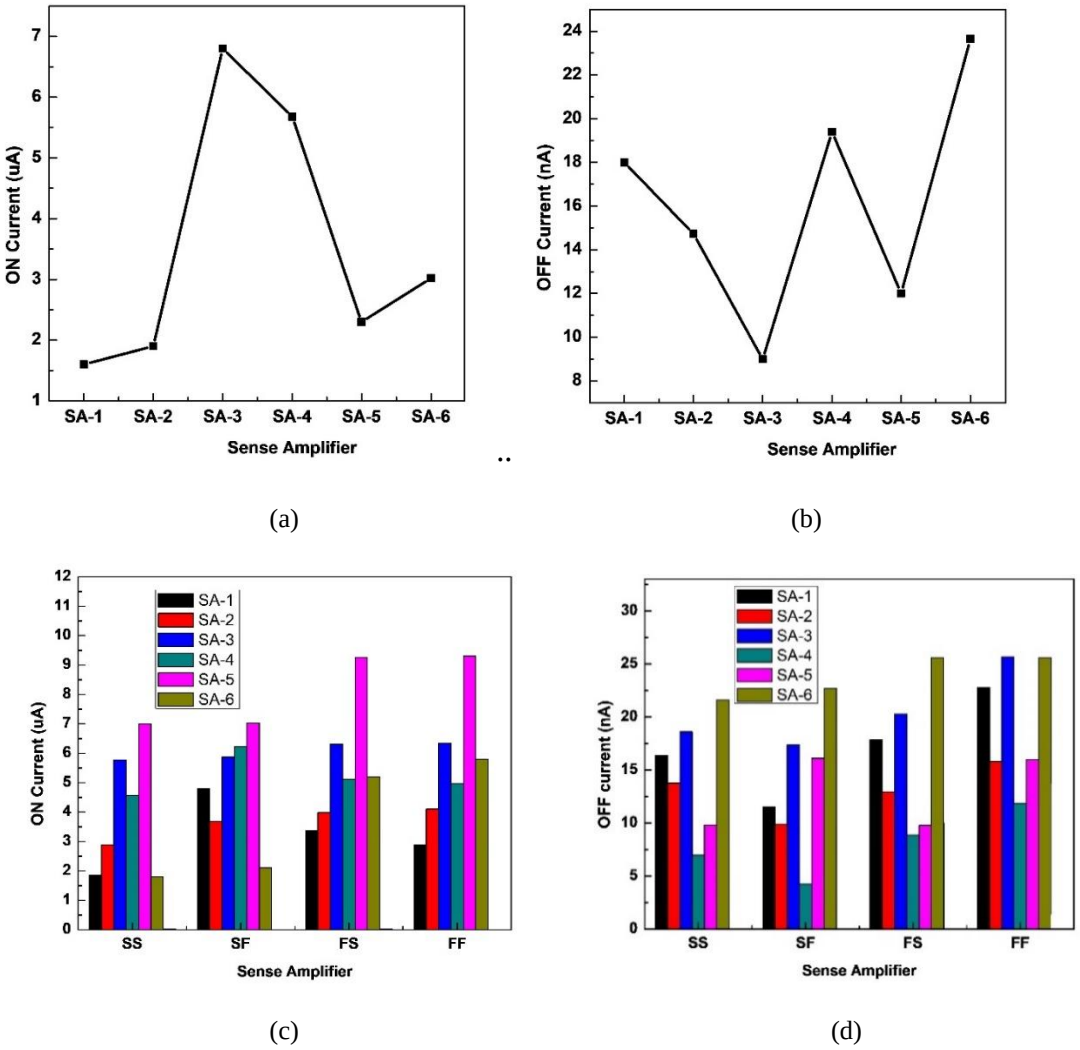


Fig. 2.16 Graphical comparison for (a) ON current, (b) OFF current, (c) ON current at different process corners and (d) OFF current at different process corners for all SAs at different process corners.

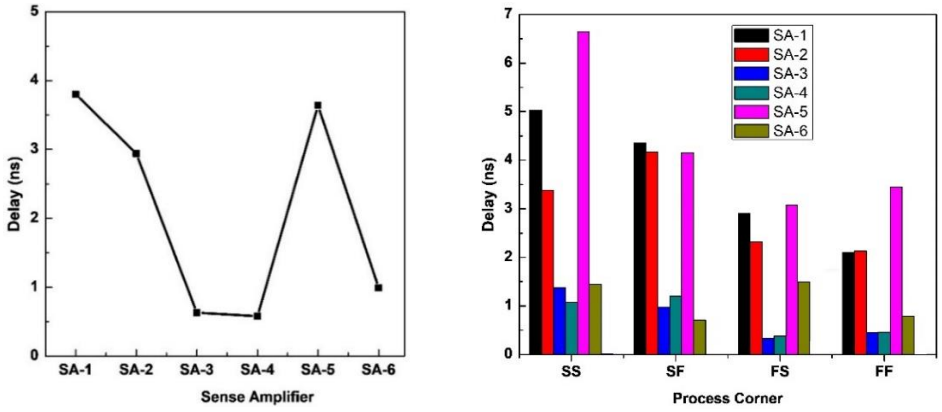
The highest ON current amongst the different SAs is obtained for SA-3 at 6.8 uA, closely followed by SA-4 at 5.68 uA. Whereas, in terms of OFF current, the lowest value is obtained for SA-3 at 9 nA, closely followed by SA-5 at 12 nA. Another SA topology that has low OFF current value is SA-5 at 12 nA. Therefore, in terms of ON and OFF current the SA-3

has the best performance. The SA-3 topology has an edge over the other SA topologies because the former is current based.

When a circuit is fabricated, there are possibilities of variation in performance of the circuit due to fabrication imperfections [114]. Therefore, the ON and OFF current performance for all the SA topologies are also calculated for the different process corners (slow-slow (SS), slow-fast (SF), fast-slow (FS), and fast-fast (FF)) and compared in Fig. 2.16 (c) and (d) respectively. This is done to ensure that the variation (calculated as the difference between the maximum and minimum current values) in the performance of the SA is within bounds.

The variation in performance of SA-1, SA-2, SA-3, SA-4, SA-5, and SA-6 are 2.95, 1.21, 0.56, 1.65, 2.3, and 4 µA, respectively. It can be inferred from the aforementioned data that the current based SAs - SA-3 and SA-4 are more resilient to process variation than voltage mode SAs. Whereas, for the OFF current values, the variation in SA-1, SA-2, SA-3, SA-4, SA-5, and SA-6 are 11.2, 5.9, 8.3, 7.6, 6.3, and 4 nA, respectively.

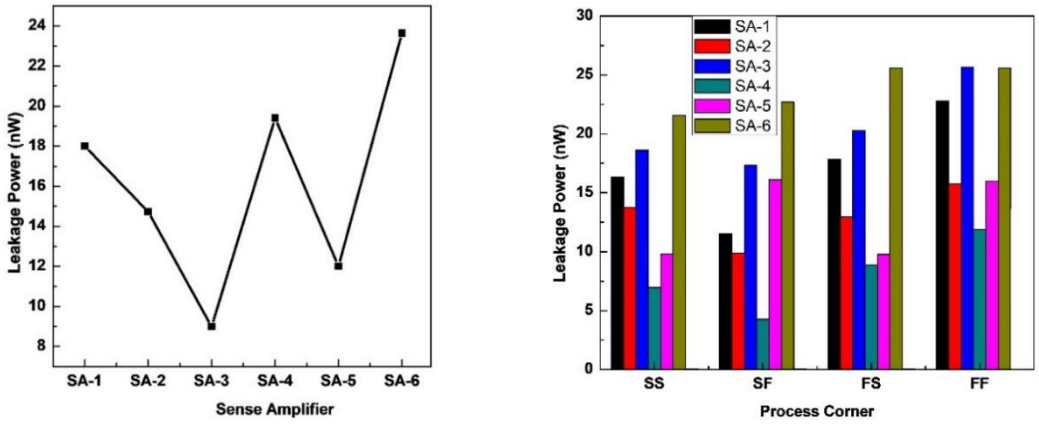
The delay recorded for the other SA topologies – SA-1, SA-2, SA-3, SA-4, SA-5, and SA-6 is 3.8, 2.94, 0.63, 0.58, 3.64, and 0.99 ns, respectively. Delay for an SA should be as minimum as possible. This increases the operating speed for the memory. The delay performance for all SA designs topologies is compared in Fig.2.17 (a). The performance for each digital circuit is subject to variation due to global variations caused during the circuit fabrication. Consequentially, the delay performance of all the pre-existing SAs at process corners is analyzed and compared in Fig. 2.17 (b).



(a) (b)

Fig. 2.17 Graphical comparison for sensing delay (a) at TT corner, and (b) all process corners for the different SA topologies.

The best performance amongst all the corners is obtained at the FS corners; here the performance for the PMOS is fast while the NMOS is made slower. This results in bridging the gap between the mobility difference for PMOS and NMOS, thereby improving the performance for the SA at FS corner. A general observation, from the figure is that worst performance for all the SAs is observed at the SS corner, due to poor performance for both PMOS and NMOS transistors. Whereas, the best performance for all SAs is observed at FS corner, as the performance parity between NMOS and PMOS is bridged at this corner.



(a) (b)

Fig. 2.18 Graphical comparison for leakage power at (a) TT corner and (b) all process corners for the different sense amplifier topologies.

An SA is dependent on high amplification of small deflection in the input voltage, consequently, it is expected that the ON and OFF current for the SA will have a significant difference. But, at scaled technology node, maintaining low leakage current is a challenge. Typically, the leakage current for a latch based SA topology is low. The leakage power values obtained for all the SAs at typical corner and all process corners are compared in Fig. 2.18 (a) and (b), respectively. The SA topology with the highest leakage power dissipation is SA-6 at 23.64 nW. The high value of leakage power dissipation for the SA-6 topology is caused by the additional boosting circuitry that adds to the leakage current sources in the circuit. The lowest leakage power is observed for SA-3 at 9 nW. While the leakage power values of the other SA topologies – SA-1, SA-2, SA-4, and SA-5 are 18, 14.73, 19.4, and 12 nW respectively.

Based on the review of the different differential ended SA topologies it was derived that (1) current drive transistor plays a crucial role in SA design, (2) it is essential to ensure global

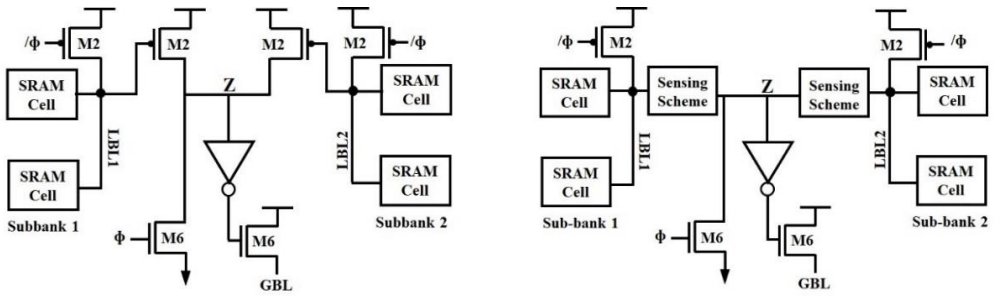
variation resilience for an SA, (3) low leakage power consumption can be achieved with the help of sleep transistors, and (4) it is essential to have an enable signal that controls the working of the SA, it ensures that minimal false read event are registered by the SA.

2.4.2 Single Ended Sense Amplifier Topologies

The convenient sensing topology deemed reliable for single ended SRAM is inverter based [115]. Thus, with the increasing popularity of single ended cell, it has become primal to investigate and design single ended SA. Conventionally, domino sensing scheme is a preferred choice [116-118] for single ended topologies, but its performance deteriorates as the number of cells per bitline increases [119]. Whereas, the pseudo differential sensing scheme is operational even when a large number of bit cells are integrated on a single bitline [120]. But its performance is limited by variability in reference voltage generation and strobe signal variations. The aforementioned problems can be resolved using techniques reported by researchers in [121-122]. But these SA topologies increase the power consumption tremendously and also cause unintentional couple between bitline and input of SA, thereby severely limiting the performance for the topology.

A. Schematic Design for Single Ended Sense Amplifier Topologies

Typically, a domino logic based circuit is composed of a static gate inserted between consecutive dynamic stages. A block diagram representation for domino based sensing scheme used for single ended read operation is depicted in Fig. 2.19 (a). The local read bitline (LBL) acts as its input. For a single-ended operation, the LBL selectively discharges (either for '1' or '0') turning ON the M2 transistor, and consequently charging node Z. As Z is high, the M6 transistor is ON thereby charging the global bitline (GBL) and completing the read sensing operation.



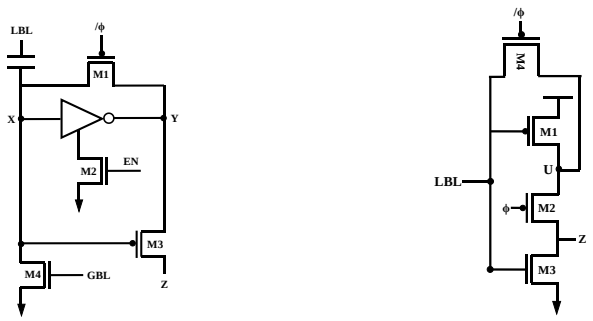
(a) (b)

Fig. 2.19 Block diagram representation for (a) domino logic based sensing, and (b) modified sensing scheme.

If a large number of cells are connected in the same column, the bitline capacitance increases drastically. This results in an extremely high delay thus, making dynamic PMOS sensing scheme not a suitable alternative for large memories. A large voltage swing is required on input bitline, to charge node Z. If the bitline capacitance is very high, the discharge time for the scheme increases, resulting in inferior performance and higher power consumption [121]. To improve the performance of the domino sensing scheme the block diagram for domino sensing scheme may be modified to replace the first PMOS transistor M2 with a dedicated sensing topology. The block diagram for the same is depicted in Fig. 2.19 (b). Two different pre-existing sensing topologies that may be utilized as the first stage for the modified domino sensing scheme are as follows.

AC Coupled Sensing Scheme

One of the topologies that has been reported for sensing scheme in Fig. 2.19 (b) is AC coupled sensing scheme (ACSS), reported in [121]. The detailed circuit diagram for ACSS is depicted in Fig. 2.20 (a). It is composed of a coupling capacitor, an inverter with a foot switch (M2), a PMOS transistor (M1) for equalization, and an output transistor M3. Additionally, an NMOS transistor (M4) is used to form the feedback connection between the GBL signal and the inverter input node X. The utility of the M2 transistor is that it enables the sensing scheme only when a particular sub-bank is selected.



(a) (b)

Fig. 2.20 Schematic diagram for (a) ACSS, and (b) SPSS topologies.

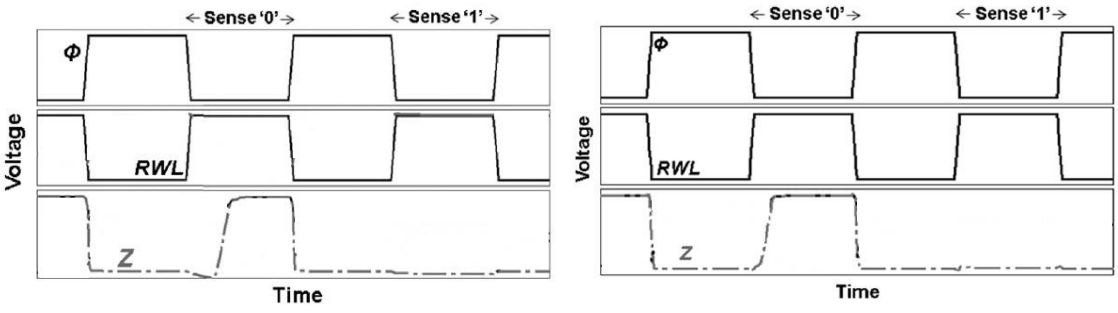
The sensing operation for the ACSS topology is a two-step process – pre-charge and evaluation. During the pre-charge phase, the enable signal ϕ is set high. Thus, transistor M1 connects the input node (X) and output node (Y). This equalization of the X and Y node biases the tri-gate inverter at the trip voltage. Additionally, the Z node is discharged to ground. Once the pre-charge step for sensing is completed the evaluation phase begins; the

ϕ signal is set low. During this phase, the read operation for the selected cell is performed.

During the read operation, the pre-charged LBL value is lowered due to read discharge current. This lowering of voltage level on LBL gets coupled with the X node. Consequently, a rapid rise in the voltage level at node Y is observed; the voltage gain for an inverter is extremely high at the trip voltage [123]. Lowering of value at node X also, turns ON the M3 PMOS transistor. Thus, the Y node is connected to the Z node via transistor M3. The output waveform for the ACSS topology is depicted in Fig. 2.21 (a). Limitations that have ill impacts on the performance of the ACSS are - firstly, biasing the inverter at the trip point results in a short circuit condition between the V_{DD} and the ground terminal. Thereby increasing its static power consumption. Second, for optimal functioning a large capacitor is required by the circuit which increases the area footprint for the circuit significantly [124].

Switching PMOS Sensing Scheme

Another circuit topology reported to be used as a replacement for the first stage dynamic PMOS SA in domino sensing scheme is the switching PMOS sensing scheme (SPSS). This scheme was reported by Jeong *et al*. 2016, the schematic diagram for the SPSS topology is depicted in Fig. 2.20 (b). The circuit comprises of a pull up PMOS transistor (M1) and a pull down NMOS transistor (M3). Two additional PMOS transistors connected in pass transistor configuration are added to the inverter; one between M1 and M3 and the other is connected between the drain of M1 and the input signal LBL.



(a) (b)

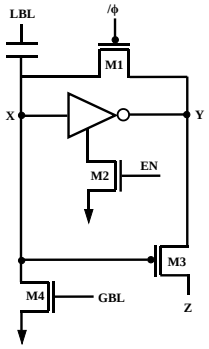
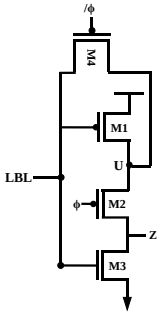
Fig. 2.21 Output waveform corresponding to (a) ACSS and (b) SPSS topologies [119].

During the pre-charge phase (ϕ = '1'), the M4 transistor is turned ON resulting in the M1 transistor in the diode connected topology. This results in LBL being pre-charged to V_{DD}-V_{TH}. In the evaluation phase (ϕ = '0'), the M4 transistor is turned OFF, and the M2 transistor is turned ON. This completes the inverter circuit, with LBL as the input and the Z node as

the output. For sensing '0' the discharge on LBL turns on transistor M4. The pre-charge level for LBL is V_{DD}-V_{TH}, only a small swing of LBL turns ON transistor M4, resulting in better performance.

The output waveform corresponding to the SPSS topology is depicted in Fig. 2.21 (b). The major limitation of the SPSS topology is its utility of large number of PMOS transistors in the circuits. The current capacity for a PMOS is lower in comparison to an equally sized NMOS transistor [123]. Therefore, due to the dominance of PMOS transistors in the SPSS topology, its performance in terms of current carrying capacity, delay and area footprint suffers. The key learning based on the review of the single ended SA topologies are summarized in Table 2.16.

Table 2.16 Summarized key features of single ended sense amplifier topologies.

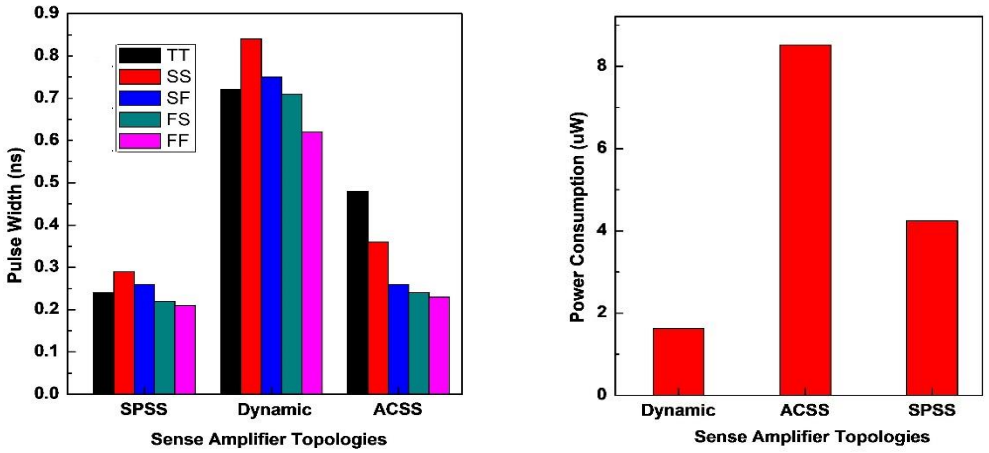
S. No.	Sense Amplifier	Schematic for the sense amplifier
1.	**Qazi *et al.* [121], 2011.** • Inverter based single ended SA topology. • M2 is used to enable the sensing scheme. • Two step sensing process – pre-charge and evaluation. • Inverter is biased at the trip voltage.	
2.	**Jeong *et al.* [119], 2016.** • Uses modified inverter topology for sensing. • Uses a PMOS switch M4. • Uses large number of PMOS. • Low drive current. • Large area footprint.	

The aforementioned single ended SAs are designed at 32 nm technology node for performance analysis. The cells are simulated for V_{DD} of 1 V. The results obtained for the SA topologies are compared in the following sub-section.

B. Performance Analysis of Single Ended Sense Amplifier Topologies

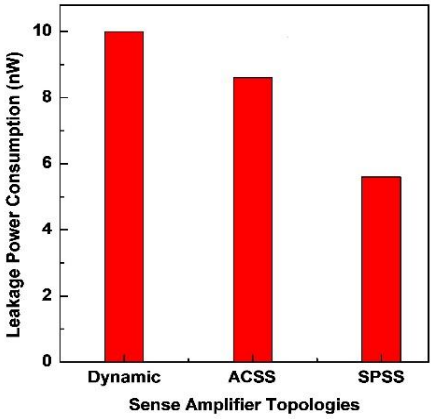
The most essential aspect for an SA topology is its timing requirement. During the read operation for single ended bit cell, the time required for flipping the output of the SA, after

the ϕ signal has been set is referred to as the read time (T_S) [119]. The sensing performance for the different SA topologies are graphically compared in Fig. 2.22 (a). The sensing performance for each SA is determined at each process corner to analyze the impact of global variation on the performance of the topology. The simulations are performed at V_{DD} of 1V.



(a)

(b)



(c)

Fig. 2.22 Comparison of (a) delay timings at different process corners, (b) average power consumption, and (c) leakage power consumption for all the SA topologies.

For all the SAs, the best performance is observed at FF corner, owing to the better performance for both NMOS and PMOS. The dynamic PMOS based SA topology has the most inferior performance in comparison to others. The best performing pre-existing SA topology in terms of delay is SPSS with delay of 0.4 ns.

Power consumption is an essential performance parameter for circuits. Thus next, the different single ended SA topologies are compared for average power consumption. The results obtained for average power consumption for each SA are compared in Fig. 2.22 (b).

The average power consumption for the ACSS topology is the highest amongst others. Its average power consumption is 34.27, and 43.06 % greater than dynamic PMOS, and SPSS, respectively. The higher power consumption of the ACSS is an implication of biasing the first-stage inverter to an intermediate voltage during pre-charge mode, resulting in a short circuit current to flow through the circuit. Whereas, the SPSS topology is able to evade this problem with the help of a switching PMOS transistor.

Therefore, the average power consumption for the two topologies is drastically lower than the ACSS topology. When the read operation is not being performed, the SA is disabled. During this disabled stated the power consumption by the SA topology is referred to as its leakage power consumption. It is calculated as the product of leakage current in the circuit and V_{DD}. The leakage power consumption values obtained for the different SA topologies are graphically compared in Fig. 2.22 (c). Amongst the pre-existing SA topologies, the best performance is demonstrated by SPSS topology; its leakage power consumption is 5.6 nW. While the highest leakage power consumption is by dynamic PMOS design.

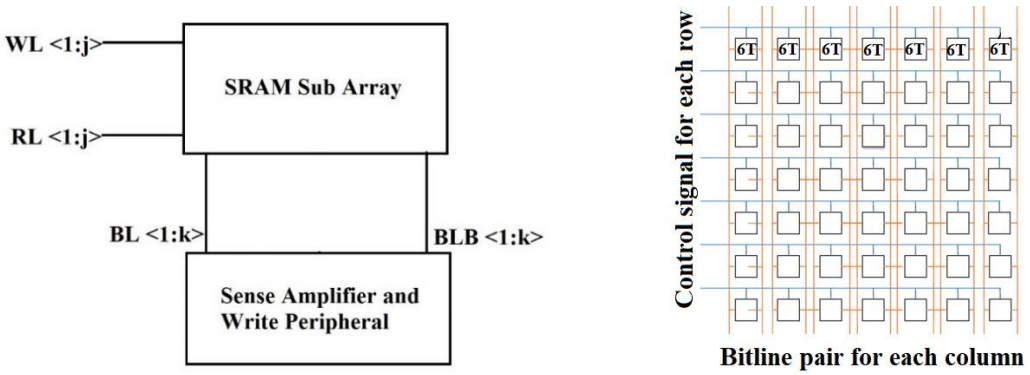
2.5 COMPARISON OF DIFFERENT SRAM ARRAY DESIGNS

An SRAM bit cell is a small peg in the matrix of the SRAM array. When a bit cell is to be accessed to perform read or write operation all the cells that share wordline (in the same row) and bitlines (in the same column) with the selected cell, get half selected (HS). Therefore, the read and write current through the bitlines is not only dependent on the selected bit cell but, also the other cells in the array. A block diagram representation for an array configuration and arrangement of cells in array is depicted in Fig. 2.23 (a) and (b), respectively. So, to develop a comprehensive understanding of array topology, it is essential to understand the existing array models in literature. Some of the array based papers are briefly summarized as follows -

When a bit cell is integrated in an array, it is essential to determine their failure probability, and their working under the influence of the others. To estimate failure probability Mukhopadhyay *et al*. [125] in 2005 used a mathematical model to estimate the failure probabilities for a bit cell when positioned in an array. It also utilizes a statistical model to determine the maximum access time a cell will require based on the number of cells in a given row and column. Based on mathematical models and their analysis a modified array

model is suggested to improve yield for the cell.

In another approach, Chang *et al*. [126] in 2011 reported a mechanism to integrate different bit cells to form an array. In this paper, the researchers have used 6T and 8T bit cells to design the array configuration. In memory information is stored in words (collection of bits). The higher order bits are of greater importance than the lower order bits. Thus, the researchers have proposed designing the higher order bits for the array using 8T cells and lower order bits using the 6T cells. This mechanism for array design has helped lower the power consumption and also the area for the memory. Another aspect that is emphasized on error tolerance enabled by different SRAM configurations when arranged in an array.



(a) (b)

Fig. 2.23 Block diagram representation of (a) array for an SRAM memory, and (b) arrangement of cell in an array.

Another group of researchers in [127] reported a mathematical model for calculation of energy consumption for an array configurations. For a defined memory size, the optimum rows to column configuration can be determined using the energy model for the array. In this paper, the cells utilized for SRAM energy models are used to optimally design the array configuration for an 8T based array. On the basis of the energy model and its calculation results, it is recommended that an array may be divided into sub-arrays for improvement in performance. It also compares the performance of an array for varying sizes.

In 2015, Pasandi *et al*. [128] reported a 9T cell that is designed to improve the read and write performance of the bit cell. The cell design is optimized to have high current ratio, thereby enabling integration of large number of bit cells in a column of the array. The design of the cell allows integration of 1k cells per column for its array configuration. In another paper by

Ahsan *et al*. [129], a cascaded inter configuration is reported for boosting performance for the array. Additionally, to uplift the performance, a three transistor inverter enables the array formation for the modified inverter design. The highlight of the design is that it enables V_{DD} reduction to 300 mV.

A completely different array approach is reported by Pasandi *et al*. [130], in 2019. A hybrid assignment technique is reported in the paper for designing an array. It pre-dominantly uses multi-threshold devices to design and improve the performance of the array configuration. The central idea behind this approach is to design higher order bits using high performance transistors and lower order bits using low performance transistors. This helps in lowering the power consumption for the array design. But, introduces layout and fabrication difficulties for the array. The key points for the review of different array design techniques and configuration are summarized in Table 2.17.

Table 2.17 Summarized key point based on array analysis.

S. No.	Reference	Key Points
1.	**Mukhopadhyay *et al*. [125], 2005**	• Uses mathematical model to estimate the failure probabilities for a bit cell when positioned in an array. • Uses statistical models to determine maximum access time based on the number of cells in a given row and column. • Based on the power and leakage performance results, it suggests an array model for improving the yield.
2.	**Chang *et al*. [126], 2011.**	• Reports a mechanism to integrate different SRAM bit cells to form an array. • Improves the power performance. • Integrating 6T and 8T cells makes the layout compact and area efficient. • Emphasizes on error tolerance enabled by different SRAM configurations when arranged in an array.
3.	**Garg, and Kim [127], 2013.**	• SRAM energy models are used to optimally design the array configuration for an 8T based array. • Division of array into sub-array is recommended to improve performance. • It also compares the performance of an array for varying sizes.

4.	**Pasandi *et al*. [128], 2015**	• A 9T cell is reported that improves read and write performance. • It is optimized to have a high on/off current ratio, enabling large number of bit cells per column. • Optimal performance is reported for 1k cells per column. • Low area footprint because of minimally sized transistors.
5.	**Ahsan *et al*. [129], 2015**	• Reports a cascaded inverter configuration to boost performance. • A three transistor inverter enables formation of an array model suited for the modified inverter configuration. • This new array model is able to reduce the V_{DD} upto 0.3V.
6.	**Pasandi *et al.* [130], 2019.**	• A hybrid assignment technique is used to design SRAM array • Cells designed using multi-V_{TH} devices are employed to design the array for improved performance. • Emphasizes on the need for high performance MSB cells and low performance LSB cells to optimize power performance.

Based on the detailed review of the different bit cells, their configurations, SA topologies, and array designs the following technical gaps are identified. These technical gaps form the basis of the research work proposed in this thesis.

2.6 TECHNICAL GAPS

The declining technology node has increased variability issues in design of an SRAM bit cell. Additionally, to reduce the total power consumption for a bit cell, the scaling of V_{DD} has resulted in an increased vulnerability of the cell towards DC noise. SRAM memories tend to be large, fast and power hungry. If the power consumption for the cell is reduced by lowering the V_{DD}, this decreases the operational speed for the cell.

Conventionally, bit cells are designed to operate in a single mode, thereby restricting the cell to operate with fixed parameters. Thereby, leaving very few design variables for the programmers. But most applications require memory to be at its best performance only when it is being accessed, otherwise it may operate in power saving mode.

A current mode SA has high drive current and fast operation. But to achieve the same, they consume high power and have large area footprint. The voltage based SA is operational at low voltage and is also area efficient. But its operation is slow, and the drive current is also low. Also, with the increasing dependence on single ended cells, it is essential to design SA

that is compatible with single ended cells.

When an SRAM bit cell is integrated in an array, its performance is dependent on the neighboring cells and also the cell itself. These interactions may result in HS issues. The other vulnerabilities that a cell may encounter when incorporated into an array are bit error, soft error and multi-bit error. These error vulnerabilities increase -with declining technology node and scaled V_{DD}.

CHAPTER – 3

A PROCESS VARIATION RESILIENT SINGLE ENDED, SINGLE PORT 7T SRAM CELL

The simplest and the most crucial component for a memory is the bit cell. The 6T cell was the industry standard for a very long duration, but with the decreasing technology node and scaling V_{DD}, its performance is deteriorating. The literature review has helped identify 7T cell as a potential successor as it has low power consumption, and high area density. But, with lowering V_{DD}, and decreasing technology node, there is need to design a 7T cell that is operational at lower V_{DD}, has improved stability margins, and is resilient to PVT variations. The following objective is framed to accommodate the aforementioned need –

"Design and analysis of an area efficient, low power 7T SRAM bit cell at 32 nm technology node, resilient to process variation."

Methodology used to achieve the desired objective in the chapter is as follows –

- Design a single ended 7T SRAM and its modifications using different port topologies and multi-threshold transistors.
- Compare the performance of different proposed cell topologies to identify the best design.
- Validate the performance of the best identified cell against the pre-existing cells.
- Analyze the proposed 7T SRAM cell for process variation against other pre-existing cells.

In this chapter, four different 7T cells are proposed, and their performance is analyzed. All the proposed cells are single ended, single port in nature. This particular configuration is chosen for its power saving properties and low area footprint. The chapter is organized into the following sections. The first section is dedicated to introduction, section 3.1. In section 3.2, the different 7T bit cell are explained, and their performance is elaborated upon. Thereafter in section 3.3, the performance for the proposed 7T bit cells are compared to identify the best performing bit cell. Whereas, in section 3.4, the performance of the best performing 7T bit cell is compared against the different pre-existing bit cell topologies. Finally, the important findings of the chapter are summarized in section 3.5.

3.1 INTRODUCTION

The growing popularity of Internet of Things has increased the processing load of microprocessors present on System on Chip (SoC). Cache memory formed by an array of bit cells is a major part of SoC. SRAM cells are reported to consume about 30% of power in any embedded system [30]. The major components of power consumption for an bit cell are static and dynamic power consumption. Static power consumption linearly depends on V_{DD}; whereas dynamic power shows a quadratic dependence on V_{DD}.

The growing popularity of sleek designs with longer battery life has forced the industry to shift towards nanometer feature size to cater to the needs of the consumer. In addition, the feature size of highly integrated nano-electronic devices is being continually reduced in keeping with Moore's Law in nanotechnology [40]. To appease the demand for higher battery life, it has become primal to reduce the power consumption of the bit cell. The most obvious method to reduce power consumption is to decrease the operational V_{DD}. But the PVT variations in deep sub micrometer region limits the reduction in V_{DD} [33].

Also, with the downscaling of V_{DD}, standby power starts to dominate active power [131]. Static power consumption makes up a major part of total power consumption for an bit cell as it operates mostly in hold mode. There is a limitation in reducing the V_{DD} as it slows down the memory operation that too with a significant increase in the bit error rate (BER) [45]. Thus, designing high-performance digital circuits with V_{DD} in the range of saturation voltage of a MOS transistor is a real challenge for designers [132, 48].

As V_{DD} decreases, the $V_{DD} - V_{TH}$ factor gets diminished, it further leads to reduction in the frequency by several orders [48]. The implication of the former is that, though there is a reduction in the total power consumption for the circuit, the leakage power consumption per instruction increases [46]. The different reasons for degradation in the transistor performance also include - geometry defects, oxide breakdown, electro migration, hot carrier injection, DIBL and ESD [133, 42]. A cell attains optimum functionality and least power consumption near the sub-threshold region [48].

Nevertheless, operating the bit cell in the sub-threshold region is also challenging. In this region, intra-die process variations such as random dopant fluctuation and line edge roughness greatly impact V_{TH} mismatch. These process variations lead to degradation in the

memory performances as adjacent bit cell may produce asymmetrical characteristics [12]. The collective effect of the aforementioned aspects has led to increased instances of failure during read, write, and hold operations. Thus, it has been predicted that embedded cache memories, which are formed by bit cells will be more prone to such failures [125]. To remedy the abovementioned shortcomings, various bit cells have been proposed over the years.

3.2 PROPOSED SINGLE ENDED, SINGLE PORT CELL DESIGNS

The literature review for the different bit cells presented in chapter 2 has helped identify the 7T bit cell as the most suitable successor for the conventional 6T bit cell. This inference is based on the fact that the 7T cell has a low area footprint and at the same time has performance that is highly improved in comparison to the 6T cell designed at lower technology node. Additionally, it was identified that differential ended cells consume more power and are also more vulnerable to the inherent read-write conflict. Thus, in this chapter, the prime focus is on designing a single ended 7T bit cell with single port configuration.

During the literature review, it was also identified that various researchers had used multi-V_{TH} devices to design their cells. Therefore, the proposed cell also includes a high performance transistor to design the proposed 7T cell. In this chapter, different 7T bit cell configurations are designed to identify its best possible configuration. The different single ended single port 7T bit cells using one or more high performance transistors are as follows –

3.2.1 Schematic Design for Proposed 7TP1, 7TP2, 7TP3 and 7TP4 SRAM Bit Cells

Four seven transistor bit cell with single bitline architecture are proposed. Inverter pairs; inv_1 (P1-N2) and inv_2 (P2-N2) are used as the memory core of the cell. An additional NMOS (N5) transistor is placed between the node QB and Q1 for connection and disconnection of the feedback between inv_2 and inv_1. The N5 is controlled by the control signal wordline bar (WLB), which is low only during the write operation. Access transistors (N3 and N4) are used to access the memory of the cell for the read and write operation, respectively. The single ended read and write operation for the cell are enabled using wordline (WL) and readline (RL), respectively. The discharge path for the bit cell for the read and write operation is provided by the bitline (BL).

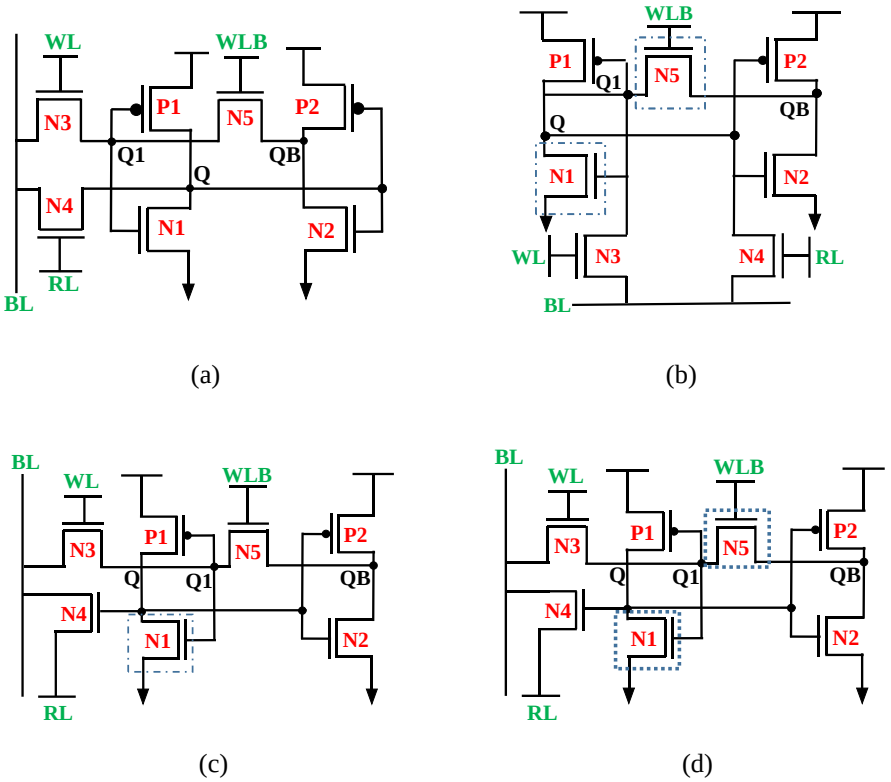


Fig. 3.1 The schematic design for (a) 7TP1, (b) 7TP2, (c) 7TP3, and (d) 7TP4 SRAM bit cell.

The first version of the proposed 7T cell (7TP1) is depicted in Fig. 3.1 (a). All transistors used in its schematic are of bulk type except N5, which is an LV_{TH} MOS. The N5 transistor is modified to improve the write performance for the cell. A modification for the 7TP1 cell is the proposed as 7TP2. The data core of the cell is similar to the 7TP1 cell, with the exception of the N5 transistor. The N5 transistor in 7TP1 cell is of conventional bulk nature, but in the 7TP2 is it LV_{TH} MOS. The transistor based circuit for 7TP2 cell is shown in Fig. 3.1 (b).

The read port for 7TP1 and 7TP2 discharges through the data node for the cell, making the cell vulnerable to read noise. Thus, two other 7T cells are proposed (7TP3 and 7TP4) with a different read port. The read port for 7TP3 and 7TP4 is designed to not include the data node in the read discharge path. Thus, the orientation for the N4 transistor is changed. The circuit diagram for 7TP3 and 7TP4 bit cell is given in Fig. 3.1 (c) and (d), respectively. The difference between 7TP3 and 7TP4 is the same as 7TP1 and 7TP2. In 7TP3 cell only N1 is LV_{TH}, and for 7TP4 both N1 and N5 transistors are of LV_{TH} MOS nature.

3.2.2 Hold, Read and Write Mechanism for Proposed Bit Cells

Each bit cell in an SRAM operates in either of the three modes of operation – hold, read, and write. The proposed four 7T cells function the same for hold and write operation. Whereas, the read operation for the 7TP1 and 7TP2 cells is the same. But it is different from the read mechanism for 7TP3 and 7TP4. The hold, read and write operation for the four bit cells are explained as follows –

A. Hold Mechanism For All Proposed 7T Bit Cells

A typical mode for a memory element is when the bit cell maintains the value stored in it. This mode of operation for the bit cell is referred to as the hold mode. During the hold operation, the access transistors are OFF and the bit cell is reduced to cross coupled inverter pair. The proposed bit cells also maintains the same. The WLB signal is high while the WL and RL signals are maintained low.

B. Read Mechanism for 7TP1 and 7TP2 Bit Cells

The 7TP1 and 7TP2 cells relies on a single bitline architecture and depends on transistor - N4 to enable the read operation. The effective read circuit configuration for reading Q = '0' and Q = '1' is given in Fig. 3.2 (a) and (b), respectively. There is no discharge path when the cell stores value '1', i.e., Q = '1', the same can be inferred from Fig. 3.2. This reduces the activity factor for the proposed bit cells to 0.5, thereby reducing its dynamic power consumption.

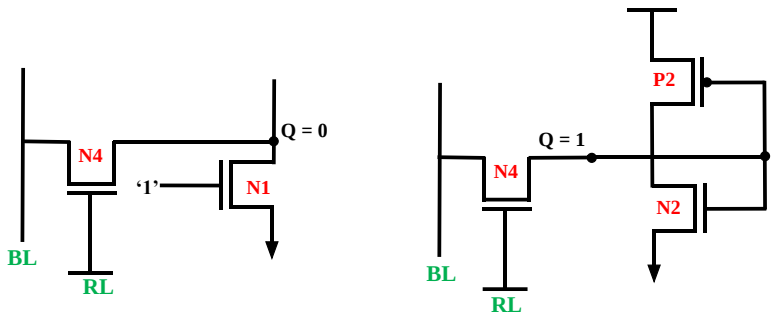


Fig. 3.2 Read path for the 7TP1 and 7TP2 bit cell for (a) Q = '0' and (b) Q = '1'.

But the read discharge path for the two cells includes the data node Q for the cell. This makes the two cells susceptible to read error. Therefore, to eliminate the data node from the read discharge path the 7TP3 and 7TP bit cell topology was proposed.

C. Read Mechanism for 7TP3 and 7TP4 Bit Cells

The orientation for the read access transistor N4 is changed for the proposed 7TP3 and 7TP4 cells. The gate terminal of N4 is connected to the Q node for enabling the read operation. If the data stored at Q is '1' then, during the read operation N4 is ON and BL discharges via N4 to RL. While for Q = '0', no discharge is observed as the N4 transistor is OFF. As the read discharge path for the bit cell does not include the data node, the read port becomes SNM free. An SRAM bit cell with such a read configuration has its RSNM equivalent to HSNM [135]. This read port configuration is also referred to as isolated read with read free noise margin [80]. If for a cell the read discharge current pass though the memory storage node, it makes the cell vulnerable to read error [136]. But cells that can isolate the data node from the read path are able to preserve data integrity during read operation [137, 138].

D. Write Mechanism for all Proposed 7T Bit Cells

The proposed bit cells are dependent on a single bitline to perform their write operation. To ensure a valid write operation, the feedback connection between the node QB and Q1 is disconnected. This is done by turning 'OFF' the N5 transistor. Thus, the effective circuit during the write operation is that of a cascaded inverter pair, as shown in Fig. 3.3. The cell is dependent on BL and the cascaded inverter configuration for the write operation. To begin the write operation, complement of the desired data is placed on BL. Thereafter, WL is activated to turn ON, N3 transistor. This enables the transfer of complementary data from BL to node Q1.

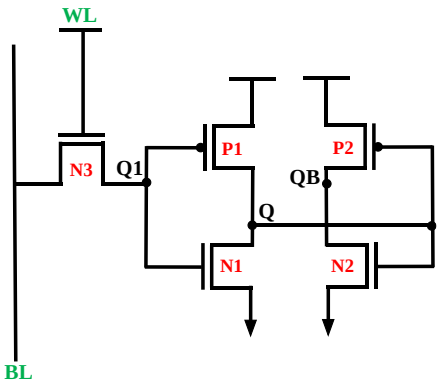


Fig. 3.3 Effective circuit during write operation for the proposed cells.

The node Q1 then drives inv_1 to develop the desired data at node QB. Similarly, inv_2 develops complementary data at Q. Therefore, it can be inferred that the speed of the write

operation depends on the speed of inv_1. The faster the switching for inv_1, the sooner the data at Q1 gets reflected at QB, thus driving inv_2 to its desired value. Therefore, it is critical to ensure a faster switching for inv_1. This implies that propagation delay for gate should be low. The propagation delay is calculated as -

$$\tau_P = \frac{C_L}{k_n (V_{DD} - V_{TH})}\left[\frac{2V_{TH}}{(V_{DD} - V_{TH})} + \ln\left(\frac{4(V_{DD} - V_{TH})}{(V_{DD} + V_{OL})} - 1\right)\right], \quad \text{here } k_n = \mu_n C_{OX} W/L \qquad (3.1)$$

Here, C_L is the load capacitance, V_{OL} is low level for the output voltage, μ_n is the mobility of electrons, C_{OX} is the oxide capacitance, W/L is the aspect ratio for the transistor. Using eq. (3.1), it can be concluded that decreasing the V_{DD} - V_{TH} can reduce the propagation delay for the gate [134]. Thus, to reduce the same, an LV_{TH} transistor (N1) is used in the circuit. The LV_{TH} NMOS due to low V_{TH} (compared to conventional NMOS) ensures faster switching. To further augment the performance of inv1, the aspect ratio for inv_1 is maintained at P1= 1 and N1 = 2.5. The N4 transistor remains OFF during the course of the write operation.

3.3 COMPARISON OF PERFORMANCE OF ALL PROPOSED CELL DESIGNS

The four proposed 7T bit cells are designed at 32 nm technology node and analysis for 300 mV V_{DD}. The four proposed cells are compared in terms of SNM, write time, and area footprint. This is done to determine the best 7T bit cell topology amongst the proposed designs. The main utility of a bit cell is to store information. A cell may encounter internal or external noise that may erroneously flip the information stored in it. Thus, the first and foremost evaluation parameter for a bit cell is the SNM. It is defined as the maximum noise that a bit cell can withstand before an erroneous flip in data is registered.

The SNM for each cell is evaluated for each operation – hold, read and write. The access operations – read and write are more crucial in terms of SNM, as the memory core for the cell is being accessed and the cell is more vulnerable to noise. The values obtained for HSNM, RSNM, and WM for the proposed 7T cells are graphically compared in Fig. 3.4. As can be observed from the figure, the HSNM values for all the cells for HSNM is nearly 90 mV. The RSNM values for 7TP1 and 7TP2 are same at 68 mV, while the values for 7TP3 are 90 mV and 7TP4 is 96 mV.

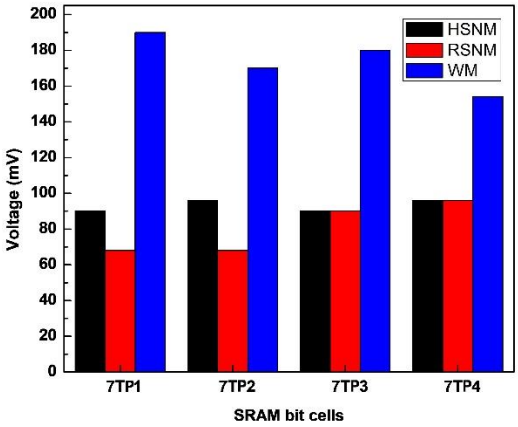


Fig. 3.4 Graphical comparison for SNM values obtained for the proposed 7T SRAM bit cell for hold, read, and write operation.

The RSNM values for 7TP3 and 7TP4 are equal to their HSNM values due to their read SNM free topology; the read discharge current for the two cells does not pass through the data node. In terms of WM, the cell with the most ideal performance is the 7TP4 cell with WM of 154 mV. The WM values for the 7TP1, 7TP2, and 7TP3 cells are 190, 170, and 180 mV, respectively.

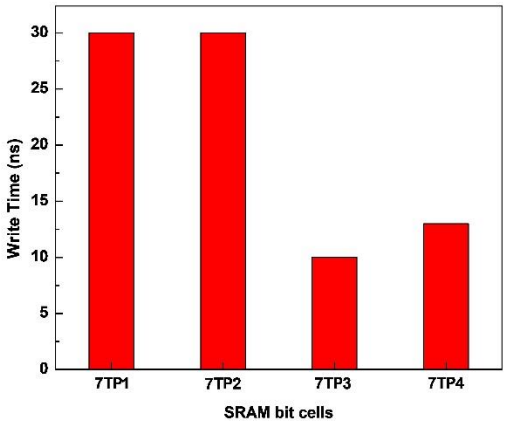


Fig. 3.5 Graphical comparison for the write time values for the different 7T proposed bit cells.

The SNM analysis takes into account only the static conditions, it does not account for the time consumed for performing an operation. The read and write operation for a bit cell are time dependent; the lower the pulse width, the better the memory. Amongst the two access operations (read and write), the write operation consumes more time, as data stored in the cell is to be altered. Thus, the timing requirement for the write operation for a cell is taken as the comparison platform amongst the cells. The write time values obtained for the four proposed 7T cells are compared in Fig. 3.5. The cell with the fastest write operation is the

7TP3 cell at 10 ns. It is closely followed by 7TP4 cell at 13 ns. While, the 7TP1 and 7TP2 cells consume more time to successfully complete write operation at 30 ns. The higher write time for the first two cells is attributed to the use of pass transistor read port transistor. It makes writing into the cell difficult.

Along with the performance parameters, the dimensions and area footprint for a cell are also essential parameters, as it determines the economic feasibility for the cell. The length (nm), width (nm) and area footprint (μm^2) for the proposed cells are compared in Fig. 3.6. The area for the 7TP1 cell is the least at 0.445 μm^2, closely followed by the 7TP3 cell with area of 0.54 μm^2. The area for 7TP2 and 7TP4 are 0.58 and 0.65 μm^2.

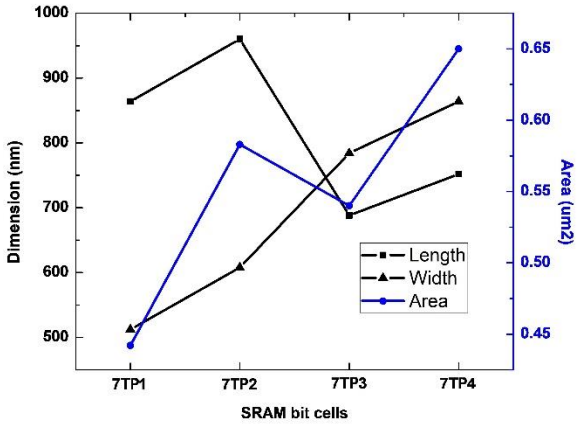


Fig. 3.6 Comparison of dimensions and area footprint for the four proposed 7T SRAM bit cells.

Based on the above stated comparison, it may be inferred that the 7TP3 is the best topology amongst the four designs. Its HSNM and RSNM are high at 90 mV; the WM value is slightly high. While, the write time is considerably low at 10 ns. Additionally, its area is also towards the lower end in comparison to others and the design is also nearly square (the length and width are more similar than other designs). Thus, the 7TP3 cell design is accepted as the best design topology amongst the four proposed 7T bit cells.

3.4 COMPARIOSN OF PERFORMANCE OF 7TP3 WITH PRE-EXISTING CELLS

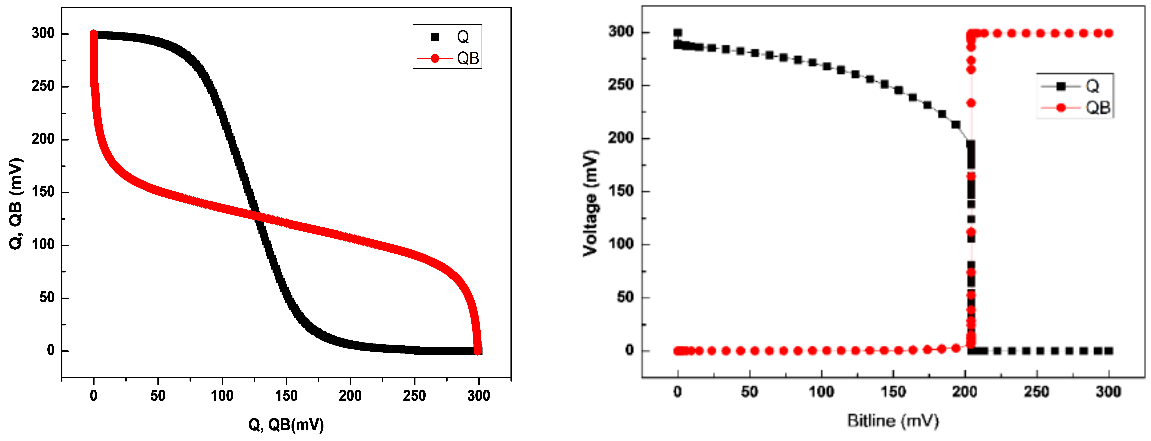
The circuits of all bit cells are designed at 32 nm technology node using PTM library files and simulated for V_{DD} of 300 mV. For the entire duration of the study, the temperature for the simulation environment is maintained at 27 ºC.

3.4.1 Static Performance Analysis for 7TP3 Against Pre-Existing Bit Cells

A highly reliable cell has high SNM for all operations. So, cells are foremost compared in terms of their static margins. The read and hold SNM for the bit cell are measured using the butterfly curve, obtained by superimposing the voltage transfer characteristics for hold and read operation, respectively. Side of the largest square inside the smaller lobe of the butterfly curve is its SNM [80]. The butterfly curve for RSNM and HSNM for the proposed bit cells are overlapping and are given in Fig. 3.7 (a).

An SNM free, isolated read port does not discharge through the memory core of the bit cell. For the proposed 7T bit cell, the read current path for the bit cell does not include Q or QB node, thereby enabling the cell to be read-SNM free [138, 139]. The read port for the bit cells decouples the storage node (Q and QB) from the bitline using the read access transistor. This produces a high RSNM and is nearly equivalent to the HSNM [135, 25]. Ahmad *et al.* [137] in 2017 have reflected the same as the HSNM and RSNM are not mentioned independently but categorized as SNM for the bit cell.

The read current path for the proposed 11T bit cells is exclusive of the memory storage node. The same is also reported by Sil *et al.* [138] in 2008. Additionally, He *et al.* [135] in 2019 have also graphically represented the same. Thus, the HSNM and RSNM for the proposed cell are found to be equal. The 7TP3 bit cell has a single ended configuration, wherein, the read path is not passing through the memory core for the bit cell. Therefore, the HSNM and RSNM for the bit cell are also equivalent. The comparison for SNM of the 7TP3 bit cell with other bit cells is shown in Fig. 3.8.



(a) (b)

Fig. 3.7 The butterfly curve for (a) HSNM and RSNM, (b) WM for 7TP3 SRAM bit cell.

The stability of the write operation is measured in terms of WM. Traditionally, write stability is measured using the WM. But recent studies have shown that WM is a more reliable parameter to ensure write stability [81]. WM is calculated for each bit cell using the method explained in [80]. The curve obtained for calculation of WM for the 7TP3 bit cell is given in Fig. 3.7 (b). The values corresponding to the WM obtained for all the bit cells are graphically compared in Fig. 3.8. For ease of comparison, the values for HSNM, RSNM, and WM for each cell are tabulated in Table 3.1.

Table 3.1 – Comparison of noise margin values for different bit cells

SRAM bit cell	HSNM (mV)	RSNM (mV)	WM (mV)
5T	80	BCC	50
6T	51	BCC	106
7T-1	75	30	196
7T-2	80	80	DP
7T-3	32	32	DP
7T-4	81	81	DP
7T-5	84	18	105
8T	84	84	144
9T	67	67	160
10T	83	83	182
7TP3	90	90	180

BCC – Butterfly Curve Collapsed, DP – Dual Pulse Write

The 5T and 6T cells have a single ended read and have their discharge path pass through the memory storage node, thereby, leading to a collapse of butterfly curve for RSNM values (represnted by butterfly curve collapse (BCC) in table). Thus, suggesting a read failure event for the two bit cells. For the 5T cell, the WM is also consideribly low at 50 mV, whereas the WM for 6T is considerable at 106 mV. The 7T-1 cell has a highly skewed performance, the HSNM is good but the RSNM is poor and the WM is extremely high at 75, 30 and 196 mV, respectively.

The 7T-2 cell though has a comparable HSNM and RSNM, but its write operation is a two-cycle process (represneted by dual pulse write (DP) in the table) and therefore, cannot be compared with the other bit cell, as the other cells are able to perform the write operation in a single cycle. Two 7T configurations 7T-3 and 7T-4 though have comparable HSNM and RSNM performance with 7TP3, but fail during the WM analysis at 300 mV. While, for 7T-5 bit cell the HSNM value is quite high, but its RSNM and WM metric are inferior at 18 and 105 mV, respectively.

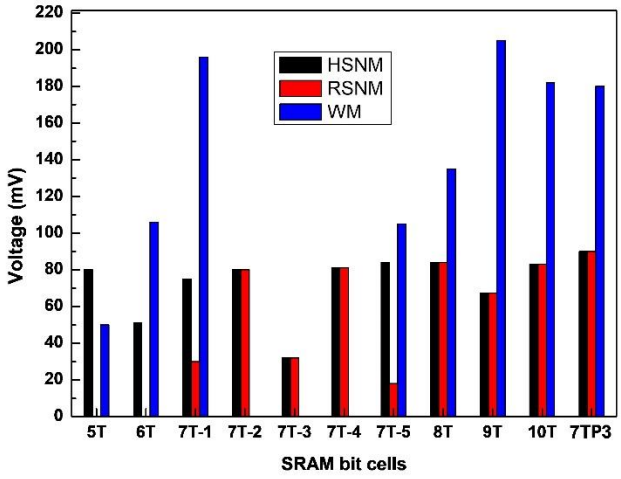


Fig. 3.8 Graphical representation for HSNM and RSNM for all SRAM bit cells.

The 8T, 9T and 10T bit cell have a comparable static performance with the 7TP3 bit cell, but there area panelties are high. Also, the power consumption for the three cells is also high, because the 8T cell has a dual port configuration, while 9T and 10T cells have a stacked inverter configuration. The stacked inverter configuration also reduces the I_{ON}/I_{OFF} ratio for the two cell. Thereby, decreasing the number cells that can be placed in an array. Therefore, it can be inferred that 7TP3 bit cell has better static performance in comparison to the other bit cells.

3.4.2 Tolerance Variation Analysis for 7TP3 Against Pre-Existing Bit Cells

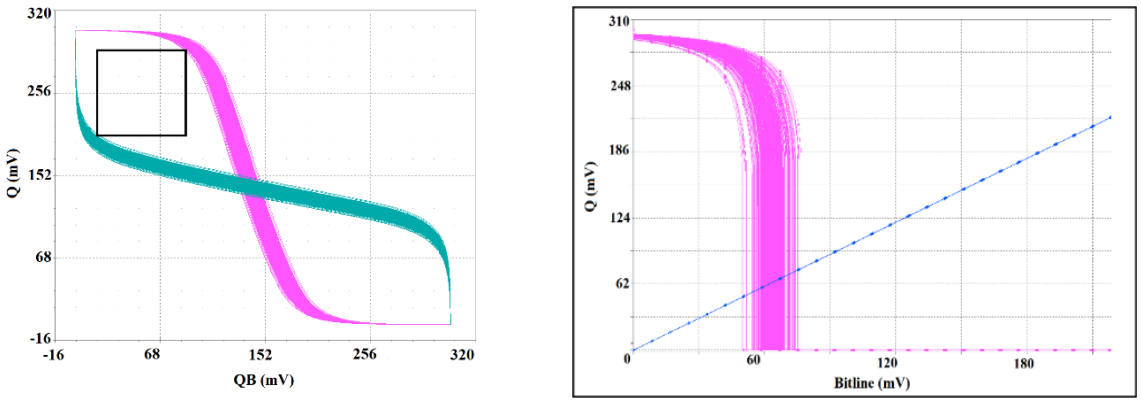
The recent decade has observed a high scaling trends in technology node. As most pre-existing bit cells were proposed for higher technology node and now are being analyzed at scaled technology node. The first impact of technology node scaling is that it introduces variability issues in circuit performance [56]. The perfromacne of bit cells is severely limited by PVT variations in deep sub micrometer regions [85,140]. Also, with the decreasing technology node the probability of error due to alpha particles and cosmic radiations has increased [141]. These errors are referred to as soft errors. As 7TP3 cell is free from HSD, bit interleaving (BI) with error correcting code is an effective method for dealing with such errors [142]. A cells susceptibility to such errors further increases with PVT variation.

A. Process Variation Analysis

The increasing demand for larger SRAM based cache memory has pushed the designers towards lower technology nodes. So, designing nanometer sized bit cell requires validation

for performance in terms of variability issues. With the increase in stress time, the bias temperature instability (BTI) increases the V_{TH} of the transistor and consequently degrades the performance of the circuit [137]. The BTI induced degradation of bit cell is different from NMOS and PMOS. In NMOS transistor, the BTI effect is caused by negative bias (NBTI) and for PMOS transistor the same is induced by positive bias (PBTI). But, both the effects impact the V_{TH} for the devices [143]. Therefore, researchers have modelled the impact of stress and aging on transistor in terms of variation in the V_{TH}.

The shifts in V_{TH} of the transistor leads to uncertainty in the circuit behavior [28]. Jin *et al.* [143] and Shah *et al.* [28] have mentioned different equations for BTI variation but they model it in terms of V_{TH}. Other factors that limit the performance of the bit cell are – hot carrier injection, gate oxide breakdown, backend dielectric breakdown, electro migration, and stress-induced voiding. But these factors have a random behavior and do not have a defined model of analysis. All variations can be transalted to an effective variation in the V_{TH} [144, 145]. Consequently, to analysie the impact of variation on device, the Gausian distribution for V_{TH} is an effective approach [24]. Therefore, for Monte Carlo (MC) simulation, the variation in the V_{TH} is taken as the primary factor for analysis.



(a) (b)

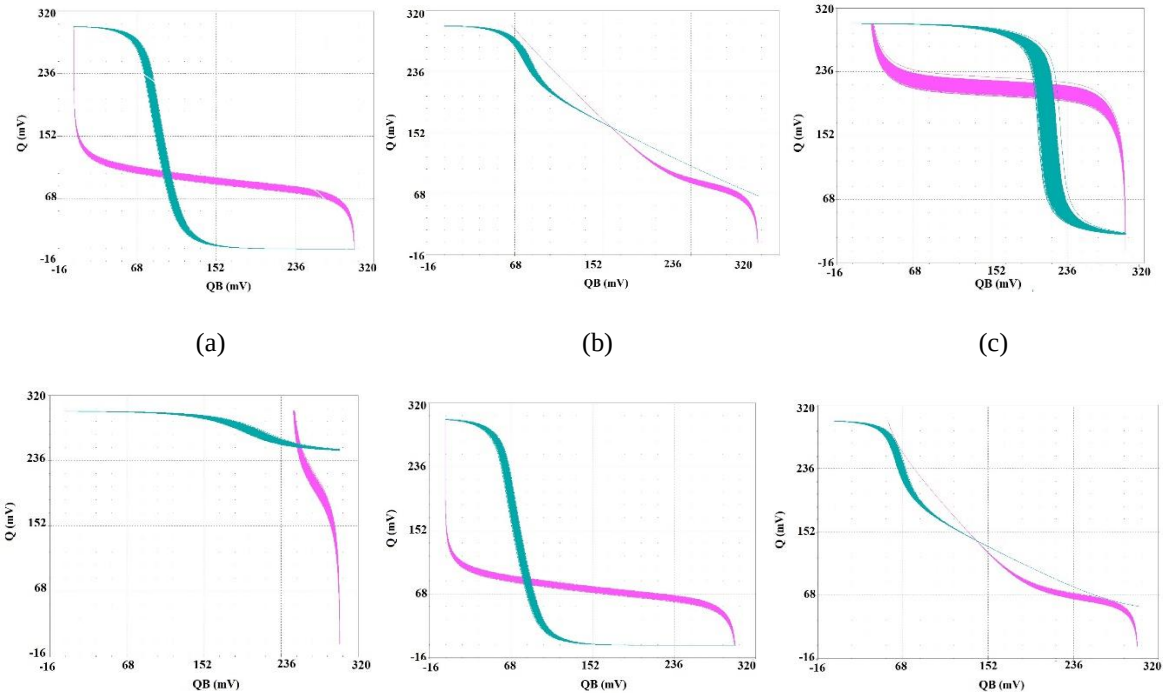
Fig. 3.9 Monte Carlo Simulations for (a) HSNM and RSNM, (b) WM for the proposed 7TP3 SRAM bit cell.

Ahmad *et al.* [137] in 2018 have used MC simulations with a sample size of 5000 to analyze the impact of BTI on the bit cell. Hence, it is essential to explore variation tolerant design solutions to mitigate variability issues due to temporal degradations. The 7TP3 bit cell is analyzed for variation tolerance under the process variation analysis using MC simulations for 10,000 sample size. Statistical methods were employed to identify the range of variability

in the performance of the 7TP3 cell. The main parameter for the statistical analysis is V_{TH} mismatch. To assure that the yield loss would be less than 0.1 for a 10 Mb cache memory, the permissible failure limit, P_{fail}, should be less than 10^{-10} [83].

The nature of probability curve is Gaussian so it corresponds to a μ_m-6σ factor. Here μ is the mean value of V_{TH}, while the 6σ factor represents the standard deviation of the distribution. So, the proposed bit cell is analyzed for 6σ variations for 10,000 point MC simulations. Therefore, MC simulations are used and V_{TH} for the bit cell is varied around the mean value for 6σ variations. The HSNM and RSNM for 10,000 points MC simulations of the 7TP3 bit cell are presented in Fig. 3.9.

The outcomes of the process variation analysis reveal that the HSNM and RSNM for the 7TP3 bit cell can vary up to 75 mV for the worst-case situation. While the WM for the bit cell increases to 215 mV. This variation in the bit cell performance is for maximum deviation from the mean value. The variation in HSNM and RSNM is 16.6% while, WM records a maximum variation of 19.44% for the 7TP3 bit cell. The MC simulation results for butterfly curve of all the different pre-existing cells described in chapter 2 are presented in Fig. 3.10.



(a) (b) (c)

(d) (e) (f)

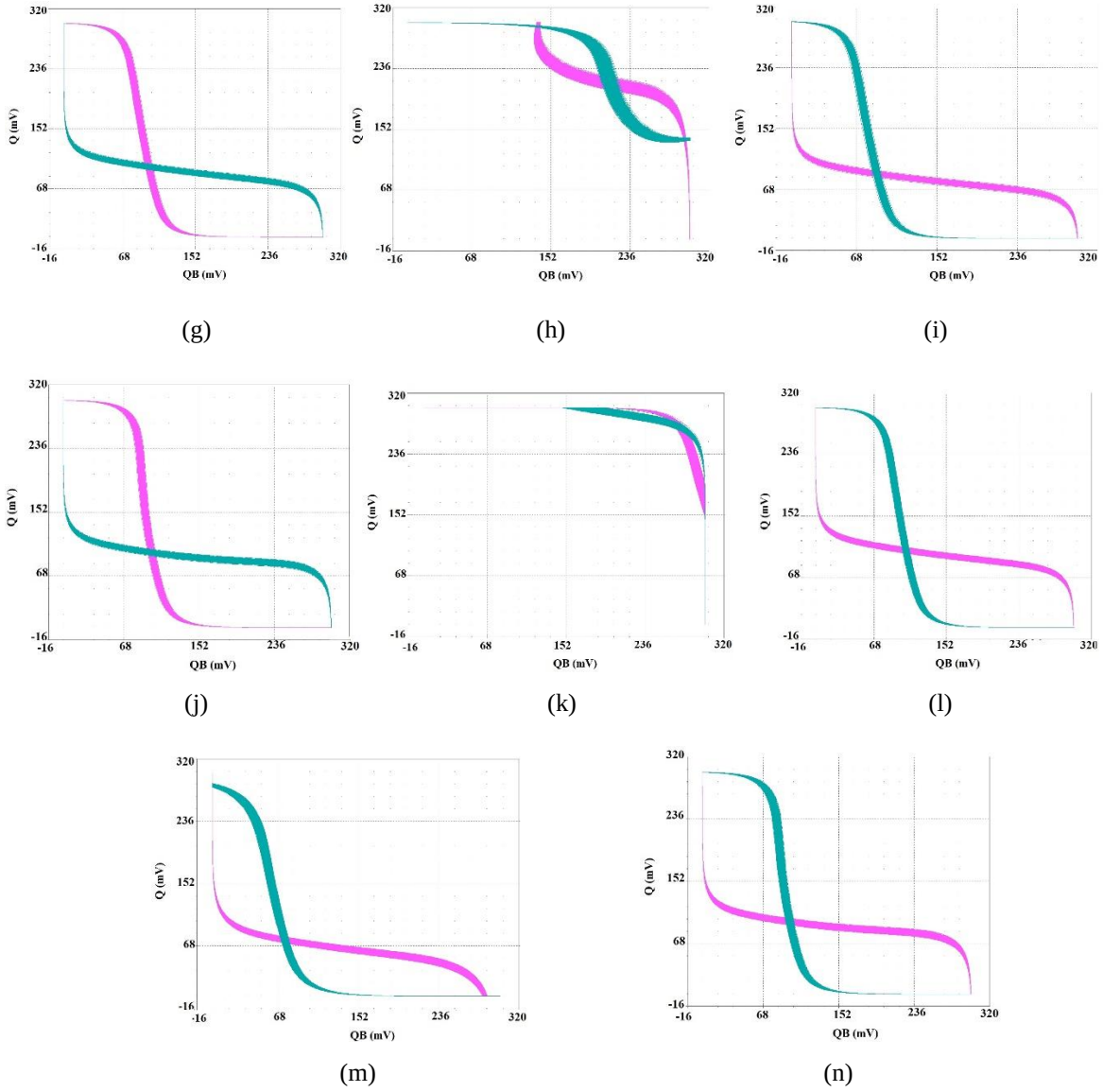


Fig. 3.10 Monte Carlo Simulations for (a) 5T HSNM (b) 5T RSNM, (c) 6T HSNM, (d) 6T RSNM, (e) 7T-1 HSNM, (f) 7T-1 RSNM, (g) 7T-2 SNM, (h) 7T-3 SNM, (i) 7T-4 SNM, (j) 7T-5 HSNM, (k) 7T-5 RSNM, (l) 8T SNM, (m) 9T SNM and (n) 10T SRAM bit cells.

The cells that register a collapse of their butterfly for the read operation are 5T, 6T, 7T-1 and 7T-5. These cells have a poor RSNM perfromance as their read path discharges through the storage nodes of the memory core, making it highliy vulnerable to read error. While, the 7T-2, 7T-3, 7T-4, 8T, 9T and 10T bit cells have equivalent HSNM and RSNM values as these cells have an isolated read port that does not discharge through the storage node of the memory core. Since, HSNM and RSNM are equal, a single curve is presented for them. The MC simulation for the WM for the bit cells are presented in Fig. 3.11.

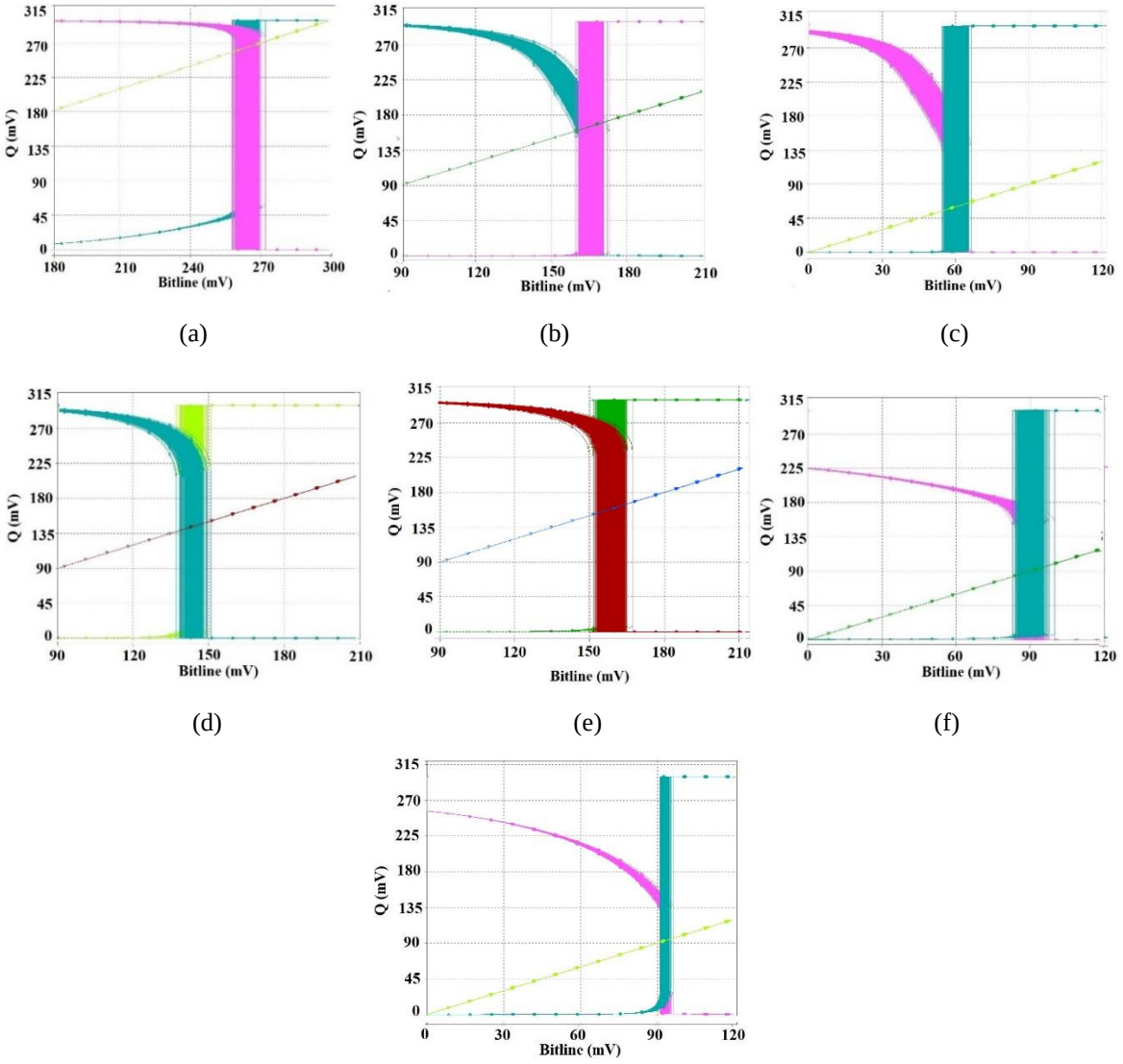


Fig. 3.11 Monte Carlo Simulations for WM for (a) 5T, (b) 6T, (c) 7T-1, (d) 7T-5, (e) 8T SNM, (f) 9T SNM and (g) 10T SRAM bit cells.

The performance of the 7TP3 bit cell is compared against the other bit cells (with the process variation analysis). The results thus obatined for process variation analysis are tabulated in Table 3.2. The MC analysis yields the variation in static performance metric for the bit cells. Therefore, four values are tabulated corresponding to minimum, maximum, mean, and standard deviation (SD) for each performance parameter (i.e. HSNM, RSNM, and WM). The cells that register maximum variation in their performance, are the 6T and 9T bit cells. These two cells have a high deviation from their mean value.

Additionally, the read static perfromance for the 6T cell at 300 mV is so inferior that the butterfly curve for RSNM is collapsed. A collapse in butterfly curve is also registered for

5T and 7T-1 cells. While, for 7T-5 SRAM bit cell the butterfly curve is on the verge of collapsing. It can be noted from Table 3.2, that perfromance of 7TP3 cell is well balanced as the MC simulations for the bit cell are moderate for all three performance parameters.

Moving forwards the worst case analysis data is of higher concern, as its impact on the perfromance of the circuit is more deteriorative. Hence the data for the worst case is graphically compared in the Fig. 3.12. It is observed that the result for each bit cell deteriorate under the process variation analysis. The 5T, 6T, 7T-1 cell observe a significant reduction in HNSM, while the RSNM is reduced to zero. Thereby, ensuring read failure for the three cells. The WM for 5T reduces to 45 mV, which is exteremly low while that for 7T-1 increases to 240 mV (too high). The 6T has a comparable WM at 135 mV but due to its read failure, the cell is categorised as inferior to 7TP3.

Table 3.2 – The values obtained for minimum, maximum, mean, and standard deviation for all the bit cell at 32 nm technology node using Monte Carlo Analysis.

Bit Cell	**HSNM (mV)**				**RSNM (mV)**				**WM (mV)**			
	Min	**Max**	**Mean**	**S D**	**Min**	**Max**	**Mean**	**S D**	**Min**	**Max**	**Mean**	**S D**
5T	66	88	77	11	BCC	BCC	-	-	30	60	45	15
6T	45	73	59	14	BCC	BCC	-	-	115	155	135	20
7T-1	64	84	74	10	BCC	BCC	-	-	230	250	240	10
7T-2	69	91	80	11	69	91	80	11	DP	DP	-	-
7T-3	21	43	32	11	21	43	32	11	DP	DP	-	-
7T-4	64	84	74	10	64	84	74	10	DP	DP	-	-
7T-5	73	89	81	8	4	18	11	7	120	160	140	20
8T	78	94	86	7.5	78	94	86	7.5	145	175	160	15
9T	45	73	59	14	45	73	59	14	180	230	205	25
10T	67	91	79	12	67	91	79	12	190	220	205	15
7TP3	80	100	90	10	80	100	90	10	160	230	195	35

BCC – Butterfly Curve Collapsed, DP – Dual Pulse Write, SD – Standard Deviation

The performane of 7T-3 is poor with respect to all static measures. The 7T-2 and 7T-4 cells have similar performance under process variation analysis. But owing to their dual write operation, the write perfroamcne cannot be compared. The MC simulation HSNM for 7T-5 is comparable to 7TP3, but its RSNM butterfly curve collapses, thereby making its perfromance inferior to the 7TP3 bit cell.

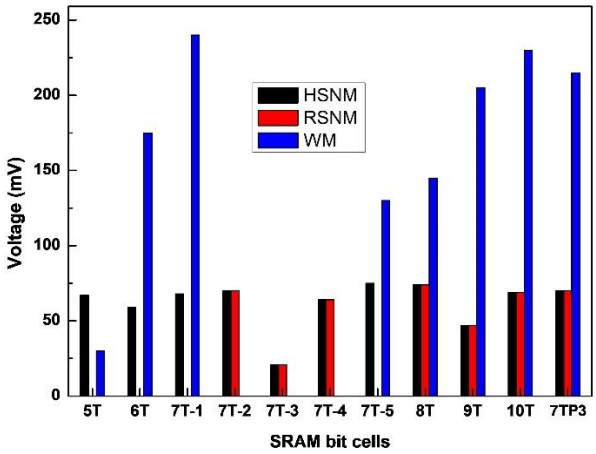
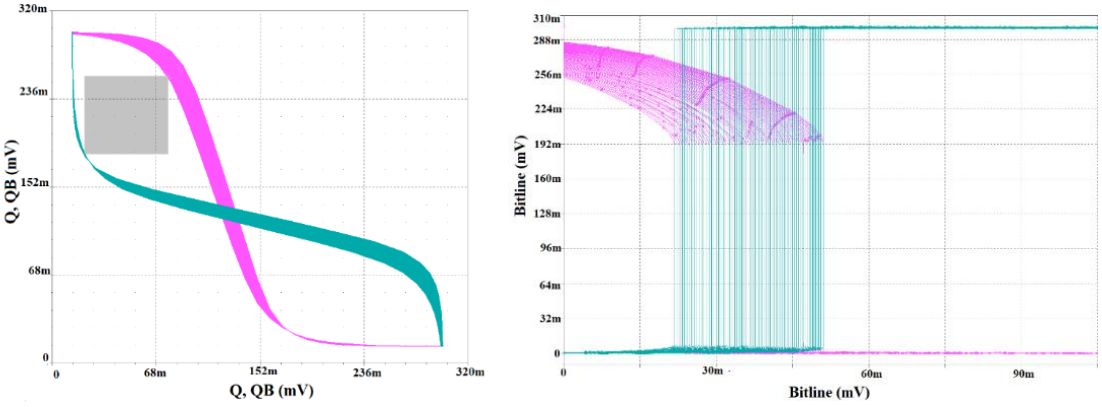


Fig. 3.12 Graphical comparison for the static margins obtained for all the SRAM bit cell under process variation analysis.

Another cell that suffers and shows an inferior performance for process variation analysis is the 9T bit cell. Its HSNM and RSNM values reduce considerably, thereby making it less suitable for low voltage utilization. While the WM increases beyond 200 mV, making it extremly difficult to write into the cell. The 8T and 10T bit cells have a considerable performance with respect to HSNM and RSNM for the cell. But the WM for 8T is low, while that for 10T bit cell is very high at 116 and 230 mV, respectively. The HSNM and RSNM for the proposed 7T bit cell is highest for the proposed 7T bit cell. Also its WM is fairly reasonable at 180 mV.

B. Temperature Variation Analysis

SRAM bit cells form a major part of SoC and these SoC's functions under wide temperature ranges. Due to continuous operation or uncontrolled environmental conditions, the device temperature may surge [146]. Therefore, an SRAM bit cell has to be analyzed for performance under varying environment temperature. So the performance of the 7TP3 bit cell is analyzed for temperature range of -10 ºC to 80 ºC. This performance analysis ensures the reliability of the cell under varying environment temperature. The results for HSNM, RSNM and WM analysis for the 7TP3 bit cell are presented in Fig. 3.13. As can be observed from the graphs, the performance of the bit cell does show a bit of deflection with temperature variation, but the performance of the cell is still within good range of performance.



(a) (b)

Fig. 3.13 Performance of the proposed 7TP3 SRAM bit cell for temperature range from -10 ºC to 80 ºC (a) HSNM and RSNM and (b) WM.

The bit cell is able to maintain HSNM and RSNM margin at 80 mV, which is 11.1% deviated from the normal functioning. While the WM increases to 190 mV. The read and hold margins are reduced by 0.1 mV/ºC. While the WM changes 0.2 mV/ºC. This data proves that the performance of the 7TP3 bit cell varies slightly with increase in temperature.

C. Voltage Variation Analysis

An SRAM cell may be subjected to varying values for V_{DD}. Also, it is imperative to analyse each cell for performance under sub-threshold and super threshold conditions. Therefore, static analysis for 7TP3 bit cell for voltage varying from 0.3 V up to 0.7 V is presented in this sub-section. The values obtained for HSNM/RSNM and WM are depicted in the Fig. 3.14. The graphical representation reflect that the 7TP3 bit cell maintains its superior performance for the entire voltage range.

The operational V_{DD} increases, the SNM and the WM values for the cell inceases. But the increase in the noise margin is more drastic for the sub-threshold region as compared to the super threshold region. As the increase of V_{DD} from 0.3 V to 0.4 V increases the HSNM by 55.5%, while the increase is 35% for 0.4 V to 0.5 V. The increase is 25.7% and 19.2% for 0.5 to 0.6 V and 0.6 to 0.7 V, respectively.

With the decreasing technology node, the vulnerability to error due to α-particles and cosmic neutrons is increasing. These particles generate extra charge through direct or indirect ionization in silicon, which is collected by sensitive nodes, creating voltage transients at those nodes [147]. This transient caused in an SRAM bit cell causes an incorrectly stored

datum and this error is referred to as soft error issue. The reduction in V_{DD}, adds to the vulnerability of SRAM bit cells towards soft error [148, 149]. Additionally, as explained by Jahinuzzaman *et al.* [150] in 2009 the process and temperature variations that a SRAM cell may encounter, add to the soft error susceptibility [151]. Therefore, the 7TP3 bit cell is analyzed for process and temperature variations.

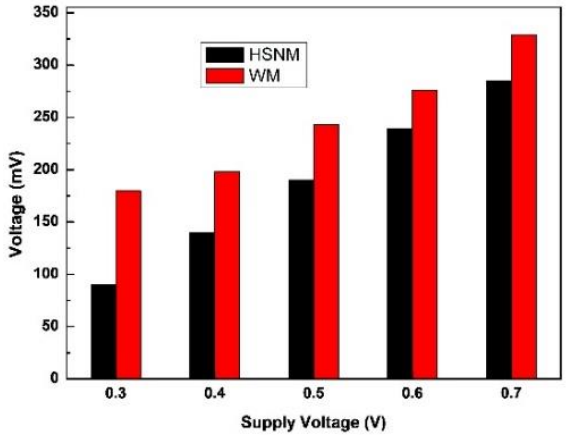


Fig. 3.14 Performance of the proposed 7TP3 SRAM bit cell with varying voltage.

The analysis reveals that the cell is fairly tolerant to these variations and registers a stable performance for the same. So, in keeping with the reference [151] and conclusion stated by Jahinuzzaman *et al.* [150], we also conclude that the 7TP3 bit cell will demonstrate reasonable performance against soft error. Many researchers: Mansore *et al.* [152], Wen *et al.* [56], Shin *et al.* [153], Ahmad *et al.* [137] have also reported BI as an effective method to eliminate soft errors.

BI technique is used to segregate the continuous bits of a single word by placing them separately [141]. This non-consecutive placement of bits on the same wordline to create an interleaving architecture is a preferred alternative to solve soft error issues. Researchers Nayak *et al.* [154] have reported their 8T bit cell to be capable of soft error minimization based on BI. The same conclusion is also reported by researcher Pal and Islam [24] for their 9T bit cell reported in 2016. As BI architecture is supported by the 7TP3 bit cell, it should also demonstrate resilience to soft errors.

BI is a technique that places only one bit of a word at a particular location rather than all the bits of a word together. It is an efficient architectural technique to deal with soft errors [141-142]. Sachdeva and Tomar [141] in 2020, reported an isolated read port based 10T bit cell.

This 10T cell uses BI as an efficient technique to shield their bit cell against soft errors. Similar information is also explained in the work reported by Mansore *et al*. [152] in 2019, for 11T bit cell, with a read SNM free isolated read port. However, BI technique is only applicable to the cells that exhibit a fully half-select free operation [137].

Using the same analogy for our 7TP3 bit cell, as it is also HSD free, it can be stated that utilizing BI will make the 7TP3 bit cell resilient to soft errors. BI is also referred to as column selection architecture. SRAM bit cells employ this technique to achieve area efficiency and provide soft error protection as reported by Wen *et al.* [56] in 2016. This work also suggests that cells with HSD free architecture are appropriate for BI configuration. Thereby supporting the claim that as the 7TP3 cell is fully half-select free, utilizing BI for designing the SRAM array will make the cell less vulnerable to errors. The cell is HSD free due to its row and column based independent signals for read and write operations.

3.4.3 Failure Probability Analysis for 7TP3 Against Pre-Existing Bit Cells

The stability for the bit cell is estimated based on the HSNM, RSNM and the WM values for the bit cell. Whereas, the failure probability for the three operations: read, hold and write, are estimated using eq. (3.2-3.4) [43]

$$\mathbf{P_{R-Fail}} = \mathbf{Prob.}\,(\mathbf{RSNM} < \mathbf{kT}) \tag{3.2}$$

$$\mathbf{P_{H-Fail}} = \mathbf{Prob.}\,(\mathbf{RSNM} < \mathbf{kT}), \text{ and} \tag{3.3}$$

$$\mathbf{P_{W-Fail}} = \mathbf{Prob.}\,(\mathbf{WM} < \mathbf{0\ mV}) \tag{3.4}$$

If the RSNM and HSNM are lower than thermal voltage (kT = 26 mV at 300 K), the thermal noise will cause a bit error in the SRAM cell. The bit error rate (BER) is defined as the probability of a random event causing an error in the bit cell during its operation [155]. The failure probabilities for each cell are calculated and the obtained values are presented in Fig. 3.15.

In keeping with the process variation analysis, the read failure probability for 5T, 6T, 7T-1 is unity, as they register a zero RSNM under process variation analysis. Similarly, the write failure probability for 7T-3 and 7T-4 are also unity, as they have zero WM. The 7T-2 cell is shown to have unity failure probability because its WM cannot be realized as it has a dual

cycle write operation. The failure probablity for 7T-5 is contrasting as its hold failure probablity is very low due to its high HSNM. While, the read failure probability is high, owing to its differential nature and its write failure probablity is also moderatly high. The 8T, 9T and 10T bit cells have lower failuer probablity in comparison to the other bit cells. The lower deviation from the static margin for the bit cell leads to the lower failure probability. The 7TP3 bit cell registers the least failure probability, thereby making it more BER tolerate than other bit cells.

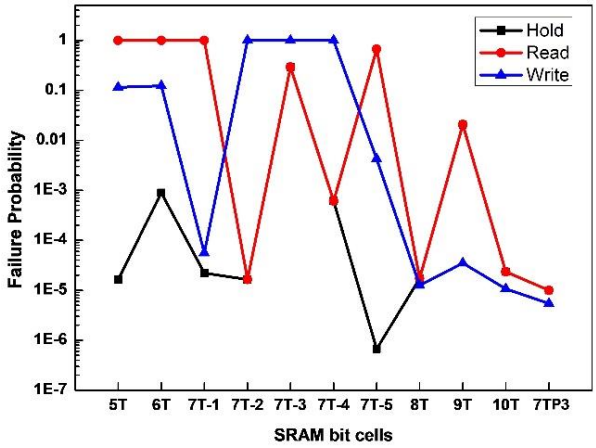


Fig. 3.15 Failure Probability Comparison for all SRAM bit cells for read, hold, and write operation.

As discussed in the previous subsection, another issue that arises in SRAM bit cell as the V_{DD} and technology node are shrinking is the soft errors [138]. These vulnerability are applicable to the 7TP3 bit cell as well. But as the tolerance variability of the 7TP3 bit cell is high and also its failure probability being low; the cell can be inferrd to be more reliable than the other cells. Also, since the 7TP3 bit cell is HSD free, employing BI makes the 7TP3 memory tolerant to soft errors. Also, employing interleaving of multiple word lines onto same physical row [156] would help to avoid soft error concerns.

3.4.4 I_{ON}/I_{OFF} Analysis for 7TP3 Against Pre-Existing Bit Cells

The relationship between the read current and leakage current is called the I_{ON}/I_{OFF} ratio. Greater I_{ON}/I_{OFF} ratio allows designer to create a larger SRAM array. A column in the SRAM array shares a SA for the read circuit. So, a greater current ratio ensures that a designer can integrate a greater number of bit cells per column. Thus, reducing the bulk of read peripheral circuit in the memory architecture. Therefore, a bit cell with higher ratio is preferred over other bit cells. The comparison for the I_{ON}/I_{OFF} ratio for all the cells is plotted in Fig. 3.16.

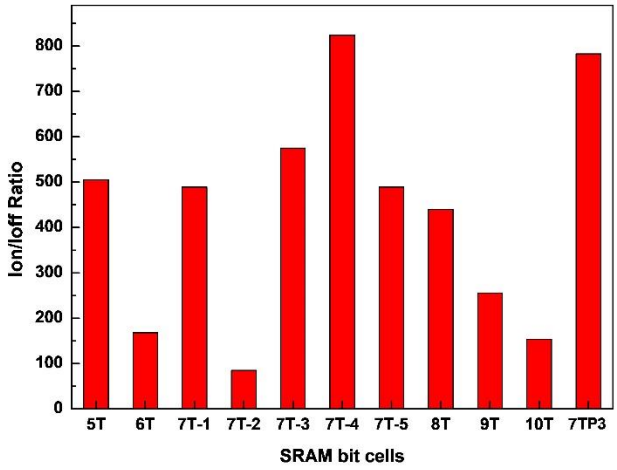
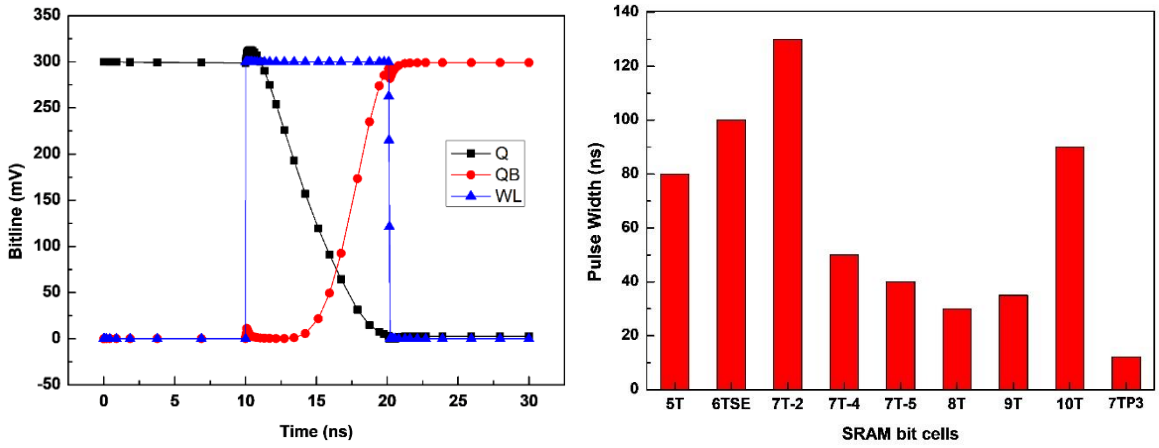


Fig. 3.16 Comparison of the I_{ON}/I_{OFF} ratio for all the SRAM bit cells.

On the basis of the graphical comparison for I_{ON}/I_{OFF} presented in Fig. 3.16, it can be concluded that the 7TP3 bit cell has improved performance with respect to I_{ON}/I_{OFF} ratio. The bit cells 6T, 7T-2, and 10T have a poor performance, as their I_{ON}/I_{OFF} ratios are 168, 85, and 154, respectively. While the 5T, 7T-1, 7T-3, 7T-5, 8T, and 9T bit cells display moderate performance with the ratio being 505, 489, 575, 489, 440, and 256, respectively. The two cells that have the highest ratio values are 7T-4 and 7TP3 at 824 and 783, respectively. Therefore, for hardware implementation they would be the preferred choice. The bit cells 5T, 7T-1, and 8T show a reasonable performance but the 7TP3 bit cell outranks them under this evaluation. The 9T and 10T bit cells suffer highly in the current ratio metric because of their stacked inverter configuration.

3.4.5 Dynamic Write Analysis for 7TP3 Against Pre-Existing Bit Cells

The static analysis of WM assumes infinite pulse width for the write operation. While real time write operations for an SRAM bit cell is dependent on a finite pulse width. Therefore, determining the minimum pulse width for a successful read operation is imperative for an SRAM bit cell design. The minimum pulse width needed to perform a successful write operation is referred to as write pulse width (T_{crit}). In this work, the T_{crit} is estimated using the method explained in reference [80]. If the pulse width on WL is lower than T_{crit}, it leads to a write failure for that cycle. Therefore, it is imperative to ensure that the pulse width of WL is greater than T_{crit}. A successful write operation at 300 mV for the 7TP3 bit cell is shown in Fig. 3.17 (a). The T_{crit} for the proposed cell is found to be 10 ns at 27 ºC.



(a) (b)

Fig. 3.17 (a) Dynamic write operation for finite pulse width of 10 ns for the proposed 7TP3 SRAM bit cell and (b) Graphical comparison for the T_{crit} needed for successful write operation for the different bit cells.

The pulse width needed for the other bit cells to perform a successful write operation are compared in Fig. 3.17 (b). All the bit cells require pulse widths multi-fold larger than the 7TP3 bit cell. The 5T, 6T, 7T-1, 7T-4, 7T-5 8T, 9T and 10T bit cell require the pulse width to be 80, 100, 130, 50, 40, 30, 35 and 90 ns, respectively. The 7T-2 and 7T-3 fails to perform dynamic write operation at 300 mV V_{DD}.

3.4.6 Power Consumption Analysis for 7TP3 Against Pre-Existing Bit Cells

SRAM occupies a major section of SoC and thus, the total power consumption by the system will have a major contribution from the memory circuit. Therefore, analyzing the power consumption of the SRAM bit cell during each operation is important. The current requirements for the bit cells are different for the three operations – read, write, and hold. Also, the power consumption of the circuit depends on the value stored in the bit cell. So, while evaluating the power consumption for each operation, the power is computed for Q = '0' and '1'. Thereby providing a very comprehensive understanding of the power consumption of the bit cell.

Power consumption for s cell is maximum during the read and write operation, as the cell is being accessed. Amongst the two, higher power consumption takes place during the write operation. As the data stored in the core of the bit cell has to be flipped to perform a successful write operation. While, the read operation requires the voltage on the bitline to drop to a point where the data in the memory core of the bit cell can be sensed by the SA.

Therefore, the read power consumption for the bit cells is lower as compared to write power consumption. The graphical comparison of the read and write power of the bit cell for Q = '0' and Q = '1' is given in Fig. 3.18. It can be observed from the power consumption graphs, that the 7TP3 bit cell has the least power consumption for read as well as write operation. This improved performance of the 7TP3 bit cell is credited to the optimal sizing of the transistors and the presence of a LV_{TH} NMOS.

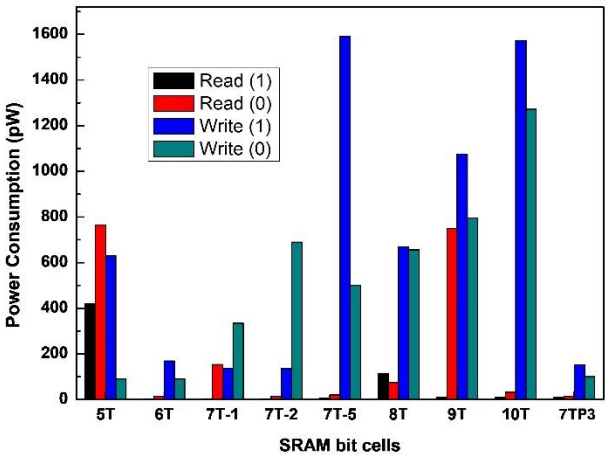


Fig. 3.18 Comparison of read and write power consumption for the proposed 7TP3 SRAM bit cells with pre-existing cells.

The 7TP3 bit cell relies on reduction of α_T to reduce the dynamic power consumption. The 7TP3 bit cell utilizes the same and is dependent on a single bitline architecture for its operation. This single bitline structure also helps in reducing the C_L for the cell, thereby ensuring a three-fold reduction in the dynamic power consumption of the 7TP3 bit cell. Additionally, as the 7TP3 cell has a considerably low τ , it can be justified that the 7TP3 is bound to have low short circuit power.

Another major factor that contributes to total power consumption of cell is static power consumption. SRAM bit cell primarily operates in the hold mode. Therefore, power consumption during the hold mode – referred to as standby power - forms a major component of the total leakage power consumption [81]. Hence, it is imperative to analyze the standby power for cell. Additionally, in submicron technologies, standby power is a major component of overall power consumption and can be attributed to the increased leakage current of nano-scaled device.

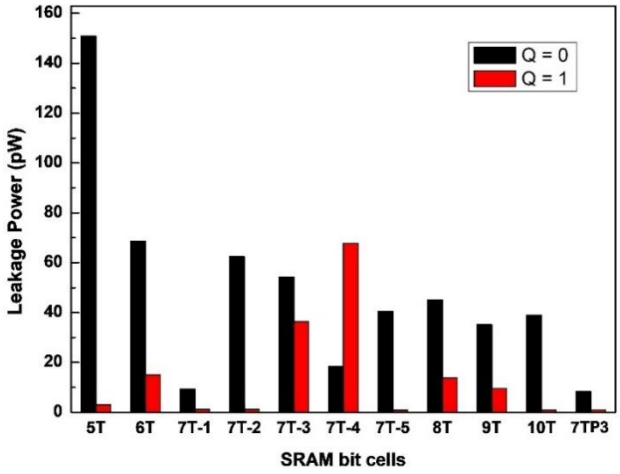


Fig. 3.19 Comparison of leakage power consumption for the proposed 7TP3 SRAM bit cells with pre-existing cells.

To evaluate the leakage current, the cell is set in the hold operation mode, i.e., the data values are stored in the cell. Then the access transistors are turned OFF. Once the access transistors are OFF the current at the drain terminal for the transistor is measured. During the process, the bitline is set high and then corresponding to data stored at Q = '0' and Q = '1', the leakage current is calculated for the bit cells. The leakage power is calculated V_{DD} times the leakage current for all the bit cells. The comparison for the leakage power for all bit cells discussed so far is presented in Fig. 3.19.

The above bar graph confirms that the proposed SRAM bit cell has the least standby power for both Q = '0' and '1' at 8.4 and 1.2 pW, respectively. The standby power for Q = '0' is highest for 5T bit cell while for Q = '1', the highest standby power is recorded for 6T bit cell. This hold mode power at Q = '0' for 5T, 6T, 7T-1, 7T-2, 7T-3, 7T-4, 7T-5, 8T, 9T and 10T bit cell is greater by 16.9, 7.17, 0.11, 6.42, 5.46, 1.18, 3.82, 4.35, 3.17 and 3.64 than the leakage power for 7TP3 cell. While for Q = '1' the standby power is greater by 1.85, 13.28, 0.14, 0.17, 33.57, 63.57, 0.15, 12.14, 8.14 and 0.14 times in comparison to the 7TP3 bit cell.

3.4.7 Layout and Area Analysis for 7TP3 Against Pre-Existing Bit Cells

Area analysis is imperative as SRAM bit cells are integrated to form large cache memory. This memory occupies a significant area of the SoC. The layout for the proposed cell is depicted in Fig. 2.20. The dimension - length (µm), breadth (µm), and area (µm^2) for the proposed cell and the pre-existing cells are tabulated in Table 3.3.

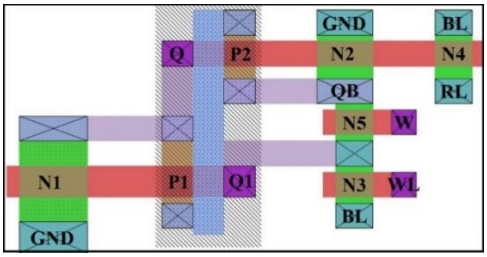


Fig. 3.20 Layout design for the proposed 7TP3 cell.

This validates that even if the transistor count increases, the area may turn out to be less if the transistors are sized accurately. Similar results were reported by Pal *et al.* [24] in 2020, wherein, their proposed 9T bit cell exhibited area 7% less than the pre-existing 8T bit cell. Gupta *et al.* [157] in 2018 have also reported a 10T bit cell with area 7% less in comparison to a pre-existing 8T bit cell.

Table 3.3 Layout dimensions for the 7TP3 and other pre-existing SRAM bit cells.

SRAM bit cells	L (µm)	W (µm)	Area (µm^2)
5T	0.736	0.896	0.659
6T	0.8	1.024	0.819
7T-1	0.864	0.848	0.733
7T-2	0.8	0.768	0.614
7T-3	0.592	0.8	0.474
7T-4	1.072	0.656	0.703
7T-5	0.72	0.8	0.576
8T	0.96	0.88	0.845
9T	1.040	0.848	0.882
10T	1.056	0.896	0.946
7TP3	0.688	0.784	0.539

The area of the proposed bit cell is 0.539 µm^2. The area for 5T, 6T, 7T-1, 7T-2, 7T-4, 8T, 9T and 10T bit cells are 0.659, 0.819, 0.614, 0.733, 0.703, 0.845, 0.882 and 0.946 µm^2 respectively. With reference to 7TP3 bit cell, 5T, 6T, 7T-1, 7T-2, 7T-4, 7T-5, 8T, 9T and 10T cells occupy more area by 22.17 %, 51.8 %, 35.8 %, 13.9 %, 30.4 %, 6.78 %, 56.6 %, 63.6 %, and 75.5 %.

3.5 SUMMARY OF IMPORTANT RESULTS

The key findings in this chapter are summarized as follows –

1. In this chapter four topologies for a single ended, single port 7T bit cell (7TP1, 7TP2, 7TP3, and 7TP4) are presented. Their perfromance is compared to identify the best

desgin amongst the four proposed designs.

2. The read SNM free port based cell, designed using six conventioanl and a high performance transistor is identified as the nest design topology amongst the proposed cell.
3. The 7TP3 is identified as the best topology amongst the four designs. Its HSNM and RSNM are high at 90 mV; the WM value is slightly high. But the write time is considerably low at 10 ns. Additionally, its area is also towards the lower end in comparison to others and the design is also nearly square (the length and width are more similar than other designs).
4. The bit cell is compared with other SRAM bit cells that have single ended operation. The bit cell is operational at 300 mV and maintains HSNM, RSNM and WM at 90, 90 and 180 mV respectively.
5. The MC analysis of the bit cell highlights that even under 6σ global variation, the cell maintains 75 mV as the read as well as hold SNM, while the WM is 215 mV. This validates the stability of the bit cell under process variation.
6. The temperature variation analysis for temperature ranging from -10ºC to 80ºC reveals that HSNM and RSNM are reduced by 0.1 mV/ºC. While the WM changes 0.2 mV/ºC.
7. The pulse width needed for the cell to perform a successful write opration in 10 ns. While the power analysis portrays that the proposed bit cell maintains a low power consumption of all operation. The highlight being the least standby power of 8.4 and 1.05 pW for Q = '0' and '1' respectively.
8. These aforementioned parameters are maintained with a very high I_{ON}/I_{OFF} ratio of 783. This implies that the number of bit cell per column of the 7TP3 bit cell is higher in comparison to other bit cells.
9. The layout for the bit cell occupies 0.539 μm^2 area. This area footprint for the bit cell is least amongst all the other cells. The 5T, 6T, 7T-1, 7T-2, 7T-4, 8T, 9T and 10T bit cells have area greater than the proposed cell by 22.17, 51.8, 35.8, 13.9, 30.4, 6.78, 56.6, 63.6 and 75.5 %.

CHAPTER – 4

DUAL MODE OPERATIONAL SRAM CELL FOR LOW POWER AND HIGH SPEED OPERATION

The growing popularity of hyper-personalized devices and round the clock connectivity has generated the need for a bit cell that can bridge the gap between low power and high-speed operation. But high-speed operation and low power performance are complementary factors, and conventionally one is obtained at the cost of the other. Therefore, memory designers cater to either of the two factors when designing a bit cell. But with the advent of internet of things and round the clock connectivity, the need for a cell that can cater to both the factors is growing. Thus, the following objective is framed to accommodate the aforementioned need –

"Design a dual mode operational SRAM bit cell with the capability to switch between different configurations."

Methodology used to achieve the desired objective in the chapter is as follows -

- Conceptualization for a dual mode operational cell for low power and high speed operation.
- Design a single ended, dual port 7T SRAM bit cell for the dual mode operational cell.
- Analyze the performance of the proposed 7T dual port cell and validate it against other pre-existing 7T bit cells.
- Design a dual mode operational cell using proposed single port and dual port cells.

In this chapter, the concept for a dual mode operational bit cell is presented. A single ended, dual port cell is proposed, its performance is analyzed, and then the best single ended, single port cell from chapter 3 is combined with this dual port cell to design the dual mode operational cell. This chapter is categorized into seven sections including introduction, section 4.1. Further in section 4.2, the concept for the dual mode operational cell is explained. Thereafter, the proposed single ended dual port cell is explained in section 4.3. Its performance for different parameters is analyzed in section 4.4. While the design for the proposed dual mode operational cell is explained in section 4.5 and its performance is

analyzed in section 4.6. Finally, the important results for the chapter are summarized in section 4.7.

4.1 INTRODUCTION

SRAM is a fundamental part of most multimedia systems [158-159]. Consequently, improving performance of an SRAM based memory is crucial to performance enhancement of the setup. Additionally, with the surge in the requirement of Internet of Things (IoT) setups, the demand for high speed, low power, and portable devices has grown exponentially. According to the present statistics, over 70% multimedia devices utilize SRAM for cache memory design, which accounts for up to 30% of the total power consumption and 50% of die area for the system [49].

In keeping with the multimedia device requirements, a memory designer must ensure low power and high-speed operation with high packaging density. The major concern for a memory designer is the dichotomic requirement of low power and high-speed operation. The two demands are complementary, and one may be achieved at the cost of the other. As a result, the gap between the two is pushing designers to search for alternatives to rectify the same. The problem is further intensified by the shrinking technology node to increase the integration density of the memory. The increasing demand for round the clock connectivity and burst towards IoT has generated the demand for versatile SRAM.

Additionally, an SRAM array is common for a system and is shared between circuits with different error tolerance, delay, and power requirements. For example, image processing application in a multimedia device has higher tolerance to error but require faster operation [49]. Whereas, data centric applications need the memory performance to be error proof, while being slightly relaxed about the speed of the circuit. But this makes the system a bit power hungry. Thus, each system has different requirements – faster operation, lower power, high error tolerance, in keeping with the application that it is presently catering to.

But from a designer's perspective, error tolerance, low power consumption, faster operation, and high integration density are trade-offs [160]. Therefore, achieving them all at the same time is an extremely difficult task in a conservative cell design. Thus, a new concept of dual mode operational SRAM is described in this chapter. The proposed cell is a versatile SRAM cell designed with the capability to function in two different single ended configurations –

single port and dual port. The single port bit cell is power efficient but with higher delay and greater error propensity than the dual port cell. While the dual port cell is more effective for faster operation but is power hungry [80]. Also, the dual port cell enables pipelining, whereas this is not the case with single port cell.

4.2 CONCEPT FOR A DUAL MODE OPERATIONAL SRAM CELL

Re-configurability in an architecture refers to its ability to rearrange the elements or settings of a system, device, or computer application. The concept of re-configurability in devices has been around for a long time. Schuyler *et al.* [161] used re-configurability to design memory cells that can function both as random access memory and read only memory. This helps to eliminate the need for designing an application specific test procedure. But this patent only modulates the use of an already designed memory cell. Each cell in the memory block is not worked upon. Also, it is not able to improve the performance of the cell.

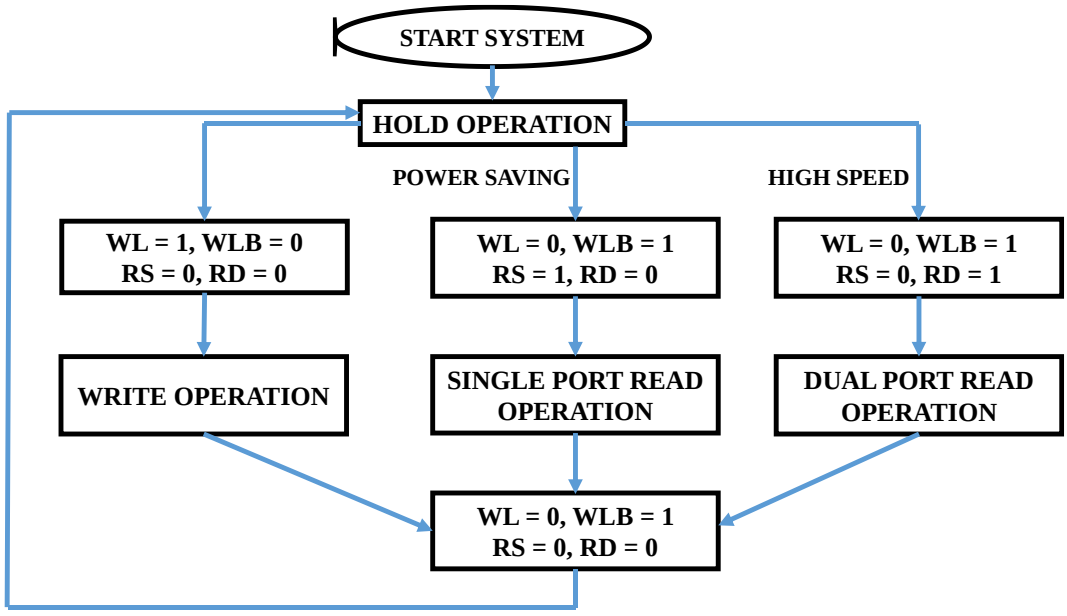


Fig. 4.1 Flow diagram representation of the proposed concept for a dual mode operational SRAM cell.

Similarly, another patent that reports re-configurability in memory was reported by Sutardja Sehat [162]. In it, the researcher has reported a block level memory structure, capable of working as per requirement of different application. But neither of the two patents work on the bit cell that stores the information. Whereas, the recent boom in demand for artificial intelligence and machine learning applications has generated the need for high performance memory circuits with minimum propensity for error. This demand is further aggravated by

increased inclusive integration of different devices for round-the-clock connectivity via internet access for developing an IoT. An IoT setup has fluctuation in its design requirements in keeping with the time of day. A device connected to the setup is expected to be operational at its full capacity for a fraction of the day; other times it may function in the power saving mode.

Thus, in this chapter the concept of a dual mode operational cell that can reconfigure between single port and dual port topology is presented. Its working is explained with the help of a flow chart demonstrated in Fig. 4.1. This reconfigurable cell includes a control circuit that enables the cell to either work in single port or dual port configuration. The bit cell is composed of eight transistors and is grouped into three sub-parts – single bit memory core, reading port and writing port. The single bit memory core of the reconfigurable memory is the part that stores the desired information. The read and the write port are the access circuitry that enable the device to read and write into the cell, respectively.

4.3 PROPOSED SINGLE ENDED, DUAL PORT SRAM BIT CELL

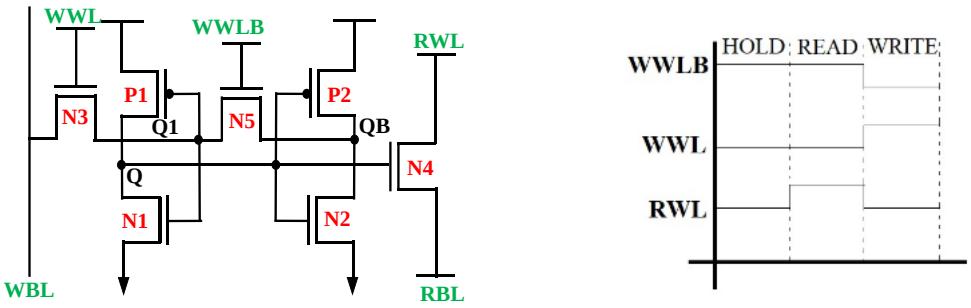
With decreasing technology node, the power consumption per bit cell has become a crucial parameter. It also accentuates the read-write conflict inherent to an bit cell, resulting in poor read and write performance. Therefore, to improve bit cell performance at scaled technology nodes, a single ended- dual port configuration is proposed in this chapter. It is the most efficient topology for eliminating the inherent read-write conflict for the bit cell. Consequently, the proposed cell is designed with single ended, dual port configuration.

The data core is more stable if the mutually coupled inverter pair configuration is employed. But the WM for single ended cross-coupled inverter pair is poor, whereas the WM is balanced if the data core is transformed into cascaded inverter configuration. Consequently, transistor N5 is added to the inverter core, to facilitate conversion of mutually coupled inverter to cascaded inverter configuration. Unlike a conventional cell, the write assist for the 7TP cell does not depend on discharge via the bitline for the write operation. Its write assist technique is only dependent on the voltage level and not current flow. During the write operation for the proposed bit cell, the complement of the data to be written into the cell, is placed on WBL. For example, if ‘1’ needs to be written into the cell, the WBL is set as ‘0’and vice-versa. Therefore, a conventional single ended write driver followed by an

inverter (to ensure that complement of the intended data is present on the WBL signal) is used.

For the read assist scheme, the conventional pass transistor mechanism made the cell vulnerable to erroneous data flip during the read operation. This vulnerability is caused by the discharge current for the read operation passing through the data node for the bit cell. Alternatively, to eliminate the read discharge current from passing through the data nodes of the cells, the gate of the read access transistor – N4, is connected to the data node, Q. This scheme ensures that current discharge occurs only when the Q data node is high, while not manipulating the information on the data nodes.

The additional advantage of this read assist scheme is that it makes the cell read SNM free. Also, owing to the single ended nature of the port, the activity factor for the cell is reduced to half, thereby reducing the dynamic power consumption for the bit cell. Consequently, a 7T cell using single ended, dual port, 1R1W configuration is proposed. It is composed of seven transistors (7TP). The memory block of the cell is composed of mutually composed inverter pair (P1-N1 and P2-N2).



(a) (b)

Fig. 4.2 (a) Schematic and (b) control signal for 7TP SRAM bit cell.

Table 4.1. Signal Status during hold, read, and write operation for the proposed 7T SRAM bit cell.

	WBL	**WWL**	**WWLB**	**RWL**	**RBL**
HOLD	1/0	0	1	1	1
READ	1/0	0	1	1	0
WRITE - 1	0	1	0	1	1
WRITE - 0	1	1	0	1	1

The working of 7TP is dependent on breaking the cross coupled inverter pair connection. This is achieved using an additional transistor (N5). The utility of N5 is that it acts as a switch to enable/disables the mutual feedback connection depending on its ON/OFF state. The working of N5 transistor as switch is controlled by signal WWLB. The write operation is facilitated by access transistor N3, controlled by write bitline (WBL) and write wordline (WWL). Together they form the write port for the 7TP cell.

While the read port is formed by access transistor (N4) controlled by read wordline (RWL) and read bitline (RBL). The circuit diagram for 7TP cell is given in Fig. 4.2 (a). While the state of control signals during different operations are illustrated in Fig. 4.2 (b). The working of 7TP cell in its three different modes, namely, hold, read and write is explained subsequently. The signal condition during hold, read, and write operation are also tabulated in Table 4.1.

4.3.1. Hold Mechanism for Proposed 7T Cell

During the hold operation the WWL signal is low (WWLB is high), while the RWL and RBL signals are maintained high. During this operation, the access transistor, N3 is OFF, as WWL is not exerted. Transistor, N5 is in ON state because signal WWLB is exerted in this operation to maintain the mutual feedback connection between the inverter pair.

4.3.2. Read Mechanism for Proposed 7T Cell

During the read operation, the signals exerted for the correct cell functioning are WWLB, RWL, and RBL. The first two control signals are high, while the RBL signal is low during the read cycle. The RWL will discharge through N4 to RBL only for Q = ‘1’. While for Q = ‘0’ no discharge event will occur as the N4 transistor is OFF. Thus, reducing the activity factor for the bit cell.

4.3.3. Write Mechanism for Proposed 7T Cell

During the write operation, the WWL signal is high (WWLB is low), while RWL and RBL signals are maintained high. Additionally, the WBL is ‘0’, when writing ‘1’ and vice-versa. During the write operation, N5 is set low to disconnect the back-to-back connection between inverter pair. The cell is now solely dependent on WBL for the write operation for the cascaded inverter configuration. The complement of the input data is placed on WBL and

WWL control signal is set high to activate W1. The data gets transferred from WBL to node Q1, which further drives P1-N1 to develop the data at node Q. Similarly, Q drives P2-N2 to develop data at QB. The read control signal, RBL and RWL remains high for the entire duration of write operation.

The write operation for the proposed cell is dependent on the mutual effect of inverter pair to develop the data values on the storage node. Therefore, to guarantee good write ability, the voltage transfer characteristic of each inverter is modified in keeping with eq. 4.1 and 4.2. This ensures faster switching of inv1 from one level to another. Thus, ensuring an efficient write operation for the bit cell.

$$\tau_{PHL} = \frac{C_L}{k_n (V_{OH} - V_{TH})}\left[\frac{2V_{TH}}{(V_{OH} - V_{TH})} + \ln\left(\frac{4(V_{OH} - V_{TH})}{(V_{OH} + V_{OL})} - 1\right)\right] \quad (4.1)$$

$$\tau_{PLH} = \frac{C_L}{k_n (V_{DD} - V_{TH})}\left[\frac{2V_{TH}}{(V_{DD} - V_{TH})} + \ln\left(\frac{4(V_{DD} - V_{TH})}{(V_{VDD} + V_{OL})} - 1\right)\right] \quad (4.2)$$

It can be inferred from eq. 4.1 and 4.2 that the gate delay is inversely proportional to $V_{DD} - V_{TH}$. Consequently, as V_{TH} decreases, the delay diminishes [163]. As, the write ability of the cell is dependent on the speed of inv1, N1 transistor is an LV_{TH} NMOS. This is done owing to its lower V_{TH} than that of conventional NMOS transistor, thereby ensuring faster write operation. In addition to this, the aspect ratio for inv1 is optimized to further augment its performance.

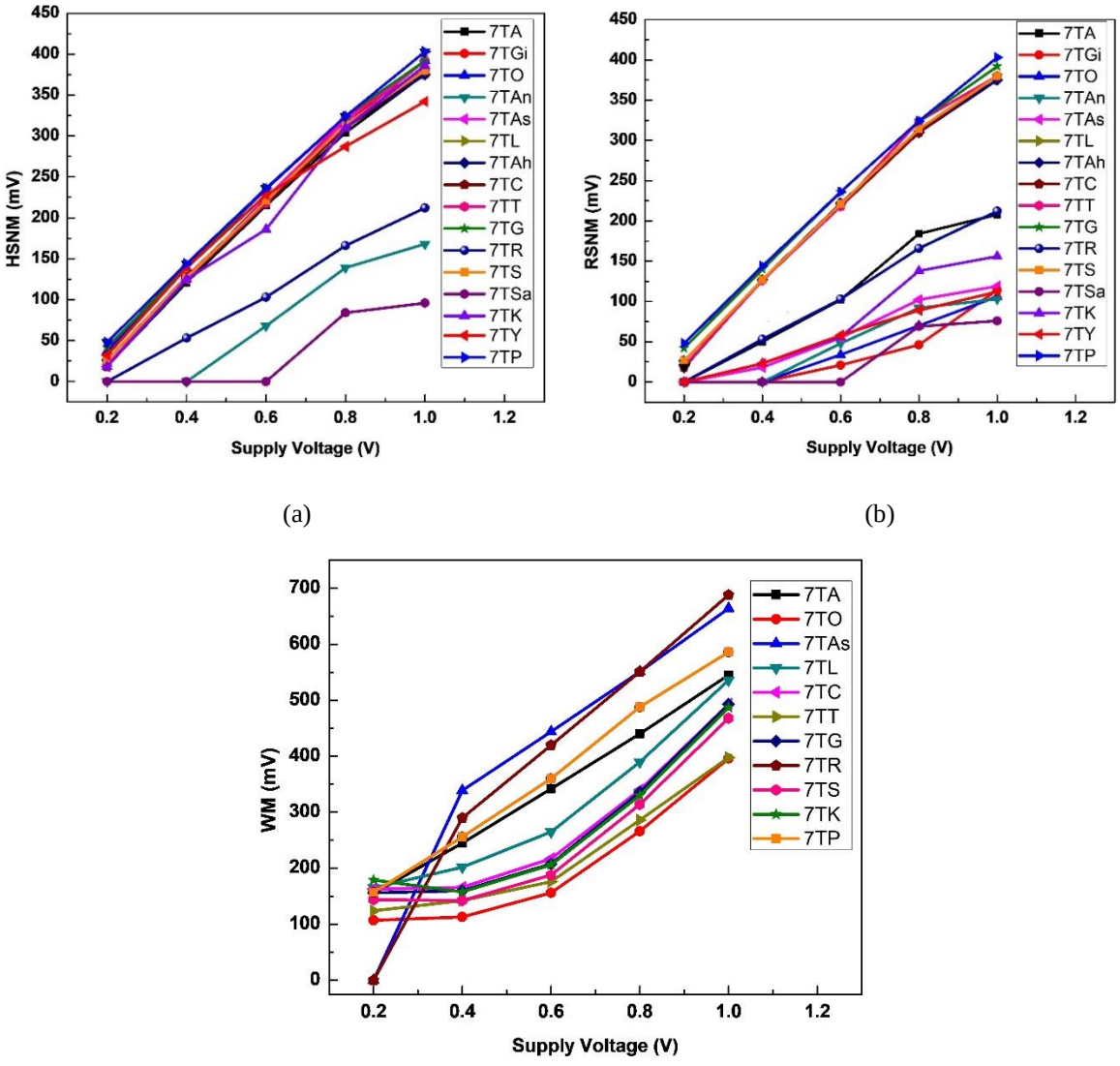
4.4 PERFORMANCE ANALYSIS FOR THE PROPSOED DUAL PORT 7T CELL

The different pre-existing 7T bit cells discussed in chapter 2 were reported for varied technology nodes and V_{DD}. Therefore, for a fair performance analysis all cells are designed at 32 nm technology node, while maintaining the aspect ratios reported in their respective papers.

4.4.1 Voltage Scaling for Optimal Supply Voltage Determination

As the technology node for each cell is reduced to 32 nm, it is imperative to evaluate all the bit cells along with the proposed cell to identify the minimal V_{DD} at which each cell is operational. As a consequence, all the bit cells are evaluated for SNM for hold, read, and

write operation for V_{DD} ranging from 0.2 V to 1 V. The results are graphically compared in Fig. 4.3. The HSNM values for different voltage ranging from 0.2 V to 1 V are depicted in Fig. 4.3 (a). Based on HSNM comparison, it can be inferred that the 7TSa and 7TG cells register a collapse in HSNM butterfly curve for 0.6 V and 0.4 V of V_{DD}, respectively. While the performance of 7TR cell is lower in comparison to the other bit cells.



(a) (b)

(c)

Fig. 4.3 Graphical comparison for (a) HSNM, (b) RSNM, and (c) WM for all different 7T SRAM bit cells for supply voltage varying from 0.2 V to 1 V.

The remaining 7T cells have similar results in terms of HSNM performance because here only the robustness of the data storage inverter couple is tested. The memory core is isolated from the bitline configuration; therefore, the HSNM attains a fairly high value. Whereas, during the read operation, the cells are subjected to read discharge current, which may lead

to vulnerability in the cell. Therefore, the RSNM analysis paints a better picture as to which cell is more robust against others. The RSNM values for the different 7T bit cells corresponding to varying V_{DD} are compared in Fig. 4.3 (b). As can be observed from Fig. 4.3 (b), the RSNM values for 7TA, 7TR, 7TK, 7TAs, 7TGi, 7TG, 7TO, 7TY, and 7TSa are fairly low in comparison to the other bit cells. Amongst these cells, the 7TK, 7TAs, 7TGi, 7TG, 7TO, 7TY, and 7TSa cells have extremely low RSNM values for V_{DD} of 0.6 V. Therefore, it is appropriate to conclude that they are not a preferential choice for low voltage operations.

A similar observation can also be made for Fig. 4.3 (c). It demonstrates WM values for different 7T cells for varying values of V_{DD}. The WM values for most bit cells have a linear decline from 1 V to 0.6 V. Whereas for values lower than 0.6 V, the WM values are converging to values between 100 to 200 mV. The 7TR and 7TAs are the only two cells to record a zero WM value at 0.2 V. It can therefore be inferred that minimal V_{DD} for most cells is 0.6 V, but the static margins are very low at this point. Therefore, for a fruitful comparison, all the bit cells are compared for 0.8 V. Also, for 0.6 V, the operation for the cells lies in the near threshold region, which may lead to inferior performance for cells, as they were not originally designed to operate in near threshold region. Therefore, all the 7T cells are evaluated for 0.8 V, so as to ensure all cells have a fair chance to perform in the analysis.

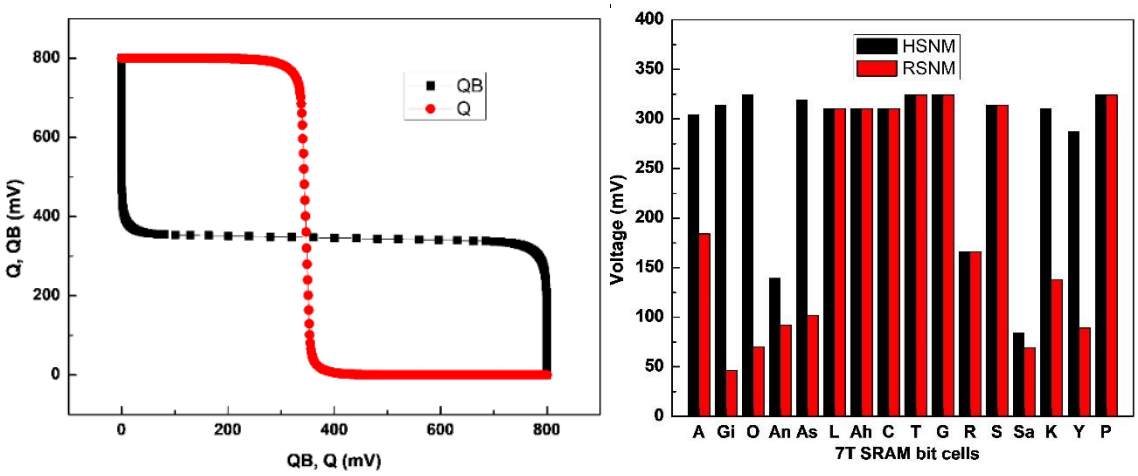
4.4.2 Stability Analysis for Proposed Dual Port 7T Cell

As explained, stability analysis is the first round of clearance that a cell must pass to qualify as a reliable bit cell. SNM is the most reliable measure to evaluate the immunity to noise during the read and hold operation [63]. It is the maximum noise that a cell can withstand before tampering the data stored in the cell. It is attained by graphically overlapping the voltage transfer characteristics of the inverter pair resulting in formation of butterfly curve [164, 165]. SNM equal to the side length of the maximum possible square embedded into the smaller lobes of the butterfly curve.

A. Hold Static Analysis

The successive decrement in technology node and V_{DD} has made SNM of chief importance. Also, most bit cells in the cache memory array are in hold mode and only one cell is accessed at an instant of time. Therefore, safeguarding stability of hold operation is imperative for a

cache. The butterfly curve for 7TP is presented in Fig. 4.4 (a) and the obtained values for all cells are compared in Fig 4.4 (b). The HSNM value obtained for the 7TP cell is 324 mV. The other bit cells that have the same HSNM value are 7TT, 7TG, and 7TO. The bit cells that have slightly less HSNM values in comparison to 7TP are 7TS, 7TGi, and 7TAs with the HSNM value of 314 mV. While the HSNM value for 7TL, 7TAh, 7TC, and 7TK is 310 mV.



(a) (b)

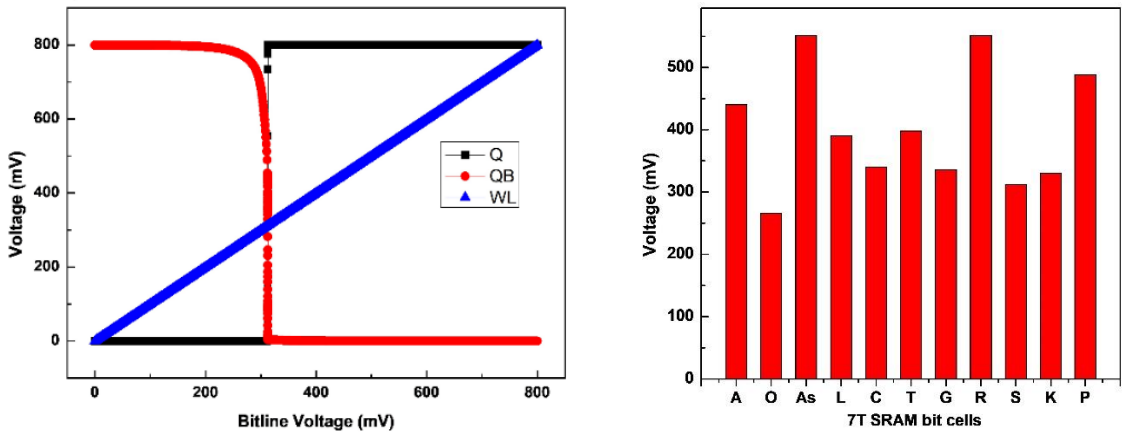
Fig. 4.4. (a) Butterfly curve for HSNM (RSNM) for 7TP cell, and (b) Graphical comparison between the HSNM/RSNM values for all 7T SRAM bit cells.

The 7TA, and 7TY bit cells have their HSNM values at 304, and 287 mV, respectively. The other bit cells; 7TR, 7TSa, and 7TAn have a significantly low HSNM at 166, 84, and 139 mV, respectively. This analysis helps categories cells into inferior and superior based on the HSNM values. The HSNM value for 7TSa is least amongst all the cells, as in the super threshold region, the inverter configuration for the cell makes the pull up network very strong and the voltage transfer characteristics for the cell are highly skewed towards high level. The second inverter acts as the body bias circuit for the first transistor; the output of second inverter is connected to the body terminal for the first inverter. Therefore, the V_{TH} for the transistors of the first inverter varies largely. Consequently, the HSNM value for the cell is poor.

B. Read Static Analysis

During the read operation, the cell is accessed, and the bitline is discharged based on the data at the storage node. But if the discharge operation includes the data storage node, it may

lead to a destructive read operation resulting in erroneous data flip in the cell. Therefore, it is imperative to quantify RSNM. Differential read operation is more prone to noise error whereas, for a single ended read port, if the read discharge path includes the data storage node (Q or QB), the susceptibility to read error increases. Thereby decreasing the RSNM for the cells. While the bit cells that do not use data storage node as a part of read discharge path, have RSNM equal to HSNM [70]. The RSNM values for all the cells are compared in Fig. 4.4 (b). The RSNM value for the 7TP cell is equivalent to its HSNM, as it has an isolated read free SNM configuration. Therefore, the butterfly curve for HSNM and RSNM for 7TP cell are overlapping in Fig. 4.4 (a).



(a) (b)

Fig. 4.5. (a) WM curve for 7TP, and (b) Graphical comparison of WM for the bit cells.

The RSNM values for 7TT, 7TG, 7TR, 7TS, 7TL, 7TAh, 7TC, and 7TP are equivalent to their HSNM values. The cells with significantly low RSNM value are 7TSa, 7TGi, 7TA, 7TK, 7TY, 7TAn, 7TAs and 7TO at 69, 46, 184, 138, 89, 92, 102, and 70 mV, respectively. The inferior RSNM performance for 7TGi, 7TA, 7TAn, 7TAs, and 7TO are attributed to their differential configuration. While the lower performance of the 7TSa, 7TK, and 7TY is caused by the discharge path passing through the storage node of the cell.

C. Write Margin Analysis

During the write operation the data stored in the cell is overturned, as data on bitline is written onto the storage node via access transistors. The stability during the write operation is measured in terms of WM [81]. The WM curve for 7TP cell and its comparison with WM for all the other bit cells is presented in Fig. 4.5 (a) and (b) respectively. The WM value for

7TP cell is 488 mV. Significantly high value for WM is registered for 7TAs and 7TR at 551 mV. The 7TT and 7TL have a balanced value that lies in the vicinity of $V_{DD}/2$. The cells that have recorded low WM value are 7TG, 7TS, 7TC, 7TK, and 7TO at 336, 312, 340, 330, and 266 mV, respectively. The 7TGi, 7TY, and 7TAn have a dual pulse write operation and therefore are not included in this analysis to prevent a pseudo inferior depiction for the cells against other cells. All the aforementioned values (HSNM, RSNM, and WM) are tabulated in Table 4.2.

4.4.3 Read and Write Timing Analysis for Proposed Dual Port 7T Cell

Static analysis assumes an infinite pulse width for the read and write operation, but real time operations have timing constraints. Thereby, deeming it necessary to measure the time constraint for read and write operation for the bit cell topologies. The write time for a cell is calculated using the method explained by Ahmad *et al.* [81]. It defines write time as the interval between the write wordline signal going high to when the data value in the memory core is flipped. Whereas, the read time for a cell with single ended read operation is estimated on the guidelines defined by Lin *et al*. [166]. They have defined the read time as the time needed to drop the voltage level of bitline to the switching voltage for inverter [166]. The read and write time values obtained for all the 7T bit cell are compared in Fig 4.6.

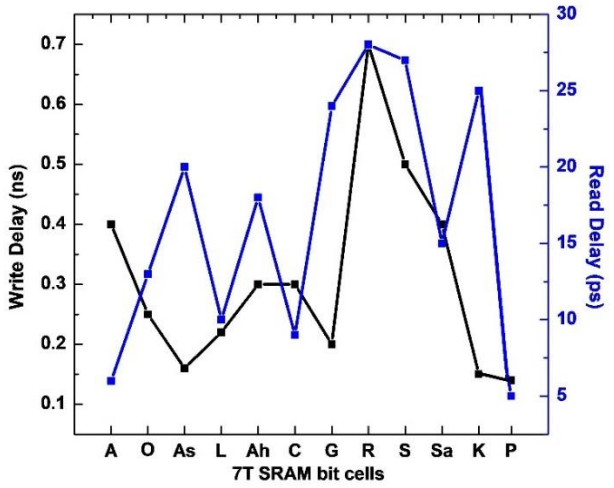


Fig. 4.6. Graphical comparison of write and read delay for the 7TP SRAM bit cell.

It can be observed from Fig. 4.6 that the 7TP cell registers a successful read and write operation in 5 ps, and 0.14 ns, respectively. The other cells with low pulse-width requirement

for the read operation are 7TA, 7TL, and 7TC with pulse-width of 6, 10, and 9 ps, respectively. Whereas, for the write operation the cells with lower pulse-width requirement are 7TO, 7TAs, 7TL, 7TAh, 7TC, 7TG, and 7TK with pulse-width requirement of 0.25, 0.16, 0.22, 0.3, 0.3, 0.2, and 0.15 ns, respectively.

While the cell that shows the most inferior performance amongst the described cells is the 7TR cell. This cell requires a 28 ps, and 0.7 ns pulse width for successful read and write operation, respectively. Four cells -7TC, 7TGi, 7TY, and 7TAn are not included in this analysis as they have a two pulse write operation and therefore comparison with single pulse write operation will project them inferior, but it would not be a fair evaluation.

4.4.4 Current Ratio Analysis for Proposed Dual Port 7T Cell

An SRAM based cache memory is formed by arranging bit cells in large array configurations. Therefore, the drive current for an bit cell during the read operation should be large so as to allow a large number of bit cells in a column of the array. The column size for the array is directly proportional to the current ratio; defined as the ratio between the read current and leakage current for the bit cell. The greater the value for the current ratio, the higher the number of cells that can be integrated in a column of the array. Consequently, when designing a cell, it is imperative to ensure highest possible value for the current ratio.

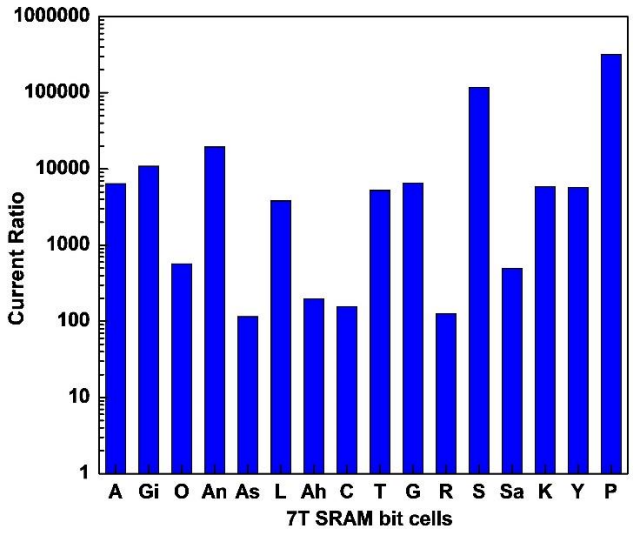


Fig. 4.7. Graphical comparison of current ratio for the different 7T SRAM bit cells.

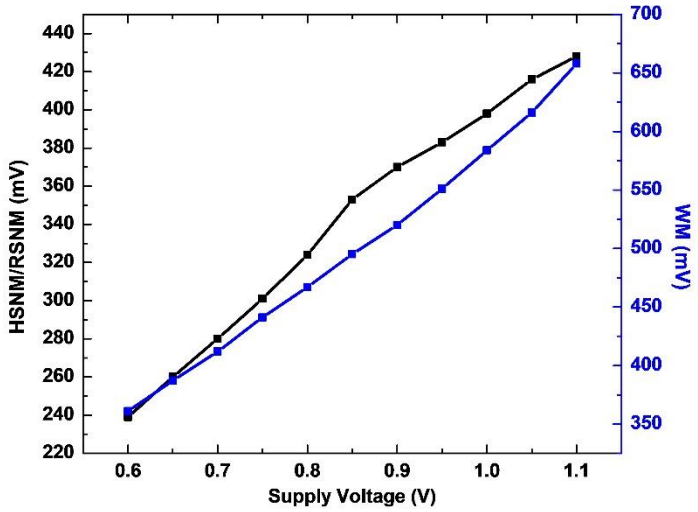
Cell topology also plays a key role in determining current ratio. Differential cells have a high read current, but they also tend to have high leakage, as a result their current ratio is

poor. While single ended cells have a low leakage current and if the cell design is skewed to have large read current, they can achieve high value for current ratio. Similar conclusions can also be drawn from the comparative graphical comparison for current ratio depicted in Fig. 4.7.

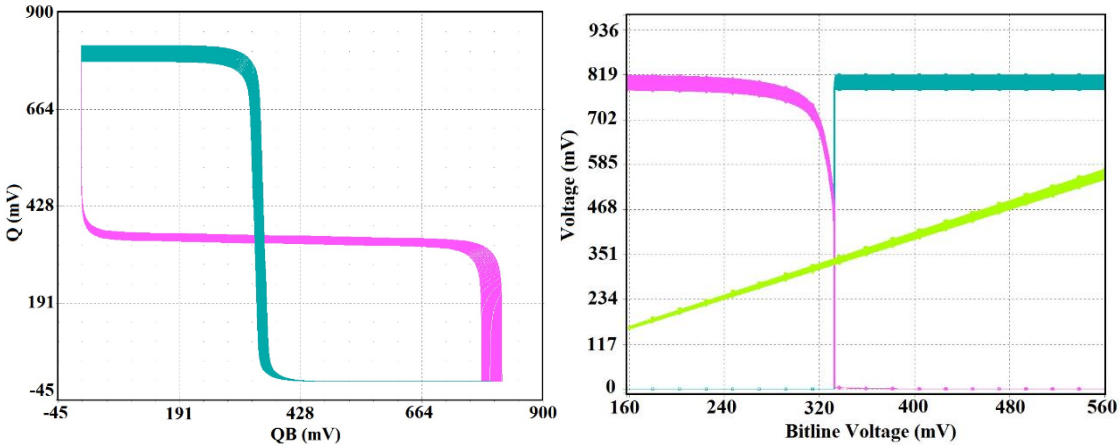
As can be observed from Fig. 4.7, the current ratio obtained for 7TAs, 7TAh, 7TC, and 7TR, is below 100. The aforementioned cell configurations except 7TR, are differential in nature and consequently they have high leakage (as will be explained in subsequent section) resulting in poor current ratio. While the highest current ratio values are obtained for 7TP and 7TS at above 105 levels. Both the cells – 7TS and 7TP are of single ended read configuration. The current ratio value for single ended single port cells - 7TK, 7TRt, and 7TY cells is approximately 5000; a fairly high value for the configuration.

4.4.5 Voltage Variation Analysis for Proposed Dual Port 7T Cell

The impact of V_{DD} scaling on the performance of the different bit cell is detailed in section 4.4.1; it is inferred in the section that the proposed bit cell maintains a reliable performance for V_{DD} scaling. But there the value for V_{DD} is increased in step size of 0.2 V. To analyze the impact of voltage variation at more detailed level, initially the impact of V_{DD} varying from 0.6 to 1.1 V in steps size of 0.05 is depicted in Fig. 4.8 (a). The static margin for cells registers a steady increase as the V_{DD} increases. Thereby, justifying the finding of section 4, that the cell has reliable performance.



(a)



(b) (c)

Fig. 4.8 Variation in the static margin for the 7TP SRAM bit cell with variation in supply voltage, (b) HSNM (RSNM) butterfly curve, and (c) WM measurement for V_{DD} variation of 0.04 mV for the proposed 7TP SRAM bit cell.

Also, in a digital circuit, it is extremely difficult to supply precise voltage, as the signal may vary slightly due to noise and other external factors. Therefore, to analyze the impact of minor voltage variation, the cell is analyzed for variations in V_{DD} ranging from 0.75 V to 0.85 V. This is done to understand the impact of minor voltage variations on the performance of the bit cell. The HSNM/RSNM, and WM curve for the 7TP cell for voltage variation are depicted in Fig. 4.8 (b), and (c) respectively.

The SNM for the cell registers a 0.2 mV change for every 1mV change in V_{DD}. Whereas, the WM for the 7TP cell registers a change of 0.25 mV per mV change in V_{DD}; this can also be inferred from Fig. 4.8 (c). This analysis helps us to establish that for minor variations in the V_{DD}, the proposed cell has negligible change in its static performance.

4.4.6 Temperature Variation Analysis for Proposed Dual Port 7T Cell

Electronic devices are subject to varying temperature ranges due to internal heating and external environmental conditions. Therefore, it is imperative to analyze the performance of a cell for varying temperature range. Thus, the static performance for each cell is analyzed by varying temperature from –10 ºC and 110 ºC. The results for each operation are individually analyzed in the following sub-sections.

During the hold operation the cell is in a static condition and the increase in temperature experienced by the cell is a consequence of external factors. The variation in HSNM/RSNM

and WM values for the proposed cell with temperature is depicted in Fig. 4.9 and 4.10 respectively. The 7TP cell has the least variation in performance with temperature variation with 0.15 mV/ºC. Thus, making the cell robust against temperature variation. The other bit cells that showcase resilience to variation in temperature are 7TR, 7TSa, 7TAs, and 7TO with their HSNM variation being less than 0.2 mV/ºC.

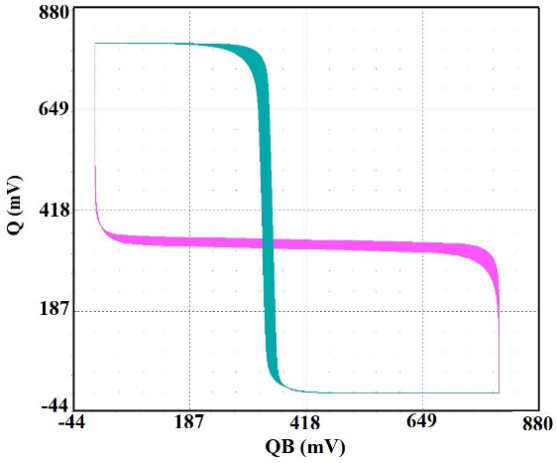


Fig. 4.9. The temperature analysis for HSNM/RSNM for the proposed 7T SRAM cell

The 7TT, 7TG, 7TS, 7TGi, 7TL, 7TAh, 7TC, and 7TAn cells have a slightly less resilience to temperature variation as their HSNM variations lies between 0.2 and 0.3 mV/ºC. The 7TL, 7TK, and 7TY have HSNM variation of 0.3, 0.32, and 0.46 mV/ºC, thereby making their performance less reliable with temperature variation. The cell with the highest HSNM variation in correspondence to the temperature variation is the 7TA with 0.725 mV/ºC. The comparison of variation in static margin values for all the bit cells is illustrated in Fig 4.9.

During the read operation, the cell is placed under vulnerable condition as the bitline discharge to identify the stored data. The cells with HSNM equivalent to the RSNM, register the same variation in their RSNM value as the HSNM variation with varying temperature. Therefore, the 7TP bit cell also have RSNM (HSNM) variation equal to the HSNM variation of 0.15 mV/ºC, as depicted in Fig. 4.9. The other cells have a slightly higher RSNM variation with respect to HSNM. This is attributed to the vulnerability the cell is exposed to during the read operation.

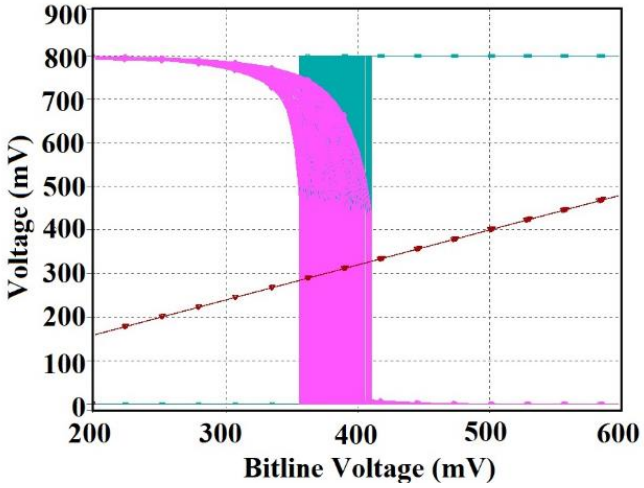


Fig. 4.10. The temperature analysis for WM of proposed 7T SRAM bit cell.

The same can be observed for 7TGi, 7TA, 7TAs, and 7TO with their variation in RSNM being 0.225, 0.15, 0.225, 0.24, 0.24, and 0.35 mV/ºC, respectively. The comparison for the same is presented in Fig. 4.11. These are the cells that are not the best choice for an application experiencing high temperature variations. While the cell that shows least variation with temperature is 7TSa. But owing to its poor SNM performance this cell is not viable. The bit cells 7TT and 7TY have a reasonable SNM and show fairly low variation with temperature at 0.158 and 0.15 mV/ºC.

As explained, the WM metric for a bit must be balanced for a successful write operation. If it is too low or too high the error vulnerability for the cell increases. The variation in the WM for the proposed 7T cell is depicted in Fig. 4.10. While the comparison of variation in WM for all the 7T cells along with the proposed cell is given in Fig. 4.11. The cell with the least variation in WM is 7TK with 0.084 mV/ºC. But the static WM value for the bit cell is low and it further reduces the WM. Therefore, even though the variation is low the performance is non-satisfactory.

The 7TAs and 7TR are the other two cell with low variation of 0.14 mV/ºC. But their WM values are extremely high; in the vicinity of 550 mV. Thereby, making the cells highly susceptible to noise. The next in line is the 7TP cell with the variation of 0.24 mV/ºC, depicted in Fig. 4.11. The cell also has a balance WM (as justified in previous section), thus verifying the reliability for the bit cell against temperature variation. The cells with comparable temperature variation performance to the 7TP cell are 7TL, and 7TO. The variation in their performance is 0.275, and 0.26 mV/ºC, respectively. Also, their static WM

value at room temperature is very balanced, making them reliable cells against temperature variation.

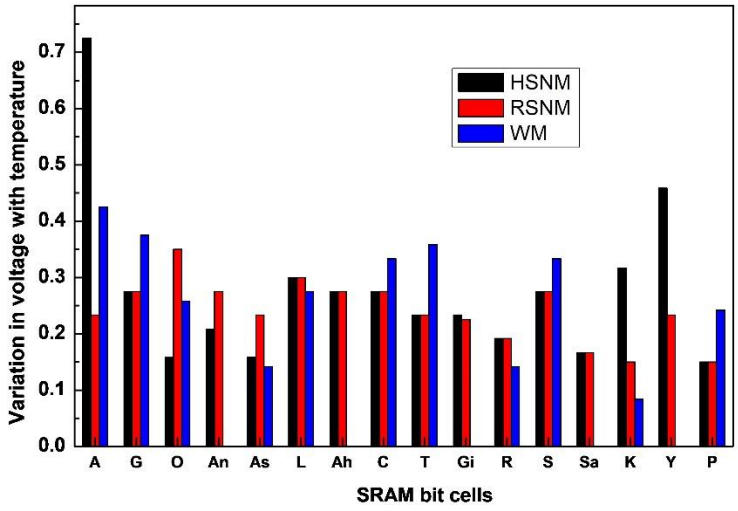


Fig. 4.11 Comparison for variation in static performance with temperature for all the SRAM bit cells.

The bit cells - 7TT, 7TG, 7TS, and 7TC have a high variation in comparison to the 7TP cell as their variation is beyond 0.3 mV/ºC. But the 7TA registers the maximum variation of all at 0.425 mV/ºC. The variation obtained in the performance of each bit cell for hold, read, and write operation is compared in Table 4.2.

4.4.7 Global Variation Analysis for Proposed Dual Port 7T Cell

During fabrication process for most inorganic devices' attributes such as discrete random dopants, oxide thickness, line edge roughness, strain variation led to process variations in the cell [144]. These variations are more dominant in scaled technology devices and result in significant component mismatches. Thus, SRAM being an area constrained circuit is highly impacted by such process variations. Therefore, process corner analysis analyzes the effect of global variation on each cell's performance. The comparative analysis for the HSNM, RSNM, and WM for each bit cell at slow-slow (SS), fast-slow (FS), slow-fast (SF) and fast-fast (FF) corner are presented in Fig. 4.12, 4.13, and 4.14, respectively. The global variation analysis for the hold operation tests the reliability of bit cell if a mismatch in the fabrication devices is registered. The HSNM values at the four corners are compared in Fig. 4.12.

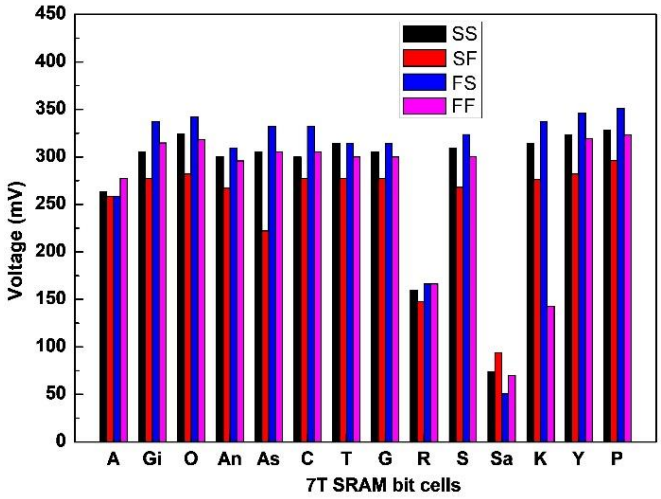


Fig. 4.12 Comparison for HSNM at SS, SF, FS and FF corner for all 7T SRAM bit cells.

The best performance for most cells is achieved at the FS corner; as the NMOS becomes slow, while the PMOS becomes fast, thereby bridging the gap between the performances of the two devices. The cell with the best FS performance is the 7TP cell. The 7TGi, 7TAh, 7TC, 7TK, and 7TY have their HSNM performance comparable to 7TP at this corner. While the corner that registers the weakest performance for most bit cells is SF.

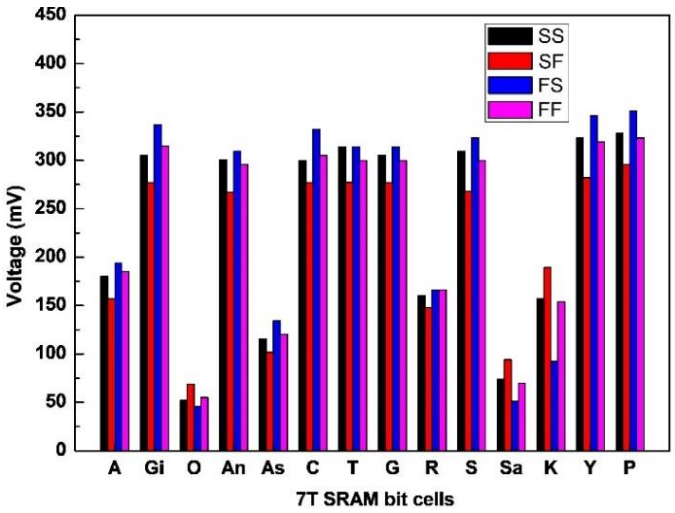


Fig. 4.13 Comparison for RSNM at SS, SF, FS, and FF process corner for the 7T SRAM bit cells.

But at the SF corner as well, the 7TP cell has the highest value for HSNM. The HSNM values for the cell at the different process corners are compared in Fig. 4.12. In terms of the variation in HSNM values, the cells with minimum variation are 7TT and 7TG with a variation of 37 mV. The 7TP cell is next in line with the variation of 44 mV. The high HSNM value for the 7TP bit cell helps outshine its slightly higher HSNM variation. Few other cells

with low HSNM variation with global variations are 7TA, 7TR, and 7TSa, but their inferior HSNM values make them unreliable. All the other bit cells have variation greater than 55mV; of them the highest variation is observed for 7TK and 7TAh with variation of 194 and 110 mV, respectively.

Table 4.2 Comparison of results for all the 7T SRAM bit cells for various evaluation parameters.

SRAM cells	Static Analysis			Temperature Variation			Global Variation			Power Consumption		
	HSNM (mV)	RSNM (mV)	WM (mV)	HSNM (mV/ºC)	RSNM (mV/ºC)	WM (mV/ºC)	HSNM (mV)	RSNM (mV)	WM (mV)	Hold (pW)	Read (µW)	Write (µW)
7TA	304	184	440	0.723	0.23	0.425	18	37	90	166	18	0.053
7TGi	314	46	-	0.23	0.225	-	60	60	-	292	26	2.46
7TO	324	70	266	0.16	0.35	0.26	60	32	101	240	18	4.32
7TAn	139	92	-	0.21	0.275	-	-	-	-	456	14	5.44
7TAs	319	102	551	0.16	0.23	0.14	-	-	-	540	31	7.84
7TL	310	310	390	0.3	0.3	0.275	42.5	42.5	79	846	30	1.76
7TAh	310	310	-	0.275	0.275	-	110	32.4	-	1128	30	0.24
7TC	310	310	340	0.275	0.275	0.34	55	55	82	865	36	3.6
7TT	324	324	398	0.23	0.23	0.36	37	37	80	240	12	2.97
7TG	324	324	336	0.275	0.275	0.375	37	37	110	652	5	2
7TR	166	166	551	0.19	0.19	0.14	18.5	18.5	50	880	14	3.76
7TS	314	314	312	0.275	0.275	0.34	56	56	105	259	30	2.74
7TSa	84	69	-	0.17	0.17	-	43	43	-	952	3	12.96
7TK	310	138	330	0.32	0.15	0.084	194	97	279	780	1	5.6
7TY	287	89	-	0.46	0.23	-	64	64	-	196	1.68	2.14
7TP	324	324	488	0.15	0.15	0.24	44	44	50	256	6	1.9

The read operation subjects the cells to vulnerability. Therefore, variation analysis for read operation highlights the cells that experience higher reliability issues. The cells that register a very low performance in terms of static RSNM are 7TR, 7TSa, 7TAh, and 7TK. Therefore, the variations for these cells are not accounted for. Amongst the remaining cells, the 7TT, 7TG, 7TO, and 7TP cells are the cells with the least variation in performance at 37, 37, 44 and 32 mV, respectively. Whereas, the highest performance variation is recorded for 7TY and 7TGi at 64 and 60 mV, respectively. The comparison for RSNM values at process corners for the cells is presented in Fig. 4.13.

The write operation is highly vulnerable for both differential and single ended cells. The WM should not experience too high a variation; it increases the error probability for the bit cell. The cells with the minimum variation in WM values due to global variation are 7TR and 7TP at 50 mV each. Thus, validating that the chances of these two cells registering a write failure a considerably less.

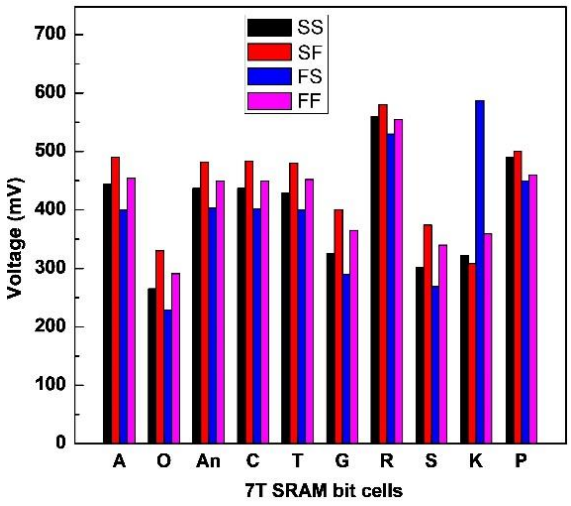


Fig. 4.14 Comparison for WM at SS, SF, FS, and FF process corner for all the 7T SRAM bit cells.

The WM variation is slightly higher for 7TT, 7TA, 7TL, and 7TC at 80, 90, 79, and 82 mV, respectively. While 7TO, 7TG, 7TS and 7TK cells have significantly high variation of 101, 110, 105, and 279 mV, respectively. The WM values at the four process corners are depicted in Fig. 4.14. The variation in performance of each bit cell caused by the global variations is tabulated in Table 4.2.

4.4.8 Local Variations Analysis for Proposed Dual Port 7T Cell

The increasing dependence on scaled technology node has improved bit cell density, but it has exposed the cell to local mismatch variations. In the previous section, it was established that the proposed cell demonstrates robust performance against other cells in terms of global variations. To ensure that the cell is also robust against local variations, it is evaluated using MC simulations. The MC simulations are performed using statistical techniques to identify the extent of variation in performance of a cell due to local variations. V_{TH} is presumed to be the key parameter for the analysis, with an independent Gaussian distribution of 6σ around the mean V_{TH} value of the device.

This technique is also utilized by references [81, 167] to evaluate the performance of their cells. This technique varies V_{TH} around its mean value in the 6σ range. The simulations results for static margin – HSNM/RSNM, and WM, for 7TP cell due to local variation are given in Fig. 4.15 (a), and (b) respectively. The results highlight that the HSNM (RSNM) may reduce to 258 mV (66 mV lower than the HSNM value for the cell at typical corner), while WM rise to 501 mV (13 mV higher than WM at typical corner) for maximum local

variations. This variation in static margins is the maximum deviation within which the 7TP cell may operate due to local variations.

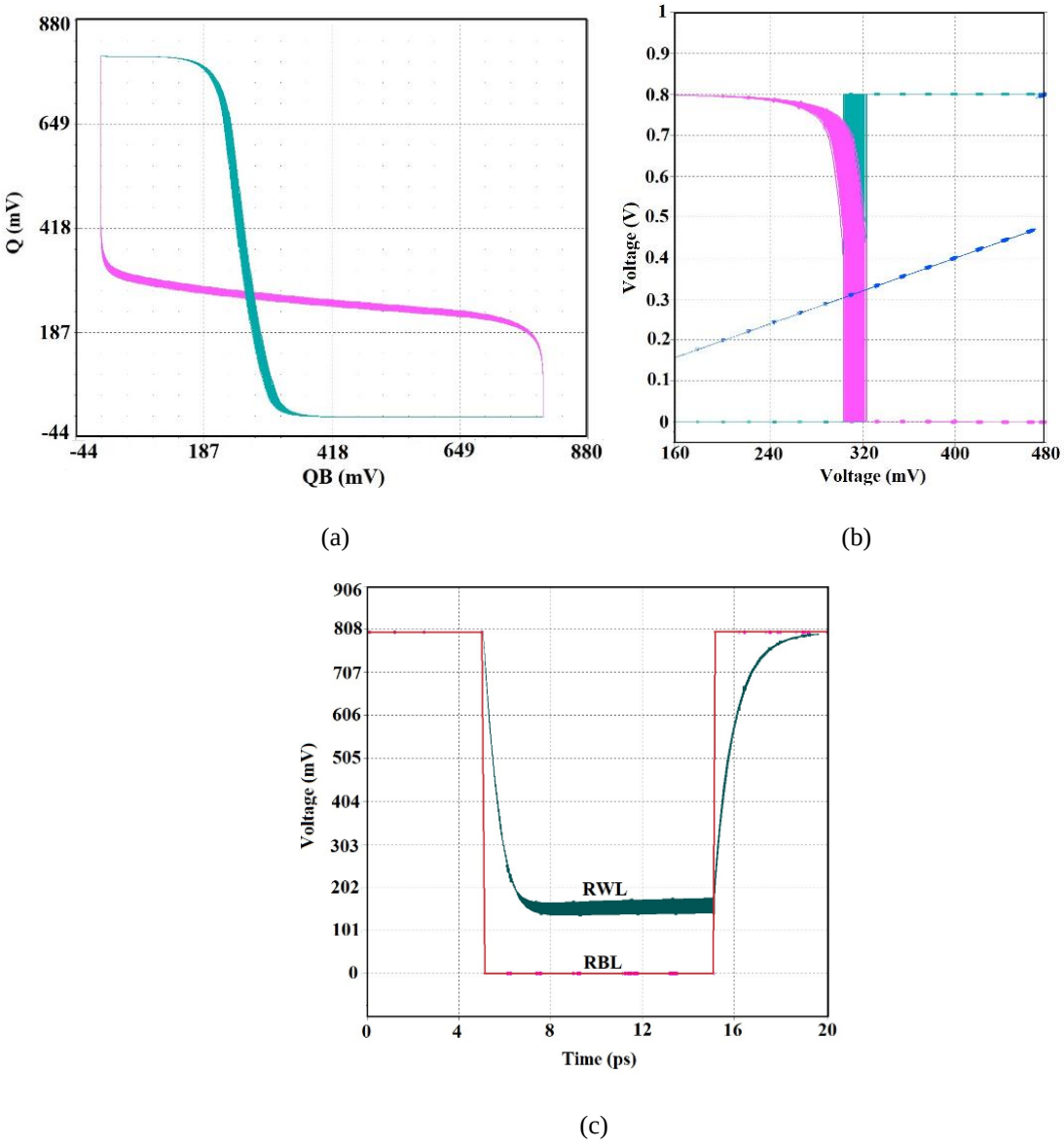


Fig. 4.15. MC simulation for results during the (a) hold (read) operation, (b) Write operation for 7TP bit cell, and (c) Read discharge current for Q = '1' at the worst corner using 10,000 Monte Carlo simulations.

The proposed cell has single ended topology, therefore during the read operation the read discharge event occurs only for Q = '1' (QB = '0'). Whereas, for Q = '0' (QB = '1') the N4 transistor in the proposed 7T cell remains OFF and no discharge event is registered. Consequently, a decline in RWL voltage is registered for Q = '1' (whereas, Q = '0' the voltage level at RWL is maintained high only). To demonstrate the resilience of the read operation for the proposed 7T cell, it is evaluated at the worst process corner for 10,000 MC

simulation. The simulation result for the same is demonstrated in Fig. 4.15 (c). As can be observed for Fig. 4.15 (c), when the RBL signal is set '0', the RWL value discharges, because of the read discharge event. Whereas, when the RBL is again set high, the RWL signal reverts to its original state.

SA is a crucial component of the peripheral circuitry for an SRAM based memory. Bit cells are arranged to form an array and the end of each column in the array is connected to a SA. The utility of the SA is to enable the circuit to perform the read operation. The proposed cell employs a single ended read topology; therefore, a single bitline enabled SA is preferential. A single ended - latch type SA is a popular choice for single ended, low power application [168]. The voltage-based latch type SA senses the voltage difference between the bitline and the reference voltage level; the output is generated based on the comparison. Another SA topology that may be employed with the proposed cell is the pseudo differential sensing [120, 169]. This can sense data even with a smaller bitline swing [119].

4.4.9 Half Select and Soft Error Resilience of the Proposed Dual Port 7T Cell

The SNM analysis and timing analysis establish the stability of a particular bit cell during a given operation. But when a bit cell in the SRAM array gets selected there are other cells in the same row and column that get HS. So, when a read/write operation is executed, these half-selected cells may register an unintentional read/write operation. This false event registered by a half-selected cell is referred to as half-select (HS) disturbance [148, 142]. So, it is imperative to ensure stability of the half-selected bit cells. HS disturbance is a drawback prevalent in shared wordline bit cell architectures [141]. Therefore, to avoid HS disturbance, it is essential that access transistors are controlled via exclusive row and column signals [154].

The pre-existing bit cells that have reported a HS disturbance free operation are 7TC, and 7TG. Of the other bit cells, the 7TGi, 7TAn, 7TAs, and 7TO cells are prone to both read and write HS disturbance. While the 7TL, 7TAh, 7TT, 7TR, 7TS, 7TK, and 7TY predominantly experience a write HS disturbance. To enable the 7TP cell to be HS free it is designed to have independent row and column-based signals. The RBL and RWL signal form the row and column-based signals for read operation; whereas during the write operation, the intersection of WWL and WWLB activates the desired cell only and the half-selected cells do not register any HS disturbance. Thus, enabling the 7TP cell HS disturbance free. The

elimination of HS disturbance and read-write conflict [170] from the 7TP cell establishes the performance reliability for the cell.

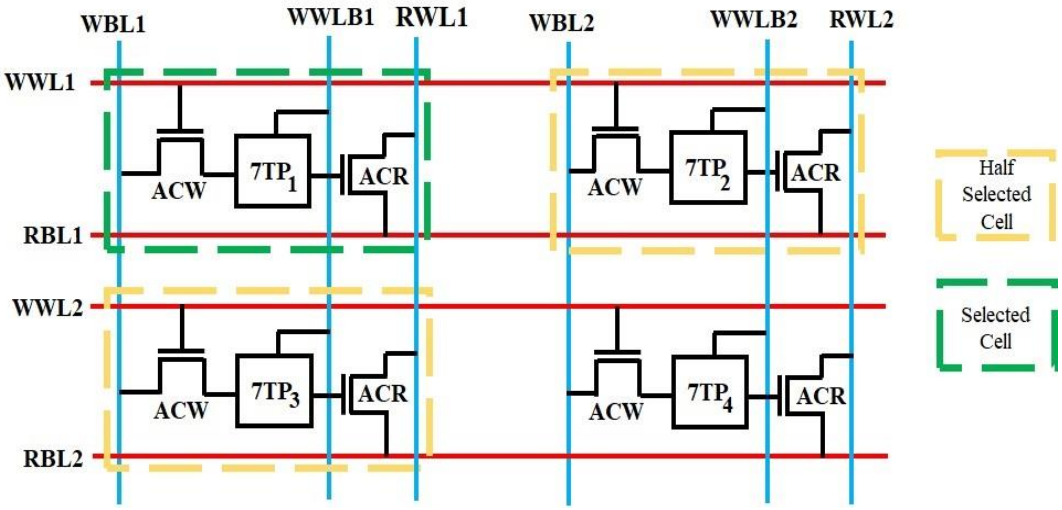


Fig. 4.16 A 2×2 array for the proposed 7TSE SRAM bit cell to depict the half-selected cells in an array when an SRAM bit cell is selected.

To further illustrate the HS resilience of the 7TP against HS disturbance. A 2×2 array for the 7TP cell is simulated to evaluate the performance of the cell against HS condition. A representation of the 2×2 array for the proposed cell is depicted in Fig. 4.16. At a given instant of time, only one cell in the array gets selected. While cells in the same row and column as the selected cell gets HS. Here the selected cell is undergoing write operation and the control signals are assigned in keeping with signal status in 4.1. Ideally, the HS cells are not a part of the on-going operation, but due to common control signal for row or column, they get partially selected [171]. The SNM curve for the half-selected cells are depicted in Fig. 4.17 (a) and (b).

The $7TP_2$ is in HS condition as WWL1 signal is high, this may trigger a write operation in the cell, but the high condition on WWLB2 does not allow for the same. Thereby, preserving the integrity of $7TP_2$ under HS condition. It may though result in a discharge current if potential difference is present between the two ends of the N3 transistor for $7TP_2$ cell. Consequently, the HSNM value for the $7TP_2$ cell under HS condition may get reduced to 277 mV; the same is depicted in Fig. 4.17 (a). To ensure that even when the cell is operated at the worst corner, its performance is retained. The SNM curve is also obtained for 10,000 MC simulation, as depicted in Fig. 4.17 (c).

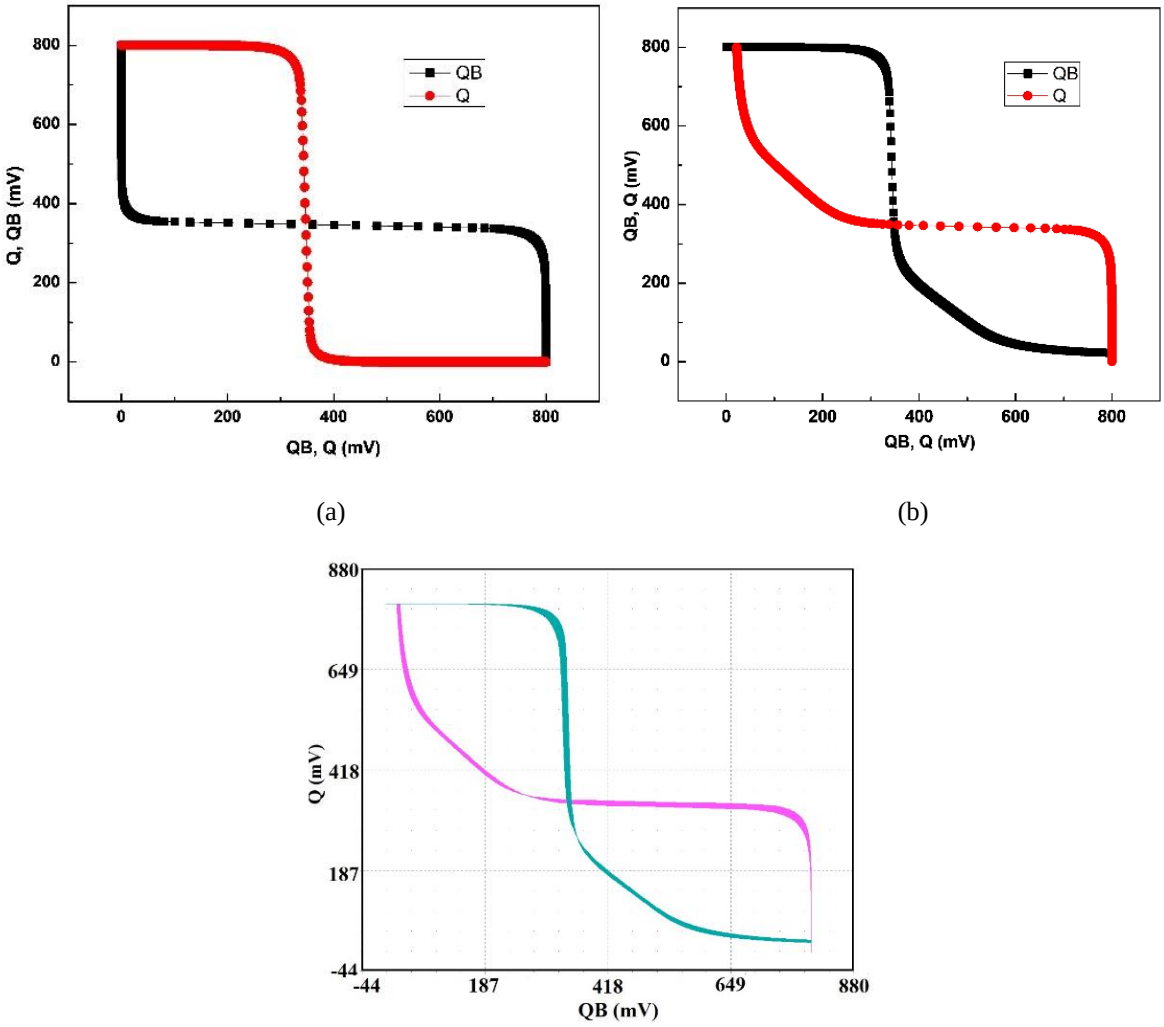


Fig. 4.17 (a) Butterfly curve for $7TP_2$ half selected cell, (b) butterfly curve for $7TP_3$ selected cell, and (c) 10,000 Monte Carlo simulation for butterfly curve for $7TP_2$ cell at the worst corner.

While for $7TP_3$ cell, the disconnection of the feedback between the inverter couple leads to a floating condition for date node for the cell. But there is no discharge current path in the cell to manipulate the data, thus preserving the data in the cell for HS condition. Consequently, the SNM curve for the $7T_3$ HS cell (depicted in Fig. 4.17 (b)) is identical to the SNM curve depicted in Fig. 4.4 (a). Thus, 7TP cell may be deemed resilient to HS disturbance. The read operation is initiated by setting the RWL signal high and the RBL signal low. So, when the data stored at node Q = '1', the RWL will discharge via the R1 transistor to RBL.

This implies that the current will discharge from RWL to RBL. In this situation the cells that get HS for the read condition are the cells in the same row. The column cells do not get HS

as the RWL signal (common to a column) is maintained at high throughout the operation, only the RBL signal (common to a row) is turned low for the duration of read operation. Therefore, in the worst-case situation even if all the half-selected cell has 1 stored in their Q data node, the possibility for an erroneous read is low.

Each column at the bottom is attached to a dedicated SA to complete the read operation. These SAs have an enable signal, which is only turned ON when the SA is expected to perform the read operation. Consequently, even if a HS cell results in an unintentional read discharge current, the SA will not be activated and read operation will not occur. Soft errors are caused in a bit cell due to α-particle or speeding cosmic neutron. The effect of soft errors is pre-dominantly noticed in scaled circuits with nanometer technology node. The α-particle or speeding cosmic neutron, due to direct or indirect ionization creates an additional charge in the circuit. This may cause voltage transition from one level to another [147]. This accidental flip in the data due to α-particle or speeding cosmic neutron is referred to as soft error [149].

Usually, soft errors occur in burst, impacting consecutive bit cell. Therefore, to ensure a cell's reliability against soft error, various researchers [81, 152, 56] have reported BI as an effective method. In BI continuous bits of a single word are segregated by placing them separately. Therefore, employing BI technique to design array architecture for the 7TP cell will make the cell resilient to soft errors. HS free operation is necessary to implement BI architecture for the SRAM array. BI implementation for a single ended write is limited by HS disturbance [137]. But as the 7TP cell is HS disturbance free, it supports BI architecture, thereby enhancing its soft error immunity.

It is also reported that process and temperature variations add to soft error susceptibility of a cell [151]. Consequently, the 7TP cell is analyzed for process and temperature variations. The process variation analysis reveals that the cell registers a variation in values of HSNM/RSNM and WM of 44 mV and 50 mV, respectively. Whereas, for temperature variation the variation in HSNM/RSNM and WM values for the cell is 0.15 mV/ºC and 0.24 mV/ºC, respectively. Therefore, it is valid to infer that the 7TP cell has resilience to process and temperature variation. So, in keeping with reference [150-151] we may infer that the proposed cell is reasonably resilient against soft error disturbance.

4.4.10 Power Consumption Analysis for Proposed Dual Port 7T Cell

As stated previously, cache memory utilizes a significant portion of the total power consumption for the system, as it is made by replicating a bit cell to form an array. Therefore, it is necessary to reduce the power consumption for a single bit cell. A small decrement in power of a single cell has multi-fold impact on the power performance for the entire memory block. The power consumption for a cell can be majorly divided into two categories – static power consumption and dynamic power consumption.

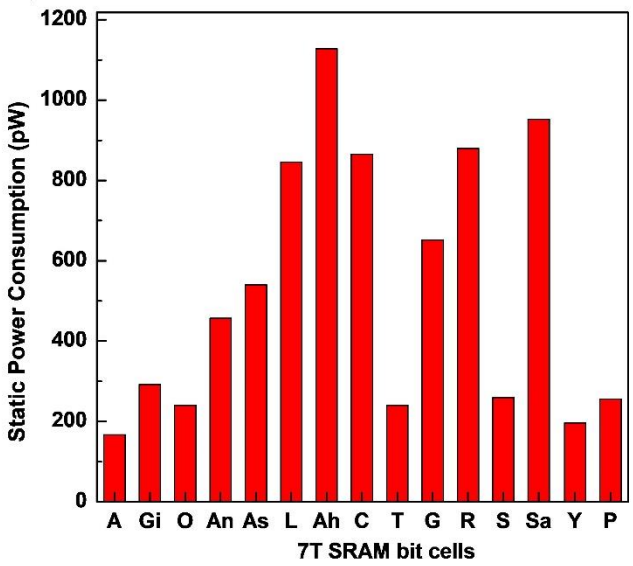


Fig. 4.18. Graphical comparison for static power consumption for the different 7T SRAM bit cell topologies.

The static power consumption is primarily caused by the leakage current in the circuit and is mathematically equal to V_{DD} times the leakage current. Whereas, the dynamic power component is further divided into read and write power consumption. The static and dynamic power consumption for all the bit cells is graphically compared in Fig. 4.18 and 4.19, respectively. The static power is found to be highest for 7TAh cell at 1128 pW; this is caused by the bitline based supply collapse for the cell and its dual port configuration. The other cells with high static power consumption are 7TL, 7TC, 7TR, and 7TSa; they are also of dual port configuration. Dual port cells; specifically, 7TL, 7TAh, and 7TC have a differential write port and a single ended read port, therefore there are multiple leakage current sources.

Consequently, the highest leakage is recorded for the differential ended with isolated read port bit cells. The leakage current for 7TP bit cell is fairly low at 256 pW; this is attributed to the write assist and read assist schemes for the cells. Unlike a conventional cell, the 7TP

cell does not depend on discharge via bitline for the write operation; consequently, it registers an incredibly low leakage power consumption. Its write assist technique is only dependent on the voltage level and not current flow, therefore resulting in better static power performance.

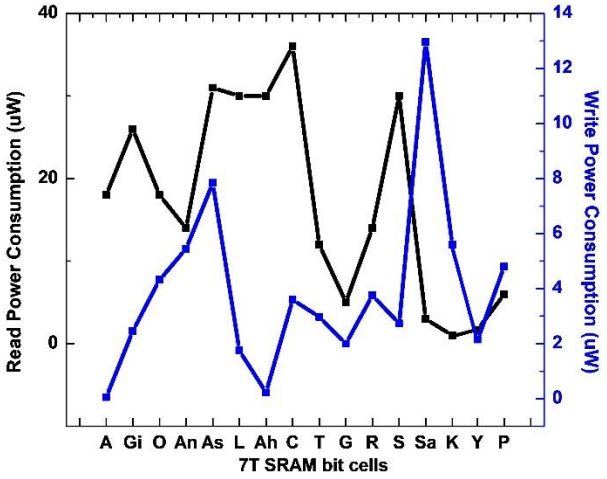


Fig. 4.19. Graphical comparison for dynamic power consumption for the different 7T SRAM bit cell topologies.

Another implication of the write assist scheme used in the 7TP cell is that it registers a low power requirement for the write operation. The 7TA cell also uses the same write assist scheme and has low write power consumption. Also, it is the only cell with differential ended single port topology with low write power requirement. All the other cells with differential ended single port scheme have high power requirement, as the cell is dependent on the discharge current for both bitlines, thereby requiring a large power requirement for the operation.

4.4.11 Area and Layout Analysis for Proposed Dual Port 7T Cell

The area that an bit cell occupies determines its economic feasibility. The cell with smaller layout area is preferred for large SRAM array formation. Thus, making the area footprint an essential performance metric for an SRAM cell. The layout for each bit cell is designed on a grid of 16 nm and based on design rules reported by Jeppson *et al.* [172]. The layout for 7TP cell is depicted in Fig. 4.20 (a) and its dimensions are mentioned alongside. The layout area for all the other 7T cells is compared in Fig. 4.20 (b). The 7TP cell occupies 0.553 μm^2 area. The other bit cells have area greater than the 7TP cell.

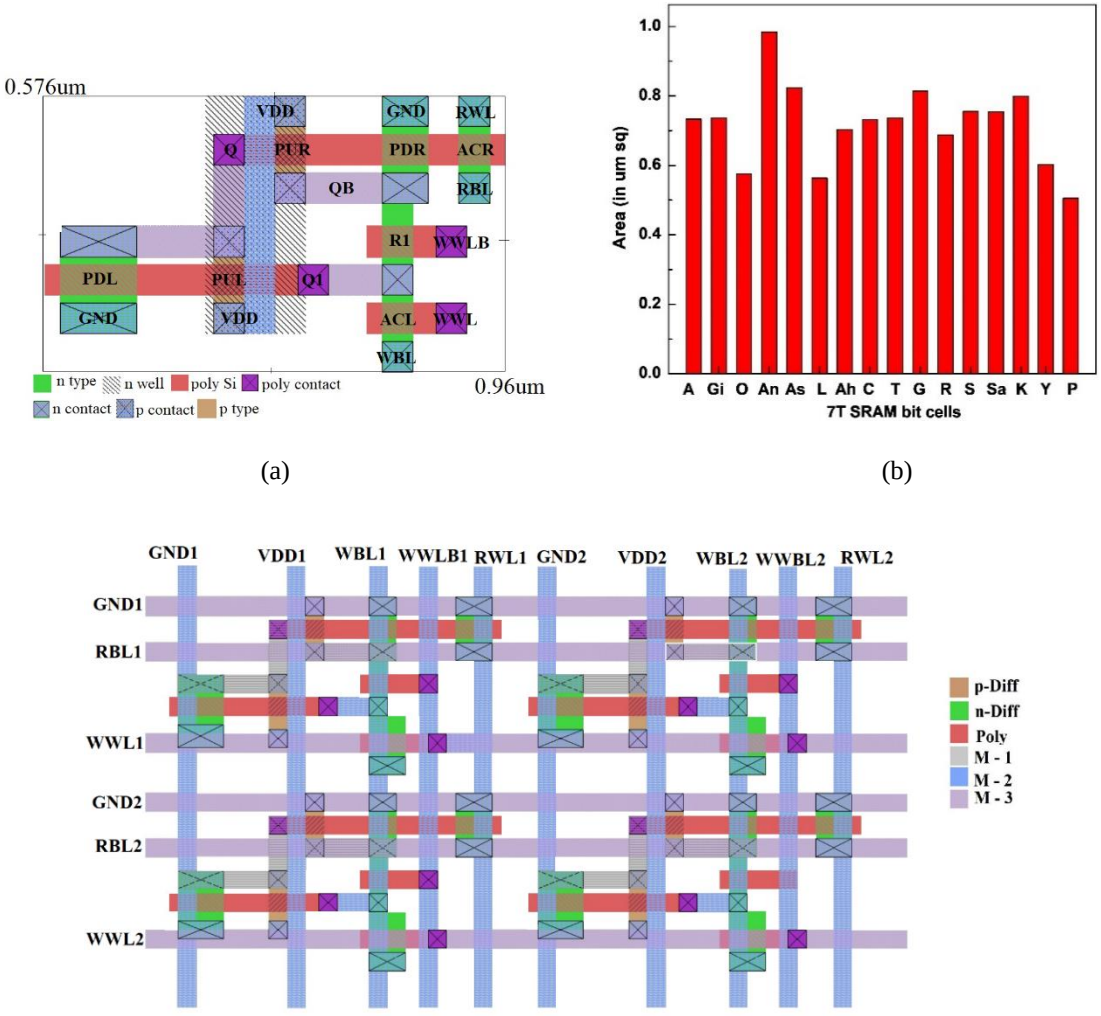


Fig. 4.20 (a) Layout for the proposed 7T SRAM bit cell, (b) Comparison of the layout area for all the SRAM bit cells, and (c) layout for 2×2 array for the 7TP SRAM bit cell.

The 7TL, 7TY, and 7TO are bit cells that have an area slightly higher than the 7TP cell, with areas being 0.563, 0.6, and 0.576 μm^2, respectively. These cells have conventional memory core and additional NMOS transistors to perform the read operation. Thus, a minimal increase in area. The 7TR cell has an area occupancy of 0.688 μm^2. Whereas, 7TAn and 7TAs cells have the highest layout area footprint. These cells modified the memory core and used a combination of HV_{TH} and LV_{TH} transistors. Thereby increasing the masking layers and spacing between transistors. The area for 7TAn and 7TAs cells are 0.984 and 0.823 μm^2, respectively. Another cell with area measurement in the same vicinity is 7TS with area of 0.814 μm^2. The area for the remaining bit cells – 7TT, 7TS, 7TGi, 7TAh, 7TK, and 7TA is 0.737, 0.755, 0.737, 0.703, 0.799, 0.733 μm^2, respectively.

The layout for the 2×2 array for the proposed 7T cell is depicted in Fig. 4.20 (c). This layout is designed to illustrate the directions for the supply lines and the control signals for the cell. As mentioned in sub-section 4.4.9, the layout for a cell needs to be designed with controls signals of each operation with independent row and column-based signals. This independence of row and column-based signals can be observed in Fig. 4.20 (c). The write operation for the cells is controlled by signals - WWL and WWLB, which are row and column based, respectively. Similarly, the row and column-based control signals - RWL and RBL respectively, are governing the read operation.

4.5 PROPOSED DUAL MODE OPERATIONAL BIT CELL

The proposed cell is composed of eight transistors of which two are PMOS (P1 and P2), while the remaining are NMOS transistors (N1- N6). The memory core for the reconfigurable cell like a conventional cell is formed by a pair of mutually connected inverters via an NMOS transistor; N3. It is used to control the connection and disconnection of mutual feedback between inverters; it is controlled using signal write wordline bar (WWLB). While the write wordline (WWL) signal controls the access transistor N4 throughout the write operation.

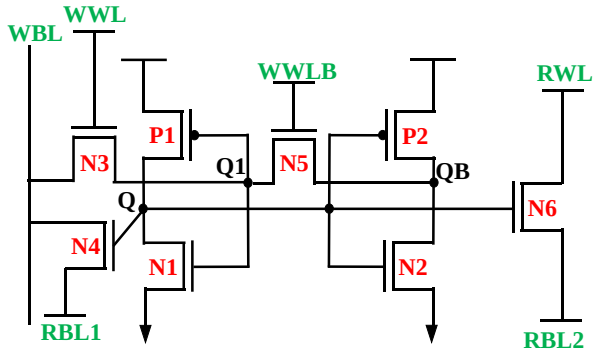


Fig 4.21. Schematic design for the proposed reconfigurable SRAM cell.

The WWL and WWLB are complementary signals thereby, making N4 and N3 operate exclusive of each other. The read operation is controlled by read bitline, (RBL1 or RBL2) signal depending on whether the single or dual port configuration is to be used, respectively. The N5 - N6 transistors are the read access transistors and operate exclusive of each other. The data is read from or written into the memory with the assistance of write bitline WBL. The schematic design for the proposed reconfigurable cell is depicted in Fig. 4.21. This

proposed configuration for the bit cell can operate in two modes; (i) single-ended, single-port and (ii) single ended, dual port. The port configuration for a cell indicates if common bitline(s) is used for both access operations or are the bitlines independent for the two operations.

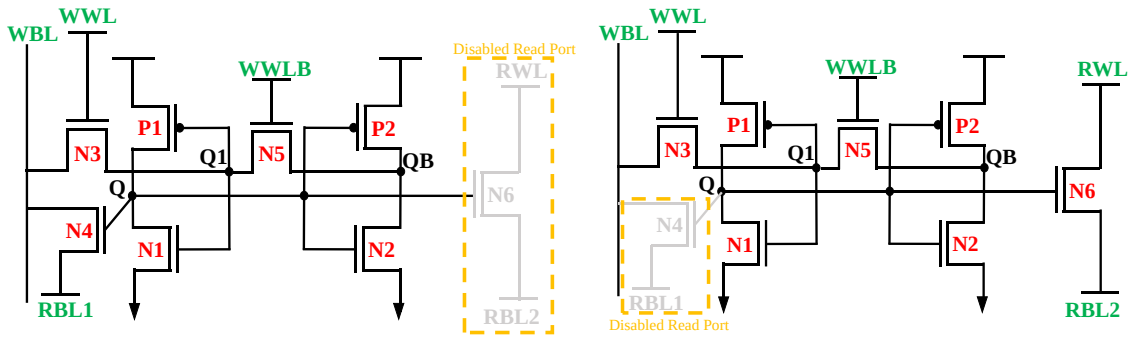
Table 4.3. The control signal conditions during the different operation of the proposed cell.

	WL	WLB	RS	RD
HOLD	'0'	'1'	'0'	'0'
WRITE	'1'	'0'	'0'	'0'
READ (SP)	'0'	'1'	'1'	'0'
READ (DP)	'0'	'1'	'0'	'1'

A single port bit cell relies on a single bitline for all its operations. Whereas, a dual port cell is dependent on two-bitlines for its operations. In the proposed cell, the control signal RBL1 for read operation ensures single port configuration and if RBL2 signal is used, then the circuit will operate in dual port configuration. For ease of understanding, the combination of control signal and their corresponding operations are listed in Table 4.3.

4.5.1. Single Port Configuration

When a device is operating at a slow pace or is in low activity and power saving mode, then the circuit must operate in single port configuration. During this configuration, the bit cell is dependent on WBL for all its operations. The RBL2 signal is low, thereby disconnecting the second read port for the cell. The effective circuit for the proposed cell during the single port configuration is given in Fig. 4.22 (a). For this configuration, the cell operation is slow with no possibility for pipelining.



(a) (b)

Fig 4.22. The effective circuit for the proposed cell when the circuit is operational in (a) single port, and (b) dual port configuration.

But use of a single ended single port configuration tends to reduce power consumption; mathematically calculated as follows:

$$P = \alpha C_L V_{DD}^2 f_{clk} \quad (4.3)$$

Here, α represents the activity factor, f_{clk} is the clock frequency and C_L is the load capacitance of the cell. For a single ended operation, the activity factor is reduced to 0.5 thereby reducing the power appetite to half of its value.

4.5.2. Dual port configuration

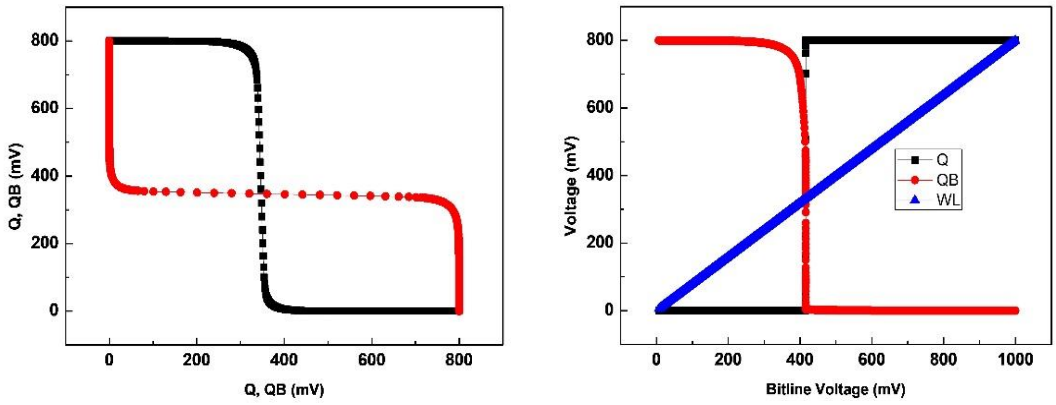
When the device is operating in a high-speed mode, i.e., the cell is required to operate with lower delay and higher speed. This scenario trades-off power with speed and is not taken as a constraint, then the cell must operate in dual port. The effective circuit for the proposed reconfigurable cell for dual port configuration is shown in Fig. 4.22 (b). The advantage of dual port is that it enables pipelining and ensures faster operation. This might increase the power load of the circuit, but the operational speed of the cell is optimum.

4.6 PERFORMANCE ANALYSIS OF DUAL MODE OPERATIONAL CELL

The proposed cell is designed at 32 nm and is simulated at V_{DD} of 0.8 V. The different parameters used to evaluate the proposed reconfigurable cell are SNM, timing requirement for access operations (read and write), and PVT variation. The performance of the proposed reconfigurable cell for each of the aforementioned parameters is explained in the subsequent sub sections.

4.6.1 Static Noise Margin Analysis for Dual Mode Operational Cell

The primary utility of a memory cell is to retain information as long as V_{DD} is applied to the cell. Therefore, the proposed reconfigurable cell is first analyzed for SNM, for its three operations - hold, read, and write. The performance is initially analyzed for ideal static condition. The hold, read, and write SNM values obtained for the proposed reconfigurable cell are 333, 333, and 470 mV, respectively. The butterfly curve (hold/read operation) and WM curve are depicted in Fig. 4.23 (a) and (b) respectively.



(a) (b)

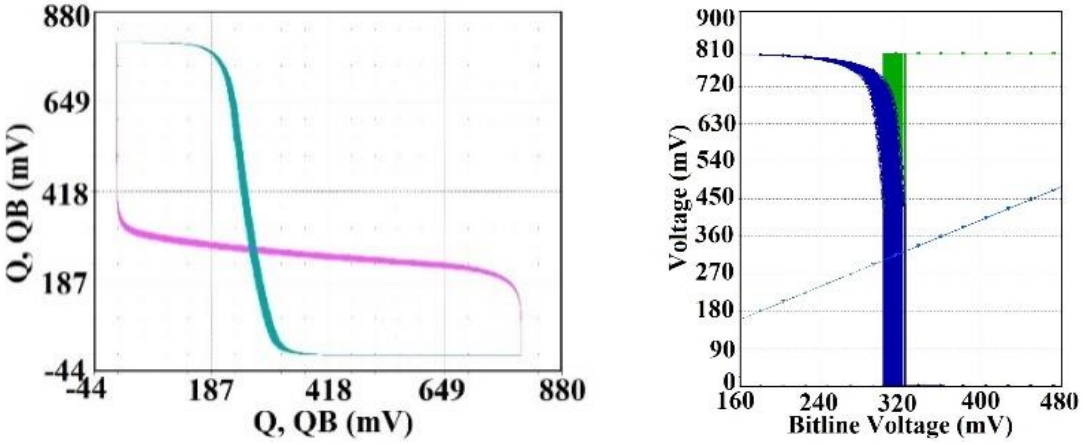
Fig. 4.23 (a) Butterfly curve for hold (read) operation, and (b) Write margin curve for the proposed reconfigurable cell.

As expected, overlapping butterfly curves are obtained for read and hold operation. The read port (for both single port and differential) is designed to exclude the data node from the read discharge path. This configuration helps protect the integrity of the data stored in the cell. Thus, during the read operation, the data stored at node Q is not disturbed resulting in HSNM value of the cell equal to its RSNM value. The HSNM (RSNM) value for the proposed cell is 333 mV, while the WSNM value for the cell is 470 mV. The SNM values obtained for the cell are balanced and lie around the ideal value of $V_{DD}/2$ [80]. But when the memory is fabricated, imperfections in the cell may arise due to different process variables. These imperfections become more prevalent at lower technology nodes. The different factors that impact a cell's performance and threaten stability are local and global variations caused due to fabrication imperfections.

4.6.2 Local Variation Analysis for Dual Mode Operational Cell

The simulation results for the proposed cell demonstrated in the previous sub section are all performance for ideal conditions. But when a circuit is fabricated, there are possibilities of minor fabrication imperfections resulting in local mismatch in the transistors adjacent to each other. This results in deviation from the performance reported for the cell. Thus, it is essential to evaluate the impact of local variation on the performance of the proposed cell. As previously stated, these local variations are due to fabrication imperfections and impact the V_{TH} for the bit cell. Thus, V_{TH} is used as the main parameter to statistically analyze the same [81, 167]. MC simulation determines the degree of variation in performance of the

proposed cell. The V_{TH} for the cell varies around the average value with 6σ standard deviation to determine the worst-case performance of the proposed reconfigurable bit cell. The simulation results for the MC simulation for the proposed cell for HSNM (RSNM) and WM are depicted in Fig. 4.24 (a) and (b), respectively.



(a) (b)

Fig. 4.24 Results of local variation for (a) HSNM (RSNM), and (b) WSNM values for the proposed reconfigurable cell.

The 6σ worst case HSNM, RSNM, and WSNM values achieved for the reconfigurable cell are 273, 273, and 540 mV, respectively. Thus, the variation in HSNM, RSNM and WSNM values for the proposed cell are 60, 60, and 70 mV, respectively. From the local variation analysis, this may be concluded that though there is variation in performance of the bit cell, it is within reasonable bounds. Therefore, it is apt to suggest that the cell has low vulnerability to local variation.

4.6.3 Global Variation Analysis for Dual Mode Operational Cell

The impact of global variation on a cell is determined using the process corner analysis. The proposed cell is therefore analyzed at the four processes. The SNM values obtained for the proposed cell at all the process corners are graphically compared in Fig. 4.25. The values obtained at each corner are also tabulated in Table 4.4.

The best performance for the cell is recorded at the FF corner. This is an implication of improved performance for both NMOS and PMOS at the FF corner. The HSNM, RSNM, and WSNM values obtained at the FF corner for the proposed cell are 340, 340, and 455

mV, respectively. Similarly, at the FS corner, the performance of PMOS is improved, while that of NMOS deteriorates. Consequently, the performance of the proposed reconfigurable cell is weakest at the FS corner with the HSNM, RSNM, and WSNM being 287, 287, and 491 mV, respectively.

Table 4.4 SNM values for the proposed reconfigurable cell at all process corners.

	TT	FF	SF	FS	SS
HSNM	333	340	324	287	352
RSNM	333	340	324	287	352
WSNM	470	455	450	491	488

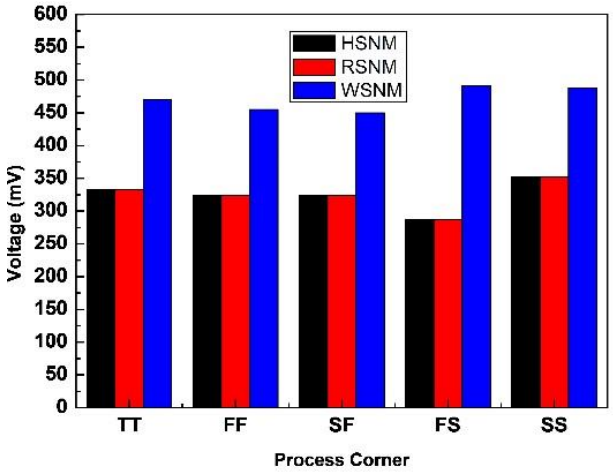


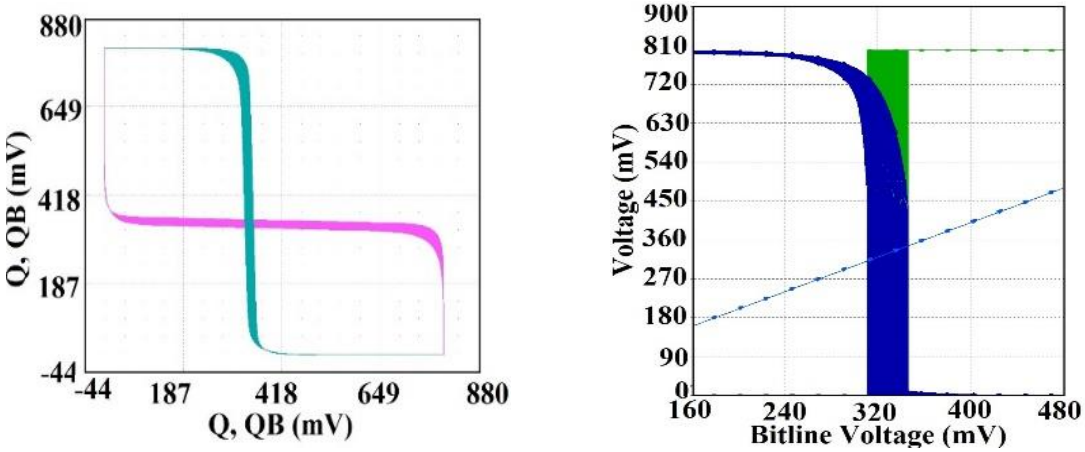
Fig. 4.25 Graphical comparison of the SNM values obtained at the different process corner for the proposed reconfigurable cell.

The essence of the global variation analysis is to determine the variation in range of SNM values. The range for SNM variation is the difference between the highest and lowest value obtained. Thus, the maximum deviation in the HSNM, RSNM, and WSNM values due to global variation is 53, 53, and 37 mV, respectively. Thus, the proposed reconfigurable cell may be deemed resistant to global variation as it registers a minor change in its performance due to global fabrication imperfections.

4.6.4 Temperature Variation Analysis for Dual Mode Operational Cell

To evaluate robustness of the proposed cell against temperature variation, its static performance is analyzed for -10 ºC to 110 ºC. The variation in HSNM/RSNM and WSNM

curves for the proposed reconfigurable cell against temperature variation is depicted in Fig. 4.26 (a) and (b) respectively.



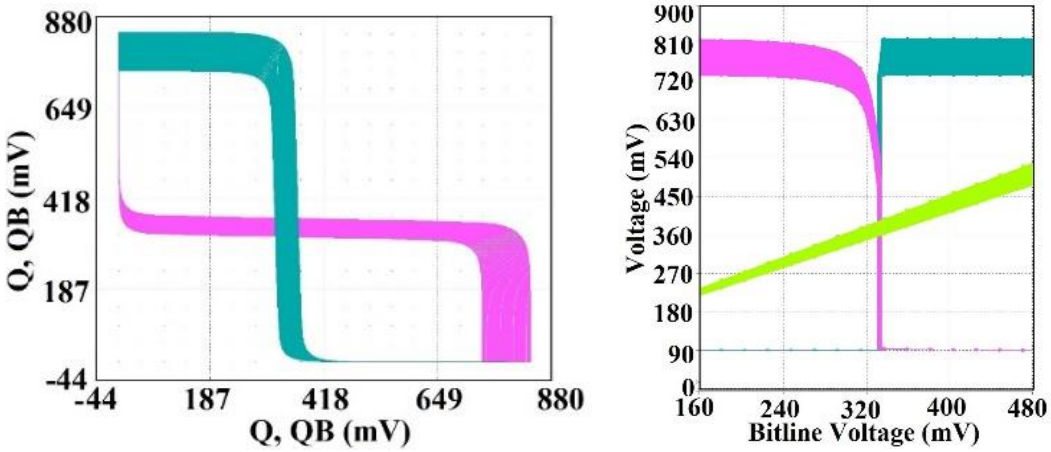
(a) (b)

Fig. 4.26 Variation in SNM for (a) hold (read), and (b) write operation for the proposed cell due temperature variation.

The proposed reconfigurable cell records a small variation in its performance when temperature is varied. The same may be inferred from Fig. 4.26 (a) and (b). The lowest HSNM (RSNM) value obtained for the proposed cell due to temperature variation is 308 mV. This is a 25 mV deviation from the nominal SNM value at room temperature. The WSNM value for the cell rises to 520 mV. This is a 50 mV rise from the WSNM value at 27 ºC. Thus, it may be concluded that the proposed reconfigurable cell demonstrates reasonable performance against temperature variation.

4.6.5 Voltage Variation Analysis for Dual Mode Operational Cell

For voltage variation analysis, the proposed reconfigurable cell is analyzed for ±10% of the operational V_{DD}. The influence of voltage variation on cell stability is depicted in terms of deviation in its HSNM (RSNM) and WSNM values. The simulation results for voltage variation analysis are presented in Fig. 4.27 (a), and (b), respectively.



(a) (b)

Fig. 4.27 Variation in SNM values for (a) hold (read) and (b) write operation for the proposed cell due to variation in voltage from 0.75 V to 0.85 V.

It may be observed from Fig. 4.27 that voltage variation has a larger impact on the cell performance in comparison to process and temperature variations. But the variation in cell performance is untroublesome and therefore, has no dire consequence on the performance of the cache memory.

4.6.6 Write and Read Time Analysis for Dual Mode Operational Cell

The analysis explained thus far is all static analysis and does not account for the time taken to complete the operation. But cell is a peg in a complex system on chip setup. Thus, identifying the minimal time required to perform an operation is essential for cell's performance evaluation. The write time for an bit cell is defined as the time interval between the instant when the write wordline signal is exerted and the data in the cell is reversed [81]. The proposed reconfigurable cell requires a minimum pulse of 0.14 ns to successfully perform the write operation. Both the node values attain their respective high/low level before the wordline signal is exerted low.

Another operation that is highly time dependent is the read operation for the cell. Both the read ports for the reconfigurable cell are single ended and identical in configuration. Due to its read SNM free configuration and single ended nature, the read discharge current is observed only for Q = '1', RWL = '1' and RBL1/RBL2 = '0'. For node Q = '0' the read port NMOS transistor N5/N6 (single/dual port configuration) remains OFF and no read current event is registered. The read time for the cell is estimated as the time required to lower the

voltage of the bitline to the switching voltage of an inverter [166]. The read time for the cell is identified to be 5 ps and in ideal condition is identical.

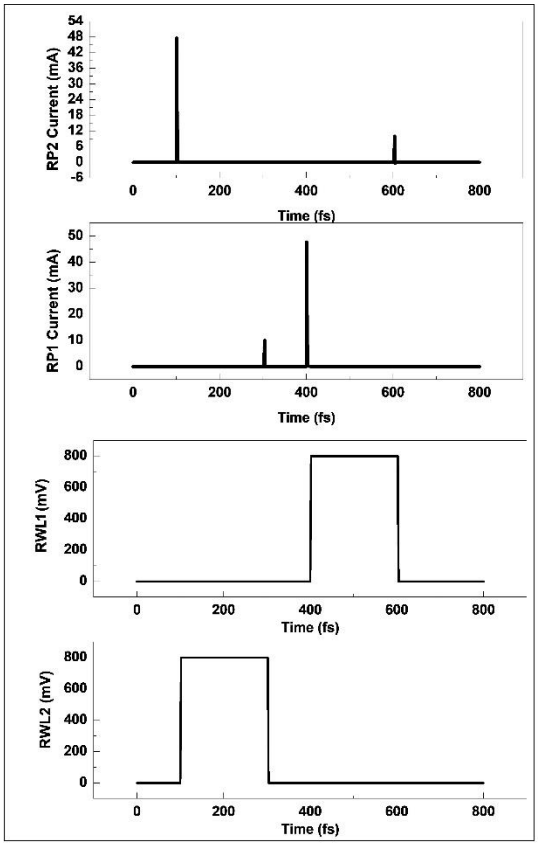


Fig. 4.28 Read current through the different read ports for the dual mode operational SRAM cell.

But single port cells do not support pipelining, whereas dual port cells enable it. Thus, when the memory is required to operate in high-speed mode, the cell should be steered into dual port configuration. Whereas, when timing is not a constraint, the cell may function in its single port mode. The working of the proposed dual mode operational cell in two different read modes is demonstrated in Fig. 4.28. The initial condition for the cell is maintained to be Q = '1', and QB = '0'. The write port for the cell is turned OFF and only the read operation is to be performed. It can be observed from Fig. 4.28, that when the RWL1 signal is high, the red current through Read Port1 (RP1) increases instantly to 47.65 mA.

This is the read discharge current that is responsible for the read operation. During this phase, the cell is being operated in single ended single port configuration, but as the read port2 (RP2) is also connected to node Q; a fickle leakage current can be observed at that port too. Whereas, when the cell is being operated in the dual port configuration, the read discharge current flows through RP2 only. This read discharge current is also in the same

range but is slightly higher than the RP1 read current at 48.6 mA.

Thus, based on the read discharge current recorded for the mode of operations for the cell, it is justified that it will be able to operate in dual mode configuration. Thus, as the proposed dual mode configuration cell may be deemed stable, resilient to PVT variations. Also, the cell can operate in both the single and dual port configurations independently.

4.7 SUMMARY OF IMPORTANT RESULTS

The key findings in this chapter are summarized as follows -

1. In this chapter, the concept for a dual mode operational cell is proposed. Thereafter, a single ended, dual port 7T bit cell is proposed. Using the proposed dual port cell and the best proposed cell from chapter 3, the dual mode operational bit cell is designed and its performance is analyzed.
2. The decreasing operational V_{DD} and scaled technology node for memory designing has widened the gap between two crucial strafes off for an SRAM – delay and power. The need for round the clock connectivity is increasing with the growing popularity of the internet of things. These mandates designing a cell with a capability to switch between low power and high-speed operation.
3. The concept for a dual mode operational cell proposes a cell that can operate as a single port or dual port single ended 7T memory cell. The switching of the mode of operation of the bit cell is controlled using the control signals for the cell.
4. A single ended, dual port, 1R1W 7T bit cell is proposed to design the dual mode operational cell. The cell is designed at 32 nm technology node and simulated for 0.8 V V_{DD}.
5. The pre-existing cells were reported for different technology nodes, and V_{DD}. After evaluation it is identified that minimal V_{DD} for most cells is 0.6 V, but the static margins are extremely low at this point. Therefore, for a fruitful comparison, all the bit cells are compared for 0.8 V of V_{DD}.
6. The static analysis of the proposed dual mode cell reveals that the hold and read noise margin for the proposed cell are equal at 324 mV each, while the write margin is 488 mV.

7. The dynamic analysis illustrates that a successful read and write operation is registered for pulse-width of 5 ps and 0.14 ns, respectively.
8. The temperature and process corner analysis are used to justify the reliability for the proposed cell. The former variation analysis yields 0.15, 0.15, and 0.24 mV/ºC variation in the HSNM, RSNM, and WM for the cell, respectively.
9. The bit cell is also HSD free and BI enabled. Thereby increasing the reliability for the cell.
10. The leakage power consumption for the cell is 256 pW, while the read, and write power consumption for the cell are 6 µW and 1.9 µW, respectively.
11. The merits for the proposed dual port cell are achieved with a minimal layout area of 0.553 μm^2.
12. The noise stability of the dual mode operational cell is obtained as 333, 333, and 470 mV for read, hold and write operation, respectively at 0.8 V V_{DD}.
13. The robustness of the cell against temperature variation, process variation and voltage variation is also analyzed. The variation recorded in each performance parameter is within the acceptable limit.
14. The write time recorded for the dual mode operational cell is 0.14 ns, while 5 ps is required to complete a successful read operation. The dual port configuration of the cell supports pipelining and thus, operates faster than its single port configuration.

CHAPTER – 5

SINGLE ENDED, SENSE AMPLIFIER DESIGN FOR PERFORMANCE ENHANCEMENT

The utility of a bit cell in SRAM is to store information, while its read, and write operation are facilitated by the peripheral circuits. A particularly important peripheral circuit used during the read operation is the SA. Conventionally, SAs were designed with differential ended topology. But the growing dependence on single ended cells has generated the need for single ended SA topology. This SA topology is usually voltage based in nature owing to their low area footprint and low operational V_{DD}. But delay and current for current mode topology are higher. Thus, generating need for a single ended SA that has low power consumption, smaller area footprint, and faster operation. Thus, the following objective is framed to accommodate the aforementioned need –

"Design and performance analysis of a sense amplifier to club the merits of voltage based and current based topologies for performance enhancement."

Methodology used to achieve the desired objective in the chapter is as follows -

- Design a modified single ended SA topology for faster sensing and low power consumption.
- Analyze the output performance of the proposed design to ensure fast operation
- Evaluate the performance of the proposed SA for PVT variation.
- Validate the performance of the proposed SA against other single ended SAs

In this chapter, a single ended voltage mode SA is designed for low bitline input, faster sensing, low power consumption, and greater reliability. This chapter is organized into four sections, including introduction, section 5.1. In section 5.2, the proposed single-ended dynamic SA architecture is elaborated upon. Further, the performance of different SA topologies is compared and analyzed in section 5.3. While, in section 5.4 the findings of the chapter are summarized.

5.1 INTRODUCTION

The increasing demand for battery powered SoC applications has forced designers to lower the power requirement for a circuit. Especially, with the growing market for implantable bio-medical devices, the need to reduce power consumption has taken the center stage. Conventionally, for a SoC the major chuck of total power consumption is consumed by cache memory and its peripheral circuitry [173]. But, with the increasing processing load, cache memories tend to occupy more area and consume a major portion of total power consumption thereby, limiting its performance. Whereas, designing a high-density cache memory operational at lower V_{DD}, is limited by the following reasons.

Firstly, designing a high-density memory requires minimally sized transistors, which are highly vulnerable to process variations [174]. Secondly, as the V_{DD} decreases the current through transistor becomes exponentially dependent on V_{TH}. Thereby increasing the circuits' vulnerability to process variation [175]. Additionally, as cache memory is a large array based on bit cell, it is unable to average out random variation effect due to multi-stage circuit design [119]. Consequently, at lower technology node SRAM is directly exposed to the ill effects of random variation caused by device mismatch.

Conventionally, an bit cell is differential in nature, and its corresponding SA is also differential. This differential SA uses two bitlines to perform the sensing operation. This SA circuit is solely responsible for detection of a small differential signal on the bitline to yield a full swing signal at the output. But the performance of differential cells is tremendously impacted by the decreasing technology node and lowering V_{DD}. One mechanism adopted to improve cell stability with decreasing technology node and V_{DD}, is to isolate the read and write ports. But this may result in an increased area footprint for the cell. Another alternative is to decouple the read and write port for the cell. This is achieved with the help of additional transistors introduced within the cell topology [51]. A common feature amongst the decoupled cell and dual port cell topologies is the utility of single bitline for read operation.

The single ended read port for the cell enables improving its read stability, results in better yield, while keeping the cell area in check. Therefore, bit cells with single ended read operation are gaining popularity; they demonstrate improved performance at lower values of V_{DD}. A cache memory designed using single ended read port, mandates designing a single

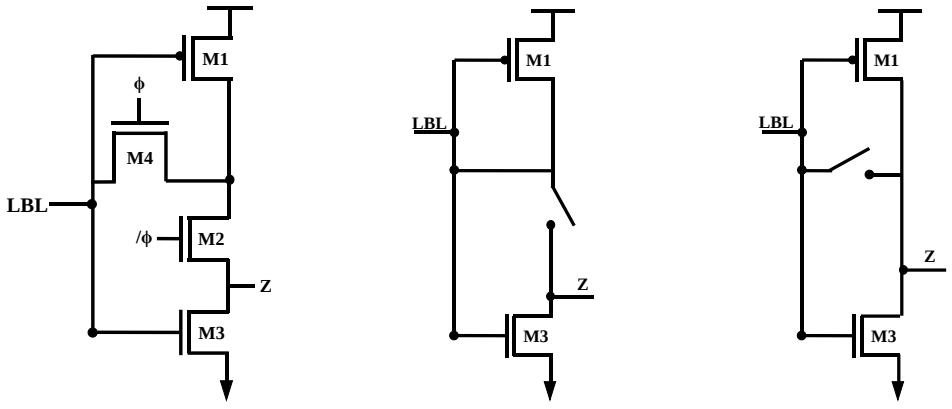
ended sensing scheme. The functioning of the single ended SA is dependent on a single bitline. One of the most common sensing schemes for single ended cell is large-signal single ended inverter [176]. For a single ended SA, the sensing margin is defined as the voltage difference between the LBL voltage levels and inverter trip voltage [176].

5.2 PROPOSED SENSE AMPLIFIER

In this chapter a single ended, switching NMOS sensing scheme (SNSS) is proposed. This SNSS topology is designed as a modification of the reported pre-existing sensing schemes. The proposed sensing scheme is designed to ensure lower area footprint and faster operation for the circuit. The structure and functioning of the proposed sensing scheme are explained in the following sub-section.

5.2.1 Structure and Functioning of the Proposed SA

The detailed structure for the proposed SNSS is depicted in Fig. 5.1 (a). The circuit topology for SNSS consists of a pull up PMOS transistor (M1) and a pull down NMOS transistor (M3). Two NMOS transistors are added to the inverter topology M2 and M4, the two are added in between M1 and M3 in a stacked configuration. The utility of M2 is that it is controlled by an additional control signal /ϕ, which is activated only when a particular sub bank is selected.



(a) (b) (c)

Fig. 5.1 Schematic diagram for (a) proposed sense amplifier design, equivalent-circuit configuration during (b) pre-charge phase, and (c) evaluation phase.

During the pre-charge phase (ϕ = '1'), the LBL is charged due to the pre-charge circuit, depicted in Fig. 5.1 (b). This circuit eliminates the short circuit current condition between

V_{DD} and ground, which gets created in the ACSS circuit. Whereas, in the evaluation phase (ϕ = '0'), the M1-M3 inverter is in conducting state; its input being the bitline voltage and the output is sensed at node Z. The equivalent circuit topology during the pre-charge and evaluation phase is depicted in Fig. 5.1 (b) and (c) respectively. The output waveform corresponding to the functioning of the proposed SNSS topology is depicted in Fig. 5.2. The circuit is simulated for V_{DD} of 1 V and 27 ºC environment temperature.

The performance of the proposed SNSS is tolerant to variations as the pre-charge voltage levels of LBL work in conjunction with the NMOS transistor (M2). The obtained output waveform for SNSS is depicted in Fig. 5.2. It can be inferred from the output waveform that SNSS performs the read sensing operation when '0' is stored in the cell. During the sense '0' operation, the read wordline is exerted and the bitline at the pre-charged voltage level is lowered due to read discharge current. During this phase, the ϕ signal is high and the sensing inverter topology is biased at the trip voltage. Once the read wordline is exerted, and the bitline has discharge the ϕ signal is set low. Then the effective circuit for SNSS, during the evaluation phase is depicted in Fig. 5.1 (c). Now, when the previously pre-charged LBL experiences a decline in voltage level, it is sufficient to turn ON transistor M1. Consequently, the sensing performance for the proposed SA is performed. Whereas, if '1' is stored in the cell, no read discharge current occurs. Thereby, no output is recorded by SNSS. The same may also be inferred from Fig. 5.2.

A small bitline discharge can turn ON transistor M1, resulting in a rise in the output level voltage. Thereby, improving its performance in comparison to the domino sensing scheme. Whereas, in comparison to SPSS, the proposed SNSS topology uses NMOS for switching, which improves its operational speed; NMOS device is faster in comparison to an equally sized PMOS transistor. Additionally, the SPSS topology is designed with stacked PMOS configuration for the pull up network, but this makes it highly skewed. Consequently, the PMOS width must be large to ensure fast operation. This also causes high levels of energy consumption for SPSS due to parasitic capacitance [177]. The local bitline (LBL) is the common bitline shared by a column; it acts as the input to the proposed sensing scheme. When the data stored in the memory cell to be read is '0', the discharge current flows through the read port of the cell and the LBL is discharged to '0'.

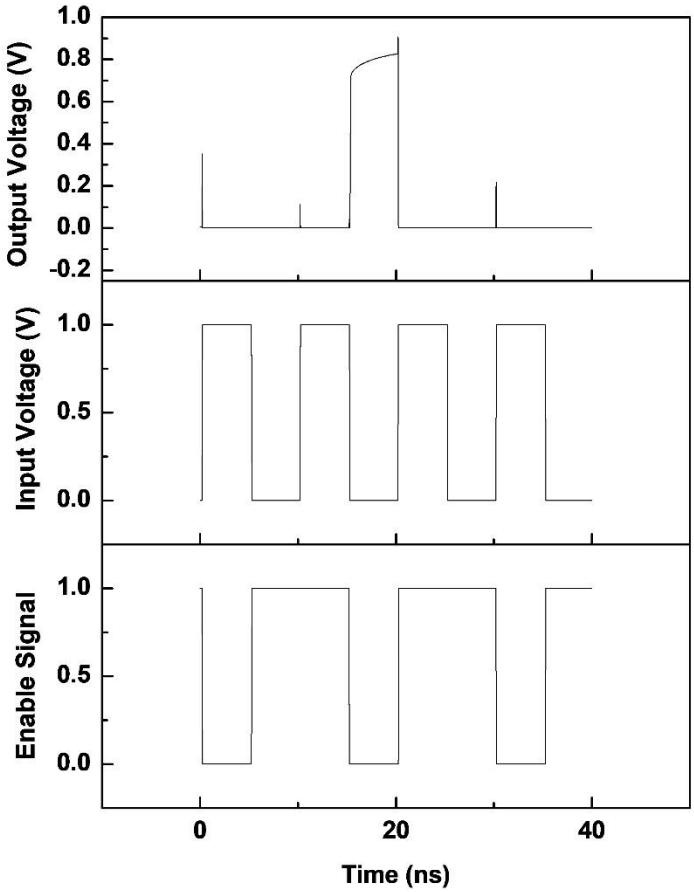


Fig. 5.2 Output waveform corresponding to the proposed SNSS topology.

This LBL is the input of the proposed sensing scheme, thus for LBL = '0' it charges Z to '1', provided ϕ = '0'. The Z node in turn, yields a full swing output as the global bitline (GBL). The GBL is important, as it is the final output for the sensing scheme. LBLs are common amongst memory columns, but the GBL is unique for the entire cache. Therefore, the number of LBLs in cache memory is dependent on the array size and configuration, but there is only one GBL per cache memory.

bit cells are arranged in rows and columns to form the storage core for the cache memory. At the bottom of each column, the bitline is connected to the input of the SA. Thus, when a read operation is to be performed for a given cell, its respective column SA is enabled. For the proposed SNSS the same applicable, one sensing scheme block is common for a given column. The proposed SA performs sensing operation only when the data stored in the bit cell is '0'. Whereas, if the data stored in the bit cell is '1', no discharge current is registered. So, when a cell in a column has to perform read operation, the enable signal (ϕ) is set low. Additionally, the ϕ signal has to be operated with slight delay with respect to read wordline

signal; this is done to ensure that, the LBL has attained its desired value after the discharge current has passed through the circuit. Once the LBL value is set, then the ϕ signal for SA of that column is set to '0'. When the read operation is completed, the ϕ signal is restored to '1' and the SA is turned OFF. Thereby lowering power consumption for the proposed SA.

5.2.2 Delay Analysis for Proposed SA

The proposed SA is designed for single ended cell, which results in read discharge current for state '0'. Therefore, LBL is low only when the selected cell has state '0' stored; for state '1', no discharge event is registered. During the LBL discharge operation, the time required to raise the output node to 90% of V_{DD} after assertion of the read word line for the cell is defined as the sensing delay [168]. The performance of the proposed SNSS topology at the different process corners is compared in Fig. 5.3. The proposed SNSS topology has the most inferior performance at the SS corner. This is because the performance of both the PMOS and NMOS transistor deteriorates at the SS corner.

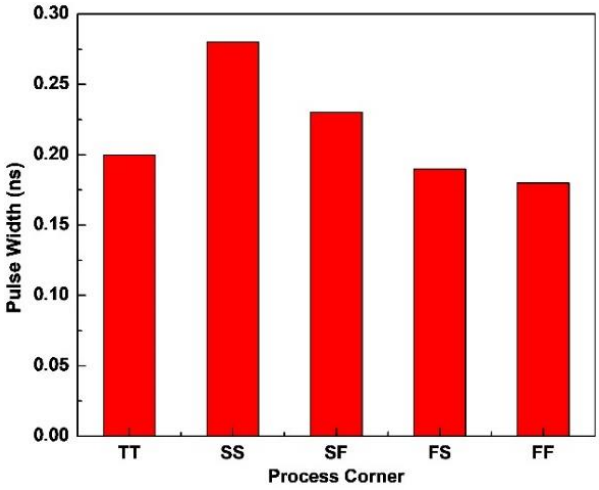


Fig. 5.3 Delay timing for the proposed sense amplifier topology at different process corner for V_{DD} = 1 V.

While, the best performance is observed at the FF corner, due to the uplifted performance of the PMOS and NMOS transistors. The performance of the proposed SNSS topology at the TT corner is 0.32 ns, which is improved in comparison to the pre-existing topologies (explained in subsequent 5.3.1).

5.2.3 Process, Voltage, and Temperature Tolerance Analysis of Proposed SA

In this sub-section the performance of the proposed SNSS is evaluated against PVT variation. The analysis is performed to validate the reliability of the proposed technique when subjected to variations due to internal and external factors. For process variation analysis, statistical methods are employed to identify the impact of variation in transistor V_{TH}, caused due to process variations. MC simulations are carried out for 10,000 data point, varying transistor V_{TH} in 6σ range around the mean V_{TH} value. The output waveform obtained for SNSS using MC simulation is depicted in Fig. 5.4.

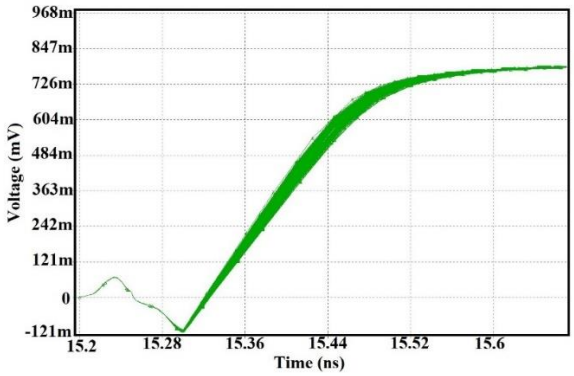


Fig. 5.4 Variation in the output waveform for the proposed SA for sensing 0 for process variation.

It can be inferred from the MC simulation output for SNSS that process variation results in a minor variation in the performance of the bit cell and the reliability of the waveform is maintained. It is also observed that as the variation in the value of V_{TH} increases, the slope gradient of the transient analysis curve decreases. This results in a very insignificant increase in time required to attain the maximum output level for the SA. The same may also be inferred from Fig. 5.5.

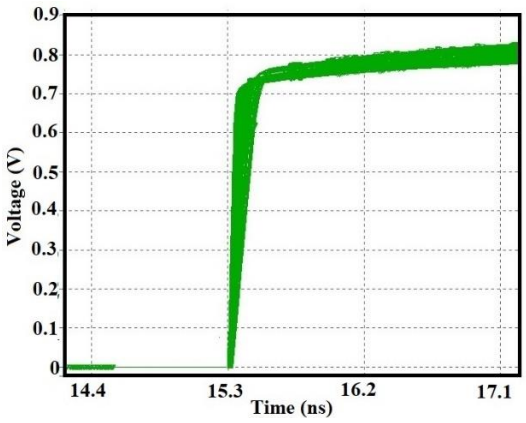


Fig. 5.5 Variation in the output waveform for the proposed SA for sensing 0 for voltage variation between 0.9 to 1.1 V.

The proposed SNSS topology is designed at 32 nm node; in nanometer vicinity the reliability of a circuit is of primal concern. A circuit design is expected to demonstrate resilience to temperature variation. Correspondingly, the performance of the proposed SNSS is evaluated for temperature variation from -10 ºC to 110 ºC. A section of the transient waveform for the SNSS is depicted in Fig. 5.6. It can be observed from Fig. 5.6, the output waveform for SNSS does register a shift in its performance. But the variation in performance of the SNSS is within manageable bounds and will not have a drastic impact on the overall performance of the circuit.

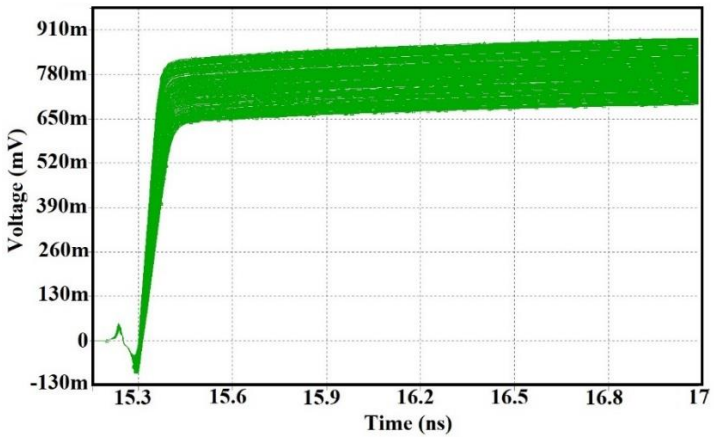


Fig. 5.6 Variation in the output waveform for the proposed SA for sensing 0 for temperature variation from -10ºC to 110 ºC.

It is identified that the worst-case output voltage for the proposed SNSS topology is ~0.75V; the same can be inferred from Fig. 5.4. While the impact of PVT variation on performance of the proposed SNSS topology is depicted in Fig. 5.4, 5.5 and 5.6, respectively. The maximum variation in output waveform of SNSS topology due to process variation is ~0.1V as can be inferred from Fig. 5.4. While voltage variation results in altering the output waveform by ~0.05V (as depicted in Fig. 5.5). The maximum variation of ~0.25V in performance of SNSS topology is caused by temperature variation (as can be inferred from Fig. 5.6), but here the maximum output voltage obtained is ~0.9V. Therefore, the minimum voltage that the output waveform may register is ~0.66V, which is within reliable voltage limits. Also, the temperature range taken into consideration is -10ºC to 110ºC.

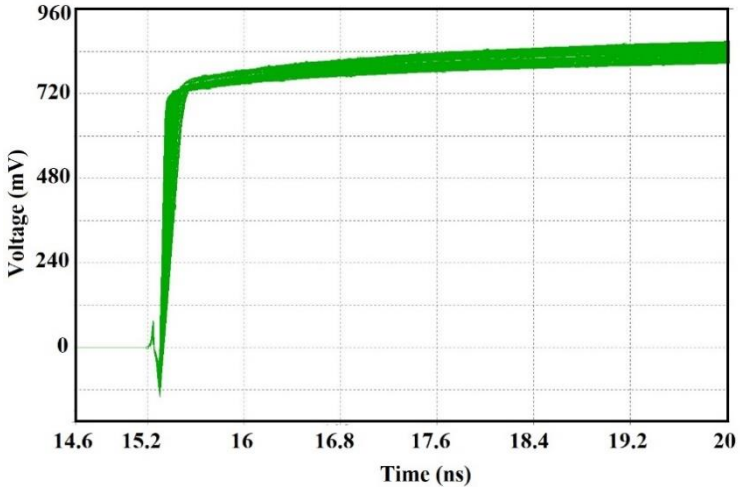


Fig. 5.7 Variation in the output waveform for the proposed SA for sensing 0 for temperature variation from 0ºC to 70 ºC.

This is an extremely wide range for evaluation of analysis, whereas most commercial electronic devices operate within 0 ºC to 70 ºC. Thus, when the cell is evaluated for this range, the variation in the performance of SNSS is considerably reduced. The same may be inferred from Fig. 5.7. It can be inferred from Fig. 5.7 that the maximum variation caused due to temperature variation is ~0.07V. Thus, the proposed SA topology; SNSS may be deemed resilient to PVT variations.

5.3 PERFORMANCE COMPARISON FOR PROPOSED SA WITH PRE-EXISTING SA TOPOLOGIES

In this section, the performance of the proposed SNSS topology (depicted in Fig. 5.1 (a)) is compared against pre-existing single ended SA designs. The SAs are designed at 32 nm technology node and are simulated for 1 V of V_{DD}. The models used for designing the circuit topology are based on the Predictive Technology Model.

5.3.1 Sensing Delay Analysis for Proposed and Pre-existing SA Topologies

The most essential aspect for an SA topology is its timing requirement. During the read operation for single ended bit cell, the time required for flipping the output of the single ended SA after the ϕ signal has been set is referred to as the read time (T_S) [119]. The proposed cell improves the delay performance by using more NMOS transistors and aptly sizing them to have sufficiently large drive current, while maintaining its area occupancy.

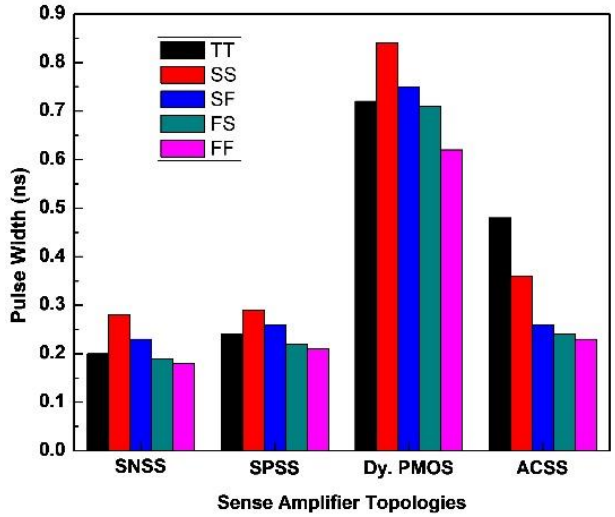


Fig. 5.8 Comparison of delay timings at different process corners for all the SA topologies.

The sensing performance for the different SA topologies along with the proposed SA are graphically compared in Fig. 5.8. The sensing performance for each SA is determined at each process corner to analyze the impact of global variation on the performance of the topology. For all the SAs, the best performance is observed at FF corner, owing to the better performance for both NMOS and PMOS. The dynamic PMOS based SA topology has the most inferior performance in comparison to others for all corners.

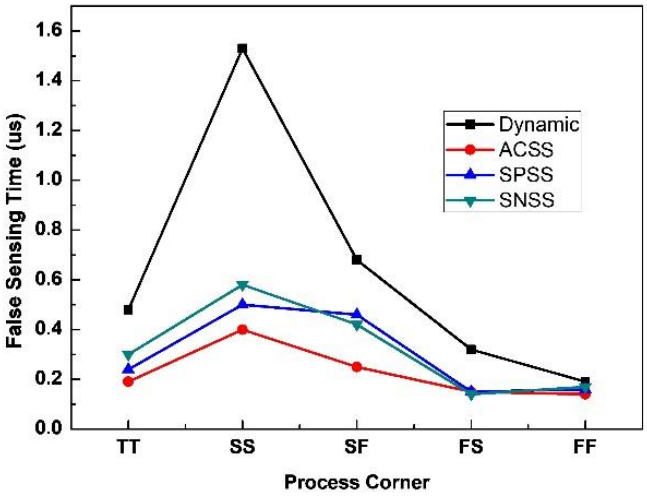


Fig. 5.9 Comparison of false read time at all process corners for all the SA topologies.

The proposed SNSS has improved performance in comparison to the other topologies. In comparison to the dynamic PMOS, ACSS, and SPSS, SNSS has improved performance by 5.25, 0.5, and 0.25 times, respectively. The best performing pre-existing SA topology in terms of delay is SPSS with delay of 0.4 ns. Whereas, the proposed SNSS topology registers

a delay of 0.32 ns. Thus, the proposed SA topology has improved delay performance in comparison to pre-existing designs.

The read operation for a single ended bit cell can be divided into stages. Firstly, the read wordline signal is asserted. Then, if the data content of the cell is '0', a read discharge current is registered, and the voltage at LBL is lowered from '1'. Otherwise, no discharge current is registered and LBL maintains its pre-charge value. Then, after a certain amount of time the ϕ signal is set low to enable the sensing scheme. If the LBL at this instance is '0', the designated cell is determined to have '0' stored in it.

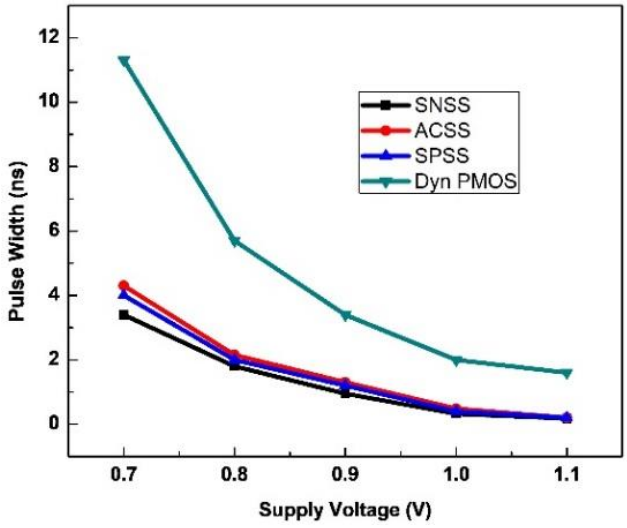


Fig. 5.10 Comparison of delay for varying V_{DD} for all the SA topologies.

Otherwise, '1' is stored in the cell. Ideally, when '1' is stored in the cell, no current should flow in the circuit. But, small amount of OFF current (leakage current) due to state '1' stored in cell may cause an unintentional discharge of LBL. The time required for this unintentional discharge to falsely flip the output of the SA is referred to as false read time. Ideally, for reliable sensing operation, the value obtained for false read time should be significantly larger than the sensing delay for that topology

The false read time values obtained for the different sensing schemes are graphically compared in Fig. 5.9. It may be observed from Fig. 5.9 that at TT corner, the dynamic PMOS SA topology has the highest false read time at 0.48 µs. While the performance of the proposed SNSS topologies is 0.3 µs. The performance of ACSS and SPSS is inferior amongst the four SA topologies, as their false read time is lower in comparison to the other SA topologies.

The SNSS topology has superior sensing performance even when evaluated for different V_{DD} values; the same can also be inferred from Fig. 5.10. The performance of all the SA topologies at different V_{DD} values is compared in Fig. 5.10. The highest delay is utilized by the dynamic PMOS topology. While the remaining single ended SA techniques have comparable performance. But, amongst the ACSS, SPSS, and SNSS topology the least delay requirement for output generation is registered by SNSS. The performance of the proposed SNSS topology is comparable against performance of SPSS and ACSS pre-existing topologies. Amongst pre-existing sensing schemes, the SPSS topology has the least delay performance.

The SNSS topology improves upon the delay performance of the SPSS topology. This is achieved by replacing the stacking PMOS transistor (M2) in SPSS topology by an NMOS transistor (M2) in the SNSS topology. The major reason for changing the nature of M2 transistor is to achieve faster operation using a smaller sized transistor; an NMOS has faster operation than an equally sized PMOS. Additionally, the SPSS topology has two PMOS transistors M1 and M2 stacked one over another. This configuration increases the delay of the circuit, while poorly impacting the area footprint for the SA (a greater number of PMOS implies larger n-wells in the layout). Thus, for the proposed SA, only one PMOS transistor is used, and its sizing is also optimized to reduce area while achieving better delay performance.

5.3.2 Power Consumption Analysis for Proposed and Pre-existing SA Topologies

Power consumed by a single ended sensing scheme is dependent on the current requirement for the sensed state and the previous state. For instance, power is consumed during the pre-charging of the current state only if ‘0’ is sensed during the previous time cycle. Similarly, for the current time period, power is consumed only when the state being sensed is ‘0’, for sensing ‘1’ no power is consumed by the circuit. Therefore, in keeping with the condition of the present state (‘0’ or ‘1’) and the previous state (‘1’ or ‘0’), four distant cases can be identified for power consumption calculation. Thus, for each SA topology power calculations are done corresponding to 00, 01, 10, and 11 cases.

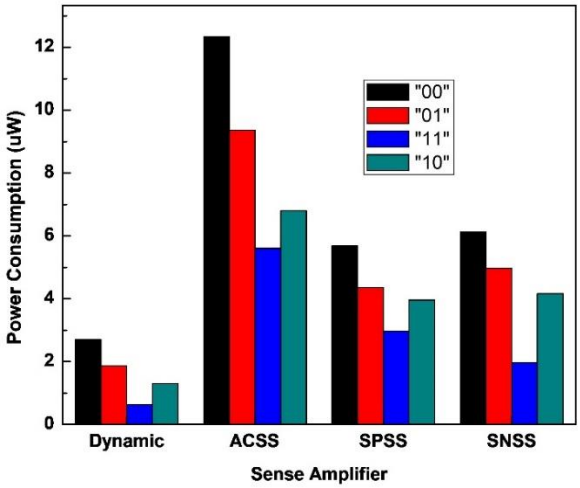


Fig. 5.11 Comparison of power consumption corresponding to four data cases – 00, 01, 10, and 11 for all the SA topologies.

The two-bit data pattern denotes the data state sensed by a given SA topology during the previous time cycle and the current time cycle. Consequently, “10” data state implies that the SA topology sensed data ‘1’ during the previous time cycle and during the current time cycle it is sensing state ‘0’. The power consumption values obtained for the different SA topologies for the four different data cases are graphically compared in Fig. 5.11. Most power consumption for any of the single ended topology discussed in the chapter is reported for “00” bit sequence. This is because of two consecutive sensing operations. Whereas, the least power consumption for all topologies is observed for data sequence “11”, as no sensing operation is performed (the single ended sensing topology only senses ‘0’ state).

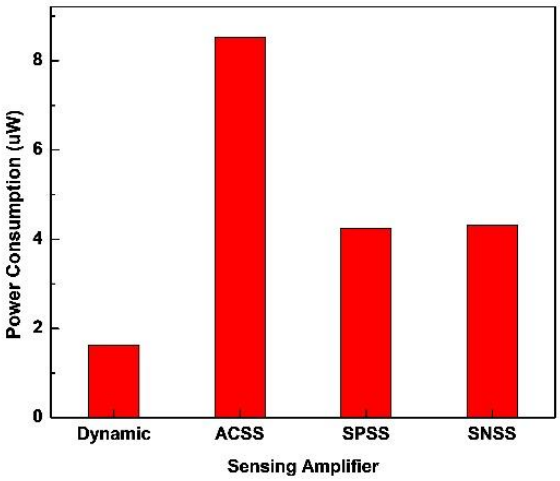


Fig. 5.12 Comparison of average power consumption for all the SA topologies.

Additional to the power consumption for four different data cases, average power

consumption for each SA topology is also calculated. The average power consumption for each SA is presented in Fig. 5.12. The average power consumption for the ACSS topology is the highest amongst others. Its average power consumption is 34.27, 43.06, and 40.72 % greater than dynamic PMOS, SPSS, and SNSS, respectively. The higher power consumption of the ACSS is an implication of biasing the first-stage inverter to an intermediate voltage during pre-charge mode, resulting in a short circuit current flowing through the circuit. Whereas, the SPSS and SNSS topologies can evade this problem with a switching PMOS and NMOS transistor, respectively. Therefore, the average power consumption for the two topologies is drastically lower than the ACSS topology.

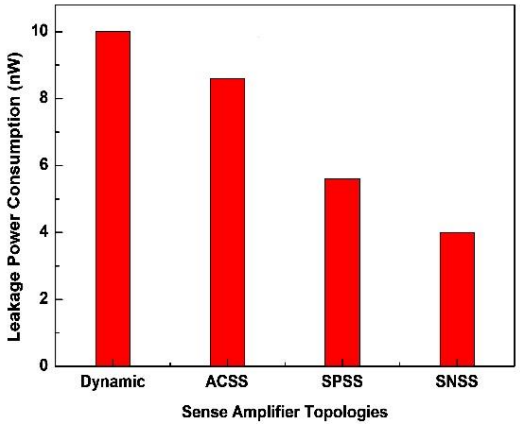


Fig. 5.13 Comparison of leakage power consumption for all the SA topologies.

When the read operation is not being performed, the SA is disabled using signal ϕ. During this state, the power consumed by the SA topology is referred to as its leakage power consumption. It is calculated as the product of leakage current in the circuit and V_{DD}. The leakage power consumption values obtained for the different SA topologies are graphically compared in Fig. 5.13. The leakage power is highest for the dynamic PMOS topology, and it is 2.5 times the value for the SNSS topology. Amongst the pre-existing SA topologies, the best performance is demonstrated by SPSS topology; its leakage power consumption is 5.6 nW. The performance of the SPSS topology is 1.4 times more than the SNSS topology. The predominant use of largely sized PMOS in its design is the culprit for the same; larger PMOS are necessary for higher drive current and smaller delay of the circuit.

5.3.3 Area Analysis for Proposed and Pre-existing SA Topologies

The different single ended SA topologies and the proposed SNSS design use a static inverter to drive a domino sensing scheme to eventually develop the correct value on GBL. The

difference lies in which sensing technique is used. Consequently, the area footprint for the sensing scheme is also dependent on the SA topology employed. The area for the domino sensing with a dynamic PMOS SA is 5.314 μm^2. The area for the ACSS, SPSS, and SNSS topologies are 16.3, 9.43, and 7.65 μm^2, respectively. The area for the ACSS, SPSS, and SNSS is multi-fold larger than the dynamic PMOS SA, this is because the transistor count for each is fairly larger. The performance improvement of the proposed SNSS outweighs its larger area overhead in comparison to the dynamic PMOS sensing scheme.

Also, the area footprint of ACSS and SPSS is 8.65, and 1.78 times larger than the area requirement of the proposed SNSS technique. The SPSS technique has larger area as for the same performance larger PMOS are required in comparison to an NMOS transistor. Therefore, increasing the area footprint for SPSS. Also, more the number of PMOS transistors the greater number of n-well are to be created in the layout design, which also increases the area footprint for the cell. Whereas, for the ACSS technique the large area is caused by a large coupling capacitor and additional static inverter (which increases its transistor count) used within its circuit topology for sensing operation. Thus, the area footprint for the ACSS is largest amongst all the single ended SA techniques discussed in this chapter.

5.4 SUMMARY OF IMPORTANT RESULTS

The key findings in this chapter are summarized as follows -

1. In this chapter, a single ended switching NMOS based SA topology is proposed. The proposed SA is operated in two modes - pre-charge and sensing operation. When sensing is not to be performed it is maintained in pre-charge phase, and during the read operation, it operates in evaluation phase.
2. Conventionally, a bit cell is differential in nature, and its corresponding SA is also differential. This differential SA uses two bitlines to perform the sensing operation.
3. The single ended read port for the cell enables improving its read stability, results in better yield, while keeping the cell area in check. Therefore, bit cells with single ended read operation are gaining popularity.
4. A cache memory designed using a single ended read port mandates designing a single ended sensing scheme. The functioning of the single ended SA is dependent on a single

bitline. One of the most common sensing schemes for single ended cell is large-signal signal ended inverter.

5. For a single ended SA, the sensing margin is defined as the voltage difference between the input voltage levels and inverter trip voltage. The most important performance metric for an SA includes - sensing delay, minimum differential input voltage, and power consumption during the read operation.
6. The proposed SA performs sensing operation only when '0' is stored in the cell. The performance of the proposed SA is robust as the maximum variation in its output waveform due to process variation is ~0.1V. While voltage variation results in altering the output waveform by ~0.05V.
7. The performance of the proposed SA is improved compared to the dynamic PMOS in delay and power. The delay requirement of 0.32 ns for the proposed scheme is significantly lower in comparison to its other counter parts.
8. In terms of power also the proposed sensing topology performance reliably. The low power consumption of the proposed SA is because of its ability to evade short circuit conditions. The leakage power for SNSS is also found to be least amongst the different SA topologies at 4 nW.
9. The average power consumption for the ACSS topology is the highest, which is 34.27, 43.06, and 40.72 % greater than dynamic PMOS, SPSS, and the proposed SA topology, respectively.
10. The additional advantage the proposed SA has its lower area footprint of 7.65 μm^2. The area footprint of pre-existing topologies - ACSS and SPSS, is 8.65, and 1.78 times larger than the area requirement of the proposed SNSS technique.
11. The proposed SNSS relies on a single PMOS for its design, thereby reducing its area footprint, and increasing its integration density and economic feasibility.

CHAPTER – 6

HYBRID ARRAY DESIGN FOR LOW BIT ERROR

Bit cells and SAs play a crucial role in the design of a cache memory. A bit cell is replicated to form an m×n array for data core for the memory. In an array configuration, the performance of a bit cell is influenced by other cells that are in the same row and column. Therefore, it is essential to analyze the performance of a bit cell when it is placed in an array configuration. Additionally, even though the power for a bit cell is low, due to sheer size of the array, the power consumption for the array is significantly large. Therefore, it is essential to identify mechanisms to lower power consumption for the array. While ensuring that the designed array topology is resilient to half-select error and has minimal bit error. Thus, the following objective is framed to accommodate the aforementioned need –

"Analyzing the proposed array arrangement to reduce vulnerability towards half select issues and bit error."

Methodology used to achieve the desired objective in the chapter is as follows -

- Analyze the performance of the proposed single port and dual port bit cells in the conventional array arrangement.
- Propose a hybrid array configuration using the proposed cells.
- Analyze the proposed cells in the hybrid array configuration for half-select disturbance.
- Evaluate the proposed array configuration for bit error and power consumption.

In this chapter, an overview of conventional array configuration is presented, and a hybrid array configuration is proposed. The chapter is divided into six sections, including section 6.1, introduction. Further, in sections 6.2 and 6.3, the conventional array configuration and the proposed hybrid array configuration are explained in detail. It is followed by section 6.4, in which the different 7T cells used to design the proposed array are explained and their performance is elaborated upon. Further, section 6.5 is dedicated to bit error and its impact on the proposed array configuration. Whereas, in section 6.6, the power model for the proposed array configuration is presented and the power consumption results are analyzed in section 6.7. Finally, the findings of the chapter are concisely summarized in section 6.8.

6.1 INTRODUCTION

The widening application range for mobile and implantable devices has increased the demand for low power systems [178-183]. The decreasing technology node, increasing demand for longer battery life, higher integration density, and lower operational voltage have made it necessary to develop innovative design paradigms. As explained previously, the essential design parameters for a cache memory include – low delay, faster operation, low power consumption and minimal area. Different bit cells and their implementation techniques have been reported in literature to achieve one or more of the abovementioned design objectives [24-48]. To improve and optimize cache memory performance, most designers usually restrict themselves to bit cell design.

Researchers have increased the transistor count [184], isolated read-write port [49], added boosting circuit [170], used multiple V_{TH} transistors [90] and even multiple configuration [185] to improve and uplift the performance for a bit cell. Consequently, there are plethora of cells that a memory designer may choose from, depending on the target application. All the different bit cells reported in literature improve performance in terms of one parameter or the other. But a bit cell is only a foundational stone in the design of a SRAM. It is a small peg that gets replicated multiple times to form the array that acts as the memory core. Thus, designing and optimizing the array configuration for memory is equally essential.

Additionally, memories that consume less power have better system performance, stability, and efficiency. Conventionally, designers reduce V_{DD} for a bit cell to lower its power consumption. But this has a drastic impact on noise margin, and delay performance for the cell [130]. Therefore, lowering V_{DD} for a cell has its limitations. Another desirable factor for memory is high density, to achieve the same; designers have aggressively scaled technology node for the circuit. But beyond a point, even this has its saturation due to PVT variations [33]. These variation parameters play a dominant role in sub-threshold, and near threshold region of operation. Thus, for a bit cell designed at lower end of the nanometer technology node, it is more convenient to operate it the super-threshold region.

Lowering the power consumption for a memory circuit is not only dependent on lowering its V_{DD}. Another alternative for power saving for memory may be optimizing the array power consumption, but very few research works have explored this arena. Also, aggressive scaling of voltage in all bits of a pixel, increases the error rates in all bits and leads to faster

degradation of image quality [186]. In a typical multimedia application the information pertaining to each pixel is coded in bits. The lower order bits are referred to as least significant bits (LSBs) and the higher order bits are labelled as the most significant bits (MSBs). Typically, in an image LSBs may be more vulnerable to noise in comparison to MSBs. Hence, appreciable performance and minimal image quality degradation can be achieved by using two different bit cells for array formation [187]. The highly important and degradation prone MSBs can be stored in a performance improved and robust dual port bit cells, while the LSBs can be stored in a low power, comparatively more compact single ended single port 7T bit cell.

6.2 CONVENTIAONAL ARRAY CONFIGURATION

Conventionally, an SRAM based cache memory is formed by a j×k array of bit cells. A generalized block diagram representation for an SRAM cache is depicted in Fig. 6.1. It can be observed that the array has five different signals, wordline (WL), readline (RL), bitline (BL), bitline bar (BLB), and wordline bar (W). The WL, W, and RL signal are used to control the mode of operation (hold, read, and write) for a cell.

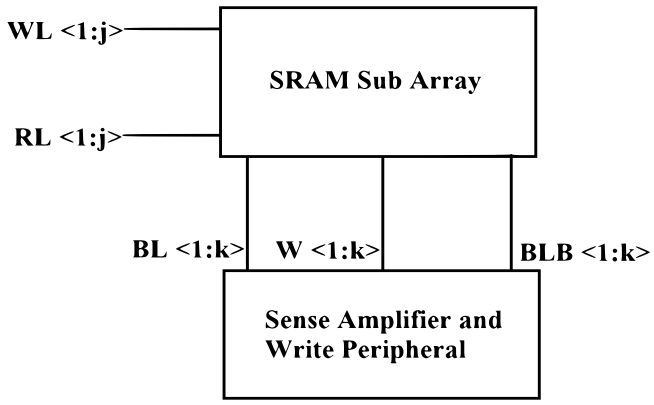


Fig. 6.1 Block diagram representation for an SRAM memory.

During the read operation, the RL and W signal are high, whereas during the write operation the WL signal is high, and W is maintained low. While, during the hold operation RL and WL signal are maintained low, while W is high. The use of BL and BLB is to facilitate the read and write operation. During the write operation, the data to be written into the cell is placed on BL and BLB. Whereas, during the read operation, the BL and BLB are pre-charged, and the read discharge current flowing through either of them, to help determine the data stored in the cell via a SA.

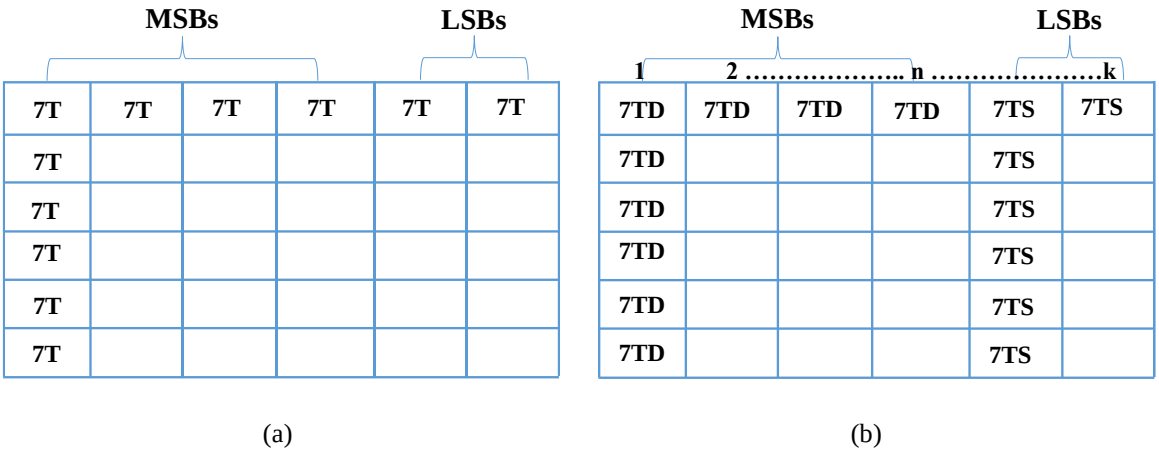


Fig. 6.2 Block level representation for cell arrangement in (a) conventional array design, and (b) in proposed hybrid array design.

In a conventional memory array of size j×k, the number of cells in a row forms a word. The bits stored in the higher order cell are regarded as MSB, whereas the lower order bits are referred to as LSBs. The same is illustrated in Fig. 6.2 (a). In this chapter only the proposed 7T bit cells (best identified cell from chapter 3 and dual port from chapter 4) are used for implementation of array.

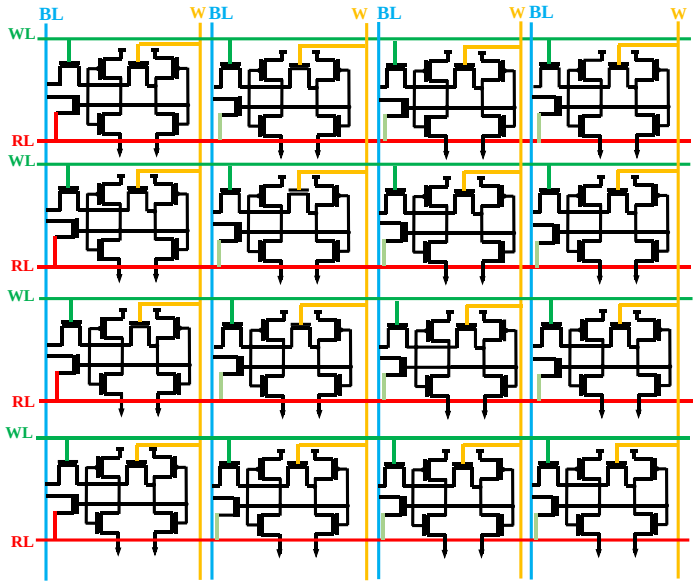


Fig. 6.3 A 4×4 array representation of SRAM memory based on single port 7T SRAM bit cell.

The array demonstrated in Fig. 6.1 is conventional in nature and is composed of 7T cells of a single configuration. The 4×4 array representation for a conventional array using single port and dual port 7T cells is given in Fig. 6.3 and 6.4, respectively. This design limits the performance of the array and also restricts the scope of optimization for the array.

Additionally, as described previously, not all bits have same level of significance in a word.

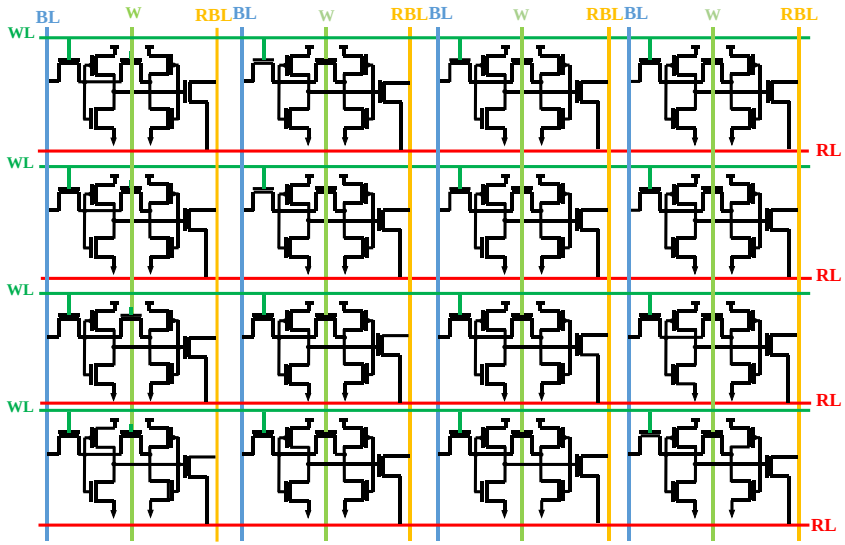


Fig. 6.4 A 4×4 array representation of SRAM memory based on dual port 7T SRAM bit cell.

The information stored in the MSBs is more crucial and should be more resilient to error than the one stored in LSBs. Thus, it may be concluded that MSBs could be designed using a different cell configuration than the LSB cells. This technique may also help cater to the increasing demand for area efficient and high density memory. This technique forms the basis for the design of the proposed hybrid array configuration.

6.3 PROPOSED HYBRID ARRAY CONFIGURATION

As discussed in the previous section, the conventional array configuration has its limitations in reducing the power consumption and area footprint for the memory. Therefore, a hybrid array configuration is proposed in this chapter using two different 7T bit cell topologies – dual port 7T cell (7TD) and single port 7T cell (7TS). The use of two different bit cells is inspired from the notion that there is always a trade-off between power, area, and economic feasibility [80]. Also, the information stored in the memory is stored in terms of words (formed by multiple bits). In a word, not all bit values have the same significance. The bits that form the MSBs for the word are more significant than the bits stored in LSBs.

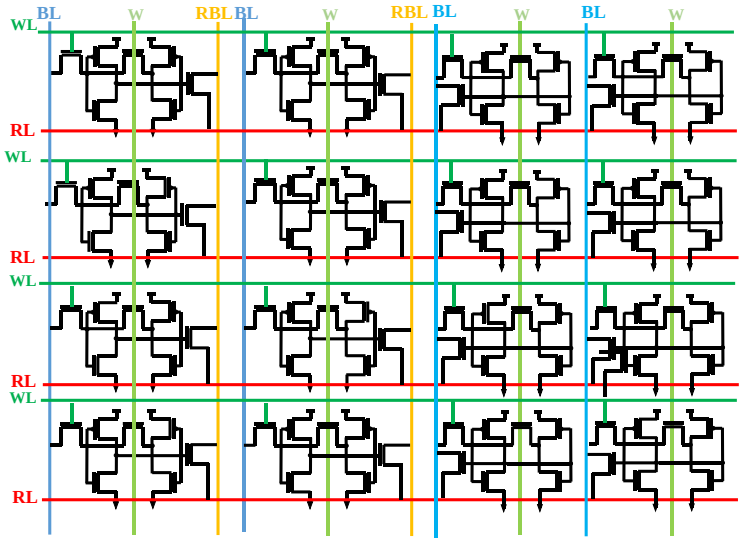


Fig.6.5 A 4×4 array representation of the proposed hybrid array configuration designed using single port and dual port 7T cells.

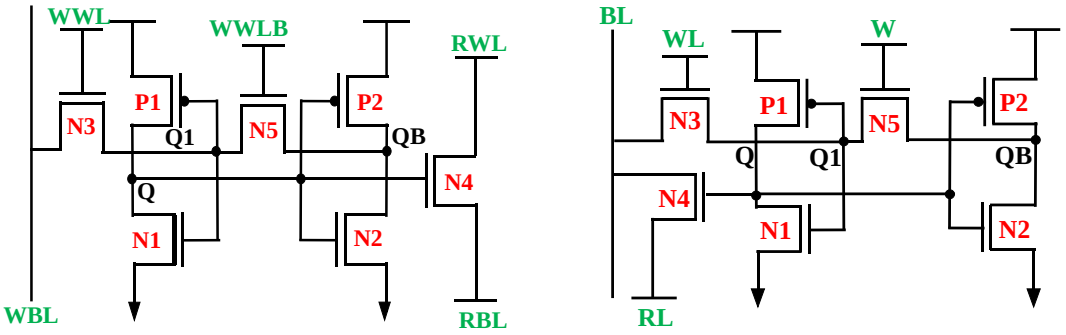
Collectively, using the aforementioned concept, the MSBs for the proposed hybrid array configuration are stored in 7TD cells, whereas the LSBs are stored in 7TS cells. A 4×4 representation of the proposed hybrid array configuration is given in Fig. 6.5. In this representation the 4×4 array is split in two equal 4×2 size 7TD array and 7TS array. But the partition for the hybrid array may vary depending upon the requirement on the specific memory and the system on chip or microprocessor it caters to.

6.4 7T SRAM BIT CELLS USED IN PROPOSED HYBRID ARRAY CONFIGURATION

Over the years, various bit cell – 7T, 8T, 9T, 10T, 11T, 12T, and 13T implementations have been reported in literature. But along with optimal cell performance, it is also essential to have a low area footprint, resulting in high cell density. Consequently, the proposed hybrid array configuration is implemented using two different 7T bit cell configurations – 7TS and 7TD. The 7TS cell is the best identified single ended single port 7T cell proposed in chapter 3 and the 7TD cell is the single ended, dual port 7T cell proposed in chapter 4.

The only difference between the 7TS and 7TD cell is that in the former cell, the read-write port share a common bitline, while they are isolated in the latter. The memory core for the two cells is identical and formed by a cross-coupled inverter pair (P1-N1 and P2-N2). The back-to-back connection between the inverter pair is dependent on N5 transistor; the N5

transistor is controlled via W signal. If W is high the internal core is a mutually coupled inverter, otherwise it is reduced to a cascaded inverter pair. W is high for read and hold operation and low for write operation. The schematic design for the 7TD cell and 7TS cell is depicted in Fig. 6.6 (a) and (b) respectively.



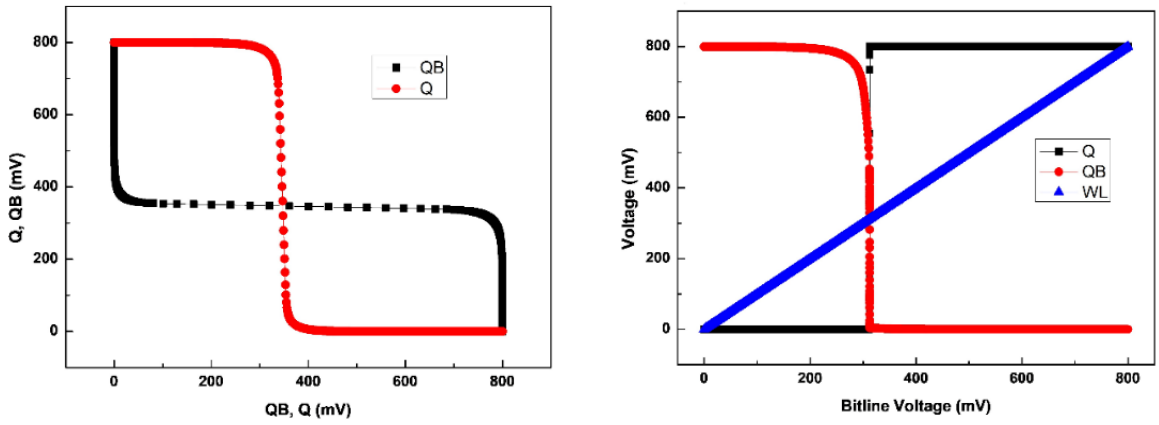
(a) (b)

Fig. 6.6 Schematic diagram of pre-existing (a) dual and (b) single port 7T SRAM cell.

The performance of the two 7T cells is explained in the subsequent sub-sections. The performance for the 7TS and 7TD cells is explained in detail in their respective chapter 3 and 4, respectively. But, to provide a common platform for evaluation of the two cells, the performance of the cell for key parameter is provided in subsequent sub-sections to validate their design.

6.4.1. Evaluation of Static Performance of 7TS and 7TD SRAM Bit Cells

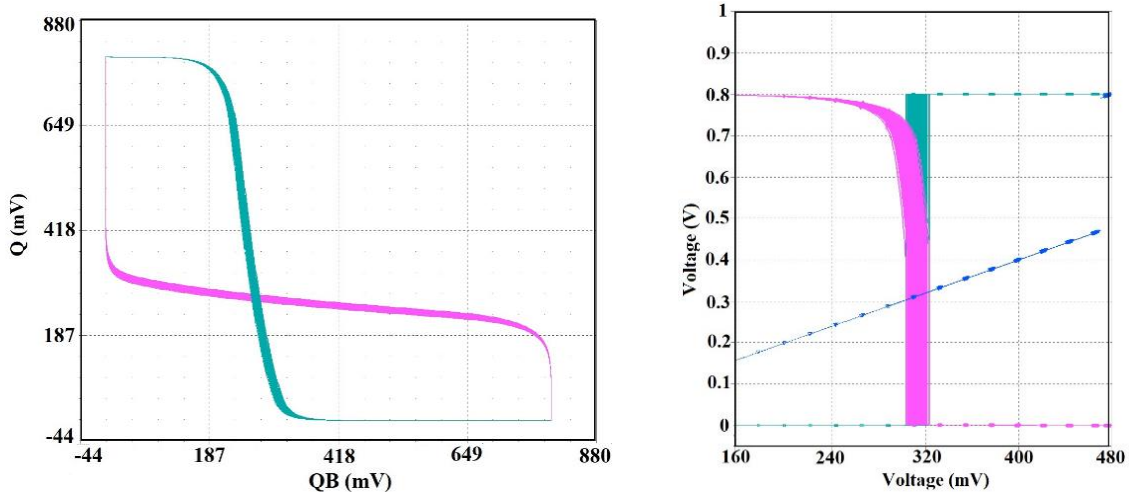
For most part of its operation, the majority cells in the SRAM array are maintained in hold mode. Therefore, it is extremely essential to have high noise tolerance for the cell during its operation. The hold and read operation butterfly for the two cells is identical and is represented in Fig. 6.7 (a). This is because, for the read operation, the read discharge current for the two 7T cells does not pass through the data node for the cell. Therefore, deeming the read operation for the cell to be read SNM free; the possibility of erroneous flip in cell data during read operation is negligible. Thus, the cell has read SNM as high as the hold SNM.



(a) (b)

Fig. 6.7 (a) Hold (read) operation butterfly curve, and (b) write margin curve for the 7T SRAM bit cells.

Consequently, the butterfly curve for the two cells are overlapping, as depicted in Fig. 6.7 (a). The two cells are identical in all respects except the port configuration. The hold and read SNM values for the two cells are also a testament to the same. Both the cells are highly stable against noise with, hold and read SNM values at 324 mV each. The write margin curve for the two cells is depicted in Fig. 6.7 (b). The write margin value obtained for the cells is 480 mV.



(a) (b)

Fig. 6.8 Impact of process variation on (a) hold (read) operation butterfly curve, and (b) write margin curve for the single port and dual port 7T SRAM bit cells.

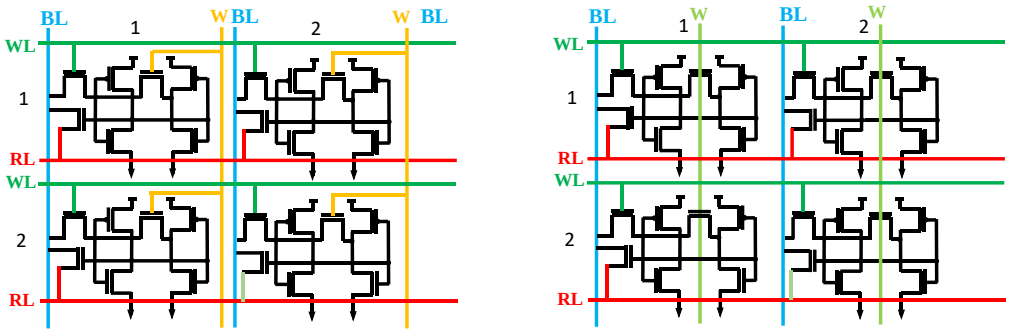
In the nanometer technology node, the impact of process variation on circuit performance becomes significant. Therefore, it is essential to analyze the impact of process variation on the performance of the bit cell. The impact of process variation on the hold (read) SNM and

WM for the 7T cells is shown in Fig. 6.8 (a) and (b) respectively. It may be observed from Fig. 6.8 (a) that hold (read) SNM for the cells may be reduced to 258 mV for highest variation. While the write margin for the cell may rise up to 501 mV. These values are 66 mV lower and 13 mV higher than the typical values recorded for hold (read) SNM and write margin, respectively. Thus, both 7TS and 7TD cells are both resilient to process variation.

6.4.2. Robustness of 7TS and 7TD Cells Against Half Select Disturbance

Analysis of a bit cell is usually done in isolation, with the control signals directly connected to the cell. But in practical terms, a cell is connected with other cells across a row and column. It also shares controls signals with these cells. Consequently, the cells that are present in the same row and column have an impact on the performance of the cell under analysis. When a cell is selected from the memory array, its control signals are exerted in keeping with the requirement of the operation.

The cells that are in the same row and column as the selected cell get half-selected. Thus, when read or write operation is being performed for the selected cell, the cells in the same row and column get half-selected. During this half-selected condition if a cell registers a false read or write event (an erroneous flip in cell data), it is referred to as half-select disturbance (HSD) [142, 148]. This is one of the major drawbacks of memories with shared wordline architecture [141]. To demonstrate the half-select condition for the 7TS and 7TD cell, a sample 2×2 array for the two cells is depicted in Fig. 6.9 (a) and (b) respectively.

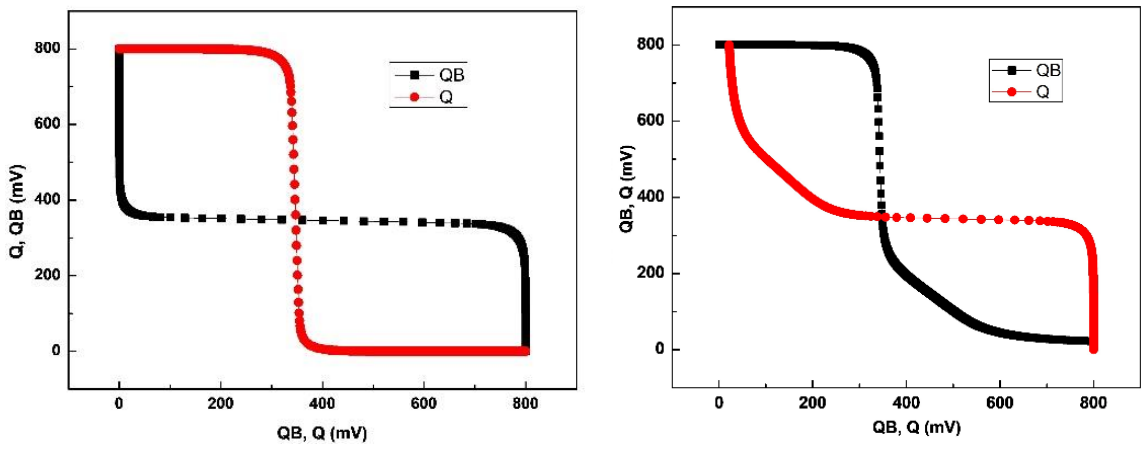


(a) (b)

Fig. 6.9 A 2×2 array representation or the (a) 7TD and (b) 7TS cell.

It has been reported in literature that if access transistors for the half-selected cells are controlled using exclusive row and column signals, the HSD condition can be avoided [154]. Thus, the control signals for 7TS and 7TD are routed to have exclusive row and column

signals for each operation. It can be observed from Fig. 6.9 (a) and (b), that the write controls signals WL and W, are exclusively row and column based, respectively. Thus, when both of them are exerted to select the first row-first column (1-1) cell, the first row-second column (1-2), and second row-first column (2-1) cell are half-selected.



(a) (b)

Fig. 6.10 Butterfly curve for (a) 7TD cell and (b) 7TS cells during the half-select condition.

But the half-selected cells will not register a write operation, as the write operation deems it necessary for the inverter core for the cell to be in cascaded configuration. Thus, the 7TD and 7TS cell are both HSD free for write operation as the two signals WL and W (which steer the cell into write mode) are designed to exclusive row and column signals. But for the read operation the 7TD cell is HSD free, while the 7TS is vulnerable. The RL and RBL signal for the 7TD cell are routed to make them exclusive for row and column, but the 7TS cell is dependent on RL and BL, though they too are routed exclusively for row and column.

The impact of HSD on stability of a cell is measured using butterfly curves. The butterfly curve for half-selected cells - 2-1, and 1-2, during the write operation are depicted in Fig. 6.10 (a) and (b), respectively. It may be observed that 1-2 cell (i.e, the cell in the first row-second column) registers a decline in SNM value at 277 mV. But the SNM values of both the cells are within reasonable range, therefore, they may be deemed resilient to HSD.

6.5 BIT ERROR ANALYSIS OF PROPOSED ARRAY CONFIGURATION

As explained in the previous sections, the proposed hybrid array configuration is based on partitioning the columns for the array into MSBs and LSBs designed using 7TD and 7TS

cells, respectively. The basis for this division is that information stored in the MSB cells is more valuable in comparison to the information stored in the LSB cells.

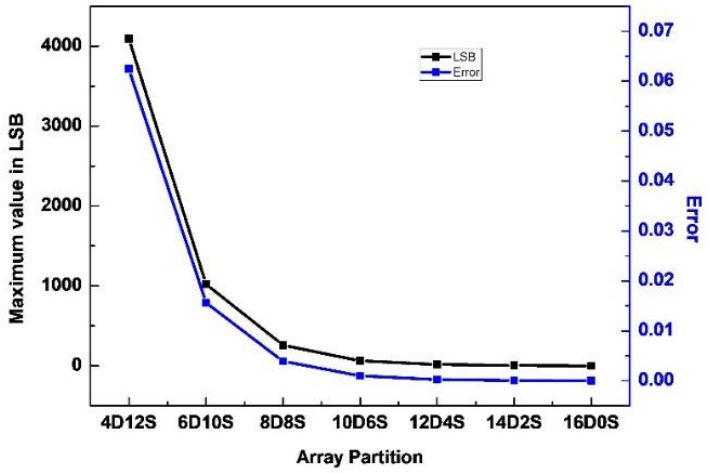


Fig. 6.11 Maximum bit error corresponding information stored in the LSB bits.

If an error is registered by the LSB cells, the eventual information of the word would not change as significantly, as when, information stored in the MSB cell changes. Based on the same, the maximum error for the error is calculated when all the LSB cells register an error in event, this is done to calculate the worst possible error scenario for the array. The error values obtained for the different partitions for the proposed hybrid array configurations are compared in Fig. 6.11. The error values are low for all partitions under six 7TD and ten 7TS (6D10S) configuration. In-fact for partition being ten 7TD cells and six 7TS cells and other partitions values below, the error value approaches zero. Thus, it may be inferred, that depending upon the data sensitivity, the partition for the hybrid array configuration can be anywhere between 6D10S to 14D2S.

6.6 POWER MODEL FOR PROPOSED HYBRID SRAM BIT CELL

Another determining factor for array partition is power consumption. Thus, in this section, the power model for the proposed hybrid array configuration is deduced based on the power model for conventional array configuration [127]. In generalized terms, the array size for the model is assumed to be j×k, with j being the number of rows and k being the number of columns. The partition of the array is done such that n number of columns are assigned to 7TS cell, while (k-n) number of columns assigned to 7TD cells. For ease of understanding the power equations are initially defined individually for 7TS cells and 7TD cells.

Power consumed by the SRAM array can be differentiated based on the different operations (hold, read, and write). The hold power (P_{S_Hold}), read power (P_{S_Read}), and write power (P_{S_Write}) equation for the 1:n 7TS bit cells is as follows:

$$P_{S\_Hold} = j * n * I_{S\_l} * t * V_{DD} \quad (6.1)$$

$$P_{S\_Read} = j * C_{RL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2 \quad (6.2)$$

$$P_{S\_Write} = j * C_{WL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2 + n * C_W \quad (6.3)$$

Here, I_{S_l} represents the leakage current for the single port cell, t is the pulse width needed by the memory for successful operation, C_{RL} is the read wordline capacitance, C_{BL} is the read bitline capacitance, C_{WL} is the write wordline capacitance, and C_W represents the write switch capacitance.

The total power consumption for the array is calculated by adding the power component for hold, read and write operation by including the probability of read (P_{Read}) and write operation (P_{Write}) for the memory. Thus, the total SRAM power for 7TS cells (P_{Ts}) can be expressed as follows –

$$P_{T_S} = P_{Hold} + P_{Read} * P_{S\_Read} + P_{Write} * P_{S\_Write} \quad (6.4)$$

$$P_{T_S} = j * n * I_{S\_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + n * C_{BL} * V_{DD}^2 + n * C_W) \quad (6.5)$$

While the hold power (P_{D_Hold}), read power (P_{D_Read}), and write power (P_{D_Write}) equations for the n+1:k 7TD bit cells is as follows

$$P_{D\_Hold} = j * (k - n) * I_{D\_l} * t * V_{DD} \quad (6.6)$$

$$P_{D\_Read} = j * C_{RL} * V_{DD}^2 + 0.5 * (k - n) * C_{RBL} * V_{DD}^2 \quad (6.7)$$

$$P_{D\_Write} = j * C_{WL} * V_{DD}^2 + 0.5 * (k - n) * C_{WBL} * V_{DD}^2 + (k - n) * C_W \quad (6.8)$$

Here the I_{D_l} represents the leakage current for the dual port cell, C_{RBL} and C_{WBL} are the bitline capacitance for read and write operation, respectively. The difference between the 7TS and 7TD cell is that it separates the BL signal into two RBL and WBL, therefore, two different capacitances are used in these equations. Also, the total power for 7TD cells (P_{TD}) for the array is calculated similar to 7TS cells by adding power component for hold, read and write operation by including the probability of read (P_{Read}) and write operation (P_{Write}).

$$P_{T_D} = P_{Hold} + P_{Read} * P_{S\_Read} + P_{Write} * P_{S\_Write} \quad (6.9)$$

$$P_{T_D} = j * (k - n) * I_{D\_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * (k - n) * C_{RBL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + 0.5\,(k - n) * C_{WBL} * V_{DD}^2 + (k - n) * C_W) \quad (6.10)$$

Thus, the total power for the proposed hybrid array configuration (P_T) can be expressed as follows

$$P_T = P_{T_S} + P_{T_D} \quad (6.11)$$

$$P_T = j * k * I_{S\_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + n * C_{BL} * V_{DD}^2 + n * C_W) + j * (k - n) * I_{D\_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * (k - n) * C_{RBL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + 0.5\,(k - n) * C_{WBL} * V_{DD}^2 + (k - n) * C_W) \quad (6.12)$$

Another, aspect that is essential to note is that the dynamic power for the memory is dependent on the different capacitance - C_{RL}, C_{WL}, C_{BL}, C_W, C_{WBL}, and C_{RBL}. While the static power is dependent on memory density ($D = j \times k$). The impact of read and write operation on the static power is minimal [163]. Assuming that D for the cache memory is constant. Let the density of the first sub array be D_1 and that of the second sub array be D_2. Thus, the total density of the cache memory can be expressed as $D = D_1 + D_2$. The total power (P_T) for the complete cache can be expressed as follows:

$$D = D_1 + D_2 \quad (6.13)$$

$$D_1 = j * n \quad (6.14)$$

$$D_2 = j * (k - n) \quad (6.15)$$

$$P_T = D * I_{S\_l} * t * V_{DD} + P_{Read}\left(j * C_{RL} * V_{DD}^2 + 0.5 * \frac{D_1}{j} * C_{BL} * V_{DD}^2\right) + P_{Write}\left(j * C_{WL} * V_{DD}^2 + \frac{D_1}{j} * C_{BL} * V_{DD}^2 + \frac{D_1}{j} * C_W\right) + D_2 * I_{D\_l} * t * V_{DD} + P_{Read}\left(j * C_{RL} * V_{DD}^2 + 0.5 * \frac{D_2}{j} * C_{BL} * V_{DD}^2\right) + P_{Write}\left(j * C_{WL} * V_{DD}^2 + 0.5 * \frac{D_2}{j} * C_{BL} * V_{DD}^2 + \frac{D_2}{j} * C_W\right) \quad (6.16)$$

The final derived equation 6.16 is used to calculate the power consumption for the hybrid array configuration. The equation is used to determine the power consumption for different partition possibilities for a fixed 8kB array. The power consumption values obtained for the different partitions of the proposed hybrid array are explained in detail in the next section.

6.7 POWER PERFORMANCE ANALYSIS OF PROPOSED ARRAY CONFIGURATION

The power equations for the proposed hybrid array configuration are calculated for a fixed 8kB memory array. In this memory array we have fixed the number of columns to 16 and the rows are maintained at 512. The equations given in the previous section are used to calculate the power consumption for the 8kB memory, to have low power requirement, while maintaining low error possibilities. The array is evaluated for seven different column configurations – four 7TD cell – twelve 7TS cell, six 7TD cells – ten 7TS cells, eight 7TD cell – eight 7TS cell, ten 7TD cell – six 7TS cells, twelve 7TD cell – four 7TS cell, fourteen 7TD cell – two 7TS cell, and sixteen 7TD cell – no 7TS cell. The static and dynamic power consumption curves obtained for the proposed hybrid memory array are depicted in Fig. 6.12.

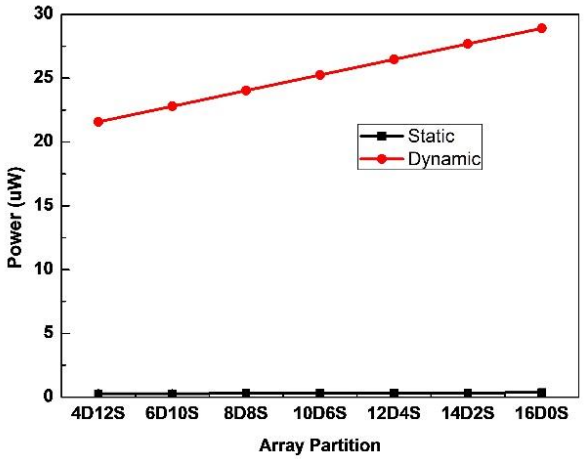


Fig. 6.12 Power consumption curve for the proposed hybrid array configuration for different array partition in absolute terms.

As seen, the dynamic power consumed by the array is high compared to the static power curve. For a fair comparison and to demonstrate that the two power components have similar trends, the power consumption values for static and dynamic components are compared in a double y axis curve in Fig. 6.13. The static power values obtained for the array is in the range of 0.27 µW to 0.37 µW, whereas the dynamic power values for the array, range between 21.5 µW to 29 µW.

It can also be inferred that the variation in static power is higher than that observed for

dynamic power. Thus, if partitioning is done, static power is more deeply impacted in comparison to dynamic power. Also, as the number of dual port cells increases, the static power consumption increases. Thus, it is essential to keep a low count for dual port cells so that power consumption for the array can be lowered. But it must also be ensured that the maximum possible error that the memory may encounter is also low.

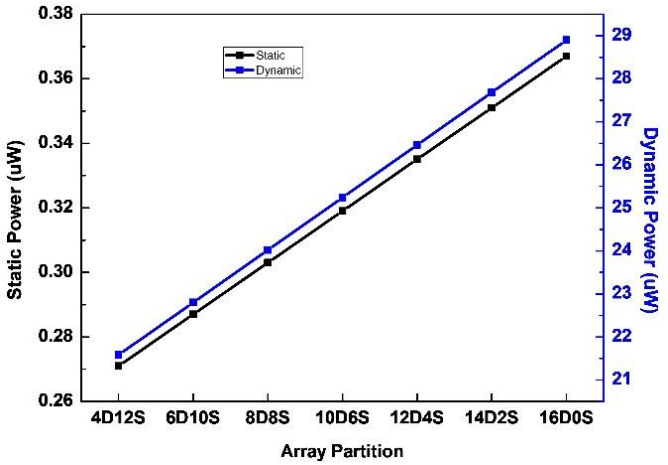
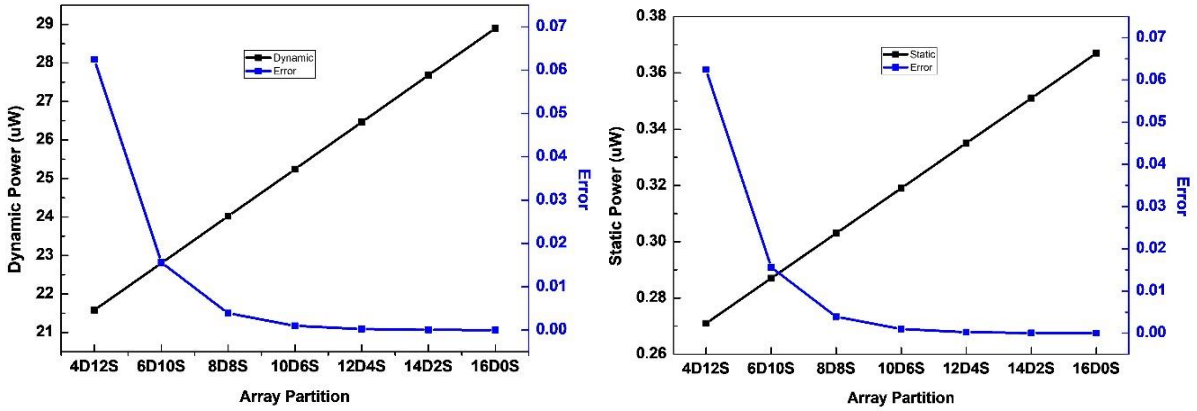


Fig. 6.13 Power consumption curve for the proposed hybrid array configuration for different array partition in relative double y curve.

The maximum error obtained for the memory partitioned (as explained in the previous section) is defined as the maximum error that may occur if all the 7TS cells register a false event. This is done to ensure that even under the worst performance condition, the output obtained will retain information that is within acceptable limits. But previously the static and dynamic power consumed were calculated in isolation with maximum bit error. But it is essential to co-relate the error and power parameter to identify the most appropriate partition for the proposed hybrid array configuration.

The dynamic power consumption and maximum bit error curves are overlapped and presented in Fig. 6.14 (a). While the static power curve overlapped with the maximum error curve for the different column partitions is presented in Fig. 6.14 (b). As, can be observed from Fig. 6.14 (a) and (b), the best results are obtained for the 6D10S partition, that is the sixteen columns of the 8kB array are partitioned such that there are six MSB cells of 7TD configuration, and ten LSB cells of 7TS configuration, the memory array is bound to have low power appetite along with error levels that are within bounds and tolerable.



(a) (b)

Fig. 6.14 Overlap curve for maximum error in keeping with array partition and (a) dynamic power consumption and (b) static power consumption.

At this configuration, the error for the memory is obtained to be 0.016, while the dynamic and static power levels for the memory are maintained at 23 µW and 0.0.29 µW, respectively. These values are 3.5% and 20.7% lower than the static and dynamic power values obtained for memory array designed using only dual port cells. Both power levels are low and therefore, deem the array power efficient and error tolerant.

6.8 SUMMARY OF IMPORTANT RESULTS

The key findings in this chapter are summarized as follows -

1. In this chapter, a hybrid array configuration is proposed to design a lower power memory core. The proposed memory array is designed using two different 7T cells with single port (the best 7T cell configuration identified amongst the proposed cells in chapter 3) and dual port (the 7T cell proposed in chapter 4) configuration.
2. The idea behind using two different cells is that all the bits in a memory word are not equally important. The higher order bits are more important than the lower order bits. Thus, it is inferred that an array may be designed using two different types of cells dedicated for higher order bits and lower order bits, respectively.
3. A detailed overview of the conventional SRAM array, its structure, functioning, and performance is elaborately explained. It is identified that the conventional SRAM array architecture is vulnerable to bit error, and HSD.

4. Additionally, the conventional SRAM array design is dependent on re-use of a single bit cell multiple times. This limits the reduction in power performance and the area footprint for the array.
5. Conventionally, when aiming to reduce power consumption, most researchers target bit cell power reduction. This methodology does reduce power consumption for memory, but it has its limitations. Another, less conventional technique to lower power consumption is changing the array design for the memory.
6. The proposed memory array is partitioned to design higher order bits with dual port 7T cells and lower order bits with single port 7T cells. The memory core and write port for the two cells are identical. The read port topology for the former is isolated, while for the latter it shares bitline with write port.
7. For the proposed hybrid array design, the best results are obtained when the sixteen bit word is partitioned and designed using six dual port cells and ten single port cells.
8. For the proposed partition, the static and dynamic power values obtained for the design are 0.29 µW and 23 µW, respectively. These values are 3.5% and 20.7% lower than the static and dynamic power values obtained for memory array designed using only dual port cells.
9. The error tolerance for this partition is approximately 0.015, which is fairly low, making this hybrid array design low power and error resistant.

CHAPTER – 7

CONCLUSIONS and FUTURE SCOPE

SRAM is an essential component for microprocessors. The decreasing technology node and increasing demand for portable devices with longer battery life has generated the need for re-designing SRAM for performance enhancement. Thus, in this thesis single ended, single port, single ended, dual port bit cell designs are proposed, that have the ability to achieve the same. Also, a new concept for a dual mode operational cell and its functioning is also explained. A compatible single ended sense amplifier topology is also proposed to ensure easy integration for the components of SRAM. Thereafter, for performance optimization a hybrid array configuration is also proposed. Thus in this chapter, the key findings of all chapters are summarized in section 7.1, and further in section 7.2 the future scope for the work is elaborated.

7.1 CONCLUSIONS

SRAM is an essential component for microprocessors and SoC. It is also preferred for cache memory implementation. The memory is formed by an array of bit cells for data storage, and its peripheral circuits. The peripheral circuit comprises of SA, row-column decoders, write drivers, and pre-charge circuitry. The 6T bit cell was the industry standard, but with decreasing technology node and V_{DD} scaling the performance for the 6T cell is deteriorating. This has motivated researchers to design other bit cells with different transistor counts and topology to improve performance. Along with the bit cell design, it is also essential to revisit SA design to make it compatible with newer bit cell topologies. Additional to circuit evaluation, array evaluation is another aspect essential for memory design.

In chapter 2, various existing bit cells topologies, categorized based on transistor count, are reviewed to identify a viable successor for the conventional 6T cell. To improve performance for the bit cell in terms of stability, timing, variation analysis and integration density, researchers have increased transistor count to achieve different targets. But it is observed that as the transistor count increases beyond nine, the area footprint for the cell becomes extremely large making it an unfeasible alternative. Based on the performance

analysis of the cells, the 7T bit cell is identified as the most eligible successor for the conventional differential 6T cell. Thereafter, the different 7T cell topologies based on the number of bitlines and port design are intensively analyzed to identify merit of each topology.

The 7T cells are categorized into the following four topologies – differential ended – single port, differential ended – isolated read port, single ended – dual port, and single ended – single port. Amongst the four different topologies for the 7T cells, the single ended cells are identified as the best performing ones. These cells are dependent on a single bitline for their functioning, thereby drastically lowering the power consumption. Additionally, if it is a dual port cell, the read and write ports are isolated, thereby eliminating the inherent read-write conflict for a bit cell.

Along with the bit cell topologies, the various pre-existing SA topologies are also reviewed. In keeping with the cell design. Conventionally, SAs were also differential in nature, but the growing popularity for single ended cells have prompted designers to design compatible single ended SAs. Additional to the bit cell and SA topology, another crucial aspect for memory is the array design. The bit cell may have low power consumption but owing to the sheer size of the array its power consumption is significant. Therefore, a detailed review of techniques for array implementation is done to determine techniques to eliminate half-select disturbance, lower power consumption and bit error in the circuit.

In chapter 3, based on the literature review, four configurations for single ended, single port 7T bit cell are proposed at 32 nm technology node. The performance for the proposed cells are compared to identify the best possible configuration. The best identified 7T cell is designed using a high performance transistor to boost the dynamic operation for the cell. And the read port for the cell is designed to exclude the data node from the read discharge current path. This helps improve the read stability for the cell. The hold, read, and write noise margin for the cell are 90, 90, and 180 mV respectively for V_{DD} of 300 mV. It requires a 10 ns pulse-width to perform a successful write operation.

MC analysis demonstrates that under 6σ global variation, the cell maintains read as well as hold SNM of 75 mV, while the WM is 215 mV. While for temperature variation analysis, the HSNM and RSNM are reduced by 0.1 mV/ºC. While the WM changes 0.2 mV/ºC. This help validate the reliability of the cell. The standby power of the cell is calculated to be 8.4

and 1.05 pW for Q = '0' and '1', respectively. Additionally, the cell is able to maintain current ratio of 783. All these merit are achieved with a cell of area 0.539 μm^2.

In chapter 4, a single ended, dual port 7T cell is proposed for 32 nm technology node. This cell is like the single ended, single port 7T cell, with the only difference being the read and write port for the cell are isolated. The stability for the hold, read, and write operation for the bit cell is 324, 324, and 488 mV respectively, for V_{DD} of 800 mV. For a successful read and write operation pulse-width of 5 ps and 0.14 ns respectively are required. Temperature variation analysis yields 0.15, 0.15, and 0.24 mV/ºC variation in hold, read, and write noise margin values, respectively. The leakage power consumption for the cell is 256 pW, while the read, and write power consumption for the cell are 6 µW and 1.9 µW, respectively. All the aforementioned merits for the proposed dual port 7T cell are achieved with a minimal layout area of 0.553 μm^2.

The growing popularity of hyper-personalized devices and round the clock connectivity has generated the need for a bit cell that can switch between low power and high speed operation. Thus, concept for a dual mode operational bit cell is also proposed in chapter 4. The dual mode operational cell is designed using the proposed single ended, single port 7T cell and single ended, dual port 7T cell. The single port cell is more suitable for low power applications and the dual port cell is better for high speed operation. Therefore, as per the requirement of the circuit at a given instant, the different configurations for the cell may be used.

The growing demand for single ended cells has also generated the need for a single ended SA topology. Thus, in chapter 5, a single ended switching NMOS based SA is proposed for 32 nm technology node. It operates in two phases – the pre-charge phase and the evaluation phase. This two-phase functioning for the proposed SA ensures there is minimal power consumption for the topology when the memory is not executing the read operation. Its pulse-width requirement of 0.32 ns is significantly lower in comparison to its counterparts. While its leakage power is least amongst the different SA topologies at 4 nW. The additional advantage the proposed SA has its lower area footprint of 7.65 μm^2.

A bit cell is a small peg in a wide m×n matrix that forms the memory core for data storage. Conventionally, a bit cell is replicated to create the entire array. But, in a typical multimedia application the lower order bits may be more vulnerable to noise than higher order bits.

Hence, appreciable performance and minimal image quality degradation can be achieved by using two different bit cells for array formation.

A hybrid array configuration using two different 7T bit cells topologies is proposed in chapter 6. The best results are obtained when six dual port and ten single port cells are used to design the array. The static and dynamic power values obtained for the design are 0.29 µW and 23 µW, respectively. These values are 3.5% and 20.7% lower than the static and dynamic power values obtained for memory array designed using only dual port cells. Also, the error tolerance for this partition is approximately 0.015, which is fairly low, making this hybrid array design low power and error resistant.

7.2 FUTURE SCOPE

Based on research carried out in this thesis and the reported results, the following future scope is suggested.

A bit cell is the key component for memory. It is the key focus of researchers for improving memory performance. But most researchers pre-dominantly focus on design of the bit cell, its transistor count and control signal. But, when the transistor count goes beyond ten, the increase in area for the cell outweighs all its performance merits. Presently, for low power applications promising results are obtained for memory cells designed using negative differential resistance circuits (NDR). The NDR circuit is used to alter the memory core for the cell. The major highlight of NDR based memory cell is that it can be designed using only four transistors. Thereby significantly lowering its transistor count, area, and V_{DD}. Therefore, it is essential for researchers to explore this technique and propose cells with similar techniques that are unique and focus on modifying the latch based memory core for performance improvement for the bit cell.

Along, with the conventional bit cell design, the concept for dual mode operational bit cell can also be explored as a potential for IoT application. Presently, in this thesis, the concept for dual mode cell and its performance is presented. The concept as well as the cell design can be further extended and modified for application specific requirements. Also, it to be used a foundational unit for memory design; array analysis can be performed and optimized for the dual mode cell as well. Additionally, there is possibility of designing a dual mode operation SA, for easy integration with the dual mode cell.

As the bit cell for the memory is altered, it mandates re-designing its corresponding SA topology as well. Present day SAs are efficient but still face a major bottleneck in terms of V_{DD} lowering. This also hampers lowering the operational V_{DD} for the cell, as the two have to work in conjunction. Thus, it is essential to come up with design techniques and circuit modifications that enable V_{DD} lowering of the memory. Additional to lowering the voltage, it is also essential to check if the concept of NDR is applicable to SA. To check if there is a possibility, to alter the latch based voltage mode SA to be designed with a different core. This will open a new dimension for designing memory.

The array analysis is another essential parameter for memory. It has the capability to analyze the performance of the memory. For array, most research revolves around cell stability, HSD, read-write timing analysis, power models, and array size optimization. But parameters such as bit-interleaving, sub-bank sizing, and divided wordline architecture for memory are fields that have potential for array performance optimization. These are areas that are purely array centric and do not rely on modifying and improving the performance of the cell. These array analysis factors have not received as much attention but hold immense potential for performance enhancement for memory.

REFERENCES

[1] M. H. Abu-Rahma and M. Anis, "Nanometer variation-tolerant SRAM: circuits and statistical design for yield," Springer, New York, 2013, 5-7.

[2] S. Miao, P. Ou, X. Zhou and L. Wang, "Zero-hardened SRAM cells to improve soft error tolerance in FPGA," in *2008 Second International Symposium on Intelligent Information Technology Application*, 20-22 December 2008.

[3] G. Prasad and A. Anand, "Statistical analysis of low-power SRAM cell structure," Analog Integrated Circuits and Signal Processing, vol. 82, pp. 349-358, January 2015.

[4] R. Mukherjee, P. Saha, I. Chakrabarti, P. K. Dutta and A. K. Ray, "Fast adaptive motion estimation algorithm and its efficient VLSI system for high definition videos," Expert Systems with Applications, vol. 101, pp. 159–175, July 2018.

[5] K. Gavaskar, U. S. Ragupathy and V. Malini, "Design of novel SRAM cell using hybrid VLSI techniques for low leakage and high speed in embedded memories," Wireless Personal Communications, vol. 108, no. 4, pp. 2311-2339, October 2019.

[6] K. Gavaskar and U. S. Ragupathy, "An efficient design and comparative analysis of low power memory cell structures," in *2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE)*, 6-8 Mar. 2014, pp. 1-5.

[7] R. Lorenzo and R. Pailly, "Single bit-line 11T SRAM cell for low power and improved stability," IET Computers and Digital Techniques, vol. 14, no. 3, pp. 114-121, March 2020.

[8] A. P. S. Rathod, P. Lakhera, A. K. Baliga, P. Mittal and B. Kumar, "Performance comparison of pass transistor and CMOS logic configuration based de-multiplexers," in *International Conference on Computing, Communication & Automation*, 15-16 May 2015, pp. 1433-1437.

[9] R. Lorenzo and S. Chaudhury, "A novel 9T SRAM architecture for low leakage and high performance," Analog Integrated Circuits and Signal Processing, vol. 92, pp. 315-325, August 2017.

[10] J. Boley, J. Wang and B. H. Calhoun, "Analyzing sub-threshold bitcell topologies and the effects of assist methods on SRAM Vmin," Journal of Low Power Electronics and Applications, vol. 2, no. 2, pp. 143–154, April 2012.

[11] D. Nayak, D. P. Acharya and K. Mahapatra, “An improved energy efficient SRAM cell for access over a wide frequency range,” Solid State Electronics, vol. 126, pp. 14-22, December 2016.

[12] K. Raj, B. Kumar and P. Mittal, “FPGA implementation of mask level CMOS layout design of redundant binary signed digit comparator,” International Journal of Computer Science and Network Security, vol. 9, no. 9, pp. 107-115, September 2009.

[13] R. Lorenzo and S. Chaudhury, “A novel SRAM cell design with a body-bias controller circuit for low leakage, high speed and improved stability,” Wireless Personal Communications, vol. 94, pp. 3513-3529, June 2017.

[14] T. S. Kumar and S. L. Tripathi, “Process evaluation in FinFET based 7T SRAM cell,” Analog Integrated Circuits and Signal Processing, vol. 109, pp. 545-551, December 2021.

[15] K. Gavaskar, P. Sivaranjani, S. Elango and G. N. Raja, “Low power SRAM cell and array structure in aerospace applications: single–event upset impact analysis,” Wireless Personal Communications, vol. 129, pp 37-55, March 2023.

[16] Y. C. Lai and S. Y. Huang, “A resilient and power-efficient automatic-power down sense amplifier for SRAM design,” IEEE Transactions on circuits and Systems II: Express briefs, vol. 55, no. 10, pp. 1031-1035, October 2008.

[17] Divya, P. Mittal, B. Rawat and B. Kumar, “Design and performance analysis of high-performance low power voltage mode sense amplifier for static RAM,” International Journal of Advances in Electrical and Electronic Engineering, vol. 19, no. 2, pp. 145-154, 2022.

[18] K. Zhang, K. Hose, V. De and B. Senyk, “The scaling of data sensing schemes for high speed cache design in sub-0.18 μ/m technologies,” in *2000 Symposium VLSI Circuits. Digest of Technical Papers*, 15-17 Jun. 2000, pp. 226–227.

[19] Divya and P. Mittal, “A low-power high-performance voltage sense amplifier for static RAM and comparison with existing current/voltage sense amplifiers,” International Journal of Information Technology, vol. 14, pp. 323-331, June 2022.

[20] E. Seevinck, P. J. V. Beer and H. Ontrop, “Current-mode techniques for high-speed VLSI circuits with application to current SA for CMOS SRAM’s,” IEEE Journal Solid-State Circuits, vol. 26, no. 4, pp. 525–536, April 1991.

[21] R. Singh and N. Baht, “An offset compensation technique for latch type sense amplifiers in high-speed low-power SRAMs,” IEEE Transactions VLSI System Transaction Briefs, vol. 12, no. 6, pp. 652–657, June 2004.

[22] R. Sarpeshkar, J. L. Wyatt, N. C. Lu and P. D. Gerber, “Mismatch sensitivity of a simultaneously latched CMOS sense amplifier,” IEEE Journal Solid-State Circuits, vol. 26, no. 10, pp. 1413–1422, October 1991.

[23] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel, “Yield and speed optimization of a latch-type voltage sense amplifier,” IEEE Journal Solid-State Circuits, vol. 39, no. 7, pp. 1148–1158, July 2004.

[24] S. Pal and A. Islam, “Variation Tolerant Differential 8T SRAM cell for ultralow power applications,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 4, pp. 549-558, April 2016.

[25] K. Cho, J. Park, T.W. Oh and S.O. Jung, “One-sided schmitt-trigger-based 9T SRAM cell for near-threshold operation,” IEEE Transactions on Circuits and Systems I: Regular papers, vol. 67, no. 5, pp. 1551-1561, May 2020.

[26] J. Jiang, Y. Xu, W. Zhu, J. Xiao and S. Zou, “Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications,” IEEE Transactions on circuits and systems I: Regular papers, vol. 66, no. 3, pp. 967-977, March 2019.

[27] S. Pal and A. Islam, “9T SRAM Cell for reliable ultralow-power applications and solving multibit soft-error issue,” IEEE Transactions on Device and Materials Reliability, vol. 16, no. 2, pp. 172-182, June 2016.

[28] A. P. Shah, N. Yadav, A. Beohar and S. K. Vishvakarma, “On-chip adaptive body bias for reducing the impact of NBTI on 6T SRAM cells,” IEEE Transactions on Semiconductor Manufacturing, vol. 31, no. 2, pp. 242-249, May 2018.

[29] M.-H. Chang, Y.-T. Chiu and W. Hwang, “Design and iso-area Vmin analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS,” IEEE Transactions on Circuits Systems II: Express Briefs, vol. 59, no. 7, pp. 429–433, July 2012.

[30] S. A. Pourbakhsh, X. Chen, D. Chen, X. Wang, N. Gong and J. Wang, “Sizing-priority based low-power embedded memory for mobile video applications,” in *2016 17th International Symposium on Quality Electronic Design (ISQED)*, 15-16 Mar. 2016.

[31] Semiconductor Industry Association (SIA), International technology roadmap for semiconductors, (2013).

[32] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R.K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Digest of Technical Papers. 2005 Symposium on VLSI Technology*, 14-16 Jun. 2005.

[33] S. O. Toh, Z. Guo, T.-J. K. Liu and B. Nikolic, "Characterization of dynamic SRAM stability in 45nm CMOS," IEEE Journal of Solid-State Circuits, vol. 46, no. 11, pp. 2702-2712, November 2011.

[34] B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for subthreshold SRAM in 65-nm CMOS," IEEE Journal Solid-State Circuits, vol. 41, no. 7, pp. 1673–1679, July 2006.

[35] B. Yang and L. Kim, "A low-power SRAM using hierarchical bit line and local sense amplifiers," IEEE Journal of Solid-State Circuit, vol. 40, no. 6, pp. 1366–1376, June 2005.

[36] R. F. Hobson, "A new single-ended SRAM cell with write-assist," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 2, pp. 173–181, February 2007.

[37] H. I. Yang, M. H. Chang, S. Y. Lai, H. F. Wang and W. Hwang, "A low-power low-swing single-ended multi-port SRAM," in *2007 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, 25-27 Apr. 2007, pp. 28–31.

[38] S. A. Sil, S. Ghosh and M. A. Bayoumi, "A novel 90 nm 8T SRAM cell with enhanced stability," in *IEEE International Conference on Integrated Circuit Design Technology (ICICDT)*, 30 May – 1 June, 2007.

[39] H. Noguchi, S. Okumura, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi and M. Yoshimoto, "Which is the best dual-port SRAM in 45-nm process technology? 8T, 10T single ended and 10T differential," in *Proceedings of International Conference in Integrated Circuit Design and Technology (ICICDT)*, 2-4 June 2008, pp. 55-58.

[40] V. Sharma, S. Vishvakarma, S. S. Chouhan and K. Halonen, "A write improved low power 12T SRAM cell for wearable wireless sensor nodes," International Journal of Circuit Theory Application, vol. 46, no. 12, pp. 2314-2333, December 2018.

[41] K. Cho, J. Park, T. W. Oh and O. K. Jung, "One sided schmitt-trigger based 9T SRAM cell for near threshold operation," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 5, pp. 1551-1561, May 2020.

[42] N. Mishra, P. Mittal and B. Kumar, "Analytical modeling for static and dynamic response of organic pseudo all-p inverter circuits," Journal of Computational Electronics, vol. 18, pp. 1490–1500, December 2019.

[43] J. P. Kulkarni and K. Roy, "Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 319–332, February 2012.

[44] G. Rawat, K. Rathore, S. Kala and P. Mittal, "Design and analysis of ALU: vedic mathematics approach," in *International Conference on Computing, Communication & Automation*, 15-16 May 2015, pp. 1372-1376.

[45] M. Kumar and J. S. Ubhi, "Design and analysis of CNTFET based 10T SRAM for high performance at nanoscale," International Journal of Circuit Theory Applications, vol. 47, no. 11, pp. 1775-1785, November 2019.

[46] R. Faraji, H. R. Naji, M. R. Nezhad and M. Arabnejhad, "A new SRAM design using body bias technique for low power and high-speed application," International Journal of Circuit Theory Applications, vol. 42, no. 11, pp. 1189-1202, November 2014.

[47] D. Anitha, K. Manjunathachari, P. S. Kumar and G. Prasad, "Design of low leakage process tolerant SRAM cell," Analog Integrated Circuits and Signal Processing, vol. 93, pp. 531–538, December 2017.

[48] P. Mittal and N. Kumar, "Comparative analysis of 90nm MOSFET and 18nm FinFET based different Multiplexers for low power digital circuits," International Journal of Advanced Science and Technology, vol. 29, no. 8, pp. 4089-4096, 2020.

[49] N. Surana and J. Mekie, "Energy efficient single-ended 6-T SRAM for multimedia applications," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 1023-1027, June 2019.

[50] R. N. Asli and S. Taghipour, "Reliable and high-performance asymmetric FinFET SRAM cell using back-gate control," Microelectronics Reliability, vol. 104, pp. 113545, January 2020.

[51] R. E. Aly and M. A. Bayoumi, "Low-power cache design using 7T SRAM cell," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 4, pp. 318-322, April 2007.

[52] Y. Yang, H. Jeong, S. C. Song, J. Wang, G. Yeap and S. O. Jung, "Single bit-line 7T SRAM cell for near-threshold voltage operation with enhanced performance and energy in 14 nm FinFET technology," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 7, pp. 1023, July 2016.

[53] K. Sanapala, S. R and S. S. Yeo, "Schmitt trigger-based single-ended 7T SRAM cell for Internet of Things (IoT) applications," Journal of Supercomputing, vol. 74, pp. 4613-4622, September 2018.

[54] S. Ahmad, S. A. Ahmad, M. Muqeem, N. Alam and M. Hasan, "TFET-based robust 7T SRAM cell for low power application," IEEE Transactions in Electron Devices, vol. 66, no. 9, pp. 3834-3840, September 2019.

[55] J. S. Liu, M. B. Clavel and M. K. Hudait, "An energy-efficient tensile strained Ge/InGaAs TFET 7T SRAM cell architecture for ultra-low voltage applications," IEEE Transactions on Electron Devices, vol. 64, no. 5, pp. 2193–2200, May 2017.

[56] L. Wen, X. Cheng, K. Zhou, S. Tian and X. Zeng, "Bit-Interleaving-enabled 8T SRAM with shared data-aware-write and reference-based sense amplifier," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 7, pp. 643-647, July 2016.

[57] S. Lin, Y. B. Kim and F. Lombardi, "A highly-stable nanometer memory for low power design," in *Proceedings of IEEE International Workshop Design Test of Nano Devices, Circuits Systems*, 29-30 September 2008, pp. 17-20.

[58] P. Singh and S. K. Vishvakarma, "Ultra-low power high stability 8T SRAM for application in object tracking system," IEEE Access, vol. 6, pp. 2279-2290, December 2017.

[59] Y. Yang, J. Park, S. C. Song, J. Wang, G. Yeap and S. -O. Jung, "Single-ended 9T SRAM cell for near-threshold voltage operation with enhanced read performance in 22-nm FinFET technology," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 11, pp. 2748-2752, November 2015.

[60] K. Cho, J. Park, T. W. Oh and O. K. Jung, "One sided schmitt-trigger Based 9T SRAM cell for near threshold operation," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 5, pp. 1551, May 2020.

[61] A. S. Rajput, M. Pattanaik and R.K. Tiwari, “Design and analysis of schmitt trigger Based 10T SRAM in 32 nm Technology node,” in *2017 IEEE Symposium on Nanoelectronics and Information Systems*, 18-20 Dec. 2017.

[62] J. P. Kulkarni and K. Roy, "Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 319–332, February 2012.

[63] J. P. Kulkarni, K. Kim and K. Roy, "A 160 mV robust schmitt trigger based subthreshold SRAM," IEEE Journal of Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, October 2007.

[64] E. Shakouri, B. Ebrahimi, N. Eslami and M. Chahardori, "Single-ended 10T SRAM cell with high yield and low standby power," Circuits, Systems and Signal Processing, vol. 40, pp. 3479-3499, July 2021.

[65] G. Pasandi and M. Pedram, "Internal write-back and read-before-write schemes to eliminate the disturbance to the half-selected cells in SRAMs," IET Circuits Devices Systems, vol. 12, no. 4, pp. 460–466, July 2018.

[66] C. B. Kushwah, and S. K. Vishvakarma, "A single-ended with dynamic feedback control 8T subthreshold SRAM cell," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 42, no. 1, pp. 373-377, January 2016.

[67] R. Giterman, M. Vicentowski, I. Levi, Y. Weizman, O. Keren and A. Fish, "Leakage power attack-resilient symmetrical 8T SRAM cell," IEEE Transactions on Very Large Integration (VLSI) Systems. vol. 26, no. 10, pp. 2180-2184, October 2018.

[68] S. Pal, S. Bose, W. H. Ki and A. Islam, "Characterization of half-select free write assist 9T SRAM cell," IEEE Transactions on Electron Devices, vol. 66, no. 11, pp. 4745-4752, November 2019.

[69] N. Eslami, B. Ebrahimi, E. Shakouri and D. Najafi, "A single-ended low leakage and low voltage 10T SRAM cell with high yield," Analog Integrated Circuits and Signal Processing, vol. 105, pp. 263-274, November 2020.

[70] Y. He, J. Zhang, X. Wu, X. Si, S. Zhen and B. Zhang, "A half-select disturb-free 11T SRAM cell with built-In write/read-assist scheme for ultralow-voltage operations," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 10, pp. 2344-2353, October 2019.

[71] R. Lorenzo and R. Pailly, "Single bit-line 11T SRAM cell for low power and improved stability," IET Computer & Digital Techniques, vol. 14, no. 3, pp. 114-121, May 2020.

[72] J. Jiang, Y. Xu. W. Zhu, J. Xiao and S. Zou, "Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications," IEEE

Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 967-977, March 2019.

[73] A. Sachdeva and V. K. Tomar, "A schmitt-trigger based low read power 12T SRAM cell," Analog Integrated Circuits and Signal Processing, vol. 105, pp. 275-295, November 2020.

[74] L. Atias, A. Teman, R. Giterman, P. Meinerzhagen and A. Fish, "A low-voltage radiation-hardened 13T SRAM bitcell for ultralow power space applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 8, pp. 2622-2633, August 2016.

[75] S. Negi, A. Rana, A. K. Baliga, P. Mittal and B. Kumar, "Performance analysis of dual gate organic thin film transistor and organic SR latch application," in *International Conference on Computing, Communication & Automation*, pp. 1427-1432, 15-16 May 2015.

[76] R. Krishna and P. Duraiswamy, "Low leakage 10T SRAM cell with improved data stability in deep sub-micron technologies," Analog Integrated Circuits and Signal Processing, vol. 109, pp. 153-163, October 2021.

[77] R. W. Mann, J. Wang, S. Nalam, S. Khanna, G. Braceras, H. Pilo and B. H. Calhoun, "Impact of circuit assist method on margin and performance in 6T SRAM," Solid State Electronics, vol. 54, no. 11, pp. 1398-1407, November 2010.

[78] B. K. N. Reddy, C. Ramalingaswamy, R. Nagulapalli and D. Ramesh, "A novel 8T SRAM with improved cell density," Analog Integrated Circuits and Signal Processing, vol. 98, pp. 357-366, February 2019.

[79] add

[80] J. Singh, S. P. Mohanty and D. K. Pradhan, "Robust SRAM designs and analysis," New York: Springer, 2013.

[81] S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, "Single-ended schmitt trigger based robust low power SRAM cell," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 8, pp. 2634-2642, August 2016.

[82] A. Islam and M. Hasan, "Leakage characterization of 10T SRAM cell," IEEE Transactions on Electron Devices, vol. 59, no. 3, pp. 631-638, March 2012.

[83] T. Doorn, E. T. Maten, J. Croon, J. D. Bucchianico and O. Wittich, "Importance sampling Monte Carlo simulations for accurate estimation of SRAM yield," in

ESSCIRC 2008 - 34th European Solid-State Circuits Conference, 15-19 September 2008.

[84] T. S. Kumar and S. L. Tripathi, "Process evaluation in FinFET based 7T SRAM cell," Analog Integrated Circuits and Signal Processing, vol. 109, pp. 545–551, December 2021.

[85] J. Ding and A. Asenov, "The analysis of static random access memory stability under the influence of statistical variability and bias temperature instability-induced aging," Semiconductor Science and Technology, vol. 36, no. 2, pp. 025008, February 2021.

[86] M. Ansari, H. Afzali-Kusha, B. Ebrahimi, Z. Navabia and A. Afzali-Kusha, "A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies," Elsevier Journal of Integration the VLSI Journal, vol. 50, pp. 91–106, June 2015.

[87] R. N. Asli and S. Taghipour, "A near-threshold soft error resilient 7T SRAM cell with low read time for 20 nm FinFET technology," Journal of Electronic Testing, vol. 33, pp. 449-462, August 2017.

[88] S. C. Chung, C. Hou, K.L. Chen and L. C. Lu, "Method of using mixed multi-Vt devices in a cell based design," US7281230B2, October 9, 2007.

[89] R. Giterman, O. Keren and A. Fish, "A 7T security oriented SRAM bitcell," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 8, pp. 1396-1400, August 2019.

[90] J.S. Oh, J. Park, K. Cho, T.W. Oh and S.O. Jung, "Differential read/write 7T SRAM with bit-interleaved structure for near-threshold operation," IEEE Access, vol. 9, 64104-64115, April 2021.

[91] B.H. Calhoun and A.P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultralow-voltage operation," IEEE Journal on Solid-State Circuit, vol. 42, no. 3, pp. 680–688, March 2007.

[92] K. C. Chun, W. Zhang, P. Jain and C. H. Kim, "A 2T1C embedded DRAM macro with no boosted supplies featuring a 7T SRAM based repair and a cell storage monitor," IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2517-2526, October 2012.

[93] J. Lin, I. Rahim, Y. Xu and A. L. Lee, "Memory circuit with PMOS access transistors," US8995175B1, March 31, 2015.

[94] Y. Lee, D. Kim, J. Cai, I. Lauer, L. Chang, S.J. Koester and D. Blaauw, "Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs)," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 9, pp. 1632–1643, September 2013.

[95] S. A. Tawfik and V. Kursun, "Low power and robust 7T dual-Vt SRAM circuit," in *Proceedings IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1452–1455, 18-21 May 2008.

[96] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi and H. Akamatsu, "A stable 2-port SRAM cell design against simultaneously read/write-disturbed accesses," IEEE Journal on Solid-State Circuit, vol. 43, no. 9, pp. 2109–2119, September 2008.

[97] S. Gupta, K. Gupta and N. Pandey, "A 32-nm subthreshold 7T SRAM bit cell with read assist," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 12, pp. 3473–3483, December 2017.

[98] P. Mittal, Y. S. Negi and R. K. Singh, "A depth analysis for different structures of organic thin film transistors: modeling of performance limiting issues," Microelectronics Engineering, vol. 150, pp. 7–18, January 2016.

[99] C. Roy and A. Islam, "Power-aware source feedback single-ended 7T SRAM cell at nanoscale regime," Microsystems Technologies, vol. 25, no. 5, pp. 1783-1791, May 2017.

[100] A. Teman, L. Pergament, O. Cohen and A. Fish, "A 250 mV 8 kb 40 nm ultra-low power 9T supply feedback SRAM (SF-SRAM)," IEEE Journal on Solid State Circuits, vol. 46, no. 11, pp. 2713–2726, September 2011.

[101] K. Zhang, K. Hose, V. De and B. Senyk, "The scaling of data sensing schemes for high speed cache design in sub-0.18 μ/m technologies," in *Symposium on VLSI Circuits Digest of Technical Papers*, 15-17 Jun. 2000, pp. 226-227.

[102] R. Houle, "Simple statistical analysis techniques to determine minimum sense amp set times," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 16-19 Sept. 2007, pp. 37-40.

[103] L. Pileggi, G. Keskin, L. Xin, M. Ken and J. Proesel, "Mismatch analysis and statistical design at 65 nm and below," in *2008 IEEE Custom Integrated Circuits Conference*, 21-24 Sept. 2008, pp. 9-12.

[104] T. Seki, E. Itoh, C. Furukawa, I. Maeno, T. Ozawa, H. Sano and N. Suzuki, "A 6-ns 1-Mb CMOS SRAM with latched sense amplifier," IEEE Journal Solid-State Circuits, vol. 28, no. 4, pp. 478-483, April 1993.

[105] J. M. Hill and J. Lachman, "A 900 MHz 2.25 MB cache with on-chip CPU—now in Cu SOI," in *IEEE International Solid-State Circuits Conference Digital Technical Papers*, 07 Feb. 2001, pp. 176-177.

[106] T. N. Blalock and R. C. Jaeger, "A high speed clamped bit-line current mode sense amplifier," IEEE Journal of Solid-State Circuits, vol. 26, no. 4, pp. 542-548, April 1991.

[107] J. Zhu, N. Bai and J. Wu, "A review of sense amplifiers for static random access memory," IETE Technical Review, vol. 30, no. 1, pp. 72-81, September 2013.

[108] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," IEEE Journal on Solid-State Circuits, vol. 28, no. 4, pp. 523-527, April 1993.

[109] B. Wicht, T. Nirschl and D. S. Landsiedel, "A yield-optimized latch-type SRAM sense amplifier," in *Proceedings of the 29th European Solid-State Circuits Conference*, 16-18 Sept. 2003, pp. 409-412.

[110] V. G. Nikolic, V. Oklobdzija, J. Stojanovic, C. Wenyan, J. K. Shing and M. K. T. Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," IEEE Journal on Solid-State Circuits, vol. 35, no. 6, pp. 876-884, June 2000.

[111] K. L. Wong and C. K. Yang, "Offset compensation in comparators with minimum input-referred supply noise," IEEE Journal on Solid-State Circuits, vol. 39, no. 5, pp. 837-840, May 2004.

[112] K. Sasaki, K. Ishibashi, T. Yamanaka, K. Shimohigashi, N. Moriwaki and S. Honjo, "A 23 ns 4 Mb CMOS SRAM with 0.5 uA standby current," in *IEEE International Solid-State Circuits Conference*, 14-16 Feb. 1990, pp. 130-131.

[113] D. Patel and M. Sachdev, "0.23-V sample-boost-latch based offset tolerant sense amplifier," IEEE Solid State Circuit Letters, vol. 1, no. 1, pp. 6-9, January 2018.

[114] W. Bogaerts and L. Chrostowski, "Silicon photonics circuit design: methods, tools and challenges," Laser & Photonics Review, vol. 12, no. 4, pp. 1700237, April 2018.

[115] H. Jeong, T. Kim, T. Son, G. Kim and S. O. Jung, "Trip-point bit-line precharge sensing scheme for single-ended SRAM," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 7, pp. 1370-1374, July 2014.

[116] L. Chang, R. K. Montoye, Y. Nakamura, K. A. Batson, R. J. Eickemeyer, R. H. Dennard, W. Haensch and D. Jamsek, "An 8 T-SRAM for variability tolerance and low-voltage operation in high-performance caches," IEEE Journal on Solid-State Circuits, vol. 43, no. 4, pp. 956-963, April 2008.

[117] S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka, Y. Oda, T. Yoshihara, M. Igarashi, M. Takeuchi, H. Kawashima, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, H. Makino, K. Ishibashi and H. Shinohara, "A 65-nm SOC embedded 6 T-SRAM designed for manufacturability with read and write operation stabilizing circuits," IEEE Journal on Solid-State Circuits, vol. 42, no. 4, pp. 820-829, April 2007.

[118] J. D. Warnock, Y.-H. Chan, S. M. Carey, H. Wen, P. J. Meaney, G. Gerwig, H. H. Smith, Y. H. Chan, J. Davis, P. Bunce, A. Pelella, D. Rodko, P. Patel, T. Strach, D. Malone, F. Malgioglio, J. Neves, D. L. Rude and W. V. Huott, "Circuit and physical design implementation of the microprocessor chip for the Enterprise system," IEEE Journal on Solid-State Circuits, vol. 47, no. 1, pp. 151-163, January 2012.

[119] H. Jeong, T. Kim, K. Kang, T. Song, G. Kim, H. S. Won and S. O. Jung, "Switching pMOS sense amplifier for high density low voltage single–ended SRAM," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 6, pp. 1555-1563, June 2015.

[120] M.-F. Chang, J.-J. Wu, T. F. Chien, Y.-C. Liu, T.-C. Yang, W.-C. Shen, Y.-C. King, C.-J. Lin, K.-F. Lin, Y.-D. Chih, S. Natarajan and J. Chang, "Embedded 1Mb ReRAM in 28 nm CMOS with 0.27-to-1 V read using swing-sample-and-couple sense amplifier and self-boost-write-termination scheme," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 09-13 Feb. 2014, pp. 332-333.

[121] M. Qazi, K. Stawiasz, L. Chang and A. P. Chandrakasan, "A 512 kb 8T SRAM macro operating down to 0.57 V with an AC-coupled sense amplifier and embedded data-retention-voltage sensor in 45 nm SOI CMOS," IEEE Journal of Solid-State Circuits, vol. 46, no. 1, pp. 85-96, January 2011.

[122] N. Verma and A. P. Chandrakasan, "A high-density 45 nm SRAM using small-signal non-strobed regenerative sensing," IEEE Journal on Solid-State Circuits, vol. 44, no. 1, pp. 163-173, January 2009.

[123] J. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Englewood Cliffs, NJ: Prentice Hall, 2002, pp. 308-309.

[124] L. Chang, Y. Nakamura, R. Montoye, J. Sawada, A. Martin, K. Kinoshita, F. Gebara, K. Agarwal, D. Acharyya, W. Haensch, K. Hosokawa and D. Jamsek, “A 5.3 GHz 8 T-SRAM with operation down to 0.41 V in 65 nm CMOS,” in *IEEE Symposium on VLSI Circuit*s, 14-16 Jun. 2007, pp. 252-253.

[125] S. Mukhopadhyay, H. Mahmoodi and K. Roy, “Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 12, pp. 1859-1880, December 2005.

[126] I. J. Chang, D. Mohapatra and K. Roy, “A priority-based 6T/8T Hybrid SRAM architecture for aggressive voltage scaling in video application,” IEEE Transactions on Circuits and Systems for Video Technology, vol. 21, no. 2, pp. 101-112, February 2011.

[127] A. Garg and T. T. H. Kim, “SRAM array structures for energy efficiency enhancement,” IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 60, no. 6, pp. 351-355, June 2013.

[128] G. Pasandi and S. M. Fakhraie, “A 256-kb 9T near-threshold SRAM with 1k cells per bitline and enhanced write and read operations,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 11, pp. 2438-2446, November 2015.

[129] J. H. Park, D. Jeon and H. S. Kim, “A 8T SRAM Cell With reduced Vmin variation and read-time variation using negative feedback control,” IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 62, no. 6, pp. 1403-1410, June 2015.

[130] Y. Zhu, Y. Ma, X. Li, H. Li, Y. Li, J. Gu, Y. Xie, H. Cao, L. J. Chang, and Y. Xie, "A 64 kByte 8T subthreshold SRAM using in-situ self-body-bias technique in 65 nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 88-89.

[131] E. Morifuji, T. Yoshida, M. Kanda, S. Matsuda, S. Yamada and F. Matsuoka, “Supply and threshold-voltage trends for scaled logic and SRAM MOSFETs,” IEEE Transactions on Electron Devices, vol. 53, no. 6, pp. 1427–1432, June 2006.

[132] F. Khateb and T. Kulej, “Design and implementation of a 0.3-V differential difference amplifier,” IEEE Transactions on Circuits Systems I: Regular Papers, vol. 66, no. 2, pp. 513–523, February 2019.

[133] G. Chen, D. Sylvester, D. Blaauw and T. Mudge, "Yield-driven near-threshold SRAM design," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 11, pp. 1590–1598, November 2010.

[134] "Predictive Technology Model (PTM)," Predictive Technology Model (PTM). [Online]. Available: http://ptm.asu.edu/. [Accessed: 12-Jan-2020].

[135] A. Sachdeva and V. K. Tomar, "Design of 10T SRAM cell with improved read performance and expanded write margin," IET Circuits, Devices and Systems, vol. 15, no. 1, pp. 42-64, January 2021.

[136] G. Pasandi and S. M. Fakhraie, "An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs," IEEE Transactions on Electron Devices, vol. 61, no. 7, pp. 2357–2364, July 2014.

[137] S. Ahmad, B. Iqbal, N. Alam and M. Hasan, "Low leakage fully half-select-free robust SRAM cells with BTI reliability analysis," IEEE Transactions on Device Material Reliability, vol. 18, no. 3, pp. 337–344, March 2018.

[138] A. Sil, S. Ghosh, N. Gogineni and M. Bayoumi, "A novel high write speed, low power, read-SNM-free 6T SRAM cell," in *2008 51st Midwest Symposium on Circuits and Systems*, 10-13 August 2008, pp. 91–94.

[139] M.-F. Chang, J.-J. Wu, K.-T. Chen, Y.-C. Chen, Y.-H. Chen, R. Lee, H.-J. Liao and H. Yamauchi, "A differential data-aware power-supplied (D2AP) 8T SRAM cell with expanded write/read stabilities for lower VDDmin applications," IEEE Journal on Solid-State Circuits, vol. 45, no. 6, pp. 1234–1246, June 2010.

[140] S. Pal, S. Bose, W. H. Ki and A. Islam, "A highly stable reliable SRAM cell design for low power applications," Microelectronics Reliability, vol. 105, 113503, February 2020.

[141] A. Sachdeva and V. K. Tomar, "Design of low power Half Select free 10T static random access memory cell," Journal of Circuits Systems and Computers, vol. 30, no. 4, p. 2150073, 2021.

[142] Y.-W. Chiu, Y.-H. Hu, M.-H. Tu, J.-K. Zhao, Y.-H. Chu, S.-J. Jou and C.-T. Chuang, "40nm bit-interleaving 12T subthreshold SRAM with data-aware write-assist," IEEE Transactions on Circuits Systems I: Regular Papers, vol. 61, no. 9, pp. 2578–2588, September 2014.

[143] Q. Jin, X. Li and J. B. Bernstein, “SRAM stability analysis considering gate oxide SBD, NBTI and HCI,” in *2007 IEEE International Integrated Reliability Workshop Final Report*, 15-18 Oct. 2007, pp. 109–114.

[144] A. Agarwal, B. C. Paul, S. Mukhopadhyay and K. Roy, “Process variation in embedded memories: failure analysis and variation aware architecture,” IEEE Journal of Solid-State Circuits, vol. 40, no. 9, pp. 1804–1813, September 2005.

[145] Y. Wang, S. Cotofana and L. Fang, “A unified aging model of NBTI and HCI degradation towards lifetime reliability management for nanoscale MOSFET circuits,” in *2011 IEEE/ACM International Symposium on Nanoscale Architectures*, 08-09 Jun. 2011, pp. 175–180.

[146] D.E. Holcomb, W.P. Burleson and K. Fu, “Power-Up SRAM state as an identifying fingerprint and source of true random numbers,” IEEE Transactions on Computer, vol. 58, no. 9, September 2009.

[147] P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” IEEE Transactions on Device Material Reliability, vol. 50, no. 3, pp. 583–604, June 2003.

[148] R. Baumann, "Soft errors in advanced computer systems," IEEE Design & Test of Computers, vol. 22, no. 3, pp. 258–266, May-June 2005.

[149] T. Granlund, B. Granbom and N. Olsson, “Soft error rate increase for new generations of SRAMs,” IEEE Transactions on Nuclear Science, vol. 50, no. 6, pp. 2065–2072, June 2003.

[150] S. H. Jahinuzzaman, D. J. Rennie and M. Sachdev, “A soft error tolerant 10T SRAM bit-cell with differential capability,” IEEE Transactions on Nuclear Science, vol. 56, no. 6, pp. 3768–3776, June 2009.

[151] S. M. Jahinuzzaman, M. Sharifkhani and M. Sachdev, “An analytical model for soft error critical charge of nanometric SRAMs,” IEEE Transactions on Very Large Scale Integration (VLSI) System, vol. 17, no. 9, pp. 1187–1191, September 2009.

[152] S. R. Mansore, R. S. Gamad and D. K. Mishra, “A 32 nm read disturb-free 11T SRAM cell with improved write ability,” Journal of Circuits Systems and Computers, vol. 29, no. 5, pp. 2050067, 2020.

[153] K. Shin, W. Choi, and J. Park, “Half-select free and bit-line sharing 9T SRAM for reliable supply voltage scaling,” IEEE Transactions on Circuits Systems I: Regular Papers, vol. 64, no. 8, pp. 2036–2045, August 2017.

[154] D. Nayak, D. P. Acharya, P. K. Rout and U. Nanda, “A high stable 8T-SRAM with bit interleaving capability for minimization of soft error rate,” Microelectronics Journal, vol. 73, pp. 43–52, March 2018.

[155] V. B. Suresh and S. Kundu, “On analysis and mitigating SRAM BER due to random thermal noise,” in *2013 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 05-07 Aug. 2013, pp. 159–164.

[156] T. Suzuki, Y. Yamagami, I. Hatanaka, A. Shibayama, H. Akamatsu and H. Ymauchi, “A sub-0.5-v operating embedded SRAM featuring a multi-bit-error-immune hidden-ecc scheme,” IEEE Journal of Solid-State Circuits, vol. 41, no. 1, pp. 152–160, January 2006.

[157] S. Gupta, K. Gupta and N. Pandey, “Pentavariate Vmin analysis of a subthreshold 10T SRAM bit cell with variation tolerant write and divided bit-line read,” IEEE Transactions on Circuits Systems I: Regular Papers, vol. 65, no. 10, pp. 3326–3336, October 2018.

[158] S. Yang, W. Wolf and N. Vijaykrishnan, “Power and performance analysis of motion estimation based on hardware and software realizations,” IEEE Transactions on Computers, vol. 54, no. 6, pp. 714–716, June 2005.

[159] G. Chen and M. Kandemir, “Optimizing address code generation for array-intensive DSP applications,” in *Proceedings of International Symposium on Code Generation Optimization*, 20-23 Mar. 2005, pp. 141–152.

[160] D. Dutt, P. Mittal, B. Rawat and B. Kumar, “Design and performance analysis of high low power voltage mode sense amplifier for static RAM,” Advances in Electrical and Electronic Engineering, vol. 20, no. 3, pp. 285-293, March 2022.

[161] S.E. Shimanek, E.E. Edwards and T.J. Davies, “Reconfigurable SRAM-ROM cell,” US 7,023,744 B1, April 04, 2006.

[162] S. Sutardja, “System on chip with reconfigurable SRAM,” TW200901225A, January 1, 2009.

[163] S. Kang, Y. Leblebici and C. Kim, “CMOS digital integrated circuits,” 3rd ed. New York; McGraw-Hill, 2015, pp. 204, 422.

[164] B. Kumar, B. K. Kaushik and Y. S. Negi, “Design and analysis of noise margin, write ability and read stability of organic and hybrid 6-T SRAM cell,” Microelectronics Reliability, vol. 54, no. 12, pp. 2801-2812, December 2014.

[165] B. Rawat, K. Gupta and N. Goel, “Low voltage 7T SRAM bit cell in 32 nm CMOS technology node,” in *2018 International Conference of Computing, Power and Communications technologies (GUCON),* 28-29 Sept. 2018.

[166] S. Lin, Y.B. Kim and F. Lombardi, “Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability,” Integration, vol. 43, no. 2, pp. 176–187, April 2010.

[167] M. Moghaddam, M.H. Moaiyeri and M. Eshghi, “Ultra low-power 7T SRAM cell design based on CMOS,” in *2015 23rd Iranian Conference on Electrical Engineering*, 10-14 May 2015.

[168] T. Na, S. H. Woo, J. Kim, H. Jeong and S. O. Jung, “Comparative study of various latch-type sense amplifiers,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 2, pp. 425-429, February 2014.

[169] S. Nalam and B. H. Calhoun, “5T SRAM with asymmetric sizing for improved read stability,” IEEE Journal on Solid-State Circuits, vol. 46, no. 10, pp. 2431–2442, October 2011.

[170] N.-C. Lien, L. W. Chu, C. H. Chen, H. I. Yang, M. S. Tu, P. S. Kan, Y. J. Hu, C. T. Chuang, S. J. Jou and W. Jwang, “A 40 nm 512 kb cross-point 8 T pipeline SRAM with binary word-line boosting control, ripple bit-line and adaptive data-aware write-assist,” IEEE Transactions on Circuits Systems I: Regular Papers, vol. 61, no. 12, pp. 3416–3425, December 2014.

[171] S. S. Ensan, M. H. Moaiyeri, M. Moghaddam and S. Hessabi, “A low-power single-ended SRAM in FinFET technology,” AEU – International Journal of Electronics and Communications, vol. 99, no. 2, pp. 361-368, February 2019.

[172] K. O. Jeppson, S. Christensson and N. Hedenstierna, “Formal definitions of edge-based geometric design rules,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 12, no. 1, pp. 59-69, January 1993.

[173] J. Zhai, C. Yan, S. G. Wang, D. Zhou, H. Zhou and X. Zeng, “An efficient non-gaussian sampling method for high sigma SRAM yield analysis,” ACM Transactions on Design Automation of Electronic Systems, vol. 23, no. 3, pp. 1-23, March 2018.

[174] D. Kim, V. Chandra, R. Aitken, D. Blaauw and D. Sylvester, “Variation-aware static and dynamic writability analysis for voltage-scaled bit-interleaved 8-T SRAMs,” in *IEEE/ACM International Symposium on Low Power Electronics and Design*, 01-03 Aug. 2011, pp. 145–150.

[175] D. Patel, A. Neale, D. Wright and M. Sachdev, “Body biased sense amplifier with auto-offset mitigation for low voltage SRAMs,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3265-3278, August 2021.

[176] M. L. Fan, V. P. H. Hu, Y. N. Chen, P. Su and C. T. Chuang, “Variability analysis of sense amplifier for FinFET subthreshold SRAM applications,” IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 59, no. 12, pp. 878-882, December 2012.

[177] O. Y. Wong, H. Wong, W. S. Tam and C. W. Kok, “Parasitic capacitance effect on the performance of two-phase switched-capacitor DC-DC converters,” IET Power Electronics, vol. 8, no. 7, pp. 1195-1208, July 2015.

[178] B. Ebrahimi, M. Rostami, A. A. Kusha and M. Pedram, “Statistical design optimization of FinFET SRAM using back-gate voltage,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 10, pp. 1911–1916, October 2011.

[179] M. Darwich, A. Abdelgawadf and M. Bayoumi, “A survey on the power and robustness of FinFET SRAM,” in *IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 16-19 Oct. 2016, pp. 1–4.

[180] M. Imani, M. Jafari, B. Ebrahimi and T. S. Rosing, “Ultra-low power finFET based SRAM cell employing sharing current concept,” Microelectronics Reliability, vol. 10, 2015.

[181] A. Shafaei and M. Pedram, “Energy-efficient cache memories using a dual-Vt 4t SRAM cell with read-assist techniques,” in *IEEE 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 14-15 Mar. 2016, pp. 457–462.

[182] S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, “Low leakage single bitline 9T (SB9T) static random access memory,” Microelectronics Journal, vol. 62, pp. 1-11, April 2017.

[183] S. Gupta, A. Raychowdhury and K. Roy, “Digital computation in subthreshold region for ultralow-power operation: A device–circuit–architecture codesign perspective,” Proceedings of the IEEE, vol. 98, no. 2, pp. 160–190, February 2010.

[184] A. Haran, E. Keren, D. David, N. Reaeli, R. Giterman, M. Assaf, L. Atias, A. Teman and A. Fish, “Single-event upset tolerance study of a low-voltage 13T radiation hardened SRAM bit cell,” IEEE Transactions on Nuclear Science, vol. 67, no. 8, pp. 1803-1812, August 2020.

[185] S. Gupta, K. Gupta, B. H. Calhoun and N. Pandey, “Low-power near-threshold, 10T SRAM bit cell with enhancement data independent read port leakage for array augmentation in 32-nm CMOS,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 978-989, March 2019.

[186] M. Cho, J. Schlessman, W. Wolf and S. Mukhopadhyay, “Reconfigurable SRAM architecture with spatial voltage scaling for low power mobile multimedia applications,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 1, pp. 161-165, January 2011.

LIST OF PUBLICATIONS

Patent Published and FER Submitted

1. Bhawna Rawat and Poornima Mittal, Indian Patent Application No. 202011056665 A dated Jan 28, 2022; Entitled: 'RECONFIGURABLE STATIC RANDOM ACCESS MEMORY (SRAM) AND METHOD THEREOF'.
   Published on: 28 – 01 – 2022
   FER response submitted on: 22 – 12 – 2022.

SCI/SCIE Indexed Journal Papers Published/Accepted

1. Bhawna Rawat and Poornima Mittal, "Single bit line accessed high performance ultra-low voltage operating 7T SRAM bit cell with improved read stability," International Journal of Circuit Theory and Application, vol. 49 no. 5, pp. 1435-1449, 2021. (**I.F. – 2.378, Wiley**).
2. Bhawna Rawat and Poornima Mittal, "A 32 nm single ended single port 7T SRAM for low power utilization," Semiconductor Science and Technology, vol. 36, no. 9, pp. 095006-095022, 2021. (**I.F. - 2.352, IOP Publishing**).
3. Bhawna Rawat Poornima Mittal, "A Reliable and Temperature Variation Tolerant 7T SRAM Cell with Single Bitline Configuration for Low Voltage Application," Circuits, Systems and Signal Processing, vol. 41, pp. 2779-2801, 2022. (**I.F. – 2.72, Springer**).
4. Bhawna Rawat and Poornima Mittal, "A low power single bit-line configuration dependent 7T RAM bit cell with process variation tolerant enhanced read performance" Analog Integrated Circuits and Signal Processing, vol. 115, pp. 77-92, 2023. (**I.F. 1.4, Springer**).
5. Bhawna Rawat and Poornima Mittal, "A comprehensive analysis of different 7T SRAM topologies to design a 1R1W bit interleaving enabled and half select free cell for 32 nm technology node," Proceedings of the Royal Society A: Mathematical, Physical, and Engineering Sciences, vol. 478, no. 2259, pp. 20210745-20210771, 2022. (**I.F. – 3.213, Proceedings of Royal Society**).

6. Bhawna Rawat and Poornima Mittal, "A switching NMOS based single ended sense amplifier for high density SRAM Application," ACM Transaction on Design Automation of Electronic Systems, vol. 28, no. 3, pp. 1-14, 2023. **(I.F. 1.447, ACM**).
7. Bhawna Rawat and Poornima Mittal, "A Latch Based Sense Amplifier with Improved performance for single ended SRAM applications" Physica Scripta, vol. 98, no. 6, pp. 065025, 2023 (**I.F. – 2.9, IOP Publishing**).
8. Bhawna Rawat and Poornima Mittal, "A single-port to dual-port reconfigurable 7T SRAM bit cell for high speed, power saving and low voltage application" ACM Transaction on Design Automation of Electronic Systems, vol. 28, no. 6, pp. 1-14, 2023 (**I.F. 1.447, ACM**).

Papers Submitted in SCI/SCIE Indexed Journals

1. Bhawna Rawat and Poornima Mittal, "A Hybrid SRAM Array Architecture using Single Port and Dual Port 7T SRAM cells for Low Power Applications" Circuits, Systems and Signal Processing (**I.F. – 2.3, Springer**).

Paper Under-Process for Future Submission in SCI/SCIE International Journal

1. Bhawna Rawat, and Poornima Mittal, "A comprehensive review of static random access memory bit cells, and array topologies for cache implementation" *Circuits, Systems and Signal Processing* (**I.F. – 2.3, Springer**)
2. Bhawna Rawat, and Poornima Mittal, "A comprehensive review of sense amplifier topologies for cache implementation" *Microprocessor and Microsystems* (**I.F. – 2.6, Springer**)

Scopus Indexed International Conference Papers

1. Bhawna Rawat and Poornima Mittal, "A Comprehensive review to Investigate the Effect of Read Port Topology on the Performance of Different 7T SRAM cells at 32 nm Technology Node," *2nd International Conference on Women Researchers in Electronics and Computing (WREC-2023),* 21-23 April, 2023.
2. Bhawna Rawat and Poornima Mittal, "Impact of high performance transistor on performance of static random access memory for low voltage applications," *2nd International Conference on Computational Electronics for Wireless Communication (ICCWC-2022),* 09-10 June, 2022.

3. Bhawna Rawat and Poornima Mittal, "Investigating the Impact of Schmitt Trigger on SRAM cells at 32 nm Technology node for low voltage applications," *Advances in VLSI and embedded systems (AVES-2021),* 18-19 December, 2021.

4. Bhawna Rawat and Poornima Mittal, "Analysis of varied architectural configuration for 7T SRAM bit cell," *4th International Conference on Recent Trend in Communication & Electronics (ICCE-2020),* 28-29 November 2020.