MACHINE LEARNING BASED ANALOG CIRCUIT DESIGN AUTOMATION

A PROJECT REPORT

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IN
VLSI DESIGN AND EMBEDDED SYSTEM DESIGN

Submitted By

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I Vipin Kumar Sharma, 2K22/VLS/23 student of MTech (VLSI Design And Embedded System Design), hereby declare that the project Dissertation titled "MACHINE LEARNING BASED ANALOG CIRCUIT DESIGN AUTOMATION" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology , is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any degree, Diploma Associateship, Fellowship or other similar title or recognition.

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I hereby certify that the project Dissertation titled "Machine Learning Based Analog Circuit Design Automation" which is submitted by Vipin Kumar Sharma, 2k22/VLS/23 Department of Electronic and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This study proposes a machine learning-based approach for the automated design of a common-source (CS) amplifier with a diode-connected load [19]. The objective is to optimise the circuit's performance characteristics, such as gain and power consumption while considering the constraints imposed by the diode-connected load utilitsing the NN model.

A dataset comprising various input parameters and corresponding circuit performance metrics is collected from a set of simulated CS amplifiers with diode-connected loads to achieve this. Deep learning algorithms, specifically Multi-layer perceptron models, are then trained on this dataset to establish the relationships between the input parameters and the desired performance metrics.

The trained models are subsequently utilised for automated circuit design. Given the desired specifications and constraints, the machine learning algorithm predicts the optimal values for the circuit parameters, including transistor dimensions, biasing, and load characteristics. This approach reduces the design iteration time and the reliance on manual tuning, enabling faster and more efficient circuit design.

The effectiveness of the proposed method is evaluated through extensive simulations and comparisons with different number of datasets in order to compare performance of estimation with respect to dataset. The results demonstrate that the machine learning-based automated design approach achieves improved RMSE and MSE of aspect ratio estimation Moreover, the automated design process exhibits robustness and scalability across different design specifications.

In conclusion, this research introduces a novel approach to automate the design process of CS amplifiers with diode-connected loads using machine learning techniques. The proposed method offers significant advantages in terms of efficiency, performance, and adaptability. It holds great potential for accelerating the development of analog circuits and fostering advancements in the field of circuit design.

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CHAPTER 1

INTRODUCTION

Traditionally, designing analog integrated circuits is a lengthy process due to the complex, non-linear between both circuit specs and design parameter Additionally, modelling estimation errors and challenging circuit analysis, influenced by numerous trade-offs, further extend the design duration [1]. Unlike digital circuits, which operate in discrete time, analog circuits function in continuous-time. This fundamental difference makes analog circuit design and synthesis more intricate compared to their digital counterparts. Moreover, various additional factors must be considered when designing analog circuits.

As a result, the analog design focuses on a broader set of parameters, including speed, power, gain bandwidth, and others. The design process is often complex, involving extensive calculations. The complexity increases with the number of transistors. Recently, machine learning has seen widespread adoption in various technological fields. In analog circuits, machine learning techniques are being used to develop models that accurately simulate circuit behaviours [4]. The flexibility and benefits of different machine learning algorithms have been crucial in solving problems related to pattern recognition, prediction, and classification [5], [6]. There is an increasing trend of using machine learning algorithms for modelling both analog and digital circuits, including tasks like evaluating transistor sizes [7]–[9].

To illustrate this application, a model of a common-source amplifier with a diode-connected load structure was created. Different machine learning algorithms were used to determine the transistor sizes within the circuit. The model was trained and simulated using Python to ascertain the dimensions of the transistors in the circuit. The few number of dataset for the 180nm technology used in this study was generated through LTSpice simulations and for the experiment purpose larger data set has been modelled using mathematical model equation and has been created using Python.

The main motivation behind this project is to understand the effective way of designing the circuit, considering all the design constraints, and also utilizing ML applications in an effective manner. The best approach to modelling the problem emerges when both expertise in analog design and ML are employed.

1.1 MOTIVATION

The motivation behind ML-based analog designing stems from the desire to enhance and streamline the process of analog circuit design. Traditional analog circuit design often requires extensive manual iterations and expertise, making it time-consuming and challenging to achieve optimal circuit performance. By incorporating machine learning (ML) techniques into the design process, several benefits and motivations arise:

1. Efficiency: ML-based analog designing aims to automate and expedite various aspects of the design process. By leveraging ML algorithms, tasks such as parameter optimization, circuit sizing, and performance prediction can be automated, saving time and effort for designers.

2. Optimization: ML techniques can explore vast design spaces and identify optimal circuit configurations by efficiently searching through numerous design possibilities. This allows for better performance and improved efficiency compared to manual design iterations.

3. Design Exploration: ML-based analog designing can facilitate exploration of unconventional or complex circuit topologies that may not be readily apparent through traditional design approaches. It enables designers to explore and discover innovative solutions beyond their conventional knowledge and expertise.

4. Robustness and Adaptability: ML models can learn from a wide range of design data and capture patterns and relationships that may not be explicitly known or considered by human designers. This leads to the development of more robust and adaptable analog circuits that can perform well under various operating conditions.

5. Knowledge Discovery: ML algorithms can provide insights and analysis of the

design space, allowing designers to gain a deeper understanding of the relationships between circuit parameters, performance metrics, and constraints. This knowledge can be leveraged to enhance future design processes and drive further innovation.

Overall, the motivation behind ML-based analog designing is to leverage the power of machine learning to optimize and automate the design process, explore novel design possibilities, improve circuit performance, and facilitate the development of more efficient and robust analog circuits.

CHAPTER 2

LITERATURE REVIEW

Figure 2.1 illustrates the commonly used design flow [10] that most analog designers follow. This approach integrates both top-down and bottom-up methodologies. The top-down design begins with system-level considerations and progresses to optimizations at the device level, while the bottom-up process involves layout synthesis and verification. Initially, designers select a topology that satisfies system specifications at the circuit level. Next, they adjust the sizes of the devices at the component level. This combination of topology selection and device sizing forms the pre-layout design phase.

After carefully crafting the schematic, designers move on to developing the circuit layout. The next steps is post-layout simulation which involve extracting parasitic elements from the layout and performing simulations that incorporate these parasitic effects. Designers must adjust parameters and repeat the process. This iterative cycle may need to be repeated multiple times before the layout is finalized [11].

Despite significant advancements in analog design automation, especially in recent decades, automated tools have not fully replaced manual efforts within the design flow [12]. Recently, researchers have been investigating the use of machine learning techniques to tackle various challenges in analog design. These efforts include tasks such as choosing the circuit configuration and determining the dimensions of the components, and analog layout in the physical domain

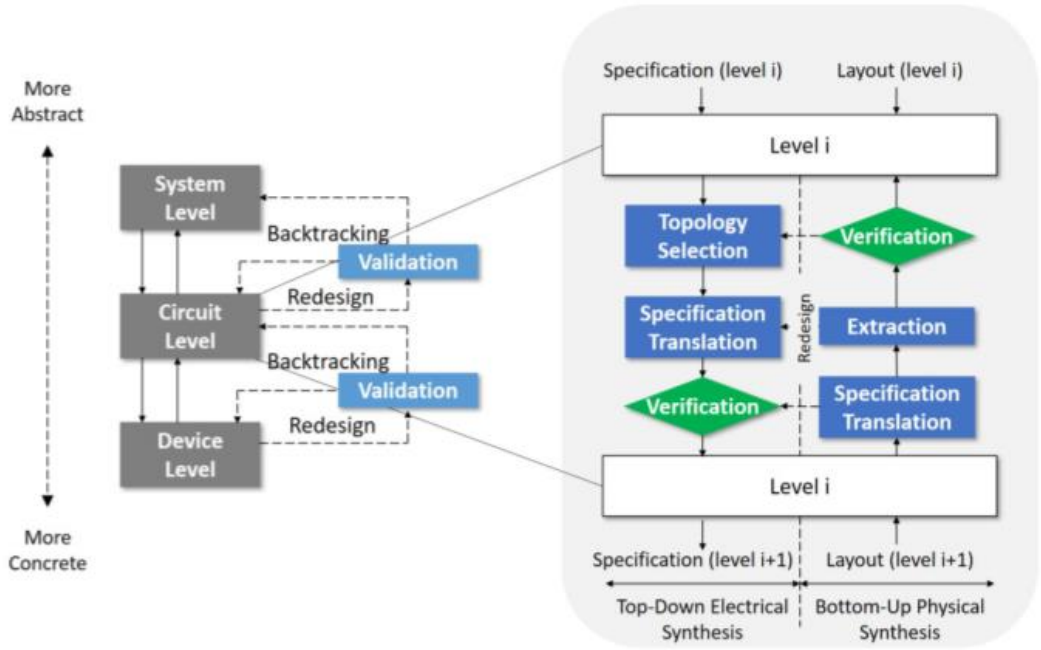

Fig.2.1 The design flow for analog circuits typically involves multiple hierarchical levels. [13]

2.1 Machine Learning for Circuit Topology Design Automation

The initial phase of designing an analog circuit usually starts with topology selection, followed by determining the sizes and parameters of the devices. This process can be quite time-consuming, and choosing an inappropriate topology may necessitate restarting the design process from scratch. Traditionally, the design of topology relies heavily on the expertise and experience of skilled designers. With the increasing demand and complexity of analog circuits, there is a pressing need for Computer-Aided Design (CAD) tools. However, automation tools for topology design are still relatively underdeveloped due to the high degree of freedom in design choices. To tackle this issue, researchers have been investigating the application of Machine Learning (ML) techniques to speed up the design process.

Some researchers focus on addressing the topology selection problem, aiming to identify the most appropriate topology from a range of available options. For instance, [16] concentrates on recognizing well-known building blocks in circuit topologies.

2.1.2 Topology Selection

When designers do not need to create designs from scratch, such as for standard circuit components like amplifiers, they can select from a predefined set of alternatives. This approach is simpler than designing from the ground up. In 1996, [15] and [16] developed tool called FASY for topology selection. This tool utilizes to map specifications (e.g., DC gain) to possible alternatives and employs backpropagation for optimizer training. More recent studies [14] have explored the use of Convolutional Neural Networks (CNN) as classifiers, where the CNN is trained with circuit specifications as inputs and topology indices as labels. However, a significant drawback of these topology selection methods is the time-consuming nature of data collection and training. As a result, topology selection is most effective in scenarios requiring repetitive designs, as the trained model can be reused efficiently.

2.1.3 Topology Generation:

While the previous studies concentrate on topology selection, a recent study [17] represents a pioneering effort in directly generating circuit topology based on given specifications. This study, which is limited to two-port circuits, employs an RNN and hypernetworks to tackle the topology generation problem. The reported performance

exceeds that of traditional methods when the inductor circuit length n is greater than or equal to 4.

2.2 Machine Learning for Device Sizing Automation

Machine learning techniques can play a crucial role in analog circuit sizing by automating and optimizing the process of determining the optimal component values for a given circuit design. Here's how machine learning can be applied in analog circuit sizing:

1. Dataset Creation: A dataset needs to be created that includes a range of circuit designs with their corresponding component values and performance metrics. This dataset can be generated through simulations, measurements, or a combination of both. The dataset should cover various circuit topologies and performance objectives.
2. Feature Extraction: Relevant features need to be extracted from the circuit designs to represent their characteristics. These features can include circuit parameters, device characteristics, design specifications, and performance metrics. The choice of features depends on the specific sizing problem and the available data.
3. Training Data Preparation: The dataset needs to be divided into training and validation sets. The training set is used to train the machine learning model, while the validation set is used to assess its performance.
4. Model Training: A machine learning algorithm, such as regression or neural networks, is trained using the training dataset. The algorithm learns the relationships between the input features (circuit parameters) and the target output (optimal component values). The training process involves optimizing the model parameters to minimize the prediction error.
5. Model Validation and Evaluation: The trained model is evaluated using the validation dataset to assess its performance. Metrics such as mean squared error (MSE) or mean absolute error (MAE) can be used to measure the accuracy of the predicted component values compared to the actual optimal values.
6. Sizing Predictions: Once the machine learning model is trained and validated, it can be used to predict the optimal component values for new circuit designs. Given a set of design specifications and performance requirements, the model takes the input features (circuit parameters) and generates predictions for the component values that maximize the desired performance objectives.

7. Model Refinement and Optimization: The performance of the machine learning model can be further improved by refining the model architecture, optimizing hyperparameters, or using more sophisticated algorithms. Iterative refinement based on feedback from designers and additional training data can enhance the model's accuracy and generalization capabilities.

2.3 Machine Learning for Analog Layout

Designing analog layouts is very difficult since parasitic elements have an immense effect on circuit performance. The intricate relationship between layout and performance, together with the mismatch between pre- and post-layout simulations, complicates the design process. Historically, designers have estimated parasitic effects based primarily on their experience, which can result in long design times and perhaps inaccurate results. As a result, research has been focusing more on automating analog layout, and machine learning algorithms have recently made significant progress in this area.

The studies discussed below are summarized in Table 2.3.1.

Generative Adversarial Networks (GANs) are used in a study to help in layout generation by imitating and learning from manual layouts the designer's activities. According to experimental findings, generated layouts, particularly for op-amp circuits, achieve post-layout circuit performance that is comparable to manual designs. Another method is to divide circuit hierarchies by training a Graph Convolutional Network (GCN). This network achieves 100% accuracy in 275 test cases with post-processing, processing circuit netlists as input and producing the circuit hierarchy as an output.

A Graph Neural Network (GNN) is being introduced in another research project to evaluate the electromagnetic (EM) properties of distributed circuits. Then, using this model in reverse, circuits with desired electromagnetic properties are designed. They also suggest an automated routing framework that uses the variational autoencoder (VAE) algorithm as its foundation. Additionally, they create a knowledge-based strategy in which the optimal match is found by comparing certain circuits with pre-existing designs. When new circuits are built, the legacy database keeps growing.

Furthermore, a different study presents a closed-loop design framework for investigating circuit layout using a multi-objective Bayesian optimization technique. The design process uses the simulation findings as input in this framework.

Some studies focus on parasite prediction prior to layout in an effort to reduce the difference between pre- and post-layout simulations. Using the circuit schematic, one

method uses a Graph Neural Network (GNN) to predict net parasitic capacitance and device characteristics. This method uses a random forest to predict net parasitic resistance and capacitance after net features are determined. Experiments show that the difference between pre- and post-layout circuit simulations is reduced from an average of 37% to 8% by projected parasitics.

Many academics are concentrating on forecasting layout performance using machine learning techniques because post-layout simulations using SPICE-like simulators need a lot of effort. Three classic machine learning algorithms—support vector machine (SVM), random forest, and neural network—are compared for prediction accuracy. An automated layout framework is then developed by combining these performance prediction techniques with simulated annealing.

A 3D Convolutional Neural Network (CNN) for circuit inputs is presented by another research endeavor. To create 3D inputs, circuits are first converted into 2D images, and then a third coordinate channel is added. In conclusion, they suggest a customized Graph Neural Network (GNN) for performance prediction, which exhibits more accuracy than the CNN-based method.\

Table 2.3.1 Summary of ML for analog layout[18]

Stage	Task	ML Algorithm
Pre-Layout Preparation	Circuit hierarchy generation	GCN
	Parasitic estimation	GNN
		Random forest
Layout Generation	Well Gneration	GAN
	Closed loop layout synthesis	Bayesian Optimisation
	Routing	VAE
Post layer evaluation	Electromagnetic properties estimation	GNN
	Performance prediction	SVM, random forest, NN
		CNN
		GNN

CHAPTER 3

PROPOSED METHODOLOGY: DESIGN CMOS CS AMPLIFIER WITH DIODE-CONNECTED LOAD USING NEURAL NETWORK

Below proposed MOS technology used to design CS amplifier using ML model is accurate and substitute traditional analog circuit design which often requires extensive manual iterations and expertise, making it time-consuming and challenging to achieve optimal circuit performance. One popular amplifier configuration which is taken for this experiment is common-source amplifier. The most straightforward variant use a resistive load, but because on-chip resistor production can be challenging, practical implementations frequently use an active load MOS transistor. The MOSFET that has both its gate and drain shorted is known as "Diode-Connected" because, as Figure 3.1 illustrates, it operates similarly to its bipolar cousin, constantly staying in the saturation area.

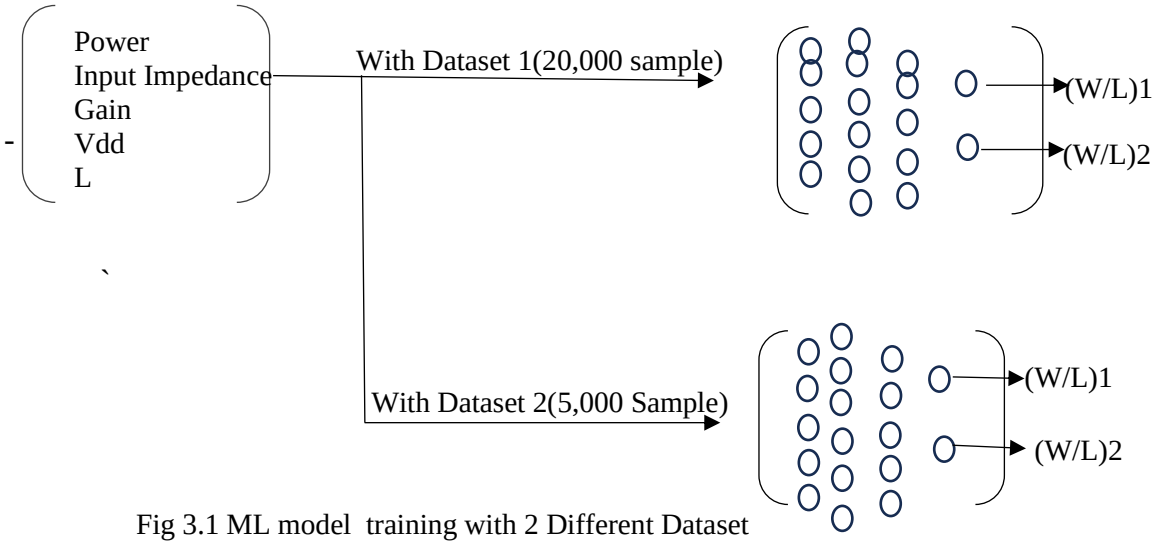

Fig 3.1 ML model training with 2 Different Dataset

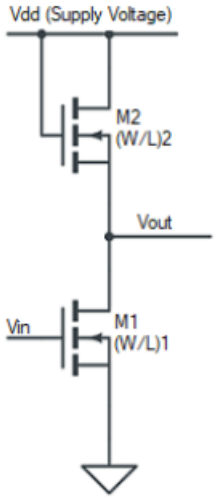

Fig 3.2 CS Amp.

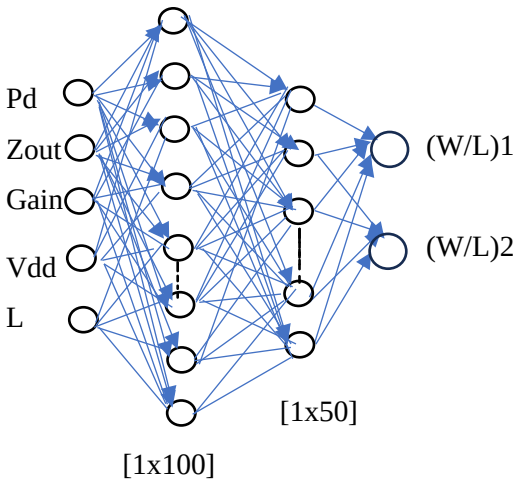

Fig 3.3 NN Model

An NMOS transistor (M1) serves as the driver and a diode-connected NMOS transistor (M2) serves as the load in the simulated amplifier. The static equations of MOS devices serve as the foundation for computations and simulations. The following approach can be used to compute the transistor aspect ratio when designing a circuit based on power budget.

$$P_d = V_{dd} * I_d \tag{3.1}$$

$$Av = \sqrt{\left(\frac{W}{L}\right)_1 \Big/ \left(\frac{W}{L}\right)_2} \tag{3.2}$$

$$\left(\frac{W}{L}\right)_1 = \frac{2\left(\frac{Pd}{Vdd}\right)}{un * Cox * \left(\frac{Vdd - Vswing}{2}\right)^2} \tag{3.3}$$

$$\left(\frac{W}{L}\right)_2 = \frac{\left(\frac{W}{L}\right)_1}{Av^2} \tag{3.4}$$

$$V_{bias} = V_{th} + \left(\frac{V_{dd} - V_{swing}}{2}\right) \tag{3.5}$$

Drain Current (Id) is computed using Equation (3.1) based on the supplied voltage and power budget specifications. The power dissipation specification, Vswing, and constants for the specified technology node are taken into account while calculating the aspect ratio of Mosfet1.Equation (3.4) can be used to determine Mosfet2's aspect ratio. Furthermore, bias voltage is a crucial characteristic that determines the operating point of a diode-connected load in the correct construction of an amplifier. Consequently, we have assumed an equal overdrive distribution for a given voltage swing in order to determine Vbias, which may be done using equation (3.5).

3.1 Neural Network Model

The above-mentioned neural model graph Fig3.2 has one input layer and 2 hidden layer with hidden neuran as 100 and 50. The hidden layers facilitate the transformation of input data to the desired output [11]. To achieve the desired output, the network's coefficients (weights) are optimized using a training algorithm.

- The ML model has been trained for 2 Dataset i.e Dataset 1 (20,000 samples) and Dataset 2 (5,000 samples) for comparing the performance of machine learning based analog circuit design as shown in Fig
- Two hidden layers, an output layer consist of (W/L)1 and (W/L)2 , and an input layer(consist of Power, Vdd, L, Gain) compose the MLP structure. Five dimensions make up the input, while three make up the output. 100 and 50, respectively, are the dimensions of the buried layers. Naturally, more neurons in the buried layer lead to more complexity, but they also cause improvisation error. To prevent lesser length data sets from being overfit, a large amount of neurons should be used.
- To calculate transistor sizes, a Multilayer Perceptron (MLP) using a backpropagation technique is employed. Often called layered networks, multilayer perceptrons are capable of implementing intricate input-output mappings. The backpropagation technique is the most widely used learning algorithm for multilayer perceptrons (MLPs). It involves methodically adjusting weights to provide the desired output with the least amount of error.
- An input layer, one or more hidden layers, and an output layer are the minimum number of layers of neurons in an MLP model. The neural network's ability to apply precise data transformations to produce the intended output depends on the hidden layers, which are essential. In order to train the network, the outputs are compared to the desired outputs, and the error is calculated. This information is then sent back through the network to modify the weights. Until the intended result is obtained, this process is repeated.
- Relu and Adam is used as activation and solver for their better accuracy and performance.

CHAPTER 4

EXPERIMENTS, RESULTS AND ANALYSIS

4.1 Dataset Description

In the first stage, multiple transistor sizes were used to simulate the common-source amplifier in DC settings and satisfy diverse needs, including voltage gain, power budget, power supply, and voltage swing for a particular technological node. Several datasets were created for this study's experimental needs using 180 nm technology. In the first experiment, the aspect size of the amplifier was predicted using 20,000 samples that had more neurons. In order to evaluate the machine learning model's performance measures, 5000 samples with fewer hidden neurons were selected for the second dataset.

4.2 Train-Test Split of Data

To train the model, 80% of the samples were used, while the remaining 20% were used to test the model. For experimental purposes, a large dataset was generated to assess accuracy. The effectiveness of the machine learning-based design of analog circuits is highly dependent on the quality and quantity of the dataset. To effectively observe, two different-sized datasets have been created and split into training and test sets based on the specified percentage.

```
from sklearn.model_selection import train_test_split

X_train, X_test, y_train, y_test = train_test_split(X, y,
test_size=0.2, random_state=42)

from sklearn.preprocessing import StandardScaler
scaler = StandardScaler() #scale the set with mean and standard
deviation
X_train = scaler.fit_transform(X_train)
X_test = scaler.transform(X_test)
```

Fig4.1 Train Test split of data set

```
#TRAINING THE MODEL
from sklearn.neural_network import MLPRegressor
from sklearn.metrics import mean_squared_error
mlp = MLPRegressor(hidden_layer_sizes=( 100, 50),
activation='relu', solver='adam', random_state=42)#random state
give same initialization
 description for hidden layer here 2 hidden layer each of 100
 & 50 neuron, fewer data set should have less hidden layer to
 avoid overfitting
 mlp.fit(X_train,y_train)
```

Fig 4.2 Training the Model using MLPRegressor

4.3 Ablation Study:

An experiment was conducted using sample sizes of dataset 1 as 20,000 and dataset 2 as 5,000 to assess the performance metrics' dependency on the ML model. The experiment found that larger sample sizes and more hidden neurons result in better performance with lower RMSE. It was concluded that RMSE should be close to 0 for optimal performance.

Case1: Actual vs Predicted value of aspect ratio(W/L) for Dataset 1 size: 20,000

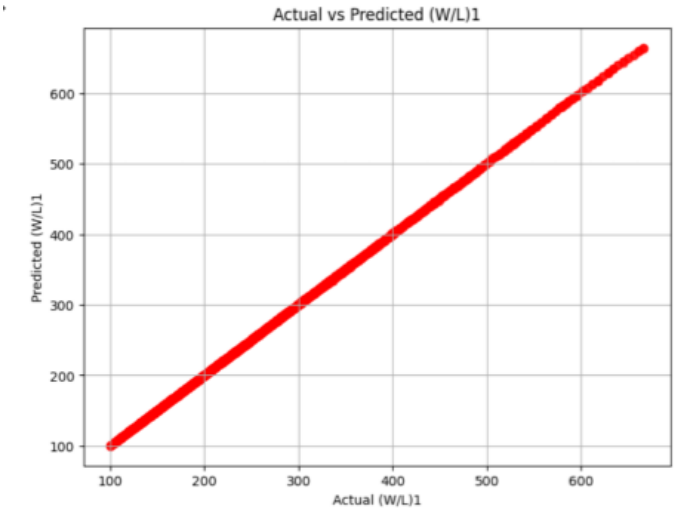

Fig 4.3 Actual vs predicted value of $(W/L)_1$

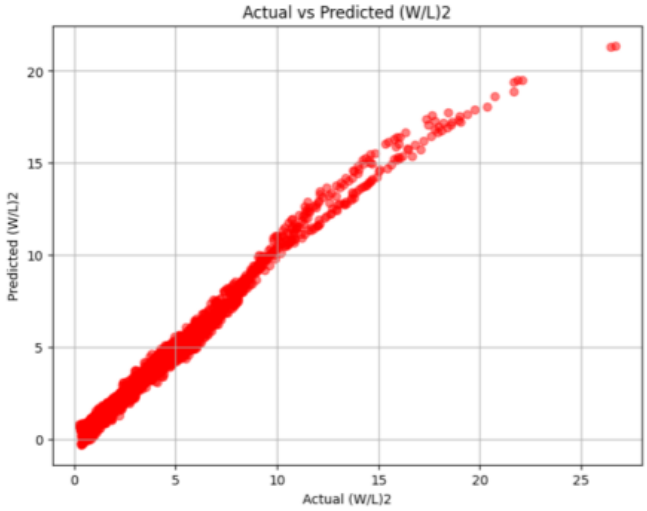

Fig 4.4 Actual vs predicted value of $(W/L)_2$

- As observed from Fig 4.4 the expected Aspect Ratio(W/L) for dataset 1 is same as with predicted (W/L), with an RMSE:0.399.

CASE2: Actual vs Predicted value of aspect ratio for Data set 2 size: 5,000

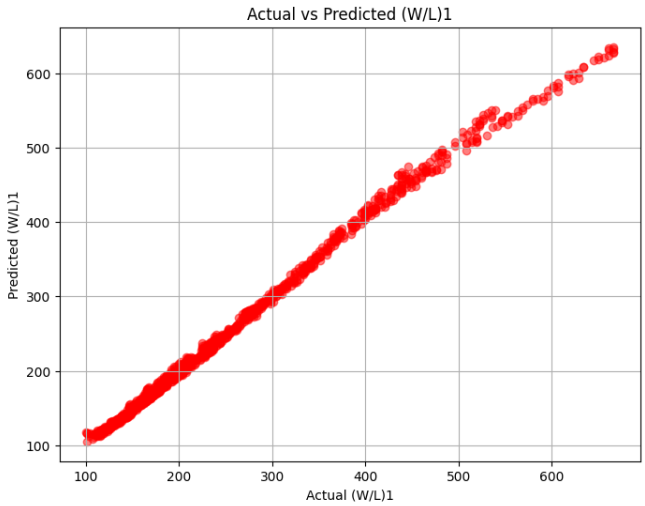

Fig 4.5 Actual vs predicted value of $(W/L)_1$

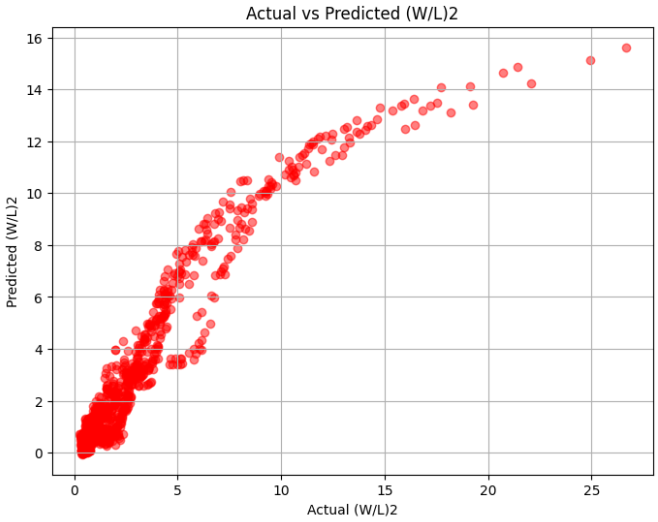

Fig 4.6 Actual vs predicted value of (W/L)2

- As observed from Figure 4.6, the expected aspect ratio (W/L) for dataset 2 is not as accurately predicted, with an RMSE of 4.92.

4.6 Comparison of Ablation Study:

Table 2: comparing regression on two different data set

RMSE for DataSet 1	RMSE for Dataset 2
MSE_TRAIN: 24.263597143463087 MSE_TEST: 22.718041457874264 RMSE: 4.925809288174187 RMSE: 4.766344664192284	MSE_TRAIN: 0.1593563628119399 MSE_TEST: 0.15609362174421054 RMSE: 0.39919464276457906 RMSE: 0.3950868534186003

CHAPTER 5
CONCLUSION AND FUTURE WORK

Conclusion

- In conclusion, the application of machine learning techniques in Electronic Design Automation (EDA) presents significant potential which can streamline the design process by eliminating the need for complex calculations, allowing for quicker circuit design. Neural Networks (NN) are particularly favoured for their accuracy and lower Root Mean Square Error (RMSE) and Mean Squared Error (MSE) metrics.
- Using the Propel ML algorithm and a substantial dataset, along with a sufficient number of neurons, can generate a more accurate ML model for predicting designs

Future Work:

- Generation of good data set for ML learning
- Looking ahead, the evolution of ML-powered EDA tools calls for the strategic combination of traditional approaches with machine learning, necessitating the creation of new models and algorithms to broaden the applicability of ML in real-world scenarios.
- A critical consideration for the widespread acceptance of ML in EDA is the establishment of trust in the predictions and outputs of machine learning models.
- Addressing concerns related to reliability, fairness, and safety is essential for fostering trust among circuit designers and EDA tool users.
- Ongoing research efforts are expected to focus on enhancing the trustworthiness of ML-driven automatic tools, ensuring they meet the standards of reliability and fairness demanded by the industry.

Overall, the trajectory of ML in EDA remains dynamic, with ongoing advancements poised to contribute to the development of more resilient and dependable ML-powered EDA tools.

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