CNTFET BASED DESIGN OF TERNARY ADDERS BASED ON GDI TECHNIQUE

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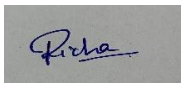

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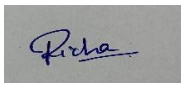
CANDIDATE'S DECLARATION

I, Richa Dubey, Roll No. 2K22/VLS/11, student of M. Tech (VLSI Design & Embedded System), hereby declare that the Project Dissertation titled **"CNTFET-based design of Ternary Adders based on GDI Technique"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.



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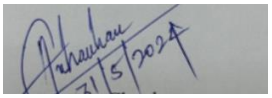
CERTIFICATE

I hereby certify that the Project Dissertation titled **"CNTFET-based design of Ternary Adders based on GDI technique"** which is submitted by Richa Dubey, Roll No. 2K22/VLS/11 Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.



Place: Delhi
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ABSTRACT

This study illustrates the design of ternary logic gates, half adders (HA) using CNTFETs, and the Gate Diffusion Input Technique (GDI). The scaling down of devices is increasing which leads to various issues in the device. We know, the dimension of devices has been decreased by two in every two years (According to Moore's) and this scaling down of devices facing several drawbacks. Nonetheless, as the ITRS 2009 edition points out, as device dimensions have decreased to the approximately 22-nm region, scaling down is encountering constraints pertaining to device performances and manufacturing technologies. This scaling down is causing problems for the devices, like passive power dissipation, changes in device structure and doping, including electron tunneling via thin insulator layers and narrow channels, as well as associated leakage currents. By changing the channel materials in most structures and substituting carbon nanotubes or arrays of carbon nanotubes, we can get around these restrictions. So, in the designing of the gates we will use CNTFET model instead of MOSFET. We all have learnt about binary logic but in our designing, we will use ternary logic as it is three valued and has more advantages over binary logic in the design of digital system. Now we can transmit more data with minimal interconnections results in less memory requirements. Because of the less estimation interconnection cost it receives more attention than others. To implement the design, we can use HSPICE or Cadence by taking model file compatible with these tools. On the Stanford University CNFET Model, the CNTFET model file is accessible. Semiconducting single-walled carbon nanotubes function as the channels in this tiny, SPICE-compatible model that represents unipolar MOSFETs working in enhancement mode... Thus, we employed this model in our project. When compared to traditional binary logic design gate techniques, this ternary logic with CNTFET design technique offers superior speed and power consumption. As a result, the power delay product is reduced. It has been noted that, in comparison to the current design, the suggested HA design's delay has been significantly reduced. In this study, the design has been covered in further detail. The device used for this simulation is cadence virtuoso.

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LIST OF ABBRIVIATIONS

S.NO.	Abbreviations	Full Name
1.	CMOS	Complementary Metal Oxide Semiconductor
2.	CNTFET	Carbon Nano Tube Field Effect Transistor
3.	MVL	Multi Valued Logic
4.	GDI	Gate Diffusion Input
5.	STI	Standard Ternary Inverter
6.	PTI	Positive Ternary Inverter
7.	NTI	Negative Ternary Inverter
8.	HA	Half Adder

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

The scaling down of devices is increasing which leads to various issues in the device. We know, the dimension of devices has been decreased by two in every two years (According to Moore's) and this scaling down of devices facing several drawbacks. However, as device dimensions shrank down to the sun 22-nm region, scaling down is encountering limitations associated to device performances and fabrication technologies, as stated by ITRS 2009 edition. As a result of this scaling down, the devices are encountering issues such as doping and device structural changes, power consumption, electron tunneling through thin insulator layers and short channels, effects like short channel and related leakage currents [1]. We can overcome these limits by modifying channel materials in MOSFET structure and replacing it with Carbon Nano- tubes or array of carbon nanotubes. So, in the designing of the gates we will use CNTFET model instead of MOSFET. Because of its low OFF-current and ballistic transport characteristics, CNTFET has become a viable option for providing special qualities like low power and high-performance design. [2] – [5]. Another advantage of using CNTEFT over CMOS is that its threshold voltage is dependent on the diameter of the CNT. As a result, by changing the diameter and, in turn, the chirality of CNTs, we can reach a variety of thresholds.

The number of transistors on a device rises as technology scales down, creating issues with interconnect routing throughout the chip [6]. Chip area is decreased when Multi-Valued Logic (MVL) is used through lowering the quantity of interconnects [7]. The comparison is made between binary and ternary from which we can conclude that circuit complexity and cost has been improved results is high performance [8]. The implementation of ternary systems can be done in two ways: unbalanced (0, $V_{dd}/2$, V_{dd}) comparable to (0,1,2) and balanced ($-V_{dd}$,0, V_{dd}) corresponding to (-1,0,1) [9].

In our design, we have used unbalanced ternary system. A supply voltage of 0.9V is used in our design i.e. V_{dd}=0.9V.

Logic gates like AND, OR, and NOR have been created with less transistors in the circuit thanks to the use of the Gate Diffusion Input (GDI) technology, resulting in a lower power consumption and reduced room required. When designing low-power circuits, this approach can be used with less transistors than PTL and CMOS approaches used today [10]. the GDI method, which is based on basic cells. It has three inputs (G, P, and N), where the PMOS drain or source is the P node, the NMOS drain or source is the N node, and the NMOS and PMOS common gate input is the G node [11]. The substrate of NMOS and PMOS is connected to the N and P, respectively. Using these ternary gates, based on GDI we have designed a Half adder. This design is then compared with the existing design [12]. Integrating all these advantages results in highly efficient computational logics like ternary half adder.

1.2 CNTFET

CNTFET stands for Carbon Nano Tube Field Effect Transistor. A carbon nanotube is used as the channel in a field effect transistor, or CNTFET. Their great current carrying capacity and excellent metallic and semiconductor qualities make them extensively utilized in several applications. The demand for integrated circuits with fast speed, low power consumption, and tiny size is growing as technology progresses. As per Moore's law the size of transistor will reduced to two after every two years, but this is giving rise to effects like: shorter channel effect which leads to direct tunnelling, increase in gate leakage current [1]. The mentioned drawbacks can be overcome using CNTFET.

CNTFET emerged as a promising candidate for offering unique properties because of its low OFF-current characteristics and ballistic transport, allowing for high-performance design at cheap power. [2] through [5]. The dependence of the CNTEFT threshold voltage on the CNT diameter is another benefit of utilizing it instead of CMOS. Thus, we can achieve numerous thresholds by varying the diameter and, consequently, the chirality of CNTs.

The carbon atoms in the nanotubes utilized in CNTFETs are connected in a hexagonal pattern and have diameters measured in nanometers. All three carbon atoms in the structure are covalently bound to one another. The carbon nanotubes have a width of one nanometer and a potential length of many centimeters, when discussing their dimensions. These nano tubes are extremely tiny but powerful. They are flexible enough to assume a bent shape before returning to its original form; they are neither brittle not fragile. CNTFETs possess several advantages over other types of transistors. First, they have high carrier velocity. Second, CNT enhances electrostatic control and consumes less power.

Semiconducting single-wall CNTs are used in CNTFETs to construct electrical devices [2]. Single-wall CNTs, also known as SWCNTs, are made up of just one cylinder shown in figure 1.1, and because of their straightforward manufacturing method, they hold great promise as a MOSFET substitute. A SWCNT has the ability to act as a conductor or a semiconductor, depending on the arrangement of atoms along the tube. This is represented by the pair of integers (n, m) and which is also called as chirality vector. Examining a carbon nanotube's (CNT) indices (n, m) can be a simple method of determining if it is metallic or semiconducting. A CNT is metallic if, for any integer i, n = m or n - m = 3i. The tube is semiconducting under all other conditions. Use the formula below to find the CNT's diameter [30] :

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (1.1)$$

where a_0 = 0.142 nm is the distance between neighboring carbon atoms on an interatomic scale. The CNTFET schematic diagram is displayed in Fig. 1.1 [30]. The CNTFET features four terminals, just like the conventional silicon device. While the undoped semiconducting nanotubes are positioned as the channel area beneath the gate in Fig. 1, in order to provide a low series resistance in the ON-state, highly doped CNT segments are placed between the gate and the source/drain [2]. Gate is used to electrostatically turn on or off the device when the gate potential increases. MOSFETs and CNTFETs have similar I-V characteristics. It is known as the

threshold voltage, or the voltage needed to switch on a transistor. The half bandgap, which is inversely related to diameter, can be used to estimate the intrinsic CNT channel's threshold voltage to the first order [30].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \qquad (1.2)$$

Where distance between carbon-carbon atom is given by a = 2.49 A˚, the electric charge unit is denoted by e , the carbon π–π bond energy in the tight bonding model is given by V_π = 3.033 eV, and the CNT diameter is given by DCNT. A CNTFET with (19, 0) CNTs as channels has a threshold voltage of 0.293 V from (6) since a (19, 0) CNT's DCNT is 1.487 nm in length. There is empirical evidence to support the accuracy of this threshold voltage. The CNTFET's threshold voltage will fluctuate concurrently with the chirality vector. The ratio between the threshold voltages of two CNTFETs with different chirality vectors can be computed as follows, assuming that the m value of the chirality vector is always zero:

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT2}}{D_{CNT1}} = \frac{n_2}{n_1} \qquad (1.3)$$

Equation (1.3) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of a carbon nanotube. The threshold voltage of a CNTFET containing (13, 0) CNTs is 0.428 V, whereas a CNTFET with (19, 0) CNTs has a threshold voltage of 0.293 V. By mimicking the drain current of a CNTFET with chirality (19, 0) at the voltage threshold determined by (1.2), the ON-current of the reference transistor is achieved.

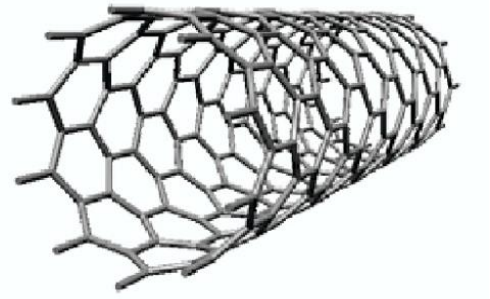


Fig.1.1 Single Walled CNT

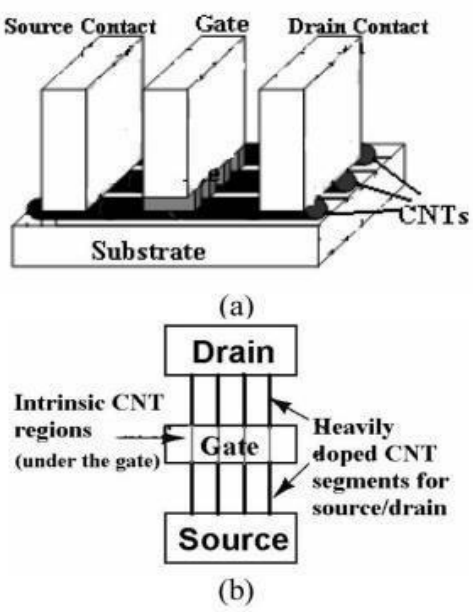


Fig. 1.2 Schematic of CNTFET a) Cross sectional view (b) Top view [30]

1.3 TERNARY LOGIC

Ternary Logic provides energy efficiency, simplicity in logic design, and a reduction in chip size and design complexity. Both serial and parallel arithmetic processes are made simpler with the aid of ternary logic. Serial and serial-parallel arithmetic processes can be completed more quickly because to ternary logic. A signed 32-bit multiplier can achieve a more than 50% reduction in chip size and power dissipation by employing an effective MVL implementation.

Based on MOS technology, there are two types of MVL (multiple valued logic) circuits: Current mode Circuits for MVLs and voltage mode Circuits for MVLs [7]. Different voltage levels are used in voltage-mode logic (VML) to represent logic values. Like this, in current-mode logic (CML), current levels are indicative of various logic values. CML circuits can be constructed with fewer transistors and are often fast. However, they have a major drawback in that they lose a lot of power. Three states 0, 1, and 2 represent the low, middle, and high ternary values in ternary logic. Voltage levels are another way to express these values. These logic states 0,1, and 2 are represented by the voltage values 0, V_{dd}, $V_{dd}/2$, and V_{dd}, [8], where V_{dd}=0.9V.

Table.1.1 Logic Symbols

Voltage level	Logic Values
0	0
$0.5V_{dd}$	1
V_{dd}	2

1.3.1 Types of Ternary logic inverters [25]:

1.3.1.1 Standard Ternary Inverter (STI)

1.3.1.2 Positive Ternary Inverter (PTI)

1.3.1.3 Negative Ternary Inverter (NTI)

The Truth Table for these three inverters is shown on Table III.

Table.1.2 Truth Table for STI, PTI and NTI [12]

Input I	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

The above inverters are implemented using the CNTFET. A ternary decoder generates three unary outputs for input I. The decoder is made up of a NOR gate based on the GDI approach, two NTI gates, and a PTI gate. The GDI approach is utilized to reduce the 10 transistors in the current NOR gate design to 8 transistors. Figure 3 shows the circuit diagram for a decoder [12].

STI (Standard Ternary Inverter): It is made up of two resistors and two MOS transistors (NMOS and PMOS). When V_{in}, the input voltage, is zero volts (logic zero), PMOS activates and NMOS switches off. Consequently, the output will become logic 2 (V_{dd}=0.9 V) and the resistor current will cease.

However, if the input voltage is 0.9V (logic 2), NMOS turns on and PMOS turns off. This prevents current from flowing through the resistors and changes the output to logic 0 (i.e., 0 volts). Furthermore, at 0.45 volts (logic 1), or the voltage level of $V_{dd}/2$, both PMOS and NMOS activate. Current may therefore pass via both resistors. The resistors, which are used to dissipate less power and have a R value of 1 mega ohm, are selected so that their resistance is substantially higher than the resistance of the transistors that are turned on [25].

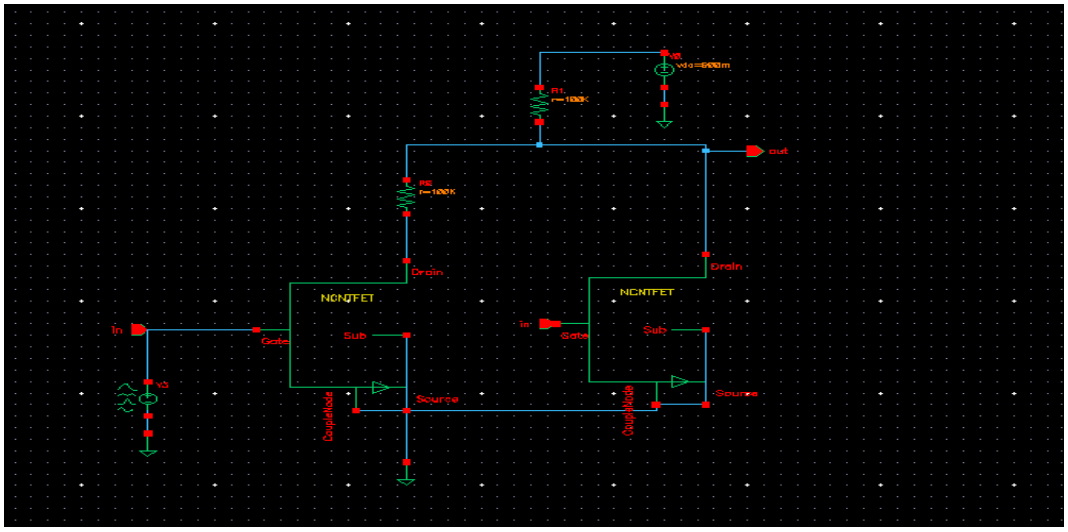


Fig.1.2 Circuit Schematic of Standard Ternary Inverter (STI)

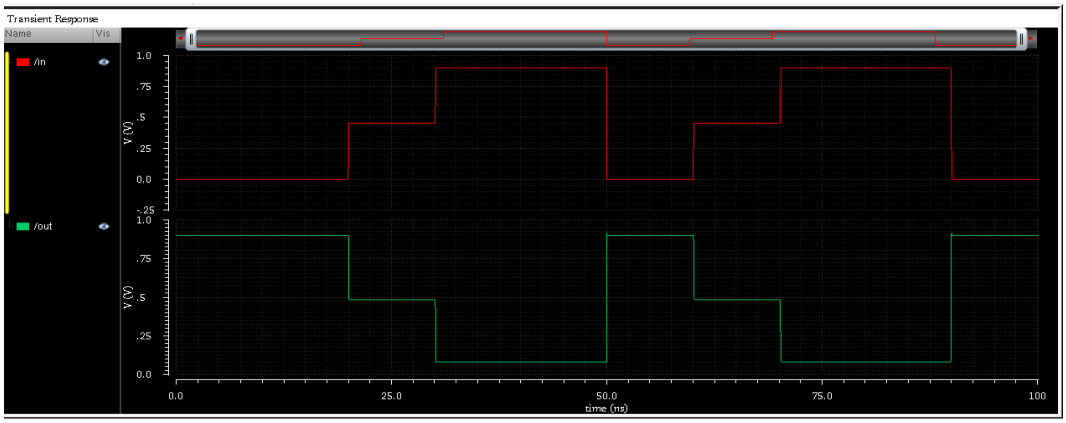


Fig.1.3 Transient response of STI

PTI (Positive Ternary Inverter): With PTI, the output is 0.9 volts (logic2) when input V_{in} hits 0 volts (logic0), as PMOS is currently turned on. This is because the circuit functions as a closed path, resulting in a total voltage drop of 1.8 volts at the output terminal. V_{in}=0.45 volts, or a logic 1, is the input; when this occurs, the output is 0.9 volts, or a logic 2. The output seems to be 0 volts (logic 0) when the input is displayed as 0.9 volts or as a logic 2 [25], this is because the PMOS gate to source terminal is open.

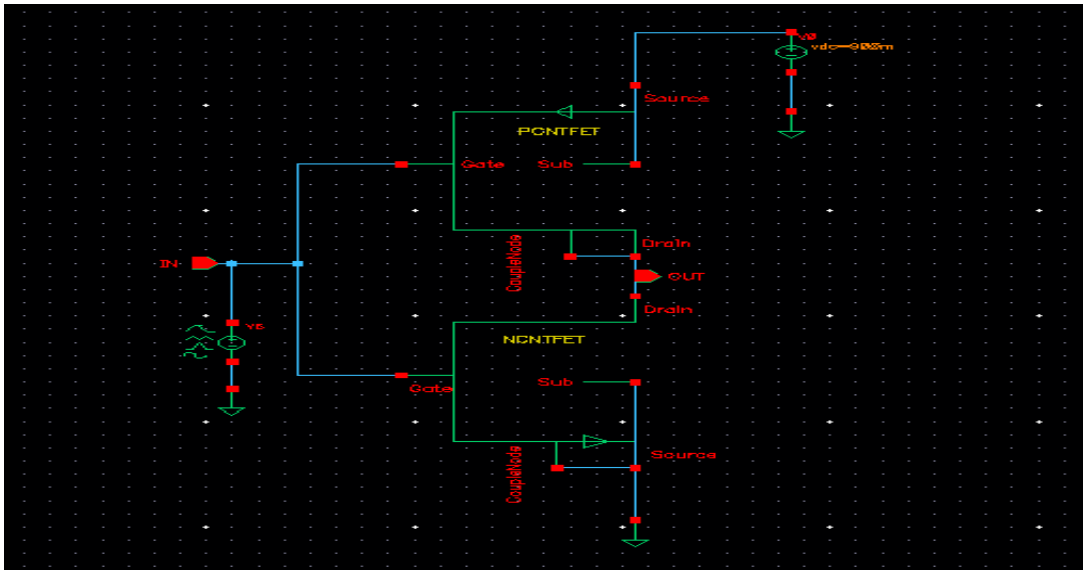


Fig.1.4 Circuit Schematic of Positive Ternary Inverter (PTI)

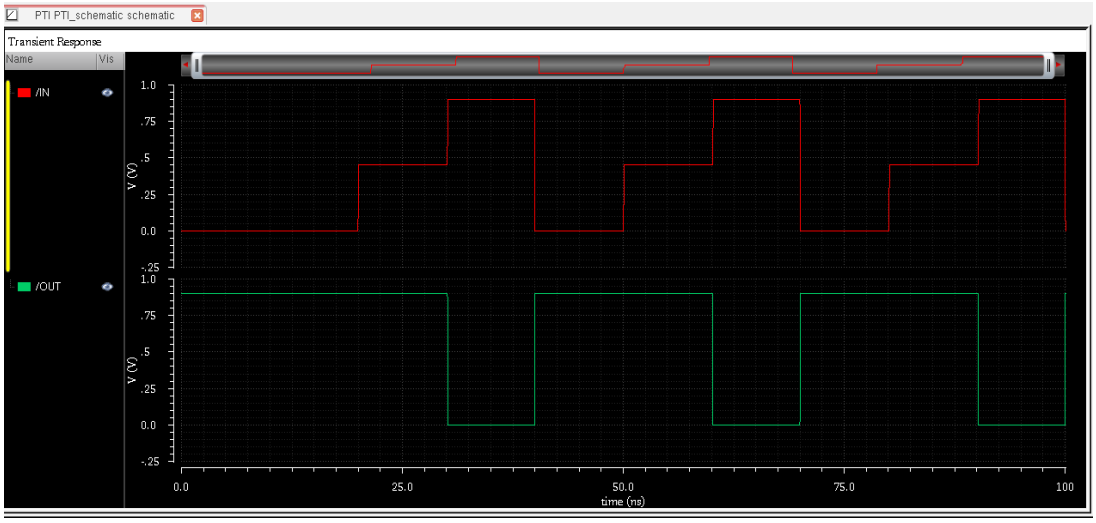


Fig 1.5 Transient response of PTI

NTI (Negative Ternary Inverter): NMOS is on when $V_{in} = 0.9V$. When a channel exists, that is, when $V_{gs} > V_t$ (the threshold voltage), current will always flow, indicating that the circuit's voltage is present. Thus, output from 0 volts (logic 0) to 0.9 volts.

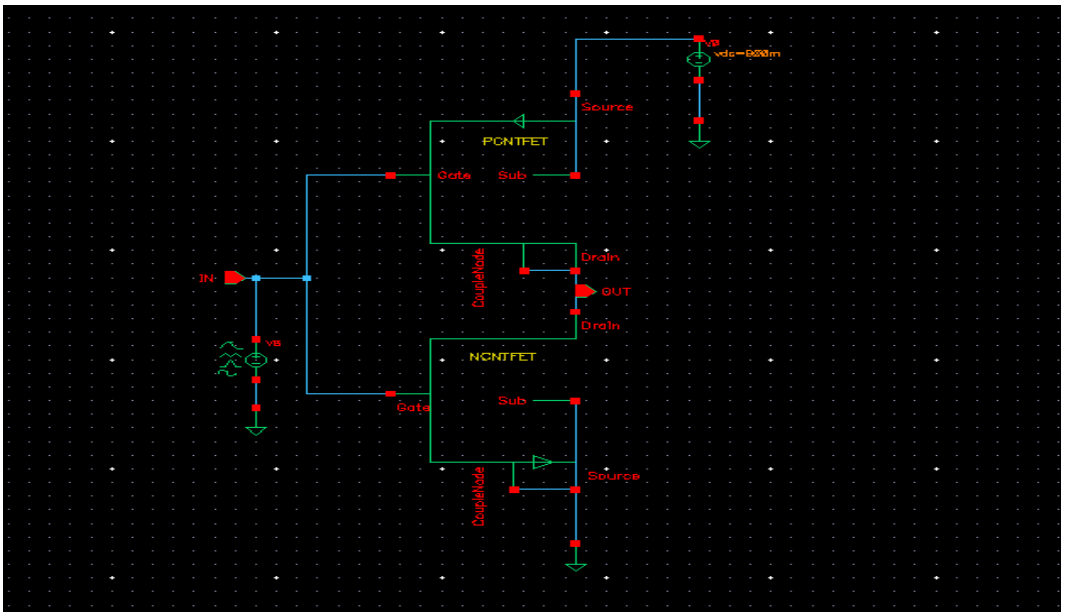


Fig 1.6 Circuit Schematic Negative Ternary Inverter (NTI)

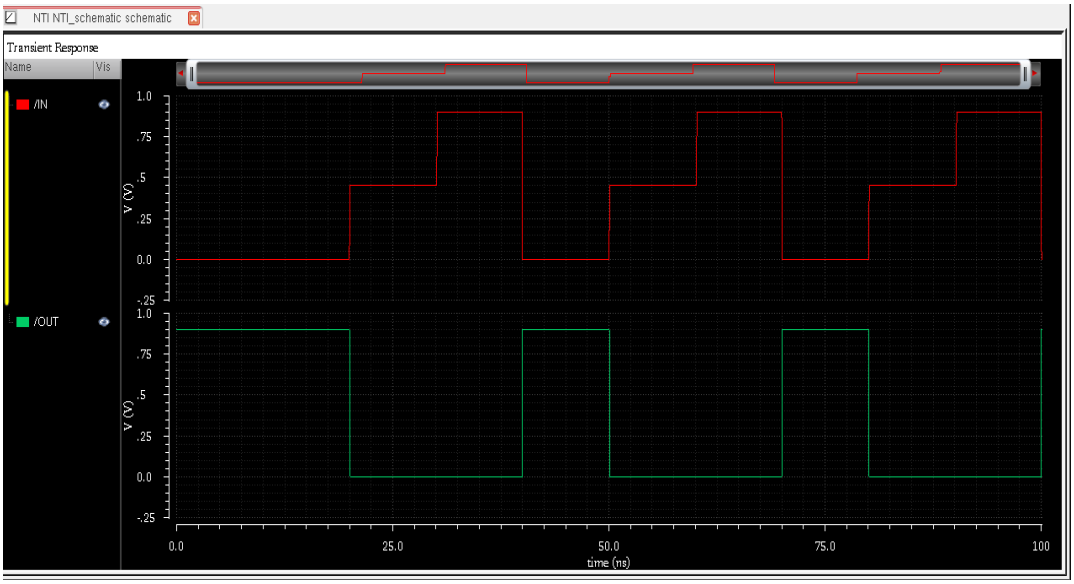


Fig 1.7 Transient response of NTI

Ternary inverters are used in the construction of ternary logic gates. Implementing ternary NAND and NOR gates is comparable to doing so with binary NAND and NOR gates. Here are several instances of fundamental resistor-based ternary NAND, T-NOR, T-AND, and T-OR gates.

1.4 SYMBOLS

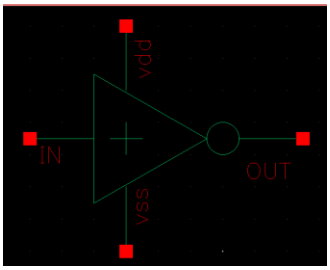


Fig. 1.8 PTI Symbol

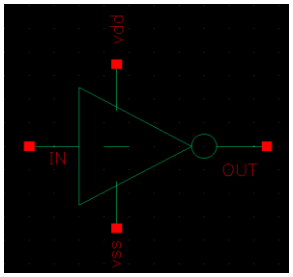


Fig.1.9 NTI Symbol

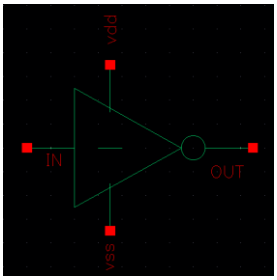


Fig.1.10 STI Symbol

Table.1.3 Truth Table for Ternary input logic gates [25]

A	B	T-NAND	T-NOR	T-AND	T-OR	T-EXOR
0	0	2	2	0	0	0
0	1	2	1	0	1	1
0	2	2	0	0	2	2
1	0	2	1	0	1	1
1	1	1	1	1	1	1
1	2	1	0	1	2	1
2	0	2	2	0	2	2
2	1	1	1	1	2	1
2	2	0	0	2	2	0

1.4 GATE DIFFUSION INPUT TECHNIQUE (GDI)

Figure 1 illustrates the GDI approach, which is predicated on the use of simple cells. There are three inputs (G, P, and N), where the G node is the NMOS and PMOS common gate input, the P node is the PMOS drain or source input, and the N node is the NMOS drain or source input [11]. The N and P, respectively, are connected to the

substrates of NMOS and PMOS.

CMOS implementation of same function required large number of transistors which require larger chip area and increases complexity. GDI based gates require less chip area, as we must only change the input to get the required functionality.

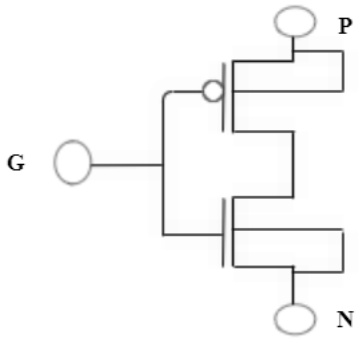


Fig.1.11 GDI basic cell [11]

Table V represents implementation of various Boolean function based on GDI technique. We can see from the Table that, by changing the input configuration results in various Boolean functions. In this paper, we have implemented functions like OR, AND, NOT, NOR (by simply using one OR and one NOT).

Table.1.4 Implementation of various Boolean function based on GDI technique.

N	P	G	Out	Function
1	Q	P	P+Q	OR
Q	0	P	PQ	AND
R	Q	P	$\bar{P}$Q+PR	MUX
0	1	P	$\bar{P}$	NOT

The main idea behind the GDI technique is that an n-type diffusion region can be diffused inside a p-type diffusion area to create a virtual gate. The gate regulates the transistor action in the circuit and serves as an input terminal. To make a GDI circuit we need a PMOS transistor, NMOS transistor and a resistive load. The GDI logic is comparatively simple that other logic gates because it has only one input terminal.

Additionally, it reduces the overall resistance of the circuit by doing away with the need for an external pull-up or pull-down resistor. When the GDI technique is implemented, it gradually decreases the number of transistors required is one of the main benefits of the GDI technique, as it greatly lowers area and power consumption. The number of transistors needed for the circuit is decreased because this method just requires one transistor for shift registers and logic conversions. In this way, the overall circuit power is also reduced.

One benefit of GDI technique is that it may create complicated digital circuits using minimal number of gates. These building pieces can be combined in several ways to produce an infinite variety of circuit designs. Moreover, the GDI technique reduces complexity of digital circuit design by simplifying circuit architectures. Many digital circuits such as adders, multipliers, low-power Boolean logic gates, RAM, analog circuits, have made extensive use of the GDI approach. Digital circuit approaches such as CMOS and SRAM can be substituted with the GDI technique.

For digital circuits found in portable electronics, GDI technology provides a dependable solution. The GDI approach is a desirable and practical substitute for conventional circuit techniques because of its advantages, which include better performance, lower power consumption, and smaller circuit sizes.

In conclusion, GDI technique is a simple and effective CMOS technology for designing low power digital circuit with high performance. The GDI technique's simplicity and low power make it one of the most viable solutions for digital circuits.

1.4 GDI (Gate Diffusion Input) BASED GATE DESIGN

1.6.1 Two input OR Gate

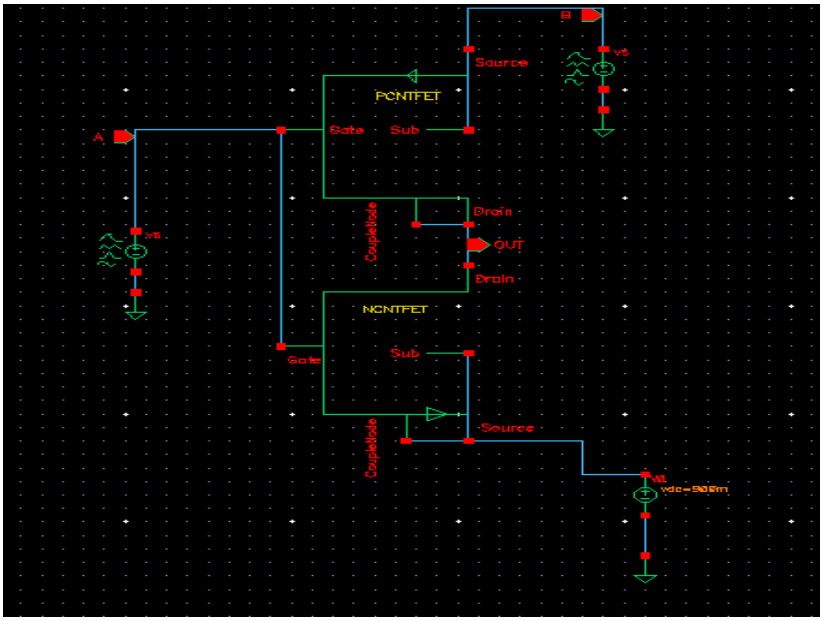


Fig.1.12 GDI based 2 input OR gate.

1.6.2 Two input AND Gate

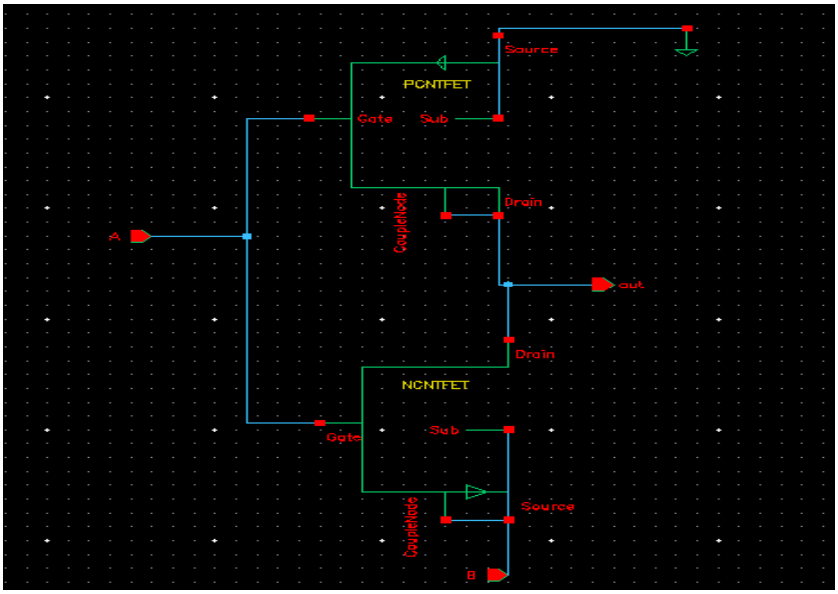


Fig.1.13 GDI based 2 input AND gate.

1.7 OBJECTIVE

Ternary Half Adder is based on ternary logic. It is designed using CNTFET and the compared with the existing design [12]. The gates used in the design of HA is based on GDI technique to reduce the quantity of transistors utilized. In the existing design of HA, the logic gates are designed using the conventional method, while in our design we are using GDI technique. One of the significant advantages of GDI technique is the reduced transistor count, which contributes significantly to low power consumption and decreased area. There is a decrease in the number of transistors needed for the circuit because this technique uses only one transistor for shift registers and logic inversion thus, lowers the circuit's overall power usage.

In the designing, we have integrated all the advantages like used CNTFET instead of MOSFET, used ternary logic instead of binary logic and used GDI technique instead of Conventional technique for logic gates design. So, integrating all this advantages, we can design highly efficient computational logics like Half adder, Full adder, Multiplier etc.

This report contains the ternary half adder's GDI-based design technique using CNTFET. The design of Half adder involves the use of ternary buffer, ternary logic gates like AND, OR and ternary decoder. In all this logic designs, we have used supply voltage i.e. V_{dd} =0.9V except ternary buffer, where supply voltage of 0.45V is used for PCNTFET. Upon comparison, our suggested Half Adder (HA) design has a significantly lower power and delay product (PDP) than the current design. Table I provides the ternary half adder's truth table.

Table.1.5 Truth Table of HA

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

Using K-map and the truth table above, we can formulate the expression for Sum and Carry as follows:

$$Sum=A_2B_0 + A_1B_1 + A_0B_2 + 1.\ (A_1B_0 + A_0B_1 + A_2B_2) \quad (1.4)$$

$$Carry=1.\ (A_1B_2 + A_2B_1 + A_2B_2) \quad (1.5)$$

The Circuit Schematic of Half Adder (HA) is shown in fig.1.14:

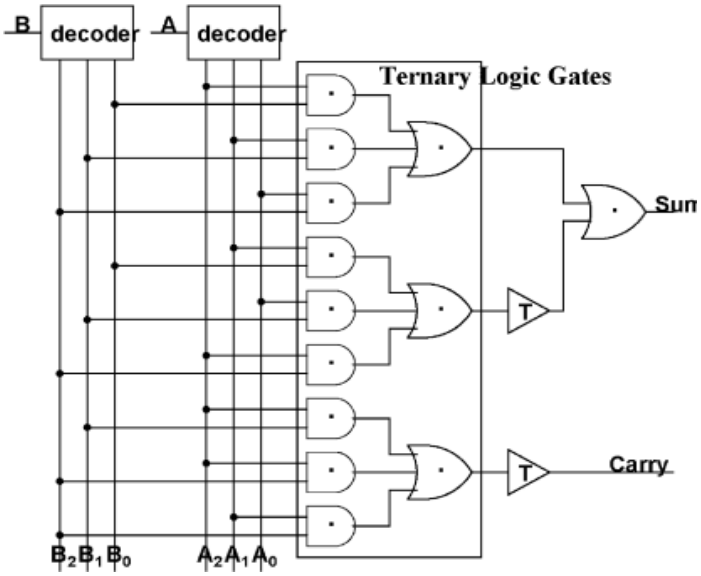


Fig.1.14 Existing Circuit Schematic of HA [13]

The above is the circuit schematic of existing design of HA. In this schematic, we have replaced the conventional logic gates with the GDI based logic gates to reduce the area and increase the overall performance.

1.8 METHODOLOGY

For the design purpose we have used Stanford CNTEFT model- Verilog A with 32nm technology. Cadence Virtuoso is the design tool utilized in the simulation.

1.9 THESIS ORGANIZATION

This Thesis is divided into six chapters. Ternary adder based on GDI technique, CNTEFT, Ternary Logic, GDI are covered in chapter 1. Chapter 1 also covers the strategy, motivation, goal, and organization of the thesis. Literature survey and all the previous work related to Ternary Adders is done in chapter 2. The comparison between ternary logic and binary logic, MOSFET and CNTFET with conclusion, is done in chapter 3. In chapter 4, there is discussion about the existing HA design, proposed HA design, ternary decoder, and ternary buffer. In chapter 5 Simulations and result is

discussed and in chapter 6, conclusion and future scope is discussed.

CHAPTER 1: Provides the information about the need of the CNTFET, Ternary logic and GDI technique. It also provides information about the existing Ternary HA circuit. The objective, tools used, Motivation is also included in this chapter.

CHAPTER 2: Literature survey is done in this unit. The previous work related to the Ternary Adders is done in this unit. A comparison has been made, based on parameters like PDP of HA with the existing HA design. The results have been shown in this report and from that we can conclude that the PDP is comparatively less than the existing HA design.

CHAPTER 3: The comparison between binary and ternary inverter, CNTFET and MOSFET, is done in this unit conclusion is also drawn, why we use Ternary logic and CNTFET in our design.

CHAPTER 4: It deals with the workflow, from where we got the idea i.e. existing HA design, proposed HA design, ternary decoder, and ternary buffer. Symbols for both Ternary buffer and Decoder is included in this chapter.

CHAPTER 5: In this chapter, conclusion and future scope is discussed. The achieved result of low PDP can be used further in other digital integrated circuits. The simulation result of proposed design is achieved using Stanford CNTEFT model-Verilog A with 32nm technology using cadence virtuoso with the supply voltage of 0.9V.

CHAPTER 6: It deals with conclusion and future scope of the proposed HA design. Later in the report, publications and references are added.

CHAPTER 2

LITERATURE REVIEW

2.1 LITERATURE REVIEW

Binary Logic is a two valued function i.e. ‘0’ and ‘1’ or ‘True’ and ‘False’. But, in some cases it is not possible to decide whether it is ‘True’ or ‘False’. For instance, every signal value in a logic circuit, which can be either 0 or 1 in a steady state, can alternate between 0 and 1 or 1 and 0 in a transient state, making it difficult to determine the value's true value. Another example where it might be challenging to determine whether a value is 0 or 1 in many situations is the starting states of sequential circuits. Moreover, it can be argued that some data are irrelevant to the algorithm or that the process does not stop for a particular set of data. Instead of using binary logic, which uses two values to represent states that are clearly true or false, we can use ternary logic, which uses three values to represent the ambiguous states described above [14].

In [15], a T-gate solution utilizing bipolar transistors is suggested. A different T-gate implementation utilizing MOS technology has been suggested by Muftah and Smith [16], [17]. The major disadvantages of Ternary Logic are its complexity. As the number of variables increases, the complexity of logic gates increases rapidly.

A different ternary logic family is presented in this contribution in [18], which can be applied to the design of sequential and combinational ternary logic circuits. The new family can be implemented in VLSI because it is based on MOS technology. It consists of a set of NANDS, NOR, and inverter gates. Charge-coupled devices (CCDs) have been used in the creation of MVL circuits [19]. Molecular devices are emerging as a possible replacement for current silicon technology as we enter the age of nanotechnology. A lot of research is being done on carbon-nanotube field-effect

transistors (CNFETs) as potential replacements for silicon MOSFETs. In-depth research has begun to investigate potential circuit applications and comprehend the device mechanics of CNFETs [20]. The bandgaps of carbon nanotubes are diameter dependent. The bandgap measures the threshold voltage of the CNTFET. Carbon nanotubes are appropriate for voltage-mode MVL implementation because their diameter may be adjusted to have specific threshold voltages [21].

It is challenging to maintain supply and threshold voltage scaling to provide the necessary reliability, controlled energy consumption, power dissipation management, and performance growth due to the rapid advancement of technology. Several design strategies have been explored to reduce power consumption [22]. Pass transistor logic is one type of logic that is frequently used in low-power digital electronics. PTL provides several advantages, including lower power consumption, faster speeds, and fewer connection effects. The GDI approach helps to lessen a few of PTL's shortcomings. This makes it possible to use just two transistors to implement a large range of complicated logic functions. Furthermore, it can be used to improve power characteristics and build low-power, fast circuits with fewer transistors than CMOS and existing PTL techniques. The GDI approach offers a straightforward top-down design methodology and is helpful for quickly building low-power circuits with just two transistors, as opposed to CMOS and existing PTL approaches [23]. Concurrently, it enhances static power characteristics and logic level swing. The comparison and analysis of various logic gates based on various technique is already done in [24]. It has been observed that the Gate Diffusion Input (GDI) design style exhibits better qualities than other design styles. In terms of factors like power and transistor count, the optimal logic design style may be the gate diffusion input design style. Therefore, high-performance, and low-power applications can both benefit from the employment of the gate diffusion input design approach. CMOS implementation of same function required large number of transistors which require larger chip area and increases complexity. GDI based gates require less chip area, as we must only change the input to get the required functionality.

An existing design of HA involves the use of CNTFET and Ternary Logic is already given in [12]. In this design, the logic gates are designed using the conventional method so, we have replaced the logic gate design with GDI technique which results in reduced area, less complexity, better speed, and low power consumption.

2.2 TECHNICAL GAP

Following observation and review of all the reported work, there is a technical gap. The main objective of the design is to reduce the power consumption and increase the speed of operation. Ternary logic provides fewer interconnections, compact circuitry, and faster computations in advanced computing systems. The proposed design when compared with existing designs, provides less power consumption, better speed, and less chip area. Today, low power consumption is the basic requirement for the VLSI system which can be achieved by reducing number of transistors on chip. So, we have used GDI (Gate Diffusion Input) technique for the designing of Gates. Instead of using MOS, we have used CNTFET as they have less power consumption and provides higher speed. Integrating all these advantages results in highly efficient computational logics like half adder and full adder. A comparison has been made, based on parameters like PDP of HA with the existing HA design. The results have been shown in this report and from that we can conclude that the PDP is comparatively less than the existing HA design.

Ternary half adders are digital circuits that can add ternary numbers. Its two inputs, A and B, and its two outputs, S and C, represent the carry that comes from the addition and the total of A and B, respectively. Carbon nanotube field-effect transistors (CNTFETs) are a promising technology for implementing high-performance and low-power digital circuits, and the GDI (Gate Diffusion Input) technique has been widely used to create effective digital circuits. Consequently, a high-performing and low-power solution can be achieved by combining the GDI technique with CNTFET technology to create a ternary half adder.

Using the GDI technique, a circuit's performance can be improved, and its transistor count can be decreased. GDI can be used to create several digital logic gates, such as the AND, OR, NOT, XOR, and XNOR gates. The Ternary logic functions required for the addition of ternary numbers can be implemented for a ternary half adder using GDI logic circuits. Furthermore, by diffusing an n-type diffusion region within a p-type diffusion area, the GDI approach may be utilized to construct a virtual gate, which lowers the number of transistors needed in the circuit.

CNTFETs are another promising technology for implementing high-performance digital circuits. They are smaller in size and have lower power consumption compared to traditional MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The unique properties of CNTFETs make them an ideal technology for designing digital circuits that require high performance and low power consumption.

By combining the GDI technique with CNTFETs, a high-performance ternary half adder circuit can be designed. The GDI technique can be used to implement the ternary logic functions needed for addition, while CNTFETs can be used in place of traditional MOSFETs to increase performance and reduce power consumption. The GDI technique also allows for the creation of virtual gates, further reducing the number of CNTFETs required in the circuit.

The design process for a ternary half adder based on GDI technique using CNTFET technology involves several steps. The logic diagram for the ternary half adder should be created based on the GDI technique and the ternary logic functions needed for addition. Using this logic diagram, each gate in the circuit can be designed using CNTFETs with the GDI technique. The circuit can then be verified using simulation software that considers the unique properties of CNTFETs. The design can be optimized to reduce power consumption and improve performance by fine-tuning the design parameters.

In conclusion, designing a ternary half adder based on GDI technique using CNTFET technology can lead to a high-performance and low-power solution for addition of ternary numbers. The GDI method can be applied to lower the number of transistors in a circuit and enhance its functionality, whereas power consumption can be decreased, and performance can be increased with CNTFETs. Future research in this area may lead to further advancements in high-performance digital circuits using CNTFETs and the GDI technique.

CHAPTER 3

COMPARISONS WITH EXISTING ART OF TECHNIQUES

3.1 BINARY VS TERNARY LOGIC

Binary logic is two valued or Boolean logic which deal with either true or false. An approach known as multi-valued logic (MVL) has more than two truth values or potential states. By adjusting the base or radix of a two-valued logic, we can convert it into an n-valued logic. For instance, ternary logic is used in three valued logics, where base or radix is three. Quaternary logic, on the other hand, is used in four valued logics, where radix is four, and so forth. These four valued logics have the logic states 0,1,2, and 3, and such three valued logics have the logic symbols 0,1, and 2. Radix is the number of distinct digits that can be stated in terms of a single digit. The binary system uses the symbols "0" and "1" to represent values, whereas the ternary system uses the three logic symbols (0, 1, and 2) [25]. Also, we can write (-1,0,1) to represent ternary logic. In the architecture of digital systems, "three valued" ternaries offer more benefits than binary logic. The primary benefit of utilizing ternary logic is that it allows us to send a greater amount of multivalued logic information, which reduces the space of the chip. It gets more attention than others because of the estimated connectivity cost being lower.

Mathematically, we can observe that ternary coding is much efficient than the binary coding. But it is less used in computation as binary logic is already established and implementation of ternary logic is more complex. Ternary logic is used in algorithms that use decision trees and in digital communications where error correction coding is employed. As the technology was absent for mass production of MVL so circuit implementation has been delayed. Recently, there has been a lot of activity in the study of compact MVL devices that incorporate multiple-switching characteristics in a single device, such as quantum dot/super lattices-based constant intermediate

current and 2D heterojunction-based negative-differential resistance (NDR)/trans conductance (NDT) devices [26]. Thus, the issue of implementation has also been resolved. When designing logic gates, the use of binary logic may result in more complex circuits and higher power consumption. While binary logic is used for quick computing, ternary logic gates are employed for decoding since they require fewer gates. As integration density rises, CMOS technology is up against a power scaling limit. MVL can be used to tackle this power scaling issue. To overcome the power scaling problem and raise integration density to peta-scale levels by lowering system complexity, multi-valued logic (MVL) is a desirable substitute.

So, at the end we can conclude that ternary logic is a good replacement to binary logic in terms of decreasing circuit complexity and resolving power scaling challenge in CMOS.

3.1.1 CONCLUSION:

Ternary logic has advantages in terms of binary arithmetic, especially for complex calculations involving many digits. Ternary arithmetic can be up to three times faster than binary arithmetic because it can process three digits at once, making it more efficient. This approach can be especially useful in computing hardware such as GPUs, where larger calculations are needed to produce high-quality graphics.

Another advantage of ternary logic is its ability to reduce circuit complexity, size, and power consumption. Compared to binary circuits, ternary circuits can perform the same operations using fewer transistors, reducing the circuits' size and power consumption. This reduction in power consumption makes ternary circuits particularly useful for battery powered devices where power efficiency is critical.

Ternary logic can also improve the computational power of digital circuits by allowing the use of multiple levels of voltage. In some cases, the third logic state can be used to store information or as an "error flag" to indicate errors during operation. This approach can increase circuit efficiency by reducing the need for additional logic gates and circuits, further reducing power consumption.

In addition, ternary logic can be useful in quantum computing, where qubits (quantum bits) are used to store data. Using qubits, more complex calculations are possible due to multiple states in Qubit. Ternary logic can be used to represent complex quantum states, leading to better performance and more efficient quantum computers. In summary, ternary logic offers several advantages over binary logic, including increased information density, improved computational power, reduced circuit complexity, and lower power consumption. The use of ternary logic can lead to faster, more powerful digital circuits with lower power consumption, making it a potentially significant technology for the future. However, the use of ternary logic is not yet widespread, and binary logic remains the dominant standard in digital electronics today.

3.2 MOSFET VS CNTFET

The MOSFET, is made by carefully oxidizing silicon. MOSFETs have an insulated gate, and the device's conductivity is determined by its voltage. In contrast to bipolar transistors like BJTs, it requires no input current to control the load current.

The term "CNTFET" refers to a type of transistor that has good performance at minimal power which uses carbon nano tube as channel, and it has low OFF- current properties.

Multiple thresholds are needed to construct ternary logic circuits using standard MOSFETs, and these can be obtained when we body bias the MOS transistor. Due to this reason we move to CNTFET as it is easy to change the threshold voltage in CNTFET by just changing the chirality. According to research, ternary logic circuits perform better with CNTFETs because they allow the physical dimensions of carbon nanotubes (CNTs) to be channeled to produce different threshold voltages. When we change the diameter of CNTFET, its chirality also changes. By changing its diameter, one can create a changeable threshold voltage. Therefore, by using CNTFETs with distinct chirality, it is possible to obtain the numerous thresholds needed to build ternary logic circuits. Because CNTFET technology offers improved energy efficiency by up to ten times than CMOS technology, it could eventually take the place of CMOS technology in circuit design.

The scaling down of devices is increasing which leads to various issues in the device. We know, the dimension of devices has been decreased by two in every two years (According to Moore's) and this scaling down of devices facing several drawbacks. But as the ITRS 2009 version points out, there are limits to scaling down related to the device performances and fabrication technology as device dimensions shrunk down to sun 22-nm range. The devices are experiencing issues such as electron tunneling through thin insulator coatings and small channels, the corresponding leakage currents, passive power dissipation, short channel effects, and changes in doping and device structure because of this scaling down [1]. We can overcome these limits by modifying channel materials in MOSFET structure and replacing it

with Carbon Nano- tubes or array of carbon nanotubes. So, in the designing of the gates we will use CNTFET model instead of MOSFET model.

We can conclude that using CNTFET instead of MOSFET increases the device performance.

3.2.1 CONCLUSION:

Digital electronics commonly uses two types of field-effect transistors: MOSFET and CNTFET. Even though they both function according to the field effect theory, they differ in several ways regarding their design, functionality, and usefulness.

For many years and up to present day, MOSFETs have dominated the field of digital electronics as they are easier and less expensive to create than CNTFETs, they have better design guidelines because of their well characterized nature.

However, CNTFETs have a few advantages over MOSFETs, such as increased size, power consumption, and performance. Because CNTFETs are composed of nanotubes that are merely a few atoms wide, more transistors may be adjusted into given amount of area.

Additionally, CNTFETs perform better than MOSFETs. They can run at lower voltages, consume less power, and have faster switching speeds. Because of these benefits, they are especially well- suited for uses like portable devices, which call for great performance and low battery consumption.

In summary, every semiconductor like MOSFETs and CNTFETs has both advantages as well as disadvantages and the decision between two relies on the objectives of the application. In digital electronics, MOSFETs continue to be the most widely used technology; nevertheless, CNTFETs have some unique benefits that set them apart for specific uses. Future advancements in both technologies are probable in store, and they likely result in even more potent and efficient digital electronics, given the ongoing progress in nanotechnology.

3.3 Symbol for MOSFET and CNTFET:

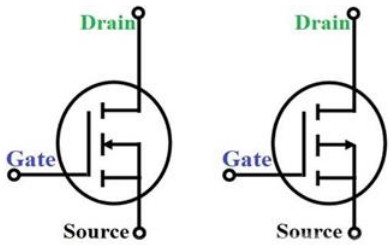
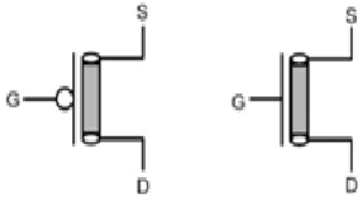


Fig 3.1 MOSFET Symbol (N-channel and P-channel) [28]



P-CNTFET N-CNTFET

Fig 3.2 CNTFET Symbol (P-CNTFET and N-CNTFET) [29]

The comparison between the techniques is done above. From the above discussion we can conclude the real reason behind the use of ternary logic instead of binary and CNTFET instead of MOSFET.

CHAPTER-4

SETUP AND SIMULATIONS

The fundamental criterion for a VLSI system nowadays is low power consumption, which can be addressed by lowering the number of transistors on the device. As a result, we designed gates using the GDI (Gate Diffusion Input) technique. Instead of using MOS, we have used CNTFET as they have less power consumption and provide higher speed. To design HA or full adder we can integrate all the advantages of highly efficient computational logic.

In the previous chapters, we have already discussed about CNTFET, GDI and Ternary logic. The gates which are used in the design of half adder has already been simulated and symbols has been created, so that we can directly use this in the HA design. The existing half adder design based on ternary logic has already been discussed. In the design of the proposed HA, we have used ternary decoder and ternary buffer also.

4.1 Existing HA Design

We learned how to create ternary logic gates using the GDI technique in previous section. These gates can now be used to build other arithmetic circuits, including full and half adders. The schematic diagram of HA described in [13] is shown in figure 4.1 below.

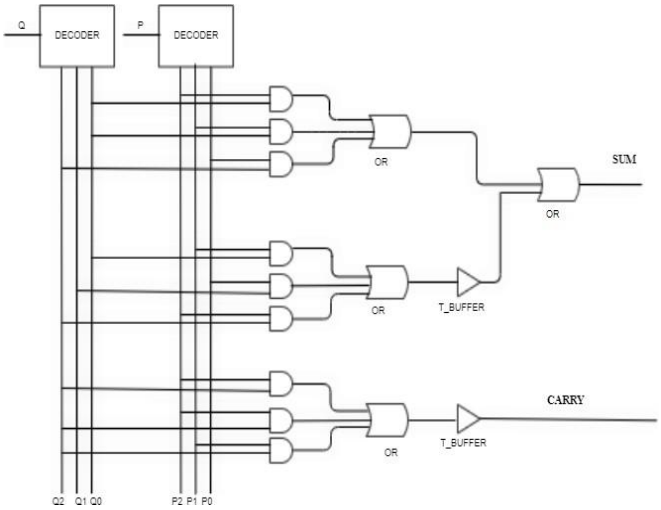


Fig.4.1 Schematic diagram of HA

We can use binary logic gates for ternary logic gates in the HA architecture given in [13] since the decoder's output only has two logic levels, 2 or 0, which are equivalent to logic 1 and logic 0 in binary. The computing speed is accelerated by these binary logic gates. However, because these logic gates need a lot of transistors, additional chip space is needed when creating them. So, to overcome this we develop a logic gate design using the GDI technique, which results in a reduced number of transistors, low power, and less area requirement.

4.2 Proposed HA Design

To lower the total area, we replaced the logic gates with GDI-based gates in the HA architecture we suggested in this work. Table IV, which is below, displays the truth table for HA.

Table.3.1 Truth Table of HA

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

The expression for sum and carry can be written as follows using the truth table above:

$Sum=P_2Q_0 + P_1Q_1 + P_0Q_2 + 1.\ (P_1Q_0 + P_0Q_1 + P_2Q_2)$ (4.1)

$Carry=1.\ (P_1Q_2 + P_2Q_1 + P_2Q_2)$ (4.2)

Where P_k and Q_k stand for the decoder's output for inputs P and Q in Figure 4.1. The logic function of the level shifter or ternary buffer employed in the current architecture is discussed further in this chapter.

4.3 Ternary Decoder

An electrical circuit with three input lines and many output lines that represent the various ways in which the input lines can be combined is called a ternary decoder. It converts input signals with three possible states—typically represented by the numbers 0, 1, and 2 into output signals that are used to control a variety of devices, including memory chips, motors, and LEDs. The decoder consists of two NTI gates, a PTI gate, and a NOR gate based on the GDI approach. The same idea is depicted in the following figure:

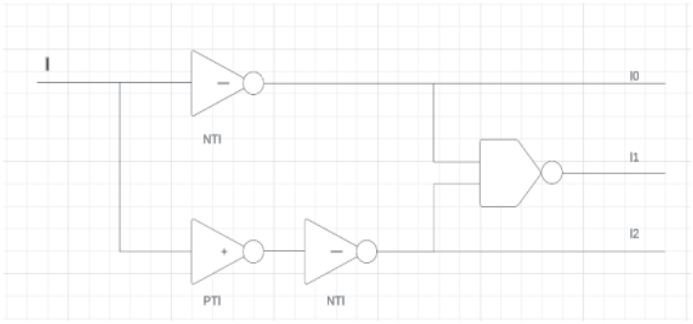


Fig 4.2 Ternary Decoder

One input and three outputs make up a combinational circuit which is called as ternary decoder. It converts an input of x into a unary function. The response of the ternary decoder for input x is given by [12]:

$$X_k = \begin{cases} 2, & if\ x = k \\ 0, & if\ x \neq k \end{cases} \qquad (4.3)$$

where k in the above equation can have logic value of 0,1 &2. A NOR Gate, two NTIs, and one PTI make up the decoder circuit. This ternary decoder will be used in our half-adder circuit design.

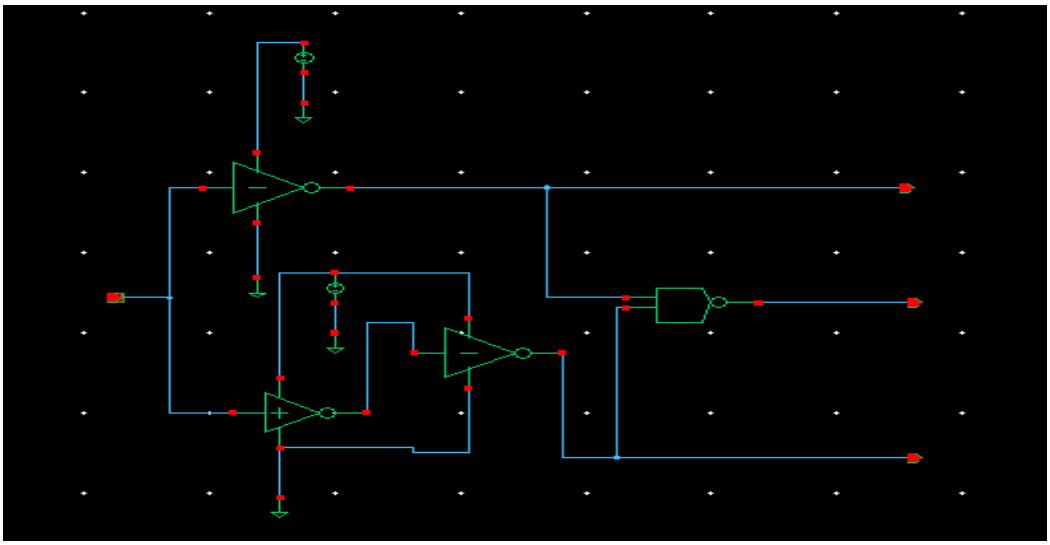


Fig.4.3 Circuit Schematic of Ternary Decoder

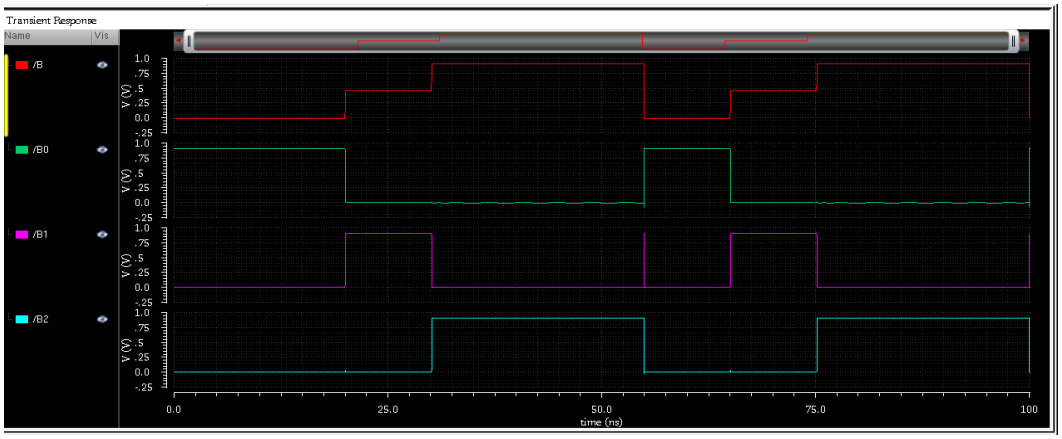


Fig.4.4 Output Waveform of Ternary Decoder

4.3.1 Symbol for Ternary Decoder:

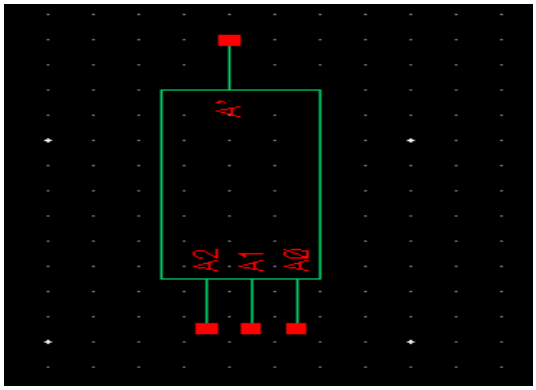


Fig.4.5 Ternary Decoder symbol

4.4 TERNARY BUFFER:

Ternary buffer (T- buffer) which is also called as level shifter. For the design of ternary buffer, we have used NCNTFET, PCNTFET and NTI. Input is given to NTI first and then the output of NTI is connected to the input of PCNTFET and NCNTFET [12]. The PCNTFET is provided with a supply voltage of 0.45V. The logic expression of Ternary Buffer is given by:

$$Out = \begin{cases} 1, & if\ in = 1,2 \\ 0, & if\ in = 0 \end{cases} \qquad (4.4)$$

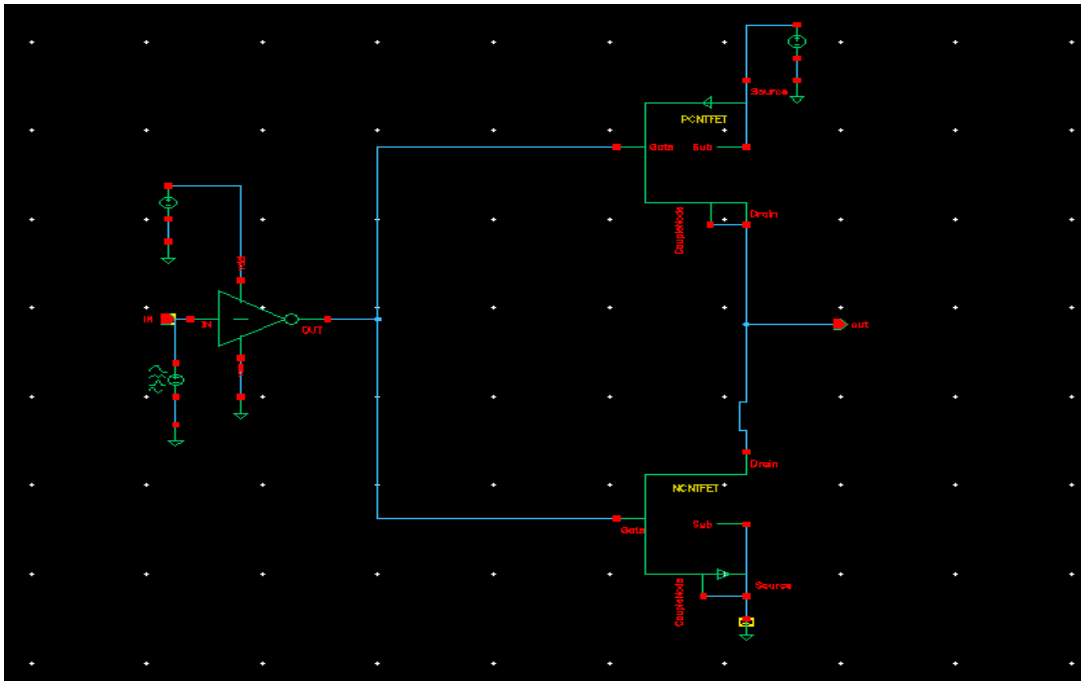


Fig.4.6 Circuit Schematic of Ternary Buffer

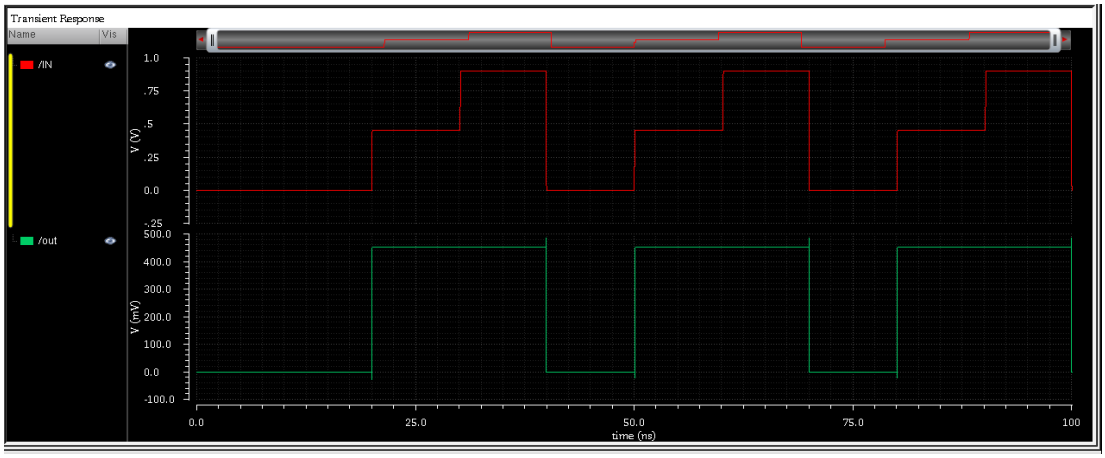


Fig 4.7 Transient response of Ternary Buffer

In this design of ternary buffer, the input is given to an NTI, source of PCNTFET is connected to the supply of 0.45V. Both NCNTFET and PCNTFET have a chirality value of (19,0).

4.4.1 Symbol for Ternary Buffer

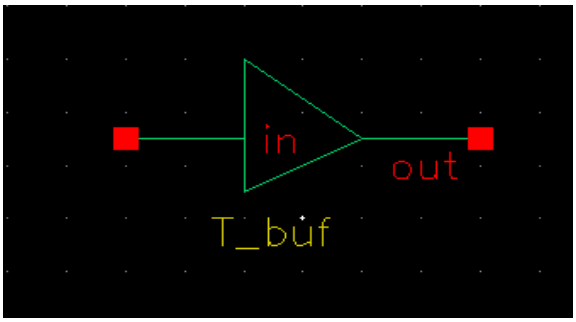


Fig.4.8 T-Buffer Symbol

CHAPTER 5

RESULTS AND DISCUSSIONS

Now, we will integrate all the components together to design a half-adder. The proposed design of the HA and its output waveform is shown in the below figure6.1 and figure6.2. Ternary buffer, Ternary Decoder, and Ternary Logic Gates (AND, OR) are used in the HA design.

5.1 SIMULATIONS

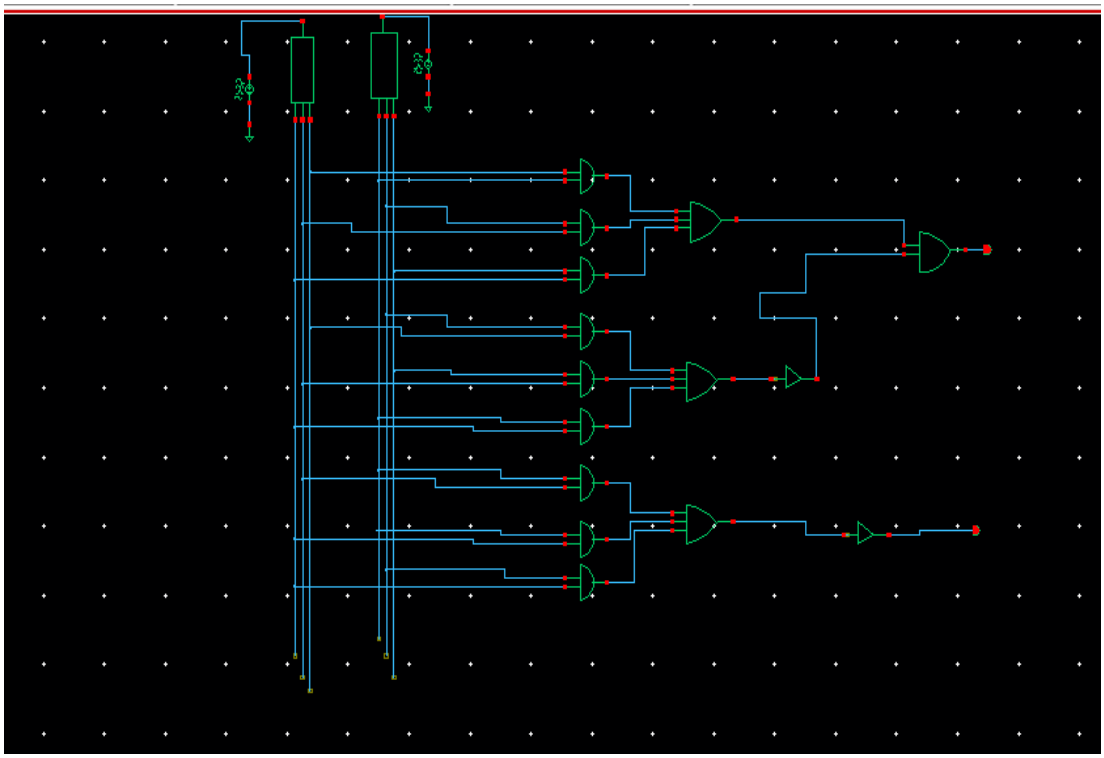


Fig. 5.1 Circuit Schematic of proposed Half Adder (HA)

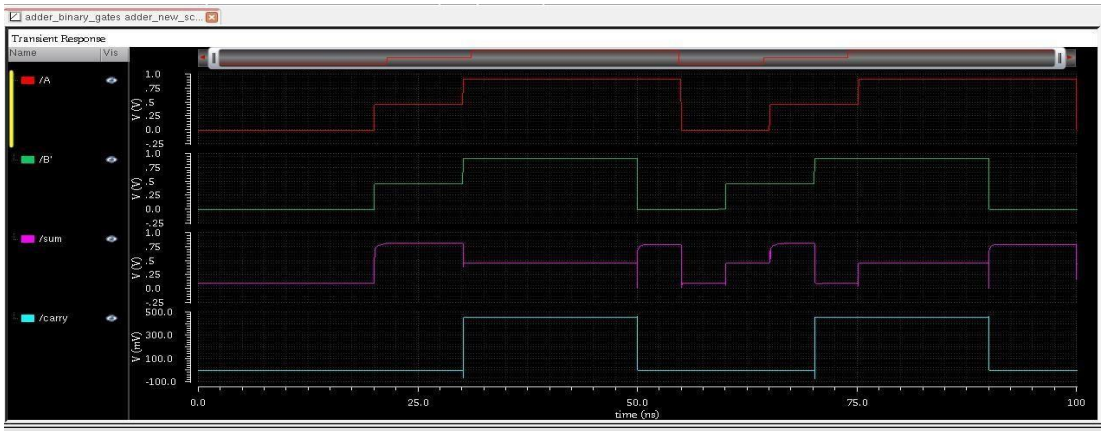


Fig 5.2 Output Waveform of HA

This output waveform can be verified form the above truth table of HA. We have converted this half adder in the form of symbol, so that we can use it in other circuit design like Full adder etc.

5.2 RESULTS

Fig.5.3 Waveform for delay calculation of proposed Half adder

Measurements have been made of the transition delays of t1, t2, t3, and t4. For instance, t1 represents the time lag between input B's rising edge "0− > 1" and the output Sum's rising edge "0− > 1". When we compare these transition delays with the

existing transition delays of HA design, we find out that the delay of our design has been decreased. The circuit performs and speeds up because of this delay reduction. Below is a comparison of the current half adder design and the suggested HA design's delays:

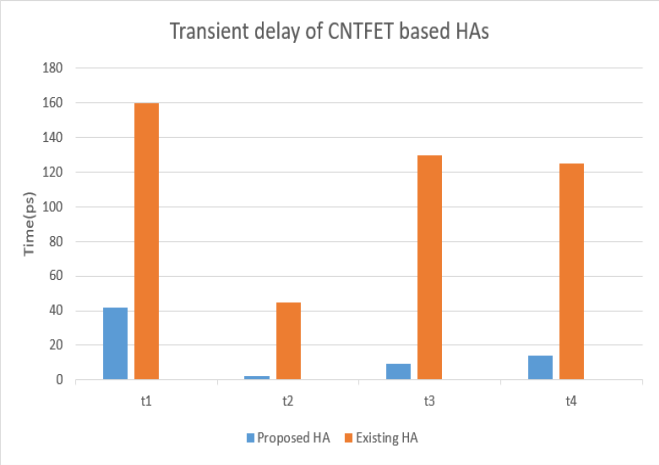


Fig 5.4 Transient delay of CNTFET based HAs.

The average delay of the proposed design is calculated and multiplied by the average power dissipation to get PDP.

Table.5.1 PDP of HAs

Proposed design(J)	Existing design(J) [13]
0.045e-20	0.411e-15

Based on the analysis above, it can be said that the suggested HA design has a lower Power Delay Product (PDP). The GDI approach, which lowers the sub-threshold leakage current, is used in the suggested design to optimize PDP [32]. As a result, the GDI approach speeds up computational logic while reducing power, circuit complexity, and transistor count [10].

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

A CNTFET-based design of a ternary adder based on the GDI technique has been implemented. The existing design is based on a ternary HA design when compared with the proposed design of HA it can be concluded that, this design reduces the chip area, and the circuit becomes faster as the number of transistor requirements is less in GDI-based logic gates.

The achieved result of low PDP can be used further in other digital integrated circuits. The simulation result of proposed design is achieved using Stanford CNTEFT model- Verilog A with 32nm technology using cadence virtuoso with the supply voltage of 0.9V.

Later, this Ternary based adder can be compared with the Quaternary based adder. Quaternary Logic uses four possible values compared to three is Ternary logic. This means that quaternary logic provides more possible combination of values and can therefore represent more complex data and operations. Some of the advantages of quaternary based adder are: Increased data density, Error Correction etc. Due to the increased number of states, quaternary logic can represent more data in smaller space, making it useful in some applications where storage is limited.

Also, quaternary logic offers better error correction capabilities that ternary logic. With four possible states, it can more easily detect and correct errors in data transmissions.

There are some drawbacks also in quaternary logic. A quaternary-based HA requires more logic gates than a ternary HA due to increased number of input states. This results in more complex and larger circuits. Due to increased number of logic gates required, a quaternary based HA may be slower in operation and require more power that ternary based HA.

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