Impact of Variation in High-K Dielectric on Analog and Switching Performance of JL-GAA-SiNW FET

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CANDIDATE'S DECLARATION

We, Kailash Chandra (2K21/MSCPHY/24) and Grace L Haokip (2K21/MSCPHY/57), students MSc(Physics), hereby declare that the project Dissertation titled "**Impact of Variation in High-K Dielectric on Analog and Switching Performance of JL-GAA-SiNW FET**" which is submitted by us to the Department of Applied Physics, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Science , is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I, hereby certify that the project dissertation titled "**Impact of Variation in High-K Dielectric on Analog and Switching Performance of JL-GAA-SiNW FET**", submitted by Kailash Chandra (2K21/MSCPHY/24) and Grace L Haokip (2K21/MSCPHY/57) to the Department of Applied Physics, Delhi Technological University in partial fulfilment of the requirement for the award of of the degree of Master of Science in Applied Physics, is a record of the project work carried out by the student under my supervision. This work has not been submitted partially or completely during any degree or diploma to this university or anywhere else, to the best of my knowledge.

Place : Delhi **Prof. Rishu Chaujar**

Date : May 2023 **SUPERVISOR**

ABSTRACT:

This research paper aims to investigate the impact of changing the dielectric material in the gate stack on the analogue performance of gate-all-around silicon nanowire field-effect transistors (GAA-SiNWFETs). GAA-SiNWFETs have garnered significant attention in the field of nanoelectronics due to their smaller size, high performance, and low power consumption, making them suitable for various future applications, including biosensors.

To conduct a comprehensive analysis, TCAD simulations using the ATLAS-3D device simulator are employed in this study. The simulations are performed at a low drain bias voltage of 0.1V, and Niobium is chosen as the gate electrode material, with a specific work-function value of 4.8eV. By focusing on the analogue parameters such as Id-Vg characteristics, transconductance (Gm), subthreshold swing, device efficiency, switching ratio, and leakage current, the research aims to understand the influence of different dielectric materials, namely SiO2, Al2O3, and HfO2, on the analogue performance of GAA-SiNWFETs. The findings of this study reveal that the choice of dielectric material significantly affects the analogue performance of GAA-SiNWFETs. The Id-Vg characteristics, which represent the drain current as a function of the gate voltage, exhibit variations depending on the dielectric material used in the gate stack. The transconductance, a measure of the device's ability to amplify signals, and the subthreshold swing, which indicates the efficiency of the device in switching between on and off states, are also influenced by the dielectric material. Furthermore, the device efficiency, switching ratio, and leakage current exhibit noticeable changes based on the dielectric material employed. To prevent electron tunnelling and ensure proper device operation, the GAA-SiNWFETs utilize an interface oxide (SiO2) in conjunction with a varied dielectric oxide at the gate. This combination aims to optimize the device performance by maintaining an appropriate balance between electron flow and gate control. The knowledge gained from this research can have significant implications for the development of high-performance analogue circuits in various applications, particularly in the fields of sensor technologies and low-power electronics.

Understanding how different dielectric materials affect the analogue performance of GAA-SiNWFETs is crucial for researchers and engineers involved in the design and optimization of

nanoelectronics devices. By considering the specific requirements and performance trade-offs associated with different dielectric materials, it becomes possible to make informed decisions and achieve improved device functionality, reliability, and energy efficiency. The insights gained from this study contribute to the advancement of emerging technologies, fostering the realization of high-performance analogue circuits that can revolutionize diverse fields of application.

Keywords:Gate-all-around (GAA), Silicon nanowire field-effect transistors (SiNWFET)

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Figure 3.5 - The curve of SS vs gate voltage for JL GAA SiNW FET at V_d=0.4V and channel length 20nm

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 INTRODUCTION

High dielectric constant gate oxides play a crucial role in metal oxide semiconductor transistors (MOSFETs) as they enable effective control of the transistor's behavior by the gate electrode. The dielectric constant, also known as the relative permittivity, determines the ability of the oxide material to store electric charge and affects the gate capacitance of the transistor. By using materials with high dielectric constants, it becomes possible to achieve larger gate capacitance, allowing for improved transistor performance and reduced power consumption.

In recent years, the demand for high-performance transistors with lower power consumption has driven the exploration of alternative gate oxide materials with higher dielectric constants than traditional silicon dioxide (SiO2). These high-k gate dielectrics offer several advantages, including improved transistor scalability, reduced leakage current, enhanced carrier mobility, and increased device reliability. By replacing SiO2 with high-k materials such as hafnium oxide (HfO2), aluminum oxide (Al2O3), or tantalum oxide (Ta2O5), MOSFETs can overcome the limitations imposed by the thickness scaling of SiO2 and achieve further miniaturization while maintaining optimal gate control.

The study of high dielectric constant gate oxides for metal oxide Si transistors focuses on exploring and understanding the properties, fabrication techniques, and performance characteristics of different high-k materials. Researchers investigate the impact of high-k gate dielectrics on transistor parameters such as threshold voltage, subthreshold slope, on/off current ratio, and carrier mobility. Additionally, they analyze the compatibility of these materials with the existing semiconductor fabrication processes, identifying potential challenges and solutions

for integrating high-k gate oxides into practical device structures. By gaining insights into the behavior and performance of high-k gate dielectrics, researchers aim to advance the development of next-generation metal oxide semiconductor devices with improved performance metrics, enabling further progress in areas such as integrated circuits, microelectronics, and nanoelectronics.

Over the past decade, there has been a growing interest in utilizing one-dimensional (1-D) structures such as silicon nanowires (SiNW), nano sheets, and carbon nanotubes (CNT) for point-of-care (POC) biomolecule applications. One of the key advantages of these structures is their ability to achieve high sensitivity, enabling the detection and targeting of biomarkers on surfaces.[1]. SiNWs, in particular, have shown great promise in this field. They possess several desirable characteristics, including compatibility with compact designs, integration into microelectronics, ease of mass fabrication, and the potential for rapid detection. These attributes make SiNWs an attractive choice for POC biomolecule applications. By employing SiNWs in field-effect transistors (FETs), researchers have been able to harness their high sensitivity and leverage their 1-D structure to detect and analyze biomarkers with precision. The FETs constructed using SiNWs exhibit exceptional performance, enabling efficient detection and analysis of biomolecules on surfaces.

The utilization of a high-k dielectric, specifically HfO2, in conjunction with SiO2 offers significant benefits in terms of improving transistor performance while maintaining control over interface characteristics[27]. One of the main advantages of incorporating a high-k dielectric layer is its higher permittivity or dielectric constant compared to SiO2. This high-k dielectric enables the gate oxide layer to be physically thicker while still providing the same level of effective capacitance. By increasing the physical thickness of the gate oxide, the tunneling current through the oxide can be significantly reduced, leading to a reduction in gate leakage current. This reduction in leakage current is crucial for ensuring the efficient operation of transistors and minimizing power consumption. Additionally, the higher permittivity of the high-k dielectric allows for better gate control over the channel region, enabling enhanced transistor performance in terms of subthreshold swing, threshold voltage, and overall device speed. Another key advantage of using a high-k dielectric on top of SiO2 is the ability to tailor the interface characteristics between the dielectric layer and the channel region. The interface

properties play a crucial role in determining the overall device performance, including carrier mobility, threshold voltage stability, and reliability. The introduction of a high-k dielectric layer can help improve the interface quality, reducing interface trap densities and improving carrier mobility, which ultimately enhances the overall transistor performance. Furthermore, the integration of a high-k dielectric material like HfO2 with SiO2 enables better compatibility with modern semiconductor manufacturing processes. It provides a means to overcome the limitations of scaling SiO2 gate oxides, which face challenges in maintaining desirable thickness and controlling gate leakage current as transistor dimensions continue to shrink. The high-k dielectric acts as a suitable replacement for SiO2 in advanced CMOS technologies, allowing for continued transistor scaling while achieving improved device performance. Incorporating a high-k dielectric, such as HfO2, on top of SiO2 offers several advantages in transistor design. It enables improved performance by reducing gate leakage current, enhancing gate control, and optimizing interface characteristics. The utilization of a high-k dielectric layer provides a pathway for achieving higher performance transistors while addressing the challenges associated with scaling traditional SiO2 gate oxides.

The main benefit of utilizing a high-k dielectric (HfO2) on top of SiO2 is to improve transistor performance while controlling interface characteristics. Hafnium dioxide (HfO2) has emerged as a highly suitable candidate for the gate stack material in the CMOS industry. It offers several advantages that make it a preferred choice for integration with silicon nanowires (SiNWs).[2]

One of the key advantages of HfO2 is its compatibility with the CMOS fabrication process. It can be efficiently integrated into wafer production, making it a time-efficient option for manufacturing. Additionally, the use of HfO2 in combination with SiNWs does not incur significant additional costs, making it an economically viable solution.The properties of HfO2, such as its high dielectric constant, make it particularly well-suited for gate stack applications. Its high-k value allows for a thinner gate oxide layer, which in turn enables higher electric fields and improved transistor performance. This leads to enhanced control over the gate electrode and improved device characteristics. Moreover, the integration of HfO2 with SiNWs brings additional benefits to the overall system. The combination takes advantage of the unique properties of SiNWs, such as their 1-D structure and high sensitivity, while leveraging the

favorable characteristics of HfO2 as the gate stack material. This synergistic integration enhances the performance and functionality of the SiNW-based devices.

Hafnium oxide (HfO2/ gate insulator material provides good thermal stability, a high recrystallization temperature and better interface qualities when compared with other gate insulator materials[28].Hafnium oxide (HfO2) as a gate insulator material offers several advantages over other alternatives, making it a favorable choice in advanced semiconductor devices. One key advantage is its excellent thermal stability, which refers to its ability to withstand high temperatures during device fabrication processes without undergoing significant structural or chemical changes. This thermal stability is crucial for maintaining the integrity and functionality of the gate insulator layer during various manufacturing steps. Additionally, HfO2 exhibits a high recrystallization temperature, meaning it can resist crystal structure degradation or phase transformations at elevated temperatures. This property ensures the stability and reliability of the gate insulator material even under harsh operating conditions, preventing performance degradation and enhancing the overall lifespan of the device. Another significant advantage of HfO2 is its superior interface qualities compared to other gate insulator materials. The interface between the gate insulator and the semiconductor channel region plays a critical role in determining the device performance. HfO2 demonstrates good interface quality, which refers to the interaction and compatibility between the gate insulator and the channel material. A high-quality interface reduces interface trap densities and enhances carrier mobility, leading to improved transistor performance in terms of speed, efficiency, and reliability. Furthermore, HfO2 offers a wide bandgap and high dielectric strength, making it highly suitable for achieving effective dielectric isolation in semiconductor devices. Hafnium-based oxides, known for their wide bandgap, high dielectric strength, and excellent thermal stability, have emerged as favorable options for improved dielectric isolation[10]. The wide bandgap ensures that the gate insulator material has a large energy gap between the valence and conduction bands, resulting in reduced leakage currents and enhanced electrical insulation properties. The high dielectric strength allows HfO2 to withstand high electric fields without breakdown, ensuring the reliability and longevity of the device. Overall, HfO2 as a gate insulator material provides good thermal stability, a high recrystallization temperature, and superior interface qualities compared to other alternatives. These properties make it a preferred choice in semiconductor technology, enabling the development of high-performance devices with improved reliability and scalability.

The characteristics of the insulator layers that act as a barrier between the semiconductor channel and the metal gate contacts play a crucial role in maintaining good electrostatics within a transistor. The equivalent oxide thickness (EOT), which represents the effective thickness of these insulator layers, is an important parameter to consider.

The demand for low power consumption in integrated circuits (ICs) has driven significant scaling of transistors over the past few decades [11, 12]. This scaling refers to the continuous reduction in the size of transistors, leading to increased transistor density on a chip. The scaling trend has been guided by Moore's Law, which states that the number of transistors on an IC chip doubles approximately every 18 months. By scaling down the transistor size, the power consumption of the circuits can be reduced while maintaining or improving their performance.

The scaling of transistors involves reducing their dimensions, such as gate length and channel length, which results in several advantages. Firstly, smaller transistors allow for faster switching speeds, enabling higher data processing rates in electronic devices. Secondly, the reduced size leads to a decrease in power consumption since smaller transistors require less energy to switch on and off. Moreover, scaling allows for increased transistor density, enabling the integration of more complex circuits on a single chip.

The continuous scaling of transistors has been made possible through advancements in semiconductor manufacturing techniques and the development of new materials. These advancements have allowed for the fabrication of transistors with smaller feature sizes, improved performance, and reduced power consumption. However, as transistors continue to shrink in size, new challenges arise, such as increased leakage currents and decreased control over device characteristics. These challenges necessitate the exploration of innovative design approaches and materials to maintain or enhance transistor performance while minimizing power consumption. This scaling has been essential in achieving faster switching speeds, higher transistor density, and improved performance. However, it has also presented new challenges that require ongoing research and development efforts to address.

From one perspective, scaling of electronic devices brings about various benefits, including improvements in power consumption, speed, functionality, cost per device, and device density per chip [13,14]. As devices are scaled down to sizes in the range of tens of nanometers, there

are certain undesirable effects that start to emerge in the electrical characteristics of these devices [15-22]. One of the effects is the threshold voltage roll-off, where the threshold voltage, which is the minimum voltage required to activate a transistor, becomes less well-defined as the device dimensions shrink. This can result in variations in device performance and difficulties in achieving precise control over the transistor's switching behavior. Another effect is known as drain-induced barrier lowering (DIBL), which refers to the reduction in the energy barrier between the source and drain regions of a transistor caused by the applied drain voltage. DIBL can lead to leakage currents and subthreshold conduction, affecting the overall performance and power efficiency of the device. Furthermore, as device sizes decrease, the leakage current through the transistor can increase. Leakage currents are unintended currents that flow through the device even when it is supposed to be in the off state. Increased leakage currents contribute to power dissipation and can limit the overall energy efficiency of the device. Additionally, the subthreshold slope, which measures the rate of change of the transistor current with respect to the gate voltage in the subthreshold region, can become less steep as devices are scaled down. A shallower subthreshold slope makes it more challenging to control the device accurately and can impact its performance and power consumption. In summary, while scaling brings numerous advantages to electronic devices, such as improved power consumption, speed, functionality, cost per device, and device density per chip, it also introduces certain undesirable effects. These effects include threshold voltage roll-off, DIBL, increasing leakage current, and subthreshold slope degradation, which can impact the electrical characteristics and performance of scaled-down devices. It is crucial to address these issues through innovative design approaches and materials to mitigate their negative impact and further enhance the performance and efficiency of scaled devices.

According to the International Technology Roadmap for Semiconductors (ITRS), as the gate length of a transistor decreases to 5 nm, the EOT of the insulator layers should be scaled down to 0.5 nm. This reduction in EOT is particularly advantageous for ultrashort nanodevices in both their OFF and ON states. By achieving such tiny EOTs, improvements in gate electrostatic control are anticipated. This improvement allows for a lower subthreshold slope (SS) in the range of 80-90 mV/decade. The subthreshold slope refers to the change in the logarithm of the drain current concerning the gate voltage and is an important factor in determining the energy efficiency of a transistor. Additionally, the increase in gate capacitance (Cg) resulting from the

reduction in EOT leads to an increase in the inverse charge densities in the channel. This, in turn, leads to higher driving currents within the transistor. The increased driving currents contribute to improved performance and functionality of the transistor. These findings, as referenced in sources [4] and [5], emphasize the importance of optimizing the characteristics of insulator layers, particularly their EOT, for achieving better electrostatic control, lower subthreshold slope, and increased driving currents in nanodevices.

Band-to-band tunneling is a phenomenon that plays a significant role in influencing the performance of carbon nanotube field-effect transistors (CNTFETs), particularly when they are operated at low drain voltages. This unique form of tunneling involves the direct transfer of charge carriers across the energy bandgap of the semiconductor material, enabling current flow even in the absence of a traditional source-drain voltage difference. In the context of CNTFETs, the occurrence of band-to-band tunneling introduces new considerations and challenges to the device characteristics that are typically observed in conventional field-effect transistors(FET). The impact of band-to-band tunneling on CNTFETs manifests in various aspects of device performance. Firstly, it alters the overall current-voltage characteristics of the transistor, deviating from the typical behavior observed in devices operating under conventional transport mechanisms. This can result in non-ideal subthreshold slopes, increased leakage current, and modified switching behavior. Furthermore, the presence of band-to-band tunneling introduces additional complexities in terms of device modeling and circuit design, requiring specialized techniques to accurately capture and simulate the behavior of these devices. Operating CNTFETs at low drain voltages exacerbates the influence of band-to-band tunneling on device performance. At these voltage regimes, the contribution of tunneling currents becomes more pronounced, and their effects on device operation become more apparent. As a result, conventional device characteristics, which are primarily defined by the operation under higher voltage regimes, may not hold true for CNTFETs when they are subjected to low drain voltages. The understanding of the impact of band-to-band tunneling in CNTFETs is crucial for optimizing their performance and advancing their applications. Researchers and engineers in the field strive to develop novel device architectures, material engineering strategies, and circuit design techniques that can mitigate the undesirable effects of tunneling currents and enhance the overall performance of CNTFETs. By addressing these challenges, it becomes possible to harness the unique properties of carbon nanotubes and leverage their potential for future

nanoelectronic devices and technologies. The band-to-band tunneling significantly impacts the performance of carbon nanotube field-effect transistors (CNTFETs) when operated at low drain voltages and challenging conventional device characteristics[9].

1.2 CMOS Technology: Developments and Challenges

In 1965, Gordon E. Moore introduced a law in which he states the number of transistors that we placed on IC or silicon chip becomes double approximately in every two years. This observation is known as Moore's Law[1]. Silicon nanowire transistors have gained attention due to their potential for high performance and precise control over device current. Scaling the gate insulator, along with other device metrics, has been considered effective to enhance transistor performance in complementary metal oxide semiconductor (CMOS) technologies. This approach aligns with Moore's Law, which predicts the doubling of transistors on an integrated circuit (IC) chip every eighteen months while reducing power consumption. The implementation of high-k and metal materials has been recognized as a significant advancement in transistor technology, allowing increased transistor density, enhanced device performance, and improved circuit functionality without escalating production costs. However, as feature sizes shrink below 45 nm, the reduction in silicon dioxide gate dielectric thickness reaches its physical limit, resulting in high gate leakage currents due to direct tunneling[10]

According to the data presented in the figure, the growth rates of transistor counts in various integrated circuit (IC) products have exhibited notable trends over the past 10-15 years. For instance, the transistor counts in dynamic random-access memory (DRAM) experienced a rapid increase, with an average growth rate of approximately 45% per year until the early 2000s. However, this growth rate subsequently decreased to around 20% through the emergence of the 16-gigabit (16Gb) generation in 2016 [30]. In the case of 2D planar NAND flash memory, which represents the highest density achievable on a single die as of January 2020, the maximum density reached 128 gigabits (128Gb). Meanwhile, 3D NAND technology, which utilizes multiple layers of memory cells, has achieved even higher densities. Presently, the maximum density for a 3D NAND chip stands at 1.33 terabits (1.33Tb) for a 96-layer quad-level-cell (QLC) device. It is anticipated that the combination of QLC technology and advancements in 96-

layer fabrication will enable 3D NAND to achieve a density of 1.5Tb in 2020. Furthermore, the introduction of 128-layer technology is expected to pave the way for the production of 2-terabit (2Tb) chips. These observations indicate the continuous progression in transistor counts and memory densities within the semiconductor industry. Advancements in technology have allowed for significant increases in memory capacity, enabling the development of more powerful and higher-density IC products.

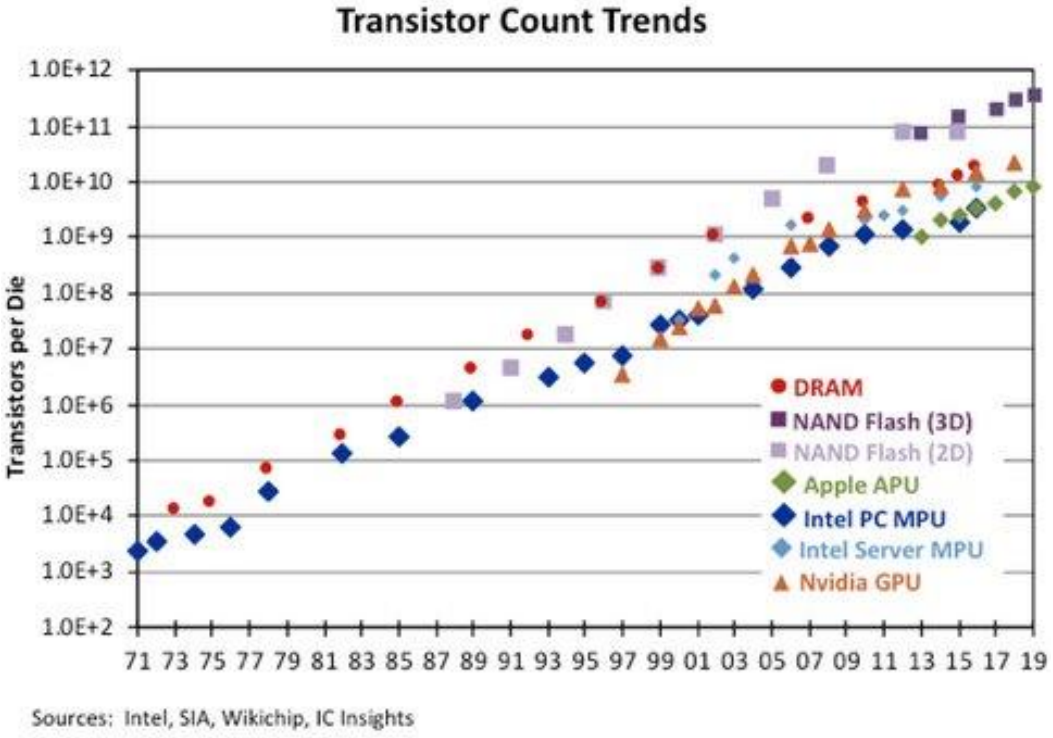


Figure 1.1- Intel's Microprocessor transistor count

Transistor counts in Intel's PC microprocessors grew approximately 40% per year through 2010, but the rate dropped to half that in the years following. The growth of transistor counts for the server microprocessors (MPUs) produced by the company experienced a temporary pause during the mid- to late-2000s. However, it resumed an upward trajectory thereafter, with an average annual growth rate of approximately 25%. It is worth noting that Intel, the company in focus, ceased disclosing specific details regarding transistor counts starting from the year 2017[31].

Consequently, the precise transistor count figures for Intel's server MPUs beyond that point are no longer publicly available.

In recent years, there has been significant tremendous research interest in exploring high-N gate dielectrics as potential alternatives to SiO2 in advanced CMOS technologies. Therefore an extensive efforts have been devoted to investigating the properties and performance of these dielectric materials [48-50]. The rapid growth of the information technology industry has driven significant advancements in silicon microelectronics over the past couple of decades. These advancements have resulted in the development of highly efficient microprocessors tailored for high-performance applications such as CPUs, gaming chips, and servers, as well as low-power devices like handheld mobile phones. The key component in these microprocessors is the metal oxide semiconductor field effect transistor (MOSFET), which serves as the fundamental solid-state element. MOSFETs can be categorized as either nFETs (electrons as majority carriers) or pFETs (holes as majority carriers) and this combine to form MOS (CMOS) logic. At the heart of the MOSFET lies the gate oxide, traditionally composed of silicon dioxide or silicon oxynitride (SiO(N)), which plays a critical role in device performance and scaling. The thickness and quality of the gate oxide are of paramount importance in determining the overall performance characteristics of the MOSFET[32]. Significant progress in CMOS technology has spurred the rapid and aggressive scaling of the MOSFET gate stack. This scaling approach aims to achieve higher device density and improved performance. By reducing the dimensions of the MOSFET gate stack, advancements have been made in packing more transistors onto a single chip, leading to increased device density. Additionally, scaling enables enhancements in device performance, such as faster switching speeds and reduced power consumption. These advancements in CMOS technology have paved the way for the development of more advanced and powerful electronic devices. Conventional poly-Si/SiO2 gate stack is approaching some practical limits, e.g. the gate oxide thickness has ceased scaling starting from 90nm node, because the gate leakage current due to tunneling and oxide breakdown is already quite high at its thickness of ~1.2 nm [32], in which it does not encourage its further reduction in physical thickness and thereafter the advanced gate stacks that involves metal gate materials and a high-k dielectrics are may be in need to introduced into IC 2 industry and also in some novel process integration technologies. But there are however immense challenges that arise in material engineering and process

integration of the advanced gate stack. Thus, over the past decade most of the attention has been drawn by both academic and industrial research and development (R & D) communities [33-34].

Due to its higher permittivity, the high-k dielectrics provides two primary advantages over conventional SiO(N) dielectrics. Firstly, the high-k dielectrics can be grown thicker physically while maintaining a similar Equivalent Oxide Thickness (EOT) as SiO2, thus it offers a significant gate leakage reduction [33–34] and thus making these materials that is suitable for low-power applications. Secondly, the high-k dielectrics have the potential to produce significantly a lower EOT values than is possible with conventional SiON dielectrics, thereby this can re-enable transistor scaling and also the use of lower gate voltages respectively. The characteristics of the insulator layers which act as a barrier between the semiconductor channel and the metal gate contacts signifies a crucial role inoder to maintain an excellent electrostatics within a transistor. The equivalent oxide thickness (EOT), which represents the effective thickness of these insulator layers, is an important parameter to consider[10]. At the beginning in the late 1990s, there was an emmense worldwide effort to search for an appropraite solution related to high-k dielectric for process of integration into CMOS technology. Even thogh the Hf-based high-k materials has emerged as the dielectric of choice in 2001–2002 [35–40], numerous incompatibilities with conventional CMOS processes delayed their introduction. However, due to recent materials and process an innovations has paved the way for this technology to evolved as a product reality which is an evidenced by the high-performance 45 nm [41, 42, 44] and low-power 32 nm [43] high-k/metal gate technology results. In pursuit of further performance enhancement, the semiconductor industry is increasingly exploring high-mobility substrates like Ge and III-V materials for CMOS technologies. This interest stems from recent advancements in high-k metal gate technology. By incorporating these high-mobility substrates into CMOS devices, there is a potential to achieve significant improvements in device performance, such as enhanced carrier mobility and faster transistor switching speeds. The utilization of high-k metal gate technology in conjunction with high-mobility substrates presents an exciting opportunity to push the boundaries of CMOS technology and unlock new possibilities for advanced electronic devices.

As technological nodes, gate lengths, and oxide thicknesses have shrunk, Short Channel Effects (SCEs) and gate leakage current have become significant challenges in semiconductor scaling.

To address these non-ideal effects and enable continued scaling, the semiconductor industry has introduced various modifications to the traditional Si-based MOSFET structure[45]. One prominent SCE is the Hot Carrier Effect, also known as Impact Ionization, which occurs in n-MOSFETs with shorter channel lengths[46]. The enhanced lateral electric fields in these devices cause carrier electrons to gain higher energy, leading to the generation of electron-hole pairs and potential damage to the gate oxide material. To mitigate this effect, physical separation between the channel and substrate, along with the use of thick high-oxide layers, is employed[47]. Gate Oxide Breakdown is the other concern that is associated with aggressive transistors scaling. As the gate oxide thickness decreases with each transistor generation, electrostatic breakdown becomes more likely, posing a threat to device reliability. The adoption of thick high-gate oxides helps address this issue while maintaining the required gate capacitance for scaling. Additionally, thicker gate oxides reduce gate leakage current by minimizing Quantum Mechanical tunneling at the channel-oxide interface. These measures contribute to enhancing device performance, reducing non-ideal effects, and ensuring the reliability of scaled transistors. During the past several decades, silicon-based microelectronics devices have infiltrated practically every aspect of our daily life. This has been accomplished by continuously achieving the characteristics of faster speed, higher density, and lower power for the individual devices, namely, the Metal Oxide Semiconductor Field Effect Transistors – MOSFETs. Therefore, “scaling”, which is the reduction in individual device size, became the focus of engineers over the past forty years. The scaling behavior has followed the well-known Moore’s law, which predicts that the number of devices on an integrated circuit increases exponentially, doubling over a 1.5–2 year period [67].

1.2 History Of Transistor

A transistor is a semiconductor device that has at least three terminals for the connection to an electric circuit. The third terminal controls the flow of current between the other two terminals in the common case. The first transistor was successfully demonstrated in the year 1947, December 23, at Bell Laboratories in Murray Hill, New Jersey. William Shockley, John Bardeen and Walter Brattain were the three individuals credited with the invention of the transistor. *bipolar junction transistor* (BJT) and *field-effect transistor* (FET)[51] are the types of transistors.

The field-effect transistor, based on the principle proposed by Julius Edgar Lilienfeld in 1925, saw its first working implementation in 1947 with the invention of the point-contact transistor by John Bardeen, Walter Brattain, and William Shockley at Bell Labs. Shockley further advanced the technology by introducing the bipolar junction transistor in 1948, leading to its widespread use in the early 1950s and marking a significant milestone in transistor development. Then in 1951 there became a sudden big innovation in transistor when Willian Shockley developed a junction transistor. Further with time more growth happened in sector of transistor developed Planer Transistors. In 1958 Silicon Transistors became replacement of Germanium as it was getting broken at high temperature which worked just like a germanium junction transistor. In 1959, Mohamed Atalla and Dawon Kahng, also at Bell Labs, invented the MOSFET (metal-oxide-semiconductor field-effect transistor), which revolutionized the industry. MOSFETs offered improved power efficiency, leading to their mass production and widespread adoption in various applications. These are not like sandwich but have a channel of either N or P type semiconductor running through a ridge on top of the other type. MOSFETs were not originally better than the junction transistor, but they are much easier to make on a integrated circuit or microprocessor, and so they soon became the preferred type of transistor. Today, the MOSFET stands as the most extensively manufactured device in history, solidifying its pivotal role in modern electronics.

1.3 Metal-oxide-semiconductor field effect transistor (MOSFET)

The fundamental MOS transistors featured a metal gate material, silicon dioxide as the insulator, and a semiconductor substrate, giving rise to the name MOS (Metal Oxide Semiconductor) transistor. On the other hand, the term FET (Field Effect Transistor) originates from the mechanism by which the gate is switched on and off through the application of an electric field across the gate oxide. In this transistor configuration, two regions are biased at varying potentials, with the lower potential region serving as the source and the higher potential region acting as the drain. The operation of the MOSFET is based on the principle of the field effect, where the electric field applied to the gate terminal controls the flow of current through the channel between the source and drain regions. By applying a voltage to the gate, the electric field

modulates the conductivity of the channel, allowing for precise control of the transistor's behavior.

The use of silicon dioxide as the gate insulator in early MOS transistors provided reliable isolation between the gate and the channel. This enabled efficient switching and low power consumption. Over time, advancements in semiconductor technology led to the introduction of alternative gate dielectric materials with higher dielectric constants, known as high-k dielectrics. These materials offer improved gate control and reduced leakage current, enabling further performance enhancements in MOSFETs. The MOSFET's ability to operate at lower power levels compared to other transistor technologies, coupled with its scalability and compatibility with integrated circuit fabrication processes, has made it the most widely manufactured device in history. It has revolutionized various industries, including electronics, telecommunications, and computing, by enabling the development of smaller, faster, and more efficient electronic devices. Overall, the combination of metal gate, oxide insulator, and semiconductor substrate in the MOSFET architecture, along with its field-effect operation, has paved the way for the advancement and widespread adoption of modern transistor technology.

MOS transistor is a four terminal device and they are classified as drain, gate, source, body [53]. According to the position of contact electrodes, the FETs are classified into four basic structures namely staggered top gate, staggered bottom gate, coplanar top gate, and coplanar bottom gate as shown in in figure 1.2.

The integration of high dielectric constant (high-k) materials as gate oxides in metal oxide silicon transistors offers potential improvements in gate capacitance, leakage current reduction, carrier mobility, and overall device performance[8]. Challenges include compatibility with fabrication processes, interface quality, and oxide layer defects. Ongoing research focuses on optimizing high-k gate oxides for reliability, thermal stability, and interface quality. Advancements in integrated circuits and microelectronics have been achieved with high-k gate oxides, driving progress in nanoelectronics and semiconductor technology.

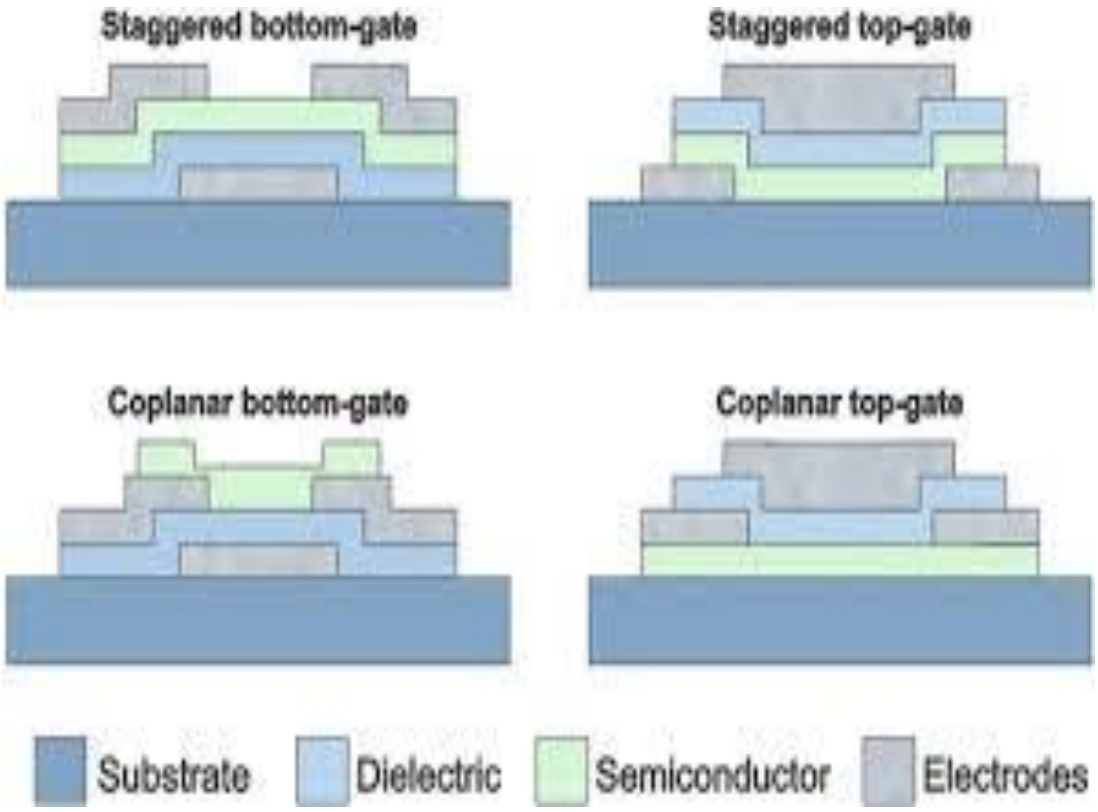


Figure 1.2 – Types of gates

In all the structures given above, it is clear that the semiconductor is placed between the source and drain electrode and the dielectric layer is sandwiched between the gate electrode and the semiconducting layer. Figure 1.3 illustrates the design of a MOSFET, a key component in Very Large Scale Integration (VLI) systems. Researchers in the field are actively focused on reducing the size of transistors to enhance their efficiency [54]. In today's semiconductor and microprocessor industry, there is a growing trend towards employing numerous nano-scaled transistors that offer low power consumption and cost-effective designs. However, scaling down devices to the nanoscale introduces challenges such as Short Channel Effects (SCEs), tunnelling effects, and threshold voltage variations, which can hinder efficiency and complicate manufacturing processes. This review article not only addresses the problems and potential solutions related to scaling, but also provides a comprehensive analysis of silicon nanowire transistors and other novel nano Field-Effect Transistors (FETs) [55]. By examining these unique nano FETs, this review aims to shed light on the advancements and potential breakthroughs in the field of transistor technology.

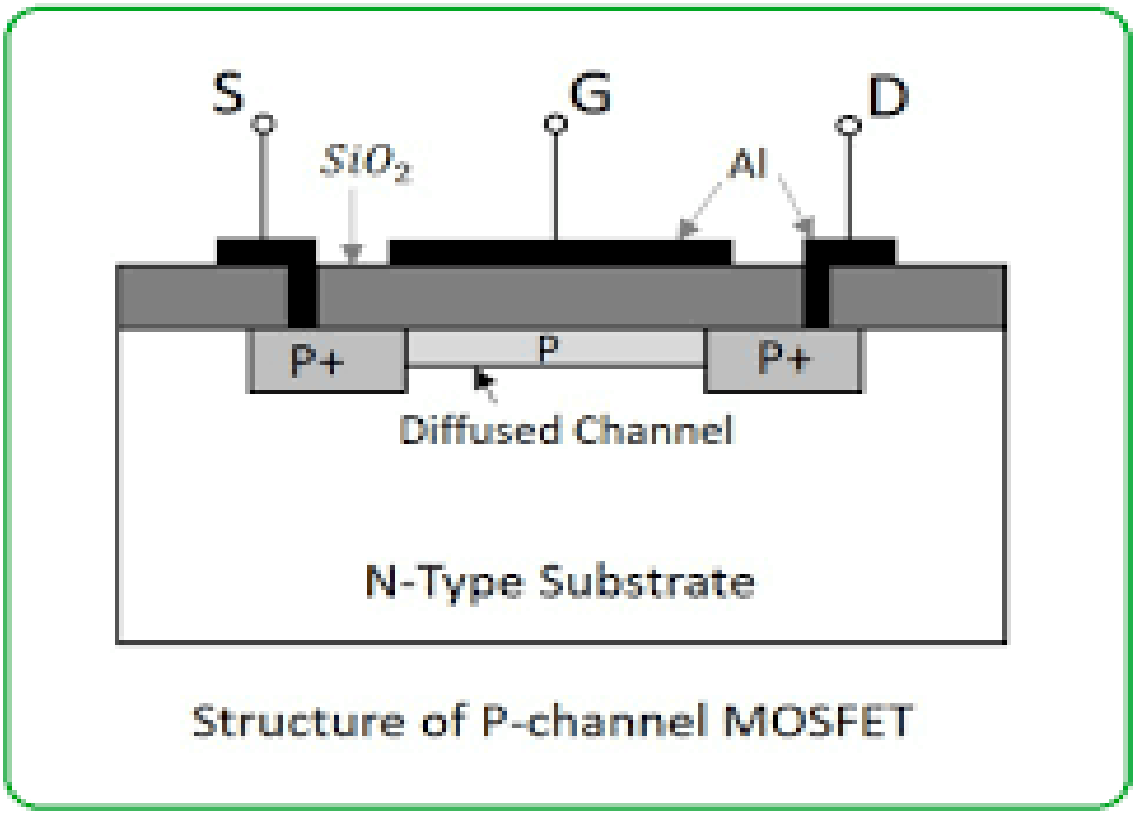


Figure 1.3. N-MOS structure [56]

1.4.1 MOSFET operation

The MOSFET, a type of encapsulated transistor, is produced through controlled oxidation processes, typically using silicon as the semiconductor material. When a voltage is applied, it induces charges on the metal plates, similar to a parallel plate capacitor, and generates counter charges in the interfacial layer of the semiconductor, as expected and anticipated [57]. This phenomenon is known as the capacitive coupling effect and forms the basis of the operation of a MOSFET. By manipulating the voltage applied to the metal gate, the charges in the semiconductor layer can be modulated, allowing for precise control of the transistor's conductivity. The controlled oxidation process ensures the formation of a thin insulating layer, typically silicon dioxide, between the metal gate and the semiconductor, preventing direct electrical contact. This insulating layer acts as a barrier, enabling the transistor to switch on and off by varying the voltage on the gate terminal. The ability to control the flow of current through

the transistor makes the MOSFET a vital component in modern electronic devices and integrated circuits, offering high performance, low power consumption, and compact size.

The primary objective of a MOSFET is to exert control over the voltage and current flow between the source and drain terminals. It achieves this through the operation of a MOS capacitor, which functions as a switch. Located beneath the oxide layer on the semiconductor surface, between the source and drain terminals, the semiconductor can undergo inversion from p-type to n-type when a positive or negative gate voltage is applied. When a positive gate voltage is applied, the holes beneath the oxide layer experience repulsive forces and are pushed downwards towards the substrate. This results in the formation of a depletion region, populated by bound negative charges associated with acceptor atoms, allowing electrons to reach the channel. Additionally, the positive voltage attracts electrons from the n+ source and drain regions into the channel. With a voltage applied between the source and drain, current can flow freely, and the electrons within the channel are controlled by the gate. On the other hand, if a negative voltage is applied, a hole channel forms under the oxide layer instead of a positive voltage[53]. This alternative configuration allows for the modulation of current flow in a different manner. By manipulating the gate voltage, the MOSFET can effectively switch between different operating modes, enabling precise control over the flow of current and voltage between the source and drain terminals. This characteristic makes MOSFETs an essential component in various electronic devices and systems. The primary capability of the MOSFET is to generate and change a conducting layer comprised of minority carriers at the semiconductor–oxide interface [57]. When $V_g>0$ is applied, holes begin to move away from the common region because a p-type substrate is employed in n-MOS transistors [53]. The depletion layer penetrates the substrate deeper, and electrons begin to inject, producing a pathway when the gate voltage is increased higher. For an n-type substrate, the channel created by a p-MOS transistor is made up of holes. MOSFETs are classified into two categories based on how they operate [58**].**

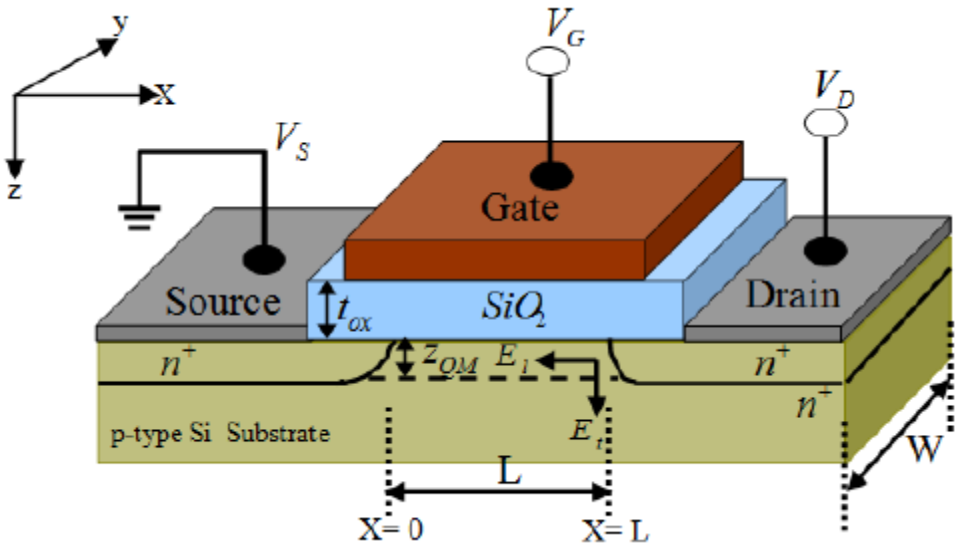


Figure 1.4 - Basic structure of an n-channel MOSFET with electrons removed from the Si/SiO 2 interface due to the quantum-confinement effect.

1.4.2 Enhancement mode

In enhancement mode, the absence of a gate voltage results in no conducting channel between the metal regions, rendering the MOSFET in an "off" state. To initiate the conducting channel and activate the MOSFET, a minimum gate voltage, known as the threshold voltage, must be applied [59]. This gate voltage induces the formation of a conducting channel, allowing current to flow between the source and drain terminals and enabling the desired functionality of the MOSFET in electronic circuits and devices.

1.4.3 Depletion mode

The depletion-mode MOSFET operates differently from the enhancement-mode MOSFET in terms of the presence of a conducting channel. Even without a gate voltage, the depletion-mode MOSFET already possesses a conducting channel (inversion layer). The threshold voltage plays a crucial role in controlling the device's operation, allowing it to be turned off when the applied

gate voltage exceeds the threshold voltage [59]. This behavior enables the depletion-mode MOSFET to serve as a switch or amplifier in various electronic applications.

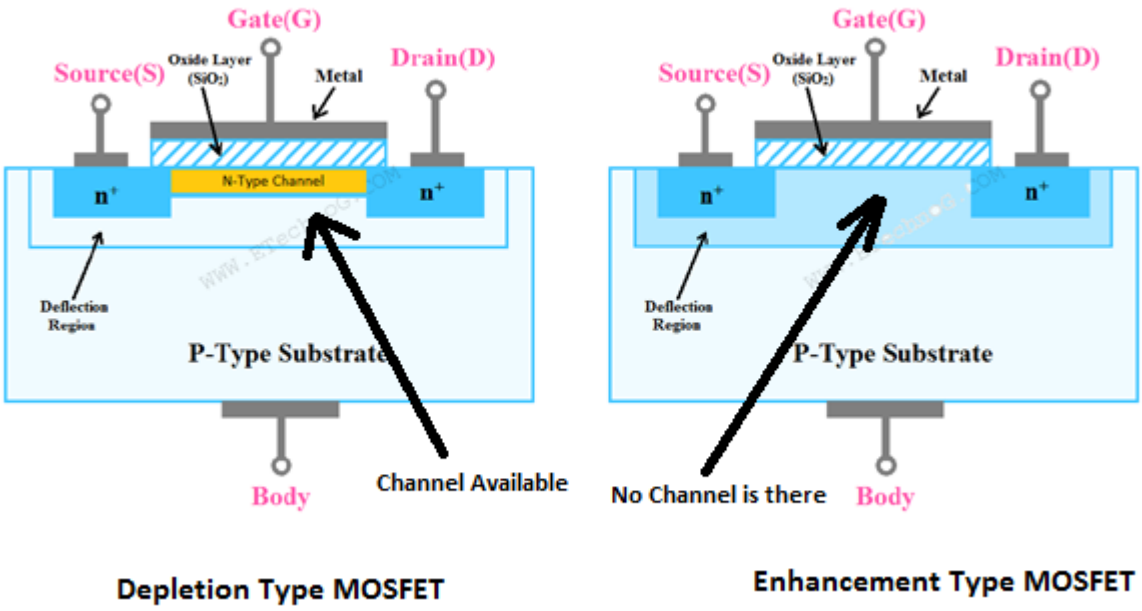


Figure 1.5- Types of MOSFET

1.5 Disadvantages and limitations of conventional MOSFET

Conventional bulk metal-on-silicon (MOS) devices are commonly used in large-scale integrated circuits. However, due to their reduced size, they are not ideal for the small-channel applications. Due to the presence of both gatedrain and gate-source overlap, the device's longitudinal field is increased [61]. The channel length of a MOSFET significantly influences its performance characteristics. Short channel devices offer advantages such as improved processing speed, lower operating potential, and higher transistor density. However, they may also exhibit drawbacks including poor frequency response, limited linearity, and susceptibility to damage from static electricity. These considerations should be taken into account when designing and utilizing FET-based circuits [62][53].

1.5.1 Short channel effect

the control of electrostatics in MOSFETs varies depending on the channel length. Long channel MOSFETs rely on the gate electrode for regulating the channel, while short channel MOSFETs involve the active participation of the source and drain regions. The reduction in channel size in short channel devices results in increased drain current and a lower threshold voltage, which can impact the switching behavior and energy efficiency of the MOSFET [53].

1.5.2 Velocity saturation

In a short channel device, the lateral electric field experiences significant growth, leading to the saturation of charge carrier velocity at approximately 10^7 cm/sec. This saturation effect has implications for the device current, which tends to be smaller than the drain current predicted by the mobility model [62].Due to the increased lateral electric field in short channel devices, the mobility of the charge carriers reaches a saturation point. Beyond this point, the velocity of the carriers no longer increases linearly with the applied electric field. Consequently, the device current achieved in practice is lower than what would be expected based on the mobility model, which assumes a linear relationship between carrier velocity and electric field.

The saturation of charge carrier velocity at around 10^7 cm/sec in short channel devices is an important consideration in their performance analysis. It influences the actual current flow and should be taken into account when predicting the device behavior and optimizing circuit designs [62].

1.5.4 Surface scattering

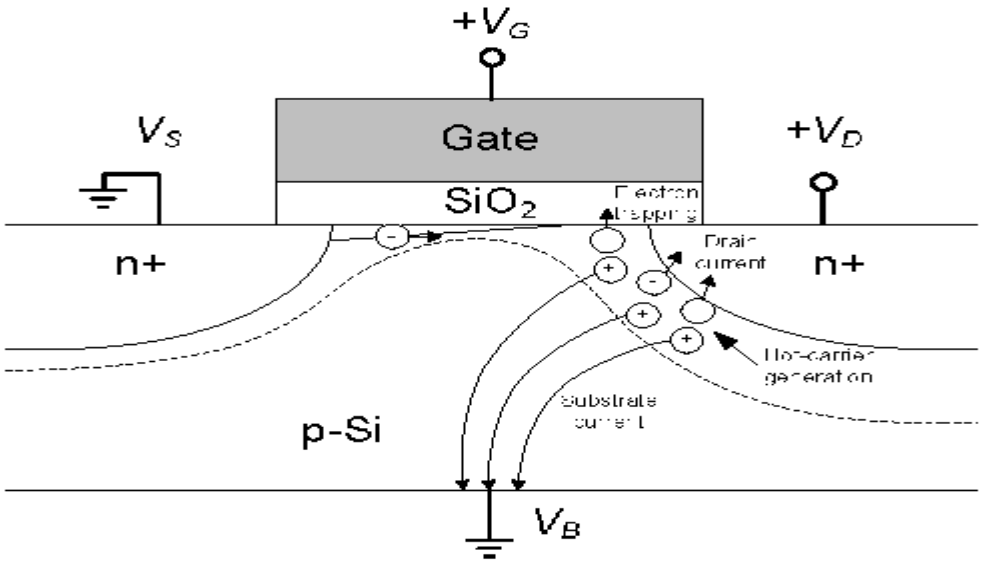
In short channel MOSFETs, the inversion layer that forms in the device is confined to a narrow region near the silicon-insulator interface. As the lateral electric field intensifies within the channel and the vertical electric field is applied, the charge carriers undergo acceleration towards the drain region. However, this acceleration also leads to collision events among the charge

carriers, resulting in a degradation of their mobility. This phenomenon is commonly referred to as surface scattering.

Surface scattering in short channel MOSFETs has a significant impact on the device's performance. It causes a reduction in the drain current compared to what would be expected based solely on the mobility of the charge carriers. The collisions between charge carriers during their journey from the source to the drain hinder their overall mobility and affect the efficiency of the device [63]. Understanding and mitigating the effects of surface scattering is crucial in the design and optimization of short channel MOSFETs. By addressing this phenomenon, researchers and engineers can work towards improving the performance and efficiency of these devices in practical applications.

1.5.5 Hot carrier effects

In short channel devices, the electric field strength within the channel regions increases, resulting in the carriers moving at high velocities. The high kinetic energy acquired by the carriers in this process can give rise to a phenomenon known as impact ionization. Impact ionization can cause degradation of the insulator layer, leading to gate leakage current. The carriers responsible for this phenomenon are referred to as hot carriers. The presence of hot carriers in short channel devices can have several undesirable effects. One such effect is the generation of substrate current, which refers to the flow of current through the substrate material. This substrate current can impact the overall performance and reliability of the device [64].Understanding and managing the effects of hot carriers is crucial in the design and optimization of short channel devices. Researchers and engineers strive to develop strategies to mitigate the impact of hot carriers, such as incorporating suitable materials and structures that can handle the high energy carriers more effectively and minimize the associated degradation and leakage currents.



igure 1. Hot-carrier generation and components in NMOSFETs

Figure 1.6 – Represenation of Hot Carriers Effect

1.6 Gate-All-Around (GAA)

By employing a large number of gate transistors, the adverse effects of small channels are significantly mitigated, resulting in improved performance. In the case of silicon Nanowire transistors, the Nanowire itself serves as the substrate [65]. Nanowires exhibit various device shapes, such as rectangular and cylindrical configurations. Depending on the specific shape of the nanowires, the transistors can be fabricated as either cylindrical gate structures or gate-all-around structures [66]. The utilization of Nanowires in transistor design offers several advantages. The cylindrical or gate-all-around structures enable better control over the channel region, facilitating enhanced electrostatics and reduced leakage currents. Moreover, the compact size of Nanowire transistors allows for higher transistor density on a chip, enabling the integration of more functionalities and improved overall performance in electronic devices. The development and optimization of Nanowire-based transistor technologies continue to be an area of active research and innovation in the field of semiconductor devices.

1.6.1 Gate All Around Field-Effect Transistors (GAA-FETs)

Recently, there has been significant research interest in the development of Gate-All-Around Field-Effect Transistors (GAA-FETs) and these transistors have a unique structure where the gate region completely wraps around the channel, offering distinct advantages over traditional transistor designs[23,24]. This innovative configuration allows for improved control over the flow of current through the channel, resulting in enhanced device performance. By enclosing the channel region with the gate material, GAA-FETs provide better electrostatic control, minimizing leakage currents and improving the transistor's ability to switch on and off. This enhanced control over the channel allows for higher device efficiency, reduced power consumption, and improved overall performance. Furthermore, the GAA-FET architecture offers scalability advantages. As device dimensions continue to shrink, GAA-FETs have shown promise in maintaining their performance characteristics due to the improved electrostatic control provided by the fully wrapped gate structure. This scalability is crucial in enabling the continued advancement of integrated circuits, as it allows for the realization of smaller, faster, and more power-efficient electronic devices. The research and development efforts focused on GAA-FETs have explored various materials and fabrication techniques to optimize their performance. By investigating novel gate materials, dielectrics, and channel materials, researchers aim to further enhance the transistor's functionality, reduce power consumption, and improve reliability. This unique configuration of GAA-FETs with a fully wrapped gate structure represents a significant advancement in transistor design and offers improved electrostatic control, scalability, and performance characteristics, making GAA-FETs a promising candidate for future nanoelectronic devices. Continued research in this field will undoubtedly lead to further advancements in device performance, enabling the realization of smaller, more efficient, and high-performing electronic systems.

GAA-FETs are expected of promising candidates for future scaling technology nodes and short channel resistance compared to other gate structures such as omega gate, double gate, and single gate, the GAA-FETs offer distinct advantages in terms of mitigating short channel resistance[25,26]. One of the key challenges in transistor scaling is the increase in short channel effects, which can degrade device performance. GAA-FETs address this challenge by utilizing a fully wrapped gate structure that surrounds the channel region from all sides. This unique

architecture provides superior electrostatic control over the channel, effectively minimizing short channel effects. Compared to other gate structures like omega gate, double gate, and single gate, GAA-FETs demonstrate enhanced performance characteristics in terms of reducing short channel resistance. This attribute is crucial in achieving high-speed operation and maintaining device reliability as device dimensions continue to shrink. The comprehensive wrapping of the gate around the channel in GAA-FETs ensures improved gate control, reduced leakage currents, and enhanced switching characteristics. These advantages make GAA-FETs well-suited for future scaling technology nodes where maintaining device performance in the face of shrinking channel lengths is of utmost importance. Research and development efforts focused on GAA-FETs continue to explore innovative materials, fabrication techniques, and optimization strategies to further enhance their scaling capabilities. By improving short channel resistance and overall device performance, GAA-FETs hold great potential for enabling the realization of advanced and highly efficient electronic systems in the future. GAA-FETs exhibit promising characteristics as candidates for future scaling technology nodes. Their ability to mitigate short channel resistance sets them apart from other gate structures, making them a compelling choice for achieving high-performance, low-power, and highly scalable transistor designs. Continued research and advancements in GAA-FET technology will further solidify their position as a leading contender in the field of nanoelectronics.

Despite their promising advantages, GAA-FETs are not without drawbacks and thus two significant challenges are associated with GAA-FETs which are high leakage current and subthreshold slope, which can limit their suitability for low-power applications and steep switching requirements[25]. Leakage current refers to the undesired flow of current in a transistor when it is in the off-state. In the case of GAA-FETs, the high leakage current can be attributed to various factors, such as tunneling currents across the gate dielectric and surface defects in the channel region. This increased leakage current can result in excessive power dissipation and compromise the overall energy efficiency of the device, making GAA-FETs less desirable for low-power applications where minimizing power consumption is crucial. Subthreshold slope, on the other hand, is a measure of how steeply the transistor turns on as the gate voltage increases. Ideally, a transistor should exhibit a sharp transition from the off-state to the on-state, allowing for efficient switching operations. However, in GAA-FETs, achieving a low subthreshold slope can be challenging due to the increased gate coupling and reduced gate

control in the fully wrapped gate structure. A higher subthreshold slope indicates a less efficient switching behavior, leading to increased power consumption and reduced overall performance in applications that require fast and precise switching operations. The limitations of high leakage current and subthreshold slope in GAA-FETs pose challenges for their suitability in certain applications. Low-power applications, where minimizing power consumption is critical, may require alternative transistor designs that offer lower leakage currents and better energy efficiency. Similarly, applications that demand steep switching characteristics may benefit from alternative transistor structures that can provide sharper transitions and improved subthreshold slopes. Researchers and engineers are actively addressing these challenges through various approaches. Strategies to reduce leakage current in GAA-FETs involve optimizing the gate dielectric materials, interface engineering, and minimizing surface defects in the channel region. Improving the subthreshold slope requires advancements in gate engineering, such as novel gate materials and optimization of the gate dielectric thickness. By addressing the issues of high leakage current and subthreshold slope, GAA-FETs can become more suitable for a wider range of applications, including low-power and steep-switching scenarios. Ongoing research and development efforts are focused on optimizing GAA-FET designs and exploring innovative solutions to overcome these limitations, ultimately enhancing their performance and expanding their applicability in various electronic systems.

1.6.2 Gate-All-Around Silicon Nanowire Field-Effect Transistor (GAA-SiNWFET)

In a Gate-All-Around Silicon Nanowire Field-Effect Transistor (GAA-SiNWFET), the high-k dielectric serves the purpose of isolating the gate from the channel. However, any variation in the high-k dielectric can give rise to several issues that impact the performance of the transistor. Firstly, variations in the high-k dielectric can result in a reduced transconductance. This reduction occurs due to a decrease in the effective gate capacitance, which directly affects the ability of the transistor to amplify the input signal. Secondly, there is the possibility of an increased off-leakage current. When the high-k dielectric varies, it can lead to higher leakage currents flowing through the transistor when it is supposed to be in the off-state. This leakage

current can adversely affect the overall power efficiency of the device. Another consequence of high-k dielectric variation is a decrease in the switching speed of the transistor. The switching speed refers to how quickly the transistor can transition between its on and off states. If the high-k dielectric is not uniform, it can impede the efficient and rapid switching of the transistor. Furthermore, variation in the high-k dielectric can contribute to increased crosstalk between neighboring transistors. Crosstalk refers to the unwanted coupling or interference between adjacent transistors, which can negatively impact their performance and introduce noise into the system.

Gate-All-Around Silicon Nanowire Field-Effect Transistors (JL-GAA-SiNWFETs) hold significant promise for future high-performance and low-power electronics.[2] When compared to other transistor designs such as GAA-MOSFETs and bulk MOSFETs, JL-GAA-SiNWFETs exhibit improved sensitivity. They offer advantages like a larger effective channel width, reduced short-channel effects, and enhanced scalability. However, it's important to note that the choice of dielectric material greatly influences the performance of JL-GAA-SiNWFETs. Any variations in the high-k dielectric can introduce challenges, as discussed earlier, and must be carefully addressed to optimize the transistor's functionality and ensure reliable operation. High-k dielectrics have emerged as a potential solution to enhance the performance of JL-GAA-SiNWFETs (Gate-All-Around Silicon Nanowire Field-Effect Transistors). These high-k dielectrics offer distinct advantages over traditional SiO2 (silicon dioxide) dielectrics, thereby addressing certain limitations. One key advantage of high-k dielectrics is their higher dielectric constant compared to SiO2. The dielectric constant, also known as the relative permittivity, measures the ability of a material to store electrical energy. With a higher dielectric constant, high-k dielectrics enable a thinner gate oxide layer to be used in the transistor structure. This reduction in oxide thickness allows for better electrostatic control of the device, leading to improved performance. Additionally, the higher dielectric constant of high-k materials facilitates a higher electric field across the gate oxide. This increased electric field enhances the transistor's ability to control the flow of current through the channel, resulting in enhanced device characteristics, such as improved carrier mobility and subthreshold behavior. Another significant advantage of high-k dielectrics is their lower leakage current. Leakage current refers to the undesired flow of current through the gate oxide when the transistor is in the off-state. By employing high-k dielectrics, the leakage current can be minimized due to their lower leakage

properties, which contribute to higher power efficiency and reduced energy consumption. The utilization of high-k dielectrics in JL-GAA-SiNWFETs presents an opportunity to overcome the limitations associated with SiO2 dielectrics. The superior properties of high-k dielectrics, including their higher dielectric constant, thinner gate oxide, higher electric field, and lower leakage current, collectively contribute to enhanced transistor performance, improved power efficiency, and better overall device characteristics. These findings from various studies and research papers [6], [7] underscore the potential of high-k dielectrics as a viable approach to optimize the performance of JL-GAA-SiNWFETs and pave the way for advancements in high-performance nanoelectronic devices.

1.7 The Rationale for Selecting Silicon Nanowire

Silicon CMOS is perhaps the nanoelectronics industry's favored technology since several decades. Because of their exceptional high qualities, MOSFETs have evolved into one of the most important phenomenon components of VLSI. A MOSFET's channel length is lowered during scaling down the device, deviations from long channel behavior has been predicted. And because of their greatly improved electrical and optical features along with the presence of semiconductor business, silicon nanowire transistors have gotten a lot of interest as a potential replacement for traditional MOSFETs [68]. It was reported that the carrier mobility of small-diameter SiNWs is high and also the ability to fabricate high performance field effect transistors FETs requires a high carrier mobility. Since silicon nanowires SiNWs consist a ratio of high surface-to-vol. , comparatively mass carriers can be easily regulated by a modest electrical field applied to the gate and it has also found that these SiNWs-related nano FETs are extremely sensitive [69].

1.8 Objective of the Research Work

In our research study, we aimed to investigate how variations in high-k dielectric materials impact the analog and switching performance of JL-GAA-SiNWFETs (Gate-All-Around Silicon Nanowire Field-Effect Transistors). To conduct our analysis, we utilized the ATLAS SILVACO-

3D simulator and performed simulations at a low bias drain voltage of 0.1V. For the gate electrode, we used Niobium with a work-function of 4.8 eV.

Our study focused on evaluating several key parameters to assess the performance of JL-GAA-SiNWFETs. These parameters included Id-Vg (drain current versus gate voltage), transconductance (measurement of how the output current changes in response to a change in the input voltage), subthreshold swing (change in gate voltage required for a tenfold change in drain current), device efficiency, switching ratio, and leakage current.

Through our simulations and analysis, we discovered that the HfO2 (hafnium oxide) dielectric material outperformed SiO2 (silicon dioxide) and Al2O3 (aluminum oxide) in all evaluated parameters. This indicates that HfO2 is the most suitable high-k dielectric material for enhancing the performance of JL-GAA-SiNWFETs.

Furthermore, our study explored an alternative approach to achieve a dielectric layer on a smaller width by utilizing a stack formation. We applied SiO2 as the first layer in the stack, as it demonstrated better compatibility with Si nanowires. The second dielectric layer was varied and studied using SiO2, Al2O3, and HfO2. This combination resulted in effective oxide thickness (EOT) values of 1nm, 0.7nm, and 0.6nm, respectively.

Overall, our research highlights the significance of high-k dielectric variations in influencing the analog and switching performance of JL-GAA-SiNWFETs. The findings indicate that HfO2 exhibits superior characteristics compared to SiO2 and Al2O3, showcasing its potential for optimizing device performance. The utilization of dielectric stack formations also provides a viable approach for achieving desired oxide thickness on smaller device dimensions.

CHAPTER 2

DEVICE STRUCTURE & SIMULATION IN ATLAS SILVACO-3D

2.1 ATLAS SILVACO-3D

ATLAS SILVACO-3D is a powerful software tool used for the three-dimensional (3D) simulation of semiconductor devices. It is developed by Silvaco Inc., a leading provider of electronic design automation (EDA) software. The software is specifically designed for advanced process technologies and enables engineers and researchers to model, analyze, and optimize the performance of semiconductor devices in a 3D environment. This software has the ability to simulate the manufacturing process of semiconductor devices, such as oxidation, diffusion, ion implantation, removal, coating, lithography, etc. This is a large suite of highly sophisticated tools—among which is ATLAS—that aid in the design and development of all types of semiconductor and VLSI devices. This module is capable of simulating different pieces of semiconductor equipment, including MOSFETs, HEMTs and solar cells, in 2D and 3D manners[70].

ATLAS SILVACO-3D provides a comprehensive suite of simulation capabilities that accurately simulate the behavior of various semiconductor devices, including transistors, diodes, solar cells, sensors, and more. It employs advanced numerical algorithms and physics-based models to capture the complex interactions between electrical, thermal, and optical phenomena within the device structures. The software allows users to define the geometric layout of the device, specify material properties, and define the operational conditions and boundary conditions. It then solves the governing equations using numerical techniques to simulate the electrical behavior of the device under different operating conditions. This includes modeling carrier transport, charge generation and recombination, electrostatics, quantum effects, and other relevant physical phenomena. ATLAS SILVACO-3D offers a wide range of analysis capabilities, such as current-voltage (IV) characteristics, capacitance-voltage (CV) characteristics, charge transport analysis, breakdown voltage analysis, thermal analysis, and more. It provides detailed insights into device performance, allowing engineers to optimize design parameters and assess the impact of process variations and design modifications. The software also offers a user-friendly graphical interface that facilitates device setup, visualization of simulation results, and post-processing of data. It supports efficient parallel computing to expedite simulation times and provides various data analysis and visualization tools to aid in result interpretation.

ATLAS SILVACO-3D is widely used in the semiconductor industry and academic research for the design and optimization of advanced semiconductor devices. Its accurate 3D simulation capabilities contribute to the development of more efficient, reliable, and high-performance electronic devices across various application domains.

2.2 DEVICE STRUCTURE

Figure 1 depicts the proposed structure of our device, showcasing its key dimensions and layers. The entire device measures 42nm in length, with a channel length of 20nm. At the interface, there is an oxide layer composed of SiO2. The device features a metal gate, which has a thickness denoted as T1. Additionally, there are varying dielectric layers with a thickness denoted as T2, and an interfacial oxide layer (SiO2) with a thickness denoted as T3. The channel diameter, represented as 2R, is also the thickness of the silicon layer.

In all simulations, the gate length remains consistent at 20nm. Similarly, the varying oxide layer and interfacial oxide layer maintain a length of 20nm. The source and drain regions measure 10nm each, while the electrodes at both ends have a length of 1nm. For a comprehensive overview, please refer to Table 1, which lists all these parameters for reference and further analysis.

By providing these detailed dimensions and layer thicknesses, the structure of the device is clearly outlined, enabling researchers and engineers to understand the physical characteristics and design considerations of the proposed device configuration.

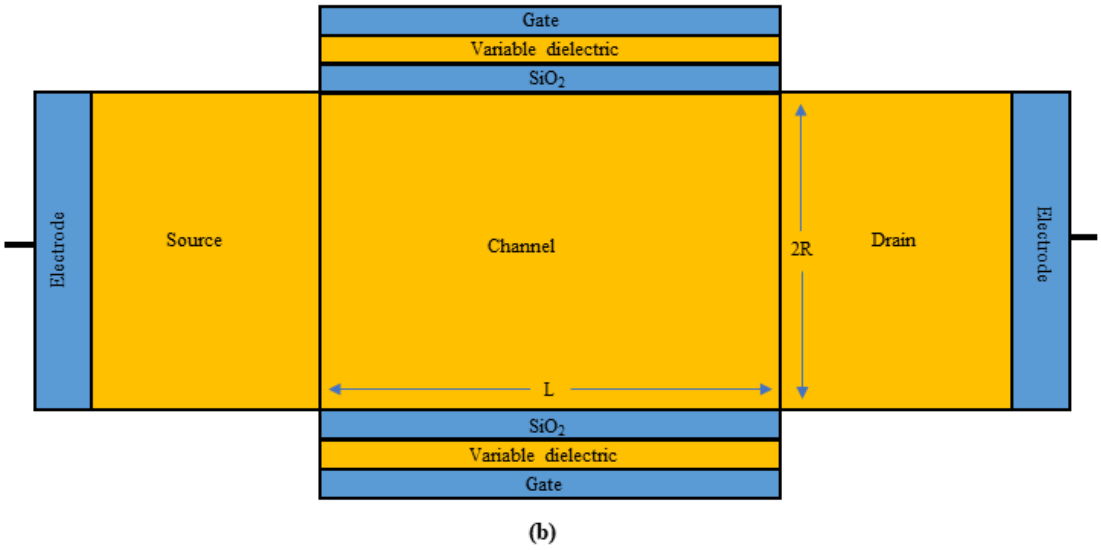


Figure 2.1 - Junction less gate all around silicon nano wire FET (a) JL-GAA-SiNW FET (b) cross sectional view.

Table 2.1: Technology parameters

Device Parameters	JL-GAA-SiNWFET
Channel Length(nm)	20.00
Diameter of Silicon film(nm)	20.00
Thickness of varied oxide and interface oxide respectively(nm)	0.5 & 0.5
Length of Source and Drain(nm)	10.00
Length/Thickness of electrode (nm)	1.00

Thickness of varied oxide and SiO_2 respectively (nm)	0.5 & 0.5
Dielectric of SiO_2, Al_2O_3, HfO_2 respectively (nm)	3.9, 9, 2.5
Gate work-Function Of Niobium (eV)	4.8
Doping of Channel, Source and Drain (N-type)	10^{19} cm^{-3}

A high and uniform doping concentration of $1x10^{19}$ cm^{-3} is implemented throughout the entire region spanning from the source to the channel and extending towards the drain. This intentional doping ensures the attainment of the desired threshold voltage for the device. It is important to note that the device is N-type doped, indicating the predominant presence of electrons as the majority carriers. By uniformly doping the device with N-type dopants, the necessary charge carrier concentration is established, enabling the device to function effectively.

CHAPTER 3:

RESULT AND DISCUSSION

3.1 Comparative Analysis of Gate Materials in JL GAA SiNW FET for Improved Performance.

This study introduces a novel device called the JL GAA SiNW FET, which demonstrates superior performance when utilizing an HfO_2 material gate substrate with a dielectric constant of 25. Figure 3.1 illustrates the relationship between drain current and gate voltage at a fixed drain voltage (V_d) of 0.05V for the junctionless gate all around silicon nanowire FET. The experiment investigates the impact of three different gate materials on the device's characteristics, specifically comparing the results obtained with HfO_2, SiO_2, and $Al2O_3$.

The analysis of the obtained curves reveals that the drain current peak is significantly higher when using HfO_2 as the gate material compared to SiO_2 and $Al2O_3$. This indicates that HfO_2 offers improved conductivity and facilitates better current flow within the device. Additionally, the off current, which represents the leakage current when the device is in the off state, is lower for HfO_2 compared to the other gate materials. This implies that HfO_2 exhibits better insulation properties and effectively suppresses the unwanted flow of current when the device is intended to be off.

Moreover, the permittivity of the gate material plays a crucial role in device performance. It is observed that as the permittivity increases, the ON current also increases. This indicates that HfO_2, with its higher permittivity, allows for a more efficient modulation of the channel and facilitates enhanced current conduction when the device is in the ON state.

Overall, the experimental findings highlight the favorable characteristics of HfO_2 as a gate material in the JL GAA SiNW FET. It exhibits higher drain current, lower off current, and improved permittivity compared to SiO2 and $Al2O_3$, making it a promising choice for enhancing the performance of nanowire FETs.

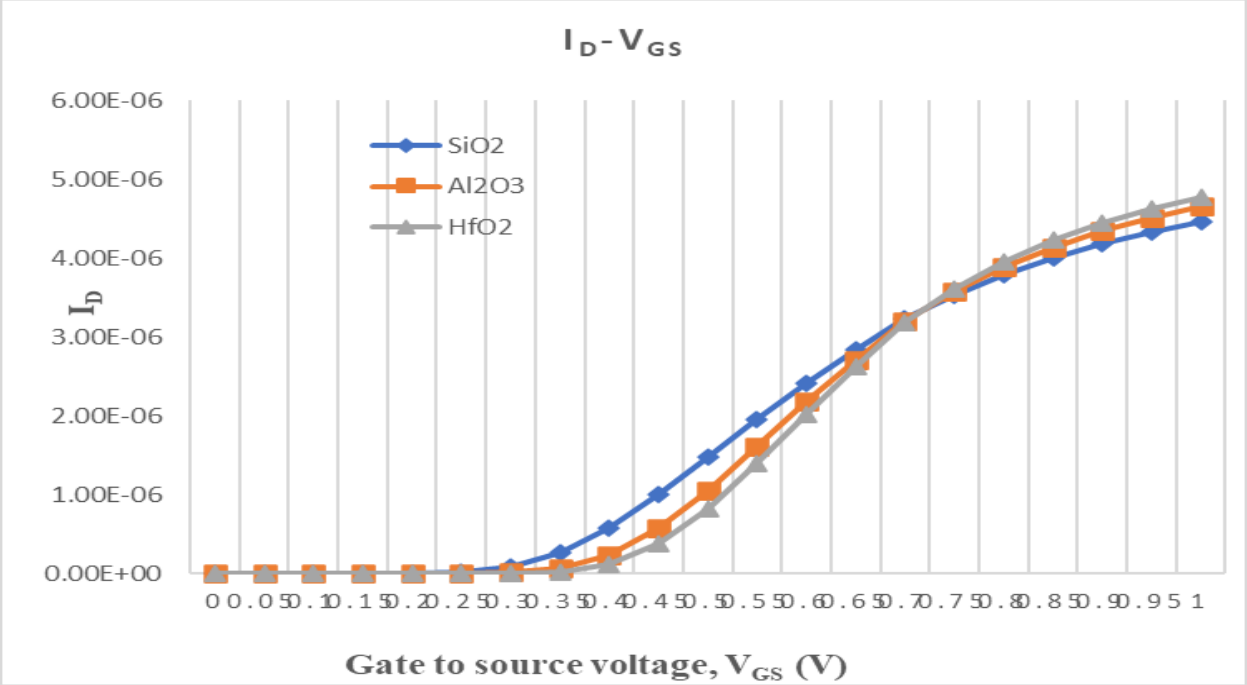


Figure. 3.1 - Transfer characteristics of drain current vs gate voltage at V_d = 0.05 V for JL GAA SiNW FET

3.2 Comparative Analysis of Gate Materials in JL GAA SiNW FET for Switching Performance and Leakage Current

In this study, we investigate the impact of different gate materials on the switching performance and leakage current of JL GAA SiNW FET. Figure 3.2 presents the switching ratio, represented by I_{ON}/I_{OFF}, as a function of dielectric constant at V_d=0.05V. The results indicate that the peak performance is achieved with HfO_2, surpassing SiO_2 and $Al2O_3$. This suggests that the speed of the device is significantly improved when utilizing HfO_2 as the gate material.

Furthermore, figure 3.3 demonstrates the leakage current, denoted by I_{OFF}, for the JL GAA SiNW FET with different gate materials. It is observed that HfO_2 exhibits lower leakage current compared to the other materials. A lower leakage current is desirable as it reduces the occurrence of the short channel effect. These findings highlight the favorable characteristics of HfO_2 gate material with a dielectric constant of 25, in terms of both switching performance and leakage current.

Overall, the study provides valuable insights into the impact of gate materials on the performance of JL GAA SiNW FET, emphasizing the superiority of HfO_2 in terms of speed enhancement and reduced leakage current.

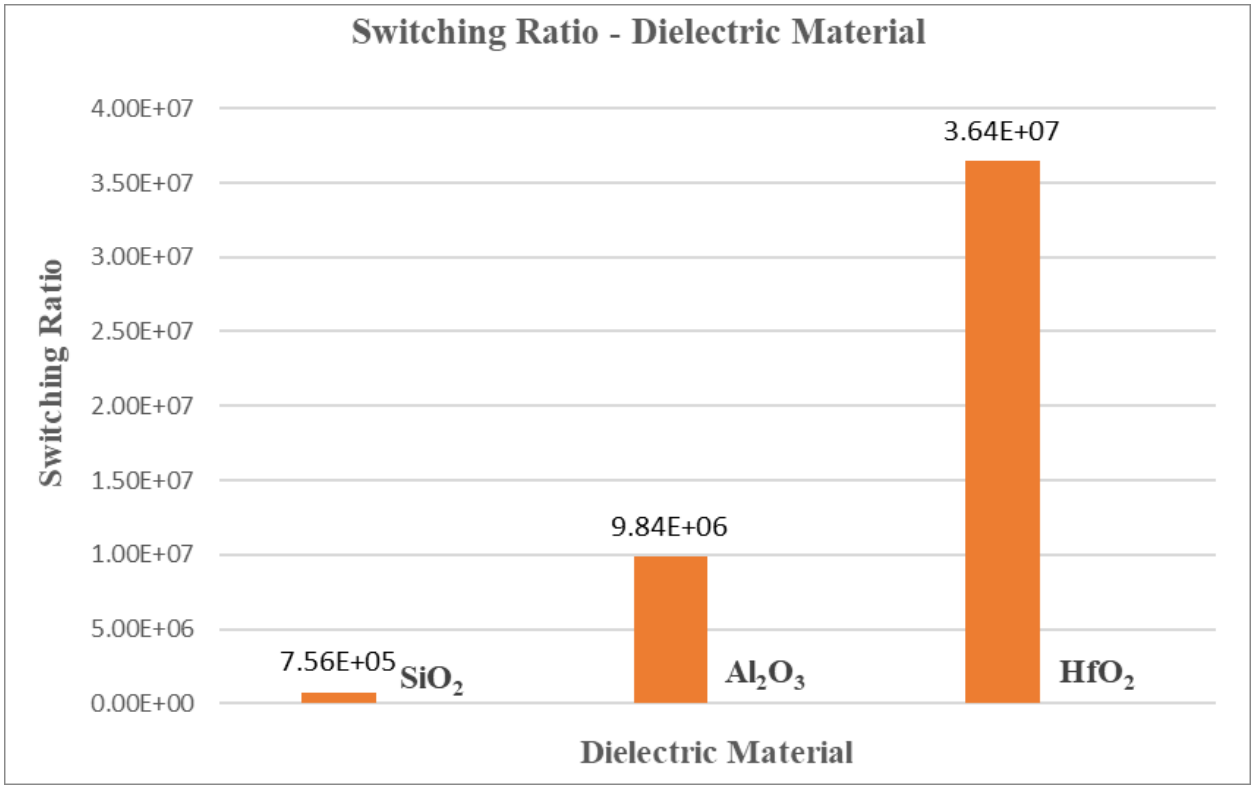


Figure 3.2 - . The graph of switching ratio vs dielectric material for JL GAA SiNW FET at V_d=0.4V.

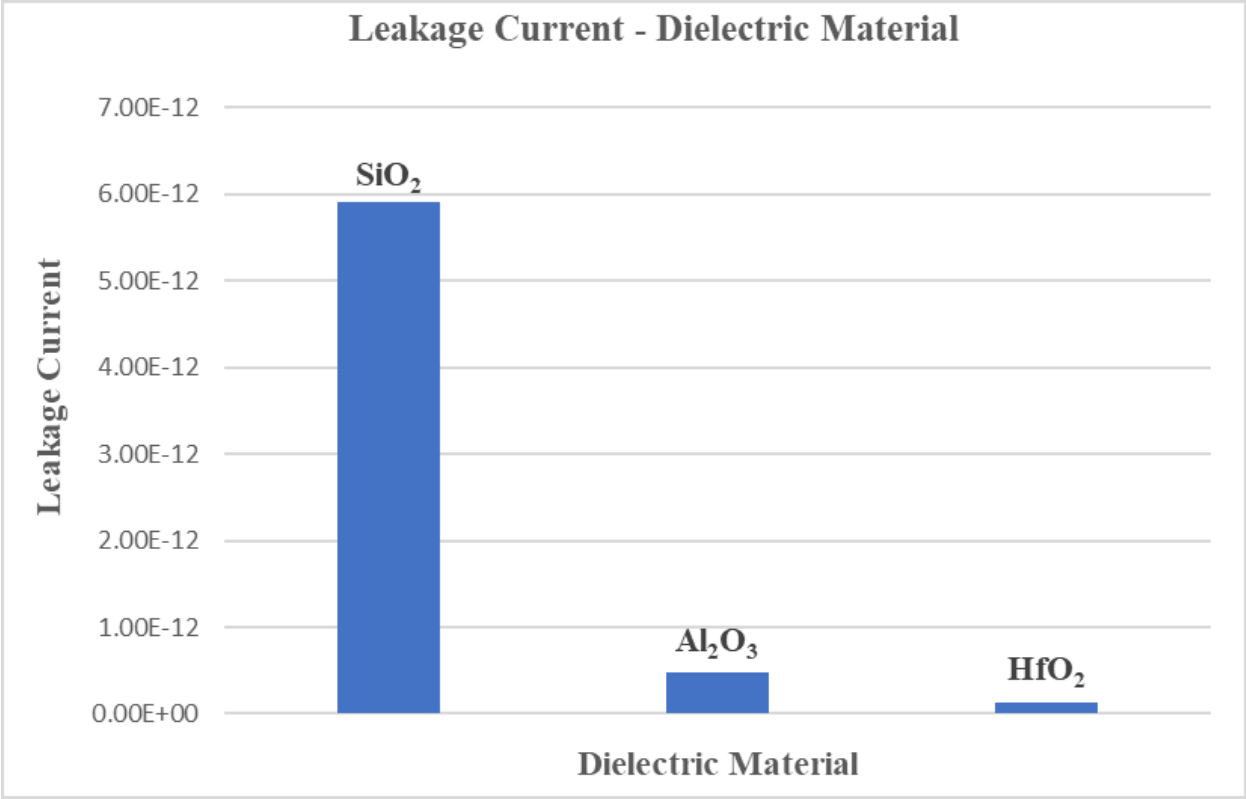


Figure 3.3 - The graph of leakage current vs dielectric material for JL GAA SiNW FET at V_d=0.1V.

3.3 Comparative Analysis of Transconductance and Transconductance Factor in JL GAA SiNW FET with Different Gate Materials

In this study, we investigate the transconductance and transconductance factor (TGF) of JL GAA SiNW FET with different gate materials. The aim is to compare the performance of HfO_2, $SiO2_2$, and Al_2O3 in terms of their impact on key analog parameters.

One of the important parameters examined is the transconductance, which is defined as the ratio of change in drain current to the corresponding gate voltage. This parameter reflects the ability of the device to amplify and control the signal. Figure 3.4 illustrates the transconductance characteristics for the different gate materials. It is observed that the transconductance (Gm) of HfO_2 is higher compared to SiO_2 and Al_2O_3. This indicates enhanced electron mobility, improved gate controllability, and higher average carrier velocity in devices utilizing HfO_2 as the

gate material. Moreover, the higher transconductance suggests a reduced decay of the short channel effect, leading to improved device performance.

Furthermore, the transconductance factor (TGF) provides insights into the efficiency and linearity of the device operation. The TGF is a measure of how effectively the device converts the gate voltage into drain current. A higher TGF indicates better performance in terms of amplification and signal fidelity.

Overall, the study highlights the impact of different gate materials, such as HfO_2, SiO_2, and $Al2O_3$, on the transconductance and transconductance factor in JL GAA SiNW FET. The results indicate that HfO_2 offers superior performance, exhibiting higher transconductance and improved device characteristics related to electron mobility, gate controllability, carrier velocity, and short channel effect.

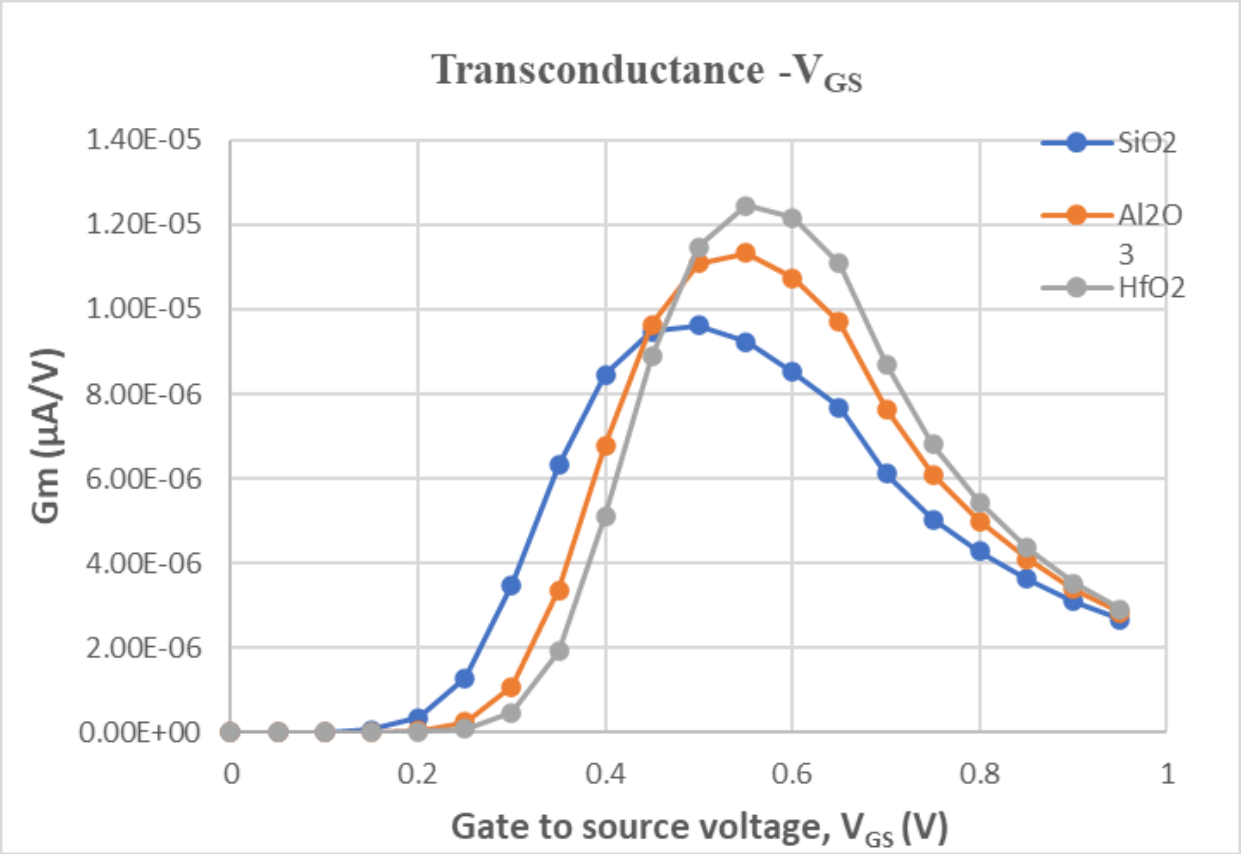


Figure 3.4 - The graph of transconductance vs gate voltage for JL GAA SiNW FET at V_d=0.4V and channel length 20nm

3.4 Comparative Analysis of Subthreshold Swing in JL GAA SiNW FET with Different Gate Materials

In modern semiconductor devices, achieving better performance and efficiency is of paramount importance. One key parameter that significantly affects device performance is the subthreshold swing (SS). The subthreshold swing quantifies the change in gate voltage required to produce a decade change in drain current when the device is operating in the subthreshold region.

In this study, we investigate the subthreshold swing characteristics of JL GAA SiNW FET using different gate materials, specifically HfO_2, SiO_2, and Al_2O_3. The objective is to compare and analyze the impact of these gate materials on the subthreshold swing, which in turn affects the device's gate controllability and gate coupling capacitance.

Figure 3.5 presents the experimental results, displaying the subthreshold swing values for HfO_2, SiO_2, and Al_2O_3 gate materials. It is observed that the subthreshold swing of HfO_2 is lower compared to SiO_2 and Al_2O_3. This implies that HfO_2 offers improved gate controllability on the channel, allowing for more precise control over the transistor's switching behavior.

A lower subthreshold swing is desirable as it signifies enhanced gate coupling capacitance, enabling efficient charge modulation and reduced leakage currents. This improved gate control ultimately leads to better overall device performance and power efficiency.

The results highlight the significance of selecting an appropriate gate material for achieving lower subthreshold swing values. HfO_2, in particular, exhibits superior performance in terms of subthreshold swing compared to SiO_2 and Al_2O_3. This finding suggests that integrating HfO_2 as the gate material in JL GAA SiNW FETs can lead to improved device performance, enhanced gate controllability on the channel, and superior gate coupling capacitance.

In summary, the study investigates the subthreshold swing characteristics of JL GAA SiNW FET using different gate materials. The findings demonstrate that HfO_2 offers a lower subthreshold swing compared to SiO_2 and Al_2O3, indicating improved gate controllability and gate coupling

capacitance. These results have significant implications for the design and optimization of semiconductor devices, particularly in achieving better performance and power efficiency.

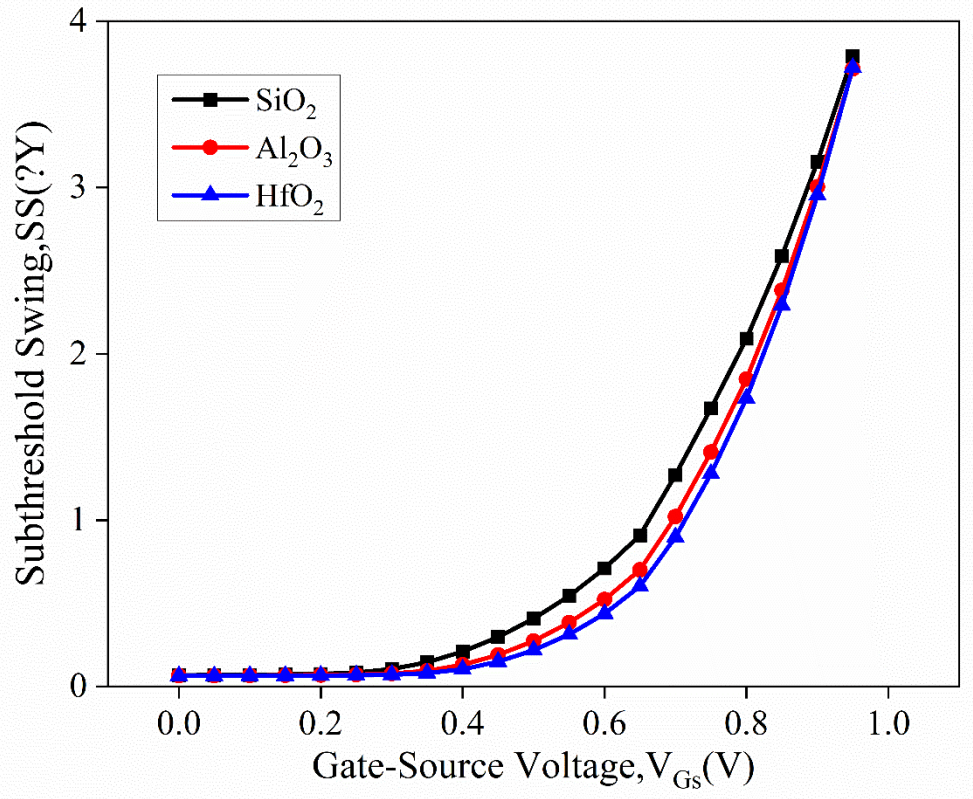


Figure 3.5 - The curve of SS vs gate voltage for JL GAA SiNW FET at V_d=0.4V and channel length 20nm

3.5 Comparative Analysis of Transconductance Generation Factor (TGF) in JL GAA SiNW FET with Different Gate Materials

Efficiency and power performance are crucial factors in the design of semiconductor devices. The transconductance generation factor (TGF) plays a significant role in determining the efficiency and gain of a device per unit power loss. In this study, we examine and compare the TGF characteristics of JL GAA SiNW FETs utilizing different gate materials, including HfO_2, SiO_2, and Al_2O_3.

Figure 3.6 illustrates the experimental results, showcasing the TGF values for each gate material. The TGF, being directly proportional to the transconductance, represents the efficiency and gain achieved per unit power dissipation in the device. Higher TGF values indicate enhanced device efficiency and superior performance, particularly when operating at low power supply levels. Our findings demonstrate that HfO_2 exhibits a higher TGF compared to SiO_2 and Al_2O_3 gate materials. This signifies that the device efficiency of HfO_2 is superior to the other materials, indicating its capability to generate more gain per unit power loss. The peak performance of HfO_2 in terms of both transconductance and TGF further highlights its effectiveness in achieving higher efficiency levels.The higher TGF observed in HfO_2-based JL GAA SiNW FETs suggests that this gate material offers improved power performance and efficiency. This finding has significant implications for low-power applications, where maximizing efficiency is crucial. By utilizing HfO_2 as the gate material, designers and engineers can optimize device performance, reduce power consumption, and achieve higher efficiency levels.

In summary, the study investigates the transconductance generation factor (TGF) in JL GAA SiNW FETs using different gate materials. The results reveal that HfO_2 exhibits a higher TGF compared to SiO_2 and Al_2O_3, indicating improved device efficiency and performance. These findings emphasize the potential of HfO_2 as a gate material for achieving higher efficiency and gain per unit power loss. Further exploration of HfO_2-based devices can lead to advancements in low-power applications, enabling more efficient semiconductor devices.

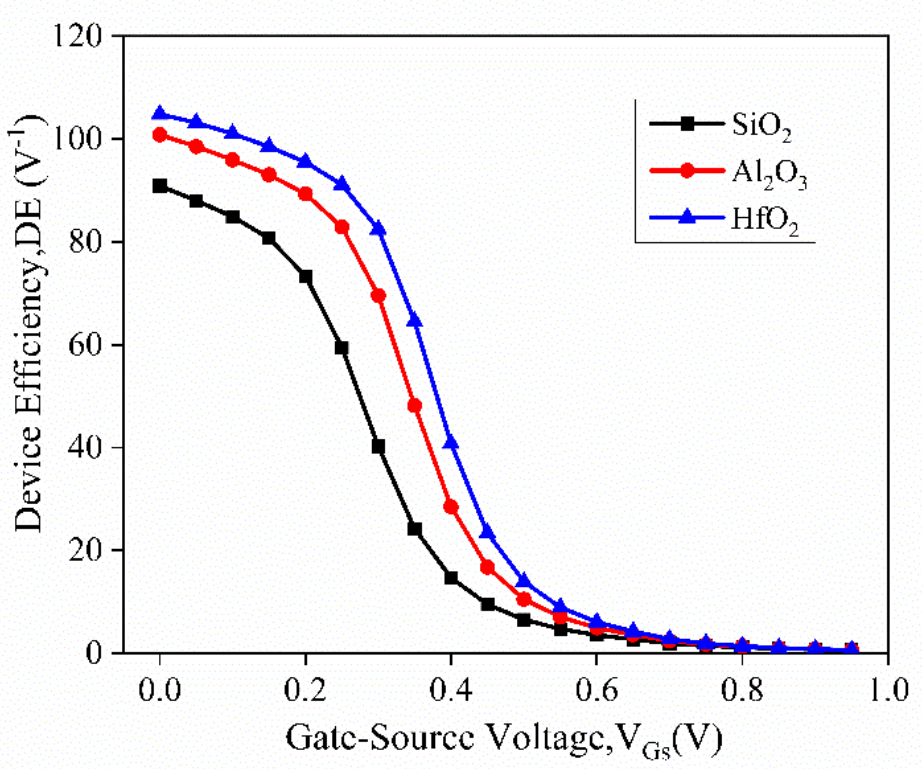


Figure 3.6 - The plot of device efficiency vs gate voltage for JL GAA SiNW FET at V_d=0.4V and channel length 20nm

3.6 Conclusion

This paper presents a comprehensive investigation into the influence of high-k dielectric variation on the analog and switching performance of GAA SiNW FETs. Using ATLAS SILVACO 3D simulation software, we conducted extensive simulations on the devices, considering a low bias drain voltage of 0.1V and utilizing Niobium as the gate electrode with a work-function of 4.8 eV. Our analysis focused on key parameters such as Id-Vg characteristics, transconductance, subthreshold swing, device efficiency, switching ratio, and leakage current.

The results of our study demonstrate significant improvements in several performance metrics when utilizing HfO_2 as the dielectric material. Specifically, the transconductance of HfO_2-based devices exhibited a remarkable enhancement of 29% compared to SiO_2. This indicates an

improved ability to control the flow of current through the channel, leading to enhanced device performance. Additionally, the subthreshold swing was observed to be lowered by 6%, indicating improved gate controllability and reduced power consumption.

The switching ratio, a crucial parameter representing the ratio of on-state current to off-state current, demonstrated a remarkable improvement of 48 times when using HfO2 as the dielectric material compared to SiO_2. This suggests that HfO_2 enables more efficient switching operations, leading to improved overall device performance.

Furthermore, the device efficiency, which represents the gain generated per unit power loss, exhibited superior performance with HfO_2 as the dielectric material. The specific characteristics of HfO_2 enabled higher efficiency levels, particularly at low power supply levels, making it a favorable choice for applications that prioritize power efficiency.

Finally, the leakage current, which is a critical factor in device reliability, was found to be lower for HfO_2 compared to SiO_2. This reduction in leakage current indicates a reduction in the occurrence of undesirable current flows and improved overall device stability.

In summary, our findings highlight the superior performance of HfO_2 as a high-k dielectric material in GAA SiNW FETs. The enhancements observed in transconductance, subthreshold swing, switching ratio, device efficiency, and leakage current make HfO_2 a promising choice for improving the analog and switching performance of these devices. This research provides valuable insights for the design and optimization of future semiconductor devices, paving the way for more efficient and high-performance electronic systems.

Future work in this field should focus on exploring alternative high-k dielectric materials, optimizing device dimensions and gate electrode materials, conducting experimental validations, studying reliability and stability, and investigating integration with other device technologies. Continued research in these areas will contribute to further advancements in GAA SiNW FETs and pave the way for their practical implementation in various electronic applications.

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