TCAD SIMULATION BASED ANALYSIS OF TFET BASED ON DIFFERENT STRUCTURAL SHAPE: F-SHAPED AND Z-SHAPED

A PROJECT REPORT
SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTERS OF SCIENCE
IN
PHYSICS

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Abstract

This work provides a thorough investigation of Z-shaped and F-shaped tunnel field-effect transistors (TFETs), emphasizing the unique structural characteristics and improved performance of these devices. With a architecture shaped like the letter "F," the F-shaped TFET provides better electrostatic control over the channel, improving tunnelling efficiency and raising on-current while preserving a competitive subthreshold swing. On the other hand, the Z-shaped TFET exhibits better control over the tunnelling junction due to its Z-like gate design, which lowers the subthreshold slope and lessens the impact of short channels. These sophisticated geometries are intended to overcome the drawbacks of traditional TFETs, including significant off-state leakage and inadequate on-current, thus positioning them as viable options for low-power and high-performance applications. It is anticipated that forthcoming developments will centre on enhancing material attributes, perfecting manufacturing methods, and investigating new device structures in order to augment the efficiency and expandability of these inventive TFET configurations. The findings of this study highlight the potential of Z-shaped and F-shaped TFETs in developing semiconductor technology and satisfying the needs of electronic gadgets of the future. Additionally, integrate these designs with newly developed materials and nanoscale manufacturing techniques.

ACKNOWLEDGEMENT

We are extremely grateful to our project guide, **Dr. Rishu Chaujar**, Professor, Department of Applied Physics, Delhi Technological University, Delhi for providing invaluable guidance and being a constant source of inspiration throughout our research. We will always be grateful to her for the extensive support and encouragement.

We are extremely grateful to all the panel members who evaluated our progress, guided us throughout our project, and gave us constant support and motivation, innovative ideas and all the information that we needed to pursue this project.

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List of Abbrevations

Abbreviations

IC- Integrated Circuit

FET- Field Effect Transistor

MOSFET- Metal Oxide Semiconductor Field Effect Transistor

CMOS- Complementary Metal-Oxide Semiconductor

FINFET- Fin Field Effect Transistor

VLSI- Very Large-Scale Integration

IGFET- Insulated-Gate Field-Effect Transistor

E-device – Enhancement mode device

D-device – Depletion mode device

SCE- Short Channel Effect

DIBL- Drain-Induced Barrier Lowering

SS- Subthreshold swing

RF- Radio frequency

TFET- Tunnel field effect transistor

BTBT- Band to band tunneling

TCAD- Technology computer aided device

GUI- Graphical user interface

G_m- Transconductance

T_{GF}- Transconductance generating Factor

Symbols

V_{ds} - Drain voltage

V_{gs} - Gate voltage

V_{th} - Threshold voltage

I_{ds} - Drain Current

V_p – Punchthrough voltag

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Chapter-1

Introduction

1.1 Field-Effect Transistor (FET):

FET has three terminals, namely the source, gate, and drain. There are two main types of FETs: MOSFET (Metal-Oxide-Semiconductor FET) and JFET (Junction Field-Effect Transistor). An electric field applied across the semiconductor material drives a FET's ability to control current flow. The MOSFET's gate terminal voltage controls the current flow between its source and drain terminals. Without input current, JFETs function by enabling current flow between the source and drain terminals when a voltage is applied to the gate terminal. Because of its high input impedance and voltage control, FETs are a good choice for applications where the input signal level is critical. Generally, FETs have slower switching speeds compared to BJTs, especially in the case of JFETs. However, MOSFETs can have very fast switching speeds, rivaling or surpassing BJTs. FETs, particularly MOSFETs, are known for their low power consumption, especially in static (non-switching) states. BJTs are commonly used in applications requiring moderate to high current amplification, such as audio amplifiers. FETs, especially MOSFETs, are widely used in integrated circuits, digital applications, and situations where high input impedance and low power consumption are essential.

1.2 CMOS Technology:

CMOS (Complementary Metal-Oxide-Semiconductor) technology is often used semiconductor manufacturing process that plays a key role in the production of ICs such as microprocessors, memory chips, and other digital logic devices. The term

"complementary" refers to the use of both n-type (negatively-doped) and p-type (positively-doped) MOSFETs within the identical integrated circuit. CMOS technology relies on the basic structure of MOSFETs. A small layer of insulating oxide separates the semiconductor from the metal gate of a MOSFET. The semiconductor material is typically silicon. CMOS circuits use both N-channel MOSFETs (NMOS) and P-channel MOSFETs (PMOS) [1]. When a positive voltage is provided to the gate of an NMOS transistor, electrons can go from the source to the drain.

When a negative voltage is given to the gate of a PMOS transistor, holes can move from the source to the drain. The use of both types of MOSFETs allows for complementary operation, where one type of transistor is off while the other is on, minimizing power consumption and heat generation. The low power consumption of CMOS technology is one of its main benefits. This is because CMOS circuits draw negligible current when they are in a static state (not switching), making them highly energy-efficient. CMOS circuits have high noise immunity due to the complementary operation.

When one transistor is off, the other is on, reducing the risk of signal corruption by noise. CMOS technology is highly scalable, allowing for the incorporation of several transistors on a single chip. This scalability has been a driving force in the miniaturization and increasing complexity of electronic devices. CMOS is versatile and is used in both digital and analog applications. It is commonly found in microprocessors, memory chips, image sensors, and other digital circuits.

The fabrication process involves creating patterns on a silicon wafer through photolithography, deposition, and etching. The process includes creating NMOS and PMOS transistors, interconnecting them with metal layers, and adding insulating layers. CMOS technology is prevalent in a variety of electronic devices, such as digital cameras, smartphones, laptops, and numerous other digital systems.

1.3 TFET

A transistor type that functions according to the principles of quantum tunneling is called a TFET. TFETs take advantage of quantum tunneling across a thin barrier [2], in contrast to conventional transistors, which depend on thermionic emission of carriers over a potential barrier. Compared to conventional MOSFETs, TFETs can

achieve reduced power consumption and possibly higher switching speeds thanks to their unique operating principle.

The TFET makes use of a phenomenon known as quantum tunneling, which allows particles to cross potential energy barriers that would be impossible in classical physics. When it comes to TFETs, electrons travel between the source and drain terminals by tunneling across a tiny barrier. TFETs have the ability to drastically lower an electrical device's power usage. Because tunneling is used for carrier transport rather than thermal emission, TFETs can function at lower voltages, which lower energy dissipation. Theoretically, TFETs' distinct tunneling mechanism can lead to quicker switching speeds than MOSFETs'. For situations where high-speed operation is essential, this feature is beneficial.

Increases in SCEs, off-leakage current, and subthreshold swing have been observed in MOSFETs that have been downscaled. MOSFETs have a minimal subthreshold swing of 60 mV/dec at normal temperature. For the deep submicron domain, MOSFET is hence unsuitable. The drawbacks of MOSFETs are being examined by means of a new device construction. The newest and most advanced device is the TFET. Because of their superior performance—low power dissipation, low leakage current, and SS of less than 60 mV/dec, TFETs are the best option for low power applications [3]. High I_{off} current is mostly caused by the ambipolar effect, which can be mitigated by structural asymmetry and different levels of doping in the source and drain. This could lead to a decrease in the TFET's I_{off} current and an increase in the I_{on}/I_{off} current ratio. Basic p-i-n structures, TFETs operate on the principle of BTBT and have reversed bias at the gate terminal. Low I_{on} current also affects TFET's fundamental structure. Nonetheless, the Ion current can be further enhanced by changing the structural physical characteristics.

Chapter-2

Overview of the SILVACO Atlas Simulation Framework

2.1 Introduction

A significant part of today's semiconductor device and process development is conducted through computer modeling. This method is known as TCAD. Technology computer aided design is a category of electronic design automation that simulates the manufacturing of semiconductors and the functioning of semiconductor devices. Process TCAD refers to the modeling of the fabrication process, whereas Device TCAD refers to the modeling of the device's functionality. A strong and adaptable tool that is frequently used in the modeling and simulation of semiconductor devices is the SILVACO Atlas simulation framework. Strong meshing capabilities are provided by SILVACO Atlas, giving users control over the mesh's density and quality. Accurate simulation results require proper meshing, particularly when working with complicated device geometries. The software offers an input deck (scripting language) for configuring simulations, and Tony Plot and other GUI (Graphical User Interface) features make it easier to visualize the results. SILVACO uses sophisticated physics models to simulate semiconductor behavior precisely. This ensures that simulations correspond with the behavior of real-world devices. It includes models for carrier transport, tunneling, and several other physical phenomena. This chapter delves into the salient characteristics and functionalities of SILVACO Atlas, with a particular emphasis on its utilization in our research on MOSFETs, DGMOSFETs and TFETs.

2.2 Overview of SILVACO Atlas

We may simulate and examine the behavior of semiconductor devices at the nanoscale with the help of SILVACO Atlas, a complete device simulation program. It has the capability of simulating the two-dimensional (2D) [4] and three-dimensional (3D) semiconductor devices and helps to predict the energy band gaps, electrical properties, some factors like DIBL, SS etc. It provides a variety of simulation functionalities, such as circuit, device, and process simulation. The program is compatible with a number of semiconductor technologies, including CMOS technology, which makes it appropriate for a broad variety of applications. The physical structures and bias conditions of semiconductor devices are given by ATLAS, which offers physics-based simulation of these devices. Deck build is an interactive visual runtime environment that we have used to construct input decks for the device simulation process. Two different file kinds that we employed are included in the output. structure files and log files. An image of the device at a specific bias voltage is provided by the structure file (.str). Additionally, the terminal features determined by ATLAS are stored in the log file (.log). Tony plot can be used to plot either of these. SILVACO Atlas receives input files through Deck Build. The code in the input file initiates Atlas to run using the commands detailed in section 2.3. After that command, the input file must follow a specific pattern. The command groups are listed in the next section.

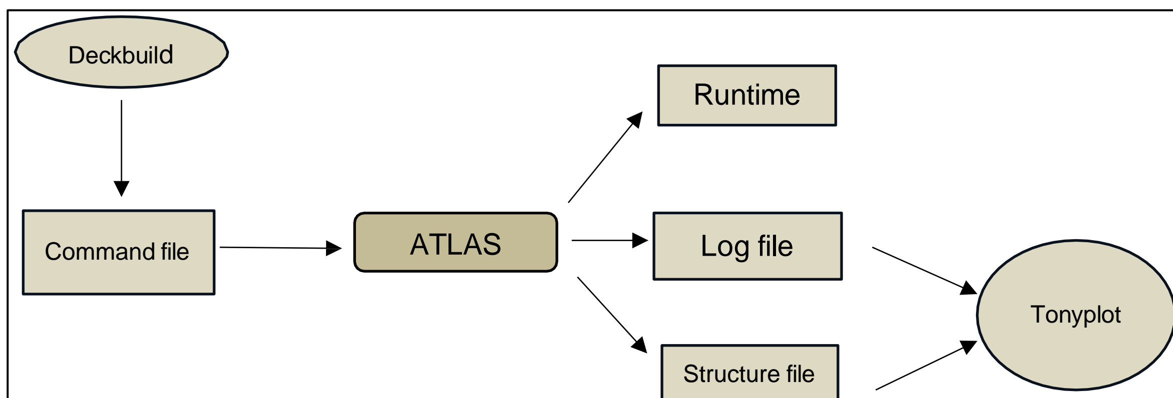


Fig 2.1: The simulation flow of Atlas

2.3 Structure simulation

The Atlas has a specified way of writing commands as any other software do have. By following the set of commands with primary statements, we have simulated the two-dimensional MOSFET and two dimensional DGMOSFET and TFET.

Group	*Statements*
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

[5]

Fig2.2: Showing the groups and statements for the SILVACO ATLAS TCAD simulation

2.4. 2D TFET proposed design

On the same tracks we have simulated the basic 2D TFET with length of the structure 0.11 micrometers. The quantum tunnelling meshing is defined. The source and drain are taken to be of silicon with doping $1e^{+20}$ each. The gate is taken of SiO_2. The n body of $1e^{+18}$ doping of silicon is use as channel body [6]. The ferroelectric material region is defined the silver metal with work function 4.07 eV have been used for gate and source and drain are taken as neutrals. mh.tunnel and me.tunnel are 0.24 and 0.20 respectively. For DC analysis, drain voltage is provided as 0V to 1V with the step of

0.1. And for the AC analysis, the ac frequency of $1e^6$ HZ is given with the input voltage of 0 Volts to -1 Volts with the step size of -0.1. Then, some of the parameters has been extracted using extract command like DIBL, Subthreshold voltage, I_{on} and I_{off} and their ratio.

Chapter 3

Tunnel Field-Effect Transistors

3.1 Tunnel Field-Effect Transistors (TFETs): An Overview

Unlike conventional FETs, which rely on thermionic emission, tunnel field-effect transistors (TFETs) use quantum tunneling to achieve current conduction. Electrons can tunnel through a barrier in a TFET from the source to the drain when a voltage is applied to the gate, which modifies the barrier width at the source-channel junction. Because of their tunneling process, TFETs can function at lower voltages than traditional MOSFETs, which could result in a reduction in power usage. TFETs are viewed as promising prospects for low-power and high-efficiency electronic applications, such as next-generation integrated circuits and low-power logic devices, because to their sharp subthreshold swing and potential for reduced off-state current. Nevertheless, difficulties including enhancing material qualities, enhancing on-current, and manufacturing.In contrast to traditional MOSFETs, which depend on thermionic emission, tunneling is utilized by TFETs, enabling them to attain subthreshold slopes that are steeper than the 60 mV/decade limit. TFETs are therefore excellent options for low-power electrical applications.

Unlike conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), tunnel field-effect transistors (TFETs) are a sophisticated family of transistors that use quantum mechanical tunneling to achieve charge carrier transport.

3.2 Fundamentals of Function

Band-to-band tunneling is the basis of operation for TFETs (BTBT). One type of carrier, such as p-type, is extensively doped in the source of a TFET, while the drain is heavily doped with the opposite type, such as n-type. The potential barrier width between the source and the channel is modulated when a voltage is applied to the

gate. Current can flow when this barrier narrows to the extent that electrons can tunnel from the valence band of the source to the conduction band of the channel.

3.3 Historical Development of TFETs:

3.3.1 Early Concepts and Theoretical Foundations:

The 1950s and 1960s were when the fundamental ideas of tunneling in semiconductors were developed. The Esaki diode, a crucial development for comprehending quantum tunneling in semiconductors, was created as a result of Leo Esaki's discovery of tunneling processes. Researchers started to suggest employing tunneling for switching devices by the 1970s, claiming that it may allow for high subthreshold slopes and lower power consumption than conventional FETs.

3.3.2 Initial Ideas and Early Technology:

The first theoretical suggestions for TFETs were made in the 1980s. Band-to-band tunneling for transistors was first studied, but there were few real-world applications and it was mostly theoretical. The viability of TFETs was demonstrated experimentally in the 1990s, overcoming obstacles including low on-current and fabrication issues.

3.3.3 Advancements in Materials and Device Design:

The twenty-first century saw significant advancements in nanofabrication techniques and materials science. To improve TFET performance, researchers experimented with a variety of semiconductor materials, such as silicon, germanium, and III-V compounds. The low-power potential of silicon-based TFETs was highlighted in 2004 when the first ones showed subthreshold slopes < 60 mV/decade. By 2006, tunneling junction performance had been improved by novel

device topologies such as heterojunction TFETs. All these advancements in design and material design leads to certain advantages despite of giving some cons has been effectively using in day to day market.

3.3.4 Modern Developments and Applications:

During the 2010s, the emphasis switched to circuit integration and TFET optimization for particular uses. Nanotechnology developments produced TFET designs that were more scalable and efficient. The demonstration of record-low subthreshold swings in 2012 and the proposal of hybrid TFET-CMOS circuits in 2015, which combine the low-power advantages of TFETs with the excellent performance of CMOS technology, are noteworthy turning points in the field. Research to address issues such as low on-current and variability has been going on in the 2020s, and TFETs are being explored for use in wearable electronics, energy-efficient computing, and the Internet of Things (IoT).

3.4 Key Points about TFETs:

- Principle of Operation: To modify current flow, TFETs use tunneling through a barrier that is controlled by gate voltage.
- Low Power Consumption: By operating at a lower voltage than MOSFETs, TFETs can drastically cut down on the amount of power used in digital circuits.
- Subthreshold Swing (SS): TFETs can attain subthreshold swing (SS) values that are lower than the 60 mV/decade limit, which improves their low-power efficiency.
- Materials and Design: TFETs can be made from a variety of materials, such as III-V compounds, silicon, and germanium, which can affect the device's overall efficiency, off-state leakage, and on-state current.

3.5 On the basis of different channel shapes:

In Tunnel Field-Effect Transistors (TFETs), the channel shape can significantly impact the device's performance. Different alphabetical channel shapes are designed to optimize various aspects of the TFET's operation, such as threshold voltage, subthreshold slope, and drive current. Some of these are:-

1. U-shaped

2. V-shaped
3. H-shaped
4. L-shaped
5. F-shaped
6. Z-shaped

3.6 Applications:

Energy-efficient integrated circuits, analog and radio frequency circuits, and low-power digital circuits are all excellent uses for TFETs.

TFETs are promising in several areas, especially when low power consumption is essential.

- Portable Electronics: The energy efficiency of TFETs can be advantageous for wearables, tablets, and smartphones.
- IoT, or the Internet of Things: TFET technology can help low-power sensors and gadgets in Internet of Things networks last longer on batteries and use less energy.
- Biomedical Devices: TFET integration can be advantageous for wearable and implantable medical devices that have low power requirements.

3.7 Challenges:

Although TFETs have great potential, they encounter obstacles including low on-current, unpredictability, and fabrication complexity. To solve these problems, research is still being done.

- On-Current (I_{ON}): TFETs' performance in high-speed applications may be constrained by their generally lower I_{ON} than MOSFETs.

- Issues with Materials and Fabrication: It is difficult to find the ideal material composition and device architecture for effective tunneling. This involves the requirement for accurate doping profiles and superior heterojunctions.
- Thermal Stability: As device dimensions decrease, it becomes increasingly important to ensure thermal stability and control heat dissipation in TFETs.

3.8 Advantages:

- Low Subthreshold Swing (SS): Unlike conventional MOSFETs, TFETs can achieve a subthreshold swing below the thermal limit of 60 mV/decade at ambient temperature. As a result, lower threshold voltages and hence lower power consumption are possible.
- Low Power Consumption: TFETs are ideally suited for low-power applications because of their effective switching properties, which make them perfect for energy-efficient and portable devices.
- High Scalability: It may be possible to scale down TFETs more efficiently than MOSFETs, enabling Moore's Law-compliant device downsizing.

3.9 Visions for the Future:

To improve TFET performance; current research is concentrated on investigating novel materials such as 2D materials (such as graphene and transition metal dichalcogenides) and creative device topologies. Although TFETs are not currently commonly used in commercial goods, recent developments indicate that they may be important in low-power electronics in the future as power efficiency becomes more and more important and technology continues to scale down. Both theoretical and practical developments have fueled the constant quest for more efficient electronic devices, which is reflected in the history and current development of TFETs. TFETs have the potential to completely transform the semiconductor industry by allowing extremely energy-efficient electronic products

Chapter 4

F-Shaped TFET

4.1 Introduction

An F-shaped Tunnel Field-Effect Transistor is a type of TFET where the channel geometry is shaped like the letter "F." With its unique F-shaped gate architecture, the F-shaped Tunnel Field-Effect Transistor (F-TFET) is a revolutionary design in the field of TFETs. By increasing electrostatic control over the channel, this design seeks to improve subthreshold swing and on-current (I_{on}), two important performance criteria for the device. The F-shaped gate provides improved control over the carrier injection from the source to the channel by enabling a more effective modification of the tunneling barrier. The F-TFET is a desirable choice for low-power applications because of its enhanced control, which can result in lower off-state currents and lower power consumption. Furthermore, the F-TFET's distinct geometry may be able to lessen some of the fabrication difficulties that come with conventional TFETs, providing a more scalable and producible alternative for upcoming semiconductor technologies.

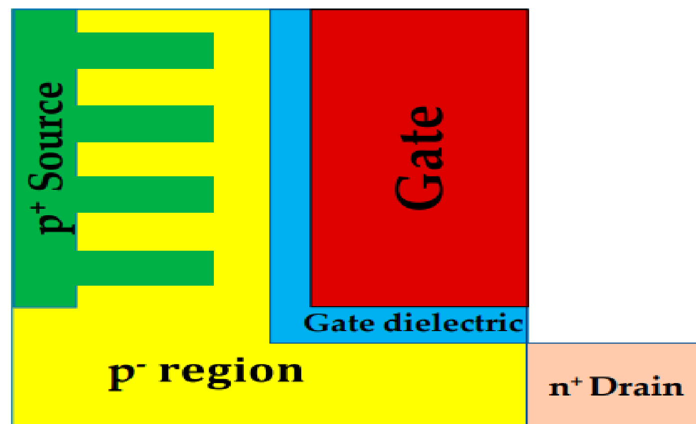


Fig. 4.1: The structure of the F-shaped TFET includes multiple sources.

By utilizing its distinct shape, this design seeks to improve a few of the TFET's performance attributes. An extensive examination of the F-shaped TFET's structure, benefits, possible uses, and difficulties is provided below.

4.2 Structure

The channel of the F-shaped TFET is made up of several horizontal and vertical segments that form the letter "F." The device's overall performance may be enhanced by the many tunneling junctions that this complicated design may produce. Usually, the structure consists of:

Vertical Segments: Band-to-band tunneling mostly takes place along these segments, which act as conduction pathways.

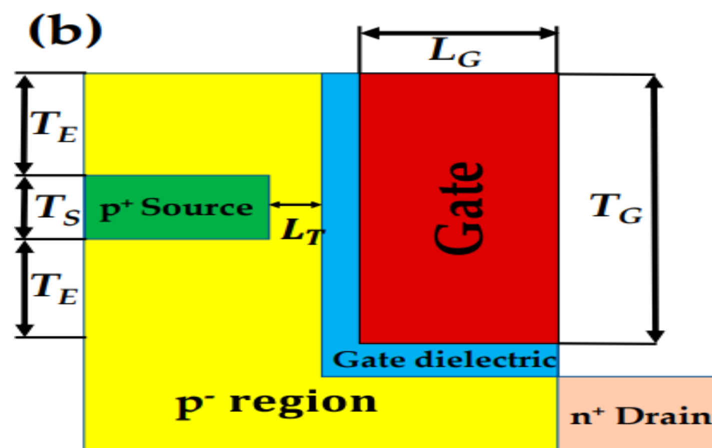


Fig. 4.2: Structure and parameter definitions of the F-shaped TFET

Horizontal Segments: Connecting vertical channels horizontally can aid in dispersing current, lowering resistance and enhancing drive current overall.

Parameters	Abbreviations	SG-F-TFET
Gate oxide thickness	T_{OX}	1nm
Gate oxide material (k-value)	-	SiO_2 (k=3.9)
Total device length	L_{tt}	160 nm
Thickness above and below source	T_2	Variable (12.5 nm)
Channel thickness at bottom of device	$T_1 = T_D + T_{OX}$	7 nm
Total device thickness	T_{tt}	42 nm
Lateral tunneling length	L_T	Variable (4 nm)
Source thickness	T_S	Variable (10 nm)
Source length	L_S	Variable (67 nm)
Gate length	L_G	20 nm
Gate thickness	$T_G = 2T_2 + T_S$	35 nm
Channel thickness	$2T_2 + T_1 + T_S$	42nm
Channel length (upper)	L_{C1}	71 nm
Channel length (bottom)	L_C	92 nm
Drain length	L_D	68 nm
Drain thickness	T_D	6nm
Gate work-function	WF_G	4.5 eV
N-type drain doping concentration	N_D	1018 cm^{-3}
P-type channel doping concentration	N_C	1015 cm^{-3}
P-type source doping concentration	N_S	1020 cm^{-3}

Table 1: A description of the fundamental design parameters utilized in TCAD simulations.

4.3 Advantages

Multiple Tunneling Junctions: By offering various parallel pathways for current conduction, multiple tunneling junctions, which the F-shaped design can include, can improve the on-current.

Better Electrostatic Control: By exerting more electrostatic control over the vertical segments, the extra horizontal segments can enhance the subthreshold swing and switching properties.

Enhanced Current Drive: By making better use of the available device area, the design may be able to enhance the drive current without appreciably expanding the footprint.

Flexibility in Design: The F-shaped structure is adaptable and versatile for a range of applications since it can be tuned for multiple performance criteria.

4.4 Why F-Shaped TFETs better than Conventional TFETs?

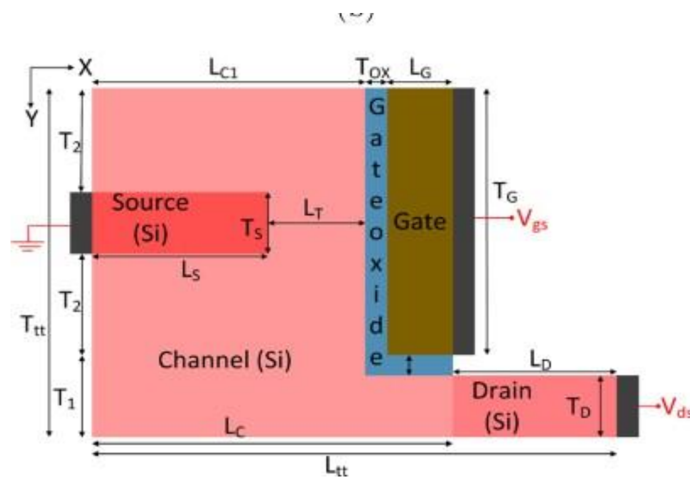


Fig. 4.3: Single-gate F-shaped TFET (SG-F-TFET) with TOX = 1 nm

The F-shaped enhances the gate's control over the channel by incorporating numerous bends and segments. This improves device performance and reduces short-channel effects. Increased scalability due to better electrostatic control enables smaller devices with the same functionality.

The geometry of the F-shaped channel allows for the incorporation of multiple tunneling junctions.

Compared to conventional TFETs, which usually feature a single tunneling area, this increases the total current flow across the device, potentially lowering the threshold voltage and improving the on-state current.

An F-shaped TFET's complex pathway can produce areas with different electric field strengths, which aids in achieving a steeper subthreshold swing which enhances the device's switching capabilities. This allows for quicker transitions between the off and on states, making it essential for low-power applications. Enhanced channel control and various tunneling areas contribute to more effective leakage current suppression, which improves off-state performance, lowers power consumption, and increases the device's energy efficiency.

4.5 Applications

- High-Performance Digital Circuits: F-shaped TFETs are suited for high-speed, low-power digital circuits due to their superior switching properties and increased current drive.
- Analog and RF Circuits: Whereas linearity and noise performance are critical, the enhanced electrostatic control and numerous conduction routes can help these circuits.
- Low-Power Devices: F-shaped TFETs are perfect for low-power applications like wearable electronics and Internet of Things devices because they can function effectively at low voltages.

4.6 Challenges

Complex Fabrication: It may be difficult to create complex F-shaped geometry using conventional lithography and etching procedures, which could raise manufacturing costs.

Device Variability: Because of the intricacy of the design, it can be difficult to guarantee consistent performance across several F-shaped TFETs. This could lead to manufacturing variability.

Integration with Existing Technologies: Integrating F-shaped TFETs with existing CMOS processes requires careful consideration of process compatibility and device architecture.

Chapter 5

Z-Shaped TFET

5.1 Introduction

A Z-shaped Tunnel Field-Effect Transistor is a type of TFET where the channel geometry is shaped like the letter "Z." The purpose of this innovative design is to improve the TFET's performance characteristics for particular applications. With a Z-shaped channel structure that improves its electrical properties, the Z-shaped Tunnel Field-Effect Transistor (Z-TFET) is a cutting-edge TFET design. Superior electrostatic control over the channel region is made possible by this unique Z-shaped design, which also enhances the efficiency of the carrier injection process by adjusting the tunnelling barrier. In order to achieve low-power and high-performance operation, the Z-TFET design offers greater on-current (ION) and a steeper subthreshold swing, which solves some of the intrinsic constraints of conventional TFETs. Additionally, the Z-shaped gate topology helps to increase switching rates and reduce leakage currents. Due to these advancements, Z-TFETs are especially well suited for low-power electronics and next-generation integrated circuit applications, where downsizing and energy efficiency are critical requirements.

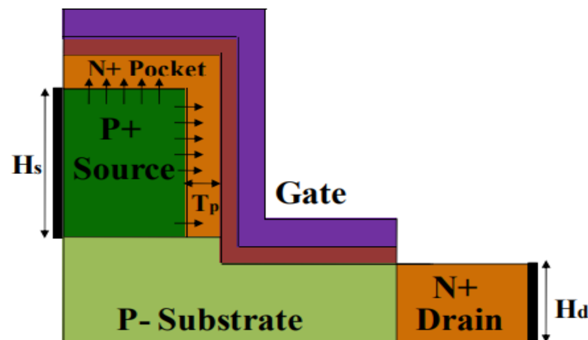


Fig. 5.1: 2-D front view of Z-shaped gate TFET

5.2 Structure

The Z-shaped TFET has a channel made up of alternating vertical and horizontal segments that zigzag like the letter "Z." The device's performance may be enhanced by the numerous tunneling junctions that this design produces along the channel.

Band-to-band tunneling mostly takes place along vertical segments, which act as conduction pathways.

Segments that connect vertical channels horizontally can aid in dispersing current, lowering resistance, and enhancing drive current overall.

Parameters	Abbreviations	Z- shaped TFET
Channel length	L_{ch}	25 nm
Source and drain lengths	L_s/L_d	30nm
Gate work-function	ϕ	4.20 eV
Source doping (p+)	N_s	1e20 cm^{-3}
Drain doping (n+)	N_d	5e18 cm^{-3}
Channel doping (intrinsic)	Nch	1e16 cm^{-3}
Gate oxide thickness	t_{ox}	1 nm
Silicon body thickness	t_{si}	10 nm
Front gate length	L_{fg}	30 nm
Back gate length	L_{bg}	25 nm
Drain voltage	V_{ds}	1.0 V
Gate voltage	V_{gs}	(- 1.0 to 1.5) (- 1.0 to 1.5)V

Table 2: List of parameters considered in the device simulation process

5.3 Advantages

Multiple Tunneling Junctions: By offering several parallel routes for current conduction, the Z-shaped design permits multiple tunneling junctions, which may

improve the on-current.

Enhanced Electrostatic Control: The extra horizontal segments can enhance gate control over the vertical segments, resulting in improved subthreshold swing and switching characteristics.

Enhanced Current Drive: By making the best use of available space, the zigzag construction may be able to raise the drive current without appreciably expanding the device's footprint.

Reduced Short-Channel Effects: To preserve performance in ultra-scaled devices, the zigzag structure can aid in reducing short-channel effects.

5.4 The advantages of source stacking compared to regular source building.

When several source regions are stacked vertically in a TFET design, it is called source stacking. Compared to conventional single-source TFETs, this design provides the following advantages:

Enhanced Tunneling Area: By increasing the tunneling area, source stacking makes it possible for multiple tunneling events to take place at once. This may lead to increase on-currents, which would enhance the TFET's overall performance.

Reduced Series Resistance: By stacking sources, the device's effective series resistance is decreased. Improved energy economy and quicker switching rates are the results of lower series resistance.

Improved Subthreshold Slope: In low-power applications where reducing leakage current is essential, a steeper subthreshold slope may result from the expanded tunneling area.

Increased Current Density: By increasing the TFET's current density, source stacking makes it possible for the device to carry more current in less space.

Enhanced Control Over Threshold Voltage: Designers can modify TFETs for particular applications by manipulating the threshold voltage by changing the number of stacked sources or the doping levels.

Compatibility with Existing Processes: Source stacking is compatible with current manufacturing processes since it can be done using common semiconductor fabrication.

5.5 Why are Z-shaped preferable to conventional TFETs?

Improved Tunneling Efficiency: There are several sudden direction changes and severe bends in the Z-shaped channel. Carriers have a higher chance of tunneling via these steep bends because they can produce regions with strong electric field gradients. When compared to the linear channels found in conventional TFETs, this may lead to a more effective tunneling process.

Improved Subthreshold Swing (SS): Because of the Z-shaped channel's unique geometry, it is possible to obtain steeper subthreshold swings, which improves the device's ability to convert from an off to an on state. This results in faster switching rates and lower power consumption in low-power applications.

Reduced Leakage Current: Better electrostatic control over the channel can be achieved by the Z-shaped design, which can assist in suppressing leakage currents

during the off state. This improves power efficiency and lowers standby power consumption, which is important for battery-powered devices.

Improved Electrostatic Control: The Z-shaped channel design makes it possible for the gate to exert more effective control over the whole length of the channel. Short-channel effects, which are frequent in traditional TFETs that have been shrunk down, are minimized by improved electrostatic control. Better performance and scalability for upcoming technological nodes are the outcome of this.

Lower Threshold Voltage: The Z-shaped channel's high electric field regions can lower the threshold voltage needed to start tunneling, allowing the device to run at lower supply voltages and so lowering power consumption, and enhancing energy efficiency.

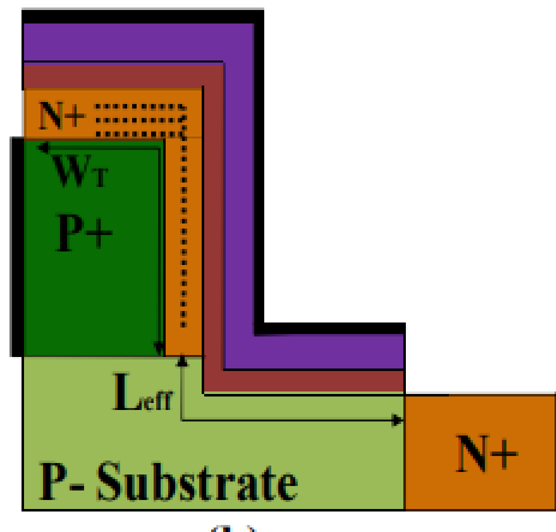


Fig. 5.2: Tunneling width and footprint of proposed ZG-TFET.

5.6 Z-Shaped preferred over F-Shaped TFET.

Subthreshold Swing (SS): The more prominent high electric field regions at the bends may give Z-shaped TFETs an advantage and result in a potentially steeper SS.

DIBL: Both designs provide adequate control; but, because Z-shaped TFETs have sharper control over the channel at the bends, they may perform slightly more effectively than F-shaped TFETs.

On-State Current (Ion): F-shaped TFETs also offer high Ion through various tunneling areas, but not more than z-shaped ones. However, Z-shaped TFETs may produce a greater Ion due to the enhanced tunneling efficiency from the sharp bends.

5.7 Applications

High-Performance Digital Circuits: Z-shaped TFETs are suited for high-speed, low-power digital circuits due to their superior switching properties and increased current drive.

Analog and RF Circuits: Where linearity and noise performance are crucial, analog and RF circuits can benefit from enhanced electrostatic control and numerous conduction channels.

Low-Power Devices: Z-shaped TFETs are perfect for low-power applications like wearable electronics and Internet of Things devices because they can function effectively at low voltages.

5.8 Challenges

Complex Fabrication: Production costs may rise if sophisticated lithography and etching procedures are needed to fabricate the complex Z-shaped geometry.

Device Variability: The complexity of the design can make it difficult to achieve consistent performance across several Z-shaped TFETs, which could lead to manufacturing variability.

Chapter 6

Results and Conclusions

6.1 Analysis of 2D F-shaped TFET

As per the section 2.3, the basic simulation of F shaped TFET has been done. From the output files we get str file and log file. The str file gives the structure of simulated TFET with the parameters considered in above section 2.3.1, as shown in figure 6.1. And the log file gives the drain current vs gate voltage curve, as shown in fig 6.2.

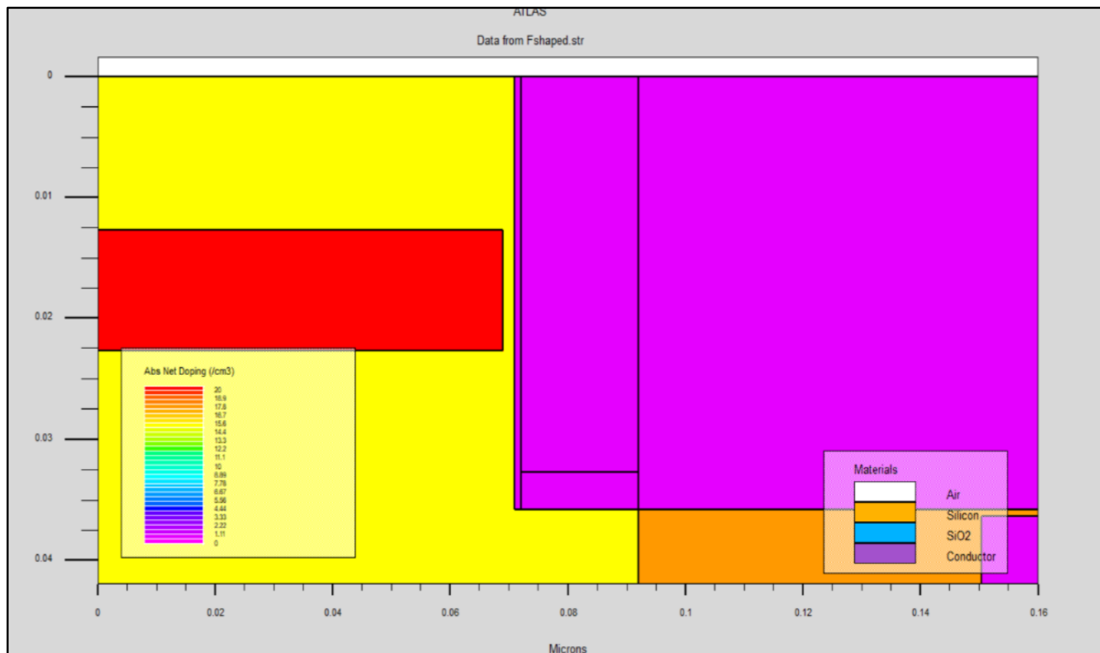


Fig 6.1: showing the structure of proposed 2D F shaped design

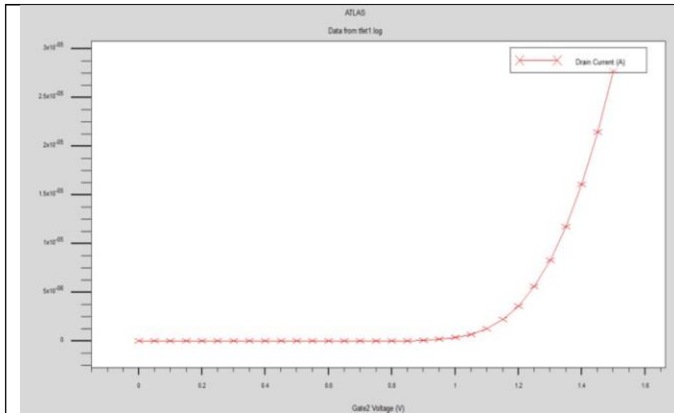


Fig 6.2: Graph showing the change in current (I) with the gate voltage (V)

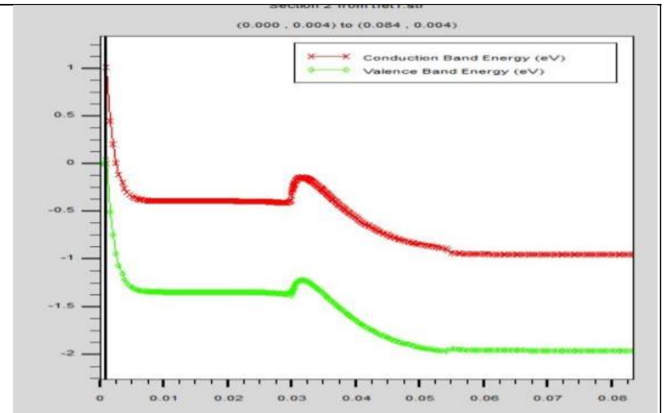


Fig 6.3: Showing the energy band diagram for the F-shaped TFET

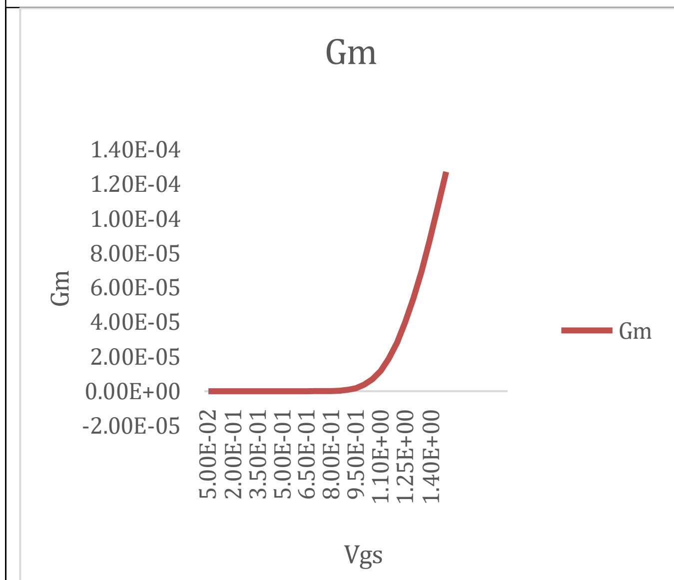


Fig 6.4: Graph showing the G_M curve

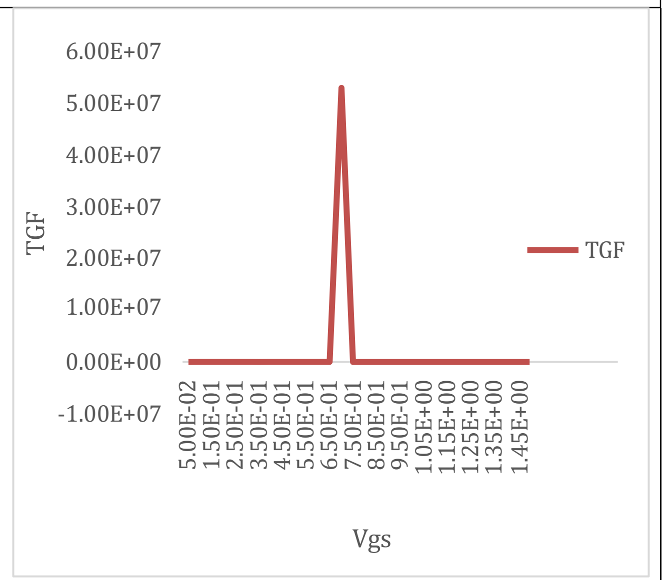


Fig 6.5: Showing the T_{GF} curve

The Details on GM curve and TFG curve:

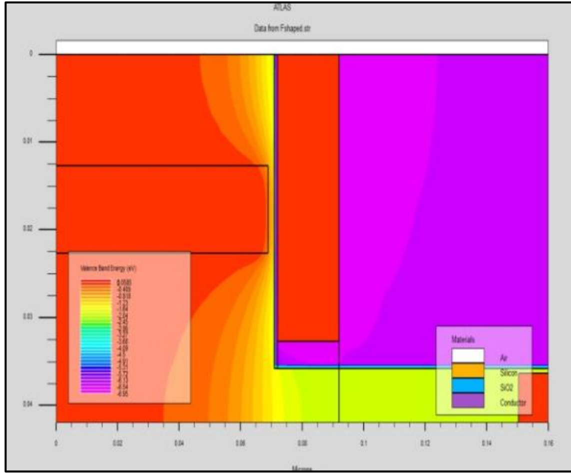


Fig6.6: figure showing the valence band contours.

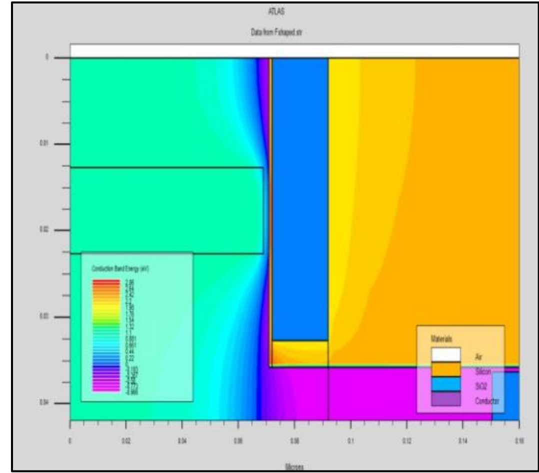


Fig 6.7: Figure showing the conduction Band contours.

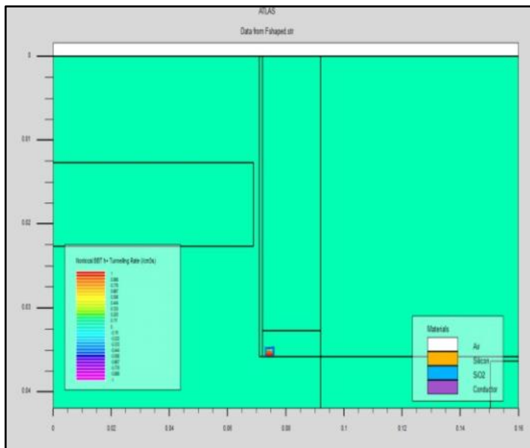


Fig6.8: figure showing the Non local BBT h+ tunneling rate contours.

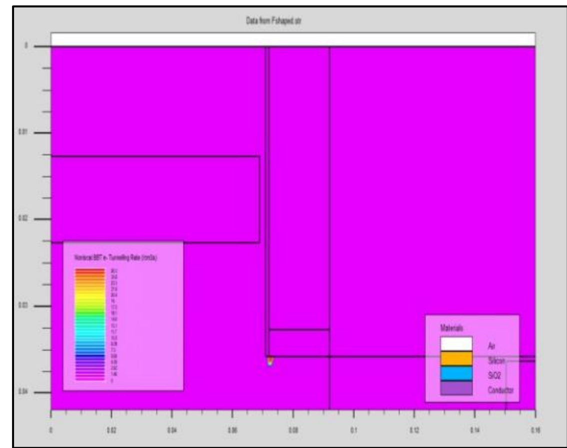
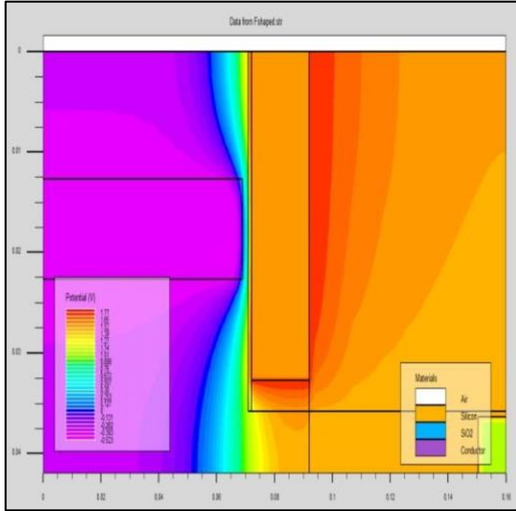


Fig6.9: Figure showing the Non local BBT e+ tunneling rate contours.



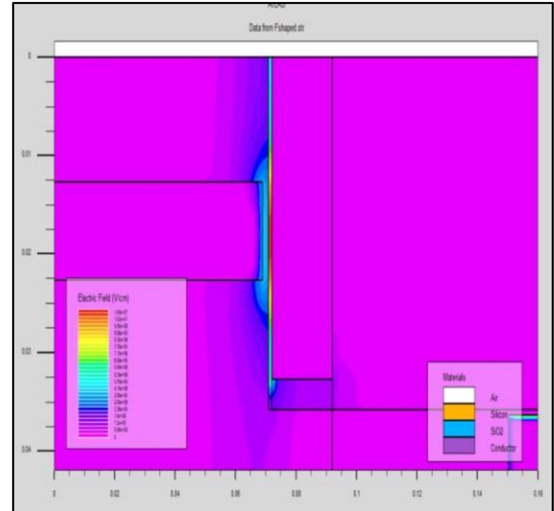


Fig6.10: Figure showing the potential contours.

Fig6.11: Figure showing the Electric. field contours

From this we have extracted potential contours and electric field contours which are shown in below figures 6.6 to 6.11. The electrostatic potential inside the device is represented by the Potential Barrier Contours. It displays the potential variation throughout the semiconductor structure, suggesting the existence of possible wells or barriers. For a TFET to regulate the flow of charge carriers across the channel, the potential barrier at the semiconductor-oxide interface is essential. The vector plots or streamlines that show the device's internal current flow's direction and magnitude are represented by current flow lines. It offers information on the routes that charge carriers—holes or electrons—take as they go from the source to the drain terminals. Comprehending the flow lines of current is crucial for maximizing the efficiency of devices and reducing undesired consequences like leakage currents.

Output showing below is the extracted values of Subthreshold voltage. The main thing we are focussing here is the subthreshold voltage which should be less than 60mV/dec for ideal TFets. And we are getting of the almost same order.

```
ATLAS>
EXTRACT> init inf="ffet.log"
EXTRACT> extract name="vt" (xintercept (maxslope (curve (abs (v."gate") ,abs (i."drain"))))        - abs(ave(v."drain"))/2.0)
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EXTRACT> extract name="subvt"        1.0/slope(maxslope(curve(abs(v."gate") ,log10(abs(i."drain")))))
subvt=0.0271382 V/decade
EXTRACT> quit
log off
ATLAS>
ATLAS> quit

ATLAS version 5.26.1.R finished at Sat Jun 01 23:59:27 2024
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6.2 Analysis of 2D Z shaped TFET

As per the section 2.3, the basic simulation of F shaped TFET has been done. From the output files we get str file and log file. The str file gives the structure of simulated TFET with the parameters considered in above section 2.3.1, as shown in figure 6.1. And the log file gives the drain current vs gate voltage curve, as shown in fig 6.2.

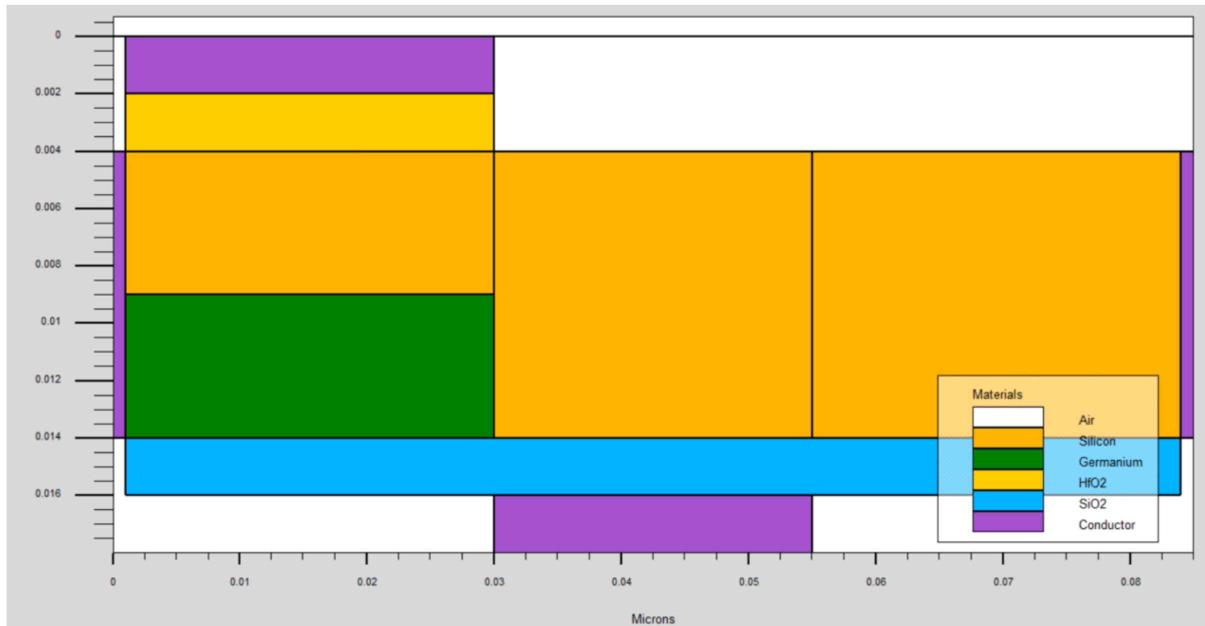


Fig 6.12: showing the structure of proposed 2D Z shaped design

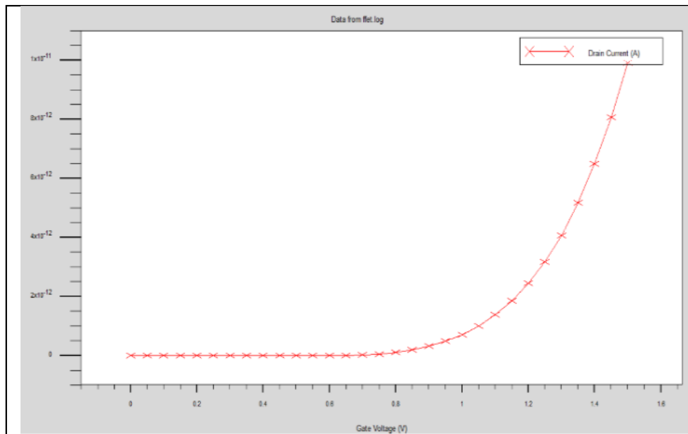


Fig 6.13: Graph showing the change in current (I) with the gate voltage (V)

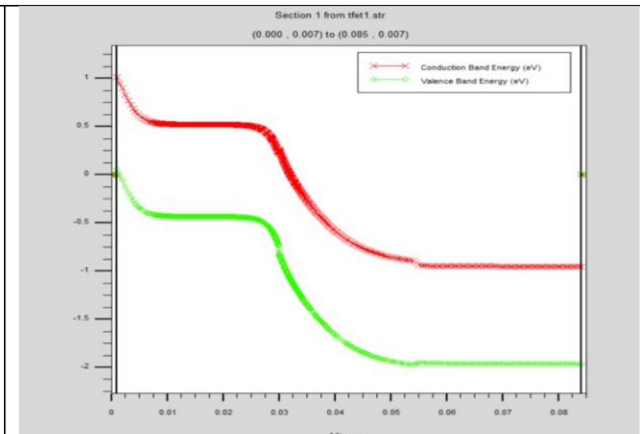
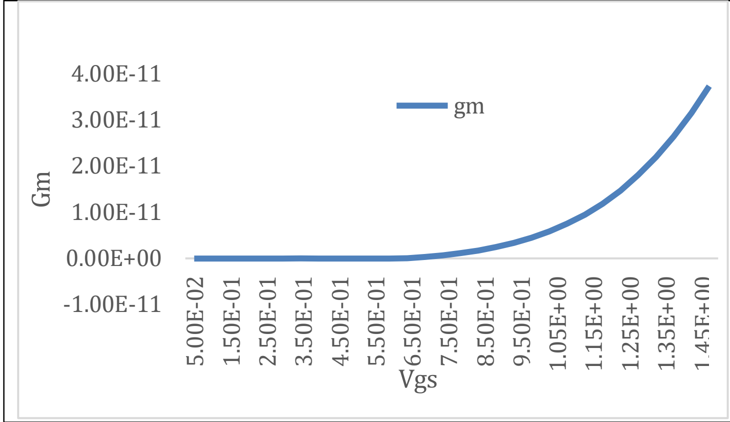
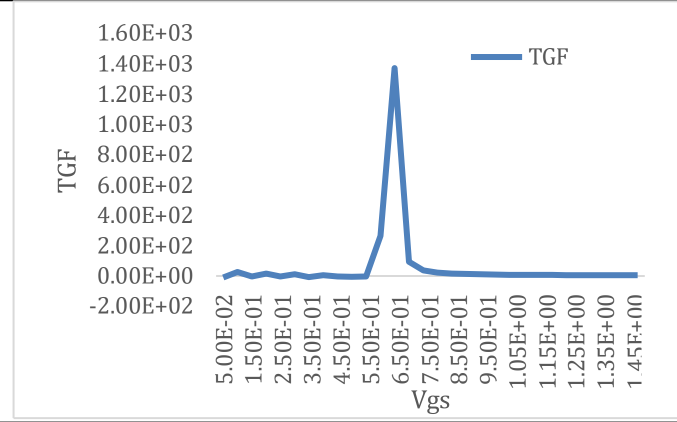


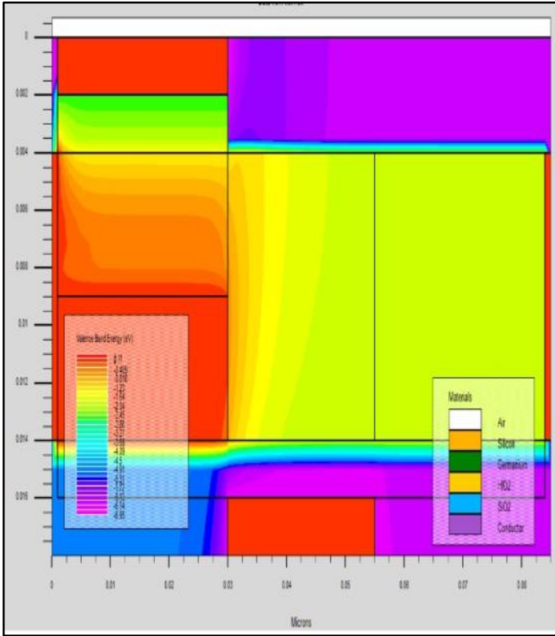
Fig 6.14: Showing the energy band diagram for the Z shaped TFET



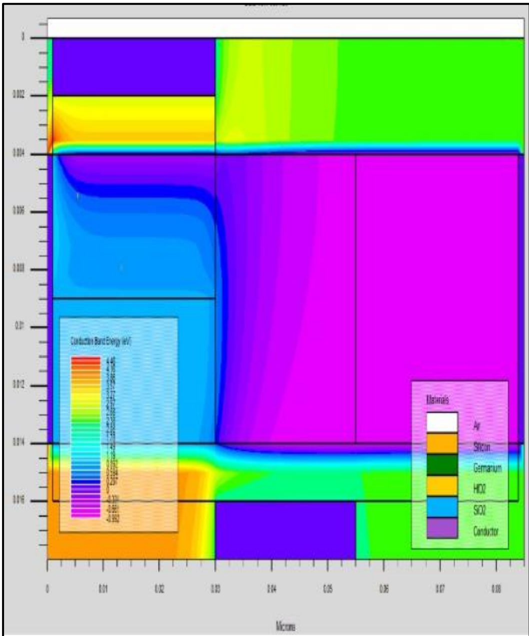
<u>Fig 6.15:</u> Graph showing the GM curve



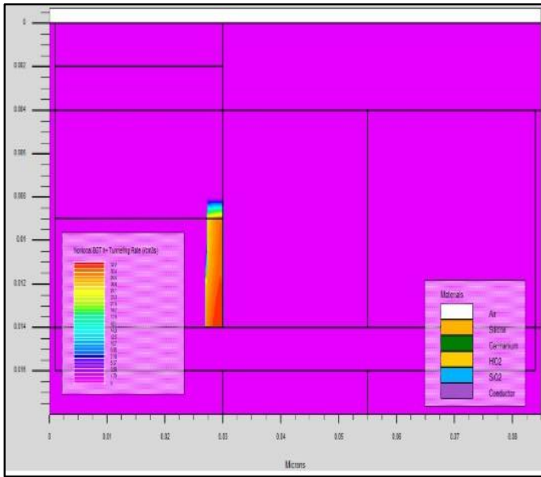
<u>Fig 6.16:</u> Showing the TGF curve



<u>Fig6.17:</u> figure showing the valence band conduction band contours.



<u>Fig 6.18:</u> Figure showing the contours.



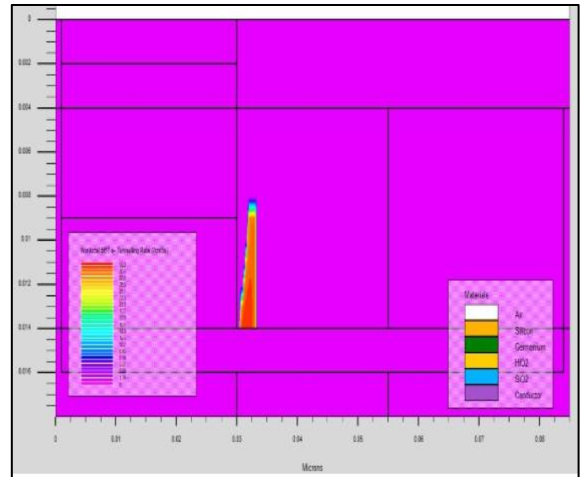
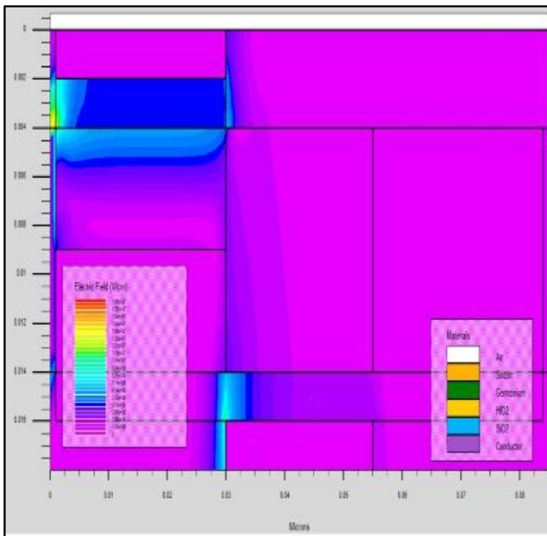


Fig 6.19: figure showing the Non local BBT h+ tunneling rate contours.

Fig 6.20: Figure showing the Non local BBT e+ tunneling rate contours.



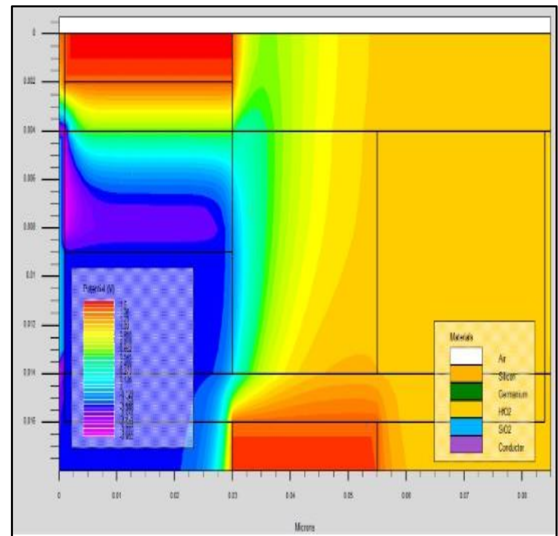


Fig6.21: figure showing the potential contours.

Fig 6.22: Figure showing the Electric. field contours

From this we have extracted potential contours and electric field contours which are shown in below figures 6.17 to 6.22. The electrostatic potential inside the device is represented by the Potential Barrier Contours. It displays the potential variation throughout the semiconductor structure, suggesting the existence of possible wells or barriers. For a TFET to regulate the flow of charge carriers across the channel, the potential barrier at the semiconductor-oxide interface is essential. The vector plots or streamlines that show the device's internal current flow's direction and magnitude are represented by current flow lines. It offers information on the routes that charge carriers—holes or electrons—take as they go from the source to the drain terminals. Comprehending the flow lines of current is crucial for maximizing the efficiency of devices and reducing undesired consequences like leakage currents.

```
ATLAS>
EXTRACT> init inf="tfet1.log"
EXTRACT> extract name="vt" (xintercept (maxslope (curve (abs (v."gate") ,abs (i."drain"))))        - abs(ave(v."drain"))/2.0)
vt=0.780995 V
EXTRACT> extract name="subvt"        1.0/slope(maxslope(curve(abs(v."gate") ,log10(abs(i."drain")))))
subvt=0.00778502 V/decade
EXTRACT> quit
log off
ATLAS>
ATLAS> quit

ATLAS version 5.26.1.R finished at Sun Jun 02 00:01:44 2024
```

Output showing above is the extracted values of Subthreshold voltage. The main thing we are focussing here is the subthreshold voltage which should be less than 60mV/dec for ideal TFets. And we are getting of the almost same order.

6.3 Conclusion

We have made computed the subthreshold voltage for F shaped TFET and Z shaped TFET and it is noted that for TFET it is less than MOSFETs. For the F shaped TFET it came upto 27.12 mV/decade and for the Z shaped it be barely 7.7 mV/decade.
One important characteristic that shows how well a Tunnel Field-Effect Transistor (TFET) can flip from the off-state to the on-state is its subthreshold slope (SS). For low-power applications, a steeper (lower) subthreshold slope is preferable since it enables the transistor to come on faster and at lower gate voltages. Because of its special gate design that offers better electrostatic control over the channel region, the Z-shaped TFET often exhibits a lower subthreshold slope than the F-shaped TFET. Here are several explanations for why this could be the case: Improved Gate Control: When compared to an F-shaped gate structure, a Z-shaped gate structure can offer the channel region a better electrostatic coupling. This enhanced control facilitates more efficient modulation.

Diminished Short-Channel Effects: The Z-shaped gate's geometry can aid in more effective electric field confinement, minimizing short-channel effects, which frequently deteriorate the subthreshold slope. This indicates that even when the device dimensions are reduced, the Z-TFET can continue to have a higher subthreshold slope.

Optimized Tunneling Junction: Compared to the F-shaped design, the Z-shaped gate might provide a more abrupt and regulated tunneling junction. A decreased subthreshold swing is directly related to an efficient tunneling process, which can be facilitated by a sharper junction.

Symmetric Electric Field Distribution: A more symmetric and consistent electric field distribution across the channel may be the outcome of the Z-shaped structure, which

aids in the achievement of more effective switching behavior. This consistency can improve the leakage currents.

6.4 Future Directions

Progress in the development of F-shaped and Z-shaped Tunnel Field-Effect Transistors (TFETs) is expected to yield notable improvements in their functionality and suitability for use in energy-efficient, low-power electronic devices. In order to achieve better electrical characteristics and lower leakage currents for F-shaped TFETs, research is likely to concentrate on optimizing the gate architecture to further improve electrostatic control and tunneling efficiency. Novel materials, such as high-k dielectrics or two-dimensional materials, like graphene and transition metal dichalcogenides (TMDs), may also be incorporated. Furthermore, the development of fabrication techniques like atomic layer deposition and accurate doping will be essential to reducing the device's dimensions without compromising its functionality. Future research on Z-shaped TFETs might focus on optimizing the Z-shaped gate design to further lower the subthreshold slope and improve the homogeneity of the electric field distribution. Furthermore, improvements in simulation and modeling tools will help in comprehending and reducing the impacts of small channels as well as improving the architecture of the device to maximize on-current and minimize off-state leakage. Further investigation into strain engineering and heat management techniques is necessary to guarantee the stability and dependability of both F-shaped and Z-shaped TFETs at nanoscale dimensions. Together, these developments will push TFET technology's limits and establish it as a pillar in the creation of next-generation semiconductor devices that put energy efficiency and miniaturization first.

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Total Pages: 50

Name of the Supervisor: Dr. Rishu Chaujar

Department: Department of Applied Physics

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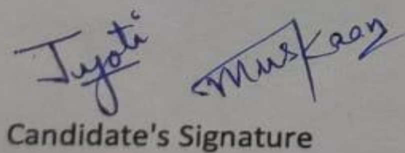

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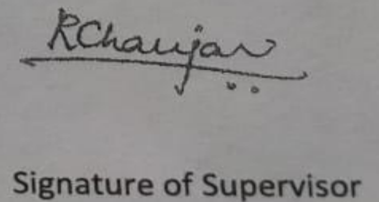

Signature of Supervisor

PAPER NAME

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WORD COUNT

6787 Words

CHARACTER COUNT

38092 Characters

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50 Pages

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