DESIGN AND OPTIMIZATION OF JUNCTIONLESS-ACCUMULATION-MODE GATE-STACK GATE-ALL-AROUND FINFET FOR RF AND BIOSENSOR APPLICATIONS

Thesis Submitted by

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Dedicated to

Lord Kṛṣṇa

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CERTIFICATE

This is to certify that the thesis titled "***Design and Optimization of Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around FinFET for RF and Biosensor Applications***" is being submitted by ***MR. BHAVYA KUMAR*** with registration number ***2K18/PHD/AP/17*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Physics. The work embodied in this thesis is a record of bonafide research work carried out by me in the Microelectronics Research Lab, Department of Applied Physics, Delhi Technological University (Formerly Delhi College of Engineering), New Delhi, under the guidance of ***PROF. RISHU CHAUJAR***. It is further certified that this work is original and has not been submitted in part or fully to any other University or Institute for the award of any degree or diploma.

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īśvaraḥ paramaḥ kṛṣṇaḥ sac-cid-ānanda-vigrahaḥ
anādir ādir govindaḥ sarva-kāraṇa-kāraṇam *(Brahma-Samhita 5.1)*

First and foremost, I humbly offer my obeisance to the ***Supreme Personality of Godhead****,* ***Kṛṣṇa****, who is the supreme cause of all causes, as concluded in the Brahma-Samhita by Lord Brahma himself. It is by His (****Kṛṣṇa****) grace that I have been blessed with the privilege of expressing my devotion. I acknowledge with utmost humility that whatever I am today, every blessing and accomplishment is a manifestation of His divine will. So, as we traverse the path of life, it is our sacred duty to chant His holy name to accomplish the purpose of this human life.*

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ABSTRACT

Design and Optimization of Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around FinFET for RF and Biosensor Applications

FinFET has emerged as the most desirable alternative to MOSFETs and is the driving force behind the current integrated circuit (IC) industry, which optimizes short-channel effects (SCEs) to achieve exceptional scalability, augment battery longevity, and minimize power consumption. FinFET ensures superior electrostatic control with three gates surrounding the fin and offers a larger packing density due to its three-dimensional construction. In this thesis, Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around (JAM-GS-GAA) FinFET architecture has been rigorously examined and compared with different structures using the SILVACO ATLAS 3D simulator. The analysis exemplified that JAM-GS-GAA FinFET overcomes the challenges faced by conventional FinFET, such as manufacturing complexity, reliability concerns, variability issues, etc. In addition, approaches such as dual-k spacer engineering have been used to further improve the device's performance.

In the beginning, a comprehensive study of the analog and RF characteristics of JAM-GS-GAA FinFET has been analyzed with the optimization of the fin aspect ratio at the sub-nano level to achieve a high-performance transistor. It has been found that the analog and RF performance of the JAM-GS-GAA FinFET device improved significantly compared to conventional FinFET because of the enhanced gate control on the channel and reduced SCEs. When compared to conventional FinFET, parameters like switching (I_{on}/I_{off}) ratio, gain transconductance frequency product (GTFP), and gain frequency product (GFP) increased by 31, 3.37, and 2.73 times, respectively, for the JAM-GS-GAA FinFET device. It has also been analyzed that the proposed device with the highest fin aspect ratio configuration exhibits the most improved analog and RF performance compared to the other lower fin aspect ratio configurations. The device with a high fin aspect ratio exhibits a considerable reduction of 94.72% in leakage current (I_{off}) and 14.90% in subthreshold swing (SS), along with notable improvements in other metrics.

Further, the performance of the proposed JAM-GS-GAA FinFET device has been compared with other existing devices on different technologies at a fixed gate length of 10 nm to evaluate its significance. Then, the reliability issues of the proposed device have been explored by considering the impact of temperature and gate electrode work function in terms of static, analog, RF, linearity, and harmonic distortion characteristics. The study's findings indicate that the JAM-GS-GAA FinFET demonstrates satisfactory reliability in the face of temperature fluctuations and changes in the gate electrode work function. The static, linearity, and harmonic distortion metrics do not change much as the temperature increases from 300 K to 500 K, while the peak values of parameters like g_m, f_T, TFP, g_{m2}, g_{m3}, VIP2, VIP3, HD2, and HD3 are approximately the same for all gate electrode work functions.

Moreover, the impact of dual-k spacer (SiO_2 + HfO_2) engineering on the JAM-GS-GAA FinFET has been investigated to further enhance the performance of the proposed device and make it suitable for sub-10 nm RFIC circuits. Different configurations such as conventional tri-gate JAM-GS-FinFET, JAM-GS-GAA-FinFET without a spacer, JAM-GS-GAA-FinFET with single-k spacers, and the proposed JAM-GS-GAA-FinFET with dual-k spacer have been examined. The dual-k spacer configuration uses HfO_2 as a high-k spacer for the inner layer and SiO_2 as a low-k spacer for the outer layer. Due to the fringing field effects, the dual-k spacer configuration improves the electron velocity, electric field, surface potential, and energy band profiles. Thereby increasing the ON-state (I_{on}) current of the dual-k spacer configuration by 35.34%, I_{on}/I_{off} ratio by approximately 10^2 times, transconductance (g_m) by 24.03%, transconductance generation factor (TGF) by 39.12%, quality factor (QF) by 46.75%, while decreasing the I_{off} by over 76 times and SS by 15.47% compared to the conventional FinFET configuration.

Further, the parasitic capacitances and small-signal behavior of JAM-GS-GAA FinFET have been inspected to assess the efficacy of GaAs as a fin material. Capacitance-related FOMs like gain bandwidth product (GBP) and transconductance frequency product (TFP) have also been analyzed for switching applications. It has been noticed that SCEs and parasitic capacitances reduced considerably, and the peak value of both GBP and TFP increased by 10 times with the incorporation of GaAs. Further, the effect that parameters like gate length (L_g), channel doping (N_{Ch}), fin width (W_{Fin}), gate electrode work function (ϕ_m), and temperature (T) have on the parasitic capacitances and scattering (S) parameters

of GaAs JAM-GS-GAA FinFET across the terahertz (THz) frequency range have been examined. The results confirm that the parasitic capacitances decreased appreciably for a device with a shorter L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m, whereas, at extremely high frequencies, the S-parameters improved considerably for a device with a larger L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m.

After analyzing the electrical properties of the proposed device, the GaAs JAM-GS-GAA FinFET has been utilized to accomplish the electrical identification of the MDA-MB-231 breast cancer cell by monitoring the device switching ratio. The switching ratio-based device sensitivity has been evaluated by analyzing the drain current characteristics for air (cell-free), MCF-10A (healthy), and MDA-MB-231 (cancerous cells), and it comes out to be 47.78% and 99.72% for healthy and cancerous breast cells, respectively. The sensor has also been assessed for its reproducibility, stability, and capability to distinguish between viable and non-viable cells and was found to be repeatable and adequately stable, with settling times of 55.51 ps for the MDA-MB-231 cell, 60.80 ps for the MCF-10A cell, and 71.58 ps for air. Further, the possibility of early detection of cancerous breast cells using Bruggeman's model and the effect of biomolecule occupancy and frequency fluctuations on the device's sensitivity has been investigated. The impact of the physical parameters, like fin height, fin width, gate electrode work function, channel doping, temperature, and drain voltage, on the device's sensitivity has been explored. Finally, the GaAs JAM-GS-GAA FinFET sensor was compared to already existing breast cancer sensors, and it was found that the proposed sensor performed much better.

Thus, JAM-GS-GAA FinFET can be considered a promising candidate for use in low-power, analog, RF, and biosensor applications due to its high switching ratio, lower leakage current, better reliability in terms of temperature and gate electrode work function, superior static, analog, and RF performance, suppressed SCEs and parasitic capacitances, and high sensitivity electrical detection of MDA-MB-231 breast cancer cells.

LIST OF FIGURES

LIST OF TABLES

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ARTICLES IN INTERNATIONAL REFEREED JOURNALS (7):

1. **B. Kumar** and R. Chaujar, "Analog and RF performance evaluation of junctionless accumulation mode (JAM) gate stack gate all around (GS-GAA) FinFET," ***Silicon***, vol. 13, pp. 919-927, 2021. **(IF – 3.4)**
2. **B. Kumar** and R. Chaujar, "TCAD temperature analysis of gate stack gate all around (GS-GAA) FinFET for improved RF and wireless performance," ***Silicon***, vol. 13, pp. 3741-3753, 2021. **(IF – 3.4)**
3. **B. Kumar** and R. Chaujar, "Numerical study of JAM-GS-GAA FinFET: A fin aspect ratio optimization for upgraded analog and intermodulation distortion performance," ***Silicon***, vol. 14, pp. 309-321, 2022. **(IF – 3.4)**
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5. **B. Kumar**, M. Sharma, and R. Chaujar, "Gate electrode work function engineered JAM-GS-GAA FinFET for analog/RF applications: Performance estimation and optimization," ***Microelectronics Journal***, vol. 135, 105766, 2023. **(IF – 2.2)**
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1. **B. Kumar** and R. Chaujar, "Fin aspect ratio optimization of novel junctionless gate stack gate all around (GS-GAA) FinFET for analog/RF applications," ***Microelectronics, Circuits and Systems, Lecture Notes in Electrical Engineering***, vol. 755, pp. 59-67, 2021.
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1. **B. Kumar**, A. Kumar, and R. Chaujar, "The effect of gate stack and high-k spacer on device performance of a junctionless GAA FinFET," ***IEEE VLSI Device, Circuit and System Conference (VLSI-DCS)***, Kolkata, India, pp. 159-163, 2020.

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3. **B. Kumar**, M. Sharma, and R. Chaujar, "Dual-k spacer JAM-GS-GAA FinFET: A device for low power analog applications," ***IEEE Silchar Subsection Conference (SILCON)***, Silchar, India, pp. 1-5, 2022.

4. **B. Kumar**, M. Sharma, and R. Chaujar, "Scattering parameter analysis of gate stack gate all around (GS-GAA) FinFET at THz for RF applications," ***8th International Conference on Signal Processing and Communication (ICSC)***, Noida, India, pp. 653-658, 2022.

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2. M. Sharma, **B. Kumar**, and R. Chaujar, "Simulation investigation of double-heterostructure T-gate HEMT with graded back-barrier engineering for improved RF performance," ***Materials Today: Proceedings***, vol. 71, no. 2, pp. 155-159, 2022.

3. M. Sharma, **B. Kumar**, and R. Chaujar, "Polarization induced doping and high-k passivation engineering on T-gate MOS-HEMT for improved RF/microwave performance," ***Materials Science and Engineering: B***, vol. 290, 116298, 2023. **(IF – 3.6)**

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1. N. Gupta, A. Kumar, R. Chaujar, **B. Kumar**, and M.M. Tripathi, "Gate engineered GAA silicon-nanowire MOSFET for high switching performance," ***IEEE VLSI Device, Circuit and System Conference (VLSI-DCS)***, Kolkata, India, pp. 258-262, 2020.

2. M. Sharma, **B. Kumar**, and R. Chaujar, "Effect of gate oxide material variability on the analog performance of T-Gate GaN-MOS-HEMT with graded buffer," ***7th International Conference on Signal Processing and Communication (ICSC)***, Noida, India, pp. 316-320, 2021.

3. M. Sharma, **B. Kumar**, and R. Chaujar, "Linearity analysis of T-gate HEMT with graded back-barrier for wireless applications," ***IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)***, Bangalore, India, pp. 1-5, 2022.

TABLE OF CONTENTS

1

CHAPTER

Introduction

- *This chapter presents a thorough background of the research work, with a primary emphasis on the importance of FinFET in the contemporary integrated circuit industry.*
- *The problems related to MOSFET scaling and the different short-channel effects have been comprehensively reviewed in this chapter.*
- *After that, this chapter encompasses an examination of several engineering methods, such as junctionless engineering, gate engineering, and dual-k spacer engineering, as well as advanced FET architectures, including SOI MOSFET, TFET, and CNTFET, as documented in different research publications, for mitigating short-channel effects.*
- *Furthermore, the chapter discusses FinFET as a potential approach to address the limitations. The chapter then progresses toward the fundamental architecture of FinFETs, categorization, basic working principles, possible benefits, and challenges confronted by FinFET technology.*
- *Finally, the chapter provides an overview of the thesis research objectives, followed by a summary of all the chapters.*

1.1 BACKGROUND

Jack Kilby independently created the integrated circuit (IC) idea in 1958 while working at Texas Instruments [1]. This breakthrough transformed the world of electronics by allowing the fabrication of multiple electronic components on a single semiconductor substrate. However, Moore's law drove the downscaling of CMOS technology, which genuinely propelled the growth of ICs. Moore's law, named after Gordon Moore, one of Intel's co-founders, is the observation that the number of transistors on a chip doubles every two years [2]. **Figure 1.1** confirms that this observation has held for over half a century and has evolved into a fundamental concept within the semiconductor industry [3]. The performance of ICs significantly improved while their cost and power consumption decreased as transistors became smaller and more densely packed on a single chip. This trend has facilitated the widespread use of diverse electronic gadgets, from personal computers and smartphones to advanced medical equipment and autonomous vehicles. This remarkable advancement in IC technology has magically transformed our daily lives, and continuous device scaling is required to maintain ongoing advances in IC technology.

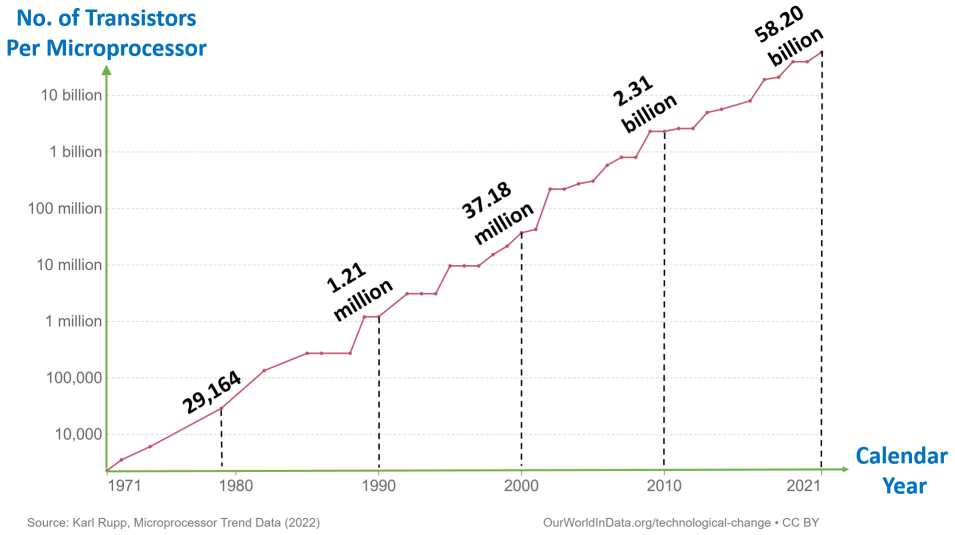

Figure 1.1: Log plot of transistor counts per microprocessor against calendar years [3].

However, maintaining this downscaling in the nanometer range is extremely difficult due to limitations such as increased leakage current, higher power consumption, heat dissipation issues, quantum effects, and short-channel effects (SCEs) [4-6]. The drain potential begins to affect the electrostatics of the channel in deeply scaled MOSFETs, resulting in an elevated leakage current between the drain and the source. Besides, transistors are also susceptible to significant SCEs, such as subthreshold slope (SS), drain-induced barrier lowering (DIBL), and threshold voltage (V_{th}) roll-off, which play a role in the loss of power [7-10]. Multiple device topologies such as multi-gate MOSFET [11], TFETs [12], HEMTs [13, 14], and FinFETs [15-17] have been suggested to alleviate these difficulties. FinFET has emerged as the most desirable alternative to MOSFETs and is the driving force behind the current IC industry, which optimizes SCEs to achieve exceptional scalability, augment battery longevity, and minimize power consumption [18, 19]. **Figure 1.2** demonstrates the performance of FinFETs over conventional planar MOSFETs. Leakage current and transistor gate delay have been reduced significantly for the FinFET structure over the planar MOSFET architecture [20]. FinFET ensures superior electrostatic control with three gates surrounding the fin. Finally, FinFET offers a larger packing density due to its three-dimensional construction [21].

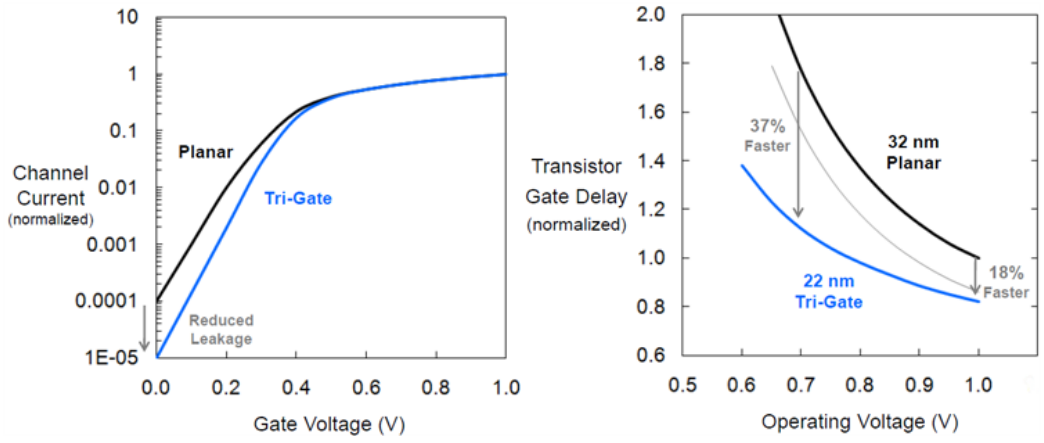

Figure 1.2: Tri-gate FinFET performance comparison with planar transistors [20].

1.2 SCALING OF MOSFET

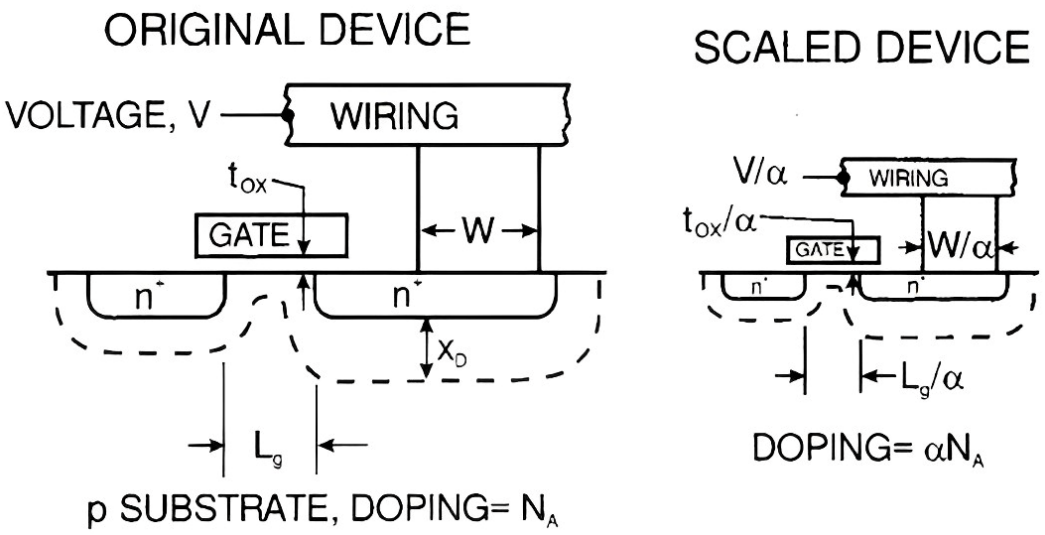

Figure 1.3: Constant field scaling principles for MOSFETs and ICs [22].

The primary objective of VLSI/ULSI electronics is to increase the switching speed of logic gates while decreasing the cost per logic function. Achieving this objective by reducing the dimensions of the devices has led to the development of new generations of ICs [23]. The size of MOS transistors has been intentionally reduced systematically to obtain reduced power dissipation, improved switching speed, and increased circuit density [24]. Dennard et al. [25] were the first to propose scaling to reduce the size of a device without compromising the voltage-current characteristics of large devices. Constant field scaling and constant voltage scaling are two prevalent forms of scaling. The scaling principles outlined by Dennard are referred to as constant field scaling. Constant field scaling involves a reduction of all dimensions and voltages by a scaling factor α(>1), resulting in a constant electric field within the device to that of the original device [22, 26, 27], as shown in **Figure 1.3**. Scaling the constant field across the channel results in the most significant decrease in the power-delay product of an individual transistor. Nevertheless, the reduction of the minimum feature size necessitates the reduction of the power supply voltage. The issue

mentioned above is not present with constant voltage scaling, making it the favored scaling technique due to its ability to maintain voltage compatibility with previous circuit technology. Constant voltage scaling has the drawback of increasing the electric field as the minimum feature length decreases. Consequently, these phenomena result in velocity saturation, leakage current augmentation, breakdown voltage reduction, and mobility degradation.

Scaling down offers the subsequent benefits [28]:

1. Fabrication of more circuits per silicon wafer contributes to reduced-cost ICs.
2. Decreased parasitic capacitances and hence increased speeds of ICs.
3. Reduced power supply voltages and power consumption.

Nevertheless, scaling down has its own set of challenges [29]:

1. Raised electric field in oxide and increased gate leakage current.
2. Power consumption, both static and dynamic.
3. Possible overheating and evaporation.

1.3 SHORT-CHANNEL EFFECTS

The significant reduction in the transistor's size gives rise to notable challenges, including undesired short-channel effects (SCEs). SCEs refer to the phenomena that occur when the channel length of the MOSFET approaches the size of the depletion layer width of the source and drain junctions. As the channel length decreases, the SCEs become more prominent, and the transistor's behavior changes significantly, affecting the transistor's performance, modeling, and reliability. SCEs are a significant concern in modern IC design, with threshold voltage roll-off, drain-induced barrier lowering, and hot-carrier effects being the most pronounced.

1.3.1 Threshold Voltage Roll-off

The threshold voltage (V_{th}) roll-off phenomenon refers to the reduction in the threshold voltage of a MOSFET as its channel length decreases. As transistors are scaled down to smaller sizes, the efficacy of the electric field in regulating the movement of charge carriers (electrons or holes) inside the channel area diminishes. Consequently, the value of threshold voltage in a short-channel device exhibits a reduction compared to the threshold voltage of a long-channel device. Threshold voltage roll-off is defined mathematically as the difference between the threshold voltages of a short-channel MOSFET and a long-channel MOSFET [30].

1.3.2 Drain-Induced Barrier Lowering

This phenomenon may be comprehensively understood by examining the potential barrier profile that an electron must surmount to traverse from the source to the drain. In the absence of external biasing ($V_{gs} = 0$ and $V_{ds} = 0$), the presence of a potential barrier impedes the movement of electrons from the source to the drain. The gate voltage reduces the energy barrier enough to enable the movement of electrons, as shown in **Figure 1.4(a)**. Ideally, this would be the only voltage that would influence the barrier. Nevertheless, as the channel is shortened, a greater V_{ds} causes an expansion of the drain depletion zone, reducing the potential barrier, as reflected in **Figure 1.4(b)**. Even when the gate-source voltage is below the threshold voltage, the progressive decrease of the potential barrier facilitates the movement of electrons between the source and the drain. Hence, the phenomenon is appropriately referred to as drain-induced barrier lowering (DIBL) [31]. Under these specified circumstances, the current that flows inside the channel is called the sub-threshold current [32].

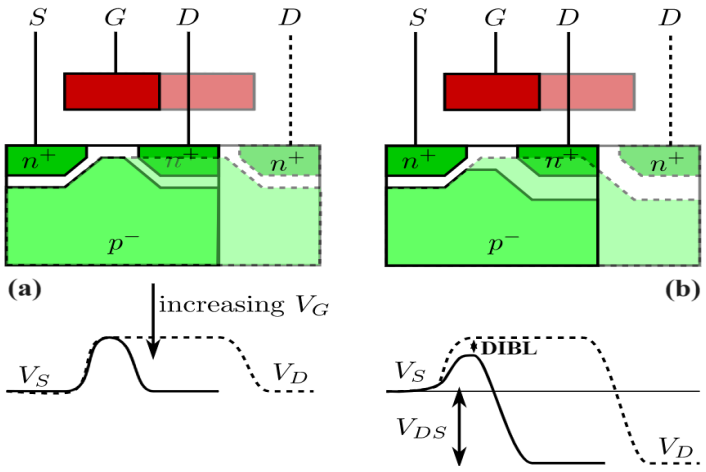

Figure 1.4: Drain-induced barrier lowering [31].

1.3.3 Hot-Carrier Effects

Hot-carrier effects (HCEs) include a range of phenomena that manifest when charge carriers (electrons or holes) acquire surplus energy due to the application of high voltages or electric fields, as shown in **Figure 1.5**. These energetic carriers can potentially harm the transistor and decrease its performance over time. Hot-carrier injection (HCI) and channel hot-carrier injection (CHCI) are the most common HCEs. Hot-carriers might remain within the channel or enter the gate oxide in HCI. In CHCI, however, the hot-carriers do not reach the gate oxide layer but instead gain enough energy to impact the transistor channel. Impact ionization is a phenomenon associated with HCI that takes place when the kinetic energy of the carriers surpasses the bandgap energy of the semiconductor material. This process disrupts the covalent bond through carrier-carrier collisions and produces electron-hole pairs contributing to the substrate current [33]. Hot-electron injection (HEI) is a specific form of HCI, and it occurs when hot electrons acquire sufficient energy to penetrate the gate oxide by overcoming the potential barrier at the gate oxide-semiconductor interface. Upon entering the gate oxide, they can get stuck in oxide defects, causing alterations to the device's threshold voltage and transfer characteristics [34, 35].

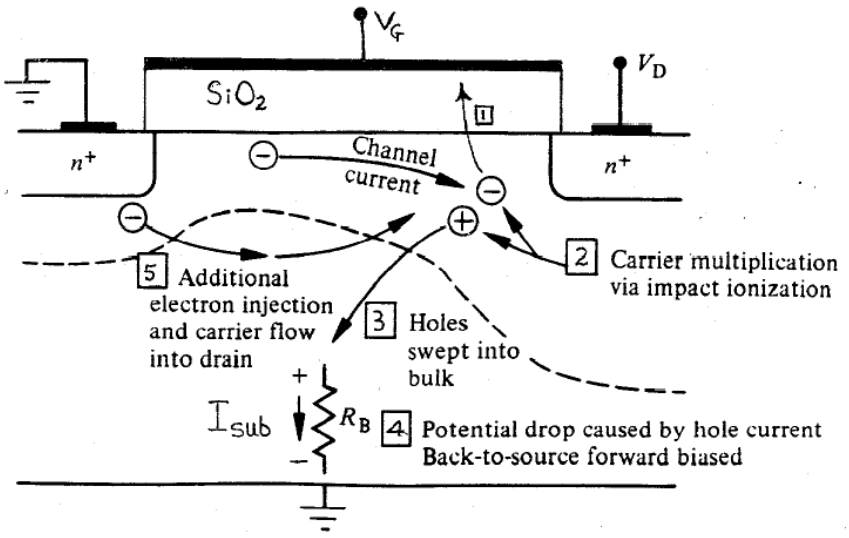

Figure 1.5: Cross-sectional view of n-channel MOSFET illustrating hot-carrier injection [35].

1.4 Ways to Overcome Short-Channel Effects

These SCEs should be minimized or eliminated to preserve the electrical long-channel behavior of a physical short-channel device, given that they impede device operation and performance. Literature from recent years suggests that the use of novel device designs and engineering techniques (as presented in **Figure 1.6**) may diminish these short-channel effects.

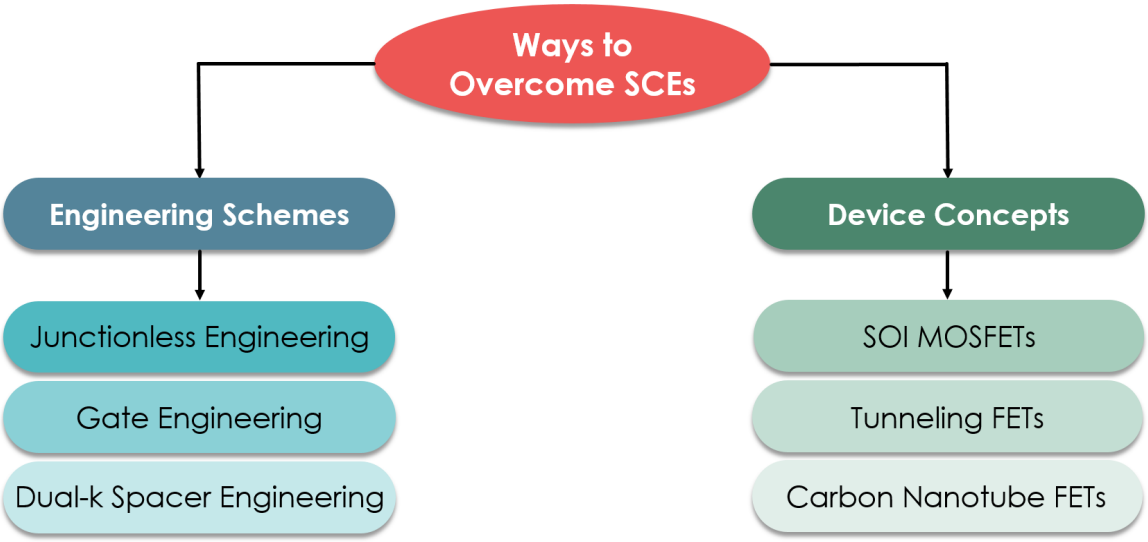

Figure 1.6: Different ways to overcome SCEs in nano-scale MOSFET.

1.4.1 Engineering Schemes

Researchers have developed various engineering schemes to mitigate the impact of SCEs on transistor performance. Here are some engineering schemes to address SCEs.

1.4.1.1 Junctionless Engineering

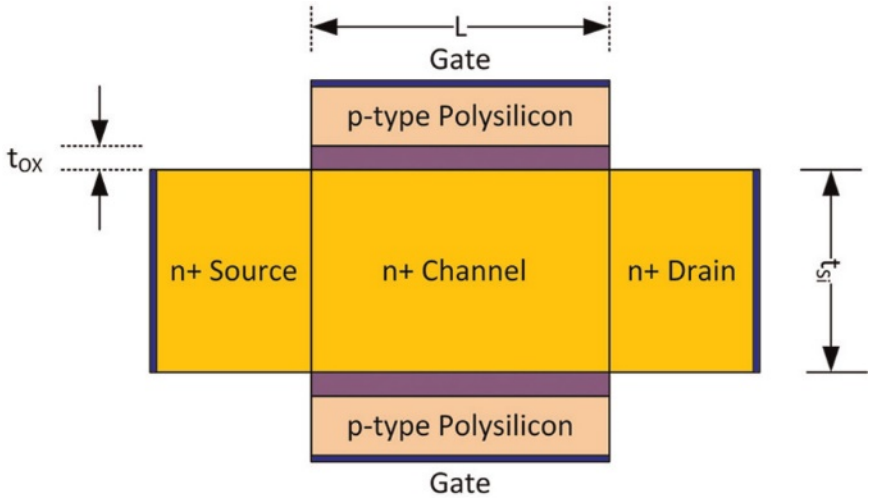

Figure 1.7: Cross-sectional view of junctionless double gate MOSFET [36].

A junctionless field effect transistor (JLFET) is a transistor that functions in its channel area without a traditional p-n junction, as depicted in **Figure 1.7** [36]. They use a single-gated silicon nanowire structure instead. This nanowire serves as the current flow channel, and the gate terminal regulates the current flow by controlling the conductivity of the nanowire [37]. When a positive gate voltage is applied, it draws negatively charged carriers (electrons) to the nanowire's surface, forming an accumulation region. This accumulation region improves the nanowire's conductivity, enabling current to pass between the source and drain terminals. When a negative gate voltage is supplied, the negatively charged carriers are repelled, resulting in a depletion zone at the nanowire's surface. The conductivity of the nanowire is reduced in this depletion zone, essentially limiting current passage between the source and drain terminals. This JL engineering has various benefits

over conventional transistors, including easier manufacture, lower production costs, lower leakage current, and higher energy efficiency. JLFETs alleviate the difficulties related to SCEs by removing the p-n junction, enabling additional scalability and performance benefits [38].

1.4.1.2 Gate Engineering

Long et al. [39] introduced the dual material gate (DMG) MOSFET in 1997, an innovative configuration that effectively mitigates SCEs while concurrently augmenting carrier velocity, as demonstrated in **Figure 1.8**. The gate of the DMG-MOSFET comprises two contacting materials with distinct work functions. The metal near the source has a larger work function, whereas the metal near the drain has a lower work function. Therefore, the threshold voltage $V_{th1} > V_{th2}$ enhances carrier transport efficiency. A metal gate with a lower work function in a DMG-MOSFET diminishes the electric field near the drain, suppressing hot-carrier effects even further. The fringing capacitance issue in DMG-MOSFET is also addressed because two gates are laterally linked into one single gate.

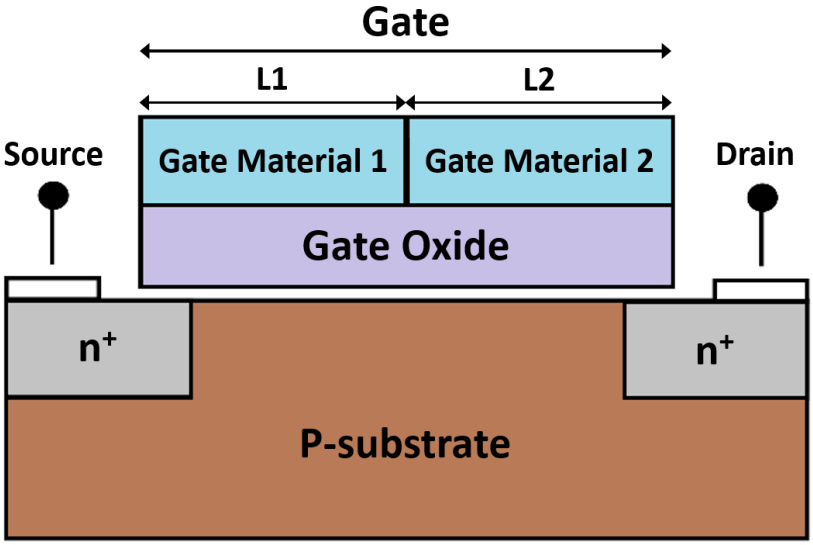

Figure 1.8: Schematic structure of dual material gate MOSFET [39].

1.4.1.3 Dual-k Spacer Engineering

Dual-k spacer engineering uses two dielectric materials with differing relative permittivity (k-values) to build spacers beside the transistor's gate electrode. **Figure 1.9** illustrates that dual-k spacer engineering combines a high-k spacer on the inside and a low-k spacer on the outside to increase device performance and reduce SCEs [40]. For the inner layer, a high-k dielectric with a higher k-value than typical silicon dioxide (SiO_2) is placed because a high-k spacer enhances electrostatic control, minimizes SCEs, and improves transistor performance. Whereas for the outer layer, a low-k dielectric such as SiO_2 is considered because silicon in SiO_2 makes the silicon channel more flexible, reducing the likelihood of encountering dangling bonds and interface traps, and the low-k spacer reduces parasitic capacitance, minimizing the impact of capacitance and leakage current on transistor performance [41]. Thus, combining high-k and low-k spacers offers greater channel control, reduces SCEs and leakage current, increases threshold voltage stability, and improves overall transistor performance.

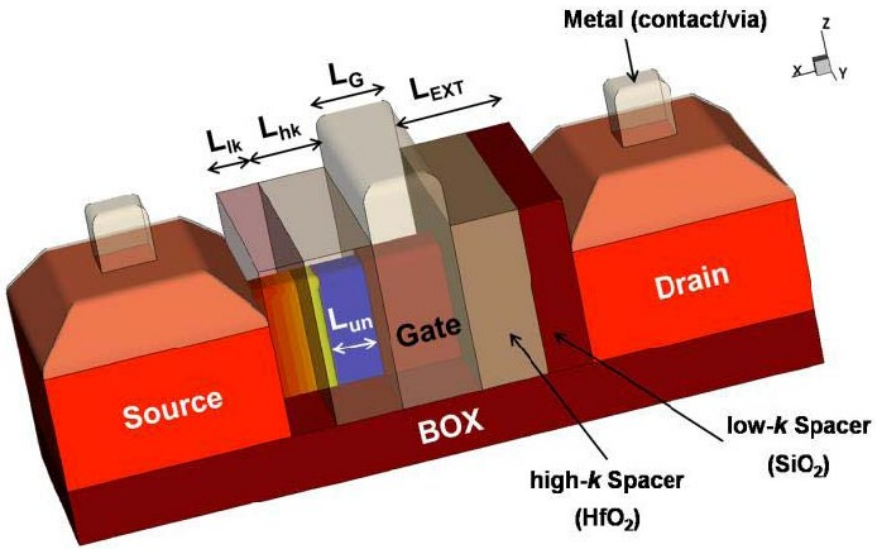

Figure 1.9: Schematic FinFET structure with dual-k underlap spacers [40].

1.4.2 Device Concepts

Researchers globally are now working to advance the speed of operation and packing density of ICs by developing novel devices. Here are some devices to address SCEs.

1.4.2.1 Silicon-on-Insulator MOSFET

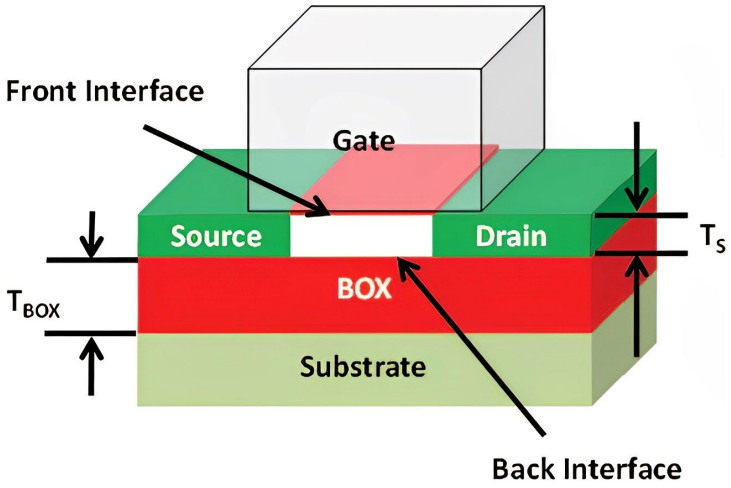

Figure 1.10: Schematic structure of FD-SOI MOSFET [42].

By sandwiching an entirely depleted silicon-on-insulator (SOI) device [42] between two connected gate electrodes, it is possible to substantially reduce SCEs. As illustrated in **Figure 1.10**, SOI technology utilizes a relatively thick silicon oxide layer to separate a thin silicon layer from a silicon substrate. The SOI technology eliminates the possibility of latch-up failures by dielectrically isolating components and reducing various parasitic circuit capacitances in conjunction with lateral isolation. SOI technology provides devices that are exceptionally dense and radiation-resistant. The leakage current is negligible due to the absence of reverse-biased junctions utilized for isolation. Furthermore, the steeper sub-threshold slope of SOI devices makes them more suitable for scaling devices into the deep-submicron regime. This feature enables threshold voltage scaling, which is particularly advantageous for low-voltage, low-power applications. The SOI MOSFET is

a highly desirable component for VLSI applications requiring low power and high performance due to its minimal parasitic capacitances.

1.4.2.2 Tunneling Field Effect Transistor

Figure 1.11 exhibits a lateral structure view of tunneling field effect transistors (TFETs), another intriguing alternative to traditional MOSFETs [43]. TFETs use the concept of band-to-band tunneling, in which charge carriers use quantum mechanical phenomena to cross a potential barrier in a semiconductor material. The capacity of TFETs to function at lower supply voltages is a significant benefit over MOSFETs. This is due to the sharp subthreshold swing characteristic of TFETs, which allows them to attain high on-state current while retaining low off-state leakage current [44]. As a consequence, TFETs have the potential to drastically lower IC power consumption. Another benefit of TFETs is that they are compatible with various semiconductor materials. This offers flexibility when developing TFET devices for multiple applications and performance requirements. Nevertheless, TFETs encounter certain limitations compared to conventional MOSFETs: their generally lower current densities restrict their applicability in high-power scenarios. Furthermore, fabricating TFETs with the required precision is a substantial task.

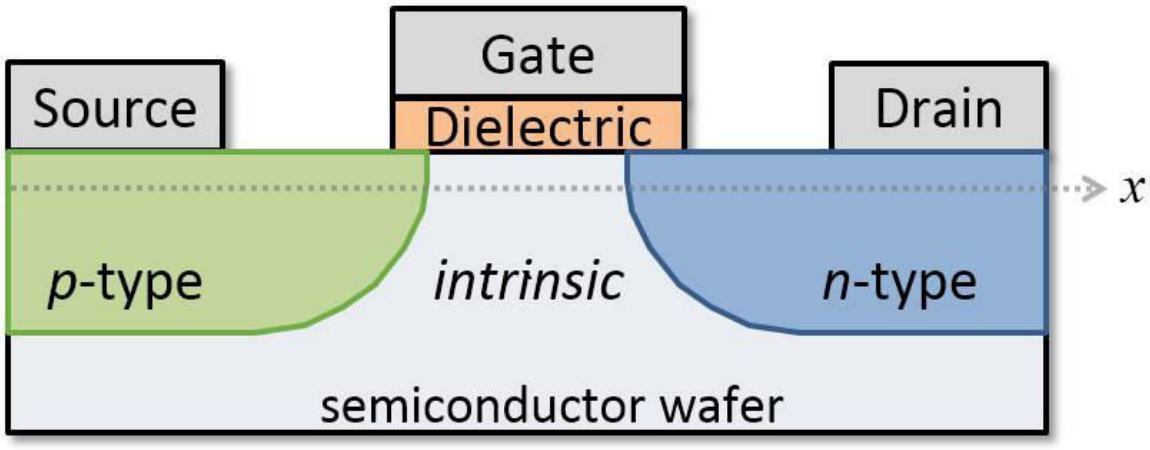

Figure 1.11: Schematic lateral structure of TFET [43].

1.4.2.3 Carbon Nanotube Field Effect Transistor

Carbon nanotube field effect transistors (CNTFETs) use carbon nanotubes as a conducting channel, as portrayed in **Figure 1.12** [45]. Carbon nanotubes are hexagonally latticed cylindrical structures made of carbon atoms. One of the most significant benefits of CNTFETs is their capacity to function at extremely small scales with reduced power consumption, thus enabling ultra-low-power operation. Furthermore, CNTFETs have high electron mobility, thermal conductivity, and mechanical strength [46]. These properties make CNTFETs capable of operating at high frequencies and high-speed switching applications such as data transmission systems. Another distinguishing aspect of CNTFETs is the ability of carbon nanotubes to be grown on flexible substrates, enabling the development of flexible and wearable electronics. Despite these potential benefits, there are still hurdles that must be overcome before CNTFETs may be widely used. Controlling the chirality of carbon nanotubes during their production is one of the most challenging tasks. Scalability, device homogeneity, and contact resistance concerns must also be addressed to guarantee the practicality and economic feasibility of CNTFETs.

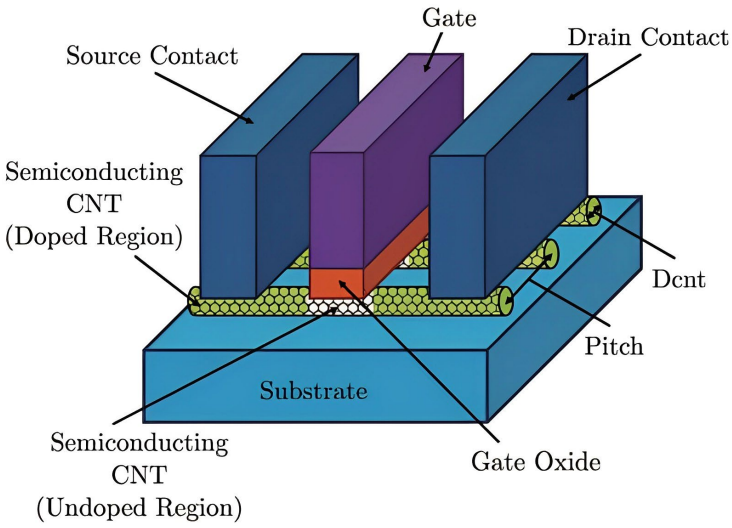

Figure 1.12: Schematic structure of CNTFET device [45].

1.5 RESEARCH GAPS

Research gaps identified after reviewing the literature are as follows, which will be attempted to address via possible solutions.

1. Need to make the device a more cost-effective solution, reduce the complexity of the fabrication process, and offer greater design flexibility.

2. The rise in off-state leakage current with the decreasing gate oxide thickness is another severe issue. This leakage results from quantum mechanical tunneling, which limits the device scaling and negatively impacts the performance of the device.

3. Densely packed VLSI and ULSI circuits often run at high temperatures due to heat production, and excessive temperatures might harm or influence the functioning of the nanoscaled devices. Therefore, device reliability must be inspected to guarantee long-term endurance and stability.

4. The parasitic capacitance and short channel effects become more significant at the sub-nm range, deteriorating device performance. Thus, thoroughly examining these impacts is essential to improve the device's performance.

5. Due to their many benefits, FET-based electronic devices are widely utilized as bio-sensors, gas-sensors, radiation-sensors, etc. With the advancement of technology towards compact devices, there is a need for new FET-based sensors that cater to different specialized applications.

1.6 POSSIBLE SOLUTION – FINFET

FinFETs are the solution because their vertical fin design provides excellent electrostatic control over the channel, reduced leakage current, and improved transistor switching characteristics, allowing for continued scaling of transistor sizes.

1.6.1 FinFET Structure

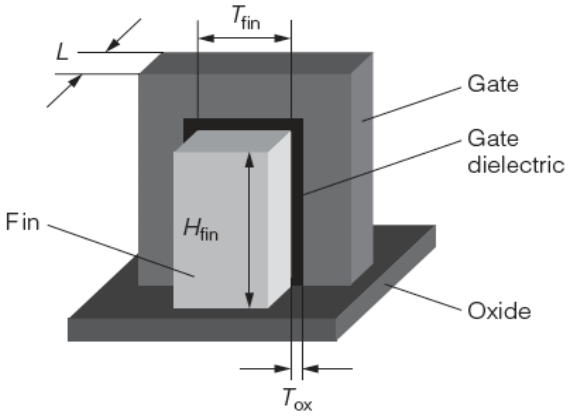

Figure 1.13: Schematic structure of conventional FinFET [47].

FinFET, or fin field effect transistor, is a non-planar multi-gate transistor utilized in the architecture of contemporary CPUs. The structure's visual resemblance to a pair of fins inspired the name. In 1989, Hisamato et al. [48] constructed a completely depleted lean channel transistor (DELTA) using a double-gate SOI structure. **Figure 1.13** illustrates a conventional three-dimensional schematic representation of a FinFET device [47], while the 3D structure and cross-sectional view of intel's tri-gate FinFET are portrayed in **Figure 1.14(a)** and **Figure 1.14(b)** [49]. The primary characteristic of a FinFET device is the structural element known as the "fin." The fin is a slender, vertically oriented silicon structure that functions as the channel area of the transistor, facilitating the passage of

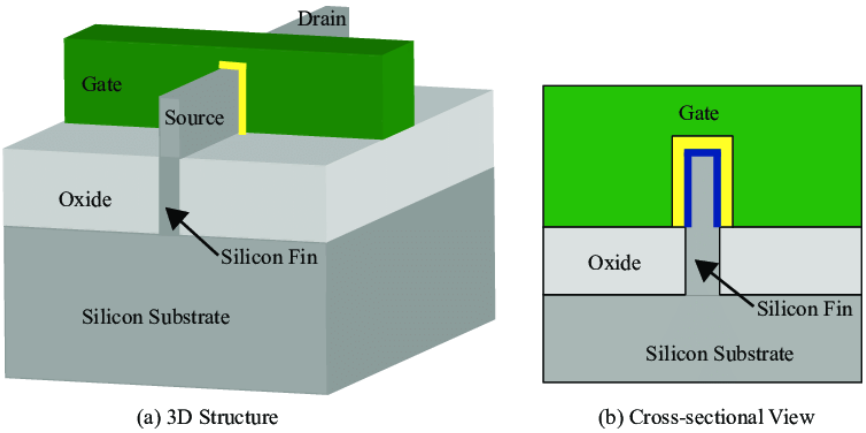

Figure 1.14: (a) 3D structure and (b) cross-sectional view of Intel's tri-gate FinFET [49].

current while the transistor is in the on-state. The gate dielectric, which consists of high-k dielectric materials, envelops the sides and upper surface of the fin. The gate dielectric functions as an insulating material and regulates the passage of electric current inside the channel using voltage application. The metal gate electrodes are used to enclose the gate dielectric. The fin structure consists of source and drain regions at its two ends. These regions have a high concentration of impurities to facilitate the establishment of electrical connections for current flow and can impact the switching behavior of the transistor through their doping profiles and design. The effective channel width (W_{Eff}) of the FinFET is determined by the height (H_{fin}) and width (T_{fin}) of the fin using Equation (1.1) [50].

$$(W_{Eff}) = (2 \times H_{fin}) + T_{fin} \quad (1.1)$$

The fundamental electrical configuration of a FinFET is almost similar to that of a conventional MOSFET. A structural comparison between a conventional MOSFET and a FinFET is illustrated in **Figure 1.15** [51]. The FinFET structure, similar to the MOSFET, comprises a single source, one drain contact, a gate, and a substrate that regulates the current flow. However, the structure of MOSFETs is planar, with the channel connecting the source and drain regions formed as a horizontal, flat layer. In contrast, FinFETs utilize a three-dimensional bar known as a fin atop the silicon substrate to represent the channel.

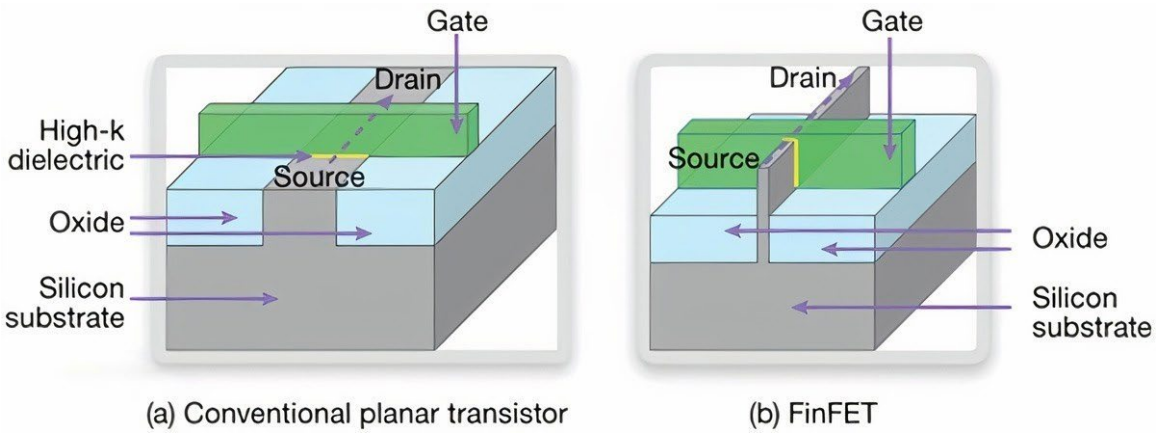

Figure 1.15: Structural comparison between (a) planar MOSFET and (b) FinFET [51].

1.6.2 FinFET Classification

FinFETs are classified into two types: shorted-gate (SG) and independent-gate (IG). **Figure 1.16** exhibits the structural comparison between SG and IG FinFETs. SG FinFETs are also called three-terminal (3T) FinFETs, whereas IG FinFETs are called four-terminal (4T) FinFETs. The front and rear gates of SG FinFETs are physically shorted, while the gates of IG FinFETs are physically isolated. Thus, front and rear gates work together to regulate the channel's electrostatics in SG FinFETs. As a result, SG FinFETs have improved on-current (I_{on}) and off-current (I_{off}) values than IG FinFETs. IG FinFETs can have distinct voltages or signals applied to their two gates [21].

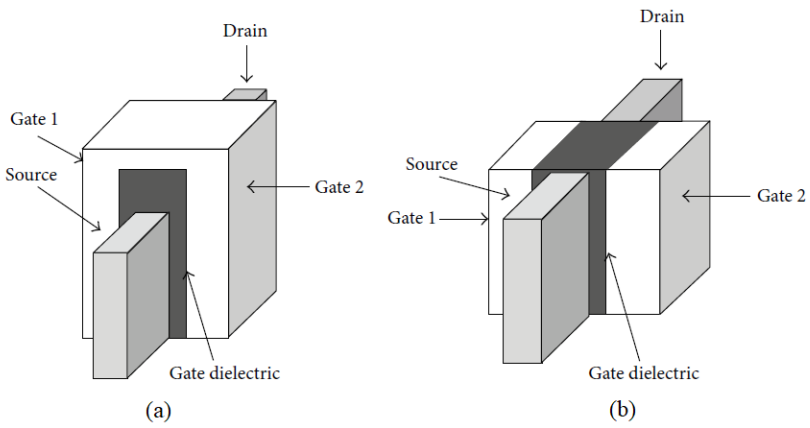

Figure 1.16: Structural comparison between (a) SG and (b) IG FinFET [21].

Based on asymmetries in their device parameters, SG FinFETs can be further classified. In a typical SG FinFET, the front and rear gates have identical work functions. However, it is possible to modify the gate work function in several ways, resulting in an asymmetric gate work function FinFET or ASG FinFET, as portrayed in **Figure 1.17** (shaded gate implies different work functions). It is possible to fabricate ASG FinFETs by selectively doping the two gate stacks. The short-channel properties of these devices are very promising and provide a two-orders-of-magnitude reduction in I_{off} than SG FinFET. However, the I_{on} of these devices is somewhat lower than that of an SG FinFET [21].

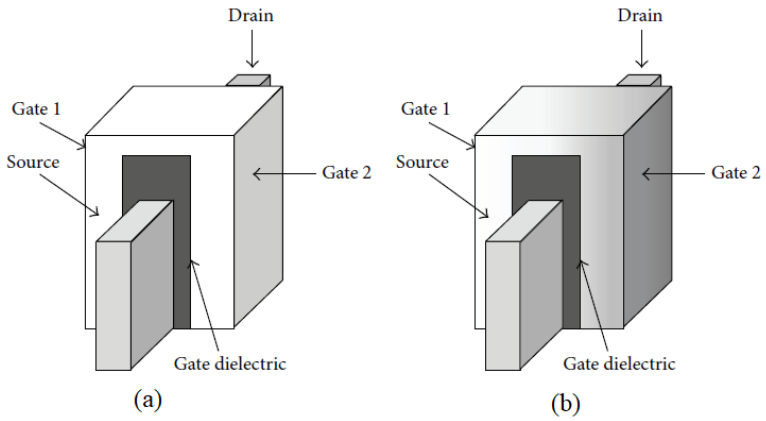

Figure 1.17: Structural comparison between (a) SG and (b) ASG FinFET [21].

1.6.3 FinFET Operation

A conventional n-type FinFET, where the source and drain regions are doped with n-type impurities, and the substrate is doped with p-type impurities, is considered to understand the working principle of the FinFET.

ON Condition:

Initially, the semiconductor fin is in its intrinsic state, meaning it has an equal number of electrons and holes. When a positive voltage is applied to the gate terminal, an electric field is generated across the insulating layer towards the channel region of the fin. The electric field will repel the holes from the surface of the fin, forming a layer of uncovered negative ions and creating a depletion region near the surface of the fin. Besides this depletion region, an inversion layer of electrons starts to form at the source, and as the gate voltage increases, that inversion layer expands towards the drain. As gate voltage passes the threshold voltage, the electrons from the source and drain flow in, forming an inversion layer of electrons connecting the source and drain regions. This creates a conductive channel between the source and drain regions, as shown in **Figure 1.18(a)**. In the channel, the direction of the current flow is from the drain to the source. The amount of current flowing through the FinFET can be controlled by adjusting the gate voltage.

OFF Condition:

When a negative voltage is applied to the gate terminal, it repels the electrons from the fin region. As the negative gate voltage increases, it creates a depletion zone in the fin region, gradually reducing the concentration of free electrons. When this depletion zone reaches a critical point, the channel becomes pinched off, and no more free electrons are available to conduct current. The transistor is in the OFF condition in this state, and no current flows from the drain to the source, as shown in **Figure 1.18(b)**.

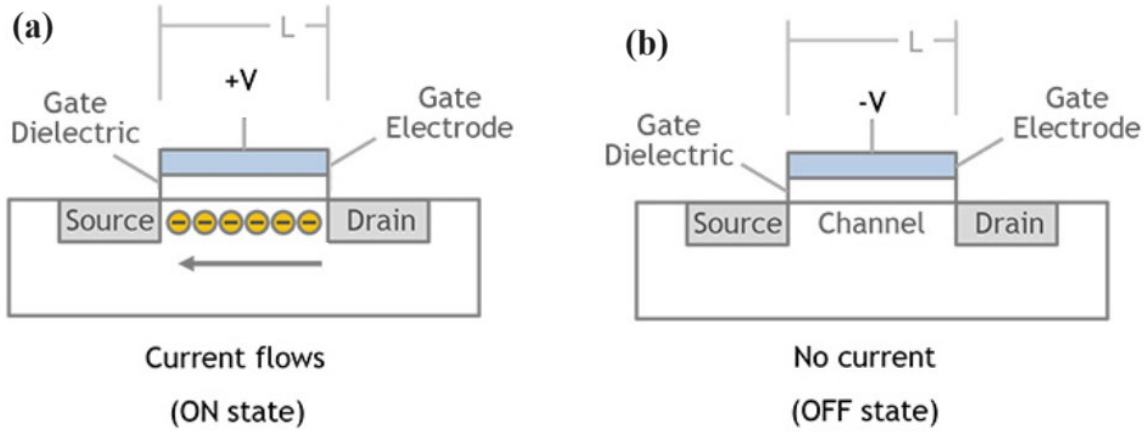

Figure 1.18: Operating principles of conventional FinFET [52].

1.6.4 Advantages of FinFET

Modern semiconductor manufacturing foundries prefer FinFET technology over traditional planar transistor designs due to its several advantages, as portrayed in **Figure 1.19**.

1. **Improved Performance:** FinFETs have enhanced electrical performance in comparison to planar transistors. These devices offer enhanced regulation of electron movement, leading to faster switching speeds and improved circuit performance.
2. **Reduced Leakage Current:** The foremost benefit of FinFETs is their capacity to mitigate leakage current. When the transistor is not actively switching, the 3D fin structure provides greater control in the transistor's OFF state, lowering power usage.

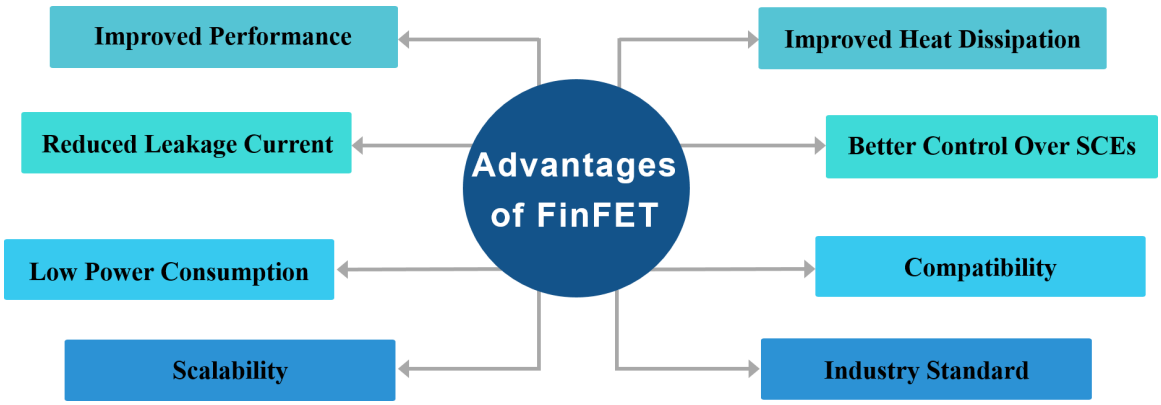

Figure 1.19: Advantages of FinFET device.

3. **Low Power Consumption:** FinFETs are ideal for applications where power consumption is of the utmost importance, such as mobile devices and IoT devices, due to their exceptional energy efficiency.
4. **Scalability:** The scalability of FinFET technology enables its seamless integration into smaller technology nodes such as 7 nm, 5 nm, and beyond. FinFETs have been crucial in preserving Moore's law and enhancing transistor density as semiconductor manufacturers shift towards lower lithography nodes.
5. **Improved Heat Dissipation:** The heat dissipation of FinFETs is also helped by their three-dimensional fin structure. The increased surface area offered by the fins facilitates improved thermal management, hence mitigating the potential for overheating in high-performance microprocessors.
6. **Better Control Over SCEs:** FinFETs provide superior control over SCEs, including drain-induced barrier lowering (DIBL) and subthreshold slope (SS) degradation, compared to planar transistors.
7. **Compatibility:** The integration of FinFET technology into current semiconductor production processes can be facilitated by certain adjustments, simplifying the transition for semiconductor manufacturers towards adopting FinFET technology.

8. **Industry Standard:** FinFET technology has emerged as a prevailing standard in advanced semiconductor fabrication, garnering widespread adoption by prominent semiconductor foundries. The extensive use of FinFET-based designs guarantees a diverse range of tools and specialized knowledge inside the ecosystem.

1.6.5 Challenges Confronted by FinFET

While FinFET technology offers numerous advantages, it also comes with some challenges. **Figure 1.20** describes the challenges confronted by the FinFET technology.

1. **Lithography Challenges:** The issues associated with lithography become more prominent as the dimensions of semiconductor nodes continue to decrease. Extreme ultraviolet (EUV) lithography has been proposed to address some challenges, yet it is a technology characterized by intricacy and high costs.
2. **Manufacturing Complexity:** Complex FinFET architectures make manufacturing more difficult, particularly at lesser nodes. Complexity increases manufacturing costs and the need for specialized fabrication equipment.

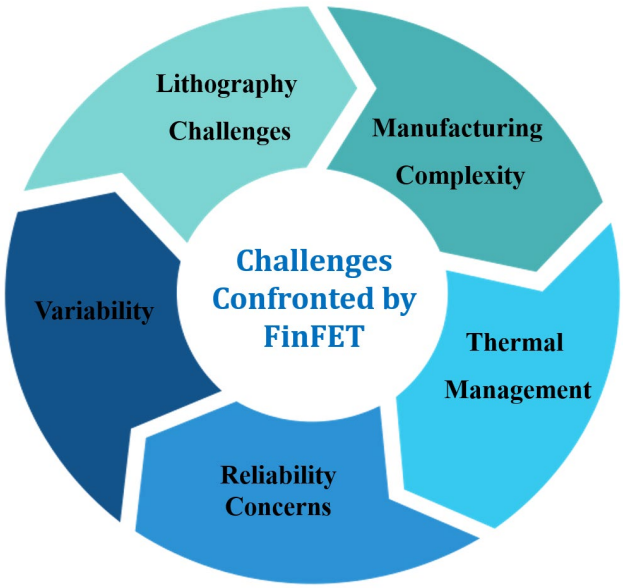

Figure 1.20: Challenges associated with FinFET technology.

3. **Thermal Management:** Although FinFETs dissipate heat more effectively than planar transistors, heat management in high-performance processors remains difficult. This is particularly pertinent in high-performance computing applications and data centers.
4. **Reliability Concerns:** The ongoing reduction in transistor sizes raises concerns regarding the long-term reliability of FinFET-based devices, such as electro-migration, aging effects, and overall device longevity.
5. **Variability:** FinFETs are susceptible to process fluctuations, and this sensitivity contributes to increased variability in transistor properties at lower nodes. It is critical to manage this variability to ensure consistent device functioning.

1.7 THESIS OBJECTIVES

1. To investigate the analog and RF performance of Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around (JAM-GS-GAA) FinFET and optimize the fin aspect ratio to achieve a high-performance transistor.
2. To discuss the reliability issues of JAM-GS-GAA FinFET by considering the impact of temperature and gate electrode work function on the proposed device's static, analog, RF, and wireless performance.
3. To explore the impact of dual-k spacer (SiO_2 + HfO_2) engineering on the RFIC design feasibility of a JAM-GS-GAA FinFET in the sub-10 nm range.
4. To replace the silicon material with III-V compound semiconductor materials like GaAs to reduce the parasitic capacitances and improve the small-signal behavior of JAM-GS-GAA FinFET.

5. To design a highly sensitive breast cancer cell detector by introducing a nanocavity gap above the gate dielectric to establish the GaAs JAM-GS-GAA FinFET as a promising contender for detecting breast cancer cells.

The underlying goal of these objectives is to design and optimize a new FinFET device that can surmount the challenges encountered by conventional FinFETs and become a viable option for low-power, analog, RF, and biosensor applications.

1.8 THESIS ORGANIZATION

The present thesis is structured into seven chapters to address and accomplish all the research objectives. Every chapter is structured in an inherently self-contained manner. The citations for each chapter are listed at the end of the corresponding chapter.

Chapter 1 describes the shortcomings of the MOSFET and the need for FinFETs. The chapter provides an overview of MOSFET scaling concerns and SCEs. After that, the ways to overcome the SCEs are discussed. In this context, the different engineering schemes (junctionless engineering, dual-k spacer engineering, etc.) and the advanced FET structures (SOI MOSFET, TFET, etc.) reported in different research articles have been presented. Further, the chapter progresses toward the architecture of FinFET, classification, fundamental operating principle, and potential advantages and drawbacks. Lastly, the chapter outlines the thesis's research objective and overall organization. It highlights the importance of the research conducted in this thesis.

Chapter 2 illustrates the comprehensive information on the proposed device's structure and the design and materials parameters used in the simulation. After that, the simulation models used in this study are enumerated, accompanied by their calibration using fabrication-based experimental data sourced from relevant literature. A step-by-step

device fabrication outline is displayed to demonstrate the fabrication feasibility of the proposed device. Further, the chapter analyses the analog and RF performance parameters of the proposed JAM-GS-GAA FinFET with conventional FinFET and GAA FinFET. The impact of the fin aspect ratio on various static, analog, and RF performance parameters of the proposed device is also examined.

Chapter 3 investigates the impact of temperature and gate electrode work function on various static, analog, RF, linearity, and harmonic distortion characteristics of the proposed device to establish its reliability. Firstly, the performance of the proposed JAM-GS-GAA FinFET device is compared with other existing devices on different technologies at a fixed gate length of 10 nm to evaluate its significance. The devices considered for comparison are junctionless double gate vertical MOSFET [23], nano-sheet transistor [24], junctionless SOI nanowire FET [25], and tunnel field effect transistor [26]. Then, the reliability of the JAM-GS-GAA FinFET is explored by analyzing the impact of temperature and gate electrode work function on parameters like the electric field, transconductance, cut-off frequency, 1-dB compression point, etc.

Chapter 4 inspects the impact of dual-k spacer (SiO_2 + HfO_2) engineering on the RFIC design feasibility of a JAM-GS-GAA FinFET in the sub-10 nm range. This chapter examined different configurations, such as conventional tri-gate JAM-GS-FinFET, JAM-GS-GAA-FinFET without a spacer, JAM-GS-GAA-FinFET with single-k spacers, and the proposed JAM-GS-GAA-FinFET with dual-k spacer. The dual-k spacer configuration uses HfO_2 as a high-k spacer for the inner layer and SiO_2 as a low-k spacer for the outer layer. This chapter describes the effect of dual-k spacers and measures the improvements in performance resulting from the implementation of the dual-k spacers in the domains of static, analog, and RF FoMs. In addition, the difference between the different static, analog,

and RF FoMs (ΔFoMs) of the dual-k spacer structure and conventional tri-gate JAM-GS-FinFET configuration are compared to highlight the benefits of the dual-k spacer structure.

Chapter 5 explores the parasitic capacitances and small-signal behavior of JAM-GS-GAA FinFET with an aim to assess the efficacy of GaAs as a fin material. Capacitance-related FOMs like gain bandwidth product (GBP) and transconductance frequency product (TFP) are also analyzed for switching applications. Further, the OFF-current (I_{off}), switching ratio (I_{on}/I_{off}), subthreshold swing (SS), and parasitic capacitances of the proposed device are examined with variations in gate length (L_g), channel doping (N_{Ch}), fin width (W_{Fin}), gate electrode work function (ϕ_m), and temperature (T). Then, a comprehensive analysis of the small-signal behavior regarding the scattering (S) parameters of GaAs JAM-GS-GAA FinFET is conducted across the terahertz (THz) frequency range. The effect that L_g, N_{Ch}, W_{Fin}, ϕ_m, and T have on the S-parameters of GaAs JAM-GS-GAA FinFET is carried out.

Chapter 6 describes the utilization of GaAs JAM-GS-GAA FinFET to accomplish the electrical identification of the breast cancer cell MDA-MB-231 by monitoring the device switching ratio. This chapter showcases the operation of a GaAs JAM-GS-GAA FinFET sensor for breast cancer cell recognition. After that, the switching ratio-based device sensitivity is evaluated by analyzing the drain current characteristics for air (cell-free), MCF-10A (healthy), and MDA-MB-231 (cancerous cells). The sensor is also assessed for its reproducibility, stability, and capability to distinguish between viable and non-viable cells. Further, the possibility of early detection of cancerous breast cells using Bruggeman's model is discussed. Next, the effect of biomolecule occupancy on the device's sensitivity is explored. This chapter also investigates how changes to the frequency and the device's physical parameters, like fin height, fin width, gate electrode

work function, channel doping, temperature, and drain voltage, influence the device's sensitivity. Finally, the effectiveness of the proposed breast cancer cell sensor is compared to that of already existing breast cancer sensors.

Chapter 7 provides a comprehensive overview of the study conducted in this thesis, including the essential findings and conclusions derived from the provided data. This chapter also examines the potential future applications of the current study and explores how it might be expanded upon and used in future research endeavors.

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2

CHAPTER

Analog and RF Performance of Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around (JAM-GS-GAA) FinFET for High-Performance Applications

- *This chapter discusses the analog and RF performance of Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around (JAM-GS-GAA) FinFET and the impact of the fin aspect ratio to achieve a high-performance transistor.*
- *It is found that the switching ratio of the JAM-GS-GAA FinFET increased almost thirty-one times, thereby improving the analog performance in terms of transconductance, device efficiency, intrinsic gain, and early voltage compared to conventional FinFET.*
- *The RF performance parameters like GTFP and GFP get enhanced by 3.37 and 2.73 times, with a 21.46% enhancement in TFP for JAM-GS-GAA FinFET configuration compared to conventional FinFET due to enhanced value of g_m, TGF, and a reduced value of g_d.*
- *It is also analyzed that the proposed device with a higher fin aspect ratio exhibits the most improved static, analog, and RF performance compared to the two other configurations with a lower fin aspect ratio.*
- *Consequently, the proposed JAM-GS-GAA FinFET device with a high fin aspect ratio would be an attractive solution for low-power and high-performance CMOS circuits.*

2.1 INTRODUCTION

As described in **Chapter 1**, the scaling of transistors has expanded throughout the last many years. This has been done to increase the maximum speed of operation that the electronic components are capable of while simultaneously increasing the number of available electronic components. Because of the diminutive size of CMOS devices, transistors are susceptible to significant short-channel effects (SCEs), which play a role in the loss of power [1-4]. Moreover, in short-channel devices, the device's I-V characteristics decrease due to the reduced gate control area across the channel. Multiple device topologies have been suggested to alleviate these difficulties, including multi-gate MOSFET [5], TFETs [6], HEMTs [7, 8], and FinFETs [9-11]. FinFET technology is the driving force behind the current integrated circuit industry, which optimizes SCEs to achieve exceptional scalability, augment battery longevity, and minimize power consumption [12, 13]. Increasing the number of gates across the channel improves the device's ability to regulate electrostatic fields. The development of the Gate-All-Around (GAA) configuration improved the sub-threshold characteristics and the device's performance [14, 15]. Consequently, GAA FinFET devices can be scaled down further.

Another concern in the continued scaling of CMOS technology is the increase in the gate direct tunneling current with the decreasing gate oxide thickness (t_{ox}), resulting in the enhanced off-state leakage current (I_{off}). A Gate-Stack (GS) configuration with a thin SiO_2 layer stabilizing the high-k dielectric and silicon substrate is implemented to suppress this rise in off-state leakage current [16]. GS design also eliminates mobility deterioration and instability of threshold voltage caused by the direct deposition of high-k dielectrics on silicon substrates [17, 18].

Fabricating p-n junctions that are ultra-shallow and sharp in the sub-10 nm domain is a challenge. In response to the research conducted by Lilienfeld, Colinge proposed junctionless (JL) transistors characterized by consistent doping across all areas [19]. Since JL transistors don't have a p-n junction and are inexpensive, they are simple to manufacture. Also, the JL devices have better immunity against the SCEs with effectively increased channel length compared to conventional CMOS devices. However, JL devices still can't attain the outstanding turn-off characteristics by completely depleting the channel during the OFF state [20]. A lower doping concentration in the channel area will quickly deplete charge carriers. However, this will decrease the drain current and increase the drain/source series resistance. The proposal to address the low channel doping concentration issue involves implementing Junctionless-Accumulation-Mode (JAM) FETs, which feature heightened doping levels in the source and drain regions [21-23]. Subsequently, the JAM-GS-GAA FinFET device was put forward, considering all the considerations.

The demand for portable and higher battery backup electronic devices has sufficiently increased in the last few years. The System-on-Chip (SoC) idea provides a means to boost the IC's speed performance and transistor density, which are necessary to keep up with the rising demand. In SoC technology, the majority of the elements of a system are integrated as an independent system on a semiconductor chip. However, device optimization is very challenging with SoC technology. The analog and RF performance of JLAM-CGAA MOSFET has been investigated extensively [24]. In another study, Raskin et al. reported the analog/RF performance of multiple gate SOI devices [25]. However, no work on the JAM-GS-GAA FinFET analog and RF performance has been published. In addition, the fin aspect ratio (AR) is an essential geometric parameter in FinFET

technology. It is described as the ratio of fin width (W_{Fin}) to fin height (H_{Fin}) in a few research papers [26, 27], but a more precise definition: the ratio of H_{Fin} to W_{Fin} is considered for this research work. Because when H_{Fin} is greater than W_{Fin}, the sidewall surface dominates over the top surface, and the device acts as a 3D device. In contrast, the device acts as a planar device when W_{Fin} is greater than H_{Fin} due to the dominance of top surface orientation [28]. In recent studies, the researchers have demonstrated that alteration of the geometrical parameters, such as gate length, gate oxide thickness, fin width, and fin height, primarily influence the FinFET performance [26, 29, 30]. Thus, the purpose of this chapter is to examine the structure of the device and enhance the performance of the proposed JAM-GS-GAA FinFET for applications in high-frequency analog/RF circuits. Three devices are considered for comparison: FinFET, GAA FinFET, and GS-GAA FinFET. FinFET is a conventional tri-gate device, while the tri-gate is enhanced to a GAA structure in GAA FinFET. GAA FinFET device, with a gate-stack configuration in the gate oxide, is the GS-GAA FinFET device. Also, the aim is to identify the optimal fin aspect ratio that will result in improved static, analog, and RF performance of the JAM-GS-GAA FinFET.

The remainder of the chapter is: Section 2 offers comprehensive information on the device's structure and the physical models employed. Section 3 demonstrates the process of calibrating the models used in the simulation setup by comparing them to the data reported in experiments. Section 4 describes the manufacturing feasibility of the device under consideration. Section 5 analyses the analog and RF performance parameters of the proposed JAM-GS-GAA FinFET with conventional FinFET and GAA FinFET. The impact of the fin aspect ratio on various static, analog, and RF performance parameters of the proposed device is also examined. Ultimately, the concluding section presents a comprehensive overview of the chapter.

2.2 DEVICE DESIGN AND PHYSICAL MODELS

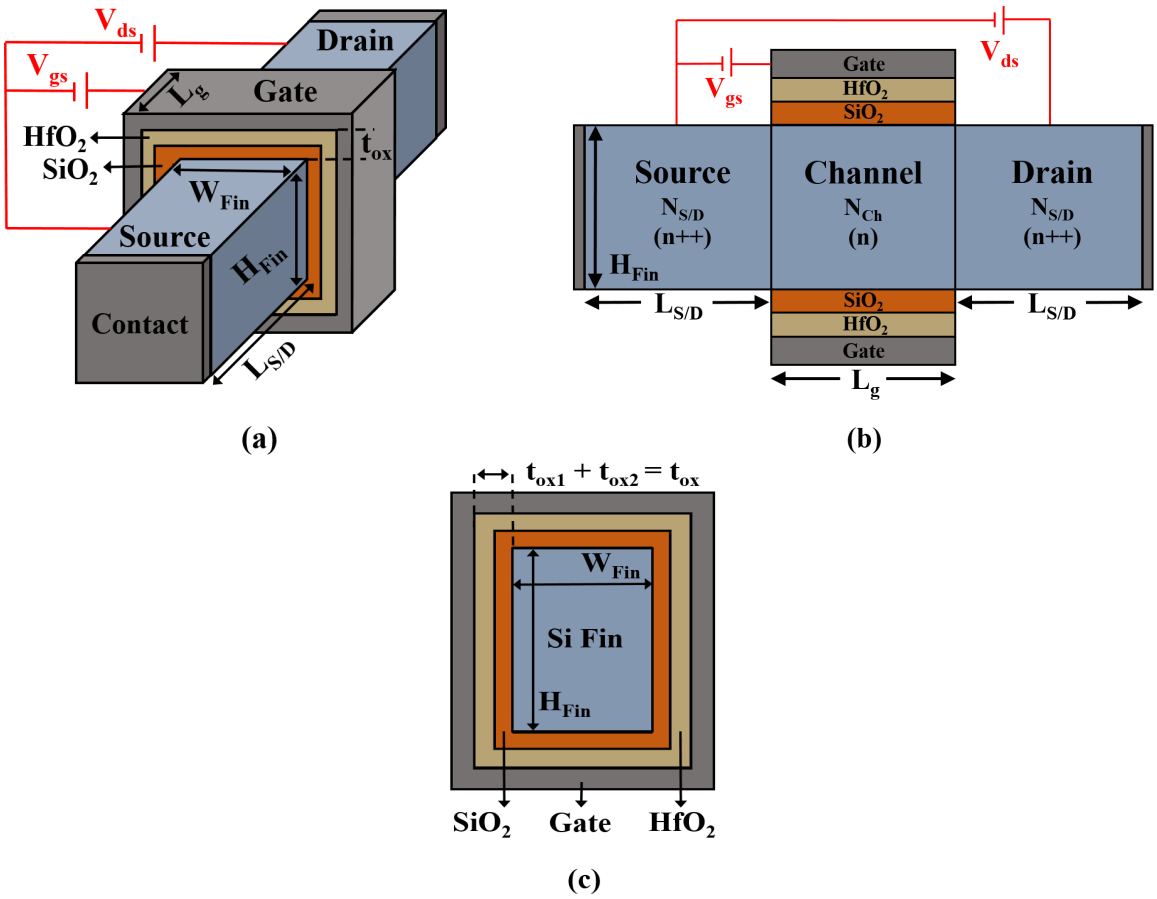

Figure 2.1: (a) Proposed JAM-GS-GAA FinFET 3-D structure, (b) horizontal, and (c) vertical 2-D view slit through the device's silicon fin [22].

Figure 2.1(a) displays the proposed 3D structure of JAM GS-GAA FinFET, whereas horizontal and vertical cross-sectional view cut along the silicon fin of the proposed device is portrayed in **Figure 2.1(b)** and **Figure 2.1(c)**, respectively. The parameters like device dimensions, doping profiles, gate work function, etc., are kept the same for all three devices for a fair comparison. The only difference is that in the JAM GS-GAA FinFET device, SiO_2 (k = 3.9) and HfO_2 (k = 25) are considered in equal proportions, whereas in the other two devices, only SiO_2 is used as a gate oxide. The gate length (L_g) of the device is 7 nm, and the length of S/D regions ($L_{S/D}$) is fixed at 10 nm. The t_{ox} is kept constant all around the fin at 1 nm for all three devices. All three regions are uniformly doped with n-type

doping species. The doping concentration in the channel region (N_{Ch}) is 1×10^{16} cm^{-3}, while the concentration in the source/drain regions ($N_{S/D}$) is 1×10^{19} cm^{-3}. Nowadays, metal gates are preferred over polysilicon gates because polysilicon shows a poly-depletion effect, thereby affecting the EOT of the device. Also, polysilicon gates are chemically unstable when in contact with high-k dielectrics. Titanium nitride (TiN) is used as the metal gate with a work function (ϕ_m) equal to 4.65 eV due to its thermal stability, high purity, low resistivity, and compatibility with CMOS processing [31, 32]. Temperature (T) is kept at 300 K, and gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) are altered from 0 V to 1.5 V and 0 V to 0.5 V, respectively. In amplifier circuits, the region of operation is decided by gate overdrive voltage (V_{gt}). So, all the analog and RF analyses have been done against V_{gt}. It is the difference between gate-source and threshold voltage, i.e., $V_{gt} = V_{gs} - V_{th}$.

Silicon material is used in the fin structure with H_{Fin} and W_{Fin} fixed at 10 nm and 5 nm, respectively, following the width quantization property, which says that W_{Fin} must be a multiple of H_{Fin} [33]. To examine the impact of the fin AR on important static, analog, and RF parameters, the proposed device's effective channel area has been kept constant at 80 nm^2 while varying the H_{Fin} and W_{Fin} because if the effective channel area ($H_{Fin} \times W_{Fin}$) has not been kept constant to a particular value, then all the related electrical parameters and the channel's conductance will be altered [34]. Table 2.1 portrays the three different configurations used for simulation placed in increasing fin aspect ratio order. The

Table 2.1: Different device configurations used for simulation [22].

Configuration No.	Fin Height, H_{Fin} (nm)	Fin Width, W_{Fin} (nm)	Effective Channel Area $H_{Fin} \times W_{Fin}$ (nm^2)	Fin Aspect Ratio, H_{Fin}/W_{Fin}
C1	10	8	80	1.25
C2	16	5	80	3.2
C3	20	4	80	5

SILVACO ATLAS 3D simulator has simulated all three different configurations [35]. In addition to Poisson and Continuity equations, alternate equations are essential for error-free and practical results. Thus, the device simulation includes a variety of physical models that are described using Equations (2.1-2.5).

1. **Shockley-Read-Hall (SRH) recombination model** includes the effect of recombination and generation.

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{E_{Trap}}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-E_{Trap}}{kT_L}\right)\right]} \quad (2.1)$$

where k signifies the Boltzmann's constant, τ_n and τ_p denote the electron and hole lifetimes, E_{TRAP} is the difference between intrinsic Fermi level and trap energy level, and T_L is the lattice temperature.

2. **Arora analytical model** correlates the low-field carrier mobility with impurity concentration and temperature.

$$\mu_n = 88\left(\frac{T_L}{300}\right)^{-0.57} + \frac{1252\left(\frac{T_L}{300}\right)^{-2.33}}{1 + \frac{N}{1.432\times10^{17}\left(\frac{T_L}{300}\right)^{2.546}}} \quad (2.2)$$

where N is the total local dopant concentration, and T_L is the lattice temperature.

3. **Klaassen band-to-band tunneling model** accounts for the electrons tunneling between the valence and conduction band.

$$G_{BBT} = D \times BB.A \times E^{BB.GAMMA}\exp\left(-\frac{BB.B}{E}\right) \quad (2.3)$$

where E signifies the electric field magnitude, D denotes the statistical factor, and BB.A, BB.B, BB.GAMMA are user-definable parameters.

4. **Crowell-Sze impact ionization model** introduces the impact ionization effects.

$$\alpha_{n,p} = \frac{1}{\lambda}\exp[C_0(r) + C_1(r)x + C_2(r)x^2] \quad (2.4)$$

where λ denotes the carrier mean free path for optical phonon generation and $C_0(r)$, $C_1(r)$, and $C_2(r)$ are the ionization coefficients.

5. **Fermi-Dirac statistics model** enhances the result accuracy.

$$f(\varepsilon) = \frac{1}{1+\exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \tag{2.5}$$

where E_F indicates the Fermi level and ε is the energy of the available electron state. Additionally, Newton and Gummel's methods are used to achieve a solution [35].

2.3 EXPERIMENTAL CALIBRATION

The Gate-All-Around (GAA) FinFET is calibrated with the experimental data extracted from Lee et al. [36] to validate the above-discussed physical models. The experimental data is calibrated by considering silicon material in the entire fin region with fixed device dimensions (L_g = 5 nm, H_{Fin} = 14 nm, and W_{Fin} = 3 nm), as mentioned in the paper, to authenticate the simulations. **Figure 2.2(a)** and **Figure 2.2(b)** describe the experimental and simulated transfer and output characteristics of the GAA FinFET, respectively. The selection of simulation models is validated due to the close agreement between the experimental and simulated data sets.

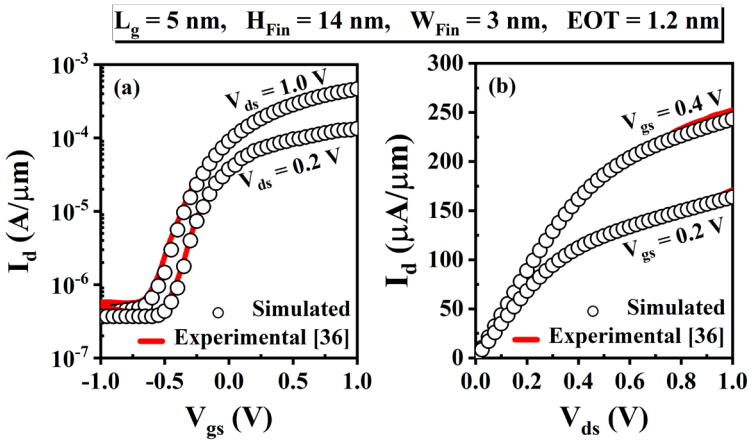

Figure 2.2: Experimental and simulated (a) transfer and (b) output characteristics of the GAA Si FinFET [22, 36].

2.4 FABRICATION FEASIBILITY

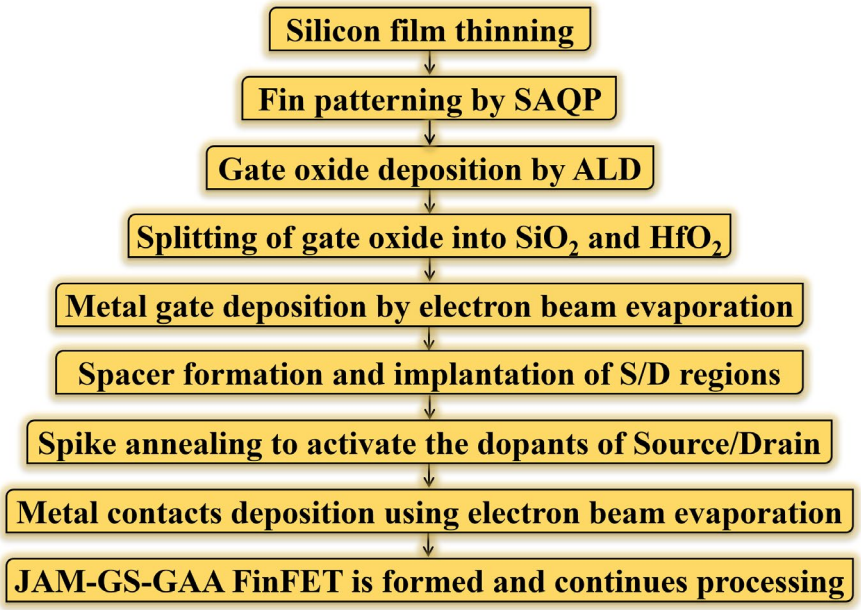

Figure 2.3: JAM-GS-GAA FinFET step-by-step fabrication outline [22].

A step-by-step device fabrication outline of JAM-GS-GAA FinFET is displayed in **Figure 2.3** to demonstrate the fabrication feasibility of the proposed device. The initial step is to thin the silicon film, followed by fin patterning using the self-aligned quadruple patterning (SAQP) method [37]. When two self-aligned double patternings (SADP) are applied in a row to enhance the feature density, it is known as SAQP. The gate dielectric (SiO_2/HfO_2) is deposited on the silicon interfacial layer by atomic layer deposition (ALD) [38]. Then, the TiN metal gate is deposited using electron beam evaporation at room temperature on the top of the gate dielectric [38]. The source and drain regions are implanted and then spike annealed to activate the source and drain region dopants. The source/drain metal contacts are deposited by electron beam evaporation followed by lift-off. The JAM-GS-GAA FinFET is formed and continues processing.

2.5 RESULTS AND DISCUSSION

2.5.1 Device Scalability

Equations (2.6-2.8) provide the current equations used to estimate the device performance in three different regions of operation: the cut-off, linear, and saturation regions.

$$I_d = \left(\frac{\mu C_{ox} W}{L}\right)(\eta - 1)\, V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{\eta\, V_T}\right)\left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \quad \text{(cut-off region)} \quad (2.6)$$

$$I_d = \left(\frac{\mu C_{ox} W}{L}\right)(V_{gs} - V_{th} - 0.5\, V_{ds})\, V_{ds} \quad \text{(linear region)} \quad (2.7)$$

$$I_d = \left(\frac{\mu C_{ox} W}{2L}\right)(V_{gs} - V_{th})^2 (1 + \lambda\, V_{ds}) \quad \text{(saturation region)} \quad (2.8)$$

where I_d is drain current, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W is channel width, L is channel length, η is subthreshold swing coefficient, V_T is the thermal voltage, V_{gs} is gate-source voltage, V_{th} is the threshold voltage, V_{ds} is drain-source voltage, and λ is the channel length modulation parameter. **Figure 2.4(a)** shows the variation of drain current (I_d) with V_{gs} at V_{ds} = 0.5 V in both linear and log scales for different configurations. It is observed that I_d increases with the increase in the V_{gs} and is maximum for GS-GAA FinFET structure. Also, it is found that I_{off} reduces significantly in GS-GAA FinFET configuration due to the enhanced gate coupling capacitances and reduced tunneling current. Consequently, as shown in **Figure 2.4(b)**, a higher switching ratio (I_{on}/I_{off}) and superior switching speed are obtained for the GS-GAA FinFET configuration. **Figure 2.4(c)** represents the threshold voltage (V_{th}) plot for conventional FinFET, GAA FinFET, and GS-GAA FinFET. The V_{th} increases sequentially and recorded maximum for GS-GAA FinFET due to the enhanced control over the channel and better shielding of drain-side potential by the GAA structure, thereby improving the subthreshold characteristics [39]. In designing a microscopic device, the subthreshold swing (SS) is an

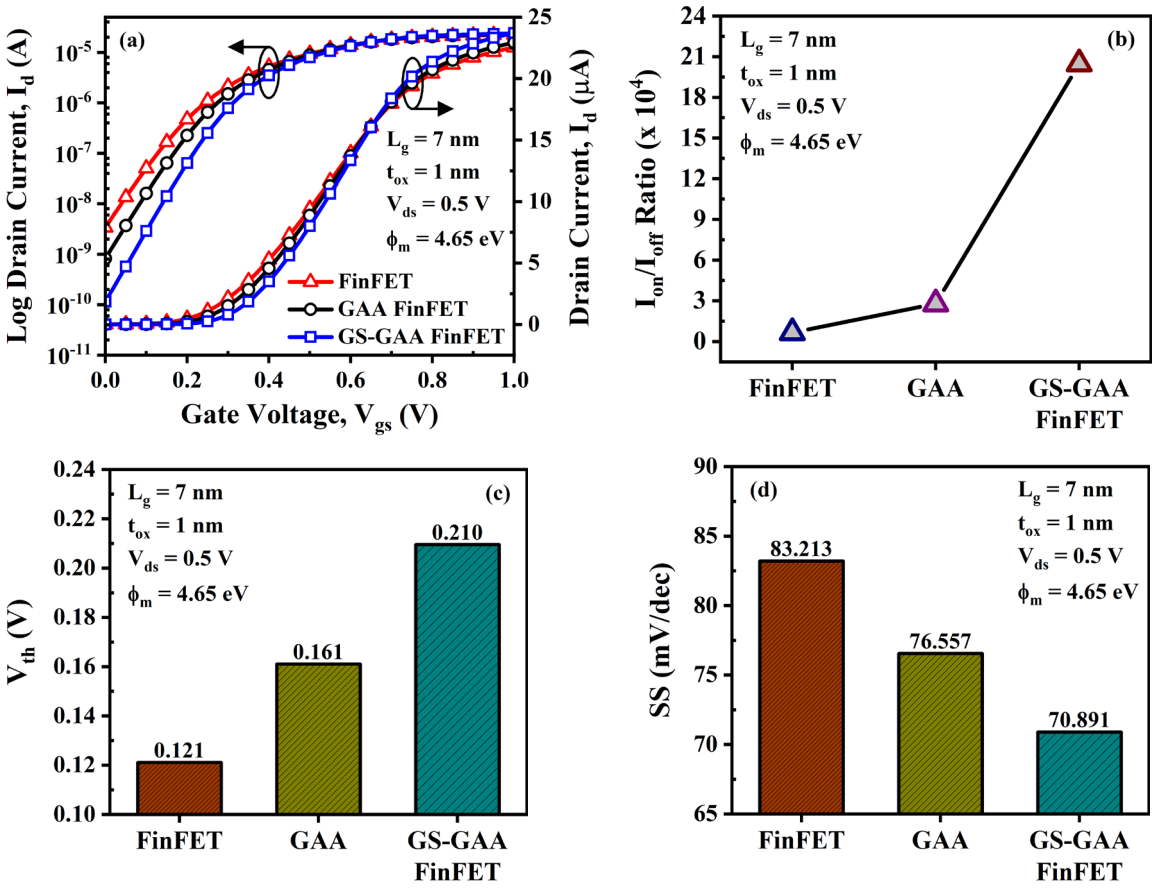

Figure 2.4: (a) Variation of I_d - V_{gs} in linear and log scales, (b) I_{on}/I_{off} ratio, (c) V_{th}, and (d) SS comparisons for different configurations [13].

essential short-channel parameter. It is visible from **Figure 2.4(d)** that SS is the lowest and nearest to its ideal value (60 mV/dec) for the GS-GAA FinFET configuration because the gate coupling capacitance increases as the permittivity (k) increases, which increases the gate control on the channel, leading to a decreased SS.

2.5.2 Analog Performance

In this subsection, from the perspective of the analog applications, several important analog parameters such as transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), early voltage (V_{EA}), and intrinsic gain (A_v) are evaluated. Equations (2.9) and (2.10) estimate g_m and TGF, respectively, and both parameters should

be high for better analog performance [40]. **Figure 2.5(a)** outlines a collaborated plot of g_m and TGF as a function of V_{gt} for all three different configurations. Transconductance is a parameter that computes the change in drain current to the shift in V_{gs} at constant V_{ds}. Thus, g_m is obtained from the derivative of the I_d - V_{gs} curve. Compared to their counterparts, the GS-GAA FinFET structure has the maximum value of transconductance because of the enhanced gate control on the channel and reduced short-channel effects. Also, gate-stack architecture enhances the average carrier velocity, resulting in improved electron mobility and g_m [41]. The transconductance generation factor is the proportion of gain generated per unit of power dissipated. The device operating at low supply voltages performs more efficiently for higher values of TGF. It is observed from **Figure 2.5(a)** that the TGF changes

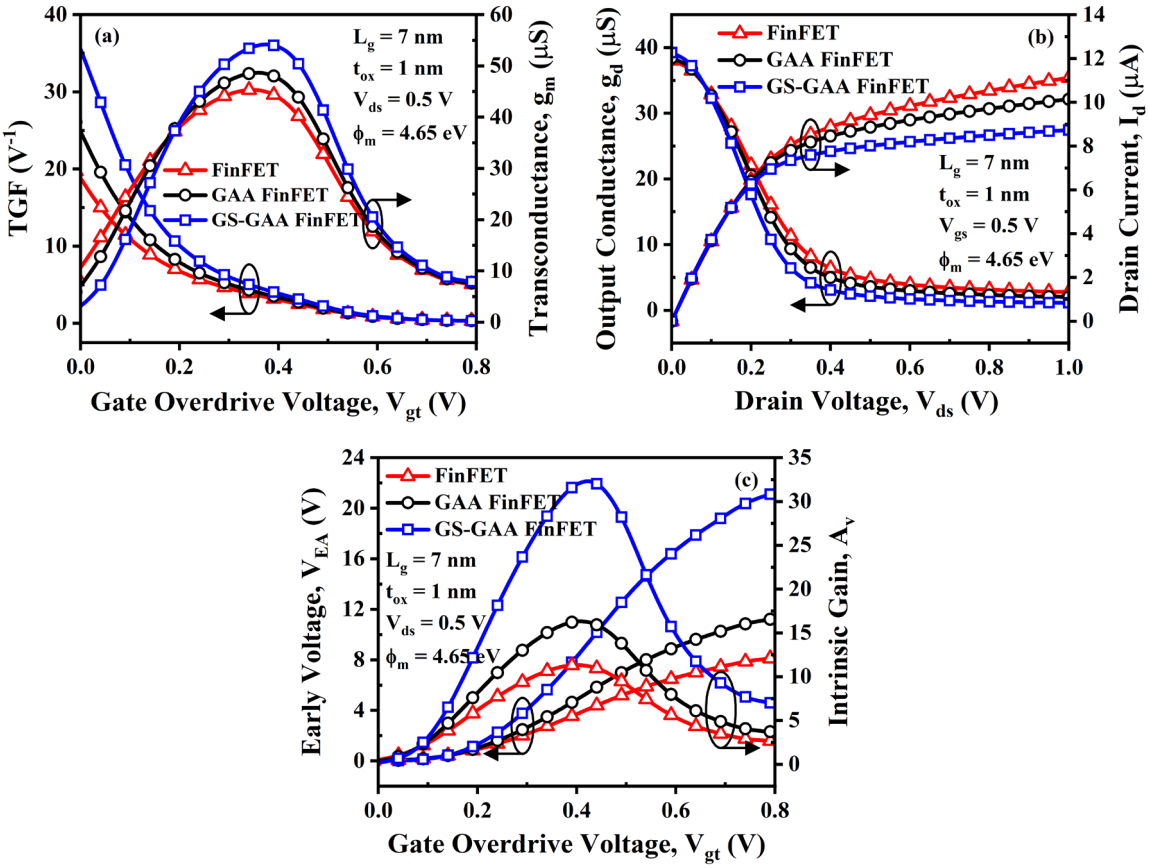

Figure 2.5: (a) g_m and TGF vs. V_{gt}, (b) g_d and I_d vs. V_{ds}, and (c) V_{EA} and A_v vs. V_{gt} for different structures [13].

only in the subthreshold region, with almost the same value in the strong inversion region. GS-GAA FinFET configuration achieves the maximum value of TGF and is closest to its ideal value of 40 V^{-1} at the device's minimum SS (60 mV/dec). This is because the higher value of I_d corresponds to higher g_m and, consequently, higher TGF.

$$g_m = \partial I_d / \partial V_{gs} \tag{2.9}$$

$$TGF = g_m / I_d \tag{2.10}$$

$$g_d = \partial I_d / \partial V_{ds} \tag{2.11}$$

$$V_{EA} = I_d / g_d \tag{2.12}$$

$$A_v = g_m / g_d = (g_m / I_d) \times V_{EA} \tag{2.13}$$

Figure 2.5(b) represents a combined plot of I_d and g_d as a function of V_{ds} at constant V_{gs} = 0.5 V. The g_d determines the driving ability of a device, as defined in Equation (2.11) [40]. The region of device operation determines the value of g_d. Initially, g_d is large in the linear region but keeps on decaying as V_{ds} increases beyond pinch-off voltage due to drain-induced barrier lowering (DIBL) and channel length modulation (CLM) [42]. In the saturation region, g_d maintains an almost constant value. Thus, due to increased gate controllability and suppressed short channel effects, g_d is the minimum for the GS-GAA FinFET compared to their counterparts. Moreover, as depicted in **Figure 2.5(b)**, lower g_d means higher output resistance, which means less increase in the drain current with V_{ds} in the saturation region. The V_{EA} and A_v are evaluated using Equations (2.12) and (2.13), respectively, and they must be as high as possible for the enhanced analog performance of the device [40]. **Figure 2.5(c)** shows the variation of V_{EA} and A_v against V_{gt} for all three configurations. The V_{EA} peak value is obtained for the GS-GAA FinFET structure due to the reduction in short channel effects, as demonstrated in Table 2.2. Also, the highest peak of A_v is observed for the GS-GAA FinFET structure because of higher g_m and lower g_d.

Table 2.2: Summary of electrostatic and analog parameters for different structures [13].

Parameter	Unit	FinFET	GAA FinFET	GS-GAA FinFET
I_{on}	(μA)	22.54	22.94	23.72
I_{off}	(A)	34.04×10^{-10}	8.22×10^{-10}	1.16×10^{-10}
I_{on}/I_{off} Ratio	-	6.62×10^{3}	27.89×10^{3}	204.72×10^{3}
V_{th}	(V)	0.121	0.161	0.210
SS	(mV/dec)	83.213	76.557	70.891
g_m	(μS)	45.30	48.50	54.01
TGF	(V^{-1})	19.71	26.09	37.09
V_{EA}	(V)	8.11	11.21	21.11
A_v	-	11.30	16.21	32.02

2.5.3 RF Performance

From the RF application's point of view, RF parameters of vital interest are cut-off frequency (f_T), maximum oscillation frequency (f_{max}), gain frequency product (GFP), transconductance frequency product (TFP), and gain transconductance frequency product (GTFP). **Figure 2.6(a)** shows the variation of the gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) as a function of V_{gt}. The C_{gs} is plotted in log scale, and C_{gd} is on a linear scale to differentiate between the curves. AC small-signal analysis has been performed to extract the values of C_{gs} and C_{gd} at an operating frequency of 1 MHz with DC voltage ramped from 0 V to 1 V with a step size of 0.05 V. It is observed from **Figure 2.6(a)** that in the subthreshold region, both C_{gs} and C_{gd} increase very slowly with V_{gt}, but with a further increase, C_{gs} and C_{gd} increase swiftly due to the enhanced lateral field, which increases the movement of charge carriers from source side to drain side. In the superthreshold region, as expected, C_{gs} and C_{gd} become constant due to the non-contribution of V_{ds}. The GS-GAA FinFET structure exhibits higher C_{gs} and C_{gd} than other

devices because gate capacitance increases with the dielectric permittivity [43]. In **Figure 2.6(b)**, total gate capacitance (C_{gg}) and f_T are displayed as a function of V_{gt} for all three devices. The variation of C_{gg} with V_{gt} is the same as that of C_{gs} and C_{gd} because C_{gg} is the sum of C_{gs} and C_{gd}. Generally, the frequency at which current gain becomes unity (0 dB) is known as f_T and is calculated using Equation (2.14) [40]. As shown in **Figure 2.6(b)**, f_T decreases slightly for the GS-GAA FinFET structure compared to the other two designs. It happens mainly due to the enhanced value of C_{gs} and C_{gd}, although a higher value of g_m significantly compensates for the deteriorating f_T.

$$f_T = g_m/2\pi\left(C_{gs} + C_{gd}\right) \tag{2.14}$$

$$f_{max} = f_T/\sqrt{4\,R_g(g_{ds} + 2\pi\,f_T\,C_{gd})} \tag{2.15}$$

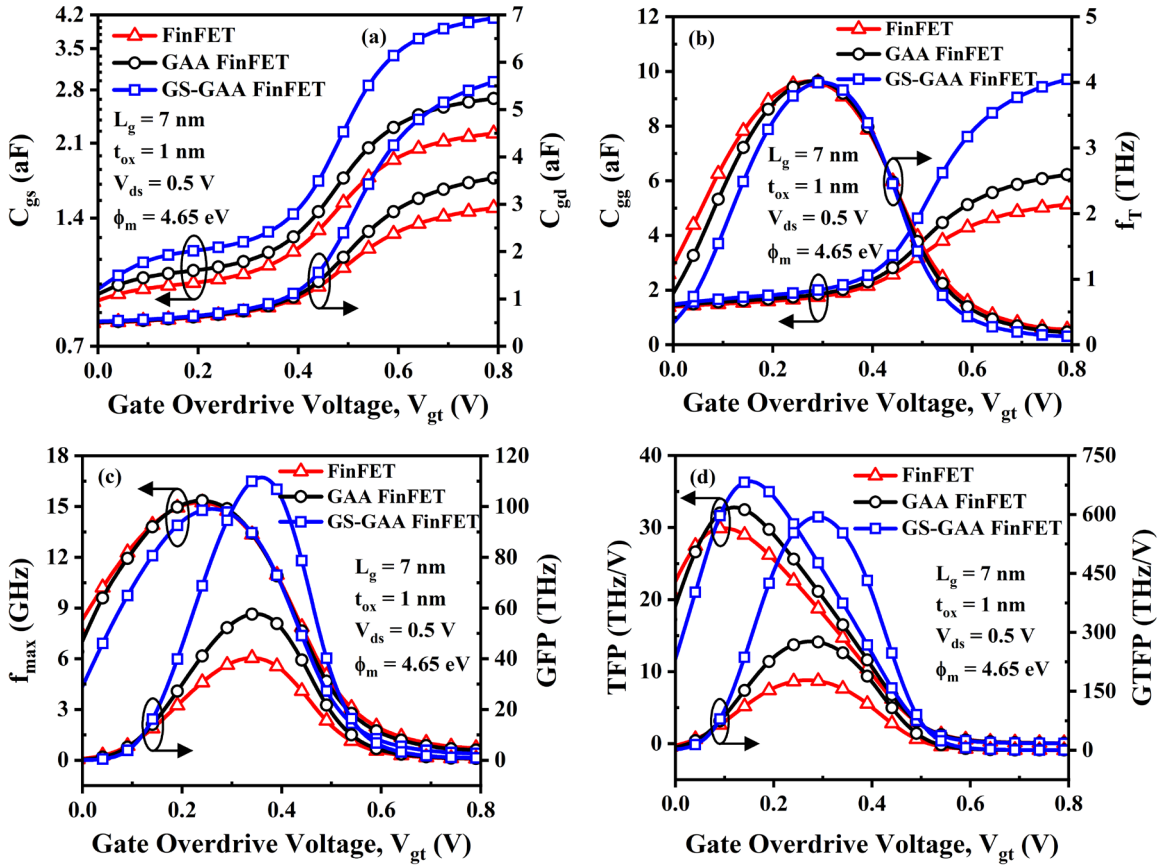

Figure 2.6: Variation of (a) C_{gs} and C_{gd} to V_{gt}, (b) C_{gg} and f_T to V_{gt}, (c) f_{max} and GFP to V_{gt}, and (d) TFP and GTFP to V_{gt} for each configuration [13].

Figure 2.6(c) represents the f_{max} and GFP with respect to V_{gt} for each device structure. The frequency at which maximum unilateral power gain becomes unity (0 dB) is known as the f_{max}. It is evaluated using Equation (2.15) in which f_T, R_g, g_{ds}, and C_{gd} denote the cut-off frequency, gate resistance, drain-source output conductance, and gate-drain capacitance, respectively [40]. The values of R_g and g_{ds} are extracted using AC small-signal analysis at an operating frequency of 1 MHz with DC voltage ramped from 0 V to 1 V with a step size of 0.05 V [44, 45]. In **Figure 2.6(c)**, f_{max} is slightly lower for GS-GAA FinFET in the subthreshold and superthreshold regions than their counterparts. It is due to the enhanced parasitic capacitances in the GS-GAA FinFET structure. The GFP is an essential parameter in high-frequency applications, as specified in Equation (2.16) [40]. It is noticed from **Figure 2.6(c)** that GFP increases as the V_{gt} increases and then attains a maximum peak before falling to a constant value in the saturation region. GS-GAA FinFET configuration records the highest value of GFP due to the improved value of g_m and g_d with a minimal decrease in f_T.

$$\mathrm{GFP} = (g_m/g_d) \times f_T \tag{2.16}$$

$$\mathrm{TFP} = (g_m/I_d) \times f_T \tag{2.17}$$

$$\mathrm{GTFP} = (g_m/g_d) \times (g_m/I_d) \times f_T \tag{2.18}$$

The other important RF parameters are the TFP and the GTFP, as expressed in Equations (2.17) and (2.18), respectively [40]. TFP is mainly utilized in high-speed designs as it exhibits an agreement between bandwidth and power. **Figure 2.6(d)** depicts the TFP and GTFP against V_{gt} for each configuration. The graph plotted for GTFP is calibrated by intrinsic gain and switching speed. The curve reflects that both TFP and GTFP increase as V_{gt} increases and reach a maximum value at a particular value of V_{gt}. With further increase in V_{gt}, both TFP and GTFP decrease owing to an increase in C_{gg} and maintain a minimum

constant value as V_{gt} reaches a saturation region. Again, for both TFP and GTFP, the highest value is obtained for the GS-GAA FinFET structure due to the enhanced value of g_m, TGF, and the reduced value of g_d with almost equivalent f_T. Thus, the proposed JAM-GS-GAA FinFET may be a promising option for designing analog and RF circuits. In Table 2.3, the values of different RF parameters are tabulated.

Table 2.3: Summary of RF parameters for different structures [13].

Parameter	Unit	FinFET	GAA FinFET	GS-GAA FinFET
C_{gs}	(aF)	2.21	2.67	4.12
C_{gd}	(aF)	2.92	3.55	5.58
C_{gg}	(aF)	5.13	6.22	9.71
f_T	(THz)	4.00	4.02	4.00
f_{max}	(GHz)	15.24	15.35	14.78
GFP	(THz)	40.32	57.59	109.93
TFP	(THz/V)	29.87	32.47	36.28
GTFP	(THz/V)	176.11	275.12	593.78

2.5.4 Fin Aspect Ratio Optimization for Static Performance

In this subsection, vital static parameters like the electric field, energy band profiles, surface potential, electron concentration, etc., are examined to optimize the fin AR for superior device performance. The electric field alteration with the channel distance for each configuration is displayed in **Figure 2.7(a)**. A lower electric field is acquired at the drain end than at the source end. In addition, because of almost the same electric field at both the drain and source end for each configuration, the channel region charge carriers accelerate, resulting in an enhanced electron injection velocity from the source to the channel region [46, 47]. A higher electric field is witnessed for the C3 configuration than their channel region counterparts. **Figure 2.7(b)** reveals the contour plot of the electric field for all three

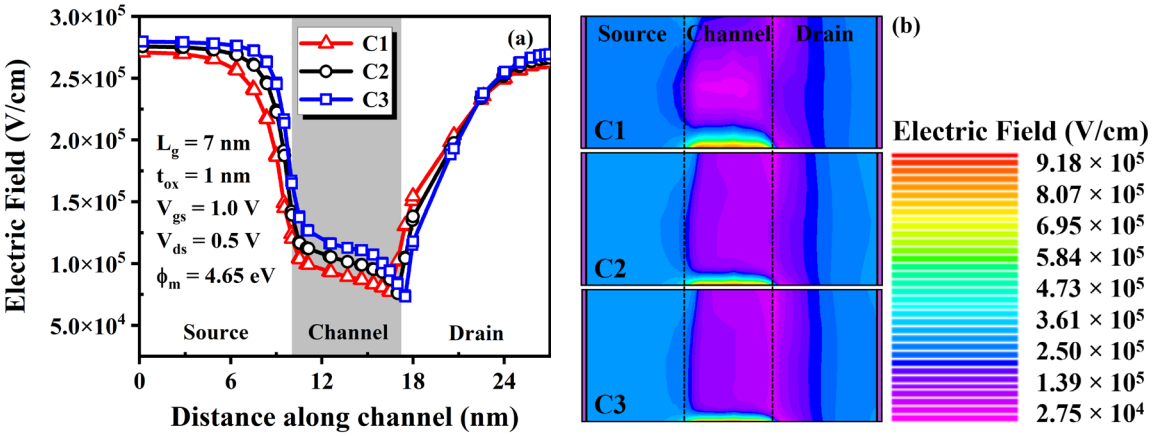

Figure 2.7: (a) Change in the electric field with the channel distance and (b) electric field contour plot for considered fin aspect ratio configurations [22].

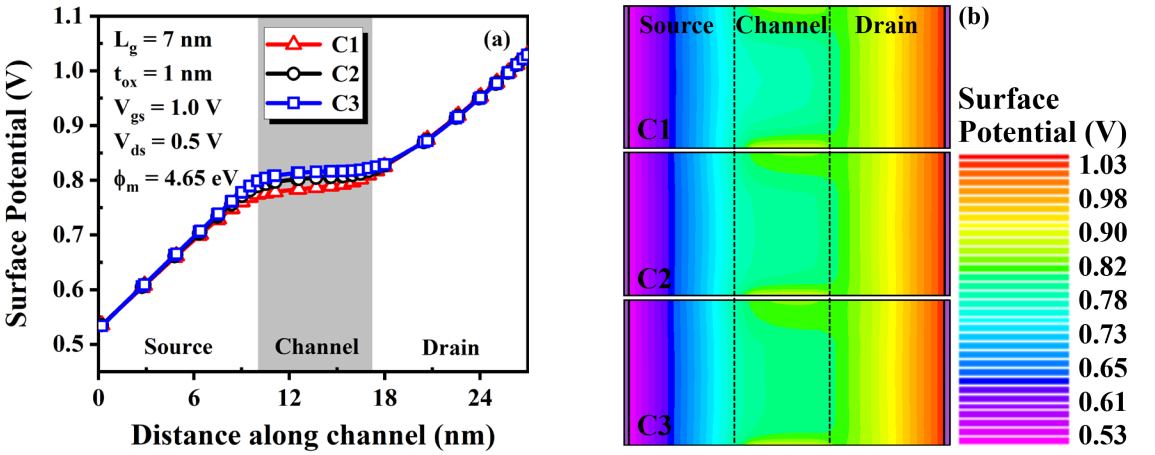

Figure 2.8: (a) Surface potential profile variation along the channel distance and (b) surface potential contour of all three fin aspect ratio configurations [22].

configurations, confirming the rise in the electric field with the rise in the fin AR. The surface potential profile along the channel distance for the respective configurations is plotted in **Figure 2.8(a)**. Due to the lower electric field at the drain end compared to the source end, surface potential improves significantly in the channel region for the C3 configuration, indicating a boost in the device surface potential with the increase in the fin AR. The surface potential contour for all three configurations is presented in **Figure 2.8(b)**, confirming the increase with the fin AR rise.

Figure 2.9(a) portrays the plot of electron concentration against the distance along the channel for each mentioned configuration. It is evident from the graph that for the C3

configuration, electron concentration increases considerably in the channel region due to the decreased electric field at the drain end compared to the source end. This surge in the concentration of electrons inside the channel region with the fin AR enhances the current drivability and improves the leakage current. The electron concentration contour profile of each simulated device is presented in **Figure 2.9(b)**. Conduction and valence band energy is represented against the distance across the channel for all three simulated devices in

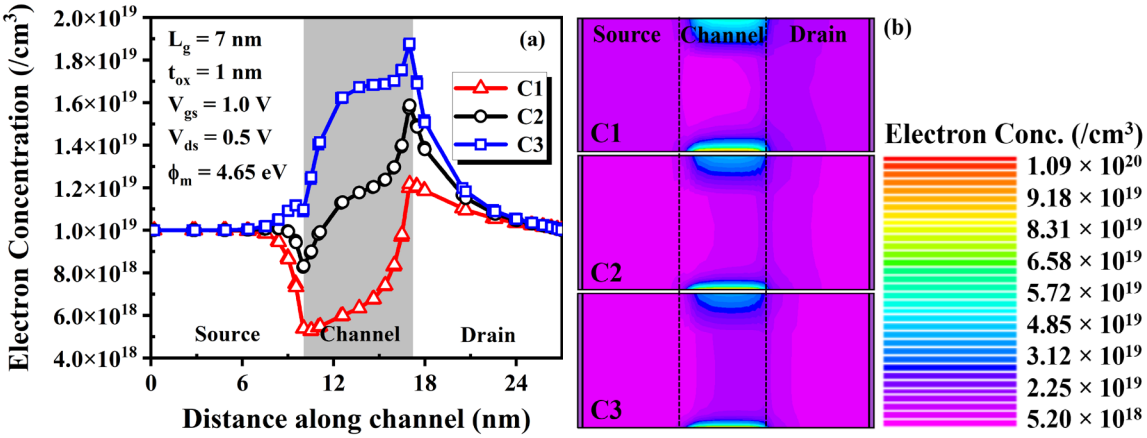

Figure 2.9: (a) Electron concentration plot against the distance along the channel and (b) electron concentration contour profile of each fin aspect ratio configuration [22].

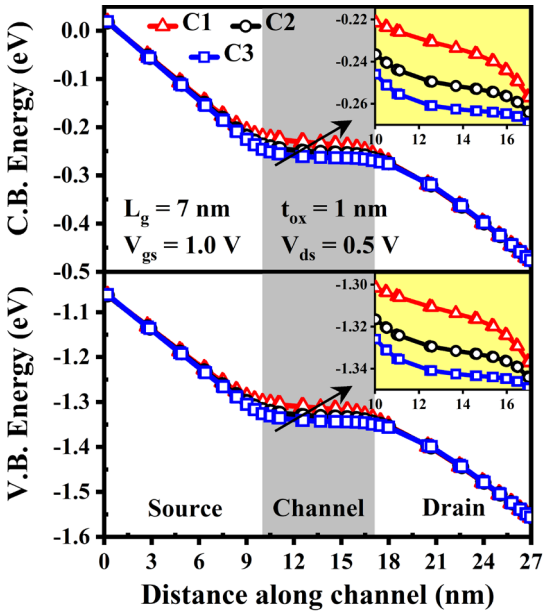

Figure 2.10: Conduction and valence band energy against the distance across the channel for all considered fin aspect ratio configurations [22].

Figure 2.10. It is observed that in the channel region, conduction and valence band energy reduces with the rise in the fin AR. The channel region inset graph demonstrates the decrease in the conduction and valence band energy with fin AR, indicating improvement in the ON and OFF current of the device. Thus, the static parameters improve appreciably with the rise in fin AR, resulting in enhanced device performance for the C3 configuration.

2.5.5 Fin Aspect Ratio Optimization for Analog Performance

This section optimizes the fin AR for enhanced device analog performance by exploring crucial analog parameters. **Figure 2.11(a)** and **Figure 2.11(b)** represent the transfer characteristics (I_d - V_{gs}) at V_{ds} = 0.5 V in linear and log scales for different configurations.

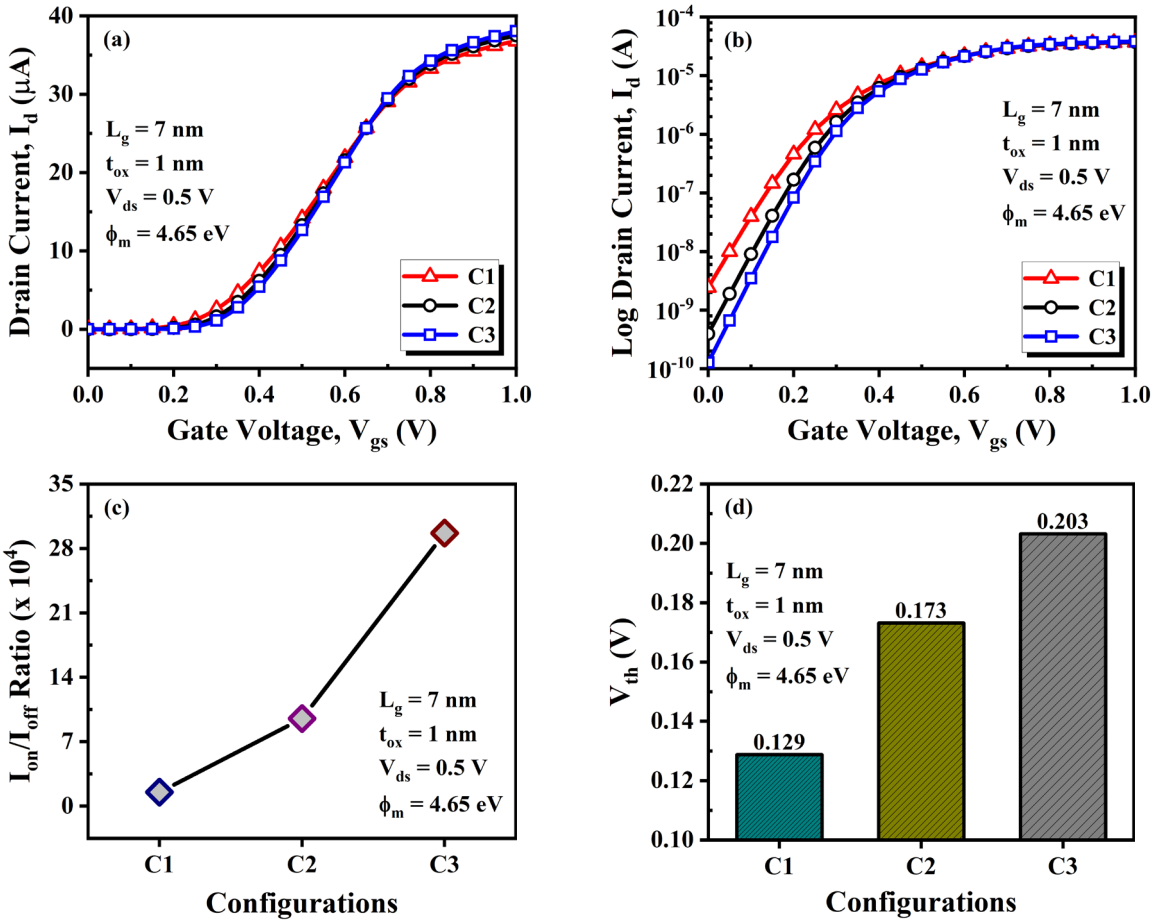

Figure 2.11: Variation of I_d - V_{gs} in (a) linear and (b) log scales, (c) I_{on}/I_{off} ratio, and (d) V_{th} for different fin aspect ratio configurations [22, 28].

It is observed that compared to the other two structures, the C3 configuration acquires the maximum value of I_d because the current drivability of the device rises with the increase in fin AR. The I_{off} also improves as the fin AR increases, as shown in **Figure 2.11(b)**. I_{off} improves significantly for the C3 configuration compared to the C1 configuration. **Figure 2.11(c)** depicts the I_{on}/I_{off} ratio plot against the fin AR for each configuration. The I_{on}/I_{off} ratio increased by 19.58 times for the C3 configuration compared to the C1 configuration owing to increased I_d and reduced I_{off}. **Figure 2.11(d)** demonstrates the change in V_{th} with respect to the fin AR. The V_{th} obtained for the C1, C2, and C3 configurations is 0.129 V, 0.173 V, and 0.203 V, respectively. This points out that V_{th} rises sequentially with the increase in the fin AR, thus enhancing the subthreshold device characteristics.

Figure 2.12(a) depicts the SS for all three configurations, and it is observed that SS reduces for a higher fin AR, and the lowest value is obtained for the C3 configuration compared to the other two configurations. In **Figure 2.12(b)**, g_m is plotted as a function of V_{gt} for different fin AR configurations. It is observed that g_m increases as the fin AR increases due to the increased drain current and decreased electric field at the drain end. Quality factor (QF) is a vital parameter that primarily defines the device switching behavior and is given as QF = g_m/SS [48]. The maximum value of g_m has been considered for the QF evaluation. **Figure 2.12(c)** exhibits the QF for all three simulated devices and shows that QF rises with fin AR. This surge in the QF value with the fin AR increase is due to the enhanced g_m and reduced SS. **Figure 2.12(d)** represents the variation of TGF with V_{gt} for each fin AR configuration. The variation in the TGF is observed only in the subthreshold region, with almost no change in the strong inversion region. TGF increases with the fin AR because the higher value of I_d corresponds to higher g_m, so higher TGF is recorded for the C3 configuration.

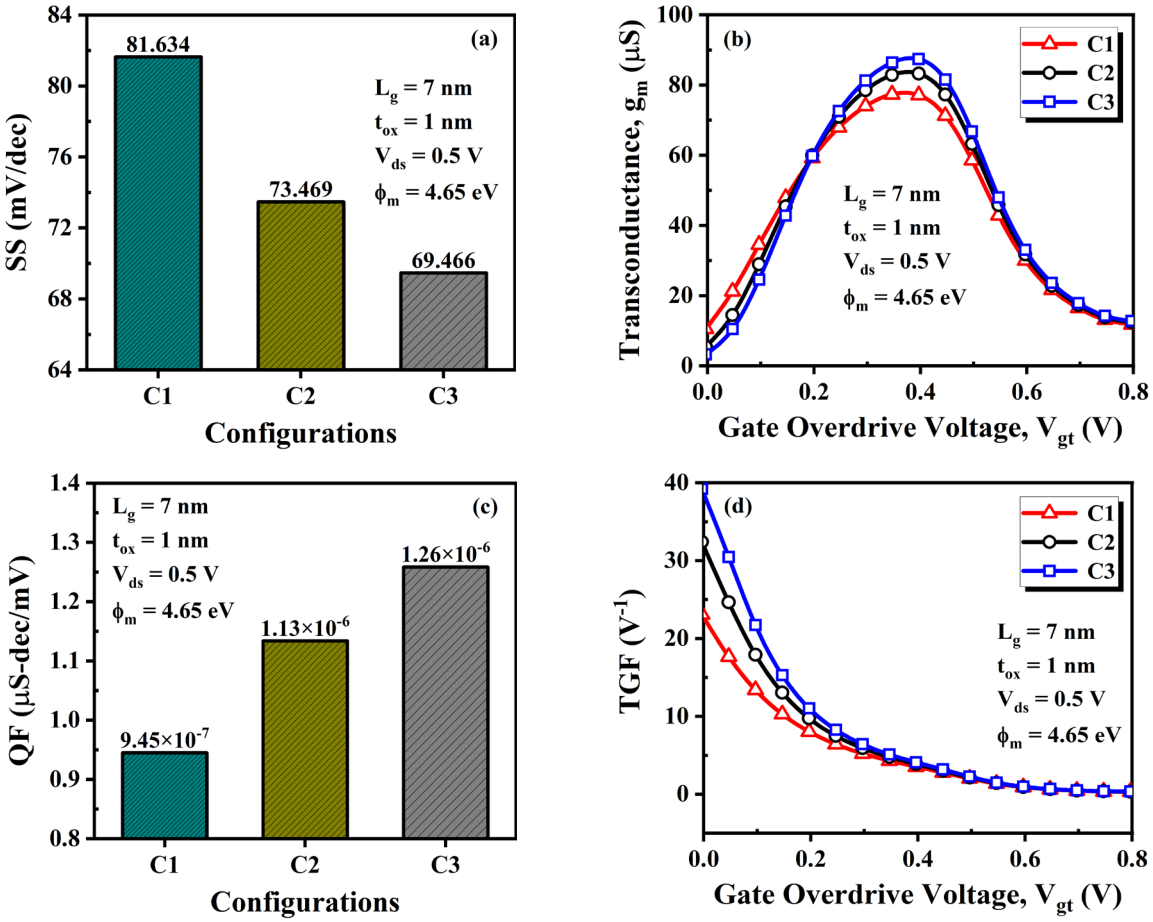

Figure 2.12: Comparison of (a) SS, (b) g_m, (c) QF, and (d) TGF for different fin aspect ratio configurations [22, 28].

Figure 2.13(a) represents the g_d variation against V_{ds} for each simulated configuration. The g_d decreases with an increase in V_{ds} in the active region before maintaining a constant value in the saturation region. Further, g_d decreases in both active and saturation regions with increased fin AR, demonstrating the suppressed SCEs and improved gate controllability. The inverse of g_d is known as output resistance (R_{out}), and it determines the device's available power gain. The deviation in R_{out} alongside fin AR is displayed in **Figure 2.13(b)**. The increase in R_{out} with the increase in fin AR is observed in both regions, with the rise in the saturation region being significantly higher than the active region. Compared to the C1 configuration, the C3 configuration acquires a 77.83% and

101.12% increase in the active and saturation regions. **Figure 2.13(c)** and **Figure 2.13(d)** demonstrate the alteration in A_v and V_{EA} against fin AR for each configuration considered. An extensive enhancement in both parameters is witnessed with the rise in fin AR. This increase with fin AR is due to the reduced g_d and enhanced g_m and I_d. Therefore, superior device performance is attained for the C3 configuration, showcasing that the analog parameters enhance noticeably with the increase in the fin AR.

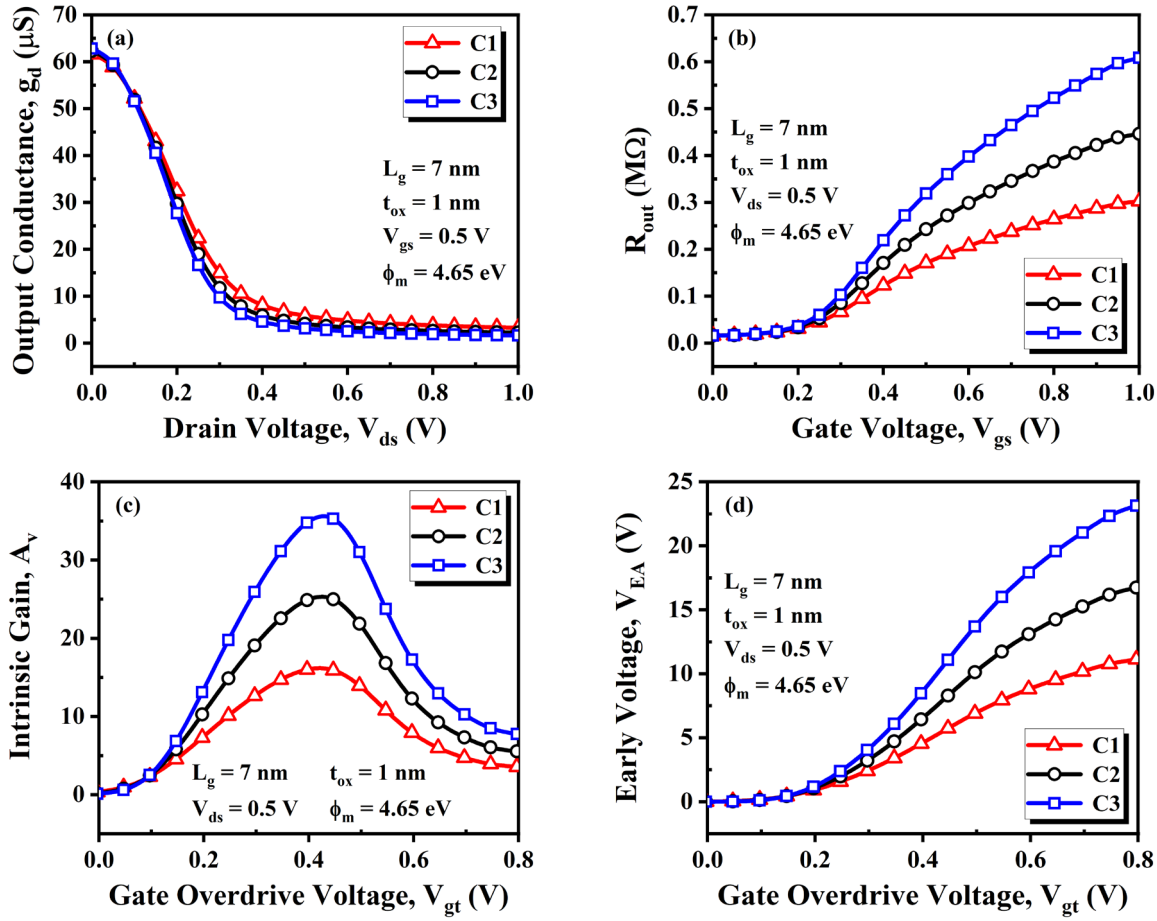

Figure 2.13: Variation of (a) g_d, (b) R_{out} against V_{ds}, (c) A_v, and (d) V_{EA} against V_{gt} for different fin aspect ratio configurations [22].

2.5.6 Fin Aspect Ratio Optimization for RF Performance

This section optimizes the fin AR for improved device RF performance by investigating critical RF parameters. In **Figure 2.14(a)**, **Figure 2.14(b)**, and **Figure 2.14(c)**, C_{gs}, C_{gd}, and

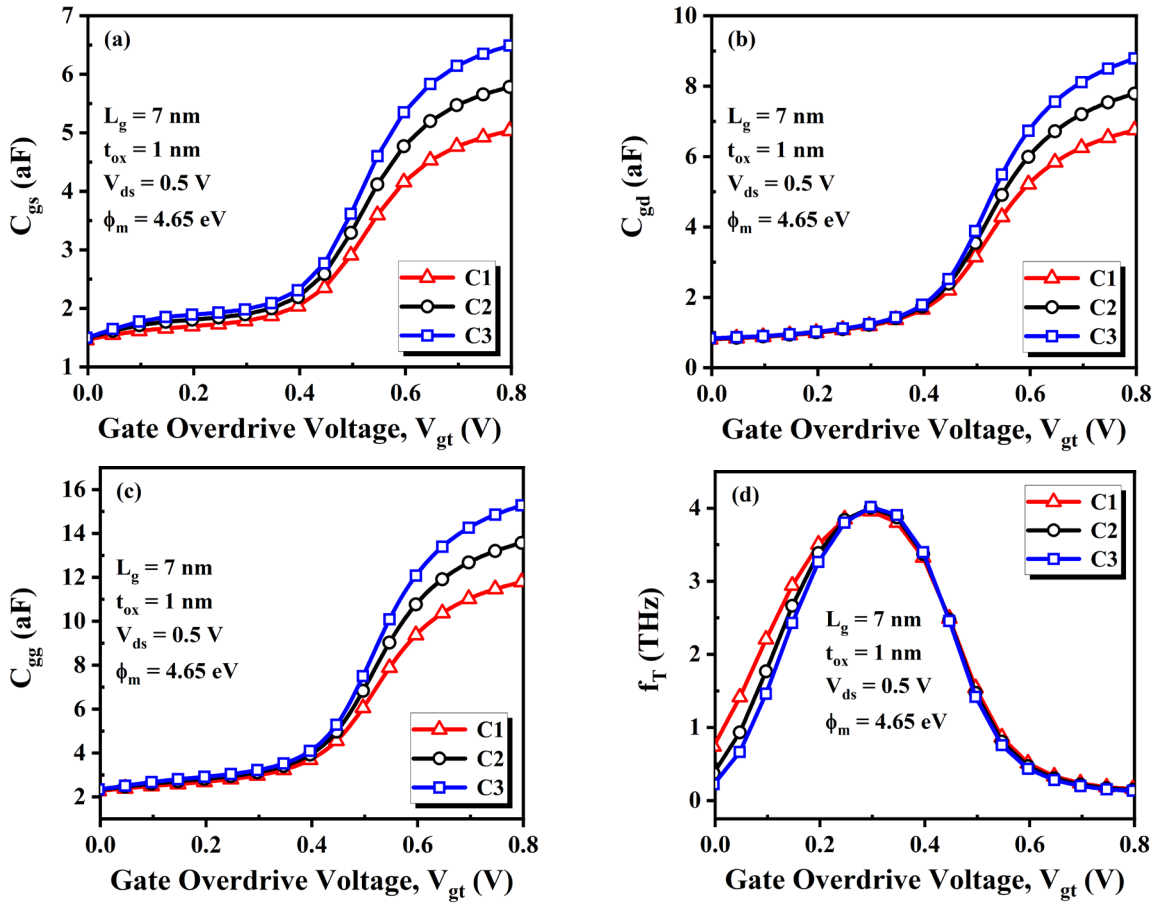

Figure 2.14: (a) C_{gs}, (b) C_{gd}, (c) C_{gg}, and (d) f_T as a function of V_{gt} for different fin aspect ratio configurations [28].

C_{gg} are displayed as a function of V_{gt} for all three configurations. Compared to the C1 configuration, a higher value of C_{gs}, C_{gd}, and C_{gg} is obtained for the C3 configuration. The fundamental reason is that as the fin AR increases, i.e., either the fin gets taller or narrower or both, the fringing field in the device increases, which in turn enhances the capacitance in the device. **Figure 2.14(d)** outlines the plot of f_T against V_{gt}. It is observed that f_T increases with the fin AR, and a slightly greater f_T value is obtained for the C3 configuration than the other two configurations. The rise in f_T is minimal due to the increased value of C_{gs} and C_{gd}, suppressing the enhancement in g_m.

Figure 2.15(a) exhibits the plot of f_{max} as a function of V_{gt} for all three configurations. It is observed that f_{max} increases with the increase in the fin AR, with the

C3 configuration obtaining a maximum value. It is because g_{ds} reduces significantly for higher fin AR, with f_T being almost the same. The plot of GFP with respect to V_{gt} for each configuration is shown in **Figure 2.15(b)**. It has been demonstrated that GFP rises as fin AR rises because A_v improves considerably, although f_T is about the same. **Figure 2.15(c)** and **Figure 2.15(d)** depict the TFP and GTFP plots against V_{gt} for each configuration. The curve reflects that both TFP and GTFP increase as the fin AR increases, and the highest value is obtained for the C3 configuration due to the enhanced value of g_m, TGF, f_T, and the reduced value of g_d. Compared to the C1 configuration, the C3 configuration produces a 22.82% increase in TFP value and a 2.55 times increase in GTFP value. Hence, RF

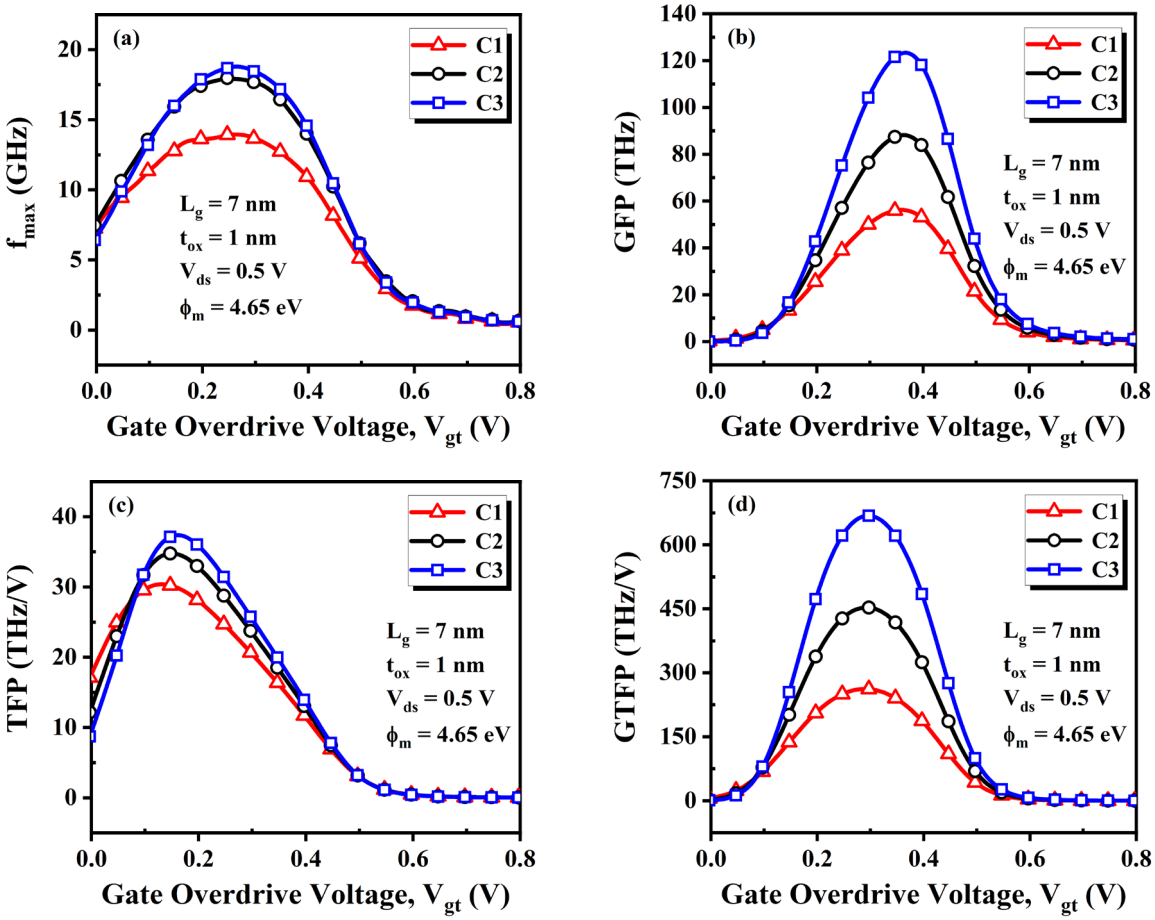

Figure 2.15: (a) f_{max}, (b) GFP, (c) TFP, and (d) GTFP as a function of V_{gt} for different fin aspect ratio configurations [28].

parameters improve considerably with the increase in the fin AR, resulting in superior device performance for the C3 configuration. Table 2.4 showcases the summary of different static (at the centre of channel region), analog, and RF parameters of each simulated configuration.

Table 2.4: Summary of different static (at the centre of channel region), analog, and RF parameters of each simulated configuration [22].

Parameter	Unit	C1	C2	C3
Electric Field	(V/cm)	0.89×10^5	1.01×10^5	1.12×10^5
Potential	(V)	0.78	0.80	0.82
Electron Conc.	($/cm^3$)	6.35×10^{18}	11.77×10^{18}	16.72×10^{18}
I_{on}/I_{off} Ratio	-	15.15×10^3	95.14×10^3	296.72×10^3
g_m	(µS)	77.35	83.29	87.42
QF	(µS-dec/mV)	0.95	1.13	1.26
TGF	(V^{-1})	23.08	32.39	39.20
g_d	(µS)	3.31	2.24	1.64
V_{EA}	(V)	11.13	16.74	23.15
A_v	-	15.91	24.98	35.28
f_T	(THz)	3.96	4.01	4.02
f_{max}	(GHz)	13.93	17.97	18.68
GFP	(THz)	55.95	87.36	121.56
TFP	(THz/V)	30.24	34.76	37.14
GTFP	(THz/V)	261.69	452.69	668.16

2.6 SUMMARY

This chapter explores the potential of JAM-GS-GAA FinFET regarding analog and RF parameters and optimizes the fin aspect ratio at the sub-nano level using extensive 3D simulations. The investigation found that the switching ratio increased almost thirty-one

times, and the leakage current was reduced by 96.59% for the JAM GS-GAA FinFET device compared to conventional FinFET. The JAM GS-GAA FinFET structure significantly improved the analog parameters, with A_v, V_{EA}, and TGF increasing by 183.36%, 160.30%, and 88.18%, respectively, compared to conventional FinFET. The RF parameters like GTFP and GFP get enhanced by 3.37 and 2.73 times, with a 21.46% enhancement in TFP for JAM-GS-GAA FinFET configuration compared to conventional FinFET. Furthermore, it is also analyzed that the C3 configuration exhibits the most improved static, analog, and RF performance compared to the two other configurations. The I_{on}/I_{off} ratio increased by 19.58 times for the C3 configuration compared to the C1 configuration, with I_{off} and SS reduced by 94.72% and 14.90%, respectively. Therefore, a high fin aspect ratio enhances the device performance and suppresses the SCEs. Compared with the C1 configuration, a 13.02%, 32.63%, and 69.84% increase in g_m, QF, and TGF is observed, while R_{out}, A_v, and V_{EA} are enhanced by more than two times in magnitude for the C3 configuration. Also, in contrast to the C1 configuration, the C3 configuration demonstrates considerable improvements in f_{max} and TFP, with increases of 34.10% and 22.82%, respectively. Additionally, the C3 configuration exhibits a more than twofold enhancement in GFP and GTFP compared to the C1 configuration. Thus, the proposed JAM-GS-GAA FinFET device with a high fin aspect ratio can be considered an attractive solution for designing analog and RF circuits.

Following a comprehensive analysis of the analog and RF characteristics of the JAM-GS-GAA FinFET, it is imperative to address the reliability concerns associated with this proposed device. Therefore, to ensure the device's reliability, it is crucial to explore its characteristics, taking into account the variations in temperature and gate electrode work function, which will be the primary focus area of the next chapter.

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3

CHAPTER

Reliability Issues of JAM-GS-GAA FinFET: Impact of Temperature and Gate Electrode Work Function

- *This chapter discusses the reliability issues of JAM-GS-GAA FinFET by considering the impact of temperature and gate electrode work function on the proposed device's static, analog, RF, and wireless performance.*
- *The study's findings indicate that the static parameters do not change much as the temperature increases from 300 K to 500 K. Analog and RF performance metrics exhibit changes to the temperature rise, whereas the influence of temperature on wireless performance is less prominent, as measured by linearity and harmonic distortion metrics.*
- *The peak values of various parameters like g_m, f_T, TFP, g_{m2}, g_{m3}, VIP2, VIP3, HD2, and HD3 are approximately the same for all gate electrode work functions. The peak value moves towards a higher gate-source voltage with a higher gate electrode work function.*
- *It can be concluded that the JAM-GS-GAA FinFET exhibits acceptable reliability when subjected to variations in temperature and gate electrode work function.*
- *Consequently, JAM-GS-GAA FinFET offers significant promise as a viable alternative for analog/RF applications demanding low power consumption and strong linearity.*

3.1 INTRODUCTION

Chapter 2 showcased the effectiveness of picking the proposed JAM-GS-GAA FinFET device by comparing its analog and RF properties with conventional FinFET and GAA FinFET. It was also demonstrated that the JAM-GS-GAA FinFET device with a high fin aspect ratio exhibits improved analog and RF performance compared to those with a lower fin aspect ratio. However, addressing the proposed device's reliability issues is crucial to guarantee its dependability. The demand for portable and high-battery backup electronic devices has recently increased because these gadgets enhance the user experience, encourage the adoption of new technologies, and satisfy the rising needs of a mobile and connected society. Thus, to maintain the increased demand, there is a need to increase the transistor density in the integrated circuit (IC) [1]. The heat dissipated in the IC increases considerably with the increase in the transistor density, thereby increasing the operating temperature [2, 3]. When the device dimension reaches below 20 nm, the high temperature can significantly affect the device's operation or even damage it. The high-temperature reliability of a device ensures its long-term durability and stability [4, 5]. Therefore, it is vital to examine the impact of temperature variation on the device's static, analog, RF, and wireless performance for better reliability. The effect of temperature on the digital and analog performance of SOI FinFETs has been investigated extensively [6, 7]. In another simulation study, Das et al. reported that at low temperatures, gate-source overlapped FinFET provides enhanced drain current characteristics [8]. Saha et al. reported the effect of temperature on analog/RF and linearity figure of merits (FOMs) in Fe-FinFET [9].

In addition, the device performance depends significantly on the gate electrode work function in the sub-10 nm regime CMOS technology. The alteration in the work

function impacts the channel region electric field at zero gate-source voltage, which affects the various device performance parameters [10]. Nowadays, the utilization of metal gates is not new because metal gates do not exhibit the poly-depletion effect. The polysilicon gates lead to unwanted fluctuations in the threshold voltage of MOSFET devices [11]. In addition, polysilicon gates become chemically unstable when placed in contact with high-k dielectrics [12]. As a result, finding the proper gate metal for enhanced device performance and better reliability becomes vital. Few papers are present on the consequences of the device's gate work function on its performance. Mohapatra et al. provide a detailed analysis of the consequences of gate work function on the GS-DG MOSFET performance [13]. RF and DC performance in multifin-FinFET for different gate work function variations is testified by Hirpara et al. [14]. Recently, Kumar et al. reported the gate work function impact on the performance analysis of DG-JL-FET [15].

According to the best of the author's knowledge, no report has been published on the impact of the temperature and gate electrode work function on the static, analog, RF, and wireless performance of JAM-GS-GAA FinFET. Thus, this chapter aims to investigate the impact of temperature and gate electrode work function on various static, analog, RF, linearity, and harmonic distortion characteristics of the proposed device to establish its reliability. This chapter is organized as follows: Section 2 offers information on the device's structure and the physical models employed. The experimental calibration between the simulation data and experimental data is discussed in Section 3. Section 4 compares the proposed JAM-GS-GAA FinFET with other existing devices and examines the effect of the temperature and gate electrode work function on the proposed device's different parameters. Section 5 provides a complete summary of the chapter.

3.2 DEVICE DESIGN AND PHYSICAL MODELS

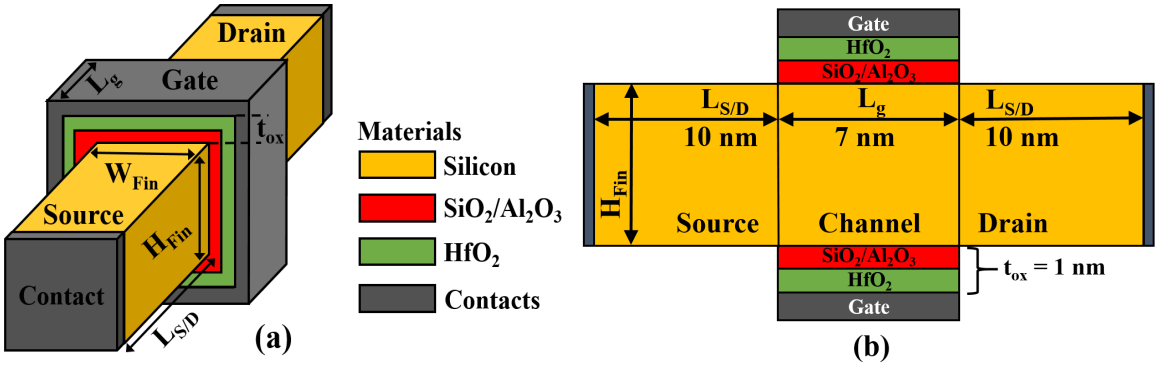

Figure 3.1: Proposed (a) 3D and (b) 2D horizontally cut structures of JAM-GS-GAA FinFET [5, 10].

Figures 3.1(a) and **Figure 3.1(b)** display the proposed 3D and 2D horizontally cut structures of JAM-GS-GAA FinFET, respectively. The fin region consists of silicon material, and gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) are altered from 0 V to 1.5 V and 0 V to 0.5 V, respectively. The source/drain length ($L_{S/D}$) and gate length (L_g) of JAM-GS-GAA FinFET are 10 and 7 nm, respectively. Throughout the simulation, the fin width (W_{Fin} = 5 nm) is fixed in multiples of the fin height (H_{Fin} = 10 nm) to obey the width quantization property [16]. All three regions are n-type uniformly doped with lower doping in the channel area ($N_{Ch} = 1 \times 10^{16}$ cm^{-3}) compared to the source/drain area ($N_{S/D} = 5 \times 10^{18}$ cm^{-3}) to lessen the parasitic capacitance and improve the device performance [17]. The total gate oxide thickness (t_{ox}) is 1 nm. In the temperature variation study, the gate oxide is stacked using a combination of SiO_2 (k = 3.9) and HfO_2 (k = 25), whereas Al_2O_3 (k = 9) is used instead of SiO_2 in the gate electrode work function variation study. In the temperature variation study, the TiN metal gate with work function (ϕ_m) 4.65 eV is considered due to its thermal stability, high purity, low resistivity, and compatibility with CMOS processing [18, 19]. Temperature (T) is kept at 300 K in the gate electrode work function investigation. Temperature varies from 300 K to 500 K in steps of 50 K, and the

gate electrode work function is altered from 4.4 eV to 4.8 eV with a step size of 0.1 eV to analyze the impact of temperature and gate electrode work function on the proposed device's different static, analog, RF, linearity, and harmonic distortion parameters.

The SILVACO Atlas 3D simulator has been used to simulate the proposed JAM-GS-GAA FinFET structure [20]. Poisson's and continuity equations expressed by Equations (3.1-3.3) provide the general framework for device simulation [20].

1. Poisson's Equation

$$\mathrm{div}(\varepsilon\nabla\psi) = -\rho \tag{3.1}$$

where ρ, ψ, and ε represent the space charge density, electrostatic potential, and permittivity. Poisson's Equation relates local space charge density and electrostatic potential.

2. Continuity Equation

For electrons,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}(\overrightarrow{J_n}) + G_n - R_n \tag{3.2}$$

For holes,

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\mathrm{div}(\overrightarrow{J_p}) + G_p - R_p \tag{3.3}$$

where n and p represent the electron and hole concentration, respectively, R_p and R_n are the recombination rates for holes and electrons, and G_n and G_p represent the generation rates for electrons and holes. The magnitude of an electron charge is denoted by q, whereas J_n and J_p represent the electron and hole current densities. The way electron and hole densities evolve because of transport, recombination, and generation is described by continuity and transport equations.

But, to obtain more realistic and accurate results, secondary equations and physical models are needed. Thus, various physical models are incorporated during the simulations. The Bohm Quantum Potential (BQP) model is important, as quantum confinement effects cannot be neglected in aggressively scaled devices. BQP model with alpha = 0.3 and gamma = 1.4 (default parameter values for silicon) is employed in the device simulation to consider the quantum confinement effects in the channel region. The Arora analytical model is used as the temperature has been varied from 300 K - 500 K to correlate the low-field carrier mobility with temperature and impurity concentration. The SRH recombination model is used to include the recombination and generation effects with a fixed carrier lifetime of 1×10^{-7} s, and to consider the specific properties of highly doped materials, Fermi-Dirac statistics are implemented [20]. The Klaassen band-to-band tunneling model is invoked to consider the tunneling of electrons (direct and indirect transitions) between the valence and conduction bands. Concentration-dependent mobility associates low-field carrier mobility with impurity concentration. The impact ionization effects are introduced with the help of the Crowell-Sze impact ionization model. The bandgap separation decreases when the doping is higher than 10^{18} cm^{-3}. The conduction band is lowered almost as much as the valence band is raised. Thus, the bandgap narrowing model is introduced to implement the bandgap narrowing effects. Furthermore, all the mathematical carrier transport equations are performed using the Newton and Block iteration methods [20].

3.3 EXPERIMENTAL CALIBRATION

The GAA FinFET is calibrated using experimental data from Lee et al. [21] to confirm the physical models. The experimental results were calibrated with fixed device dimensions

and assumed silicon material in the fin area to validate the simulations, as specified in the publication. **Figure 3.2(a)** reflects the simulated and experimental I_d - V_{ds} characteristics of a 5 nm GAA FinFET at V_{gs} = 0.2 V, V_{gs} = 0.4 V, and V_{gs} = 0.6 V. The I_d - V_{gs} characteristics for the same device at V_{ds} = 0.2 V and V_{ds} = 1.0 V are shown in **Figure 3.2(b)**. Also, as the results focus on temperature dependence, **Figure 3.2(c)** displays the experimental and simulated I_d - V_{gs} characteristics at two different temperatures [22]. It is visible that the results are well-calibrated, thus validating the choice of simulation models used in the device simulation. The fabrication feasibility of the proposed JAM-GS-GAA FinFET device has already been discussed in **Chapter 2**.

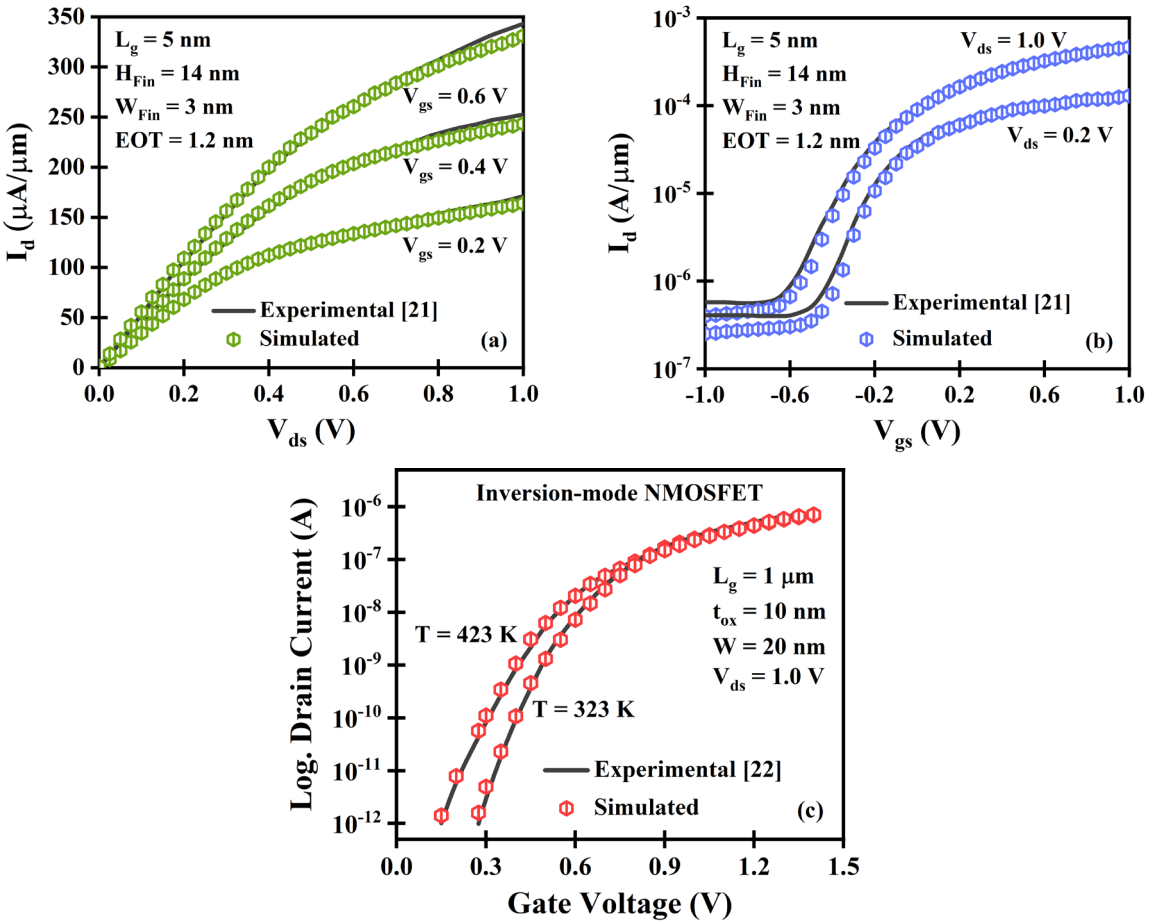

Figure 3.2: Calibrated (a) I_d - V_{ds}, (b) I_d - V_{gs} characteristics of 5 nm GAA FinFET [10, 21], and (c) I_d - V_{gs} characteristics at two different temperatures of inversion-mode NMOSFET [5, 22].

3.4 RESULTS AND DISCUSSION

In this section, the performance of the JAM-GS-GAA FinFET is compared with other existing devices on different technologies to evaluate its significance. Several aspects influence the performance of a FinFET. Hence, the reliability is examined by analyzing the impact of temperature and gate electrode work function on the static, analog, RF, and wireless performance of the JAM-GS-GAA FinFET.

3.4.1 Performance Comparison with Other Existing Devices

Table 3.1 thoroughly compares the various characteristics of JAM-GS-GAA FinFET with different published works at a fixed gate length of 10 nm for a fair comparison. The devices considered for comparison are junctionless double gate vertical MOSFET (JLDGVM) [23], nano-sheet transistor (NST) [24], junctionless SOI nanowire FET (JL-SOI-NW FET) [25], and tunnel field effect transistor (TFET) [26]. It has been observed that the performance of a JAM-GS-GAA FinFET is better than that of any other state-of-the-art device considered, thereby validating our proposed device structure.

Table 3.1: Comparison of JAM-GS-GAA FinFET with existing devices at fixed L_g = 10 nm [10].

Ref.	Platform Device	Parameters								
		I_{off} (A)	I_{on}/I_{off} ratio ($\times 10^5$)	TGF (V^{-1})	A_v	V_{EA} (V)	C_{gs} (fF)	C_{gd} (fF)	f_T (THz)	GBP (THz)
[23]	JLDGVM	NA	NA	26.7	NA	0.59	5.36	1.01	0.083	0.376
[24]	NST	7.62×10^{-10}	1.90	NA	6.03	2.67	0.07	0.07	0.585	NA
[25]	JL-SOI-NW FET	7.10×10^{-10}	0.82	41.81	NA	NA	0.04	0.04	0.254	0.05
[26]	TFET	1.51×10^{-13}	NA	4.39	0.93	NA	0.258	0.422	0.940	0.973
This Work	JAM-GS-GAA FinFET	3.73×10^{-13}	455.28	40.09	58.17	19.57	0.002	0.004	2.845	0.774

*NA – data not available.

3.4.2 Impact of Temperature on Static and Analog Performance

The change in the electric field along the channel with temperature is depicted in **Figure 3.3(a)**. Temperature rise from 300 K to 500 K leads to higher carrier concentration, which raises the electric field. Also, the drain end has a smaller electric field than the source end, indicating the corner effect's reduction. **Figure 3.3(b)** shows the change in surface potential (ϕ_f) with the temperature, and it is directly related to temperature by Equation (3.4) [4]:

$$\phi_f = (kT/q) \times \ln(n/n_i) \tag{3.4}$$

where n_i signifies the intrinsic carrier concentration, q denotes the elementary charge, and T and k represent temperature and Boltzmann's constant, respectively. The n_i depends on

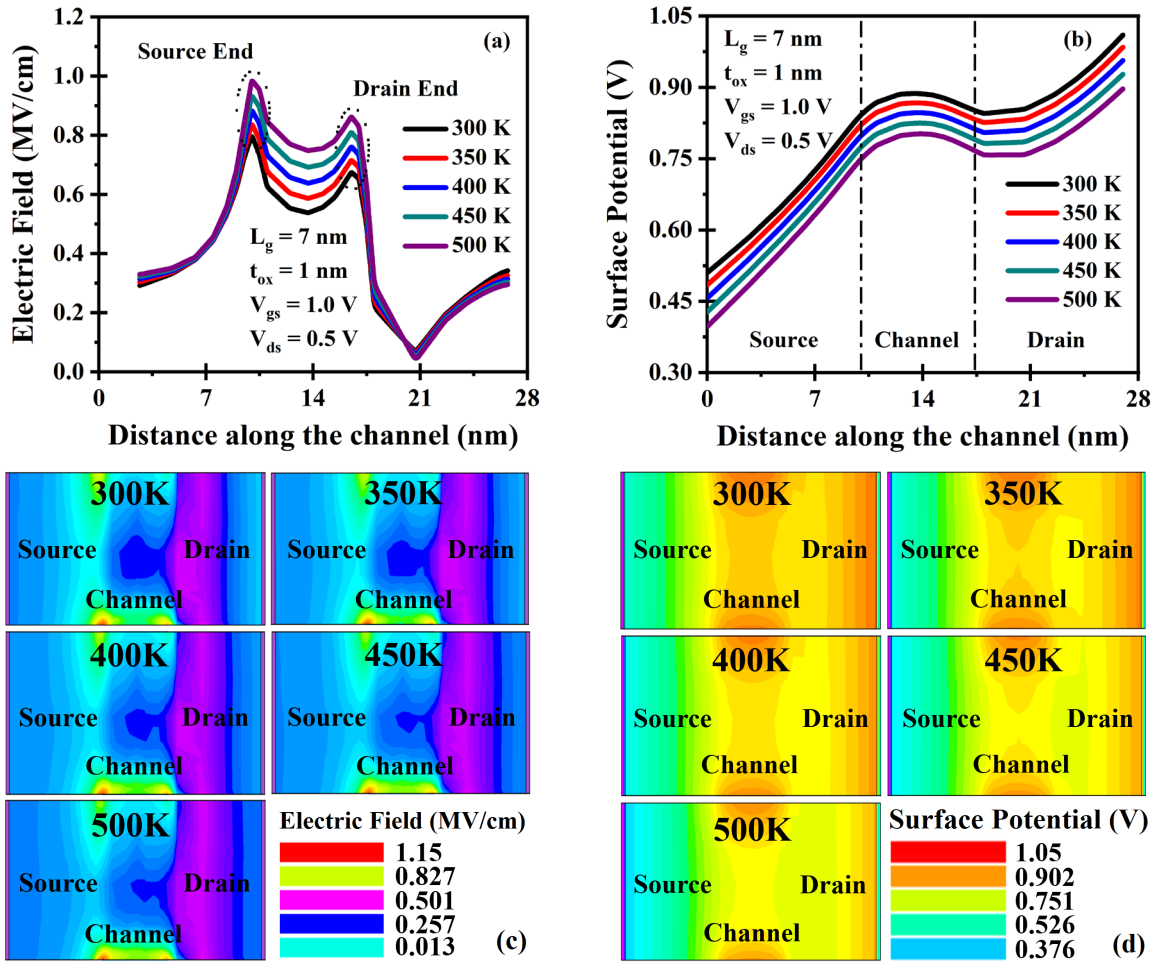

Figure 3.3: Impact of temperature variation on (a) electric field and (b) surface potential [5]. Contour profile of (c) electric field and (d) surface potential at different temperatures [5].

the temperature as $n_i \propto \exp(-E_g/2kT)$. The increase in temperature increases the intrinsic carrier concentration, resulting in a decreased $\ln(n/n_i)$ term in Equation (3.4). Thus, the surface potential decreases with the rise in temperature. **Figure 3.3(c)** and **Figure 3.3(d)** depict the corresponding contour profile of the electric field and surface potential with the temperatures, respectively.

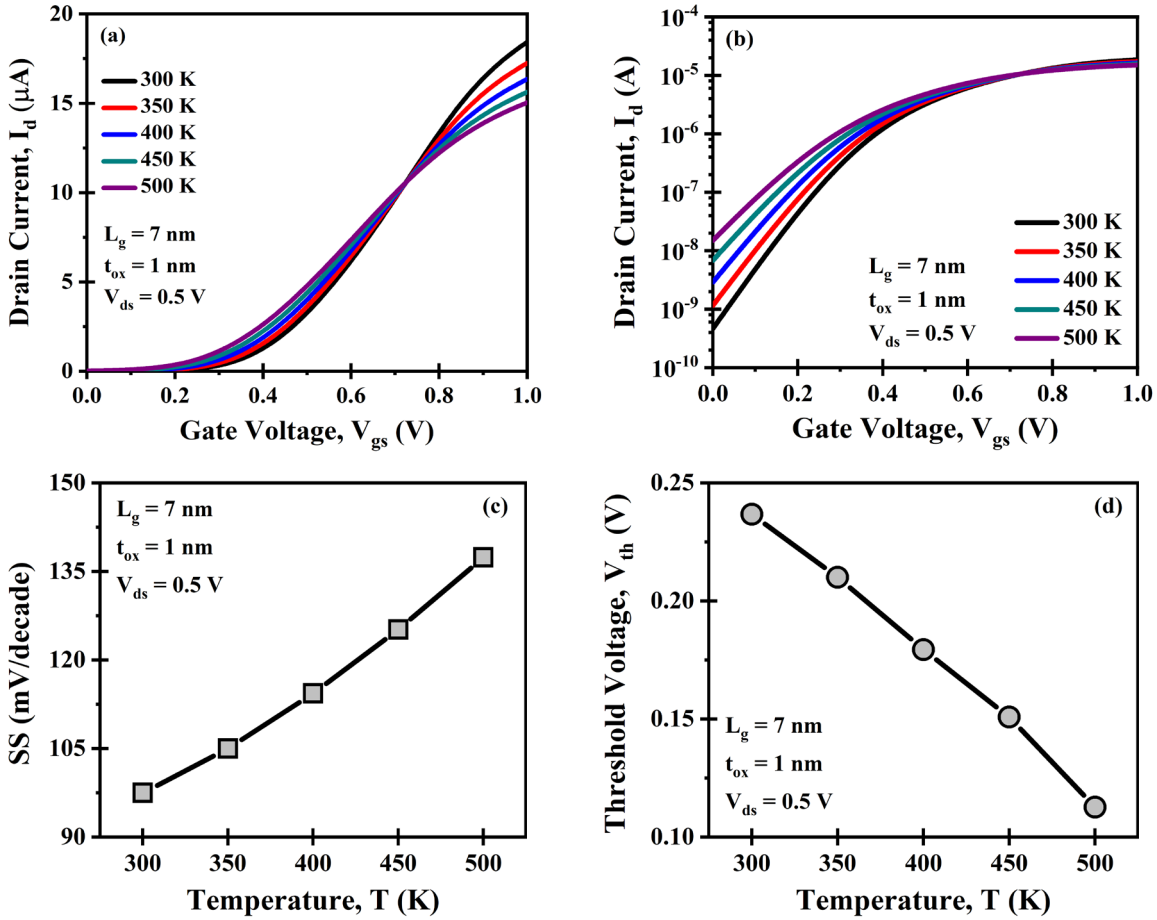

Figure 3.4: Influence of considered temperatures on (a) I_{on} current, (b) I_{off} current, (c) SS, and (d) V_{th} [5].

Figure 3.4(a) and **Figure 3.4(b)** display the device's transfer characteristics in linear and log scales for different temperatures. The opposite effect of temperature on drain current (I_d) is observed at high and low V_{gs}. At low V_{gs}, the energy band gap decreases as the temperature increases, enhancing the device's leakage current (I_{off}). At high V_{gs}, with

the temperature rise, the decrease in mobility due to scattering of the carrier dominates over the energy bandgap decrease, resulting in a degradation of the on-current (I_{on}) of the device [9]. Thus, an increase in the temperature results in the degradation of both I_{on} and I_{off}. The variation of subthreshold swing (SS) with temperature is portrayed in **Figure 3.4(c)**. The SS as a function of temperature (Kelvin) is given as SS = (60*T)/300 [27]. Thus, with the rise in temperature, SS increases, resulting in device performance degradation. **Figure 3.4(d)** plots the threshold voltage (V_{th}) against the temperature. The increase in the temperature from 300 K to 500 K leads to a decrease in V_{th}.

Figure 3.5(a) outlines the plot of peak transconductance (g_m) against different temperatures. The peak value of g_m is obtained at V_{gs} = 0.75 V for all the considered

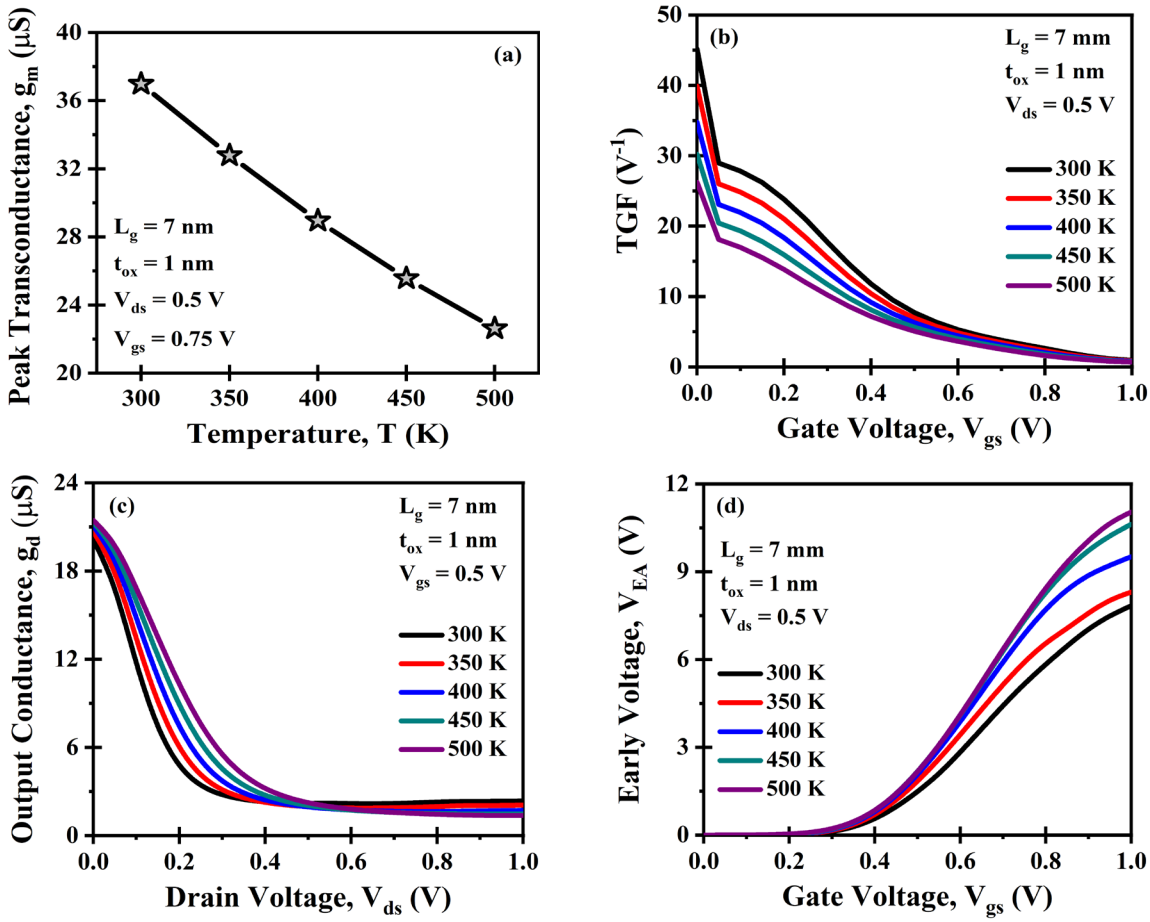

Figure 3.5: Consequences of the temperature on (a) g_m, (b) TGF, (c) g_d, and (d) V_{EA} [5].

temperatures, which decreases with increased temperature due to reduced mobility. The variation of transconductance generation factor (TGF) with temperature is shown in **Figure 3.5(b)**. In the subthreshold region, a higher value of TGF is attained for all the temperatures, demonstrating the suitability of JAM-GS-GAA FinFET for ultra-low-power applications. At low V_{gs}, an increase in the temperature results in a decrease in TGF. However, the temperature impact on TGF decreases with an increase in V_{gs} and eventually becomes negligible at high V_{gs}. **Figure 3.5(c)** represents the variation of output conductance (g_d) as a function of V_{ds} and temperature. At low V_{ds}, g_d increases with an increase in temperature and decreases at high V_{ds}. The effect of temperature on the early voltage (V_{EA}) as a function of V_{gs} is reflected in **Figure 3.5(d)**. In the subthreshold region, the temperature impact on the V_{EA} is almost negligible. However, V_{EA} increases with the temperature at a high V_{gs} since the reduction in g_d is higher than the I_d reduction. Thus, the static and analog parameters of JAM-GS-GAA FinFET show reliable performance in temperature variations.

3.4.3 Impact of Temperature on RF and Wireless Performance

Figure 3.6(a) shows the cut-off frequency (f_T) peak value plot with the temperature at V_{gs} = 0.65 V. The reduction in the peak value of f_T is observed as the temperature is raised from 300 K to 500 K. The main reason for this behavior is the dependence of f_T on g_m and gate capacitance (C_{gg}). The f_T decreases because of an increment in C_{gg} and a reduction in g_m with temperature. The gain frequency product (GFP) is an essential parameter in high-frequency applications. **Figure 3.6(b)** depicts the peak value of GFP for temperatures ranging from 300 K to 500 K at V_{gs} = 0.65 V. The peak value of GFP decreases with the rise in temperature due to the reduction in g_m and f_T. Transconductance frequency product (TFP) is mainly utilized in high-speed designs, exhibiting an agreement between bandwidth

and power. **Figure 3.6(c)** outlines the change in TFP with the temperature. TFP decreases for higher temperatures due to reduced g_m and f_T with a temperature rise. Due to higher mobility degradation, the TFP shifts towards lower V_{gs} as the temperature rises from 300 K to 500 K. The gain transconductance frequency product (GTFP) evaluates the complete device performance. GTFP exhibits an agreement between f_T, TGF, and A_V. **Figure 3.6(d)** displays the temperature impact on GTFP, and the peak value of GTFP reduces due to reduced g_m and f_T as the temperature increases from 300 K to 500 K.

$$g_{mn} = (1/n!) \times (\partial^n I_{DS}/\partial V_{GS}^n) \qquad \text{where } n = 1,2,3, \text{and so on} \tag{3.5}$$

$$VIP2 = 4 \times (g_m/g_{m2}) \tag{3.6}$$

$$VIP3 = \sqrt{24 \times (g_m/g_{m3})} \tag{3.7}$$

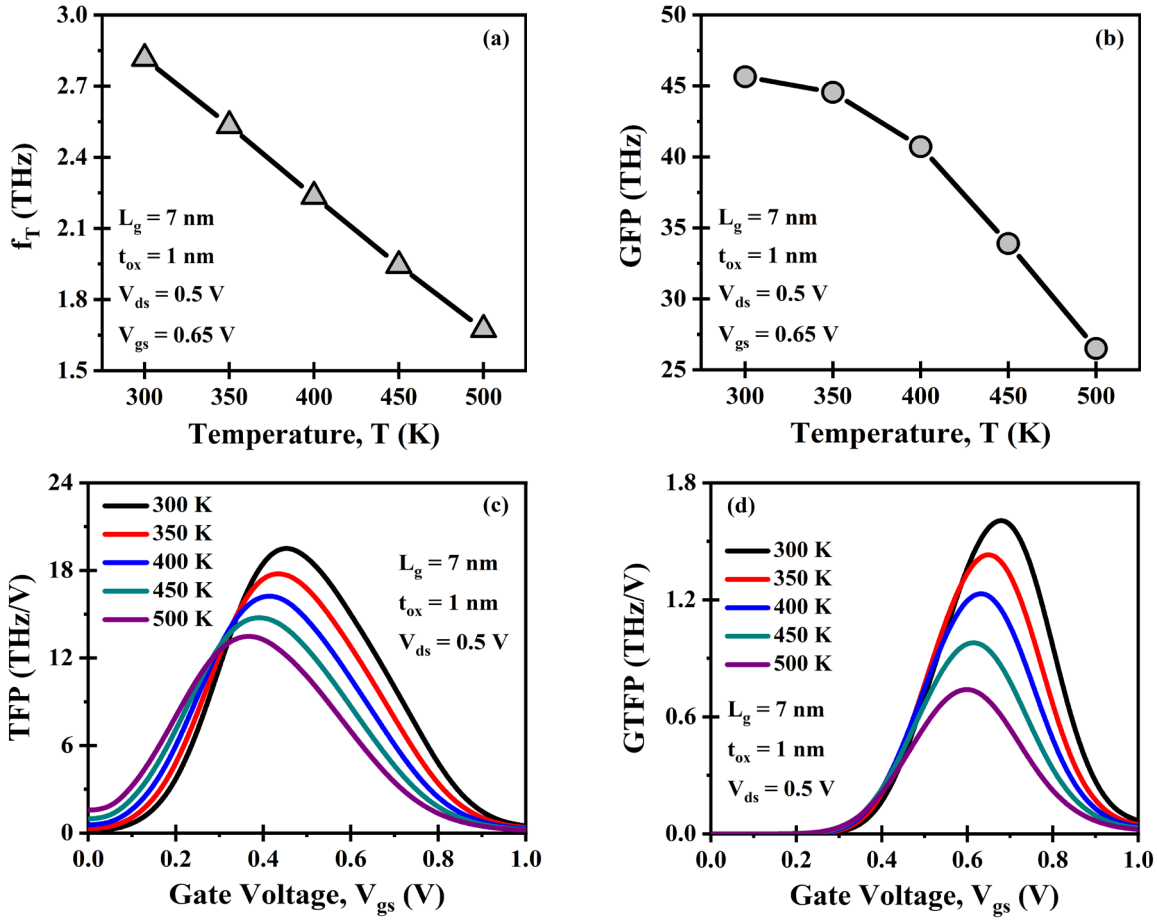

Figure 3.6: Alteration of (a) f_T, (b) GFP, (c) TFP, and (d) GTFP for the different temperatures [5].

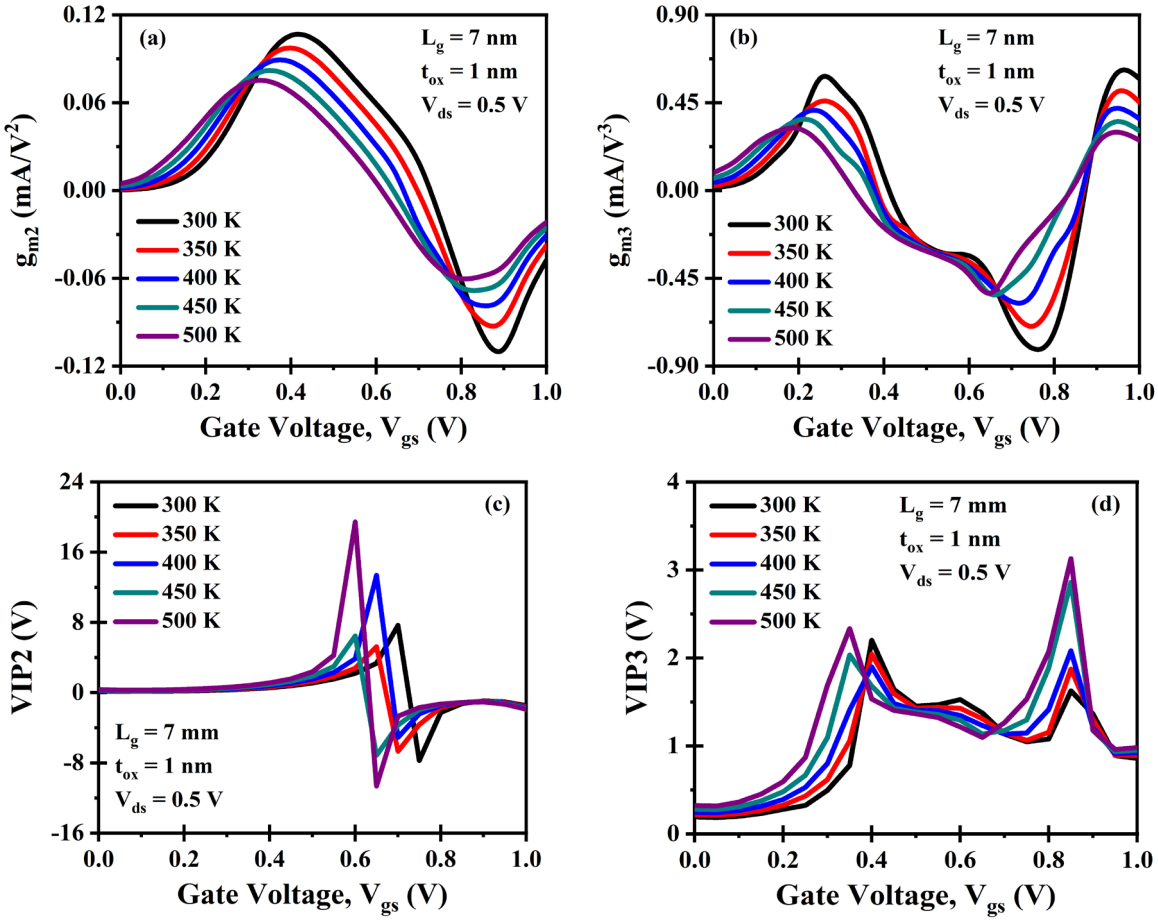

Figure 3.7: Plot of (a) g_{m2}, (b) g_{m3}, (c) VIP2, and (d) VIP3 concerning the different temperatures [5].

In wireless communication systems, transistors with low distortion parameters are desirable. Linearity is an essential parameter that ensures the least intermodulation and harmonic distortion at the output [28]. The higher-order coefficients of transconductance, i.e., g_{m2} and g_{m3}, provide an estimate of the non-linearity of a transistor. Equation (3.5) evaluates these parameters and should be low for better linearity [29]. **Figure 3.7(a)** and **Figure 3.7(b)** portray the impact of temperature variation on g_{m2} and g_{m3} as a function of V_{gs}, respectively. The peak value of g_{m2} and g_{m3} decreases with the rise in temperature due to the deterioration of short channel characteristics, indicating the device's improved linearity characteristics. The primary reason for the negative value of g_{m2} is the reduction in g_m at a high V_{gs}. The extrapolated gate voltage at which fundamental tone amplitude and

second-order harmonic amplitude are equal is VIP2. Similarly, VIP3 is the extrapolated gate voltage at which the fundamental tone amplitude equals the third-order harmonic amplitude. The high peak values of VIP2 and VIP3, as expressed in Equations (3.6) and (3.7), respectively, indicate better linearity characteristics of the device [28]. **Figure 3.7(c)** and **Figure 3.7(d)** display a plot of VIP2 and VIP3 as a function of V_{gs} for all the temperatures considered, respectively. The peak value of both VIP2 and VIP3 rises with the rise in temperature. The reason for this increase is the reduction in g_{m2} and g_{m3} with the temperature. The 1-dB compression point, as expressed in Equation (3.8), refers to the input power level at which the output power of the device decreases by 1 dB from its small-signal linear gain [28]. For highly linear applications and to attain maximum gain, a 1-dB compression point should have a high value. **Figure 3.8(a)** reflects the 1-dB compression point plot against V_{gs} and temperature. The rise in 1-dB compression point values due to reduced g_{m3} peak values with the temperature indicates superior linearity performance.

$$1-\text{dB compression point} = 0.22 \times \sqrt{(g_m/g_{m3})} \tag{3.8}$$

$$\text{IMD3} = \left((9/2) \times (\text{VIP3})^2 \times g_{m3}\right)^2 \times R_s \tag{3.9}$$

$$\text{HD2} = (0.5 \times V_a \times (dg_m/dV_{gs}))/2 \times g_m \tag{3.10}$$

$$\text{HD3} = (0.25 \times V_a^2 \times (d^2g_m/dV_{gs}^2))/6 \times g_m \tag{3.11}$$

The rise in distortion due to the non-linear device performance in analog/RF applications is a significant concern. Distortion vitiates the strength of the signal by generating unwanted components whose frequency doesn't match the proper band of frequencies [30]. Thus, distortion at the output of a linear amplifier should be as minor as possible. The Integral Function Method (IFM) approach has been used instead of Fourier-based methods to extract distortion parameters as they acknowledge DC measurements

instead of AC characterization [31, 32]. Equations (3.9-3.11) provide mathematical relations of distortion parameters like third-order intermodulation distortion (IMD3) and second (HD2) and third-order harmonics (HD3) [31-33]. In these equations, source resistance (R_s) is taken as 50 Ω, and the amplitude of the AC signal (V_a) is assumed to be 50 mV [34, 35]. IMD3, HD2, and HD3 values should be as low as possible for lesser distortion in device operation and improved linear characteristics. IMD3 symbolizes the extrapolated intermodulation distortion power at which the first and third-order intermodulation power is equal [29]. **Figure 3.8(b)** outlines the impact of temperature variation on IMD3 as a function of V_{gs}. In the IMD3 - V_{gs} plot, for V_{gs} < 0.5 V, IMD3 increases with the temperature, and for V_{gs} > 0.5 V, IMD3 decreases with the temperature.

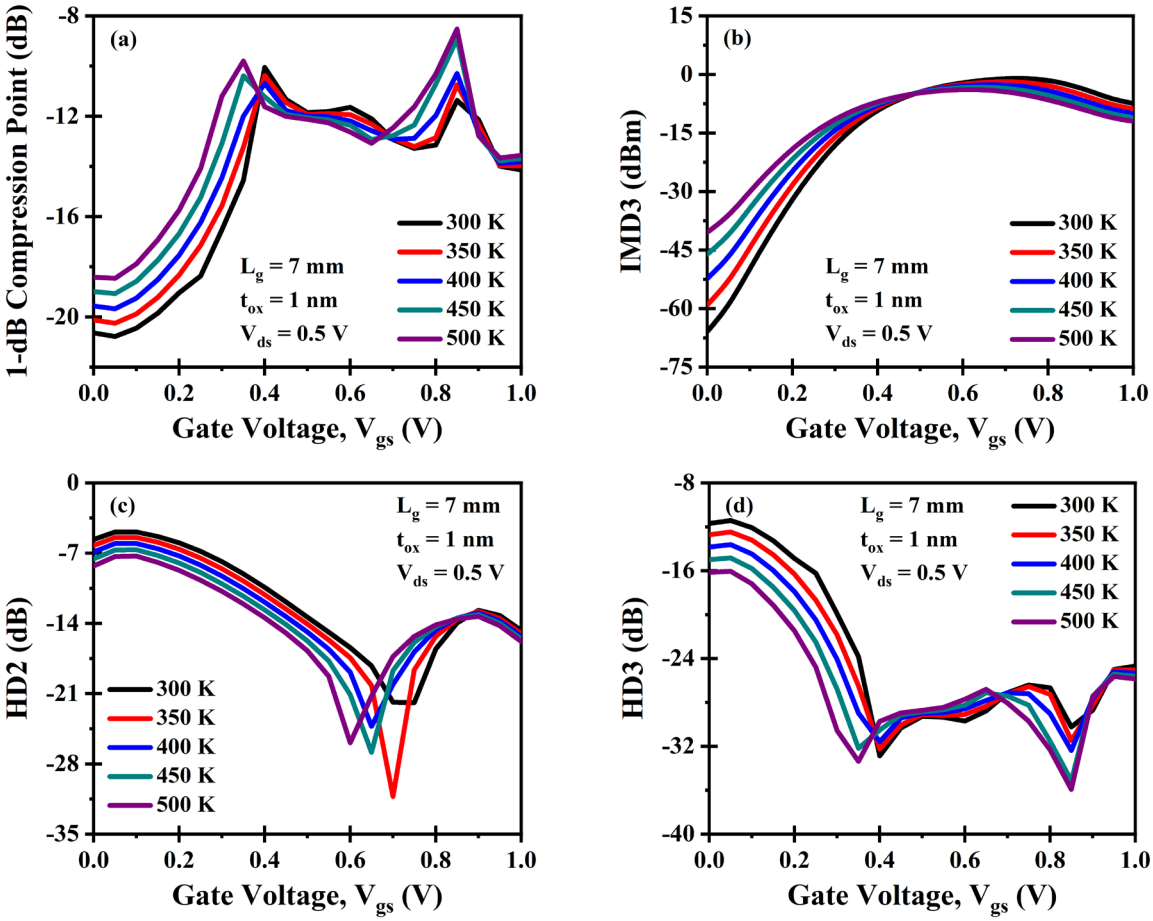

Figure 3.8: Impact of considered temperatures on (a) 1-dB compression point, (b) IMD3, (c) HD2, and (d) HD3 [5].

Figure 3.8(c) and **Figure 3.8(d)** outline the impact of temperature on HD2 and HD3. The value of HD2 and HD3 decreases with the rise in temperature because, at higher temperatures, due to higher intrinsic carrier density, g_m increases more rapidly than the dg_m/dV_{gs} and d^2g_m/dV^2_{gs}, respectively. Therefore, the JAM-GS-GAA FinFET device exhibits acceptable reliability when subjected to variations in temperature.

Table 3.2: Comparison of two oxide layers used for simulation.

Configuration	**I_{on} (µA)**	**I_{off} (nA)**	**I_{on}/I_{off} ratio**	**SS (mV/dec)**	**V_{th} (V)**	**g_m (µS)**	**TGF (V^{-1})**
SiO_2	18.427	0.464	39713.36	97.467	0.236	36.98	45.165
Al_2O_3	20.562	0.248	82911.29	91.563	0.247	42.30	50.323
Improvement (%)	11.59	46.55	108.77	6.06	4.66	14.39	11.42

3.4.4 Impact of Work Function on Static and Analog Performance

A combination of SiO_2 and HfO_2 was employed to stack the gate oxide in the temperature variation investigation. However, Al_2O_3 was used instead of SiO_2 in the gate electrode work function variation study due to the benefits of a gate oxide layer with a higher dielectric constant. Table 3.2 displays the values of a few parameters acquired using two oxide layers, and the enhancement in device performance resulting from the replacement is evident, with the I_{on}/I_{off} ratio and I_{off} current showing the greatest improvement. The electric field plot and contour profiles along the channel for each gate electrode work function are shown in **Figure 3.9(a)** and **Figure 3.9(b)**, respectively. The electric field is much more significant for the 4.4 eV than the 4.8 eV in the channel region because a reduction in work function shifts the Fermi level towards the conduction band, facilitating electron transitions from the valence band to the conduction band. The displacement of the Fermi level increases the number of electrons in the conduction band, resulting in an enhanced electric field inside

the channel. The surface potential of all the devices along the channel with altered gate electrode work functions is displayed in **Figure 3.9(c)**. The surface potential increases with reduced work function in the channel area because decreasing the work function reduces the energy barrier for electron emission, facilitating the release of more electrons from the surface and thereby affecting the charge distribution in the semiconductor. This alteration in the distribution of electric charge contributes to an increase in the surface potential. The electron concentration plot for the different gate electrode work functions is outlined in **Figure 3.9(d)**. In the channel region, the electron concentration rises considerably with the decrement in the work function due to the reduced energy barrier for electron emission.

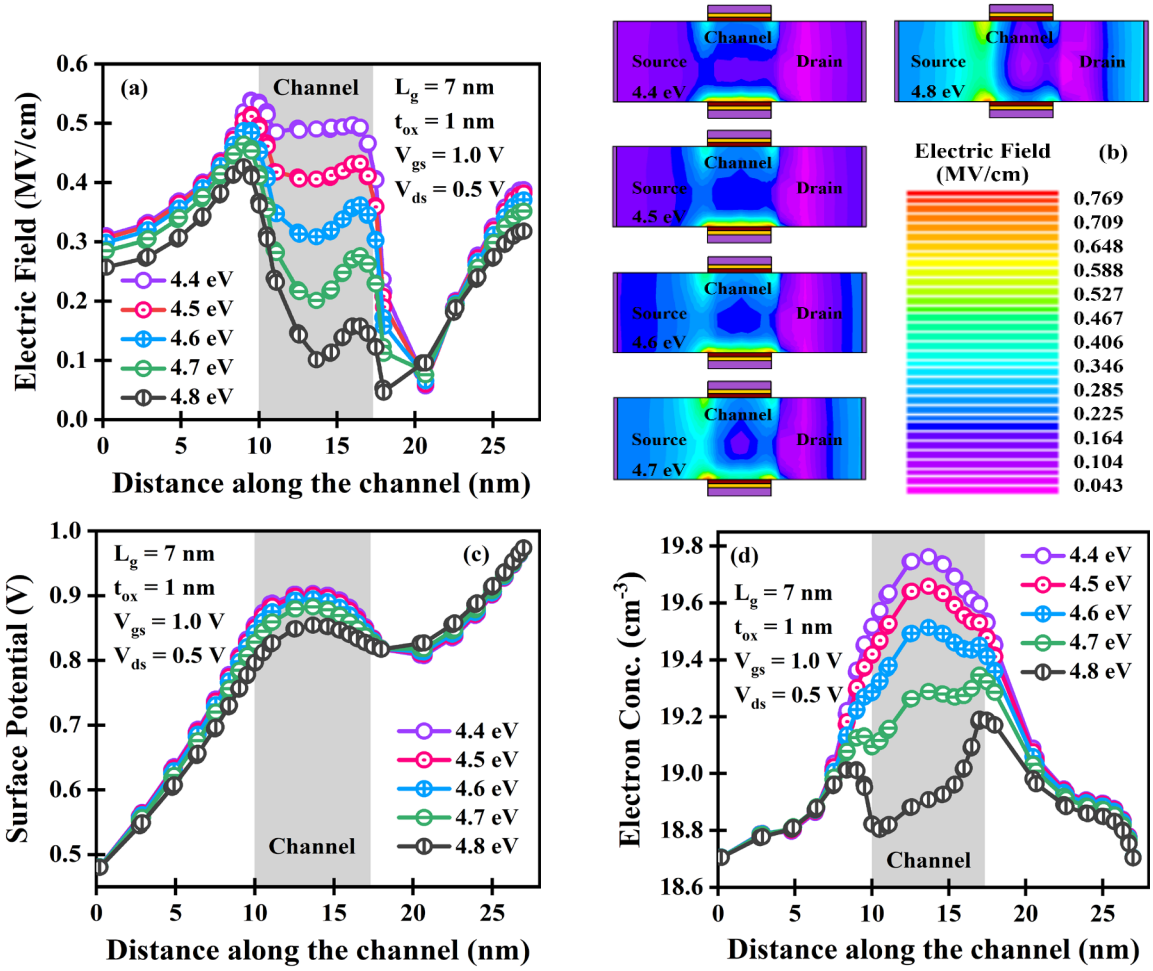

Figure 3.9: (a) Electric field plot, (b) electric field contour profile, (c) surface potential, and (d) electron concentration for altered gate electrode work functions [10].

Figure 3.10(a) depicts the influence of considered gate electrode work functions on the device's I_d at constant V_{ds}. The V_{th} rises with a surge in the work function. Subsequently, a reduction in the I_{on} current is observed with an escalation in the work function. However, a rise in the work function leads to increased bending of energy bands, which improves the device's I_{off} current, as illustrated in **Figure 3.10(b)**. The SS variation against different gate electrode work functions is demonstrated in **Figure 3.10(c)**. A considerable reduction in the SS is observed with an escalation in the work function due to reduced leakage current, indicating an improvement in SCEs. **Figure 3.10(d)** depicts the deviation of V_{th} with the gate electrode work function. The V_{th} increases linearly with the growth in the work function, and the maximum value (0.397 V) is observed for the 4.8 eV.

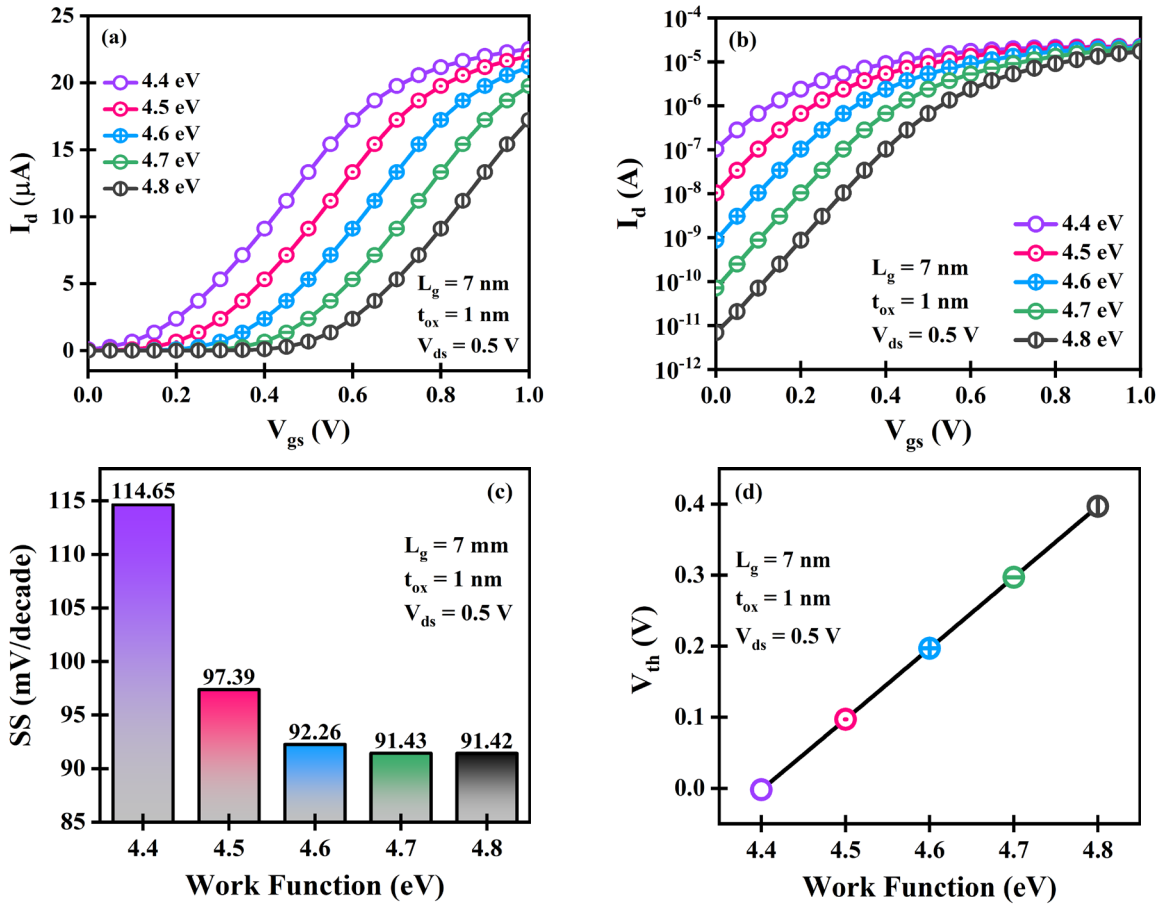

Figure 3.10: Influence of considered gate electrode work functions on (a) I_{on} current, (b) I_{off} current, (c) SS, and (d) V_{th} [10].

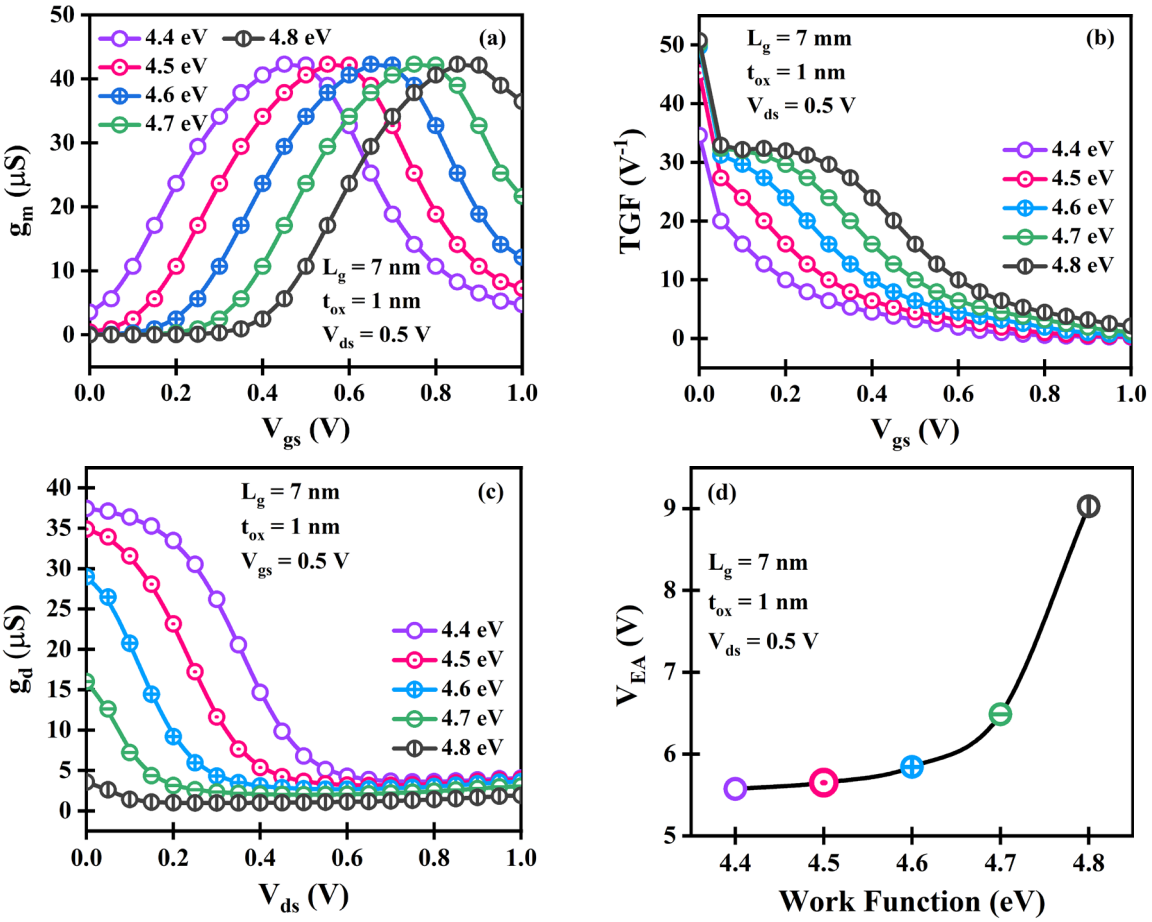

Figure 3.11: Consequences of the considered gate electrode work function on (a) g_m, (b) TGF, (c) g_d, and (d) V_{EA} [10].

The reduction in the drain current leads to a rise in the V_{th} of the device. **Figure 3.11(a)** illustrates the consequences of the gate electrode work function on the transconductance. Due to reduced drain current, g_m reduces with a surge in the work function at an inferior V_{gs}. The maximum value of g_m is approximately the same for all work functions. However, the peak value shifts towards higher V_{gs} with a higher work function. **Figure 3.11(b)** depicts the plot of TGF against the different gate electrode work functions considered. The maximum value of TGF is acquired for the 4.8 eV, whereas the lowest is for the 4.4 eV because of the reduced I_d and identical g_m with the rise in the work function. However, the increase in the peak value decreases with a rise in the work function. **Figure 3.11(c)**

portrays the influence of the gate electrode work function on the device g_d at constant V_{gs}. The g_d value must be low for enhanced analog performance, and the same is observed for the device with a 4.8 eV work function. The V_{EA} variation concerning the different gate electrode work functions is demonstrated in **Figure 3.11(d)**. The V_{EA} peak values increase by 62.12%, with a 0.4 eV increase in the work function. It is mainly because the g_d improves considerably for the higher work function. Thus, the static and analog parameters of JAM-GS-GAA FinFET exhibit significant reliability to the gate electrode work function with superior static performance at 4.4 eV and significantly improved analog performance with the 4.8 eV gate electrode work function.

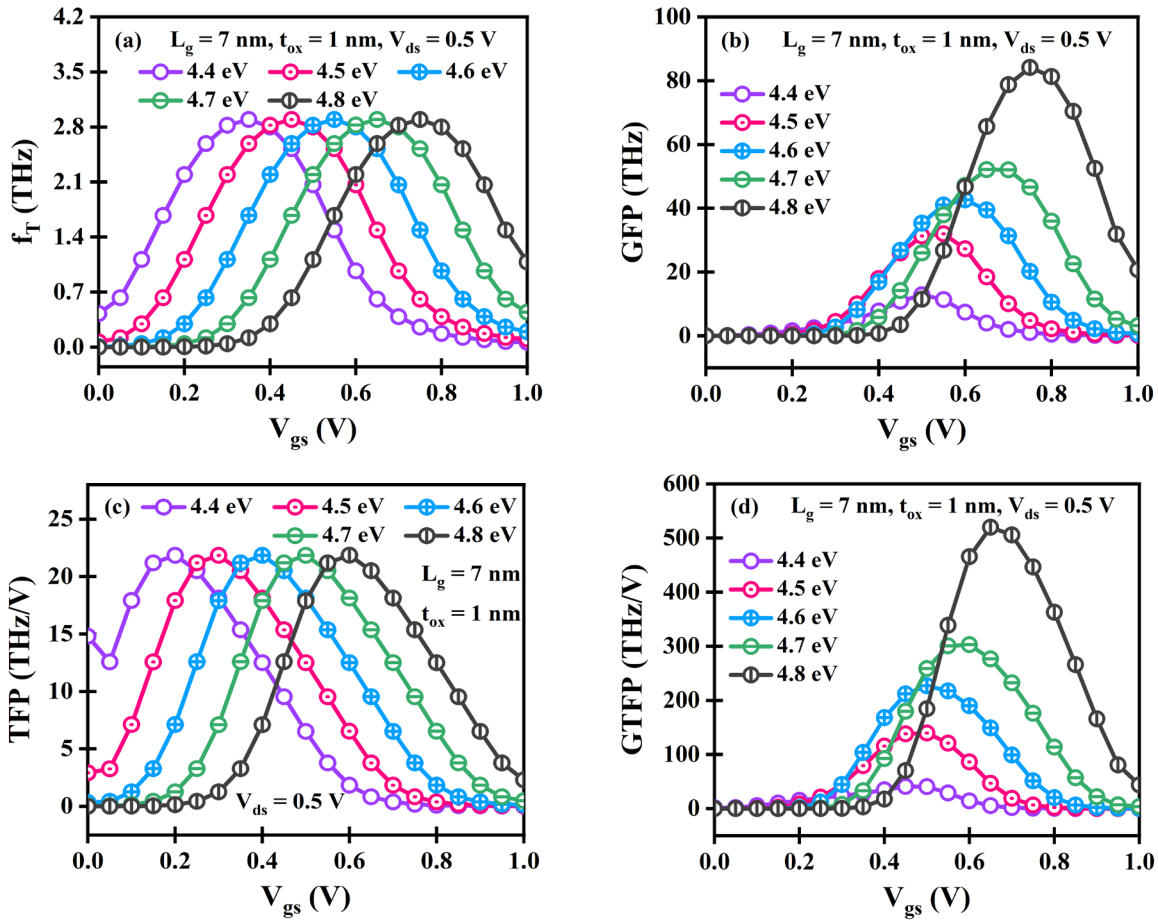

Figure 3.12: Alteration of (a) f_T, (b) GFP, (c) TFP, and (d) GTFP for the different gate electrode work functions [10].

3.4.5 Impact of Work Function on RF and Wireless Performance

Figure 3.12(a) represents the f_T plot against V_{gs} for different gate electrode work functions. Initially, f_T increases with the V_{gs}, reaches a maximum value and then decreases with a further increase in the V_{gs}. The work function escalation shifts the peak value of f_T towards higher V_{gs}. However, the peak value is almost identical in all cases. The work function increase reduces the C_{gg} and g_m. As a result, the peak value remains constant for all the devices with different work functions. **Figure 3.12(b)** depicts the variation of GFP for altered gate electrode work functions against V_{gs}. The maximum value of GFP is obtained for the device with a 4.8 eV work function due to the reduced g_d and identical g_m and f_T.

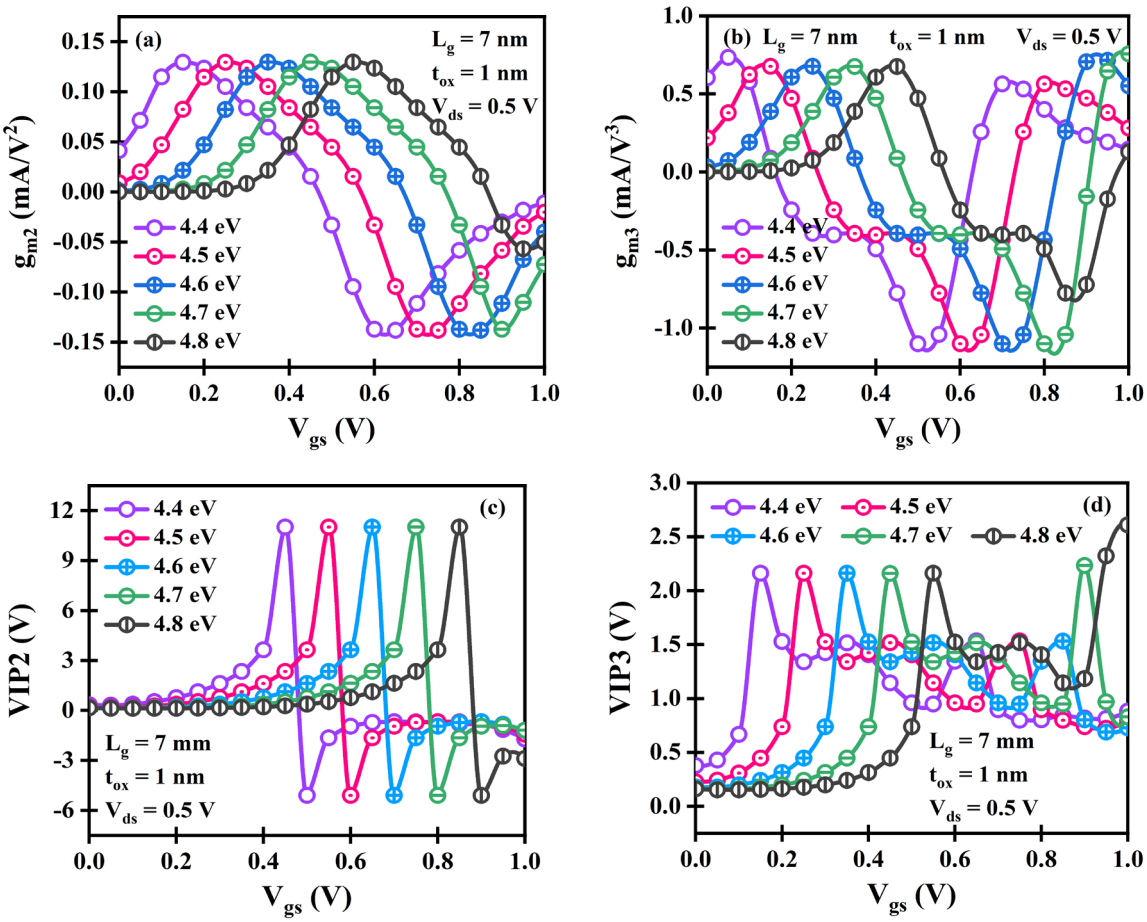

Figure 3.13: Plot of (a) g_{m2}, (b) g_{m3}, (c) VIP2, and (d) VIP3 concerning the different gate electrode work functions.

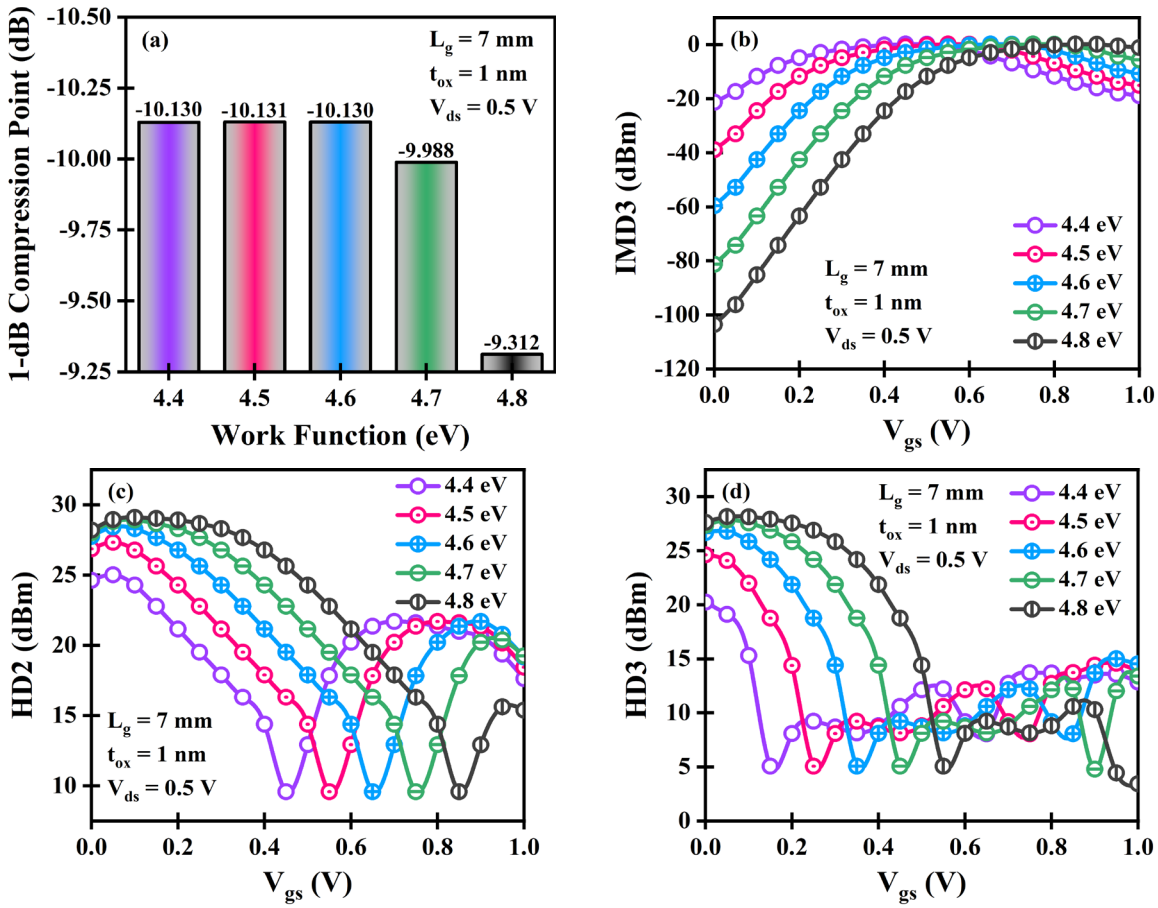

Figure 3.14: Impact of considered gate electrode work functions on (a) 1-dB compression point, (b) IMD3, (c) HD2, and (d) HD3.

The alteration of the TFP and GTFP for the different gate electrode work functions is outlined in **Figure 3.12(c)** and **Figure 3.12(d)**. Since TFP directly depends on the g_m and f_T, the TFP peak value is almost identical for the considered work functions. But GTFP increases when the work function is raised by 0.4 eV, primarily due to the reduced g_d.

Figure 3.13(a) and **Figure 3.13(b)** depict the effect of gate electrode work functions on g_{m2} and g_{m3} against V_{gs}. The maximum value of g_{m2} and g_{m3} is approximately the same for all work functions. However, the peak value of g_{m2} and g_{m3} shifts towards higher V_{gs} with a higher work function. **Figure 3.13(c)** and **Figure 3.13(d)** portray a plot of VIP2 and VIP3 against V_{gs} for considered gate electrode work functions. The highest value of VIP2 and VIP3 is almost identical for all work functions because of the inverse

proportionality relationship with g_{m2} and g_{m3}. 1-dB compression point variation against gate electrode work functions is represented in **Figure 3.14(a)**. The 1-dB compression point increases with an increase in the work function and attains the maximum value for the device with a 4.8 eV work function because of the reduced gate leakage (I_{off}) current. **Figure 3.14(b)** reveals IMD3 variation against V_{gs} for each gate electrode work function considered. In the IMD3 - V_{gs} plot, for lower values of V_{gs}, IMD3 decreases with the increase in the work function, whereas an opposite trend is observed at higher values of V_{gs}. **Figure 3.14(c)** and **Figure 3.14(d)** represent the variation of HD2 and HD3 against V_{gs} for all gate electrode work functions. The lowest value of distortion parameters is almost the same for the considered work functions due to the dependence on the g_m, g_{m2}, and g_{m3}. However, the device with a 4.8 eV work function shows the least distortion for the higher values of V_{gs} compared to other devices. Thus, the JAM-GS-GAA FinFET device reliably operates when exposed to gate electrode work function changes.

3.5 SUMMARY

This chapter inspected the impact of temperature and gate electrode work function on the static, analog, RF, and wireless performance to explore the reliability issues of the JAM-GS-GAA FinFET. The study's findings indicate slight variations in the static parameters, such as the electric field and surface potential, as the temperature increases from 300 K to 500 K. Analog and RF performance parameters like g_m, TGF, f_T, GFP, TFP, and GTFP exhibit changes with the rise in temperature while minor changes were observed in other analog and RF metrics to the temperature rise. The influence of temperature on the wireless performance is less prominent, as measured by linearity and harmonic distortion metrics. Further, results revealed that the peak values of various static, analog, RF, and wireless

performance parameters like g_m, f_T, TFP, g_{m2}, g_{m3}, VIP2, VIP3, HD2, and HD3 are approximately the same for all gate electrode work functions. However, the peak value shifts towards higher V_{gs} with a higher gate electrode work function. In addition, it was seen that the other parameters under discussion exhibit little variations in response to an increase in the gate electrode work function. Therefore, it can be inferred that the proposed JAM-GS-GAA FinFET device demonstrates satisfactory reliability in the face of temperature fluctuations and changes in the gate electrode work function. As a result, it has excellent potential as a viable option for applications requiring analog/RF functionality and low power consumption with good linearity.

Following a thorough reliability examination of the JAM-GS-GAA FinFET device, improving its performance further and making it appropriate for RFIC circuits in the sub-10 nm region is critical. One fascinating development is the dual-k spacer, which integrates a high-k spacer on the inside and a low-k spacer on the outside to improve the device's drain current and subthreshold characteristics. Thus, the next chapter aims to quantitatively describe the impact of dual-k spacers on the JAM-GS-GAA FinFET device and measure the improvements in device performance in the static, analog, and RF domains.

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4

CHAPTER

Dual-k Spacer Engineering on JAM-GS-GAA FinFET for Low-Power RFIC Circuits

- *This chapter investigates the impact of dual-k spacer (SiO_2 + HfO_2) engineering on the RFIC design feasibility of a JAM-GS-GAA FinFET in the sub-10 nm range.*
- *The findings indicate that incorporating a dual-k spacer improves the electron velocity, electric field, surface potential, valence band energy, and conduction band energy due to the fringing field effects.*
- *In comparison to the conventional FinFETs, the I_{on} of the dual-k spacer JAM-GS-GAA FinFET increased by 35.34%, I_{on}/I_{off} ratio by roughly 10^2 times, g_m by 24.03%, TGF by 39.12%, QF by 46.75%, V_{EA}, A_v, GFP, and GTFP by five times, while the I_{off} decreased by almost 76 times, g_d by 21.13%, DIBL by 66.61%, and SS by 15.47%.*
- *The transitioning from a single-k spacer to a dual-k spacer improves I_{off}, V_{EA}, A_v, GTFP, and GFP by 81.78%, 78.17%, 73.98%, 70.28%, and 53.46%, respectively. These findings highlight the advantages associated with the adoption of the more complicated dual-k spacer configuration.*
- *Consequently, JAM-GS-GAA FinFET with dual-k spacer is an encouraging device for low-power RFIC circuits.*

4.1 INTRODUCTION

In **Chapter 3**, the reliability of the JAM-GS-GAA FinFET device was extensively investigated by analyzing the impact of temperature and gate electrode work function on the device's various characteristics. Now, it is essential to further enhance the performance of the JAM-GS-GAA FinFET device and make it suitable for sub-10 nm RFIC circuits. It can be achieved using a spacer configuration that elongates the separation between the drain and source contact terminals [1]. However, the series resistance will rise on extending the distance separating two potential terminals because of a lower on-state current. An underlap high-k spacer is a technical solution to this problem. Underlap high-k spacer engineering is a technique that reduces the influence of drain bias in the channel area, thereby improving device performance and minimizing short-channel effects (SCEs) [2]. Studies have shown that devices using high-k spacers in the underlap area have good control over the channel, improved on-state current, and lower leakage current [3-8]. But this has some serious consequences. The primary challenge of utilizing a solitary high-k spacer is the amplified fringe capacitance constituents [9], thereby delaying the circuit by coupling with the gate. Second, carrier mobility is hampered by induced trapped charges caused by Coulomb scattering at the silicon-dielectric interface [9]. Therefore, spacer analysis should be used strategically. Consequently, reducing the utilization of a high-k spacer within the vicinity where fringing fields could produce elevated carrier densities within a restricted range would be advantageous. One fascinating new development is the dual-k spacer, which integrates a high-k spacer on the inside with a low-k spacer on the exterior to improve the on-state current and subthreshold characteristics and lower the parasitic capacitance of the device [10].

This chapter aims to describe the impact of dual-k spacers on multiple configurations under consideration and to measure the improvements in performance resulting from the implementation of the JAM-GS-GAA FinFET in the domains of static, analog, and RF FoMs. This chapter has considered five configurations: C_1, C_2, C_3, C_4, and C_5, with descriptions provided in Table 4.1. The C_1 configuration consists of a conventional tri-gate JAM-GS-FinFET. The tri-gate is upgraded to a gate-all-around (GAA) structure with no spacer in the C_2 configuration. Compared to the C_2 configuration, the manufacturing process of the C_3 and C_4 configurations involves incorporating an extra layer of a single-k spacer. The C_3 configuration features air in the spacer region, while the C_4 configuration comprises SiO_2. The JAM-GS-GAA-FinFET arrangement with a dual-k spacer is used in the C_5 configuration. The C_5 configuration employed a HfO_2 high-k spacer for the inner layer and a SiO_2 low-k spacer for the outer layer. Because silicon in SiO_2 makes the silicon channel more flexible, reducing the likelihood of encountering dangling bonds and interface traps. The remainder of the chapter is: Section 2 covers device structure and physical models. Sections 3 and 4 discuss the experimental calibration and device manufacturing feasibility. Section 5 analyzes the effects of dual-k spacers on various device performances. The findings and implications of this analysis are summarised in Section 6.

Table 4.1: Details of different configurations used for comparison [10].

Configuration Name	Device Descriptions	Spacer Details
C_1	JAM-GS-FinFET	NA
C_2	JAM-GS-GAA-FinFET without spacer	NA
C_3	JAM-GS-GAA-FinFET with single-k spacer	Air, k = 1
C_4	JAM-GS-GAA-FinFET with single-k spacer	SiO_2, k = 3.9
C_5	JAM-GS-GAA-FinFET with dual-k spacer	SiO_2, k = 3.9 and HfO_2, k = 25

4.2 DEVICE DESIGN AND PHYSICAL MODELS

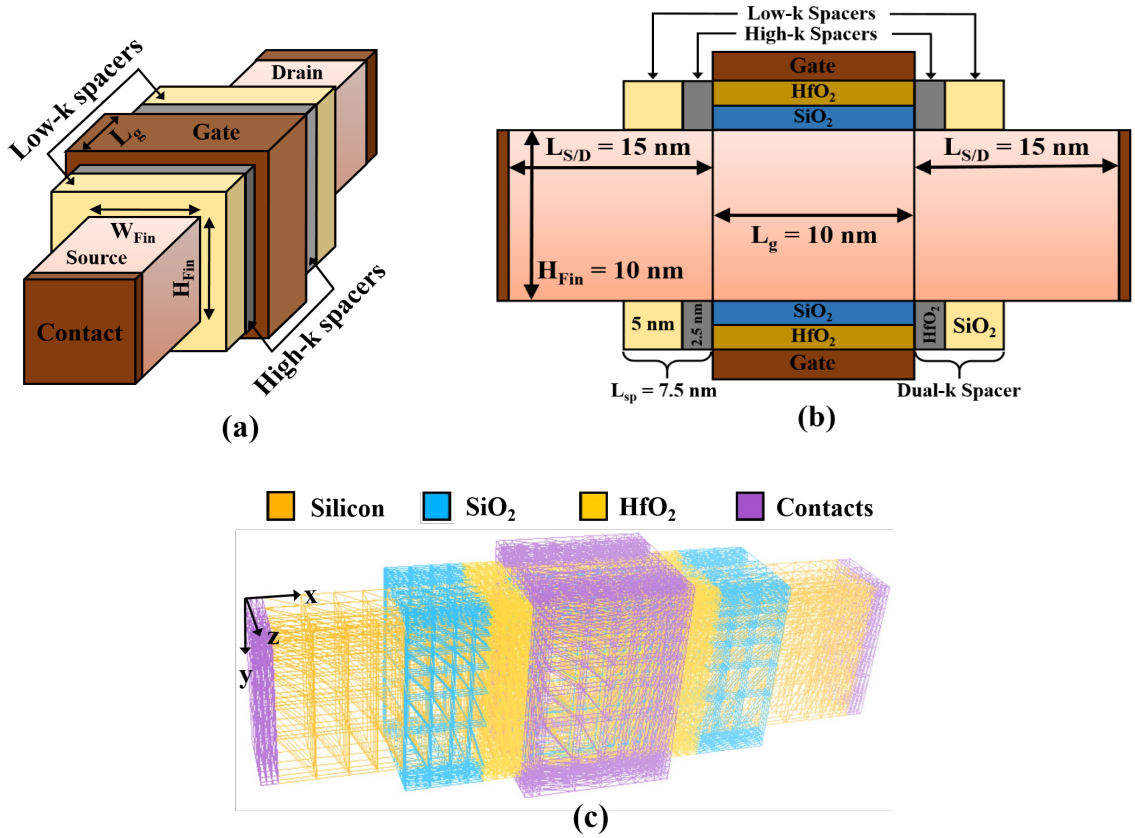

Figure 4.1: (a) Methodical 3D, (b) horizontally sliced 2D, and (c) 3D meshed designs of the proposed JAM-GS-GAA FinFET device with dual-k spacers [10].

Figure 4.1(a-c) exhibits the proposed device with dual-k spacers in its methodical 3D, horizontally sliced 2D, and 3D meshed designs, respectively. A comprehensive summary of the different parameters of device architecture is listed in Table 4.2. The structure's fins are made of silicon. The dual-k spacer separates into 5 nm (SiO_2) and 2.5 nm (HfO_2) spacer lengths, with the total spacer length (L_{sp}) being 7.5 nm. The gate oxide is built using HfO_2 and SiO_2. By setting H_{Fin}/W_{Fin} = 2, the width quantization condition [11, 12] is guaranteed to be satisfied across all simulations. With reduced doping in the channel area compared to the source/drain area, all three regions are doped with n-types to enhance device performance and minimize parasitic capacitance. Titanium nitride (TiN) is the preferred

substance for use in metal gates, which has superior characteristics and a work function of 4.65 eV [13]. The transfer characteristics were obtained by systematically increasing the gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) from 0 V to 1.5 V and 0 V to 0.5 V, respectively, with increments of 0.05 V. On the other hand, the output characteristics were obtained by ramping V_{gs} from 0 V to 0.5 V and V_{ds} from 0 V to 1.5 V, using a step size of 0.05 V.

Table 4.2: Values of different parameters used for simulation [10].

Parameters	**Symbol**	**Value**	**Unit**
Source/Drain Length	$L_{S/D}$	15	nm
Gate Length	L_g	10	nm
Spacer Length	L_{sp}	7.5	nm
Oxide Thickness	t_{ox}	1	nm
Fin Height	H_{Fin}	10	nm
Fin Width	W_{Fin}	5	nm
Channel Doping	N_{Ch}	1×10^{16}	cm^{-3}
Source/Drain Doping	$N_{S/D}$	5×10^{18}	cm^{-3}
Work Function	ϕ_m	4.65	eV
Temperature	T	300	K
Gate-Source Voltage	V_{gs}	1.5	V
Drain-Source Voltage	V_{ds}	0.5	V

All the considered configurations are simulated with the assistance of the Atlas 3D simulator [14], with the Poisson and Continuity equations serving as the general basis for the modeling. However, formulae and supplementary physical models are required to obtain more credible and precise results. Therefore, many different physical models are

built into the scenarios. The consequences of quantum confinement are a critical factor that cannot be disregarded in rapidly scaling systems. It is for this reason that the Bohm Quantum Potential (BQP) model is incorporated [14], which comprises a position-dependent quantum potential (Q). Further models considered are Fermi-Dirac statistics, Crowell-Sze impact ionization, concentration-dependent mobility, Klaassen tunneling, SRH recombination, and bandgap narrowing [14]. Incorporating Fermi-Dirac statistics is necessary to accommodate the characteristics of heavily doped materials. The Crowell-Sze model incorporates the phenomenon of impact ionization. The concentration-dependent mobility model has been activated to establish a correlation between the mobility of carriers in low fields at a temperature of 300 K and the concentration of impurities. The band-to-band Klaassen tunneling model accounts for direct and indirect electron tunneling between the conduction and valence bands. Implementing the SRH recombination model with a fixed carrier lifetime of 1×10^{-7} s accounts for the generation and recombination effects. The model of bandgap narrowing has been incorporated to accommodate the reduction in the separation of the bandgap due to the occurrence of intense doping. Newton and Block iteration solve all carrier motion math issues [14].

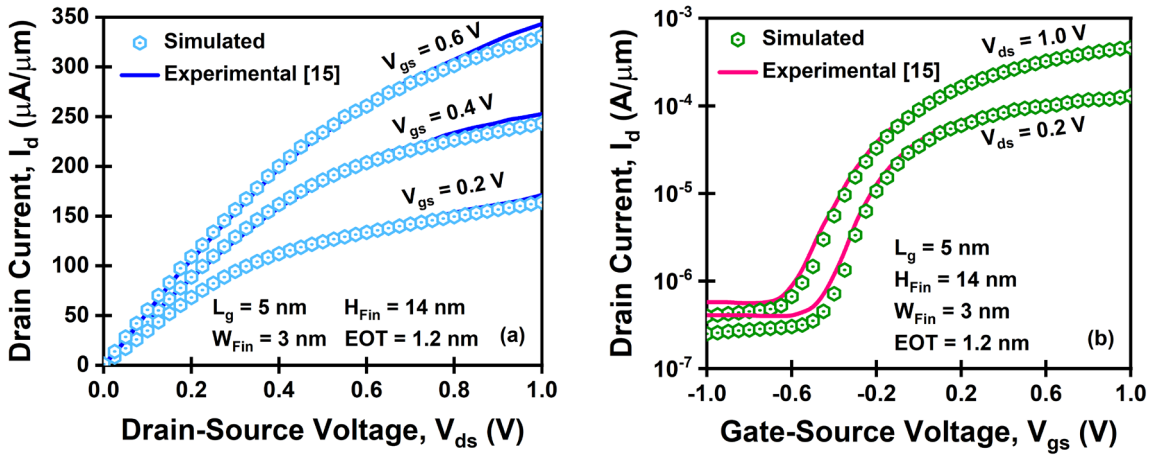

Figure 4.2: Experimental calibration of the (a) output and (b) transfer characteristics of the GAA FinFET device [10, 15].

4.3 EXPERIMENTAL CALIBRATION

In order to verify the physical models, the GAA FinFET is validated with the actual results of Lee et al. [15]. The published parameters for the device dimensions and anticipated silicon throughout the fin region are used to check the accuracy of the models. **Figure 4.2(a)** shows the output characteristics of the GAA FinFET device at varying gate voltages, and **Figure 4.2(b)** shows the transfer characteristics at varying drain voltages. The high degree of alignment between the actual and simulated output and transfer features supports the model selections.

4.4 FABRICATION FEASIBILITY

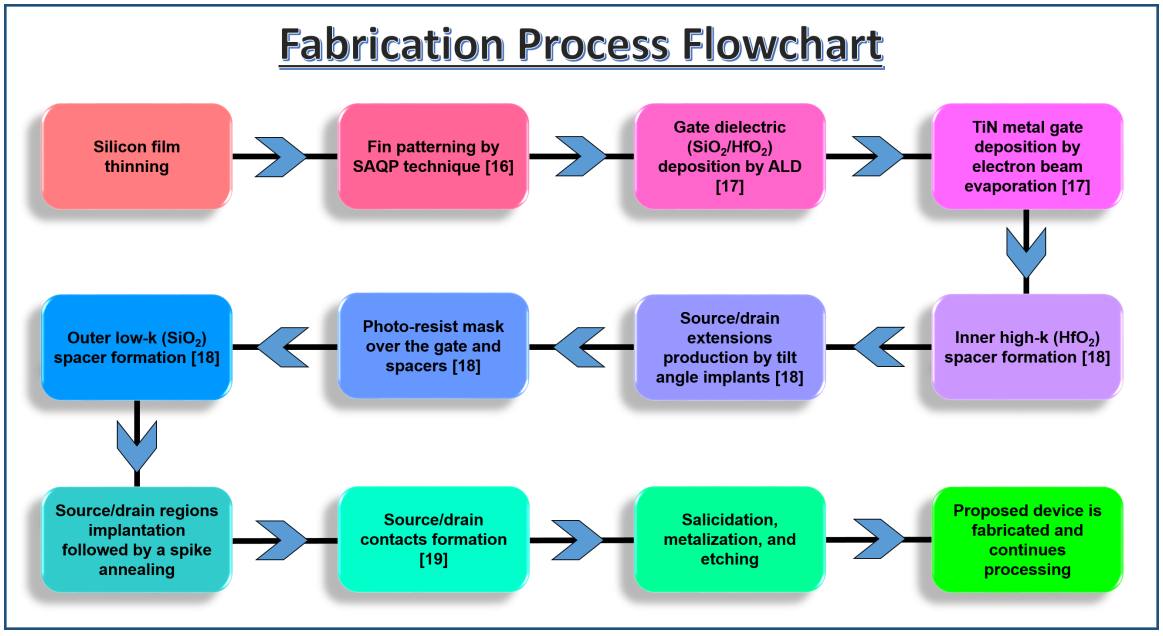

Figure 4.3: JAM-GS-GAA FinFET with dual-k spacers fabrication process flowchart [10].

Figure 4.3 presents a detailed procedure for the fabrication of JAM-GS-GAA FinFET with dual-k spacer, showcasing the practicality of the proposed device. The first stage involves thinning the silicon film, which is then succeeded by fin patterning through the self-aligned quadruple patterning (SAQP) technique [16]. The process of oxidation and etching is

employed after the fin patterning. The deposition of the gate dielectric (SiO_2/HfO_2) onto the silicon interfacial layer is carried out through the utilization of atomic layer deposition (ALD) [17]. The gate dielectric is then covered with a metal gate made of TiN using electron beam evaporation at room temperature [17]. High-k spacers (HfO_2) are deposited on both sides, and source/drain extensions are produced utilizing tilt angle implants to achieve symmetric doping profiles [18]. Next, a photoresist mask is created over the gate and spacers, followed by the formation of low-k spacers (SiO_2) within the remaining extension [18]. The implantation of the source and drain regions is followed by a spike annealing process to activate the dopants in the source and drain regions. The formation of source and drain contacts is followed by the deposition of metal interconnect layers [19]. The device fabrication process is finalized by executing additional backend processing steps, including salicidation, metalization, and etching. The JAM-GS-GAA FinFET, featuring a dual-k spacer, is fabricated and undergoes testing and characterization to evaluate its electrical characteristics.

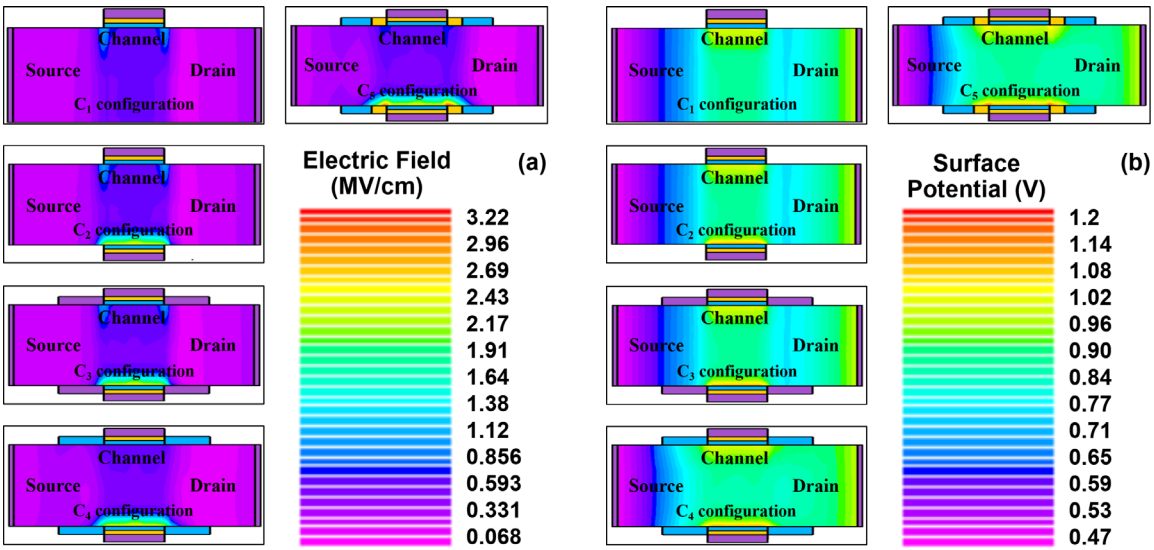

Figure 4.4: (a) Electric field and (b) surface potential contour plots along the channel across the range of configurations [10].

4.5 RESULTS AND DISCUSSION

This section compares the five considered configurations to examine the effectiveness of the JAM-GS-GAA-FinFET with a dual-k spacer on important static, analog, and RF performance metrics.

4.5.1 Static Performance

In this subsection, the static parameters like the electron velocity, electric field, surface potential, and band energy profiles are computed at a constant V_{gs} = 1.5 V and V_{ds} = 0.5 V to quantify the electrical behavior of the device. **Figure 4.4(a)** and **Figure 4.4(b)** exhibit the electric field and surface potential contour plots along the channel across the range of configurations, and the most improved electric field and surface potential profiles have been observed for the C_5 configuration because of the gate fringing fields that propagate through the high-k spacers. Additionally, the peak values of the electric field and surface potential in the channel area against various configurations are displayed in **Figure 4.5(a)**, with the peak value for both parameters observed for the C_5 configuration. The variation in electron velocity across various configurations is demonstrated in **Figure 4.5(b)**. The incorporation of a dual-k spacer increases electron mobility, thereby augmenting the velocity of electrons. Accordingly, a discernible increase in the velocity of the electrons can be seen in the channel region when the C_5 configuration is utilized. **Figure 4.5(c)** portrays the valence and conduction band energy profiles along the channel against V_{gs} for the five considered configurations. Analysis of **Figure 4.5(c)** indicates that a notable barrier between the channel and drain is present in the C_1 configuration. In contrast, the barrier height is considerably reduced in the C_5 configuration because of the elevated fringing fields in the underlap zone, thus amplifying the effective channel width.

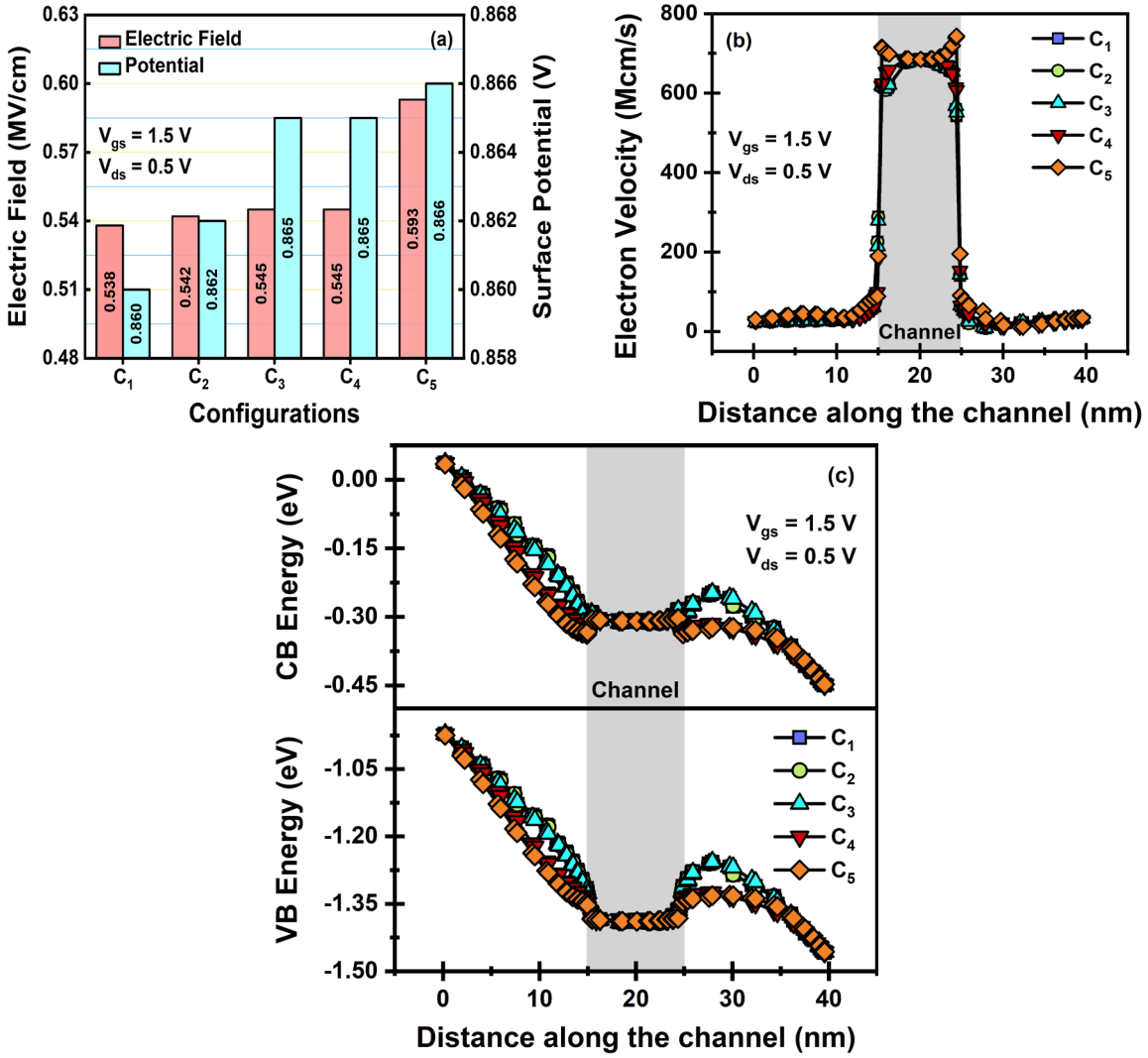

Figure 4.5: Plot of (a) electric field and potential peak values, (b) electron velocity, and (c) valence and conduction band energy profiles across various configurations [10].

4.5.2 Analog Performance

This subsection evaluates several important analog parameters from the analog applications perspective. **Figure 4.6(a)** depicts the variation in ON-current (I_{on}) against the different configurations. The I_{on} current is the value of the drain current obtained at V_{gs} = 1.5 V and V_{ds} = 0.5 V. It can be seen that maximum I_{on} is observed for the C_5 configuration. I_{on} is 35.34% higher for the C_5 configuration than the C_1 configuration. It is attributed to the effects of the fringing field in the underlap zones. The OFF-current (I_{off}) for considered

configurations is plotted in **Figure 4.6(b)**. The I_{off} current is the value of the drain current obtained at V_{gs} = 0 V and V_{ds} = 0.5 V. The value of I_{off} found for the C_1 configuration is 4.24×10^{-11} A, which decreases drastically to 5.54×10^{-13} A for the C_5 configuration, for an improvement of over 76 times. This is because of the increase in spacer area; the depletion region increases, resulting in a wider fringing region and consequently better I_{off} and SCEs. **Figure 4.6(c)** displays the switching ratio (I_{on}/I_{off}) of different devices. The C_5 configuration has a greater I_{on} and a smaller I_{off} than the C_1 configuration, leading to an I_{on}/I_{off} ratio roughly 10^2 times higher. **Figure 4.6(d)** displays the threshold voltage (V_{th}) shift across the range of configurations studied. The V_{th} shows an increment of 29.79% for the C_5 configuration related to the C_1 configuration. This shows that the subthreshold device characteristics are enhanced as V_{th} rises linearly along with the spacer dielectric constant rise. Drain-induced barrier lowering (DIBL) derived using Equation (4.1) indicates drain bias management on the potential barrier in the channel region [20]. **Figure 4.6(e)** shows the DIBL plot for all five configurations. DIBL recorded for the C_1 configuration is 124.16 mV/V, which decreases to 41.46 mV/V for the C_5 configuration, improving SCEs by 66.61%. The leaking currents caused by the device's characteristics are indicated by the subthreshold swing (SS) metric, making it an essential one to measure. In order to boost SCEs, it is advised to decrease the amount of SS of all devices, as depicted in **Figure 4.6(f)**. The decrease in SS of 15.47% for the C_5 configuration demonstrates the success of the proposed device.

$$\text{DIBL} = \left|(V_{th})_{V_{ds}\,=\,0.5\ V} - (V_{th})_{V_{ds}\,=\,0.1\ V}\right| / (0.5 - 0.1) \tag{4.1}$$

The output characteristics (I_d - V_{ds}) at fixed V_{gs} for the different configurations are plotted in **Figure 4.7(a)**. Initially, I_d rises exponentially with V_{ds}, then increases gradually with a further rise in V_{ds}. The I_d is significantly lower for the C_5 than the C_1 configuration.

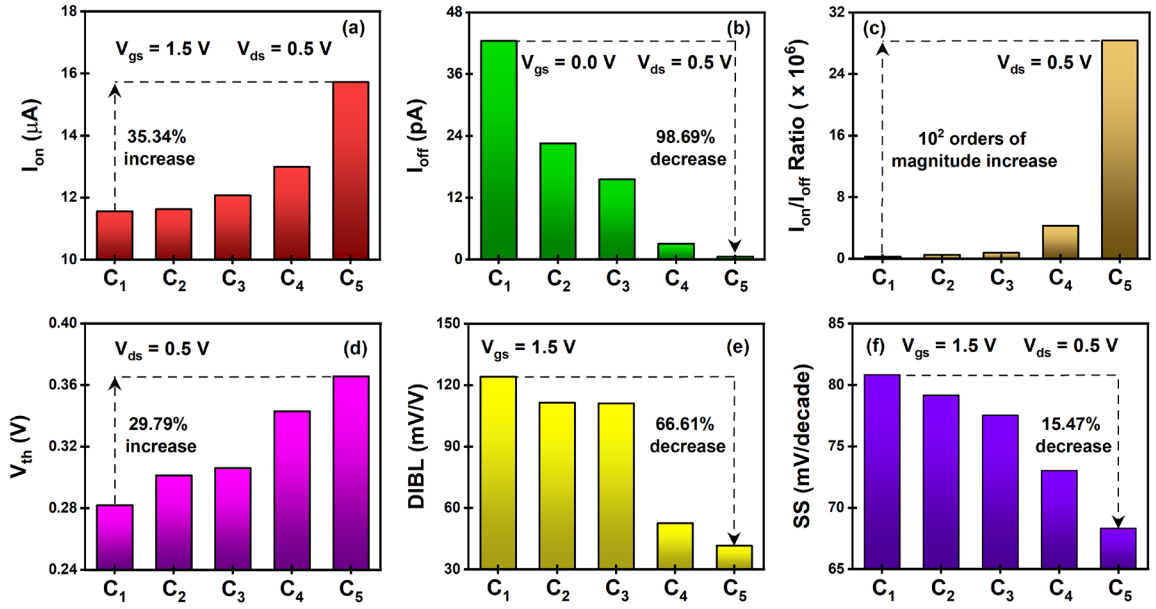

Figure 4.6: Variation in (a) I_{on}, (b) I_{off}, (c) I_{on}/I_{off} ratio, (d) V_{th}, (e) DIBL, and (f) SS against the different configurations [10].

This is because, for C_1, C_2, and C_3 configurations, as the V_{ds} is increased, the depletion region located at the drain end undergoes expansion in the channel region, thereby reducing the effective channel length [21, 22]. This decrease in the effective channel length results in a phenomenon known as channel length modulation (CLM), which in turn causes a rise in the drain current. In contrast, the CLM effect is mitigated in C_4 and C_5 configurations by using underlap single-k or dual-k spacers, which significantly reduces the width of the drain depletion region and lessens the impact of drain bias in the channel area [2]. Thus, the C_5 configuration exhibits improved device performance and stability due to good control over CLM and DIBL. The output conductance (g_d) primarily characterizes a device's propulsion capacity. **Figure 4.7(b)** exhibits the g_d for the configurations considered at fixed V_{gs}. As V_{ds} increases, the g_d initially drops before stabilizing at an undeviating value. Further, it can be seen that the g_d is lowest for the C_5 configuration because of reduced I_d due to good control over CLM and DIBL. The g_d value reduces by 21.13% for the C_5 configuration related to the C_1 configuration. The output resistance (R_{out}) determines the device's usable

power gain, and **Figure 4.7(c)** depicts the variation of R_{out} against V_{ds} for all five considered configurations. Initially, the R_{out} rises, reaches a peak value, and then starts decreasing with a rise in V_{ds}. The R_{out} peak value obtained for the C_1 arrangement is 0.84 MΩ, which is raised more than four times to 3.58 MΩ for the C_5 arrangement because of a lower g_d.

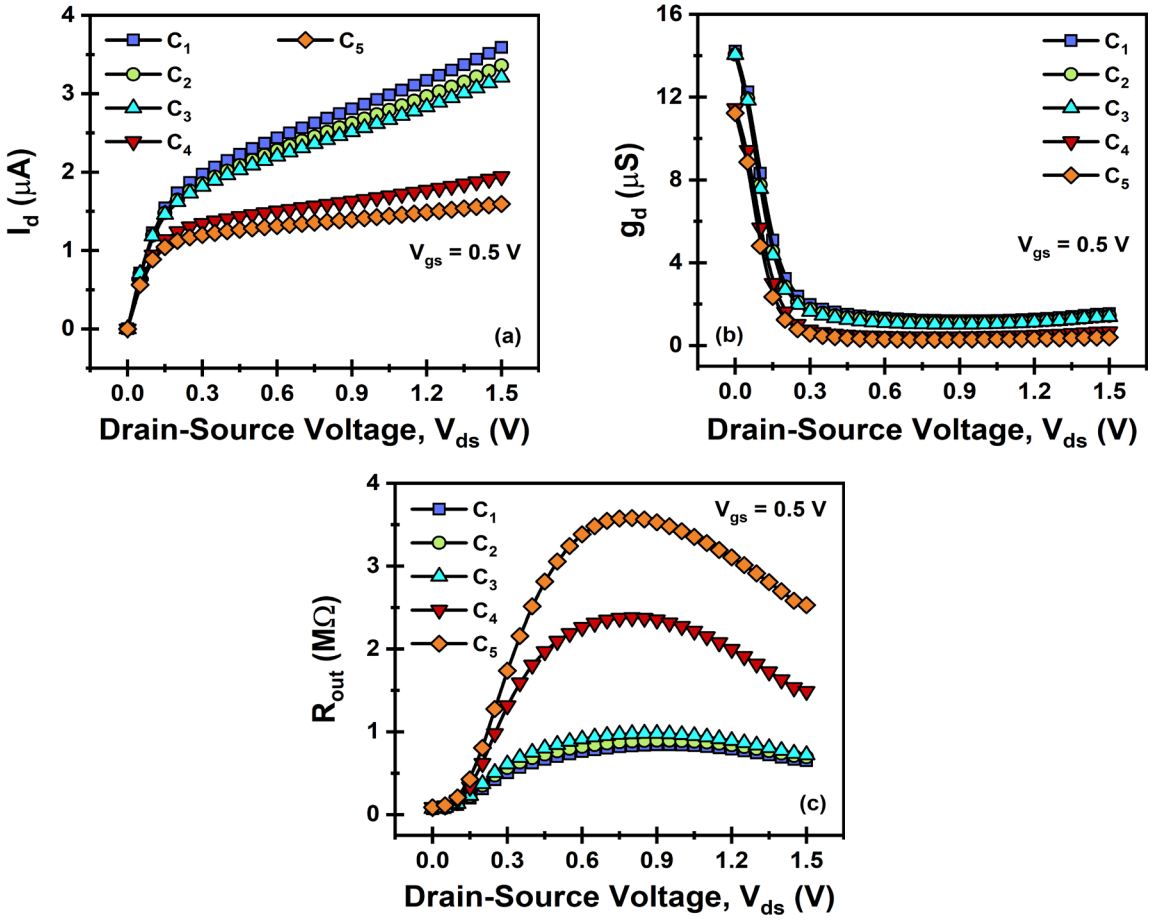

Figure 4.7: Plot of (a) I_d, (b) g_d, and (c) R_{out} against V_{ds} for all five considered configurations [10].

Noise efficiency, offset, DC gain, and bandwidth are controlled by the transconductance (g_m) in an amplifier. The transconductance generation factor (TGF) measures the efficiency of a device in converting small-signal AC input variations into changes in the output current. The TGF also reflects a device's signal amplification capabilities, albeit at the expense of some electricity. **Figure 4.8(a)** displays a collaborated plot of g_m and TGF against V_{gs} for the different configurations. Because the implication of

a dual-k spacer lowers the potential barrier and escalates the gate effective length, the highest g_m value is obtained for the C_5 configuration. In **Figure 4.8(a)**, the TGF value is higher for all combinations at low V_{gs} and decreases afterward for higher V_{gs} due to enhanced drain current. The C_5 configuration has the highest TGF compared to the others because it has the highest g_m, and a higher g_m number indicates a higher TGF value. The quality factor (QF) is one of the most crucial criteria for evaluating the device's switching behavior and is calculated using the maximum g_m value (obtained at 0.7 V) [23]. **Figure 4.8(b)** depicts the QF for the various device structures examined. The QF increases linearly with the maximum value being obtained for the C_5 configuration. The C_5 configuration demonstrates a 46.75% increase in QF compared to the C_1 configuration, attributed to

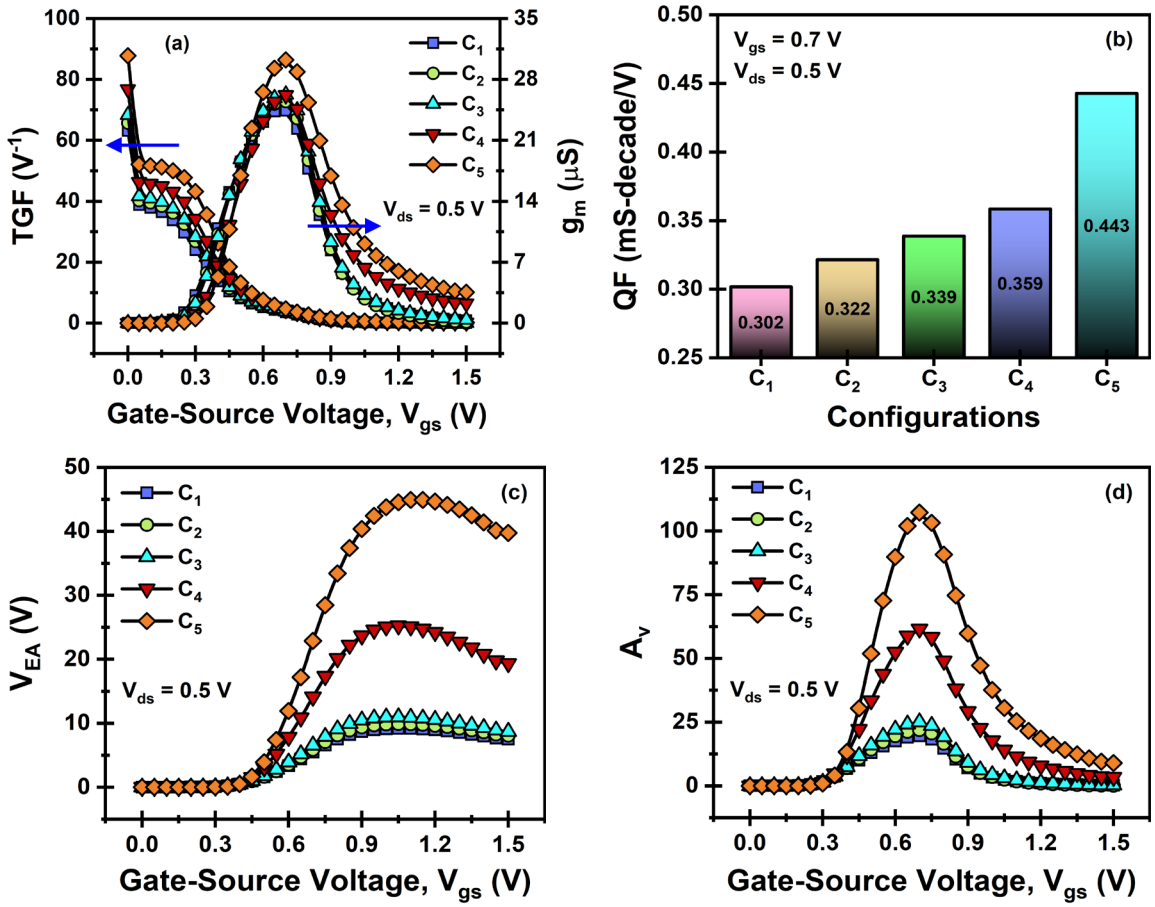

Figure 4.8: Variance of (a) g_m and TGF, (b) QF, (c) V_{EA}, and (d) A_v against V_{gs} for all five considered configurations [10].

enhancements in g_m and a reduction in SS. The variation in early voltage (V_{EA}) and intrinsic gain (A_v) against the V_{gs} across the range of configurations studied is shown in **Figure 4.8(c)** and **Figure 4.8(d)**. When V_{gs} increases, both V_{EA} and A_v first increase, peak, and then begin to decrease. The values of both V_{EA} and A_v are significantly higher for the C_5 configuration than the others. This is primarily because the g_d improves considerably, in addition to the improvement in I_d and g_m with the implementation of a dual-k spacer.

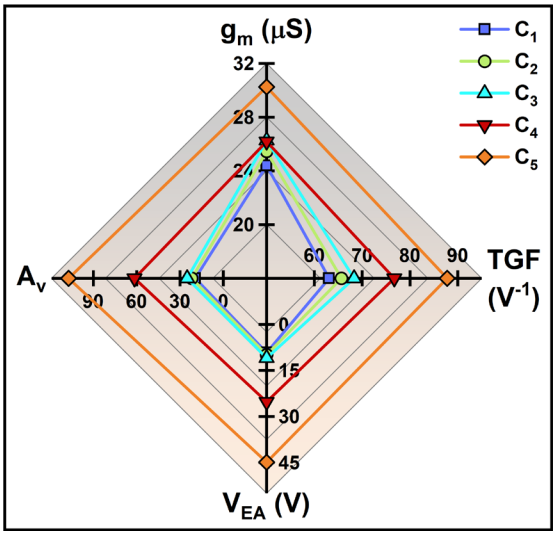

Figure 4.9: Spider-chart representation of the variance in peak values of g_m, TGF, V_{EA}, and A_v over the five different combinations [10].

Figure 4.9 exhibits the spider-chart representation of the variance in peak values of g_m, TGF, V_{EA}, and A_v over the five different combinations. The g_m peak value increases from 24.39 µS (C_1 configuration) to 30.25 µS (C_5 configuration), thereby exhibiting a rise of 24.03%. The TGF peak value rises by 39.12%, going from 63.09 V^{-1} (C_1 configuration) to 87.77 V^{-1} (C_5 configuration). Similarly, for the C_5 configuration, V_{EA} and A_v increased around fivefold to the values obtained for the C_1 configuration. For the C_1 configuration, V_{EA} is 9.18 V, and A_v is 19.52; for the C_5 configuration, both parameters are raised to 44.92 V and 107.23, respectively. A higher g_m, TGF, QF, V_{EA}, and A_v values suggest a greater enhancement factor, ensuring the device/component can be used in analog applications.

4.5.3 RF Performance

Several crucial RF parameters are evaluated in this subsection from the RF application's point of view. The RF performance assessment necessitates the use of factors such as gate resistance (R_g), drain-source conductance (g_{ds}), gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), and total-gate capacitance (C_{gg}). The parameters R_g, g_{ds}, C_{gs}, C_{gd}, and C_{gg} were determined through AC small-signal analysis conducted at a frequency of 1 MHz. The parameters like g_{ds}, C_{gs}, C_{gd}, and C_{gg} were obtained through direct extraction, while the value of R_g was determined with the assistance of Y-parameters (or admittance parameters) using the formula $R_g = (\text{Real } Y_{11})/(\text{Imag } Y_{11})^2$ [24, 25], where Y_{11} is known as the input admittance. **Figure 4.10(a-c)** displays a plot of C_{gs}, C_{gd}, and C_{gg} against V_{gs} for the different configurations. The C_{gs}, C_{gd}, and C_{gg} for all the configurations stay almost the same in the subthreshold region. However, a substantial variation in the C_{gs}, C_{gd}, and C_{gg} is found in the above-threshold region, particularly in the C_5 configuration. This is because the depletion capacitance dominates in the subthreshold region, and the limited charge storage and fixed charge distribution in the depletion region make it less susceptible to changes induced by fringing fields, whereas in the above-threshold region, inversion capacitance dominates, and fringing fields have a greater effect due to mobile charge carriers and their effective extension of capacitor plates in the channel region, increasing the effective capacitor area, thus amplifying the capacitance.

The current gain and unilateral power gain are unity (0 dB) at the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}), respectively. **Figure 4.11(a)** shows the peak value of f_T obtained at $V_{gs} = 0.6$ V for the five different configurations. The maximum g_m value is achieved at a consistent V_{gs} value across all structures. Consequently, the peak value of the f_T is also attained at a specific V_{gs} value due to its direct correlation with g_m.

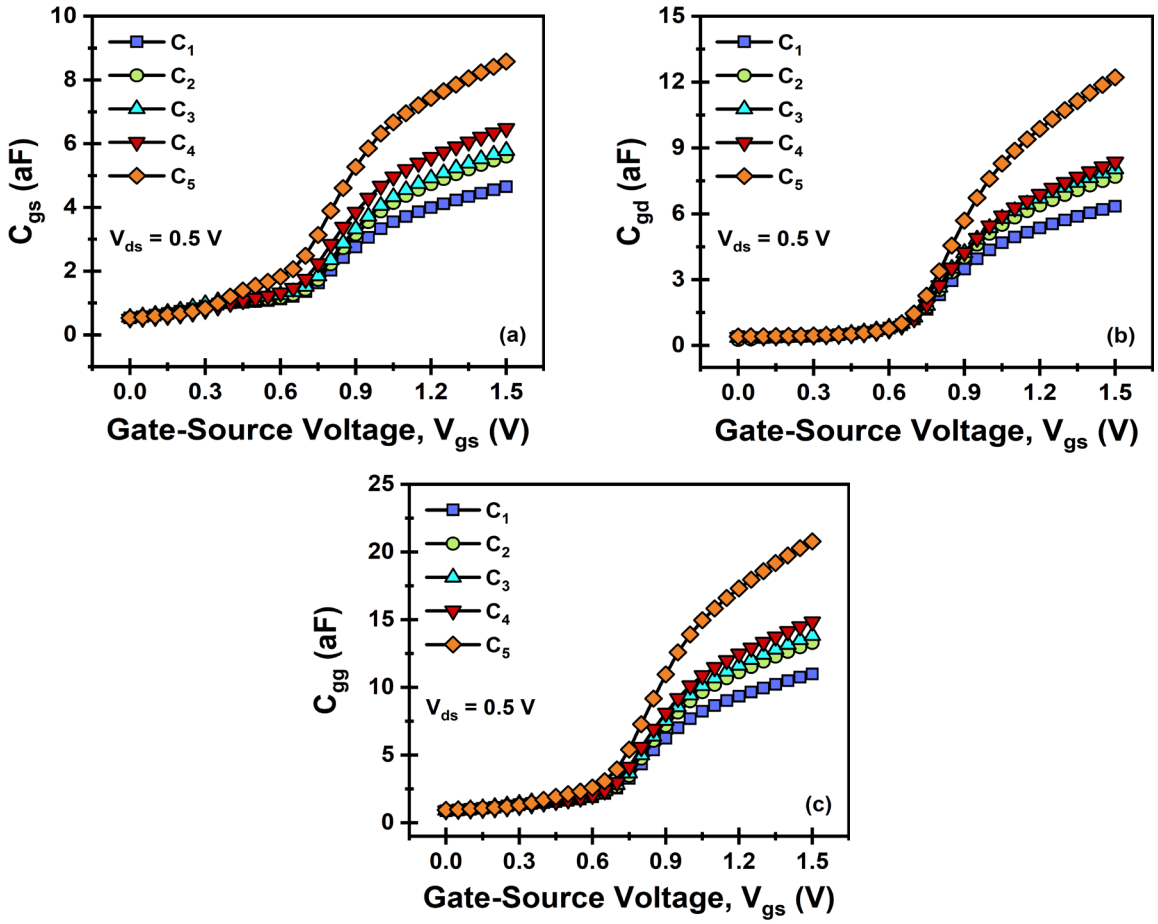

Figure 4.10: Plot of (a) C_{gs}, (b) C_{gd}, and (c) C_{gg} against V_{gs} for the different configurations [10].

The topmost value of f_T for the C_1 configuration is 1.94 THz, which reduces to 1.63 THz for the C_5 configuration owing to the increase in the gate capacitances. The variation of f_{max} against V_{gs} for the distinct configurations is depicted in **Figure 4.11(b)**. Due to the rise in gate capacitances, f_{max} is lowered by 24.10% for the C_5 compared to the C_1 configuration. The gain bandwidth product (GBP) is the product of the bandwidth and the gain of an amplifier. It can be calculated by Equation (4.2), depending on the C_{gd} and g_m values [26]. **Figure 4.11(c)** illustrates the maximum value of GBP obtained at V_{gs} = 0.55 V across the five varied configurations. Again, the GBP peak value is attained at a specific V_{gs} value due to its direct correlation with g_m. The maximum value of GBP for the C_1 configuration is 0.50 THz, but it escalates to 0.55 THz for the C_5 configuration because of increased g_m.

$$GBP = g_m/(20\pi \times C_{gd}) \quad (4.2)$$

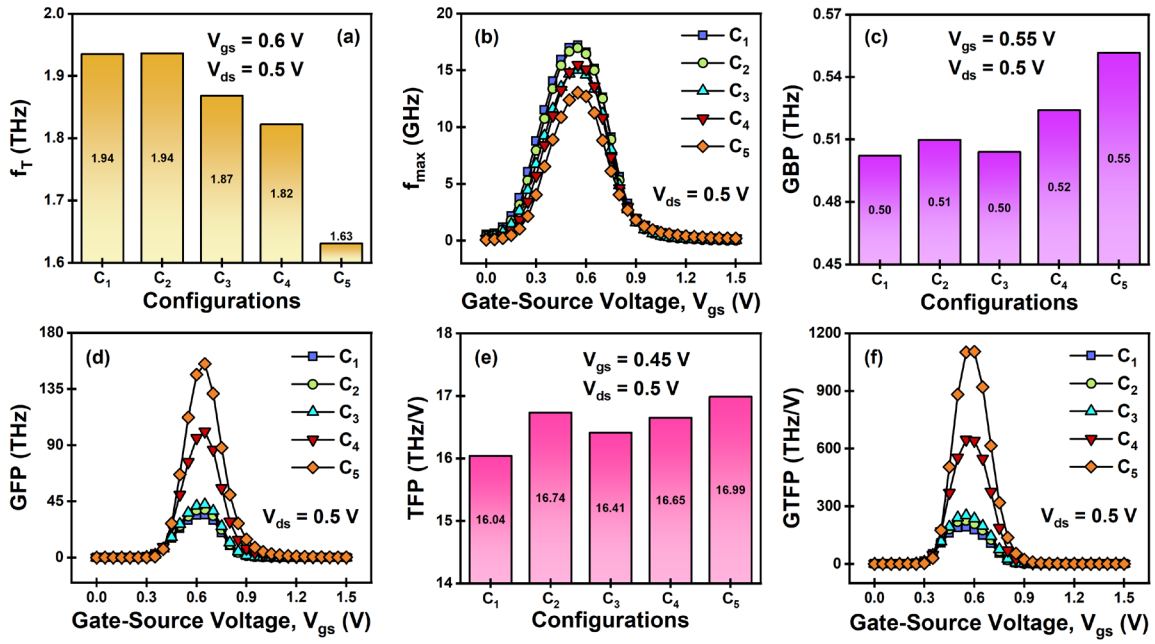

Figure 4.11: Variance in (a) f_T, (b) f_{max}, (c) GBP, (d) GFP, (e) TFP, and (f) GTFP against the different configurations [10].

Gain frequency product (GFP) is an important metric when working with high frequencies. **Figure 4.11(d)** exhibits the change in GFP with respect to V_{gs} for the five considered configurations. When V_{gs} increases, GFP first increases, peaks at 0.65 V, and then begins to decrease. For the C_5 configuration, the value of GFP increases by more than four times the value obtained for the C_1 configuration. This substantial increase in GFP can be attributed to the improvement in intrinsic gain. **Figure 4.11(e)** displays the peak value of the transconductance frequency product (TFP) obtained at V_{gs} = 0.45 V for the five different configurations. The TFP peak value is achieved at a particular V_{gs} value owing to its direct association with g_m and f_T. The C_1 configuration yields a peak TFP value of 16.04 THz/V, whereas the C_5 configuration has a higher TFP peak of 16.99 THz/V. Since the decrease in f_T offsets the escalation in TGF, the resulting increase in TFP is modest. The variation in gain transconductance frequency product (GTFP) against the V_{gs} across the

range of configurations studied is shown in **Figure 4.11(f)**. The trend observed in GTFP is analogous to that of GFP, owing to a similar underlying cause. The GTFP value for the C_5 configuration increases by more than five times compared to the value obtained for the C_1 configuration owing to A_v and TGF improvements.

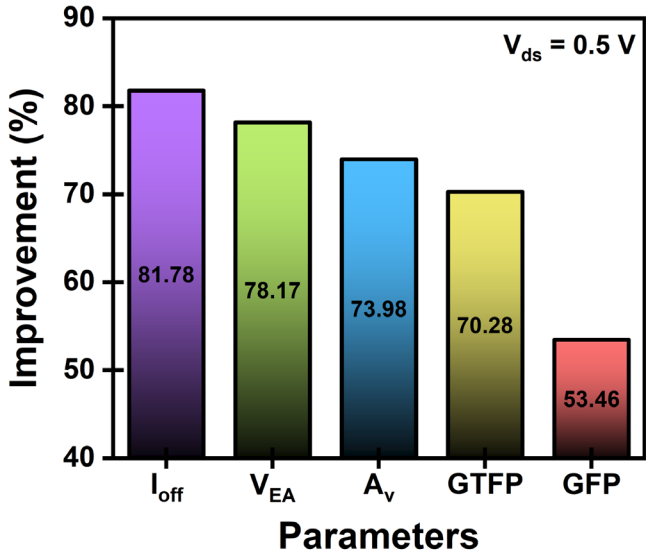

Figure 4.12: Representation of the improvement in I_{off}, V_{EA}, A_v, GTFP, and GFP parameters following the transition from the C_4 to the C_5 configuration [10].

There is no denying that the addition of a dual-k spacer structure makes the fabrication process more complicated. Therefore, the dual-k spacer structure (C_5 configuration) and the single-k spacer structure with SiO_2 (C_4 configuration) are compared to highlight better the benefits of the more complicated dual-k spacer structure. The percentage change following the transition from the C_4 configuration to the C_5 configuration assesses the extent of parameter improvement. **Figure 4.12** depicts a graphical representation of the percentage improvement of the mentioned parameters. The results indicate that transitioning from a C_4 configuration to a C_5 configuration yields significant enhancements in I_{off}, V_{EA}, A_v, GTFP, and GFP, with improvements of 81.78%, 78.17%, 73.98%, 70.28%, and 53.46%, respectively. Further, the I_{on}/I_{off} ratio rises seven

times with substantial improvement in other parameters, as shown throughout the paper. Thus, the dual-k spacer structure offers substantial advantages despite the complexity of its fabrication. In addition, the difference between the different static, analog, and RF FoMs (ΔFoMs) of C_5 and C_1 configurations have been evaluated using Equation (4.3). Table 3 displays the ΔFoMs for the assessed parameters. The observed enhancements in the static, analog, and RF ΔFoMs (barring the f_T and f_{max}) signify that the C_5 configuration outperforms the C_1 configuration, thus corroborating the efficacy of our proposed JAM-GS-GAA-FinFET with dual-k spacer device structure.

$$(\Delta\text{FoMs}) = (\text{FoMs})_{C_5\ \text{Conf.}} - (\text{FoMs})_{C_1\ \text{Conf.}} \quad (4.3)$$

Table 4.3: Overview of the prominent static, analog, and RF ΔFoMs [10].

Parameters	**(FoMs)$_{C5\ Conf.}$**	**(FoMs)$_{C1\ Conf.}$**	**(ΔFoMs)**
Electric Field (MV/cm)	0.593	0.538	0.055
Surface Potential (V)	0.866	0.860	0.006
Electron Velocity (Mcm/s)	743.40	683.12	60.28
g_m (μS)	30.25	24.39	5.86
TGF (V^{-1})	87.77	63.09	24.68
V_{EA} (V)	44.92	9.18	35.74
A_v	107.23	19.52	87.71
f_T (THz)	1.63	1.94	-0.31
f_{max} (GHz)	13.04	17.18	-4.14
GBP (THz)	0.55	0.50	0.05
GFP (THz)	155.03	34.28	120.75
TFP (THz/V)	16.99	16.04	0.95
GTFP (THz/V)	1104.36	191.84	912.52

4.6 SUMMARY

The impression of adding a dual-k spacer on the RFIC design viability of a JAM-GS-GAA FinFET in the sub-10 nanometer region is investigated in this chapter. The calculated findings of the proposed device are compared to those of a conventional FinFET and the devices without a spacer (no spacer), with air, and with a single-k spacer (SiO_2). It was observed that the proposed device improves the electron velocity, electric field, surface potential, and energy band profiles due to the fringing field effects. Thereby increasing the I_{on} of the C_5 configuration by 35.34%, I_{on}/I_{off} ratio by approximately 10^2 times, g_m by 24.03%, TGF by 39.12%, QF by 46.75%, V_{EA} and A_v by five times, while decreasing the I_{off} by over 76 times, g_d by 21.13%, DIBL by 66.61%, and SS by 15.47% compared to the C_1 configuration. Thus, due to its advantageous characteristics, the proposed device is an ideal option for high-performance CMOS circuits. Although the f_T and f_{max} drop are observed, the GFP and GTFP skyrocket more than five times. Also, the single-k spacer and dual-k spacer structures were compared to highlight the benefits of the more complicated dual-k spacer structure. The results indicate that transitioning from a single-k spacer to a dual-k spacer improves I_{off}, V_{EA}, A_v, GTFP, and GFP by 81.78%, 78.17%, 73.98%, 70.28%, and 53.46%, respectively. Thus, JAM-GS-GAA FinFET with dual-k spacer can be seen as a potential element in future low-power RFIC circuits.

With dual-k spacer engineering for low-power RFIC circuits, higher device performance in the static, analog, and RF FoMs is achieved. The growing interest in high ULSI applications and assuring better RF/microwave performance encourages the next chapter of this thesis to investigate the parasitic capacitances and small signal behavior of nano-scaled JAM-GS-GAA FinFETs.

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5

CHAPTER

Investigation of Parasitic Capacitances and Small-Signal Behavior of JAM-GS-GAA FinFET

- *This chapter investigates the parasitic capacitances and small-signal behavior of JAM-GS-GAA FinFET with GaAs as the fin material.*
- *The findings show that GaAs fins considerably decrease SCEs and parasitic capacitances. For GaAs, the I_{off} current lowers by 100 times, the I_{on}/I_{off} ratio rises by 10^3 times, DIBL halves, and SS decreases by 26% compared to silicon.*
- *The parasitic capacitances also decrease with GaAs fins: C_{gs} by 52.71%, C_{gd} by 75.48%, and C_{gg} by 67.52%. Due to this significant parasitic capacitance drop, GBP and TFP peak values rise 10 times.*
- *The impact of parameters such as L_g, N_{Ch}, W_{Fin}, ϕ_m, and T on the parasitic capacitances and S-parameters of GaAs JAM-GS-GAA FinFET is also investigated. Parasitic capacitances decrease with shorter L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m. In contrast, S-parameters increase with bigger L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m at high frequencies.*
- *Consequently, by establishing a balance with gate length, the GaAs JAM-GS-GAA FinFET with the above specifications can be used for both low-power ULSI switching applications and microwave oscillators and amplifiers.*

5.1 INTRODUCTION

The influence of dual-k spacers on different configurations under consideration was thoroughly explored in **Chapter 4**, and the improvements in performance resulting from implementing the JAM-GS-GAA FinFET in the static, analog, and RF FoM domains were simulated. The proposed device achieved higher performance with dual-k spacer engineering for low-power RFIC circuits. However, the dimensions of CMOS devices are scaled down continuously to meet the ULSI industry's demand, and further downscaling will be very demanding due to many practical limitations, like parasitic capacitances, threshold voltage roll-off, drain-induced barrier lowering (DIBL), etc. Unsurprisingly, further enhancement in transistor performance and speed while downscaling the device will be possible using new semiconductor materials. Given future logic applications, III-V compound semiconductor materials are the encouraging contenders among the latest materials [1]. Compared to silicon, gallium arsenide (GaAs) demonstrate many high-caliber electrical properties, for instance, large energy band gap, high electron mobility, high device on-currents at the low power supply, and a simple hetero-structure approach in microelectronic devices [2, 3]. However, some technical challenges are associated with using these new wide bandgap semiconductor materials. It includes exploiting these materials to their full potential, competing directly against existing silicon power devices, and further development and commercialization. The major hurdle in GaAs-bases devices is infeasible monolithic integration with silicon digital circuitries, no consistent scaling technology driven by a well-planned roadmap [4], and the unavailability of thermodynamically stable, high-quality insulators on GaAs, which can complement the device standards as silicon dioxide (SiO_2) on silicon.

However, after years of endeavors, it has been feasible to form a high-quality dielectric on III-V semiconductors with atomic layer deposition (ALD) [5] and molecular beam epitaxy (MBE) [6, 7]. The gate leakage current in a device can be reduced significantly by using a larger energy band gap gate material, which provides a higher potential barrier than other materials of the same thickness. Aluminum oxide (Al_2O_3) is a highly preferable gate dielectric because of its high thermal stability, good interface quality on GaAs, large energy band gap of 9 eV, and it remains amorphous under normal processing conditions [5, 8]. However, the dielectric constant of Al_2O_3 is small and insufficient for aggressive effective oxide thickness (EOT) scaling [9]. To further scale down the EOT, Gate-Stack (GS) configuration [10] of high-k dielectric HfO_2 with dielectric constant k = 25 and Al_2O_3 k = 9 has been formed on GaAs by ALD [11].

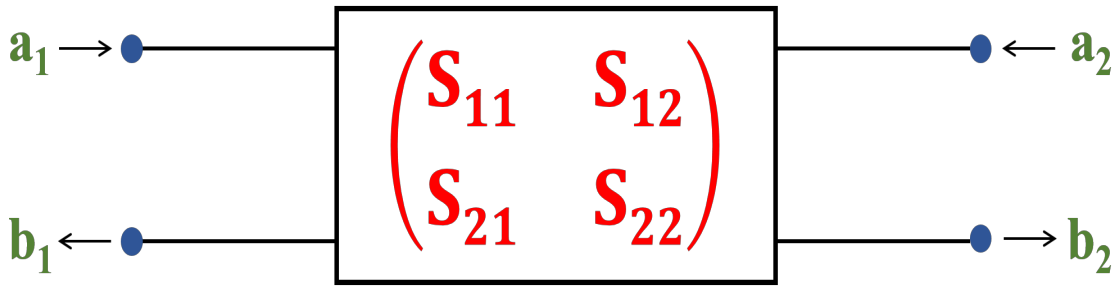

Figure 5.1: Generalized two-port network for S-parameter measurement [12].

The small-signal behavior of a transistor may be precisely characterized by utilizing the transistor's scattering (S) parameters, which can be reliably calculated using a vector network analyzer (VNA) [12]. **Figure 5.1** depicts a generalized two-port network for S-parameter measurement. Assuming that each port is terminated at the reference impedance, the four S-parameters of the 2-port can be calculated using Equations (5.1-5.4). The equations mentioned for S_{11} and S_{21} are obtained by making the incident signal a_2 equal to zero. Similarly, S_{12} and S_{22} are obtained by setting a_1 equal to zero.

S_{11} = Reflected Signal / Incident Signal = b_1/a_1 (5.1)

S_{12} = Reflected Signal / Incident Signal = b_1/a_2 (5.2)

S_{21} = Transmitted Signal / Incident Signal = b_2/a_1 (5.3)

S_{22} = Transmitted Signal / Incident Signal = b_2/a_2 (5.4)

The above basic conversion formulae make it feasible to derive additional analogous characteristics such as hybrid (H), admittance (Y), and impedance (Z) parameters [13, 14]. When performed at high frequencies, measurements of MOSFET S-parameters are the approach that proves to be the most fruitful in learning about the device. S-parameters are typically used for networks that operate at radio and microwave frequencies because it is extremely difficult to predict the current and the voltage compared to signal power and energy analysis when the frequency is high. It isn't easy to produce open and short circuits at high frequencies, which are important for defining most n-port characteristics. This indicates that waves and matching terminations play a significant influence on the way that microwave engineers deal with S-parameters. This strategy also contributes to mitigating the unfavorable consequences of reflection [15].

As the device dimension scales down, the parasitic capacitances and many higher-order effects become prominent. These effects significantly impact the device's performance, making it incompatible with low-power and switching applications. Thus, there is a necessity to investigate the C-V (capacitance-voltage) measurements besides I-V (current-voltage) measurements to analyze the impact of parasitic capacitances on the device performance and correctly estimate how the device would behave under various environmental circumstances [16, 17]. Consequently, this chapter compares the parasitic capacitances of JAM-GS-GAA FinFET using silicon and GaAs as fin materials. Further, the ON-current (I_{on}), OFF-current (I_{off}), switching ratio (I_{on}/I_{off}), subthreshold swing (SS),

and parasitic capacitances of the proposed device are examined with variations in gate length (L_g), channel doping (N_{Ch}), fin width (W_{Fin}), gate electrode work function (ϕ_m), and temperature (T). Then, a comprehensive analysis of the small-signal behavior regarding the S-parameters of GaAs JAM-GS-GAA FinFET has been conducted across the terahertz (THz) frequency range. The effect that L_g, N_{Ch}, W_{Fin}, ϕ_m, and T have on the S-parameters of GaAs JAM-GS-GAA FinFET was carried out. This chapter is organized as follows: Section 2 outlines the device structure and physical models. Sections 3 and 4 focus on calibrating experimental and simulation data and fabrication feasibility. Section 5 analyzes the impact of GaAs on the parasitic capacitances and short-channel effects. Also, the impact of the mentioned parametric variations on parasitic capacitances and small-signal behavior of GaAs JAM-GS-GAA FinFET is investigated. Section 6 summarizes the chapter.

5.2 DEVICE DESIGN AND PHYSICAL MODELS

The proposed device's systematic three-dimensional, horizontally, and vertically chopped two-dimensional architectures with parasitic capacitances are labeled in **Figure 5.2(a-c)**. GaAs and silicon materials make up the fin section of the structure. The device dimensions consist of fin height (H_{Fin} = 10 nm), source/drain length ($L_{S/D}$ = 10 nm), L_g = 7 nm, and W_{Fin} = 5 nm. H_{Fin}/W_{Fin} = 2 ensures the width quantization property is met across all simulations. The overall thickness of the gate oxide is 1 nm, which is layered using a mixture of Al_2O_3 and HfO_2 in equivalent proportions. N-type uniform doping with silicon as the dopant is used in the entire fin area. The doping in the source/drain regions ($N_{S/D}$) is 5×10^{18} cm^{-3}, and in the channel region (N_{Ch}) is 1×10^{16} cm^{-3}. Titanium nitride (TiN) is considered the metal gate, with a work function (ϕ_m = 4.65 eV) due to its compatibility with CMOS processing, low resistivity, high purity, and thermal stability [18]. Temperature (T)

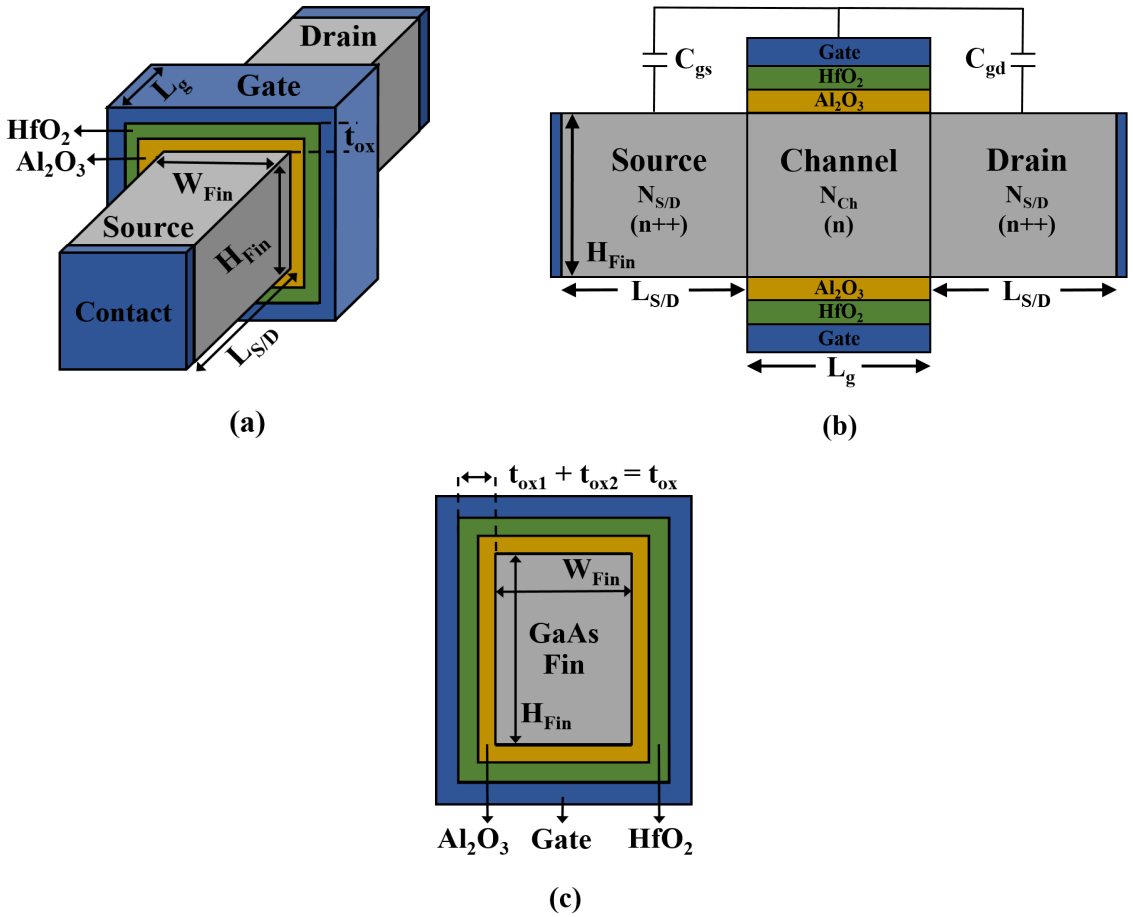

Figure 5.2: (a) Systematic simulated 3-D structure, (b) horizontal, and (c) vertical 2-D view of GaAs JAM-GS-GAA FinFET with parasitic capacitances [3].

has been set at 300 K, and gate voltage (V_{gs}) and drain voltage (V_{ds}) are varied from 0 - 1 V and 0 - 0.5 V, respectively. AC frequency has been varied within a single SOLVE statement using the NFSTEP, FSTEP, and MULT.F parameters for small-signal analysis. The NFSTEP indicates how many frequency steps are to be simulated, FSTEP indicates the step size, and MULT.F specifies the start frequency is multiplied by the step size for the specified number of steps. The start frequency is set at 4 THz, FSTEP is 0.5, and NFSTEP is 12. The study involves examining L_g from 5 nm to 10 nm, changing N_{Ch} spans from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}, exploring W_{Fin} within the range of 3 nm to 7 nm, altering ϕ_m from 4.55 eV to 4.75 eV, and varying T from 250 K to 450 K to study the effect that L_g, N_{Ch}, W_{Fin}, ϕ_m, and T have on the parasitic capacitances and S-parameters.

The proposed device has been simulated by the SILVACO Atlas 3D simulator [19]. The Continuity and Poisson equations provide the backbone of the device simulation, but supplementary physical models and equations are necessary to get more correct findings. Consequently, several different physical models are integrated into the simulations. In aggressively scaled devices, quantum confinement effects become prominent and cannot be neglected. Thus, the Bohm Quantum Potential (BQP) model consisting of a position-dependent quantum potential (Q) is employed to incorporate the quantum confinement effects [19]. The Shockley-Read-Hall (SRH) recombination model is implemented with a 1×10^{-7} s fixed carrier lifetime to include the generation and recombination effects. The band-to-band Klaassen tunneling model explores both direct and indirect tunneling of electrons between the conduction and valence bands. The concentration-dependent mobility model can link low-field carrier mobility at 300 K to impurity concentration. Fermi-Dirac statistics are used to account for the characteristics of heavily doped materials. The impact ionization effects are introduced with the help of the Crowell-Sze impact ionization model and the bandgap narrowing model is introduced to implement the bandgap narrowing effects. Furthermore, all the mathematical issues associated with the carrier motions are solved using Newton and Block iteration methods [19].

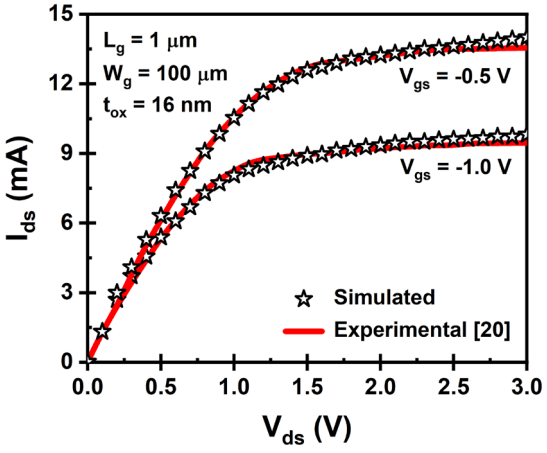

Figure 5.3: Experimental and simulated output characteristics of Al_2O_3/GaAs MOSFET [3, 20].

5.3 EXPERIMENTAL CALIBRATION

As this chapter emphasizes the effectiveness of GaAs as a fin material, the published results of Ye et al. [20] are extracted without changing the device parameters to validate the above-discussed physical models. **Figure 5.3** displays the experimental and simulated output characteristics of Al_2O_3/GaAs MOSFET at V_{gs} = -1.0 V and V_{gs} = -0.5 V. The fact that the simulated and experimental data sets coincide closely lends credence to the models chosen in the simulations.

5.4 FABRICATION FEASIBILITY

Figure 5.4 exhibits the fabrication feasibility of the proposed GaAs JAM-GS-GAA FinFET using a step-by-step fabrication process flowchart. The first step is the GaAs film thinning, and then fin patterning is performed by the self-aligned quadruple patterning (SAQP) technique [21]. Using the atomic layer deposition (ALD), the gate dielectric (Al_2O_3/HfO_2) deposition is executed on the GaAs interfacial facial [22]. Afterward, a metal gate (TiN) is

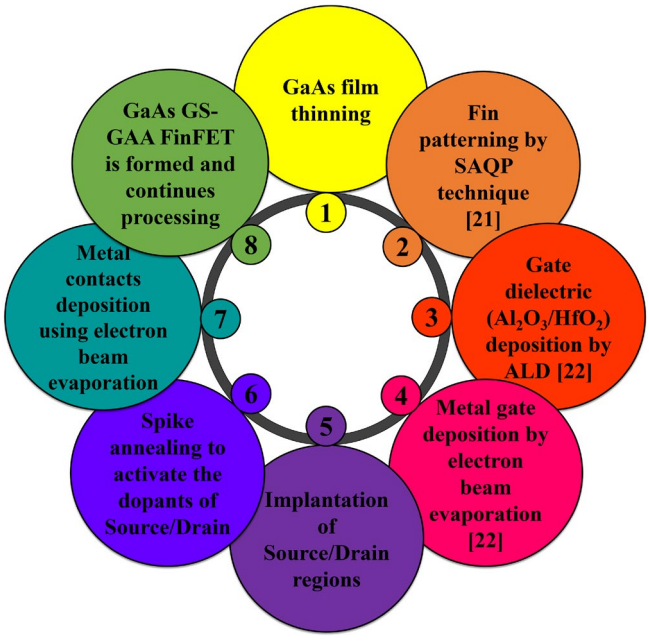

Figure 5.4: Fabrication process flowchart of proposed GaAs JAM-GS-GAA FinFET [3].

grown at room temperature on the top of the gate insulator by electron beam evaporation [22]. The drain and source regions are implanted, and the dopants of these regions are activated using spike annealing. By electron beam evaporation, drain/source metal contacts are deposited, followed by a lift-off process. This completes the process of manufacturing the proposed device.

5.5 RESULTS AND DISCUSSION

5.5.1 Impact of GaAs on Parasitic Capacitances

This subsection compares the impact of silicon and GaAs as fin materials on the analog metrics and parasitic capacitances of the proposed JAM-GS-GAA-FinFET. **Figure 5.5(a)** and **Figure 5.5(b)** represent the comparison of I_d - V_{gs} characteristics in log scale and switching ratio (I_{on}/I_{off}) for silicon and GaAs JAM-GS-GAA FinFET, respectively. The drain current (I_d) enhances, and the leakage current (I_{off}) reduces appreciably, so the I_{on}/I_{off} ratio increases $\sim 10^3$ times for GaAs. The I_{off} ranges between 10^{-12} and 10^{-10} for GaAs and silicon, respectively. GaAs large energy bandgap and high electron mobility are the primary reasons for this significant reduction in the leakage current. **Figure 5.5(c)** demonstrates the plot of threshold voltage (V_{th}) for silicon and GaAs JAM-GS-GAA FinFET. A higher V_{th} is obtained for GaAs (0.41611 V) than silicon (0.24795 V). The study of DIBL and SS becomes essential for aggressively scaled devices. DIBL signifies the drain bias control on the channel region's potential barrier, whereas SS provides perception about the leakage currents related to device characteristics. The lower the values of DIBL and SS, the better the short-channel effects (SCEs). **Figure 5.5(d)** exhibits the collaborated plot of DIBL and SS for silicon and GaAs. DIBL reduces by ~50% from 263.19 mV/V to 130.04 mV/V, while a ~26% reduction is observed in SS for GaAs.

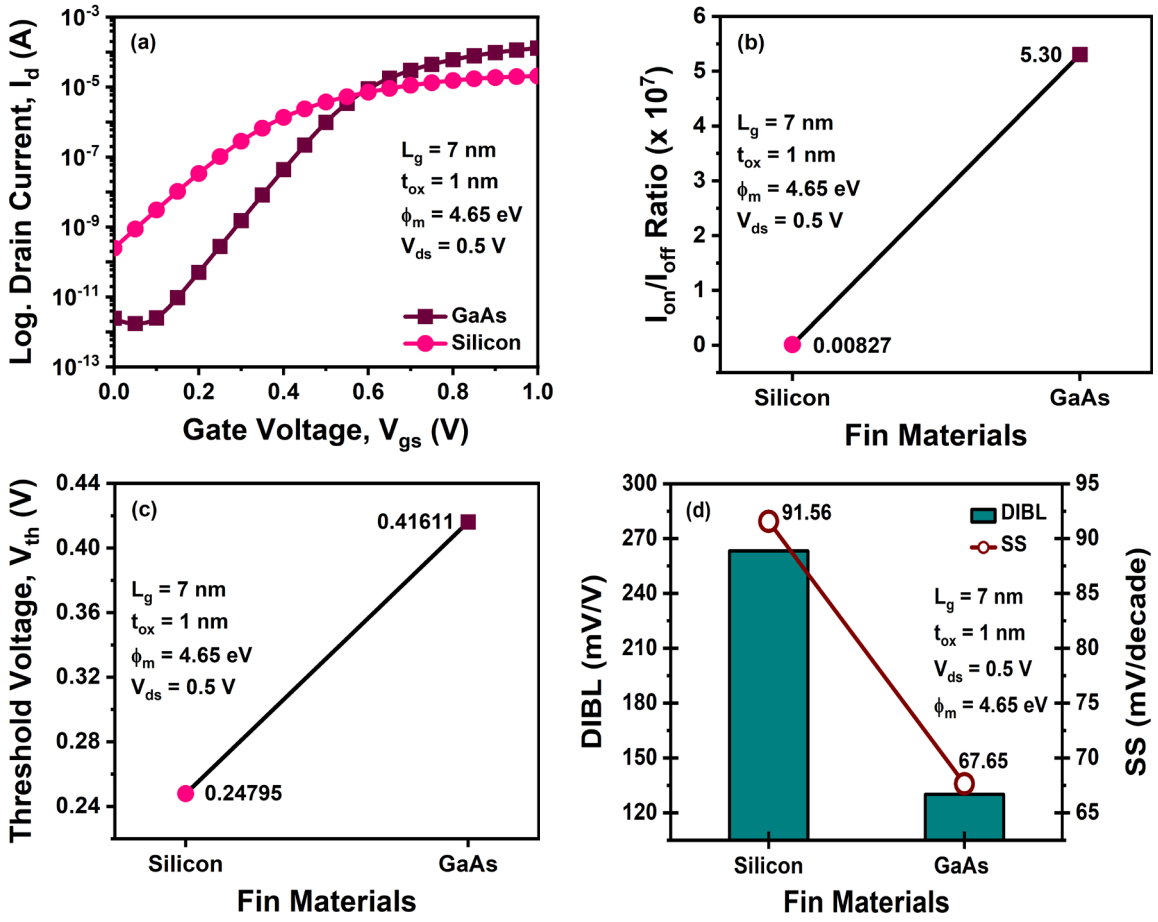

Figure 5.5: Variation in (a) transfer characteristics, (b) switching ratio, (c) threshold voltage, and (d) DIBL and SS for silicon and GaAs JAM-GS-GAA FinFET [3].

Figure 5.6(a) and **Figure 5.6(b)** reflect the variation of parasitic capacitances (C_{gs}, C_{gd}, C_{gg}) against V_{gs} and V_{ds}, respectively. It is observed that the parasitic capacitances increase with the increase in V_{gs} due to the aggregation of charge carriers close to the gate. In contrast, an increase in V_{ds} causes the depletion region around the drain terminal to expand into the channel region. This widening of the depletion region alters the electric field distribution, reducing C_{gs}, C_{gd}, and C_{gg}. Moreover, the parasitic capacitances decrease considerably for GaAs compared to silicon due to its higher energy bandgap. Thus, a higher switching speed is acquired, and therefore, delay time decreases, making GaAs JAM-GS-GAA FinFET a suitable device for ULSI switching applications.

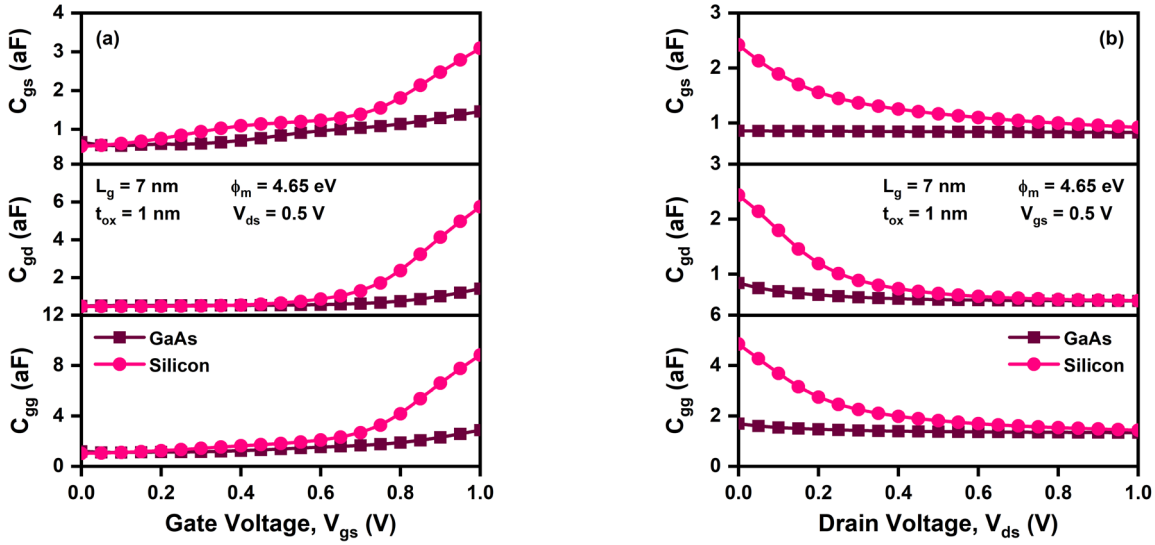

Figure 5.6: Change in parasitic capacitances of silicon and GaAs JAM-GS-GAA FinFET against (a) gate voltage and (b) drain voltage [3].

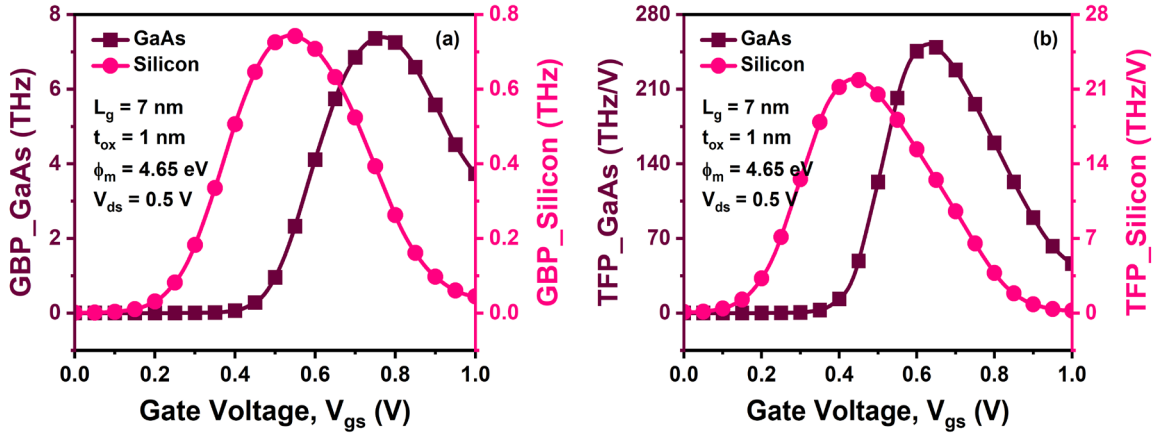

Figure 5.7: Plot of (a) GBP and (b) TFP against V_{gs} for silicon and GaAs JAM-GS-GAA FinFET [3].

The peak value of the gain bandwidth product (GBP) denotes the frequency at which the device acquires maximum gain. **Figure 5.7(a)** outlines the variation of GBP against gate bias for GaAs and silicon, and it is noticed that GaAs exhibit a higher peak value of GBP (7.35 THz) compared to Si (0.74 THz). It is due to the significant improvement in transconductance and drain capacitance. Transconductance frequency product (TFP) is an essential capacitance-dependent FOM. **Figure 5.7(b)** portrays the change in TFP against gate bias for GaAs and silicon. It can be seen that TFP increases with the increase in V_{gs} in the subthreshold region and then achieves a maximum value in

the inversion region. It starts declining due to an increment in C_{gg} with further enhancement in V_{gs}, i.e., in the deep inversion region. Besides, the peak value of TFP improves considerably from 21.84 THz/V to 249.18 THz/V for GaAs due to the parasitic capacitance reduction and transconductance increment. Thus, replacing silicon with GaAs significantly improves the device analog metrics (I_{on}/I_{off} ratio, I_{off}, DIBL, and SS) and capacitance-related parameters (C_{gs}, C_{gd}, C_{gg}, TFP, and GBP), as portrayed in Table 5.1.

Table 5.1: Summary of different analog metrics and parasitic capacitances for silicon and GaAs JAM-GS-GAA FinFET [3].

Parameters	Silicon JAM-GS-GAA FinFET	GaAs JAM-GS-GAA FinFET
I_{off} (A)	2.48×10^{-10}	2.45×10^{-12}
I_{on}/I_{off} ratio	8.27×10^{4}	5.30×10^{7}
DIBL (mV/V)	263.19	130.04
SS (mV/decade)	91.56	67.65
C_{gs} (aF)	3.08	1.45
C_{gd} (aF)	5.74	1.40
C_{gg} (aF)	8.82	2.86
GBP (THz)	0.74	7.35
TFP (THz/V)	21.84	249.18

5.5.2 Impact of Parametric Variations on Parasitic Capacitances

This subsection evaluates the impact of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T on analog metrics and parasitic capacitances of GaAs JAM-GS-GAA FinFET, considering the benefits of GaAs over silicon. Extensive simulations have been run on the GaAs JAM-GS-GAA FinFET device with a range of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T values to accomplish this task. **Figure 5.8(a)** displays the graph of I_{on} current corresponding to the specified values of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T. It has been observed that I_{on} current reduces by 4.59%, 7.78%, 28.64%, and 31.49% when L_g increases from 5 nm to 8 nm, N_{Ch} from 1×10^{16} cm^{-3} to 5×10^{17} cm^{-3}, ϕ_m from

4.55 eV to 4.7 eV, and T from 250 K to 400 K, respectively and by 41.92% when the W_{Fin} is lowered from 7 nm to 4 nm. **Figure 5.8(b)** shows the plot of I_{off} current for the mentioned L_g, N_{Ch}, W_{Fin}, ϕ_m, and T. It is noticed that I_{off} current improves by 84.39%, 37.56%, and 56.59% when L_g increases from 5 nm to 8 nm, N_{Ch} from 1×10^{16} cm^{-3} to 5×10^{17} cm^{-3}, and ϕ_m from 4.55 eV to 4.7 eV, respectively. On the other hand, I_{off} current improves by more than 22 and 11 times when the W_{Fin} is lowered from 7 nm to 4 nm and T is reduced from 400 K to 250 K, respectively. The primary reason for this improvement is that the device has improved electrostatic control over the channel area, decreased quantum mechanical tunneling, mitigated short-channel effects, reduced carrier generation, and carrier mobility by having a longer L_g, greater N_{Ch}, higher ϕ_m, and lower W_{Fin} and T.

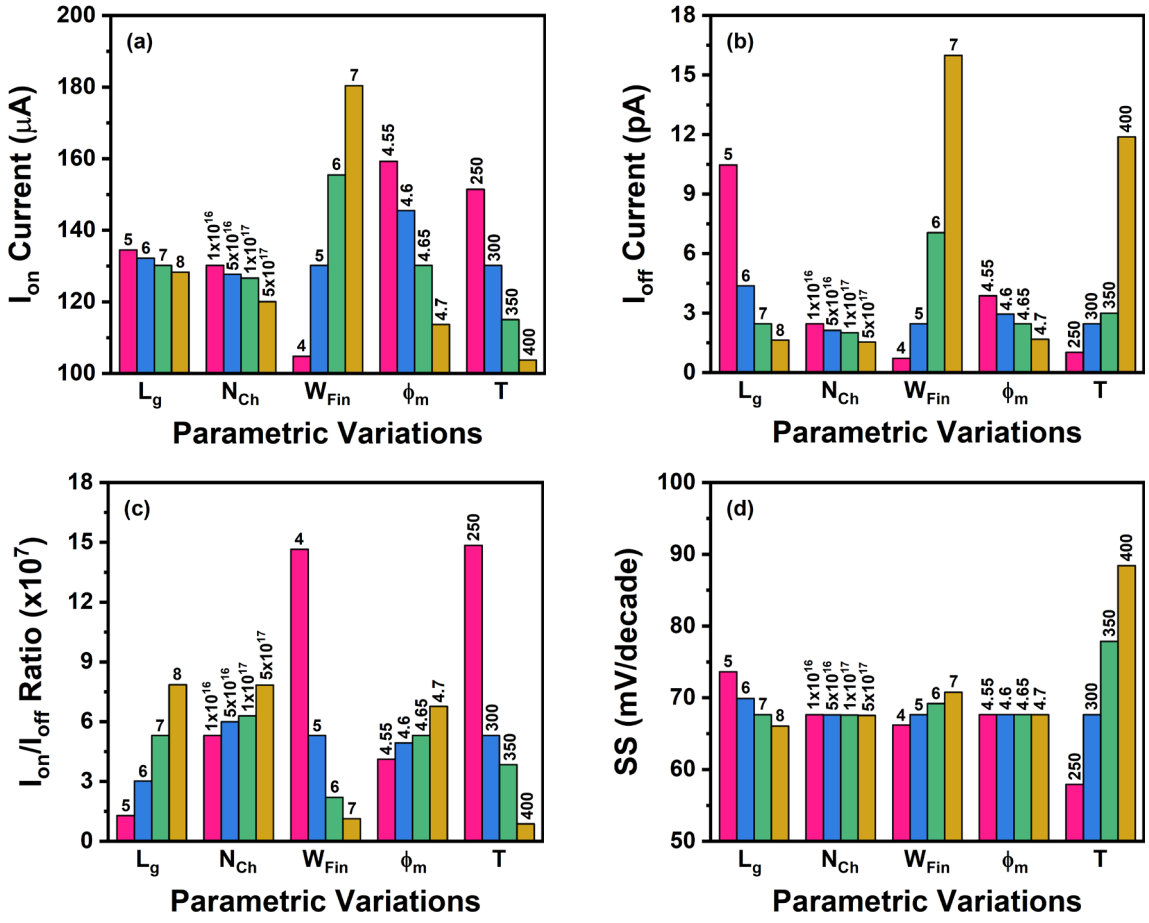

Figure 5.8: Impact of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T on (a) I_{on}, (b) I_{off}, (c) I_{on}/I_{off} ratio, and (d) SS of GaAs JAM-GS-GAA FinFET.

For the given values of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T, the graph of the I_{on}/I_{off} ratio is shown in **Figure 5.8(c)**. The reduction in the I_{off} current is more than the reduction in the I_{on} current for the mentioned parameters, which results in the upgradation of the I_{on}/I_{off} ratio. Consequently, the I_{on}/I_{off} ratio increases by 6 times, 47.69%, 13 times, 64.39%, and 17 times for the variations mentioned in the L_g, N_{Ch}, W_{Fin}, ϕ_m, and T, respectively. **Figure 5.8(d)** portrays the plot of SS concerning the mentioned L_g, N_{Ch}, W_{Fin}, ϕ_m, and T, and it has been observed that SS follows a similar trend to I_{off}. Although the change in the SS for N_{Ch} and ϕ_m alterations is minor, it is considerably more evident in other parameters, with the temperature change showing the most significant variance. Thus, the proposed device with a longer L_g, greater N_{Ch}, higher ϕ_m, and lower W_{Fin} and T exhibits improved electrostatic control over the channel area and mitigated short-channel effects.

Figure 5.9(a) depicts the combined plot of C_{gs}, C_{gd}, and C_{gg} against V_{gs} for different gate lengths. The parasitic capacitances decrease with the decrease in L_g because the overlapping area between the gate electrode and other conductive regions decreases as the L_g decreases. This reduction in overlapping area greatly impacts the total capacitance between these structures, resulting in reduced parasitic capacitance values. The same movement is observed in the previously published results [23, 24]. C_{gs}, C_{gd}, and C_{gg} reduce by 29.45%, 22.23%, and 26.03%, respectively, with the shrinking of L_g from 10 nm to 5 nm. The collaborated plot of C_{gs}, C_{gd}, and C_{gg} versus V_{gs} for various channel dopings is shown in **Figure 5.9(b)**. When the N_{Ch} is reduced from 1×10^{18} cm^{-3} to 1×10^{16} cm^{-3}, the parasitic capacitances see a corresponding drop because a drop in the N_{Ch} corresponds to a decrease in the number of charge carriers, reducing the total charge density inside the channel area. Consequently, a lower charge density leads to less charge separation between the channel and adjacent regions, ultimately causing a fall in parasitic capacitances.

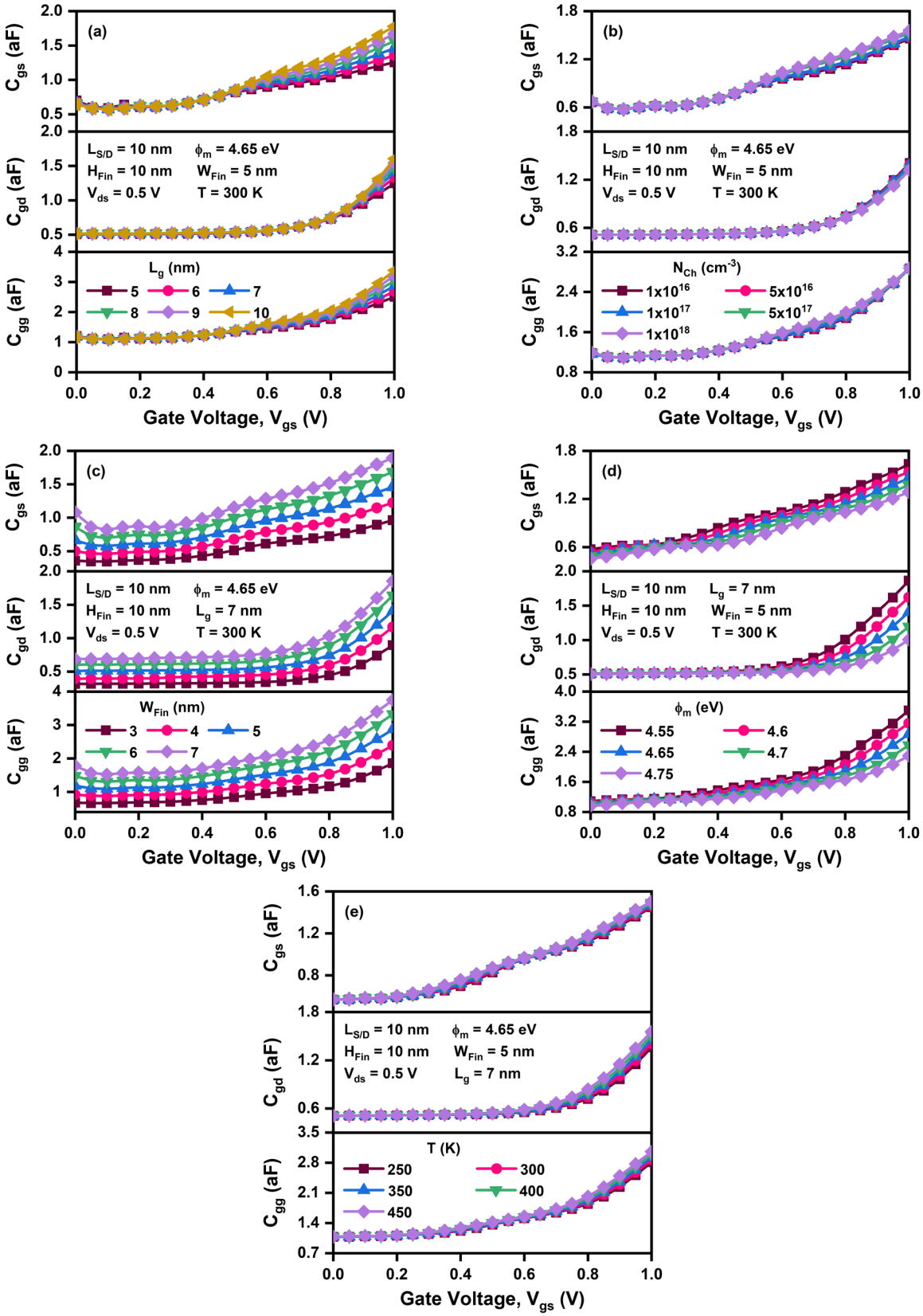

Figure 5.9: Change in parasitic capacitances for different (a) L_g, (b) N_{Ch}, (c) W_{Fin}, (d) ϕ_m, and (e) T against V_{gs}.

Figure 5.9(c) outlines the variation of parasitic capacitances against V_{gs} for different fin widths. Parasitic capacitances are observed to decrease significantly with the decrease in the W_{Fin}. The overlap region between the gate and the fin shrinks as the W_{Fin} diminishes. Because the capacitance is directly proportional to the area of overlap between conducting structures, this reduced overlapping area immediately lowers the parasitic capacitance. The shrinking of W_{Fin} from 7 nm to 3 nm leads to a reduction of 49.13%, 51.66%, and 50.38% in C_{gs}, C_{gd}, and C_{gg}, respectively. For different gate electrode work functions, C_{gs}, C_{gd}, and C_{gg} are all shown together against V_{gs} in **Figure 5.9(d)**. The rise in the ϕ_m from 4.55 eV to 4.75 eV reduces the parasitic capacitances because the augmentation of the ϕ_m induces changes in the distribution of charge, electric field, and surface potential inside the device. These modifications collectively reduce the C_{gs} by 21.28%, C_{gd} by 45.96%, and C_{gg} by 34.42%, respectively. **Figure 5.9(e)** outlines the variation of parasitic capacitances against V_{gs} for different temperatures. Parasitic capacitances decrease with the decrease in the T from 400 K to 250 K. Changes in the dielectric characteristics of materials, charge carrier mobility, and charge distribution at lower temperatures are the primary causes of this parasitic capacitance decrease.

The impact of L_g, N_{Ch}, W_{Fin}, ϕ_m, and T on parasitic capacitances of GaAs JAM-GS-GAA FinFET against V_{ds} is also demonstrated. **Figure 5.10(a)** depicts the combined plot of C_{gs}, C_{gd}, and C_{gg} against V_{ds} for different gate lengths. The parasitic capacitances decrease with the decrease in gate length. C_{gs}, C_{gd}, and C_{gg} reduce by 6.78%, 1.89%, and 4.94%, respectively, with the shrinking of L_g from 10 nm to 5 nm. The collaborated plot of C_{gs}, C_{gd}, and C_{gg} versus V_{ds} for various channel dopings is shown in **Figure 5.10(b)**. When the N_{Ch} is reduced from 1×10^{18} cm^{-3} to 1×10^{16} cm^{-3}, the parasitic capacitances see a corresponding drop.

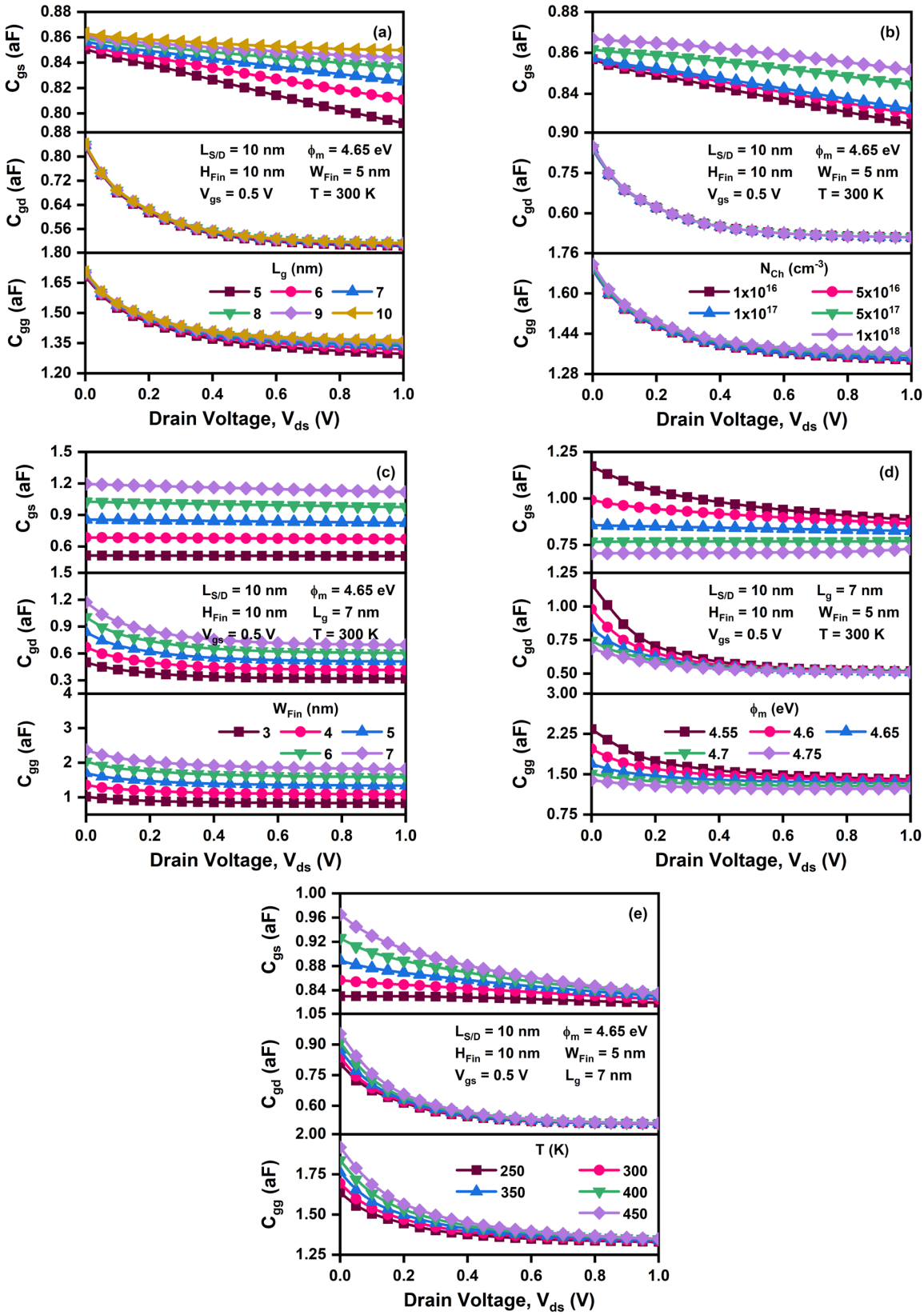

Figure 5.10: Change in parasitic capacitances for different (a) L_g, (b) N_{Ch}, (c) W_{Fin}, (d) ϕ_m, and (e) T against V_{ds}.

Figure 5.10(c) outlines the variation of parasitic capacitances against V_{ds} for different fin widths. Parasitic capacitances are observed to decrease significantly with the decrease in the W_{Fin}. The shrinking of W_{Fin} from 7 nm to 3 nm leads to a reduction of 54.41%, 54.33%, and 54.38% in C_{gs}, C_{gd}, and C_{gg}, respectively. For different gate electrode work functions, C_{gs}, C_{gd}, and C_{gg} are all shown together against V_{ds} in **Figure 5.10(d)**. The rise in the ϕ_m from 4.55 eV to 4.75 eV reduces the C_{gs} by 17.61%, C_{gd} by 1.59%, and C_{gg} by 11.69%, respectively. **Figure 5.10(e)** outlines the variation of parasitic capacitances against V_{ds} for different temperatures. Parasitic capacitances decrease with the decrease in the T from 400 K to 250 K. The reduction in T from 400 K to 250 K leads to an improvement of 1.82%, 0.76%, and 1.42% in C_{gs}, C_{gd}, and C_{gg}, respectively. Thus, parasitic capacitances decrease appreciably for the proposed device with a shorter L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m, and the proposed device with mentioned specifications can be considered a suitable candidate for low-power ULSI switching applications.

5.5.3 Impact of Parametric Variations on Small-Signal Behavior

In this subsection, the small-signal behavior of the GaAs JAM-GS-GAA FinFET has been examined by looking at the S-parameters in real forms. S_{11} and S_{22} are the input and output reflection coefficients, whereas S_{12} and S_{21} are the reverse and forward transmission coefficients. S_{11} and S_{22} quantify the degree to which a port's impedance matches the terminating load [13]. When describing the high-frequency small-signal behavior of an active device, S_{11} is the most popular parameter to utilize. In most RF circuits, matching is essential. The reflection coefficient is zero at a perfect match, and no waves are reflected. S_{12} specifies the amount of transmission of information from the output port 2 to the input port 1, whereas S_{21} specifies the amount of information sent from the input port 1 to the

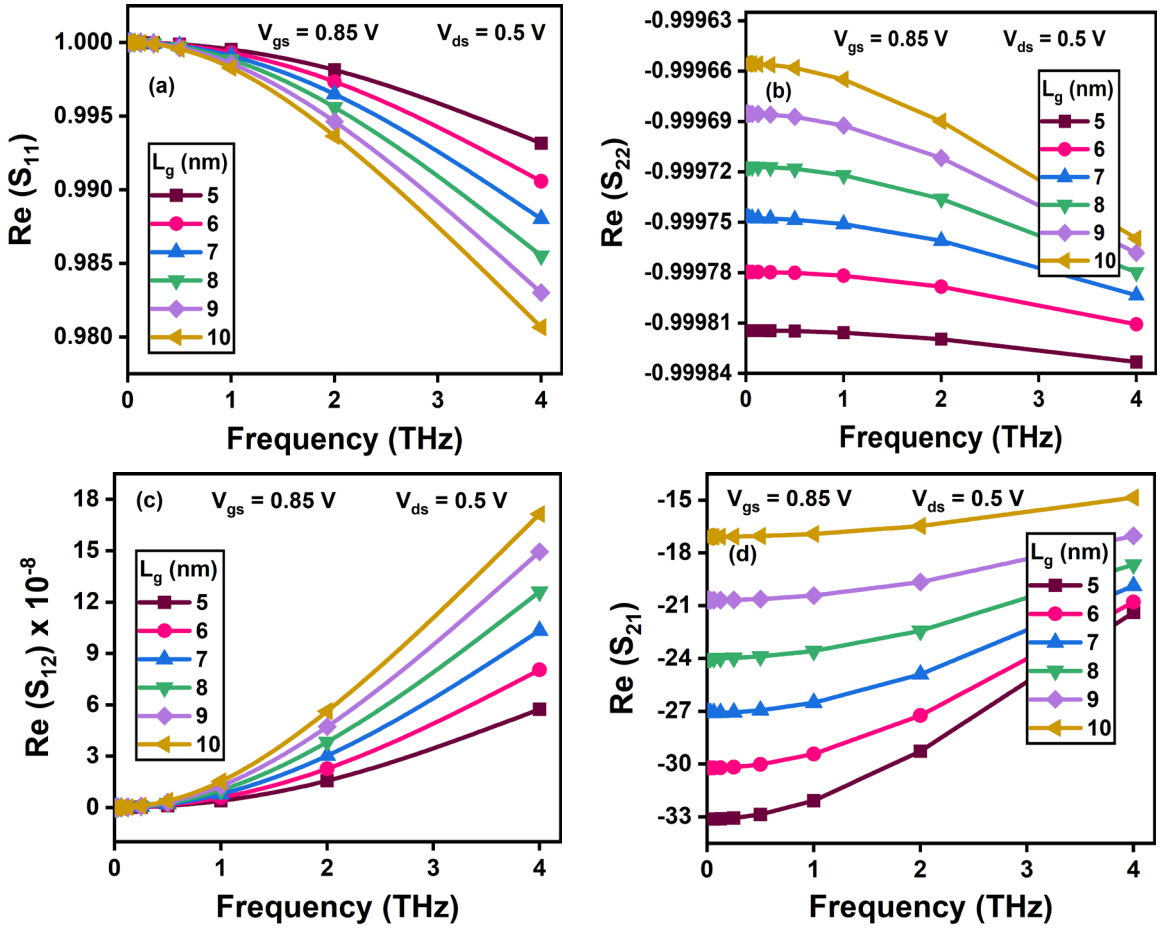

Figure 5.11: Variations of (a) S_{11}, (b) S_{22}, (c) S_{12}, and (d) S_{21} of the GaAs JAM-GS-GAA FinFET at THz frequencies for different gate lengths [14].

output port 2 [15]. The high-frequency stability of an amplifier is determined by the value of S_{12}, while S_{21} is also known as the forward gain of a two-port device.

The S-parameters of the GaAs JAM-GS-GAA FinFET have been examined at THz frequencies with gate lengths going from 5 nm to 10 nm. The fluctuations of S_{11}, S_{22}, S_{12}, and S_{21} for mentioned L_g as a function of frequency are shown in **Figure 5.11(a-d)**. It is observed that S_{11} and S_{22} at ports 1 and 2 improve when the L_g is enhanced. S_{12} increases and moves toward a more positive value, and S_{21} also increases with the rise in L_g because increasing the L_g causes a surge in the drain current, which leads to a larger transconductance and, consequently, improved reflection and transmission coefficients.

The S-parameters of the GaAs JAM-GS-GAA FinFET have been examined at THz frequencies for the mentioned channel dopings for high-frequency performance. **Figure 5.12(a-d)** displays the variations of S_{11}, S_{22}, S_{12}, and S_{21} as a function of N_{Ch} at the THz frequency range. It can be seen that reduced N_{Ch} produces an improved S_{11} and S_{22} and a higher S_{12} and S_{21}. Because as the channel doping of the GaAs JAM-GS-GAA FinFET is reduced, the inversion charge density is enhanced, leading to a decrease in the threshold voltage and, consequently, an improvement in the on-state current. The rise in on-state current causes a corresponding rise in the transconductance, which in turn causes an improvement in the reflection and transmission coefficients.

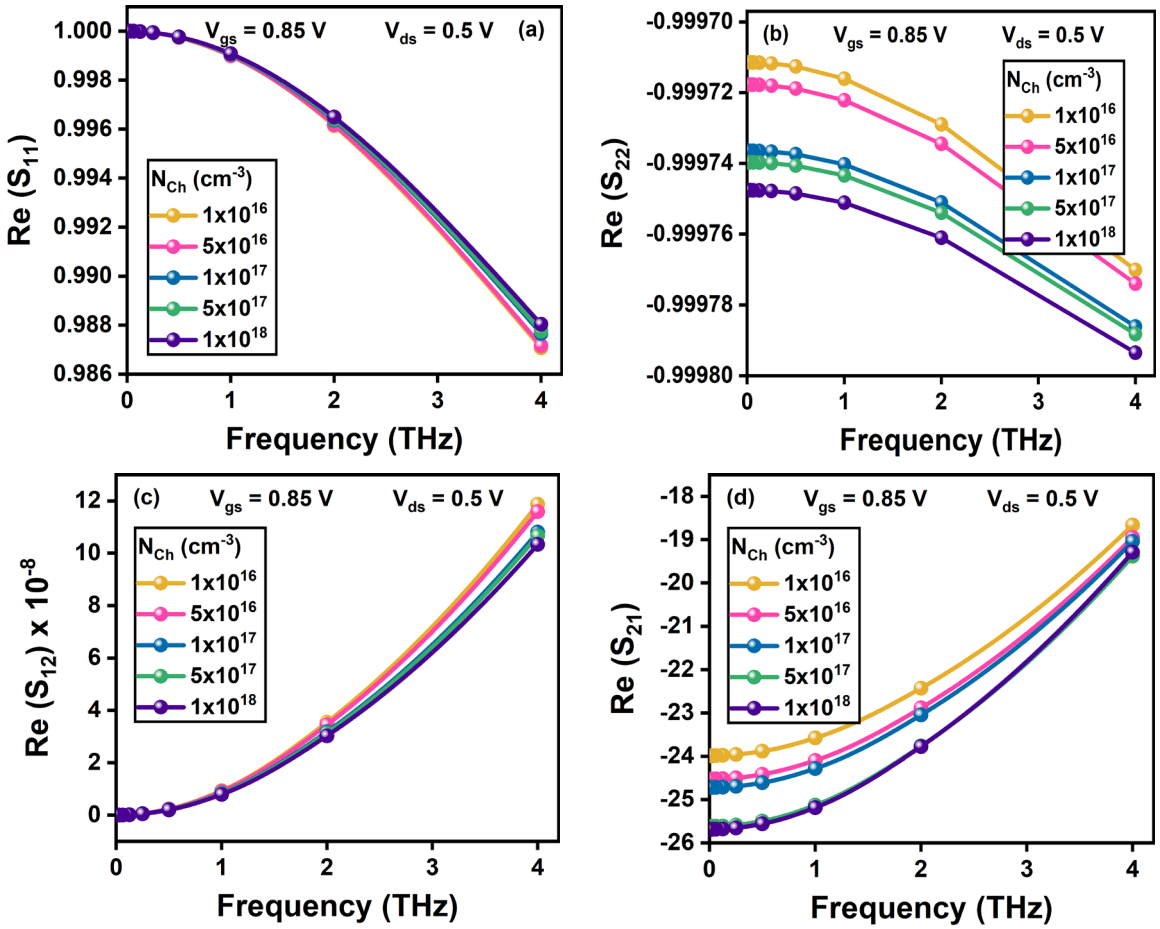

Figure 5.12: Variations of (a) S_{11}, (b) S_{22}, (c) S_{12}, and (d) S_{21} of the GaAs JAM-GS-GAA FinFET at THz frequencies for different channel dopings [14].

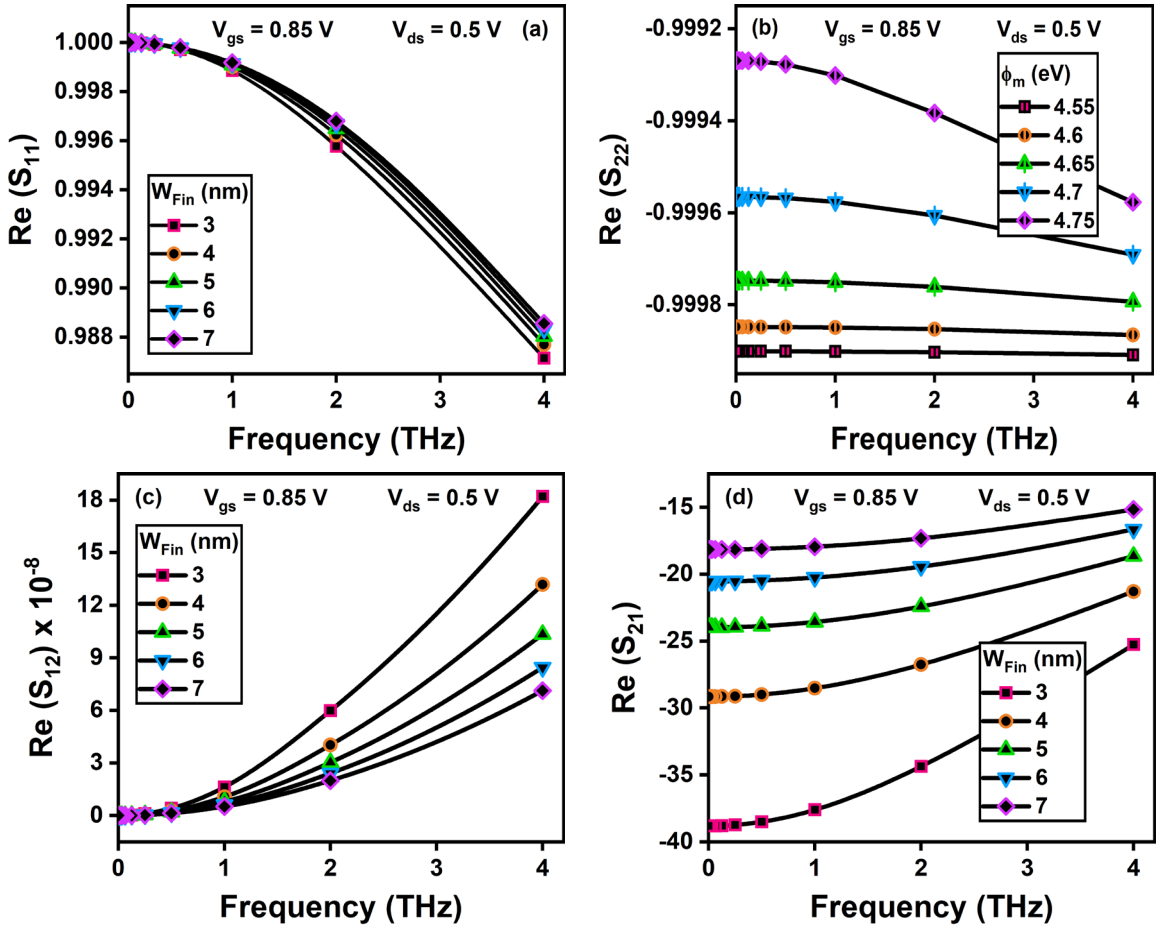

Figure 5.13: Variations of (a) S_{11}, (b) S_{22}, (c) S_{12}, and (d) S_{21} of the GaAs JAM-GS-GAA FinFET at THz frequencies for different fin widths [12].

Figure 5.13(a-d) depicts the S_{11}, S_{22}, S_{12}, and S_{21} variations at THz frequencies with fin widths ranging from 3 nm to 7 nm. Reducing W_{Fin} reduces the reflection and enhances the transmission coefficients because a gate with a narrower fin width imparts a stronger electrostatic influence on the channel due to the increased proximity between the gate and the channel region. This improved control permits the gate voltage to exert a greater influence on the channel, resulting in increased transconductance and improved reflection and transmission coefficients. Changing the gate electrode work function from 4.55 eV to 4.75 eV in **Figure 5.14(a-d)** shows how the S_{11}, S_{22}, S_{12}, and S_{21} change at THz frequencies. The S_{11}, S_{22}, S_{12}, and S_{21} improve with the rise in the ϕ_m because a greater ϕ_m

reduces the impact of short-channel effects and increases the extent to which the gate exerts electrostatic control over the channel area. This ultimately leads to improvements in transconductance and the reflection and transmission coefficients. The shifts in S_{11}, S_{22}, S_{12}, and S_{21} at THz frequencies for various temperatures are shown in **Figure 5.15(a-d)**. The reflection and transmission coefficients improve with the reduction in T due to the enhanced transconductance. Thus, at extremely high frequencies, the proposed device GaAs JAM-GS-GAA FinFET may be utilized as a microwave oscillator and amplifier with an appropriate adjustment in gate length, channel doping concentration, fin width, gate electrode work function, and temperature.

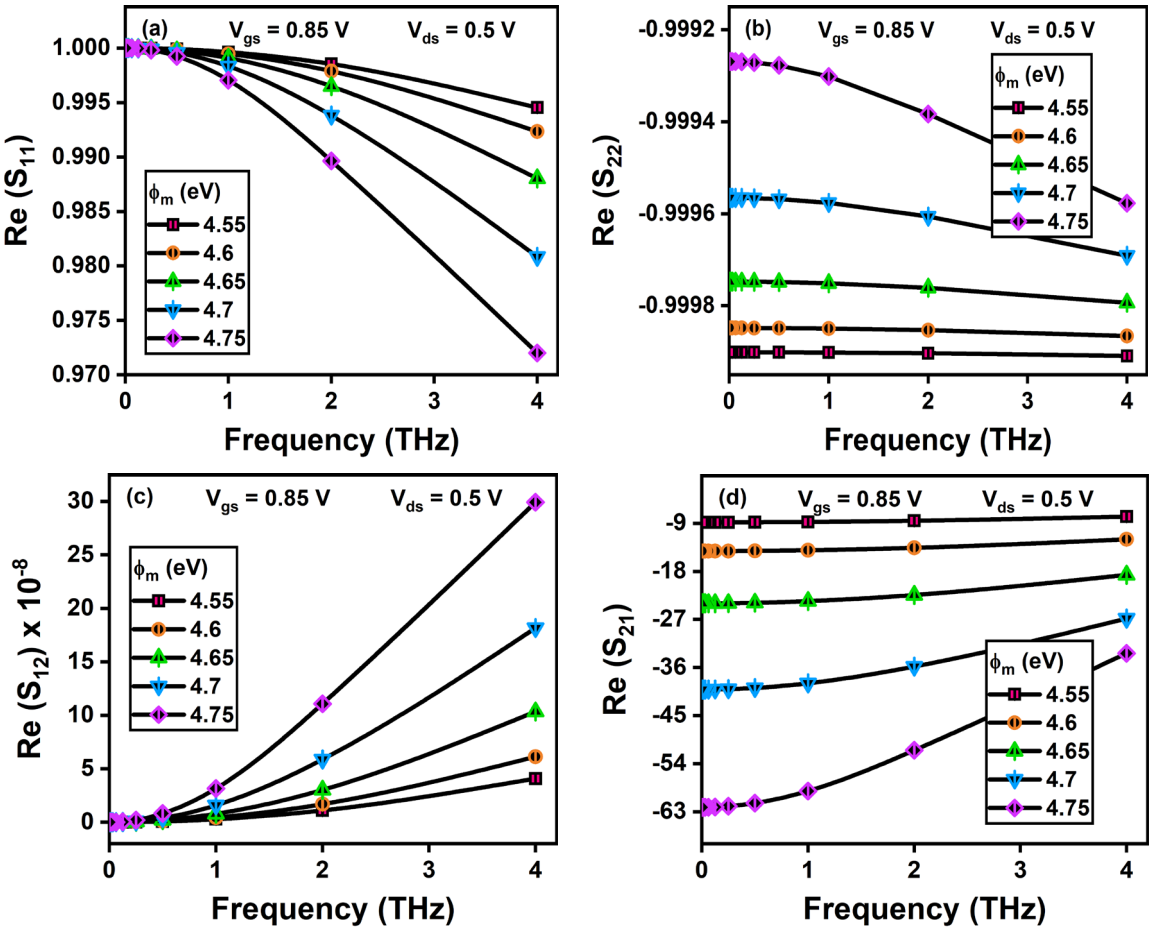

Figure 5.14: Variations of (a) S_{11}, (b) S_{22}, (c) S_{12}, and (d) S_{21} of the GaAs JAM-GS-GAA FinFET at THz frequencies for different gate electrode work functions [12].

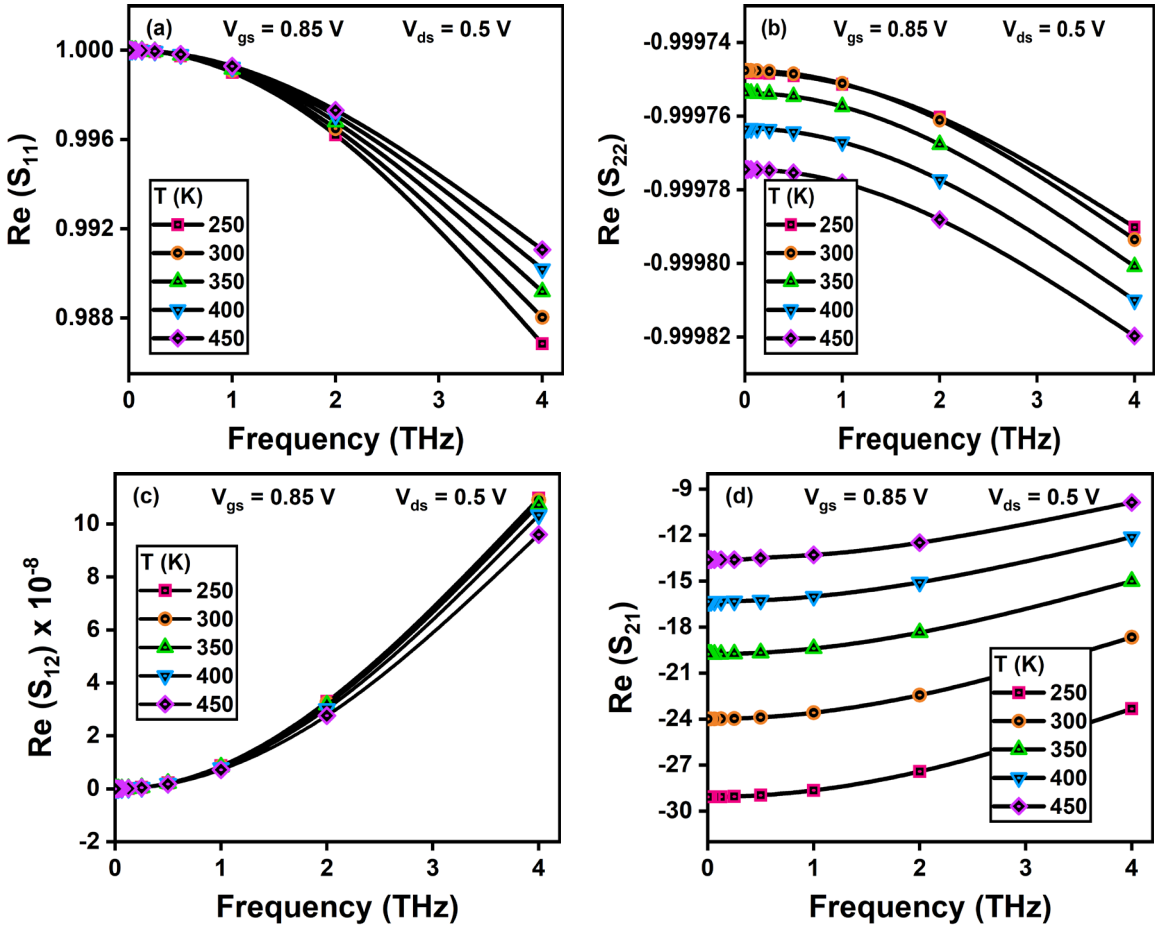

Figure 5.15: Variations of (a) S_{11}, (b) S_{22}, (c) S_{12}, and (d) S_{21} of the GaAs JAM-GS-GAA FinFET at THz frequencies for different temperatures [12].

5.6 SUMMARY

This chapter explores the parasitic capacitances and small-signal behavior of JAM-GS-GAA FinFET with GaAs as a fin material. Capacitance-related FOMs like GBP and TFP are also analyzed for switching applications. It is noticed from the results that the use of GaAs as a fin material significantly reduces the SCEs and parasitics capacitances of the device. Compared to silicon, the I_{off} current reduces approximately 100 times, the I_{on}/I_{off} ratio increases by ~10^3 times, DIBL becomes half, and SS decreases by ~26% for GaAs. The parasitic capacitances follow the same trend: C_{gs} reduced by 52.71%, C_{gd} by 75.48%, and C_{gg} by 67.52% with the incorporation of GaAs. Due to this considerable decrease in

the parasitic capacitances, the peak value of both GBP and TFP increases by 10 times. Further, the effect that parameters like L_g, N_{Ch}, W_{Fin}, ϕ_m, and T have on the parasitic capacitances and S-parameters of GaAs JAM-GS-GAA FinFET are examined. Parasitic capacitances are found to decrease appreciably for the proposed device with a shorter L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m, whereas, at extremely high frequencies, the S-parameters improve considerably for the proposed device with a larger L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m. Thus, the proposed device with mentioned specifications can be considered suitable for both low-power ULSI switching applications and microwave oscillators and amplifiers by striking a balance of gate length.

After discussing the parasitic capacitances and small-signal behavior of the proposed device, the next chapter of this thesis focuses on the real-time application of GaAs JAM-GS-GAA FinFET. Hence, the capability of the proposed device to accomplish the electrical identification of the breast cancer cell MDA-MB-231 with high sensitivity by monitoring the device switching ratio is explored for use in bio-medical diagnosis.

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6

CHAPTER

Switching Ratio-Based Sensitivity Analysis of GaAs JAM-GS-GAA FinFET for MDA-MB-231 Breast Cancer Cells Detection

- *This chapter describes the utilization of GaAs JAM-GS-GAA FinFET to accomplish the electrical identification of the breast cancer cell MDA-MB-231 by monitoring the device switching ratio.*
- *The sensor measures the switching ratio-based sensitivity and comes out to be 99.72% for MDA-MB-231 (cancerous) and 47.78% for MCF-10A (healthy) breast cells. The sensor was tested for stability and reproducibility and found to be repeatable and sufficiently stable with a settling time of 55.51 ps, 60.80 ps, and 71.58 ps for the MDA-MB-231, MCF-10A cell, and air, respectively.*
- *Based on electrical response alterations, the sensor can distinguish between viable and non-viable cells. The possibility of early detection of cancerous breast cells using Bruggeman's model is also discussed. This chapter also explains how to maximize the sensing performance by adjusting the biomolecule occupancy, frequency, and various device's physical parameters.*
- *The proposed breast cancer cell sensor is compared to existing breast cancer cell sensors and shows considerable improvement.*
- *Consequently, GaAs JAM-GS-GAA FinFET has the potential to emerge as a promising contender for detecting MDA-MB-231 breast cancer cells.*

6.1 INTRODUCTION

Chapter 5 extensively investigates the parasitic capacitances and small-signal behavior of the proposed device. Now, the objective is to identify the MDA-MB-231 breast cancer cells electrically using the GaAs JAM-GS-GAA FinFET with high sensitivity for use in medical diagnosis. Cancer is not an infectious illness; instead, it is caused by a malfunction in the DNA of a cell or tissue [1]. These cells do not perform their usual functions but rather proliferate and replicate in an uncontrolled manner, resulting in the formation of a tumor. In 2020, according to WHO fact sheets, cancer was the leading cause of mortality worldwide, accounting for around 10 million deaths, or almost one in every six, with breast cancer (2.26 million cases) as the most prevalent cancer [2]. The formation of malignant tumors in women's breasts is the primary cause of breast cancer, and the lifetime chance of developing it is 12%. The most common cancerous breast cells are MDA-MB-231, MCF-7, T47D, and Hs578t, while MCF-10A is a healthy nontumorigenic breast cell [1]. Compared to MCF-7 and T47D, Hs578t and MDA-MB-231 cells are the most invasive. Since invasive breast cancer cells are so dangerous and may spread rapidly, diagnosis at an early stage is important. Early diagnosis may aid in more effective disease management, and more than 70% of cases are expected to be cured with early detection [3, 4].

Cell isolation separates one or more cell populations from a heterogeneous mixture of cells. Targeted cells are separated and sorted by kind. Many cell isolation techniques are available depending on the separated cells, with a few significant ones covered in this chapter, each with pros and cons. The computer-controlled micropipette (CCMP) method uses a small glass or quartz micropipette with a fine tip that a computer can control to precisely separate cells. CCMP involves manipulating a micropipette towards a suspended

cell and applying a tiny suction pressure to partly aspirate the cell within the micropipette. As suction pressure rises, the cell deforms and flows into the micropipette. Researchers have widely employed this approach to explore the adhesion force measurements [5] and mechanical characteristics of diverse cells [6]. Fluorescence-activated cell sorting (FACS) is a flow cytometry method that uses fluorescence characteristics to separate cells. FACS begins with labeling cells with fluorescent dyes that attach to specific cell surface markers. In front of a laser, the suspended cells are passed in a stream of droplets, each containing a single cell. This stream is then directed via a series of lasers, which activate the cell-bound fluorophores, resulting in light scattering and fluorescent emissions. The fluorescence detecting system recognizes cells of interest based on the wavelengths generated by the laser excitation. Due to its wide application, FACS research includes bacteria [7], protoplasts [8], bone marrow cells [9], etc. Microfluidics is a cell separation technique that uses fluid manipulation on a microscopic scale. Cell isolation approaches based on microfluidics vary depending on their size, density, compressibility, electrical and magnetic characteristics, etc. The membrane filtering technique uses thin membrane layers with micro-pores to detect and isolate cells based on their size [10]. Cells of different densities and compressibilities may be separated using acoustic waves in a process called acoustophoresis [11]. In dielectrophoresis, non-uniform electric fields separate and isolate cells based on their dielectric properties [12]. Cells that contain magnetic nanoparticles may be identified and separated via magnetic cell sorting [13]. Laser microdissection is a high-resolution technique for isolating cells from their surrounding tissues that employ a laser beam and direct microscopic visualization. The sample is mounted on a microscope slide, and an infrared or ultraviolet laser selectively cuts off the cells of interest. This technique has been extensively used in liver illnesses [14], mass spectrometry [15], etc.

X-ray mammography, sonography, and magnetic resonance imaging (MRI) scans are some screening methods for breast cancer identification. Currently, x-ray mammography is the predominant method for breast cancer detection. Although this technology has made significant strides in this sector, there have been reports of many drawbacks [16, 17]. In addition, x-ray mammography's specificity and sensitivity drastically decrease to 89% and 67% for dense breasts, and the method also includes radiation exposure dangers [18]. While sonography may be a cost-effective tool in the fight against breast cancer, the accuracy of a diagnosis relies on the experience of the person doing the procedure, and hence, it may provide erroneous findings at times [19]. MRIs with improved contrast have a higher sensitivity (93-100%) [20], but they are difficult to use, costly, and limited to hospital use.

The microwave imaging technique was created to overcome the drawbacks of conventional imaging. This method uses the large dielectric difference between healthy and cancerous tissue to perform microwave imaging and heating [21, 22]. Scientists have been interested in how different types of malignant cells behave and may be detected when exposed to microwave frequencies [23]. Kim et al. calculated the dielectric characteristics of fatty glandular, fibro, and malignant breast tissues from 50 MHz to 5 GHz frequency [24]. It was noted that the dispersion of malignant tissues differs from that of healthy breast tissue. In the frequency range of 50-900 MHz, Joines et al. investigated the dielectric characteristics of human tissues and found that cancerous tissues have greater conductivity and permittivity than normal tissues [25]. Many investigations have been conducted to know the dielectric characteristics of various human body components, such as the liver [26]. The dielectric characteristics of numerous in vitro breast malignant cell lines between 200 MHz and 13.6 GHz have been examined by Hussein et al. [1]. It was found that breast

cancer cells, because of their high water content, exhibit varying dielectric characteristics, leading to enhanced scattering at microwave frequencies.

Compared to imaging methods, molecular biotechnology tests may detect breast cancer sooner. However, they cannot substitute imaging techniques but complement imaging methods for diagnosing breast cancer. Molecular biotechnology examines biomarkers like nucleic acid, proteins, cells, and tissues of patients. Effective molecular biotechnology examination tools utilized for identifying breast cancer cells include quantitative polymerase chain reaction (qPCR), mass spectrometry (MS), single-cell resonant waveguide gratings (SCRWGs), digital holographic microscopy (DHM), etc. The qPCR, or real-time PCR, quantifies DNA and gene expression levels in samples. qPCR has been used to assess circulating tumor cells in many solid tumors, such as breast cancer [27]. The qPCR technology may guide breast cancer therapy by monitoring mRNA expression [28]. Matrix-assisted laser desorption/ionization (MALDI) mass spectrometry imaging (MSI) [29], surface-enhanced laser desorption/ionization (SELDI) MS [30], and liquid chromatography-tandem mass spectrometry (LC-MS/MS) [31] are some of the MS-based techniques utilized for breast cancer diagnosis. The concentration of adhesion proteins inside the cell-substrate contact zone causes a change in the refractive index, which may be monitored in real time using SCRWGs. The SCRWGs technology was used to monitor the adhesion of HeLa cancer cells [32]. DHM technology provides high-resolution three-dimensional (3D) imaging of transparent biological specimens such as live cells and tissues. DHM may be utilized to capture digital holograms of breast tissues and analyze their malignancy using a deep learning approach [33]. Each technique has pros and cons, depending on the nature of the investigated molecules.

Microelectromechanical systems (MEMS) based sensors [34], fiber Bragg grating (FBG) [35], and optical sensors [36] have also played significant roles in identifying breast cancer cells. However, FET-based devices have recently attracted attention in biosensing applications for their many benefits, including small size, low cost, high sensitivity, suitability for CMOS technology, controllable electrical response, and reproducibility [37]. TFETs [38], HEMTs [39], and FinFETs [40] have been used in the past in breast cancer diagnosis. Previous chapters have showcased that the proposed device demonstrates superior performance compared to planar devices and optimizes the short-channel effects (SCEs). Thus, the GaAs JAM-GS-GAA FinFET device is used to identify breast cancer cells based on their dielectric constant value. The proposed device employs a GAA design that encloses the gate on all four sides; consequently, four nanocavities are carved beneath the gate electrodes toward the source area for enhanced detection sensitivity. The presence or absence of breast cancer cells affects the dielectric constant of the cavity area. The change in the dielectric constant alters the device's electrical properties, which may then be utilized to identify the presence of sickness in the body. MCF-10A and MDA-MB-231 breast cells were chosen for examination and may be produced by the procedure described by Hussein et al. [1].

Simulations were run to test the device sensitivity regarding switching ratio by analyzing the drain current characteristics for air (cell-free), MCF-10A, and MDA-MB-231 cells. The efficiency of any given sensor is directly proportional to the degree to which it can be recognized with a high level of accuracy or precision. Therefore, Equation (6.1) is utilized to calculate the switching ratio-based sensitivity (S_{SR}) [41]:

$$S_{SR}(\%) = \left|(SR_{(air)} - SR_{(healthy/cancerous\ cell)})/SR_{(air)}\right| \times 100 \quad (6.1)$$

Further, the healthy and malignant breast cells were taken together in various concentrations, and an investigation was carried out to identify an MDA-MB-231 infection, even in small amounts. When breast cancerous and healthy cells are combined in different concentrations, the effective dielectric constant (ε_{eff}) is determined using the formulas from Bruggeman's model [42].

$$\varepsilon_{eff} = (H_b + \sqrt{H_b^2 + 8\varepsilon_c\varepsilon_h}\,)/4 \text{ where } H_b = (2 - 3C_m)\varepsilon_c - (1 - 3C_m)\varepsilon_h \quad (6.2)$$

where ε_c and ε_h are the dielectric constants of cancerous and healthy cells, and C_m represents the healthy cell fractional volume. Next, the effect of biomolecule occupancy on the device's sensitivity is explored. In biomolecule detection, it is assumed that the cavity area has been completely filled. However, during biomolecule immobilization, the target biomolecule only fills a portion of the cavity areas, leaving some empty space, which can change the proposed device's electrical performance for different target biomolecules. Thus, there is a need to consider the biomolecule occupancy factor (γ_{Bio}) as it can potentially affect the sensitivity of the sensor. γ_{Bio} is defined as follows [38]:

$$\gamma_{Bio}(\%) = (\text{Thickness of cavity filled} / \text{Total thickness of the cavity}) \times 100 \quad (6.3)$$

This chapter also investigates how changes to the frequency and the device's physical parameters influence the device's sensitivity. Based on the findings, optimal device settings for maximizing sensitivity may be selected. Finally, the effectiveness of the proposed breast cancer cell detector is compared to that of already existing breast cancer detectors. The remainder of the chapter is: Section 2 covers device structure and physical models. Sections 3 and 4 discuss the experimental calibration and device operation for breast cancer detection. Section 5 and Section 6 analyze and summarize the findings and the implications of this analysis.

6.2 DEVICE DESIGN AND PHYSICAL MODELS

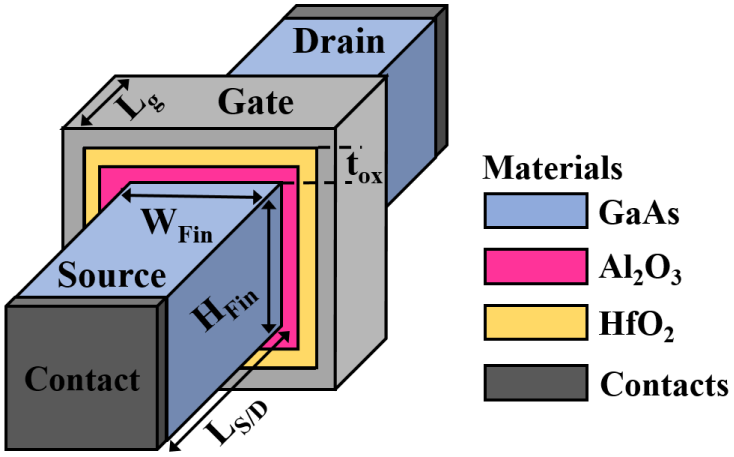

Figure 6.1: Symmetric 3D view of the GaAs JAM-GS-GAA FinFET [41].

Figure 6.1 illustrates the symmetric 3D view of the GaAs JAM-GS-GAA FinFET. Table 6.1 contains detailed descriptions of the device's structural parameters. The fin area is made of GaAs material. The simulations adhere to the width quantization property by keeping fin width (W_{Fin}) at a constant proportional multiple of fin height (H_{Fin}) [43]. In FinFET devices, it is recommended that the W_{Fin} should be less than one-third of the gate length (L_g) and H_{Fin} should be in the 0.6 L_g to 0.8 L_g range to minimize the SCEs [44, 45]. The recommendations were considered during the device dimension consideration. The gate oxide has a combination of coatings of Al_2O_3 and HfO_2. All sections are uniformly n-type doped with lower channel doping than the source/drain doping to lessen the parasitic capacitance. At 200 MHz frequency, the dielectric constants (k) for MCF-10A and MDA-MB-231 are 4.33 and 24.50, respectively, while at 13.6 GHz, they drop to 2.76 and 16.65 [1]. For air, which does not have any cells, k is 1. To obtain the transient analysis, TSTOP is set at 10^{-9} s, TSTEP is 10^{-12} s, RAMPTIME is 5×10^{-11} s, and V_{gs} is 1.5 V. TSTOP is the time that solutions will stop, TSTEP specifies the initial step size, and the RAMPTIME specifies the time duration over which the voltage or current are ramped up or down.

The GaAs JAM-GS-GAA FinFET structure was simulated using the SILVACO-Atlas 3D simulator [46]. The Poisson and Continuity equations are frequently used in the device simulation, but additional equations and models are also needed to improve device simulation results. As a result, the simulations include a wide variety of physical models. Quantum confinement effects are an essential design consideration for rapidly scalable devices. To consider the consequences of quantum confinement, the Bohm Quantum Potential (BQP) model uses a position-dependent quantum potential (Q) [47]. Fermi-Dirac statistics, Crowell-Sze impact ionization, concentration-dependent mobility, Klaassen tunneling, SRH recombination, and bandgap narrowing are the other standard models that have been incorporated [46]. Additionally, drain current characteristics are simulated using Newton and Block iteration methods for breast cancer cell identification.

Table 6.1: Different simulation parameters and their values [41].

Parameters	**Symbol**	**Value**	**Unit**
Source/Drain Length	$L_{S/D}$	50	nm
Gate Length	L_g	50	nm
Cavity Length	C_L	25	nm
Cavity Height	C_H	3	nm
Oxide Thickness	t_{ox}	3	nm
Fin Height	H_{Fin}	30	nm
Fin Width	W_{Fin}	15	nm
Gate Thickness	G_t	5	nm
Channel Doping	N_{Ch}	1×10^{16}	cm^{-3}
Source/Drain Doping	$N_{S/D}$	5×10^{18}	cm^{-3}
Gate Electrode Work Function	ϕ_m	4.65	eV
Temperature	T	300	K
Gate-Source Voltage	V_{gs}	1.5	V
Drain-Source Voltage	V_{ds}	0.5	V

6.3 EXPERIMENTAL CALIBRATION

The findings published by Ye et al. [48] are used to verify the simulation models discussed before. The output characteristics of an Al_2O_3/GaAs MOSFET operated with V_{gs} = -0.5 V and V_{gs} = -1.0 V are revealed in **Figure 6.2**, along with the experimental and simulated results. The fact that the data sets obtained via simulation and experiment are comparable adds credibility to the simulation models chosen. The steps in creating the proposed GaAs JAM-GS-GAA FinFET device were thoroughly covered in **Chapter 5**, including a flowchart illustrating the whole process. Moreover, the cavity region can be created by dry etching the gate dielectric toward the source area.

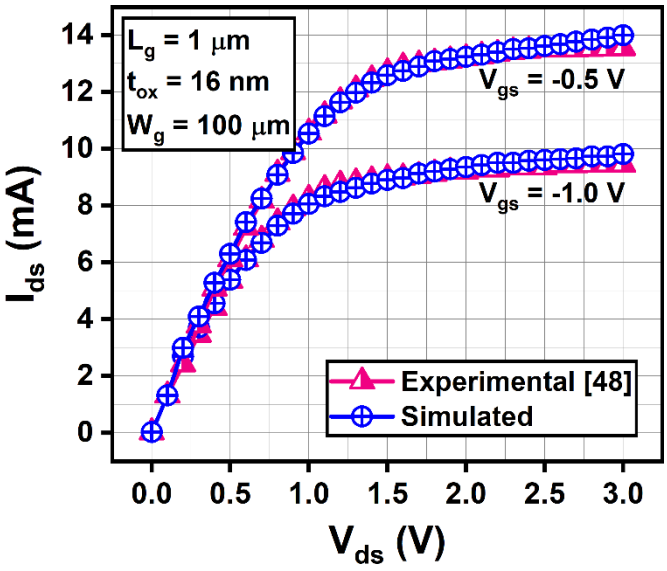

Figure 6.2: Calibration curve of an Al_2O_3/GaAs MOSFET [41, 48].

6.4 DEVICE OPERATION

Figure 6.3 presents a diagrammatic representation of the operation of a GaAs JAM-GS-GAA FinFET sensor for breast cancer cell recognition. Firstly, the biomarker may be generated using aspirate fluid, blood, and urine samples obtained from patients diagnosed with breast cancer. The biomarker was then drop-cast onto the nanocavity area of the GaAs

JAM-GS-GAA FinFET sensor carved beneath the gate electrodes to analyze the desired parameters using a technique based on dielectric modulation.

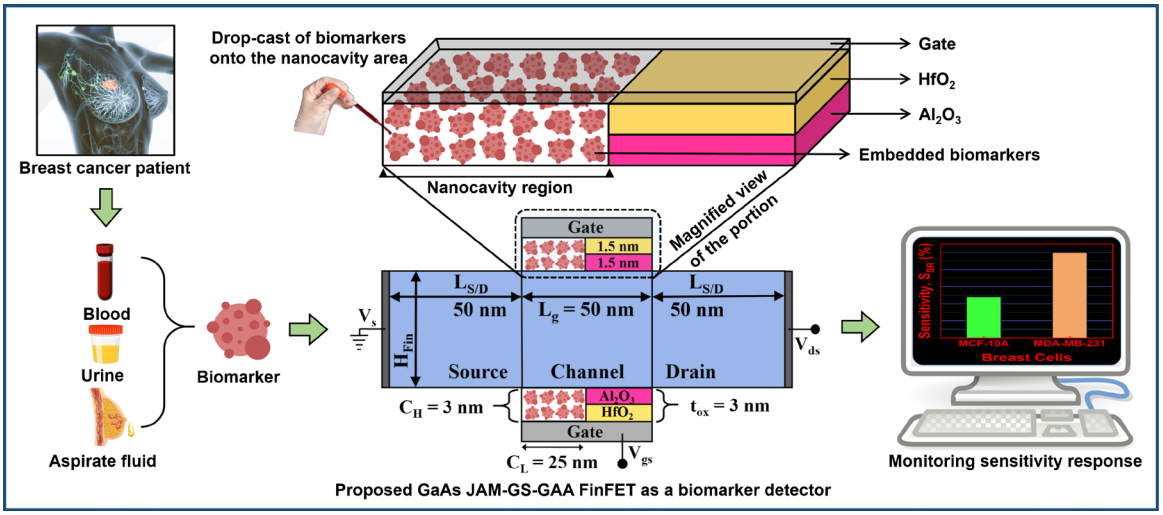

Figure 6.3: Diagrammatic representation of the operation of a GaAs JAM-GS-GAA FinFET sensor for breast cancer cell recognition [41].

6.5 RESULTS AND DISCUSSION

6.5.1 Switching Ratio-Based Sensitivity Analysis

Figure 6.4(a) depicts the transfer characteristics (I_d - V_{gs}) of the proposed sensor for the air, MCF-10A, and MDA-MB-231 in linear and log form. The sensor is examined at V_{ds} = 0.5 V field bias conditions. The drain current increases with the gate-source voltage (V_{gs}) and attains maximum value for MDA-MB-231. In contrast, the opposite trend is observed in the leakage current and degrades significantly for the MDA-MB-231 cancer cell. **Figure 6.4(b)** provides a clearer picture of the fluctuation in ON-current (I_{on}), OFF-current (I_{off}), and switching ratio (SR = I_{on}/I_{off}) (which is subsequently employed as a sensitivity parameter). It can be seen that I_{on} is higher for the MDA-MB-231 cancer cell than for air and healthy cells. It is because introducing the breast cancer cells in the cavity region leads to enhanced effective gate oxide, which in turn increases the coupling between the channel

region and gate metal, and thereby ON-current. The difference in I_{off} between air and MCF-10A is not very large, but for MDA-MB-231, it is noticeably greater, which brings the SR down to a rather remarkable level. **Figure 6.4(c)** compares MDA-MB-231 and MCF-10A cells in terms of their S_{SR}. The graph reveals that the S_{SR} for MDA-MB-231 is 99.72% and 47.78% for MCF-10A. The presence of MDA-MB-231 cells causes a more pronounced shift in I_{off}, which ultimately enhances the device's sensitivity. **Figure 6.4(d)** demonstrates the limit of detection (LoD) plot for the three samples considered. The lowest concentration of an analyte that can be accurately identified from a sample with a high degree of certainty is known as the LoD [49]. LoD is calculated using the response of slope and standard

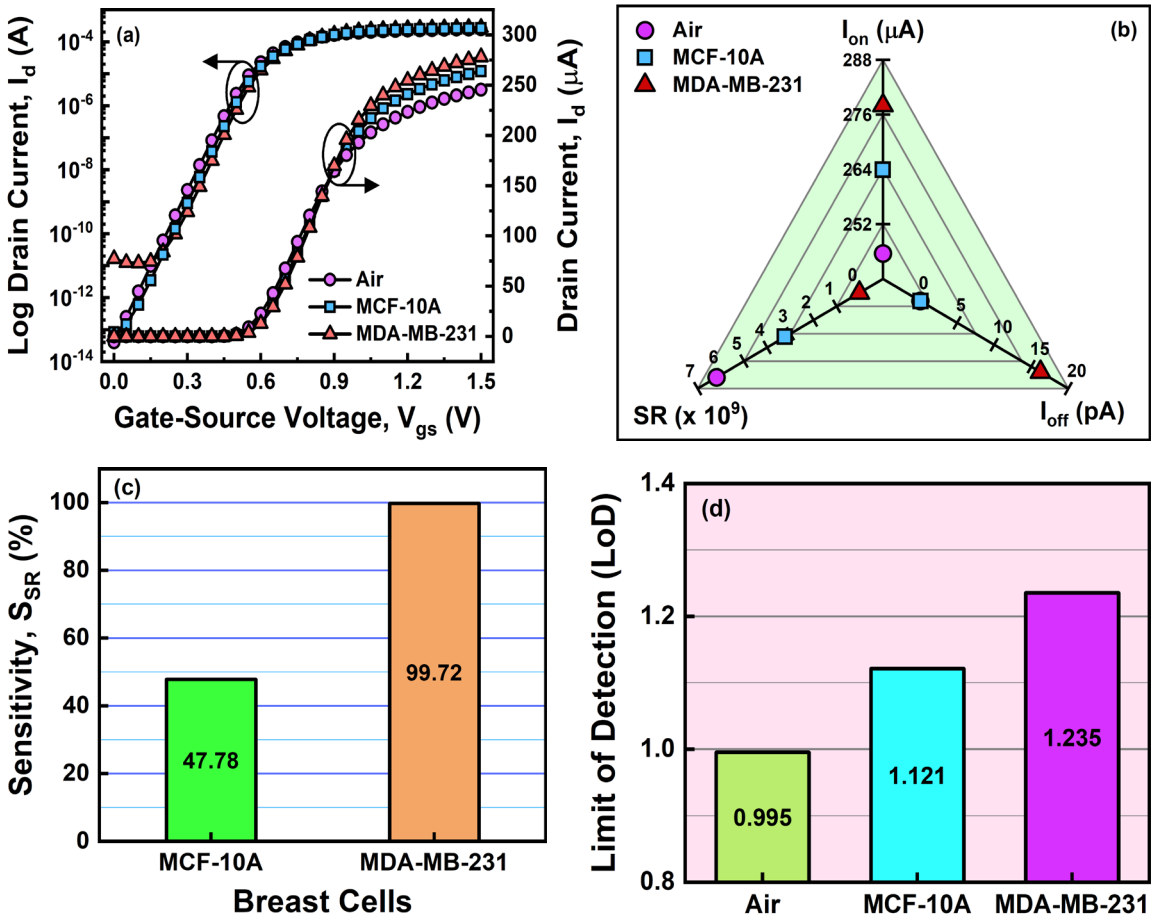

Figure 6.4: (a) Transfer characteristics in linear and log form for air, MCF-10A, and MDA-MB-231, (b) fluctuation in I_{on}, I_{off}, and SR for air, MCF-10A, and MDA-MB-231, (c) S_{SR} comparison of MDA-MB-231 and MCF-10A cells, and (d) LoD plot for air, MCF-10A, and MDA-MB-231 [41].

deviation of the intercept. The slope and standard deviation of the intercept for MDA-MB-231, MCF-10A, and air are analyzed using the transfer characteristics curve (**Figure 6.4(a)**). The slope is 0.0002 for all samples, and the standard deviation is 0.0000749, 0.0000679, and 0.0000603 for MDA-MB-231, MCF-10A, and air. As a result, the LoD obtained for MDA-MB-231 is slightly higher than those for air and MCF-10A. These results provide the relevance of reducing execution variability between devices and enhancing sensitivity while designing and producing nano-FET biosensors.

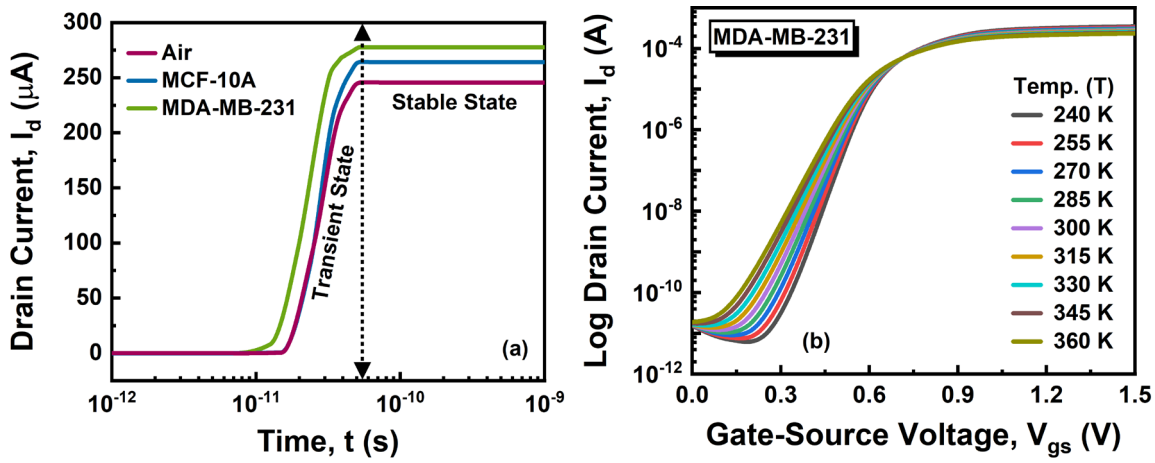

Figure 6.5: Transient response of the drain current for air, MCF-10A, and MDA-MB-231 cells and (b) temperature dependence of the I_d - V_{gs} characteristics of the MDA-MB-231 cancer cell [41].

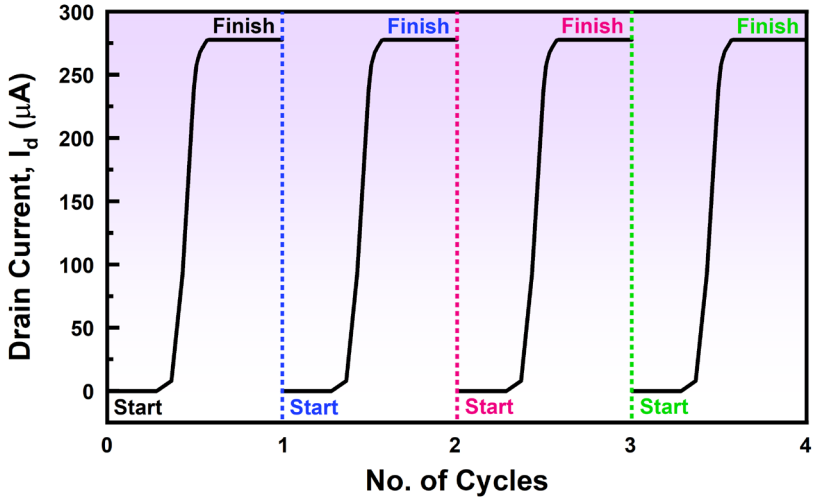

Figure 6.6: Transient response of the proposed sensor for MDA-MB-231 cancerous cells over four cycles [41].

6.5.2 Stability and Reproducibility Analysis

The transient analysis of air, MCF-10A, and MDA-MB-231 cell lines was carried out to test the stability of the proposed sensor. The time it takes for the drain current to settle from its transient state to its steady state is called the settling time (t_{sett}) [50, 51]. The transient response is simulated by applying V_{gs} with an amplitude of 1.5 V, a ramp time of 5×10^{-11} s, a stop time of 1×10^{-9} s, and a step time of 1×10^{-12} s. **Figure 6.5(a)** shows the transient response of the drain current for the air, MCF-10A, and MDA-MB-231 cells. It was observed that the drain current is higher for the MDA-MB-231 cell compared to MCF-10A and air, due to which t_{sett} for the MDA-MB-231 cell is somewhat lower (55.51 ps) than t_{sett} for the MCF-10A cell (60.80 ps) and air (71.58 ps). After t_{sett}, the current becomes steady at a magnitude equal to that at V_{gs} = 1.5 V (**Figure 6.4(a)**). The effect of temperature on the transfer characteristics is investigated to further probe the stability of our proposed sensor. **Figure 6.5(b)** displays the temperature dependence of the I_d - V_{gs} characteristics of the MDA-MB-231 cancer cell; it can be observed that the I_d - V_{gs} curves do not vary significantly between 240 K and 360 K.

Secondly, to examine reproducibility, it is necessary to test the sensor's repeatability under controlled use settings. As shown in **Figure 6.6**, the transient simulation of the proposed sensor is conducted for MDA-MB-231 cancerous cells over four cycles with a gap of 30 minutes between each cycle. The drain current is measured for four cycles, and the findings reveal that the drain current can be reliably reproduced with unnoticeable deviation. The above data suggest that the GaAs JAM-GS-GAA FinFET is sufficiently stable and reproducible.

6.5.3 Cell Viability

The term "oxidative stress" pertains to a state of imbalance between the generation of reactive oxygen species and the capacity of cells to counteract the consequent harm. Cells undergo either apoptotic or necrotic cell death when their antioxidant defence mechanisms are overwhelmed by high amounts of oxidative stress. Zou et al. employed a silicon-based attenuated total reflectance terahertz time-domain spectroscopy (ATR THz-TDS) system to monitor cell mortality caused by oxidative stress in MCF-10A breast cells [52]. This study shows the THz dielectric responses of living and dead MCF-10A breast cells, in which cell death is induced by oxidative stress using a high concentration of hydrogen peroxide (10 mM, H_2O_2). Thus, with the assistance of this study, the dielectric constants at 0.3 THz frequency for MCF-10A breast cells before and after the oxidative stress were extracted to monitor the electrical response of the proposed sensor on the live and dead cells. The sample under consideration (MCF-10A) may be produced by the procedure described by Zou et al. Unfortunately, to the author's best knowledge, no analysis has been

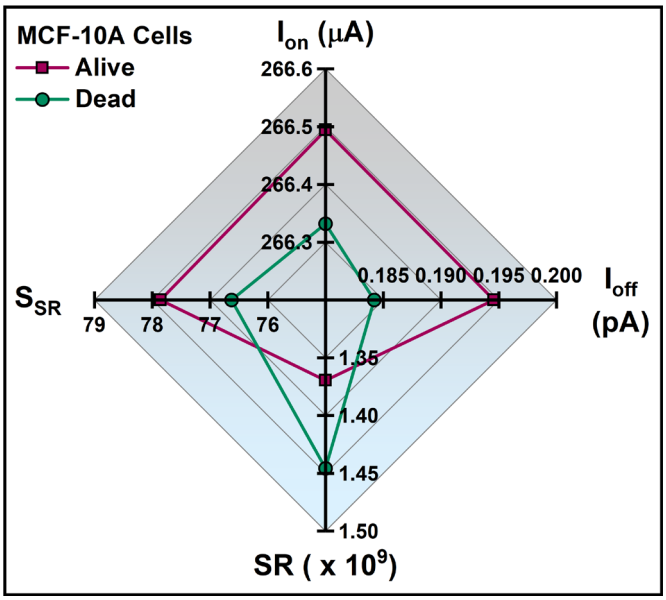

Figure 6.7: Variation in I_{on}, I_{off}, SR, and S_{SR} of living and dead MCF-10A breast cells [41].

performed to characterize the dielectric responses of dead MDA-MB-231 cancerous breast cells. As a result, the electrical response of the proposed sensor on the dead MDA-MB-231 cancerous breast cells could not be determined. The spider-chart depiction of the variation in I_{on}, I_{off}, SR, and S_{SR} of living and dead MCF-10A breast cells is shown in **Figure 6.7**. The induction of cell death through oxidative stress reduces I_{on} from 266.49 μA to 266.33 μA and I_{off} from 0.195 pA to 0.184 pA. Since the reduction in I_{off} is bigger than the drop in I_{on}, SR is increased by 5.55%, and S_{SR} is lowered from 77.86% to 76.62%. Despite the relatively minor changes in the electrical response, the sensor under consideration may differentiate between viable and non-viable cells.

6.5.4 Early Detection

Figure 6.8(a) and **Figure 6.8(b)** demonstrate the transfer characteristics for five different combinations in linear and log form. In the graph, HC represents the healthy cell, and CC is the cancerous cell. The presence of 90% HC and 10% CC indicates a very low quantity of cancerous breast cells, while the presence of 10% HC and 90% CC indicates a very high concentration of breast cancer cells. An enlarged view of the peaks generated by mixing various numbers of healthy and malignant cells is also shown in the inset of **Figure 6.8(a)** and **Figure 6.8(b)**. It is visible that the drain current and the leakage current increase with the rise in the concentration of MDA-MB-231 cancerous cells. **Figure 6.8(c)** exhibits the spider-chart representation of the variance in I_{on}, I_{off}, and SR over the five different combinations. I_{on} increases from 265 μA to 277 μA, I_{off} increases by $\sim 10^2$ orders, and SR decreases by 98.48% when the concentration of cancerous cells is raised from 10% to 90%. Thus, the developed sensor can detect the presence of breast cancer cells, even at low concentrations, allowing for early illness diagnosis.

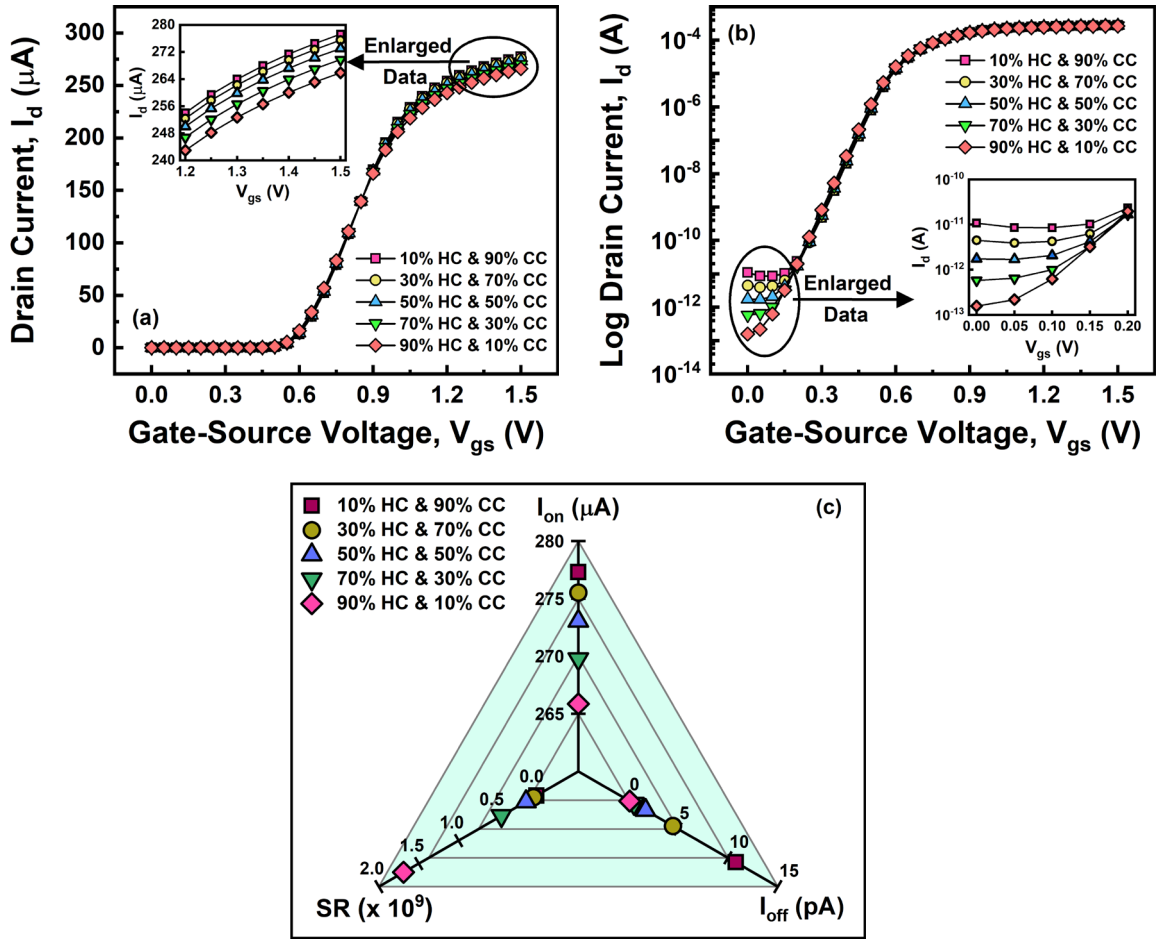

Figure 6.8: Transfer characteristics for five different combinations in (a) linear and (b) log form, and (c) variation in I_{on}, I_{off}, and SR for the combinations considered [41].

6.5.5 Effect of Biomolecule Occupancy on Sensitivity

In order to examine the biomolecule occupancy of the device, five different sites were analyzed: 20%, 40%, 60%, 80%, and 100%. A section of the cavity is covered with biomolecules, while the remaining space is filled with air or left vacant to study the effect of biomolecule occupancy on sensor sensitivity. **Figure 6.9(a)** shows the I_{on}, I_{off}, and SR for a healthy MCF-10A cell, while **Figure 6.9(b)** shows the same data for a malignant MDA-MB-231 cell for the five considered occupancy combinations of biomolecules. The increase in the γ_{Bio} leads to an increase in the effective dielectric and capacitance in the cavity area, ultimately increasing I_{on}. For MCF-10A, the I_{on} is 256 μA at 20% biomolecule

occupancy, which rises to 264 µA for 100% occupancy. Similarly, I_{on} is 267 µA at 20%, which rises to 278 µA at 100% occupancy for MDA-MB-231. I_{off} and SR show the same trend and improve with the increase in γ_{Bio} for MDA-MB-231 and MCF-10A cells. The sensitivity performance for healthy and malignant cells is plotted against different γ_{Bio} in **Figure 6.9(c)**. The sensitivity S_{SR} is 99.85% at 20% biomolecule occupancy, which decreases to 99.72% at 100% occupancy for MDA-MB-231. Similarly, S_{SR} decreases from 66.98% to 47.78% for MCF-10A. Thus, S_{SR} decreases slightly with the increase in γ_{Bio} for MDA-MB-231 and MCF-10A cells.

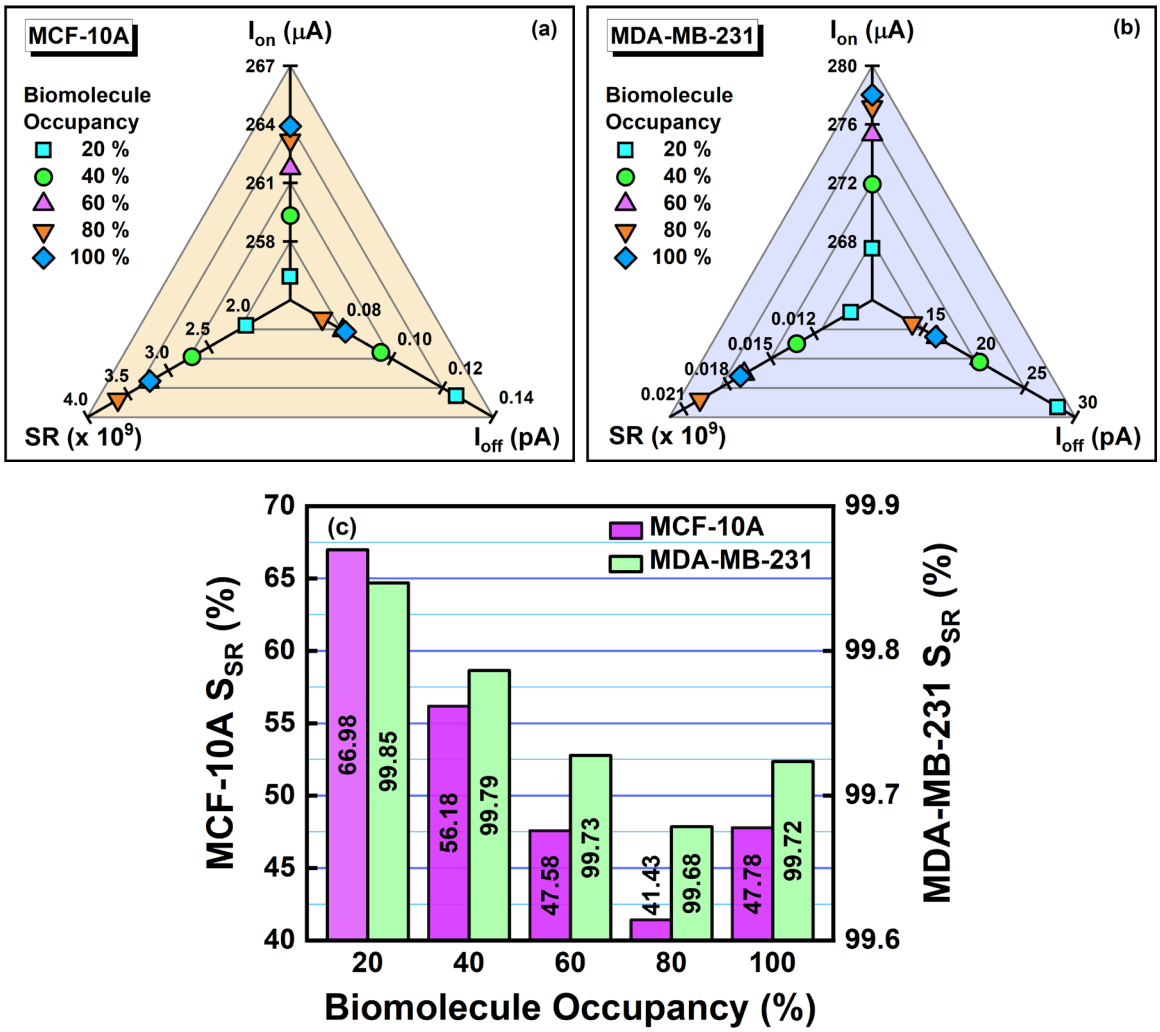

Figure 6.9: Biomolecule occupancy impact on I_{on}, I_{off}, and SR for (a) MCF-10A and (b) MDA-MB-231, and (c) sensitivity performance for healthy and malignant cells against different γ_{Bio} [41].

6.5.6 Effect of Device Parametric Variation on Sensitivity

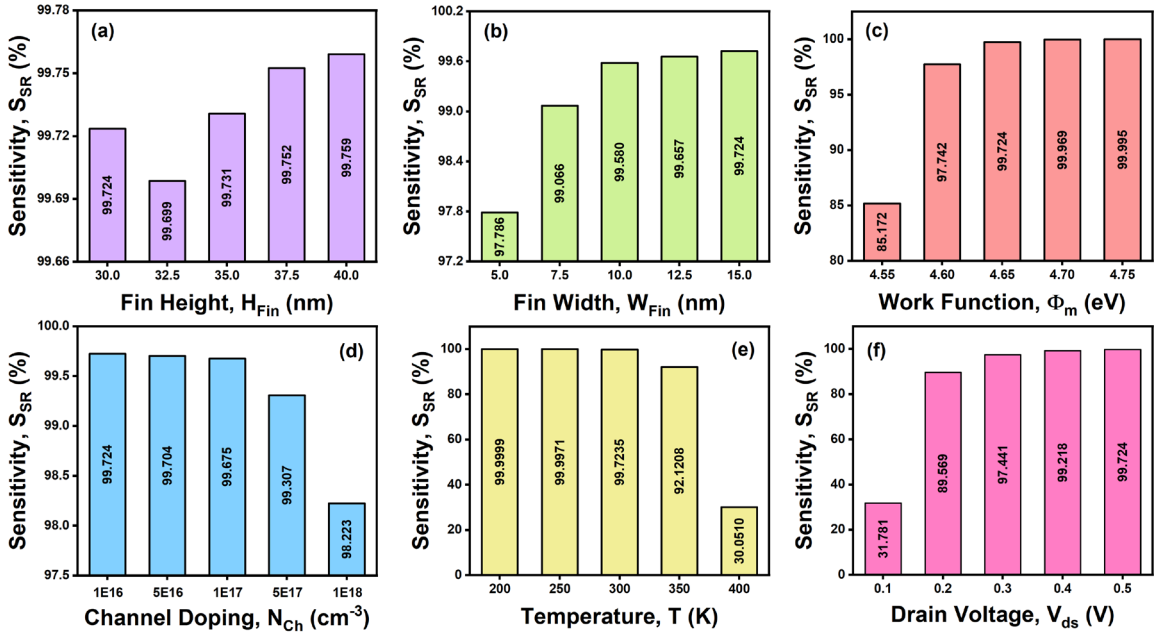

Figure 6.10: S_{SR} of the proposed sensor against the deviation of mentioned parameters for the MDA-MB-231 cancerous cell [41].

Figure 6.10(a-f) collectively demonstrates the S_{SR} of the proposed sensor against the deviation of the mentioned parameters for the MDA-MB-231 cancerous cell. The fin height (H_{Fin}) varies from 30 nm to 40 nm with a step size of 2.5 nm. The S_{SR} of the proposed device increases with the surge in the H_{Fin}, as shown in **Figure 6.10(a)**. Fin width (W_{Fin}) is altered from 5 nm to 15 nm with a step size of 2.5 nm. **Figure 6.10(b)** displays the sensitivity S_{SR} as a function of W_{Fin} and shows an improvement in S_{SR} with the rise in W_{Fin}, thus following the path of H_{Fin}. The gate electrode work function (ϕ_m) is varied from 4.55 eV to 4.75 eV with an increase of 0.5 eV. The S_{SR} is 85.17% for 4.55 eV, which rises to 99.99% for 4.75 eV, as depicted in **Figure 6.10(c)**. Next is channel doping (N_{Ch}), which is considered from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}. **Figure 6.10(d)** exhibits the variation of S_{SR} with N_{Ch} and shows that the increase in the N_{Ch} results in sensitivity degradation. The temperature (T) range is from 200 K to 400 K, with a measurement taken for every 50 K,

as portrayed in **Figure 6.10(e)**. The reduction in the S_{SR} is marginal from 200 K to 300 K, but afterward, S_{SR} reduces significantly with the reduction in T. Lastly, in **Figure 6.10(f)**, the sensitivity is plotted against the drain voltage (V_{ds}), which varies from 0.1 V to 0.5 V with a step size of 0.1 V. The S_{SR} is relatively lower at 0.1 V but increases after that with the increase in the V_{ds}, with the highest value being recorded at V_{ds} = 0.5 V. Thus, to summarize, the increased levels of fin height, fin width, gate electrode work function, and drain voltage, and the decreased levels of channel doping and temperature, make it simpler to identify the breast cancer cells.

6.5.7 Effect of Frequency on Sensitivity

Four parameters, namely I_{on}, I_{off}, SR, and S_{SR} of MDA-MB-231 and MCF-10A breast cells, were evaluated at 13.6 GHz to study the effect of frequency on these parameters. The comparative statistics for 200 MHz and 13.6 GHz in tabular form are shown in **Figure 6.11**, along with a plot of the percentage change in each performance parameter mentioned above for MDA-MB-231 and MCF-10A breast cells. The percentage change was evaluated considering 200 MHz as the initial value and 13.6 GHz as the final value, and the actual percentage change was plotted to better understand the impact of the frequency of the respective parameter. When the frequency is raised from 200 MHz to 13.6 GHz, the I_{on} reduces by 1.93% and S_{SR} by 2.85%, and I_{off} and SR improve by 3.70% and 2.48%, respectively, for MCF-10A. Similarly, for MDA-MB-231, the I_{on} reduces by 0.86% and S_{SR} by 0.69%, and I_{off} and SR improve by 71.57% and 247.06%, respectively, with the rise in frequency. Thus, the proposed sensor detection sensitivity is significantly better at 200 MHz compared to 13.6 GHz for MDA-MB-231 and MCF-10A.

Parameters	MCF-10A		MDA-MB-231	
	200 MHz	13.6 GHz	200 MHz	13.6 GHz
I_{on} (μA)	263.90	258.80	278.00	275.60
I_{off} (pA)	0.081	0.078	16.25	4.62
SR ($\times 10^9$)	3.23	3.31	0.017	0.059
S_{SR} (%)	47.78	46.42	99.72	99.03

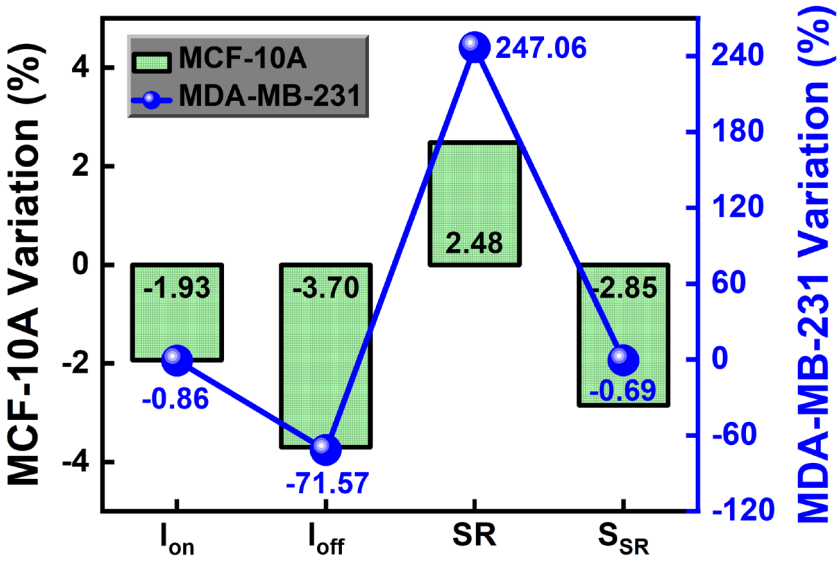

Figure 6.11: Percentage change in each mentioned performance parameter for MDA-MB-231 and MCF-10A breast cells [41].

6.5.8 Comparison with Existing/Published Breast Cancer Detectors

An evaluation of the proposed breast cancer sensor against existing breast cancer detectors is required to determine its efficacy. Table 6.2 overviews the proposed FinFET breast cancer sensor with other already published breast cancer sensors regarding the change in drain current (ΔI_{ds}) and drain current sensitivity (S_{Id}). The ΔI_{ds} data were unavailable for the reduced graphene oxide (rGO) encapsulated nanoparticle (NP)-based FET biosensor, so the device's sensitivity is mentioned, which is about 3.9%. The highest reported ΔI_{ds} was 6 μA for the AlGaN/GaN HEMT structure, with ΔI_{ds} for the remaining devices being

relatively low. The proposed GaAs JAM-GS-GAA FinFET sensor exhibits improved results compared to the breast cancer detectors mentioned in Table 6.2, with ΔI_{ds} of about 32.5 μA and S_{Id} of 13.21%.

Table 6.2: Overview of proposed FinFET-based cancer detector vs. existing cancer detectors [41].

Ref.	Platform device	Detection	ΔI_{ds} (μA)	S_{Id} (%)
[39]	AlGaN/GaN HEMT	c-erbB-2, a breast cancer marker	6	-
[53]	rGO encapsulated NP-based FET	HER2 and EGFR, a breast cancer marker	-	3.9
[54]	Apta-cyto-sensor	MDA-MB-231 breast cancer cells	3	-
[55]	CNT FET biosensor	Breast cancer exosomal miRNA21	1.65	-
[38]	DL-NC-FE-TFET	Different breast cancer lines	1.83	-
This work	GaAs JAM-GS-GAA FinFET	MDA-MB-231 breast cancer cells	32.5	13.21

6.6 SUMMARY

This chapter details the usage of a GaAs JAM-GS-GAA FinFET to monitor the device switching ratio to achieve the electrical identification of the MDA-MB-231 breast cancer cell. In order to increase the detection sensitivity, the proposed sensor makes use of four nanocavities that are carved underneath the gate electrodes. The switching ratio-based sensitivity of the sensor is measured for healthy and malignant breast cells and turns out to be 47.78% and 99.72%, respectively. The sensor was evaluated for its reproducibility and stability. It was found to be repeatable and adequately stable with settling times of 55.51 ps for the MDA-MB-231 cell, 60.80 ps for the MCF-10A cell, and 71.58 ps for air. Furthermore, the sensor is capable of distinguishing between viable and non-viable cells based on changes in their electrical response. The research also shows that breast cancer cells can be identified with the assistance of Bruggeman's model even when present in a

mixed solution of malignant and healthy cells, even though the quantity of cancerous cells is lower. The effect of biomolecule occupancy and frequency fluctuations on the device's sensitivity is also investigated. This chapter also describes how to enhance the sensing performance by altering the fin height, fin width, gate electrode work function, channel doping, temperature, and drain voltage. The proposed sensor can better identify malignant cells when the levels of H_{Fin}, W_{Fin}, ϕ_m, and V_{ds} increase and the N_{Ch} and T levels decrease. Finally, this work compared the proposed GaAs JAM-GS-GAA FinFET sensor to previously published breast cancer sensors regarding the change in drain current and drain current sensitivity and found that the proposed sensor performed much better. Thus, the proposed GaAs JAM-GS-GAA FinFET sensor may be considered an intriguing candidate for MDA-MB-231 breast cancer cell detection.

Furthermore, the next chapter serves as the culmination of the research done in the thesis and provides an outlook on potential future developments regarding the proposed solutions.

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7

CHAPTER

Conclusion and Future Scope

- *This chapter provides a summary of the research conducted throughout this thesis.*
- *Furthermore, the concrete conclusion derived from the presented results is also briefly discussed.*
- *Subsequently, this chapter outlines the potential future scope of work that might be pursued to expand upon the present study.*

7.1 CONCLUSION

This thesis mainly encompasses a Junctionless-Accumulation-Mode Gate-Stack Gate-All-Around (JAM-GS-GAA) FinFET architecture to overcome the challenges faced by conventional FinFET as it provides improved sub-threshold characteristics, suppressed off-state leakage current, extremely high packing density, and reduced fabrication cost and complexity. In this thesis, various scalability and reliability issues of JAM-GS-GAA FinFET have been rigorously examined and compared with different architectures. Additionally, approaches such as dual-k spacer engineering have been used to further increase the performance of JAM-GS-GAA FinFETs. Starting with a comprehensive study of the analog and RF characteristics of JAM-GS-GAA FinFET has been explored in **Chapter 2** with the optimization of the fin aspect ratio at the sub-nano level using extensive 3D simulations. The investigation found that the analog and RF parameters significantly improved for the JAM-GS-GAA FinFET device compared to conventional FinFET. When compared to conventional FinFET, parameters like I_{on}/I_{off} ratio, GTFP, and GFP increased by 31, 3.37, and 2.73 times, respectively, while A_v, V_{EA}, I_{off}, TGF, and TFP improved by 183.36%, 160.30%, 96.59%, 88.18%, and 21.46% for the JAM-GS-GAA FinFET device. Furthermore, it is also analyzed that the proposed device with the highest fin aspect ratio configuration exhibits the most improved analog and RF performance compared to the other lower fin aspect ratio configurations. I_{off} and SS are reduced by 94.72% and 14.90%, respectively, while R_{out}, A_v, V_{EA}, GFP, and GTFP are enhanced by more than two times in magnitude for a device with a high fin aspect ratio. Thus, the proposed JAM-GS-GAA FinFET device with a high fin aspect ratio can be considered an attractive solution for designing analog and RF circuits.

Despite the improved analog and RF performance achieved for the JAM-GS-GAA FinFET device, addressing the proposed device's reliability issues is crucial to guarantee its dependability. Thus, in **Chapter 3**, the impact of temperature and gate electrode work function on the static, analog, RF, and wireless performance has been inspected to explore the reliability issues of the JAM-GS-GAA FinFET. The study's findings indicate that the static parameters do not change much as the temperature increases from 300 K to 500 K. Analog and RF performance metrics exhibit changes to the temperature rise. As the temperature increases from 300 K to 500 K, the influence of temperature on wireless performance is less prominent, as measured by linearity and harmonic distortion metrics. Further, results revealed that the peak values of parameters like g_m, f_T, TFP, g_{m2}, g_{m3}, VIP2, VIP3, HD2, and HD3 are approximately the same for all work functions. Therefore, it can be inferred that the JAM-GS-GAA FinFET demonstrates satisfactory reliability in the face of temperature fluctuations and changes in the gate electrode work function. As a result, JAM-GS-GAA FinFET has excellent potential as a viable option for applications requiring analog/RF functionality and low power consumption with good linearity.

Now, it is essential to further enhance the performance of the JAM-GS-GAA FinFET device and make it suitable for sub-10 nm RFIC circuits. It can be achieved using a dual-k spacer configuration, which integrates a high-k spacer on the inside with a low-k spacer on the exterior to improve the device's performance. Consequently, the impression of adding a dual-k spacer on the RFIC design viability of a JAM-GS-GAA FinFET in the sub-10 nm region is investigated in **Chapter 4**. It was observed that the dual-k spacer configuration improves the electron velocity, electric field, surface potential, and energy band profiles due to the fringing field effects. Thereby increasing the I_{on} of the dual-k spacer configuration by 35.34%, I_{on}/I_{off} ratio by approximately 10^2 times, g_m by 24.03%, TGF by

39.12%, QF by 46.75%, V_{EA}, A_v, GFP, and GTFP by five times, while decreasing the I_{off} by over 76 times, g_d by 21.13%, DIBL by 66.61%, and SS by 15.47% compared to the conventional FinFET configuration. Also, the results indicate that transitioning from a single-k spacer structure to a complicated dual-k spacer structure improves I_{off}, V_{EA}, A_v, GTFP, and GFP by 81.78%, 78.17%, 73.98%, 70.28%, and 53.46%, respectively. Thus, JAM-GS-GAA FinFET with dual-k spacer can be seen as a potential element in future low-power RFIC circuits.

As the dimensions of CMOS devices are scaled down continuously to meet the ULSI industry's demand, further downscaling will be very demanding due to many practical limitations, like parasitic capacitances, threshold voltage roll-off, drain-induced barrier lowering (DIBL), etc. Unsurprisingly, further enhancement in transistor performance and speed while downscaling the device will be possible using new semiconductor materials. Thus, **Chapter 5** explores the parasitic capacitances and small-signal behavior of JAM-GS-GAA FinFET with GaAs as a fin material. It is noticed that compared to silicon, the I_{off} current reduces ~100 times, the I_{on}/I_{off} ratio increases ~10^3 times, DIBL becomes half, and SS decreases ~26% for GaAs. The parasitic capacitances follow the same trend: C_{gs} reduced by 52.71%, C_{gd} by 75.48%, and C_{gg} by 67.52% with the incorporation of GaAs. Due to this considerable decrease in the parasitic capacitances, the peak value of both GBP and TFP increases by 10 times. Further, the effect that parameters like L_g, N_{Ch}, W_{Fin}, ϕ_m, and T have on the parasitic capacitances and S-parameters of GaAs JAM-GS-GAA FinFET are examined. Parasitic capacitances are found to decrease appreciably for a device with a shorter L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m, whereas, at extremely high frequencies, the S-parameters improve considerably for a device with a larger L_g, smaller N_{Ch}, lower W_{Fin} and T, and higher ϕ_m. Thus, the proposed

device with the mentioned specifications can be considered suitable for both low-power ULSI switching applications and microwave oscillators and amplifiers by striking a balance of gate length.

Now, the objective is to identify the MDA-MB-231 breast cancer cells electrically using the GaAs JAM-GS-GAA FinFET with high sensitivity for use in medical diagnosis. The usage of a GaAs JAM-GS-GAA FinFET to monitor the device switching ratio to achieve the electrical identification of the MDA-MB-231 breast cancer cell is examined in **Chapter 6**. The proposed sensor uses four nanocavities carved underneath the gate electrodes for enhanced detection sensitivity. The switching ratio-based sensitivity of the sensor is measured for healthy and cancerous breast cells and turns out to be 47.78% and 99.72%, respectively. The sensor was found to be repeatable and adequately stable, with settling times of 55.51 ps for the MDA-MB-231 cell, 60.80 ps for the MCF-10A cell, and 71.58 ps for air. Furthermore, the sensor is capable of distinguishing between viable and non-viable cells based on changes in their electrical response. Breast cancer cells can be identified with the assistance of Bruggeman's model even when present in a mixed solution of cancerous and healthy cells, even though the quantity of cancerous cells is lower. The effect of biomolecule occupancy and frequency fluctuations on the device's sensitivity is also investigated. The proposed sensor can better identify cancerous cells when the levels of H_{Fin}, W_{Fin}, ϕ_m, and V_{ds} increase and the N_{Ch} and T levels decrease. Finally, the GaAs JAM-GS-GAA FinFET sensor is compared to previously published breast cancer sensors regarding the change in drain current and drain current sensitivity, and found that the proposed sensor performed much better. Thus, the proposed GaAs JAM-GS-GAA FinFET sensor may be considered an intriguing candidate for MDA-MB-231 breast cancer cell detection.

7.2 FUTURE SCOPE

The primary objective of this thesis is to design and optimize a JAM-GS-GAA FinFET device that can address the constraints associated with a conventional FinFET structure. The investigation of the proposed device's immunity to temperature variations and variations in gate electrode work function has been conducted to ascertain the device's reliability. This thesis primarily focuses on the static, analog, RF, and wireless characteristics of the JAM-GS-GAA FinFET device. Engineering schemes like dual-k spacer engineering have been incorporated to improve the device's performance. Another objective of this research work is to assess the suitability of the proposed device to detect the MDA-MB-231 breast cancer cells. All research objectives have been achieved through extensive 3D numerical simulations. However, there are some objectives that can be explored as potential future elements.

1. The circuit behavior of the JAM-GS-GAA FinFET can be explored to make the proposed device suitable for digital circuit applications such as CMOS inverters, SRAM, and other gated logic designs.
2. The investigation of the noise characteristics of JAM-GS-GAA FinFET is a valuable endeavor, particularly noise performance metrics such as cross-correlation, auto-correlation, noise figures, and others. This exploration highlights the potential of JAM-GS-GAA FinFET as a compelling solution for the ongoing integration process in analog and digital design technology and for designing low-noise amplifiers.
3. The research conducted in this thesis does not consider the presence of interface trap charges (ITC). Thus, it is crucial to analyze the proposed device for both mobile and stationary ITCs to understand the reliability implications regarding defects.

4. Only silicon and GaAs are examined as channel material in this thesis work. However, there is potential for further investigation into other materials, including III-V compounds and 2D materials like graphene. These materials exhibit enhanced carrier mobility, and efforts can be made to make the proposed device compatible with high-speed applications, such as high-frequency communication devices.
5. A thin sheet of ferroelectric material may be integrated into the gate construction. The JAM-GS-GAA FinFET with a ferroelectric layer is appropriate for non-volatile memory cells and low-power logic devices because it retains its state even when the power supply is turned off.
6. Moreover, the design of the biosensor device may be engineered to effectively identify and measure other viruses, such as influenza, HIV, and SARS-CoV-2. Alternatively, it can also serve as a gas sensor capable of detecting hazardous chemicals.

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ORIGINAL PAPER

Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET

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Abstract
This work presents the analog and RF performance evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET, and the results acquired have been compared with conventional FinFET and GAA FinFET. It has been observed that in comparison to conventional FinFET, leakage current (I_{off}) reduces by almost thirty times for the GS-GAA FinFET configuration. Thus, revamping the threshold voltage (V_{th}), switching ratio (I_{on}/I_{off}), and subthreshold slope (SS) of the proposed device. Also, major analog parameters like transconductance (g_m), transconductance generation factor (TGF) enhances considerably with early voltage (V_{EA}) and intrinsic gain (A_v) increased by over two times in magnitude for the GS-GAA FinFET configuration. Furthermore, several important RF parameters have been explored, and the outcome of the study is that the GS-GAA FinFET configuration shows superior RF performance. In GS-GAA FinFET configuration, the gain frequency product (GFP) and gain transconductance frequency product (GTFP) amplified by over two times in magnitude with minimal decrease in the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). Thus, the proposed GS-GAA FinFET device can be looked upon as an appealing option for high-frequency analog/RF applications.

Keywords Analog/RF parameters · Gate Stack (GS) · Gate All Around (GAA) FinFET · Junctionless Accumulation Mode (JAM) · Short Channel Effects (SCEs) · TiN metal gate

1 Introduction

According to Gordon E. Moore, the number of transistors in a given unit of space will double up almost every eighteen months [1]. Thus, to follow up with Moore's Law, CMOS technology is being aggressively scaled-down and is reaching its fundamental limits. As the channel length of the device decreases gradually, the device starts suffering from issues like pin-point ultra-sharp S/D junction's formation, and short-channel effects (SCEs) such as drain induced barrier lowering, mobility degradation [2–4]. Colinge et al. resolved the problem in the form of junctionless field-effect transistors (JLFETs) [5]. In JL transistors, doping species (either n-type or p-type) is the same in all the regions. The junctionless device, in comparison to conventional CMOS devices, has better immunity against the SCEs with effectively increased channel length. However, the difficulty arises in the fabrication of a narrow and thin channel layer, which is essential to completely deplete the channel during the OFF state to attain excellent turn-off characteristics [6]. If the doping concentration of the channel region is relatively low, then carriers will quickly deplete in the OFF state; however, it leads to increased S/D series resistance accompanied by a decrease in drain current. Therefore, to get over these problems, junctionless accumulation mode (JAM) FETs with increased S/D doping is used [7, 8]. In 1999, professor Chenming Hu proposed a "3D" transistor named FinFET to alleviate the SCEs [9]. Several research papers have already been published on FinFET and taking into consideration that as the number of gates increases, electrostatic control over the channel increases, GAA structure has been explored for better device performance and improved SCEs [10]. As per the International Technology Roadmap for Semiconductors (ITRS) guideline, GAA is also known as "ultimate structure" [11].

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Another primary concern is the increment in the gate direct tunneling current with the decreasing gate oxide thickness, resulting in the enhanced off-state leakage current [12, 13]. The use of high-κ dielectric materials, like HfO_2 (κ = 25) [14], proved to be the most technological solution. However, the direct deposition of high-κ dielectrics on Si substrate remains a challenging field. The challenges that need to be overcome are mobility degradation accompanied by below-par subthreshold swings, threshold voltage instability, and maintaining the interface quality between the high-κ dielectric and Si substrate [15, 16]. An alternative is to use Gate Stack (GS) architecture comprising of a thin interfacial SiO_2 layer as passivation between the Si substrate and high-κ dielectrics by maintaining the effective oxide thickness (EOT) constant [17]. Thus, keeping in mind all the considerations, we are proposing a JAM GS-GAA FinFET. Nowadays, metal gates are preferred over polysilicon gates because polysilicon shows a poly-depletion effect, thereby affecting the EOT of the device. Also, polysilicon gates, when brought in contact with high-κ dielectrics, are chemically unstable [18]. TiN is picked as the metal gate due to its thermal stability, high purity, low resistivity, and compatibility with CMOS processing [19, 20].

In the last few years, demands for portable and higher battery backup electronic devices have sufficiently increased. To maintain the increased demand, speed performance, and transistors density in the IC needs to go up, and that can be obtained by System-on-Chip (SoC) concept. In SoC technology, the majority of the elements of a system are integrated as an independent system on a semiconductor chip. The device optimization is very challenging with SoC technology [21]. Thus, the purpose of this study is to analyze the device structure and improve the device performance for high-frequency analog/RF circuit applications. Analog and RF performance of JLAM-CGAA MOSFET has been investigated extensively [22]. In another study, Raskin et al. reported the analog/RF performance of multiple gate SOI devices [23]. However, to the best knowledge of the authors, no report has been published on the analog and RF performance of JAM GS-GAA FinFET. In this work, extensive simulations have been performed to investigate the several important electrostatic, analog, and RF parameters of the three different devices, namely, conventional FinFET, GAA FinFET, GS-GAA FinFET. Besides, we have also evaluated various other RF metrics significant for RF applications such as f_{max}, GFP, TFP, and GTFP for RF performance.

It is observed from the simulated results that JAM GS-GAA FinFETs provide several advantages like higher switching ratio, improved subthreshold slope, etc. with minimal decrease in the f_T and f_{max} in comparison to the other two devices.

Starting with the introduction, section 2 narrates the device structure. Section 3 deals with the simulation methodology used and calibration between the simulation data and experimental data. Section 4 analyses the analog and RF performance parameters of the device with concluding remarks in section 5, authenticating the originality of the paper.

2 Device Structure

Figure 1 displays the proposed 3D structure of JAM GS-GAA FinFET, whereas horizontal and vertical cross-sectional view cut along the silicon fin of the proposed device is portrayed in Fig. 2 (a) and (b), respectively. The gate length (L_g) of the device is 7 nm, and the length of S/D regions ($L_{S/D}$) is fixed at 10 nm. The oxide thickness (t_{ox}) is kept constant all around the fin at 1 nm, as depicted in Table 1. In GS-GAA FinFET, SiO_2 and HfO_2 are amalgamated in equal proportion, whereas in the other two structures, only SiO_2 is used as a gate oxide. Silicon material is used in the fin structure with height (H_{Fin}) and width (W_{Fin}) of the fin fixed at 10 nm and 5 nm, respectively, thereby following the property of width quantization, which says that W_{Fin} must be a multiple of H_{Fin} [24, 25]. All the regions are uniformly doped with n-type doping species. The doping concentration in the source/drain regions ($N_{S/D}$) is 10^{19} cm^{-3}, and that of the channel region (N_{Ch}) is 10^{16} cm^{-3}. The work function (φ_m) is kept at 4.65 eV for the TiN metal gate [20].

3 Simulation Methodology and Calibration

The SILVACO ATLAS 3D simulator has simulated all the three different configurations. In the entire device simulation, V_{ds} is fixed at 0.5 V, V_{gs} is changed from 0 V to 1 V, and the T is at 300 K. In amplifier circuits, the region of operation is decided by gate overdrive voltage (V_{gt}). As a result, all the analog and RF analysis has been done against V_{gt}. It is the voltage difference between gate to source voltage and threshold voltage, i.e., $V_{gt} = V_{gs} - V_{th}$. Several physical models are included in device simulation for different purposes like the Arora model is incorporated to grab concentration-dependent

Table 1 Different device parameters used for simulation

Parameter	FinFET	GAA FinFET	GS-GAA FinFET
L_g (nm)	7	7	7
$L_{S/D}$ (nm)	10	10	10
t_{ox} (nm)	1 (SiO_2)	1 (SiO_2)	1 (0.5 SiO_2 + 0.5 HfO_2)
H_{Fin} (nm)	10	10	10
W_{Fin} (nm)	5	5	5
$N_{S/D}$ (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
N_{Ch} (cm^{-3})	1×10^{16}	1×10^{16}	1×10^{16}
φ_m (eV)	4.65 (TiN)	4.65 (TiN)	4.65 (TiN)

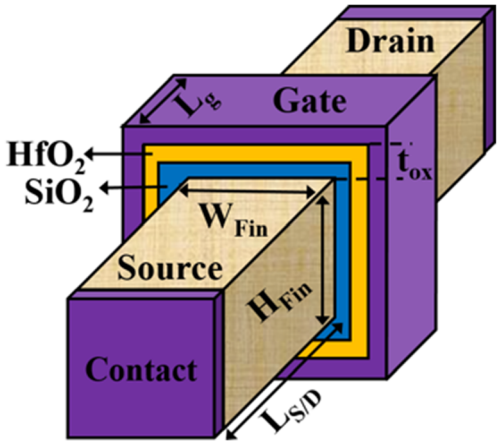

Fig. 1 Systematic 3-D structure of the proposed JAM GS-GAA FinFET

mobility. For recombination effects, Shockley-Read-Hall (SRH) model is employed to imitate the existence of trap charges at the interface. The Fermi-Dirac statistics model is used to increase the precision in the results. Crowell impact ionization and Klaassen band to band tunneling models are also included to incorporate the impact ionization and tunneling effects. Further, Gummel and Newton's methods are used to attain a solution [26]. The physical models discussed above have been validated with the published results of Hyunjin Lee et al. [27]. Figure 3(a) shows the simulated and experimental I_d - V_{gs} characteristics of a 5 nm All-Around-Gate (AAG) FinFET at $V_{ds} = 1.0$ V. Figure 3(b) reflects the I_d - V_{ds} characteristics at $V_{gs} = 0.2$ V and $V_{gs} = 0.4$ V. It is visible from both Fig. 3(a) and (b) that the results are well-calibrated.

4 Results and Discussion

4.1 Device Scalability

In Fig. 4, the variation of drain current (I_d) with gate to source voltage (V_{gs}) at $V_{ds} = 0.5$ V is displayed in both linear and log scale for different configurations. It is observed that I_d increases with the increase in the V_{gs} and is maximum for GS-GAA FinFET structure. Also, it is found that leakage current (I_{off}) reduces significantly in GS configuration due to the enhanced gate coupling capacitances and reduced tunneling current. Thus, as shown in Fig. 5 due to increased drain current and decreased leakage current, higher switching ratio (I_{on}/I_{off}), and consequently, superior switching speed is obtained for GS-GAA FinFET configuration. Figure 6 represents the threshold voltage (V_{th}) for conventional FinFET, GAA FinFET, GS-GAA FinFET. The threshold voltage increases sequentially and recorded maximum for GS-GAA FinFET due to the enhanced control over the channel and better shielding of drain-side potential by the GAA structure, thereby improving the subthreshold characteristics [28].

In designing a microscopic device, the subthreshold swing (SS) is an essential short channel parameter. It is visible from Fig. 7 that SS is lowest and nearest to its ideal value (60 mV/dec) for GS-GAA FinFET. It is because the gate coupling capacitance increases as the permittivity (κ) increases, which increases the gate control on the channel, leading to an increased SS.

4.2 Analog Performance

In this subsection, from the perspective of the analog application, several important analog parameters such as transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), early voltage (V_{EA}), and intrinsic gain (A_v) are evaluated. Equations (1) and (2) estimates g_m and TGF, respectively, and both parameters should be high for better analog performance [29]. Figure 8 outlines a collaborated plot of g_m and TGF as a function of V_{gt} for all the three different configurations. Transconductance is a parameter that computes the change in drain current to the shift in V_{gs} at constant V_{ds}. Thus, g_m is obtained from the derivative of the I_d-V_{gs} curve. Comparing to their counterparts, GS-GAA FinFET has the maximum value of transconductance because

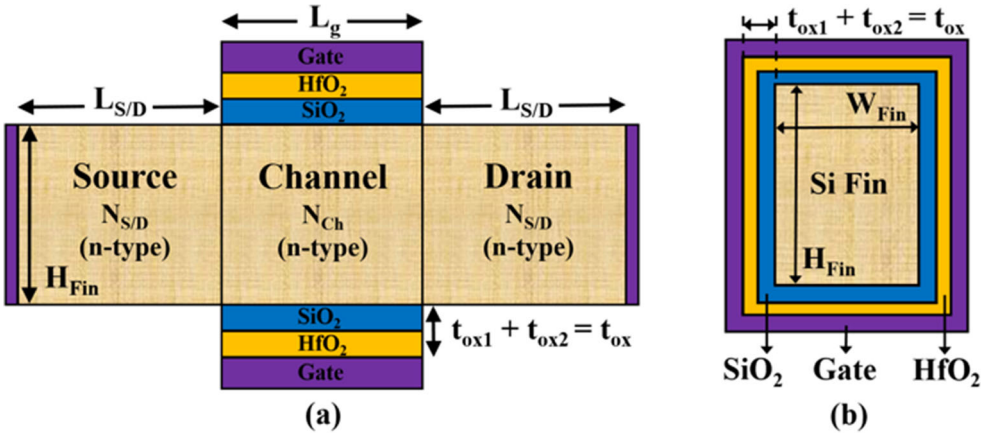

Fig. 2 (**a**) Horizontal (**b**) Vertical cross-sectional view cut along the silicon Fin of the proposed JAM GS-GAA FinFET

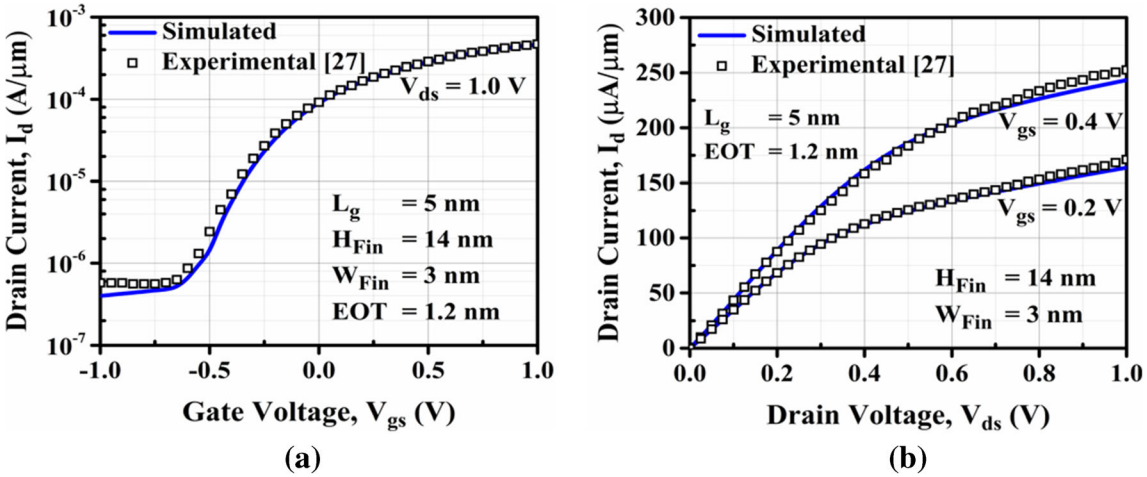

Fig. 3 (**a**) Calibrated I_d-V_{gs} characteristics of 5 nm All-Around-Gate FinFET. (**b**) Calibrated I_d-V_{ds} characteristics of 5 nm All-Around-Gate FinFET

of the enhanced gate control on the channel and reduced short channel effects. Also, gate-stack architecture enhances the average carrier velocity, resulting in improved electron mobility, and consequently, g_m increases [30]. The transconductance generation factor is the proportion of gain generated per unit power loss. The device operating at low supply voltages performs more efficiently for higher values of TGF. It is observed from Fig. 8 that the TGF changes only in the subthreshold region, with all most having the same value in the strong inversion region. GS-GAA FinFET configuration achieves the maximum value of TGF and is closest to its ideal value $\approx 40\ V^{-1}$ at the device's minimum SS (60 mV/dec) [29]. The reason for this is that the higher value of I_d corresponds to higher g_m and, consequently, higher TGF.

$$g_m = \partial I_d / \partial V_{gs} \tag{1}$$

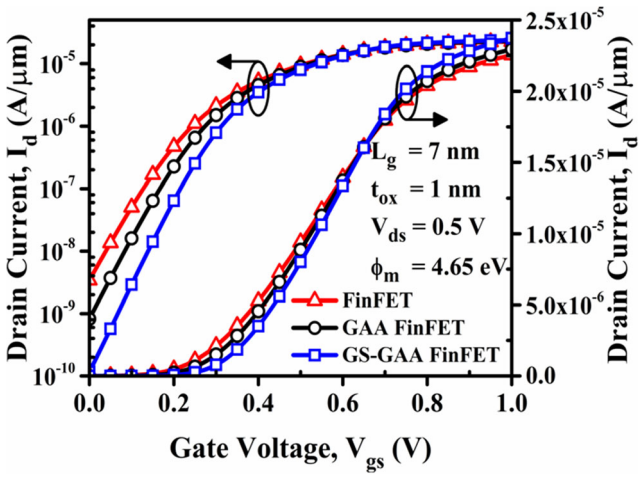

Fig. 4 Variation of I_d-V_{gs} in linear and log scale for different configurations

$$TGF = g_m / I_d \tag{2}$$

$$g_d = \partial I_d / \partial V_{ds} \tag{3}$$

$$V_{EA} = I_d / g_d \tag{4}$$

$$A_v = g_m / g_d = (g_m / I_d) \times V_{EA} \tag{5}$$

Figure 9 represents a combined plot of drain current and output conductance as a function of a drain to source voltage at constant $V_{gs} = 0.5$ V. Output conductance determines the driving ability of a device, as defined in Eq. (3) [29]. The region of device operation determines the value of output conductance. Initially, g_d is large in the linear region but keeps on decaying as V_{ds} increases beyond pinch-off voltage due to drain-induced-barrier-lowering (DIBL) and channel length modulation (CLM) [31]. In the saturation region, g_d maintains a constant value. Thus, due to increased gate controllability and suppressed short channel effects, g_d is minimum for GS-

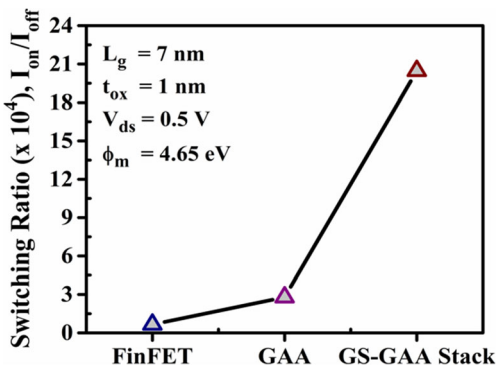

Fig. 5 Switching (I_{on}/I_{off}) ratio comparison for different structures

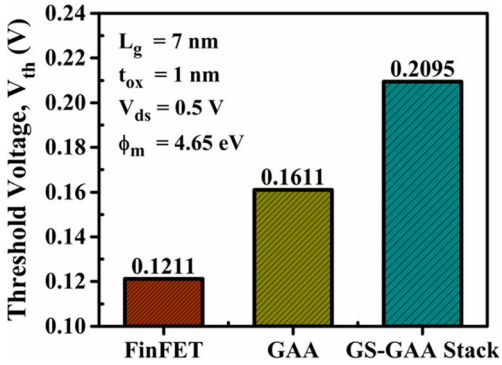

Fig. 6 Threshold Voltage (V_{th}) comparison for different structures

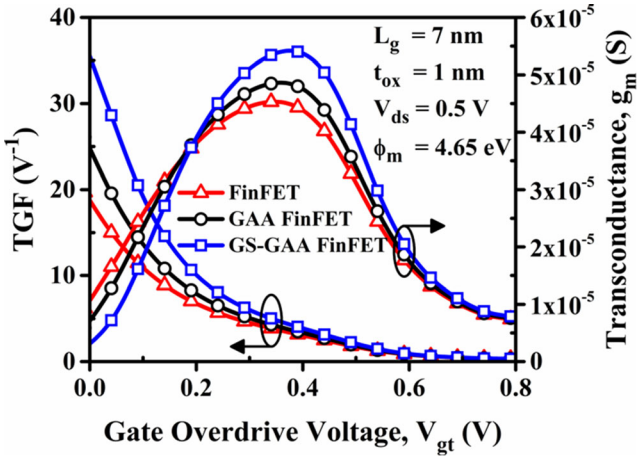

Fig. 8 TGF and g_m vs gate overdrive voltage (V_{gt}) for different structures

GAA FinFET when compared to their counterparts. Moreover, as depicted in Fig. 9, lower g_d means higher output resistance, which means less increase in drain current with V_{ds} in the saturation region.

Early voltage and intrinsic gain are evaluated using Eqs. (4) and (5), respectively, and they must be as high as possible for the enhanced analog performance of the device [29]. Figure 10 shows the variation of early voltage and intrinsic gain against V_{gt} for all three configurations. The maximum value of early voltage is obtained for GS-GAA FinFET structure due to the reduction in short channel effects, as demonstrated in Table 2. Also, the highest peak of intrinsic gain is observed for GS-GAA FinFET because of higher g_m and lower g_d.

4.3 RF Performance

From the RF application's point of view, RF parameters of vital interest are cut-off frequency (f_T), maximum oscillation frequency (f_{max}), gain frequency product (GFP), transconductance frequency product (TFP), and gain transconductance frequency product (GTFP). Figure 11 shows the variation of the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of V_{gt}. C_{gs} is plotted in log scale, and C_{gd} is on a linear scale to differentiate between the two curves. AC small-signal analysis has been performed to extract the values of these intrinsic gate capacitances (C_{gs} and C_{gd}) at an operating frequency of 1 MHz with DC voltage ramped from 0 V to 1 V with a step size of 0.05 V. It is observed from Fig. 11 that in the subthreshold region, both intrinsic gate capacitances increase very slowly with V_{gt}, but with further increase in V_{gt}, C_{gs} and C_{gd} increase swiftly due to the enhanced lateral field, which increases the movement of charge carriers from source side to drain side. In the superthreshold region, as expected, C_{gs} and C_{gd} become constant due to the non-contribution of V_{ds}. The GS-GAA FinFET structure exhibits higher C_{gs} and C_{gd} in comparison to other devices because gate capacitance increases with the increase in the dielectric permittivity [32].

In Fig. 12, total gate capacitance (C_{gg}) and cut-off frequency (f_T) are displayed as a function of V_{gt} for all three devices. The variation of C_{gg} with V_{gt} is the same as that of C_{gs} and C_{gd} because C_{gg} is the sum of intrinsic gate capacitances.

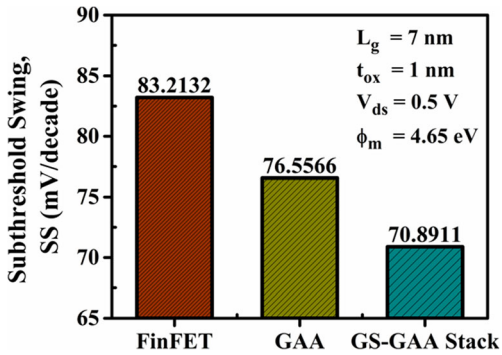

Fig. 7 Subthreshold Swing (SS) comparison for different structures

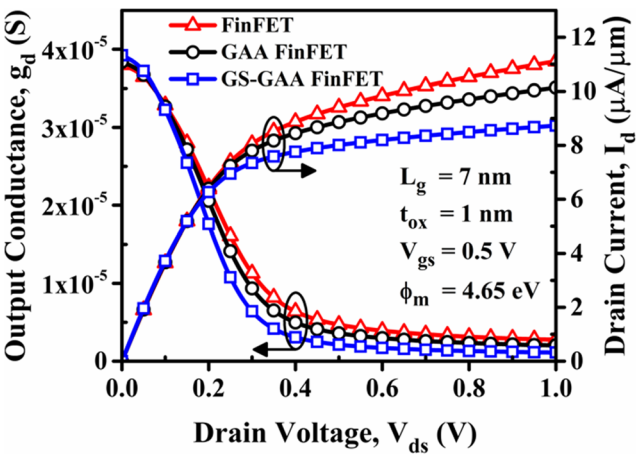

Fig. 9 g_d and I_d vs drain to source voltage (V_{ds}) for different structures

Table 2 Summary of electrostatic and analog parameters for different structures, $V_{ds} = 0.5$ V

Parameter	FinFET	GAA FinFET	GS-GAA FinFET
I_{on} (A/μm)	2.25×10^{-5}	2.29×10^{-5}	2.37×10^{-5}
I_{off} (A/μm)	34.04×10^{-10}	8.22×10^{-10}	1.15×10^{-10}
V_{th} (V)	0.12	0.16	0.20
SS (mV/dec)	83.21	76.55	70.89
g_m (S)	4.52×10^{-5}	4.85×10^{-5}	5.40×10^{-5}
TGF (V^{-1})	19.70	26.09	37.09
g_d (S)	11.29×10^{-6}	9.35×10^{-6}	6.41×10^{-6}
V_{EA} (V)	8.11	11.20	21.10
A_v (dB)	11.30	16.20	32.01

Generally, the frequency at which current gain becomes unity (0 dB) is known as cut-off frequency and is calculated using Eq. (6) [33]. As shown in Fig. 12, f_T decreases slightly for the GS-GAA FinFET structure in comparison to the other two designs. It happens mainly due to the enhanced value of C_{gs} and C_{gd}, although a higher value of g_m significantly compensates the deteriorating f_T.

$$f_T \approx g_m / 2\pi (C_{gs} + C_{gd}) \tag{6}$$

$$f_{max} = f_T / \sqrt{4R_g (g_{ds} + 2\pi f_T C_{gd})} \tag{7}$$

$$GFP = (g_m / g_d) \times f_T \tag{8}$$

Figure 13 represents the maximum oscillation frequency (f_{max}) and gain frequency product (GFP) with respect to V_{gt} for each device structure. The frequency at which maximum unilateral power gain becomes unity (0 dB) is known as maximum oscillation frequency (f_{max}). It is evaluated using Eq. (7) in which f_T, R_g, g_{ds}, C_{gd} denotes the cut-off frequency, gate resistance, drain to source output conductance, and gate to drain capacitance, respectively [34]. The values of R_g, g_{ds}, and C_{gd} are extracted using AC small-signal analysis at an operating frequency of 1 MHz with DC voltage ramped from 0 V to 1 V with a step size of 0.05 V [35, 36]. In Fig. 13, f_{max} is slightly lower for GS-GAA FinFET in the subthreshold and superthreshold region compared to their counterparts. It is due to the enhanced parasitic capacitances in the GS-GAA FinFET structure. Gain frequency Product is an essential parameter used in high-frequency applications, as specified in Eq. (8) [33]. It is noticed from Fig. 13, GFP increases as the gate overdrive voltage increases and then attains a maximum peak before falling to a constant value in the saturation region. GS-GAA FinFET configuration records the highest value of

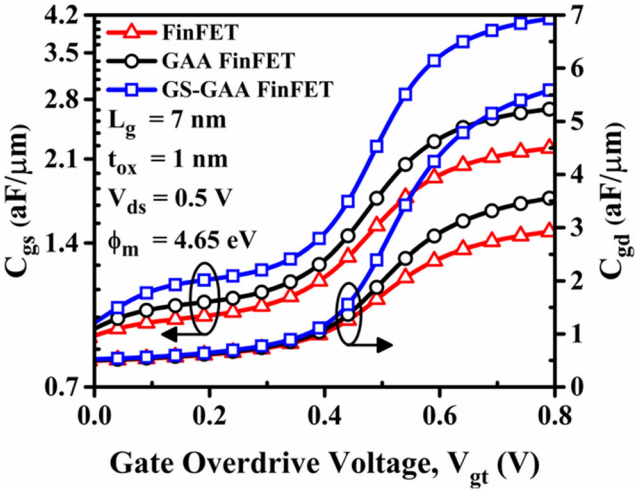

Fig. 11 Variation of C_{gs} and C_{gd} with respect to V_{gt} for each configuration

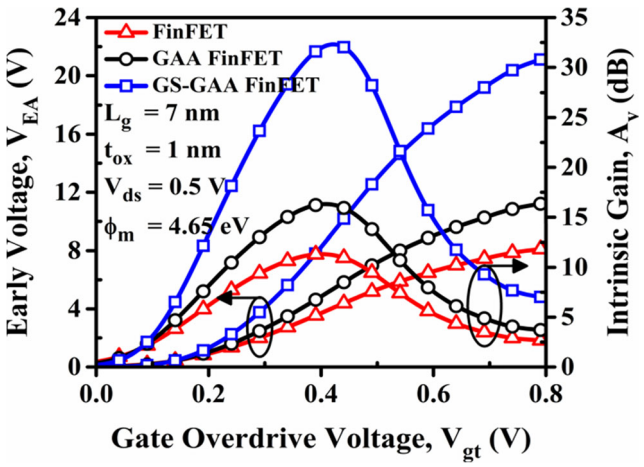

Fig. 10 V_{EA} and A_v vs gate overdrive voltage (V_{gt}) for different structures

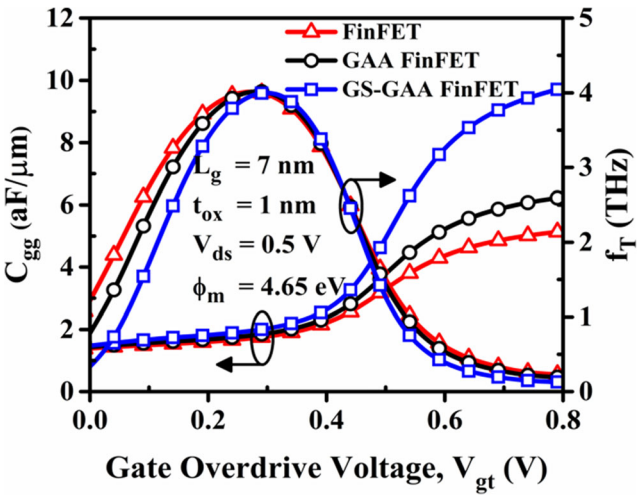

Fig. 12 Variation of C_{gg} and f_T with respect to V_{gt} for each configuration

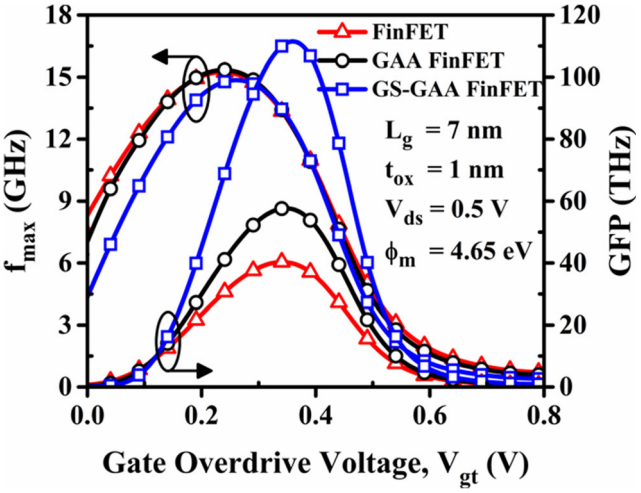

Fig. 13 Variation of f_{max} and GFP with respect to V_{gt} for each configuration

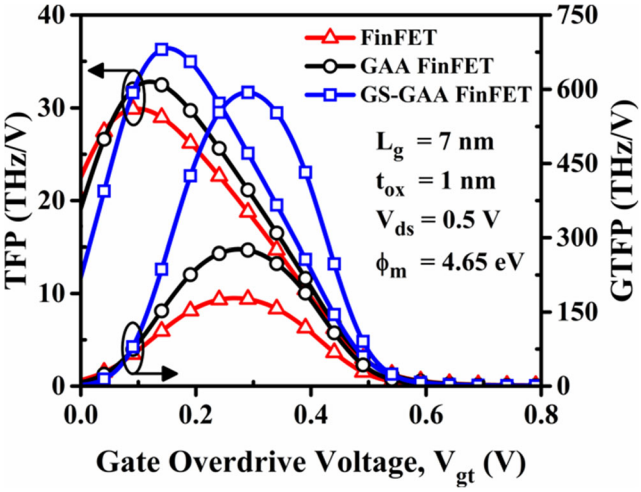

Fig. 14 Variation of TFP and GTFP with respect to V_{gt} for each configuration

GFP due to the improved value of transconductance and output transconductance with a minimal decrease in cut-off frequency.

The other important RF parameters of discussion are transconductance frequency product (TFP) and the gain transconductance frequency product (GTFP), as expressed in Eqs. (9) and (10), respectively [33]. TFP is mainly utilized in high-speed designs as it exhibits an agreement between bandwidth and power [37]. Figure 14 depicts the TFP and GTFP against V_{gt} for each configuration. The graph plotted for GTFP is calibrated by both the intrinsic gain and switching speed. The curve reflects that both TFP and GTFP increases as V_{gt} increases then reaches a maximum value at a particular value of V_{gs}. With further increase in V_{gt}, both TFP and GTFP decreases owing to increment in C_{gg} and maintains a minimum constant value as V_{gt} reaches in a saturation region. Again, for both TFP and GTFP highest value is obtained for GS-GAA FinFET structure due to the enhanced value of g_m, TGF, and reduced value of g_d with almost equivalent f_T. Thus, GS-GAA FinFET is the best suitable structure in terms of speed, transconductance, and gain. In Table 3, the values of different RF parameters are tabulated.

Table 3 Summary of RF parameters for different structures, V_{ds} = 0.5 V

Parameter	FinFET	GAA FinFET	GS-GAA FinFET
C_{gs} (aF/μm)	2.21	2.67	4.12
C_{gd} (aF/μm)	2.92	3.55	5.58
C_{gg} (aF/μm)	5.13	6.22	9.71
f_T (THz)	3.96	3.92	3.79
f_{max} (GHz)	15.2	15.3	14.7
GFP (THz)	40.3	57.5	109.9
TFP (THz)	29.8	32.4	36.2
GTFP (THz)	176	275	593

$$TFP = (g_m/I_d) \times f_T \tag{9}$$

$$GTFP = (g_m/g_d) \times (g_m/I_d) \times f_T = A_v \times TFP \tag{10}$$

5 Conclusion

In this work, we demonstrated the effect of high-κ SiO_2-HfO_2-TiN gate stack on device performance in terms of analog and RF parameters using the SILVACO ATLAS 3D simulator. The proposed JAM GS-GAA FinFET device shows the most improved results with the switching ratio increased by almost thirty-one times in comparison to conventional FinFET. Also, the leakage current and subthreshold swing get reduced by 96.62% and 14.80%, respectively, indicating that JAM GS-GAA FinFET configuration significantly reduces the SCEs. The JAM GS-GAA FinFET structure exhibits a remarkable improvement in analog parameters with A_V, V_{EA}, TGF increased by 183.27%, 160.17%, and 88.27%, respectively. Furthermore, RF parameters like GTFP gets enhanced by 236.93%, GFP by 172.70%, and TFP by 21.47% with a minimal decrease in f_T and f_{max} for GS-GAA FinFET configuration. Thus, from the results obtained in this study, the proposed JAM GS-GAA FinFET device can be considered as an attractive solution for the designing of analog and RF circuits.

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Authors' Contribution All authors contributed to the study conception and design.

Data Availability The above-mentioned authors have all the relevant data associated with this research work and will be dedicated to share that, if they will be asked to do so in future.

Compliance with Ethical Standard All the Ethical Standards have been seen by the authors and will supposed to follow them in future as well.

Conflict of Interests The authors declare that they have 'no known conflict of interests or personal relationships' that could have appeared to influence the work reported in this paper.

Consent to Participate & for Publication Since, the concerned research paper is based for the 'non-life science journal'. So, 'Not Applicable' here.

However, the authors have gone through all policies of journal and consent the authorities for further processing.

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ORIGINAL PAPER

TCAD Temperature Analysis of Gate Stack Gate All Around (GS-GAA) FinFET for Improved RF and Wireless Performance

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Abstract
In this article, we investigated the impact of temperature variation on DC, analog, RF, and wireless performance of Gate Stack Gate All Around (GS-GAA) FinFET using SILVACO Atlas 3D simulator. The GAA structure introduction enhances the switching ratio (I_{on}/I_{off}) by ~152.37% and reduces the subthreshold swing (SS) by ~6.5%. At gate voltage (V_{gs}) ~ 0.725 V, the GS-GAA FinFET device exhibits the ZTC (Zero-Temperature-Coefficient) bias point, i.e., the effect of temperature on drain current gets nullified. DC parameters such as leakage current (I_{off}), on current (I_{on}), SS, and threshold voltage (V_{th}) deteriorate with the rise in temperature. The enhancement in temperature degrades the RF and analog performance of the device by suppressing the parameters like transconductance (g_m), device efficiency (TGF), cut-off frequency (f_T), gain frequency product (GFP), gain-bandwidth product (GBP), etc. The device's wireless performance is analyzed using linearity and harmonic distortion parameters such as gm_3, gm_2, 1-dB compression point, IIP3, VIP3, VIP2, IMD3, HD3, and HD2, and it shows significant improvement as the temperature increases from 300 K to 500 K.

Keywords Analog/RF performance · Gate Stack (GS) · Gate All Around (GAA) FinFET · High-temperature · Quantum effects · Wireless performance

1 Introduction

In recent years, CMOS technology is being aggressively scaled-down and is reaching its fundamental limits. MOSFET's continuous scaling results in increased I_{off} current and short channel effects (SCEs), which deteriorates the device performance [1–3]. FinFET, a "3D" field-effect transistor, emerged as one of the encouraging devices in comparison to other multi-gate devices due to its (1) reduced SCEs owing to increased electrostatic control over the channel by the multiples gates of the device, (2) favourable switching ratio, and (3) increased drive current per unit cross-sectional area [4]. Gate All Around (GAA) structure has been explored further to enhance the performance of the FinFET [5]. As per the International Technology Roadmap for Semiconductors (ITRS) guideline, the GAA structure is also known as the "ultimate structure" [6]. GAA FinFET exhibits increased electrostatic control over the channel, as the channel is covered from all four sides by the gate. Consequently, GAA FinFET shows improved SCEs and can be further scaled-down compared to Tri-Gate (TG) FinFET. Another concern in the continued scaling of CMOS technology is the increment in the gate direct tunneling current with the decreasing gate oxide thickness, resulting in the enhanced off-state leakage current [7, 8]. The most technological solution is the use of high-κ dielectric materials, like ZrO_2 (κ = 25) and HfO_2 (κ = 25) [9, 10].

However, there are certain drawbacks in the head-on deposition of high-κ dielectrics on Si substrate. It includes maintaining the interface's quality between Si substrate and high-κ dielectric, threshold voltage instability, mobility degradation accompanied by below-par subthreshold swings [11, 12]. The implementation of the Gate Stack (GS) configuration resolves the problem. GS architecture inserts a thin SiO_2 layer between the high-κ dielectrics and Si substrate while maintaining the effective oxide thickness constant [13]. Thus, considering all considerations, we propose a Gate Stack Gate All Around (GS-GAA) FinFET.

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Recently, the demand for portable and high battery backup electronic devices has substantially increased. Thus, to maintain the increased demand, there is a need to increase the transistor density in the IC [14]. The heat dissipated in the IC increases considerably with the increase in the transistor density, thereby increasing the operating temperature [15, 16]. When the device dimension reaches below 20 nm, the high temperature can significantly affect the device operation or even damage it. The high-temperature reliability of a device ensures its long durability and stability [17]. Therefore, it is vital to examine the temperature variation impact on the device's RF, analog, and wireless performance for better reliability.

The temperature effect on the digital and analog performance of SOI FinFETs has been investigated extensively [18, 19]. In another simulation study, Das et al. reported that at low temperatures, gate-source overlapped FinFET provides enhanced drain current characteristics [20]. Saha et al. reported the temperature effect on RF/analog and linearity figure of merits (FOMs) in Fe-FinFET [21]. However, to the best of authors' knowledge, no report has been published on the temperature impact on RF, analog, and wireless performance of GS-GAA FinFET. In this article, simulations have been carried out to analyze the temperature impact on various important electrostatic, analog, RF, linearity, and harmonic distortion parameters of GS-GAA FinFET by varying the temperature from 300 K to 500 K in steps of 50 K. We have also shown a comparison between GAA FinFET and Tri-Gate FinFET and highlighted the superior performance of GAA FinFET in terms of enhanced transconductance, increased drain current, improved switching ratio, and reduced subthreshold swing. Starting with the introduction, section 2 narrates the device structure. Section 3 deals with the simulation methodology used and calibration between the simulation data and experimental data. Section 4 analyzes the impact of temperature variation on device performance with concluding remarks in section 5, authenticating the paper's originality.

2 Device Structure

Figure 1(a) displays the proposed 3D structure of GS-GAA FinFET. In contrast, Fig. 1(b) and (c) portrays the vertical and horizontal cross-sectional view cut along the proposed device's silicon fin, respectively. Table 1 exhibits all the device parameters used for simulation. Silicon material is used in the fin structure with width (W_{Fin}) and height (H_{Fin}) of the fin fixed at 5 nm and 10 nm, respectively, thereby following the width quantization property, which says that W_{Fin} must be a multiple of H_{Fin} [22, 23]. A combination of SiO_2 ($\kappa = 3.9$) [10] and HfO_2 ($\kappa = 25$) is used to stacking gate oxide. All the regions are uniformly doped with n-type doping species. The source and drain regions are heavily doped compared to the channel region to reduce the parasitic capacitance [24]. TiN metal gate is considered due to its thermal stability, high purity, low resistivity, and compatibility with CMOS processing [25, 26].

3 Simulation Framework and Calibration

The SILVACO Atlas 3D simulator has simulated the proposed device GS-GAA FinFET. Poisson's and continuity equations expressed by Eqs. (1), (2), and (3) provide the general framework for device simulation [27].

1. Poisson's Equation

$$\mathrm{div}(\varepsilon \nabla \psi) = -\rho \tag{1}$$

where ρ, ψ, and ε represent the space charge density, electrostatic potential, and permittivity. Poisson's equation provides a relation between local space charge density and electrostatic potential.

2. Continuity Equation

For electrons,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}\left(\overrightarrow{J_n}\right) + G_n - R_n \tag{2}$$

For holes,

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\mathrm{div}\left(\overrightarrow{J_p}\right) + G_p - R_p \tag{3}$$

where n and p represent the electron and hole concentration, R_p and R_n are the recombination rates for holes and electrons, G_n and G_p represent the generation rates for electrons and holes. The magnitude of an electron charge is denoted by q, whereas J_n and J_p represent the electron and hole current densities. The way electron and hole densities evolve because of transport, recombination, and generation is described by continuity and transport equations.

But to obtain more realistic and accurate results, secondary equations and physical models are needed. Thus, to correlate the low-field carrier mobility with temperature and impurity concentration, Arora analytical model is used as the temperature has been varied from 300 K - 500 K [28]. SRH recombination model is used to include the recombination and generation effects with a fixed carrier lifetime of 1×10^{-7} s, and to consider the specific properties of highly doped materials, Fermi-Dirac statistics are implemented. Klaassen band to band tunneling model is invoked to consider the tunneling of electrons (both direct and indirect transitions) between valence and conduction band. Crowell-Sze impact ionization model is also enabled [27]. Furthermore, quantum confinement effects play an important role and may not be overlooked in the enormously scaled devices. Thus, Bohm Quantum Potential (BQP) model with alpha = 0.3 and gamma = 1.4 (default parameter values for Si) is employed in the device simulation to consider the quantum confinement effects in the channel region [27, 29]. The physical models and equations

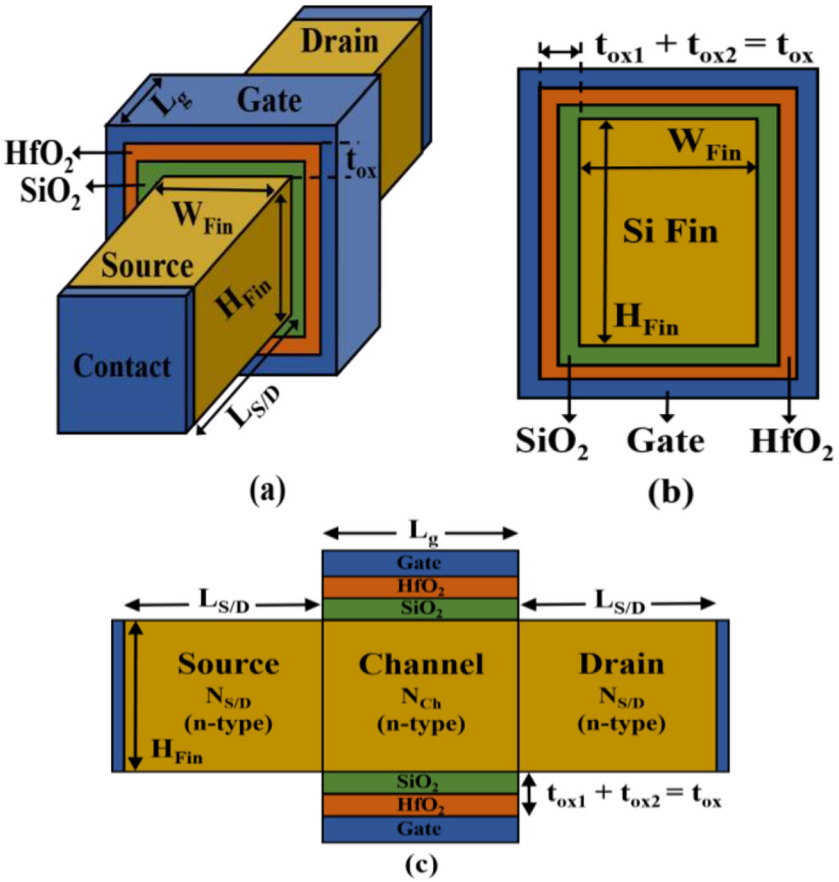

Fig. 1 (**a**) Systematic 3-D structure of the proposed GS-GAA FinFET (**b**) Vertical (**c**) Horizontal cross-sectional view cut along the silicon fin of the proposed GS-GAA FinFET

invoked during the device simulation are shown in Table 2. In SRH recombination, T_L denotes the lattice temperature in Kelvin. The difference between the trap energy level and intrinsic Fermi level is E_{TRAP}, τ_p and τ_n represent the hole electron lifetimes, and k is the Boltzmann's constant. In Fermi-Dirac statistics, ε and E_F represent energy and Fermi level, respectively. In Crowell-Sze impact ionization, λ is the carrier mean free path for optical phonon generation. In Klaassen band to band tunneling, BB.GAMMA, BB.B, BB.A is user-definable parameters, D is a statistical factor, and E represents the magnitude of the electric field. In BQP, n represents electron (or hole) density, α and γ are adjustable parameters, $\hbar$ is Planck's constant, and M^{-1} denotes inverse effective mass tensor.

Table 1 Different Device Parameters Used for Simulation

Device Parameters	GS-GAA FinFET
Gate Length (L_g)	7 nm
Length of Source/Drain Regions ($L_{S/D}$)	10 nm
Width of Fin (W_{Fin})	5 nm
Oxide Thickness (t_{ox})	1 nm
Height of Fin (H_{Fin})	10 nm
Channel Doping (N_{Ch})	1×10^{16} cm^{-3}
Source/Drain Doping ($N_{S/D}$)	5×10^{18} cm^{-3}
Work Function (ϕ_m)	4.65 eV (TiN)
Drain-Source Voltage (V_{ds})	0.5 V
Gate-Source Voltage (V_{gs})	1.0 V

The physical models discussed above have been validated with the published results of Hyunjin Lee et al. [30]. Figure 2(a) reflects the simulated and experimental $I_d - V_{ds}$ characteristics of a 5 nm All-Around-Gate (AAG) FinFET at $V_{gs} = 0.2$ V and $V_{gs} = 0.4$ V. The $I_d - V_{gs}$ characteristics for the same device at $V_{ds} = 1.0$ V is shown in Fig. 2(b). Also, as the focus of the results is on temperature dependence, Fig. 2(c) displays the experimental and simulated $I_d - V_{gs}$ characteristics at two different temperatures [31]. It is visible that the results are well-calibrated. Thus, validating the choice of simulation models used in the device simulation. Furthermore, Fig. 3 displays the fabrication feasibility of the proposed GS-GAA FinFET through a fabrication process flow chart.

4 Results and Discussion

4.1 Performance Comparison between FinFET and GAA FinFET

The device dimension of both FinFET and GAA FinFET is the same, as discussed in section 2. Instead of a gate oxide

Table 2 Physical models and equations included in the device simulation

Models	Equations
Shockley-Read-Hall recombination	$R_{SRH} = \frac{pn-n_{ie}^2}{\tau_p\left[n+n_{ie}\exp\left(\frac{E_{Trap}}{kT_L}\right)\right]} + \tau_n\left[p + n_{ie}\exp\left(\frac{-E_{Trap}}{kT_L}\right)\right]$
Fermi-Dirac statistics	$f(\varepsilon) = \frac{1}{1+\exp\left(\frac{\varepsilon - E_F}{kT_L}\right)}$
Crowell-Sze impact ionization	$\alpha_{n,p} = \frac{1}{\lambda}\exp[C_0(r) + C_1(r)x + C_2(r)x^2]$
Klaassen band to band tunneling	$G_{BBT} = D\ \ BB.A\ \ E^{BB.GAMMA}\ \exp\left(-\frac{BB.B}{E}\right)$
Bohm Quantum Potential	$Q = \frac{\hbar^2}{2}\gamma\frac{\nabla\left[M^{-1}\nabla(n^\alpha)\right]}{n^\alpha}$

stack, only a single layer of SiO_2 is used as the gate oxide for this comparison. Figure 4(a) reflects the performance comparison between FinFET and GAA FinFET in terms of g_m and I_d, and the GAA FinFET structure shows significant improvement in g_m and I_d. This significant increment in I_d and g_m for the GAA FinFET device is because of the reduced SCEs and enhanced control over the channel by the gate. Furthermore, leakage current reduces by ~59.25% in GAA FinFET due to the improved gate coupling capacitances and reduced tunneling current. Figure 4(b) outlines the plot of switching ratio and subthreshold swing (SS) for further performance comparison between FinFET and GAA FinFET. In GAA FinFET, the switching ratio increases immensely by ~152.37% due to the increased drain current and reduced leakage current, and consequently, superior switching speed is obtained for GAA FinFET configuration. The SS reduces by ~6.5% in GAA FinFET due to the increased gate controllability over the channel. On account of these advantages over FinFET, the impact of temperature variation on device scalability, analog, RF, and wireless performance has been presented for the proposed device.

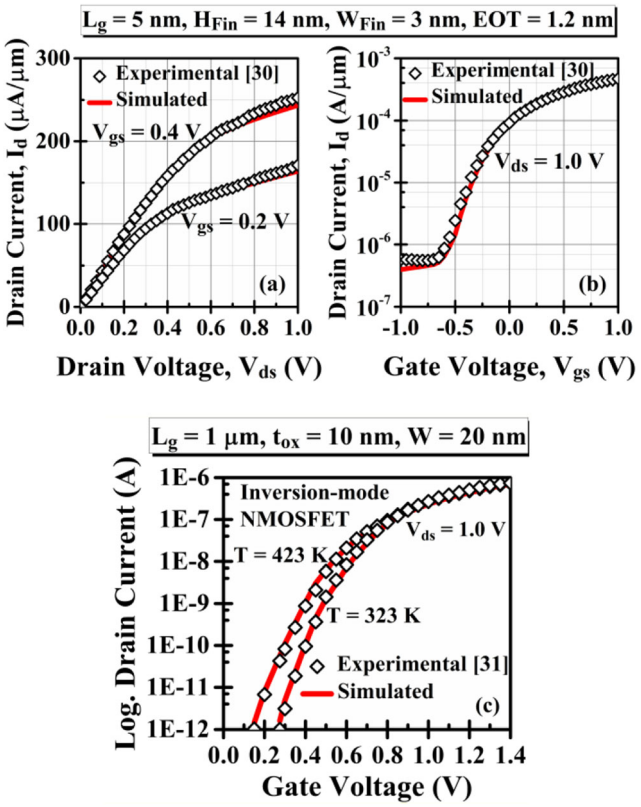

Fig. 2 Calibrated (**a**) I_d-V_{ds} (**b**) I_d-V_{gs} characteristics of 5 nm All-Around-Gate FinFET [30] (**c**) transfer characteristics at two different temperatures [31]

4.2 Temperature Impact on DC Performance in GS-GAA FinFET

Figure 5(a) and (b) display the device's transfer characteristics in linear and log scales for different temperatures. The opposite effect of temperature on drain current (I_d) is observed at high and low gate-source voltages (V_{gs}). At low gate voltage, the energy band gap decreases as the temperature increases, enhancing the device's leakage current. At high V_{gs}, with the temperature rise, the decrease in mobility due to scattering of

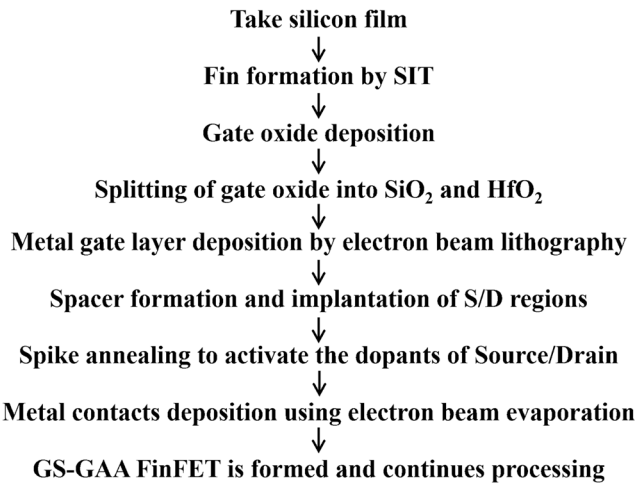

Fig. 3 Fabrication process flow chart of proposed GS-GAA FinFET

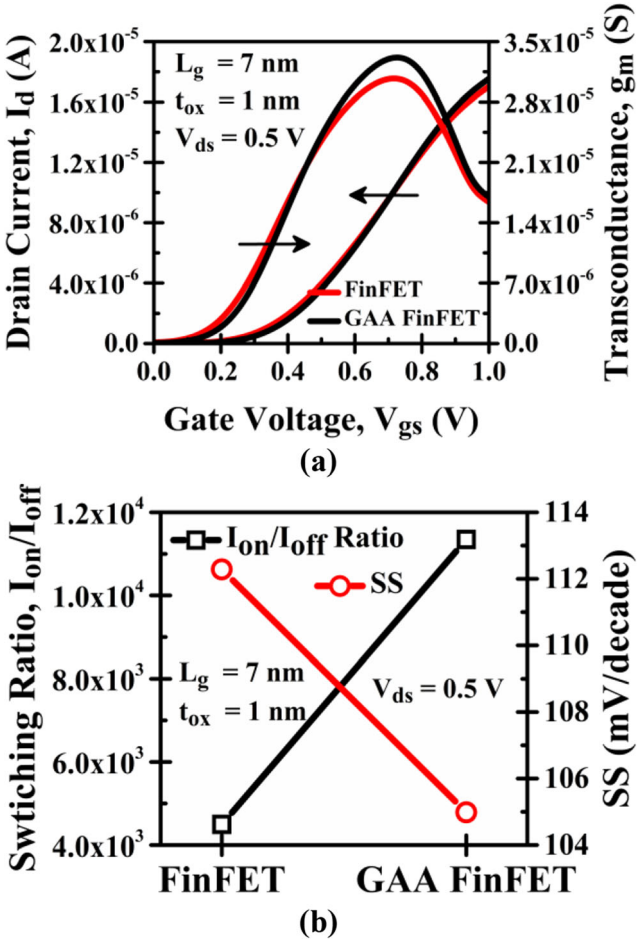

Fig. 4 (**a**) I_d and g_m (**b**) I_{on}/I_{off} ratio and SS comparison between FinFET and GAA FinFET

the carrier dominates over the energy bandgap decrease, resulting in a degradation of on-current (I_{on}) of the device [21]. Thus, an increase in the temperature results in the degradation of both I_{on} and I_{off}, as shown in Fig. 6(a). However, at $V_{gs} \sim 0.725$ V, the impact of temperature variation on I_d gets nullified. Consequently, the ZTC (Zero-Temperature-Coefficient) bias point of the GS-GAA FinFET is at $V_{gs} \sim 0.725$ V [32, 33]. The variation of subthreshold swing (SS) with temperature is portrayed in Fig. 6(b). The subthreshold swing as a function of temperature (Kelvin) is given as SS = (60*T)/300 [34]. Thus, with the rise in temperature, SS increases, resulting in device performance degradation. In Fig. 6(b), the threshold voltage (V_{th}) is plotted against the temperature. The increase in drain current in the subthreshold region with the temperature leads to a decrease in V_{th}. Thus, raising the temperature deteriorates the performance of GS-GAA FinFET in terms of I_{on}, I_{off}, switching ratio, SS, and threshold voltage.

Furthermore, Fig. 7(a) reflects the change in surface potential with temperature along the channel. Surface potential (ϕ_f) is directly related to temperature by the Eq. (4) [17]:

$$\phi_f = \frac{kT}{q} \ln\left(\frac{n}{n_i}\right) \tag{4}$$

where n_i signifies the intrinsic carrier concentration, q denotes the elementary charge, T and k represent temperature, Boltzmann's constant, respectively. The n_i is also dependent on the temperature as $n_i \propto \exp.(-E_g/2kT)$. The increase in temperature increases the intrinsic carrier concentration, resulting in a decreased $\ln(n/n_i)$ term in Eq. (4). Thus, the overall surface potential decreases slightly with the rise in T. The electric field change with temperature along the channel is depicted in Fig. 7(b), and it increases as the temperature is raised from 300 K to 500 K. Also, the electric field at the drain end is significantly lower than the source end, indicating the corner effect's reduction. Figure 8(a) and (b) depicts the corresponding contour profile of the surface potential and electric field with the temperature, respectively.

4.3 Temperature Impact on Analog/RF Performance in GS-GAA FinFET

Figure 9(a) outlines the plot of peak transconductance (g_m) at $V_{gs} = 0.75$ V for temperatures ranging from 300 K to 500 K. Transconductance ($g_m = \partial I_d/\partial V_{gs}$) is a parameter that computes the change in drain current to the shift in V_{gs} at constant V_{ds}. Thus, the transconductance plot shows the same temperature trend as the I_d-V_{gs} plot. At low gate voltage, it increases with an increase in temperature, and at high gate voltage, the opposite behaviour of transconductance is observed. Moreover, it decreases with an increase in temperature owing to the reduction in mobility. The transconductance generation factor (TGF = g_m/I_d) is the proportion of gain generated per unit power loss. A higher value of TGF at low gate voltage indicates a reliable and effective ultra-low-power (ULP) circuit [35]. In the subthreshold region, a higher value of TGF is obtained for all the temperatures considered, as shown in Fig. 9(b), which demonstrates the suitability of GS-GAA FinFET for ULP applications. At low gate voltage, with the increase in T, the increase in I_d is very significant than the rise in g_m, resulting in a decrease in TGF. However, the temperature impact on TGF decreases with an increase in V_{gs} and eventually becomes negligible at high gate voltage.

Figure 9(c) represents the variation of output conductance (g_d) as a function of V_{ds} and T. Output conductance ($g_d = \partial I_d/\partial V_{ds}$) determines the driving ability of a device. It follows the same temperature trend as followed by drain current. At low drain voltage, g_d increases with an increase in temperature and decreases at high V_{ds}. Figure 9(d) reflects the effect of temperature on the early voltage (V_{EA}) as a function of V_{gs}. For the device's enhanced analog performance, early voltage ($V_{EA} = I_d/g_d$) must be as high as possible. In the subthreshold region, the temperature impact on the V_{EA} is almost

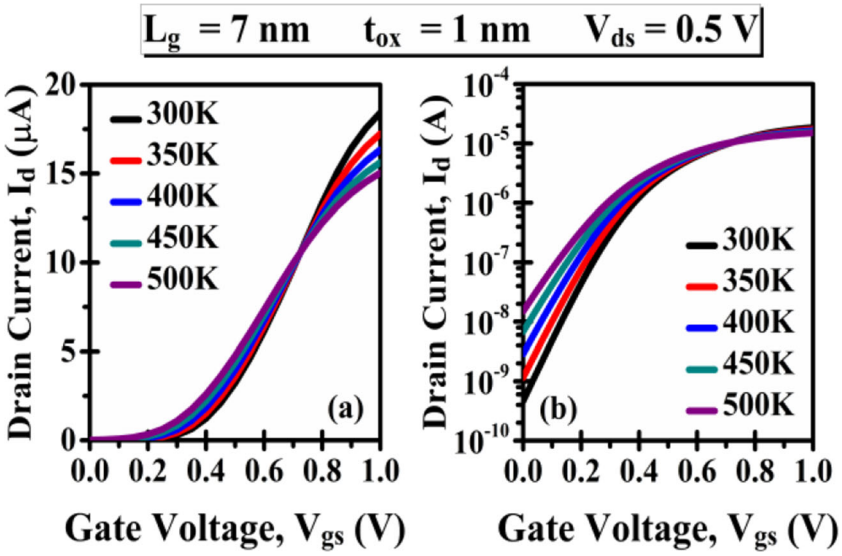

Fig. 5 Impact of temperature variation on transfer characteristics in (**a**) linear scale and (**b**) log scale

negligible. However, early voltage increases with the temperature at a high gate voltage.

Figure 10(a) portrays the temperature impact on total gate capacitance (C_{gg}), and it increases with a rise in T. As the temperature changes from 300 K to 500 K, the carrier concentration in the channel increases due to a reduction in the energy band gap, which increases the charge in the gate region and consequently increases the gate capacitance. The frequency at which current gain becomes unity (0 dB) is the cut-off frequency (f_T) [36]. Figure 10(b) shows the variation of cut-off frequency with T at V_{gs} = 0.65 V. The reduction in peak value of f_T is observed as the temperature is raised from 300 K to 500 K. As expressed in Eq. (5), the main reason for this behaviour is the dependence of f_T on g_m and C_{gg} [37]. The f_T decreases because of an increment in gate capacitance and a reduction in transconductance with temperature. Also, at low gate voltage, f_T increases as temperature rises and falls off at high gate voltage.

$$f_T \approx g_m/2\pi(C_{gs} + C_{gd}) \tag{5}$$

The gain-bandwidth product (GBP) and gain frequency product (GFP) are essential parameters used in high-frequency applications. Figure 11(a) and (b) depict GBP and GFP variation for temperatures ranging from 300 K to 500 K at V_{gs} = 0.65 V. As specified in Eq. (6) and Eq. (7), the peak value of both GBP and GFP decreases with the rise in temperature due to the increment in gate-drain capacitance (C_{gd}) and reduction in transconductance and cut-off frequency [38, 39].

$$GBP = g_m/(20\pi \times C_{gd}) \tag{6}$$

$$GFP = (g_m/g_d) \times f_T \tag{7}$$

$$TFP = (g_m/I_d) \times f_T \tag{8}$$

$$GTFP = (g_m/g_d) \times (g_m/I_d) \times f_T \tag{9}$$

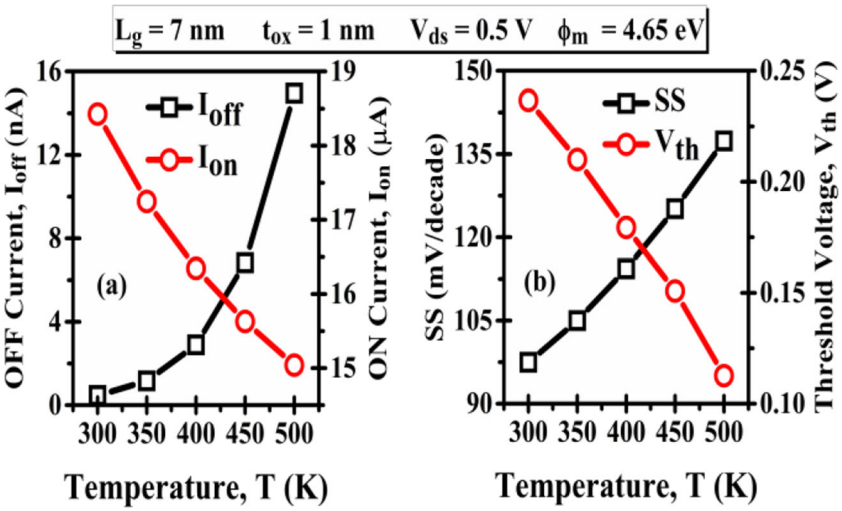

Fig. 6 (**a**) I_{off} current and I_{on} current and (**b**) subthreshold swing and threshold voltage at different temperatures

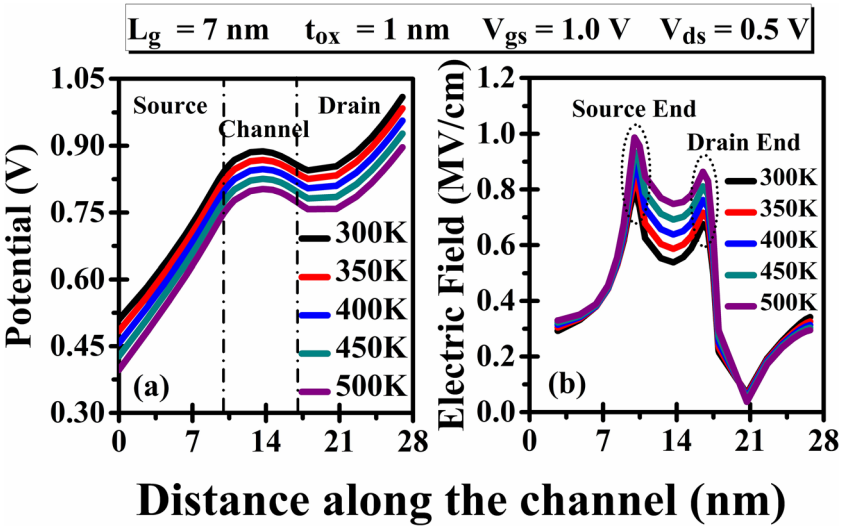

Fig. 7 Impact of temperature variation on (**a**) surface potential and (**b**) electric field

Transconductance frequency product (TFP) is mainly utilized in high-speed designs as it exhibits an agreement between bandwidth and power [40]. In Fig. 11(c), the change in TFP with the temperature is outlined. Transconductance frequency product decreases for higher temperature due to reduced g_m and f_T with a temperature rise, as defined in Eq. (8). Also, TFP shifts towards the low gate bias as temperature changes from 300 K to 500 K due to higher mobility degradation. The gain transconductance frequency product (GTFP) evaluates the complete device performance. As indicated in Eq. (9), GTFP exhibits an agreement between cut-off frequency, TGF, and intrinsic gain. Figure 11(d) displays the temperature impact on GTFP, and as expected, the peak value of GTFP reduces as the temperature is increased from 300 K to 500 K.

4.4 Temperature Impact on Wireless Performance in GS-GAA FinFET

In wireless communication systems, transistors with low distortion parameters are desirable. Linearity is an essential parameter that ensures the least intermodulation and harmonic distortion at the output [41]. The higher-order coefficients of transconductance, i.e., gm_2 and gm_3, provide an estimate about the non-linearity of a transistor. Eq. (10) evaluates these parameters and should be low for better linearity [42].

$$g_{mn} = \left(1/n!\left(\partial^n I_{DS}/\partial V_{GS}^n\right)\right) \quad \text{where, } n = 2, 3 \tag{10}$$

Figure 12(a) and (b) portrays the impact of temperature variation on gm_2, and gm_3 as a function of V_{gs}, respectively. The peak value of gm_2 and gm_3 decreases with the rise in temperature due to the deterioration of short channel characteristics, indicating the device's improved linearity performance. The primary reason for the negative value of gm_2 is the reduction in transconductance at a high gate voltage. The extrapolated gate voltage at which fundamental tone amplitude and second-order harmonic amplitude are equal is VIP2. Similarly, VIP3 is the extrapolated gate voltage at which fundamental tone amplitude is equal to the third-order harmonic amplitude. The high peak value of VIP2 and VIP3, as expressed in Eq. (11) and Eq. (12), respectively, indicates better linearity characteristics of the device [41]. Figure 12(c) and (d) display a plot of VIP2 and VIP3 as a function of V_{gs} for all the temperatures considered, respectively. The peak value of both VIP2 and VIP3 rises with the temperature rise. The reason for this increase is the reduction in gm_2 and gm_3 with the increased temperature.

$$\text{VIP2} = 4 \times (g_m/g_{m2}) \tag{11}$$

$$\text{VIP3} = \sqrt{24 \times (g_m/g_{m3})} \tag{12}$$

The third-order input intercept point (IIP3) is that extrapolated input power at which first and third-order harmonics powers are equal. IMD3, third-order intermodulation distortion, symbolizes the extrapolated intermodulation distortion power at which the first and third-order intermodulation power is equal. Eqs. (13) and (14) evaluates IIP3 and IMD3, respectively [42].

$$\text{IIP3} = (2/3) \times (g_m/(g_{m3}R_s)) \tag{13}$$

$$\text{IMD3} = \left((9/2) \times (\text{VIP3})^2 \times g_{m3}\right)^2 \times R_s \tag{14}$$

where R_s is taken as 50 Ω for analog and RF applications [42].

A high value of IIP3 and a low value of IMD3 are desirable for improved linear characteristics. Figures 13 and 14(a) outlines the impact of temperature variation on IIP3 and IMD3 as a function of V_{gs}, respectively. The value of IIP3 increases with the temperature rise, indicating the improvement in linearity. In the IMD3-V_{gs} plot, for $V_{gs} < 0.5$ V, IMD3 increases

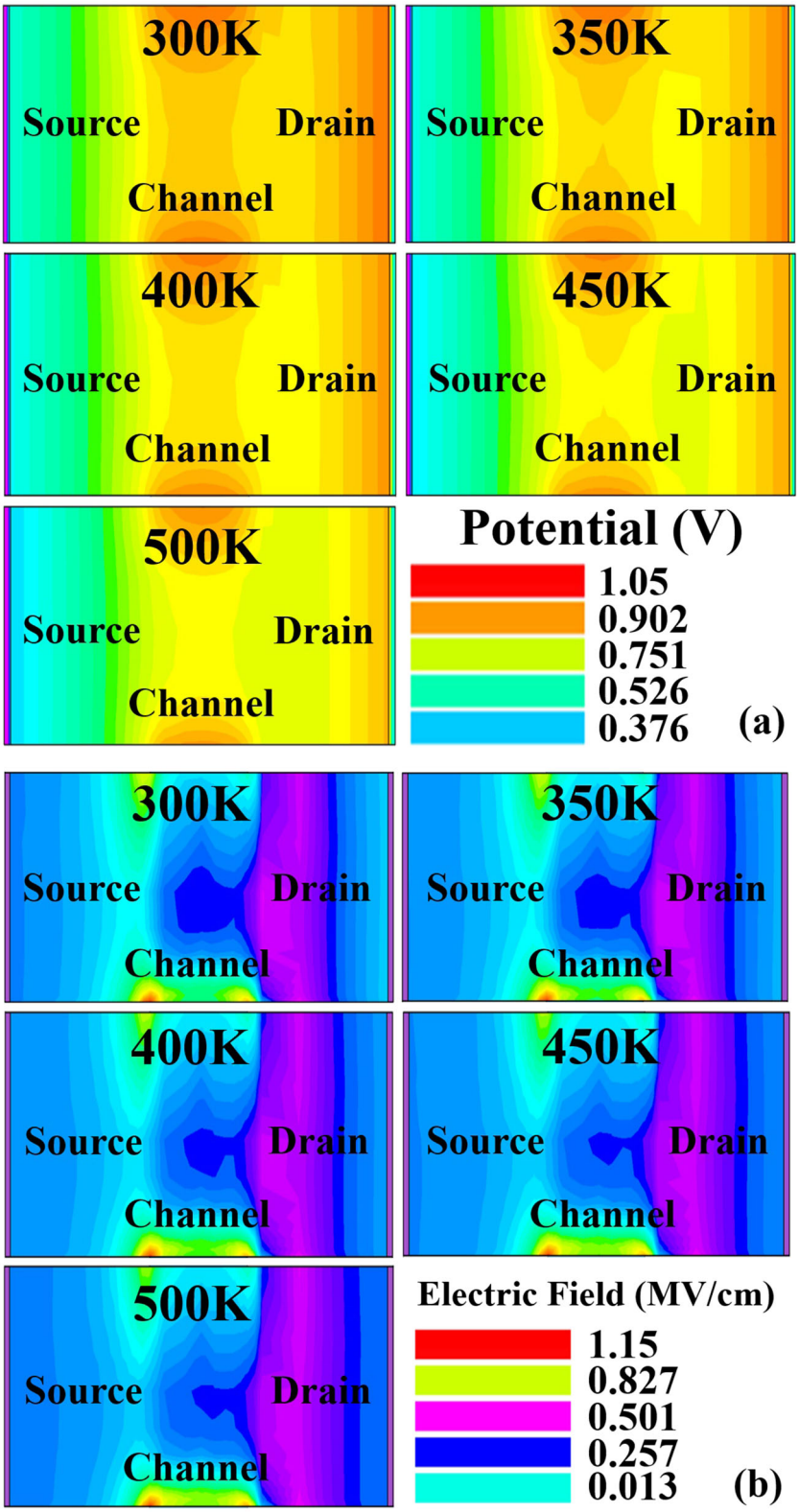

Fig. 8 Contour profile of (**a**) surface potential, and (**b**) electric field at different temperatures

with the temperature, and for $V_{gs} > 0.5$ V, IMD3 decreases with the temperature. Furthermore, at low gate voltage, IIP3 is higher than the IMD3, which implies a reduction in hot carrier effect and improved device performance. 1-dB compression point, as expressed in Eq. (15), is the level of input power at which shifting of output power from linearity by 1 dB occurs. Figure 14(b) reflects the 1-dB compression point variation as a function of V_{gs} and T. The rise in 1-dB

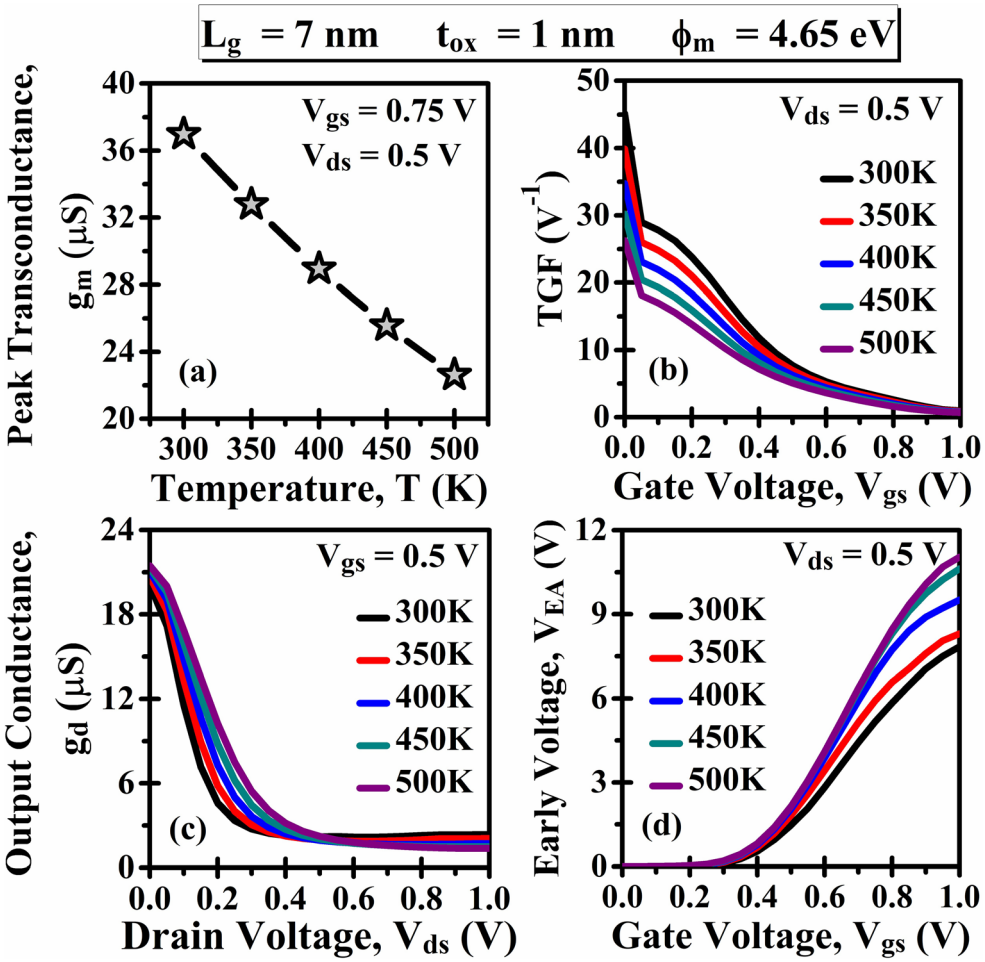

Fig. 9 Impact of temperature variation on (**a**) transconductance (g_m) (**b**) device efficiency (TGF) (**c**) output conductance (g_d) and (**d**) early voltage (V_{EA})

compression point values with temperature indicates superior linearity performance.

$$1\text{−dB compression point} = 0.22 \times \sqrt{(g_m/g_{m3})} \tag{15}$$

$$HD2 = 0.5\ V_a \frac{\left(\frac{dg_m}{dV_{gs}}\right)}{2g_m} \tag{16}$$

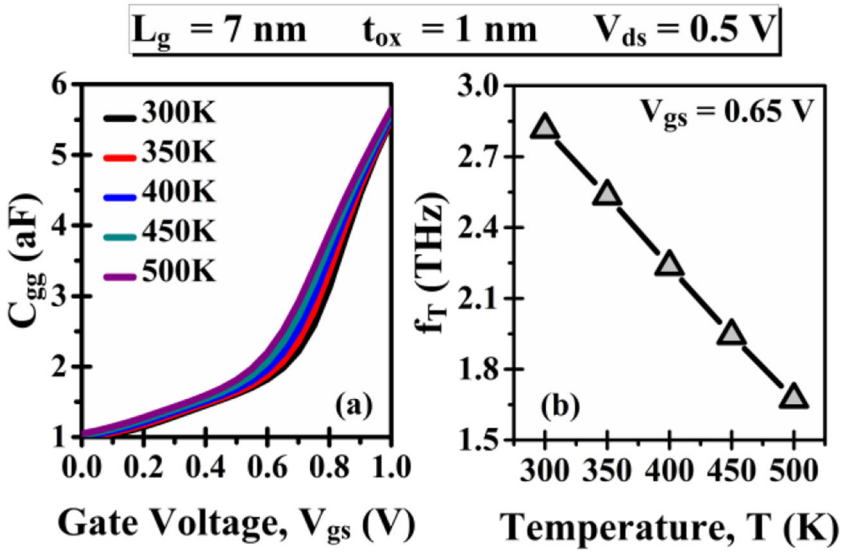

Fig. 10 Impact of temperature variation on (**a**) total gate capacitance (C_{gg}) and (**b**) cut-off frequency (f_T)

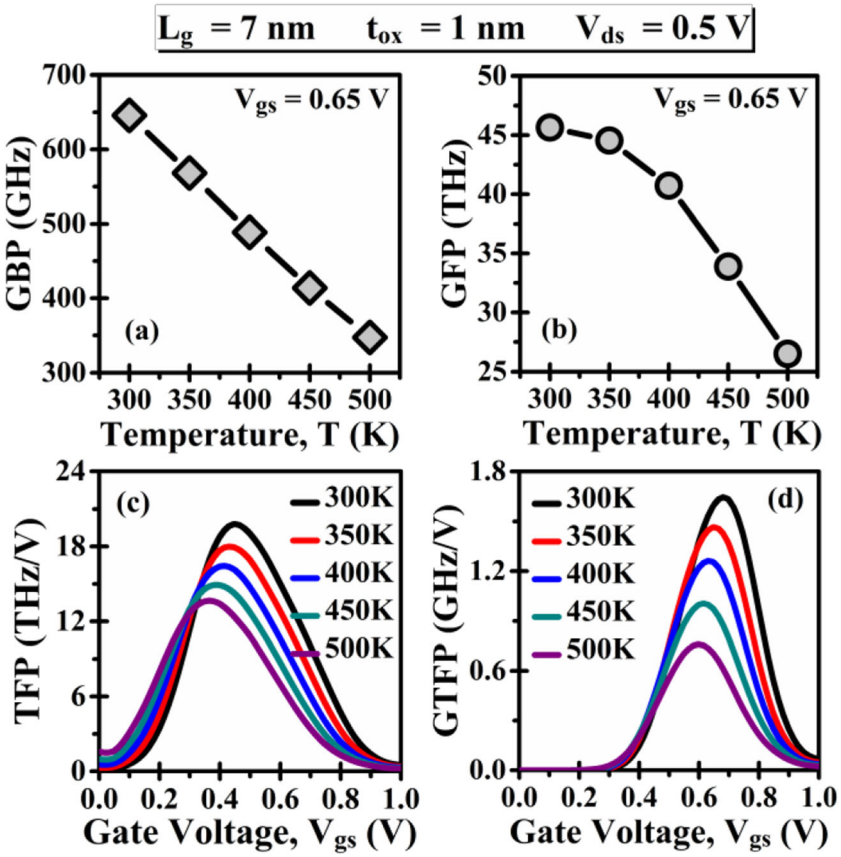

Fig. 11 Impact of temperature variation on (**a**) GBP (**b**) GFP (**c**) TFP and (**d**) GTFP

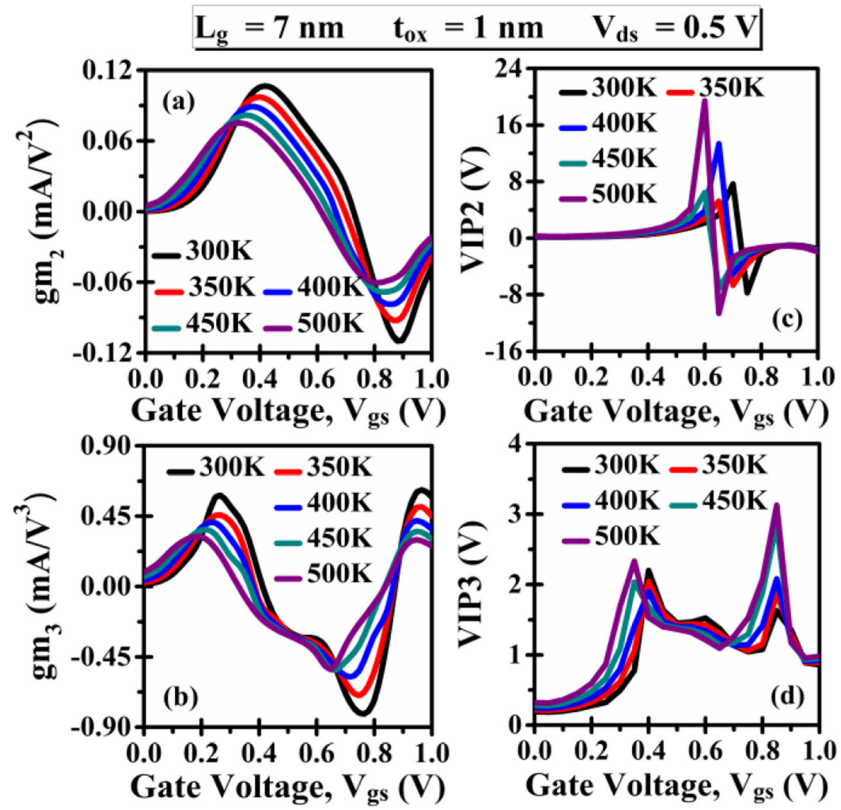

Fig. 12 Impact of temperature variation on (**a**) g_{m2} (**b**) g_{m3} (**c**) VIP2 and (**d**) VIP3

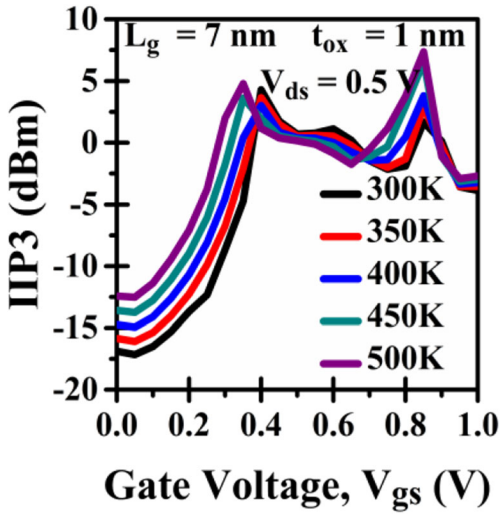

Fig. 13 Impact of temperature variation on IIP3

$$\mathrm{HD3} = 0.25\ V_a^2 \frac{\left(\frac{d^2 g_m}{dV_{gs}^2}\right)}{6 g_m} \tag{17}$$

To evaluate the temperature impact on distortion characteristics, HD2 and HD3 are estimated using the approximate analytical expression given by Eqs. (16) and (17), respectively [43]. The AC signal (V_a) amplitude is taken to be 50 mV [43, 44]. The values of HD2 and HD3 should be as low as possible for lesser distortion in device operation. Figure 14(c) and (d) outlines the temperature impact on HD2 and HD3. The value of HD2 and HD3 decreases with the rise in temperature because, at higher T, due to higher intrinsic carrier density, g_m increases more rapidly than the dg_m/dV_{gs} and d^2g_m/dV^2_{gs}, respectively.

5 Conclusion

It is observed that in GAA FinFET, I_{off} reduces by 59.25%, SS by 6.5%, and I_{on}/I_{off} increases by 152.37% in comparison to TG FinFET. Thus, GAA FinFET can be further scaled-down and is suitable for low-power applications. The ZTC bias point of the GS-GAA FinFET is obtained at $V_{gs} \sim 0.725$ V. The impact of temperature variation on DC, analog, RF, and wireless performance is reported for GS-GAA FinFET. Results revealed that as the temperature rises from 300 K to 500 K, the DC parameters degrade with I_{on} reduced by 18.38%, and SS increased by 40.93%. Analog and RF parameters also deteriorate with the temperature rise with g_m, TGF, f_T, GBP, GFP, TFP, and GTFP reduced by 38.82%, 41.90%,

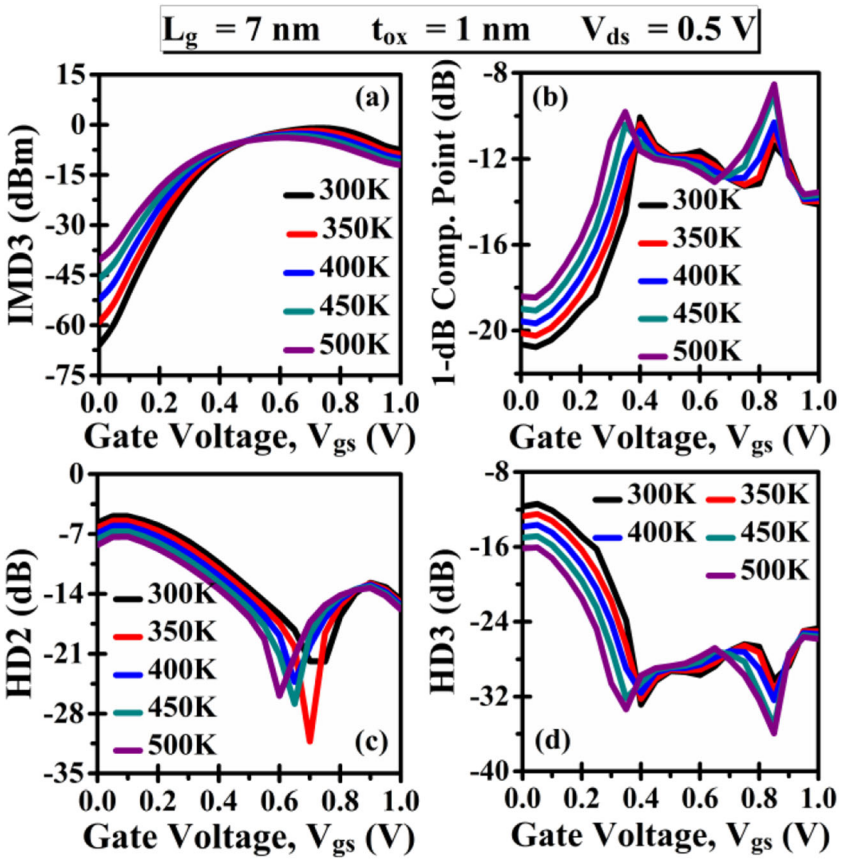

Fig. 14 Impact of temperature variation on (**a**) IMD3 (**b**) 1-dB compression point (**c**) HD2 and (**d**) HD3

40.58%, 46.24%, 41.94%, 31.31%, 53.37%, respectively. On the other hand, with a rise in temperature from 300 K to 500 K, harmonic distortion parameters such as HD3 and HD2 are reduced by 18% approx, and linearity parameters like 1-dB compression point, IIP3, VIP3, VIP2 are significantly improved. Thus, the rise in temperature suppresses the analog, RF performance and enhances the wireless performance of the GS-GAA FinFET.

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Availability of Data & Material The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Authors' Contribution All authors contributed to the study conception and design.

Declarations The authors have seen all the Ethical Standards and will supposed to follow them in the future.

Consent to Participate & for Publication Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here.

However, the authors have gone through all journal policies and consent the authorities for further processing.

Conflict of Interests The authors declare that they have no known conflict of interests or personal relationships that could have influenced the work reported in this paper.

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ORIGINAL PAPER

Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance

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Abstract
This paper optimizes the fin aspect ratio (AR) of Junctionless Accumulation Mode Gate Stack Gate All Around (JAM-GS-GAA) FinFET with constant conducting channel area for upgraded static, analog, and distortion performance. The crucial static and analog parameters, for instance, electric field, potential, band diagram, electron concentration, transconductance, quality factor, drain current, early voltage, intrinsic gain, output resistance, and output conductance, are evaluated and analyzed. The simulated results reveal that the static and analog performance of JAM-GS-GAA FinFET enhances with the increase in the fin AR. Besides, linearity and distortion parameters like voltage intercept points (VIP2, VIP3), 1-dB compression point, zero crossover point, harmonic distortions (HD2, HD3), and total harmonic distortion are explored. It has been noticed that a low fin AR lessens the distortion in the device and improves the device's linearity performance. Moreover, the zero crossover point decreased significantly for the device with low fin AR, which reduces the device operation optimum bias point. Thus, the findings of this paper can help engineers to design 3-D devices according to their needs.

Keywords Distortion Performance · Gate All Around (GAA) FinFET · Junctionless Accumulation Mode (JAM) · Fin Aspect Ratio (AR) · Gate Stack (GS) · Analog Performance

1 Introduction

In modern years, the desire for higher battery backup and portable electronic devices has increased significantly, leading to a gradual reduction in the transistor size [1]. The electronic device's efficiency reduces severely with the transistor size reduction due to unwanted short channel effects (SCEs) [2–4]. Researchers over the years have proposed several multi-gate (MG) device structures, and FinFET has appeared as one of the most encouraging devices to alleviate the SCEs [5]. However, at such small dimensions, the fabrication of sharp junctions is not a straightforward task. The junctionless field-effect transistors (JLFETs) are economical and easy to fabricate [6]. In JLFETs, the problem arises in depleting the channel completely to achieve excellent turn-off characteristics during the OFF state [7]. The relatively low doping concentration in the channel region resolves the issue, but it also decreases drain current accompanied by increased source/drain (S/D) series resistance. Thus, Junctionless Accumulation Mode (JAM) FETs with enhanced source/drain doping are considered [8, 9].

During complementary metal oxide semiconductor (CMOS) scaling, reducing gate oxide thickness beyond a certain level leads to an enhancement in the tunneling gate current [10, 11]. The application of high-κ dielectric materials on a silicon substrate is the best technical solution, although it contains drawbacks like mobility degradation, threshold voltage instability, etc. [12, 13]. Therefore, a Gate Stack (GS) configuration providing a narrow SiO_2 layer to stabilize the high-κ dielectric and silicon substrate without affecting the device's effective oxide thickness is implemented [14]. The device's electrostatic control increases with the addition of the number of gates over the channel. Thus, Gate All Around (GAA) arrangement was introduced to enhance the device performance and sub-threshold characteristics [15, 16]. As a consequence, we have proposed a JAM-GS-GAA FinFET.

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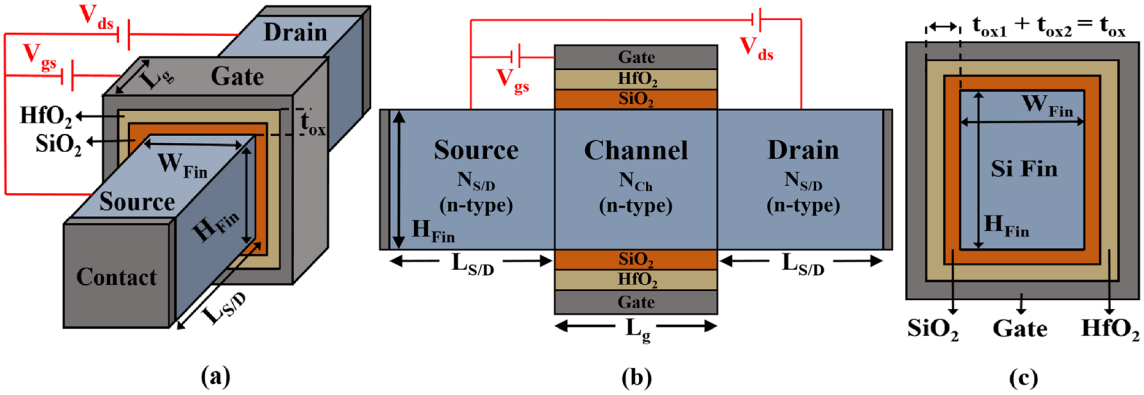

Fig. 1 (**a**) The simulated JAM-GS-GAA FinFET 3-dimensional structure (**b**) horizontal (**c**) vertical 2-dimensional view slit through the device's silicon fin

The System-on-Chip (SoC) technology can handle the increased passive components and transistor density in a single chip to achieve suitable device performance [17]. The system elements are independently incorporated on a semiconductor chip, and optimization of the device is an uphill task with the SoC concept. Therefore, this study aims to determine the optimized fin aspect ratio for upgraded analog and intermodulation distortion performance of the JAM-GS-GAA FinFET. In recent studies, the researchers have demonstrated that alteration of the geometrical parameters such as oxide thickness (t_{ox}), fin width (W_{Fin}), gate length (L_g), fin height (H_{Fin}) primarily influence the FinFET performance [17–19]. The aspect ratio (AR) is an essential geometric parameter in FinFET technology. It is described as the ratio of W_{Fin} to H_{Fin} in a few research papers [17, 20], but we have considered the more precise definition: the ratio of H_{Fin} to W_{Fin}. Because when H_{Fin} is greater than W_{Fin}, the sidewall surface dominates over the top surface, and the device acts as a 3D device. In contrast, the device acts as a planar device when W_{Fin} is greater than H_{Fin} due to the dominance of top surface orientation [21]. In the research conducted on the fin AR, the effective channel area ($H_{Fin} \times W_{Fin}$) has not been kept constant to a particular value while varying W_{Fin} and H_{Fin}. In this scenario, all the related electrical parameters and the channel's conductance will be altered [22]. Therefore, we have kept the device's effective channel area constant to get the exact effect of the fin AR on crucial static, analog, and intermodulation distortion parameters while optimizing the fin AR.

This work is arranged as Section 2 outlines the device structure, Section 3 describes the simulation framework and physical models, Section 4 discusses the experimental calibration and fabrication feasibility of the proposed JAM-GS-GAA FinFET. Section 5 analyses the influence of the fin aspect ratio on the device's various static, analog, and distortion performance parameters with a conclusion note in Section 6 validating the uniqueness of the work.

2 Device Structure

The JAM-GS-GAA FinFET 3-dimensional structure is presented in Fig. 1(a). In contrast, the horizontal and vertical 2-dimensional view slit through the device's silicon fin is represented in Fig. 1(b) and (c). Silicon material is used in the entire fin region. The length of the source/drain regions ($L_{S/D}$) and gate (L_g) are kept constant at 10 nm and 7 nm, respectively. The thickness of the oxide (t_{ox}) is 1 nm with t_{ox1} = 0.5 nm (SiO_2, κ = 3.9) and t_{ox2} = 0.5 nm (HfO_2, κ = 25) [23] are employed to stack the gate oxide. The concentration of the doping in the channel region (N_{Ch}) is 1×10^{16} cm^{-3}, while it is 1×10^{19} cm^{-3} in the source/drain regions ($N_{S/D}$). Every region is doped uniformly with n-type. Due to the presence of the poly-depletion effect in polysilicon gates, metal gates are used these days. Besides that, metal gates have high thermal stability, high purity, and they are also compatible with CMOS processing [24, 25]. Therefore, titanium nitride (TiN) is used as the metal gate with a work function (ϕ_m) equal to 4.65 eV [26]. The effective channel area

Table 1 Different device configurations used for simulation

Config. No.	Fin Height, H_{Fin} (nm)	Fin Width, W_{Fin} (nm)	Effective Channel Area $H_{Fin} \times W_{Fin}$ (nm^2)	Fin Aspect Ratio, AR (H_{Fin}/W_{Fin})
C1	10	8	80	1.25
C2	16	5	80	3.2
C3	20	4	80	5

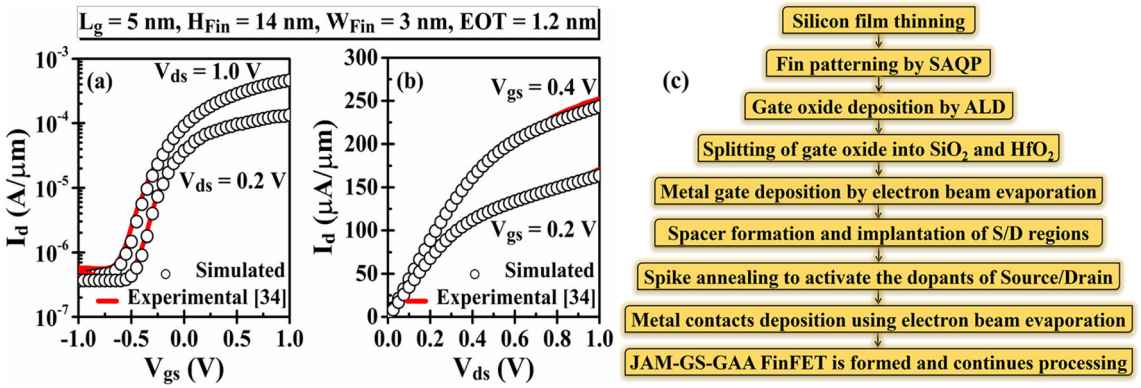

Fig. 2 Experimental and simulated (**a**) transfer (**b**) output characteristics of the All-Around-Gate (AAG) Si FinFET [34] (**c**) JAM-GS-GAA FinFET step-by-step fabrication outline

is constant at 80 nm^2 while varying the fin width and height. Table 1 portrays the three different configurations used for simulation placed in increasing fin aspect ratio order.

3 Simulation Framework and Physical Models

The simulations have been performed in the SILVACO ATLAS 3D simulator [27]. The gate-source voltage (V_{gs}) is varied from 0 to 1 V, whereas drain-source voltage (V_{ds}) and temperature (T) is fixed at 0.5 V and 300 K, respectively, during the entire simulations. Equations (1–5) describes the different physical models included in the device simulation to achieve accurate results.

A. Shockley-Read-Hall (SRH) recombination model includes the effect of recombination and generation [28, 29].

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{E_{Trap}}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-E_{Trap}}{kT_L}\right)\right]} \quad (1)$$

where k signifies the Boltzmann's constant, τ_n and τ_p denotes the electron and hole lifetimes, E_{TRAP} is the difference between intrinsic Fermi level and trap energy level, and T_L is the lattice temperature.

B. Arora analytical model correlates the low-field carrier mobility with impurity concentration and temperature [30].

$$\mu_n = 88\left(\frac{T_L}{300}\right)^{-0.57} + \frac{1252\left(\frac{T_L}{300}\right)^{-2.33}}{1 + \frac{N}{1.432\times10^{17}\left(\frac{T_L}{300}\right)^{2.546}}} \quad (2)$$

where N is the total local dopant concentration and T_L is the lattice temperature.

C. Klaassen band to band tunneling model accounts for the electrons tunneling between valence and conduction band [31].

$$G_{BBT} = D \times BB.A \times E^{BB.GAMMA}\exp\left(-\frac{BB.B}{E}\right) \quad (3)$$

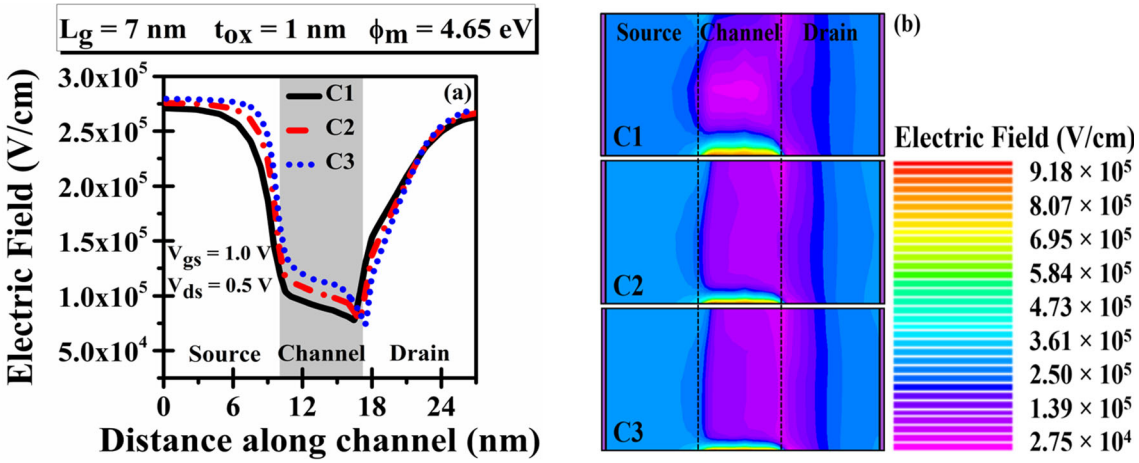

Fig. 3 (**a**) Change in the electric field with the channel distance (**b**) electric field contour plot for each configuration considered

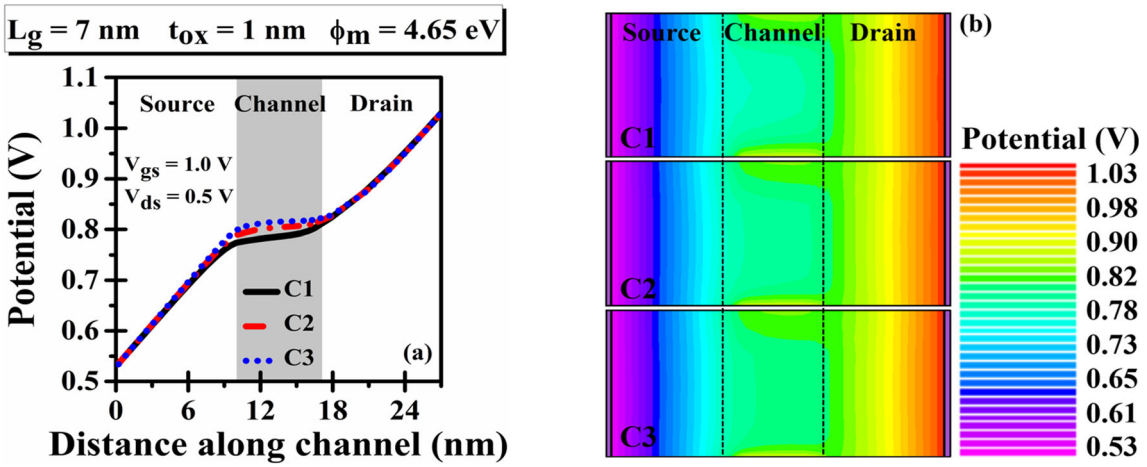

Fig. 4 (**a**) Potential profile variation along the channel distance (**b**) potential contour of all three configurations

where E signifies the electric field magnitude, D denotes statistical factor, and BB.A, BB.B, BB.GAMMA, are user-definable parameters.

D. Crowell-Sze impact ionization model introduces the impact ionization effects [32].

$$\alpha_{n,p} = \frac{1}{\lambda}\exp\left[C_0(r)+C_1(r)x + C_2(r)x^2\right] \quad (4)$$

where λ denotes the carrier mean free path for optical phonon generation.

E. Fermi-Dirac statistics model enhances the result accuracy [33].

$$f(\varepsilon) = \frac{1}{1+\exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \quad (5)$$

where E_F indicates the Fermi level and ε represents energy.

Additionally, Newton and Gummel's methods are used to achieve a solution [27].

4 Experimental Calibration and Fabrication Feasibility

The All-Around-Gate (AAG) Si FinFET is calibrated with the experimental data extracted from Hyunjin Lee et al. [34] to validate the above-discussed physical models. We have calibrated the experimental data by considering silicon material in the entire fin region with fixed device dimensions (L_g = 5 nm, H_{Fin} = 14 nm, and W_{Fin} = 3 nm) as mentioned in the paper to authenticate the simulations. Figure 2(a) and (b) describes the experimental and simulated transfer and output characteristics of the All-Around-Gate (AAG) Si FinFET, respectively. The selection of simulation models is validated due to the close agreement between the experimental and simulated data sets.

Furthermore, the step-by-step device fabrication outline of JAM-GS-GAA FinFET is displayed in Fig. 2(c) to demonstrate the fabrication feasibility of the proposed device. The initial step is to thin the silicon film followed by fin patterning using the self-aligned quadruple patterning (SAQP) method [35]. When two self-aligned double patternings (SADP) are applied in a row to enhance the feature density, it is known as

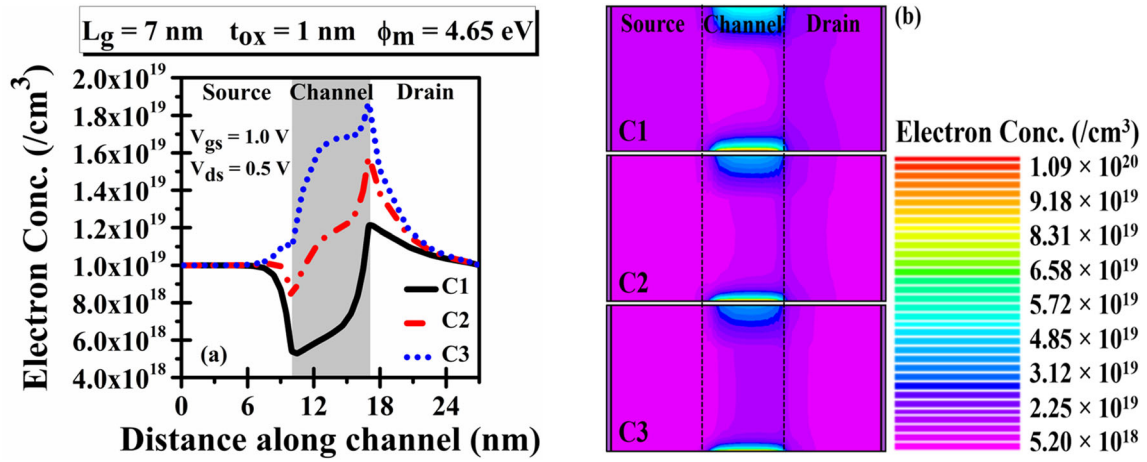

Fig. 5 (**a**) Electron concentration plot against the distance along the channel (**b**) electron concentration contour profile of each simulated device

SAQP. The gate dielectric (SiO_2/HfO_2) is deposited on the silicon interfacial layer by atomic layer deposition (ALD) [36]. Then TiN metal gate is deposited using electron beam evaporation at room temperature on the top of the gate dielectric [36]. The source and drain regions are implanted and then spike annealed to activate the source and drain region dopants. The source/drain metal contacts are deposited by electron beam evaporation followed by lift-off. The JAM-GS-GAA FinFET is formed and continues processing.

5 Results and Discussion

5.1 Fin Aspect Ratio Optimization for Static Performance

It is essential to evaluate the vital static parameters like the electric field, energy band profiles, potential, electron concentration, etc., to precisely examine the device performance. Therefore, in this subsection, discussed static parameters are examined to optimize the fin AR for superior device performance. The electric field alteration with the channel distance for each configuration is displayed in Fig. 3(a). A lower electric field is acquired at the drain end compared to the source end. In addition, because of the almost same electric field at both drain and source end for each configuration, the channel region charge carriers accelerate, resulting in an enhanced electron injection velocity from the source to the channel region [37–39]. A higher electric field is witnessed for the C3 configuration compared to their counterparts in the channel region. Figure 3(b) reveals the contour plot of the electric field for all three configurations, which confirms the rise in the electric field with the fin AR increase.

The potential profile along the channel distance for the respective configurations is plotted in Fig. 4(a). Due to the lower electric field at the drain end compared to the source end, potential improves significantly in the channel region for the C3 configuration, indicating a boost in the device potential with the increase in the fin AR. The equivalent potential contour for all three configurations is presented in Fig. 4(b), which confirms the increase in potential with the rise in the fin AR. Figure 5(a) portrays the plot of electron concentration against the distance along the channel for each mentioned configuration. It is evident from the graph that for the C3 configuration, electron concentration increases massively in the channel region due to the decreased electric field at the drain end compared to the source end. This surge in the concentration of electrons inside the channel region with the fin AR enhances the current drivability and improves the leakage current. The electron concentration contour profile of each simulated device is presented in Fig. 5(b).

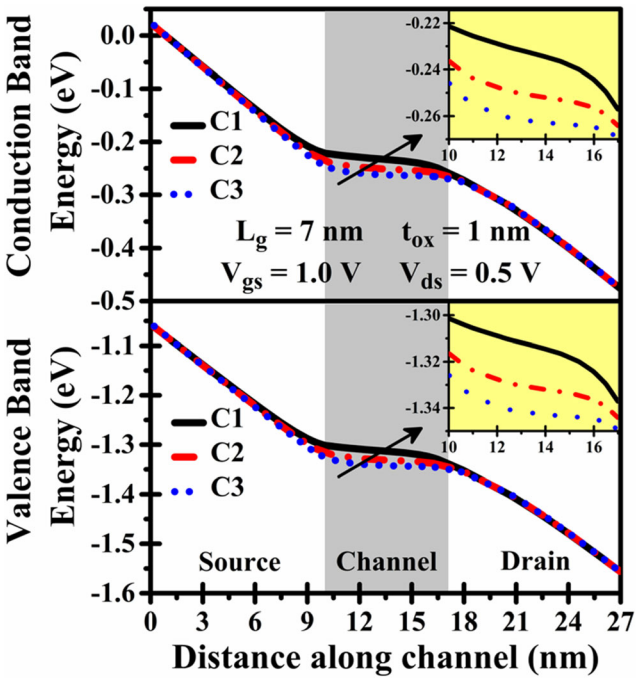

Fig. 6 Conduction and valence band energy against the distance across the channel for all the three simulated devices

Conduction and valence band energy is extracted and represented against the distance across the channel for all the three simulated devices in Fig. 6. It is observed that in the channel region, conduction and valence band energy reduces with the rise in the fin AR. The channel region inset graph clearly demonstrates the decrease in the conduction and valence band energy with fin AR, indicating improvement in the ON and OFF current of the device. Thus, discussed static parameters improve appreciably with the fin AR increase, i.e., enhanced device performance is obtained for the C3 configuration.

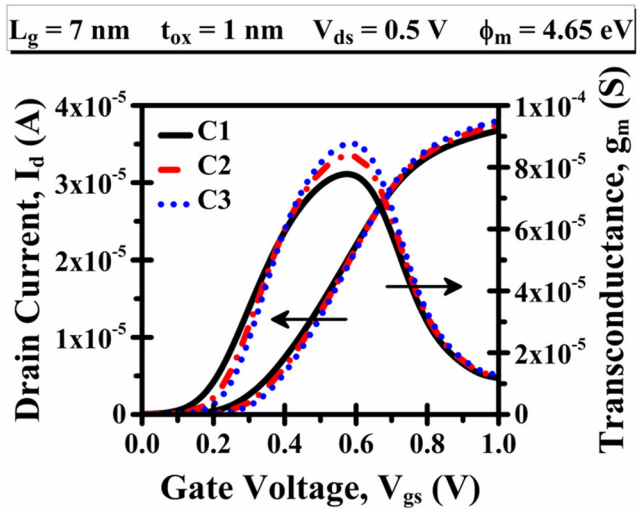

Fig. 7 Plot of I_d and g_m against V_{gs} at a static V_{ds} for each configuration

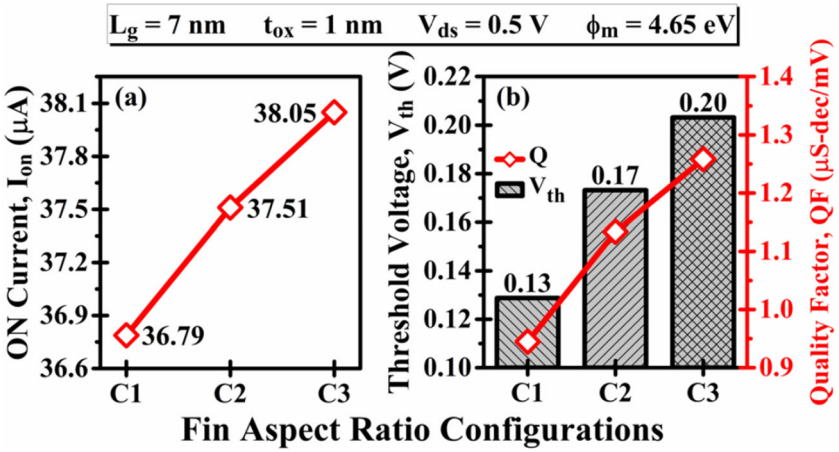

Fig. 8 Change in (**a**) ON current (**b**) threshold voltage and quality factor against different fin aspect ratio configurations

5.2 Fin Aspect Ratio Optimization for Analog Performance

This section optimizes the fin AR for enhanced device analog performance by exploring crucial analog parameters, for instance, transconductance (g_m), quality factor (QF), drain current (I_d), early voltage (V_{EA}), intrinsic gain (A_v), etc. The collaborated plot of I_d and g_m against V_{gs} at a static V_{ds} for each configuration is displayed in Fig. 7. It is observed that compared to the other two simulated structures, the C3 configuration acquires the maximum value of drain current because the current drivability of the device rises with the increase in fin AR. Transconductance (g_m) measures the deviation in the drain current to the gate-source voltage alteration at uniform drain-source voltage, i.e., $g_m = \partial I_d/\partial V_{gs}$ [40]. Figure 7 confirms that transconductance rises with the fin AR increase because of the enhanced drain current and lower electric field at the drain end. Consequently, the C3 configuration displays a more excellent transconductance value than the C1 and C2 configurations.

Figure 8(a) displays the ON current (I_{on}) of the respective configurations, increasing with the fin AR rise. The I_{on} observed for the C3 configuration is 38.05 μA, whereas it is 36.79 μA for the C1 configuration. Thus, when fin AR changes from 1.25 to 5, the device acquires a 3.42 % increase in ON current. Furthermore, Fig. 8(b) demonstrates the threshold voltage (V_{th}) change against the fin AR. The threshold voltage obtained for C1, C2, and C3 configurations is 0.13 V, 0.17 V, and 0.20 V. This points out that V_{th} rises sequentially with the increase in the fin AR, thus enhancing the subthreshold device characteristics. Quality factor (QF) is an additional vital parameter that primarily defines the device switching behavior and is given as QF = g_m/SS, where SS denotes subthreshold swing [41, 42]. The SS attained for C1, C2, and C3 configurations are 81.63 mV/dec, 73.47 mV/dec, and 69.46 mV/dec. The maximum value of g_m (obtained at V_{gs} = 0.6 V) has been considered for the QF evaluation. Figure 8(b) exhibits the QF for all three simulated devices and shows that QF rises with fin AR. This surge in the QF value with fin AR increase is due to the enhanced transconductance and reduced subthreshold

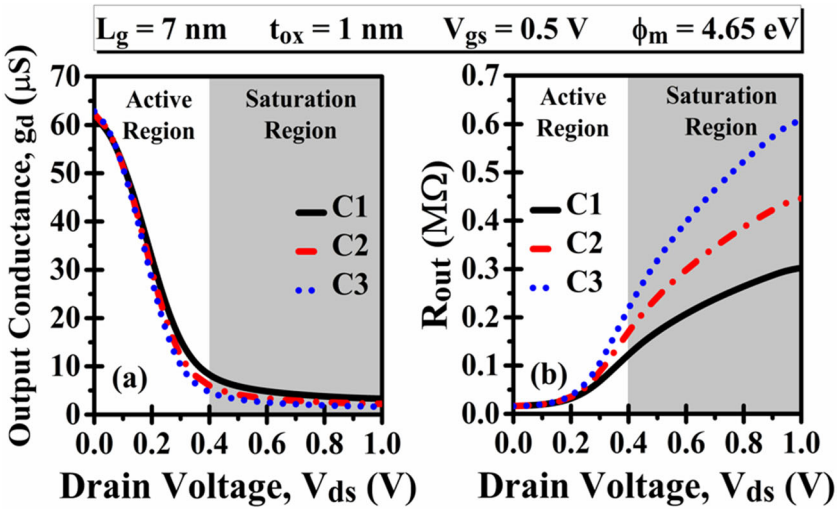

Fig. 9 Variation of (**a**) g_d (**b**) R_{out} against drain-source voltage for each simulated configuration

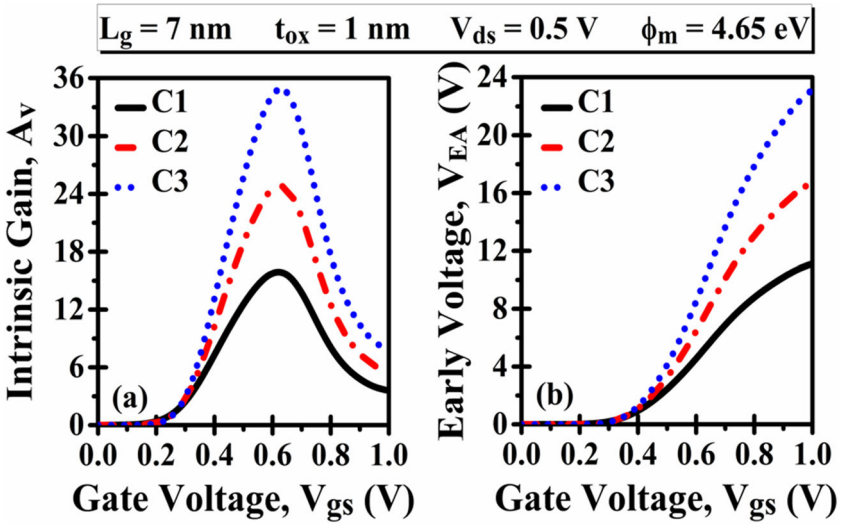

Fig. 10 Alteration of (**a**) A_v (**b**) V_{EA} against fin aspect ratio for all three configurations

swing. Consequently, device switching performance boosts with the increase in the fin AR.

The device's driving ability is estimated by output conductance ($g_d = \partial I_d/\partial V_{ds}$), and its value is determined through the region of device operation [43]. Figure 9(a) represents the output conductance variation against drain-source voltage for each simulated configuration. The g_d decreases with an increase in V_{ds} in the active region before maintaining a constant value in the saturation region. Further, g_d decreases in both active and saturation regions with increased fin AR, demonstrating the suppressed SCEs and improved gate controllability. The converse of output conductance is known as output resistance ($R_{out} = 1/g_d$), and it determines the device's available power gain. The deviation in R_{out} alongside fin AR is displayed in Fig. 9(b). The increment in R_{out} with the increase in fin AR is observed in both regions, with the rise in the saturation region is significantly higher than the active region. Compared to the C1 configuration, the C3 configuration acquires a 77.82 and 101.11 % increase in the active and saturation region.

$$A_V = \frac{g_m}{g_d}; V_{EA} = \frac{I_d}{g_d} \tag{6}$$

Equation (6) evaluates the other crucial analog parameters, i.e., intrinsic gain (A_v) and early voltage (V_{EA}) [43, 44]. To acquire superior analog performance, both these parameters must possess a high value. Figure 10(a) and (b) demonstrate the alteration in A_v and V_{EA} against fin AR for each configuration considered. An extensive enhancement in both the parameters is witnessed with the rise in fin AR. This increase with fin AR is due to the reduced g_d and enhanced g_m and I_d, as shown in Fig. 7. Therefore, superior device performance is attained for C3 configuration, i.e., analog parameters enhance noticeably with the increase in the fin AR, as indicated in Table 2.

5.3 Fin Aspect Ratio Optimization for Linearity Performance

Linearity is necessary to confirm the minimum harmonic distortion and intermodulation at the output [45]. The transistor's non-linearity is evaluated through higher-order derivatives of transconductance, i.e., g_{m2} and g_{m3}.

$$g_{m2} = \frac{\delta^2 I_d}{\delta V_{gs}^2}; g_{m3} = \frac{\delta^3 I_d}{\delta V_{gs}^3} \tag{7}$$

Table 2 Summary of different static (at the center of channel region) and analog parameters of each simulated configurations

Configuration	Parameters									
	Electric Field (V/cm)	Potential (V)	Electron Conc. (/cm^3)	I_{on} (μA)	g_m (S)	QF (μS-dec/mV)	g_d (μS)	Rout (MΩ)	A_v	V_{EA} (V)
C1	0.89×10^5	0.78	6.34×10^{18}	36.79	7.73×10^{-5}	0.95	3.30	0.30	15.91	11.12
C2	1.01×10^5	0.80	1.17×10^{19}	37.51	8.32×10^{-5}	1.13	2.24	0.44	24.97	16.74
C3	1.12×10^5	0.82	1.67×10^{19}	38.05	8.74×10^{-5}	1.26	1.64	0.61	35.27	23.14

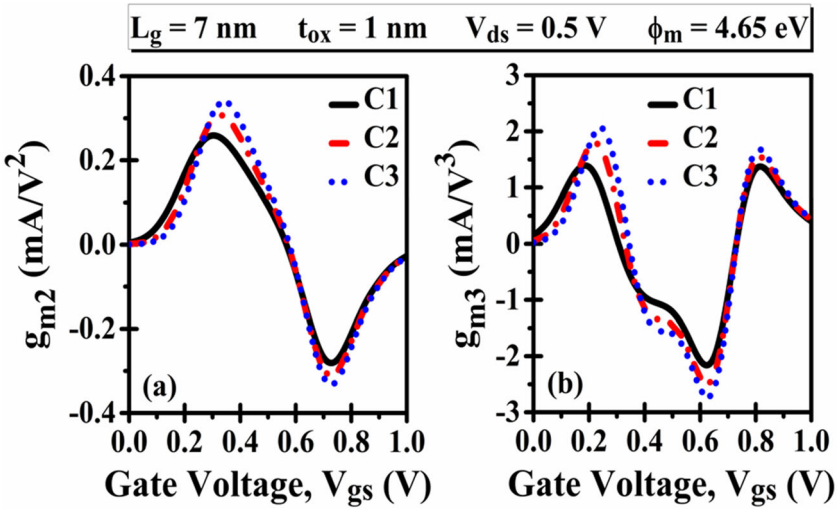

Fig. 11 Variation of (**a**) g_{m2} (**b**) g_{m3} against V_{gs} for each simulated configuration

Equation (7) defines g_{m2} and g_{m3}, and both parameters should be less for improved linearity operation [46]. Figure 11(a) and (b) depict the effect of fin AR on g_{m2} and g_{m3} against V_{gs}. The maximum value of g_{m3} and g_{m2} lessens with the reduction in the fin AR, signifying the enhancement in the linearity performance with fin AR reduction. Equations (8–11) calculates the different linearity parameters such as voltage intercept points (VIP2, VIP3), third-order input intercept point (IIP3), 1-dB compression point [47].

$$\mathrm{VIP2} = \frac{4 \times g_m}{g_{m2}} \tag{8}$$

$$\mathrm{VIP3} = \sqrt{\frac{(24 \times g_m)}{g_{m3}}} \tag{9}$$

$$\mathrm{IIP3} = \frac{2 \times g_m}{3 \times g_{m3} \times R_s} \tag{10}$$

$$1 - \mathrm{dB\ compression\ point} = 0.22 \times \sqrt{\frac{g_m}{g_{m3}}} \tag{11}$$

where R_s is the source-channel resistance with a value of 50 Ω.

VIP2 is the extrapolated gate voltage at which second-order harmonic amplitude and fundamental tone amplitude are equal. Similarly, VIP3 is the extrapolated gate voltage at which third-order harmonic and fundamental tone amplitude is equal. The values of VIP2 and VIP3 should be high for better device linearity characteristics. Figure 12(a) and (b) portrays a plot of VIP2 and VIP3 against V_{gs} for each different configuration. The highest value of VIP2 and VIP3 is attained for the C1 configuration, showing improved linearity performance with decreased fin AR. The inverse proportionality

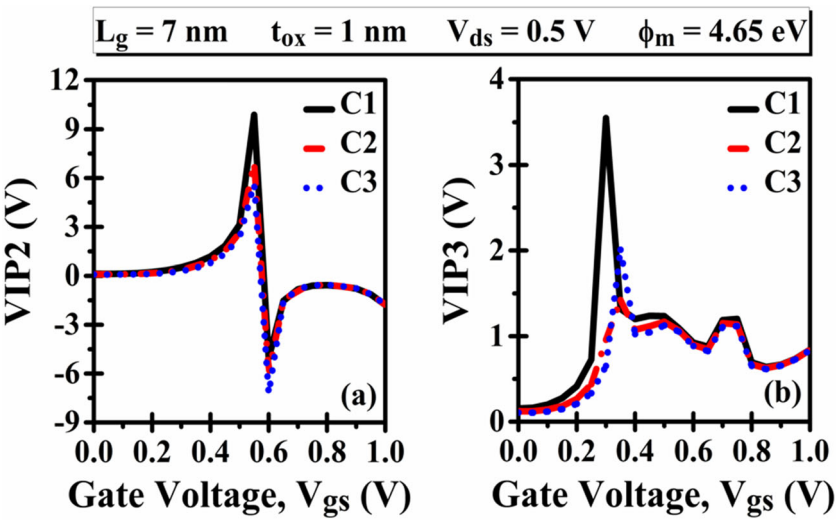

Fig. 12 Alteration in (**a**) VIP2 (**b**) VIP3 against V_{gs} for all three configurations

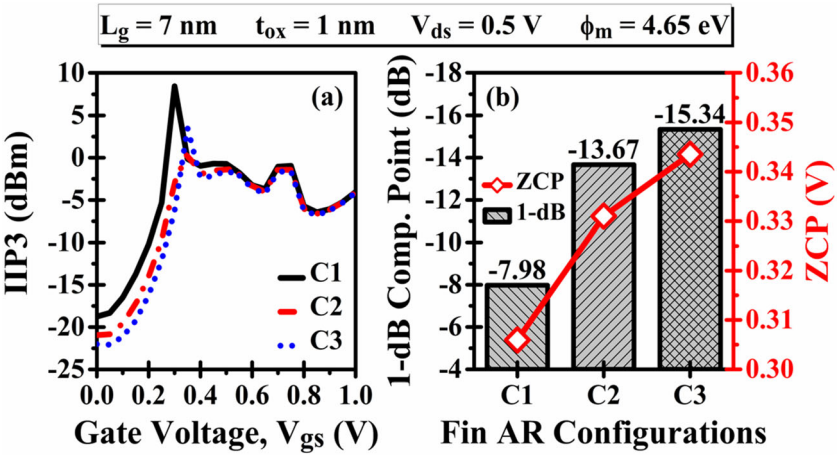

Fig. 13 Plot of (**a**) IIP3 (**b**) 1-dB compression point and ZCP for each configuration

relationship with g_{m2} and g_{m3} is the reason for this increase in VIP2 and VIP3, respectively. Further, the peak value of the C1 configuration is obtained at a lesser value of the V_{gs} that demonstrates superior linearity performance can be obtained with less power for the lower fin AR.

IIP3 is the extrapolated input power at which third and first-order harmonics powers are equivalent. Therefore, IIP3 should be large for better device linearity. Figure 13(a) reflects IIP3 variation against V_{gs} for each configuration considered. The IIP3 maximum value is obtained for the C1 configuration and acquired at a lower gate-source voltage, showing the enhanced linearity characteristics with decreased fin AR. The 1-dB compression point is the input power at which the gain falls by 1 dB from the normal gain. For highly linear applications and to attain maximum gain, 1-dB compression point should have a high value. Figure 13(b) represents the 1-dB compression point variation against V_{gs}. The 1-dB compression point attains the maximum value for C1 configuration, specifying superior linearity performance with decreased fin AR. The zero crossover point (ZCP) is the V_{gs} value for which higher-order derivatives of g_m (g_{m2} and g_{m3}) are zero [48]. The device optimum bias point is determined by ZCP, and it is desirable to be low for better linearity performance. Figure 13(b) represents the ZCP for each configuration, and it shows the distortion is more effectively suppressed in the device with low fin AR. Hence, linearity parameters improve considerably with the fin AR decrease, i.e., superior device performance is attained for the C1 configuration.

5.4 Fin Aspect Ratio Optimization for Distortion Performance

The rise in distortion due to the non-linear device performance in analog/RF applications is a significant concern. Distortion vitiates the strength of the signal by generating unwanted components whose frequency doesn't match the proper band of frequencies [49]. Thus, distortion at the output of a linear amplifier should be as minor as possible. The IFM (Integral Function Method) approach has been used instead of Fourier-based methods to extract distortion parameters as they acknowledge DC measurements in place of AC characterization

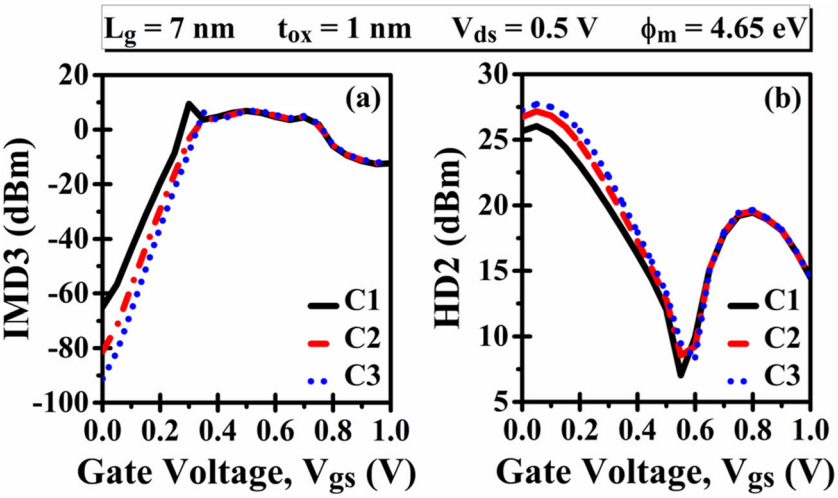

Fig. 14 Variation of (**a**) IMD3 (**b**) HD2 against V_{gs} for each simulated configuration

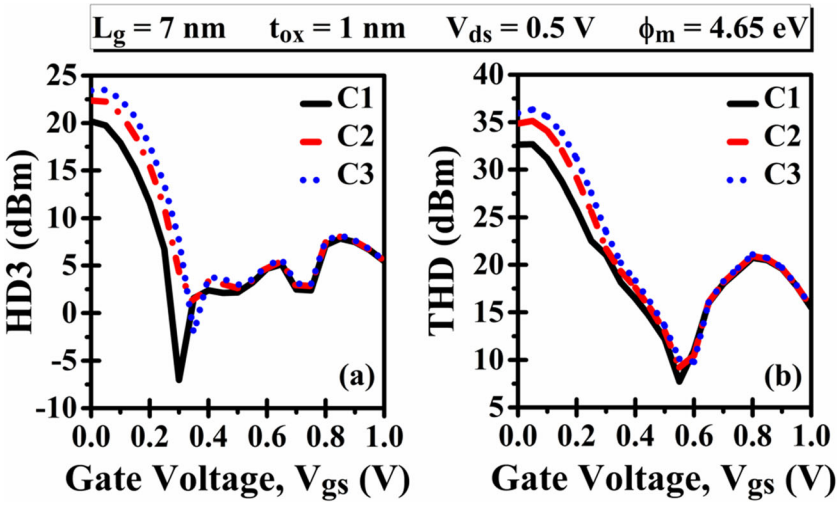

Fig. 15 Alteration of (**a**) HD3 (**b**) THD against V_{gs} for each configuration

[50, 51]. Equations (12–15) provides mathematical relation of several distortion parameters like third-order intermodulation distortion (IMD3), second and third-order harmonics (HD2, HD3), and total harmonic distortion (THD) [50–52].

$$\mathrm{IMD3} = \left[4.5 \times (\mathrm{VIP3})^2 \times g_{m3}\right]^2 \times R_s \tag{12}$$

$$\mathrm{HD2} = 0.5V_a \frac{\left(\frac{dg_m}{dV_{gs}}\right)}{2g_m} \tag{13}$$

$$\mathrm{HD3} = 0.25V_a^2 \frac{\left(\frac{d^2 g_m}{dV_{gs}^2}\right)}{6g_m} \tag{14}$$

$$\mathrm{THD} = \sqrt{(\mathrm{HD2})^2 + (\mathrm{HD3})^2 + \ldots} \tag{15}$$

where R_s is the source-channel resistance with a value of 50 Ω, and V_a is the small AC signal amplitude of about 50 mV.

IMD3 is the extrapolated intermodulation distortion power at which third and first-order intermodulation power are equal. For improved linear characteristics, IMD3 should have a low value [45]. Figure 14(a) reveals IMD3 variation against V_{gs} for each configuration considered. In the IMD3-V_{gs} plot, for lower values of V_{gs}, IMD3 increases with the increase in fin AR, whereas an opposite trend is observed at higher values of V_{gs}. This surge in IMD3 is because the increase in the VIP3 dictates the decrease in the g_{m3} at lower V_{gs} for the C1 configuration.

HD2, HD3, and THD are extracted using the approximate analytical expression to estimate the effect of fin AR on the device harmonic distortion characteristics. These harmonics parameters should have a low value to enhance the gain and linearity of the system and reduce the distortion. Figure 14(b) represents the variation of HD2, whereas the HD3 and THD alteration against gate-source voltage for all three simulated configurations is displayed in Fig. 15(a) and (b). It is witnessed from the simulated results that distortion parameters decrease with the decrease in fin AR, showing the distortion in the device decreases with the fin AR reduction. This decrease in the distortion parameters is because the reduction in higher-order transconductance dominates over the g_m reduction. Consequently, distortions parameters

Table 3 Summary of different linearity and intermodulation distortion parameters of each simulated configurations

Configuration	Parameters										
	g_{m2} (mA/V^2)	g_{m3} (mA/V^3)	VIP2 (V)	VIP3 (V)	IIP3 (dBm)	1-dB Compression Point (dB)	ZCP (V)	IMD3 (dBm)	HD2 (dBm)	HD3 (dBm)	THD (dBm)
C1	0.27	1.48	9.88	3.54	8.44	-7.97	0.30	1.90	25.66	20.18	32.64
C2	0.31	1.81	6.95	1.42	0.50	-13.66	0.33	1.99	26.73	22.37	34.86
C3	0.35	2.26	5.63	2.01	3.50	-15.33	0.34	2.25	27.26	23.44	35.95

boost substantially with the reduction in the fin AR, i.e., better device performance is achieved for the C1 configuration, as mentioned in Table 3.

6 Conclusion

This paper describes the numerical study of JAM-GS-GAA FinFET while optimizing the fin AR for upgraded static, analog, and distortion performance. The C3 configuration (fin AR = 5) exhibits the most improved static and analog performance compared to the two other configurations. Compared with the C1 configuration (fin AR = 1.25), an 18.12 and 33.18 % increase in g_m and QF is observed, while R_{out}, A_v, and V_{EA} are enhanced by more than two times in magnitude for the C3 configuration. On the other hand, lesser distortion and enhanced linearity are acquired for the device with low fin AR, i.e., the C1 configuration. The VIP2 and VIP3 increased by 75.40 and 76.61 % for the C1 configuration compared to the C3 configuration. Besides, for the C1 configuration, linearity parameters like 1-dB compression point and IIP3 get enhanced by 47.99 and 140.80 %. The device's optimum bias point determined by ZCP is reduced by 10.94 % for the C1 configuration. Thus, for RF applications, a device with a high fin AR is beneficial, and for designing less distortion and low-power linear applications, a device with a low fin AR can be considered an attractive solution. So, engineers can design the 3-D devices using the paper's findings, but we also must consider the fabrication limitations while creating such configurations.

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Author Contributions All authors contributed to the study's conception and design.

Data Availability The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Declarations

The authors have seen all the Ethical Standards and will suppose to follow them in the future.

Conflict of Interests The authors declare that they have no known conflict of interests or personal relationships that could have appeared to influence the work reported in this paper.

Consent to Participate & for Publication Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

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Regular Article

Numerical simulation of analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for ULSI switching applications

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Abstract This paper explores the efficacy of Gallium Arsenide (GaAs) as a fin material on the analog metrics and parasitic capacitances of Gate Stack Gate-All-Around (GS-GAA) FinFET. Besides, capacitance-related parameters such as gain–bandwidth product (GBP) and transconductance frequency product (TFP) are also evaluated to analyze the device switching and DC performance. The simulated results validate that compared to Si, GaAs as a fin material increases the switching (I_{on}/I_{off}) ratio by $\sim 10^3$ times and reduces the leakage current, DIBL, and SS by $\sim$ 99%, $\sim$ 50%, and $\sim$ 26%, respectively. Moreover, for GaAs, the peak value of GBP and TFP increases by 9.93 and 11.40 times compared to Si due to the considerable decrease in the parasitic capacitances. Thus, replacing Si with GaAs as a fin material significantly improves the short-channel effects (SCEs) of the device (I_{off}, DIBL, and SS) and capacitances-related parameters (C_{gs}, C_{gd}, C_{gg}, GBP, and TFP). Besides, the impact of gate length (L_g), fin height (H_{Fin}), and fin width (W_{Fin}) of GaAs GS-GAA FinFET on analog metrics and parasitic capacitances are assessed for low power ULSI switching applications. The simulated results reveal that the SCEs and parasitic capacitances improve considerably with decreased L_g, H_{Fin}, and W_{Fin}.

1 Introduction

To meet the ULSI industry's demand, the dimensions of CMOS devices are continuously scaled down and are reaching their fundamental limits. At such small dimensions, short-channel effects (SCEs) such as subthreshold swing (SS), gate leakage current (I_{off}), drain induced barrier lowering (DIBL), etc., start dominating and degrading the device performance [1–4]. Several device structures such as multi-gate MOSFET [5], cylindrical gate MOSFET [6–8], Recessed Channel (RC) MOSFET [9–11], and FinFETs [12, 13] have been proposed to reduce the problems associated with device scaling. FinFET emerged as the most capable device to effectively overcome the SCEs while continuing to downsize CMOS devices to obey the ITRS roadmap's projection [14]. To further escalate the FinFET performance and subthreshold characteristics, gate-all-around (GAA) structure was proposed. As

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the gate covers the channel from all four sides, the channel's electrostatic control shoots up for GAA FinFET [15]. Accordingly, due to the improved subthreshold characteristics, the GAA FinFET device can be scaled down further.

But, considering the scaling limits of FinFETs, further downscaling will be very demanding due to many practical limitations, like parasitic capacitance, threshold voltage roll-off, DIBL, etc. Unsurprisingly, further enhancement in transistor performance and speed while downscaling the device will be possible using new semiconductor materials. Given future logic applications, III-V compound semiconductor materials are the encouraging contender among the new materials [16]. Compared to silicon, GaAs demonstrates many high-caliber electrical properties, for instance, large energy bandgap, high electron mobility, high device on-currents at the low power supply, and a simple hetero-structure approach in microelectronic devices [17, 18]. But, there are some technical challenges associated with using these new wide bandgap semiconductor materials. It includes the need to exploit these materials to their full potential, compete directly against existing silicon power devices, and further development and commercialization. The major hurdle in GaAs-bases devices is (1) infeasible monolithic integration with silicon digital circuitries, (2) no consistent scaling technology driven by a well-planned roadmap [19], and (3) the unavailability of thermodynamically stable, high-quality insulators on GaAs, which can complement the device standards as SiO_2 on Si. However, after years of endeavors, it has been feasible to form a high-quality dielectric on III-V semiconductors with atomic layer deposition (ALD) [20] and molecular beam epitaxy (MBE) [21, 22].

The gate leakage current in a device can be reduced significantly by using a larger energy bandgap gate material which provides a higher potential barrier than other materials of the same thickness. Aluminum oxide (Al_2O_3) is a highly preferable gate dielectric because of its high thermal stability, good interface quality on GaAs, large energy bandgap ~ 9 eV, and it remains amorphous under normal processing conditions [20, 23]. However, the dielectric constant of Al_2O_3 is small and insufficient for aggressive effective oxide thickness (EOT) scaling [24]. To further scale down the EOT, Gate Stack (GS) configuration [25] of high-k dielectric HfO_2 with dielectric constant $\kappa = 25$ [26] and Al_2O_3 $\kappa = 9$ [27] has been formed on GaAs by ALD [28]. Thus, we put forward a Gate Stack Gate-All-Around (GS-GAA) FinFET considering all the considerations.

As the device dimension scales down, the parasitic capacitance becomes more prominent, affecting the performance of the device and making it incompatible for use in low power and switching applications. Thus, there is a necessity to investigate the C-V (capacitance–voltage) measurements besides I-V (current–voltage) measurements to analyze the impact of parasitic capacitances on the performance [29, 30]. In this article, a comparative assessment of parasitic capacitances and analog metrics of GS-GAA FinFET has been performed by undertaking Si and GaAs as fin materials. It is found that on using GaAs as fin material, SCEs and parasitic capacitances are reduced significantly.

The rest of the paper is organized as follows: Section 2 delineates the 3D structure of the device. Section 3 focuses on the simulation framework along with the calibration of experimental and simulation data. Section 4 analyzes the impact of GaAs on device performance in terms of parasitic capacitances and short-channel effects. Further, the impact of gate length, fin height, and fin width variation on parasitic capacitances and analog metrics of GS-GAA FinFET is investigated. Section 5 authenticates the paper's originality with concluding remarks.

2 Device structure

The 3-dimensional systematic structure of the proposed GS-GAA FinFET is displayed in Fig. 1a. The horizontal and vertical 2-dimensional view of GaAs GS-GAA FinFET with parasitic capacitances is shown in Fig. 1b and c, respectively. The channel region is uniformly doped to 1×10^{16} cm^{-3} (n-type), whereas drain and source regions are uniformly heavily doped to 5×10^{18} cm^{-3} (n-type) to reduce the parasitic capacitances [31]. The oxide thickness and gate length are maintained at 1 nm and 7 nm, respectively. Al_2O_3 and HfO_2 are considered in equal proportions to stack the gate oxide, and all the default device parameters are mentioned in Table 1. During the GaAs simulations, width quantization property is followed by maintaining W_{Fin} at a fixed dimension in multiple of H_{Fin} [4, 32]. In the fin region, GaAs and silicon material are incorporated to evaluate GaAs impact on the SCEs and parasitic capacitances. Gate–source voltage (V_{gs}) and drain–source voltage (V_{ds}) are varied from 0 to 1 V and 0 to 0.5 V, respectively. TiN metal gate is taken into account in place of the polysilicon gate because of its compatibility with CMOS processing, low resistivity, high purity, and thermal stability [33–35].

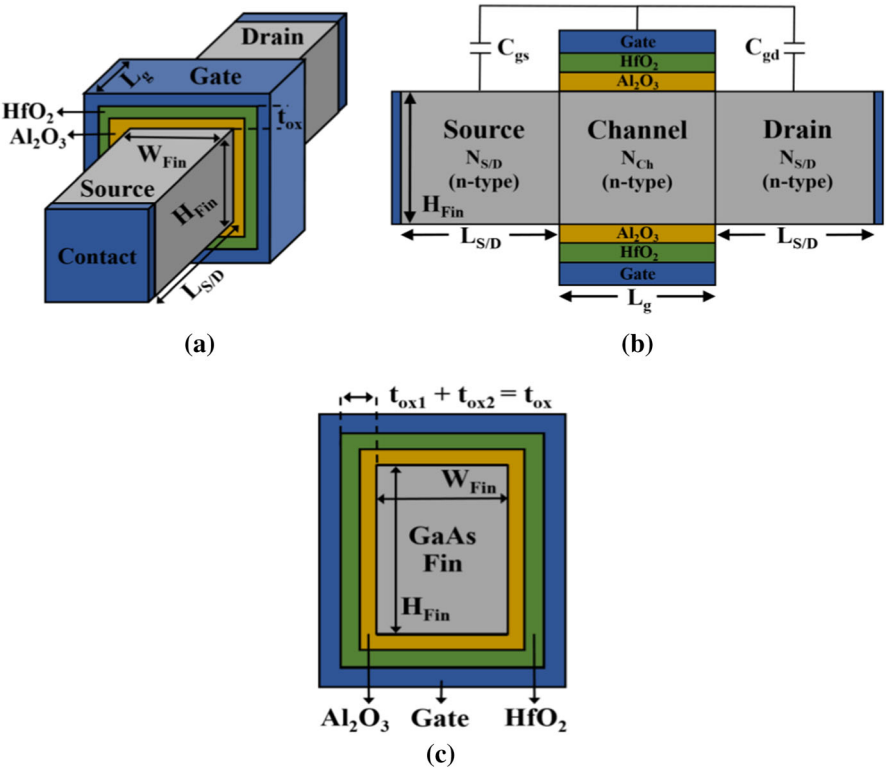

Fig. 1 **a** The systematic simulated 3-D structure **b** horizontal **c** vertical 2-D view of GaAs GS-GAA FinFET with parasitic capacitances

Table 1 Default device parameters of GaAs GS-GAA FinFET

Device parameters	GaAs GS-GAA FinFET
Gate–source voltage (V_{gs})	1.0 V
Drain–source voltage (V_{ds})	0.5 V
Source/drain doping ($N_{S/D}$)	5×10^{18} cm^{-3} (n-type)
Channel doping (N_{Ch})	1×10^{16} cm^{-3} (n-type)
Oxide thickness (t_{ox})	1 nm
Gate length (L_g)	7 nm
Fin height (H_{Fin})	10 nm
Fin width (W_{Fin})	5 nm
Source/drain regions length ($L_{S/D}$)	10 nm
Work function (ϕ_m)	4.65 eV (TiN)

3 Model validation

3.1 Simulation framework

The proposed device GS-GAA FinFET has been simulated by the SILVACO Atlas 3D simulator [36]. The general framework for device simulation is provided by Continuity and Poisson equations. However, secondary equations are also required to obtain more accurate and realistic results. In the aggressively scaled devices, quantum confinement effects become very prominent and cannot be neglected. Thus, Bohm Quantum Potential (BQP) model with gamma = 1.4 and alpha = 0.3 is employed to incorporate the quantum confinement effects [37, 38]. To include the generation and recombination effects, the Shockley–Read–Hall recombination model is implemented with a 1×10^{-7} s fixed carrier lifetime [36]. Fermi–Dirac statistics are included to account for the properties of highly doped materials. To consider both direct and indirect tunneling of electrons between conduction and valence band, the band-to-band Klaassen tunneling model is employed. The concentration-dependent mobility model is enabled to correlate the low-field carrier mobility at 300 K to the impurity concentration. Crowell-Sze impact ionization and bandgap narrowing models are also applied. Further, we have implemented the block and newton's methods to perform all the mathematical carrier transport equations [36].

3.2 Experimental calibration and fabrication feasibility

As the emphasis of this paper is on the effectiveness of GaAs as a fin material, we have extracted the published results of Ye et al. [39] without changing the device parameters to authenticate the simulations. The experimental and simulated output characteristics of Al_2O_3/GaAs MOSFET at $V_{gs} = -1.0$ V and $V_{gs} = -0.5$ V are plotted in Fig. 2a. Besides, the All-Around-Gate (AAG) Si FinFET is calibrated with the experimental data extracted from Hyunjin Lee et al. [40] to validate the above-discussed physical models. The transfer and output characteristics of the same device are portrayed in Fig. 2b and c, respectively. The selection of simulation models is validated due to the close agreement between the experimental and simulated data sets.

Figure 2d exhibits the fabrication feasibility of the GaAs GS-GAA FinFET using a step-by-step fabrication process flowchart. The first step is the GaAs film thinning, and then fin patterning is performed by the self-aligned quadruple patterning (SAQP) technique [41].

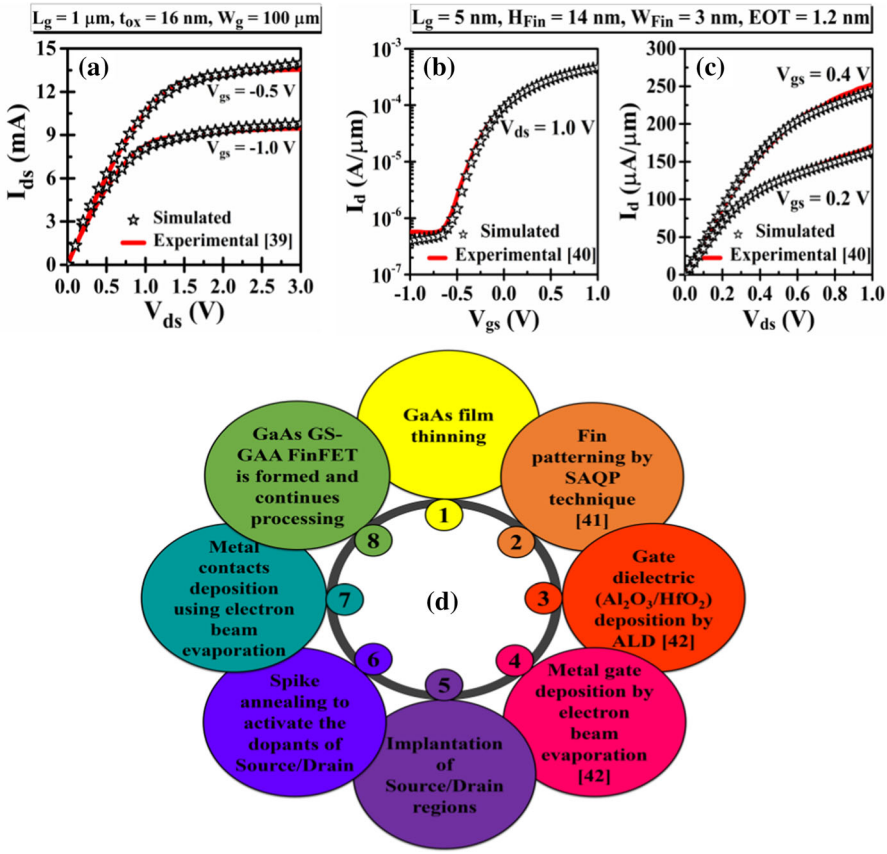

Fig. 2 **a** Experimental and simulated output characteristics of 1 μm gate length Al_2O_3/GaAs MOSFET [39] **b** transfer **c** output characteristics of calibrated AAG Si FinFET [40] **d** fabrication process flowchart of proposed GaAs GS-GAA FinFET

Using the atomic layer deposition (ALD), the gate dielectric (Al_2O_3/HfO_2) deposition is executed on the GaAs interfacial facial [42]. Afterward, a metal gate (TiN) is grown at room temperature on the top of the gate insulator by electron beam evaporation [42]. The drain and source regions are implanted, and the dopants of these regions are activated using spike annealing. By electron beam evaporation, drain/source metal contacts are deposited, followed by a lift-off process. This completes the process of manufacturing the proposed device.

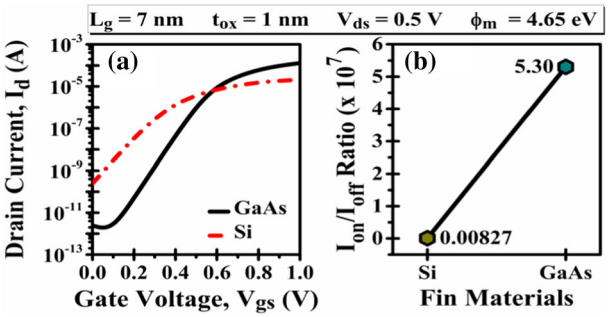

Fig. 3 Variation in (**a**) transfer characteristics **b** switching ratio of Si and GaAs GS-GAA FinFET

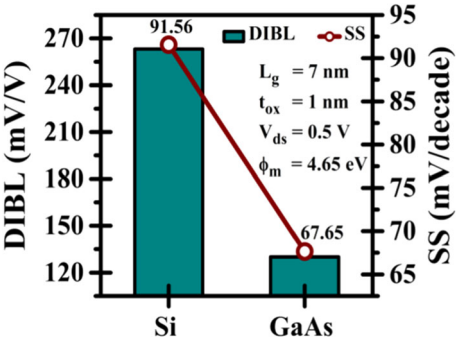

Fig. 4 Variation of DIBL and SS for Si and GaAs GS-GAA FinFET

4 Results and discussion

4.1 Impact of GaAs on analog metrics and parasitic capacitances

Figure 3a and b represents the comparison of $I_d - V_{gs}$ characteristics in log scale and switching (I_{on}/I_{off}) ratio for Si and GaAs GS-GAA FinFET, respectively. The drain current (I_d) enhances and leakage current (I_{off}) reduces appreciably, due to which I_{on}/I_{off} ratio increases by $\sim 10^3$ times for GaAs. The I_{off} is found to be in the range of 10^{-12} and 10^{-10} for GaAs and Si, respectively. GaAs large energy bandgap and high electron mobility is the primary reason for this significant reduction in the leakage current. The study of DIBL and SS becomes essential for aggressively scaled devices. DIBL extracted using Eq. (1) signifies the control of drain bias on the channel region's potential barrier, whereas SS provides perception about the leakage currents related to device characteristics. The lower the value of DIBL and SS, the better will be the SCEs. Figure 4 exhibits the collaborated plot of DIBL and SS for both Si and GaAs. DIBL reduces by ~50% from 263.19 mV/V to 130.04 mV/V, while a ~26% reduction is observed in SS for GaAs.

$$\text{DIBL} = \frac{\left|(V_{\text{th}})_{V_{ds}=1.0V} - (V_{\text{th}})_{V_{ds}=0.1V}\right|}{(1.0 - 0.1)} \tag{1}$$

Figure 5a reflects the variation of parasitic capacitances (C_{gs}, C_{gd} and C_{gg}) against gate—source voltage. It is observed that the parasitic capacitances increase with the increase in V_{gs} due to the aggregation of charge carriers close to the gate. The collaborated plot of C_{gs}, C_{gd}, and C_{gg} against drain–source voltage is shown in Fig. 5b. The charge carriers accumu-

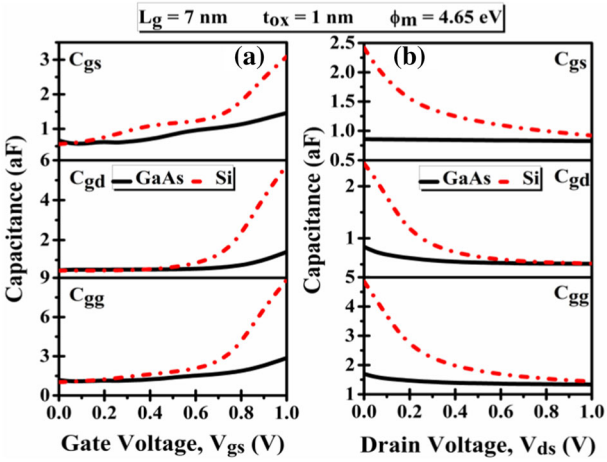

Fig. 5 Change in parasitic capacitances of Si and GaAs GS-GAA FinFET against **a** gate–source voltage **b** drain–source voltage

late near the source side with the increase in V_{ds}, and to conserve charge neutrality, drain capacitance decreases, and consequently, gate capacitance decreases. Moreover, the value of parasitic capacitances decreases considerably for GaAs than Si due to its higher energy bandgap and electron mobility. Thus, higher switching speed is acquired, and consequently, delay time decreases, making GaAs GS-GAA FinFET a suitable device for ULSI switching applications.

Mathematically expressed in Eq. (2) [43], gain–bandwidth product (GBP) is the product of the bandwidth and gain of an amplifier. The peak value of GBP denotes the frequency at which the device acquires maximum gain [30]. Figure 6a outlines the variation of GBP against gate bias for both GaAs and Si, and it is noticed that GaAs exhibits a higher peak value of GBP (7.35 THz) compared to Si (0.74 THz). It is due to the significant improvement in transconductance and drain capacitance.

$$\text{GBP} = \left(\frac{g_m}{2\pi \times 10 \times C_{gd}}\right) \tag{2}$$

$$\text{TFP} = \left(\frac{g_m}{I_d}\right) \times \left(\frac{g_m}{2\pi(C_{gs} + C_{gd})}\right) \tag{3}$$

Transconductance frequency product (TFP) is an essential capacitance-dependent FOM as defined in Eq. (3) [44]. Principally, it is the product of cutoff frequency and device efficiency. TFP exhibits an agreement between bandwidth and power and is mainly utilized in high-speed designs [45, 46]. Figure 6b portrays the change in TFP against gate bias for both GaAs and Si. It can be seen that TFP increases with the increase in V_{gs} in the subthreshold region and then achieve a maximum value in the inversion region. It starts declining due to an increment in C_{gg} with further enhancement in V_{gs}, i.e., in the deep inversion region. Besides, the peak value of TFP improves from 21.84 THz/V to 249.18 THz/V for GaAs due to the parasitic capacitance reduction and transconductance increment.

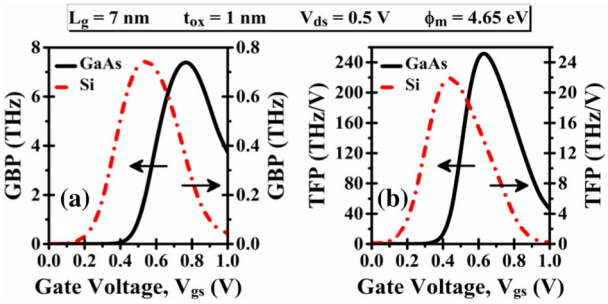

Fig. 6 Plot of **a** GBP **b** TFP against V_{gs} for Si and GaAs GS-GAA FinFET

Thus, as portrayed in Table 2, replacing Si with GaAs significantly improves the device analog metrics (I_{on}/I_{off} ratio, I_{off}, DIBL, and SS) and capacitance-related parameters (C_{gs}, C_{gd}, C_{gg}, TFP, and GBP). Thereby, on account of these advantages, the impact of gate length, fin height, and fin width of GaAs GS-GAA FinFET on analog metrics and parasitic capacitances has been explored further in the paper.

4.2 Impact of gate length (L_g) on analog metrics and parasitic capacitances

To investigate the analog metrics and parasitic capacitances characteristics concerning gate length, the GaAs GS-GAA FinFET device has been simulated for 5, 7, and 10 nm gate lengths. Figure 7a and b shows the device transfer characteristics in the log scale and switching ratio for mentioned gate lengths. The I_d is almost the same, while the I_{off} increases with the gate length reduction. I_{off} current increases by 150% when gate length reduces from 10 to 7 nm, while a further 301.22% increase in I_{off} is observed when gate length changes from 7 to 5 nm. This increase in the leakage current with gate length reduction results in the decrement of the switching ratio. The I_{on}/I_{off} ratio reduces by 89.24% with L_g reduction from 10 to 5 nm. Figure 8a represents the variation of DIBL against different gate lengths. It has been observed from the simulated results that, like I_{off}, DIBL also increases with the gate length reduction. When we reduce the L_g from 10 to 7 nm, DIBL enhances by 36.75%, and for 7 to 5 nm L_g reduction further 23.95% increase is noticed in DIBL. The SS plot concerning mentioned gate lengths is portrayed in Fig. 8b, and a similar trend for SS also follows, although the increase is not significant. A 6.11% increase in SS is obtained when L_g changes from 10 to 7 nm, while a further 2 nm reduction in L_g results in an 8.81% enhancement of SS. Thus, as represented in Table 3, a decrease in gate length increases the SCEs appreciably.

Figure 9a depicts the combined plot of C_{gs}, C_{gd}, and C_{gg} against gate–source voltage for different gate lengths. It is evident that parasitic capacitances decrease with the decrease in the gate length. The same movement is observed in the previously published results as well [47, 48]. C_{gs}, C_{gd}, and C_{gg} reduce by 18.07%, 12.50%, and 15.38%, respectively, with the shrinking of gate length from 10 to 7 nm. Besides, when L_g changes from 7 to 5 nm, C_{gs} decreases by 13.10%, C_{gd} by 10.71%, and C_{gg} by 12.23%. The change in parasitic capacitances against drain–source voltage for mentioned gate lengths is shown in Fig. 9b. In V_{ds} variation for different L_g, a similar trend is observed with minimal decrement. When we decrease L_g from 10 to 7 nm, C_{gs} reduces by 2.89%, C_{gd} by 0.58%, and C_{gg} by 2.02%. Also, for a further 2 nm reduction in L_g (7 to 5 nm), a 3.04%, 1.35%, and 2.39% decrease in C_{gs}, C_{gd}, and C_{gg} are obtained. Thus, parasitic capacitances reduce in GaAs GS-GAA

Table 2 Summary of different analog metrics and parasitic capacitances for Si and GaAs GS-GAA FinFET

Device	Parameters								
	I_{off} (A)	I_{on}/I_{off} ratio	DIBL (mV/V)	SS (mV/dec)	C_{gs} (aF)	C_{gd} (aF)	C_{gg} (aF)	GBP (THz)	TFP (THz/V)
Si GS-GAA FinFET	2.48×10^{-10}	8.27×10^{4}	263.19	91.56	3.08	5.74	8.82	0.74	21.84
GaAs GS-GAA FinFET	2.45×10^{-12}	5.30×10^{7}	130.04	67.65	1.45	1.40	2.86	7.35	249.18

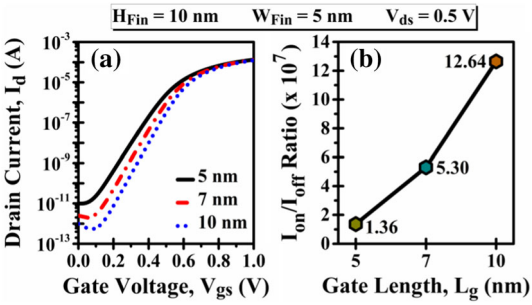

Fig. 7 Variation of **a** transfer characteristics **b** switching ratio against different gate lengths

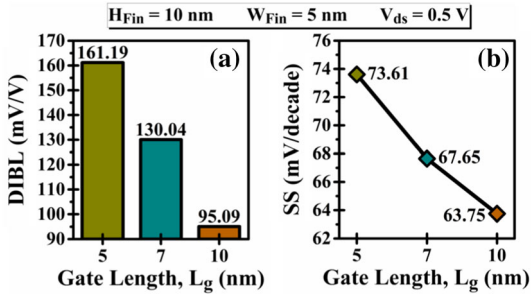

Fig. 8 Plot of **a** DIBL **b** SS against various gate lengths

FinFET with gate length shrinkage. Consequently, the proposed device exhibits enhanced circuit density in IC fabrication. Figure 10a and b reflects the change in GBP and TFP with gate bias for different gate lengths, and an opposite behavior is observed in GBP and TFP with the decrease in the L_g. The drain capacitance and transconductance reduce significantly with L_g reduction, leading to an increment in GBP and a decrement in TFP.

4.3 Impact of fin height (H_{Fin}) on analog metrics and parasitic capacitances

In this section, the GaAs GS-GAA FinFET device has been simulated for 5, 10, and 15 nm fin heights to explore its impact on analog metrics and parasitic capacitances characteristics. The change in the $I_d - V_{gs}$ characteristics in the log scale and switching ratio of the device for mentioned fin heights is reflected in Fig. 11a and b. The device leakage current improves appreciably with the decrease in the fin height from 15 to 5 nm, but a slight reduction in drain current is observed. I_{off} current decreases by 45.91% when H_{Fin} changes from 15 to 10 nm, while a further 5 nm decrease in H_{Fin} (10 to 5 nm) results in an 82.45% improvement in I_{off}. This improvement in I_{off} current leads to a significant increase in the I_{on}/I_{off} ratio. It is increased by 253.93% when H_{Fin} changes from 15 to 5 nm. The plot of DIBL against different fin heights is displayed in Fig. 12a, and a similar trend also follows for DIBL. DIBL improves by 15.68% when we reduce the H_{Fin} from 15 to 10 nm. An additional 15.54% improvement in DIBL is observed for change in H_{Fin} from 10 to 5 nm. Figure 12b shows the change in SS with the change in fin height, and it has been observed from the simulated results that, like I_{off} and DIBL, SS also decreases with the fin height reduction. When we reduce the H_{Fin} from 15 to 10 nm, SS changes from 68.56 mV/dec to 67.65 mV/dec, and for 10 to 5 nm H_{Fin} reduction, SS reduces to 65.49 mV/dec, which is closest to the ideal value of SS (60 mV/dec). Thus, reducing the fin height of the device significantly improves the SCEs characteristics, as displayed in Table 4.

Table 3 Summary of different analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for various gate lengths

Gate lengths	Parameters								
	I_{off} (A)	I_{on}/I_{off} ratio	DIBL (mV/V)	SS (mV/dec)	C_{gs} (aF)	C_{gd} (aF)	C_{gg} (aF)	GBP (THz)	TFP (THz/V)
5 nm	9.83×10^{-12}	1.36×10^{7}	161.19	73.61	1.26	1.25	2.51	7.40	232.25
7 nm	2.45×10^{-12}	5.30×10^{7}	130.04	67.65	1.45	1.40	2.86	7.35	249.18
10 nm	0.98×10^{-12}	12.6×10^{7}	95.09	63.75	1.77	1.60	3.38	7.19	253.30

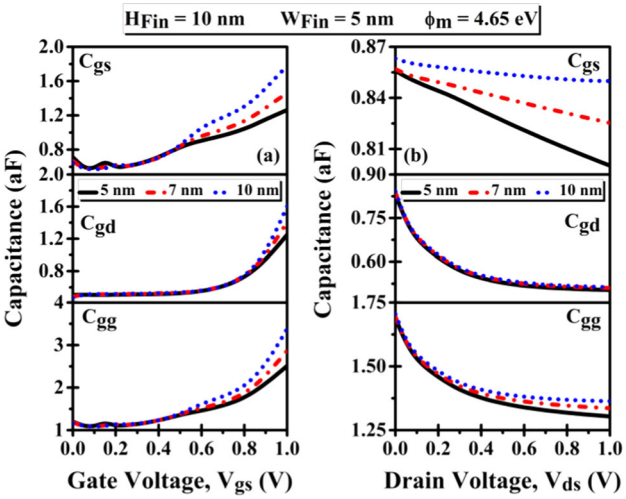

Fig. 9 Change in parasitic capacitances against **a** gate–source voltage **b** drain–source voltage for mentioned gate lengths

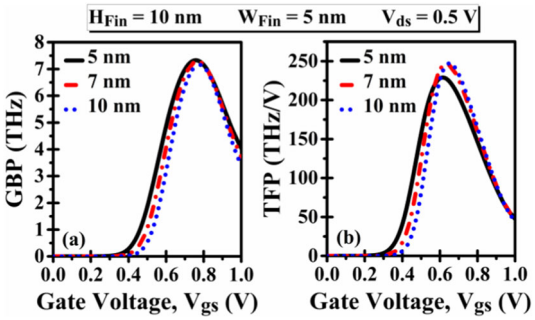

Fig. 10 Variation of **a** GBP **b** TFP against different gate lengths

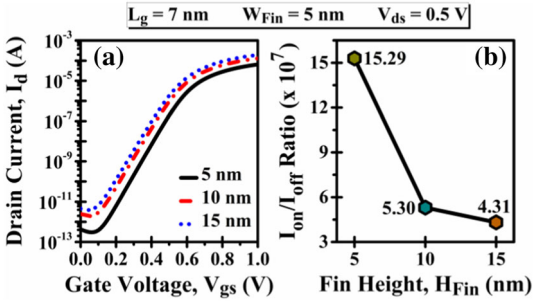

Fig. 11 Variation of **a** transfer characteristics **b** switching ratio against different fin heights

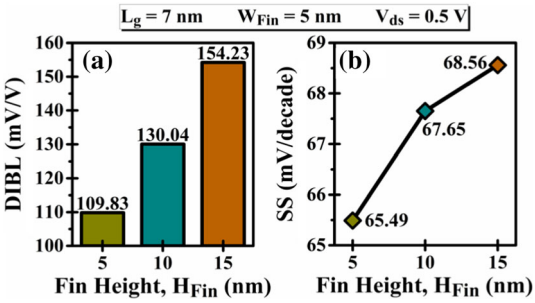

Fig. 12 Plot of **a** DIBL **b** SS against various fin heights

The collaborated plot of parasitic capacitances (C_{gs}, C_{gd}, and C_{gg}) against V_{gs} for different fin heights are represented in Fig. 13a. It is visible that parasitic capacitances decrease notably with the decrease in fin height. When we decrease the H_{Fin} from 15 to 10 nm, C_{gs} reduces by 32.24%, C_{gd} by 33.01%, and C_{gg} by 32.54%. Also, for a further 5 nm reduction in H_{Fin} (10 to 5 nm), a 46.89%, 47.85%, and 47.55% decrease in C_{gs}, C_{gd}, and C_{gg} are obtained. Figure 13b shows the alteration in the parasitic capacitance with change in V_{ds} for mentioned fin heights. C_{gs}, C_{gd}, and C_{gg} reduce by 32.6%, 32.58%, and 32.59%, respectively, with the shrinking of H_{Fin} from 15 to 10 nm. When H_{Fin} changes from 10 to 5 nm, C_{gs} decreases by 48.84%, C_{gd} by 48.61%, and C_{gg} by 48.75%. Thus, with shrinkage in fin height from 15 to 5 nm, parasitic capacitances reduce in the proposed device. Figure 14a and b exhibits the variation in GBP and TFP with V_{gs} for different fin heights, and the peak value of both the parameters increases with the reduction in the H_{Fin}. When we reduce the H_{Fin} from 15 to 5 nm, the GBP peak value obtained at $V_{gs} = 0.75$ V shifts from 7.34 THz to 7.58 THz, and the peak value of TFP obtained at $V_{gs} = 0.65$ V changes from 241.72 THz/V to 272.70 THz/V. This increase in GBP and TFP is due to the enhanced g_m and reduced parasitic capacitances with fin height.

4.4 Impact of fin width (W_{Fin}) on analog metrics and parasitic capacitances

The GaAs GS-GAA FinFET has been evaluated for different fin widths (3, 5, and 7 nm) to evaluate the impact of fin width on analog metrics and parasitic capacitances characteristics. Figure 15a and b represents the variation in $I_d - V_{gs}$ characteristics in the log scale and switching ratio for mentioned fin widths. It has been observed from the simulated results that the drain current reduces slightly, and the leakage current improves significantly with the fin width reduction. When W_{Fin} changes from 7 to 5 nm and from 5 to 3 nm, the I_{off} current decreases by 84.66% and 93.46%, respectively. This significant improvement in I_{off} current leads to a massive enhancement in the I_{on}/I_{off} ratio. Figure 16a portrays the variation in DIBL for different fin widths. It has been observed that DIBL decreases with the decrease in fin width from 7 to 3 nm. When we reduce the W_{Fin} from 7 to 5 nm, DIBL improves from 152.05 mV/V to 130.04 mV/V, and when W_{Fin} reaches 3 nm, DIBL further reduces to 108.97 mV/V. The SS plot against mentioned fin widths is depicted in Fig. 16b, and like I_{off}, DIBL, SS also decreases with the decrease in the W_{Fin}. A 4.39% decrease in SS is obtained when W_{Fin} changes from 7 to 5 nm, and an additional 4.22% improvement in SS is observed when W_{Fin} changes from 5 to 3 nm. Thus, as presented in Table 5, SCEs characteristics of the GaAs GS-GAA FinFET improve appreciably with a decrease in fin width.

Table 4 Summary of different analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for various fin heights

Fin heights	Parameters								
	I_{off} (A)	I_{on}/I_{off} ratio	DIBL (mV/V)	SS (mV/dec)	C_{gs} (aF)	C_{gd} (aF)	C_{gg} (aF)	GBP (THz)	TFP (THz/V)
5 nm	0.43×10^{-12}	15.3×10^{7}	109.83	65.49	0.77	0.73	1.50	7.58	272.70
10 nm	2.45×10^{-12}	5.30×10^{7}	130.04	67.65	1.45	1.40	2.86	7.35	249.18
15 nm	4.53×10^{-12}	4.31×10^{7}	154.23	68.56	2.14	2.09	4.24	7.34	241.72

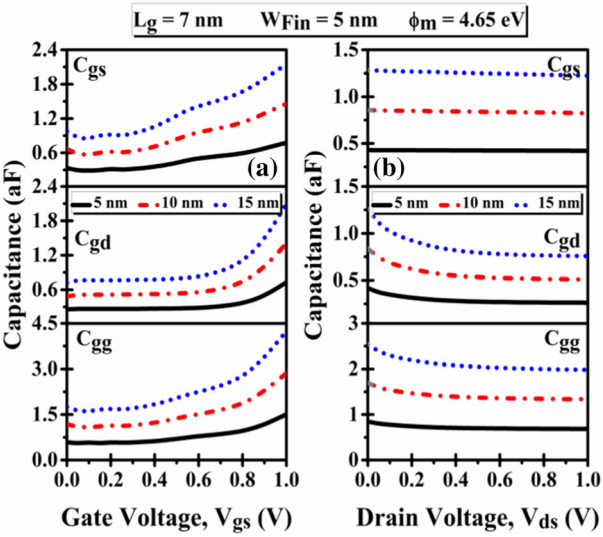

Fig. 13 Change in parasitic capacitances against **a** gate–source voltage **b** drain–source voltage for mentioned fin heights

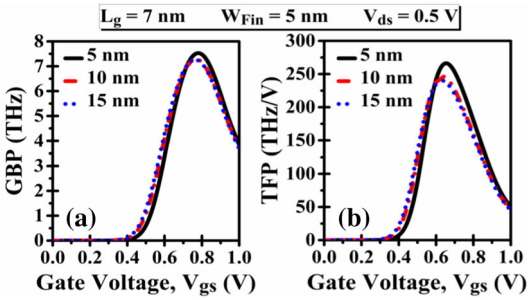

Fig. 14 Variation of **a** GBP **b** TFP against different fin heights

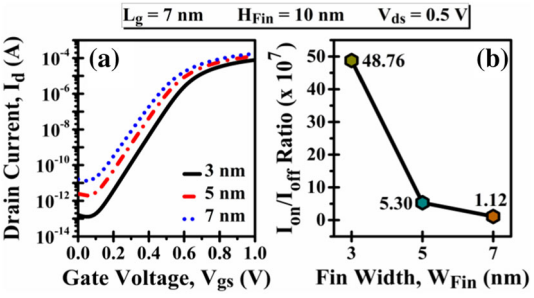

Fig. 15 Variation of **a** transfer characteristics **b** switching ratio against different fin widths

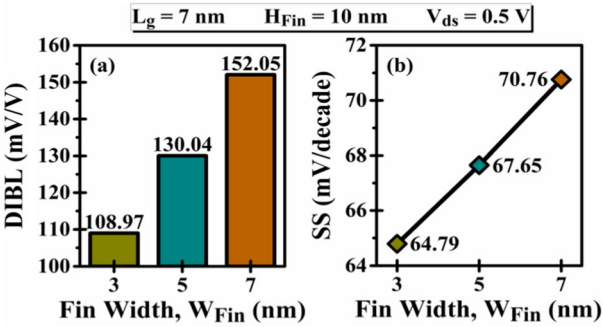

Fig. 16 Plot of **a** DIBL **b** SS against various fin widths

Figure 17a outlines the variation of parasitic capacitances against gate–source voltage for different fin widths. It is observed that parasitic capacitances decrease significantly with the decrease in the fin width. The shrinking of W_{Fin} from 7 to 5 nm leads to a decrease of 23.28%, 24.32%, and 23.52% in C_{gs}, C_{gd}, and C_{gg}, respectively. Besides, when W_{Fin} changes from 5 to 3 nm, C_{gs} decreases by 33.79%, C_{gd} by 36.42%, and C_{gg} by 35.31%. The variation of parasitic capacitances as a function of drain–source voltage and fin widths is shown in Fig. 17b. C_{gs}, C_{gd}, and C_{gg} reduce by 26.19%, 26.54%, and 26.32%, respectively, with the reduction of W_{Fin} from 7 to 5 nm. C_{gs} decreases by 38.22%, C_{gd} by 37.82%, and C_{gg} by 38.07% when W_{Fin} changes from 5 to 3 nm. Thus, a decrease in fin width significantly improves the parasitic capacitances characteristics of the GaAs GS-GAA FinFET. The change in GBP and TFP with gate bias for different fin widths is shown in Fig. 18a and b. The peak value of both the parameters increases and shifts toward the higher gate bias with a reduction in the fin width. GBP and TFP peak value increases because of the reduction in parasitic capacitances and increment in transconductance. The peak value of GBP shifts from 7.15 THz to 7.81 THz when we reduce the W_{Fin} from 7 to 3 nm. Similarly, the peak value of TFP increases from 229.27 THz/V to 286.31 THz/V. In addition, we have compared the analog metrics and parasitic capacitances obtained in this work with several different device structures at fixed 10 nm gate length, as shown in Table 6. It can be seen that the results obtained in this work stand out from the recently published work. The reduction in SCEs, parasitic capacitances, and increment in GBP and TFP is very significant compared to other papers.

5 Conclusion

This paper explores the analog metrics and parasitic capacitances characteristics of Gate Stack Gate-All-Around (GS-GAA) FinFET with GaAs as a fin material. We have also analyzed certain capacitance-related FOMs like GBP and TFP for switching applications. It is noticed from the simulated results that the use of GaAs as a fin material significantly reduces the

Table 5 Summary of different analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for various fin widths

Fin widths	Parameters								
	I_{off} (A)	I_{on}/I_{off} ratio	DIBL (mV/V)	SS (mV/dec)	C_{gs} (aF)	C_{gd} (aF)	C_{gg} (aF)	GBP (THz)	TFP (THz/V)
3 nm	0.16×10^{-12}	48.7×10^{7}	108.97	64.79	0.96	0.89	1.85	7.81	286.31
5 nm	2.45×10^{-12}	5.30×10^{7}	130.04	67.65	1.45	1.40	2.86	7.35	249.18
7 nm	15.9×10^{-12}	1.12×10^{7}	152.05	70.76	1.89	1.85	3.74	7.15	229.27

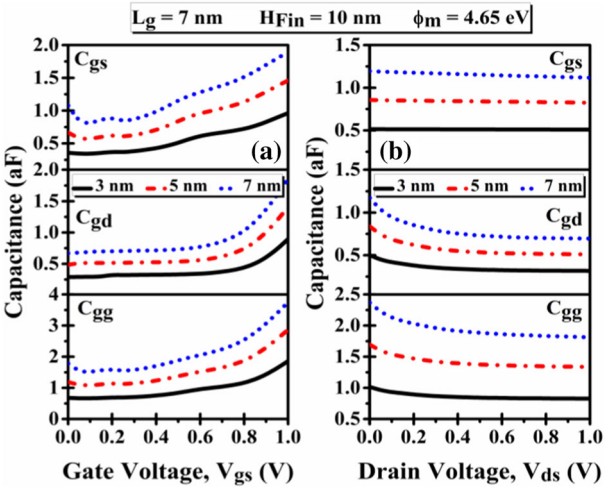

Fig. 17 Change in parasitic capacitances against **a** gate–source voltage **b** drain–source voltage for mentioned fin widths

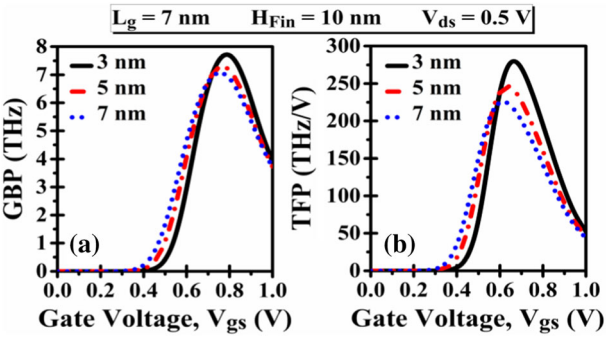

Fig. 18 Variation of **a** GBP **b** TFP against different fin widths

Table 6 Comparison of various analog metrics and parasitic capacitances of different devices at a fixed gate length, $L_g = 10$ nm

References	Year	DIBL (mV/V)	SS (mV/dec)	C_{gs} (fF)	C_{gd} (fF)	C_{gg} (fF)	GBP (THz)	TFP (THz/V)
[49]	2017	N.A	79.8	0.38	3.62	3.99	0.00039	N.A
[50]	2018	99.79	114.60	N.A	N.A	0.97	N.A	3.78
[51]	2019	N.A	N.A	5.36	1.01	6.37	0.37	2.22
[52]	2020	42.95	74.63	0.07	0.07	0.14	N.A	2.18
[43]	2020	N.A	N.A	0.0043	0.0019	0.0059	1.61	45.70
[53]	2021	81.27	71.87	0.04	0.04	0.08	0.05	0.01
[54]	2021	98.48	65.6	0.27	0.24	0.52	0.46	9.48
Present work	–	95.09	63.75	0.0017	0.0016	0.0033	7.19	253.30

The data which is not available is mentioned as N.A

SCEs and parasitics capacitances of the device. The I_{off} current approximately reduces by 100 times, DIBL becomes half, and SS decreases by ∼26% for GaAs compared to Si. The parasitic capacitances follow the same trend, with C_{gs} reduced by 52.92%, C_{gd} by 75.60%, and C_{gg} by 67.57%. Due to this considerable decrease in the parasitic capacitances, the peak value of GBP and TFP increases by 893.24% and 1040.93%, respectively. Moreover, parameters like L_g, H_{Fin}, and W_{Fin} are varied to enhance the device performance further. It is found that with the decrease in the L_g, H_{Fin}, and W_{Fin}, the SCEs and parasitic capacitances decrease appreciably. Thus, GaAs GS-GAA FinFET architecture with $L_g = 5$ nm, $H_{Fin} = 5$ nm, and $W_{Fin} = 3$ nm can be considered a suitable candidate for low power ULSI switching applications.

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Authors' contribution All authors contributed to the study's conception and design.

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Data Availability Statement This manuscript has associated data in a data repository. [Authors' comment: The authors mentioned above have all the relevant data associated with this research work and will be dedicated to share that if asked to do so in the future.].

Declarations

Conflict of interests The authors declare that they have no known conflict of interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethical approval The authors have seen all the Ethical Standards and will suppose to follow them in the future.

Consent for participate Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

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Gate electrode work function engineered JAM-GS-GAA FinFET for analog/RF applications: Performance estimation and optimization

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ABSTRACT

In this study, the gate electrode work function engineered Junctionless Accumulation Mode Gate Stack Gate All Around (JAM-GS-GAA) FinFET has been rigorously investigated for analog/RF applications. The simulated findings show that decreasing the gate electrode work function by 0.4 eV improves the static characteristics such as electric field (46.68%), electron mobility (55.0%), potential (5.74%), and electron concentration (2.97%). A 0.4 eV escalation in the gate electrode work function improves the analog parameters of the JAM-GS-GAA FinFET significantly in terms of leakage current (I_{off}) (10^4 times), subthreshold swing (SS) (20.26%), switching ratio (I_{on}/I_{off}) (10^2 to 10^6), and quality factor (QF) (25.54%), intrinsic gain (A_v) (280.73%), early voltage (V_{EA}) (62.12%), and output conductance (g_d) (90.52%). The RF parameters follow the same trend as analog parameters. GFP and GTFP increased more than eight and ten times, respectively, with a surge in the gate electrode work function. Consequently, the findings of this research can assist engineers in designing nanoelectronic devices that meet their requirements.

1. Introduction

The aggressive downscaling in the transistor size inflicts numerous hindrances on the device performance and fabrication challenges [1]. The device efficiency degrades significantly due to increased gate leakage current and short channel effects (SCEs) [2–5]. Multi-gate device structures like FinFET [6,7] demonstrate superiority over planar devices to overcome these SCEs while obeying ITRS roadmap projections [8]. The ultimate candidate is the Gate All Around (GAA) structure which offers high current driving capability, steep subthreshold slope, higher packing density, and enhanced electrostatic control over the channel [9,10]. High series resistance and junction fabrications are serious disadvantages in these extremely scaled devices. Novel solutions like Junctionless (JL) transistors have been extensively researched [11,12]. Junctionless Accumulation Mode (JAM) transistors with increased doping in source and drain areas have been proposed to counter the low channel doping concentration issues [13,14]. Gate Stack (GS) configuration suppresses the rise in off-state leakage current (I_{off}) during MOS technology downscaling [15]. In addition, GS configuration resolves the limitations like threshold voltage instability and mobility degradation that occur during straight deposition of high-k dielectrics on silicon substrates [16,17]. Subsequently, we put forward JAM-GS-GAA FinFET.

The device performance depends significantly on the gate electrode work function in the sub-10 nm regime CMOS technology. The alteration in the work function impacts the channel region electric field at zero gate-source voltage, which affects the various device performance parameters. Nowadays, the utilization of metal gates is not new because metal gates do not exhibit the poly-depletion effect. The polysilicon gates lead to unwanted fluctuations in the threshold voltage of MOSFET devices [18]. In addition, polysilicon gates become chemically unstable when placed in contact with high-k dielectrics [19]. As a result, finding the proper gate metal for enhanced device performance and better reliability becomes vital. Few papers are present on the consequences of the device's gate work function on its performance. Mohapatra et al. provide a detailed analysis of the consequences of gate work function on the GS-DG MOSFET performance [20]. RF and DC performance in Multifin-FinFET for different gate work function variations is testified by Hirpara et al. [21]. Recently, Kumar et al. reported the gate work function impact on the performance analysis of DG-JL-FET [22]. However, no work has been published on the JAM-GS-GAA FinFET static and analog/RF performance evaluation with varied gate electrode work functions. Thus, this investigation determines the effect of the work function on the proposed device's different static, analog, and RF

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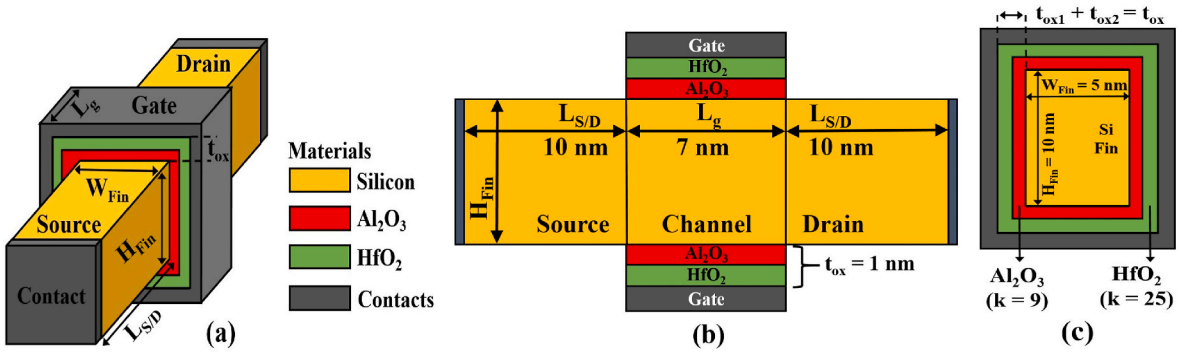

Fig. 1. (a) 3D systematic structure, (b) 2D horizontally, and (c) 2D vertically cut structures of JAM-GS-GAA FinFET.

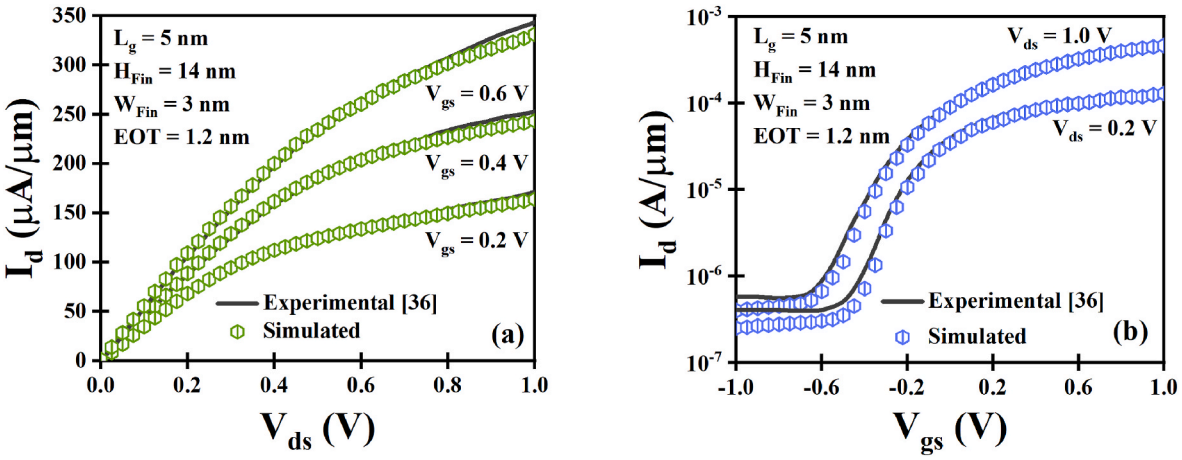

Fig. 2. Calibrated GAA FinFET device's (a) output and (b) transfer characteristics.

parameters.

The remainder of the manuscript is: Section 2 offers information on the device's structure and the physical models employed. The experimental calibration and the proposed device manufacturing feasibility are discussed in Section 3. Section 4 compares the proposed JAM-GS-GAA FinFET with conventional FinFET and other existing devices and examines the effect of the gate electrode work function on the proposed device's different parameters. With concluding observations, Section 5 proves the paper's originality.

2. Device structure and physical models

Fig. 1(a–c) presented the 3D systematic structure and 2D horizontally and vertically cut structures of JAM-GS-GAA FinFET. The fin region consists of Silicon (Si) material. The source/drain length ($L_{S/D}$) and gate length (L_g) of JAM-GS-GAA FinFET are 10 and 7 nm, respectively. Throughout the simulation, the fin width (W_{Fin} = 5 nm) is fixed in a multiple of the fin height (H_{Fin} = 10 nm) to obey the width quantization property [23,24]. 1 nm is the total gate oxide thickness, and the gate oxide is stacked using a combination of Al_2O_3 (k = 9) and HfO_2 (k = 25) in equal proportions. All three regions are n-type uniformly doped with

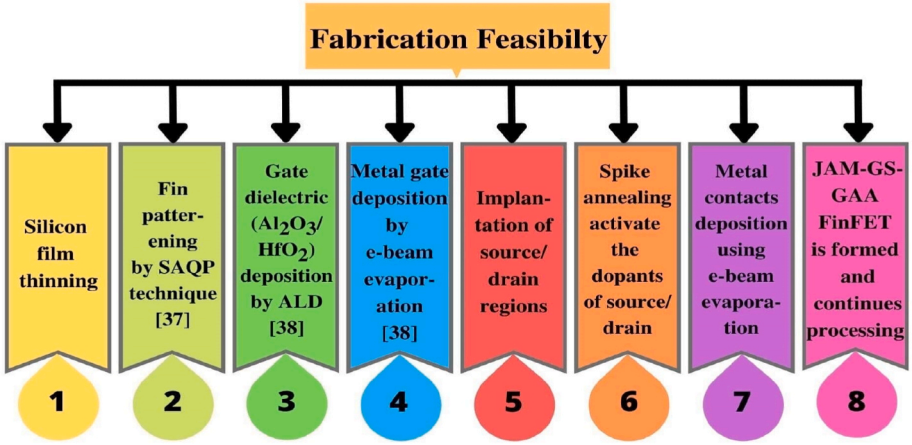

Fig. 3. A step-by-step manufacturing process flowchart of the proposed device.

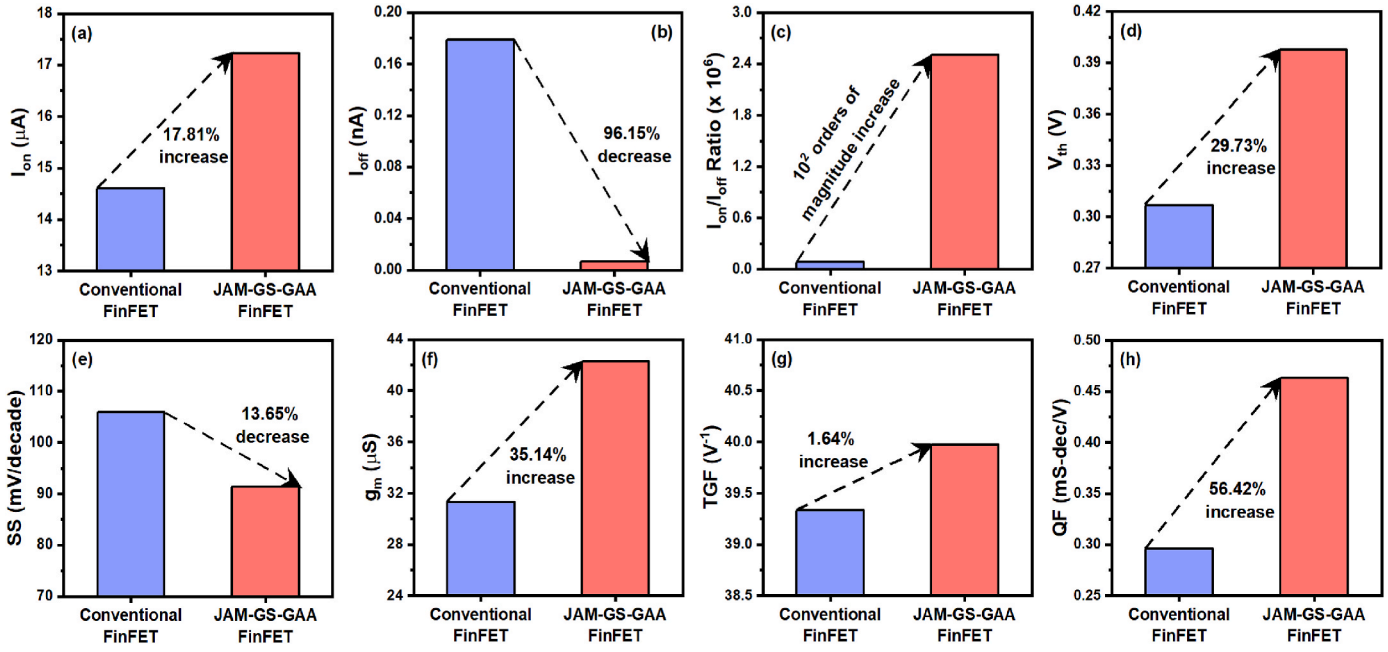

Fig. 4. Plot of (a) I_{on}, (b) I_{off}, (c) I_{on}/I_{off} ratio, (d) V_{th}, (e) SS, (f) g_m, (g) TGF, and (h) QF for conventional FinFET and JAM-GS-GAA FinFET devices.

lower doping in the channel area ($N_{Ch} = 1 \times 10^{16}$ cm^{-3}) compared to the source/drain area ($N_{S/D} = 5 \times 10^{18}$ cm^{-3}) to lessen the parasitic capacitance and improve the performance [25,26]. The gate electrode work function is altered during the simulation from 4.4 eV to 4.8 eV with a step size of 0.1 eV to analyze the proposed device's different static, analog, and RF parameters. Temperature (T) is kept at 300 K, and gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) are altered, as mentioned in the respective figures.

The SILVACO Atlas 3D simulator has been used to simulate the proposed JAM-GS-GAA FinFET structure [27]. In addition to Poisson and Continuity equations, alternate equations are essential for error-free and practical results. Thus, various physical models are incorporated during the simulations. The Bohm Quantum Potential (BQP) model is important, as quantum confinement effects cannot be neglected in aggressively scaled devices [28,29]. The other included models are bandgap narrowing, SRH recombination, Klaassen tunneling, concentration-dependent mobility, Crowell-Sze impact ionization, and Fermi-Dirac statistics [30–35]. Furthermore, all the mathematical carrier transport equations are performed using the Newton and Block iteration methods.

3. Experimental calibration and fabrication feasibility

The GAA FinFET is calibrated using experimental data from H. Lee et al. [36] to confirm the physical models. To validate the simulations, we calibrated the experimental results with fixed device dimensions ($W_{Fin} = 3$ nm, $H_{Fin} = 14$ nm, and $L_g = 5$ nm) and assumed Si material in the fin area as specified in the publication. The GAA FinFET device's output characteristics for different gate voltages are depicted in Fig. 2 (a), whereas transfer characteristics at $V_{ds} = 0.2$ V and $V_{ds} = 1.0$ V are demonstrated in Fig. 2(b). The strong agreement between the experimental and simulated output and transfer characteristics validates the model choices.

A step-by-step manufacturing process flowchart of the JAM-GS-GAA FinFET is shown in Fig. 3 to demonstrate the proposed device's fabrication feasibility. The silicon film is thinned first. Then, using the self-aligned quadruple patterning (SAQP) approach, fin patterning is done [37]. SAQP is the application of two self-aligned double patternings in a row. Atomic layer deposition (ALD) is used to deposit the gate dielectric (Al_2O_3/HfO_2) on the silicon interfacial layer [38]. The metal gate of choice is then coated on top of the gate dielectric using electron beam evaporation at room temperature. Spike annealing activates the dopants in the drain and source areas after being implanted. Electron beam evaporation deposits the source/drain metal contacts, which are lifted off. The JAM-GS-GAA FinFET is produced and handling proceeds.

Table 1
Detailed comparison of JAM-GS-GAA FinFET with different existing devices at fixed $L_g = 10$ nm.

Ref.	Year	Platform Device	Parameters								
			I_{off} (A)	I_{on}/I_{off} ratio ($\times 10^5$)	TGF (V^{-1})	A_v	V_{EA} (V)	C_{gs} (fF)	C_{gd} (fF)	f_T (THz)	GBP (THz)
[39]	2019	Junctionless Double Gate Vertical MOSFET	NA	NA	26.7	NA	0.59	5.36	1.01	0.083	0.376
[40]	2020	Nano-sheet Transistor	7.62×10^{-10}	1.90	NA	6.03	2.67	0.07	0.07	0.585	NA
[41]	2021	SOI Junctionless Nanowire FET	7.10×10^{-10}	0.82	41.81	NA	NA	0.04	0.04	0.254	0.05
[42]	2022	Tunnel Field Effect Transistor	1.51×10^{-13}	NA	4.39	0.93	NA	0.258	0.422	0.940	0.973
This Work	–	Junctionless Accumulation Mode Gate Stack Gate All Around FinFET	3.73×10^{-13}	455.28	40.09	58.17	19.57	0.002	0.004	2.845	0.774

*NA – data not available.

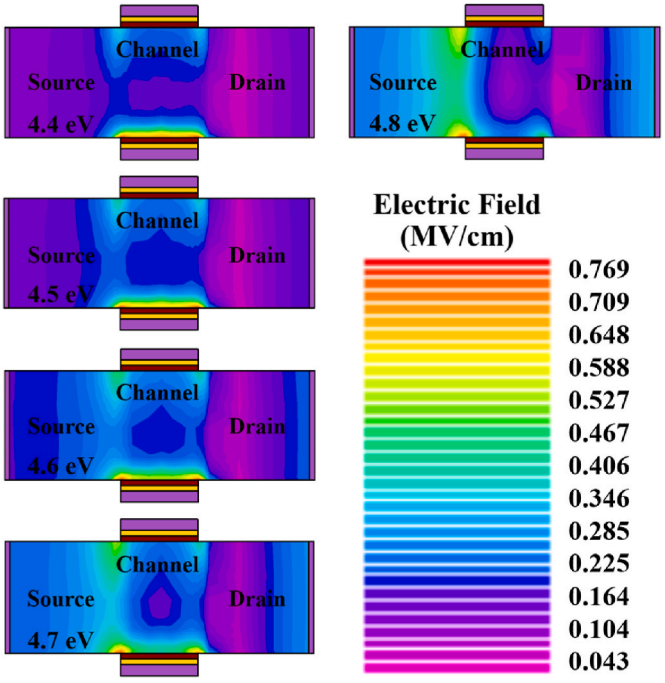

Fig. 5. Contour profile of electric field for altered gate electrode work functions.

4. Results and discussion

4.1. Performance comparison with conventional FinFET and other existing devices

It is necessary to compare the performance of the proposed device and that of the conventional FinFET before analyzing the static and analog/RF performance of the JAM-GS-GAA FinFET. Conventional FinFET and JAM-GS-GAA FinFET devices have the same device dimensions, as described in section 2. The gate electrode work function used for both devices is 4.8 eV. Fig. 4(a–h) describes the comparison of important parameters such as ON current (I_{on}), OFF current (I_{on}), switching ratio (I_{on}/I_{off}), threshold voltage (V_{th}), subthreshold swing (SS), transconductance (g_m), device efficiency (TGF), and quality factor (QF) for both the devices. In Fig. 4(a and b), it can be seen that I_{on} enhanced by 17.81% while I_{off} improved by 96.15% for JAM-GS-GAA FinFET compared to conventional FinFET. Thereby increasing the I_{on}/I_{off} ratio by almost 10^2 orders of magnitude (Fig. 4(c)). The V_{th} shows an improvement of 29.73%, whereas SS is reduced by 13.65% for the proposed JAM-GS-GAA FinFET in Fig. 4(d and e). In Fig. 4(f), an increase of 35.14% is observed in g_m with a slight enhancement in TGF (Fig. 4 (g)). Lastly, in Fig. 4(h), it is observed that QF exhibits a rise of 56.42% for the JAM-GS-GAA FinFET compared to conventional FinFET. Thus, it is clear that the proposed JAM-GS-GAA FinFET performs far better than the conventional FinFET. Further, this study also benchmarks with other existing devices on different technologies to evaluate the significance of JAM-GS-GAA FinFET [39–42]. For a fair comparison, Table 1 thoroughly compares the various characteristics of JAM-GS-GAA FinFET with different published works at a fixed gate length of 10 nm. The devices considered for comparison are junctionless double gate vertical

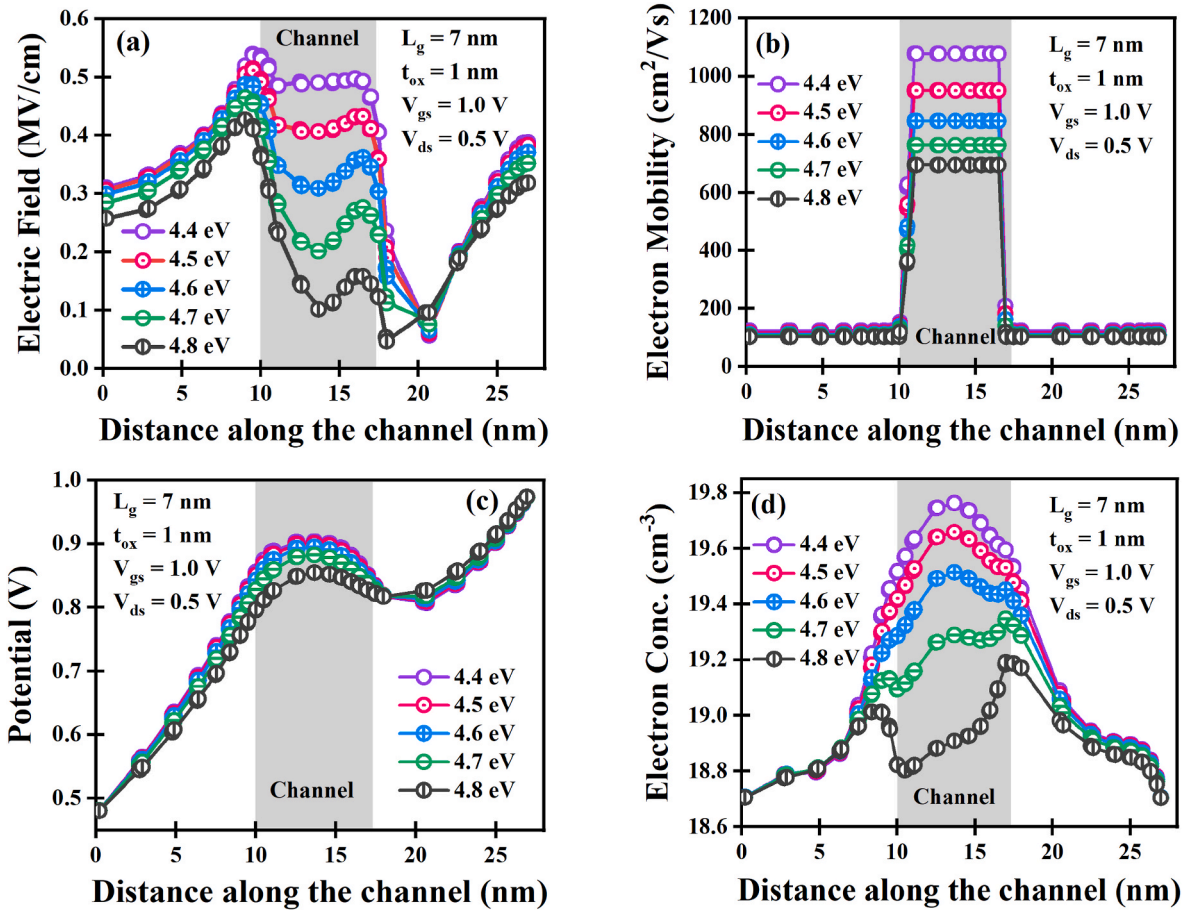

Fig. 6. Plot of (a) electric field, (b) electron mobility, (c) potential, and (d) electron concentration for altered gate electrode work functions.

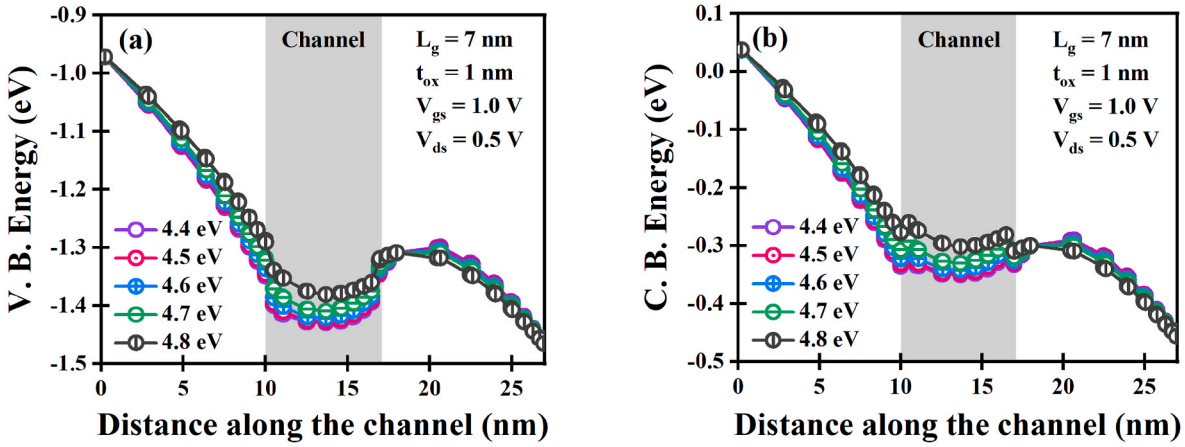

Fig. 7. (a) VB energy and (b) CB energy plot for all the devices with different gate electrode work functions along the channel.

Table 2
Overview of evaluated static parameters of JAM-GS-GAA FinFET with different work functions.

Parameters	Work Function	
	4.4 eV	4.8 eV
Electric Field (MV/cm)	0.531	0.362
Electron Mobility (cm^2/Vs)	1076.27	694.35
Potential (V)	0.903	0.854
Electron Concentration (cm^{-3})	19.76	19.19
Valence Band Energy (eV)	−1.342	−1.291
Conduction Band Energy (eV)	−0.315	−0.259

MOSFET, nano-sheet transistor, SOI junctionless nanowire FET, and tunnel field effect transistor. It has been observed that the performance of a JAM-GS-GAA FinFET is better than that of any other state-of-the-art device, thereby validating our proposed device structure.

4.2. Static performance

The electric field contour profiles and the electric field plot along the channel for each gate electrode work function considered are demonstrated in Figs. 5 and 6(a), respectively. The electric field is much greater for the 4.4 eV than the 4.8 eV in the channel region. Fig. 6(b) depicts the effect of gate electrode work function on electron mobility. It can be seen

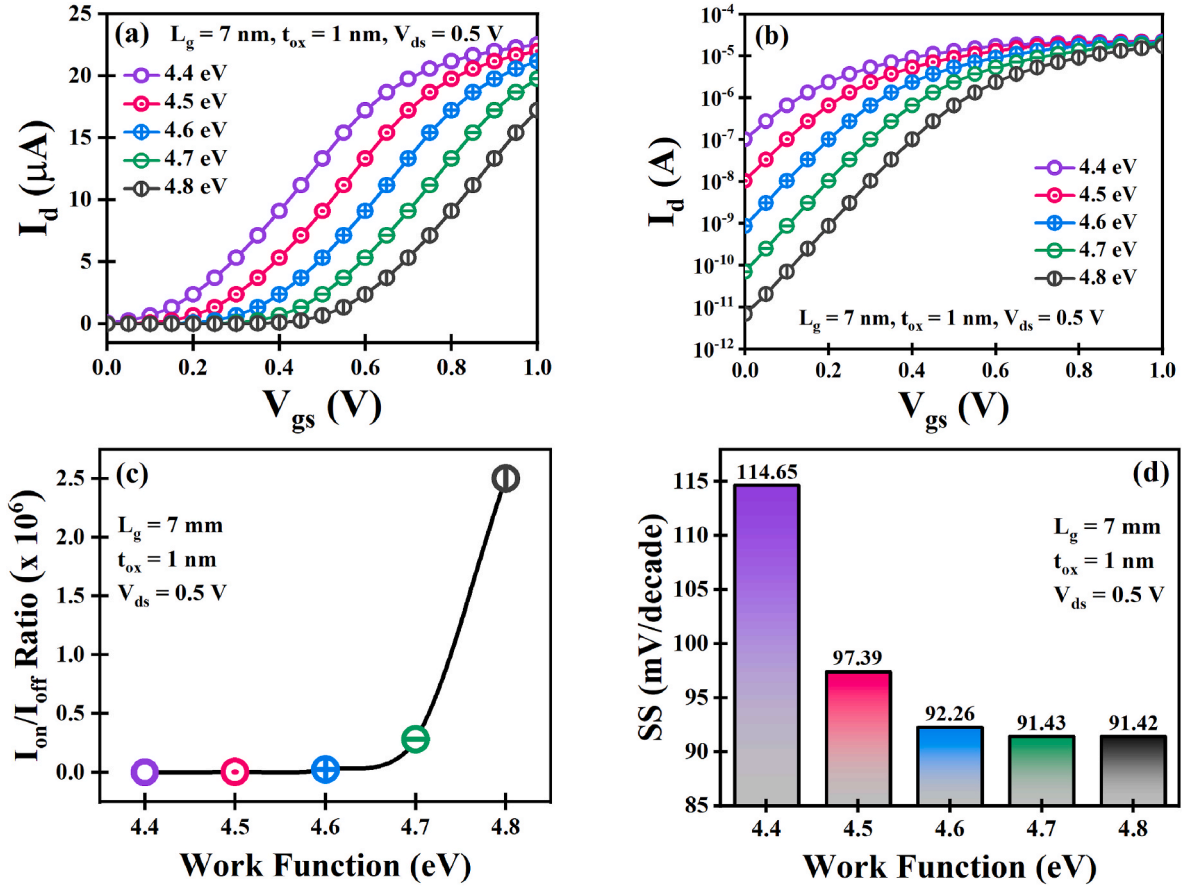

Fig. 8. Influence of considered gate electrode work functions on (a) I_{on} current, (b) I_{off} current, (c) I_{on}/I_{off} ratio, and (d) SS.

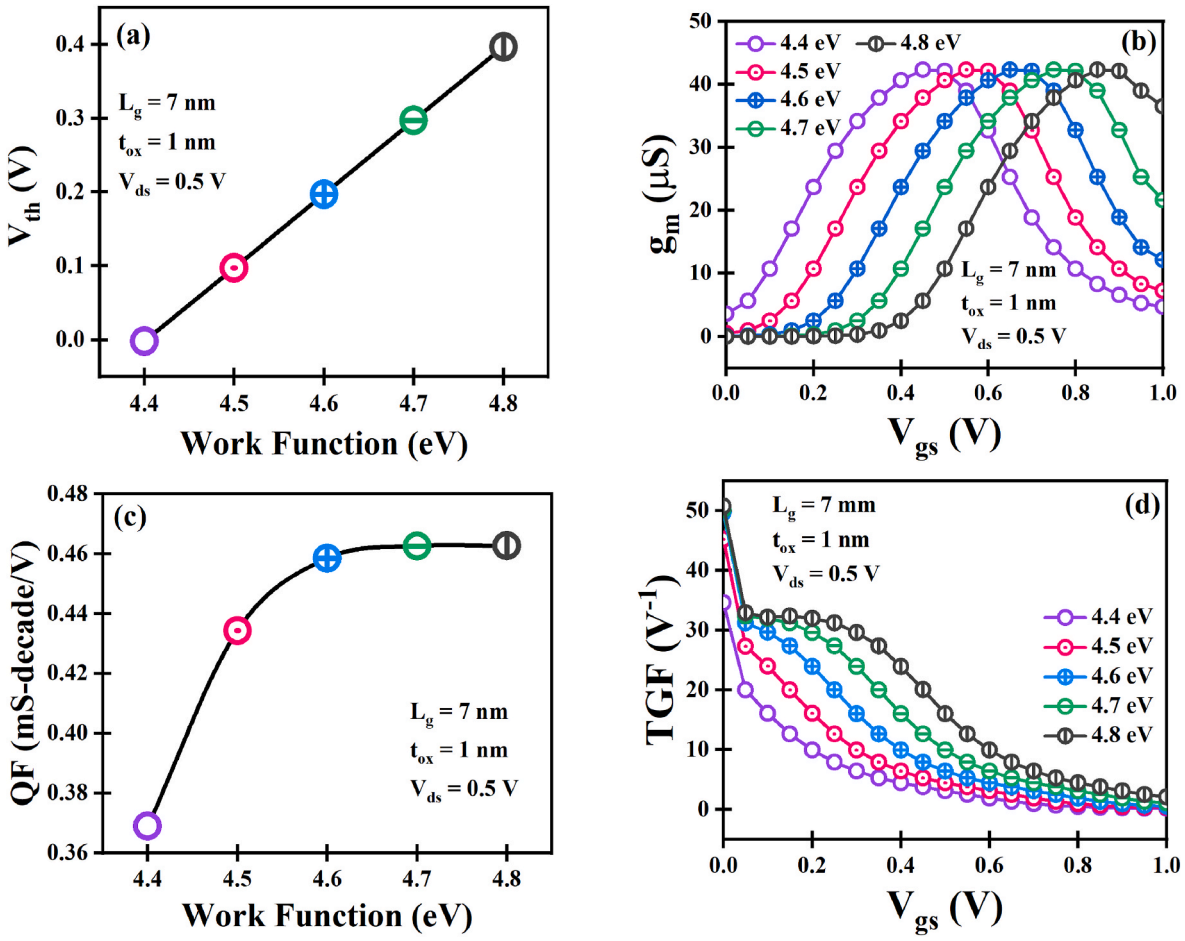

Fig. 9. Consequences of the gate electrode work function on (a) V_{th}, (b) g_m, (c) QF, and (d) TGF.

that the electron mobility in the channel region is higher with a 4.4 eV gate electrode work function which leads to enhanced electron velocity, which in turn enhances the device's electric field. The potential of all the devices with altered gate electrode work functions is evaluated along the channel and displayed in Fig. 6(c). The potential increases with reduced gate electrode work function in the channel area. Again, the increased electron mobility in the channel area is the reason for the same behavior. The alteration of the electron concentration for the different gate electrode work functions along the channel is outlined in Fig. 6(d). In the channel region, the electron concentration rises considerably with the decrement in the gate electrode work function. The energy band profile includes electron energy levels in the MOS structure. Fig. 7(a–b) depicts the valence band energy (VB) and conduction band energy (CB) for all the devices with different gate electrode work functions along the channel. It is evident from the results that both VB and CB are higher for the device with a 4.8 eV work function in comparison to the devices with lower work functions. The comparison of gate electrode work functions on the evaluated static parameters is abridged in Table 2. The table reflects the peak value in the channel region of the evaluated static parameters.

4.3. Analog performance

Fig. 8(a) depicts the influence of considered gate electrode work functions on the device's drain current (I_d) at constant V_{ds}. The threshold voltage rises with a surge in the gate electrode work function. Subsequently, a reduction in the I_{on} current is observed with an escalation in the work function. However, a rise in the gate electrode work function leads to increased band bending, which improves the device's I_{off} current, as illustrated in Fig. 8(b). The consequences of the gate electrode work function on the switching ratio (I_{on}/I_{off}) are portrayed in Fig. 8(c). The switching ratio is ~10^4 times more for 4.8 eV than 4.4 eV because the drop in the I_{off} current is more noticeable than the reduction in I_{on} current. The subthreshold swing (SS) variation against different work functions is demonstrated in Fig. 8(d). A considerable reduction in the SS is observed with an escalation in the gate electrode work function, indicating an improvement in short-channel effects.

$$g_m = \partial I_d / \partial V_{gs} \tag{1}$$

Fig. 9(a) depicts the deviation of threshold voltage (V_{th}) with the gate electrode work function. The V_{th} increases linearly with the growth in the gate electrode work function, and the maximum value (0.397 V) is observed for the 4.8 eV. The reduction in the drain current leads to a rise in the threshold voltage of the device. The change in I_d with gate bias at fixed drain voltage is known as transconductance (g_m). It should be high for enhanced device performance and is expressed using Eq. (1) [43]. Fig. 9(b) illustrates the consequences of the gate electrode work function on the transconductance. Due to reduced drain current, g_m reduces with the surge in the work function at an inferior V_{gs}. The maximum value of g_m is approximately the same for all work functions. However, the peak value shifts towards higher V_{gs} with a higher gate electrode work function. The parameter that mainly describes the device's switching behavior is the quality factor (QF). QF is the transconductance and subthreshold swing ratio, as defined in Eq. (2) [44,45]. QF variation concerning the different work functions is portrayed in Fig. 9(c). QF enhances initially with the increase in the work function but becomes almost constant for the higher work function values. It is so because the SS improves for the higher work function values, whereas the maximum

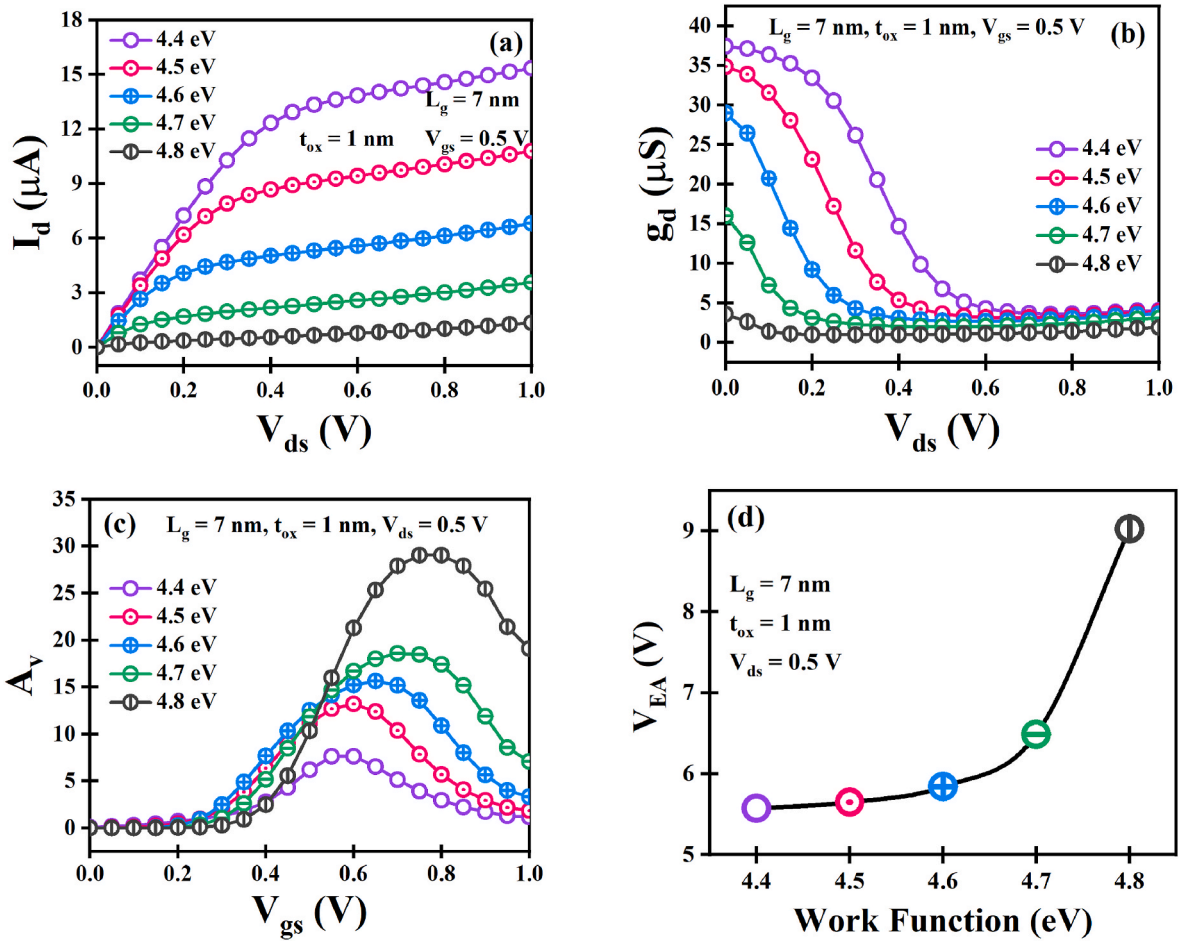

Fig. 10. Plot of (a) I_d, (b) g_d, (c) A_v, and (d) V_{EA} concerning the different gate electrode work functions.

$$QF = g_m/SS \quad (2)$$

$$TGF = g_m/I_d \quad (3)$$

$$A_v = (g_m / g_d) \quad (4)$$

$$V_{EA} = (I_d / g_d) \quad (5)$$

value of g_m is nearly identical. Eq. (3) defines the transconductance generation factor (TGF) as the g_m and I_d ratio [46]. TGF computes how current is controlled to get a specific amount of transconductance. Fig. 9 (d) depicts the plot of TGF against the different work functions considered. The maximum value of TGF is acquired for the 4.8 eV, whereas the lowest is for the 4.4 eV. However, the increase in the peak value decreases with a rise in the gate electrode work function.

Fig. 10(a–b) portrays the influence of the work functions on the device output characteristics and output conductance (g_d) at constant V_{gs}, respectively. The increase in the I_d is larger for lower drain-source voltages than for higher V_{ds}. Moreover, I_d decreases significantly with the surge in the gate electrode work function, indicating a boost in the device performance. The output conductance mainly describes the driving capability of any device. The g_d value must be low for enhanced analog performance, and the same is observed for the device with a 4.8 eV work function. Intrinsic gain (A_v) is the g_m and g_d ratio, while early voltage (V_{EA}) is the drain current and output conductance ratio, as defined in Eqs. (4) and (5) [47,48]. For improved analog performance, A_v and V_{EA} must acquire a superior value. The intrinsic gain and early voltage variations concerning the different gate electrode work functions are demonstrated in Fig. 10(c–d). The A_v and V_{EA} peak values increase by 280.73% and 62.12%, with a 0.4 eV increase in the work function. It is mainly because the output conductance improves considerably for the higher work function. Table 3 compares the influence of gate electrode work functions on the evaluated analog parameters. The table reflects the peak value of the parameters obtained at

Table 3
Overview of evaluated analog parameters of JAM-GS-GAA FinFET with different work functions.

Work Function	Parameters									
	I_{on} (μA)	I_{off} (A)	I_{on}/I_{off} ratio	SS (mV/dec)	g_m (μS)	QF (mS-dec/V)	TGF (V^{-1})	g_d (μS)	A_v	V_{EA} (V)
4.4 eV	22.52	1.03×10^{-7}	2.18×10^{2}	114.65	42.29	0.368	34.59	37.44	7.63	5.57
4.8 eV	17.23	6.88×10^{-12}	2.50×10^{6}	91.42	42.29	0.462	50.74	3.55	29.05	9.03

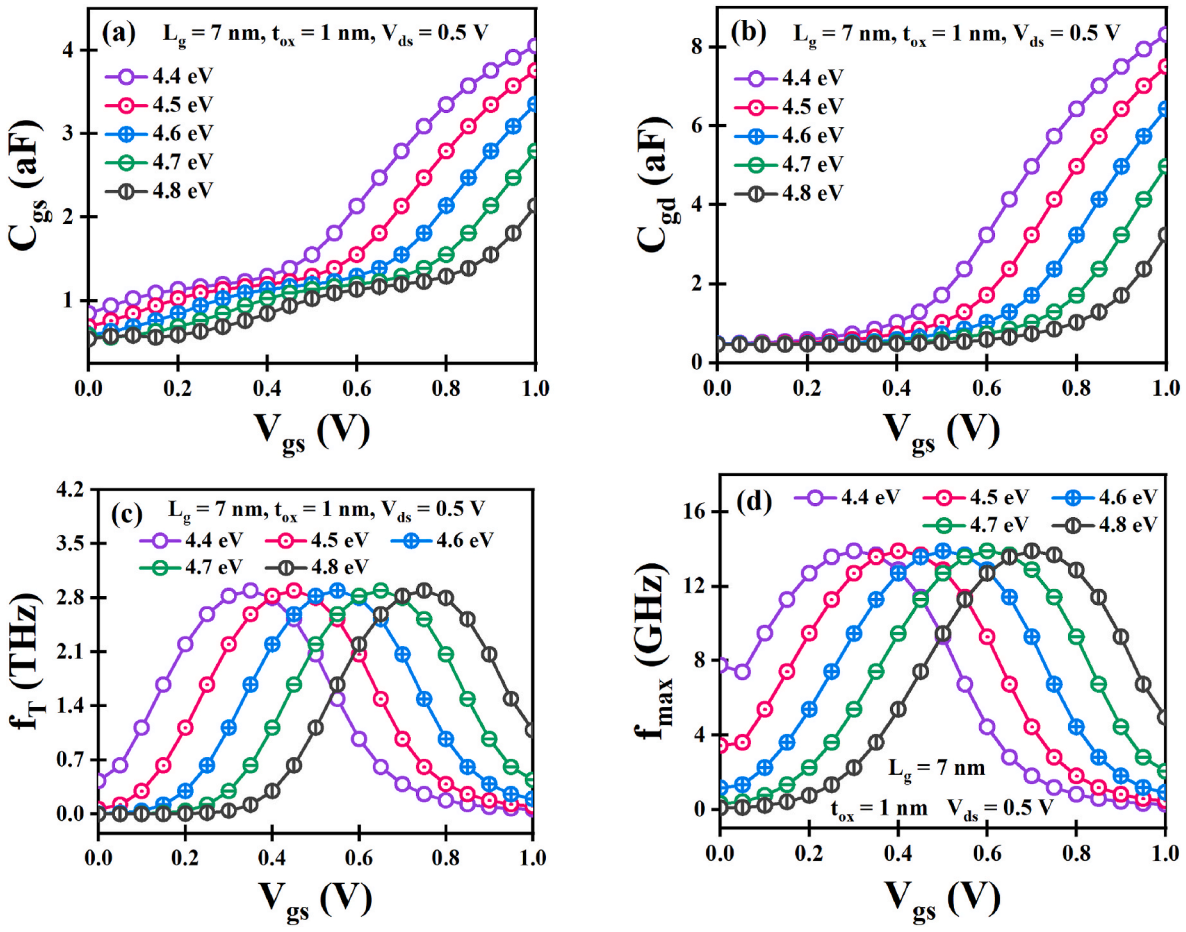

Fig. 11. (a) C_{gs}, (b) C_{gd}, (c) f_T, and (d) f_{max} plot against the gate electrode work functions considered.

$$f_T = g_m / 2\pi \left(C_{gs} + C_{gd}\right) \tag{6}$$

different V_{gs} and V_{ds}.

4.4. RF performance

The parameters like gate-source capacitance (C_{gs}), gate resistance (R_g), drain-source conductance (g_{ds}), and gate-drain capacitance (C_{gd}) are needed for the RF performance evaluation. These parameters are extracted at an operating frequency of 1 MHz using small-signal analysis. Fig. 11(a–b) depicts the C_{gs} and C_{gd} plots against the gate electrode work functions considered. It is noted that C_{gs} and C_{gd} decrease appreciably with a 0.4 eV increase in the work function. The frequencies at which current gain and unilateral power gain become unity (0 dB) are known as cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). Both parameters are evaluated using Eqs. (6) and (7) [49]. Fig. 11 (c–d) represents the plot of f_T and f_{max} against V_{gs} for different gate electrode work functions. Initially, both parameters increase with the V_{gs}, reach a maximum value, and then decrease with a further increase in the V_{gs}. The work function escalation shifts the peak value of f_T towards higher V_{gs}. However, the peak value is almost identical in all cases. The same trend follows for the f_{max}. The work function increase reduces the capacitances and the transconductance. As a result, the peak value remains constant for all the devices with different gate electrode work functions.

Eq. (8) computes the gain frequency product (GFP), the product of the A_v and f_T [50]. From a high-frequency perspective, GFP is a vital parameter. Fig. 12(a) depicts the variation of GFP for altered work functions against V_{gs}. The maximum value for the device with a 4.8 eV work function is obtained. This increment is due to the rise in the intrinsic gain with the work function. Gain bandwidth product (GBP) is evaluated using Eq. (9), depending on the g_m and C_{gd} [51]. The gate electrode work function's consequences on GBP are displayed in Fig. 12 (b). GBP follows the same trend as f_T and f_{max} for the same reason. Eqs. (10) and (11) calculate the crucial parameters transconductance frequency product (TFP) and gain transconductance frequency product (GTFP) [52]. TFP is the TGF and f_T product, while GTFP is the gain and TFP product. The alteration of the TFP and GTFP for the different work functions is outlined in Fig. 12(c–d). TFP follows the same trend as other parameters for the same reason. But GTFP significantly increases the gate electrode work function primarily due to the intrinsic gain. GTFP improves by 1169.30% when the work function is raised by 0.4 eV. The influence of gate electrode work functions on the evaluated RF parameters is compared in Table 4. It includes the peak value of different parameters for 4.4 and 4.8 eV work functions obtained at different V_{gs}. Table 5 provides an overview of the evaluated static, analog, and RF parameter trends with the gate electrode work function of JAM-GS-GAA FinFET compared to various existing devices [20–22,53–55]. All the trends (increment/decrement) mentioned are with respect to the increase in the value of the gate electrode work function. The parameter trends mentioned for different gate electrode work functions in the proposed device are observed to match those of the existing devices.

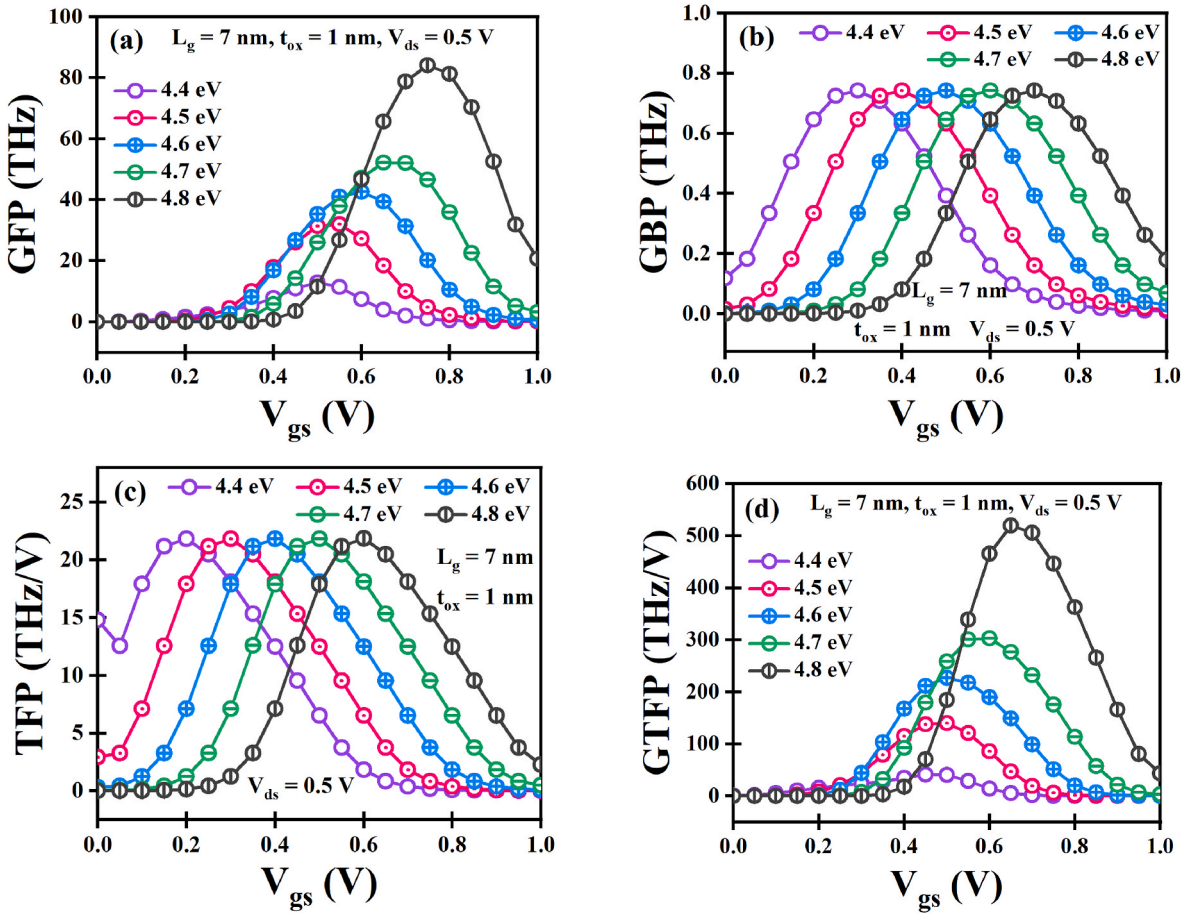

Fig. 12. The alteration of (a) GFP, (b) GBP, (c) TFP, and (d) GTFP for the different gate electrode work functions.

$$f_{max} = f_T \Big/ \sqrt{4\,R_g\left(g_{ds} + 2\pi f_T\,C_{gd}\right)} \tag{7}$$

$$GFP = \left(g_m / g_d\right) \times f_T \tag{8}$$

$$GBP = g_m \Big/ \left(20\pi \times C_{gd}\right) \tag{9}$$

$$TFP = \left(g_m / I_d\right) \times f_T \tag{10}$$

Table 4
Overview of evaluated RF parameters of JAM-GS-GAA FinFET with different work functions.

$$GTFP = \left(g_m / g_d\right) \times \left(g_m / I_d\right) \times f_T \tag{11}$$

Work Function	Parameters							
	C_{gs} (aF)	C_{gd} (aF)	f_T (THz)	f_{max} (GHz)	GFP (THz)	GBP (THz)	TFP (THz/V)	GTFP (THz/V)
4.4 eV	4.05	8.31	2.89	13.89	12.82	0.742	21.84	40.95
4.8 eV	2.13	3.23	2.89	13.89	84.10	0.742	21.85	519.78

5. Conclusion

This research paper inspected the static, analog, and RF performance of the gate electrode work function engineered JAM-GS-GAA FinFET for analog/RF applications. The performance of the JAM-GS-GAA FinFET and conventional FinFET has been compared, and it has been observed that JAM-GS-GAA FinFET performs far better than the conventional FinFET. For JAM-GS-GAA FinFET, the I_{on} enhanced by 17.81%, g_m by 35.14%, and QF by 56.42%, while I_{off} and I_{on}/I_{off} ratio improved by 96.15% and ~10^2 orders of magnitude, respectively. In addition, the various characteristics of JAM-GS-GAA FinFET are also compared with different published works. The efficacy of a JAM-GS-GAA FinFET has been found to be superior to that of comparable state-of-the-art devices. The proposed device's static characteristics, like the electric field, electron mobility, potential, and electron concentration, degrade while the analog and RF performance improves significantly with the 0.4 eV increase in the gate electrode work function. In comparison, results demonstrate that an increase in work function by 0.4 eV enhances

Table 5
Overview of parametric trends of JAM-GS-GAA FinFET with different existing devices.

Ref.	Year	W. F. Variation	Parametric Trends												
			E. F.	Potential	Elec. Conc.	I_{on}	I_{off}	I_{on}/I_{off} ratio	SS	g_m	g_d	A_v	C_{gd}	f_T	GTFP
[20]	2014	4.52 → 4.7	NA	NA	NA	↑	↓	NA	↑	↑	↓	↑	↓	↑	↑
[53]	2019	3.9 → 4.6	↓	↓	↓	↓	↓	↑	↓	NA	NA	NA	NA	NA	NA
[21]	2021	4.4 → 4.7	NA	NA	NA	↓	↓	↑	↓	↑	↓	↑	NA	↑	NA
[22]	2021	4.6 → 5.6	NA	↓	↓	↓	↓	↑	↓	↑	NA	NA	NA	NA	NA
[54]	2021	4.4 → 4.8	NA	NA	NA	↓	↓	↑	NA	↑	↓	↑	NA	↑	↑
[55]	2022	4.2 → 5.0	NA	NA	NA	↓	↓	↑	↓	↓	↓	↓	↓	↓	↓
This Work	–	4.4 → 4.8	↓	↓	↓	↓	↓	↑	↓	↑	↓	↑	↓	↑	↑

*NA – data not available, ↑ – increment, ↓ – decrement.

analog parameters like quality factor by 25.54%, switching ratio by 10^4 times, early voltage by two times, intrinsic gain by four times, and reduces subthreshold swing by 20.26%, leakage current by 10^4 times, output conductance by ten times. On the other hand, RF parameters also improve with the escalation in the gate electrode work function. GFP and GTFP increased by more than eight and ten times, respectively. Accordingly, engineers can create nanoelectronic devices using the gate electrode work functions (4.4 eV–4.8 eV) for analog/RF applications.

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Authors statement

Bhavya Kumar: Conceptualization, methodology, software, analysis, data curation, writing-original draft preparation. **Megha Sharma:** Conceptualization, analysis, data curation, writing-editing. **Rishu Chaujar:** Conceptualization, analysis, data curation, writing - review and editing at different stages, supervision.

Compliance with ethical standards

The authors have seen all the ethical standards and will follow them in the future.

Consent to participate and for the publication

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The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Junctionless-accumulation-mode stacked gate GAA FinFET with dual-k spacer for reliable RFIC design

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ABSTRACT

This study investigates how incorporating a dual-k spacer (SiO_2 + HfO_2) affects the RFIC design feasibility of a junctionless-accumulation-mode (JAM) stacked-gate (GS) gate-all-around (GAA) FinFET in the sub-10 nm range. The proposed device is compared with a conventional FinFET and those without a spacer, air, and a single-k spacer (SiO_2). At a low voltage power supply, fringing field effects raise the proposed device's on-current by 35.34% and reduce the off-current by more than 76 times compared to conventional FinFET, thereby improving electron velocity, energy band profiles, transconductance, device efficiency, etc. Thus, the proposed device is well-suited for high-performance CMOS circuits. Further investigation shows that integrating a dual-k spacer reduces the output conductance, which boosts the intrinsic gain and early voltage by five times the value recorded for conventional FinFET. Although the cut-off frequency drops by 15.98%, the GTFP and GFP soar by 475.67% and 352.25%, respectively. Consequently, JAM-GS-GAA FinFET with dual-k spacer is an encouraging device for low-power RFIC circuits.

1. Introduction

The scaling of transistors has expanded throughout the last many years. This has been done to escalate the maximum speed of operation that the electronic components are capable of while simultaneously increasing the number of available electronic components. Because of the diminutive size of CMOS devices, transistors are susceptible to significant short-channel effects (SCEs), which play a role in the loss of power [1–4]. Moreover, in short-channel devices, the device's I–V characteristics decrease due to the reduced gate control area across the channel. Multiple device topologies have been suggested to alleviate these difficulties, including multi-gate MOSFET [5], TFETs [6], HEMTs [7,8], and FinFETs [9–11]. FinFET technology is the driving force behind the current integrated circuit industry, which optimizes SCEs to achieve exceptional scalability, augment battery longevity, and minimize power consumption [12,13]. Increasing the number of gates across the channel improves the device's ability to regulate electrostatic fields. The development of the Gate All Around (GAA) configuration improved the sub-threshold characteristics and the device's performance [14,15]. Consequently, GAA FinFET devices may be much smaller.

An additional difficulty presented by continuous CMOS technology scaling is a rise in off-state leakage current (I_{off}) along with a decrease in gate oxide thickness (t_{ox}). Gate Stack (GS) configuration with a thin SiO_2 layer stabilizing the high-k dielectric and silicon substrate is implemented to suppress this rise in I_{off} [16]. GS design also eliminates mobility deterioration and instability of threshold voltage caused by the direct deposition of high-k dielectrics on silicon substrates [17,18]. Fabricating p-n junctions that are ultra-shallow and sharp in the sub-10 nm domain is a challenge. In response to Lilienfeld's results, Colinge proposed Junctionless (JL) transistors, which had continuous doping throughout [19]. Since JL transistors don't have a p-n junction and are inexpensive, they are simple to manufacture. As a result of the channel length improvements, JL devices are also less susceptible to SCEs. However, JL devices still can't attain the outstanding turn-off characteristics by completely emptying the channel in the OFF state [20]. A lower channel area doping concentration may quickly deplete charge carriers. However, this will decrease the drain current and increase the drain/source series resistance. The proposal to address the low channel doping concentration issue involves implementing Junctionless Accumulation Mode (JAM) FETs, which feature heightened doping levels in the drain and source regions [21,22]. JAM-GS-GAA FinFET was subsequently proposed.

This study uses a spacer configuration that elongates the separation between the drain and source contact terminals [23]. Nevertheless, the

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series resistance will rise if you extend the distance that separates two potential terminals. This is because there will be a lower on-state current (I_{on}). An underlap high-k spacer is a technical solution to this problem. Underlap high-k spacer engineering is a technique that reduces the influence of drain bias in the channel area, thereby improving device performance and minimizing SCEs [24]. Studies have shown that devices using high-k spacers in the underlap area have great control over the channel, improved I_{on}, and lower I_{off} [25–29]. But this has some additional serious consequences. The primary challenge of utilizing a solitary high-k spacer is the amplified fringe capacitance constituents [30], thereby delaying the circuit by coupling with the gate. Second, carrier mobility is hampered by induced trapped charges caused by Coulomb scattering at the silicon-dielectric interface [30]. Therefore, spacer analysis should be used strategically. Thus, reducing the utilization of a high-k spacer within the vicinity where fringing fields could produce elevated carrier densities within a restricted range would be advantageous. One fascinating new development is the dual-k spacer, which integrates a high-k spacer on the inside with a low-k spacer on the exterior to improve the I_{on} and subthreshold characteristics and lower the parasitic capacitance.

This work has considered five configurations: C_1, C_2, C_3, C_4, and C_5, with descriptions provided in Table 1. The C_1 configuration consists of a conventional tri-gate JAM-GS-FinFET. The tri-gate is upgraded to a GAA structure with no spacer in the C_2 configuration (JAM-GS-GAA-FinFET without spacer). Compared to the C_2 configuration, the manufacturing process of the C_3 and C_4 configurations involves incorporating an extra layer of a single-k spacer (JAM-GS-GAA-FinFET with a single-k spacer). The C_3 configuration features air with a dielectric constant of 1 in the spacer region, while the C_4 configuration comprises SiO_2 with a dielectric constant of 3.9. The JAM-GS-GAA-FinFET arrangement with a dual-k spacer is used in the C_5 configuration. The C_5 configuration employed a HfO_2 high-k spacer with a dielectric constant of 25 for the inner layer and a SiO_2 low-k spacer with a dielectric constant of 3.9 for the outer layer. Because silicon in SiO_2 makes the silicon channel more flexible, reducing the likelihood of encountering dangling bonds and interface traps. This research aims to describe the impact of dual-k spacers on multiple configurations under consideration and to measure the improvements in performance resulting from the implementation of the JAM-GS-GAA FinFET in the domains of static, analog, and RF FoMs. The remainder of the manuscript is: Section 2 covers device structure, physical models, and experimental calibration. Section 3 discusses device manufacturing feasibility. Section 4 analyzes the effects of dual-k spacers on various parameters. Section 5 concludes the paper's uniqueness.

2. Device architecture and simulation approach

In Fig. 1(a–c), we see the proposed device with dual-k spacers in its methodical 3D, horizontally sliced 2D, and 3D meshed designs. A comprehensive summary of the different parameters of device architecture is listed in Table 2. The structure's fins are made of silicon. The dual-k spacer separates into 5 nm (SiO_2) and 2.5 nm (HfO_2) spacer lengths, with the total spacer length (L_{sp}) being 7.5 nm. The gate oxide is built using HfO_2 and SiO_2. By setting $H_{Fin}/W_{Fin} = 2$, the width quantization condition [31,32] is guaranteed to be satisfied across all simulations. With reduced doping in the channel area compared to the source/drain area, all three areas are evenly doped with n-types to enhance performance and reduce parasitic capacitance. Titanium nitride (TiN) is the substance of preference for use in metal gates, which has superior characteristics and a work function of 4.65 eV [33]. The transfer characteristics were obtained by systematically increasing the gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) from 0 V to 1.5 V and 0 V to 0.5 V, respectively, with increments of 0.05 V. On the other hand, the output characteristics were obtained by ramping V_{gs} from 0 V to 0.5 V and V_{ds} from 0 V to 1.5 V, using a step size of 0.05 V.

Table 1
Details of different configurations used for comparison.

Configuration Name	Device Descriptions	Spacer Details (Name, Dielectric Constants)
C_1	JAM-GS-FinFET	NA
C_2	JAM-GS-GAA-FinFET without spacer	NA
C_3	JAM-GS-GAA-FinFET with single-k spacer	Air, k = 1
C_4	JAM-GS-GAA-FinFET with single-k spacer	SiO_2, k = 3.9
C_5	JAM-GS-GAA-FinFET with dual-k spacer	SiO_2, k = 3.9 and HfO_2, k = 25

All the considered configurations are simulated with the assistance of the Atlas 3D simulator [34], with the Poisson and Continuity equations serving as the general basis for the modelling. However, formulae and supplementary physical models are required to obtain more credible and precise results. Therefore, many different physical models are built into the scenarios. The consequences of quantum confinement are a critical factor that cannot be disregarded in rapidly scaling systems. It is for this reason that the Bohm Quantum Potential (BQP) model is incorporated [34], which comprises a position-dependent quantum potential (Q). Further models considered are Fermi-Dirac statistics, Crowell-Sze impact ionization, concentration-dependent mobility, Klaassen tunneling, SRH recombination, and bandgap narrowing [34]. Incorporating Fermi-Dirac statistics is necessary to accommodate the characteristics of heavily doped materials. The Crowell-Sze model incorporates the phenomenon of impact ionization. The concentration-dependent mobility model has been activated to establish a correlation between the mobility of carriers in low fields at a temperature of 300 K and the concentration of impurities. The band-to-band Klaassen tunneling model accounts for direct and indirect electron tunneling between the conduction and valence bands. Implementing the SRH recombination model with a fixed carrier lifetime of 1×10^{-7} s accounts for the generation and recombination effects. The model of bandgap narrowing has been incorporated to accommodate the reduction in the separation of the bandgap due to the occurrence of intense doping. Newton and Block iteration solve all carrier motion math issues [34].

In order to verify the physical models, the GAA FinFET is validated with the actual results of Lee et al. [35]. We used the published parameters for the device dimensions and anticipated silicon throughout the fin region to check the accuracy of the models. Fig. 2(a) shows the output characteristics of the GAA FinFET device at varying gate voltages, and Fig. 2(b) shows the transfer characteristics at varying drain voltages. The model selections are supported by the high degree of alignment between the actual and simulated output and transfer features.

3. Fabrication feasibility

Fig. 3 presents a detailed procedure for the fabrication of JAM-GS-GAA FinFET with dual-k spacer, showcasing the practicality of the proposed device. The first stage involves thinning the silicon film, which is then succeeded by fin patterning through the self-aligned quadruple patterning (SAQP) technique [36]. Implementing two consecutive self-aligned double patternings (SADP) techniques to augment feature density is called self-aligned quadruple patterning (SAQP). The process of oxidation and etching is employed after the fin patterning. The deposition of the gate dielectric (SiO_2/HfO_2) onto the silicon interfacial layer is carried out through the utilization of atomic layer deposition (ALD) [37]. The gate dielectric is then covered with a metal gate made of TiN using electron beam evaporation at room temperature [37]. High-k spacers (HfO_2) are deposited on both sides, and source/drain extensions are produced utilizing tilt angle implants to achieve symmetric doping profiles [38]. Next, a photoresist mask is created over the gate and spacers, followed by the formation of low-k spacers (SiO_2) within the

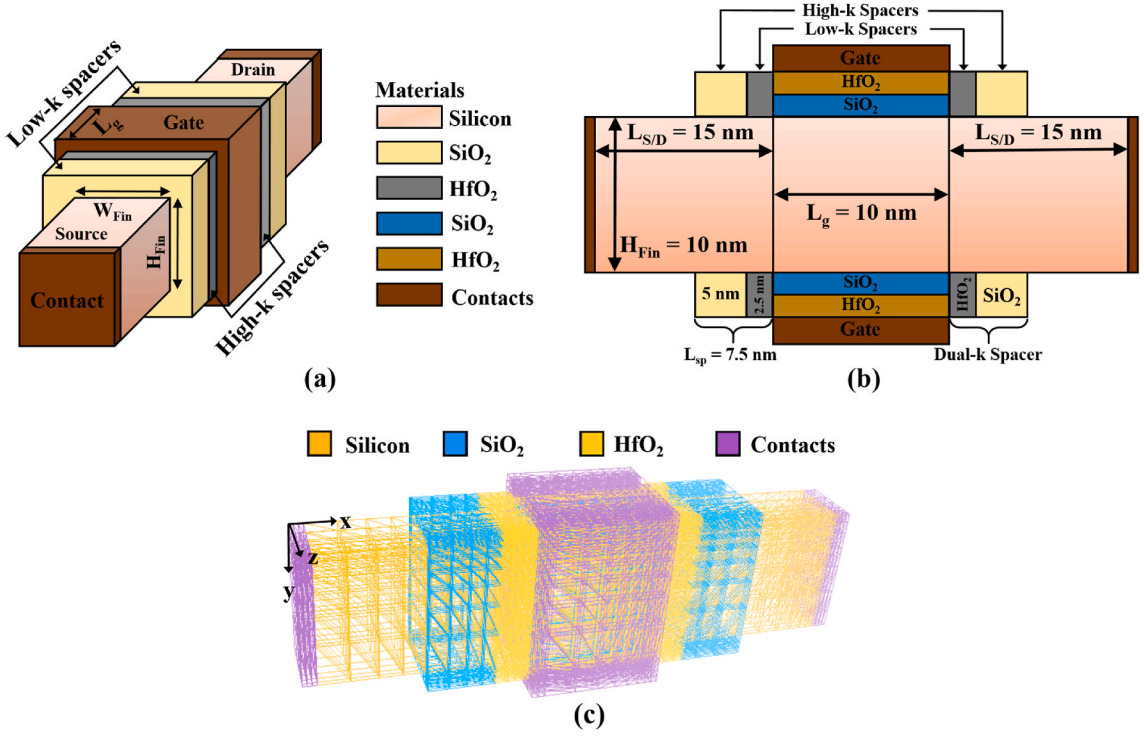

Fig. 1. (a) Methodical 3D, (b) horizontally sliced 2D, and (c) 3D meshed designs of the proposed JAM-GS-GAA FinFET device with dual-k spacers.

Table 2
Values of different parameters used for simulation.

Parameters	Symbol	Value	Unit
Source/Drain Length	$L_{S/D}$	15	nm
Gate Length	L_g	10	nm
Spacer Length	L_{sp}	7.5	nm
Oxide Thickness	t_{ox}	1	nm
Fin Height	H_{Fin}	10	nm
Fin Width	W_{Fin}	5	nm
Channel Doping	N_{Ch}	1×10^{16}	cm^{-3}
Source/Drain Doping	$N_{S/D}$	5×10^{18}	cm^{-3}
Work Function	φ_m	4.65	eV
Temperature	T	300	K
Gate-Source Voltage	V_{gs}	1.5	V
Drain-Source Voltage	V_{ds}	0.5	V

remaining extension [38]. The implantation of source and drain regions is followed by a spike annealing process to activate the dopants present in the source and drain regions. The formation of source and drain contacts is followed by the deposition of metal interconnect layers [39]. The device fabrication process is finalized by executing additional backend processing steps, including salicidation, metalization, and etching. The JAM-GS-GAA FinFET, featuring a dual-k spacer, is fabricated and undergoes testing and characterization to evaluate its electrical characteristics.

4. Results and discussion

This section compares the five configurations to examine the effectiveness of the JAM-GS-GAA-FinFET with a dual-k spacer on important static and analog/RF performance metrics. The static parameters like the electron velocity, electric field, potential, and band energy profiles are computed at a constant $V_{gs} = 1.5$ V and $V_{ds} = 0.5$ V to quantify the electrical behavior of the device. Fig. 4(a and b) exhibits the electric field and potential contour plots along the channel across the range of configurations. In Fig. 5(a), the peak values of the electric field and potential in the channel area are displayed against various configurations. It can be seen that the peak value for both electric field and

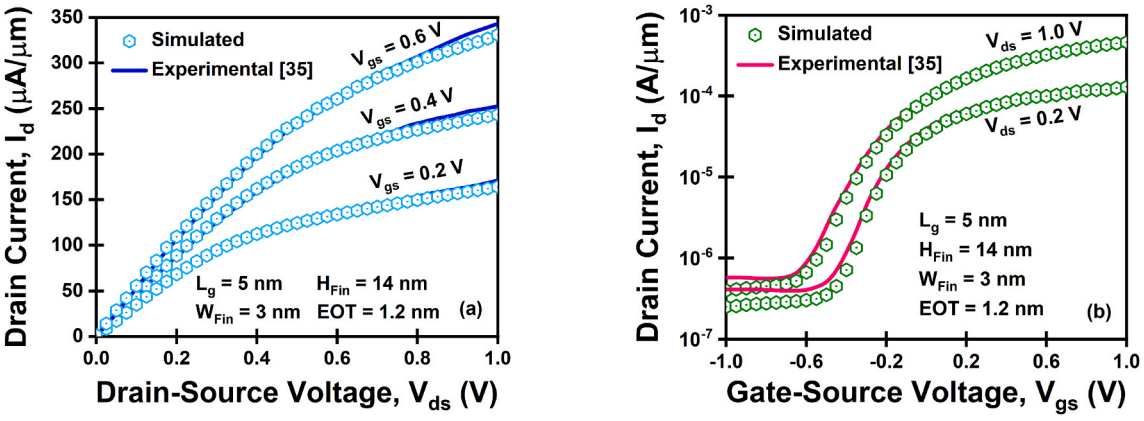

Fig. 2. Experimental calibration of the (a) output and (b) transfer characteristics of the GAA FinFET device.

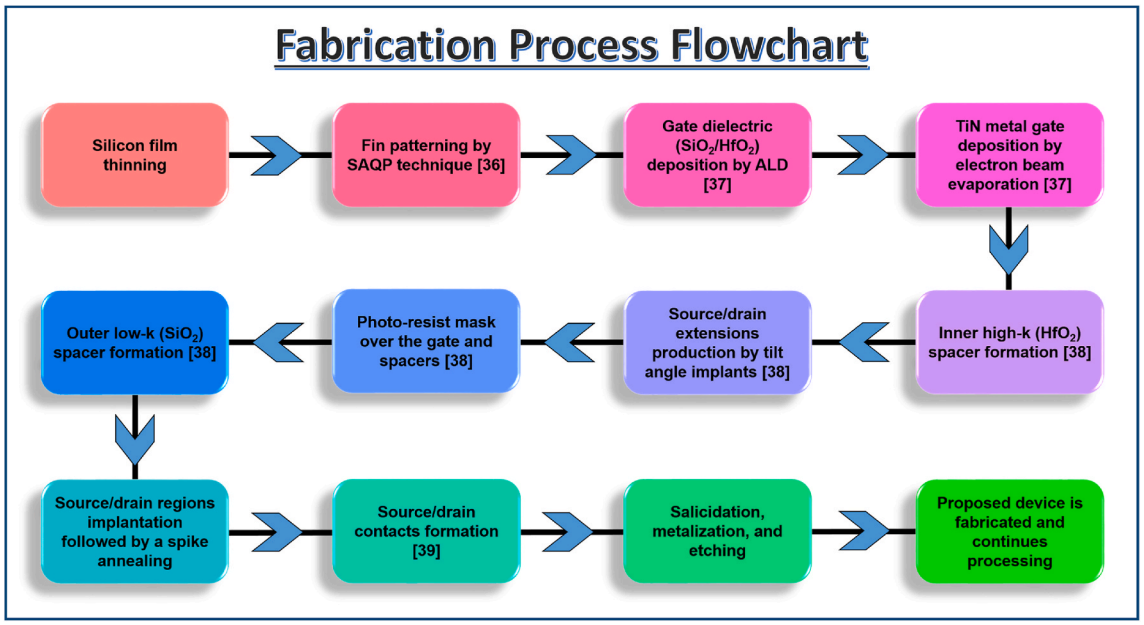

Fig. 3. Fabrication process flowchart for the JAM-GS-GAA FinFET device with dual-k spacers.

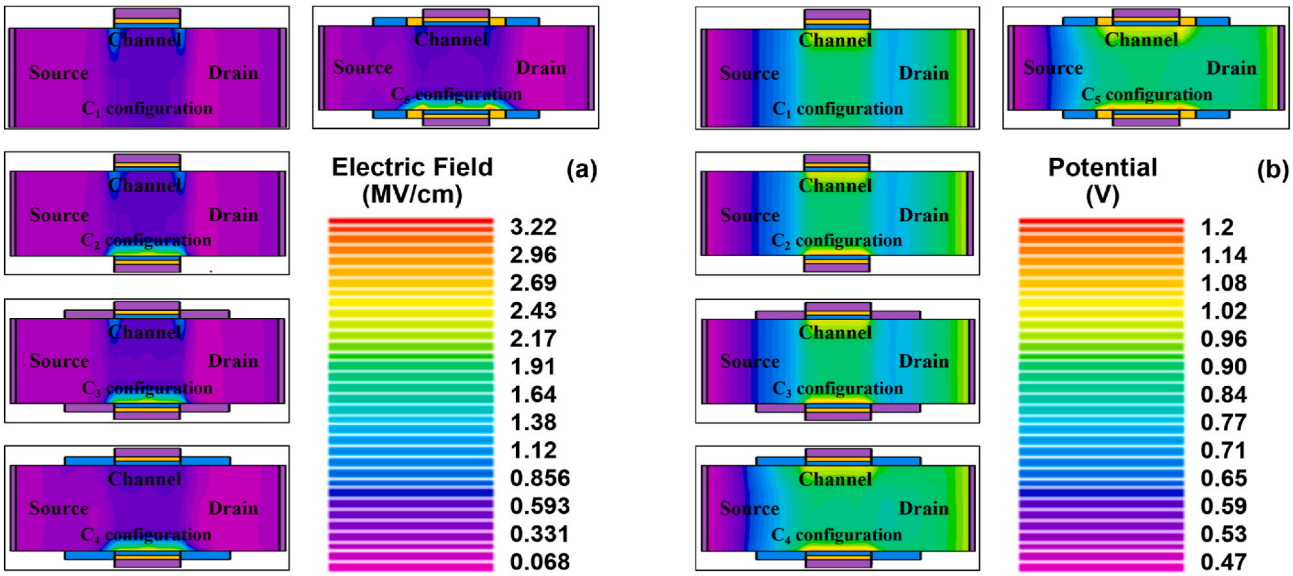

Fig. 4. (a) Electric field and (b) potential contour plots along the channel across the range of configurations.

potential is observed for the C_5 configuration because of the gate fringing fields that propagate through the high-k spacers. The variation in electron velocity across various configurations is demonstrated in Fig. 5(b). The incorporation of a dual-k spacer increases electron mobility, thereby augmenting the velocity of electrons. Accordingly, a discernible increase in the velocity of the electrons can be seen in the channel region when the C_5 configuration is utilized. Fig. 5(c) portrays the valence and conduction band energy profiles along the channel against V_{gs} for the five considered configurations. Analysis of Fig. 5(c) indicates that a notable barrier between the channel and drain is present in the C_1 configuration. In contrast, the barrier height is considerably reduced in the C_5 configuration because of the elevated fringing fields in the underlap zone, thus amplifying the effective channel width.

Fig. 6(a) depicts the variation in ON-current (I_{on}) against the different configurations. The I_{on} current is the value of the drain current obtained at $V_{gs} = 1.5$ V and $V_{ds} = 0.5$ V. It can be seen that maximum I_{on} is observed for the C_5 configuration. I_{on} is 35.34% higher for the C_5 configuration than the C_1 configuration. It is attributed to the effects of the fringing field in the underlap zones. The OFF-current (I_{off}) for considered configurations is plotted in Fig. 6(b). The I_{off} current is the value of the drain current obtained at $V_{gs} = 0$ V and $V_{ds} = 0.5$ V. The value of I_{off} found for C_1 is 4.24×10^{-11} A, which decreases dramatically to 5.54×10^{-13} A for the C_5 configuration, for an improvement of over 76 times. This is because of the increase in spacer area; the depletion region increases, resulting in a wider fringing region and consequently better I_{off} and SCEs. Moreover, because the I_{off} is exponentially dependent on the threshold voltage (V_{th}), an increase in V_{th} for the C_5 configuration (Fig. 6(d)) also reduces the I_{off}. Fig. 6(c) displays the switching ratio (I_{on}/I_{off}) of the different devices. The C_5 configuration has a greater I_{on} and a smaller I_{off} than the C_1 configuration, leading to an I_{on}/I_{off} ratio roughly 10^2 times higher. Fig. 6(d) displays the V_{th} shift across the range of configurations studied. The V_{th} shows an

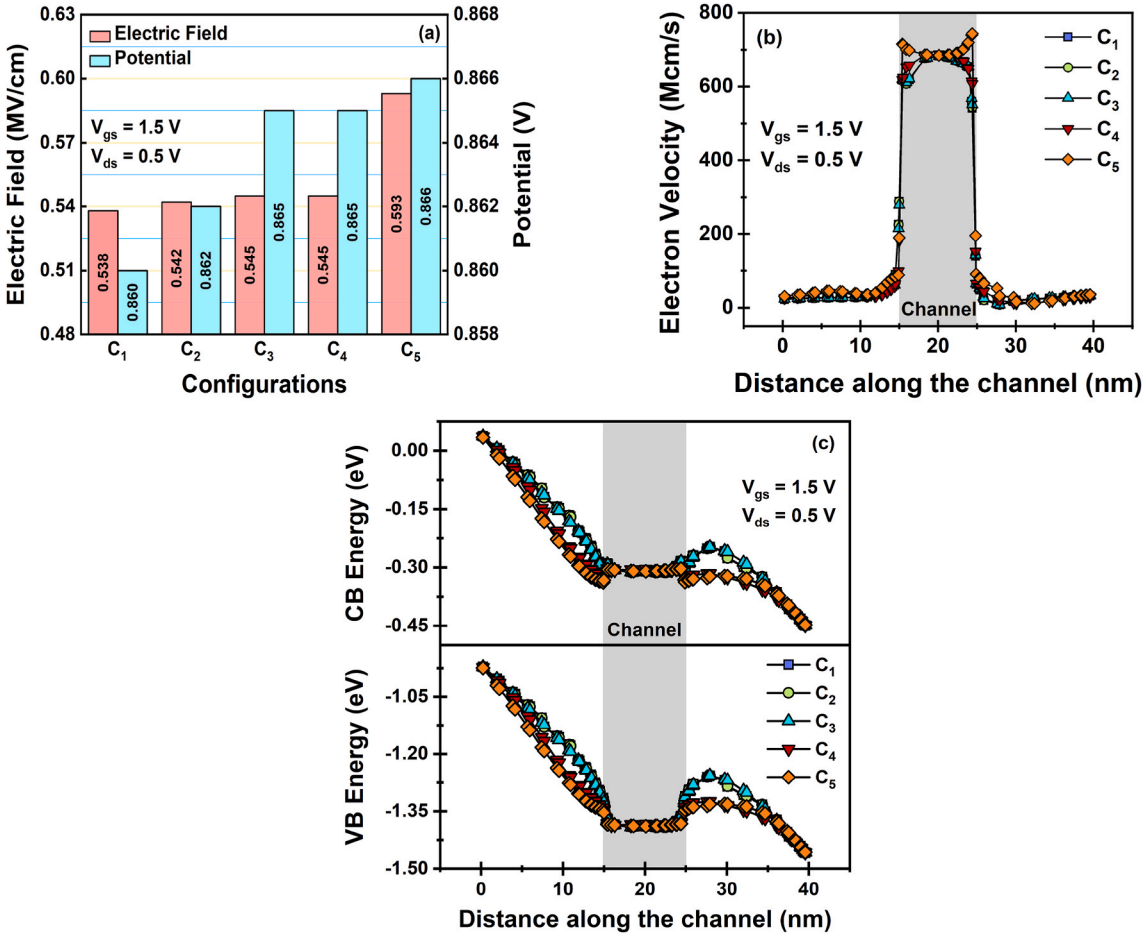

Fig. 5. Plot of (a) electric field and potential peak values, (b) electron velocity, and (c) valence and conduction band energy profiles across various configurations.

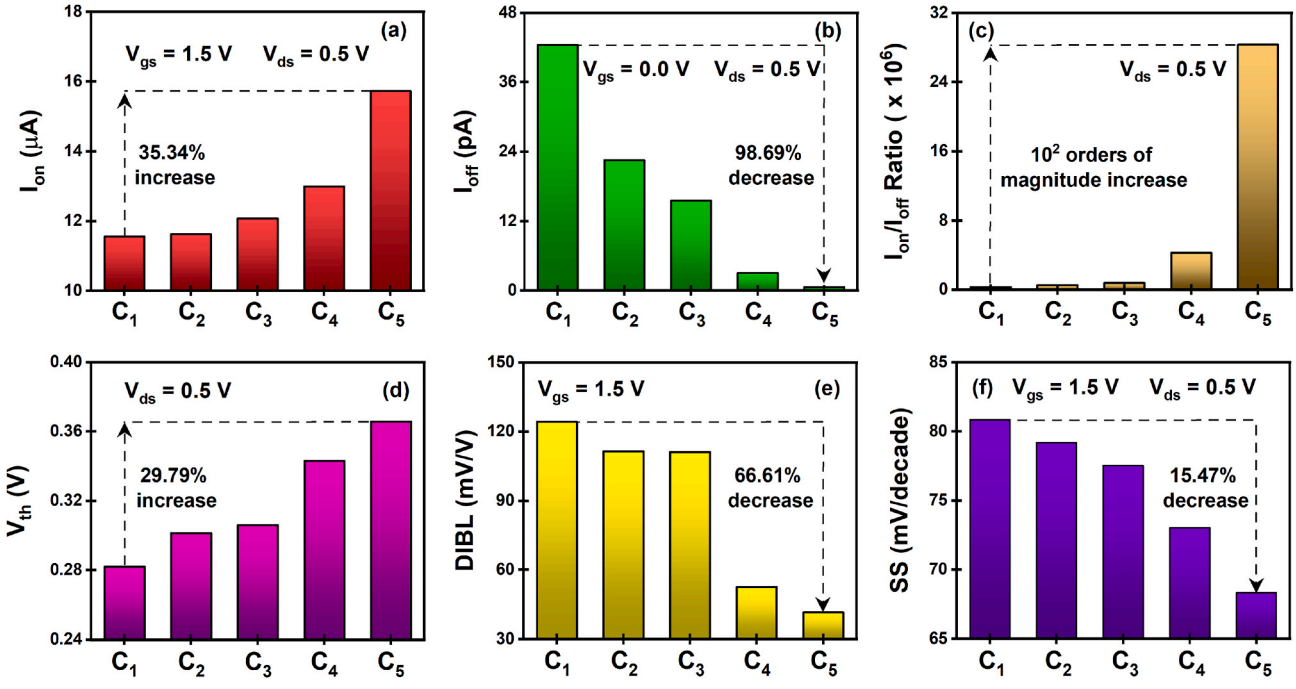

Fig. 6. Variation in (a) I_{on}, (b) I_{off}, (c) I_{on}/I_{off} ratio, (d) V_{th}, (e) DIBL, and (f) SS against the different configurations.

improvement of 29.79% for the C_5 configuration related to the C_1 configuration. This shows that the subthreshold device characteristics are enhanced as V_{th} rises linearly along with the spacer dielectric constant rise. Drain-induced-barrier-lowering (DIBL) derived using Eq. (1) indicates drain bias management on the potential barrier in the channel region [40]. Fig. 6(e) shows the DIBL plot for all five configurations. DIBL recorded for the C_1 configuration is 124.16 mV/V, which decreases to 41.46 mV/V for the C_5 configuration, improving SCEs by 66.61%. The leaking currents caused by the device's characteristics are indicated by the subthreshold swing (SS) metric, making it an essential one to measure. In order to boost SCEs, it is advised to decrease the amount of SS of all devices, as depicted in Fig. 6(f). The decrease in SCEs of 15.47% for the C_5 configuration demonstrates the success of the proposed device.

$$\mathrm{DIBL} = \left|(V_{th})_{V_{ds}=0.5V} - (V_{th})_{V_{ds}=0.1V}\right| \Big/ (0.5-0.1) \tag{1}$$

The output characteristics (I_d - V_{ds}) at fixed V_{gs} for the different configurations are plotted in Fig. 7(a). Initially, with a rise in V_{ds}, the I_d rises exponentially before levelling off. The I_d is significantly lower for the C_5 configuration than the C_1 configuration. This is because, for C_1, C_2, and C_3 configurations, as the V_{ds} is increased, the depletion region located at the drain end undergoes expansion in the channel region, thereby reducing the effective channel length [41,42]. This decrease in the effective channel length results in a phenomenon known as channel length modulation (CLM), which in turn causes a rise in the drain current. In contrast, the CLM effect is mitigated in C_4 and C_5 configurations by using underlap single-k or dual-k spacers, which significantly reduces the width of the drain depletion region and lessens the impact of drain bias in the channel area [24]. Thus, the C_5 configuration exhibits improved device performance and stability due to good control over CLM and DIBL (as shown in Fig. 6(e)). The output conductance (g_d) primarily characterizes a device's propulsion capacity. The g_d must be low to achieve improved device performance. Fig. 7(b) exhibits the output conductance for the configurations considered at fixed V_{gs}. As V_{ds} increases, the g_d initially drops before stabilizing at an undeviating value. Further, it can be seen that the g_d is lowest for the C_5 configuration. The g_d value reduces by 21.13% for the C_5 configuration related to the C_1 configuration. The output resistance (R_{out}) determines the device's useable power gain, which is the opposite of output conductance ($R_{out} = 1/g_d$). Fig. 7(c) depicts the variation of R_{out} against V_{ds} for all five considered configurations. Initially, the R_{out} rises, reaches a peak value, and then starts decreasing with a rise in V_{ds}. The R_{out} peak value obtained for the C_1 arrangement is 0.84 MΩ, which is raised more than four times to 3.58 MΩ for the C_5 arrangement.

$$g_m = \partial I_d / \partial V_{gs} \tag{2}$$

$$\mathrm{TGF} = g_m / I_d \tag{3}$$

For a particular V_{ds}, the ratio of the drain current to the gate-source voltage is measured by the transconductance (g_m), and it is given by Eq. (2) [43,44]. Noise efficiency, offset, DC gain, and bandwidth are all controlled by the g_m in an amplifier. As defined in Eq. (3), the transconductance generation factor (TGF) measures a device's efficiency at converting DC electricity to AC current [45]. The TGF also reflects a device's signal amplification capabilities, albeit at the expense of some electricity. Fig. 8(a) displays a collaborated plot of g_m and TGF against V_{gs} for the different configurations. Because the implication of a dual-k spacer lowers the potential barrier and escalates the gate effective length, the highest g_m value is obtained for the C_5 configuration. In Fig. 8 (a), the TGF value is higher for all combinations at low V_{gs} and decreases afterward for higher V_{gs} due to enhanced drain current. The C_5 configuration has the highest TGF compared to the others because it has the highest g_m, and a higher g_m number indicates a higher TGF value. The quality factor (QF) is one of the most crucial criteria for evaluating the device's switching behavior. It is the ratio of transconductance to the subthreshold swing (QF = g_m/SS) [46,47]. The QF is calculated using the maximum value of g_m (obtained at 0.7 V) and directly impacts the switching behavior's reliability. Fig. 8(b) depicts the QF for the various device structures examined. The QF increases linearly with the maximum value being obtained for the C_5 configuration. The C_5 configuration demonstrates a 46.75% increase in QF compared to the C_1 configuration, attributed to enhancements in g_m and a reduction in SS. A higher g_m, TGF, and QF values suggest a greater enhancement factor, ensuring the device/component can be used in analog applications.

$$V_{EA} = (I_d / g_d) \tag{4}$$

$$A_v = (g_m / g_d) \tag{5}$$

According to Eqs. (4) and (5), the ratio of the drain current to the output conductance is the early voltage (V_{EA}), and the ratio of the transconductance to output conductance is the intrinsic gain (A_v) [45]. A higher value for V_{EA} and A_v will lead to better analog performance. The variation in V_{EA} and A_v against the V_{gs} across the range of configurations studied is shown in Fig. 8(c and d). When V_{gs} increases, both V_{EA} and A_v first increase, peak, and then begin to decrease. The values of both V_{EA} and A_v are significantly higher for the C_5 configuration than the others. This is primarily because the output conductance improves considerably in addition to the improvement in drain current and transconductance with an implication of a dual-k spacer. Fig. 9 exhibits the spider-chart representation of the variance in peak values of g_m, TGF, V_{EA}, and A_v over the five different combinations. The g_m peak value increases from 24.39 μS (C_1 configuration) to 30.25 μS (C_5 configuration), thereby exhibiting a rise of 24.03%. The TGF peak value rises by 39.12%, going from 63.09 V^{-1} (C_1 configuration) to 87.77 V^{-1} (C_5 configuration). Similarly, for the C_5 configuration, V_{EA} and A_v increased approximately fivefold to the values obtained for the C_1 configuration. For the C_1 configuration, V_{EA} is 9.18 V, and A_v is 19.52; for the C_5 configuration, both parameters are raised to 44.92 V and 107.23, respectively.

The RF performance assessment necessitates the use of factors such

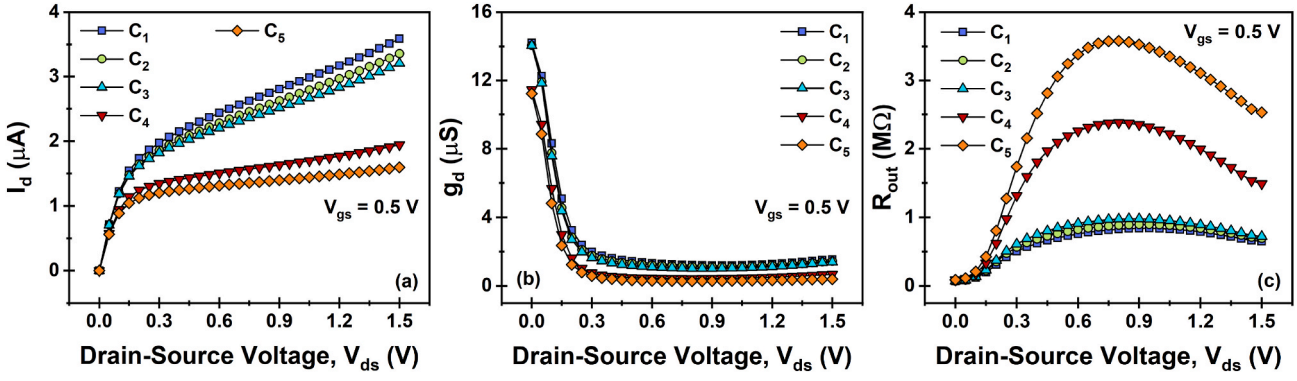

Fig. 7. Plot of (a) I_d, (b) g_d, and (c) R_{out} against V_{ds} for all five considered configurations.

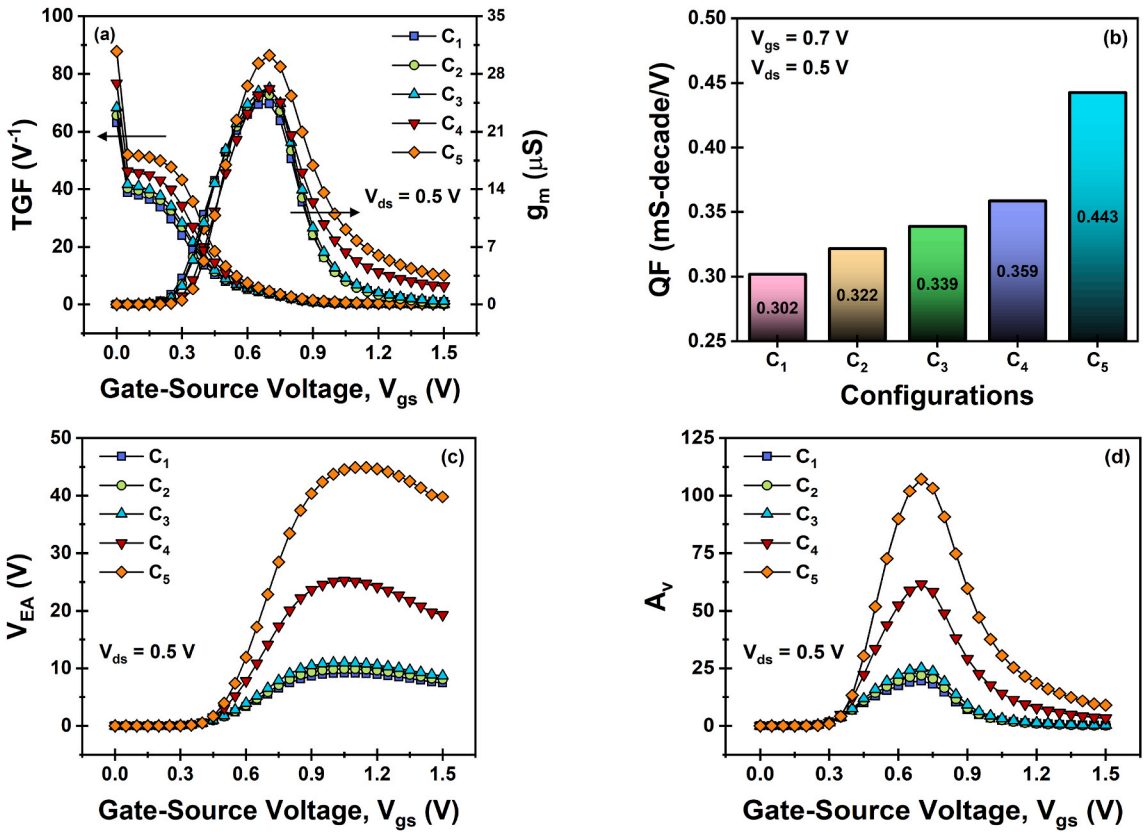

Fig. 8. Variance of (a) g_m and TGF, (b) QF, (c) V_{EA}, and (d) A_v against V_{gs} for all five considered configurations.

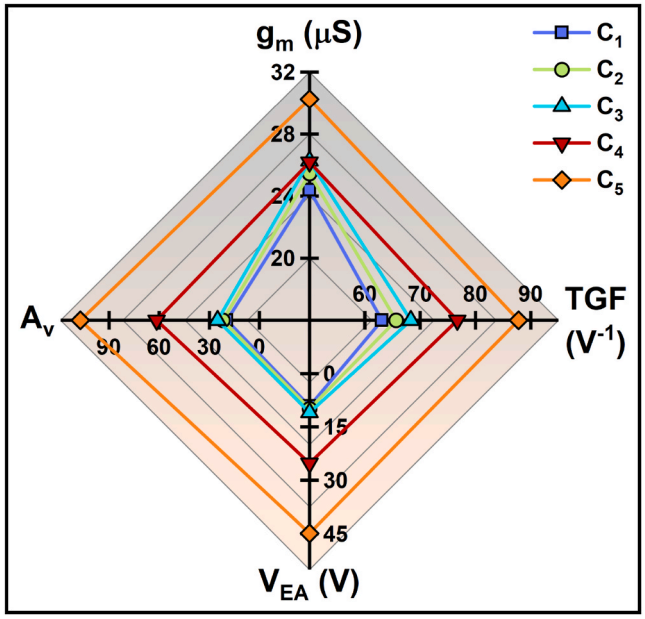

Fig. 9. Spider-chart representation of the variance in peak values of g_m, TGF, V_{EA}, and A_v over the five different combinations.

as gate resistance (R_g), drain-source conductance (g_{ds}), gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), and total-gate capacitance (C_{gg}). The parameters R_g, g_{ds}, C_{gs}, C_{gd}, and C_{gg} were determined through AC small-signal analysis conducted at a frequency of 1 MHz. During the analysis, the gate-source voltage was systematically increased from 0 V to 1.5 V in increments of 0.05 V, while the drain-source voltage was ramped from 0 V to 0.5 V with a step size of 0.05 V. The parameters like g_{ds}, C_{gs}, C_{gd}, and C_{gg} can be obtained through direct extraction, while the value of R_g was determined with the assistance of Y-parameters using the formula $R_g = (\text{Real } Y_{11})/(\text{Imag } Y_{11})^2$ [48,49], where Y_{11} is known as the input admittance. Due to increased effective channel width and enhanced electrostatic control, the value of R_g is observed to be lowest for the C_5 configuration and greatest for the C_1 configuration. Fig. 10(a–c) displays a plot of C_{gs}, C_{gd}, and C_{gg} against V_{gs} for the different configurations. The C_{gs}, C_{gd}, and C_{gg} for all the configurations stay the same in the subthreshold range. However, a substantial variation in the C_{gs}, C_{gd}, and C_{gg} is found beyond the subthreshold areas, particularly in the C_5 configuration. This is because the gate-induced fringing field facilitates the passage of charge carriers from the source to the drain side, and the gate capacitance is directly proportional to the dielectric permittivity ($C \propto k$).

$$f_T = g_m / 2\pi \left(C_{gs} + C_{gd}\right) \tag{6}$$

$$f_{max} = f_T \Big/ \sqrt{4\, R_g \left(g_{ds} + 2\pi f_T\, C_{gd}\right)} \tag{7}$$

$$GBP = g_m / \left(20\pi \times C_{gd}\right) \tag{8}$$

The current gain and unilateral power gain are unity (0 dB) at the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}), respectively. Eqs. (6) and (7) are used to figure out the values of both factors [50,51]. Fig. 11(a) shows the peak value of f_T obtained at $V_{gs} = 0.6$ V for the five different configurations. The maximum g_m value is achieved at a consistent V_{gs} value across all structures. Consequently, the peak value of the f_T is also attained at a specific V_{gs} value due to its direct correlation with g_m. The topmost value of f_T for the C_1 configuration is 1.94 THz, which reduces to 1.63 THz for the C_5 configuration owing to the increase in the gate capacitances. The variation of f_{max} against V_{gs} for the distinct configurations is depicted in Fig. 11(b). Due

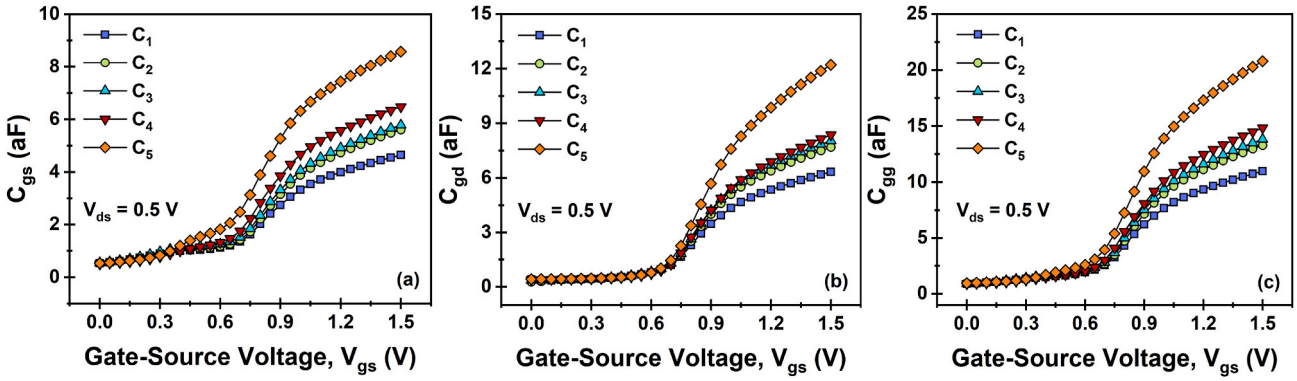

Fig. 10. Plot of (a) C_{gs}, (b) C_{gd}, and (c) C_{gg} against V_{gs} for the different configurations.

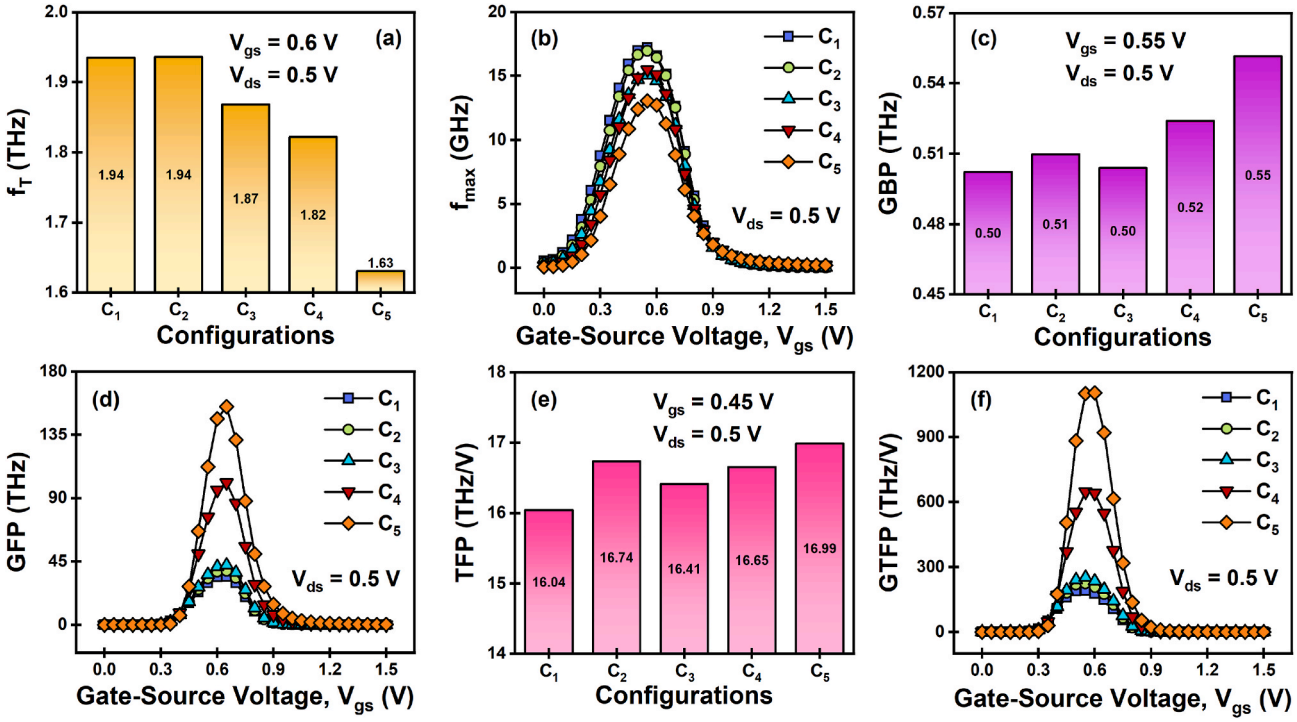

Fig. 11. Variance in (a) f_T, (b) f_{max}, (c) GBP, (d) GFP, (e) TFP, and (f) GTFP against the different configurations.

to the rise in gate capacitances, f_{max} is lowered by 24.10% for the C_5 compared to the C_1 configuration. The Gain Bandwidth Product (GBP) can be calculated by Eq. (8), depending on the C_{gd} and g_m values [52]. Fig. 11(c) illustrates the maximum value of GBP obtained at $V_{gs} = 0.55$ V across the five varied configurations. Again, the GBP peak value is attained at a specific V_{gs} value due to its direct correlation with g_m. The maximum value of GBP for the C_1 configuration is 0.50 THz, but it escalates to 0.55 THz for the C_5 configuration because of the increase in the transconductance.

$$GFP = (g_m / g_d) \times f_T \tag{9}$$

$$TFP = (g_m / I_d) \times f_T \tag{10}$$

$$GTFP = (g_m / g_d) \times (g_m / I_d) \times f_T \tag{11}$$

The product of the A_v and f_T is the gain frequency product (GFP), which is also shown in Eq. (9) [53]. GFP is an important metric to consider when working with high frequencies. Fig. 11(d) exhibits the change in GFP with respect to V_{gs} for the five considered configurations. When V_{gs} increases, GFP first increase, peak at 0.65 V, and then begin to decrease. For the C_5 configuration, the value of GFP increases by more than four times the value obtained for the C_1 configuration. This substantial increase in GFP can be attributed to the improvement in intrinsic gain. Transconductance frequency product (TFP) and gain transconductance frequency product (GTFP) can be determined using Eqs. (10) and (11), respectively [54]. TFP is the f_T and TGF product, whereas GTFP is the intrinsic gain, TGF, and f_T product. Fig. 11(e) displays the peak TFP obtained at $V_{gs} = 0.45$ V for the five different configurations. The TFP peak value is achieved at a particular V_{gs} value owing to its direct association with g_m and f_T. The C_1 configuration yields a peak TFP value of 16.04 THz, whereas the C_5 configuration has a higher TFP peak of 16.99 THz. Since the decrease in f_T offsets the escalation in TGF, the resulting increase in TFP is modest. The variation in GTFP against the V_{gs} across the range of configurations studied is shown in Fig. 11(f). The trend observed in GTFP is analogous to that of GFP, owing to a similar underlying cause. The GTFP value for the C_5 configuration increases by more than five times compared to the value obtained for the C_1 configuration owing to intrinsic gain and TGF improvements.

There is no denying that the addition of a dual-k spacer structure makes the fabrication process more complicated. Therefore, we have

compared the dual-k spacer structure (C_5 configuration) and the single-k spacer structure with SiO_2 (C_4 configuration) to highlight better the benefits of the more complicated dual-k spacer structure. We assessed the extent of improvement in the parameters by the percentage change following the transition from the C_4 configuration to the C_5 configuration. Fig. 12 depicts a graphical representation of the percentage improvement of the mentioned parameters. The results indicate that transitioning from a C_4 configuration to a C_5 configuration yields significant enhancements in I_{off}, V_{EA}, A_v, GTFP, and GFP, with improvements of 81.78%, 78.17%, 73.98%, 70.28%, and 53.46%, respectively. Further, I_{on}/I_{off} ratio rises seven times with substantial improvement in other parameters, as shown throughout the paper. Thus, the dual-k spacer structure offers substantial advantages despite the complexity of its fabrication. In addition, the difference between the different static, analog, and RF FoMs (ΔFoMs) of C_5 and C_1 configurations have been evaluated using Eq. (12). Table 3 displays the ΔFoMs for the assessed parameters. The observed enhancements in the static, analog, and RF ΔFoMs (barring the f_T and f_{max}) signify that the C_5 configuration outperforms the C_1 configuration, thus corroborating the efficacy of our proposed JAM-GS-GAA-FinFET with dual-k spacer device structure.

$$(\Delta FoMs) = (FoMs)_{C_5\ Conf.} - (FoMs)_{C_1\ Conf.} \quad (12)$$

5. Conclusion

The impression of adding a dual-k spacer on the RFIC design viability of a JAM-GS-GAA FinFET in the sub-10 nm region is investigated in this research. The calculated findings of the proposed device are compared to those of a typical FinFET and the devices without a spacer (no spacer), with air, and with a single-k spacer (SiO_2). In a study conducted, it was found that the proposed device improves the ON-current, OFF-current, transconductance, device efficiency, electron velocity, conduction and valence band energy profiles, etc., due to the fringing field effects. Due to its advantageous characteristics, the proposed device is an ideal option for high-performance CMOS circuits. Further analysis demonstrates that integrating a dual-k spacer decreases the output conductance, resulting in a fivefold enhancement of the intrinsic gain and early voltage compared with the figures observed for conventional FinFETs. Although the cut-off frequency and maximum oscillation frequency drop are observed, the gain transconductance frequency product and gain frequency product skyrocket by more than five times. To that end, JAM-GS-GAA FinFET with dual-k spacer can be seen as a potential element in future low-power RFIC designs.

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Author statement

Bhavya Kumar: Conceptualization, methodology, software, analysis, data curation, writing-original draft preparation. Megha Sharma: Conceptualization, analysis, data curation, writing-editing. Rishu Chaujar: Conceptualization, analysis, data curation, writing - review and editing at different stages, supervision.

Compliance with ethical standards

The authors have seen all the ethical standards and will follow them in the future.

Consent to participate and for the publication

The study article is from a "non-life science journal." 'Not Applicable.' However, the authors have studied all journal regulations and agreed with authorities for further processing.

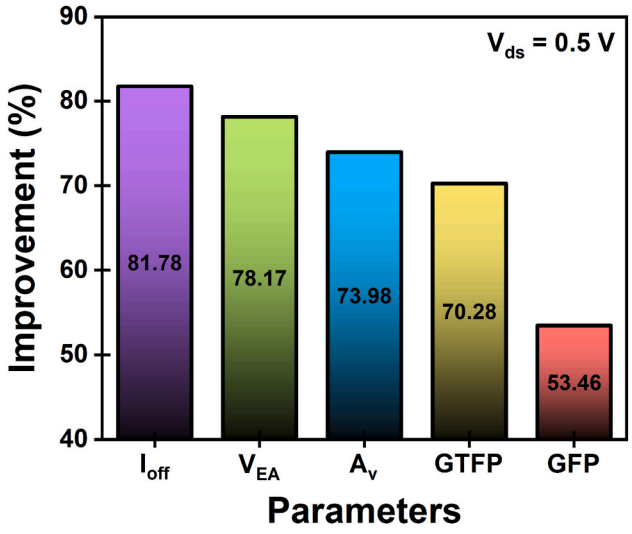

Fig. 12. Representation of the improvement in I_{off}, V_{EA}, A_v, GTFP, and GFP parameters following the transition from the C_4 to the C_5 configuration.

Table 3
Overview of the prominent static, analog, and RF ΔFoMs.

Parameters	$(FoMs)_{C5\ Conf.}$	$(FoMs)_{C1\ Conf.}$	(ΔFoMs)
Electric Field (MV/cm)	0.593	0.538	0.055
Potential (V)	0.866	0.860	0.006
Electron Velocity (Mcm/s)	743.40	683.12	60.28
g_m (μA)	30.25	24.39	5.86
TGF (V^{-1})	87.77	63.09	24.68
V_{EA} (V)	44.92	9.18	35.74
A_v	107.23	19.52	87.71
f_T (THz)	1.63	1.94	−0.31
f_{max} (GHz)	13.04	17.18	−4.14
GBP (THz)	0.55	0.50	0.05
GFP (THz)	155.03	34.28	120.75
TFP (THz/V)	16.99	16.04	0.95
GTFP (THz/V)	1104.36	191.84	912.52

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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Fin field-effect-transistor engineered sensor for detection of MDA-MB-231 breast cancer cells: A switching-ratio-based sensitivity analysis

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The present study describes the utilization of a gallium-arsenide gate-stack gate-all-around (GaAs-GS-GAA) fin field-effect transistor (FinFET) to accomplish the electrical identification of the breast cancer cell MDA-MB-231 by monitoring the device switching ratio. The proposed sensor uses four nanocavities carved beneath the gate electrodes for enhanced detection sensitivity. MDA-MB-231 (cancerous) and MCF-10A (healthy) breast cells have a distinct dielectric constant, and it changes when exposed to microwave frequencies spanning across 200 MHz and 13.6 GHz, which modifies the electrical characteristics, allowing for early diagnosis. First, a percentage shift in the primary DC characteristics is presented to demonstrate the advantage of GS-GAA FinFET over conventional FinFET. The sensor measures the switching-ratio-based sensitivity, which comes out to be 99.72% for MDA-MB-231 and 47.78% for MCF-10A. The sensor was tested for stability and reproducibility and found to be repeatable and sufficiently stable with settling times of 55.51, 60.80, and 71.58 ps for MDA-MB-231 cells, MCF-10A cells, and air, respectively. It can distinguish between viable and nonviable cells based on electrical response alterations. The possibility of early detection of cancerous breast cells using Bruggeman's model is also discussed. Further, the impact of biomolecule occupancy and frequency variations on the device sensitivity is carried out. This study also explains how to maximize the sensing performance by adjusting the fin height, fin width, work function, channel doping, temperature, and drain voltage. Lastly, this article compared the proposed breast cancer cell detectors to existing literature to evaluate their performance and found considerable improvement. The findings of this research have the potential to establish GaAs-GS-GAA FinFET as a promising contender for MDA-MB-231 breast cancer cell detection.

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I. INTRODUCTION

Cancer is not an infectious illness; instead, it is caused by a malfunction in the DNA of a cell or tissue [1]. These cells do not perform their usual functions but rather proliferate and replicate in an uncontrolled manner, resulting in the formation of a tumor. In 2020, according to WHO fact sheets, cancer was the leading cause of mortality worldwide, accounting for around 10 million deaths, or almost one in every six, with breast cancer (2.26 million cases) as the most prevalent cancer, followed by lung cancer (2.21 million cases), colon and rectum cancer (1.93 million cases), and so on [2]. The formation of malignant tumors in women's breasts is the primary cause of breast cancer, and the lifetime chance of developing it is 12%. The most common cancerous breast cells are MDA-MB-231, MCF-7, T47D, and Hs578t, while MCF-10A is a healthy nontumorigenic breast cell [1]. Compared to MCF-7 and T47D, Hs578t and MDA-MB-231 cells are regarded as the most invasive. Since invasive breast cancer cells are so dangerous and may spread rapidly, diagnosis at an early stage is very important. Early diagnosis may aid in more effective disease management, and more than 70% of cases are expected to be cured with early detection [3,4].

Cell isolation separates one or more particular cell populations from a heterogeneous mixture of cells. Targeted cells are identified, isolated, and then segregated by kind. Many cell isolation techniques are available depending on the kind of cells being separated, with a few significant ones covered in this paper, each having pros and cons. The computer-controlled micropipette (CCMP) method uses a small glass or quartz micropipette with a fine tip that a computer can control to precisely separate cells. CCMP involves manipulating a micropipette towards a suspended cell and applying a tiny suction pressure to partly aspirate the cell within the micropipette. As suction pressure rises, the cell deforms and flows into the micropipette. Researchers have widely employed this approach to explore the adhesion force measurements [5] and mechanical characteristics of diverse cells [6,7]. Fluorescence-activated cell sorting (FACS) is a flow cytometry method that uses fluorescence characteristics to separate cells. FACS begins with labeling cells with fluorescent dyes that attach to specific cell surface markers. In front of a laser, the suspended cells are passed in a stream of droplets, each containing a single cell. This stream is then directed via a series of lasers, which activate the cell-bound fluorophores, resulting in light scattering and fluorescent emissions. The fluorescence detecting system recognizes cells of interest based on the wavelengths generated by the laser excitation. Due to its wide application, FACS research includes bacteria [8], protoplasts [9], bone marrow

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cells [10], etc. Microfluidics is a cell separation technique that uses fluid manipulation on a microscopic scale. Cell isolation approaches based on microfluidics vary depending on their size, density, compressibility, electrical and magnetic characteristics, etc. The membrane filtering technique uses thin membrane layers with micropores to detect and isolate cells based on their size [11]. Cells of different densities and compressibilities may be separated using acoustic waves in a process called acoustophoresis [12]. In dielectrophoresis, nonuniform electric fields separate and isolate cells based on their dielectric properties [13]. Cells that contain magnetic nanoparticles may be identified and separated via magnetic cell sorting [14]. Laser microdissection is a high-resolution technique for isolating cells from their surrounding tissues that employs a laser beam and direct microscopic visualization. The sample is mounted on a microscope slide, and an infrared or ultraviolet laser selectively cuts off the cells of interest. After that, the sliced cells are collected for further examination. This technique has been extensively used in the research of liver illnesses [15], mass spectrometry [16], etc.

X-ray mammography, sonography, and magnetic resonance imaging (MRI) scans are some screening methods for breast cancer identification. Currently, x-ray mammography is the predominant method for breast cancer detection. Although this technology has made significant strides in this sector, there have been reports of many drawbacks [17,18]. In addition, x-ray mammography's specificity and sensitivity drastically decrease to 89% and 67% for dense breasts, and the method also includes radiation exposure dangers [19]. While sonography may be a cost-effective tool in the fight against breast cancer, the accuracy of a diagnosis relies on the experience of the person doing the procedure, and hence it may provide erroneous findings at times [20]. MRIs with improved contrast have a higher sensitivity (93–100%) [21], but they are difficult to use, costly, and limited to hospital use.

The microwave imaging technique was created to overcome the drawbacks of conventional imaging. This method uses the large dielectric difference between healthy and cancerous tissue to perform microwave imaging and heating [22–24]. Scientists have been interested in how different types of malignant cells behave and may be detected when exposed to microwave frequencies [25,26]. Kim *et al.* calculated the dielectric characteristics of fatty glandular, fibro, and malignant breast tissues from 50 MHz to 5 GHz frequency [27]. It was noted that the dispersion of malignant tissues differs from that of healthy breast tissue. In the frequency range of 50–900 MHz, Joines *et al.* investigated the dielectric characteristics of human tissues and found that cancerous tissues have greater conductivity and permittivity than normal tissues [28]. Many investigations have been conducted to know the dielectric characteristics of various human body components, such as the liver [29]. Dielectric characteristics of numerous *in vitro* breast malignant cell lines have been examined between 200 MHz and 13.6 GHz by Hussein *et al.* [1]. It was found that breast cancer cells, because of their high water content, exhibit varying dielectric characteristics, leading to enhanced scattering at microwave frequencies.

Compared to imaging methods, molecular biotechnology tests may detect breast cancer sooner. However, they cannot substitute imaging techniques but complement imaging methods for diagnosing breast cancer. Molecular biotechnology examines biomarkers like nucleic acid, proteins, cells, and tissues of patients. Effective molecular biotechnology examination tools utilized for identifying breast cancer cells include quantitative polymerase chain reaction (qPCR), mass spectrometry (MS), single-cell resonant waveguide gratings (SCRWGs), digital holographic microscopy (DHM), etc. The qPCR, or real-time PCR, quantifies DNA and gene expression levels in samples. qPCR has been used to assess circulating tumor cells in many solid tumors, such as breast cancer [30]. The qPCR technology may guide breast cancer therapy by monitoring mRNA expression [31]. Matrix-assisted laser desorption/ionization (MALDI) mass spectrometry imaging (MSI) [32], surface-enhanced laser desorption/ionization (SELDI) MS [33], and liquid chromatography-tandem mass spectrometry (LC-MS/MS) [34] are some of the MS-based techniques utilized for breast cancer diagnosis. The concentration of adhesion proteins inside the cell-substrate contact zone causes a change in the refractive index, which may be monitored in real-time using SCRWGs. The SCRWGs technology was used to monitor the adhesion of HeLa cancer cells [35]. DHM technology provides high-resolution three-dimensional (3D) imaging of transparent biological specimens such as live cells and tissues. DHM may be utilized to capture digital holograms of breast tissues and analyze their malignancy using a deep learning approach [36]. Each technique has pros and cons, depending on the nature of the investigated molecules.

Microelectromechanical systems (MEMS) based sensors [37,38], fiber Bragg grating (FBG) [39,40], and optical sensors [41] have also played significant roles in identifying breast cancer cells. However, field-effect-transistor (FET) based devices have recently attracted attention in biosensing applications for their many benefits, including small size, low cost, high sensitivity, suitability for CMOS (complementary metal-oxide-semiconductor) technology, controllable electrical response, and reproducibility [42,43]. Tunnel field-effect transistors (TFETs) [44], high-electron-mobility transistors (HEMTs) [45], and fin field-effect transistors (FinFETs) [46] have been used in the past in breast cancer diagnosis. FinFET demonstrates superior performance compared to planar devices and optimizes the short-channel effects (SCEs) by allowing for high scalability, decreased power utilization, and longer battery life [47,48]. The gate-all-around (GAA) design provides enhanced electrostatic control over the channel, higher packing density, a steep subthreshold slope, and high current driving capability [49,50]. During MOS technology downscaling, the gate-stack (GS) design inhibits the increase in off-state leakage current (I_{off}) [51]. Furthermore, the GS design eliminates the mobility degradation and threshold voltage instability that occur with direct deposition of high-k dielectrics on silicon substrates [52,53]. Figure 1 shows a quick comparison of the conventional FinFET and GS-GAA FinFET devices concerning the percentage change in the fundamental DC performance characteristics. It is worth noting that, at a supply voltage of 0.5 V, the GS-GAA FinFET device provides an 86.26% lower off-current (I_{off}), which leads to an improvement of 693.48% in the switching ratio (SR).

Gallium arsenide (GaAs) is considered in the fin area because it has several superior electrical properties to silicon, including high electron mobility and a large energy band gap

Parameters	Conv. FinFET V_{ds} = 0.05V	GS-GAA FinFET V_{ds} = 0.05V	Conv. FinFET V_{ds} = 0.5V	GS-GAA FinFET V_{ds} = 0.5V
I_{on} (μA)	2.19	2.32	21.00	22.83
I_{off} (pA)	10.37	1.94	22.78	3.13
SR ($\times 10^6$)	0.21	1.19	0.92	7.30
SS (mV/dec)	67.52	61.49	67.05	61.86
V_{th} (V)	0.27	0.29	0.25	0.27

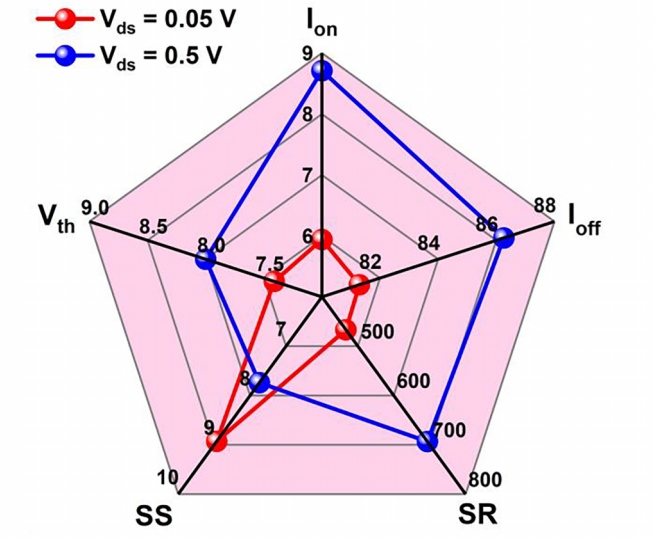

FIG. 1. Conventional FinFET vs GS-GAA FinFET concerning the percentage change in DC performance characteristics.

[54]. The absence of GaAs-based thermodynamically stable, high-quality insulators to augment device standards like SiO_2 on silicon is the primary difficulty with GaAs-based devices. Nonetheless, molecular beam epitaxy (MBE) and atomic layer deposition (ALD) have successfully built high-quality dielectrics atop III-V semiconductors [55–57]. Aluminum oxide (Al_2O_3) is favored as a gate dielectric because of its capacity to stay noncrystalline throughout manufacturing processing, excellent GaAs interface quality, huge 9 eV energy band gap, and high thermal stability [58]. Consequently, we proposed the GaAs-GS-GAA FinFET.

The proposed device employs a GAA design that encloses the gate on all four sides; consequently, four nanocavities are carved beneath the gate electrodes toward the source area for enhanced detection sensitivity. The presence or absence of breast cancer cells affects the dielectric constant of the cavity area. The change in the dielectric constant alters the device's electrical properties, which may then be utilized to identify the presence of sickness in the body. Thus, we used a GaAs-GS-GAA FinFET device in this study to identify breast cancer cells based on their dielectric constant value. MCF-10A and MDA-MB-231 breast cells were chosen for examination and may be produced by the procedure described by Hussein *et al.* [1]. Simulations were run to test the device sensitivity regarding switching ratio by analyzing the drain current characteristics for air (cell free), MCF-10A, and MDA-MB-231 cells. The efficiency of any given sensor is directly proportional to the degree to which it can recognize with a high level of accuracy or precision. Therefore, we utilized Eq. (1)

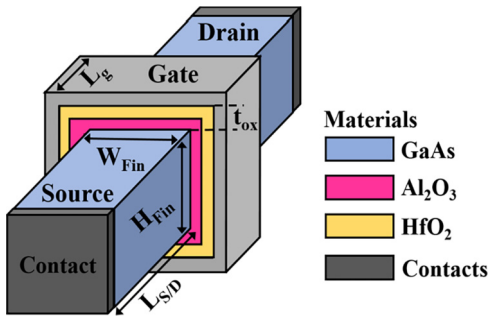

FIG. 2. Symmetric 3D view of the GaAs-GS-GAA FinFET.

to calculate the switching-ratio-based sensitivity (S_{SR}):

$$S_{SR}(\%) = \left| \frac{SR_{(air)} - SR_{(healthy/cancerous\ cell)}}{SR_{(air)}} \right| \times 100. \quad (1)$$

Further, the healthy and malignant breast cells were taken together in various concentrations, and an investigation was carried out to identify an MDA-MB-231 infection, even in small amounts. When breast cancerous and healthy cells are combined in different concentrations, the effective dielectric constant (ε_{eff}) is determined using the formulas from Bruggeman's model [59,60]:

$$\varepsilon_{eff} = \frac{H_b + \sqrt{H_b^2 + 8\varepsilon_c\varepsilon_h}}{4},$$
$$\text{with } H_b = (2 - 3C_m)\varepsilon_c - (1 - 3C_m)\varepsilon_h. \quad (2)$$

ε_c and ε_h are the dielectric constants of cancerous and healthy cells, and C_m represents the healthy cell fractional volume. Next, the effect of biomolecule occupancy on the device's sensitivity is explored. In biomolecule detection, the cavity area is assumed to have been completely filled. However, during biomolecule immobilization, the target biomolecule only fills a portion of the cavity areas, leaving some empty space, which can change the proposed device's electrical performance for different target biomolecules. Thus, there is a need to consider the biomolecule occupancy factor (γ_{Bio}) as it can potentially affect the sensitivity of the sensor. γ_{Bio} is defined as follows

TABLE I. Values of different parameters used for simulation.

Parameters	Symbol	Value	Unit
Source/drain length	$L_{S/D}$	50	nm
Gate length	L_g	50	nm
Cavity length	C_L	25	nm
Cavity height	C_H	3	nm
Oxide thickness	t_{ox}	3	nm
Fin height	H_{Fin}	30	nm
Fin width	W_{Fin}	15	nm
Gate thickness	G_t	5	nm
Channel doping	N_{Ch}	1×10^{16}	cm^{-3}
Source/drain doping	$N_{S/D}$	5×10^{18}	cm^{-3}
Work function	ϕ_m	4.65	eV
Temperature	T	300	K
Gate-source voltage	V_{gs}	1.5	V
Drain-source voltage	V_{ds}	0.5	V

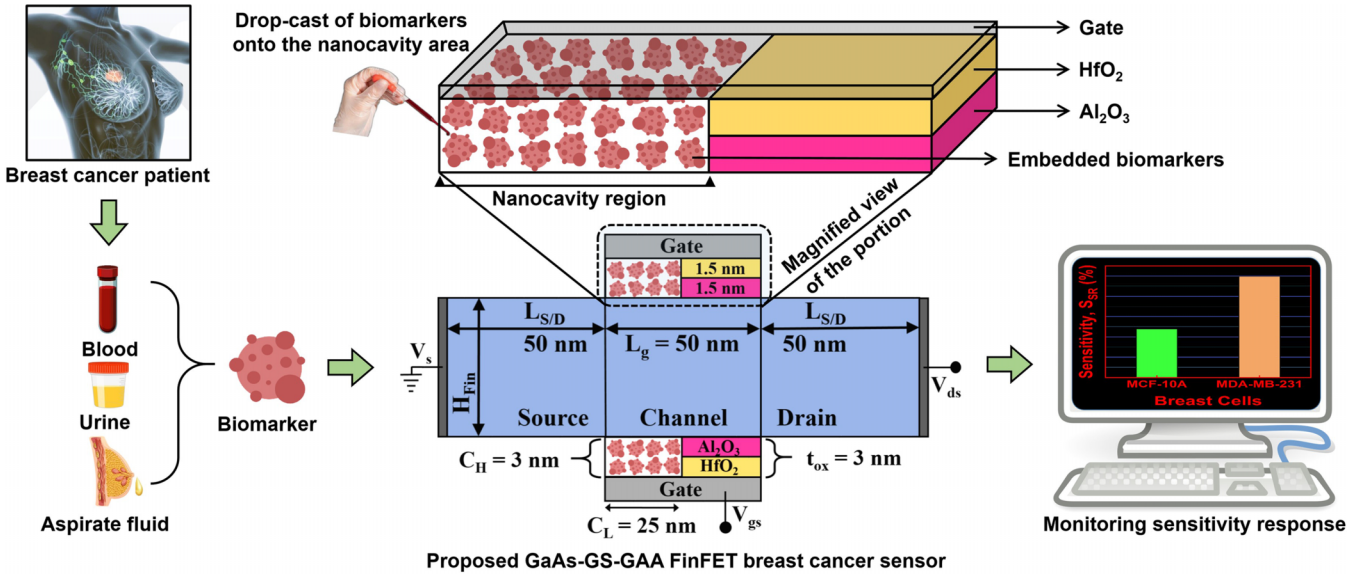

FIG. 3. Diagrammatic representation of the operation of a GaAs-GS-GAA FinFET sensor for breast cancer cell recognition.

[44]:

$$\gamma_{\text{Bio}}(\%) = \frac{\text{Thickness of cavity filled}}{\text{Total thickness of the cavity}} \times 100. \quad (3)$$

The proposed study also investigates how changes to the frequency and device's physical parameters, like fin height, fin width, work function, channel doping, temperature, and drain voltage, influence the device's sensitivity. Based on the findings, optimal device settings for maximizing sensitivity may be selected. Finally, the effectiveness of the proposed breast cancer cell detector is compared to that of already existing breast cancer detectors.

II. DEVICE ARCHITECTURE AND SIMULATION APPROACH

Figure 2 illustrates the symmetric 3D view of the GaAs-GS-GAA FinFET. Table I contains detailed descriptions of the device's structural parameters. The fin area is made of GaAs material. The simulations adhere to the width quantization property by keeping fin width (W_{Fin}) at a constant proportional multiple of fin height (H_{Fin}) [61,62]. In FinFET devices, it is recommended that the W_{Fin} should be less than one-third of the gate length (L_g) and H_{Fin} should be in the $0.6L_g$ to $0.8L_g$ range to minimize the SCEs [63,64]. We considered that recommendation during the device dimension consideration. The gate oxide has a combination of coatings of Al_2O_3 and HfO_2. All sections are uniformly n-type doped with lower channel doping than the source/drain doping to lessen the parasitic capacitance. At 200 MHz frequency, the dielectric constants (k) for MCF-10A and MDA-MB-231 are 4.33 and 24.50, while at 13.6 GHz, they drop to 2.76 and 16.65, respectively [1]. For air, which does not have any cells, k is 1. Figure 3 presents a diagrammatic representation of the operation of a GaAs-GS-GAA FinFET sensor for breast cancer cell recognition. The biomarker was drop-cast onto the nanocavity area carved beneath the gate electrodes to analyze the desired parameters using a technique based on dielectric modulation.

The GaAs-GS-GAA FinFET structure was simulated using the SILVACO-Atlas 3D simulator [65]. The Poisson and continuity equations are frequently used in the device simulation, but additional equations and models are also needed to improve device simulation results. As a result, the simulations include a wide variety of physical models. Quantum confinement effects are an essential design consideration for rapidly scalable devices. To consider the consequences of quantum confinement, the Bohm quantum potential (BQP) model uses a position-dependent quantum potential (Q) with parameters $\gamma = 1.4$ and $\alpha = 0.3$ [66]. Fermi-Dirac statistics, Crowell-Sze impact ionization, concentration-dependent mobility, Klaassen tunneling, Shockley-Read-Hall (SRH) recombination, and band gap narrowing are the other

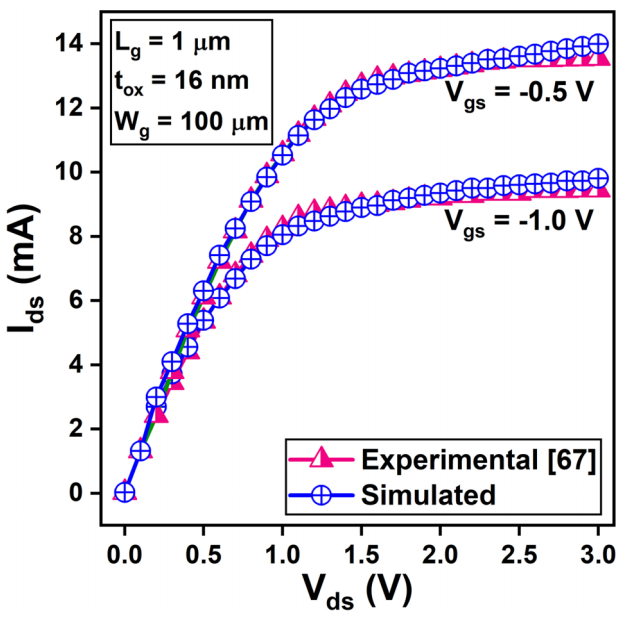

FIG. 4. Calibration curve of an Al_2O_3/GaAs MOSFET.

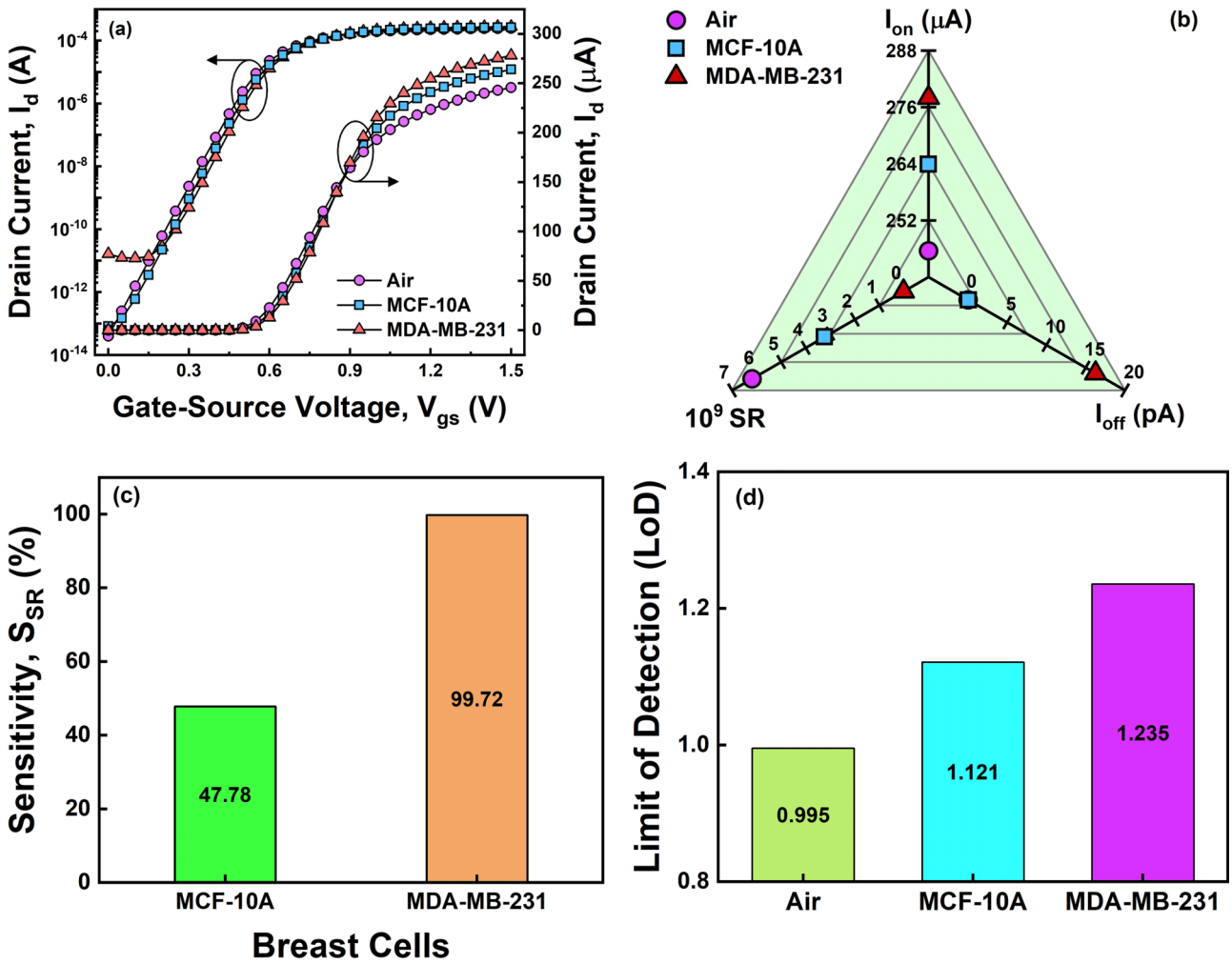

FIG. 5. (a) Transfer characteristics of the proposed sensor for air, MCF-10A, and MDA-MB-231 in linear and logarithmic form. (b) Fluctuation in I_{on}, I_{off}, and SR for air, MCF-10A, and MDA-MB-231. (c) S_{SR} comparison of MDA-MB-231 and MCF-10A cells. (d) LoD plot for air, MCF-10A, and MDA-MB-231.

standard models that have been incorporated [65]. Additionally, drain current characteristics are simulated using Newton and Block iteration methods for breast cancer cell identification.

We used the findings published by Ye *et al.* [67] to verify the simulation models discussed before. The output characteristics of an Al_2O_3/GaAs MOSFET operated with $V_{gs} = -0.5$ V and $V_{gs} = -1.0$ V are revealed in Fig. 4, along with the experimental and simulated results. The fact that the data sets obtained via simulation and experiment are comparable adds credibility to the simulation models chosen. The steps in creating the proposed GaAs-GS-GAA FinFET device were thoroughly covered in our earlier article [68], including a flowchart illustrating the whole process. Moreover, the cavity region can be created by dry etching the gate dielectric toward the source area.

III. RESULTS AND DISCUSSION

A. Switching-ratio-based sensitivity analysis

Figure 5(a) depicts the transfer characteristics ($I_d - V_{gs}$) of the proposed sensor for the air, MCF-10A, and MDA-MB-231 in linear and logarithmic forms. The sensor is examined at $V_{ds} = 0.5$ V field bias conditions. The drain current increases with the gate-source voltage (V_{gs}) and attains maximum value for MDA-MB-231. In contrast, the opposite trend is observed in the leakage current and degrades significantly for the MDA-MB-231 cancer cell. Figure 5(b) provides a clearer picture of the fluctuation in on-current (I_{on}), off-current (I_{off}), and switching ratio ($SR = I_{on}/I_{off}$) (which is subsequently employed as a sensitivity parameter). It can be seen that I_{on} is higher for the MDA-MB-231 cancer cell than for air and healthy cells. It is because introducing the breast cancer cells in the cavity region leads to enhanced effective gate oxide, which in turn increases the coupling between the channel region and gate metal, and thereby on-current. The difference in I_{off} between air and MCF-10A is not very large, but for MDA-MB-231 it is noticeably greater, which brings the SR down to a rather remarkable level. Figure 5(c) compares MDA-MB-231 and MCF-10A cells in terms of their S_{SR}. The graph reveals that the S_{SR} for MDA-MB-231 is 99.72%, and it is 47.78% for MCF-10A. The presence of MDA-MB-231 cells causes a more pronounced shift in I_{off}, which ultimately enhances the device's sensitivity. Figure 5(d) demonstrates the

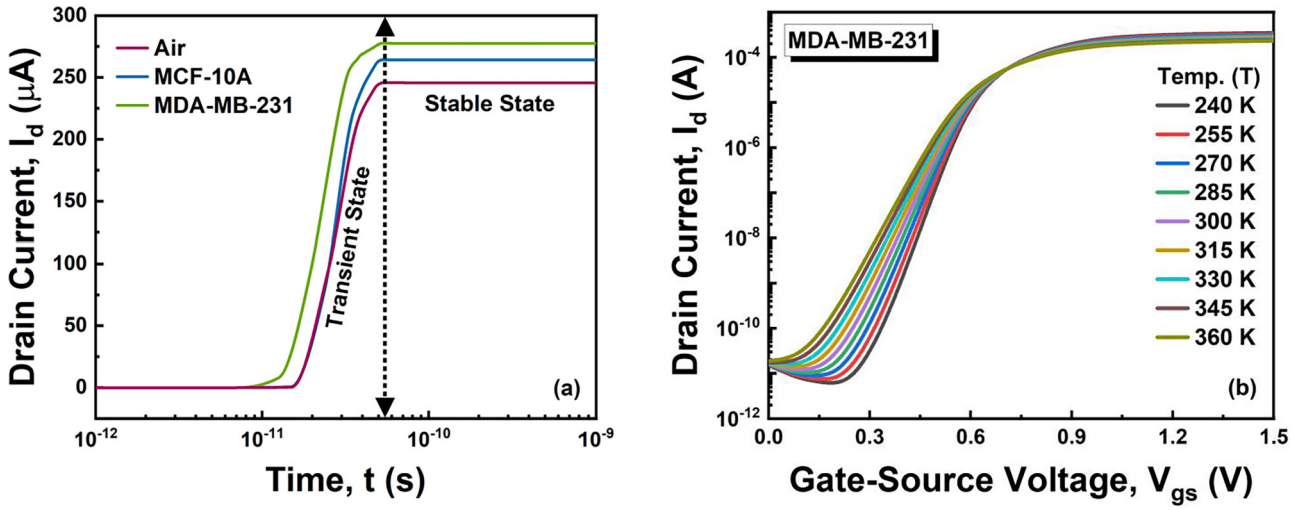

FIG. 6. (a) Transient response of the drain current for air and for MCF-10A and MDA-MB-231 cells. (b) Temperature dependence of the $I_d - V_{gs}$ characteristics of the MDA-MB-231 cancer cell.

limit of detection (LoD) plot for the three samples considered. The lowest concentration of an analyte that can be accurately identified from a sample with a high degree of certainty is known as the LoD [69]. LoD is calculated using the response of slope and standard deviation (SD) of the intercept. The slope and SD of the intercept for MDA-MB-231, MCF-10A, and air are analyzed using the transfer characteristics curve [Fig. 5(a)]. The slope is 0.0002 for all samples, and the SD values come out to be 0.0000749, 0.0000679, and 0.0000603 for MDA-MB-231, MCF-10A, and air. As a result, the LoD obtained for MDA-MB-231 is slightly higher than those for air and MCF-10A. The relevance of reducing execution variability between devices and enhancing sensitivity while designing and producing nano-FET biosensors is provided by these results.

B. Stability and reproducibility analysis

The transient analysis of air and of MCF-10A and MDA-MB-231 cell lines was carried out to test the stability of the proposed sensor. The time it takes for the drain current to settle from its transient state to its steady state is called the settling time (t_{sett}) [70,71]. The transient response is simulated by applying V_{gs} with an amplitude of 1.5 V, a ramp time of 5×10^{-11} s, a stop time of 1×10^{-9} s, and a step time of 1×10^{-12} s. Figure 6(a) shows the transient response of the drain current for air and for MCF-10A and MDA-MB-231 cells. It was observed that the drain current is higher for the MDA-MB-231 cell compared to MCF-10A and air, due to which t_{sett} for the MDA-MB-231 cell is somewhat lower (55.51 ps) than t_{sett} for the MCF-10A cell (60.80 ps) and air (71.58 ps). After t_{sett}, the current becomes steady at a magnitude equal to that at $V_{gs} = 1.5$ V [Fig. 5(a)]. The effect of temperature on the transfer characteristics is investigated to further probe the stability of our proposed sensor. Figure 6(b) displays the temperature dependence of the I_d-V_{gs} characteristics of the MDA-MB-231 cancer cell; it can be observed that the I_d-V_{gs} curves do not vary significantly between 240 and 360 K.

Second, to examine reproducibility, it is necessary to test the sensor's repeatability under controlled use settings. As shown in Fig. 7, we conducted the transient simulation of the proposed sensor for MDA-MB-231 cancerous cells over four cycles with a gap of 30 minutes between each cycle. The drain current is measured for four cycles, and the findings reveal that the drain current can be reliably reproduced with unnoticeable deviation. The above data suggest that the GaAs-GS-GAA FinFET is sufficiently stable and reproducible.

C. Cell viability

The term "oxidative stress" pertains to a state of imbalance between the generation of reactive oxygen species and the capacity of cells to counteract the consequent harm. Cells undergo either apoptotic or necrotic cell death when their antioxidant defense mechanisms are overwhelmed by high amounts of oxidative stress. Zou *et al.* employed a silicon-based attenuated total reflectance terahertz time-domain spectroscopy (ATR THz-TDS) system to monitor cell mortality caused by oxidative stress in MCF-10A breast

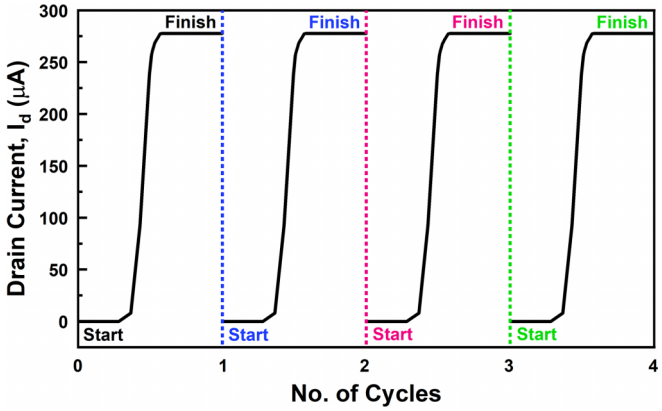

FIG. 7. Transient response of the proposed sensor for MDA-MB-231 cancerous cells over four cycles.

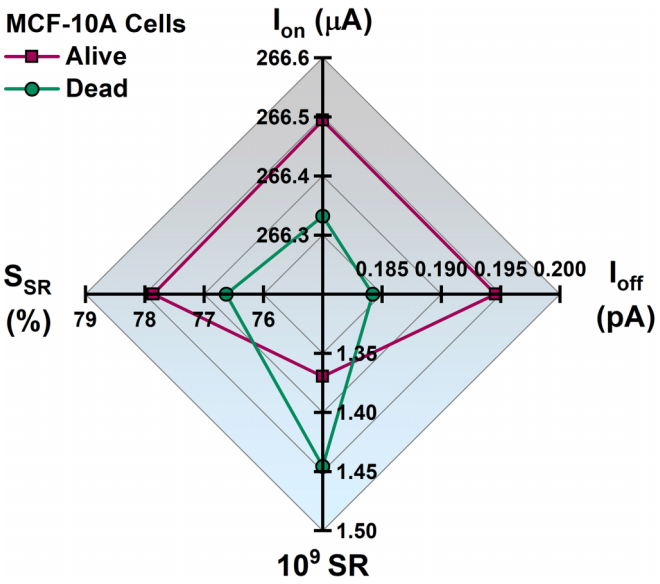

FIG. 8. Variation in I_{on}, I_{off}, SR, and S_{SR} of living and dead MCF-10A breast cells.

cells [72]. This study shows the THz dielectric responses of living and dead MCF-10A breast cells, in which cell death is induced by oxidative stress using a high concentration of hydrogen peroxide (10 mM, H_2O_2). Thus, with the assistance of this study, we have extracted the dielectric constants at 0.3 THz frequency for MCF-10A breast cells before and after the oxidative stress to monitor the electrical response of the proposed sensor on the live and dead cells. The sample under consideration (MCF-10A) may be produced by the procedure described by Zou *et al.* Unfortunately, to the author's best knowledge, no analysis has been performed to characterize the dielectric responses of dead MDA-MB-231 cancerous breast cells. As a result, the electrical response of the proposed sensor on the dead MDA-MB-231 cancerous breast cells could not be determined. The spider-chart depiction of the variation in I_{on}, I_{off}, SR, and S_{SR} of living and dead MCF-10A breast cells is shown in Fig. 8. The induction of cell death through oxidative stress reduces I_{on} from 266.49 to 266.33 μA and I_{off} from 0.195 to 0.184 pA. Since the reduction in I_{off} is bigger than the drop in I_{on}, SR is increased by 5.55%, and S_{SR} is lowered from 77.86% to 76.62%. Despite the relatively minor changes in the electrical response, the sensor under consideration may differentiate between viable and nonviable cells.

D. Early detection

Figures 9(a) and 9(b) demonstrate the transfer characteristics for five different combinations in linear and logarithmic form. In the graph, HC represents the healthy cell and CC is the cancerous cell. The presence of 90% HC and 10% CC indicates a very low quantity of cancerous breast cells, while the presence of 10% HC and 90% CC indicates a very high concentration of breast cancer cells. An enlarged view of the peaks generated by mixing various numbers of healthy and malignant cells is also shown in the insets of Figs. 9(a) and 9(b). It is visible that the drain current and the leakage current increase with the rise in the concentration of MDA-MB-231 cancerous cells. Figure 9(c) exhibits the spider-chart representation of the variance in I_{on}, I_{off}, and SR over the five different combinations. I_{on} increases from 265 to 277 μA, I_{off} increases by $\sim 10^2$ orders, and SR decreases by 98.48% when the concentration of cancerous cells is raised from 10% to 90%. Thus, the developed sensor can detect the presence of breast cancer cells, even at low concentrations, allowing for early illness diagnosis.

E. Effect of biomolecule occupancy on sensitivity

In order to examine the biomolecule occupancy of the device, five different sites were analyzed: 20%, 40%, 60%, 80%, and 100%. A section of the cavity is covered with biomolecules, while the remaining space is filled with air or left vacant to study the effect of biomolecule occupancy on sensor sensitivity. Figure 10(a) shows the I_{on}, I_{off}, and SR for a healthy MCF-10A cell, while Fig. 10(b) shows the same data for a malignant MDA-MB-231 cell for the five considered occupancy combinations of biomolecules. The increase in the γ_{Bio} leads to an increase in the effective dielectric and capacitance in the cavity area, ultimately increasing I_{on}. For MCF-10A, I_{on} is 256 μA at 20% biomolecule occupancy, which rises to 264 μA for 100% occupancy. Similarly, I_{on} is 267 μA at 20%, which rises to 278 μA at 100% occupancy for MDA-MB-231. I_{off} and SR show the same trend and improve with the increase in γ_{Bio} for MDA-MB-231 and MCF-10A cells. The sensitivity performance for healthy and malignant cells is plotted against different γ_{Bio} in Fig. 10(c). The sensitivity S_{SR} for MDA-MB-231 and MCF-10A decreases slightly with the increase in γ_{Bio}.

F. Effect of device parametric variation on sensitivity

Figures 11(a) to 11(f) collectively demonstrate the S_{SR} of the proposed sensor against the deviation of the mentioned parameters for the MDA-MB-231 cancerous cell. The fin height (H_{Fin}) varies from 30 to 40 nm with a step size of 2.5 nm. The S_{SR} of the proposed device increases with the surge in H_{Fin}, as shown in Fig. 11(a). Fin width (W_{Fin}) is altered from 5 to 15 nm with a step size of 2.5 nm. Figure 11(b) displays the sensitivity S_{SR} as a function of W_{Fin} and shows an improvement in S_{SR} with the rise in W_{Fin}, thus following the path of H_{Fin}. The work function (ϕ_m) is varied from 4.55 to 4.75 eV with an increase of 0.5 eV. The S_{SR} is 85.17% for 4.55 eV, which rises to 99.99% for 4.75 eV, as depicted in Fig. 11(c). Next is channel doping (N_{Ch}), which is considered from $1 \times 10^{16}\,cm^{-3}$ to $1 \times 10^{18}\,cm^{-3}$. Figure 11(d) exhibits the variation of S_{SR} with N_{Ch} and shows that the increase in the N_{Ch} results in sensitivity degradation. The temperature (T) range is from 200 to 400 K, with a measurement taken for every 50 K, as portrayed in Fig. 11(e). The reduction in the S_{SR} is marginal from 200 to 300 K, but afterward S_{SR} decreases significantly with the reduction in T. Lastly, in Fig. 11(f), the sensitivity is plotted against the drain voltage (V_{ds}), which varies from 0.1 to 0.5 V with a step size of 0.1 V. The S_{SR} is relatively lower at 0.1 V but increases after that with the increase in V_{ds}, with the highest value being recorded at $V_{ds} = 0.5$ V. Thus, to summarize, the increased levels of

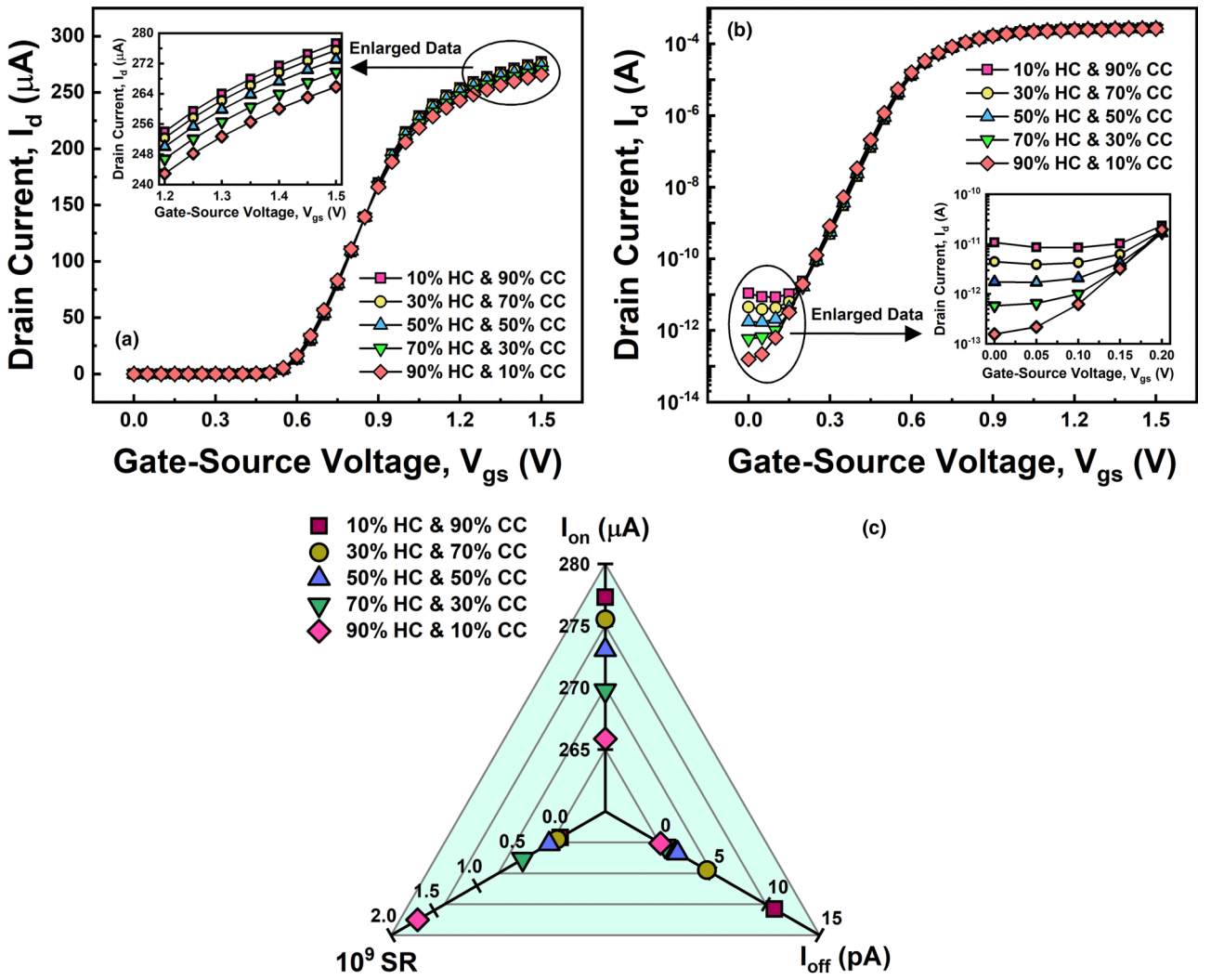

FIG. 9. Transfer characteristics for five different combinations in (a) linear and (b) logarithmic form. (c) Variation in I_{on}, I_{off}, and SR for the combinations considered.

H_{Fin}, W_{Fin}, ϕ_m, and V_{ds}, and the decreased levels of N_{Ch} and T, make it simpler to identify the breast cancer cells.

G. Effect of frequency on sensitivity

We evaluated four parameters, namely I_{on}, I_{off}, SR, and S_{SR} of MDA-MB-231 and MCF-10A breast cells at 13.6 GHz, to study the effect of frequency on these parameters. The comparative statistics for 200 MHz and 13.6 GHz in tabular form are shown in Fig. 12, along with a plot of the percentage change in each performance parameter mentioned above for MDA-MB-231 and MCF-10A breast cells. We evaluated the percentage change considering 200 MHz as the initial value and 13.6 GHz as the final value and plotted the actual percentage change to understand better the impact of the frequency on the respective parameter. When the frequency is raised from 200 MHz to 13.6 GHz, I_{on} decreases by 1.93% and S_{SR} by 2.85%, and I_{off} and SR improve by 3.70% and 2.48%, respectively, for MCF-10A. Similarly, for MDA-MB-231, I_{on} decreases by 0.86% and S_{SR} by 0.69%, and I_{off} and SR improve by 71.57% and 247.06%, respectively, with the rise in frequency. Thus, the proposed sensor detection sensitivity is significantly better at 200 MHz compared to 13.6 GHz for MDA-MB-231 and MCF-10A.

H. Comparison with published breast cancer detectors

An evaluation of the proposed breast cancer sensor against existing breast cancer detectors is required to determine its efficacy. Table II gives an overview of the proposed FinFET breast cancer sensor with other already published breast cancer sensors regarding the change in drain current (ΔI_{ds}) and drain current sensitivity (S_{Id}). The ΔI_{ds} data were unavailable for the reduced graphene oxide (rGO) encapsulated nanoparticle (NP) based FET biosensor, so we mentioned the device's sensitivity, which is about 3.9%. The highest reported ΔI_{ds} was 6 μA for the AlGaN/GaN HEMT structure, with ΔI_{ds} for the remaining devices being relatively low. The proposed GaAs-GS-GAA FinFET sensor exhibits improved results compared to the breast cancer detectors mentioned in Table II, with ΔI_{ds} of about 32.5 μA and S_{Id} of 13.21%.

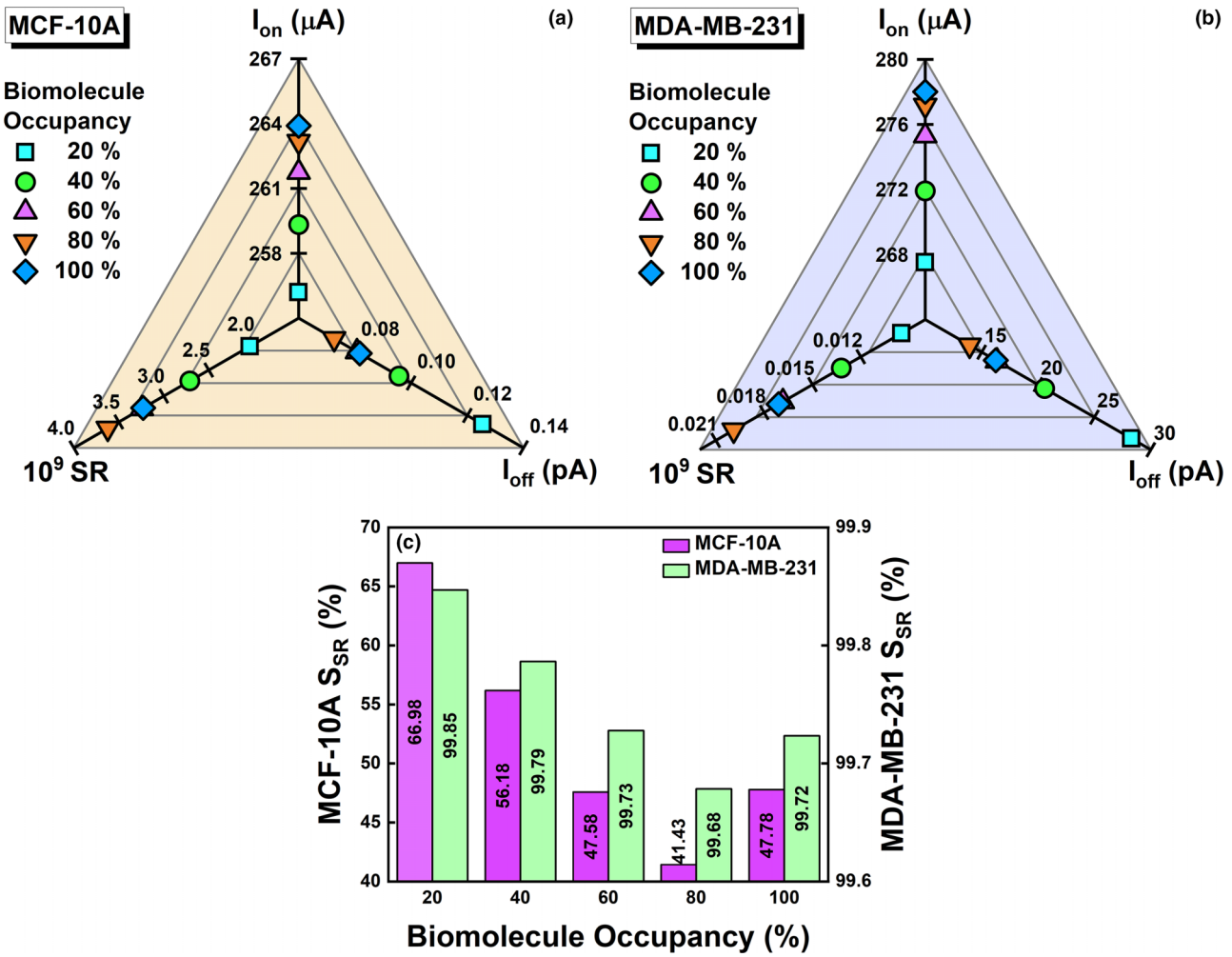

FIG. 10. Biomolecule occupancy impact on I_{on}, I_{off}, and SR for (a) MCF-10A and (b) MDA-MB-231. (c) Sensitivity performance for healthy and malignant cells against different γ_{Bio}.

IV. CONCLUSION

The current work details the usage of a GaAs-GS-GAA FinFET to monitor the device switching ratio to achieve the electrical identification of the MDA-MB-231 breast cancer cell. In order to increase the detection sensitivity, the suggested sensor makes use of four nanocavities that are carved underneath the gate electrodes. To emphasize the advantages of GS-GAA FinFET over traditional FinFET, a percentage change in the crucial electrical parameters is displayed for both types of FinFET. The switching-ratio-based sensitivity of the sensor is measured for healthy and malignant breast cells and turns out to be 47.78% and 99.72%, respectively. The sensor was evaluated for its reproducibility and stability

TABLE II. Overview of proposed FinFET-engineered cancer detector vs other published cancer detectors.

References	Year	Platform device	Detection	Change in drain current, ΔI_{ds} (μA)	Drain current sensitivity, S_{Id}(%)
[45]	2009	AlGaN/GaN HEMT	c-erbB-2, a breast cancer marker	6	–
[73]	2011	rGO encapsulated NP-based FET	HER2 and EGFR, a breast cancer marker	–	3.9
[74]	2020	Apta-cyto-sensor	MDA-MB-231 breast cancer cells	3	–
[75]	2021	CNT FET biosensor	Breast cancer exosomal miRNA21	1.65	–
[44]	2022	DL-NC-FE-TFET	T47D, Hs578T, MDA-MB-231, and MCF-7 breast cancer lines	1.83	–
This work		GaAs-GS-GAA FinFET	MDA-MB-231 breast cancer cells	32.5	13.21

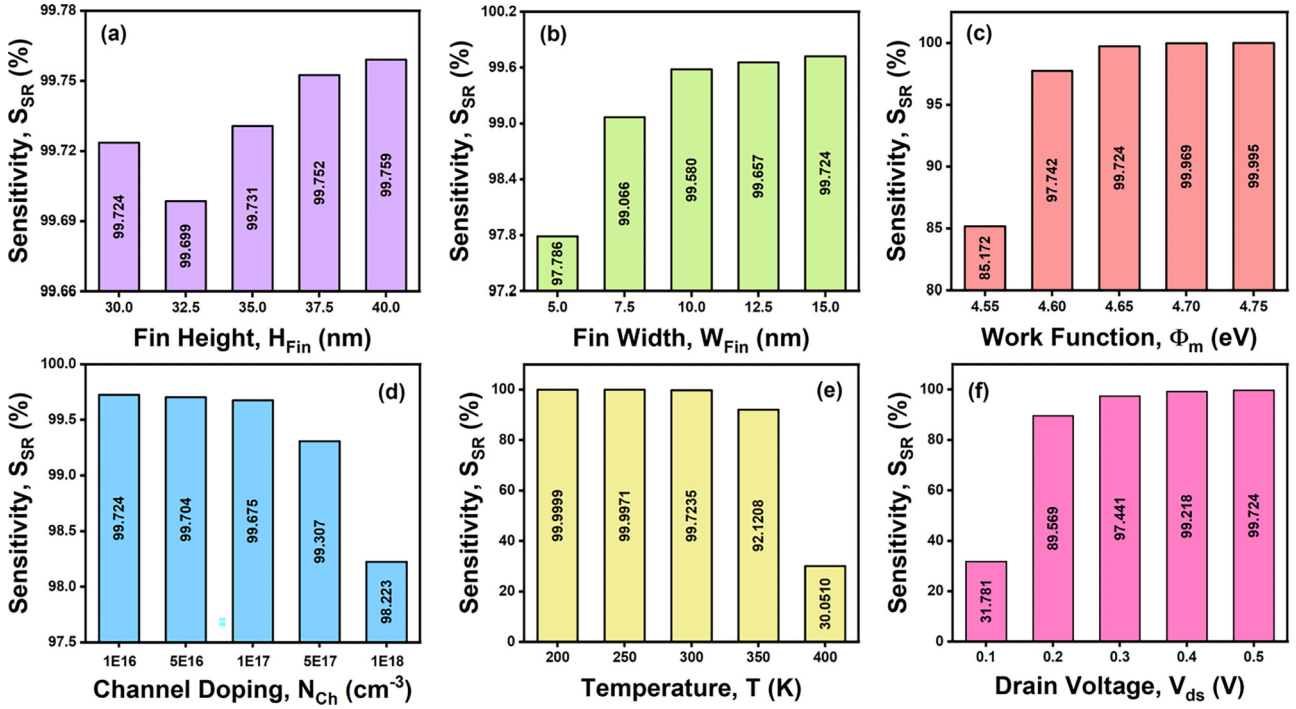

FIG. 11. S_{SR} of the proposed sensor against the deviation of mentioned parameters for the MDA-MB-231 cancerous cell.

and was found to be repeatable and adequately stable with settling times of 55.51 ps for the MDA-MB-231 cell, 60.80 ps for the MCF-10A cell, and 71.58 ps for air. Furthermore, the sensor is capable of distinguishing between viable and nonviable cells based on changes in their electrical response. The research also shows that breast cancer cells can be identified with the assistance of Bruggeman's model even when present in a mixed solution of malignant and healthy cells, even though the quantity of cancerous cells is lower. The effect of biomolecule occupancy and frequency fluctuations on the device's sensitivity is also investigated. This research also describes how to enhance the sensing performance by altering the fin height, fin width, work function, channel doping, temperature, and drain voltage. The proposed sensor can better identify malignant cells when the levels of H_{Fin}, W_{Fin}, ϕ_m, and V_{ds} increase and the N_{Ch} and T levels decrease. Finally, this work compared the suggested GaAs-GS-GAA FinFET sensor to previously published breast cancer sensors regarding the change in drain current and drain current sensitivity and found that the proposed sensor performed much better. Thus, the proposed GaAs-GS-GAA FinFET sensor may be considered an intriguing candidate for MDA-MB-231 breast cancer cell detection.

Parameters	MCF-10A		MDA-MB-231	
	200 MHz	13.6 GHz	200 MHz	13.6 GHz
I_{on} (μA)	263.90	258.80	278.00	275.60
I_{off} (pA)	0.081	0.078	16.25	4.62
SR ($\times 10^9$)	3.23	3.31	0.017	0.059
S_{SR} (%)	47.78	46.42	99.72	99.03

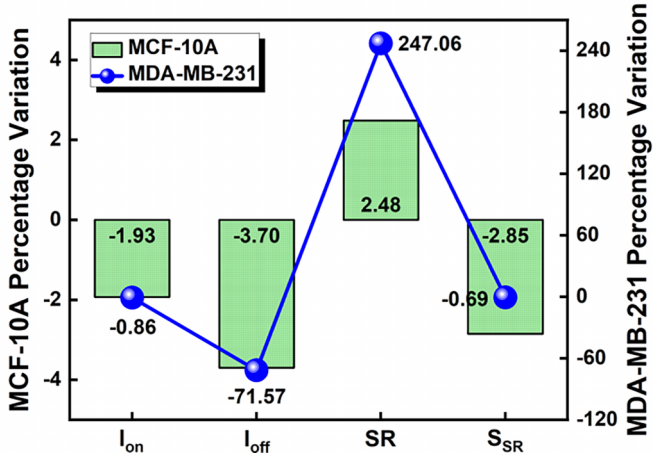

FIG. 12. Percentage change in each mentioned performance parameter for MDA-MB-231 and MCF-10A breast cells.

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B.K. conceptualized the work and was responsible for methodology, software, analysis, data curation, and original draft preparation. R.C. conceptualized the work and was responsible for analysis, data curation, review and editing of the paper at different stages, and supervision.

The authors declare that they have no known conflict of interest or personal relationships that could have appeared to influence the work reported in this paper.

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