TCAD Analysis and Simulation of T-Gate E-Mode GaN HEMT

THESIS SUBMITTED BY

MEGHA SHARMA

In Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Under the Supervision of

Prof. Rishu Chaujar

Department of Applied Physics
Delhi Technological UniversityDelhi, India.

July-2023

In the memory of my late father in law……

Delhi Technological University

(Govt. of National Capital Territory of Delhi)

Bawana Road, Delhi-110042

CERTIFICATE

This is to certify that the thesis titled "***TCAD Analysis and Simulation of T-Gate E-Mode GaN HEMT***" is being submittedby ***Ms. MEGHA SHARMA*** with registration number ***2K18/PHDAP/18*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Applied Physics. The work embodied in this thesis is a record of bonafide research work carried out by me in the Microelectronics Research Lab, Applied Physics Department, Delhi Technological University, New Delhi under the guidance of ***Prof. RISHU CHAUJAR***. It is further certified that this work is original and has not been submitted in part or fully to any other university or institute for the award of any degree or diploma.

Megha Sharma
Candidate
Roll No. 2K18/PHDAP/18

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

Prof. Rishu Chaujar
Supervisor (Professor)
Department of Applied Physics
Delhi Technological University
Delhi, India

Prof. A. S. Rao
Head
Department of Applied Physics
Delhi Technological University
Delhi, India

ACKNOWLEDGEMENTS

This five-year journey of my research work has been an incredible and transformative experience, filled with numerous lessons and personal growth. As I reflect upon this momentous milestone, I am overwhelmed with gratitude for the many individuals who have guided, supported, and believed in me throughout this tremendous journey. Without their unwavering assistance, completing this thesis would have been an immensely challenging task. Therefore, I would like to express my deepest appreciation and acknowledge their invaluable contributions.

First and foremost, I extend my heartfelt thanks to my mentor ***Prof. Rishu Chaujar****, whose expertise and guidance have been instrumental in shaping my research direction.* ***Prof. Chaujar*** *has not only been an exceptional mentor but also an extraordinary individual whom I consider to be the most remarkable person I have ever had the privilege to meet. During the course of my research, I have encountered numerous challenges and obstacles, both academic and personal. However, with* ***Prof. Chaujar*** *by my side, I have felt an immense sense of reassurance and encouragement. Her steadfast belief in my abilities has been a constant source of motivation, empowering me to persist in the face of difficulties.*

I am thankful to ***Prof. A. S. Rao****, Head of Department, Applied Physics DTU, and* ***Prof. R.K Saini****, Vice Chancellor, DTU for their munificent support and providing the abundant core for executing the research work efficiently. I further thank SRC and DRC members* ***Prof. S.C Sharma*** *(chairman DRC),* ***Prof. R.S. Gupta*** *(External Expert),* ***Prof. Annapurni*** *(External Expert) for taking their momentous time serving in my committee and giving their priceless endorsement on my thesis.*

The journey of pursuing a PhD is a challenging and demanding effort that often requires the support and encouragement of good friends. I consider myself incredibly fortunate to developed meaningful friendships during my PhD. I want to thank ***Bhavya Kumar*** *for his support and encouragement. Receiving rejections from academic journals is an inevitable part of the research process, and it can be disheartening and discouraging. However, Bhavya has always been there to uplift my spirits and motivates me. I am immensely grateful for the presence of* ***Ankita Banwal*** *in my life, as she has brought immeasurable joy and positivity into my PhD*

journey. Her ability to make me laugh and put me at ease during challenging times has been a true blessing.

I would like to express sincere gratitude towards my labmates, ***Yash Pathak, Rashi Mann, Anshul, Ayushi Lamba and Kajal Verma****. Their unconditional support and understanding, have made my time in the lab truly memorable and enjoyable. I would also like to thank* ***Vishal Singh*** *for being there to lighten the stressful atmosphere of the lab by cracking jokes and fun talks to make the moments memorable.*

*I would like to express my deepest gratitude to a very special person, my husband****, Mr. Nikhil Sharma****. His love, care, and unconditional support have been the driving force behind my successful completion of my Ph.D. degree. Thank you so much for being always around at times when it seemed impossible to continue, you helped me to keep things in perspective. I greatly value your contribution and deeply appreciate your belief in me. It is a blessing to have a life partner like you, who has given the liberty and charge of my life in my hands.*

I am profoundly grateful for the immense impact that my father, ***Mr. Bhim Chand Sharma****, has had on my life. Words fall short in capturing the depth of my gratitude towards him. He has consistently supported and motivated me in every step of my life, instilling in me the confidence to pursue my dreams fearlessly. I would also like to express my gratitude to my mother,* ***Mrs. Upma Sharma****. She is the pillar of love and understanding in my life. Throughout my PhD journey, she has been my confidante, the one person with whom I can freely share my worries, doubts, and problems. Her unwavering support and comforting presence have provided me with the strength to face challenges head-on. I extend my thanks to my mother-in-law,* ***Mrs. Anju Sharma****, whose love and care have been a constant source of comfort. Her presence in my life has been a blessing and I am grateful for her affectionate support. I would also like to express my appreciation to my siblings,* ***Dr. Dinesh Chand Sharma****,* ***Gunjan Sharma****,* ***Tanya Sharma****,* ***Utkarsh Sharma*** *and* ***Raveesh Sharma.*** *They have played a significant role in my life, providing both companionship and support. I would also like to thank my niece,* ***Sarahna Sharma****, her adorable nature and positive energy have brought immense joy and relaxation.*

I would like to extend my heartfelt gratitude to my roommate, ***Shanu Bhardwaj****, who has been an integral part of my journey throughout my Ph.D. studies. Her presence has brought immense joy, laughter, and a sense of comfort to our shared living space.*

Lastly, I want to dedicate my thesis to my late father-in-law, ***Mr. Satish Sharma****, whose presence in my life has left an indelible mark. In the short span of time, I formed a deep and meaningful connection with him. Even on my most difficult days, his extraordinary sense of humour could instantly make me feel better. All my troubles seemed to vanish when I was with him. It is impossible to express in mere words the depth of love and admiration I felt for him. He touched my life in ways that are beyond measure, and his impact will continue to resonate within me for the rest of my life.*

Megha Sharma

ABSTRACT

TCAD Analysis and Simulation of T-Gate E-Mode GaN HEMT.

GaN-HEMT semiconductor technology has already solidified its position as the dominant contender in the realm of high-power and RF applications. In this thesis, performance of GaN HEMT device has been studied and various techniques have been proposed to overcome the major roadblock of GaN HEMT such as spilling of 2DEG, leakage current, threshold voltage (V_{th}), and parasitic capacitances.

In this regard, firstly polarization induce doping in the buffer layer (buffer Engineering), heavily doped source/drain region, and recessed T-gate (Gate Metal Engineering) are integrated simultaneously on a GaN HEMT i.e. T-gate E mode polarization induced doped buffer HEMT has been proposed. The polarization-induced doping in the buffer layer bent the conduction band upwardly convex, which enhanced the 2DEG confinement, reduced the buffer leakage current, and significantly uplifted the breakdown voltage (33 V), which is 5 times higher than the conventional InAlN/AlN GaN buffer HEMT (8 V). The recessed gate engineering further enhances various performance parameters. It achieves an impressive on/off ratio of 10^9, reduces the subthreshold swing (SS) to 78 mV/dec, and minimizes the drain-induced barrier lowering (DIBL) to 100 mV/V. The proposed device exhibits a high current density of 2.8 A/mm, transconductance 1.55 S/mm, cutoff frequency f_T (583 GHz), and maximum oscillation frequency f_{max} (840 GHz). At room temperature, the carrier density and mobility measured are 2.8×10^{13} cm^{-2} and 1250 cm^2/Vs. The large Johnson figure of merit (f_T. V_{BR}) 19.23 THz and $(f_T . f_{max})^{1/2}$ 699 GHz shows the potential of the proposed device for high-power millimeter-wave applications.

Additionally, high-k gate oxide engineering has also been conducted, where a specific region of the recessed gate is substituted with a high-k dielectric material. This integration of the high-k dielectric brings about notable improvements in both interfacial and transport characteristics,

while concurrently reducing the gate leakage current. However, the insertion of gate oxide alone does not enable E-mode operation. As a result, the superior option for achieving E-mode operation is through the utilization of gate-recessed engineering technique.

After analyzing the performance of T-gate E mode polarization induced doped buffer HEMT, the in-depth investigation of the influence exerted by the T-gate shape on both the DC and RF performance of the device have been analyzed. The impact of T-shaped gate geometry on parasitic capacitance and RF Figure of Merits (FOMs) such as maximum oscillation frequency (f_{max}), gain-bandwidth product (GBP), cut-off frequency (f_T), maximum stable and available power gain (Gms and Gma), maximum transducer power gain (MSG) and stability factor (k) has also been investigated for different gate head length (H_{length}), gate stem height (S_{height}), and gate foot length (F_{length}). The simulated results confirm that the proper choice of H_{length} (280 nm), S_{height} (100 nm), and F_{length} (10 nm) significantly reduced the parasitic capacitance (C_{gs} = 350 fF/mm and C_{gd} = 140 fF/mm) and enhanced the f_{max} (840 GHz), GBP (636 GHz), f_T (583 GHz) and also improve the power gains. The simulated results of the proposed device provided the detailed knowledge about the impact of T-gate geometry on RF FOMs at such aggressively scaled dimensions.

The noise and scattering parameters are critical in determining the overall performance of a device. The noise parameters are important because they determine the amount of noise that is present in the signal as it passes through the device. On the contrary, the scattering parameters determine the magnitude of power dissipated during the transmission of the signal across the device. Thus to account the noise performance T-gate E mode polarization induced doped buffer HEMT, the in depth investigation of the small signal and noise behavior of proposed device has been studied. The results show that the polarization-induced doping in the buffer layer bent the conduction band upwardly convex, which enhanced the 2DEG confinement, reduced the buffer leakage current, and significantly enhance the transconductance (1.55 S/mm). The increment in transconductance leads to a reduction in the reflection coefficient (S11, S22) and an improvement in the transmission coefficient (S21) as compared to GaN buffer HEMT. Furthermore, noise parameters such as auto/cross-correlation factor, minimum noise figure, noise conductance, and optimal noise resistance and reactance were also evaluated for the proposed device. Simulated results reveal that the proposed device has a lower noise figure and noise conductance than the GaN buffer HEMT by 57% and 20%, respectively. This research demonstrates that the T-gate polarization doped buffer (PDB-HEMT) structure is an excellent choice for Low Noise Amplifiers (LNA) operating at higher frequencies.

Although using the back barrier engineering enhances the RF and noise performance of device. However, it also reduces the drain current density. Therefore, it is important to find a balance between RF performance and drain current density in device. In this regard, a double channel engineering is executed on T-gate HEMT by inserting the AlN layer below the InAlN/GaN interface developing a double channel HEMT. Simulation results showed that formation of double channel significantly enhance the drain current density of 2.5 A/mm. However, due to a lack of gate controllability over a lower channel, the high leakage current is observed in double channel HEMT. This issue has been addressed by using the InGaN as a back barrier, which improves the carrier confinement of 2DEG by raising the conduction band for the GaN buffer and considerably improves the gate controllability over a lower channel. The performance of the proposed device is compared with that of conventional double-channel HEMTs. The simulation results showed, the proposed double channel back barrier HEMT (DC-BB-HEMT) exhibited substantial improvements in analog performance. The intrinsic gain, which indicates a higher signal amplification capability, improved by 50%. Similarly, the transconductance gain frequency (TGF) increased by an impressive 477%, while the early voltage was enhanced by 23%. These numbers suggest that the InGaN back barrier significantly contributes to the device's analog performance. Moreover, RF performance of (DC-BB-HEMT) also compared with conventional DC-HEMTs. Simulation results showed that both the cut-off frequency and maximum oscillation frequency increased by around 11.7% and 10%, respectively. Moreover, the study also investigated the device's linearity performance with varying back barrier distances. It has been observed that the linearity performance of proposed device improved at a back barrier distance of 30 nm. This result implies that careful optimization of the back- barrier distance can further enhance the device's linearity performance.

LIST OF PUBLICATIONS

ARTICLES IN INTERNATIONAL REFEREED JOURNALS (7):

1. **SHARMA, M.,** and CHAUJAR, R. 2022. Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications," **Int. J. RF Microw. Comput. Aided Eng**.,32,23057 **(IF-1.98).**
2. **SHARMA, M.,** and CHAUJAR, R. 2021. Design and investigation of recessed-T-gate double channel HEMT with InGaN back barrier for enhanced performance. **Arabian Journal for Science and Engineering**, 1-8. **(IF-2.9).**
3. **SHARMA, M.,** and CHAUJAR, R. Device Optimization of T-shaped gate and polarized doped buffer engineered InAlN/GaN HEMT for improved RF/ microwave performance. **Arabian Journal for Science and Engineering (IF-2.9)**.
4. **SHARMA, M.,** KUMAR, B. and CHAUJAR, R. 2023. Polarization induced doping and high-k passivation engineering on T-gate MOS-HEMT for improved RF/microwave performance. **Materials Science and Engineering**,290,116298. **(IF-3.4).**
5. **SHARMA, M.,** KUMAR, B., and CHAUJAR, R. 2023. Small signal and noise analysis of T-gate HEMT with polarization doped buffer for LNAs. **Micro and Nanostructures**, 180, 207593. **(IF-3.22)**.
6. KUMAR, B., **SHARMA, M.,** and CHAUJAR, R. 2023. Gate electrode work function engineered JAM-GS-GAA FinFET for analog/RF applications: Performance estimation and optimization. **Microelectronics Journal, 135**, 105766. **(IF-2.2).**
7. KUMAR, B., **SHARMA, M.,** and CHAUJAR, R. 2023. Junctionless-accumulation-mode stacked gate GAA FinFET with dual-k spacer for reliable RFIC design. Microelectronics Journal, 139, 105910. **(IF-2.2).**

ARTICLES IN INTERNATIONAL CONFERENCES (9):

1. **SHARMA, M.,** and CHAUJAR, R. 2022. BGaN back barrier engineering on E-mode T-gate double heterostructure HEMT for high RF applications. In 2022 IEEE International RF and Microwave Conference (RFM) (pp. 1-4). IEEE.
2. **SHARMA, M.**, and CHAUJAR, R. 2020. Impact of graded back-barrier on linearity of recessed gate InAlN/GaN HEMT. In 2020 IEEE VLSI Device Circuit and System (VLSI DCS) (pp. 154-158). IEEE.

3. **SHARMA, M.,** and CHAUJAR, R. 2021. The Performance Analysis of 70nm T-gate InAlN/AlN MOS-HEMT using Graded Buffer. In 2021 Devices for Integrated Circuit (DevIC) (pp. 466-470). IEEE.

4. **SHARMA, M.,** KUMAR, B., and CHAUJAR, R. 2022. Linearity analysis of T-gate HEMT with graded back-barrier for wireless applications. In 2022 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT) (pp. 1-5). IEEE.

5. **SHARMA, M.**, KUMAR, B., and CHAUJAR, R. 2021. Effect of Gate Oxide Material Variability on The Analog Performance of T-Gate GaN-MOS-HEMT with Graded Buffer. In 2021 7th International Conference on Signal Processing and Communication (ICSC) (pp. 316-320). IEEE.

6. **SHARMA, M.,** KUMAR, B., and CHAUJAR, R. 2022. Simulation investigation of double-heterostructure T-gate HEMT with graded back-barrier engineering for improved RF performance. Materials Today: Proceedings, 71, 155-159.

7. KUMAR, B., **SHARMA, M.,** and CHAUJAR, R. 2022. Scattering Parameter Analysis of Gate Stack Gate All Around (GS-GAA) FinFET at THz for RF Applications. In 2022 8th International Conference on Signal Processing and Communication (ICSC) (pp. 653-658). IEEE.

8. KUMAR, B., **SHARMA, M.,** and CHAUJAR, R. 2022. Dual-k Spacer JAM-GS-GAA FinFET: A Device for Low Power Analog Applications. In 2022 IEEE Silchar Subsection Conference (SILCON) (pp. 1-5). IEEE.

9. KUMAR, B., **SHARMA, M.,** and CHAUJAR, R. 2021. Static Performance Assessment of Junctionless Accumulation Mode Gate Stack Gate All Around (JAM-GS-GAA) FinFET Under Severe Temperature. In 2021 7th International Conference on Signal Processing and Communication (ICSC) (pp. 386-390). IEEE

TABLE OF CONTENTS

Page No.

CERTIFICATE ..... *i*

ACKNOWLEDGEMENTS ..... *ii-iv*

ABSTRACT ..... *v-vii*

LIST OF PUBLICATIONS ..... *viii-ix*

CHAPTER -1 ..... **1**

INTRODUCTION **1**

1.1 BACKGROUND 2

1.2 THEORY OF GaN HEMT 4

1.2.1 BASIC STRUCTURE 4

1.2.2 PIEZOELECTRIC AND SPONTANEOUS POLARIZATION EFFECT 6

1.2.3 GaN-HEMT-OPERATION 9

1.2.4 DEVICE ENGINEERING TECHNIQUES 11

1.2.4.1 DOUBLE HETEROSTRUCTURE HEMT WITH GRADED BACK BARRIER 11

1.2.4.2 GATE FIELD PLATE HEMT 12

1.2.4.3 HIGH GATE MULTI-RECESSED BUFFER HEMT 13

1.2.4.4 DOUBLE CHANNEL MOS- HEMT 15

1.2.4.5 P-GATE GaN HEMT 16

1.2.4.6 FERROELECTRIC GATE GaN HEMT 16

1.3 ADVANTAGES OF GaN HEMT 17

1.4 CHALLENGES CONFRONTED BY THE GaN HEMT 18

1.5 RESEARCH OBJECTIVES 19

1.6 THESIS ORGANIZATION 20

1.7 REFERENCES 22

CHAPTER-2 ..... **28**

SIMULATION OF T-GATE E-MODE HEMT WITH POLARIZATION INDUCED DOPED BUFFER FOR ELECTRICAL AND RF PERFORMANCE 28

2.1 INTRODUCTION 29

2.2 DEVICE STRUCTURE 33

2.3 SIMULATION MODEL AND CALIBRATION 35

2.4 FABRICATION PROCESS FLOW 36

2.5 RESULTS AND DISCUSSION 37

2.5.1 BAND DIAGRAM 37

2.5.2 DC CHARACTERISTICS 39
2.5.3 MICROWAVE CHARACTERISTICS 41
2.5.4 IMPACT OF RECESSED GATE DEPTH 43
2.5.5 IMPACT OF GATE OXIDE 45
2.6 SUMMARY 48
2.7 REFERENCES 49

CHAPTER-3 54

DEVICE OPTIMIZATION OF T-SHAPED GATE AND POLARIZED DOPED BUFFER ENGINEERED INALN/GAN HEMT 54

3.1 INTRODUCTION 55
3.2 DEVICE STRUCTURE 57
3.3 RESULTS AND DISCUSSION 59
3.3.1 DC CHARACTERISTICS 59
3.3.2 EFFECT OF GATE FOOT LENGTH 60
3.3.3 EFFECT OF GATE STEM HEIGHT 65
3.3.4 EFFECT OF GATE HEAD LENGTH 68
3.4 SUMMARY 71
3.5 REFERENCES 72

CHAPTER-4 76

SMALL SIGNAL AND NOISE BEHAVIOR OF T-GATE E-MODE HEMT WITH POLARIZATION INDUCED DOPED BUFFER 76

4.1 INTRODUCTION 77
4.2 DEVICE STRUCTURE 80
4.3 RESULTS AND DISCUSSION 81
4.3.1 SMALL SIGNAL ANALYSIS 82
4.3.2 NOISE ANALYSIS 86
4.4 SUMMARY 92
4.5 REFERENCES 92

CHAPTER-5 96

DESIGN AND INVESTIGATION OF E-MODE-T-GATE DOUBLE CHANNEL HEMT WITH INGAN BACK BARRIER FOR ENHANCED PERFORMANCE 96

5.1 INTRODUCTION 97
5.2 DEVICE STRUCTURE 99
5.3 RESULTS AND DISCUSSION 100
5.3.1 BAND DIAGRAM AND ELECTRON CONCENTRATION 100
5.3.2 DC AND ANALOG PERFORMANCE 102
5.3.3 RF PERFORMANCE 105

5.3.4 LINEARITY ANALYSIS OF DC-BB-HEMT WITH VARIABLE T_{BB} 108
5.4 SUMMARY 111
5.5 REFERENCES 111

CHAPTER-6 114

SUMMARY AND FUTURE SCOPE..... 114

6.1 SUMMARY 115
6.2 FUTURE SCOPE 118

REPRINTS OF JOURNAL PUBLICATION

CHAPTER 1

INTRODUCTION

Firstly, this chapter provides a comprehensive background of the research work, with a primary focus on the significance of gallium nitride (GaN) in the power electronics industry. After then, the chapter moves on to the fundamental theory of GaN HEMT, covering topics like its polarization effect and its operating principle. In addition to this, the chapter investigates a number of device engineering techniques that have been reported to overcome the problems faced by HEMT. The chapter continues with a description of the challenges confronted by the GaN HEMT that are found while literature survey. After that, a description of the main objective of this thesis is provided, which is then followed by an overview of all the chapters.

1.1. Background

The advancement of semiconductor technology paved the way for the creation of an enormous industry and many applications that profoundly altered our way of life. Silicon technology, which has been the main workhorse of modern electronics, has dominated the semiconductor sector over a decade. Transistors made from silicon have been implemented in many different fields. However, silicon-based devices are quickly reaching their theoretical limit of operation, and future RF and microwave applications will require even higher levels of performance that cannot be achieved with the current technology. As a result, researchers are exploring alternative materials and device architectures to overcome these limitations and enable the next generation of RF and microwave devices. Group III-V semiconductors such as SiC, GaAs, and GaN have all been investigated as possible silicon substitutes. GaAs's high electron mobility in the bulk makes it a promising candidate for use in MESFETs operating at high frequencies. Nevertheless, its inadequate thermal conductivity renders the material unsuitable for high-power applications. Because of this, GaAs MESFETs can only be used in low-power devices like mobile phones and other portable electronics (*Kameche and Rozdovski, 2005*). SiC, on the other hand, is highly suitable for both high-temperature and high-voltage applications due to its distinctive material properties. Due to their excellent resistance to heat and voltage, SiC MESFETs find widespread use in demanding industries like aerospace and defence. However, SiC devices are unsuitable for high-frequency activities because of their limited electron mobility and inability to create a heterojunction.

Gallium Nitride High Electron Mobility Transistor (GaN-HEMT) semiconductor technology has solidified its position as the dominant contender in the realm of high-power and RF applications. Optoelectronics *(Cai et al., 2018)*, MEMS *(Rais et al., 2017)*, and electronics *(Karmalkar and Mishra, 2001)* are just a few of the fields that have benefited from the unique features of GaN-based materials. Aluminium gallium nitride (AlGaN)/GaN devices have become highly regarded as top contenders among solid-state microwave power devices for various applications. In comparison to devices based on Si and GaAs, they are better because of their capacity to produce enhanced power densities at higher frequencies. GaN contains a number of beneficial properties, which together lead to the material's outstanding performance. A wide bandgap (3.4 eV), substantial electric breakdown field strengths (3×10^6 V/cm), and a

TABLE 1.1

Characteristics of GaN and rival semiconductor materials. (*Trew, 2002, Kemerley et al., 2002*)

Material	4*H*-SiC	GaAs	InP	**GaN**	Si
E_g(eV)	3.26	1.4	1.34	**3.4**	1.1
κ(W·cm^{-1}·K^{-1})	4.5	0.5	0.68	**1.3**	1.5
n_i (/cm^3)	8.2×10^{-9}	2.1×10^6	1.3×10^7	**1.9×10^{-10}**	1.5×10^{10}
v_{sat}(10^7 cm/s)	2.0	2.0	0.9	**2.5**	1.0
μ_n(cm^2·V^{-1}·s^{-1})	720	8500	5400	**900**	1350
ε_r	10	12.8	10	**9.0**	11.8
E_c(MV/cm)	2.0	0.4	0.5	**3.3**	0.3

high saturation electron drift velocity (>2×10^7 cm/s) are some of these characteristics. The HEMTs made from AlGaN/GaN are particularly appealing because of their superior performance at high power *(Wu et al., 2001)*, high-frequency (*Kumar et al., 2002, Chung et al., 2010)*, and high temperature *(Gaska et al., 1997)*.

Table 1.1 shows how GaN stacks up against other prominent semiconductors in terms of its key intrinsic electronic properties (*Trew, 2002, Kemerley et al., 2002)*. Compared to Si, GaAs, and InP, it's clear that GaN offers numerous benefits. Due to its larger band gap (E_g), larger critical electrical field (E_c) than Si, GaAs, and InP by as much as a factor of ten. As a result of its high electronegativity, GaN HEMTs have a substantially greater breakdown voltage than other semiconductor devices, making them ideal for high-voltage and high-power applications. GaN transistor-based circuits exhibit remarkable reliability, attributed to their high breakdown voltage. These devices can function at very high frequencies with high drain current thanks to their exceptional electron mobility, saturation drift velocity and high two-dimensional electron gas (2DEG) concentration, which are crucial for high-power RF applications. GaN is a broad band-gap semiconductor with a significantly lower intrinsic carrier generation rate than Si, GaAs, or InP. This allows GaN-based transistors to function at high voltage while maintaining

a low leakage current. As an added bonus, GaN-based devices can operate in high-temperature and high-pressure conditions because of their high thermal conductivity. GaN is the dominating technology for high-power applications at high frequency due to its great mobility and strong critical field, which permits aggressive scaling of the transistor size.

Due to their potential for high frequency and high-power electronic devices, the AlN/GaN (*Smorchkova et al., 2001*), AlInN/GaN (*Kuzmik, 2001*), and AlInN/GaN/GaN (*Lim et al., 2010*, *Wang et al., 2013*) material systems are the topic of active study. Device performance may be enhanced by using these material solutions, which provide both increased carrier densities and aggressive downscaling of gate lengths. AlGaN/GaN HEMTs have already found niche applications and are anticipated to play an increasingly important role in future electronic systems.

1.2. Theory of GaN HEMT

1.2.1 Basic Structure

HEMT is a type of semiconductor device used in high-frequency electronic circuits. It consists of two layers of semiconductor materials with different bandgaps, in which the wide bandgap

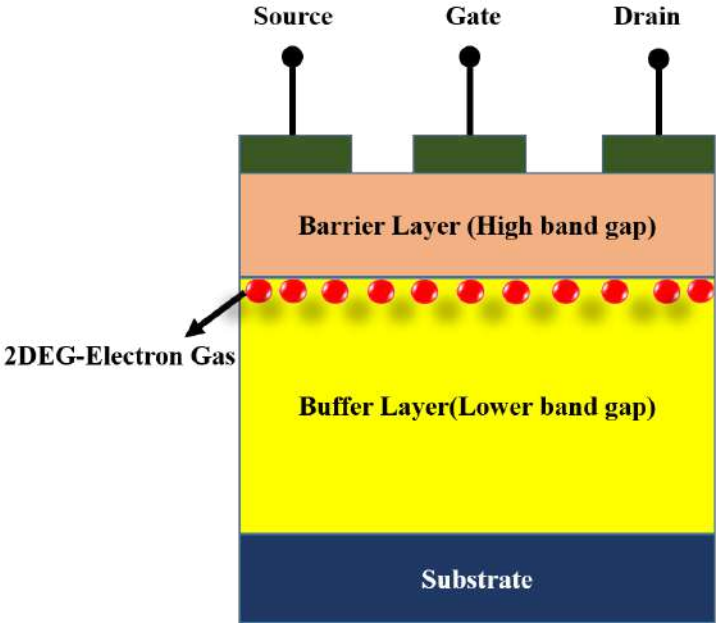

Figure. 1.1 Basic structural cross section of a HEMT *(Nirmal and Ajayan, 2019)*

material is grown over the narrow bandgap material. The structure of a HEMT is illustrated in **Figure 1.1**, showing the cross-section of the device. To create a HEMT, a substrate of semiconductor material is first prepared. On the substrate, the buffer layer is then grown, followed by the barrier layer. Both layers are usually doped with impurities to create n-type conductivity. The doping concentration in the barrier layer is higher than that in the buffer layer,

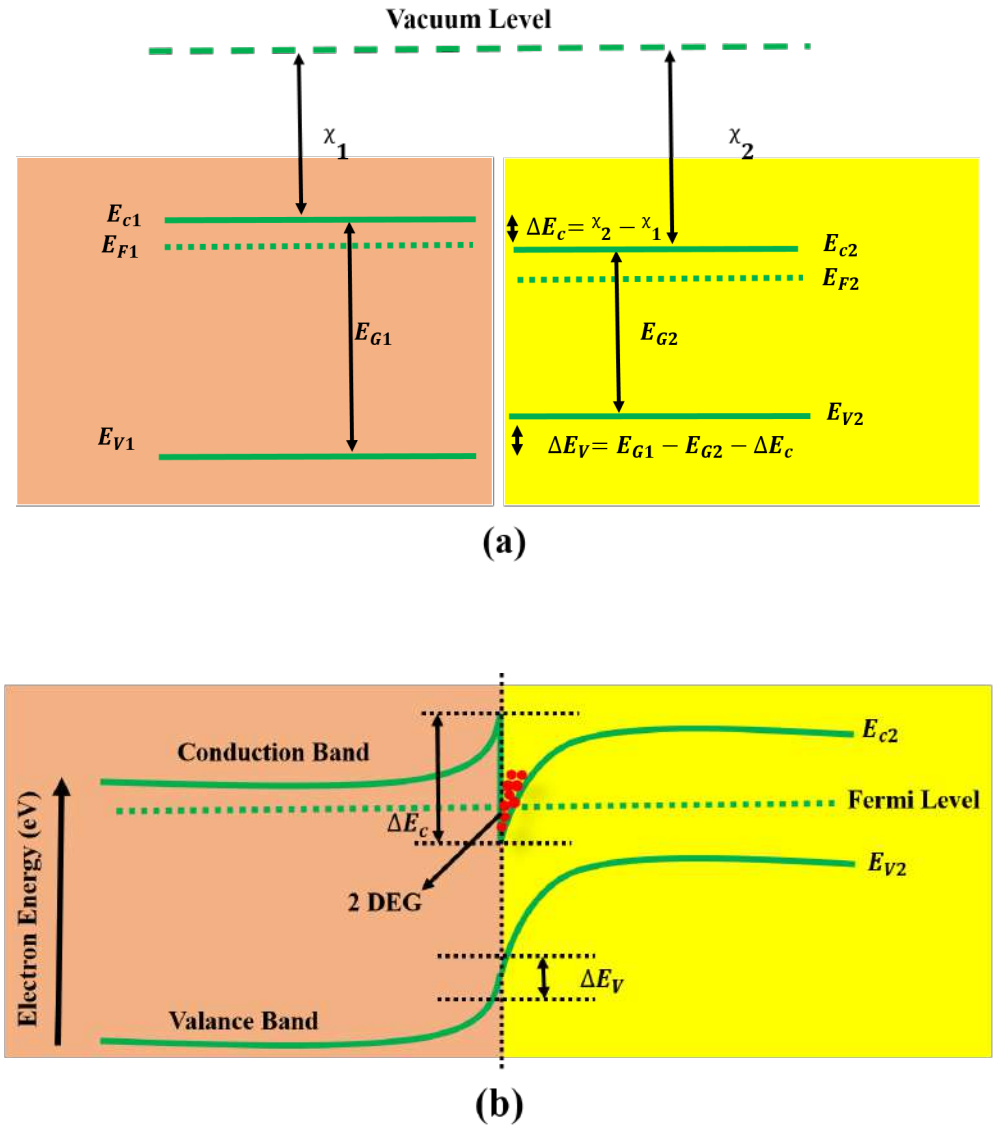

Figure. 1.2 Energy band diagram of heterostructure material (a) before forming the heterojunction (b) bend bending after forming the heterojunction *(Nirmal and Ajayan, 2019)*.

which creates a heterojunction. When the barrier layer is brought into contact with the buffer layer, electrons from the barrier layer diffuse into the buffer layer to achieve a minimum energy configuration. The electron transfer occurs because the two materials have different electron affinities, band gaps, and work functions. The electrons accumulate at the interface between the

two layers, forming a 2DEG with high mobility and conductivity.

The energy band diagram of the HEMT device in its state prior to the formation of the heterojunction is shown in **Figure 1.2 (a). Figure 1.2 (b)** shows the heterojunction interface formation when a material with a large band gap is brought into contact with a material with a small band gap**.** Due to band bending, a two-dimensional quantum well with a finite energy barrier is formed in the channel area. The electrons that are present in the channel are prevented from leaving the quantum well and are forced to remain at their respective energy levels, which results in the formation of a 2DEG. The electrons that are contained in the quantum well have very high mobility and are often referred to as two-dimensional electron gas. This is the distinguishing quality of HEMTs. Whereas the drain and source make ohmic contacts with the barrier layer, and the gate makes a schottky contact.

1.2.2 Piezoelectric and Spontaneous Polarization Effect

In AlGaN/GaN HEMT, 2DEG is not formed in the same way as it is in the more common AlGaAs/GaAs semiconductor at the heterojunction. **Figure 1.3 (a)** depicts the hexagonal or wurtzite crystal structure of GaN, in which the bilayers are composed of two closely spaced hexagonal layers created by Ga atoms and N atoms, respectively *(Qin et al., 2017)*. A strong net polarization field is induced at the AlGaN/GaN heterojunction interface because the wurtzite structure in GaN is not symmetrical, unlike other semiconductors like GaAs and InP with zincblende crystal structure (*Khan et al., 1994*). Since this polarization field is formed naturally by the GaN material's elemental makeup and crystalline structure, which refer as spontaneous polarization. Ga-face and N-face are the two primary classifications of GaN material, and they are determined by the direction in which the material grows. As can be seen in **Figure 1.3 (b)** the polarization field directions in the two distinct forms of GaN are directly opposed to one another. All of the devices that were examined in this study were constructed out of Ga-face GaN material.

The difference in polarization that exists between GaN and AlN may be attributed to the fact that structural factors have a substantial impact on the determination of spontaneous polarization *(Ambacher et al., 1999)*. While going from GaN to AlN, the crystal structure

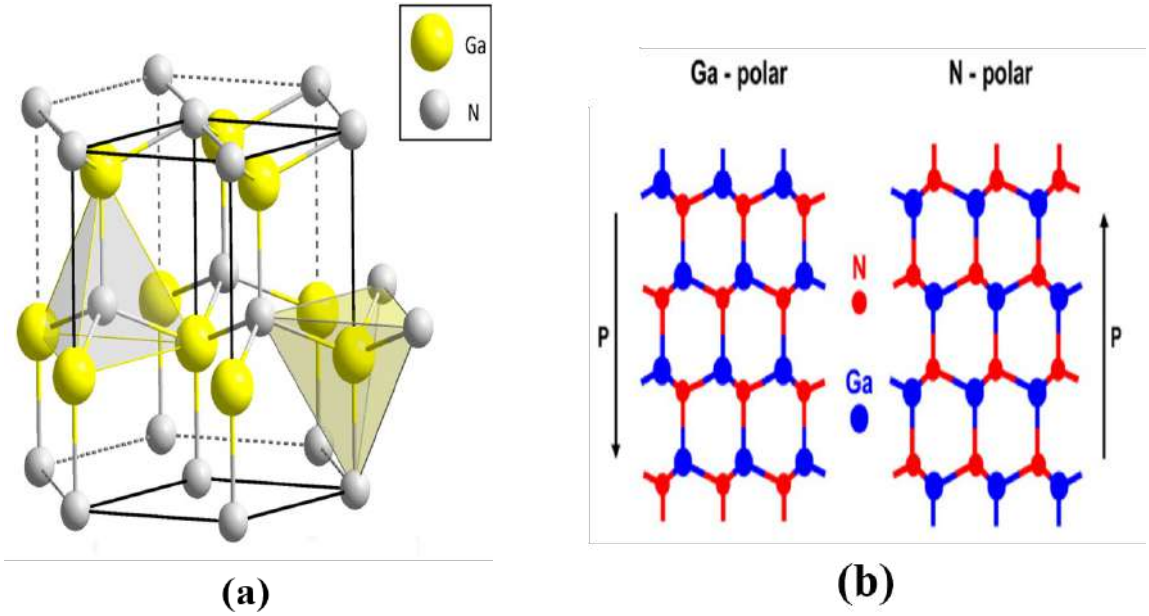

Figure. 1.3 (a) Wurtzite crystal structure of GaN *(Kente et al., 2016)* (b) Ga-face and N-face GaN crystal atomic arrangement *(Keller et al., 2014)*

becomes increasingly less perfect, which increases spontaneous polarization. The typical AlGaN/GaN epitaxial film developed along the [0001] axis has the only spontaneous polarization that is taken into consideration along that axis. $P_{SP} = P_{SP}.z$ is the relation that describes the spontaneous polarization along the c-axis.

Lattice mismatched GaN-based heterostructures, including AlGaN and AlN, exhibit an intriguing phenomenon known as piezoelectric polarization. This type of polarization is engendered by the strain that arises when dissimilar materials with varying lattice constants are combined in a heterostructure.

Notably, the critical thickness of the barrier layer plays a crucial role in determining the presence and magnitude of piezoelectric polarization *(Ambacher et al., 1999)*. The critical thickness is the maximum thickness at which the barrier layer can be formed without introducing any dislocations. The piezoelectric polarization is induced when the thickness of the AlGaN or AlN barrier is reduced below its critical value.

The piezoelectric polarization can be calculated using the values of e33 and e31, which are the coefficients of piezoelectricity *(Ambacher et al., 1999)*.

$$P_{PE} = e_{33}\varepsilon_z + e_{33}(\varepsilon_x + \varepsilon_y) \quad (1.1)$$

$$\varepsilon_z = \frac{C - C_o}{C_o} \tag{1.2}$$

$$\varepsilon_x = \varepsilon_y = \frac{a - a_o}{a_o} \tag{1.3}$$

The strain along the c-axis is denoted by the ε_z , where a_o and C_o are the equilibrium values of the lattice parameters. Wurtzite GaN lattice constants are related using the following equation.

$$\frac{C - C_o}{C_o} = 2\frac{C_{13}}{C_{33}}\left(\frac{a - a_o}{a_o}\right) \tag{1.4}$$

The net polarization along the c-axis can be determined by combining equations (1.1) and (1.4)

$$P_{PE} = 2\frac{a - a_o}{a_o}(e_{31} - e_{33})\frac{C_{13}}{C_{33}} \tag{1.5}$$

As can be seen in **Figure 1.4(a, b)**, the spontaneous polarization of Ga-face GaN and AlGaN is negative. This is due to the fact that the direction vector points in the direction of the substrate. **Figure 1.4(a)** demonstrates that, when the strain is tensile, the piezoelectric and spontaneous polarizations align parallel to each other. On the other hand, in the case of compressive strain, these polarizations adopt an anti-parallel orientation. This behavior is demonstrated and visually depicted in **Figure 1.4(b)**.

The polarization induced space charge density is given by:

$$\rho_P = \nabla . P \tag{1.6}$$

At the abrupt interface polarization sheet charge density (σ) of an AlGaN/GaN or GaN/AlGaN heterostructure is *(Ambacher et al., 1999)*:

$$\sigma = P(bottom) - P(top) \tag{1.7}$$

Free electrons will try to neutralise the charges caused by polarization if the polarization-generated sheet charge density is positive (+), and vice versa. At the heterojunction between the barrier and the buffer layer, these charges will begin to accumulate which will result in the formation of a 2DEG. These two polarization effects increase the device structure's electric field, which boosts 2DEG carrier concentration and channel confinement.

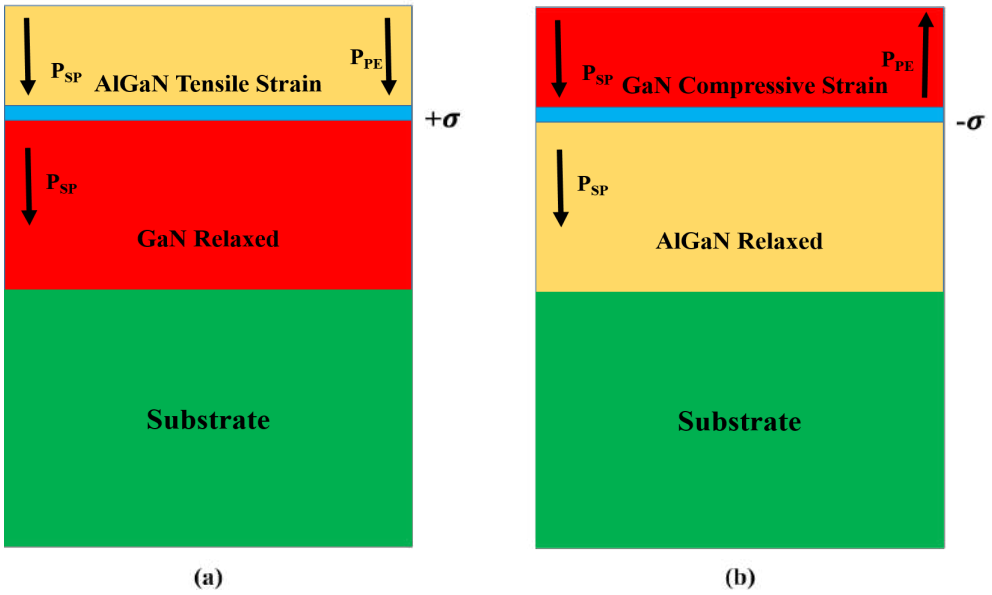

Figure. 1.4 Directions of spontaneous and piezoelectric polarization in AlGaN/GaN heterostructure (a) Tensile strain (b) Compressive strain *(Ambacher et al., 1999)*.

1.2.3 GaN-HEMT-Operation

Device operation requires a gate electrode to modulate drain-to-source current by controlling the density of 2DEG. Since the heterostructure causes the 2DEG to exist, a negative gate voltage is necessary to deplete it beneath the gate and stop the flow of current through the device. Therefore, GaN HEMTs that do not have specially engineered gate stacks are normally-on (also known as depletion-mode or D-mode) devices. **Figure 1.5(a)** shows the schematic structure of AlGaN/GaN HEMT. The output characteristics of a depletion mode AlGaN/GaN HEMT are shown in **Figure 1.5(b)**. Using a common source configuration is by far the most typical method of applying the bias to a HEMT. The input is at the gate electrode, the output at the drain electrode, and the common terminal at the source. The gate's input signal controls the device's state and may turn it on and off. To turn off a depletion mode device, a negative voltage is applied to the device, depleting the channel of electrons and creating a very resistive channel through which no current may flow, which is called pinch-off.

The equation that describes the relationship between the amount of applied bias voltage and the total number of carriers in the channel is as follows *(Ambacher et al., 2000)*:

$$n_s = \frac{\varepsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_{gs} - V_{TH}) \quad (1.8)$$

where, n_s, d_{AlGaN}, Δd, V_{gs}, and V_{TH} are the charge density per unit area of the 2DEG, AlGaN barrier layer thickness, distance of the 2DEG from the heterointerfaces, gate bias voltage, and threshold voltage.

Due to the term (V_{gs} -V_{TH}) in Equation 1.8, $n_s = 0$ for $V_{gs} = V_{TH}$, and the device is to be turned off. The channel of a HEMT is inherently densely packed with electrons at $V_{gs} = 0$ V, and applying a drain-to-source voltage will result in current flow between the source and drain.

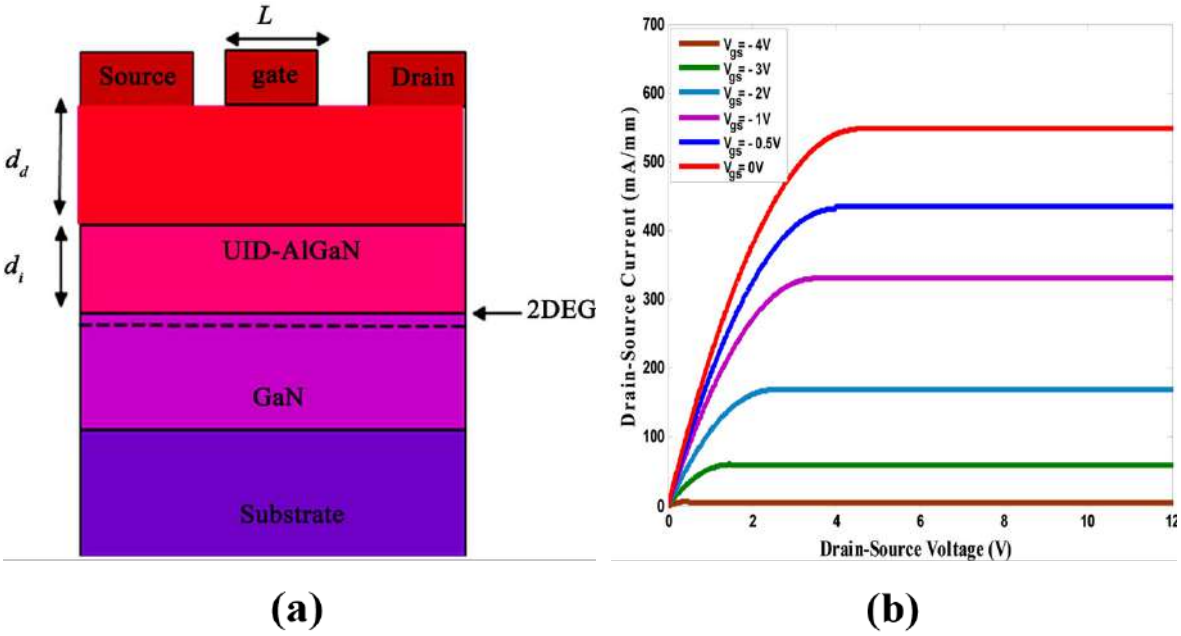

Figure. 1.5 (a) AlGaN/GaN HEMT structure (b) Drain characteristics of AlGaN/GaN HEMT for different gate bias *(Manel et al., 2012)*

The device is said to be operating in the linear regime when the drain voltage is low i.e. $V_{ds} < V_{gs} - V_{TH}$. Since the current is proportional to the electric field strength, the velocity of the electrons in the channel will rise as the field strength increases. At this instant, the current flowing between the source and the drain may be expressed as:

$$I_{ds} = qn_sV_{eff}W_G \quad (1.9)$$

where V_{eff} and W_G are the effective velocity and the gate width.

The electrons' velocity in the channel is a function of the electrons' mobility and the electric field strength as expressed by Equation 1.10.

$$V = \mu_n E \tag{1.10}$$

where μ_n and E are the electron mobility and applied electric field.

Carrier scattering through defects and dislocations in the semiconductor crystal impact electron mobility in the 2DEG of an AlGaN/GaN HEMT *(Germain et al., 2003)*. When $V_{ds} < V_{gs} - V_{TH}$, the current is demonstrated to grow linearly for low fields by using the result of Equation (1.10), which states that electron velocity grows with the applied electric field. Nevertheless, when the drain bias is high enough ($V_{ds} > V_{gs} - V_{TH}$), the effective electron velocity saturates and stops being affected by the bias or the electric field. In the saturated regime, the drain current is given by

$$I_{ds} = \frac{\varepsilon_{AlGaN}\, V_{sat} W_G}{(d_{AlGaN} + \Delta d)} (V_{gs} - V_{TH}) \tag{1.11}$$

The above equation shows that the at high drain bias, I_{ds} is independent of V_{ds}. In reality, I_{ds} is not absolutely free from V_{ds} influence. Under conditions of high drain bias, high electric fields emerge between the drain and gate contacts, potentially leading to the injection of electrons into the GaN buffer or captured by electron traps.

1.2.4 Device Engineering Techniques

1.2.4.1 Double Heterostructure HEMT with Graded Back Barrier

Double heterostructure HEMT with the graded back barrier is designed to enhance the performance of HEMT *(Gu et al., 2019)*. As shown in **Figure 1.6**, the barrier layer in this design is made of InAlN rather than AlGaN because the device's performance is enhanced by the lattice matching between the two materials (where the Al content of InAlN is 0.83) *(Neuburger et al., 2004)*. Between the InAlN barrier layer and the GaN channel layer lies an additional AlN interlayer. As AlN has a wider forbidden bandwidth, it may cause more discontinuity in the conduction band at the heterojunction interface, which is a major contributor to the dramatic rise in 2DEG concentration *(Shrestha et al., 2014)*. Increased device mobility is another benefit of the AlN in the $In_{0.17}Al_{0.83}N$/GaN heterojunction interface *(Teke et al., 2009)*. The leakage of 2DEG from the channel to the buffer is a problem for single heterostructure HEMTs. The

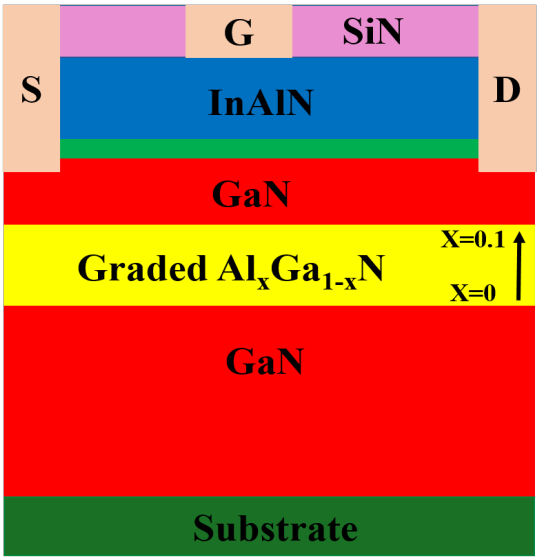

Figure. 1.6 Schematic representation of InAlN/GaN HEMT with graded back barrier *(Gu et al., 2019)*

utilization of a back-barrier, creating a double heterojunction structure, is a direct and effective approach for enhancing the confinement of the heterojunction 2DEG and minimizing the carrier overflow into the buffer layer. Many researchers have looked at the effects of AlGaN back-barrier layers on HEMTs structures. Carrier confinement is improved to some extent, but an undesirable parasitic channel is created at the interface of the AlGaN back-barrier and the GaN buffer. Parasitic channel effects may be reduced with the use of a graded AlGaN back-barrier in which the Al concentration varies linearly from 0 to 0.1. The findings show that the graded AlGaN back-barrier HEMT benefits greatly from the conduction band discontinuity at the GaN/AlGaN heterojunction interface, which greatly enhances carrier confinement. In contrast to the standard $Al_{0.1}Ga_{0.9}N$ back-barrier HEMT, a gradient Al composition results in full lattice relaxation without piezoelectric polarisation, which decreases the concentration of the parasitic electron channel's two-dimensional electron gas. Furthermore, a graded AlGaN back barrier may provide superior radio-frequency performance, greater transconductance, and higher current compared to the standard back-barrier HEMT with a fixed Al content.

1.2.4.2 Gate Field Plate HEMT

The use of field plate technology has gained significant attention in the field of electronic devices, specifically in high-electron-mobility transistors. Researchers have found that this

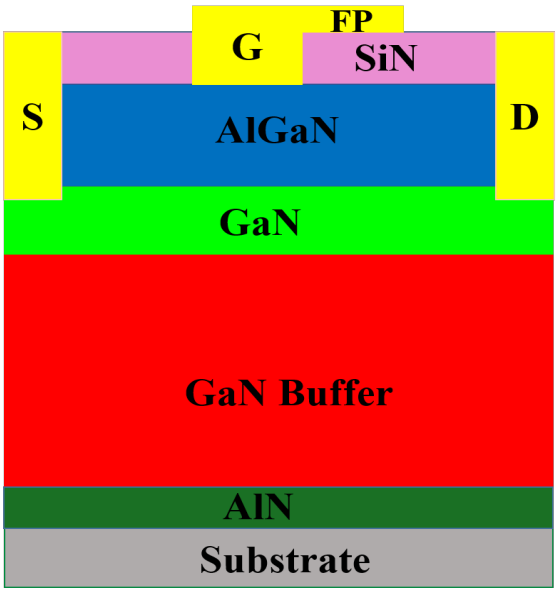

Figure. 1.7 Schematic representation of Gate field plate HEMT (*Kumar et al., 2022*)

innovative method offers a practical and efficient approach to enhancing the breakdown voltage of HEMTs by reducing the peak value of the electric field along the channel (*Karmalkar et al., 2001*). **Figure 1.7** illustrates a schematic view of a gate field plate HEMT, demonstrating the implementation of this technology (*Kumar et al., 2021*).

In a gate field plate HEMT, the gate is deposited onto the passivation layer and extended towards the drain side of the device. This extension of gate electrode toward drain side significantly minimizes the electric field at the surface of the AlGaN layer and enhances the breakdown voltage (*Karmalkar et al., 2005*). This improvement in breakdown voltage is of utmost importance in electronic devices as it not only enhances their power capabilities but also elevates their operational speed.

1.2.4.3 High Gate Multi-Recessed Buffer HEMT

The high gate multi-recessed buffer HEMT (HGMRB-HEMT) is an innovative design introduced (*Zhu et al., 2019*) to address two crucial aspects of device performance: breakdown voltage and RF characteristics. The structure of the HGMRB-HEMT incorporates specific features aimed at simultaneously enhancing these key parameters. In the HGMRB-HEMT, the barrier region is intentionally positioned lower than the source, drain, and gate electrodes, creating a higher gate section. This distinctive arrangement can be observed in **Figure 1.8**.

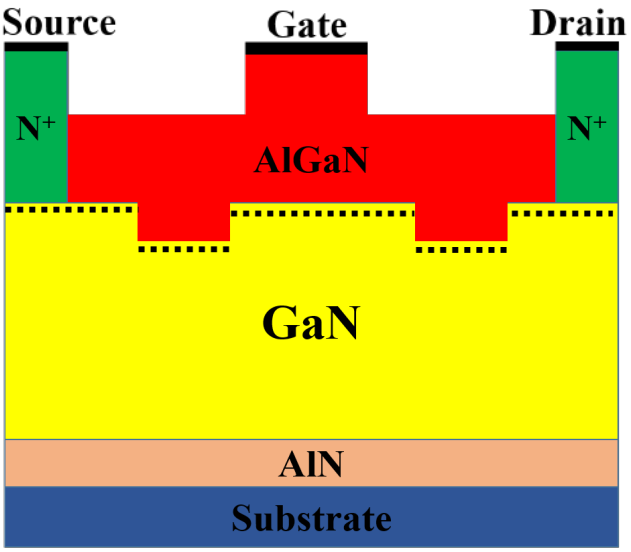

Figure. 1.8 Schematic representation of high gate multi recessed buffer HEMT (*Zhu et al., 2019*).

Additionally, the buffer layer of the HGMRB-HEMT includes recessed regions on both the left and right sides. These recessed regions contribute to the optimization of device performance.

When a high drain voltage is applied in traditional GaN HEMTs, a significant electric field builds up at the edge of the gate. This concentrated electric field can lead to a breakdown near the gate position on the drain side. The implementation of the HGMRB-HEMT introduces a modified electric field distribution that reduces the peak electric field at the edge of the gate electrode. This modification raises the HGMRB-HEMT's breakdown voltage by making it more resistant to greater drain voltages. The decrease in gate-to-source capacitance is yet another great feature of the HGMRB-HEMT. This reduction is primarily attributed to the presence of the high gate in the structure, which facilitates the diffusion of the depletion region mainly in a vertical downward direction. This reduces the capacitance between the gate and the source, which boosts the functionality of the device.

The enhancement in breakdown voltage and reduction in gate-to-source capacitance lead to enhanced output power density and power-added efficiency (PAE) of HGMRB-HEMT. Devices with higher breakdown voltages are capable of withstanding increased power levels without experiencing a breakdown, rendering them appropriate for high-power applications. The decrease in capacitance between the gate and source enables enhanced signal integrity and increased efficacy of power transmission, leading to greater output power density and power-

added efficiency (PAE). Hence HGMRB-HEMT is an attractive choice for applications that require both high power and high efficiency.

1.2.4.4 Double Channel MOS- HEMT

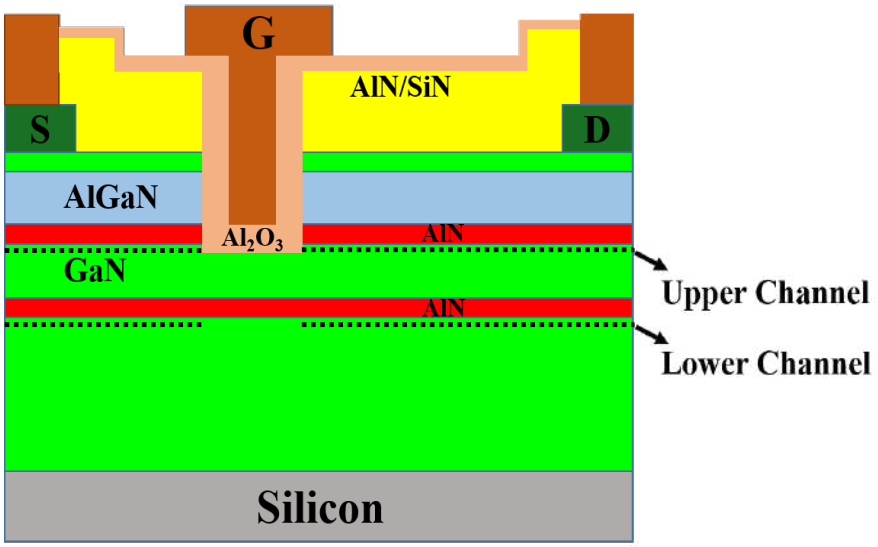

Figure. 1.9 Schematic representation of E mode double channel MOS-HEMT (*Wu et al., 2020*)

Figure 1.9 depicts a recessed gate in a DC-MOS-HEMT device from a two-dimensional perspective. When one examines the figure, it is immediately apparent that the DC-MOS-HEMT is composed of not one but two distinct channel layers. The amount of space that is available between the upper and lower channel layers is the primary factor that governs the distribution of electrons in each of these channel levels. As a result of the reverse electric field that is present in the GaN upper layer compared to the AlN layer, the 2DEG density in the lower channel is reduced when there is a big distance between these two channels. In contrast, the 2DEG density in the upper channel is increased when there is a high distance between these two channels. Additionally, the recessed gate design that is used in DC-MOS-HEMT devices assists to terminate the top channel and shift the threshold voltage to the positive side of the voltage scale. The DC-MOS-HEMT offers a strong subthreshold swing, which refers to the efficiency of the device in switching between on and off states. A lower subthreshold swing indicates better control over the device's conductive and non-conductive states, enhancing overall device performance and power efficiency.

1.2.4.5 P-Gate GaN HEMT

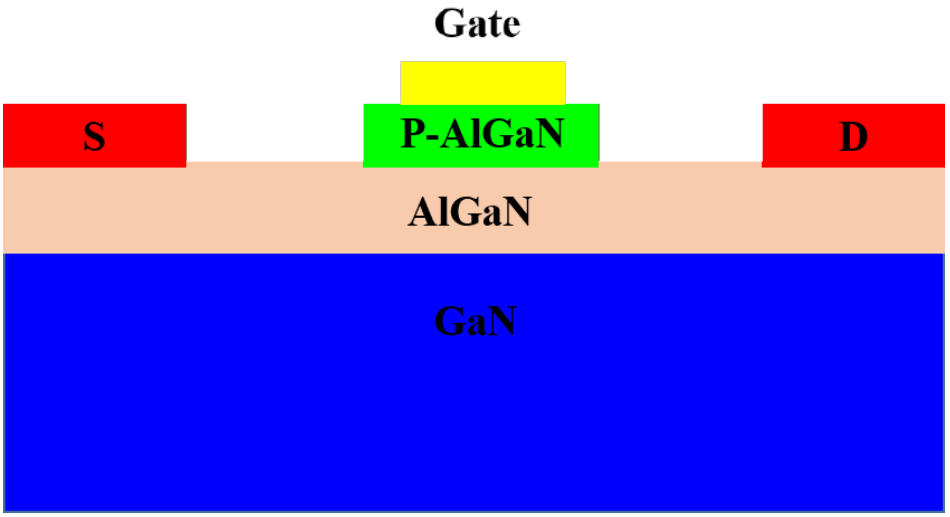

Figure. 1.10 Schematic representation of P-Gate GaN HEMT (*Greco et al., 2018*)

Adding a p-GaN (or p-AlGaN) layer to the AlGaN/GaN heterostructure at the gate contact area is the most promising strategy so far. Even in the absence of a bias (V_{gs} = 0) that is imposed from the outside, depletion of the 2DEG channel may still take place due to the p-GaN layer lifting the band diagram. **Figure 1.10** shows a simplified diagram of the basic operating principle of a E-mode HEMT with a p-GaN gate. In an AlGaN/GaN heterostructure, normally-on operation is achieved by using a conventional schottky contact as the gate electrode. However, when a p-GaN cap layer is added to the AlGaN, the AlGaN's conduction band is raised, and the 2DEG is depleted. This allows for the possibility of normally-off functioning of the device.

1.2.4.6 Ferroelectric Gate GaN HEMT

Ferroelectric gate AlGaN/GaN HEMT construction is shown in **Figure 1.11.** Ferroelectric materials have a strong polarization effect, which can control the polarization in 2-D electron gases (2DEG) and threshold voltage. E-mode GaN-based HEMTs are possible because ferroelectric polarization is opposite to nitride polarization, which is dependent on the growth process and applied voltage. The E-mode ferroelectric gate HEMTs with V_{th} = 1 V had a very high field-effect mobility of 1819 cm^2/Vs, a low SS of 90 mV/dec, and a significant I_{ON}/I_{OFF} of 1.5×10^{10} (*Zhu et al., 2017*). As the 2DEG channel is preserved in ferroelectric gate E-mode

HEMTs, they are excellent candidates for use in high-speed logic circuits.

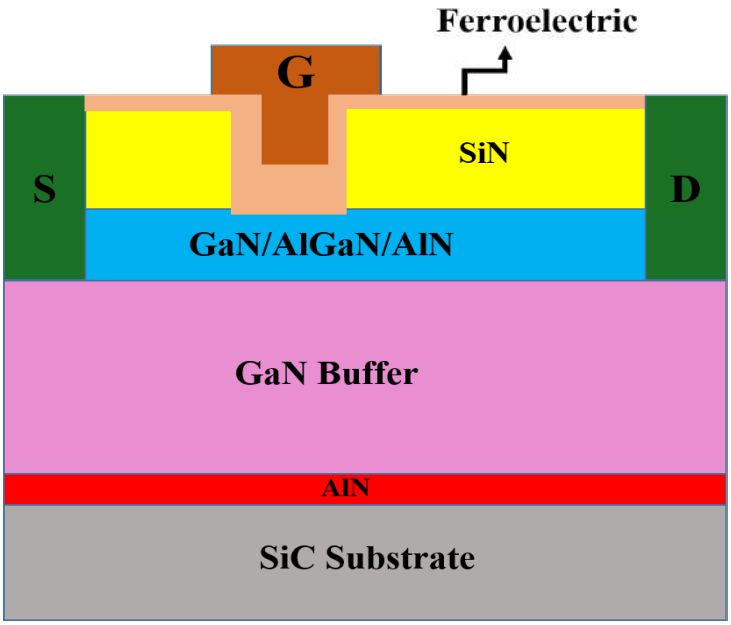

Figure. 1.11 Schematic representation of ferroelectric gate GaN-HEMT (*Zhu et al., 2017*)

1.3 Advantages of GaN HEMT

1. High Power Density: GaN HEMTs offer higher power density compared to traditional silicon-based transistors, enabling smaller and more compact power electronic systems.

2. High Switching Speed: GaN HEMTs have fast switching speeds in the nanosecond range, which makes them well-suited for high-speed switching applications such as wireless communication systems, radar, and power converters.

3. High Breakdown Voltage: GaN HEMTs have a wide bandgap, which allows them to handle high voltage levels without experiencing a premature breakdown, making them suitable for high-voltage applications.

4. Wide Temperature Range: GaN HEMTs can operate at high temperatures, which makes them useful in high-temperature applications such as aerospace, automotive, and industrial environments.

1.4 Challenges Confronted by the GaN HEMT

Although GaN HEMT devices showcasing outstanding performance in RF and microwave power applications, they predominantly operate in depletion mode (d-mode). However, the market demand leans towards enhancement mode (E-mode) devices. Consequently, extensive research and development have been dedicated to E-mode HEMTs and metal-oxide-semiconductor field-effect transistors (MIS-HEMTs) in recent years, driven by the increasing demand from various applications. The utilization of E-mode devices in RF/microwave circuits enables the elimination of negative-polarity power supply, simplifying the circuit and system architecture. Additionally, power switches based on E-mode devices offer intrinsic fail-safe operation, making them highly desirable for power electronics. Various methods have been proposed for realizing E-mode devices, such as thin barrier structures (*Endoh et al., 2004*), fluorine plasma treatment (*Su et al., 2014*), and p-GaN cap structures (*Hu et al., 2000*). Each approach has its own advantages and disadvantages, leaving room for further improvement.

One significant challenge encountered with HEMT technology is the undesired spilling of 2DEG from the GaN channel to the buffer layer, leading to reduced mobility and device reliability (*Khan et al., 1992*). Numerous techniques have been reported to address this issue and prevent the overflow of 2DEG into the buffer layer. For instance, the double heterostructure HEMT method introduces a back-barrier layer between the channel and the buffer layer (*Gu et al., 2019*). This approach, considered the simplest and most effective way to enhances the confinement of the heterojunction 2DEG and prevents excessive carrier flow into the buffer layer. Various studies (*Chen et al., 2003, Lee et al., 2011, Meng et al., 2012*) have explored the impact of AlGaN back-barrier layers on HEMTs. To some extent, the carrier confinement is improved using this approach, but it also creates a parasitic channel at the junction between the AlGaN back barrier and the GaN buffer. Researchers have also adopted another technique involving doping the buffer layer with iron (Fe) or carbon (C) acceptors to increase its resistivity (*Pampili and Parbrook, 2017*). However, these dopants generate deep-level acceptors in the layer, leading to current collapse (*Uren et al., 2012*).

Another significant challenge that GaN HEMT encounters is related to its strain problem, which arises due to the lattice mismatch at the interface of GaN/AlGaN. At the interface between the barrier-layer and buffer of the AlGaN/GaN HEMT, a polarization discontinuity is formed,

resulting from piezo and spontaneous polarization. This polarization discontinuity generates a highly mobile sheet charge that serves as the channel charge. The polarization discontinuity of standard AlGaN/GaN-HEMTs, which incorporates piezo and random components, is proportional to the aluminium concentration in the barrier layer. Either using modulation doping or increasing the amount of aluminium in the barrier layer is required in order to achieve the desired increase in sheet charge density and subsequent increase in maximum DC-output current. However, excessive Al concentration increases strain and degrades the material quality. Thus, it is crucial to explore new barrier engineering approaches that can overcome the strain issue and enhance the device's performance.

1.5 Research Objectives

1. To create a GaN HEMT that can surmount the major challenges of GaN HEMT such as spilling of 2DEG and high leakage current. For this, various engineering schemes such as polarization-doped buffer engineering, T-shaped gate metal engineering, and InAlN/AlN barrier engineering have been amalgamated over GaN HEMT.

2. To investigate the influence of a high-k dielectric material, specifically HfO_2, on the performance of an E-mode T-gate InAlN/AlN HEMT with a polarization-doped buffer. The primary goal here is to get a knowledge of how the presence of HfO_2 changes the electrical properties of the device as well as its overall performance. By examining parameters such as threshold voltage, transconductance, and subthreshold slope, the impact of the high-k dielectric on the device's performance can be evaluated.

3. To investigate the impact of T-shaped gate geometry on parasitic capacitance and RF Figure of Merits (FOMs) such as maximum oscillation frequency, gain-bandwidth product, cut-off frequency, maximum stable and available power gain, maximum transducer power gain and stability factor of E-mode T-gate InAlN/AlN HEMT with polarization doped buffer.

4. To examine the small signal and noise behavior of T-gate E mode HEMT with a polarization-doped buffer. By studying the small signal and noise behaviour, valuable insights can be gained regarding the device's overall performance, signal amplification capabilities, and noise figure.

5. To design the double channel E-mode T-gate HEMT with back barrier which significantly affects the current driving capability and the switching performance. The various performance parameters, such as drain current, transconductance, intrinsic gain, output conductance, early voltage, parasitic capacitances, cut-off frequency, maximum oscillation frequency, gain frequency product, transconductance frequency product, and gain transconductance frequency product, can be evaluated in order to reflect its effectiveness in RF applications.

6. To examine the influence of the back barrier distance from the lower channel in an E-mode T-gate double channel HEMT. In order to assess the linearity and intermodulation distortion parameters, which are critical for evaluating the performance of modern high-frequency wireless communication systems.

1.6 Thesis Organization

This thesis is divided into six chapters, each of which is aimed to address specific research objectives. At the end of the respective chapter the references to each chapter are listed.

Chapter 1 introduces wide-bandgap materials, focusing on gallium nitride (GaN)'s importance in power electronics. The chapter covers GaN HEMT basics including the polarization effect and operating principle. The chapter also examines literature-reported device engineering schemes. These schemes include the double heterostructure HEMT with a graded back barrier, gate field plate, high gate multi-recessed buffer, double-channel MOS-HEMT, P-gate GaN HEMT and Ferroelectric gate GaN HEMT. These engineering methods are described to demonstrate their potential performance improvements in GaN HEMT technology. The chapter also discusses GaN HEMT challenges. Lastly, the Chapter concludes by outlining the overall organization of the thesis. It emphasizes the significance of the research presented in this thesis.

Chapter 2 describes the proposed device along with simulation parameters. The chapter also describes the simulation models used in this investigation, including their calibration using experimental data from relevant literature. A step-by-step fabrication process flow is shown to determine device fabrication feasibility. The chapter examines how gate and drain bias, gate recessed depth, and high k gate dielectric affect the electrical and RF performance of E-mode T-gate InAlN/AlN HEMTs with polarization doped buffer *(Sharma and Chaujar, 2022*,

Sharma et al., 2023a).

Chapter 3 investigates the impact of T-shaped gate geometry on parasitic capacitance and RF Figure of Merits (FOMs) such as maximum oscillation frequency (f_{max}), gain-bandwidth product (GBP), cut-off frequency (f_T), maximum stable and available power gain (Gms and Gma), maximum transducer power gain (MSG) and stability factor (k) of E-mode T-gate InAlN/AlN HEMT with polarization doped buffer. Furthermore, the chapter investigates the impact of gate head length (H_{length}), gate stem height (S_{height}), and gate foot length (F_{length}) on the RF FOMs. The simulation results for the proposed device structure showcase its suitability for high-performance RF/microwave applications.

Chapter 4 discusses the characteristics of a T-gate E mode HEMT with a polarization-doped buffer, focusing on its small signal and noise behaviour. The polarization-induced doping in the buffer layer creates an upwardly convex conduction band, resulting in improved confinement of the 2DEG, reduced buffer leakage current, and significantly enhanced transconductance. This increase in transconductance leads to a decrease in the reflection coefficient (S11, S22) and an improvement in the transmission coefficient (S21) compared to GaN buffer HEMTs. The various noise parameters, including the minimum noise figure, noise conductance, and auto/cross-correlation factor for the proposed device are evaluated. The simulated results indicate that the T-gate polarization-doped buffer (PDB-HEMT) structure is an excellent choice for Low Noise Amplifiers (LNA) operating at higher frequencies *(Sharma et al., 2023b).*

Chapter 5 discusses the design and analysis of E-mode T-gate double-channel High Electron Mobility Transistor (HEMT) with an InGaN back barrier. The formation of the double channel is due to the addition of the AlN layer underneath the InAlN/GaN interface, which in turn results in an increase in the drain current density of 2.5 A/mm. However, due to a lack of gate controllability over a lower channel, a high leakage current is observed in double channel HEMT. The use of InGaN as a back barrier allowed for the successful resolution of this issue. This increases the conduction band for the GaN buffer, which results in better carrier confinement in 2DEG. The proposed device's performance is measured against that of standard double-channel HEMT. Various performance parameters, such as drain current (I_{ds}), transconductance (g_m), intrinsic gain (A_v), output conductance (g_d), early voltage (V_{EA}), TGF, parasitic capacitances (C_{gs}, C_{gd}), cut-off frequency (f_T), maximum oscillation frequency (fmax), gain frequency product (GFP), transconductance frequency product (TFP), and gain

transconductance frequency product (GTFP), are investigated. Furthermore, the linearity parameters such as VIP2, VIP3, IIP3, 1-dB compression point has been investigated by varying the back barrier distance from the lower channel. *(Sharma and Chaujar, 2021).*

Chapter 6 provides a summary of the overall research work illustrated in this thesis. Additionally, this chapter explores the potential for future advancements and discusses how this work can be expanded and used in future for further research directions.

1.7 References

AMBACHER, O., FOUTZ, B., SMART, J., SHEALY, J. R., WEIMANN, N. G., CHU, K., MURPHY, M., SIERAKOWSKI, A. J., SCHAFF, W. J., EASTMAN, L. F., DIMITROV, R., MITCHELL, A. and STUTZMANN, M. 2000. Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures. Journal of applied physics, 87, 334-344.

AMBACHER, O., SMART, J., SHEALY, J. R., WEIMANN, N. G., CHU, K., MURPHY, M., SCHAFF, W. J., EASTMAN, L. F., DIMITROV, R., WITTMER, L., STUTZMANN, M., RIEGER, W. and HILSENBECK, J. 1999. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures. Journal of applied physics, 85, 3222-3233.

ASIF KHAN, M., KUZNIA, J. N., OLSON, D. T., SCHAFF, W. J., BURM, J. W., and SHUR, M. S. 1994. Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor. Applied Physics Letters, 65, 1121-1123.

CAI, Y., GONG, Y., BAI, J., YU, X., ZHU, C., ESENDAG, V., LEE, K. B. and WANG, T. 2018. Controllable uniform green light emitters enabled by circular HEMT-LED devices. IEEE Photonics Journal, 10, 1-7.

CHEN, C. Q., ZHANG, J. P., ADIVARAHAN, V., KOUDYMOV, A., FATIMA, H., SIMIN, G., YANG, J. and ASIF KHAN, M.2003. AlGaN/GaN/AlGaN double heterostructure for high-power III-N field-effect transistors. Appl. Phys. Lett., 82, 4593-4595.

CHUNG, J. W., HOKE, W. E., CHUMBES, E. M., and PALACIOS, T. 2010. AlGaN/GaN

HEMT With 300-GHz fmax. IEEE Electron Device Letters, 31, 195-197.

ENDOH, A., YAMASHITA, Y., IKEDA, K., HIGASHIWAKI, M., HIKOSAKA, K., MATSUI, T., HIYAMIZU, S. and MIMURA, T.2004.Non-Recessed-Gate Enhancement-Mode AlGaN/GaN High Electron Mobility Transistors with High RF Performance.*Jpn. J. Appl. Phys.,*43, 2255.

GASKA, R., CHEN, Q., YANG, J., OSINSKY, A., KHAN, M. A., and SHUR, M. S. 1997. High-temperature performance of AlGaN/GaN HFETs on SiC substrates. IEEE Electron Device Letters, 18, 492-494.

GERMAIN, M., LEYS, M., BOEYKENS, S., DEGROOTE, S., WANG, W., SCHREURS, D., RUYTHOOREN, W., CHOI, K. H., VAN DAELE, B., VAN TENDELOO, G. and BORGHS, G. 2003. High electron mobility in AlGaN/GaN HEMT grown on sapphire: strain modification by means of AlN interlayers. MRS Online Proceedings Library (OPL), 798, Y10-22.

GRECO, G., IUCOLANO, F., and ROCCAFORTE, F. 2018. Review of technology for normally-off HEMTs with p-GaN gate. Materials Science in Semiconductor Processing, *78*, 96-106.

GU, Y., CHANG, D., SUN, H., ZHAO, J., YANG, G., DAI, Z., and DING, Y. 2019. Theoretical study of InAlN/GaN high electron mobility transistor (HEMT) with a polarization-graded AlGaN back-barrier layer. Electronics, 8, 885.

HU, X., SIMIN, G.,YANG, J., ASIF KHAN, M., GASKA, R. and SHUR, M.S.2000. Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate.*Electronics Letters*,36,753-754.

KAMECHE, M., and DROZDOVSKI, N. V. 2005. GaAs-, InP-and GaN HEMT-based microwave control devices: what is best and why. Microwave Journal, 48, 164-173.

KARMALKAR, S., and MISHRA, U. K. 2001. Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate. IEEE transactions on electron devices, 48, 1515-1521.

KARMALKAR, S., SHUR, M. S., SIMIN, G., and KHAN, M. A. 2005. Field-plate engineering for HFETs. IEEE Transactions on electron devices, 52, 2534-2540.

KELLER, S., LI, H., LAURENT, M., HU, Y., PFAFF, N., LU, J., and BROWN, D. F. (2014). N. A. FICHTENBAUM, JS SPECK, SP DENBAARS, UK MISHRA, Recent progress in metal-organic chemical vapor deposition of (000-1) N-polar group-III nitrides. Semiconductor Science and Technology, 29, 113001.

KEMERLEY, R. T., WALLACE, H. B., and YODER, M. N. 2002. Impact of wide bandgap microwave devices on DoD systems. Proceedings of the IEEE, 90, 1059-1064.

KENTE, T., and MHLANGA, S. D. 2016. Gallium nitride nanostructures: Synthesis, characterization and applications. Journal of Crystal Growth, 444, 55-72.

KHAN, M. A., KUZNIA, J. N., OLSON, D. T., SCHAFF, W. J., BURM, J. W., and SHUR, M. S. 1994. Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor. *Applied Physics Letters*, *65*, 1121-1123.

KHAN, M.A., KUZNIA, J.N., HOVE, J.M., PAN, N., and CARTER, J. 1992. Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-AlxGa1-xN heterojunctions. *Appl. Phys. Lett.*,60,3027–3029.

KUMAR, J. R., NIRMAL, D., HOODA, M. K., SINGH, S., AJAYAN, J., and ARIVAZHAGAN, L. 2021. Intensive study of field-plated AlGaN/GaN HEMT on silicon substrate for high power RF applications. Silicon, 1-6.

KUMAR, V., LU, W., SCHWINDT, R., KULIEV, A., SIMIN, G., YANG, J., KHAN, M. A. and ADESIDA, I. 2002. AlGaN/GaN HEMTs on SiC with f T of over 120 GHz. IEEE Electron Device Letters, 23, 455-457.

KUZMÍK, J. 2001. Power electronics on InAlN/(In) GaN: Prospect for a record performance. IEEE Electron Device Letters, 22, 510-512.

LEE, D.S.,GAO, X., GUO, S., and PALACIOS, T.2011. InAlN/GaN HEMTs with AlGaN back barriers. IEEE Electron Devcies Lett.,32, 617–619.

LIM, T., AIDAM, R., WALTEREIT, P., HENKEL, T., QUAY, R., LOZAR, R., MAIER, T., KIRSTE, L. and AMBACHER, O. 2010. GaN-based submicrometer HEMTs with lattice-matched InAlGaN barrier grown by MBE. IEEE Electron Device Letters, 31, 671-673.

MANEL, C., HAFEDH, B., MOHAMED ALI, Z., and HASSEN, M. 2012. 2-D Theoretical

Model for Current–Voltage Characteristics in AlGaN/GaN HEMT's. Journal of Modern Physics, 2012.

MENG, F., ZHANG, J., ZHOU, H., MA, J., XUE, J., DANG, L., ZHANG, L., LU, M., AI, S., LI, X., and HAO, Y.2012. Transport characteristics of AlGaN/GaN/AlGaN double heterostructures with high electron mobility. J. Appl. Phys.,112, 023707.

NEUBURGER, M., ZIMMERMANN, T., KOHN, E., DADGAR, A., SCHULZE, F., KRTSCHIL, A., GUNTHER, M., WITTE, H., BLASING, J., KROST, A., DAUMILLER, I. and KUNZE, M. 2004. Unstrained InAlN/GaN HEMT structure. In Proceedings. IEEE Lester Eastman Conference on High Performance Devices. 161-166.

NIRMAL, D., and AJAYAN, J. (Eds.). 2019. Handbook for III-V high electron mobility transistor technologies. CRC Press.

PAMPILI, P. and PARBROOK, P.J.2017. Doping of III-nitride materials.Mater. Sci. Semicond. Process.,62,180–191.

QIN, H., LUAN, X., FENG, C., YANG, D., and ZHANG, G. 2017. Mechanical, thermodynamic and electronic properties of wurtzite and zinc-blende GaN crystals. Materials, 10, 1419.

RAIS-ZADEH, M., ZHU, H., and ANSARI, A. 2017. Applications of gallium nitride in MEMS and acoustic microsystems. In 2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) (pp. 9-11). IEEE.

SHARMA, M., and CHAUJAR, R. 2021. Design and investigation of recessed-T-gate double channel HEMT with InGaN back barrier for enhanced performance. Arabian Journal for Science and Engineering, 1-8.

SHARMA, M., and CHAUJAR, R. 2022. Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications," Int. J. RF Microw. Comput. Aided Eng.,32,23057.

SHARMA, M., KUMAR, B. and CHAUJAR, R. 2023a. Polarization induced doping and high-k passivation engineering on T-gate MOS-HEMT for improved RF/microwave performance. Materials Science and Engineering,290,116298.

SHARMA, M., KUMAR, B., and CHAUJAR, R. 2023b. Small signal and noise analysis of T-gate HEMT with polarization doped buffer for LNAs. Micro and Nanostructures, 180, 207593.

SHRESTHA, N. M., LI, Y., and CHANG, E. Y. 2014. Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer. Japanese Journal of Applied Physics, 53, 04EF08.

SMORCHKOVA, I. P., CHEN, L., MATES, T., SHEN, L., HEIKMAN, S., MORAN, B., ... KELLER, S., DENBAARS, S.P., SPECK, J. S. and MISHRA, U. K. 2001. AlN/GaN and (Al, Ga) N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy. Journal of Applied Physics, 90, 5196-5201.

SU, L.Y., LEE, F. and HUANG, J.J.2014. Enhancement-Mode GaN-Based High-Electron Mobility Transistors on the Si Substrate With a P-Type GaN Cap Layer.*IEEE Transactions on Electron Devices*,61,460-465.

TEKE, A., GÖKDEN, S., TÜLEK, R., LEACH, J. H., FAN, Q., XIE, J., OZGUR, U., MORKOC, H., LISESIVDIN, S. B., ÖZBAY, E. 2009. The effect of AlN interlayer thicknesses on scattering processes in lattice-matched AlInN/GaN two-dimensional electron gas heterostructures. New Journal of Physics, 11, 063031.

TREW, R. J. 2002. SiC and GaN transistors-is there one winner for microwave power applications?. Proceedings of the IEEE, 90, 1032-1047.

UREN, M. J., MOREKE, J. and KUBALL, M.2012. Buffer design to minimize current collapse in GaN/AlGaN HFETs.IEEE Trans. Electron Devices,59,3327–3333.

WANG, R., LI, G., KARBASIAN, G., GUO, J., SONG, B., YUE, Y., HU, Z., LABOUTIN, O., CAO, Y., JOHNSON, W., SNIDER, G., FAY, P., JENA, D. and XING, H. G. 2013. Quaternary Barrier InAlGaN HEMTs With fT/ fmax of 230/300 GHz. IEEE Electron Device Letters, 34, 378-380.

WU, T. L., TANG, S. W., and JIANG, H. J. 2020. Investigation of recessed gate AlGaN/GaN MIS-HEMTs with double AlGaN barrier designs toward an enhancement-mode characteristic. Micromachines, 11, 163.

WU, Y. F., KAPOLNEK, D., IBBETSON, J. P., PARIKH, P., KELLER, B. P., and MISHRA,

U. K. 2001. Very-high power density AlGaN/GaN HEMTs. IEEE Transactions on Electron Devices, 48, 586-590.

ZHU, S., JIA, H., LI, T., TONG, Y., LIANG, Y., WANG, X., ZENG, T. and YANG, Y. 2019. Novel high-energy-efficiency AlGaN/GaN HEMT with high gate and multi-recessed buffer. Micromachines, 10, 444.

ZHU, J., CHEN, L., JIANG, J., LU, X., YANG, L., HOU, B., LIAO, M., ZHOU, Y., MA, X. and HAO, Y. 2017. Ferroelectric gate AlGaN/GaN E-mode HEMTs with high transport and sub-threshold performance. IEEE Electron Device Letters, 39, 79-82.

CHAPTER 2

Simulation of T-Gate E-Mode HEMT with Polarization Induced Doped Buffer for Electrical and RF Performance

This chapter focuses on the DC and RF performance of T-gate E mode HEMT with polarization induced doped buffer. The proposed device has the feature of polarization induce doping in the buffer layer (buffer Engineered), heavily doped source/drain region, and recessed T-gate (Gate Metal Engineered) structure. The polarization-induced doping in the buffer layer bent the conduction band upwardly convex, which enhanced the 2DEG confinement, reduced the buffer leakage current, and significantly uplifted the breakdown voltage (33 V), which is 5 times higher than the conventional InAlN/AlN GaN buffer HEMT (8 V). The recessed gate engineering further enhances various performance parameters. It achieves an impressive I_{on}/I_{off} ratio of 10^9, reduces the subthreshold swing (SS) to 78 mV/dec, and minimizes the drain-induced barrier lowering (DIBL) to 100 mV/V. The proposed device exhibits a high current density of 2.8 A/mm, transconductance 1.55 S/mm, cutoff frequency f_T (583 GHz), and maximum oscillation frequency f_{max} (840 GHz). At room temperature, the carrier density and mobility measured are 2.8×10^{13} cm^{-2} and 1250 cm^2/Vs. The large Johnson figure of merit ($f_T . V_{BR}$) 19.23 THz and $(f_T . f_{max})^{1/2}$ 699 GHz shows the potential of the proposed device for high-power millimeter-wave applications.

Additionally, high-k gate oxide engineering has also been conducted in this chapter, where a specific region of the recessed gate is substituted with a high-k dielectric material. This integration of the high-k dielectric brings about notable improvements in both interfacial and transport characteristics, while concurrently reducing the gate leakage current. Nevertheless, it is important to note that implanting the gate oxide alone does not enable E-mode operation. As a result, the superior option for achieving E-mode operation is through the utilization of gate-recessed engineering techniques.

2.1 Introduction

The HEMT is a special type of field effect transistor designed to operate at microwave frequencies. The HEMT is able to function at extremely high microwave frequencies and has a low noise figure. This is a very desirable combination. As a consequence of this, the device is utilized in regions of RF design in which it is necessary to achieve good performance at extremely high RF frequencies. Over the past few years, researchers have significantly enhanced the capabilities of GaN-based transistors used in high-frequency RF power amplifiers. Significant progress has been made in bridging the performance difference between low bandgap semiconductor technologies through advancements in raising the maximum cut-off frequency from several tens of GHz to around 450 GHz. Likewise, innovative methods for maintaining high speeds within broad bias ranges and cutting-edge technologies for enhancing peak frequency performance have emerged. Notably, HEMT devices find application across various RF design domains including radio astronomy, radio telecommunications, direct broadcast receivers (DBS), and RADAR (Radio Detection and Ranging System).

Recently, there has been a lot of interest in AlGaN/GaN HEMTs as a possible technology for the next generation. In order for mobile communication applications to improve, the upcoming generation of cell phones should have a broader frequency range and be more effective than the previous ones. The progress in satellite transmission and TV programming also requires amplifiers that can function at higher frequencies and power. Considering these requirements, AlGaN/GaN HEMTs are an excellent choice for utilizing microwave power in wireless communication due to their exceptional properties. AlGaN/GaN HEMTs have been the subject of several studies *(Mishra et al., 2002, Sano et al., 2018)* due to their usefulness in high RF applications. However, AlGaN/GaN HEMT also faces a number of difficulties that prevent it from being widely used. The primary roadblock that AlGaN/GaN HEMT faces is its strain problem, which is originates from the lattice mismatch between the GaN and AlGaN contact. As described in **Chapter- 1** *(Ambacher et al., 2000*), the polarization discontinuity at the interface barrier-layer / buffer of the AlGaN/GaN HEMT forms a highly mobile sheet charge serving as the channel charge. This charge is caused by piezo and spontaneous polarization respectively. The polarization discontinuity of standard AIGaN/GaN-HEMTs, which include

piezo and random components, is proportional to the aluminium concentration in the barrier layer. Either the aluminium content of the barrier layer needs to be increased, or modulation doping needs to be used in order to achieve the desired increase in sheet charge density and subsequent increase in maximum DC-output current. However, excessive Al concentration increases strain and degrades the material quality.

In this contribution, an InAIN layer is used in place of an AlGaN barrier layer, which results in the formation of a new layer structure. The greater spontaneous polarization of InAIN in comparison to AIGaN *(Kuzmik, 2001*) makes this layer structure capable of producing theoretically higher sheet charge concentrations. For In contents below 17%, InAIN layers can be grown under tensile stress on GaN, and for In contents above 17%, InAIN layers must be grown under compressive stress. By maintaining an In composition of 17% in the overall structure, the lattice of InAlN matches that of the GaN layer, thereby reducing strain at the InAlN/GaN junction *(Kuzmik, 2001)*. High sheet charge concentrations of 2.9 x 10^{13} cm^{-2} are anticipated when this technology is applied to InAlN/GaN HEMTs enhancing the drain current density of 3.3 A/mm, which is 205% higher than the AlGaN HEMT *(Kuzmik, 2001*). The InAlN/AlN-based HEMTs allow the device's aggressive scaling, empowering the cutoff frequency and reducing the short-channel effects (SCEs). Nowadays, InAlN/GaN attracted much attention in high-power RF applications due to its high power and current gain frequency, minimum SCEs, lower leakage current, and high drain current density *(Cui and Zeng, 2021, Chand et al., 2021*). The device performance has also been improved by introducing the AlN layer between the InAlN/GaN layer, which increases the conduction band's discontinuity and enhances the 2DEG concentration *(Shrestha et al., 2014*). Additionally, it reduces the alloy's scattering, which results in a considerable increase in the device's mobility.

Another major challenge with HEMT is the spilling of 2DEG from the GaN channel to the buffer layer, which reduces the mobility and reliability of the device *(Khan et al., 1992*). There are many techniques that have been reported to prevent the overflowing of 2DEG into the buffer layer, such as the double heterostructure HEMT method, in which a back-barrier layer is introduced between the channel and the buffer layer, as is discussed in **Chapter 1** *(Gu et al., 2019*). It is the simplest and most straightforward method for improving the confinement of heterojunction 2DEG and preventing an excess flow of carriers into the buffer layer. Several studies *(Chen et al., 2003, Lee et al., 2011, Meng et al., 2012*) have reported on the impacts of

the AlGaN back-barrier layers on HEMTs that have double heterojunction structures. To some extent, it can improve carrier confinement to some degree, but it also creates a parasitic channel at the junction between the AlGaN back barrier /GaN buffer. The researchers have also adapted another technique, which involves increasing the resistivity of the buffer layer by doping it with either iron (Fe) or carbon (C) acceptors *(Pampili and Parbrook, 2017*). On the other hand, these dopants cause the generation of deep-level acceptors in the layer, which results in a current collapse *(Uren et al., 2012*). Recently, polarization doping produced by grading the AlGaN layer has been regarded as a superior option. Because of the polarization-induced doping in the buffer, the potential can be bent upwardly convex. This increases the resistivity in the buffer layer without any intentional doping, which significantly reduces the buffer leakage current, improving the pinch-off voltage and microwave performance of the device.

Many experimental and theoretical papers have already been published for the different types of graded engineering. *Li et al., 2012* published experimental work on the polarization-induced pn junction. *Jena et al., 2002* shows the experimental work on polarization bulk doping. *Li et al., 2013* exhibit polarization-induced hole doping in which Al comp changes from 0.7 to 1. *Yao et al., 2015* used polarization doping for UV LEDs, and *Han et al., 2018* reported the polarization doping reduces SCEs. *Li et al., 2015* show the breakdown and current collapse characteristics of graded AlGaN buffer. Graded AlGaN buffers in AlGaN/GaN HEMTs can significantly reduce the buffer-related current collapse and buffer leakage current *(Inoue et al., 2008*).

GaN-based devices are normally on devices by nature. Despite the fact that these devices are often used in cascode package solutions or with specialized controllers in power semiconductor systems, the market requires enhancement mode (E-mode) or normally-off devices instead. In recent years, E-mode HEMTs and metal-oxide-semiconductor field-effect transistors (MIS-HEMTs) have undergone intensive research and development due to rising demand from various applications. For RF/microwave circuits, E-mode devices make it possible to eliminate the negative-polarity power supply, which simplifies the circuit and system architecture. Power switches achieved by E-mode devices offer highly desirable intrinsic fail-safe operation, making them ideal for use in power electronics. GaN devices operating in E-mode would improve overall circuit and system efficiency when used in high RF and new digital applications. Several methods have been proposed for obtaining E-mode devices; these include

thin barrier structure *(Endoh et al., 2004*), fluorine plasma treatment *(Su et al., 2014*), and p-GaN cap structure *(Hu et al., 2000*). The p-type GaN layer is grown on top of the AlGaN barrier, a gate metal is deposited and patterned, and the AlGaN barrier is recessed selectively to create a p-GaN HEMT. To achieve E-mode operation, the gate metal layer makes a Schottky or ohmic contact with the p-GaN layer, elevating the potential in the channel. Recessed-gate metal insulator HEMTs (recessed gate MISHEMTs) are another method of achieving E mode operation by (completely or partly) recessing the AlGaN barrier below the gate to interrupt the 2DEG and obtain normally-off operation *(Choi et al., 2014*). The recessed-gate MIS structure device is the most promising approach to fabricating the E-mode AlGaN/GaN power device due to its high breakdown voltage, threshold voltage and gate voltage fluctuation.

To outstretch the operating frequency of GaN HEMTs for mm-wave application. It is important to reduce the gate length of the device to the nanometer range. Many researchers have published their work on different gate geometry to enhance RF performance. Such as camel-shaped *(Khan et al., 2013*), T-shaped *(Murugapandiyan et al., 2017a*), and gamma-shaped *(Peroni et al., 2007*) gate structures. Among all these gate structures, the T-shaped gate geometry is appropriate to enhance the RF performance of the device. As the T-shaped structure decreases, the gate resistance and gate capacitance reduces by providing a larger gate area and lower foot length.

Hence, individual engineering approaches like as barrier, buffer, and gate design are insufficient to address the issues posed by HEMT. As a result of this, the primary objective of this chapter is to include all of the barrier, buffer, and gate engineering into a single HEMT. Thus, with an anticipation of the combined advantages of the InAlN barrier layer, polarization-doped buffer layer, and T-shaped gate geometry for improved device characteristics, E-mode T-gate InAlN/AlN HEMT with polarization-doped buffer is analyzed throughout the thesis. In this chapter, an InAlN barrier layer, polarization-doped buffer layer, and T-shaped gate structure has been integrated into HEMT to acquire an improved device DC and RF performance. These advancements have not only enhanced the transistor's operational efficiency but also opened up new possibilities for various applications in the field of electronics.

The following outline constitutes this chapter's structure: The first section of this chapter

provides an overview of the device construction, along with the structural parameters and computational models that were applied throughout the course of this study. The confirmation of the simulation setup is demonstrated in the second portion of the chapter, which details how the models used in the simulation setup were calibrated with the experimental data provided and how this was accomplished. In the following section of the chapter, the possibility of the suggested device's manufacturing will be discussed. The later part of the chapter discusses the results obtained through simulation. These results include the effect of gate and drain bias, effect of gate recessed depth, impact of high k gate dielectric; all of these factors have an impact on the electrical and RF performance of E-mode T-gate InAlN/AlN HEMTs with polarization doped buffers. The conclusion of the chapter is presented in the final part of the chapter's summary.

2.2 Device Structure

The two-dimensional view of the simulated device structure, which is an E-mode T-gate InAlN/AlN HEMT comprising of recessed gate engineered and polarization doped buffer engineered, is displayed in **Figure 2. l(a)**. **Table 2.1** contains a summary of the structural parameters of the device along with their respective values. The device is made up of a lattice-matched InAlN barrier layer, AlN spacer layer, which increases the conduction band discontinuity at AlN/GaN junction and enhances the 2DEG concentration, GaN channel layer,

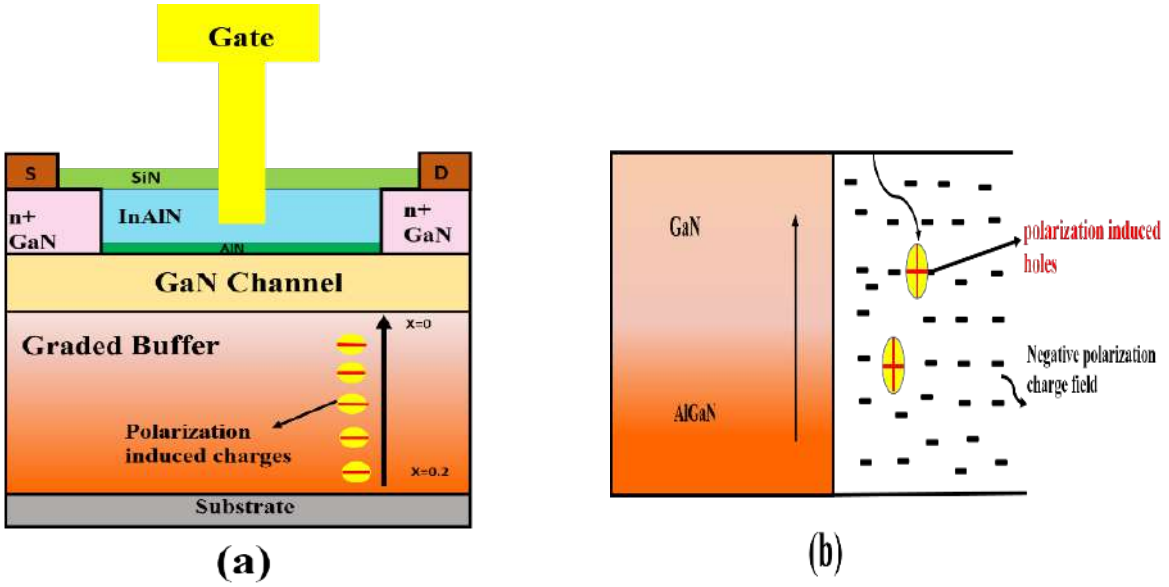

Fig. 2.1 (a) Schematic structure InAlN/AlN T-gate E-mode with polarization doped buffer (b) polarization induced doping *(Sharma and Chaujar, 2022)*.

and AlGaN buffer layer in which aluminum composition linearly changes from 0.2 to 0 along the (0001) direction. The T-shaped Schottky gate consists of a Pt/Au metal stack with a smaller footprint and a larger gate area. The T-shaped structure decreases the gate resistance and gate capacitance by providing a larger gate area and lower foot length *(Zhang et al., 2013*). The source and drain region doped with Si of order 10^{19} cm^{-3} to reduce the contact resistance *(Murugapandiyan et al., 2017b*). The SiN layer is used to passivate the device, which reduces the parasitic capacitance and enhances the device's frequency parameters *(Murugapandiyan et al., 2017b*). All simulations have been performed using the ATLAS device simulator *(Manual, 2016).* The physics of polarization-induced doping in the buffer is depicted in **Figure 2.l(b)**. The polarization charge discontinuity across the heterojunction formed the fixed polarization charges. When the Al composition changes from the AlGaN to GaN, a negative polarization charge field is induced over bulk, and the induced charge density is calculated by the divergence of the polarization field, which changes along the growth direction. Due to the charge neutrality, equivalent holes are induced by the negative polarization charge field. Hence bulk-free electrons are more deeply compensated by the high-density polarization-induced holes and significantly reduce the buffer leakage current.

TABLE 2.1

Values of Device Parameters *(Sharma and Chaujar, 2022*).

Parameters	Values
Buffer layer	1 μm
Channel layer	20 nm
Spacer layer	1 nm
Barrier layer	6 nm
Passivation layer	20 nm
Gate Length	10 nm
Gate Width	50 μm
Source /drain doping	1×10^{19} cm^{-3}
Gate to source length	400 nm
Gate to drain length	590 nm

2.3 Simulation Model and Calibration

During the simulation, the following models were used to simulate the device response: the hydrodynamic model, the Fermi-Dirac model, the low-field electron mobility model, the high-field mobility model, the Shockley–Read–Hall (SRH) model, and the polarization model *(Manual, 2010)*. The hydrodynamic model is the one that was used for carrier transport in this study. The typical drift-diffusion model of charge transport overlooks non-local transport phenomena such velocity overshoot, diffusion related with carrier temperature, and impact ionisation rate depending on carrier energy distributions. These phenomena can significantly influence the terminal properties of submicron devices. As a consequence of this, Atlas provides a hydrodynamic model of charge transport, which is an advantageous model to use when simulating deep submicron devices.

Electric fields are responsible for the acceleration of electrons and holes; however, the electrons and holes ultimately lose velocity due to the different scattering processes. Lattice oscillations, ions impurities, other carriers, surfaces, and various other material imperfections are all examples of scattering mechanisms. The low-field mobility model and the high-field mobility model have both been utilized in the course of this investigation into the various scattering mechanisms. The statement is known as ALBRCT.N and has referred to the low-field Albrecht Model. In the MOBILITY statement, the variable GANSAT.N is responsible for specifying the "high field mobility" model, which is a nitride-specific field-dependent mobility model. In order to investigate the electron capturing process that occurs at each trap level, Shockley–Read–Hall (SRH) recombination, which is also known as trap-assisted recombination, is employed. As mentioned in **Chapter 1**, GaN is a polar material that shows significant polarization effects. In order to take into account these kinds of impacts, the simulation makes use of the POLARIZATION model. In addition, the CALC.STRAIN statement is utilized in order to perform the calculation of the piezoelectric polarization. Since $In_{0.17}Al_{0.83}N$ has a lattice that is matched to GaN, and because the graded back barrier layer is believed to have complete lattice relaxation, the total polarization in the device is spontaneous polarization and does not include any piezoelectric polarization. It is possible that a space polarization-induced charge could be produced by a gradient of polarization in the $Al_xGa_{1-x}N$ back-barrier, provided that the polarization gradient changes along the growing direction. When the electric field across an insulator is sufficiently strong, it has the potential to induce the tunneling of electrons

from the fermi level of a semiconductor (or metal) into the conduction band of the insulator. This procedure is highly dependent on the applied electric field, but it is not affected by the temperature of the surrounding environment. In the simulation, the FN tunneling model is called upon to be used to account for such effects. It is necessary to specify the FNORD parameter of the model statement in order to facilitate Fowler-Nordheim tunneling *(Lenzlinger et al., 1969*).

In order to simulate the device structure, a well-calibrated TCAD setup was utilized. This was done in order to correlate the simulation models with the experimental findings that have already been published *(Han et al., 2016*). **Figure 2.2** demonstrates that the calibration of simulation models with experimental data for transfer characteristics reveals close proximity, which justifies the choice of model parameters considered in the simulation setup.

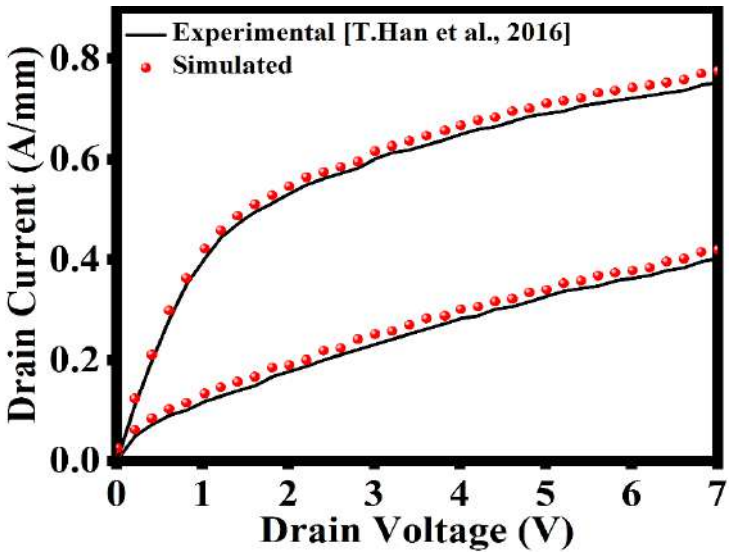

Fig. 2.2 Comparative analysis of experimental *(T. Han et al., 2016)* and simulation result with 70 nm T-gate length HEMT at V_{gs} = -3V, -2V.

2.4 Fabrication Process Flow

The process of fabricating the T-gate E-mode HEMT with polarized doped buffer is depicted in **Figure 2.3**. The molecular beam epitaxy (MBE) technique is used to produce the epitaxial stack (InAlN/AlN/GaN/AlGaN) on top of the SiC substrate *(Jena et al., 2002)*. The ohmic source/drain n++ GaN regions are regrown by MBE with a SiO_2 growth mask *(Guo et al., 2012)*. First, a SiO_2/SiNx mask was made using plasma-enhanced chemical vapour deposition (PECVD) and then patterned by reactive ion etching. After that, the ohmic region of the

InAlN/AlN/GaN layer was etched down in the ohmic region, followed by an undercut etch of the SiO_2 regrowth mask. A GaN: Si (> 1×10^{19} cm^{-3}) was regrown by MBE, and the specific growth conditions were described by *Guo et al., 2011*. After ohmic regrowth, non-alloyed ohmic contacts were formed by the deposition of a Mo/Au-based stack. The device was finally passivated by a SiN layer using PECVD *(Micovic et al., 2017)*. The fabrication of the T-gate consists following steps. The electron beam lithography is used for gate definition, gate foot is partially recessed into the barrier layer by dry etching, then the deposition of gate metal by an electron beam evaporator (EBE) *(Micovic et al., 2017)*.

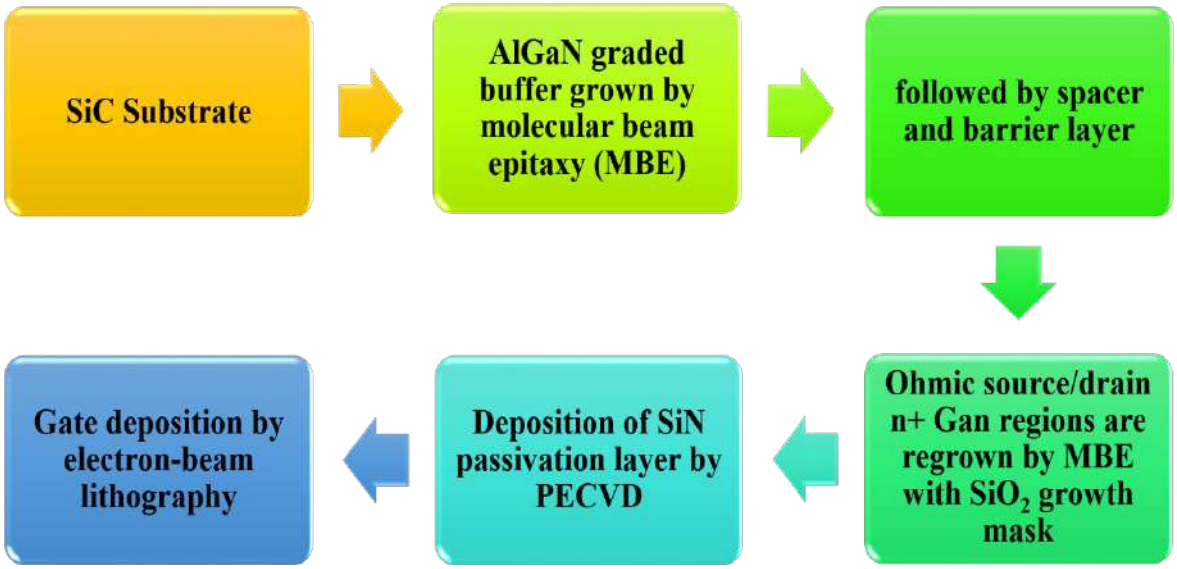

Fig. 2.3 fabrication process flow of proposed structure *(Sharma and Chaujar, 2022)*.

2.5 Results and Discussion

2.5.1 Band Diagram

Figure 2.4(a) illustrates a band energy diagram for the T-gate E-mode HEMT with a polarization-doped buffer. The device has a buffer with an AlGaN-graded composition, which generates a negative space polarization charge based on Equations 2.1 and 2.2, which increases the potential of the buffer layer towards the backside *(Inoue et al., 2008)*.

$$P_{SP}(Al_xGa_{1-x}N) = x\,P_{SP.}\,(AlN) + (1-x)\,P_{SP.}\,(GaN) \qquad (2.1)$$

$$\rho P = -\nabla . P = -\frac{\partial P}{\partial Z} \tag{2.2}$$

In addition to this, the bandgap of the polarization-graded AlGaN buffer continuously widens as the amount of Al content in the buffer increases. As a direct consequence of this, the buffer's conduction band shifts towards the upward direction, making the buffer layer potentially upwardly convex and effectively confined the 2DEG in the channel. Moreover, the discontinuity in the bandgap of heterostructure forms the quantum well at the AlN/GaN interface. The InAlN/GaN heterojunction has a large band discontinuity and strong polarization effect, allowing the large 2DEG formation in the device. The 2DEG concentration can be calculated using Equation 2.3 *(Qin et al., 2018*).

$$n_s = \frac{1}{(d_{InAlN}+d_{AlN})} \times \left\{ \frac{\sigma_{InAlN} \times d_{InAlN}}{e} + \frac{\sigma_{AlN} \times d_{AlN}}{e} - \frac{\varepsilon(x)\varepsilon_0}{e^2} \times \left\{ e\emptyset_b(x) + E_F[x, n_s(x)] - \Delta E_{c,AlN/GaN} + \Delta E_{c,InAlN/GaN}(x) \right\} \right\} \tag{2.3}$$

where $\sigma_{InAlN}, \sigma_{AlN}, d_{InAlN}, d_{AlN}, m_{InAlN}, m_{AlN}, m_{GaN}, \varepsilon_{InAlN}, \varepsilon_{AlN}, \chi_{InAlN}, \chi_{AlN}, \chi_{InN}$ are the induced polarization charge density, thickness, effective mass, dielectric constant, and electron affinity of the InAlN, AlN layer. $\emptyset_b(x), E_F$ is the schottky barrier height and fermi energy level. $\Delta E_{c,AlN/GaN}$ and $\Delta E_{c,InAlN/GaN}(x)$ is the conduction band offset. The values of various parameters are depicted in **Table 2.2**. The total charge density in the channel region is 2.8 × 10^{13} cm^{-2} obtained as depicted in **Figure 2.4(b)**.

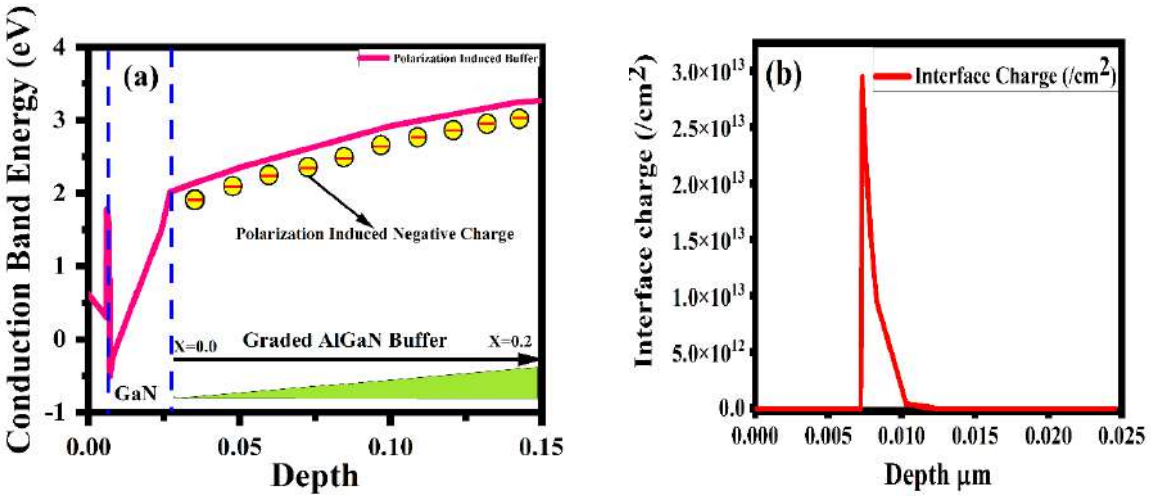

Fig. 2.4 (a) Conduction band diagram (b) Total charge density in the channel of the T-gate E-mode HEMT with polarization doped buffer *(Sharma and Chaujar, 2022*).

TABLE 2.2

Values of Parameters Used in Simulation *(Sharma and Chaujar, 2022)*.

Parameters	Values
σ_{InAlN}	-4.189×10^{13} Cm^{-2}
σ_{GaN}	-1.84×10^{13} Cm^{-2}
$\emptyset_s$	2.8 eV
$\Delta E_{c,InAlN/GaN}$	0.8eV
$\Delta E_{c,AlN/GaN}$	1.7 eV
m_{InAlN}	0.25 m_o
m_{AlN}	0.32 m_o
m_{GaN}	0.20 m_o
ε_{InAlN}	10.1
ε_{AlN}	9.5
χ_{InAlN}	2.5 eV
χ_{AlN}	2.1 eV
χ_{InN}	4.7 eV

2.5.2 DC Characteristics

This subsection investigates the effect of the gate and drain bias on the DC and analog performance of the proposed device (T-gate E-mode HEMT with polarized doped buffer). **Figure 2.5(a)** depicts the characteristics of the drain current for the proposed device with the gate voltage (V_{gs}) at various drain bias (V_{ds}) voltages (1V, 3V). It is observed that for V_{ds}= 1V, drain current starts increasing linearly at V_{gs}= 1V and saturates at V_{gs}= 2V. In addition, by increasing the V_{ds} to 3V, the drain current increases along with the gate bias, and a greater drain current density of 2.8 A/mm is obtained when the V_{gs} value is reached 3V. The reason

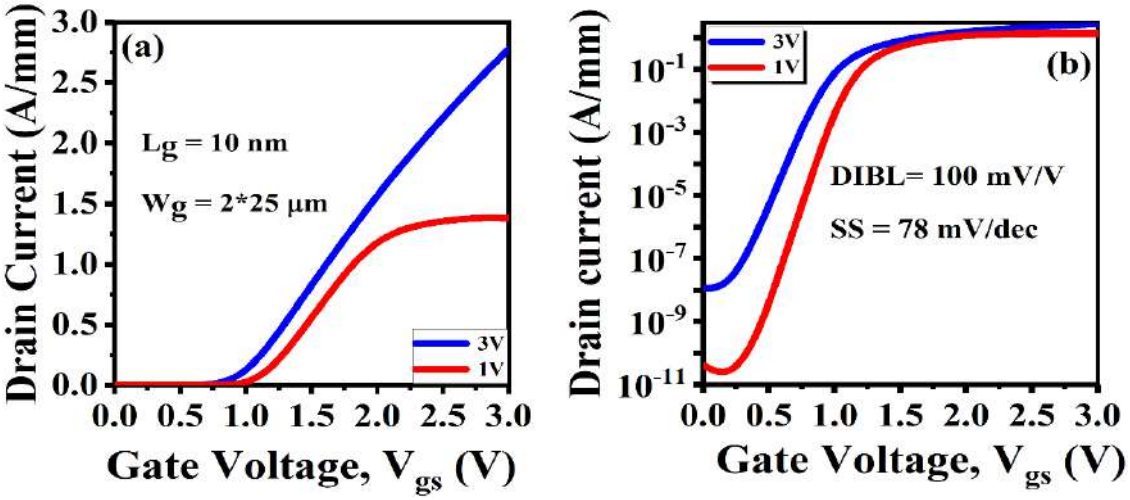

Fig. 2.5 (a) Linear scale (b) Log scale drain current density of the 10 nm gate length T-gate E-mode HEMT with polarization doped buffer at V_{ds} = 1V and 3V *(Sharma and Chaujar, 2022)*.

why drain bias causes a rise in drain current is that the velocity of electrons in the channel is proportionate to the applied electric field, so the current will grow as the field strength does (see **Chapter 1's** Equation 1.9 for the relationship between drain current and electron velocity). The ultra-scaled devices have one significant problem, and that is the short channel effect, which is especially problematic in the 10-nanometer gate length. The DIBL and subthreshold swing are the most pronounced SCEs, and for better device performance, these effects should be low. DIBL investigates the change of threshold voltage with the drain voltage. The potential barrier between the source and drain in long gate devices is typically governed by the gate bias. However, as the gate length is aggressively decreased, the potential barrier will also be reduced by the positive drain-source voltage. As a consequence of this, the DIBL effect is causing a decrement in the threshold voltage (V_{th}) value in response to an increase in V_{ds}. **Figure 2.5(b)** displays the transfer characteristics as a logarithmic curve for V_{ds}= 1 and 3 V. It was found that the proposed device has a DIBL that is 100 mV/V. A transistor's subthreshold swing measures how quickly it can be switched on or off. As a function of gate bias, it is defined by the inverse slope of the exponential drain current in the subthreshold region and calculated as

$$SS = \left(\frac{\partial(\log I_{ds})}{\partial V_{gs}}\right)^{-1} \tag{2.4}$$

In an ideal world, excellent transistors would turn off when the threshold voltage was reached. However, this is not possible in practice because short-channel effects can have a significant impact. The SS value of the proposed device was determined to be 78 mV/dec. Based on these findings, the polarization-doped buffer can exert effective control over the SCEs and significantly improve the modulation efficiency of the gate. The transconductance of a transistor reflects how much a transistor can produce current by applying input voltage across its gate. It tells you how much strong it is to convert a small amount of voltage into a desirable current. It is defined as the derivative of drain current with gate bias at constant drain voltage. The transconductance characteristics of the proposed device are depicted in **Figure 2.6(a)**. It has been observed that on increasing the gate voltage, transconductance also increases, and a higher peak of the transconductance of 1.55 S/mm is obtained at V_{gs} = 1.4 V and V_{ds} = 3 V after that, a downward swing is observed at higher gate bias. This reduction in transconductance at higher gate bias is due to the saturation of drain current at higher gate voltage, as shown in

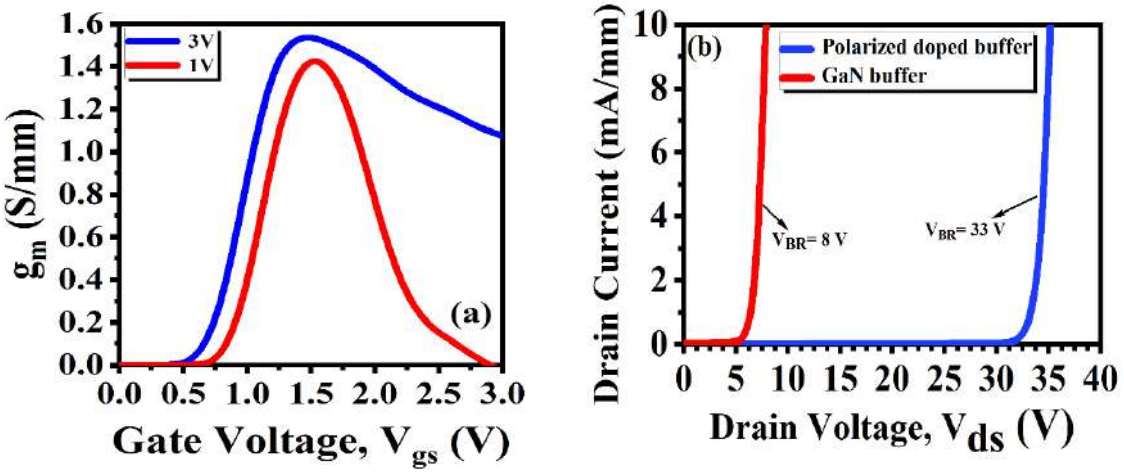

Fig. 2.6 (a) Transconductance of the 10 nm gate length T-gate E-mode HEMT with polarization doped buffer at V_{ds} = 1V and 3V (b) Breakdown voltage for both the devices *(Sharma and Chaujar, 2022)*.

Figure 2.5(a). **Figure 2.6(b)** exhibits the breakdown characteristics of the proposed T-gate E-mode HEMT with a polarized doped buffer. The higher breakdown voltage, i.e., 33V, was obtained for the proposed 10 nm T-gate InAlN/AlN HEMT with a polarized doped buffer, which is 5 times higher than the conventional InAlN/AlN GaN buffer HEMT. The enhancement of the breakdown voltage in a proposed device is because of the polarization-induced doping in the buffer layer, which reduces the buffer leakage current.

2.5.3 Microwave Characteristics

The microwave properties of the proposed device are investigated in this section through S-parameter simulation. These types of analysis are called small-signal analysis, as small input signals are required for the characterization. The parameters investigation includes cut off frequency (f_T), max oscillation frequency (f_{max}), max. stable gain (MSG), and Mason's unilateral gain (MUG). All these parameters are directly calculated from the S parameters by using the following equations *(Ramkumar et al., 2021)*.

$$h_{21} = \left|\frac{-2S_{21}}{(1-S_{11})\times(2-S_{22})-S_{12}\times S_{21}}\right| \tag{2.5}$$

$$\text{MUG} = \left(\frac{|S_{21}|^2}{(1-|S_{11}|^2)\times(1-|S_{22}|^2)}\right) \tag{2.6}$$

$$MSG = \frac{|S_{21}|^2}{|S_{12}|^2} \times \left(K \pm \sqrt{(K^2-1)}\right) \quad (2.7)$$

$$K = \frac{1 - |S_{21}|^2 - |S_{12}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 \times |S_{12}|^2 \times |S_{12}|^2} \quad (2.8)$$

f_T defines as the frequency at which forward current gain (h_{21}) becomes unity. Mason's unilateral gain (MUG) is an important figure of merit used to investigate the max oscillation frequency. MUG defines as the power gain of two pot network where output to input feedback is zero. **Figure 2.7(a)** and **Figure 2.7(b)** exhibit the small-signal characteristics of the proposed device at V_{gs}=1.4V and V_{ds}= 3V. At the point when the current gain and the unilateral gain both equal 0 dB, the f_T and f_{max} values are calculated. The f_T and f_{max} values 583 GHz and 840 GHz are recorded for the proposed device. A microwave transistor has the capacity to amplify or sustain the oscillation in the circuit. Whether the transistor in the circuit oscillates or not its depends upon the input and output load impedance. The choice of stability of the device is important while designing the amplifier otherwise amplifier will turn to an oscillator. RF transistors whose operating frequency is greater than the critical frequency(f_k) are unconditionally stable, and if the operating frequency is lower than the f_k, the transistor is conditionally stable. The rollett stability factor (K>1) is the sufficient condition for the device's stability *(Lenka et al., 2013)*. The K value indicates whether the device oscillates or not. When the K>1, it shows the conjugate matching of input and output loads. This is the standard criteria of stability, and the circuit is unconditionally stable. If the K<1, then the circuit is conditionally

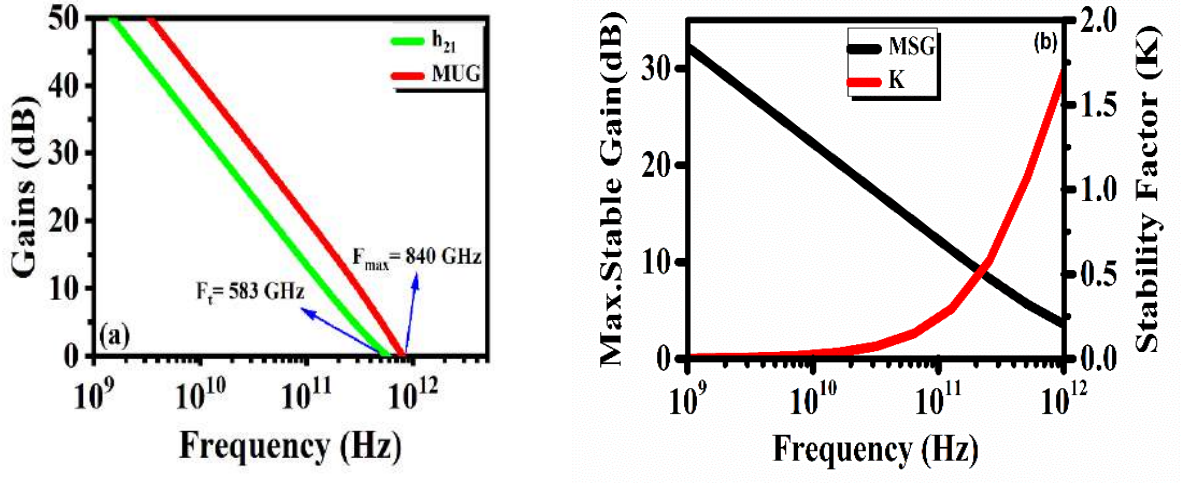

Fig. 2.7 (a) Current gain and unilateral gain (b) Rollett stability factor and max. stable gain of the T-gate E-mode HEMT with polarization doped buffer *(Sharma and Chaujar, 2022)*.

stable. Once the stability condition is satisfied, the maximum stable gain is calculated using the stability factor and S parameters, as shown in Equation 2.8. The rollett stability factor and MSG are plotted in **Figure 2.7(b)**. It has been observed that the device is conditionally stable in the cutoff frequency region and behaves as a stable amplifier.

2.5.4 Impact of Recessed Gate Depth

In this subsection, the effect of recessed depth (R_d) on the DC and RF performance of the proposed device is investigated. The drain current density of variable recessed depth (R_d) is depicted in **Figure 2.8(a).** It has been observed that on increasing the recessed depth from 2 nm to 5 nm, the threshold voltage is shifted toward the positive side with a significant decline in drain current. This is due to the fact that when the gate is recessed into the barrier then the gap between the gate and the channel gets smaller, which results in an increase in the controllability of the gate on the channel. **Figure 2.8(b)** shows the high on/off ratio 10^7 for the recessed depth 5 nm at V_{ds} = 3V. **Figure 2.9(a)** shows the transconductance characteristics of variable gate recessed depth. It has been observed that transconductance increases by increasing the recessed depth from 2 nm to 5 nm. This increment is because gate controllability over a channel increases by increasing the recessed depth, enhancing the transconductance, and reducing the short channel effect. **Figure**.**2.9(b)** shows the graph of breakdown voltage with gate recessed depth. A higher breakdown voltage has been observed for the 5 nm recessed depth.

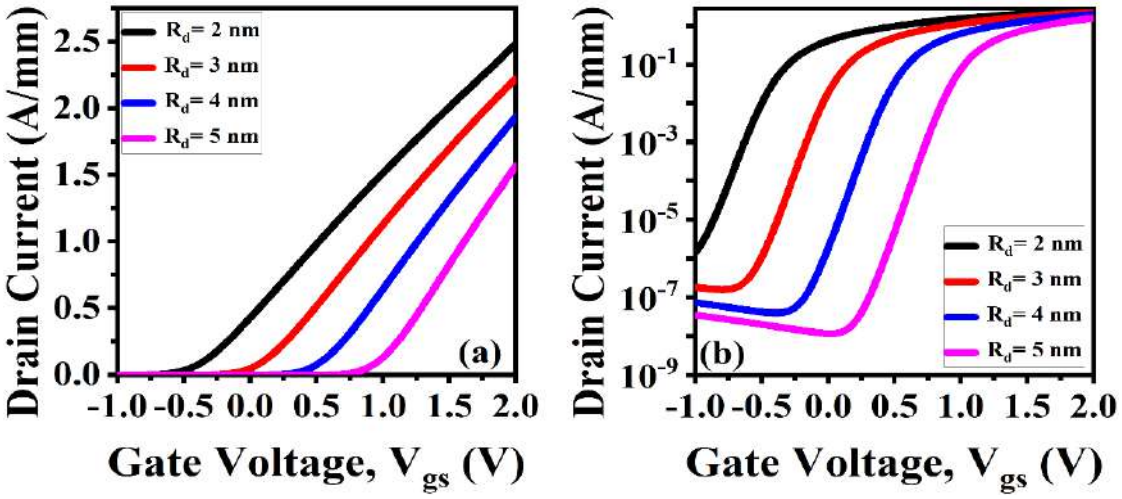

Fig. 2.8 (a) Linear scale (b) Log scale drain current density for variable recessed depth (R_d) of the T-gate E-mode HEMT with polarization doped buffer *(Sharma and Chaujar, 2022*).

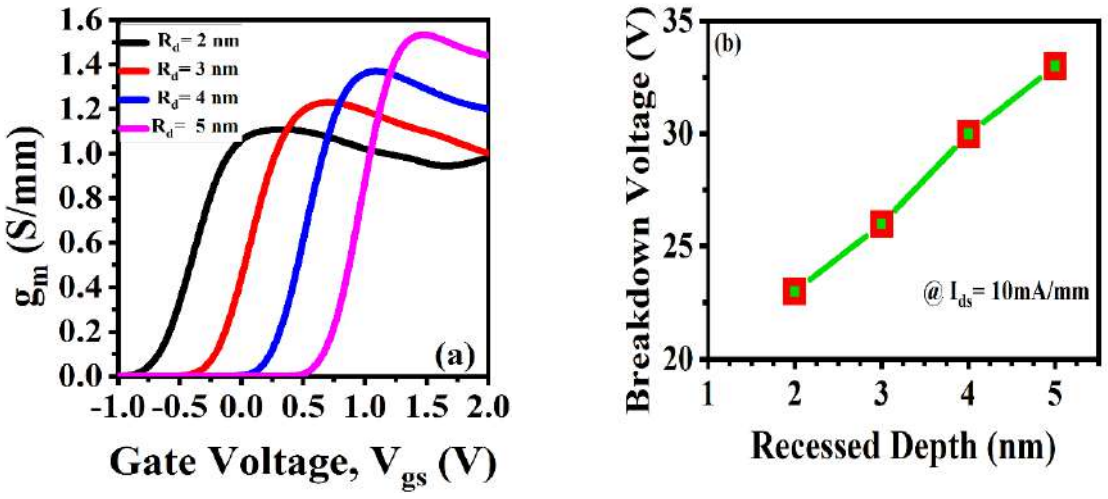

Fig. 2.9 (a) Transconductance (b) Breakdown voltage for variable recessed depth of the T-gate E-mode HEMT with polarization doped buffer *(Sharma and Chaujar, 2022)*.

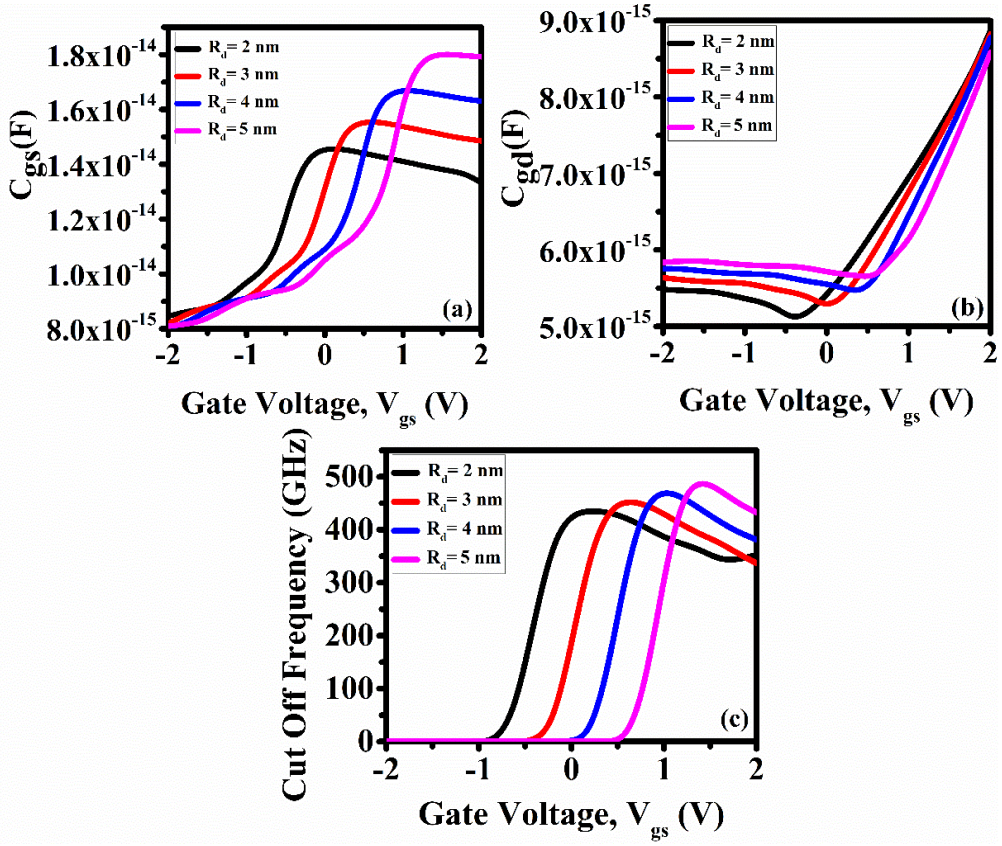

Fig. 2.10 (a) Gate to source (b) Gate to drain capacitance (c) Cut off frequency of the T-gate E-mode HEMT with polarization doped buffer for variable recessed depth *(Sharma and Chaujar, 2022)*.

The impact of gate recessed depth on parasitic capacitance and the cutoff frequency is shown in **Figure 2.10(a-c)**. The plot of the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) with gate bias is shown in **Figure 2.10(a, b)**. For better RF performance,

these parasitic capacitances should be low. At lower gate voltage, there is a slow increment in C_{gs} and C_{gd}, but at higher gate bias, there is a quick increment in C_{gs} and C_{gd} due to the enhancement of the lateral electric field, which increases the carrier movement from the drain to the source side. For the gate recessed depth of 5 nm, a higher value of C_{gs} and a lower value of C_{gd} are observed at higher gate bias. **Figure 2.10(c)** exhibits the plot of cutoff frequency with gate bias. The mathematical formula of cutoff frequency is expressed by Equation 2.9.

$$f_T \approx g_m / 2\pi(C_{gs}+C_{gd}) \tag{2.9}$$

It is seen that f_T depends upon transconductance and parasitic capacitance. The higher value of parasitic capacitance for recessed depth 5 nm detroit the f_T, but the higher value of g_m significantly enhanced the f_T.

2.5.5 Impact of Gate Oxide

This subsection investigates the impact of high k gate dielectric on the proposed device. Many researchers have described the usage of metal-oxide-semiconductor (MOS) structures to minimize gate leakage current and acquire considerable pinch-off characteristics. SiO_2 *(Brown et al., 2014)*, ZnO *(Lee et al., 2010)*, Al_2O_3 *(Liu et al., 2013)*, and ferroelectric material *(Qi et al., 2021)* have also been employed as gate dielectrics in nitride-HEMTs to create a more effective

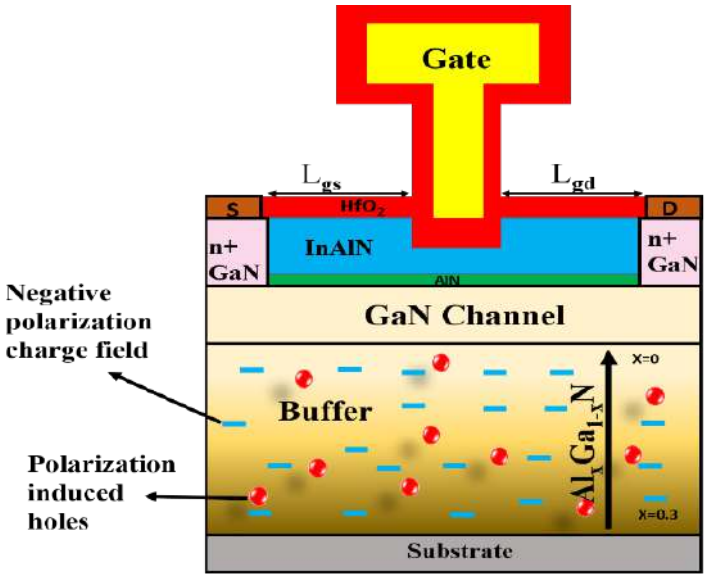

Fig. 2.11 T-gate HEMT with polarization doped buffer and high k dielectric (PD-MOS-HEMT) *(Sharma et al., 2023)*.

MOS structure. Recently, high-k materials such as HfO_2 emerged as potential gate-insulating material that enhances the device's stability and transport performance *(Yue et al., 2008)*. In this section, a 70 nm T-gate HEMT with polarization doped buffer is used, passivated by the HfO_2 layer. In place of the recessed gate in the barrier layer, a 5 nm HfO_2 layer is recessed in the barrier, as shown in **Figure 2.11**.

Figure 2.12 depict the drain current characteristics for four different structures on the same dimensions: conventional T-gate HEMT (GaN-HEMT), T-gate HEMT with high k dielectric (MOS-HEMT), T-gate HEMT with polarization doped buffer (PD-HEMT), and T-gate HEMT with polarization doped buffer and high k dielectric (PD-MOS-HEMT). It has been observed that the insertion of HfO_2 below the gate significantly shifts the threshold voltage toward the positive side, as shown in **Figure 2.12(a)**. The polarization-induced doping in the buffer region reduced the off-state current (10^{-13}), as shown in **Figure 2.12(b)**. The polarization doping in the buffer layer acts as a blocking layer that hinders the 2DEG in the buffer region, effectively suppressed the buffer leakage current. The transconductance curve for all four devices is shown in **Figure 2.13**. It can be observed that the insertion of a high k gate dielectric significantly enhances the transconductance by about 170% as compared to the conventional HEMT due to the high gate leakage blocking ability. In comparison, a 51% enhancement in transconductance is observed for PD-HEMT.

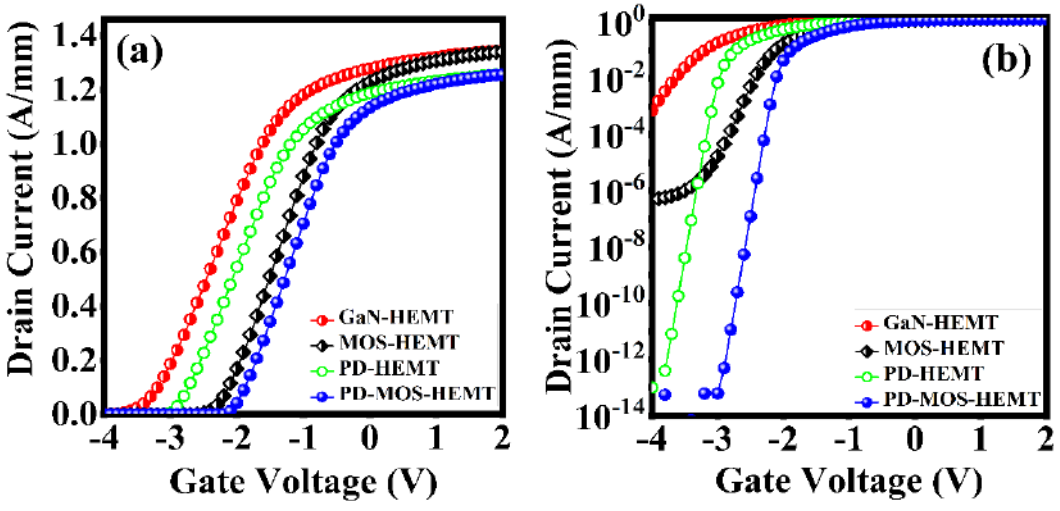

Fig. 2.12 (a) Linear scale (b) Log scale drain current density for 70 nm gate length conventional T-gate HEMT (GaN-HEMT), T-gate HEMT with high k dielectric (MOS-HEMT), T-gate HEMT with polarization doped buffer (PD-HEMT), and T-gate HEMT with polarization doped buffer and high k dielectric (PD-MOS-HEMT) *(Sharma et al., 2023)*.

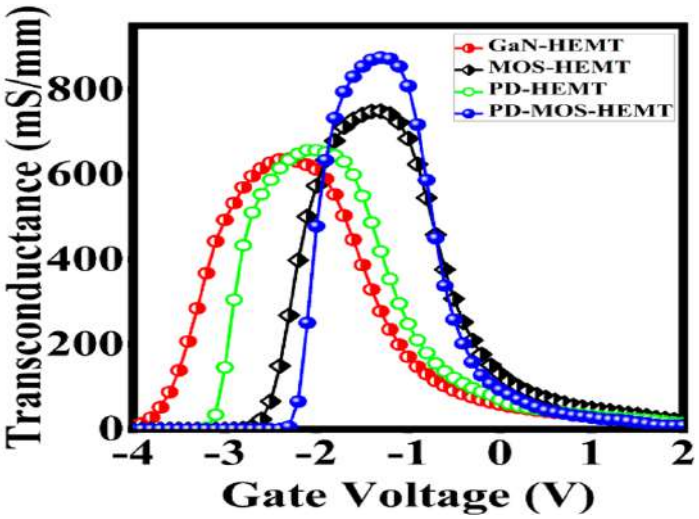

Fig. 2.13 Comparative analysis of transconductance for GaN-HEMT, MOS-HEMT, PD-HEMT, and PD-MOS-HEMT. *(Sharma et al., 2023*)

Hence the collective engineering of high k gate dielectric and polarization induces doping in the buffer region in the proposed structure (PD-MOS-HEMT), significantly shifts the threshold voltage positive side, reduces off current (10^{-14}), and enhances the transconductance (900 mS/mm) about 215%. The comparative analysis of 10 nm and 70 nm gate length PD-MOS-HEMT is exhibited in **Table 2.3**. It has been observed that on reducing the gate length to 10nm, the switching ratio reduces to 10^5, a negative shift in threshold voltage and a 50% reduction in transconductance is observed. Therefore, the T-gate PD-MOS-HEMT demonstrates outstanding performance when operated with a gate length of 70 nm. However, it is worth noting that the PD-MOS-HEMT primarily operates in D-mode. On the other hand, devices operating in E-mode offer a highly desirable intrinsic fail-safe operation, making them exceptionally well-suited for power electronics applications. Considering these advantages, our thesis focuses on the development and analysis of recessed gate E-mode T-gate HEMTs with a polarized doped buffer.

TABLE 2.3

Comparative analysis of T-gate PD-MOS-HEMT for different gate length

Parameter	10 nm T-gate PD-MOS-HEMT	70 nm T-gate PD-MOS-HEMT
Switching ratio (I_{on}/I_{off})	10^5	10^{14}
Threshold voltage (V_{th})	-3.9 V	-2.3 V
Transconductance (g_m)	0.061	0.074

2.6 Summary

In this chapter, a T-gate E-mode HEMT with a polarization-doped buffer has been proposed, and a detailed DC and RF performance analysis has been developed. The results demonstrate that the utilization of recessed gate engineering and polarization-induced doped buffer engineering yields substantial improvements across various performance metrics. Notably, these techniques achieve a remarkable on/off ratio of 10^9, a significant reduction in subthreshold swing to 78 mV/dec, and a DIBL of just 100 mV/V. Furthermore, they increase the breakdown voltage to 33 V, improve the cutoff frequency to 583 GHz, and maximize the oscillation frequency to 840 GHz. Moreover, the use of lattice-matched InAlN barrier layer and AlN spacer layer enhances the electron mobility (1250 cm^2/Vs) and 2DEG density (2.8×10^{13} cm^{-2}) due to which higher drain current density has been achieved (2.8 A/mm). Additionally, the impact of gate recessed depth (R_d) on DC and RF performance is also investigated. It has been observed that on increasing the gate recessed depth from 2 nm to 5 nm, a positive shift in threshold voltage (0.8V), lower off current (10^{-8}), and higher transconductance (1.55 S/mm) is achieved.

Moreover, a high-k gate oxide engineering approach has been employed, wherein a particular segment of the recessed gate is substituted with a high-k dielectric material. This strategic implementation of the high-k dielectric significantly enhances the interfacial and transport characteristics of the device while effectively reducing the gate leakage current. However, it has been observed that implanting the gate oxide alone does not enable E-mode operation. Therefore, gate-recessed engineered T-gate E-mode HEMT with polarization doped buffer is the superior choice for achieving E-mode operation and a potential candidate for high-power millimeter-wave applications.

The downscaling of the device has a notable impact on its DC and RF performance characteristics. Consequently, it becomes crucial to carefully determine the dimensions of the T-shaped gate structure to ensure optimal device operation. In light of this, the next chapter will conduct an in-depth investigation of the influence exerted by the T-gate shape on both the DC and RF performance of the device.

2.7 References

AMBACHER, O., FOUTZ, B., SMART, J., SHEALY, J., WEIMANN, N., CHU, K., MURPHY, M., SIERAKOWSKI, A., SCHA, W. and EASTMAN, L.2000. Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped Al-GaN/GaN heterostructures. *Journal of Applied Physics*,87,334-344.

BROWN, R., MACFARLANE, D., AL-KHALIDI, A., LI, X., TERNENT, G., ZHOU, H., THAYNA, I. WASIGE, E.2014. A Sub-Critical Barrier Thickness Normally-Off AlGaN/GaN MOS-HEMT. *IEEE Electron Device Letters*,35,906-908.

CHAND, N., SWAIN, S.K., BISWAL, S.M., SARKAR, A. and ADAK, S.2021. Comparative study on Analog & RF Parameter of InAlN/AlN/GaN Normally off HEMTs with and without AlGaN Back Barrier. *Devices for Integrated Circuit (DevIC)*,616–620.

CHEN, C. Q., ZHANG, J. P., ADIVARAHAN, V., KOUDYMOV, A., FATIMA, H., SIMIN, G., YANG, J. and ASIF KHAN, M.2003. AlGaN/GaN/AlGaN double heterostructure for high-power III-N field-effect transistors. *Appl. Phys. Lett.*, 82, 4593-4595.

CHOI, W., SEOK, O., RYU, H., CHA, H.Y. and SEO, K.S.2014. High-Voltage and Low-Leakage-Current Gate Recessed Normally-Off GaN MIS-HEMTs With Dual Gate Insulator Employing PEALD- SiN /RF-Sputtered- HfO2.*Electron Device Letters, IEEE,*35,175-177.

CUI, P. and ZENG, Y.2021. Electrical properties of 90-nm InAlN/GaN HEMT on a silicon substrate. *Phys. E Low-Dimensional Syst. Nanostructures*,134,114821.

ENDOH, A., YAMASHITA, Y., IKEDA, K., HIGASHIWAKI, M., HIKOSAKA, K., MATSUI, T., HIYAMIZU, S. and MIMURA, T.2004.Non-Recessed-Gate Enhancement-Mode AlGaN/GaN High Electron Mobility Transistors with High RF Performance.*Jpn. J. Appl. Phys.,*43, 2255.

GU, Y., CHANG, D., SUN, H., ZHAO, J., YANG, G., DAI, Z., and DING, Y.2019. Theoretical Study of InAlN/GaN High Electron Mobility Transistor (HEMT) with a Polarization-Graded AlGaN Back-Barrier Layer. *Electronics*,8,885.

GUO, J., CAO, Y., LIAN, C., ZIMMERMANN, T., LI, G., VERMA, J., GAO, X., GUO, S., SAUNIER,

P., JENA, D., and XING, H.2011. Metal-face InAlN/AlN/GaN high electron mobility transistors with regrown ohmic contacts by molec-ular beam epitaxy. *Phys. Stat. Sol. (A)*,208,1617–1619.

GUO, J., LI, G., FARIA, F., CAO, Y., WANG, R., VERMA, J., GAO, X., GUO, S., BEAM, E., KETTERSON, A., SCHUETTE, M., SAUNIER, P., WISTEY, M., JENA, D. and XING, J. 2012. MBE-regrown ohmic in InAlN HEMTs with a regrowth interface resistance of 0.05 Ωmm. *IEEE Electron Device Lett.*,33,525–527.

HAN, T., DUN, S., LU, Y., GU, G., SONG, X., WANG, Y., XU, P. and FENG, Z.2016. 70-nm-gated InAlN/GaN HEMTs grown on SiC substrate with fT/fmax > 160 GHz. *J. Semicond*.,37,4–8.

HAN, T., ZHAO, H., PENG, X. and LI, Y.2018. Control of short-channel effects in InAlN/GaN high-electron-mobility transistors using graded AlGaN buffer.*Superlattices Microstruct.*,116,207–214.

HU, X., SIMIN, G.,YANG, J., ASIF KHAN, M., GASKA, R. and SHUR, M.S.2000. Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate.*Electronics Letters*,36,753-754.

INOUE, T., NAKAYAMA, T., ANDO, Y., KOSAKI, M., MIWA, H., HIRATA, K., UEMURA, T. and MIYAMOTO, H.2008. Polarization engineering on buffer layer in GaN-based heterojunction FETs. *IEEE Trans. Electron. Dev.*,55,483-488.

JENA, D., HEIKMAN, S., GREEN, D., ILAN, B., COFFIE, R., XING, H.G.,KELLER, S., DENBAARS, S., SPECK, J. AND MISHRA, U. K.2002. Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys. *Appl Phys. Lett.*,81,4395–4397.

KHALAF, I., TAI, H.Y., PROPHET, E., BURNHAM, S.D., WONG, J.C., REGAN, D., FUNG, H.H. and TANG, Y.2017. GaN DHFETs Having 48% Power Added Efficiency and 57% Drain Efficiency at V-Band. *IEEE Electron Device Lett.,*38,1708–1711.

KHAN, M.A., HEO, J.W., KIM, Y.J., PARK, H.C., PARK, H.M., KIM, H.S. and MUN, J.K. 2013.Effects of a recessed camel-gate head structure on normally-off ALGaN/GaN HEMTs.*Journal of the Korean Physical Society*,62,787-793.

KHAN, M.A., KUZNIA, J.N., HOVE, J.M., PAN, N., and CARTER, J. 1992. Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-AlxGa1-xN heterojunctions. *Appl. Phys. Lett.*,60,3027–3029.

KUZMIK, J.2001. Power electronics on InAlN/(In)GaN: Prospect for a record performance. *IEEE Electron Device Letters*,22,510-512.

LEE, C.T., CHIOU, Y.L. and LEE, C.S. 2010. AlGaN/GaN MOS-HEMTs With Gate ZnO Dielectric Layer. *IEEE Electron Device Letters*,31,1220-1223.

LEE, D.S.,GAO, X., GUO, S., and PALACIOS, T.2011. InAlN/GaN HEMTs with AlGaN back barriers. *IEEE Electron Devcies Lett.*,32, 617–619.

LENKA, T.R., DASH, G.N. and PANDA, A.K. 2013. RF and microwave characteristics of a 10 nm thick InGaN-channel gate recessed HEMT. *J. Semicond.*,34,114003.

LENZLINGER, M. and SNOW, E.H.1969. Fowler-Nordheim Tunneling into Thermally Grown SiO_2. *J. Applied Physics*, 40,278-283.

LI, C., LI, Z., PENG, D., NI, J., PAN, L., ZHANG, D., DONG, X. AND KONG, Y.2015. Improvement of breakdown and current collapse characteristics of GaN HEMT with a polarization-graded AlGaN buffer.*Semicond. Sci. Technol.*,30,035007.

LI, S., WARE, M., WU, J.,MINOR, J., WANG, Z., WU, Z.,JIANG, Y. and SALAMO, G.J.2012. Polarization induced pn-junction without dopant in graded AlGaN coherently strained on GaN.*Appl. Phys. Lett.*,101,122103.

LI, S., ZHANG, T., WU, J., YANG, Y., WANG, Z., WU, Z., CHEN, Z. AND JIANG, Y.2013. Polarization induced hole doping in graded AlxGa 1-xN ($x = 0.7 \sim 1$) layer grown by molecular beam epitaxy.*Appl. Phys. Lett.*,102,1–4.

LIU, H., CHOU, B., HSU, W., LEE, C., SHEU, J. and HO, C. 2013. Enhanced AlGaN/GaN MOS-HEMT Performance by Using Hydrogen Peroxide Oxidation Technique. *IEEE Transactions on Electron Devices*,60,213-220.

MANUAL, A.U.S. 2016. *Silvaco . Santa Clara, CA*.

MENG, F., ZHANG, J., ZHOU, H., MA, J., XUE, J., DANG, L., ZHANG, L., LU, M., AI, S., LI, X., and HAO, Y.2012. Transport characteristics of AlGaN/GaN/AlGaN double heterostructures with high electron mobility. *J. Appl. Phys.*,112, 023707.

MICOVIC, M., BROWN, D.F., KURDOGHLIAN, A., SANTOS, D., GRABAR, B., MAGADIA, J., KHALAF, I., TAI, H., PROPHET, E.M., BURNHAM, S.D., WONG, J.C., REGAN, D., FUNG, H., and TANG, Y. 2017. GaN DHFETs Having 48% Power Added Efficiency and 57% Drain Efficiency at V -Band. *IEEE Electron Device Letters, 38*, 1708-1711.

MISHRA, U. K., PARIKH, P.& WU, Y. F.2002. AlGaN/GaN HEMTs - An overview of device operation and applications. *Proc. IEEE,* 90, 1022–1031.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J.2017a. 30 nm T-gate enhancement-mode InAlN/AlN/GaN HEMT on SiC substrates for future high power RF applications.*Journal of Semiconductors*,38, Issue 8,084001.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J. 2017b. DC and microwave characteristics of Lg 50nm T-gate InAlN/AlN/GaN HEMT for future high power RF applications. *AEU - International Journal of Electronics and Communications*,77,163-168.

PAMPILI, P. and PARBROOK, P.J.2017. Doping of III-nitride materials.*Mater. Sci. Semicond. Process.*,62,180–191.

PERONI, M., ROMANINI, P., PANTELLINI, A., CETRONIO, A., MARIUCCI, L., MINOTTI, A., GHIONE, G., CAMARCHI, V., LIMITI, A., SERINO, E. and CHINI, A.2007. Design, Fabrication, and Characterization of Gamma-gate GaN HEMT for High-Frequency/Wide-Band applications.*Proceedings of 31st Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*,371-378.

QI, L., RUAN, S. and ZENG, Y.J.2021. Review on Recent Developments in 2D Ferroelectrics: Theories and Applications. *Adv. Mater.*,33,2005098.

QIN, J., ZHOU, Q., LIAO, B. and WANG, H. 2018. Modeling of 2DEG characteristics of InxAl1−xN/AlN/GaN-based HEMT considering polarization and quantum mechanical effect. *Electronics*,7,410.

RAMKUMAR, N. and ESWARAN, P. 2021. In AlN / GaN High Electron Mobility Transistor with In GaN Back barrier for Future High-Frequency Applications. *Elementary Education,*20,2186–2193.

SANO, S., EBIHARA, K., YAMAMOTO, T., SATO, T. and MIYAZAWA, N.2018. GaN HEMTs for wireless communication.*SEI Tech. Rev.*, 86,65–70.

SHARMA, M., and CHAUJAR, R. 2022. Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications," *Int. J. RF Microw. Comput. Aided Eng.*,32,23057.

SHARMA, M., KUMAR, B. and CHAUJAR, R. 2023. Polarization induced doping and high-k passivation engineering on T-gate MOS-HEMT for improved RF/microwave performance. *Materials Science and Engineering,*290,116298.

SHRESTHA, N.M., LI, Y. and CHANG, E.Y.2014.Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer. *Jpn. J. Appl. Phys*.,53,04EF08.

SU, L.Y., LEE, F. and HUANG, J.J.2014. Enhancement-Mode GaN-Based High-Electron Mobility Transistors on the Si Substrate With a P-Type GaN Cap Layer.*IEEE Transactions on Electron Devices*,61,460-465.

UREN, M. J., MOREKE, J. and KUBALL, M.2012. Buffer design to minimize current collapse in GaN/AlGaN HFETs.*IEEE Trans. Electron Devices*,59,3327–3333.

YAO, C., YANG, G., LI, Y., SUN, R., ZHANG, Q., WANG, J. and GAO, S.M..2015.Investigation of N-face AlGaN ultraviolet light-emitting diodes with composition-varying AlGaN electron blocking layer.*Opt. Quantum Electron.*,48,1–9.

YUE, Y., HAO, Y., ZHANG, J., NI, J., MAO, W., FENG, Q. and LIU, L. 2008. AlGaN/GaN MOS-HEMT With HfO2 Dielectric and Al2O3 Interfacial Passivation Layer Grown by Atomic Layer Deposition. *IEEE Electron Device Letters*,29,838-840.

ZHANG, X., JIA, K., WANG, Y., FENG, Z. and ZHAO, Z.2013.AlNGaN HEMT T- gate Optimal Design," *Proceedings of the 2nd International Symposium on Computer, Communication, Control and Automation (ISCCCA),*845-847.

CHAPTER 3

Device Optimization of T-shaped Gate and Polarized Doped Buffer Engineered InAlN/GaN HEMT

This chapter investigates the impact of T-shaped gate geometry on parasitic capacitance and RF Figure of Merits (FOMs) such as maximum oscillation frequency (f_{max}), gain-bandwidth product (GBP), cut-off frequency (f_T), maximum stable and available power gain (Gms and Gma), maximum transducer power gain (MSG) and stability factor (k) of E-mode T-gate InAlN/AlN HEMT with polarization doped buffer. The simulation results show that the parasitic capacitances are deeply affected by the geometry of the T-gate. The less influence of gate-to-source capacitance (C_{gs}) by the drain voltage possesses constant depletion charges at the source side, leading to a persistent value of C_{gs} with drain bias. Furthermore, the polarization doped buffer layer is also used, which enhances the two-dimensional electron gas confinement by bending the conduction band upwardly convex, which effectively reduces the leakage current (10^{-8}), the positive shift of V_{th} (0.9 V), and improves the switching ratio (10^{8}) as compared to GaN-buffer HEMT. The effect of gate head length (H_{length}), gate stem height (S_{height}), and gate foot length (F_{length}) on RF Figure of Merits (FOMs) are deeply investigated. The simulated results confirm that the proper choice of H_{length} (280 nm), S_{height} (100 nm), and F_{length} (10 nm) significantly reduced the parasitic capacitance (C_{gs} = 350 fF/mm and C_{gd} = 140 fF/mm) and enhanced the f_{max} (840 GHz), GBP (636 GHz), f_T (583 GHz) and also improve the power gains. The simulated results of the proposed device design show its applicability for high-performance RF/microwave applications.

3.1 Introduction

Silicon technology has been at the forefront of the semiconductor industry for the last two decades, enabling the development of advanced electronic devices such as nanowires *(Abdelmoneam et al., 2018, Muscato et al., 2019)*, cylindrical gates *(Auth and Plummer, 1997, Sarkar et al., 2012)*, recessed channel MOSFETs *(Kumar et al., 2018*), and FinFETs *(Kumar and Chaujar, 2022)*. The role played by these devices in transforming the electronics sector cannot be overstated. They have facilitated the development of compact and powerful devices that consume minimal energy. Still, there is a pressing need for high power RF applications whose demands exceed what can be met with silicon based technology that is already at its maximum capacity. As the demand for higher performance and faster processing speeds continues to increase, researchers are exploring alternative materials and structures that can provide better performance than silicon-based devices. One such material is Gallium Nitride (GaN), which offers higher electron mobility, thermal stability, and power handling capabilities than silicon. GaN-based devices have the potential to provide improved efficiency and power density, making them suitable for high-frequency and high-power applications.

In recent years, AlGaN/GaN high-electron-mobility transistors (HEMTs) have received considerable interest as a promising contender for next-generation technology. The frequency range and efficiency of the next generation of cell phones must improve upon those of its predecessors for use in mobile communication applications. Amplifiers that can operate at higher frequencies and more power are also necessary for the development of satellite transmission and TV programs. In light of these demands, AlGaN/GaN HEMTs appear as a very desired choice for the utilization of microwave power in wireless communication owing to their remarkable features, i.e. bigger bandgap, greater breakdown voltage, strong thermal conductivity, and high mobility *(Mishra et al., 2002*). Moreover, the polarization effect in GaN HEMTs formed the two-dimensional electron gas (2DEG) at the interface, further enhancing the electron mobility and making the GaN-based device a suitable applicant for high-power applications. AlGaN/GaN HEMTs have already shown their applicability for high-power applications. To outstretch the operating frequency of GaN HEMTs for mm-wave application. It is important to reduce the gate length of the device to the nanometer range. Many researchers have published their work on different gate geometry to enhance RF performance. Such as

camel-shaped *(Khan et al., 2013*), T-shaped *(Murugapandiyan et al., 2017a*), and gamma-shaped *(Peroni et al., 2007*) gate structures. Among all these gate structures, the T-shaped gate geometry is appropriate to enhance the RF performance of the device. As the T-shaped structure decreases, the gate resistance and gate capacitance reduces by providing a larger gate area and lower foot length.

The DC and RF performance of a device are quite sensitive to the T-gate size. When the foot length of the T-gate is decreased to below 50 nm, issues such as high leakage current (*Deng et al., 2019*), decreased breakdown voltage (*Murugapandiyan et al., 2017b*), high current collapse (*Saadaoui et al., 2020*), and parasitic resistance (*Cao et al., 2004*) have surfaced. The DC and RF properties of the device might be adversely affected by these problems. Inefficient power dissipation and shortened device lifetimes might result from excessive leakage current. High current collapse may cause instability and a gradual decline in device performance, while a low breakdown voltage might cause device failure. Parasitic resistance, on the other hand, can limit the device's maximum frequency of operation, leading to reduced RF performance. Therefore, selecting the proper T-gate size is crucial to enhancing the device's RF performance. Improper T-gate size selection can never improve the device frequency parameters, and it may even worsen the performance of the device.

Moreover, gate engineering is insufficient to suppress the short-channel effect (SCE). Some more buffer and barrier engineering is required to reduce the SCE and enhance the RF performance of the device. Hence to enhance the performance of the T-gate HEMT device, some barrier and buffer engineering has been done in the proposed structure. The conventional AlGaN barrier layer is replaced by the lattice-matched InAlN material with a lattice constant of 0.83 *(Neuburger et al., 2004*). Constructive buffer engineering has been done where initially used Fe doping *(Pampili and Parbrook, 2017*) is replaced by polarization-induced doping by changing the Al composition of AlGaN material in the buffer region. Although Fe or C doping in the buffer region enhances the resistivity in the buffer, it also creates deep-level acceptors that further increase the current collapse *(Uren et al., 2012*). The polarization doping in the buffer layer acts as a blocking layer that hinders the 2DEG in the buffer region, effectively enhances the breakdown voltage, and reduces the leakage current as discussed in **Chapter 2**. The collective implementation of the graded and T-gate engineering on the proposed structure has significantly enhanced the device's RF performance. The device's high electron mobility and transconductance make it ideal for millimeter-wave applications, and the changes made to

the barrier and buffer engineering have significantly improved the device's performance. The above mentioned engineering techniques collectively formed a E-mode T-gate HEMT which can be used in 5G communications systems, satellite communications, and radar systems.

This chapter investigates the effect of varying the gate and drain bias on the intrinsic parasitic capacitances of a proposed device. Additional research is conducted to learn how varying gate head lengths, gate stem heights, and gate foot lengths affect the device's intrinsic capacitances. The capacitance properties of the device and how they vary under various situations are the focus of this investigation. When evaluating a device's RF performance, it is essential to look at its parasitic capacitances using one of many figures of merits (FOMs). Maximum oscillation frequency, gain-bandwidth product, cut-off frequency, maximum available power gain, maximum transducer power gain, and stability factor are all examples of these FOMs. overall, this section sheds light on key aspects of the proposed device's performance. By analyzing the parasitic capacitances built into the device and looking at the different FOMs, researchers may improve the RF performance of the device for a wide range of uses. These results have important implications for the future of telecommunications, wireless networks, and satellite communication systems, among other disciplines where RF devices are used.

This chapter is organized as described below: In this chapter's Section II, we take a look at the overall design of the tool. The outcomes of the simulations are discussed in Section III of the chapter. These findings examine the relationship between the parasitic capacitance and different figures of merit (FOMs) of E-mode T-gate InAlN/AlN HEMTs with a graded buffer and the lengths of the gates' heads (H_{length}), stems (S_{height}), and foot (F_{length}). The conclusion of the chapter is presented in the final part of the chapter's summary.

3.2 Device Structure

Figure 3.l(a) depicted the proposed T-gate E-mode InAlN/AlN HEMT with polarized doped buffer /graded buffer HEMT (Graded buffer HEMT). The structural parameters of the device are the same as discussed in **Chapter 2** in **Table 2.1**. The device is made up of a lattice-matched InAlN barrier layer, AlN spacer layer, which increases the conduction band discontinuity at AlN/GaN junction and enhances the 2DEG concentration, GaN channel layer, and AlGaN buffer layer in which aluminum composition linearly changes from 0.2 to 0 along the (0001) direction. The T-shaped Schottky gate consists of a Pt/Au metal stack with a smaller footprint

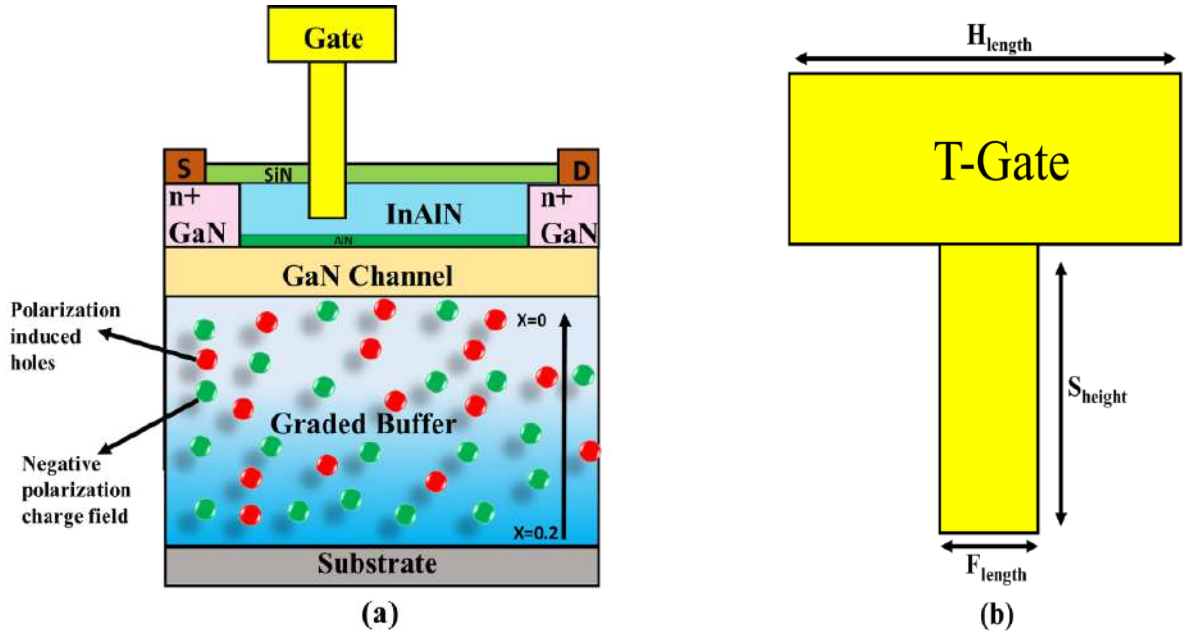

Fig. 3.1 (a) Proposed T-gate InAlN/AlN/ graded buffer HEMT (b) T-gate structure.

and a larger gate area. As can be seen in **Figure 3.l(b)**, the gate head length is expressed by the symbol (H_{length}), the gate stem height is marked by the symbol (S_{height}), and the gate foot length is denoted by the symbol (F_{length}). The dimensions of the T-gate, i.e., gate head length, gate stem height, and gate foot length, were taken as variables to study the impact of gate geometry on device performance. The T-shaped structure decreases the gate resistance and gate capacitance by providing a larger gate area and lower foot length *(Zhang et al., 2013*). The source and drain region doped with Si of order 10^{19} cm^{-3} to reduce the contact resistance *(Murugapandiyan et al., 2017a*). The SiN layer is used to passivate the device, which reduces the parasitic capacitance and enhances the device's frequency parameters *(Murugapandiyan et al., 2017b*). All simulations have been performed using the ATLAS device simulator *(Manual, 2016).*

In the proposed device (graded buffer HEMT) as depicted in **Figure 3.l(a)** the polarization charge discontinuity across the heterojunction formed the fixed polarization charges. When the Al composition changes from the AlGaN to GaN, a negative polarization charge field is induced over bulk, and the induced charge density is calculated by the divergence of the polarization field. This polarization charge density significantly reduce the buffer leakage current as discussed in **Chapter 2**.

3.3 Results and Discussion

3.3.1 DC Characteristics

This subsection focuses on the transfer and electrical performance of proposed (Graded buffer-HEMT) and conventional (GaN buffer-HEMT) devices. The results show that the proposed device has a lower drain current and leakage current than the conventional device, as seen in **Figure 3.2(a, b)**. This reduction in leakage current is attributed to the polarization-

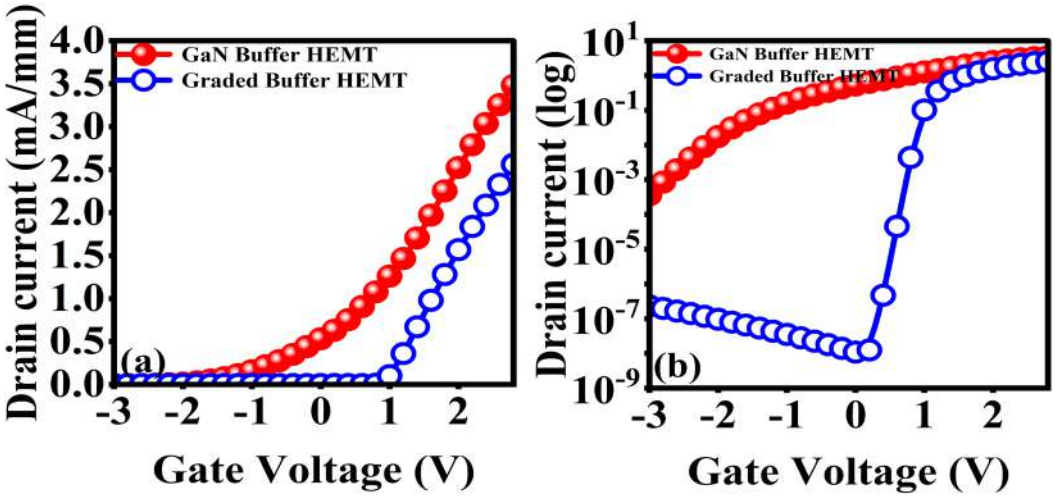

Fig. 3.2 Drain current density (a) Linear scale (b) Log scale for GaN-buffer-HEMT and Graded-buffer-HEMT.

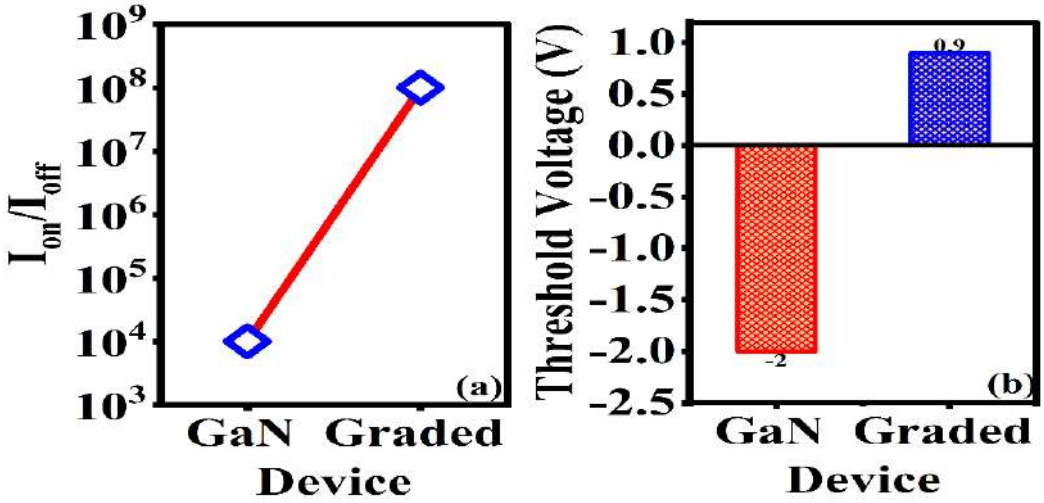

Fig. 3.3 (a) threshold voltage (b) I_{on}/I_{off} ratio for GaN-buffer-HEMT and Graded-buffer-HEMT.

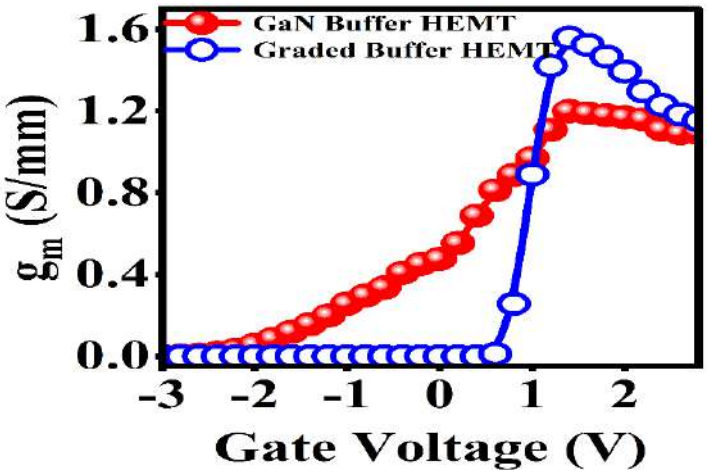

Fig. 3.4 Transconductance characteristics for GaN-buffer-HEMT and Graded-buffer-HEMT.

doped buffer, which improves the I_{on}/I_{off} ratio for the graded buffer HEMT as depicted in **Figure 3.3(a)**. The presence of a negative polarization field in the graded buffer region also enhances the 2DEG confinement and gate controllability, which shifts the threshold voltage positively by 0.9 V as shown in **Figure 3.3(b)**. Additionally, the proposed device exhibits a higher transconductance peak of 1.55 S/mm, which is about 23% better than the conventional device, as shown in **Figure 3.4**. The graded buffer HEMT also displays a sharp change in transconductance at the pinch-off region, which results in a lower subthreshold current in the device. The simulation results are also compared and presented in **Table 3.1**. The proposed device demonstrates superior electrical performance compared to the conventional device, making it an excellent candidate for high-frequency and high-power applications.

TABLE 3.1

Comparison of Device Performance

Device	I_d (A/mm)	I_{off} (A/mm)	g_m (S/mm)	V_{th} (V)	I_{on}/I_{off}
GaN Buffer HEMT	3.48	10^{-3}	1.26	-2	10^4
Graded Buffer HEMT	2.56	10^{-8}	1.55	0.9	10^8

3.3.2 Effect of Gate Foot Length (F_{length})

This subsection investigates the impact of the gate foot length on the parasitic capacitance, RF, and Microwave characteristics of the proposed device. **Figure 3.5(a-d)** exhibits the parasitic capacitance (C_{gs} and C_{gd}) dependency on F_{length} for drain voltage 1 V to 3 V as a function of

gate bias. The parasitic capacitance (C_{gs} and C_{gd}) Vs gate bias relationship is shown for F_{length} = 10 nm in **Figure 3.5 (a)**. C_{gs} and C_{gd} are seen increasing slowly with increasing gate voltages. However, at higher gate bias, there is a rapid rise in C_{gs} and C_{gd} due to the enhanced lateral electric field, which promotes carrier movement from the drain to the source side**.** Additionally, an interesting observation is that as the drain voltage increases from 1 V to 3 V, both C_{gs} and C_{gd} start to decrease. Notably, the decrease in C_{gd} is more significant compared to the gate-to-source capacitance. This discrepancy is attributed to the increase in drain voltage, which results in a reduction of the depletion layer near the drain end. **Figure 3.5 (b)** shows the parasitic characteristics for F_{length} = 20 nm. It has been observed that as the F_{length} increases from 10 nm

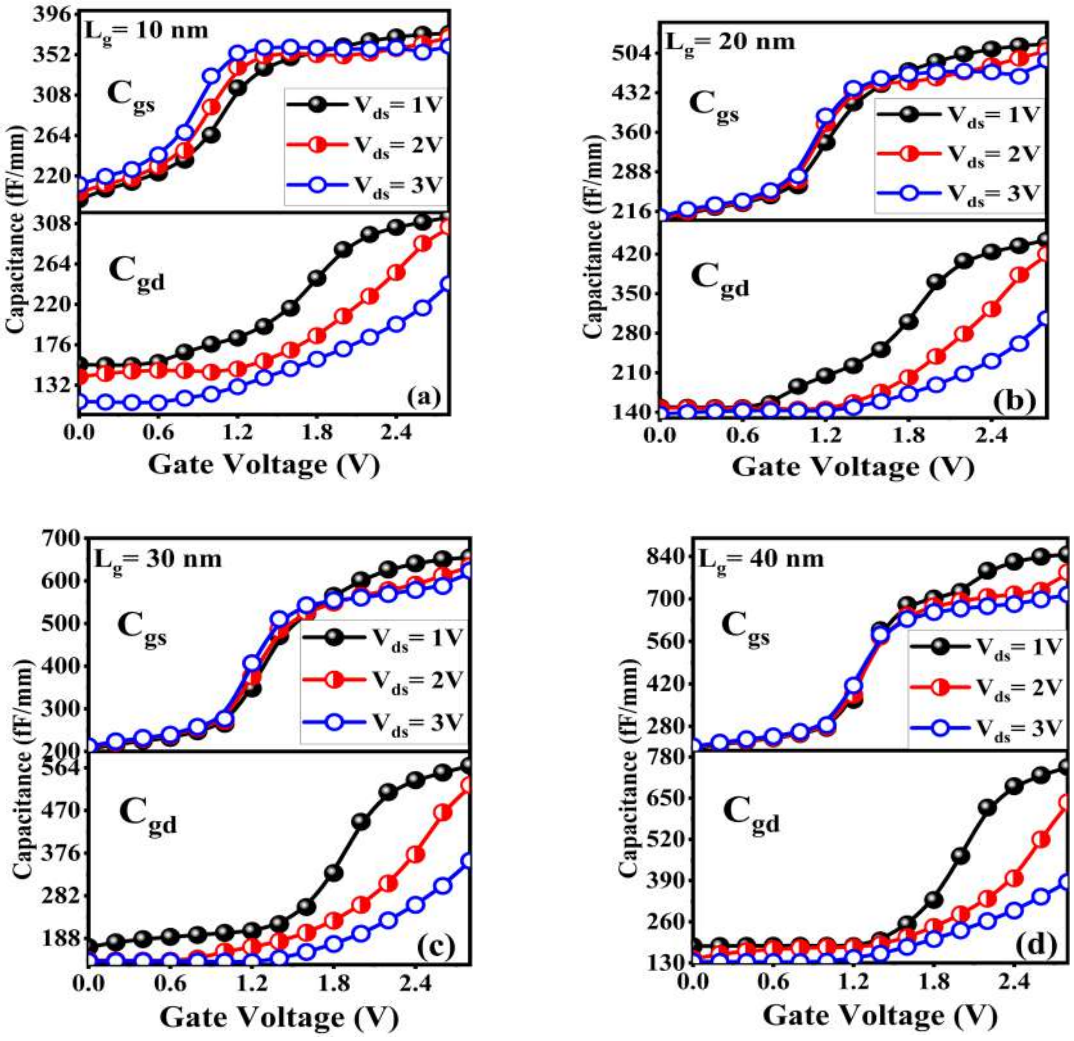

Fig. 3.5. Parasitic capacitance of proposed device for (a) F_{length} 10 nm (b) F_{length} 20 nm (c) F_{length} 30 nm (d) F_{length} 40 nm for V_{ds} 1 V to 3 V.

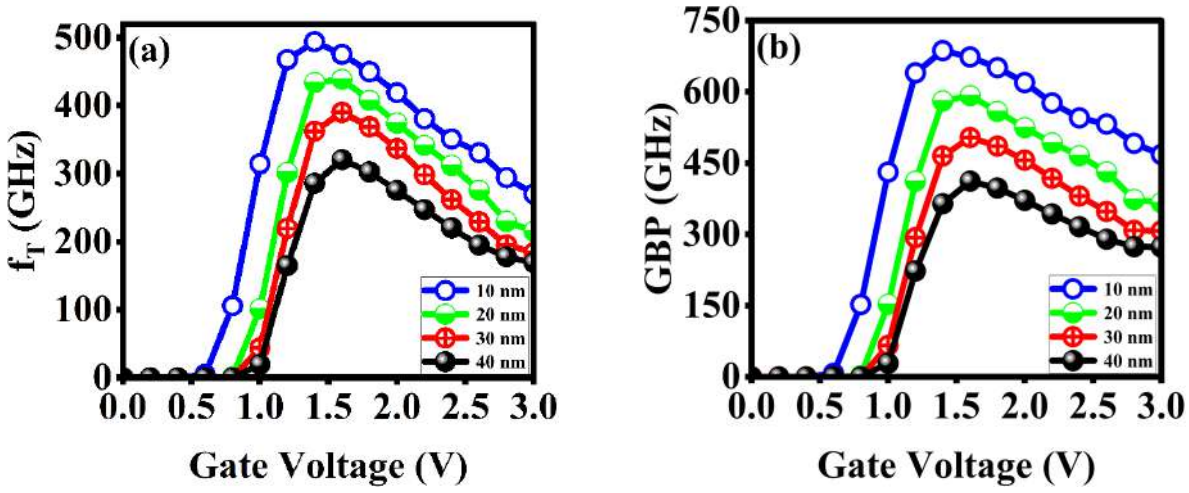

Fig. 3.6. Comparison of (a) f_T (b) GBP (c) C_{gs} and C_{gd} for variable F_{length}.

to 20 nm the C_{gs} and C_{gd} increases to 427 fF/mm and 153 fF/mm at V_{ds} = 3V and V_{gs} = 1.8V which is 22% and 9% higher than the 10 nm gate length. **Figure 3.5 (c, d)** further shows that as the F_{length} increases to 30 nm and 40 nm parasitic capacitance increases. This enhancement in parasitic capacitance with an increase in F_{length} is due to the redistribution of an electric field at the edges of the gate foot**.** The variation of cut-off frequency (f_T) for different F_{length} is depicted in **Figure 3.6(a)**, and the mathematical expression for the f_T is expressed in **Chapter 2**, Equation 2.9 *(Kumar and Chaujar, 2021)*. The reduction of F_{length} from 40 nm to 10 nm enhances the f_T by about 72 %. This enhancement in f_T value for lower F_{length} is due to the decrement of parasitic capacitance with F_{length}. This enhancement in cut-off frequency makes the proposed device suitable for millimeter-wave applications. Another capacitance-dependent parameter is the gain-bandwidth product (GBP), which measures the amplifier's gain and bandwidth. The maximal gain of the device is represented by the peak value of GBP at a specific frequency. The mathematical expression for the GBP is shown in Equation 3.1 *(Gupta et al., 2020)*.

$$GBP = \frac{g_m}{2\pi\, C_{gs}} \tag{3.1}$$

The variability in GBP against gate bias is shown for various F_{length} in **Figure 3.6(b)**. The value of GBP is seen to increase with gate bias at first, reaching a maximum at V_{gs}= 1.5V, then declining with increasing gate bias. This decrease is primarily attributable to the increase in capacitance at increasing gate bias. Furthermore, a higher value of GBP is reported for F_{length}=

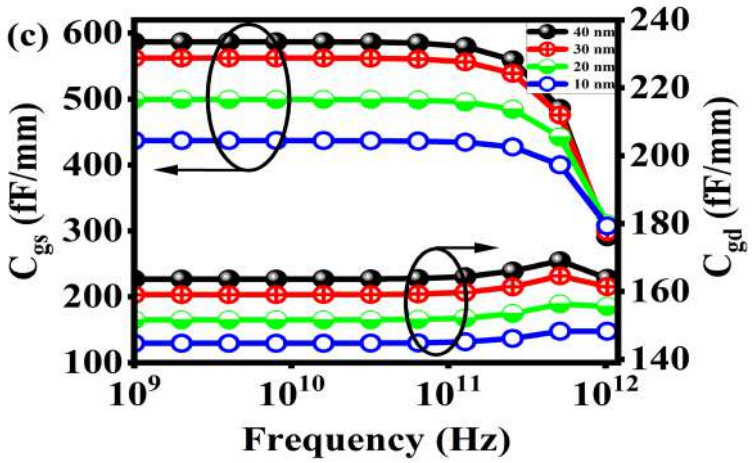

Fig. 3.7 Comparative analysis of gate to source (C_{gs}) and gate to drain capacitance (C_{gd}) for variable F_{length}.

10 nm, which is 88% greater than F_{length}= 40 nm. The increase in GBP value with decreasing gate length is due to the reduction in parasitic capacitance with gate length.

Capacitance versus frequency characteristics for various gate length is displayed in **Figure 3.7**. In the low-frequency range, it was noted that the capacitance was almost unaffected by the frequency; on the other hand, a decrease in capacitance was observed for the high-frequency range. Interface trap charges are present in the heterostructure, and they are responsible for the capturing and releasing of electrons, as well as the generation of interface trap capacitance at lower frequencies. Because of this, when the frequency is high, they no longer respond to the AC signal, and the interface trap capacitance becomes zero; this results in a significant decrease in capacitance. This further proved that the reduction of F_{length} reduces the parasitic capacitance. Thus, the best results are obtained at F_{length} = 10 nm. The microwave properties of graded buffer HEMT for variable F_{length} are shown in **Figure 3.8**. These analyses are also known as small-signal analyses as they require a small input signal for the characterization. **Figure 3.8(a)** and **Figure 3.8(b)** exhibit the variation of current gain (h_{21}) and unilateral power gain (U) with frequency for different F_{length}. The mathematical expression of current gain and unilateral power gain in terms of S-parameters is depicted in **Chapter 2**, Equation 2.5, 2.6 *(Malik et al., 2012)*. The device's f_T and f_{max} are obtained at which current gain and unilateral power gain become unity. The inset bar graph of **Figure 3.8(a, b)** exhibits the f_T and f_{max} for different F_{length}. The higher value of f_T (523 GHz) and f_{max} (840 GHz) is observed for the F_{length} =10 nm, which is 45 % and 20 % higher than the F_{length}= 40 nm. This enhancement is basically due to the reduction of parasitic capacitance (C_{gs} and C_{gd}) with gate length, as shown in **Figure 3.5**. The

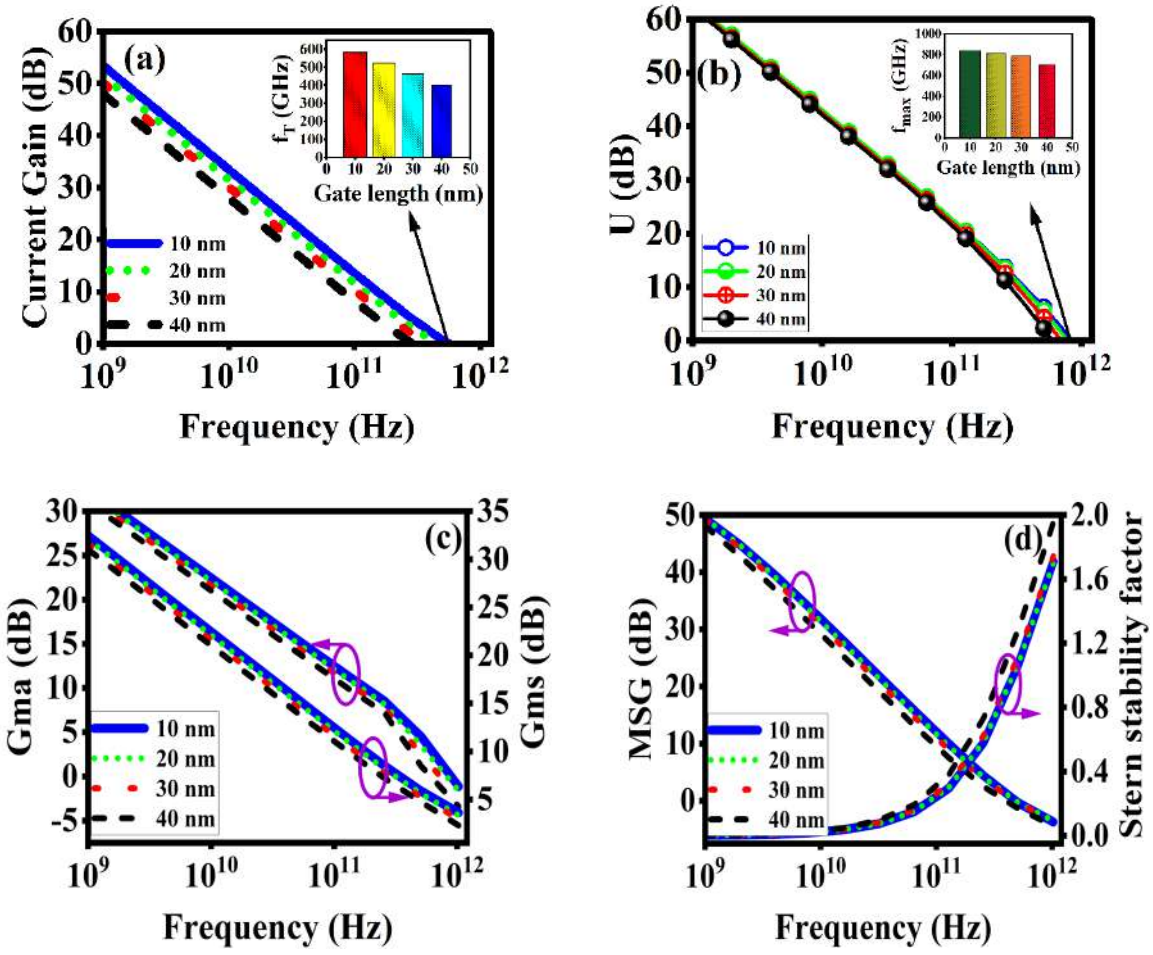

Fig. 3.8. Variation of (a) Current gain (b) Unilateral gain (c) Gma and Gms (d) MSG and Stability factor for different F_{length}.

reduction in parasitic capacitance with the reduction of F_{length} is due to the redistribution of an electric field at the edges of the gate foot. The effect of F_{length} on the device's maximum stable and available power gain Gms and Gma are shown in **Figure 3.8(c)**. For RF amplifier design, the study of Gma and Gms is important. **Figure 3.8(c)** depicted that scaling F_{length} to 10 nm enhances the Gma and Gms by 50 % and 40 %. The rollett stability factor (K > 1) is the sufficient condition for the device's stability, the expression of K is discussed in **Chapter 2**, Equation 2.8 *(Lenka et al., 2013)*. The stability factor and MSG for different F_{length} are shown in **Figure 3.8(d)**. A 20 % improvement in MSG is observed when the F_{length} is reduced to 10 nm, whereas a high stability factor is observed for 40 nm F_{length}. The stability factor for 10 nm F_{length} is K > 1 for high frequency and K < 1 for low frequency, which is suitable for designing the amplifier. The impact of F_{length} on device performance is tabulated in **Table 3.2**. It has been observed that a reduction in gate length from 40 nm to 10 nm leads to a remarkable decrease

in parasitic capacitance (C_{gs} and C_{gd}). This reduction in parasitic capacitance exerts a significant positive influence on key RF performance parameters including f_T, F_{max}, and GBP, resulting in a notable enhancement of the device's overall RF performance. Therefore, based on these noteworthy findings, it can be concluded that a gate length of 10 nm is more favorable for achieving superior RF performance.

TABLE 3.2

Comparison of Device Performance for Variable Gate Foot Length

F_{length} (nm)	C_{gs} (fF/mm)	C_{gd} (fF/mm)	f_T (GHz)	GBP (GHz)	f_{max} (GHz)
10	350	140	583	686	840
20	427	153	525	580	810
30	484	161	465	464	790
40	539	166	400	364	700

3.3.3 Effect of Gate Stem Height (S_{height})

This subsection investigates the impact of the gate stem height of the proposed structure on the parasitic capacitance, RF, and Microwave characteristics of the device. **Figure 3.9(a-d)** investigates the impact of S_{height} on the parasitic capacitances. It has been observed that as the stem height increases from 20 nm to 100 nm, the parasitic capacitance decreases. The increase in the gate stem height of the device causes an increase in the distance between the gate-source and the gate-drain, which results in a decrease in the parasitic capacitance of the device. The graph of parasitic capacitance versus gate voltage for S_{height} 20, 50, and 100 nm are shown in **Figure 3.9(a, b)**. The 125 % and 167 % reduction of C_{gs} and C_{gd} are observed for increasing the S_{height} from 20 nm to 100 nm. Moreover, the variation of parasitic capacitance with frequency is shown in **Figure 3.9(c, d)**. This further proved that the increment of S_{height} reduces the parasitic capacitance.

Figure 3.10(a, b) illustrates how the cut-off frequency and gain-bandwidth product change in response to changes in gate voltage. The increment in S_{height} to 100 nm enhances the f_T and GBP by about 147 % and 132 %. This improvement in f_T and GBP parameters is due to the significant reduction in parasitic capacitance. The impact of S_{height} on microwave performance is shown in **Figure 3.11(a-d)**. The impact of S_{height} on current gain and unilateral gain is depicted in **Figure 3.11(a, b)**.The calculated value of f_T and f_{max} at which current gain and unilateral gain become

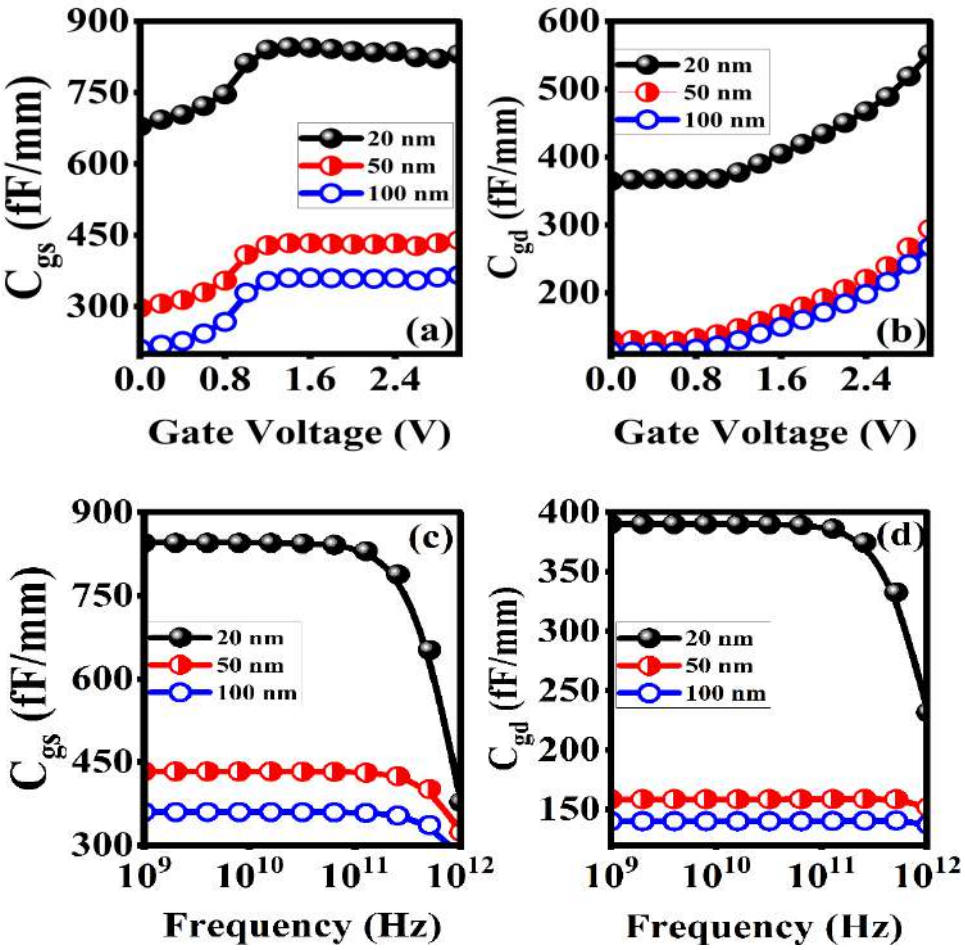

Fig. 3.9. Impact of S_{height} on (a) C_{gs} (b) C_{gd} with gate bias (c) C_{gs} (d) C_{gd} with frequency

unity is portrayed by the inset bar graph of **Figure 3.11(a, b)**. The 160 % and 142 % enhancement of f_T and F_{max} is observed when S_{height} increases to 100 nm. In **Figure 3.11(c)**, the 304 % and 88 % enhancement in Gma and Gms is observed on increasing the S_{height} from 20nm to 100 nm. The maximum stable gain and stability factor for different S_{height} is depicted in **Figure 3.11(d).** Increment in S_{height} further improves the maximum stable gain by about 239 %. The stability factor for S_{height} 100 nm in the cut-off frequency range is 1.08, which shows the stable frequency operation in the device. **Table 3.3** summarizes the effects of S_{height} on device performance. Through observations, it has been determined that an increase in gate stem height from 20 nm to 100 nm results in a notable decrease in parasitic capacitance (C_{gs} and C_{gd}). This reduction in parasitic capacitance has a significant positive impact on RF performance parameters such as f_T, F_{max}, and GBP, consequently enhancing the overall RF performance of the device. Consequently, based on these findings, it can be concluded that a S_{height} of 100 nm is more conducive to achieving superior RF performance.

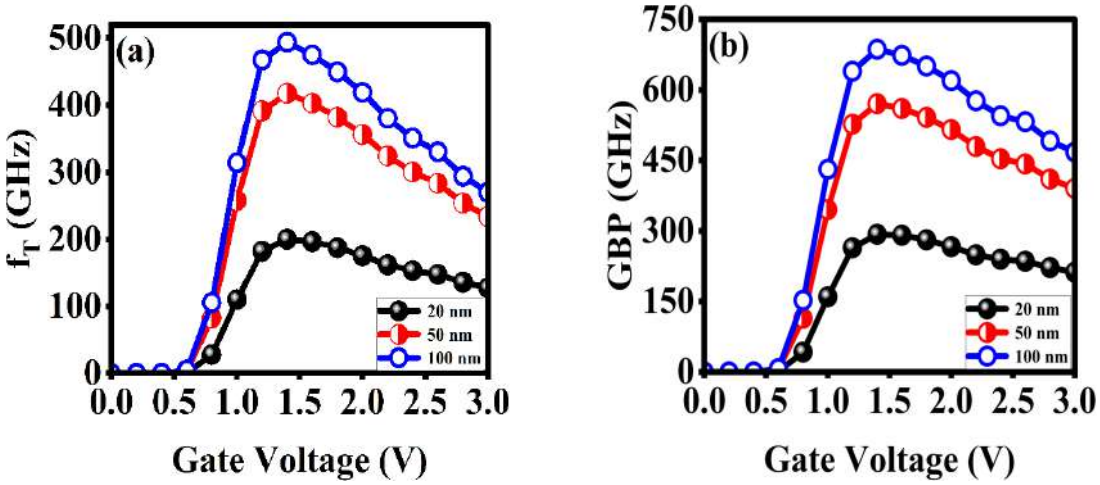

Fig. 3.10. Impact of S_{height} on (a) f_T (b) GBP with gate bias

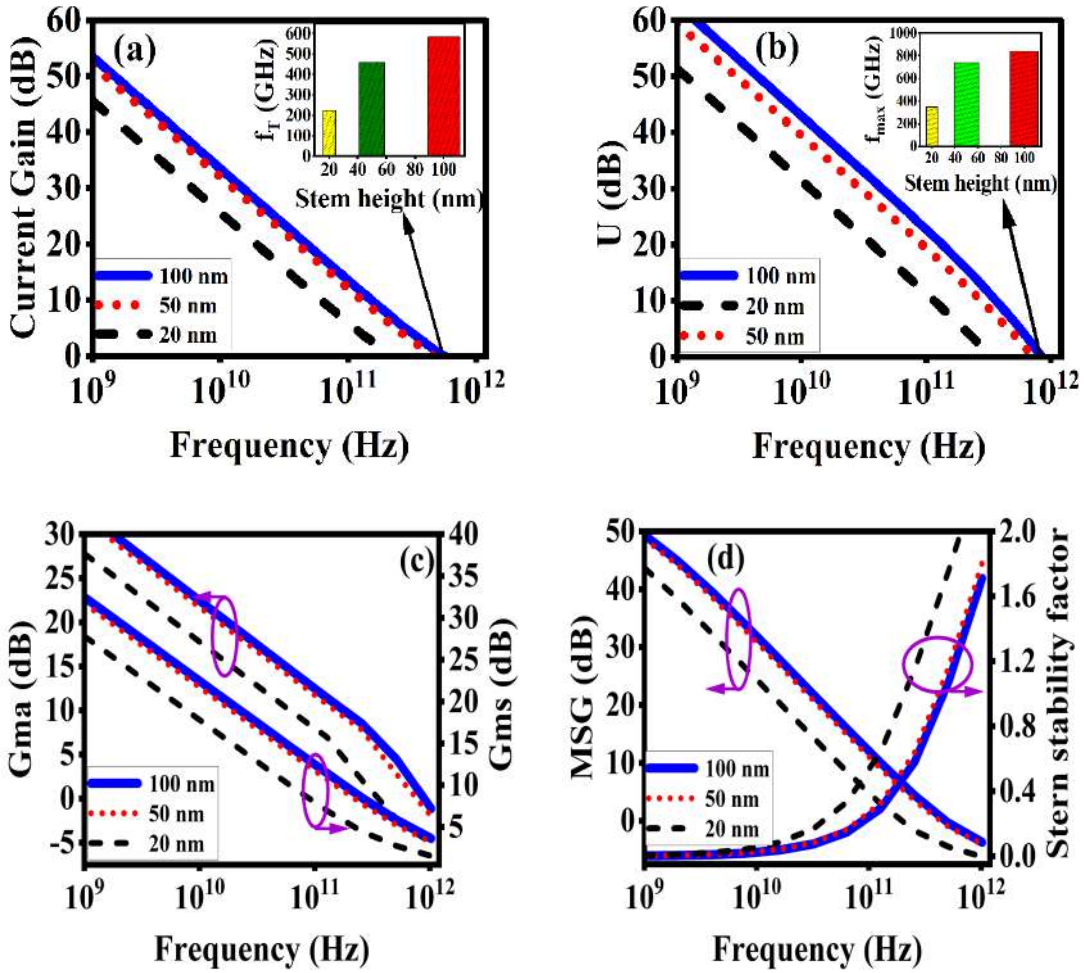

Fig. 3.11. Variation of (a) Current gain (b) Unilateral gain (c) Gma and Gms (d) MSG and Stability factor for different S_{height}

TABLE 3.3
Comparison of Device Performance for Variable Gate Stem Height

S_{height} (nm)	C_{gs} (fF/mm)	C_{gd} (fF/mm)	f_T (GHz)	GBP (GHz)	f_{max} (GHz)
20	788	374	224	292	346
50	424	158	460	570	741
100	350	140	583	686	840

3.3.4 Effect of Gate Head Length (H_{length})

This subsection investigates the impact of the gate head length of the proposed structure on the parasitic capacitance, RF, and Microwave properties of the device. **Figure 3.12(a-d)** investigates the impact of H_{length} on the parasitic capacitances. A parallel decrease in parasitic

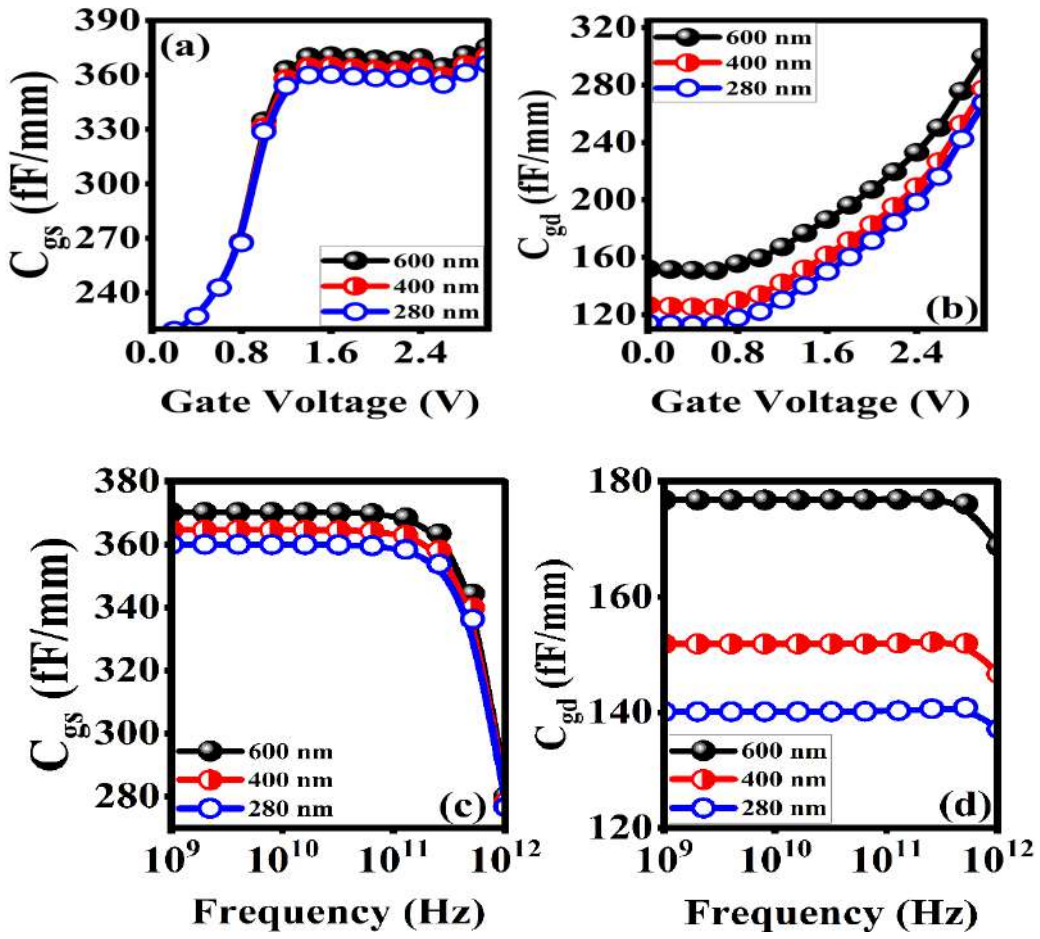

Fig. 3.12. Impact of H_{length} on (a) C_{gs} (b) C_{gd} with gate bias (c) C_{gs} (d) C_{gd} with frequency.

capacitance has been observed as H_{length} is reduced from 600 nm to 280 nm. This is because the increase in H_{length} regulates the depletion layer by providing a consistent electric field distribution below the gate edges. Because of the redistribution of the electric field at the gate edges, the channel depletion length is suppressed and lengthened, which consequently increases capacitance. **Figure 3.12(a, b)** exhibit the graph of parasitic capacitance with gate voltage for H_{length} 280, 400, and 600 nm. It has been observed that C_{gs} and C_{gd} increase gradually at low gate voltage but rapidly at high gate bias due to an increase in the lateral electric field that speeds up the movement of carriers from the drain to the source. The 2.8 % and 25 % reduction of C_{gs} and C_{gd} is observed for reducing the H_{length} from 600 nm to 280 nm. Furthermore, the variation of parasitic capacitance with frequency is shown in **Figure 3.12(c, d)**.

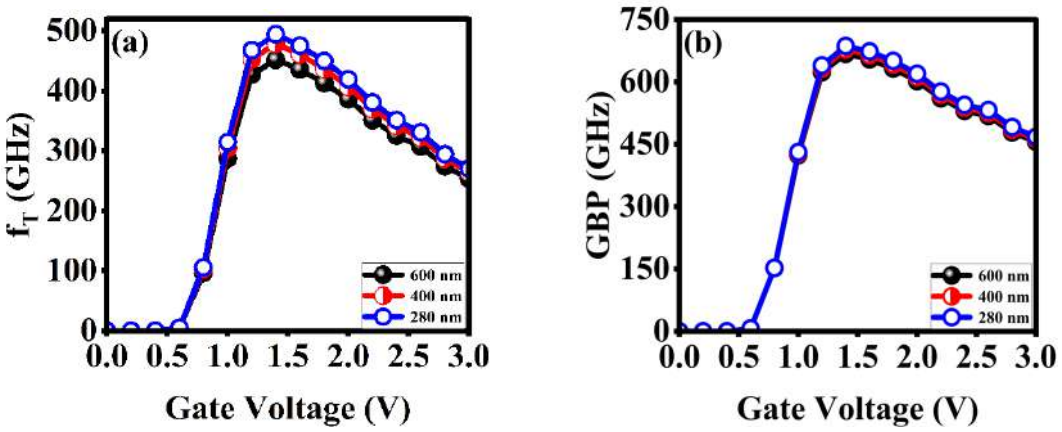

Fig. 3.13. Impact of H_{length} on (a) f_T (b) GBT with gate bias.

Figure 3.13(a, b) illustrate how the cut-off frequency and the gain-bandwidth product change as a function of the gate bias for different H_{length}. The decrement in H_{length} to 280 nm enhances the f_T and GBP by about 9.5 % and 2.5 % due to the significant reduction of parasitic capacitance with H_{length}. The impact of H_{length} on microwave performance is shown in **Figure 3.14(a-d)**. The less impact of H_{length} on h_{21} and unilateral gain is observed in **Figure 3.14(a, b)**. The calculated value of f_T and f_{max} at which current gain and unilateral gain become unity is portrayed by the inset bar graph of **Figure 3.14(a, b)**. The 9.5 % and 7.5 % enhancement of f_T and f_{max} is observed when H_{length} decreases to 280 nm. In **Figure 3.14(c)**, a small enhancement in Gma and Gms is observed on increasing the H_{length} from 600 nm to 280 nm. A minor improvement is observed in maximum stable gain and stability factor for different H_{length} shown

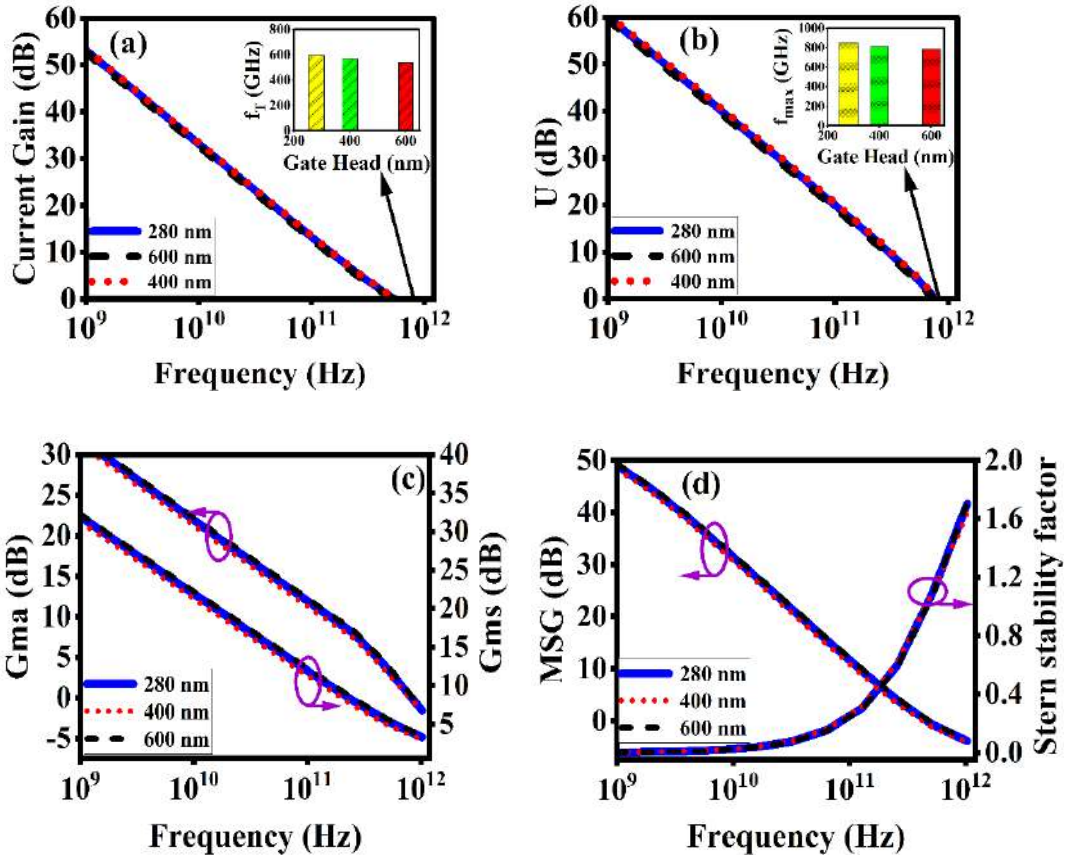

Fig. 3.14 Variation of (a) Current gain (b) Unilateral gain (c) Gma and Gms (d) MSG and Stability factor for different H_{length}.

in **Figure 3.14(d)**. The impact of H_{length} on device performance is tabulated in **Table 3.4**. Observations reveal that as the H_{length} decreases from 600 nm to 280 nm, there is a noticeable reduction in parasitic capacitance (C_{gs} and C_{gd}). This reduction in parasitic capacitance leads to significant improvements in key RF performance metrics such as f_T, F_{max}, and GBP, subsequently enhancing the device's RF performance. Based on these findings, it can be

TABLE 3.4

Comparison of Device Performance for Variable Gate Head Length

H_{length} (nm)	C_{gs} (fF/mm)	C_{gd} (fF/mm)	f_T (GHz)	GBP (GHz)	f_{max} (GHz)
280	350	140	583	686	840
400	358	152	562	678	814
600	363	176	532	668	781

concluded that a H_{length} of 280 nm is more suitable for achieving superior RF performance. **Table 3.5** provides a thorough comparison of the results obtained from our proposed device and the findings reported in published work. Results indicate that our proposed device has greater performance over a wide range of parameters in comparison to the results that have been published.

TABLE 3.5
Comparison of proposed structure with simulated published papers on T-gate HEMT

Reference	L_g	I_d (A/mm)	C_{gs} (fF/mm)	C_{gd} (fF/mm)	f_T (GHz)	f_{max} (GHz)
(Murugapandiyan et al., 2017c)	20 nm	2.6	258	511	343	236
(Murugapandiyan et al., 2017a)	30 nm	2.1	-	-	350	340
(Murugapandiyan et al., 2017d)	30 nm	2.4	434	173	246	290
(Zine-eddine et al., 2019)	10 nm	2.5	315	121	524	758
(Murugapandiyan et al., 2020)	30 nm	2.7	572	84	426	366
(Four and Kameche, 2020)	30 nm	0.6	-	-	50	150
This work	10 nm	2.5	350	140	583	840

3.4 Summary

In this chapter, the proper structure of a T-gate InAlN/AlN/graded buffer HEMT along with its influence on the device's parasitic capacitance, RF performance, and microwave performance were investigated. The results of the simulation verified that increasing H_{length} to 280 nm, decreasing F_{length} to 10 nm, and increasing the increment of S_{height} to 100 nm greatly decreased

the C_{gs} by 2.8%, 125%, and 54%, and C_{gd} to 25%, 167%, and 18%. This contributes to an increase in the value of the GBP and f_T of 2.5%, 132%,88%, 9.5%, 160%, and 72% respectively. It has also been discovered that f_{max} increases with a variety of power advancements, which is evidence that the device requires suitable gate geometry optimization. The findings of the simulation lead one to the additional conclusion that the stem height of the gate has a significant impact on both the parasitic and RF performance. Therefore, an InAlN/AlN T-gate with a graded buffer HEMT that has a F_{length} equal to 10 nm, a S_{height} equal to 100 nm, and a H_{length} equal to 280 nm is an applicant that is suited for use in RF and microwave applications.

Moreover, noise and scattering parameters are critical in determining the overall performance of a device. The noise parameters are important because they determine the amount of noise that is present in the signal as it passes through the device. On the contrary, the scattering parameters determine the magnitude of power dissipated during the transmission of the signal across the device. Subsequently, the next chapter of the thesis will investigate the impact of polarization-doped buffer engineering on the noise and scattering characteristics of T-gate HEMTs. The investigation will aim to determine how the changes in buffer engineering impact the noise and scattering parameters, and whether the changes are beneficial or detrimental to the device performance.

3.5 References

ABDELMONEAM, A., INIGUEZ, B. and FEDAWY, M. 2018. Compact modelling of quantum confinement in III-V gate all around nanowire MOSFET. *2018 Spanish Conference on Electron Devices (CDE),*1-4.

AUTH, C.P. and PLUMMER, J. D. 1997. Scaling theory for cylindrical, fully depleted, surrounding-gate MOSFETs. *IEEE Electron Device Letters*,18,74-76.

CAO, X., THOMAS, S., MACINTYRE, D., MCLELLAND, H., BOYD, E., ELGAID, K., HILL, R., STANLEY, C. R. and THAYNE, I. G. 2004. Fabrication and performance of 50 nm T-gates for InP high electron mobility transistors. *Microelectronic Engineering*,73,818-821.

DENG, J., SHAO, J., WAN, J., LU, B. and CHEN, Y. 2019. A theoretical study of gating effect on InP-InGaAs HEMTs by tri-layer T–shape gate. *Microelectronic Engineering*,208,54-59.

FOUR, I. and KAMECHE, M. 2020. Optimization of D.C. and A.C. performances for Al 0 . 26 Ga 0 .

74 N / GaN / 4H-SiC. *International Journal of Nanoelectronics and Materials*,13,361–372.

GUPTA, N., KUMAR, A. and CHAUJAR, R. 2020. Design Considerations and Capacitance Dependent Parametric Assessment of Gate Metal Engineered SiNW MOSFET for ULSI Switching Applications. *Silicon*,12,1501-1510.

KHAN, M.A., HEO, J.W., KIM, Y.J., PARK, H.C., PARK, H.M., KIM, H.S. and MUN, J.K. 2013.Effects of a recessed camel-gate head structure on normally-off ALGaN/GaN HEMTs.*Journal of the Korean Physical Society*,62,787-793.

KUMAR, A., TRIPATHI, M.M. and CHAUJAR, R. 2018. Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. *IEEE Transactions on Electron Devices,*65,860–866.

KUMAR, B. and CHAUJAR, R. 2021. Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET. *Silicon*,13,919-927.

KUMAR, B. and CHAUJAR, R. 2022. Numerical simulation of analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for ULSI switching applications. *The European Physical Journal Plus*,137,110.

LENKA, T. R., DASH, G. N. and PANDA, A. K. 2013. RF and microwave characteristics of a 10 nm thick InGaN-channel gate recessed HEMT. *Journal of Semiconductors*,34,114003.

MALIK, P., GUPTA, R.S., CHAUJAR, R. and GUPTA, M. 2012. AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. *Microelectronics Reliability*,52,151-158.

MANUAL, A.U.S. 2016. *Silvaco . Santa Clara, CA*.

MISHRA, U. K., PARIKH, P.and WU, Y. F.2002. AlGaN/GaN HEMTs - An overview of device operation and applications. *Proc. IEEE,* 90, 1022–1031.

MURUGAPANDIYAN P., RAVIMARAN, S., WILLIAM, J., AJAYAN, J. and NIRMAL, D. 2017c. DC and microwave characteristics of 20 nm T-gate InAlN/GaN high electron mobility transistor for high power RF applications. *Superlattices and Microstructures*,109,725–734.

MURUGAPANDIYAN, P., MOHANBABU, A., RAJYA LAKSHMI, V., RAMAKRISHNA, V. N., VARGHESE, A., WASIM, M., BASKARAN, S., SARAVANA KUMAR, R. and JANAKIRAMAN, V. 2020. Performance analysis of HfO2/InAlN/AlN/GaN HEMT with AlN buffer layer for high power microwave applications. *Journal of Science: Advanced Materials and*

Devices,5,192–198.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J. 2017b. DC and microwave characteristics of Lg 50nm T-gate InAlN/AlN/GaN HEMT for future high power RF applications. *AEU - International Journal of Electronics and Communications*,77,163-168.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J.2017a. 30 nm T-gate enhancement-mode InAlN/AlN/GaN HEMT on SiC substrates for future high power RF applications.*Journal of Semiconductors*,38, Issue 8,084001.

MURUGAPANDIYAN, P., RAVIMARAN, S., WILLIAM, J. and MEENKSHI SUNDARAM, K. 2017d. Design and analysis of 30 nm T-gate InAlN/GaN HEMT with AlGaN back-barrier for high power microwave applications. *Superlattices and Microstructures*,111, 1050–1057.

MUSCATO, O., CASTIGLIONE, T. and COCO, A. 2019. Hydrodynamic modeling of electron transport in gated silicon nanowires transistors. *Atti della Accademia Peloritana dei Pericolanti-Classie di Scienze Fisiche, Matematiche e Naturali*,97,18.

NEUBURGER, M., ZIMMERMANN, T., KOHN, E., DADGAR, A., SCHULZE, F., KRTSCHIL, A., GUNTHER, M., WITTE, H., BLASING, J., KROST, A., DAUMILLER, I. and KUNZE, M. 2004. Unstrained InAlN/GaN HEMT structure. *Proceedings. IEEE Lester Eastman Conference on High Performance Devices, 2004*,14,161–166.

PAMPILI, P. and PARBROOK, P.J.2017. Doping of III-nitride materials.*Mater. Sci. Semicond. Process.*,62,180–191.

PERONI, M., ROMANINI, P., PANTELLINI, A., CETRONIO, A., MARIUCCI, L., MINOTTI, A., GHIONE, G., CAMARCHI, V., LIMITI, A., SERINO, E. and CHINI, A.2007. Design, Fabrication, and Characterization of Gamma-gate GaN HEMT for High-Frequency/Wide-Band applications.*Proceedings of 31st Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*,371-378.

SAADAOUI, S., FATHALLAH, O. and MAAREF, H. 2020. Effects of current transportation and deep traps on leakage current and capacitance hysteresis of AlGaN/GaN HEMT. *Materials Science in Semiconductor Processing*,115,105100.

SARKAR, A., DE, S., DEY, A. and SARKAR, C. K. 2012. Analog and RF Performance Investigation of Cylindrical Surrounding-Gate MOSFET with an Analytical Pseudo-2D Model. *Journal of Computational Electronics,*11,182–195.

UREN, M. J., MOREKE, J. and KUBALL, M.2012. Buffer design to minimize current collapse in

GaN/AlGaN HFETs.*IEEE Trans. Electron Devices*,59,3327–3333.

ZHANG, X., JIA, K., WANG, Y., FENG, Z. and ZHAO, Z.2013.AlNGaN HEMT T- gate Optimal Design," *Proceedings of the 2nd International Symposium on Computer, Communication, Control and Automation (ISCCCA),*845-847.

ZINE-EDDINE, T., ZAHRA, H. and ZITOUNI, M. 2019. Design and analysis of 10 nm T-gate enhancement-mode MOS-HEMT for high power microwave applications. *Journal of Science: Advanced Materials and Devices*,4,180–187.

CHAPTER 4

Small Signal and Noise Behavior of T-Gate E-Mode HEMT with Polarization Induced Doped Buffer

This chapter investigates the small signal and noise behavior of T-gate E mode HEMT with a polarization-doped buffer. The polarization-induced doping in the buffer layer bent the conduction band upwardly convex, which enhanced the 2DEG confinement, reduced the buffer leakage current, and significantly enhance the transconductance (1.55 S/mm). The increment in transconductance leads to a reduction in the reflection coefficient (S11, S22) and an improvement in the transmission coefficient (S21) as compared to GaN buffer HEMT. Furthermore, noise parameters such as auto/cross-correlation factor, minimum noise figure, noise conductance, and optimal noise resistance and reactance were also evaluated for the proposed device. Simulated results reveal that the proposed device has a lower noise figure and noise conductance than the GaN buffer HEMT by 57% and 20%, respectively. This research demonstrates that the T-gate polarization doped buffer (PDB-HEMT) structure is an excellent choice for Low Noise Amplifiers (LNA) operating at higher frequencies.

4.1 Introduction

In recent years, numerous nations have been making concerted efforts to commercialize millimeter-wave (mm-Wave) fifth-generation (5G) new radio (NR) communication in an effort to better manage the exponential growth in mobile data traffic. As a result, a significant amount of research has been carried out in order to develop and ensure the viability of solutions that are high-performing, low-cost, and highly dependable in preparation for the wide-scale implementation of 5G base stations *(Hossain and Hasan, 2015)*. In point of fact, the mm-Wave 5G NRs of the future will implement enormous multiple-input multiple-output (MIMO) technology, which will make use of a phased-array antenna configuration. Therefore, there is a significant demand for high radio frequency (RF) and low noise amplifiers for a modern wireless communication system.

Low Noise Amplifiers (LNAs) are the foundation of any wireless network. The signal-to-noise ratio of a weak transmission can be preserved by using a low-noise amplifier, which is an electrical amplifier. Both the data and the noise at the amplifier's input will be amplified, but the amplifier will also introduce some new noise. The purpose of LNAs is to reduce this background disturbance. Extra noise can be kept to a minimum by designers opting for low-noise components, working points, and circuit designs. Power gain and impedance matching are two other design objectives that need to be balanced with reducing unwanted noise. There are a variety of applications for LNAs, including electrical diagnostic tools, medicinal devices, and wireless transmission systems. In some cases, a standard LNA can provide a power increase of 100 (20 dB) while simultaneously reducing the signal-to-noise ratio by less than a factor of two (3 dB NF). Although low-noise amplifiers are mainly concerned with feeble signals just above the noise level, bigger signals that produce intermodulation interference must also be taken into account.

Regarding LNA design, there are four key considerations: gain, noise figure, non-linearity, and impedance matching. One of the most critical aspects of a low-noise amplifier's performance is its noise figure *(Mohanbabu et al., 2017*). Thus, we can determine which LNA best suits a certain application. When a Low Noise Amplifier does not have a high gain, noise in the LNA circuit might impact the signal and even attenuate it. Gain and noise figures are balanced via input-matching circuits. Through the use of scattering parameter analysis, the circuit's gain, noise figure, and stability circle were all calculated. The initial stage of the amplifier must have

a high amplification level to reduce the amount of noise.

AlGaN/GaN high-electron-mobility transistors (HEMTs) have recently gained a significant amount of attention as a potential candidate for the technology of the next generation. When it comes to mobile communication applications, the next generation of cell phones needs to have both a wider frequency and better effectiveness than their predecessors. In light of these requirements, AlGaN/GaN HEMTs emerge as a highly desirable option for the use of microwave power in wireless communication due to their extraordinary properties. AlGaN/GaN HEMTs have been the subject of several studies *(Mishra et al., 2002, Sano et al., 2018)* due to their usefulness in high RF applications. AlGaN/GaN HEMT *(Liu et al., 2022, Chen et al., 2022)*, together with its low noise and high power microwave performance, as well as its high current drive capabilities, drew attention to its use in low noise applications. In the context of wideband robust receiver applications, various AlGaN/GaN HEMT-based LNAs were created *(Kobayashi, 2012, Moon et al., 2016)*. GaN HEMTs have made significant progress in their development for usage in LNAs, with results showing NF_{min} values of 1.6 dB at 30 GHz *(Sun et al., 2009*) and 1.2 dB at 20 GHz *(Chang et al., 2010*) when using a gate length of 100 nm. *Shinohara et al., 2013,* reported a good NF_{min} of around 0.5 dB at 30 GHz, which exhibited the cut-off frequency (f_T) of 400 GHz and maximum oscillation frequency (f_{max}) of 500 GHz using 20-nm T-gate AlGaN/GaN HEMTs.

However, AlGaN/GaN HEMT also faces a number of difficulties that prevent it from being widely used. The primary roadblock that AlGaN/GaN HEMT faces is its strain problem, which is caused by the lattice mismatch at the interface of GaN/ AlGaN. As described in **Chapter- 1** *(Ambacher et al., 2000*), the polarization discontinuity at the interface barrier-layer / buffer of the AIGaN/GaN HEMT forms a highly mobile sheet charge serving as the channel charge. This charge is caused by piezo and spontaneous polarization, respectively. The polarization discontinuity of standard AIGaN/GaN-HEMTs, which incorporates piezo and random components, is proportional to the aluminium concentration in the barrier layer. Either the aluminium content of the barrier layer needs to be increased, or modulation doping needs to be used in order to achieve the desired increase in sheet charge density and subsequent increase in maximum DC-output current.

However, excessive Al concentration increases strain and degrades the material quality. In this contribution, an InAIN layer is used in place of an AlGaN barrier layer, which results in the

formation of a new layer structure. The greater spontaneous polarization of InAlN in comparison to AlGaN *(Kuzmik, 2001*) makes this layer structure capable of producing theoretically higher sheet charge concentrations. The HEMTs that are based on InAlN and AlN make it possible for the device to scale aggressively, which increases the f_T and decreases the short-channel impact *(Sun and Benedickter, 2010)*. Though the InAlN/AlN T-Gate HEMTs claimed to have numerous benefits, they also had one significant drawback: 2DEG spilling from the channel into a buffer, which lowers the device's mobility and reliability *(Khan et al., 1992*). Therefore, the performance of InAlN HEMTs has to be made more resilient by implementing creative buffer engineering. Polarization doping, which may be achieved by grading the AlGaN layer, has recently gained popularity and is seen as a superior option *(Jena et al., 2002*). The researchers have also adapted another technique, which involves increasing the resistivity of the buffer layer by doping it with either iron (Fe) or carbon (C) acceptors *(Pampili and Parbrook, 2017*). On the other hand, these dopants cause the generation of deep-level acceptors in the layer, which results in a current collapse *(Uren et al., 2012).* Therefore, polarization doping produced by grading the AlGaN layer has been regarded as a superior option. Because of the polarization-induced doping in the buffer, the potential can be bent upwardly convex. This increases the resistivity in the buffer layer without any intentional doping, which significantly reduces the buffer leakage current, improving the pinch-off voltage and microwave performance of the device.

To outstretch the operating frequency of GaN HEMTs for mm-wave application. It is important to reduce the gate length of the device to the nanometer range. The T-shaped gate geometry is appropriate to enhance the RF performance of the device by providing a larger gate area and lower foot length as discussed in **Chapter 3**.

Thus, with an anticipation of the combined advantages of the InAlN barrier layer, polarization-doped buffer layer, and T-shaped gate geometry. The small signal and noise behavior of the proposed device structure i.e., E-mode T-gate InAlN/AlN HEMT with polarization-doped buffer/graded buffer (PDB-HEMT) has been examined in this chapter. Measurements of a HEMT's S-parameters offer the best approach for analysing the small-signal behavior of the device when it is subjected to high frequencies. S-parameters are utilized most frequently by networks that operate at radio frequency and microwave frequencies because it is simpler to calculate signal power and energy analysis at these frequencies than it is to determine voltages and currents. Since it is very challenging to determine current and voltage at high frequencies.

At high frequencies, it is difficult to create a short circuit or an open circuit. As a consequence of this, microwave engineers deal with S-parameters, which utilize waves and matched terminations (50Ω). This strategy reduces the impact of reflection issues as well *(Liou and Schwierz, 2003*). Additionally, it has been observed that reducing the gate length below 50 nm lead to enhancement of the short channel effect. In order to overcome scaling limitations, polarization-doped buffer engineering has been implemented in the proposed structure which reduced the buffer leakage current, enhanced microwave performance, and reduced noise, and provide new opportunities for low-noise applications.

The following outline constitutes this chapter's structure: The first section of this chapter provides an overview of the device construction. The later part of the chapter discusses the results obtained through simulation. These results include the scattering parameters and noise parameters such as auto/cross-correlation factor, minimum noise figure, noise conductance, and optimal noise resistance and reactance of E-mode T-gate InAlN/AlN HEMTs with polarization doped buffer. The conclusion of the chapter is presented in the final part of the chapter's summary.

4.2 Device Structure

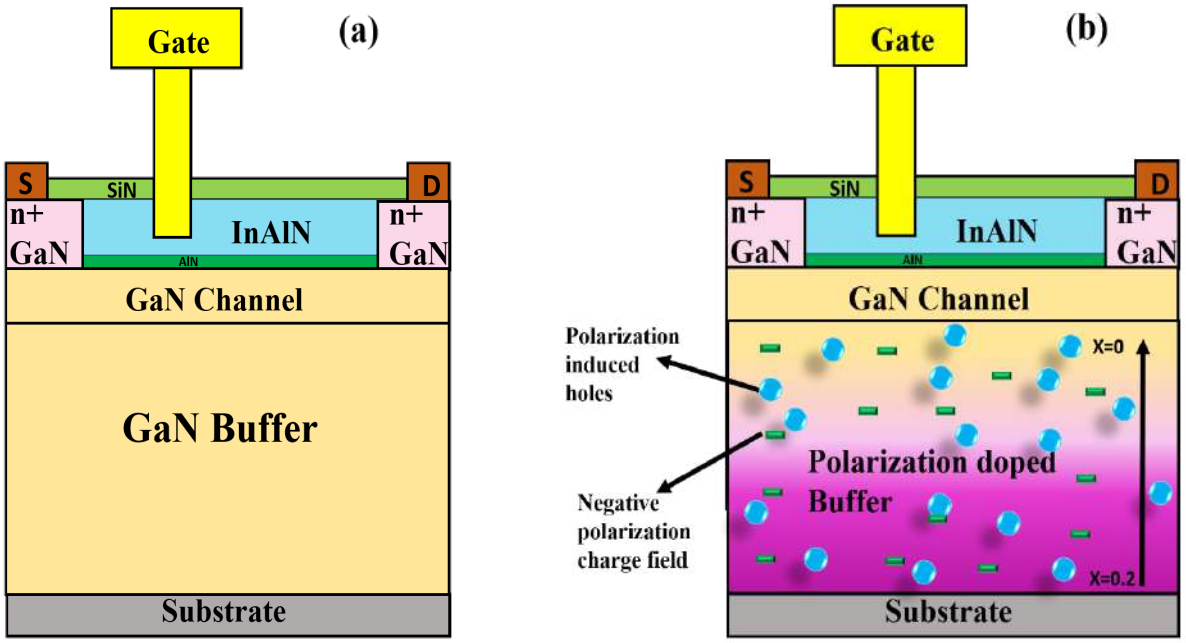

Fig. 4.1 (a) GaN buffer HEMT(GaN-HEMT) (b) polarization doped buffer HEMT(PDB-HEMT) *(Sharma et al., 2023*).

Figure 4.1(a, b) depicted the conventional GaN-HEMT and proposed PDB-HEMT's schematic structure. The dimensions of both devices are the same. The structural parameters of the device are the same as discussed in **Chapter 2** in **Table 2.1**. The device is made up of a lattice-matched InAlN barrier layer, AlN spacer layer, which increases the conduction band discontinuity at AlN/GaN junction and enhances the 2DEG concentration, GaN channel layer, and AlGaN buffer layer in which aluminum composition linearly changes from 0.2 to 0 along the (0001) direction. The T-shaped Schottky gate consists of a Pt/Au metal stack with a smaller footprint and a larger gate area. The T-shaped structure decreases the gate resistance and gate capacitance by providing a larger gate area and lower foot length *(Zhang et al., 2013)*. The source and drain region doped with Si of order 10^{19} cm^{-3} to reduce the contact resistance *(Murugapandiyan et al., 2017a).* The SiN layer is used to passivate the device, which reduces the parasitic capacitance and enhances the device's frequency parameters *(Murugapandiyan et al., 2017b*). All simulations have been performed using the ATLAS device simulator *(Manual, 2016).*

In the proposed device PDB-HEMT as depicted in **Figure 4.1(b)** the polarization charge discontinuity across the heterojunction formed the fixed polarization charges. When the Al composition changes from the AlGaN to GaN, a negative polarization charge field is induced over bulk, and the induced charge density is calculated by the divergence of the polarization field, which changes along the growth direction. This polarization charge density significantly reduce the buffer leakage current as discussed in **Chapter 2**.

4.3 Results and Discussion

In this section we have investigated the small signal and noise behavior of proposed polarization doped buffer HEMT (PDB-HEMT) and GaN-buffer HEMT (GaN-HEMT). The DC characteristics of both devices are exhibited in **Figure 4.2**. The lower drain current density, positive shift in threshold voltage, and higher transconductance value is observed for PDB-HEMT as discussed in **Chapter 3**. **Figure 4.2** shows that PDB-HEMT has E-mode characteristics and GaN-HEMT has D-mode characteristics. Hence for a fair comparison, we have investigated the small signal and noise behavior at V_{gs}= 1.4 V for PDB-HEMT and V_{gs}= 1.8 V for GaN-HEMT. These voltages are taken into consideration because a peak of transconductance has been observed in these voltages. Therefore, we have investigated the small signal and noise behavior on these voltages throughout the chapter.

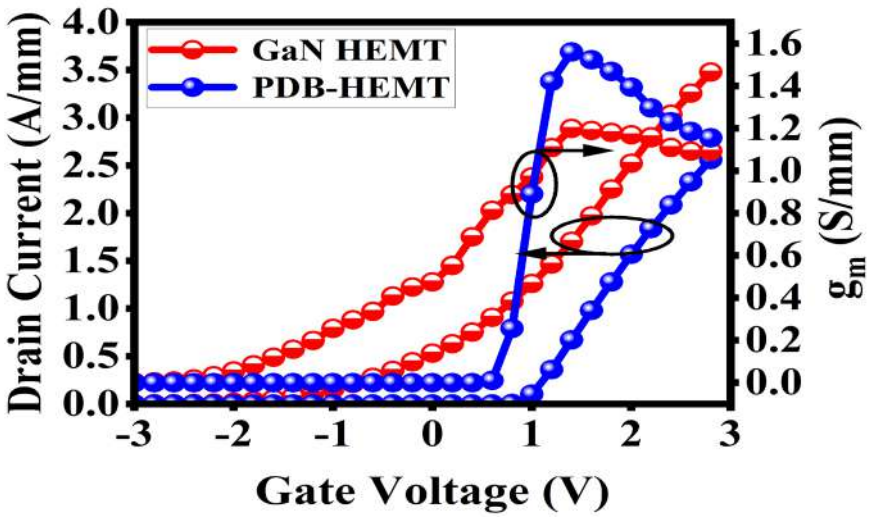

Fig. 4.2 Comparative analysis of drain current and transconductance for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023)*.

4.3.1 Small Signal Analysis

In this subsection, we have focused on the small signal behavior of the proposed PDB-HEMT and also compared the simulated result with the GaN-HEMT. One of the greatest ways to look into the high-frequency small-signal behavior of HEMTs is via measurements of their S-parameter. Networks that operate at microwave frequencies often use S-parameters because it is simpler to compute signal power and energy at radio and microwave frequencies than currents and voltages. The S parameters are based on the assumption that the incident and reflected waves on a transmission line may be decomposed into voltage and current at each port, respectively.

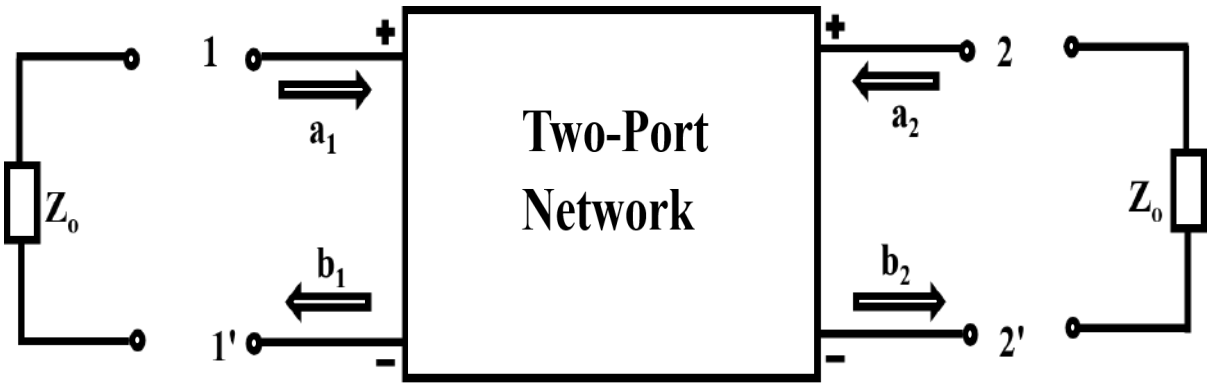

Fig. 4.3 Representation of two port network with the set of incident and reflected parameters (a_1, b_1) and (a_2, b_2) *(Hasirci et al., 2018)*.

The S parameters provide information about the behavior of an input wave when it interacts with a specific port. This input signal may be reflected at that port or it may be transmitted through the system to the output port. Therefore, S parameters are used to characterize the amount of the wave that travels along each of these trajectories. The S parameter of an N-port network consists of an N/N matrix where each matrix element describes a possible trajectory for a voltage wave incident on a port, either reflecting out that same port or transmitting through another port. **Figure 4.3** shows the two-port network system. There are two different sets of parameters that represent the incident and reflected waves for the two-port network at terminals 1-1' and 2-2', respectively. These sets of parameters are (a_1, b_1) and (a_2, b_2). As a consequence of this, the scattering parameters of the two-port network may be described in terms of the incident and reflected parameters as follows *(Kumar et al., 2018)*:

$$S_{11} = \frac{b_1}{a_1}, a_2 = 0 \qquad S_{12} = \frac{b_1}{a_2}, a_1 = 0$$
$$S_{21} = \frac{b_2}{a_1}, a_2 = 0 \qquad S_{22} = \frac{b_2}{a_2}, a_1 = 0 \tag{4.1}$$

Parameter S11 in Equation 4.1 is the input reflection coefficient, whereas S21 represents forward transmission, S12 is the reverse transmission, and S22 is the output reflection coefficient. Each of the four scattering parameters is written as a ratio of the reflected to incident parameters. When a_1 and a_2 are equal to zero then the reference impedance of port 1 and port 2 is equal to the terminating impedance. The reflection coefficient evaluates the matching between the terminating impedance and the port. For RF circuit design, matching is required, and a perfectly matching condition occurs when the reflection coefficient reduces to zero *(Gupta and Chaujar, 2016)*. Hence, a lower value of S11 and S22 is required for better RF performance. In **Figure 4.4(a, b)**, the lower value of S11 and S22 is obtained for the PDB-HEMT. The reduction of the S11 parameter in PDB-HEMT is due to the reduction of source resistance and gate resistance in PDB-HEMT, which is 27.7% and 67.6% lower than the GaN-HEMT as shown in **Figure 4.5(a, b)**. The lower value of gate and source resistance increases the coupling between the input and output port and decreases the S11 parameter. The higher value of drain resistance, transconductance, and lower channel resistance reduce the S22 parameter. However, in PDB-HEMT lower drain resistance is observed which is 13% lower than the GaN-HEMT as exhibited in **Figure 4.5(c)**, and higher channel resistance is observed which is 7% higher than the GaN-HEMT as shown in **Figure 4.7(b)**, which lead to increase

the S22 parameter, but the higher transconductance is observed in **Figure 4.5(d)** which is 30% higher than the GaN-HEMT and reduced the S22 parameter.

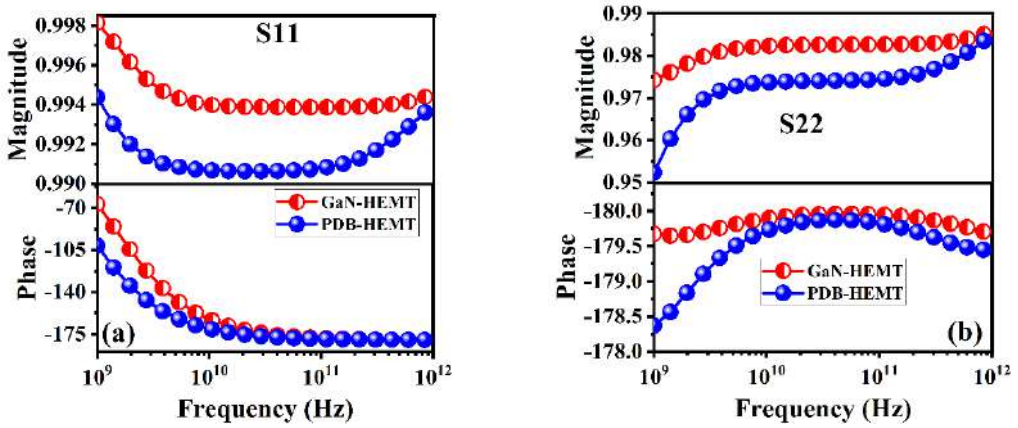

Fig. 4.4 (a) Input reflection coefficient S11 (b) Output reflection coefficient S22 for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023)*.

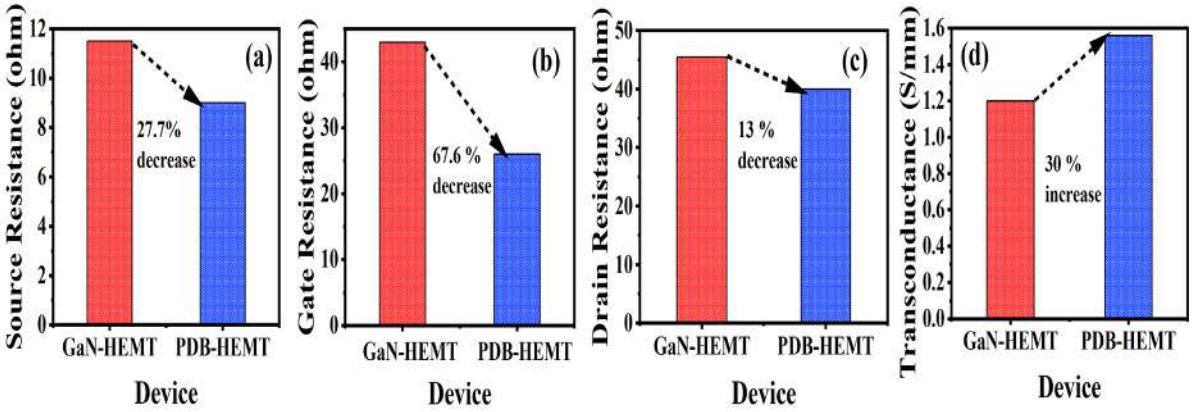

Fig. 4.5 Bar graph of (a) Source resistance (b) Gate resistance (c) drain resistance (d) Transconductance for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023)*.

The amount of feedback an amplifier receives from its output to its input is measured by the reverse isolation parameter S12, which affects the amplifier's supremacy in terms of its stability at high frequencies. The magnitude and phase change of the forward and reverse transmission coefficients (S21, S12) for both devices is exhibited in **Figure 4.6(a, b)**. For better RF performance, the S21 parameters should be high and the S12 parameter should be as low as possible to reduce the feedback of the output signal to the input port. **Figure 4.6(a)** shows the improvement in the S21 parameter for PDB-HEMT which is 69% higher than the GaN-HEMT. This enhancement is due to the polarization-doped buffer engineering in the proposed

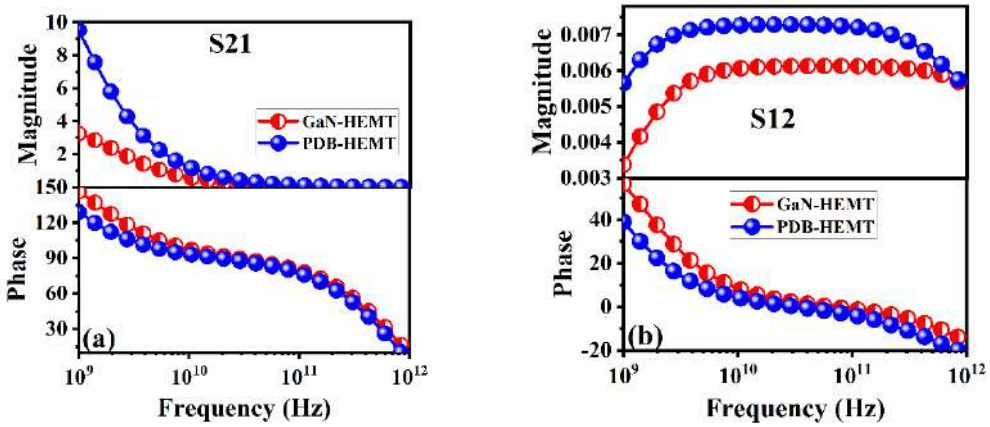

Fig. 4.6 (a) Forward transmission coefficient S21 (b) Reverse transmission coefficient S12 for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023*).

structure. The polarization-doped buffer engineering caused a negative polarization field in the buffer, which limited the electrons to a shallower depth range and enhanced gate controllability. Because of this, the transconductance increases, which ultimately leads to an improvement in the S21 parameter. However small increment in the S12 parameter is also observed for PDB-HEMT which is 8% higher than the GaN-HEMT as shown in **Figure 4.6(b)**.

Figure 4.7(a, b) exhibit the graph of parasitic capacitance i.e., gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and gate capacitance (C_{gg}) for both devices. The lower value of parasitic capacitances is observed for PDB-HEMT which enhances cut off frequency and maximum oscillation frequency of the device. **Figure 4.7(b)** exhibits the graph of channel resistance for both devices. It has been observed that in PDB-HEMT channel resistance increases by 7% as compared to GaN-HEMT.

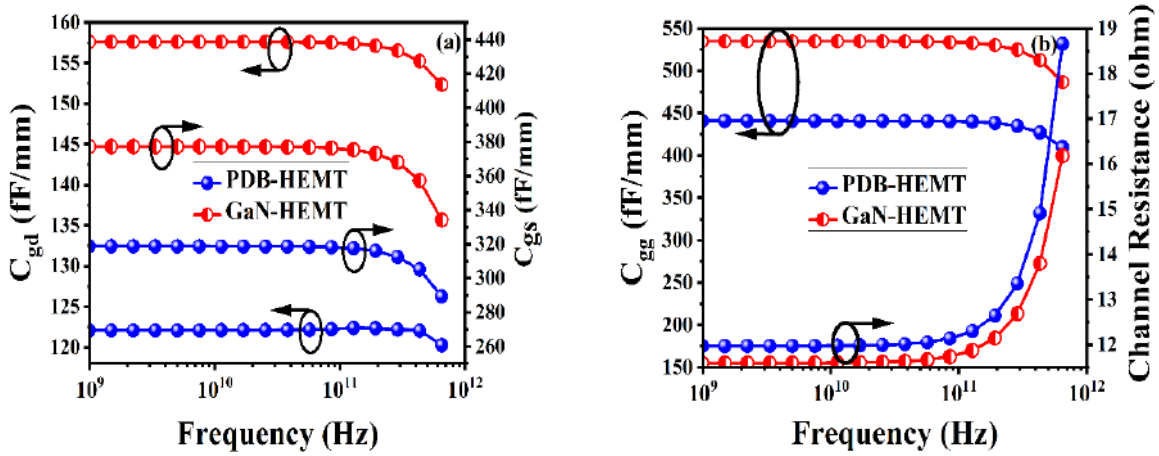

Fig. 4.7 Variation of (a) gate to drain and source capacitance (b) gate capacitance and channel resistance for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023*).

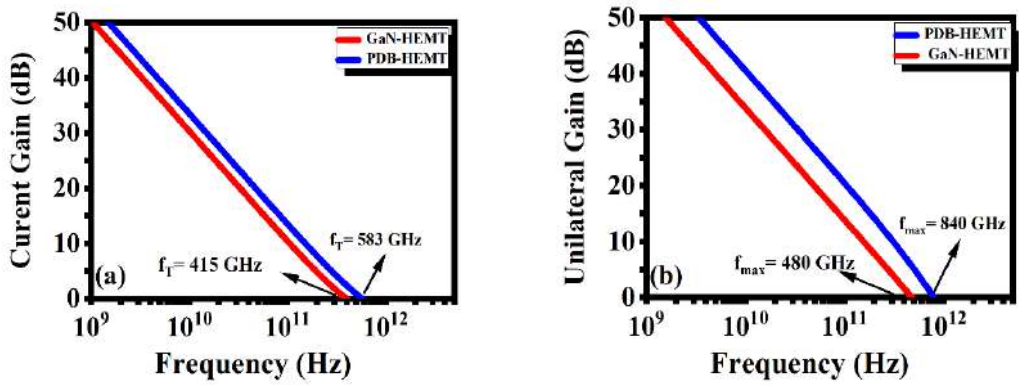

Fig. 4.8 Variation of (a) current gain (b) unilateral power gain for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023*).

This enhancement of channel resistance is due to the lower 2DEG density in PDB-HEMT. However, enhancement in channel resistance adversely affects the f_{max} of the device but a higher value of transconductance and lower parasitic capacitance overcome this effect. When the device's current and unilateral power gain are both unity, the device's f_T and f_{max} are calculated. The PDB -HEMT's f_T (583 GHz) and f_{max} (840 GHz) are displayed in **Figure 4.8(a, b)**, and they are 40% and 75% more efficient than the conventional device.

4.3.2 Noise Analysis

The two-port noisy network is often required to investigate internal sources of noise *(Van, 1969)*, as seen in **Figure 4.9**. It is possible to replace a linearly noisy two-port network with a noise-free network having a noise current and voltage source. There is a correlation between these two noise sources in real devices *(Hartmann and Strutt, 1973)*. The noise parameters of the general circuit are obtained from the measurement conducted on two-port networks. The

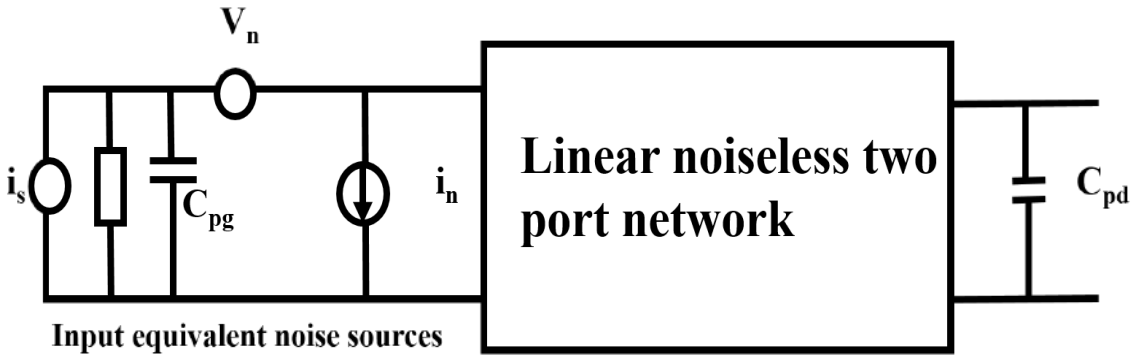

Fig. 4.9 The equivalent noise circuit *(Sharma et al., 2023*).

noise performance of the PDB-HEMT is examined with the help of the two port circuits by using the following parameters: NF_{min} (the least noise figure), the noise conductance (G_n), optimum source impedance (Z_{opt}), and the auto/cross-correlation function. The optimum source impedance (Z_{opt}) is the impedance that gives the minimum noise figure *(Gupta et al., 2022)*. Z_{opt} is a complex number that has both real and imaginary values, as expressed in Equation 4.2

$$Z_{opt} = R_{opt} + jX_{opt} \tag{4.2}$$

The real value of Z_{opt} is optimum source resistance (R_{opt}), and the imaginary part of Z_{opt} is optimum reactance (X_{opt}) as expressed by the Equations 4.3 and 4.4 *(Dubey et al., 2022)*. Where P and R are the noise coefficient and C_r is the correlation factor *(Takahashi et al., 2017)*.

$$R_{opt} = \frac{1}{\omega C_{gs}}\sqrt{\frac{g_m\left(R_{gs}+R_s\right)+R\left(1-C_r^2\right)}{P}}+\sqrt{\omega^2 C_{GS}^2\left(R_{gs}+R_s\right)^2} \tag{4.3}$$

$$X_{opt} = \frac{1}{\omega C_{gs}}\left(1-C_r\sqrt{\frac{R}{P}}\right) \tag{4.4}$$

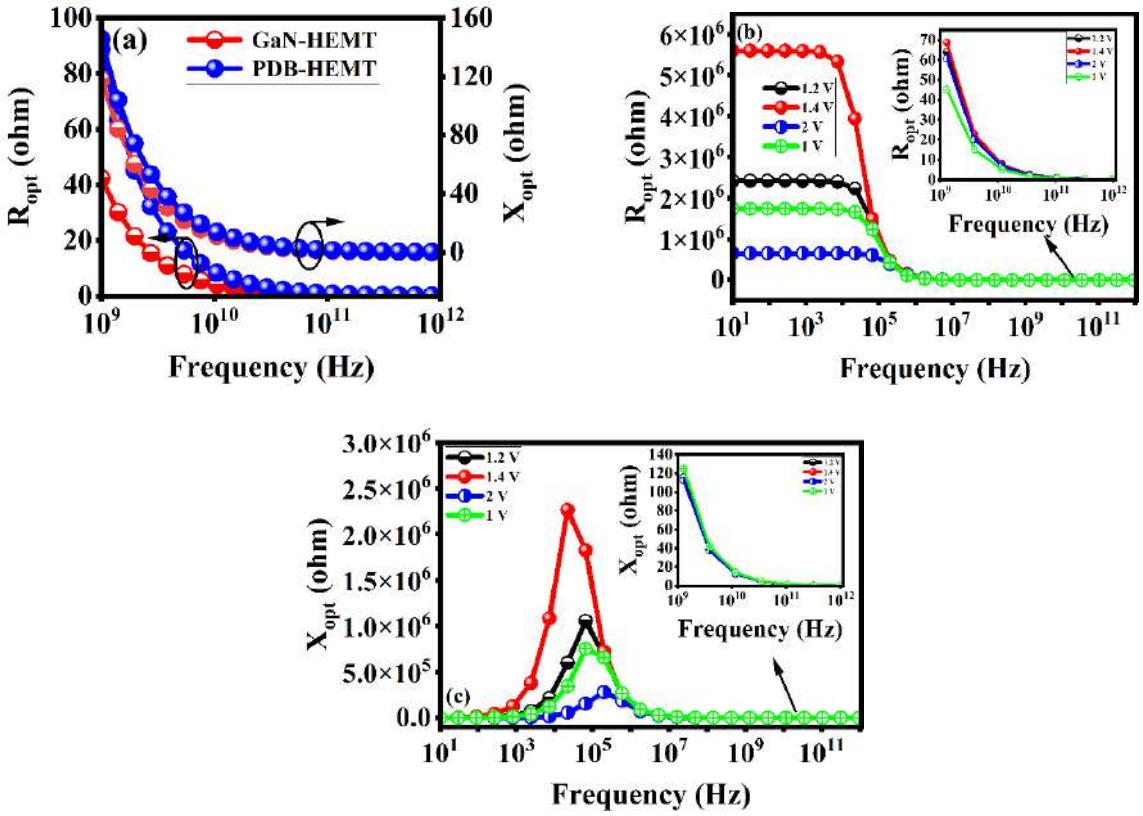

Fig. 4.10 (a) Optimum source resistance and reactance for PDB-HEMT and GaN-HEMT (b) optimum noise resistance (c) reactance for different V_{gs}. *(Sharma et al., 2023)*.

Figure 4.10(a) depicts the variation of R_{opt} and X_{opt} with frequency for both devices. The optimum source resistance and reactance value drop with increasing frequency and become saturated at a higher frequency. The impact of gate voltage on optimum source resistance (R_{opt}) and optimum reactance (X_{opt}) is depicted in **Figure 4.10(b, c)**. The optimum source resistance increases with gate voltage due to the enhancement of carrier concentration at the channel region. Moreover, R_{opt} is constant at the MHz frequency region and decreases at a greater frequency region, as depicted in **Figure 4.10(b)**. The inset graph of **Figure 4.10(b)** exhibited the optimum source resistance at a higher frequency region. The optimum reactance versus frequency for different gate voltages are exhibited in **Figure 4.10(c)**. At the lower frequency range, the optimum reactance increases with the frequency due to the recombination of charge carriers *(Ivanov et al., 2022*), and a higher peak of X_{opt} is observed for V_{gs} = 1.4V; after that, there is a downward swing in X_{opt}. The inset graph of **Figure 4.10(c)** shows the value of X_{opt} at a higher frequency range.

One of the essential metrics used to evaluate the performance of a low-noise amplifier (LNA) is noise conductance (G_n), expressed by Equation 4.5. Where S_I is the drain current noise spectral density, and T_a is the reference temperature 290K.

$$G_n = \frac{S_I}{4K_B T_a |Y_{21}|^2} \tag{4.5}$$

The power spectral densities of noise current generators are often estimated using noise conductance. RF and low-noise amplifiers (LNAs) need low-noise conductance *(Poornachandran et al., 2019*). The fluctuation of noise conductance with frequency for both devices is shown in **Figure 4.11(a)**. At 583 GHz frequency, the PDB-HEMT exhibits a lower noise conductance, which is 20% lower than the GaN-HEMT. **Figure 4.11(b)** shows how the gate voltage affects the noise conductance. The flat G_n response is observed at the lower frequency region and linearly increases at a higher frequency. The lower noise conductance is observed at V_{gs} = 1.4 V. The inset graph of **Figure 4.11(b)** shows the value of G_n at a higher frequency range. The mathematical expression of the noise figure for a two-port network is depicted by Equation 4.6 *(Lee et al., 2003*).

$$NF = NF_{min} + \frac{R_n}{G_s}(G_s - G_{opt})^2 + \frac{R_n}{G_s}(B_s - B_{opt})^2 \tag{4.6}$$

The optimal source susceptance and conductance are expressed by G_{opt} and B_{opt} *(Zhu et al.,*

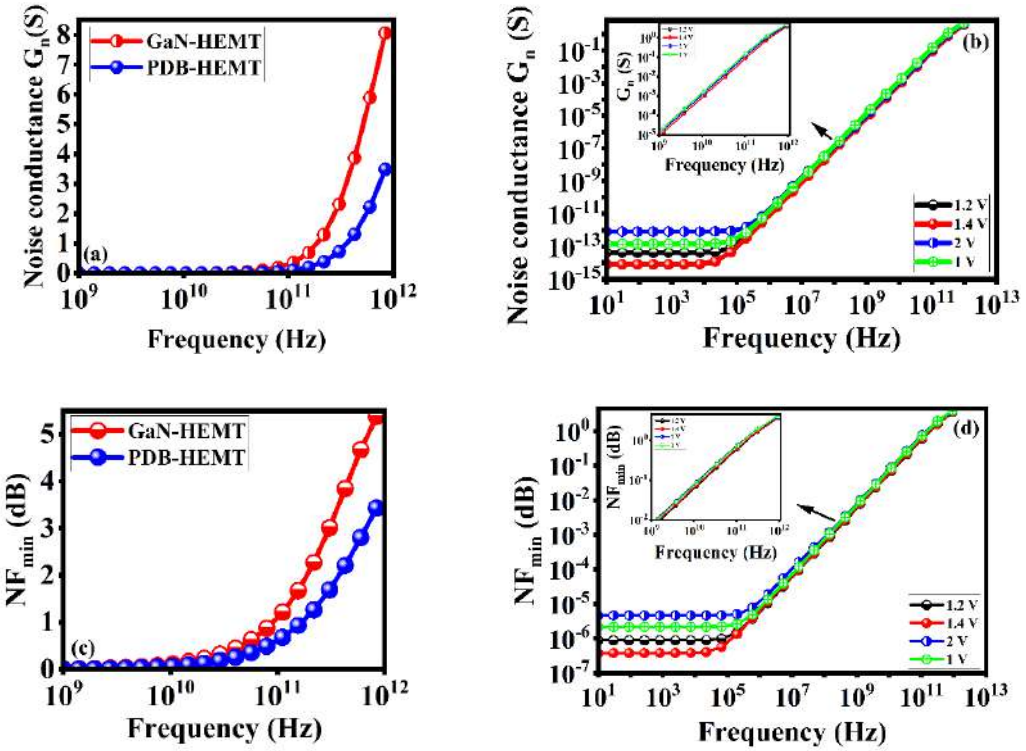

Fig. 4.11 Noise conductance (a) PDB-HEMT and GaN-HEMT (b) variable gate voltage; NF_{min} (c) PDB-HEMT and GaN-HEMT (d) variable gate voltage. *(Sharma et al., 2023)*.

2008). The minimum noise figure (NF_{min}) is obtained when $G_s = G_{opt}$ and $B_s = B_{opt}$. The frequency-dependent fluctuation of NF_{min} for both devices is shown in **Figure 4.11(c)**. The reduction in NF_{min} is noticed for PDB-HEMT compared to the conventional HEMT. The NF_{min} is inversely proportional to the transconductance. In PDB-HEMT, the graded buffer engineering caused a negative polarization field in the buffer, which limited the electrons to a shallower depth range and enhanced gate controllability. Because of this, the transconductance increases, leading to an improvement in the low noise figure compared to the conventional HEMT. The impact of gate voltage on the noise figure is exhibited in **Figure 4.11(d)**. It has been observed that at the MHz frequency range, NF_{min} is constant; at the GHz region, NF_{min} linearly increases with frequency. The NF_{min} value decreases with an increase in the gate voltage from 1 V to 1.4 V; the afterward higher value of NF_{min} is observed for V_{gs} = 2V. This variation in NF_{min} is basically due to the transconductance variation with gate voltage, as exhibited in **Figure 4.2**. The NF_{min} is the inverse of the transconductance. It is observed from **Figure 4.2** that transconductance increases with an increment in gate voltage from 1 V to 1.4 V, and a higher peak of transconductance is observed at V_{gs}= 1.4V afterward downward swing is observed. The inset graph of **Figure 4.11(d)** shows the value of NF_{min} at a higher frequency.

Figure 4.12 depicts the HEMT as a two-port device, with V1 representing noise generated at the gate and V2 representing noise received at the output *(Agarwala and Chaujar, 2012)*. A little statistical analysis is required for this study since noise is a random event. These two ports are examined in terms of autocorrelation and cross-correlation of their voltages. **Figure 4.13(a, b)** shows the cross-correlation (V1. V2) and autocorrelation between the input

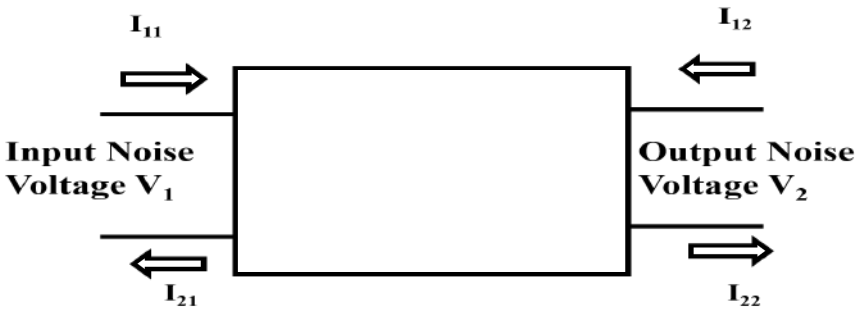

Fig. 4.12 Two-port device *(Sharma et al., 2023)*.

(V1. V1) and output voltages (V2. V2) for both structures. In contrast to the GaN-HEMT, the PDB-HEMT has a stronger auto/cross-correlation. The polarization-doped buffer in PDB-HEMT significantly bends the conduction band of the buffer layer upwardly convex. This enhances the carrier confinement in the channel and prevents the channel electrons from interacting with the traps in the buffer layer to reduce the trapping effects, which attribute to the enhancement of electron mobility and reduces the scattering. Therefore, the scattering mechanism in PDB-HEMT is inefficient in disrupting the correlation among the gate and drain current, significantly enhancing the auto/cross-correlation between them. The real and imaginary part of the cross-correlation of PDB-HEMT for V_{gs}= 1V, 1.2V, 1.4V, and 2V is

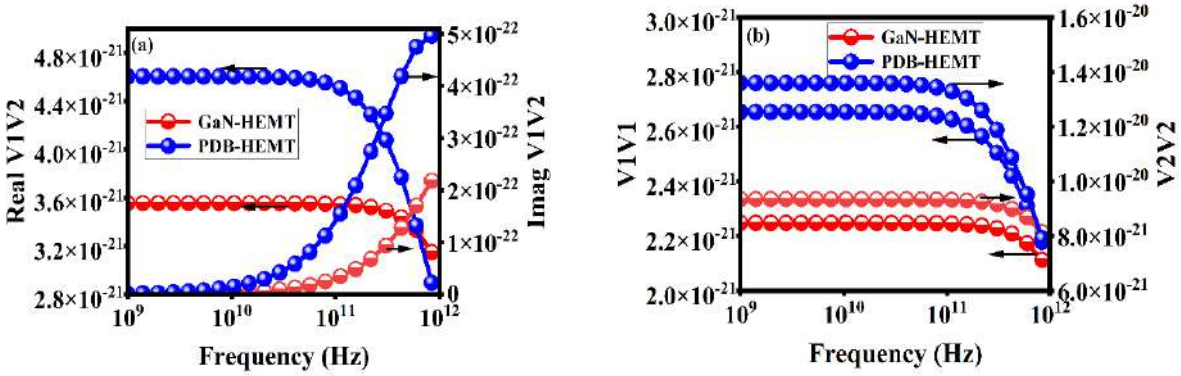

Fig. 4.13 (a) Cross-correlation (b) autocorrelation for GaN-HEMT and PDB-HEMT *(Sharma et al., 2023)*.

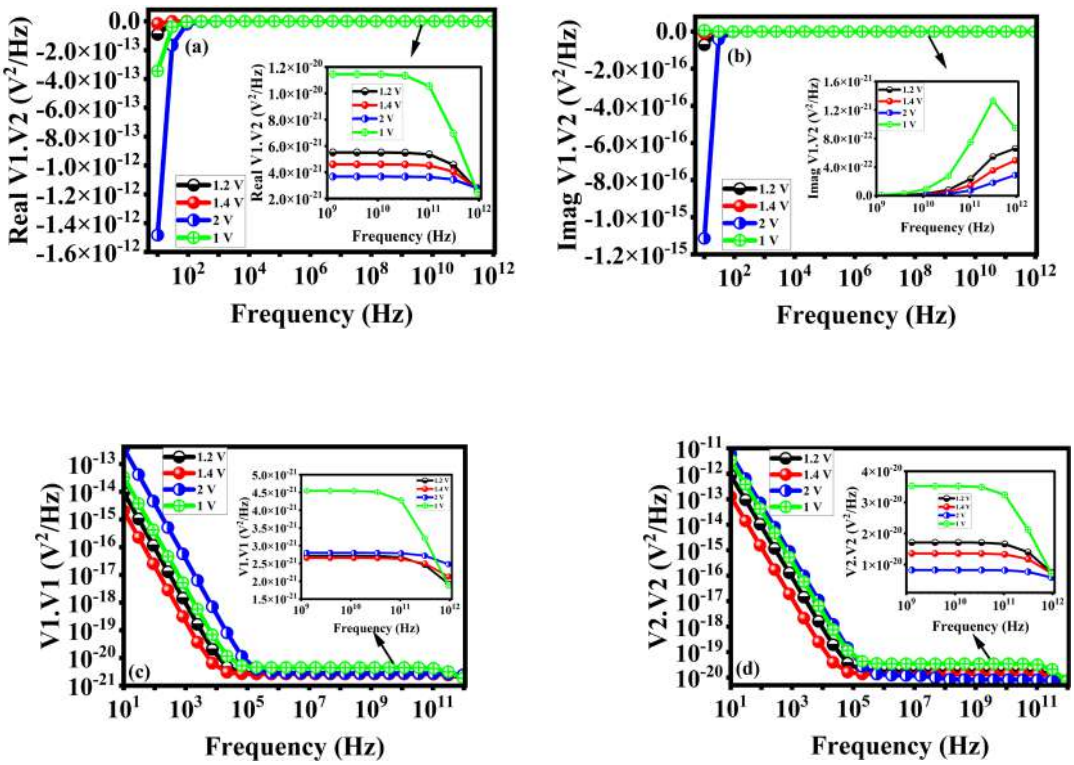

Fig. 4.14 For different gate voltage (a) real part of cross-correlation (b) imag part of cross-correlation (c) input (d) output autocorrelation. *(Sharma et al., 2023*).

exhibited in **Figure 4.14(a, b)**. The real part of cross correlation remains constant in the frequency range 1GHz to 100 GHz after that linear reduction is observed in the THz frequency region shown in inset graph of **Figure 4.14(a)**. The lower value of the cross-correlation function is observed for high gate voltage.

Figure 4.14(c, d) depicts the fluctuation of the auto-correlation function concerning the variation of the gate voltage (V_{gs}). The autocorrelation function falls linearly with lower order frequency (MHz) and stays constant with higher order frequency (GHz). The autocorrelation function reduces as the gate voltage (V_{gs}) of the PDB-HEMT increases. The inset graph of **Figure 4.14(c, d)** shows the value of auto-correlation function at higher frequency region. The linear reduction in autocorrelation function is observed in the THz frequency and lower value of the autocorrelation function is observed for high gate voltage.

Hence, this work's results show that using the polarized doped buffer in T-gate InAlN/GaN HEMT devices may achieve extremely low noise levels via improved structural design.

4.4 Summary

In this chapter, a T-gate E-mode HEMT with a polarization-doped buffer has been proposed, and a detailed Small signal and noise performance analysis has been developed. Results show that using a polarization-induced doped buffer engineering significantly enhance the transconductance by 30% and reduced the gate, source resistance by 67.6%, 27.7% which lead to a reduction in the reflection coefficients (S11, S22). Enhancement in transconductance further improved the forward transmission coefficient (S21) by 69% as compared to GaN-HEMT. Even at high frequencies, the PDB-HEMT device has a minimum noise figure of NF_{min}= 1.62 dB, lower noise conductance, and stronger auto/cross-correlation. These outstanding results show that PDB-HEMT is suitable for creating microwave amplifiers and oscillators. These findings make it abundantly evident that the T-gate PDB HEMT structure is an excellent candidate for high-performance RF applications and LNAs.

Although using the back barrier enhances the RF and noise performance of device, it also reduces the drain current density. Therefore, it is important to find a balance between RF performance and drain current density in device. The double channel engineering is the best way to enhance the drain current density of the device. In light of this, the next chapter will conduct an in-depth investigation into the double channel engineering on the T-gate shape HEMT with back barrier.

4.5 References

AGARWALA, A. and CHAUJAR, R. 2012. Investigation of frequency-dependent noise performance matrices for gate electrode work function engineered recessed channel MOSFET. *Technical Proceedings of the 2012 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2012*,38-41.

AMBACHER, O., FOUTZ, B., SMART, J., SHEALY, J., WEIMANN, N., CHU, K., MURPHY, M., SIERAKOWSKI, A., SCHA, W. and EASTMAN, L.2000. Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped Al-GaN/GaN heterostructures. *Journal of Applied Physics*,87,334-344.

CHANG, C. T., HSU, H. T., CHANG, E. Y., KUO, C. I., HUANG, J. C., LU, C. Y., and MIYAMOTO, Y. 2010. 30-GHz Low-Noise Performance of 100-nm-Gate-Recessed n-GaN/AlGaN/GaN HEMTs. *IEEE Electron Device Letters*,31,105-107.

CHEN, D., YUAN, P., ZHAO, S., LIU, S., XIN, Q., SONG, X., YAN, S., ZHANG, Y., XI, H., ZHU, W. and ZHANG, W. Wide-range-adjusted threshold voltages for E-mode AlGaN/GaN HEMT with a p-SnO cap gate. *Science China Materials*,65,795-802.

DUBEY, S. K., MISHRA, M. and ISLAM, A. 2022. Characterization of AlGaN/GaN based HEMT for low noise and high-frequency application. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*,35,e2932.

GUPTA, A. K., RAMAN, A. and KUMAR, N. 2022. Design Considerations and Optimization of Electrostatic Doped Ferroelectric Nanotube Tunnel FET: Analog and Noise Analysis. *Silicon*,14,10357-10373.

GUPTA, N. and CHAUJAR, R. 2016. Influence of gate metal engineering on small-signal and noise behavior of silicon nanowire MOSFET for low-noise amplifiers. *Applied Physics A*,122, 717-725.

HARTMANN, K. and STRUTT, M. J. O. 1973. Changes of the four noise parameters due to general changes of linear two-port circuits. *IEEE Transactions on Electron Devices*,20,874-877.

HASIRCI, Z., CAVDAR, I. H., and ÖZTÜRK, M. 2018. RLGC (f) modeling of a busbar distribution system via measured S-parameters atCENELEC and FCC bands. *Turkish Journal of Electrical Engineering and Computer Sciences*, *26*, 489-500.

HOSSAIN, E. and HASAN, M. 2015. 5G cellular: Key enabling technologies and research challenges. *IEEE Instrumentation & Measurement Magazine*,18, 11–21.

IVANOV, A. M., NENASHEV, G.V. and ALESHIN, A.N. 2022. Low-frequency noise and impedance spectroscopy of device structures based on perovskite-graphene oxide composite films," *Journal of Materials Science: Materials in Electronics*,33,21666–21676.

JENA, D., HEIKMAN, S., GREEN, D., ILAN, B., COFFIE, R., XING, H.G.,KELLER, S., DENBAARS, S., SPECK, J. AND MISHRA, U. K.2002. Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys. *Appl Phys. Lett.*,81,4395–4397.

KHAN, M. A., KUZNIA, J. N., VAN HOVE, J. M., PAN, N., and CARTER, J. 1992. Observation of a two-dimensional electron gas in low-pressure metalorganic chemical vapor deposited GaN-AlxGa1-xN heterojunctions. *Applied Physics Letters*,60,3027–3029.

KOBAYASHI, K. W. 2012. An 8-W 250-MHz to 3-GHz Decade-Bandwidth Low-Noise GaN MMIC Feedback Amplifier With > +51-dBm OIP3. *IEEE Journal of Solid-State Circuits*,47,2316-2326

KUMAR, A., TRIPATHI, M.M. and CHAUJAR, R.2018. In_2O_5Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications. *AEU - International Journal of Electronics and Communications*,93,233-241.

KUZMIK, J.2001. Power electronics on InAlN/(In)GaN: Prospect for a record performance. *IEEE Electron Device Letters*,22,510-512.

LEE, S, WEBB, K. J., TILAK, V. and EASTMAN, L.F. 2003. Intrinsic noise equivalent-circuit parameters for AlGaN/GaN HEMTs. *IEEE Transactions on Microwave Theory and Techniques*,51,1567–1577.

LIOU, J.J. and SCHWIERZ, F. 2003. RF MOSFET: recent advances, current status and future trends. *Solid-State Electronics*,47,1881–1885.

LIU, K., WANG, R., WANG, C., ZHENG, X., MA, X., BAI, J., CHENG, B., LIU, R., LI, A., ZHAO, Y. and HAO, Y.2022. The influence of lightly doped p-GaN cap layer on p-GaN/AlGaN/GaN HEMT. *Semiconductor Science and Technology*,37,075005.

MANUAL, A.U.S. 2016. *Silvaco . Santa Clara, CA*.

MISHRA, U. K., PARIKH, P. and WU, Y. F.2002. AlGaN/GaN HEMTs - An overview of device operation and applications. *Proc. IEEE,* 90, 1022–1031.

MOHANBABU, A., KUMAR, R. S., and MOHANKUMAR, N. 2017. Noise characterization of enhancement-mode AlGaN graded barrier MIS-HEMT devices. *Superlattices and Microstructures*, *112*, 604-618.

MOON, J. S., KANG, J., BROWN, D., GRABAR, R., WONG, D., FUNG, H., CHAN, P., LE, D. and MCGUIRE, C. 2016. Wideband linear distributed GaN HEMT MMIC power amplifier with a record OIP3/Pdc. *IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*,5-7.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J. 2017b. DC and microwave characteristics of Lg 50nm T-gate InAlN/AlN/GaN HEMT for future high power RF applications. *AEU - International Journal of Electronics and Communications*,77,163-168.

MURUGAPANDIYAN, P., RAVIMARAN, S. and WILLIAM, J.2017a. 30 nm T-gate enhancement-mode InAlN/AlN/GaN HEMT on SiC substrates for future high power RF applications.*Journal of Semiconductors*,38, Issue 8,084001.

PAMPILI, P. and PARBROOK, P.J.2017. Doping of III-nitride materials.*Mater. Sci. Semicond. Process.*,62,180–191.

POORNACHANDRAN, R., MOHANKUMAR, N., SARAVANAKUMAR, R. and SUJATAH, G. 2019. Analysis of microwave noise in an enhancement-mode dual-quantum-well InAs HEMT. *Journal of Computational Electronics*,18**,**1280–1290.

SANO, S., EBIHARA, K., YAMAMOTO, T., SATO, T. and MIYAZAWA, N.2018. GaN HEMTs for wireless communication.*SEI Tech. Rev.*, 86,65–70.

SHARMA, M., KUMAR, B., and CHAUJAR, R. 2023. Small signal and noise analysis of T-gate HEMT with polarization doped buffer for LNAs. *Micro and Nanostructures*, *180*, 207593.

SHINOHARA, K., REGAN, D. C., TANG, Y., CORRION, A. L., BROWN, D. F., WONG, J. C., ROBINSON, J. F., FUNG, H. H., SCHMITZ, A., OH, T. C., KIM, S. J., CHEN, P. S., NAGELE, R. G., MARGOMENOS, A. D., and MICOVIC, M. 2013.Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications," *IEEE Transactions on Electron Devices*,60,2982-2996.

SUN, H., ALT, A. R., BENEDICKTER, H. and BOLOGNESI, C. R. 2009. High-Performance 0.1- μm Gate AlGaN/GaN HEMTs on Silicon With Low-Noise Figure at 20 GHz. *IEEE Electron Device Letters*,30,107-109.

SUN, H., ALT, A. R., BENEDICKTER, H., FELTIN, E., CARLIN, J. F., GONSCHOREK, M., GRANDJEAN, N. R. and BOLOGNESI, C. R. 2010. 205-GHz (Al,In)N/GaN HEMTs. *IEEE Electron Device Letters*,31,957-959

TAKAHASHI, T., HATSUSHIBA, S., FUJIKAWA, S., and FUJISHIRO, H.I. 2017. Comparative study on noise characteristics of As and Sb-based high electron mobility transistors. *Physica Status Solidi (a)*,214**,**1600599.

UREN, M. J., MOREKE, J., and KUBALL, M. 2012. Buffer design to minimize current collapse in GaN/AlGaN HFETs. *IEEE Transactions on Electron Devices*, 59, 3327-3333.

VAN DER ZIEL, A. 1969. Representation of noise in linear two-ports. *Proceedings of the IEEE*, vol. 57,1211-1211.

ZHANG, X., JIA, K., WANG, Y., FENG, Z. and ZHAO, Z.2013.AlNGaN HEMT T- gate Optimal Design," *Proceedings of the 2nd International Symposium on Computer, Communication, Control and Automation (ISCCCA),*845-847.

ZHU, Y., WEI, C., KLIMASHOV, O., LI, B., ZHANG, C. and TKACHENKO, Y. 2008 Gate width dependence of noise parameters and scalable noise model for HEMTs. *European Microwave Integrated Circuit Conference,* Amsterdam,298–301.

CHAPTER 5

Design and Investigation of E-Mode-T-Gate Double Channel HEMT with InGaN Back Barrier for Enhanced Performance

This chapter discusses the design and analysis of E-mode T-gate double-channel High Electron Mobility Transistor (HEMT) with an InGaN back barrier. The insertion of the AlN layer below the InAlN/GaN interface results in the formation of the double channel, which in turn results in an increase in the drain current density of 2.5 A/mm. However, due to a lack of gate controllability over a lower channel, the high leakage current is observed in double channel HEMT. This issue has been addressed by using the InGaN as a back barrier, which improves the carrier confinement of 2DEG by raising the conduction band for the GaN buffer and considerably improves the gate controllability over a lower channel. The performance of the proposed device is compared with that of conventional double-channel HEMTs. Various performance parameters, such as drain current (I_{ds}), transconductance (g_m), intrinsic gain (A_v), output conductance (g_d), early voltage (V_{EA}), TGF, parasitic capacitances (C_{gs}, C_{gd}), cut-off frequency (f_T), maximum oscillation frequency (fmax), gain frequency product (GFP), transconductance frequency product (TFP), and gain transconductance frequency product (GTFP), are investigated. Furthermore, the improvement in linearity parameters such as VIP2, VIP3, IIP3, 1-dB compression point has been observed by varying the back barrier distance from the lower channel.

5.1 Introduction

III-Nitride-based HEMTs (High Electron Mobility Transistors) have been gaining significant attention in recent years for their use in high-power RF (Radio Frequency) applications. The GaN material used in these HEMTs exhibits a higher power output density compared to GaAs at high-frequency operations due to its larger bandgap, higher saturation velocity, and higher electron mobility *(Mishra et al., 2002, Frayssinet et al., 2000)*. Several research papers have been published to enhance the performance of AlGaN/GaN HEMTs *(Feng et al., 2004, Lin et al., 2004)*, which are used in high-power applications such as radar, satellite communication, and 5G cellular networks. To enhance the RF characteristics of GaN HEMTs, it is essential to scale down the device dimension. As the device dimensions are reduced, the parasitic capacitances (C_{gs} and C_{gd}) that occur between the gate and the source/drain regions decrease, resulting in an improvement in the RF parameters. Researchers have been looking at several ways to shorten the gate length in order to overcome this issue. However, the lattice mismatch between the AlGaN and GaN junction presents an additional difficulty. Due to the lattice mismatch, strain is always induced when a thin AlGaN barrier layer is utilised in the device. To address this issue, researchers have started using an InAlN layer instead of the AlGaN barrier layer. The InAlN layer has a lattice match with the GaN layer when the Al composition in the InAlN layer is 0.83 *(Neuburger et al., 2004*) as discussed in **Chapter 2**.

T-gate single-channel HEMTs with various kinds of buffer and back-barrier engineering have previously been the subject of a significant amount of research and development. *Lee et al., 2011a* demonstrated a passivated Al_2O_3 layer on a 65 nm gate length HEMT with a back-barrier layer. This HEMT exhibited a drain current of 1.49 A/mm and a transconductance (g_m) of 539 mS/mm. The use of Al_2O_3 as a passivation layer provides a high-quality surface with low interface state density, which results in improved device performance. *Adak et al., 2014* designed a 150 nm gate length HEMT with a p-GaN back barrier. This device recorded a drain current density of 1.24 A/mm and a g_m of 589 mS/mm. *Han et al., 2018* designed a 70 nm gate length HEMT with a graded buffer. This device recorded a drain current of 1.4 A/mm.

The impact of polarization doped buffer back barrier engineering on RF and noise performance is already discussed in **Chapter 3** and **Chapter 4.** It has been observed that by inserting the back barrier below the channel layer reduces the drain current density. Hence, it is important to find a balance between RF performance and drain current density in HEMTs.

Double-channel HEMTs (DC-HEMT) *(Zhang et al., 2017, Chugh et al., 2018)* have recently emerged as a better alternative to single-channel HEMT. The DC-HEMT engineering involves the two heterointerfaces, which creates two channels in the device. This unique feature of DC-HEMTs makes them suitable for radio frequency (RF) circuit design because of their high current drivability *(Jha et al., 2008, Chu et al., 2005)*. The AlGaN/GaN double heterojunction HEMT demonstrated by *Ravikiran et al., 2015* has an excellent frequency response of f_T/f_{max} 22/25 GHz, exhibits great potential in high-frequency electronic applications. Despite the advantages of the DC-HEMT, it has some limitations.

The poor confinement of 2DEG and poor gate controllability over the lower channel are the primary challenges that need to be addressed. In order to improve the confinement of 2DEG, buffer engineering is required. The InGaN back barrier engineering is one of the most effective buffer engineering which enhance the 2DEG confinement and reduce the short channel effect *(Lee et al., 2011b, Palacios et al., 2005)*. The poor gate controllability over the lower channel is another major challenge with DC-HEMTs. This issue can be solved through gate-recessed engineering, which enhances the gate controllability over the lower channel and shifts the threshold voltage towards the positive side.

In this chapter, we thoroughly examine both analog and RF performance characteristics exhibited by a DC-BB-HEMT (double channel T-gate HEMT with InGaN back barrier). This chapter place particular emphasis on closely analysing how certain device parameters are impacted upon by introduction of an InGaN back-barrier layer. Additionally, a careful investigation has been done on the linearity parameters of the device with variable back barrier distance from lower channel.

The following outline constitutes this chapter's structure: Section II of this chapter provides an overview of the device construction. Section III of the chapter discusses the results obtained through simulation. These results include the analog and RF performance of DC-BB-HEMT and DC-HEMT. The impact of back-barrier distance on linearity parameters also investigates in the result section. The conclusion of the chapter is presented in the final part of the chapter's summary.

5.2 Device Structure

Figure 5.l exhibits the schematic structure of recessed 70 nm T- gate InAlN/AlN DC-BB-HEMT. All the parameters used in the structure are defined in **Table 5.1**. The Al_2O_3 layer passivates the device to reduce the parasitic capacitance. The source and drain regions are doped with Si of order 10^{20} cm^{-3} to reduce the contact resistance. The first AlN layer placed below the InAlN layer enhances the mobility of 2DEG. The second AlN layer is placed at a distance of 10 nm from the first AlN layer. The second AlN layer formed the second triangular quantum well at the interface of AlN (2)/GaN and formed the second channel. The 2 nm InGaN back barrier layer is placed below the lower channel to enhance the 2DEG confinement This layer improves the performance of the device by reducing the leakage current and increasing the breakdown voltage. The layer is also responsible for providing a high potential barrier for the 2DEG, which helps to prevent its spilling in the buffer region. Overall, the design of the recessed 70 nm T-gate InAlN/AlN DC-BB-HEMT is optimized to achieve high performance for specific applications. The combination of the different layers and regions results in a device that exhibits high mobility, low contact resistance, and reduced parasitic capacitance. The models used to simulate the device are the same as discussed in **Chapter 2**.

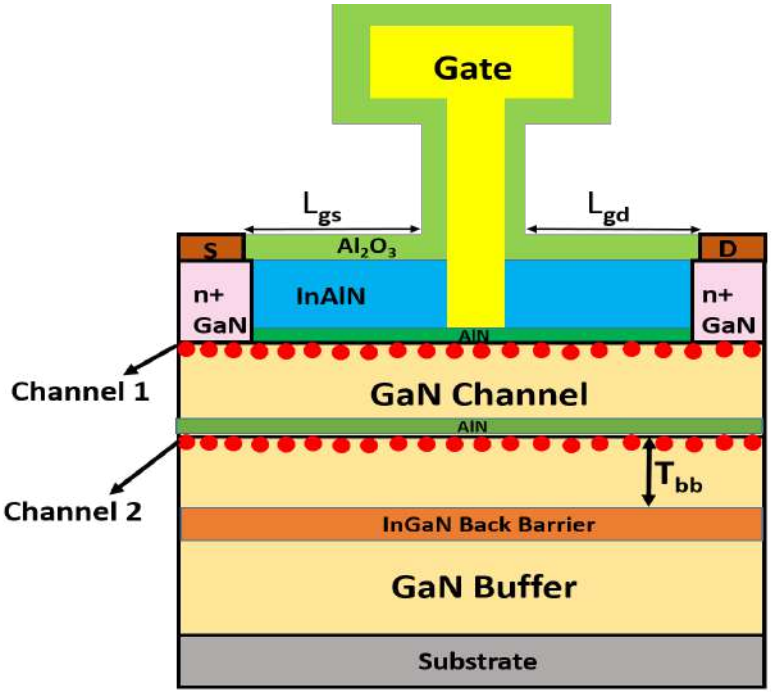

Fig. 5.1 Proposed T-gate Double channel back barrier HEMT (DC-BB-HEMT) ***(Sharma and Chaujar, 2021*****).**

TABLE 5.1

DESIGN PARAMETERS OF DC-BB-HEMT AND DC- HEMT *(SHARMA AND CHAUJAR, 2021)*

Device Parameter	DC-HEMT	DC-BB-HEMT
Gate length (L_g)	70 nm	70 nm
Al_2O_3 passivation layer	10 nm	10 nm
Distance b/w two channels	10 nm	10 nm
Distance b/w lower channel and back barrier (T_{bb})	30 nm	30 nm
Source to gate length (L_{gs})	400 nm	400 nm
Gate to drain length (L_{gd})	1.5 µm	1.5 µm
Barrier layer (InAlN)	10 nm	10 nm
AlN layer	1 nm	1 nm
InGaN back barrier	-	2 nm
GaN buffer	1.5 µm	1.5 µm
Source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Gate width	2×50 µm	2×50 µm
Gate stem height	100 nm	100 nm
Gate head	400 nm	400 nm

5.3 Results and Discussion

5.3.1 Band Diagram and Electron Concentration

This subsection focuses on the conduction band discontinuity and electron concentration of DC-BB-HEMT and DC-HEMT. As shown in **Figure 5.2**, both devices have a conduction band

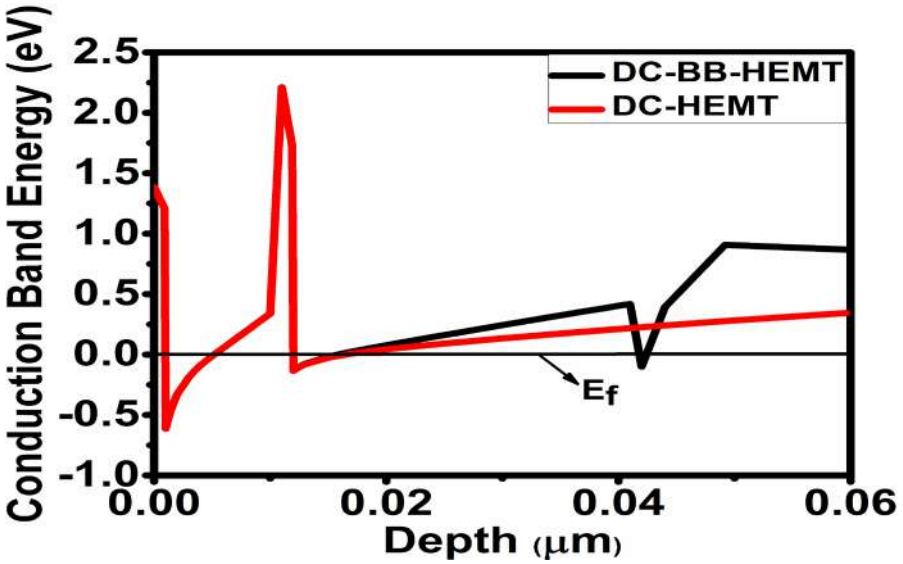

Fig. 5.2 Conduction band diagram of DC-BB-HEMT & DC-HEMT *(Sharma and Chaujar, 2021)*.

diagram with two quantum wells, namely the primary quantum well and the secondary quantum well. The primary quantum well is formed at the interface of AlN (1)/GaN and has a relatively deeper quantum depth, which generates the major upper channel region and accumulates the highest electron concentration. On the other hand, the second quantum well is formed at the interface of AlN (2)/GaN, which generates the second channel. The DC-BB-HEMT, in particular, has a unique feature where a sharp notch is formed at the back of the lower channel. This notch is created by the induced polarization charges between the InGaN and GaN, which raises the potential barrier and confines the electrons in the channel region. This confinement enhances the gate controllability over the lower channel, leading to better device performance.

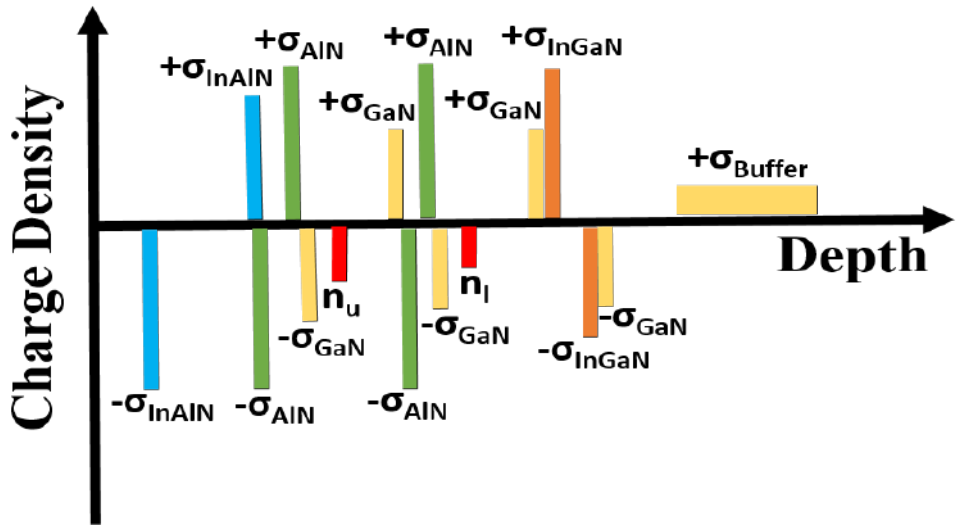

Fig. 5.3 Polarization Charge distribution of each layer in DC-BB-HEMT *(Sharma and Chaujar, 2021)*.

Figure 5.3 displays the charge distribution of a DC-BB-HEMT. In this device, piezoelectric and spontaneous polarization charges are induced at the interface of different layers. The polarization effect causes the accumulation of negative and positive charges on each layer's opposite sides. The values of these polarization charges are calculated using Equation 1.7 in **Chapter 1**.

The contour plot of the electron concentration is shown in **Figure 5.4(a, b)**, respectively, for DC-HEMT and DC-BB-HEMT. It has been observed that the concentration of electrons is larger at the AlN (1)/GaN interface which generates the main channel, whereas the AlN (2)/GaN interface forms the minor channel. As compared to the DC-HEMT, the DC-BB-HEMT exhibits a lower electron concentration at the AlN (2)/GaN. This decrease in electron concentration may be due to the insertion of an InGaN layer, which prevents the spilling of

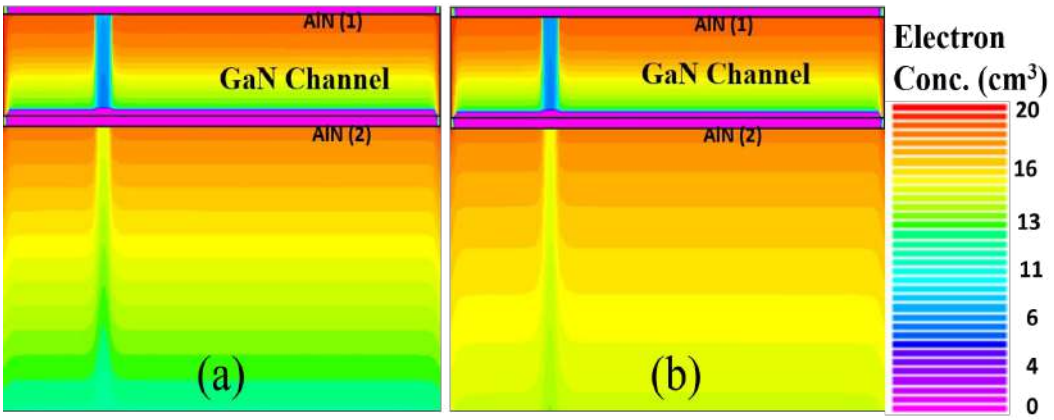

Fig. 5.4 Electron concentration Contour plot of (a) DC-BB-HEMT (b) DC-HEMT. *(Sharma and Chaujar, 2021*).

electron in the buffer layer, hence improving electron confinement and resulting in a lower overall electron concentration.

5.3.2 DC and Analog Performance

This subsection aims to evaluate the DC and analog performance of the proposed device (DC-BB-HEMT) and compare it with the conventional device (DC-HEMT). **Figure 5.5** shows the drain current characteristics for both devices. Initially, due to the lack of gate controllability over channel 2 in DC-HEMT, channel 2 remains in an ON state, and a negative threshold voltage is observed. As the gate voltage is increased, channel 1 is turned on, which is the primary channel with a higher 2DEG density. Once channel 1 is turned on, it screens channel 2 and saturates the 2DEG in channel 2. The presence of the InGaN back barrier in DC-BB-

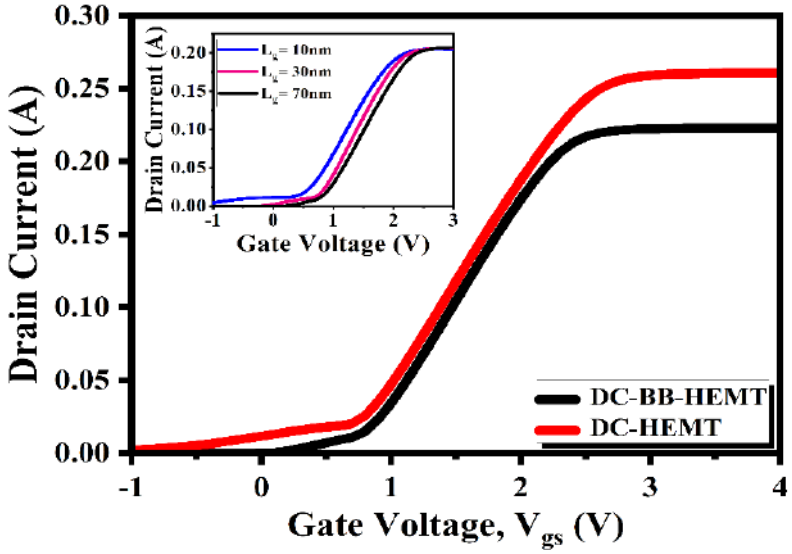

Fig. 5.5 Drain Current Characteristics of DC-BB-HEMT & DC-HEMT *(Sharma and Chaujar, 2021*).

HEMT enhances the 2DEG confinement, improves the gate controllability over channel 2, and shifts the threshold voltage significantly toward the positive side. At V_{gs} = 3V, the drain current density obtained in DC-BB- HEMT is 2.2A/mm, which is approximately 16.6% lower than that of DC-HEMT (2.59A/mm). This decrease in current density is due to the threshold voltage shift of DC-BB-HEMT (0.3V) toward the positive side, which is about 1.5V higher than that of DC-HEMT (-1.8V). The inset graph of **Figure 5.5** shows the drain current characteristics for different gate lengths for DC-BB- HEMT. It has been observed that at a gate length of 10 nm, the device exhibits an "on" state when V_{gs} = 0V. However, as the gate length increases to 70 nm, the device demonstrates E-mode characteristics. As a result, to ensure optimal E-mode performance of the device, we adhere to the 70 nm gate length.

This subsection also evaluates the analog parameters, including transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), early voltage (V_{EA}), and intrinsic gain (A_v), for the proposed device and compares them to those of the conventional device. The mathematical formulations of these parameters, as shown below *(Kumar and Chaujar, 2021a)*, are crucial for analog applications.

$$g_m = \partial I_d / \partial V_{gs} \tag{5.1}$$

$$TGF = g_m / I_d \tag{5.2}$$

$$g_d = \partial I_d / \partial V_{ds} \tag{5.3}$$

$$V_{EA} = I_d / g_d \tag{5.4}$$

$$A_v = g_m / g_d = (g_m / I_d) \times V_{EA} \tag{5.5}$$

Figure 5.6(a) shows the plot of transconductance with gate bias for both devices. Transconductance is defined as the change in the drain current to the gate voltage at constant drain voltage. In **Figure 5.6(a)**, double peaks, i.e., primary and secondary peaks, have been observed in the transconductance graph due to the formation of two channels. The higher primary peak is observed for the DC-BB-HEMT at V_{gs} = 0.8 V due to the improvement of electron confinement and gate controllability for channel 2 by the InGaN back barrier. Simultaneously, the secondary peak for both devices is comparable, which shows that the presence of the InGaN back barrier does not affect channel 1. **Figure 5.6(b)** exhibits the plot of the transconductance generation factor (TGF) for both devices. TGF is the ratio of

transconductance and drain current. It is a crucial factor in the analog application. TGF is the gain available per unit power dissipation *(Pardeshi, 2015, Chaujar et al., 2008)*, where g_m represents the gain and drain current represents the dissipated power. The smaller the value of TGF, the lower will be the input drivability, which dissipated the high power at the capacitative load circuit. In **Figure 5.6(b)**, it can be seen that at lower V_{gs} high peak of TGF is attained for DC-BB-HEMT (32 V^{-1}), which is about 10 times higher than the DC-HEMT (1.73 V^{-1}). As the gate voltage increases, the value of TGF is reduced severely due to the increment of drain current at high gate bias.

Figure 5.6(c) shows the plot of intrinsic gain with gate bias. The high peak of intrinsic gain for DC-BB-HEMT (4 dB) observed at V_{gs} = 1.5 V. Intrinsic gain depends on two factors: transconductance and output conductance. The decrement of output conductance significantly enhances the intrinsic gain of about 50% in the proposed device. **Figure 5.6(d)** shows the variation of early voltage with gate bias for both devices. Early voltage is another analog parameter which is the ratio of drain current and output conductance. For better analog

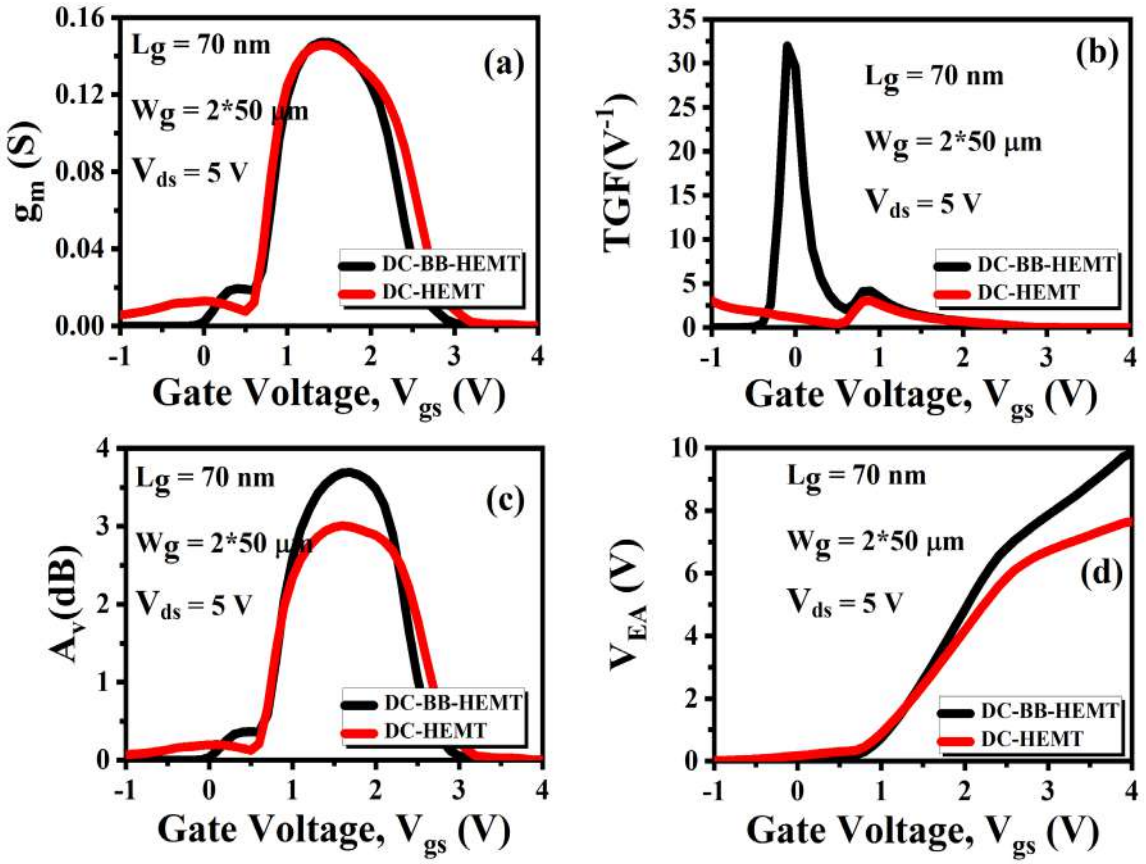

Fig. 5.6 (a) Transconductance (b) TGF (c) Intrinsic gain (d) Early voltage for both devices. *(Sharma and Chaujar, 2021)*.

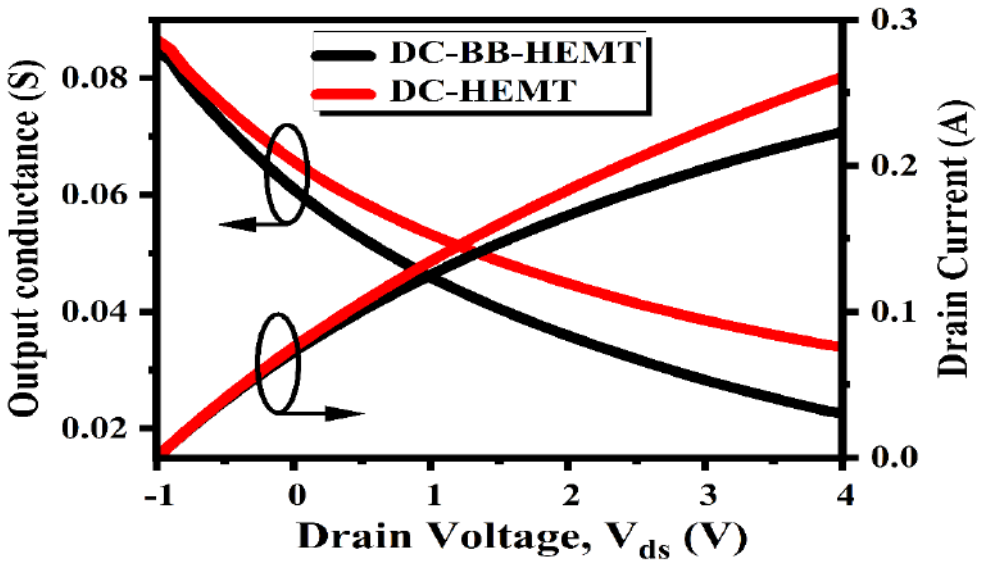

Fig. 5.7 Output conductance of DC-BB-HEMT & DC-HEMT *(Sharma and Chaujar, 2021)*.

performance, both intrinsic gain and early voltage should be high. The higher value of early voltage is obtained for DC-BB-HEMT (10V), which is about 53% higher than the DC-HEMT (6.5V). This increment in the early voltage is due to the lower output conductance, which enhances the proposed device's analog parameters. The plot of output conductance for DC-BB-HEMT and DC-HEMT with drain bias is shown in **Figure 5.7**. Output conductance calculates the driving ability of the device. The higher value of output conductance is observed at lower drain voltage. As the V_{ds} increase, the output conductance is decreased exponentially. Due to the higher gate controllability, minimum output conductance is observed for DC-BB-HEMT as compared to DC-HEMT.

5.3.3 RF Performance

In this subsection, small-signal AC analysis has been conducted for DC-BB-HEMT and DC-HEMT - at an operating frequency of 1 MHz. The purpose of this analysis is to investigate various RF parameters of these HEMTs, including f_T, f_{max}, GFP, GTFP, and TFP. The mathematical formulation of these parameters is listed below *(Chaujar et al., 2008).*

$$f_T \approx g_m / 2\pi(C_{gs}+C_{gd}) \tag{5.6}$$

$$f_{max} = f_T / \sqrt{4R_g(g_{ds}+2\pi f_T C_{gd})} \tag{5.7}$$

$$GFP = (g_m/g_d) \times f_T \tag{5.8}$$

$$TFP = (g_m/I_d) \times f_T \quad (5.9)$$

$$GTFP = (g_m/g_d) \times (g_m/I_d) \times f_T \quad (5.10)$$

Figure 5.8(a, b) exhibit the plot of the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) with gate bias. For better RF performance, these parasitic capacitances should be low. At lower gate voltage, there is a slow increment in C_{gs} and C_{gd}, but at higher gate bias, there is a quick increment in C_{gs} and C_{gd} due to the enhancement of the lateral electric field, which increases the carrier movement from the drain to the source side. The DC-BB-HEMT shows a lower value of C_{gs} and C_{gd} in comparison to the DC-HEMT. At the metal/InAlN interface, charges increase due to the higher sheet charge density in the quantum well, which enhances the capacitance for DC-HEMT.

Figure 5.8(c) shows the plot of cut-off frequency (f_T) with gate bias. The cut-off frequency is defined as the frequency at which current gain reduces to unity. From Equation 5.6, it is seen that f_T depends upon transconductance and parasitic capacitance. The double peak structure

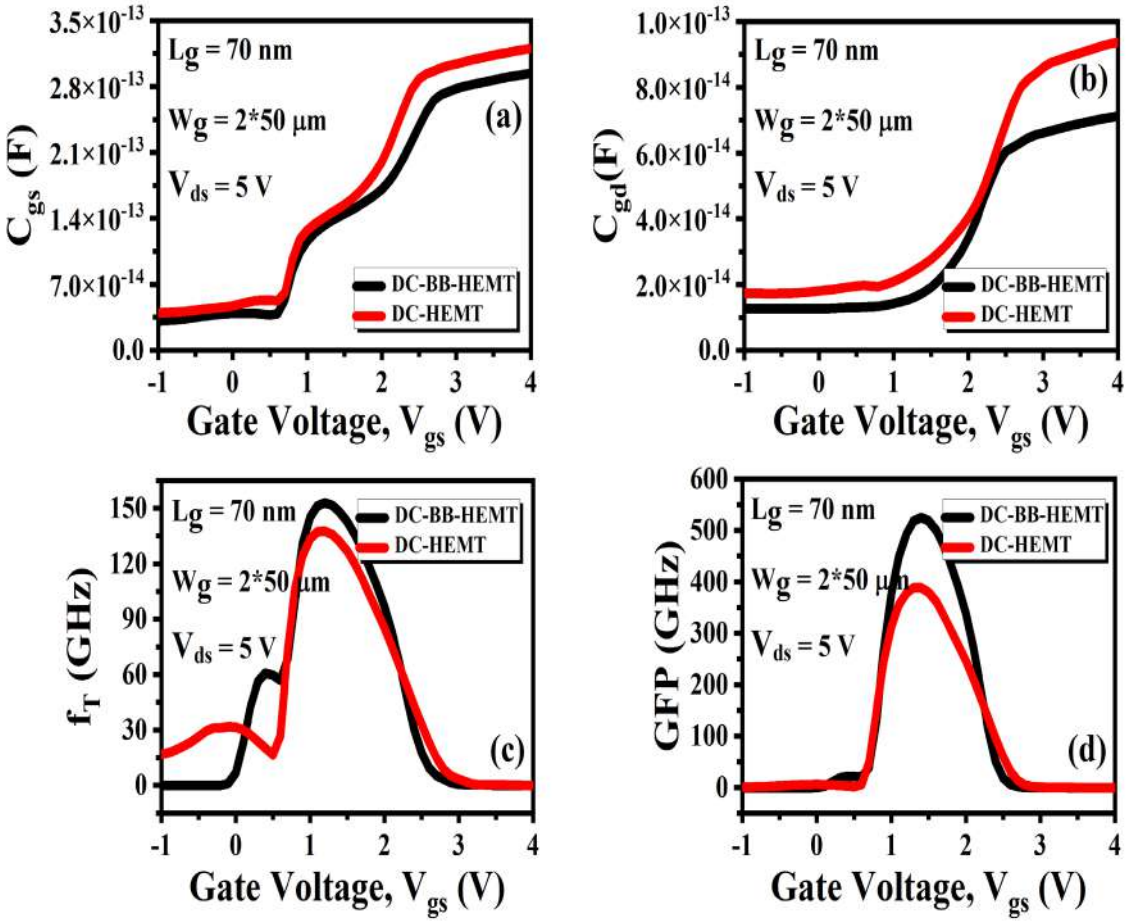

Fig. 5.8. Variation of (a) C_{gs} (b) Cgd (c) f_T (d) GFP for both devices. *(Sharma and Chaujar, 2021)*.

has been observed, the same as the transconductance curve **Figure 5.6(a)**. The primary and secondary peaks are formed due to channel 2 and channel 1. The InGaN back barrier's presence increases the primary transconductance peak, which further enhances the cut-off frequency. The secondary transconductance peak is not affected by the InGaN back-barrier, but the parasitic capacitance for the DC-BB-HEMT is lower, enhancing the cut-off frequency. The cut-off frequency obtained for DC-BB-HEMT (153 GHz) is 11.7% higher than the DC-HEMT (136 GHz). In **Figure 5.8(d)**, the gain frequency product (GFP) has been plotted against the gate bias. The GFP is another essential parameter for high-frequency applications. Initially, with increasing the gate voltage, GFP increases linearly and holds an optimum value, after that, it decreases in the saturation region. The higher peak of GFP obtained for DC-BB-HEMT is 526 GHz which is about 35.2% higher than the DC-HEMT (389 GHz). GFP improvement in DC-BB-HEMT is mainly due to the improvement in cut-off frequency, transconductance, and reduction of output conductance.

Variation of the drain to source conductance (g_{ds}) and maximum oscillation frequency (f_{max}) with gate bias is shown in **Figure 5.9(a, b)**, respectively. The maximum oscillation frequency is

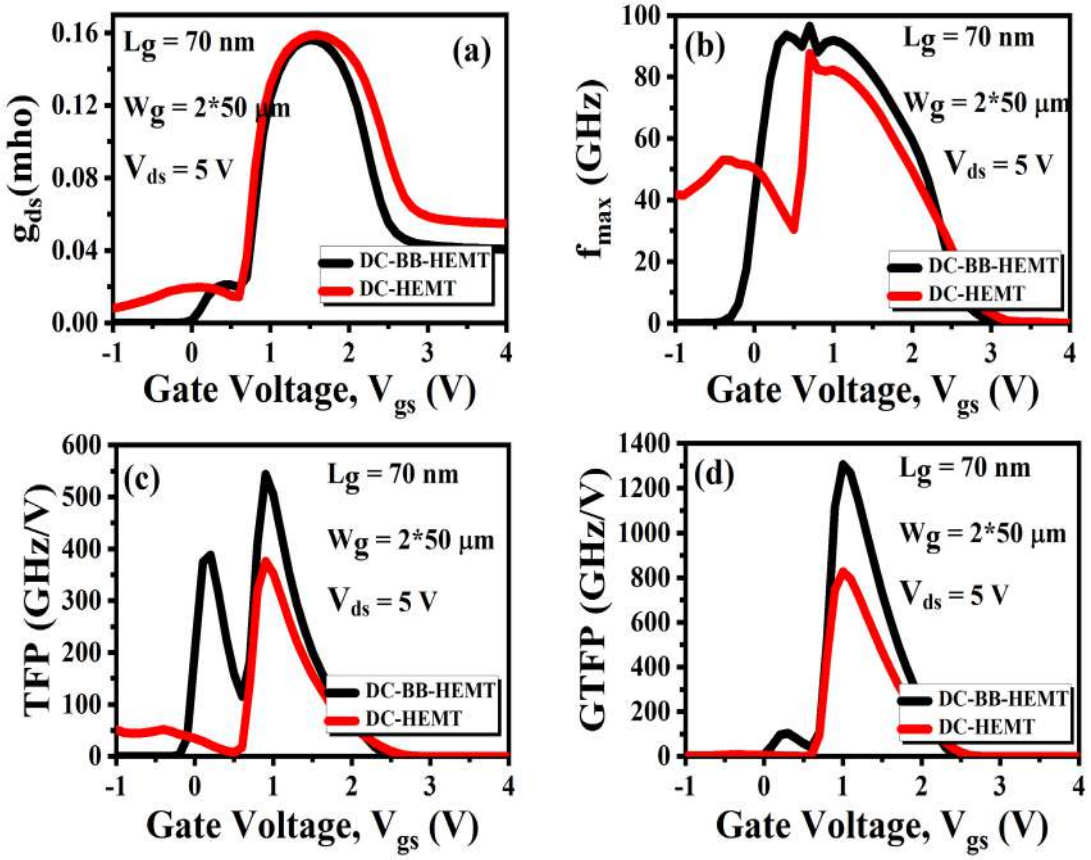

Fig. 5.9. Variation of (a) g_{ds} (b) f_{max} (c) TFP (d) GTFP for both devices. *(Sharma and Chaujar, 2021)*.

defined as the frequency at which max unilateral gain reduces to unity. Equation 5.9 shows that the f_{max} depends upon parasitic capacitance, drain-to-source conductance (g_{ds}), and f_T. The 2 times higher f_{max} is obtained for DC-BB-HEMT (92 GHz) in comparison to DC-HEMT (36 GHz) due to the lower parasitic capacitance (C_{gd}), g_{ds}, and higher f_T. Variation of transconductance frequency product (TFP) with gate bias is shown in **Figure 5.9(c)**. TFP is utilized in moderate to high-speed design. In **Figure 5.9(c)**, higher primary and secondary peaks are observed for the DC-BB-HEMT than the DC-HEMT due to the higher g_m, f_T, and lower I_d. Gain transconductance frequency product (GTFP) is another essential FOM that gives critical information regarding circuit designing by determining the perfect region to achieve the tradeoff among the gain, transconductance, and device speed. In **Figure 5.9(d)**, the higher value of GTFP is observed for DC-BB-HEMT (1310 GHz/V), which is about 57% higher than the DC-HEMT (828 GHz/V). The improvement of these parameters for DC-BB-HEMT is mainly due to the improvement of g_m and reduction of output conductance.

5.3.4 Linearity Analysis of DC-BB-HEMT with Variable T_{bb}

This subsection investigates the impact of the back-barrier distance from the lower channel (T_{bb}) on the linearity performance of DC-BB-HEMT. **Figure 5.10(a, b)** exhibit the drain current and transconductance characteristics for different T_{bb} values. It has been observed that while increasing the back barrier distance from the lower channel, the drain current and transconductance characteristics improved. As the back barrier distance increases from 10 nm to 30 nm, the drain current density also increases. A higher value of drain current is observed at 2.3 A/mm for 30 nm T_{bb}. On increasing the back barrier distance, the second quantum depth increases, which results in the enhancement of 2DEG concentration. Improvement in transconductance characteristics on increasing the back barrier distance is basically due to the lower scattering and higher mobility of 2DEG. When the InGaN back barrier is placed near the lower channel, the mobility of 2DEG is badly affected by the back barrier due to the alloy disorder scattering mechanism.

The investigation of non-linear parameters is very important as they are the primary source of distortion. So to achieve high linearity, the non-linear parameters should be low. The second and third-order transconductance parameters (g_{m2}, g_{m3}) are the non-linear parameters. **Figure**

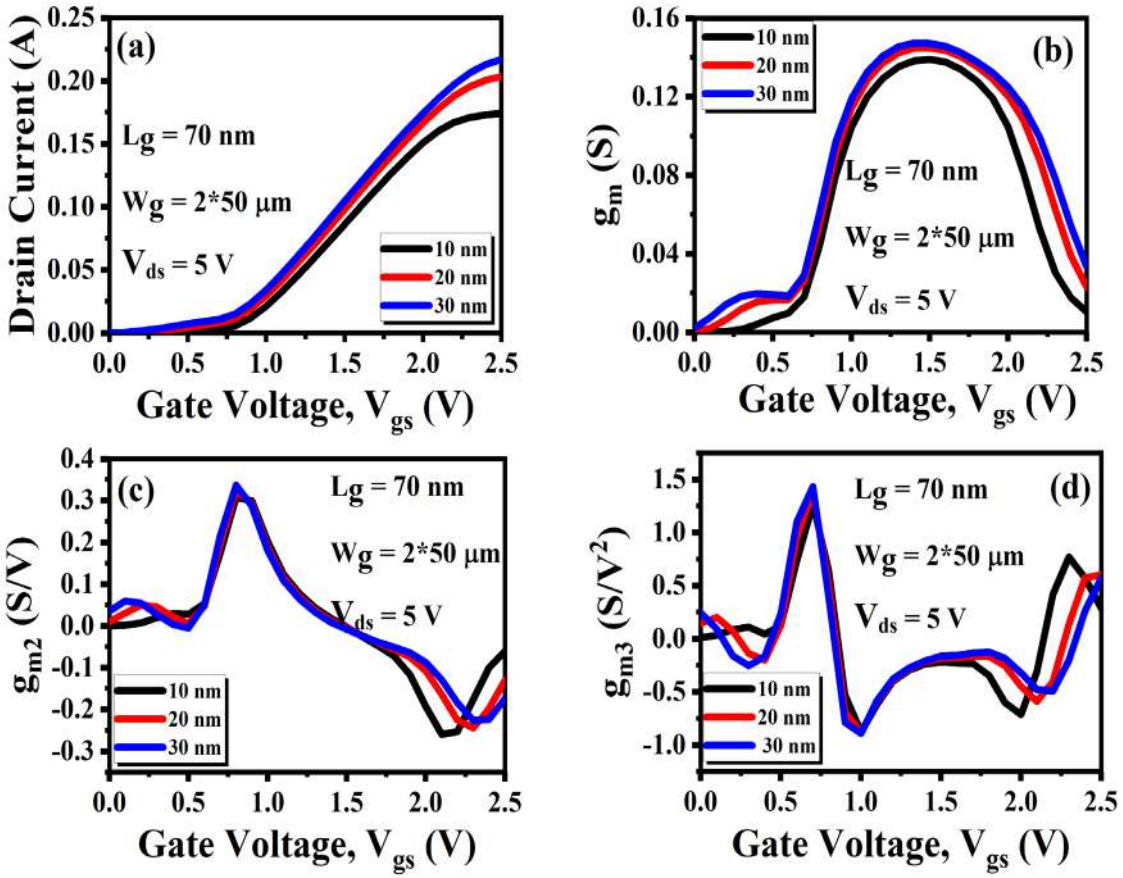

Fig. 5.10. (a) Transfer characteristics (b) transconductance (c) gm_2 (d) gm_3 for variable T_{bb}. *(Sharma and Chaujar, 2021)*.

5.10(c, d) shows the variation of non-linear parameters with gate bias for different back barrier distance. It has been observed that by increasing the T_{bb} from 10 nm to 30 nm, the non-linear parameters are almost comparable, which shows increasing the back barrier distance does not affect the non-linear parameters.

The linearity parameters are mathematically expressed as *(Kumar and Chaujar, 2021b).*

$$\text{VIP2} = 4 \times (g_m/g_{m2}) \tag{5.11}$$

$$\text{VIP3} = \sqrt{24 \times (g_m/g_{m3})} \tag{5.12}$$

$$\text{IIP3} = (2/3) \times \left(g_m/(g_{m3}R_s)\right) \tag{5.13}$$

$$1-\text{dB compression point} = 0.22 \times \sqrt{(g_m/g_{m3})} \tag{5.14}$$

VIP2 & VIP3 express the extrapolated gate voltage amplitude at which second and third-order harmonics equal the fundamental tone in device current (I_{ds}). These FOMs can accurately

investigate the distortion characteristics from DC parameters. In order to attain high linearity and low distortion, these parameters should be as high as possible. **Figure 5.11(a, b)** exhibit the graph of VIP2 and VIP3 with gate bias for different back barrier distances. It has been observed that by increasing the T_{bb} from 10 nm to 30 nm, VIP2 and VIP3 increase. The higher peak of VIP2 and VIP3 is observed at 65.3 V and 5.1 V for 30 nm T_{bb} which is 2 times higher than the 10 nm T_{bb} (29 V and 2.9 V). As shown in Equation 5.11 and 5.12, VIP2 and VIP3 parameters depend upon the transconductance and the second and third order transconductance. Due to the lower scattering disorder and higher mobility of 2DEG, higher g_m has been obtained for 30 nm T_{bb}.

Third-order input intercept point (IIP3) and 1-dB compression point are other essential FOMs investigating linearity performance. IIP3 exhibits the extrapolated input power at which the first and third harmonics are equal. **Figure 5.11(c)** shows the variation of IIP3 with gate bias for variable T_{bb}. The IIP3 parameter also increases on increasing the back barrier distance from the lower channel. The higher peak of IIP3 observed at V_{gs} = 1.8 V is 51 dBm for 30 nm T_{bb} which

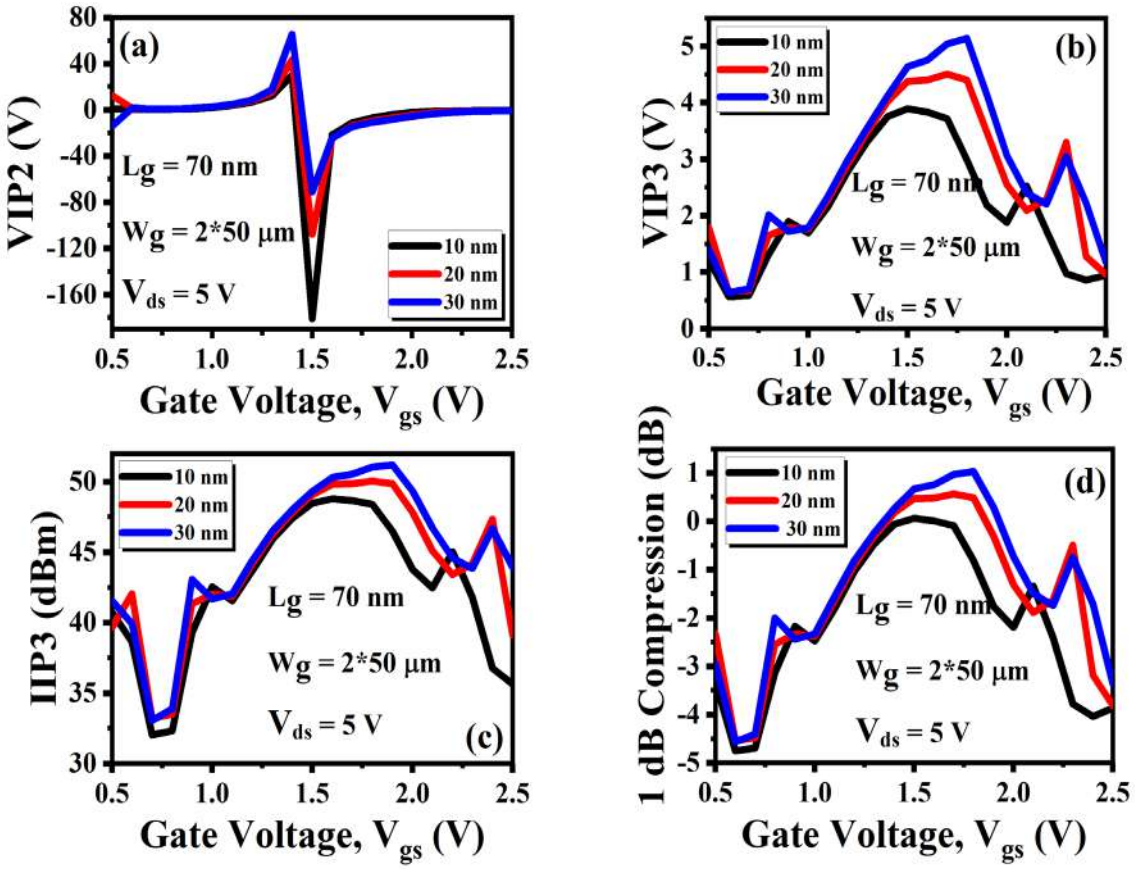

Fig. 5.11. Variation of linearity parameters with gate bias for different back barrier distance (a) VIP2 (b) VIP3 (c) IIP3 (d) 1-dB compression point. *(Sharma and Chaujar, 2021)*.

is about 10% higher than the 10 nm T_{bb} (46 dBm). 1-dB compression point is defined as the input power value at which the gain of the amplifier drops by 1-dB. The study of this parameter is essential for the amplifier circuit. **Figure 5.11(d)** exhibits the higher peak of 1 dB compression point for 30 nm (1.3 dB), which is 8 times higher than the 10 nm (-8.1 dB) and emphasizes the superior linearity performance of DC-BB- HEMT with 30 nm T_{bb}. Thus results reflect that RF harmonic distortion and linearity improve by increasing the InGaN back barrier distance from the lower channel.

5.4 Summary

This chapter explored the performance of double channel T-gate E-mode HEMT with back barrier (DC-BB-HEMT). The simulated results proved that the DC-BB-HEMT exhibited substantial improvements in analog performance. The intrinsic gain, which indicates a higher signal amplification capability, saw a whopping 50% increase. Similarly, the transconductance gain frequency (TGF) increased by an impressive 477%, while the early voltage was enhanced by 23%. These numbers suggest that the DC-BB-HEMT significantly improve the device's analog performance.

The DC-BB-HEMT further showcased superior RF performance when compared to conventional HEMT. Both its cut-off frequency and maximum oscillation frequency observed an increase of around 11.7% and 10%, respectively. Additionally, there was a significant improvement in gain frequency product (GFP), gate transconductance-frequency product (GTFP), and TFP by almost 35.2%, 57% and 44% correspondingly. Moreover, the study also investigated the device's linearity performance with varying back barrier distances. It has been observed that the linearity performance of proposed device improved at a back barrier distance of 30 nm. This result implies that careful optimization of the back- barrier distance can further enhance the device's linearity performance.

5.5 References

ADAK, S., SARKAR, A., SWAIN, S., PARDESHI, H., PATI, S. K., and SARKAR, C. K. 2014. High performance AlInN/AlN/GaN p-GaN back barrier gate-recessed enhancement-mode HEMT. *Superlattices and Microstructures*, *75*, 347-357.

CHAUJAR, R., KAUR, R., SAXENA, M., GUPTA, M., and GUPTA, R. S. 2008. Laterally

amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI. *Microelectronic engineering*, *85*, 566-576.

CHU, R., ZHOU, Y., LIU, J., WANG, D., CHEN, K. J., and LAU, K. M. 2005. AlGaN-GaN double-channel HEMTs. *IEEE Transactions on electron devices*, *52*, 438-446.

CHUGH, N., BHATTACHARYA, M., KUMAR, M., DESWAL, S. S., and GUPTA, R. S. 2018. Polarization dependent charge control model for microwave performance assessment of AlGaN/GaN/AlGaN double heterostructure HEMTs. *Journal of Computational Electronics*, *17*, 1229-1240.

FENG, Z. H., ZHOU, Y. G., CAI, S. J., and LAU, K. M. 2004. Enhanced thermal stability of the two-dimensional electron gas in Ga N⁄Al Ga N⁄Ga N heterostructures by Si_3N_4 surface-passivation-induced strain solidification. *Applied physics letters*, *85*, 5248-5250.

FRAYSSINET, E., KNAP, W., LORENZINI, P., GRANDJEAN, N., MASSIES, J., SKIERBISZEWSKI, C., and MAUDE, D. 2000. High electron mobility in AlGaN/GaN heterostructures grown on bulk GaN substrates. *Applied Physics Letters*, *77*, 2551-2553.

HAN, T., ZHAO, H., PENG, X., and LI, Y. 2018. Control of short-channel effects in InAlN/GaN high-electron mobility transistors using graded AlGaN buffer. *Superlattices and Microstructures*, *116*, 207-214.

JHA, S. K., SURYA, C., CHEN, K. J., LAU, K. M., and JELENCOVIC, E. 2008. Low-frequency noise properties of double channel AlGaN/GaN HEMTs. *Solid-state electronics*, *52*, 606-611.

KUMAR, B. and CHAUJAR, R. 2021a. Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET. *Silicon*,13,919-927.

KUMAR, B., and CHAUJAR, R. 2021b. TCAD temperature analysis of gate stack gate all around (GS-GAA) FinFET for improved RF and wireless performance. *Silicon*, *13*, 3741-3753.

LEE, D. S., GAO, X., GUO, S., and PALACIOS, T. 2011a. InAlN/GaN HEMTs with AlGaN back barriers. *IEEE Electron Device Letters*, *32*, 617-619.

LEE, D. S., GAO, X., GUO, S., KOPP, D., FAY, P., and PALACIOS, T. 2011b. 300-ghz inaln/gan hemts with ingan back barrier. *IEEE Electron Device Letters*, *32*, 1525-1527.

LIN, Z., KIM, H., LEE, J., and LU, W. 2004. Thermal stability of Schottky contacts on strained

AlGaN/GaN heterostructures. *Applied physics letters*, *84*, 1585-1587.

MANUAL, A.U.S. 2016. *Silvaco . Santa Clara, CA*.

MISHRA, U. K., PARIKH, P.and WU, Y. F.2002. AlGaN/GaN HEMTs - An overview of device operation and applications. *Proc. IEEE,* 90, 1022–1031.

PALACIOS, T., CHAKRABORTY, A., HEIKMAN, S., KELLER, S., DENBAARS, S. P., and MISHRA, U. K. 2005. AlGaN/GaN high electron mobility transistors with InGaN back-barriers. *IEEE Electron device letters*, *27*, 13-15.

PARDESHI, H. 2015. Analog/RF performance of AlInN/GaN underlap DG MOS-HEMT. *Superlattices and Microstructures*, *88*, 508-517.

RAVIKIRAN, L., DHARMARASU, N., RADHAKRISHNAN, K., AGRAWAL, M., YIDING, L., ARULKUMARAN, S., ... and NG, G. I. 2015. Growth and characterization of AlGaN/GaN/AlGaN double-heterojunction high-electron-mobility transistors on 100-mm Si (111) using ammonia-molecular beam epitaxy. *Journal of Applied Physics*, *117*, 025301.

SHARMA, M., and CHAUJAR, R. 2021. Design and investigation of recessed-T-gate double channel HEMT with InGaN back barrier for enhanced performance. *Arabian Journal for Science and Engineering*, 1-8.

ZHANG, W., XUE, J., ZHANG, L., ZHANG, T., LIN, Z., ZHANG, J., and HAO, Y. 2017. Trap state analysis in AlGaN/GaN/AlGaN double heterostructure high electron mobility transistors at high temperatures. *Applied Physics Letters*, *110*, 252102.

CHAPTER 6

SUMMARY AND FUTURE SCOPE

This chapter provides a summary of the research conducted in this thesis. In addition, the conclusions generated from the results are highlighted briefly. After that, this chapter discusses the potential future work that may be done to expand the research.

6.1 Summary

Silicon technology, which has been the main workhorse of modern electronics, has dominated the semiconductor sector for over a decade. Transistors made from silicon have been implemented in many different fields. However, silicon-based devices are quickly reaching their theoretical limit of operation, and future RF and microwave applications will require even higher levels of performance that cannot be achieved with the current technology. The GaN HEMT technology has solidified its position as the dominant contender in the realm of high-power and RF applications. GaN contains a number of beneficial properties, which together lead to the material's outstanding performance. In this thesis, a T-gate E-mode HEMT architecture is mainly encompassed as it provides the aggressively scaling of device and high RF performance. Moreover, to overcome various challenges faced by conventional HEMT, different engineering schemes have also been integrated on T-gate HEMT. A polarization induced doping in the buffer layer (buffer Engineered), heavily doped source/drain region, and recessed T-gate (Gate Metal Engineered) structure has been developed in **Chapter 2.** The 2-D TCAD simulations have been executed to explore T-gate E-mode HEMT with a polarization-doped buffer, and a detailed DC and RF performance analysis has been developed. The results demonstrate that the utilization of recessed gate engineering and polarization-induced doped buffer engineering yields substantial improvements across various performance metrics. Notably, these techniques achieve a remarkable I_{on}/I_{off} ratio of 10^9, a significant reduction in subthreshold swing to 78 mV/dec, and a DIBL of just 100 mV/V. Furthermore, they increase the breakdown voltage to 33 V, improve the cutoff frequency to 583 GHz, and maximize the oscillation frequency to 840 GHz. Moreover, the use of lattice-matched InAlN barrier layer and AlN spacer layer enhances the electron mobility (1250 cm^2/Vs) and 2DEG density (2.8×10^{13} cm^{-2}) due to which higher drain current density has been achieved (2.8 A/mm). Additionally, the impact of gate recessed depth (R_d) on DC and RF performance is also investigated. It has been observed that on increasing the gate recessed depth from 2 nm to 5 nm, a positive shift in threshold voltage (0.8V), lower off current (10^{-8}), and higher transconductance (1.55 S/mm) is achieved. Moreover, a high-k gate oxide engineering approach has been done, wherein a particular segment of the recessed gate is substituted with a high-k dielectric material. This strategic implementation of the high-k dielectric significantly enhances the interfacial and

transport characteristics of the device while effectively reducing the gate leakage current. However, it has been observed that implanting the gate oxide alone does not enable E-mode operation. Therefore, gate-recessed engineered T-gate E-mode HEMT with polarization doped buffer is the superior choice for achieving E-mode operation and a potential candidate for high-power millimeter-wave applications as discussed in **Chapter 2**.

However, the downscaling of the device has a notable impact on its DC and RF performance characteristics. Consequently, it becomes crucial to carefully determine the dimensions of the T-shaped gate structure to ensure optimal device operation. In regard of this, the **Chapter 3** will conduct an in-depth investigation of the influence exerted by the T-gate shape on both the DC and RF performance of the device. The impact of T-shaped gate geometry on parasitic capacitance and RF Figure of Merits (FOMs) such as maximum oscillation frequency (f_{max}), gain-bandwidth product (GBP), cut-off frequency (f_T), maximum stable and available power gain (Gms and Gma), maximum transducer power gain (MSG) and stability factor (k) are discussed in **Chapter 3**. The simulation results show that the parasitic capacitances are deeply affected by the geometry of the T-gate. The less influence of gate-to-source capacitance (C_{gs}) by the drain voltage possesses constant depletion charges at the source side, leading to a persistent value of C_{gs} with drain bias. Furthermore, the effect of gate head length (H_{length}), gate stem height (S_{height}), and gate foot length (F_{length}) on RF Figure of Merits (FOMs) are deeply investigated. The simulated results confirm that the proper choice of H_{length} (280 nm), S_{height} (100 nm), and F_{length} (10 nm) significantly reduced the parasitic capacitance (C_{gs} = 350 fF/mm and C_{gd} = 140 fF/mm) and enhanced the f_{max} (840 GHz), GBP (636 GHz), f_T (583 GHz) and also improve the power gains. The simulated results of the proposed device design show its applicability for high-performance RF/microwave applications.

Furthermore, parameters for noise and scattering play an important role in establishing a device's overall performance. Noise parameters are critical because they govern how much background noise will be added to the signal as it transmits through the device. On the other hand, the scattering parameters are determining the amount of power that is lost when the signal travels through the device. Therefore, in order to ensure the reliability of the device, it is necessary to investigate the effect that polarization-doped buffer engineering has on the noise and scattering characteristics of T-gate HEMTs. This is the key emphasis area of **Chapter 4**. The detailed discussion on S-parameters and noise performance has been developed. Results

showed that using a polarization-induced doped buffer (PDB) engineering significantly enhance the transconductance by 30% and reduced the gate, source resistance by 67.6%, 27.7% which lead to a reduction in the reflection coefficients (S11, S22). Enhancement in transconductance further improved the forward transmission coefficient (S21) by 69% as compared to GaN-HEMT. Even at high frequencies, the PDB-HEMT device has a minimum noise figure of NF_{min}= 1.62 dB, lower noise conductance, and stronger auto/cross-correlation. These findings make it abundantly evident that the T-gate PDB HEMT structure is an excellent candidate for high-performance RF applications and low noise amplifiers.

The implementation of the back barrier on T-gate HEMT significantly enhances the RF and noise performance of device as discussed in **Chapter 2** and **Chapter 4**. However, it also reduces the drain current density. Therefore, a double channel engineering is executed in the **Chapter 5** by inserting the AlN layer below the InAlN/GaN interface developing a double channel HEMT. Simulation results showed that formation of double channel significantly enhance the drain current density of 2.5 A/mm. However, due to a lack of gate controllability over a lower channel, the high leakage current is observed in double channel HEMT. This issue has been addressed by using the InGaN as a back barrier, which improves the carrier confinement of 2DEG by raising the conduction band for the GaN buffer and considerably improves the gate controllability over a lower channel. The performance of the proposed device is compared with that of conventional double-channel HEMTs. The simulation results showed, the proposed double channel back barrier HEMT (DC-BB-HEMT) exhibited substantial improvements in analog performance. The intrinsic gain, which indicates a higher signal amplification capability, improved by 50%. Similarly, the transconductance gain frequency (TGF) increased by an impressive 477%, while the early voltage was enhanced by 23%. These numbers suggest that the InGaN back barrier significantly contributes to the device's analog performance. Moreover, RF performance of (DC-BB-HEMT) also compared with conventional DC-HEMTs. Simulation results showed that both the cut-off frequency and maximum oscillation frequency increased by around 11.7% and 10%, respectively. Additionally, there was a significant improvement in gain frequency product, gate transconductance-frequency product (GFP), TFP and GTFP by almost 36%, 44% and 57% correspondingly. These findings highlight the significant role played by InGaN back barriers in enabling enhanced RF performances in devices. Moreover, the study also investigated the device's linearity performance with varying back barrier distances. It has been observed that the linearity

performance of proposed device improved at a back barrier distance of 30 nm. This result implies that careful optimization of the back- barrier distance can further enhance the device's linearity performance.

6.2 Future Scope

The prime objective of this thesis is to design a E-mode GaN HEMT device which can overcome the limitations of conventional GaN HEMT. Various engineering schemes, including polarization-doped buffer engineering and T-shaped gate metal engineering has been incorporating to mitigate 2DEG spilling issues in the buffer and reduce leakage current, leading to improved device performance. Further, the proposed device design is also investigated for small signal and noise behaviour. By studying the small signal and noise behaviour, valuable insights can be gained regarding the device's overall performance, signal amplification capabilities, and noise figure. Another objective of this research work is to implement the double channel engineering on the proposed device structure in order to make a balance between RF performance and drain current density in device. All of the objectives, nevertheless, are accomplished to a significant degree via the use of extensive numerical simulations. In spite of this, taking into account the work that has been done so far, it would be interesting to investigate and develop the following features as future aspects.

1. Temperature analysis can be performed to study the application of the T-gate E-mode polarization induced doped buffer for a wide range of temperature.

2. In sensing applications, the T-gate E-mode double channel HEMT with InGaN back barrier may be applied as a biochemical sensor. This sensor can detect biomolecules such as glucose, DNA, proteins, cancer, and dangerous gases.

3. The jagged field plate engineering can be implemented in order to enhance the breakdown voltage of the device.

4. The output power of FETs is highly constrained by the phenomena of current collapse, which is related to traps. It reduces the microwave frequency output power of a device compared to what would be predicted from its DC characteristics. This is due to the

device structure contains defects and traps at the surface or epitaxial layer. Therefore, it is essential to understand the defects and traps in this structure in order to enhance the performance of the device.

Received: 26 June 2021 | Revised: 9 November 2021 | Accepted: 22 December 2021

DOI: 10.1002/mmce.23057

ORIGINAL ARTICLE

INTERNATIONAL JOURNAL OF RF AND MICROWAVE COMPUTER-AIDED ENGINEERING WILEY

Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications

Megha Sharma | **Rishu Chaujar**

Department of Applied Physics, Delhi Technological University, Delhi, India

Correspondence
Rishu Chaujar, Department of Applied Physics, Delhi Technological University, Delhi, India.
Email: chaujar.rishu@dtu.ac.in

Abstract

The DC and RF performance of ultra-scaled 10 nm E mode InAlN/AlN HEMT with polarized doped buffer has been investigated. The proposed device has the feature of polarized doped buffer, heavily doped source/drain region, and recessed T-gate structure. The polarization-induced doping in the buffer layer bent the conduction band upwardly convex, which enhanced the 2DEG confinement, reduced the buffer leakage current, and significantly uplifted the breakdown voltage (33 V), which is 5 times higher than the conventional InAlN/AlN GaN buffer HEMT (8 V). The short channel effect was further reduced by the recessed gate engineering (high on/off ratio 10^9, subthreshold swing 78 mV/dec, and DIBL 100 mV/V), and smaller 10 nm foot length of T-gate reduced the parasitic capacitance, which uplifts the RF parameters of the proposed device. The proposed device exhibits a high current density of 2.8 A/mm, transconductance 1.55 S/mm, cutoff frequency f_T (583 GHz), and maximum oscillation frequency f_{max} (840 GHz). At room temperature, the calculated carrier density and mobility are 2.8×10^{13} cm^{-2} and 1250 cm^2/Vs. The large Jhonson figure of merit (f_T. V_{BR}) 19.23 THz and (f_T. f_{max})$^{1/2}$ 699 GHz shows the potential of the proposed device for high-power millimeter-wave applications.

KEYWORDS

breakdown voltage, conduction band, cutoff frequency, heterostructure, Polarization

1 | INTRODUCTION

The GaN-based devices have preeminent physical properties such as higher breakdown voltage, larger bandgap, high mobility, and good thermal conductivity. These superior properties attracted the extensive attention of researchers to develop the high-power amplifier for image sensing, remote sensing, radar, and space research.[1–3] Several research papers have been published on AlGaN/GaN HEMTs[1–8] for high RF applications. To achieve the operating frequency in the millimeter range, a reduction of the device geometry is required. The reduction of AlGaN barrier thickness produces an unavoidable strain at the AlGaN/GaN junction. The decrement of gate length induces the short channel effect due to the lower aspect ratio. The lattice-matched InAlN layer successfully reduced the strain at InAlN/GaN junction.[9] The spontaneous polarization induces the higher 2DEG density at InAlN/AlN interface, enhancing the drain current density 3.3 A/mm, which is 205% higher than the AlGaN HEMT.[10] The InAlN/AlN-based HEMTs allow the device's aggressive scaling, empowering

the cutoff frequency and reducing the short-channel effect (SCE). Nowadays, InAlN/GaN attracted much attention in high-power RF applications due to its high power and current gain frequency, minimum SCE, lower leakage current, and high drain current density.[11–16] The device performance has also been improved by introducing the AlN layer between the InAlN/GaN layer, which increases the conduction band's discontinuity and enhances the 2DEG concentration.[17] It also reduces the alloy scattering, which significantly improves the device's mobility. The InAlN/AlN T-Gate HEMTs stated many advantages but also suffered from the one major issue of spilling 2DEG from the channel into a buffer which reduces the mobility and reliability of the device.[18] Thus, innovative buffer engineering is required to robust the performance of InAlN HEMTs. Initially, the resistivity of the buffer is increased by the doping of Fe or C acceptors, which compensate for the bulk-free electrons.[19] However, these dopants generate deep-level acceptors in the layer, leading to a strong current collapse.[20] Recently polarization doping has been considered a better alternative, which can be obtained by grading the AlGaN layer. Many experimental and theoretical papers have already been published for the different types of graded engineering. Shibin Li et al. published the experimental work on the polarization-induced pn junction.[21] Debdeep Jena et al. show the experimental work on polarization bulk doping.[22] Shibin Li et al.[23] exhibits the polarization-induced hole doping in which Al comp changes from 0.7 to 1. Simon et al. used the polarization doping for UV LEDs,[24] Tiecheng Han et al. reported the polarization doping to reduce SCEs.[25] Chuanhao Li et al. show the breakdown and current collapse characteristics of graded AlGaN buffer.[26]

This paper has designed and investigated the DC and microwave performance of ultra-scaled 10 nm T-gate InAlN/AlN E-mode HEMT with heavily doped source/drain region and polarization doped buffer. The higher f_T/f_{max}, high breakdown voltage, and tighter 2DEG confinement have been achieved for the proposed HEMT. The T-gate shape provided a large gate area by keeping the lower foot length, significantly reducing gate capacitance and gate access resistance.[27] The higher aspect ratio is also maintained (L_g/d) by recessing the gate length, which effectively reduces the short channel effect.[28] The heavily doped source/drain region significantly reduced the contact resistance.[29] The polarization-induced doping in the buffer allows the potential to bend upwardly convex, enhancing the resistivity in the buffer layer without any intentional doping, which significantly reduced the buffer leakage current, improving the pinch-off voltage and microwave performance of the proposed device.

2 | DEVICE STRUCTURE

The schematic structure of the proposed HEMT is shown in Figure 1A. The proposed device is made up of 6 nm lattice-matched InAlN barrier layer, 1 nm AlN spacer layer, which increases the conduction band discontinuity at AlN/GaN junction and enhances the 2DEG concentration, 20 nm GaN channel layer, and 1 μm AlGaN buffer layer in which aluminum composition linearly changes from 0.2 to 0 along the (0001) direction. The T-shaped Schottky gate consists of a Pt/Au metal stack with a smaller footprint and a larger gate area (10 nm length, 100 nm stem height, 400 nm head, 2×25 μm gate width). The T-shaped structure decreases the gate resistance and gate capacitance by providing a larger gate area and lower foot length. The source and drain region doped with Si of order 10^{19} cm^{-3} to reduce the contact resistance. The 20 nm SiN layer is used to passivate the device, which reduces the parasitic capacitance and enhances the device's frequency parameters.

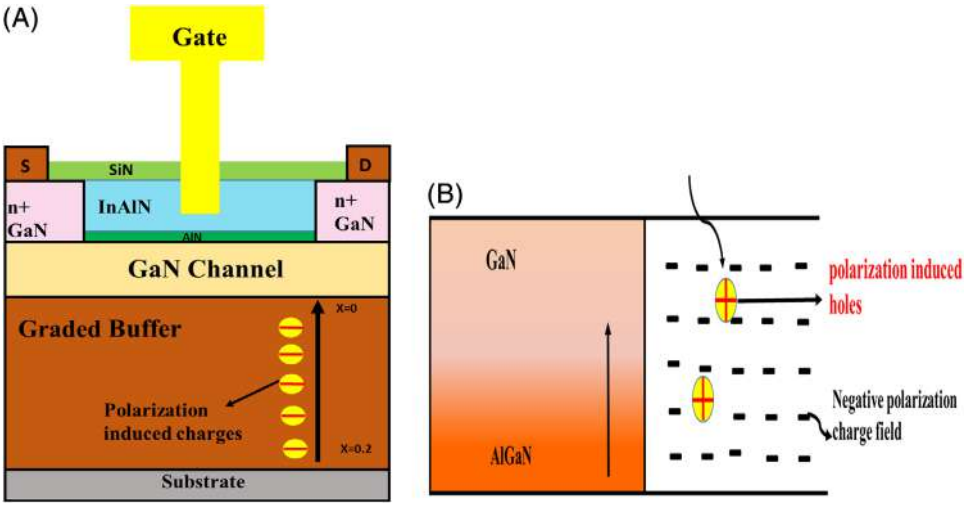

FIGURE 1 (A) InAlN/AlN T-gate with polarized buffer (B) polarization induced doping

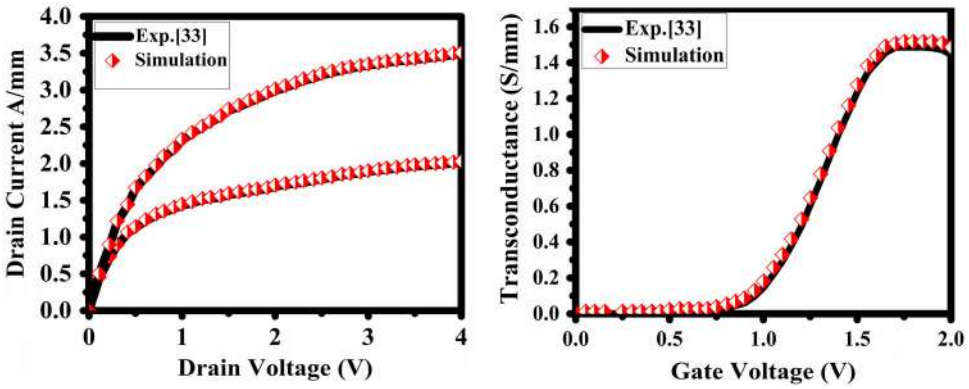

FIGURE 2 Calibration of transfer characteristics of 20 nm T-gate HEMT[33]

The physics of polarization-induced doping in the buffer is depicted in Figure 1B. The polarization charge discontinuity across the heterojunction formed the fixed polarization charges. When the Al composition changes from the AlGaN to GaN, a negative polarization charge field is induced over a bulk, the induced charge density is calculated by the divergence of the polarization field, which changes along the growth direction. Due to the charge neutrality, equivalent holes are induced by the negative polarization charge field. Hence bulk-free electrons are more deeply compensated by the high-density polarization induced holes and significantly reduce the buffer leakage current.

3 | EXPERIMENTAL CALIBRATION AND MODELS

The simulation of the proposed device is carried out by the Atlas-Silvaco simulator.[30] Various physical models such as Fermi-Dirac, high field mobility, Shockley-Read-Hall, low field mobility, and polarization models are used during the simulation. The two mobility models are defined in Equation (1) and Equation (2), respectively.

1. High field mobility model[30]

$$\mu(E)=\frac{\mu(N,T)+V_{sat}\frac{E(N_1-1)}{E_C{}^{N_1}}}{1+a_n\left(\frac{E}{E_C}\right)^{N_2}+\left(\frac{E}{E_C}\right)^{N_1}} \quad (1)$$

where v_{sat} and E are the saturated velocity, and electric fields of electrons and E_C, a_n, N_1, N_2 are coefficients.

2. Low field mobility model[30]

$$\frac{1}{\mu(T,N)}=a\left(\frac{N}{N^{ref}}\right)\left(\frac{T}{300}\right)^{-15}\times\ln\left[1+3\left(\frac{T}{300}\right)^{2}\left(\frac{N}{N^{ref}}\right)^{-2/3}\right]+b\left(\frac{T}{300}\right)^{1.5}+\frac{c}{(e^{1065/T})-1} \quad (2)$$

The mobility function of the ambient temperature and doping is represented by μ (T, N).

3. Polarization model[31]

In GaN-based devices, the two types of polarization have been induced, that is, piezoelectric and spontaneous polarization. The total polarization model is defined in Equation (3).

$$P_{total}=[(P_{PE}+P_{SP.})(bottom)]-[(P_{PE}+P_{SP.})(top)] \quad (3)$$

For the $In_{0.17}Al_{0.83}N$/GaN, only spontaneous polarization has been considered as the lattice of InAlN/GaN is matched. The complete lattice relaxation of the lattice has been assumed for the graded buffer. Hence total polarization is spontaneous polarization without any piezoelectric effect. The polarization gradient in the buffer layer induces the space polarization charges, and the density of these polarization charges is expressed by Equation (4). Equation (5) exhibits the expression for the spontaneous polarization, where x is the composition of Al.

$$\rho P=-\nabla.P=-\frac{\partial P}{\partial Z} \quad (4)$$

$$P_{SP}(Al_xGa_{1-x}N)=x\,P_{SP.}(AlN)+(1-x)\,P_{SP.}(GaN) \quad (5)$$

4. Fowler-Nordheim (FN) tunneling model[32]

FN-Tunneling is the tunneling of the electrons from the metal/semiconductors to the conduction band of the insulator. In the simulation, the off-state current is simulated using the FN tunneling model. The expression of FN-Tunneling is defined in Equation (6).

$$J=\frac{q^3E^2}{8\pi h\emptyset}\exp\left[-\frac{4(2m)^{1/2}\emptyset^{3/2}}{3hqE}\right] \quad (6)$$

where $E, q, m, and \emptyset$ are the electric field, electronic charge, mass of a free electron, and barrier height.

In Figure 2, the physical models have been calibrated with the experimental results of K. Shinohara

et al..[33] It has been observed that the experimental result exhibits an outstanding agreement with the simulated result.

4 | RESULTS AND DISCUSSION

4.1 | Band diagram

This section investigates the conduction band of the proposed device at $V_{gs} = 0$ V. The band diagram explains the electron confinement and 2DEG formation at AlN/GaN interface. The discontinuity in the bandgap of heterostructure gives rise to the band bending, which forms the quantum well at the AlN/GaN interface. The InAlN/GaN heterojunction has a large band discontinuity and strong polarization effect, allowing the large 2DEG formation in the device. The 2DEG concentration can be calculated using Equation (7).[34]

$$n_s = \frac{1}{(d_{InAlN} + d_{AlN})} \times \left\{ \frac{\sigma_{InAlN} \times d_{InAlN}}{e} + \frac{\sigma_{AlN} \times d_{AlN}}{e} - \frac{\varepsilon(x)\varepsilon_0}{e^2} \times \left\{ e\emptyset_b(x) + E_F[x, n_s(x)] - \Delta E_{c,AlN/GaN} + \Delta E_{c,InAlN/GaN}(x) \right\} \right\} \quad (7)$$

where $\sigma_{InAlN}, \sigma_{AlN}, d_{InAlN}, d_{AlN}, m_{InAlN}, m_{AlN}, m_{GaN}, \varepsilon_{InAlN}, \varepsilon_{AlN}, \chi_{InAlN}, \chi_{AlN}, \chi_{InN}$ are the induce polarization charge density, thickness, effective mass, dielectric constant, and electron affinity of the InAlN, AlN layer. $\emptyset_b(x), E_F$ is the schottky barrier height and fermi energy level. $\Delta E_{c,AlN/GaN}$ and $\Delta E_{c,InAlN/GaN}(x)$ is the conduction band offset. The values of various parameters are depicted in Table 1. Figure 3 exhibits the conduction band diagram of the proposed device. The graded buffer region has the polarization-induced negative space charge, making the buffer potential upwardly convex and enhancing the 2DEG confinement. The interface charge density of the proposed device is shown in Figure 4A. The total charge density in the channel region is $2.8 \times 10^{13}\,cm^{-2}$ obtained. It can be observed that 2DEG concentration depends upon the polarization-induced sheet charge density. The fabrication process flow of the proposed device is depicted in Figure 4B.

4.2 | DC Characteristics

This section investigates the DC performance of the proposed device. Figure 5A exhibits the drain current density of the proposed device at $V_{ds} = 3$ V is 2.8 A/mm and

TABLE 1 Values of parameters used in simulation

Parameters	Values
σ_{InAlN}	$-4.189 \times 10^{13}\,cm^{-2}$
σ_{GaN}	$-1.84 \times 10^{13}\,cm^{-2}$
$\emptyset_s$	2.8 eV
$\Delta E_{c,InAlN/GaN}$	0.8 eV
$\Delta E_{c,AlN/GaN}$	1.7 eV
m_{InAlN}	0.25 m_o
m_{AlN}	0.32 m_o
m_{GaN}	0.20 m_o
ε_{InAlN}	10.1
ε_{AlN}	9.5
χ_{InAlN}	2.5 eV
χ_{AlN}	2.1 eV
χ_{InN}	4.7 eV

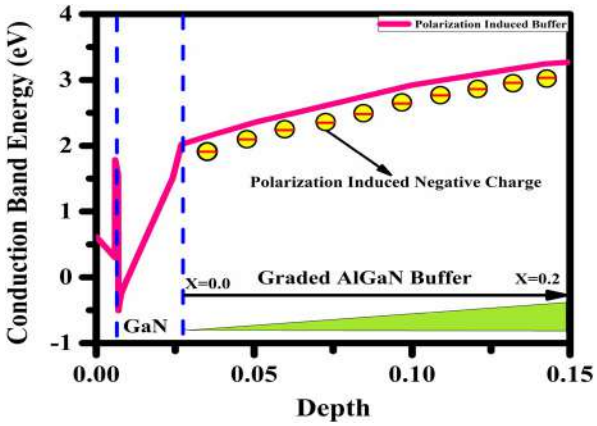

FIGURE 3 Conduction band diagram of the proposed structure

1.3 A/mm at $V_{ds} = 1$ V. The high current density is achieved due to the higher mobility (1250 cm^2/Vs) with a larger carrier density ($2.8 \times 10^{13}\,cm^{-2}$) in the channel region. The ultra-scaled devices have the one major issue of short channel effect, particularly in 10 nm gate length. SCEs are significantly reduced in the proposed device by maintaining the high aspect ratio with gate recessed and reducing buffer leakage current by polarization doping. The subthreshold swing (SS) and drain induced barrier lowering (DIBL) from the log scale are 78 mV/dec and 100 mV/V depicted in Figure 5B. The drain current density of variable recessed depth (R_d) is depicted in Figure 5C. It has been observed that on increasing the recessed depth from 2 to 5 nm, the threshold voltage is shifted toward the positive side with a significant decline in drain current. Figure 5D shows the high on/off ratio 10^7 for the recessed depth 5 nm at $V_{ds} = 3$ V.

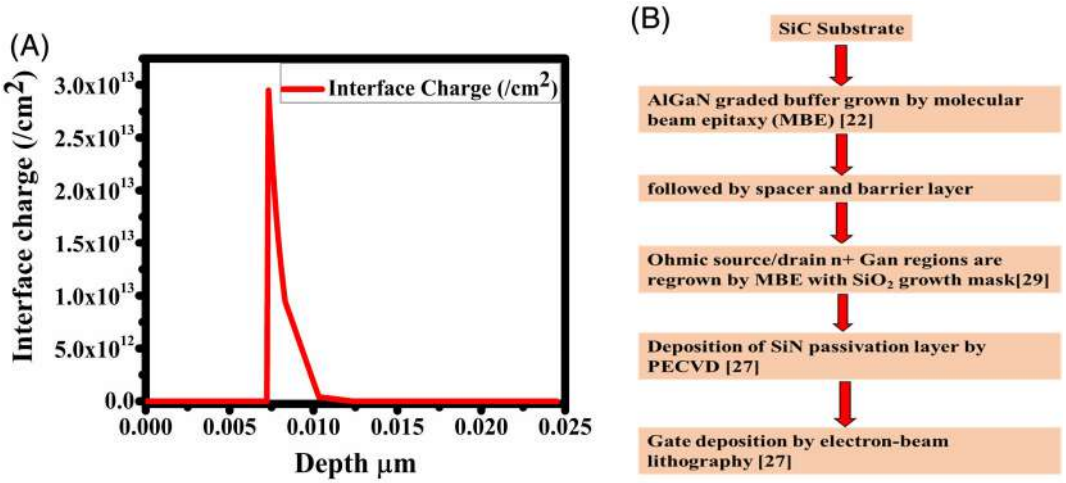

FIGURE 4 (A) Interface charge density of the proposed structure (B) fabrication process flow of proposed device

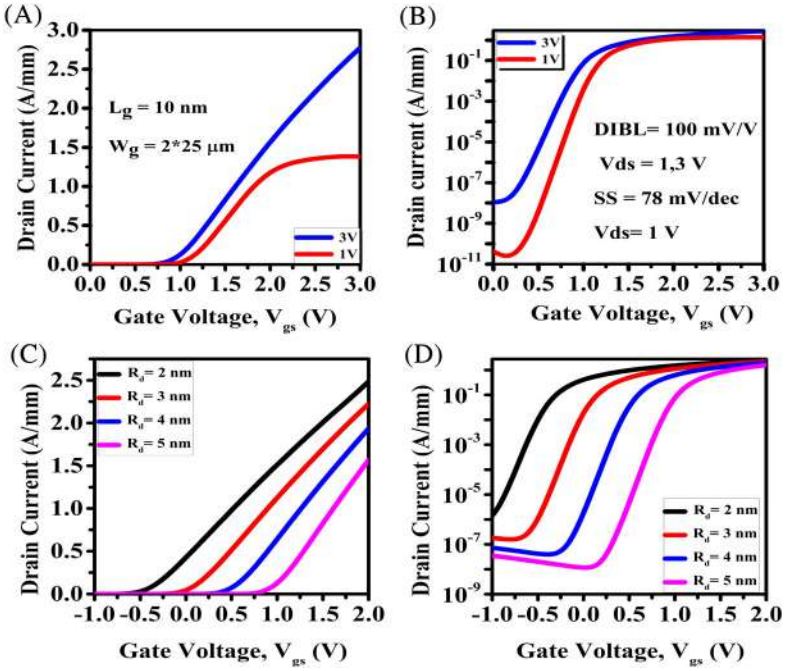

FIGURE 5 (A) Linear scale (B) log scale (C) variable recessed depth, linear scale (D) variable recessed depth, log scale drain current density of the proposed device

The transconductance characteristics of the proposed device are depicted in Figure 6A. A higher peak of the transconductance of 1.55 S/mm is obtained at $V_{gs} = 1.4$ and $V_{ds} = 3$ V. Transconductance of the device is defined as the change in drain current with change in gate voltage. Figure 5A shows the variation of drain current with gate bias for $V_{ds} = 1$ and 3 V. It has been observed that for $V_{ds} = 1$ V, the drain current starts saturating at $V_{gs} = 1$ V, leading to degradation of transconductance at earlier gate bias, whereas at $V_{ds} = 3$ V, drain current is still increased. The increment of drain voltage enhances the lateral electric field and electron velocity in the channel, further enhancing the drain current.

Figure 6B shows the transconductance characteristics of variable gate recessed depth. It has been observed that transconductance increases by increasing the recessed depth from 2 to 5 nm. This increment is because gate controllability over a channel increases by increasing the recessed depth, enhancing the transconductance, and reducing the short channel effect. Figure 6C exhibits the comparison of published data with our proposed work for various gate lengths.[35–39] The proposed device has a more balanced DC characteristic which is highly required for high power and high-frequency applications. The breakdown voltage of HEMT devices is the essential parameter for high RF applications. However, the gate

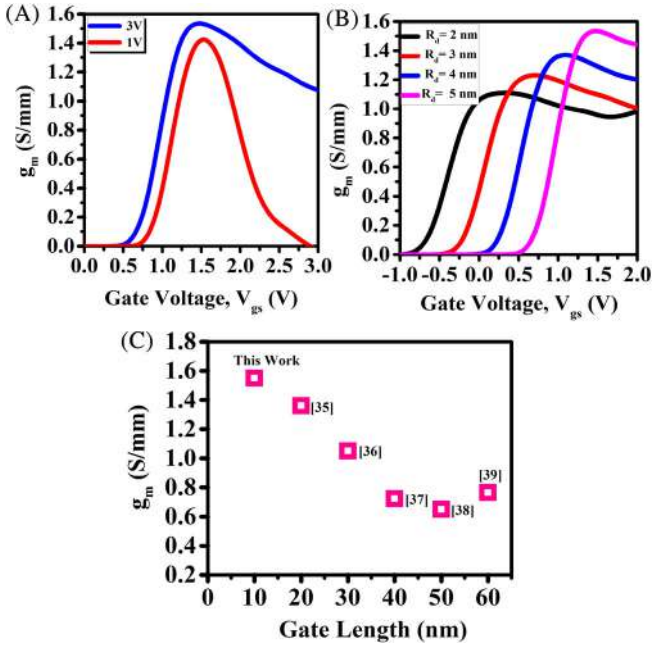

FIGURE 6 (A) Transconductance of the proposed device (B) transconductance value for variable gate recessed depth (C) comparison of transconductance value with published results

length below 50 nm significantly reduced the breakdown voltage because of the high leakage current. In Figure 7A graph of breakdown voltage with gate recessed depth is shown. A higher breakdown voltage has been observed for the 5 nm recessed depth. Figure 7B exhibits the breakdown characteristics of the proposed and conventional device. The higher breakdown voltage, that is, 33 V, was obtained for the proposed 10 nm T-gate InAlN/AlN HEMT with a polarized doped buffer, which is 5 times higher than the conventional InAlN/AlN GaN buffer HEMT. The enhancement of the breakdown voltage in a proposed device is because of the polarization-induced doping in the buffer layer, which reduces the buffer leakage current. The breakdown voltage obtained for the proposed device is the best among the literature for the 10 nm gate length HEMT.

4.3 | Microwave results

The microwave properties of the proposed device are investigated in this section through S-parameter simulation. These types of analysis are called small-signal analysis, as small input signals are required for the characterization. The parameters investigation includes cutoff frequency (f_T), max oscillation frequency (f_{max}), max. Stable gain (MSG), and Mason's unilateral gain (MUG). All these parameters are directly calculated from the S parameters by using the following Equations.[15]

$$H_{21} = \left| \frac{-2S_{21}}{(1-S_{11}) \times (2-S_{22}) - S_{12} \times S_{21}} \right| \tag{8}$$

$$MUG = \left(\frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right) \times \left(1-|S_{22}|^2\right)} \right) \tag{9}$$

$$MSG = \frac{|S_{21}|^2}{|S_{12}|^2} \times \left(K \pm \sqrt{(K^2-1)} \right) \tag{10}$$

$$K = \frac{1-|S_{21}|^2-|S_{12}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2 \times |S_{12}|^2 \times |S_{12}|^2} \tag{11}$$

f_T defines as the frequency at which forward current gain (h_{21}) becomes unity.[40] Mason's unilateral gain (MUG) is an important figure of merit used to investigate the max oscillation frequency. MUG defines as the power gain of two port networks where output to input feedback is zero.[41] Figure 8A exhibits the small-signal characteristics of the proposed device at $V_{gs} = 1.4$ V and $V_{ds} = 3$ V. The f_T and f_{max} are evaluated where current gain and unilateral gain become 0 dB. The f_T and f_{max} values 583 and 840 GHz are recorded for the proposed device. The rollett stability factor and MSG are plotted in Figure 8B. It has been observed that the device is unconditionally stable in the cutoff frequency region and behaves as a stable

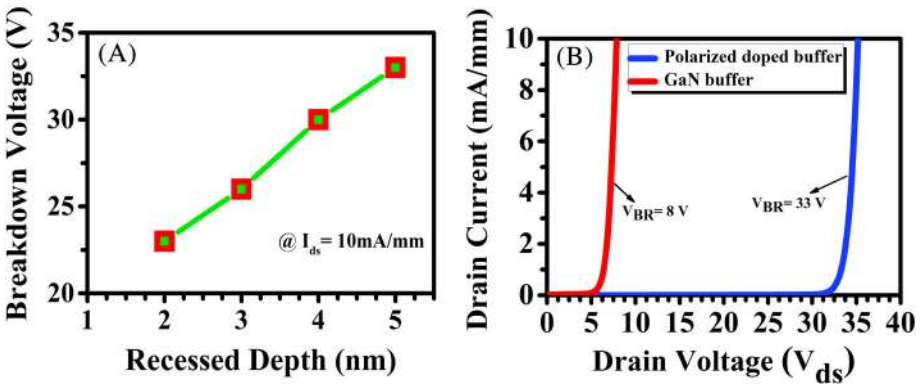

FIGURE 7 (A) Breakdown voltage with gate recessed depth for the proposed device (B) breakdown characteristics of the proposed and conventional device

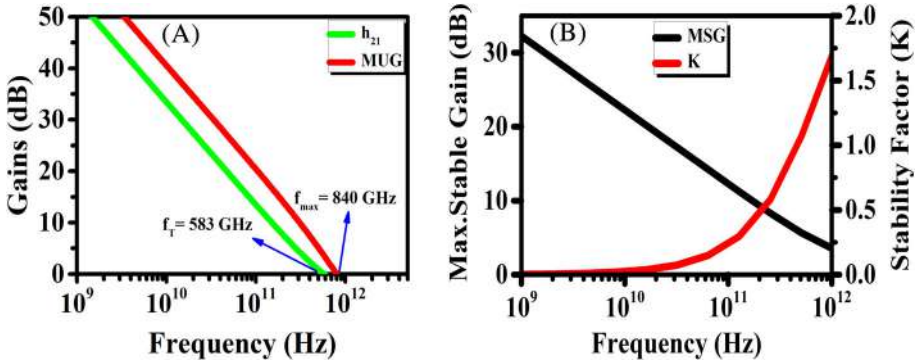

FIGURE 8 (A) Current gain and unilateral gain (B) stability factor and max. Stable gain of the proposed structure

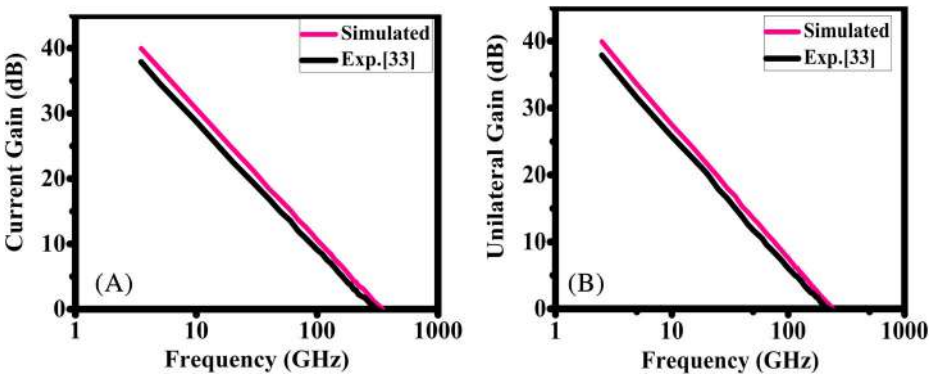

FIGURE 9 Exhibits the calibration of microwave performance parameter of 20 nm T-gate HEMT

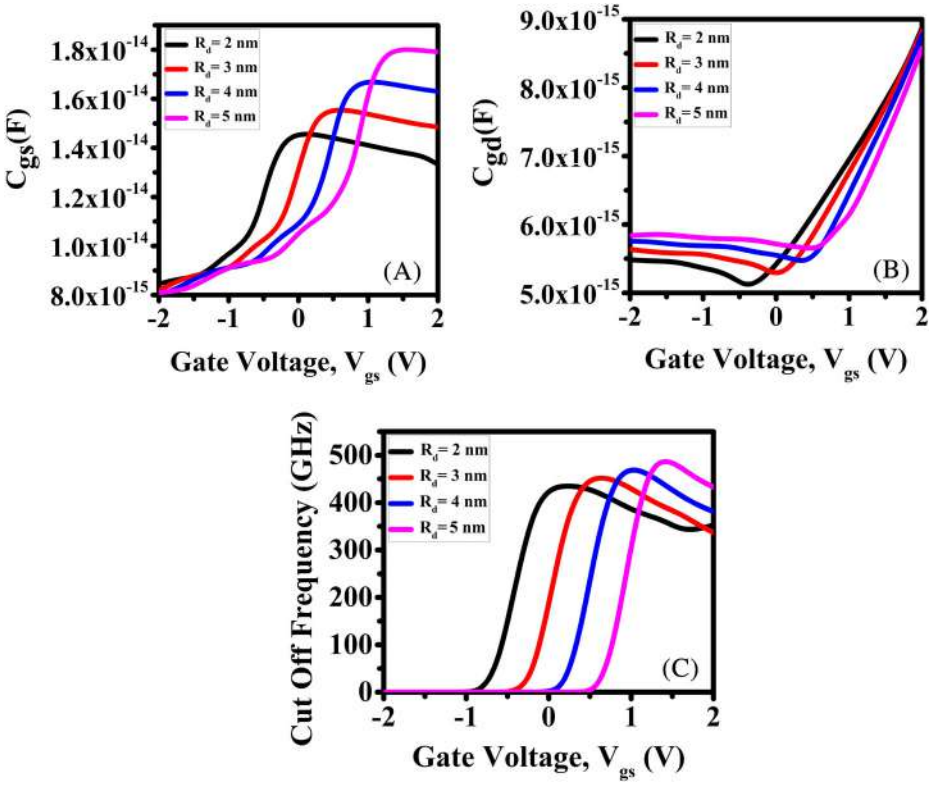

FIGURE 10 (A) C_{gs} (B) C_{gd} (C) Cutoff frequency of proposed device with gate bias

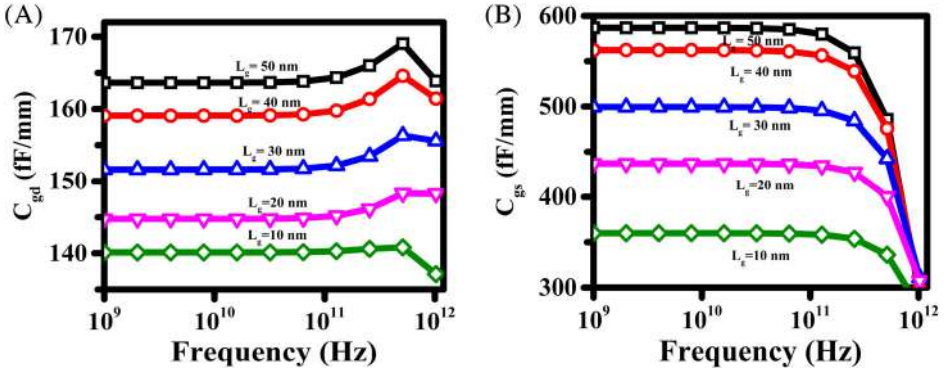

FIGURE 11 (A) C_{gd} (B) C_{gs} of proposed device for different gate length

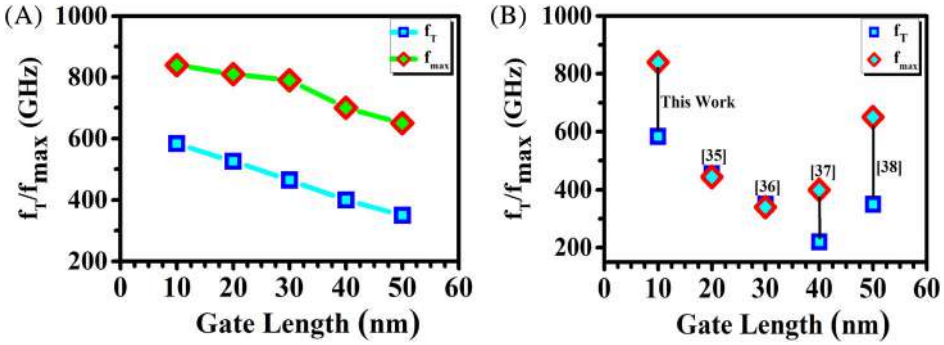

FIGURE 12 (A) Variation of f_T /f_{max} with gate length (B) comparison of f_T/f_{max} of a proposed device with published results

amplifier. Figure 9 shows the microwave performance of experimental paper with simulated data.

In Figure 10, the impact of gate recessed depth on parasitic capacitance and the cutoff frequency is investigated at an operating frequency of 1 MHz

$$f_T \approx g_m/2\pi\left(C_{gs}+C_{gd}\right) \tag{12}$$

Figure 10A,B exhibit the plot of the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) with gate bias. For better RF performance, these parasitic capacitances should be low. At lower gate voltage, there is a slow increment in C_{gs} and C_{gd}, but at higher gate bias, there is a quick increment in C_{gs} and C_{gd} due to the enhancement of lateral electric field, which increases the carrier movement from drain to the source side. For the gate recessed 5 nm, a higher value of C_{gs} and a lower value of C_{gd} is observed at higher gate bias. Figure 10C exhibits the plot of cutoff frequency (f_T) with gate bias. From Equation (12), it is seen that f_T depends upon transconductance and parasitic capacitance. The higher value of parasitic capacitance for recessed depth 5 nm detroit the f_T, but the higher value of g_m significantly enhanced the f_T.

Figure 11A,B shows the graph of parasitic capacitance with frequency for different gate lengths. It has been observed that on reducing the gate length, the parasitic capacitance is reduced. For gate length 10 nm lower value of C_{gd} (140 fF/mm) and C_{gs} (350 fF/mm) has been observed

Ref	Year	L_g (nm)	I_d (A/mm)	g_m (S/mm)	f_T	f_{max}
[42]	2017	20	2.6	1.63	343	236
[36]	2017	30	2.1	1.05	350	340
[43]	2017	30	2.4	1.65	246	290
[15]	2019	10	2.5	1.43	524	758
[44]	2020	30	2.7	0.92	426	366
[45]	2020	30	0.6	0.2	50	150
[46]	2021	55	4.45	0.7	274	288
This work		10	2.8	1.55	583	840

TABLE 2 Latest research work on T-gate HEMT

for the proposed device, which significantly uplifts the RF performance of the device. Figure 12A exhibits the impact of gate length on f_T /f_{max}. On increasing the gate length, the value of f_T /f_{max} decreases due to the increment of parasitic capacitance. Figure 12B compares the proposed device with the various experimental and simulated results with different gate lengths. The higher value of f_T/f_{max} confirms that the proposed structure is appropriate for high-power millimeter-wave applications. The performance of a proposed device with the latest research work is listed in Table 2. Our proposed device shows the best results among the various published results.

5 | CONCLUSION

This paper investigates the DC and RF characteristics of 10 nm T-gate E mode InAlN/AlN. The polarization-induced doping in the buffer layer raises the buffer layer's potential, which significantly enhances the 2DEG confinement and reduces the buffer leakage current. The recessed T-gate structure further reduced the short channel effect (high on/off ratio 10^9, subthreshold swing 78 mV/dec, and DIBL 100 mV/V). The smaller 10 nm foot length reduced the parasitic capacitance C_{gd} (140 fF/mm), C_{gs} (350 fF/mm), and the highly doped source-drain region reduced the contact resistance. The above features in the proposed device significantly uplift the DC and RF performance. The higher drain current density (2.8 A/mm), transconductance (1.55 S/mm), breakdown voltage (33 V), cutoff frequency f_T (583 GHz), and maximum oscillation frequency f_{max} (840 GHz). The tremendous DC and RF performance of the proposed device exhibits the potential for high-power millimeter-wave applications.

ACKNOWLEDGMENT

The authors of this paper are obliged to Microelectronics lab, DTU, for their support.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

REFERENCES

1. Mishra UK, Parikh P, Wu YF. AlGaN/GaN HEMTs—an overview of device operation and applications. *Proc IEEE*. 2002; 90(6):1022-1031.
2. Mari D. Cermets and Hardmetals. *Encycl Mater Sci Technol*. 2001;96(2):1118-1122.
3. Frayssinet E, Knap W, Lorenzini P, et al. High electron mobility in AlGaN/GaN heterostructures grown on bulk GaN substrates. *Appl Phys Lett*. 2000;77(16):2551-2553.
4. Feng ZH, Zhou YG, Cai SJ, Lau KM. Enhanced thermal stability of the two-dimensional electron gas in GaN/AlGaN/GaN heterostructures by Si3N4 surface-passivation-induced strain solidification. *Appl Phys Lett*. 2004;85(22):5248-5250.
5. Lin Z, Kim H, Lee J, Lu W. Thermal stability of Schottky contacts on strained AlGaN/GaN heterostructures. *Appl Phys Lett*. 2004;84(9):1585-1587.
6. Kumar SP, Agarwal A, Chaujar R, Gupta RS. Device linearity and intermodulation distortion comparison of dual material gate and conventional AlGaN/GaN high electron mobility transistor. *Microelectronics Reliability*. 2011;51:587-596.
7. Shaveta HM, Ahmed M, Chaujar R. Rapid detection of biomolecules in a dielectric modulated GaN MOSHEMT. *J Mater Sci Mater Electron*. 2020;31:16609-16615.
8. Sano S, Ebihara K, Yamamoto T, Sato T, Miyazawa N. GaN HEMTs for wireless communication. *SEI Tech Rev*. 2018;86:65-70.
9. Neuburger M, Zimmermann T, Kohn E. Unstrained InAlN/GaN HEMT structure. *Int J High Speed Electron Syst*. 2004;14(3):785-790.
10. Kuzmik J. Power electronics on InAlN/(in)GaN: Prospect for a record performance. *IEEE Electron Device Lett*. 2001;22(11):510-512.
11. Cui P, Zeng Y. Electrical properties of 90-nm InAlN/GaN HEMT on a silicon substrate. *Phys E Low-Dimens Syst Nanostruct*. 2021;134:114821.
12. Cui P, Zeng Y. Technology of sub-100 nm InAlN/GaN HEMTs on silicon with suppressed leakage current. *Solid State Electron*. 2021;185:108137.
13. Chand N, Swain SK, Biswal SM, Sarkar A, Adak S. Comparative study on analog & RF parameter of InAlN/AlN/GaN normally off HEMTs with and without AlGaN Back barrier. *Devices Integr Circuit*. 2021;616-620.
14. Sharma M, Chaujar R. Impact of graded Back-barrier on linearity of recessed gate InAlN/GaN HEMT. *Proc 2nd Int Conf VLSI Device, Circuit Syst*. 2020;18-19.
15. C. Engineering, T. Nadu, E. Parthasarathy, C. Engineering, and T. Nadu, In AlN/GaN High Electron Mobility Transistor with In GaN Back barrier for Future High-Frequency Applications, vol. 20, no. 1, pp. 2186–2193, 2021.
16. M. Sharma and R. Chaujar, The Performance Analysis of 70nm T-gate InAlN/AlN MOS-HEMT using Graded Buffer, vol. 1, pp. 466–470, 2021.
17. Shrestha NM, Li Y, Chang EY. Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer. *Jpn J Appl Phys*. 2014;53:04EF081-04EF086. doi: 10.7567/jjap.53.04ef08
18. Khan MA, Kuznia JN, Van Hove JM, Pan N, Carter J. Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-AlxGa1-xN heterojunctions. *Appl Phys Lett*. 1992;60(24):3027-3029.
19. Pampili P, Parbrook PJ. Doping of III-nitride materials. *Mater Sci Semicond Process*. 2017;62:180-191.
20. Uren MJ, Moreke J, Kuball M. Buffer design to minimize current collapse in GaN/AlGaN HFETs. *IEEE Trans Electron Devices*. 2012;59(12):3327-3333.
21. Li S et al. Polarization induced pn-junction without dopant in graded AlGaN coherently strained on GaN. *Appl Phys Lett*. 2012;101(12):1221031-1221033. doi:10.1063/1.4753993
22. Jena D, Heikman S, Green D, et al. Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys. *Appl Phys Lett*. 2002;81(23):4395-4397.

23. Li S, Zhang T, Wu J, et al. Polarization induced hole doping in graded AlxGa 1-xN (x = 0.7 ∼ 1) layer grown by molecular beam epitaxy. *Appl Phys Lett*. 2013;102(6):1-4.
24. Yao C, Yang G, Li Y, et al. Investigation of N-face AlGaN ultraviolet light-emitting diodes with composition-varying AlGaN electron blocking layer. *Opt Quantum Electron*. 2016; 48(1):1-9.
25. Han T, Zhao H, Peng X, Li Y. Control of short-channel effects in InAlN/GaN high-electron-mobility transistors using graded AlGaN buffer. *Superlattices Microstruct*. 2018;116:207-214.
26. Li C et al. Improvement of breakdown and current collapse characteristics of GaN HEMT with a polarization-graded AlGaN buffer. *Semicond Sci Technol*. 2015;30(3):0350071-0350076. doi:10.1088/0268-1242/30/3/035007
27. Micovic M, Brown DF, Kurdoghlian A, et al. GaN DHFETs having 48% power added efficiency and 57% drain efficiency at V-band. *IEEE Electron Device Lett*. 2017;38(12):1708-1711.
28. Androse DR, Deb S, Radhakrishnan SK, Sekar E. T-gate AlGaN/GaN HEMT with effective recess engineering for enhancement mode operation. *Mater Today Proc*. 2021;45: 3556-3559.
29. Guo J, Li G, Faria F, et al. MBE-regrown ohmic in InAlN HEMTs with a regrowth interface resistance of 0.05 Ω̇mm. *IEEE Electron Device Lett*. 2012;33(4):525-527.
30. ATLAS User's Manual, SILVACO International, CA, USA, 2016.
31. Ambacher O, Majewski J, Miskys C, et al. Pyroelectric properties of Al(in)GaN/GaN hetero- and quantum well structures. *J Phys Condens Matter*. 2002;14(13):3399-3434.
32. Lenzlinger M, Snow EH. Fowler-Nordheim tunneling into thermally grown SiO2. *J Appl Phys*. 1969;40(1):278-283.
33. Shinohara K et al. Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency. *Tech Dig - Int Electron Devices Meet*. 2011;1200:453-456.
34. Qin J, Zhou Q, Liao B, Wang H. Modeling of 2DEG characteristics of InxAl1−xN/AlN/GaN-based HEMT considering polarization and quantum mechanical effect. *Electronics*. 2018;7(12): 4101-41012. doi:10.3390/electronics7120410
35. Tang Y, Shinohara K, Regan D, et al. Ultrahigh-speed GaN high-electron-mobility transistors with F_t/F_{max} of 454/444 GHz. *IEEE Electron Device Lett*. 2015;36:549e551.
36. Murugapandiyan P, Ravimaran S, William J. 30 nm T-gate enhancement-mode InAlN/AlN/GaN HEMT on SiC substrates for future high power RF applications. *J Semicond*. 2017;38(8): 1-6.
37. Shinohara K et al. 220GHz fT and 400GHz fmax in 40-nm GaN DH-HEMTs with re-grown ohmic. *2010 Int Electron Devices Meet*. 2010:3011-3014. doi:10.1109/IEDM.2010.5703448
38. Murugapandiyan P, Ravimaran S, William J. DC and microwave characteristics of Lg 50 nm T-gate InAlN/AlN/GaN HEMT for future high power RF applications. *AEU - Int J Electron Commun*. 2017;77:163-168.
39. Lv Y, Song X, Guo H, Fang Y, Feng Z. High-frequency AlGaN/GaN HFETs with f T/f max of 149/263 GHz for D-band PA applications. *Electron Lett*. 2016;52:1340-1342.
40. Rastogi G, Chaitanya MK, Khare S, et al. Performance improvement of Al0.3Ga0.7N/AlN/GaN HEMTs using nitrogen pretreated Si3N4 passivation. *Microelectron Eng*. 2021;249:111617.
41. Lenka TR, Dash GN, Panda AK. RF and microwave characteristics of a 10 nm thick InGaN-channel gate recessed HEMT. *J Semicond*. 2013;34(11):114003.
42. Murugapandiyan P, Ravimaran S, William J, Ajayan J, Nirmal D. DC and microwave characteristics of 20 nm T-gate InAlN/GaN high electron mobility transistor for high power RF applications. *Superlattices Microstruct*. 2017;109:725-734.
43. Murugapandiyan P, Ravimaran S, William J, Meenakshi Sundaram K. Design and analysis of 30 nm T-gate InAlN/GaN HEMT with AlGaN back-barrier for high power microwave applications. *Superlattices Microstruct*. 2017;111:1050-1057.
44. Murugapandiyan P, Mohanbabu A, Rajya Lakshmi V, et al. Performance analysis of HfO2/InAlN/AlN/GaN HEMT with AlN buffer layer for high power microwave applications. *J Sci Adv Mater Devices*. 2020;5(2):192-198.
45. H. T-gate, I. Four, and M. Kameche, Optimization of DC and AC performances for Al 0 . 26 Ga 0 . 74 N / GaN / 4H-SiC, vol. 13, no. 2, pp. 361–372, 2020.
46. Revathy A, Boopathi CS. Composite-channel In0.17Al0.83N/In0.1Ga0.9N/GaN/Al0.04Ga0.96N high electron mobility transistors for RF applications. *Int J RF Microw Comput Eng*. 2021;31(9): 1-13.

How to cite this article: Sharma M, Chaujar R. Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications. *Int J RF Microw Comput Aided Eng*. 2022;e23057. doi:10.1002/mmce.23057

Arabian Journal for Science and Engineering
https://doi.org/10.1007/s13369-021-06157-7

RESEARCH ARTICLE-PHYSICS

Design and Investigation of Recessed-T-Gate Double Channel HEMT with InGaN Back Barrier for Enhanced Performance

Megha Sharma[1] · **Rishu Chaujar**[1]

Received: 2 May 2021 / Accepted: 29 August 2021

Abstract
In this paper, a novel recessed T-gate double channel HEMT with InGaN back barrier has been designed and studied. The double channel is formed by the AlN layer's insertion below the InAlN/GaN interface, enhancing the drain current density (2.5A/mm). However, double channel HEMT suffers from a lack of gate controllability, due to which device performance decreases. This problem has been resolved by using the InGaN as a back barrier which enhances the carrier confinement of 2DEG by raising the conduction band for the GaN buffer and significantly enhances the gate controllability over a lower channel. Precisely a brief comparison has been done of the proposed device with conventional double channel HEMT. Performance parameters like drain current (I_{ds}), transconductance (g_m), intrinsic gain (A_v), output conductance (g_d), early voltage (V_{EA}), TGF, parasitic capacitances (C_{gs}, C_{gd}), cut-off frequency (f_T), maximum oscillation frequency (f_{max}), gain frequency product (GFP), transconductance frequency product (TFP), and gain transconductance frequency product (GTFP) have been investigated. Further, the improvement in linearity parameters such as VIP2, VIP3, IIP3, and 1-dB compression point has been observed by varying the back barrier distance from the lower channel.

Keywords Analog · Back barrier · Double channel · Heterostructure · Linearity · Recessed gate

1 Introduction

In recent years, the III-Nitride-based HEMTs attracted extensive attention in high power RF applications. The GaN material shows a high power output density than the GaAs at high frequency operation due to its larger bandgap, higher saturation velocity, and higher electron mobility [1–3]. Several research papers have been published to enhance the performance of AlGaN/GaN HEMTs [1–8]. To improve the RF performance of GaN HEMTs, the scaling of device dimension is required. The reduction of AlGaN barrier layer produces the unwanted strain at the lattice mismatched AlGaN/GaN junction. The AlGaN layer successfully replaced by the lattice matched InAlN layer with Al composition 0.83 [9] and significantly enhances the device performance. To achieve finer RF performance, it is important to reduce the gate length as the gate length reduces the parasitic capacitance reduces (C_{gs}, C_{gd}), which significantly uplifts the RF parameters. Much work has already been done on T-gate single channel HEMT with different types of buffer and back barrier engineering. Dong Seup Lee et al. demonstrated the 65 nm gate length passivated by Al_2O_3 layer with a back barrier layer, exhibits the drain current 1.49 A/mm and g_m of 539 mS/mm [10]. Sarosij Adak et al. designed the p-GaN back barrier HEMT with 150 nm gate length and recorded the drain current density 1.24 A/mm, g_m of 589 mS/mm [11], 70 nm gate length HEMT with graded buffer designed by Tieching Han et al. recorded the drain current 1.4 A/mm [12]. Although using the back barrier enhances the RF performance, but it also reduces the drain current density.

Double channel HEMTs (DC-HEMT) [13, 14] have recently emerged as a better alternative to single-channel HEMT. L. Ravikiran et al. demonstrated the AlGaN/GaN double heterojunction HEMT and exhibited the f_T/f_{max} 22/25 GHz [15]. Nisha Chugh et al. show the polarization-dependent charge control model for AlGaN/GaN DC-HEMT [14]. A DC-HEMT comprises two heterointerfaces which lead to forming the two 2DEGs. However, the DC-HEMT shows high current drivability due to the formation of two

✉ Rishu Chaujar
chaujar.rishu@dtu.ac.in

Megha Sharma
meghasharma_phd2k18@dtu.ac.in

[1] Department of Applied Physics, Delhi Technological University, Delhi, India

Published online: 18 September 2021

channels which is advantageous in RF circuit design [16, 17]. However, DC-HEMT suffers from the poor confinement of 2DEG and poor gate controllability over the lower channel, leading to the severe short channel effect. We need some buffer engineering to restrict the spilling of 2DEG in the buffer. The InGaN back barrier engineering was very impressive [18, 19]. It effectively reduced the short channel effect by confining the 2DEG in channel region. The gate recessed engineering further enhances the gate controllability over the channel and shift the threshold voltage toward the positive side.

This paper has proposed the recessed T-gate InAlN/AlN double channel HEMT with InGaN back barrier (DC-BB-HEMT). The analog and RF performance of double channel HEMT with a back barrier and DC-HEMT without a back barrier has been investigated. It has been observed that the proposed device's analog and RF performance are improved by introducing the back barrier. The effect of back barrier distance from the lower channel on linearity parameters has also been investigated.

2 Device Structure

Figure 1 exhibits the schematic structure of recessed 70 nm T-gate InAlN/AlN DC-BB-HEMT. All the parameters are defined in Table 1. The Al_2O_3 layer passivates the device to reduce the parasitic capacitance. The drain and source regions are doped with Si of order 10^{20} cm^{-3} to reduce the contact resistance. The first AlN layer placed below the InAlN layer enhances the mobility of 2DEG [20]. The distance between the first and second AlN layer is 10 nm. The second AlN layer formed the second triangular quantum well at the interface of AlN (2)/GaN and formed the second channel. The 2 nm InGaN back barrier layer is placed below the lower channel to enhance the 2DEG confinement [18, 19].

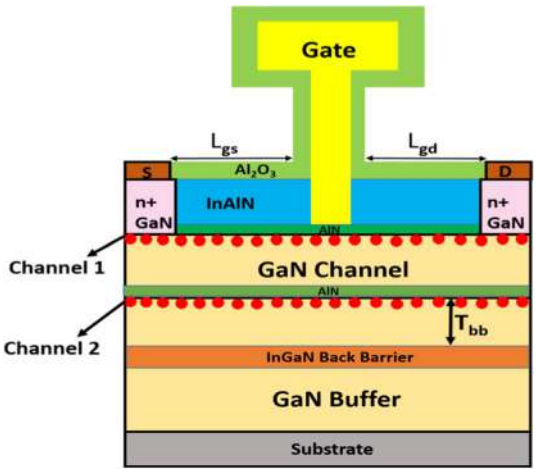

Fig. 1 Proposed structure of InAlN/AlN T-gate DC-BB-HEMT

Table 1 Design parameters of DC-BB-HEMT and DC- HEMT

Device Parameter	DC-HEMT	DC-BB-HEMT
Gate length (L_g)	70 nm	70 nm
Al_2O_3 passivation layer	10 nm	10 nm
Distance b/w two channels	10 nm	10 nm
Distance b/w lower channel and back barrier (T_{bb})	30 nm	30 nm
Source to gate length (L_{gs})	400 nm	400 nm
Gate to drain length (L_{gd})	1.5 µm	1.5 µm
Barrier layer (InAlN)	10 nm	10 nm
AlN layer	1 nm	1 nm
InGaN back barrier	–	2 nm
GaN buffer	1.5 µm	1.5 µm
Source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Gate width	2×50 µm	2×50 µm
Gate stem height	100 nm	100 nm
Gate head	400 nm	400 nm

3 Experimental Calibration and Models

The Atlas-Silvaco simulator has been used for simulating the proposed structure [21]. The models which are used in simulating the proposed structure are low field mobility, Fermi–Dirac, high field mobility, polarization, and Shockley–Read–Hall model. The electron trapping mechanism has been calculated by the SRH model. The mobility models are used to calculate the scattering mechanism [21]. Both models are defined in Eq. (1) and (2), respectively.

1. High Field Mobility Model

$$\mu(E) = \frac{\mu(N,T) + V_{sat}\frac{E(N_1-1)}{E_C{}^{N_1}}}{1 + a_n\left(\frac{E}{E_C}\right)^{N_2} + \left(\frac{E}{E_C}\right)^{N_1}} \tag{1}$$

where E and v_{sat} are the electric fields and saturated velocity of electrons and E_C, a_n, N_1, N_2 are coefficients.

2. Low Field Mobility Model

$$\frac{1}{\mu(T,\ N)} = a\left(\frac{N}{N^{ref}}\right)\left(\frac{T}{300}\right)^{-15} \times \ln\left[1 + 3\left(\frac{T}{300}\right)^{2}\left(\frac{N}{N^{ref}}\right)^{\frac{-2}{3}}\right] + b\left(\frac{T}{300}\right)^{1.5} + \frac{c}{\left(e^{\frac{1065}{T}}\right) - 1} \tag{2}$$

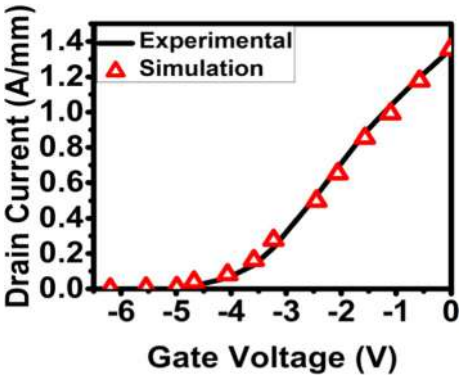

Fig. 2 Show the transfer characteristics of InAlN/AlN T-gate HEMT with $L_g = 70$ nm, $V_d = 5$ V and $W_g = 2 \times 40$ µm compare with the experimental data

where µ(T, N) is the mobility as a function of the doping and ambient temperature.

3. Total Polarization Model

In GaN-based devices, the two types of polarization have been induced, i.e., piezoelectric and spontaneous polarization. The total polarization model is defined in Eq. (3) [22]:

$$P_{total} = [(P_{PE} + P_{SP})(bottom)] - [(P_{PE} + P_{SP})(top)] \quad (3)$$

The above-mentioned models have been calibrated with the experimental paper of Han Tingting et al. [23]. Figure 2 exhibits the simulated and experimental I_d-V_g curve of 70 nm T-gate InAlN/GaN HEMT at $V_{ds} = 5$ V. It has been observed that the experimental result exhibits a good agreement with the simulated result.

4 Results and Discussion

4.1 Band Diagram and Electron Concentration

In this section, we have investigated the conduction band discontinuity and electron concentration of both devices. Figure 3 exhibits the conduction band diagram of both devices. Two quantum wells, i.e., primary quantum well and secondary quantum, are formed in the proposed device. The primary quantum well is generate at the interface of AlN (1)/GaN. This quantum depth is relatively deeper, which generates the major upper channel region and accumulates the highest electron concentration. The second quantum well is formed at the interface of AlN (2)/GaN, which generates the second channel. In Fig. 3, it can be seen that in DC-BB-HEMT, a sharp notch is formed at the back of the lower channel. This notch is formed by the induced polarization

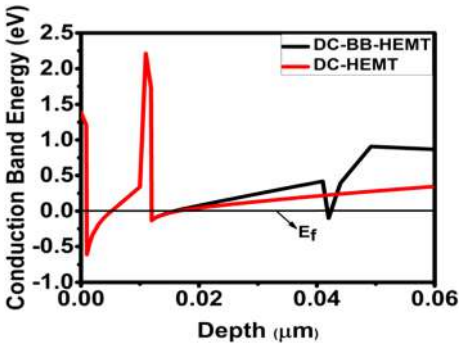

Fig. 3 Conduction band diagram of DC-BB-HEMT & DC-HEMT

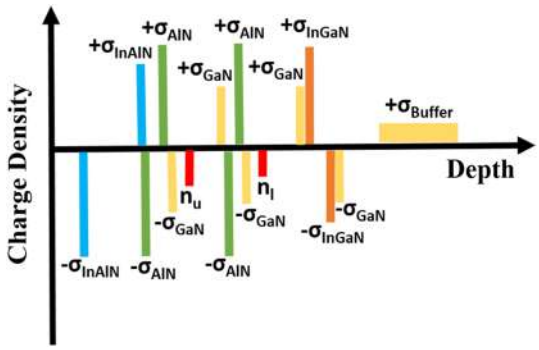

Fig. 4 Polarization charge distribution of each layer in DC-BB-HEMT

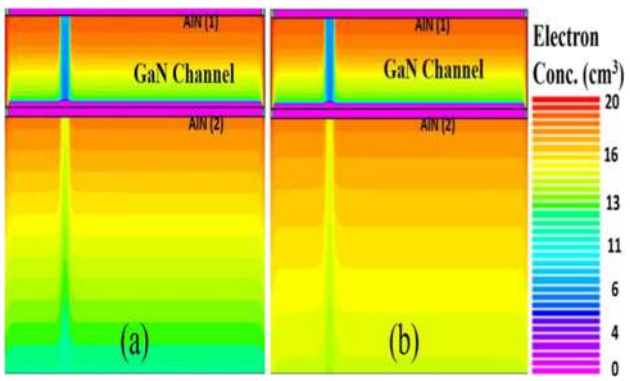

Fig. 5 Electron concentration contour plot of **a** DC-BB-HEMT **b** DC-HEMT

charges between the InGaN and GaN, which raises the potential barrier and confines the electron in the channel region, thereby enhancing the gate controllability over the lower channel.

Figure 4 exhibits the charge distribution of DC-BB-HEMT. Piezoelectric and spontaneous polarization charges are induced at the interface of layers. Due to the polarization effect, negative and positive polarization charges are induced on each

layer's opposite sides. The value of these polarization charges is calculated using [22]. Figure 5a and b show the electron concentration contour plot of DC-BB-HEMT and DC-HEMT. The higher electron concentration has been observed at AlN (1)/GaN heterojunction interface, which formed the major channel, whereas at the AlN (2)/GaN interface, the minor channel is formed. In Fig. 5a, the electron concentration below the lower channel is reduced more significantly than the Fig. 5b, which attributes to the fact that the insertion of InGaN layer restricts the diffusion and leakage of electron toward the buffer layer and considerably enhances the electron confinement.

4.2 Analog Performance of DC-BB-HEMT & DC-HEMT

Figure 6 reflects the drain current characteristics for DC-BB-HEMT and DC-HEMT devices. Initially, channel 2 is in ON-state due to the lack of gate controllability over channel 2 in DC-HEMT, and the negative threshold voltage is observed. As the gate voltage is increased, channel 1 is turned on, which is a major channel as it has a higher 2DEG density. When channel 1 is turned on, it screened channel 2 and saturates the 2DEG in channel 2. The InGaN back barrier's presence enhances the 2DEG confinement, increases the gate controllability over channel 2, and significantly shifts the threshold voltage toward the positive side. The drain current density in DC-BB-HEMT is (2.2A/mm) is obtained at $V_{gs}=3$ V, which is about 16.6% lower than the DC-HEMT (2.59A/mm). This decrement of current density due to the shift of threshold voltage of DC-BB-HEMT (0.3 V) toward the positive side about 1.5 V compared with DC-HEMT (− 1.8 V).

In this subsection, we have investigated the analog parameters such as g_m, TGF, g_d, V_{EA}, and A_v of the proposed device for the analog applications and compared them with the conventional device. The mathematical formulation of these parameters is shown below [24]:

$$g_m = \partial I_d/\partial V_{gs} \tag{4}$$

$$\mathrm{TGF} = g_m/I_d \tag{5}$$

$$g_d = \partial I_d/\partial V_{ds} \tag{6}$$

$$V_{EA} = I_d/g_d \tag{7}$$

$$A_v = g_m/g_d = (g_m/I_d) \times V_{EA} \tag{8}$$

Figure 7a shows the plot of transconductance with gate voltage for both devices. Transconductance is defined as the change in the drain current to the gate voltage at constant drain voltage. In Fig. 7a, double peaks, i.e., primary and secondary peaks, have been observed in the transconductance graph due to the formation of two channels. The higher primary peak is observed for the DC-BB-HEMT at $V_{gs}=0.8$ V due to the improvement of electron confinement and gate controllability for channel 2 by the InGaN back barrier. Simultaneously, the secondary peak for both the devices is comparable, which shows that the InGaN back barrier layer does not affect channel 1. Figure 7b exhibits the plot of transconductance generation factor (TGF) for both devices. It is an essential analog parameter which is defined as the ratio of transconductance and drain current. TGF also expressed as available gain/dissipate power [25, 26], where gain and power dissipation are represented by the g_m and drain current. The minimum value of TGF will lower the input driveability and dissipate the high power at the load. In Fig. 7b, at smaller $V_{gs,}$ high peak of TGF is obtained for DC-BB-HEMT (32 V^{-1}), which is about 10 times larger than the DC-HEMT (1.73 V^{-1}). The TGF value

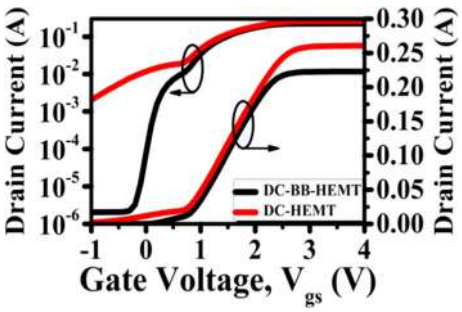

Fig. 6 Drain current characteristics of DC-BB-HEMT and DC-HEMT

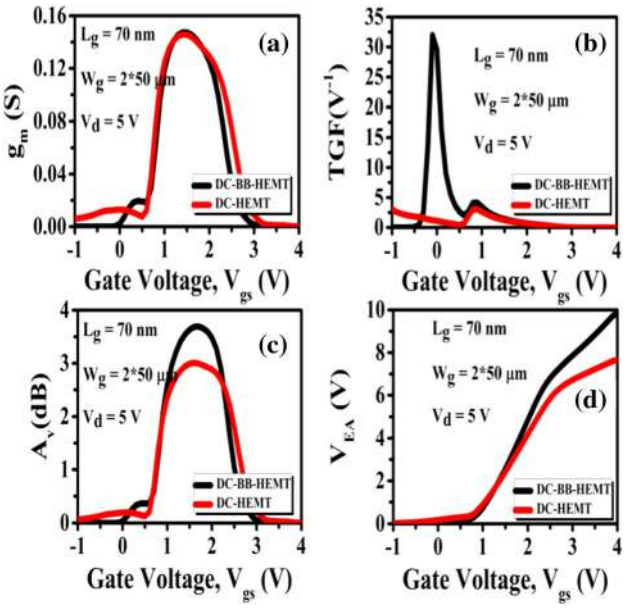

Fig. 7 **a** Transconductance **b** TGF **c** Intrinsic gain **d** Early voltage for both devices

is decreased as the gate bias increases, because of the enhancement of drain current at higher gate voltage.

Figure 7c shows the variation of intrinsic gain with gate bias. The high peak of intrinsic gain for DC-BB-HEMT (4 dB) observed at $V_{gs} = 1.5$ V. Intrinsic gain depends on the two factors: transconductance and output conductance. The decrement of output conductance significantly enhances the intrinsic gain of about 50% in the proposed device. Figure 7d exhibits the early voltage variation with gate bias for both structures. Early voltage is expressed as the ratio of drain current and output conductance. For better analog performance, both intrinsic gain and early voltage should be high. The early voltage for DC-BB-HEMT is 10 V observed, which is 53% higher than the DC-HEMT (6.5 V). This enhancement in the early voltage is because of the lower output conductance, which enhances the proposed structure's analog performance. The plot of output conductance for DC-BB-HEMT and DC-HEMT with drain bias is exhibited in Fig. 8. Output conductance calculates the driving ability of the device. At lower drain voltage, the higher value of output conductance is obtained. As the V_{ds} increases, the output conductance is decreased exponentially. Due to the higher gate controllability, minimum output conductance is observed for DC-BB-HEMT as compared to DC-HEMT.

4.3 RF Performance of DC-BB-HEMT and DC-HEMT

In this section, small-signal AC analysis has been performed with an operating frequency of 1 MHz for DC-BB-HEMT and DC-HEMT. All the RF parameters such as f_T, f_{max}, GFP, GTFP, and TFP have been investigated. The mathematical formulation of these parameters is listed below [26]:

$$f_T \approx g_m/2\pi(C_{gs} + C_{gd}) \tag{9}$$

$$f_{max} = f_T/\sqrt{4R_g(g_{ds} + 2\pi f_T C_{gd})} \tag{10}$$

$$\text{GFP} = (g_m/g_d) \times f_T \tag{11}$$

$$\text{TFP} = (g_m/I_d) \times f_T \tag{12}$$

$$\text{GTFP} = (g_m/g_d) \times (g_m/I_d) \times f_T \tag{13}$$

Figure 9a and b exhibit the plot of the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) with gate bias. For better RF performance, these parasitic capacitances should be low. At lower gate voltage, there is a slow increment in C_{gs} and C_{gd}, but at higher gate bias, there is a quick increment in C_{gs} and C_{gd} because of the enhancement of lateral electric field, which enhances the carrier movement from drain to the source side. The DC-BB-HEMT shows a lower value of C_{gs} and C_{gd} in comparison with the DC-HEMT. At the metal/InAlN interface, charges increase due to the higher sheet charge density in the quantum well, which enhances the capacitance for DC-HEMT.

Figure 9c exhibits the plot of cut-off frequency (f_T) with gate voltage. The cut-off frequency is defined as the frequency at which current gain reduces to unity. From Eq. (9), it is seen that f_T depends upon transconductance and parasitic capacitance. The double peak structure has been observed, the same as the transconductance curve Fig. 7a. The primary and secondary peaks are formed due to channel 2 and channel 1. The InGaN back barrier's presence increases the primary transconductance peak, which further enhances the cut-off frequency. The secondary transconductance peak is not affected by the InGaN back barrier, but the parasitic capacitance for the DC-BB-HEMT is lower, enhancing the cut-off frequency. The cut-off frequency obtained for DC-BB-HEMT (153 GHz) is 11.7%

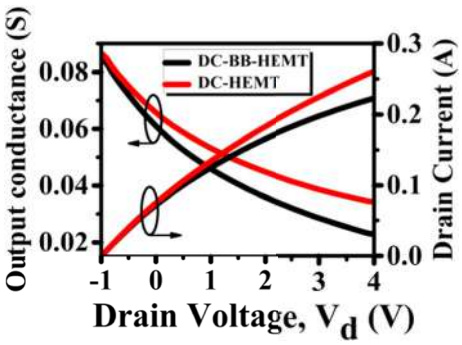

Fig. 8 Output conductance for both devices

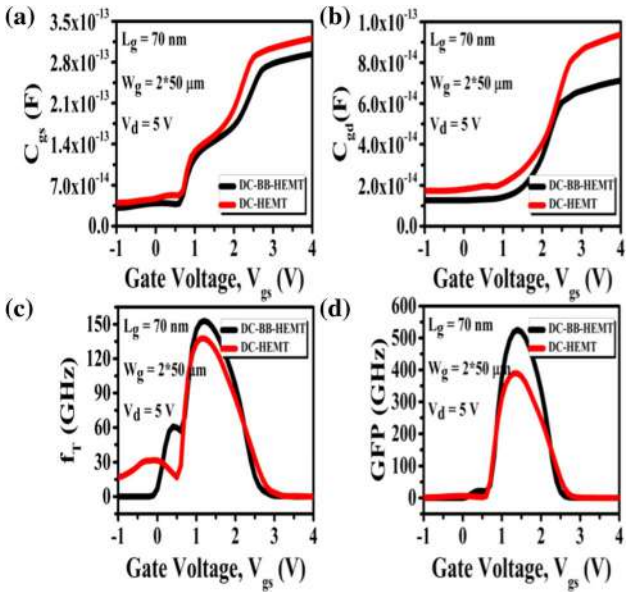

Fig. 9 Variation of **a** Cgs **b** Cgd **c** fT **d** GFP for both devices

higher than the DC-HEMT (136 GHz). In Fig. 9d, the gain frequency product (GFP) has been plotted against the gate bias. The GFP is another essential parameter for the high frequency application. Initially, with increasing the gate voltage, GFP increases linearly and holds an optimum value, after that, it decreases in the saturation region. The higher peak of GFP obtained for DC-BB-HEMT is 526 GHz which is about 35.2% higher than the DC-HEMT (389 GHz). GFP improvement in DC-BB-HEMT is mainly due to the increment in cut-off frequency, transconductance, and reduction of output conductance.

Variation of the drain to source conductance (g_{ds}) and maximum oscillation frequency (f_{max}) with gate bias is shown in Fig. 10a and b. The maximum oscillation frequency is defined as the frequency at which max unilateral gain reduces to unity. Equation (10) shows that the f_{max} depends upon parasitic capacitance, drain to source conductance (g_{ds}), and f_T. The 2 times higher f_{max} is obtained for DC-BB-HEMT (92 GHz) in comparison with DC-HEMT (36 GHz) due to the lower parasitic capacitance (C_{gd}), g_{ds}, and higher f_T.

Variation of transconductance frequency product (TFP) with gate bias is shown in Fig. 10c. TFP is utilized in moderate to high-speed design. In Fig. 10c, higher primary and secondary peaks are observed for the DC-BB-HEMT than the DC-HEMT due to the higher g_m, f_T, and lower I_d. Gain transconductance frequency product (GTFP) is another essential FOM that gives critical information regarding the circuit designing by determining the perfect region to achieve the tradeoff among the gain, transconductance, and device speed. In Fig. 10d, the higher value of GTFP is

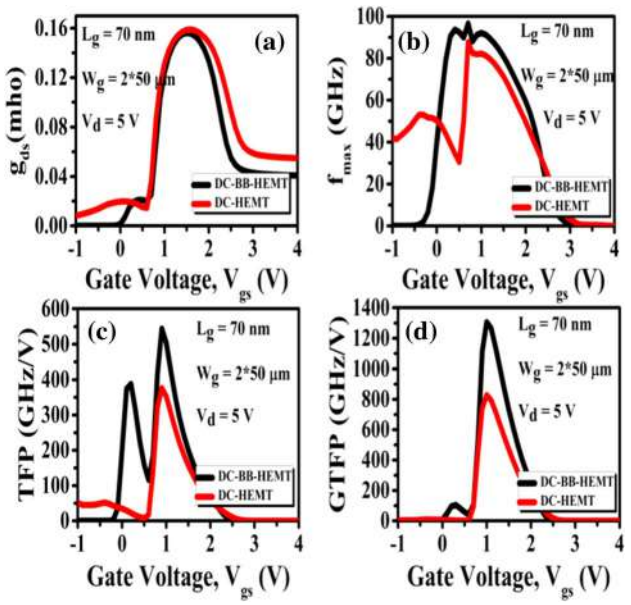

Fig. 10 Variation of **a** gds **b** fmax **c** TFP **d** GTFP with gate bias

observed for DC-BB-HEMT (1310 GHz/V), which is about 57% higher than the DC-HEMT (828 GHz/V). The improvement of these parameters for DC-BB-HEMT is mainly due to the improvement of g_m and reduction of output conductance.

4.4 Linearity Analysis of DC-BB-HEMT for Variable Tbb

Figure 11a and b exhibit the drain current and transconductance characteristics for different T_{bb} values. It has been observed that while increasing the BB distance from the lower channel, the drain current and transconductance characteristics improved. As the back barrier distance increases from 10 to 30 nm, the drain current density also increases. A higher value of drain current is observed 2.3 A/mm for 30 nm T_{bb}. On increasing the back barrier distance, the second quantum depth increases, which results in the enhancement of 2DEG concentration. Improvement in transconductance characteristics on increasing the back barrier distance is basically due to the lower scattering and higher mobility of 2DEG. When the InGaN back barrier is placed near the lower channel, the mobility of 2DEG is badly affected by the back barrier due to the alloy disorder scattering mechanism.

The investigation of nonlinear parameters is very important as they are the primary source of distortion. So to achieve high linearity, the nonlinear parameters should be low. The second- and third-order transconductance parameters (gm_2, gm_3) are the nonlinear parameters. Figure 11c and d exhibits the plot of nonlinear parameters with gate voltage for different back barrier distance. It has been observed that by increasing the T_{bb} from 10 to 30 nm, the nonlinear parameters are almost comparable, which shows increasing the back barrier distance does not affect the nonlinear parameters. The linearity parameters are mathematically expressed as [27].

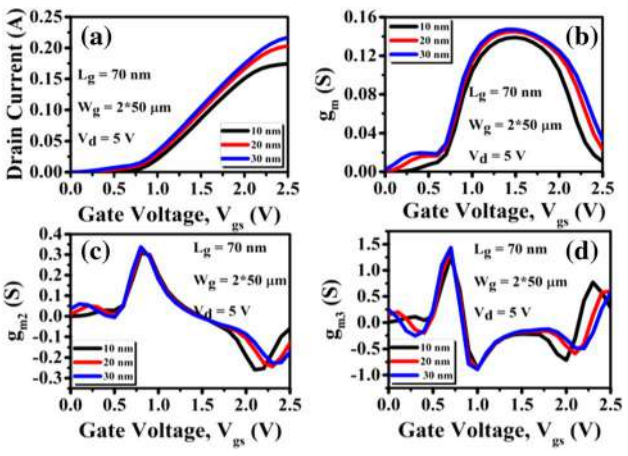

Fig. 11 **a** Transfer characteristics **b** transconductance **c** gm2 **d** gm3 for both devices

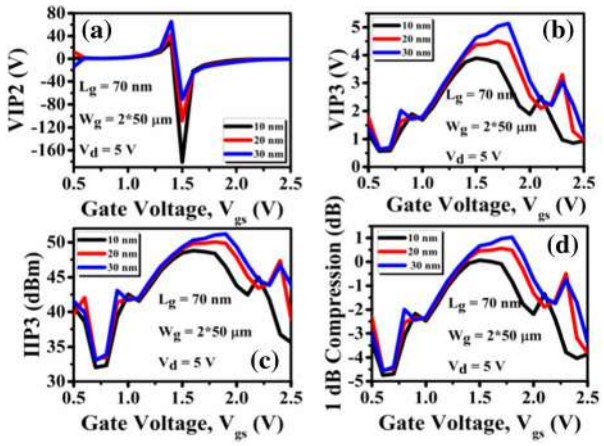

Fig. 12 Variation of linearity parameters with gate bias for different back barrier distance **a** VIP2 **b** VIP3 **c** IIP3 **d** 1-dB compression point

$$\mathrm{VIP2} = 4 \times \left(g_m/g_{m2}\right) \tag{14}$$

$$\mathrm{VIP3} = \sqrt{24 \times \left(g_m/g_{m3}\right)} \tag{15}$$

$$\mathrm{IIP3} = (2/3) \times \left(g_m/\left(g_{m3}R_s\right)\right) \tag{16}$$

$$1-\mathrm{dB\ compression\ point} = 0.22 \times \sqrt{\left(g_m/g_{m3}\right)} \tag{17}$$

VIP2 and VIP3 express the extrapolated gate voltage amplitude at which second- and third-order harmonics equal the fundamental tone in device current (I_{ds}). These FOMs can accurately investigate the distortion characteristics from DC parameters. In order to attain high linearity and low distortion, these parameters should be as high as possible. Figure 12a and b exhibit the graph of VIP2 and VIP3 with gate bias for different back barrier distance. It has been observed that by increasing the T_{bb} from 10 to 30 nm, VIP2 and VIP3 increase. The higher peak of VIP2 and VIP3 is observed 65.3 V and 5.1 V for 30 nm T_{bb} which is 2 times higher than the 10 nm T_{bb} (29 V and 2.9 V). As shown in Eqs. (14) and (15), VIP2 and VIP3 parameters depend upon the transconductance and the second- and third-order transconductance. Due to the lower scattering disorder and higher mobility of 2DEG, higher g_m has been obtained for 30 nm T_{bb}.

Third-order input intercept point (IIP3) and 1-dB compression point are other essential FOMs investigating linearity performance. IIP3 exhibits the extrapolated input power at which first and third harmonics are equal. Figure 12c shows the variation of IIP3 with gate bias for variable T_{bb}. The IIP3 parameter also increases on increasing the back barrier distance from the lower channel. The higher peak of IIP3 observed at $V_{gs} = 1.8$ V is 51 dBm for 30 nm T_{bb} which is about 10% higher than the 10 nm T_{bb} (46 dBm). 1-dB compression point is defined as the input power value at which the gain of the amplifier drops by 1-dB. The study of this parameter is essential for the amplifier circuit. It estimates the maximum input power that the circuit can handle by providing a fixed amount of gain. As the input power surpasses the 1-dB compression point, then gain starts decreasing. Thus, it is important to have a high 1-dB point. Figure 12d exhibits the higher peak of 1 dB compression point for 30 nm (1.3 dB), which is 8 times higher than the 10 nm (−8.1 dB) and emphasizes the superior linearity performance of DC-BB- HEMT with 30 nm T_{bb}. Thus, results reflect that RF harmonic distortion and linearity improve by increasing the InGaN back barrier distance from the lower channel.

5 Conclusion

The work presented in this paper concentrates on the impact of the InGaN back barrier on the analog/RF and linearity performance of the double channel T-gate HEMT. The proposed device exhibited improved results as compared to the conventional device. For analog performance, intrinsic gain increased by 50%, TGF increased by 477%, and early voltage was enhanced by 23%. The cut-off frequency increased by 11.7% for RF performance, maximum oscillation frequency raised by 10%, GFP, TFP, and GTFP increased by 36%, 44%, and 57%, respectively. The proposed device's linearity performance with varying back barrier distance shows the improved results for the 30 nm back barrier distance. Thus, inserting the InGaN back barrier in double channel HEMT enhances the device's analog/RF performance. The careful optimization of the back barrier distance further enhances the device's linearity performance.

Acknowledgements Authors are grateful to Microelectronics Lab, Applied Physics Deptt., DTU, to support the work.

Authors' Contribution All the authors to this study are conception and design.

Funding No funding has been received to carry out this study.

Availability of Data and Material The above-mentioned authors have all the relevant data associated with this research work and will be dedicated to share that, if they will be asked to do so in future.

Declarations

Conflict of Interest The authors declare that they have no conflict of interest.

Ethical Approval All the Ethical Standards have been seen by the authors and will supposed to follow them in future as well.

References

1. Mishra, U.K.; Parikh, P.; Wu, Y.F.: AlGaN/GaN HEMTs - An overview of device operation and applications. Proc. IEEE **90**(6), 1022–1031 (2002). https://doi.org/10.1109/JPROC.2002.1021567
2. Mari, D.: Cermets and Hardmetals. Encycl. Mater. Sci. Technol. **96**(2), 1118–1122 (2001). https://doi.org/10.1016/b0-08-043152-6/00209-6
3. Frayssinet, E., et al.: High electron mobility in AlGaN/GaN heterostructures grown on bulk GaN substrates. Appl. Phys. Lett. **77**(16), 2551–2553 (2000). https://doi.org/10.1063/1.1318236
4. Feng, Z.H.; Zhou, Y.G.; Cai, S.J.; Lau, K.M.: Enhanced thermal stability of the two-dimensional electron gas in GaN/AlGaN/GaN heterostructures by Si3N4 surface-passivation-induced strain solidification. Appl. Phys. Lett. **85**(22), 5248–5250 (2004). https://doi.org/10.1063/1.1828231
5. Lin, Z.; Kim, H.; Lee, J.; Lu, W.: Thermal stability of Schottky contacts on strained AlGaN/GaN heterostructures. Appl. Phys. Lett. **84**(9), 1585–1587 (2004). https://doi.org/10.1063/1.1650875
6. Kumar, S. P.; Agarwal, A.; Chaujar, R.; Gupta, R.S.: Device linearity and intermodulation distortion comparison of dual material gate and conventional AlGaN/GaN high electron mobility transistor. *Microelectron*, 51, 587–596, 2011.
7. Ahmed, H.M.; Chaujar, R.: Rapid detection of biomolecules in a dielectric modulated GaN MOSHEMT. J. Mater. Sci.: Mater. Electron. **31**(19), 16609–16615 (2020)
8. Sano, S.; Ebihara, K.; Yamamoto, T.; Sato, T.; Miyazawa, N.: GaN HEMTs for wireless communication. SEI Tech. Rev. **86**, 65–70 (2018)
9. Neuburger, M.; Zimmermann, T.; and Kohn, E.: Unstrained InAlN/GaN HEMT Structure. 14(3), 785–790, 2004.
10. Lee, D.S.; Gao, X.; Guo, S.; Palacios, T.: InAlN/GaN HEMTs with AlGaN back barriers. IEEE Electron Device Lett. **32**(5), 617–619 (2011). https://doi.org/10.1109/LED.2011.2111352
11. Adak, S.; Sarkar, A.; Swain, S.; Pardeshi, H.; Pati, S.K.; Sarkar, C.K.: High performance AlInN/AlN/GaN p-GaN back barrier Gate-Recessed Enhancement-Mode HEMT. Superlattices Microstruct. **75**, 347–357 (2014). https://doi.org/10.1016/j.spmi.2014.07.036
12. Han, T.; Zhao, H.; Peng, X.; Li, Y.: Control of short-channel effects in InAlN/GaN high-electron mobility transistors using graded AlGaN buffer. Superlattices Microstruct. **116**, 207–214 (2018). https://doi.org/10.1016/j.spmi.2018.02.031
13. Zhang, W., et al.: Trap state analysis in AlGaN/GaN/AlGaN double heterostructure high electron mobility transistors at high temperatures. Appl. Phys. Lett. **110**(25), 252102 (2017)
14. Chugh, N.; Bhattacharya, M.; Kumar, M.; Deswal, S.S.; Gupta, R.S.: Polarization dependent charge control model for microwave performance assessment of AlGaN/GaN/AlGaN double heterostructure HEMTs. J. Comput. Electron. **17**(3), 1229–1240 (2018). https://doi.org/10.1007/s10825-018-1190-0
15. Ravikiran, L., et al.: Growth and characterization of AlGaN/GaN/AlGaN double-heterojunction high-electron-mobility transistors on 100-mm Si (111) using ammonia-molecular beam epitaxy. J. Appl. Phys. **117**(2), 025301 (2015)
16. Jha, S.K.; Surya, C.; Chen, K.J.; Lau, K.M.; Jelencovic, E.: Low-frequency noise properties of double channel AlGaN/GaN HEMTs. Solid. State. Electron. **52**(5), 606–611 (2008). https://doi.org/10.1016/j.sse.2007.10.002
17. Chu, R.; Zhou, Y.; Liu, J.; Wang, D.; Chen, K.J.; Lau, K.M.: AlGaN-GaN double-channel HEMTs. IEEE Trans. Electron Devices **52**(4), 438–446 (2005)
18. Lee, D.S.; Gao, X.; Guo, S.; Kopp, D.; Fay, P.; Palacios, T.: 300-GHz InAlN/GaN HEMTs With. IEEE Electron Device Lett. **32**(11), 1525–1527 (2011)
19. Palacios, T.; Chakraborty, A.; Heikman, S.; Keller, S.; DenBaars, S.P.; Mishra, U.K.: AlGaN/GaN high electron mobility transistors with InGaN back-barriers. IEEE Electron Device Lett. **27**(1), 13–15 (2006). https://doi.org/10.1109/LED.2005.860882
20. Shrestha, N.M.; Li, Y.; Chang, E.Y.: Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer. Jpn. J. Appl. Phys. **53** (2014)
21. ATLAS User's Manual: SILVACO International. CA, USA (2016)
22. Ambacher, O., et al.: Pyroelectric properties of Al (In) GaN/GaN hetero- and. J. Phys. Condens. Matter **14**, 3399–3434 (2002)
23. Wang, R., et al.: Gate-recessed enhancement-mode InAlN/AlN/GaN HEMTs with 1.9-A/mm drain current density and 800-ms/mm transconductance. IEEE Electron Device Lett. **31**(12), 1383–1385 (2010). https://doi.org/10.1109/LED.2010.2072771
24. Kumar, B.; Chaujar, R.: Analog and RF performance evaluation of junctionless accumulation mode (JAM) gate stack gate all around (GS-GAA) FinFET. SILICON **13**(3), 919–927 (2021)
25. Pardeshi, H.: Superlattices and microstructures analog/RF performance of AlInN/GaN underlap DG MOS- HEMT. Superlattices Microstruct. **88**, 508–517 (2015)
26. Chaujar, R.; Kaur, R.; Saxena, M.; Gupta, M.; Gupta, R.S.: Laterally amalgamated DUal material GAte Concave (L-DUMGAC) MOSFET for ULSI. Microelectron. Eng. **85**(3), 566–576 (2008). https://doi.org/10.1016/j.mee.2007.10.002
27. Kumar, B.; Chaujar, R.: TCAD Temperature analysis of gate stack gate all around (GS-GAA) FinFET for improved RF and wireless performance. SILICON (2021). https://doi.org/10.1007/s12633-021-01040-4

Materials Science and Engineering B 290 (2023) 116298

Contents lists available at ScienceDirect

Materials Science & Engineering B

journal homepage: www.elsevier.com/locate/mseb

Polarization induced doping and high-k passivation engineering on T-gate MOS-HEMT for improved RF/microwave performance

Megha Sharma, Bhavya Kumar, Rishu Chaujar *

Department of Applied Physics, Delhi Technological University, Delhi, India

ARTICLE INFO

Keywords:
Heterostructure
Polarization
Conduction band
Cut-off frequency
T-shaped gate

ABSTRACT

High electron-mobility transistors (HEMTs) based on III-nitrides are well-known as ideal choices for high-power, radio-frequency applications. HEMTs, on the other hand, must deal with the critical issues of the large gate and buffer leakage currents, which unavoidably restrict device performance and reliability. Here, we use HfO_2 as a gate dielectric to mimic an InAlN/AlN meta-oxidesemiconductor high electron mobility transistor (MOS-HEMT) that can enhance the interfacial and transport characteristics and reduce the gate leakage current. Furthermore, polarization-induced doping in the buffer region is also implemented, enhancing the two-dimensional electron gas confinement by bending the conduction band upwardly convex, effectively reducing the buffer leakage current, and enhancing the breakdown voltage (35 V). The implementation of the above two engineerings significantly enhances the gain maximum oscillation frequency (246 GHz) and cut-off frequency (156 GHz). The simulated results of the proposed device design show its applicability for high RF/microwave applications.

1. Introduction

For many years, silicon technology has been the most important part of the semiconductor business. Nowadays, silicon-based devices such as nanowires [1,2], cylindrical gates [3,4], recessed channels [5-7], MOSFETs, and FinFETs [8-10] are reaching their theoretical operating limit, and so are not capable of achieving the performance expected by future RF and microwave applications. In addition, the poor carrier mobility and saturation velocity make it unsuitable for current electronic applications like television broadcasting and mobile communications. As a result, novel materials such as SiGe, SiC, and group III-V semiconductors have been researched as potential replacements for current silicon technology. The III-Nitride-based HEMTs have shown their dominance in radar, military, and telecommunication [11] due to the remarkable features of GaN devices, i.e., larger bandgap, greater breakdown voltage, and decent mobility thermal conductivity.

Furthermore, the polarization effect in GaN HEMTs caused the creation of a two-dimensional electron gas (also known as 2DEG) at the interface between the two materials, boosting electron mobility and making the GaN-based device ideal for high-power applications. AlGaN/GaN HEMTs have already shown their applicability for high-power applications. To increase the operating frequency of GaN HEMTs to be used in mm-wave devices, it is important to reduce the device's size to the nanoscale range. The AlGaN/GaN heterostructure based on ultrathin barriers has continued to be a difficult task [12]. Enhanced polarization, improved thermal stability, and a significant increase in drain current density have been achieved in $In_{0.17}Al_{0.83}N$/GaN-based lattice-matched heterostructure [13]. Despite the significant increase in operating frequency, HEMTs based on InAlN have a problem with a low breakdown voltage, high leakage currents, and severe short-channel effects. Many investigations have recently described the usage of metal-oxidesemiconductor (MOS) structures to minimize gate leakage current and acquire considerable pinch-off characteristics. SiO_2 [14,15], ZnO [16], Al_2O_3 [17], and ferroelectric material [18] have also been employed as gate dielectrics in nitride-HEMTs to create a more effective MOS structure. However, dielectric engineering increases the distance from the channel to the gate electrode, lowering the device's transconductance (g_m). Recently, high-k materials such as HfO_2 emerged as potential gate-insulating material that enhances the device's stability and transport performance [19]. However, gate oxide engineering is not enough to enhance the device's performance. To lower the leakage current from the buffer and raise the breakdown voltage of the device, some ingenious buffer engineering is also needed.

This article focuses on gate and buffer engineering of the InAlN/GaN HEMT device. The proposed device surface is rendered passive by the HfO_2 layer, which helps to reduce the parasitic capacitance. The source/

* Corresponding author.
E-mail addresses: meghasharma_phd2k18@dtu.ac.in (M. Sharma), bhavyakumar_phd2k18@dtu.ac.in (B. Kumar), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.mseb.2023.116298
Received 14 November 2022; Received in revised form 9 January 2023; Accepted 17 January 2023
Available online 23 January 2023

drain region is highly doped, reducing the contact resistance. The introduction of HfO_2 below the gate reduced the gate leakage current. Furthermore, constructive buffer engineering has been done. Initially used, Fe doping [20] is replaced by polarization-induced doping by changing the Al composition of AlGaN material in the buffer region. Although Fe or C doping in the buffer region enhances the resistivity in the buffer, it also creates deep-level acceptors that further increase the current collapse [21].

The polarization doping in the buffer layer acts as a blocking layer that hinders the 2DEG in the buffer region, effectively enhances the breakdown voltage (V_{br}), and reduces the buffer leakage current. The collective implementation of the high-k gate dielectric and polarization-induce doping on the proposed structure enhances the device's RF performance and makes it suitable for millimeter-wave applications. This article is broken down into the following sections: Section 2 discusses the construction of the device and the simulation models, Section 3 discusses the possibility of fabricating the device, Section 4 analyses the device's RF and microwave performance, and the paper concludes in Section 5.

2. Device design and simulation model

Fig. 1 illustrates the device's two-dimensional structure. The design parameters are tabulated in Table 1. The T-shaped gate structure is used to reduce the parasitic capacitance of the device. Passivating the device's surface with HfO_2 improves the device's radio frequency (RF) performance. A 5 nm HfO_2 is introduced below the gate. AlGaN-graded buffer layer is used, which changes the Al composition from 0.2 to 0 along the (0001) direction. The negative polarization charge field in the buffer was generated by this linear compositional change. Based on the polarization field's divergence, we can calculate the induced charge density as -.

$$\rho = -\nabla \hat{A} \cdot P = -\frac{\partial P}{\partial Z} \tag{1}$$

The negative polarization charge field induces corresponding holes because of charge neutrality. For this reason, the buffer leakage current is much reduced as the high-density polarization-induced holes more deeply compensate the bulk-free electrons. To carry out the proposed structure simulation process, we have used the Silvaco TCAD software [22]. Table 2 lists the models used in the simulation procedure [23].

Table 1
Design Parameters of PD-MOS-HEMT.

Parameters	Values
Buffer layer	1.5 μm
Channel layer	30 nm
Spacer layer	1 nm
Barrier layer	10 nm
Passivation layer (HfO_2)	20 nm
Drain/source doping	1×10^{20} cm^{-3}
Gate to source length	400 nm
Gate to drain length	1 μm
Gate oxide (HfO_2)	5 nm
Gate width	100 μm
Gate length	70 nm

3. Experimental calibration and fabrication feasibility

In Fig. 2, the physical models are calibrated with the experimental paper [24]. The simulated and experimental results exhibit a definitive agreement. The unintentional n-type doping is involved in all simulations with low density (1×10^{16} cm^{-3}). The acceptor-like traps with energy level and trap density 0.5 eV and 5×10^{16} cm^{-3} below the conduction band are introduced. Moreover, the donor-like traps with energy level and trap density 0.42 eV and 3.86×10^{13} cm^{-3} below the conduction band are also considered. The progression of the manufacturing process for the proposed structure is shown in Fig. 3.

For the suggested device, there are two techniques for fabrication: bottom-up and top-down. The epitaxial stack (InAlN/AlN/GaN/AlGaN) is grown on the SiC substrate utilizing the bottom-up technique. From the top down, gate patterning and source/drain mesas are created. The molecular beam epitaxy (MBE) is used to build the epitaxial stack [25]. MBE with a SiO_2 growth mask is used to produce the ohmic source/drain n++ GaN areas [26]. The HfO_2 gate dielectric with a thickness of 5 nm is deposited using tetrakis dimethyl amido-hafnium [27]. After that, a T gate is formed with the use of electron beam lithography [28]. Finally, a buffered oxide etchant was used to remove the HfO_2 from the gate-drain and gate-source regions. A 20-nm HfO_2 layer was then deposited to passivate the surface.

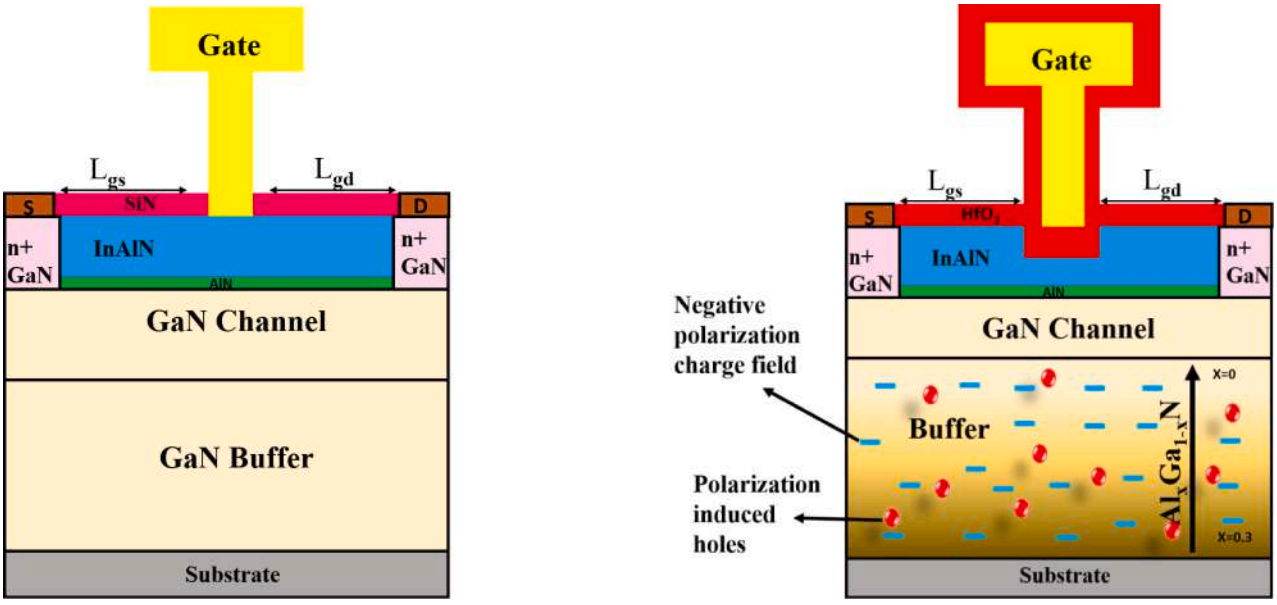

Fig. 1. (a)T-gate HEMT with GaN buffer (b) Proposed T-gate MOS-HEMT with polarized doped buffer.

Table 2
Physical Models [22].

Models	Formula used	Explanation
Mobility Model (High Field)	$\mu(E) = \frac{\mu(N,T) + V_{sat}\frac{E(N_1-1)}{E_C{}^{N_1}}}{1 + a_n\left(\frac{E}{E_C}\right)^{N_2} + \left(\frac{E}{E_C}\right)^{N_1}}$	The electric field accelerate the holes and electron due to which they lose their momentum and lead to the scattering process. Therefore, mobility models have been used to calculate the scattering mechanism in the device
Mobility Model (Low Field)	$\frac{1}{\mu(T,\ N)} = a\left(\frac{N}{N^{ref}}\right)\left(\frac{T}{300}\right)^{-15} \times \ln\left[1 + 3\left(\frac{T}{300}\right)^{2}\left(\frac{N}{N^{ref}}\right)^{-\frac{2}{3}}\right] + b\left(\frac{T}{300}\right)^{1.5} + \frac{c}{(e^{1065/T}) - 1}$	The Albrecht model is used for the low field mobility. The ALBRCT statement is used to specified the model.
Polarization Model [23]	$P_{total} = [(P_{PE} + P_{SP.})(bottom)] - [(P_{PE} + P_{SP.})(top)]$	The wurtzite crystal structure of III-nitrides is pyroelectric in nature. They possess the two types of polarization:- piezoelectric (P_{PE}) and spontaneous (P_{SP}) polarization.
Recombination Model	$R^{SRH} = \frac{pn - n_i{}^2}{\tau_p\left[n + n_i exp\left(\frac{E_{trap}}{kT}\right)\right] + \tau_n\left[p + n_i exp\left(\frac{-E_{trap}}{kT}\right)\right]}$	Shockley-Read-Hall (SRH) investigates the electron trapping process at each trap level
Impact Ionization	$G = \frac{\alpha_n\lvert J_n\rvert + \alpha_p\lvert J_p\rvert}{q}$	Impact ionization model is used to investigate the device breakdown voltage.

4. Results and discussion

4.1. Conduction band

The conduction band of the polarization-doped MOS-HEMT (PD-MOS-HEMT) at zero gate bias is exhibited in Fig. 4. The band diagram explains the electron confinement in the channel region and 2DEG formation at AlN/GaN interface. The heterostructure's bandgap discontinuity causes band bending; a quantum well is generated at the AlN/GaN interface because GaN's conduction band is below the Fermi level, as illustrated in the inset graph Fig. 4. The electrons that live in the well are constrained to behave in accordance with the properties of electron waves. The device can construct a 2DEG due to the large band discontinuity and strong polarization effect caused by the InAlN/GaN heterojunction. Using Eq. (2) [23], we can determine the 2DEG concentration.

$$n_s = \frac{1}{(d_{InAlN} + d_{AlN})} \times \{\frac{\sigma_{InAlN} \times d_{InAlN}}{e} + \frac{\sigma_{AlN} \times d_{AlN}}{e} - \frac{\varepsilon(x)\varepsilon_0}{e^2} \times \{e\varnothing_b(x) + E_F[x, n_s(x)] - \Delta E_{c,AlN/GaN} + \Delta E_{c,InAlN/GaN}(x)\}\} \quad (2)$$

Furthermore, polarization doping in the buffer region effectively raises the buffer potential and reduces the buffer leakage current.

4.2. DC and RF characteristics

Fig. 5 depicts the drain current and transconductance characteristics for four different structures: conventional HEMT (GaN-HEMT), high k dielectric MOS-HEMT, polarization doped HEMT(PD-HEMT), and proposed structure (PD-MOS-HEMT). It has been observed that the insertion of HfO_2 below the gate significantly shifts the threshold voltage toward the positive side, as shown in Fig. 5(a). This shift is due to the reduction of the gate-to-channel distance. The polarization-induced doping in the buffer region reduced the off-state current (10^{-13}), as shown in Fig. 5(b). The polarization doping in the buffer layer acts as a blocking layer that hinders the 2DEG in the buffer region, effectively suppressed the buffer leakage current. The transconductance curve for all four devices is shown in Fig. 5(c). It can be observed that the insertion of a high k gate dielectric significantly enhances the transconductance by about 170 % as compared to the conventional HEMT due to the high gate leakage blocking ability. Whereas 51 % enhancement in transconductance is observed for PD-HEMT. Hence the collective engineering of high k gate dielectric and polarization induces doping in the buffer region in the proposed structure (PD-MOS-HEMT), significantly shifts the threshold voltage positive side, reduces off current (10^{-14}), and enhances the transconductance (900 mS/mm) about 215 %.

For different drain voltages, the drain current and transconductance are shown in Fig. 6(a, b). With the increase in drain voltage by 3 V, the drain current and transconductance rise. The channel region's lateral electric field and electron velocity improve as drain voltage rises. Fig. 6 (c) exhibit the breakdown characteristics for both structure. For RF applications, the most important metric to consider is the breakdown voltage. Compared to the GaN- HEMT, the PD-MOS-HEMT has a much greater breakdown voltage (35 V). The increment in breakdown voltage is because of the presence of polarization-induced negative charges that uplift the conduction band of the buffer layer and constrain the spilling of 2DEG into the buffer. Because of this, the leakage current in the buffer dramatically decreased.

Fig. 7(a) shows the gain frequency product (GFP) plot with the gate bias. The value of GFP increases linearly with gate bias; afterward, it decreases at high gate voltage. A PD-MOS-HEMT has a greater GFP value, which is 91.1 % higher than a GaN-HEMT. The mathematical formulation of GFP is expressed by Eq. (3) [29]. Improvement in GFP value for the PD-MOS-HEMT is due to the higher value of g_m, F_t, and lower g_d of the PD-MOS-HEMT. Fig. 7(b) exhibits the transconductance frequency product (TFP) graph with gate voltage. TFP depends upon the g_m and F_t parameters. The higher value of g_m and F_t of the PD-MOS-HEMT leads to enhancing the TFP value, which is three times higher than the GaN-HEMT. Fig. 7(c) exhibits the gain transconductance frequency product (GTFP) graph. There is shown to be a high peak of GTFP for a PD-MOS-HEMT, which is seen to be four times greater than the GaN-HEMT. Increased GTFP in PD-MOS-HEMTs may be attributed to their enhanced transconductance and decreased gd. The mathematical expression of TFP and GTFP is expressed by Eq. (4–5) [30,31].

$$GFP = \left(\frac{g_m}{g_d}\right) \times F_t \quad (3)$$

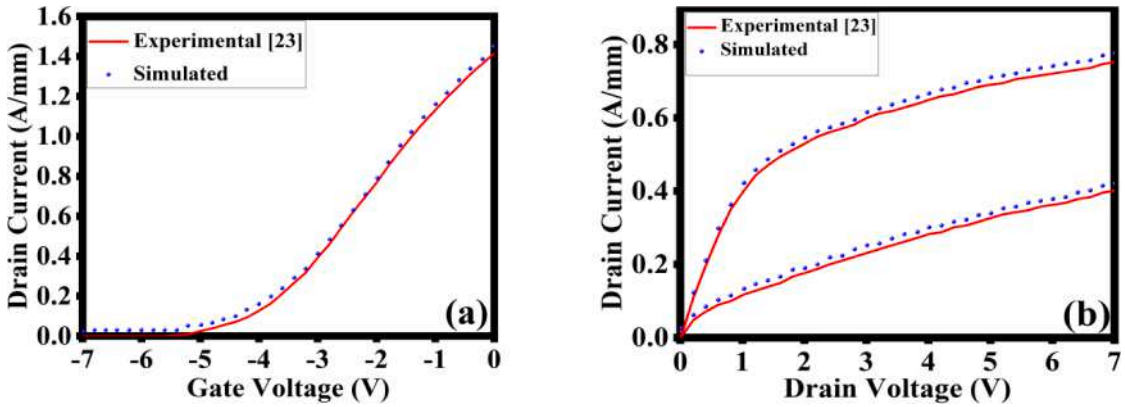

Fig. 2. (a) Transfer V_{ds} = 7 V (b) V_{gs} = -3V, −2V output characteristics of experimental and simulated results.

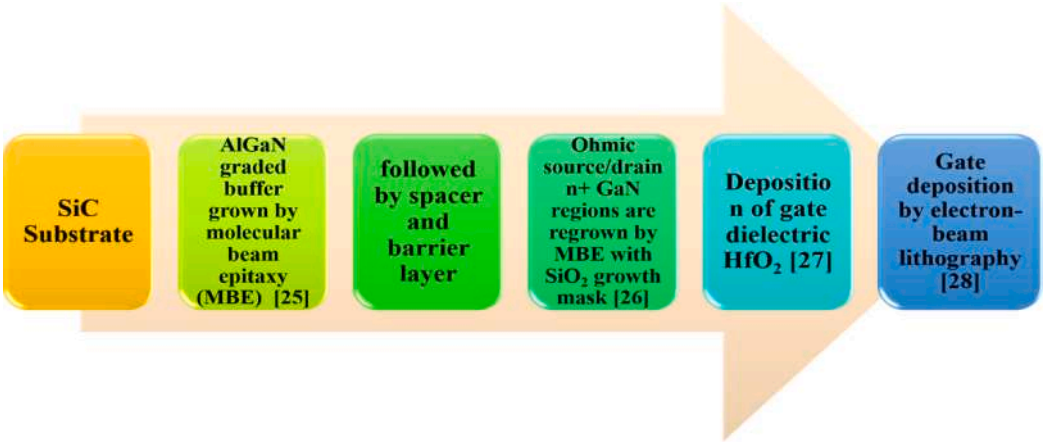

Fig. 3. Fabrication flow of PD-MOS-HEMT.

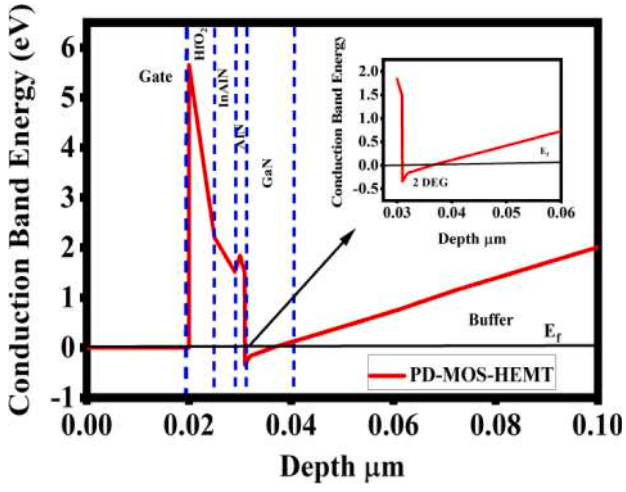

Fig. 4. Conduction band diagram of PD-MOS-HEMT.

$$TFP = \left(\frac{g_m}{I_d}\right) \times F_t \quad (4)$$

$$GTFP = \left(\frac{g_m}{g_d}\right) \times \left(\frac{g_m}{I_d}\right) \times F_t \quad (5)$$

4.3. Small signal analysis

This section studies the small-signal behavior of the PD-MOS-HEMT at a higher frequency. The S-parameter measurement is the best way to study the transistor's small-signal behavior at high frequencies. The S11 and S22 parameters measure the port's input and output reflection coefficients. These parameters determine how well the port impedance and the terminating impedance line up. In most RF circuits, matching is essential. The reflection coefficient becomes zero when the reflected wave matches perfectly. Fig. 8(a, b) exhibits the input and output reflection coefficients of PD-MOS-HEMT and GaN-.

HEMT. It has been witnessed that the input and output coefficient declines at a higher frequency, and this reduction is higher in PD-MOS-HEMT. The reflection coefficient lowers when the port's matching improves due to lower reflected power. Fig. 8(c, d) exhibits the graph of reverse and forward transmission coefficients (S12, S21) for both devices. These transmission coefficient increases for PD-MOS-HEMT. Fig. 9 (a, b) depicted the variation of current gain (h21) and unilateral power gain (U) with frequency for both structures. Eq. (6–7) expresses the mathematical expression of current and unilateral power gain in S-parameters [32-36].

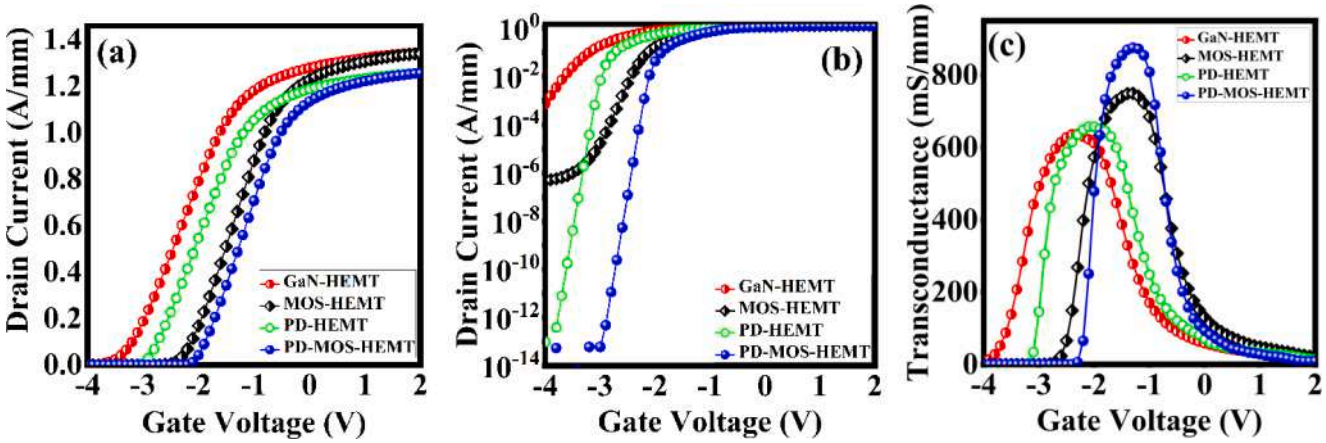

Fig. 5. (a) Drain current (b) log scale (c) Transconductance for different devices.

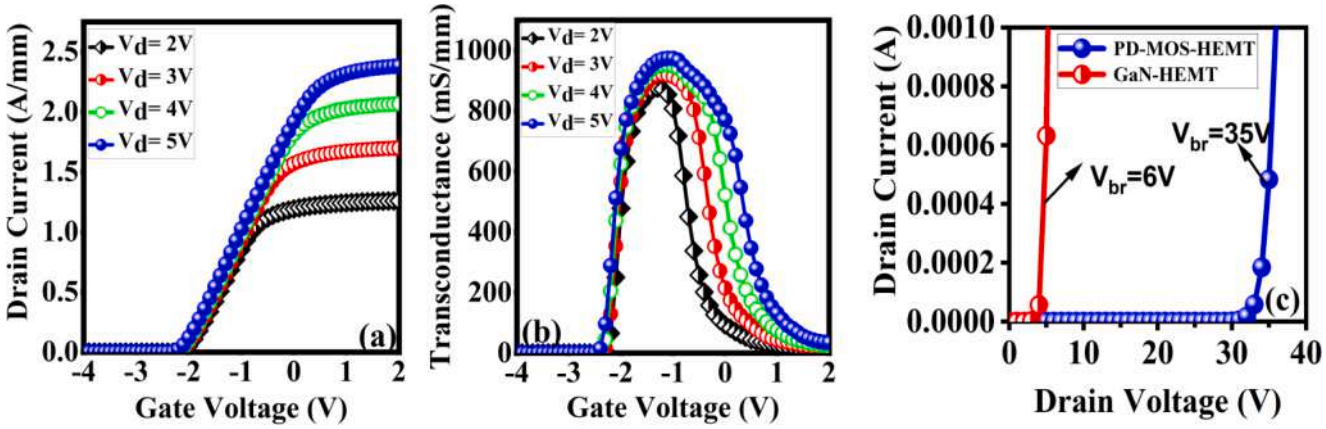

Fig. 6. (a) Drain current (b) transconductance for variable drain voltage (c) breakdown voltage.

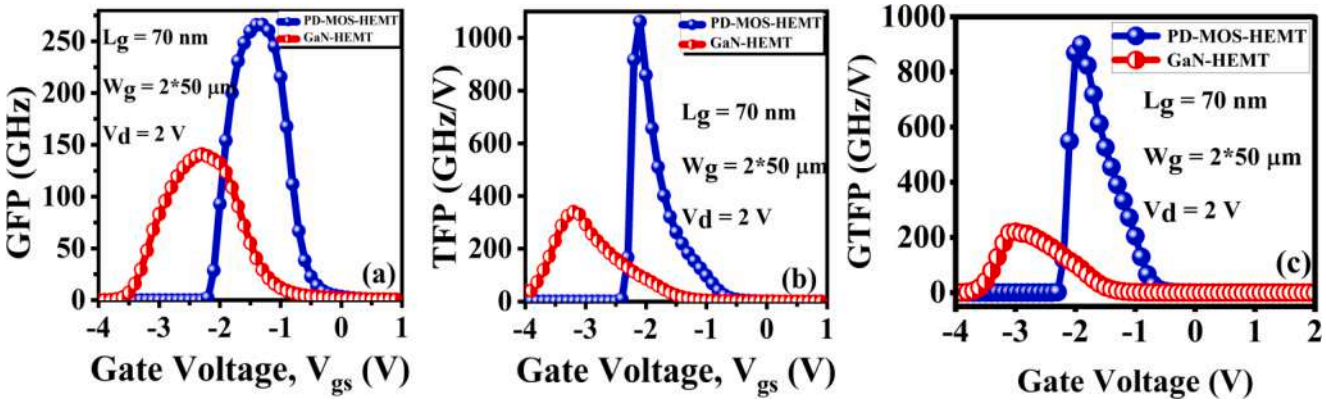

Fig. 7. Comparison of (a) GFP (b) TFP (c) GTFP for both the structures.

$$h_{21} = \left| \frac{-2S_{21}}{(1 - S_{11}) \times (2 - S_{22}) - S_{12} \times S_{21}} \right| \quad (6)$$

$$U = \left(\frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right) \times \left(1 - |S_{22}|^2\right)} \right) \quad (7)$$

$$Gma = \frac{P_{load\ max}}{P_{source\ max}} \quad (8)$$

$$K = \frac{1 - |S_{21}|^2 - |S_{12}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 \times |S_{12}|^2 \times |S_{12}|^2} \quad (9)$$

$$MSG = \frac{|S_{21}|^2}{|S_{12}|^2} \times \left(K \pm \sqrt{(K^2 - 1)} \right) \quad (10)$$

The device's F_t and F_{max} are obtained when current and unilateral power gain reaches unity. The inset bar graph of Fig. 9(a, b) exhibits the F_t (156 GHz) and F_{max} (246 GHz) for PD-MOS-HEMT, which is 56 % and 75 % more efficient than the GaN-HEMT. Fig. 9(c) exhibits the graph of

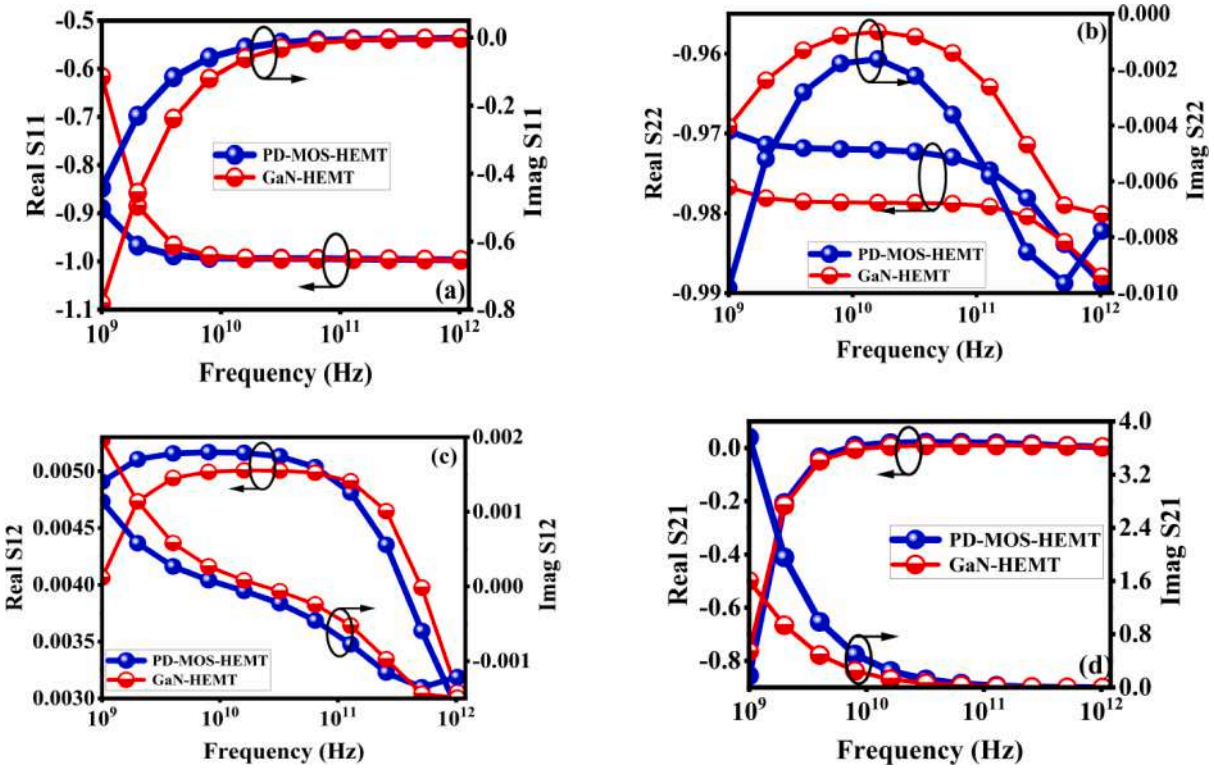

Fig. 8. S- parameters (a) S11 (b) S22 (c) S12 (d) S21 for both the structures.

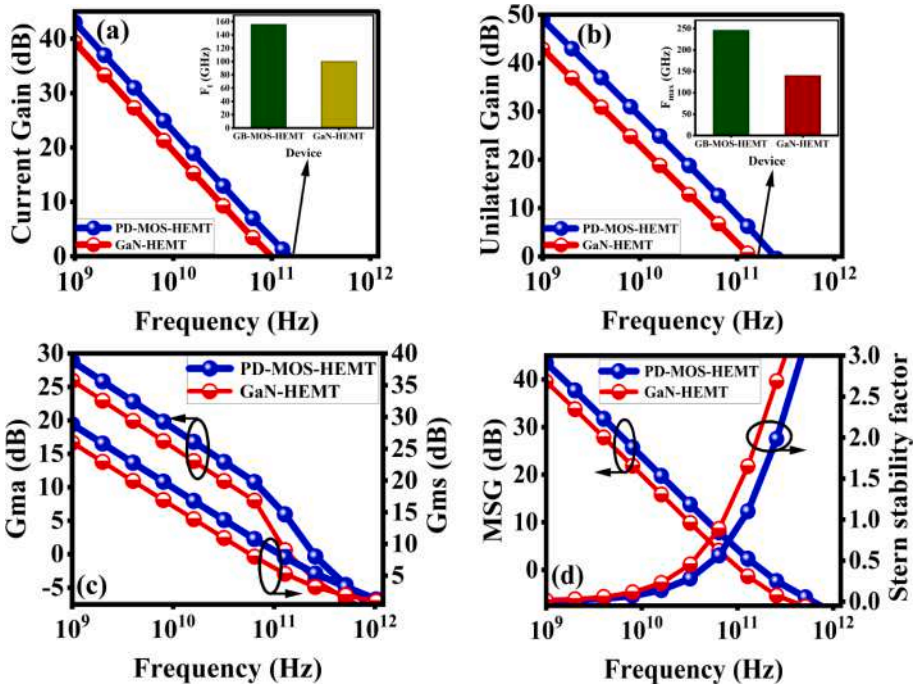

Fig. 9. Variation of (a) current gain (b) unilateral gain (c) Gma and Gms (d) MSG and stability factor for both the structures.

the device's maximum stable and available power gain Gms and Gma. The expression of Gma is defined by Eq. (8) [37]. For RF amplifier design, the study of Gma and Gms is important. Fig. 9(c) shows that Gma and Gms get enhanced by 50 % and 40 % for the PD-MOS-HEMT.

A microwave transistor can amplify or sustain the oscillation A microwave transistor can amplify or sustain oscillation in the circuit. Whether the transistor in the circuit oscillates or not depends upon the input and output load impedance. The choice of stability of the device is important while designing the amplifier; otherwise, the amplifier will turn into an oscillator. R.F. transistors whose operating frequency greater than the critical frequency (f_k) are unconditionally stable, and if the operating frequency is lower than the f_k, then.

the transistor is conditionally stable. The rollett stability factor ($K > 1$) is the sufficient condition for the device's stability [34]. The K value

indicates whether the device oscillates or not. The K > 1 shows the conjugate matching of input and output loads. This is the standard stability criteria, and the circuit is unconditionally stable. Once the stability condition is satisfied, the maximum stable gain (MSG) is calculated using the stability factor and S parameters, as shown in Eq. (9, 10). The stability factor and MSG for PD-MOS-HEMT and GaN-HEMT are demonstrated in Fig. 9(d). A 75 % improvement in MSG is observed for PD-MOS-HEMT, whereas a high stability factor is observed for GaN-HEMT. The stability factor PD-MOS-HEMT is K > 1 for high frequency and K < 1 for low frequency, which is suitable for designing the amplifier.

5. Conclusion

This work explored the performance analysis of high-k passivated InAlN/AlN/polarization doped buffer MOS-HEMT. The RF/microwave performance of the device is greatly improved by using high-k dielectric and polarization-doped engineering in the buffer zone. The simulation results showed a five times enhancement of breakdown voltage, 91 % improvement in gain frequency product, four and three times enhancement in gain transconductance frequency product and TFP, 56 % and 75 % improvement in F_t and F_{max}. The five times enhancement in maximum available gain and 40 % increment in maximum stable gain have been observed for PD-MOS-HEMT. The simulation findings revealed that the PD-MOS-HEMT is an appropriate candidate for RF/microwave applications.

Availability of Data & Material

The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] A. Abdelmoneam, B. Iñiguez, M. Fedawy, "Compact modelling of quantum confinement in III-V gate all around nanowire MOSFET," in: 2018 IEEE Spanish Conference on Electron Devices (CDE), 2018, pp. 1-4, DOI: 10.1109/CDE.2018.8597131.

[2] O. Muscato, T. Castiglione, and A. Coco, "Hydrodynamic modeling of electron transport in gated silicon nanowires transistors," Atti della Accademia Peloritana Dei Pericolanti-Classe di Scienze Fisiche, vol. 97, no. S1, 2019, DOI: 10.1478/AAPP.97S1A18.

[3] C.P. Auth, J.D. Plummer, Scaling theory for cylindrical, fully depleted, surrounding-gate MOSFETs, IEEE Electron Device Lett. 18 (2) (1997) 74–76, https://doi.org/10.1109/55.553049.

[4] A. Sarkar, S. De, A. Dey, C.K. Sarkar, Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model, J. Comput. Electron 11 (2) (2012) 182–195, https://doi.org/10.1007/s10825-012-0396-9.

[5] A. Kumar, M. Tripathi, R. Chaujar, Comprehensive analysis of sub-20 nm black phosphorus-based junctionless-recessed channel MOSFET for analog/RF applications, Superlattice Microst. 116 (2018) 171–180, https://doi.org/10.1016/j.spmi.2018.02.018.

[6] A. Kumar, Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC MOSFET, Superlattice Microst. 109 (2017) 626–640, https://doi.org/10.1016/j.spmi.2017.05.045.

[7] A. Kumar, M.M. Tripathi, R. Chaujar, Reliability issues of In_2O_5Sn gate electrode Recessed Channel MOSFET: impact of Interface trap charges and temperature, IEEE Trans. Electron Devices 65 (3) (2018) 860–866, https://doi.org/10.1109/TED.2018.2793853.

[8] A. Kumar, N. Gupta, S. Kumar, M.M. Tripathi, R. Chaujar, Performance evaluation of linearity and intermodulation distortion of nanoscale GaN-SOI FinFET for RFIC design, AEU-Int. J. Electron. C. 115 (2020), 153052, https://doi.org/10.1016/j.aeue.2019.153052.

[9] B. Kumar, R. Chaujar, Numerical simulation of analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for ULSI switching applications, Eur. Phys. J. Plus 137 (2022) 110, https://doi.org/10.1140/epjp/s13360-021-02269-z.

[10] B. Kumar, R. Chaujar, Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance, SILICON 14 (2022) 309–321, https://doi.org/10.1007/s12633-021-01395-8.

[11] U.K. Mishra, P. Parikh, Y.F. Wu, AlGaN/GaN HEMTs - An overview of device operation and applications, Proc. IEEE 90 (6) (2002) 1022–1031, https://doi.org/10.1109/JPROC.2002.1021567.

[12] M. Higashiwaki, T. Mimura, and T. Matsui, "Gallium Nitride Materials and Devices III," International Society for Optics and Photonics, vol. 6894, pp. 293-301, 2008.

[13] M. Neuburger, T. Zimmermann, E. Kohn, Unstrained InAlN/GaN HEMT structure, Int J High-Speed Electron Syst 14 (3) (2004) 785–790, https://doi.org/10.1142/S0129156404002831.

[14] M.A. Khan, et al., AlGaN/GaN metal oxide semiconductor heterostructure field effect transistor, IEEE Electron Device Lett. 21 (2) (2000) 63–65, https://doi.org/10.1109/55.821668.

[15] R. Brown, et al., A Sub-Critical Barrier Thickness Normally-Off AlGaN/GaN MOS-HEMT, IEEE Electron Device Lett. 35 (9) (2014) 906–908, https://doi.org/10.1109/LED.2014.2334394.

[16] C. Lee, Y. Chiou, C. Lee, AlGaN/GaN MOS-HEMTs With Gate ZnO Dielectric Layer, IEEE Electron Device Lett. 31 (11) (2010) 1220–1223, https://doi.org/10.1109/LED.2010.2066543.

[17] H. Liu, B. Chou, W. Hsu, C. Lee, J. Sheu, C. Ho, Enhanced AlGaN/GaN MOS-HEMT Performance by Using Hydrogen Peroxide Oxidation Technique, IEEE Trans. Electron Devices 60 (1) (2013) 213–220, https://doi.org/10.1109/TED.2012.2227325.

[18] L. Qi, S. Ruan, Y.-J. Zeng, Review on Recent Developments in 2D Ferroelectrics: Theories and Applications, Adv. Mater 33 (2021) 2005098, https://doi.org/10.1002/adma.202005098.

[19] Y. Yue, et al., AlGaN/GaN MOS-HEMT With HfO_2 Dielectric and Al_2O_3 Interfacial Passivation Layer Grown by Atomic Layer Deposition, IEEE Electron Device Lett. 29 (8) (2008) 838–840, https://doi.org/10.1109/LED.2008.2000949.

[20] P. Pampili, P.J. Parbrook, Doping of III-nitride materials, Mater. Sci. Semicond. Process. 62 (11) (2017) 180–191, https://doi.org/10.1016/j.mssp.2016.11.

[21] M.J. Uren, J. Moreke, M. Kuball, Buffer design to minimize current collapse in GaN/AlGaN HFETs, IEEE Trans. Electron Devices 59 (12) (2012) 3327–3333, https://doi.org/10.1109/TED.2012.2216535.

[22] ATLAS User's Manual, SILVACO International, CA, USA, 2016.

[23] O. Ambacher, et al., Pyroelectric properties of Al(In)GaN/GaN hetero and quantum well structures, J. Phys. Condens. Matter 14 (13) (2002) 3399–3434, https://doi.org/10.1088/0953-8984/14/13/302.

[24] T. Han, et al., 70-nm-gated InAlN/GaN HEMTs grown on SiC substrate with f_T/f_{max} > 160 GHz, J. Semicond. 37 (2) (2016) 4–8, https://doi.org/10.1088/1674-4926/37/2/024007.

[25] D. Jena, et al., Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys, Appl. Phys. Lett. 81 (23) (2002) 4395–4397, https://doi.org/10.1063/1.1526161.

[26] J. Guo, et al., MBE-regrown ohmic in InAlN HEMTs with a regrowth interface resistance of 0.05 Ωmm, IEEE Electron Device Lett. 33 (4) (2012) 525–527, https://doi.org/10.1109/LED.2012.2186116.

[27] X. Sun, O.I. Saadat, K.S. Chang-Liao, T. Palacios, S. Cui, T.P. Ma, Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method, Appl. Phys. Lett. 102 (2013), 103504, https://doi.org/10.1063/1.4795717.

[28] M. Micovic, et al., GaN DHFETs Having 48% Power Added Efficiency and 57% Drain Efficiency at V-Band, IEEE Electron Device Lett. 38 (12) (2017) 1708–1711, https://doi.org/10.1109/LED.2017.2763940.

[29] B. Kumar, R. Chaujar, Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET, SILICON 13 (2021) 1–9, https://doi.org/10.1007/s12633-020-00910-7.

[30] Y. Pathak, B.D. Malhotra, R. Chaujar, Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer, SILICON (2022), https://doi.org/10.1007/s12633-022-01822.

[31] M. Sharma, R. Chaujar, Design and Investigation of Recessed-T-Gate Double Channel HEMT with InGaN Back Barrier for Enhanced Performance, Arab. J. Sci. Eng. 47 (2022) 1109–1116, https://doi.org/10.1007/s13369-021-06157-7.

[32] P. Malik, R.S. Gupta, R. Chaujar, M. Gupta, AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications, Microelectron. Reliab. 52 (1) (2012) 151–158, https://doi.org/10.1016/j.microrel.2011.07.070.

[33] P. Murugapandiyan, et al., Performance analysis of HfO_2/InAlN/AlN/GaN HEMT with AlN buffer layer for high power microwave applications, J. Sci. Adv. Mater. Devices 5 (2) (2020) 192–198, https://doi.org/10.1016/j.jsamd.2020.04.007.

[34] T.R. Lenka, G.N. Dash, A.K. Panda, RF and microwave characteristics of a 10 nm thick InGaN-channel gate recessed HEMT, J. Semicond. 34 (11) (2013) 1–6, https://doi.org/10.1088/1674-4926/34/11/114003.

[35] M. Sharma, R. Chaujar, "Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications," Int, J. RF Microw. Comput. Aided Eng. 32 (4) (2022) 23057, https://doi.org/10.1002/mmce.23057.

[36] T. Zine-eddine, H. Zahra, M. Zitouni, Design and analysis of 10 nm T-gate enhancement-mode MOS-HEMT for high power microwave applications, J. Sci. Adv. Mater. Devices 4 (1) (2019) 180–187, https://doi.org/10.1016/j.jsamd.2019.01.001.

[37] A. Kumar, R. Chaujar, Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications, Superlattice. Microst. 91 (1) (2016) 290–301, https://doi.org/10.1016/j.spmi.2016.01.027.

Micro and Nanostructures 180 (2023) 207593

Contents lists available at ScienceDirect

Micro and Nanostructures

journal homepage: www.journals.elsevier.com/micro-and-nanostructures

Small signal and noise analysis of T-gate HEMT with polarization doped buffer for LNAs

Megha Sharma, Bhavya Kumar, Rishu Chaujar *

Department of Applied Physics, Delhi Technological University, Delhi, India

ARTICLE INFO

Keywords:
Heterostructure
Polarization
Noise
Small signal
T-shaped gate

ABSTRACT

Small signal behavior and RF noise performance of T-gate InAlN/GaN HEMT with polarization doped buffer (PDB-HEMT) have been examined in this paper and compared to conventional HEMTs at GHz frequency range. Enhancement mode operation is possible in the PDB-HEMT device, which has a recessed T-gate structure with a gate length of 10 nm and delivers the threshold voltage (V_{th}) of 0.9 V and a high transconductance of 1.55 S/mm. This study examines the auto/cross-correlation factor, minimum noise figure, reflection/transmission coefficients, noise conductance, and optimal noise resistance and reactance. The enhanced transconductance of PDB-HEMT has resulted in a considerable increase in the forward transmission coefficient and a decrease in the input/output reflection coefficient compared to traditional HEMTs. It has also been shown that the PDB- HEMT has a lower noise figure and noise conductance than the GaN buffer HEMT by 57% and 20%, respectively. This research demonstrates that the T-gate polarization doped buffer (PDB-HEMT) structure is an excellent choice for Low Noise Amplifiers (LNA) operating at higher frequencies.

1. Introduction

In every wireless communication system, Low Noise Amplifiers (LNAs) are the building blocks. LNA is used to enhance extremely weak signals that are picked up by an antenna. Regarding LNA design, there are four key considerations: gain, noise figure, non-linearity, and impedance matching. One of the most critical aspects of a low-noise amplifier's performance is its noise figure [1]. Thus, we can determine which LNA best suits a certain application. When a Low Noise Amplifier (LNA) does not have a high gain, noise in the LNA circuit might impact the signal and even attenuate it. Gain and noise figures are balanced via input-matching circuits. Through the use of scattering parameter analysis, the circuit's gain, noise figure, and stability circle were all calculated. The initial stage of the amplifier must have a high amplification level to reduce the amount of noise.

GaN-based HEMTs are a particularly ideal choice for such applications because of unique material properties like greater bandgap energy, higher electron saturation velocity, higher electron density, and higher breakdown voltage [2,3] when compared to existing materials such as gallium arsenide (GaAs). In addition, the polarization property of GaN material led to the formation of a 2DEG at the AlGaN/GaN junction [4]. Because of this improvement in electron mobility, the GaN device became a fantastic option for use in high-power settings applications. The superior microwave properties of the AlGaN/GaN HEMT [5–12], together with its low noise and high power microwave performance, as well as its high current drive capabilities, drew attention to its use in low noise applications. In

* Corresponding author.
E-mail addresses: meghasharma_phd2k18@dtu.ac.in (M. Sharma), bhavyakumar_phd2k18@dtu.ac.in (B. Kumar), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.micrna.2023.207593
Received 13 November 2022; Received in revised form 7 April 2023; Accepted 26 April 2023
Available online 29 April 2023

the context of wideband robust receiver applications, various AlGaN/GaN HEMT-based LNAs were created [13–15]. GaN HEMTs have made significant progress in their development for usage in LNAs, with results showing NF_{min} values of 1.6 dB at 30 GHz [16] and 1.2 dB at 20 GHz [17] when using a gate length of 100 nm. Shinohara et al. reported a good NF_{min} of around 0.5 dB at 30 GHz, which exhibited the cut-off frequency (f_T) of 400 GHz and maximum oscillation frequency (f_{max}) of 500 GHz using 20-nm T-gate AlGaN/GaN HEMTs [18]. Although AlGaN/GaN HEMTs have seen a large rise in operating frequency, they still suffer from strain issues [19]. When the thickness of the AlGaN barrier is decreased, there is an inevitable strain produced at the junction of AlGaN and GaN. This problem is effectively minimized by using a lattice-matched InAlN layer [20]. The HEMTs that are based on InAlN and AlN make it possible for the device to scale aggressively, which increases the f_T and decreases the short-channel impact (SCE) [21]. Though the InAlN/AlN T-Gate HEMTs claimed to have numerous benefits, they also had one significant drawback: 2DEG spilling from the channel into a buffer, which lowers the device's mobility and reliability [22]. Therefore, the performance of InAlN HEMTs has to be made more resilient by implementing creative buffer engineering. Polarization doping, which may be achieved by grading the AlGaN layer, has recently gained popularity and is seen as a superior option [23]. This has already been shown in our prior study that implementation of polarization doping in the buffer region of InAlN/AlN T-gate HEMT significantly enhances the f_T and f_{max} of the device [24].

The small-signal behavior and noise FOMs of InAlN/AlN T-gate HEMT with polarized doped buffer are investigated in this study by employing the ATLAS SILVACO simulator. The following subheadings constitute the various sections of this article: Section 2 analyses the simulation models and device construction; Section 3 and 4 addresses the feasibility of fabrication of the device and the performance of the device in terms of small signals and noise; and Section 5 provides a conclusion to the article.

2. Device design and simulation models

Fig. 1(a and b) depicted the conventional GaN-HEMT and proposed PDB-HEMT's schematic structure. The dimensions of both devices are the same. The proposed device consists of a 1 μm AlGaN buffer layer with a linear reduction in aluminum concentration from 0.2 to 0 in the (0001) direction, a 20 nm GaN channel layer, a 1 nm AlN spacer layer, and 6 nm lattice-matched InAlN barrier layer. The smaller foot length and bigger gate area of the T-shaped construction (gate length = 10 nm, gate width = 50 μm) reduce gate resistance and capacitance. Reduction in contact resistance is achieved by doping source and drain regions with Silicon. The spacing between the source-drain region is 1 μm. To minimize parasitic capacitance and improve the device's RF characteristics, the circuit is passivated by the 20 nm SiN layer. Silvaco TCAD software was used to simulate the device [25]. The high and low field mobility model, polarization, and SRH recombination models have been used in the simulation procedure [25].

3. Experimental calibration and fabrication feasibility

Fig. 2 shows how the physical models match the experimental results [26]. The acceptor and donor-like traps with energy levels 0.5eV, 0.42eV, and trap density $5 \times 1016\ cm^{-3}$, $3.86 \times 10^{13}\ cm^{-3}$ are considered below the conduction band to fit the experimental 2DEG density. The agreement between the simulated and experimental outcomes is remarkable. Fig. 3 depicts the proposed structure's fabrication process. Two fabrication methods exist for the proposed structure.: top-down and bottom-up. The epitaxial stack is fabricated via molecular beam epitaxy (MBE) [27]. The InAlN/AlN/GaN/AlGaN epitaxial stack is grown utilizing the bottom-up technique on the SiC substrate. To create the n++ GaN ohmic source/drain regions, MBE is utilized with a SiO_2 growth mask [28]. By using plasma-enhanced chemical vapor deposition (PECVD), the passivation layer is deposited on top of the epitaxial stack. Following are the stages involved in making the T-gate. To define the gate, electron beam lithography (EBL) is employed and partly recessed the gate foot into the barrier layer by dry etching [29].

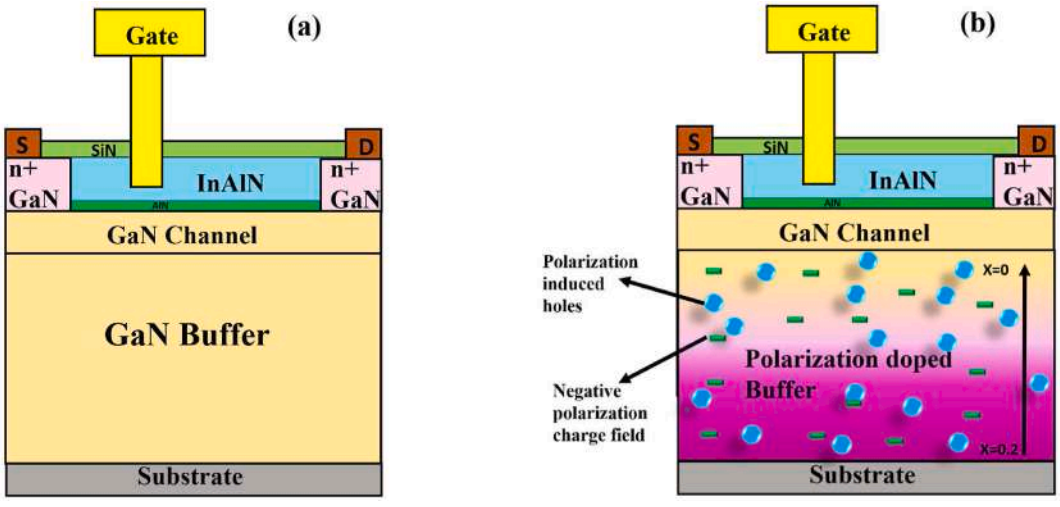

Fig. 1(a). GaN-HEMT (b) PDB-HEMT

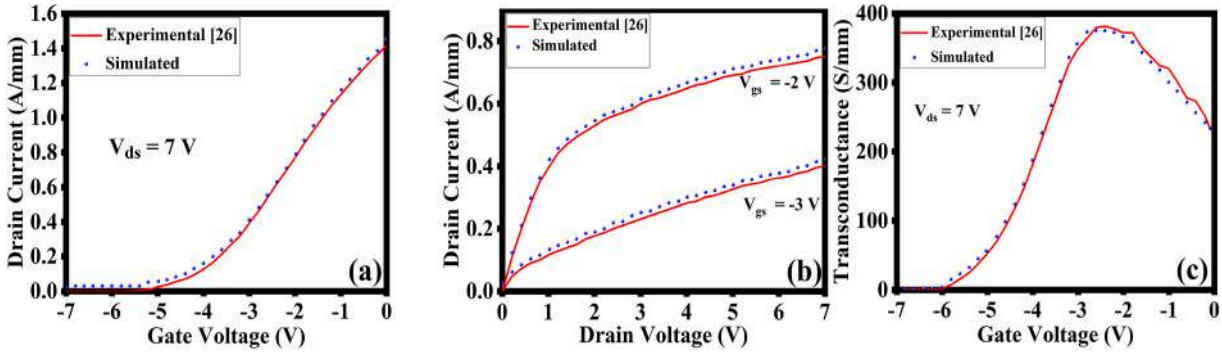

Fig. 2. Comparison of simulated and experimental data.

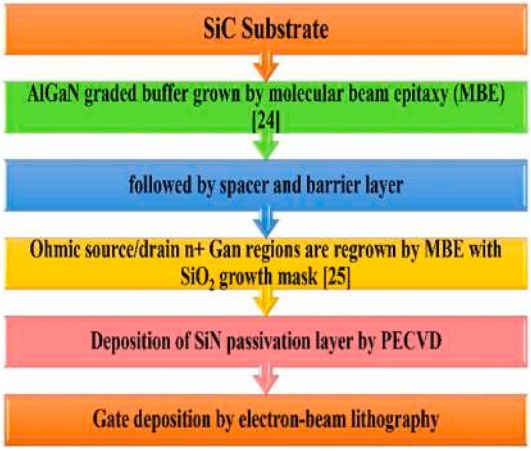

Fig. 3. PDB-HEMT calibration process.

4. Results and discussion

Fig. 4 depicts the transfer characteristics of the proposed polarized doped buffer HEMT (PDB-HEMT) and conventional GaN-HEMT. In comparison to the conventional ones, the PDB-HEMT exhibits a lower drain current (2.56 A/mm) and a greater transconductance peak (1.55 S/mm) at $V_{gs} = 1.4$ V. The suggested structure exhibits a dramatic increase in transconductance at the pinch-off area, which shows the lower subthreshold current in the device.

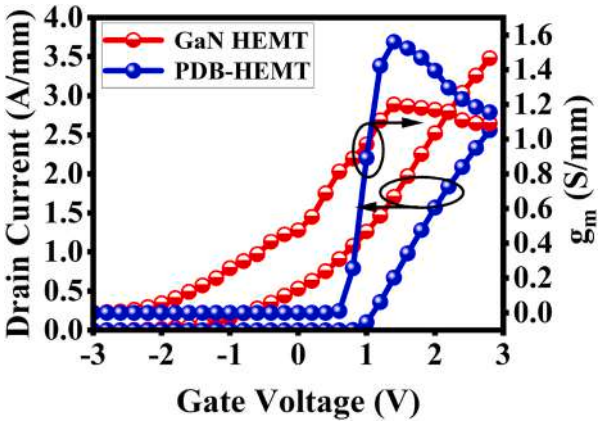

Fig. 4. Transfer characteristics for both the structure.

4.1. Small signal analysis

The scattering (reflection and transmission coefficients) properties of PDB-HEMT at $V_{gs} = 1.4V$ and GaN-HEMT at $V_{gs} = 1.8V$ are examined at fixed drain bias voltage of 3V. We have chosen these gate voltages because the transconductance peak is observed for PDB-HEMT at $V_{gs} = 1.4$ V and for GaN buffer at $V_{gs} = 1.8$ V as shown in Fig. 4.

One of the greatest ways to look into the high-frequency small-signal behavior of HEMTs is via measurements of their S-parameter. Networks that operate at microwave frequencies often use S-parameters because it is simpler to compute signal power and energy at radio and microwave frequencies than currents and voltages. The input/output reflection coefficient is defined as [30].

$S11 = \frac{\text{reflection wave at port 1}}{\textit{Incident wave at port 1}}$, where port 2 terminated on the characteristic impedance

$S22 = \frac{\text{reflection wave at port 2}}{\textit{Incident wave at port 2}}$, where port 1 terminated on the characteristic impedance

These parameters evaluate the matching between the terminating impedance and the port. For RF circuit design, matching is required, and a perfectly matching condition occurs when the reflection coefficient reduces to zero [31]. Hence, a lower value of S11 and S22 is required for better RF performance. In Fig. 5(a and b), the lower value of S11 and S22 is obtained for the PDB-HEMT. The reduction of the S11 parameter in PDB-HEMT is due to the reduction of source resistance and gate resistance in PDB-HEMT, which is 27.7% and 67.6% lower than the Gan-HEMT as shown in Fig. 6(a and b). The lower value of gate and source resistance increases the coupling between the input and output port and decreases the S11 parameter. The higher value of drain resistance, transconductance, and lower channel resistance reduce the S22 parameter. However, in PDB-HEMT lower drain resistance is observed which is 13% lower than the Gan-HEMT as exhibited in Fig. 6(c), and higher channel resistance is observed which is 7% higher than the GaN-HEMT as shown in Fig. 7(b), which lead to increase the S22 parameter, but the higher transconductance is observed in Fig. 6(d) which is 30% higher than the GaN-HEMT and reduced the S22 parameter.

The amount of feedback an amplifier receives from its output to its input is measured by the reverse isolation parameter S12, which affects the amplifier's supremacy in terms of its stability at high frequency. The magnitude and phase change of the reverse and forward transmission coefficients (S12, S21) for both devices is exhibited in Fig. 5 (c, d). For better RF performance, the S21 parameters should be high and the S12 parameter should be as low as possible to reduce the feedback of the output signal to the input port. Fig. 5(c) shows the improvement in the S21 parameter for PDB-HEMT which is 69% higher than the GaN-HEMT. This enhancement is due to the polarization-doped buffer engineering in the proposed structure. The polarization-doped buffer engineering caused a negative polarization field in the buffer, which limited the electrons to a shallower depth range and enhanced gate

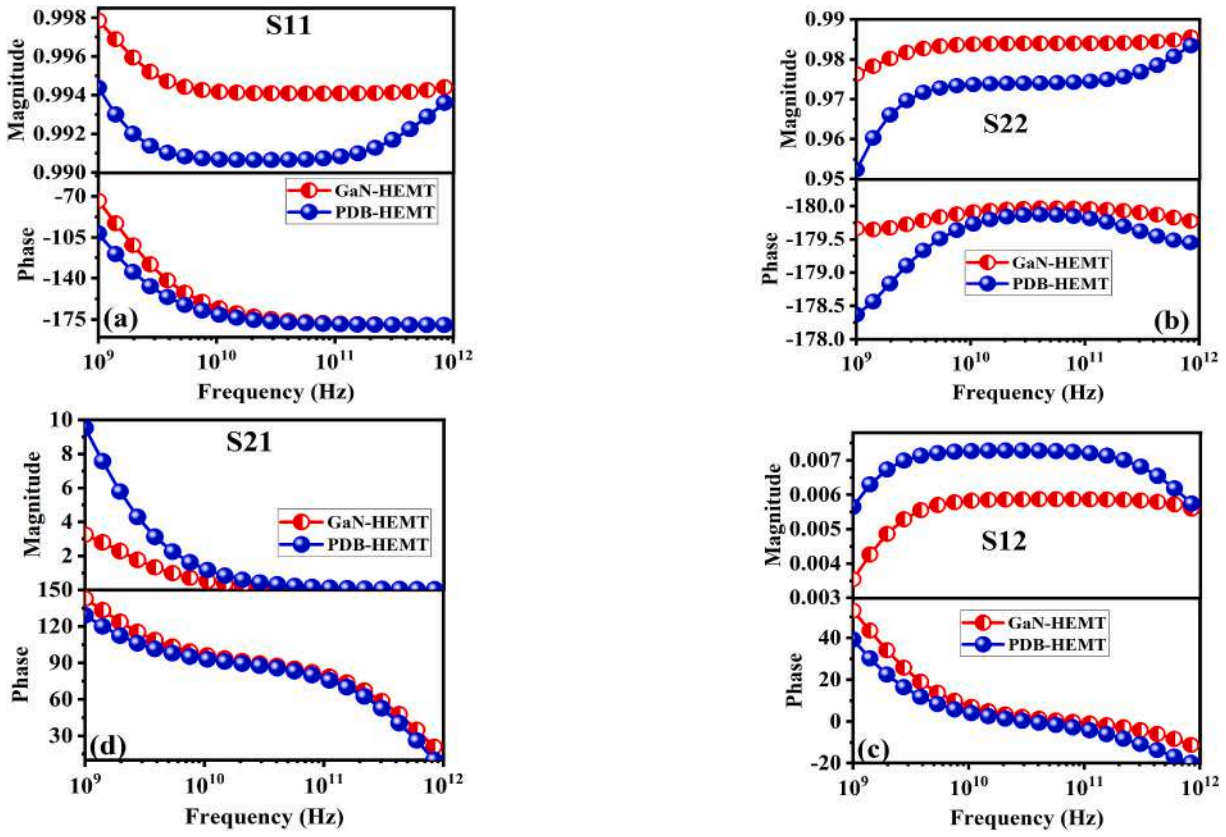

Fig. 5. Variation of magnitude and phase of (a) input (b) output reflection coefficient (c) forward (d) reverse transmission coefficient.

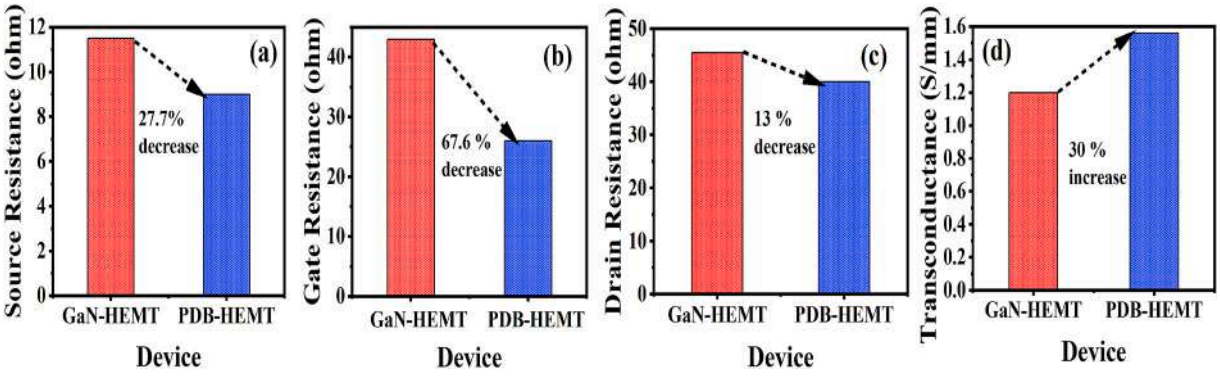

Fig. 6. Bar graph of (a) Source resistance (b) Gate resistance (c) drain resistance (d) Transconductance for both the devices.

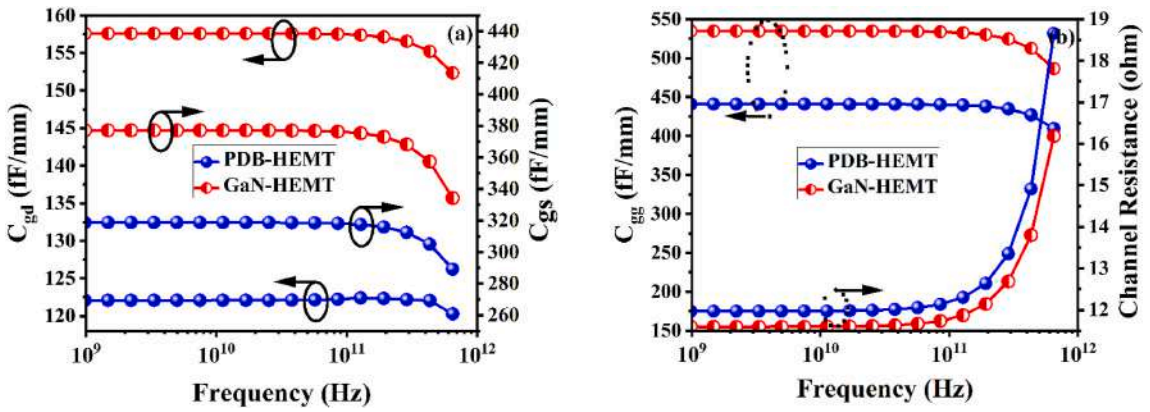

Fig. 7. Variation of (a) gate to drain and source capacitance (b) gate capacitance and channel resistance for both the structures.

controllability. Because of this, the transconductance increases, which ultimately leads to an improvement in the S21 parameter. However small increment in the S12 parameter is also observed for PDB-HEMT which is 8% higher than the GaN-HEMT.

Fig. 7(a and b) exhibits the graph of parasitic capacitance i.e., gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), gate capacitance, and gate capacitance (C_{gg}) for both devices. The lower value of parasitic capacitances is observed for PDB-HEMT which enhances cut off frequency (f_T) and maximum oscillation frequency (f_{max}) of the device. Fig. 7(b) exhibits the graph of channel resistance for both devices. It has been observed that in PDB-HEMT channel resistance increases by 7% as compared to GaN-HEMT. This enhancement of channel resistance is due to the lower 2DEG density in PDB-HEMT. However, enhancement in channel resistance adversely affects the f_{max} of the device but a higher value of transconductance and lower parasitic capacitance overcome this effect.

When the device's current and unilateral power gain are both unity, the device's f_T and F_{max} are calculated. The PDB -HEMT's f_T (583 GHz) and f_{max} (840 GHz) are displayed in Fig. 8(a and b), and they are 40% and 75% more efficient than the conventional device.

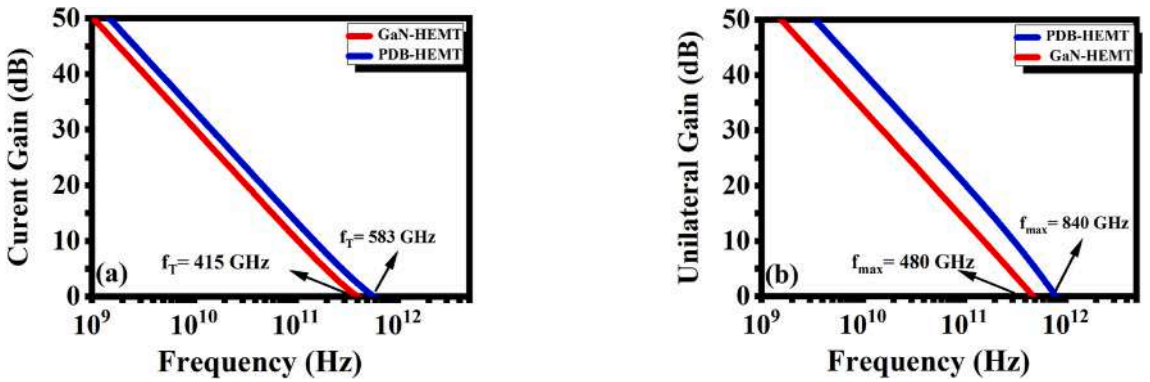

Fig. 8. Variation of (a) current gain (b) unilateral power gain for both the structures.

4.2. Noise analysis

The two-port noisy network is often required to investigate internal sources of noise [32], as seen in Fig. 9. It is possible to replace a linearly noisy two-port network with a noise-free network having a noise current and voltage source. There is a correlation between these two noise sources in real devices [33]. The noise parameters of the general circuit are obtained from the measurement conducted on two-port networks. The noise performance of the PDB-HEMT is examined with the help of the two port circuits by using the following parameters: NF_{min} (the least noise figure), the noise conductance (G_n), optimum source impedance (Z_{opt}), and the auto/cross-correlation function. The optimum source impedance (Z_{opt}) is the impedance that gives the minimum noise figure [34]. Z_{opt} is a complex number that has both real and imaginary values, as expressed in Eqn. (1).

$$Z_{opt} = R_{opt} + jX_{opt} \tag{1}$$

The real value of Z_{opt} is optimum source resistance (R_{opt}), and the imaginary part of Z_{opt} is optimum reactance (X_{opt}) as expressed by Eqn. (2) and (3) [35]. Where P and R are the noise coefficient and Cr is the correlation factor [36].

$$R_{opt} = \frac{1}{\omega C_{gs}} \sqrt{\frac{g_m\left(R_{gs} + R_s\right) + R\left(1 - C_r^2\right)}{P}} + \sqrt{\omega^2 C_{GS}^2 \left(R_{gs} + R_s\right)^2} \tag{2}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} \left(1 - C_r \sqrt{\frac{R}{P}}\right) \tag{3}$$

Fig. 10(a) depicts the variation of R_{opt} and X_{opt} with frequency for both devices. The optimum source resistance and reactance value drop with increasing frequency and become saturated at a higher frequency. The impact of gate voltage on optimum source resistance (R_{opt}) and optimum reactance (X_{opt}) is depicted in Fig. 10(b and c). The optimum source resistance increases with gate voltage due to the enhancement of carrier concentration at the channel region. Moreover, R_{opt} is constant at the MHz frequency region and decreases at a greater frequency region, as depicted in Fig. 10(b). The inset graph of Fig. 10(b) exhibited the optimum source resistance at a higher frequency region. The optimum reactance versus frequency for.

different gate voltages are exhibited in Fig. 10(c). At the lower

frequency range, the optimum reactance increases with the frequency due to the recombination of charge carriers [37], and a higher peak of X_{opt} is observed for $V_{gs} = 1.4$V; after that, there is a downward swing in X_{opt}. The inset graph of Fig. 10(c) shows the value of X_{opt} at a higher frequency range.

One of the essential metrics used to evaluate the performance of a low-noise amplifier (LNA) is noise conductance (G_n), expressed by Eqn. (4). Where S_I is the drain current noise spectral density, and T_a is the reference temperature 290K.

$$G_n = \frac{S_I}{4K_B T_a |Y_{21}|^2} \tag{4}$$

The power spectral densities of noise current generators are often estimated using noise conductance. RF and low-noise amplifiers (LNAs) need low-noise conductance [38]. The fluctuation of noise conductance with frequency for both devices is shown in Fig. 11(a). At 583 GHz frequency, the PDB-HEMT exhibits a lower noise conductance, which is 20% lower than the GaN-HEMT. Fig. 11(b) shows how the gate voltage affects the noise conductance. The flat G_n response is observed at the lower frequency region and linearly increases at a higher frequency. The lower noise conductance is observed at $V_{gs} = 1.4$ V.

The mathematical expression of the noise figure for a two-port network is depicted by Eqn. (5) [39].

$$NF = NF_{min} + \frac{R_n}{G_s}\left(G_s - G_{opt}\right)^2 + \frac{R_n}{G_s}\left(B_s - B_{opt}\right)^2 \tag{5}$$

The optimal source susceptance and conductance are expressed by G_{opt} and B_{opt} [40]. The minimum noise figure (NF_{min}) is

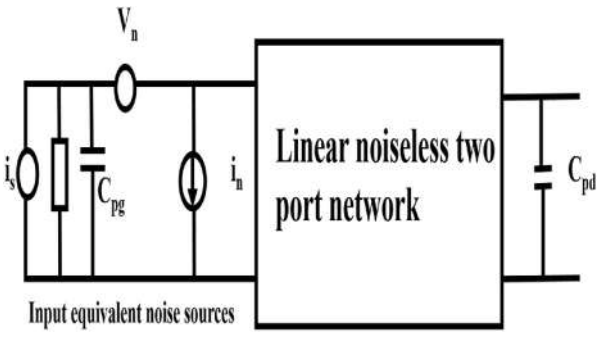

Fig. 9. The equivalent noise circuit.

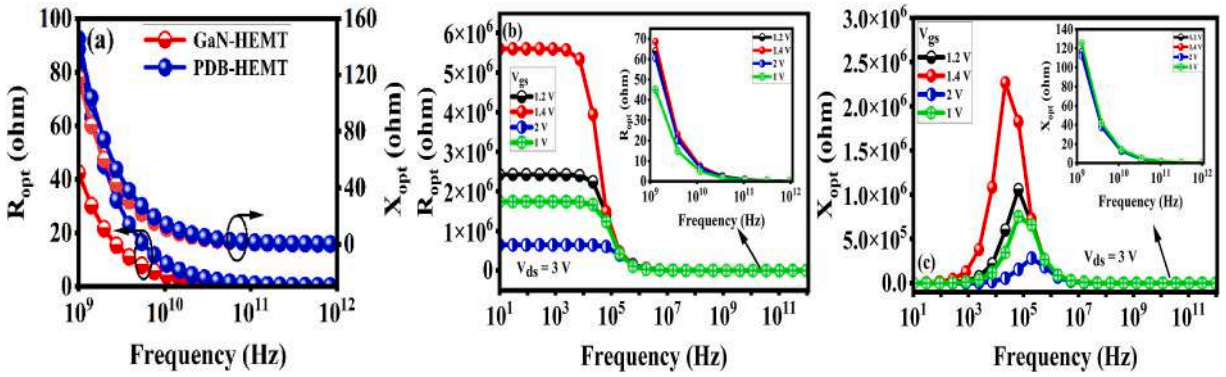

Fig. 10. (a) optimum source resistance and reactance for PDB-HEMT and GaN-HEMT (b) optimum noise resistance (c) reactance for different V_{gs}.

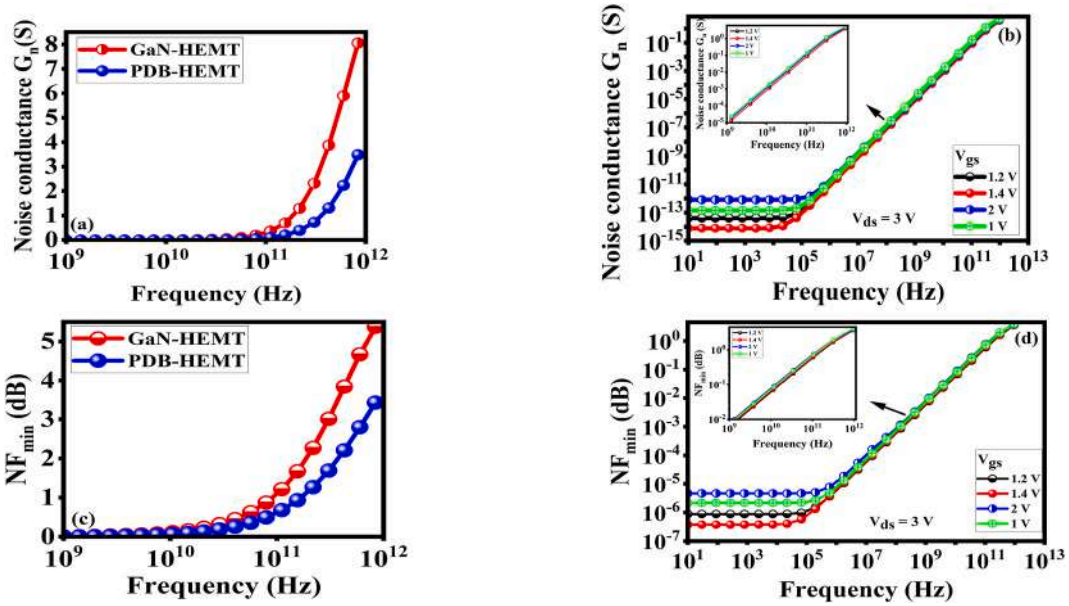

Fig. 11. Noise conductance (a) PDB-HEMT and GaN-HEMT (b) variable gate voltage; NF_{min} (c) PDB-HEMT and GaN-HEMT (d) variable gate voltage.

obtained when $G_s = G_{opt}$ and $B_s = B_{opt}$. The frequency-dependent fluctuation of NF_{min} for both devices is shown in Fig. 11(c). The reduction in NF_{min} is noticed for PDB-HEMT compared to the conventional HEMT. The NF_{min} is inversely proportional to the transconductance. In PDB-HEMT, the graded buffer engineering caused a negative polarization field in the buffer, which limited the electrons to a shallower depth range and enhanced gate controllability. Because of this, the transconductance increases, leading to an improvement in the low noise figure compared to the conventional HEMT. The impact of gate voltage on the noise figure is exhibited in Fig. 11(d). It has been observed that at the MHz frequency range, NF_{min} is constant; at the GHz region, NF_{min} linearly increases with frequency. The NF_{min} value decreases with an increase in the gate voltage from 1 V to 1.4 V; the afterward higher value of NF_{min} is observed for $V_{gs} = 2V$. This variation in NF_{min} is basically due to the transconductance variation with gate voltage, as exhibited in Fig. 4. The NF_{min} is the inverse of the transconductance. It is observed from Fig. 4 that transconductance increases with an increment in gate voltage from 1 V to 1.4 V, and a higher peak of transconductance is observed at $V_{gs} = 1.4V$ afterward downward swing is observed.

Fig. 12 depicts the HEMT as a two-port device, with V1 representing noise generated at the gate and V2 representing noise received at the output [41]. A little statistical analysis is required for this study since noise is a random event. These two ports are examined in terms of autocorrelation and cross-correlation of their voltages. Fig. 13(a and b) shows the cross-correlation (V1. V2) and autocorrelation between the input (V1. V1) and output voltages (V2. V2) for both structures. In contrast to the GaN-HEMT, the PDB-HEMT has a stronger auto/cross-correlation. The polarization-doped buffer in PDB-HEMT significantly bends the conduction band of the buffer layer upwardly convex. This enhances the carrier confinement in the channel and prevents the channel electrons from interacting with the traps in the buffer layer to reduce the trapping effects, which attribute to the enhancement of electron mobility and reduces the scattering. Therefore, the scattering mechanism in PDB-HEMT is inefficient in disrupting the correlation among the gate and drain

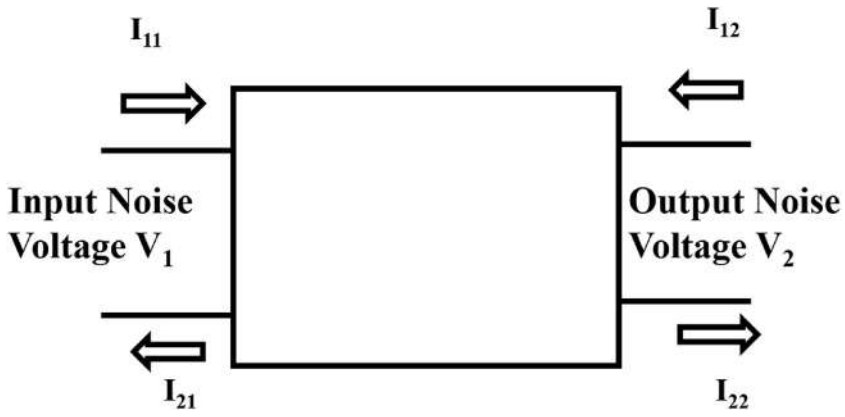

Fig. 12. Two-port device.

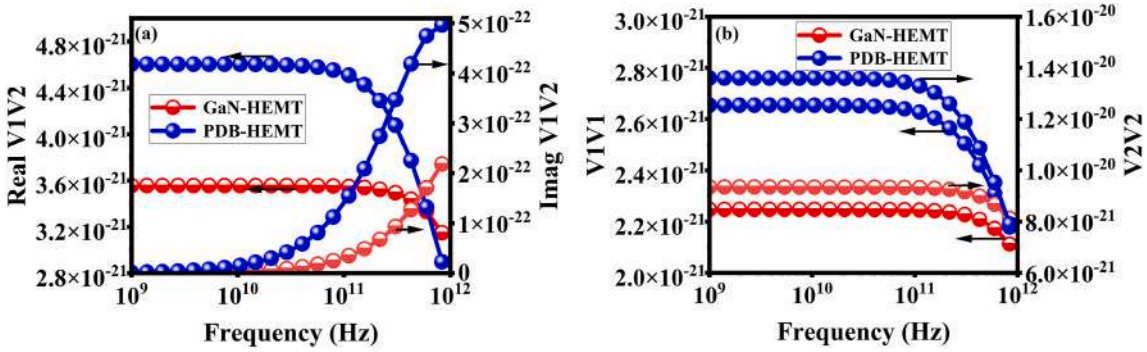

Fig. 13. (a) Cross-correlation (b) autocorrelation for both the structures.

current, significantly enhancing the auto/cross-correlation between them.

The real and imaginary part of the cross-correlation of PDB-HEMT for $V_{gs} = 1V$, 1.2V, 1.4V, and 2V is exhibited in Fig. 14(a and b). The real part of cross correlation remains constant in the frequency range 1 GHz–100 GHz after that linear reduction is observed in the THz frequency region shown in Fig. 14(b). Furthermore, the cross-correlation function decreases with increasing gate voltage. Fig. 14 (c) depicts the fluctuation of the auto-correlation function concerning the variation of the gate voltage (V_{gs}). The autocorrelation function falls linearly with lower order frequency (MHz) and stays constant with higher order frequency (GHz). The autocorrelation function reduces as the gate voltage (V_{gs}) of the PDB-HEMT increases. Hence, this work's results show that using the polarized doped buffer in T-gate InAlN/GaN HEMT devices may achieve extremely low noise levels via improved structural design.

5. Conclusion

This study presents a comprehensive investigation of the small-signal behavior and noise analysis of PDB-HEMT operating in the GHz frequency range. The simulated results suggest that the introduction of the polarization-doped engineering scheme into the buffer region results in a reduction in the reflection coefficient and an increment in the transmission coefficient in comparison with traditional GaN buffer HEMT. Even at high frequency, the PDB-HEMT device has a minimum noise figure of $NF_{min} = 1.62$ dB, lower noise conductance, and stronger auto/cross-correlation. These outstanding results show that PDB-HEMT is suitable for creating microwave amplifiers and oscillators. These findings make it abundantly evident that the T-gate PDB HEMT structure is an excellent candidate for high-performance RF applications and LNAs.

Authors statement

Megha Sharma: Conceptualization, Methodology, Software, Data Curation, Writing-Original draft preparation. **Bhavya Kumar**: Conceptualization, Methodology, Software, Data Curation, Writing-Original draft preparation. **Rishu Chaujar**: Supervision, Reviewing, and Editing.

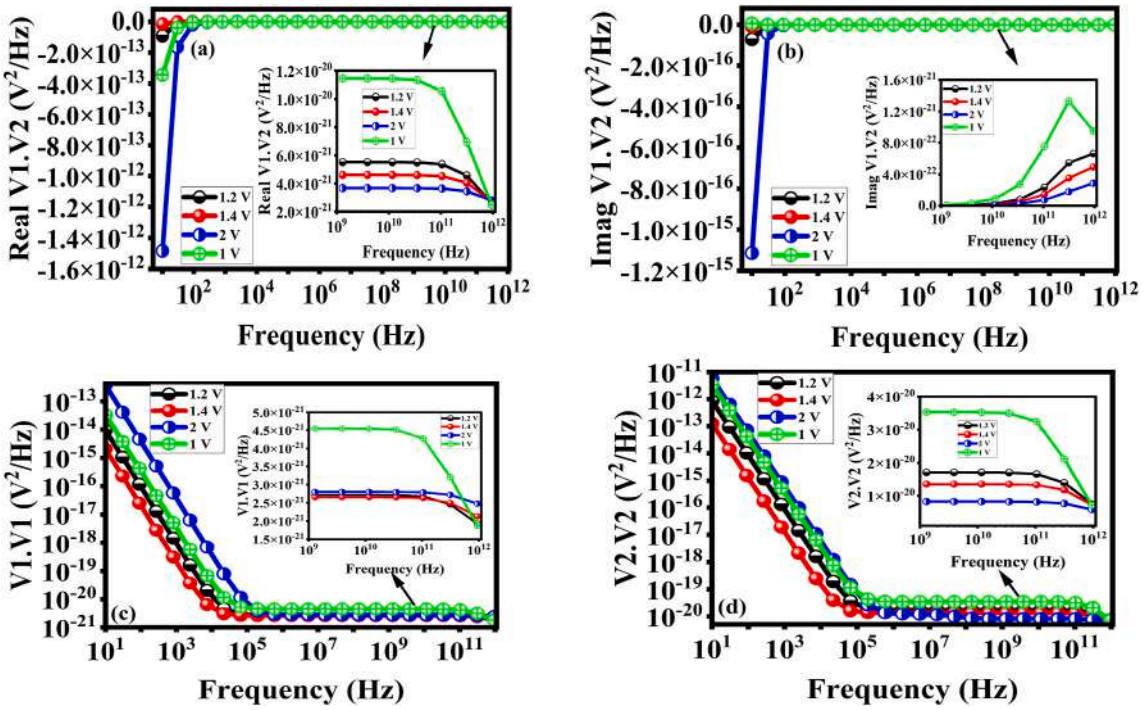

Fig. 14. For different gate voltage (a) real part of cross-correlation (b) imag part of cross-correlation (c) input (d) output autocorrelation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

References

[1] A. Mohanbabu, R. Saravana Kumar, N. Mohankumar, Noise characterization of enhancement-mode AlGaN graded barrier MIS-HEMT devices, Superlattice. Microst. 112 (2017) 604–618, https://doi.org/10.1016/j.spmi.2017.10.020.
[2] Y. Zhang, K. H Teo, T. Palacios, Beyond thermal management: incorporating p-diamond Back-barriers and cap layers into AlGaN/GaN HEMTs, IEEE Trans. Electron. Dev. 6 (2016) 2340–2345, https://doi.org/10.1109/TED.2016.2553136.
[3] S. Prasad, A.K. Dwivedi, A. Islam, Characterization of AlGaN/GaN and AlGaN/AlN/GaN HEMTs in terms of mobility and subthreshold slope, J. Comput. Electron. 15 (2016) 172–180, https://doi.org/10.1007/s10825-015-0751-8.
[4] H. Xiao-Guang, Z. De-Gang, J. De-Sheng, Formation of a two-dimensional electron gas at AlGaN/GaN heterostructure and the derivation of its sheet density expression, Chin. Phys. B 24 (2015), 067301, https://doi.org/10.1088/1674-1056/24/6/067301.
[5] K. Liu, R. Wang, C. Wang, X. Zheng, X. Ma, J. Bai, B. Cheng, R. Liu, A. Li, Y. Zhao, Y. Hao, The influence of lightly doped p-GaN cap layer on p-GaN/AlGaN/GaN HEMT, Semicond. Sci. Technol. 37 (2022) 268–1242.
[6] S.P. Kumar, A. Agrawal, R. Chaujar, M. Gupta, R.S. Gupta, Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGaN/GaN HEMT, Superlattice. Microst. 44 (2008) 37–53, https://doi.org/10.1016/j.spmi.2008.01.023.
[7] S.P. Kumar, A. Agrawal, R. Chaujar, M. Gupta, R.S. Gupta, Device linearity and intermodulation distortion comparison of dual material gate and conventional AlGaN/GaN high electron mobility transistor, Microelectron. Reliab. 51 (2011) 587–596, https://doi.org/10.1016/j.microrel.2010.09.033.
[8] D. Chen, P. Yuan, S. Zhao, S. Liu, Q. Xin, X. Song, S. Yan, Y. Zhang, H. Xi, W. Zhu, W. Zhang, Wide-range-adjusted threshold voltages for E-mode AlGaN/GaN HEMT with a p-SnO cap gate, Sci. China Mater. 65 (2022) 795–802.
[9] S. Chatterjee, M. Mukherjee, Band-engineered quasi-AlGaN/GaN high-electron-mobility-avalanche-transit-time (HEMATT) oscillator: electro-optical interaction study in the sub-mm frequency domain, Eur. Phys. J. Plus 137 (2022) 1–5.
[10] S. Qu, X. Wang, H. Xiao, C. Wang, L. Jiang, Analysis of transconductance characteristic of AlGaN/GaN HEMTs with graded AlGaN layer, Eur. Phys. J. Appl. Phys. 66 (2014), 20101, https://doi.org/10.1051/epjap/2014130368.
[11] J. Liu, Y. Zhou, J. Zhu, Y. Cai, K.M. Lau, K.J. Chen, DC and RF characteristics of AlGaN/GaN/inGaN/GaN double-heterojunction HEMTs, IEEE Trans. Electron. Dev. 54 (1) (Jan. 2007) 2–10, https://doi.org/10.1109/TED.2006.887045.
[12] O. Fathallah, M. Gassoumi, B. Grimbert, C. Gaquière, H. Maaref, Parasitic effects and traps in AlGaN/GaN HEMT on sapphire substrate, Eur. Phys. J. Appl. Phys. 51 (1) (2010), 10304.
[13] O. Fathallah, M. Gassoumi, B. Grimbert, C. Gaquière, H. Maaref, Wideband AlGaN/GaN HEMT MMIC low noise amplifier, IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535) 1 (2004) 153–156, https://doi.org/10.1109/MWSYM.2004.1335828.
[14] K.W. Kobayashi, An 8-W 250-MHz to 3-GHz decade-bandwidth low-noise GaN MMIC feedback amplifier with > +51-dBm OIP3, IEEE J. Solid State Circ. 47 (10) (2012) 2316–2326, Oct, https://doi.org/10.1109/JSSC.2012.2204929.

[15] J.-S. Moon, J. Kang, D. Brown, R. Grabar, D. Wong, H. Fung, P. Chan, D. Le, C. McGuire, "Wideband Linear Distributed GaN HEMT MMIC Power Amplifier with a Record OIP3/Pdc", IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR), 2016, pp. 5–7, https://doi.org/10.1109/PAWR.2016.7440127.
[16] H. Sun, A.R. Alt, H. Benedickter, C.R. Bolognesi, High-performance 0.1- μm gate AlGaN/GaN HEMTs on silicon with low-noise figure at 20 GHz, IEEE Electron. Device Lett. 30 (2) (Feb. 2009) 107–109, https://doi.org/10.1109/LED.2008.2010339.
[17] C.-T. Chang, H.-T. Hsu, E.Y. Chang, C.-I. Kuo, J.-C. Huang, C.-Y. Lu, Y. Miyamoto, 30-GHz low-noise performance of 100-nm-Gate-Recessed n-GaN/AlGaN/GaN HEMTs, IEEE Electron. Device Lett. 31 (2) (Feb. 2010) 105–107, https://doi.org/10.1109/LED.2009.2037167.
[18] K. Shinohara, D.C. Regan, Y. Tang, A.L. Corrion, D.F. Brown, J.C. Wong, J.F. Robinson, H.H. Fung, A. Schmitz, T.C. Oh, S.J. Kim, P.S. Chen, R.G. Nagele, A. D. Margomenos, M. Micovic, Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications, IEEE Trans. Electron. Dev. 60 (10) (2013) 2982–2996, Oct, https://doi.org/10.1109/TED.2013.2268160.
[19] M. Higashiwaki, T. Mimura, T. Matsui, Gallium Nitride Materials and Devices III, vol. 6894, International Society for Optics and Photonics, 2008, pp. 293–301.
[20] M. Neuburger, T. Zimmermann, E. Kohn, Unstrained InAlN/GaN HEMT structure, Int. J. High Speed Electron. Syst. 14 (3) (2004) 785–790, https://doi.org/10.1142/S0129156404002831.
[21] H. Sun, H. Benedickter, 205-GHz (Al,In)N/GaN HEMTs, IEEE Electron. Device Lett. 31 (9) (Sept. 2010) 957–959, https://doi.org/10.1109/LED.2010.2055826.
[22] M.A. Khan, J.N. Kuznia, J.M. Van Hove, N. Pan, J. Carter, Observation of a two-dimensional electron gas in low-pressure metalorganic chemical vapor deposited GaN-AlxGa1-xN heterojunctions, Appl. Phys. Lett. 60 (24) (1992) 3027–3029, https://doi.org/10.1063/1.106798.
[23] D. Jena, S. Heikman, D. Green, D. Buttari, R. Coffie, H. Xing, S. Keller, Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys, Appl. Phys. Lett. 81 (23) (2002) 4395–4397, https://doi.org/10.1063/1.1526161.
[24] M. Sharma, R. Chaujar, Ultrascaled 10 nm T-gate E-mode InAlN/AlN HEMT with polarized doped buffer for high power microwave applications, Int. J. RF Microw. Computer-Aided Eng. 32 (4) (2022), 23057, https://doi.org/10.1002/mmce.23057.
[25] ATLAS User's Manual, SILVACO International, CA, USA, 2016.
[26] T. Han, S. Dun, Y. Lü, G. Gu, X. Song, Y. Wang, P. Xu, Z. Feng, 70-nm-gated InAlN/GaN HEMTs grown on SiC substrate with fT/fmax > 160 GHz, J. Semiconduct. 37 (2) (2016) 4–8, https://doi.org/10.1088/1674-4926/37/2/024007.
[27] D. Jena, et al., Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys, Appl. Phys. Lett. 81 (23) (2002) 4395–4397, https://doi.org/10.1063/1.1526161.
[28] J. Guo, et al., MBE-regrown ohmic in InAlN HEMTs with a regrowth interface resistance of 0.05 Ωmm, IEEE Electron. Device Lett. 33 (4) (2012) 525–527, https://doi.org/10.1109/LED.2012.2186116.
[29] M. Micovic, et al., GaN DHFETs having 48% power added efficiency and 57% drain efficiency at V-band, IEEE Electron. Device Lett. 38 (12) (2017) 1708–1711, https://doi.org/10.1109/LED.2017.2763940.
[30] A. Kumar, M.M. Tripathi, R. Chaujar, In_2O_5Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications, AEU - Int. J. Electron. Commun. 93 (1434–8411) (2018) 233–241, https://doi.org/10.1016/j.aeue.2018.06.014.
[31] N. Gupta, R. Chaujar, Influence of gate metal engineering on small-signal and noise behavior of silicon nanowire MOSFET for low-noise amplifiers, Appl. Phys. A 122 (2016) 1–9, https://doi.org/10.1007/s00339-016-0239-9.
[32] A. van der Ziel, Representation of noise in linear two-ports, Proc. IEEE 57 (6) (June 1969) 1211, https://doi.org/10.1109/PROC.1969.7203, 1211.
[33] K. Hartmann, M.J.O. Strutt, Changes of the four noise parameters due to general changes of linear two-port circuits, IEEE Trans. Electron. Dev. 20 (1973), https://doi.org/10.1109/T-ED.1973.17761.
[34] A. K Gupta, A. Raman, N. Kumar, Design considerations and optimization of electrostatic doped ferroelectric nanotube tunnel FET: analog and noise analysis, Silicon (2022), https://doi.org/10.1007/s12633-022-01720-9.
[35] S. K Dubey, M. Mishra, A. Islam, Characterization of AlGaN/GaN based HEMT for low noise and high-frequency application, Int. J. Numer Model 35 (2022), https://doi.org/10.1002/jnm.2932.
[36] T. Takahashi, S. Hatsushiba, S. Fujikawa, H.I. Fujishiro, Comparative study on noise characteristics of as and Sb-based high electron mobility transistors, Phys. Status Solidi A 214 (2017), 1600599, https://doi.org/10.1002/pssa.201600599.
[37] A.M. Ivanov, G.V. Nenashev, A.N. Aleshin, Low-frequency noise and impedance spectroscopy of device structures based on perovskite-graphene oxide composite films, J. Mater. Sci. Mater. Electron. 33 (2022) 21666–21676, https://doi.org/10.1007/s10854-022-08955-7.
[38] R. Poornachandran, N. Mohankumar, R. Saravanakumar, et al., Analysis of microwave noise in an enhancement-mode dual-quantum-well InAs HEMT, J. Comput. Electron. 18 (2019) 1280–1290, https://doi.org/10.1007/s10825-019-01365-9.
[39] S. Lee, K. J Webb, V. Tilak, L. F Eastman, Intrinsic noise equivalent-circuit parameters for AlGaN/GaN HEMTs, IEEE Trans. Microw. Theor. Tech. 51 (2003) 1567–1577.
[40] Y. Zhu, C. Wei, O. Klimashov, B. Li, C. Zhang, Y. Tkachenko, Gate Width Dependence of Noise Parameters and Scalable Noise Model for HEMTs, European Microwave Integrated Circuit Conference, Amsterdam, 2008, pp. 298–301.
[41] A. Agarwala, R. Chaujar, "Investigation of Frequency-dependent Noise Performance Matrices for Gate Electrode Work Function Engineered Recessed Channel MOSFET,", Technical Proceedings of the 2012 NSTI Nanotechnology Conference and Expo, 2012.