ANALYSIS OF CMOS BASED APLICATION ON CIRCUIT SIMUALTOR

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CANDIDATE'S DECLARATION

I, Saksham Singh, Roll No. 2K21/VLS/24 student of M. Tech (VLSI and Embedded Systems), hereby declare that project Dissertation titled **"Analysis of CMOS based application on circuit simulator"** which is submitted by us to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the major Project Dissertation titled **"Analysis of CMOS based application on circuit simulator"** which is submitted by **Saksham Singh**, Roll No. **2K21/VLS/24** of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out bythe students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
Date: 31-05-2023

SUPERVISOR
Dr. Priyanka Jain
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ABSTRACT

In communication systems the data signal gets deteriorated while passing through the transmission medium to the receiver. It becomes difficult for the receiver to retrieve data from this signal since its too weak . This deterioration is often caused due to interference of noise present in the transmission medium . Therefore a low noise amplifier is used at the first stage of the receiver .This amplifier not only strengthens the data signal but also adds minimum noise possible. A good low noise amplifier should have low noise figure, high gain, high linearity, high stability , less sensitivity , and less area. All these attribute are not perfectly best in a practical LNA . Thus engineers design LNAs according to specifications and rely on trade of between different factor to achieve their goals. In this thesis we have worked on a existing LNA circuit and tried to improve its power consumption while keeping the noise figure same and trading off the gain. Also this LNA has been implemented on Cadence Virtuoso at 90nm technology . Use of Current mode to build ciruit has become a choice over voltage mode. This is because current mode can have many advantages like better bandwidth , better gain, better linearity, lower power consumption. In this thesis a have implement and verified a differential difference current conveyor transconductance amplifier (DDCCTA) using LTSPICE.

ACKNOWLEDGEMENT

A successful project can never be prepared by the efforts of the person to whom the project is assigned, but it also demands the help and guardianship of people who helped in completion of the project. We would like to thank all those people who have helped us in this research and inspired us during our study.

With profound sense of gratitude, we thank Prof. Priyanka Jain, our Research Supervisors, for his encouragement, support, patience and guidance in this project work. We heartily appreciate the guidance given by her in the project presentation that has improved our presentation skills with her comments and advices. We take immense delight in extending Our acknowledgement to our families and friends who have helped us throughout this projectwork.

Saksham Singh

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LIST OF ABBREVIATIONS

LNA	Low noise amplifier
CS	Common source
CG	Common gate
NF	Noise figure
TA	Transconductance amplifier
DDCCTA	Differential difference current conveyor transconductance amplifier

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Low Noise Amplifier

Electronic devices which amplifies low strength signals and not lowers signal-to-noise ratio are called low noise amplifier. A normal amplifier usual has noisy components which produce additional noise and this noise is also amplified along with the actual signal and hence distorts the whole output signal. Therefore we require a special kind of amplifier that adopts certain methodologies to eliminate or reduce this noise considerably. This can be done by using less noisy components or by adopting certain circuit topologies in the architecture or by impedance matching. The topology has to be such that the minimization of additional noise has minimum affect on other attributes of an amplifier.

LNAs are the most crucial part of a receiver as they play the biggest role in reducing the noise of overall receiver. There proper implementation and optimization can thereby be the deciding factor in the performance of receivers. Usually the noise figure of a decent LNA is around 3db and the gain produced is around 20 db.
Following attributes are the major deciding factor for the performance of a Low noise amplifier.

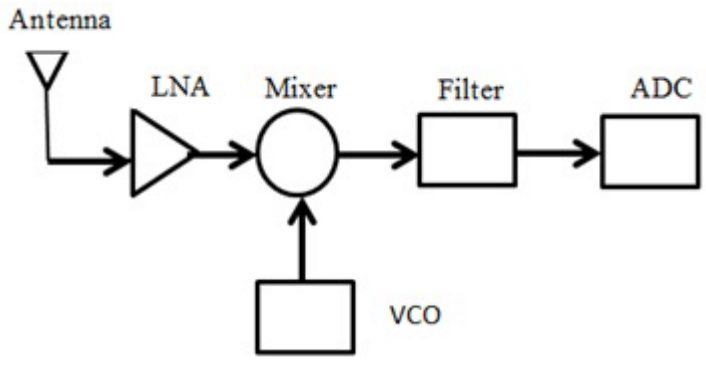

Fig1.1 LNA in Receiver block

1.1.1 Gain

It is a numerical figure which tells by how much the strength of an input signal is increased by an amplifier to produce the output signal. It is expressed in decibels(db). It is the most important attribute of an amplifier and decides the performance majorly. A detailed analysis of the performance can be done by analysing how gain varies with frequency response. Gain is limited by the external power supply i.e. in practical applications it will always have a finite value.

1.1.2 Noise Figure

Noise figure is a numerical figure which estimates the efficiency of an amplifier. This figure is use to identify how much noise has been added to the output by the amplifier. Gain and noise figure are independent of each other. It is the log of the ratio of signal to noise ratio at output to signal to noise ratio at input. Noise figure is also calculated in decibels. Noise figure is the most important factor in determining the performance of a low noise amplifier. Noise figure also varies with respect to frequency and thus its detailed analysis can be use to identify the bandwidth of a low noise amplifier.

1.1.3 Linearity

It is factor used to identify how proportionally is the output signal changing with respect to input signal in an amplifier. Linearity can be seen from the transfer function of an amplifier. If the graph is a straight line then the output is varying linearly with respect to input. This is an important factor as absence of linearity can lead to addition of new frequencies in the output signal which were absent in input signal. No harmonic distortion is seen in a linear amplifier.

1.1.4 Bandwidth

Bandwidth of an amplifier is the frequency range in which the amplifier is best working in. For a low noise amplifier bandwidth is decided by both gain and noise figure. Bigger bandwidth is considered as a desirable factor.

1.1.5 Impedance matching

Amplifiers are often used in multiple stages. In such cases the power transfer from one stage to next becomes a major deciding factor for the overall performance of the amplifier. Therefore the output impedance of first stage amplifier should be adjusted according to input impedance of second amplifier so that gain can be properly transferred.

1.2 Different topologies of LNA

Following 3 topologies are the most prevalent in low noise amplifier architecture

1.2.1 Common source

It has moderate gain compared to Common-gate and Cascode. The Low noise amplifier based on common source transistor is built to have the lowest noise figure and this major advantage has a drawback as the stability of the device is reduced considerably, the circuit becomes sensitive to temperature, bias, component tolerance etc. the bandwidth of common source is narrow. Due to high input impedance there is less signal attenuation. The output signal in case of common source is out of phase with input signal. Common source topology can be used in wideband applications using impedance matching circuits.

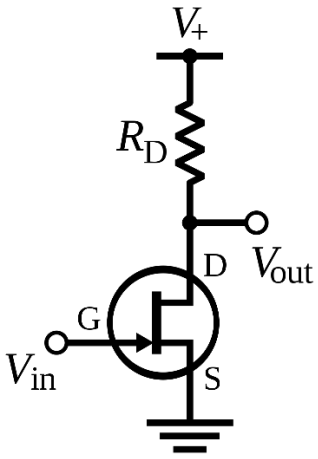

Fig1.2 Common source topology

1.2.2 Common gate

This topology for low noise amplifier is only suitable at low frequencies as the noise figure increases drastically with increase in frequency of input signal.
It has the worst gain in all three topologies talked about here. Except in gain and noise figure common gate is better than common source topology in linearity, bandwidth and stability.
Drawbacks in both common source and common gate topologies can be compensated using different techniques. Like in case of common gate topology the implementation of inductive feedback can improve gain and noise figure at higher frequencies

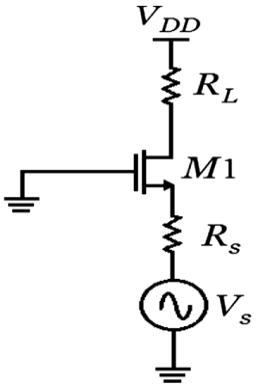

Fig 1.3 Common gate topology

1.2.3 Cascode

The cascode amplifier is a 2-stage amplifier with first and input stage as common-source and second stage as common-gate. The cascode topology produces the best performance amongst other three topologies. The disadvantage of this topology is increase in area and design complexity and slightly compromised noise figure. The advantages are highest gain, highest linearity, high stability and broadest bandwidth.

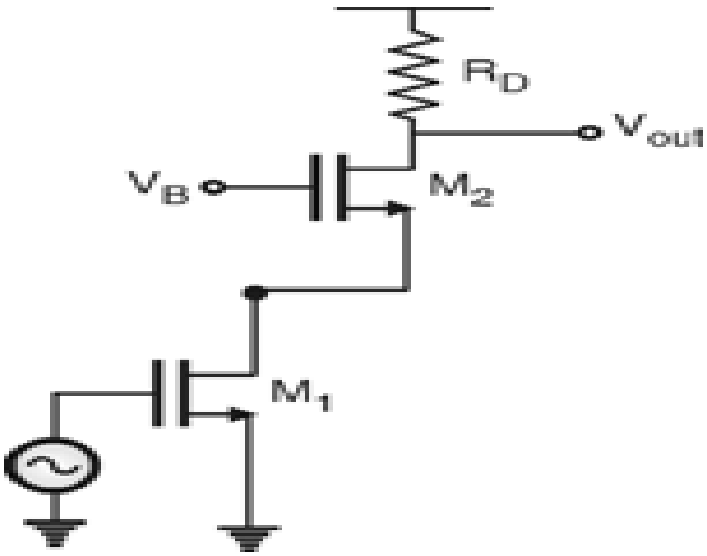

Fig 1.4 Cascode topology

1.3 .1 Transconductance amplifier

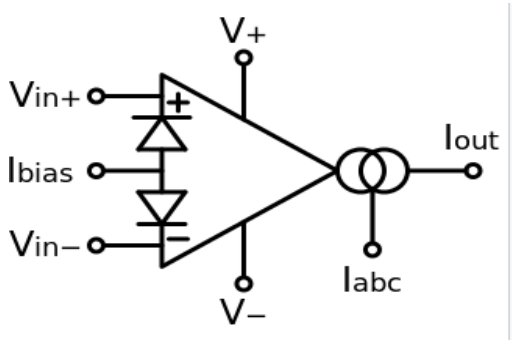

Fig 1.5 TA

A simple amplifier takes voltage as its input and produces a voltage at output. Compared to this a transconductance amplifier takes voltage as input and produces current as outputs. The gain is the ratio of output current to input voltage and is termed as transconductance of the whole amplifier. This gain can be controlled by changing the changing the transconductance of the amplifier through another input current. Functioning of transconductance is very to a operation amplifier as it has a high input impedance and can work with feedbacks to improve performance.

$$I_{out} = (V_{in+} - V_{in-}) * g_m$$

1.3.2 Differential amplifier

It's a two input device with a function to multiply the strength of the difference of voltages at both inputs. Devices 1 and 2 in figure 1.6 are mosfets with same characteristics. A bias current is used to keep both transistors in saturation mode and the drain of both the transistor is connected to a power supply through a load. Input voltages are applied at the gate of both transistor and the output is taken from the drain. Load at both sides are kept equal. Now since both transistor have same characteristics the drain current through them is also equal

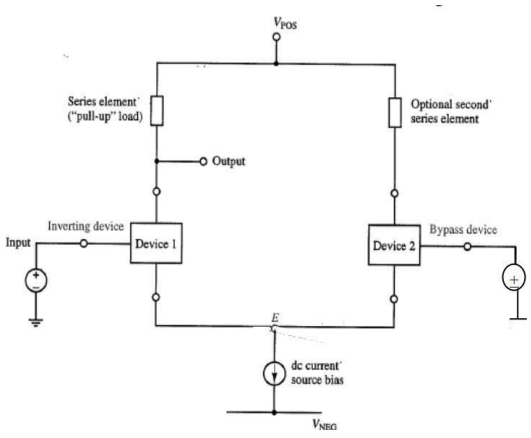

Fig1.6 Differential amplifier

1.3.3 Current mirror

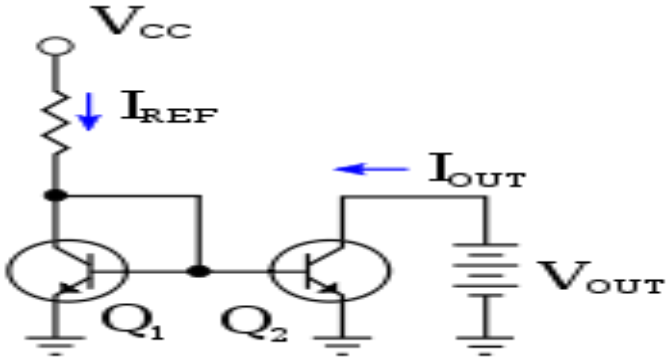

Fig 1.7 Current mirror

A current mirror has two transistors which have the same characteristics. Its main functionality is that current through one transistor can be controlled through the current through the other transistor. Here I_{ref} is set with the help of the resistor. And this I_{ref} current then determines the V_{gs} of both the transistors and thus sets output current I_{out} . Transistor Q2 has to be in saturation region for current mirror to work.

1.3.4 Current conveyor

Current mode circuits are those which work on current signal as input signal or output signal or control signal. Voltage mode circuits are those which work on voltage signals as input signals or output signals or control signals. Earlier Operation amplifiers were based on voltage mode but current mode amplifier have several advantages like better load transient response, better bandwidth, lower power consumption.

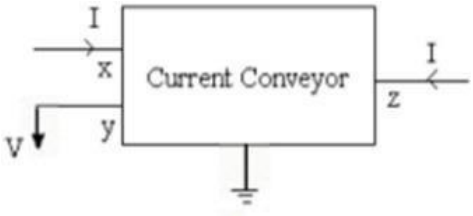

Fig1.8 Current conveyor

Above figure shows a current conveyor block diagram. It mainly has two inputs and one outputs. As we can see in this block diagram a voltage V has been applied at y terminal. A same voltage will then appear at x terminal. Similarly I current is applied at x terminal, same current will then appear at y terminal . output terminal z will produce same I current as output and will act as aconstant current source with high output impedance.

CHAPTER 2

LOW NOISE AMPLIFIER

2.1 Noise cancellation Technique

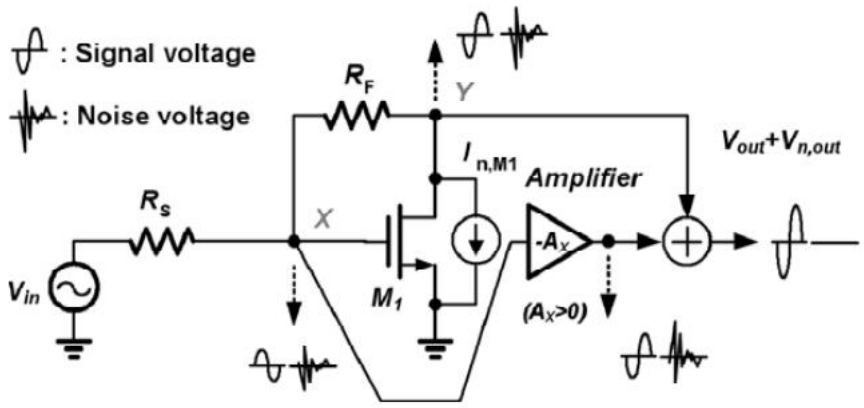

Fig 2.1 Simplified resistive shunt feedback using noise cancellation technique

Above figure shows a resistive shunt feedback LNA using noise cancellation technique. Here noise cancellation is achieved by producing a signal from the noise which has opposite polarity and add it to the noise thus cancelling its effect on the output.

As we can see in above circuit for noise cancellation the feedback path sends the noise of the common source amplifier back to its input from here it goes through a voltage amplifier which pushes it to out of phase. The output of this voltage amplifier is added to the noise from the common source and thus cancels it at the output of overall low noise amplifier. Here the output of common source amplifier is already out of phase with input signal of the common source amplifier and therefore when this signal is added to output of voltage amplifier signal since they are in-phase they add constructively . Therefore at output of LNA we successfully get only the amplified output signal with opposite polarity.

3.2 Low noise amplifier design

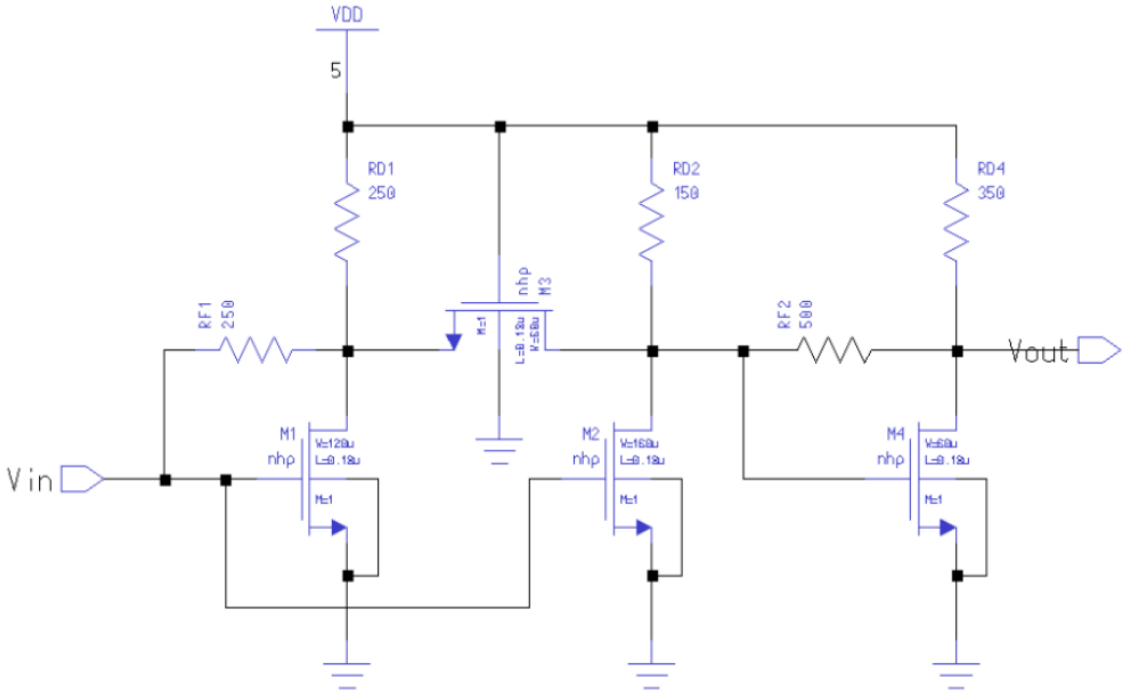

Fig 2.2 resistive shunt feedback noise cancelling LNA

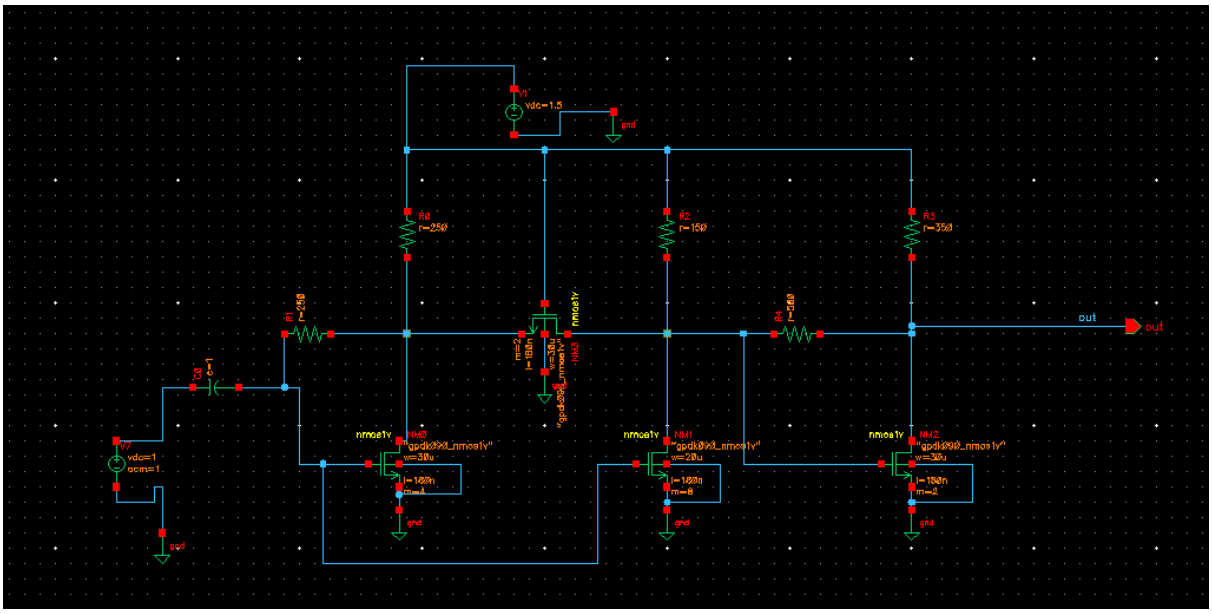

Fig 2.3 resistive shunt feedback noise cancelling LNA on virtuoso on 90nm technology

Fig 2.2 shows the actual LNA circuit implemented using noise cancellation technique. The resistor R_f acts as the feedback resistor in shunt. It is used to increase broadband of the amplifier and also for impedance matching. Also the noise from output of common gate configuration transistor is transferred to input using this resistor.

In common source configuration a polarity inversion occurs. Signals at output of transiStors M1 and M2 would have been out of phase if M3 would have been in common source configuration. To keep these signals in in-phase we are using common gate configuration since we cannot afford to use another stage to covert the polarity at output of M2 as it can increase power consumption. Next noise from M2 goes to the next transistor M4(also in common source configuration) and cancel with out of phase Noise at from r3

3.3 Proposed circuit

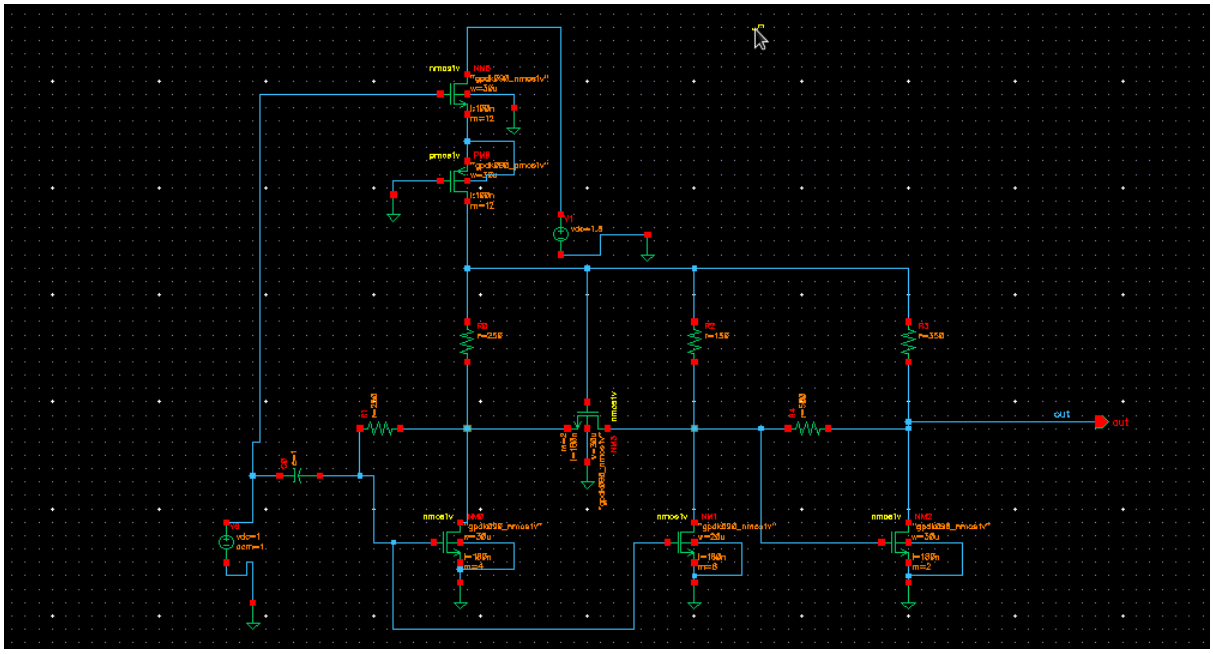

Fig 2.4 Proposed LNA circuit

Main aim in this project is to reduce the power consumed keeping the noise figure constant. Above figure shows the new proposed circuit. In this circuit a pseudo nmos is used as the power supply to reduce DC power consumption. The pseudo nmos basically shuts off the power supply to the parts of the circuit which are not in use during operation thereby reducing overall power consumption

In this project a Low noise amplifier based on above figure topology has been implement and simulated through cadence virtuoso software on 90 nm technology. Its gain versus frequency, power and noise have been calculated and analysed.

The resistive feedback helps in achieving input matching while increasing the bandwidth. The gain is increased while the power consumption is reduced. On the other hand the trade off with area is also minimized

In table 1 the width and length of all transistors is shown.

parameters	values
W_1	30u
W_2	20u
W_3	30u
W_4	30u
L_1,L_2,L_3,L_4	180n

Table 1 LNA design parameters

CHAPTER 3

DIFFERENTIAL DIFFERENT CURRENT CONVEYOR TRANSCONDUCTANCE AMPLIFIER(DDCCTA)

3.1 Theory

Differential difference amplifier basically amplifies the difference between three input voltages and has high input impedance, low output impedance. Current conveyor circuit can be used also with differential difference amplifier to increase the gain and bandwidth. This DDCC circuit can then act as input of operational transconductance amplifier. The DDCCTA has all the advantages from other circuits like differential voltage current conveyor transconductance amplifier. Often to implement DDCC and TA we connect there separate together as 2 stages but DDCCTA circuit can implement the same functionality on a single monolithic chip.

3.2 DDCCTA

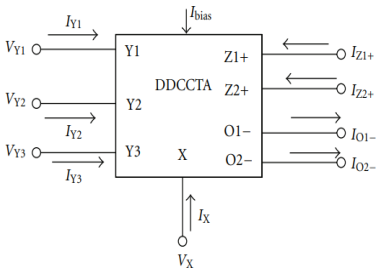

Fig 3.1 Block diagram of DDCCTA

The input-output relation is shown in the figure through a matrix. Through these relations we can clearly see DDCCTA circuit has four parts – Differential amplifier, current mirror, current conveyor, transconductance amplifier.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_{Z1+} \\ I_{Z2+} \\ I_{01} \\ I_{O2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1+} \\ V_{Z2+} \\ V_{O1-} \\ V_{O2-} \end{bmatrix},$$

3.1 Small signal analysis of DDCCTA circuit

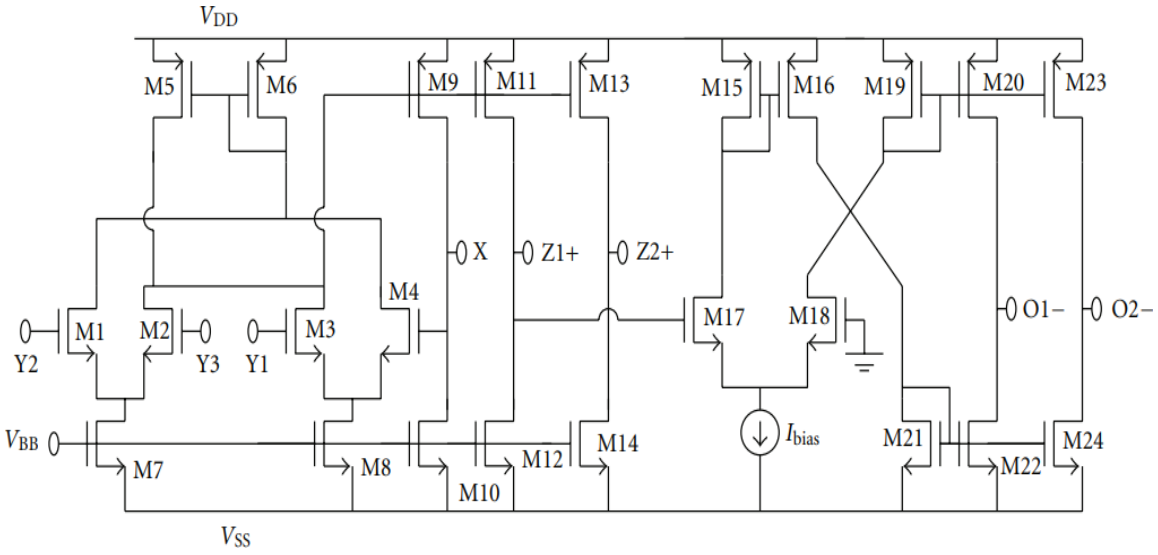

Fig 3.2 DDCCTA circuit

This is the internal circuit of DDCCTA. It is made up of 24 mosfets in total. The transconductance of the overall circuit is controlled through biasing circuit. In this project the basic aim was to implement and verify this designs operation and transconductance. The circuit is simulated on Ltspice at 0.25 um technology. Initially small signal model was used to verify the functionality of the circuit and then transconductance of this amplifier is calculated practically and theoretically. Input output graph is also plotted in simulation results.

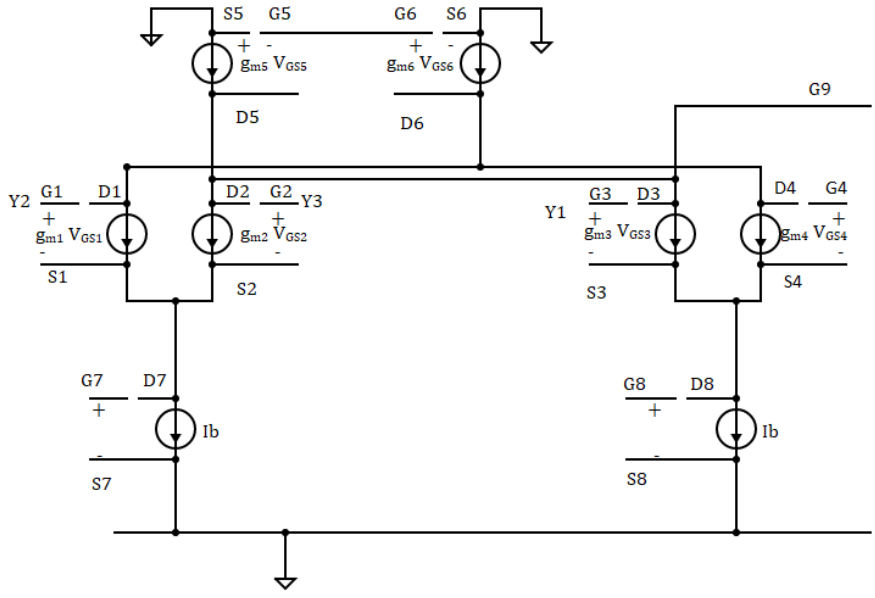

Fig3.3.1 Small signal model of DDCTA circuit

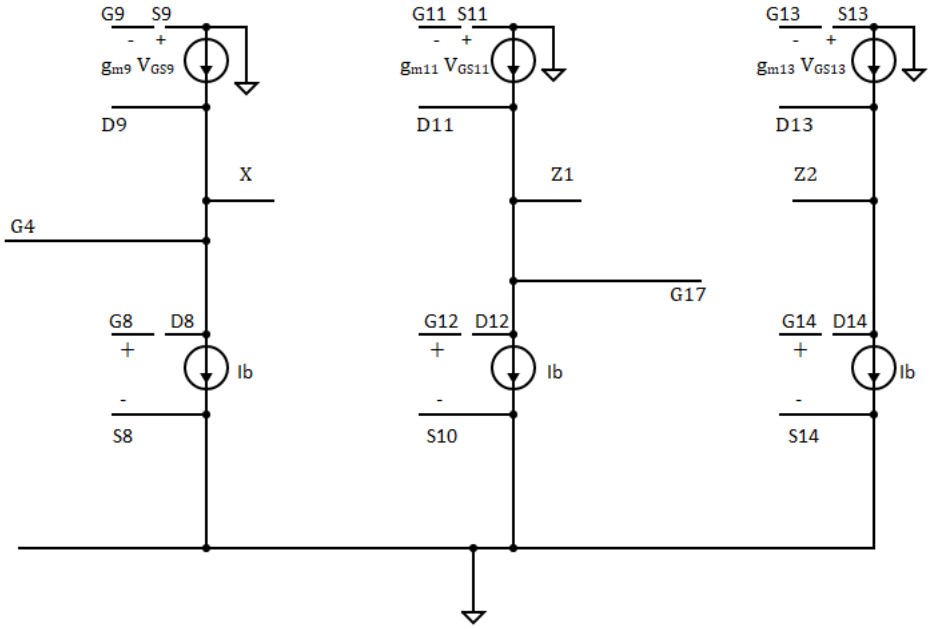

Fig 3.3.2 Small signal model of DDCTA circuit

$Y_3 - V_{GS2} = V_2 - V_{GS1}$ (1)

$Y_1 - V_{GS3} = V_X - V_{GS4}$ (2)

$g_{m1} V_{GS1} + g_{m2} V_{GS2} = I_B = g_{m3} V_{GS3} + g_{m4} V_{GS4}$ (3)

$g_{m5} V_{GS5} = g_{m2} V_{GS2} + g_{m3} V_{GS3}$ (4)

$g_{m6} V_{GS6} = g_{m1} V_{GS1} + g_{m4} V_{GS4}$ (5)

$V_{GS5} = V_{GS6}$ (6)

Using equations (4), (5) & (6),

$\Rightarrow \frac{g_{m2} V_{GS2} + g_{m3} V_{GS3}}{g_{m5}} = \frac{g_{m1} V_{GS1} + g_{m4} V_{GS4}}{g_{m6}}$

$\Rightarrow g_{m6} g_{m2} V_{GS2} - g_{m1} g_{m5} V_{GS1} = g_{m4} g_{m5} V_{GS4} + g_{m3} g_{m6} V_{GS3}$ (7)

$V_{GS1} = Y_2 - Y_3 + V_{GS2}$

Using equation (3),

$\Rightarrow g_{m1} (Y_2 - Y_3 + V_{GS2}) + g_{m2} V_{GS2} = I_B$

$\Rightarrow V_{GS2} = \frac{(I_B - g_{m1} Y_2 + g_{m1} Y_3)}{(g_{m1} + g_{m2})}$ (8)

Therefore, $V_{GS1} = Y_2 - Y_3 + \frac{(I_B - g_{m1} Y_2 + g_{m1} Y_3)}{(g_{m1} + g_{m2})}$ (9)

Similarly using equations (2) & (3),

$V_{GS3} = \frac{(I_B - g_{m4} V_x + g_{m4} Y_1)}{(g_{m3} + g_{m4})}$ (10)

$V_{GS4} = V_x - Y_1 + \frac{(I_B - g_{m4} V_x + g_{m4} Y_1)}{(g_{m3} + g_{m4})}$ (11)

Using equations (7), (8), (9), (10) & (11),

$$I_B\left(\frac{(g_{m4}\,g_{m5})}{(g_{m3}+g_{m4})}-\frac{(g_{m3}\,g_{m6})}{(g_{m3}+g_{m4})}\right)+(V_x-Y_1)\left(g_{m4}\,g_{m5}-\frac{g_{m4}\,(g_{m4}\,g_{m5}-g_{m3}\,g_{m6})}{g_{m3}+g_{m4}}\right)=$$
$$I_B\left(\frac{(g_{m2}\,g_{m6})}{(g_{m1}+g_{m2})}-\frac{(g_{m1}\,g_{m5})}{(g_{m1}+g_{m2})}\right)+(Y_3-Y_2)\left(g_{m1}\,g_{m5}-\frac{g_{m1}\,(g_{m1}\,g_{m5}-g_{m2}\,g_{m6})}{g_{m1}+g_{m2}}\right) \quad (12)$$

In equation (12), put $g_{m1}= g_{m2}= g_{m3}= g_{m4}$ and $g_{m5}= g_{m6}$

$\Rightarrow V_{x}= V_{Y1} - V_{Y2} + V_{Y3}$

$I_X + g_{m9}\, V_{GS9} = I_B$ (13)

$I_{Z1} + g_{m11}\, V_{GS11} = I_B$ (14)

Using equation (13),

$\Rightarrow V_{GS9} = \frac{I_B - I_X}{g_{m9}}$ (15)

Also, $V_{GS9}= V_{GS11}$ (16)

Using equations (14), (15), (16),

$\Rightarrow I_{Z1} - g_{m11}\frac{I_X - I_B}{g_{m9}} = I_B$

$\Rightarrow I_{Z1} = I_X\frac{g_{m11}}{g_{m9}} + I_B\left(1-\frac{g_{m11}}{g_{m9}}\right)$

If $g_{m11}= g_{m9}$

$\Rightarrow I_{Z1} = I_X$

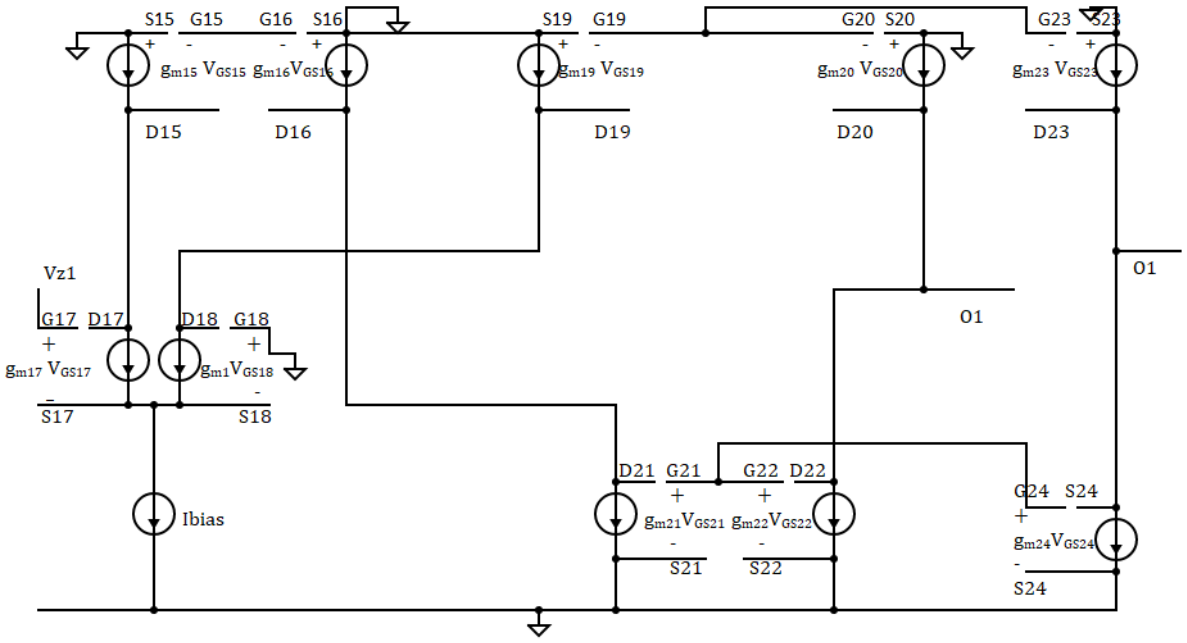

Fig 3.3.4 Small signal model of DDCTA circuit

$I_{O1} = g_{m22}\, V_{GS22} + g_{m20}\, V_{GS20}$ (1)

$I_{O2} = g_{m24}\, V_{GS24} + g_{m23}\, V_{GS23}$ (2)

$g_{m17}\, V_{GS17} + g_{m18}\, V_{GS18} = I_{bias}$ (3)

$0 - V_{GS18} = V_{Z1} - V_{GS17}$

$\Rightarrow V_{GS17} = V_{Z1} + V_{GS18}$ (4)

$g_{m19}\, V_{GS19} = g_{m18}\, V_{GS18}$ (5)

$g_{m16}\, V_{GS16} = g_{m21}\, V_{GS21}$ (6)

$V_{GS15} = V_{GS16}$ (7)

$g_{m15}\, V_{GS15} = g_{m17}\, V_{GS17}$ (8)

$V_{GS23} = V_{GS19} = V_{GS20}$ (9)

$V_{GS21} = V_{GS22} = V_{GS24}$ (10)

Using equations (3), (4),

$\Rightarrow V_{GS18} = \frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}$

$\Rightarrow V_{GS17} = V_{z1} + \frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}$

Using equations (5), (9),

$\Rightarrow V_{GS20} = V_{GS19} = \frac{g_{m18}}{g_{m19}} \left(\frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}\right)$

Using equations (8), (10),

$\Rightarrow V_{GS22} = V_{GS21} = \frac{g_{m17}}{g_{m15}} \left(V_{Z1} + \frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}\right)$

Using the above in equation (1),

$\Rightarrow I_{O1} = \frac{g_{m22} g_{m17}}{g_{m15}} \left(V_{Z1} + \frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}\right) + \frac{g_{m20} g_{m18}}{g_{m19}} \left(\frac{I_{bias} - g_{m17} V_{z1}}{g_{m17} + g_{m18}}\right)$

With $g_{m17} = g_{m18}$, $g_{m21} = g_{m22} = g_{m24}$, $g_{m15} = g_{m16} = g_{m19} = g_{m20} = g_{m23}$

$\Rightarrow I_{O1} = g_{m17}\, V_{Z1}$

CHAPTER 4

SIMULATION AND RESULTS

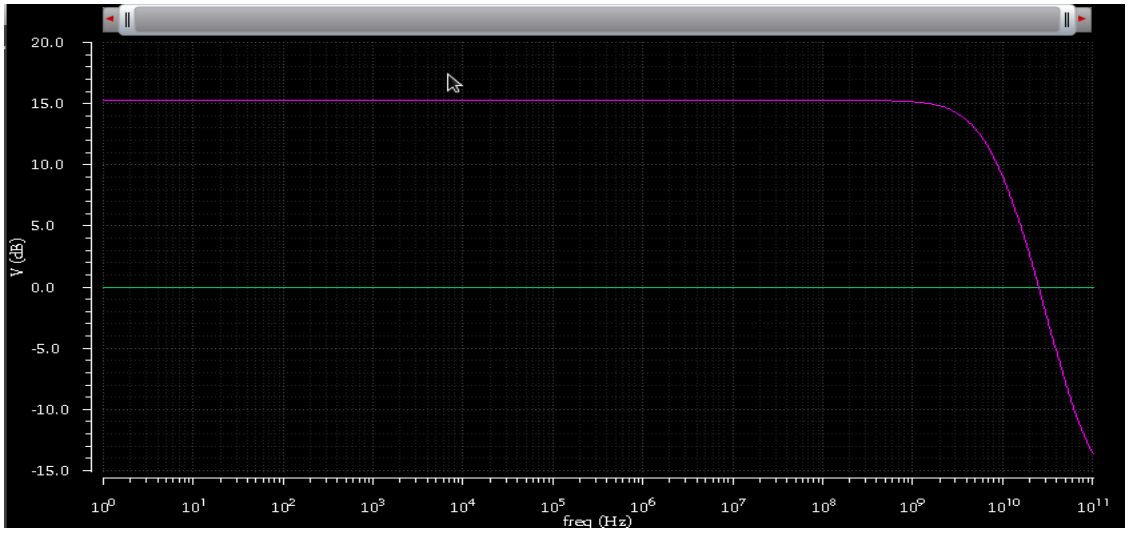

Fig 4.1.1. LNA gain at 1v

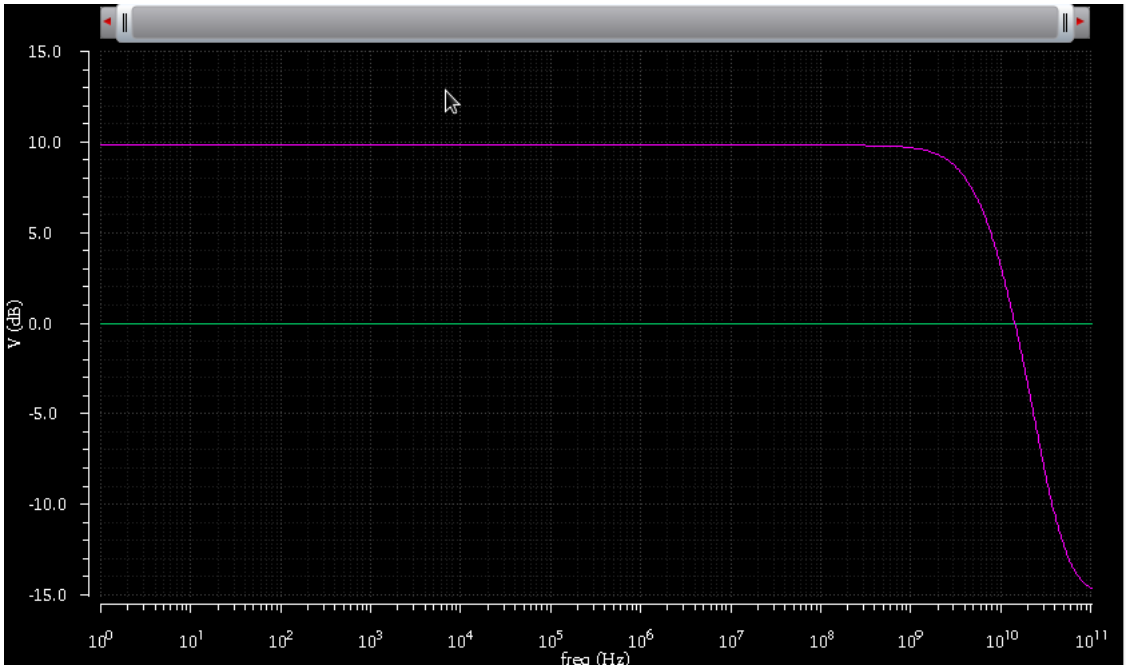

Fig 4.1.2 Proposed LNA gain at 1V

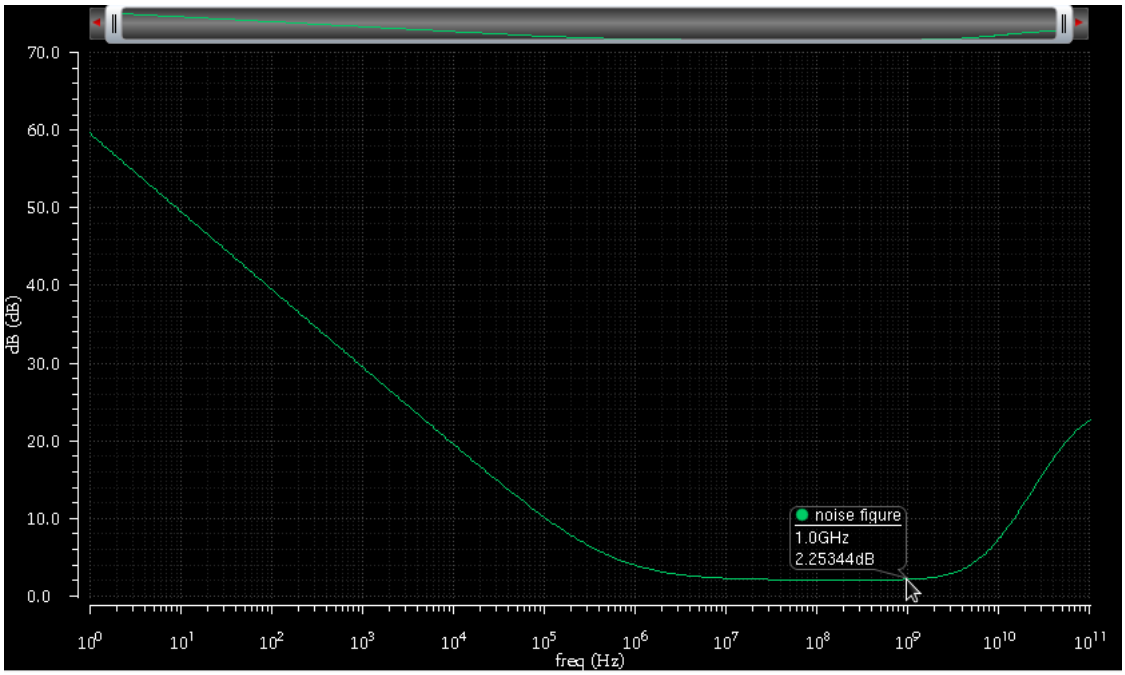

Fig 4.2.1 LNA NF at 1V

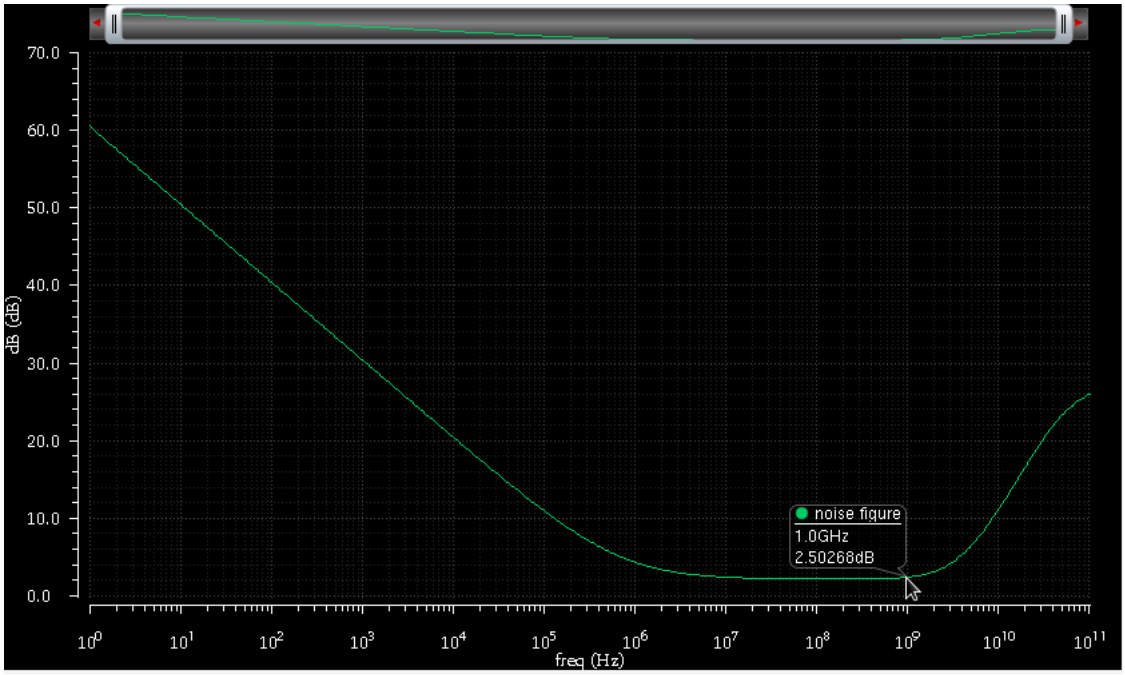

Fig 4.2.2 Proposed LNA NF at 1V

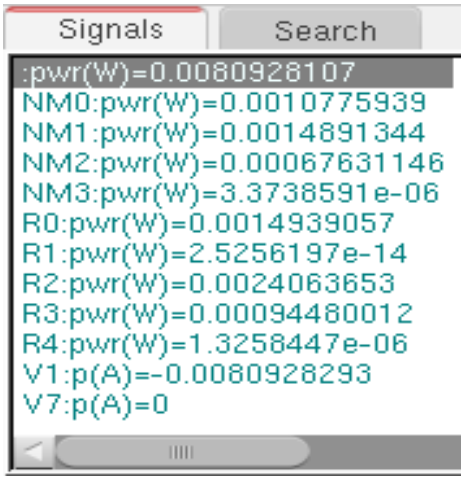

Fig 4.3.1 LNA power consumed at 1 v

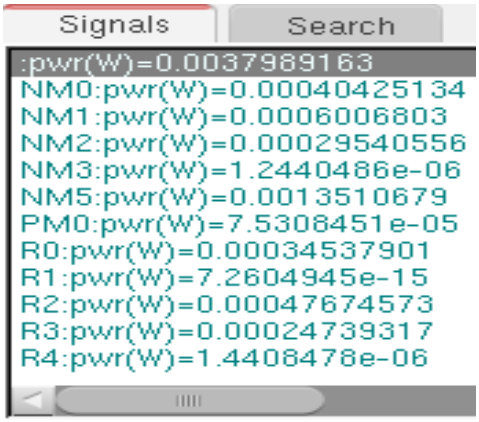

Fig 4.3.2 Proposed LNA power consumed at 1V

We can compare the results at 1V for both designs

- LNA gain is 15.2dB, proposed LNA gain is 9.9 dB
- LNA NF is 2.25dB, proposed LNA NF is 2.5dB at 1GHz
- LNA power is 8.09mW, proposed LNA power is 3.7mW

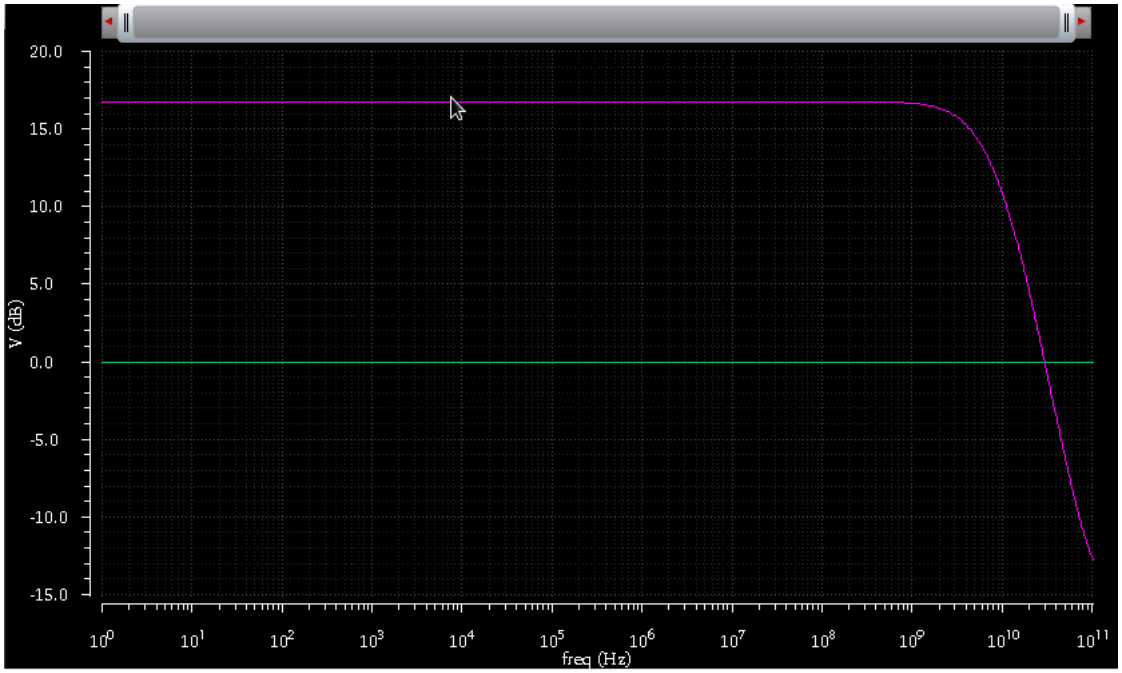

Fig 4.4.1 LNA gain at 1.2V

Fig 4.4.2 Proposed LNA gain at 1.2V

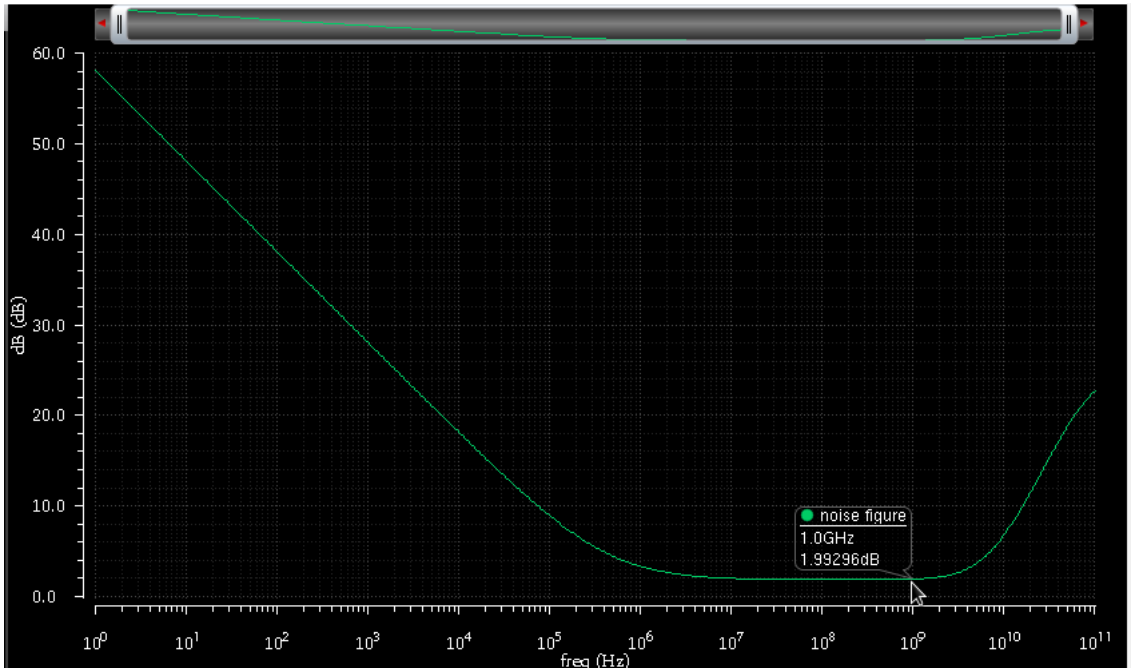

Fig 4.5.1 LNA NF at 1.2V

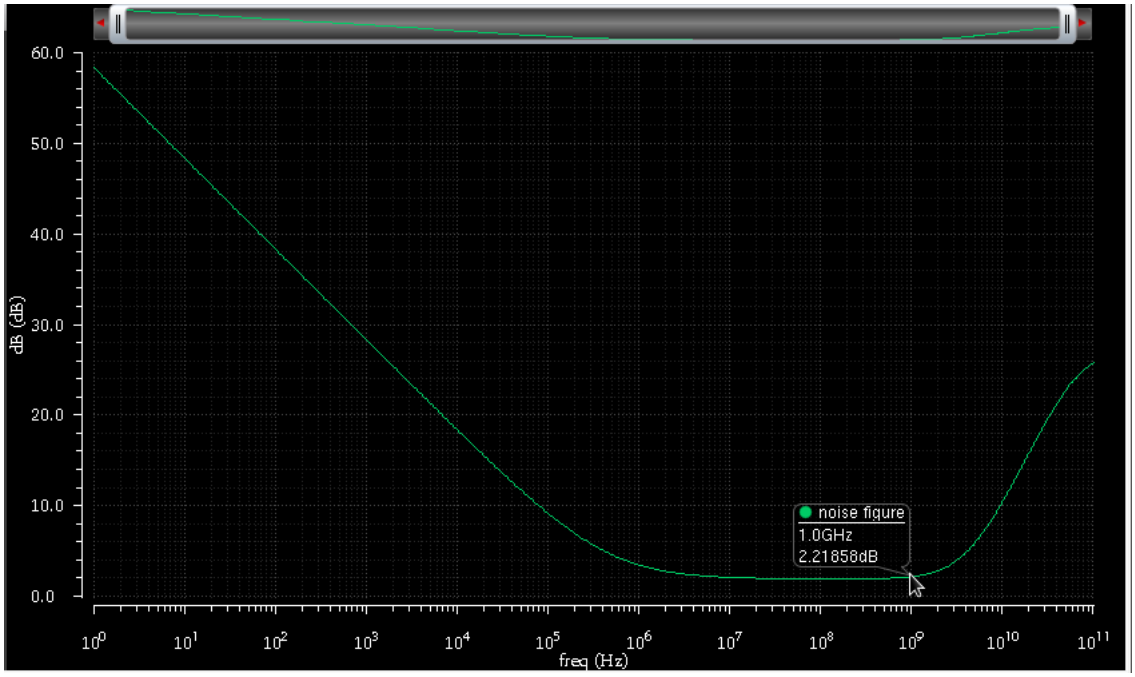

Fig 4.5.2 Proposed LNA output noise at 1.2V

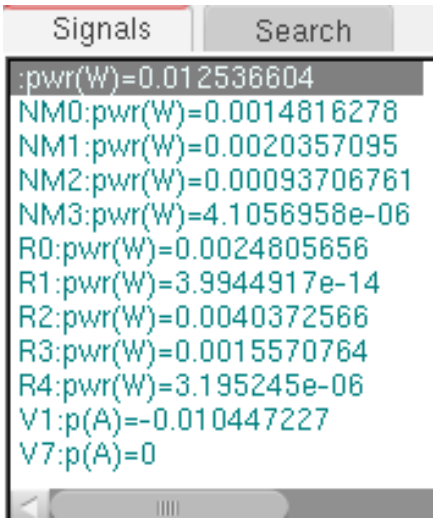

Fig 4.6.1 Proposed LNA power consumed at 1.2V

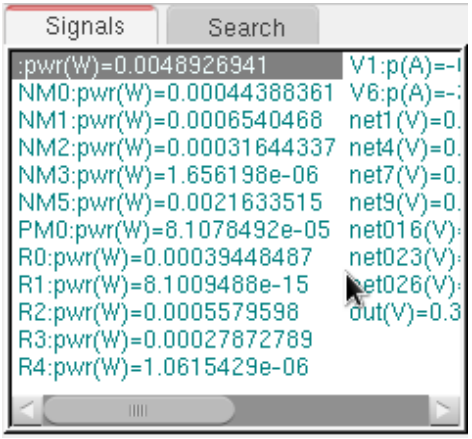

Fig 4.6.2 Proposed LNA power consumed at 1.2V

We can compare the results at 1.2V for both designs

- LNA gain is 16.6dB, proposed LNA gain is 10.4 dB
- LNA NF is 1.99dB, proposed LNA NF is 2.21dB at 1GHz
- LNA power is 12.5mW, proposed LNA power is 4.89 mW

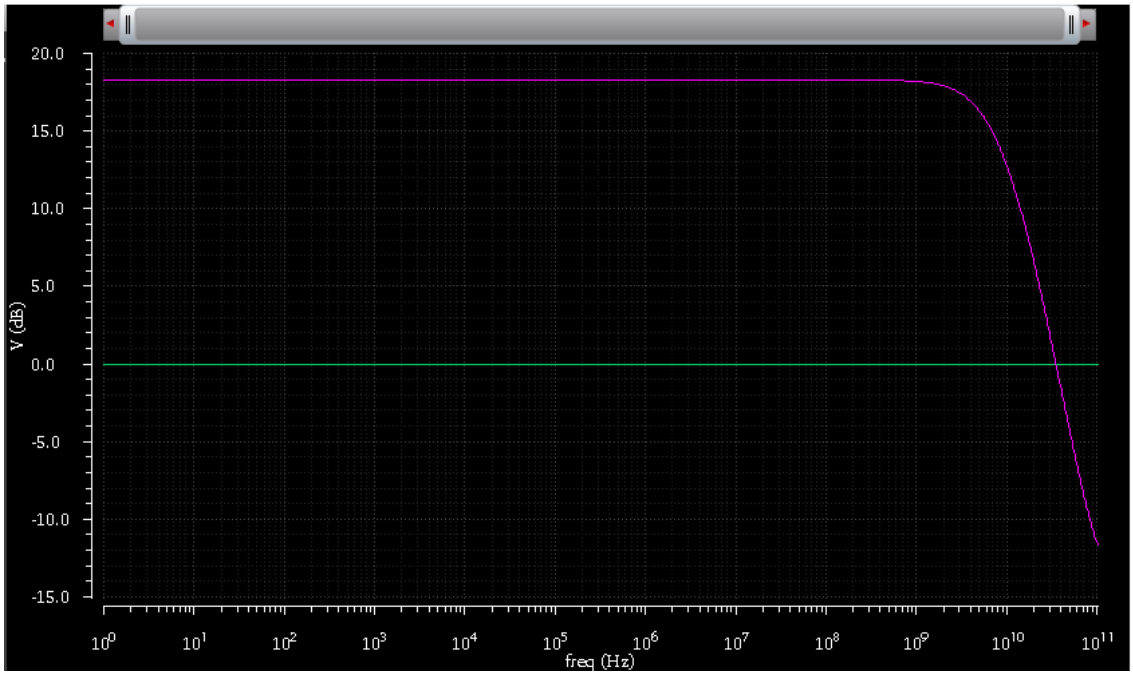

Fig 4.7.1 LNA gain at 1.5V

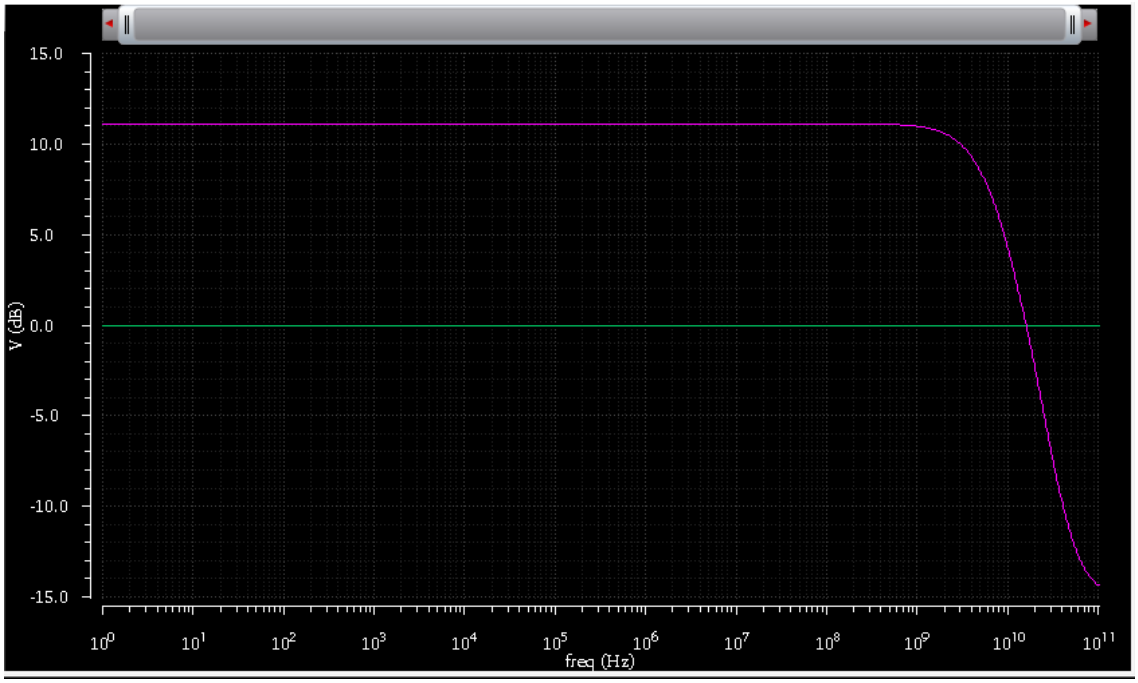

Fig 4.7.2 Proposed LNA gain at 1.5V

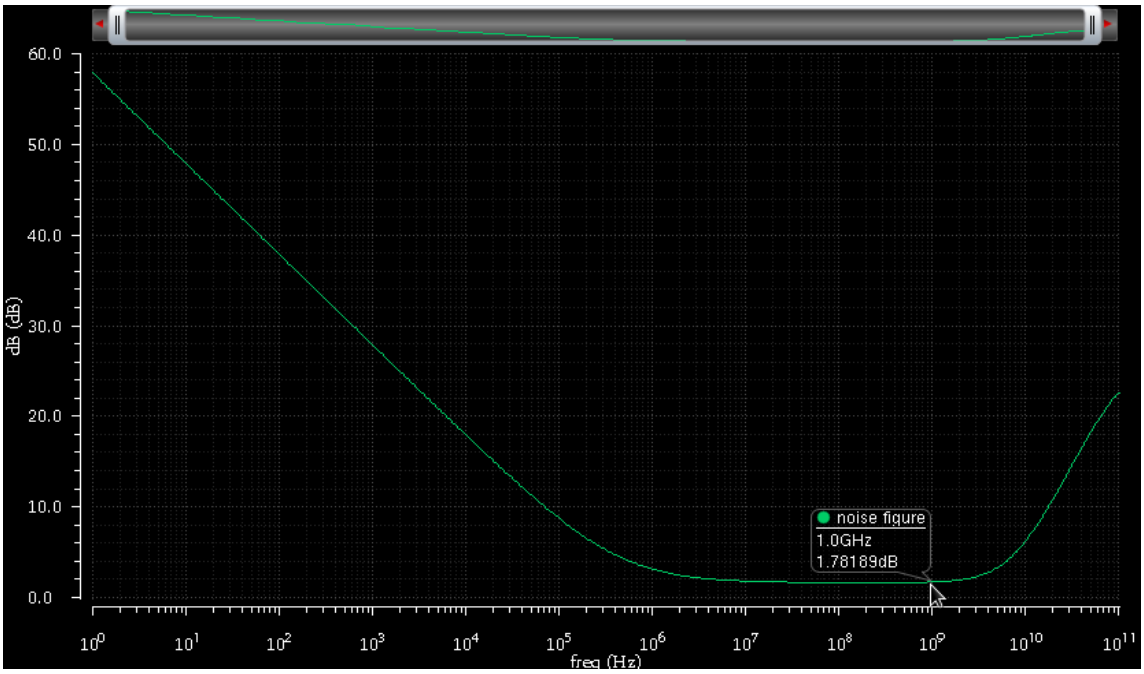

Fig 4.8.1 LNA NF at 1.5V

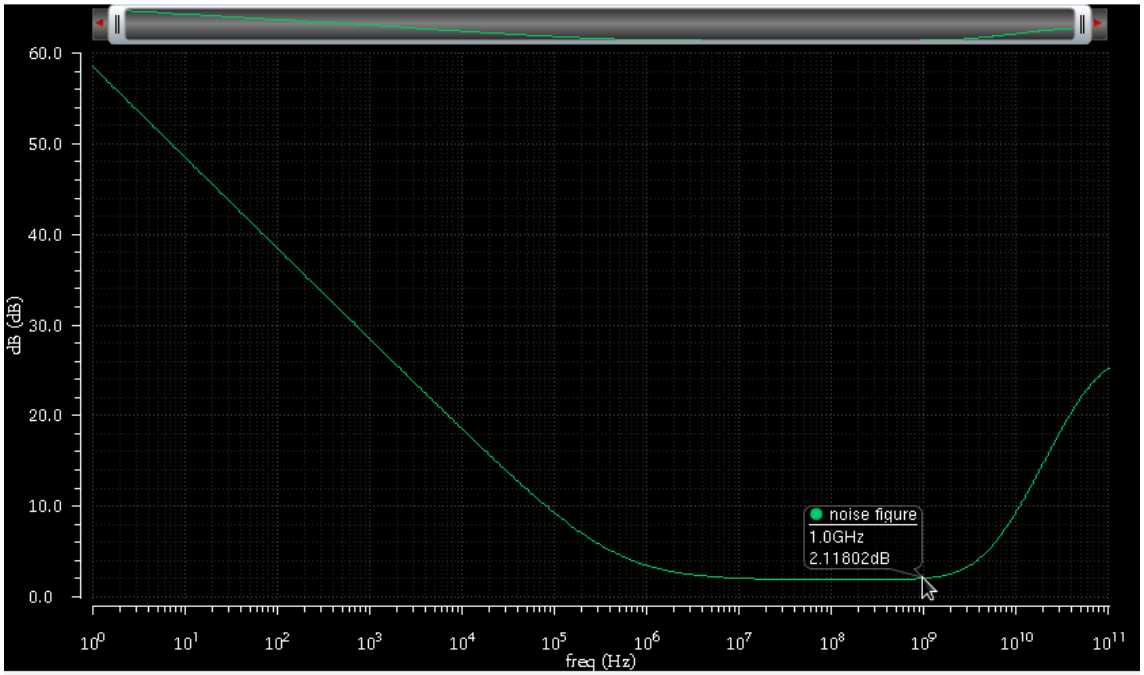

Fig 4.8.2 Proposed LNA NF at 1.5V

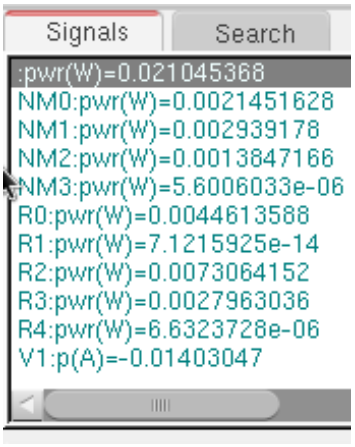

Fig 4.9.1 LNA power consumed at 1.5V

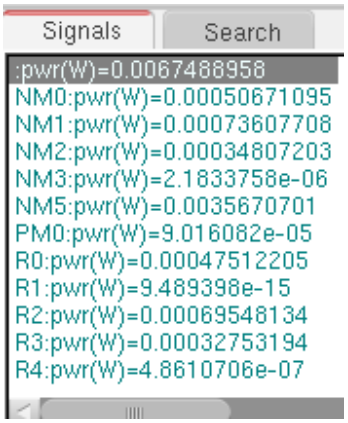

Fig 4.9.2 Proposed LNA power consumed at 1.5V

We can compare the results at 1.5V for both designs

- LNA gain is 18.3dB ,proposed LNA gain is 11.1 dB
- LNA NF is 1.78dB, proposed LNA NF is 2.11dB at 1GHz
- LNA power is 21.04mW, proposed LNA power is 6.7mW

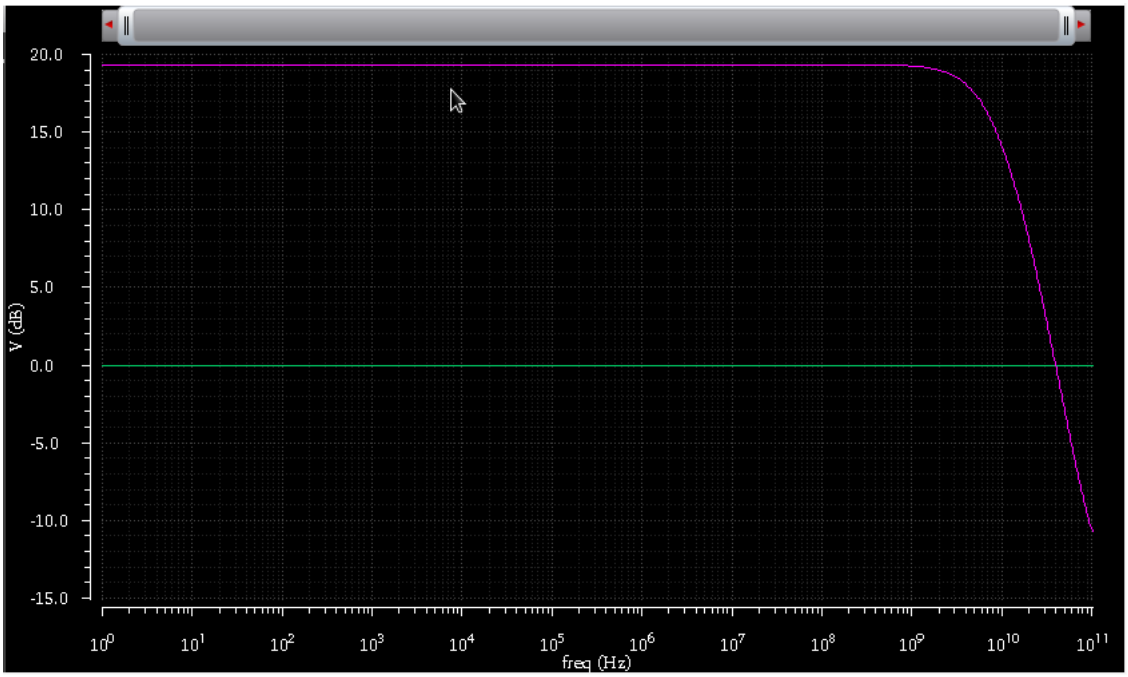

Fig 4.10.1 LNA gain at 1.8V

Fig 4.10.2 Proposed LNA gain at 1.8V

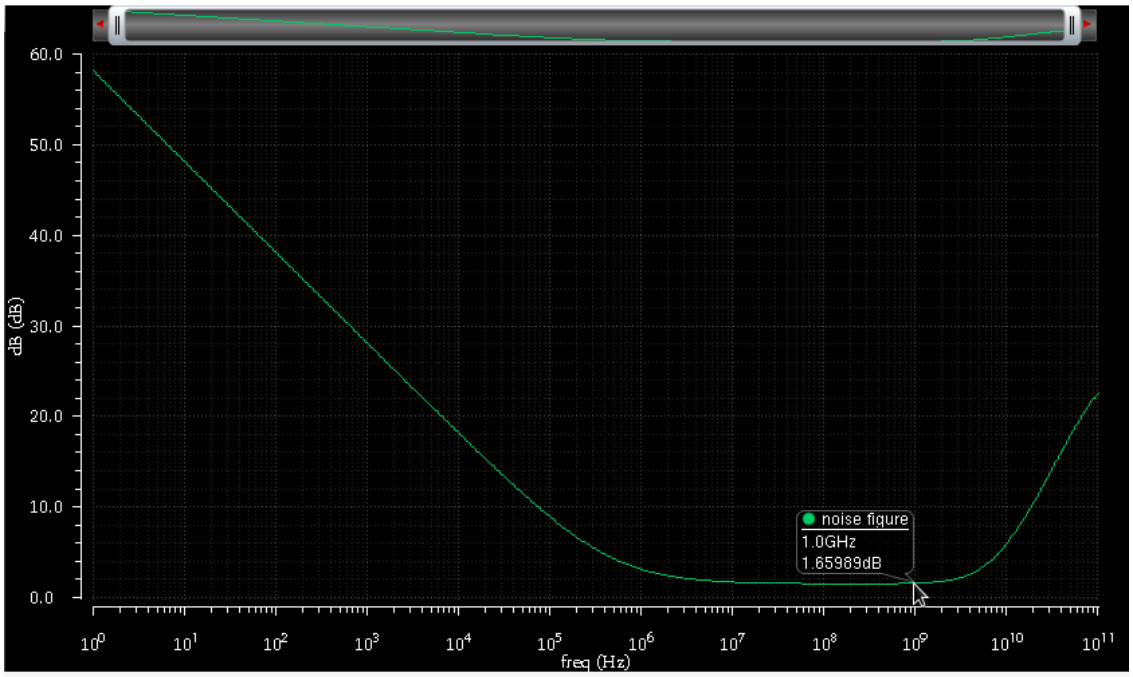

Fig 4.11.1 LNA NF at 1.8V

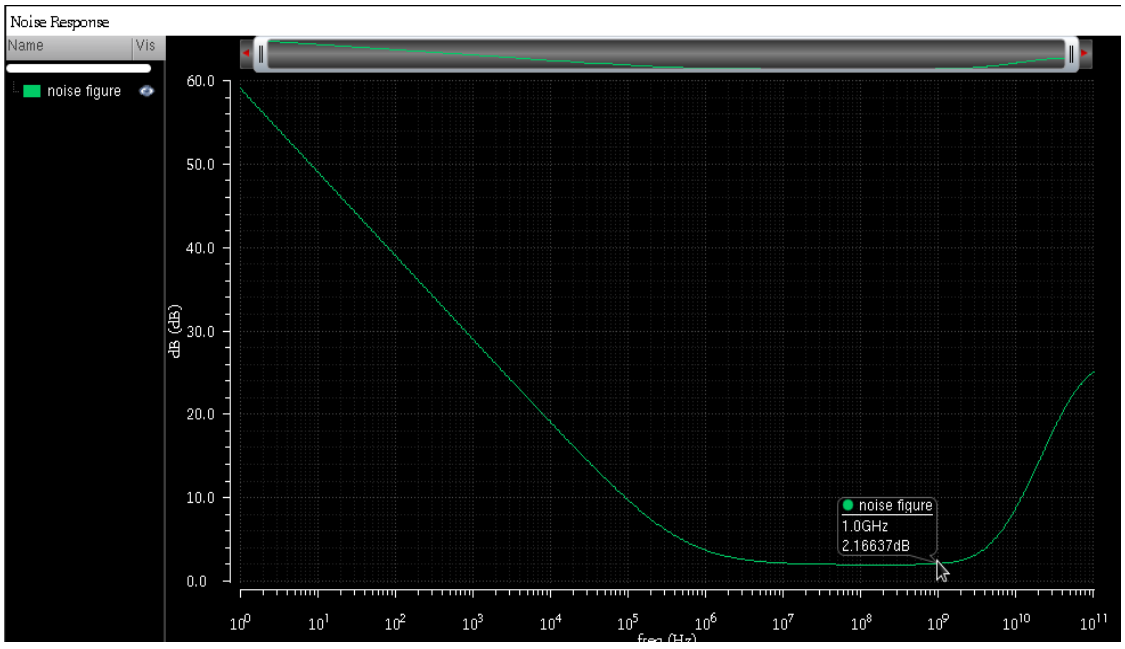

Fig 4.11.2 Proposed LNA NF at 1.8V

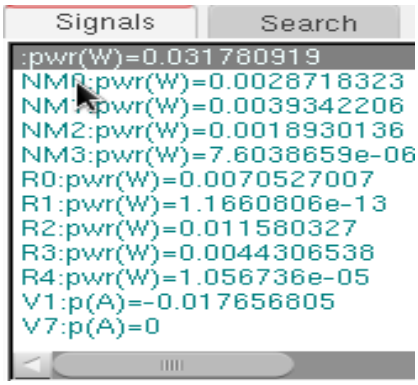

Fig 4.12.1 LNA power consumed at 1.8V

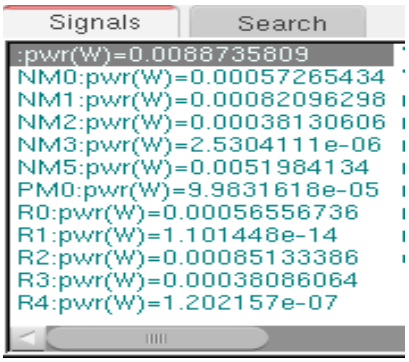

Fig 4.12.2 Proposed LNA power consumed at 1.8V

We can compare the results at 1.8V for both designs

- LNA gain is 19.2dB proposed LNA gain is 11.8 dB
- LNA NF is 1.65dB proposed LNA NF is 2.16dB at 1GHz
- LNA power is 31.7mW proposed LNA power is 8.87mW

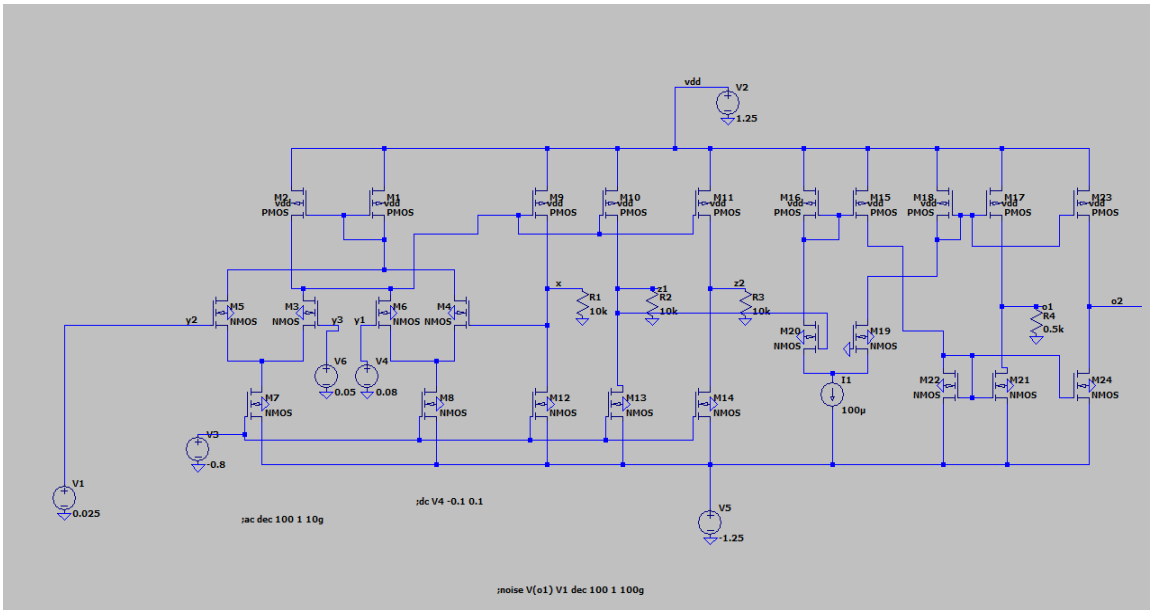

Fig 13 DDCTAA circuit

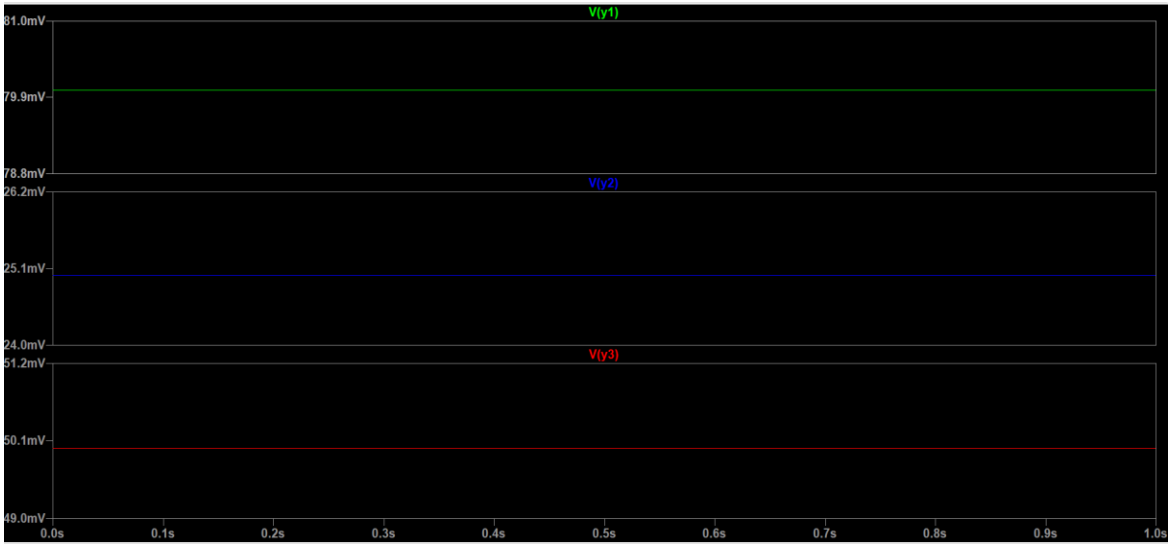

Fig 4.14.1 input Y

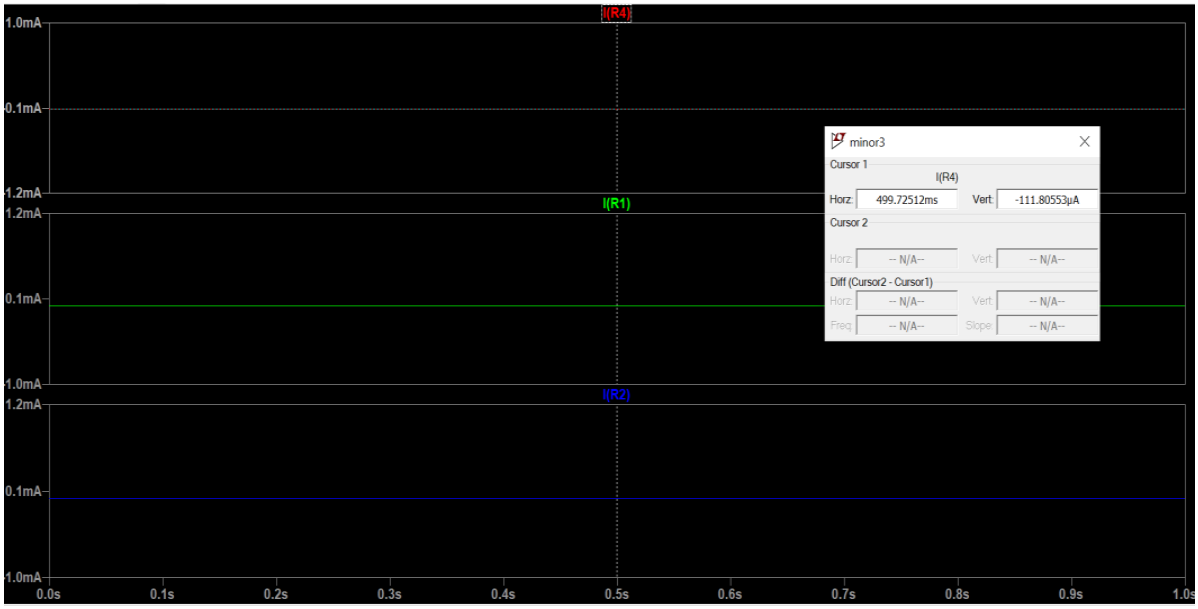

Fig 4.14.2 Output current Io1, Ix,Iz

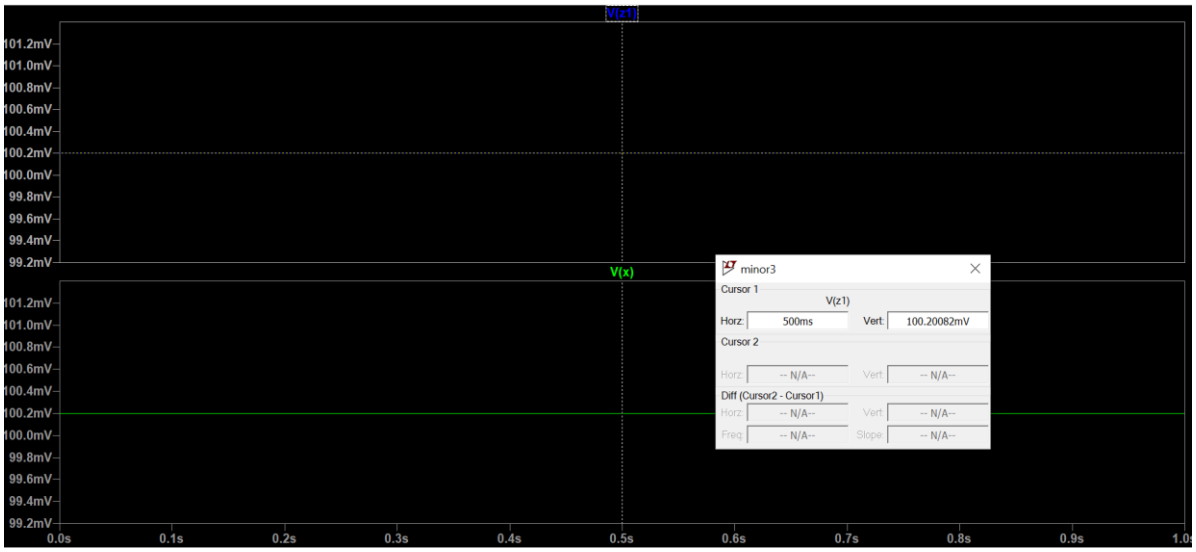

Fig 4.14.3 Output voltages V(z1), V(x)

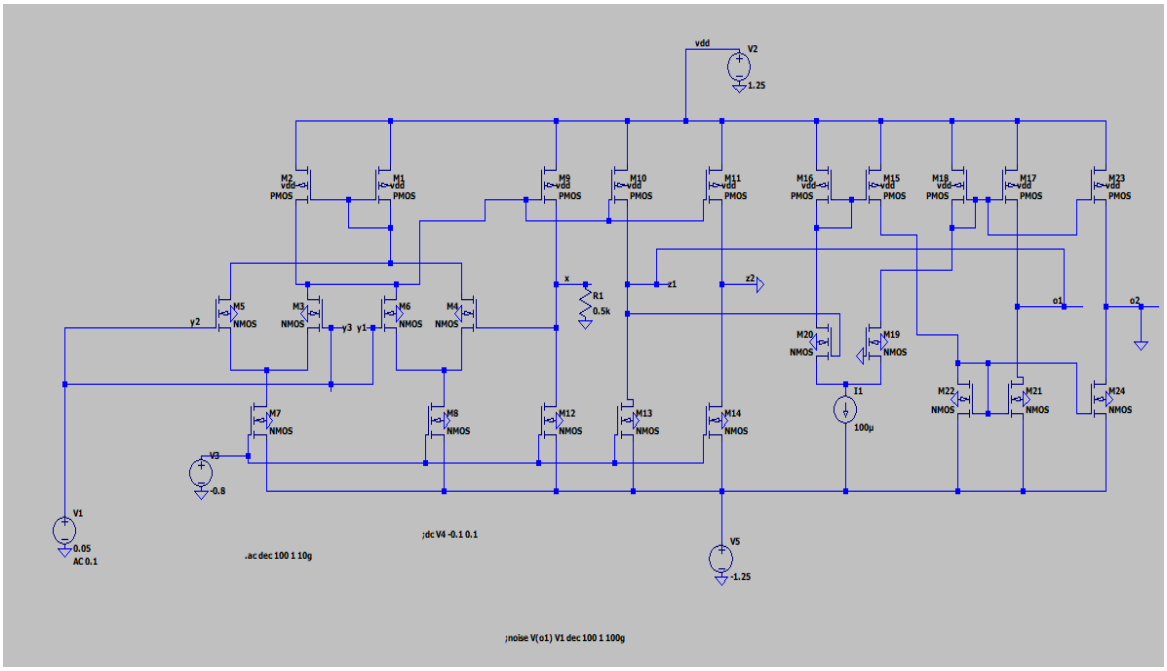

Fig 4.15 DDCCTA as voltage amplifier

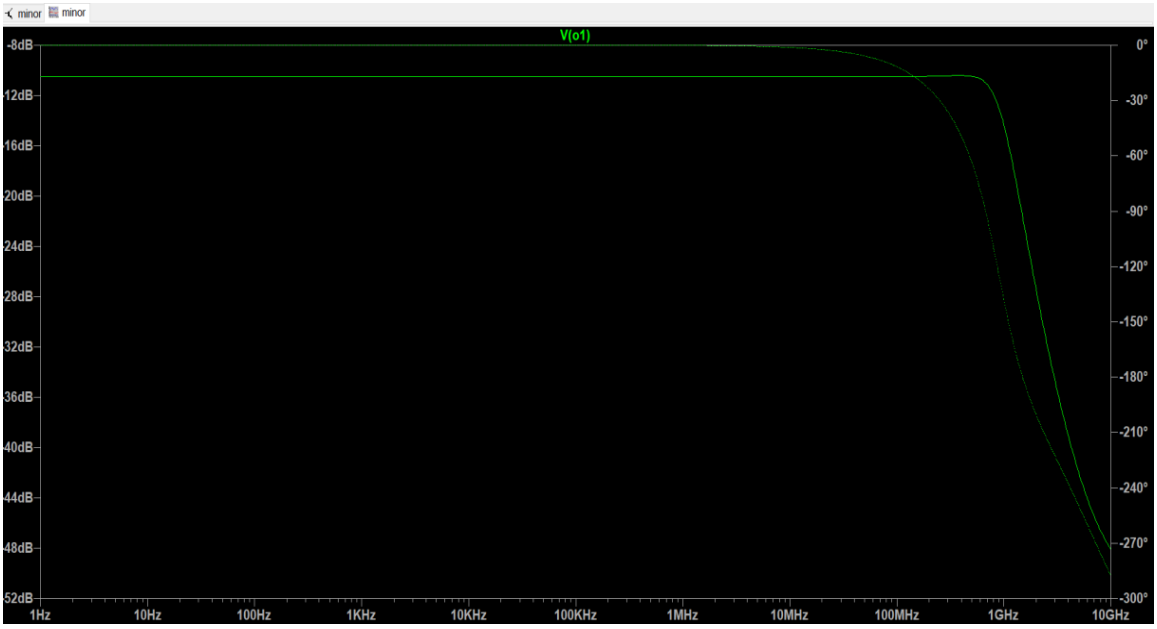

Fig 4.16 Output(bandwidth 962MHz)

Verifying Transconductance,

$g_{m17} = \sqrt{(2\ \mu\, cox(^{\omega}/_{l})_{17}\ I_D)}$

$2\ \mu\, cox(^{\omega}/_{l})_{17} = 75.398 * 10^{-4}\ \ ^{A}/_{V^2}$

From the ciruit we calculate the value of drain current through

$I_D = 83.6\ \mu A$

$g_{m17} = \sqrt{2 * 75.398\ *\ 10^{-4} * 83.6 *\ 10^{-6}} = 1.12$ mS (Theoretical Value)

$g_{m17} = \frac{I_{O1}}{V_{Z1}} = \frac{111.8\ \mu A}{100.2\ mV} = 1.115$ mS (Practical Value)

CONCLUSION

For the low noise amplifier, from the above simulation results we can verify that there was a successful power reduction in the design keeping noise figure almost same. There is a trade off with gain and area. The bandwidth of LNA is 1MHz-2GHz and is not affected by the modification in LNA circuit.

Voltage supply	LNA	Proposed LNA
1	8.09mW	33.7mW
1.2	12.5mW	4.89mW
1.5	21.04mW	6.7mW
1.8	31.7mW	8.87mW

Table 2. power consumption at different voltages

Voltage supply	LNA	Proposed LNA
1	15.5	9.9
1.2	16.6	10.4
1.5	18.3	11.1
1.8	19.2	11.8

Table 3 gain at different voltages

The noise figure for the proposed LNA is 2.09dB and the original LNA has 1.79dB noise figure.

For the differential difference current conveyor transconductance amplifier we successfully verified the result,
$V_{x1} = V_{y1} - V_{y2} + V_{y3}$

The theoretical and practical value of transconductance showed an error of 2.6%.
Then DDCCTA as implemented as voltage amplifier to check for bandwidth and gain.
Gain came out to be 9dB and cut off frequency was 962MHz

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