COMPARATIVES ANALYSIS OF RING OSCILLATOR FOR LOW POWER APPLICATION

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SUBMITTED BY:

RASHMI BHARTI

2K19/VLS/13

UNDER THE SUPERVISION

Dr. POORNIMA MITTAL

PROFESSOR

ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

NOV, 2021

ELECTRONICS & COMMUNICATION

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(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

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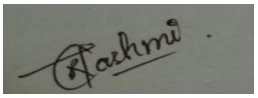
I, Rashmi Bharti, Roll No. 2K19/VLS/13 student of M.Tech (VLSI & Embedded systems), hereby declare that the project Dissertation titled **"Comparatives Analysis of Ring Oscillator for Low Power Application"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.



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DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"Comparatives Analysis of Ring Oscillator for Low Power Application"** which is submitted by **Rashmi Bharti, 2K19/VLS/13**, to the Department of Electronics & Communication Enigineering, Delhi Technological University, Delhi in partial fulfillment of the prerquisite for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date**:** Nov 12, 2021

Prof. Poornima Mittal

Supervisor

Professor

Department of ECE, DTU

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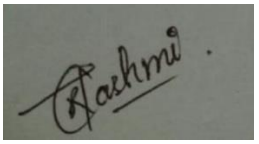

Rashmi Bharti

2K19/VLS/13

M.Tech: VLSI Design and Embedded System

(2019-2021)

ABSTRACT

VLSI is an evergreen field that is constantly expanding. To fit more gates on a given chip area, a significant amount of work is required. As a result, removing the heat generated is difficult. Using low-power circuits, this problem can be solved. In the time being computerized industry, a low power requirement has become primary goal. In the design of VLSI chips, power draining has becomes as critical as performance and size. Low-power chip requirements are becoming increasingly important in the VLSI business as chip dimensions shrink and environmental issues become more important. Because of the requirement to low package cost and increase battery life, power optimization is as critical as time for many systems. In the past, the total power dissipation of CMOS devices was dominated by dynamic power. This thesis discusses CMOS, lector, forced NMOS, forced 2 NMOS, forced PMOS as approaches for reducing power requirements at various stages of CMOS architecture. The results are examined at various supply voltages while maintaining the load capacitance (C_{load} = 500fF) which include power, delay, switching threshold voltage, noise margin, the inverter utilizing forced NMOS technology is considered good because the noise margin obtained is the highest here, 2.48V evaluated at 4.02V supply voltage. When all other factors are equal, the inverter adopting the lector approach consumes less power than the other inverters at all supply voltages.

This thesis approaches with the design and exploration of the frequency of ring oscillators using the CMOS 45nm, 32nm, 22nm in a Symica simulation tool. A Ring Oscillator is an effectual device incorporated of an odd number of NOT gates and its output runs between two levels of power standing up and down. There are many challenges forth while framing a CMOS ring oscillator that can be delay, sound, and glitches. CMOS is the technology of choice for several applications, low-power CMOS oscillators are in high demand. The frequency of a CMOS ring oscillator was measured using waveform time zones for five, seven, and nine phases. This aids in the comparison of ring oscillators at various technology nodes and it is observed that the frequency is found to be maximum at a five-stage ring oscillator in each case i.e. 12.97GHz at 45 nm, 8.25GHz at 32 nm, 4.74GHz at 22 nm.

Further, the designing of the ring oscillator is done to keep down the power consumption of the circuit while making the other parameters like the dimensions of the

transistors constant i.e. width and length of transistor at 45nm technology. The proposed designs of the ring oscillator are sleepy stack ring oscillator, forced NMOS ring oscillator, forced 2 NMOS ring oscillator, forced PMOS ring oscillator, lector ring oscillator, forced stack ring oscillator. Simulations of these circuits show that as the value of V_{DD} increases the current across the circuit increases and as the value of current rise, the power of the ring oscillators shoot up. The power consumption of forced stack, lector, forced NMOS, forced PMOS, sleepy stack, forced 2 NMOS ring oscillators at 0.2V are 0.0216µW, 0.0348µW, 0.021µW, 0.044µW, 0.03µW, 0.129µW, 0.134µW.

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LIST OF ABBREVIATIONS

RO- RING OSCILLATOR

MOS- Metal Oxide Semiconductor

CMOS- Complementary Metal Oxide Semiconductor

MOSFET- Metal Oxide Semiconductor Field Effect Transistor

LSSR - Lector Stack State Retention Technique

LECTOR - Leakage Control Transistor

SOC- System on chip

PMOS- P channel Metal Oxide Semiconductor

NMOS- N channel Metal Oxide Semiconductor

PDP- Power Delay Product

CHAPTER 1

INTRODUCTION

Especially in the electronic and optical oscillator, the oscillatory behavior is ubiquitous. Oscillators are used for frequency translation of channel selection and information signal primarily for radio waves and simple wave communication systems. They are also available in a digital electronic system, which requires a time reference e.g. a clock signal, to synchronize operations. There is the availability of a diversity of oscillators but the operating principle, the frequency oscillation-band, and operating in a noisy circumtances vary from one stage to another [1, 2, 5].

Generally, the performance of the resting oscillator but not as good as the sinusoidal oscillator. However, the efforts done by researchers and scientists have improved the performance of the ring oscillator to determine the level of satisfaction that can be used effectively in communication systems [1, 2].

Designers must manage power consumption in complicated SOC and custom processors because they are critical components in embedded systems and other mobile devices, with 70% of customers requesting longer talk and standby times as major mobile features. The functionality, as well as the battery life, determine the quality/performance of these types of devices. There is a market demand for smaller batteries, which in turn influences the size of the gadget and must be reduced. The power utilization of a die is rising as the density of transistors in a die increases. There are two types of power consumption: dynamic power consumption and leakage power. When the circuit performs a function and the signals vary, dynamic power is consumed. Static power, also known as leakage, is spent continuously, even when the circuit is turned off. It is superfluous, and one would like to get rid of it. In mobile applications, power leakage is a major cause. As a result, multiple strategies are applied at the circuit and process levels to resolve this. To minimize overall power in high-performance nanoscale circuits, new low-power approaches are necessary. Lector, forced NMOS, forced 2 NMOS, sleepy stack, forced stack, and forced PMOS are examples of circuit approaches.

How much optimization can be done in managing the power consumed by devices determines how good a design analysis is. To reduce power consumption in the final product, it's critical to estimate power early on. Digital circuits must be understood, designed, and optimized for a variety of quality metrics such as power dissipation, cost, reliability, and performance (speed). At the gate level, redundancy can occur in a circuit. The current that passes through a transistor while it is turned off is known as leakage current. It fluctuates exponentially with a threshold voltage, temperature, and other parameters and is dependent on gate length and oxide thickness. The VLSI chip designer must fulfill the severe lemit on total power dissipation in portable electronics applications such as smartphones and tablets computers while still satisfying the computational requirements.

However, as wireless devices grow in importance in the user electronics distributes; a fundamental design fundamental for handy execution, namely the device's total power consumption, must be familiarized. Lowering the total power consumption in these systems is critical because it is intended to enlarge execution time while meeting minimum size, battery support, and battery weight criteria. As a result, when building SOC for portable devices, the most important issue to consider is 'low power design' [6].

1.1 Motivation

This research is entitled New Lower VLSI Logic and Memory Modes. While designing the power dissipation of the VLSI system is one of the major concerns. The dynamics of up to 3 times were one major concern; but as the size of the technology element shrinks static energy becomes an important issue as a dynamic force. The formerly popular method called the sleep transistor technique disconnects V_{dd} connections and/or Gnd transistors to save leak power consumption. However, when the transistors are allowed to float, the system may have to wait a long time to reliably recover the lost state and thus may be experiencing very poor performance. Therefore, maintenance is important for a system that needs a quick response even if it is inactive.

The total leakage capacity is chiefly due to sub-threshold leakage. In addition, leakage of gate-oxide is another factor that can affect the leakage capacity. A attainable result analyzed extensively is the possible use of high-k (high dielectric constant) gate insulators. Therefore, many ideas have been suggested to address the problem of energy leakage. With the continuous practice of technical measurements, leak power contributes

significantly to the total power consumption in CMOS circuits. V_{dd} balancing reduces power consumption but also reduces circuit performance. This can be compensated in part by lowering V_{th} but at the expense of increasing leakage capacity. Reducing the use of leak energy is currently a major research challenge. And the purpose of this thesis is to readdress the reduction of part of the sub-threshold leakage of static power consumption by the variable approachs used to date. The ambition of this thesis is to provide an overview of the latest method of achieving a significant reduction in leakage capacity in CMOS circuits.

The new approaches to make new ring oscillators are sleepy stack, forced NMOS, forced 2 NMOS, forced PMOS, lector ring oscillator LSSR (Lector Stack State Retention Technique) which are explained further.

1.2 Objective

The main purpose of this thesis is to provide new low-cost solutions for the creators of Very Large Scale Integration (VLSI). In particular, we focus on reducing leakage capacity. Although leakage capacity was not present at 0.18µ and above technology, in nanoscale technology, such as 0.07µ, the leakage capacity is approximately equal to the use of dynamic energy. In this thesis, the work aims to make a novel structure of the ring oscillators that use low-voltage, low-power for applications.

- Analyzing and discussing different inverters at 45 nm technology node and ring oscillators at different technology nodes. This will give us the idea about working of the inverter and RO and will help to improvise the advanced structure of RO. This will also benefit to find out the trend of RO using different technology nodes that, what will be the performance of RO.
- Performance analysis is done for advanced RO structures to find out which one gives the immense better performance. Compared and tabulated their results to conclude their working ability for low-power applications.
- Designing and analyzing the novel RO structures that ensembles the advanced inverter configurations, which help in selecting the best ring oscillator in terms of power consumption i.e which has a better performance.

1.3 Methodology:

The proposed ring oscillators are consist of advanced inverter configuration i.e. In this dissertation, the basic concept and basic ring oscillator and inverter structures have been described. Also, many new enhanced RO named “sleepy stack ring oscillator, forced NMOS ring oscillator, forced 2 NMOS ring oscillator, forced PMOS ring oscillator, lector ring oscillator, forced stack ring oscillator” and structure of these are detailed, and as it is notified that inverter’s accuracy plays a major part in the operation of RO. Hence, the best performance given the RO is used further. Furthermore, the various parameter of an inverter has been characterized and studied. An analysis of different advanced inverter configurations is also used to observe their performance on different V_{DD}. The basic CMOS RO structure of 5, 7, 9 stages are verified over different technologies including 45 nm, 32 nm, and 22 nm. Another different advanced ring oscillator has been simulated at 45 nm CMOS technology which helps in detecting the best ring oscillator according to the power consumption.

1.4 Organization of Thesis:

This thesis has been standerdized into 7 chapters. The introduction of ring oscillator, the inverter is categorized in Chapter 1. Further, Chapter 1 includes the motivation, objective, and methodology. Chapter 2 is related to the literature review and the technology gap. Chapter 3 explains the performance parameter extraction for inverter Chapter 4 deals with a discussion and analysis of different types of inverter topologies and their parameters. Chapter 5 presents frequency analysis of different stages ring oscillators at different technology nodes. Chapter 6 illustrates the proposed ring oscillator design based on the advanced inverter configuration, its study, and analysis. Conclusion and future scope are presented in Chapter 7.

- CHAPTER 1- Includes a brief introduction about ring oscillator, inverter, their application fields, how they work on low power and low voltage. Objective, motivation, methodology, and organization report are described in this chapter.

- CHAPTER 2- This chapter described the previously done research work on Ring Oscillator and Inverter. Different kind of inverter topologies has been addressed in the literature. Different kinds of techniques and devices have been used in the

inverter to improvise the performance of the inverter such as low power dissipation at different voltages, low delay values, lower phase noise, etc.

- CHAPTER 3- This chapter explains the performance parameter extraction for inverter i.e. power dissipation in CMOS circuits, delay in CMOS circuits, switching threshold voltage of the inverter and noise margin, and basics of the ring oscillator.

- CHAPTER 4- This chapter explains the five types of inverter, their working, and parameters (Power dissipation in CMOS circuits, delay, switching threshold voltage of the inverter, and noise margin). All five inverters were analyzed at 45 nm technology. Then their parameters have been compared based on their parameters and structures.

- CHAPTER 5- Description and parametric analysis of CMOS ring oscillator i.e. are done in this chapter. The frequency analysis is done concerning the V_{DD} which is obtained from a particular period.

- CHAPTER 6- The proposed design of advanced ring oscillators i.e. sleepy stack ring oscillator, forced NMOS ring oscillator, forced 2 NMOS ring oscillator, forced PMOS ring oscillator, lector ring oscillator, forced stack ring oscillator are illustrated in this chapter. This chapter includes the structure description, it's working, and also previously reported RO based on some low power technologies are compared with the proposed design to capture the superior performance of the proposed designed RO.

- CHAPTER 7- The conclusion and future scope of the proposed RO is written in this chapter.

In the last, publication list is mentioned and references are listed which provided the broad idea and concept of the current mirror and current comparator.

CHAPTER 2

LITERATURE REVIEW

2.1 Previous Reported Work

S. Suman, M. Bhardwaj and B.P. Singh [1] introduces a new approach to the development frequency operation of the CMOS ring oscillator. Postulated on the summation of MOS transistor to increase fipping speed oscillator delay cell. The method that can be used simply too is a different oscillator and provides an easy way to get started tuning the frequencies without the introduction of any additional category noise. Using 0.35 m CMOS technology, the simulation outcomes show that implementing the procedure to a simple ring oscillator grants an improvement of frequency oscillation by 80%. And, its impersonation shows that the improvement in frequency can be up to 300% if the process is associated with positive feedback.

S. Kumar and G. Kaur [2] examined previously the scheming and accomplishment of the nine-stage ring oscillator using 45nm technology were done in which the noise, delay glitches are examined and abolished. This paper shows that the line is more favorable confines using a ring oscillator ring controlled by various CMOS can be reached. Simulation results show that the come up oscillator can work at a very high-level oscillation frequency compared to a normal ring oscillator. In addition, the proposed schemes offer simplicity in how to use frequency tuning without the introduction of any additional category sound. Also explained the maximum allowable voltage employed to the circuit confines the speed of a given oscillator. Secondly, a small number of inverters have been used to generate rings as a result of the high frequency of oscillation. A CMOS inverter incorporated a PMOS transistor attached at the drain terminal whereas an NMOS transistor is connected with the gate terminal. The VDD supply voltage and ground are adjoined to the source terminal of PMOS and NMOS transistors respectively.

S. Khan [4] took notice of the situation. Of particular unease in the construction of low-power projects are energy consumption and design alterability. Energy losses, delays, and space can be reduced with the help of measuring technology. In this paper, the CMOS Inverter is introduced with very low power dispersion obtained by measurement of electrical power and sizes of transistors. This inverter is built with 180nm Tsmc CMOS

technology with a powerful 1V supply and simulation is made with the PSpice tool. The power consumption of this CMOS Inverter is 7.25 picowatt. The effect of the supply voltage scaling and transistor size scaling on power dissipation and the delay is investigated. With the scaling of supply power and transistor size, both decrease.

V. Sikarwar, N. Yadav, and S. Akashe [5] noticed that the power expenditure is reduced in the nine-stage ring oscillator. The phase noise, power consumption, and other parameters are calculated for the ring oscillator. That paper also explained that oscillatory signals can also be utilized in radio and communication systems. Electronic oscillators are manufactured to produce these signals. Linear/harmonic and nonlinear/relaxation are the two main categories of oscillators.

A. K. Mahato [6] explained the concept of a CMOS thyristor used to operate a low frequency ring oscillator using 2.5-volt power supply and 1pF loading power using 250nm technology. In addition to this static power dissipation CMOS ring oscillator has been further developed for CMOS thyristor-based ring oscillator.

S. Chauhan, R. Mehra [7] analyzed CMOS design and analyse the ring oscillator is made up of 5 stages, Stage 7 and Stage 9 use the cadence virtuoso tool on 45nm technology. At the exit of all stages of the ring oscillator, 500aF capacitor and in charge, a 5fF capacitor is used for different phases. Energy consumption was reduced by 79% in the 5 stages of the ring oscillator compared to the 9-stage ring oscillator.

M.K. Mandal and Sarkar [14] explained that an oscillator is a device that operates without any external signal and gives an output that is continuous means repeated pattern like alternating waveform. The unidirectional current likewise the D.C signal is transformed into the A.C signal have a need of frequency by the oscillators, moreover, the production depends upon components of circuits. Frequency oscillation expression of a complimentary oxide semiconductor (CMOS) cell-based RO-based delays is introduced and the delay in the dispersion of the delay phases is calculated. Normal RO limits have been tested and a few ways to overcome these limitations have been identified. In this context, some of the modified properties of ring oscillators such as sound sources in the production of ring oscillators have also become studied. Other potential applications of the ring oscillator based on its tuning power features and output of multiple phases are also mentioned.

S. Kusuma and P. Kumar [16] compared the 3 and 9 stage ring oscillators at 45nm and 22nm using the Tanner EDA tool. After all, one of the utmost broadly used integrated circuits is the ring oscillator, which is a built-in device with a weird number of stages of the inverter delay united to a closed-loop with a negative response, the output of which oscillates between the two voltage levels, depicting TRUE and FALSE. Although the developers use ring oscillators in all semiconductor waffles for monitoring gate delays and high-speed power inverter products made in MOS, but widely used in the construction of PLL, Signal.Generators. In this paper, the 3 and 9 phase CMOS Ring oscillators are operated using the Tanner EDA with PTM22nm technology to compare 45nm and 22nm similar designs. As a result of the increased demand for the smaller devices and the use of ring oscillators at various larger technology nodes, a lot of effort is being put into developing circuits that operate at lower supply.

A. Tah and D. K. Rakshit [17] set out a specific method for designing a frequency oscillator ring. We too bring a comparative diagosis of ring oscillators and try to find a way to link their frequency characteristics with environmental resistance and strength. The formula found here is much simpler compared to all the others available. In addition, allows for a faster, more accurate composition of the frequency. Also, a detailed analysis of CMOS and DTMOS based design has been created and the parameter has been designed to determine the efficiency of both CMOS and DTMOS. The simulation platform used here is by LTSpice IV and the models used are based on CMOS technology BSIM4.0 54.

R. P. Rao [19] studied the CMOS inverter and discovered that as the Vdd and load capacitance increases, the power obtained increases as well i.e “Leakage power can be minimized by having higher geometries of transistors and higher values of power supply”. From the analysis done the work can be concluded by- “Large amount of load power, high transistor geometry and high values of the voltage of the power supply affects all the power of a CMOS inverter "," Increased power consumption shortens circuit capacity ”and“ Leakage capacity can be reduced by having high transistor geometry and high numbers of Power supply ". CMOS performance analysis of the inverter helps to understand energy sources to disperse.

The proposed methods were compared to existing leakage reduction strategies by P. Saini and R. Mehra [20]. In the past many ways were proposed to reduce leakage capacity such

as a forced, drowsy stack, sleep retainer, double sleep method, etc. using similar approaches transistor sizing, multi-Vth, dual-Vth, transistors stacking, etc. In this paper, new ways of saying are suggested reduction of leakage power in 90nm technology. Coming up approaches will be compared to previous leaks mitigation strategies. The effect is pretended using Microwind.3.1 on CMOS technology of 90nm at room temperature.

A. Agarwal and S. Sharma [21] are four found Sleepy CMOS-Sleepy Stack (SCSS) Technique provides excellent results of reduced distribution delays, static power losses, and medium power compared to Dynamic Threshold CMOS Technique (DTMOS), SCCMOS - Super Cut-of CMOS Technology, Sleep Method, CMOS Technique General (CCT), Transistor Stacking Technique, Sleepy Keeper Technique, Multi Threshold CMOS Technique, and Variable Threshold CMOS Technique (VTMOS). S. Sharma, R. Devasia, and G. Sharma have offered a comparative examination of all three logic methods [22].

A. N. Adwani, H. V. Chopade, S. S. Jain [23] discussed various energy reduction strategies for various stages of CMOS design such as Dynamic Power Suppression, Adiabatic Circuits, Logic Design for Low Power, Reducing Glitches, Logic Level Power Optimization, Standby Mode Leakage Suppression, Variable Body Biasing, Sleep Transistors, Dynamic Threshold MOS, Short Circuit Power Suppression.

V. H. Rane, A.J. Patil, and R. R. Karhe [24] use basic CMOS gates and compares a simple circuit to a proposed new circuit with a lector mode in which the p-type and the n-type leakage control transistor (LCT) are infused in the midst of the drag and drop network.

Various Low Power Digital design Techniques were compared and performance analyzed by F. Buch, A. Bhardwaj, S. Gupta, and G. Sharma [28]. They compared various low-power digital design techniques are performed in terms of various design metrics. As the stationary power ceased one of the main problems in the sub-nanometer system in particular less than 65 nm on CMOS where it contributes about 80 percent of total power destruction. Novel packing techniques are used at 0.13µm to overcome static power dissipation such as and improve the qualification rate. Same packing techniques are also used in low technology such as 45nm as well the effect of force, the delay is measured by the change in width as and a technical node. The results are compared to the basis of the qualifying figure. Comparing other novel techniques used in the 1-bit full adder circuit are available GDI where GDI is used as a multiplexer to use 1-bit. A full adder is also

introduced. Average for all strategies are made based on design metrics. The youth of this function is that comparisons are made between the various strategies will be a very useful tool for efficiency app capabilities for specific digital circuits.

The study by S. Gaonkar [30] examines the reduction of the CMOS circuit led to increasing leakage of sub-threshold current by decreasing threshold voltage. LECTOR is a way of reducing the value leakage dispute in CMOS circuits, including two additional leaks, controlling the transistors, self-regulating, on the way from supply to the ground which provides additional resistance that will be reducing the problem of current leakage in the CMOS cycle and also demonstrated that the leakage current in basic CMOS Inverter utilizing LECTOR methodology with Cadence-45nm technology.

The work by D. V. R. Raju [31] examines several low-leakage power design strategies for reducing power consumption. Leaking power plays an decisive role right now in CMOS technology. The size of the feature decreases leakage of power also increased. Power dispersal becomes important considered as working and local chip design in the modern VLSI industry. International Technology Roadmap for Semiconductors (ITRS) predicts what is below threshold leaks power dissipation may control the dissipation of dynamic energy. There are two types of internal waste disposal CMOS technologies are static Dispersion and Elimination of Powerful Power. This paper is very focused on static a waste of energy, in which especially in reward power. This paper updates various subcategories of leak power design strategies to achieve low power dissipation.

L. Kumre, B. P. Shrivastava, N. Rai [32] in 45nm technology, a comparative examination of CMOS inverter for low leakage power has been presented and In this paper, a comparative analysis of the inverter circuit has been being made using the standard CMOS method to make a sleeping stack technology. Some inverter techniques are forced by NMOS, forced PMOS, 2 compulsive NMOS 2, and stack method also updated. Schematic circuit design and Layout design of an inverter that uses all the techniques are made in the DSCH as well MICRO WIND tool. Energy consumption and space consumption are listed in all strategies. It ends with the power dissipation in the path of the sleeping stack being as small as compared to other strategies but the area is increasing as a result of an additional number of transistor calculations. Loss of energy in the sleep stack method is 47.6% lower compared to normal CMOS. The results suggest that the sleepy stack technique consumes

52% less power than the regular CMOS technology [16]. M. Saad and S. Mangesh [34] introduce a renewed inverter conversion method known as reducing swing by forcing 2n mos. The proposed (RSFM) reduces swing with Forced 2nmos uses your location both to reduce switches and nmos inverters. It, therefore, offers lower power dissipation correlated to other inverter approaches. It uses the stack strategy to change the current using mos devices by changing the W / L of mos devices. However, a reduction fee on the power is remitted by the increased delay and the location of the building.

S. H. Kim and V. J. Mooney [38] have proposed a novel approach, called a "sleeper keeper," which reduces current leaks while maintaining a more accurate sense of humor. The sleeper uses estabilished sleep transistors and two additional transistors - driven by a pre-calculated gate exit - to save status through sleep mode. Dual Vth values can be pertained to the sleeper to dramatically reduce current leakage below the subthreshold. In short, as a sleep deprivation method, the sleep retainer gains a reduction in the leakage capacity equal to sleep patterns and zigzag but with the benefit of maintaining a positive state of mind (rather than spoiling the logical state of sleep mode). Based on 4-bit add-circuit tests, the sleeper mode reaches up to 49% delay and 49% less than the sleep stack method. Dreadfully, the sleeper details more dynamic energy consumption, about 15% more than base case (no sleep transistors are used at all).

N. Bako and A. Baric [42] explained The synchronization function is required in digitally operated electronic systems and this condition is fulfilled by using oscillating signal produced by oscillators as a clock signal.

G. Bansal [43] explained, First of all, the applied voltage can be increased which consequently increment the oscillation's frequency and consumption of the current.

F. Khatoon [44] explained that the ring oscillator is advantageous in form of covering minute space, having high speed, and easily designable along with integrated circuit technology (IC). At the low voltage, the oscillations are generated by the ring oscillator, and low power is dissipated to produce high-frequency oscillations. It can be electrically tuned and an immense tuning range is provided. Because of their simplistic structure, the multiphase outputs are provided.

H. Masten [45] explained that to produce the specific output, the system is comprised of a particular number of stages, which otherwise cannot be attained through by the usage of

an even number of stages. In this circuit, sustainable CMOS inverter stages having 'T' delay are used in ring oscillators, and provide the oscillation frequency as F= (1) in comparison to LC & RC oscillators, Wien bridge oscillator, the ring oscillators proved to be the closely packed device. The supply voltage is separated from 0.075V to 1.2V to test the frequency and power consumption of the region. The estimated frequency was 19.7MHz to 15.3GHz and power consumption varies from 0.338uW to 54.0mW. As expected, frequency and intensity consumption increases with increasing power provide. To measure the voltage and temperature on a chip the application of ring oscillator is used. The ring oscillators prove to be useful in hardware irregular number generators. The jitter of the ring oscillator in the hardware irregular number generator is commonly used.

Michal [46] explained that In case when the even number of inverters are connected for designing the ring oscillators, the output attained at the last stage is similar to that of the initial stage input, so it is not feasible to design the oscillator with an even number of stages. There are two frequent methods used for prompting the oscillation's frequency.

Nayak [47] explained that ring oscillator is used as a part of PLL for clock and data recovery, clock synchronization, and frequency synthesis. A ring oscillator has digital as well as analog features which make them functional for data conversion tasks such as phase and phase width modulation. It is used in biomedical circuits and systems, Radio frequency identification tags in addition to wireless sensor cable networks. An in-ring oscillator CMOS inverter is used. The function of the inverter is the computation of its input to the logical NOT and it is analyzed that when inverters are connected in odd numbers then the last obtained output is the same as the output of the initial inverter. The period remains finite between the period when the introductory input is asserted and the ultimate output is obtained, in addition to this oscillations are caused when a part of the final output signal is fed back to the input signal.

A. Shivhare and M. K.Gupta [49] explained that a ring oscillator is a device comprised of an odd number of NOT gates, the gates midway their outputs two different voltage levels represent logic 1 and logic 0. The NOT gates or inverters are coapted in a series and the last inverter's output is observed from the initial gate. There is no difference between sole ended ring oscillator and the digital oscillator, produce by a tumble of odd, n number of CMOS inverters in a ring. It was concluded that the proposed oscillator ring performs better performance during power consumption and the low power output is approximately

3.476µw thus reducing by 54.64% in 1v and 28.40% in 0.9v. therefore, this approach provides an handily way to control central power and leakage power for regional designers. It also describes the design of the low power CMOS ring oscillator is proposed and analyzed for power consumption. In the proposed cycle, reduced power consumption is achieved and combined with low power consumption to help deploy the region on mobile devices, the Ring oscillator is the best choice in a cheap digital system.

2.2 Technical Gap

After observing and analyzing all the reported work, there is a technical gap. Many low power technologies are used in inverters to lower the power consumption or better the performance of the inverter like lector, forced stack, sleepy stack, forced NMOS, forced PMOS, forced 2 NMOS, and many more but these technologies are not utilized in ring oscillator circuit, so to improvise the performance of RO circuit this thesis analyzed and designed the novel ring oscillator circuit to lower the power consumption of the circuit.

Keeping in view all these issues, this thesis proposed a ring oscillator structure with previously reported advanced inverter structures whose performance is well analyzed and discussed. These proposed ring oscillators show very low power consumption as the V_{DD} increases.

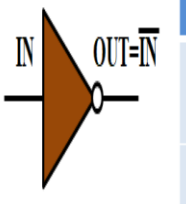
CHAPTER 3

INVERTER AND RING OSCILLATOR

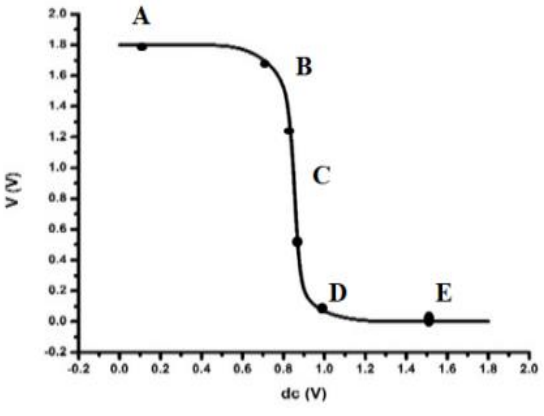
3.1 Inverter

This chapter will describe the basic elements of the RO i.e. inverter. As shown in Fig. 3.1 (c), an inverter is made up of PMOS and NMOS coupled by a gate with an output delay element. When the input is high, NMOS is activated and PMOS gets OFF. An inverter's inverted output is low because the NMOS transistor's source is connected to the ground. Similarly, when a low input is used, a high output is obtained which is depicted in Fig. 3.1. (a) [2- 5, 21, 22]. All three bias states are used by CMOS transistors: OFF-state, saturated-state,and the linear state (ohmic, non-satured). The CMOS inverter has two networks: pull-up network and pull-down network. In a pull-up network, the PMOS i used as a load while the NMOS is used as a pull-down network [4, 6, 15, 27, 33]

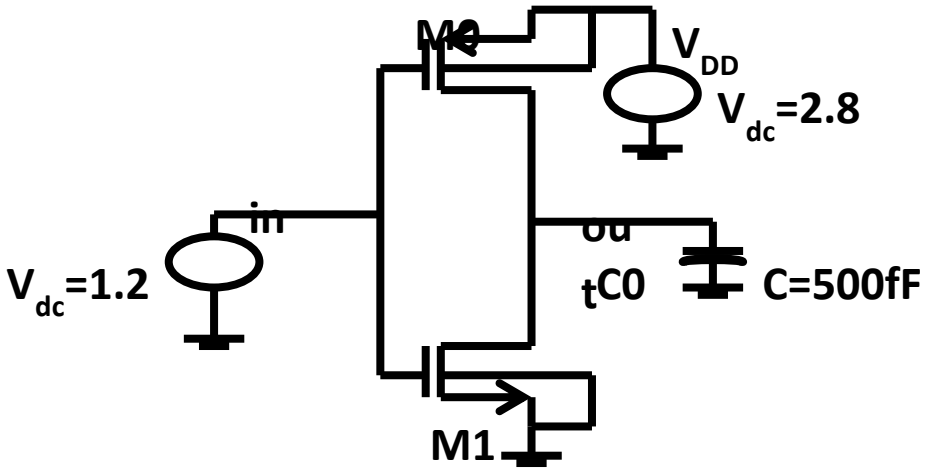
The output of the PMOS and NMOS is obtained at the drain, and the input is delivered at the gate terminal of both devices, as shown in Fig 3.1 (c). To acquire the voltage transfer characteristics displayed in Fig. 3.1. (b)., certain steps are followed. The circuit is needed to be supplied by a 1.2 V supply and features 1u and 3u NMOS and PMOS widths, as well as a 500fF capacitor at the output of the inverter circuit [7-11, 14].



IN	OUT	V_{IN}	V_{OUT}
0	1	V_L	V_H
1	0	V_H	V_L



(a) (b)



(c)

Fig. 3.1. (a) Inverter: symbol and truth table (b) Inverter's Voltage Transfer Characteristics (c) Circuit of CMOS Inverter

The voltage transfer characteristics of the inverter depict the region of operation of the inverter: at point A, NMOS is in cut-off and PMOS is linear, at point B NMOS is in saturation and PMOS is in linear, and at point C both transistors are saturated. At point D, NMOS depicts to be in linear and PMOS gets saturated and at E, NMOS is in linear as showed in above figure and PMOS is in the cut-off region.V_L and V_H are two voltages that represent logic signals 0 and 1.

The operating principle states that for small values of input voltage, $V_{IN,}$ the NMOS is off, PMOS is on, and the output mode is connected to V_{DD} and when the input voltage is high, $V_{IN,}$ the NMOS is on, PMOS is off, and the output mode is connected to the ground.

3.2 Performance Parameter Extraction For Inverter

3.2.1 Power Dissipation in CMOS Circuits

The temperature rise of the chip is caused by the power dissipation. Whatever the state of the device either on or off, it is affected by the temperature rise. So, to reduce the dissipation of power, a low power design methodology is used. The main sources of dissipation of power are:

Static Power Dissipation (P_S): Its occurrence is found when the device is in standby mode. The current effect of state intensity and strength is 0 as the current DC path exists from V_{DD} to GND. The static power dissipation is due to:

Sub-threshold Current: It exists at gate voltage below threshold voltage and it arises from the charges of inversion.

Reverse-biased Diode Leakage: Parasitic diodes have the reverse bias current. The static power dissipation is expressed as:

$$P_S = I_{leakage} * V_{DD} \quad (1)$$

Where P_s is static power dissipation, $I_{leakage}$ is a leaking power now, V_{DD} is a power dissipation force.

Gate-induced drain leakage: Leakage to the substrate caused by a solid field impact on the reduced compact area of MOS transistors is known as a door that is designed to eliminate leakage power. When the NMOS is reduced to one side to the supply voltage (V_{DD}) and the door is to one side to zero or negative voltage, a terminal area is established under the door, and a reduced cover circuit is formed. Because of torrential slide augmentation, this creates noticeable band bowing in the deplete allowing electron gap combine era. As the holes are swiftly emptied to the substrate, a deep fatigue situation is created. Meanwhile, the depletion collects electrons, leading to Gate Induced Drain Leakage current [4, 5].

Dynamic Power Consumption (P_D): Causes charging and discharge of load capacity. During the one cycle of completion, current flow from V_{DD} to the load capacitance to charge and then flow from the charged load to GND at the time of discharge.

$$P_D = \alpha\, C_L {V_{DD}}^2 f_{CLK} \quad (2)$$

Where P_D is a dynamic power dissipation, α is an activity factor, C_L is load capacitance, V_{DD} is a power supply, f_{CLK} is a clock frequency [3].

Short Circuit Power Dissipation (P_{SC}): It occurs when both PMOS and NMOS transistors are ON for short time during the input between V_{tn} and V_{DD} -$|V_{tp}|$. The short-term current results from a short circuit path between V_{DD} and GND, which causes the incrimination in power dissipation of about 10 percent. The total power dissipation is expressed as [3].

$$P_{Total} = P_S + P_D + P_{SC} \quad (3)$$

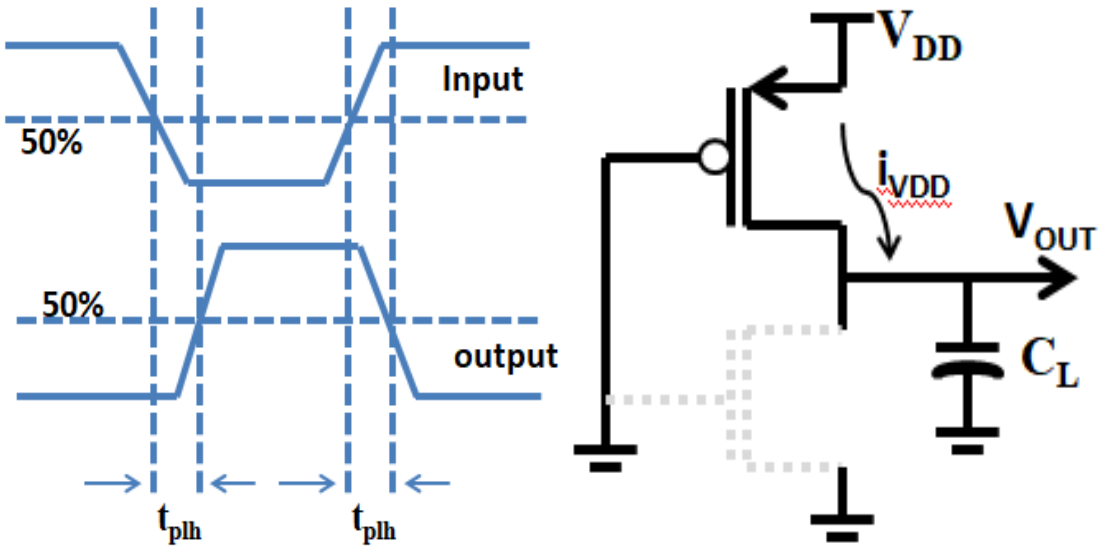
The square of th**e** supply voltage is directly proportional to the power dissipation. When the supply voltage is reduced, the device's power consumption is reduced, but the

device's performance in terms of speed is influenced. The threshold voltage is decreased to compensate for the delay. However, because of the decreased threshold voltage, leakage current increases. Reduced power consumption because of the availability of big packages and various cooling solutions capable of dissipating the generated heat, power consumption has not been a major concern. Continuously rising chip density and system size, on the other hand, may make it difficult to supply proper cooling, resulting in either a major cost increase or a limit on the amount of functionality that can be given. Another element driving the demand for low-power CPUs is the growing market for battery-powered portable consumer electronics [1, 8, 9]. Low-power consumption is a major challenge for these high-performance portable digital devices that run on batteries, such as laptops, mobile phones, and personal digital assistants (PDAs) because it has a direct impact on performance by reducing battery life. As a result, low-power VLSI design has become a very busy and quickly evolving discipline [3].

3.2.2 Delay in CMOS Circuits

The length of time between the input signal is 50% VDD and the output signal is 50% VDD is known as the distribution delay, and is divided into two parts: low-to-high transition delays and high-to-low transition delays. Distribution delays can be calculated using the formula below:

$$\tau_{pd} = \frac{\tau_{PLH}+\tau_{PHL}}{2} \quad (4)$$



(a) (b)

Fig.3.2 (a) Transition delay for low to high and high to low (b) Equivalent circuit of first-order load capacitance during charging.

Where τ_{PLH} denotes low-to-high transition delay and τ_{PHL} signifies the high-to-low transition delay. The existence of the inverter's load capacitances causes the propagation delay [22, 23]. The corresponding first-order circuit for the charging process of load capacitance is given in Fig.3.2 (b). It is easy to determine the charging time of the load capacitance when the input signal is a step signal using the first order circuit analysis method [31-35]. The discharge time is τ_{PLH} to as

$$\tau_{PLH} = \ln(2)\, R_{eqp} C_L = 0.69 R_{eqp} C_L \quad (5)$$

Where R_{eqp} denotes the PMOS equivalent resistance. τ_{PHL} has the same derivation as that of τ_{PLH}, hence, the propagation delay is given by formula 6.

$$\tau_{pd} = 0.69 C_L \frac{R_{eqp}+R_{eqp}}{2} \quad (6)$$

PDP is a basic metrics that are widely used to measure the quality and performance of the CMOS process. It is defined as a power output and a deal and indicates the amount of power required for each switching event [35, 38].

3.2.3 Switching Threshold Voltage of the Inverter

Value of Switching threshold = point on Voltage Transfer Characteristics where $V_{out} = V_{in}$ is also known as inverter's midpoint voltage, here $V_{in} = V_{out} = V_M$ [4, 7]. Because both the transistors are in saturation at V_M, and $I_{Dn} = I_{Dp}$ for an inverter, the V_M must be calculated.

$$\frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GSn} - V_{tn})^2 = \frac{\beta_n}{2}(V_{GSn} - V_{tn})^2 = \frac{\beta_p}{2}(V_{GSn} - V_{tn})^2 = I_{Dp}) \quad (7)$$

$$\frac{\beta_n}{2}(V_M - V_{tn})^2 = \frac{\beta_p}{2}\left(V_{DD} - V_M - |V_{tp}|\right)^2 \quad (8)$$

$$\frac{\sqrt{\beta_n}}{\sqrt{\beta_P}}(V_M - V_{tn}) = V_{DD} - V_M - |V_{tp}| \quad (9)$$

$$V_M = \frac{V_{DD} - |V_{tp}| + V_{tn}\frac{\sqrt{\beta_n}}{\sqrt{\beta_P}}}{1+\frac{\sqrt{\beta_n}}{\sqrt{\beta_P}}} \quad (10)$$

3.2.4 Noise Margin

Noise Margin: NM is a parameter that is connected to the input-output characteristics. It defines the maximum noise voltage that can be applied to the input without affecting the

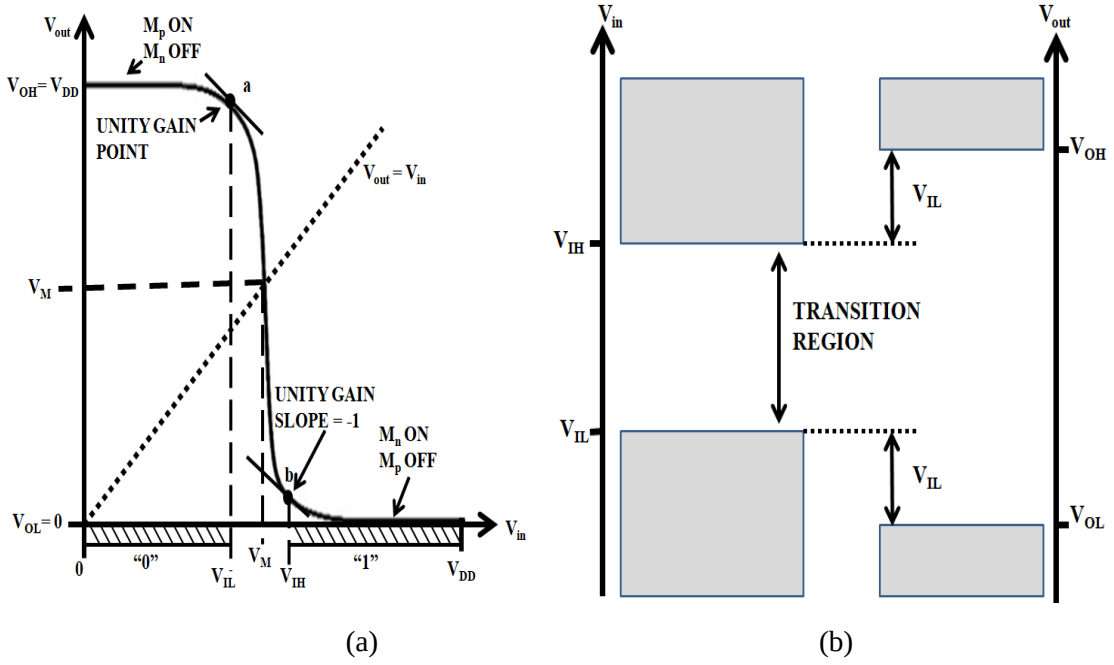
output. We will define it in terms of two factors: LOW noise margin and HIGH noise margin [19, 35, 36].

LOW noise margin: the magnitude difference between the driving gate's maximum Low output voltage and the driven's gate maximum input voltage acknowledged.

$$NM_L = |V_{IL} - V_{OL}| \quad (11)$$

HIGH noise margin: It is the magnitude difference between the driving gate's minimum high output voltage and the minimum input voltage [22, 24, 39, 40].

$$NM_H = |V_{OH} - V_{IH}| \quad (12)$$



(a) (b)

Fig. 3.3 (a) Noise Margin For CMOS Inverter (b) Definition of NM_L and NM_H (shaded region indicate high and low levels for input and output signals)

3.3 Ring Oscillator

The role of the ring oscillator in the electronics industry cannot be overstated. The ring oscillator is an important component of the electronic device. The importance of Ring Oscillator has increased with the developments in the VLSI field. A ring Oscillator is a closed loop that contains an unequal number of parallel inverters that form a response circuit as shown in Fig 3.4. In the low-cost digital CMOS process, it becomes a better choice [2, 7].

The concept of a ring oscillator with a delay stages chain has sparked a lot of interest because of its many useful attributes. These attributes incorporate oscillations that can be accomplished at low voltage; designing can be easily done using integrated circuit technology (Bi-CMOS, CMOS). It is possible to adjust it electronically. Because of their basic structure, multiphase outputs are provided with a high frequency of oscillation while dissipating low power [9-14][16][18][37].

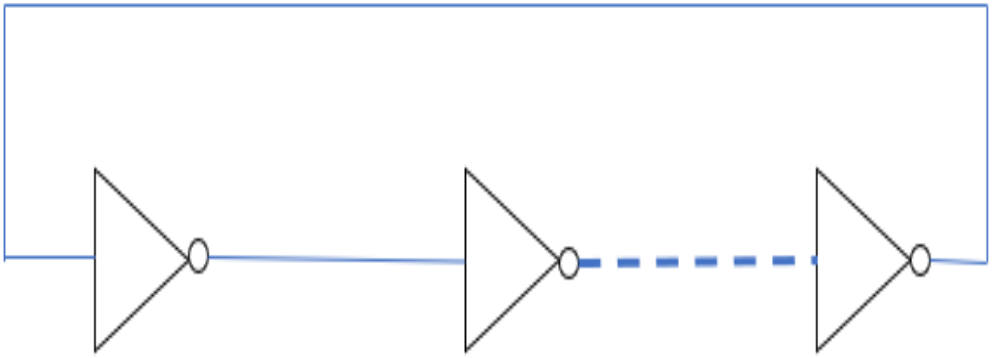


Fig. 3.4 Structure of Ring Oscillator

A ring oscillator with an even number of circular transistors cannot be used, as the outcome of the inverter is the same as the input. The ring oscillator with multi-stage numbers can be used as a basic SRAM module and is considered part of memory [14, 16].

CHAPTER 4

ANALYSIS OF DIFFERENT INVERTER TOPOLOGIES

4.1 Inverter

As Ring Oscillator is consists of inverters, generally an inverter is comprised of PMOS and NMOS connected through the gate with output delay element as shown in Fig 4.1 (a). When the input is high, NMOS gets ON and PMOS gets OFF. The inverted output provided by the inverter i.e. low as the source of the NMOS transistor is connected to the ground. Similarly, high output is obtained when low input is applied [1, 4, 8]. Fig 4.1 (a) shows the inverter circuit in which the output is obtained at the drain of the PMOS and NMOS device and input is given at the gate terminal of both devices. To obtain the voltage transfer characteristics presented in Fig 3.1 (b). The circuit is powered by a 1.2 V supply, with NMOS and PMOS widths of 2u and 5u, respectively, and a 500F capacitor at the output.

Logic signals 0 and 1 are represented as two voltages V_L and V_H

4.1.1 Inverter using Lector Technique

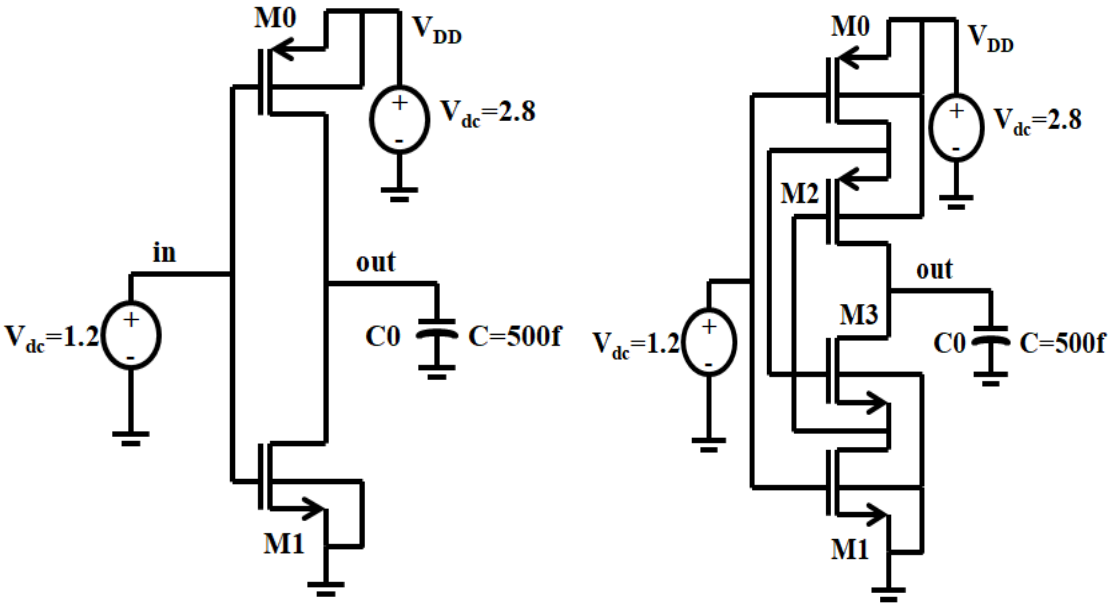
Leakage control transistors (LCTs) are two additional transistors used by LECTOR. Within the logic circuit, these two transistors are put between PUN and PDN, as shown in Fig. 4.1 (b). The transistors in LCTs are coupled in such a way that they are always near the cutoff voltage [8-10]. LCTs improve the resistance of the path from the supply to the ground, resulting in significant leakage reduction [12]. The advantages of the lector method are that it does not require any additional control and observation hardware, thus constraining range expansion and power dissipation in a dynamic state when compared to other systems and it does not influence dynamic power, which is a significant constraint with other leakage reduction methodologies, is also investigated in this thesis [13, 14, 16, 18, 21]. The main idea of working in a student program while studying previous generals we found a common point about the student approach that, is the best way to calculate the amount of leakage power compared to other methods. In line with this, another advantage of the LECTOR strategy is that it does not affect the flexible power of large limits and other leakage reduction strategies [41, 43, 48].

4.1.2 Inverter using Forced nmos approach

This method is similar to traditional CMOS, but with the addition of an NMOS at the bottom. Because the two NMOS devices increment the delay, the circuit's leakage power is reduced. When compared to traditional CMOS, an additional NMOS reduces $I_{leakage}$ through the MOS device, resulting in lower power consumption [6, 15, 16, 18, 25]. The forced NMOS transistor inverter is depicted in Fig. 4.1. (c).

4.1.3 Inverter using Forced 2 nmos approach

This method combines the advantages of both reduced swing as well forced NMOS inverters. Because $V_{gs} = V_{ds}$, the load PMOS transistor in decreased swing inverter is always saturated. When a rotating clock signal reaches its maximum voltage, it lowers the voltage at the source of the second PMOS in each converter to approximately Vdd-Vtp, thus shutting it down [8, 9].This method uses less power but has a longer delay and a larger pattern area. The output voltage fluctuates between 0 to V_{dd} - V_{tp}. Because PMOS functions as a load, the voltage swing is reduced to V_{dd} - V_{tp}. This depletion in swing leads to a reduction in power usage [5, 6, 12]. The inverter adopting forced 2 NMOS techniques is indicated in Fig. 4.1. (d). This strategy allows the designer to use less power but at the cost of long delay and pattern area [16, 18, 21, 26][50-52].



(a) (b)

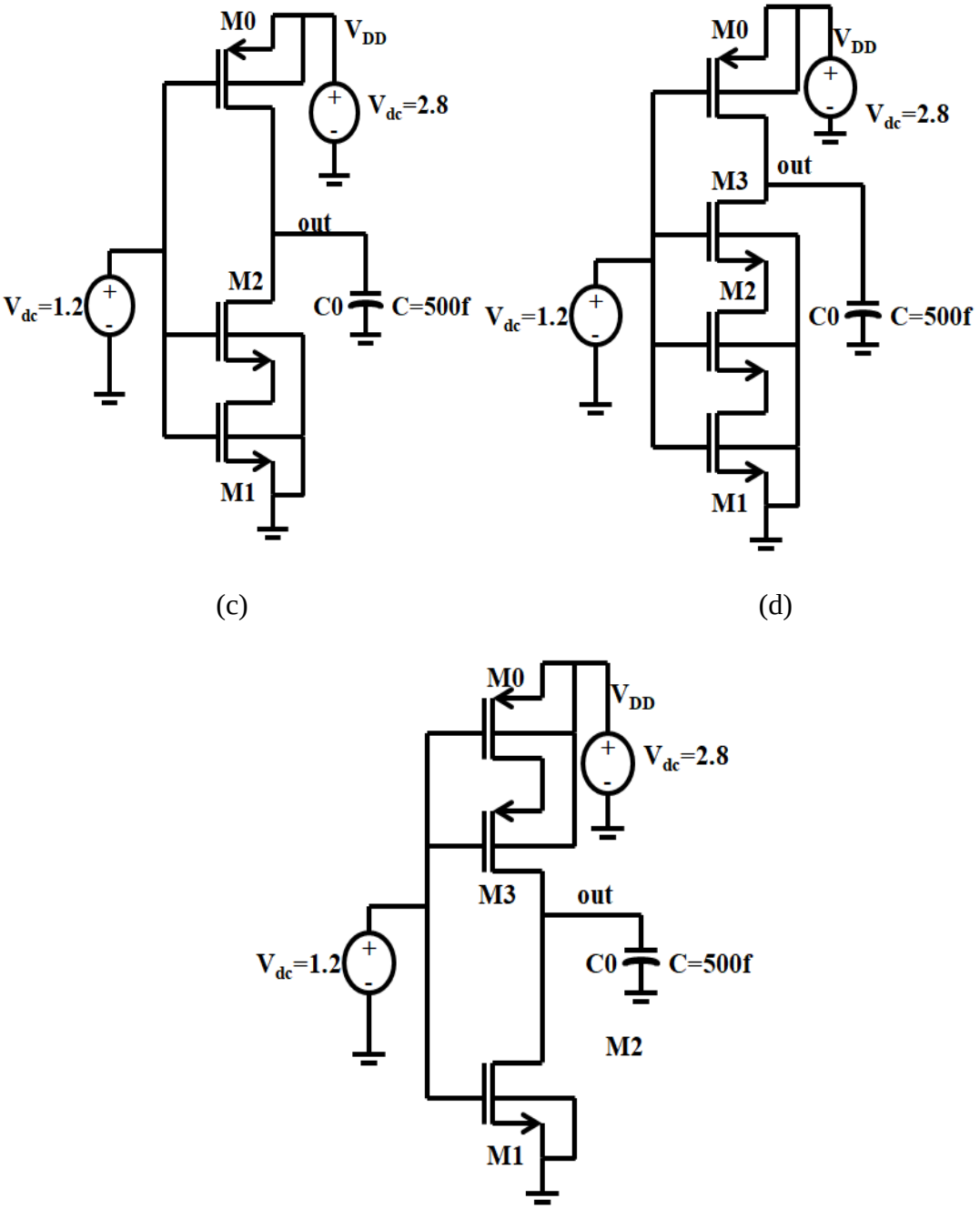


Fig. 4.1. Circuit schematics of (a) CMOS inverter (b) Inverter using Lector technique (c) Inverter using forced NMOS methodology (d) Inverter using forced 2 NMOS strategy (e) Inverter using forced PMOS technique.

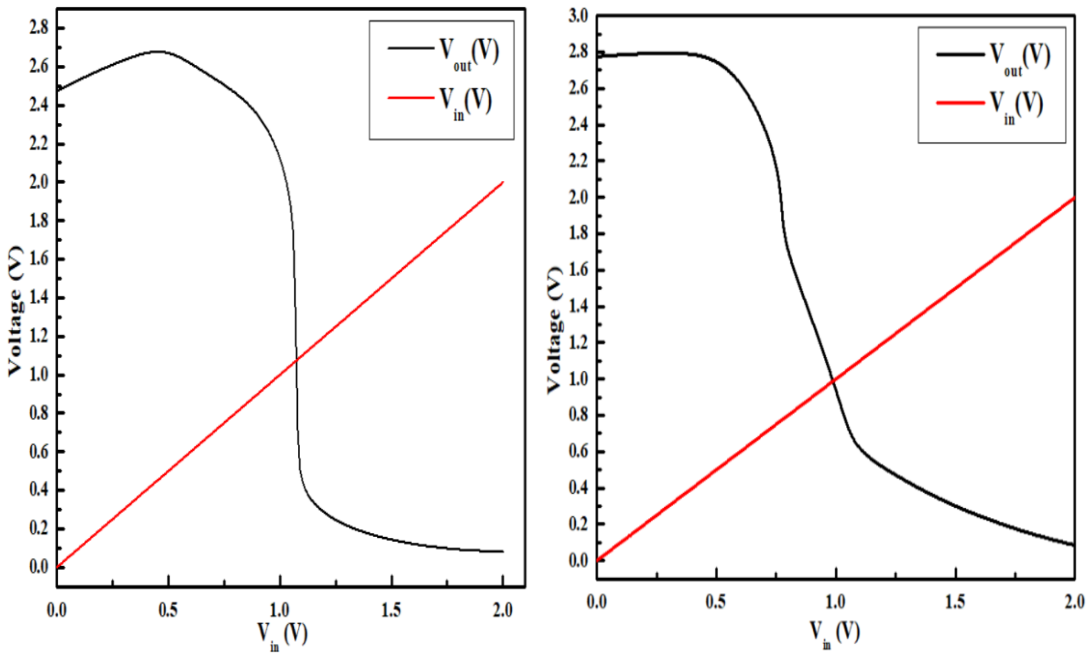
4.1.4 Inverter using Forced pmos approach

The circuit is made up of two PMOS and one NMOS in this method. In other words, it can be seen as a regular CMOS with the addition of a PMOS at the top. The delay is increased

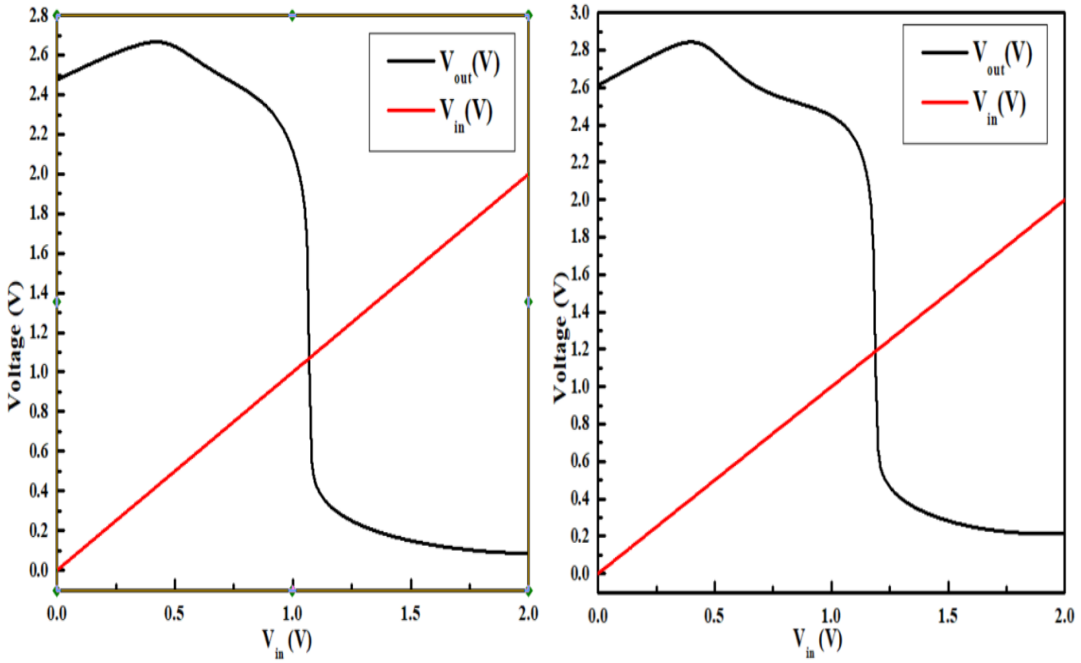
by the addition of two PMOS devices, lowering leakage power in the circuit. Fig. 4.1. (e) depicts the forced NMOS method [15, 16, 18, 27, 28].

The design of different types of inverters is simulated using CMOS technology at a 45nm technology node. The widths of both NMOS and PMOS transistors are 1u and 3u and the length of the transistor considered here is 500nm respectively. The Symica tool was used to design the CMOS, lector, forced NMOS, forced 2 NMOS, forced PMOS inverters, and their schematics are shown above in Fig. 4.2. and simulations are shown below in Fig. 4.2 and 4.3. Fig. 4.2 shows the DC characteristics of CMOS, lector, forced NMOS, forced 2 NMOS, forced PMOS inverters when the supply voltage is 2.8 V and the input voltage given is 1.2 V, here each graph also specifies the switching threshold of these inverters and the rest of the values obtained are mentioned in Table 4.1. The switching threshold voltage of the inverter increases as the supply voltage increases.

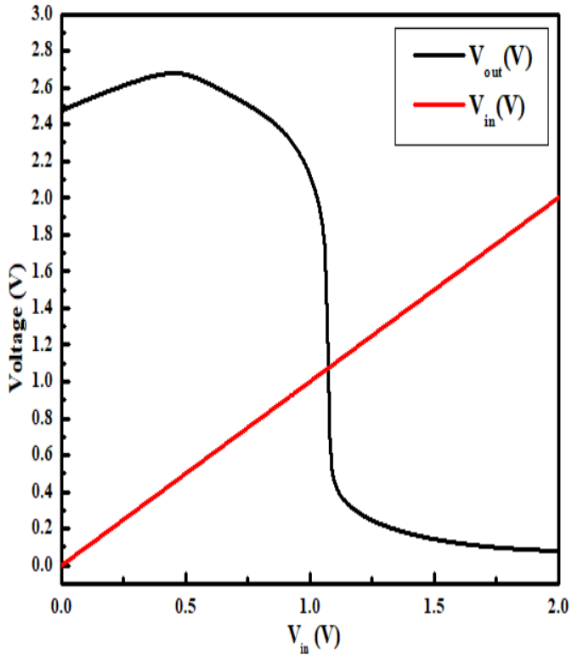
The minimum value of the switching threshold is obtained by the inverter using the lector technique which is 0.988V at 2.8V supply voltage and the maximum value of the switching threshold is obtained by the forced PMOS inverter at 4.02V which is 1.52V while the lector technique has the minimum switching threshold at 4.02V as compared to the other inverters which have the highest noise margin of 2.48V when assessed at 4.02V supply voltage.



(a) (b)



(c) (d)

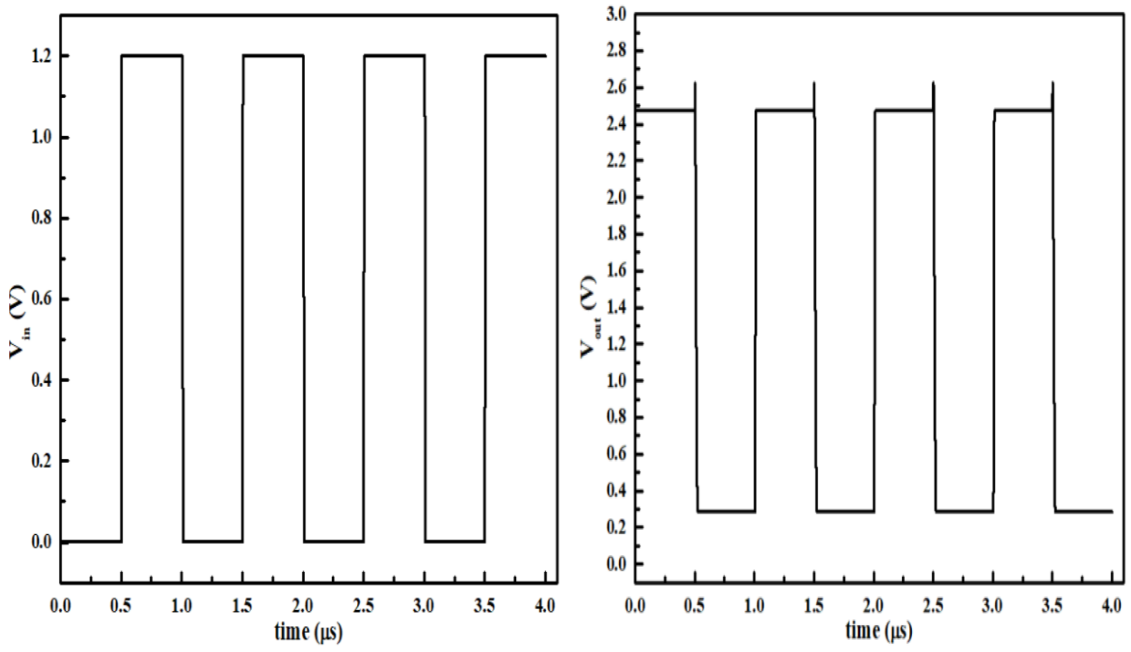


(e)

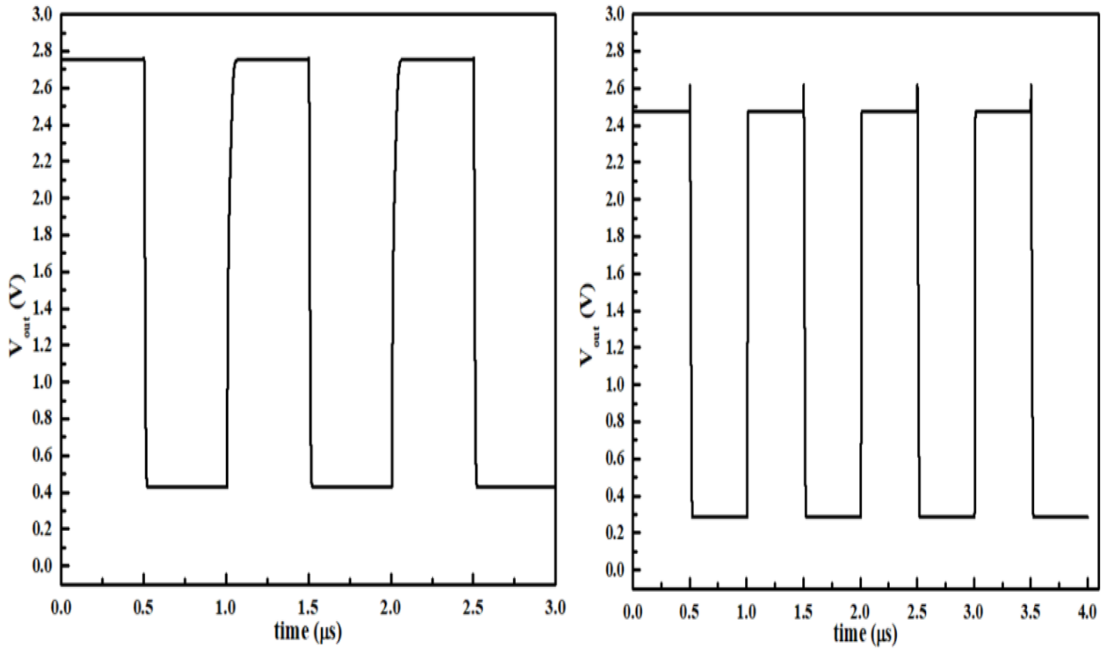
Fig. 4.2 DC characteristics of (a) CMOS inverter (b) inverter using lector technique (c) inverter using forced nmos approach (d) inverter using forced 2 nmos approach (e) inverter using forced pmos approach

As illustrated in Fig. 4.2, a DC analysis of CMOS, lector, forced NMOS, forced 2 NMOS, forced PMOS inverters at 45nm technology node are performed. The noise margin of the inverters can be calculated using the voltage transfer characteristics of different inverters, as illustrated in Table I. The low noise margin values of the various inverters are

0.831V, 0.5323V, 0.88V, 0.86V, 0.85V, which are obtained at the supply voltage of 2.8V, while the high noise margin values of the different inverters are 1.612V, 1.688V, 1.62V, 1.62V, 1.58V which are obtained at 2.8V, and the rest of the values are summarised in Table 4.1. Because the noise margin must be high, circuits with higher noise margins are deemed good such as the inverter employing the forced NMOS technique, which has the highest noise margin of 2.48V when assessed at 4.02V supply voltage.



(a) (b)



(c) (d)

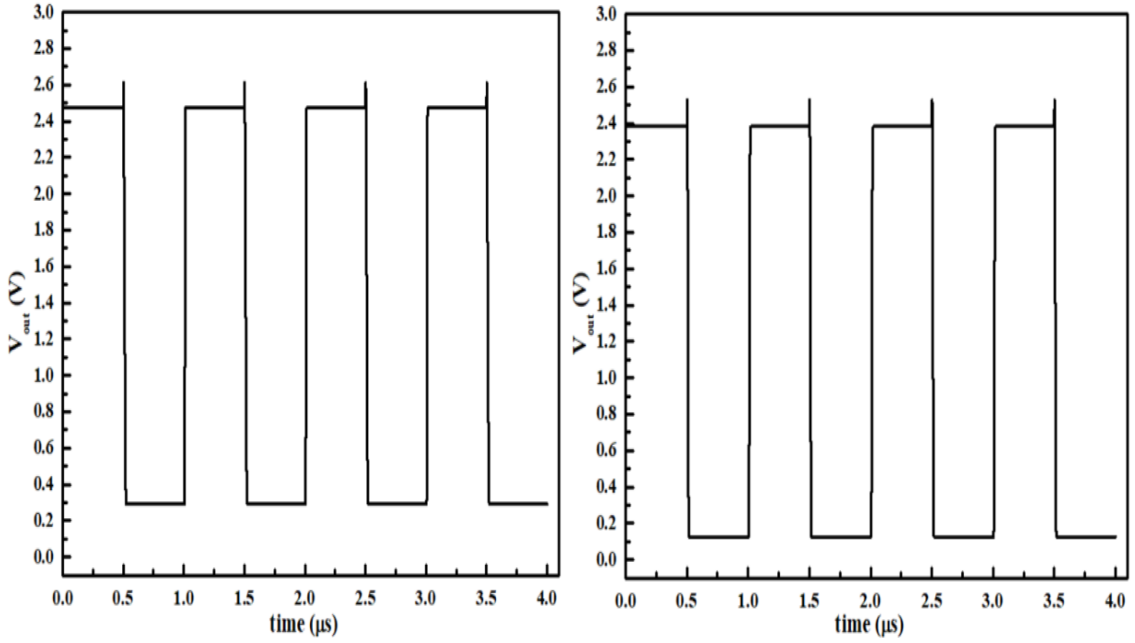


Fig. 4.3 (a) Input waveform for the corresponding inverters and output waveform of the (b) CMOS inverter (c) inverter using lector technique (d) inverter using forced NMOS approach (e) inverter using forced 2 NMOS approach (f) inverter using forced PMOS approach.

The input voltage is 1.2 V during simulation, and the transient analysis is performed for different supply voltages to calculate the average power, delay of the various inverters. Transient response of CMOS, lector, forced NMOS, forced 2 NMOS, forced PMOS inverters at 45nm technology node are shown in Fig. 4.3. which aids in the evaluation of the power and delay.

Table 4.1. shows the experimental values of the power, delay, switching threshold voltage, low noise margin, high noise margin which itself is self-explanatory that the average power of inverter increases as the voltage supply increases as expressed in equation 1 and the dynamic power of the inverter increases as well, as shown in equation 2. If all other parameters are considered to be the same, the inverter adopting lector methodology consumes less power as compared to the other inverters. The smallest value of power obtained by the lector inverter as opposed to that of the other inverter is 1.71mW grows as the supply voltage increases.

Table 4.1 summarizes the power, delay, switching threshold voltages, and noise margin of the various inverters at the 45nm technology node. The propagation delay of the inverter decreases as the supply voltage increases, at supply voltage 2.8V the propagation delay of

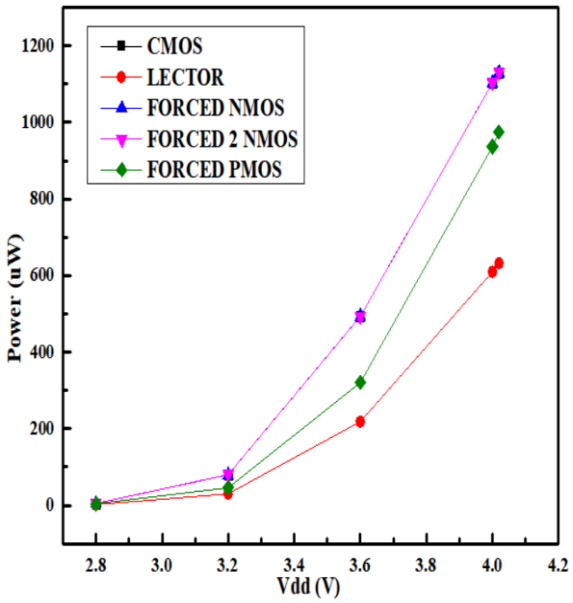
the inverter employing the lector technique is 7.78ns which is the smallest as compared to the other inverters while the inverter with forced PMOS strategy has the highest delay of 9.93ns.

Table. 4.1 Power, delay, noise margin, and subthreshold voltage analysis of different types of inverters at various supply voltage.

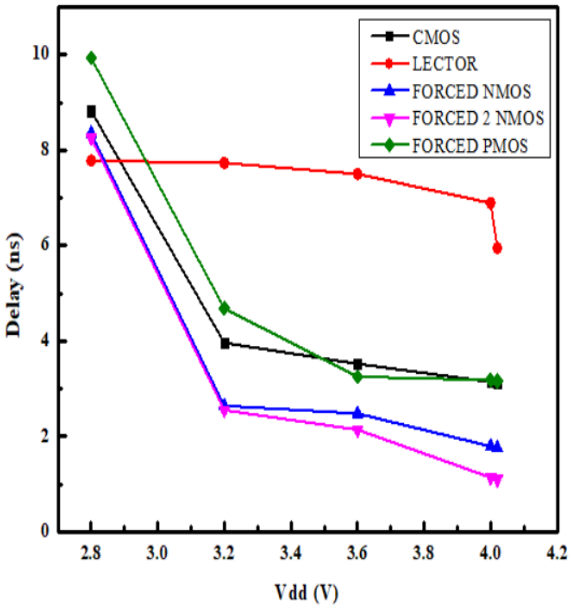
	V_{dd}	**CMOS**	**LECTOR**	**FORCED NMOS**	**FORCED 2 NMOS**	**FORCED PMOS**	**P_{dy} (mW) for all inverters**
P_{avg} (mW)	2.8	4.9	1.71	4.9	4.9	4	0.00392
	3.2	79.96	29.9	79.9	79.96	45.7	0.00512
	3.6	493.34	218.44	493.34	493.3	320.3	0.00648
	4	1103.7	609.89	1103.7	1103.7	936.8	0.00800
	4.02	1130.8	632.69	1130.7	1130.7	974.9	0.00808
Delay (ns)	2.8	8.82	7.78	8.35	8.25	9.93	-
	3.2	3.96	7.73	2.64	2.55	4.68	-
	3.6	3.52	7.5	2.48	2.14	3.25	-
	4	3.14	6.89	1. 79	1.14	3.18	-
	4.02	3.12	5.95	1.76	1.10	3.16	-
Switching threshold Voltage (V)	2.8	1.07	0.988	1.07	1.07	1.10	-
	3.2	1.19	1.053	1.18	1.18	1.24	-
	3.6	1.31	1.163	1.30	1.3	1.38	-
	4	1.42	1.292	1.41	1.41	1.51	-
	4.02	1.43	1.303	1.42	1.42	1.52	-
Low Noise margin (V)	2.8	0.831	0.5323	0.88	0.86	0.85	-
	3.2	0.998	0.542	1.04	1.02	1.03	-
	3.6	1.149	0.551	1.18	1.16	1.20	-
	4	1.286	0.538	1.30	1.28	1.36	-
	4.02	1.293	0.539	1.31	1.3	1.37	-
High Noise margin (V)	2.8	1.612	1.688	1.62	1.62	1.58	-
	3.2	1.88	1.969	1.89	1.9	1.83	-
	3.6	2.155	2.252	2.17	2.40	2.08	-
	4	2.437	2.492	2.46	2.47	2.34	-
	4.02	2.451	2.503	2.48	2.6	2.36	-

But overall the Table 4.1. shows the comparison of several inverters at 45nm technology nodes based on data simulated using the Symica simulation tool. The combined-graphical representation of the average power, propagation delay, Switching threshold voltage, Low noise margin, High noise margin, Dynamic power is shown in Fig. 4.4.

The first graph in Fig. 4.4 demonstrates that the inverter using the lector has average power consumption less as compared to that of other inverters. The second graph illustrated that the delay of forced 2 nmos inverter is smallest as compared to that of other inverters.



(a)



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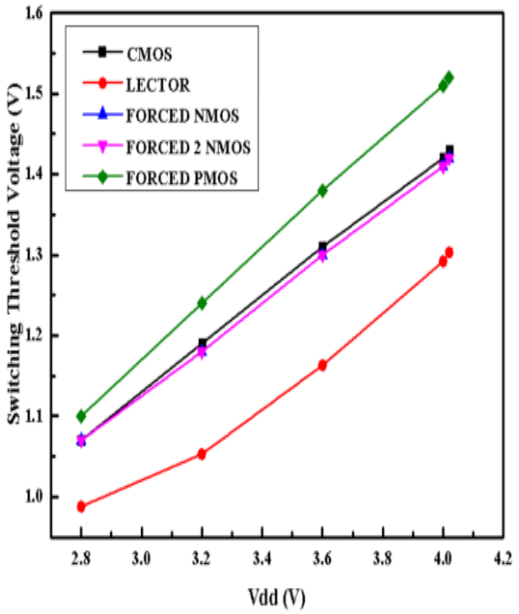
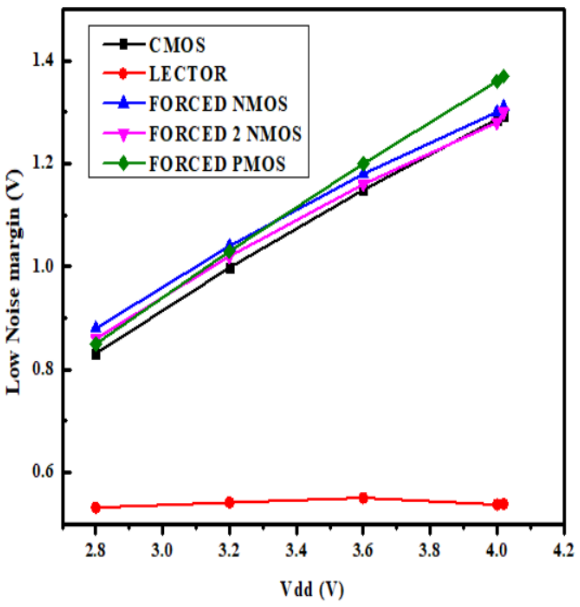
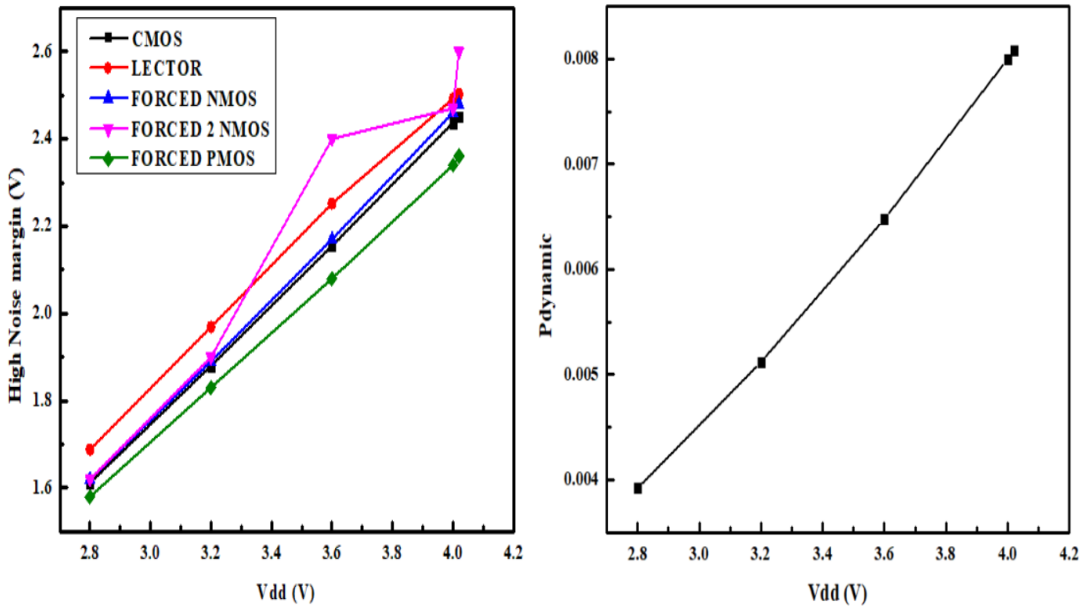


(c)



(d)



(e) (f)

Fig. 4.4 Comparison concerning V_{DD} of (a) Average power (b) Propagation delay (c) Switching threshold voltage (d) Low noise margin (e) High noise margin (f) Dynamic power

The third graph shows the lector technique has the switching threshold values lesser than the other inverters. The fourth graph depicts that the low noise margin values are lower for inverters using lector techniques and higher for inverters using the forced pmos approach. The fifth graph demonstrates the high noise margin of the inverter which depicts that the inverter using the forced PMOS strategy has the lowest high noise margin while the inverter using the forced 2 nmos technique has the highest high noise margin values and lastly the sixth graph illustrate the dynamic power variation concerning V_{DD}.

The circuits are designed in the Symica Design Environment with the help of the gpdk045 library. Transient analysis is being performed at various supply voltages for numerous inverters using different low power techniques to obtain simulations in which different current values are noted to determine the power from Table 4.1, it has been noticed that as the supply voltage rises, the inverter's switching threshold voltage rises as well. The maximum value of the switching threshold is obtained by the forced PMOS inverter at 4.02V, which is 1.52V, and the minimum value of the switching threshold is obtained by the inverter using the lector technique, which is 0.988V at 2.8V supply voltage. The lector technique has the lowest switching threshold at 4.02V as compared to the other inverters, which is 1.303V. Because the noise margin must be high, the inverter utilizing

forced NMOS technology is considered good because the noise margin obtained is the highest here, 2.48V evaluated at 4.02V supply voltage. When all other factors are equal, the inverter adopting the lector approach consumes less power than the other inverters at all supply voltages considered in this paper and it keeps rising as the supply voltage increases during the simulation of the circuit.

As a result, it's confirmed that as the supply voltage drops, the inverter's power rises and the delay falls, while the switching threshold voltage and noise margin rise. The information in the preceding table is summarized using graphical representations as shown in Fig. 4.4. This allows comparing inverters based on their power, delay, switching threshold voltage, Low noise margin, High noise margin. The average power of forced PMOS inverter is less as compared to that of other inverters. The power of the inverter increase and the delay diminished as the supply voltage decreases while the switching threshold voltage and noise margin increase as the supply voltage increases.

4.2 Important Outcomes:

- Designing and analysis of different types of INVERTERS are accomplished on 45nm technology node.
- The power, delay, switching threshold voltages, and noise margin of the various inverters at the 45nm technology node are concluded with the help of various graphs keeping all parameters of the transistor constant.
- A conclusion can be made based on the observation the smallest value of power obtained by the lector inverter as opposed to that of the other inverter is 1.71mW grows as the supply voltage increases.

CHAPTER 5

FREQUENCY ANALYSIS OF RING OSCILLATOR AT DIFFERENT TECHNOLOGY NODE

5.1 Different Stage CMOS Ring Oscillator

A ring Oscillator is a closed loop that contains an unequal number of parallel inverters that form a response circuit. In the low-cost digital CMOS process, it becomes a better choice [2, 7]. The concept of a ring oscillator with a delay stages chain has sparked a lot of curiosity because of its many fruitful attributes. These peculiarities incorporate oscillations that can be accomplished at low voltage; designing can be easily done using integrated circuit technology (Bi-CMOS, CMOS). It is possible to adjust it electronically. Because of their basic structure, multiphase outputs are provided with a high frequency of oscillation while dissipating low power [9-14, 16, 18].

A ring oscillator with an even number of circular transistors cannot be used, as the outcome of the inverter is the same as the input. The ring oscillator with multi-stage numbers can be used as a basic SRAM module and is considered part of memory [14, 16].

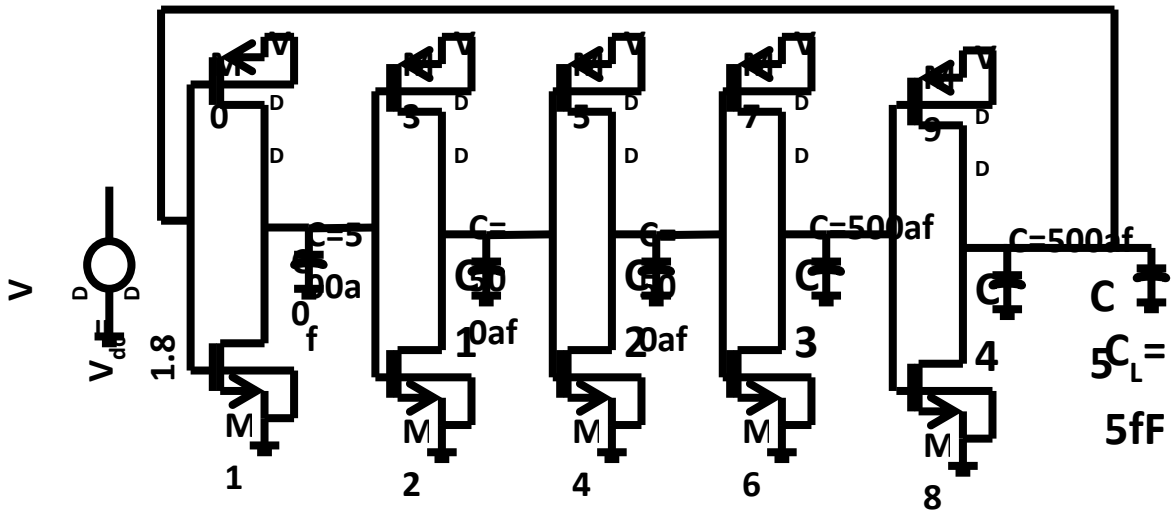


Fig. 5.1. - Five-stage ring oscillator circuit

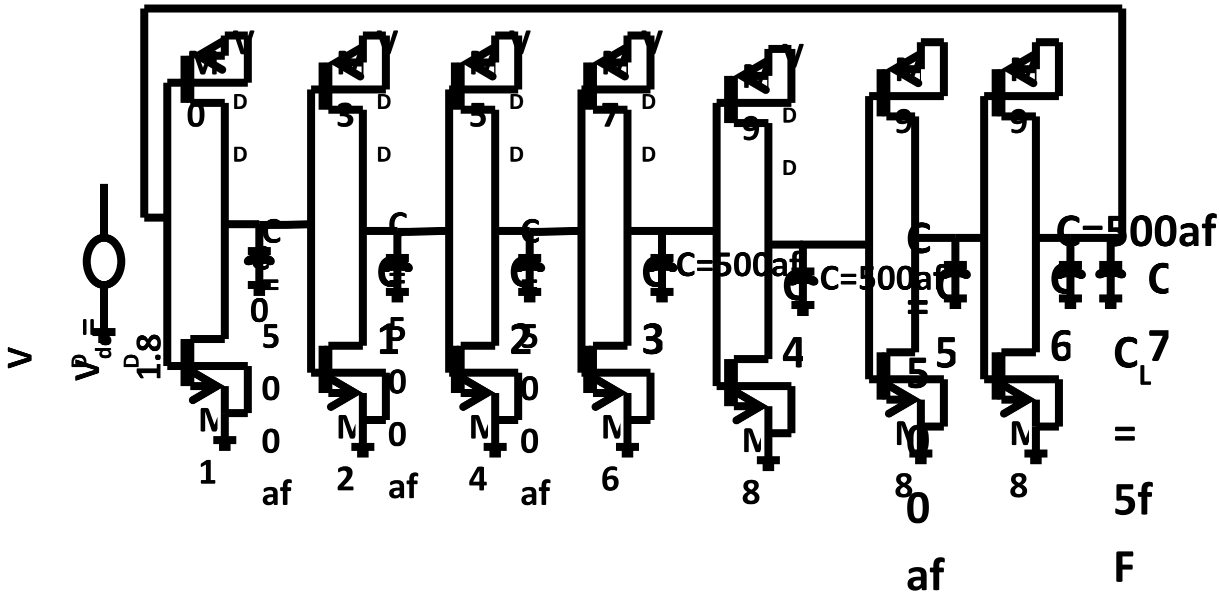


Fig. 5.2. - Seven-stage ring oscillator circuit

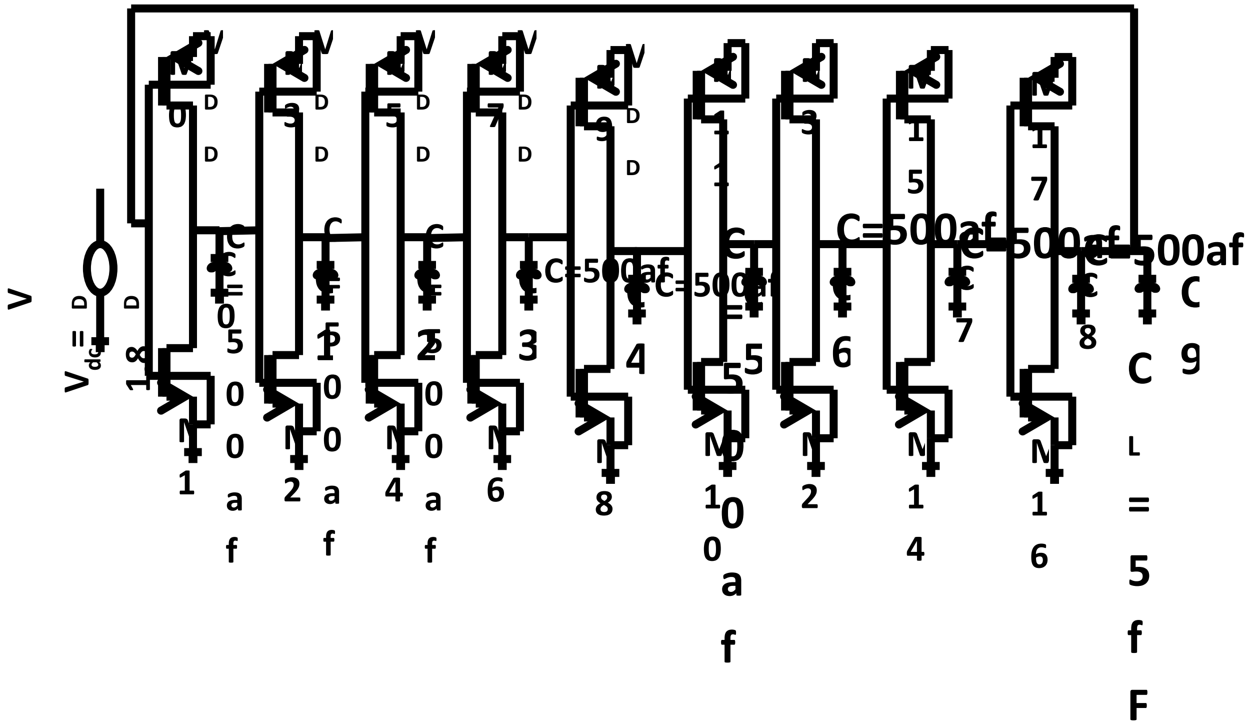


Fig. 5.3. – Nine-stage ring oscillator circuit

The designing and analysis of 5, 7, 9 stage ring oscillators as shown in Fig. 5.1, Fig. 5.2, Fig. 5.3. Fig. 5.1 depicts the structure of the five-stage ring oscillator. Fig. 5.2 illustrates the structure of the seven-stage ring oscillator. Fig. 5.3 depicts the structure of

the nine-stage ring oscillator, during which 1.8 V supply is used and capacitor of 500aF and load capacitor of 5fF used to calculate the frequency [7, 53].

The ring oscillator oscillation is known as the total delay for each step being doubled. In the ring oscillator, the oscillator starts automatically over a certain threshold voltage. As the number of stages raises, the total delay rises and reduces the frequency of oscillation. Increased supply voltage reduces the delay and increases the oscillation frequency [2, 5, 6, 9, 10, 55].

5.2 Oscillation Frequency

The phase shift of 2π is provided to achieve self-sustained oscillations at the frequency of oscillation unity voltage gain is there. Ring oscillator comprises of N number of stages, each stage in it provides a π/N phase shift, and the residual phase shift π is provided by dc inversion [54]. The oscillation frequency is stated

$$f_o = \frac{1}{2Nt_d} \tag{13}$$

Where f_o is Ring Oscillator oscillation frequency, t_d is each delay stage propagation delay and N denotes the number of stages used in the ring oscillator. The frequency of the ring oscillator rely on the transmission delay $t_d$and the number of phases. The oscillation regularity can be resolved from the t_d expression based on the parameters of the circuit. But the biggest obstacle to detecting exposure t_d arises due to nonlinearities and parasitic circuits [5-7, 9, 10].

5.3 Result Analysis of Ring Oscillator

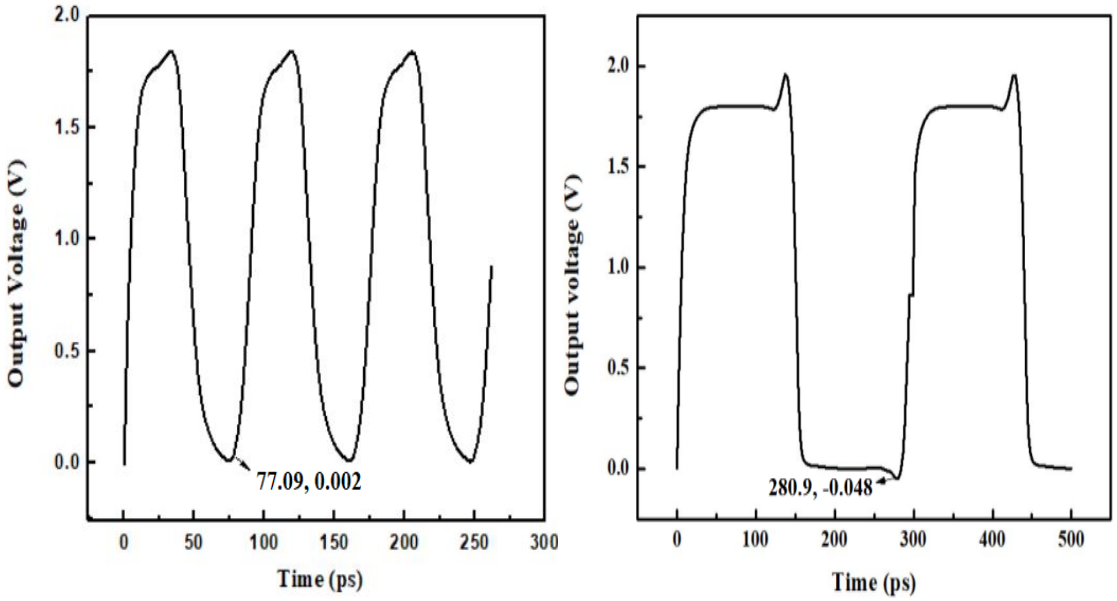
The implication within the wavering recurrence of the ring oscillator can be attained in two ways: by lessening the number of stages in the structure of the ring oscillator. There is a dependency of each stage delay on the process parameters and circuit structures. For increment in speed of operation and reduction in power consumption and saving area, the abatement in several stages is found captivating [6, 7, 11, 12, 17].

The design of ring oscillators for different stages is simulated using CMOS technology at different technology nodes such as 45nm, 32nm, 22nm. The widths of both NMOS and PMOS transistors are 2u and 5u respectively. The symica tool was used to design the 5 stages, 7 stages, and 9 stage ring oscillator, and their schematics are shown above from

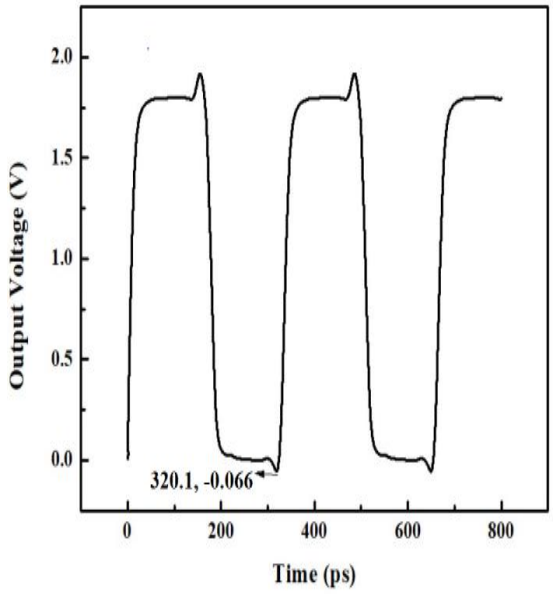
fig. 5.1 to 5.3 and simulations are shown below fig. 5.4 to 5.6. Fig 5.4 to 5.6 shows the output alternating between 0 to 1.8 V as expected.

As per the functioning of the ring oscillator, when the input voltage is enforced directly, oscillation begin immediately. While doing simulation the input voltage applied is 1.8 V and the transient analysis is carried out for different periods. Transient responses of five, seven, nine stages at 45nm technology node are shown in Fig. 5.4 which helps in evaluating the frequency of oscillation. The period of five, seven, nine-stage ring oscillators are 77.09ps, 280.9ps, and 320.1ps, respectively which help in evaluating the frequency of the respective ring oscillators as calculated using equation 13.

All the ring oscillators consist of 5 stages, 7 stages, 9 stage cascaded inverters, and the corresponding oscillation frequency is calculated for a fair comparison. Table 5.1 summarizes the oscillation frequency of all the ring oscillators considered.



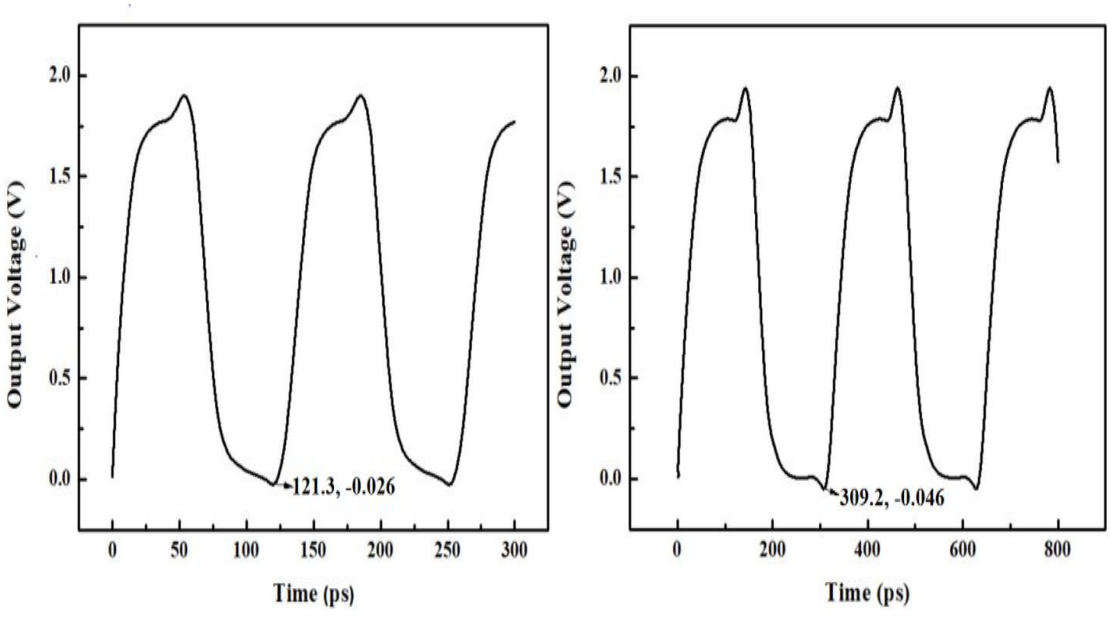
(a) (b)



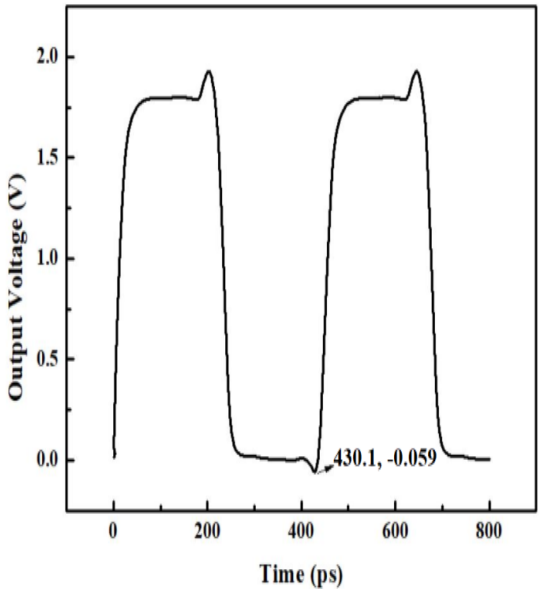
(c)

Fig. 5.4. Output waveform at 45nm technology node (a) Five-stage ring oscillator (b) Seven-stage ring oscillator (c) Nine-stage ring oscillator

A comparison is carried out so the transient analysis of five, seven, nine stages at 32nm and 22nm technology node is deiplayed in Fig. 5.5 and Fig.5.6.



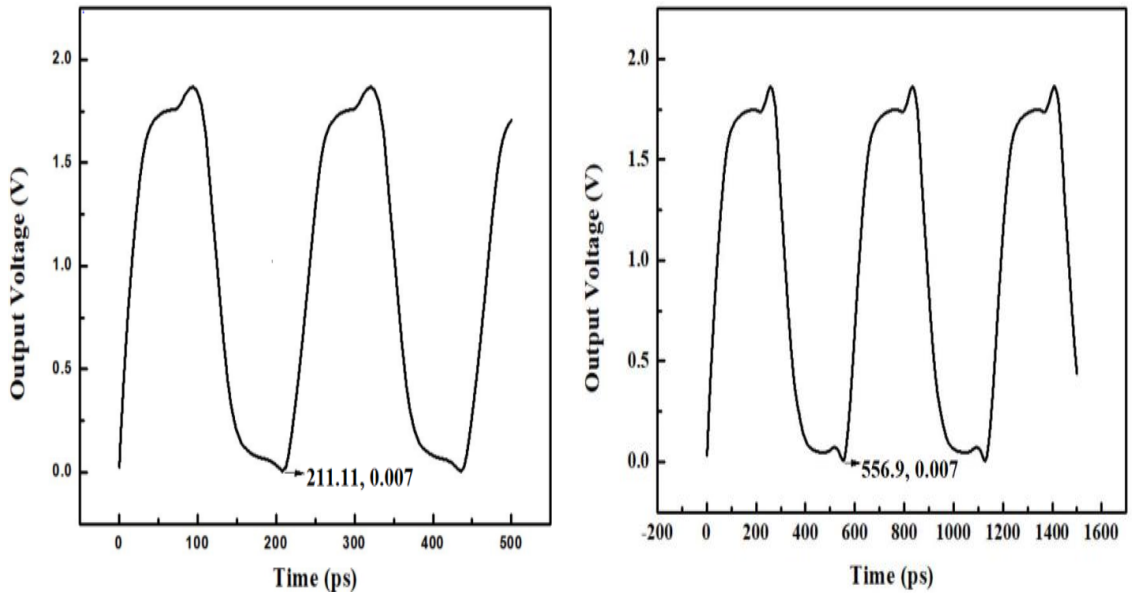
(a) (b)



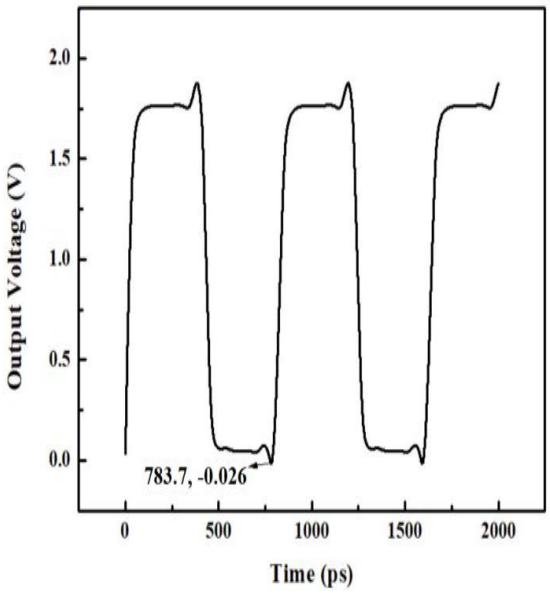
(c)

Fig. 5.5.Output waveform at 32nm technology node (a) Five-stage ring oscillator (b) Seven-stage ring oscillator (c) Nine-stage ring oscillator

The period of five, seven, nine stages ring oscillators are 121.3ps, 309.2ps, 430.1ps, respectively, while the other remaining ring oscillators have periods of 211.1ps, 556.9ps, 783.7ps which promotes the calculation of frequency for the respective oscillators at different stages.



(a) (b)



(c)

Fig. 5.6. Output waveform at 22nm technology node (a) Five-stage ring oscillator (b) Seven-stage ring oscillator (c) Nine-stage ring oscillator

Comparative data that was simulated on the Symica simulation tool has been tabulated in Table II. which illustrates the comparison of different stages of ring oscillator at different technology nodes. These measured period values support the calculation of frequency with the help of equation (13) which defines the relationship between frequency and period. The table itself shows the same behavior as the equation i.e. the frequency is inversely proportional to the period (as the period increases, the frequency decreases).

TABLE 5.1 Comparision of Different Stages of Ring Oscillator at Different Technology Node

Technology Node	**5 stage**	**7 stage**	**9 stage**
45 nm	T=77.09 ps F=12.9 GHz	T=280.9 ps F=3.56 GHz	T=320.1 ps F=3.12 GHz
32nm	T=121 ps F=8.25 GHz	T=309.2 ps F=3.23 GHz	T=430.1 ps F=2.33 GHz
22 nm	T=211.1ps F=4.74 GHz	T=556.9 ps F=1.8 GHz	T=783.7 ps F=1.28 GHz

The design entry of the circuits is carried out in the Symica Design Environment using gpdk045, gpdk032, gpdk022 library. For multiple ring oscillators, transient analysis is being performed at various technology nodes to obtain simulations in which interval is

observed at various stop times. From Table II, it is observed that maximum frequency is obtained at 5 stage ring oscillator in each case i.e 12.97GHz in 45 nm, 3.25GHz in 32 nm, 4.74GHz in 22 nm. The detailed analysis also helps in observing that as the technology node decreases, the frequency also decreases, and as the number of stages and periods increases, the frequency decreases. Consequently, it is confirmed that frequency decreases as the period increments.

5.4 Important Outcomes:

- 5, 7, 9 stages ring oscillators are analyzed at different technology nodes with a power supply of 1.8 V.
- Frequency Analysis of these ring oscillators is done and it is observed that as the technology node decreases, the frequency also decreases, and as the number of stages and periods increases, the frequency decreases.
- 5 stage ring oscillator has a maximum frequency at all technology nodes.

CHAPTER 6

PROPOSED RING OSCILLATOR BASED ON ADVANCED INVERTER CONFIGURATION

Most mobile applications, such as portable communication devices, and laptops run at limited power. Devices allied to cell phones have everlasting unoccupied times and work in standby mode when not in use. As a result, the extension of battery-based operating time is an important design goal that can be used effectively by controlling the 3 current leaks flowing through the CMOS gate. Low power consumption in active VLSI circuits is a eminently advisable feature as it is directly related to battery growth time, fidelity, packing, and heat removal costs. Historically, in the 1980s CMOS technology took over VLSI design cables because CMOS consumed much less power than its predecessors (nMOS, bipolar, etc.). While this benefit still exists, the withdrawal of CMOS power has been

problematic yet. Over time, the variable power accounts for more than 90% (usually, more than 99%) of the total chip capacity, and thus was often used as the entire power consumption of 0.18µ technology and foregoing. However, as technology reaches tens of thousands of nanometers, leak energy becomes as important as dynamic energy. Therefore, many ideas have been suggested to address the problem of energy leakage. With the continuous practice of technical measurements, leak power contributes significantly to the overall power consumption in CMOS circuits. Vdd balancing reduces power consumption but also reduces circuit performance. This can be compensated in part by lowering Vth but at the expense of increasing leakage capacity. Reducing the use of leak energy is currently a major research challenge. Low-level leaks have a few options available. To provide an encouraging context to illustrate the potential impact of this thesis, let us compare the effect of static energy (leakage) on the context of a mobile model. We think that in general, the cell phone we are considering is always on (i.e., 24 hours a day). However, the actual time to use a cell phone is very short. If we take a 500-minute call system with a total of 500 minutes used per month, the cell phone only works by 1.15% (500min / (30days ∗ 24hours ∗ 60min)) for the total operating time. This means that during breaks - 98.85% of the time - the cell phone is not working; However, due to the use of static power, during breaks (set aside) the cell phone still powers and shortens battery life. For technologies such as 0.07µ, the impact of the leak force is significant.

Based on advanced inverter configuration for low power applications novel ring oscillator circuits are designed which are:

6.1 Forced Stack Ring Oscillator

Here the first goal of reducing energy consumption in a cycle, can be achieved by reducing current power and voltage and other factors are also useful but in this cycle, it is currently being considered. To reduce the current of the circuit, there is a need to increase the resistance of the circuit. This cycle has used this process which is to increase the resistance of the method and this is achieved by packing the transistor display under fig 6.1. [49]

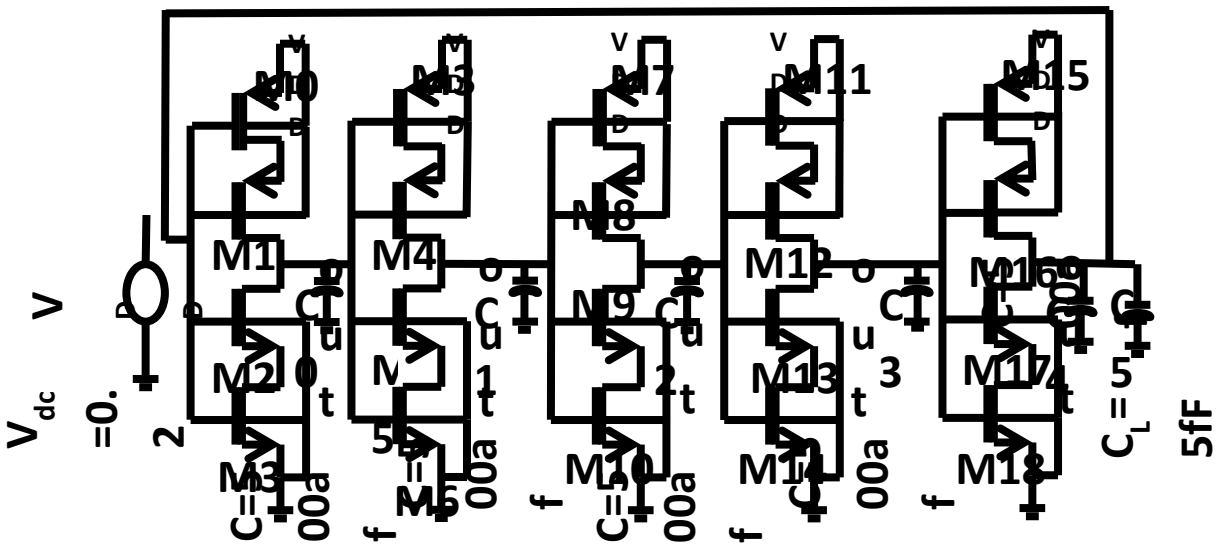


Fig. 6.1 Schematic of Forced Stack Ring Oscillator

Another way to reduce the leakage power of the stack system, which force the effect of the stack by breaking the existing transistor into half transistors. For example, in FST if size W / L = 8 pMOS and W / L = 4 nMOS where a standard CMOS converter can use W / L = 16 pMOS and W / L = 8 in nMOS each transistor is divided into sections two equal. transistors thus conserve input power. When two transistors are switched off together, the bias caused by the recurrence between the two transistors leads to a decrease in current leakage. However, isolated transistors increase the delay noticeable and may restraint the usefulness of the method [28, 38].

The forced stack method uses the stack effect of the transistors and reduces leakage. This is due to the reduction of the gate of the power source and the decrease of the coefficient of DIBL due to the slow pumping of water to the source power thus reducing leakage. The forced stack method fails to preserve power consumption in standby mode [38].

6.2 Sleepy Stack Ring Oscillator

This process was introduced by Park in the year 2005. The sleeping stack method incorporates both sleep patterns and stack methods. The sleep stack strategy, like the stack method, separates existing transistors into two partial transistors. Then, in conjunction with one of the separated transistors, sleep transistors were added. Its structure is shown in Fig 6.2. In sleeping stack, the benefits of both stack and sleeping techniques are applied together. The sleep transistor is in active mode during sleep, and the stacked transistor

overcomes the current leak while maintaining the condition. Each sleep transistor is connected to a single transistor stack, reducing the resistance of both transistors and reducing the delay in all-active mode. When sleep transistors are closed, the presence of a channel from the Vdd or ground prevents the flow from flowing, and in this case, the current leak can be suppressed by applying a high threshold voltage to the sleep transistor and the transistor in parallel [38]. The main disadvantage of this method is that each of the first transistors is replaced by three transistors of same sleeping stack.

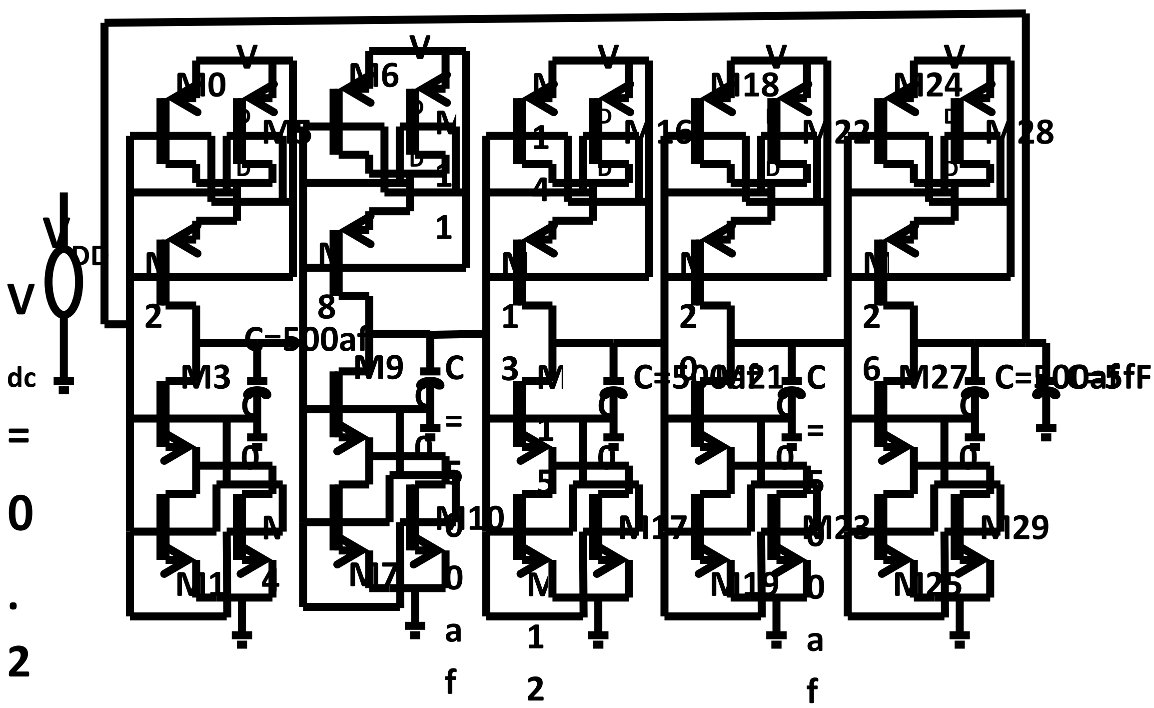


Fig. 6.2. Schematic of Sleepy Stack Ring Oscillator

6.3 Forced NMOS Ring Oscillator

The explanation of this technique is done in the above chapter of the inverter in which the advanced configurations of CMOS inverter are discussed. The technique used in that inverter for low power application is used in ring oscillator for its better performance. The circuit pictograph of this ring oscillator is displayed in Fig. 6.3.

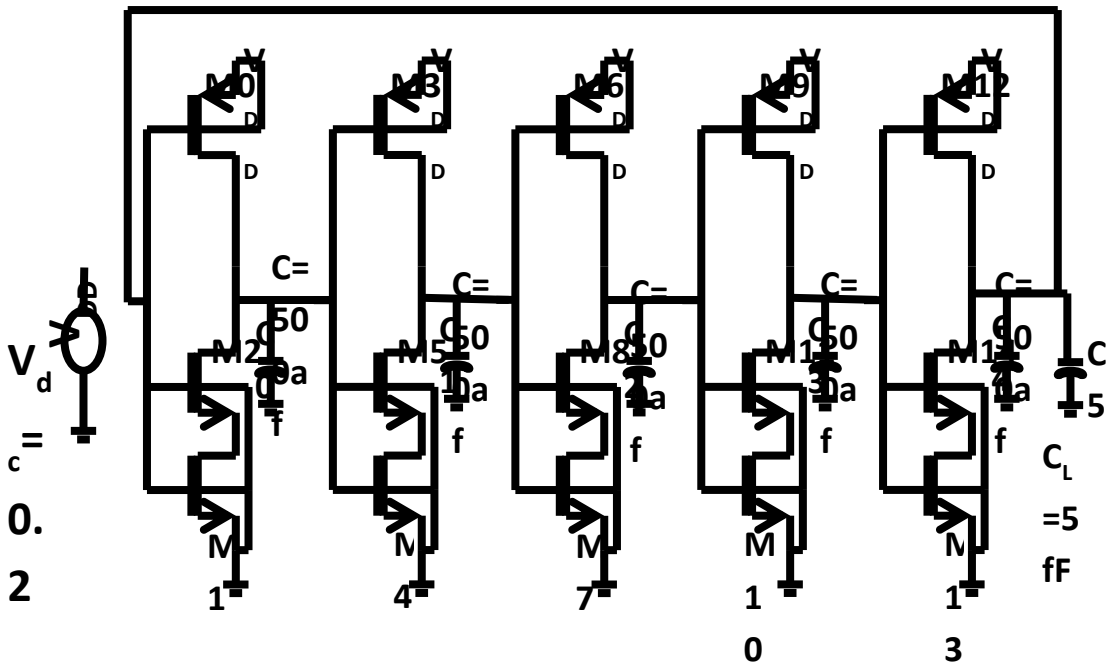


Fig. 6.3. Schematic of Forced NMOS Ring Oscillator

6.4 Forced 2 NMOS Ring Oscillator

To demonstrate this oscillator first we have to understand this low power technology named forced 2 NMOS with the help of which this ring oscillator is designed and analyzed. Fig. 6.4 depicts the circuit diagram of the forced 2 NMOS Ring Oscillator.

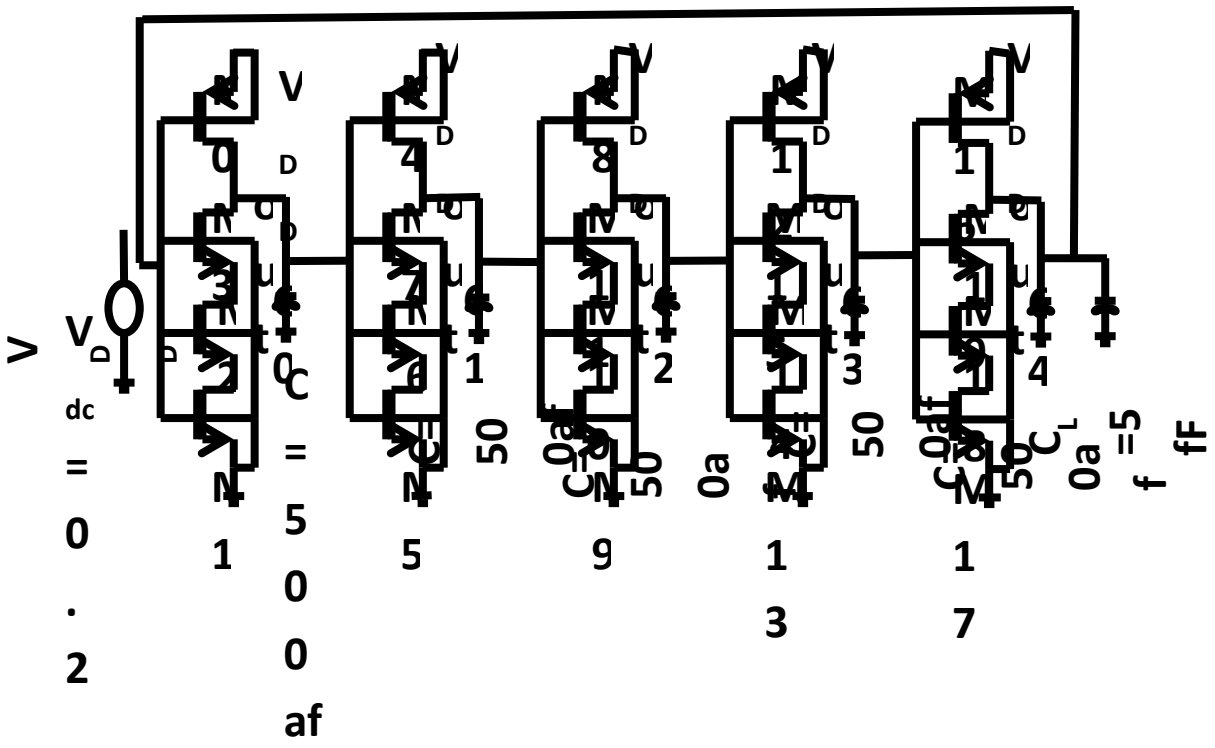


Fig. 6.4. Schematic of Forced 2 NMOS Ring Oscillator

6.5 Forced PMOS Ring Oscillator

Forced PMOS technique is used in ring oscillator to analyze the circuit performance so that it is easy for the designer and consumer to identify which ring oscillator is better in terms of many parameters (here main consideration is power consumption). The circuit's explanation is done by Fig 6.5.

6.6 LECTOR Ring Oscillator

The analysis and explanation of this technique are done in the above chapter of the inverter for the easiness of the designer to design the best circuit out of the analyzed circuits. The circuit which is to be analyzed and simulated by the designer is pictured in Fig. 6.6.

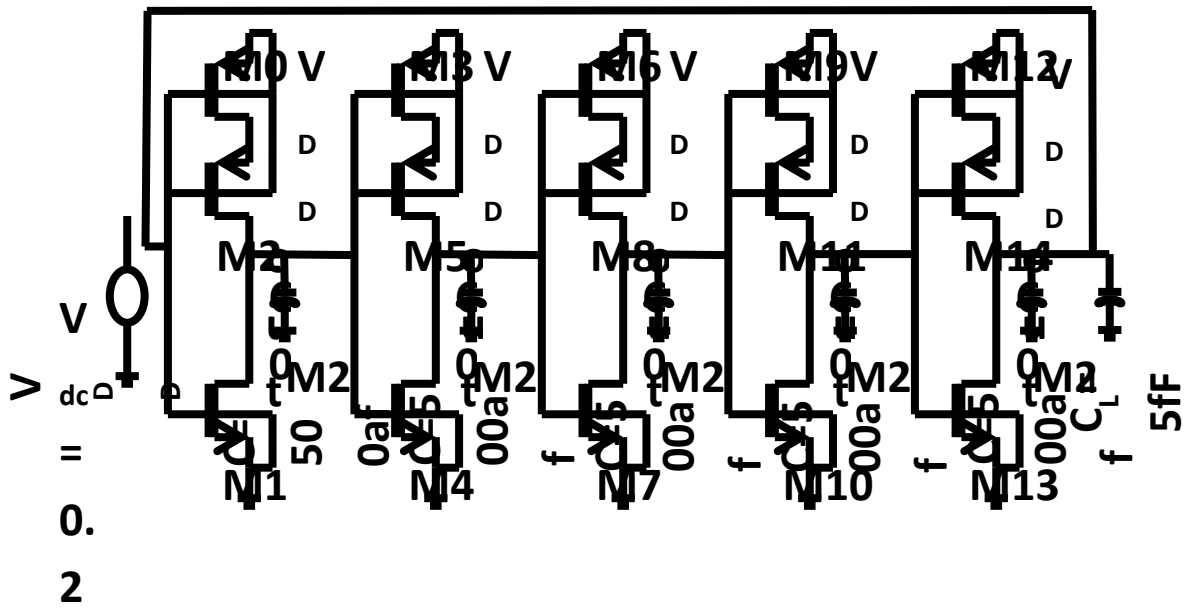


Fig. 6.5. Schematic of Forced PMOS Ring Oscillator

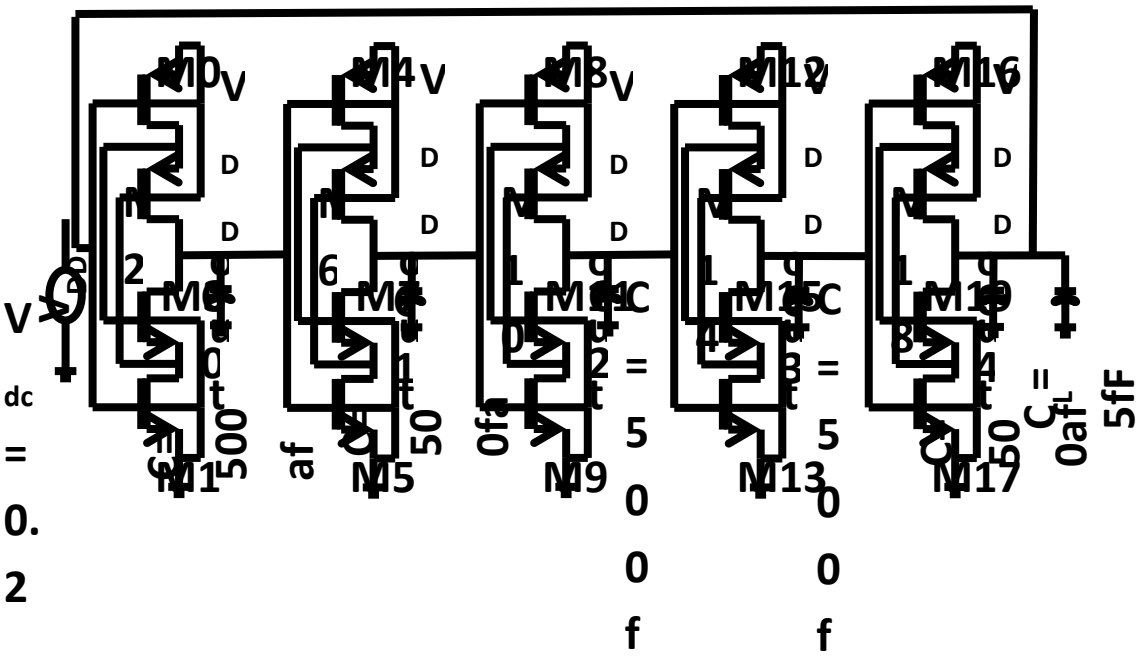


Fig. 6.6. Schematic of LECTOR Ring Oscillator

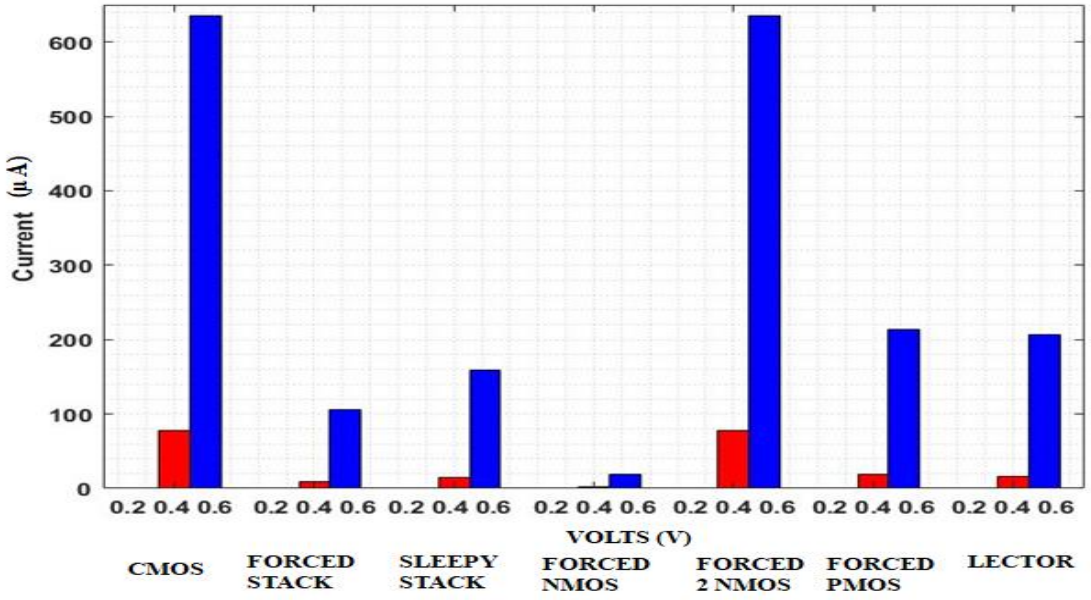
Table 6.1 Power calculation of different types of Ring Oscillators

RING OSCILLATOR TECHNOLOGY	VDD	CURRENT (µ A)	AVERAGE POWER (µ W)

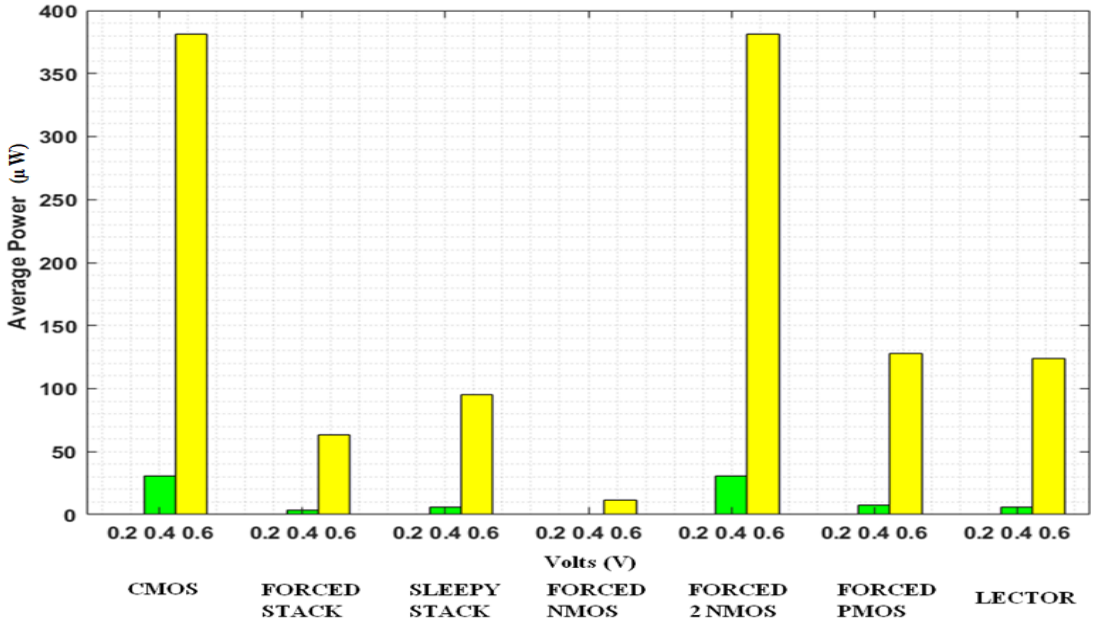
CMOS	0.2	0.672	0.134
	0.4	77.64	31.04
	0.6	635.7	381.42
FORCED STACK	0.2	0.108	0.0216
	0.4	9.13	3.652
	0.6	106.28	63.72
SLEEPY STACK	0.2	0.159	0.031
	0.4	14.35	5.74
	0.6	158.96	95.34
FORCED NMOS	0.2	0.105	0.021
	0.4	1.61	0.644
	0.6	19.22	11.53
FORCED 2 NMOS	0.2	0.646	0.129
	0.4	77.55	31.02
	0.6	635.7	381.42
FORCED PMOS	0.2	0..223	0.044
	0.4	18.31	7.32
	0.6	213.0	127.8
LECTOR	0.2	0.174	0.034
	0.4	15.90	6.36
	0.6	207.09	124.2

In this thesis, the 5-stage oscillator was victoriously performed and simulated using the Symica virtuoso instrument at 45nm. The main goal is to reduce the power consumption to medium and leak power. Improving antecedent research work by contracting the power supply to provide and implement different approaches and simulation results. Table 6.1 shows the comparisons between different ring oscillators. Depending on the simulation results obtained, it can be summed up that the proposed oscillator ring performs better performance during power consumption.

Table 6.1 itself depicts the values of current and power concerning VDD and it shows that as the value of VDD increases the current across the circuit increases and as the value of current incremented, the power of the ring oscillators raises. The power consumption of forced stack, lector, forced NMOS, forced PMOS, sleepy stack, forced 2 NMOS ring oscillators at 0.2V are 0.0216µW, 0.0348µW, 0.021µW, 0.044µW, 0.03µW, 0.129µW, 0.134µW.



(a)



(b)

Fig. 6.7. Current and power comparison of different types of Ring Oscillators concerning V_{DD}.

From Table 6.1 it is demonstrated that less power is consumed by forced stack and forced NMOS at 0.2V which is 0.021µW and as the value of VDD increases, the current also increases which in turn results in an increment of the power. While at 0.4V the NMOS is considered, as power increases while the consumption of power in forced NMOS is less

as compared to all other ring oscillators. This whole comparison of all the ring oscillators designed with the help of advanced inverter topologies is shown in Fig 6.7 which depicts which ring oscillator consumes less power and which consumes more power at what voltage and also shows the behavior of current and power concerning $V_{DD.}$ It has been a challenge for designers to keep power consumption within tolerable limits without affecting other structures such as location and delays due to reduced size of the technical aspect. In this thesis, a review of other low-power design strategies is presented. Each method has its advantages and disadvantages. It is the designers' choice to choose the one that best suits their needs and design process.

IMPORTANT OUTCOMES:

- The proposed ring oscillators has been analyzed and simulated.
- Current and power have been calculated.
- Our proposed design shows superior performance over the conventional ring oscillator.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

The circuits are designed in the Symica Design Environment with the help of the gpdk045 library. Transient analysis is being performed at various supply voltages for numerous inverters using different low power techniques to obtain simulations in which different current values are noted to determine the power from Table 4.1, it has been noticed that as the supply voltage rises, the inverter's switching threshold voltage rises as well. The maximum value of the switching threshold is obtained by the forced PMOS inverter at 4.02V, which is 1.52V, and the minimum value of the switching threshold is obtained by the inverter using the lector technique, which is 0.988V at 2.8V supply voltage. The lector technique has the lowest switching threshold at 4.02V as compared to the other inverters, which is 1.303V. Because the noise margin must be high, the inverter utilizing forced NMOS technology is considered good because the noise margin obtained is the highest here, 2.48V evaluated at 4.02V supply voltage. When all other factors are equal, the inverter adopting the lector approach consumes less power than the other inverters at all supply voltages considered in this paper and it keeps rising as the supply voltage increases during the simulation of the circuit.

As a result, it's confirmed that as the supply voltage drops, the inverter's power rises and the delay falls, while the switching threshold voltage and noise margin rise. The information in the preceding table is summarized using graphical representations as shown in Fig. 4. This allows comparing inverters based on their power, delay, switching threshold voltage, Low noise margin, High noise margin. The average power of forced PMOS inverter is less as compared to that of other inverters. The power of the inverter increase and the delay decays as the supply-voltage decreases while the switching threshold voltage and noise margin increase as the supply voltage raises.

The design entry of the circuits is carried out in the Symica Design Environment using gpdk045, gpdk032, gpdk022 library. For multiple ring oscillators, transient analysis is being performed at various technology nodes to obtain simulations in which interval is observed at various stop times. From Table 5.1, it is observed that maximum frequency is obtained at 5 stage ring oscillator in each case i.e 12.97GHz in 45 nm, 3.25GHz in 32 nm,

4.74GHz in 22 nm. The detailed analysis also helps in observing that as the technology node decreases, the frequency also decreases, and as the number of stages and periods increases, the frequency decreases. Consequently, it is confirmed that frequency decreases as the period increments.

Today, as the size of the technical aspect decreases, it has become a challenge for designers to keep power consumption at tolerable limits without much impact on other location-based parameters and top-down delays. In this thesis, a review of some of the most widely used low power design techniques is presented with the help of new oscillator rings. i.e sleepy stack ring oscillator, forced NMOS ring oscillator, forced 2 NMOS ring oscillator, forced PMOS ring oscillator, lector ring oscillator, and forced stack ring oscillator. The above chapter depicts the simulation and results in the analysis of these several ring oscillators to selective in case of choosing the best ring oscillator according to their performance concerning various parameters (here mainly power is considered). From the thesis, it can be easily concluded that as the value of VDD increases the current across the circuit raises, and as the value of current increases the power of the ring oscillators increases. The power consumption of forced stack, lector, forced NMOS, forced PMOS, sleepy stack, forced 2 NMOS ring oscillators at 0.2V are 0.0216µW, 0.0348µW, 0.021µW, 0.044µW, 0.03µW, 0.129µW, 0.134µW.

7.2 Future Scope

Based on the assesment, it is estimated that at lower technology node Ring Oscillator work properly. As technology nodes getting shrinking down their frequency of oscillation is degrades. For more improvised RO's, new techniques can be carried out in practice. Based on result analysis as in this thesis Symica is used to mimic and acquire static energy, dynamic energy, and distribution delays. Dependence on static power, dynamic energy, and distribution delays in VDD, and temperature fluctuations can be limited to these methods. Our proposed new methods can be used in additional phases of the oscillator ring and other ring oscillator applications in the future. Also, sound analysis of this can be done for further improvement.

LIST OF PUBLICATIONS

Published

1. R. Bharti and P. Mittal, "Frequency Analysis of Ring Oscillator at Different Technology Node", *International Conference on Simulation, Automation & Smart Manufacturing* (*SASM 2021*), organized by GLA University, Mathura, held on 20-21 Aug 2021; **(**to be published by **IEEE**, **Scopus Indexed**).

   Status: Presented the paper during conference

2. R. Bharti and P. Mittal, "Comparative Analysis of Different Types of Inverters for Low Power at 45nm," *Third International Conference on Advances in Computing, Communication Control and Networking* (*ICAC3N 2021*), Galgotias College of Engineering and Technology, Greater Noida, UP, India, 17-18 Dec 2021 (to be published by **IEEE**, **Scopus Indexed**)

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REFERENCES

[1] S. Suman, M. Bharadwaj and B. P. Singh, "An Improved Performance Ring Oscillator Design", IEEE Computer Society, pp. 236-239, 2012.

[2] S. Kumar and G. Kaur, "Design and Performance Analysis of Nine Stages CMOS Based Ring Oscillator" In International Journal of VLSI design & Communication Systems, vol. 3, pp. 57-69, VLSICS, 2012.

[3] S. Negi, P. Mittal and B. Kumar, "Analytical Modeling and Parameters Extraction of Multilayered OLED", IET Circuits, Devices, and Systems, pp. 1255-1261, 2019.

[4] S. Khan, "Design of Ultra-Low Power CMOS Inverter", International Journal of Innovative Research in Electrical, Electronics, Instrumentation, and Control Engineering, IJIREEICE, pp. 55-57, 2016.

[5] V. Sikarwar, N. Yadav and S. Akashe, "Design and analysis of CMOS ring oscillator using 45 nm technology", 3rd IEEE International Advance Computing Conference, pp. 1491-1495, 2013.

[6] A. K. Mahato, "Ultra Low-Frequency CMOS Ring Oscillator Design", Proceedings of RAECS UIET Panjab University Chandigarh, IEEE, 2014.

[7] S. Chauhan and R. Mehra, "CMOS Design and Performance Analysis of Ring Oscillator for Different Stages", International Journal of Engineering Trends and Technology, vol. 32, pp. 234-237, IJETT, 2016.

[8] N. Mishra, P. Mittal, and B. Kumar, "Analytical Modeling for Static and Dynamic Response of Organic Pseudo All-p Inverter Circuits", Journal of Computational Electronics, pp. 1490–1500, 2019.

[9] B. Rawat and P. Mittal, "Single Bit Line Accessed High-Performance Ultra Low Voltage operating 7-T SRAM Cell with Improved Read Stability", International Journal of circuit theory and applications, vol. 49, pp. 1435-1449, 2021.

[10] A. Koithyar and T. K. Ramesh, "Frequency equation for the submicron CMOS ring oscillator using the first-order characterization", J. Semicond., vol. 39, pp. 055001-1-055001-6, 2018.

[11] P. Mittal, “Ditch and Elevated OTFT based Improved Common Source Voltage Amplifier: Frequency Response Characteristics and Analytical Modeling”, Journal of the Society for Information Display, pp. 1-17, 2021.

[12] B. Kinger, S. Suman, K. G. Sharma, and P. K. Ghosh, “Design of Improved Performance Voltage Controlled Ring Oscillator”, Fifth International Conference on Advanced Computing & Communication Technologies, pp. 441-445, 2015.

[13] P. Mittal and N. Kumar, "Comparative analysis of 90nm MOSFET and 18nm FinFET based different Multiplexers for Low Power Digital Circuits", International Journal of Advanced Science and Technology, vol. 29, pp. 4089-4096, 2020.

[14] M. K. Mandal and B. C. Sarkar, “Ring oscillators: Characteristics and applications”, Indian Journal of Pune & Applied Physics, vol. 48, pp. 136-145, 2010.

[15] B. Kumar, K. Raj, and P. Mittal, “FPGA implementation and mask level CMOS layout design of redundant binary signed digit comparator”, International Journal of Computer Science and Network Security, pp. 107-115, 2009.

[16] S. Kusuma and P. Kumar, “Design and Implementation of Ring Oscillator Circuit using 22nm Technology”, International Journal of Scientific Engineering and Technology Research, vol. 04, pp. 12428-12432, IJSETR, 2015.

[17] A. Tah and D. K. Rakshit, “Study of the frequency of the Frequency Characteristics of a Ring Oscillator”, International Journal of Computing and Network Technology, pp. 171-183, 2013.

[18] N. Kumar and P. Mittal, “Performance Analysis of FinFET based 2:1 Multiplexers for Low Power Application”, 6thStudents Conference on Engineering and Systems (SCES), MNNI, Allahabad, India, 2020.

[19] R.P. Rao, “Dynamic Power Analysis of CMOS Inverter with Various Parameters”, International Journal for Research in Engineering Application & Management (IJREAM), vol. 04, pp. 177-180, June 2018.

[20] P. Saini and R. Mehra, “Leakage Power Reduction in CMOS VLSI Circuits”, International Journal of Computer Applications, vol. 55, pp. 42-48, 2012.

[21] A. Agarwal and Dr. Shobha Sharma, “Study and an assortment of various leakage reduction techniques in CMOS inverter circuit in 45nm technology node”, International

Journal of Advanced Research in Engineering and Technology (IJARET), vol. 10, pp. 376-385, Nov-Dec 2019.

[22] S. Sharma, R. Devasia and G. Sharma, " A novel low power and highly efficient inverter design", Int. j. inf. Technol., 2020.

[23] A. N. Adwani, H. V. Chopade, and S. S. Jain, "Analysis of Power Dissipation & Low Power VLSI Chip Design", International Journal of Modern Trends in Engineering and Research, vol. 02, pp. 89-95, 2015.

[24] V. H. Rane, A. J. Patil and R. R. Karhe, "Basic CMOS Gates using Lector Technique to Reduce Leakage Current in Tanner Tool", IJESC, vol. 9, pp. 23244- 23252, July 2019.

[25] V. R. Nandyala and K. K. Mahapatra, "A Circuit Technique for Leakage Power Reduction in CMOS VLSI Circuits", 2016 International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI-SATA), 2016.

[26] B. T. Geetha, B. Padmavathi, and V. Perumal, "Design Methodologies and Circuit Optimization Techniques for Low Power CMOS VLSI Design", IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-2017), pp. 1759-1763, 2017.

[27] P. K. Rahi, S. Dewangan, T. Yadav and G. S. Rajawat, "Low Power and Area Efficient Design For CMOS Inverter", International Journal for Research in Emerging Science and Technology, vol. 2, 204-208, 2015.

[28] F. Buch, A. Bhardwaj, S. Gupta, and G. Sharma, "Comparison and Performance Analysis of Various Low Power Digital Design Techniques", International Journal of Applied Engineering Research, vol. 13, pp. 5845-5857, 2018.

[29] R. Lorenzo, S. Chaudhury, "Dynamic Threshold Sleep Transistor Technique for High Speed and Low Leakage in CMOS Circuits", Circuits Syst Signal Process, 2016.

[30] S. Gaonkar, "Design of CMOS inverter using lector technique to reduce the leakage power", International Journal of Technical Research and Applications, pp.. 231-233, 2015.

[31] D. V. R. Raju, "Ultra-low power VLSI design", vol. 5, pp. 21-25, 2018.

[32] L. Kumre, B. P. Shrivastava, N. Rai, "Comparative Analysis Of Cmos Inverter For Low Leakage Power", International Journal of Scientific & Technology Research, vol. 8, pp. 1598-1601, 2019.

[33] Z. Han, “The power-delay product and its implication to CMOS Inverter”, Journal of Physics: Conference Series, pp. 1-11, 2021

[34] M. Saad, S. Mangesh, “Design of low power CMOS inverter using forced NMOS approach”, International Journal of Scientific & Engineering Research, vol. 4, pp. 2413-2418, 2013.

[35] E. Sipos, R. Groza, and L. N. Ivanciu, “Power consumption and noise margin comparison between simple ternary inverter and a binary inverter”, vol. 58, pp. 13-16, 2017.

[36] S. M. Kumar, “Design and Analysis of Low Power Digital Circuits”, International Journal of Applied Engineering Research, vol. 14, pp. 66-71, 2019.

[37] D. Vijayalakshmi and P. C. K. Raja, “Leakage Power Reduction Techniques in CMOS VLSI Circuits – A Survey”, International Journal of Scientific Development and Research (IJSDR), vol. 1, pp. 717-722, 2016.

[38] S. H. Kim, V. J. Mooney III, “Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design”, IFIP, 367-372, 2006.

[39] A.P.S. Rathod, P. Lakhera, A.K. Baliga P. Mittal and B. Kumar, "Performance Comparison of Pass Transistor and CMOS Logic Configuration based DeMultiplexers," International Conference on Computing Communication and Automation (ICCCA- 2015), pp. 1433-1437, May 2015.

[40] A. S. Chakraborty, M. Chanda, and C. K. Sarkar, “Analysis of Noise Margin of CMOS Inverter in Sub-Threshold Regime”, IEEE, 2018.

[41] A.P.S. Rathod, P. Mittal, and B. Kumar, "Analysis of Factors Affecting the Solar Radiation Received by any Region," IEEE International Conference on Emerging Trends on Communication Technologies (ICETCT-2016), Graphic Era University, Dehradun, India, Nov 18-19, 2016.

[42] N. Bako and A. Baric, A low-power, temperature, and supply voltage compensated currently starved ring oscillator. Microelectronics Journal, vol. 44 (12), 1154-1158, 2013.

[43] G. Bansal, S. Agrawal and N. Saxena, “Analysis of ultra-high frequency CMOS ring oscillator and study the supply voltage variation on performance parameter” International Journal of Innovative Research in Engineering and Applied Sciences, 2-2, 2017.

[44] F. Khatoon, T. A. Chandel, Design of Ring VCO using nine stages of Differential Amplifier, International Journal of Research in Engineering and Technology, 120-123, 2014.

[45] H. Masten, Ring oscillator design in 32nm CMOS with frequency and power analysis for changing the supply voltage.

[46] V.Michal, "On the low-power design, stability improvement and frequency estimation of the CMOS ring oscillator", In Radio Elektronika (RADIOELEKTRONIKA), 22nd International Conference, 1-4, 2012.

[47] R. Nayak, I. Kianpoor, and P. G. Bahubalindruni, "Low power ring oscillator for IoT applications", Analog Integrated Circuits and Signal Processing, 93(2), 257-263, 2017.

[48] P. K. Rout and D. P. Acharya, "Design of CMOS ring oscillator using CMODE", In Energy, Automation, and Signal (ICEAS), 1-6, 2011.

[49] A. Shivhare, M. K. Gupta, "Low power ring Oscillator at 180nm CMOS Technology", International Journal of Computer Applications, 0975–8887, 2016.

[50] U. Yodprasit, C. Botteron, P. A. Farine, and A. Heubi, "Shunt-feedback ring oscillator: a new topology for wideband multiphase signal generations", In Radio-Frequency Integration Technology, 78-81, Dec 2007.

[51] A.P.S. Rathod, P. Mittal, and B. Kumar, "Analysis of Factors Affecting the Solar Radiation Received by any Region," IEEE *International Conference on Emerging Trends on Communication Technologies* (ICETCT-2016), Graphic Era University, Dehradun, India, Nov 18-19, 2016.

[52] S. Singhal1, N. Gaur, A. Mehra, and P. Kumar, "Analysis and Comparison of Leakage Power Reduction Techniques in CMOS circuits", IEEE, 936-944, 2015.

[53] S. Hathwalia, S. C. Sankhyan, "Ultra-low power sub-threshold CMOS inverter at 90nm CMOS technology", International Journal of Engineering Research and Applications (IJERA), vol. 3, pp. 2441-2443, Jul-Aug 2013.

[54] B. T. Geetha, B. Padmavathi, and V. Perumal, "Design Methodologies and Circuit Optimization Techniques for Low Power CMOS VLSI Design", IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-2017), pp. 1759-1763, 2017.

[55] V. K. Sharma and S. Soni, “Low power CMOS inverter design at different technologies”, International Journal of Applied Engineering Research, vol. 1, pp. 372-381, 2010.