DESIGN AND PERFORMANCE ANALYSIS OF NOVEL CURRENT COMPARATOR BASED ON EXTREMELY LOW VOLTAGE HIGH COMPLIANCE CURRENT MIRROR

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I, Monika, Roll No. 2K19/VLS/08 student of M. Tech (VLSI & Embedded systems), hereby declare that the project Dissertation titled **"Design and Performance Analysis of Novel Current Comparator Based on Extremely Low Voltage High Compliance Current Mirror"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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Date: Jul 30, 2021

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"Design and Performance Analysis of Novel Current Comparator Based on Extremely Low Voltage High Compliance Current Mirror"** which is submitted by **Monika, 2K19/VLS/08**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This thesis presents the novel structure of the current comparator which embraces the Extremely Low-Voltage High-Compliance Current Mirror (ELVHC CM) as the current differencing stage. The current comparator is a elementary unit of current mode applications. Their performance is found better than the voltage comparator in the literature. In the literature, the very first current comparator shows the 10 ns delay with higher resolution. Later many designs were proposed with specific advantages per application. In the current comparator, the current mirror (CM) plays a crucial role. CM provides the current differences that have to be measured.

In this thesis, six types of CM have been discussed, analyzed, and simulated. Name of all these CMs are Simple current mirror, Wilson current mirror, Improved Wilson current mirror, Cascode current mirror, ELVHC CM, and BDQFG FVF CM. The first four CMs are the basic types of CM structures and the remaining two CMs are the advanced topology of CM. The significant parameters of CM which describe the overall performance of CM are Current transfer characteristics, PER, Compliance voltage, Bandwidth and input/output resistance. For basic CM structures i.e. Simple current mirror, Wilson current mirror, Improved Wilson current mirror, and Cascode current mirror, Current transfer characteristics, PER, Compliance voltage, and output resistance. All these basic four current mirror structures have been simulated on various technology nodes such as CMOS 180 nm, 90 nm, 45 nm, and FinFET 18 nm on the Cadence Virtuoso simulator and then compared based on technology node and the topology. If a comparison of basic four CM has seen technology-wise then 180 nm shown better performance among all technology nodes. Whereas, Simple CM shows 11.25% of PER for 180 nm technology node while 74.62% of PER is observed for 90 nm technology node, 12.58% for 45 nm, and 13.17% for FinFET 18 nm. Similarly, 0.1 V output compliance voltage is observed for all technology node of Simple CM and 45 nm technology node Simple CM depicted 199 MΩ output resistance which is greatest among all technology node pf Simple CM. Talking about Wilson CM 180 nm technology node shown best performance among all technology nodes as -16.17% of PER is spotted. Furthermore, minimum compliance voltage 0.2 V is seen for 90 nm technology node, and 168 MΩ of highest resistance is noticed for FinFET 18 nm technology node of Wilson CM. Improved Wilson CM experience similar

resistance as Wilson CM for all technology nodes. While mirroring accuracy is found quite similar of Improved Wilson CM and Cascode CM. But for Cascode CM 180 nm technology node shown lower output resistance and higher compliance voltage which is not good in practice, although FinFET Cascode CM depicted 293 MΩ of output resistance.

Afterward, two advanced current mirrors named ELVHC CM and BDQFG FVF CM are discussed, analyzed, and simulated on Cadence Virtuoso Simulator. Their small-signal analysis has been done with mathematical equations and Monte Carlo analysis is also carried out. Transfer characteristics, PER, and Output compliance voltage are calculated for these two CMs. Moreover in BDQFG FVF CM, bulk driven quasi floating gate and flipped voltage follower techniques and their working as been discussed. Based on the comparison of both CM it is concluded the ELVHC CM is better than BDQFG FVF CM. Also, it is observed that at 200 μA input current ELVHC CM depicted 0.03% of PER. Moreover, BDQFG FVF CM shown 0.12 V of minimum output compliance voltage while ELVHC CM presents 0.091 V.

In conclusion, it is noticed that ELVHC CM's performance is better than BDQFG FVF CM. Based on this statement a novel design of the current comparator has been proposed which comprises ELVHC CM as a current differencing stage. To find out the workability of the proposed design, a new proposed comparator is analyzed and simulated on a 180 nm technology node and compared with BDQFG FVF CM based current comparator. Where, majorly three parameters are calculated such as propagation delay, power, and PDP. It is noticed that both comparators have a resolution of 5 nA. Further, the proposed design depicts 74.2% and 30.2% propagation delay and power dissipation respectively less than BDQFG FVF CM based comparator. All these analyses show that the current comparator based on ELVHC CM's performance is superior.

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LIST OF ABBREVIATIONS

ADC- Analog to Digital Converter

DAC- Digital to Analog Converter

PSRR- Power Supply Rejection Ratio

ELVHC CM- Extremely Low Voltage High Compliance Current Mirror

BDQFG FVF CM- Bulk Driven Quasi Floating Gate Flipped Voltage Follower Current Mirror

CM – Current Mirror

PER– Percentage Error Ratio

PDP- Power Delay Product

MOS- Metal Oxide Semiconductor

CMOS- Complementary Metal Oxide Semiconductor

FinFET- Fin Field Effect Transistor

MOSFET- Metal Oxide Semiconductor Field Effect Transistor

SHCCM- Self-biased High swing Cascode Current Mirror

CCM- Cascode Current Mirror

GD-QFB- Gate Driven Quasi Floating Bulk

LSFVF- Level Shifted Flipped Voltage Follower

CHAPTER 1

INTRODUCTION

A basic and primary unit of the analog-to-digital block is the comparator, which requires maximum power. Hence a improvised design for the comparator is need. A comparator's basic work is to compare two input entities (voltage or current) and give the result in the form of a digital signal. A simple voltage comparator can be realized by using an op-amp, but the power consumption and dc offset errors are found to be high in voltage comparators. Whereas the current comparators got low offset errors and low power consumption when compared to voltage comparators. Also, current comparators got a small area as the size of their transistors is small.

The main task of a current comparator is to detect which one of the current is greater (Iin or Iref). It represents the current difference in form of Voltage. This output voltage is presented in a digital signal (pulse waveform). Parameters that majorly define the performance of the comparator are propagation delay, power dissipation, and power delay product (PDP). The current comparator circuit contains the current difference stage, gain stage, and output stage. To enhance these parameters current difference stage plays a major role and this stage is consists of a current mirror.

The current mirror is a basic element in analog electronics. The current mirror (CM) is an accomplished and significant part of analog circuits. It produces a mirror image of an input current at output node of high resistance value. A major purpose of the current mirror as the active load, current amplifier, current source, and used as biasing in operational transconductance amplifiers (OTAs), operational amplifiers (Op-amps), operational mirrored amplifiers, analog filters, current conveyors, current- feedback op-amps, digital-to-analog converters, and analog-to-digital, etc. Thus, CM plays a crucial role in these integrated circuits. Performance criteria of current mirrors which are also essential are; bandwidth, input/output compliance voltage, output resistance, input resistance, and accuracy. The parameter accuracy is defined as the percentage error ratio means a precise copy of the input current to the output current, whereas, the input/output compliance voltage is represented as the maximum voltage at the output of a current source while it attempts to produce the desired matched current. The utmost performance requirement of the current mirror includes a high accuracy which is essential for many applications like

bio amplifiers, implantable microstimulators, and biomedical circuits. However, Bluetooth filters, operational amplifiers, universal bi-quad filters, and biomedical circuits require low compliance voltage CMs and are used in low voltage applications. Current mirrors that have high output resistance and low input resistance are used to minimize the loading effect and this proficiency can be used to improve PSRR, DC gain, and common-mode rejection ratio which is a crucial factor for differential input pairs. Further, current mirrors with high bandwidth are required in high-speed circuits such as high-speed current-mode amplifiers, current steering D/A converters, etc. Many CMs have been reported earlier in the literature with improvements of different parameters. Low compliance voltage has been achieved in Low voltage cascode CM, high swing cascode current mirror, etc. Whereas, higher output resistance has been seen in Active Feedback CM, regulated cascode CM, self-cascode MOSFET CM, etc.

1.1 Motivation

Today, where energy conservation is a major concern in every field, significant efforts are made towards low voltage and low power techniques for high speed, portability, higher resolution, and energy-saving applications. The evolvement of low-voltage, low-power technology is essential nowadays due to the demand for these durable and portable devices in life. With this trend, ADC and DAC can be seen as a major part of most of the electronics devices and digital electronics especially. Now, as growth in this field increasing day by day, it is necessary to make them handy, durable, portable, and cost-effective. Therefore, most of the research is done in this field and it can be done by reducing the feature size, modified the already existing structures, lowering the power supply voltage, etc. Thus, it can be said low-voltage; low-power design methodologies are desirable in modern technologies.

A current Comparator is a fundamental unit of Signal conversion (ADC/DAC). And in today's world digital technology getting used in every field. Portability and long-lasting battery power are favorable choices for all users. In modern applications, high resolution is required. All the reported literature focusing on low power comparators and improved resolution of the current comparator. As low power reduces the energy, voltage, heating, etc. and resolution means to give a fast response to minor changes in input (response time) and make the device compatible.

Continuing the trend, this thesis also presents the low power dissipation current comparator with high resolution means low response time to give the output. The comparator comprises the advanced structure of CM to improvise the performance.

1.2 Objective

This work aims to make a novel structure of the current comparator which uses low-voltage, low-power for applications such as ADC, sequence detector, Schmitt trigger, etc. In this comparator an enhanced current mirror i.e. "Extremely Low-Voltage, High-Compliance Current Mirror" is used for the current differencing stage, which enhances the performance of the comparator. This is done by connecting two current mirrors in parallel in the current differencing stage of the current comparator.

- Analyzing and discussing different current mirrors at different technology nodes. This will give us the idea about working of the current mirror and will help to improvise the advanced structure of CM. This will also benefit to find out the trend of CM using different technology node that what will be the performance of CM.
- Performance analysis is done for advanced CM structures to find out which one gives the immense better performance. Also performed a mathematical small-signal analysis of these two structures. Compared and tabulated their results to conclude their working ability for low-power applications.
- Designing and analyzing the novel current comparator structure which ensembles the core structure of [47] and uses the current mirror from [10] for the current differencing stage.

1.3 Methodology:

The proposed current comparator is consists of three-stage i.e. current differencing stage, gain stage, and output stage. The first stage comprises the current mirror. In this dissertation, the basic concept and basic current mirror structures have been described. Also, a new enhanced current mirror named "Extremely low voltage high compliance current mirror" and "Bulk driven quasi floating gate flipped voltage follower current mirror" structure is detailed, and as it is reported that current mirror's accuracy plays a major role in the operation of current comparator. Hence, the best performance given the current mirror is used in the current differencing stage. Furthermore, a various parameter of a current mirror has been characterized and studied. The four basic CM structure named

as Simple, Wilson, Improved, and Cascode is verified over different technologies including 180 nm, 90 nm, 45 nm and 18 nm FinFET. Other two advanced current mirror has been simulated at 180 nm CMOS technology and used same technology node in the comparator. An analysis of ELVHC CM and BDQFG FVF CM Monte Carlo analysis is also used to observe their performance on different temperature and threshold voltages. After this, the ELVHC CM is implemented in the Current Comparator and analyzed this new structure.

1.4 Organization of Thesis:

This thesis has been organized into 7 chapters. Introduction of the current comparator, a current mirror is categorized in Chapter 1. Further, Chapter 1 includes the motivation, objective, and methodology. Chapter 2 is related to the literature review and the technology gap. Chapter 3 deals with a discussion and analysis of different current mirror topologies and their parameters. Chapter 4 presents an analysis of two advanced current mirror structures, their parameters, and their performance. It also ensembles the Monte Carlo analysis and small-signal analysis. Chapter 5 illustrates the proposed comparator design, its study, and analysis. Conclusion and future scope are presented in Chapter 6.

- CHAPTER 1- Includes a brief introduction about current comparator, current mirror, their application fields, how they work on low power and low voltage. Objective, motivation, methodology, and organization report are described in this chapter.
- CHAPTER 2- This chapter described the previously done research work on Current Comparator and Current Mirror. Reported research work stated the slightly higher power dissipation and PDP. Different kind of CM topologies has been reported in the literature. Different kinds of techniques and devices have been used in CM to improvise the performance of CM such as negative-positive mutually controlled feedback, Bulk driven MOS, Quasi floating gate, Self-biased MOS, current-mode amplifier, voltage mode amplifier, etc.
- CHAPTER 3- This chapter explains the four basic CM structures, their working, and parameters (Current transfer characteristics, PER, compliance voltage, and output resistance). All four CM were analyzed at four different technology nodes such as CMOS 180nm, 90 nm, 45 nm, and FinFET 18 nm. Then their parameters have been compared based on their structures and technology node.

- CHAPTER 4- Description and parametric analysis of advanced CM i.e. ELVHC CM and BDQFG FVF CM are done in this chapter. Moreover, Monte Carlo and Small-signal analysis for the deep study of these two CM is done also. Transfer characteristics, PER, and compliance voltage are calculated for these structures.
- CHAPTER 5- The proposed design is illustrated in this chapter. This chapter includes the structure description, it's working, and also previously reported comparator based on BDQFG FVF CM is compared with proposed design to capture the superior performance of the proposed designed comparator. Major parameters i.e. propagation delay, power dissipation, and PDP are calculated for the proposed current comparator design.
- CHAPTER 6- The conclusion and future scope of the proposed current comparator is written in this chapter.

In the last, publication list is mentioned and references are listed which provided the broad idea and concept of the current mirror and current comparator.

CHAPTER 2

LITERATURE REVIEW

2.1 PREVIOUS REPORTED WORK:

D. A. Freitas, K. W. Current [1], Proposed the very first current comparator. It uses a high impedance current mirror for amplification of small differences of input current and converts it to voltage entity. But due to its high output resistance the frequency performance getting worse when an inverter is used for its full rail-to-rail swing.

H. Traff [2], presented the current comparator with higher accuracy. It uses the source follower input stage to provide low input resistance and feedback to the gates. It also uses positive voltage feedback to improve the gain at the input stage. It implements the CMOS inverter at the last stage to get the rail to rail swing in output voltage. It has an accuracy of 1µA and a propagation delay of 4 ns. But it has disadvantages also i.e. input voltage which is fed to a positive feedback inverter. This voltage doesn't have a rail-to-rail swing and due to this nonzero DC power dissipation is caused in the circuit.

A. T, K. Tang, C. Toumazou [3], Proposed the current comparator with higher speed compared to [1] and [2]. It improves the speed/power ratio at a lower input current range. It shows an 11 ns propagation delay and 1.4 mW power dissipation at 0.1 µA input current. Like all, it has also the disadvantage of increased power dissipation and circuit complexity.

A. Rodr´ıguez-V´azquez, R. Dom´ınguez-Castro, F. Medeiro, M. Delgado-Restituto [4], depicts high resolution current comparator. This current comparator includes feedback structures that provide self-tracking and gives a higher resolution (<1 pA). Furthermore, it has a moderately complex circuit.

L. Ravezzi, D. Stoppa, G. F. Dalla Betta [5] is a modification of Traff's [2] current comparator with little complexity. It shows greater performance than Traff's comparator such as the time delay is found four-time lesser than Traff's comparator and also it shows high input current sensitivity. But this advantage comes at the cost of lower swing output voltage. Also, the dynamic performance is compared to [3].

B. M. Min, S. W Kim [6] present a high-speed current comparator with a small area that consists of resistive feedback. This paper compared the results with [2] and [3] where the speed of the comparator is found to be 7 ns while the conventional comparator shows 40 ns. Further power consume by the proposed comparator is 0.45mW and PDP is 3.15 pJ. It is concluded that a 400% improvement is observed in this comparator.

L. Chen, B. Shi, C. Lu [7] present the current comparator with higher speed and lower power. It incorporates CMOS complementary amplifiers, CMOS inverters, and resistive load amplifiers. Also, it includes the MOS resistor as negative feedback in the CMOS complementary amplifier which resolves the voltage swing delay time issues of the comparator. It compares the result with [2] and [3].

R. Chavoshiani, O. Hashimpor [8] proposed the current comparator which comprises of current conveyor circuit and gives high speed and small response time results in wideband application. It provides a propagation delay of 0.4 ns and 158 µW power dissipation. This circuit includes second-generation current conveyors (CCII) to improve the parameters of the current comparator. In CCII current mirror and differentials pairs are used by feedback connections.

D. Banks, C. Toumazou [9] this paper presents the current comparator circuitry which is much similar to and modification of Traff's [2] comparator. The main idea behind this paper is to lower the consumption of power while maintaining the speed of the comparator. The positive latched feedback is used in the proposed comparator. It is found that the DC quiescent current with this latched feedback is 10s of femtoampere.

K. Monfaredi, H. F. Baghtash [10] represents the novel structure of current mirrors for low power, low voltage applications. This structure establishes the cooperative positive-negative local feedback to improvise the compliance voltage of the current mirror. This current mirror depicts the higher accuracy in current transfer characteristics and shows the PER of 0.4%. also, the output resistance is experienced higher for this proposed circuit i.e. 121.36 GΩ which is a notably high value. Furthermore, the output compliance voltage is seen at 0.038 V.

S. J. Azhari, G. Nickhah [11] proposed the novel structure of current mirrors for low power, low voltage applications. Although it uses a slightly higher power supply voltage i.e. 1.2 V than [10]. But the output resistance found in this current mirror is in TΩ and the

minimum output voltage i.e. output compliance voltage is 91 mV. For improvement of frequency performance, an active resistor is implemented, and also amplifier is designed using a transistor. For operating at a lower current the circuit uses a higher bias current for the amplifier.

M. Bchir, I. Aloui, N. Hassen [12] illustrates the current mirror which uses bulk driven quasi floating gate technique for lower power consumption. It depicts higher output resistance of 9.5 GΩ and minimum PER 0.2%. Also, it can work on 0.4 V supply voltage with 3.5 % PER. This current mirror provides low input impedance due to the use of negative feedback. Instead of all these advantages, high power consumption is still an issue for this structure.

M. Doreyatim, M. Akbari, M. Nazari, S. Mahani [15], have proposed the current mirror for low voltage application based on gain boosting structure with high output resistance. It uses bulk driven diode-connected transistor at the input side to eliminate the limitation of the threshold voltage for low headroom voltage. To abolish the limitation of threshold voltage in rail-to-rail swing in circuit, a current amplifier is attached in gain boosting structure. Further, one more gain boosting structure is used for higher output resistance which comprises a voltage-mode amplifier. In this paper, 66.3 Ω and 10.5 G Ω resistance are observed for the input and output sides respectively. Moreover, PER is depicted as very low such as -0.085% to 0.075%.

S. J. Azhari, H. F. Baghtash, K. Monfaredi [16], In this paper a novel structure of CM is presented which provides high compliance voltage, higher accuracy, high output resistance for low power application. This structure includes negative and positive feedback which is mutually controlled to provide higher values of compliance voltage, higher output resistance with higher accuracy. Minimum input/output compliance voltage is observed of 0.058 and 0.055 V respectively while using CMOS technology. Whereas, 34.3 GΩ and 13.3 Ω were observed for output and input resistance respectively while 210 MHz cutoff frequency for this CM is experienced.

B. Aggarwal, M. Gupta, A. K. Gupta [18], this paper proposed a novel Self-biased high swing cascode current mirror (SHCCM) for low voltage application, higher output resistance. This CM replaces the conventional passive resistance with an active MOS transistor to improvise the performance. For deep analysis of this CM small-signal analysis has been done. Although this proposed CM depicts moderate values of output resistance

such as 578 KΩ and 2.73 KΩ for input resistance. Also, the comparison has been carried out in this paper with conventional gate-driven CCM and Bulk-driven CCM.

N. Raj, A. K. Singh, A. K. Gupta [19], in this paper high-performance, self-biased, cascode bulk-driven CM is proposed for low voltage application. In this quasi floating gate, MOS transistors are used with bulk-driven technique to improve the performance of CM. The proposed CM consists of four bulk-driven transistors in which two transistors are bulk-driven quasi floating gate transistors. It also provides input/output resistance in KΩ such as 0.306 KΩ and 165 KΩ respectively. Also, the minimum output compliance voltage is 0.10 V for this proposed CM in this paper.

N. Raj, A. K. Singh, A. K. Gupta [20], proposed a high-performance current mirror that uses quasi-floating techniques to improve the accuracy. In this proposed structure the bulk is made quasi-floating then connected to the gate terminal. That's how Gate Driven Quasi Floating Bulk (GD-QFB) technique is proposed. Then this technique is used for three different CM to observe the improvement. Where GD-QFB CCM presents 1.35 MΩ, GD-QFB SHCCM shows 46 KΩ and GD-QFB CM presents 20 GΩ output resistance. All this simulation is done on 180 nm CMOS technology in this paper.

B. Aggarwal, M. Gupta, A. K. Gupta, [22] presents the paper which elaborates the CM based on level-shifted flipped voltage follower (LSFVF CM) for low voltage application. The level shifter is added in a feedback path of CM. The input resistance of the proposed CM is observed of 26 Ω while output resistance is 562 KΩ. All the simulation is done by using a 1 V power supply. The power experienced by this CM at 50 μA is 402.5 μW.

2.2 TECHNICAL GAP

After observing and analyzing all the reported work, there is a technical gap. The reported current comparator shows higher power dissipation due to structural issues. Also, some starting reports of current comparators have no gain stage or lower gain stage. They also had less accurate current mirrors in a current differencing stage. Further, CM studies shown in reported work depict that they have less accuracy, higher compliance voltage, inappropriate resistance values cause issues in low power, low voltage application. Also, the lower technology node in CM shows poor performance over the higher technology node. Using FinFET in basic CM topologies getting degraded performance.

Keeping in view all these issues, this thesis proposed a new current comparator structure with a previously reported CM structure whose performance is well analyzed and discussed. This proposed comparator shows very low power with lower resolution and improved PDP.

CHAPTER 3

CURRENT MIRROR

This chapter will describe the basic elements of the current comparator i.e. current mirror. The current difference stage is comprised of two CM as can be seen in Fig. 3.1. Its working can be explained as this circuit mirror the current from the input current source irrespective of any variation in the input source it will provide the constant and accurate current to the load. Now following section will demonstrate the basic structures of CM and how they work and provide the basic idea behind the topology. Further, two more novel structure of CM is introduced in this section.

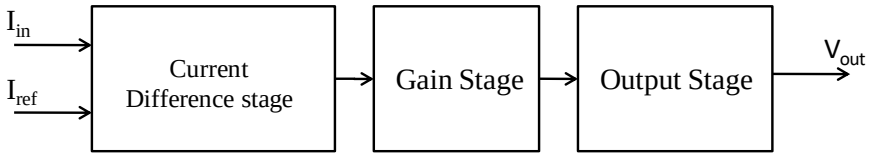


Fig. 3.1 Simplified block diagram of the current comparator

3.1 Different Current Mirror Topologies

This section is describing different current mirror basic structures. There four basic structure which is used at initial level in research i.e. simple (Conventional CM), Wilson current mirror, Improved Wilson current mirror, and Cascode current mirror.

3.1.1 Simple CM

Fig. 3.2(a) depicts the structure of a simple current mirror; all the structures are based on a well-defined MOSFET CM, which is already developed in the literature. The working of the current mirror depends on the applied voltage and their process parameters such as aspect ratio. Hence, in Fig. 3.2(a) both transistors are identical and their length should be equal (L1=L2) for mirroring. Here, the gate-source voltage of M1 and M2 is equal hence the channel current will be equal. For the proper mirroring operation of the circuit, transistors should remain in the saturation region.

Current mirror structures can be made by adding two transistors by their gate and the input side transistor should be diode-connected and the output side transistors will get the required gate-source voltage by this diode-connected transistor. For the current mirror to be working as an amplifier the aspect ratio of M2 should be greater than M1 [13, 14].

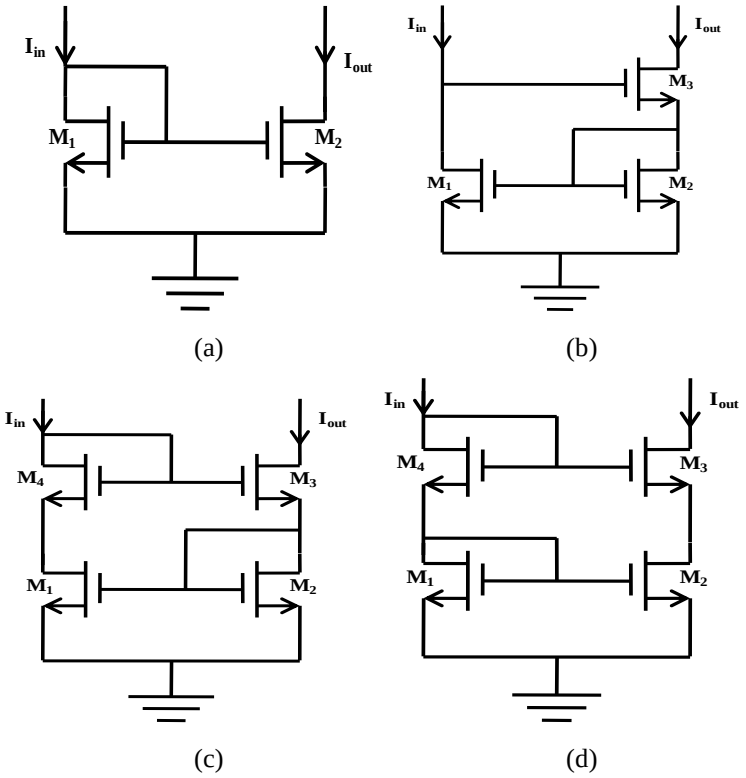


Fig. 3.2 Basic CM topologies (a) Simple, (b) Wilson, (c) Improved Wilson, and (d) Cascode

3.1.2 Wilson CM

To modify the performance of simple current mirror Wilson CM is demonstrated (Fig. 3.2(b)). It consists of three transistors where one of them is a diode connected to maintain the gate-source voltage for mirroring. Transistor M3 is implemented in such a way that it produces a shunt-series type of negative feedback. Due to this feedback higher output resistance can be seen in Wilson CM. But this topology comes up with a deficiency of large compliance voltage which should be as low as possible. The voltages are given as:

$$V_{\text{out min}} = V_{\text{Th}} + 2V_{\text{DS sat}} \tag{3.1}$$

$$V_{\text{in min}} = 2V_{\text{Th}} + 2V_{\text{DS sat}} \tag{3.2}$$

Where $V_{\text{out min}}$ and $V_{\text{in min}}$ are the minimum output and input voltage. V_{Th} represents the threshold voltage of the transistor and its minimum drain-source voltage for maintaining it in the saturation region is given as V_{DSsat}. One more drawback of Wilson CM is that it has not equaled the drain-source voltage of transistors M1 and M2. This is the result of channel length modulation and it causes lesser mirroring accuracy. The following section will describe the next improvised version of Wilson's current mirror which reduces the drawback of the Wilson CM [13, 14].

3.1.3 Improved Wilson CM

To improve the performance of a Wilson CM many works of literature have developed various techniques and resulting in an Improved Wilson current mirror, as shown in Fig. 3.2(c). This topology is depicted as four transistors with input side transistors working in diode-connected mode and transistors M3 and M4 provide the precise current gain by doing the equalization in V_{DS} of base transistors M1 and M2. While the resistance and compliance voltage would be the same as Wilson current mirror. Output resistance can be indicated as:

$$r_{out} \approx \frac{g_{m1} r_{o1} g_{m3} r_{o3}}{g_{m2}} \tag{3.3}$$

where g_m is transconductance and r_o is the output resistance of the transistor.

A conclusion can be made here that an increased number of transistors results in higher parasitic capacitance [13, 14].

3.1.4 Cascode Current Mirror

Cascode CM is further designed to increase the output resistance, minimize the compliance voltage, and enhance the accuracy, as illustrated in Fig. 3.2(d). This technique increased the accuracy which is the result of a difference in output and input voltage. And also V_{DS} of M1 and M2 are balanced by transistors M3 and M4. Its output resistance is shown as:

$$r_{out} = r_{o3} + r_{o2}(1 + r_{o3}(g_{m3} + g_{mb3})) \tag{3.4}$$

Cascode CM is considered as a cascoded version of simple CM. For proper working of Cascode CM drain-source voltage of M2 should follow the V_{DS} of M1. Transistor M2 and M3 should be maintained in the saturation region for this purpose. And this would happen only if $\frac{(W/L)2}{(W/L)1} = \frac{(W/L)3}{(W/L)4}$. The compliance voltage is given as in Equation (3.5):

$$V_{outmin} = 2V_{DSsat} + V_{Th} \tag{3.5}$$

Here observable point is that Wilson CM, Improved Wilson CM, and Cascode CM have similar compliance voltage. In Cascode CM, based on the structure asymmetry of input/output voltage and channel length modulation can't affect the performance of the CM, only process variation (like length, width, V_{Th}, etc.) may affect. Hence care should be taken during layout and fabrication. Further, M1 and M2 can be optimized for better

matching accuracy, whereas M3 and M4 can be sized for a higher range of transconductance. Moreover, at present many current mirrors with various techniques to improvise different parameters for specific applications like bulk-driven quasi-floating gate FVF CM, low-voltage gain boosting CM, extremely low-voltage and high-compliance CM, novel ultra-low-power, low-voltage, ultra-high-output resistance, and high bandwidth CM, etc. have been developed. Some of these current mirrors have one or two specific parameter improvements and some have average performance [10-15].

3.2 Performance Analysis of CM's Basic Structures

Illustrated current mirrors in Fig. 2(a-d) are simulated on 0.18 µm, 90 nm, 45nm, and 18nm technology nodes employing the power supply voltage of 1 V. The input current has taken for DC analysis as 10 µA and swept for 0-500 µA range. Similarly, for DC analysis output voltage is taken to have values of 1 V. For compliance voltage calculation, the output voltage is swept for 0-5 V range. Calculation of output resistance carried out at AC analysis within 1-100 GHz range as a log scale. The aspect ratio for different technology is 5 µ/250 n, 2µ/100n, 2µ/45n, and L=18 nm for 180 nm, 90 nm, 45 nm, and 18 nm technology respectively.

3.2.1 Current Transfer Characteristics

Current transfer characteristics show the plot between input and output current and also show the pattern that how a current mirror will track the input current and gives a better result. The current transfer characteristics of the entire given CM are shown in Fig. 3.3(a-d). At 180 nm technology node simple current mirror gives overall better performance followed by 18 nm, 45 nm, and 90 nm technology node as shown in Fig. 3.3(a).

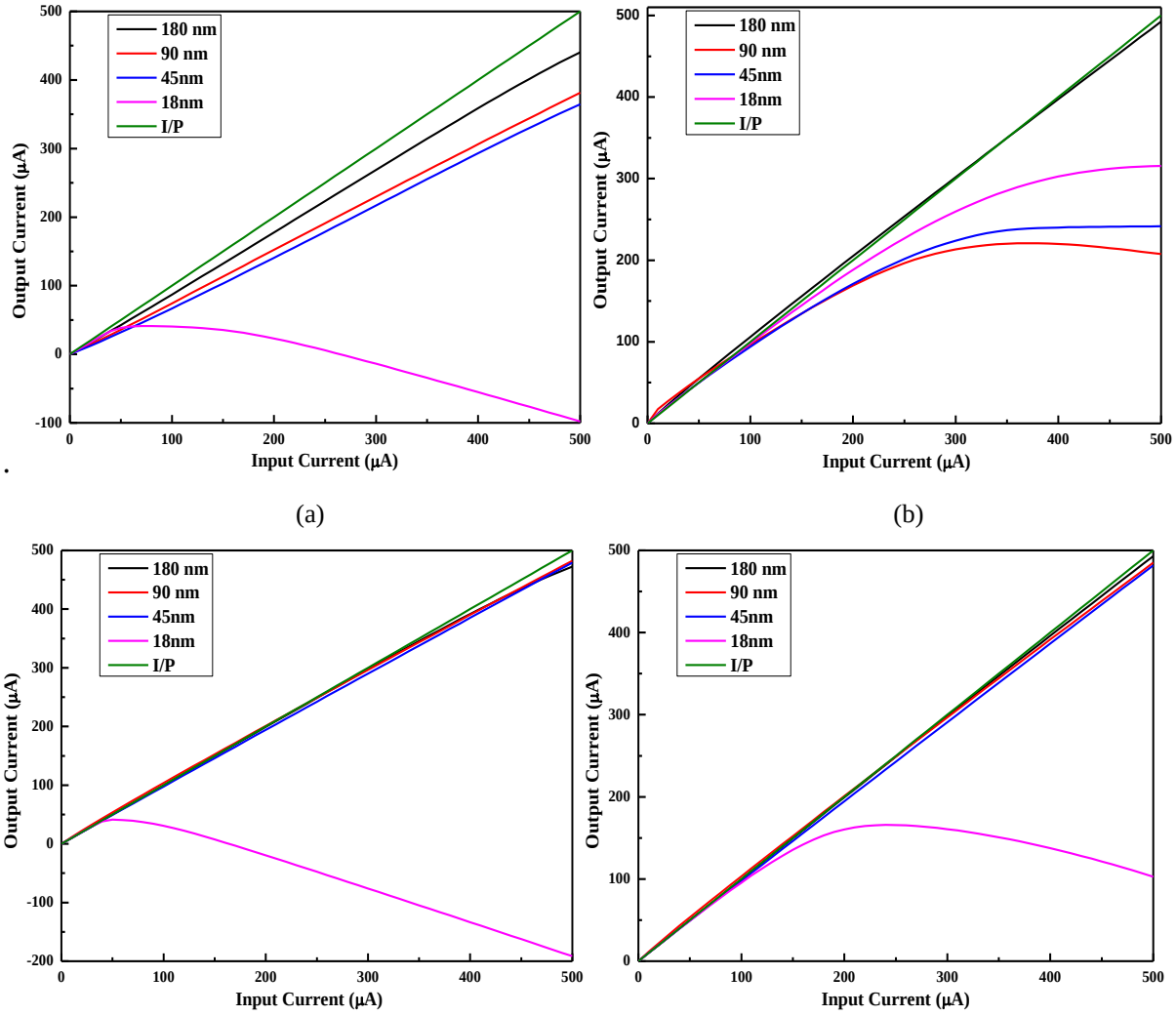


Fig. 3.3 Current Transfer Characteristics of (a) Simple, (b) Wilson, (c) Improved Wilson, (d) Cascode

For a small range of input current, all technology nodes show better accuracy but after a certain range, they start to degrade. At I_{in}= 10 µA, 180 nm CM shows 12.1 µA output current which is near to the input current whereas at 90 nm output current is found 75% more to the input current, but at 45 nm and 18 nm, CM gives only 13% more to the input current. Fig. 3.3(b) represents the characteristics for Wilson CM; in which 180 nm depict higher accuracy over the range than 90 nm, 45 nm, and 18 nm. Wilson CM using 180 nm technology node shows 17.6% of input current lesser value while 18 nm demonstrate 16.2% less from input current. For more accuracy, Improved Wilson is developed and its characteristics plot portrait in Fig. 3.3(c). It is found that all technology nodes except 18 nm, displayed the highest accuracy, and produced similar values. Similarly, Cascode CM

presents the highest accuracy among all current mirrors. At input current 10 µA it shows a similar trend as given in Improved Wilson current mirror as shown in Fig. 3.3(d).

3.2.2 PER

To find the error in accuracy PER is calculated by using this equation $\frac{I_{out}-I_{in}}{I_{in}} \times 100\%$, where I_{out} is taken at the output node of CM. For PER, all plots are illustrated in Fig. 3.4(a-d). The lowest error is found in 180 nm at the complete range of input current in a simple current mirror, as depicted in Fig. 3.4(a). But at I_{in}= 10 µA, a low error of12.58% is seen in 45 nm then after a certain value of input current, the error is increased. Whereas 90 nm technology exhibits excessive error over the complete input current range and 180 nm shows 62% more error from 45 nm technology.

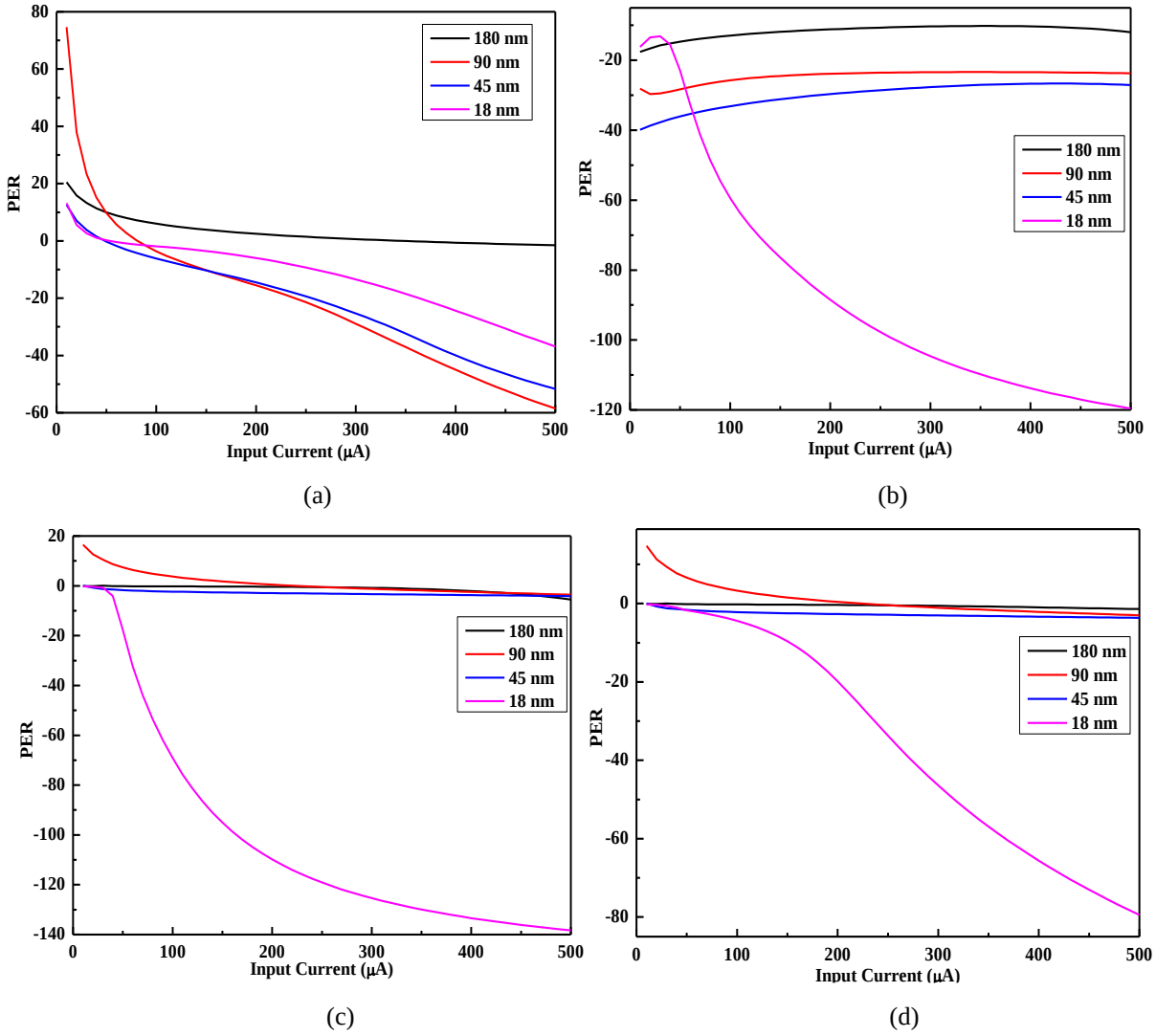


Fig. 3.4 PER plot of (a) Simple, (b) Wilson, (c) Improved Wilson, (d) Cascode

Further, 18 nm FinFET indicates a 4.68% extra error from 45 nm MOSFET. To summarize, a manner for PER 180 nm exhibits great performance for the large current range. PER characteristics for Wilson CM are illustrated in Fig. 3.4(b). It can be seen that for a very small input current 18 nm FinFET gives a small error and then after a particular input current, its PER plot starts decreasing i.e. the error is going to achieve a higher value. Among the four of them, technology 180 nm demonstrated fewer errors over the complete range. At I_{in}= 10 µA 45 nm shows -39.9 % error while 90 nm depict -28.13 % error. Fig. 3.4(c) represents the PER characteristics for Improved Wilson CM, in which 180 nm, 90 nm, and 45 nm show a very less error ratio over a range. At a particular value of I_{in}= 10 µA, 45 nm CM presents the lowest error i.e. 0.012% but after few values of input current, it slightly increases. Whereas in starting values of input current, 180 nm CM shows 7 times higher error at I_{in} = 10 µA, while at the same value 18 nm FinFET CM displayed -0.18% error. Moreover, 90 nm exhibits poor performance at this particular value. A similar trend can be seen in Cascode current mirror, it expresses comparable values as shown in Fig. 3.4(d).

3.2.3 Compliance Voltage

The minimum output voltage to maintain the output leg of the current mirror in saturation for the perfect operation of matching is called compliance voltage. Hence, $V_{out}=V_{CV}=V_{GS-out}=V_{DS-out}$, which is required as low as possible for a higher compliance range (here V_{CV} is a compliance voltage). The output compliance voltage for a simple CM is shown in Fig. 3.5(a), where it is found that due to channel length modulation it has a higher compliance voltage. 180 nm current mirror demonstrates 0.1-0.5 V and a similar value can be seen in 45 nm, 18 nm, and 90 nm. Fig. 3.5(b) depicts the characteristics for Wilson CM which expresses high compliance voltage in 180 nm and 18 nm where the output transistor enters in saturation voltage of 0.6 V. Further, 45 nm current mirror presents 16.6% less value from the highest compliance voltage of 180 nm and 18 nm. For 90 nm CM, compliance voltage is found at 0.4 V. Fig. 3.5(c) represents the compliance voltage plot for Improved Wilson CM. Although90 nm shows the compliance voltage of 0.3 V to maintains the MOSFET in saturation. After a few voltages current increases dramatically. For 180 nm, 45 nm, and 18 nm, compliance voltage is obtained the same as Wilson CM. Cascode CM's compliance voltage is illustrated in Fig. 3.5(d). The lowest compliance voltage is found

for 90 nm i.e. 0.3 V, while a 33.33% increment in 180 nm and 66.66% increment in 45 nm and 18 nm have been observed.

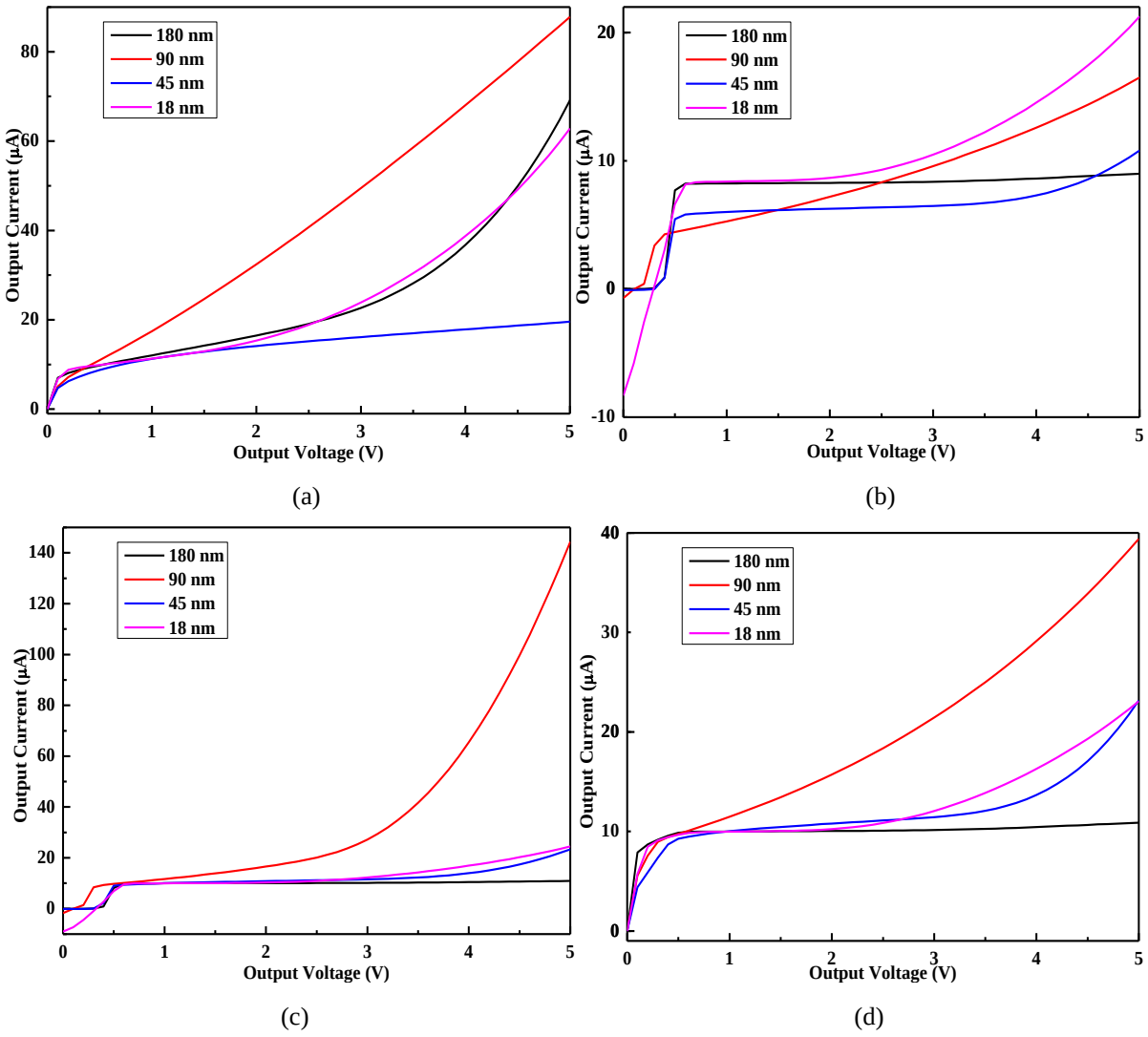


Fig. 3.5 I_{out} Vs V_{out} plot for compliance voltage of (a) Simple, (b) Wilson, (c) Improved Wilson, (d) Cascode

3.2.4 Output resistance

Here, output resistance is reciprocal of output current as output voltage has a value of 1 V and it has been plotted with frequency using AC analysis. For all current mirror topologies, the resistance vs. Frequency plot has been illustrated in Fig. 3.6(a-d). Fig. 3.6(a) shows the resistance for a simple current mirror, in which the highest resistance, 199 MΩ, is observed at 45 nm, where its 70.40% decrement in resistance can be seen in 18 nm. 180 nm and 90 nm represent the output resistance of 45.5 MΩ and 29.3 MΩ respectively.

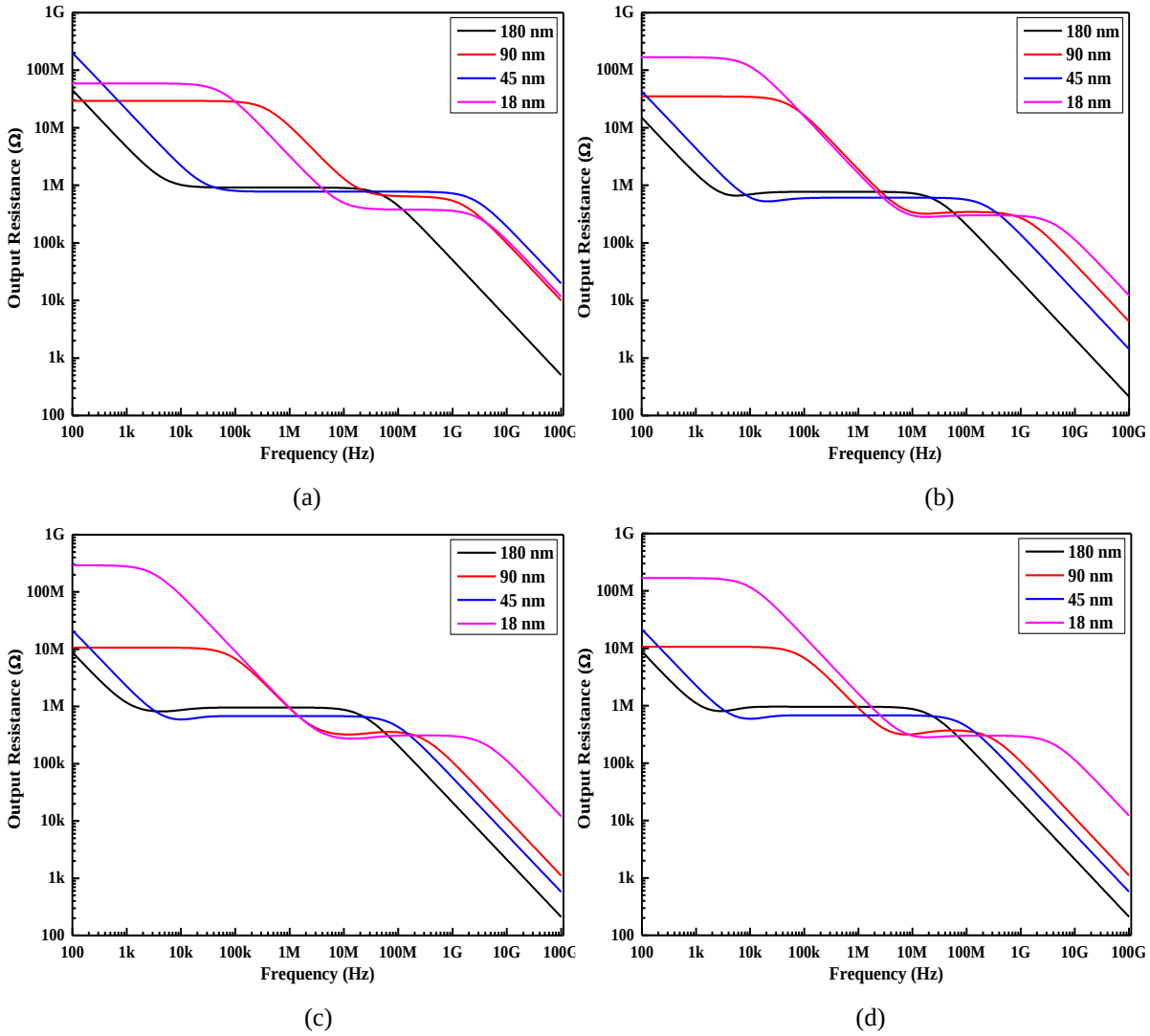


Fig. 3.6 Output resistance vs. frequency plot of (a) Simple, (b) Wilson, (c) Improved Wilson, (d) Cascode

Wilson current mirror's highest output resistance has been obtained at 18 nm, which is 168 MΩ, as shown in Fig. 3.6(b). Moreover, ¼ of 18 nm resistance is observed in the 45 nm current mirror. Further, 180 nm and 90 nm current mirrors exhibit 15.1 MΩ and 35 MΩ resistances, respectively. Cascode CM's output resistance has been plotted in Fig. 3.6(d). In Cascode CM lowest resistance has been observed in 180 nm CM which gives the value of 8.83 MΩ and its nearly 20% increment is obtained in 90 nm CM, whereas, highest output resistance has been displayed by 18 nm CM, i.e. 293 MΩ and 21.2 MΩ has been shown in 45 nm.

Table 3.1- Comparative results for different technology nodes for different CM structures

Topology	**Parameter**	**180 nm**	**90 nm**	**45 nm**	**18 nm**
Simple CM	Mirroring accuracy*	Better	Poor	Poor	Poor
	PER (%)[a]	11.25	74.62	12.58	13.17
	Compliance Voltage (V)	0.1-0.5	0.1-0.3	0.1-0.5	0.1-0.5
	Output Resistance (MΩ)	45.5	29.3	199	58.9
Wilson CM	Mirroring accuracy*	Better	Good	Good	Poor
	PER (%)[a]	-16.17	-28.13	-39.9	-17.62
	Compliance Voltage (V)	0.4-0.8	0.2-0.6	0.4-0.7	0.5-0.9
	Output Resistance (MΩ)	15.1	35.7	42.4	168
Improved Wilson CM	Mirroring accuracy*	Better	Better	Better	Poor
	PER (%)[a]	-0.085	16.53	0.057	-0.18
	Compliance Voltage (V)	0.5-1.2	0.2-1.1	0.4-1.1	0.6-1
	Output Resistance (MΩ)	9.89	10.7	21.7	168
Cascode CM	Mirroring accuracy*	Better	Better	Better	Poor
	PER (%)[a]	-0.083	14.76	0.012	-0.2
	Compliance Voltage (V)	0.4-1.2	0.2-0.7	0.4-1.2	0.2-0.7
	Output Resistance (MΩ)	9.89	10.7	21.7	293

* Overall Performance; [a] At input current=10 µA

All the comparative simulated data has been tabulated in Table I, where all parameters are categorized based on topology and technology node. Table I shows that as topology changes with an increased number of transistors, accuracy is also increased with the penalty of increased compliance voltage. It is examined that at lower technology node in CMOS technology, the performance of the current mirror is found poor due to SCEs and it is also figured out that using FinFET for CM is not beneficial for these four topologies. A various number of current mirrors exhibit different techniques for greater performance that have been developed using 180 nm technology node.

For better understanding to continue with 180 nm Fig. 3.7 concludes basic parameters comparison for all four basic CM structures. Where it can be seen that Cascode CM gives superior performance among all structures.

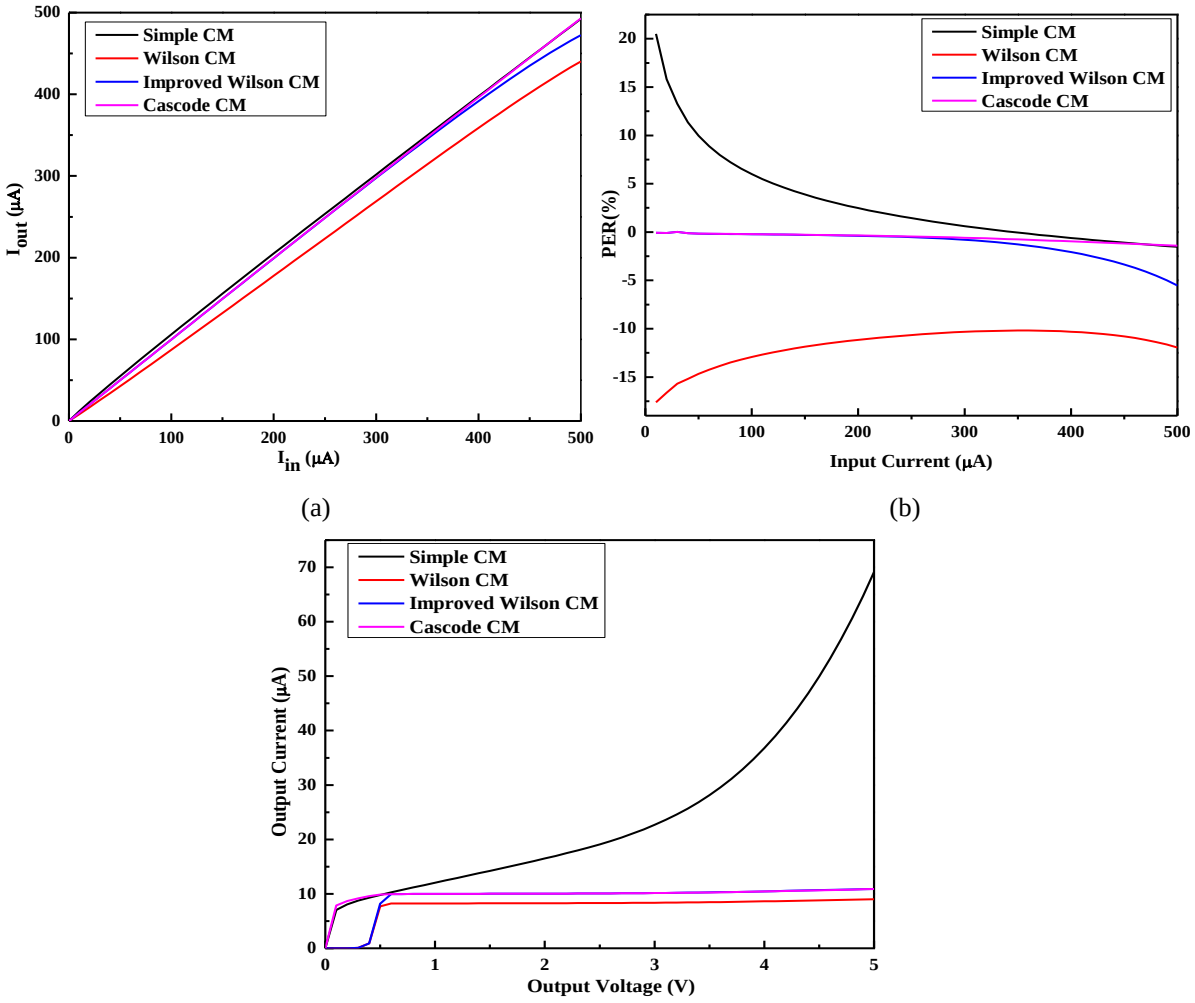


Fig. 3.7 Comparative plots of basic CMs structures at 180 nm (a) Current transfer characteristics (b) PER (c) Output Compliance Voltage

IMPORTANT OUTCOMES:

- Designing and analysis of different types of CM are accomplished on different technology nodes.
- The input current has taken for DC analysis as 10 µA and swept for 0-500 µA range. Similarly, for DC analysis output voltage is taken to have values of 1 V and the output voltage is a sweep for 0-5 V for compliance voltage calculation.
- A conclusion can be made based on the observation that Cascode CM has shown the best performance than other three CM and also, as technology node gets lower performance is degrading.

CHAPTER 4

PARAMETRIC COMPARISON AND SMALL-SIGNAL ANALYSIS FOR ADVANCED CURRENT MIRROR STRUCTURE

4.1 Advanced Current Mirror Structures

This section will describe the advance modified current mirrors with enhancing performance in terms of accuracy, resistance, and compliance voltage, and these two current mirrors are also compared in this section. Parameters such as characteristics, PER, and compliance voltage is simulated and compared here. Here it is shown that how this structure is different from previously mentioned basic structures.

4.1.1 Extremely Low Voltage High Compliance CM (ELVHC CM)

The transistor level of implementation of the ELVHC current mirror is shown in Fig. 4.2. This CM is the upgraded version of the CM present in [16] Fig. 4.1. In this structure, high swing cascode CM is used.

The ELVHC CM structure comprises two feedbacks; one is positive feedback consisting of transistors M1-M4 and the other one is negative feedback made up of transistors M2, M4, and M5, and an amplifier comprising of M_{ac1} and M_{a1}. This negative feedback stabilizes the output current adjacent to the variations of output voltage which results in an excellent performance of the current mirror. But as output voltage tends to ground, the negative feedback fails. So an alternative approach comes in structure is to use positive feedback which is more suitable for low voltage applications. The current compensated transistors Mc1-Mc2 allow positive feedback at a higher range of input current and for the lower range of input current, they have an insignificant effect. The increased difference between transistors' M1 and M2 VDS voltages applied to the gate of Mc1-Mc2 led to enlarge the positive feedback [10].

4.1.1.1 Small Signal Analysis

The small-signal analysis model of the ELVHC current mirror has been shown in Fig. 4.3(a) and Fig. 4.3(b). This structure takes only two capacitors for practicable calculation as Cd3 and Cd4 which is at high impedance node. Doing some calculations on a small-signal model following equations can be retrieved [16].

$$g_{m4}(V_{d4} - V_{d2}) + g_{mc2}V_{d3} + \left[\frac{1}{\frac{1}{C_{d4}} \| r_{dsc2} \| r_{ob2}}\right] V_{d4} = 0 \qquad (4.1)$$

where $C_{d4} = C_{gsc1} + C_{gsa1} + C_{dsc2} + (1 + A)C_{gdac1}$

where g_m, $r_{ds,}$ and r_o stands for transconductance, output drain to source resistance, and output resistance of transistors, respectively, while C_{gs}, C_{ds}, $C_{gd,}$ and C_d represents the gate to source capacitance, drain to source capacitance, a gate to drain capacitance and drain capacitance, respectively. And V_d is the drain voltage.

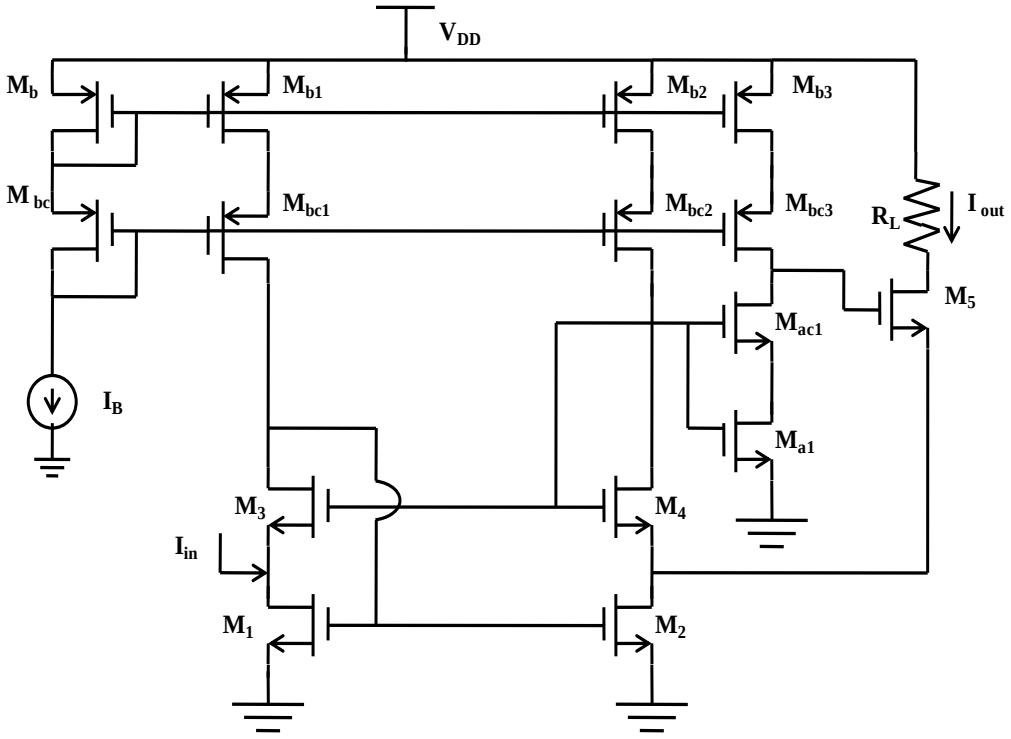


Fig. 4.1 Transistor Implementation of CM [16]

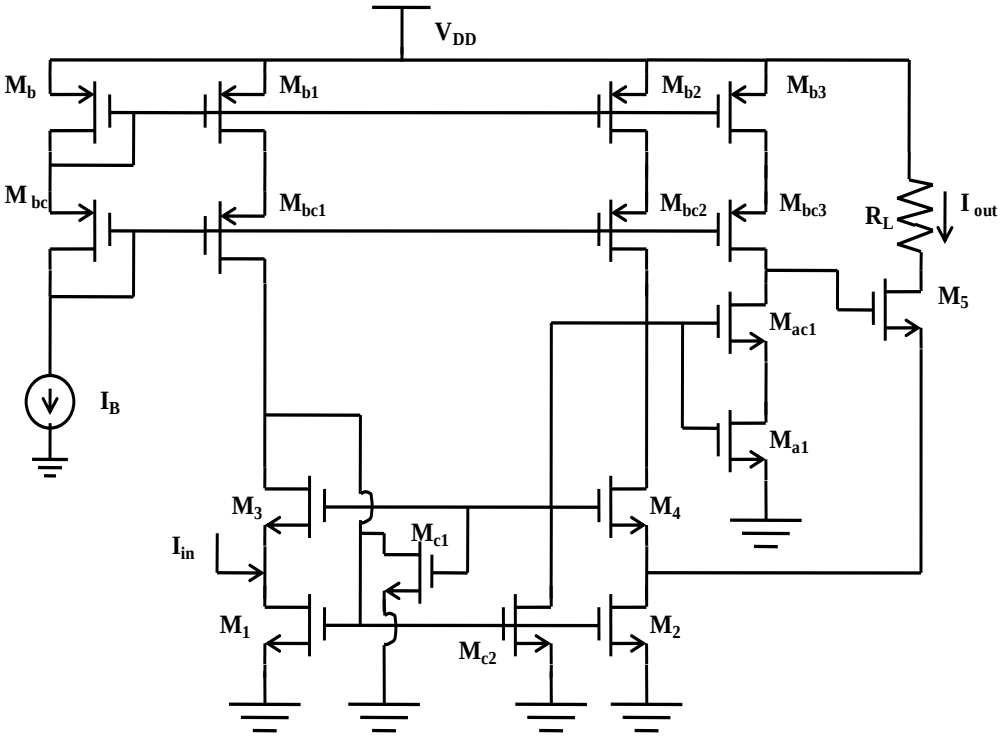


Fig. 4.2 Transistor Implementation of ELVHCCM [10]

Applying KCL at output node:

$$I_{out} = g_{m4}(V_{d2} - V_{d4}) + \frac{1}{r_{ds2}}V_{d2} + g_{m2}V_{d3} \tag{4.2}$$

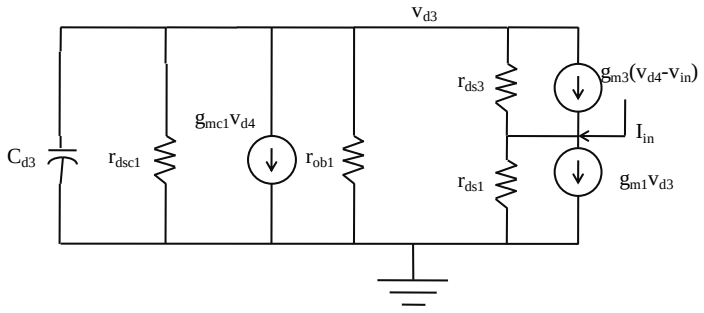
$$I_{out} = \frac{1}{r_{ds5}}V_{out} - g_{m5}V_{d2} - Ag_{m5}V_{d4} \tag{4.3}$$

$$g_{m3}(V_{d4} - V_{in}) + \frac{V_{d3}}{\frac{1}{C_{d3}s}\|r_{dsc1}\|r_{ob1}\|r_{ds3}} + g_{mc1}V_{d4} = 0 \tag{4.4}$$

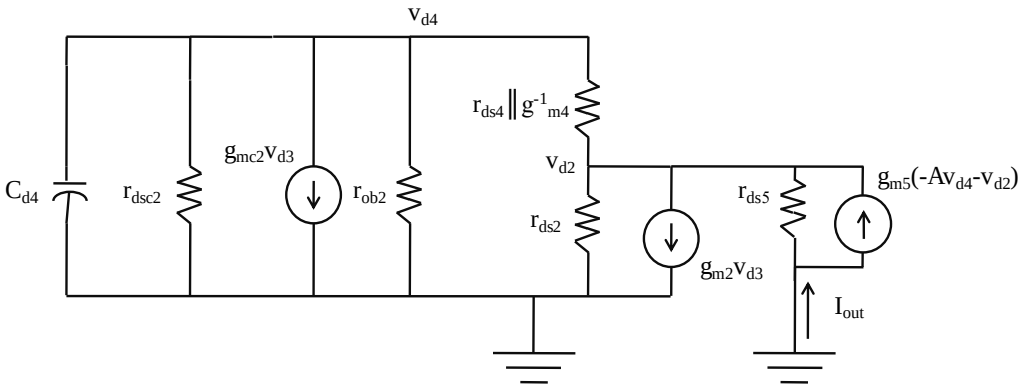
where$C_{d3} = C_{gs1} + C_{gs2} + C_{dsc1} + C_{gsc2} + C_{gdbc1}$.

$$I_{in} = \frac{1}{r_{ds1}}V_{in} + g_{m1}V_{d3} + g_{mc1}V_{d4} \tag{4.5}$$

where $A = \frac{g_{ma1}g_{mac1}r_{dsa1}r_{dsac1}r_{ob3}}{r_{ob3}+g_{mac1}r_{dsac1}r_{dsa1}}$.



(a)

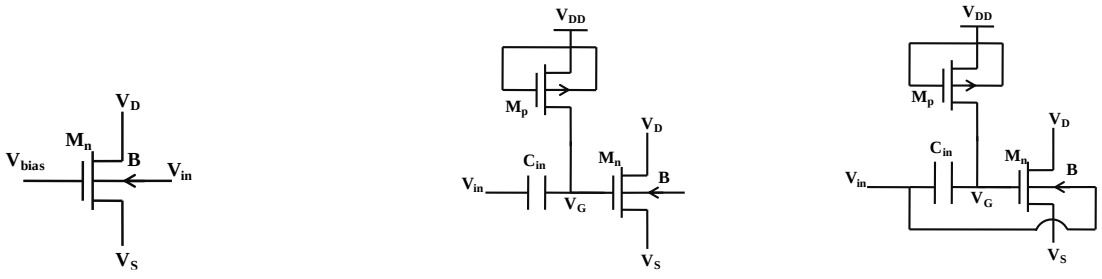


(b)

Fig. 4.3 Small signal analysis model for ELVH CM (a) and (b)

4.1.2 Bulk Driven Quasi Floating Gate FVF CM (BDQFG FVF CM)

One of the most used current mirrors is Cascode CM and its variants. Its characteristics are high output impedance, low input impedance and higher accuracy can be observed in [17]. One of the variants of this CM that removes the drawbacks of CCM (Cascode current mirror) is depicted as Bulk Driven technique although it also experiences lower bandwidth [18-19]. Also, references [20-21] represent the Bulk Driven Quasi Floating Gate Current mirror which improvised the input impedance and bandwidth but still with lack in output impedance. Now using all the above-described techniques are used in BDQFG FVF CM which is analyzed in this paper. It has simple circuitry with ultra-low power consumption and using a low voltage [12].



(a) (b) (c)

Fig. 4.4 Transistor implementation: (a) BD MOST, (b) QFG MOST and (c) BDQFGMOS

Bulk-driven MOSFET (BD MOST) is shown in Fig. 4.4(a), in which the input signal is applied to a bulk node. V_{bias} is arranged in the form to create the inversion layer to start the operation of conduction. This technique is useful for linearity and gain in analog circuits for low voltage applications. Now, Quasi floating gate MOSFET (QFG MOSFET) is depicted in Fig. 4.4(b). The transistor Mn is supplied with input voltage via capacitance

and the gate of the Mn is connected weakly to a high-value resistance which comprises PMOS (M_p) and lying in the cut-off region.

By merging BD MOST and QFG MOST technique, Fig. 4.4(c) is obtained as the result. This technique represents the advantages of the BD technique such as full input voltage swing and low voltage application usage while the QFG technique shows the higher values of transconductance.

The above techniques are implanted in the current mirror which is shown in Fig. 4.5. The flipped voltage follower technique is used here to get the benefits of low input impedance by using the negative feedback which comprises M3 and M5 transistors. In this type of current mirror, the variations in the input current are immersed by the M1 transistor which forms the change in the Vgs voltage which is again mirrored in the output current.

4.1.2.1 Operation of BDQFG FVF CM

Fig. 4.5 is showing the transistor implementation of bulk driven quasi floating gate current mirror. Where the input and output resistance of the Flipped Voltage Follower part is given as (here N and P denotes NMOS and PMOS respectively):

$$R_{inN,P} \approx \frac{1}{g_{m1N,P} g_{m3N,P} r_{o1N,P}} \tag{4.6}$$

$$R_{outN,P} \approx r_{o2N,P} r_{o4N,P} g_{m2N,P} \tag{4.7}$$

The FVF CM shows low voltage, higher values of output resistance, and lower input resistance. In Fig. 4.5 transistors M1 and M2 comprise BDQFG CM. An input signal is fed in the drain of M1. M1 and M2 are arranged in the manner that both gates are connected to the capacitance C1 and C2 and M3 and M4 give the high resistance value which is obtained by operating in the cut-off region. In various studies, it has been shown that BDQFG MOS represents a greater value of transconductance which can be given by [22]:

$$g_{m1eff} = k(g_{m1} + g_{mb1}) \tag{4.8}$$

$$g_{m2eff} = k(g_{m2} + g_{mb2}) \tag{4.9}$$

4.1.2.2 Small Signal Analysis

In this subsection small-signal analysis has been done for Fig. 4.5 on the input side and output side. The small-signal analysis model is represented in Fig. 4.6 and Fig. 4.7. Here it is assumed that transistors M6 and M7 are in the cutoff region and all remaining transistors are in the saturation region. From Fig. 4.6, at node 2 (here V_1, V_2, I_1, I_2, etc. are node voltage and branch current):

$$V_2 = -r_{05} I_1 \tag{4.10}$$

$$V_2 - V_1 = r_{03}(I_1 + g_{m3} V_1) \tag{4.11}$$

Similarly at node 1:

$$V_1 = r_{01}(I_{in} + I_1 - (kg_{m1} + kg_{mb1})V_2) \tag{4.12}$$

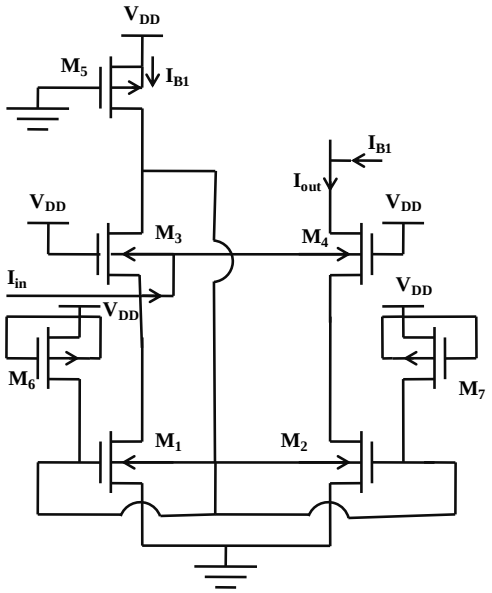


Fig. 4.5 Bulk Driven Quasi Gate Floating Flipped Voltage Follower CM

Using Equation (4.10) and (4.11):

$$I_1 = \frac{(1+rg_{m3})V_1}{r_{05}+r_{03}} \tag{4.13}$$

Using Equation (4.10) and (4.12):

$$V_1 = r_{01}\big(I_{in} + I_1 - (kg_{m1} + kg_{mb1})(r_{05} I_1)\big) \tag{4.14}$$

From Equation (4.13) and (4.14) input resistance is represented as:

$$r_{in} = \frac{V_1}{I_{in}} = \frac{r_{01}(r_{03}+r_{05})}{(r_{03}+r_{05})+\big(r_{01}(1+r_{03}g_{m3})\big(1+r_{05}(kg_{m1}+kg_{mb1})\big)\big)} \tag{4.15}$$

Similarly, output resistance can be derived from Fig. 4.7, at node 3:

$$V_3 = -r_{02}(g_{m4}V_3 + g_{mb4}V_3 + I_1) \tag{4.16}$$

$$V_{out} - v_3 = -r_{04}I_1 \tag{4.17}$$

$$-I_{out} = (g_{m4} + g_{mb4})V_3 + I_1 \tag{4.18}$$

By using the given above three Equations i.e. (4.16), (4.17), and (4.18) r_{out} can be given as:

$$r_{out} = \frac{V_{out}}{I_{out}} = r_{04} + r_{02} + (g_{m4} + g_{mb4})r_{02} \tag{4.19}$$

BDQFG FVF CM shows a higher resistance value as compared to Equation (4.7).

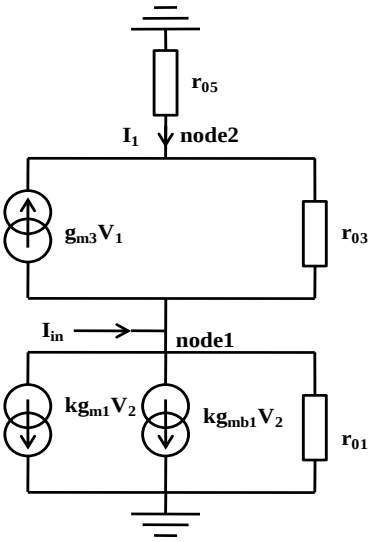


Fig. 4.6 Small-signal model of BDQFG FVF CM for input resistance calculation

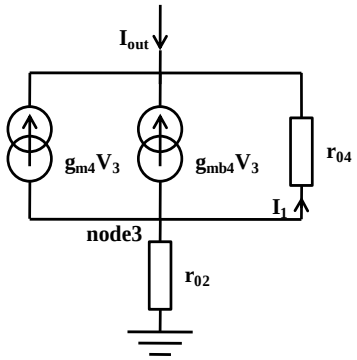


Fig. 4.7 Small-signal model of BDQFG FVF CM for output resistance calculation

4.2 Performance Analysis of ELVHC CM and BDQFG FVF CM

Here DC analysis is done to examine the performance of both CM and for efficient functionality; Monte Carlo analysis is accomplished on design parameters concerning the

threshold voltage and temperature variations. Here the objective is to compare both structures regarding their parameters to conclude which one is robust and reliable.

Specification and aspect ratio is listed in Table 4.1 and Table 4.2. The ELVHC CM is operated at a 1 V power supply whereas BDQFG FVF CM is at 0.5 V. Both CM are analyzed over 0-200 μA for input current versus output current characteristics. While for the output compliance voltage, the range for V_{out} is taken 0-5 V. This paper presents the performance based on the parameters such as; output current versus input current, percentage error ratio, and output compliance voltage. The schematics of both CM are shown in Fig. 4.8 and Fig. 4.9.

Table 4.1- Aspect ratio for ELVHC CM

Transistor	**W/L (μm)**
M_1-M_2	45 /0.54
M_3	29.7 /0.18
M_4	30/0.18
M_5	50/0.18
M_{c1}	0.36/4.86
M_{c2}	3/4.86
M_{ac1}	10/0.18
M_{a1}	36/0.18
M_b, M_{b1}, M_{b2}, M_{bc}, M_{bc1}, M_{bc2}	1/0.18
M_{b3}	2/0.18
M_{bc3}	2/0.18

Table 4.2- Aspect ratio for BDQFG FVF CM

Transistor	**W/L (μm)**
M_1	33 /0.18
M_2	40 /0.18
M_3	22 /0.18
M_4	37/0.18
M_5	0.12/0.18
M_6-M_7	0.5/0.18

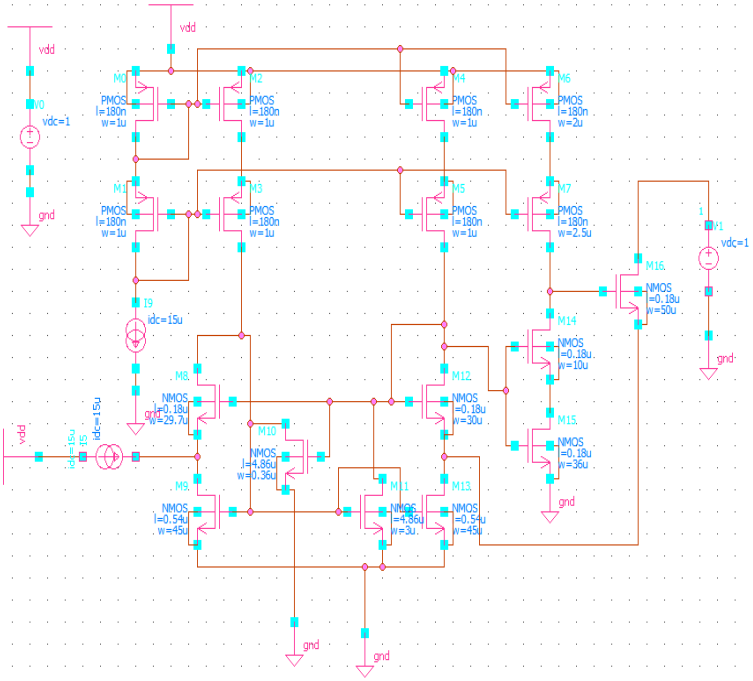


Fig. 4.8 Schematic of ELVHC CM

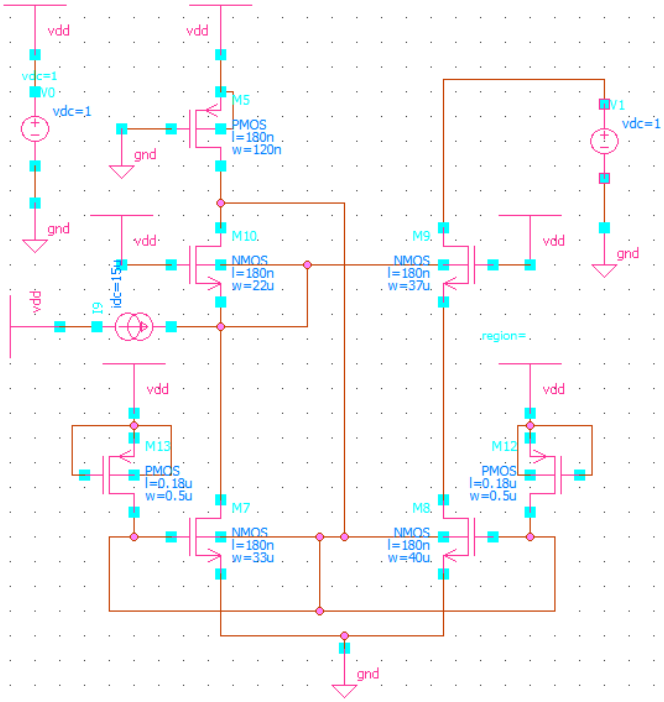


Fig. 4.9 Schematic of BDQFG FVF CM

To examine the current mirroring of both CM, the current transfer characteristics are shown in Fig. 4.10(a). In these characteristics, ELVHC and BDQFG FVF CM are compared with the input current. It can be seen in these characteristics that ELVHC CM shows a higher matching with the input current whereas BDQFG FVF CM displayed

comparatively less matching. To demonstrate the error percentage of mirroring, the Percentage Error Ratio (PER) is plotted in Fig. 4.10(b).

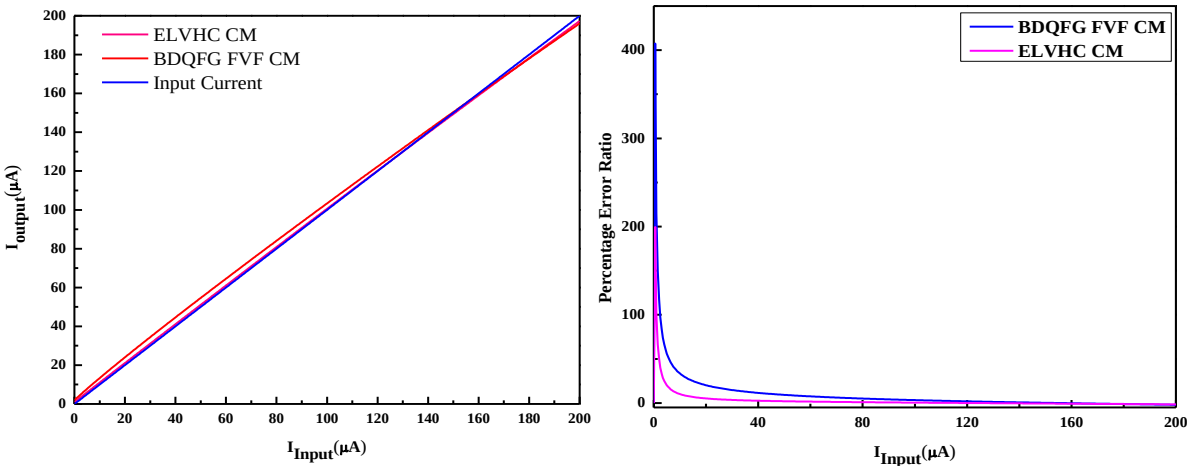
The PER is given by the following formula:

$$PER = \frac{I_{out} - I_{in}}{I_{in}} \times 100 \tag{4.20}$$

Fig. 4.10(b) represents that BDQFG FVF shows the error higher than the ELVHC CM. It is found that at input current 15μA, PER is 4.2% in ELVHC CM where for BDQF FVF CM the PER is 18.7%. For both CM, as the input current range goes high the PER is also proceeding lower means accuracy is enhanced.

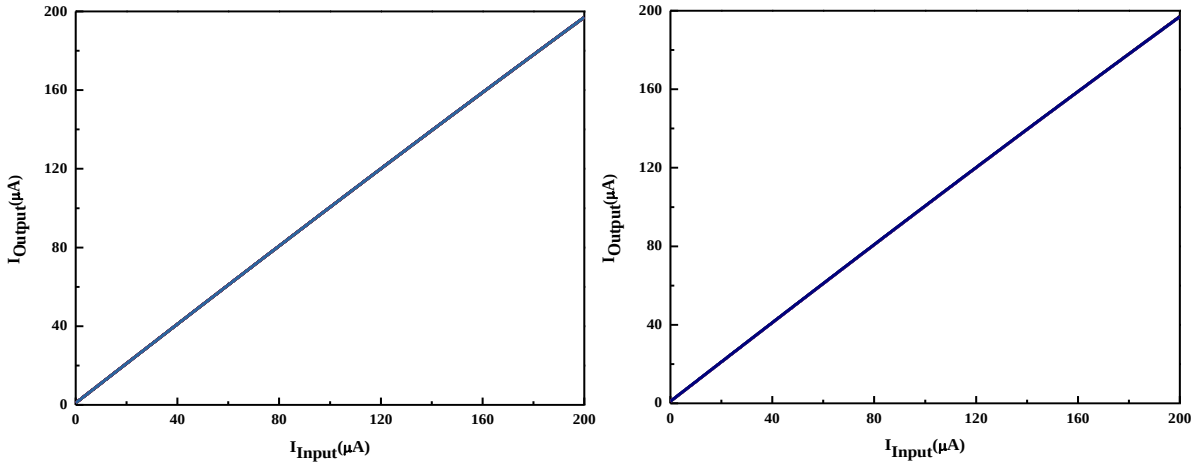
The impact of variations in threshold voltage in ELVHC CM is shown by Monte Carlo analysis with 10 numbers of runs as depicted in Fig. 4.11(a). It is observed that as the threshold voltage goes high accuracy will be less while going towards lower threshold voltage accuracy getting improved. Similarly, Monte Carlo analysis for ELVHC CM with temperature variation for 0°C, 25°C, 50°C, 75°C, 100°C, and 125°C is shown in Fig. 4.11(b), where it is realized as the temperature increased accuracy also enhanced.

Talking about BDQFG FVF CM's Monte Carlo analysis for current transfer characteristics with threshold voltage variation is shown in Fig. 4.12(a) while the variation in temperature from 0ºC to 125ºC is described in Fig. 4.12(b), whereas the temperature goes higher the output current gets amplified.



(a) (b)

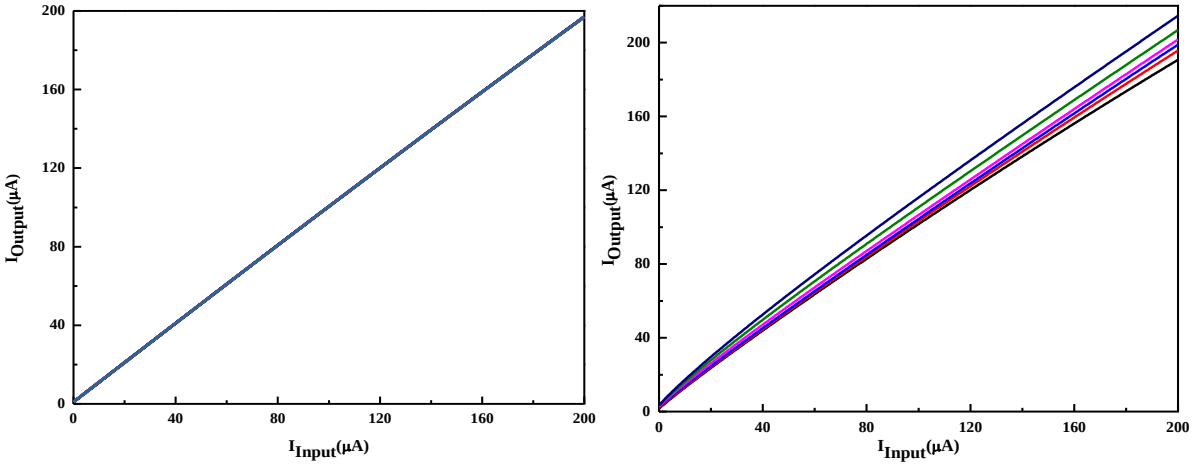
Fig. 4.10 Comparative results of advanced modified current mirrors (a) Current transfer characteristics (b) PER



(a) (b)

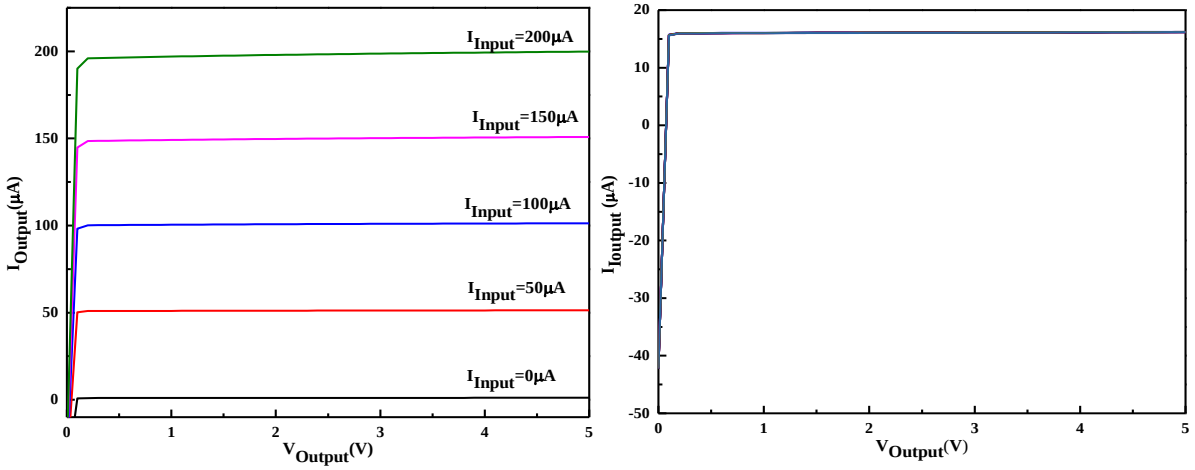
Fig. 4.11 I_{out} Vs I_{in} Monte Carlo analysis applying (a) in V_{th} (b) in temperature for ELVHC CM

The computation of output compliance voltage for ELVHC CM output characteristics is plotted in Fig. 4.13(a) where the output voltage range used is 0-5 V. This characteristic is plotted with input current which stepped from 0 to 200 μA in steps of 50 μA. It is recognized that at an input current of 15 μA the output compliance voltage is found 0.091 V. Monte Carlo analysis with threshold voltage and temperature variation is done and demonstrated in Fig. 4.13(b) and Fig. 4.13(c). Observing Fig. 4.13(b), it is discovered that the output compliance voltage increases with an increase in the threshold voltage, and the same pattern is spotted in Fig.4.13(c) with temperature.

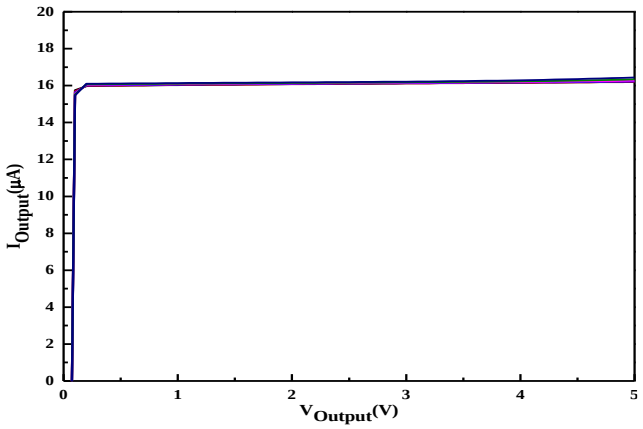


(a) (b)

Fig. 4.12 I_{out} Vs I_{in} Monte Carlo analysis applying (a) in V_{th} (b) in temperature for BDQQFG FVF CM

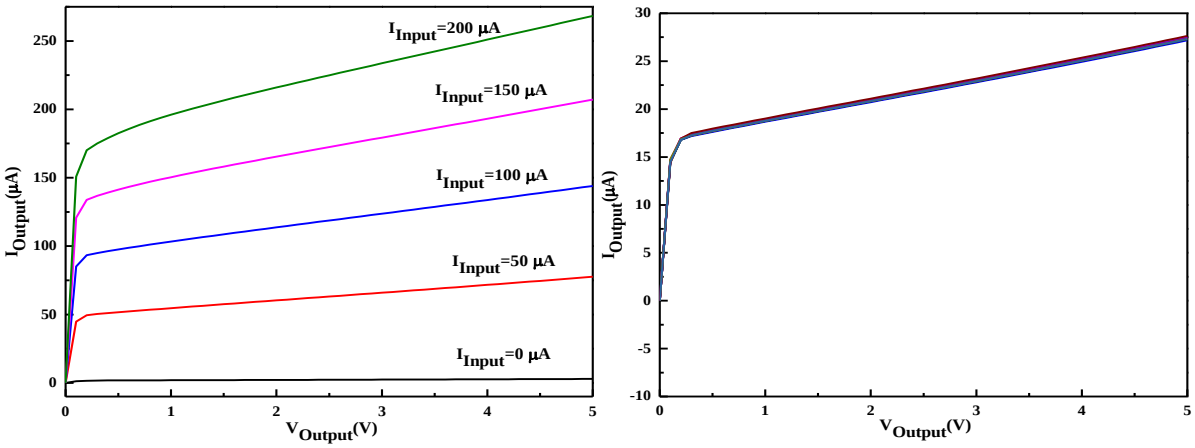


(a) (b)

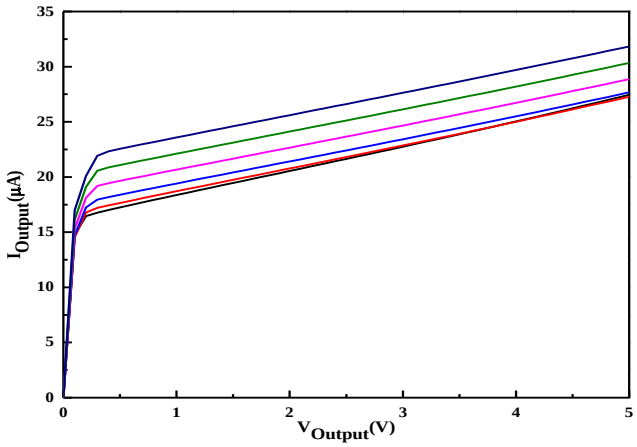


(c)

Fig. 4.13 Output current Vs output voltage for ELVHC CM (a) with variations in input current, (b) Monte Carlo analysis in V_{th}, and (c) temperature variations



(a) (b)



(c)

Fig. 4.14 Output current Vs output voltage for BDQFG FVF CM (a) with variations in input current, (b) Monte Carlo analysis in V_{th}, and (c) temperature variations

Fig 4.14 depicts the output characteristics for the BDQFG FVF CM with similar specifications as used in ELVHC CM. The output compliance voltage is gained at 0.12 V for the input current at 15 μA and also it is viewed that as the input current is reached at its higher value, the output compliance voltage also goes increases, as shown in Fig. 4.14(a). Now the process variation i.e. threshold voltage applied on it and results are shown in Fig. 4.14(b), where it is found that as threshold voltage decrease the output compliance voltage increases. Further, as the temperature increases the compliance voltage decreases which is shown in Fig. 4.14(c).

Table 4.3- Comparative Results for ELVHC CM and BDQFG FVF CM

Parameters	**Current mirror**	
	ELVHC	**BDQFG FVF**
I_{in} (μA)	15	15
CDR (μA)[a]	200	200
I_b (μA)	15	NA
PER (%)[b]	4.2 (0.03 @ 200 μA)	18.7 (0.02 @ 200 μA)
$V_{out,min}$(V)	0.091	0.12
V_{supply} (V)	1	1
Technology	180 nm	180 nm

[a] Current dynamic range; [b] Percentage error ratio @ 15 μA

Table 4.3 concludes the comparative results for both CM. It can be seen in the table that ELVHC shows great performance as compared to BDQFG FVF CM. The current dynamic range for this paper is taken 0-200 μA as shown in Tab. 4.3.

IMPORTANT OUTCOMES:

- ELVHC CM and BDQFG FVF CM are analyzed at a 180 nm technology node with a power supply of 1 V.
- Using Monte Carlo Analysis of ELVHC CM it is observed that as the threshold voltage goes high accuracy will be less while going towards lower threshold voltage accuracy getting improved
- For temperature parametric analysis for ELVHC CM, it is realized as the temperature increased accuracy is also enhanced.
- In a conclusive statement, ELVHC CM shows better performance than BDQFG FVF CM.

CHAPTER 5

PROPOSED CURRENT COMPARATOR

A simple voltage comparator can be realized by using an op-amp, but the power consumption and dc offset errors are found to be high in voltage comparators. Whereas the current comparators got low offset errors and low power consumption when compared to voltage comparators. Also, current comparators got a small area as the size of their transistors is small. The main function of a current comparator is to detect which of the current is greater (Iin or Iref). It represents the current difference in form of Voltage. Parameters that majorly define the performance of the comparator are propagation delay, power dissipation, and power delay product (PDP). The current comparator circuit includes the current difference stage, gain stage, and output stage. To enhance these parameters current difference stage plays a major role.

A current comparator can be found in various applications such as current-mode signal processing, analog to digital converter (ADC), oscillator circuits, WTA (winner take all) in VLSI neural network implementations, temperature sensors, photo-sensors, current Schmitt triggers, function generators, current to frequency converters, sequence detection, fuzzy system, and non-linear filters, implantable biomedical devices, etc. [23-46].

Hence this chapter will introduce the fundamental concepts of the current comparator. The following sections will describe the functionality of the current comparator and the application of the current comparator.

5.1 Basic Concept of Current Comparator

The basic current comparator takes the current difference as an input to determine which of the current is greater Iin or Iref and the output is served in the form of voltage such as logic '0' or logic '1' i.e. if Iin is greater than Iref then it produces a high voltage (logic '1') else low voltage (logic '0'). Iref is constant current while the variable signal is Iin i.e. pulse in this paper. The mathematical representation can be shown:

$$\boldsymbol{V_{out}(t)} = \begin{cases} \mathbf{1}, & \boldsymbol{I_{in}(t) > I_{ref}(t)} \\ \mathbf{0}, & \boldsymbol{I_{in}(t) < I_{ref}(t)} \end{cases} \tag{4.1}$$

The behavior of the current comparator is decided by propagation delay, power consumption, and power delay product which impact largely on low power application. As said earlier generally the current comparator is consists of three stages, the current difference stage, gain stage, and output stage (Fig. 5.1).

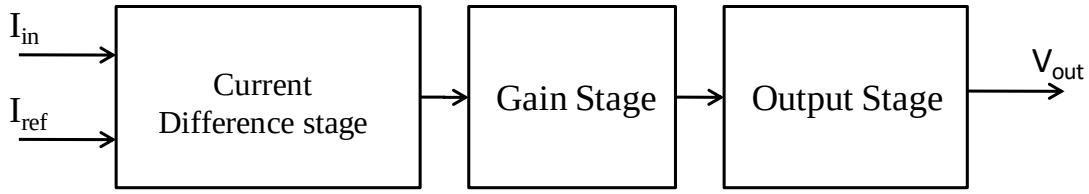


Fig. 5.1 Simplified block diagram of the current comparator

The current difference stage is a combination of two identical current mirrors (CM) and arranged in this manner that it will produce the difference of two currents. Choice of the suitable current mirror impacts the overall performance of the current comparator. The output resistance of the current mirror affects the delay of the circuits and efficiency. Next, the gain stage amplifies the voltage and its variations. Also the rise time, fall time, noise immunity has been improved in this stage and for rail to rail swing output stage is used to obtain the desired output level.

5.2 Proposed Current Comparator

The current comparator in Fig. 5.2 is consisting of the current differencing stage which is made of Bulk driven quasi floating gate flipped voltage follower current mirror (BDQFG FVF CM) that has been shown better performance in [12]. But as these two current mirrors, BDQFG FVF CM and ELVHC CM have been compared and the better current transfer accuracy found in ELVHC CM and it is already mentioned that current differencing plays a major role in the current comparator. Hence current comparator based on these two current mirrors is represented in Fig. 5.2 and Fig. 5.3.

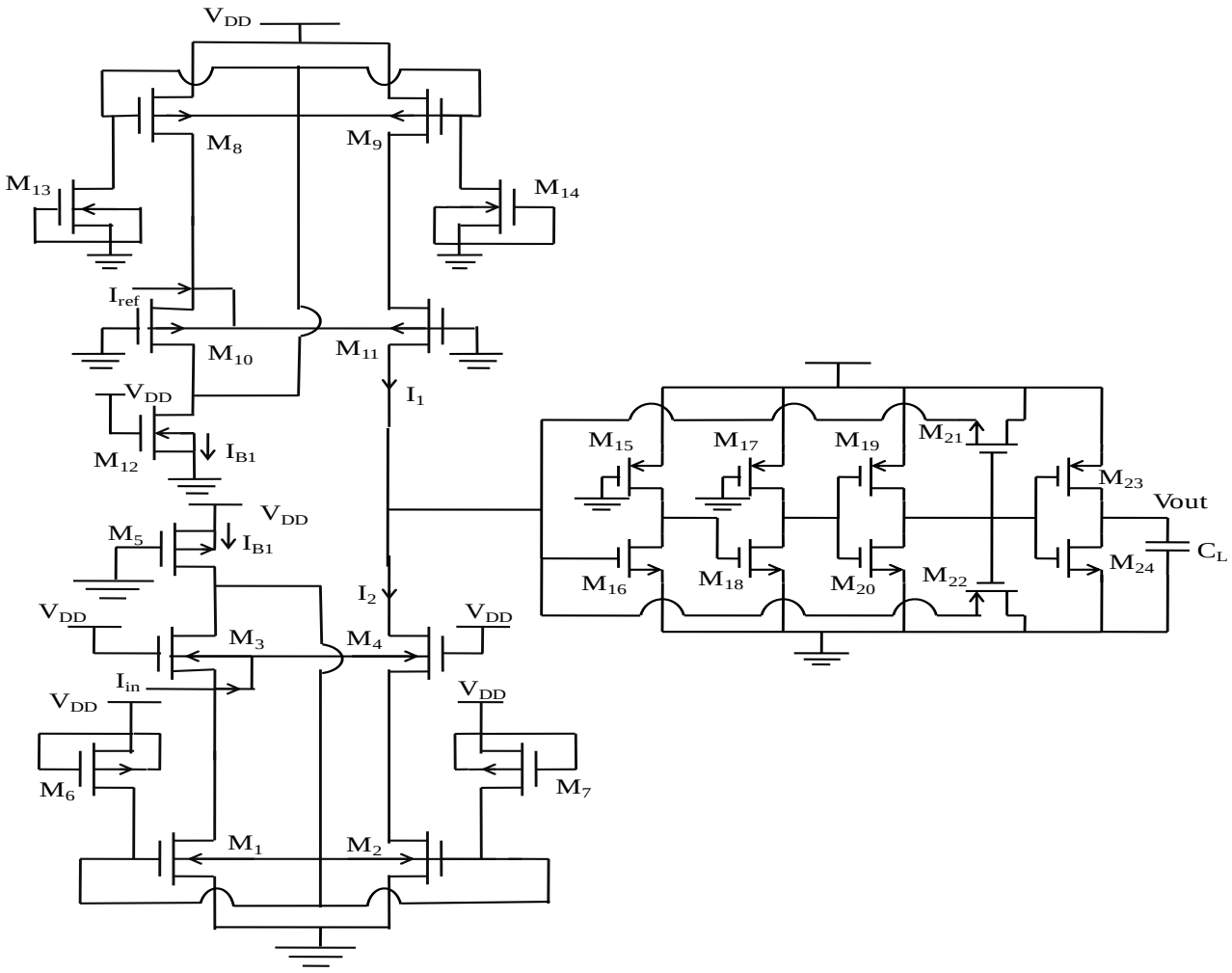


Fig. 5.2 Current Comparator based on BDQFG FVF CM

5.2.1 Proposed Structure Description

Based on an Extremely low voltage high compliance comparator current mirror (ELVHC CM) [10], a new design of current comparator is proposed (Fig. 5.3) in this paper to enhance the parameter delay, power consumption, and PDP. The circuit diagram of the proposed current comparator is depicted in Fig. 5.3. It comprises of two ELVHC current mirrors which are connected in parallel, a nonlinear feedback gain stage, and an output stage. The operability can be represented as each current mirror consist of a biasing current generating circuits, current compensated transistor (M_5, M_6, M_{22}, M_{23}), amplifier stage (M_7, M_8, M_{24}, M_{25}), mirroring transistors (M_1, M_2, M_{18}, M_{19}), the cascode transistors (M_3, M_4, M_{20}, M_{21}) and the output current buffer transistors ($M1_7$, M_{34}).

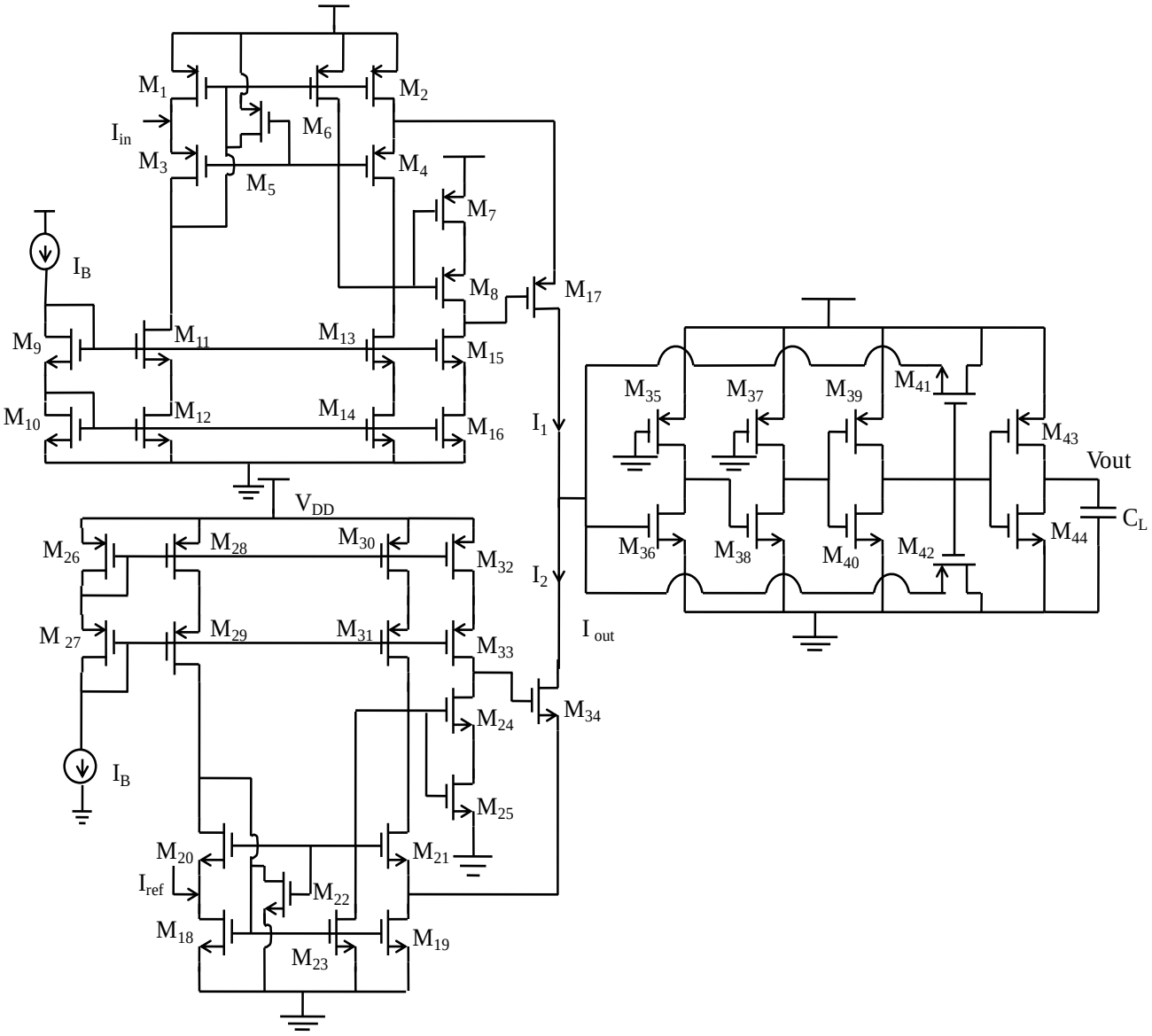


Fig. 5.3 Proposed Current Comparator based on ELVHC CM

There are two feedbacks: negative feedback built from M_2, M_4, M_7, M_8, and M_{17} whereas the positive feedback assembled M_1, M_2, M_3, and M_4. The negative feedback is used to maintain the output current against the variations of output voltage. But for low voltage, the negative feedback is failed to handle this function because those transistors make the feedback loop drop the saturation region which results in destructive feedback gain hence positive feedback comes into a picture and recovers the feedback gain. Furthermore, for boosting the positive feedback for high-value input current and broaden the range for low power applications, the current compensated transistors M_5 and $M_6$are used [16].

Now, this current mirror is used in the current differencing stage (M_1-M_{34}) for a proposed current comparator. This current difference is fed into the gain stage (M_{35}-M_{42}). The stage structure consisting of two cascaded resistive amplifiers (M_{35}-M_{36}, M_{37}-M_{38}), an inverter stage (M_{39}-M_{40}), and nonlinear feedback (M_{41}-M_{42}). The functioning of a gain stage can be described as it rebuilds the current difference into a corresponding voltage at the input of the output stage. The nonlinear feedback transistors are guided by this converted voltage. When the current difference is very low, the input and output voltage of the gain stage is not quite enough to turn on the M_{41}-M_{42} and this resulting the input node of the gain stage become capacitive which brings slow charging/discharging of the voltage at the input node. In contrast to lower input current difference, when the value goes positively high of current difference, increased voltage at input resulting in a decrement in the output of gain stage due to its inverting behavior and it causes $M_{42\ to}$ turn ON. Thus it is resulting in a stop of feedback loop. Similarly, when the negative current comes at the input, transistor M_{41} is turned ON. And this output voltage of the gain stage is going for rail to rail swing output through the output stage (M_{43}-M_{44}) [47].

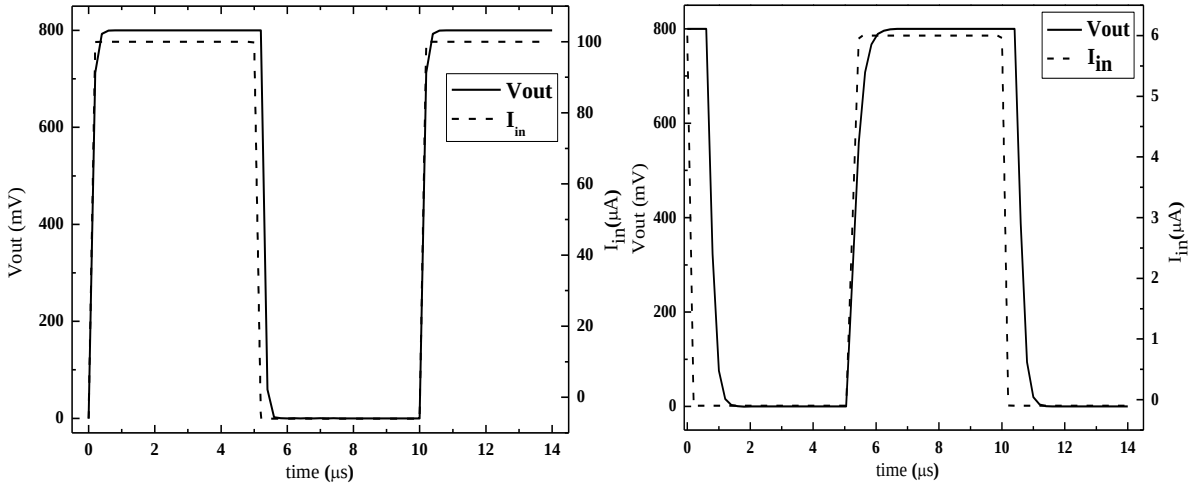
5.2.2 Parametric Extraction of Current Comparator

The major parameters of a general current comparator are propagation delay, resolution, power consumption, and power delay product (PDP). Propagation delay is a time taken by output in switching following the input whereas resolution is a minimum current difference required to operate the comparator. Power consumption is the power used by the circuit to operate the function. To calculate all these parameters, the comparator is simulated with Cadence Virtuoso simulator using 0.18 μm gpdk technology and 0.8 supply voltage. The aspect ratio of the proposed comparator is listed in Table 5.1.

The input current (I_{in}) range is ±5 μA and the reference current (I_{ref}) is 0.5 μA taken for the operation of a comparator. And biasing current I_B is used as 1 μA. Acceptable performance can be acquired at 5 nA difference current, hence the resolution of this current comparator is 5 nA. The output of the proposed comparator is shown in Fig. 5.4(a) while the comparator based on BDQFG FVF CM is depicted in Fig. 5.4(b).

Table 5.1- Aspect ratio of transistor for Proposed Comparator

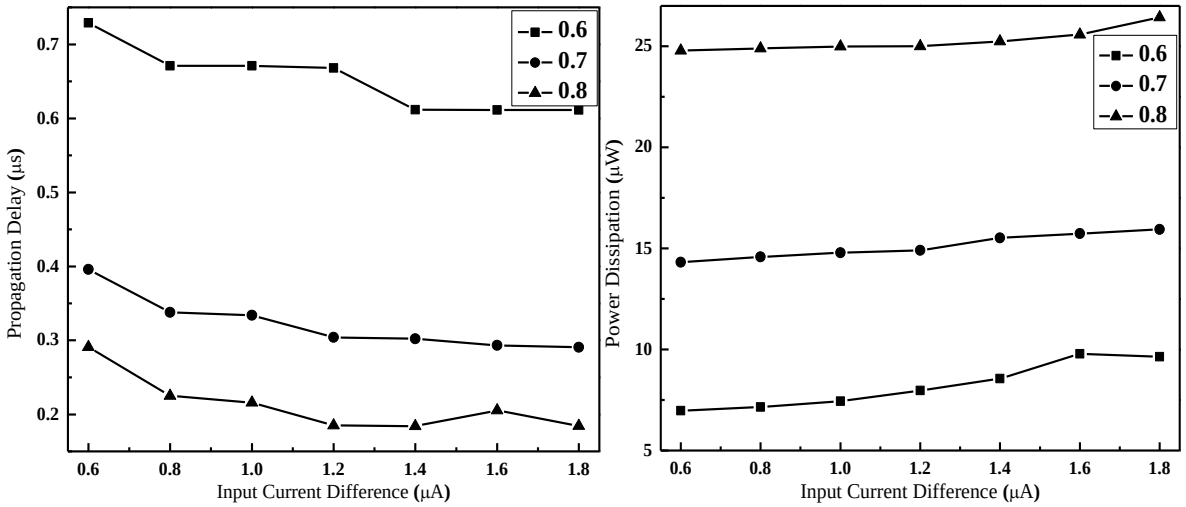
Transistor	Width (µm)	Length (µm)	Transistor	Width (µm)	Length (µm)
M_1, M_2, M_{18}, M_{19}	45	0.54	M_{35}	0.4	0.36
M_3, M_4, M_{20}, M_{21}	29.7	0.18	M_{36}	1.675	0.36
M_5, M_6, M_{22}, M_{23}	0.4	4.86	M_{37}	0.4	0.18
M_7, M_{25}	36	0.18	M_{38}	19	0.18
M_8, M_{24}	4.5	0.18	M_{39}	0.72	0.36
M_9-M_{16}, M_{26}-M_{33}	2	0.18	M_{40}	0.42	0.36
M_{17}, M_{34}	36	0.18	M_{41}, M_{42}	0.54	0.18
M_{43}	1	0.36	M_{44}	0.42	0.36



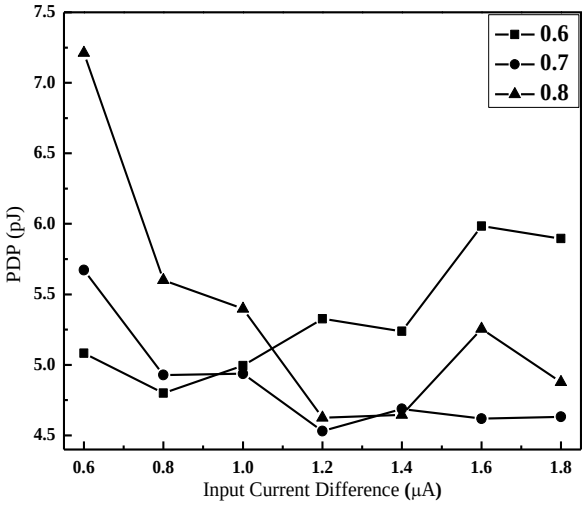
(a) (b)

Fig. 5.4 Output response of the (a) Proposed Current Comparator, (b)Current Comparator based on BDQFG FVF CM

The impact of variation in current difference on delay, power dissipation, and PDP can be seen in Fig. 5.5 and Fig. 5.6. They represent the parameters of BDQFG FVF CM based comparator and proposed comparator respectively, over different supply voltages i.e. 0.6 V, 0.7 V, and 0.8 V. In Fig. 5.4 the output response of the comparator is taken at 0.8 V supply voltage and I_{ref} is 20 nA and it is observed in the waveform that proposed comparator gives smaller delay than comparator based on BDQFG FVF CM. It is combinedly concluded that as the input current difference is increased the delay will be decreased. Here the effect of supply voltage can also be seen where greater supply voltage represents smaller delay.



(a) (b)



(c)

Fig. 5.5 Simulated waveform of (a) Propagation Delay, (b) Power dissipation, and (b) Power delay product versus Input current difference for Current Comparator based on BDQFG FVF CM

Furthermore in addition to power consumption proposed comparator shows lesser consumption than BDQFG FVF CM based comparator which is depicted in Fig. 5.5(b) and Fig. 5.6(b). Fig. 5.5(c) and Fig. 5.6(c) portrayed the characteristics of PDP of the BDQFG FVF CM based comparator and proposed comparator respectively wherein it is described the result of the product of delay and power consumption. The trend of delay and power of the proposed comparator and comparator based on BDQFG FVF CM can be summarized in Fig. 5.5 and Fig. 5.6. It is noticed as power supply voltage increased the delay of the comparator decreased and a similar pattern can be spotted when increasing the input current difference. Furthermore, in Fig. 5.6(b) the power dissipation is increasing with input current difference and also with supply voltage. Additionally, the PDP is a

product of delay and power, shown in Fig. 5.6(c) and the curve shows the decreasing PDP as current difference rise and power supply voltage increases.

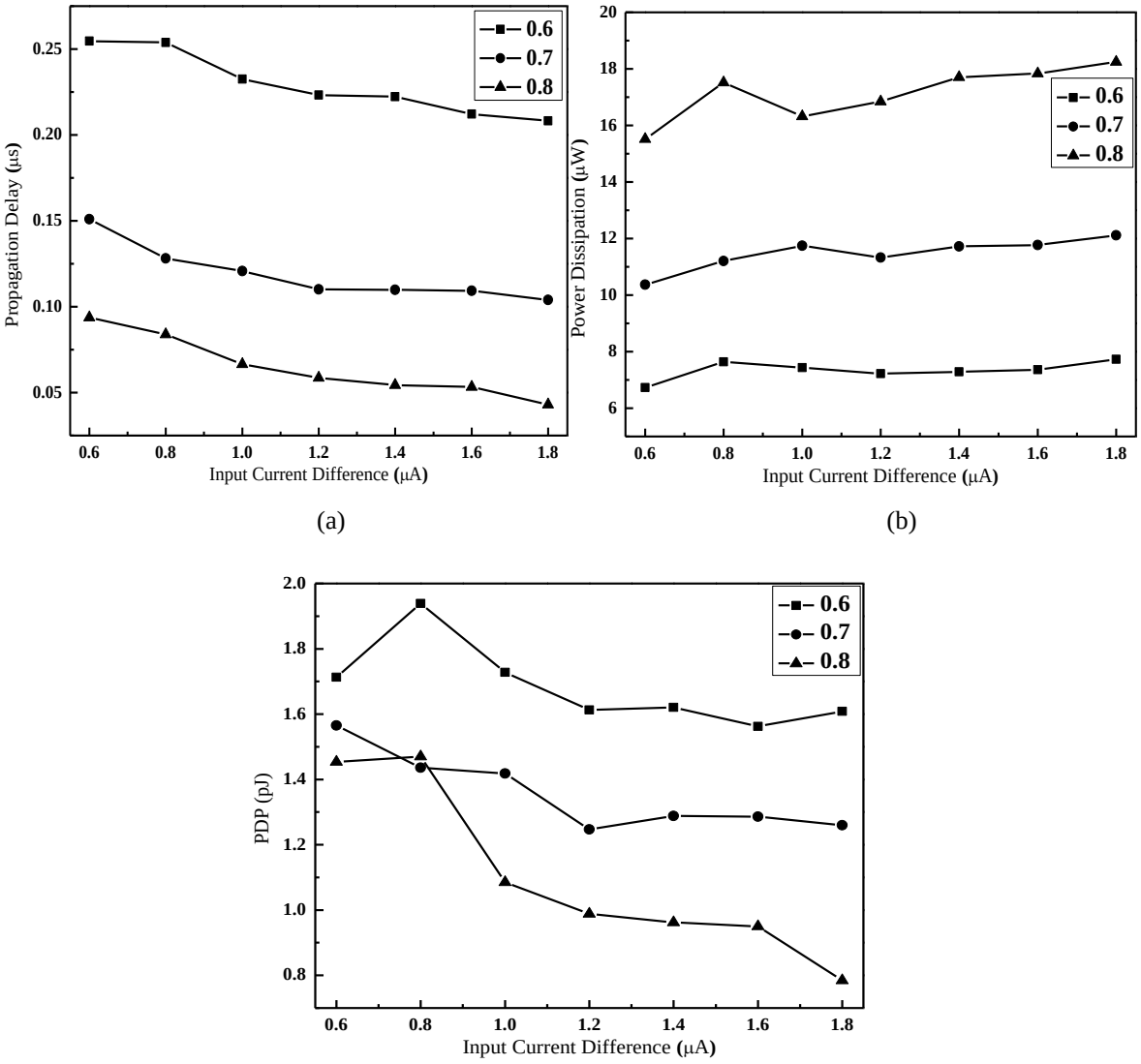


Fig. 5.6 Simulated waveform of (a) Propagation Delay, (b) Power dissipation, and (b) Power delay product versus Input current difference for Proposed Current Comparator

5.3 Results and Discussion of Proposed Comparators

In this section comparative results of the comparator based on ELVHC CM and BDQFG FVF CM of parameter delay, power dissipation, and PDP. Here all these parameters are simulated and compared at 0.8 V power supply voltage. It can be noticed in Fig. 5.7(a) that there is much difference between both proposed and BDQFG FVF CM based comparator. At input current difference of 1.2 μA difference between both comparators is 0.13 μA and at 1.8 μA is 0.14 μA on 0.8 supply voltage. Similarly in Fig. 5.7(b), power

dissipation can be seen more in BDQFG FVF CM based comparator than proposed. At 1.2 μA current difference is 32.6 percent decrement and at 1.8 μA current difference 29.82 percent decrement in power dissipation is observed in the proposed comparator. Moreover in Fig. 5.7(c) at 1.2 μA input current difference, 78.63 percent difference in PDP is observed. Whereas, at 1.8μA 83.92 percent difference has been seen.

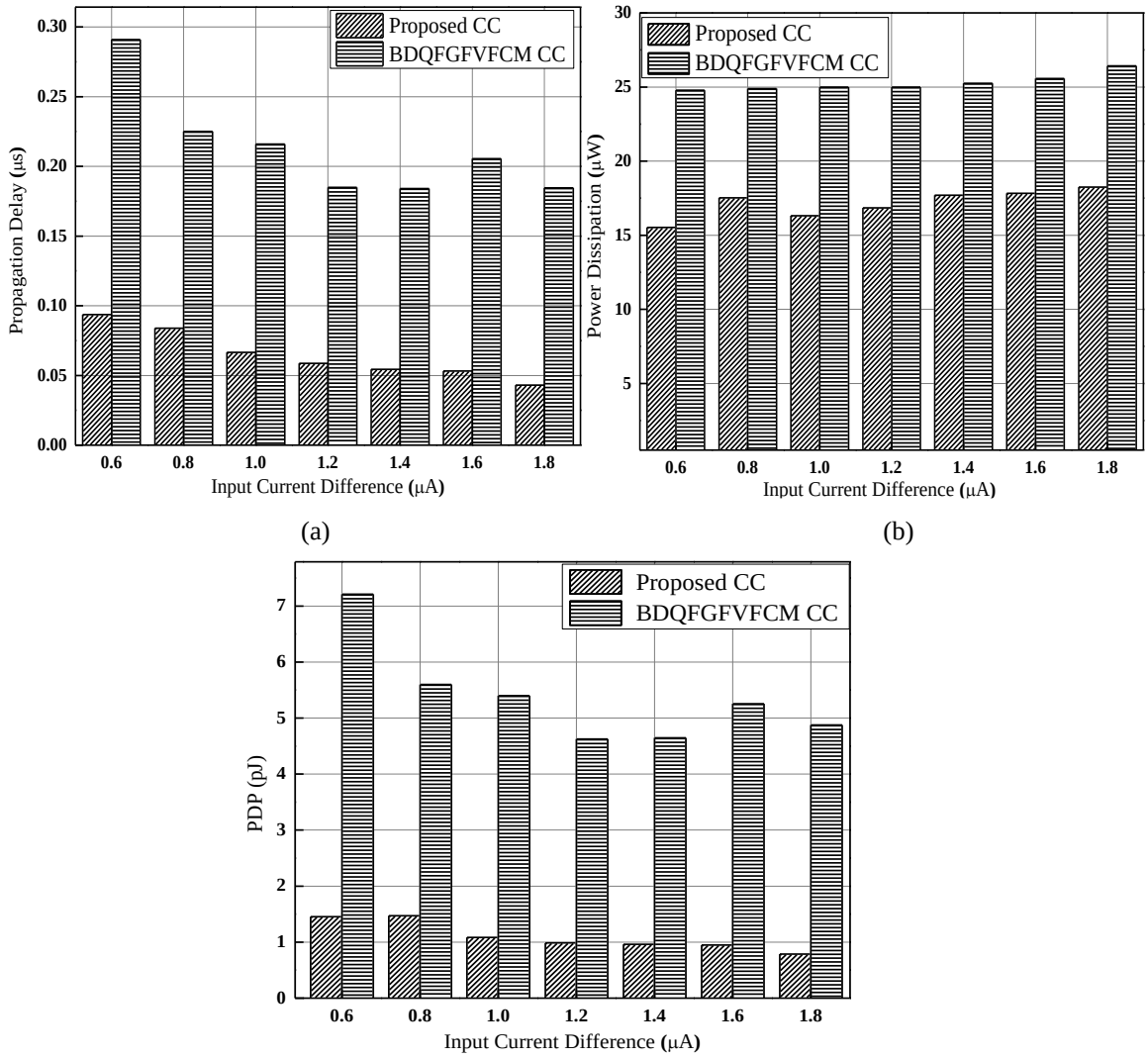


Fig. 5.7 Comparison of (a) delay, (b) Power dissipation, (c) Power delay product versus Input current difference of Proposed comparator and BDQFG FVF CM based comparator at V_{DD} =0.8 V

The proposed comparator is compared with BDQFG FVF CM based comparator and tabulated in Table 5.2. As it can be interpreted that the proposed comparator illustrated the exceptional performance under delay, power, and supply voltage.

Table 5.2- Comparative results of both comparators

Parameter	**[12]**	**Proposed Work**
Technology (μm)	0.18	0.18
Resolution (nA)	5	5
Propagation Delay (μs)	0.2055	0.053
Power Dissipation (μW)	25.576	17.832
PDP (pJ)	5.26	0.95

IMPORTANT OUTCOMES:

- The proposed current comparator has been analyzed and simulated.
- Power, delay, and PDP have been calculated and plotted.
- Our proposed design shows superior performance over the current comparator based on BDQFG FVF CM.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

Basic CM structures have been analyzed in this report. Simple, Wilson, Improved Wilson, and Cascode CMs is simulated on CMOS technology node of 180 nm, 90 nm, 45 nm, and FinFET 18 nm. For 180 nm Cascode CM shown the best performance among four of them. Where Simple CM at 180 nm node shown the 12.2 µA current at 10 µA input current. For Wilson CM at FinFET 18 nm technology node output current is 16.2% of the input current is experienced. Whereas, Improved Wilson CM has shown extreme accuracy at all technology nodes except 18 nm FinFET and a similar trend is observed in Cascode CM.

For PER at input current 10 µA, 180 nm Simple CM depicts the lowest PER. While 18 nm FinFET shows 4.6% more PER than 45 nm Simple CM. Whereas, for Wilson CM it can be seen that for a very small input current 18 nm FinFET gives a small error and then after a particular input current, its PER plot starts decreasing i.e. the error is going to achieve a higher value. For Improved Wilson CM and Cascode CM, at a particular value of I_{in}= 10 µA, 45 nm CM presents the lowest error i.e. 0.012% but after few values of input current, it slightly increases. Whereas in starting values of input current, 180 nm CM shows 7 times higher error at I_{in} = 10 µA, while at the same value 18 nm FinFET CM displayed -0.18% error. Compliance voltage of Simple CM at 180 nm current mirror exhibits 0.1-0.5 V and a similar value can be seen in 45 nm, 18 nm, and 90 nm. For Wilson CM 0.6 V is observed for 180 nm and 18 nm technology nodes. For Cascode CM 90 nm shows minimum compliance voltage i.e. 0.3 V. For Simple CM output resistance of 199 MΩ is observed for 45 nm technology node. While for 180 nm Cascode CM 8.83 MΩ the output resistance is observed. While at 18 nm 293 MΩ the resistance for Cascode CM is noticed. Overall conclusion for basic CM structure can be made that at 180 nm the cascode current mirror has been shown the better performance.

Then two advanced CM structures have been analyzed and their Monte Carlo simulation is also done. Where it is found that at input current of 15 µA PER for ELVHC CM is 4.2% and for BDQFG FVF CM is 18.7%. While for compliance voltage 0.091 V is depicted for ELVHC CM and 0.12 V is observed for BDQFG FVF CM. For ELVHC CM it is recognized that at an input current of 15 µA, the output compliance voltage is found

0.091 V. It is discovered that the output compliance voltage increases with an increase in the threshold voltage, and the same pattern is spotted in temperature variation. Further, according to Monte Carlo analysis, it is depicted that for the BDQFG FVF CM output compliance voltage is gained at 0.12 V for the input current at 15 μA and also it is viewed that as the input current is reached at its higher value, the output compliance voltage also goes increases. Also, according to process variation, it is found that as threshold voltage decreases the output compliance voltage increases. Further, as the temperature increases the compliance voltage decreases. For these two CM, it is concluded that ELVHC CM represents greater performance than BDQFG FVF CM.

The proposed current comparator has been analyzed with a comparison of BDQFG FVF CM based current comparator. This proposed comparator consists of cooperative positive-negative feedback in the current differencing stage as above mentioned current mirror and also nonlinear feedback in the gain stage. All the parameters have been simulated on Cadence Virtuoso simulator at 0.18 μm gpdk CMOS technology and over different supply voltage. Where 5 nA resolution is observed for the proposed comparator. At input current difference of 1.2 μA and 1.8 μA, the difference in delay values between both comparators is 0.13 μA and 0.14 μA, respectively on 0.8 supply voltage. At 1.2 μA current difference, 32.6 percent decrement and at 1.8 μA current difference 29.82 percent decrement from BDQFG FVF CM based current comparator in power dissipation is observed in the proposed comparator. Moreover, the proposed design experience 0.95 pJ PDP and BDQFG FVF CM based current comparator depicts 5.26 pJ PDP.

The conclusion can be made that the proposed comparator is based on ELVHC CM which shows the low power and is suitable for low voltage application.

6.2 FUTURE SCOPE

Based on the analysis, it is concluded that at lower technology node analog CM can’t be work properly. As technology nodes getting shrinking down their performance is also degrading. For more improvised current comparators, new techniques can be carried out in practice. Also, the gain stage, current differencing stage, and output stage can be improved using different structures and different devices. Using improvised CM in the current comparator will directly upgrade the performance of the comparator and its applications. As the current comparator is promising and a fundamental part of digital

devices, speed and power are important aspects. In the future, there can be a lot to do for increasing performance.

LIST OF PUBLICATIONS

Published

1. M. and P. Mittal, "Performance Comparison of FinFET based Different Current Mirror Configurations," *Third International Conference on VLSI, Communication and Signal Processing (VCAS 2020)* (ISSN: 1876-1100), MNNIT, Allahabad, UP, India, 9-11 Oct, 2020 (Published by Springer, **Scopus Indexed**). DOI: 10.1007/978-981-16-2761-3.
2. Monika and P. Mittal, "Different Current Mirror Topologies at Multiple Technology Nodes: Performance Comparison and Parameters Extraction", *International Conference on Simulation, Automation & Smart Manufacturing (SASM 2021)*, to be organized by GLA University, Mathura, 20-21 Aug, 2021 (**Accepted,** to be published by IEEE, **Scopus Indexed**).

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