Memristor Based Memory Design

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CERTIFICATE

This is to certify that the thesis entitled "**Memristor Based Memory Design"** submitted by Damyanti Singh (2K18/PhD/EC/02) to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi, for the award of the degree of Doctor of Philosophy is based on the original research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirement of the regulations relating to the degree. It is further certified that the work presented in this thesis is not submitted to any other university or institution for the award of any other degree or diploma.

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DECLARATION

I hereby declare that the work presented in this thesis entitled "**Memristor Based Memory Design**" has been carried out by me under the supervision of **Prof. Neeta Pandey**, Department of Electronics & Communication Engineering, Delhi Technological University, Delhi and **Prof. Kirti Gupta**, Department of Electronics and Communication Engineering, Bharati Vidyapeeth's College of Engineering, Delhi and is hereby submitted for the award of the degree of Doctor of Philosophy in Department of Electronics & Communication, Delhi Technological University, Delhi.

I further undertake that the work embodied in this thesis has not been submitted for the award of any other degree or diploma elsewhere.

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ABSTRACT

Since the past few decades, SRAM is preferred in portable devices and it makes up a large portion of a system-on-chip area. Despite the fact that it is fast, the volatile nature limits its applications. Moreover, the continuous downscaling in technology and supply voltage encounters serious issues in device performance such as higher leakage power consumption. To overcome such issues, the researchers and academia have come up with a solution which is introduction of non-volatile memory (NVM) device with SRAM known as nvSRAM. The NVM device is generally used to back up the information in SRAM when supply voltage is turned off. Further, NVM devices can suppress leakage power consumption by turning off supply voltage of infrequently used SRAMs without loss of information. Among the different types of NVM, memristor have certain benefits such as small size, high-speed of operation, low programming voltage and compatibility with CMOS manufacturing process.

The 6T2R cell is the most common nvSRAM cell. However, it suffers with leakage issue due to the direct connection of memristor with internal nodes. To overcome this, various methods are suggested in literature. The commonly used approach is isolating memristor with internal nodes through a control transistor. Other than this, different techniques to improve nvSRAM performances like margin, power consumption, store/restore functionality are introduced in the existing work.

In most of the existing nvSRAM cells, differential write operation is performed. It needs charging/discharging of bitline pair that contributes significant percentage in total power consumption. To reduce this, a nvSRAM design is introduced in this work that performs single ended write operation and reduces write power consumption in an extent. The

proposed design uses a feedback transistor to improve write operation. It also improves store/restore performance through 1T1M structure. The presence of feedback transistor causes increment in leakage power consumption; three different approaches are suggested to overcome this.

To overcome write/read conflict, two nvSRAM designs with read decoupled (RD) port are introduced in this work. The isolation of read operation from internal nodes enhances read margin of the proposed designs. In one of the designs, the grounded gate low threshold voltage transistor is used to maintain the performance near threshold voltage. It also uses a charge pump circuit to overdrive read port to improve read performance. Another, proposed design uses column shared technique to improve write and restore performances. The 1T1M structure is used in both the designs to perform non-volatile operation.

Other than margins and power consumption, delay is also an important parameter and less attention is paid in this direction. The longer store/restore delay values may lead to loss of data. For this, three different techniques to reduce store and restore delays are presented in this work. These techniques are generic and are applicable to nvSRAM cells which uses 1T1M configuration to perform non-volatile operation. The control signals values are altered in these approaches. For verification purpose, these techniques are applied on one of the proposed designs. Other than this, a transmission gate (TG) based nvSRAM design is also introduced in this work. In existing nvSRAM cell performing single ended write operation, ~~the~~ an NMOS transistor is used to access the data. As it passes strong ‘0’ and weak ‘1’, the write ‘1’ operation speed is degraded. To overcome this, the NMOS access transistor is replaced by TG that gives both strong ‘0’ and ‘1’ and leads to improved write performance.

In this design, memristor is connected between internal node and read bitline through read pass transistor to perform non-volatile operation.

The scaling in technology and supply voltage lead to degradation in nvSRAM cell performance due to increase in sensitivity to process variations. Hence, it is required to introduce process invariant nvSRAM cells. In this work, two process invariant nvSRAM designs are introduced. Both the designs use Schmitt Trigger (ST) inverters in the core instead of CMOS inverters. The ST inverter provides tolerance against process variations specially at lower voltages. Also, the RD port is used to perform read operation. In one of the designs, memristor is connected between internal node and read bitline line to perform non-volatile operation. Another design uses 1T1M structure to perform non-volatile operation. Further, the failure probability analysis is carried out to examine the performance of both the proposed designs against process variations and Vmin values are observed through the analysis.

In the thesis, the performances of proposed designs are analyzed through SPICE simulations and TiO_2 based memristor model is used to perform non-volatile operation. The results of proposed designs are compared with the considered nvSRAM cells. The supply voltage variation study is also performed for completeness.

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Chapter 1

Introduction

1.1. Motivation

In electronic portable devices, most of the chip area is occupied by static random access memory (SRAM). Thus, it is necessary to design low power SRAM cells to enhance the battery life of portable devices. Tremendous efforts have been devoted in SRAM cell design to address issues related to device [1]–[3], technology [4], [5], and applications [6], [7]. The methods such as power gating [8], [9], clock gating [10], [11] and voltage scaling [12], [13] are widely used to design low power SRAM cells. Among these, voltage scaling is the most popular approach to reduce the power consumption due to its quadratic dependency. Although, this method reduces the power consumption; it degrades device performance at the lower voltages [12], [13].

In SRAM array, the required cell is selected using address decoder, while rest of the unselected SRAM cells remain in idle state. The unselected SRAM cells consume static power in addition to the selected cell [14]. The SRAM cell being volatile in nature retains data as long as it is powered up. Thus, the unselected cells cannot be turned off to save power. This issue can be resolved if non-volatile feature is added in SRAM cells. There are some non-volatile devices available in the literature which have been added in SRAM cell to add non-volatile feature. Due to the intense demand for a high-density, high-speed, and low-power non-volatile memory (NVM) in semiconductor industry, the market of NVM device has grown much faster than the entire semiconductor market in recent years [15]–[17]. There are mainly five types of non-volatile memory technology: Flash memory, ferroelectric random-access memory (FeRAM), magnetic random access memory (MRAM), phase-change memory (PCM), resistive random access memory (RRAM) and memristor [18], [19]. Flash memory is an electronic storage device that uses a floating gate cell design to remember

its state before being switched OFF [18], [19]. In FeRAM, the polarization properties of a ferroelectric substance are used as a memory device [18], [19]. MRAM stores the data in magnetic storage element while in PCM, data storage is based on reversible phase conversion between the amorphous and the crystalline state of a glass [18], [19]. In RRAM, the data is stored in the form of resistive state of dielectric material which is sandwiched between conducting plates through a filament or conduction path formed [19]. Memristor follows the same working principle as RRAM. It is formed by sandwiching undoped titanium di-oxide (TiO_2) and doped oxygen deficient titanium dioxide (TiO_{2-X}) layers between platinum (Pt) electrodes [20]–[22]. It is considered as a strong candidate among existing NVM devices due to its compatibility with CMOS technology, high speed and low power consumption [19]. Hence, in this work, memristor based memory cells are worked upon and are commonly reflected as non-volatile SRAM (nvSRAM) cells.

1.2. Literature review

In literature, several memristor based memory (nvSRAM) cells are available which use either one, two or three memristors to add non-volatile feature in SRAM cell [23]–[45]. In most of the nvSRAM cells, the conventional 6T SRAM cell is used as the core [23]–[41]. A brief discussion on existing nvSRAM cells is given here.

The first nvSRAM cell is 6T2R cell having six transistors and two memristors as shown in Fig. 1.1 [23]. The back-to-back connected inverter pair formed by transistors Mn1-Mp1 and Mn2-Mp2 stores a single bit of data at internal nodes Q and QB. The access transistors Mn3 and Mn4 are controlled by wordline WL. The complimentary bitline pair BL and BLB represents the data during both write and read operation. Memristors controlled by a signal CTL are connected at both the internal nodes to add non-volatile feature. The detailed

operation of 6T2R nvSRAM cell [23] along with the performance metrics are discussed below.

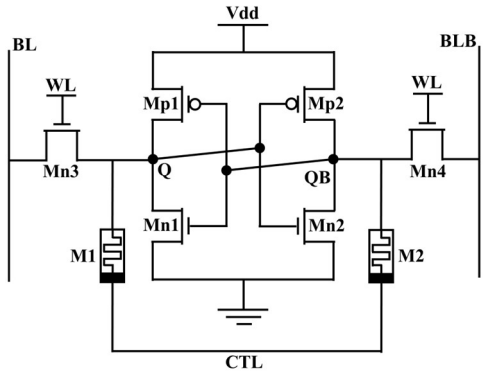

Fig. 1.1. Schematic of 6T2R cell [23]

Write operation

A write operation refers to the manner of updating the cell contents with new data. In this operation, the bitline pair is pre-charged to Vdd prior to write operation and the signal CTL is asserted HIGH. For a write '1' operation, BL remains at Vdd, while, BLB is discharged to ground potential (GND). After this, write wordline (WL) is asserted HIGH such that the internal node Q gets charged to Vdd through transistor Mn3. On the other side, the internal node QB is discharged to GND through transistor Mn4. The following design metrics are used to characterize the write performance of the cell.

- *Write margin (WM):* It is characterized by the write trip point which defines the maximum amount of voltage needed to flip the data of internal node of the cell. The WM is measured as the difference between Vdd and write trip point [46]. In this work, the word line sweep method is used to determine write trip point and WM of the cell [47], [48].
- *Write delay:* It is defined as the time interval between 50% activation of WL signal and the time when internal node Q reaches 50% of its full swing value [46].

- *Write power consumption:* It is defined as the dynamic power consumed during writing of new contents in the nvSRAM cell.

Read operation

The read operation refers to manner in which the stored contents are read from the nvSRAM cell. The bitline pair is pre-charged prior to read operation. For a read '1' operation, the signals WL and CTL are asserted HIGH. The bitline BL remains at Vdd while the BLB gets discharged via transistors Mn4 and Mn2. The potential difference in bitline pair is sensed by a sense amplifier. The read '0' operation is also performed in the similar manner. In read operation, the following design metrics of the cell are taken into account.

- *Read margin (RM):* It is determined as the maximum amount of DC noise voltage that can be tolerated by cross coupled inverter pair without state flip or a destructive read. It is measured by fitting the largest square inside the butterfly curve wherein the side length of the square is considered as RM [46].
- *Read delay:* It is given as the time delay between 50% of WL activation to 10% of pre-charged voltage difference between the bitline pair [46].
- *Read power consumption:* It is determined as the power consumed by the nvSRAM cell during read operation.

Hold operation

In hold operation, WL is asserted LOW, while, signal CTL is asserted HIGH. The back-to-back connected inverter pair maintains the cell data. The hold operation is characterized by the following design metrics.

- *Hold margin (HM):* It is defined as the maximum amount of DC noise voltage that can be tolerated by back-to-back connected inverter pair such that the cell retains its data.

The butterfly curve method is used to measure the HM of the cell [46]. The side length of the largest square that can be fitted inside the butterfly curve gives HM value.

- *Leakage Power Consumption:* It is defined as the amount of power consumed when nvSRAM cell is in hold state [46].

Non-volatile operation

The non-volatile operation consists of store, power down and restore operations. In store operation, the content at internal nodes Q and QB are stored in memristors M1 and M2, while, in restore operation, the contents are rewritten on the internal nodes after power down. When, a positive potential is applied across memristor, the oxygen deficiencies occupy most of the device thickness. In this position, memristor is said to be in low resistance state (LRS) and it is denoted by R_{ON}. If negative voltage is applied across memristor, the amount of oxygen deficiencies is reduced and thickness of undoped region is increased. In this position, memristor is said to be in high resistance state (HRS) and is represented by R_{OFF}.

It is assumed that the internal node Q is at logic '1', while internal node QB is at logic '0'. During store operation, the signal CTL is asserted LOW such that a positive potential difference is developed across memristor M1. It helps in changing the state of memristor M1 to LRS, while, memristor M2 continues to remain in HRS state due to zero potential difference across it. The store operation is followed by power down mode. In this mode, the power supply is turned off and the data stored on internal nodes is lost. However, both the memristors maintain their respective states. When the power supply is turned on again, the data is restored at the internal nodes through the restore operation.

In restore mode, CTL is asserted HIGH. As memristors M1 and M2 are in LRS and HRS states, respectively, therefore, the internal node Q gets charged faster than QB. Thus, logic

'1' is restored on internal node Q, whereas internal node QB attains logic '0' due to back-to-back connected inverter pair. After completion of restore operation, the memristors are reset to their initial HRS state by raising CTL signal above Vdd. The following design metrics are analysed during non-volatile operation.

- *Store delay:* It is given as the time required to change the state of memristor from HRS to LRS during store operation.
- *Store power consumption:* It is represented as the power consumed by the nvSRAM cell while performing store operation.
- *Restore delay:* The restore delay is given as the time required to recover the data from memristor to internal node of the cell after power down operation.
- *Restore power consumption:* It is represented at the power consumed by the nvSRAM cell during restore operation.

Further, a close look at Fig. 1.1 shows that a current, however, small may flow through memristors as internal nodes store complimentary data leading to degraded cell stability. Thus, few additional transistors are included in the cell along with memristors to achieve non-volatile feature with improved performance. The nvSRAM cells [24]–[41] work on this methodology.

The 7T2M cell [24] is modified version of 6T2R cell [23] wherein a control transistor is placed between common node of memristor and GND. The write and read performances of 7T2M cell [24] are similar to 6T2R cell [23]. The control transistor is activated during store and restore operations only. During store operation, both the memristors are set to different states due to difference in data available at both the internal nodes. In restore operation, the data is recovered at internal nodes according to respective memristor state. The 7T2M cell

[24] cell aims to increase the stability during write/read operations; however, it has memristor connection same as 6T2R cell [23] and hence, the leakage issue is still there.

The 7T2R cell [25] retains the structure of 6T2R cell [23]. An additional switch transistor (RSW), controlled by signal CTL, is connected between bitline BL and common node of memristors. The RSW transistor provides a parallel path during write operation that improves the WM and write delay in comparison to 6T2R cell [23]. The read operation remains similar to 6T2R cell [23]. During store and restore operations, the RSW transistor remains ON. In store operation, the internal node data is transferred to memristor and its state is changed accordingly, while, in restore operation, the data is rewritten to internal nodes of the cell. The direct connection of memristor with internal nodes of the cell still exists in 7T2R cell [25] and hence, the leakage issue remains unresolved. The Rnv8T2R cell [26] also uses conventional 6T SRAM cell in the core. This cell has two additional transistors each connected between the internal node and corresponding bitline. During write operation, two write paths exist that enhances WM and reduces write delay of the cell. In read operation, the switch transistors are turned off and the cell behaves as 6T2R cell [23]. The absence of direct path between internal nodes and memristors that exists in 7T2R cell [25], reduces the leakage in the cell. In store operation, two subphases namely set and reset are performed to change the memristor state. In restore operation, the original data is recovered in the cell depending on memristor state. Although, the leakage and stability issues are resolved in this cell, the presence of two memristor paths increase the store/restore power consumption. Also, due to two parallel write paths, the write power of the cell is also increased.

The initialization and overwrite (IOW) 7T1R cell [27] introduced an alternate approach to improve cell performance. In this cell, the inverters of latch are operated at different power supply during write operation. The driving capability of the inverter powered by higher

supply voltage than other inverter leads to improvement in WM. The read operation is similar to 6T2R cell [23]. Moreover, the IOW 7T1R cell [27] has a single memristor connected between internal node Q and switch transistor (RSW) which is further connected to switch line (RSL) instead of BL. The store operation takes place in set and reset phases while restore operation need two phases: differential supply initialization (DSI) and pulse overwrite (POW). The IOW 7T1R cell [27] needs to change the state of one memristor only that reduces store/restore power consumption of the cell in comparison to Rnv8T2R cell which requires changing the state of two memristors [26].

The average 7T1R cell [28] further improves WM and reduce restore power consumption in comparison to IOW 7T1R cell [27]. Here, a column shared switch transistor (SN) is used to improve WM of the cell. The SN transistor is turned off during write operation. It reduces pull-down strength and improves WM of the cell. The read operation is similar to 6T2R cell [23]. However, SN transistor is turned on during read operation which reduces RM slightly therefore the cell uses read favoured sizing of transistors. The store operation is similar to IOW 7T1R cell [27]. The restore operation is carried out in two phases namely, circuit self-recovery (CSR) phase and resistance dependent recovery (RDR) phase. As the restore operation is similar to write operation, the presence of SN transistor helps in restore power reduction in comparison to IOW 7T1R cell [27]. Although, the average 7T1R cell [28] improves WM and reduces restore power consumption of the cell, the subphases in store and restore operations increase the cell complexity and, hence, reduces the store/restore operation speed.

In 8T2R cell [29], [30], the combination of memristor and transistor (1T1M structure) is connected to both the internal nodes, while in 8T2R cell [31], the NMOS transistor of 1T1M structure are replaced by PMOS transistors. The write and read operations are similar to 6T2R

cell [23]. In these cells, the memristor needs to reset to their initial state prior to store operation by providing voltage more than Vdd. Although, the complexity during store operation is reduced, the presence of two memristors and voltage needed to reset memristor to their initial state, cause increase in store/restore power consumption. In 7T1R cell [32], the 1T1M structure in connected to internal node Q only. It also needs to reset the memristor to its initial state prior to store operation, however, it does not need voltage more than Vdd. It results in reduction of store/restore power consumption in comparison to 8T2R cell [29]–[31]. Also, it performs write and store operation at the same time, this leads to increment in write/store delay and decrement in WM.

The 7T2M cell [33] uses two memristors wherein one of them improves volatile performance of the cell while the other perform non-volatile operation. The first memristors is placed between pull-down transistors and GND terminal. It is set to HRS state during write operation which reduces the pull-down strength of inverter pair and enhances WM of the cell. The memristor is set to LRS state during read operation and works similar to 6T2R cell [23]. The second memristor is connected to internal node Q through a transistor. Two signals are used to control operation of transistor and memristor, respectively, during store/restore operation. The 7T2M cell [33] also overcomes the issue of complex store/restore operation, however, the cell shows increased store/restore delay. The 8T3R cell [34] is modified form of 7T2M cell [33]. Here, the 1T1M structure is connected at both internal nodes. The store and restore operations are performed through two paths leading to improvement in store/restore delay, however, it increases store/restore power consumption.

The 8T1R cell introduced in [35], maintains the cell stability by performing differential write/read operations similar to 6T2R cell [23]. The control transistors are connected at both the internal nodes of the cell and a memristor is connected in between. During store operation

the control transistors are activated by applying voltage more than Vdd whereas an additional circuit is required for restoring data. The restore circuit provides delay to power supply of both the inverters. Due to this, there is increase in restore delay and power consumption of the cell.

An alternate structure of 8T1R cell is introduced in [36]. It uses 1T1M structure, connected between both the internal nodes Q and QB, to perform non-volatile operation. An additional transistor (gate and drain terminal connected to bitline BL and source terminal connected to internal node Q) is used to store and restore data. The store operation takes place right after write operation. The set and reset phases are required to store data into memristor which necessitates charging/discharging of bitline BL. After store operation, the read operation take place and it is followed by power down mode and restore operation. The data is recovered into cell according to memristor state. The main advantage of this structure is the use of a minimal number of signals (BL, WL and Vdd). The drawback of this structure is related to the store and restore operations complexity, which is executed in two steps.

A modified version of 7T2R [25] is presented in [37] as TG 7T1R which uses transmission gate (TG) in place of access transistors. It improves write performance of the cell as TG provides two parallel write paths. This structure [37] uses a single memristor to support non-volatile operation, therefore, it has better store/restore power consumption than the cells employing two memristors.

Another structure 7T1R cell [38] is introduced in literature that uses single bitline BL to perform write operation. However, in the single ended write operation, the WM of the cell degraded due to asymmetrical structure [46]. It also gives reduced write power consumption. The read operation is performed through a reference resistor and sensing the voltage across it. The store and restore operations are performed in similar manner to 7T2M cell [33].

In nvSRAM cells mentioned above, the read/write conflict issue exists as the same port is used to perform read/write operation. In 6T2R cell [23], shown in Fig. 1.1, the pull-down transistor Mn1/Mn2 has to be stronger than access transistor Mn3/Mn4 for successful read operation. For write operation, the access transistor Mn3/Mn4 need to be stronger than pull-up transistor Mp1/Mp2. As the requirement for read and write operations are conflicting in nature, there is a need to analyse the sizing issues separately for read and write assist transistors [46]. Another way is to decouple the read operation by using a separate read port. The nvSRAM cells [39]–[41] has a read decoupled (RD) port to perform read operation. The 9T2R cell [39] is a modified form of Rnv8T2R cell [26]. A RD port having read pass transistor (RPT) controlled by internal node Q with separate read bitline (RBL) is used to read data on internal node. The read decoupled 9T2R cell [39] has high RM. The 9T2R cell [39] reads opposite data and, hence, an additional inverter is required to retrieve original data. The write, store and restore operations remain similar to Rnv8T2R cell [26].

The RD 8T1R cell [40] has a read decoupled port comprised of a read pass transistor (RPT) and a read decision transistor (RDT). The read wordline (RWL) and internal node QB controls operation of RPT and RDT, respectively. The non-volatile operation is achieved by connecting a memristor between internal node Q and RPT. Additionally, this cell uses two function and word sharing transistors: gate enabled transistor (GET) and write assist transistor (WAT) which are controlled by WCT signal. These transistors are used in write and restore operations, assisting write and data recovery process, respectively. The store operation takes place in two subphases: set and reset. The restore operation also requires two subphases, namely: self-recovery ‘0’ (SR) and memristor data recovery (MDR). After restore operation, the opposite data is recovered in the cell, hence, an additional inverter is required

at output stage to get original data. The multiple sharing (MS) 7T1R cell [41] is similar to RD 8T1R cell [40] except write operation. It performs single ended write operation in contrast to differential write operation in [40]. The read, store and restore operations are similar to RD 8T1R cell [40]. In these cells, the read decoupled port enhances the RM, while, the shared per word scheme improves write and restore performances.

The above study reveals that the write delay and WM are improved by using additional transistors, differential power supply rails, column shared transistor, memristor between pull-down transistors and GND terminal of inverter pair and using TG in place of access transistors. It is also observed that the read decoupled port and shared per word scheme can be used to improve read and WM of the nvSRAM cell, respectively. Limited investigations are done on improving write delay of the cells. Further, there is no specific technique for reducing store/restore delay. In small geometry devices, the inter die and intra die process variations limit the memory cell operations especially near threshold region. It may result in threshold mismatch between adjacent transistors in memory cell which may lead to memory failure. This aspect in context of nvSRAM cell design is not looked into.

1.3. Research gaps

Based on study of literature on memristor based memories, following research gaps are identified:

1. The researchers have concentrated toward improving the WM and write delay of nvSRAM cell. The efforts to reduce write power are limited. Therefore, there is a need to design a novel nvSRAM cell with reduced write power consumption.
2. Most of the existing nvSRAM cells perform write and read operation through a common port wherein read/write conflict exist that degrade the overall performance.

So, novel read decoupled nvSRAM cells wherein different techniques to enhance read and write performances are required.

3. The main thrust in nvSRAM cells is to enhance read stability and write ability, however, the delay performance of the cell remains bottleneck.
4. There is an impact of technology scaling and process variations on the performance of nvSRAM cell. Hence, it is necessary to introduce process invariant nvSRAM cells.

1.4. Research objectives

Based on the gaps the following objectives are formulated:

1. To design memristor based memory with improved write performance.
2. To design memristor based memory with improved read margin.
3. To improve delay performance of memristor based memory.
4. To design process invariant memristor based memory cell.

1.5. Organization of the thesis

The focus of this research is on nvSRAM cells and improvement in its performance. The organisation of this research work is presented in chapter-wise format as follows:

Chapter 1

This chapter outlines the issues of SRAM cell in portable devices. The introduction of non-volatile memory (NVM) devices with SRAM cell has emerged as one of the possible solutions to these issues. The working of a nvSRAM cell and its performance parameters are briefly described. The available nvSRAM cells are reviewed followed by identification of research gaps and laying down of research objectives.

Chapter 2

In this chapter, a novel low power 8T1M nvSRAM cell (Proposed design 1) is introduced. The detailed explanation on working of the Proposed design 1 is put forward and its operation is verified through timing waveforms. The write performance, read performance, store and restore performances of the Proposed design 1 are compared with its 8T nvSRAM counterparts. The leakage power analysis for Proposed design 1 is also studied and three different cases are introduced to reduce it. The supply voltage variation study is also carried out for the sake of completeness.

Chapter 3

This chapter presents two nvSRAM cells with read decoupled port (Proposed design 2 and 3) to improve read performance. The techniques to improve WM are also applied to the Proposed designs. The Proposed design 2 aims to improve its performance near threshold voltage. In Proposed design 3, the column shared technique is used to improve the cell performance. The performances such as write, read, store and restore are verified through simulations and the results are compared with considered read decoupled nvSRAM cells. The supply voltage variation study is also carried out for each performance parameters.

Chapter 4

This chapter uses transmission gate as access transistor in read decoupled nvSRAM cell (Proposed design 4) to improve write delay. The write, read, store and restore performances are studied for the Proposed design and the results are compared with considered nvSRAM cells. Further, three techniques namely boosted CTL1, negative CTL2 and floating Vss are introduced to reduce store and restore delays. These techniques are applied on the Proposed design 1 and a comparison is made to evaluate the effect of each introduced technique on

store and restore delays. The supply voltage variation study is also carried out for each performance parameter.

Chapter 5

This chapter put forward two process invariant nvSRAM cells (Proposed design 5 and 6) which use read decoupled port. Both Proposed designs use Schmitt trigger inverter as core which helps in maintaining performance against process variation. The performance of the Proposed designs is verified and is compared against available RD nvSRAM cells, Proposed design 2, Proposed design 3 and Proposed design 4. The impact of process variation on cell performance is examined. The failure probability analysis is carried out to check the stability of the cells under process variations. Further, the leakage power analysis is also carried out for the Proposed designs. The supply voltage variation study is also carried out for the sake of completeness.

Chapter 6

This chapter summarizes the work presented in the thesis. It also gives the idea for the future work which can be carried out to improve nvSRAM cell functionality.

Chapter 2

nvSRAM Cell with Improved Write Performance

The contents of this chapter are published in:

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2.1. Introduction

In battery operated portable devices, most of the power is consumed during memory access that have significant impact on battery life [49]. In these portable devices, SRAM cell occupies major chip area and consumes significant amount of active power and leakage power. The reduction in leakage power can be achieved by addition of memristor with SRAM cell that leads to introduction of nvSRAM cell [39]. It enables a portable device to switch off its power supply to suppress leakage power without a loss of data. The active power can be effectively reduced in two manners: (1) by lowering the supply voltage as it is quadratically dependent on total power consumption and (2) by lowering charging/discharging of capacitance of word and bitline [49] as upto 60% of total active power is consumed in charging/discharging of bitlines during write operation [50], [51].

In this chapter, eight transistors based nvSRAM cell (Proposed design 1) is introduced which performs single ended write operation and differential read operation. For this, a feedback transistor is introduced in feedback path of back-to-back connected inverter pair. This feedback transistor remains off during write operation and remains on otherwise. To perform non-volatile, a combination of a transistor and a memristor (1T1M) is used. A brief discussion on existing 8T nvSRAM cells is presented in section 2.2. Thereafter, the working of Proposed design 1 during write, read, hold, store and restore operations is elucidated in section 2.3. This section also includes the timing waveform of Proposed design 1 during non-volatile operation. The performance parameters of Proposed design 1 are also analysed and compared with the considered 8T nvSRAM cells during different operations. Different design cases to reduce leakage power consumption of Proposed design 1 are also introduced. The findings are comprehended in section 2.4.

2.2. Existing 8T nvSRAM cells

In this section, a brief review on 8T nvSRAM cell is carried out. The core of these cells is similar and comprise of back-to-back connected inverter pair to store single bit of data. The access transistors perform differential write and read operations. The difference resides in non-volatile functionality of the cells.

The available 8T nvSRAM cells resolve leakage issue of 6T2R cell [23] by adding a control transistor that eliminates the current path through memristor. The 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35] and 8T1R cell [36] uses 1T1M structure at the internal nodes to perform non-volatile operation. The nvSRAM cells [29], [35] perform write operation through access transistors whereas, an additional path for write operation is formed through memristor in the nvSRAM cells reported in [26], [36].

Further, in Rnv8T2R cell [26], 8T1R cell [35] and 8T1R cell [36], the set and reset phases are required to perform store operation. It needs supply voltage and control signal value V_{SET} which is set voltage of memristor. Although, the 8T2R cell [29] does not need set/reset phase, it needs control signal value more than Vdd to perform store operation. The restore operation of 8T1R cell [35] requires a restore circuitry for the delayed activation of the supply voltage of inverters. In 8T1R cell [36], the restore operation is performed in two phases which are quite complex. Moreover, in nvSRAM cells [29], [36], memristor needs to initialize to its initial HRS state by performing reset operation.

From above discussion, it is observed that in 8T2R cell [29], the supply voltage more than Vdd is required to perform both store and restore operations. Also, an additional reset phase is required to initialize memristor to HRS state prior to store operation. In Rnv8T2R cell [26] and 8T1R cells [35], [36], the set and reset phases are required during store operation. Hence,

due to need of high supply voltage and multiple phases during store and restore operations, the store and restore power consumptions and complexity is increased.

Also, in most of the existing 8T nvSRAM cells [23], [26], [29], [35], [36] differential write operation is performed. The probability of discharging one of the bit line pair equals '1' which means that the activity factor of switching the bit line pair equals '1'. The bitline power consumption is given as $P = \alpha_{WBL} * C_{BL} * V_{dd}^2 * f_{write}$ where $\alpha_{WBL} = 1$. The use of single bitline to perform write operation can reduce the switching activity factor α_{WBL} to '0.5' which effectively reduces the active power consumption [52]. It also exploits the fact that most of the bits in SRAM are "zeros" for both data and instruction memories to reduce the write power consumption [53], [54]. Hence, it is required to introduce nvSRAM cell that exhibit simple store and restore operations and has reduced write power consumption.

2.3. Proposed design 1

The Proposed design 1 is an eight transistor with one memristor nvSRAM cell as shown in Fig. 2.1. It exhibits single ended write and differential read operations through its bitline pair (WBL and WBLB). It consists of back-to-back inverters (Mn1-Mp1 and Mn2-Mp2), connected through a feedback transistor, to store the data on internal nodes Q and QB. The transistors Mn3 and Mn4 are the access transistors controlled by write wordline (WWL) and read signal (R), respectively. A feedback transistor Mf1, controlled by write signal (W), is introduced to exhibit single ended write operation by disconnecting the feedback connection between inverters. Thus, there exist a sequential storage of data on two internal nodes, thereby lowering the write power consumption of Proposed design 1. Alternatively, transistor Mf1 turned on during the read operation to retain the advantage of fast differential read as

exhibited in considered 8T nvSRAM cells. The control signals CTL1 and CTL2 monitor the operation of 1T1M non-volatile structure.

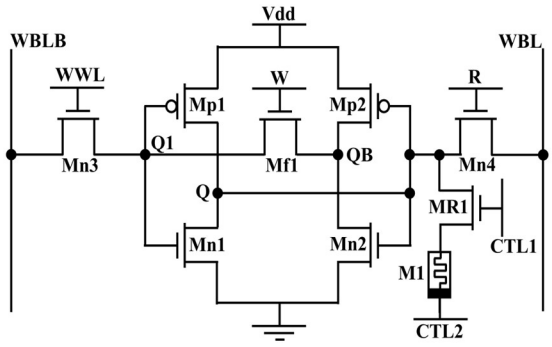


Fig. 2.1. Schematic of Proposed design 1

2.3.1. Operation of Proposed design 1

In this subsection, the operation of Proposed design 1 is described during write, read, hold, store and restore operations. The status of control signals during each operation is summarized in Table 2.1.

Table 2.1. Operating Condition of Proposed design 1

Signals	Operations				
	Write	Read	Hold	Store	Restore
WWL	HIGH	HIGH	LOW	LOW	LOW
R	LOW	HIGH	LOW	LOW	LOW
W	LOW	HIGH	HIGH	HIGH	HIGH
CTL1	LOW	LOW	LOW	HIGH	HIGH
CTL2	LOW	LOW	LOW	LOW	HIGH

Write operation

In a write operation, the two bitlines WBL and WBLB are pre-charged to Vdd prior to writing new data values in the Proposed design 1. The control signals are asserted as mentioned in

Table 2.1. The resulting structure represents cascade of two inverters as shown in Fig. 2.2. The new data loaded on the WBLB line gets stored at node Q1 through transistor Mn3, which is then updated sequentially at internal nodes Q and QB through the two inverters (Mn1-Mp1, Mn2-Mp2).

During a write '0' operation, WBLB remains at Vdd (logic 1) and the cascade of two inverters stores logic '0' and logic '1' at nodes Q and QB sequentially. Thus, it can be noted here that the Proposed design 1 eliminates the need of discharging of WBL bitline in contrast to considered 8T nvSRAM cells. This reduces the activity factor α_{WBL} of the bitlines and reduces write power of the Proposed design 1 in a write '0' operation. Alternatively, in write '1' event, the WBLB line discharges, in such cases Proposed design 1 consumes the same power as the considered 8T nvSRAM cells.

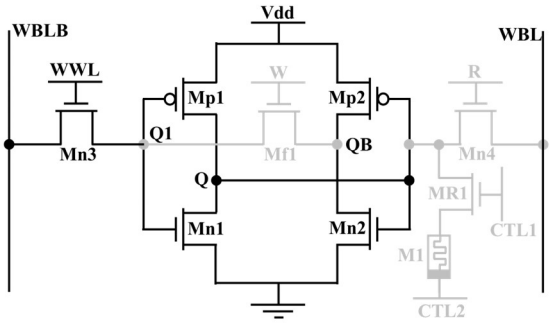
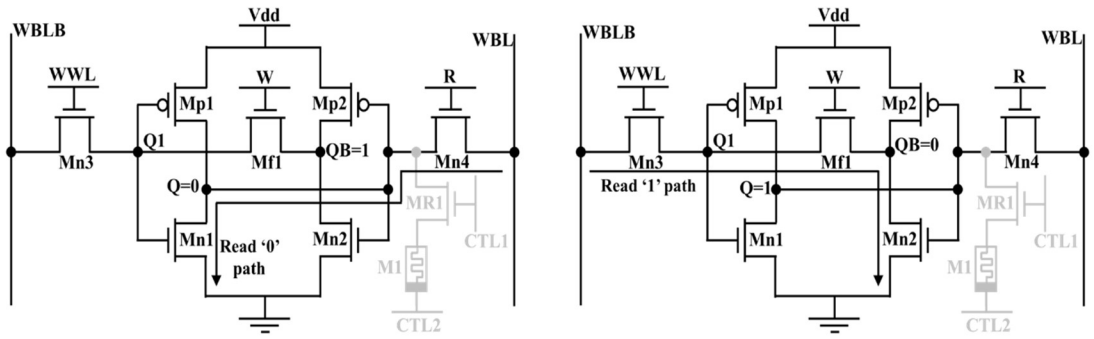


Fig. 2.2. Proposed design 1 during write operation

Read operation

The Proposed design 1 exhibits differential read operation. The bitlines WBL and WBLB are pre-charged to Vdd prior to read operation. The control signals are asserted as enlisted in Table 2.1. Depending on the value stored at internal nodes, a discharge path is formed through either of the two bitlines, as illustrated in Fig. 2.3. For a read '0', WBL discharges through Mn4 and Mn1 as depicted in Fig. 2.3(a). Alternatively, in a read '1' event, WBLB

discharges through a path consisting of three transistors Mn3, Mf1 and Mn2 as represented in Fig. 2.3(b). The difference in number of transistors in discharging requires optimum sizing of transistors.



(a) (b)

Fig. 2.3. Proposed design 1 during (a) read '0' and (b) read '1' operation

Hold operation

The control signals are asserted as tabulated in Table 2.1 during hold operation. The access transistors remain off in this operation. The data is stored in the Proposed design 1 by back-to-back connected inverter pair as feedback transistor Mf1 is working as shown in Fig. 2.4.

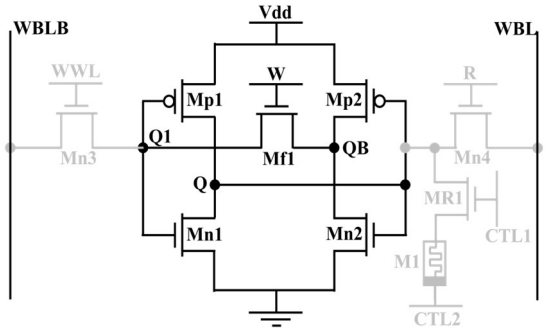


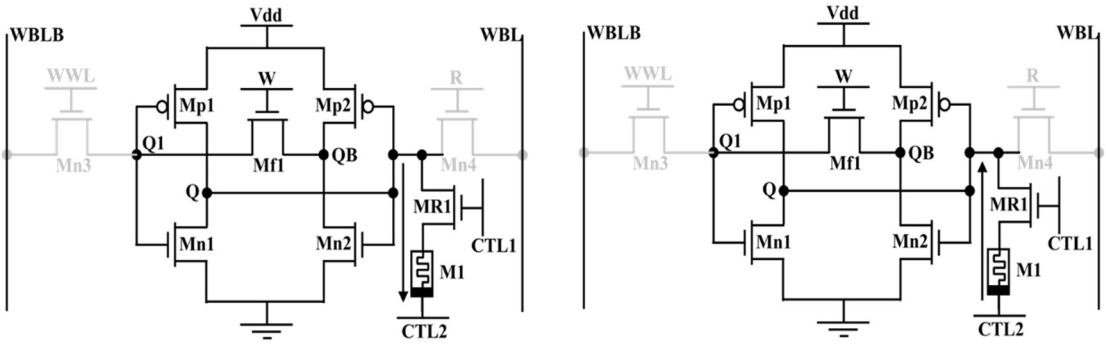
Fig. 2.4. Proposed design 1 during hold operation

Non-volatile operation

The non-volatile operation of Proposed design 1 comprises of store, power down and restore operations. It is performed after write (logic '1' or logic '0') operation. It is pertinent to

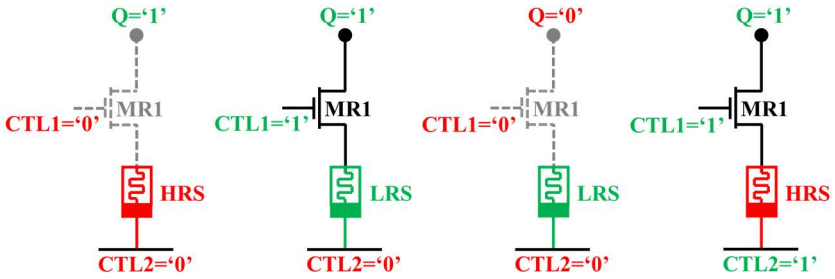
mention that the initial state of memristor M1 is HRS irrespective of the internal node content.

In store operation, the signals (CTL1, W) and CTL2 are asserted HIGH and LOW, respectively. The schematic for Proposed design 1 during store operation is shown in Fig. 2.5(a). Assuming the logic '1' is stored on internal node Q, the memristor states are depicted in Fig. 2.6. In this case, the internal node Q stores logic '1', the memristor M1 changes its state from HRS to LRS as there is a negative potential across the it. During power down, the supply voltage is turned off and all the control signals are asserted LOW. Due to this, the internal nodes Q and QB lose their data while the memristor M1 maintains its LRS state. In restore operation, the supply voltage is turned on again. The control signals W, CTL1 and CTL2 are asserted HIGH while other control signals remain LOW. The schematic of Proposed design 1 during restore operation is depicted in Fig. 2.5(b). As memristor M1 is in LRS state, there is a large flow of current through transistor MR1 and the internal node Q is restored to logic '1'. The memristor M1 changes its state from LRS to HRS, which is also its initial state.



(a) (b)

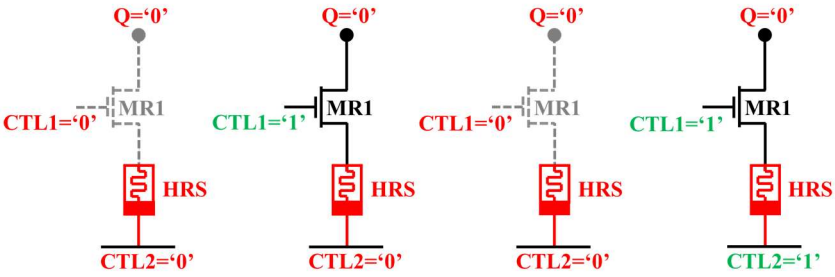
Fig. 2.5. Proposed design 1 during (a) store and (b) restore operation



(a) (b) (c) (d)

Fig. 2.6. State of memristor during non-volatile operation (a) initial (b) store (c) power down and (d) restore for logic '1'

Similarly, the states of memristor during the non-volatile operation for logic '0' is shown in Fig. 2.7. As the internal node Q is at logic '0', there is zero potential difference across memristor M1 and, hence, it does not change its state during store operation and remain in HRS. After, the store operation, power down occurs and internal node data is lost. After power down, the restore operation is carried out. As memristor M1 is in HRS state, a low current flow through it which is not sufficient to raise the potential of internal node Q and it remains at logic '0'. It can be observed that memristor M1 remains in HRS after restore operation. Thus, the Proposed design 1 does not require resetting of memristor after restore which is necessary in the considered 8T nvSRAM cells.



(a) (b) (c) (d)

Fig. 2.7. State of memristor during non-volatile operation (a) initial (b) store (c) power down and (d) restore for logic '0'

2.3.2. Simulation results and discussion

The SPICE simulations are carried out using 32nm PTM model to analyse the performance of Proposed design 1. The memristor model suggested in [55] is used to analyse the non-volatile performance. The Proposed design 1 and considered 8T nvSRAM cells are designed for same RM and the corresponding aspect ratio of various transistors are enlisted in Table 2.2. In this section, first the timing waveform of Proposed design 1 is explained at Vdd = 1.0V. It is followed by the performance evaluation during different operations and its comparison with the considered 8T nvSRAM cells.

Table 2.2. Aspect ratio of various transistors of considered 8T nvSRAM cells and Proposed design 1

Transistor	**Aspect ratio (W/L)**				
	8T2R [29]	**Rnv8T2R** [26]	**8T1R** [35]	**8T1R** [36]	**Proposed design 1**
Mn1	256nm/32nm	256nm/32nm	256nm/32nm	256nm/32nm	166.4nm/32nm
Mn2	256nm/32nm	256nm/32nm	256nm/32nm	256nm/32nm	211.2nm/32nm
Mn3	128nm/32nm	128nm/32nm	128nm/32nm	128nm/32nm	83.2nm/32nm
Mn4	128nm/32nm	128nm/32nm	128nm/32nm	128nm/32nm	64nm/32nm
Mp1	64nm/32nm	64nm/32nm	64nm/32nm	64nm/32nm	64nm/32nm
Mp2	64nm/32nm	64nm/32nm	64nm/32nm	64nm/32nm	128nm/32nm
Mf1	-	-	-	-	256nm/32nm
MR1	64nm/32nm	64nm/32nm	128nm/32nm	64nm/32nm	64nm/32nm
MR2	64nm/32nm	64nm/32nm	128nm/32nm	64nm/32nm	-

Timing waveform

The timing waveform for the complete execution of store, power down and restore logic '1' in the Proposed design 1 is shown in Fig. 2.8(a). The time period for each operation is taken as 2ns [56]. The following observation can be made:

a) The write '1' operation is performed during 0 to 2ns. The WBLB is discharged to ground and the signal WWL is asserted HIGH. The control signal W, CTL1 and CTL2 are asserted LOW. As shown in Fig. 2.8(a), the internal nodes Q and QB are written as logic '1' and logic '0', respectively.

b) From 2ns to 4ns, the store operation takes place. The control signals (W and CTL1) and CTL2 are asserted HIGH and LOW, respectively such that the transistor MR1 turns on. Since internal node Q is at logic '1' and CTL2 is at ground potential, the memristor M1 changes its state from HRS to LRS.

c) From 4ns to 6ns, the supply voltage is turned off and the control signals are asserted LOW. It can be observed that the internal node Q discharges but the memristor M1 retains its LRS state.

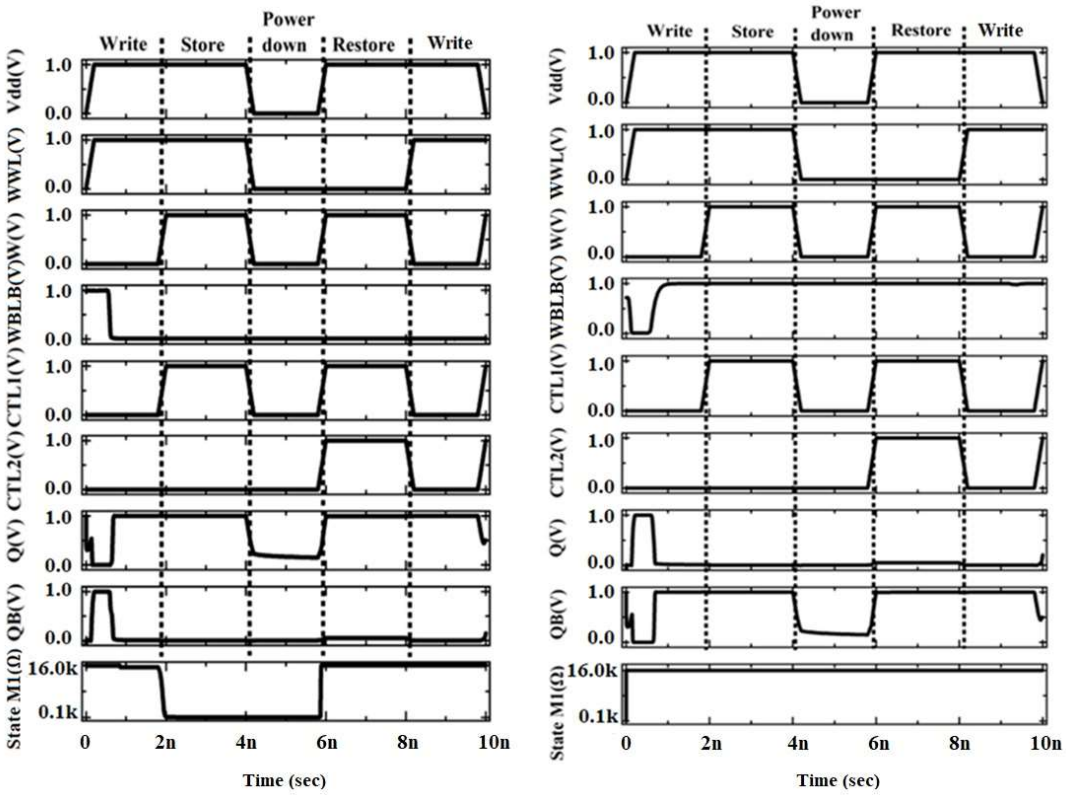
d) Finally, from 6ns to 8ns, in the restore operation, the supply voltage is turned on and signals W, CTL1 and CTL2 are asserted HIGH. The internal node Q is charged back to Vdd i.e., logic '1'. It is due to the large flow of current through transistor MR1. After restore operation, the memristor M1 changes its state back to HRS which is its initial state.

Similarly, Fig. 2.8(b) shows the complete execution for store, power down and restore logic '0' in Proposed design 1. First, the write '0' operation takes place by keeping WBLB at Vdd. In store operation, as internal node Q is at logic '0', memristor M1 continues to remain in the HRS state due to zero potential difference across it. During power down, the supply voltage is turned off. The internal nodes lose their data, however, memristor M1 retain its HRS state. Subsequently, in the restore operation, internal node Q does not get charged as memristor is in HRS state but internal node QB attains logic '1' due to the back-to-back connection of

inverters in the Proposed design 1. It is worth noting that after the restore operation, the memristor is in HRS.

Performance analysis

Various performance parameters such as margin, delay and power consumption are evaluated for Proposed design 1 during different operations. The results are compared with considered 8T nvSRAM cells. The effect of supply voltage variation is also studied for completeness.



(a) (b)

Fig. 2.8. Timing waveform for non-volatile operation of Proposed design 1 for (a) Logic '1' and (b) Logic '0'

- Write Performance Analysis

  The write performance of the Proposed design 1 is analysed in terms of WM, write delay and write power consumption. The results are also compared with the considered 8T nvSRAM cells.

Write margin (WM): The WM for considered 8T nvSRAM cells and Proposed design 1 is analysed at Vdd = 1.0V. The value of WM is observed as 371mV, 529mV, 371mV, 371mV and 505mV for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. The improvement of 26.53% is observed in the WM of Proposed design 1 in comparison to 8T2R [29], 8T1R [35] and 8T1R [36] cells. The improvement in WM of Proposed design 1 may be attributed to the writing mechanism that disconnects that feedback connection of inverter pair and eases writing into the cell. The WM of Proposed design 1 is smaller than Rnv8T2R cell [26] by 4.53% which is due to presence of extra parallel write path in the later one.

Write delay: The write delay for considered 8T nvSRAM cell and Proposed design 1 is analysed at Vdd = 1.0V. The values are obtained as 29.56ps, 27ps, 30.05ps, 29.05ps and 35ps for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. It is noted that the write delay of Proposed design 1 is increased by 15.54%, 22.85%, 14.14% and 17% in comparison to 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36], respectively. It is attributed to the fact that the new data is written on internal nodes of the Proposed design 1 through a cascade connection of inverters in contrast to the back-to-back connection of inverters as in the considered 8T nvSRAM cells.

Write power consumption: The write power consumption of Proposed design 1 and considered 8T nvSRAM cells is evaluated for different write patterns i.e., 0 – 0, 1 – 0, 0 – 1 and 1 – 1 at Vdd = 1.0V. The observations are summarized in Table 2.3 and the following points are noted:

- The write power consumption of considered 8T nvSRAM cells remain almost same for all write patterns whereas the Proposed design 1 shows very low write

power consumption for 0 – 0 and 1 – 0 write patterns. This is due to the differential write operation in considered 8T nvSRAM cells against single ended write operation in Proposed design 1.

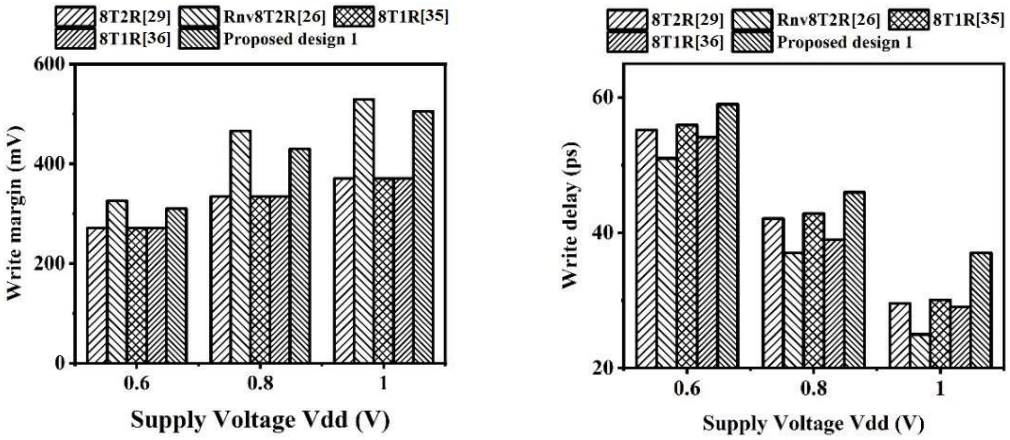
- The Proposed design 1 shows 99.5% and 96.03% power saving for write '0' with respect to considered 8T nvSRAM cells when the original cell data is '0' and '1', respectively. This is attributed to the fact that write '0' operation in Proposed design 1 does not require WBLB to discharge as exhibited in its counterparts.
- The write patterns 0 – 1 consumes more power than write pattern 1 – 1 for Proposed design 1 and considered 8T nvSRAM cells.

Table 2.3. Write power consumption (μw) of considered 8T nvSRAM cells and Proposed design 1 at Vdd=1.0V

nvSRAM cells	**Write power consumption (μW) for different write patterns**			
	0 - 0	**1 - 0**	**0 - 1**	**1 - 1**
8T2R [29]	98.83	101.11	100.98	98.85
Rnv8T2R cell [26]	104.81	109.78	110.88	104.45
8T1R [35]	98.51	101.35	100.65	98.86
8T1R [36]	99.85	102.01	101.56	99.15
Proposed design 1	0.48	4.35	102.31	99.73

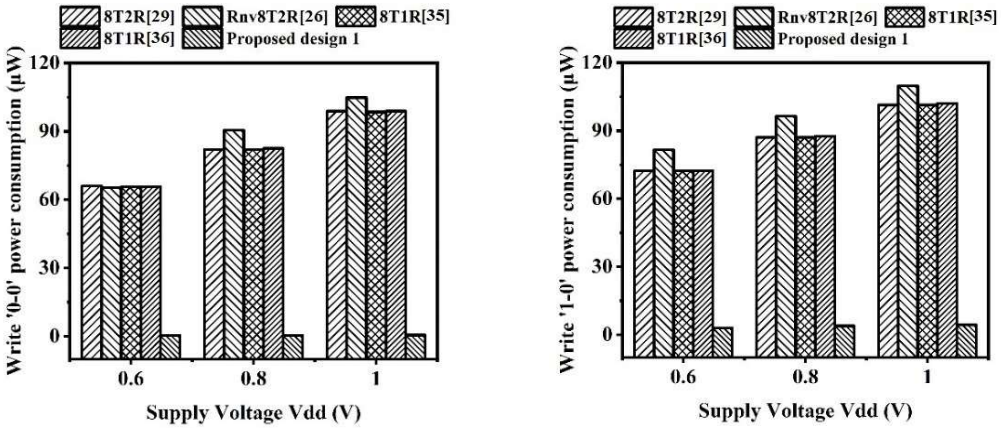
The supply voltage variation study of write performance parameters is also carried out for the sake of completeness. The findings for WM and write delay are depicted in Fig. 2.9,

whereas, the observations for write power consumption are shown in Fig. 2.10. With decrease in supply voltage, it may be noted that WM and write power consumption shows downward trend for all considered nvSRAM cells and Proposed design 1. For the write delay, however, all nvSRAM cells show an increasing trend with lowering supply voltage.

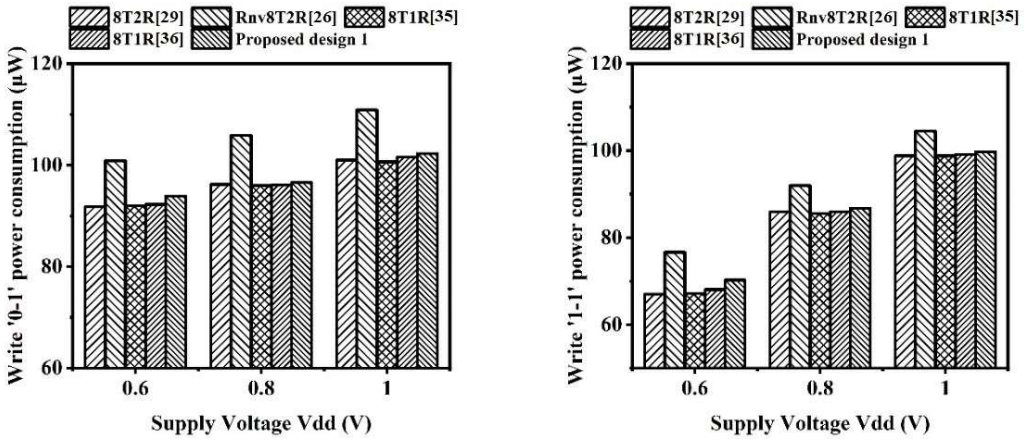


(a) (b)

Fig. 2.9. Write margin and write delay of considered 8T nvSRAM cells and Proposed design 1 at different supply voltage



(a) (b)



(c) (d)

Fig. 2.10. Write power consumption of considered 8T nvSRAM cells and Proposed design 1 with different write patterns (a) 0-0 (b) 1-0 (c) 0-1 and (d) 1-1 at different supply voltage

- Read Performance Analysis

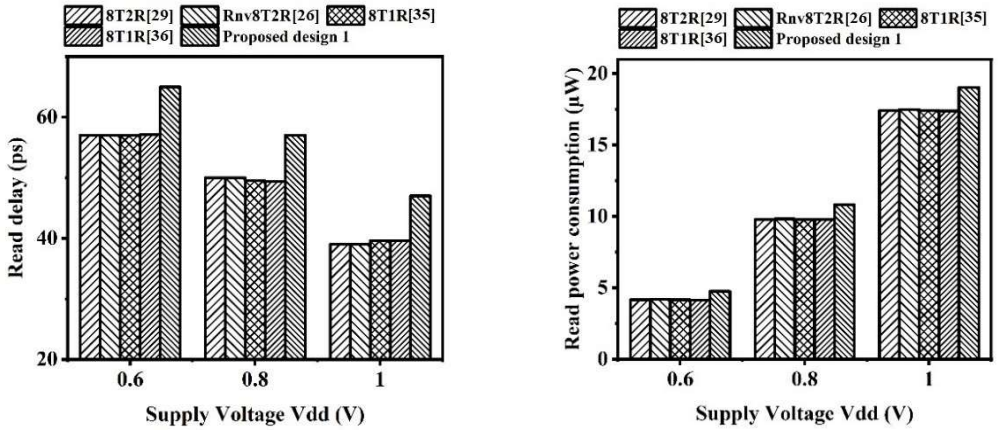
  The read delay and read power consumption are evaluated for Proposed design 1 during read operation. The results are also compared with considered 8T nvSRAM cells.

  Read delay: The read delay of considered 8T nvSRAM cells and Proposed design 1 is analysed at Vdd = 1.0V. The values for read delays are observed as 39ps, 39ps, 39.6ps, 39.6ps and 47ps for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. The Proposed design 1 shows an increment of 17.02% in read delay in comparison to considered nvSRAM cells. This increase in read delay is due to the stack of three transistor formed during the read '1'operation as illustrated in Fig. 2.3(b). The considered 8T nvSRAM cells show comparable read delay values as their read operation is similar.

  Read power consumption: The read power consumption of considered 8T nvSRAM cells and Proposed design 1 is analysed at Vdd = 1.0V. The values are found as

17.38µW, 17.40µW, 17.40 µW, 17.38µW and 19.02µW for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. The Proposed design 1 shows an increment of 8.6% in read power consumption. It is due to the increase in the cell size which leads to longer word line interconnect and using two separate control signals W and R, to activate the Proposed design 1 during read operation. The considered nvSRAM cells shows similar read power consumption due to their similar read operation.

The effect of supply voltage variation is also studied on read delay and read power consumption of considered 8T nvSRAM cells and Proposed design 1 and the results are shown in Fig. 2.11. It is observed that read delay increases, while read power consumption decreases with lowering of supply voltage.



(a) (b)

Fig. 2.11. Read delay and read power consumption of considered 8T nvSRAM cells and Proposed design 1 at different supply voltage

- Hold Performance Analysis

The hold performance of Proposed design 1 is analysed in terms of leakage power consumption. It is compared with considered 8T nvSRAM cells at Vdd = 1.0V and the

results are observed as 25.33µW, 25.89µW, 25.75µW, 25.55µW and 28.95µW for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. It is observed that the Proposed design 1 shows increment of 12.5% in leakage power consumption in comparison to considered 8T nvSRAM cells. This happens as one of the PMOS load transistor in the inverter remains in weak conduction since transistor Mf1 reduces the high logic level voltage by one threshold voltage (V_T) drop. The leakage power consumption can be lowered through the introduction of multiple V_T transistors in the Proposed design 1. A low V_T transistor Mf1 and a high V_T PMOS load can be used for leakage power reduction. To examine the effect of such a change on performance parameters, three design cases are considered: Case-1 with low V_T Mf1, Case-2 with high V_T Mp1/Mp2, Case-3 with low V_T Mf1 and high V_T Mp1/Mp2 and Proposed design 1 with nominal V_T is considered as Case-4. The performance parameters are obtained through simulations for all design cases and are enlisted in Table 2.4. From the three solutions, it can be deduced that use of high V_T Mp1/Mp2 shows significant improvement in leakage power reduction as well as overall performance improvement.

The supply voltage variation study is also carried out for leakage power consumption and the result is shown in Fig. 2.12. It is observed that the leakage power consumption decreases with decrease in supply voltage for all the nvSRAM cells.

- Store Performance Analysis

  Various performance parameters such as delay and power consumption are evaluated for Proposed design 1 during store operation. The results are compared with considered 8T nvSRAM cells.

Table 2.4. Performance parameters of Proposed design 1 for different design cases at Vdd = 1.0V

Performance parameters	Design cases			
	Case - 1	Case - 2	Case - 3	Case - 4
Leakage power (µW)	26.59	24.85	25.66	27.85
Read power (µW)	18.36	14.15	18.45	19.02
Read delay(ps)	62.86	64.59	61.56	65
Write delay(ps)	57.76	58.85	56.58	59
Read Margin(mV)	325	310	305	336
Write Margin(mV)	595	605	582	629
Write Power (0-0) (µW)	0.39	0.45	0.42	0.48
Write Power (0-1) (µW)	99.65	101.95	100.85	102
Write Power (1-0) (µW)	4.25	4.31	4.28	4.35
Write Power (1-1) (µW)	97.56	99.05	98.51	99.73
Store delay(ps)	39.15	40.68	38.65	41
Restore delay(ps)	25.15	25.55	24.56	26
Store power (µW)	22.1	26.4	23.5	29.5
Restore power (µW)	26.5	30.1	27.9	32.6

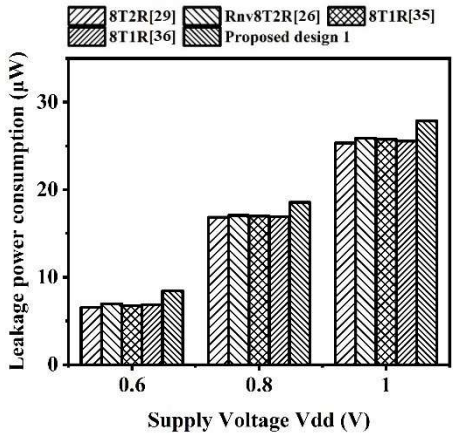
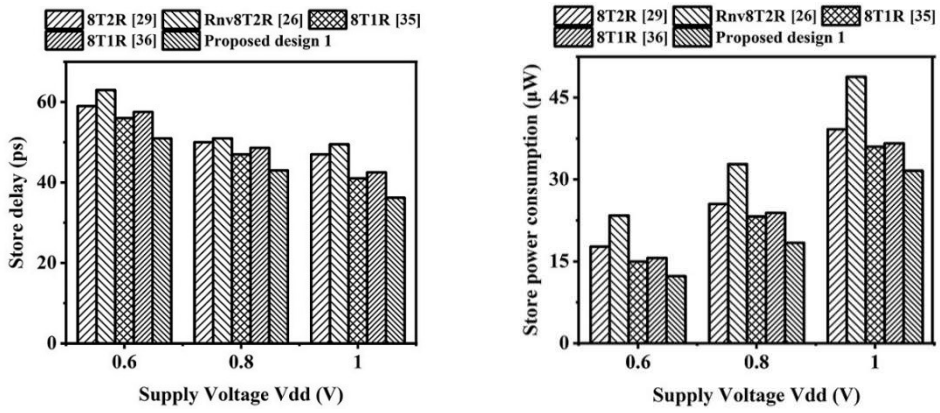


Fig. 2.12. Leakage power consumption of different 8T nvSRAM cells at different supply voltage

Store delay: The store delay for considered 8T nvSRAM cells and Proposed design 1 is observed at Vdd = 1.0V. The results are found to be 47ps, 49.5ps, 41ps, 42.5ps and 36.2ps for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. It is observed that the Proposed design 1 is the fastest among considered nvSRAM cells during store operation. Quantitatively, a maximum reduction of 26.86% is observed in store delay in comparison with considered 8T nvSRAM cells. In the considered 8T nvSRAM cells, the switching of power supply voltage to higher levels or two phases (set/reset) in store operation leads to increase in store delay. Such a switching is not required in the memristor used in the Proposed design 1.

Store power consumption: The store power consumption is observed for considered 8T nvSRAM cells and Proposed design 1 at Vdd = 1.0V. The results are found as 39.2µW, 48.8µW, 36µW, 36.6µW and 31.6µW for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. There is maximum of 35.24% reduction in store power consumption in comparison with the considered 8T nvSRAM cells. The Proposed design 1 avoids the requirement of raising the supply voltage to higher voltage levels as is performed in the considered nvSRAM cells. Thus, the Proposed design 1 exhibits reduced store power consumption than the considered 8T nvSRAM cells.

The supply volatge variation study for store delay and store power consumption is also carried out for the sake of completeness and the results are shown in Fig. 2.13. All considered nvSRAM cells as well as the Proposed design 1 show an increasing trend in store delay with lowering supply voltage, while, the store power consumption shows the downward trend with similar change in supply voltage.



(a) (b)

Fig. 2.13. (a) Store delay and (b) store power consumption of considered 8T nvSRAM cells and Proposed design 1 at different supply voltage

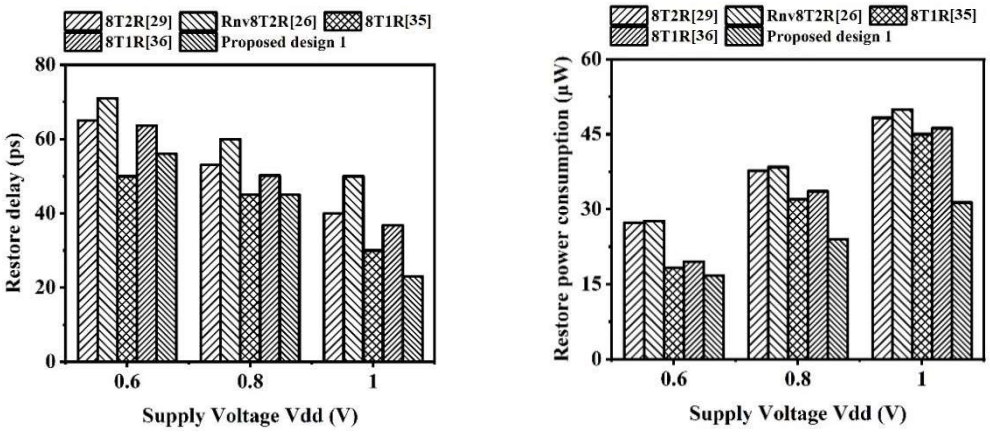
- Restore Performance Analysis

  Various performance parameters such as delay and power consumption are evaluated for Proposed design 1 during restore operation. The results are compared with considered 8T nvSRAM cells.

  Restore delay: The restore delay for considered 8T nvSRAM cells and Proposed design 1 is analysed at Vdd = 1.0. The results are observed as 40ps, 50ps, 30ps, 36.8ps and 23.2ps for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively. It is observed that the Proposed design 1 is the fastest among the considered nvSRAM cells during restore operation. Quantitatively, a maximum reduction of 53.6% is observed in restore delay in comparison with considered 8T nvSRAM cells. In these cells, the recovery of data from memristor to internal nodes takes more time due to change in voltage levels of supply voltage and control signals which leads to increase in restore delay. Such configuration is not required in Proposed design 1.

Restore power consumption: The results for restore power consumption during restore operation are observed as 48.3µW, 49.9µW, 45µW, 46.2µW and 35.3µW for 8T2R cell [29], Rnv8T2R cell [26], 8T1R cell [35], 8T1R cell [36] and Proposed design 1, respectively, at Vdd = 1.0V. There is a maximum reduction of 29.3% in restore power consumption in comparison with the considered 8T nvSRAM cells. The Proposed design 1 avoids the requirement of raising the supply voltage to higher voltage levels as is performed in the considered nvSRAM cells. Thus, the Proposed design 1 exhibit reduced restore power consumption than the considered 8T nvSRAM cells.

The supply voltage variation study is also carried out for restore delay and restore power consumption of considered 8T nvSRAM cells and Proposed design 1 and the results are shown in Fig. 2.14. It is observed that with decrease in supply voltage, restore delay increases while restore power consumption decreases for all the considered nvSRAM cells and Proposed design 1.



(a) (b)

Fig. 2.14. (a) Restore delay and (b) restore power consumption of considered 8T nvSRAM cells and Proposed design 1 at different supply voltage

2.4. Conclusion

In this chapter, the Proposed design 1 (8T1M nonvolatile SRAM cell) with low power consumption is introduced that employs a single TiO_2 memristor as a nonvolatile device. The Proposed design 1 reduces the write power consumption by avoiding discharge of bitlines during write '0' operation. Additionally, the Proposed design 1 avoids use of multiple cell supply voltage levels, two phases in store and restore operations, additional reset phase as well as complex sequencing of control signals in comparison with the considered 8T nvSRAM cells. The design of Proposed design 1 based on condition maintaining same RM is put forward. The functionality of the Proposed design 1 is verified through SPICE simulations using 32nm CMOS PTM model and a performance comparison with the considered 8T nvSRAM cells is carried out at Vdd = 1.0V. The results indicate that the Proposed design 1 reduces the write power consumption by 99.7% during write '0' operation. The store and restore power consumptions are also reduced by 39.95% and 37.27%, respectively, in comparison to considered 8T nvSRAM counterparts. Also, the corresponding improvement of 41.01%, 54.94% and 67.9% is observed in WM, store delay and restore delay, respectively, of Proposed design 1 with respect to the considered 8T nvSRAM cells at same supply voltage. The Proposed design 1 shows 12.53% increased leakage power consumption in comparison to considered 8T nvSRAM cells. Three different design cases are investigated and it is observed that high V_T pull-up transistor are useful for reducing leakage power consumption.

Chapter 3

nvSRAM cell with Improved Read Margin

The contents of this chapter are published in:

[1] D. Singh, K. Gupta, and N. Pandey, **"A novel read decoupled 8T1M nvSRAM cell for near threshold operation,"** *Microelectronics Journal*, vol. 126, pp. 1-16, 2022, doi: 10.1016/j.mejo.2022.105496. **(SCIE indexing, 1.992 IF)**

[2] D. Singh, N. Pandey, and K. Gupta, **"A novel read decoupled 8T1M nvSRAM cell with improved read/write margin,"** *Analog Integrated Circuits and Signal Processing*, vol. 114, no. 1, pp. 89–101, 2023, doi: 10.1007/s10470-022-02121-z. **(SCIE indexing, 1.321 IF)**

3.1. Introduction

In chapter 2, a single ended write 8T nvSRAM cell is introduced to reduce power consumption. This chapter addresses another issue of nvSRAM namely read write conflict that is prevalent specially at lower technology nodes and lower supply voltages. This issue is resolved by introducing read decoupled (RD) port in nvSRAM cell. In this chapter, two eight transistor nvSRAM cells namely Proposed design 2 and Proposed design 3 are presented. Both the nvSRAM cells perform single ended write and read operations, and use RD port formed by two transistors and 1T1M structure to support non-volatile feature. In Proposed design 2, one of the pull-down transistors is grounded gate low threshold voltage (LVT) which helps in maintaining performance near threshold voltages in hold mode. It also improves write ability and, hence, WM. A column shared transistor is used in Proposed design 3 that remain off during write operation only in order to improve WM.

The section 3.2 gives a brief introduction of existing RD nvSRAM cells. It is followed by detailed discussion of Proposed design 2 and its working during write, read, hold, store and restore operations in section 3.3. This section also includes the timing waveform of Proposed design 2 during non-volatile operation. The performance of Proposed design 2 are also analyzed and the results are compared with considered RD nvSRAM cells. Thereafter, in section 3.4. the schematic of Proposed design 3 is discussed and it is followed by detailed explanation of its working during write, read, hold, store and restore operations. The timing waveform during non-volatile operation of Proposed design 3 are also discussed in this section. The results of Proposed design 3 are observed during different operations and the results are compared with considered RD nvSRAM cells and Proposed design 2. The observations are comprehended in summary section 3.5.

3.2. Existing RD nvSRAM cells

From literature, it is found that there are two RD nvSRAM cells [40], [41] wherein memristor is connected between internal node and read bitline RBL through read pass transistor. Although, it provides parallel write and read paths to reduce write and read delay, the direct connection of memristor with internal node causes degradation in write and read margin. It also leads to increase in leakage power consumption. The write operation in RD 8T1R cell [40] is differential, while, in MS 7T1R [41], it is single ended. The read operation in both the cells [40], [41] is performed through read port. Two special function transistors, shared per word, are used to improves write and restore operation.

In the considered RD nvSRAM cells [40], [41], the store operation is performed in set and reset phases. The set phase is performed to change the memristor state to LRS, while, reset phase changes memristor state to HRS. The reset phase requires discharging of bitline RBL that causes increase in store power consumption. The restore operation consists of SR0 and MDR phases. The SR0 phase ensures logic '0' at internal node Q after power down. In MDR phase, the data is recovered according to memristor state. Here, opposite data is recovered after restore operation and, hence, additional inverter is required to obtain original data.

From the above discussion, it is observed that the store and restore operations of existing RD nvSRAM cells [40], [41] are performed in two phases which results in performance degradation. Also, it is required to completely discharge read bitline RBL during store operation that increases store power consumption. Further, the direct connection of memristor to internal node Q causes leakage in the cell that results in degradation in read and WMs. Hence, it is required to introduce nvSRAM cell that avoids complete discharging of RBL line and has simple store and restore operations. Also, the RD port along with the

isolation of memristor from internal nodes of the cell may be incorporated in order to improve read margin/read delay.

3.3. Proposed design 2

The Proposed design 2 is eight transistors with one memristor nvSRAM cell as shown in Fig. 3.1. It supports single ended write and single ended read operation through bitlines WBL and RBL, respectively. It consists of an inverter formed by transistors Mn2 and Mp2 and a pull-up transistor Mp1, which are coupled together to store single bit of data. The pull-down transistor Mn1 is a grounded gate low threshold voltage transistor (LVT) and helps in maintaining Proposed design 2 performance near threshold voltages in hold mode. The access transistors Mn3 is used to perform the write operation which is controlled by write wordline WWL. The series transistors T1 and T2 are used to perform read operation where transistor T1 is controlled by internal node QB while transistor T2 is controlled by read wordline RWL. The 1T1M structure formed by transistor MR1 and memristor M1 is used to perform non-volatile operation. The control signals CTL1 and CTL2 are used for monitoring the non-volatile operation.

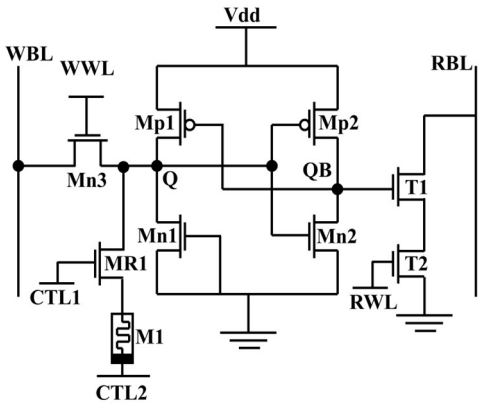


Fig. 3.1. Schematic of Proposed design 2

3.3.1. Operation of Proposed design 2

In this subsection, the operation of Proposed design 2 is described during write, read, hold, store and restore operations. The status of control signals during each operation is summarized in Table 3.1.

Table 3.1. Operating Condition of Proposed design 2

Signals	Operations				
	Write	**Read**	**Hold**	**Store**	**Restore**
WWL	HIGH	LOW	LOW	LOW	LOW
RWL	LOW	HIGH	LOW	LOW	LOW
CTL1	LOW	LOW	LOW	HIGH	HIGH
CTL2	LOW	LOW	LOW	LOW	HIGH

Write operation

The single ended write operation is difficult to perform than differential one. It is due to the fact that in differential write operation either of the internal nodes (Q or QB) discharges quickly through corresponding bitline. The single ended write operation depends on the mutual feedback effect of the inverter pair. The write ability in single ended nvSRAM cells is achieved by modifying the voltage transfer curve (VTC) of each inverter which can be achieved by resizing each transistor. However, it becomes less effective near threshold voltage due to diminished WM and increased susceptibility to noise. During write '1' operation, it becomes difficult to rise internal node Q to Vdd due to pull-down effect of NMOS transistor. Given enough time, the mutual feedback effect of the inverters eventually changes the internal node content. However, this writing process eventually fails for single ended cells at lower voltages.

To overcome this situation, the pull-down effect is eliminated by turning off NMOS transistor Mn1 as shown in Fig. 3.1. However, because of the elimination of the pull-down effect, the hold '0' state turns unstable due to the flow of leakage currents into the internal node Q. To overcome this problem, the WBL is kept low during hold mode and is pulled up only during write operation.

Prior to the write operation, the bitline WBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 3.1. The schematic of Proposed design 2 during write operation is shown in Fig. 3.2. During write '1' operation, bitline WBL remain at Vdd. The internal node Q is charged to Vdd more quickly due to absence of pull-down path. During write '0' operation, bitline WBL is discharged to ground. The internal node Q discharges through transistor Mn3. As internal node Q is connected to inverter (Mn2 - Mp2), it turns off transistor Mn2 and the internal node QB is charged to Vdd through transistor Mp2.

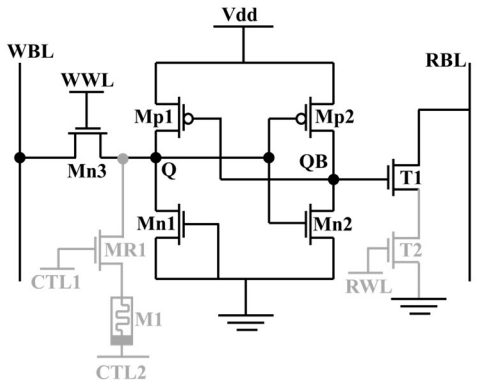


Fig. 3.2. Proposed design 2 during write operation

Read operation

The Proposed design 2 performs single ended read operation. Prior to the read operation, the bitline RBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 3.1. The schematic of Proposed design 2 during read operation is shown in Fig. 3.3. The

transistor T1 is controlled by the data stored at internal node QB, while transistor T2 is controlled by RWL. If logic '1' is stored at internal node Q, the transistor T1 becomes off as internal node QB is at logic '0'and the bitline RBL remains at Vdd. If internal node Q stores logic '0', and QB stores logic '1', the transistor T1 gets on and the read bitline RBL is discharged to ground. At higher supply voltages, the transistors T1 and T2 remain in the strong inversion region so the RBL is discharged sufficiently fast. However, at lower supply voltages, the read current decreases to a great extent leading to read failure. Hence, a read assist technique [57] is used in the Proposed design 2 for successful read operation. A charge pump circuit is used to overdrive the transistor T2 which sets the signal RWL at approximately 2Vdd (RWL ≈ 2Vdd). This increases the driving capability of transistor T2 resulting into faster read operation.

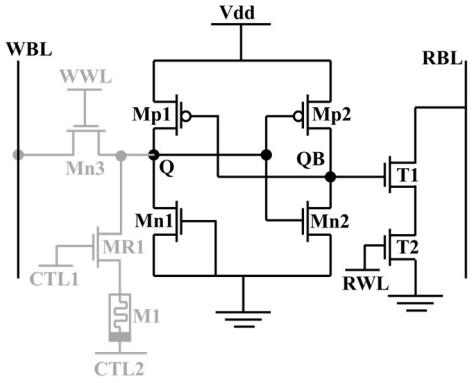


Fig. 3.3. Proposed design 2 during read operation

Hold operation

During hold operation, the control signals are asserted as mentioned in Table 3.1. The schematic of Proposed design 2 in hold mode is shown in Fig. 3.4. The internal node data is hold by coupling between transistor Mp1 and inverter formed by transistor Mp2 and Mn2. The detailed analysis for stability during hold '0' and hold '1' operations is carried out in the results and discussion section.

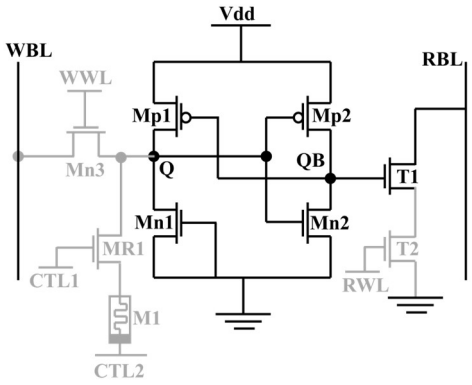


Fig. 3.4. Proposed design 2 during hold operation

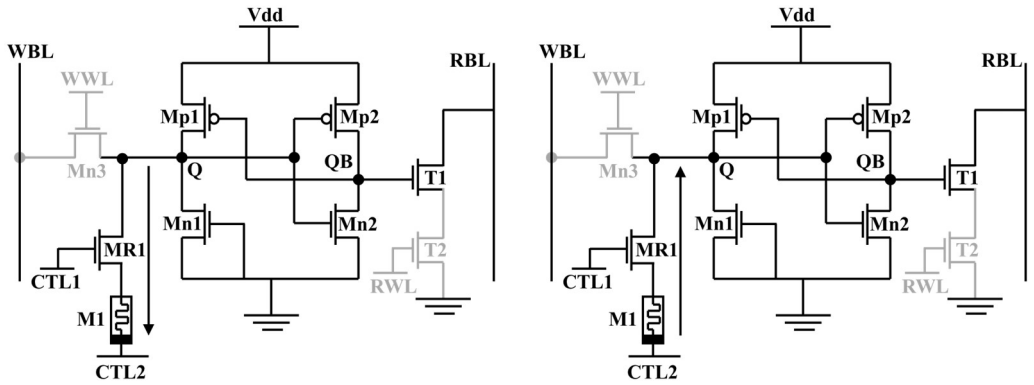
Non-volatile operation

The non-volatile operation of Proposed design 2 is performed after write operation. It consists of store, power down and restore operations. The control signals are asserted as mentioned in Table 3.1. The schematic of Proposed design 2 during store and restore operations is shown in Fig. 3.5. It is pertinent to mention that the initial state of memristor M1 is HRS irrespective of the internal node content.

During store operation, the control signals CTL1 and CTL2 are asserted HIGH and LOW, respectively. If logic '1' is present at internal node Q, a potential difference generates across memristor M1 and it changes its state from HRS to LRS. Alternatively, if logic '0' is present at internal node Q, there is zero potential difference across memristor M1 and it remains in HRS state. It is followed by power down where the supply voltage is turned off and the control signals are asserted LOW. The data present at internal nodes is lost due to absence of power supply whereas memristor retains its state.

After power down, the restore operation takes place by turning on the supply voltage. The control signals CTL1 and CTL2 are asserted HIGH. It turns on transistor MR1. It memristor M1 is in LRS state, a large current flow through it which charges internal node Q to Vdd i.e.,

logic '1'. If memristor is in HRS state, the flow of current through memristor M1 is very low. In this case, the transistor Mp2 would be charging internal node QB faster and turning off transistor Mp1 as driving strength of transistor Mp1 is lower than transistor Mp2, however, transistor Mn1 leaks away the residual charge thus ensuring restore logic '0'. After the recovery of data to internal nodes, memristor changes its state to initial HRS state.



(a) (b)

Fig. 3.5. Proposed design 2 during (a) store and (b) restore operation

3.3.2. Simulation results and discussion

The SPICE simulations are carried out using 32nm PTM model to analyse the performance of Proposed design 2. The memristor model suggested in [55] is used to observe the non-volatile performance. The aspect ratios of different transistors of considered RD nvSRAM cells and Proposed design 2 are enlisted in Table 3.2. In this section, first the timing waveform of Proposed design 2 is discussed at Vdd = 0.6V. It is followed by the performance evaluation during different operations such as write, read, hold, store and restore. The results are also compared with the considered RD nvSRAM cells.

Table 3.2. Aspect ratio of various transistors of considered RD nvSRAM cells and Proposed design 2

Transistor	**Aspect ratio (W/L)**		
	RD 8T1R [40]	**MS 7T1R** [41]	**Proposed design 2**
Mn1	72nm/36nm	54nm/108nm	72nm/36nm
Mn2	72nm/36nm	108nm/36nm	72nm/36nm
Mn3	144nm/36nm	144nm/36nm	162nm/36nm
Mn4	144nm/36nm	-	-
Mp1	72nm/36nm	108nm/36nm	72nm/54nm
Mp2	72nm/36nm	54nm/108nm	54nm/36nm
T1	72nm/36nm	72nm/36nm	72nm/36nm
T2	72nm/36nm	72nm/36nm	72nm/54nm
MR1	-	-	72nm/36nm

Timing waveform

The non-volatile operation is performed in store, power down and restore operations. The time period for each operation is set more than twice of the time period taken by memristor to change its state from HRS to LRS [32]. Fig. 3.6(a) shows the timing waveform for execution of store – power down – restore logic '1'. The following observations are made:

a) First, write '1'operation takes place from 0 to 2ns. The pre-charged bitline WBL remains at Vdd. The control signals WWL is asserted HIGH, while other reman LOW. The internal node Q is updated to logic '1' through the access transistor Mn3 while internal node QB is updated to logic '0'.

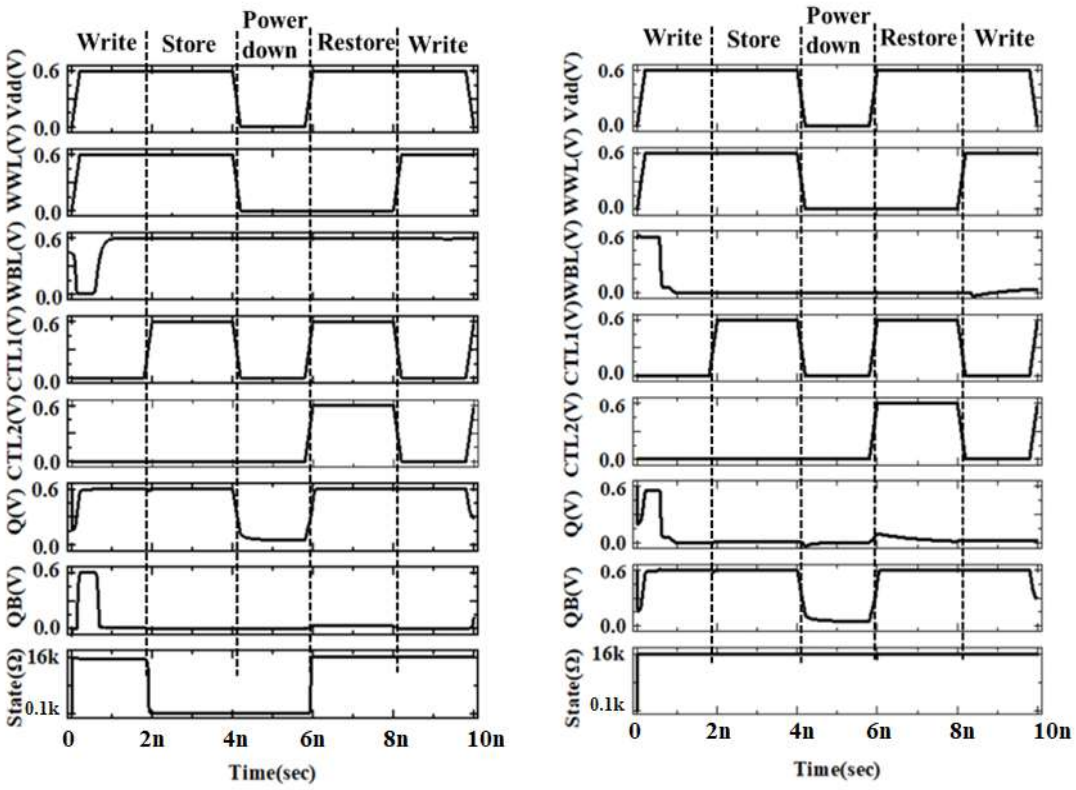
b) The store operation takes place from 2ns to 4ns. During this period, the control signal CTL1 is asserted HIGH, while, other remain LOW. Since, the internal node

Q is at logic '1' while CTL2 is at '0', M1 changes its state from HRS to LRS due to the potential difference across it.

c) The supply voltage is turned off from 4ns to 6ns. The control signals are also asserted LOW. The internal nodes lose their data due to absence of supply voltage, however, memristor M1 retains its LRS state.

d) After power down, the restore operation is performed from 6ns to 8ns. The supply voltage is turned on again. The control signals CTL1 and CTL2 are asserted HIGH while other control signals remain LOW. Due to the LRS state of memristor M1, a large current flow through it and the internal node Q is restored to logic '1'. After restore operation, memristor M1 is be set to the HRS state which is its initial state also.

Similarly, Figure 3.6(b) shows the waveform to execute store – power down – restore logic '0'. To perform the write '0' operation, the bitline WBL is discharge to ground. The signals WWL is asserted HIGH. The internal node Q is updated to logic '0' through the transistor Mn3 while the internal node QB is updated to logic '1'. During the store operation, the signals CTL1 and CTL2 are asserted HIGH and LOW, respectively. Memristor M1 remains in the HRS state as the internal node Q is at logic '0'. During power down, all the control signals are asserted LOW and the supply voltage is turned off. The internal nodes lose their data, while memristor M1 maintains its HRS state. In the restore operation, the power supply is turned on, the control signal CTL1 and CTL2 are asserted HIGH. The internal node Q is restored to logic '0', while the internals node QB is restored to logic '1'. It needs to observed that after successful restore operation, memristor M1 returns to its initial HRS state.



(a) (b)

Fig. 3.6. Timing waveform for non-volatile operation of Proposed design 2 for (a) Logic '1' and (b) Logic '0 operation

Performance analysis

In this sub-section, the performance of Proposed design 2 is compared with the considered RD nvSRAM cells. Various performance parameters such as delay, margin and power consumption are evaluated for write, read, hold, store and restore operations. The effect of variation in supply voltage Vdd is also studied for completeness.

- Write Performance Analysis

  The write performance of the Proposed design 2 is analysed in terms of WM, write delay and write power consumption. The results are compared with the considered RD nvSRAM cells at Vdd = 0.6V.

Write margin (WM): The WM of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2 is observed at Vdd = 0.6V and the results are found as 120mV, 50mV and 190mV, respectively. Thus, the WM of Proposed design 2 shows an improvement of 36.84% and 73.68% in comparison to RD 8T1R cell [40] and MS 7T1R cell [41], respectively.

Write delay: The write delay of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2 is observed at Vdd = 0.6Vand the results are obtained as 53ps, 63.5ps and 65.8ps, respectively. Therefore, the Proposed design 2 shows an increment of 19.45% and 3.49% in comparison to RD 8T1R cell [40] and MS 7T1R cell [41], respectively.

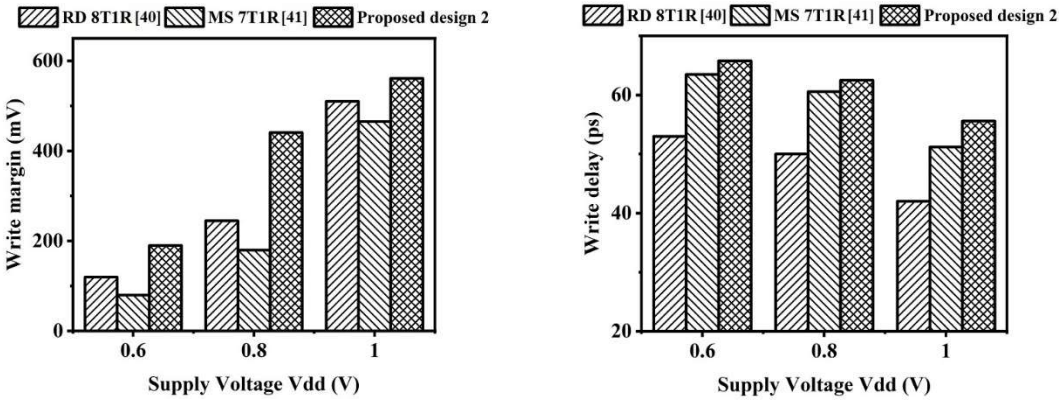
Write power consumption: The write power consumption of Proposed design 2 and considered RD nvSRAM cells [40], [41] is evaluated for different write patterns i.e., 0 – 0, 1 – 0, 0 – 1, and 1 – 1 at Vdd = 0.6V. The observations are summarized in Table 3.3 and the following point are noted:

- The write power consumption for RD 8T1R cell [40] remains almost same for all write patterns whereas MS 7T1R cell [41] and Proposed design 2 show very low write power consumption for 0 – 1 and 1 – 1 write patterns. This is due to differential write operation in RD 8T1R cell [40] against single ended write operation in other two.
- The Proposed design 2 shows 99.7% write power saving in comparison to RD 8T1R cell [40] for write '1' as bitline WBL does not require discharging operation.
- The write pattern 0 – 1 consumes more write power that 1 – 1 write pattern in both MS 7T1R cell [41] and Proposed design 2.

Table 3.3. Write power consumption (µW) of different RD nvSRAM cells and Proposed design 2 at Vdd = 0.6V

RD nvSRAM cells	Write power consumption (µW) for different write patterns			
	0 - 0	**1 – 0**	**0 – 1**	**1 – 1**
RD 8T1R cell [40]	92.45	95.65	93.89	87.95
MS 7T1R cell [41]	91.96	95.15	4.59	0.45
Proposed design 2	91.58	94.58	3.26	0.31

The WM, write delay and write power consumption of Proposed design 2 and considered RD nvSRAM cell are studied at different supply voltages and the results are shown in Fig. 3.7 and Fig. 3.8. It is observed that both the WM and write power consumption increase, while, write delay decreases with increment in supply voltage for Proposed design 2 and considered RD nvSRAM cell.



(a) (b)

Fig. 3.7. (a) WM and (b) Write delay of different RD nvSRAM cells at different supply voltage

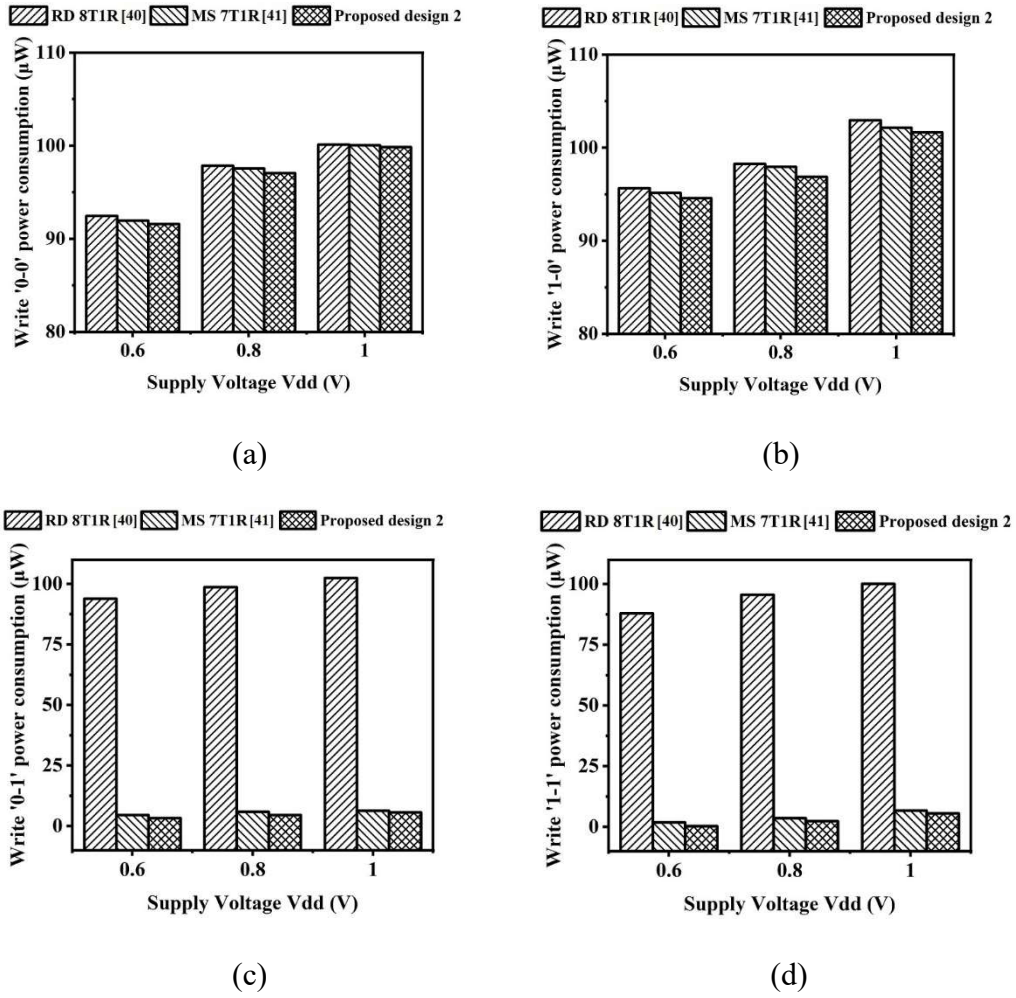


Fig. 3.8. Write power consumption for Proposed design 2 and considered RD nvSRAM cells at different supply voltage for (a) 0-0 (b) 1-0 (c) 0-1 and (d) 1-1 write pattern

- Read Performance Analysis

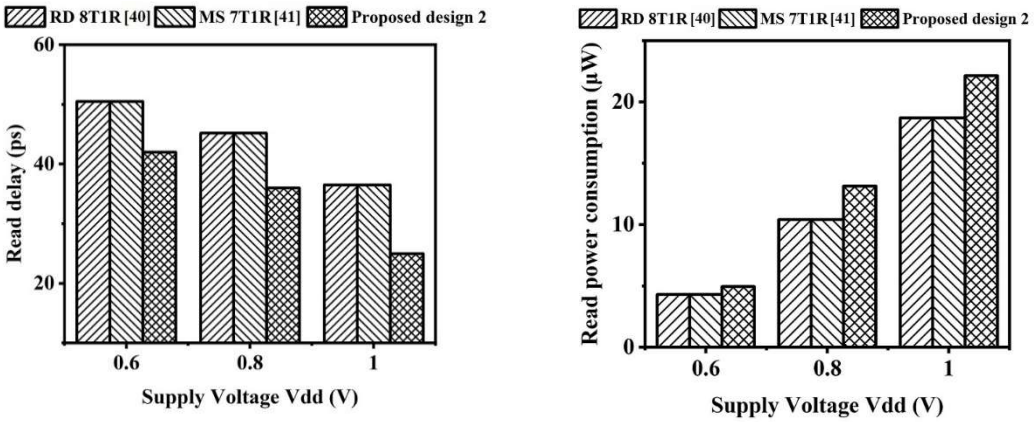
  The read performance of the Proposed design 2 is analysed in terms of read delay and read power consumption. The results are compared with the considered nvSRAM cells at Vdd = 0.6V.

  Read delay: The read delay of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2 is analysed at Vdd = 0.6V and the results are found to be 50.5ps, 50.5ps and 42ps. It is observed that the read delay is minimum for Proposed design 2 and it is

reduced by 16.8% in comparison to considered RD nvSRAM cells. In the Proposed design 2, the read assist circuit is used which boosts the signal RWL approximately equal to 2Vdd. Hence, the read operation is fast in Proposed design 2 in comparison to the considered RD nvSRAM cell [40], [41].

Read power consumption: The read power consumption of RD 8T1R [40], MS 7T1R [41] nvSRAM cell and Proposed design 2 is measured at Vdd = 0.6V and the corresponding values are found as 4.31µW, 4.31µW and 4.95µW, respectively. In proposed deign 2, there is a large flow of read current through read port which increases the read power consumption by 12.92% in comparison to considered RD nvSRAM cell [40], [41].

The supply voltage variation study is also carried out for read delay and read power consumption of Proposed design 2 and considered RD nvSRAM cells. The results are shown in Fig. 3.9. It is observed that read delay is decreased, while, read power consumption is increased with increase in supply voltage.

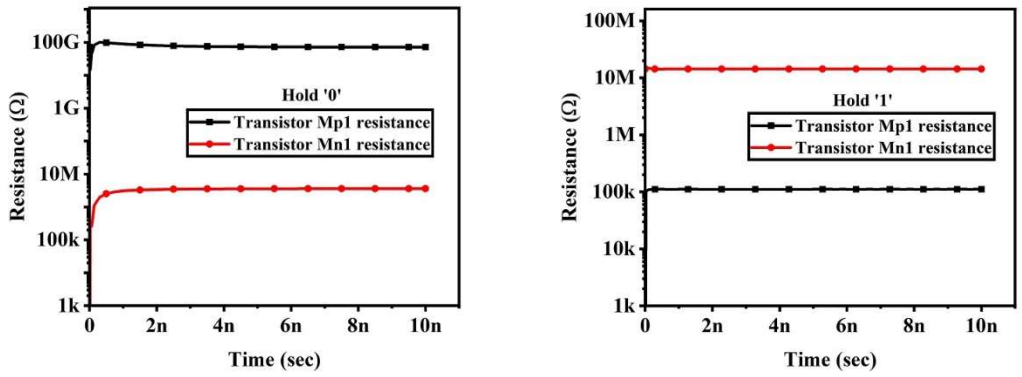


(a) (b)

Fig. 3.9. (a) Read delay and (b) read power consumption of considered RD nvSRAM cells and Proposed design 2 at different supply voltage

- Hold Performance Analysis

It is pertinent to mention here that low threshold voltage transistor (LVT) usually brings higher leakage current. To analyse the impact of LVT, the operation of the Proposed design 2 is examined in hold mode. The hold '0' state is vulnerable due to leakages from access transistor which is handled by using longer transistor Mp1 and LVT Mn1 as it increases the resistance of transistors Mp1 and lowers resistance of transistor Mn1. The plot of resistance of transistors Mp1 and Mn1 for hold '0' state is shown in Fig. 3.10(a). It is observed that resistance of transistor Mp1 is approximately 1000 times higher than resistance of transistor Mn1 ensuring the voltage at internal node Q to retain at logic '0'. Alternatively, in hold '1' state the leakage through transistor Mn1 may cause decrease in internal node voltage. The resistance of transistors Mp1 and Mn1 for hold '1' state is plotted in Fig. 3.10(b) which clearly shows that the resistance of transistor Mp1 is approximately 1000 times less than resistance of transistor Mn1 thus the state in maintained.



(a) (b)

Fig. 3.10. Resistance of transistor Mn1 and Mp1 during (a) hold '0' and (b) hold '1' operation

The hold performance of Proposed design 2 and considered RD nvSRAM cells is analysed in terms of leakage power consumption at Vdd =0.6V. The results are found as 423nw, 423nW and 390nw for RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. Thus, the Proposed design 2 shows minimum leakage power consumption with respect to considered RD nvSRAM cells. This is due to the fact that considered RD nvSRAM cells use memristor connected directly to internal node which causes leakage current. Also, the supply voltage variation study is carried out for leakage power consumption and the result is shown in Fig. 3.11. An increasing trend in leakage power consumption is observed with increase in supply voltage.

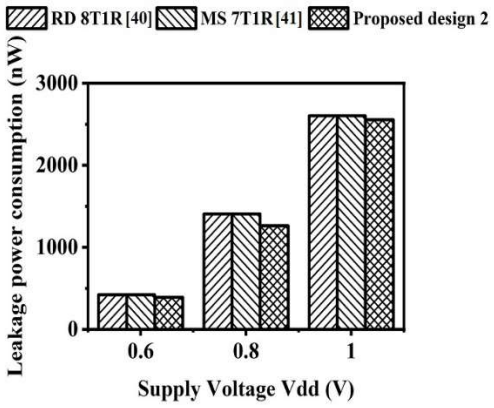


Fig. 3.11. Leakage power consumption of different RD nvSRAM cells at different supply voltage

- Store Performance Analysis

The store performance of Proposed design 2 is analysed in terms of store delay and store power consumption. The results are compared with the considered RD nvSRAM cells at Vdd = 0.6V.

Store delay: The store delay for Proposed design 2 and considered RD nvSRAM cells is analysed at Vdd=0.6V. The results are obtained as 53.55ps, 53.55ps and 47.95ps for

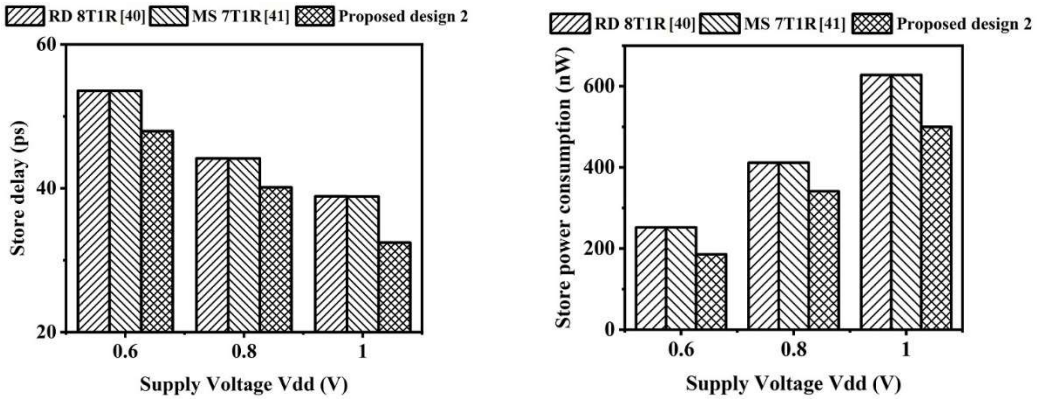
RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. It is observed that the Proposed design 2 is the fastest among the considered RD nvSRAM cells in performing store operation. The improvement in store delay is 16.56% in comparison to the considered RD nvSRAM cell. It is due to the presence of 1T1M structure formed by transistor MR1 and memristor M1 which perform simple store operation unlike the considered RD nvSRAM cells. In the considered RD nvSRAM cell, the store operation requires set/reset phases on the memristor for storing data.

Store power consumption: The store power consumption for Proposed design 2 and considered RD nvSRAM cell is analysed at Vdd = 0.6V. The results are obtained as 252nW, 252nW and 186nW for RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. It is evident that the Proposed design 2 achieves significant reduction in store power consumption. It is reduced by 27.63% in comparison to considered RD nvSRAM cells. The Proposed design 2 does not need high voltage level during store operation which is required in the considered RD nvSRAM cells and results in more store power consumption.

The supply voltage variation study is also carried for store performance analysis of Proposed design 2 and considered RD nvSRAM cells. The results are shown in Fig. 3.12. The decreasing trend in store delay, while increasing trend in store power consumption is observed with increase in supply voltage.

- Restore Performance Analysis

  The restore performance of Proposed design 2 is analysed in terms of restore delay and restore power consumption. The results are compared with the considered RD nvSRAM cells at Vdd= 0.6V.



(a) (b)

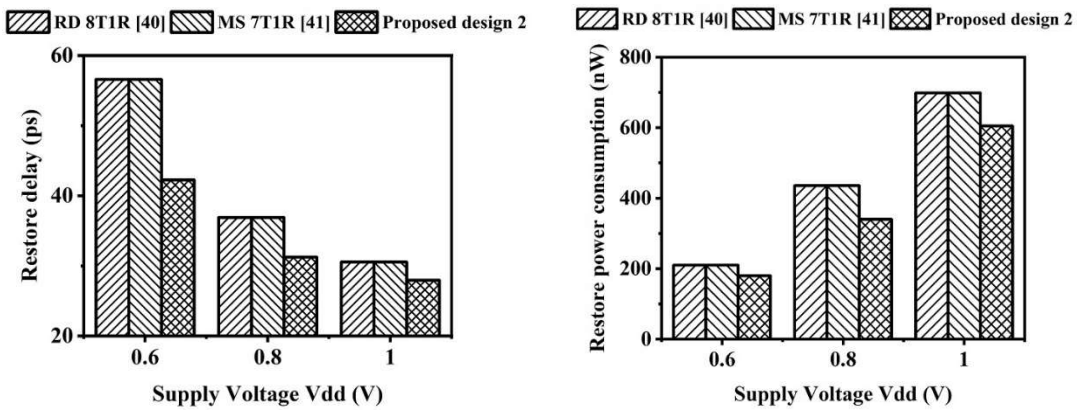
Fig. 3.12. (a) Store delay and (b) store power consumption of different RD nvSRAM cells at different supply voltage

Restore delay: The restore delay for Proposed design 2 and considered RD nvSRAM cells is analysed at Vdd = 0.6V. The results are found to be 56.59ps, 56.59ps and 42.26ps for RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. It is observed that the Proposed design is the fastest among the considered RD nvSRAM cells in performing restore operation. The improvement in restore delay is 25.33% in comparison to considered RD nvSRAM cells. It is due to the presence of 1T1M structure formed by transistor MR1 and memristor M1 which perform simple restore operation unlike the considered RD nvSRAM cells that requires SR0 and MDR phases to recover the data from memristor.

Restore power consumption: The restore power consumption of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2 are found to be 210nW, 210nW and 180nW, respectively, at Vdd = 0.6V. It is evident that the Proposed design 2 achieves significant reduction in restore power consumption. It is reduced by 16.24% for Proposed design 2 in comparison to considered RD nvSRAM cells. The Proposed design 2 does not

need high voltage level during restore operation which is required in the considered RD nvSRAM cells resulting more restore power consumption.

The supply voltage variation study for restore performance analysis of Proposed design 2 and considered RD nvSRAM cell is also carried out and the results are shown in Fig. 3.13. It is observed that restore delay decreases, while restore power consumption increases with increase in supply voltage.



(a) (b)

Fig. 3.13. (a) Restore delay and (b) restore power consumption of different RD nvSRAM cells at different supply voltage

3.4. Proposed design 3

This section presents Proposed design 3 that uses RD port similar to Proposed design 2. The schematic of Proposed design 3 is shown in Fig. 3.14. It consists of two back-to-back connected inverters formed by transistors Mn1-Mp1 and Mn2-Mp2. The bitlines WBL and RBL are used to perform write and read operations, respectively. The transistor ST, controlled by control signal CTL is a shared per column transistor. It remains off during write and restore operations. The pass transistor Mn3 is used to perform write operation at internal

node Q and it is controlled by write wordline WWL. The transistors T1 and T2 form a read port and are controlled by internal node QB and read wordline RWL, respectively. The 1T1M structure formed by transistor MR1 and memristor M1 is used to perform non-volatile operation. The control signals CTL1 and CTL2 are used for monitoring the non-volatile operation.

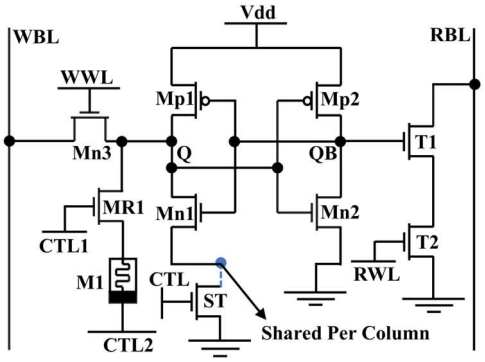


Fig. 3.14. Schematic of Proposed design 3

3.4.1. Operation of Proposed design 3

In this subsection, the write, read, hold, store and restore operations are elucidated. The status of control signals during each operation is enlisted in Table 3.4.

Table 3.4. Operating Condition of Proposed design 3

Signals	**Operations**				
	Write	**Read**	**Hold**	**Store**	**Restore**
WWL	HIGH	LOW	LOW	LOW	LOW
RWL	LOW	HIGH	LOW	LOW	LOW
CTL	LOW	HIGH	HIGH	HIGH	LOW
CTL1	LOW	LOW	LOW	HIGH	HIGH
CTL2	LOW	LOW	LOW	LOW	HIGH

Write operation

Prior to write operation, the bitline WBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 3.4. The resulting schematic of Proposed design 3 during write operation is presented in Fig. 3.15. As column shared transistor (ST) is off during write operation, the pull-down strength of inverter Mn1-Mp1 is low. For write '1' operation, the WBL remains at Vdd. The potential of internal node Q is increased to Vdd due to the write current flow from WBL to internal node Q through transistor Mn3. The increased potential of internal node Q turns on transistor Mn2 and cause voltage of internal node QB to decrease. This increases current through transistor Mp1 and results into faster charging of internal node Q to logic '1' and internal node QB discharged to logic '0'. Similarly, during write '0' operation, the bitline WBL is discharged to ground. The internal node Q is flipped to logic '0' through transistor Mn3.When internal node Q is discharged to ground, the transistor Mp2 is turned on and transistor Mn2 is turned off. It raises the potential of internal node QB to logic '1' and causes transistor Mp1 to cut off. Thus, the ST transistor improves the write ability and, hence, the WM of Proposed design 3.

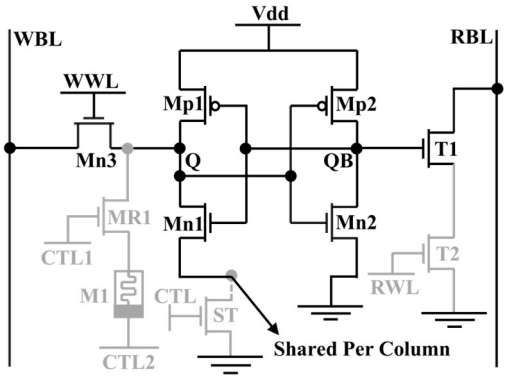


Fig. 3.15. Proposed design 3 during write operation

Read operation

The Proposed design 3 performs single ended read operation. Prior to the read operation, the bitline RBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 3.4. The resulting schematic of Proposed design 3 during read operation is shown in Fig. 3.16. As the internal nodes Q and QB are at logic '0' and logic '1', respectively, the transistor T1 is turned on. With the assertion of signal RWL, the read current path is formed through transistor T1 to transistor T2 to ground. It discharges the bitline RBL performing read '0' operation. For read '1' operation, internal node Q is at logic '1', the internal node QB is at logic '0'. The transistor T1 turns off and the bitline RBL remains at Vdd. Since, the charging/discharging of bitline RBL does not affect the internal nodes Q and QB and, also, memristor is isolated from internal nodes which occurs in considered RD nvSRAM cells, the RM of Proposed design 3 is improved.

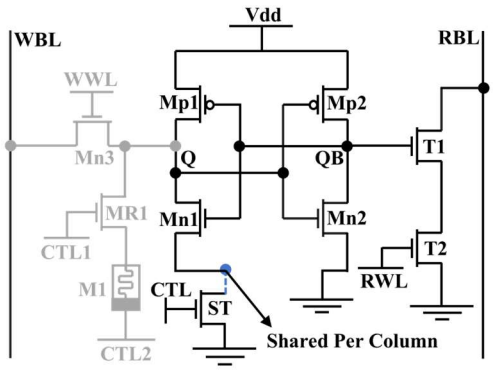


Fig. 3.16. Proposed design 3 during read operation

Hold operation

During hold operation, the control signals are asserted as mentioned in Table 3.4. The resulting schematic of Proposed design 3 during hold operation is shown in Fig. 3.17. The back-to-back connected inverter pair stores the data during hold mode.

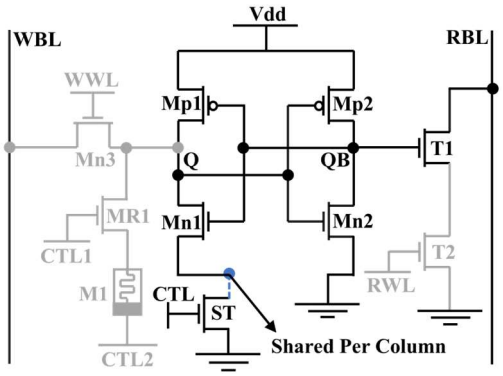


Fig. 3.17. Proposed design 3 during hold operation

Non-volatile operation

The non-volatile operation in Proposed design 3 consists of store, power down and restore operations. The control signals are asserted as mentioned in Table 3.4. The schematic of Proposed design 3 during store and restore operations is shown in Fig. 3.18. Prior to store operation, the write operation takes place. It is also required to mention that memristor M1 remain in its initial HRS state irrespective of internal node data.

In store operation, the control signals (CTL and CTL1) and CTL2 are asserted HIGH and LOW, respectively. Memristor M1 changes its state from HRS to LRS if internal node Q stores logic '1'. It is due to the potential difference developed across it. If the internal node Q is at logic '0', the memristor M1 does not change its state due to zero potential difference across it and remains in HRS state. During power down, the supply voltage Vdd is turned off and all the control signals are asserted LOW. It this phase, the internal nodes Q and QB lose their data, while the memristor M1 maintains its state.

During restore operation, the supply voltage is turned on again. The control signals CTL1 and CTL2 are asserted HIGH. If memristor M1 is in LRS state, there is a large flow of current through transistor MR1 and the internal node Q is charged to Vdd i.e., restored to logic '1'.

After restore operation, memristor M1 changes its state to HRS. If memristor M1 is in HRS state, the internal node Q is not be able to rise to Vdd and logic '0' is restored at the internal node Q. After restoring the data, the memristor M1 continues to remain at HRS, which is its initial state also.

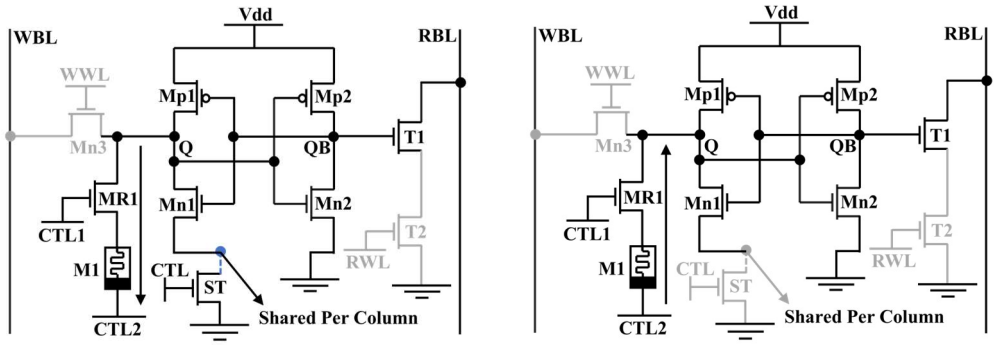


Fig. 3.18. Proposed design 3 during (a) store and (b) restore operation

3.4.2. Simulation results and discussion

The SPICE simulations for the functional verification of Proposed design 3 are performed using 32nm PTM model. The memristor model suggested in [55] is used to observe the non-volatile performance. In this section, first the timing waveform of Proposed design 3 is discussed at Vdd =1.0V. It is followed by the performance evaluation during different operations such as write, read, hold, store and restore and the results are compared with RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2. The aspect ratio of all transistors of Proposed design 3 and considered nvSRAM cell is kept same i.e., (W/L) = (72nm/36nm).

Timing waveform

The timing waveform for Proposed design 3 executing store, power down and restore operations is shown in Fig. 3.19. The time period of each phase is taken as 2ns which is more

than two times of the time required to change the state of memristor [56]. The following observations are made for non-volatile operation for logic '1' through Fig. 3.19(a).

a) Prior to store operation, the write operation takes place from 0 to 2ns. The pre-charged WBL remain at Vdd. The control signal WWL is asserted HIGH while the other signals are asserted LOW. The internal node Q changes its data to logic '1' through pass transistor Mn3.

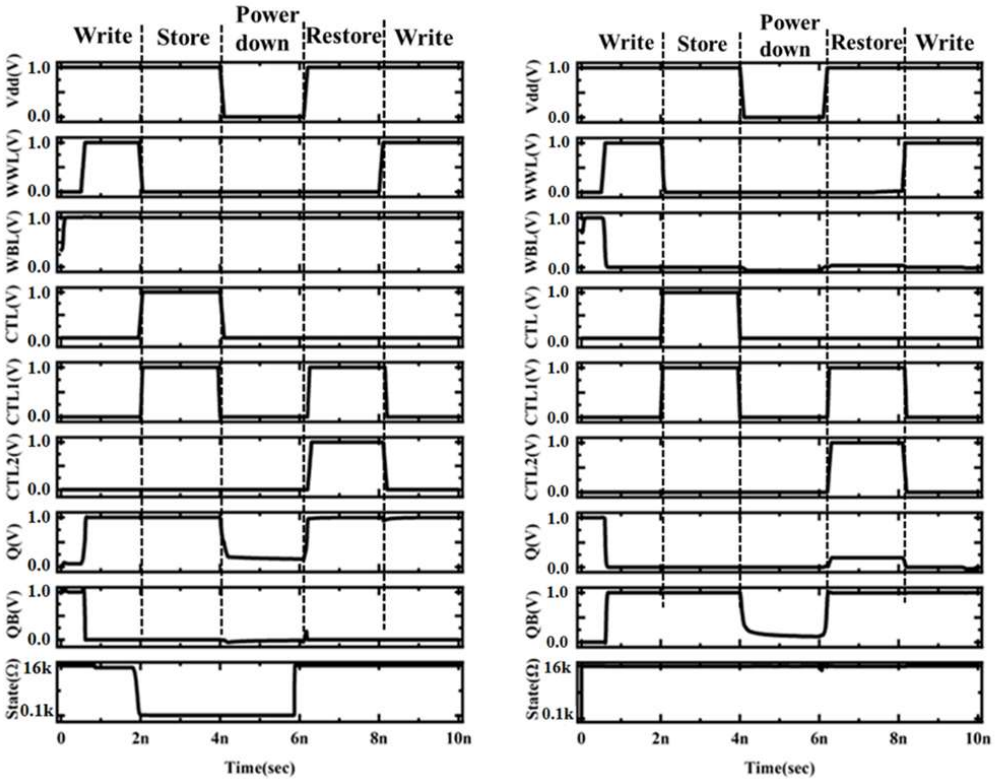
b) The store operation is performed from 2ns to 4ns. In this operation, the control signals CTL, CTL1 are asserted HIGH while the other signals are asserted LOW. As the data at internal node Q is logic '1', a potential difference is developed across memristor M1 and it changes its state from HRS to LRS.

c) The power down takes place from 4ns to 6ns. The supply voltage is turned off and all the control signals are asserted LOW. The data at internal nodes Q and QB is lost due to power down while memristor M1 maintains its LRS state.

d) After power down, the restore operation is performed from 6ns to 8ns. In restore operation, the power supply is turned on again and the control signals CTL1 and CTL2 are asserted HIGH while other signals remain LOW. Due to the LRS state of memristor M1, a large current flow through it and the internal node Q is charged to Vdd indicating recovery of logic '1'. After restore operation, memristor M1 changes it state to HRS which is its initial state also.

Similarly, Fig. 3.19(b) shows the non-volatile operation for logic '0'. First, the write '0' operation takes place. The pre-charged bitline WBL is discharged to ground and due to this, the internal node Q data is changed to logic '0' through transistor Mn3. In store operation, as internal node Q is at logic '0', the memristor M1 remains in HRS state due to zero potential difference across it. During power down, the supply voltage is turned off and the control

signals are asserted LOW. The internal nodes Q and QB lose their data, however, memristor M1 maintains its HRS state. In restore operation, the supply voltage is turned on again and the control signals CTL1 and CTL2 are asserted HIGH. Due to HRS state of memristor M1, a low current flow through it which is not enough to charge internal node Q so it remains at logic '0'. After recovery of data, memristor M1 continues to remain in its initial state i.e., HRS.



(a) (b)

Fig. 3.19. Timing waveform for non-volatile operation of Proposed design 3 for (a) Logic '1' and (b) Logic '0 operation

Performance analysis

In this sub-section, the performance of Proposed design 3 is compared with the considered RD nvSRAM cells [40], [41] and Proposed design 2. Various performance parameters such

as delay, margin and power consumption are evaluated for write, read, hold, store and restore operations. The effect of variation in supply voltage Vdd is also studied for completeness.

- Write Performance Analysis

  The write performance of the Proposed design 3 is analysed in terms of WM, write delay and write power consumption. The results are compared with the considered RD nvSRAM cells [40], [41] and Proposed design 2 at Vdd = 1.0V.

  Write margin (WM): The WMs of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 510mV, 485mV, 580mV and 650mV, respectively, at Vdd = 1.0V. It is observed that the WM of Proposed design 3 is increased by 27.45%, 34.02% and 25.38% in comparison to RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively.

  Write delay: The write delay of Proposed design 3 and considered RD nvSRAM cells is analysed at Vdd = 1.0V. The results are found to be 32.76ps, 54.98ps, 51.26ps and 47.43ps for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3, respectively. It is observed that the write delay of Proposed design 3 is increased by 44.78% in comparison to RD 8T1R cell [40] and decreased by 13.73% and 7.47% in comparison to MS 7T1R cell [41] and Proposed design 2, respectively.

  Write power consumption: The write power consumption of considered RD nvSRAM cells, Proposed design 2 and Proposed design 3 is analysed at Vdd=1.0V. The corresponding values are found to be 96.52µW, 1.85µW, 1.98µW and 2.35µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3, respectively. It is observed that the write power consumption (during write '1') of Proposed design 3 is decreased by 98.08% and increased by 21.28% and 15.74% in

comparison to RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively.

The supply voltage variation study is also carried out for write performance of Proposed design 3 and considered RD nvSRAM cells and the results are shown in Fig. 3.20. It is observed that decreases in supply voltage decreases WM and write power consumption. However, the increasing trend for write delay is observed with reduction in supply voltage for all the RD nvSRAM cells.

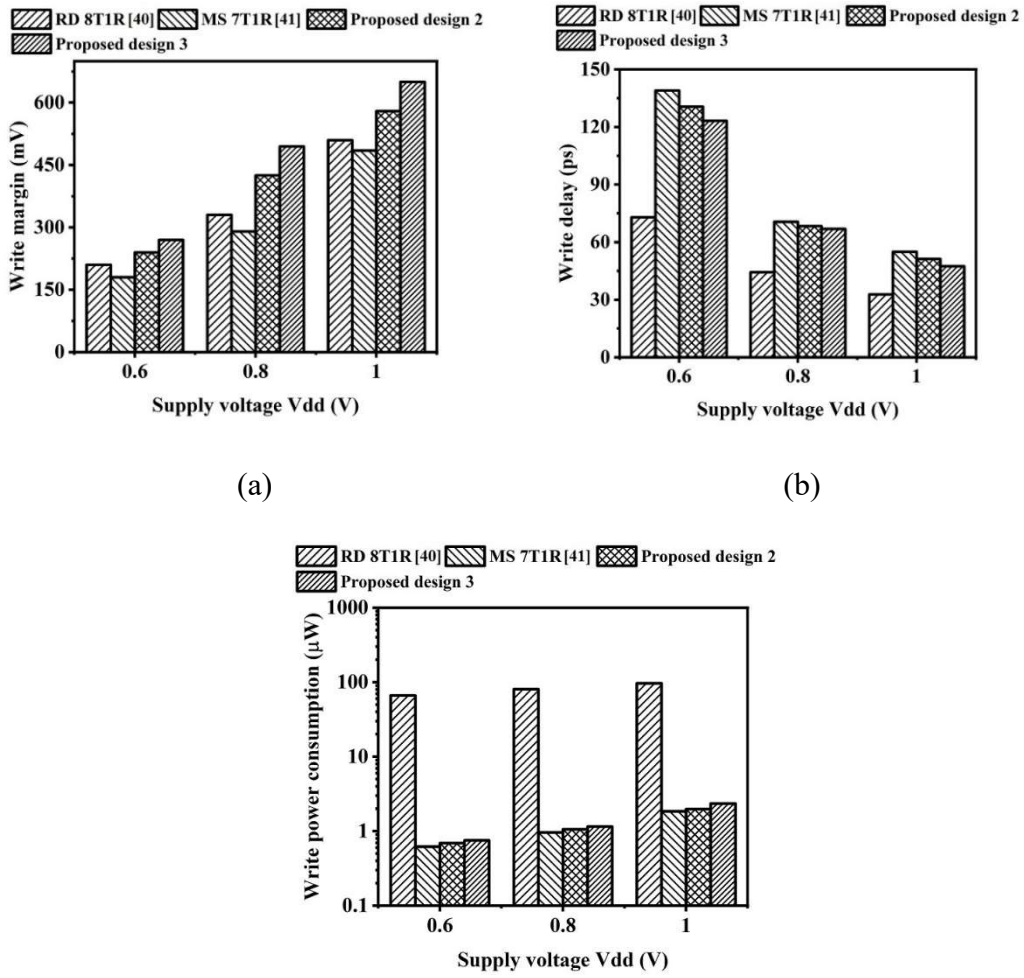


Fig. 3.20. (a) Write margin (b) write delay and (c) write power consumption of considered RD nvSRAM cells and Proposed design 3 at different supply voltage

- Read Performance Analysis

The read performance of the Proposed design 3 is analysed in terms of RM, read delay and read power consumption. The results are compared with the considered RD nvSRAM cells [40], [41] and Proposed design 2 at Vdd = 1.0V.

Read margin (RM): The RMs of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 295mV, 295mV, 255mV and 370mV, respectively, for Vdd = 1.0V. It is observed that the RM of Proposed design 3 is 19.56%, 19.56% and 25.42% better than that of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. For RD 8T1R cell [40] and MS 7T1R cell [41], the direct connection of memristor to internal node of the cell affects the internal node potential which affects RM of the cell. However, in Proposed design 3, the transistor MR1 avoids the directs connection of memristor to internal node resulting improvement in RM.

Read delay: The read delay of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are observed as 36.52ps, 36.11ps, 27.95ps and 27.29ps, respectively, at Vdd = 1.0V. It is pertinent to mention here that Proposed design 3 uses the same read port as Proposed design 2. Therefore, both designs have same read delay performance. An improvement of 25.28% is observed in read delay of Proposed design 3 in comparison to RD 8T1R cell [40], MS 7T1R cell [41]. It is due to the high read current flowing through read port of Proposed design 2 and 3 during discharging of read bitline RBL.

Read power consumption: The read power consumption of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 16.85µW,

16.85µW, 20.62µW and 20.56µW, respectively, at Vdd = 1.0V. It is observed that the read power consumption of Proposed design 3 is increased by 22.01% in comparison to RD 8T1R cell [40], MS 7T1R cell [41]. It is due to the high read current flowing through read port of Proposed design 3. The read power consumption of Proposed design 2 is similar to Proposed design 3.

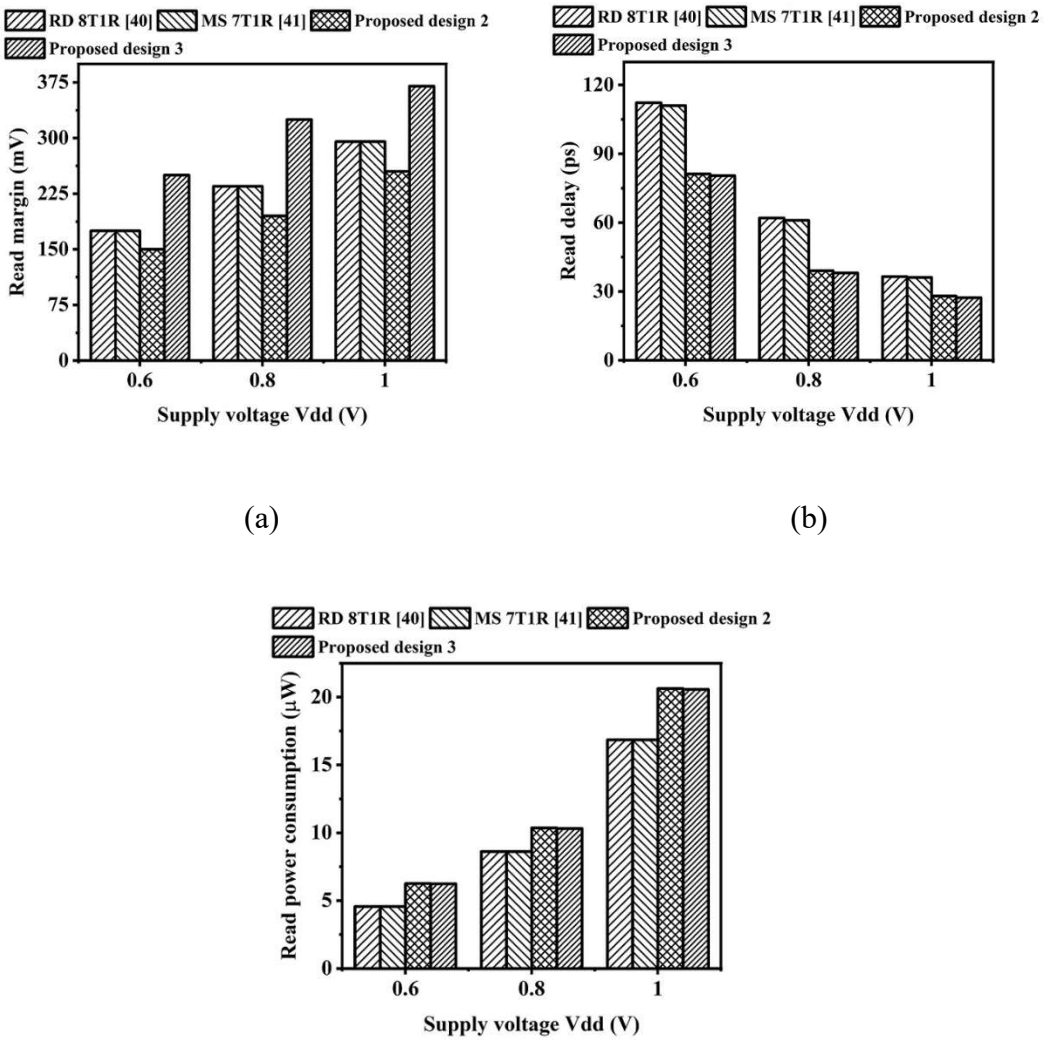


Fig. 3.21. (a) Read margin (b) read delay and (c) read power consumption of considered RD nvSRAM cells and Proposed design 3 at different supply voltage

The supply voltage variation study is also carried out to analyse read performance of Proposed design 3 and considered RD nvSRAM cells and the results are shown in Fig. 3.21. With decrease in supply voltage, all considered RD nvSRAM cells show a downward trend in RM and read power consumption, whereas read delay shows an upward trend.

- Hold Performance Analysis

  The hold performance of Proposed design 3 is analysed in terms of leakage power consumption and the results are compared with considered RD nvSRAM cells at Vdd = 1.0V. The corresponding values are obtained as 15.71µW, 10.94µW, 20.18µW and 8.73µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3, respectively. It is observed that the Proposed design 3 shows minimum leakage power consumption and it is reduced by 44.41%, 20.18% and 56.75% in comparison to RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 2, respectively. In RD 8T1R cell [40] and MS 7T1R cell [41], the direct connection of memristor to internal node Q exists which introduces a leakage path through memristor (for Q = '0' and QB = '1') and causes higher leakage in the cell. Such path is not present

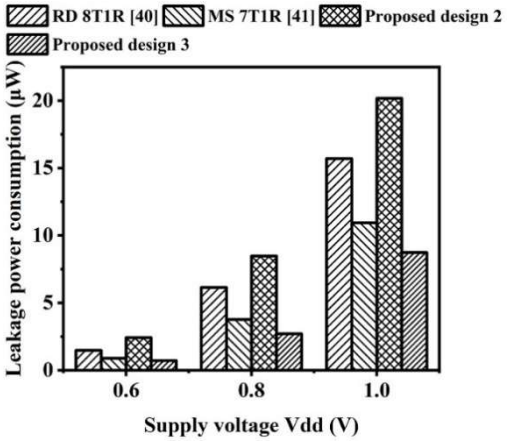


Fig. 3.22. Leakage power consumption of different RD nvSRAM cells at different supply voltage

in the Proposed design 2 and 3. Further, one of the pull-down transistors Mn1 remains off in Proposed design 2 and it is LVT also, which is a cause of increased leakage power consumption. The supply voltage variation study is also carried out for leakage power consumption analysis and the result is shown in Fig. 3.22. It is observed that the decrease in supply voltage decreases the leakage power consumption.

- Store Performance Analysis

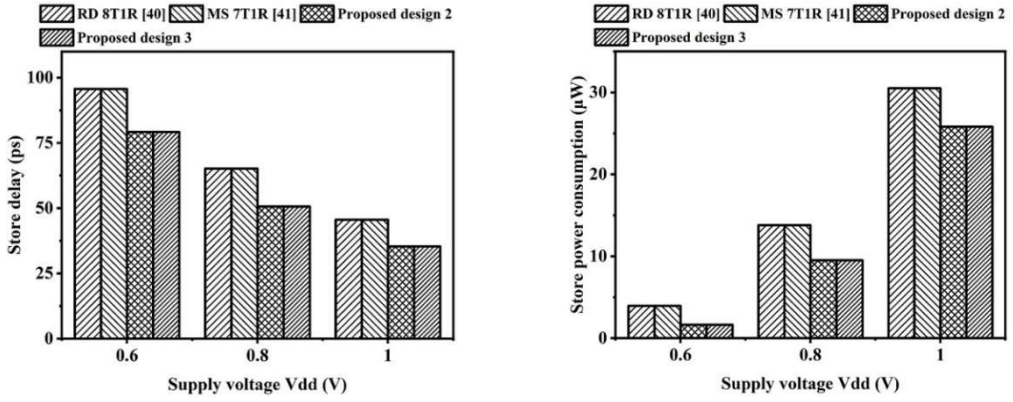
The store performance of Proposed design 3 is analysed in terms of store delay and store power consumption. The results are compared with the considered RD nvSRAM cells [40], [41] and Proposed design 2 at Vdd = 1.0V.

Store delay: The store delays of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 30.56ps, 30.56ps, 25.33ps and 25.33ps, respectively, Vdd = 1.0V. It is observed that the store delay of Proposed design 3 is similar to Proposed design 2 due to similar store operation. It is reduced by 17.11% in comparison to RD 8T1R cell [40], MS 7T1R cell [41]. In these cells [40], [41], the store operation requires two phases, namely set and reset, while, the Proposed design 2 and 3 do not require such complex operations to store data into memristor.

Store power consumption: The store power consumption of considered RD nvSRAM cells and Proposed design 3 are evaluated at Vdd=1.0V. The corresponding values are found to be 30.5µW, 30.5µW, 25.8µW and 25.8µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3, respectively. It is observed that the store power consumption of Proposed design 3 is similar to Proposed design 2, while it is reduced by 22.66% in comparison to RD 8T1R cell [40], MS 7T1R cell [41]. The increased store power consumption in RD 8T1R cell [40] and MS 7T1R cell [41] is due to the fact that the read bitline needs to be discharged to change memristor state.

The store process is simpler in Proposed design 2 and Proposed design 3 which explains reduced store power consumption.

The store performance for Proposed design 3 and considered RD nvSRAM cells is also studied at different supply voltages also and the results are shown in Fig. 3.23. With increase in supply voltage, the store delay decreases whereas store power consumption shows upward trend.



(a) (b)

Fig. 3.23. (a) Store delay and (b) store power consumption of different RD nvSRAM cells and Proposed design 3 at different supply voltage

- Restore Performance Analysis

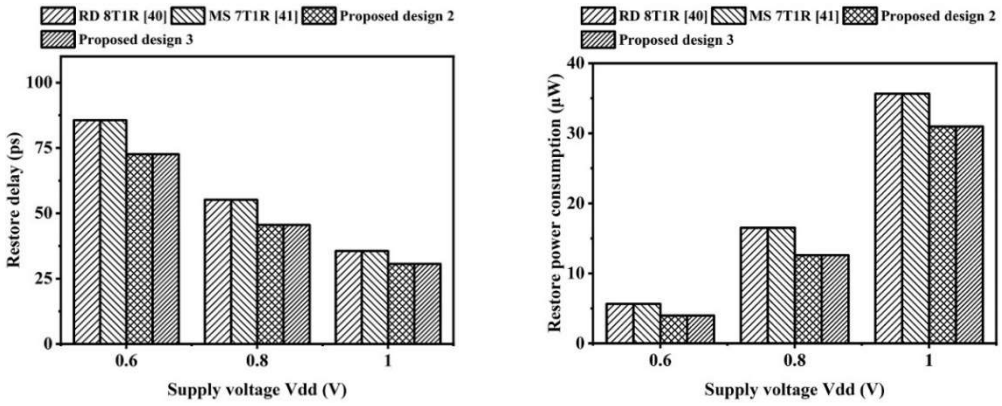
The restore performance of Proposed design 3 is analysed in terms of restore delay and restore power consumption. The results are compared with the considered RD nvSRAM cells [40], [41] and Proposed design 2 at Vdd = 1.0V.

Restore delay: The restore delays for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 26.15ps, 26.15ps, 20.63ps and 20.63ps, respectively, at Vdd= 1.0V. It is observed that the restore delay of Proposed design 2 and 3 is same due to their similar restore operation, while it is reduced by 21.12% in

comparison to RD 8T1R cell [40] and MS 7T1R cell [41]. The cells [40], [41] requires two complex phases namely self-recovery to '0' (SR0) and memristor data recovery (MDR) are required that cause increment in restore delay, while in Proposed design 2 and 3, such complex phases in recovery of data are not required.

Restore power consumption: The restore power consumption of RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3 are found to be 35.64µW, 35.64µW, 30.97µW and 30.97µW, respectively, at Vdd = 1.0V. It is observed that the restore power consumption of Proposed design 3 is similar to Proposed design 2, while it is reduced by 14.47% in comparison to RD 8T1R cell [40], MS 7T1R cell [41]. It is due to increased supply voltage needed to restore the data at internal nodes in [40] and [41], while it is not required in Proposed design 2 and 3.

The supply voltage variation study is also carried out to analyse the restore performance of Proposed design 3 and considered RD nvSRAM cells and the results are shown in Fig. 3.24. The increasing trend in restore delay, while decreasing trend in restore power consumption is observed with reduction in supply voltage.



(a) (b)

Fig. 3.24. (a) Restore delay and (b) restore power consumption of different RD nvSRAM cells and Proposed design 3 at different supply voltage

3.5. Conclusion

In this chapter, two designs (Proposed design2 and Proposed design 3) are presented that uses read decoupled port to improve RM of nvSRAM cell. Both designs employ TiO_2 based memristor to support non-volatile operation. The Proposed design 2 is suitable near subthreshold voltage operation. For this, one of the pull-down transistors is LVT and its gate is grounded. It is done to improve write ability of the cell. The 1T1M structure is connected to internal node Q to perform store and restore operation. The improvement in the WM is 69% in comparison to the considered RD nvSRAM cells at Vdd = 0.6V. It also reduces the write power consumption by avoiding the discharging of bitline WBL during write '1' operation. The power consumption during write '1' operation is reduced by 99.7% in comparison to considered RD nvSRAM cells. Additionally, the use of 1T1M structure eliminates the reset phase in store/restore operation in Proposed design 2. The results indicate that in Proposed design 2, the store and restore powers are saved by 27.63% and 16.24%, respectively, while store and restore delays are improved by 16.56% and 25.33% in comparison to considered RD nvSRAM cells.

The Proposed design 3 uses the column shared technique. The column shared transistor is connected to the source terminal of one of the pull-down transistors. It weakens the pull-down effect of inverter and supports the write '1' operation. It improves WM of the cell. In case of power consumption, the uses of single bitline during write operation helps in consuming most of the cell power. The Proposed design 3 shows the improvement of 31.08% and 10.77% in RM and WM, respectively, while, the write delay is improved by 7.47% in comparison to Proposed design 2. In addition to this, the store and restore performance of Proposed design 3 is similar to Proposed design 2.

Chapter 4

nvSRAM cell with Delay Reduction Techniques

The contents of this chapter are published in:

[1] D. Singh, N. Pandey, and K. Gupta, **"MS 8T1M nvSRAM Cell with Improved Write Performance,"** *in 2022 International Mobile and Embedded Technology Conference (MECON)*, 2022, pp. 425–429, doi: https://doi.org/10.1109/MECON53876.2022.9752160.

[2] D. Singh, N. Pandey and K. Gupta, **"Store and Restore Delay Reduction Techniques of Non-volatile SRAM cells,"** *2023 International Conference on Sustainable Computing and Smart Systems (ICSCSS)*, 2023, pp. 1271-1276, doi: 10.1109/ICSCSS57650.2023.10169690.

4.1. Introduction

In the nvSRAM cells available in literature, the most common issues are leakage, stability and power consumption. Various techniques such as differential power line, shared per word, shared per column, isolation of memristor through internal node using transistor are introduced to overcome the mentioned issues. The delay reduction is also an important concern that is not dealt in the aforementioned cells. The longer delays may lead to extended power on/off time and causes data loss at the time of sudden power failure. The 8T1R [35] and 8T2R [58] nvSRAM cells are introduced to fasten the store and restore operations, however, the method increases the complexity of the nvSRAM cell during non-volatile operation. Thus, there is limited work in the direction of reducing store and restore delays. This chapter brings forward three store/restore delay reduction techniques which are applicable to nvSRAM cells employing 1T1M structure for adding non-volatile feature. To verify the techniques, the Proposed design 1 is taken as case study.

The proposed store/restore delay reduction techniques work on control signals (CTL1 and CTL2) pertaining to 1T1M structure. In addition, this chapter also addresses the improvement in write delay by employing transmission gate (TG) as access transistor. In existing nvSRAM cells with single ended write operation wherein the NMOS transistor is used as access transistor. The NMOS access transistor passes a strong ‘0’ and weak ‘1’. As TG passes both strong ‘1’ and strong ‘0’, it makes write operation faster and reduces write delay. This write delay reduction technique is generic and can be used in existing nvSRAM cells. In this chapter, the TG is introduced as access transistor in MS 7T1R cell [41] and the nvSRAM cell is named as Proposed design 4.

The proposed techniques for store and restore delay reduction are elucidated in section 4.2. It is followed by application of the introduced technique on Proposed design 1 and the timing waveform for store and restore operations are discussed. It also gives the comparative analyses of proposed techniques in terms of store/restore delay and power consumption. In section 4.3, eight transistors and one memristor based Proposed design 4 is introduced. It is followed by detailed explanation of its working during write, read, hold, store and restore operations. The timing waveform during non-volatile operation of Proposed design 4 are also discussed in this section. The results of Proposed design 4 are observed during different operations and the results are compared with considered RD nvSRAM cells. The observations of proposed delay reduction techniques and Proposed design 4 are comprehended in summary section 4.4.

4.2. Techniques for store and restore delay reduction

In nvSRAM cells, the long store and restore time may lead to the loss of data at the time of sudden power failure. From the literature survey, it is observed that nvSRAM cells with 1T1M configuration avoid the complexity during non-volatile operation. This configuration also improves delay and power consumption of the nvSRAM cells during storage and recovery of the data.

The generic structure of nvSRAM cell with 1T1M configuration is shown in Fig. 4.1. Its non-volatile operation consists of store, power down and restore operations. The status of control signals CTL1 and CTL2 during different operations are given in Table 4.1. In SRAM operation, the write, read and hold operations are carried out. It is required to mention here that memristor remains in its initial state i.e., HRS irrespective of internal node content. During store operation, the data transfer takes place as depicted in Fig. 4.1. The logic ‘1’ at

internal node develops a potential difference across memristor and causes memristor state to change from HRS to LRS. If logic '0' is stored at internal node, memristor remains in HRS. The supply voltage is turned off after store operation which causes the internal node to lose its data while, memristor preserves its state. In restore operation, the supply voltage is turned on again to recover the data from memristor as shown in Fig. 4.1. A significant current flow through memristor in its LRS state, charging the internal node to Vdd i.e., logic '1'. After recovery of data, memristor regains its initial state i.e., HRS. When the memristor is in HRS, a modest current flow but it cannot charge the internal node upto Vdd, hence, remains at ground potential i.e., logic '0'. Memristor remains in HRS after restore '0' operation.

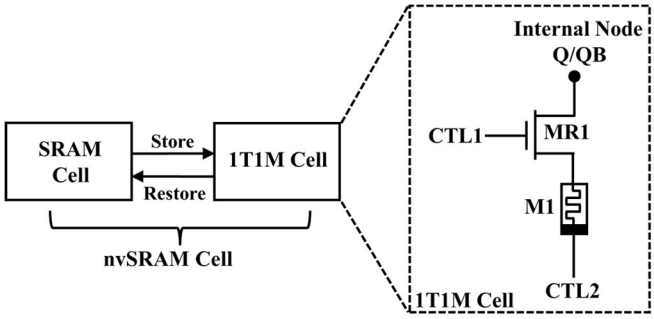


Fig. 4.1. Generic structure of nvSRAM cell with 1T1M structure

Table 4.1. Status of control signals during different operations

Control signals	**Operations**		
	SRAM	**Store**	**Restore**
CTL1	LOW	HIGH	HIGH
CTL2	LOW	LOW	HIGH

In the following subsection, different techniques to reduce store and restore delays are presented.

4.2.1. Negative CTL2 Technique

This technique is applicable for store delay reduction only. In this method, the signal CTL2 is pulled to a negative voltage instead of ground potential during store operation only. The timing waveform for CTL1 and CTL2 during store operation is shown in Fig. 4.2. The negative voltage at CTL2 is achieved by coupling capacitance method suggested in [59], [60]. The increased potential difference across memristor results in larger memristor current which causes faster change in memristor state from HRS to LRS. Due to this, the store delay is reduced effectively. Although, the negative CTL2 technique fastens the store operation speed, it increases store power consumption.

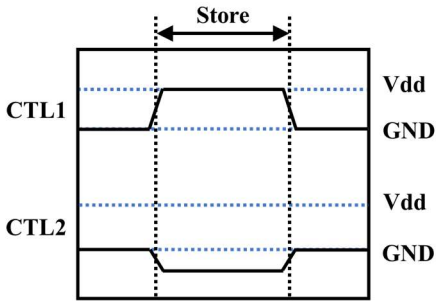


Fig. 4.2. Negative CTL2 technique

4.2.2. Boosted CTL1 Technique

This technique is applicable for the reduction of both store and restore delays. The boosted control signal CTL1 is achieved by charge pump circuit [61] or capacitive coupling method [62]. The timing waveform for CTL1 and CTL2 during store and restore operations is depicted in Fig. 4.3. The boosted CTL1 increases the strength of pass transistor MR1 during store and restore operation. Consequent upon this, the transfer of data into memristor during store operation and recovery of data to the internal node during restore operation become fast. Hence, the store and restore delays are reduced. This advantage is achieved at the cost of increased store and restore power consumption.

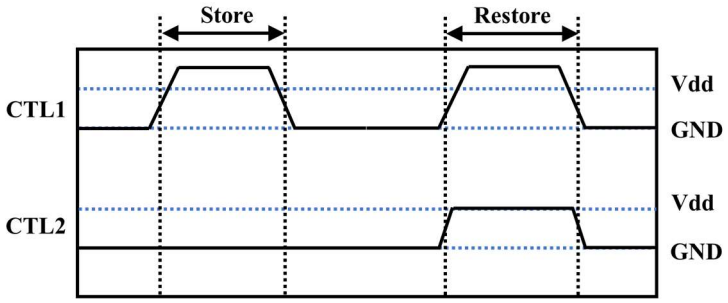


Fig. 4.3. Boosted CTL1 technique

4.2.3. Floating Vss Technique

This technique is useful for restore delay reduction only. In nvSRAM cell, Vss is the source potential of pull-down transistors which generally kept at ground potential. In this approach, the Vss of one of the pull-down transistors is raised to few hundred mV instead of ground [63], as shown in Fig. 4.4. This reduces the strength of pull-down path of the nvSRAM cell. When the data is restored at the internal nodes, the high potential of Vss makes easier recovery of the data leading to reduction of cell's restore delay.

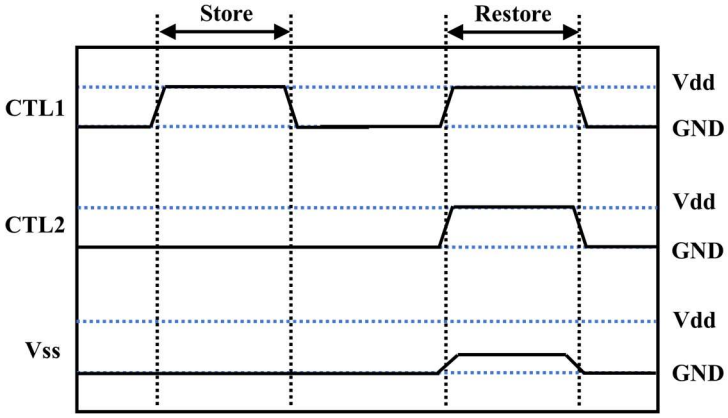


Fig. 4.4. Floating Vss technique

4.2.4. Application of Proposed techniques

The proposed techniques for store and restore delay reduction are applied on Proposed design 1. The memristor model suggested in [55] is used for the analysis of non-volatile performance

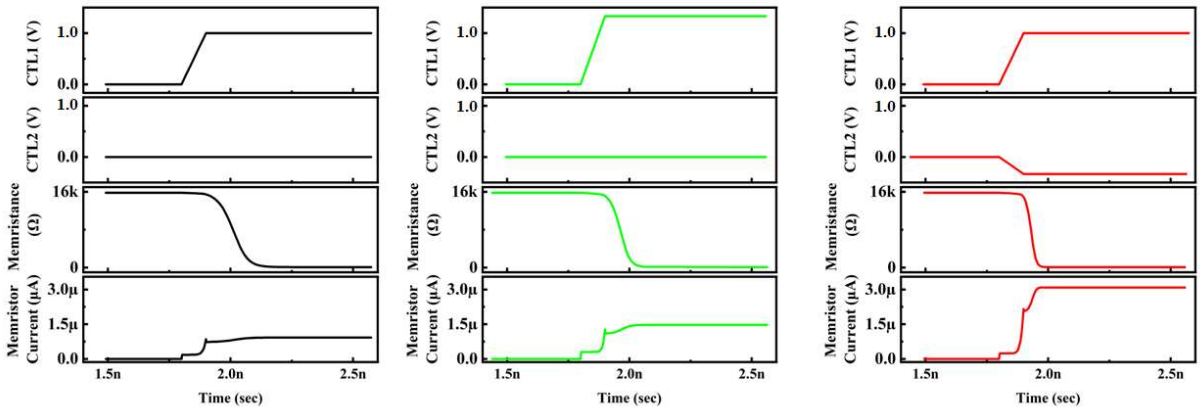
of nvSRAM cell. The timing waveforms, delay and power consumption with different store and restore delay reduction techniques are discussed in this section. For the sake of completeness, the supply voltage variation study on performance parameters is also carried out.

- Store Performance Analysis

  The timing waveform for CTL1, CTL2, the memristance and memristor current for normal values of (CTL1, CTL2); boosted CTL1 and negative CTL2 techniques are shown in Fig. 4.5. It may be observed that the current through memristor is the largest for negative CTL2 technique and the boosted CTL1 technique shows second largest memristor current. This observation is also evident from the memristance change in Fig. 4.5. The store delay for normal values of CTL1 and CTL2 is observed as 38.54ps, while the values of boosted CTL1 and negative CTL2 techniques are 34.52ps and 30.98ps, respectively, at Vdd = 1.0V.

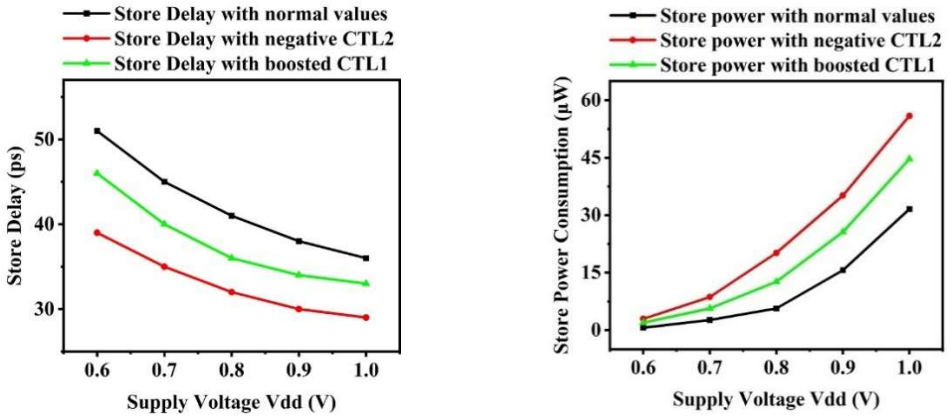
  From the above discussion, it is observed that with boosted CTL1 technique, the store delay is reduced by 10.33%, while a reduction of 19.41% is observed in store delay by negative CTL2 technique in comparison to store delay with normal values of CTL1 and CTL2. It may therefore be summarized that the reduction in store delay is achieved at the cost of increased store power consumption. The power consumption value is observed as 31.6µW, 44.69µW and 55.92µW for normal values of CTL1 and CTL2, boosted CTL1 and negative CTL2 techniques, respectively, at the same supply voltage. It is observed that the store power consumption is increased by 29.3% and 43.5% using boosted CTL1 and negative CTL2 techniques, respectively, in comparison to store power consumption with normal values of CTL1 and CTL2.

The effect of supply voltage variation is also analyzed for store delay and store power consumption and the results are shown in Fig. 4.6. It is observed that the store delay increases, while, store power consumption decreases with reduction is supply voltage.



(a) (b) (c)

Fig. 4.5. Timing waveform for store operation using (a) normal values (b) boosted CTL1 technique and (c) negative CTL2 technique of Proposed design 1



(a) (b)

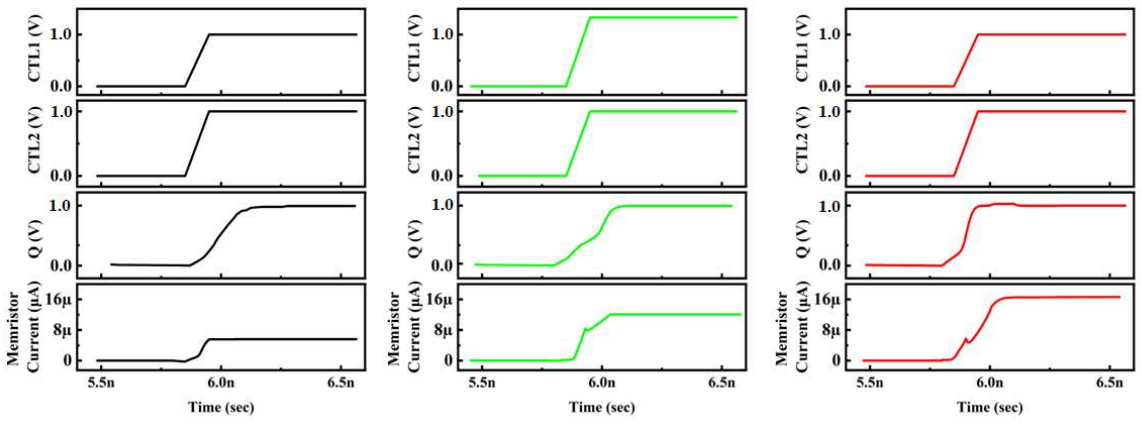
Fig. 4.6. (a) Store delay and (b) store power consumption of Proposed design 1

- Restore performance analysis

  The timing waveforms for control signals CTL1 and CTL2, data recovery at internal node Q and memristor current with normal values of CTL1 and CTL2, boosted CTL1

and floating Vss techniques at Vdd = 1.0V are depicted in Fig. 4.7. It may be observed that the current through memristor is larger when floating Vss technique is applied and second largest is case of boosted CTL1 technique. The faster change is also observed in data recovery at internal node Q as memristor current increases. With normal values of CTL1 and CTL2. the restore delay is found as 24.56ps. The restore delay with boosted CTL1 and floating Vss technique is found to be 20.95ps and 19.26ps, respectively.

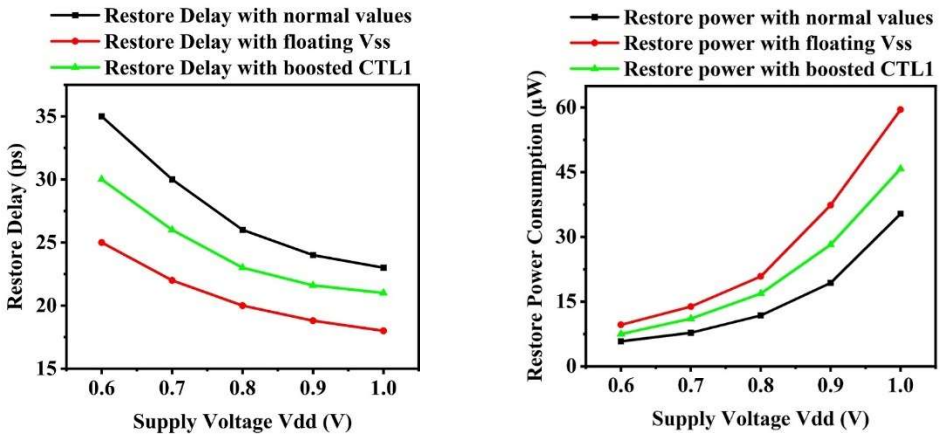
From the above discussion, it is observed that the restore delay is reduced by 14.54% and 21.74% due to boosted control signal CTL1 technique and floating Vss technique, respectively, in comparison to restore delay with normal values of CTL1 and CTL2. This reduction in restore delay is achieved at the cost of increased restore power consumption. The boosted CTL1 method increases the restore power consumption by 22.75%, while, the floating Vss method gives a maximum increment of 40.67%.



(a) (b) (c)

Fig. 4.7. Timing waveform for restore operation using (a) normal values (b) floating Vss technique and (c) boosted CTL1 technique of Proposed design 1

The supply voltage variation study is also carried out to examine restore delay and restore power consumption and the results are shown in Fig. 4.8. The increasing trend in restore delay, while, decreasing trend in restore power consumption is observed with reduction is supply voltage.



(a) (b)

Fig. 4.8. (a) Restore delay and (b) restore power consumption of Proposed design 1

4.3. Proposed design 4

The section 4.2 presents different store and restore delay reduction techniques which are applicable on nvSRAM cells which uses 1T1M structure to perform non-volatile operation. These techniques alter the values of signals CTL1 and CTL2. A brief introduction of each technique is given in section 4.2. In addition to this, write delay is also an important factor. In existing nvSRAM cells with single ended write operation, the NMOS transistor is used to perform write operation. As the NMOS transistor passes strong '0' and weak '1'. Due to this, write '1' operation becomes difficult. To overcome this, the NMOS transistor is replaced by transmission gate (TG). It consists of NMOS and PMOS transistor connected in parallel and passes strong '0' and strong '1' which makes write '1' operation easier and reduces write

delay. In Proposed design 4, a TG based nvSRAM cell is introduced and its description is given below.

The diagrammatic representation of Proposed design 4 is shown in Fig. 4.9. It contains back-to-back inverters consisting of transistors Mn1-Mp1 and Mn2-Mp2 that can store single bit of data at internal nodes Q and QB. The transmission gate (TG) consists of transistors Mn3 and Mp3 and it is used to perform write operation. The TG is controlled by control signal WWL and complemented signal WWLB. The read decoupled port formed by transistors T1 and T2 is used to perform the read operation. The signal RWL controls transistor T1 and internal node QB controls transistor T2. The bitlines WBL and RBL performs write and read operations, respectively. The memristor M1 is attached with internal node Q of the Proposed design 4 and its operation is controlled by transistor T1. Memristor initial state is HRS and it changes to LRS depending on internal node Q content during store operation. According to memristor state, the data is recovered to internal node in restore operation. Additionally, the write assist transistor (WAT) and gate enabled transistor (GET) are shared-per-word transistors which assists Proposed design 4 during write and restore operations. Also, the Vs line is asserted high during write and restore operation and it is asserted low during read operation.

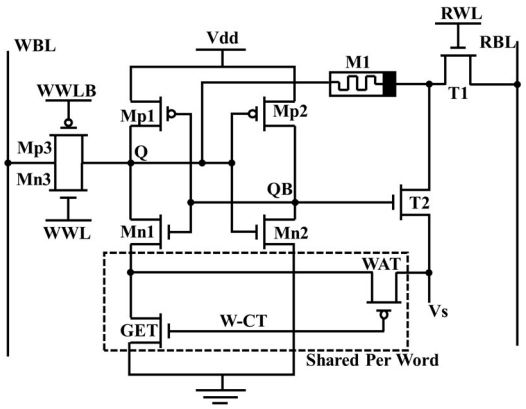


Fig. 4.9. Schematic of Proposed design 4

4.3.1. Operation of Proposed design 4

In this subsection, the operation of Proposed design 4 is described during write, read, hold, store and restore operations. The status of control signals during each operation is summarized in Table 4.2.

Table 4.2. Operating Condition of Proposed design 4

Signals	**Operations**				
	Write	**Read**	**Hold**	**Store**	**Restore**
WWL	HIGH	LOW	LOW	LOW	LOW
WWLB	LOW	HIGH	HIGH	HIGH	HIGH
RWL	LOW	HIGH	LOW	HIGH	HIGH
W-CT	LOW	HIGH	HIGH	HIGH	HIGH

Write operation

Prior to write operation, the bitline WBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 4.2. The GET transistor is turned off, while WAT transistor is turned on due to ground potential of WCT signal and the pull-down effect of transistor Mn1 is removed. During write '1' operation, the bitline WBL remains at Vdd. With the assertion of signals WWL and WWLB, the TG is turned on. The removal of pull-down effect of transistor Mn1 supports the flipping of internal node Q content to logic '1'. The internal node QB content is flipped to logic '0' due to feedback connection. During write '0' operation, the bitline WBL is discharged to ground. With the assertion of control signals WWL and WWLB, the logic '0' is transferred to internal node Q through TG, while internal node QB content is flipped to logic '1'. The write paths of Proposed design 4 are shown in Fig. 4.10. Due to the presence of TG, the write delay of Proposed design 4 is reduced. The

additional path through memristor further supports write operation. The removal of pull-down effect of transistor Mn1 along with TG increases write ability and hence, WM of Proposed design 4 is also improved.

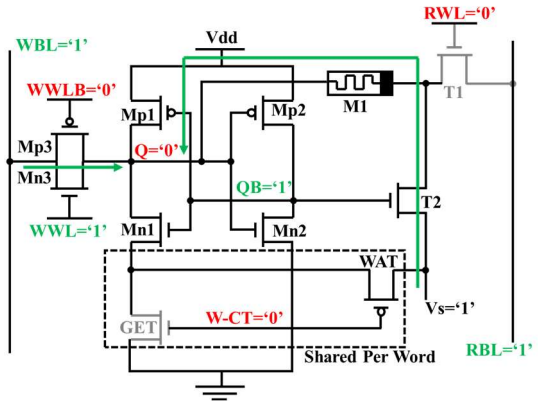


Fig. 4.10. Proposed design 4 during write operation

Read operation

Prior to read operation, the read bitline RBL is pre-charged to Vdd. The control signals are asserted as mentioned in Table 4.2. With the assertion of RWL signal, the read pass transistor T1 is turned on. If internal node Q = '0' then node QB = '1'; it turns on transistor T2 and the bitline RBL is discharged through read path and read '0' operation is performed. Similarly, if node Q = '1' then node QB = '0'; the transistor T2 remains off, no path is formed to discharged bitline RBL and hence, it remains at Vdd performing read '1' operation. The Proposed design 4 consists of two read paths: one path is through read port formed by transistors T1 and T2 and another path is through transistor T1 to memristor M1 to internal node Q as shown in Fig. 4.11. It reduces read delay of the Proposed design 4. Also, the RM of the Proposed design 4 is improved due to the isolated read port.

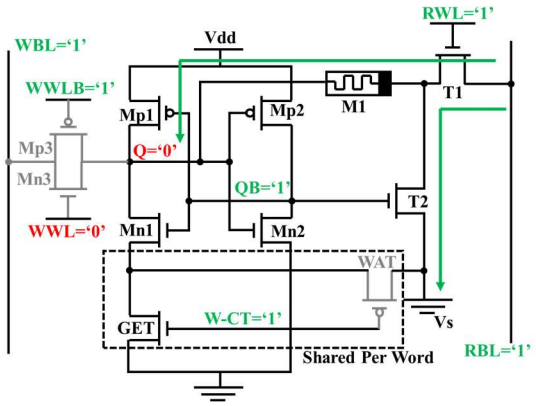


Fig. 4.11. Proposed design 4 during read operation

Hold operation

During hold operation, the control signals are asserted as mentioned in Table 4.2. The schematic of Proposed design 4 in hold mode is shown in Fig. 4.12. The internal node content is hold by back-to-back connected inverter pair.

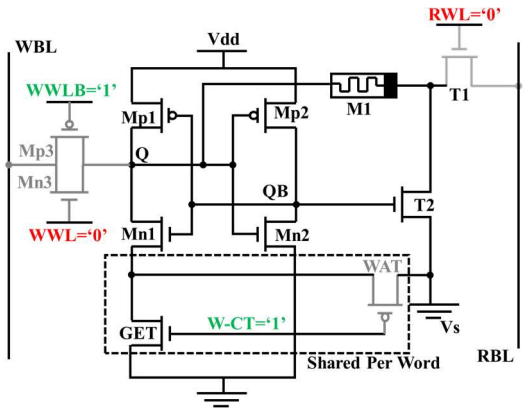


Fig. 4.12. Proposed design 4 during hold operation

Non-volatile operation

In Proposed design 4, the non-volatile operation consists of store, power down and restore operations. The control signals are asserted as mentioned in Table 4.2. Prior to store operation, the write operation is performed. Memristor M1 remains in its initial HRS state irrespective of internal node content. The store operation is performed in two phases, namely:

set and reset. During set phase, the RWL signal is asserted HIGH and RBL line is charged to Vdd. If logic '0' is present at the internal node Q, the memristor state is changed to LRS. Otherwise memristor M1 remains in its initial state if logic '1' is present at internal node Q. It is due to zero potential difference across memristor. In reset phase, the bitline RBL is discharged to ground. If internal node Q is at logic '1', the memristor retain its HRS state, else it remains in LRS state for Q = '0'. After completion of store operation, supply voltage is turned off and the control signals are asserted LOW. Due to this, the data is lost from the internal node of Proposed design 4, however, memristor M1 maintains its state.

In restore operation two phases are performed: self-recovery to '0' (SR0) and memristor data recovery (MDR). In SR0 phase, the supply voltage is turned on, the bitline WBL is set to ground and signals WWL and WWLB are asserted HIGH and LOW, respectively. It is done to maintain logic '0' at the internal node Q. After SR0 phase, data is recovered from memristor to internal node of the Proposed design 4 during MDR phase. The signal RWL is asserted HIGH and bitline RBL is charged to Vdd. The LRS state of memristor allows the flow of a large current through it and internal node Q is charged to Vdd indicating that logic '1' is restored at node Q. If memristor is in HRS state, the current passing through the memristor is not sufficient to raise the internal node Q potential and it continues to remain at ground potential indicating that node Q is restored with logic '0'. As opposite data is recovered at internal node of the Proposed design 4 after completion of restore operation, additional inverters are required at input and output stage to obtain the original data. During store/restore operation, the potential of Vs line is fixed to Vdd so that the effect of transistor T2 can be neglected. The signal WCT is set to voltage less than Vdd during restore operation to weaken the GET transistor which improves the restore performance of Proposed design 4.

4.3.2. Simulation results and discussion

The SPICE simulations are carried out using 32nm PTM model to analyse the performance of Proposed design 4. The memristor model suggested in [55] is used to observe the non-volatile performance. In this section, first the timing waveform of Proposed design 4 is discussed at Vdd=1.0V. It is followed by the performance evaluation during different operations such as write, read, hold, store and restore and the results are compared with the considered RD nvSRAM cells [40], [41]. For the sake of fair comparison, the aspect ratios (W/L) of different transistors of considered RD nvSRAM cells [40], [41] and Proposed design 4 are taken as 72nm/36nm.

Timing waveform

The non-volatile operation is subdivided into store, power down and restore. The time period for each operation is set more than twice of the time period taken by memristor to change its state from HRS to LRS [32]. The following observations are made from Fig. 4.13(a) that shows the waveform to execute write – store – power down – restore logic '1' operation.

a) First, write '1' operation is performed from 0 to 2ns. For this, the pre-charged bitline WBL remains at Vdd. The signal WWL is asserted HIGH while, the control signals WCT, WWLB and RWL are asserted LOW. The internal node Q content is changed to logic '1' through TG while, internal node QB is changed to logic '0'.

b) From 2ns to 4ns, the store operation is performed. The signals WWLB, WCT and RWL are asserted HIGH, while, the signal WWL is asserted LOW. The store operation takes place in set and reset phases. In set phase, the RBL line remains at Vdd therefore, memristor remains in its initial state. Subsequently, RBL is discharged in reset phase. However, memristor retains its state.

c) The power down mode occurs from 4ns to 6ns. The supply voltage is turned off and the controlling signals are asserted LOW. The internal node loses their data, while memristor M1 maintains its HRS state.

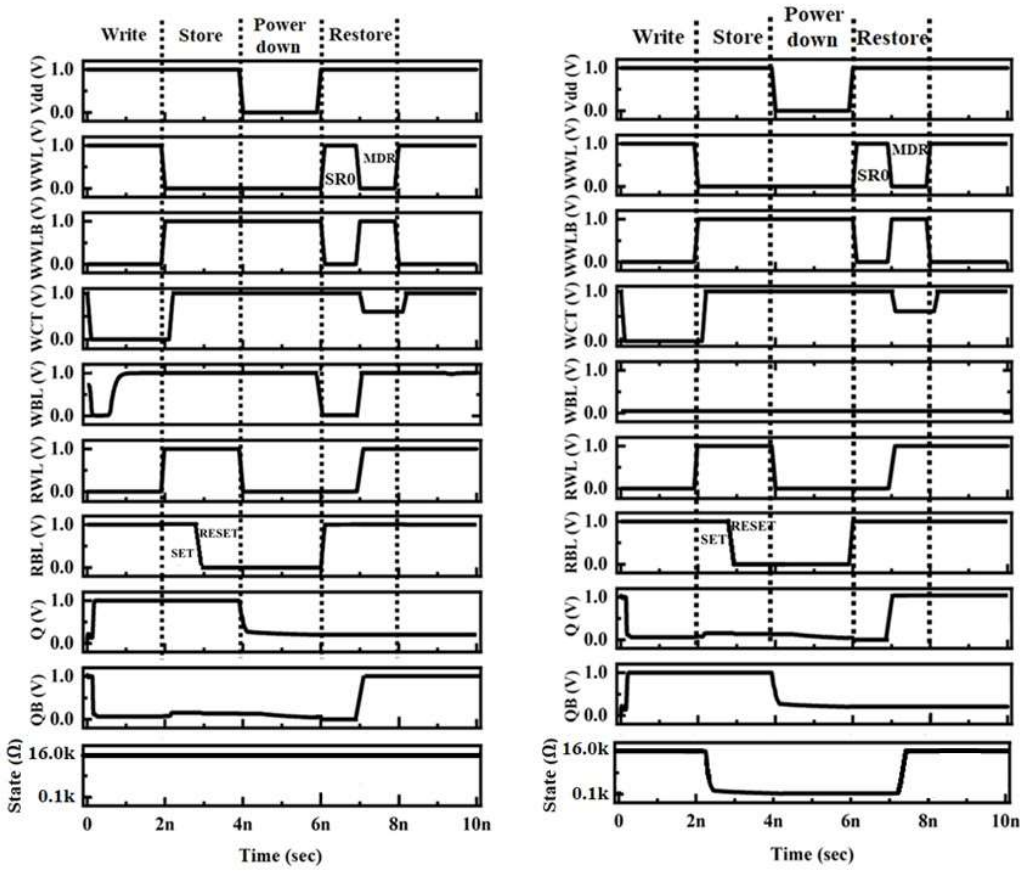
d) After power down, the restore operation is performed from 6ns to 8ns. It is performed in SR0 and MDR phases. In SR0 phase, the write '0' operation is performed to ensure logic '0' at internal node Q. For this, WWL and WWLB signals are asserted HIGH and LOW, respectively, and WBL is discharged to ground. In MDR phase, the control signals WWLB and RWL are asserted HIGH and WWL is asserted LOW. Due to HRS state of memristor, a low current flow through it which is not sufficient to raise the internal node Q potential and it continues to remain at ground potential i.e., logic '0'.

Similarly, the timing waveform to execute write – store – power down – restore logic '0' operation is shown in Fig. 4.13(b). First, the write '0' operation is performed by discharging bitline WBL to ground. The control signal WWL is asserted HIGH, while the remaining signals are asserted LOW. It changes internal node Q to logic '0'. It is followed by store operation. The data transfer in memristor is done during set phase. The RBL line remains at Vdd. With the assertion of signal RWL, the memristor M1 changes its state to LRS. During reset phase, the RBL line is discharged to ground. Due to this, the potential difference across memristor is zero and hence, memristor continues to retain its LRS state.

During power down, the supply voltage is turned off and the control signals are asserted LOW. Due to this, the internal nodes lose their data, however, memristor M1 maintains its LRS state. In restore operation, first SR0 phase take place by performing write '0' operation. In MDR phase, the signals RWL is asserted HIGH and RBL line is charged to Vdd. Due to

LRS state of memristor, a large current flow through it and the internal node Q is charged to Vdd i.e., logic '1'.

From Fig. 4.13(a) and (b), it is observed that the opposite data is recovered at the internal nodes after completion of restore operation. Hence, with the help of additional inverter, the original data can be retrieved.



(a) (b)

Fig. 4.13. Timing waveform for non-volatile operation of Proposed design 4 for (a) Logic '1' and (b) Logic '0

Performance analysis

In this sub-section, the performance of Proposed design 4 is compared with the considered RD nvSRAM cells [40], [41] at Vdd = 1.0V. Various performance parameters such as

margin, delay and power consumption are evaluated for write, read, hold, store and restore operations. The effect of variation in supply voltage Vdd is also studied for completeness.

- Write Performance Analysis

  The write performance of Proposed design 4, RD 8T1R cell [40] and MS 7T1R cell [41] is discussed in terms of WM, write delay and write power consumption.

  Write margin (WM): The WM for RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 are found as 518mV, 490mV and 585mV, respectively, at Vdd = 1.0V. Thus, the WM of Proposed design 4 is improved by 11.45% and 16.24% in comparison to RD 8T1R cell [40] and MS 7TR cell [41], respectively. It is due to presence of TG that gives strong '1' and strong '0' through PMOS and NMOS transistors, respectively, and improves the pull-up ratio which increases WM of Proposed design 4.

  Write delay: The write delay of RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 are found to be 32.76ps, 54.98ps and 28.74ps, respectively at Vdd = 1.0V. Therefore, the write delay for Proposed design 4 is reduced by 12.27% and 47.26% in comparison to RD 8T1R cell [40] and MS 7T1R cell [41], respectively. As the TG provides two paths to write data from bitline WBL to internal node Q of the Proposed design 4 which increases write operation speed and reduces write delay.

  Write power consumption: The write power consumption for RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 are observed as 96.52µW, 2.35µW and 3.55µW, respectively, for write operation at Vdd =1.0V. Thus, the write power consumption of Proposed design 4 is reduced by 96.32% in comparison to the RD 8T1R cell [40] due to single ended write operation. However, an increment of 33.8% is observed in the write power consumption of Proposed design 4 in comparison to MS 7T1R cell [41].

The supply voltage variation is also studied to analyse the write performance of Proposed design 4, RD 8T1R cell [40] and MS 7TR cell [41] and the results are shown in Fig. 4.14. It is observed that the WM and write power consumption decreases, while, write delay increases with reduction in supply voltage.

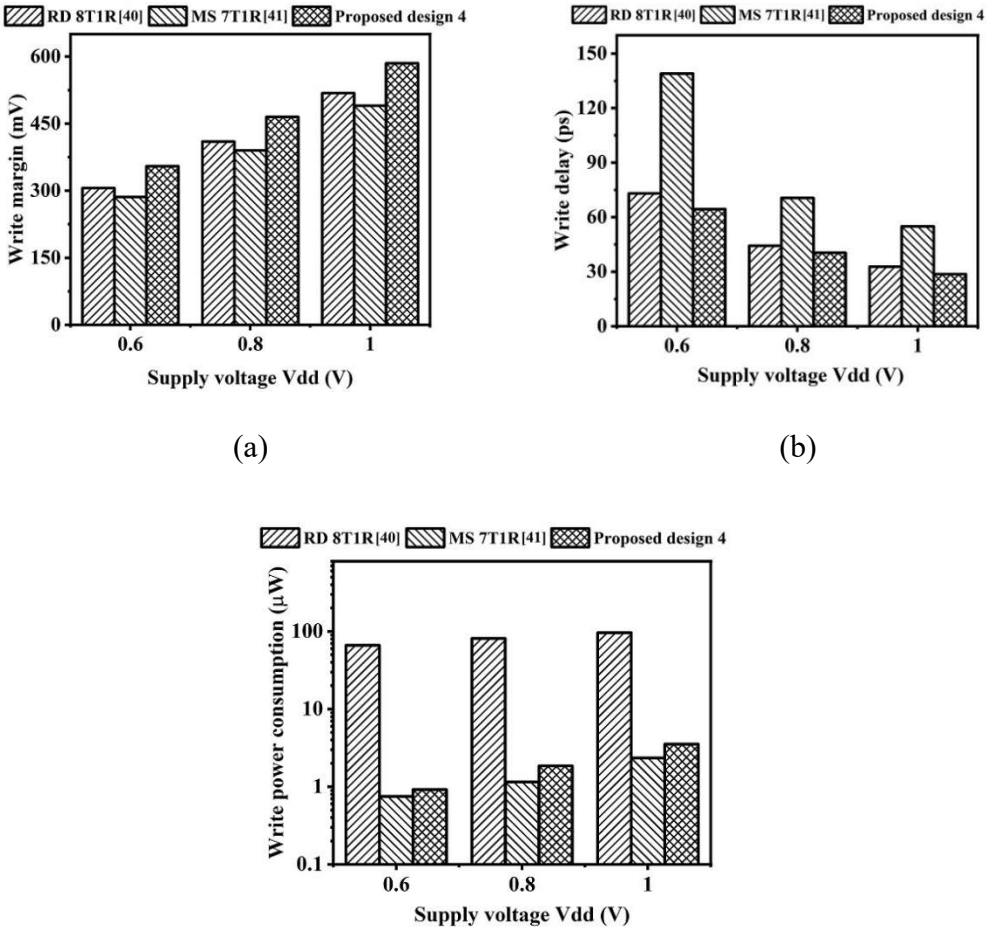


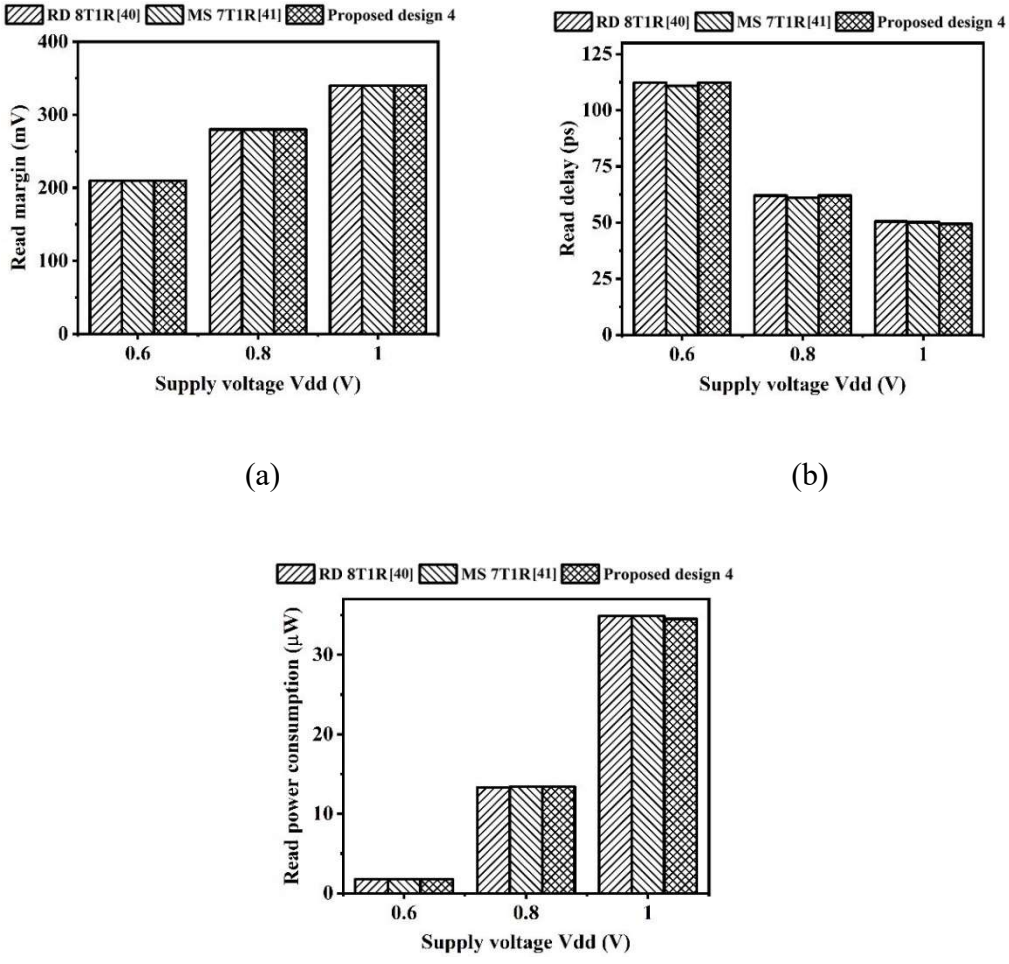
Fig. 4.14.(a) Write margin (b) write delay and (c) write power consumption of Proposed design 4 and considered RD nvSRAM cells at different supply voltage

- Read Performance Analysis

  The read performance of Proposed design 4 is analysed in terms of read margin (RM), read delay and read power consumption and the corresponding values are found to be

340mV, 49.49ps and 34.5µW, respectively, at Vdd =1.0V. As the read operation in Proposed design 4, RD 8T1R cell [40] and MS 7TR cell [41] is performed through the same port, their read performance is similar.

The supply voltage variation study to analyse the read performance of Proposed design 4, RD 8T1R cell [40] and MS 7TR cell [41] is also carried out and the results are shown in Fig. 4.15. The decreasing trend in RM and read power consumption, while an increasing trend in read delay is observed with reduction in supply voltage.



(a) (b)

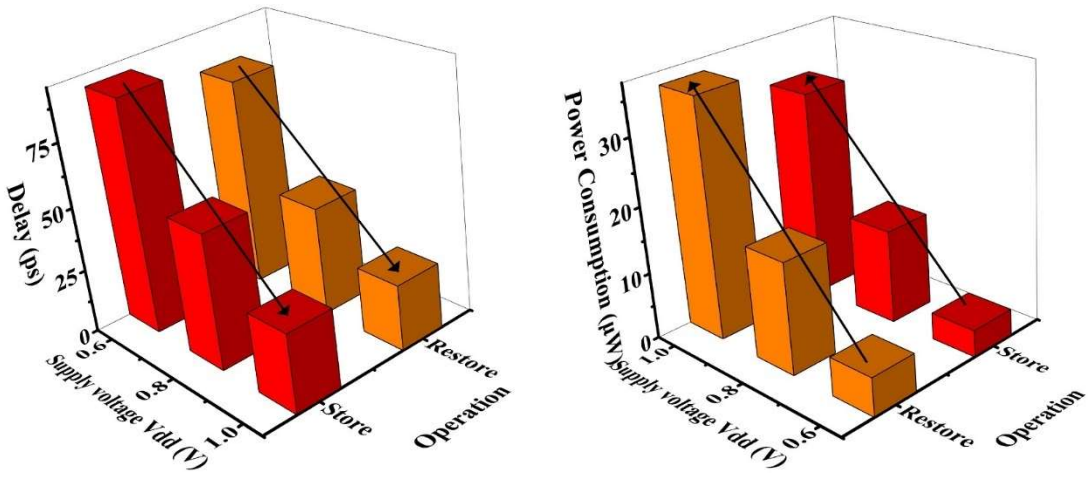
(c)

Fig. 4.15. (a) Read margin (b) read delay and (c) read power consumption of Proposed design 4 and considered RD nvSRAM cells

- Store and Restore Performance Analysis

  The store and restore performances of Proposed design 4, RD 8T1R cell [40] and MS 7TR cell [41] are analyzed in terms of delay and power consumption at Vdd = 1.0V. As the Proposed design 4 and considered RD nvSRAM cells follow same process to perform store and restore operations, their delay and power consumption is similar. From simulations, it is found that the time needed to store the internal node content into memristor is 30.25ps. The data form memristor is restored to internal node in 25.05ps. The store and restore power consumptions are observed as 30.5µW and 35.64µW, respectively.

For the sake of completeness, the supply voltage variation study is also carried out for store/restore delay and power consumption and the results are shown in Fig. 4.16. It is observed that the reduction in supply voltage increases store/restore delay, while, the store/restore power consumption is decreased.



(a) (b)

Fig. 4.16. Store and restore (a) delay and (b) power consumption of Proposed design 4

4.4. Conclusion

In this chapter, different techniques for the reduction of store and restore delay of nvSRAM cells are introduced. The negative CTL2 and boosted CTL1 techniques are introduced to reduce store delay. The floating Vss and boosted CTL1 techniques are introduced to reduce restore delay of the nvSRAM cell. The negative CTL2 technique gives a maximum reduction of 19.41% in store delay at Vdd = 1.0V. The floating Vss technique shows the best performance in restore delay reduction and it is reduced by 21.74% at the same supply voltage. However, the reduction in store and restore delays is achieved at the cost of increased store/restore power consumption.

Further, the Proposed design 4 is introduced to reduce write delay. The use of TG between bitline WBL and internal node Q decreases the write delay of the Proposed design 4. Also, the WAT and GET are shared-per-word transistors which improves the write '1' performance and WM of Proposed design 4. The single bitline to perform write operation decreases write power consumption of Proposed design 4 to an extent in comparison to the differential RD nvSRAM cell. The read operation is performed through read decoupled port. The Proposed design 4 maintains store and restore delay and power consumption performance same as the considered RD nvSRAM cells. The Proposed design 4 shows the maximum improvement of 47.26% and 16.24% in write delay and WM, respectively, in comparison to the considered RD nvSRAM cells at Vdd=1.0V.

Chapter 5

Process Invariant nvSRAM Cell

The contents of this chapter are published in:

[1] D. Singh, N. Pandey, and K. Gupta, **"Schmitt Trigger 12T1M Non-volatile SRAM cell with improved process variation tolerance,"** *AEUE - International Journal of Electronics and Communications*, vol. 162, pp. 1–12, 154573, 2023, doi: 10.1016/j.aeue.2023.154573. **(SCIE indexing, IF 3.169)**

[2] D. Singh, N. Pandey, and K. Gupta, **"Process invariant Schmitt Trigger non-volatile 13T1M SRAM cell,"** *Microelectronics Journal*, vol. 135, pp. 1–10, 2023, doi: 10.1016/j.mejo.2023.105773. **(SCIE indexing, IF 1.992)**

5.1. Introduction

The semiconductor memory is an indispensable part of computing platforms as well as hand held devices [19], [64]. The proliferation of wearable and IOT devices has necessitated the designs that consume less power for extended battery life. The introduction of non-volatile memory (NVM) device in SRAM is an effective choice in power constrained devices that enable power-down mode [65] to save power in addition to storing the state of SRAM. However, due to scaling in technology and supply voltage, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for nvSRAM cells employing minimum-sized transistors [66], [67].

The voltage scaling reduces the power consumption quadratically and lowers the leakage power linearly (up to first order) [68]. However, at lower supply voltage, nvSRAM cell may suffer from memory failures and increased sensitivity toward process variations [66]. In small geometry devices, the inter die and intra die process variations such as random dopant fluctuation (RDF) and line edge roughness (LER) limit the memory cell's operations especially near subthreshold region [67], [68]. It may result in threshold voltage mismatch between adjacent transistors in a memory cell [69]. The combined effect of inter die and intra die variations may result in memory failure like write failure, read failure, hold failure, access time, store and restore failure. The memory failure probability is further deteriorating with at lower technology nodes. Therefore, there will be limitation on minimum supply voltage (Vmin) at which memory cell can perform all modes of operation. The literature survey on nvSRAM cells shows that no work has been done in the direction of failure probability and Vmin analysis therefore it is apt to address this issue.

In this chapter, two process invariant nvSRAM cells (Proposed design 5 and Proposed design 6) are introduced. The CMOS inverters in core are replaced by Schmitt trigger (ST) inverters which has inherent tolerance against process variations. The differential write along with ST action improves write performance of the proposed designs, while, the read decoupled (RD) port along with ST action improves RM. In Proposed design 5, the non-volatile operation in obtained by placing memristor between internal node and read bitline through read pass transistor, whereas, 1T1M structure is used in Proposed design 6 for same purpose.

The section 5.2 gives the detailed description of Proposed design 5 during write, read, hold, store and restore operations. It also provides the timing analyses of non-volatile waveform. Further, the performance of Proposed design 5 is analyzed for all operations and the results are compared with considered RD nvSRAM cells. Thereafter, the schematic and working of Proposed design 6 is discussed in section 5.3. This section also includes the timing waveform of Proposed design 6 during non-volatile operation and comparative analyses with considered RD nvSRAM cells for all operations. Further, the failure probability analysis is carried out to observe Vmin value of both the proposed designs and considered RD nvSRAM cells in section 5.4. The findings are comprehended in the last section 5.5 of the chapter.

5.2. Proposed design 5

The Proposed design 5, as shown in Fig. 5.1, uses two back-to-back ST inverters to store single bit of data at internal nodes Q and QB. The transistors (Mp1-Mn1-Mn5-Mn6) and (Mp2- Mn2-Mn7-Mn8) form ST inverters. The write access transistors Mn3 and Mn4 are controlled by write wordline WWL and performs the write operation at internal nodes Q and QB, respectively. The read port transistors T1 and T2 are controlled by read wordline RWL and node QB, respectively. The bitlines WBL/WBLB and RBL are used to perform the write

and read operations of the nvSRAM cell, correspondingly. The column-based signals WL_Y1 and WL_Y2 controls the ST action of the Proposed design 5. The memristor M1 is used to perform the non-volatile operation. It is connected to the internal node Q of the Proposed design 5 and its operation is controlled by read pass transistor T1 and read bitline RBL.

The feedback transistors Mn6 and Mn8 activates the ST action of the Proposed design 5 by enhancing the threshold voltage of transistors Mn1 and Mn2, respectively. During write mode, the ST action supports write operation by enhancing the WM of the Proposed design 5, while, during read and hold modes, the ST action gives the tolerance against process variations.

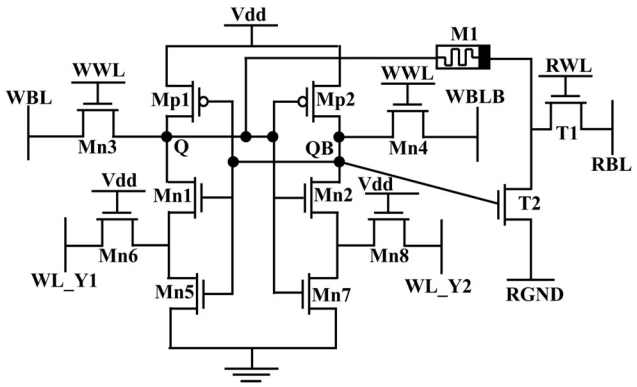


Fig. 5.1. Schematic of Proposed design 5

Table 5.1. Operating condition of Proposed design 5

Signals	Operations					
	Write '1'	**Write '0'**	**Read**	**Hold**	**Store**	**Restore**
WWL	HIGH	HIGH	LOW	LOW	LOW	LOW
WL_Y1	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
WL_Y2	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
RWL	LOW	LOW	HIGH	LOW	HIGH	HIGH
RGND	HIGH	HIGH	LOW	HIGH	HIGH	HIGH

5.2.1. Operation of Proposed design 5

In this subsection, the operation of Proposed design 5 is described during write, read, hold, store and restore operations. The status of control signals during each operation is summarized in Table 5.1.

Write operation

To perform the write operation, the write bitlines WBL and WBLB are pre-charged to Vdd. The control signals are asserted as tabulated in Table 5.1. During write '1′ operation, the bitline WBL remains at Vdd while, bitline WBLB is discharged to ground. The threshold voltage of transistor Mn1 is increased due to presence of transistor Mn6, causing decreased driving capability of pull-down path (through transistors Mn1 and Mn5). It supports the charging of internal node Q to Vdd. An additional write path is formed through memristor M1 as shown in Fig. 5.2. If memristor is in LRS state, two paths exist to support the charging of node Q as shown in Fig. 5.2(a), whereas the additional path does not have any role in case memristor is in HRS state as shown in Fig. 5.2(b). On the other side, internal node QB discharges through access transistor Mn4. An additional discharging path is formed through feedback transistor Mn8 which supports quick discharging of internal node QB. The write '0′ operation is performed in the similar manner due to the symmetrical structure of the Proposed design 5. The bitline WBL is discharged to ground while WBLB remains at Vdd. The internal node Q discharges through access transistor Mn3 and feedback transistor Mn6. Due to ST action, the feedback transistor Mn8 increases the threshold voltage of transistor Mn2. It reduces the driving capability of pull-down path formed by transistors Mn2 and Mn7 and it supports the charging of internal node QB.

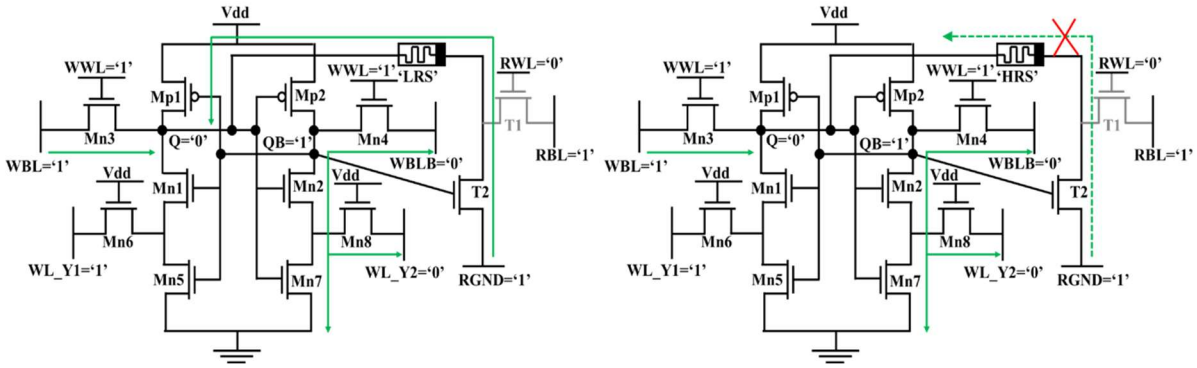
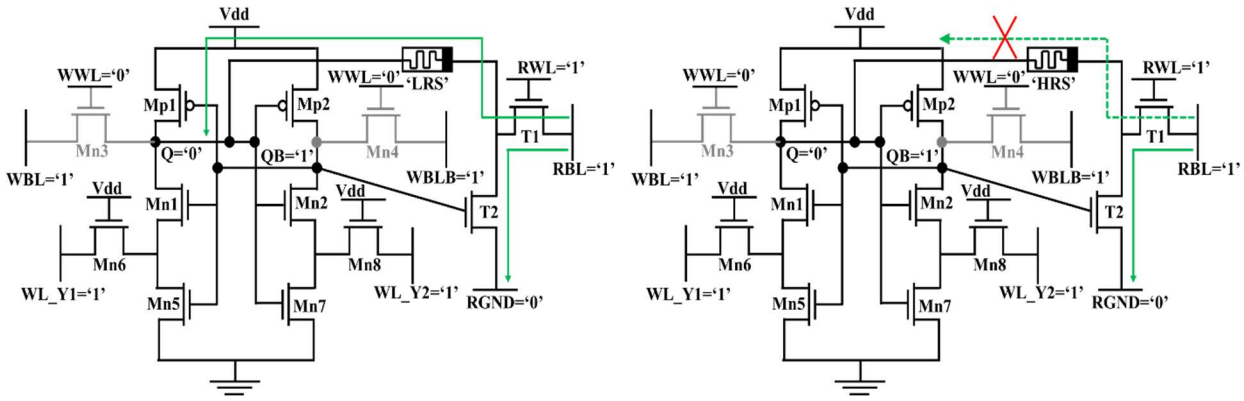


Fig. 5.2. Proposed design 5 during write '1' operation when memristor M1 is in (a) LRS state and (b) HRS state

Read operation

To perform the read operation, the read bitline RBL is pre-charged to Vdd. The control signals are asserted as enlisted in Table 5.1. During read '0′ operation, transistor T2 turns on due to high potential of internal node QB. The current discharge path is formed through bitline RBL- transistor T1 - transistor T2 - signal RGND, as shown in Fig. 5.3. An additional read path exists through transistor T1 - memristor M1 - internal node Q which supports the read operation. The LRS state of memristor allows the flow of current through this path as shown in Fig. 5.3(a). While, the HRS state of memristor disrupts the current flow through it as shown in Fig. 5.3(b). During read '1′ operation, the transistor T2 turns off as internal node QB is at logic '0′ and prevents the discharging of bitline RBL. Also, the signals WL_Y1 and WL_Y2 are asserted HIGH during read operation to activate the ST action of the Proposed design 5. It prevents the internal nodes Q and QB to flip the internal node data and hence, improves the read stability of Proposed design 5.



(a) (b)

Fig. 5.3. Proposed design 5 during read '0' operation when memristor M1 is in (a) LRS state and (b) HRS state

Hold operation

During hold operation, the control signals are asserted according to Table 5.1 and the resulting schematic of Proposed design 5 is shown in Fig. 5.4. Any change at internal node (Q and QB) due to process variation is prevented by ST action of feedback transistors (Mn6 and Mn8) and the stacking effect of pull-down transistors (Mn1-Mn5 and Mn2-Mn7), resulting in improved stability against process variations.

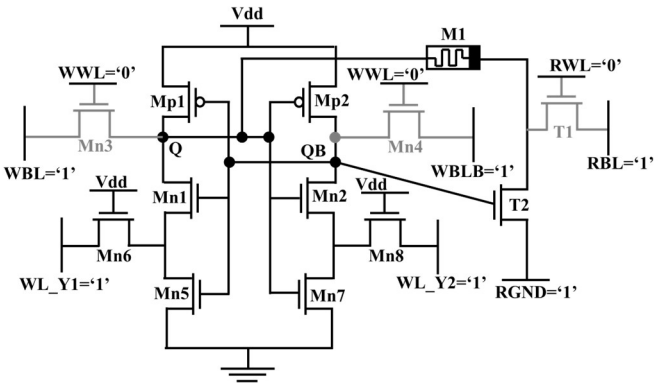


Fig. 5.4. Proposed design 5 during hold operation

Non-volatile operation

The non-volatile operation of Proposed design 5 is carried out in store, power down and restore operations. It is required to mention that initial state of memristor is HRS irrespective of internal node content. Prior to store operation, the write operation is performed. It is followed by store operation that is performed in two phases, namely: set and reset. In set phase, the supply voltage and signal RWL are asserted to V_{SET} (set voltage of memristor). The bitline RBL is also charged to V_{SET}. If logic '0′ is stored at internal node Q, the state of memristor is changed to LRS. If internal node Q is at logic '1′, memristor maintains its initial state as there is no potential drop across it. In reset phase, the supply voltage, Vdd is set to V_{RESET} (reset voltage of memristor) and the bitline RBL is discharged to ground. If logic '1′ is stored at internal node Q, the memristor's state is changed to HRS and if logic '0′ is present at internal node Q, the memristor maintains its LRS state as both terminals of memristor are at same potential.

After completion of store operation, the power down takes place. The supply voltage is turned off and all the control signals are asserted LOW that causes the loss of internal node data whereas memristor maintains its state.

When supply voltage is turned on again, the data is restored from memristor to internal node of the Proposed design 5. To perform the restore operation, first self-recovery to '0' (SR0) phase takes place. This phase is performed to ensure that logic '0' is available at internal node Q. It is followed by memristor data recovery (MDR) phase wherein, the signal RWL is asserted HIGH and the bitline RBL is charged to Vdd. If memristor is in LRS state, a large current flow through memristor and charges the internal node Q to logic '1′, performing the restore '1′ operation. While, the HRS state of memristor slow down the flow of current which

is not enough to charge the internal node Q to Vdd and it remain at logic ‘0′, completing restore ‘0′ operation. It should also be noted that the opposite data is recovered at internal node after restore operation. To obtain the original data, the additional inverters are required at input and output stages.

5.2.2. Simulation results and discussion

The SPICE simulations are carried out using 32nm PTM model to analyse the performance of Proposed design 5. The memristor model suggested in [55] is used to observe the non-volatile performance. In this section, first the timing waveform of Proposed design 5 is discussed at Vdd=0.6V. It is followed by the performance evaluation during different operations such as write, read, hold, store and restore and the results are compared with the RD 8T1R cell [40], MS 7T1R [41], Proposed design 2 and Proposed design 4. For the sake of fair comparison, the aspect ratios (W/L) of different transistors of considered RD nvSRAM cells and Proposed design 5 are taken as 72nm/36nm.

Timing waveform

The non-volatile operation is subdivided into store, power down and restore operation. The time period for each operation is set more than twice of the time period taken by memristor to change its state from HRS to LRS [32]. The waveform to execute write – store – power down – restore logic ‘1’ operation is depicted in Fig. 5.5(a). Following are the observations:

a) From 0 to 2ns, write ‘1’ operation is performed. To perform write ‘1’ operation, the bitline WBL remains at Vdd, while WBLB is discharged to ground. The signals WWL, WL_Y1 and RGND are asserted HIGH while, the control signals WL_Y2 and RWL are asserted LOW. Due to such signal configuration, the content of

internal node Q is changed to logic '1', while, internal node QB is changed to logic '0'.

b) From 2ns to 4ns, the store operation is performed. The signals RWL, RGND, WL_Y1 and WL_Y2 are asserted HIGH, while, the signal WWL is asserted LOW. The store operation takes place in set and reset phases. In set phase, the RBL line remains at Vdd therefore, memristor remains in its initial state. Subsequently, RBL is discharged in reset phase. However, memristor retains its state.

c) The power down takes place from 4ns to 6ns. The supply voltage is turned off and the control signals are asserted LOW. The internal nodes lose their data, while memristor M1 maintains its HRS state.

d) After power down, the restore operation is performed from 6ns to 8ns. First, SR0 phase takes place by performing write '0' operation. For this, WWL signals is asserted HIGH and WBL is discharged to ground. It is followed by MDR phase. The control signals RWL, RGND, WL_Y1 and WL_Y2 are asserted HIGH, while, WWL signal is asserted LOW. Due to HRS state of memristor, a low current flow through it which is not sufficient to raise the internal node Q potential and it continues to remain at ground potential i.e., logic '0'. Due to back-to-back connection, internal node QB is charged to Vdd i.e., logic '1'.

Similarly, the timing waveform to execute write – store – power down – restore logic '0' operation is shown in Fig. 5.5(b). First, the write '0' operation is performed by discharging bitline WBL to ground. The control signal WWL, WL_Y2 and RGND are asserted HIGH, while the RWL and WL_Y1 signals are asserted LOW. It changes internal node Q to logic '0' and QB to logic '1'. It is followed by store operation. The data transfer in memristor is done during set phase. The RBL line remains at Vdd. With the assertion of signal RWL, the

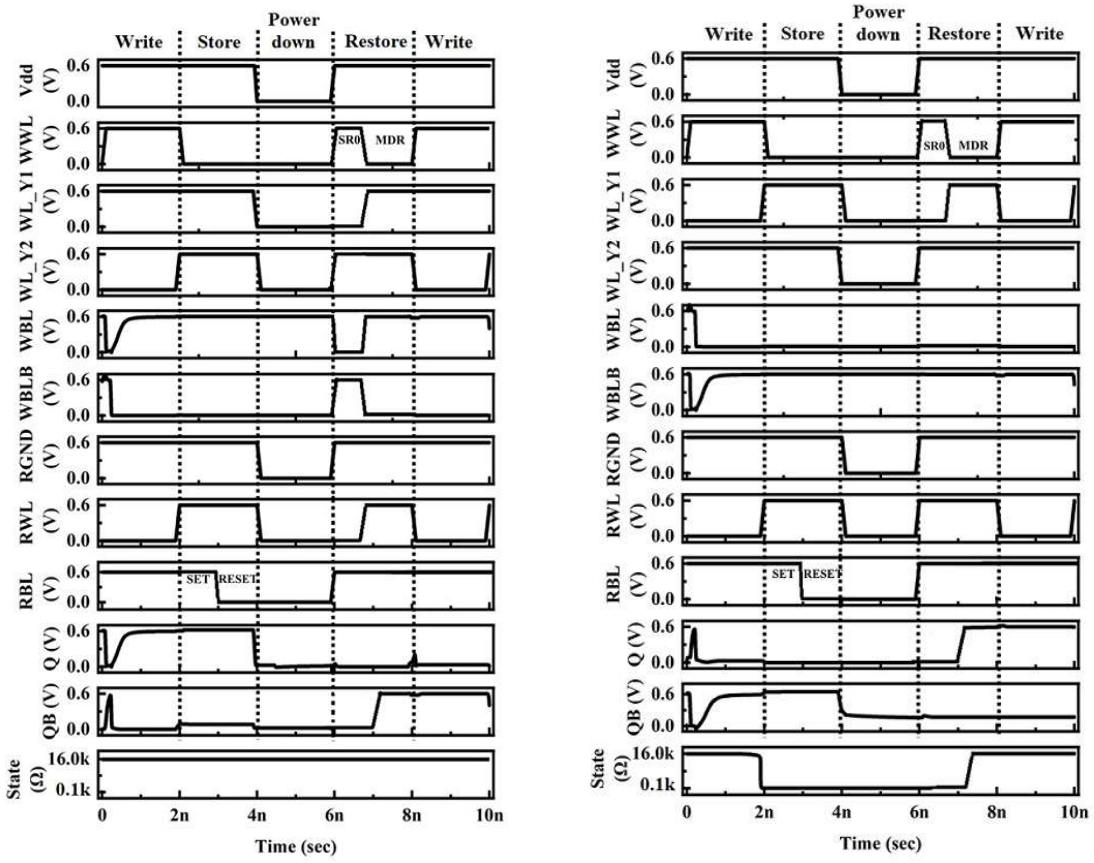
memristor M1 changes its state to LRS. During reset phase, the RBL line is discharged to ground. Due to this, the potential difference across memristor is zero and hence, memristor continues to retain its LRS state.

In power down, the supply voltage is turned off and the control signals are asserted LOW. The internal nodes lose their data, however, memristor M1 maintains its LRS state. In restore operation, first SR0 phases takes place by performing write '0' operation. It is followed by MDR phase wherein, the signal RWL is asserted HIGH and RBL line is charged to Vdd. Due to LRS state of memristor, a large current flow through it and the internal node Q is charged to Vdd i.e., logic '1', while, internal node remains at logic '0'.

From Fig. 5.5(a) and (b), it is observed that the opposite data is recovered at the internal nodes after completion of restore mode. Hence, with the help of additional inverter, the original data can be retrieved.

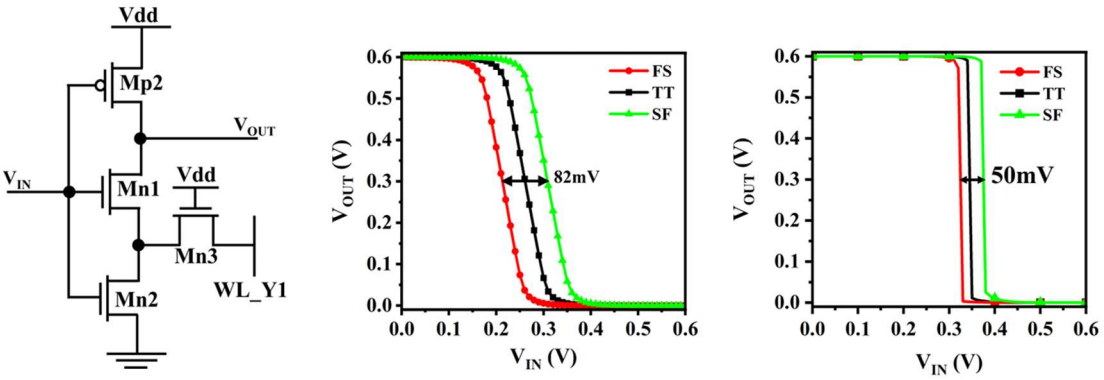
Process variation analysis

To examine the effect of process variation on proposed nvSRAM cell, the switching threshold voltages of ST inverter and CMOS inverter are studied. The schematic of ST inverter used in Proposed design 5 is shown in Fig. 5.6(a), and the VTC for both CMOS and ST inverters is depicted in Fig. 5.6(b) and (c), respectively at TT corner and skewed corners i.e., FS and SF. The worst case spread in switching threshold voltage is found to be 50 mV in case of ST inverter while for CMOS inverter, the value is observed as 82 mV. It may be inferred that there is significant improvement in variation of switching threshold voltage.



(a) (b)

Fig. 5.5. Timing waveform for non-volatile operation of Proposed design 5 for (a) Logic '1' and (b) Logic '0



(a) (b) (c)

Fig. 5.6. Schematic of ST inverter, VTC of (b) CMOS inverter and (c) ST Inverter at TT and skewed corners

Performance analysis

In this sub-section, the performance of Proposed design 5 is compared with RD 8T1R cell [40], MS 7T1R [41], Proposed design 2 and Proposed design 4 at Vdd = 0.6V. Various performance parameters such as margin, delay and power consumption are evaluated for write, read, hold, store and restore operations. The effect of variation in supply voltage Vdd is also studied for completeness.

- Write Performance Analysis

  The write performance of Proposed design 5 and considered RD nvSRAM cell is evaluated in terms of WM, write delay and write power consumption.

  Write margin (WM): The WM of Proposed design 5 and considered RD nvSRAM cells is observed at Vdd = 0.6V. The corresponding WM values are found as 306mV, 286mV, 320mV, 330mV and 365mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. The Proposed design 5 shows 16.16%, 21.64%, 12.33% and 9.59% improvement in WM in comparison to RD 8T1R cell [40], MS 7T1R [41], Proposed design 2 and Proposed design 4, respectively. The feedback transistor Mn6/Mn8 increases the threshold voltage of transistor Mn1/Mn2 which reduces the driving capability of pull-down path. It results in increased WM of the Proposed design 5.

  Write delay: The variation in write delay of Proposed design 5 and considered RD nvSRAM cells is observed at Vdd = 0.6V. The values for write delay is found as 92.64ps, 102.08ps, 113.65ps, 74.46ps and 85.64ps are found for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. The write delay of Proposed design 5 is reduced by 7.55%, 16.1% and

24.64% in comparison to RD 8T1R cell [40], MS 7T1R [41] and Proposed design 2, respectively. The reduction in driving capability of pull-down path and existence of additional path through feedback transistor supports charging and discharging, respectively, of internal nodes which reduces the write delay of proposed cell. The Proposed design 4 shows improved write delay by 13.05% in comparison to Proposed design 5. It is due to the presence of transmission gate to access the data from bitline.

Write power consumption: The write power consumption for Proposed design 5 and considered RD nvSRAM cells is also studied at Vdd = 0.6V. The corresponding values are found as 60.56µW, 0.55µW, 0.35µW, 0.95µW and 85.23µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. It is observed that the write power consumption of Proposed design 5 is increased by 26.85%, 97.95%, 98.55% and 98.16% in comparison to RD 8T1R cell [40], MS 7T1R [41], Proposed design 2 and Proposed design 4, respectively. The use of single bitline to perform the write operation in MS 7T1R [41], Proposed design 2 and Proposed design 4 reduce the power consumption to an extent. The RD 8T1R cell [40] performs differential write operation and need less write current leading to reduced write power consumption in comparison to Proposed design 5.

The supply voltage variation study is also carried out to analyse the write performance of Proposed design 5 and considered RD nvSRAM cells and the results are shown in Fig. 5.7. It is observed that the WM and write power consumption are increased, while, write delay is decreased with increase in supply voltage.

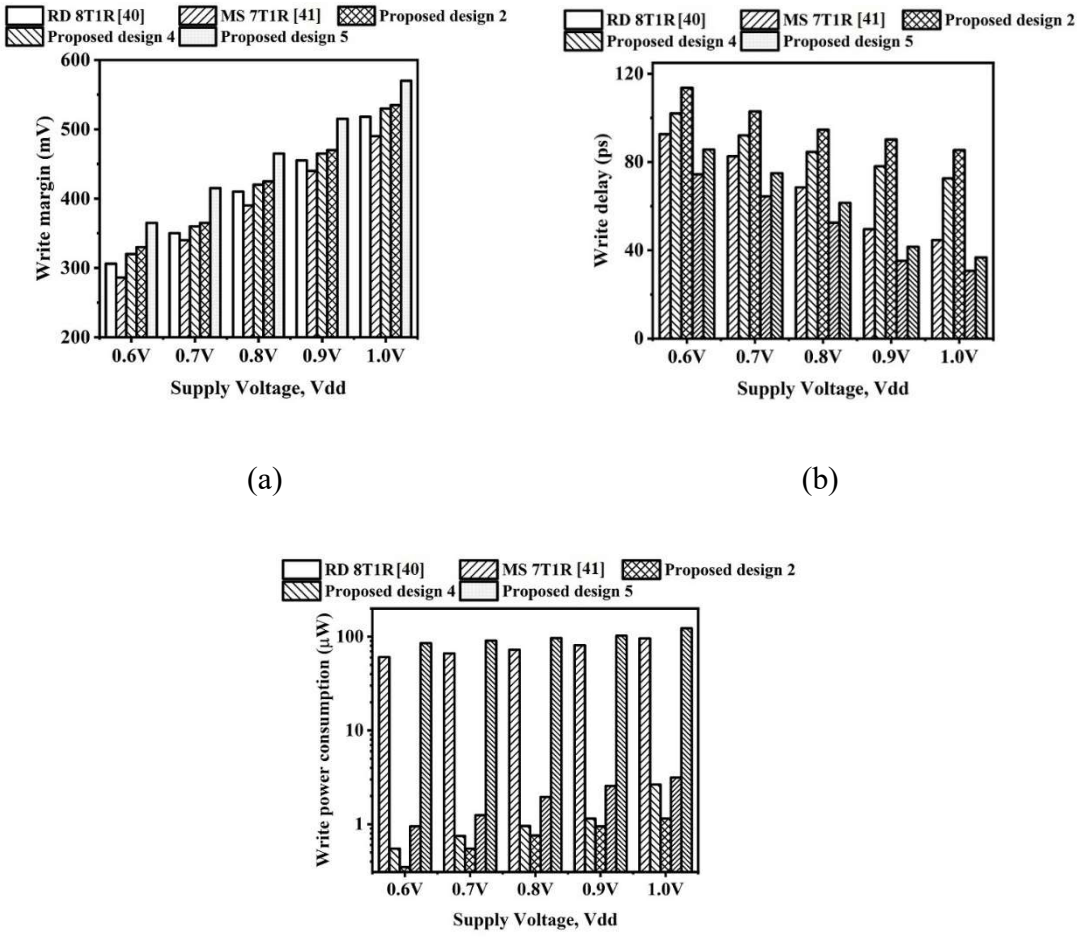


Fig. 5.7. (a) Write margin (b) write delay and (c) write power consumption of Proposed design 5 and considered RD nvSRAM cells at different supply voltages

- Read Performance Analysis

  The read performance of Proposed design 5 and considered RD nvSRAM cells is evaluated in terms of RM, read delay and read power consumption.

  Read margin (RM): The RM of Proposed design 5 and considered RD nvSRAM cells is observed at Vdd =0.6V. The corresponding values are observed as 140mV, 140mV, 130mV, 140mV and 170mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. The maximum

improvement of 23.53% is observed in RM of Proposed design 5 in comparison to considered RD nvSRAM cells. In Proposed design 5, the feedback transistors Mn6 and Mn8 remain on to activate the ST action. It prevents the flipping of internal nodes and improves RM of Proposed design 5.

Read delay: The read delay of Proposed design 5 and considered RD nvSRAM cells is analyzed at Vdd = 0.6V. The read delay values are observed as 98.5ps, 99.1ps, 92.5ps, 100ps and 100.5ps for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. As the read port used in Proposed design 5 and considered RD nvSRAM cells, except for Proposed design 2, is similar, their read delay is same. The Proposed design 2 shows the reduction of 7.96% in read delay in comparison to Proposed design 5.

Read power consumption: The read power consumption of Proposed design 5 and considered RD nvSRAM cells is observed at Vdd = 0.6V. The corresponding values are found as 3.31µW, 3.29µW, 3.51µW, 3.25µW and 3.25µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. It is observed that the read power consumption of Proposed design 5 is similar to RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4. The Proposed design 2 shows the increment of 7.41% in read power consumption in comparison to Proposed design 5.

The read performance of Proposed design 5 and considered RD nvSRAM cells is analysed for different supply voltages also and the results are shown in Fig. 5.8. It is observed that the RM and read power consumption are increased, while read delay is decreased with increase in supply voltage.

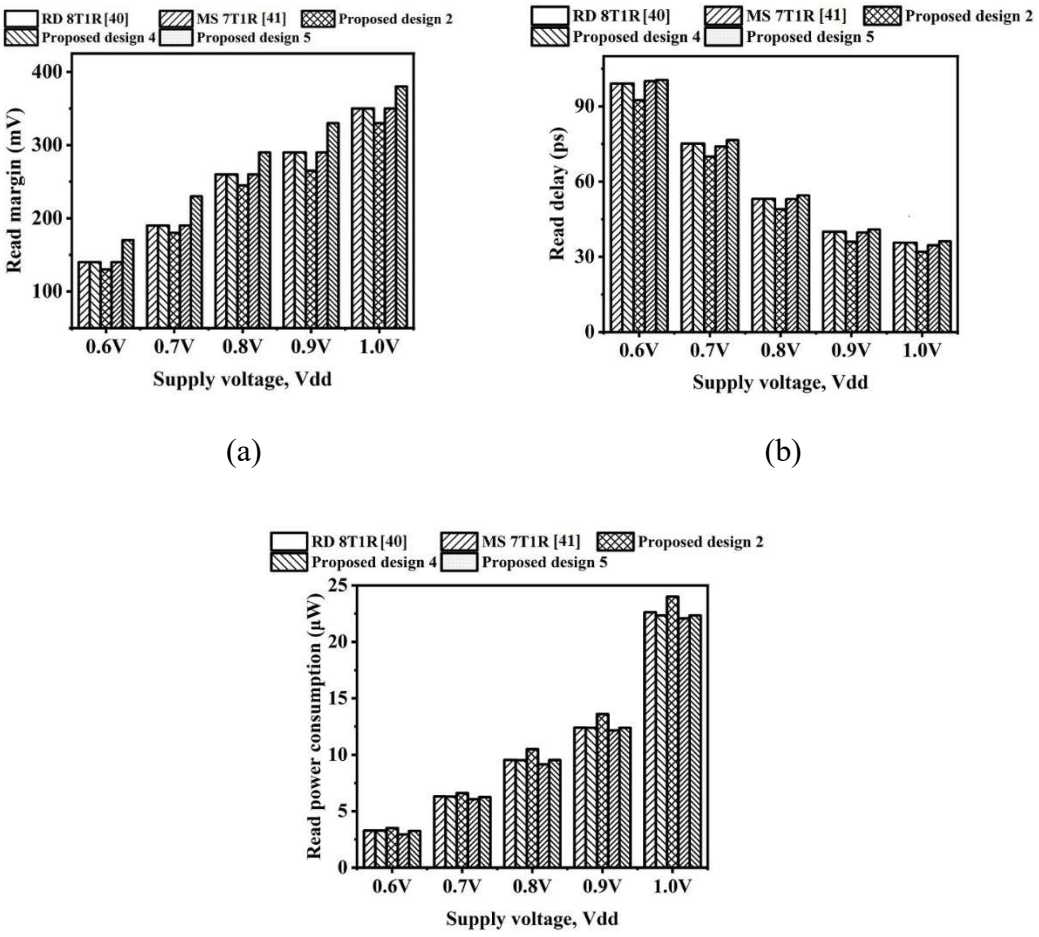


Fig. 5.8. (a) Read margin (b) read delay and (c) read power consumption of Proposed design 5 and considered RD nvSRAM cells at different supply voltages

- Hold Performance Analysis

The hold performance of Proposed design 5 is evaluated in terms of HM and leakage power consumption. The results are compared with considered RD nvSRAM cells.

Hold margin (HM): The HM of Proposed design 5 and considered RD nvSRAM cells is evaluated at Vdd = 0.6V. The HMs are obtained as 150mV, 150mV, 130mV, 150mV and 170mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. The HM of Proposed design 5 shows an

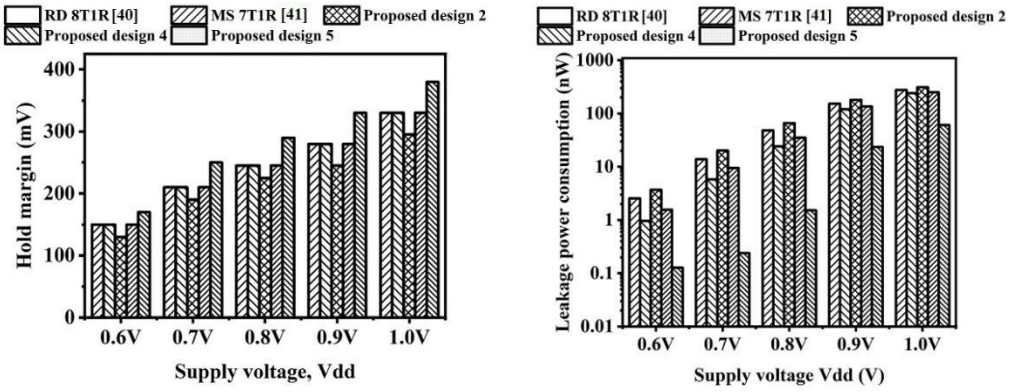
improvement of 11.76% and 23.53% in comparison to (RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4) and Proposed design 2, respectively. In Proposed design 5, the ST action due to feedback transistors along with stacking effect of pull-down transistors prevents the flipping of internal node data during hold operation and improves HM.

Leakage power consumption: The leakage power consumption of Proposed design 5 and considered RD nvSRAM cells is analysed at Vdd = 0.6V. The results are obtained as 2.56nW, 0.96nW, 3.68nW, 1.56nW and 0.138nW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 4 and Proposed design 5, respectively. It is found that leakage power consumption of Proposed design 5 is reduced by 94.59%, 88.76%, 95.56% and 92.15% in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 4, respectively. It is due to the ST action which maintains the stability of Proposed design 5 and reduces leakage power consumption during hold operation in comparison to considered RD nvSRAM cells.

Further, the supply voltage variation study is also carried out to analyse the hold performance of Proposed design 5 and considered RD nvSRAM cells. The results are shown in Fig. 5.9. It is observed that both the HM and leakage power consumption increase with increment in supply voltage.

- Store Performance Analysis

The store performance of Proposed design 5 is evaluated in terms of store delay and store power consumption. The results are compared with considered RD nvSRAM cells at Vdd=0.6V.



(a) (b)

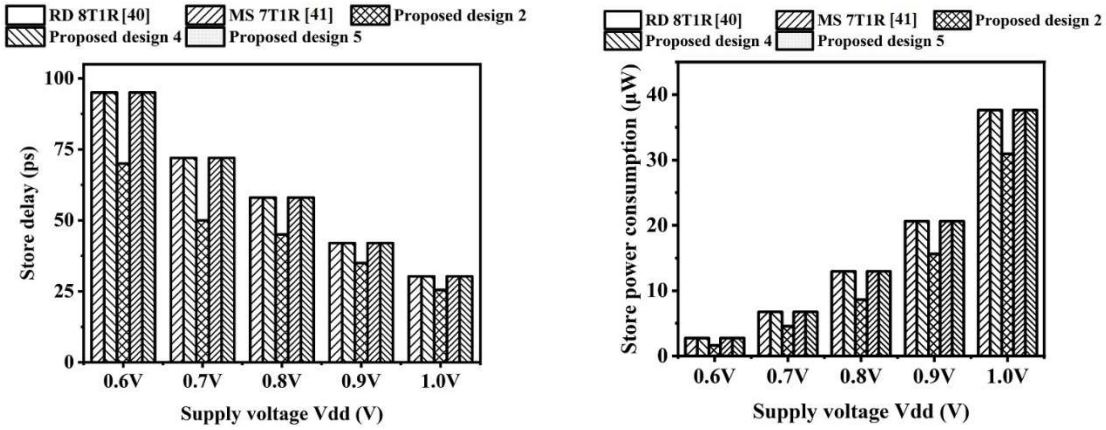
Fig. 5.9. (a) Hold margin and (b) leakage power consumption of Proposed design 5 and considered RD nvSRAM cells at different supply voltages

Store delay: The Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 follow same approach for store operation and, hence, their store delay is similar which is found as 86.25ps at Vdd = 0.6V. For Proposed design 2, the store delay is found as 72.5ps. In Proposed design 5, the set and reset phases are required to perform store operation that leads to increase in store delay by 15.65% in comparison to Proposed design 2.

Store power consumption: The store power consumption for Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 is similar due to their similar store operation and it is found to be 2.15µW at Vdd = 0.6V. For Proposed design 2, the store power consumption is found as 1.65µW. In Proposed design 5, the bitline RBL need to discharge for performing store operation and it causes increase in store power consumption by 18.18% in comparison to Proposed design 2.

The supply voltage variation study is also carried out to analyse the store performance of Proposed design 5 and considered RD nvSRAM cells and the results are shown in Fig. 5.10.

With increase in supply voltage, store delay decreases whereas store power consumption shows an increasing trend.



(a) (b)

Fig. 5.10. (a) Store delay and (b) store power consumption of Proposed design 5 and considered RD nvSRAM cells at different supply voltages

- Restore Performance Analysis

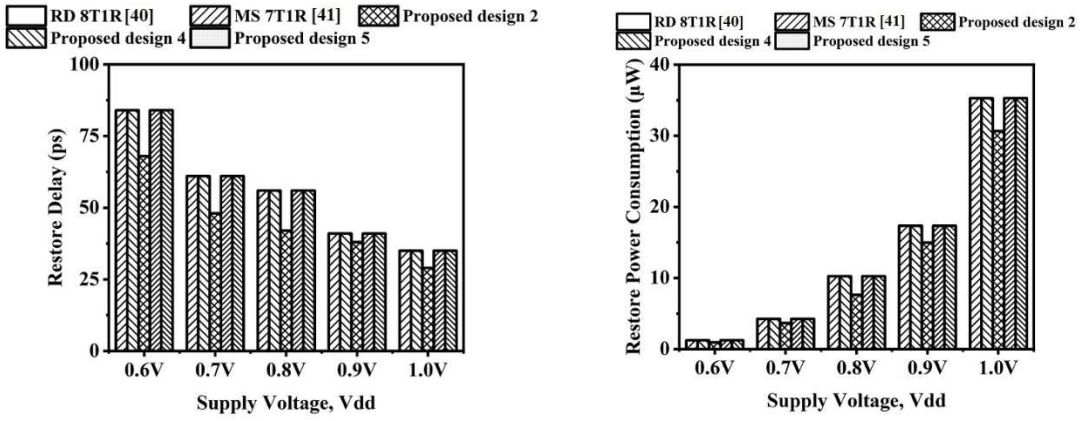
  The restore performance of Proposed design 5 is evaluated in terms of restore delay and restore power consumption. The results are compared with considered RD nvSRAM cells at Vdd = 0.6V.

  Restore delay: The restore delay of Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 is similar as they follow same method to recover the data. The value is found to be 80.05ps at Vdd = 0.6V. The restore delay for Proposed design 2 is found as 68.4ps. Hence, the reduction of 14.5% is observed in restore delay value of Proposed design 2 in comparison to Proposed design 5.

  Restore power consumption: It is found that the restore power consumed by Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 is 1.25µW at Vdd = 0.6V, while for Proposed design 2, it is 0.95µW. It is observed that the restore

power consumption of Proposed design 2 is reduced by 24% in comparison to Proposed design 5.

The supply voltage variation study is also performed to analyze restore performance of Proposed design 5 and considered RD nvSRAM cells and the results are shown in Fig. 5.11. The decreasing trend in restore delay, while increasing trend in restore power consumption is observed with increment in supply voltage.



(a) (b)

Fig. 5.11. (a) Restore delay and (b) restore power consumption of Proposed design 5 and considered RD nvSRAM cells at different supply voltages

5.3. Proposed design 6

The Proposed design 6 consists of two ST inverters connected back-to-back and formed by Inverter 1: Mp1-Mn1-Mn5-Mn6 and Inverter 2: Mp2-Mn2-Mn7-Mn8 as shown in Fig. 5.12. The feedback transistors Mn6 and Mn8 are responsible for the ST action in the Proposed design 6. The data to be written is loaded on bitlines WBL/WBLB and is stored on internal nodes through write access transistor Mn3 and Mn4 controlled by write wordline (WWL) signal. The read port has two stacked transistors T1 and T2 controlled by read wordline (RWL) signal and internal node QB, respectively, to perform read operation through bitline

RBL. The column-based signals WL_Y1 and WL_Y2 are used to control the ST action. The ST action makes the Proposed design 6 tolerable against process variations during write, read, hold, store and restore operations. It improves the write performance by enhancing the WM. It also increases the cell stability during read and hold operations. The pass transistor MR1 and memristor M1 are used to perform non-volatile operation via control signals CTL1 and CTL2.

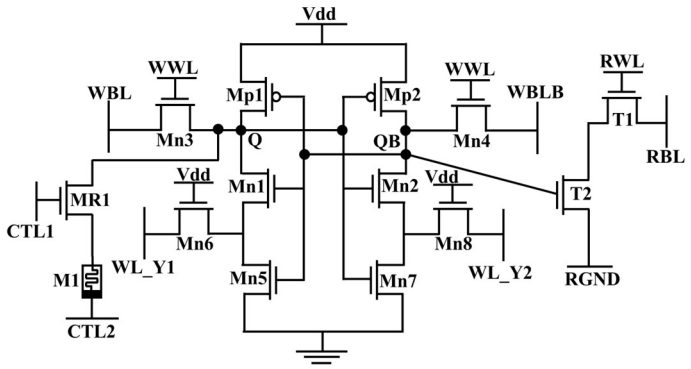


Fig. 5.12. Schematic of Proposed design 6

Table 5.2. Operation condition of Proposed design 6

Signals	**Operations**					
	Write '1'	**Write '0'**	**Read**	**Hold**	**Store**	**Restore**
WWL	HIGH	HIGH	LOW	LOW	LOW	LOW
WL_Y1	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
WL_Y2	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
RWL	LOW	LOW	HIGH	LOW	LOW	LOW
RGND	HIGH	HIGH	LOW	HIGH	HIGH	HIGH
CTL1	LOW	LOW	LOW	LOW	HIGH	HIGH
CTL2	LOW	LOW	LOW	LOW	LOW	HIGH

5.3.1. Operation of Proposed design 6

In this subsection, the operation of Proposed design 6 is described during write, read, hold, store and restore operations. The status of control signals during each operation is enlisted in Table 5.2.

Write operation

The bitlines WBL and WBLB are pre-charged to Vdd prior to write operation. The write '1' operation is performed by discharging WBLB to ground, while WBL remains at Vdd. The write '1' operation is elucidated in Fig. 5.13. The control signals are asserted as mentioned in Table 5.2. With the assertion of WL_Y1 signal, the ST action of feedback transistor Mn6 is activated. It increases threshold voltage of transistor Mn1 and degrades the driving capability of pull-down path. It supports the charging of node Q. Another signal WL_Y2 is asserted LOW, leading to formation of two discharge paths: one through write access transistor Mn4 and another path through feedback transistor Mn8. It facilitates faster discharging of internal node QB. Similarly, during write '0' operation, WBLB remains at Vdd while WBL is discharged to ground. The signals WL_Y1 and WL_Y2 are asserted LOW and HIGH, respectively. With assertion of WWL signal, the node Q is discharged to ground through write access transistor Mn3 and feedback transistor Mn6. On the other side, node QB is pulled up to Vdd which is favored by increased threshold of transistor Mn2 due to feedback transistor Mn8. The reduced driving capability of pull-down path also supports the charging of internal node QB. Hence, due to the presence of ST action, the WM of Proposed design 6 is improved.

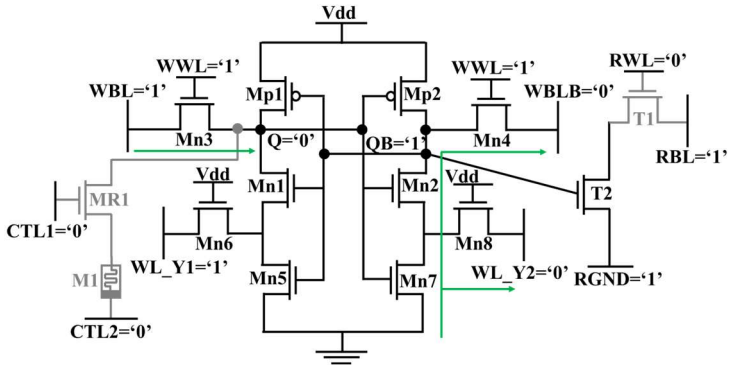


Fig. 5.13. Proposed design 6 during write operation

Read operation

The read bitline RBL is pre-charged to Vdd before read operation. The control signals are asserted as mentioned in Table 5.2. During read '1' operation, RBL does not get a discharging path through read port transistors T1 and T2 as internal node QB is at logic '0' which turns off the transistor T2 and bitline RBL remains at Vdd. For read '0' operation, the bitline RBL discharges as the internal node QB is at logic '1', it turns on transistor T2. The schematic for read '0' operation is shown in Fig. 5.14. The signals WL_Y1 and WL_Y2 remain HIGH during read operation which activates the ST action in Proposed design 6 and increases the read stability of the cell.

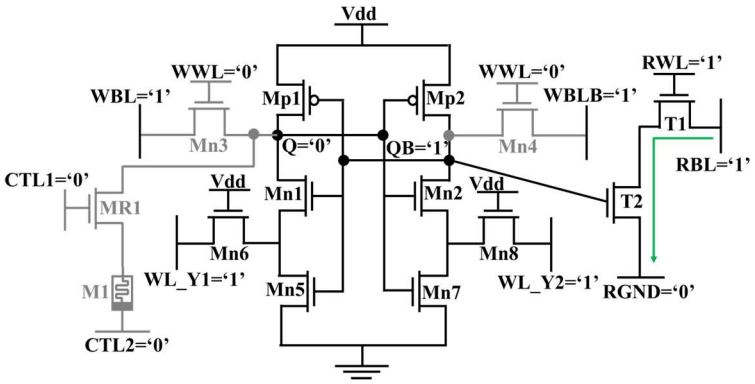


Fig. 5.14. Proposed design 6 during read operation

Hold operation

The status of control signals during hold operation are given in Table 5.2 and the schematic of Proposed design 6 during hold operation is shown in Fig. 5.15. Any changes due to process variation at internal nodes of the proposed design are resisted by ST action of feedback transistors Mn6/Mn8 and stack of pull-down transistors (Mn1, Mn5) and (Mn2, Mn7). The feedback transistors Mn6 and Mn8 remain activated due to Vdd potential at their gate terminal. The control signals WL_Y1 and WL_Y2 also remain HIGH during hold operation. It increases the threshold volage of transistor Mn1 and Mn2 and reduces the flow of current during hold mode. The stacking of pull-down transistors further reduces the flow of current. Hence, it reduces leakage in the proposed design and increases the stability during hold operation.

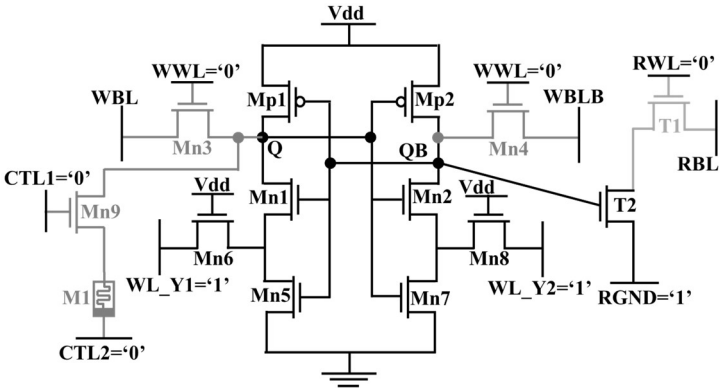


Fig. 5.15. Proposed design 6 during hold operation

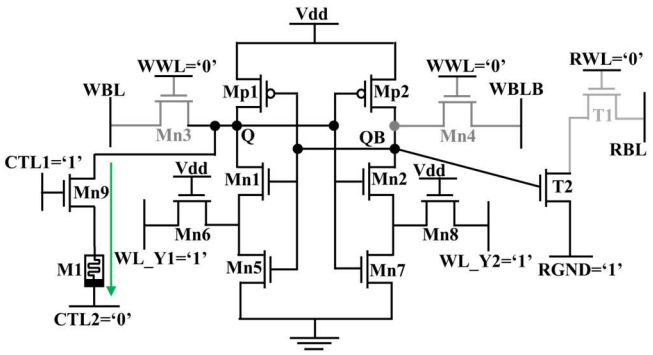
Non-volatile operation

The non-volatile operation consists of store, power-down and restore operations. The status of control signals during different operations is given in Table 5.2 and the schematic of Proposed design 6 during store and restore operations is shown in Fig. 5.16. Prior to store

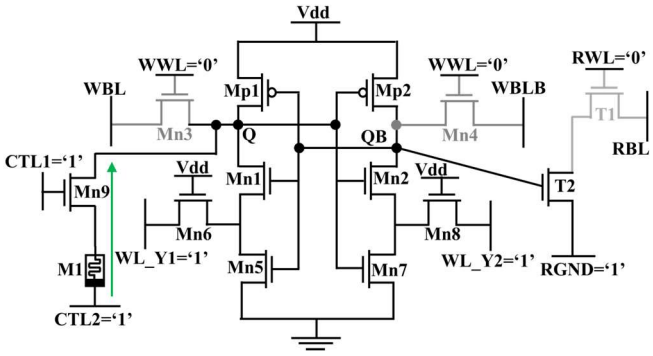
operation, write operation takes place. It is required to mention here that memristor remains in its initial HRS state irrespective of internal node content.

The signal configuration for store operation mentioned in Table 5.2 turns on transistor MR1 connecting memristor M1 to internal node Q. If logic '1' is stored at internal node Q, both the terminals of memristor are at different potential which generate a potential difference across memristor. It changes memristor state from HRS to LRS representing logic '1' is stored in the memristor. If logic '0' is stored at internal node Q, both the terminals of memristor remain at logic '0', there is no potential drop across the memristor and it remains in HRS state representing logic '0' is stored in it. During power down, all the control signals are asserted LOW and supply voltage is turned off. The stored data at internal node Q and QB is lost, however the memristor retains its state.

In restore operation, the supply voltage is turned on again and the control signals are asserted as mentioned in Table 5.2. If memristor M1 is in LRS state, a large current flow through it which is sufficient to raise the potential of internal node Q to Vdd and due to the back-to-back connection of ST inverters, the internal node QB remain at logic '0'. If memristor is in HRS state, a low current flows through the memristor which is not enough to raise the potential of internal node Q and it remains at logic '0'. After completion of restore operation, memristor state is changes to HRS which is its initial state also. During store operation, the ST action increases the cell stability so that the correct data is stored in memristor. During restore operation, the ST action helps in recovery of internal node data as it was before power down.



(a)



(b)

Fig. 5.16. Proposed design 6 during (a) store and (b) restore operation

5.3.2. Simulation results and discussion

The SPICE simulations are carried out using 32nm PTM model to analyse the performance of Proposed design 6. The memristor model suggested in [55] is used to observe the non-volatile performance. In this section, first the timing waveform for non-volatile operation of Proposed design 6 is discussed at Vdd = 0.6V. It is followed by the performance evaluation during different operations such as write, read, hold, store and restore. The results are compared with the RD 8T1R cell [40], MS 7T1R [41], Proposed design 2, Proposed design 4 and Proposed design 5. For the sake of fair comparison, the aspect ratios (W/L) of different transistors of considered RD nvSRAM cells and Proposed design 6 are taken as 72nm/36nm.

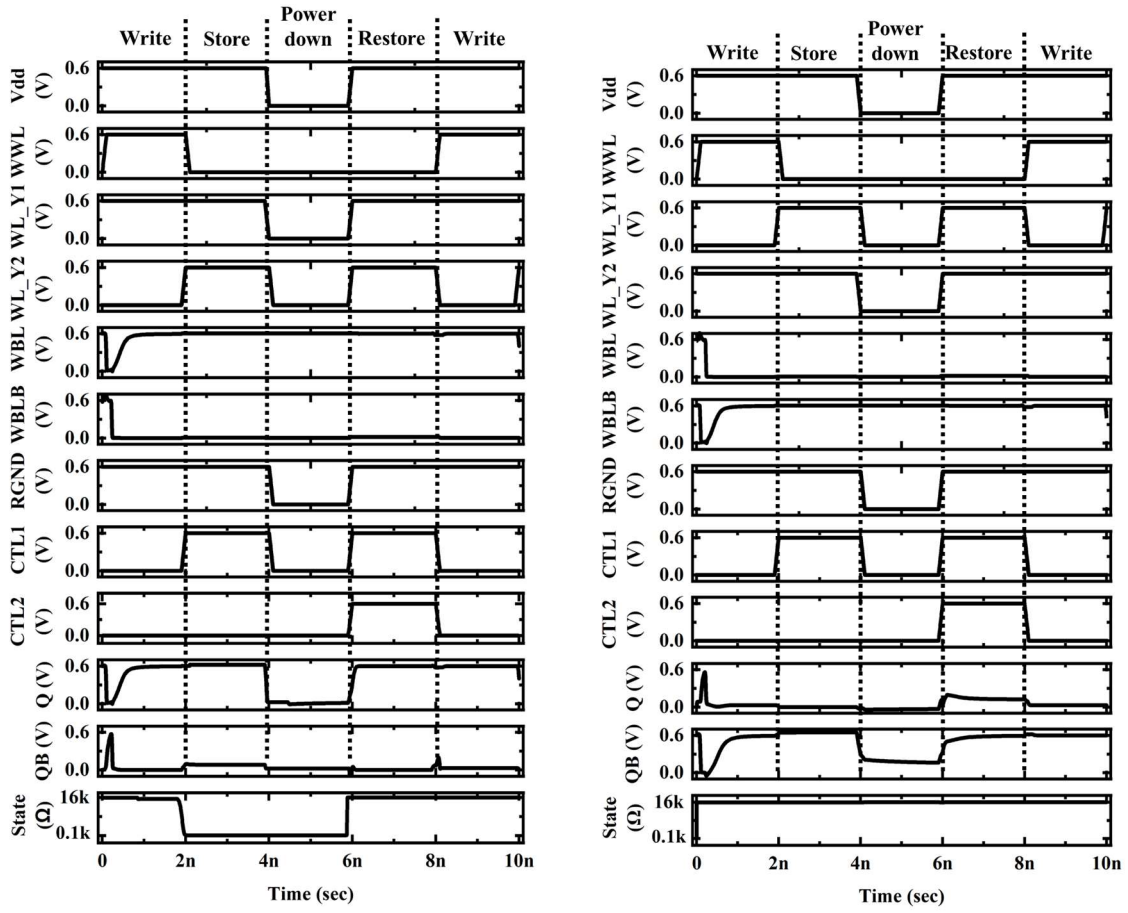
Timing waveform

The execution of store, power down and restore operations for logic '1' is shown in Fig. 5.17(a). The time duration for each operation is taken more than twice of time required to change memristor state [32]. The following observations are made from Fig. 5.17(a):

a) Initially, the write '1' operation takes place from 0 to 2ns. The pre-charged bitline WBL remain at Vdd, while WBLB is discharged to ground. With the assertion of signals WWL and WL_Y1, the internal node Q changes its content to logic '1'.
b) The store operation takes place from 2ns to 4ns. With the assertion of signal CTL1, the transistor MR1 turns on, connecting internal node Q to memristor M1. As internal node Q is at logic '1' and signal CTL2 is at logic '0', a potential difference is developed across memristor M1 due to which it changes its state from HRS to LRS.
c) During power down from 4ns to 6ns, the supply voltage is turned off and the control signals are asserted LOW. The internal nodes lose their data, however, memristor M1 retains its LRS state.
d) From 6ns to 8ns, the restore operation takes place. The supply voltage is turned on again and the control signals CTL1 and CTL2 are asserted HIGH. Due to the LRS state of memristor, a large current flow through it which is enough to raise the potential of internal node Q to Vdd i.e., logic '1'. After restore operation memristor changes its state to initial HRS state.

Similarly, the non-volatile operation for logic '0' is shown in Fig. 5.17(b). First, write '0' operation takes place by discharging WBL to ground, while, WBLB remain at Vdd. With the assertion of signals WWL and WL_Y2, the internal node Q is discharged to ground i.e., logic

'0', while internal node QB is charged to Vdd i.e., logic '1'. During store operation, the potential difference across memristor is zero as both internal node Q and signal CTL2 are at ground potential. Due to this, memristor remains in HRS state. After this, the supply voltage is turned off. The internal nodes lose their data, however, memristor retains its HRS state. During restore operation, the supply voltage is turned on again and control signals CTL1 and CTL2 are HIGH. As memristor is in HRS, a low current flow through it which is not sufficient to raise the potential of internal node Q to Vdd and it remain at logic '0'. After restore operation, memristor continues to remain its HRS state.



(a) (b)

Fig. 5.17. Timing waveform for non-volatile operation of Proposed design 6 for (a) Logic '1' and (b) Logic '0

Performance analysis

In this sub-section, the performance of Proposed design 6 is compared with RD 8T1R cell [40], MS 7T1R [41], Proposed design 2, Proposed design 3, Proposed design 4 and Proposed design 5 at Vdd = 0.6V. Various performance parameters such as delay, margin and power consumption are evaluated for write, read, hold, store and restore operations. The effect of variation in supply voltage Vdd is also studied for completeness.

- Write performance analysis

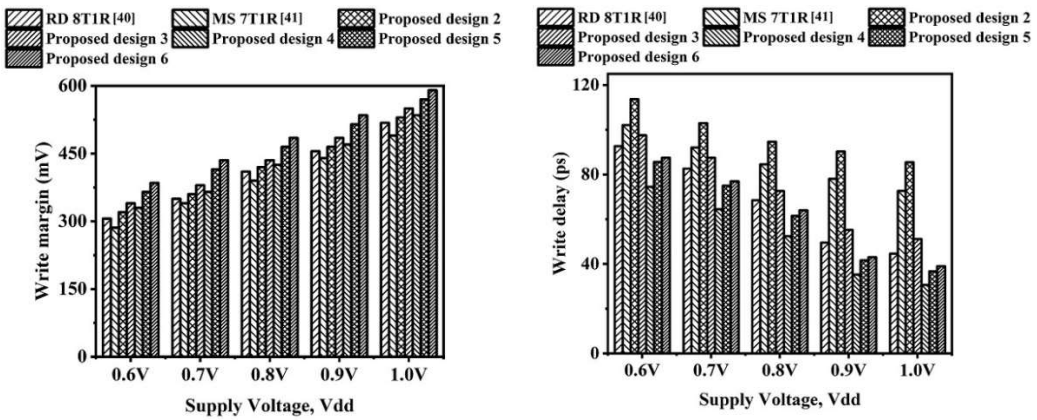
  The write performance of Proposed design 6 and considered RD nvSRAM cell is evaluated in terms of WM, write delay and write power consumption.

  Write margin (WM): The WM of Proposed design 6 and considered RD nvSRAM cells is analyzed at Vdd = 0.6V. The corresponding values are found as 306mV, 286mV, 320mV, 340mV, 330mV, 365mv and 385mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. The improvement of 20.52%, 25.71%, 16.88%, 11.68%, 14.28% and 5.19% is observed in WM of Proposed design 6 in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4 and Proposed design 5, respectively. The ST action in Proposed design 6 increases the threshold voltage of transistor Mn1/Mn2 and hence, reduces the driving capability of pull-down path. Also, it avoids the direct connection of memristor to internal nodes that improves WM of Proposed design 6 in comparison to Proposed design 5.

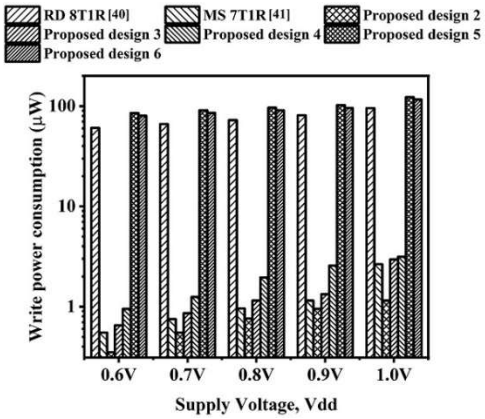
  Write delay: The write delay of Proposed design 6 and considered RD nvSRAM cells is calculated at Vdd = 0.6V. The following values 92.64ps, 102.08ps, 113.65ps,

97.52ps, 74.46ps, 85.64ps and 87.5ps are found for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. The write delay of Proposed design 6 is reduced by 6.62%, 15.26%, 23.89% and 11.3% in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2 and Proposed design 3, respectively, while, it is increased by 14.9% and 2.12% in comparison to Proposed design 4 and Proposed design 5, respectively.

Write power consumption: The write power consumption for Proposed design 6 and considered RD nvSRAM cells is studied at Vdd = 0.6V. The corresponding values are found as 60.56µW, 0.55µW, 0.35µW, 0.65µW, 0.95µW, 85.23µW and 80.25µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. The write power consumption of Proposed design 6 is increased by 24.53%, 99.32%, 99.56%, 99.19% and 98.81% in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3 and Proposed design 4, respectively, while it is reduced by 5.84% in comparison to Proposed design 5.



(a) (b)



(c)

Fig. 5.18. (a) Write margin (b) write delay and (c) write power consumption of Proposed design 6 and considered RD nvSRAM cells at different supply voltages

The supply voltage variation study is also carried out to analyse the performance of Proposed design 6 and considered RD nvSRAM cells and the results are shown in Fig. 5.18. An increasing trend in WM and write power consumption, while, decreasing trend in write delay is observed with an increase in supply voltage for all the RD nvSRAM cells.

- Read Performance Analysis

  The read performance of Proposed design 6 and considered RD nvSRAM cell is evaluated in terms of RM, read delay and read power consumption.

  Read margin (RM): The RM of Proposed design 6 and considered RD nvSRAM cells is analyzed at Vdd = 0.6V. The corresponding values are observed as 140mV, 140mV, 130mV, 150mV, 140mV, 170mV and 180mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. The increment of 22.22%, 22.22%, 27.78%, 16.67%, 22.22% and 5.56% is observed in RM of Proposed design 6 in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design

4 and Proposed design 5, respectively. The ST action in Proposed design 6 maintains RM. Also, the isolation of memristor through internal nodes further enhances RM of proposed deign 6.

Read delay: The read delay of Proposed design 6 and considered RD nvSRAM cells is analyzed at Vdd = 0.6V. The values are observed as 98.5ps, 99.1ps, 92.5ps, 92.1ps, 100.5ps, 100.5 and 102.5ps for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. As the read port used in Proposed design 6 and considered RD nvSRAM cells, except for Proposed design 2 and Proposed design 3, is similar, their read delay is same. The Proposed design 2 and Proposed design 3 shows the reduction of 10.15% in read delay in comparison to Proposed design 6.

Read power consumption: The read power consumption of Proposed design 6 and considered RD nvSRAM cells is observed at Vdd = 0.6V. The corresponding values are found as 3.31µW, 3.29µW, 3.51µW, 3.52µW, 3.25µW, 3.25µW and 3.15µW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. It is observed that the read power consumption of Proposed design 6 is similar to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5. The Proposed design 2 and Proposed design 3 shows the increment of 10.52% in read power consumption in comparison to Proposed design 6.

The supply voltage variation study is also carried out to study read performance of Proposed design 6 and considered RD nvSRAM cells and the results are shown in Fig. 5.19. The

upward trend in RM and read power consumption, while, downward trend in read delay is observed with respect to increase in supply voltage for all the RD nvSRAM cells.

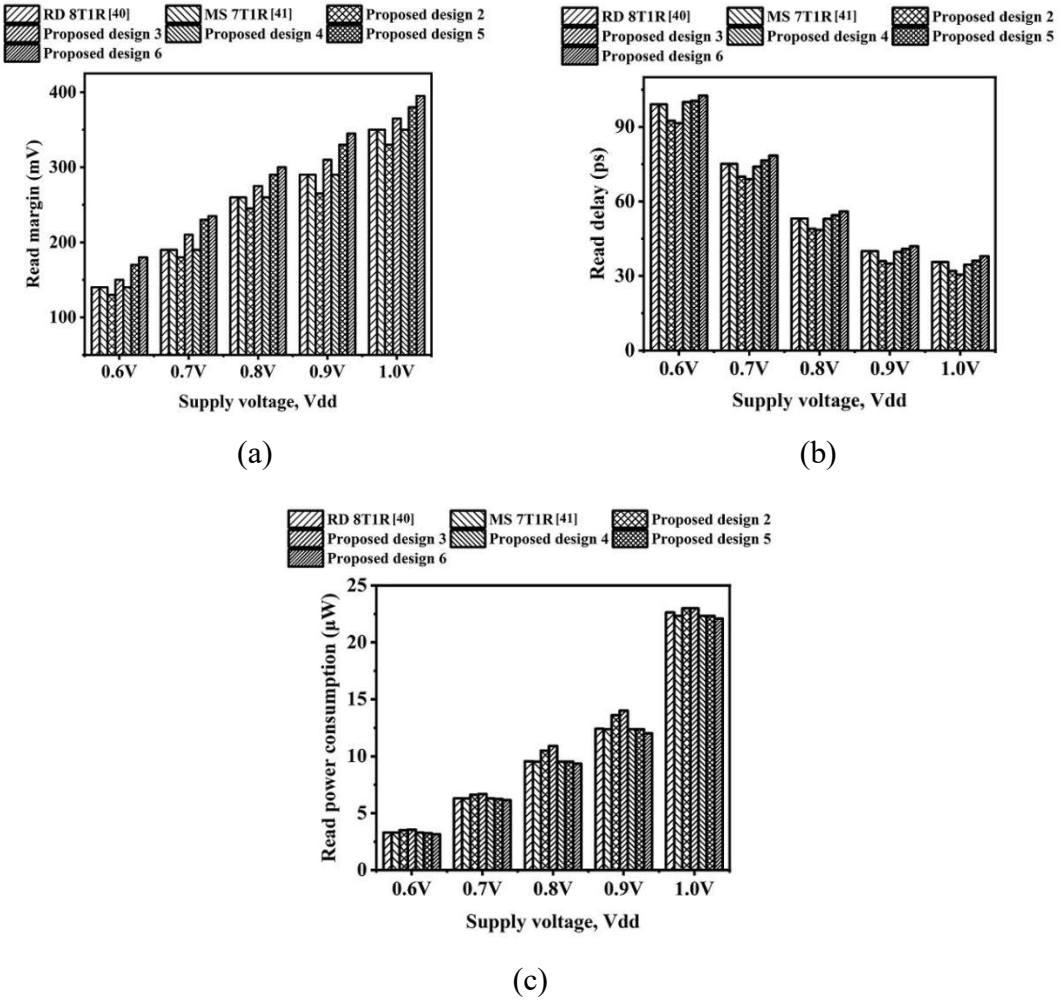


Fig. 5.19.(a) Read margin (b) read delay and (c) read power consumption of Proposed design 6 and considered RD nvSRAM cells at different supply voltages

- Hold Performance Analysis

  The hold performance of Proposed design 6 and considered RD nvSRAM cell is evaluated in terms of margin, write delay and write power consumption.

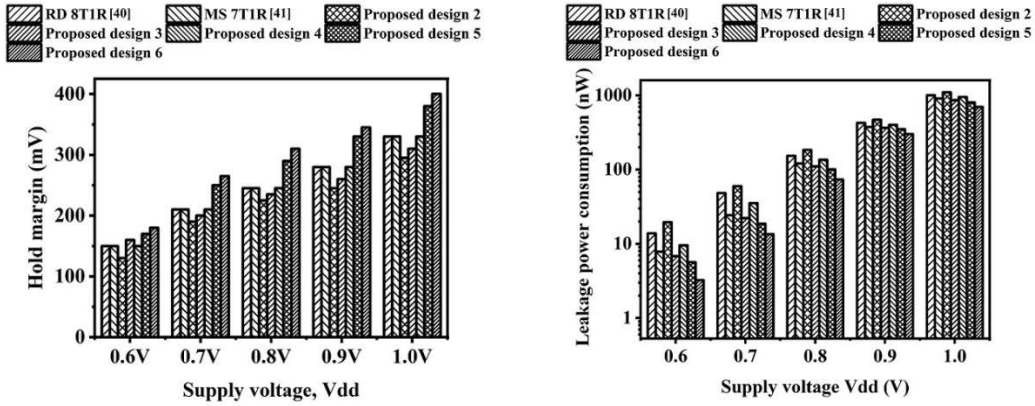
  Hold margin (HM): The HM of Proposed design 6 and considered RD nvSRAM cells is evaluated at Vdd = 0.6V. The results are obtained as 150mV, 150mV, 130mV,

160mV, 150mV, 170mV and 180mV for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively. The HM of Proposed design 6 shows an improvement of 16.67%, 27.78%, 11.11% and 5.56% in comparison to (RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4), Proposed design 2, Proposed design 3 and Proposed design 5, respectively. In Proposed design 6, the ST action due to feedback transistors along with stacking effect of pull-down transistors prevent flipping of internal node data during hold operation. Also, the isolation of memristor from internal nodes improve HM.

Leakage power consumption: The leakage power consumption in hold mode is an important component of total power consumption. The corresponding values are found as 2.56nW, 0.96nW, 3.68nW, 0.88nW, 1.56nW, 0.138nW and 0.115nW for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 2, Proposed design 3, Proposed design 4, Proposed design 5 and Proposed design 6, respectively, at Vdd= 0.6V. Hence, the leakage power consumption of Proposed design 6 is reduced by 95.51%, 88.02%, 96.87%, 86.93%, 92.63% and 16.67% in comparison to RD 8T1R [40], MS 7T1R [41], Proposed design 2, Proposed design 3, Proposed design 4 and Proposed design 5, respectively. In Proposed design 6, the ST action helps in reducing leakage power consumption, also it avoids direct connection between memristor and internal nodes which exist in to RD 8T1R [40], MS 7T1R [41], Proposed design 4 and Proposed design 5.

The supply voltage variation study is also carried out to observe hold performance of Proposed design 6 and considered RD nvSRAM cells and the result is shown in

Fig. 5.20. The increasing trend in HM and leakage power consumption is observed with increase in supply voltage.



(a) (b)

Fig. 5.20. (a) Hold margin and (b) leakage power consumption of Proposed design 6 and considered RD nvSRAM cells at different supply voltage

- Store Performance Analysis

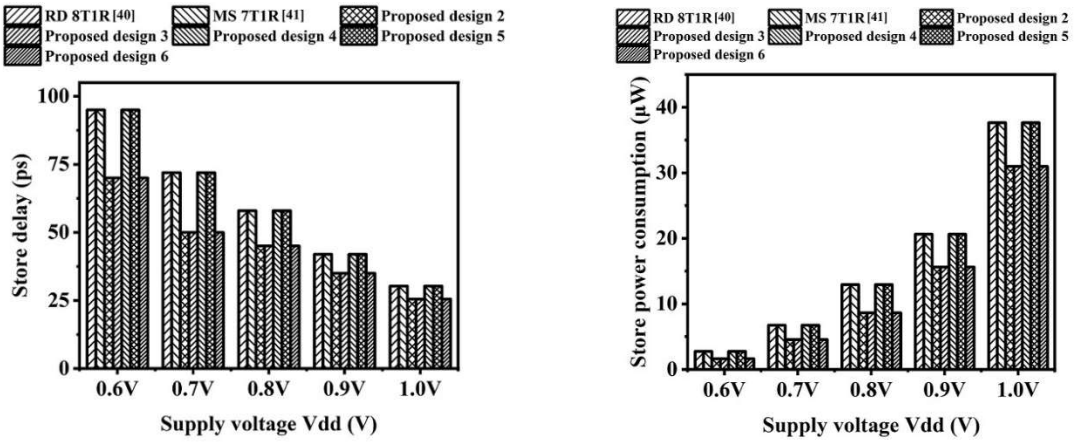
  The store performance of Proposed design 6 and considered RD nvSRAM cell is evaluated in terms of store delay and store power consumption.

  Store delay: The store delay of Proposed design 6, Proposed design 2 and Proposed design 3 is similar as 1T1M structure is used to perform store operation. The store delay value is found as 72.5ps at Vdd = 0.6V. For RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5, the store delay is observed as 86.25ps at same supply voltage. The reduction in store delay of Proposed design 6 is 15.94% in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5.

  Store power consumption: For Proposed design 6, Proposed design 2 and Proposed design 3, the store power consumption is found as 1.65µW at Vdd = 0.6V. The store

power consumption for RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5 is similar due to their similar store operation and it is found to be 2.15µW at same supply voltage. In RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5, the bitline RBL need to discharge for performing store operation and it causes increase in store power consumption by 18.18% in comparison to Proposed design 6.

The supply voltage variation study is also carried out to analyse the store performance of Proposed design 6 and considered RD nvSRAM cells and the results are shown in Fig. 5.21. A decrease in store delay, while an increases in store power consumption is observed with increase in supply voltage.



(a) (b)

Fig. 5.21. (a) Store delay and (b) store power consumption of Proposed design 6 and considered RD nvSRAM cells at different supply voltages

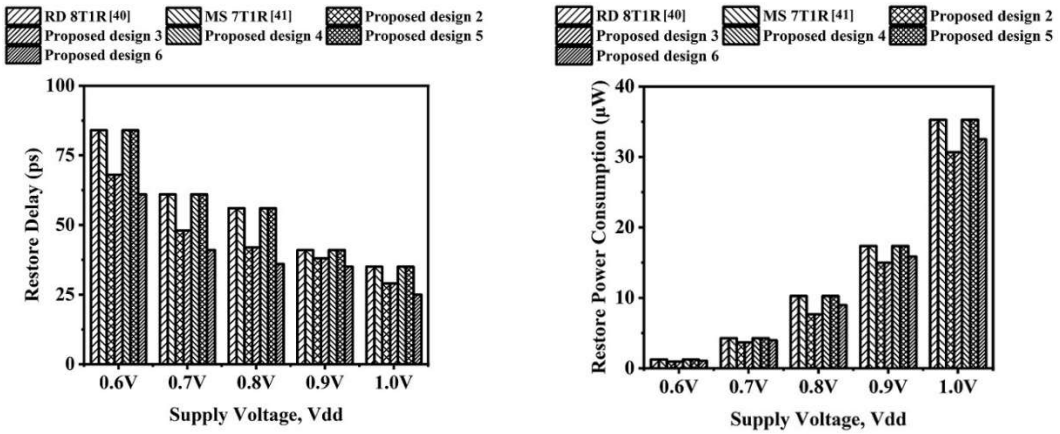
- Restore Performance Analysis

  The restore performance of Proposed design 6 and considered RD nvSRAM cell is evaluated in terms of restore delay and restore power consumption.

Restore delay: The restore delay for Proposed design 6 is found as 62.1ps, while for Proposed design 2 and Proposed design 3, it is examined as 68.4ps at Vdd = 0.6V. The restore delay of Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4 is similar as they follow same method to recover the data. The value is found to be 80.05ps at same supply voltage. Hence, the reduction of 22.42% and 9.21% is observed in restore delay value of Proposed design 6 in comparison to (Proposed design 5, RD 8T1R cell [40], MS 7T1R cell [41] and Proposed design 4) and (Proposed design 2 and Proposed design 3), respectively.

Restore power consumption: The restore power consumption for Proposed design 6 is found as 1.05µW, while for Proposed design 2 and Proposed design 3, it is examined as 0.95µW at Vdd = 0.6V. It is found that the restore power consumed by RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5 is 1.25µW at same supply voltage. It is observed that the restore power consumption of Proposed design 6 is reduced by 16% in comparison to RD 8T1R cell [40], MS 7T1R cell [41], Proposed design 4 and Proposed design 5, while it is increased by 9.52% in comparison to Proposed design 2 and Proposed design 3.

The supply voltage variation study is also done to analyze restore performance of propose design 6 and considered RD nvSRAM cells and the results are shown in Fig. 5.22. The decreasing trend in restore delay, while increasing trend in restore power consumption is observed with increase in supply voltage.



(a) (b)

Fig. 5.22. (a) Restore delay and (b) restore power consumption of Proposed design 6 and considered RD nvSRAM cells at different supply voltages

5.4. Failure Probability Analysis

The process variations influence the margins (WM, RM, HM) and access time (write access, read access, store and restore) due to variations in threshold voltage of transistors. It may cause failure in accomplishing write, read, hold, store and restore operations. The worst-case estimation of write ability, read ability, hold ability etc necessitates a large number of Mote Carlo runs which are computationally prohibitive [70]. An alternate scheme to evaluate the performance is suggested in [71] which facilitates failure probability estimation in only few runs.

For instance, to calculate the write failure probability ($P_{write-failure}$), the write margin (WM) of the cell is calculated using wordline sweep method [47]. The 6σ failure probability at which WM of the cell is 0mV i.e., $P_{write-failure} = 1E-9$, is known as write failure probability and the corresponding supply voltage is known as write Vmin. In this method,

WM is calculated by changing threshold voltage of each transistor one by one. The expression for evaluating write failure probability ($P_{write-failure}$) is given by equation (5.1).

$$P_{write-failure} = \int_{-\infty}^{-(WM_{\mu}/WM_{\sigma})} \frac{1}{\sqrt{2\pi}} e^{\frac{-y^2}{2}} dy \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.1)$$

where, WM_{μ} and WM_{σ} refer to mean and standard deviation calculated over all WMs. Similarly, the read and hold failure probabilities are calculated using read margin (RM) and hold margin (HM), respectively. The RM and HM are estimated by embedding a square in the butterfly curve and the dimension of the square gives the value of RM and HM [46]. The 6σ failure probability at which RM and HM are equal to thermal voltage (kT = 26mV at 300K) i.e., $P_{read-fail} = P_{hold-failure} = 1E-9$, is known as read and hold failure probability and the corresponding supply voltages are known as read Vmin and hold Vmin, respectively. The expression for $P_{read-failure}$ and $P_{hold-failur}$ are given by equation (5.2) and (5.3), respectively.

$$P_{read-failure} = \int_{-\infty}^{-(RM_{\mu}/RM_{\sigma})} \frac{1}{\sqrt{2\pi}} e^{\frac{-y^2}{2}} dy \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.2)$$

$$P_{hold-failure} = \int_{-\infty}^{-(HM_{\mu}/HM_{\sigma})} \frac{1}{\sqrt{2\pi}} e^{\frac{-y^2}{2}} dy \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.3)$$

where, (RM_{μ}, RM_{σ}) and (HM_{μ}, HM_{σ}) refer to (mean, standard deviation calculated over all RMs) and (mean, standard deviation calculated over all HMs), respectively.

The failure probabilities of Proposed design 5, Proposed design 6 and considered nvSRAM cells for write, read and hold operations are shown in Fig. 5.23, and the Vmin values are

tabulated in Table 5.3. From Fig. 5.23, it is depicted that the Proposed design 5 and 6 shows the minimum failure probability during write, read and hold operations. From Table 5.3, the static Vmin (considering write, read and hold margins) of Proposed design 5 and 6 is observed as 450mV and 510 mV, respectively, which are lower than the Vmin of considered RD nvSRAM cells.

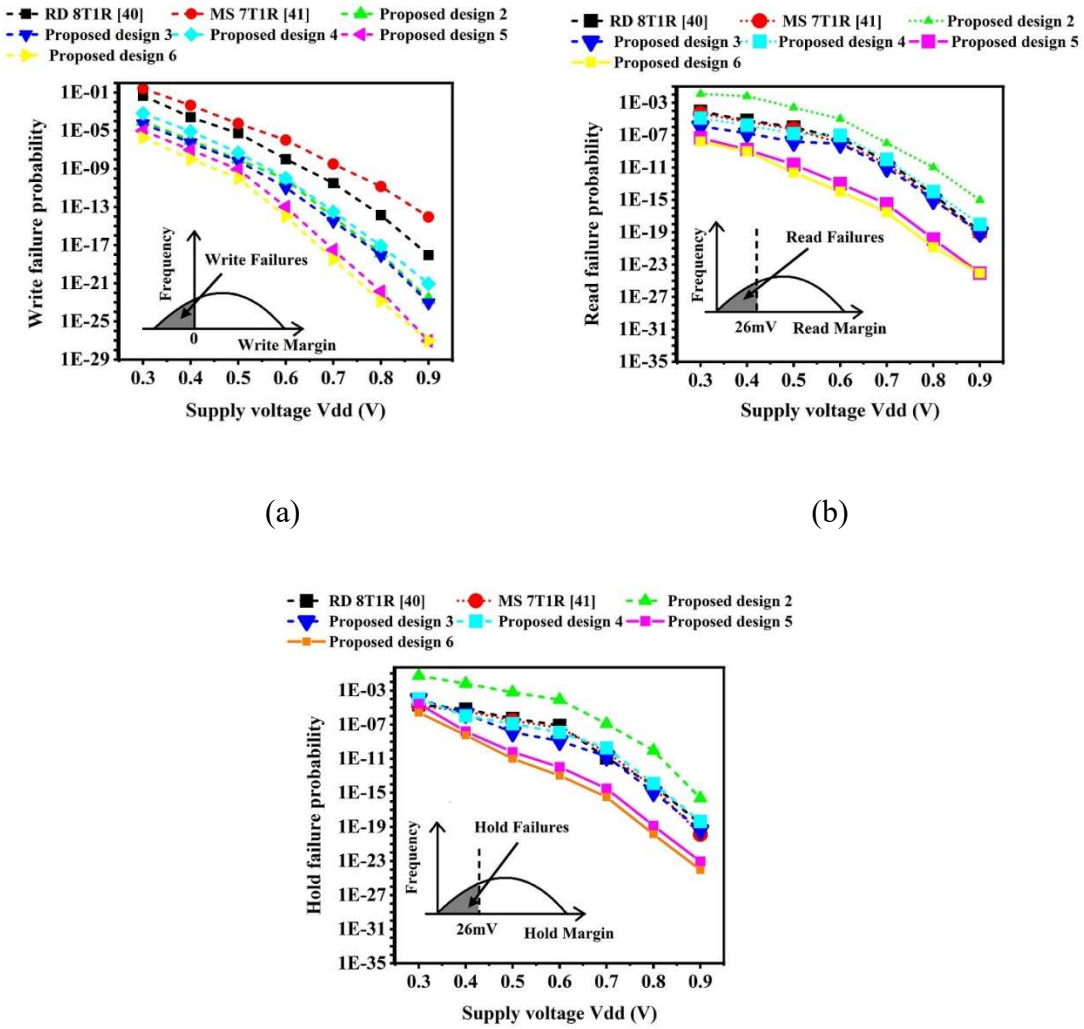


Fig. 5.23. (a) Write (b) read and (c) hold failure probabilities of Proposed design 6 and considered RD nvSRAM cells

The above analyses are sufficient to study the static behavior, however, does not account for dynamic behavior of nvSRAM cells. The write/read operations are successful for longer write/read wordline but might fail for shorter duration of pulses. Hence, the timing analysis of nvSRAM cells is an important constraint and therefore dynamic performance must be evaluated. For this, the clock period is calculated first which is considered as the time delay of twenty minimum sized fan-out of four inverters [72].

The write access failure ($P_{w-accesse}$) occurs when the cell is unable to flip the internal node data in given duration of pulse width. Similarly, the read access failure ($P_{r-access}$) occurs when the read bitline is not able to discharge and the sense amplifier does not produce the required output during the desired duration of pulse width. The store failures (P_{store}) occurs when memristor is not able to change its state for given pulse width. While, the restore failures ($P_{restore}$) occurs when the data is not recovered from memristor to internal nodes after power down for desired duration of pulse width. The write access, read access, store and restore failure probabilities are defined as:

$$P_{w-access} = Prob\left(T_{write} < T_{WWL}^{write}\right) \dots\dots\dots\dots\dots \quad (5.4)$$

$$P_{r-access} = Prob\left(T_{read} < T_{RWL}^{read}\right) \dots\dots\dots\dots\dots \quad (5.5)$$

$$P_{store} = Prob(T_{store} < T_{CTL1}^{store}) \dots\dots\dots\dots\dots \quad (5.6)$$

$$P_{restore} = Prob(T_{restore} < T_{CTL1}^{restore}) \dots\dots\dots\dots\dots \quad (5.7)$$

where, T_{write}/T_{read} is the write access/read access and $T_{store}/T_{restore}$ is store delay/restore delay time; $T_{WWL}^{write}/T_{RWL}^{read}$ is the pulse width of write/read wordline and $/T_{CTL1}^{store}/T_{CTL1}^{restore}$is the pulse width of control signals CTL1. Here, the inverse of $T_{write}/T_{read}/T_{store}/T_{restore}$

can be easily approximated using normal gaussian distribution [72]. Hence, the write access/read access/store/restore failure probabilities can be easily calculated by evaluating the sensitivities of $(1/T_{write})$ or $(1/T_{read})$ or $(1/T_{store})$ or $(1/T_{restore})$ with respect to switching threshold voltage variation.

$$P_{w-access} = Prob\left(\frac{1}{T_{write}} < \frac{1}{T_{WWL}^{write}}\right) = \emptyset\left(\frac{\frac{1}{T_{WWL}^{write}} - \left(\frac{1}{T_{write}}\right)_{nom}}{\sigma_{write}}\right) \ldots\ldots\ldots\ldots\ldots (5.8)$$

$$P_{r-acces} = Prob\left(\frac{1}{T_{read}} < \frac{1}{T_{RWL}^{read}}\right) = \emptyset\left(\frac{\frac{1}{T_{RWL}^{read}} - \left(\frac{1}{T_{read}}\right)_{nom}}{\sigma_{read}}\right) \ldots\ldots\ldots\ldots\ldots (5.9)$$

$$P_{store} = Prob\left(\frac{1}{T_{store}} < \frac{1}{T_{CTL}^{store}}\right) = \emptyset\left(\frac{\frac{1}{T_{CTL1}^{store}} - \left(\frac{1}{T_{store}}\right)_{nom}}{\sigma_{store}}\right) \ldots\ldots\ldots\ldots\ldots (5.10)$$

$$P_{restore} = Prob\left(\frac{1}{T_{restore}} < \frac{1}{T_{CTL}^{restore}}\right) = \emptyset\left(\frac{\frac{1}{T_{CTL1}^{restore}} - \left(\frac{1}{T_{restore}}\right)_{nom}}{\sigma_{restore}}\right) \ldots\ldots\ldots\ldots (5.11)$$

where, σ_{write}, σ_{read}, σ_{store} and $\sigma_{restore}$ are standard deviation of $(1/T_{write})$, $(1/T_{read})$, $(1/T_{store})$ and $(1/T_{restore})$, respectively. The write access, read access, store and restore failure probabilities are determined at the 6σ failure probability i.e., $P_{w-access} = P_{r-access} = P_{store} = P_{restore} = 1E-9$.

The access time failure probabilities for proposed and considered nvSRAM cells are shown in Fig. 5.24 and the corresponding Vmin values are given in Table 5.3. From Fig. 5.24, it is observed that the Proposed design 5 shows minimum write access, read access failure

probabilities, while Proposed design 6 shows minimum store access and restore access failure probabilities. From Table 5.3, the dynamic Vmin (considering write access, read access, store access and restore access) of Proposed design 5 and 6 is observed as 795mV and 732mV, respectively, which are lower than the dynamic Vmin of considered RD nvSRAM cells.

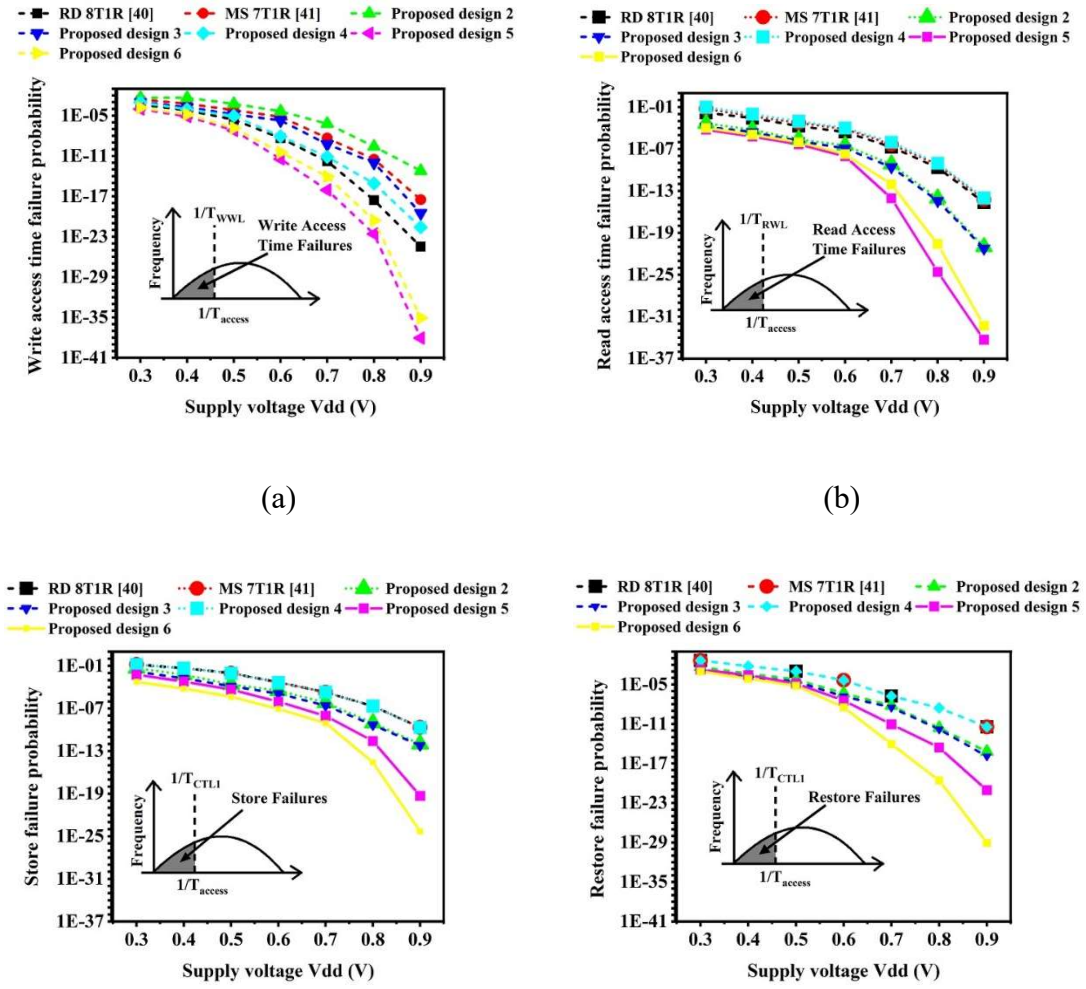


Fig. 5.24. (a) Write access (b) read access (c) store access and (d) restore access failure probability of Proposed design 6 and considered RD nvSRAM cells

Table 5.3. Vmin of Proposed design 6 and considered RD nvSRAM cells

Vmin	nvSRAM cells						
	RD 8T1R [40]	**MS 7T1R** [41]	**Proposed design 2**	**Proposed design 3**	**Proposed design 4**	**Proposed design 5**	**Proposed design 6**
Write Vmin (mV)	640	720	530	540	550	450	510
Read Vmin (mV)	630	620	730	610	630	405	410
Hold Vmin (mV)	595	595	720	580	595	410	395
Write access Vmin (mV)	630	727	796	710	642	550	555
Read access Vmin (mV)	792	792	690	690	798	630	635
Store Vmin (mV)	870	870	815	815	875	795	732
Restore Vmin (mV)	807	807	751	751	819	710	645

5.5. Conclusion

In this chapter, two process invariant designs (Proposed design 5 and Proposed design 6) are introduced. Both the proposed designs use ST inverter in core instead of CMOS inverter. The built-in feedback mechanism of ST inverter provides tolerance against process variations and increases the cell stability during all modes of operations. In Proposed design 5, memristor is connected between internal node Q and bitline RBL via read pass transistor.

For Proposed design 5, the maximum reduction in write and read delay is observed as 24.64% and 23.53%, respectively, at Vdd =0.6V in comparison to considered RD nvSRAM cells. In addition to this, the store and restore delays are observed as 86.25ps and 80.05ps,

respectively, while, the store and restore power consumptions are observed as 2.15µW and 1.25µW, respectively at Vdd = 0.6 V for the Proposed design 5.

In Proposed design 6, 1T1M structure is used to perform non-volatile operation. The maximum improvement of 25.71%, 27.78% and 27.78% is observed in WM, RM and HM, respectively, in comparison to considered RD nvSRAM cells. The maximum reduction in write delay is 23.89% in comparison to existing RD nvSRAM cells, Proposed design 2 and 3. The store and restore delays of Proposed design 6 is minimum and reduced by 15.94% and 22.42%, respectively, in comparison to considered RD nvSRAM cells, proposed design 4 and 5.

The 6σ failure point is used to calculate the failure probability and the corresponding supply voltage, known as Vmin, is observed. It is found that the Proposed design 6 shows minimum Vmin, which is 732mV, in comparison to existing and proposed RD nvSRAM cells. Also, minimum leakage power consumption is found for Proposed design 6.

Chapter 6

Conclusion and Scope for Future Work

In this thesis, different nvSRAM cells are introduced to improve performance during various operations such as write, read, hold, store and restore. The process invariant nvSRAM cells are also introduced in this work. A comprehensive summary of each chapter highlighting the important features and significant findings is described in the subsequent section along with the scope for future work.

6.1. Summary of work done

The first chapter of this thesis puts forward an overview of existing nvSRAM cells. The issues of SRAM cell such as its volatile nature and leakage are discussed in this chapter. The introduction of NVM device to SRAM known as nvSRAM comes out as an approach to overcome above mentioned issues. It is followed by detailed description of nvSRAM cell during write, read, hold, store and restore operations. The common terminologies used for nvSRAM cell are also discussed. Hereafter, a brief overview of existing nvSRAM cells is presented that leads to finding of the research gaps and on the basis of this, the research objectives are identified. In the last, the organization of thesis is presented.

Chapter 2 puts forward an eight transistor nvSRAM cell named as Proposed design 1. It performs single ended write operation and differential read operation. Here, a feedback transistor is used that remains off during write operation, hence, leading to series connection of inverters instead of back-to-back connection. This causes the dependency of write operation on charging/discharging of single bitline only that helps in write power reduction. The Proposed design 1 uses 1T1M structure to perform non-volatile operation. The SPICE simulations are carried out to verify the functionality of Proposed design 1 and analyse its performance with respect to considered 8T nvSRAM cells. The effect of supply voltage variations is also examined. The presence of feedback transistor causes higher leakage power

consumption than its counterparts. To mitigate this issue, three different design cases are provided: Case-1 with low V_T Mf1, Case-2 with high V_T Mp1/Mp2 and Case-3 with low V_T Mf1 and high V_T Mp1/Mp2. Among the given solutions, Case 2 comes out as the best approach to reduce leakage power consumption.

In chapter 3, two nvSRAM cells (Proposed design 2 and Proposed design 3) comprising of RD port are presented with an aim of improving read performance. Both the proposed designs employ 1T1M structure for supporting non-volatile operation. Further, single ended write operation is used in both the proposed designs to reduce write power consumption. In Proposed design 2, one of the pull-down transistors is a grounded gate LVT which helps in maintaining the performance near threshold voltage. To supplement read operation near threshold voltages, a charge pump circuit is used that overdrive RD port and fasten reading of the data. The SPICE simulations are carried out to verify the functionality of Proposed design 2 and analyse its performance with respect to considered RD nvSRAM cells. The Proposed design 3 uses column shared transistor to improve write performance of RD nvSRAM cell. This transistor remains off during write operation, thus weakening the current driving capability of pull-down path and improving WM. The functionality of Proposed design 3 is verified through SPICE simulations. Its performance is analysed and compared with considered RD nvSRAM cells and Proposed design 2. The supply voltage variation study is also shown at the end of each performance analysis for both Proposed design 2 and 3.

Along with the write/read margin and power consumption, delay is also an important parameter. The longer store/restore delay may lead to loss of the data. Chapter 4 presents different techniques to reduce store/restore delay. To reduce store delay, boosted CTL1 and

negative CTL2 techniques are introduced. For restore delay reduction, boosted CTL1 and floating Vss techniques are presented. These techniques are generic in nature and can be applied to nvSRAM cells that uses 1T1M structure to perform non-volatile operation. For verification purpose, these techniques are applied on Proposed design 1 and the results are verified through SPICE simulations. It is found that negative CTL2 technique gives reduced store delay, while, floating Vss technique gives reduced restore delay. It is also observed that the reduction in store/restore delay is achieved at the cost of increased power consumption. Further, the Propose design 4 is introduced in order to reduce write delay. In this design, the access transistor is replaced with transmission gate. It provides strong '1' leading to fast write '1' operation and improvement in WM. The read operation is performed through RD port. To perform non-volatile operation, memristor is connected between internal node and read bitline through read pass transistor. The SPICE simulations are carried out to verify the non-volatile functionality. Its performance is analysed and the results are compared with existing RD nvSRAM cells. The supply voltage variation study is also performed for completeness.

Due to continuous downscaling in technology and supply voltage, the sensitivity of nvSRAM cells against process variations is increased. Considering this fact, two process invariant nvSRAM cells (Proposed design 5 and Proposed design 6) are introduced in chapter 5. Both the proposed designs use ST inverter in the core and RD port for performing read operation. The ST action improves WM, and provides tolerance against process variations during read and hold operations. In Proposed design 5, the memristor is connected between internal node and read bitline through read pass transistor. The functionality of Proposed design 5 is verified through SPICE simulations and its performance is compared with existing RD nvSRAM cells, Proposed design 2 and Proposed design 4. The Proposed design 6 uses 1T1M

structure to perform non-volatile operation. The functionality is verified through timing waveform using SPICE simulations and its performance is compared with existing RD nvSRAM cells, Proposed design 2, Proposed design 3, Proposed design 4 and Proposed design 5. The effect of supply voltage variation on performance parameter is also examined. In addition to this, the failure probability analysis for all existing and proposed RD nvSRAM is also carried out to observe Vmin values. From the analysis, it is observed that Proposed design 5 and Proposed design 6 give lower failure probability and lower Vmin value in comparison to existing RD nvSRAM cells, Proposed design 2, Proposed design 3 and Proposed design 4.

6.2. Scope for future work

Memristor based SRAM are gaining popularity in memory design space due to its capability of retaining data in power down mode. This thesis majorly focuses on introducing new nvSRAM designs for better performance. The sensitivity to process variations are discussed and the process invariant nvSRAM cells are introduced in this work. There are several dimensions where this work can be further extended. Some possibilities are as follows:

a) Three techniques are suggested for improving store/restore delay and studied in context of Proposed design 1. The impact of these techniques on other nvSRAM cells may be investigated.
b) Multi-gate devices such as FinFETs, Carbon nanotube FETs have good scaling ability, better subthreshold slope, high ON current, reduced threshold voltage variations and short channel effects in comparison to CMOS. The nvSRAM cells may be designed and developed using these technologies.

c) The work on process invariant nvSRAM cell may be extended to explore designs with single ended write to present low power process invariant nvSRAM cells.

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