ANALYTICAL MODELLING AND NUMERICAL SIMULATION OF PLASMA-ASSISTED GATE ALL AROUND CARBON NANOTUBE FIELD EFFECT TRANSISTOR

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By

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Dedicated to
my loving family

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CERTIFICATE

This is to certify that the thesis entitled "**Analytical Modelling And Numerical Simulation of Plasma-Assisted Gate All Around Carbon Nanotube Field Effect Transistor**" submitted by ***Ms. Mansha Kansal (2K19/PhD/AP/508)*** to Delhi Technological University (DTU), Delhi, India for the degree of Doctor of Philosophy, is a bonafide record of the research work carried out by her under my supervision and guidance. The work embodied in this thesis has been carried out in the Plasma & Nano-Simulation Lab, Department of Applied Physics, Delhi Technological University (DTU), Delhi, India. The work of this thesis is original and has not been submitted in parts or fully to any other Institute or University for the award of any other degree or diploma.

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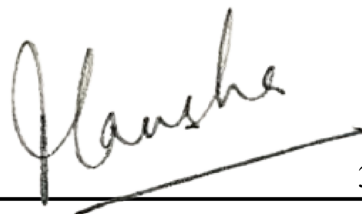
DECLARATION

I, **Ms. Mansha Kansal**, hereby certify that the thesis titled **"Analytical Modelling and Numerical Simulation of Plasma-Assisted Gate All Around Carbon Nanotube Field Effect Transistor"** submitted in the fulfilment of the requirements for the award of the degree of Doctor of Philosophy is an authentic record of my research work carried out under the supervision of ***Prof. Suresh C. Sharma***. This work in the same form or any other form has not been submitted by me or anyone else earlier for any purpose. Any material borrowed or referred to is duly acknowledged.



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Mansha Kansal

ABSTRACT

Carbon Nanotube Field-Effect Transistors (CNTFETs) are becoming the torch-bearers of advancements in the realm of electronics. The semiconductor industry's backbone, traditional silicon-based transistors, is reaching its scaling limits. Power consumption, heat dissipation, and quantum effects become increasingly pressing as the size of these transistors continues to decrease. CNTFETs may be able to help us get around these restrictions by leveraging the use of the distinct properties of Carbon Nanotubes (CNTs).

CNTFETs are desirable for use in cutting-edge electronics because of their excellent electrical characteristics. Due to their great carrier mobility, CNTFETs may provide rapid processing and enhanced efficiency. In response to the growing need for low-power electronic devices, their high current-carrying capacity makes it possible for these devices to function efficiently.

In addition, CNTFETs have potential applications in bioelectronics and sensing. Their great sensitivity and biocompatibility make them useful in biosensors, implantable devices, and bioelectronic interfaces. Precision detection and monitoring of biological species are leading to new possibilities in healthcare, diagnostics, and personalised medicine. In conclusion, the quest for high-performance, energy-efficient, flexible, and bio-compatible electronic devices has led to the development of CNTFETs as a solution to the limits possessed by conventional silicon-based transistors.

The thesis aims to shed light on the potential of Plasma-Assisted Gate-All-Around CNTFET technology to revolutionise the future of electronic devices by examining its development and many applications. The research demonstrates the effect of plasma parameters on the performance of a simulated device known as Plasma-Assisted Vertically Aligned Dual-Metal Carbon Nanotube Field-Effect Transistor (VA-DMCNFET). A vertically aligned semiconducting Carbon Nanotube (CNT), produced via the Plasma-Enhanced Chemical Vapour Deposition (PECVD) technology, has been used as the channel. A typical Si-based Nanowire Field-Effect Transistor (NWFET) may be compared to the proposed device, which demonstrates a

considerable increase in performance. The DC and analogue performance of the VA-DMCNFET is analysed for various plasma parameters corresponding to different values of CNT channel radius (for fixed CNT channel length) and varied values of CNT channel length (for fixed CNT channel radius). It has been found that lower values of plasma parameters are necessary for higher values of drain current, transconductance, output conductance, and cutoff frequency, as well as lower values of threshold voltage and channel resistance. On the other hand, higher values of plasma parameters are necessary for a better I_{ON}/I_{OFF} current ratio, early voltage, and gain of the proposed device. It is possible to increase the device's efficiency and, as a result, its applicability and performance in real-world settings by making alterations to the plasma parameters.

Further in this study, the simulation analysis of a novel device known as a Plasma-Assisted Dual-Material Stacked Gate-Oxide Carbon Nanotube Field Effect Transistor (DM-SGCNFET) is shown. This device has a stacked gate oxide structure that is composed of two oxides: SiO_2 and HfO_2. The performance metrics of the simulated device are compared with a SiO_2-based DM-CNFET for changing sets of plasma characteristics that correlate to different values of channel length. Comparing the DM-SGCNFET to the DM-CNFET, the in-depth study reveals that the former has superior characteristics in terms of the drain current, transconductance, output conductance, early voltage, gain, gate capacitance, improved switching ratio and lower channel resistance. The novel architecture of DM-SGCNFET paves the way for the device to be a suitable candidate for digital and analogue applications that need high efficiency. This work investigates the simulated device further for its linearity distortion performance. This is done by analysing the values of g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3, and the 1-dB compression point for varying plasma parameter values. The results show promising application potential for the simulated device in wireless communication systems.

In addition, this study develops a HfO_2 based Plasma-Assisted Gate All Around Carbon Nanotube Field Effect Transistor (GAA-CNTFET). The results of the study conclude that utilising HfO_2 results in improvements in all the observed performance metrics, including higher values for drain current, transconductance, output conductance, early voltage, and gate capacitance. The simulated device was put to

study for sensing applications. This is achieved by implementing a cavity in the oxide layer and using the notion of dielectric modulation, which makes it possible to discover the change in performance characteristics of the device upon altering the dielectric permittivity of the molecule inside the cavity. The higher the dielectric constant value, the better the performance and the more sensitive the device will be. The findings of this research provide useful information for quantifying the device's potential uses in the sensing fields of biology, the environment, and other important sectors.

Thermal stability and conductivity shown by CNT is another fascinating area of research as it opens the doors for unprecedented applications. The study showcases the robustness and stability shown by a simulated DM-SGCNFET device by testing it at different temperature values for temperatures up to 500K. Precision-demanding industries such as aerospace, military, and heavy-scale industries can take benefit from the findings of this study to develop new-age solutions.

ABBREVIATIONS

CNT	Carbon Nanotube
GAA	Gate-All-Around
TCVD	Thermal Chemical Vapour Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
CNTFET	Carbon Nanotube Field-Effect Transistor
NWFET	Nanowire Field-Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
VA-DMCNFET	Vertically Aligned Dual-Metal Carbon Nanotube Field-Effect Transistor
DM-SGCNFET	Dual-Material Stacked Gate-Oxide Carbon Nanotube Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
GAA-CNTFET	Gate-All-Around Carbon Nanotube Field Effect Transistor
VACNTs	Vertically aligned CNTs
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RF	Radio Frequency
SCE	Short Channel Effect

LIST OF PUBLICATIONS

International journals

1. **Mansha Kansal**, Suresh C. Sharma, “Investigation of Plasma-Assisted Stacked Gate-Oxide Gate All Around CNTFET (SG-GAA-CNTFET) with Temperature Variations for High Frequency and Wireless Applications**”** (Communicated).
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1. **Mansha Kansal**, Suresh C. Sharma, **“**Numerical Simulation of Performance Metrics of Dual Metal Gate Carbon Nanotube Field Effect Transistor (DM-CNTFET) for Numerous Sensing Purposes**”,** *Materials Today: Proceedings,* SI: ICAMN (2022).
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INTRODUCTION

1

INTRODUCTION

1.1 BACKGROUND AND RESEARCH MOTIVATION

Advancements in nanoelectronics has made it possible to realise new-age electronic devices that are smaller, faster and more energy-efficient. The study of designing, developing, and ultimately deploying electrical components at the nanoscale level is known as nanoelectronics. The study and use of nanomaterials is now the most rapidly expanding area in material science and engineering.

At nanoscale dimensions, certain physical and chemical characteristics of materials are highlighted, leading to novel functionality of the synthesized electronic devices. Nanoelectronics has revolutionized several industries, including computer processing, sensing, energy, and medicine.

There are three primary configurations of elemental Carbon: Graphite, which consists of stacked planar graphitic sheets, Diamond, in which the carbon atoms are bonded tetrahedrally to each other in a massive three-dimensional structure and Fullerenes, a large and diverse class of hollow spheres, ellipses, and tubes made of sp^2 hybridized carbon atoms [1,2]. The discovery of fullerenes [3] and carbon nanotubes (CNTs) [4] sparked the development of a new area of research, leading to an increase in our knowledge of physics, chemistry, and potential technological applications [5,6] of these carbon configurations. Carbon nanotubes (CNTs) are cylindrical nanostructures composed of carbon atoms arranged in a hexagonal lattice. Figure 1.1 shows transformation of 2D graphene into various carbon nanostructures. Each discovery, notably the most recent [7,8] ones, has forecasted a major shift in materials science and electronics. Single-walled carbon nanotube (SWCNT) production was rapidly demonstrated using a laser ablation approach [9]. Single-walled carbon nanotubes (SWCNTs) are the building blocks of multi-walled carbon nanotubes (MWCNTs). Iijima [4] reported the finding of MWCNTs in the early 1990s. These are tubular carbon nanostructures that have been crystallized and stacked several times. They have

remarkable mechanical, electrical, and thermal properties and have gathered much interest from researchers.

Ever since their discovery, there has been a lot of enthusiasm for studies involving manufacturing, characterization, growth process, chemical modifications, and potential uses of CNTs. Extensive research has opened the door for CNTs to find applications in industries such as nanoelectronics, energy storage, composites, sensors, and biomedicine. Due to their superior electrical properties and scaling capabilities, CNTs are front runners to replace conventional channel materials and keep CMOS technology relevant for the modern age.

Nanoarchitectonics has made it possible to harness the special properties of CNTs into realisable electronic circuits. Incorporating CNTs into nanoarchitectonic frameworks, has opened the doors for exciting avenues in the near future.

1.2 INTRODUCTION TO CARBON NANOTUBE (CNT)

Carbon Nanotube (CNT) is a superior new-age composed of carbon atoms arranged in a cylindrical structure with a diameter in the nanometre range [10]. Since their discovery in 1991 [1], CNTs have sparked much interest from researchers owing to their distinct and superior material properties. Carbon nanotubes are the perfect answer to two big problem statements of conventional materials - scaling limitations and power limitations. They stands as the number one candidate to take advantage of rapid advancements in nanotechnology.

The unique abilities possessed by CNTs arise from their nanoscale dimensions and high aspect ratio. They exhibit exceptional mechanical strength along with superior electrical and thermal conductivity. Their versatility makes them an ideal material for testing and research applications.

The superior electrical conductivity of CNTs has great application potential. They are known to conduct electricity at exceptionally low resistance. Nanoelectronics has received a major boost owing to CNTs' exceptional electrical conductivity, with extensive work being done to integrate them with transistors, sensors, and other electrical components. Their high power capabilities are set to revolutionize the electronics industry as we know it.

The thermal conductivity of CNTs is amongst the highest seen in current mainstream materials and has been another area of fascination. They are resistant to high temperatures, expanding their applications to usage in heat sinks, thermal management, and more. Their ability to conduct a high magnitude of current at high-temperature values makes them frontrunners for usage in innovative solutions for heatsink applications.

In conclusion, CNTs offer highly desirable research avenues owing to their superior material properties and application potential. The meteoric rise in the number of patent applications and academic courses on CNT is a testament to the excitement and interest shown by researchers around the globe ever since their discovery. A lot of unknowns need to be unlocked before CNTs are deployed for wide scale applications and start replacing conventional materials.

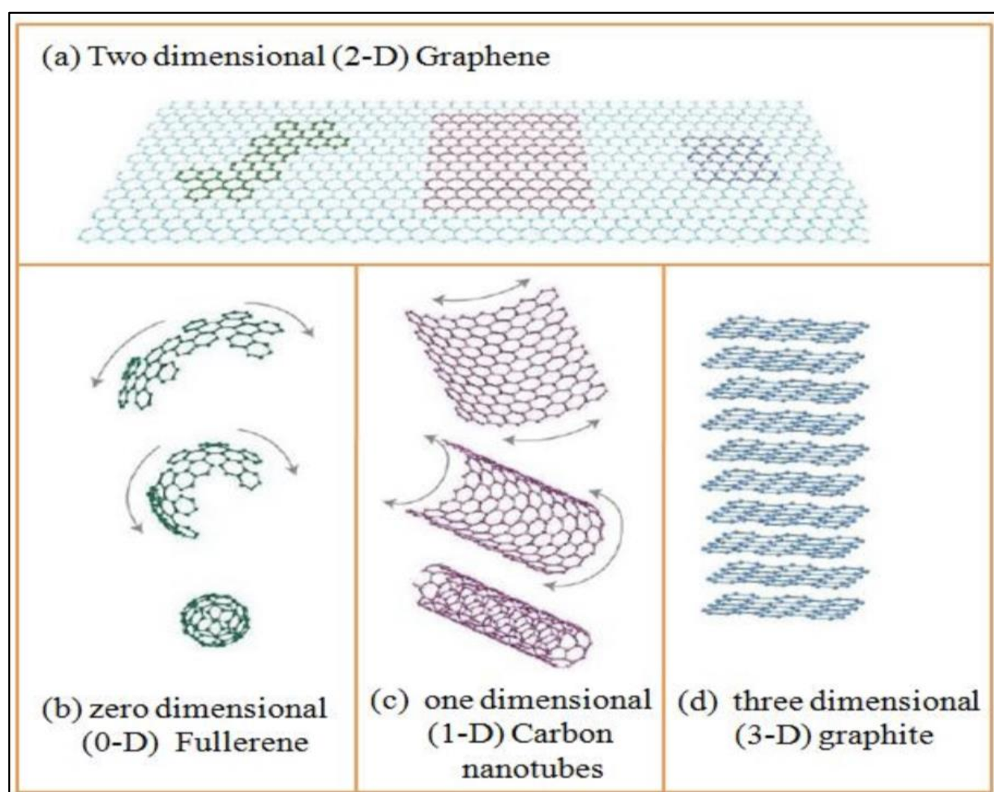

Figure 1.1: Transformation of 2D graphene into various carbon nanostructures [11].

1.3 STRUCTURE OF CARBON NANOTUBE

A CNT can be visualized as a rolled-up sheet of graphene. A graphene sheet comprises of carbon atoms bonded and arranged in a hexagonal mesh. The carbon-carbon bond strength provides CNTs with tough strength. The direction and angle of rolling of this graphene sheet affects the properties of resultant CNT. It affects its physical properties, such as diameter and chirality, which in turn affects its electrical properties. Figure 1.2 represents the schematic of the graphene lattice with $\boldsymbol{C}$ as the chiral vector; $\boldsymbol{T}$ as the translation vector; and $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ as basis vectors, respectively [12].

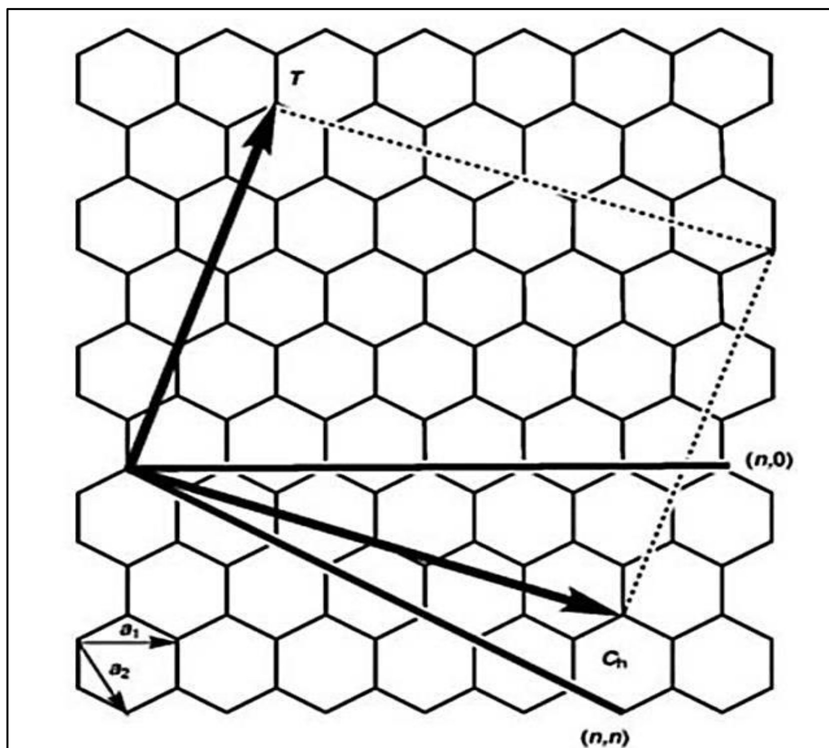

Figure 1.2: Schematic of graphene lattice with $\boldsymbol{C}$ as the chiral vector; $\boldsymbol{T}$ as the translation vector; and $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ as basis vectors, respectively [12].

1.4 TYPES OF CARBON NANOTUBE

CNTs can be structurally characterized into three types - Single-Walled, Double-Walled and Multi-Walled Carbon Nanotubes. All of them have significantly different physical properties. The sizes of single-walled carbon nanotubes (SWCNTs), and

multi-walled carbon nanotubes (MWCNTs) are quite different, as shown in Figure 1.3. Despite minimal diameters, they have extremely high aspect ratios. Therefore, CNTs are considered to be quasi-one-dimensional materials [13]. There are typically two types of CNTs: (1) single-walled CNTs (SWCNTs), which have only one graphene layer, and (2) multi-walled CNTs (MWCNTs), which have nested co-axial arrays of single-walled CNTs that are spaced apart by an average of 0.34 nm, which is marginally more significant than the interlayer separation of graphite.

1.4.1 SINGLE-WALLED CARBON NANOTUBES (SWCNTS)

Single-Walled Carbon Nanotubes are carbon atoms in a single hollowed-up graphene sheet. They have 1-2 nm diameters and an aspect ratio as high as 10^4. The properties of SWCNTs are governed by two important metrics - diameter and chirality. Chirality is a measure of the orientation of the hexagon carbon lattice with respect to the tube axis. The chiral angle plays a crucial role in determining the electrical properties of the resultant CNT. Based on the chiral vector orientation, they can be both metallic and semiconductors.

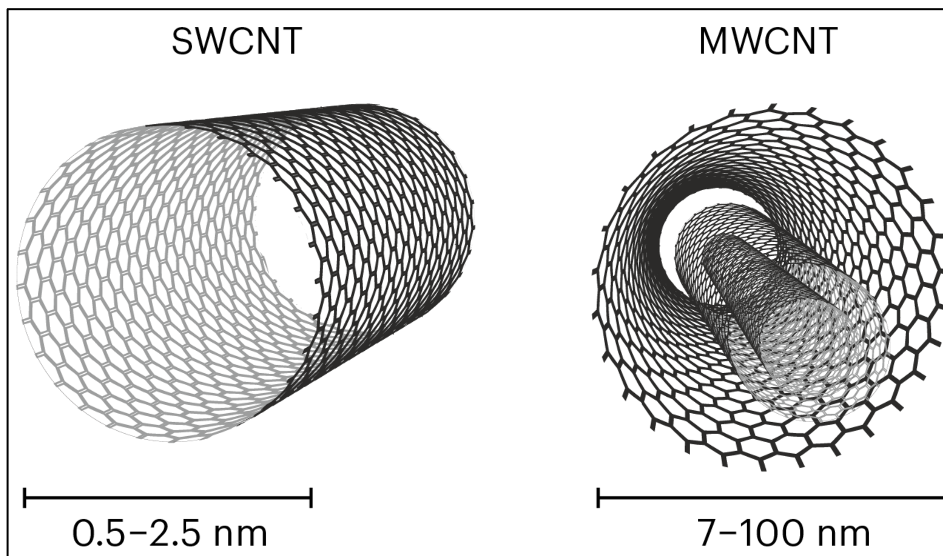

Figure 1.3: Types of CNTs: SWCNT (single-walled carbon nanotubes) and MWCNT (multi-walled carbon nanotubes) [14,15]

1.4.2 MULTI-WALLED CARBON NANOTUBES (MWCNTS)

As the name suggests, MWCNTs consist of multiple sheets of graphene rolled to form concentric cylindrical tubes. They can be imagined as multiple SWCNTs rolled up over one another. They have unique properties with diameters ranging to 100 nm and an aspect ratio of 10^3.

1.5 PROPERTIES OF CARBON NANOTUBE

Since CNTs have a high aspect ratio and a hollow structure, charge carriers move in one dimension in these materials. Their resistivity is 10^{-6} Ω cm at room temperature, much less than that of the resistivity of silver and copper [9,16]. The mobility of holes in semiconducting CNTs (~2×10^4 cm^2/Vs) is higher than that of electrons and holes in silicon (~1.5×10^3 cm^2/Vs) and (~4.5×10^2 cm^2/Vs). The CNTs also have a high current density (10^7-10^9 A/cm^2) [17,18]. The experimental range for CNT Young's modulus [19,24] is 0.7-1.8 TPa, whereas theoretically [25] is 0.5-5 TPa. This shows that CNTs are more robust and stiffer than steel [26,27], with Young's modulus of about 0.18-0.2 TPa.

Numerous electronic devices can find CNT relevant because of its diameter-dependent energy gap. CNT-based Field-Effect Transistors (FETs) feature metal electrodes linked via a CNT on the high substrate point and topped by an insulating layer. CNTs have an inherent advantage over bulk semiconducting materials to function as the key component of a single electron transistor (SET) because the CNT's 1D nature constrains electron delivery in the nanostructure. CNT conductance is very sensitive to the electrostatic environment because of the enormous surface-to-volume ratio of CNTs.

Semiconducting CNTs can flip between conducting and non-conducting states, hence allowing them to precisely regulate electrical current flow, making them appropriate for use as transistors and other electronic devices.

Scalability and integration possibilities for CNTs are quite promising. Researchers have created methods for precisely arranging individual CNTs, making it possible to

fabricate integrated circuits, interconnects, and transistors based on CNTs. Controlling CNT chirality, large-scale synthesis, and assuring device repeatability are still some of the issues that need to be addressed.

The field of nanoelectronics has received a major boost since the rise of CNT. The creation of cutting-edge electronic devices and integrated circuits based out of CNTs are promising owing to their high electrical conductivity, bandgap flexibility, ambipolar behavior, and scalability.

1.6 APPLICATIONS OF CARBON NANOTUBE

Since its discovery, CNT has been labelled as a superior new-age material. Excellent electrical and thermal conductivity, high physical strength, and versatility are notable advantages it holds over its counterparts.

Owing to these properties, CNTs are studied for various applications – both for improvements in pre-existing solutions and the development of novel applications. Some of the most prominent applications currently being investigated for CNT usage are -

1.6.1 MOLECULAR ELECTRONICS

Molecular electronics is a fast-developing area that investigates using specific molecules or nanoscale materials as electrical device building blocks. CNTs have attracted much attention in molecular electronics. Owing to their great electrical conductivity and low resistance, they can function as nanoscale wires or interconnects in electronic circuits, allowing for the downscaling of electronic components.

CNTs may be incorporated into nanoscale transistors, switches, and sensors. They are well suited for nanoscale logic circuits due to their high carrier mobility, low power consumption, and temperature adaptability. More and more work is being done to create sophisticated electrical devices with high-density integration of CNTs.

CNTs have shown huge potential to function as molecular sensors. Their quick reaction time to external changes implies that they offer high sensitivity – a metric strongly

measured for high-performance sensors. Adding to this, they also benefit with quick reaction times, and the capacity to identify minute quantities of target molecules, thus making for an all-rounded sensor.

1.6.2 STRUCTURAL MATERIALS

CNTs have remarkable mechanical qualities. They are strong, rigid, and low-density making them very appealing for usage as a structural material. Composites reinforced with CNTs have demonstrated better mechanical characteristics, such as increased tensile strength, toughness, and thermal stability. Industries such as aerospace, automotive, and sports goods sectors, which need a strong yet lightweight material, may find CNTs useful.

1.6.3 BIOMEDICAL APPLICATIONS

CNTs are the frontrunners to revolutionise biosensing applications. To find infections and biomarkers, CNTs may also be employed as biosensors. Target molecules in biological samples can be detected selectively and sensitively by functionalizing the CNT surface with certain receptors or antibodies. CNT-based biosensors also have usages in food safety, environmental monitoring, and illness.

1.6.4 FIELD-EFFECT TRANSISTORS

Carbon Nanotube-based Field-Effect Transistors, often known as CNTFETs, offer enormous potential for use in electronics. CNTFETs are appealing for various applications, including high-performance logic circuits, flexible electronics, and low-power devices [28,29].

Because of the nanoscale size of CNTs, CNTFETs can enable the miniaturization of electrical devices. They can produce ultra-compact, high-density integrated circuits, which can improve Internet of Things (IoT) applications, wearable electronics, and portable electronics.

Additionally, CNTFETs showcase excellent electrical performance, including high ON/OFF ratios and quick switching times.

CNTs offer a plethora of application possibilities in several industries. They are a frontrunner to revolutionize many industries and be the primary material of choice for more innovative solutions in the future.

1.7 SYNTHESIS OF CARBON NANOTUBES

Synthesis of CNTs can be done in various ways that allow for the controlled development of these unique nanostructures. A few well-known methods include Arc Discharge, Laser Ablation, Chemical Vapour Deposition (CVD), and Plasma-Enhanced Chemical Vapour Deposition (PECVD).

A common approach is CVD, which involves the catalyzed breakdown of carbon-containing gases at high temperatures. It makes it possible to create CNTs with greater customization, including single-walled and multi-walled carbon nanotubes (SWNTs and MWNTs). The Arc Discharge process creates MWNTs using a high-current arc between graphite electrodes. SWNTs are produced via laser ablation, which uses a high-temperature furnace to vaporize a graphite target.

1.7.1 PLASMA ENHANCED CHEMICAL VAPOUR DEPOSITION (PECVD)

While each synthesis technique mentioned above have their own unique advantages, the Plasma Enhanced Chemical Vapour Deposition (PECVD) technique has received much interest. PECVD offers flexibility in resultant CNT that no other synthesis method can.

Since heat is the principal source for chemical reactions, temperatures higher than 750°C are required for the CVD synthesis of CNTs. Microelectronics fabrication typically tops out at about 400°C – 500°C. Thus, this is much beyond that range. The PECVD technique of CNT synthesis is a low-temperature synthesis method. Plasma (a quasineutral state consisting of electrons, ionic species, neutrals, radicals, and others) generates energy that dissociates gaseous species. Vertically aligned CNTs (VACNTs) oriented in the direction normal to the substrate (along the electric field) by the electric field created by the plasma sheath are formed because of the PECVD technique [30,34]. Due to plasma etching of etchant species and ultra-long CNTs, the catalyst deactivation rate (i.e., the formation rate of the amorphous carbon layer over

the catalyst's active region) may be decreased. However, excessive etching can also be detrimental to CNT growth.

The formation of CNTs at high temperatures via Thermal Chemical Vapour Deposition (TCVD) is a vapor-liquid-solid mechanism. During the TCVD-CNT growth process, the catalyst is in a liquid drop state, and carbon species produced from the gaseous species are dissolved into it. The supersaturated eutectic liquid is used as a source of precipitation for the CNTs. It has been claimed that the activation energies necessary for synthesis in TCVD for ~ 700 ^{O}C are between ~ 1.2 – 1.8 eV.

The catalysts can remain solid at low temperatures, so a low-temperature CNT growing mechanism is required. The activation energies for low-temperature CNT growth [35] should be between ~0.2 - 0.4 eV. This is close to the activation energies of carbon surface diffusion [36] on Ni (0.3 eV). The carbon diffusion on the catalyst's surface at low temperatures was suggested as the rate-limiting stage for plasma-assisted growth.

The PECVD method is simple, easy to control, uses low temperatures and pressure, and is the most popular method for synthesizing carbon-based nanostructures. The PECVD method, as mentioned above, uses plasma energy to synthesize CNTs. Some of these plasma sources include -

- Radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD)
- Microwave plasma-enhanced chemical vapor deposition (MW-PECVD)
- Inductively coupled plasma-enhanced Chemical Vapour Deposition (IC-PECVD)
- Direct current plasma-enhanced chemical vapor deposition system (DC-PECVD)

Input power increases the electric field strength of the plasma sheath, causing highly energetic ion bombardments. In PECVD, the ion strikes the electrode and can cause a powerful ionization in the locality of the electrodes. The electric field then accelerates secondary electrons produced into the plasma sheath. This intense plasma causes nanotubes to be damaged. The plasma significantly influences CNT synthesis and ion bombardment of the substrate should be minimized. Luo *et al.* [37] investigated the

ion-bombardment effects and produced high-quality VACNTs using capacitively coupled PECVD by increasing the plasma parameters like input power and pressure.

In PECVD, plasma speeds up the chemical vapor deposition procedure and encourages CNT development. The plasma energy, which is commonly produced by radiofrequency or microwave excitation, is used to split precursor gases apart and produce the reactive species required for the formation of CNTs.

Figure 1.4 displays the schematic representation of the MW-PECVD system. A high frequency of up to 2.45 GHz generates plasma for MW-PECVD. The highly energetic electrons created by this high-density plasma speed up the dissociation of the gaseous species. The process produces hydrogen radicals by dissociating atomic hydrogen, which aids in the efficiently etching of amorphous carbon species and encourages the formation of CNT [38]. The plasma must be produced at high MW power and low pressures, or else the plasma will become unstable. In addition to creating bamboo-like nanotubes deposited using a MW-PECVD system, Srivastava et al. [39] also investigated the impact of gas compositions on the development and morphology of CNTs. It was thought that the composition of the gaseous plasma may regulate the growth of CNTs.

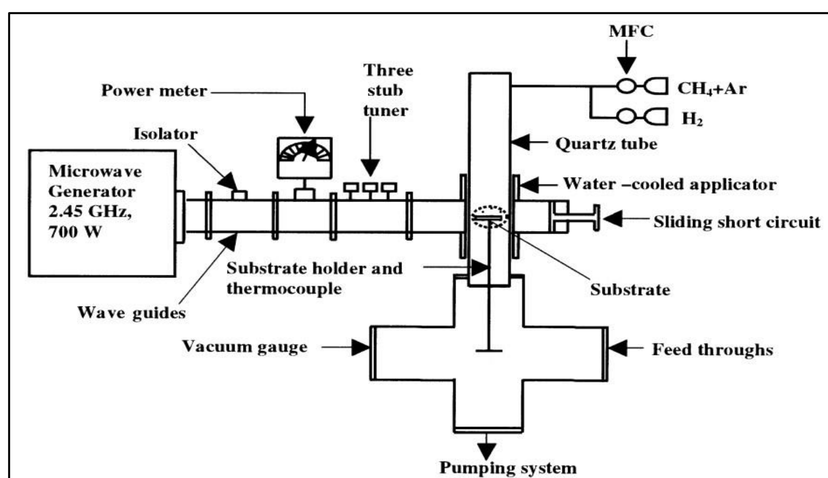

Figure 1.4: Schematic of MW-PECVD setup [40].

1.7.1.1 ADVANTAGES OF PECVD TECHNIQUE

Compared to other techniques, PECVD technique has several benefits for the manufacturing of CNTs.

- **Scalability:** PECVD is a highly scalable process, making it appropriate for the industrial-scale synthesis of CNT. By making deposition on bigger substrates, the synthesis of CNTs can be done for a bigger volume.
- **Precision Control of Growth Parameters:** With the help of Plasma Parameters, PECVD offers fine control over the growth of resultant CNTs. Plasma parameters can control the physical dimensions of CNT, which in turn affect the electrical and thermal conductivity of the material. PECVD offers the highest flexibility in resultant CNT properties, among other synthesis options.
- **Accelerated development rates:** Compared to traditional thermal CVD techniques, the plasma adds more energy to the development process, accelerating the growth of CNTs. Along with the scalability advantages, PECVD is a quick method of producing CNTs.
- **Low Growth Temperatures:** PECVD can produce CNTs at lower temperatures than conventional CVD techniques, which is useful for sensitive substrates. Additionally, this lower growing temperature improves synthesis control and lowers the chance of substrate breakdown.

1.8 PLASMA AND PLASMA SHEATH

Apart from solids, liquids, and gas, plasma is one of our universe's naturally occurring forms of matter. The state of matter is determined by the thermal energy of the atoms and molecules and the interparticle binding energy. The particle's binding energy is highest in solids, lowest in liquids, and almost non-existent in gases. When solids are heated, the thermal energy of their constituent particles outweighs their potential energy, causing bonds to dissolve and a solid-to-liquid phase change. Similarly to this, a liquid turns into gaseous form when heated. The atomic species of the gas develop very high thermal energy and collision with one another at very high temperatures (10,000 ^{O}K or over), which releases electrons from the atoms. The resulting state, often called plasma or ionized gas, compromises of electrons, ions, neutrals, and other

radical species. Although not all ionized gases may be considered plasma, they must meet specific requirements known as quasineutrality and collective behaviour [41] to be classified. When the ion number density and electron number density are in equilibrium in plasma with a length greater than the Debye length, the condition of quasineutrality is met. The Debye length, which is correlated with the electron density (n_{eo}) and temperature (T), is the characteristic length over which the potential caused by a charge within plasma may be shielded.

If a substrate exists in a PECVD reactor, this quasineutrality occurs everywhere except at the boundary or wall. The plasma is in a high-energy state but is neutral since it is created by heating the gas or using electrical energy. Due to quasineutrality, no space-charge zone forms within the bulk of the plasma. Due to higher temperature and lower mass than ions, electrons are far more mobile and have larger fluxes in plasma. The density of positively charged ions in the plasma sheath is marginally more than that of electron density. Figure 1.5 shows the region of the plasma sheath.

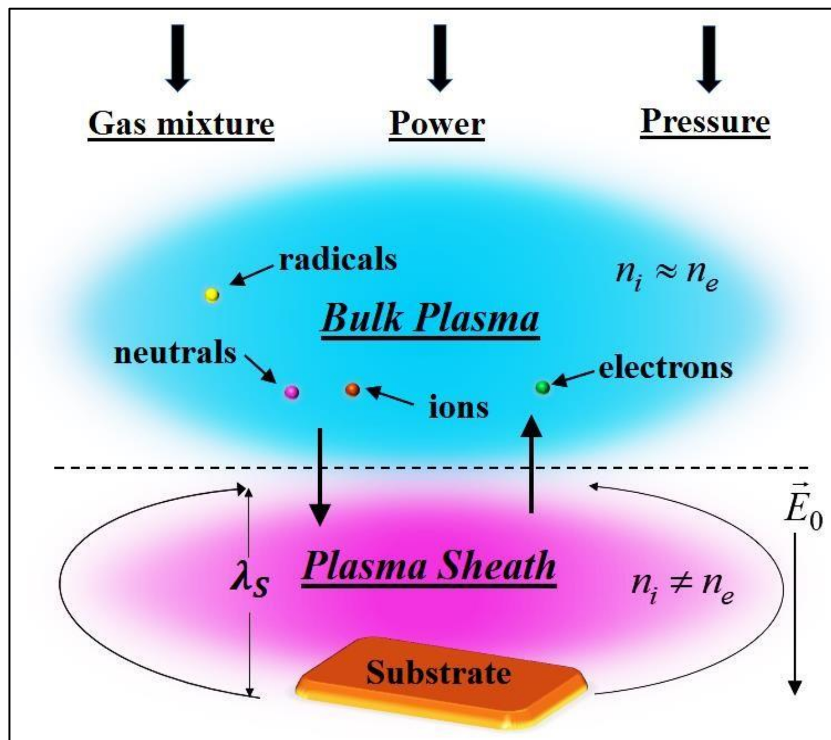

Figure 1.5: Schematic of plasma sheath region [42].

Creating this plasma sheath is essential for the PECVD technique of synthesizing nanostructures because the substrate or surface of the material also interacts with the plasma. In addition, nanostructures also develop in this plasma sheath area.

1.9 MOSFET SCALING AND MOORE'S LAW

Over the past few decades, there have been notable and game-changing breakthroughs in electronics, resulting in the creation of smaller, faster, and more effective electronic devices. The transistor size reduction has been a great triumph for the semiconductor industry. Faster, more potent, and more energy-saving electronic devices have been created as a result. The number of transistors per chip doubles every two years, according to Moore's Law, which explains why this is the case [43-45].

Traditional Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), however, suffer considerable difficulties that prevent further scaling as transistor dimensions continue to decrease. The conventional MOSFET device is getting dangerously close to its scaling limitations. There are significant problems, such as Short-Channel Effects (SCEs), that need to be addressed [46]. Because of these SCEs, the subthreshold swing (SS) goes over the basic limit of MOSFETs, which is 60 mV/decade, and as a result, the leakage current goes up. In order to bring the supply voltage of the MOSFET down to a more manageable level, the threshold voltage must be lowered. The non-scalability of SS, on the other hand, causes a greater threshold voltage, and as a result, the leakage current increases at an exponential rate. It causes problems with the supply voltage scaling, consequently resulting in higher power consumption. Researchers worldwide have developed innovative ideas for materials and device engineering approaches to solve these problems [47-50].

1.10 INTRODUCTION TO CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNTFETs)

Advancements in transistor technology have paved the way for modern electronics. The performance and scalability of conventional silicon-based transistors is constrained by the increasing need for smaller, quicker, and more energy-efficient devices. In order to support the continued development of the semiconductor industry as conventional silicon-based transistors approach their physical limits, researchers

and engineers have been looking into alternate materials and device topologies [51-52]. As a potential answer to the scaling problems facing the semiconductor industry, Carbon Nanotube Field-Effect Transistors (CNTFETs) have come to light. Immense research efforts are being poured into CNTFETs ever since their discovery for the development of next-generation devices for nanoelectronics [53-54]. A schematic diagram for CNTFET is shown in Figure 1.6.

In conclusion, CNTFET technology is of utmost importance to the electronics industry. It is a very attractive contender for the next generation of electronic devices due to its enhanced performance, capacity for scaling, adaptability, and suitability for beyond-CMOS applications [55]. Further research and development are required to overcome the unanswered questions and open the way for sophisticated, high-performance electronic systems.

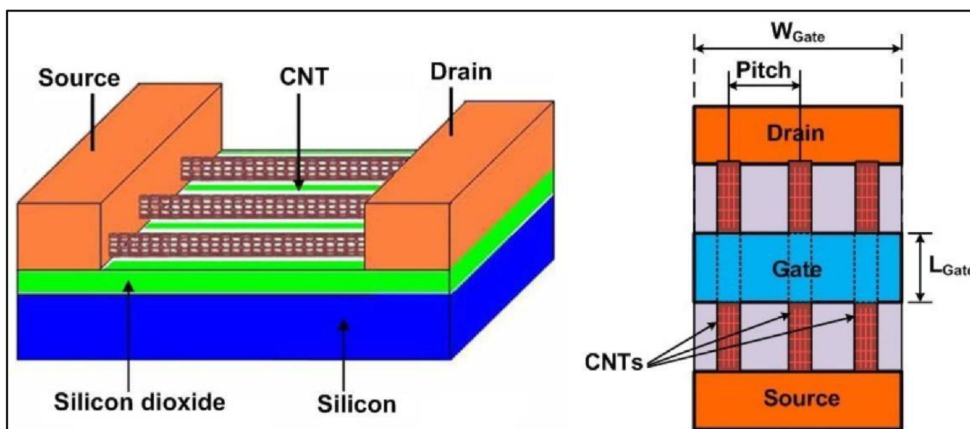

Figure 1.6: Carbon Nanotube Field Effect Transistor (CNTFET) [56]

CNTs have extraordinary electrical characteristics. They show ballistic transport, which enables electrons to pass through the CNTs without scattering, and they have high carrier mobilities, which allow electrons to move quickly across the channels [57]. CNTFETs are intriguing for high-performance and low-power electronics because of their distinctive properties.

The adaptability of CNTFETs is another significant quality. They may be configured in various transistor topologies, including single-gate and multi-gate designs. They provide circuit designers additional options when designing circuits and facilitating

integration into other electronic systems. Due to their adaptability, CNTFETs are suitable for various applications, including sensors, communication systems, memory devices, and logic circuits.

1.11 OVERVIEW AND SIGNIFICANCE OF CNTFET TECHNOLOGY

A CNTFET, as the name suggests, is a type of Field Effect Transistors (FET) that uses a CNT or arrays of CNTs in place of bulk silicon for the channel material. Source and drain electrodes are attached to it, and a gate electrode that is isolated from the CNT channel by an insulating layer regulates the current flow by altering the charge carriers in the CNT channel. The importance of CNTFETs is seen in their exceptional electrical characteristics. High carrier mobility provides for quick electron transit inside the CNT channels. Additionally, they have ballistic transport, which reduces energy waste and improves the device's functionality [54]. CNTFETs can flip between the ON and OFF states with low gate voltages, so they can function at low power levels and use relatively less power overall.

The control of electron transport through a carbon nanotube (CNT) channel by a gate voltage is crucial to the functioning of a CNTFET. The CNTFET can alternate between various operational modes by changing the gate voltage. The electrostatic potential prevents the flow of electrons from the source to the drain in the OFF state when the gate voltage is below a threshold value. The minimal gate voltage necessary to allow electron passage through the channel is known as the threshold voltage. As a result, the CNT channel experiences a high resistance condition, and barely any current flows through it. When the gate voltage is higher than the threshold in the ON state, the electrostatic potential inverts, letting the electrons pass through the CNT channel. As a result, a low resistance path is created, allowing a sizeable current to pass from the source to the drain. By regulating the gate voltage, the CNTFET can control the current flow through the channel. This characteristic leads to precise output control and easier implementation in amplifiers and logic circuits.

1.12 MULTI-GATE MOSFETs

Multi-gate MOSFETs are proposed to mitigate the SCEs through improved electrostatic control over the channel region [58]. The multi-gate structure provides better channel electrostatic control, enhancing device performance. Figure 1.7 shows the different architectures of a MOSFET.

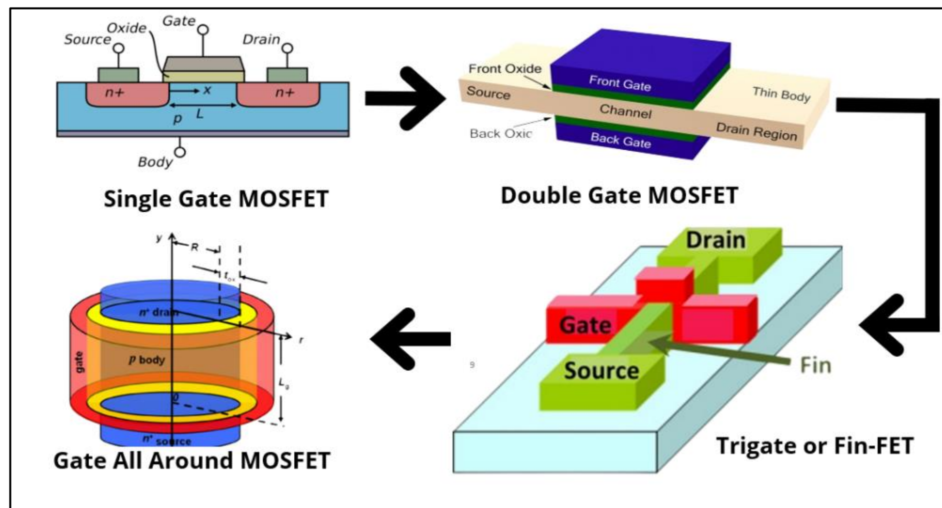

Figure 1.7: Different configurations of a MOSFET [59]

1.13 TYPES OF CNTFET

Depending on the structure and arrangement of the CNTs deployed, various CNTFETs exist. Each kind offers benefits and unique performance traits. To fully utilize the potential of these distinct CNTFET types in various applications, researchers are continually investigating and optimizing them.

1.13.1 BACK-GATED CNTFET

One of the earliest synthesized designs of CNTFET is the back-gated CNTFET, also referred to as a bottom-gated CNTFET, as shown in Figure 1.8. It features a gate electrode positioned on the substrate's reverse side, across from the area where the CNTs are forming the channel. The semiconducting CNT is deposited in between two metal strips over the substrate. These metal strips act as a source and drain. To regulate the conductivity of the channel, the gate voltage is delivered via the substrate. Back-

gated CNTFETs are relatively easy to fabricate and effectively control the resultant transistor's electrical properties. However, the resultant transistors have problems of their own. Due to inadequate contact between the gate dielectric and CNT, turning the devices ON and OFF at low voltages is difficult. Additionally, a Schottky barrier arises at the metal-semiconductor interface due to the semiconducting properties of CNT, raising the contact resistance.

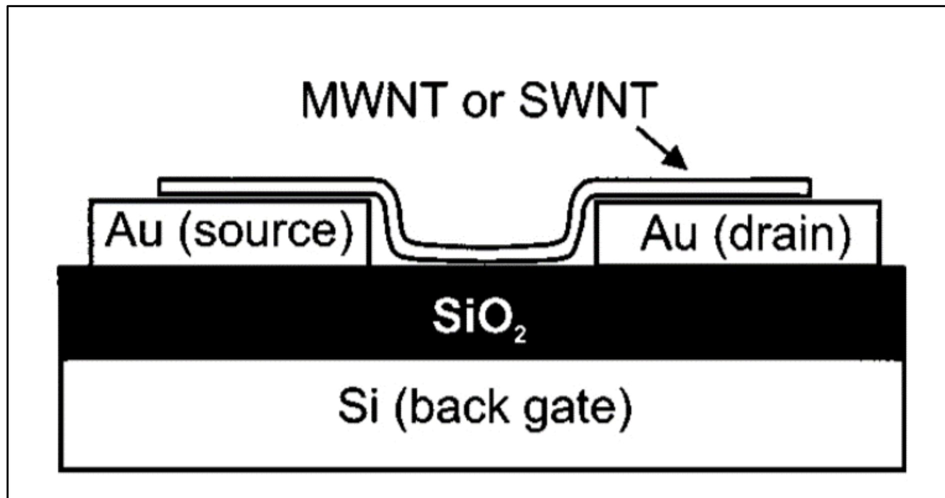

Figure 1.8: Back-Gated Carbon Nanotube Field Effect Transistor [60]

1.13.2 TOP-GATED CNTFET

In Top-Gated CNTFETs, also known as front-gated CNTFETs, the gate electrode is positioned on the top surface of the channel, as observed in Figure 1.9. The CNT channel is first deposited to a SiO_2 substrate. After that, high-resolution electron beam lithography is used to define and design the source and drain connections. The top-gate dielectric is subsequently applied to the nanotube by Atomic Layer Deposition (ALD) or evaporation. The process is completed by depositing the top gate contact on the gate dielectric.

Unlike back-gated CNTFET, the CNT channel in this configuration is immediately exposed to the gate voltage, with only a dielectric layer separating them. Compared with back-gated CNTFETs, it offers increased gate control and decreased contact resistance, thus improving device performance and reducing power consumption. It is also possible to create arrays of top-gated CNTFETs on the same wafer using this

configuration. However, manufacturing top-gated CNTFETs is difficult since it requires precise alignment between the gate and the channel.

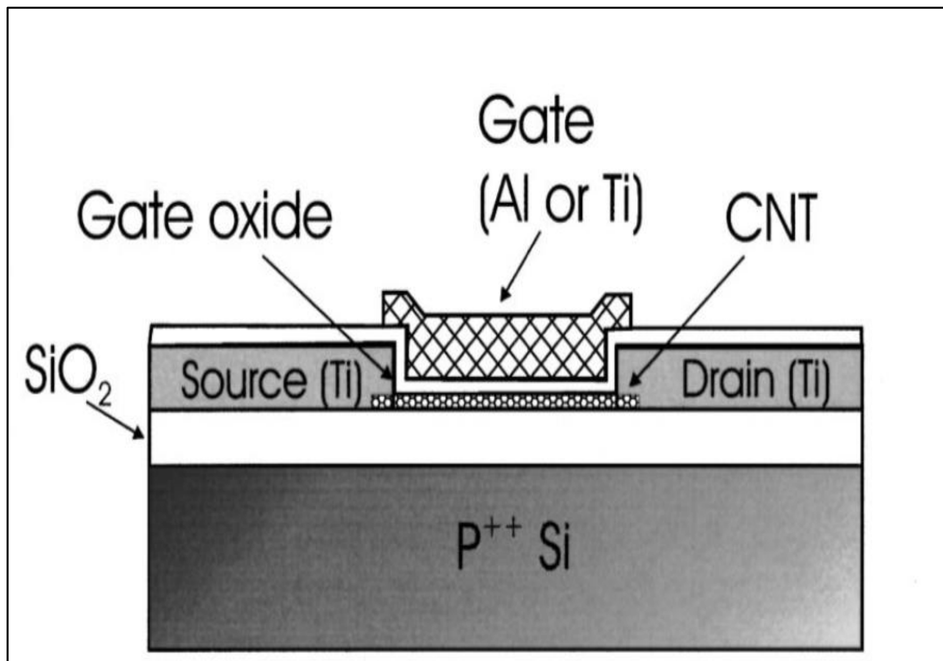

Figure 1.9: Top-Gated Carbon Nanotube Field Effect Transistor [61]

1.13.3 SUSPENDED CNTFET

In a suspended CNTFET, a CNT channel is suspended between two electrodes, which function as source and drain. The suspended arrangement reduces the impact of substrate-induced effects and improves electrostatic control over the channel. They offer improved electrical properties, such as decreased parasitic capacitance and increased carrier mobility, opening the doors for high-frequency applications.

1.13.4 GATE-ALL-AROUND (GAA) CNTFET

Gate-All-Around CNTFETs have attracted much interest lately due to their superior performance. The gate electrode wraps around the CNT channel in GAA CNTFETs, improving electrostatic control and minimizing SCEs [62]. This arrangement offers increased subthreshold swing, decreased leakage currents, and improved gate efficiency - all essential for producing high-performance transistor devices [62-64].

GAA CNTFETs are considered strong candidates for deploying advanced nanoscale technology.

1.14 WHY GATE-ALL-AROUND (GAA) CNTFET?

One of the most common CNTFET designs that have shown promise for cutting-edge nanoscale technology is the Gate-All-Around (GAA) design. Advanced nanoscale technologies, where precise channel management and enhanced electrostatics are crucial, show considerable potential for GAA CNTFETs. There are significant advantages that it offers compared to its counterparts -

- **Improved Electrostatic Control:** The GAA arrangement provides better electrostatic control over the channel region than other transistor designs. It offers improved gate-to-channel coupling as the gate electrode wraps the CNT channel, enabling accurate current flow control. Device performance is improved as a result of the increased control.
- **Suppression of Short-Channel Effects:** Short-Channel Effects become more evident as transistor dimensions reduce. These phenomena, such as threshold voltage roll-off and Drain-Induced Barrier Lowering (DIBL), can affect device performance and raise power consumption. Due to a more even distribution of the electric field throughout the channel, the GAA structure helps to counteract these effects. As a result, short-channel effects are less significant, thus increasing device scalability.
- **Scaling Potential:** Maintaining accurate control over the channel gets more difficult as transistors continue to miniaturise. The GAA structure enables superior electrostatics and gate control, even at the nanoscale levels.
- **Increased Gate Controllability:** The charge carriers in the CNT channel are regulated by gate electrodes in CNTFETs. Greater gate efficiency is achieved owing to the wider contact area offered by GAA configuration between the gate electrode and the channel.
- **Reducing Off-State Leakage:** When a transistor is OFF, leakage currents are known as off-state leakage flow or I_{OFF} from the source to the drain, unnecessarily increasing power consumption and reducing energy efficiency.

By improving channel control and reducing current leakage routes, the GAA structure contributes to reducing OFF-state leakage.

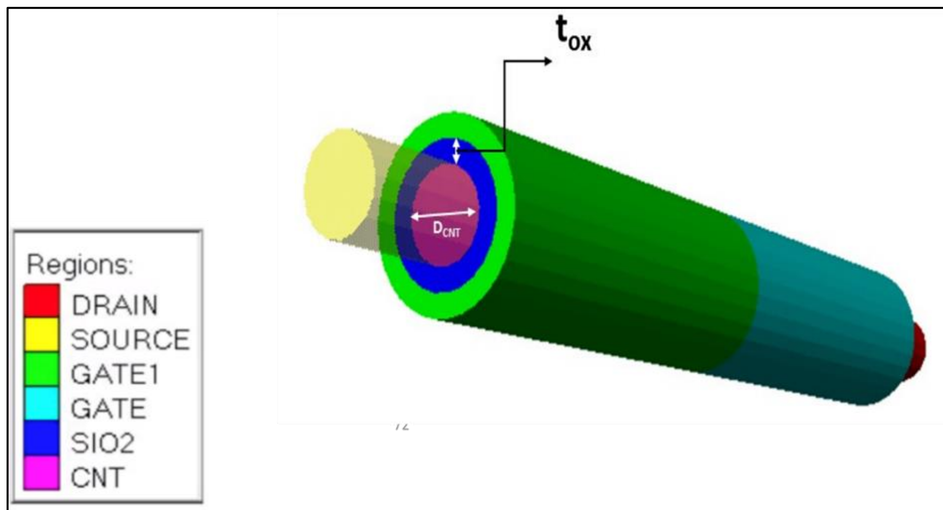

Figure 1.10: Gate-All-Around Carbon Nanotube Field Effect Transistor (GAA-CNTFET)

1.15 METHODS FOR ACHIEVING GAA GEOMETRY

The GAA geometry in CNTFETs can be achieved using a variety of techniques. The concentric architecture of GAA-CNTFET is constructed using the wrap-around process. This procedure requires the pre-treatment of a suspended CNT with trimethylaluminum vapour and NO_2 gas. The Atomic Layer Deposition ALD procedure deposits the oxide layer on the functionalized CNT. Ge et al. [65] explain how a layered oxide structure is created. The gate material is then deposited on top of the dielectric using the ALD procedure. At the ultimate end of the construction, space is provided for the gate and source metallic ends on each side. Transmission electron microscope imaging (TEM) and scanning electron microscope (SEM) imaging can be used to confirm the layers of materials deposited using ALD.

1.16 STRATEGIES FOR IMPROVING DEVICE PERFORMANCE

Device performance in GAA-CNTFETs can be improved using several techniques. Some of the most common practices currently being researched are:

1.16.1 CHANNEL ENGINEERING

Enhancing the characteristics of the CNT channel to enhance device performance can be labelled channel engineering. It is made possible by carefully controlling the CNT growth characteristics, such as alignment, chirality, and physical dimensions. For synthesis of CNTs with specific necessary properties, certain strategies can be used. The PECVD synthesis method is the most versatile method for channel engineering. The power to alter plasma parameters used in the synthesis method ensures that the resultant CNT is grown with the apt physical dimensions, ultimately affecting the device's performance.

1.16.2 GATE ENGINEERING

Gate engineering aims to improve the electrostatic control of the CNTFET by optimizing the gate structure and materials. Gate insulators can be made of high-k dielectric materials to decrease gate leakage and boost efficiency. A variety of techniques can be used to improve device performance using gate engineering –

- **HIGH-K DIELECTRIC MATERIALS**

While SiO_2 has been investigated for years and offers unprecedented robustness, its difficulties arise due to its poor scalability and low dielectric constant. To get beyond these, high-k dielectric materials are used as gate dielectrics. New-age high-k dielectric oxides such as Hafnium oxide (HfO_2), Aluminium oxide (Al_2O_3), or Zirconium oxide (ZrO_2) offer better gate capacitance and less gate leakage [66]. The CNT channel can be better electrostatically controlled owing to these materials, which improves device performance. Incorporating unconventional oxides has allowed researchers to reach beyond the last-mile optimizations that are being tried to continue to use SiO_2 still.

- **GATE WORK FUNCTION ENGINEERING**

Gate work function engineering requires choosing gate materials with appropriate work functions. The work function determines the barrier height between the gate and the CNT channel, which affects threshold voltage and charge injection efficiency. Gate Work Function Engineering can be achieved in the following ways-

- **METAL GATE ELECTRODES**

Metal gate electrodes can offer low resistance and effective charge injection into the CNT channel. Due to their advantageous work functions for CNTFET applications, metals such as gold (Au), platinum (Pt), or tantalum nitride (TaN) are frequently used as gate electrodes. Metal gate electrodes facilitate efficient control over the gate potential, enabling quicker charge carrier modulation and improved switching characteristics.

- **MULTI-MATERIAL GATES**

Deploying multi-material gates is an effective way to boost device performance. Gates can comprise several layers of various materials, each with a particular function. A multi-metal gate stack, for instance, can use several metals to succeed at work function engineering [67]. A metal/high-k dielectric/metal (MHM) gate construction can also be used - which offers low resistivity and efficient charge injection, while the high-k dielectric layer improves gate capacitance. There are a variety of multi-material gate architectures that are being investigated by academics, of which the following two hold the most significance -

Dual Material Gate: In a dual material gate, two distinct materials with different work functions are included in the gate stack, as seen in Figure 1.11. With this method, the gate work function can be altered as needed, leading to better electrostatic control and increased device performance. Typically, the bottom layer of the gate stack is made of a high-work-function metal, while the top layer is made of a low-work-function metal. While the high-work-function metal layer facilitates improved carrier injection and lowers contact resistance, the low-work-function metal layer aids in reaching the necessary threshold voltage and optimizing the channel properties. The work function of the gate can be accurately adjusted, providing effective control over the transistor

functioning and improving performance by carefully selecting the materials and their corresponding thickness.

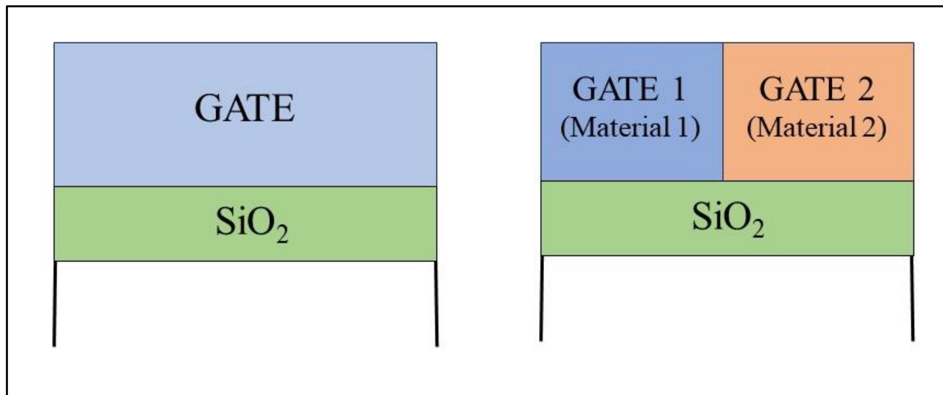

Figure 1.11: Single and Dual Material Gate Architecture

Triple Material Gate: By utilizing three distinct materials in the gate stack, triple material gates extend the above-mentioned concept. This new configuration offers even more refined control over the work function and allows for greater device performance optimization. A high-work-function metal layer, a low-work-function metal layer, and an intermediate layer are the conventional components of the triple-material gate stack.

1.16.2.1 ADVANTAGES OF MULTI-MATERIAL GATES

- **Improved Work Function Control:** The work function of the gate can be accurately altered by selectively using multiple materials, enabling superior optimization of the transistor's threshold voltage and enhancing overall performance.
- **Reduced Contact Resistance:** Integrating various materials improves device efficiency by lowering contact resistance at the metal-CNT interface. This improves carrier injection.
- **Enhancing I_{ON}/I_{OFF} Ratio and Improving Device Switching Characteristics:** Multiple material gates offer improved electrostatic control over the channel area.
- **Performance of the Device Can Be tailored to Specific Performance Requirements:** The flexibility provided by material and triple material gates

enables the device performance to be tailored to particular application and performance requirements, such as low-power operation, high-speed switching, and increased reliability.

1.16.3 GATE AND DIELECTRIC LAYER DIMENSIONS

When optimizing GAA-CNTFETs, gate, and dielectric layer dimensions are also critical. Gate capacitance, gate leakage, and electrostatic control are all impacted by the thickness of the gate insulator. Gate leakage may be reduced, and gate efficiency can be increased by altering the dielectric layer thickness. The width and length of the gate also affect the gate control and device characteristics.

1.17 DESIGN FACTORS FOR LOW-POWER AND HIGH-FREQUENCY APPLICATIONS

There is much promise for high-frequency and low-power applications with GAA-CNTFETs. Hence, design considerations are critical. Minimizing parasitic capacitance and resistance is crucial in high-frequency applications. High-frequency performance can be enhanced by altering the channel's length and width, reducing source/drain contact resistance, and using low-loss dielectric materials. Furthermore, decreased gate capacitance and enhanced gate control allow quicker switching rates and improved frequency responsiveness. For low-power applications, off-state leakage current reduction is essential. Utilizing high-k materials with low leakage properties and enhancing the dielectric gate thickness is critical for efficiently utilizing GAA-CNTFET for low-power applications.

1.18 APPLICATIONS OF CNTFET

By incorporating an unconventional channel material, CNTFETs are the number one candidate to take conventional CMOS technology forward. With the distinct properties that CNTs bring to the table, CNTFETs can serve a wide variety of applications, with more being researched with heavy focus.

They match their unprecedented electrical conductivity with superior thermal conductivity, thus giving rise to potentially game-changing applications in the future.

For the scope of this research, wireless communications, biosensing applications, and sensors in high-temperature environment are explored for CNTFET's applications.

1.18.1 WIRELESS COMMUNICATIONS

Before enlisting the innumerable benefits that CNTFETs offer in wireless communications, it is important to fully understand the scope of wireless communications where CNTFETs can be desirable for deployment.

Mobile Communication is one of the primary domains within wireless communications where CNTFETs can provide value. They can improve the effectiveness and efficiency of mobile communication systems. CNTFETs can also increase the functionality of Wi-Fi routers and access points. They can also find their place in radio frequency (RF) front-end circuits of wireless networking systems to improve signal reception and transmission. The versatile offered by CNTFETs makes them viable for satellite communications as well. There are a wide variety of applications that CNTFETs can serve on satellites.

The rapidly developing and quickly rising popularity of 5G connectivity and IoT technologies can also benefit from deploying CNTFETs. Any advancement in connectivity requires ultra-fast data transmission, reduced latency, and enhanced network capacity, all of which are strong suits of CNTFETs.

To correctly understand how CNTFETs can play such a crucial role in the wide variety of wireless communication applications, it is important to dive deep into the distinct properties that make them suitable for the same -

- **High-Speed Operation**: Special characteristics of CNTs, such as high carrier mobility and quick switching rates, make them an ideal candidate for high-speed operations, especially for quick signal processing and transmission.
- **Low power consumption**: The high ON/OFF current ratio offered by CNTFETs and the ability to run at lower supply voltages result in an energy-efficient operation.

- **Frequency Range**: The ability of CNTFETs to work over a broad range of frequencies, including millimetre- and microwave frequencies, makes them ideal for all sorts of wireless communication applications, as mentioned above.

1.18.2 SENSING APPLICATIONS

CNTFETs can be deployed as sensors in various industries due to their nanoscale architecture and high sensitivity. The ability to detect and react quickly to external circumstances makes them a top candidate for usage in industries where super-fast detection is necessary. The possible applications with CNTFET include –

- **GAS SENSING**

The electrical characteristics of the CNTFET are altered due to the interaction between gas molecules and the nanotube surface, enabling the identification and measurement of gases. Selective gas sensing can be accomplished by functionalizing the surface of the CNTFET with specific gas-sensitive materials. Mostly they are used as gas sensors for workplace safety and gas leakage detectors.

- **ENVIRONMENTAL MONITORING**

CNTFET sensors can monitor the environment, detecting poisons, pollutants, and dangerous materials. Early warning systems and pollution management require great sensitivity, thus making them a fit for CNTFETs.

1.18.3 BIOSENSING APPLICATIONS

CNTFETs are highly suited for game-changing biosensing applications. The surface sensitivity is better than most conventional materials, thus helping in realizing devices that can detect diseases, changes, and more early.

One possible way CNTFETs achieve bio-sensing capabilities is by etching a nanogap cavity inside the oxide layer of the device. When bio-molecules get immobilized in the nanogap cavity, it changes the overall dielectric constant of the oxide region, thus affecting the device's electrical properties.

The desired molecule can be identified by measuring the change in electrical properties.

Following are some more details on the benefits of CNTFETs in biosensing:

- **High Sensitivity and Selectivity**: CNTFETs are very responsive to environmental changes, including interactions with biological molecules. The detection and analysis of certain biomarkers, proteins, DNA sequences, or cells are only made possible because of the high sensitivity offered by CNTFETs.
- **Scalability**: CNTFET-based biosensors can be manufactured at the nanoscale level, making it possible to miniaturize and integrate them with portable and point-of-care devices. The creation of extremely sensitive and selective biosensing platforms is only made possible by the size of CNTFETs.

1.18.4 SENSORS IN HIGH-TEMPERATURE AND HIGH-ENDURANCE ENVIRONMENTS

CNTFETs also exhibit exceptional chemical resistance, thermal conductivity, and stability alongside supreme electrical conductivity. The outstanding thermal stability enables them to keep their structural integrity and electrical performance even at high temperatures. This makes them an excellent candidate for sensing applications where temperatures can reach severe levels, such as aerospace, automotive, power generation, and combustion. Their ability to operate over a large temperature range allows them to function at high-temperature extremes, low-temperature extremes and ambient temperatures. This makes them very useful for thermal management systems and combustion monitoring systems.

Outstanding chemical resistance implies they can endure contact with corrosive gases or liquids. Due to this, they may be used for sensing applications in extreme, high-endurance settings such as chemical plants, industrial operations, and oil and gas exploration.

In conclusion, CNTFETs have opened the route for unprecedented applications. Researchers can create cutting-edge solutions for wireless communication systems and

sensing applications, which has opened the route for more acceptance of CNTFET as a replacement for conventional devices.

1.19 ORGANIZATION OF THESIS

Chapter 1 – This chapter gives an insight into the basics of Carbon Nanotube (CNT) and their relevance. It throws light on their structure, basic properties, production methods, and the various applications under research. The Plasma Enhanced Chemical Vapor Deposition (PECVD) method has been elaborated on in detail in this chapter. The advantages it holds over other synthesis methods have also been identified. This chapter also discusses Carbon Nanotube Field Effect Transistors (CNTFETs) – their benefits, types, and applications. This chapter also touches upon the various possible configurations of CNTFET, with special emphasis on Gate-All-Around geometry.

Chapter 2 – This chapter intends to highlight the effect of plasma parameters on the performance metrics of the simulated Plasma-Assisted Vertically Aligned Dual-Metal Carbon Nanotube Field-Effect Transistor (VA-DMCNFET) device. A vertically aligned semiconducting CNT synthesized using Plasma-Enhanced Chemical Vapor Deposition (PECVD) technique is implemented as the channel. The proposed device significant improves performance over conventional Nanowire Field-Effect Transistor (NWFET). Next, the device geometry and electrical properties are related to the plasma parameters through a physical model. The DC and analog performance of VA-DMCNFET at various plasma parameters corresponding to different values of CNT channel radius (for fixed CNT channel length) and different values of CNT channel length (for fixed CNT channel radius) is analyzed. It is observed that lower values of plasma parameters are essential for higher values of drain current, transconductance, output conductance, cutoff frequency, and lower values of threshold voltage and channel resistance.

On the other hand, higher values of plasma parameters are essential for better I_{ON} / I_{OFF} current ratio, early voltage, and gain of the proposed device. By altering the plasma parameters, the device's efficiency can be improved, leading to better real-life applicability and performance. The study’s results have been assessed and compared with the existing experimental observations which accredit the proposed mechanisms.

Chapter 3 – This work intends to improve the previously simulated device by replacing the conventional SiO_2 gate oxide with a stacked structure featuring a high-k oxide HfO_2. The resultant novel device, known as Plasma-Assisted Dual-Material Stacked Gate-Oxide Carbon Nanotube Field Effect Transistor (DM-SGCNFET), is put under observation for a variety of analyses. The stacked gate oxide helps to circumvent the performance and downscaling problems associated with SiO_2. The performance metrics of the simulated device are compared with a SiO_2-based similar device (DM-CNFET) for varying sets of plasma parameters that correspond to different values of channel length. The comprehensive analysis highlights the improvements in performance metrics of DM-SGCNFET over DM-CNFET. The chapter further explores the DM-SGCNFET device for linearity distortion performance by evaluating g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point for altering values of plasma parameters.

Chapter 4 –This study aims to implement a Hafnium Oxide (HfO_2) based Plasma-Assisted Gate All Around Carbon Nanotube Field Effect Transistor (GAA-CNTFET) and use it for a better understanding of plasma parameters and their effect on the device. A comparative analysis has been performed, based on which it can be concluded that using HfO_2 improves in all observed performance metrics—higher drain current, transconductance, output conductance, early voltage, and gate capacitance. The critical component of this chapter is the analysis done towards the device's sensing abilities. By implementing a cavity in the oxide layer and utilizing the concept of dielectric modulation, the device was tested for sensing applications for different molecules with different dielectric constants. The results of this chapter can help quantify the practical deployment of the device as biosensors, gas sensors, and more.

Chapter 5 – The research investigates the practical applications of devices incorporating CNTs. In order to cover the relevant bases, two devices featuring PECVD-grown CNT as channel material are being investigated for two different applications – the DM-CNFET for sensing applications and DM-SGCNFET for high frequency and wireless applications under temperature variations and high-temperature values. The simulated device's performance is investigated under varying

temperature ranges ranging from 300K – 500K at steps of 50 K each. RF, analog, and linearity analysis are performed to investigate the impact of temperature change on wireless communications more thoroughly.

Chapter 6 – The last chapter incorporates the conclusion and the future scope of this research. The work performed in the present thesis is not limited to designing and simulating the Plasma-Assisted CNTFET but also assessing the applications of the simulated device. This chapter also includes the future work that can be performed to study Plasma-Assisted CNTFET more thoroughly and efficiently to make its production more accessible and enhance its applications in various fields.

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Chapter 2

PLASMA-BASED NANOARCHITECTONICS FOR VERTICALLY ALIGNED DUAL-METAL CARBON NANOTUBE FIELD EFFECT TRANSISTOR (VA-DMCNFET) DEVICE: EFFECT OF PLASMA PARAMETERS ON TRANSISTOR PROPERTIES

Publications

1. **Mansha Kansal** and Suresh C. Sharma, "Plasma-based nanoarchitectonics for vertically aligned dual-metal carbon nanotube field-effect transistor (VA-DMCNFET) device: effect of plasma parameters on transistor properties". Appl. Phys. A 128, 28 (2022).

2. **Mansha Kansal** and Suresh C. Sharma, "Impact of PECVD characteristics on metrics of a Plasma-Assisted Vertically Aligned Carbon Nanotube FET (VA-CNTFET) device," 2022 IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience & Nanotechnology (5NANO), 2022.

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PLASMA-BASED NANOARCHITECTONICS FOR VERTICALLY ALIGNED DUAL-METAL CARBON NANOTUBE FIELD EFFECT TRANSISTOR (VA-DMCNFET) DEVICE: EFFECT OF PLASMA PARAMETERS ON TRANSISTOR PROPERTIES

2.1 BRIEF OUTLINE

In this chapter, we intend to show the role of plasma parameters on the performance of the simulated device Plasma-Assisted Vertically Aligned Dual-Metal Carbon Nanotube Field-Effect Transistor (VA-DMCNFET) for the first time. Here, vertically aligned semiconducting Carbon Nanotube (CNT) synthesized using Plasma-Enhanced Chemical Vapor Deposition (PECVD) technique is implemented as the channel. The proposed device shows significant improvement in performance over conventional Nanowire Field-Effect Transistor (NWFET). Next, the device geometry and electrical properties are related to the PECVD parameters by means of a physical model. The DC and analog performance of VA-DMCNFET at various plasma parameters corresponding to different values of CNT channel radius (for fixed CNT channel length) and different values of CNT channel length (for fixed CNT channel radius) is analyzed. It is observed that lower values of plasma parameters are essential for higher values of drain current, transconductance, output conductance, cutoff frequency, and lower values of threshold voltage and channel resistance. On the other hand, higher values of plasma parameters are essential for better I_{ON}/I_{OFF} current ratio, early voltage, and gain of the proposed device. By altering the plasma parameters, efficiency of the device can be improved leading to better real-life applicability and performance. The results obtained from this study have been verified with the existing experimental observations for validation of chosen mechanisms.

2.2 INTRODUCTION

The semiconductor industry is faced with a daunting problem that has invited extensive research so far–reduce the physical dimensions while improving the performance of the device [1]. The scaling limitations in silicon are being considered by integration of non-conventional high mobility channel materials [2, 3]. Carbon Nanotube (CNT) has been extensively researched lately with the same intention. CNTs are characterized as graphitic filaments which have a cylindrical shape of radius in the nanometer scale and length in the micrometer range [4, 5]. CNTFETs were first showcased in 1998 [6]. Since then, they have been the subject of significant research interest leading to significant progress in understanding device physics and in enhancing transistor performance due to high-speed operation of CNT [7, 8]. The CNTFETs show superior device performance in comparison with existing silicon-based devices because of ballistic transport in the single-walled CNTs. The Plasma-Enhanced Chemical Vapor Deposition (PECVD) technique gives birth to vertically aligned carbon nanostructures. Growth of vertically aligned CNT is due to the electric field of the plasma sheath which applies force on the nanostructure, leading to growth in a vertical direction [9–14]. PECVD technique stands out from the rest because the resultant CNTs produced have a high semiconductive CNT ratio leading to higher values of drain current [15]. Since CNTFETs are involved in a wide range of applications, the said ratio is of paramount importance. For CNTs synthesized using PECVD, this can be as high as 90% [16, 17]. Plasma-based nanoarchitectonics deal with the production of systems from plasma-based nanoscale objects. Nanoarchitectonics will yield application opportunities ensuring these nanomaterials benefit our day-to-day lives. Mizutani et al. [18] have fabricated CNTFETs using the grid inserted PECVD technique. The horizontally aligned nanotubes were used as a channel. With a channel length of 7 μm and channel width of 30 μm, they were able to obtain an ON/OFF current ratio of 10^3 and good pinch-of characteristics. Bashir et al. [19] have proposed a novel device of Schottky barrier metal–oxide–semiconductor field effect transistor (MOSFET), where Hafnium creates charge plasma in the undoped silicon. Due to the employment of charge plasma concept, various properties like I_{ON}/I_{OFF} current ratio, ON current, cutoff frequency have significantly improved.

In this chapter, for the first time, the role of plasma parameters on the performance of the simulated Assisted Vertically Aligned Dual-Metal Carbon Nanotube Field Effect Transistor (VA-DMCNFET) with cylindrical dual metal surrounding gate is studied. From the obtained results, it can be observed that VA-DMCNFET shows better performance over Nanowire Field-Effect Transistor (NWFET). It is further shown that lower values of plasma parameters are essential for higher values of drain current, transconductance, output conductance and cutoff frequency, and lower values of threshold voltage and channel resistance. On the other hand, higher values of plasma parameters are essential for better values of I_{ON}/I_{OFF} current ratio, early voltage, and gain of the proposed device. Hence, finding the right balance between the appropriate plasma parameters becomes important for optimum device performance.

2.3 DEVICE SIMULATION

The proposed device Plasma-Assisted Vertically Aligned Dual-Metal Carbon Nanotube Field-Effect Transistor (VA-DMCNFET) is simulated. The carbon nanotubes have been experimentally synthesized via microwave PECVD using a mixture of argon and methane gases on nickel coated and silicon substrates [20]. Figure 2.1 and Figure 2.2 represent the 3-D and cross-sectional view of VA-DMCNFET, respectively. Figure 2.3 represents the contour plot of potential with V_{ds} = 0.0 V and V_{gs} = 0.0 V. The cylindrical dual-metal gate FET has the gate with the lower work function at the drain side, and gate with the higher work function on the other side. The structure parameters of VA-DMCNFET are enlisted in Table 2.1. The silicon dioxide (SiO_2) is used as the gate dielectric. The doping concentration, N_d, for source(n+)-drain(n+) is 10^{18} cm^{-3}. The simulations are run on ATLAS 3D device simulator using the models listed as follows. MUN and MUP parameters in ATLAS 3D device simulator have been used to set constant values for electron and hole mobilities. The Shockley–Read–Hall (SRH) model is used to simulate the leakage currents. The Auger recombination model is also used to consider minority carrier recombination. Boltzmann model is used for considering the carrier statistics. Lastly, Gummel and Newton techniques have been used for the numerical solutions [22].

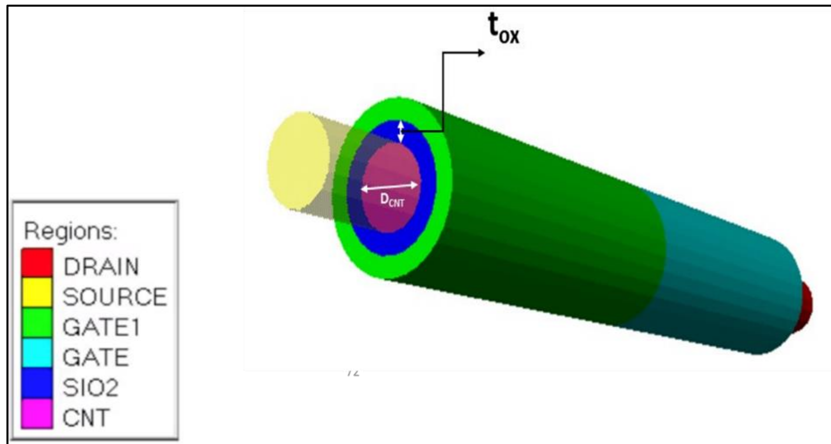


Figure 2.1: 3-D structure of cylindrical VA-DMCNFET

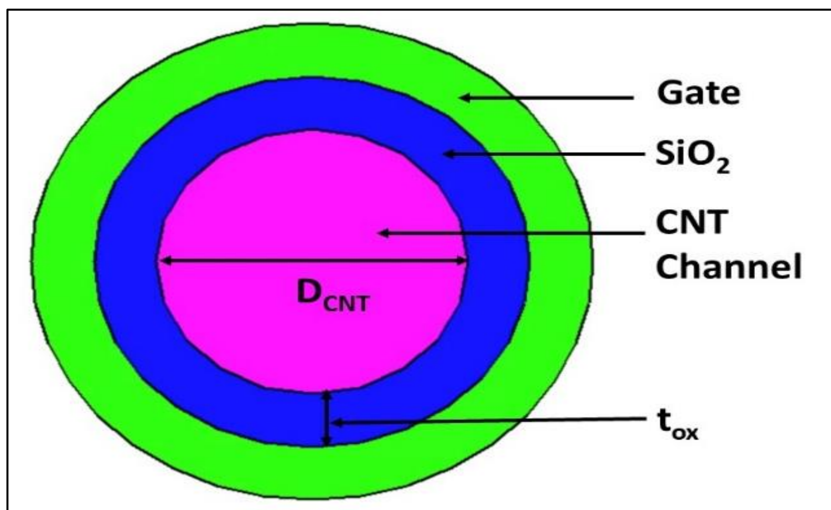


Figure 2.2: Cross Sectional view of VA-DMCNFET

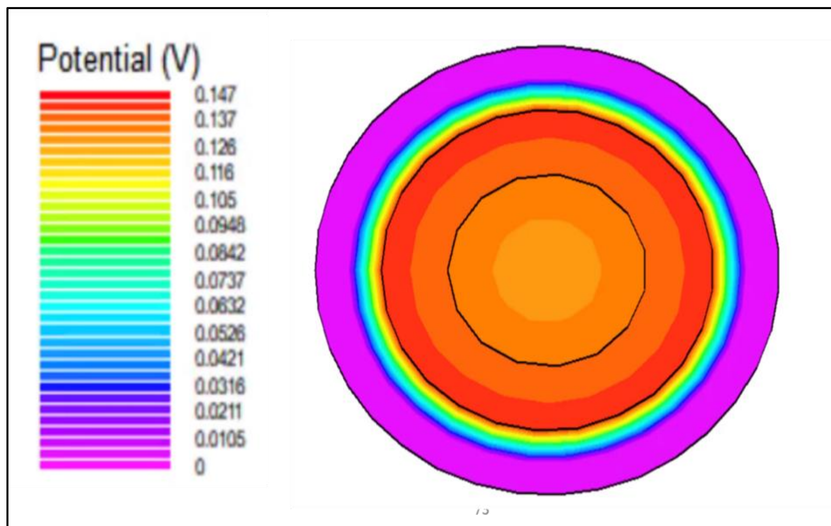


Figure 2.3: Potential contour profile of VA-DMCNFET with V_{ds}= 0.0 V and V_{gs}= 0.0 V

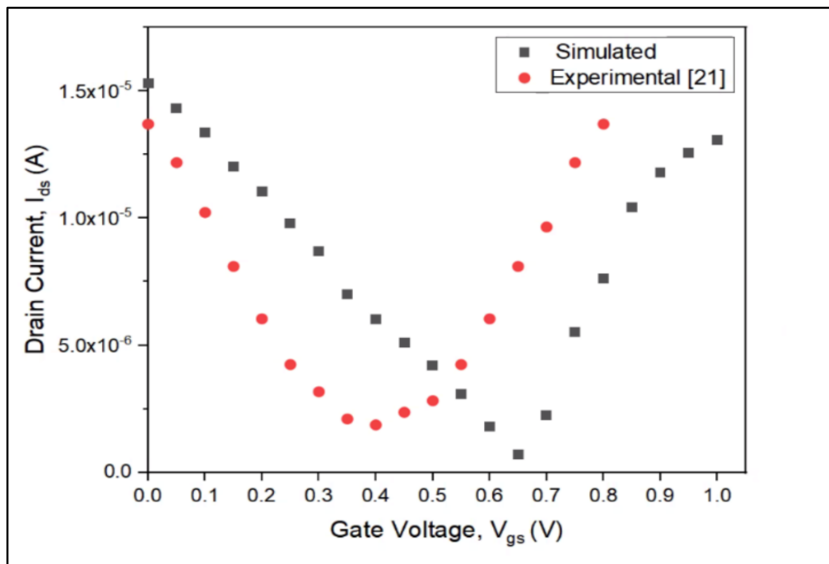


Figure 2.4: Calibration of simulation results with experimental data at $V_{ds} = 0.8$ V

Figure 2.4 shows that the results of the simulated device showcase trends similar to the published research work of Yang et al. [21]. The absolute values, however, cannot be compared owing to minor differences in configuration of the two devices.

Table 2.1: Device Specifications

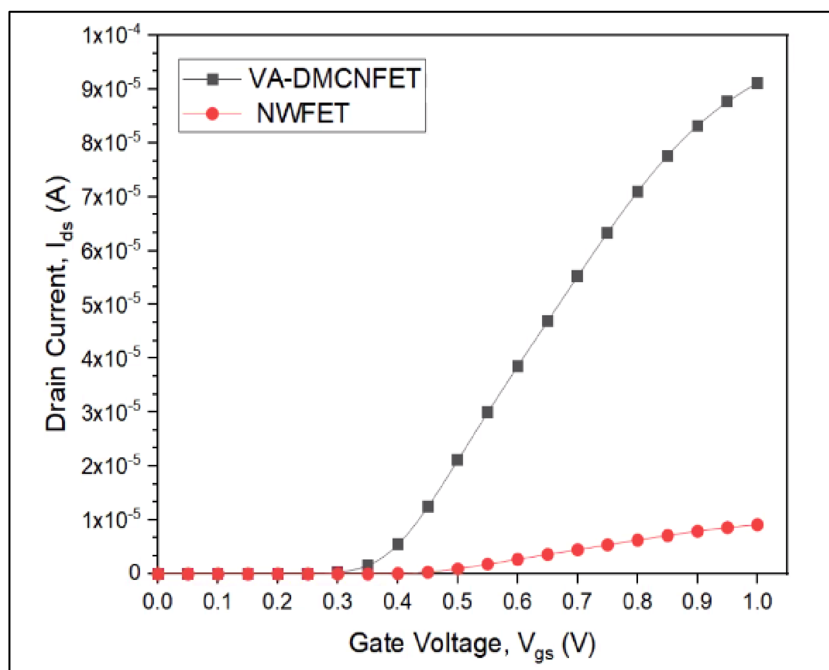
Parameter	Symbol	Value(s)
Channel Length (µm)	L	1,2,3 (at fixed channel radius)
Channel Radius (nm)	R	2,3,4,5 (at fixed channel length)
Silicon dioxide thickness (nm)	t_{ox}	2
Source/ Drain Length (nm)	L_s/L_d	14
Gate metal work function (eV)	ϕ_1 , ϕ_2	4.4, 4.7
Oxide Permittivity	ε_{ox}	3.9

2.4 RESULTS AND DISCUSSION

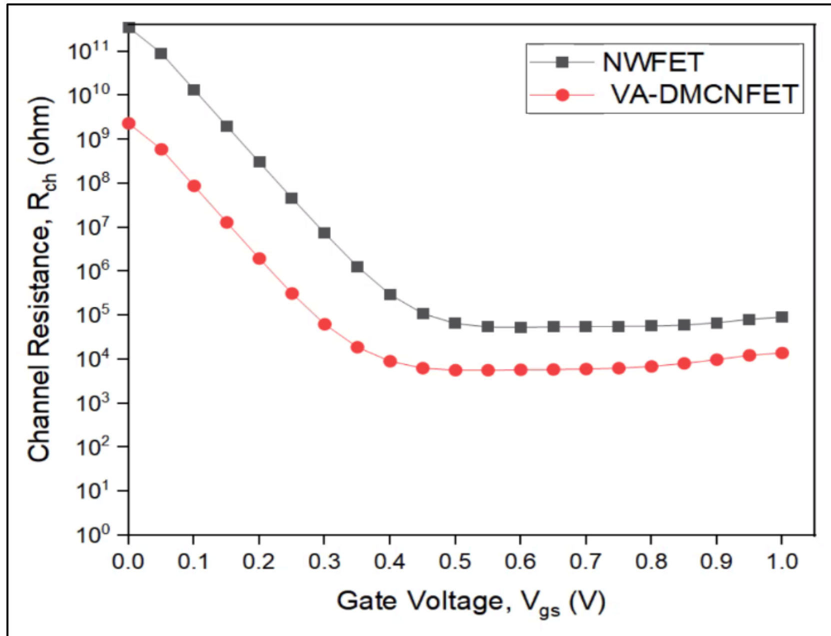
The structure and characteristics of the device are developed and extracted, respectively, via SILVACO 3D ATLAS TCAD simulator.

2.4.1 PERFORMANCE COMPARISON BETWEEN VA-DMCNFET AND NWFET

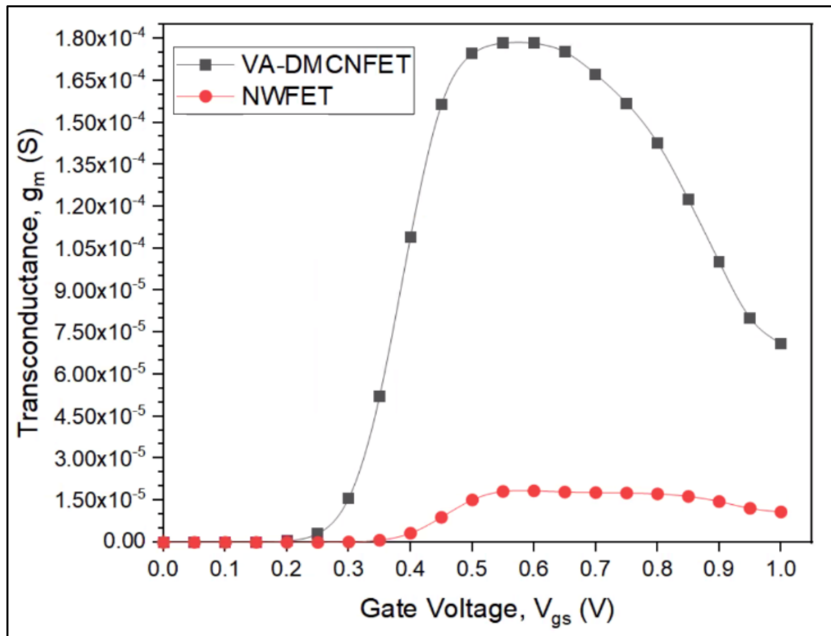
In Figure 2.5, the performance of VA-DMCNFET has been compared against NWFET, with both devices having same geometry and constant parameters (L = 100 nm). The results improve drastically with the inclusion of CNT as channel when compared to the conventional silicon channel owing to excellent electrical properties of CNT. Figure 2.5 (a) shows transfer characteristics of the VA-DMCNFET and NWFET, and it can be seen that VA-DMCNFET exhibits higher ON state current (I_{ds} at V_{gs} = 1.0 V for constant V_{ds} = 0.5 V) as compared to NWFET. Furthermore, the VA-DMCNFET exhibits lower channel resistance than NWFET, ensuring high current drive as can be seen from Figure 2.5 (b). It can also be observed that there is achievement of lower threshold voltage in VA-DMCNFET than NWFET. Due to lower threshold voltage, the proposed device gets turned on at a lower gate voltage as compared to NWFET. The extremely high carrier mobility in the CNT in VA-DMCNFET provides high transconductance and operating speed for CNT-based FETs as can be seen from Figure 2.5 (c) [23].



(a)



(b)



(c)

Figure 2.5: Comparison between proposed device VA-DMCNFET and NWFET having same parameters: Variation in (a) Drain current I_{ds} with gate voltage V_{gs} (b) Channel Resistance R_{ch} with V_{gs} (in log scale) (c) Transconductance gm

2.4.2 EVALUATING ROLE OF PLASMA PARAMETERS ON THE PERFORMANCE OF VA-DMCNFET

Through the means of physical model as shown by Sharma et al. [9], the device geometry and electrical properties of VA-DMCNFET are related to the PECVD parameters. Precise control of the channel radius is a critical predicament for the success of any CNT-based device technology. Channel radius of the CNTFET has a strong impact on the band gap of the semiconducting CNT channel, which further influences various properties of the device [24, 25]. The value of CNT radius decreases with increase in values of plasma parameters: electron density n_{eo} and electron temperature T_{eo}, ion density n_{io} and ion temperature T_{io}. For a given set of plasma parameters, CNT radius increases initially with time, till a saturation value is achieved. As n_{eo} and T_{eo} increase, positively charged ions and electrons are created at the expense of neutral atoms due to ionization of neutral atoms. Because the accumulation of neutral atoms leads to growth of CNT, the gradual reduction in the density of neutral atoms with increasing values of plasma parameters leads to a decrease in the radius of the CNT [9, 28]. It becomes quintessential to optimize various plasma parameters for optimum device performance, considering they can directly affect the geometry of the synthesized CNT device. Plasma parameters control the CNT channel radius and CNT channel length which further gives them control over the conductivity of the channel, gate controllability, contact resistance and other electrostatics.

In this part, we intend to understand how these plasma parameters influence various properties of the device. This research breaks down the variation in plasma parameters into two sets:

Set 1: Variation in plasma parameters corresponding to different values of channel radius for a fixed value of channel length. The channel radius which correlates with the chosen value of plasma parameters varies from 2 to 5 nm (cf. Table 2.2).

Set 2: Variation in plasma parameters corresponding to different values of channel length for a fixed value of channel radius. The channel length which correlates with the chosen value of plasma parameters varies from 1 to 3 μm (cf. Table 2.3).

Table 2.2: Variation of Plasma parameters: n_{eo} and T_{eo}, n_{io} and T_{io} with channel radius (For a fixed value of channel length = 100 nm)

Case	Channel Radius (nm)	Plasma Parameter 1 (electron density n_{eo} in cm^{-3})	Plasma Parameter 2 (electron temperature T_{eo} in eV)	Plasma Parameter 3 (ion density n_{io} in cm^{-3})	Plasma Parameter 4 (ion temperature T_{io} in Kelvin)
1	2	10^7	0.5	$5x10^6$	2400
2	3	$5x10^6$	0.45	$4.2x10^6$	2300
3	4	10^6	0.4	$2.5x10^6$	2200
4	5	10^5	0.3	10^6	2100

Table 2.3: Variation of Plasma parameters: n_{eo} and T_{eo}, n_{io} and T_{io}, with channel length (For a fixed value of channel radius = 5 nm)

Case	Channel Length (µm)	Plasma Parameter 1 (electron density n_{eo} in cm-3)	Plasma Parameter 2 (electron temperature T_{eo} in eV)	Plasma Parameter 3 (ion density n_{io} in cm-3)	Plasma Parameter 4 (ion temperature T_{io} in Kelvin)
1*	1	$5x10^8$	1.1	$5x10^7$	2180
2*	2	10^9	1.2	$5x10^8$	2210
3*	3	$5x10^9$	1.3	10^9	2250

The value of channel radius and channel length pertaining to the chosen plasma parameters is mentioned as follows. Based on the existing knowledge of Plasma Physics, surface potential is given by

$$V_s = \frac{-2e}{L} \times log(\frac{\lambda_d}{R}) \tag{2.1}$$

where e = electronic charge and λ_d = Plasma Debye length. Hence, value of channel radius R can be written as

$$R = e^{\frac{V_s L}{2e}} \lambda_d \tag{2.2}$$

Also,

$$\frac{1}{\lambda_d^2} = \frac{1}{\lambda_e^2} + \frac{1}{\lambda_i^2}$$

where λ_e= electron plasma Debye length, λ_i = ion plasma Debye length and can be written as

$$\lambda_e = \sqrt{\frac{T_{eo}}{4\pi n_{eo} e^2}} \quad and \quad \lambda_i = \sqrt{\frac{T_{io}}{4\pi n_{io} e^2}} \tag{2.3}$$

And

$$R^2 = e^{\frac{V_s L}{e}} \left[\frac{\lambda_e^2 \lambda_i^2}{\lambda_e^2 + \lambda_i^2} \right] \tag{2.4}$$

Putting the values of λ_e and λ_i , Eq. (2.4) can be rewritten as

$$R^2 = e^{\frac{V_s L}{e}} \left[\frac{1}{\frac{4\pi n_{eo} e^2}{T_{eo}} + \frac{4\pi n_{io} e^2}{T_{io}}} \right]$$

Or

$$R^2 = e^{\frac{V_s L}{e}} \left[\frac{1}{4\pi e^2 (\frac{n_{eo}}{T_{eo}} + \frac{n_{io}}{T_{io}})} \right] \tag{2.5}$$

The band gap of CNT channel can be defined as [26]:

$$E_g = \frac{2a_o E_\pi}{D_{CNT}} \tag{2.6}$$

where E_g = tight-binding parameter, a_o = carbon–carbon distance in CNT structure and D_{CNT} = diameter of CNT. By inserting the value of radius of CNT from Eq. (2.7), we obtain

$$E_g = a_o E_\pi e^{\frac{-V_s L}{2e}} \sqrt{4\pi e^2 \left[\frac{n_{eo}}{T_{eo}} + \frac{n_{io}}{T_{io}}\right]}$$

We can write the above equation as –

$$E_g = k e^{\frac{-V_s L}{2e}} \sqrt{\frac{n_{eo}}{T_{eo}} + \frac{n_{io}}{T_{io}}} \quad (2.7)$$

where $k = a_o E_\pi \sqrt{(4\pi e^2)}$

Threshold voltage can be defined as:

$$V_{th} \approx \frac{E_g}{2e} = \frac{a_o E_\pi}{e D_{CNT}} = \frac{a_o E_\pi}{2eR} \quad (2.8)$$

(without considering DIBL effect)

The drain current in the linear regime is :

$$I_{ds} = \frac{\mu C}{L^2} V_{ds} (V_{gs} - V_{th}) \quad (2.9)$$

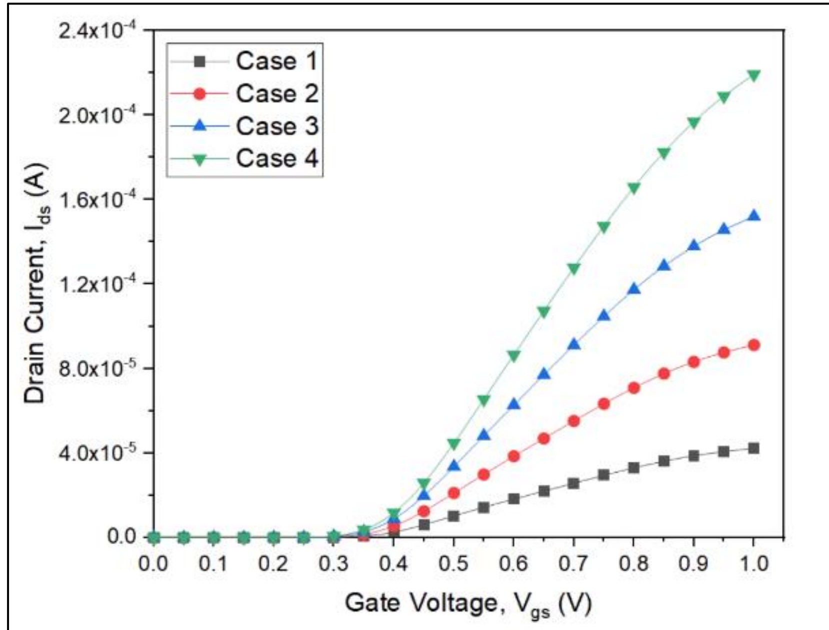
C= Capacitance of the CNT and μ=apparent mobility in linear regime.

By substituting the value of R from Eq. (2.5) in Eqs. (2.7–2.9), for the first time, the relation between the above-mentioned properties, e.g., band gap, threshold voltage can be obtained in terms of plasma parameters. The transfer characteristics for different values of plasma parameters that correspond to different values of channel radius (for a fixed value of channel length) at V_{ds} = 0.5 V are shown in Figure 2.6 (a) and for different values of channel length (for a fixed value of channel radius) are shown in Figure 2.6 (b). The output characteristics for different values of plasma parameters that correspond to different values of channel radius (for a fixed value of channel length) are shown in Figure 2.7 (a) and for different values of channel length (for a fixed value

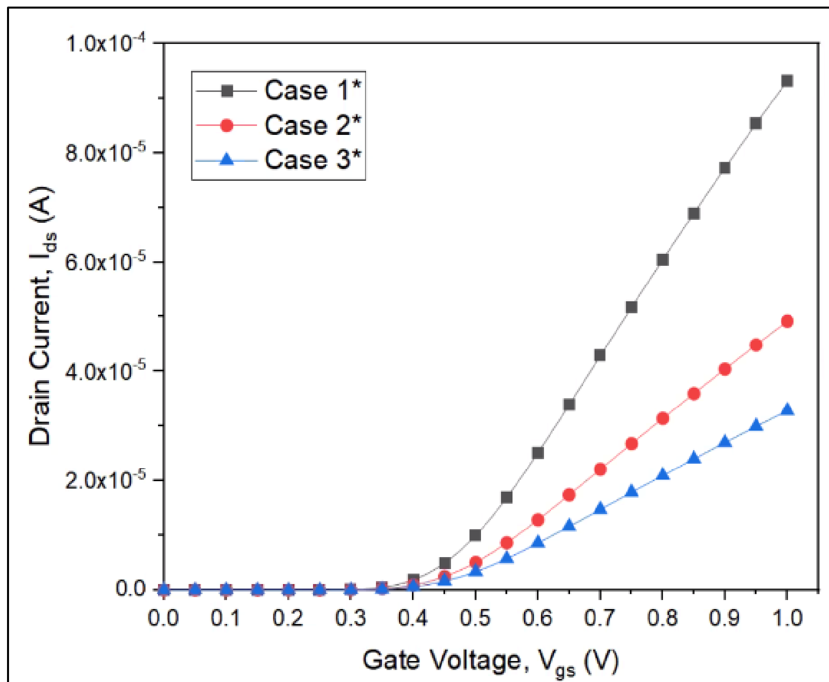
of channel radius) are shown in Figure 2.7 (b). On reducing the values of plasma parameters, the value of saturated drain current increases. The semiconducting CNT band gap is inversely proportional to the channel radius as can be seen from Eq. (2.6) mentioned above. Since I_{ds} of a FET depends on the total charge that fills up the first sub band, I_{ds} becomes dependent on channel radius and hence on the plasma parameters. Scaling down plasma parameters leads to scaling down of channel length, which further leads to better gate controllability resulting in increasing the value of saturated drain current. This makes the right balance of plasma parameters extremely important for efficient working of a device.

Figure 2.8 (a) and (b) shows the variation in channel resistance R_{ch} with V_{gs} (at fixed value of V_{ds} = 0.5 V) for varying values of plasma parameters corresponding to different values of channel radius and channel length, respectively. It can be observed that R_{ch} reduces with decreasing values of plasma parameters, thus ensuring high current drive.
From Figure 2.9, it can be observed that on reducing the values of plasma parameters corresponding to different values of channel radius, threshold voltage decreases. With reducing plasma parameters that directly affect the channel radius, gate electrode's control on the mid of the channel decreases, leading to reduced electric field lines originating from the gate electrode. This reduces the threshold voltage.

I_{ON}/I_{OFF} current ratio is an essential parameter to measure the digital performance of the device. As can be seen from Figure 2.10, with increasing values of plasma parameters, the I_{ON}/I_{OFF} ratio increases. Figure 2.11 shows the variation in threshold voltage and I_{ON}/I_{OFF} current ratio for different values of plasma parameters corresponding to different values of channel length. The level of ON current increases with reducing plasma parameters. For Figure 2.10, with reducing plasma parameters, channel radius increases, which reduces the bandgap and hence increasing ON current [32].

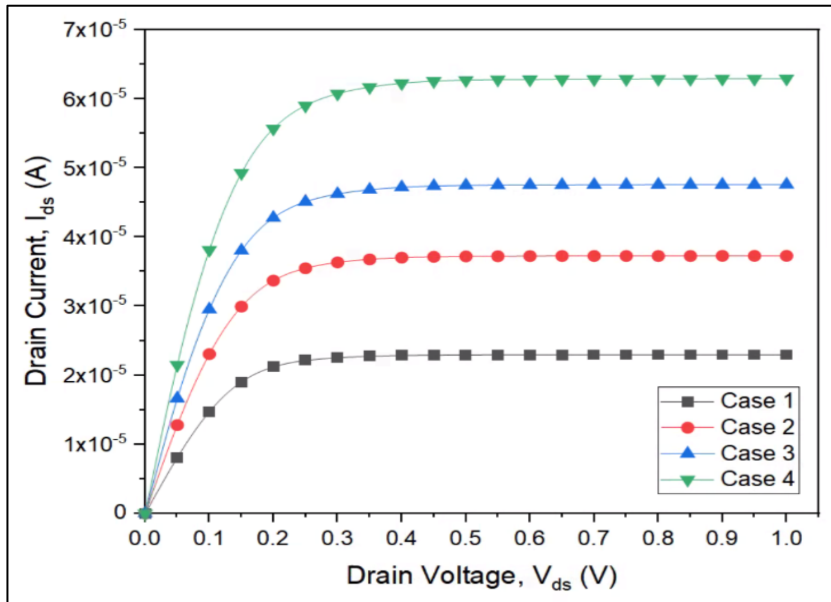


(a)

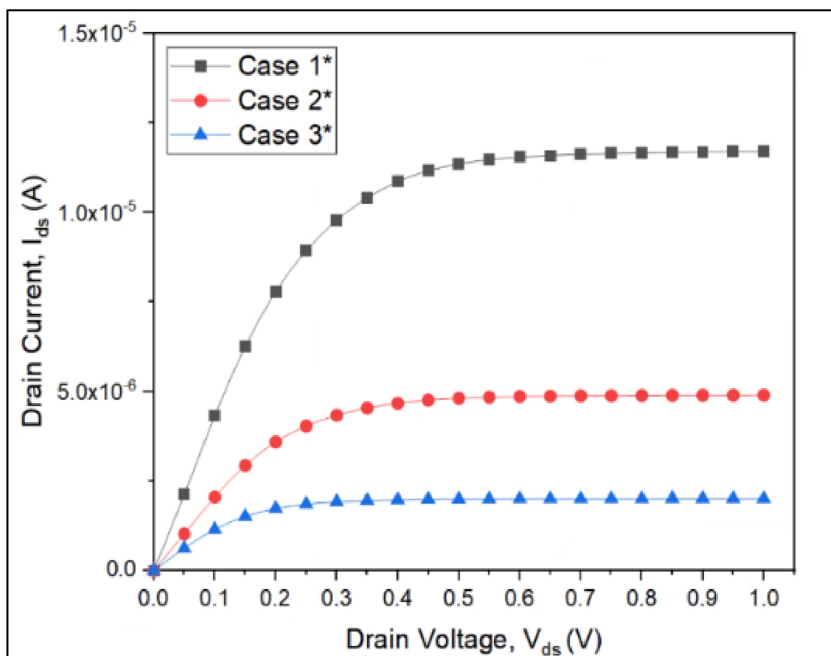


(b)

Figure 2.6: Transfer characteristics for VA-DMCNFET for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2), (b) channel length (in µm) (Table 2.3) at V_{ds}= 0.5V.

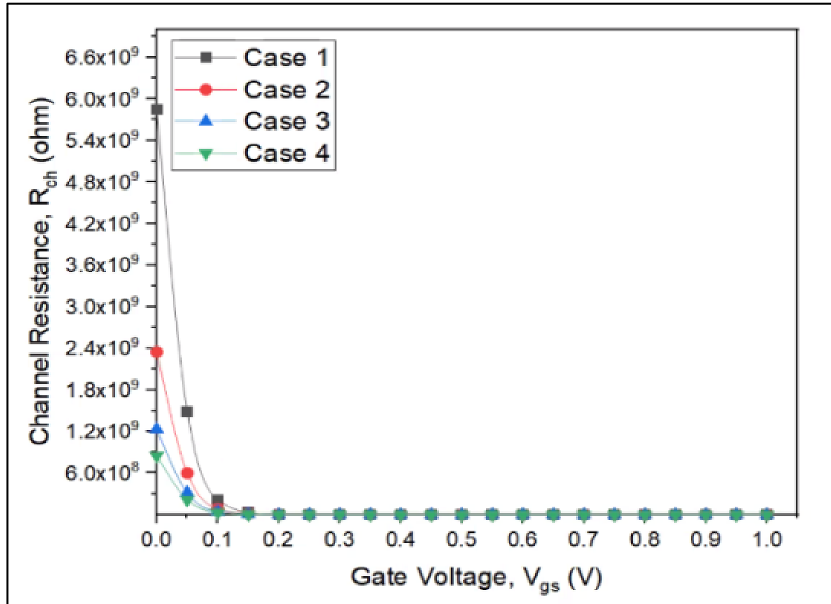


(a)

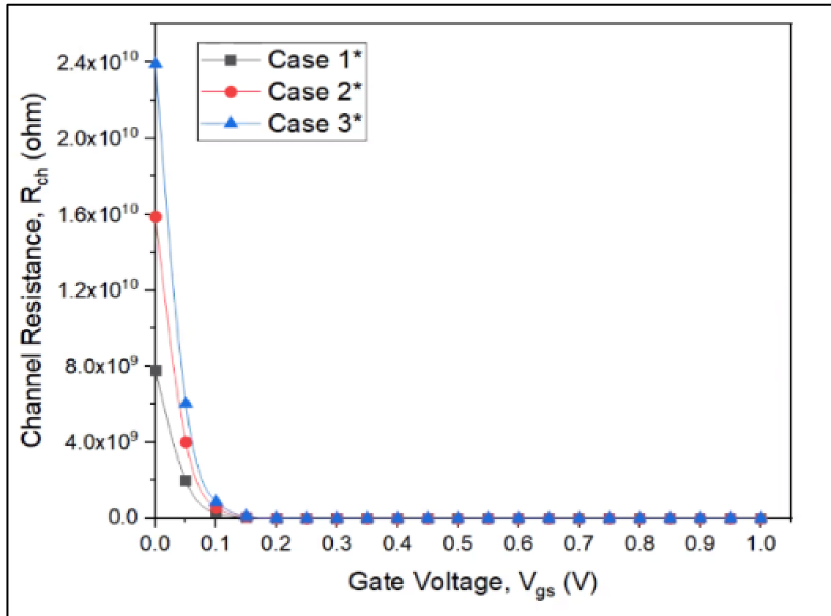


(b)

Figure 2.7: Output characteristics of VA-DMCNFET for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2), (b) channel length (in µm) (Table 2.3) at $V_{gs} = 0.5$ V



(a)



(b)

Figure 2.8: R_{ch} vs V_{gs} for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2), (b) channel length (in μm) (Table 2.3) at V_{ds} = 0.5

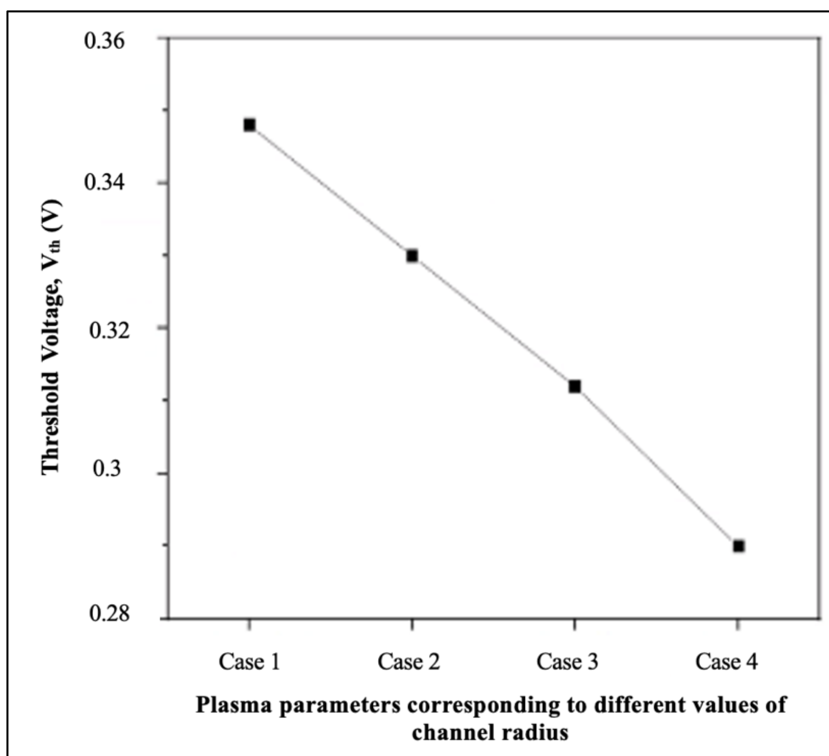


Figure 2.9: Variation of V_{th} for different values of plasma parameters corresponding to different values of channel radius (in nm) (Table 2.2) at V_{ds} = 0.1 V

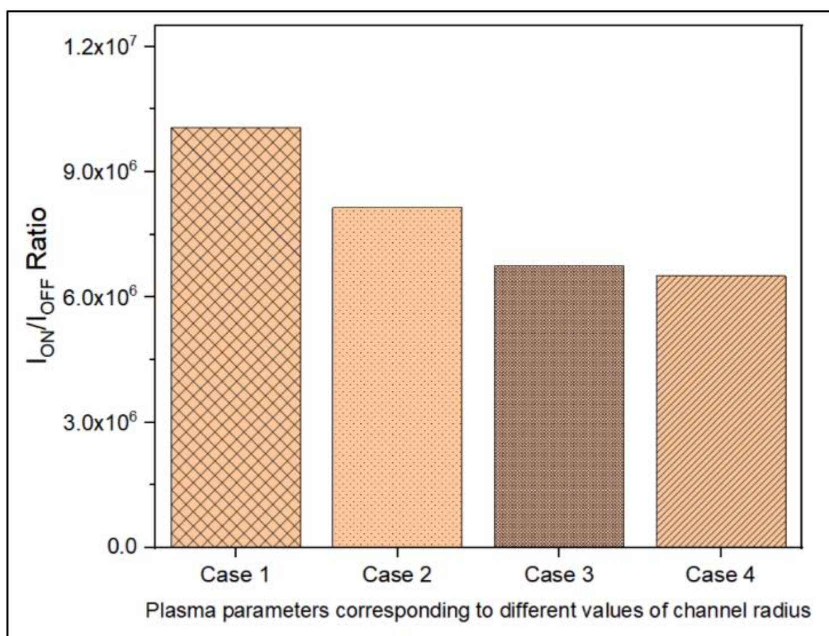


Figure 2.10: Variation of I_{ON}/I_{OFF} ratio for different values of plasma parameters corresponding to different values of channel radius (in nm) (Table 2.2) at V_{ds} = 0.5 V

For Figure 2.11, with increasing values of plasma parameters, channel length increases which reduces charge carrier density. However, with increasing ON current, OFF state current also increases due to leakages, which should be factored in accordingly. Transconductance (g_m) is a critical property that governs the performance of a FET. It is known that g_m of a device increases with the decrease in band gap owing to a stronger control of gate on the channel. A larger value of g_m is capable of delivering larger gain of device, when all other factors are kept constant. Figure 2.12 (a) and 2.12 (b) shows the variation in g_m with V_{gs} (at fixed value of $V_{ds} = 0.5$ V) for varying values of plasma parameters corresponding to different values of channel radius and channel length, respectively. The value of g_m increases with decreasing values of plasma parameters which can be attributed to higher values of drain current as is observed from Figure 2.6 (a) and 2.6 (b). A higher transconductance of the device implies a higher transport efficiency and hence a better applicability for analog devices. Hence, the higher the value of transconductance, the better it is.

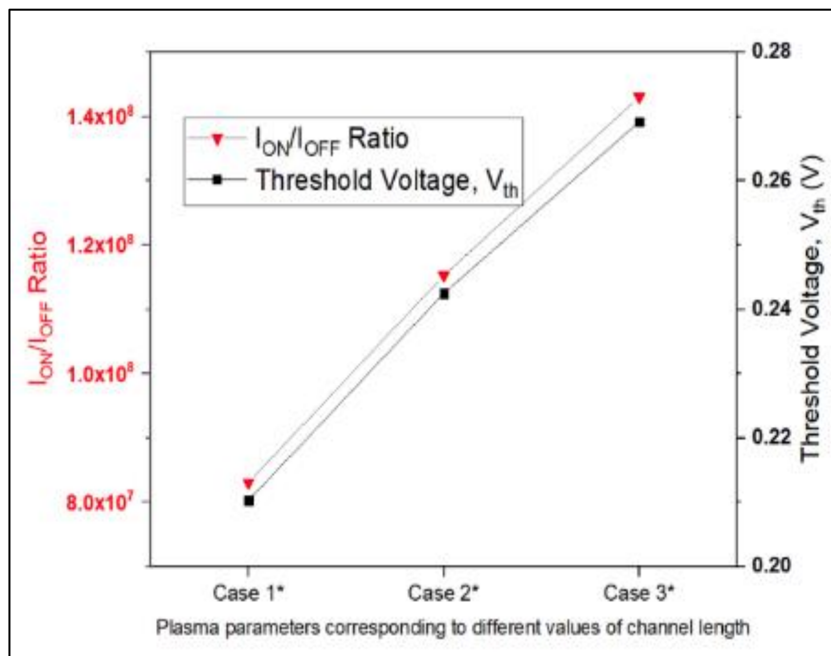
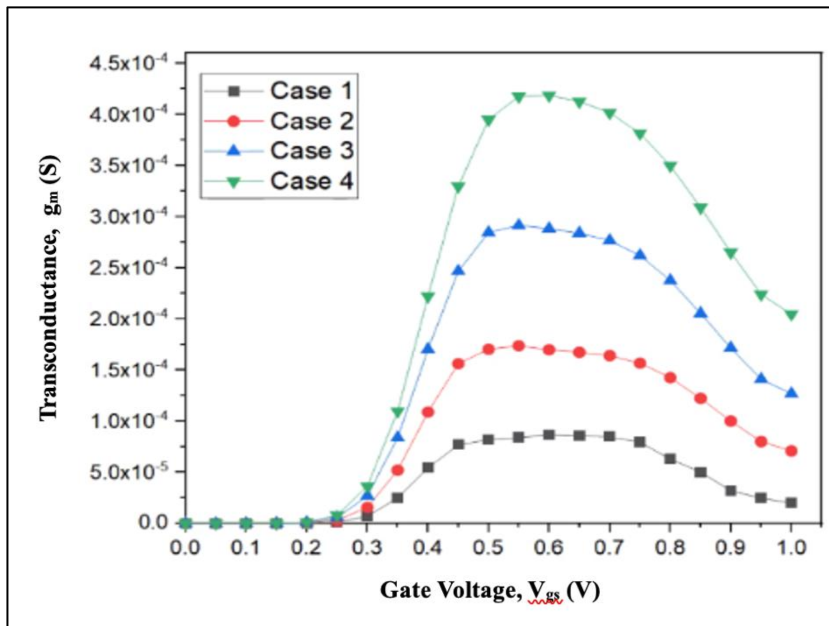
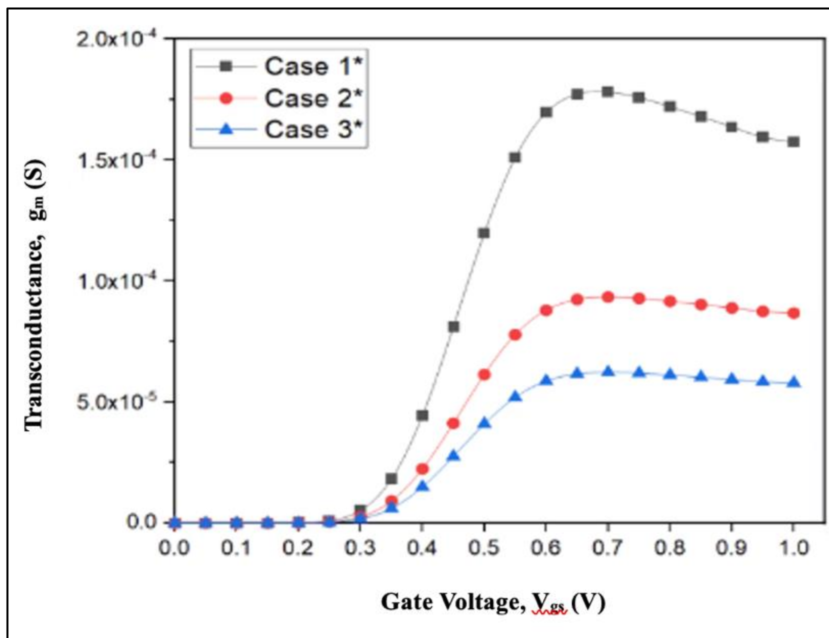


Figure 2.11: Variation of Threshold voltage, V_{th} and I_{ON}/I_{OFF} ratio for different values of plasma parameters corresponding to different values of channel length (in µm) (Table 2.3) at V_{ds}



(a)



(b)

Figure 2.12: g_m vs V_{gs} for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2) (b) channel length (in μm) (Table 2.3) at V_{ds} = 0.5 V

Mathematically, output conductance, g_d, is defined as the derivative of I_{ds} to V_{ds} at fixed gate bias V_{gs}. Figure 2.13 (a) shows g_d vs V_{ds} for different values of plasma parameters corresponding to different channel radius for a fixed channel length at fixed V_{gs} = 0.5 V. As observed from Figure 2.13 (a), value of g_d is higher at lower values of plasma parameters corresponding to higher value of channel radius. As the output conductance is a derivative of the drain current, an improvement in the drain current would subsequently result in the increase in output conductance. In Figure 2.13 (b), the value of g_d increases with scaling down of plasma parameters and is attributed to the fact that higher drain currents are observed for lower value of plasma parameters and lower values of channel length due to better gate controllability. Hence, lower plasma parameter conditions are the most appropriate for higher values of g_d.

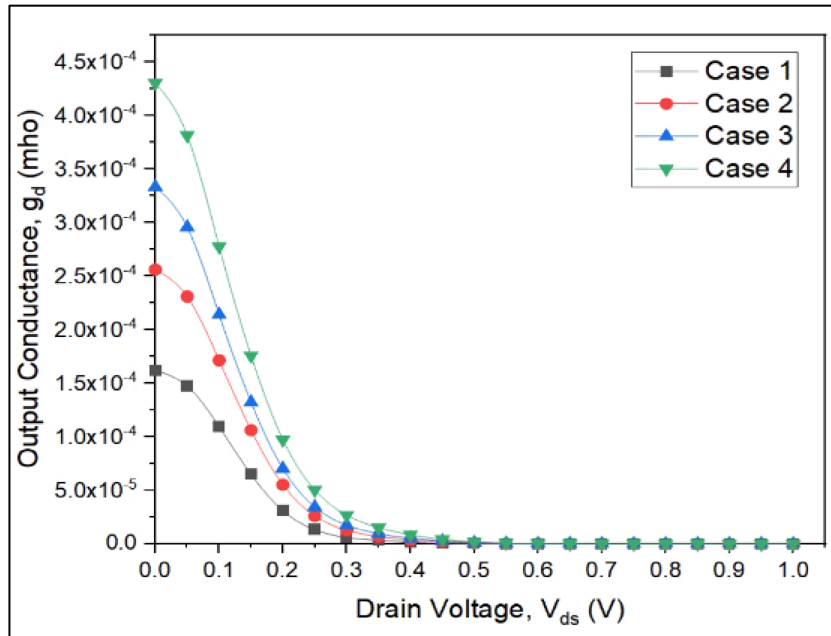
Early voltage V_{EA} is defined as the ratio of drain current I_{ds} and output conductance g_d, i.e. ,

$$V_{EA} = \frac{I_{ds}}{g_d}$$

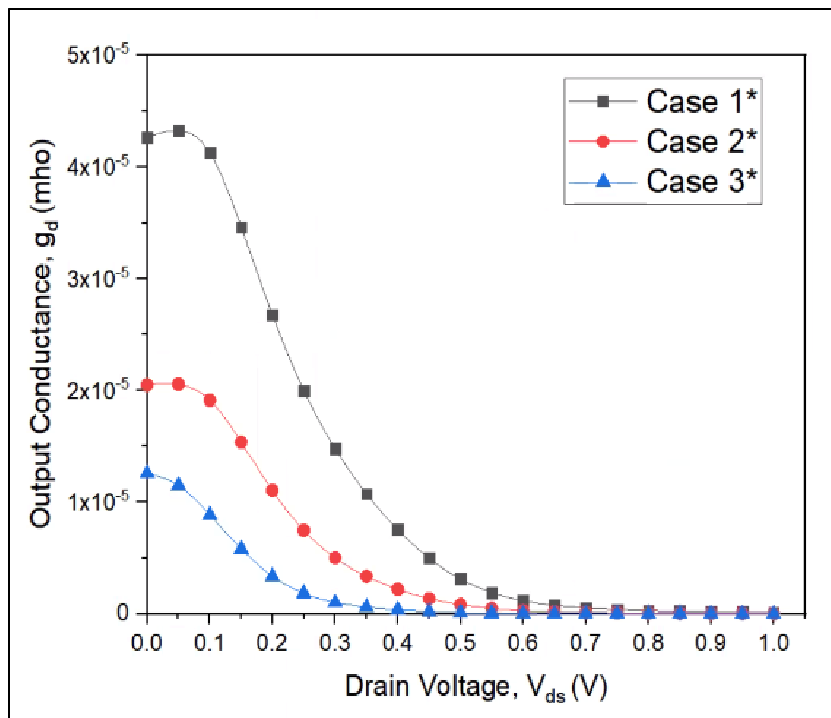
The gain A_V of the proposed device can be expressed as:

$$A_v = \frac{g_m}{I_{ds}} \times V_{EA}$$

Higher values of V_{EA} and A_V are required for better analog performance [33].
Figure 2.14 (a) and 2.14 (b) shows the shift in V_{EA} with V_{ds} (at fixed V_{gs} = 0.5 V) for different values of plasma parameters corresponding to varying values of channel radius (at fixed channel length) and varying values of channel length (at fixed value of channel radius), respectively. As observed, the value of early voltage increases on increasing the values of the plasma parameters. While both I_{ds} and g_d reduce with increasing plasma parameters, the rate of reduction in g_d is more pronounced in this case, leading to increase in V_{EA}. Higher values of plasma parameters are required for higher V_{EA} and hence higher gain A_v which finds extensive applications for high-gain amplification purposes.

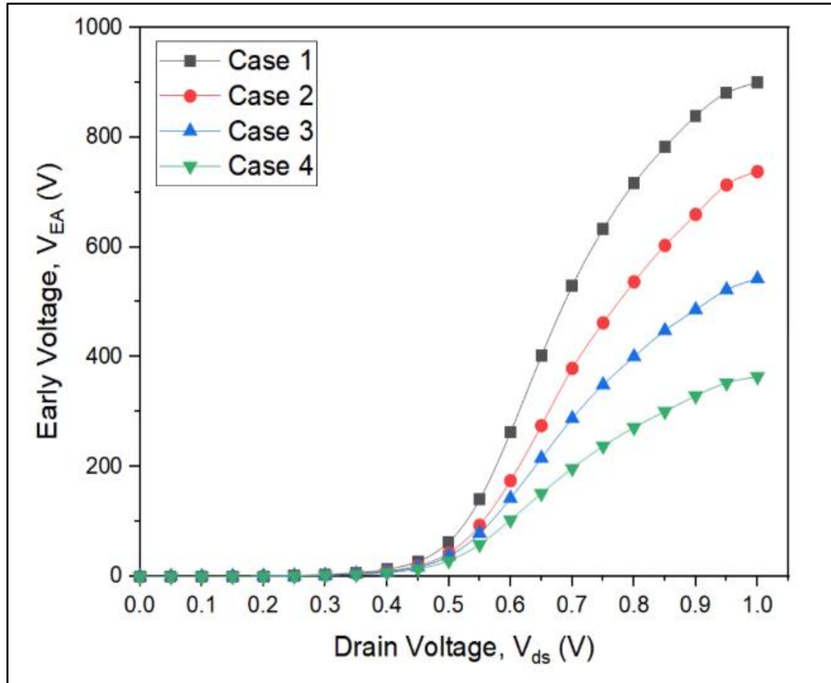


(a)

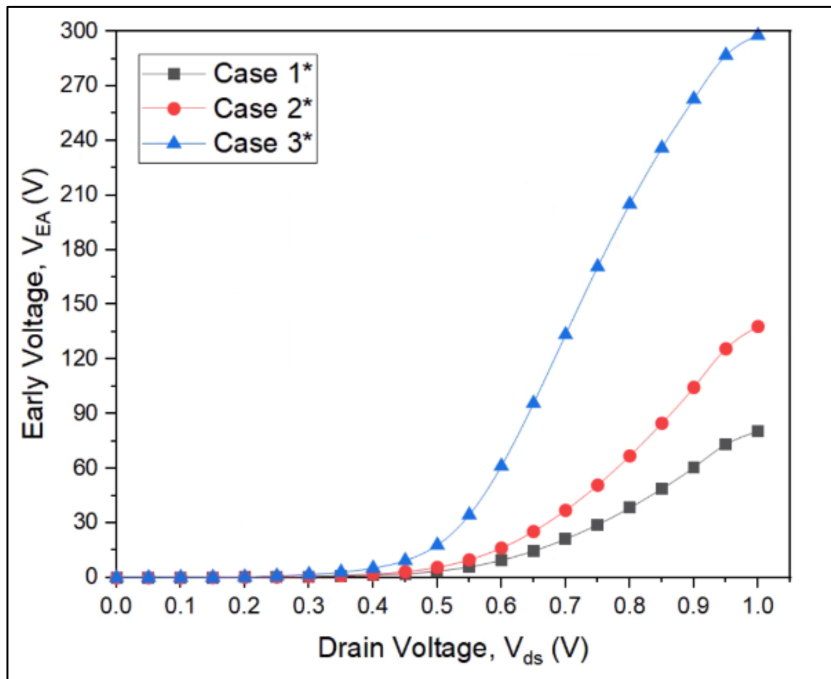


(b)

Figure 2.13: g_d vs V_{ds} for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2) (b) channel length (in μm) (Table 3)



(a)



(b)

Figure 2.14: V_{EA} vs V_{ds} for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2) (b) channel length (in µm) (Table 2.3) at V_{gs} = 0.5 V

Cutoff frequency f_c can be defined as:

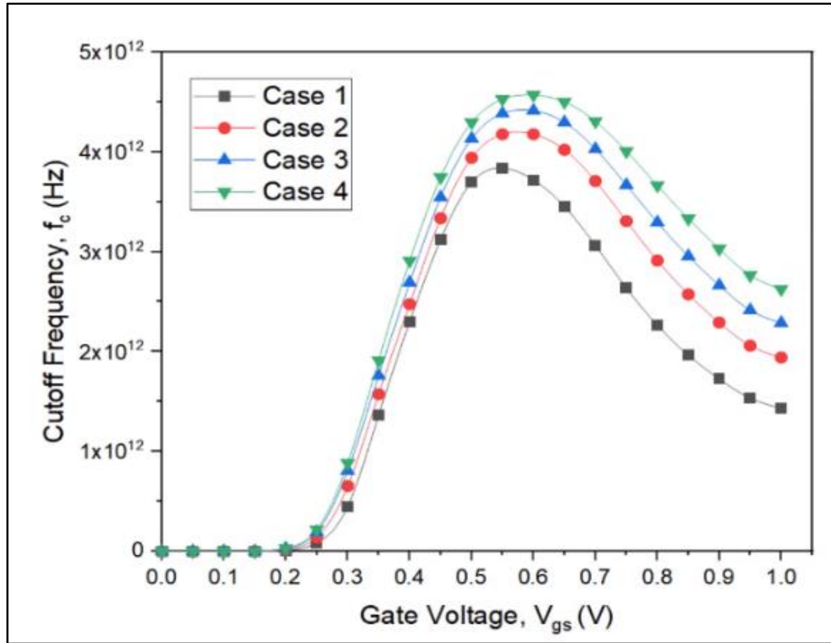
$$f_c = \frac{g_m}{2\pi C_{GG}}$$

It directly depends on transconductance g_m and is inversely related to gate capacitance C_{GG} as can be seen above [27]. It is a critical parameter for comparing transistors for RF applications. A large value of f_c is preferred since the high frequency operation of a FET is directed by the same. Figure 2.15 (a) shows that the value of f_c increases with reduction in plasma parameters (on increasing channel radius) as higher value of transconductance will direct higher value of cutoff frequency.

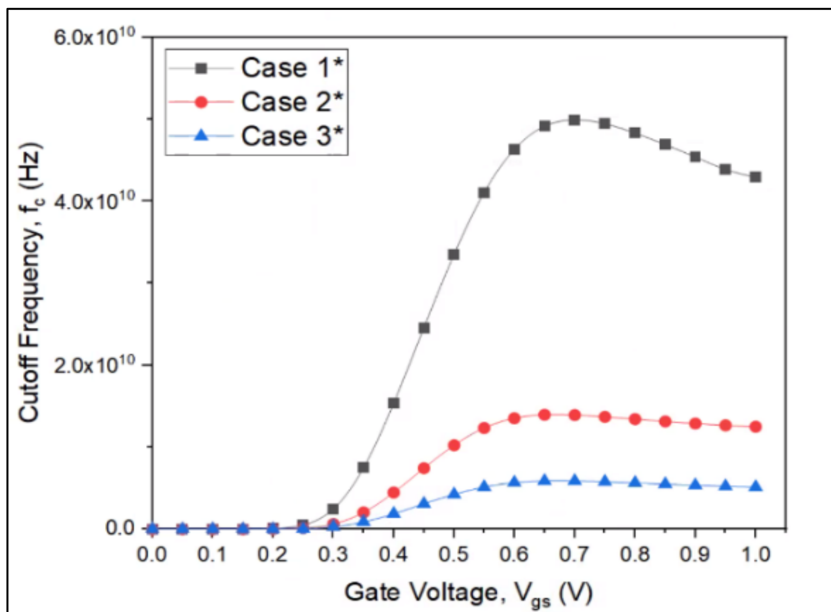
From Figure 2.15 (b), on reducing the values of plasma parameters (for reducing channel length), the value of f_c increases due to increase in transconductance and reduction in parasitic gate capacitance. Hence, for high frequency operation of the device, lower values of plasma parameters are required.

The summary of relation between plasma parameters and transistor performance is given in Table 2.4. The simulated device VA-DMCNFET has a wide range of applications. Plasma assisted devices find their usage in bio-sensors, logic gates, etc. Due to high values of drive current and transconductance, the proposed device can be used to maximize speed for digital logic applications [29].

CNTs are ideal for on-chip interconnect applications in microelectronics since they can carry high current densities with fixed resistance over several micrometres [30,31,32]. The semiconducting CNTs are responsive to their environment and hence used in bio and electro-chemical sensors for detecting biological species such as proteins, DNA, antibodies etc. [34].



(a)



(b)

Figure 2.15: f_c vs V_{gs} for different values of plasma parameters corresponding to different values of (a) channel radius (in nm) (Table 2.2) (b) channel length (in µm) (Table 2.3) at V_{ds} = 0.5 V

Table 2.4 Summary Table

S.No	Transistor property	Relation with plasma parameters (n_{eo}, T_{eo} & n_{io}, T_{io})
1.	Drain Current	Increases with decreasing values of plasma parameters
2.	Channel Resistance	Decreases with decreasing values of plasma parameters
3.	Threshold Voltage	Decreases with decreasing values of plasma parameters
4.	I_{ON}/I_{OFF} Ratio	Decreases with decreasing values of plasma parameters
5.	Transconductance	Increases with decreasing values of plasma parameters
6.	Output Conductance	Increases with decreasing values of plasma parameters
7.	Early Voltage	Decreases with decreasing values of plasma parameters
8.	Cut-off Frequency	Increases with decreasing values of plasma parameters

2.5 CONCLUSION

The proposed device VA-DMCNFET with vertically aligned semiconducting CNT grown in presence of plasma sheath through the process of PECVD technique as the channel was successfully implemented. The obtained results were compared with the existing experimental observations and are found in good agreement. The proposed device shows far improved metrics as compared to NWFET. Further, using this research, we can conclude that with reducing plasma parameters i.e., increasing values of CNT channel radius for fixed CNT channel length or decreasing values of channel length for fixed channel radius, the absolute value of saturated drain current, transconductance, output conductance increase whereas channel resistance along with threshold voltage can be seen reducing. Along the same lines, I_{ON}/I_{OFF} current ratio, early voltage and gain of the device increase on increasing the values of plasma parameters. In both the sets, reducing plasma parameters helps in increasing the value of cutoff frequency, thus leading to better RF performance. The research that we have conducted can be used as a base in future by several experimentalists for their respective study. Moreover, our simulation results can be useful for explaining many more experimental findings such as their application in digital devices and biosensors.

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Chapter-3

PERFORMANCE EVALUATION & LINEARITY DISTORTION ANALYSIS FOR PLASMA- ASSISTED DUAL-MATERIAL CARBON NANOTUBE FIELD EFFECT TRANSISTOR WITH A SiO_2-HfO_2 STACKED GATE-OXIDE STRUCTURE (DM-SGCNFET)

Publication

1. **Mansha Kansal** and Suresh C. Sharma, "Performance Evaluation & Linearity Distortion Analysis for Plasma- Assisted Dual-Material Carbon Nanotube Field Effect Transistor with a SiO_2-HfO_2 Stacked Gate-Oxide Structure (DM-SGCNFET)", *Silicon* 14, 12381–12391 (2022)

3

PERFORMANCE EVALUATION & LINEARITY DISTORTION ANALYSIS FOR PLASMA- ASSISTED DUAL-MATERIAL CARBON NANOTUBE FIELD EFFECT TRANSISTOR WITH A SiO_2-HfO_2 STACKED GATE-OXIDE STRUCTURE (DM-SGCNFET)

3.1 BRIEF OUTLINE

This work demonstrates the simulation analysis of a novel device Plasma-Assisted Dual-Material Stacked Gate-Oxide Carbon Nanotube Field Effect Transistor (DM-SGCNFET) with a stacked gate oxide structure consisting of two oxides - SiO_2 and HfO_2. The performance metric of the simulated device is compared with a SiO_2 based similar device (DM-CNFET) for varying sets of plasma parameters that corresponds to different values of channel length. Both the devices feature a PECVD grown vertically aligned semiconducting carbon nanotube implemented as the channel material. The comprehensive analysis delineates that the DM-SGCNFET offers enhanced values of drain current, transconductance, output conductance, early voltage, gain, gate capacitance, better switching ratio, and reduced channel resistance as compared to DM-CNFET. The novel structure contemplating a dual-material gate and a high-k dielectric gate stack in CNT based transistors warrants as an appropriate device for digital and analog applications providing high efficiency. The chapter further explores the DM-SGCNFET device for linearity distortion performance by evaluating g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3 and 1-dB compression point for altering values of plasma parameters.

3.2 INTRODUCTION

Carbon Nanotubes (CNTs) have emerged as a lucrative option to the ever growing global trend of downscaling the physical dimensions of transistors while simultaneously aiming for increased device performance [1]. Owing to their capable electrical and mechanical properties, the rise of CNTs has made nanotechnology more viable, thus opening new avenues of real life applications as well. CNT based devices offer a host of advantages making them popular for nanotechnology and nano-architectonics. They showcase high speed operation, high mechanical flexibility, high current density, excellent thermal conductivity etc. [2,3]. The field of nano-architectonics is an emerging concept which uses the concept of nanotechnology to produce systems built from nanoscale objects. In simpler words, nano-architectonics is used to create real life practical systems from nanotechnology. After years of extensive research on silicon and silicon-based devices, CNT based devices have gathered massive interest and emerged as viable alternatives [4,5].

CNTs can be synthesized using a variety of ways. Among these, PECVD (Plasma Enhanced Chemical Vapor Deposition) technique stands out owing to a variety of reasons. This particular synthesis technique allows for large scale production of vertically aligned CNT structures with relatively better control over the structure's dimensions and physical properties, that too at a lower temperature. This is made possible owing to the existence of diverse combination of some active species - electrons, ions, radicals, neutrals etc. within the plasma region. The electric field of the plasma sheath is responsible for applying force on the carbon nanostructures, which leads to their growth in a vertical direction [6-12].

The robust nature of SiO_2 has allowed for its extensive usage in CMOS technology. In spite of the significant advantages it holds, it suffers from a relatively lower dielectric constant. Since capacitance is inversely proportional to dielectric thickness, SiO_2 needs to be scaled down accordingly. SiO_2 however, suffers from a variety of scaling problems such as increasing gate leakage current, increasing direct tunnelling current, reliability degradation etc. This can lead to erroneous operation of logic device and an increase in static power consumption [13].

Innovations through novel materials and structures are paving the way for significant advancements in performance and reliability. One such innovation is the usage of high-k dielectrics as gate oxide. Out of the various viable high-k dielectrics, HfO_2 has emerged as a promising material. It possesses some remarkable properties such as high dielectric constant ($\kappa \sim 22$), high thermal stability, comparably large bandgap (5.3 eV), and also high heat of formation [14].

While high-k materials such as HfO_2 has its merits, on the flip side, its direct deposition is not so favourable. A head-on deposition can suffer from unstable threshold voltage, degradation in mobility and subpar subthreshold swing. Moreover, an increased thickness of high-k dielectrics leads to large magnitudes of fringing fields, thus causing poor gate controllability [15]. Thus, implementing a stacked gate oxide structure is preferred. A gate stack structure requires a thin SiO_2 layer between the high-k dielectric and the channel material, thus taking advantage of superior SiO_2 interface quality.

In this chapter, Plasma-Assisted Dual-Material Stacked Gate-Oxide Carbon Nanotube Field Effect Transistor (DM-SGCNFET) has been simulated using SILVACO ATLAS 3D simulator. The device features a cylindrical surrounding gate structure. Further shown is the variation of electrical properties of device such as drain current, channel resistance, I_{ON}/I_{OFF} ratio, transconductance, output conductance, early voltage, gain and gate capacitance with plasma parameters - electron density n_{eo}, electron temperature T_{eo} and ion density n_{io}, ion temperature T_{io}, corresponding to different sets of channel length at fixed channel radius. The results have been compared to SiO_2 based Plasma-Assisted Dual-Material Carbon Nanotube Field Effect Transistor (DM-CNFET). It can be seen that due to employment of stacked gate oxide structure, there is considerable improvement in performance over DM-CNFET. This work further examines the effect of plasma parameters on the wireless operation of the proposed device using linearity and harmonic distortion parameters - g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3 and 1-dB compression point.

3.3 DEVICE SIMULATION

The proposed device DM-SGCNFET is designed and simulated. The experimental synthesis of carbon nanotubes has been done using PECVD technique at relatively low temperature using Argon and Methane as precursor gases on a silicon substrate with nickel deposited by thermal evaporation [16]. The 3-D and cross-sectional view of DM-SGCNFET are depicted in Figure 3.1 & Figure 3.2, respectively.

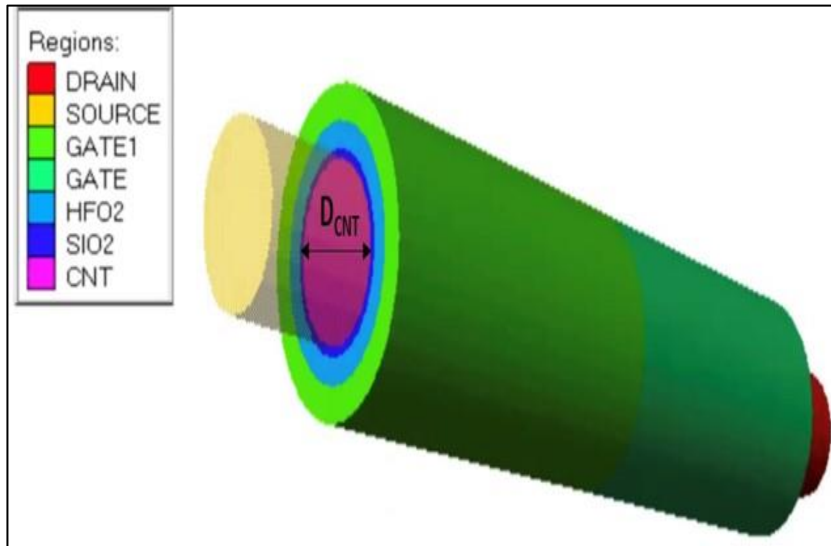


Figure 3.1: 3-D view of the proposed DM-SGCNFET

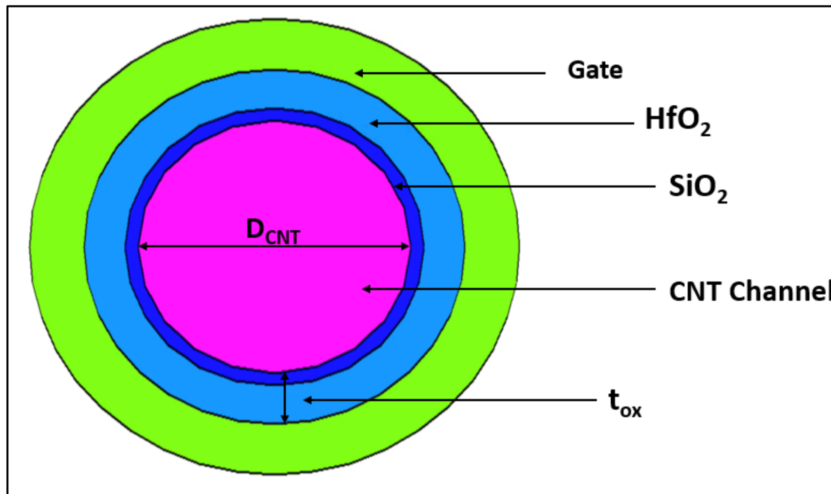


Figure 3.2: Depiction of cross-sectional view of DM-SGCNFET

The contour plot of potential at V_{gs} = 0 V and V_{ds} = 0 V is shown in Figure 3.3. The proposed device uses a dual-material gate having work functions 4.4 eV and 4.7 eV, with the former at the drain side and latter at the source end. Table 3.1 shows the structure specifications of the device DM-SGCNFET. SiO_2 (κ = 3.9) and HfO_2 (κ = 22) are used to simulate a stacked gate oxide structure. HfO_2 has been deployed above SiO_2 in order to increase the oxide capacitance of the device.

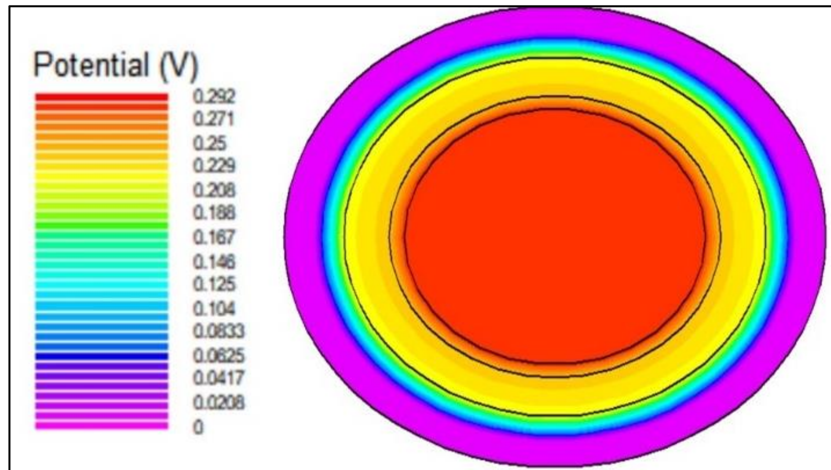


Figure 3.3: Potential contour plot of DM-SGCNFET at V_{ds} = 0 V and V_{gs} = 0 V

The source and drain contacts are used with doping concentration $10^{18}/cm^3$. Silvaco Atlas TCAD software is used to run the device simulations [17].

Table 3.1: Device Specifications

Parameter	**Symbol**	**Value(s)**
Channel Length (µm)	L	1.5, 2.5, 3.5
Channel Radius (nm)	R	5
Oxide thickness (nm)	t_{ox}	2
Source/ Drain Length (nm)	L_s/L_d	15
Gate work function (eV)	ϕ_1 , ϕ_2	4.4, 4.7
SiO_2 Permittivity	ε_{ox1}	3.9
HfO_2 Permittivity	ε_{ox2}	22

By using MUP and MUN parameters, mobility for holes and electrons is defined for simulating CNT. The leakage currents are simulated using Shockley-Read-Hall (SRH) model while minority carrier recombinations are factored in using the Auger recombination model. The Boltzmann model is implemented and Newton and Gummel's method are incorporated for mathematical solutions [18].

The results obtained after simulating the device DM-SGCNFET, as shown in Figure 3.4, can be seen following the same trend as the device reported by Yang et al. and Kansal et al. [18,19]. The difference in magnitude is owing to basic structural differences that exist between the two devices.

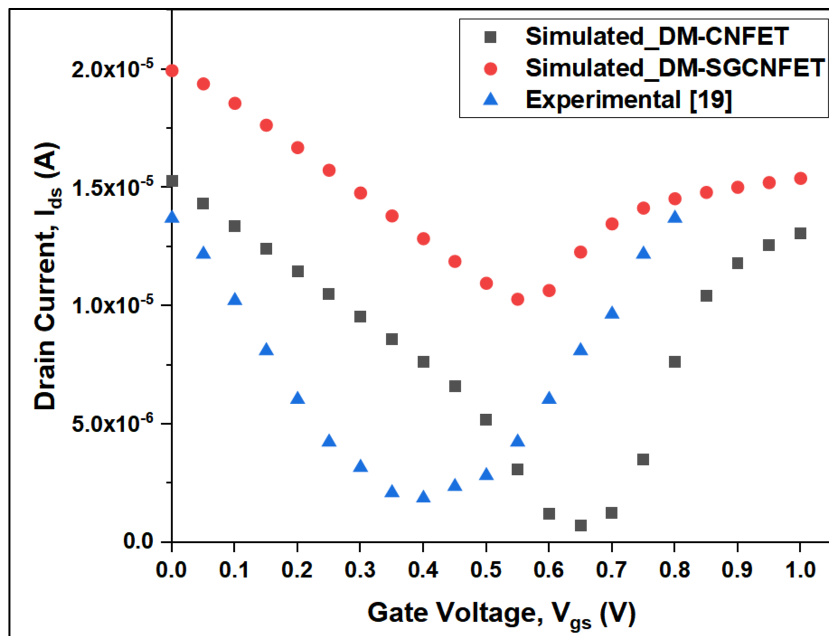


Figure 3.4: Comparison of simulated devices with experimental results at V_{ds}= 0.8 V

Table 3.2: Value of Plasma parameters corresponding to varying values of channel length (at constant value of R = 5 nm)

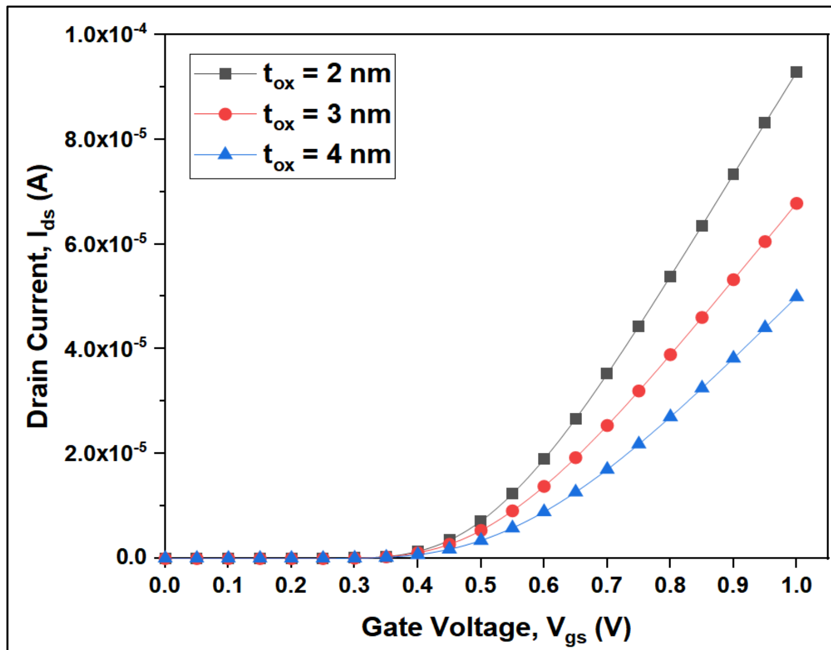
Scenario	Channel Length (µm)	Plasma Parameter I - electron density n_{eo} (cm^{-3})	Plasma Parameter II - electron temperature T_{eo} (eV)	Plasma Parameter III - ion density n_{io} (cm^{-3})	Plasma Parameter IV - ion temperature T_{io} (K)
Case 1	1.5	$8x10^8$	1.15	$7x10^7$	2200
Case 2	2.5	$2x10^9$	1.25	$6x10^8$	2235
Case 3	3.5	$8x10^9$	1.35	$2x10^9$	2280

3.4 RESULTS AND DISCUSSION

The structure and characteristics of the proposed device DM-SGCNFET are simulated and analysed using the Silvaco 3D Atlas TCAD Simulator.

3.4.1 PERFORMANCE EVALUATION OF DM-SGCNFET WITH VARYING SiO_2 OXIDE THICKNESS

The first part of the research aims to analyse the characteristics of SiO_2 based DM-CNFET with varying oxide thickness. From Figure 3.5 (a), (b) & (c), it is observed that there is an improvement in the performance of the device on reducing the oxide thickness. However, it is known that on reducing the oxide thickness, even for improved performance, gate tunnelling current & gate leakage current increases. Thus, it becomes difficult to reduce or scale down the dimensions of the device without risking its breakdown caused by the inability to further reduce the oxide thickness. Moreover, SiO_2 is predicted to reach the limits of its scaling after which it will act as a hindrance in the continued downscaling trend. Owing to these limitations, research is now focused more towards the advent of new material technologies than continuing to usher in the era of existing ones. High-k oxide materials, as a result, have sparked tremendous amounts of interest [20].



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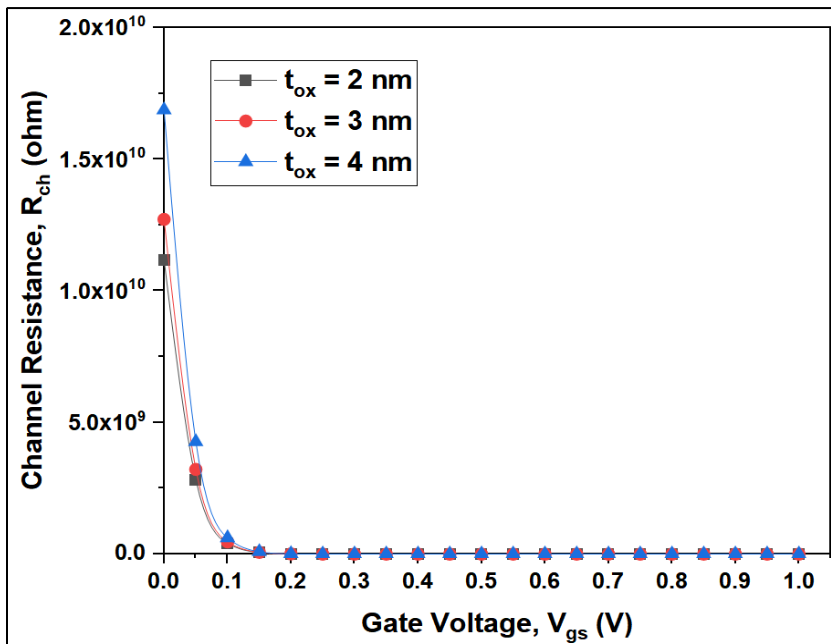

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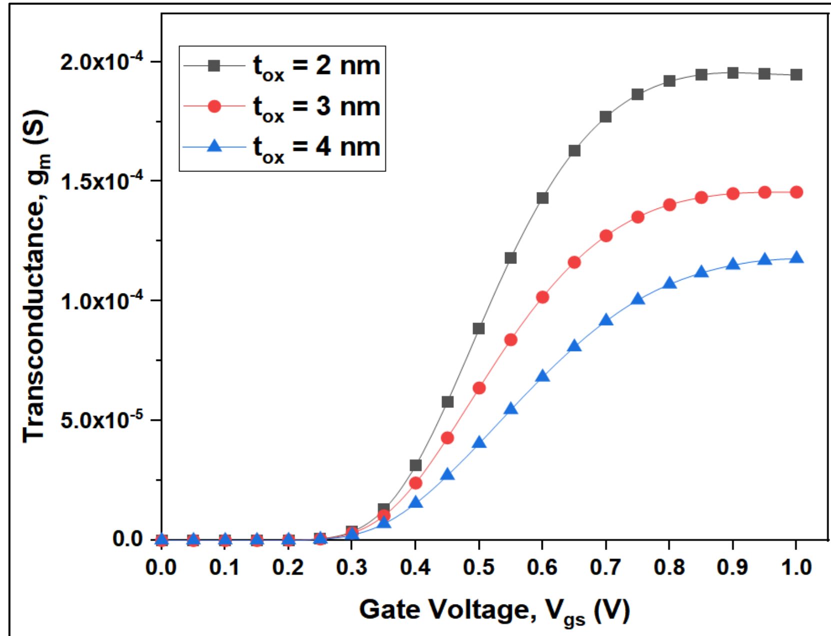


(c)

Figure 3.5: Impact of oxide thickness variation on SiO_2 based DM-CNFET: (a) Drain current I_{ds} v/s gate voltage V_{gs} (b) Channel Resistance R_{ch} v/s V_{gs} (c) Transconductance g_m v/s V_{gs} (at constant V_{ds} = 0.8 V)

3.4.2 PERFORMANCE COMPARISON OF DM-SGCNFET WITH DM-CNFET

With the help of a physical model as developed by Sharma and Tiwari [21], the relation between plasma parameters and device geometry can be drawn. With increment in values of plasma parameters: electron density n_{eo} and electron temperature T_{eo}, ion density n_{io} and ion temperature T_{io} , the CNT length increases initially with time before hitting the saturation level. For increasing plasma parameters: n_{io} and T_{io}, there is an increase in the thickness of the plasma sheath and there is a faster generation of carbon monomers. Consequently, there is more diffusion of the carbon ions taking place, hence leading to increase in length of the CNT [10, 22].

Plasma parameters play a severely important role in deciding the performance of the synthesized device. Owing to their control over the channel radius and channel length, they have a direct control over critical electrostatic properties such as gate controllability, contact resistance, conductivity etc. The intention is to further cement

our knowledge about the impact of plasma parameters by analyzing the characteristics of DM-SGCNFET over varying sets of plasma parameters corresponding to various values of channel length, at a fixed channel radius.

Following Kansal and Sharma [18], surface potential can be defined as:

$$V_s = \frac{-2e}{L} \times log\left(\frac{\lambda_d}{R}\right) \tag{3.1}$$

where e=electronic charge and λ_d = Plasma Debye length.
From Equation (1),

$$L = \frac{-2e}{V_s} log\left(\frac{\lambda_d}{R}\right) \tag{3.2}$$

Also, by the definition of Debye length:

$$\frac{1}{\lambda_d^2} = \frac{1}{\lambda_e^2} + \frac{1}{\lambda_i^2} \tag{3.3}$$

where λ_e= electron plasma Debye length, λ_i = ion plasma Debye length and can be written as

$$\lambda_e = \sqrt{\frac{T_{eo}}{4\pi n_{eo} e^2}} \quad and \quad \lambda_i = \sqrt{\frac{T_{io}}{4\pi n_{io} e^2}} \tag{3.4}$$

By using Eq. (3.3) and Eq. (3.4), Eq. (3.2) can be written as –

$$L = \frac{-2e}{V_s} log\left[\frac{1}{R} \times \left(\frac{\lambda_e \lambda_i}{\sqrt{\lambda_e^2 + \lambda_i^2}}\right)\right] \tag{3.5}$$

$$L = \frac{-e}{V_s} log\left[\frac{1}{R^2} \times \left(\frac{\lambda_e^2 \lambda_i^2}{\lambda_e^2 + \lambda_i^2}\right)\right]$$

$$L = \frac{e}{V_s} log \left[R^2 \left(\frac{1}{\lambda_e^2} + \frac{1}{\lambda_i^2} \right) \right] \tag{3.6}$$

Putting the values of λ_e and λ_i from Eq. (3.4), Eq. (3.6) can be rewritten as

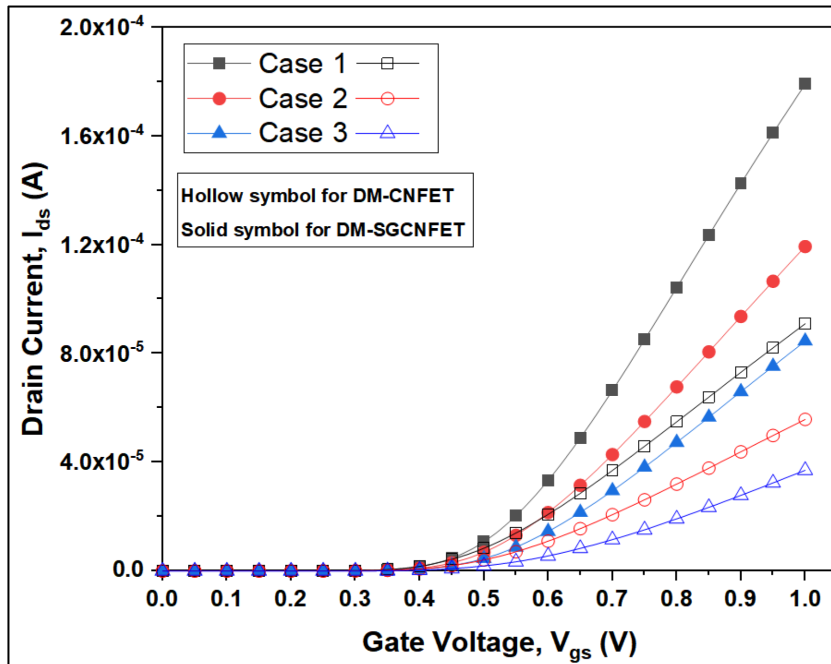
$$L = \frac{e}{V_s} log \left[4\pi e^2 R^2 \times \left(\frac{n_{eo}}{T_{eo}} + \frac{n_{io}}{T_{io}} \right) \right] \tag{3.7}$$

The drain is formulated as –

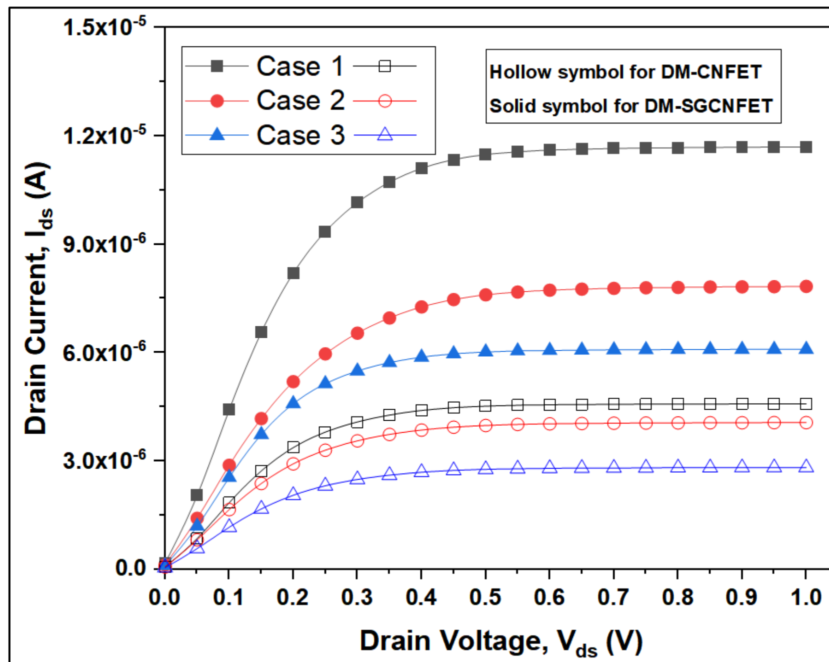
$$I_{ds} = \frac{\mu C}{L^2} V_{ds} \left(V_{gs} - V_{th} \right) \tag{3.8}$$

Where, C = Capacitance of the CNT, μ= apparent mobility in linear regime and V_{th} = threshold voltage. By putting the value of channel length L from Eq. (3.7) in Eq. (3.8), it becomes possible to relate the drain current of the device with the plasma parameters. As other characteristics of any device such as transconductance (g_m), output conductance (g_d), early voltage (V_{EA}) etc. depend on the drain current, so we can further draw a relation between these transistor properties and the plasma parameters. The transfer and output characteristics for the DM-SGCNFET device at V_{ds} = 0.8 V and V_{gs} = 0.5 V, respectively for varying sets of plasma parameters is depicted in Figure 3.6 (a) and (b), respectively. It reveals that the proposed device shows considerable enhancement in drain current and degradation in channel resistance as can be seen from Figure 3.7 when compared to SiO_2 based DM-CNFET device. This is due to the incorporation of gate stack scheme having high-k dielectric. HfO_2 has band gap of 5.3 eV whereas the band gap for SiO_2 is 9.0 eV [23]. Due to lower energy gap in DM-SGCNFET, there is a lower energy barrier than DM-CNFET, which leads to faster

carrier generation and hence increased drain current can be encountered in the simulated device.



(a)



(b)

Figure 3.6: Impact of plasma parameters variation (Table 2) on (a) transfer characteristics at V_{ds} = 0.8 V (b) output characteristics at V_{gs} = 0.5 V

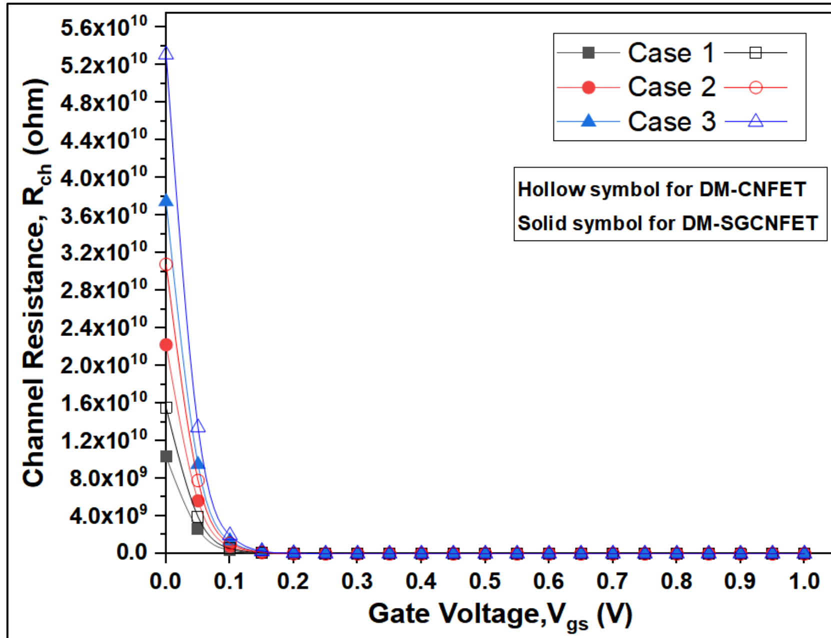


Figure 3.7: Impact of different values of plasma parameters (Table 3.2) on channel resistance (R_{ch}) at V_{ds} = 0.8 V

Figure 3.8 exhibits the I_{ON}/I_{OFF} ratio for both device structures. Low values of I_{ON}/I_{OFF} ratio causes low output transitions, whereas an appropriate value can help in improving speed and minimize leakage. It can be defined as the ratio of ON state current (value of I_{ds} at V_{gs} = 1.0 V) that determines the current driving capability of the device and OFF state current (value of I_{ds} at V_{gs} = 0 V) that refers to the power dissipation. Though there is a slight increase in the leakage current on using the SiO_2-HfO_2 stacked gate oxide but the increase in I_{ON} is much higher for the proposed device, hence leading to improved values of the switching ratio.

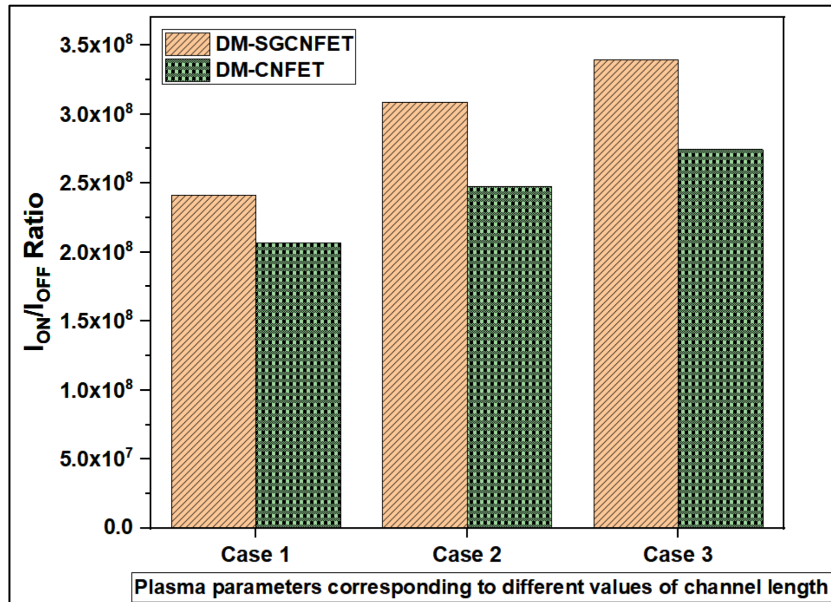


Figure 3.8: Variation of I_{ON}/I_{OFF} Ratio for different values of plasma parameters (Table 3.2) at V_{ds} = 0.8 V

Transconductance (g_m) is a crucial parameter used to define the optimum bias point. It is also an important measure for RF and analog applications. Figure 3.9 outlines the plot of variation of g_m with V_{gs} for different sets of plasma parameters at V_{ds} = 0.8 V for SiO_2 based DM-CNFET and DM-SGCNFET devices. g_m tends to follow an increasing trend with drop in the values of plasma parameters and it can be observed that DM-SGCNFET shows improved values of g_m in comparison to DM-CNFET due to high values of drain current as reported for former device. The increasing values of I_{ds} for the simulated device is attributed to the higher capacitance of HfO_2 as it leads to a hike in the electron concentration that takes place in the channel.

Output conductance, g_d is another parameter that determines the driving ability of a device and can be denoted as the derivative of drain current to drain bias at fixed V_{gs}. As g_d is directly dependant on drain current, any fluctuation in drain current due to employment of high-k dielectric stack would consequently lead to change in output conductance. In Figure 3.10, the value of g_d increases with scaling down of plasma parameters and the simulated device shows enhancement in g_d due to incorporation of high-k gate stack. Owing to high permittivity of the oxide layer, there is an increase in capacitance leading to creation of higher electric field, which further leads to

enhancement in the electron velocity. Hence, the electrons traverse faster and consequently increasing the I_{ds}.

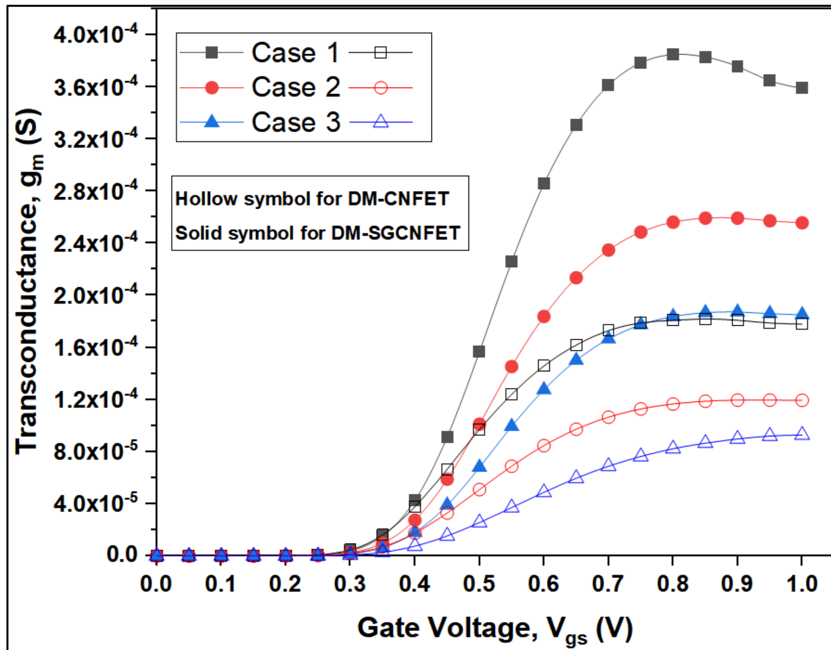


Figure 3.9: Impact of plasma parameters variation (Table 3.2) on transconductance (g_m) at $V_{ds} = 0.8$ V

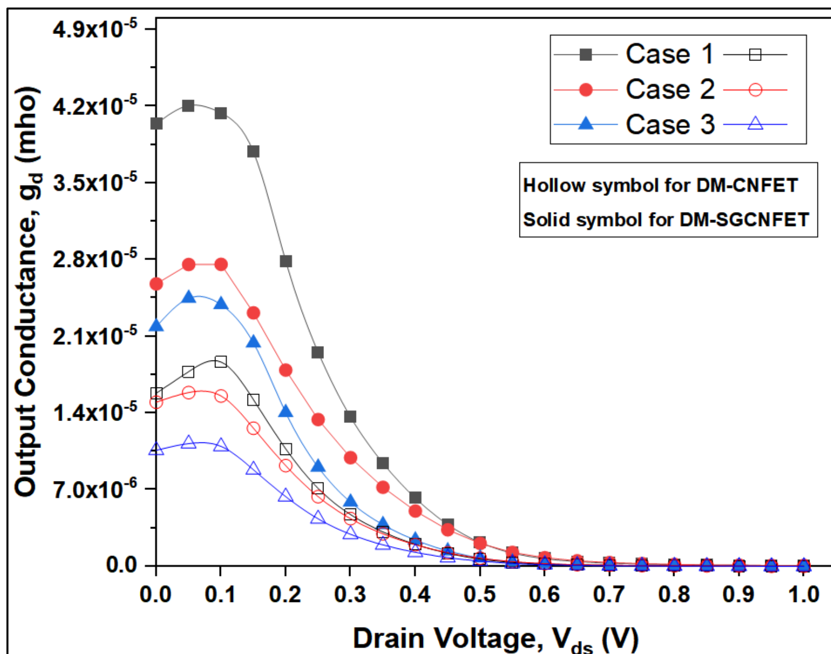


Figure 3.10: Impact of plasma parameters variation (Table 3.2) on output conductance (g_d) at $V_{ds} = 0.8$ V

Early voltage V_{EA} plays a significant role in determining the analog performance of a device. It is formulated as the ratio of drain current I_{ds} and output conductance g_d [24]. Higher V_{EA} implies enhanced gain of the device and its value improves with increasing set of plasma parameters. This can be attributed to the fact that g_d decreases at a more pronounced rate as compared to I_{ds}. From Figure 3.11, it is observed that DM-SGCNFET exhibits better values of early voltage in comparison to DM-CNFET making it an appropriate device for OPAMP applications.

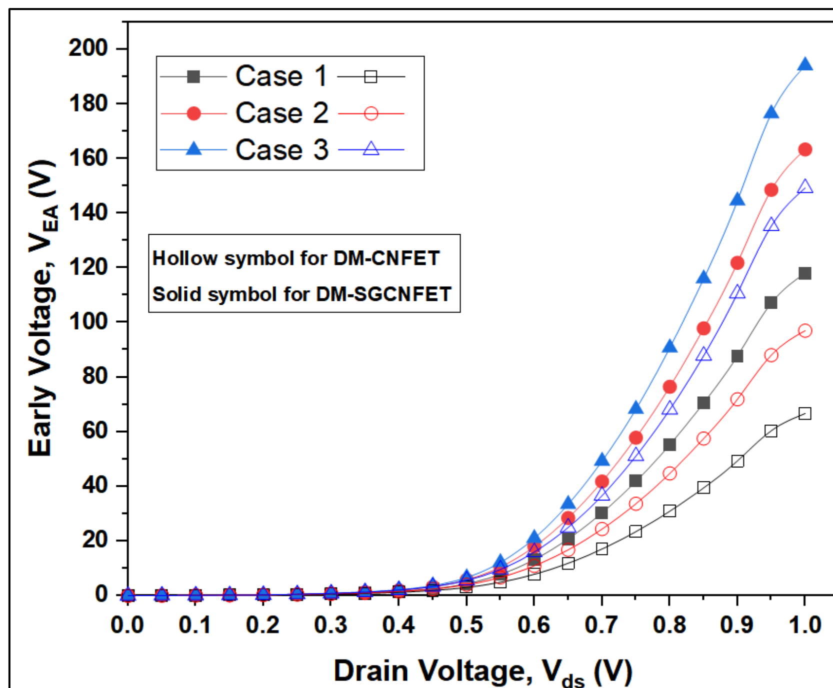


Figure 3.11: Impact of different values of plasma parameters (Table 3.2) on early voltage (V_{EA}) at V_{gs} = 0.5 V

The variation of the total Gate Capacitance (C_{GG}) that comprises of both gate to source capacitance (C_{GS}) and gate to drain capacitance (C_{GD}) with V_{gs} for both the devices for different set of plasma parameters is depicted in Figure 3.12. The simulation using AC analysis of C_{GG} is executed by coupling an input small AC signal with DC bias at the gate terminal. It can be clearly observed from the figure that the simulated device DM-SGCNFET offers large C_{GG} due to its higher gate capacitance as the fringing field capacitances comes into picture in addition to the above mentioned capacitances C_{GS} and C_{GD} on employment of high-k gate stack structure [25].

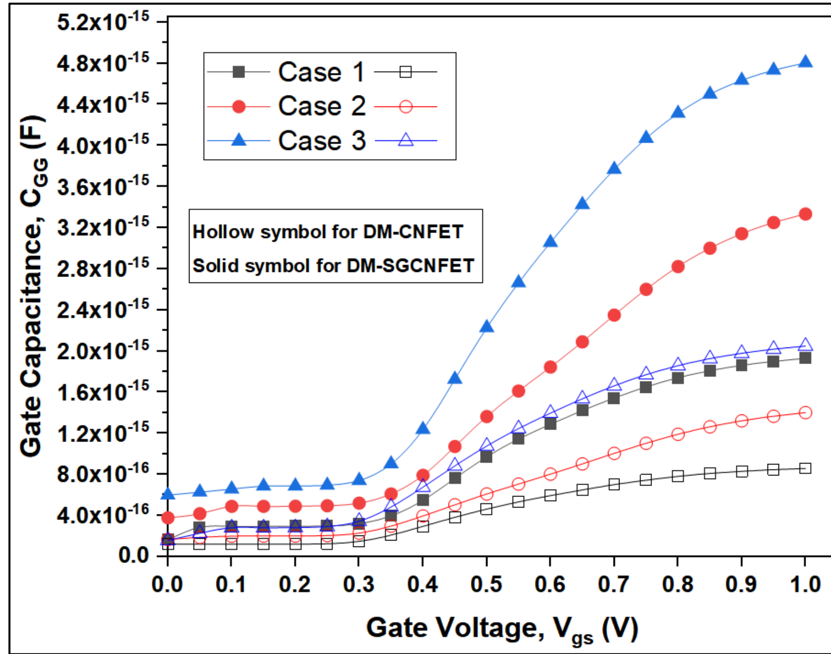


Figure 3.12: Impact of different sets of plasma parameters (Table 2) on Gate Capacitance (C_{GG}) at V_{ds} = 0.8 V

3.4.3 IMPACT OF PLASMA PARAMETERS ON LINEARITY CHARACTERISTICS OF DM-SGCNFET

Transistors with low distortion parameters are quite desirable for wireless communication systems. The parameters like high-order derivatives of transconductance (g_{m2} and g_{m3}) exhibit non-linearity and hence amplitude of these should be minimal in order to safeguard linearity and for lesser distortion. The nonlinearity effects lead to the degradation of the device characteristic and performance. Figure 3.13 (a) and Figure 3.13 (b) show the effect of plasma parameters on g_{m2} and g_{m3} with respect to V_{gs}. The values of g_{m2} and g_{m3} decrease with increasing sets of plasma parameters. At higher gate voltage, g_{m3} attains negative peak values. The Figure of Merit (FOM) VIP2, the second-order voltage intercept point and VIP3 known as the third-order voltage intercept point can be defined as the extrapolated gate voltage at which the fundamental tone amplitude is equal to the second-order and third-order harmonic amplitude respectively and can be used for the assessment of the characteristics of signal distortion using DC parameters [26].The high peak values of these parameters VIP2 and VIP3 indicate better linearity characteristics of the device.

The device FOM can be formulated as [26,27]:

$$VIP2 = 4 \times \frac{g_m}{g_{m2}} \tag{3.9}$$

$$VIP3 = \sqrt{24 \times (\frac{g_m}{g_{m3}})} \tag{3.10}$$

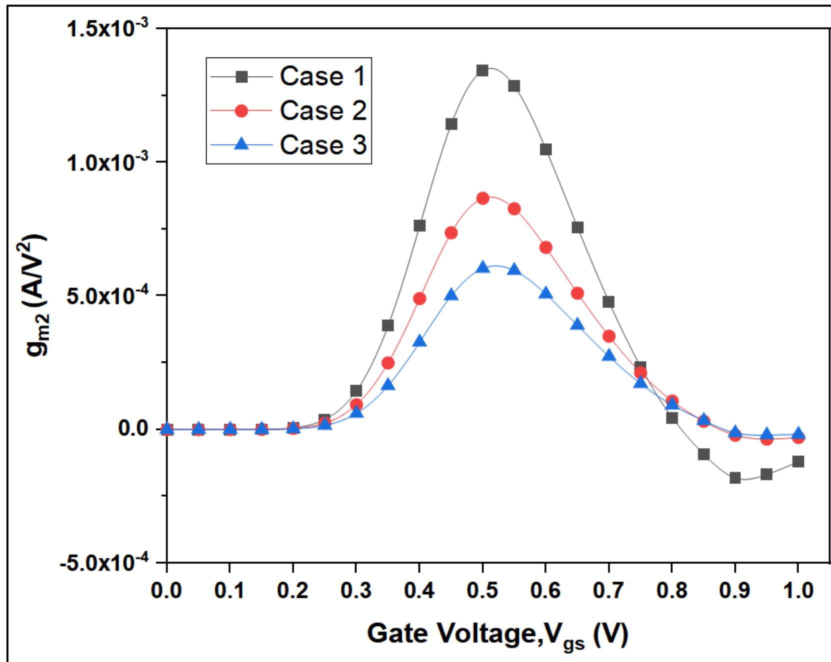
$$IIP3 = \frac{2}{3} \times \frac{g_m}{g_{m3} \times R_s} \tag{3.11}$$

$$IMD3 = (\frac{9}{2} \times VIP3^2 \times g_{m3})^2 \times R_s \tag{3.12}$$

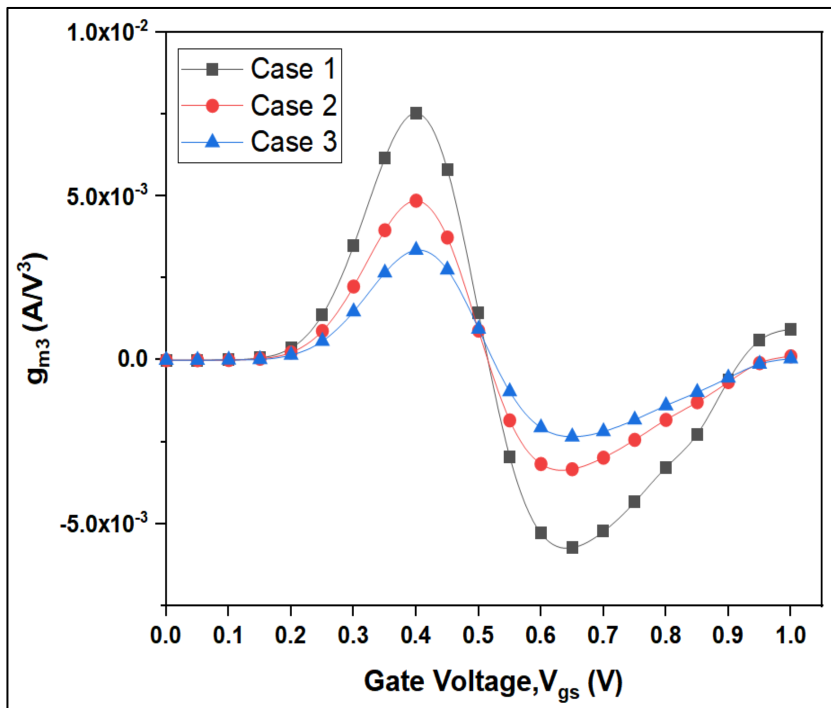
$$1 - dB\, compression\, point = 0.22 \times \sqrt{\frac{g_m}{g_{m3}}} \tag{3.13}$$

where R_s is known as the internal resistance and its value can be taken as 50 Ω.

In Figure 3.13 (c) and Figure 3.13 (d), VIP2 and VIP3 variation with respect to V_{gs} at V_{ds} = 0.8 V has been plotted for different sets of plasma parameters, respectively. A higher value of VIP2 is favourable. Superior values of VIP2 are observed for higher values of plasma parameters. The values climb with increasing V_{gs} and hit their peak values, after which there is a drop in the magnitude. By virtue of a more prominent fall in the values of g_{m3} compared to g_m, VIP3 has its paramount value found for highest value of plasma parameters i.e., longest channel length at higher values of V_{gs}. The peak value shifts towards higher V_{gs} upon increasing plasma parameters.



(a)



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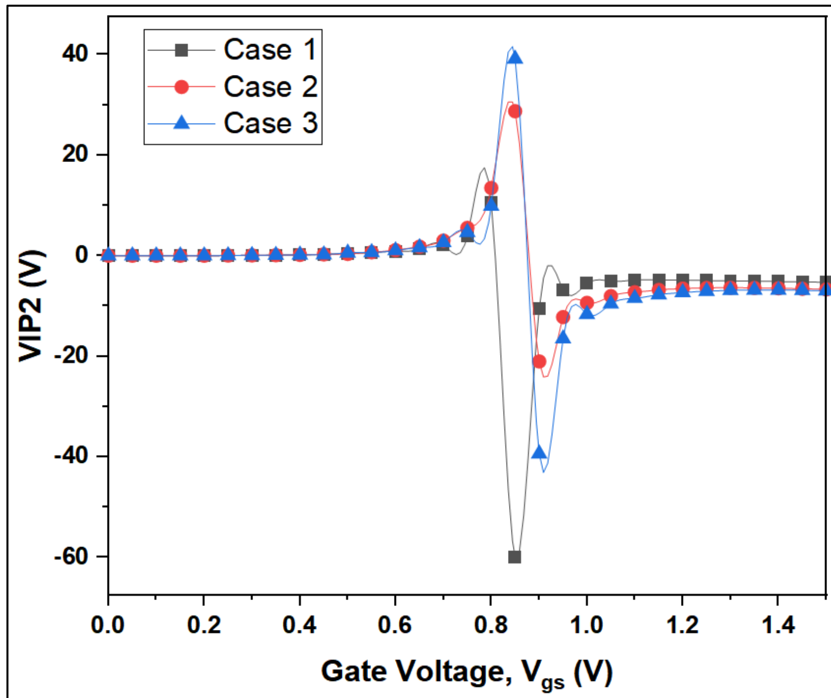

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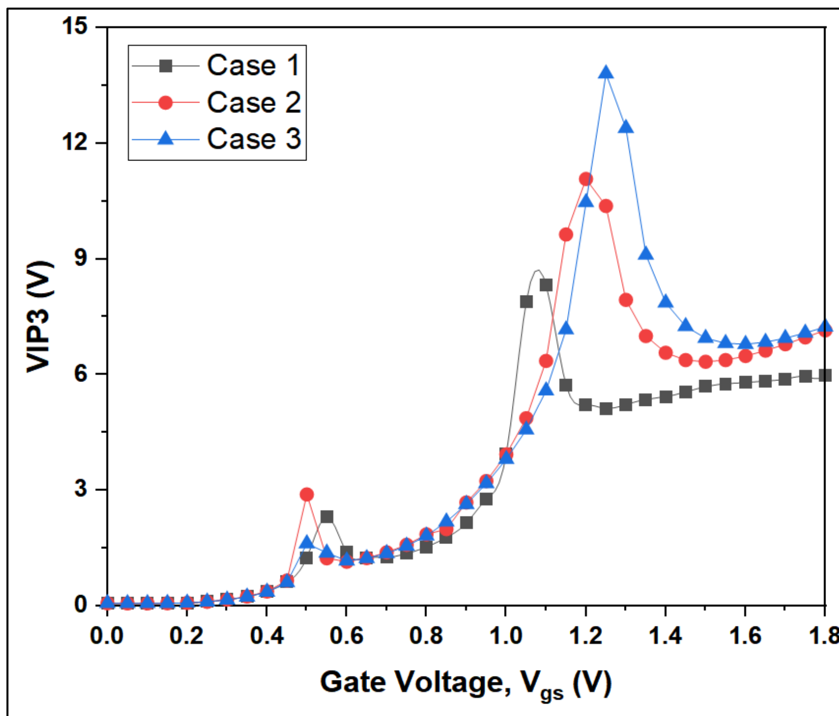

(d)

Figure 3.13: Impact of plasma parameters variation (Table 3.2) on (a) g_{m2} (b) g_{m3} (c) VIP2 (d) VIP3 at V_{ds} = 0.8 V

IMD3 also known as the third-order intermodulation distortion, represents the extrapolated intermodulation distortion power at which the first and third-order intermodulation power is equal [27]. IIP3 is defined as the third-order intercept input power characteristics. Higher values of IIP3 whereas lower values of IMD3 are preferred for improved linear characteristics. Figure 3.14 and Figure 3.15 illustrate the impact of plasma parameters on IIP3 and IMD3 of the aforesaid device. IMD3 increases with increasing V_{gs} before attaining saturation for all investigated cases. Further, it is witnessed that lowest value of IMD3 is encountered at highest value of plasma parameters.

Magnitude of the peak value of IIP3 increases with increasing sets of plasma parameters, i.e., for longer channel lengths, its peak value is higher. The peak values shift towards higher values of V_{gs} with increment in plasma parameter values. 1-dB compression point is defined as the input power at which output power gets deviated from linearity by 1-dB. The peak value is marked up for increasing sets of plasma parameters, ensuring high linearity which is represented in Figure 3.16. Table 3.3 summarizes the variation in linearity metrics with increasing values of plasma parameters.

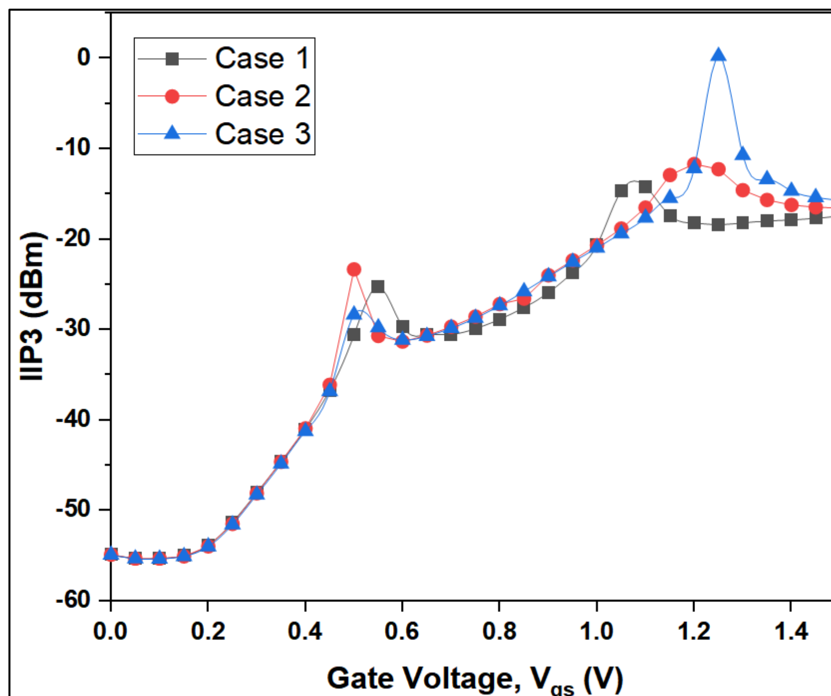

Figure 3.14: Impact of plasma parameters variation (Table 3.2) on IIP3 at V_{ds} = 0.8 V

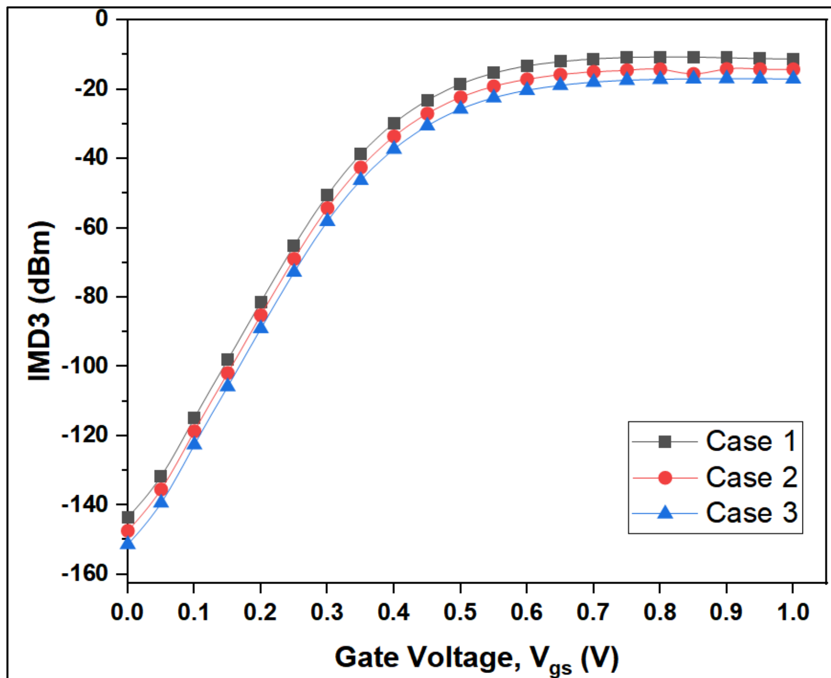

Figure 3.15: Impact of plasma parameters variation (Table 3.2) on IMD3 at V_{ds} = 0.8 V

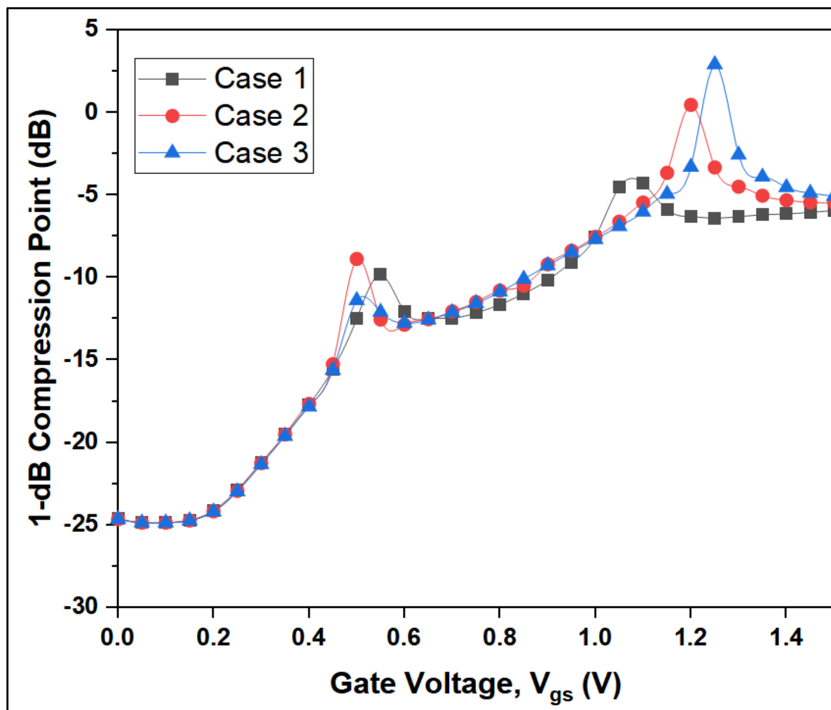

Figure 3.16: Impact of plasma parameters variation (Table 3.2) on 1-dB Compression Point at V_{ds} = 0.8 V

The obtained results further cement the DM-SGCNFET as a superior device for real life applicability. The results reported in this investigation can deeply benefit plasma-based nanoarchitectonics and related applications. DM-SGCNFET takes over the advantages of DM-CNFET and improves them even further through a high-k stacked oxide structure, thus stamping itself as a better device. Other applications of the simulated device include bio & electro-chemical sensors for detecting biological species, on-chip interconnect applications etc. [28-32].

Table 3.3: Review Table

S.No	Linearity metrics	Trend with increasing values of plasma parameters (n_{eo}, T_{eo} & n_{io}, T_{io})
1.	g_{m2}	Lower peak values
2.	g_{m3}	Lower peak values
3.	VIP2	Higher peak values
4.	VIP3	Higher peak values
5.	IIP3	Higher peak values
6.	IMD3	Lower peak values
7.	1-dB Comp. point	Higher peak values

3.5 CONCLUSION

The proposed device with SiO_2-HfO_2 Stacked Gate-Oxide structure has been proposed to counter the downscaling problems associated with conventional SiO_2 gate oxide. Researchers are propelling in the direction of novel materials for FETs instead of last mile optimisations of the current ones. Usage of high-k dielectrics fall in the same line. The simulated DM-SGCNFET device showcases much better electrical properties such as higher values of drain current, I_{ON}/I_{OFF} ratio, g_m, g_d, V_{EA}, gain and C_{GG} along with lower values of R_{ch} when compared against a SiO_2 based DM-CNFET device. Further, the linearity of the said device has been examined by comparing the linearity metrics of a transistor for varying sets of plasma parameters. From the simulations carried out in this study, it can be inferred that the preferred attributes (i.e., superior values of VIP2, VIP3, IIP3, 1-dB compression point and lower values of g_{m2}, g_{m3} and IMD3) are observed for higher values of plasma parameters.

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Chapter- 4

EXPLORATION OF NOVEL HAFNIUM OXIDE (HfO_2) BASED PLASMA-ASSISTED GATE ALL AROUND CARBON NANOTUBE FET (GAA-CNTFET) FOR HIGH SENSING APPLICATIONS

Publications

1. **Mansha Kansal** and Suresh C. Sharma, "Exploration of Novel Hafnium Oxide (HfO_2) Based Plasma Assisted Gate All Around Carbon Nanotube FET (GAA-CNTFET) for High Sensing Applications", 2022 *ECS J. Solid State Sci. Technol.* 11 101002, (2022).
2. **Mansha Kansal**, Suresh C. Sharma, **"**Simulation Based Analysis of Plasma-Assisted Carbon Nanotube Field Effect Transistor (CNTFET) for improved device metrics and applications**"**, International Conference on Nanotechnology: Opportunities and Challenges, 2022 (ICNOC-2022).

4

EXPLORATION OF NOVEL HAFNIUM OXIDE (HfO_2) BASED PLASMA-ASSISTED GATE ALL AROUND CARBON NANOTUBE FET (GAA-CNTFET) FOR HIGH SENSING APPLICATIONS

4.1 BRIEF OUTLINE

The present research aims to implement a Hafnium Oxide (HfO_2) based Plasma-Assisted Gate All Around Carbon Nanotube Field Effect Transistor (GAA-CNTFET) and use it for a better understanding of plasma parameters and their effect on the device. With a more streamlined focus on plasma synthesized (PECVD technique) CNT for channel material, the intention is to understand how the incorporation of high-k dielectrics leads to enhanced device performance. HfO_2 is used as a high-k dielectric to overcome the limitations of conventional Silicon Dioxide (SiO_2) gate dielectric. A comparative analysis has been performed, based on which it can be concluded that using HfO_2 leads to improvement in all observed performance metrics - higher drain current, transconductance, output conductance, early voltage, and gate capacitance. Furthermore, by implementing a cavity in the oxide layer and utilizing the concept of dielectric modulation, it can be observed that tailoring the dielectric permittivity of the cavity affects and alters the device's performance characteristics. Better performance and high sensitivity are tilted towards a higher dielectric constant value. This analysis's results help quantify the practical usage of the device for sensing applications in biology, environment and other prominent industries.

4.2 INTRODUCTION

The surge in performance requirements necessitates an intensive focus on improving Field-Effect Transistor (FET) output. While work has been done to evolve current materials and mechanisms for improved efficiency, it is of paramount that resources are also spent wisely towards including new materials that can bring forward drastic performance improvements over conventional devices. This need has further accelerated owing to various scaling limitations possessed by the current generation of materials [1]. Among the new age materials that have garnered interest, Carbon Nanotube (CNT), with its superior material properties, is the number one contender to keep the CMOS technology relevant. The increased mobility offered by CNT ensures higher drain current and operating frequencies compared to its counterparts under similar conditions. In contrast, a modest bandgap, compared to Graphene, ensures lower leakage current and much-improved RF power gain [2-8]. The simulated device and this subsequent research can aid the field of nanoarchitectonics. Nanoarchitectonics, an upcoming field, uses the concept of nanotechnology to implement practical nanoscale systems. Progress in this field is necessary to realize and implement next-generation devices. The simulated device features a vertically aligned plasma assisted carbon nanotube as the channel synthesized using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. Among the known synthesis techniques for CNT, PECVD offers increased controllability of the resultant structure, which as an added advantage, is attained at a relatively lower temperature [9-12]. Vertically aligned structures are attained due to the plasma sheath's electric field, which applies force on the carbon nanostructures [13-15]. New age CNT-based FETs predominantly use Silicon Dioxide (SiO_2) as a gate oxide. It has been the choice of material to be used as a gate dielectric for an incredibly long time, thanks to its unparalleled robustness and stability. However, SiO_2 has started acting as a roadblock to further improvements in performance and efficiency owing to scalability issues. SiO_2-based devices have begun to hit the peak of their performance figures [16]. Keeping this in mind, efforts are better spent on novel materials that can act as alternatives to SiO_2. This quest has led to increased attention being poured to high-k oxides such as HfO_2. HfO_2 has emerged as the most viable new-age replacement for SiO_2 and is the primary material under inspection in this research [17-19].

Incorporating high-k materials, such as HfO_2, help reduce leakage current and increase gate capacitance, thus improving device performance. The device in contention features a dual-metal gate in a cylindrical structure. Hafnium Oxide (k = 22) is used as the gate dielectric, and a comparative study is performed in order to inspect the device characteristics such as drain current (I_{ds}), transconductance (g_m), output conductance (g_d), early voltage (V_{EA}), and gate capacitance (C_{GG}). SILVACO TCAD has been used as a simulation tool to implement the device and analyze its characteristics. The rising prominence of CNTFETs has drastically improved the performance and usability of sensors used in healthcare and other prominent industries. Owing to the high speed of detection, significantly better scaling technology, and higher efficiency, CNTs have become the primary material of choice in the industry for high-sensing applications. In order to investigate and draw more insights into the simulated device's real-life applicability, a nanogap cavity is created within the HfO_2 layer. The latter half of this research uses the dielectric modulation technique to understand better the variation of performance with changing values of the dielectric constant of this nanogap cavity. Changes in electrical characteristics such as I_{ds}, g_m, g_d, Transconductance Generation Factor (TGF), threshold voltage V_{th}, I_{ON}/I_{OFF} Ratio, C_{GG}, cut-off frequency f_c, Gain Bandwidth Product GBWP. Sensitivity parameters like drain current sensitivity, I_{ON}/I_{OFF} sensitivity for the above-proposed device, for different dielectric constant values (k = 1, 2, 4, 8 and 16) occupying the cavity have been recorded. This analysis is also critical for the real-life applicability of the device since it can be deployed in a health monitor device.

4.3 DEVICE SIMULATION MODEL

Figure 4.1 and Figure 4.2 represent the 3-D and cross-sectional view of the HfO_2-based Plasma-Assisted Gate All Around Carbon Nanotube FET (GAA-CNTFET). The PECVD technique leads to the formation of vertically aligned CNTs, which is used as the channel here. The synthesis of CNT via the PECVD experimental method is done using precursor gases such as argon and methane on silicon and nickel-coated substrates at relatively lower temperatures [20]. As the name suggests, HfO_2 is used as a high-k gate dielectric in the device, with thickness fixed at 2 nm. The simulated device has a dual gate structure with cylindrical geometry. The gates are devised of different materials with metal-gate-work-function equivalent to 4.4 at the drain and 4.7

at the source. Metallic source and drain contacts with a uniform doping concentration of 10^{18} cm^{-3} are used at either end. Table 4.1 represents the device's structural parameters. Silvaco TCAD offers a variety of models that help in the accuracy and predictability of the simulation [21]. Leakage currents are simulated using Shockley-Read-Hall (SRH) model, whereas minority carrier recombinations are taken into account using the Auger recombination model. Mobility parameters such as "MUN" and "MUP" have been used for electrons and holes. Carrier statistics are looped in using the Boltzmann model, while Gummel and Newton techniques aid with numerical solutions [21,22]. Keeping the CNT radius fixed at 5 nm, characteristics are noted for three sets of plasma parameters that correspond to the following values of channel length − 1.5 µm, 2.5 µm & 3.5 µm. Similar observations are made by replacing HfO_2 with SiO_2 to help with a comparative study. Figure 4.3 (a) and Figure 4.3 (b) show that the simulation results achieved after designing the HfO_2-based GAA-CNTFET device are seen following the same trajectory as the device investigated by Kansal and Sharma (Theoretical), Yang and Mohanram (Experimental) [22,23] and Franklin et al. [24] respectively. There can be seen a difference in magnitude between the experimental and simulated results due to basic differences in structure. The process recipe for a GAA-CNTFET fabrication is explained as follows. The concentric structure for GAA-CNTFET is fabricated using the wrap-around process [25]. A suspended carbon nanotube is prepared for this process by exposing it to NO_2 gas and trimethylaluminum vapor. On top of this functionalized CNT, the oxide layer is deposited using the ALD process. Process for synthesis of a stacked oxide structure can be explained by Ge at al. [26]. Using the ALD process again, the gate material is deposited over the dielectric. Gate and source metallic end points are accommodated at the very end on each side of the structure. The layers of materials deposited using ALD can be verified using transmission electron microscope imaging (TEM) and Scanning Electron Microscope (SEM).

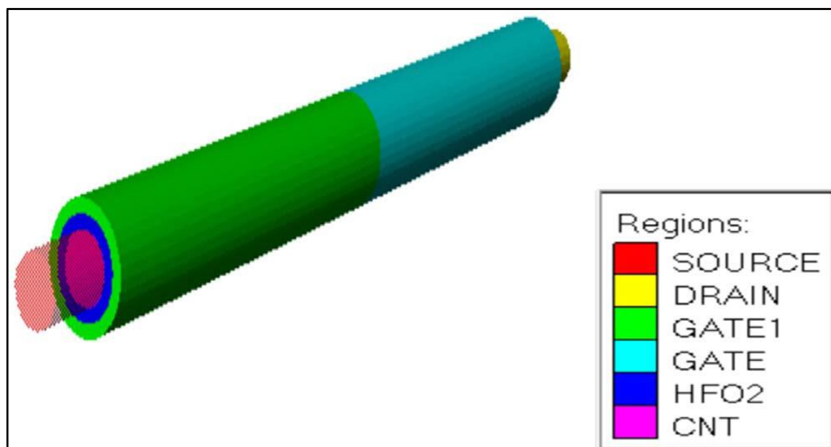


Figure 4.1: 3-D structure of cylindrical GAA-CNTFET

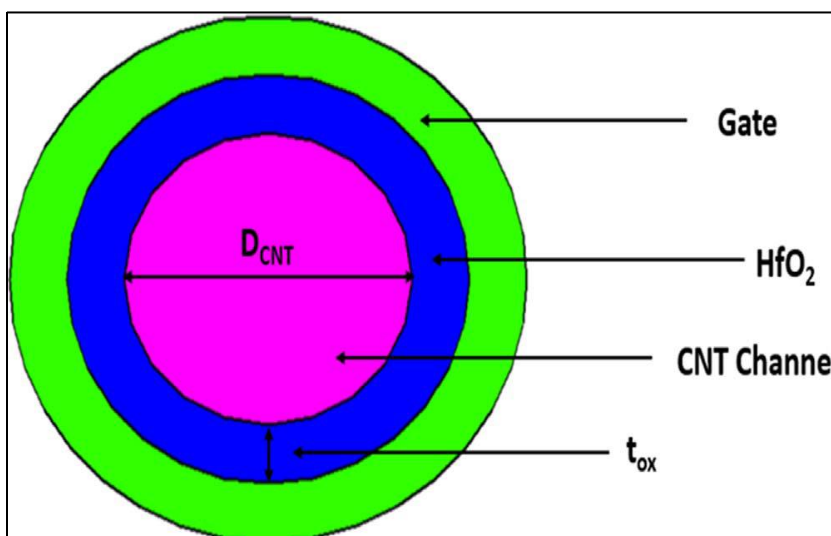
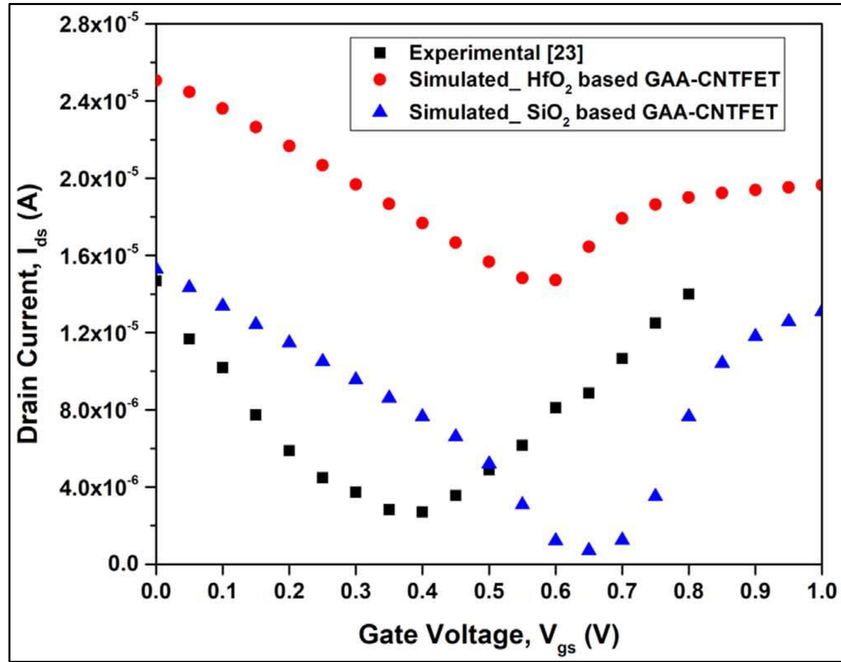
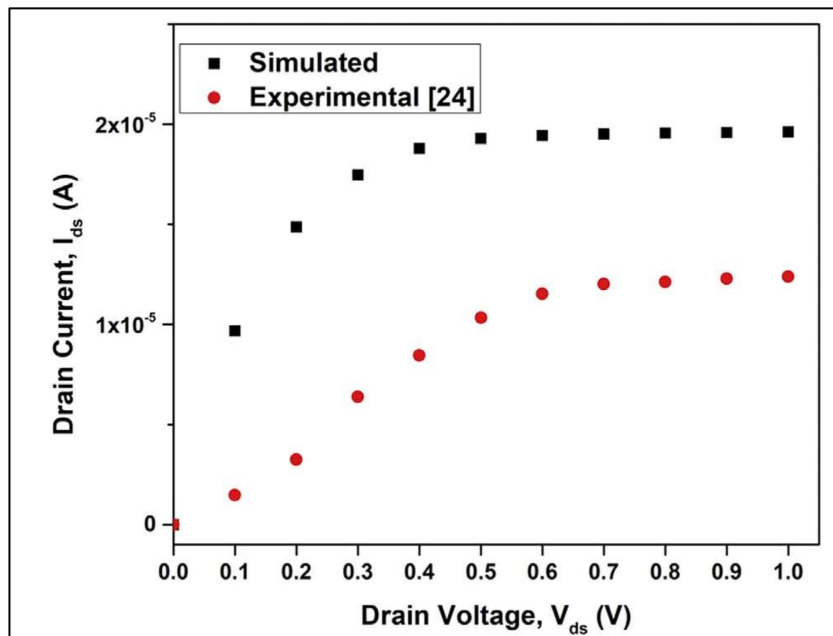


Figure 4.2: Cross-sectional view of cylindrical GAA-CNTFET



(a)



(b)

Figure 4.3: Comparison of simulated devices with (a) experimental results by Kansal and Sharma (Theoretical) and Yang and Mohanram (Experimental) [22,23] at V_{ds} = 0.8 V (b) experimental results by Franklin et al. [24] at V_{ds} = 0. 75 V

Table 4.1: Device Specifications

Parameter	Symbol	Value(s)
Oxide thickness (nm)	t_{ox}	2
Source/ Drain Length (nm)	L_s/L_d	15
Gate work function (eV)	ϕ_1, ϕ_2	4.4, 4.7
HfO_2 Permittivity	ε_{ox}	22
Channel Radius (nm)	R	5
Channel Length (µm)	L	1.5, 2.5, 3.5

Table 4.2: Plasma parameters variation corresponding to varying values of channel length (at a constant value of R = 5 nm)

Case	Channel Length (µm)	Plasma Parameter I - electron density n_{eo} (cm^{-3})	Plasma Parameter II - electron temperature T_{eo} (eV)	Plasma Parameter III - ion density n_{io} (cm^{-3})	Plasma Parameter IV - ion temperature T_{io} (K)
Case 1	1.5	$8x10^8$	1.15	$7x10^7$	2200
Case 2	2.5	$2x10^9$	1.25	$6x10^8$	2235
Case 3	3.5	$8x10^9$	1.35	$2x10^9$	2280

4.4 RESULTS AND DISCUSSION

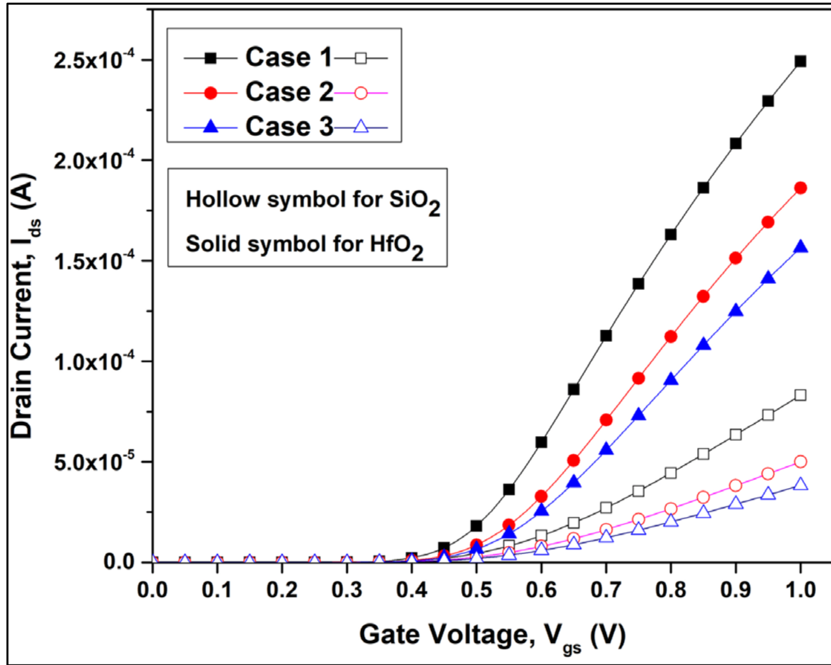
The work done by Sharma and Tiwari [27] has aided researchers in decoding the unknowns of the PECVD process. As mentioned above, the PECVD process offers superior control over the resultant CNT geometry. It is made possible through plasma parameters, also known in this reference as glow discharge parameters. The proposed physical model developed by them can be used to draw a link between these parameters and device geometry. It can be shown that for a certain set of plasma parameters, the CNT length increases initially with time before it saturates. The saturation value increases with increasing plasma parameter values, as shown in Table 4.2. Sharma and Tiwari's work, and subsequently this research, concerns itself with the following plasma parameters - electron density n_{eo} and electron temperature T_{eo}, ion density n_{io} and ion temperature T_{io}. Increasing values of n_{io} and T_{io} lead to a faster generation of

carbon monomers, thus leading to more diffusion of carbon ions [27-29]. This leads to an increase in CNT length. PECVD parameters directly influence device performance because they influence device geometry (radius and length) [30]. Control and a better understanding of PECVD parameters are critical for deciphering performance metrics. This research intends to take the broader problem statement of unknowns of plasma parameters and break down their control over the resulting device. Silvaco 3D ATLAS TCAD simulator simulates the device and its subsequent performance analysis.

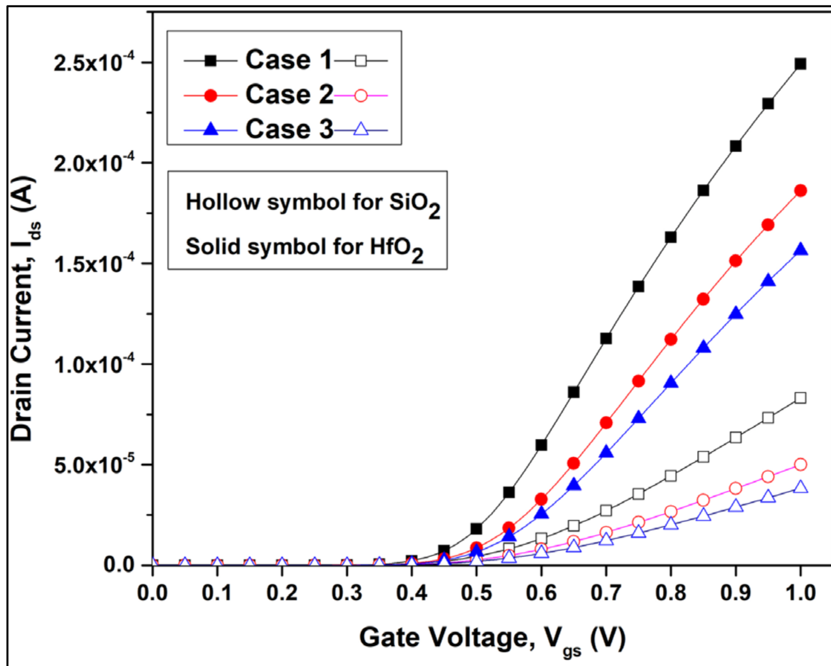
4.4.1 IMPACT OF VARIATION OF PLASMA PARAMETERS FOR SiO_2 AND HfO_2 BASED GAA-CNTFET

This research has a HfO_2-based GAACNTFET device at its centre stage, which is compared to a similar configured SiO_2-based GAA-CNTFET and results for the same can be seen in the subsequent section. From Figure 4.4 (a) and Figure 4.4 (b), it can be seen that the simulated device showcases considerable improvements in transfer and output characteristics as compared to SiO_2-based GAA-CNTFET for altering values of plasma or glow discharge parameters. HfO_2 benefits from a reduced band gap of 5.3 eV compared to SiO_2, which has a bandgap of 9.0 eV [18]. The lower energy band gap means a faster generation of carriers, thus leading to an improved drain current, hence improved characteristics. Figure 4.5.(a) shows the variation in transconductance g_m w.r.t. gate voltage V_{gs} at constant drain voltage V_{ds} = 0.8 V. Figure 4.5 (b) and Figure 4.6 show the variation of output conductance g_d and early voltage V_{EA} respectively w.r.t. V_{ds} at constant V_{gs} = 0.5 V respectively.

All properties show improvement after incorporation of high-k dielectric such as HfO_2. This is attributed to the high capacitance offered by HfO_2, which leads to a rise in the carrier concentration in the channel region. Transconductance, used to measure the optimum bias point, is a direct representation of the device's switching speed. Higher transconductance implies a better switching speed of the device [22]. The properties mentioned earlier, such as g_m and g_d, show an increasing trend with a drop in values of plasma parameters. The improvement in g_m and g_d on the inclusion of HfO_2 is due to their direct dependence on variation in drain current. The enhanced capacitance due to the high permittivity of HfO_2 results in an improved electric field, boosting electron velocity. Thus, the faster movement of electrons increases the drain current.

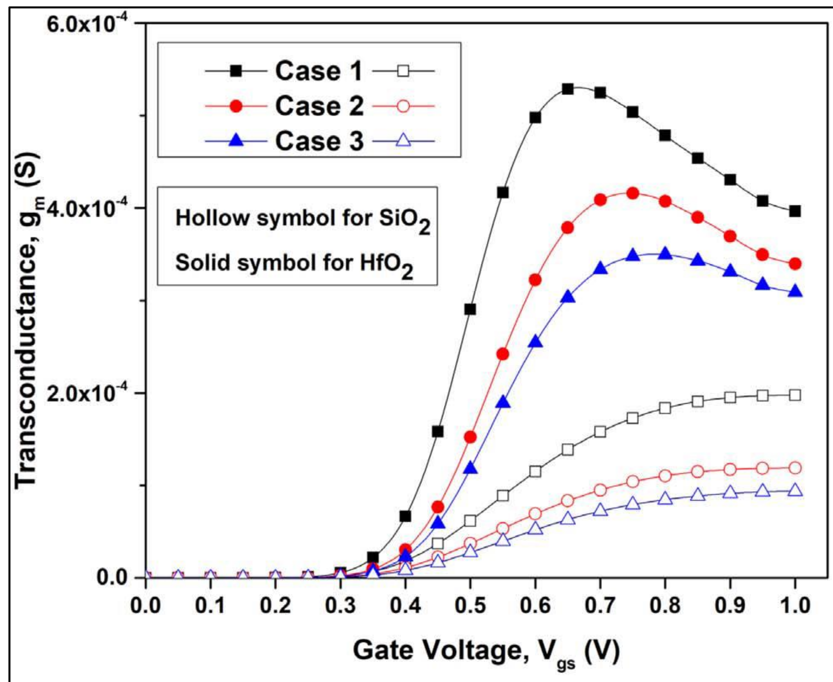


(a)

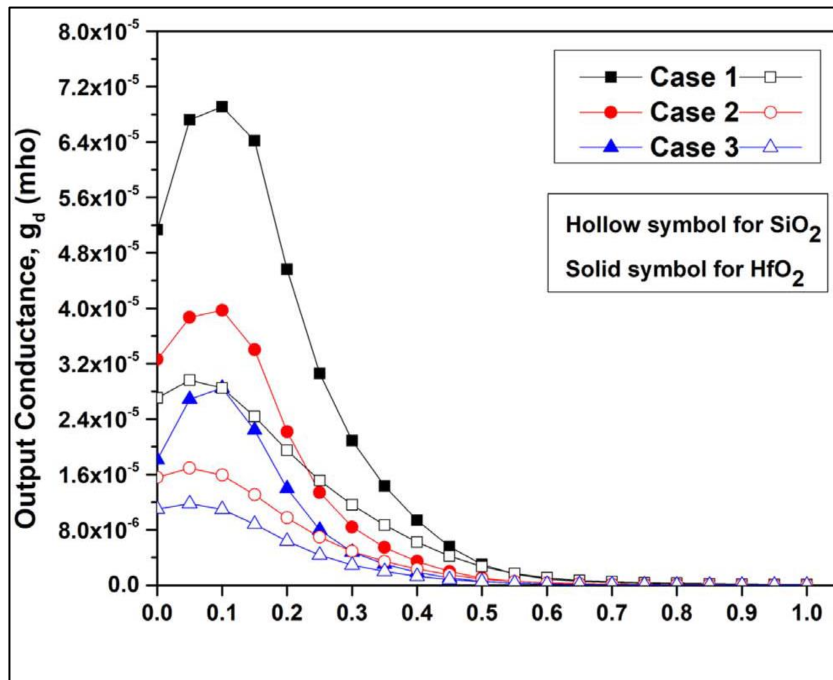


(b)

Figure 4.4: Impact of variation of plasma parameters (Table 4.2) for both SiO_2 and HfO_2 based GAA-CNTFET on (a) transfer characteristics at V_{ds} = 0.8 V (b) output characteristics at V_{gs} = 0.5 V



(a)



(b)

Figure 4.5: Impact of variation of plasma parameters (Table 4.2) for both SiO_2 and HfO_2 based GAA-CNTFET on (a) transconductance, g_m at $V_{ds} = 0.8$ V (b) output conductance, g_d at $V_{gs} = 0.5$ V

Early voltage, V_{EA} is a measure of the amplifying capacity of the device under consideration [31]. Also, from Figure 4.6, it is seen that HfO_2-based GAA-CNTFET showcases greater V_{EA} values than SiO_2-based GAA-CNTFET.

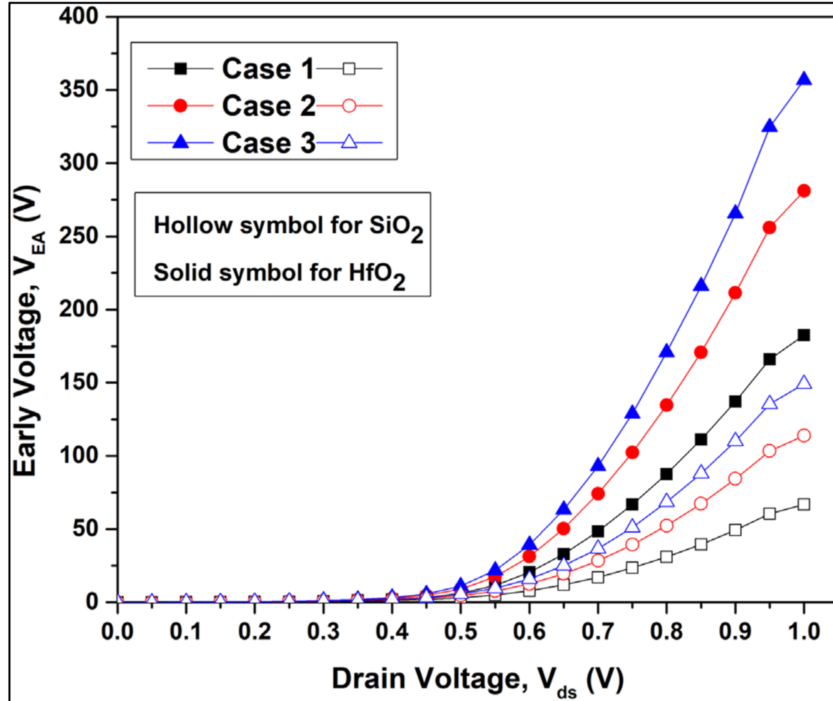


Figure 4.6: Impact of variation of plasma parameters (Table 4.2) for both SiO_2 and HfO_2 based GAA-CNTFET on Early voltage, V_{EA} at $V_{gs} = 0.5$ V

The total Gate Capacitance C_{GG}, which is a combination of the gate to source capacitance, C_{GS} and gate to drain capacitance, C_{GD}, can be observed varying with different values of plasma parameters for both SiO_2 and HfO_2-based GAA-CNTFET in Figure 4.7. HfO_2 based device exhibits superior C_{GG} values compared to its SiO_2 based counterpart.

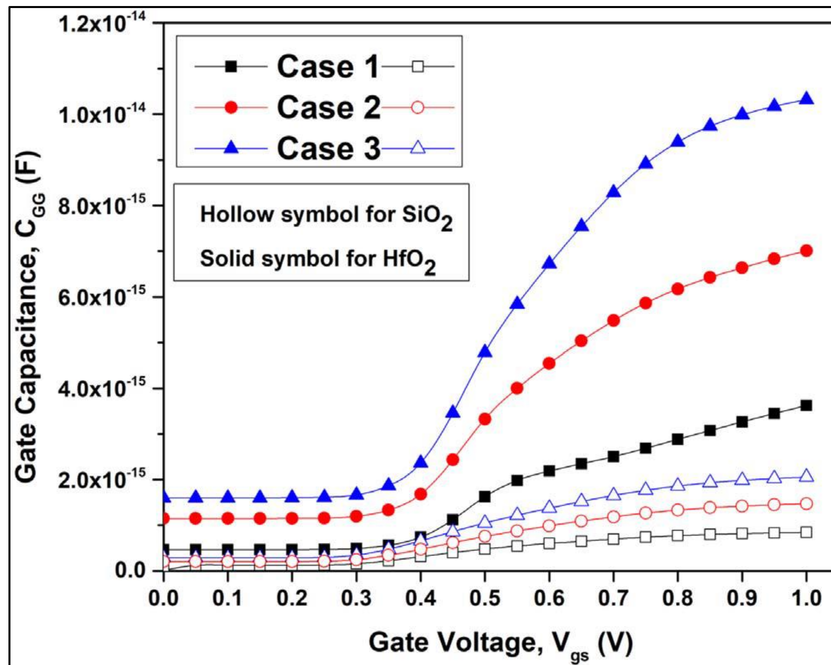


Figure 4.7: Impact of variation of plasma parameters (Table 4.2) for both SiO_2 and HfO_2 based GAA-CNTFET on Gate Capacitance, C_{GG} at V_{ds} = 0.8 V

4.4.2 DIELECTRIC MODULATION OF HfO_2 BASED GAA-CNTFET FOR SENSING APPLICATIONS

After concluding the possible performance improvements due to the inclusion of HfO_2 in the GAA-CNTFET device, the focus is now on implementing the dielectric modulation technique through a specialized architecture. The 2-D view of the device structure shown in Figure 4.8 is similar to the device used before, with the simple addition of a cavity carved beneath the gate inside the HfO_2 region. The working principle behind this is that when different molecules are immobilized inside the cavity, alterations in the dielectric constant (k) lead to modulation in the device's electrical properties. In line with the novel nature of work, sensitivity analysis will further help examine how a device of such architecture and configuration will behave to be deployed in health monitor systems, gas sensors and more.

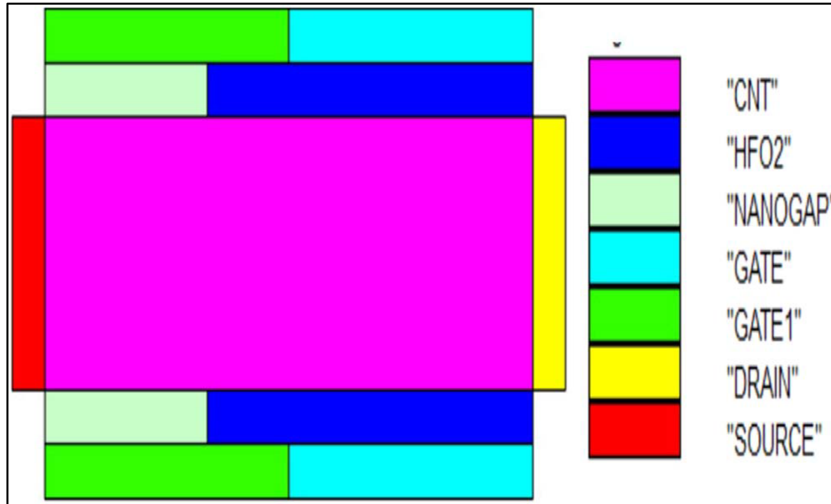


Figure 4.8: 2-D structure of cylindrical GAA-CNTFET with nanogap cavity

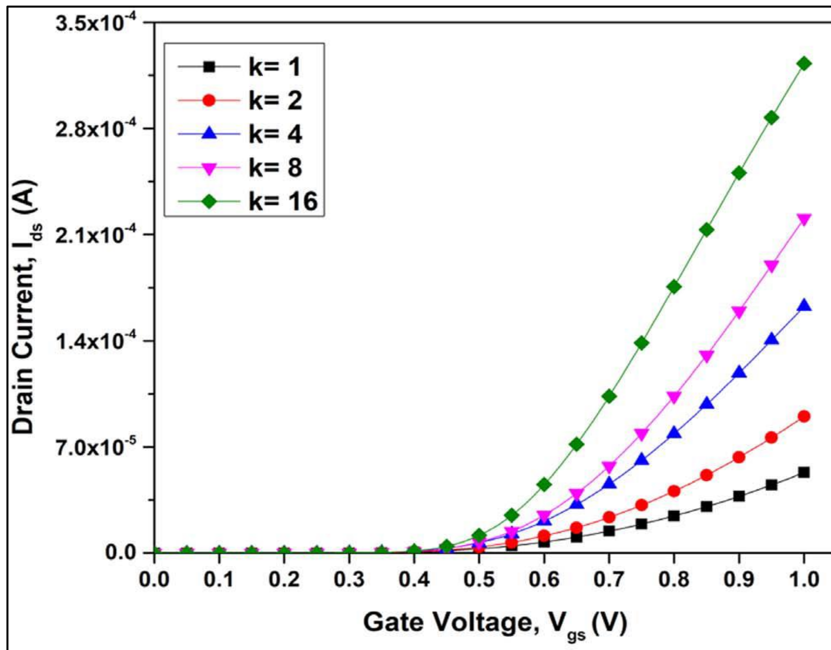
From Figure 4.9 (a) and Figure 4.9 (b), it can be seen that there is an improvement in drain current with increasing dielectric constant. On increasing the k-value, the capacitive nature increases as it is directly proportional to k, increasing the electric field lines and accumulating more charges. Hence, a rise in the current can be observed. Figure 4.10 (a) pictures the variation of g_m w.r.t. V_{gs} at constant V_{ds} = 1.0 V for varying k values. As transconductance is the derivate of the drain current, it increases with an increase in drain current for changing k values.

When occupied with high-k material, the device has better gate controllability over the channel. Transconductance Generation Factor TGF is one of the key metrics for analogue applications and explains the amount of AC gain that can be extracted from DC power [32,33]. Mathematically, it can be represented by Eq. (4.1). High values of TGF allow for low-power and high-gain analogue circuits. From Figure 4.10 (b), it can be concluded that the value of TGF is higher with a larger dielectric constant. This can be credited to a more prominent effect of g_m than I_{ds} as both g_m and I_{ds} increase with increasing dielectric constant values.

$$TGF = \frac{g_m}{I_{ds}} \tag{4.1}$$

The minimum gate voltage at which the transistor is turned ON and begins the conduction process is expressed by threshold voltage V_{th}. Figure 4.11 represents the

variation in g_d w.r.t. V_{ds} at constant V_{gs} = 0.5 V. Better performance in terms of higher g_d is tilted towards higher permittivity.



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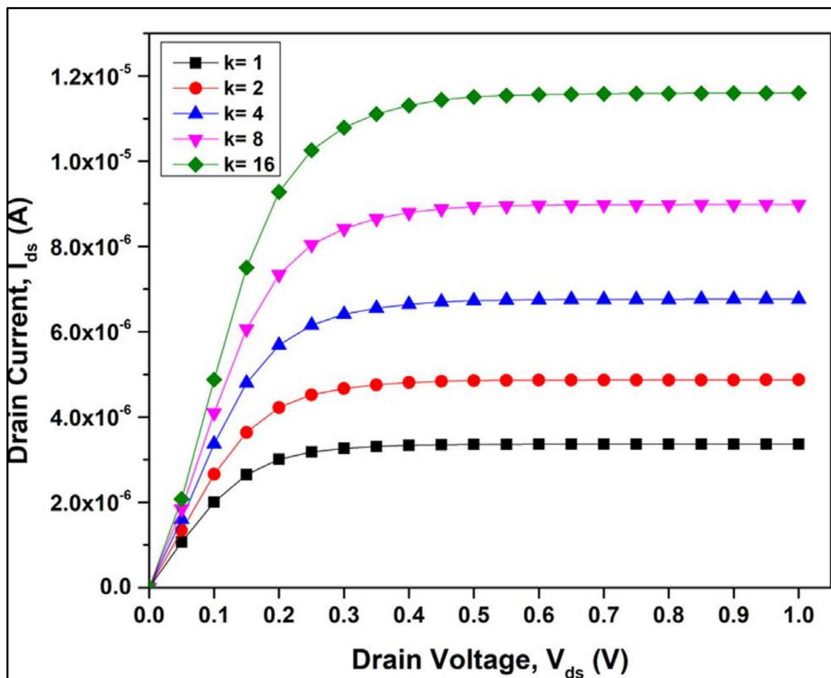
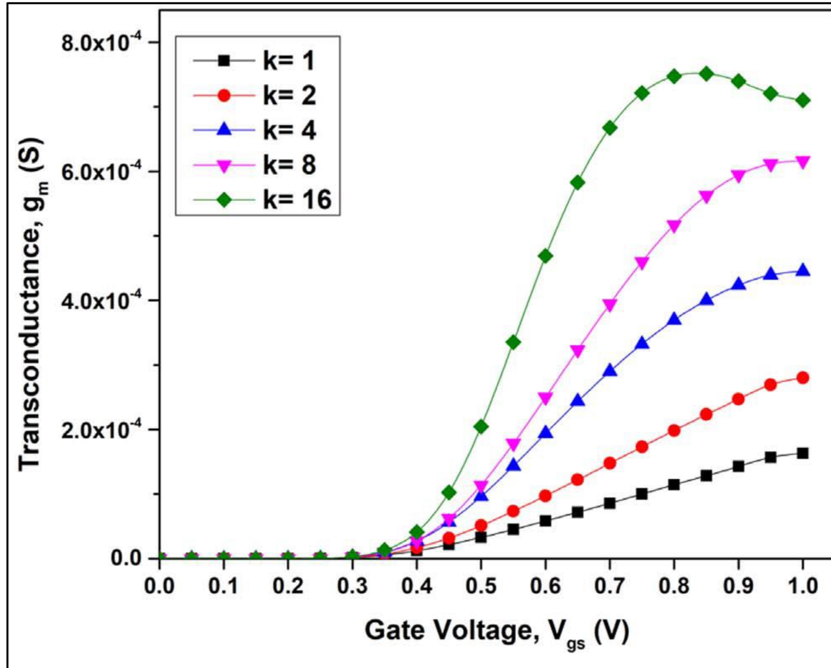


(b)

Figure 4.9: Impact of variation of dielectric constant on (a) transfer characteristics at V_{ds} = 1.0 V (b) output characteristics at V_{gs} = 0.5 V



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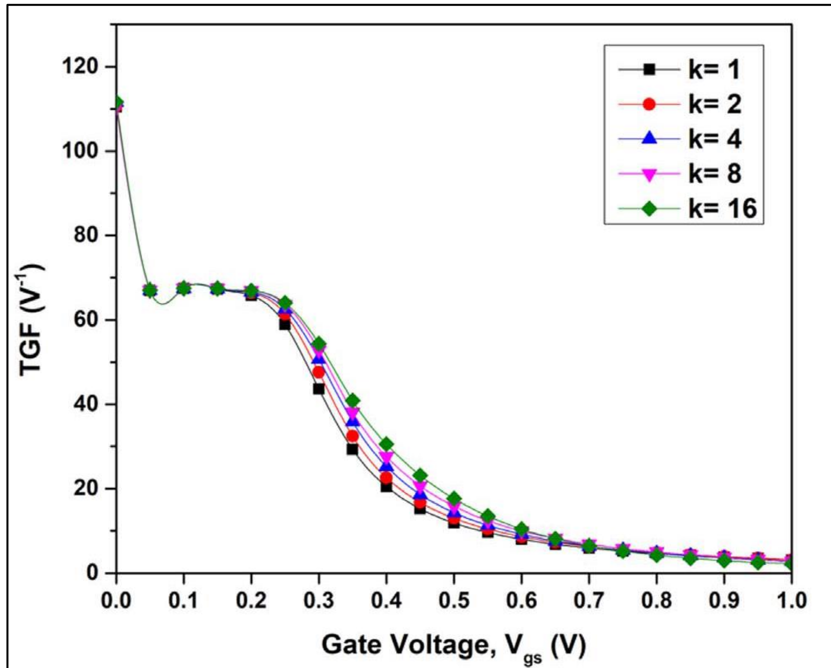


(b)

Figure 4.10: Impact of variation of dielectric constant on (a) g_m (b) TGF at V_{ds} = 1.0 V

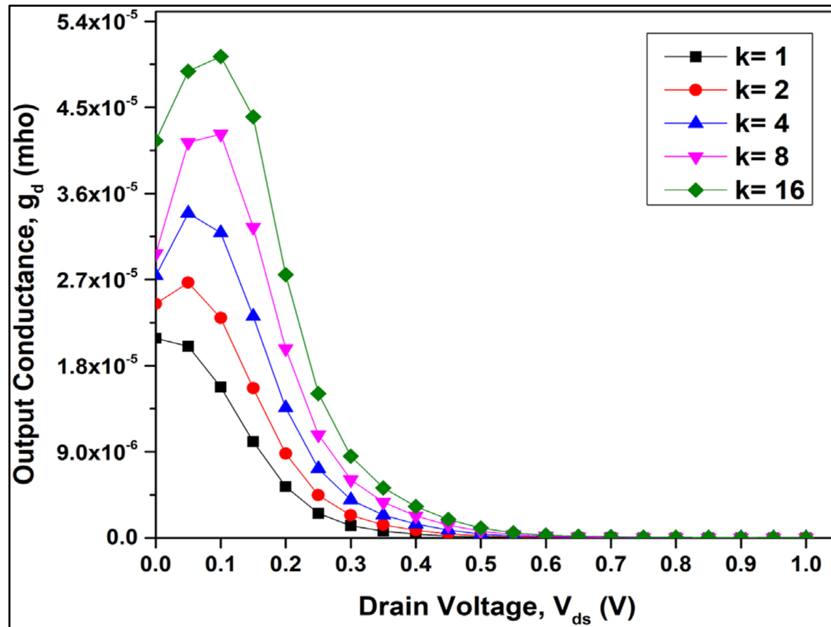
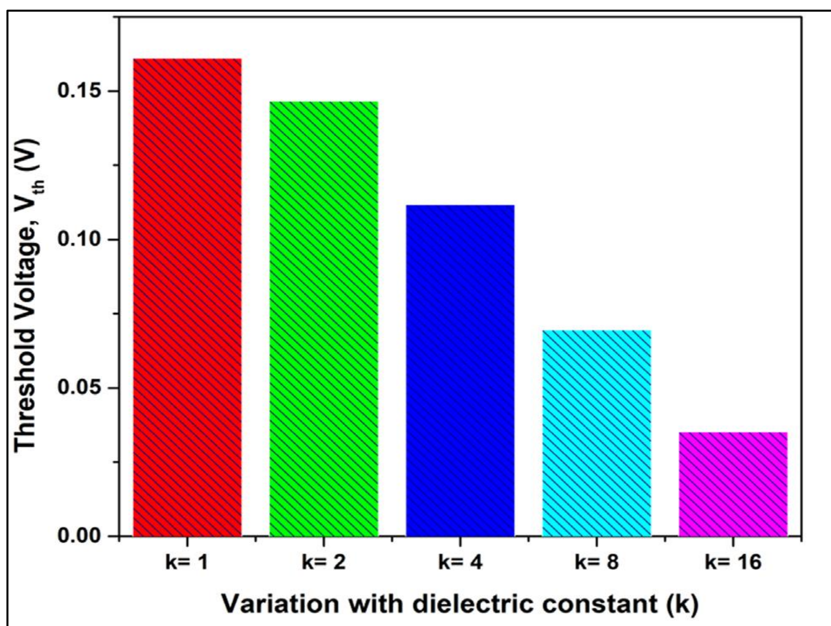


Figure 4.11: Impact of variation of dielectric constant on g_d at V_{gs} = 0.5 V

The drift in V_{th} by tailoring the dielectric constant can be observed in Figure 4.12 (a), and it can be concluded that the value of V_{th} shows decrement with increasing dielectric constant of the nanogap cavity. Figure 4.12 (b) shows the I_{ON}/I_{OFF} ratio variation for the chosen dielectric constant molecules. This ratio is a representation of the switching speed of the device for digital applications. Hence, a higher value is preferred to judge the real-life applicability of the device. Any progress toward a better understanding of the simulated HfO_2-based GAA-CNTFET for sensing applications is left incomplete without a sensitivity analysis. In almost all cases, high sensitivity is preferred because it represents a high probability of detecting the target species.

The drain current sensitivity can be defined as the relative improvement in drain current of a particular material compared to air, and its variation with V_{gs} can be seen in Figure 4.13 (a). The improvement in sensitivity can be attributed to an improvement in drain current with an increment in dielectric constant in the nanogap cavity. Alongside drain current sensitivity, another critical parameter to assess the device's sensitivity is the I_{ON}/I_{OFF} sensitivity ratio, and its variation can be seen in Figure 4.13 (b). Much like the previous one, the I_{ON}/I_{OFF} sensitivity ratio is the relative improvement in the I_{ON}/I_{OFF} ratio of a particular material compared to air. The I_{ON}/I_{OFF} sensitivity ratio with increasing dielectric constant can be explained by improving the I_{ON}/I_{OFF} ratio as given in Figure 4.12 (b).



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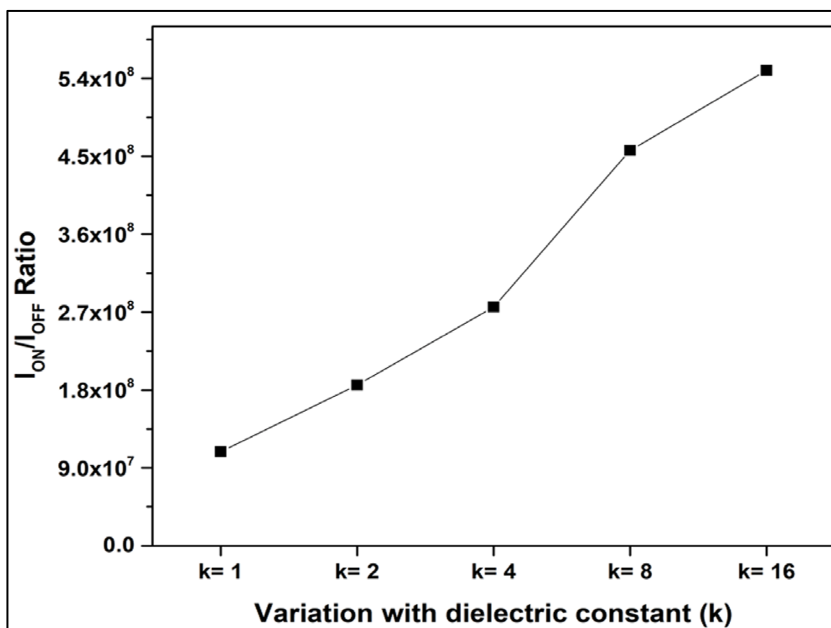
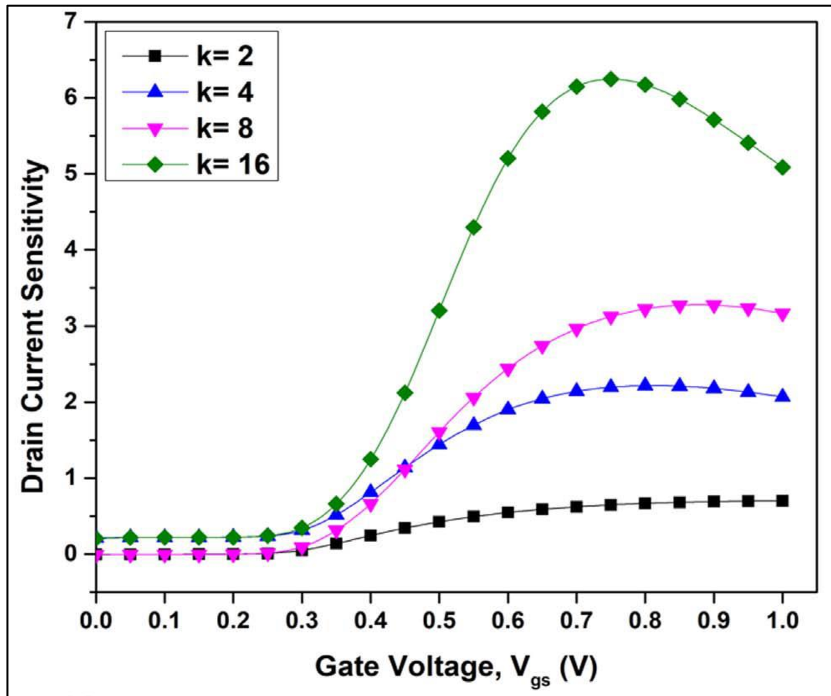


(b)

Figure 4.12: Impact of variation of dielectric constant on (a) Threshold voltage, V_{th} (b) I_{ON}/I_{OFF} Ratio at V_{ds} = 1.0 V



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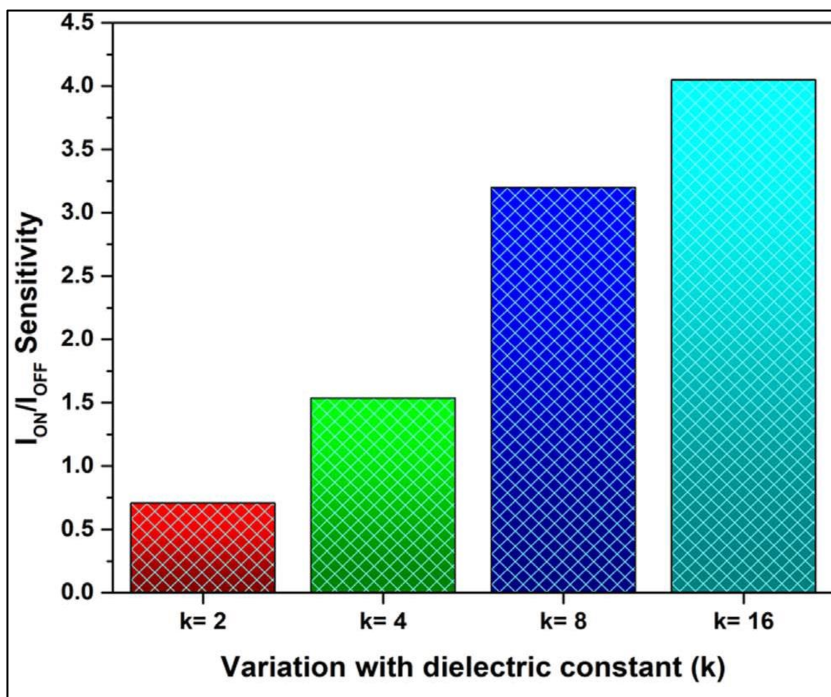


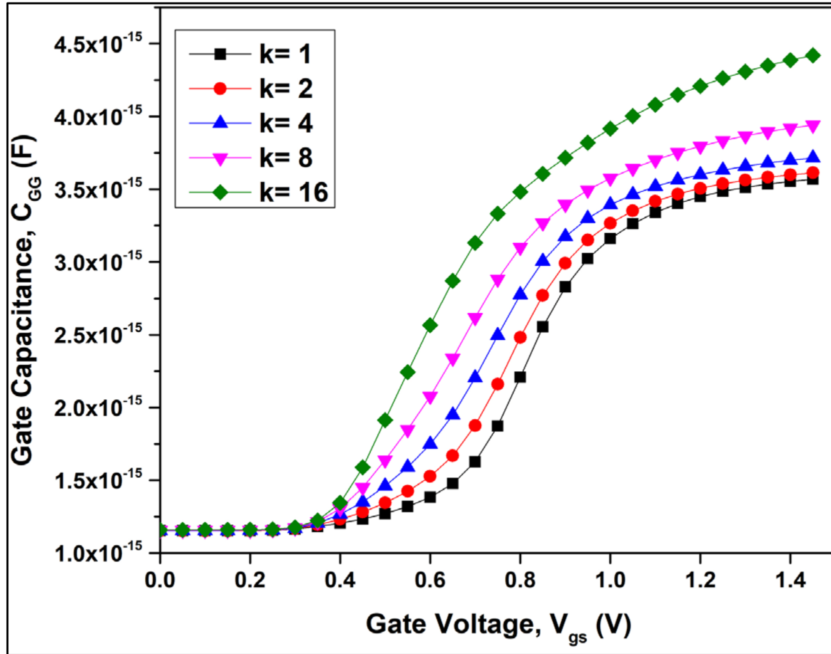
(b)

Figure 4.13: Impact of variation of dielectric constant on (a) Drain Current Sensitivity (b) I_{ON}/I_{OFF} Sensitivity at $V_{ds} = 1.0$ V

In order to analyze the RF performance of the proposed device, certain essential parameters such as Gate Capacitance C_{GG}, Cut-off Frequency f_c, and Gain-Bandwidth Product GBWP have to be studied. These parameters are plotted in Figure 4.14 (a), (b), (c) respectively. C_{GG} and f_c show increasing values for increasing k. As it is obvious from Eq. (4.2), f_c has a direct dependence on g_m and an inverse relation with C_{GG} [33]. However, in this case, g_m's effect is more pronounced than C_{GG}. The Gain-Bandwidth Product is a crucial metric deployed in high-frequency applications and can be formulated as shown in Eq. (4.3) [34,35]. The peak value of GBWP increases with the rise in k due to the more pronounced increment in transconductance compared to the gate-to-drain capacitance C_{GD}.

$$f_c = \frac{g_m}{2\pi C_{GG}} \tag{4.2}$$

$$GBWP = \frac{g_m}{20\pi C_{GD}} \tag{4.3}$$



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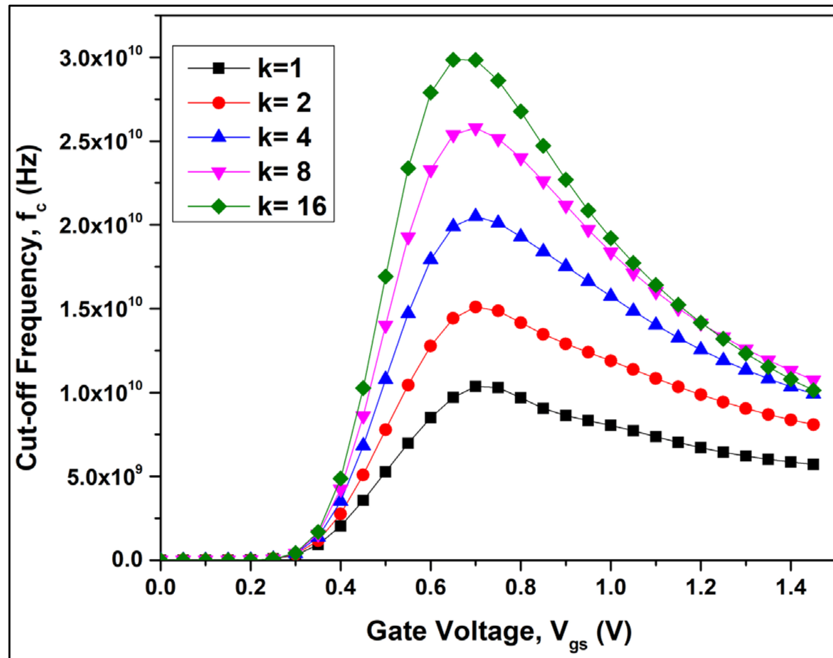

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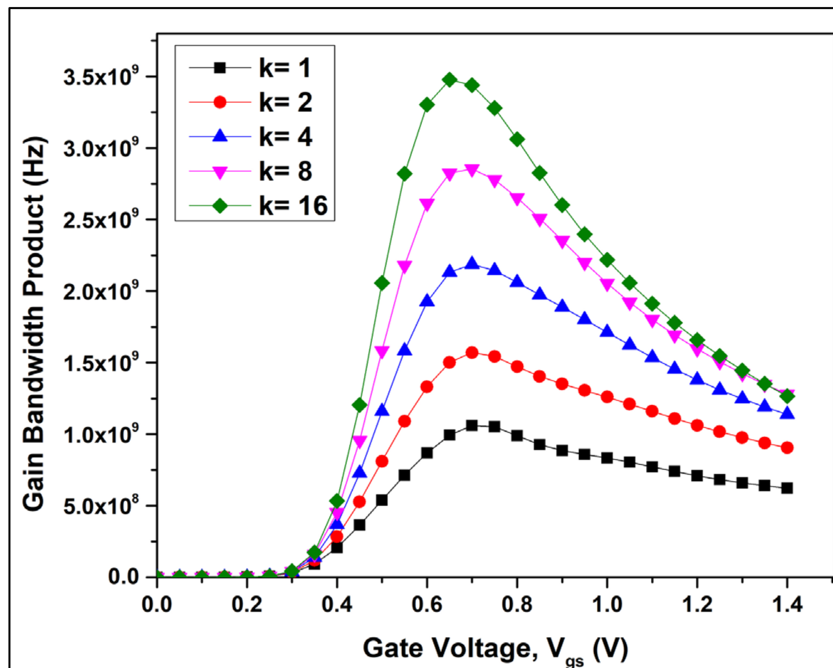

(c)

Figure 4.14: Impact of variation of dielectric constant on (a) C_{GG} (b) Cut-off Frequency f_c (c) Gain Bandwidth Product at

The work presented in this manuscript makes a case for using the simulated device for sensor-based applications. Devices incorporating CNT as the channel benefit from the high detection speed, far improved scalability and good versatility. For the first time,

a device proposed in the manuscript is subjected to dielectric modulation, as presented here. Owing to superior heat and electrical conductivity and rapid response time, CNT-based sensory devices are used in medical, environmental & other prominent industries. With expanding interest of researchers, CNTs are predicted to become the mainstream material of choice for biosensors and other sensors as and when the challenges and unknowns are debugged with time [36,38].

4.5 CONCLUSION

This research intends to move one step closer to better understanding CNTFET devices. With the work done here, the unknowns of plasma parameters are further tackled, and important conclusions are drawn. Incorporating a non-conventional material such as HfO_2 in an already superior CNTFET device brings significant performance gains compared to last-mile upgrades possible in current ones. Using high-k dielectric leads to an improved drain current, transconductance, output conductance, early voltage and gate capacitance in the proposed device. The results showcase that HfO_2 can be used as a substitute to tackle scaling and performance constraints showcased by SiO_2. In order to propel the real-life applicability of the simulated device for sensing applications, the dielectric modulation technique was adopted, and variation in device characteristics and performance was noted. Better electrical characteristics performance and high sensitivity were tilted towards a higher dielectric value. The results are promising and make a solid case for high-sensing applications.

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Chapter- 5

PERFORMANCE ASSESSMENT OF PLASMA-ASSISTED DM-CNFET FOR SENSING APPLICATIONS AND TEMPERATURE FLUCTUATIONS

Publication

1. **Mansha Kansal** and Suresh C. Sharma, *"Numerical Simulation of Performance Metrics of Dual Metal Gate Carbon Nanotube Field Effect Transistor (DM-CNTFET) for Numerous Sensing Purposes"*, 2nd INTERNATIONAL CONFERENCE ON ADVANCED MATERIALS AND NANOTECHNOLOGY (ICAMN2022), (2022).

2. **Mansha Kansal** and Suresh C. Sharma, *"Impact of Temperature Variation on Plasma-Assisted Stacked Gate-Oxide Gate All Around CNTFET (SG-GAA-CNTFET) for High Frequency and Wireless Applications"* (Communicated)

5

PERFORMANCE ASSESSMENT OF PLASMA-ASSISTED DM-CNFET FOR SENSING APPLICATIONS AND TEMPERATURE FLUCTUATIONS

5.1 BRIEF OUTLINE

The chapter revolves around investigating practical applications of devices incorporating Carbon Nanotubes (CNTs). CNT is a paramount material in the sensing application industry due to the high speed of detection, much enhanced scaling capabilities, and enhanced efficiency. This work revolves around Plasma Enhanced Chemical Vapor Deposition (PECVD) grown CNT being deployed as a channel in two devices being investigated for two different applications – the Dual-Metal CNTFET (DM-CNFET) for sensing applications and Stacked-Gate Dual-Metal-CNTFET (DM-SGCNFET) for robustness against high temperature values and variations.

As was discussed in Chapter 4, in order to assess the proposed device for its sensing abilities, the first step is the carving of a nanogap cavity in the oxide layer and focusing on implementation of dielectric modulation by immobilization of different molecules. The research conducted in this chapter focuses on a comparative study between a SiO_2 based DM-CNFET and a similar Si-Nanowire counterpart in order to better assess the sensing superiority that CNTFETs possess. As the value of dielectric constant increases, a boost in performance metrics such as drain current, transconductance, output conductance, I_{ON}/I_{OFF} ratio, I_{ON}/I_{OFF} Sensitivity can be noted. All the mentioned metrics show increase in values on increasing the dielectric constant of the molecule. Compared to Si-Nanowire FET, the stark difference in magnitude of the mentioned values is maintained. At all investigated dielectric constants, the CNT based device showcases a 10% better sensitivity ratio compared to its Silicon counterpart.

The Stacked-Gate Dual-Metal Carbon Nanotube Field Effect Transistor (DM-SGCNFET) replaces the conventional SiO_2 gate oxide with a stacked HfO_2-SiO_2 oxide architecture and is assessed for robustness against temperature variations. This is accomplished by varying the operating temperature of the simulated device over a

range of 300K to 500K . The ability of the simulated device to tolerate temperature fluctuations and maintain stability at high temperatures can open the doors for multiple applications. Hence, a thorough RF, analog and linearity analysis is also conducted for the same. The results prove that the device maintains the desired performance levels and stability across all measure metrics at high temperatures.

This research can open multiple doors for CNTFETs and lead the way for more innovative solutions in the field of nanoelectronics.

5.2 INTRODUCTION

In this era of accelerated technological advancements, scaling down of devices has become all but mandatory. However, scaling down after a limit can lead to serious consequences which can hamper the device performance and stability. Limitations to scaling can easily resolved by incorporating new age superior materials such as Carbon Nanotube (CNT). Advancements in CNTs have made it the choice material for keeping the CMOS technology relevant [1-8]. Increasing avenues of applications has further made the acceptability of CNT significantly easier. It would be wise to considered them as the paramount material for sensing application industry due to the high speed of detection, much enhanced scaling technology and enhanced efficiency [9].

This research deals with the numerical simulation of two different devices using CNT as the channel grown via Plasma Enhanced Chemical Vapor Deposition (PECVD) technique – the Dual-Metal Carbon Nanotube Field Effect Transistor (DM-CNFET) and Stacked-Gate Oxide Dual-Metal Carbon Nanotube Field Effect Transistor (DM-SGCNFET).

The first half of the research deals with evaluating sensing applicability for DM-CNFET. This is accomplished by carving a cavity in the oxide layer and using dielectric modulation for immobilization of different molecules. Varying the dielectric constant of the nanogap cavity directly impacts the device characteristics [10,11]. A comparative study between the simulated DM-CNFET device and a Si Nanowire FET (SiNW FET) has been performed to better understand the performance gains possible with the proposed device. This is accomplished by measuring their performance against varying values of dielectric constants. The findings confirm the device's

superior sensor capabilities compared to SiNW FET. The proposed device demonstrated stability and superior performance under all simulated scenarios. CNTFETs have higher electron mobility and can operate at higher frequencies than SiNW FETs. The superior sensitivity showcased by DM-CNFET ensures that it can be a choice transistor for avenues demanding precise detection.

In the second half of the study, the DM-SGCNFET replaces the conventional SiO_2 oxide with a SiO_2-HfO_2 layered oxide structure. Such a stacked oxide configuration is offers superior performance along with comparable robustness compared to SiO_2 [12,13].

The simulated device is tested against varying values of temperature to evaluate stability at higher temperatures and robustness at different temperature values. In precision-demanding industries like space, medicine, and communication, adaptability to external variables is of paramount importance. Performance variation with temperature changes is a good measure of robustness for a device [14,15]. To accurately assess the performance, a thorough RF, analog and linearity analysis was conducted.

5.3 DEVICE SIMULATION

The focus of this study is on a Dual Metal Gate Carbon Nanotube Field Effect Transistor (DM-CNFET) that was both implemented and simulated using Silvaco TCAD simulator. The device utilizes a CNT as the channel material with dimensions of 1.5 µm in length and 5 nm in radius. The FET features a dual gate system, with one gate having a work function of 4.4 and another having a work function of 4.7 at the drain and source ends, respectively. The device also includes a 2 nm thick gate oxide, which provides robustness due to its superior bonding with the CNT channel material. To conduct dielectric modulation, a nanogap is etched into the oxide layer, which is then filled by a dummy molecule featuring varying dielectric constants that are of particular interest in this research. Silvaco provides several models that are employed in this study, including the SRH model for implementing leakage currents, the Auger recombination model to account for minority carrier recombinations, and the Boltzmann model to loop in carrier statistics [16]. To assist with numerical solutions,

Gummel and Newton techniques are utilized. This chapter also features Figure 5.1 and Figure 5.2, which showcase the 3-D and cross-sectional views, respectively, of the Plasma Assisted Carbon Nanotube Field Effect Transistor (DM-CNFET). This implementation of a DM-CNFET features a SiO_2 gate oxide.

Figure 5.3 and Figure 5.4 depict the 3-D and cross-sectional views of the Stacked-Gate Plasma Assisted Carbon Nanotube Field Effect Transistor (DM-SGCNFET). This device features a stacked gate oxide structure with HfO_2 as a high-k dielectric.

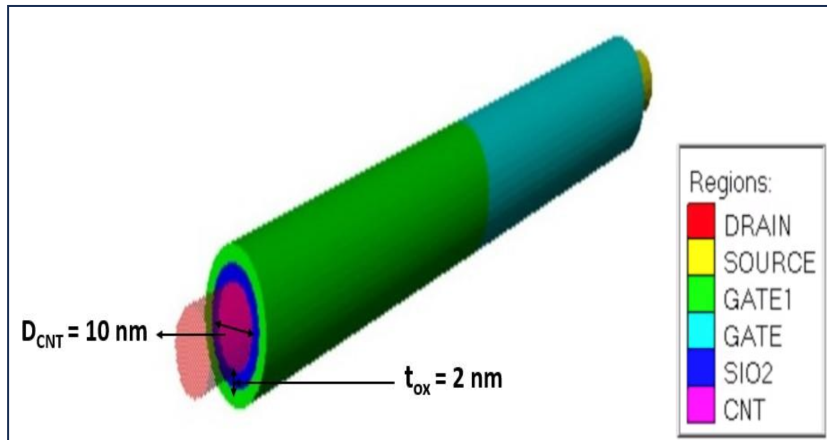


Figure 5.1: 3-D structure of cylindrical DM-CNFET

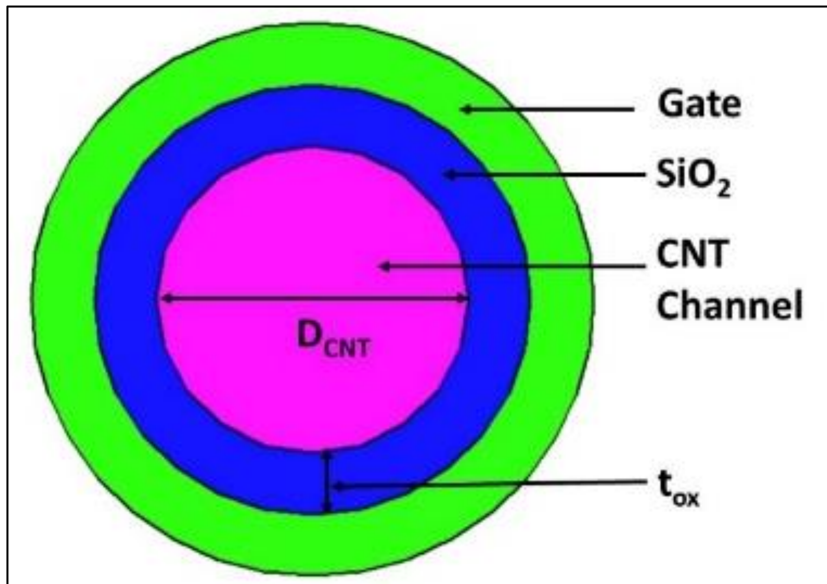


Figure 5.2: Cross- sectional view of cylindrical DM-CNFET with 1.5 μm in length and 5 nm in radius

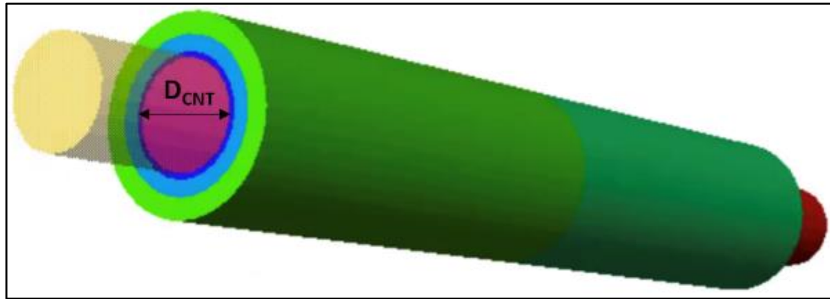


Figure 5.3: 3-D structure of cylindrical DM-SGCNFET

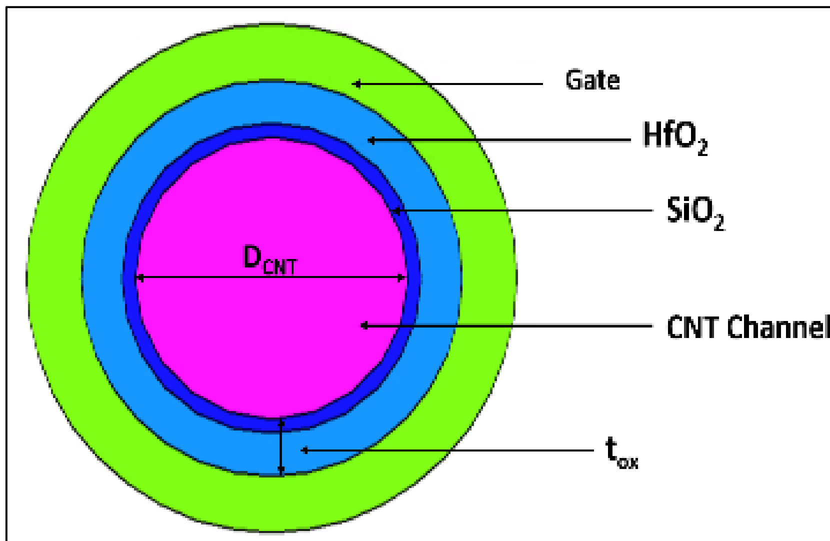


Figure 5.4: Cross- sectional view of DM-SGCNFET with SiO_2-HfO_2 stack

5.4 RESULTS AND DISCUSSION

The device simulation performed here helps in evaluating the device capability for sensing and wireless communications.

5.4.1 SENSING APPLICATIONS WITH DM-CNFET

To achieve the desired results, the first step of this research involves creating a nanogap cavity in the SiO_2 oxide layer. Subsequently, the focus is on employing the technique of dielectric modulation by immobilization of different molecules. Silvaco 3D ATLAS TCAD simulator helps in the fabrication and simulation of the proposed device and its subsequent analysis for performance metrics. Figure 5.5 and Figure 5.6 illustrate the transfer characteristics at constant V_{ds} = 1.0 V and output characteristics at V_{gs} = 0.5 V respectively for two different device configurations mentioned above. The

enhancement in performance is observed as the dielectric constant increases. As the value of dielectric constant increases, the capacitive strength increases, leading to a rise in the electric field lines. As a result, there is more accumulation of charges which further results in an increase in the drain current and transconductance g_m, both of which exhibit improved outcomes with higher k-values. CNTFET far outperforms the Si Nanowire FET owing to superior material properties such has higher mobility of electrons, thus resulting in better conductivity.

Figure 5.7 and Figure 5.8 display the changes in transconductance with respect to V_{gs} and output conductance with respect to V_{ds} for both Si Nanowire FETs and DM-CNFETs. These two properties are highly dependent on the drain current. Therefore, as the drain current increases, both devices exhibit improved outcomes in terms of transconductance and output conductance with higher k-values. Figure 5.9 shows the I_{ON}/I_{OFF} ratio for the chosen dielectric constant values, which represents the device's switching speed for digital applications [17-18]. Therefore, a higher ratio is recommended for practical applications of the device. As can be seen, DM-CNFET showcases far superior I_{ON}/I_{OFF} ratio compared to Si Nanowire FET owing to superior carrier mobility and reduced leakage current control, which further increases with increasing values of dielectric constant.

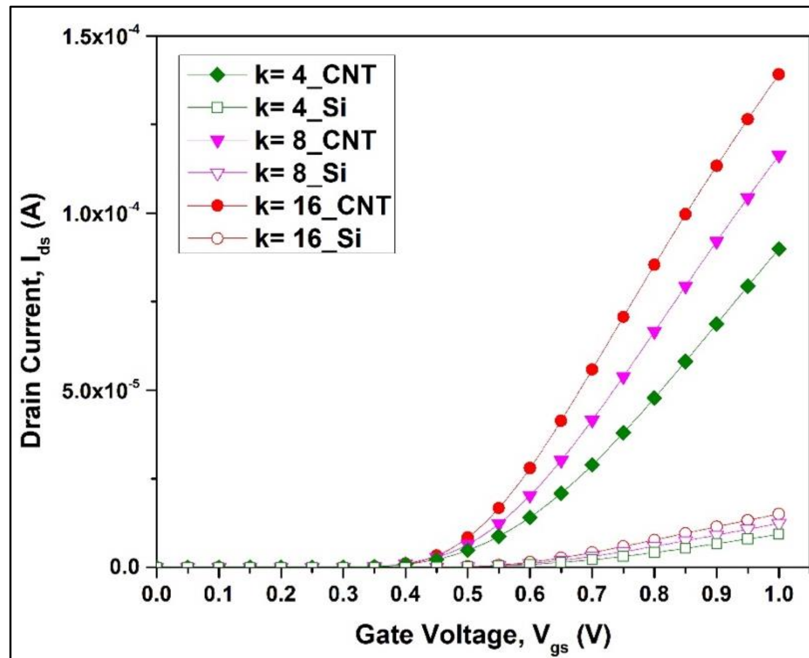


Figure 5.5: Variation of dielectric constant on transfer characteristics for SiNW FET and DM-CNFET at V_{ds} = 1V

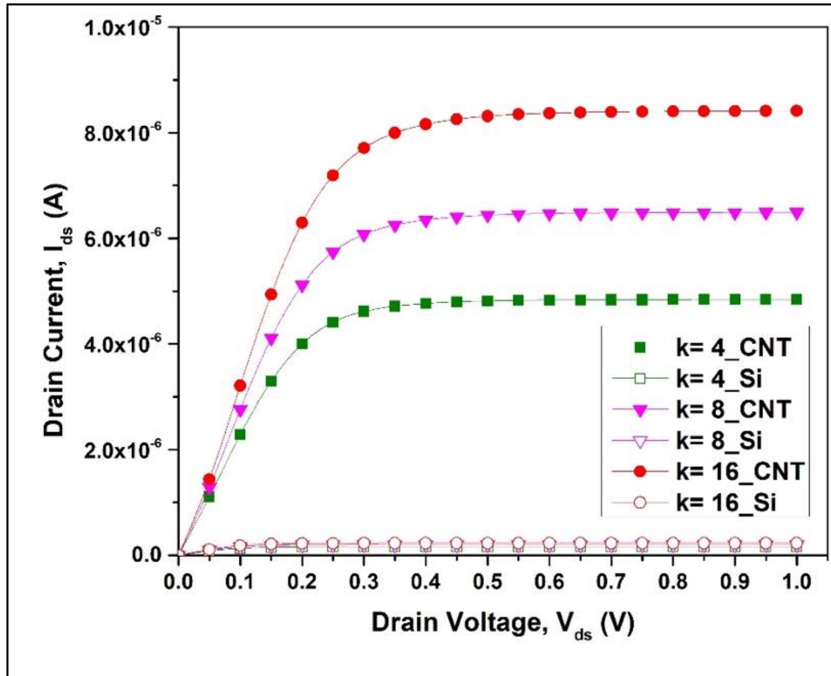


Figure 5.6: Variation of dielectric constant on output characteristics for SiNW FET and DM-CNFET at $V_{gs} = 0.5$ V

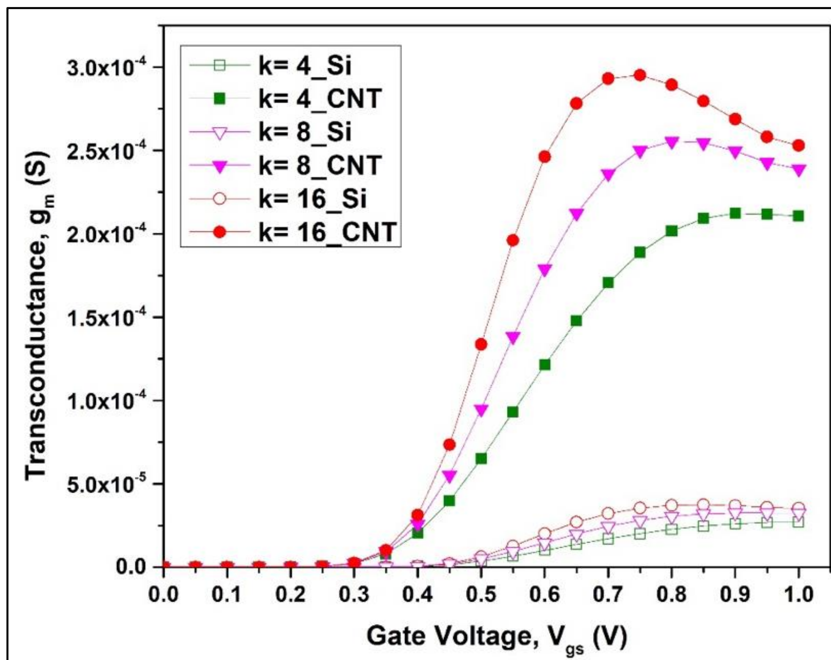


Figure 5.7: Variation of dielectric constant on transconductance, g_m for SiNW FET and DM-CNFET at V_{ds} = 1.0 V

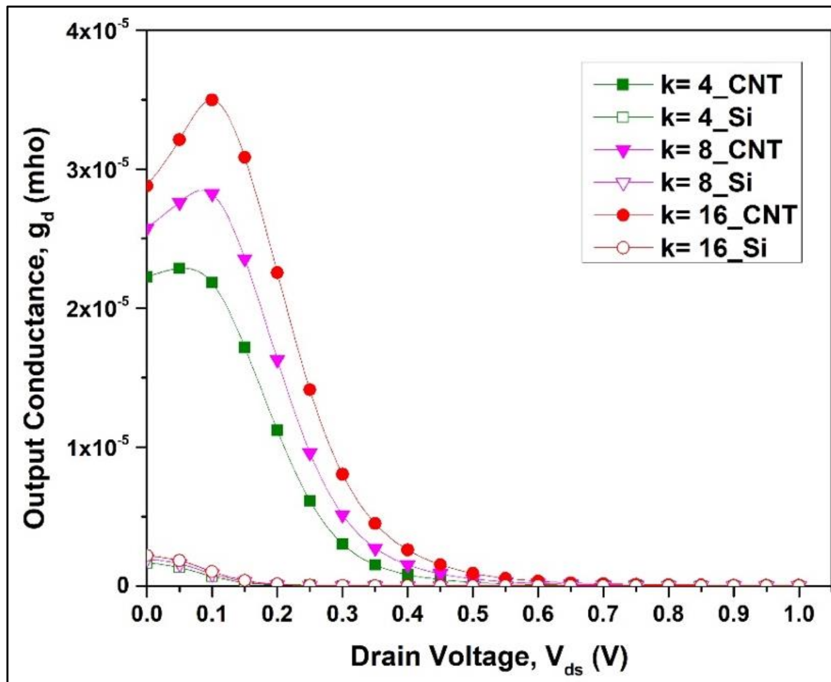


Figure 5.8: Variation of dielectric constant on output conductance, g_d for SiNW FET and DM-CNFET at V_{gs} = 0.5 V

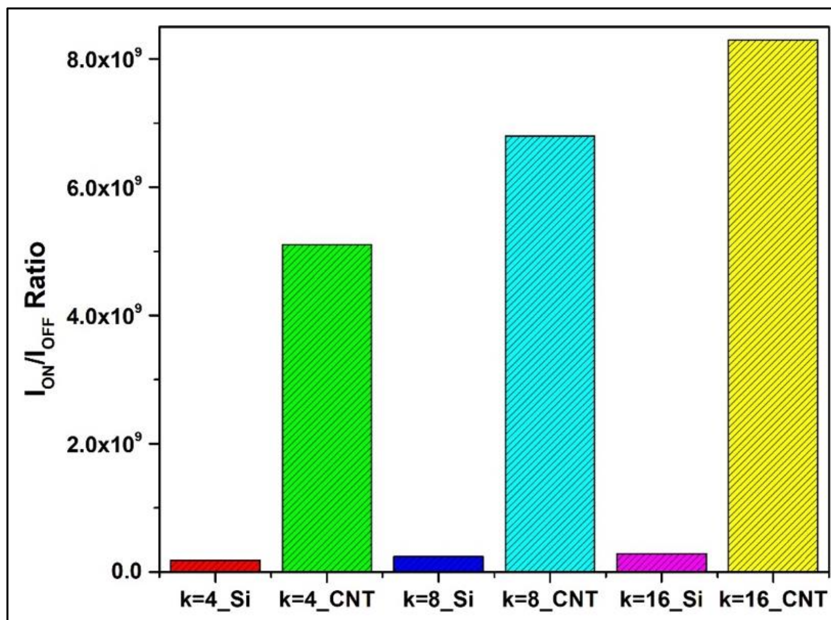


Figure 5.9: Variation of dielectric constant on I_{ON}/I_{OFF} Ratio for SiNW FET and DM-CNFET at V_{ds} = 1.0 V

In the context of the current study, sensitivity analysis is an essential metric to evaluate the effectiveness of both Si Nanowire FETs and DM-CNFETs for sensing applications. The results of sensitivity analysis can help researchers determine which device is better suited for specific sensing applications based on its ability to detect small changes in the surrounding environment. Figure 5.10 displays the changes in the I_{ON}/I_{OFF} sensitivity ratio which is the relative improvement in the I_{ON}/I_{OFF} ratio of a specific molecule when compared to air as seen in the formula below.

$$S_{molecule} = \frac{I_{ON}/I_{OFF}\,(Molecule) - I_{ON}/I_{OFF}(Air)}{I_{ON}/I_{OFF}\,(Air)}$$

The research conducted in this study provides compelling evidence in favour of using DM-CNFETs as sensor devices. CNTs, with their superior material properties, offer several advantages, including faster detection speed and greater scalability strength, compared to Si Nanowire FETs. The advantages of CNT-based sensors make them well-suited for deployment in various industries, including environmental monitoring, medical devices such as health monitoring systems, and many others [19].

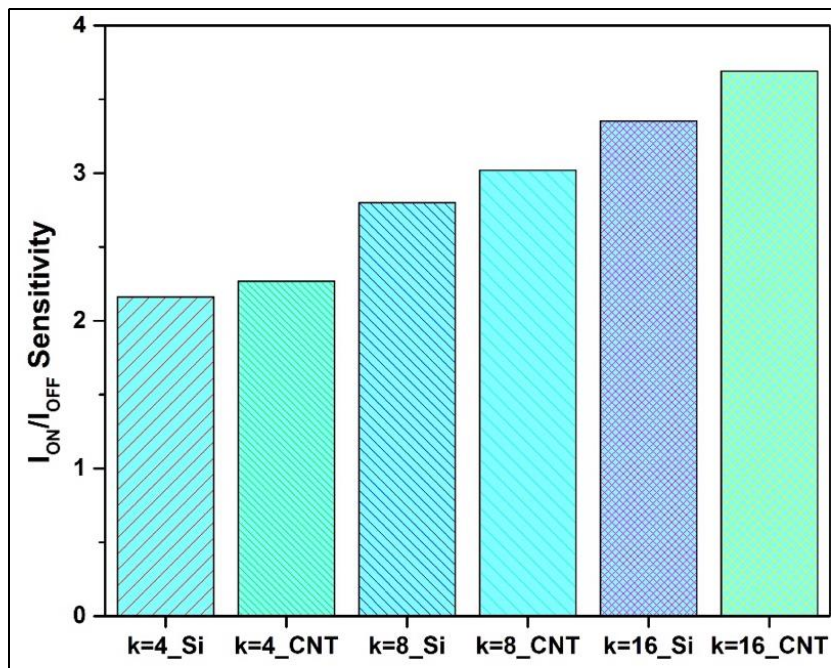


Figure 5.10: Variation of dielectric constant on I_{ON}/I_{OFF} Sensitivity for SiNW FET and DM-CNFET at V_{ds} = 1.0 V

5.4.2 TEMPERATURE VARIATION ON DM-SGCNFET FOR HIGH FREQUENCY AND WIRELESS APPLICATIONS

CNTs have long been touted as the perfect material against temperature variations. In order to validate and understand the behaviour of the simulated device against varying and high temperature values, it is tested against temperature values ranging from 300 K to 500 K. At higher temperature values, increase in mobility [20,21] is also accompanied with increased leakage currents, thus making it important to analyse CNTFET closely at such temperatures.

The transfer characteristics of DM-SGCNFET are shown in Figure 5.11 for varying temperature values. The effect of temperature on I_{ds} is different at high and low values of gate-source voltage (V_{gs}). At low gate bias, increasing temperature values decreases the energy band gap, thus enhancing the leakage current. At high gate bias, with rising temperatures, the mobility suffers since the scattering of the carriers outweighs the decrease in the energy band gap, leading to a fall in the on-current of the proposed device. The Zero-Temperature Coefficient (ZTC) bias point of the proposed device SG-GAA-CNTFET is nearly around V_{gs} = 0.55 V, at which the effect of temperature alteration on drain current nullifies. This condition at a given bias point is due to the mutual cancelation of mobility and threshold voltage dependencies on temperature. It is already known that there is an increase in drain current as mobility increases and threshold value decreases. As the temperature rises, the mobility and threshold voltage show a decreasing trend. However, at the Zero-Temperature Coefficient bias point, both these effects cancel each other.

Figure 5.12 shows the variation of transconductance, g_m wrt V_{gs}, at constant V_{ds} = 0.8 V at different temperature values. The resultant trend is similar to that of drain current The value of g_m increases due to a rise in drain current owing to the decrease in bandgap with a temperature rise at low gate bias. Transconductance plays a crucial role in determining the gain of the device and must have high values to effectively convert gate voltage into ON current. Fluctuation in output conductance, g_d, with drain bias V_{ds} and a constant V_{gs} = 0.5 V for various temperature values is plotted in Figure 5.13. Output conductance is a critical element of the device that determines its driving capacity. At low drain voltage, output conductance decreases with a rise in temperature while exhibiting an increasing trend with rising temperature values. At higher values of drain voltage, it shows very minimal variations. The effects of temperature on total

gate capacitance C_{GG} can be seen in Figure 5.14. As temperature rises, the narrowing of energy band gap leads to an increase in the carrier concentration, further leading to an enhancement in charge, thus increasing C_{GG} [22-24].

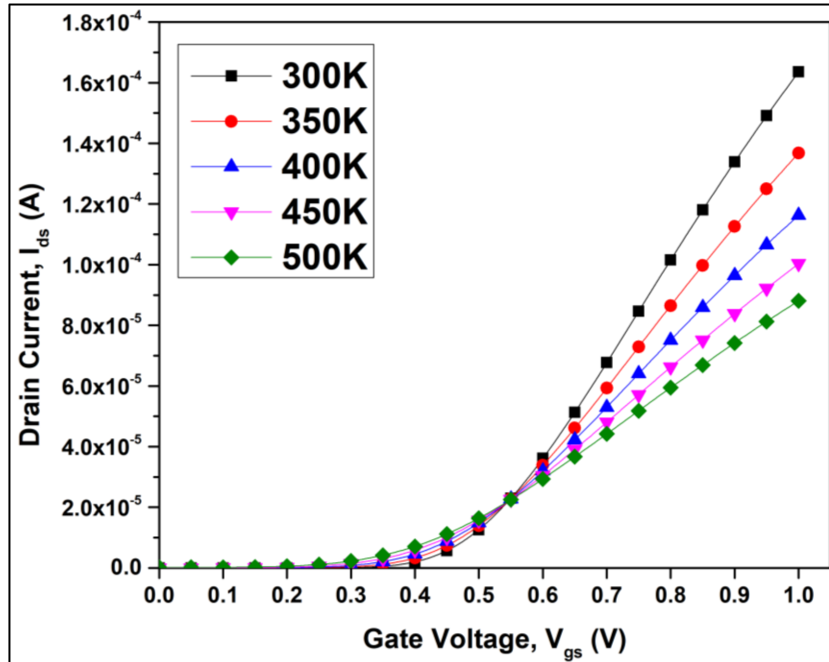


Figure 5.11: Effect of temperature variation on transfer characteristics for DM-SGCNFET at V_{ds} = 0.8 V

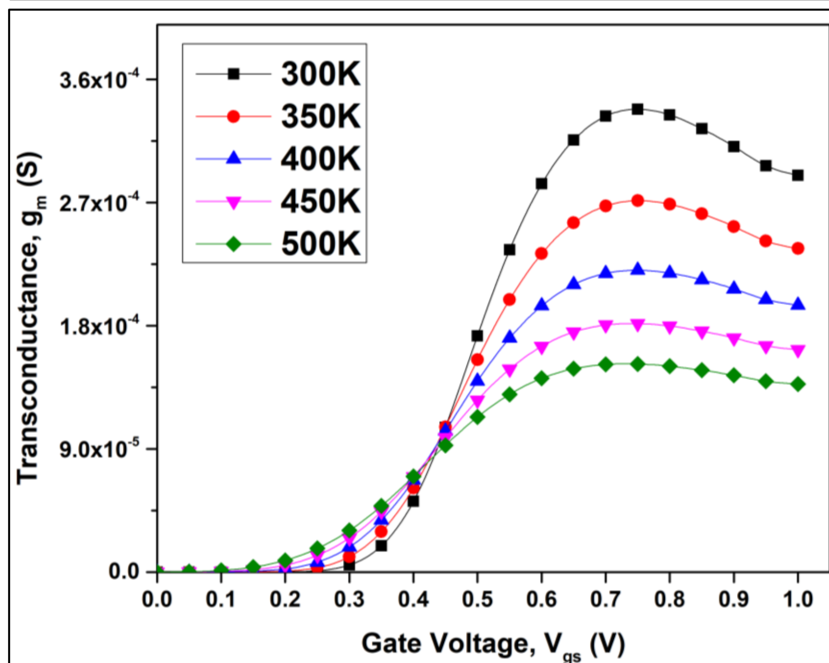


Figure 5.12: Effect of temperature variation on transconductance for DM-SGCNFET at V_{ds} = 0.8 V

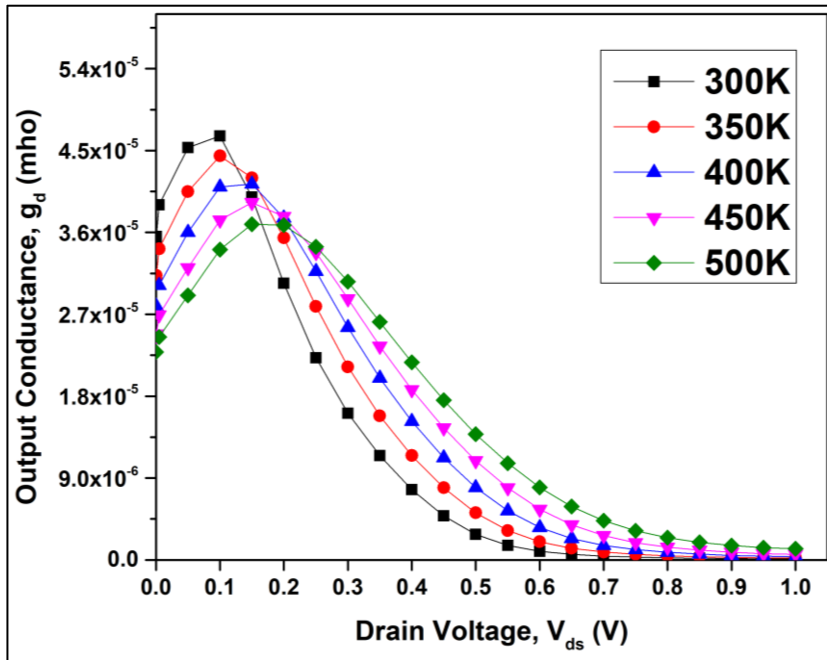


Figure 5.13: Effect of temperature variation on Output Conductance, g_d for the simulated device. (at V_{gs} = 0.5 V)

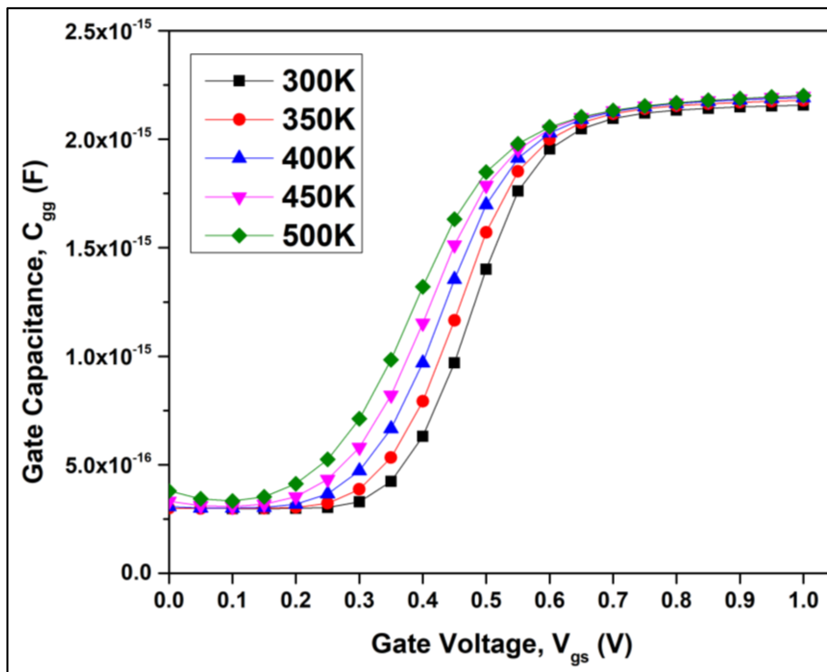
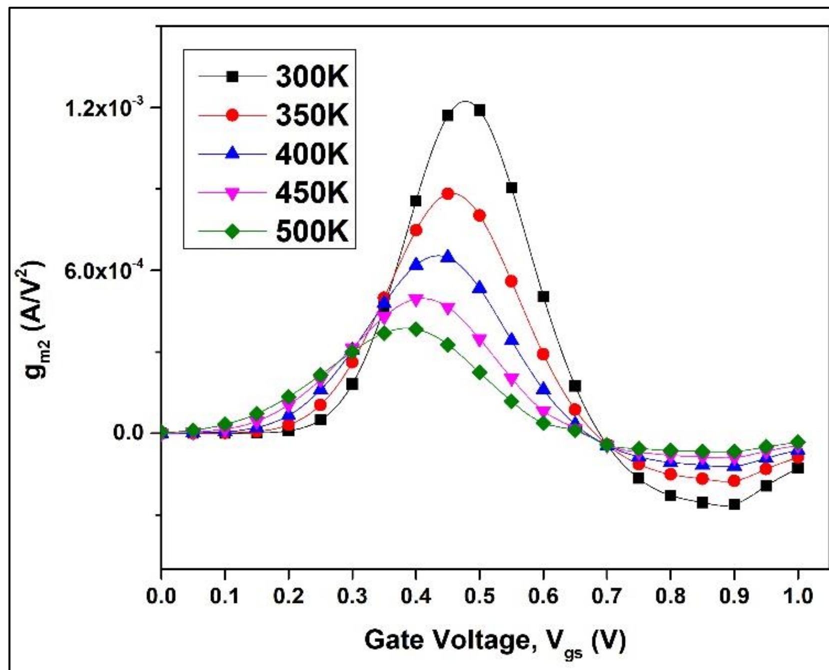


Figure 5.14: Effect of temperature variation on the Gate Capacitance C_{GG} of DM-SGCNFET

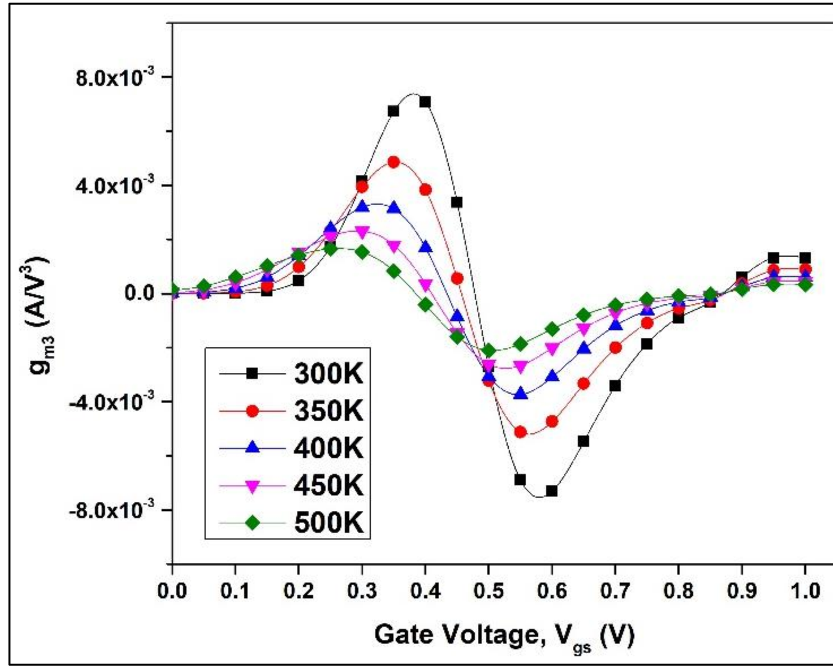
The results of the study are able to establish the robustness of DM-SGCNFET against temperature variations. The device shows complete stability even at higher temperature values and good performance numbers, that are in line with what is expected from CNTFETs. In order to further prove the robustness of the device, linearity analysis of the simulated device is conducted.

The impact of changing temperature on the values of g_{m2} and g_{m3}, respectively, is shown in Figure 5.15 (a) and Figure 5.15 (b).

When the temperature is increased from 300 K to 500 K, it is observed that the peak values g_{m2} and g_{m3} decrease, which emphasises the significant improvement in the linear behaviour of the device. It is interesting to note that g_{m2} and g_{m3} first reach low values in the subthreshold region before gradually showing improvement with increasing gate voltage due to increased current drive. The values of g_{m2} and g_{m3} indicate a decrease at all temperature ranges when gate voltage increases due to mobility degradation [25].



(a)



(b)

Figure 5.15: Effect of temperature variation on (a) g_{m2} and (b) g_{m3} of DM-SGCNFET

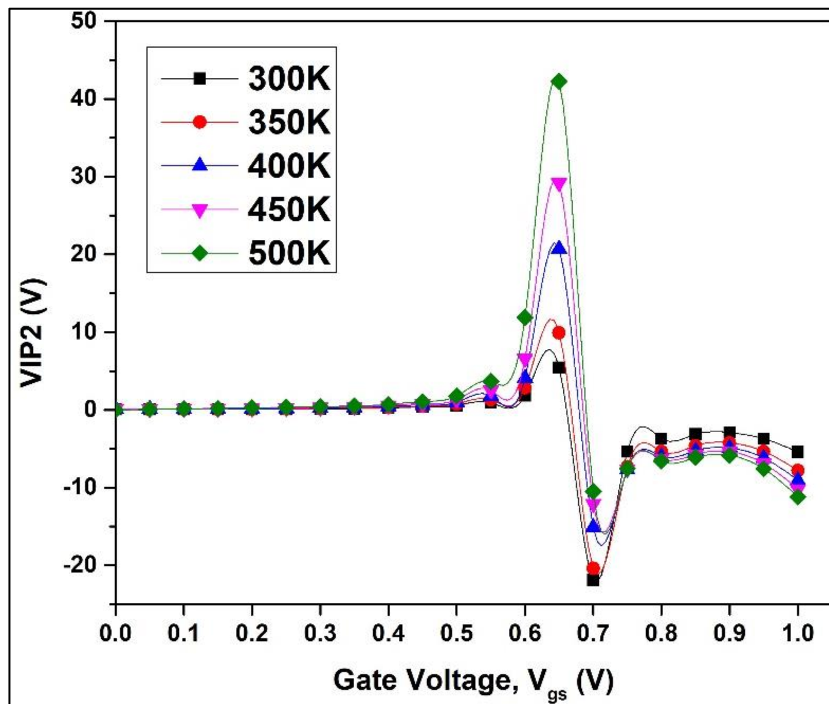
VIP2 and VIP3 can be used to express the predicted input voltage at which the first-order harmonic voltage is similar to the second-order harmonic voltage and third-order harmonic voltage, respectively. Mathematically, it can be expressed through the following equations –

$$VIP2 = 4 \times \frac{g_m}{g_{m2}}$$

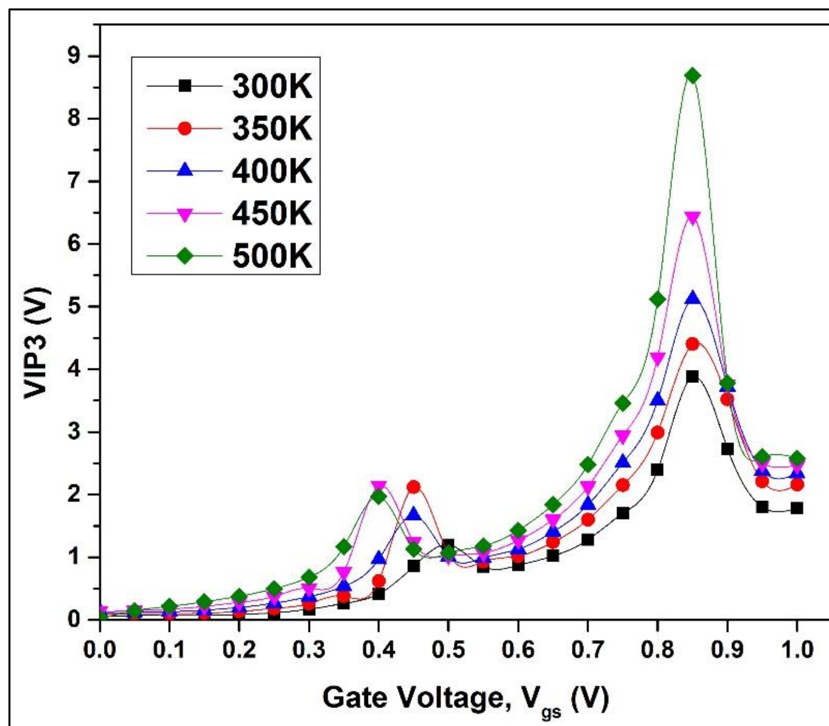
$$VIP3 = \sqrt{24 \times (\frac{g_m}{g_{m3}})}$$

$$IIP3 = \frac{2}{3} \times \frac{g_m}{g_{m3} \times R_s}$$

Higher values of VIP2 and VIP3 is desirable for distortion-free output. Figure 5.16 (a) and Figure 5.16 (b) demonstrate that both increase in value with increasing temperature values. As evident from the equations above, VIP2 and VIP3 are inversely reliant on g_{m2} and g_{m3}, respectively, and directly dependent on g_{m1} with the latter having a stronger influence on the values of the above mentioned properties.



(a)



(b)

Figure 5.16: Effect of temperature variation on (a) VIP2 and (b) VIP3 of DM-SGCNFET

IIP3, which shows how much the gate may influence carrier flow via the channel, is another crucial measure to evaluate the device's linearity. As shown in Figure 5.17, the proposed device produces improved peak values at higher temperatures.

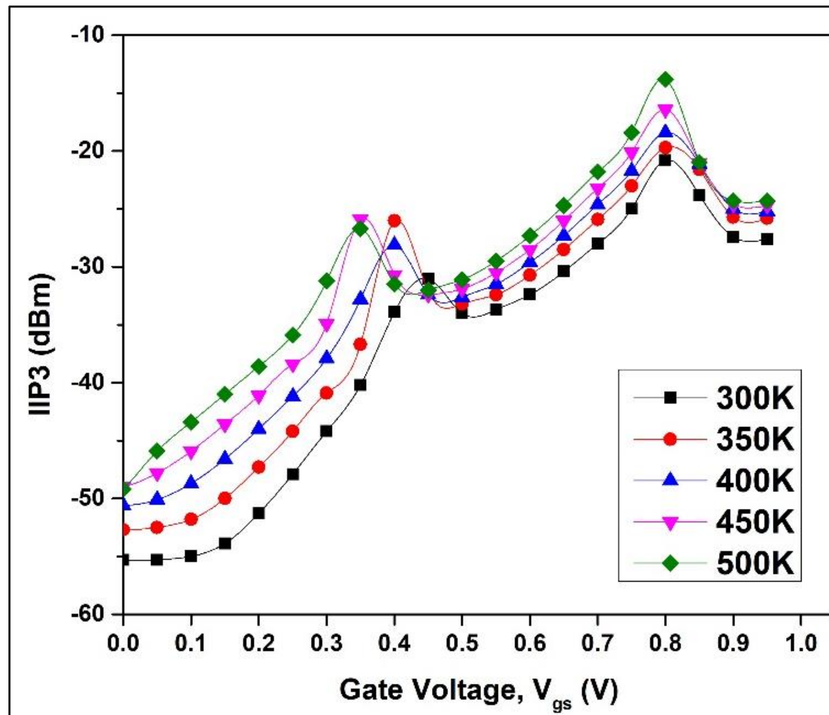


Figure 5.17: Effect of temperature variation on IIP3 of DM-SGCNFET

Linearity analysis also proves the robustness of the simulated device. The ability of the device to withhold temperature variations and showcase stable performance at high temperature values, opens the doors for unprecedented applications.

New age applications where this proven robustness can be put to use such as aerospace, satellite communications, aircraft and military applications are being explored and studied.

5.5 CONCLUSION

With the advancements in nanotechnology, materials like carbon nanotubes (CNTs) have gained significant attention. The primary objective of this manuscript is to comprehend the relevance of CNT-based devices for practical applications. Due to their superior material properties, CNTs have emerged as strong contenders to be used as channel materials for MOSFETs of next generation. The research was conducted

with the aim to expand the range of applications for CNT-based devices by exploring their sensing capabilities and temperature resilience for new age applications. Two variations of the device were simulated – one with SiO_2 as gate dioxide and another with a stacked gate oxide featuring HfO_2 alongside SiO_2. Both pass the desired tests with ease and prove their utility for the tested applications.

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CONCLUSION AND FUTURE SCOPE

6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

It has already been concluded that CNTs are superior materials, capable of bringing revolutionary advancements in the field of nanoelectronics. CNTs make it possible to construct ultra-compact and high-density integrated circuits, opening the door for the creation of sophisticated and powerful electronic devices. Hence, they are emerging as a desirable option for a diverse array of applications.

Carbon Nanotube Field-Effect Transistors, often known as CNTFETs, have been at the forefront of significant breakthroughs in electronic device performance, linearity distortion, and high-sensing applications, owing to the massive scale of research and investigation that has been poured globally for their study.

Compared to typical silicon-based transistors, CNTFETs have shown significantly better performance, with the potential for faster speed, reduced power consumption, increased scalability, and better reliability. Unlocking the full potential of CNTFETs will need ongoing efforts in research and development that are focused on overcoming the obstacles associated with synthesis, manufacturing, and integration. CNTFETs have the potential to revolutionise a variety of sectors, leading to electronic devices that are quicker, smaller, and more energy-efficient, with applications spanning from computing and communication to sensing and beyond.

CNTFETs also showcase great thermal stability, which enables them to maintain stability and high performance even under harsh environments with temperature fluctuations and high overall temperature values. This trait paves the way for potential applications in industries such as aircraft, automotive, and the military, all of which place a premium on dependability even under the most trying of circumstances.

The research was conducted to better understand the PECVD grown vertically aligned CNTs synthesized at lower temperatures and understand the influence of plasma

parameters on the performance of the proposed device. There is a wide spectrum of applications possible with CNTFETs. However, in order to deploy CNTFETs successfully, studies such as the current one become very important - it allows researchers to understand more about the material, its performance benchmarks, behaviour and decode the unknowns.

- Successful implementation of the suggested VA-DMCNFET device with vertically aligned semiconducting CNT produced in the presence of plasma sheath using the PECVD method as the channel was done. The acquired findings were compared to the previously recorded experimental data, and a satisfactory agreement was discovered. When compared to conventional NWFET, the suggested device exhibits much better metrics. With the help of this research, it can be concluded that when plasma parameters are reduced, such as by increasing CNT channel radius for a fixed CNT channel length or decreasing CNT channel length for a fixed CNT channel radius, there is a rise in the absolute values of saturated drain current, transconductance, and output conductance while channel resistance and threshold voltage are seen to decrease. Similarly, when the values of the plasma parameters show an increasing trend, properties such as gain, early voltage, and I_{ON}/I_{OFF} current ratio show a rising curve. In both sets, decreasing plasma parameters aids in raising the cutoff frequency value, improving RF performance. The findings may be utilised as a starting point by other experimentalists for their own studies in the future. Additionally, the simulation results obtained may be used to explain a wide range of other experimental outcomes, including their employment in biosensors and digital devices.

-The next part of research involves Dual-Metal Stacked-Gate CNTFET (DM-SGCNFET) device. It has been suggested that the device with the SiO_2-HfO_2 Stacked Gate-Oxide structure might be used to circumvent the downscaling issues that are often associated with conventional SiO_2 oxide. When contrasted with a similar SiO_2-based CNTFET device, the DM-SGCNFET showcased significantly improved performance metrics. These include higher values of I_{ds}, I_{ON}/I_{OFF} ratio, g_m, g_d, V_{EA}, gain, C_{GG}, as well as lower values for R_{ch}. The study also investigated the linearity of the simulated device in order to draw a relation between linearity metrics and plasma parameters. It was deduced, based on the simulations that were run for this purpose, that higher values of plasma parameters resulted in better values for VIP2, VIP3, IIP3, and 1-dB

compression point, as well as lower values for g_{m2}, g_{m3}, and IMD3. This can lead to the device being utilized for wireless applications.

-With an intention of understanding the sensing capabilities of CNTFET, the research shifted its focus towards a device known as Gate-All-Around CNTFET (GAA-CNTFET) featuring a high-k dielectric HfO_2 as gate oxide for superior performance. The use of a high-k dielectric results in enhancements to the drain current, transconductance, output conductance, early voltage, and gate capacitance. The sensing applications of the same device were also investigated through dielectric modulation by etching a nanogap cavity in the oxide layer. The findings were able to bring to conclusion that the device performance was better when a higher dielectric value was used. Strong performance, coupled with high sensitivity paint a very encouraging picture for the deployment of the simulated device for sensing applications, include biosensing.

-The last part of the research conducted as part of this study was done with the intention of understanding more avenues of CNTFETs and their applicability. Two types of devices were simulated – one tested against Silicon Nanowire FET for comparative study on sensing capabilities and another tested against temperature variations and high-temperature performance to assess robustness for wireless applications. The DM-CNFET tested against NWFET proved the better electrostatics and sensitivity for the simulated device and help draw a parallel between performance metrics and dielectric constant values. The results of the temperature variation study showcased that the device was robust, resilient to temperature changes and stable at high temperature values as well. This can potentially open the door for revolutionary applications in the very near future.

6.2 FUTURE SCOPE

The future scope of Plasma-Assisted CNTFETs is hugely promising, providing numerous opportunities for both research and development. CNTFETs have a significant opportunity to revolutionise electronics and integrated circuit design as the field of nanotechnology advances. Device optimisation is one important area of attention, where researchers can study various parameters such as chirality, channel length, diameter, and gate dielectric characteristics to enhance device performance metrics in terms of speed, power efficiency, and reliability. Also, circuit design offers a fascinating chance to take advantage of the special characteristics of CNTFETs, creating innovative topologies and optimisation methods to realise low-power logic gates, memory components, and amplifiers.

Integration with current CMOS technology is a significant requirement, since this can enable the realisation of hybrid systems by ensuring compatibility and addressing issues with device interconnects, signal levels, and noise immunity. It can also help with the creation of reliable CNTFET devices to investigate noise and reliability concerns including temperature fluctuations and random telegraph noise. High-frequency devices, mixers, detectors, and oscillators now have more options owing to the study of CNTFETs in areas other than digital applications, like analogue and radio frequency (RF) domains. By tackling issues with yield, scalability, and manufacturability as they pertain to large-scale integration, researchers might eventually pave the path for real-world implementation.

Additionally, the convergence of CNTFETs with cutting-edge technologies like memristors, spintronics, and neuromorphic computing offers promising opportunities for breakthroughs in artificial intelligence, neuromorphic computing, and energy-efficient computing. In conclusion, the future of CNTFETs is promising, embracing a wide range of study fields and offering chances for creativity and technological advancements in electronic systems and devices.

The future scope of CNTFET based biosensors is incredibly promising, opening a wide range of possibilities for diverse applications. These devices owing to their unique properties and capabilities have the capability to revolutionize various fields.

CNTFET biosensors have a lot of potential in the field of medicine for wearable health monitoring, personalised medication, and enhanced diagnostics. By giving real-time

data on biomarkers and enhancing patient outcomes, they can enable early illness identification and monitoring.

Environmental monitoring is another domain where CNTFET sensors can make a huge impact. They offer high sensitivity and selectivity, enabling the detection and analysis of pollutants, toxins, and contaminants in real-time. CNTFET sensors could also be utilized for monitoring air and water quality, ensuring the safety of food and agricultural products, and safeguarding the environment from harmful substances.

In security applications, CNTFET sensors could be employed for the rapid identification of hazardous substances or the detection of explosives and chemical agents. These developments will significantly improve the sensitivity, selectivity, stability, and integration capacities of CNTFET sensors, opening the door for their broad adoption and use across several sectors.

In summary, the future scope of CNTFET based devices is incredibly promising, encompassing healthcare, environmental monitoring, food safety, security etc. With their unique properties, these devices have the capability to bring about transformative changes, improving human health, enhancing environmental sustainability, and advancing various aspects of our daily lives.