Impact of Variation in High-k Dielectric on Analog and Switching Performance of JL-GAA-SiNWFET

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CANDIDATE'S DECLARATION

We, Kailash Chandra (2K21/MSCPHY/24) and Grace L Haokip (2K21/MSCPHY/57), students MSc(Physics), hereby declare that the project Dissertation titled "**Impact of Variation in High-k Dielectric on Analog and Switching Performance of JL-GAA-SiNWFET**" which is submitted by us to the Department of Applied Physics, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Science is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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CERTIFICATE

I, hereby certify that the project dissertation titled "**Impact of Variation in High-K Dielectric on Analog and Switching Performance of JL-GAA-SiNWFET**", submitted by Kailash Chandra (2K21/MSCPHY/24) and Grace L Haokip (2K21/MSCPHY/57) to the Department of Applied Physics, Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Science in Applied Physics, is a record of the project work carried out by the student under my supervision. This work has not been submitted partially or completely during any degree or diploma to this university or anywhere else, to the best of my knowledge.

Place: Delhi

Prof. Rishu Chaujar

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ABSTRACT

This paper examines how changing dielectric material in gate stack JL-GAA-SiNWFET device affects the analog performance. A comprehensive analysis has been carried out using the ATLAS-3D TCAD device simulator at low drain bias voltage (0.1V) and niobium as a gate electrode having a work function of 4.8eV. The study focuses on the impact of SiO_2, Al_2O_3, and HfO_2 dielectric materials on the analog parameters of the proposed device. The device analog characteristics such as I_D-V_G, transconductance (G_M), subthreshold swing, device efficiency, switching ratio, and leakage current have been examined. The results show that HfO_2 performed best with 28.6%, 15.5%, and 48 times increase in respective transconductance, device efficiency, and switching ratio, and 6.4%, and 95.8% decrement in subthreshold swing and leakage current respectively than SiO_2. This device uses interface oxide (SiO_2) and dielectric oxide which is being varied, at the gate to prevent electron tunneling. These findings could be useful in the development of high-performance analog circuits for various applications, including sensor technologies and low-power electronics.

Keywords: Gate-all-around (GAA), Silicon nanowire field-effect transistors (SiNWFET)

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

Symbol/Index	Meaning/Abbreviation
JL-GAA-SiNWFET	Junction-less Gate All Around Silicon Nanowire Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Transistor
POC	Point of Care
CNT	Carbon Nanotube
CMOS	Complementary Metal Oxide Semiconductor
EOT	Equivalent Oxide Thickness
ICs	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors
QLC	Quad Level Cell
FTIR	Fourier Transform Infrared Analysis
SiO(N)	Silicon Dioxide or Silicon Oxynitride
CNTFETs	Carbon Nanotube Field-Effect Transistors
C_g	Capacitance
DRAM	Dynamic Random Access Memory
SCEs	Short Channel Effects
EDA	Electronic Design Automation
SRH	Shockley-Read-Hall
V_D	Drain Voltage
BJT	Bipolar Junction Transistor

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

High dielectric constant gate oxides play a crucial role in metal oxide semiconductor transistors (MOSFETs) as they enable effective control of the transistor's behavior by the gate electrode. The dielectric constant, also referred to as the relative permittivity, plays a crucial role in determining the charge storage capability of the oxide material and influences the gate capacitance of the transistor. By using materials with high dielectric constants, it becomes possible to achieve larger gate capacitance, allowing for improved transistor performance and reduced power consumption.

In the past few years, there has been a growing need for high-performance transistors that consume less power. As a result, researchers have been actively exploring alternative gate oxide materials with higher dielectric constants compared to conventional silicon dioxide (SiO2). These high-k gate dielectrics offer several advantages, including improved transistor scalability, reduced leakage current, enhanced carrier mobility, and increased device reliability. Through the substitution of silicon dioxide (SiO2) with high-k materials like hafnium oxide (HfO2) and aluminum oxide (Al2O3), MOSFETs can overcome the limitations imposed by the thickness scaling of SiO_2 and achieve further miniaturization while maintaining optimal gate control.

The research on high-k gate oxides for metal oxide Si transistors aims to comprehensively investigate and comprehend the properties, fabrication methods, and performance attributes of various high-k materials. Through extensive exploration, scientists aim to gain insights into the influence of high-k gate dielectrics on crucial transistor parameters, including threshold voltage, subthreshold slope, on/off current ratio, and carrier mobility. By examining these factors, researchers seek to enhance the understanding and utilization of high-k materials in transistor design and optimization. Additionally, they analyze the compatibility of these materials with the existing semiconductor fabrication processes, identifying potential challenges and solutions for integrating high-k gate oxides into practical device structures. By gaining insights into the behavior and performance of high-k gate dielectrics, researchers aim to advance the development of next-generation metal oxide semiconductor devices with improved performance metrics, enabling further progress in areas such as integrated circuits, microelectronics, and nanoelectronics.

Over the last ten years, there has been an increasing fascination surrounding the subject of utilizing one-dimensional (1-D) structures such as silicon nanowires (SiNW), nanosheets, and carbon nanotubes (CNT) for point-of-care (POC) biomolecule applications. One of the key advantages of these structures is their ability to achieve high sensitivity, enabling the detection and targeting of biomarkers on surfaces[1]. SiNWs have shown great promise in this field. They possess several desirable characteristics, including compatibility with compact designs, integration into microelectronics, ease of mass fabrication, and the potential for rapid detection. These attributes make SiNWs an attractive choice for POC biomolecule applications. By employing SiNWs in field-effect transistors (FETs), researchers have been able to harness their high sensitivity and leverage their 1-D structure to detect and analyze biomarkers with precision. The FETs constructed using SiNWs exhibit exceptional performance, enabling efficient detection and analysis of biomolecules on surfaces.

The utilization of a high-k dielectric, specifically HfO_2, in conjunction with SiO_2, offers significant benefits in terms of improving transistor performance while maintaining control over interface characteristics[2]. One of the main advantages of incorporating a high-k dielectric layer is its higher permittivity or dielectric constant compared to SiO_2. This high-k dielectric enables the gate oxide layer to be physically thicker while still providing the same level of effective capacitance. This reduction in leakage current is crucial for ensuring the efficient operation of transistors and minimizing power consumption. Additionally, the higher permittivity of the high-k dielectric allows for better gate control over the channel region, enabling enhanced transistor performance in terms of subthreshold swing, threshold voltage, and overall device speed. The interface properties play a crucial role in determining the overall device performance, including carrier mobility, threshold voltage stability, and reliability. The introduction of a high-k dielectric layer can help improve the interface quality, reducing interface trap densities and improving carrier mobility, which ultimately enhances the overall transistor performance. Furthermore, the integration of a high-k dielectric material like HfO_2 with SiO_2 enables better compatibility with modern semiconductor manufacturing processes. It provides a means to overcome the limitations of scaling SiO_2 gate oxides, which face challenges in maintaining desirable thickness and controlling gate leakage current as transistor dimensions continue to shrink. The high-k dielectric acts as a suitable replacement for SiO_2 in advanced CMOS technologies, allowing for continued transistor scaling while achieving improved device performance. Incorporating a high-k dielectric,

such as HfO_2, on top of SiO_2 offers several advantages in transistor design. It enables improved performance by reducing gate leakage current, enhancing gate control, and optimizing interface characteristics. The utilization of a high-k dielectric layer provides a pathway for achieving higher-performance transistors while addressing the challenges associated with scaling traditional SiO_2 gate oxides.

Enhancing transistor performance and effectively managing interface characteristics are the primary advantages of incorporating a high-k dielectric, such as HfO2, in conjunction with SiO2. Hafnium dioxide (HfO_2) has emerged as a highly suitable candidate for the gate stack material in the CMOS industry. It offers several advantages that make it a preferred choice for integration with (SiNWs) [1].

HfO2 offers significant advantages in terms of its compatibility with the CMOS fabrication process, making it an attractive choice. It can be efficiently integrated into wafer production, making it a time-efficient option for manufacturing. Additionally, the use of HfO_2 in combination with SiNWs does not incur significant additional costs, making it an economically viable solution. The properties of HfO_2, such as its high dielectric constant, make it particularly well-suited for gate stack applications. Its high-k value allows for a thinner gate oxide layer, which in turn enables higher electric fields and improved transistor performance. This leads to enhanced control over the gate electrode and improved device characteristics. Moreover, the integration of HfO_2 with SiNWs brings additional benefits to the overall system. The combination takes advantage of the unique properties of SiNWs, such as their 1-D structure and high sensitivity, while leveraging the favorable characteristics of HfO_2 as the gate stack material. This synergistic integration enhances the performance and functionality of the SiNW-based devices.

When compared to other gate insulator materials, hafnium oxide (HfO2) is a good choice because of its superior interface qualities, high recrystallization temperature, and great thermal stability [3]. Hafnium oxide (HfO_2) as a gate insulator material offers several advantages over other alternatives, making it a favorable choice in advanced semiconductor devices. One key advantage is its excellent thermal stability, which refers to its ability to withstand high temperatures during device fabrication processes without undergoing significant structural or chemical changes. This thermal stability is crucial for maintaining the integrity and functionality of the gate insulator layer during various manufacturing steps. Additionally, HfO_2 exhibits a high recrystallization

temperature, meaning it can resist crystal structure degradation or phase transformations at elevated temperatures. This property ensures the stability and reliability of the gate insulator material even under harsh operating conditions, preventing performance degradation and enhancing the overall lifespan of the device. Another significant advantage of HfO_2 is its superior interface qualities compared to other gate insulator materials. The interface between the gate insulator and the semiconductor channel region plays a critical role in determining the device's performance. HfO_2 demonstrates good interface quality, which refers to the interaction and compatibility between the gate insulator and the channel material. A high-quality interface reduces interface trap densities and enhances carrier mobility, leading to improved transistor performance in terms of speed, efficiency, and reliability. Furthermore, HfO_2 offers a wide bandgap and high dielectric strength, making it highly suitable for achieving effective dielectric isolation in semiconductor devices. Hafnium-based oxides, known for their wide bandgap, high dielectric strength, and excellent thermal stability, have emerged as favorable options for improved dielectric isolation [3]. The wide bandgap ensures that the gate insulator material has a large energy gap between the valence and conduction bands, resulting in reduced leakage currents and enhanced electrical insulation properties. The high dielectric strength allows HfO_2 to withstand high electric fields without breakdown, ensuring the reliability and longevity of the device. These properties make it a preferred choice in semiconductor technology, enabling the development of high-performance devices with improved reliability and scalability.

The characteristics of the insulator layers that act as a barrier between the semiconductor channel and the metal gate contacts play a crucial role in maintaining good electrostatics within a transistor. The equivalent oxide thickness (EOT), which represents the effective thickness of these insulator layers, is an important parameter to consider.

The continuous drive for low power consumption in integrated circuits (ICs) has led to significant scaling of transistors during the past few decades [5][6]. This scaling refers to the continuous reduction in the size of transistors, leading to increased transistor density on a chip. By scaling down the transistor size, the power consumption of the circuits can be reduced while maintaining or improving their performance.

The scaling of transistors involves reducing their dimensions, such as gate length and channel length, which results in several advantages. Firstly, smaller transistors allow for faster switching

speeds, enabling higher data processing rates in electronic devices. Secondly, the reduced size leads to a decrease in power consumption since smaller transistors require less energy to switch on and off. Moreover, scaling allows for increased transistor density, enabling the integration of more complex circuits on a single chip.

The continuous scaling of transistors has been made possible through advancements in semiconductor manufacturing techniques and the development of new materials. These advancements have allowed for the fabrication of transistors with smaller feature sizes, improved performance, and reduced power consumption. However, as transistors continue to shrink in size, new challenges arise, such as increased leakage currents and decreased control over device characteristics. These challenges necessitate the exploration of innovative design approaches and materials to maintain or enhance transistor performance while minimizing power consumption. This scaling has been essential in achieving faster switching speeds, higher transistor density, and improved performance. However, it has also presented new challenges that require ongoing research and development efforts to address.

[4], [5]. As devices are scaled down to sizes in the range of tens of nanometers, certain undesirable effects start to emerge in the electrical characteristics of these devices [3], [6]– [14]. One consequence is the threshold voltage roll-off, whereby as a device's dimensions decrease, the threshold voltage—the minimum voltage needed to activate a transistor—becomes less well-defined. This may lead to fluctuations in device performance and make it challenging to provide precise control over the switching behavior of the transistor. Drain-induced barrier lowering (DIBL), another effect, is the lowering of the energy barrier between a transistor's source and drain regions as a result of the drain voltage being applied. DIBL can lead to leakage currents and sub-threshold conduction, affecting the overall performance and power efficiency of the device. Furthermore, as device sizes decrease, the leakage current through the transistor can increase. Leakage currents are unintended currents that flow through the device even when it is supposed to be in the off state. Increased leakage currents contribute to power dissipation and can limit the overall energy efficiency of the device. A shallower sub-threshold slope makes it more challenging to control the device accurately and can impact its performance and power consumption. In conclusion, scaling has both positive and negative consequences on electronic devices. While scaling improves power consumption, speed, functionality, cost per device, and chip density, it

also lowers the cost per device. These impacts, which can affect the electrical properties and functionality of scaled-down devices, include threshold voltage roll-off, DIBL, rising leakage current, and sub-threshold slope deterioration. It is crucial to address these issues through innovative design approaches and materials to mitigate their negative impact and further enhance the performance and efficiency of scaled devices.

According to (ITRS), as the transistor length of the gate decreases to 5 nm, the EOT of the insulator layers should be scaled down to 0.5 nm. This reduction in EOT is particularly advantageous for ultrashort nanodevices in both their OFF and ON states. By achieving such tiny EOTs, improvements in gate electrostatic control are anticipated. This improvement allows for a lower subthreshold slope (SS) in the range of 80-90 mV/decade. Additionally, the increase in gate capacitance (Cg) resulting from the reduction in EOT leads to an increase in the inverse charge densities in the channel. This, in turn, leads to higher driving currents within the transistor. The increased driving currents contribute to improved performance and functionality of the transistor. These findings, as referenced in sources [15] and [16], emphasize the importance of optimizing the characteristics of insulator layers, particularly their EOT, for achieving better electrostatic control, lower subthreshold slope, and increased driving currents in nanodevices.

Band-to-band tunneling is a phenomenon that plays a significant role in influencing the performance of carbon nanotube field-effect transistors (CNTFETs), particularly when they are operated at low drain voltages. This unique form of tunneling involves the direct transfer of charge carriers across the energy bandgap of the semiconductor material, enabling current flow even in the absence of a traditional source-drain voltage difference. In the context of CNTFETs, the occurrence of band-to-band tunneling introduces new considerations and challenges to the device characteristics that are typically observed in conventional (FET). The impact of band-to-band tunneling on CNTFETs manifests in various aspects of device performance. Firstly, it alters the overall current-voltage characteristics of the transistor, deviating from the typical behavior observed in devices operating under conventional transport mechanisms. This can result in non-ideal subthreshold slopes, increased leakage current, and modified switching behavior. Furthermore, the presence of band-to-band tunneling introduces additional complexities in terms of device modeling and circuit design, requiring specialized techniques to accurately capture and simulate the behavior of these devices. Operating CNTFETs at low drain voltages exacerbates the

influence of band-to-band tunneling on device performance. At these voltage regimes, the contribution of tunneling currents becomes more pronounced, and their effects on device operation become more apparent. As a result, conventional device characteristics, which are primarily defined by the operation under higher voltage regimes, may not hold for CNTFETs when they are subjected to low drain voltages. The understanding of the impact of band-to-band tunneling in CNTFETs is crucial for optimizing their performance and advancing their applications. Researchers and engineers in the field strive to develop novel device architectures, material engineering strategies, and circuit design techniques that can mitigate the undesirable effects of tunneling currents and enhance the overall performance of CNTFETs. By addressing these challenges, it becomes possible to harness the unique properties of carbon nanotubes and leverage their potential for future nanoelectronics devices and technologies. The band-to-band tunneling significantly impacts the performance of carbon nanotube field-effect transistors (CNTFETs) when operated at low drain voltages and challenging conventional device characteristics [17].

1.2 CMOS Technology: Developments and Challenges

The law that Gordon E. Moore developed in 1965 asserts that the number of transistors we put on an IC or silicon chip doubles roughly every two years. Moore's Law is the name given to this observation [1]. Due to their potential for high performance and precise control over device current, silicon nanowire transistors have drawn interest. In CMOS technology, scaling the gate insulator has been found to improve transistor performance along with other device metrics. This strategy is in line with Moore's Law, which states that the number of transistors on an integrated circuit (IC) device will double every 18 months while power consumption decreases. The implementation of high-k and metal materials has been recognized as a significant advancement in transistor technology, allowing increased transistor density, enhanced device performance, and improved circuit functionality without escalating production costs. However, the reduction in silicon dioxide gate dielectric thickness approaches its physical limit as feature sizes decrease below 45 nm, leading to large gate leakage currents through direct tunneling. [18].

According to the data presented in the figure, the growth rates of transistor count in various integrated circuit (IC) products have exhibited notable trends over the past 10-15 years.

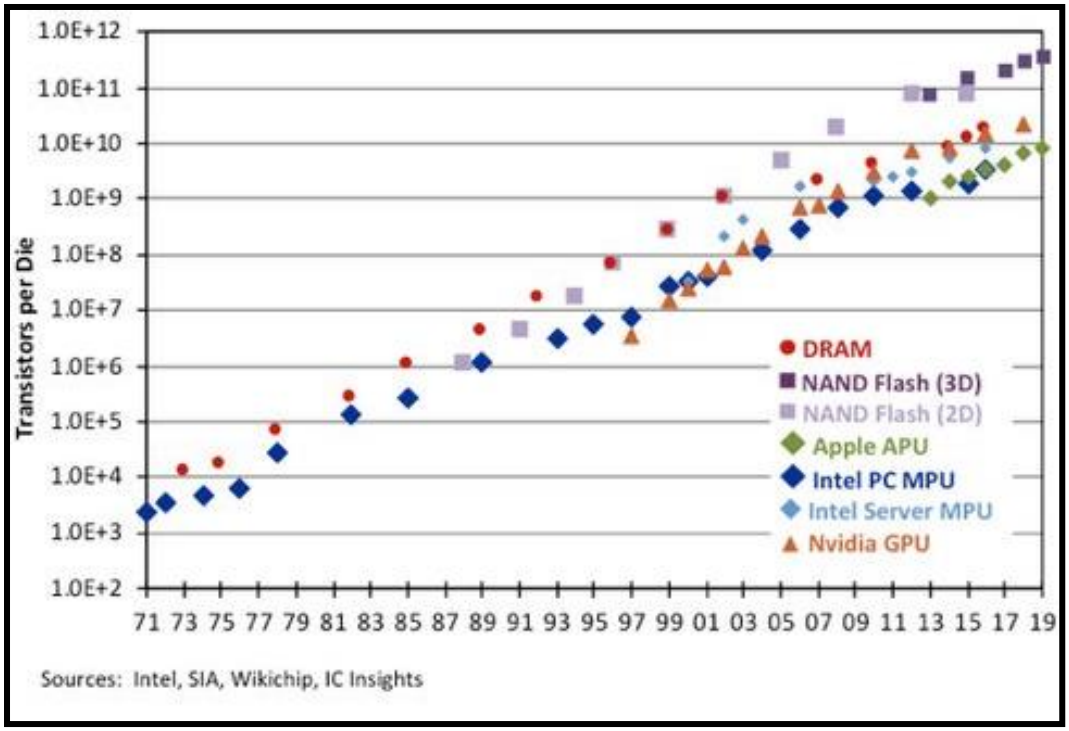


Figure 1.1 Intel's Microprocessor transistor count[19]

For instance, the transistor counts in dynamic random-access memory (DRAM) experienced a rapid increase, with an average growth rate of approximately 45% per year until the early 2000s. However, this growth rate subsequently decreased to around 20% through the emergence of the 16-gigabit (16 GB) generation in 2016 [20]. It is anticipated that the combination of QLC technology and advancements in 96-layer fabrication will enable 3D NAND to achieve a density of 1.5 TB in 2020. Furthermore, the introduction of 128-layer technology is expected to pave the way to produce 2-terabit (2Tb) chips. These observations indicate the continuous progression in transistor counts and memory densities within the semiconductor industry. Advancements in technology have allowed for significant increases in memory capacity, enabling the development of more powerful and higher-density IC products. Transistor counts in Intel's PC microprocessors increased by about 40% annually until 2010, but the rate then decreased to 50%. The mid-to late-2000s saw a brief lull in the increase of transistor counts for the company's server microprocessors (MPUs). However, it resumed an upward trajectory thereafter, with an average annual growth rate of approximately 25%. It is worth noting that Intel, the company in focus, ceased disclosing specific details regarding transistor counts starting from the year 2017[21]. Consequently, the

precise transistor count figures for Intel's server MPUs beyond that point are no longer publicly available.

In recent years, there has been significant tremendous research interest in exploring high-N gate dielectrics as potential alternatives to SiO_2 in advanced CMOS technologies. Therefore, an extensive effort has been devoted to investigating the properties and performance of these dielectric materials [22]. The MOSFET, which acts as the basic solid-state element, is a crucial component of modern microprocessors. To create MOS (CMOS), MOSFETs must be classified as either nFETs (which use electrons as the majority carriers) or pFETs (which use holes as the majority carriers). The gate oxide, which is often made of silicon dioxide or silicon oxynitride (SiO(N)), is what drives device performance and scaling. It is located at the center of the MOSFET. The thickness and quality of the gate oxide are of paramount importance in determining the overall performance characteristics of the MOSFET. Significant progress in CMOS technology has spurred the rapid and aggressive scaling of the MOSFET gate stack. This scaling approach aims to achieve higher device density and improved performance. By reducing the dimensions of the MOSFET gate stack, advancements have been made in packing more transistors onto a single chip, leading to increased device density. Additionally, scaling enables enhancements in device performance, such as faster switching speeds and reduced power consumption. The traditional poly-Si/SiO2 gate stack is reaching some practical limits. For example, the gate oxide thickness has stopped decreasing starting at the 90 nm node because the gate leakage current caused by tunneling and oxide breakdown is already quite high at this thickness of 1.2 nm [25]. Afterward, advanced gate stacks involving metal gate materials and a high-k dielectric may be required to overcome these limitations. However, the advanced gate stack's material engineering and process integration face significant difficulties. As a result, over the past 10 years, both academic and industrial research has attracted most of the focus.

The high-k dielectrics have two main benefits over traditional SiO (N) dielectrics because of their increased permittivity. First off, because the high-k dielectrics can be physically grown thicker while maintaining an equivalent oxide thickness (EOT) that is like SiO2, it offers a significant reduction in gate leakage and makes these materials acceptable for low-power applications [26, 27]. Second, high-k dielectrics may be able to achieve EOT values that are substantially lower than those achievable with traditional SiON dielectrics, which may allow for the restoration of transistor

scaling and the usage of lower gate voltages, respectively. The characteristics of the insulator layers which act as a barrier between the semiconductor channel and the metal gate contacts signify a crucial role to maintain excellent electrostatics within a transistor. The equivalent oxide thickness (EOT), which represents the effective thickness of these insulator layers, is an important parameter to consider [[3]. There was a significant global effort made at the beginning of the late 1990s to find a suitable high-k dielectric solution for the integration process into CMOS technology. Even though in 2001–2002 Hf–based high–k materials were the preferred dielectric [23]–[26]. Their launch was delayed by several issues with traditional CMOS techniques. However, thanks to recent advancements in materials and manufacturing techniques, this technology has become a reality as proven by the high-performance 45 nm semiconductor [27]– [30] including low-power 32 nm [28]and the outcomes of high-k/metal gate technology. The semiconductor industry is progressively looking into high-mobility substrates like Ge and III-V materials for CMOS technologies to further improve performance. This interest stems from recent advancements in high-k metal gate technology. By incorporating these high-mobility substrates into CMOS devices, there is a potential to achieve significant improvements in device performance, such as enhanced carrier mobility and faster transistor switching speeds. The utilization of high-k metal gate technology in conjunction with high-mobility substrates presents an exciting opportunity to push the boundaries of CMOS technology and unlock new possibilities for advanced electronic devices.

As technological nodes, gate lengths, and oxide thicknesses have shrunk, Short Channel Effects (SCEs) and gate leakage current have become significant challenges in semiconductor scaling. To address these non-ideal effects and enable continued scaling, the semiconductor industry has introduced various modifications to the traditional Si-based MOSFET structure. One prominent SCE is the Hot Carrier Effect, also known as Impact Ionization, which occurs in n-MOSFETs with shorter channel lengths. The enhanced lateral electric fields in these devices cause carrier electrons to gain higher energy, leading to the generation of electron-hole pairs and potential damage to the gate oxide material. To mitigate this effect, physical separation between the channel and substrate, along with the use of thick high-oxide layers, is employed. Gate Oxide Breakdown is the other concern that is associated with aggressive transistor scaling. As the gate oxide thickness decreases with each transistor generation, electrostatic breakdown becomes more likely, posing a threat to device reliability. The adoption of thick high-gate oxides helps address this issue while maintaining the required gate capacitance for scaling. Additionally, thicker gate oxides reduce gate

leakage current by minimizing Quantum Mechanical tunneling at the channel-oxide interface. These measures contribute to enhancing device performance, reducing non-ideal effects, and ensuring the reliability of scaled transistors. Silicon-based microelectronics devices have permeated almost every area of our daily lives during the past few decades. This has been made possible by repeatedly achieving for the individual MOSFET devices the features of quicker speed, higher density, and lower power. Therefore, for the past forty years, engineers have concentrated on "scaling," which is the reduction in each device size. The scaling behavior has adhered to the well-known Moore's rule, which states that the number of devices on an integrated circuit would double over a 1.5–2-year period. [67].

1.3 History of Transistor

Transistors are semiconductor devices with at least three terminals for connecting to electrical circuits. In the normal instance, the third terminal regulates how much current moves between the other two terminals. At Bell Laboratories in Murray Hill, New Jersey, the first transistor was successfully demonstrated on December 23, 1947. The three men that share credit for developing the transistor are William Shockley, John Bardeen, and Walter Brattain. Transistor types include (BJT) and (FET) [51].

The FET, based on the principle proposed by Julius Edgar Lilienfeld in 1925, saw its first working implementation in 1947. Shockley further advanced the technology by introducing the bipolar junction transistor in 1948, leading to its widespread use in the early 1950s and marking a significant milestone in transistor development. Then in 1951, there became a sudden big innovation in the transistor when William Shockley developed a junction transistor. Further with time more growth happened in the sector of transistor developed Planer Transistors. In 1958 Silicon Transistors became a replacement for Germanium as it was getting broken at high temperatures which worked just like a germanium junction transistor. The MOSFET was created in 1959 by Mohamed Atalla and Dawon Kahng at Bell Labs, and it revolutionized the industry. MOSFETs offered improved power efficiency, leading to their mass production and widespread adoption in various applications. These have a N or P-type semiconductor channel that passes via a ridge on top of the other kind. Even though MOSFETs are simpler to manufacture on an integrated circuit or microprocessor than junction transistors, they quickly replaced them as the

favored kind of transistor. Today, the MOSFET stands as the most extensively manufactured device in history, solidifying its pivotal role in modern electronics.

1.4 Metal-oxide-semiconductor Field Effect Transistor (MOSFET)

The fundamental MOS transistors featured a metal gate material, silicon dioxide as the insulator, and a semiconductor substrate, giving rise to the name MOS (Metal Oxide Semiconductor) transistor. On the other hand, the name "FET" refers to the process by which an electric field is applied across the gate oxide to turn the gate on and off. In this transistor configuration, two regions are biased at varying potentials, with the lower potential region serving as the source and the higher potential region acting as the drain. The electric field delivered to the gate terminal, which governs the flow of current across the channel between the source and drain regions, is the foundation of the MOSFET's operation. The electric field modifies the conductivity of the channel when a voltage is applied to the gate, allowing the transistor's behavior to be precisely controlled. The use of silicon dioxide as the gate insulator in early MOS transistors provided reliable isolation between the gate and the channel. This enabled efficient switching and low power consumption. As semiconductor technology advanced, new gate dielectric materials with greater dielectric constants known as high-k dielectrics were introduced throughout time. These materials offer improved gate control and reduced leakage current, enabling further performance enhancements in MOSFETs. The MOSFET's ability to operate at lower power levels compared to other transistor technologies, coupled with its scalability and compatibility with integrated circuit fabrication processes, has made it the most widely manufactured device in history. Overall, the combination of a metal gate, oxide insulator, and semiconductor substrate in the MOSFET architecture, along with its field-effect operation, has paved the way for the advancement and widespread adoption of modern transistor technology. A MOS transistor has four terminals and is categorized as having a drain, gate, source, and body [31]. The integration of high dielectric constant (high-k) materials as gate oxides in metal oxide silicon transistors offers potential improvements in gate capacitance, leakage current reduction, carrier mobility, and overall device performance [32]. Challenges include compatibility with fabrication processes, interface quality, and oxide layer defects. Ongoing research focuses on optimizing high-k gate oxides for reliability, thermal stability, and interface quality. Advancements in integrated circuits and microelectronics have been achieved with high-k gate oxides, driving progress in nanoelectronics and semiconductor technology.

As shown in Figure 1.2, there are four fundamental types of FET structures based on the location of the contact electrodes: coplanar top gate, coplanar bottom gate, and staggered top gate.

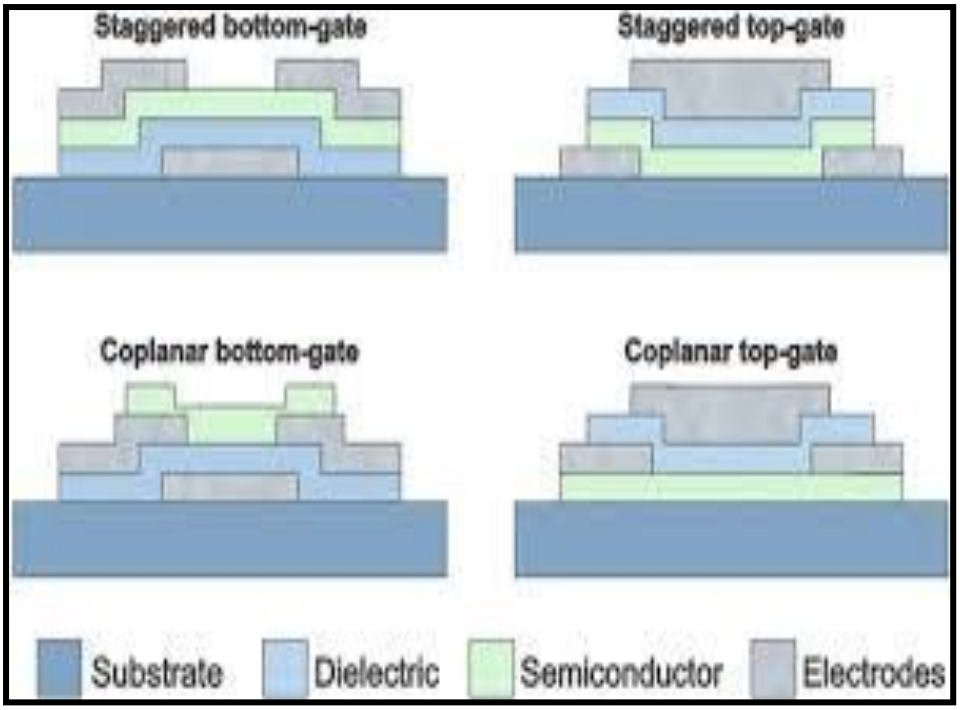


Figure 1.2 Types of Gates [33].

The semiconductor is positioned between the source and drain electrodes in all the configurations, and the dielectric layer is sandwiched between the gate electrode and the semiconducting layer. Figure 1.3 illustrates the design of a MOSFET, a key component in Very Large-Scale Integration (VLI) systems. Researchers in the field are actively focused on reducing the size of transistors to enhance their efficiency. In today's semiconductor and microprocessor industry, there is a growing trend toward employing numerous nano-scaled transistors that offer low power consumption and cost-effective designs. However, scaling down devices to the nanoscale introduces challenges such as Short Channel Effects (SCEs), tunneling effects, and threshold voltage variations, which can hinder efficiency and complicate manufacturing processes. This review article not only addresses the problems and potential solutions related to scaling but also provides a comprehensive analysis of silicon nanowire transistors and other novel nano Field-Effect Transistors (FETs) [34]. By examining these unique nano FETs, this review aims to shed light on the advancements and potential breakthroughs in the field of transistor technology.

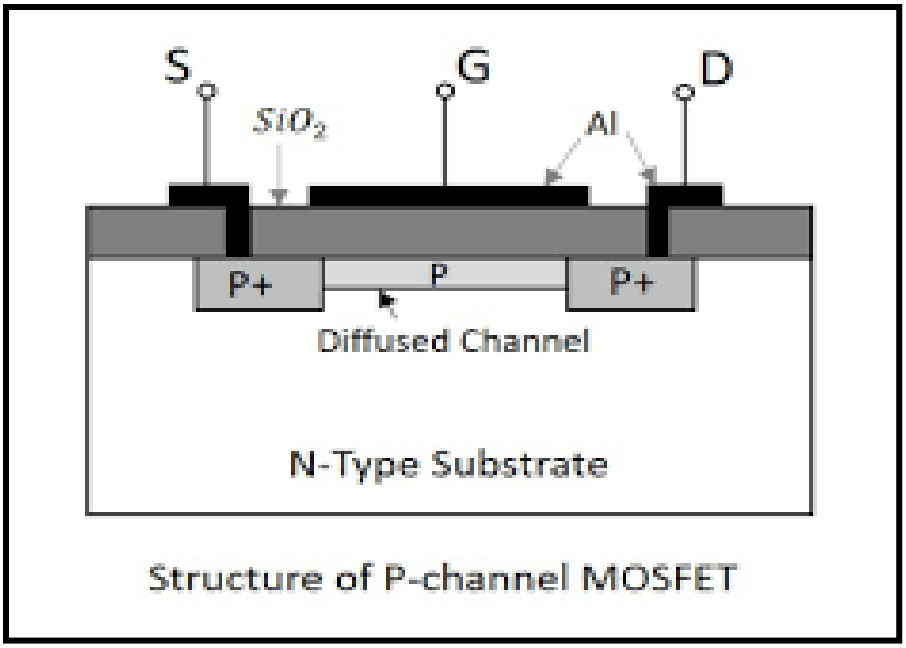


Figure 1.3 N-MOS structure [35].

1.4.1 MOSFET Operation

The MOSFET, a type of encapsulated transistor, is produced through controlled oxidation processes, typically using silicon as the semiconductor material. When a voltage is applied, it induces charges on the metal plates, like a parallel plate capacitor, and generates counter charges in the interfacial layer of the semiconductor, as expected and anticipated [36]. This phenomenon is known as the capacitive coupling effect and forms the basis of the operation of a MOSFET. By manipulating the voltage applied to the metal gate, the charges in the semiconductor layer can be modulated, allowing for precise control of the transistor's conductivity. The controlled oxidation process ensures the formation of a thin insulating layer, typically silicon dioxide, between the metal gate and the semiconductor, preventing direct electrical contact. This insulating layer acts as a barrier, enabling the transistor to switch on and off by varying the voltage on the gate terminal. The ability to regulate the direction of current through the transistor makes the MOSFET a vital component in modern electronic devices and integrated circuits, offering high performance, low power consumption, and compact size.

Controlling the voltage and current flow between the sources and drain terminals is the main goal of a MOSFET. It achieves this through the operation of a MOS capacitor, which functions as a

switch. The semiconductor can change from p-type to n-type when a positive or negative gate voltage is applied. It is situated beneath the oxide layer on the semiconductor surface, between the source and drain terminals. The holes beneath the oxide layer are pulled down towards the substrate when a positive gate voltage is supplied because of repelling forces. This causes the creation of a depletion area, which is inhabited with bound negative charges linked to the acceptor atoms and opens the channel for electrons. Additionally, electrons from the n+ source and drain regions are drawn into the channel by the positive voltage. Current can freely flow when there is a voltage placed between the source and drain, and the gate controls the movement of the electrons inside the channel. Instead of a positive voltage, a hole channel forms beneath the oxide layer if a negative voltage is supplied [31]. This alternative configuration allows for the modulation of current flow in a different manner. By manipulating the gate voltage, the MOSFET can effectively switch between different operating modes, enabling precise control over the voltage and current flow between the source and drain terminals. This characteristic makes MOSFETs an essential component in various electronic devices and systems.

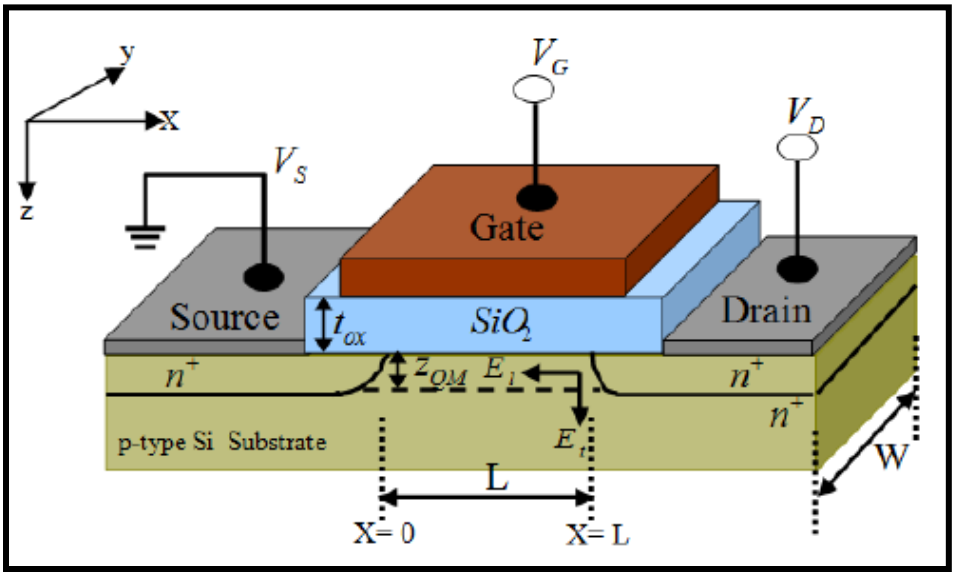


Figure 1.3 Basic structure of an n-channel MOSFET with electrons removed from the Si/SiO 2 interface due to the quantum-confinement effect [37].

The primary capability of the MOSFET is to generate and change a conducting layer comprised of minority carriers at the semiconductor–oxide interface [36]. When Vg>0 is applied, holes begin to move away from the common region because a p-type substrate is employed in n-MOS transistors [31]. The depletion layer penetrates the substrate deeper, and electrons begin to inject,

producing a pathway when the gate voltage is increased higher. For an n-type substrate, the channel created by a p-MOS transistor is made up of holes. MOSFETs are classified into two categories based on how they operate [38].

1.4.2 Enhancement mode

In enhancement mode, the absence of a gate voltage results in no conducting channel between the metal regions, rendering the MOSFET in an "off" state. To initiate the conducting channel and activate the MOSFET, a minimum gate voltage, known as the threshold voltage, must be applied. To enable the MOSFET's desired functionality in electronic circuits and devices, this gate voltage induces the development of a conducting channel, allowing current to pass between the source and drain terminals.

1.4.3 Depletion mode

The depletion-mode MOSFET operates differently from the enhancement-mode MOSFET in terms of the presence of a conducting channel. Even without a gate voltage, the depletion-mode MOSFET already possesses a conducting channel (inversion layer).

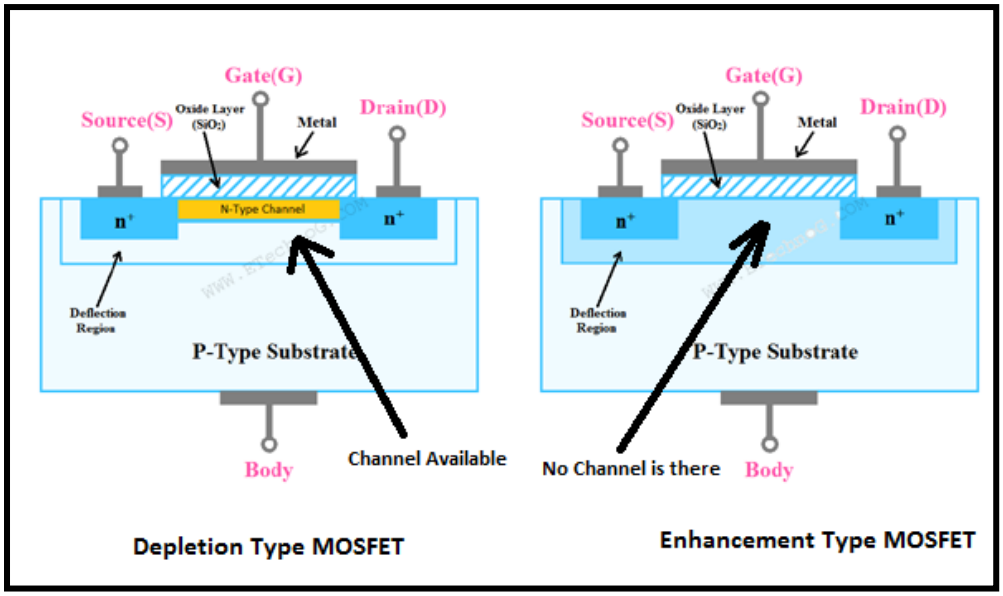


Figure 1.4 Types of MOSFET [39].

The threshold voltage plays a crucial role in controlling the device's operation, allowing it to be turned off when the applied gate voltage exceeds the threshold voltage. This behavior enables the depletion-mode MOSFET to serve as a switch or amplifier in various electronic applications.

1.5 Disadvantages and limitations of conventional MOSFET

Conventional bulk metal-on-silicon (MOS) devices are commonly used in large-scale integrated circuits. However, due to their reduced size, they are not ideal for small-channel applications. Due to the presence of both gate-drain and gate-source overlap, the device's longitudinal field is increased. Short-channel devices offer advantages such as improved processing speed, lower operating potential, and higher transistor density. However, they may also exhibit drawbacks including poor frequency response, limited linearity, and susceptibility to damage from static electricity. These considerations should be considered when designing and utilizing FET-based circuits [40][31].

1.5.1 Short channel effect

The control of electrostatics in MOSFETs varies depending on the channel length. Long-channel MOSFETs rely on the gate electrode for regulating the channel, while short-channel MOSFETs involve the active participation of the source and drain regions. The reduction in channel size in short-channel devices results in increased drain current and a lower threshold voltage, which can impact the switching behavior and energy efficiency of the MOSFET [31].

1.5.2 Velocity saturation

In a short channel device, the lateral electric field experiences significant growth, leading to the saturation of charge carrier velocity at approximately 10^7 cm/sec. This saturation effect has implications for the device current, which tends to be smaller than the drain current predicted by the mobility model [40]. Due to the increased lateral electric field in short-channel devices, the mobility of the charge carriers reaches a saturation point. Beyond this limit, the rate of growth of the carriers' velocity with the applied electric field is no longer linear. Consequently, the device current achieved in practice is lower than what would be expected based on the mobility model, which assumes a linear relationship between carrier velocity and electric field. The saturation of charge carrier velocity at around 10^7 cm/sec in short channel devices is an important consideration

in their performance analysis. It influences the actual current flow and should be considered when predicting the device behavior and optimizing circuit designs [40].

1.5.4 Surface scattering

In short-channel MOSFETs, the inversion layer that forms in the device is confined to a narrow region near the silicon-insulator interface. As the lateral electric field intensifies within the channel and the vertical electric field is applied, the charge carriers undergo acceleration towards the drain region. However, this acceleration also leads to collision events among the charge carriers, resulting in a degradation of their mobility. This phenomenon is commonly referred to as surface scattering. Surface scattering in short-channel MOSFETs has a significant impact on the device's performance. It causes a reduction in the drain current compared to what would be expected based solely on the mobility of the charge carriers. The collisions between charge carriers during their journey from the source to the drain hinder their overall mobility and affect the efficiency of the device [41]. Understanding and mitigating the effects of surface scattering is crucial in the design and optimization of short-channel MOSFETs. By addressing this phenomenon, researchers and engineers can work towards improving the performance and efficiency of these devices in practical applications.

1.5.5 Hot carrier effects

The carriers move at rapid speeds in short-channel devices because the electric field intensity in the channel areas grows. The high kinetic energy acquired by the carriers in this process can give rise to a phenomenon known as impact ionization. Impact ionization can cause degradation of the insulator layer, leading to gate leakage current. The carriers responsible for this phenomenon are referred to as hot carriers. The presence of hot carriers in short-channel devices can have several undesirable effects. One such effect is the generation of substrate current, which refers to the flow of current through the substrate material. This substrate current can impact the overall performance and reliability of the device [41]. Understanding and managing the effects of hot carriers is crucial in the design and optimization of short-channel devices. Researchers and engineers strive to develop strategies to mitigate the impact of hot carriers, such as incorporating suitable materials and structures that can handle the high-energy carriers more effectively and minimize the associated degradation and leakage currents.

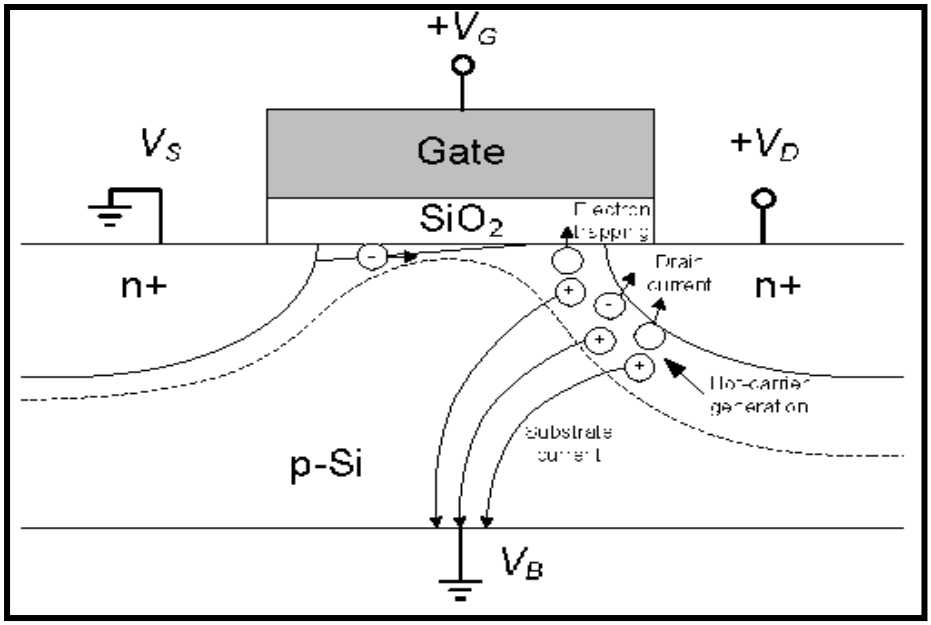


Figure 1.5 Representation of Hot Carriers Effect [42].

1.6 Gate-All-Around (GAA)

By employing many gate transistors, the adverse effects of small channels are significantly mitigated, resulting in improved performance. The nanowire itself acts as the substrate in silicon nanowire transistors [43]. Nanowires exhibit various device shapes, such as rectangular and cylindrical configurations. The utilization of Nanowires in transistor design offers several advantages. The cylindrical or gate-all-around structures enable better control over the channel region, facilitating enhanced electrostatics and reduced leakage currents. Moreover, the compact size of Nanowire transistors allows for higher transistor density on a chip, enabling the integration of more functionality and improved overall performance in electronic devices. The development and optimization of Nanowire-based transistor technologies continue to be an area of active research and innovation in the field of semiconductor devices.

1.6.1 Gate All-Around Field-Effect Transistors (GAA-FETs)

These transistors have a unique structure where the gate region completely wraps around the channel, offering distinct advantages over traditional transistor designs [44], [45]. This innovative configuration allows for improved control over the flow of current through the channel, resulting in enhanced device performance. By enclosing the channel region with the gate material, GAA-FETs provide better electrostatic control, minimizing leakage currents and improving the

transistor's ability to switch on and off. This enhanced control over the channel allows for higher device efficiency, reduced power consumption, and improved overall performance. GAA-FETs have shown promise in maintaining their performance characteristics due to the improved electrostatic control provided by the fully wrapped gate structure. This scalability is crucial in enabling the continued advancement of integrated circuits, as it allows for the realization of smaller, faster, and more power-efficient electronic devices. By investigating novel gate materials, dielectrics, and channel materials, researchers aim to further enhance the transistor's functionality, reduce power consumption, and improve reliability. This unique configuration of GAA-FETs with a fully wrapped gate structure represents a significant advancement in transistor design and offers improved electrostatic control, scalability, and performance characteristics, making GAA-FETs a promising candidate for future nanoelectronics devices. GAA-FETs offer distinct advantages in terms of mitigating short-channel resistance [44], [45]. GAA-FETs address this challenge by utilizing a fully wrapped gate structure that surrounds the channel region from all sides. This unique architecture provides superior electrostatic control over the channel, effectively minimizing short-channel effects. Compared to other gate structures like omega gate, double gate, and single gate, GAA-FETs demonstrate enhanced performance characteristics in terms of reducing short channel resistance. The comprehensive wrapping of the gate around the channel in GAA-FETs ensures improved gate control, reduced leakage currents, and enhanced switching characteristics. These advantages make GAA-FETs well-suited for future scaling technology nodes were maintaining device performance in the face of shrinking channel lengths is of utmost importance. By improving short-channel resistance and overall device performance, GAA-FETs hold great potential for enabling the realization of advanced and highly efficient electronic systems in the future. Continued research and advancements in GAA-FET technology will further solidify their position as a leading contender in the field of nanoelectronics.

Despite their promising advantages, GAA-FETs are not without drawbacks and thus two significant challenges are associated with GAA-FETs which are high leakage current and subthreshold slope, which can limit their suitability for low-power applications and steep switching requirements [44]. High leakage current in GAA-FETs compromises energy efficiency and is unsuitable for low-power applications. Achieving a low subthreshold slope is challenging in GAA-FETs, affecting switching efficiency. Alternative transistor designs are needed for low-power and fast-switching applications. Researchers are working on reducing leakage current through gate

dielectric optimization and surface defect minimization. Improving the subthreshold slope requires advancements in gate engineering. By addressing the issues of high leakage current and subthreshold slope, GAA-FETs can become more suitable for a wider range of applications, including low-power and steep-switching scenarios. Ongoing research and development efforts are focused on optimizing GAA-FET designs and exploring innovative solutions to overcome these limitations, ultimately enhancing their performance, and expanding their applicability in various electronic systems.

1.6.2 Gate-All-Around Silicon Nanowire Field-Effect Transistor (GAA-SiNWFET)

The high-k dielectric serves the purpose of isolating the gate from the channel. However, any variation in the high-k dielectric can give rise to several issues that impact the performance of the transistor. Firstly, variations in the high-k dielectric can result in reduced transconductance. This reduction occurs due to a decrease in the effective gate capacitance, which directly affects the ability of the transistor to amplify the input signal. Secondly, there is the possibility of an increased off-leakage current. The transistor may experience larger leakage currents when it should be in the off-state due to variations in the high-k dielectric. The overall power efficiency of the gadget may suffer as a result of this leakage current. The reduced switching speed of the transistor is another effect of high-k dielectric variation. The switching rate relates to how quickly the transistor can transition between its on and off states. If the high-k dielectric is not uniform, it can impede the efficient and rapid switching of the transistor. Furthermore, variation in the high-k dielectric can contribute to increased crosstalk between neighboring transistors. Crosstalk refers to the unwanted coupling or interference between adjacent transistors, which can negatively impact their performance and introduce noise into the system.

JL-GAA-SiNWFETs hold significant promise for future high-performance and low-power electronics. When compared to other transistor designs such as GAA-MOSFETs and bulk MOSFETs, JL-GAA-SiNWFETs exhibit improved sensitivity [46]. They offer advantages like a larger effective channel width, reduced short-channel effects, and enhanced scalability. However, it's important to note that the choice of dielectric material greatly influences the performance of JL-GAA-SiNWFETs. High-k dielectrics have emerged as a potential solution to enhance the performance of JL-GAA-SiNWFETs. These high-k dielectrics offer distinct advantages over traditional SiO_2 (silicon dioxide) dielectrics, thereby addressing certain limitations. One key

advantage of high-k dielectrics is their higher dielectric constant compared to SiO_2. The dielectric constant, also known as the relative permittivity, evaluates a material's capacity to store electrical energy. With an increased dielectric constant, high-k dielectrics enable a thinner gate oxide layer to be used in the transistor structure. This reduction in oxide thickness allows for better electrostatic control of the device, leading to improved performance. Additionally, the higher dielectric constant of high-k materials facilitates a higher electric field across the gate oxide. This increased electric field enhances the transistor's ability to control the flow of current through the channel, resulting in enhanced device characteristics, such as improved carrier mobility and subthreshold behavior. Another significant advantage of high-k dielectrics is their lower leakage current. By employing high-k dielectrics, the leakage current can be minimized due to their lower leakage properties, which contribute to higher power efficiency and reduced energy consumption. The utilization of high-k dielectrics in JL-GAA-SiNWFETs presents an opportunity to overcome the limitations associated with SiO_2 dielectrics. The superior properties of high-k dielectrics, including their higher dielectric constant, thinner gate oxide, higher electric field, and lower leakage current, collectively contribute to enhanced transistor performance, improved power efficiency, and better overall device characteristics. These findings from various studies and research papers [45], [14] underscore the potential of high-k dielectrics as a viable approach to optimize the performance of JL-GAA-SiNWFETs and pave the way for advancements in high-performance nanoelectronics devices.

1.7 The Rationale for Selecting Silicon Nanowire

Silicon CMOS is perhaps the nanoelectronics industry’s favored technology for several decades. Because of their exceptionally high qualities, MOSFETs have evolved into one of the most important phenomenon components of VLSI. A MOSFET's channel length is lowered during scaling down the device; deviations from long channel behavior have been predicted. And because of their greatly improved electrical and optical features along with the presence of the semiconductor business, silicon nanowire transistors have gotten a lot of interest as a potential replacement for traditional MOSFETs. It was reported that the carrier mobility of small-diameter SiNWs is high and the ability to fabricate high-performance field-effect transistors FETs requires high carrier mobility. Since silicon nanowires SiNWs consist of a ratio of high surface-to-vol.,

comparatively, a little electrical field applied to the gate can readily control mass carriers and it has also been found that these SiNWs-related nano FETs are extremely sensitive [47].

1.8 Objective of the Research Work

In our research study, we aimed to investigate how variations in high-k dielectric materials impact the analog and switching performance of JL-GAA-SiNWFETs (Gate-All-Around Silicon Nanowire Field-Effect Transistors). To conduct our analysis, we utilized the ATLAS SILVACO-3D simulator and performed simulations at a low bias drain voltage of 0.1V. For the gate electrode, we used Niobium with a work function of 4.8 eV.

Our study focused on evaluating several key parameters to assess the performance of JL-GAA-SiNWFETs. These parameters included Id-Vg (drain current versus gate voltage), transconductance (measurement of how the output current changes in response to a change in the input voltage), subthreshold swing, device efficiency, switching ratio, and leakage current. Through our simulations and analysis, we discovered that the HfO_2 (hafnium oxide) dielectric material outperformed SiO_2 (silicon dioxide) and Al_2O_3 (aluminum oxide) in all evaluated parameters. This indicates that HfO_2 is the most suitable high-k dielectric material for enhancing the performance of JL-GAA-SiNWFETs.

Furthermore, our study explored an alternative approach to achieve a dielectric layer on a smaller width by utilizing a stack formation. We applied SiO_2 as the first layer in the stack, as it demonstrated better compatibility with Si nanowires. The second dielectric layer was varied and studied using SiO_2, Al_2O_3, and HfO_2. This combination resulted in effective oxide thickness (EOT) values of 1nm, 0.7nm, and 0.6nm, respectively.

Overall, our research highlights the significance of high-k dielectric variations in influencing the analog and switching performance of JL-GAA-SiNWFETs. The findings indicate that HfO_2 exhibits superior characteristics compared to SiO_2 and Al_2O_3, showcasing its potential for optimizing device performance. The utilization of dielectric stack formations also provides a viable approach for achieving desired oxide thickness on smaller device dimensions.

CHAPTER 2

DEVICE STRUCTURE & SIMULATION IN ATLAS SILVACO-3D

2.1 ATLAS SILVACO-3D

ATLAS SILVACO-3D is a powerful software tool used for the three-dimensional (3D) simulation of semiconductor devices. Silvaco Inc., a well-known electronic design automation (EDA) software supplier, created it. The software is specifically designed for advanced process technologies and enables engineers and researchers to model, analyze, and optimize the performance of semiconductor devices in a 3D environment. The production of semiconductor devices, including oxidation, diffusion, ion implantation, removal, coating, and lithography, can be simulated using this software. This is a sizable collection of extremely sophisticated tools, including ATLAS, that support the design and creation of all varieties of semiconductor and VLSI devices. This module can simulate many semiconductor devices in 2D and 3D, including MOSFETs, HEMTs, and solar cells [48].

ATLAS SILVACO-3D provides a comprehensive suite of simulation capabilities that accurately simulate the behavior of various semiconductor devices, including transistors, diodes, solar cells, sensors, and more. It employs advanced numerical algorithms and physics-based models to capture the complex interactions between electrical, thermal, and optical phenomena within the device structures. The software allows users to define the geometric layout of the device, specify material properties, and define the operational conditions and boundary conditions. It then solves the governing equations using numerical techniques to simulate the electrical behavior of the device under different operating conditions. This includes modeling carrier transport, charge generation and recombination, electrostatics, quantum effects, and other relevant physical phenomena. ATLAS SILVACO-3D offers a wide range of analysis capabilities, such as current-voltage (IV) characteristics, capacitance-voltage (CV) characteristics, charge transport analysis, breakdown voltage analysis, thermal analysis, and more. It provides detailed insights into device performance, allowing engineers to optimize design parameters and assess the impact of process variations and design modifications. The software also offers a user-friendly graphical interface that facilitates device setup, visualization of simulation results, and post-processing of data. It supports efficient parallel computing to expedite simulation times and provides various data analysis and visualization tools to aid in result interpretation.

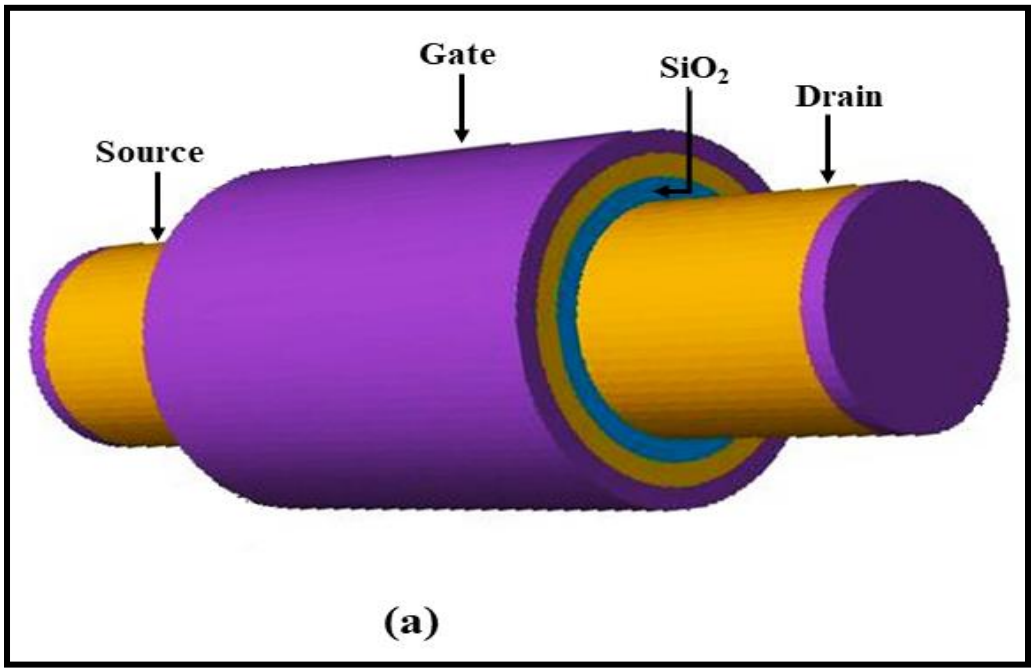
ATLAS SILVACO-3D is widely used in the semiconductor industry and academic research for the design and optimization of advanced semiconductor devices. Its accurate 3D simulation capabilities contribute to the development of more efficient, reliable, and high-performance electronic devices across various application domains.

2.2 Device Structure

Figure 2.1 depicts the proposed structure of our device, showcasing its key dimensions and layers. The entire device measures 42nm in length, with a channel length of 20nm. At the interface, there is an oxide layer composed of SiO_2. The device features a metal gate, which has a thickness denoted as T1. Additionally, there are varying dielectric layers with a thickness denoted as T2, and an interfacial oxide layer (SiO_2) with a thickness denoted as T3. The channel diameter, represented as 2R, is also the thickness of the silicon layer.

In all simulations, the gate length remains consistent at 20nm. Similarly, the varying oxide layer and interfacial oxide layer maintain a length of 20nm. The source and drain regions measure 10nm each, while the electrodes at both ends have a length of 1nm. For a comprehensive overview, please refer to Table 1, which lists all these parameters for reference and further analysis.

By providing these detailed dimensions and layer thicknesses, the structure of the device is clearly outlined, enabling researchers and engineers to understand the physical characteristics and design considerations of the proposed device configuration.



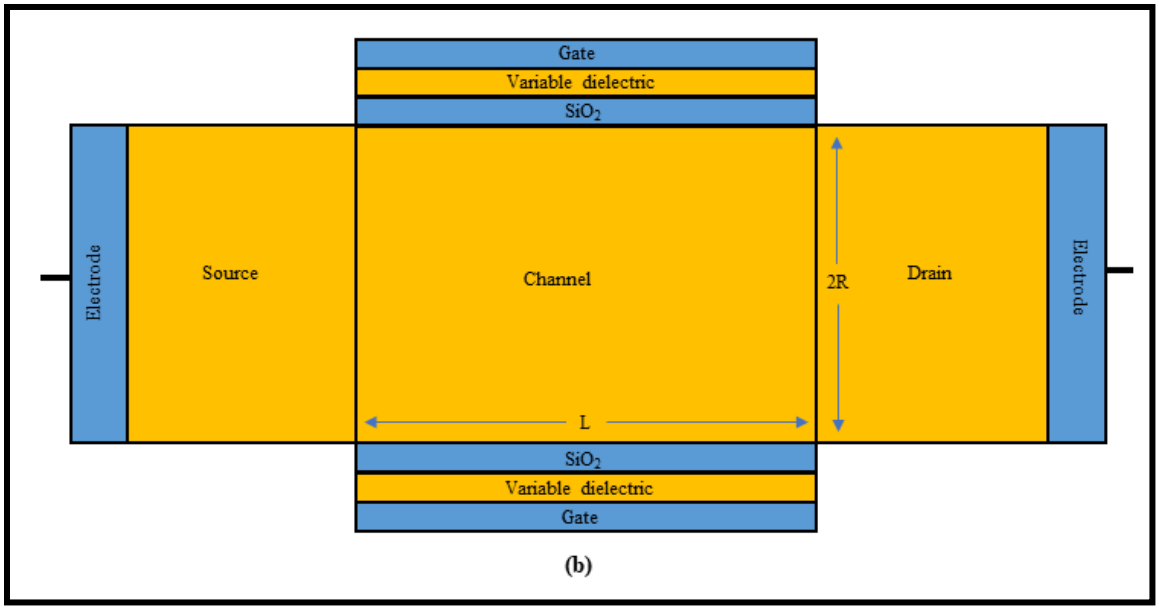


Figure 2.1 - Junctionless gate all around silicon nanowire FET (a) JL-GAA-SiNWFET (b) cross-sectional view.

Table 2.1: Technology parameters

Device Parameters	JL-GAA-SiNWFET
Channel length (nm)	20.00
Diameter of silicon film (nm)	20.00
The thickness of varied oxide and interface oxide respectively, (nm)	0.5 & 0.5
Length of Source and Drain, (nm)	10.00
Length/Thickness of electrode, (nm)	1.00
Thickness of varied oxide and SiO_2 respectively, (nm)	0.5 & 0.5
Dielectric of SiO_2, Al_2O_3, HfO_2 respectively	3.9, 9, 25
Gate work-function of Niobium, (eV)	4.8
Doping of Channel, Source, and Drain, (N-type)	10^{19} cm^{-3}

A high and uniform doping concentration of $1x10^{19}$ cm^{-3} is implemented throughout the entire region spanning from the source to the channel and extending towards the drain. This intentional doping ensures the attainment of the desired threshold voltage for the device. It is significant to remember that the device is N-type doped, indicating the predominant presence of electrons as the majority carriers. By uniformly doping the device with N-type dopants, the necessary charge

carrier concentration is established, enabling the device to function effectively.

2.3 Methodology

. The Shockley-Read-Hall (SRH) recombination model is also activated to account for the recombination of majority and minority carriers [49]. The ripple currents that the posterior charge carrier causes are also considered in the drift-diffusion model. Fermi-Dirac statistics were developed as a result of extensive source and drain doping. Concentration, voltage, and temperature (CVT) and Boltzmann transport statistics [50] Model of Lombardi mobility [51] considered parallel and perpendicular field mobility [50]. Here, the gate is made of niobium, a rare, soft, gray dielectric transition metal. Due to its superconductivity and higher critical temperature than helium (~4.2 K), it is one of the best materials for the gate electrode in NWFETs.**Error! Bookmark not defined.** Figure 1 shows (a) a 3D structure and (b) a 2D cross-sectional view of the JL-GAA-SiNWFET N-type niobium metal gate. The JL-GAA-SiNWFET structure consisting of a 40nm long N-type doped channel and a doping concentration of $1x10^{19}cm^{-3}$ was applied from the source to drain through the channel uniformly. The models and settings that will be used throughout the simulation are listed in the runtime output via the PRINT parameter. You can test models and material settings in this way. The GUMMEL approach will address each unknown in turn while maintaining the status quo for the other variables, and iterate through the process until a stable solution is reached. The system of sums of unknowns is solved using NEWTON's approach combined [52]. Use the syntax of the following numerical algorithms in isothermal drift-diffusion simulations to get around the issue of subpar starting estimates. METHOD OF NEWTON GUMMEL To get a better initial estimate for NEWTON's solution diagram, this method first executes a GUMMEL iteration. Despite being more effective, this approach takes longer to complete than utilizing only the NEWTON diagram.

CHAPTER 3

RESULT AND DISCUSSION

For Analog analysis the desired parameters like I_D-V_G, transconductance, subthreshold swing, device efficiency, switching ratio, and leakage current are evaluated with SILVACO-3D. In this work, JL-GAA-SiNWFET is a proposed device that shows a better result in the HfO_2 material gate substrate with dielectric constant 25.

Table 3.1. Simulation results concerning all-dielectric

Dielectric Materials	Dielectric Constant (K)	Transconductance (G_M)	Subthreshold Swing (SS)	Device Efficiency (DE)	Switching Ratio (I_{ON} /I_{OFF})	Leakage Current (I_{OFF})
SiO_2	3.9	9.63E-06	6.72E-02	9.09E+01	7.56E+05	5.92E-12
Al_2O_3	9	1.13E-05	6.40E-02	1.01E+02	9.84E+06	4.73E-13
HfO_2	2.5	1.24E-05	6.29E-02	1.05E+02	3.64E+07	1.31E-13

3.1 Comparative Analysis of I_D-V_G in JL-GAA-SiNWFET for Improved Performance

This study introduces a novel device called the JL-GAA-SiNWFET, which demonstrates superior performance when utilizing an HfO_2 material gate substrate with a dielectric constant of 25. Figure 3.1 illustrates the relationship between drain current and gate voltage at a fixed drain voltage (V_D) of 0.01V for the junctionless gate all around silicon nanowire FET. The experiment investigates the impact of three different gate materials on the device's characteristics, specifically comparing the results obtained with HfO_2, SiO_2, and Al_2O_3.

The analysis of the obtained curves reveals that the drain current peak is significantly higher when using HfO_2 as the gate material compared to SiO_2 and Al_2O_3. This indicates that HfO_2 offers improved conductivity and facilitates better current flow within the device. Additionally, the off

current, which represents the leakage current when the device is in the off state, is lower for HfO_2 compared to the other gate materials. This implies that HfO_2 exhibits better insulation properties and effectively suppresses the unwanted flow of current when the device is intended to be off.

Moreover, the permittivity of the gate material plays a crucial role in device performance. As the permittivity rises, the ON current is shown to rise as well. This indicates that HfO_2, with its higher permittivity, allows for more efficient modulation of the channel and facilitates enhanced current conduction when the appliance is turned on.

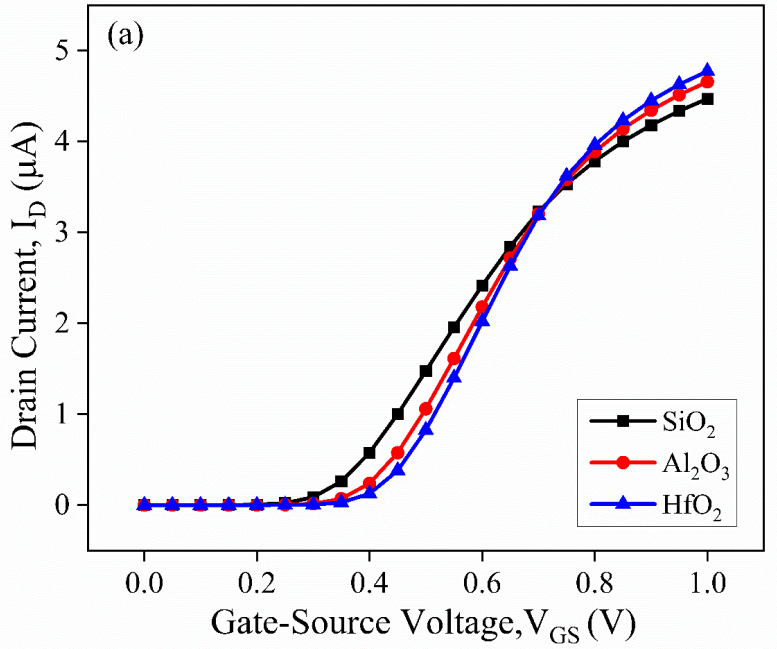


Figure. 3.1 - Transfer characteristics of drain current vs gate voltage at V_D = 0.01 V for JL-GAA-SiNWFET

Overall, the experimental findings highlight the favorable qualities of HfO_2 as a gate material in the JL GAA-SiNWFET. It exhibits higher drain current, lower off current, and improved permittivity compared to SiO_2 and Al_2O_3, making it a promising choice for enhancing the performance of nanowire FETs.

3.2 Comparative Analysis of Transconductance in JL-GAA-SiNWFET with Different Dielectric Materials

In this study, we investigate the transconductance of JL-GAA-SiNWFET with different gate materials. The aim is to compare the performance of HfO_2, SiO_2, and Al_2O_3 in terms of their impact on key analog parameters.

One of the important parameters examined is transconductance, which is characterized by the relationship between the change in drain current and the accompanying gate voltage. This parameter reflects the ability of the device to amplify and control the signal.

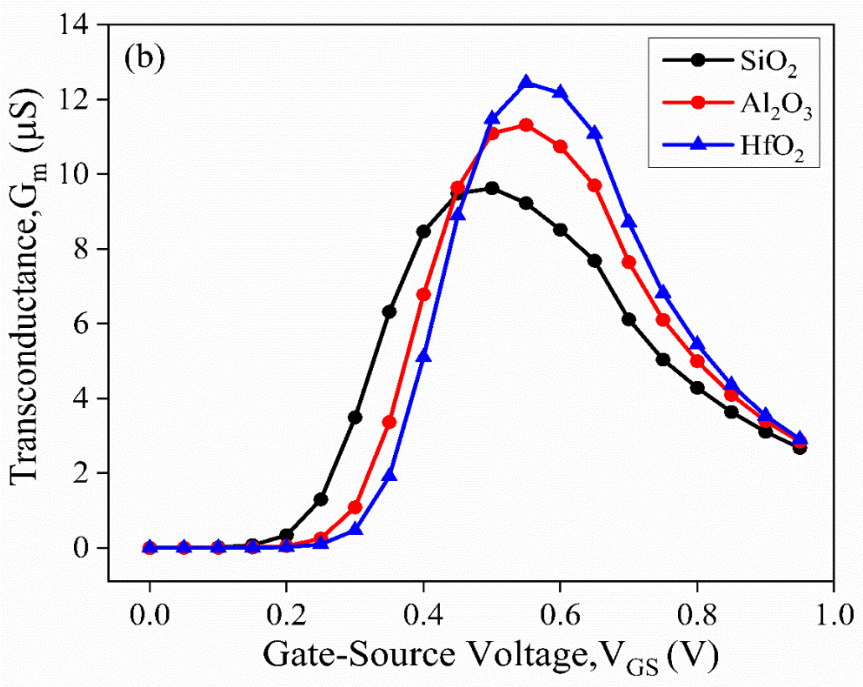


Figure 3.2 - The transconductance vs gate voltage graph for JL-GAA-SiNWFET at V_D=0.1V

Figure 3.2 illustrates the transconductance characteristics of the different gate materials. It is observed that the transconductance (Gm) of HfO_2 is higher compared to SiO_2 and Al_2O_3. This indicates enhanced electron mobility, improved gate controllability, and higher average carrier velocity in devices utilizing HfO_2 as the gate material. Moreover, the higher transconductance suggests a reduced decay of the short channel effect, leading to improved device performance. Furthermore, the transconductance factor (TGF) provides insights into the efficiency and linearity of the device's operation. The TGF is a measure of how effectively the device converts the gate

voltage into drain current. A higher TGF indicates better performance in terms of amplification and signal fidelity.

Overall, the study highlights the impact of different gate materials, such as HfO_2, SiO_2, and Al_2O_3, on the transconductance and transconductance factor in JL GAA-SiNWFET. The results indicate that HfO_2 offers superior performance, exhibiting higher transconductance and improved device characteristics related to electron mobility, gate controllability, carrier velocity, and short-channel effect.

3.3 Comparative Analysis of Subthreshold Swing in JL-GAA-SiNWFET with Different Dielectric Materials

In modern semiconductor devices, achieving better performance and efficiency is of paramount importance. One key parameter that significantly affects device performance is the subthreshold swing (SS). The subthreshold swing quantifies the shift in gate voltage necessary to cause a tenfold shift in drain current when the device is operating in the subthreshold region. In this study, we investigate the subthreshold swing characteristics of JL-GAA-SiNWFET using different gate materials, specifically HfO_2, SiO_2, and Al_2O_3. The objective is to compare and analyze the impact of these gate materials on the subthreshold swing, which in turn affects the device's gate controllability and gate coupling capacitance.

Figure 3.3 presents the experimental results, displaying the subthreshold swing values for HfO_2, SiO_2, and Al_2O_3 gate materials. It has been noticed that the subthreshold swing of HfO_2 is less in comparison to SiO_2 and Al_2O_3. This implies that HfO_2 offers improved gate controllability on the channel, allowing for more precise control over the transistor's switching behavior. A lower subthreshold swing is desirable as it signifies enhanced gate coupling capacitance, enabling efficient charge modulation and reduced leakage currents. This improved gate control ultimately leads to better overall device performance and power efficiency.

The results highlight the significance of selecting an appropriate gate material for achieving lower subthreshold swing values. HfO_2 exhibits superior performance in terms of subthreshold swing compared to SiO_2 and Al_2O_3. This finding suggests that integrating HfO_2 as the gate material in

JL GAA-SiNWFETs can lead to improved device performance, enhanced gate controllability on the channel, and superior gate coupling capacitance.

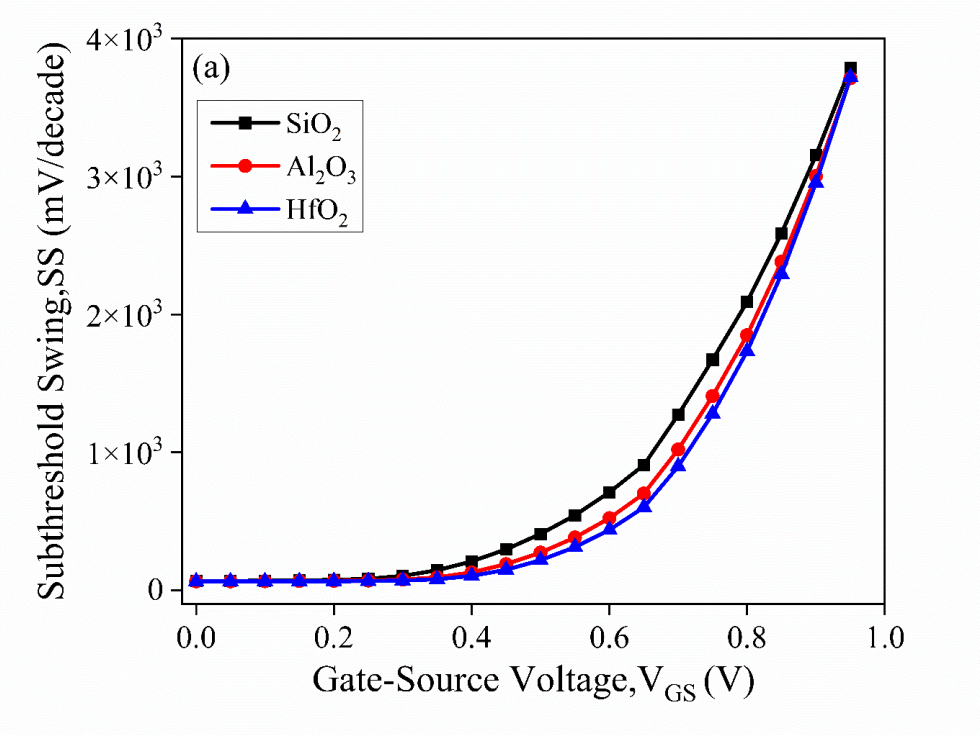


Figure 3.3 - The subthreshold swing vs gate voltage graph for JL-GAA-SiNWFET at V_D=0.1V

In summary, the study investigates the subthreshold swing characteristics of JL-GAA-SiNWFET using different gate materials. The findings demonstrate that HfO_2 offers a lower subthreshold swing compared to SiO_2 and Al_2O_3, indicating improved gate controllability and gate coupling capacitance. These results have significant implications for the design and optimization of semiconductor devices, particularly in achieving better performance and power efficiency.

3.4 Comparative Analysis of Device Efficiency in JL-GAA-SiNWFET with Different Dielectric Materials

Efficiency and power performance are crucial factors in the design of semiconductor devices. The transconductance generation factor (TGF) plays a significant role in determining the efficiency and gain of a device per unit power loss. In this study, we examine and compare the TGF characteristics of JL GAA-SiNWFETs utilizing different gate materials, including HfO_2, SiO_2, and Al_2O_3.

Figure 3.4 illustrates the experimental results, showcasing the TGF values for each gate material. The TGF, being directly proportional to the transconductance, represents the efficiency and gain achieved per unit of power dissipation in the device. Higher TGF values indicate enhanced device efficiency and superior performance, particularly when operating at low power supply levels. Our findings demonstrate that HfO_2 exhibits a higher TGF compared to SiO_2 and Al_2O_3 gate materials. This signifies that the device efficiency of HfO_2 is superior to the other materials, indicating its capability to generate more gain per unit power loss. The peak performance of HfO_2 in terms of both transconductance and TGF further highlights its effectiveness in achieving higher efficiency levels. This finding has significant implications for low-power applications, where maximizing efficiency is crucial. By utilizing HfO_2 as the gate material, designers and engineers can optimize device performance, reduce power consumption, and achieve higher efficiency levels. In summary, the study investigates the transconductance generation factor (TGF) in JL GAA-SiNWFETs using different gate materials. The results reveal that HfO_2 exhibits a higher TGF compared to SiO_2 and Al_2O_3, indicating improved device efficiency and performance. These findings emphasize the potential of HfO_2 as a gate material for achieving higher efficiency and gain per unit power loss. Further exploration of HfO_2-based devices can lead to advancements in low-power applications, enabling more efficient semiconductor devices.

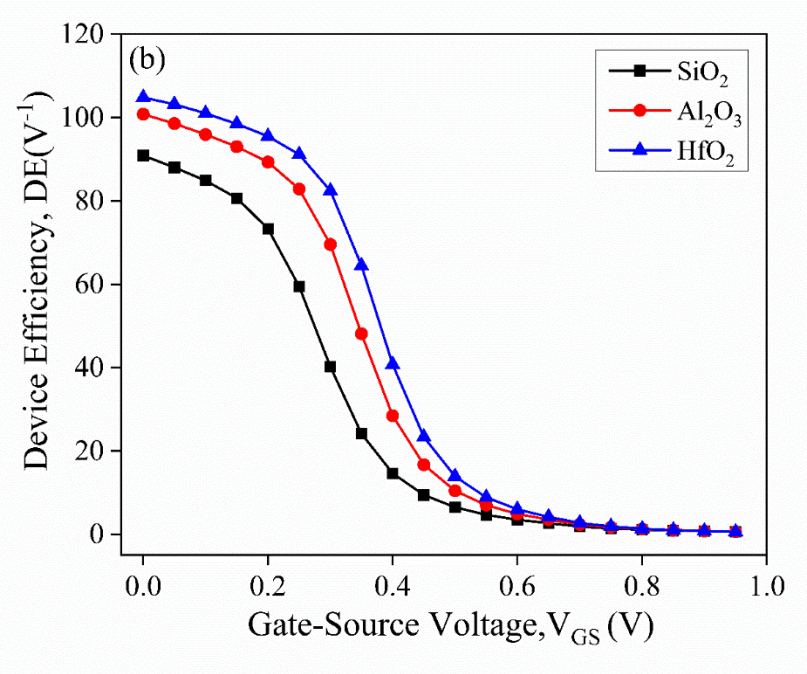


Figure 3.4 - The device efficiency vs gate voltage graph for JL-GAA-SiNWFET at V_D=0.1V

3.5 Comparative Analysis of Different Dielectric Materials in JL-GAA-SiNWFET for Switching Performance and Leakage Current

This study examines the effects of various gate materials on the switching performance and leakage current of JL GAA-SiNWFET. Figure 3.5 presents the switching ratio, represented by I_{ON}/I_{OFF}, as a function of the dielectric constant at V_D=0.1V. The results indicate that the peak performance is achieved with HfO_2, surpassing SiO_2 and Al_2O_3. This suggests that the speed of the device is significantly improved when utilizing HfO_2 as the gate material. Furthermore, figure 3.6 demonstrates the leakage current, denoted by I_{OFF}, for the JL-GAA-SiNWFET with different gate materials. It is observed that HfO_2 exhibits a lower leakage current compared to the other materials. A lower leakage current is desirable as it reduces the occurrence of the short channel effect. These findings highlight the favorable characteristics of HfO_2 gate material with a dielectric constant of 25, in terms of both switching performance and leakage current. Overall, the study provides valuable insights into the impact of gate materials on the performance of JL GAA-SiNWFET, emphasizing the superiority of HfO_2 in terms of speed enhancement and reduced leakage current.

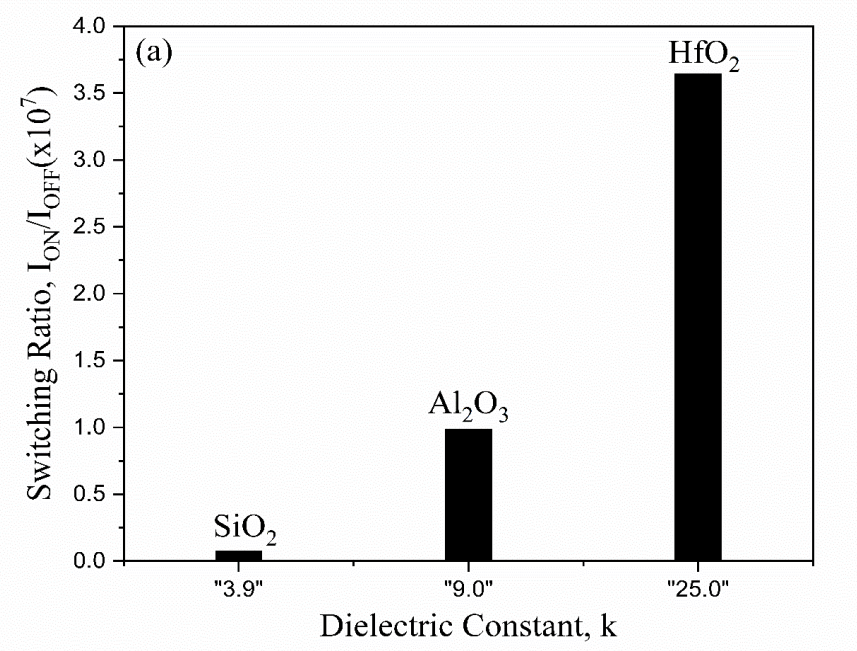


Figure 3.5 -. The switching ratio vs dielectric material graph for JL-GAA-SiNWFET at V_D=0.1V.

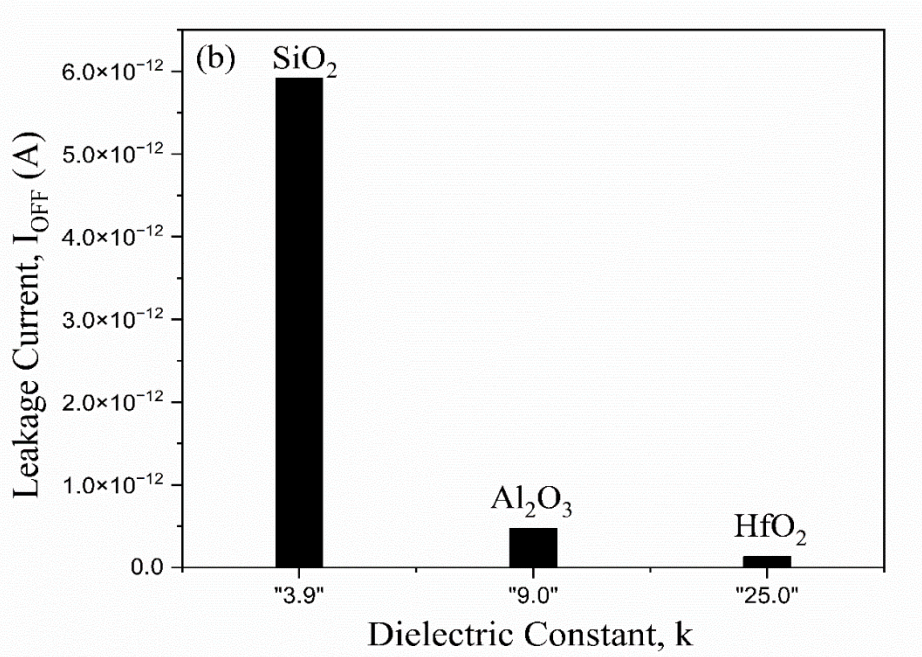


Figure 3.6 - The leakage current vs dielectric material graph of JL-GAA-SiNWFET at V_D=0.1V.

CONCLUSION

In this paper, we have investigated the impact of variation in high-k dielectric materials on the analog and switching performance of JL-GAA-SiNWFETs. We have used ATLAS SILVACO 3D to simulate the devices at low bias drain voltage (0.1V) and Niobium as gate electrodes having a work function of 4.8eV. We have studied the following parameters: I_D-V_G, transconductance, subthreshold swing, device efficiency, switching ratio, and leakage current. The transconductance of HfO_2 is 29% enhanced from SiO_2, the subthreshold swing is lowered by 6%, and the switching ratio is 48 times better than SiO_2. We have found that HfO_2 dielectric material performs best in all these parameters.

REFERENCES

[1] G. Jayakumar *et al.*, "Wafer-scale HfO 2 encapsulated silicon nanowire field effect transistor for efficient label-free DNA hybridization detection in dry environment," *Nanotechnology*, vol. 30, no. 18, Feb. 2019, doi: 10.1088/1361-6528/aaffa5.

[2] M. Karbalaei, D. Dideban, and H. Heidari, "Impact of high-k gate dielectric with different angles of coverage on the electrical characteristics of gate-all-around field effect transistor: A simulation study," *Results Phys*, vol. 16, Mar. 2020, doi: 10.1016/j.rinp.2019.102823.

[3] S. K. Dargar and V. M. Srivastava, "Performance analysis of high-k dielectric based silicon nanowire gate-all-around tunneling FET," *International Journal of Electrical and Electronic Engineering and Telecommunications*, vol. 8, no. 6, pp. 340–345, Nov. 2019, doi: 10.18178/ijeetc.8.6.340-345.

[4] Y. Taur and T. H. Ning, *Fundamentals of modern VLSI devices*. Cambridge University Press, 2009.

[5] "CMOS VLSI Design A Circuits and Systems Perspective."

[6] M. Zareiee, "A new architecture of the dual gate transistor for the analog and digital applications," *AEU - International Journal of Electronics and Communications*, vol. 100, pp. 114–118, Feb. 2019, doi: 10.1016/j.aeue.2019.01.012.

[7] A. G. Nassiopoulou *et al.*, *EUROSOI-ULIS 2017 : Joint International EUROSOl Workshop & International Conference on Ultimate Integration on Silicon-ULIS : 3-5 April, 2017, Athens, Greece*.

[8] A. G. Nassiopoulou *et al.*, *EUROSOI-ULIS 2017 : Joint International EUROSOl Workshop & International Conference on Ultimate Integration on Silicon-ULIS : 3-5 April, 2017, Athens, Greece*.

[9] M. Karbalaei and D. Dideban, "A novel Silicon on Insulator MOSFET with an embedded heat pass path and source side channel doping," *Superlattices Microstruct*, vol. 90, pp. 53–67, Feb. 2016, doi: 10.1016/j.spmi.2015.12.001.

[10] M. K. Anvarifard and A. A. Orouji, "A novel nanoscale SOI MOSFET with Si embedded layer as an effective heat sink," *International Journal of Electronics*, vol. 102, no. 8, pp. 1394–1406, Aug. 2015, doi: 10.1080/00207217.2014.982213.

[11] M. K. Anvarifard and A. A. Orouji, "A novel nanoscale low-voltage SOI MOSFET with dual tunnel diode (DTD-SOI): Investigation and fundamental physics," *Physica E Low Dimens Syst Nanostruct*, vol. 70, pp. 101–107, 2015, doi: 10.1016/j.physe.2015.02.015.

[12] Z. Ramezani and A. A. Orouji, "Improving self-heating effect and maximum power density in SOI MESFETs by using the hole's well under channel," *IEEE Trans Electron Devices*, vol. 61, no. 10, pp. 3570–3573, Oct. 2014, doi: 10.1109/TED.2014.2352317.

[13] A. A. Orouji and M. K. Anvarifard, “Novel reduced body charge technique in reliable nanoscale SOI MOSFETs for suppressing the kink effect,” *Superlattices Microstruct*, vol. 72, pp. 111–125, 2014, doi: 10.1016/j.spmi.2014.04.010.

[14] A. A. Orouji and M. K. Anvarifard, “SOI MOSFET with an insulator region (IR-SOI): A novel device for reliable nanoscale CMOS circuits,” *Mater Sci Eng B Solid State Mater Adv Technol*, vol. 178, no. 7, pp. 431–437, Apr. 2013, doi: 10.1016/j.mseb.2013.01.017.

[15] M. Luisier and O. Schenk, “Gate-stack engineering in n-type Ultrascaled SI Nanowire field-effect transistors,” *IEEE Trans Electron Devices*, vol. 60, no. 10, pp. 3325–3329, 2013, doi: 10.1109/TED.2013.2278573.

[16] Y. Pathak, B. D. Malhotra, and R. Chaujar, “Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer,” *Silicon*, vol. 14, no. 18, pp. 12269–12280, Dec. 2022, doi: 10.1007/s12633-022-01822-4.

[17] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, “Band-to-band tunneling in carbon nanotube field-effect transistors,” *Phys Rev Lett*, vol. 93, no. 19, Nov. 2004, doi: 10.1103/PhysRevLett.93.196805.

[18] S. K. Dargar and V. M. Srivastava, “Performance analysis of high-k dielectric based silicon nanowire gate-all-around tunneling FET,” *International Journal of Electrical and Electronic Engineering and Telecommunications*, vol. 8, no. 6, pp. 340–345, Nov. 2019, doi: 10.18178/ijeetc.8.6.340-345.

[19] Daniel Nenni, “Transistor Count Trends Continue to Track with Moore’s Law,” *SemiWiki (The open forum for semiconductor professionals)*, Mar. 05, 2020.

[20] E. N. Ganesh, K. Ragavan, and K. Kumar, “STUDY AND SIMULATION OF SILICON NANOWIRE FIELD EFFECT TRANSISTOR AT SUBTHRESHOLD CONDITIONS USING HIGH K DIELECTRIC LAYER AT ROOM TEMPERATURE,” *GESJ: Physics*, no. 1, 2010, [Online]. Available: https://www.researchgate.net/publication/230639927

[21] J. Wang, E. Polizzi, and M. Lundstrom, “A Computational Study of Ballistic Silicon Nanowire Transistors.”

[22] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-κ gate dielectrics: Current status and materials properties considerations,” *J Appl Phys*, vol. 89, no. 10, pp. 5243–5275, May 2001, doi: 10.1063/1.1361065.

[23] M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, “Application of HfSiON as a gate dielectric material,” *Appl Phys Lett*, vol. 80, no. 17, pp. 3183–3185, Apr. 2002, doi: 10.1063/1.1476397.

[24] A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, and T. Zabel, "Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films," *J Appl Phys*, vol. 90, no. 12, pp. 6466–6475, Dec. 2001, doi: 10.1063/1.1417991.

[25] E. Gusev *et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices", doi: 10.00.

[26] D. C. Gilmer *et al.*, "Compatibility of silicon gates with hafnium-based gate dielectrics," in *Microelectronic Engineering*, Sep. 2003, pp. 138–144. doi: 10.1016/S0167-9317(03)00290-9.

[27] K. Kumar, A. Raman, B. Raj, S. Singh, and N. Kumar, "Design and optimization of junctionless-based devices with noise reduction for ultra-high frequency applications," *Appl Phys A Mater Sci Process*, vol. 126, no. 11, Nov. 2020, doi: 10.1007/s00339-020-04092-2.

[28] Institute of Electrical and Electronics Engineers., *2008 IEEE Symposium on VLSI Circuits : Honolulu, HI, 18-20 June 2008.* IEEE, 2008.

[29] M. Chudzik *et al.*, "1A-1 High-Performance High-/Metal Gates for 45nm CMOS and Beyond with Gate-First Processing," 2007.

[30] K. Mistry *et al.*, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," 2007.

[31] M. Zaremba-Tymieniecki, C. Li, K. Fobelets, and Z. A. K. Durrani, "Field-effect transistors using silicon nanowires prepared by electroless chemical etching," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 860–862, Aug. 2010, doi: 10.1109/LED.2010.2050572.

[32] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Reports on Progress in Physics*, vol. 69, no. 2, pp. 327–396, 2006, doi: 10.1088/0034-4885/69/2/R02.

[33] "Chapter 2 Thin-Film Transistors,"

[34] al-Ǧāmiʿa al-Lubnānīya Beirut, International Conference on Microelectronics 25 2013.12.15-18 Beirut, and ICM 25 2013.12.15-18 Beirut, *2013 25th International Conference on Microelectronics (ICM) 15-18 Dec. 2013, Beirut, Lebanon*.

[35] Emma Ashley, "What is MOSFET? A detailed guide on MOSFET," *Designspark*, Jun. 18, 2021.

[36] A. H. Bayani, J. Voves, and D. Dideban, "Effective mass approximation versus full atomistic model to calculate the output characteristics of a gate-all-around germanium nanowire field effect transistor (GAA-GeNW-FET)," *Superlattices Microstruct*, vol. 113, pp. 769–776, Jan. 2018, doi: 10.1016/j.spmi.2017.12.019.

[37] I. Saad *et al.*, "The dependence of saturation velocity on temperature, inversion charge, and electric field in a nanoscale MOSFET The dependence of saturation velocity on temperature, inversion charge and electric field in a nanoscale MOSFET," 2010. [Online]. Available: https://www.researchgate.net/publication/229021006

[38] al-Ǧāmiʿa al-Lubnānīya Beirut, International Conference on Microelectronics 25 2013.12.15-18 Beirut, and ICM 25 2013.12.15-18 Beirut, *2013 25th International Conference on Microelectronics (ICM) 15-18 Dec. 2013, Beirut, Lebanon*.

[39] "Enhancement VS Depletion MOSFET Advantages, Applications," *E Techno G*, 2018.

[40] B. Kumar and R. Chaujar, "Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance", doi: 10.1007/s12633-021-01395-8/Published.

[41] J. Madan and R. Chaujar, "Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 227–234, Jun. 2016, doi: 10.1109/TDMR.2016.2564448.

[42] C. Electrical Engineering/Electronics, *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, 2008, ECTI-CON 2008, 5th International Conference on : 14-17 May 2008.* IEEE, 2007.

[43] A. Kuc, N. Zibouche, and T. Heine, "Influence of quantum confinement on the electronic structure of the transition metal sulfide TS2," *Phys Rev B Condens Matter Mater Phys*, vol. 83, no. 24, Jun. 2011, doi: 10.1103/PhysRevB.83.245213.

[44] S. Dash and G. P. Mishra, "An extensive electrostatic analysis of dual material gate all around tunnel FET (DMGAA-TFET)," *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 7, no. 2, Jun. 2016, doi: 10.1088/2043-6262/7/2/025012.

[45] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Drain current model for a gate all around (GAA) p-n-p-n tunnel FET," *Microelectronics J*, vol. 44, no. 6, pp. 479–488, Jun. 2013, doi: 10.1016/j.mejo.2013.04.002.

[46] R. Chaujar and M. G. Yirak, "Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor," *Silicon*, vol. 15, no. 1, pp. 609–621, Jan. 2023, doi: 10.1007/s12633-022-02242-0.

[47] S. Manikandan, & P. S. Dhanaselvam, and & M. K. Pandian, "A 2D Unified Subthreshold Drain Current Investigation for Junctionless Cylindrical Surrounding Gate(JCSG) Silicon Nanowire Transistor", doi: 10.1007/s12633-021-01292-0/Published.

[48] N. Fakhri, M. S. Naderi, S. G. Farkoush, S. S. Nahaei, S. N. Park, and S. B. Rhee, "Simulation of perovskite solar cells optimized by the inverse planar method in silvaco: 3d electrical and optical models," *Energies (Basel)*, vol. 14, no. 18, Sep. 2021, doi: 10.3390/en14185944.

[49] M. W. Ha, O. Seok, H. Lee, and H. H. Lee, "Mobility models based on forward current-voltage characteristics of P-type Pseudo-vertical diamond Schottky barrier diodes," *Micromachines (Basel)*, vol. 11, no. 6, p. 598, Jun. 2020, doi: 10.3390/MI11060598.

[50] International Conference on Electrical Information and Communication Technology 3. 2017 Khulna, Institute of Electrical and Electronics Engineers Bangladesh Section, International Conference on Electrical Information and Communication Technology 3 2017.12.07-09 Khulna, and EICT 3 2017.12.07-09 Khulna, *3rd International Conference on Electrical Information and Communication Technology EICT 2017 : 7-9 December 2017*.

[51] N. Gupta and R. Chaujar, "Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers," *Appl Phys A Mater Sci Process*, vol. 122, no. 8, Aug. 2016, doi: 10.1007/s00339-016-0239-9.

[52] A. Buchanan, "by D Scaling the gate dielectric: Materials, integration, and reliability," 1999.