TCAD Analysis and Modelling of Gate Stack Gate-All-Around Junctionless Nanowire Field-Effect Transistor for Sensing Applications

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This thesis is dedicated to my parents,

For their endless support and encouragement.

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CERTIFICATE

This is to certify that the thesis entitled "**TCAD Analysis and Modelling of Gate Stack Gate-All-Around Junctionless Nanowire Field-Effect Transistor for Sensing Applications**," being submitted by **Mekonnen Getnet Yirak (Reg. No. 2K18/PhD/AP/31)**, to Delhi Technological University, Bawana Road, Delhi-110042 (India), for the award of degree of **DOCTOR OF PHILOSOPHY** is a bonafide record of the research work carried out by him under my supervision and guidance. According to University standards, the thesis is complete. It is further certified that the work embodied in this thesis is original and has neither partially nor fully submitted to any other Institute or University for the award of any other degree or diploma.

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DECLARATION

I, Mekonnen Getnet Yirak, hereby certify that the thesis titled **"TCAD Analysis and Modelling of Gate Stack Gate-All-Around Junctionless Nanowire Field-Effect Transistor for Sensing Applications,"** submitted in the fulfilment of the requirements for the award of the degree of Doctor of Philosophy is an authentic record of my research work carried out under the supervision of **Prof. Rishu Chaujar**. This work in the same form or any other form has not been submitted by me or anyone else earlier for any purpose. Any material borrowed or referred to is duly acknowledged.

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Nomenclature / Terminology

GIDL	Gate-induced-drain leakage
DIBL	Drain-induced-barrier-lowering
DGJLT	Double-gate-junctionless-transistor
DGS	Double-layer gate stack
EOT	Effective oxide thickness
GAA	Gate all around
SiNW	Silicon Nanowire
IM	Inversion-mode
JLT	Junctionless transistor
LPCVD	Low-pressure-chemical-vapor-deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
Mug-FET	Multiple gate field effect transistor
SCEs	Short channel effects
SOI	Silicon on insulator
SS	Subthreshold swing
CLM	Channel length modulation
V_{th}	Threshold Voltage
V_{GS}	Gate source Voltage
DGMOS	Double-gate metal-oxide-semiconductor
V_{DS}	Drain Source Voltage
ITRS	International roadmap for semiconductors
BTBT	Band to band tunneling
TCAD	Technology computer-aided design
TFET	Tunnel field-effect transistor
High-K	High dielectric material/high dielectric gate oxide
CMOS	Complementary metal oxide semiconductor

Abstract

Continuous market demand drives device engineers to create Integrated Circuits (ICs) with low power dissipation and low fabrication complexity. Nanoelectronics technology is approaching the atomic/physical device limits due to the increasing demands of semiconductor chips. Significant technological development has been in the integrated circuit industry over the past few decades. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a crucial Integrated Circuits (IC) component. The integrated circuit doubled the number of on-chip transistors every generation, reducing physical device size. It has attracted numerous novel structures and MOSFET devices. However, scaling presents numerous challenges as it approaches the nanometre regime. It causes threshold voltage roll-off, short channel effect (SCEs), increases body-bias impact, and other negative consequences. SiO_2 gate oxides, in particular, have already reached a few atom lengths and thicknesses, resulting in increased power dissipation due to the quantum mechanical tunnelling effect.

Therefore, new materials and novel device architectures are necessary to guarantee the final scaling in device dimensions and sustain the anticipated performance benefit from the scaling. One of the most promising device architectures for extending the scaling of the CMOS device is the Gate All Around (GAA) MOSFET, which provides better hot carrier reliability than the Bulk MOSFET due to improved gate control and the best electrostatic control of the channel. Serious challenges with the device and circuit dependability are caused by scaling trends in MOSFETs, operating constraints, process damage, and radiation damage. At the Si-SiO_2 interface of the MOSFET, all of these degradation mechanisms lead to the formation of interface traps and localized charges. For instance, hot-carrier-induced deterioration in the form of interface traps in nanoscale MOSFETs caused by impact ionization in the channel near the drain junction has become a significant reliability issue since it reduces the design margin for circuits. Even a minuscule amount of interface traps/charges might negatively impact the device's performance due to the rising integration density of integrated circuits and the reduction in device size. Understanding MOSFET-level degradation, developing analytical models that include the effects of interface charges, and investigating new device architectures and techniques that are self-sufficient in preventing the formation of interface traps are crucial for improving overall design efficiency.

Newly designed device structure, like multi-gate architecture, helps reduce leakage currents, interface trap charges, and other detrimental short-channel effects. For instance, the Gate All

Around (GAA) structure is considered to be one of the best multiple gate structures as it shows better gate controllability, suppressed floating body effect, and excellent CMOS compatibility, even at the nanoscale regime. Also, in short-channel devices, the fabrication complexity due to a steep source/drain and channel junctions is difficult. Other impacts like short channel effects and hot carriers are undesirably increasing when device design goes near and below the 20nm technology node. As a result of these factors, the junctionless transistor has been developed as a superior replacement for the junction-based transistor in addition to its remarkable properties. Since the source, channel, and drain regions are all uniformly strongly doped, no junctions can form, resolving the problem of impurity diffusion. With this in mind, a novel Junctionless Surrounding metal Gate Stack Nanowire FET Sensor device was designed to incorporate multi-gate MOSFETs' advantages for high-sensing applications. This thesis investigates the sensitivity of junctionless gate stack Gate All Around NWFET devices and how they behave when subjected to hot carrier-induced interface localized charges. For instance, impact of localized charge on device electrical characteristics, such as I_{OFF} switching ratio, drain currents, transconductance (g_m), output conductance (g_d), surface potential, intrinsic voltage gain, output resistance, device efficiency, and device sensitivity (shifting threshold voltage and subthreshold current ratio) have been examined.

A 2D analytic model was also developed for surface potential, drain current and threshold voltage using the superposition theorem by applying the boundary conditions and validating at different silicon film radius channel lengths. The analytical model has been validated at different channel lengths and silicon film radii. The effect of varying gate work functions (gate optimization technique) on the performance of the device sensitivity was also studied. In addition to localized charge, the gate leakages seriously hamper the device performance at shorter channel lengths and impact the device sensitivity or performance; Due to this, a novel device architecture, “cylindrical Metal Gate (CMG) Dielectric Engineered (DE) JLNWFET,” was developed to improve device efficiency and sensitivity. In this direction, high Channel uniformly doping single/ dual/triple hybrid gate material engineering GAA NWFETsensors were designed to enhance their current driving capability and transconductance without increasing the electric field at the drain side. When MOS devices are utilized in sensing applications, the dielectric, which determines the performance and reliability of the device, also plays a crucial role. In this work, gate stack metal gate electrode GAA JL NWFET for various sensing applications has been investigated. Gate stack GAA JL NWFET with catalytic metal gate is studied for its use as a hydrogen gas sensor. Gate stack GAA JL NWFET with a nanocavity region for dielectric has

been investigated for dielectric modulation-based biosensor applications. Also, an analytical model for gate stack GAA JL NWFETs with varied gate electrode engineering is established to study the impact of different gate electrodes on the performance of Gate stack GAA JL NWFET devices; analytical results are verified with device simulation results. Gate stack GAA JL NWFET shows much higher sensitivity for biosensing and hydrogen gas sensing in the subthreshold region as compared to conventional bulk MOSFET. The junctionless gate stack GAA NWFET' is a promising device architecture for creating a low-power, extremely sensitive, and nanoscale CMOS-compatible biosensor and hydrogen gas sensor due to its high surface-to-volume ratio, low leakage current, and almost optimal subthreshold slope (SS) close to (60 mV/decade).

List of Publications

Articles in International Journal:

1. **Mekonnen Getnet and Rishu Chaujar, "**Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor," ***Silicon Journal*****, Vol.15,** pp.609-621, ***Springer (SCIE, IF-2.941),*** **2022.**
2. **Mekonnen Getnet and Rishu Chaujar, "**Sensitivity Analysis of Biomolecule Nanocavity Immobilization in a Dielectric Modulated Triple-Hybrid Metal Gate-All-Around Junctionless NWFET Biosensor for Detecting Various Diseases", ***Journal of Electronic Materials*****, Vol.51, No.5, pp**.2236-2247. ***Springer (SCIE, IF-2.047),*** **2022.**
3. **Mekonnen Getnet and Rishu Chaujar, "**Numerical Modelling for triple hybrid gate optimization dielectric modulated junctionless gate all around SiNWFET based uricase and ChO_X biosensor," ***Journal of Electronic Materials (Springer), Submitted,*** **2023.**
4. **Mekonnen Getnet and Rishu Chaujar, "**Effect of trap charges on Dielectric Modulated Triple Hybrid Metal Gate Junctionless Gate All Around Silicon Nanowire FET based APTES & Biotin Biosensor", ***Silicon Journal (Springer),*** (Submitted), **2023.**

International Conference Proceedings:

1. **Mekonnen Getnet and Rishu Chaujar**, "TCAD Analysis and Modelling of Gate-Stack Gate All Around Junctionless Silicon NWFET-Based Bio-Sensor for Biomedical Application," **2nd International Conference on IEEE VLSI Device, Circuit, and System (VLSI-DCS)**, on July 18th -19th, 2020.
2. **Mekonnen Getnet and Rishu Chaujar**, "Interface Trap Charge Analysis of Junctionless Triple Metal Gate High-k Gate All Around Nanowire FET-Based Biotin Biosensor for Detection of Cardiovascular Diseases," **7th International Conference on Microelectronics, circuits, and systems**, on July 25th -26th, 2020.

***Book Chapter Contribution*:**

1. **Mekonnen Getnet and Rishu Chaujar,** "Demand of Low power-driven FET as Biosensors in Biomedical applications," published in CRC **Press Taylor & Francis Group, USA**, **pp.255-272, 2022**.
2. **Mekonnen Getnet and Rishu Chaujar,** "TFET: "Operation Principle and Fabrication of TFET," **Under Production in Wiley**, **2023**.
3. **Mekonnen Getnet and Rishu Chaujar,** "Fundamental of Emerging Nano-Materials (Graphite, Graphene, CNT, Insulators and High-k Materials and Perovskite Materials including their applications)," **Under Production in Springer Nature**, **2023**.

CHAPTER -1

1.1 Introduction

The international economy has been driven by computing and communication technology over the last decade. The electronics industry currently accounts for more than 10% of the global economy, and this number is continuously rising[1]. In 1947, Bell Labs' own Bardeen, Brattain, and Shockley developed the first solid-state device, a bipolar point-contact transistor on a Germanium (Ge) substrate[2]. This development marked the beginning of a revolution in the semiconductor industry. Bipolar transistors have almost been superseded by complementary metal oxide semiconductor (CMOS) field-effect transistors due to the former's reduced power consumption and technological advantages. Gordon Moore stated in 1965 that with improved characteristics, the number of transistors per chip would double every 18 months[3]. Interestingly, as illustrated in **Figure 1. 1**, the semiconductor manufacturing industry has proven this rule over five decades. With lower dimensions for higher packing density, ultra-low power dissipation, and higher circuit speed, CMOS technology has established itself as the industry standard. Over the past few decades, the IC industry has expanded astronomically due to MOS transistors' rapid and ongoing scaling [4]. As illustrated in **Figure 1. *2***, industry consumers raised their need for faster data rates, which supported the demand for additional electronic devices[5]. However, as transistor dimensions continue to reduce in order to attain better dynamic read-only memory (DRAM) chip density and microprocessor speed, conventional single-gate MOSFETs encounter performance problems due to short channel effects and gate leakage currents[6]. When conventional MOSFETs are downscaled to the sub-micrometer range, the device size and isolation length roughly match the depletion widths, which causes short channel effects (SCE), which can have serious consequences, including reducing the threshold voltage and increasing substrate bias effect[7]. Due to short channel effects and gate leakage currents, conventional single-gate MOSFETs struggle to meet the needed performance as transistor dimensions continue to shrink to attain greater DRAM chip density and microprocessor speed[8]. Gate control, current output, the power-to-performance ratio, and variation and dependability are some of the challenges associated with scaling the device down to a technology node smaller than 22 nm [9]. The gate control challenges are the SCEs (which include gate-induced drain leakage, drain-induced barrier lowering, and subthreshold slope degradation, amongst other things) that produce unacceptable leakage and subthreshold characteristics [10]. When the MOS downscaling approaches the fundamental limitations, unique materials and novel device architectures are required to achieve the ultimate scale in device dimensions and preserve anticipated performance gain [11]. For low-power applications, Gate All Around (GAA) MOSFETs have proven to be the most promising device structure for extending the scaling of the CMOS device due to their superior intrinsic RF scaling capability, excellent subthreshold characteristics, and excellent electrostatic control [12]. In addition to resilience to short-channel effects, tunnelling and reliability are critical concerns for nanoscale devices[13]. Device performance deterioration caused by interface traps resulting from hot carrier/radiation/process damage poses major reliability concerns[14]. Therefore, it is necessary to address these reliability challenges to estimate and optimize device

performance deterioration. The current delivered through the channel must be raised to improve device performance for each technological generation[15]. The industry has developed methods for improving mobility, such as strained silicon, an alternative gate electrode, and even substitute channel materials like silicon or germanium nanowires. GAA MOSFETs are being evaluated for numerous sensing applications due to their effective gate control and excellent surface-to-volume ratio. This chapter discusses various scaling challenges, like short-channel effects and different engineering schemes to reduce those challenges. **Figure 1.1** illustrates Moore's law by plotting transistor counts (number) versus product launch dates. According to the graph, the count increases by a factor of two every two years [16].

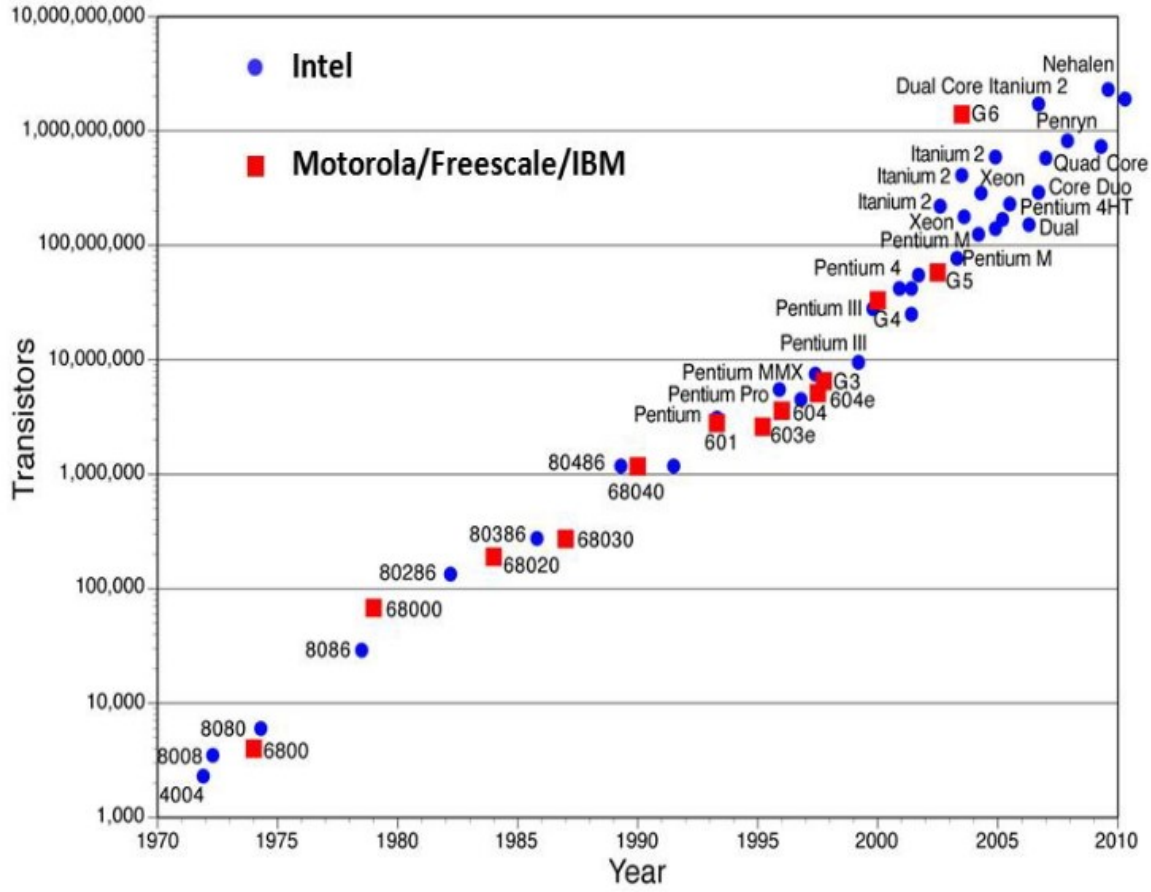


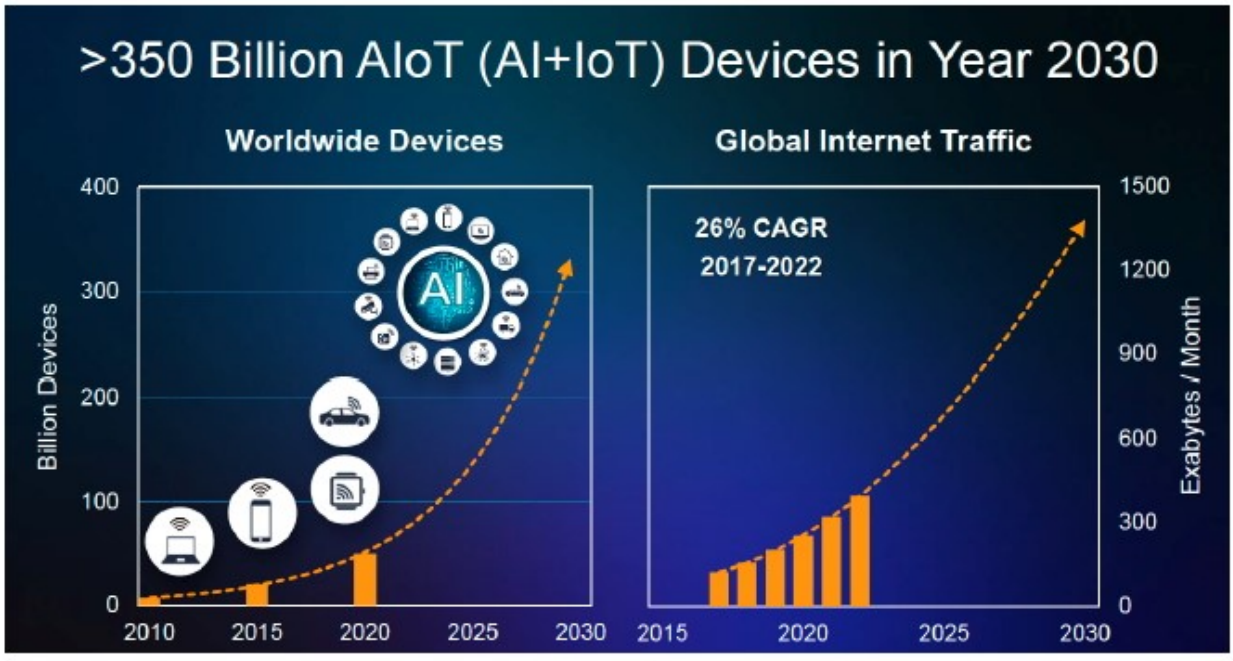
Figure 1. 1. illustrates Moore's law by plotting transistor counts (number) versus product launch date [16].

1.2 MOSFET Scaling (Review Literature)

Silicon CMOS has developed as the dominating technology in the microelectronics industry over the last 25 years[17]. Over several technological generations, the concept of device scaling has been constantly implemented, resulting in consistent improvements in device density and performance. The scaling pattern outlined in the ITRS roadmap (ITRS97) is shown in **Table 1.1** [18].

Table 1. 1. High-performance logic design requirements table. Information obtained from the 2003 ITRS.

Year in Production	units	2007	2008	2009	2010	2012	2013	2015	2016	2018
Physical Gate Length	nm	25	22	20	18	14	13	10	9	7
EOT (Equivalent Oxide Thickness)	A	9	8	8	7	7	6	6	5	5
Gate Layer Thickness value	A	4	4	4	4	4	4	4	4	4
Gate Dielectric Thickness Value	A	13	12	12	11	11	10	10	9	9
Maximum Gate Leakage Limit	A/cm^2	$9.3E^{+2}$	$1.1E^{+3}$	$1.2E^{+3}$	$1.9E^{+3}$	$2.4E^{+3}$	$7.7E^{+3}$	$1.0E^{+4}$	$1.9E^{+4}$	$2.4E^{+4}$
Power Supply Voltage	V	1.1	1	1	1	0.9	0.9	0.8	0.8	0.7
Saturation Threshold Voltage	V	0.18	0.17	0.16	0.15	0.14	0.11	0.12	0.10	0.11
Source/Drain Leakage Current	uA/um	0.07	0.07	0.07	0.1	0.1	0.3	0.3	0.5	0.5



Source: 2020 IEEE ISSCC, Cisco VNI Global IP Traffic Forecast 2017-2022

Figure 1. 2. Depicts the need for increased data speeds while simultaneously increasing demand for billions of devices [18].

3.2.1 Reasons for scaling

- Scaling down the MOSFET device enables the integration of additional transistors on a single chip, increasing the chip's packing density. This is especially significant in modern semiconductor technologies, with limited chip space. This opens up the possibility of making larger chips with greater functionality in the same space [3], [19] or smaller chips with the same functionality.
- Better performance can be achieved as a result of the fact that smaller devices often have shorter channel lengths. This, in turn, leads to faster switching speeds and enhanced performance.
- When MOSFET devices are shrunk in size, the operating voltage drops along with it, resulting in lower power usage.
- Scaling down MOSFET devices is a logical development in the history of semiconductor technology since they are compatible with modern fabrication techniques, which makes it easier to build smaller devices with higher accuracy [19], [20].

In general, scaling down MOSFET devices enables improved performance, increased packing density, lower power consumption, decreased cost, and compatibility with advanced production techniques. Because of these benefits, it has become an integral component of semiconductor technology.

These developments are causing an uptick in the need for portable systems with high processing and integration capacity. However, as MOSFETs are shrinking to deep submicron dimensions, the integrated circuit industry is finding it increasingly challenging to continue scaling at the same rate it has in the past. This is due to the small dimensions and the fact that certain vital devices, materials, and process limits are being approached[18]. Moreover, new materials with their learning curves for production will likely be introduced at future technology nodes, complicating scaling at these nodes even further. For instance, the need for low voltages and the complexity of the device fabrication process limit the size reduction of MOSFET transistors[21]. Excessive gate leakage current, boron penetration from the P+ polysilicon gate electrode into the MOSFET channel, and the growing destructive impact of polysilicon depletion in the polysilicon gate electrodes are all issues that have arisen as a result of the shrinking gate dielectric thickness[18]. In addition, projections show that as transistor sizes get smaller, the electron and hole mobility in the inversion layer will drop below what is required to achieve the desired transistor performance. Finally, the conventional planar bulk MOSFET itself will likely become insufficient to meet transistor requirements, mainly due to the difficulty in effectively controlling short-channel and quantum effects and statistical variability for very small transistors. To address these issues, numerous technological innovations were being explored (termed "potential solutions" in the ITRS)[20]. The development and implementation of these technological innovations into manufacturing will necessitate substantial improvements to computational modelling and characterization techniques and capabilities. Also, it won't be easy to achieve the required precision and accuracy in measuring the increasingly miniaturized transistor dimensions[18]. For instance,

the generation of traps, interface states, fixed charges, and defects in the oxide bulk or at the Si-SiO_2 interface is a common source of reliability issues in addition to heat removal and cooling becoming worse because the magnitude of power dissipated per unit area is increased[22]. Interface charges can be caused by various damage mechanisms, including but not limited to stress-induced damage, process-induced damage, damage caused by heat carriers, and damage caused by radiation [23]. As a result, understanding the degradation of CMOS devices and circuits due to various types of damage (e.g., radiation damage, stress/hot carrier/process damage) is required for the successful use of CMOS-based circuits. Therefore, a brief review of scaling challenges (short-channel effects) and their device implications is needed. The following section examines the various short-channel effects raised due to deep submicron dimensions MOSFET scaling.

1.3 Short Channel Effects in MOSFETs

A MOS transistor is considered short when its effective channel length (L_{eff}) is less than or equal to the depletion width of its source and drain junctions. In this instance, the potential distribution in the channel is influenced not only by the device's standard electric field but also by the device's lateral electric field. As a result, the channel area of a short-channel MOSFET is affected by the source/drain (S/D) as much as it is by the gate, leading to a complex 2-dimensional geometry in the depletion zone. This causes the short-channel effects listed in the following [7], [24]. Using a single gate to control the silicon region makes it challenging to eliminate these effects in ultra-short channel lengths, but it is possible to reduce them [7]. Researchers have attempted to reduce them using various techniques such as channel engineering, gate engineering, implementing different architectures with different working physics, and so on.

1.3.1 Drain-Induced Barrier Lowering

This phenomenon occurs when the gate voltage is less than the device's threshold voltage. As shown in **Figure 1. 3,** the depletion region under the drain can lower the potential barrier from the source-to-channel junction as the voltage drop between the source and drain increases [25]. More electrons can be injected into the channel region if the barrier between the source and channel is lowered. So, the gate has less effect over the channel current, and the threshold voltage drops[26]. Because of the inherent potential between the channel and the S/D regions, the channel is depleted even before a positive bias is applied to the gate. This potential is known as inherent potential. Drain-induced barrier lowering (DIBL) [27] describes a phenomenon in which the p-n junctions between the S/D and the channel are biased in the opposite direction, amplifying this effect [27]. When the gate length is shortened, the unwanted coupling between the S/D region and the channel grows, lowering the transistor's threshold voltage [22].

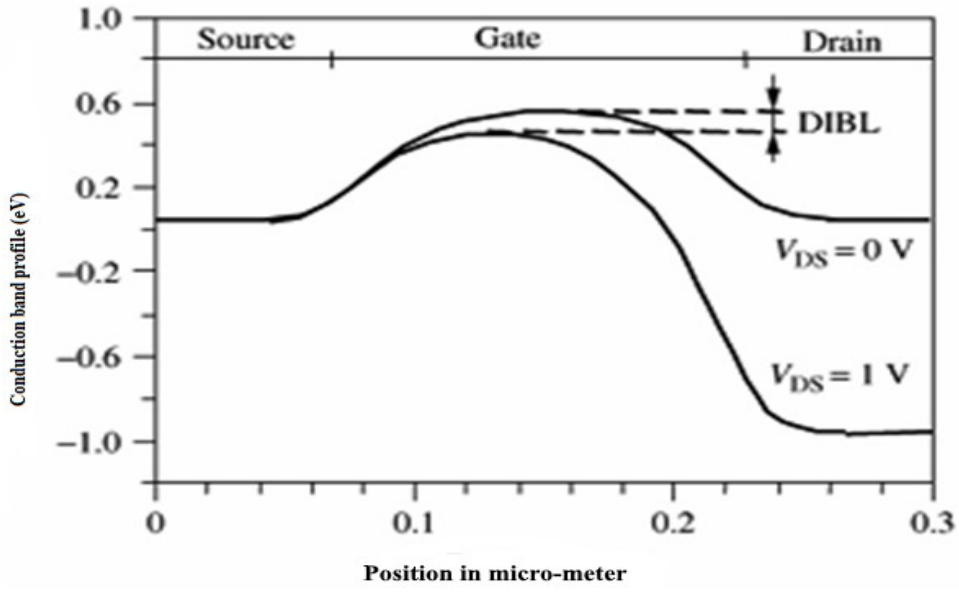


Figure 1. 3. Illustrates Drain-Induced Barrier Lowering (DIBL) [29].

1.3.2 Punchthrough

A punch-through occurs when the source and drain depletion regions meet [30]. When the depletion areas cross, as shown in **Figure 1. 4**, space-charge-limited current flows between the drain and the source. The drain bias and substrate doping are both critical for punch-through. The main reason for transistor punch-through is that current transport occurs deeper within bulk and away from the gate, leading to increased subthreshold leakage current and increased power consumption [19]. Punchthrough current (subthreshold leakage current) is highly sensitive to source/drain junction depths and applied drain voltage [19]. To prevent punch-through, higher substrate doping and spatially restricted dopant implantations, such as halo or pocket implantations, are required [31]. On the other hand, a higher doping level would result in a more significant rise in the tunnelling current that flows between the source and drain p-n junctions and the substrate [32].

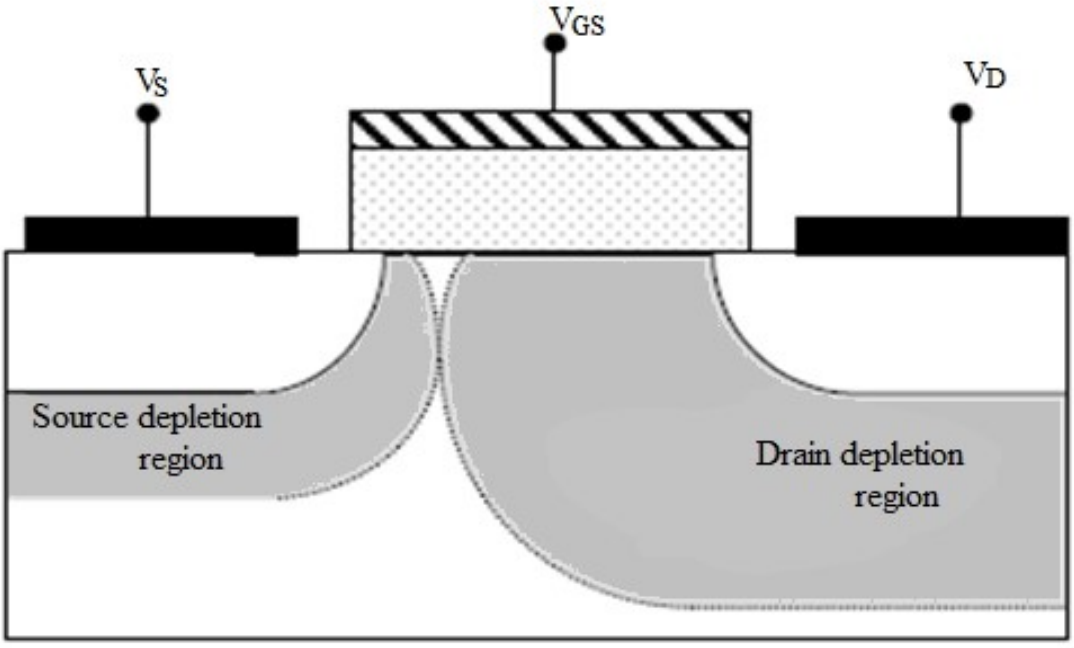


Figure 1. 4. Illustrates a schematic diagram for punch-through [30].

The depletion region can be made smaller by reducing the drain bias to prevent punch-through, higher substrate doping is required [31].

1.3.3 Higher Subthreshold Conduction

Subthreshold conduction is the term used to describe the flow of current between the source and drain of a MOSFET while the transistor is operating in the subthreshold area, which is also referred to as the weak-inversion region. This current is also known as subthreshold leakage or subthreshold drain current. This phenomenon occurs when the voltage from the gate to the source is less than the threshold voltage [24], [27]. As MOSFET geometries get smaller, the gate voltage that can be used must also decrease to keep the devices reliable. Reducing the MOSFET's threshold voltage is also essential to maintain performance. When the threshold voltage of a transistor is lowered, the available voltage swing becomes too small to allow for a complete turn-off to turn-on shift, thus leading to an increasing subthreshold current. When designing circuits, it is necessary to strike a balance between a high current in the "on" case and a low current in the "off" case [24].

1.3.4 Impact Ionization and Hot Electron Effect

The process by which one energetic charge carrier in a material loses energy due to the formation of other charge carriers in that material is referred to as impact ionization [33]. In semiconductors, the production of an electron-hole pair occurs when an electron (or a hole) with enough kinetic energy dislodges (knocks) a bound electron from its position in the valence band and promotes it to a condition in the conduction band [34]. When a MOS device conducts in saturation, the channel injects many carriers into the drain depletion region. The high field

around the drain speeds up these carriers, and some of them, through impact ionization, become hole-electron pairs[24]. Carriers travelling from the source to the drain might receive sufficient energy to generate impact ionization, producing electron-hole pairs in silicon and overcoming the interfacial energy barrier [33], [35]. When carriers are injected into a gate dielectric, this produces device degradation, which reveals itself as a change in the threshold voltage and a reduction in the drain current [33]. As a result, the transistor lifetime is significantly shortened due to hot carrier injection (HCI). To minimize this impact, the gate oxide separating the gate and channel should be as thin as possible to boost on-state channel conductivity and performance and decrease off-state subthreshold leakage. However, electron tunnelling between the gate and channel happens with today's gate oxides, which have a thickness of about 1.2 nm, leading to increased power consumption[36].

1.3.5 Channel Length Modulation (CLM)

It is helpful to visualize the MOSFET channel as consisting of two separate parts: the first part runs from the source to the saturation point, and the second component runs from the saturation point to the drain [25]. The saturation point of a channel gets closer to the source when the drain bias is increased. Thus, the effective channel length shortens, and the drain current grows even at saturation as a function of the drain voltage. The decrease in channel length is an increasing function of the V_{DS}-V_{DSAT}, leading to the channel length modulation (CLM) effect [26]. As can be seen in **Figure 1. 5**, the pinch point in the channel shifts from the drain terminal to the source terminal. When the effective channel length (L_{eff} = L-ΔL) decreases, the drain current increases for a given drain to source voltage (V_{DS})[25].

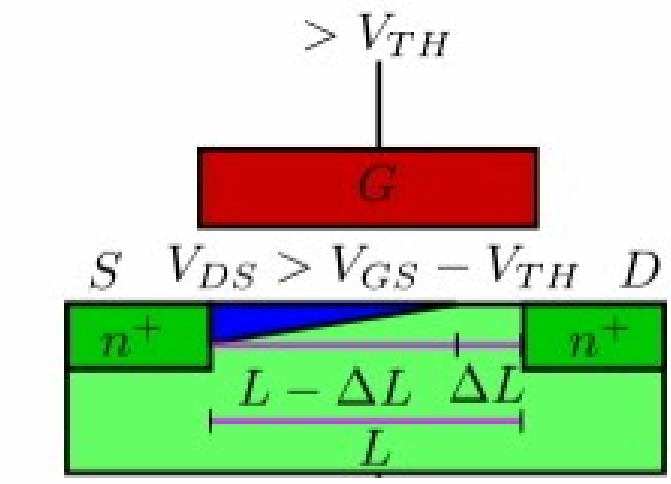


Figure 1. 5. Shows channel length modulation(CLM[25].

1.3.6 Velocity Saturation

Charge carriers' velocity, such as electrons or holes, is proportional to the electric field that drives them, but this is only applicable to small fields[37]. When the field strength increases, their velocities tend to saturate. As gate length decreases, the longitudinal electric field (E) between the source and drain increases, and carrier drift velocity (V_D) varies according to the lateral electric field[38], [39]. The rate of phonon emission increases with increasing electric

field strength, and velocity saturation occurs when the rate of energy gained from the electric field equals the rate of energy loss to the crystal via phonons[40]. So, for sufficiently high fields along the channel, the carrier velocity,($V = \mu E$), eventually saturates at a value of about 10^7 cm/s(for silicon channels)[27]. Here, μ and E denote the carrier mobility and electric field, respectively[41]. Therefore, saturation velocity affects the transistors' voltage transfer characteristics greatly because, at saturation velocity, they no longer obey Ohm's law[25], [27]. This effect increases the time a MOSFETS carrier travels the channel[25].

1.3.7 Gate Oxide Leakage

Because of its excellent interfacing capability with silicon material, SiO_2 is a very popular gate insulator used in MOSFETs[26]. However, gate oxide thickness has already approximated to 1 nm or less due to dimension scaling for better device performance. When the gate oxide thickness is less than $\sim$1 nm, the probability of tunnelling increases, resulting in an increase in oxide leakage current and quantum tunnelling effect [42], [43]. In recent times, to minimize direct tunnelling leakage current, high-k dielectric materials have been used[44]. To date, researchers have determined that hafnium oxide (HfO_2), hafnium silicates (HfSiON), and zirconium oxides (ZrO_2) are the most promising candidate dielectrics for thinner gate oxide MOSFET device structures to minimize short channel effect [45], [46].

1.3.8 Band-to-Band Tunnelling

The term "tunnelling" refers to a process in quantum mechanics that includes the movement of electrons through potential energy barriers [47]. Band-to-band tunnelling is the process that takes place when electrons move from the valence band to the conduction band (or vice versa) via the forbidden energy band gap [47]–[49]. This occurs as the oxide thickness decreases and the electric fields increase between the gate and drain regions of the semiconductor device. If the gate voltage is low and the drain bias is high, the electric field in the region where the gate and drain overlap will be larger. This band-to-band tunnelling probability is activated due to the overlap region, which is located where the valance band and the conduction band of the drain overlap [23]. Gate-induced drain leakage [32] may occur when electron-hole pairs are swept by band-to-band tunnelling into the drain and substrate regions.

1.3.9 Mobility Degradation (Surface Scattering)

The gate-induced vertical electric field acts on carriers as they move along the channel under the influence of the horizontal electric field, pushing carriers towards the gate oxide and encouraging or motivating them to crash into the oxide channel interface [50]. Due to an imperfect oxide channel interface, carriers lose mobility [51]. This effect, known as surface scattering, causes a decrease in mobility, impacting the drain current and transconductance[38].

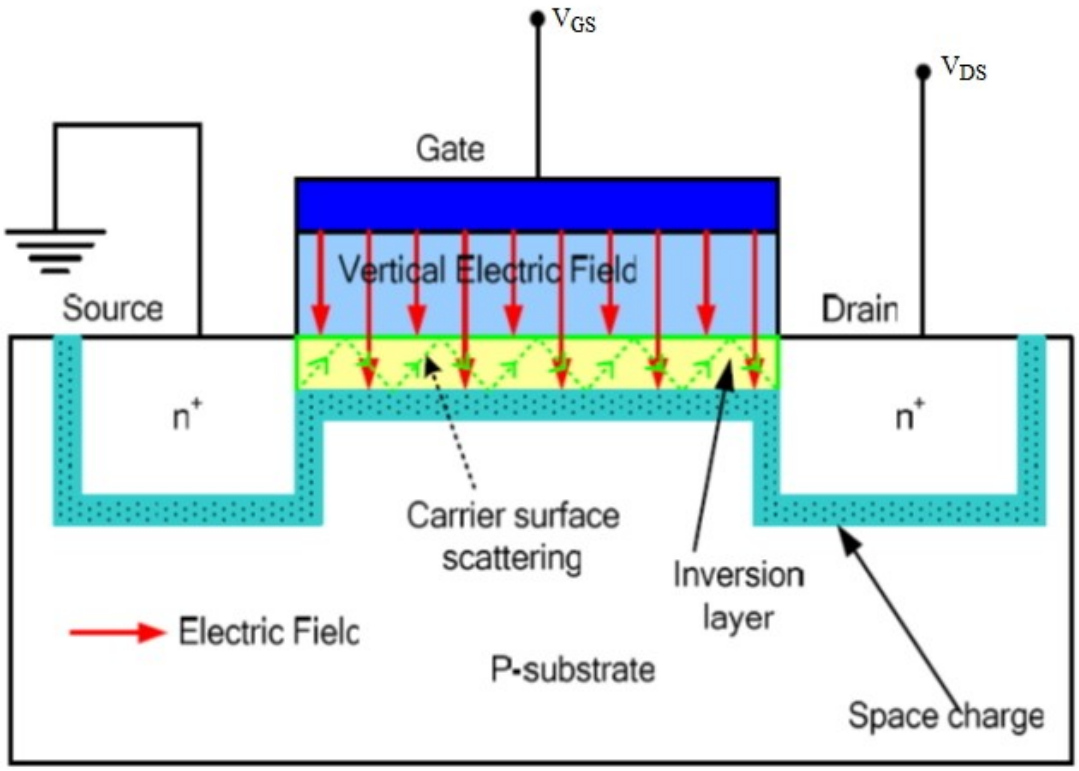


Figure 1. 6: Shows the vertical electric field and surface scattering in a short channel MOSFET [50].

1.4 Engineering schemes to reduce short channel effects

As previously discussed, both lateral and vertical dimensions (gate oxide thickness and junction depth) should be reduced to increase device packing density and device performance. However, producing MOSFETs with deep micrometre (nanometer) channel lengths is complex and will cause several challenges. In order to address scaling issues that have been encountered, there are potential solutions, such as the addition of new materials and new structures. Therefore, it is necessary to develop new silicon technology that incorporates a wide range of technological improvements. Here, we'll review some engineering techniques designed to improve conventional devices' electrical efficiency.

1.4.1 Gate Dielectric Engineering

Since the 1960s, SiO_2 has been the gate insulator of choice for silicon MOSFETs. Over the period of this time, the oxide thickness has shrunk, going from 300 nm for 10 nm technology to 1.2 nm for 65 nm technology [37], [52]. The reason for reducing oxide thickness is to obtain greater oxide capacitance (C_{OX}), which increases on-current (I_{ON}) and is desirable for maximizing circuit speed and controlling threshold voltage roll-off (V_{th}) in the presence of decreasing channel length[53]. Because of the thin oxide layer, electrons from strongly inverted surfaces can tunnel into or through the SiO_2 layer. This phenomenon, known as gate-induced drain leakage (GIDL), is what causes tunnelling current through decreased gate oxide thickness [54]. This takes place as a consequence of the thin oxide layer, which causes the breadth of the

potential barrier to be relatively narrow. The tunnelling leakage current becomes the dominant limiting factor when SiO_2 gate oxide is thinner than 1.5 nm. In a short channel device, drain electric field is strong, which causes thinner gate oxide to be destroyed and leads to a leakage current [49]. Below 1nm gate oxide thickness or decreases rapidly with the new technologies, the gate leakage current will become more prominent, increasing exponentially as a function of the gate oxide thickness and applied drain-source voltage[50]. In order to solve these significant problems, high-gate dielectrics have been employed in place of SiO_2 gate dielectrics and the physical thickness of the dielectric layer will be kept broad. This has the effect of lowering the gate leakage current while keeping the capacitance value the same [42], [43], [55], [56]. These materials make it possible to have a high physical thickness while keeping a tiny effective oxide thickness (EOT), making it possible to scale the EOT for future generations of MOS devices [55]. The equivalent oxide thickness (EOT) refers to the thickness of a layer of SiO_2 that has the same capacitance as the high-k dielectric layer [57][58]. Increased gate control over the channel is possible by using high-k dielectric materials[44]. Still, these improvements are not without drawbacks due to imperfections such as interface traps, fixed bulk charges, low interface carrier mobility, and phase stability issues[57][59]. SiO_2 forms a thin interfacial layer on silicon because no other dielectric material can create a native oxide on the silicon[60]. For the purpose of immobilizing biomolecules in the cavity region, a substantial layer of SiO_2 serves as a binding agent layer. As a consequence of this, as can be seen in **Figure 1. 7**, the majority of these unique dielectrics now consist of a thick High-k layer sandwiched between a thin SiO_2 interfacial layer and a poly-Si or metal gate electrode [61]. Depending on the physical layer thickness and k values, the applied gate voltage is dipped(dropped) over the interfacial SiO_2 and high-k layers.

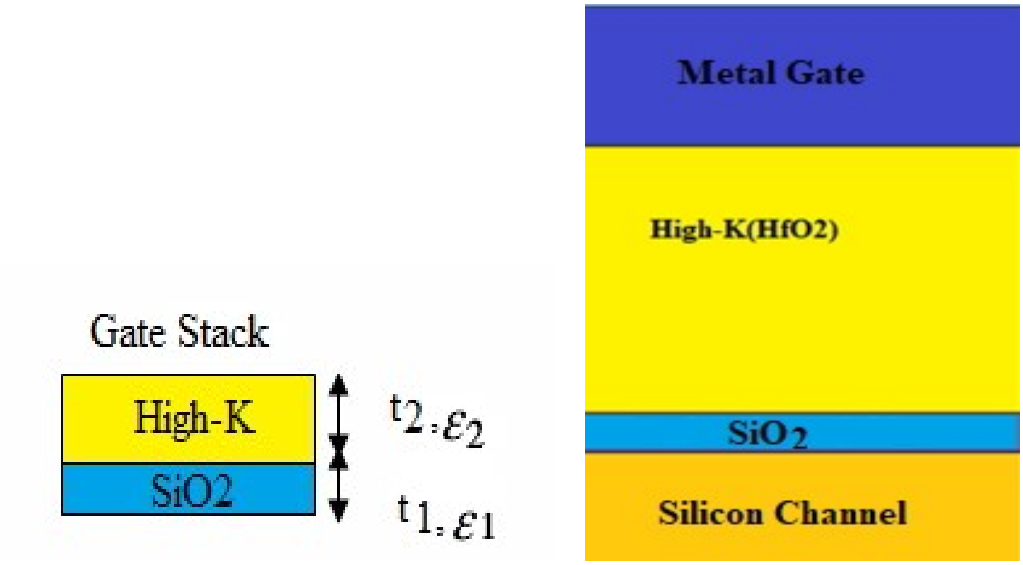


Figure 1. 7. Illustrates Gate Stack Architecture[62].

Therefore, the extra-thin low-k interlayer enhances the quality and stability of the interface in a stacked gate architecture. Adding a low-k layer to a stacked gate architecture with the same EOT significantly reduces the fringing electric field. Because of the continuity of the displacement, the high fringing fields are electrically focused into the low-k dielectric layer,

which may alter the relative fringing field effect on the device's characteristics[63]. In gate stack architecture, the formula will decide the effective thickness(EOT)[42], [57] shown below.

$$(EOT) = t_{high-k}\left(\frac{k_{SiO_2}}{k_{high-k}}\right) + t_{low-k} \quad (1.1)$$

1.4.2 Gate Electrode Engineering

Leakage currents have become an issue in VLSI MOS technology due to the ongoing scaling of gate lengths, gate oxides, and threshold voltages. These currents need to be relieved (controlled) so that the problem may be addressed. Power dissipation is another problem, especially for small devices, because of the leakage currents [45]. The electric field distribution along the channel affects MOSFET gate transport efficiency [51]. In a field effect transistor, electrons have a slow initial velocity as they enter the channel, but their speed rapidly increases as they move closer to the drain [64]. Because the maximum electron drift velocity is attained closest to the drain, the electrons move very quickly in that region; nevertheless, they move relatively slowly, closest to the source. This is due to the fact that the highest electron drift velocity is reached closest to the drain. As a consequence, the speed of the device is impacted by the comparatively slow electron drift velocity in the channel that is located close to the source region. as a result of the depletion effects brought about by the polysilicon gate [65]. To provide no depletion effect and significantly improved threshold voltage control, a polysilicon gate must be replaced by a metal gate electrode [66]. As a result, different architecture like double gate material MOSFET was proposed to improve the gate transport efficiency and lower the SCEs[37], [67], as shown in **Figure 1. 8**. To improve carrier velocity, the electric field profile of the channel is optimized to be larger near the source end and smaller near the drain end [68].

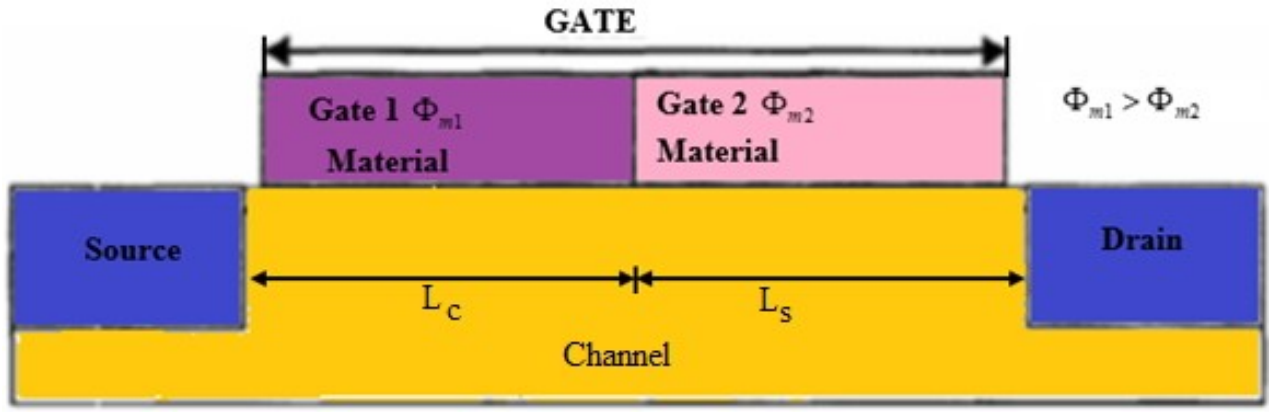


Figure 1. 8. Illustrates double material gate (DMG) MOSFET structure [69].

An accelerating force is provided for charge carriers in the channel by the difference in work function of the double material gate between the two laterally contacting gate materials of lengths L_C and L_S. This difference also serves as a screening effect, which helps suppress SCEs.

One of the gate materials serves as a control gate with metal work-function ϕ_{M1} and the other as a screening gate with work-function ϕ_{M2} which should be less than ϕ_{M1} [37]. For improved carrier transport efficiency and a higher drain current, screening the control gate from drain potential changes reduces the hot electron effect by lowering the electric field [45].

1.4.2.1 Need for Metal Gates in MOSFET

a) Poly-Si gate depletion effect

At shorter gate lengths, the poly-Si gate depletion that is produced by weakly doping the poly-Si gate adds a poly gate depletion capacitance (C_{PD}), which is connected in series with the oxide capacitance (C_{OX}). When the devices are turned on, this results in a decrease in the total gate capacitance (C_g), which is caused by the existence of gate depletion [70]. This lowers the inversion charge density by raising the threshold voltage (V_{th}), which, in the occurrence of potential decreases, causes drain current depletion effects at the gate sidewalls due to fringing gate fields [29]. Therefore, devices with dimensions less than 70 nm can't use poly-Si gates [45].

b) Compatibility with high-κ gate dielectrics

Employing a high-dielectric material in conjunction with a poly-Si gate does not lend itself well to high-performance logic applications. This is due to the fact that the high-/poly-Si transistors that result from this combination have a high V_{th}, which leads to a reduction in channel mobility and, as a result, poor drive current performance [45]. Surface scattering due to high concentrations of interface charges is the principal source of channel mobility degradation in high-dielectric poly-Si gate devices. Phonon scattering due to soft optical phonons influences mobility in high-poly-Si gate devices [71]. Metal gate electrodes are able to effectively prevent phonon scattering in high-dielectrics from connecting to the channel when the device is operating in inversion conditions [71]. This is because the electric dipoles in the oscillating gate plasma and high-gate dielectrics cancel each other out, resulting in weaker coupling between high-phonons and carriers in the Si channel [71]. Therefore, the appropriate transistor threshold voltage (V_{th}) can be provided by a metal gate with work function optimizations to reduce mobility degradation. This will make it possible for future logic applications to achieve excellent performance while maintaining low gate leakages. Therefore, high-performance and low-power MOS applications in the 45 nm node and beyond will necessitate metal gate electrodes with high-dielectrics gate oxide [45].

c) High gate resistance

For a short-channel CMOS device, the performance limitations of high gate resistance are most apparent in the cut-off frequency and maximum oscillation frequency [72]. On the other hand, metal gates have a lower sheet resistance; as a result, current MOS devices use stacked gate electrodes with silicide (metal plus poly-Si) to minimize gate resistance [45]. The gate resistance of a MOSFET can impact its performance in several ways. Here are some of the potential impacts:

Delay: MOSFETs with high gate resistance can experience a delay in their turn-on and turn-off times. This can be particularly problematic in applications where fast switching speeds are required.

Power loss: High gate resistance can result in power loss due to the additional energy required to charge and discharge the gate capacitance. This can increase the MOSFET's on-state resistance, leading to higher power dissipation.

Reliability: MOSFETs with high gate resistance can also experience reliability issues. This is because the gate oxide layer can be damaged if the gate voltage is not applied properly. If the gate resistance is too high, the gate voltage may not be applied correctly, leading to oxide breakdown and eventual device failure.

Noise sensitivity: High gate resistance can make MOSFETs more susceptible to noise, which can interfere with the gate voltage and cause the device to malfunction.

Therefore, choosing MOSFETs with appropriate gate resistances for a given application is crucial to avoid these issues. The gate resistance can be controlled by selecting MOSFETs with suitable gate geometries and electrodes by designing the gate driver circuit to provide adequate gate drive current.

d) Fluctuations of V_{th} for thin body devices

Since the depletion charge density in the ultra-thin body (UTB) silicon oxide insulator (SOI) devices with lightly doped bodies are insufficiently low to have an impact on the threshold voltage (V_{th}), V_{th} must be controlled by the metal gate work function alone [73]. Consequently, there has been a significant uptick in interest in switching traditional poly-Si gates for metal gates [37]. The threshold voltage of these thin-body devices is proportional to the Si film's thickness [74]. However, in the case of ultra-thin body devices with body thicknesses of less than 10 nm, it is not simple to keep the uniformity of the Si film across the wafer [75]. The decrease in mobility and overall performance that results from increasing the amount of body doping used to control V_{th}. Therefore, in order to attain the performance improvements associated with UTB devices, it is necessary for the V_{th} of the thin-film device to be controlled by the metal gate work function alone [76].

1.4.3 Junctionless Transistor (Gated Resistor)

As we have stated earlier, with the advancement of MOS technology, scaling conventional MOSFETs has created difficulties in fabricating short-channel MOSFETs[75], [77], [78] due to existence of source-channel-drain pn junctions[79]. This pn junction either allows current to flow through it or prevents it from doing so, depending on the gate bias voltage[80]. Recently, Junctionless (JL) MOSFETs have been proposed as a potential solution to this problem[81] since it has uniform doping from the source to drain through the channel, simplifies the fabrication steps of MOSFETs by improving the device's switching (I_{ON}/I_{OFF}) ratio[82]–[84]. Furthermore, manufacturing JL-MOSFETs is more straightforward because homogeneous

doping eliminates the need for a large thermal budget[85]. These characteristics of JL MOSFETs are advantageous for fabrication sensor devices [67]. There is no pn junction in the source-channel drain path of a junctionless transistor (JLT), as shown in **Figure 1. 9.**

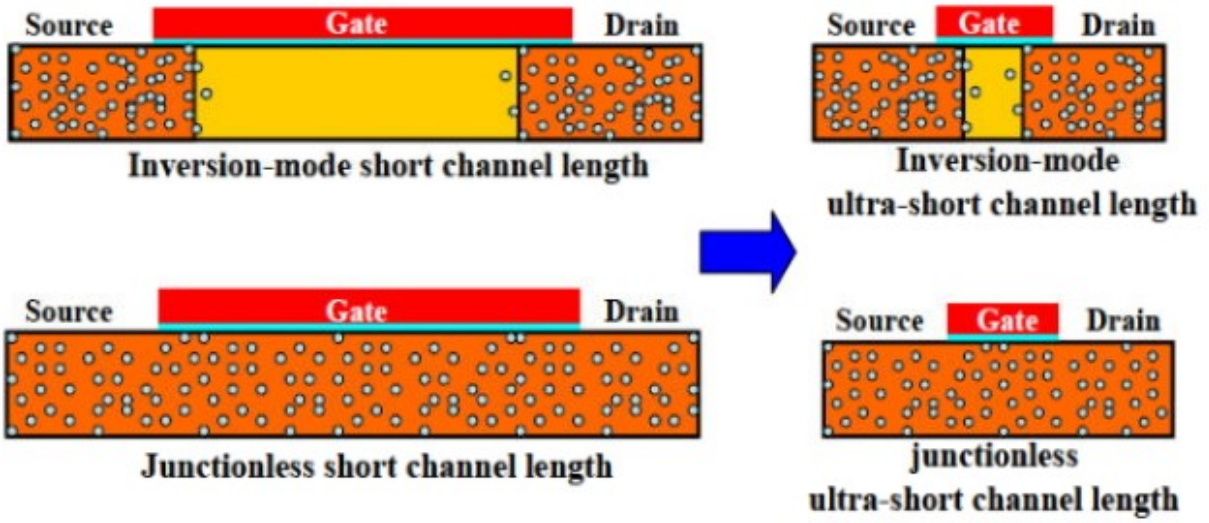


Figure 1. 9. Depicts inversion-mode and junctionless transistor for source and drain doping in small dimension short channel device[86].

The junctionless transistor is essentially a very thin silicon (~5-10 nm) accumulation mode device. Junctionless transistor, also known as a "gated resistor" or a "nanowire pinch-off FET," is highly doped (typically between $8x10^{18}$ cm^{-3} and $8x10^{19}$ cm^{-3}) in order to have an acceptable drain current[75], [78], [80]. Compared to traditional MOSFETs, JLTs have many benefits, including higher scalability and improved performance (less drain-induced barrier lowering (DIBL) and subthreshold slope [SS] degradation), lower sensitivity to doping fluctuations, and lower negative bias thermal instability[87]. A junctionless transistor eliminates the subsequent annealing process due to uniform and homogeneous doping in the channel region, allowing the device to be fabricated with shorter channel lengths, and it provides low standby power and low gate-induced drain leakage[80], [88], [89]. In part, increased mobility in junctionless MOSFETs can be attributed to the fact that the vertical electric field in a JLT is much lower than in a junction-based MOSFET MOSFET[90]. Unlike a junction-based device, the OFF-state current in a junctionless transistor is entirely determined by electrostatic control of the gate[91]. Theoretically, junctionless transistors have been studied with single, double, triple, and gate-all-around architectures[24].

However, besides the numerous advantages mentioned above, JLT has some drawbacks. Due to high doping concentration (N_D) in the channel region, JLT has a lower ON-state current (I_D) and transconductance (G_m) than IM MOSFETs[84]. For non-planar structures, it is also extremely challenging and expensive to have a highly doped uniform channel of such a thin thickness (~5-10 nm) s[75]. The threshold voltage varies with doping concentration and nanowire width [75], [92]. This is because a higher channel doping concentration leads to a higher ON-state current. Therefore, a solution to the difficulties associated with deep submicron transistor scaling cannot consist of either uniform doping or a junctionless transistor.

1.4.4 Latest Device Structures Proposed to Overcome Short Channel Effects.

Continuous scaling of semiconductors has reduced the device's size, improving the device's performance and speed of operation[84]. But beyond 45 nm technology, the short channel effects will rise and degrade the performances of the MOSFETs[7], [85]. To overcome these challenges, the engineers have designed new device structures, such as mullite gates and cylindrical gate transistors, and efforts are being made to enhance these devices' performance[84], [86]. In multi-gate structures [85], the electrostatics is enhanced because the gate influences the channel potential from different directions, minimizing the requirement for doping.

Figure 1. 10 shows the development of multiple-gate transistors, with the order of development corresponding to the degree of gate electrostatic control. In this section, some device structures and applications have been mentioned.

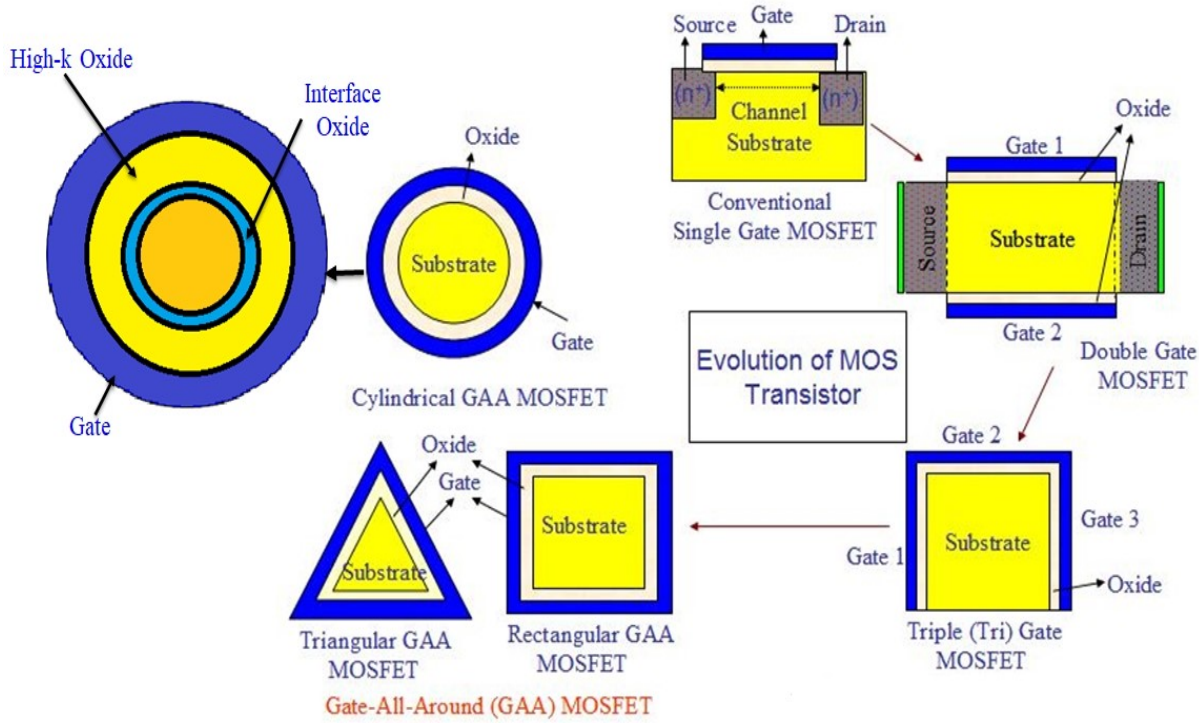


Figure 1. 10. Illustrates the development of the device architecture from the single-gated planar to the fully GAA NWMOSFETs[85], [87].

1.4.4.1 Silicon on Insulator (SOI) MOSFET

Silicon-on-insulator (SOI) technology in semiconductor manufacturing is the fabrication of silicon semiconductor devices in a layered silicon-insulator-silicon substrate to reduce parasitic capacitance within the device and hence improve performance[41], [88]. Silicon-on-insulator (SOI) MOSFETs are one example of a non-classical device that has emerged as a result of the limits of bulk-CMOS scaling as shown in **Figure 1. 11(a)**3-D structure and **(b)** cross-sectional

view. These devices are interesting for high-speed VLSI applications requiring low power consumption due to their low parasitic capacitance. The lack of wells in SOI technology is largely responsible for this highly dense structure[85]. SOI CMOS devices, on the other hand, can be isolated through reach-through oxidation, in contrast to bulk devices, which frequently depend on junction isolation. Dielectric isolation between devices is used in SOI CMOS technology. Because of this separation, the parasitic junction capacitance is minimized.

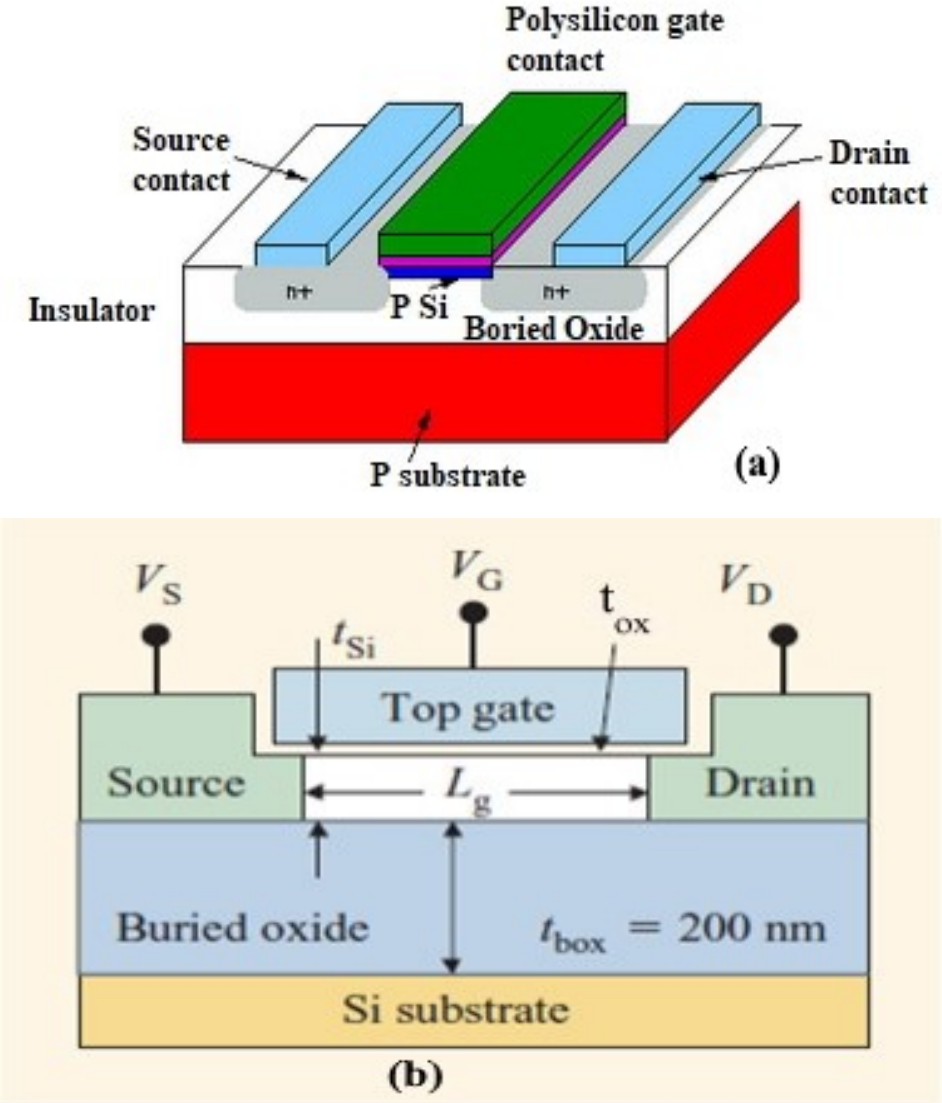


Figure 1. 11. Illustrates SOI MOSFET **(a)** 3-D view and **(b)** 2-D schematic structure [85].

Figure 1. 12(a) depicts the parasitic junction capacitance in a bulk CMOS device. This capacitance has two parts: the drain-to-substrate capacitance and the drain-to-channel-stop-implant capacitance, both of which lie beneath the field oxide. High substrate doping is required to counteract short-channel effects as the device scales down to the nanometer range [89]. This raises the junction's parasitic capacitance. The parasitic capacitance between the junction and substrate in the SOI CMOS devices depicted in **Figure 1. 12 (b)** is much reduced than its corresponding equivalent item in a bulk device. With less parasitic junction capacitance, SOI CMOS circuits are able to achieve their high-speed performance [85], [90].

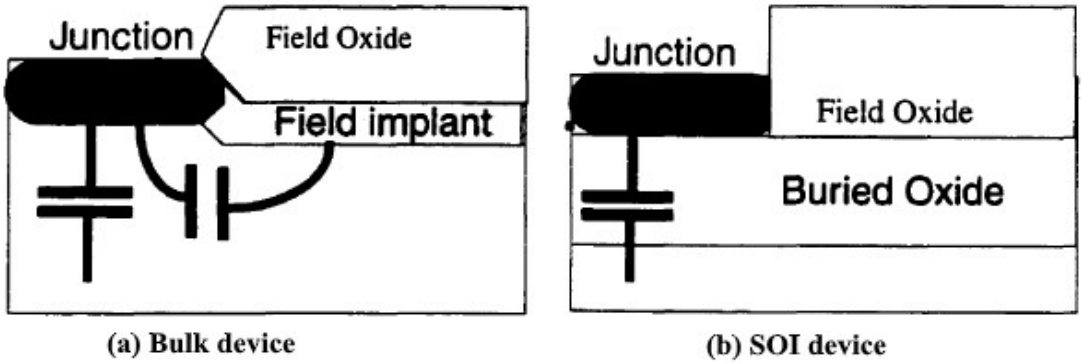


Figure 1. 12. Depicts parasitic junction capacitances in bulk and SOI MOSFETs [89].

It's important that the channel length (L_{Ch}) isn't too short during the scaling. The reason for this is that as L_{Ch} gets shorter, so does threshold voltage (V_{th}) [91]. In the manufacturing facility, it undergoes extensive inspection[85]. Instead, the lateral diffusion of the source and drain junctions makes it difficult to precisely calculate the channel length. Doping the bodies of short-channel devices more heavily than long-channel devices allows for the possibility of increasing their threshold voltage, which is denoted by the notation V_{th}.

Figure 1. 13 shows the schematic two-capacitor network in MOSFET [91]. We can see the first capacitor, C_G, between the gate and the channel, and the second capacitor, C_D, between the drain and the channel, both of which end in the channel's middle. Capacitance C_D denotes the drain-to-channel barrier point capacitively coupled region. A capacitive coupling takes place between the channel barrier point and the drain, and the capacitor denoted by the symbol represents this C_D. Because the distance from the drain to the "channel" is also reduced when the length of the channel is shortened, the amount of C_D that is produced as a result is greater [91]. To mitigate the negative effects of the short-channel effect, it is highly recommended that the doping level in the channel region be raised. Because of this, C_D goes up, which ultimately leads to an increase in the inverse subthreshold slope[85], [89], [91]. It is important to remember that the capacitance will rise when the two electrodes are brought closer to each other.

In general, the characteristic length (l_D) must be reduced in proportion to channel length as we advance to successively more advanced technological nodes. This means that we must minimize oxide thickness (T_{OX}), width depth (W_{dep}), and drain junction depth (X_i). Because of this, lowering T_{OX} leads to an increase in gate control, also known as ((C_{oxe}). By reducing X_i, C_D can be brought down to a lower value by decreasing the size of the drain electrode. C_D is also decreased when W_{dep} is reduced because this results in introducing a ground plane, either the substrate's neutral region or the bottom of the depletion zone. This ground plane tends to electrostatically protect the channel from the drain.

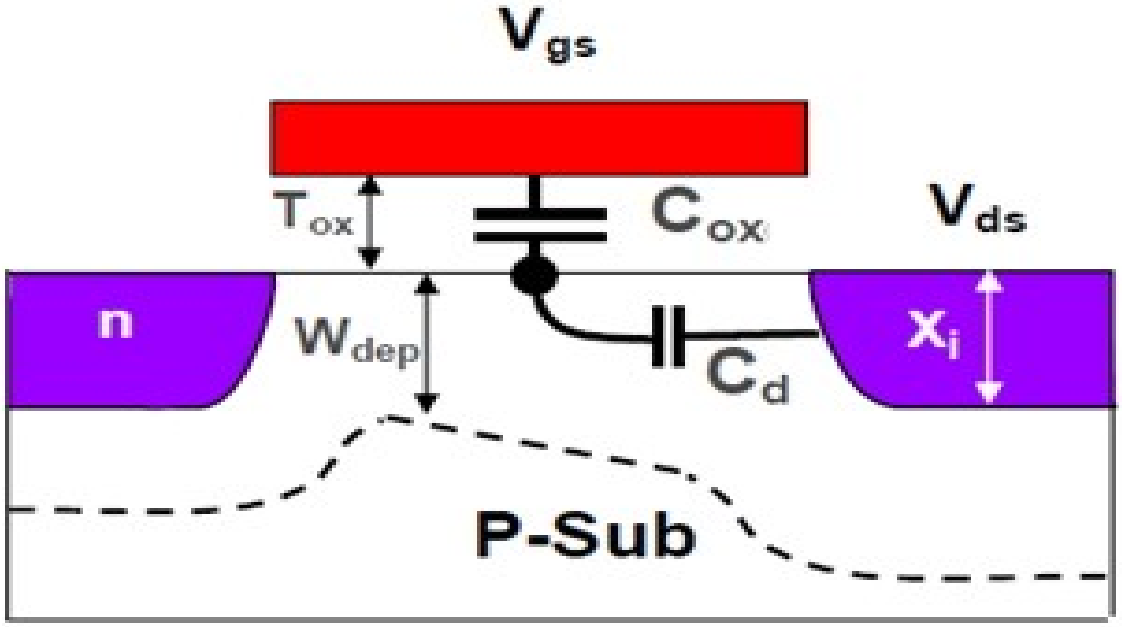


Figure 1. 13. Schematic of the two-capacitor network in MOSFET [89].

The occurrence of buried oxide reduces not only the junction's capacitance but also the capacitance of other parasitic connections, such as the ones that exist between the silicon substrate and the various ends [89]. If the thickness of the silicon film (t_{Si}), is greater than the substantial inversion depletion width, the channel area will be partially depleted even though the device will continue to function normally. This is a partially depleted (PD) SOI device[89]. If t_{Si} is less than the depletion width, the channel region under the inverting layer will be completely depleted during device operation. Compared to bulk Si CMOS, the short-channel effects in partially depleted SOI structures are less severe. Consequently, the inverse subthreshold slope can be improved while the impacts of short channels are reduced by optimizing the channel's doping profile. The channel region is completely depleted in a thin film SOI device. This causes the PD SOI MOSFET's inverse subthreshold slope to reach the optimal value of 60 mV/decade. Because it permits the use of devices with a lower level of threshold voltage without an increase in the amount of leakage current that those devices may produce, a reduced inverse subthreshold slope is highly desirable for low-power consumption and low-voltage applications. This is because it enables the use of devices with a lower level of subthreshold slope.

When the control of the gate over the channel region is modified by electric field lines coming from the source and drain, this phenomenon causes short-channel effects [91]. Electric field lines go via the depletion zones associated with the junctions when a bulk device is being considered [89].

Increasing the amount of doping in the channel area can minimize their negative influences. Before reaching the channel region, nearly all of the field lines in a completely depleted SOI device first pass through the buried oxide, also known as the BOX [85], [89], [91]. Generally, SOI CMOS device performance is accepted to be better than that of its bulk counterpart.

However, the existence of the BOX layer, on the other hand, causes self-heating and floating body effects [89]. Self-heating occurs because the buried insulator prevents heat transfer between the transistors and the substrate.

As a consequence of this, the disposal of surplus heat that is produced within SOI devices is less efficient than it is within bulk devices. This might lead to a significant increase in the device's temperature. However, the impacts of self-heating are far less problematic in low-power applications because the design minimizes the amount of power that is consumed. The silicon film under the channel region of an SOI MOSFET is electrically floating [90]. A neutral region occurs with partially depleted SOI NMOS devices, introducing a potential barrier between the source and drain. The floating body causes various parasitic effects, including the kink effect [89], [90]. Increases in the drain to source voltage (V_{DS}) cause an increase in the impact ionization that produces electron-hole pairs. In this setup, electrons can freely travel to the drain region, while holes can move to the floating body with low potential. Because of the presence of the buried oxide layer, holes cannot be extracted through the substrate and are trapped in the neutral region. The accumulation of holes causes a rise in potential in bulk, which, in turn, causes a fall in the threshold voltage of the material. On the other hand, one can see a kink (also known as a curve) in the saturation region. The holes that are created as a result of impact ionization in bulk MOSFETs are transported to the substrate in the form of a current that flows through the bulk MOSFET. On the other hand, holes caused due to impact ionization are confined to the neutral region in the SOI structure.

Overall, the device's functionality and performance suffer due to the existence of the floating body. These effects may be traced back to their underlying causes, which include the capacitive coupling between the gate and the floating body and the charging and discharging of the floating body that occurs due to currents flowing from the source or drain.

1.4.4.2 Double Gate (DG) MOSFET

A metal-oxide-semiconductor field-effect transistor, also known as a MOSFET, with two gates rather than one is referred to as a double gate or double gate MOSFET. The current flow through the transistor may be controlled more precisely because the gates are located on both sides of the channel. In the early 1980s, [92] researchers introduced the double-gate FET (DG FET), as depicted in **Figure 1. 14**. The channel in a planar Double Gate (DG) MOSFET is sandwiched between two independently fabricated gates. As illustrated in **Figure 1. 14 (a)** and **(b)**, DG MOSFETs can be configured in two ways: asymmetric DG MOSFETs and symmetric DG MOSFETs, respectively. The two oxides in asymmetrical DG MOSFET have different thicknesses, and the gates are biased independently of one another. DG MOSFETs allow improved control over the transistor's threshold voltage and the voltage at which it conducts. DG MOSFET threshold voltages are affected by both gates, unlike ordinary MOSFETs. DG MOSFETs operate at lower voltages and use less power, making them desirable for low-power applications.

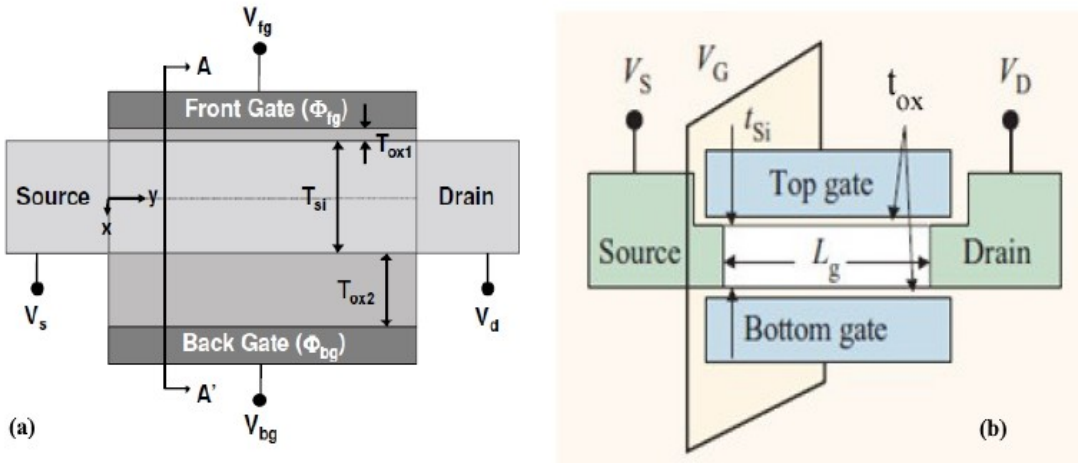


Figure 1. 14. Structure of **(a)** Asymmetric, **(b)** Symmetric Double gate MOSFET [92].

The basic premise behind a Double Gate MOSFET is to efficiently manage the Si channel by using a tiny channel width and providing a gate contact on both sides. This idea helps to reduce the impact of short-channel effects and results in larger currents than those achievable with a single-gate MOSFET [90]. Due to the gate's ability to shield the channel on both sides, DG MOSFETs are significantly more robust to electrostatic forces than their single-gated counterparts. This is because the field from the gate is not able to penetrate as deeply, and short-channel effects are minimized[85], [90]. When a fully depleted SOI device is placed between two coupled gate electrodes, one can considerably limit the effects of short-channeling [90]. When using this design, improved control of the channel depletion zone can be achieved in contrast to a "regular" SOI MOSFET. This can be done because a different region controls the channel depletion region. The short-channel effect is also greatly diminished since the drain electric field has such little impact on the channel. The symmetrical version of the DG MOSFET is said to be further improved by better channel mobility compared to that of a bulk MOSFET, in accordance with the universal mobility model [93], [94]. This is because dispersion due to interface roughness is reduced. After all, the average electric field in the channel is decreased. Overall, the DG MOSFET is a promising technology for enhancing electronic device performance and efficiency, particularly in low-power applications.

1.4.4.3 Triple Gate (TG) MOSFET

As the need for higher current drive and improved short-channel characteristics (double-, triple-, or quadruple-gate devices) grows, Silicon-on-insulator (SOI) MOS transistors are shifting from conventional, single-gate devices to three-dimensional, multi-gate devices [95]. This happens because typical SOI MOS transistors are single-gate devices, and conventional SOI MOS transistors are planar devices. It has been speculated that multi-gate Metal Oxide Semiconductor Field Effect Transistors, also known as MGMOSFETs, would be a viable solution and an appropriate choice for CMOS devices utilizing nanoscale technology [96][97]. This is because of their high output resistance, low leakage current, robust driving controllability, and excellent immunity to short-channel effects (SCEs). A new type of

MOSFET known as a Triple-Gate (TG) MOSFET is introduced along with its development and characteristics. Triple Gate (TG) MOSFETs are a unique form of MOSFET that has three gate terminals rather than the standard MOSFET's single terminal. Compared to traditional MOSFETs, this design has various advantages, including better control over electron flow, lower leakage current, and faster operating speeds. TG MOSFETs have three gates separated by thin insulating layers, each controlling a different channel region. The device's electrical characteristics can be precisely controlled by tuning the channel's electric field with gate voltages. The introduction of CMOS technology at the nanoscale scale necessitates a new approach to overcome a wide range of short-channel effects (SCEs) [95], [96], [98]. The triple-gate (TG) MOSFET is characterized by its high trans-conductance, attractive sub-threshold factor, and superior ability to suppress the short-channel effect (SCE) [96], [98]. The triple-gate MOSFET is distinguished by its high transconductance, excellent subthreshold factor, and superior immunity to the adverse effects caused by the short-channel effect (SCE) [86], [99], [100].

Additionally, this MOSFET has three gates instead of two. Scaling a MOSFET using a single gate, also known as SG MOSFET, is the best option for overcoming biassed short-channel effects (SCEs) and, as a result, improving the device's dependability [96]. This is because of the increasing speed at which technology is developing and being applied[98]. Due to an increase in charge sharing from source to drain, the threshold voltage becomes less under the control of the gate voltage as the channel length decreases. While providing protection from SCEs [95], [96], it is crucial to account for the significant effects of drain-induced barrier lowering (DIBL), where the length of the channel shortens as the threshold voltage decreases. It was suggested that triple-gate (TG) MOSFETs be used to enhance the exemption to a level comparable to that of SCEs. These MOSFETs have a thin gate insulator and a gate on each of the three sides of the channel, as shown in **Figure 1. 15** [98].

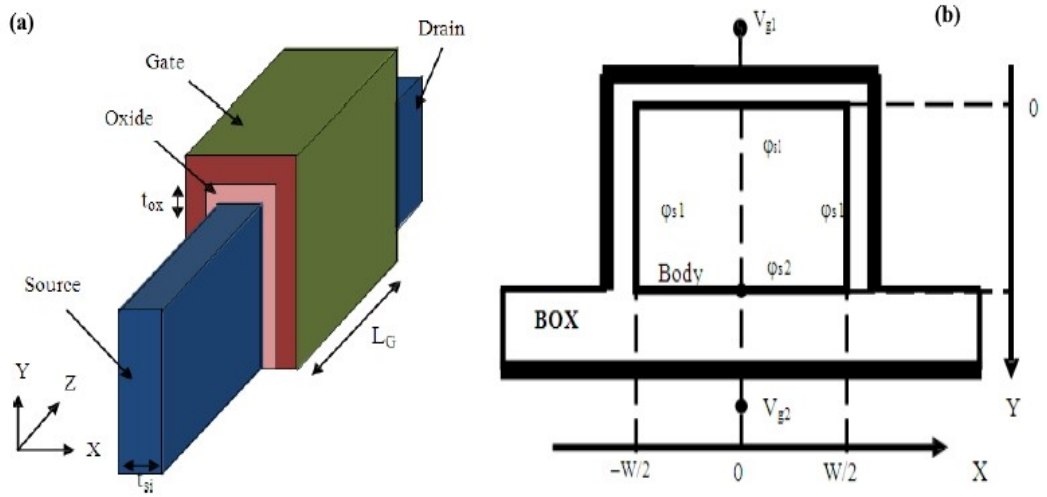


Figure 1. 15. Illustrates basic (a) 3D structure model, (b) cross-sectional view of Triple Gate SOI MOSFET[98].

Very-large-scale integration (VLSI) is expected to extensively use triple-gate MOSFETs in the near future, particularly for reduced power and high performance at 45 nm CMOS Technology

[95]. The gates of a triple-gate MOSFET wrap around the silicon body, making it a non-planar narrow transistor. The gates regulate the top horizontal channel and both lateral channels. The film is made up of a long, thin island of silicon that has gates on three sides. In instances where a transistor's base is completely depleted, the triple gate transistor emerges. A thin semiconductor body is created on a substrate to form the triple gate MOSFET. Misalignment of the top and bottom gates in a DG MOSFET arrangement causes parasitic capacitance; therefore, correcting it is essential. Like FinFET's self-aligned triple gate arrangement, a triple gate solves this issue[95]. TM MOSFETs' high voltage and high current handling capacities may also find use in power electronics and other industries. **Figure 1. 15 (b)** depicts the cross-sectional view of n-channel triple-gate MOSFETs, which represents the current flow direction that is perpendicular to the axis, and this is used to model parameters like surface potential, threshold Voltage, and Electric field.

Generally, Short-channel effects (SCEs) are mitigated in Triple gate (TG) MOSFETs compared to the Double-gate (DG) MOSFET design. The electric field, DIBL, and drain conductance are all lowered in a Triple-gate (TG) MOSFET compared to a Double-gate (DG) MOSFET, while trans-conductance, surface potential, voltage gain, and drain current are all improved [95], [101]. However, TG MOSFETs are still in their early stages; therefore, they aren't commonly employed in production items yet. The future of this technology is exciting because of the ongoing research in this field.

1.4.4.4 Gate All Around (GAA) NWFET

From many types of multi-gate device structures of the transistor, a Cylindrical gate transistor has emerged in which the semiconductor nanowire channel is wholly surrounded by the metal gate [84], [102]. This section discusses an overview of the modelling approach and short-channel behavior of a cylindrical GAA JL NWFET. In most devices, short channel effects and hot carriers increase when the design scale goes below 22nm technology node [7], [103]. The Gate All Around (GAA) structure is regarded as being among the most effective multiple gate structures because it demonstrates improved gate controllability, decreased floating body effects, and excellent CMOS compatibility [104], [105]. Because the transistor channel in a GAA NWFET is a nanowire surrounded by gate electrodes on all sides, this type of device is referred to as having a "Gate All Around." Compared to other types of transistors, this design enables greater control over the direction in which the current flows through the transistor, as well as less leakage and enhanced performance. The GAA NWFET's main advantage is high packing density for vertical structures and excellent electrostatic integrity even at the nanoscale. Still, its main disadvantage is low current-carrying capability per device. Silicon nanowires have been successfully used as the basis for gate-all-around NWFETs[106]. The top-down fabricated, gate-all-around architecture that makes use of a Si nanowire channel appears to have promise for upcoming generations of technological advancement. The gate-all-around architecture enhances electrostatic control, which, in turn, increases the gate length's scalability.

Furthermore, it allows for the use of an undoped channel, which has the potential to reduce threshold voltage variation due to lower random dopant fluctuations. GAA NWFETs with

cylindrical gate geometry are among the best candidates for improving the device's scalability. Energy efficiency, speed, and performance are all areas where the GAA NWFET shows promise for the future of electronics. However, it has not yet seen widespread adoption in commercial devices and is still in development.

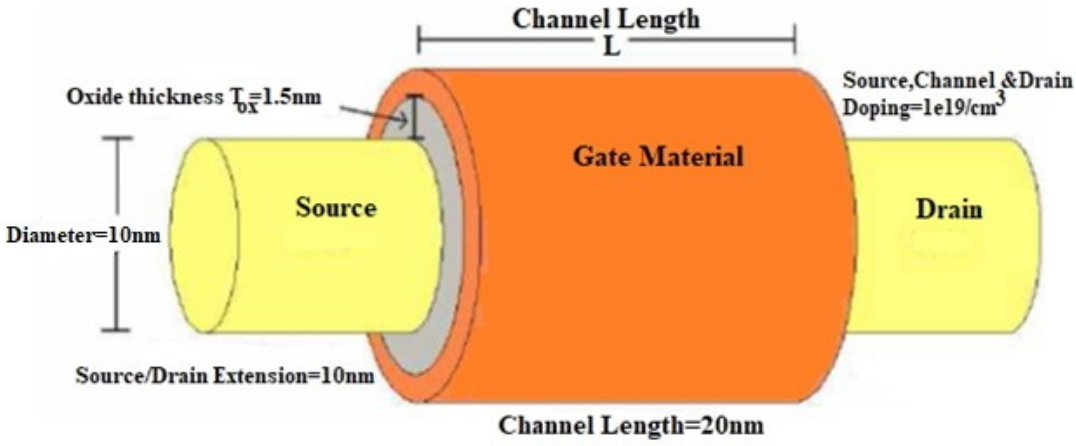


Figure 1. 16. Illustrates 3D schematic structure of a cylindrical JL GAA-SiNWFET[107].

Recent developments in semiconductor technology have allowed us to study alternate techniques for fabricating transistors, enabling us to lower the size of transistors and increase their performance [71]. The development of p-type and n-type areas in conventional transistors is carried out by doping atoms onto a silicon substrate. This results in the formation of semiconductor junctions. When the size of such transistors is decreased to the lower end of the nanoscale scale, the junctions become increasingly near, which makes the process significantly more challenging because it requires highly high gradients in the doping concentration [72]. Implementing junctionless transistors is one of the most promising ways to solve this problem[71], [107]. Since the first junctionless device was fabricated in 2010[108], numerous other transistors of this type, including FinFET, Thin Film, and Gate-All-Around, have been proposed and studied[71], [108]. In the Gate-All-Around transistor, the gate electrode surrounds the transistor channel, which might have a cylindrical or rectangular form. Gate-all-around JL FET geometry improves electrostatic control and, as a result, gate length scalability[11], while rectangular gate-all-around FET suffers from performance degradation due to corner effects[109]. The junctionless Gate-All-Around field effect transistor shown in **Figure 1. 16** is cylindrical. The complexity of the equations used to represent the device's behaviour is determined, in part, by the channel geometry [71]. Since cylindrical coordinates are introduced, the solutions to the Poisson equations become more involved[73]. The channel length is an important design element that must be considered when creating cylindrical GAAFETs. When the channel length is reduced from 40 to 16 nm, the DIBL rises from 12 mV/V to 123 mV/V, and the SS rises from 62 to 82 mV/dec [71]. The hot carrier effect was also observed to degrade the intrinsic gain of cylindrical GAA JL NWFET when SiO_2 oxide thickness is ≤2nm[103]. Threshold voltage roll-off was investigated for cylindrical gate-all-around junctionless transistors (GAA JLFET) [110] under extremely reduced gate oxide (SiO_2) thickness (below 1.2 nm), and the findings demonstrated that the gate oxide tunnelling current

[111] is caused by electrons tunnelling through the oxide layer between the substrate and the gate under the influence of an applied electric field.

1.5 Device Simulation

Device simulation is an integral part of device design. It provides quick feedback on device design before the lengthy and costly fabrication process[112]–[115]. Discrete device simulators, like SILVACO-ATLAS TCAD (Technology Computed Aided Design), employ a grid on a 2D surface or 3D volume to solve each point using a partial differential equation solver[115]. It provides insight into the internal physical principles connected with device operation while predicting the electrical behavior of specified semiconductor architectures [115]. Nonlinear difference equations are solved using iteration techniques such as the Newton-Raphson Method. "Terminal currents, voltages, and charges are calculated using physical device equations such as Poisson's (relates variations in the electrostatic potential to local charge densities) and the Continuity equations(provide an account of the changes in electron and hole densities caused by transport, generation, and recombination)" [116]. Parameters like temperature, pressure, and others can be altered in a device simulator, in addition to many different types of materials available[117]. The variability of models, such as carrier statistics and current continuity, appears to be limitless. SILVACO-ATLAS TCAD's 3-D device simulator was used in this thesis. It provides for predicting electrical behavior for predefined semiconductor architectures and elucidates the fundamental physical mechanisms of device operation. ATLAS has several potential applications independently and as a central component of SILVACO's VIRTUAL simulation. Device simulation follows process simulation and SPICE model extraction for estimating process factors' effect on circuit performance[115]. **Figure 1. 17** below summarizes ATLAS "command groups with the primary statements in each group during device simulation" from structure specification to parameter extraction. Failure to do so usually results in an error message, program termination, and incorrect program operation[115].

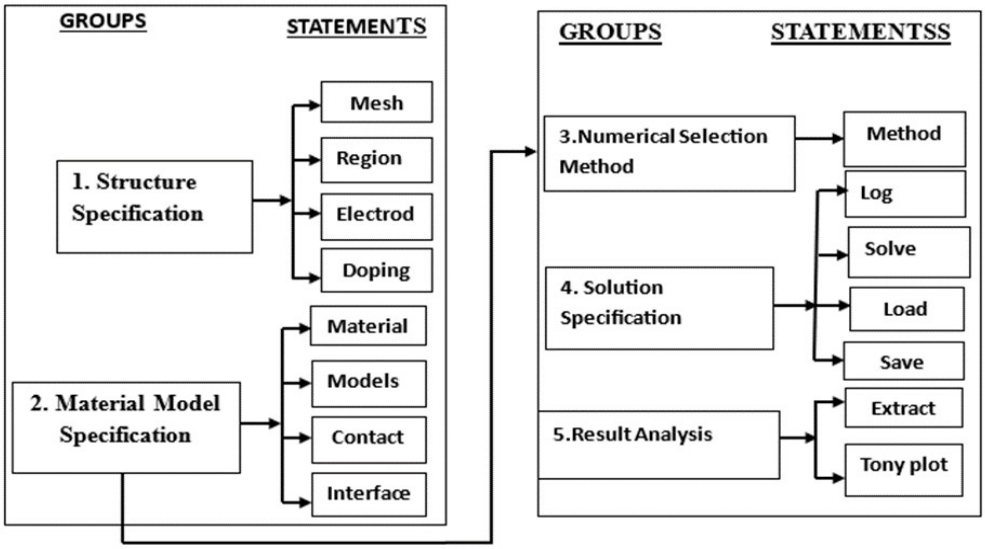


Figure 1. 17. Illustrates the basic flow chart applied during the proposed device simulation [115].

The MODELS statement contains descriptions of all models available, with the exception of impact ionization. The IMPACT statement specifies impact ionization.

Table 1. 2: Shows different models available in ATLAS to model various physical phenomenal [115].

Category	**Models Available**
Mobility	Concentration-dependent mobility (Arora model, Analytic, Standard), Surface scattering mobility model, Carrier-Carrier scattering model, electric field dependent mobility model, Lombardi (CVT) model.
Recombination	Auger recombination model, Shockley-Read-Hall (SRH) recombination model with fixed lifetime, SRH recombination model with concentration-dependent lifetime.
Tunnelling	Models of direct quantum tunnelling, hot carrier injection, and band-to-band tunnelling were addressed.
Impact ionization	Selberherr model, Crowell and Sze model, and Grant's model.
Energy transport	Energy balance and hydrodynamic model.

To have an accurate simulation of the device, all of the essential and relevant models that are required to describe its physical properties should be included. The thesis organization is described next to the objectives of the thesis.

1.6 Research Gaps

- We chose Junctionless gate-all-around architecture in this thesis because a metal gate wholly warps its channel, has reasonable gate control of tunnelling current in the channel region, and has excellent scalability among the various FET architectures reported, namely, bulk planer, single-gate, double-gate, triple-gate, and gate-all-around FET. Since most junctionless transistor research has focused on analog and digital applications, this thesis focuses on sensing applications. The sensitivity of proposed device performance parameters was examined using extensive device simulations with SILVACO TCAD and compared to conventional counterparts.

- The major problem faced by GAAFET is the ambipolar diffusion/ current[104], [105], which is conduction in the opposite direction (consisting of both electrons and positive ions moving in the opposite direction) or switching the device in a reverse bias state. Ambipolarity results in unsuitability for digital switching applications because it is not on- or off-state (it has a detrimental effect on the device operation in both the on- and off-state)[106]. Therefore, the impact of ambipolar behavior on the technological device performance should be parameterized quantitatively and has been evaluated as a function of the device structure[107] to enhance device on-current. So in this work, ambipolarity

has been minimized by introducing novel device structures and gate (engineering) optimization techniques.

- Further study on improving the On-current (I_{ON}) and device performance in the silicon nanowire transistor bio-sensor using different materials and structures has been studied experimentally[80]. However, the nanowire itself suffers from a worse situation of leakage current due to its size scaling down under the nanosized regime[108], [109]. Therefore, the overall optimization of the silicon nanowire transistor is highly desired for sensing applications[110], [111], including device consistency, subthreshold swing (SS), OFF-current (I_{OFF}), ON-current (I_{ON}), and drain-induced barrier lowering (DIBL) effects. So, in this work, we have developed a nanowire GS_GAAJLT to address and solve problems related to gate-induced drain leakage current, SCE, and band-to-band tunnelling (BTBT) using high-k dielectric materials as gate oxide materials and a gate electrode. High-k gate dielectrics are used in modern technology in order to prevent leakage currents from flowing through gates with extremely thin oxide layers. The effect of fringing fields emanating(arising) from high-k gate dielectrics on device sensitivity performance was investigated. A hybrid metal gate-electrode technique (different gate electrodes on the source and drain sides) is used to mitigate the negative impact of fringing fields on device performance. Analytical models that are valid from subthreshold to accumulation regions are rare for shorter-channel Gate stack GAA JL FETs. The channel potential and drain current models of a Gate stack GAA JL FET with a shorter channel length are developed. The threshold voltage and drain-induced barrier-lowering values are extracted. The SILVACO-TCAD simulator [112] provides overviews of probable manufacturing procedures for gate stack GAA JL FETs.

1.7 Objectives of the Study

Throughout the duration of the thesis, it was proposed that improved methods should be developed to address the fundamental aspects that minimize the impacts of the short channel effect on the GAAJLNWFET when it is used in sensing applications. The following is a summary of the objectives that were proposed as potential solutions to the problem statements.

A) Developing gate stack junctionless gate all around nanowire field effect transistor for hydrogen gas sensing application.
B) Investigating hybrid gate stack junctionless gate all around nanowire field effect transistor for biomedical sensing application.
C) Examine the impacts of interface trap (localized) charges on the junctionless gate all around silicon nanowire field effect transistor, including biomolecule species on the cavity region.
D) Modelling and analyzing the impact of hybrid gate electrodes on gate stack junctionless gate all around nanowire field effect transistor sensitivity using different biomolecules.

1.8 Organization of the Thesis

This thesis is divided into six chapters so that it may accommodate the effort of doing research. Each chapter has been organized so that it may stand on its own, for the most part. This thesis has a separate summary and reference list at the end of each chapter.

Chapter-1 presents the fundamental introduction to the research work done, including the historical background of earlier work done in the field of modeling and simulation of MOSFETs and their reliability difficulties. The chapter's first section reviews MOSFET fundamentals, scaling challenges, and short-channel effects. The chapter progresses to the requirement for advanced MOSFET architectures such as GAA JL MOSFET for additional scaling and immunity to short-channel effects. Furthermore, the significance and features of the study are provided in this dissertation and include a summary of the thesis contributions.

Chapter-2 demonstrates the capability of junctionless metal gate GAA NWFET-based hydrogen gas sensors for various sensing applications. Nanowire MOSFET or GAA MOSFET is the ultimate choice for sensor applications because of its small size and large surface-to-volume ratio. Analytical model is validated with simulated results using ATLAS device simulator. An analytical model is built to simulate the response of junctionless GAA NWFET with respect to variations in the catalytic metal gate work function (palladium) and temperature value changes. This model is then confirmed with the simulation results obtained using ATLAS-3D device simulator. The junctionless metal gate GAA NWFET hydrogen gas sensor sensitivity is compared with bulk MOSFET and GAA MOSFET gas sensors based on subthreshold current and threshold voltage sensitivity parameters, enabling low power operation with high sensitivity.

Chapter-3 Emphasis on increasing the biosensor's sensitivity by immobilizing biomolecules in nano-cavities inside a dielectric-modulated, triple-metal-gate-all-around-junctionless NWFET device. Nanowire MOSFET or GAA MOSFET is the ultimate choice for sensor applications because of its small size and large surface-to-volume ratio. A new junctionless high-k GAA NWFET biosensor with vacuum gate dielectric is proposed for enhanced sensitivity of label-free detection neutral biomolecules. A comparative analysis of dielectric modulated triple metal gate all around junctionless nanowire field-effect transistor biosensor has been carried out with double metal gate transistor and existing biosensor devices using different neutral biomolecule species like DNA, Uricase, APTES, Streptavidin, ChO_X, and Biotin in the nano-cavity region. The output characteristics such as drain off-current ratio, threshold voltage, surface potential, subthreshold slope, transconductance, output conductance, intrinsic voltage gain, output resistance, and device efficiency have been studied with biomolecule species. Shifting threshold voltage and drain off-current ratio were used as sensing metering to indicate device sensitivity for the target biomolecule. Lower leakage current and higher sensitivity have been investigated in a proposed device compared with a double metal gate transistor and existing biosensor.

Chapter-4 presents the impact of trap charge on triple metal gate high-k gate all around junctionless nanowire field-effect transistor biosensor on device sensitivity with APTES and biotin biomolecules. But in order to analyze the CMOS device sensitivity, investigation of performance degradation of p-channel Junctionless high-k gate GAA NWFET due to localized charges is necessary. So this chapter first illustrates the impact of localized charges on the electrical performance of the p-channel junctionless high-k gate GAA NWFET biosensor with different trap charges. Effects of ITCs were utilized in this objective to do a comparative analysis of the output properties of double and triple metal gate high-k gate all around junctionless NWFET biosensors. The impact of ITCs on output characteristics such as transconductance, output resistance, device efficiency, leakage current, and switching ratio with and without APTES biomolecule has been studied. For detecting the different biomolecules, such as APTES biomolecule, vital in diagnosing Alzheimer's disease, several ITCs and the drain-off current ratio were examined as sensing metrics. We conclude that the performance of a biosensor device based on a triple metal gate high-k gate-all-around junctionless nanowire field-effect transistor is improved by a negative ITC as opposed to a positive ITC.

Chapter-5 To examine the effect of metal gate work-function modification on the sensitivity of different biomolecules, especially, Uricase and ChO_x biomolecules, a triple metal gate high-k gate-all-around junctionless nanowire FET-based biosensor was developed. The analytical results are validated by employing a technology called "ATLAS-3D", which is a device simulation. Triple metal gate high-k gate all around junctionless NWFET biosensors have been investigated, and their output properties have been compared over various biomolecules and metal gate work functions.

Fermi-Dirac Statics, doping versus mobility, and concentration-dependent mobility model have been used to simulate band gap mobility in the high channel doping along the bandgap narrowing (BGN) model and also Shockley–Read–Hall (SRH) model along the Boltz-man transport model has been used to account recombination of minority carriers within the drift or diffusion. The impact of different metal gate work-function on output characteristics such as transconductance, shifting threshold voltage, device efficiency, output conductance, intrinsic voltage gain, and switching ratio with Uricase and ChO_x biomolecules has been studied.

Chapter-6 summarises the entire effort depicted in this thesis and the concrete conclusions reached from the results presented in this thesis. This chapter also looks at the current study's limitations and potential scope, as well as how this work could be extended and used in the future for more relevant applications.

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CHAPTER -2

Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor

Abstract

MOSFET-based gas sensors have recently become popular due to their low cost and high sensitivity, making them useful in various commercial, residential, and even medical settings. In this objective, a junctionless(JL) gate all around (GAA) silicon nanowire field-effect transistor with catalytic metal gate (palladium) was proposed for high sensitivity and low power hydrogen gas (H_2) recognition using ATLAS-3D device simulator and also analytical modelling. Due to its sensitivity to hydrogen gas (H_2), palladium (Pd) is employed as a gate electrode in H_2 gas sensing. Unsafe conditions can result if hydrogen escapes and accumulates in an enclosed space throughout the purifying process; this is why we try to investigate technologically ultra-small-scale hydrogen gas sensor devices. Temperature and palladium (Pd) gate work function variations in the translation processes were well-thought-out to examine the shift in surface potential, channel electron/hole concentration, subthreshold current, and threshold voltage to predict the sensor's response employing extensive simulations. Shift in threshold voltage (V_{th}), Ion, and Ioff ratio as a result of the metal work function variation was examined. These alterations can be thought of as sensitivity parameters for the purpose of sensing hydrogen gas molecules. The resulting analytical models of shifting threshold voltage (ΔVth) and subthreshold current $\left(S_{I_{OFF}}\right)$ sensitivities were consistent with simulation data. When the sensitivity $\left(S_{I_{OFF}}\right)$ of JL-GAA-SiNWFET is compared with GAA-MOSFET and bulk MOSFET, JL-GAA-SiNWFET shows improved sensitivity. The results show that as 150mV Pd work function shifts at the gate, the sensitivity improvement with JL-GAA-SiNWFET-based hydrogen gas sensors was 51.65% and 124.51% compared with GAA MOSFET and MOSFET, respectively. High dielectric oxide (HfO_2) and interface oxide (SiO_2) are also employed at the gate to overcome electron tunnelling. Results show that a junctionless silicon nanowire field-effect transistor with a catalytic metal gate is more suitable for hydrogen molecule detection than a bulk metal oxide semiconductor field-effect transistor (MOSFET).

This finding provides novel promises for using Pd island gate junctionless gates all around SiNW field-effect transistor sensors to detect hydrogen gas. It is applicable for industries such as petrochemical plants, nuclear reactors, hydrogen manufacturing facilities, petroleum refineries, space launching, leak detection, fuel cells, medical diagnostics, and nuclear power plants; in addition to its low power consumption, easy integration, good thermal stability, and enhanced hydrogen sensing properties.

2.1 Introduction

In this Chapter, a junctionless (JL) gate-all-around (GAA) silicon nanowire field-effect transistor sensor has been investigated for hydrogen gas (H_2) detection. Today's contemporary society has brought various luxurious things, but with them have come to a slew of issues, such as air pollution and harmful gas emissions[1], [2]. As a result of the growing awareness of the importance of regulating the emissions of these gases, a demand for gas sensors has emerged[3], [4]. Because of its high heat of combustion, low minimum ignition energy, and rapid combustion velocity, hydrogen is considered one of the most significant clean energy carriers and the ultimate fossil fuel contender and renewable energy source[5], [6]. Hydrogen gas is also utilized in metal smelting, petroleum extraction, semiconductor processing, glassmaking, and the everyday chemical industry[7], [8] due to its powerful reducing properties. Since hydrogen gas is odourless, humans cannot detect its presence [9], [10]. Due to its low explosion energy and wide flammable range, it is highly combustible and explosive[6], [11].

Consequently, an efficient and dependable hydrogen sensing device is necessary for hydrogen production and consumption, monitoring and managing hydrogen concentrations in nuclear reactors and coal mines, and detecting and alarming H_2 leakage during storage, transportation, production, and consumption[5], [12]–[14]. Sensors that detect gases have many functions and can be found in various businesses and settings, such as pollution detection, chemical analysis, and vehicle emissions[15], [16]. A wide variety of industries use sensors, from aircraft to manufacturing to fuel cells[3], [17]. Various types of SiNWFET-based hydrogen gas detection devices have been implemented in recent years to identify gas molecules by analyzing the induced gate work function at the surface of an attractive film [9], [14]. From many types of gas sensors, NWFET-based gas detectors have received much attention[8]. As stated in Chapter 1, GAA MOSFET, also known as surrounding gate nanowire MOSFET, is one of the most hopeful device architectures for extending CMOS device scaling because it offers the best electrostatic control of the channel[18] in the area of sensing applications. Since GAA MOSFET is more vigorous against hot carriers than Bulk MOSFET due to increased gate control and less short channel effects[19], this device provides low power consumption, high mobility, high sensitivity, low cost, small size, technology compatibility, on-chip integration, and CMOS compatibility[12], [20], and is more reliable against hot carriers than Bulk MOSFET due to improved gate control and reduced short channel effects[19]. Junctionless silicon nanowire field effect transistors (SiNWFET sensors are attractive for gas sensing [9] because of technology compatibility) [18] for on-chip integration, portability, low power consumption, and the ability to detect both weakly bound strongly bonded and chemical bonding species at room temperature [19,20]. To detect gas, a sensor device uses the interaction of a tiny coating of palladium (Pd) to hydrogen gas[2], [9], [21]. The detection process relies on the interfacial adsorption of hydrogen molecules that have become dissociated into the palladium gate, where they develop a dipole layer and produce a considerable shift in the gate's threshold voltage (ΔV_{th})[1], [9], [13].

In this chapter, high-k gate oxide materials hafnium oxide (HfO_2) and interface oxide (SiO_2) were chosen to develop nanoscale electrical devices with high performance that have relied significantly on gate dielectric materials. Since hafnium oxide (HfO_2) is the most excellent and powerful dielectric material and improves the sensing performance of FET at the nanoscale when compared to other dielectric materials[22], [23], and is more stable over silicon substrates, needs less power, has a less direct tunnelling effect, and reduce leakage current. The importance of using (palladium) Pd metal gate as a catalyst to increase SiNW thin film H_2-sensing performance is the simple synthesis, which allows for careful control of SiNW and palladium (Pd) metal gate thicknesses to generate detectors with the highest possible sensitivity[1], [9]. A thin Pd film's reaction to hydrogen gas makes this a valuable device for detecting gases[9]. The interfacial adsorption of disassociated hydrogen molecules into the Pd gate produces a dipole layer, which alters the gate's work function and results in a measurable shift in threshold voltage[9], [11].

The hydrogen gas sensor was realized using conventional MOSFET [12], Metal Insulator Semiconductor (MIS) architectures[24], Tunnel FET (TFET)[9], temperature-regulated phase transition FET along with Palladium (Pd) gate electrode[24]. However, the possibility of the cylindrical GAA JL NWFET with the catalytic metal gate for gas sensing applications has not been investigated. Since Short Channel Effects [9] can significantly decrease the sensing performance of conventional FETs at shorter gate lengths, making them less desirable potential candidates for implementing H_2 gas sensors[8]. To address the shortcomings of conventional FET-based H_2 gas sensors, junctionless gate-all-around SiNWFET-based sensors have been investigated to improve sensitivity while reducing SCEs. In this study, we present systematic research for sensing performance characteristics of a shorter-channel junctionless gate-all-around SiNWFET at lower supply voltage and compare it to its inversion mode counterpart.

2.2 Device Structure and Simulation Models

2.2.1 Device Structure

The three-dimensional structures and two-dimensional cross-sectional view of the p-type palladium metal gate Junctionless (JL) GAA SiNWFET-based hydrogen gas sensor are shown in **Figure 2. 1**. The GAA SiNWFET architecture contains a 40 nm long p-type doped with a $1x10^{19}$ cm^{-3} doping concentration from the source to drain through the channel uniformly. Also, L (20nm) is the length of dielectric material (HfO_2), channel, (SiO_2) is an interface oxide layer and T_1, T_2, and T_3 are the thickness of the catalytic metal gate, hafnium oxide, and interface (SiO_2) oxides, respectively, and 2R is the channel diameter (silicon film thickness), as shown in **Table 2.1**. For our developed p-type substrate devices, a high doping concentration ($1x10^{19}$ cm^{-3}) was applied uniformly through the channel from the source to the drain to provide a tolerable threshold voltage. The supply gate-source voltage (0.6V) was used for all simulations with a consistent drain-source voltage (0.05V). All simulations were carried out with the Atlas simulator in the Silvaco TCAD tool. In order to prevent parasitic resistance effects, it is commonly believed that the source and drain extensions are less than the channel length [25].

The device gate length is 20nm for all simulations, while the source and drain lengths are 10nm, as illustrated in **Table 2.1.**

Table 2. 1: Physical parameter setting for simulation structure [30].

Device Parameters	GAA-JL-SiNWFET
Channel length (nm)	20.00
Thickness of oxide HfO_2 & SiO_2 respectively, (nm)	1.50 & 0.30
Interface Oxide (SiO_2) thickness, (nm)	1.00
Oxide (SiO_2) length, (nm)	20.00
Source and Drain length/thickness (nm)	10.00
Hafnium Oxide (HfO_2) length, (nm)	20.00
Radius of silicon film (nm)	10.00
Drain, Source & Channel Doping (N_D+)	$10^{19}cm^{-3}$
Oxide dielectric constant, HfO_2 & SiO_2	25.00 & 3.90
Reference gate work function (Palladium), (eV)	5.20

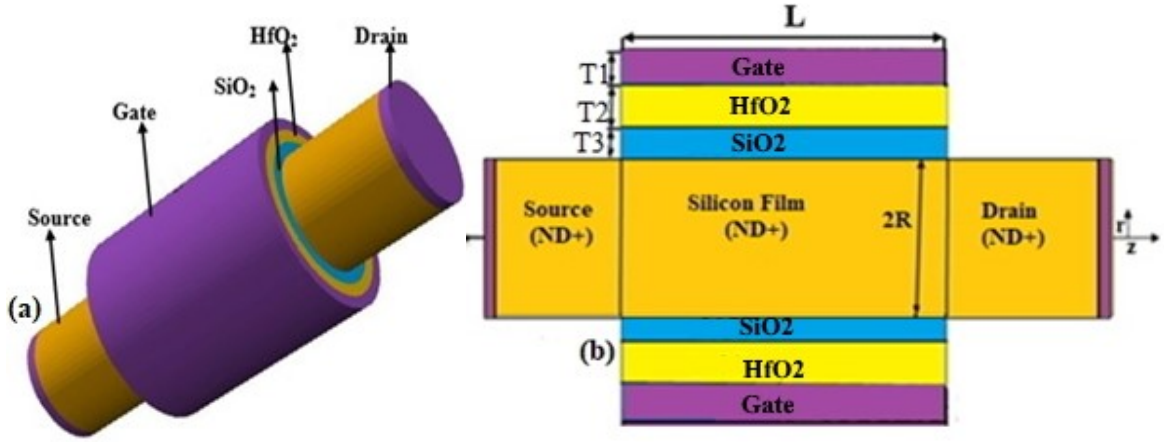

Figure 2. 1. illustrates **(a)** a schematic of 3D structure and **(b)** 2D cross-sectional view for a p-type substrate cylindrical JL-GAA-SiNWFET-based hydrogen sensor [30].

2.2.2 Simulation Models

All simulations in this chapter are performed using the Silvaco TCAD-ATLAS tool. To incorporate electron mobility models, concentration-dependent mobility, drift-diffusion, and field-dependent mobility models are activated [26], [27]. To take into account majority-minority charge carrier recombination, the Shockley-Read-Hall (SRH) recombination model is activated [17]. The drift-diffusion model includes a charge carrier following the driving current[28]. Fermi Dirac Statistics were introduced because of heavy source and drain doping[29], [30] without impact ionization. Band-gap narrowing and Newton-Gummel technique are used to simulate the device. The Boltzmann transport statistics and concentration, voltage, and temperature (CVT) [39] Lombardi mobility model [16] account for parallel and

perpendicular field mobility[31]. All of the simulations of the devices have been run with the technological parameters and supply voltages specified by the ITRS [31].

2.2.3 Function description

In this study, we used catalytic metal gate engineering to characterize the behavior of a JL-GAA-SiNWFET-based hydrogen gas sensor. Palladium(Pd), a catalytic metal gate, has good compatibility with hydrogen gas, making it suitable for detecting hydrogen storage (reversibly introduced))[10], [11], [33]; Van der Waals forces interact between hydrogen gas molecules and palladium atoms when interacting with the palladium surface[24]. The hydrogen molecules adsorb on the palladium surface, and the attractive interactions between the palladium and the hydrogen atoms weaken the H-H bond, causing the hydrogen molecules to dissociate into hydrogen atoms[16]. The Pd work function must significantly affect how the device's electrical field properties change over time. As illustrated in

Figure 2. 2(b), when exposed to H_2 gas, molecules break off at the metal surface of the metal gate (Pd) and then diffuse into the metal gate. As a result, some hydrogen atoms diffuse through the gate metal, resulting in the dipole at and within the interface by modifying the metalwork function[16]. The electrical characteristics of the sensor are altered because of the change in palladium's work function caused by the dipole layer[16]. Due to this effect, the proposed device's I_{ON}/I_{OFF} ratio, drain-off sensitivity ($S_{I_{OFF}}$), and performance shifts in threshold voltage are investigated.

Figure 2. ***2***(a) shows that the analytical model[34] published before has been used to calibrate and validate the simulation results in designing the proposed JLGAA SiNW FET hydrogen gas sensor.

Figure 2. ***2***(a) shows a good agreement between the simulated result and the data from the previous analytical model[34]. As a result, it justifies the various simulation models and methods employed in this work. Several electrical characteristics were examined to investigate the behavior of the JL GAA SiNWFET as a gas sensor when hydrogen gas of varying concentrations is adsorbed on the Pd gate.

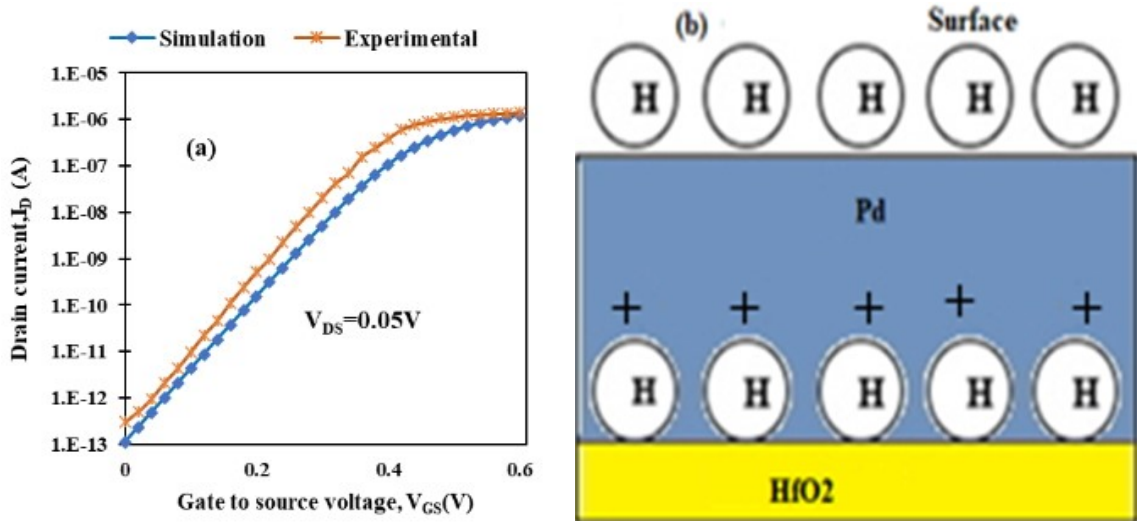

Figure 2. 2. Depicts **(a)** Calibration of simulation results [30] with experimental results [34] and **(b)** 2D Electrical dipole formation at the Pd/HfO_2 interface.

2.3 Two-Dimensional Analytical Subthreshold Model

2.3.1 Surface Potential and Subthreshold Current Modeling

Short-channel effects can be easily understood with the use of evanescent-mode analysis. It yields qualitatively different scaling predictions than analysis based on the parabolic approximation and correctly accounts for the 2-D nature of the electrostatics. A solution to Poisson's equation in cylindrical coordinates for the distribution of potential energy in a silicon layer was written as[35];

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi(r,z)\right)+\frac{\partial^2}{r^2}\phi(r,z)=\frac{qN_A}{\varepsilon_{Si}} \tag{2. 1}$$

where $\phi(r,z)$ is the two-dimensional electric potential distribution in the silicon film, "N_A" is the silicon film doping, "q" is the electron charge, and ε_{Si} is the silicon dielectric permittivity. When hydrogen gas molecules are exposed to a catalytic metal gate at the terminal gate to source voltage (V_{gs}), they dissociate and become adsorbed[17]. Dissociated hydrogen gas molecules at the gate-dielectric interface form a dipole. These dipoles alter the metal gate's work function, which in turn causes a change in the flat band voltage (V_{fb}). In light of this, the sensor's bounds have been defined as [36]:

The superposition approach derives the potential distribution $\phi(r,z)$ in two dimensions. As illustrated below, we can derive the potential with Poisson's equation $\phi(r,z)$[36]; The solution of the two-dimensional potential $\phi(r,z)$ obtained using the boundary conditions, as shown below;

i) The radial potential at the center depends simply on z;

$$\phi(r = 0, z) = \phi_S(z) \tag{2. 2}$$

ii) At the center of the silicon film, the electric field is at zero;

$$\left.\frac{d\phi(r,z)}{dr}\right|_{r=0} = 0 \tag{2. 3}$$

iii) The electric field at the silicon oxide contact is calculated as follows;

$$\left.\frac{d\phi(r,z)}{dr}\right|_{r=\frac{t_{Si}}{2}} = \beta\left[\phi\left(r = \frac{t_{Si}}{2}, z\right) - V_{gs} + V_{fb}\right], \quad \text{for P-channel} \tag{2. 4}$$

Where $\beta = C_{oxcyl}$

where V_{fb} is the flat band voltage, C_{oxcyl} is the gate oxide capacitance per unit area of the cylindrical-gate NWFET, and is given as;

$$C_{oxcyl} = \frac{2\varepsilon_{ox}}{t_{Si}\ln\left[1 + \left(\frac{2t_{ox}}{t_{Si}}\right)\right]} = \frac{\varepsilon_{ox}}{\left(\frac{R}{2}\right)\ln\left[1 + \left(\frac{t_{ox}}{R}\right)\right]} \tag{2. 5}$$

Where the gate to source voltage is V_{gs}, the oxide layer thickness is t_{ox}, the silicon film thickness (channel) is ($t_{Si} = 2R$), and the dielectric permittivity of the oxide layer is ε_{ox}.

The variation in the amount of hydrogen gas that is present on the metal gate brings about a commensurate shift in the work function, which in turn brings about a change in the flat band voltage. The effective flat-band voltage (V_{fbeff}), is a measurement that determines the extent to which the reactivity of gas molecules produces a change in the work function of the catalytic metal. This change in work function is measured at the surface of the metal [9], [36].

$$V_{fbeff} = \phi_m - \phi_s \pm \Delta\phi_m \tag{2. 6}$$

where ϕ_m represents a metal's work function and ϕ_s the silicon's work function, as shown below.

$$\phi_s = \frac{E_g}{2} + \chi - V_T\left(ln\left(\frac{N_A}{n_i}\right)\right), \quad \text{for p-type} \tag{2. 7}$$

The thermal voltage is denoted by $V_T = \frac{K_B T}{q}$, whereas the Boltzmann constant, temperature, and charge are denoted by K_B, T, and q, respectively χ is silicon's electron affinity, and n_i is intrinsic carrier concentration. The proposed hydrogen gas sensor uses a Palladium (Pd) catalytic gate electrode (m=5.2eV) [17] as its detecting element. This chapter investigates the

change in metal gate work function due to temperature variation at constant pressure. The changed work function is as follows:

$$\Delta\phi_m(T) = -\left(\frac{\theta_i N_i \mu}{\varepsilon_0}\right) \tag{2. 8}$$

Where θ_i is the hydrogen interface coverage, μ the hydrogen-induced effective dipole moment, N_i the total concentration of hydrogen adsorption sites at the metal-oxide interface, and ε_0 free space permittivity [9]. The change in metal gate work function is affected by hydrogen gas flux (F), interface coverage θ_i, pressure (P), surface (θ_s)[4], and temperature (T)[12], [17]. The gas flux is given as follows [17]:

$$Flux(F) = \frac{N_a P}{\sqrt{2\pi mRT}} \tag{2. 9}$$

Here, Avogadro's constant is Na, the molar mass of hydrogen gas is m, and the gas constant is R. The change value in the work function is obtained using **(eq.2.8)** at different temperatures ranging from 300k to 500k. Introducing gas molecules to the gate of the device causes a shift in the flat band voltage, which alters the device's surface potential.

The distribution of surface potentials in the channel regions is derived using the two-dimensional (2-D) Poisson's equation under potential and field continuity assumptions. As a result, the radial surface potential $\phi_S(z)$ is calculated by applying boundary conditions.

$$\phi_S(z) = -(Ae^{kz} + Be^{-kz} + \Phi), \quad \text{for the p-type channel} \tag{2. 10}$$

Where K and Φ is given by;

$$k = \sqrt{\frac{2\varepsilon_{OX}}{\varepsilon_{Si} R^2 \, ln\left(1 + \frac{t_{OX}}{R}\right)}} \tag{2. 11}$$

$$\Phi = V_{gs} - V_{fb} - qN_{Si}/\varepsilon_{Si}k^2 \tag{2. 12}$$

The coefficients A and B are determined by the source and drain boundary conditions and are expressed as

$$A = \frac{(V_{bi} + \phi)(1 - e^{-kL}) + V_{ds}}{2\,sinh(k_B L)} \tag{2. 13}$$

$$B = \frac{(V_{bi} + \phi)(e^{kL} - 1) - V_{ds}}{2\,sinh(k_B L)} \tag{2. 14}$$

The whole two-dimensional potential is given by

$$\phi(r,z)=\phi_s(z)+\frac{C_{ox}}{2\varepsilon_{Si}}\left(\phi_s(z)-V_{gs}+V_{fb}\right)\left(r^2-R^2\right), \text{ for p-channel} \quad (2.15)$$

Based on a 2-dimensional potential relation, subthreshold current is given by.

$$I_{Sub}=2\pi R\mu q n_i \frac{\int_{V_{gs}}^{V_{ds}} e^{-qv(z)/KT}dV(z)}{\int_0^L \frac{dz}{\left(\int_0^R e^{q\phi(r,z)/KT}dr\right)}}, \text{ for p-channel} \quad (2.16)$$

Drift-diffusion modelling is used to calculate the source-drain current flowing, as shown below;

$$I_{dlinear}=\left[\mu\varepsilon_{ox}\frac{T_{Si}}{L_g}\left(\left(V_{gs}-V_{th}\right)V_d\right)-\frac{V_d^{\,2}}{2}\right] \quad (2.17)$$

The following mobility reduction effects are included in the model;

$$\mu_{eff}=\frac{\mu_0}{1-\alpha\left(V_{gs}-V_{th}\right)} \quad (2.18)$$

Here, α (~0.04) is the fitting parameter, n_i is the concentration of intrinsic carriers, $C_{ox=\varepsilon_{oxide}}$ is the oxide dielectric permittivity, V_d is the drain voltage, V_{th} is the threshold voltage, L_g is the gate length, and V_g is the gate voltage.

2.3.2 Threshold Voltage (V_{th}) Modeling

The threshold voltage (V_{th}) in an enhancement mode of a p-channel MOSFET device can be calculated using eq (19) [37].

$$V_{th}=V_{(T,0)}+\gamma\left(\sqrt{|V_{SB}+2\phi_s|}-\sqrt{|2\phi_s|}\right) \quad (2.19)$$

where V_{th} is the threshold voltage, V_{SB} is the source-to-body substrate bias, $V_{(T,0)}$ is the zero-substrate bias threshold voltage, ϕ_s is the contact potential, and (γ) is a constant body effect parameter defined as[12];

$$\gamma=\left(t_{OX}/\varepsilon_{OX}\right)\sqrt{2q\varepsilon_{Si}N_A} \quad (2.20)$$

$$\phi_s=\frac{K_BT}{q}ln\left(\frac{N_A}{n_i}\right) \quad (2.21)$$

$$n_i = 5.2x10^{15} xT^{3/2} x\, exp\left(\frac{-E_g}{2K_B T}\right) \quad (2.22)$$

Here t_{ox} is the thickness of the oxide, ε_{ox} is the relative permittivity of the oxide, T is Temperature, N_A is the doping concentration, k is Boltzmann's constant, q is the charge of an electron, n_i is the silicon intrinsic doping parameter, and ε_{Si} is the relative permittivity of silicon semiconductors.

Therefore, the radius-dependent threshold voltage for a GAA-JL-SiNWFET is obtained by eq.(2.23))[38];

$$V_{th} = \Delta\Phi_M + \frac{K_B T}{q} ln\left(\frac{8K_B T\varepsilon_{Si}}{q^2 n_i}\right) - \frac{2K_B T}{q} ln\left[R\left(\frac{1+t_{OX}}{R}\right)^{\frac{2\varepsilon_{Si}}{\varepsilon_{OX}}}\right] \quad (2.23)$$

The difference in work functions is denoted by $\Delta\Phi_M$, where R is the device's radius of cylindrical JL-SiNWFET.

2.4 Simulation Results and Discussion

2.4.1 Change in Drain Current

The I_{ON}-state current of the devices is shown in **Figure 2. 3** (a &b) for channel lengths, L = 20 nm and Tsi = 10 nm and extracted at a drain voltage of (V_D =0.05V) in all simulations. **Figure 2. 3 (a &b)** depicts the temperature and palladium metal gate work function-dependent drain current shift for a p-type gate-all-around junctionless SiNWFET sensor. Since the change in drain current is an essential feature for distinguishing hydrogen gas molecules. In this case, hydrogen gas molecules reacting with the catalytic metal gate determine the gate's work function[24], [36], [39]. The sensitivity to hydrogen gas is evaluated regarding a shift in the device's threshold voltage and drain current. The proposed device's drain current shifts by $1.08x10^{-10}$A from 5.20eV to 5.40eV and by $1.0x10^{-8}$A from 300K to 500K, as shown in **Figure 2. 3 (a and b)**, respectively, when the work function and temperature are varied. In all situations, the impact of metalwork function and temperature variation causes I_{OFF}-current to shift rapidly in the tiny inversion zone, and this change is inversely proportional to hydrogen gas concentration[40]. The result is a significant hydrogen gas sensor device with dramatically increased sensitivity in the subthreshold region at the expense of power consumption. In the absence of Fermi level restraining, hydrogen gas molecule surface reactivity on palladium metal causes a change in the gate work function, leading to higher sensitivity in the subthreshold region [16], [17], [40]. I_{OFF} varies exponentially with the work function in millivolts, as shown in **Figure 2. 3**. Since the effect of gas molecules on I_{OFF} is substantially stronger than I_{ON}, the subthreshold area enables much higher sensitivity and low-power operation, resulting in a low-cost gas sensor device[41]. The close agreement between the simulated and analytical results demonstrates the validity of the analytical model for p-channel

GAA-JL-SiNWFETs. We conclude that the proposed technology is useful for detecting hydrogen gas molecules.

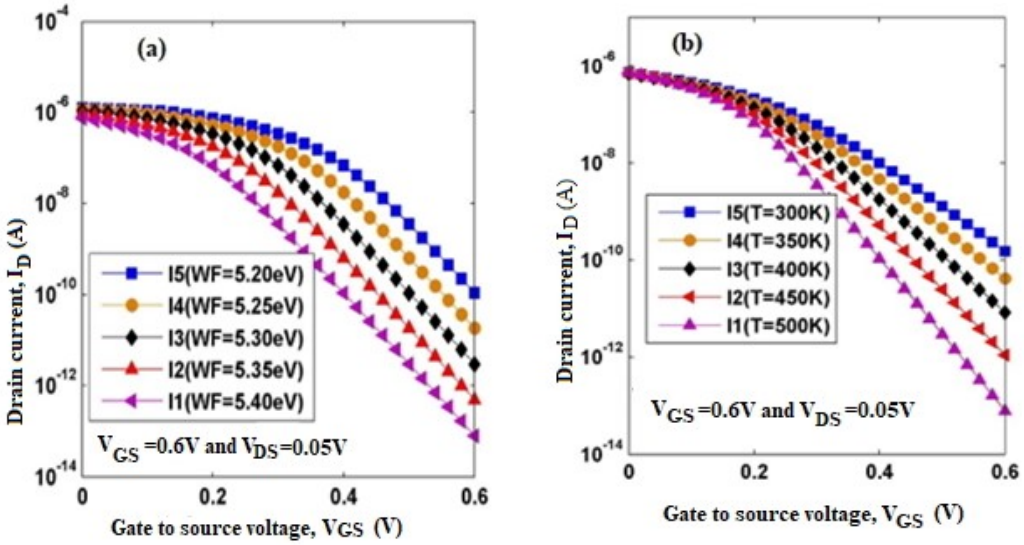

Figure 2. 3. Illustrates the impact of **(a)** palladium (Pd) work function and **(b)** Temperature on I_D-V_G for p-channel cylindrical JL SiNWFET [30].

2.4.2 Surface Potential-Based Sensing

A change in the work function at the surface of the sensitive film or the catalytic metal induces a change in the drain-source current, and the FET functions as a transducer by transforming this change into an electrical signal [39]. **Figure 2. 4** shows the variation in surface potential with respect to channel length over a range of temperatures and palladium work functions with a Palladium metal gate on P-channel junctionless GAA SiNWFET. The graph clearly shows that when the metal work function rises, so does the minimum surface potential. As the concentration of hydrogen gas on the catalytic gate increases, so does the number of dipoles generated at the gate and oxide interface[5], [17]. As the concentration of hydrogen gas increases, so does the surface potential[16]. The flat-band voltage shifts because of the additional band bending generated by gas molecules' interaction at the catalytic metal's gate surface [42]. The change in energy bands (conduction and valence bands) [39] is more pronounced in the channel region than in the source and drain regions, making JL cylindrical SiNWFETs more sensitive[24]. A shift in the surface potential, drain current, and threshold voltage (V_{th}) occurs whenever there is a change in the voltage of the flat band. Thus, it is possible to detect the presence of hydrogen gas molecules using a palladium catalytic metal gate by monitoring the shifting of I_{OFF}, switching ratio, and V_{th}, as shown in **Figure 2. 4(a).** Various papers have reported that the surface potential shifts slightly with temperature [7]. In this chapter, temperature variation also impacts the sensitivity capability for p-channel junctionless GAA-SiNWFET, as depicted in **Figure 2. 4(b).**

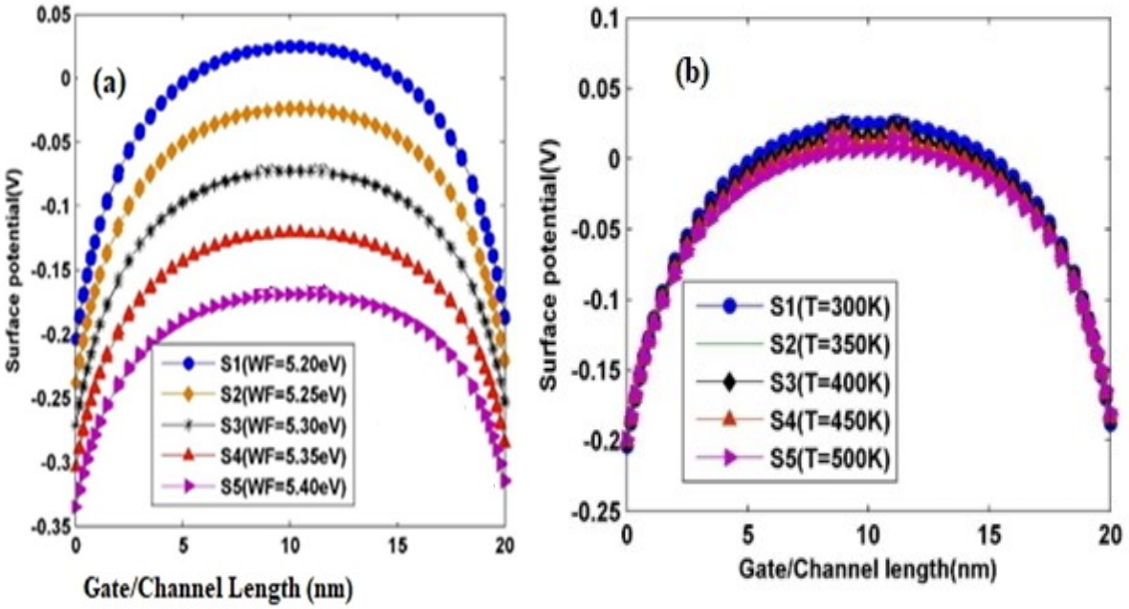

Figure 2. 4 depicts the effect of (**a)** palladium (Pd) work function and **(b)** Temperature on surface potential (V) for p-channel cylindrical JL SiNWFET [30], ($V_{GS} = 0.6V \; and \; V_{DS} = 0.05V$).

2.4.3 Electron Mobility-Based Sensing

a) Electron mobility

As indicated in **Figure 2. 5**, the electron mobility throughout the channel was also extracted. The reactivity of hydrogen gas molecules at the gate surface alters the work function of the catalytic metal gate, causing electron mobility shifts in the channel region. The change in electron concentration in the channel region is much more significant than in the source and drain regions. Modified electron concentration and charge flow are developed due to an altered electric field in the channel region[8], [43]. The interaction of H_2 gas with the palladium gate electrode generates a change in gate potential, which causes a shift in channel electron mobility between the source and drain[24]. Finally, we conclude that the interaction of hydrogen molecule catalytic metal electrode affects electron mobility or concertation in channel regions at different temperatures and electrode work function as depicted in **Figure 2. 5**.

As a result, electron mobility is crucial in determining MOSFET performance. To obtain high device performance, material parameters like as doping concentration and crystal orientation must be optimized to improve electron mobility. GAA JL MOSFETs are suitable for applications like high-speed logic circuits and power electronics due to their increased electron mobility, which can result in quicker switching rates, larger driving currents, and reduced power consumption.

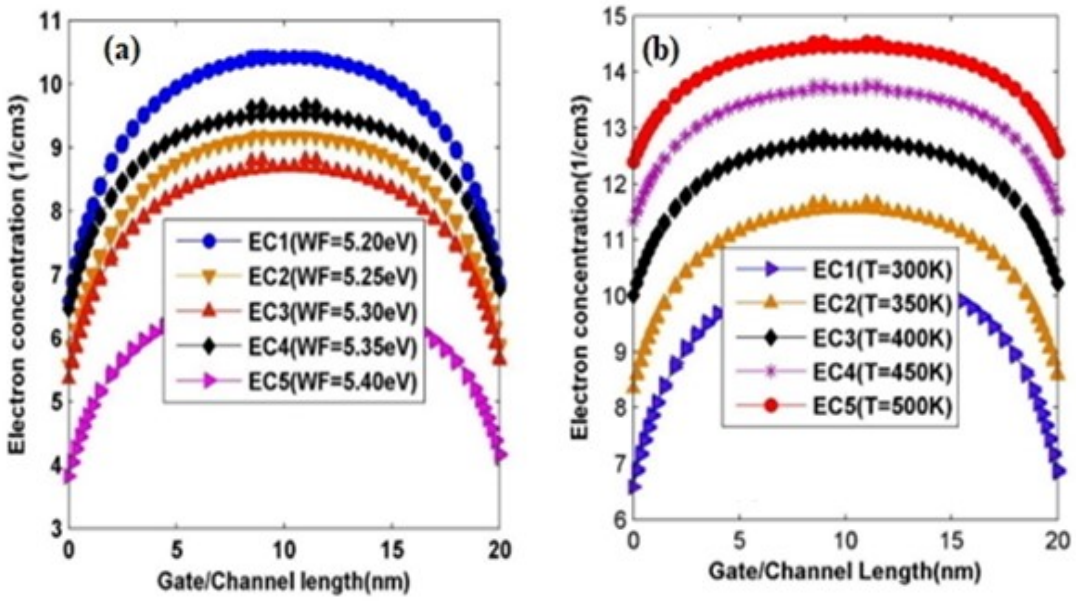

Figure 2. 5. Effects of **(a)** palladium (Pd) gate work- function and **(b)** Temperature variation on electron concentration ($1/cm^3$) for p-channel cylindrical JL-SiNWFET [30], ($V_{GS} = 0.6V \; and \; V_{DS} = 0.05V$).

b) Hole Mobility

In a Gate-All-Around (GAA) Junctionless (JL) MOSFET, hole mobility is the ability of holes, which are positively charged carriers, to move through the device's channel area when an electric field is present. The hole mobility in a GAA JL MOSFET is affected by many things, such as the crystal orientation of the channel region, the doping concentration, the temperature, and the presence of scattering mechanisms like impurities, defects, and phonons. The change in palladium metal work function and temperature also led to a shift in hole concentration. As stated earlier, the reactivity of hydrogen gas molecules at the catalytic metal gate surface changes the work function of the gate metal, resulting in additional band bending and a change in flat-band voltage[17]. The channel's hole concentration difference is significantly more than in the source and drain regions, as illustrated in **Figure 2. 6**. Because hole concentration affects the electric field in the channel, the flow of charges in the channel is also influenced, leading to shifting in drain current and, eventually, device sensitivity. Gate electrode work function affects hole concentration, as shown in **Figure 2. 6(a),** and it also changes the mobility of carriers in the device due to hydrogen molecules' interaction on the metal surface. Temperature variations also affect hole concentration, as shown in **Figure 2. 6(b),** and it also changes the mobility of carriers in the device due to hydrogen molecules' interaction on the metal surface[44]. This suggests that the diffusion rate of hydrogen molecules significantly influences the hole concentration through the channel, which increases with increasing temperature[24].

High hole mobility is required for high device performance, such as faster switching rates and more significant drive currents, which are vital for applications such as high-speed logic circuits and power electronics. Because holes have a higher effective mass than electrons, their mobility in a GAA JL MOSFET is often lower than that of electrons. However, excellent hole

mobility in GAA JL MOSFETs can be achieved by carefully developing the device structure and optimizing the material parameters.

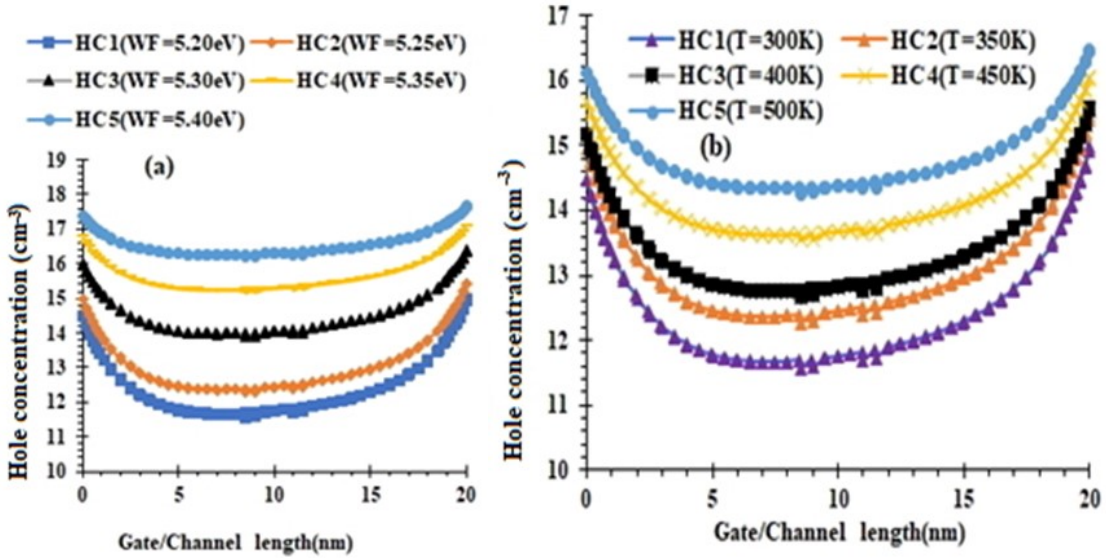

Figure 2. 6. Impacts of **(a)** palladium (Pd) work function and **(b)** Temperature variation on hole concentration ($1/cm^3$) for p-channel substrate cylindrical JL-SiNWFET [30], ($V_{GS} = 0.6V$ and $V_{DS} = 0.05V$).

2.4.4 Sensitivity Parameters (ΔV_{th} and $S_{I_{OFF}}$ ratio)

This section examines various parameters due to hydrogen molecules interacting with a catalytic metal electrode on the proposed device. For instance, threshold voltage variation, drain current shift, and surface potential changes are some electrical characteristics that determine the FET device's sensitivity. Threshold voltage (V_{th}) shift is a crucial characteristic that can be utilized to detect hydrogen gas[12], [30] in addition to drain current change, and variation in threshold voltage has a direct effect on the operation of a device, making it a crucial parameter[35]. As we have seen earlier, changes in the gate work function of the palladium metal and temperature cause the change in drain current and threshold voltage (V_{th}) in response to a fluctuation in the flat-band voltage. Changes in I_{ON}, V_{th}, and I_{OFF} can be used as indicators of the presence of hydrogen gas molecules[39]. As a result, hydrogen atoms diffuse into the gate metal, altering the metal work function and forming the dipole at and within the interface. We have extracted those output data from the simulation, and those factors can be thought of as sensitivity variables, as we have analyzed the I_{ON}/I_{OFF} ratio, drain-off sensitivity ($S_{I_{OFF}}$), and shift in threshold voltage(ΔV_{th}) of the proposed devices. As seen in **Figure 2. 7(a)**, sensitivity varies exponentially as the work function is raised due to the interaction of hydrogen gas molecules in the metal surface and can be estimated using **eq (2.24).** Therefore, the proposed hydrogen gas sensor's sensitivity is investigated by utilizing threshold voltage sensitivities ($S_{V_{th}}$) [17] and drain current sensitivities ($S_{I_{OFF}}$)[24]. The sensitivity of the drain current is calculated using the ratio of the difference in I_{OFF} between before and after the hydrogen gas reaction to the I_{OFF} value obtained before the reaction. $S_{I_{OFF}}$ is defined as[24];

$$S_{I_{OFF}} = \frac{I_{OFF}(\text{after gas reaction})}{I_{OFF}(\text{before gas reaction})} \quad (2.\ 24)$$

Adsorption of hydrogen molecules shows a variation in drain current sensitivity with changing work functions of catalytic metal gates, as seen in **Figure 2. 7(a).** The plot that measures the sensitivity of the drain current demonstrates that the $S_{I_{OFF}}$ value dramatically rises as the amount of hydrogen gas molecules adsorbed onto the Pd gate increases. As a result, the fact that $S_{I_{OFF}}$ is dependent on the drain current and exhibits the same behavior upon the entrance of hydrogen gas molecules.

Another important parameter used in gas molecule detection is shifting threshold voltage (ΔV_{th}), defined as the difference between the threshold voltage with and without hydrogen gas adsorption, is illustrated in **Figure 2. 7** as a function of palladium metal gate work function and temperature. The plot indicates that the value of $S_{V_{th}}$ increases in direct proportion to the rising concentration of hydrogen gas on the Pd gate. Both palladium gate electrode work function and temperature rise cause a change in the threshold voltage ($S_{V_{th}}$), which in turn increases the concentration of hydrogen gas molecules, as depicted in **Figure 2. 7** and defined by (**eq. 2.25).**

$$S_{V_{th}} = \left| V_{th}(after \text{ gas reaction}) - V_{th}(before \text{ gas reaction}) \right| \quad (2.\ 25)$$

In this section, we conclude that even while the presence of hydrogen gas can be determined by both the drain current and the threshold voltage shift, the subthreshold current sensitivity is a more suitable method for detecting the existence of hydrogen gas, as illustrated in **Figure 2. 7(a).**

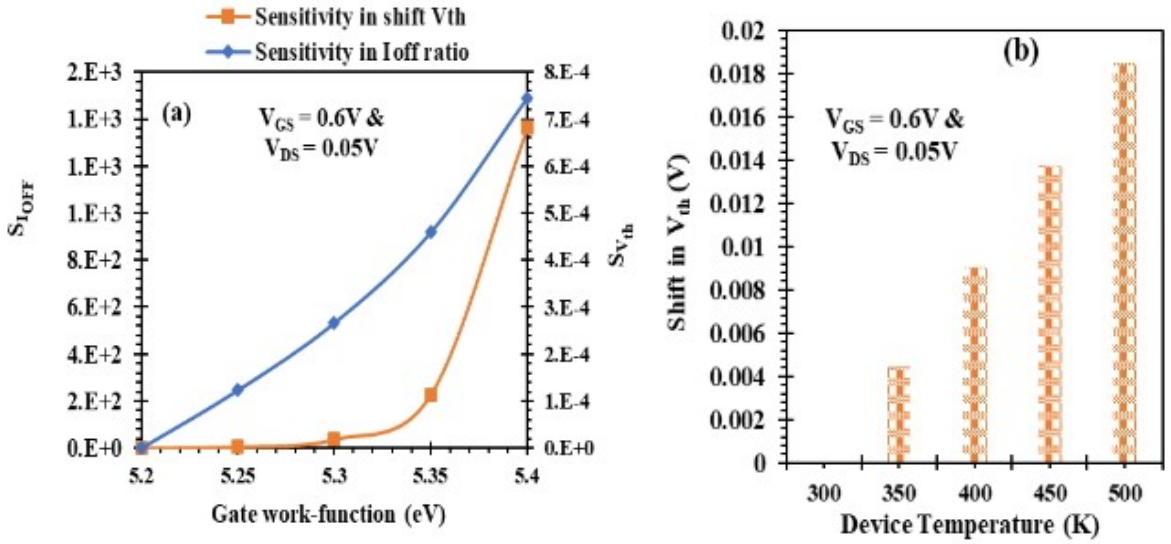

Figure 2. 7. Depicts the impact of **(a)** palladium (Pd) metal gate work and **(b)** Temperature on the I_{OFF} ratio for p-channel substrate cylindrical JL-SiNWFET [30].

Also, the proposed device performance and stability in the case at different palladium gate electrode work functions and temperatures are assessed considering the device switching ratio, as shown in

Figure 2. 8. It has been established in this chapter that unlike the subthreshold current shift and the threshold voltage, the switching ratio does not change drastically with changes in palladium (Pd) metalwork functions or temperature.

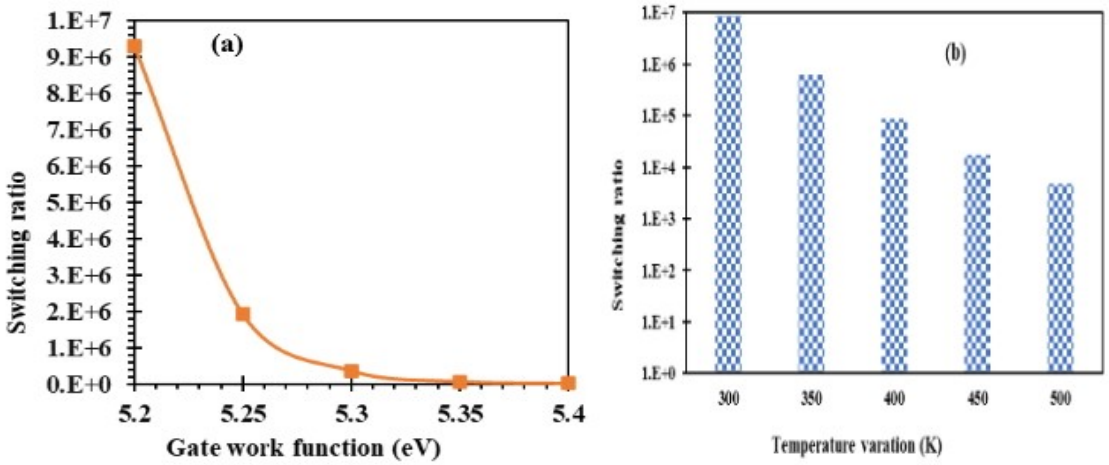

Figure 2. 8. Illustrate the impact of **(a)** palladium (Pd) metal gate work function on switching ratio and **(b)** Temperature on shifting threshold voltage for p-channel substrate cylindrical JL-SiNWFET [30], ($V_{GS} = 0.6V$ and $V_{DS} = 0.05V$).

Figure 2. 9 shows the proximity of the analytical model and the simulated results of the threshold voltage for the proposed device. The graph also demonstrates the remarkable agreement between the analytical model and simulation findings for the developed hydrogen gas sensor, and the model can predict how the device would behave.

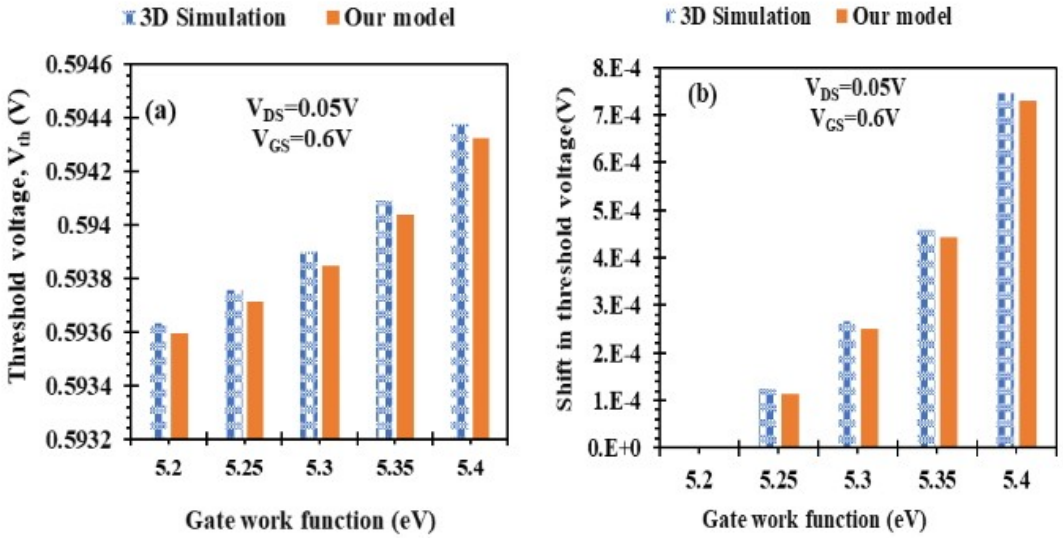

Figure 2. 9. Shows the effect of palladium (Pd) work function variation on **(a)** the threshold voltage (V_{th}) and **(b)** the shift in the threshold voltage (ΔV_{th}) for p-channel cylindrical JL-SiNWFET [30].

Figure 2. 10 shows the proximity of the analytical model and the simulated results of the proposed device's switching ratio and subthreshold/leakage current. The graph demonstrates the remarkable agreement between the analytical model and simulation findings for the developed hydrogen gas sensor, and the model can predict how the device would behave. The validation of the analytical model with simulation subthreshold current for p-channel JL GAA SiNWFETs comes from the high degree of agreement between the simulated and analytical data[17].

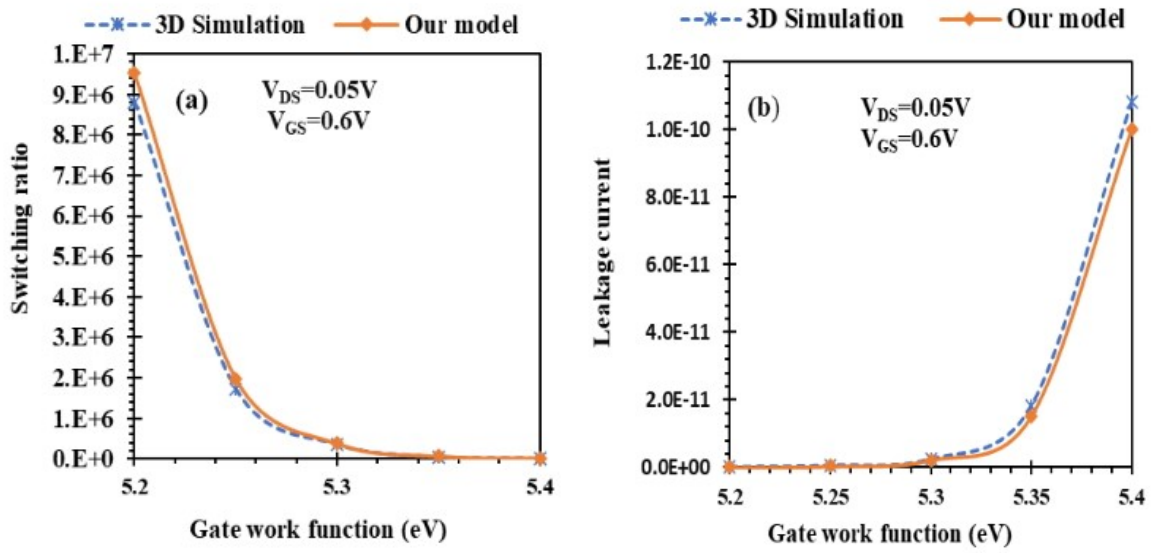

Figure 2. 10. Shows the impact of palladium electrode work function (Pd), **(a)** on the switching ratio, and **(b)**leakage current cylindrical p-channel substrate JL-SiNWFET [30].

To evaluate the JL -GAA-SiNW FET's performance, we compare its sensitivity ($S_{I_{OFF}}$) to that of the bulk MOSFET and the Gate All Around (GAA) nanowire FET hydrogen gas sensor[39]. The p-type substrate of bulk MOSFET, GAA-MOSFET, and JL-GAA-SiNWFET with palladium gate electrode sensitivity comparison is depicted in **Table 2. 2.** As we've already mentioned, the sensitivity parameter for gas sensing in this study is the change in subthreshold current, so these subthreshold properties are crucial. The increased sensitivity is due to better gate control and a lower subthreshold leakage current in the case of thinner silicon bodies with a higher surface-to-volume ratio. In **Table 2. 2,** for all devices simulation, the catalytic metal gate of palladium has been considered, and sensitivity in terms of current ($S_{I_{OFF}}$) before and after the gas reaction at the gate electrode has been analyzed at the same drain-source voltage (V_{DS}). Three architectures, namely bulk MOSFET, GAA MOSFET, and JL-GAA-SiNWFET are compared in terms of the influence of work function change induced by gas molecules on the device sensitivity ($S_{I_{OFF}}$). When the sensitivity of JL-GAA-SiNWFET was compared to the sensitivity of bulk MOSFET and GAA MOSFET, the sensitivity was found to be higher in JL-GAA-SiNWFET because the sensitivity ($S_{I_{OFF}}$) equation tells us that the hole mobility is related to the subthreshold leakage current and high-k dielectric materials in the case of JL-GAA-SiNWFET exposed to the channel is a more effective control. This ensures that bulk MOSFET and GAA MOSFET devices have a more significant subthreshold current than JL-GAA-SiNWFET. For instance, JL-GAA-SiNWFET demonstrates enhanced sensitivity ($S_{I_{OFF}}$)

compared to GAA-MOSFET and bulk MOSFET for 150mV shift in of Pd electrode work function at the gate, exhibits an increase in sensitivity of 51.65% compared to GAA-MOSFET and 124.51% compared to MOSFET. As mentioned before, this study's sensitivity parameter for gas sensing is the change in subthreshold current, making these subthreshold properties crucial. The increased sensitivity is due to better gate control and a lower subthreshold leakage current in the case of thinner silicon bodies with a higher surface-to-volume ratio.

Table 2. 2 also shows how the sensitivity of the JL-GAA SiNWFET gas sensor changes as the radius of the silicon pillars changes. As mentioned before, this study's sensitivity parameter for gas sensing is the change in subthreshold current, making these subthreshold properties crucial. The increased sensitivity is due to better gate control and a lower subthreshold leakage current in the case of thinner silicon bodies with a higher surface-to-volume ratio.

Table 2. 2: Palladium electrode gate sensitivity comparison shows the p-channel substrate of bulk MOSFET, GAA-MOSFET, and cylindrical JL-SiNWFET.

	$S_{I_{OFF}} = \frac{I_{OFF(after\ gas\ reaction)}}{I_{OFF(before\ gas\ reaction)}}$		
	Previously designed devices[39]		**Proposed device**
Shifting in Pd work function	Bulk-MOSFET $t_{Si} = 20nm$	GAA MOSFET $t_{Si} = 20nm$ R=10nm	JL-GAA-SiNWFET $t_{Si} = 10nm$ R=5nm
$\Delta\Phi_m = 50mV$	5.08	5.96	6.17
$\Delta\Phi_m = 100mV$	4.56	33.10	37.80
$\Delta\Phi_m = 150mV$	102	151	229
Device parameters: Drain, Source, and Channel doping (N_{Si})=$10^{19}cm^{-3}$, Oxide thickness is 1.5&0.3nm, oxide dielectric constants (HfO_2 & SiO_2 are 25.0 & 3.90, respectively), channel length(L)=40nm, radius(R)=5nm, gate to source voltage (V_{GS})=0.6V, and in all case drain-source voltage (V_{DS})=0.05V			

Therefore, the physical significance of the proposed device is described here: As we have stated earlier, hydrogen is one of the most critical future clean energy sources on the road to a more sustainable World and the replacement of fossil fuels[42], [45]. Among many other things, the widespread availability of hydrogen gas could play a significant role in propelling the energy transition and decarbonization[15]. Due to these and other applications, we studied and designed a Palladium gate modulated JL-GAA-SiNWFET-based hydrogen sensor, which is crucial in applications where health is significant due to their unique qualities, particularly their low fire risk, making them the technology of choice, such as mass transit hydrogen-powered vehicles and H_2 accidental leakage[43]. As a result, palladium electrode material is highly sensitive and selective to H_2, and it can perform in the absence of oxygen [42]**.** This chapter examines Palladium electrode JL-GAA-SiNWFET-based hydrogen gas sensor and its potential uses.

2.5 Summary

There is a growing need for reliable and cost-effective gas detection systems to mitigate the risk of gas leaks at different fueling stations, healthcare, industry, environment, and the military. Detecting various gases has applications in various industries, including the medical business, agriculture, and environmental studies. For instance, Hydrogen is an odourless, colourless, and highly combustible gas utilized as a medium for energy storage and used to generate power fuel cells.

In this chapter, a computationally efficient two-dimensional analytical model accurately models JL-GAA SiNWFET with cylindrical geometry incorporated to detect hydrogen gas. As a result of its surrounding gate structure and larger surface-to-volume ratio, the JL-GAA SiNWFET with a catalytic palladium metal gate demonstrates superior sensitivity to the typical bulk MOSFET for detecting hydrogen gas molecules. Several sensing characteristics of the proposed gas sensor are studied in order to establish which electrical parameter varies most in hydrogen gas. All studied electrical parameters are threshold voltage, electron concentration, surface potential, subthreshold current, and hole concentration (charge concentration). The presence of hydrogen gas molecules causes a noticeable change in the surface potential, the threshold voltage, the charge concentration, and the subthreshold current. The sensor shows reduced variation in I_{ON} current compared to other electrical metrics. The proposed hydrogen gas sensor's threshold voltage and subthreshold current sensitivity are also studied. The sensitivity of a change in subthreshold current to a shift in the work function of the gate metal as a result of gas molecule reactivity at the surface of the gate catalytic metal is much higher than the sensitivity of a change in threshold voltage. Operating a device in the subthreshold range is also desirable since it offers a low-cost, low-power hydrogen gas sensor. Table 2 reveals that JL-GAA-SiNWFET exceeds bulk MOSFET and GAA-MOSFET by 124.51% and 51.65%, respectively, in terms of the subthreshold current sensitivity ($S_{I_{OFF}}$). JL-GAA SiNWFET's efficient gate control, improved short-channel characteristics, and large surface-to-volume ratio make it a promising choice for compact, ultrasensitive, low-cost, low-power, CMOS-based hydrogen gas sensors. Due to its high sensitivity and ease of manufacture, the JL GAA SiNWFET sensor with a palladium catalytic metal gate is a potential hydrogen gas sensor. It can be used in industries like nuclear reactors, petroleum refineries, fuel cells, space launching, medical diagnostics, and leak detection. Following an analysis of the electrical characteristics of the JL-GAA SiNWFET's sensitivity to hydrogen gas, next chapter focuses on the effect of various biomolecules on the dielectric modulated triple hybrid metal gate GAA-JL NWFET sensing applications.

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CHAPTER -3

Sensitivity Analysis of Biomolecule Nano-Cavity Immobilization in Dielectric Modulated Triple Hybrid Metal Gate-All-Around Junctionless NWFET Biosensor for Detecting Various Diseases

Abstract

In this objective, a novel biomolecule nano-cavity immobilization in dielectric modulated triple hybrid metal gate-all-around junctionless (JL) NWFET has been explored to improve sensitivity for detecting various diseases. A comparative analysis of dielectric modulated triple hybrid metal gate all around JL-NWFET biosensor has been carried out with unique and double hybrid metal gate transistors immobilizing different biomolecules (neutral) like Streptavidin, ChO_X, APTES, Uricase, and Biotin in the nanogap-cavity region. The simulation results were analyzed using atlas-3D device simulation tool. Effect of neutral biomolecules on devices output characteristics such as switching (I_{ON}/I_{OFF}) ratio, shifting threshold voltage (ΔV_{th}), intrinsic voltage gain (g_m/g_d), drain-off sensitivity ($S_{I_{OFF}}$), subthreshold slope, transconductance (g_m), output conductance (g_d), surface potential, and output resistance($1/g_d$) have been studied. Sensitivity of the proposed device for detecting a specific neutral biomolecule was examined using a drain-off-current ratio metric system, and the results were compared with available works. The result shows that higher sensitivity has been investigated in a triple hybrid metal gate than a unique and a double hybrid metal gate transistor in addition to existing works, as we have inspected under the results and discussion section. Also, compared to GAA, the novel junctionless gate stack GAA structure has a lower off-state current, making it a promising candidate for future low-power and energy-efficient devices. Due to the different work-function materials near the source/drain regions suppress/overcome short channel effects and quantum mechanical tunnelling caused by hot-carrier and electron scattering due to a high electric field and saturation velocity. So, we can say that the proposed device in this objective can be used to diagnose and detect early, rapidly transmitted biomarker diseases like breast and lung cancer (APTES) and uric acid in human blood serum (Uricase).

3.1 Introduction

In recent years, biomolecular species detection has been regarded as essential research for identifying biomolecular species that are utilized to identify biological diseases like cardiovascular [1], breast cancer [2], ovarian cancer (viral infections), Alzheimer's [3], Ebola, and others[4]. However, on-line monitoring is not feasible when biomolecules like Uricase, APTES, Streptavidin, tumor markers, ChO_X, antigen-antibody complexes and Biotin are detected using conventional techniques like spectrometry, optical measurements, and surface plasmon resonance requires a significant amount of time and is very expensive [5]–[8]. For instance, utilizing an optical microarray reader to identify the DNA sample complex is quite expensive and results in unnecessary enabling DNA labels in a single microarray area[4], [9]. Additionally, these labelling methods add complexity and delay to the sample preparation process[10]. In addition to the complexity of device production, there is an increasing need to open conservative clinical laboratories in rural areas, military bases, and remote areas to detect biomolecules[11]. To address these and other shortcomings, there is a need to use newer and advanced FETs[12]. The field-effect transistors (FET) sensors, based on the interaction of biological or chemical elements directly connected to the electric field, marked the beginning of the recent development in the 1970s[13]. A FET biosensor is an analytical equipment that can detect biological species such as proteins, streptavidin, enzyme, blood cell, DNA, etc. [14]–[16]. FET biosensors have been found to have applications in many fields as diverse as biological diagnosis, illness progression, point-of-care treatment monitoring, biomedical research, drug discovery, forensics, food control, automated manufacturing, and environmental monitoring[15], [19], [20]. Because of their high sensitivity, mass production, low cost, downsizing, and compatibility with current CMOS technology, biosensors based on FETs have emerged as possible candidates[20], [21]. With a NWFET-based biosensor, "boosting and analyzing circuits can be integrated on the same chip, saving both cost and real estate" ”[22]. Because of its ultra-low off-state leaking current when compared to FinFET, nanowire structure is now viewed as a possible choice for a future generation of sensing devices[23]. This is why NWFET-based biosensors have sparked so much attention in recent years. There is a significant need for innovative technologies that can assess biological components such as biomolecules and cells speedily and accurately while also being label-free[12]. Recent research has proposed using dielectrically modulated(DM) double and triple-gated nanowire field effect transistors to overcome the ionic (Nernst) sensitivity limit in single-gated field effect transistors[24], [25]. It has already been reported that an experimental demonstration of a dielectrically controlled nanogap-embedded biosensor was carried out[18], [26]. A revised version of ion-sensitive field effect transistors (ISFETs) has also been used to recognize biomolecules such as Proteins, DNA, and biomarkers that indicate the presence of certain diseases[27]. However, there are significant issues with reliably detecting biomolecules with ISFET [28]. Electrical signals generated by the ISFET biosensor are determined to depend on the sample solution's ionic concentration [29], which is described by the value of the Debye length. In addition, the interaction potential is responsible for the conductance modulation in the ISFET sensor, and the buffer solution's high ionic strength can partially screen this potential[2], [28], [30]. This

screening is completely dependent on the Debye–Hückel length[28]. Therefore, field-effect transistors (FETs) are good candidates for sensors and diagnostic instruments [31].

Such devices based on field-effect transistors (FETs) are appealing for realizing label-free, fast, inexpensive, simple, and real-time analysis of bioanalytes because of their ability to directly translate the interaction with target molecules on their surface into a readable signal and because they are compatible with advanced micro- and nano-fabrication technology[21], [28]. Nanometer-sized molecules can be detected using NWFET-based sensors [32], [33]. For instance, the size of numerous biological entities such as atoms (0.1 nm), DNA (1 nm), proteins (10 nm), and viruses (10-100 nm) can be measured using nanometers[34]–[37]. The proposed device's detecting site/nano-cavity has a thickness of 10 nm, which is compatible with the dimensions of biological molecules such as DNA, atoms, and proteins. Previous investigations have shown that low-power silicon nanowire-based inversion mode MOSFETs can detect DNA [36,37], proteins [4], [7], [38]–[41], and pH values [12], [42]. When fabricating conventional FET biosensors at ultra-small scall device size, critical issues like short channel effect (SCEs), drain-induced barrier lowering (DIBL), hot-electron effect, threshold voltage instability, impact ionization effect, sub-threshold swing, and gate tunnelling current arise [7], [24], [43], [44]. For example, it can be challenging to keep the drain on current (I_{ON}) high while keeping the drain off-current (I_{OFF}) low when the device dimensions are on a small scale which leads to quantum mechanical tunneling and the short channel effect (SCEs) [45], [46][47]. Super doping profiles caused by "diffusion of impurities between a p- or n-type drain/source (D/S) region and an n- or p-type substrate/body region raise an interface charge which creates parasitic gate resistance in the fabrication of ultra-small-scale devices" and develop abrupt doping profile between source, channel and drain[14], [48], [49]. In order to control SCEs and improve electrostatic gate controllability, recent research has developed multi-gate, junctionless device structures, including Surrounding-Gate-FET, Fin-FET, and Double Gate (DG) FET [24], [44], [50]. Since, Junctionless devices have uniform doping from source to channel to drain, which can either be n- n- n or p- p -p-type[51], [52]. It simplifies the fabrication of the proposed device, lowers SCEs, and enhances the device's I_{ON}/I_{OFF} ratio [53]. As CMOS continues to shrink, thinner and thinner gate dielectrics are needed [47]. However, direct tunnelling limits the thinning of the oxide layer, increasing the leakage current. As a result, these impacts produce substantial reliability concerns and performance degradation over time. To overcome problems associated with gate oxide thickness in the fabrication of small-scale devices, silicon dioxide (SiO_2) gate insulators should be replaced by high-k dielectric gate oxide materials such as hafnium oxide (HfO_2,=25) along interface oxide (SiO_2) using gate engineering device scaling while maintaining effective oxide thickness (EOT) constant [44], [48], [54], [55]. HfO_2, a high-k dielectric material, has been used with SiO_2 in the proposed structure to reduce leakage current[56], [57], allowing for more efficient carrier production and higher performance. It has been shown [58] that introducing an ultrathin SiO_2 interlayer between the high-K layer and the silicon substrate improves the quality of the interface by decreasing the trap density and ensuring stability.

In addition to the trend toward the miniaturization of devices, there is a growing demand for the establishment of conventional clinical laboratories in rural, remote, and military regions for

the label-free, fully electronic detection of biomolecule species [41]. The nanometer-sized molecules are detectable via field-effect transistors (FETs) sensors. They are more sensitive, can be detected electronically without a label, and may be produced in large quantities [59]. It is possible to synthesize/ characterize biomolecules like uricase and ChOx biomolecules in the form of nanometer size using Transmission Electron Microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) instruments[60]–[62] to develop device sensitivity and selectivity. Because of this, the sensing device needs to have a lower feature size to provide suitable sensing capabilities for very few biological or chemical species. The detecting devices need to have a reduced feature size in order to provide a sufficient sensitivity level in order for it to be able to detect such small chemical or biological species. The size of a variety of biological species is depicted in **Figure 3. 1.**

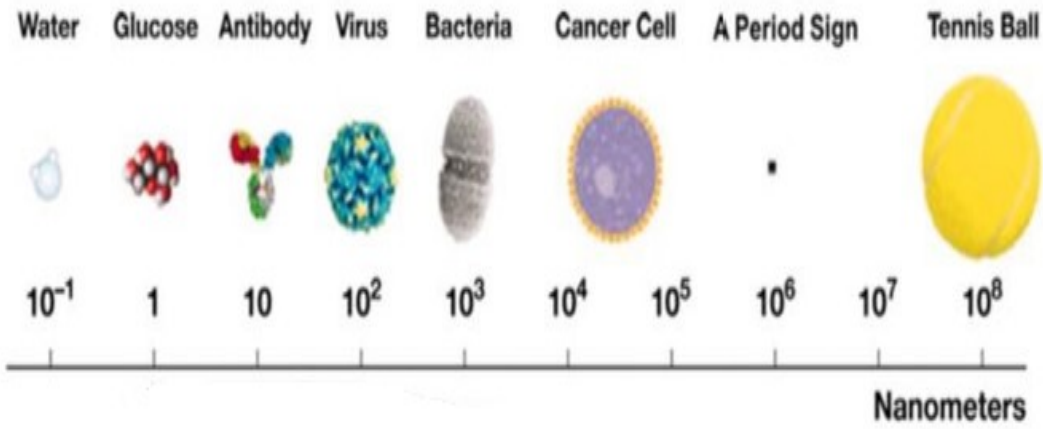

Figure 3. 1. Illustrates the size of biological species for characterization and electrical detection with NWFET-based biosensors [61].

In this chapter, Junctionless (JL) triple hybrid gate dielectric modulated GAA SiNWFET has been proposed as one of the viable alternatives [63], [64] to alleviate shout channel effects and to study the impacts of a biomolecule on the electrical characteristics of the device using the atlas-3D device simulation tool to analyze a specific biomolecule for the detection of various diseases. A triple material gate (TMG)-FET is made up of three laterally connected metal gates with different work functions. It is commonly known that the performance of a device would decline if high-k dielectrics were placed as the gate material on a silicon substrate[55]. The increased fringing electric field would limit the gate control and make FET-based biosensors less sensitive[21]. In order to circumvent this constraint, an engineering technique known as gate stacks (high-k+low-k) has been described [65], which maintains the oxide/channel interface strength [56], [66]. In order to increase the biosensor's sensitivity, we have implemented gate oxide stack engineering, a triple material gate, and a drain-sided cavity into our device structure[67]. For this reason, a triple metal gate, gate oxide stacked JL-GAA SiNWFET-based biosensor is developed here to detect low concentrations of biomolecules with improved sensitivity[67].

3.2 Device Structure and Simulation Models

3.2.1 Device Structure

Figure 3.2. depicts the proposed device architecture. Here, L_1 (6nm), L_2 (8nm), and L_3 (6nm) are the gate lengths of G_1, G_2, and G_3, respectively, and L_4 (10nm) are the length of the nanogap cavity and silicon dioxide (SiO_2), which are near the drain and source ends, respectively, and L (20nm) is the length of high-k oxide (HfO_2) and an interface oxide layer (SiO_2). T_1, T_2, T_3, and T_4, represent the thicknesses of the metal gate, biomolecule cavity, hafnium oxide, and interface (SiO_2) oxides, respectively, while 2R represents the thickness of the silicon film. Here, a high-k/low-k dielectric material serves as the gate oxide stack to enhance the sensor's sensitivity[14]. In modelling the THM-GAA-JL-NWFET biosensor, the tunable work function (each gate metal has a different work function), as shown in **Table 3.1**, including device physical parameters, has been considered for this study. High dielectric materials like hafnium oxide were employed to mitigate the ionization and hot-carrier effect caused by a strong electric field near the drain end (another type of SCE)[47], [68] threshold voltage fluctuation, parasitic gate resistance, and channel doping variation [56]. A decrease at the drain end regulates the electric field, and this decrease occurs when the gradient of work functions increases from the source to the drain [47]. In a nanogap cavity region, the target biomolecules are assumed to be uniformly immobilized and interact with the device. The air cavity ($\epsilon = 1.0$) was also taken into consideration by introducing its dielectric constant in the cavity [48] and is not reacting with SiO_2 and HfO_2 oxide materials [70], which leads to produce a unique trace of a binding event as a result of a change in electrical properties. Biomolecules such as (APTES, $\epsilon = 3.57$), Choli oxidase (ChO_x, $\epsilon = 3.30$), (Streptavidin, $\epsilon = 2.10$), (Biotin, $\epsilon = 2.63$) and (Uricase, $\epsilon = 1.5$) were simulated interchangeably by presenting their dielectric constants in the cavity region. A possible flowchart for the fabrication of JL-GSTMGAASiNWFET is illustrated in **Figure 3. 5**.

To obtain a tolerable threshold voltage variation and reduce bandgap separation, a high doping concentration (N_D=1x$10^{19}$$cm^{-3}$) was applied consistently in modelling THM-GAA-JL-NWFET biosensor through the channel from source to drain [71], [72]. **Table 3. 1** presents various device parameters that were considered for this study.

Table 3. 1: Designed parameters of GAA-JL-NWFETs with double and triple hybrid metal gates [59].

Physical Device Parameters	**DHM-GAA-JL-NWFET**	**THM- GAA-JL-NWFET**
Channel length (nm)	20.0	20.0
Oxide thickness, HfO_2 & SiO_2 (nm)	1.5 & 0.3	1.5 & 0.3
Source Oxide thickness SiO_2(nm)	1.0	1.0
Source Oxide length, SiO_2 (nm)	10.0	10.0
Length of the cavity (nm)	10.0	10.0

Length and thickness of Source/Drain (nm)	10.0		10.0		
Thickness of the cavity (nm)	1.0		1.0		
Thickness of silicon film (nm)	10.0		10.0		
Source/Drain & Channel Doping (N_D+)	$1x10^{19}cm^{-3}$		$1x10^{19}cm^{-3}$		
HfO_2 and SiO_2 dielectric constants	25.0 & 3.9		25.0 & 3.9		
Metal Gate work functions (eV)	4.89	4.50	4.96	4.86	4.50

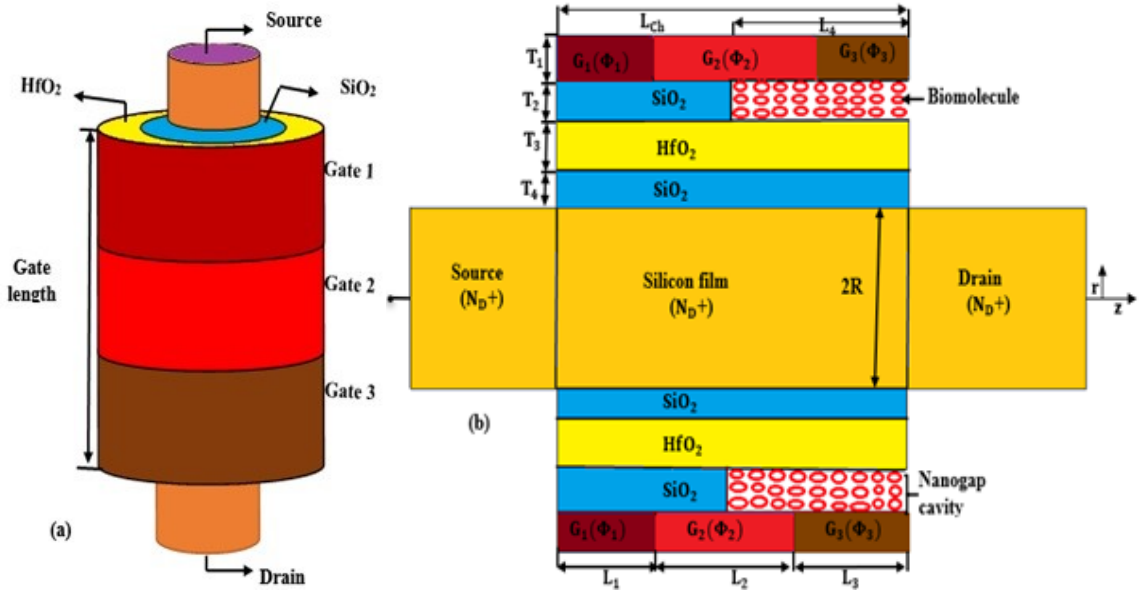

Figure 3. 2. Depicts **(a)** 3D schematic diagram and **(b)** 2D cross-sectional interpretations of n-substrate channel JL-DM triple-hybrid metal gate-all-around NWFET biosensor [69].

3.2.2 Device Simulation

Numerous simulations were performed utilizing the materials specified in **Table 3.1.** Due to the effects of high doping, electron concentration, and hole concentration, we employed the carrier-carrier scattering (CCSMOB) [72] model in our simulation. Boltz-man transport equations and Shockley–Read–Hall (SRH) also accounted for minority carrier recombination under semiconductors without impact ionization model [73]. The drift-diffusion model describes drain-current as a function of drain-voltage, incorporating device surface potential that meets model equations. The drift-diffusion model describes drain-current as a function of drain-voltage, incorporating device surface potential that meets model equations. The ATLAS TCAD tool's default drift-diffusion model [43] describes the density of electron and hole change due to transport, generation, and recombination processes in the simulation [45]. Boltzmann Transport approximation Equations [74], [75] were used for accurate numerical simulation results. The SHR recombination lifetime model [72], [76] determines carrier lifetime, which can be used with the continuity equation to create carriers and recombinations. The Shockley–Read–Hall (SRH) model [77] not only describes the statistics of recombination and generation of holes and electrons in semiconductors that occur as a result of the trapping

process, but it also explains how they are generated. CVT model simulations analyzed parallel and perpendicular field-dependent carriers and doping-dependent mobility [73]. The model is not considered a quantum effect because the channel radius is not less than 5nm.

3.2.3 Suggested fabrication steps for a semiconductor device

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is an integral part of modern electronics that can be made differently. The group lead by Colinge at Ireland's Tyndall National Institute developed the first functional junctionless transistor using a nanowire-gated register design [23]. Currently, various groups have fabricated junctionless transistors. Current CMOS technologies involve over 200 fabrication steps[78]. In this topic, a feasible and relatively simple process flow chart for a triple-gate junctionless gate-all-around field effect transistor (TGJLGAAFET) is illustrated in **Figure 3. 3**. The process involves a series of steps that include [25] procedures.

- Wafer processing to produce the appropriate substrate type.
- Photolithography is used to identify each region accurately.
- Steps for adding/modifying materials include oxidation, deposition, and ion implantation.
- Etching is used to remove materials from wafers.

a) Wafer Processing

Wafers used in CMOS technology must be of an extremely high purity level because they contain the technology's initial components[23], [46], [78]. The wafer has to be manufactured as a single-crystal body made of silicon, with as few defects or impurities caused by parasites as is humanly possible. In order to achieve the necessary level of resistivity, the wafer needs to have the correct quantity of doping impurity associated with it [79]. The Crystal growth method is commonly employed for this purpose. In this setup, molten silicon is slowly withdrawn while revolving around a crystalline silicon seed. This process creates a substantial single-crystal cylindrical "ingot"(iron alloy) from which wafers can be sliced. Polishing and chemical etching of the wafer repair any surface damage introduced by the slicing process[80].

b) Photolithography

It refers to the technique of accurately transferring information about a circuit design upon a wafer. The layout comprises polygons representing several layers, including polysilicon, contacts, n-wells, source/drain areas, and so on [23], [81]. A precisely controlled electron beam first writes the layers or patterns onto a transparent glass mask[82]. A photoresist is used to coat a wafer, and then ultraviolet light is employed to project the pattern into the wafer through a mask. After the photoresist has been exposed, it is etched. Thus, photolithography combines multiple processes into a single cycle. The step includes cleaning, preparing, applying photoresist, exposing to UV light and developing, etching, and finally removing the photoresist[23], [78].

c) Oxidation

On the surface, silicon will produce a uniform oxide layer that will cause very little lattice strain. HfO_2/SiO_2 interface acts as a protective covering in various fabrication phases and serves as a gate dielectric. SiO_2 is formed by immersing exposed silicon in an oxidizing environment such as oxygen at temperatures ranging from 900°C to 1150°C. The type, temperature, and doping of silicon all influence oxide formation. The oxide thickness has an effect on the current handling capabilities of the devices, as well as the noise and dependability of the chip[78], [83].

d) Ion Implantation

Ion implantation refers to the process of implanting dopants into an exposed silicon area using an accelerated, high-energy beam of ions[84]. The degree of doping depends on the depth and length of the implantation. The beam's intensity is set at a constant rate that is proportional to the silicon area's depth. Having ions implanted into silicon can cause significant damage to the lattice structure[85]. As a result, silicon is heated from 900°C to 1150°C for 15 to 30 minutes to re-form the lattice bonds. This is known as annealing. As a result, annealing is performed only once after all implantations have been completed[23].

e) Deposition and Etching

In order to fabricate a device, it is necessary to deposit materials such as polysilicon and dielectric materials that act as a barrier between the interconnect layers and the metal layers that serve as interconnects. Typically, wafers are placed in a furnace with a gas that creates the material through a chemical reaction, a process known as "Chemical Vapour Deposition at Low Pressure (LPCVD)" [86]. Etching is a technique used to remove unwanted parts of a material. Both chemical and physical etching methods can be utilized in order to achieve this result. One example would be using plasma etching to remove material from a silicon dioxide layer in order to form a gate electrode for a MOSFET construction. It is an essential process that must be managed with precision [23], [78], [79]. Etching times, materials, accuracy, and selectivity need to be considered. The ability to precisely regulate the material properties and dimensions through deposition and etching processes is crucial in MOSFET production.

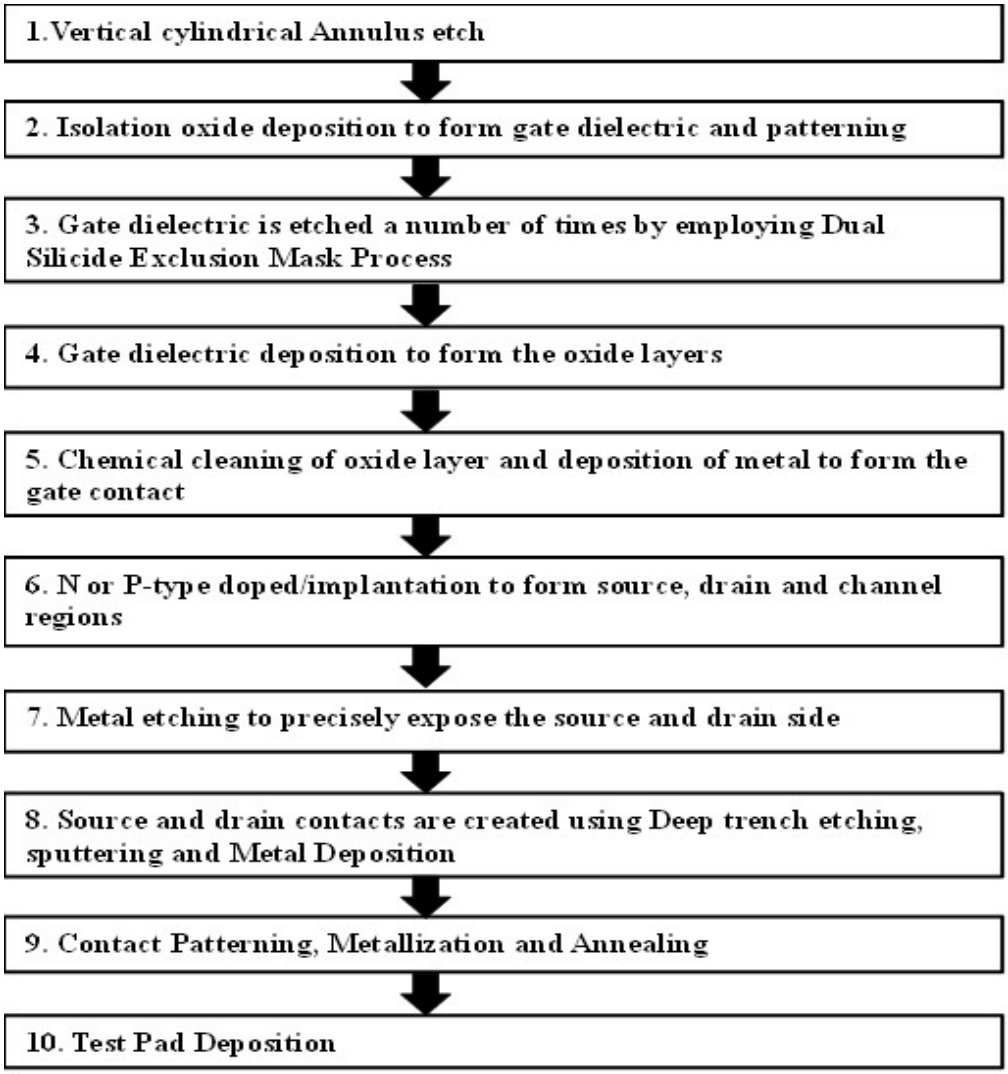

Figure 3. 3. illustrates the suggested fabrication step flow chart [23], [78], [83].

Terminology of the above steps

Step (1): Formation of light-doped silicon cylindrical body/substrate over the highly doped n^+ silicon drain extension and creation of isolation layer to form the oxide layer for fabricating the base for the vertical surrounding gate NWFET biosensor (pilar formation)[23], [83].

Step (2, 3&4): Formation of gate stacking to deposit SiO_2 using dry oxidation to form high-k oxide thin film at a temperature between 900^{o}c -1150^{o}c and then HfO_2 formation using atomic layer deposition (ALD) and electron beam vaporization(e-beam) at temperature 300^{o}c-500^{o}c (**to form gate stacked oxide layer)**[78], [83]**.**

Step (5): Gate is carefully deposited over the gate oxide layer and is etched multiple times to deposit triple metal and form a common electrode; (**triple gate formation-sub process)**[78]**.**

Step (6): Formation of highly doped n^+ silicon source node using high energy ion-implantation process for the controlled deposition of dopant at 100^{o}c -200^{o}c followed by annealing carried out at high temperature 900^{o}c-1000^{o}c; (**apply thermal annealing-Sub process)**[83].

Step (7, 8&9): Formation of source and drain electrodes using deep trench etching and sputtering technique, whereas the excess metal is etched and removed using masking and dry etching; (***apply*** **Deposition → Annealing → Metalization-Sub process)**[23], [83]**.**

Step (10): Finally, damage assessment and testing should be done.

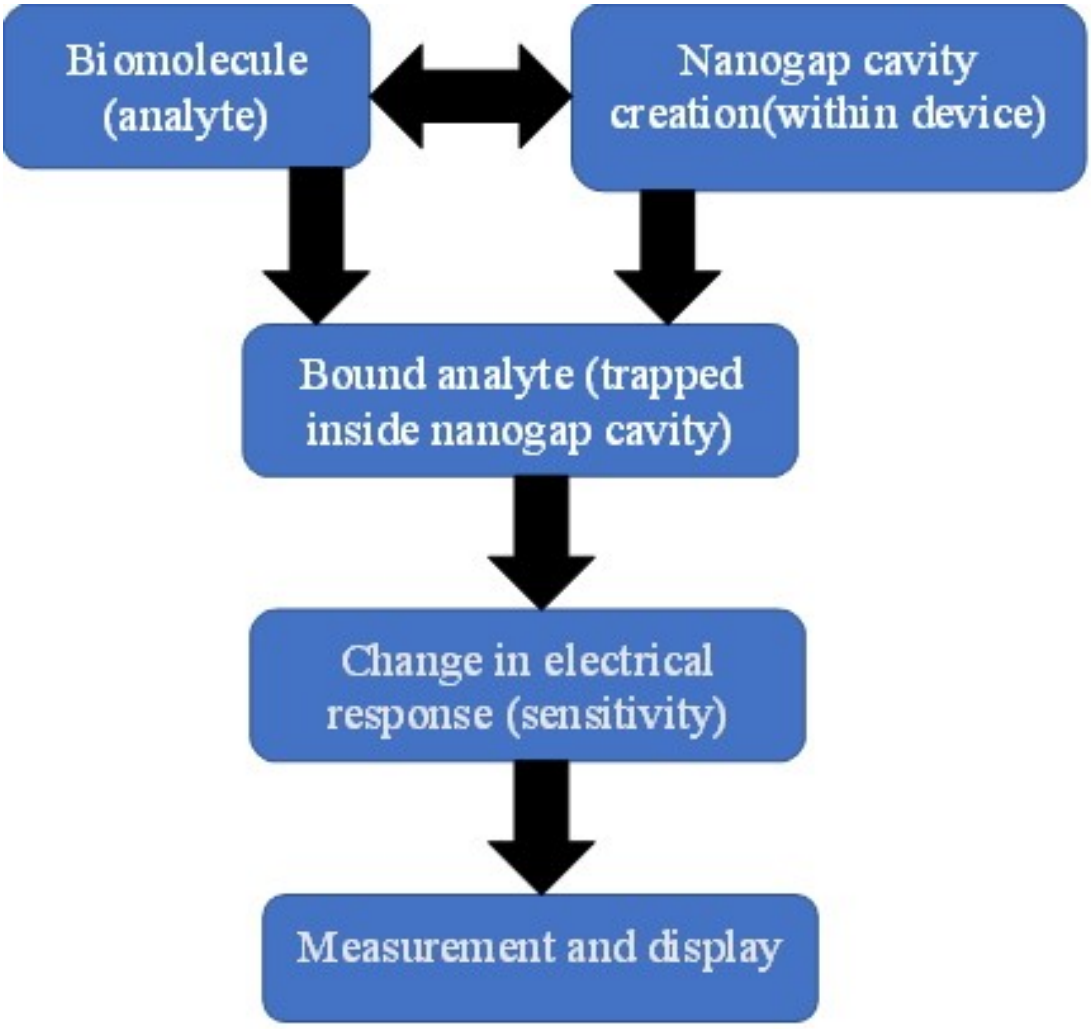

Figure 3. 4. Flowchart illustrating the biosensing principle [79].

Differences in drain current for single, double, and triple hybrid metal gates in identical conditions (apart from gate work functions) are shown in **Figure 3. 5**. Since the triple hybrid metal gate has a lower parasitic gate resistance than the single and double hybrid metal gates, the tunnelling current for the triple hybrid metal gate is significantly lower. The higher work function region of $G_{1(\Phi)}$ improves gate control and induces downside band bending, which creates a larger electric field surrounding the source-channel tunnelling junction, reducing the tunnel width from source to channel[47].

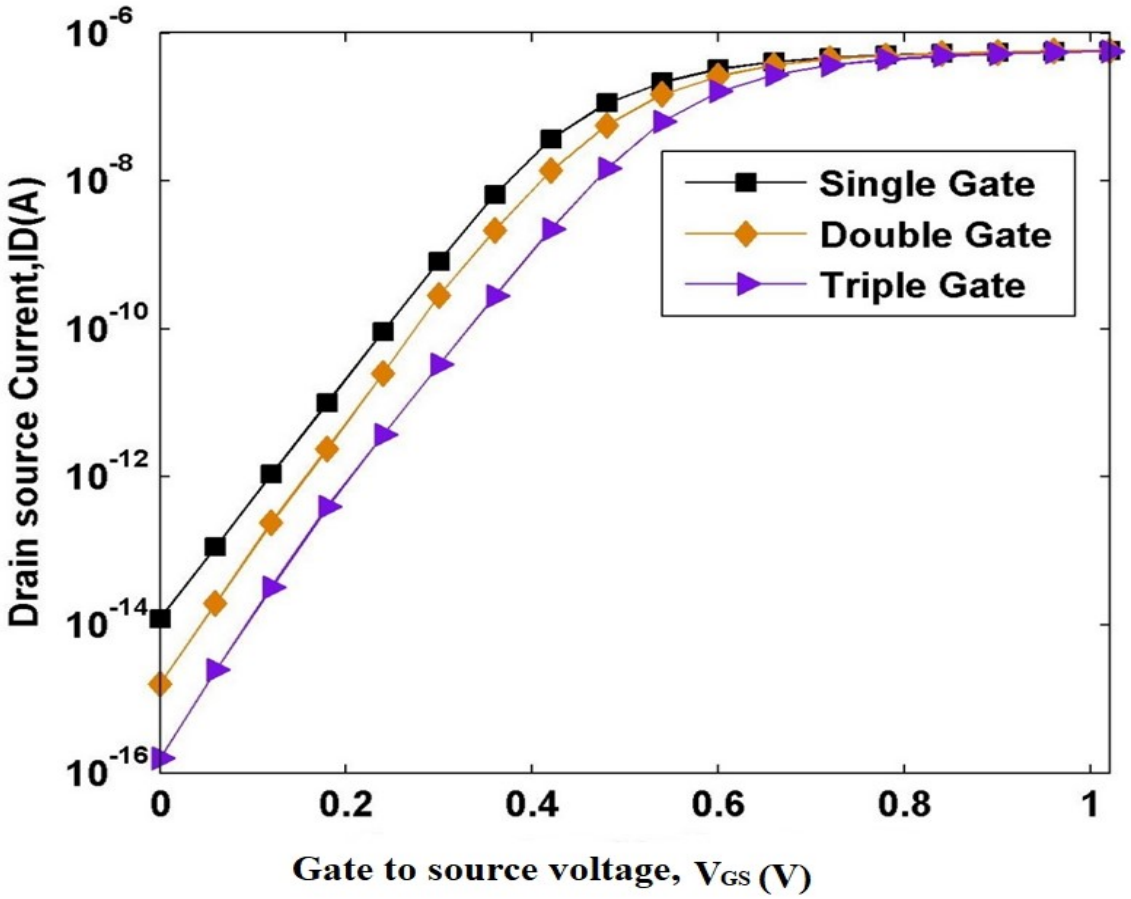

Figure 3. 5. Shows the simulation results of I_D vs V_{GS} for n-substrate channel dielectric modulated unique, double, and triple hybrid cylindrical metal gate JL-NWFET in a log file at (V_{DS}=0.05V) [59].

3.3 Results and Discussion

3.3.1 Comparative Analysis on Dielectric Modulated Double- and Triple-Hybrid Metal GAA-JL-NWFET-Based Biosensors on Electrical Transfer Characteristics

Here, we explore how the proposed biosensor device responds when introducing immobilized charged biomolecules. The nanogap cavities are assumed to be wholly and uniformly filled with a neural biomolecule. The immobilization of biomolecules inside the cavity affects the electric field and gate oxide capacitance, which in turn changes the device output characteristics[79]. **Figure 3. 6**(a) depicts the influence of biomolecules on the subthreshold slope in both devices. Since the biomolecule dielectric constant and the metal work function modulate electrostatic gate control, reducing the threshold voltage roll-off through the channel, as seen with high-k materials, reduces subthreshold swing [14], [87]. A decrease in subthreshold swing value indicates improved switching performance in triple hybrid metal gate devices than single and double gate devices. For instance, the subthreshold slope for a double hybrid metal gate transistor is 6.90×10^{-2} V/decade, and that of a triple hybrid metal gate

transistor is 6.50x10^{-2} V/decade for APTES (=3.57) biomolecule. Research has found that the gate's work-function value also impacts the device's sensitivity. As a result of a rise in dielectric constant and different electrode work functions (Φ_{G1}), by screening out, leads to improved gate controllability, reducing the hot-electron effect and improving carrier mobility across the silicon film [84]. **Figure 3. 6(b)** depicts the influence of biomolecules on the threshold swing for both devices. When the dielectric constant increases, the threshold voltage rises because gate dielectric materials reduce threshold voltage roll-off [47], [88]. For example, for APTES ($\epsilon = 3.57$) neutral biomolecule, the threshold voltage (V_{th}) in both devices is 0.33V and 0.47V, respectively, for a double and triple hybrid metal gate at V_{GS}=1.0V and V_{DS}=0.05V, which means the triple-hybrid metal gate improved 42.42% more than the double-hybrid. This threshold voltage fluctuation (shift) suggests increased sensitivity in the triple-hybrid metal gate over the double-hybrid metal gate due to different metal gate work functions and surface potential profiles leading to uniformity carrier mobility on the channel[24]. The research shows and demonstrates that the sensitivity of a triple gate design improves significantly when compared to the sensitivity of a single or double metal gate. The difference in the gate work functions is used to deplete the charge carriers in the channel[79]. In general, multiple gates with different work functions($\Delta\Phi$) provide better control over the charge carriers flowing over the channel, influencing the device's sensitivity pattern.

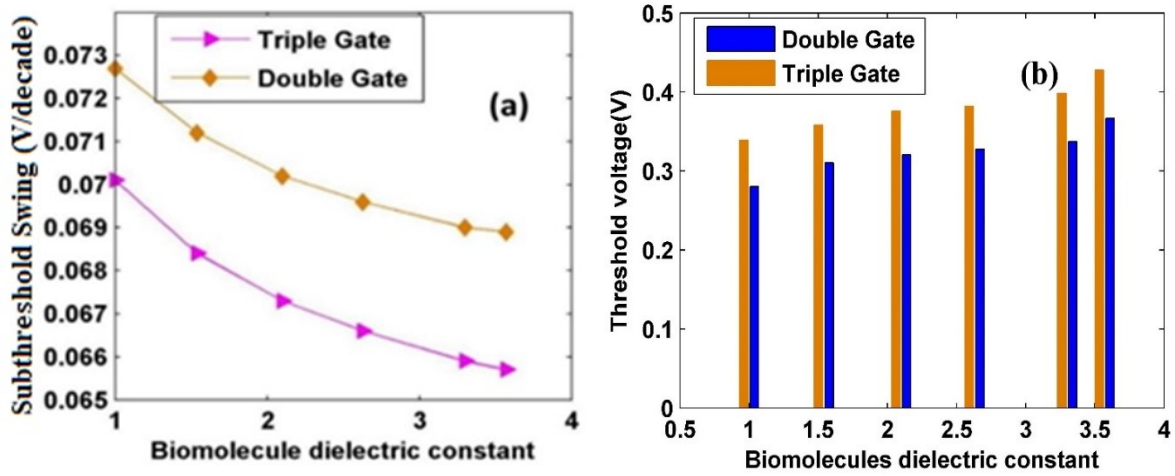

Figure 3. 6. Impacts of biomolecules on **(a)** subthreshold slope **(b)** threshold voltage(V_{th}) for n-substrate channel double and triple hybrid metal gate all around junctionless NWFET at a constant ($V_{DS} = 0.05V \; and \; V_{GS} = 1.0V$) [59].

Figure 3. 7(a) shows the influence of the neutral (APTES) biomolecule on drain current for single, double, and triple hybrid metal gate all around junctionless NWFETs. Due to the fact that the gate work function is able to overcome the parasitic resistance and increase gate capacitive controllability at thinner gate oxide, the tunnelling current in a triple metal gate is significantly lower than that of a single metal gate or a double metal gate. Furthermore, higher-gate dielectric materials reduce equivalent oxide thickness (EOT), increase gate capacitance, and lower leakage current. If the drain current is more variable, then the threshold voltage will shift more in response to a shift in dielectric constant. **Figure 3. 7(b)** depicts the effects of neutral biomolecules on leakage current in the case of double and triple hybrid metal gate devices, and the results show that as dielectric constant increases, leakage current decreases.

This is because a higher biomolecule dielectric constant increases gate electrostatic controllability by reducing electron tunnelling from the gate, thereby enhancing gate control capacitance[89], [90]. This is because a potential barrier created by a higher gate dielectric oxide in the channel region significantly reduces drain-to-source reverse tunnelling current[91]. For instance, leakage current measurements in both devices at APTES ($\epsilon = 3.57$) biomolecule are $2.32\text{x}10^{-12}$ and $1.24\text{x}10^{-13}$A for double and triple metal gate devices, respectively. The work function (Φ_{G_2}) in a device with a triple metal gate produces a barrier potential in the channel region, which increases the driving current from source to drain and reduces the high electric field and short channel effect relative to a device with a double metal gate[92]. In addition to this, the HfO_2 stack structure contributes to an increase in the channel's electron concentration by giving a greater capacitance, which in turn leads to a rise(improved) in the device's drain current (I_{DS})[56], [79]. In order to prevent electrons from overshooting their targets, triple-metal devices average out the electric field across the entire region, resulting in a greater current flow than that of a single-metal device [47]. This allows for a more consistent electric field distribution across the entire region. This can be concluded as the effect of the biomolecule on sensitivity increases in proportion to the biomolecule's dielectric constant.

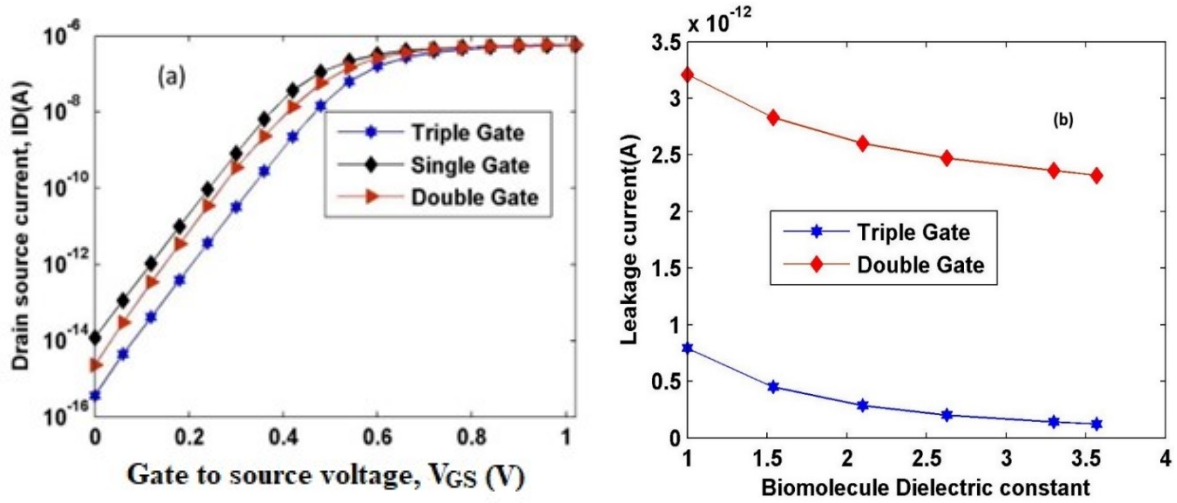

Figure 3. 7. Depicts **(a)** drain current (I_D-V_G) and **(b)** leakage current comparison, including different biomolecules for n-substrate channel double and triple hybrid metal gate all around JL-NWFET at ($V_{DS} = 0.05$V and $V_{GS} = 1.0$V), [59].

The variation in transconductance (g_m) and output conductance (g_d) with gate voltage (V_{GS}) and drain voltage (V_{DS}) for single, double, and triple hybrid metal gate-all-around junctionless NWFETs is shown in **Figure 3. 8**. The output conductance (g_d) for all devices can be calculated by derivation of drain current relative to the drain voltage at a constant V_{GS} [47].

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=\text{constant}} \tag{3. 1}$$

In a similar manner, the transconductance (g_m), can be calculated for any device by deriving the drain current in relation to the gate voltage (V_{GS}) while maintaining the value of V_{DS} constant.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \tag{3. 2}$$

Figure 3. 8(a) clearly reveals that the triple hybrid metal gate device has lower output/drain conductance (g_d) under a weak inversion region than the unique and double hybrid gates due to reduced drain-induced barrier lowering, short channel effect, and parasitic [55], [93].

In different gate engineering designs, the transconductance g_m in **Figure 3. 8(b)** is the first-order derivative of drain-source current (I_{DS}) with respect to gate-source voltage (V_{GS}) at constant (V_{DS}=0.1V) using **(eq.3.2).** In any circumstance, it is possible to observe that the transconductance first goes up when the device is in the log region but that it subsequently tends to go down when the device enters the saturation region. Since, HfO_2 high-k material in a triple metal gate with average work function improves carrier mobility and gate control over the channel region, leading to higher drain current and transconductance (since g_m is proportional to I_{DS})[47]. For example, transconductance (g_m) measurements at a constant V_{GS}=0.7V and V_{DS}=0.1V are 2.34x10^{-5}, 2.63x10^{-5}, and 2.72x10^{-5} Siemens(S) for single, double, and triple hybrid metal gate devices, respectively. Double- and triple-hybrid metal-gate enhancements are 12.39% and 16.24% compared to single-metal-gate devices. This is because the THM-GAAJL-NWFET has an engineered gate work function, which boosts electrostatic coupling in the channel, improves carrier mobility, and enhances device performance[47].

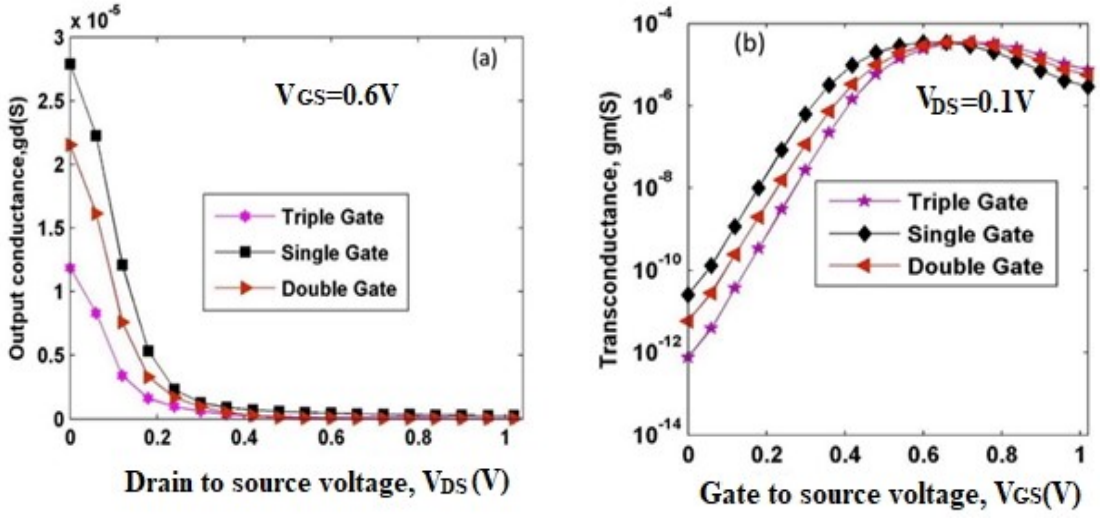

Figure 3. 8. Depicts **(a)** output conductance (g_d) and **(b)** Transconductance (g_m) comparison for n-substrate channel single, double and triple hybrid metal gate all around JL-NWFET [59].

The effect of various biomolecules on the drain-off sensitivity ($S_{I_{OFF}}$) of JL-NWFETs in single, double, and triple hybrid metal gates at V_{DS}=0.05V and V_{GS}=1.0V is depicted in **Figure 3. 9(a).** This shows that the sensitivity of a triple gate structure is noticeably higher than that of a single

or double gate structure. It clearly illustrates that when the dielectric constant decreases, the change in drain-off sensitivity increases for all devices due to lowered electrostatic gate regulating and increased tunnelling current. However, the influence of increasing dielectric constant on modulating gate electrostatic control reduces drain-off sensitivity as the dielectric constant of biomolecules increases. The effect of a neutral biomolecule on the switching ratio is depicted in **Figure 3. 9(b)**. It is evident that the change in the switching ratio (I_{ON}/I_{OFF}) increases as the biomolecule dielectric constant increases since a higher biomolecule dielectric constant suppress the tunneling current and improves gate electrostatic controllability. A higher gate work-function difference offers excellent band bending near the source end, which enhances carrier mobility[58]. When APTES ($\epsilon = 3.57$) biomolecules were immobilized in all nano-cavity regions under identical conditions, as shown in the graph, a higher switched ratio was observed in the triple hybrid metal gate devices. This higher switching ratio in the triple hybrid metal gate is due to a potential barrier created in the channel region by the gate work function, suppressing reverse tunnelling from the drain[91]. It also indicates that the device has better sensitivity when target biomolecules are immobilized uniformly in the targeted site. The sensitivity of the device when it is in a weak inversion region is referred to as the drain-off sensitivity ($S_{I_{OFF}}$), which may be calculated using (eq.3.3)[5], [38];

$$S_{I_{OFF}} = \frac{I_{OFF}[with\ biomolecule]}{I_{OFF}[without\ biomolecule]}\Bigg|_{at\ V_{GS}=0V} \tag{3. 3}$$

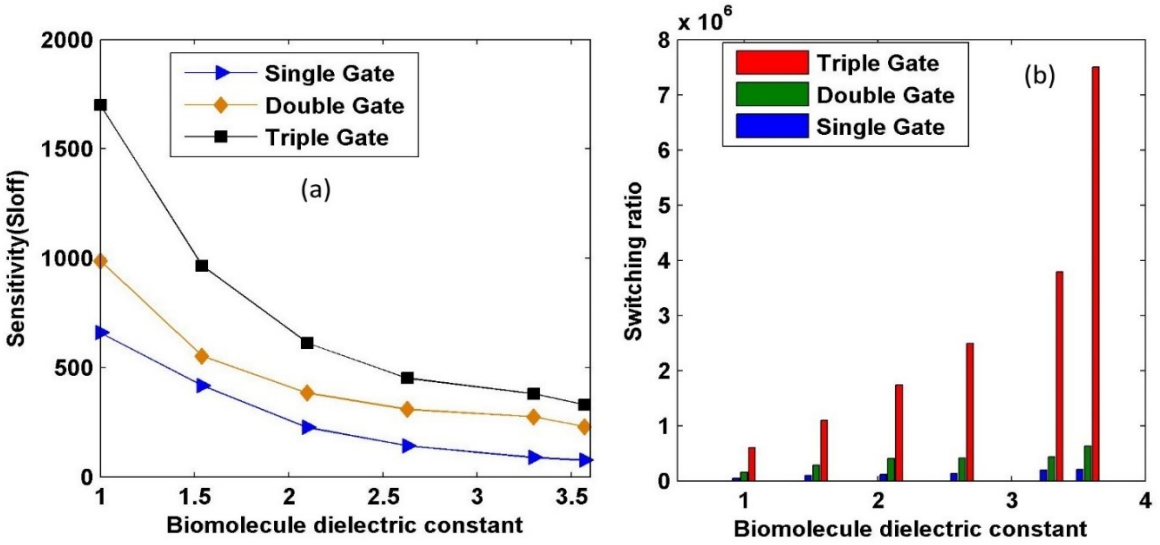

Figure 3. 9. illustrates the effect of biomolecules on **(a)** the sensitivity ($S_{I_{OFF}}$) and **(b)** switching ratio for n-substrate single, double, and triple hybrid metal gate all around JL-NWFET at ($V_{DS} = 0.05V\ and\ V_{GS} = 1.0V$) [59].

3.3.2 Sensitivity for different biomolecules

In this section, variations in various electrical parameters, such as surface potential, subthreshold current, threshold voltage, switching ratio, and transconductance, were

investigated to establish how the sensor would respond to or be influenced by a variety of biomolecules.

a) Surface Potential Based Sensing

The surface potential, which defines the threshold voltage fluctuation, is imperative to interpreting the proposed device's sensitivity following uniform biomolecule interaction in the targeted cavity. **Figure 3. 10** demonstrates the variation in surface potential profile along the channel length for different biomolecules on the THMG GAA JL NWFET. The graph shows that the lowest surface potential rises proportionately to the dielectric constant. Near the drain end, a cavity of 10 nm is considered. In the presence of a biomolecule, the presence of nanogap cavities at the drain end causes the potential to shift from lower to higher in the cavity region. When different biomolecules are filled in the cavity region, a higher variation in surface potential is observed, as illustrated in **Figure 3. 10**. The surface potential of the part of the channel (drain side) over which various biomolecules were immobilized is determined by the dielectric constant value within the nanocavity region. This value can range from lower to higher, as illustrated in **Figure 3. 10**. The surface potential on the source side of the device, which is not covered by the gate, is lower. This leads us to the conclusion that the surface potential of the dielectric-modulated THM-GAA-JL-NWFET varies more when the dielectric constant of the nanogap cavity changes. This surface potential change can also be used as a sensing metric to identify the presence of specific biomolecules trapped in the nanocavity.

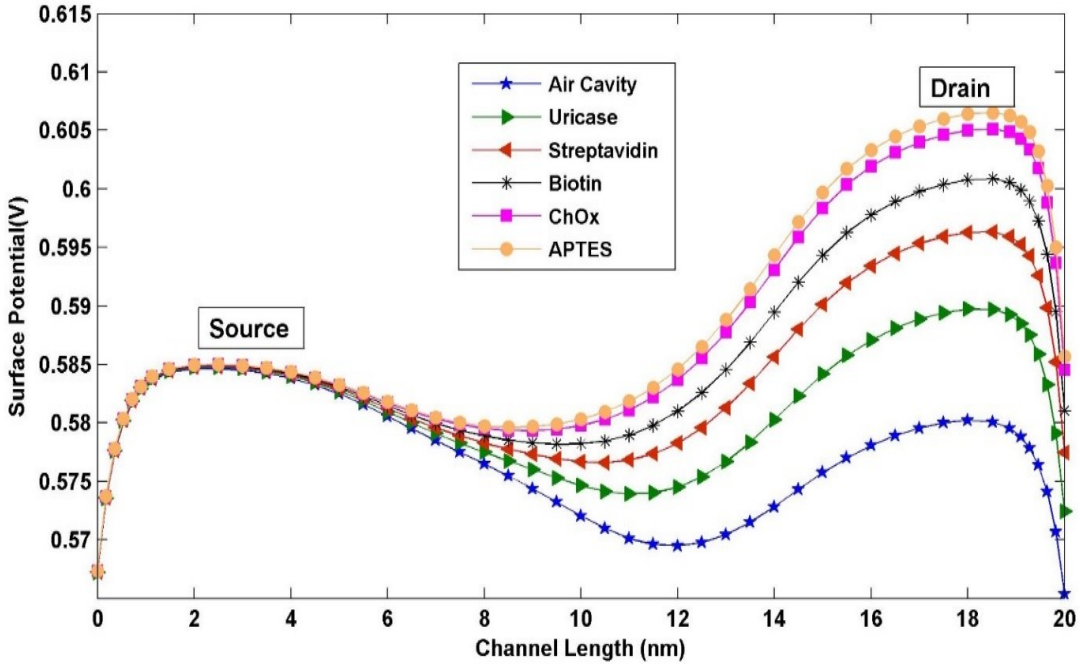

Figure 3. 10. illustrates the effect of different biomolecules on the surface potential for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05$V) [59].

b) Threshold Voltage Based Sensing

The threshold voltage is another important parameter that can be utilized to detect the presence or absence of biomolecules. It is clear that threshold voltage has a significant relationship with

the dielectric constant, as depicted in **Figure 3. 11**. The plot indicates that as the dielectric constant increases, threshold voltage also increases. Because of the increased surface potential at higher dielectric constants, a higher gate voltage is required to deplete the channel completely. Because of this, the device's threshold voltage increases as a direct consequence. Since variation in the threshold voltage immediately impacts the operation of the entire device, making it an essential parameter for any device[94]. Thus, the neutral biomolecule is detected by a threshold voltage.

When different biomolecules are present in the nanocavity, the sensitivity of the DM THM GAA JL NWFET-based biosensor can be described in terms of the shift in the threshold voltage as follows[5], [16], [95];

$$S_{V_{th}} = \left| V_{th(\varepsilon_{bio})} - V_{th(\varepsilon_{air})} \right| \quad (3.4)$$

where V_{th} (air) and V_{th} (bio) are the DM THMG GAA JL NWFET threshold voltages obtained using the constant-current method with and without biomolecules present in the nanocavity, respectively.

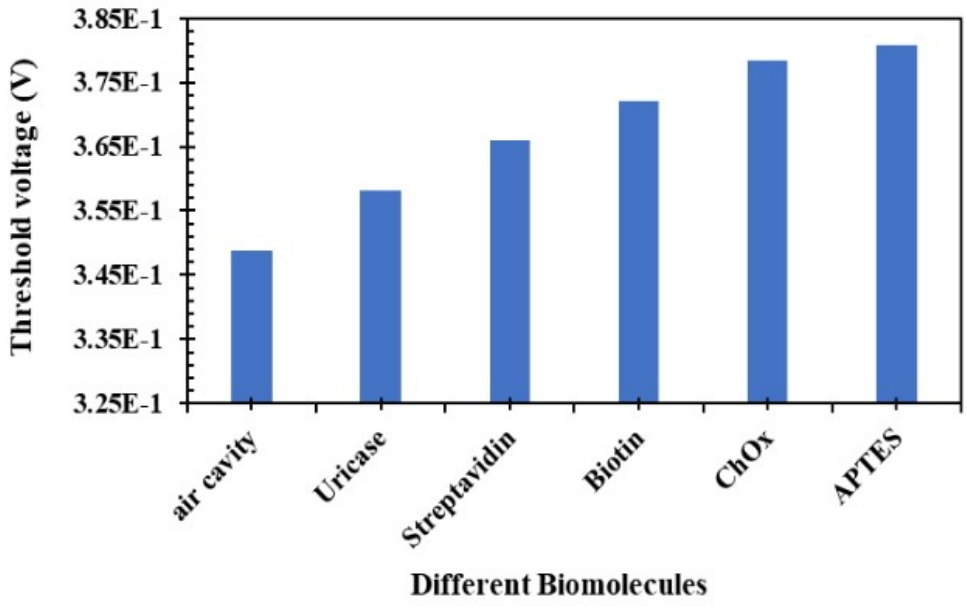

Figure 3. 11. illustrates the effect of different biomolecules on the threshold voltage for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$) [59].

The biomolecule-dependent shift in the sensitivity of the threshold voltage ($S_{V_{th}}$) is shown in **Figure 3. 12**. The plot depicts that an increase in the dielectric constant on the nanocavity region results in an increase in ($S_{V_{th}}$). The threshold voltage obtained for the designed molecular biosensor determines the ($S_{V_{th}}$). As a result, the proposed biosensor performs better at larger dielectric constants due to increased sensitivity of its threshold voltage.

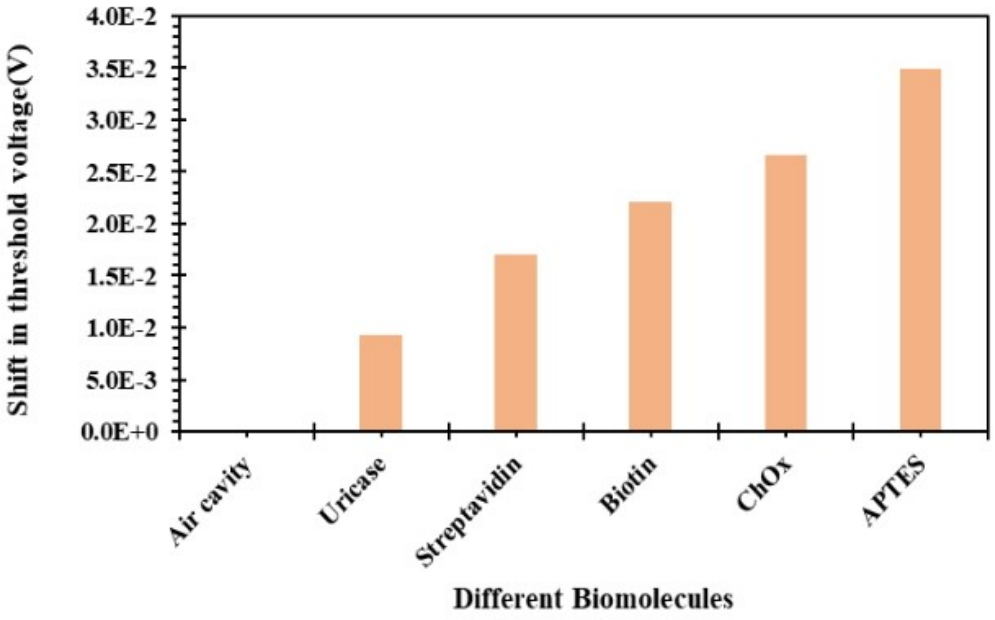

Figure 3. 12. illustrates the effect of different biomolecule shifts in threshold voltage for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05$V) [59].

Figure 3. 12 shows that the highest change in threshold voltage is approximately 34.9mV at K = 3.57 (when filled with APTES), and the minimum charge is 9.31mV at K = 1.54 (when filled with Uricase). Additionally, the relative change in the V_{th} shift values for APTES and Uricase are 274.9%, which indicates that the proposed device is highly sensitive to higher dielectric biomolecules. The absolute sensitivity profile in **Figure 3. 12** shows that the proposed device can detect biomolecules at low supply voltage, making it appropriate for low-power sensing applications.

c) OFF-current Based Sensitivity ($S_{I_{OFF}}$)

The current that runs through the device when no gate voltage is applied (V_{GS} = 0V) is referred to as the OFF-current, which is the drain current. The change of OFF-current with gate voltage (V_{GS}=0.0V) for different biomolecules on the DM THMG GAA JL NWFET biosensor at V_{DS}=0.05V is depicted in **Figure 3. 13**. This graph shows that the OFF-current drops when there is a rise in the dielectric constant of the biomolecules that are coating the nanocavity. This is demonstrated by a decrease in the OFF-current. An increment in threshold voltage due to higher dielectric constants of biomolecules reduces leakage current and hence (I_{OFF}) in the channel.

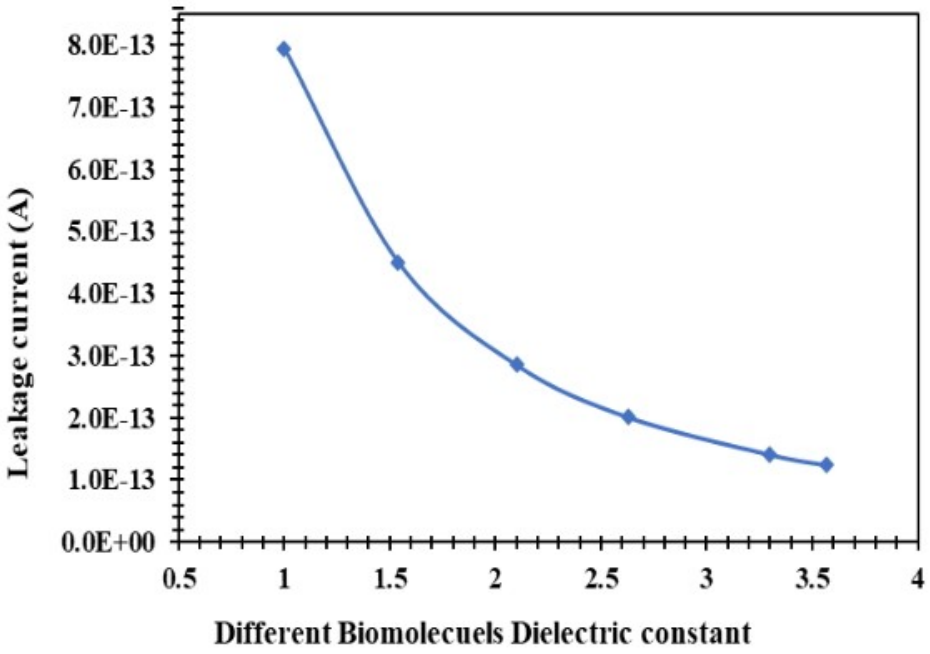

Figure 3. 13. illustrates the effect of different biomolecules on leakage current for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 0.0V$ and $V_{DS} = 0.05$V) [59].

The definition of drain current sensitivity is the ratio of the drain current I_{OFF} in the presence of biomolecules in the drain current I_{OFF} in the absence of biomolecules in the nanocavity defined in **(eq.3.3).** The difference in drain current sensitivity caused by the immobilization of a variety of biomolecules in the nanocavity region is depicted in

Figure 3. 14. When nanocavity biomolecule dielectric constant increases, drain current sensitivity plot shows ($S_{I_{OFF}}$) drops drastically. Since $S_{I_{OFF}}$ depends on drain current, it is affected by immobilized biomolecules on nanocavity. As shown in

Figure 3. 14, the drain-off current sensitivity ($S_{I_{OFF}}$) increases when the dielectric constant of the immobilized biomolecules in the nanocavity region decreases. As shown in

Figure 3. 14, the highest change in ($S_{I_{OFF}}$) sensitivity is approximately $9.66x10^2$ at K = 1.54 (when filled with Uricase), and the minimum change is $3.5x10^2$ at K = 3.57 (when filled with APTES). In addition, the proposed device is extremely sensitive to certain biomolecules in the subthreshold region, as evidenced by a 176% relative change in the ($S_{I_{OFF}}$) shift values for APTES and Uricase. Therefore, the proposed device presents a remarkable performance in terms of the current sensitivity metric at an extremely low gate-source supply voltage of 1.0V.

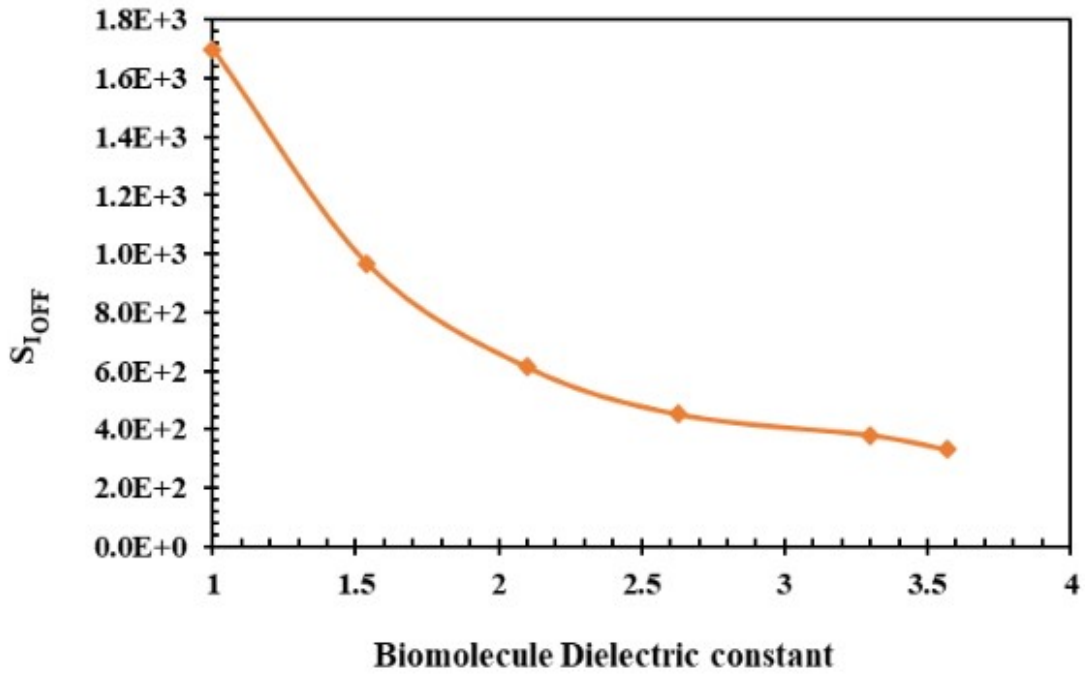

Figure 3. 14. illustrates the effect of different biomolecules on leakage current shift for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 0.0V$ and $V_{DS} = 0.05$V) [59].

d) Switching ratio (I_{ON}/I_{OFF}) Characteristics

The threshold voltage and switching ratio (I_{ON}/I_{OFF}) are the device metrics that are used in this study. These findings demonstrated an improvement in electrostatics and sensitivity with a fabrication method that was greatly simplified, a reduction in random dopant fluctuations, and a high degree of control over the doping, which was explored for both charged and uncharged biomolecules. At a constant drain bias of 0.05V, **Figure 3. 15** demonstrates the fluctuation of drain current with gate-source bias voltage for various biomolecules' dielectric constants. As illustrated in **Figure 3. 15**, an increase in the I_{ON}/I_{OFF}ratio due to differences in the biomolecules' dielectric constants represents promising sensing metrics. Here, at V_{GS} = 1.0 V and V_{DS} = 0.05V, there is a change of more than 8.5 times in the device's I_{ON}/I_{OFF} ratio from K = 1 ($6.02x10^5$) to K = 3.57 ($5.10x10^6$). Therefore, improving the switching ratio for a certain biomolecule can be used as a crucial criterion for determining how well that biomolecule can be detected or sensed. As shown in **Figure 3. 15**, when the dielectric constant of the biomolecule changes from 1 to 3.57, I_{OFF} changes by ~8.478 times. As a result, the proposed device performs excellently in terms of current sensitivity at an ultralow supply voltage of 0.05 V. As a result, the device has been described as having outstanding performance in terms of the current sensitivity metric while operating at the extremely low drain-source supply voltage of 0.05V.

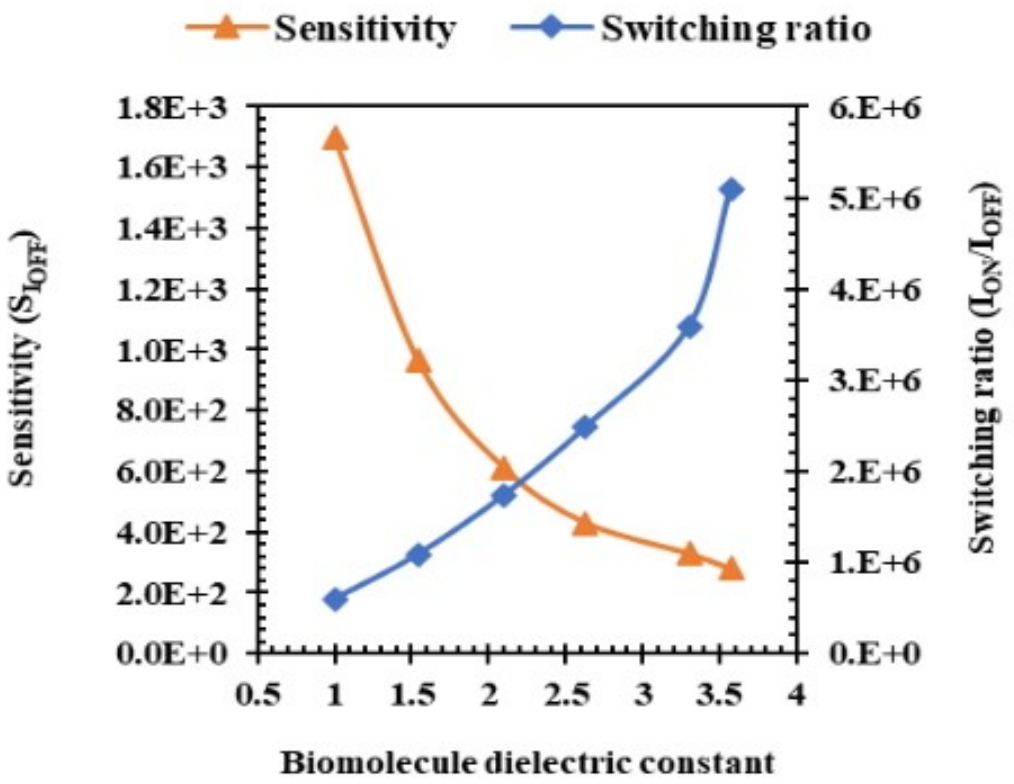

Figure 3. 15. illustrates the effect of different biomolecules on leakage current shift and switching ratio for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05$V) [59].

e) Variation of sensitivity with nanogap cavity length

This study examined how a biomolecule's location influenced the device's threshold voltage and sensitivity to biomolecule detection. The impact of cavity length on device transfer characteristics is shown in **Figure 3. 16** when various biomolecules were uniformly immobilized at the nanocavity. The simulation outcomes were obtained by employing 5, 10, and 15 nanometers cavity lengths while maintaining the same gate length and nanogap cavity thickness. A significant rise in shifting threshold voltage (ΔV_{th}) is observed when the cavity length is increased. As depicted in **Figure 3. 16**, the shift in threshold voltage (ΔV_{th}) is lower at 5 nm cavity length than 10 and 15 nm. This is because a very small number of biomolecules is implanted in the cavity region, contributing negligibly significant change to the change in the threshold voltage[5], [38]. As illustrated in **Figure 3. 16**, the variation in threshold voltage increases when the length of the nanogap cavity increases. This corresponds to the halfway point of the gate length. Since the length of the cavity is dependent on the biomolecule's dielectric constant that is to be detected (for example, APTES and ChO_X, their dielectric constants are between 3-4)[38], the sensitivity would be higher for a high biomolecule's dielectric constant than the other lower dielectric constant biomolecules to be immobilized in the nanocavity region. In light of this, it is critical to be aware that the gap in the nanoscale size substantially impacts the electrical characteristics of the FET. I_{ON} reaches its maximum value/saturates when the gate length is almost wholly covered by a higher dielectric biomolecule constant and threshold voltage roll-off (threshold voltage fluctuation) is nearly

constant. This combination causes a change in threshold voltage decrease due to small band bending amplitude in the case of a higher biomolecule dielectric constant. The channel is "pinched OFF" at the drain end, which causes maximum drain current and leads to current saturation behavior[96] in the case of higher dielectric biomolecules being immobilized in the nanocavity. Because of this, the threshold voltage shift becomes less pronounced when $\frac{L_{gate}}{L_{nanogap}} > 0.5$, since the change in threshold voltage reaches saturation level. According to the findings of this investigation, a more significant threshold voltage variation (ΔV_{th}) was seen at a cavity length of 10 nm (midway of gate length) compared to other cavity lengths, as depicted in **Figure 3. 16**.

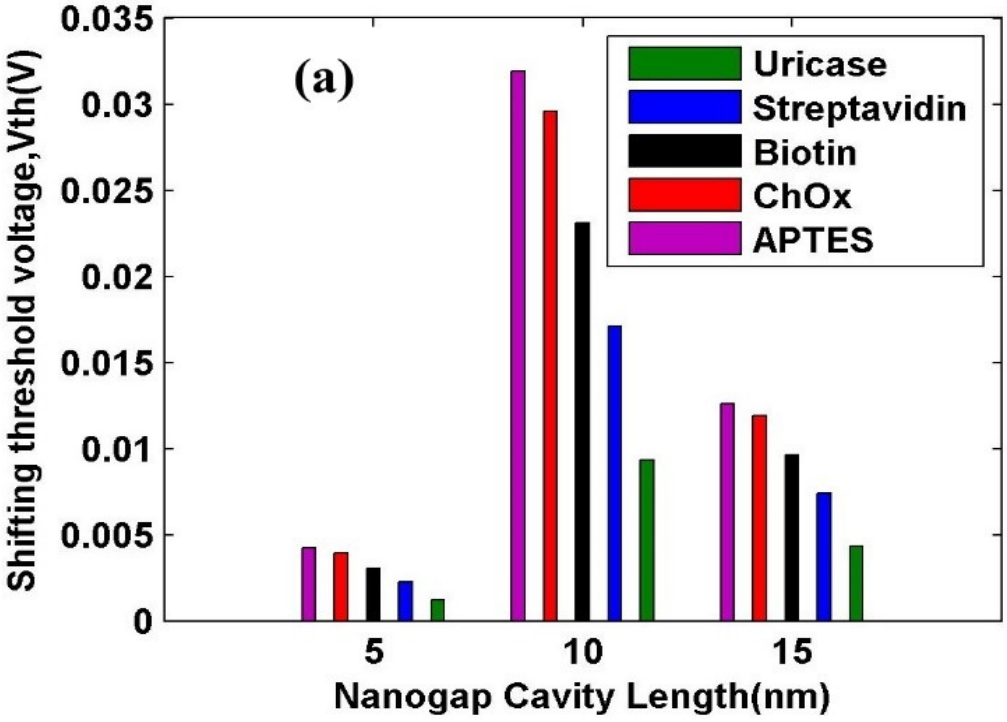

Figure 3. 16. illustrates the effect of different biomolecules on leakage current shift and switching ratio for n-substrate channel DM-THMG -GAA-JL-NWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05$V) [59].

Figure 3. 17 examines a comparison of the drain-off sensitivity ($S_{I_{OFF}}$) dielectric modulated triple hybrid metal-GAA-JL-FET with the available works[38]. The dimensions of both devices, including the channel length, cavity length, pillar radius, etc., are identical. As can be shown in **Figure 3. 17**, the triple hybrid metal-GAA-JL-FET exhibits a significantly more excellent ($S_{I_{OFF}}$) sensitivity parameter compared to the available works[38]. The subthreshold current, also known as leakage current, is entirely controlled by a high-k gate oxide and different gate electrodes in the DM-THMG-GAA junctionless transistor[59], [97]. This also proves that the leakage current is sensitive to changes in dielectric permittivity. Our modelling of the device, which includes novel technologies like gate oxide material (high-k) and a designed gate electrode, improves not only the drain-off sensitivity ($S_{I_{OFF}}$) but also the switching ratio, drain-on current and surface potential compared to previously published works[38]. Since the proposed device includes an interface layer (SiO_2), high-k layer (HfO_2),

and engineered gate electrode, thus leading to suppressing tunnelling current under-20 nm technology node and minimizing short channel effects. Therefore, a DM-THMG-GAA junctionless transistor significantly improves sensitivity over the available technology [38], making it a promising candidate for detecting diseases caused by neutral biomolecules.

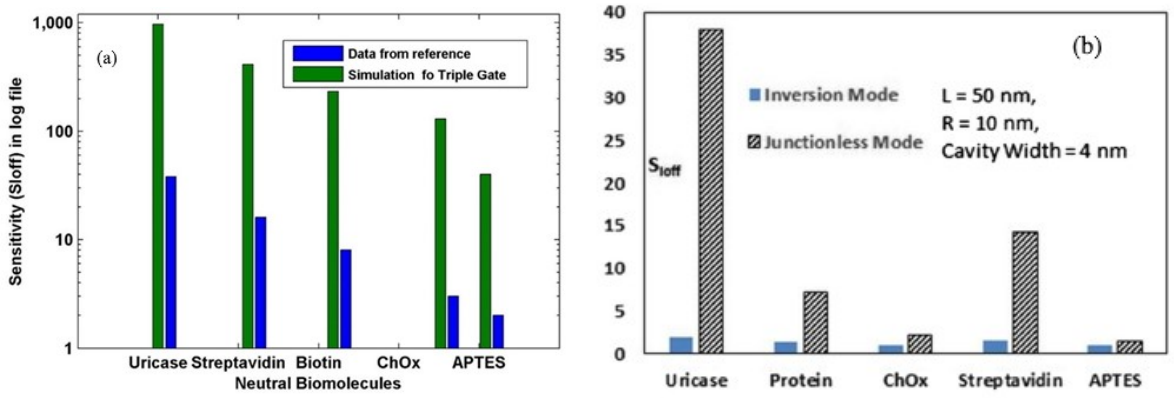

Figure 3. 17. illustrates sensitivity ($S_{I_{OFF}}$) comparison DM-THMG -GAA-JL-NWFET with available works[38], [59], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05$V).

3.3.3 Assessment of the Linearity Performance

Less distortion and better linearity are needed to produce FET-based biosensors with increased speed and sensitivity[95], [98]. Additionally, nonlinearity causes intermodulation distortion (IMD), degrading the device's performance by generating an undesired signal distortion [26], [95]. Transconductance, output conductance, and output resistance are electrical parameters used to analyze the linearity of the proposed biosensor devices.

a) Transconductance($\mathbf{g_m}$) and Output conductance ($\mathbf{g_d}$) variation

The transconductance ($\mathbf{g_m}$) can be determined by differentiating the drain current relative to the gate voltage by keeping the drain voltage constant, as we have seen in **(eq.3.1).** As shown in **Figure 3. 18 (a),** a decrease in transconductance relative to the linear region characterizes the saturation zone of the device. As the biomolecule's dielectric constant changes in the nanocavity region, the transconductance of the DM-THMG-GAA-JL FET biosensor reaches a peak at various gate voltages. This is because the device's transconductance varies with the ON-current at different gate voltages, which in turn varies with the dielectric constant of the biomolecule. **Figure 3. 18 (a)** demonstrates that as the biomolecules' dielectric constant increases, so does the gain, with the maximum gain reaching at a gate bias voltage (0.6V) and used to indicate device linearity due to its nonlinearity [95].

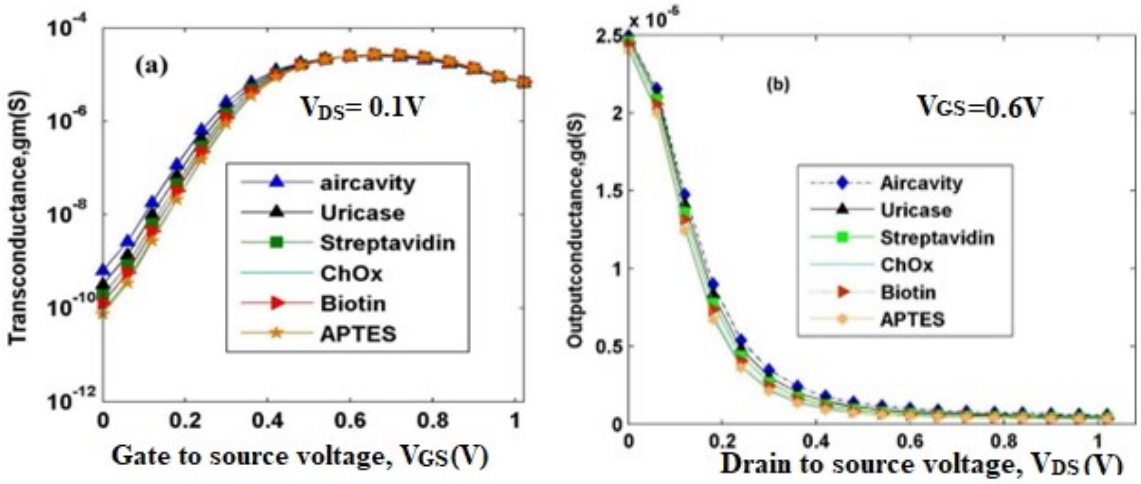

Figure 3. 18. illustrates impacts of biomolecules on **(a)** Transconductance (g_m) log file and **(b)** Output conductance (g_d) for DM-THMG -GAA-JL-NWFET biosensor[59].

Figure 3. 18b) illustrates the proposed device output conductance versus drain voltage at different biomolecule dielectric constants. The output conductance is shown to be greater under the weak inversion zone than it was observed under the strong inversion region. This is because in regions with weak inversion, increased DIBL and SCEs impact carrier mobility throughout the channel, which in turn degrades the device's performance and efficiency[99].

b) Intrinsic voltage gain $\left(\mathbf{A_V = \frac{g_m}{g_d}}\right)$ and output resistance $\left(\mathbf{R_{Out} = \frac{1}{g_d}}\right)$

An amplifier's "intrinsic voltage gain" indicates how much voltage can be amplified without negatively impacting signal quality through noise or distortion. However, input and output impedances typically place upper bounds on voltage gain in practical settings. **Figure 3. 19 a)** shows how the intrinsic voltage gain $\left(\frac{\mathbf{g_m}}{\mathbf{g_d}}\right)$ varies in response to changes in the dielectric constant of biomolecules (neutral). The transconductance is proportional to the gate voltage and the drain current, whereas the output conductance is proportional to the drain voltage and current. The gate controls the channel charge in a GAA-JL-MOSFET, which impacts the transconductance and output conductance. The transistor's nanowire structure also influences these factors. This is because the inversion charge interaction on the channel increases as the dielectric constant increases in this region. **Eq. (3.5)** [100] provides the mathematical expression of the intrinsic voltage gain, which is denoted by the symbol ($\mathbf{A_V}$).

$$\left|A_V\right| = \frac{g_m}{g_d} \tag{3. 5}$$

It is possible to estimate the output resistance of a GAA-JL-MOSFET by taking into account the parasitic resistances in the circuit, including the resistance of the source and drain contacts, the parasitic resistance of the nanowire, and any other resistances in the circuit. Additionally, the output resistance can be affected by the gate voltage and discharge current.

Figure 3. 19 b) illustrates that the output resistance of the proposed device increases as the dielectric constant under a strong inversion region. A higher dielectric constant increases carrier mobility through the channel and decreases the output conductance, which modulates gate controllability. As a result, output resistance is an important parameter of a transistor and its maximum ($\mathbf{R_{Out}}$) determines the maximum gain ($\mathbf{A_V}$) of the transistor. The equation for calculating the output resistance of a transistor, denoted by the notation ($\mathbf{R_{Out}}$), is provided in **(eq.3.6)**[101].

$$R_{Out} = \frac{1}{g_d} \tag{3.6}$$

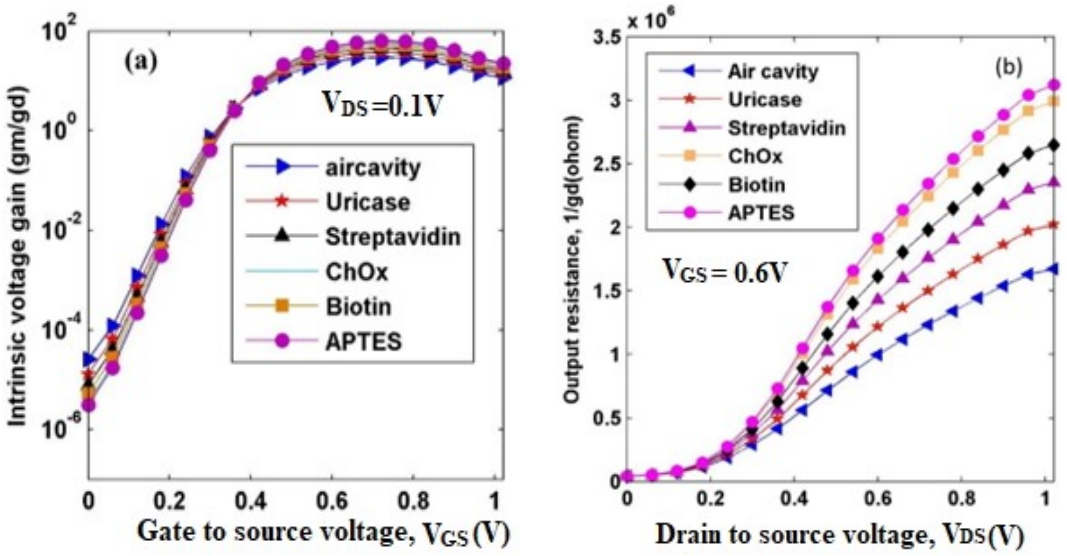

Figure 3. 19. illustrates impacts of biomolecules on **(a)** intrinsic voltage gain ($\frac{g_m}{g_d}$) log file and **(b)** output resistance ($1/g_d$) for DM-THMG -GAA-JL-NWFET biosensor [59].

In conclusion, the intrinsic voltage gain and output resistance of a GAA-JL-MOSFET relies on many things, such as how the transistor was designed and how it is being used. Modelling and simulation can be used to estimate these parameters, making them better for certain uses.

3.4 Summary

This chapter presented an n-substrate channel dielectric modulated triple hybrid metal gate-all-around junctionless nanowire transistor for the first time and compared it with single, double, and triple hybrid metal gate transistors for various disease sensing applications employing atlas-3D device simulation tool. In all devices (single, double, and triple metal gate dives), electrical characteristics were examined in terms of subthreshold slope, drain-off sensitivity $(S_{I_{OFF}})$, surface potential, switching ratio(I_{ON}/I_{OFF}), output conductance (g_d) output resistance $(1/g_d)$, and transconductance (g_m), have been studied in the presence of biomolecules. The results show that including a high-k and customized gate for DM THMG-GAA-JL-FET-based biosensors significantly boosts carrier velocity and efficiency, eliminates DIBL, hot-carrier effect, and other SCEs reduces power dissipation. In addition, the DM THMG-GAA-JL-FET -based biosensor demonstrates an impressive sensitivity profile regarding the transconductance gain and the output resistance. Another significant improvement of the triple hybrid metal gate over the double hybrid metal gate is device sensitivity, i.e., at APTES biomolecule, shifting the threshold voltage (ΔV_{th}) is $3.59x10^{-3}V$ for a double hybrid metal gate and $3.19x10^{-2}V$ is for a triple hybrid metal gate, so a 788.6% improvement was observed in the triple metal gate compared with a double hybrid metal gate. In addition to the biomolecule dielectric constant value, the nanogap cavity length influences the proposed device's performance. Thus, the DM THMGAA-JL-NWFET-based biosensor could be a low-voltage, dielectric-modulation-based biomolecule detector with high sensitivity. Our investigation led us to conclude that DM THMGAA-JL-NWFET-based biosensor could be a promising technology for the detection of biomolecules such as APTES, Streptavidin, Biotin, Uricase, and Choli oxidase (ChO_x) in the area of biomedical application. In light of this, we can state that the proposed device can be utilized to identify and diagnose early, rapidly spreading biomarker diseases, including breast and lung cancer (APTES) and uric acid in human blood serum (Uricase); the next chapter will discuss the impact of localized or trap charge one device sensing performance.

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CHAPTER -4

Effect of Trap Charges on Dielectric Modulated Triple Hybrid Metal Gate Junctionless Gate All Around Silicon Nanowire FET-based Biosensor

Abstract

In this objective, a triple hybrid metal gate dielectric modulated gate all around junctionless nanowire field-effect transistor (NWFET)-based biosensor was designed to investigate the effects of interface trap charge (ITCs) on device performance. The ability to predict the effect of induced localized charges on device performance in future nanometer-scale device dimensions due to radiation damage, hot carrier damage, and process damage is crucial. For instance, ionizing radiation damages silicon-based electronic devices by causing trapped holes in the oxide and increasing trap density at the Si-SiO_2 interface. These defects cause degradation of device parameters such as sub-threshold swing, drain current, switching ratio, threshold voltage shifts, etc. In this objective, the effect of negative and positive ITCs on the sensitivity of a JL double and triple metal gate GAA SiNWFET biosensor in the sub-threshold regime has been studied and compared using the SILVACO ATLAS-TCAD device simulation tool. The output electrical characteristics of both devices were studied by considering uniformly immobilized APTES biomolecules on the nanogap cavity region. These characteristics included switching ratio, output conductance, transconductance, drain current, subthreshold voltage, intrinsic voltage gain, and threshold voltage. Trap charges (TCs) of $\pm 5x10^{12} cm^{-2}$ were applied in between SiO_2 and silicon interface region. When an APTES biomolecule is immobilized uniformly in both nanogap cavity regions, the results reveal a triple hybrid metal gate device delivers an 184% improvement in shifting threshold voltage over a double hybrid metal gate device under a negative trap charge. The findings indicated that the proposed device's performance was enhanced by considering a negative trap charge for the interface layer. In light of the results, it was observed that considering negative interface trap charges in a device modelling significantly improved the accuracy of the threshold voltage shift and efficiency estimation of the device.

4.1 Introduction

This chapter presents how the electrical performance of the junctionless cylindrical Gate Silicon nanowire FET is affected by localized charges caused by hot carriers, radiation, and process degradation. The best electrostatic control of the channel [1], may be found in the JL-GAA NWFET, also known as the surrounding gate nanowire MOSFET, which has been shown to be one of the most promising device architectures to expand the scaling of the CMOS device. JL-GAA NWFET has better hot carrier reliability than Bulk MOSFET due to improved gate control and reduced short channel effects[2]. Much research is being carried out on fabrication techniques of Jl-GAA MOSFET[3]–[5]. Recent research has focused on semiconductor device size to address the need for smaller integrated circuits (ICS) with the same functionality and to increase the number of ICs on a chip for higher device performance [6], [7]. CMOS technology has become a promising option for label-free detection due to its continuous scaling of the minimum channel length and the subsequent rise in sensitivity response[8]. As very large-scale integration technology develops, the feature sizes of metal-oxide-semiconductor field effect transistors (MOSFETs) are progressively reduced to boost the packing density[9], [10]. In order to achieve continuous scaling in bulk MOSFETs, it is required to increase the channel doping. This is because increasing the channel doping minimizes the junction electric field in the channel. In addition, the higher doping prohibits the channel region depletion widths from overlapping the source and drain regions[11]. However, impurity scattering in the high-channel doping region causes mobility reduction[12].

In contrast, further scaling following the ITRS roadmap[9] is seriously compromised by short-channel effects (SCEs). Numerous innovative structures based on diverse engineering principles have been presented to reduce SCEs in the SOI platform[13]. Ionizing radiation is also another issue in CMOS or MOS downscaling on electronic devices and technologies[13]. Because of the evolution of the source/drain (S/D) junction for Nano dimensional MOSFETs, downscaling of Field Effect Transistor (FET) in CMOS Technology is challenging [14]. As a result, the combination of these impacts results in substantial reliability concerns and causes performance to degrade over a period of time [15]. To address these difficulties, bulk transistors can be replaced with devices that lack S/D junction, such as Junctionless GAA-SiNWFETs[16]–[18] or multi-gate transistors were proposed because of its promising device for future scaling[19]. Due to its low leakage current, improved subthreshold slope, better electrostatic control inside the device[20], and decreased mobility degradation with gate-to-source voltage (V_{GS}) [2-5], the JL Triple Gate-GAA-SiNWFET has attracted significant interest.

Previous research on the performance of JL-GAA NWFETs has shown that they have better label-free biomolecular detection capability and are suitable for low-power sensing applications[21], [22]. Since detection of these biomolecular species is used for early detection of biological diseases, such as Alzheimer's[23], breast cancer[24], [25], ovarian cancer (viral diseases), hepatocellular carcinoma (HCC)[8], [24], and other biological diseases. For instance, Biological molecules such as RNA, DNA, Uricase, APTES, Streptavidin, ChO_XAnd biotin biomolecules play a vital role in screening out those biological diseases[26]–[28]. The

effectiveness of biosensor technology depends on being able to convert the biomolecule's biological properties into corresponding electronic properties[7]. Recently, many researchers have been interested in NWFET-based biosensors for the following reasons[29]: Easy scalability, cost-effectiveness, label-free detection [24], compatibility with bulk CMOS [30], high sensitivity [31], productive on-chip integration, less detection reaction time and lower fabrication cost, as well as low power consumption [32]–[34]. However, with continuous scaling, the quality and properties of the channel/gate oxide interface have an impact on device performance and reliability[35]. With the increasing integration density of integrated circuits and the decreasing dimensions of the device, the probability of generating interface traps/charges is rather considerable, and these charges have harmful impacts on the performance of the device. Degradation in device performance and a decrease in device efficiency and lifetime are brought on by interface charges, which might be intrinsic, process-related, or operationally induced. Nanoscale multi-gate metal oxide semiconductor field-effect transistors are vulnerable to contamination, which can lead to the development of interface trap charges [28,29]. As a result, these devices contain significantly more defects or interface charge traps than state-of-the-art CMOS devices, which may impact their electrical properties.

Similarly to conventional MOSFETs, ionizing radiation can cause traps and defects[19] and lead to serious device reliability issues. Interface trap charges may be generated due to hot carrier-induced [37], process/stress-induced, and radiation-induced damage. In summary, this ITC can cause significant problems with device reliability in scaled JL-GAA-NWFETs. Since the current is highly sensitive to the process and voltage variation, they increases significantly in the sub-threshold region[14]. The influence of the ITC on the power and delay of the JL-MOSFET device is significant, and as such, a simulation or theoretical framework to handle this issue is essential. Therefore, it is important to understand how ITC affects the functioning of the device so that precautions might be taken during fabrication.

The effect of ITC on JL-MOSFETs using a charge-based model and the implications of localized trap charges on work-function-engineered SOI-MOSFETs have been examined[14]. However, the impact of ITC on the performance of ultra-low-power (ULP) integrated electronics, such as the effect of ITC on power dissipation, delay, and reliability issues, has not been investigated in the literature. Consequently, determining the extent to which localized charges degrade performance and optimizing device characteristics to boost performance in sensing applications are both essential.

This chapter comprehensively investigates how interface trap charges affect the JL-electrical triple metal gate GAA-NWFET'biosensor performance. Immobilizing different biomolecules in the nanogap cavity n-type double and triple hybrid metal gate JL-GS-GAA-NWFET has been analyzed under the same room temperature. Additionally, the outcome of localized/interface trap charge on the device's parameters (threshold voltage variation, transconductance, switching ratio, intrinsic voltage gain, output conductance, device efficiency, and tunnelling current) has been extensively studied. Device parameters such as potential, transconductance, threshold voltage, subthreshold current, and subthreshold slope are examined in relation to the density of localized interface charges (both positive and

negative). The influence of localized charges on the biomolecule sensitivity of the JL-THM GAA NWFET is also discussed in this chapter. The goal is to explain the mechanisms that contribute to device degradation due to localized charges in the presence of biomolecules.

4.2 Device Structure and Simulation Models

4.2.1 Device Structure

The device design for n-substrate channel cylindrical junctionless high-k triple hybrid metal gate NWFET-based biosensor with ITCs has been demonstrated in **Figure 4. 1(b)**. Where, $L_1(6nm)$, $L_2(8nm)$, $L_3(6nm)$ are the lengths of M_1, M_2, and M_3 respectively and $L_4(10nm)$, are the length of the nanogap cavity and silicon dioxide (SiO_2), etching near the source and drain end, and L(20 nm) channel length. $L_1(6nm)$, $L_2(8nm)$, $L_3(6nm)$ are the lengths of M_1, M_2, and M_3 respectively and $L_4(10nm)$, are length of the nanogap cavity and silicon dioxide (SiO_2), etching near the source and drain end, and L (20 nm) channel length. T_1, T_2, $T_3$and T_4 are the thickness of metal gate, hafnium oxide, nanogap cavity, and interface (SiO_2) oxide, respectively, and 2R is the diameter of the silicon film. The interface layer (SiO_2) between hafnium oxide and silicon film is considered to produce a favourable region for carrier mobility between hafnium oxide and silicon film[38]. The gate materials denoted by $M_1, M_2$and M_3 have different work-function given ($\Phi_{M1} = 4.96$, $\Phi_{M2} = 4.86$ and $\Phi_{M3} = 4.50$), respectively. The work function (Φ_{M1}) between the source and drain ends is used to adjust the channel's potential profile and decrease drain-induced barrier lowering (DIBL), and work function near the drain end (Φ_{M3}) is used for screening effects and controls high drain electric field fluctuation due to V_{DS}, while the highest work function (Φ_{M1}) near the source end is used to control electron saturation velocity and doping fluctuation[39], [40]. The nanogap cavity region is used as a detecting site in which target biomolecules, like (APTES, ϵ =3.57), Biotin, ϵ =2.63), Uricase, ϵ =1.54, ChO_2, ϵ =3.30, Streptavidin, ϵ =2.10 and (air, ϵ =1.0) are uniformly introducing their dielectric constant, interchangeably [41]. Different types of ITCs (positive and negative) are given by ($N_f = \pm 5x10^{16} cm^{-2}$)and also without interface (Neutral) charge ($N_f = 0$) are simulated interchangeably to study the effects of ITCs on the proposed device biosensor performance. The damaged region caused by the interface oxide trap charges (N_f) is shown in **Figure 4. 1b)** has a zigzag line towards the drain.

Table 4. 1: Describes proposed device structural parameters.

Parameters	**DG-GAA-JL-NWFET**	**TG-GAA-JL-NWFET**
Length of the channel (nm)	20.0	20.0
Thickness of Hafnium Oxide (nm)	HfO_2=1.5 &SiO_2=0.3	HfO_2=1.5 &SiO_2=0.3
Thickness of Oxide near-source side (nm)	SiO_2=1.0	SiO_2=1.0
Length of Oxide source side (nm)	SiO_2=10.0	SiO_2=10.0
Length of nanogap cavity (nm)	10.0	10.0
Drain/Source thickness (nm)	10.0	10.0
Source/Drain length (nm)	10.0	10.0

Thickness of nanogap cavity (nm)	1.0		1.0		
Silicon film diameter(nm)	10.0		10.0		
Interface trap charges (ITCs)	$\pm 5x10^{12} cm^{-2}$		$\pm 5x10^{12} cm^{-2}$		
Source/Drain & Channel Doping (N_D+)	$10^{19} cm^{-3}$		$10^{19} cm^{-3}$		
Oxide Dielectric constant	SiO_2=3.9&HfO_2=25.0				
Gate Work functions (eV)	4.86	4.50	4.96	4.86	4.50

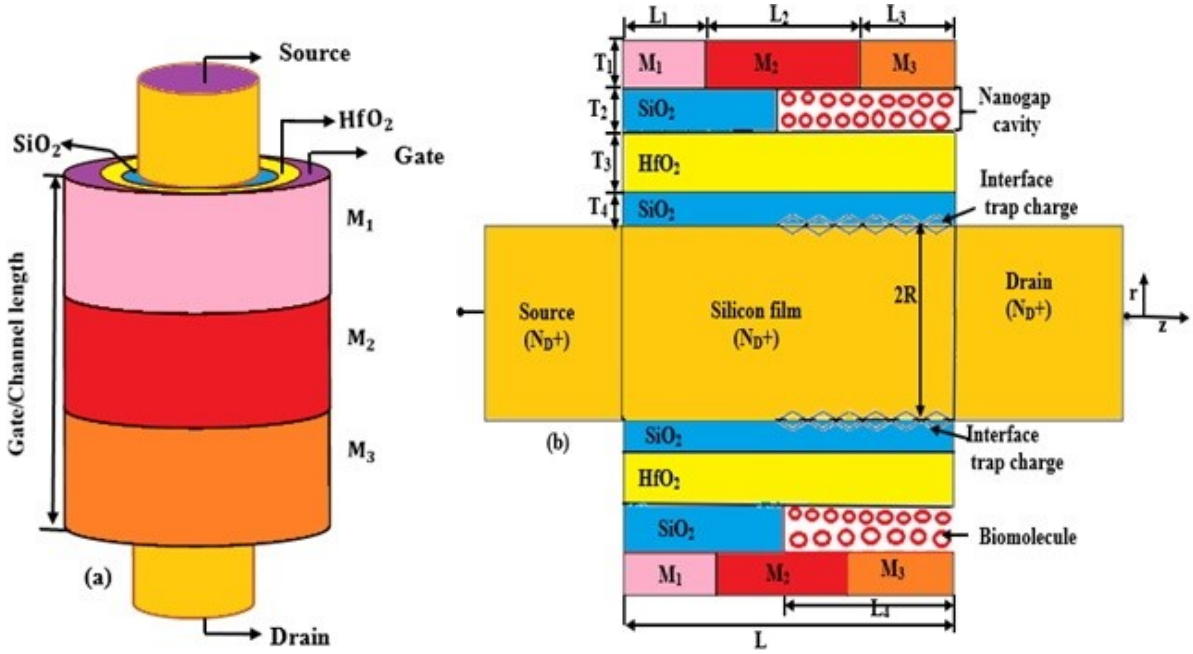

Figure 4. 1. (a) 3-D schematic structure and **(b)** 2-D cross-sectional view with cavity region for n-type triple hybrid metal gate all around JL-NWFET [7].

4.2.2 Simulation Models

Based on these device structural parameters, several simulations were done using the Atlas-3D device simulator tool to characterize the proposed device's electrical characteristics. Models like (CONMOB) concentration-dependent mobility [42] were activated to study doping versus mobility distribution. The silicon band gap narrowing model, also known as the BGN model, was made active. This model estimates the intrinsic carrier concentration. The drift-diffusion carrier transport model was activated in the Atlas- 3D TCAD device simulation tool. Carrier-carrier scattering mobility model (CCSMOB) is a model which is used to analyze carrier mobility and concentration[42]. Perpendicular and parallel field-dependent carrier mobility was described using Lombardi (CVT) models[42]. This work did not include quantum mechanical models in this simulation since the silicon film radius is larger than 4nm[16]. By considering uniformly distributed interface trap charge ($N_f = 0, \pm 5x10^{12} cm^{-2}$) at the Si–$SiO_2$ interface, as demonstrated in **Figure 4. 1(b),** its impact on device performance has been examined relative to ($N_f = 0$)**.** Since interface trap charges near the drain side are vulnerable to a high drain electric field in the case of short channel device[43]; Hot carriers are induced by the high electric field, leading to a rise in localized charge at the Si–SiO_2 interface and will

permanently damage the device's performance[44], so we are interested in studying the proposed device. The majority of the results in this analysis are shown on a graph for the case where localized charges are present over half of the Si-SiO_2 interface close to the drain side (i.e., L_4=L/2=10nm), as the drain end is more vulnerable to damage because of the presence of a high electric field.

Models used in device simulations for Surrounding Gate MOSFET [45] were applied to TMGAA JL SiNWFET to validate and authenticate our work. The close agreement between the simulated data and the available work [45] verifies the validity of the models employed in the simulations without considering interface trap charge and biomolecule nanogap cavity. As illustrated in **Figure 4. 2**, our simulated data is in good agreement with the work of [45].

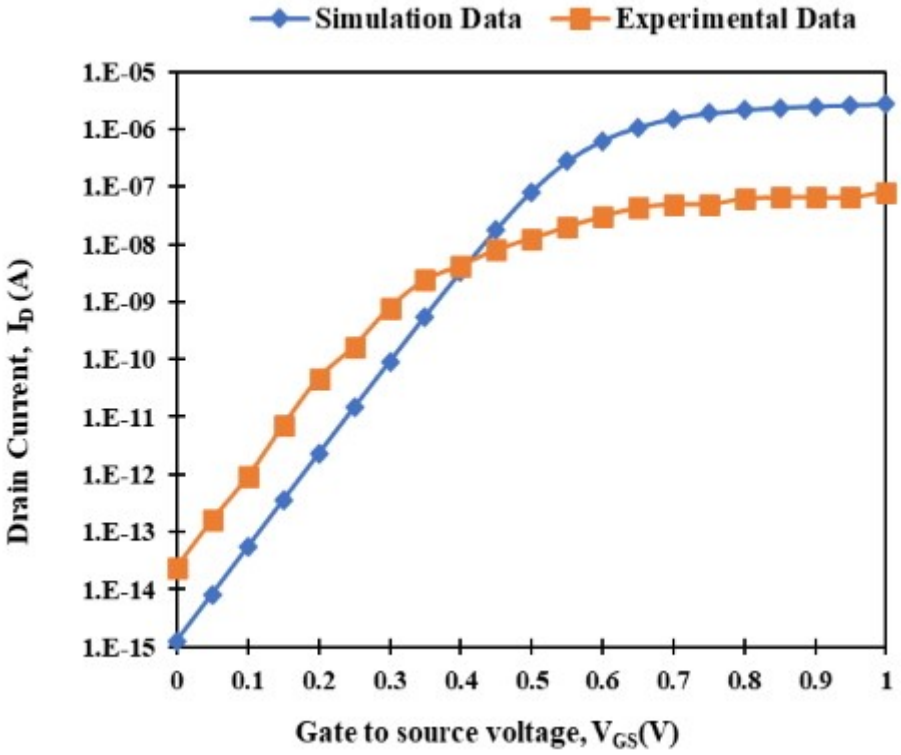

Figure 4. 2. Demonstrates calibration simulation results of n-substrate channel triple hybrid metal gate all around JL-NWFET without nanogap cavity region, (V_{DS}=0.05V) [7], with the work of [45].

4.3 Results and Discussion

Here, we look at how using varying trap charges on the Si–SiO_2 interface close to the drain side layer, and various biomolecules can change the output properties of a double and triple hybrid metal gate dielectric modulated gate all around junctionless NWFET-based biosensor. By assuming, the introduced biomolecules in the nanogap cavity do not react with the silicon oxide interface and high-k dielectric material.

4.3.1 Impact of Localized Charges on Transfer Characteristics

a) Effects of ITCs on drain current

Figure 4. 3. Illustrates the simulated results of I_D-V_G transfer characteristics on a log scale at $V_D = 0.05V$ with different interface trap charges for double and triple hybrid metal gates. As shown in the graph, different ITCs affect the drain current in both devices. The triple hybrid metal gate has a lower leakage current than a double hybrid metal gate in the case of a negative trap charge. The reason is that the highest work function (Φ_1) near the source region is used to overcome electron saturation velocity and hot carrier effects through the channel by reducing the tunnelling barrier[46] and increasing carrier mobility across the channel with a negative trap charge. In addition, the intermediate work function (Φ_2) lowers drain-induced barrier lowering and parasitic resistance, thereby increasing gate controllability[47]. Since ITCs rise at $Si - SiO_2$ interface will accept an electron from an acceptor-type ITC, acting as a fixed negative interface trap charge[9]. In the same way, the donor-type interface trap can be thought of as a localized positive charge [48]. These interface traps can be transferred into an equivalent interface fixed charge, leading to band bending under the gate[49], causing a rise in flat band voltage under the damaged region and affecting electron mobility in the channel[44]. **Figure 4. 3** illustrates lower tunnelling current for a negative interface charge and a higher tunnelling current due to a higher electric field for a positive interface charge in both devices[9]. For instance, in a triple metal gate, leakage current (I_{OFF}) results for positive and negative interface trap charges are $1.5x10^{-15}$A and $7.97x10^{-17}$A respectively at $V_{GS} = 0$ and $V_{DS} = 0.05V$. The study signifies that the proposed devices are more vulnerable in the case of positive ITC causing more tunneling current and hot carrier effects leading to carrier mobility degradation in the channel.

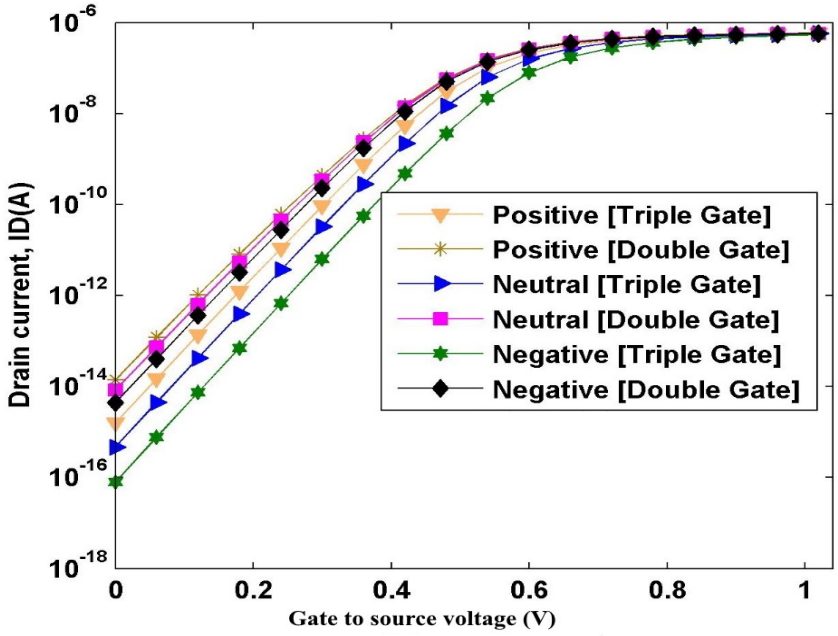

Figure 4. 3. Describes the effect of interface trap charge on I_{DS}-V_{GS} for n-type double and triple hybrid metal gate all around JL-NWFET without cavity region [2], $V_{DS} = 0.05V$ *and* $V_{GS} = 1.0V$.

b) Effect of ITCs on threshold voltage (V_{th}) and subthreshold slope

Figure 4. 4. Illustrates variation of **(a)** threshold voltage (V_{th}) **(b)** subthreshold slope at $V_{gs} = 1.0V$ and $V_{DS} = 0.05V$ with ITCs for double and triple hybrid metal gates with different trap charges. **Figure 4. 4(a).** Shows that threshold voltage is larger for the negative interface charger than when $N_F = 0$ and the positive interface charge in both devices. This is because of the smaller barrier height in the case of a positive trap charge [9]. The positive interface charge will produce the highest electric field peak compared to the $N_F = 0$ and negative trap charge [9]. As a result of the high electric field, positive interface charge cases will impose a greater SCE on the device than negative charge cases[10]. **Figure 4. 4(b)** illustrates a lower subthreshold slope under triple than a double hybrid metal gate. The reason is that work function (Φ_1) near the source region controls carrier injection through the channel, and the intermediate work function the (Φ_2) develops a barrier potential to reduce reverse current from the drain through the channel, thereby increasing mobility carriers [47]. Variation in threshold voltage is caused by varying localized/interface trap charges, which introduces a step potential profile in the channel due to the high electric field near the drain side; this causes damage to the oxide interface near the drain junction[50]. The metal gate work function (Φ_3) lowers the peak electric field at the drain side and raises the average electric field near the gate to enhance device performance[44]. Fixed localized charge at the interface causes band bending under the gate, leading to changes in flat band voltage in the damaged region leading to a shift in threshold voltage[9]. Higher degradation of SS in the triple hybrid metal gate for negative ITCs is investigated due to higher electron mobility and threshold voltage than positive interface trap charge; this enhances electrostatic gate control[51], as shown in **Figure 4. 4(b)** compared to a double hybrid metal gate transistor.

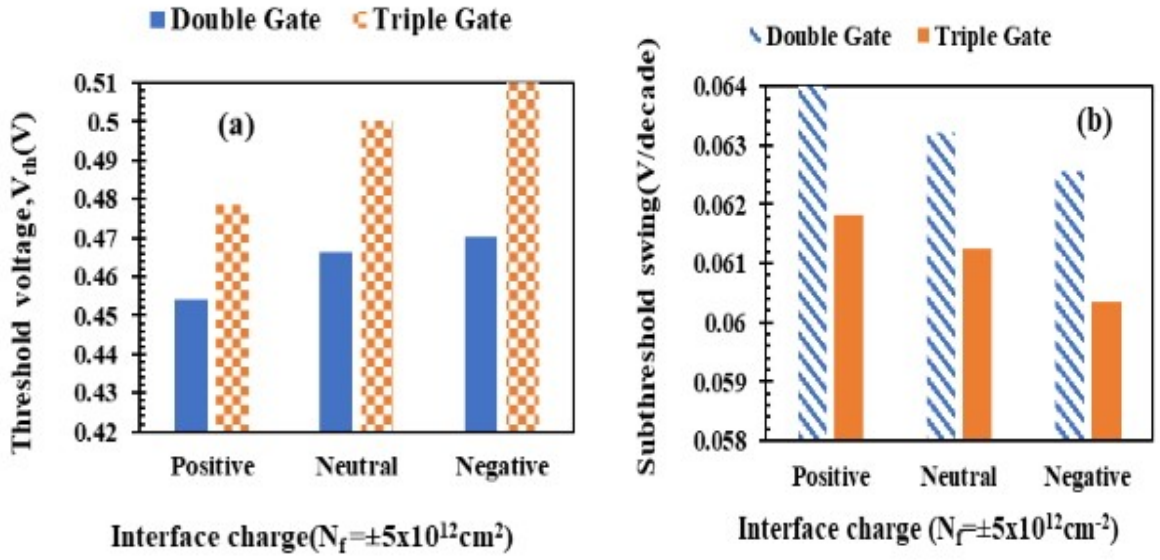

Figure 4. 4. Effect of ITCs on **(a)**threshold voltage (V_{th}) and **(b)** subthreshold slope for n-type double and triple hybrid metal gate all around JL-NWFET, ($V_{DS} = 0.05V$ and $V_{GS} = 1.0V$).

c) Impact of localized/trap charge on drain current

Figure 4. 5. Demonstrates variation of **(a)** switching ratio $\left(\frac{I_{ON}}{I_{OFF}}\right)$, **(b)** tunneling current at ITCs ($N_f = \pm 5 \times 10^{12}$) on double and triple hybrid metal gate transistors transfer characteristics. It shows that lower tunnelling/leakage current and higher switching ratios are investigated in triple hybrid metal gates than double hybrid metal gate devices when negative ITC was considered. The gate electrodes reduce hot carriers caused by a high drain fringing electric field. The negative ITCs have a higher switching ratio and lower leakage current in both devices than positive and neutral ITCs, as illustrated in

Figure 4. 5(a). It signifies that negative ITC can mitigate DIBL caused by hot-carrier effects, thereby increasing mobility carriers and drain on currents in the channel[52], [53]. Drain-off current ratio decreases/increases for positive /negative interface trap charge in all operation regions. Reduced I_{ON}/I_{OFF} ratio for positive interface trap charge and improved I_{ON}/I_{OFF} ratio for negative interface trap charge, as shown in

Figure 4. 5(a). For instance, switching (I_{ON}/I_{OFF}) ratio in the case of APTES (biomolecule) are $4.18x10^6$ and $4.18x10^8$ respectively for double and triple hybrid metal gate devices at negative interface trap charge (ITC). So, the overall effect is a higher I_{ON}/I_{OFF} ratio when the fixed/trap charge is negative and a lower I_{ON}/I_{OFF} ratio when the fixed charge is positive for both devices. This is because using three instead of double gates raises the potential profile's steepness, which varies with the work function difference[54]. The transport efficiency, the step profile of the channel's potential, and the flow of a large number of charge carriers are enhanced by a larger work function difference between the adjacent gates in a triple-gate architecture[1].

Figure 4. 5(b). Demonstrates the impact of ITCs on leakage current with APTES biomolecule for double and triple hybrid metal gate dielectric modulated GAA-JL-NWFET. The graph illustrates double metal gate device is more vulnerable to localized charge than triple metal gate device. Reduced charge carriers in the channel due to positive interface trap charge (ITC) allows the depletion layer to become thicker across the reverse junction[49], allowing the flow of charge carriers in the OFF state, resulting from higher leakage current[55]. Hot carriers generate high-drain electric fields and cause serious problems, such as reliability and device efficiency[11].

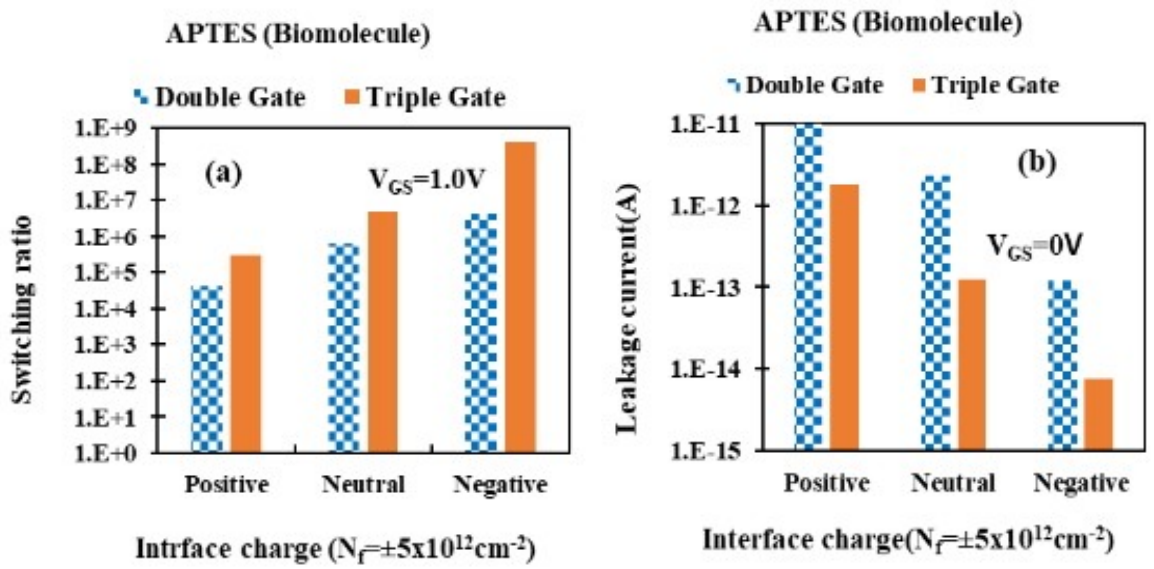

Figure 4. 5. (a) describes **(a)** shift of switching ratio and **(b)** leakage current, with different ITCs for n-type double and triple hybrid metal gate all around JL-NWFET, ($V_{DS} = 0.05V$).

d) Effect of interface charge on device sensitivity (ΔV_{th} and $S_{I_{OFF}}$)

The threshold voltage is an essential characteristic of the NW-MOSFET biosensor used as the detecting parameter to sense the device's sensitivity when the biomolecule interacts with the device. The detection mechanism of biomolecule species is carried out by introducing APTES (biomolecule) dielectric constant in the nanogap cavity and studying variations of electrical parameters, like threshold voltage, drain current, subthreshold slope, etc. Shifting threshold voltage (V_{th}) of MOSFET device is obtained using **(eq.4.1)**[56].

$$\Delta V_{th} = \left| V_{th(bio)} - V_{th(Air)} \right| \qquad (4.1)$$

Where ($\epsilon_{APTES} = 3.57$) represents APTES biomolecule dielectric constant and ($\epsilon_{air} = 1$) is air dielectric constant placed in the nanogap cavity region during simulations. **Figure 4. 6(a)** demonstrates higher threshold voltage shifting for negative than positive interface charge in both devices because negative ITC increases mobility carrier throughout the channel and reduces threshold voltage roll-off [13]. This is because fixed charges at the interface cause the band bending under the gate, which changes the flat band voltage in the damaged region [12]. Therefore, the threshold voltage is affected by the variation in the minimum surface potential. In this investigation, negative ITC is mainly used to improve mobility carriers and stabilize high electric fields near the drain for the n-type channel device. This threshold voltage variation is used to detect biomolecules in both devices, as shown in **Figure 4. 6(a),** in the presence of APTES biomolecules.

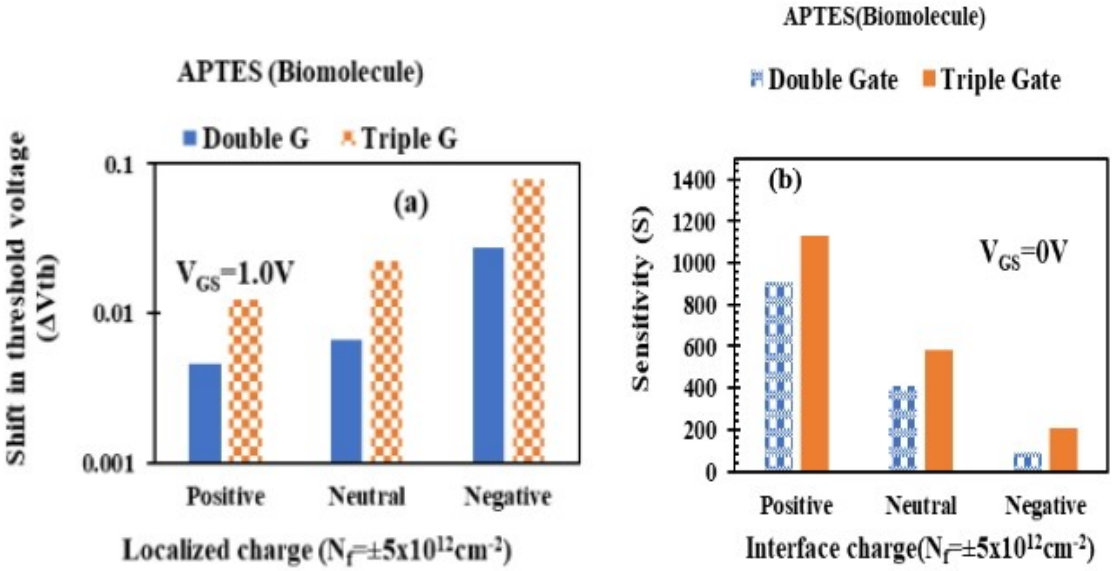

Figure 4. 6. Describes **(a)** shifting threshold voltage variations and (**b)** sensitivity ($S_{I_{OFF}}$), with ITCs for n-type double and triple hybrid metal gate all around JL-NWFET, ($V_{DS} = 0.05V$).

As we have discussed before, fixed/interface charges influence device transfer characteristics. Although positive (negative) interface fixed charges increase (reduce) drain OFF-current in subthreshold region, the change in OFF-current is of a higher order of magnitude than the change in ON-current; due to this higher variation of OFF-current ratio; employed as a device sensitivity metric system. **Figure 4. 6(a),** demonstrates drain-current sensitivity ($S_{I_{OFF}}$) is decreased for negative interface charge due to lower leakage current variation when negative interface trap charge is considered. Positive ITCs increase leakage current and drain-induced barrier-lowering effects due to hot carries caused by localized charge, leading to carrier mobility reduction in the channel. Effects of ITCs, on device sensitivity ($S_{I_{OFF}}$) or drain-current sensitivity is given by **(eq.4.2)**[54].

$$S_{I_{OFF}} = \left.\frac{I_{OFF(with\ biomolecule)}}{I_{OFF(without\ biomolecule)}}\right|_{V_{GS=0}} \quad (4.2)$$

The overall impact is an increased switching ratio for negative fixed charges and a decreased I_{ON}/I_{OFF} ratio for positive fixed charges. Intermediate higher work-function the (Φ_2) and lower work function (Φ_3) for triple hybrid metal gate, reduces threshold voltage roll-off and drain-induced barrier lowering impressions in addition to parasitic resistance, thereby enhancing gate capacity than double gate device [53].

4.3.2 Impact of Localized Charges on Analog Performance

The output characteristics, such as transconductance and output conductance, are known as the device analog parameters, which can examine the device's gain (amplification) and reliability[19], [51].

a) Evaluation of Transconductance (g_m)

Since the gain of any given device is determined by its transconductance (g_m), it needs to be sufficiently high for the device to gain significantly. As can be observed, the presence of positive (negative) fixed charges causes a decrease (an increase) in the transconductance of the material in the inversion region. Degradation of the drain current due to localized charges also leads to degradation of the transconductance [57].

Figure 4. 7(a) describes the variation of transconductance g_m with gate voltage in different trap interface charges for double and triple hybrid metal gate devices when APTES biomolecule interacts with the device. Large transconductance in the case of negative ITC was observed when other factors were kept constant, and it can be given by **(eq.(4. 3)**[58]**.**

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_i \frac{W}{L} V_D \qquad (4.\ 3)$$

Where C_i, L, μ_{FF}, and W, are capacitance of the gate oxide, channel length, field-effect mobility, and channel width, respectively.

Figure 4. 7(b) illustrates the impact of ITCs on transconductance (g_m) for double and triple hybrid metal gate high-k gate all around junctionless NWFET, at ($V_{DS} = 0.6V$ and $V_{GS} = 0.1V$). Generally, localized charges induce more deterioration in the subthreshold and linear regions than in the saturation region because localized charges have less influence on band bending when $V_{GS} > V_{th}$.

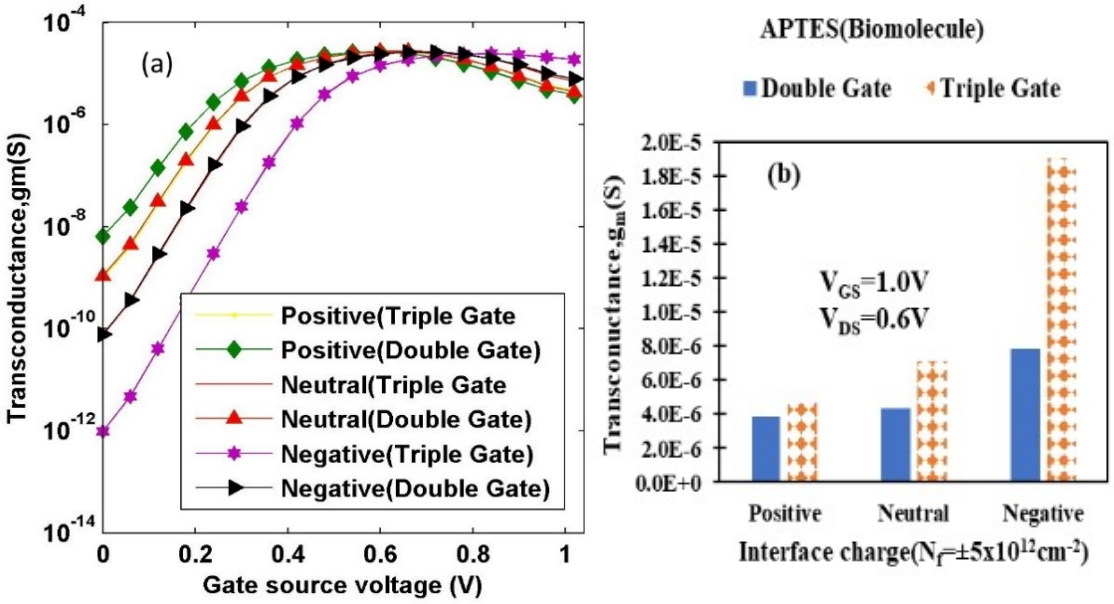

Figure 4. 7. Variation of transconductance with ITCs for n-type double and triple hybrid metal gate all around JL-NWFET, ($V_{DS} = 0.6V$ and $V_{GS} = 0.1V$).

b) Evaluation of drain conductance (g_d)

Drain conductance (g_d), also known as output conductance, is another crucial analog circuit parameter impaired by localized/trap charges[59]. It is caused by channel length modulation (CLM) caused by a change in drain voltage (V_{DS}). A smaller value for the drain conductance

indicates that the drain current should vary less with the voltage that is applied between the drain and the source. This suggests that the effect of the drain bias on the channel charge can be better suppressed, and the gate can be controlled more precisely. As a result, the device's drain conductance (g_d) should be as small as possible to have a greater intrinsic voltage gain (g_m/g_d).

Figure 4. 8. Illustrates the output conductance (g_d) of double and triple hybrid metal gate dielectric modulated GAA-JL-NWFET, which is used to characterize its output resistance ($R_{out} = \frac{1}{g_d}$) of the device. In both devices, output conductance decreases for negative but increases for positive; it can be obtained using **(eq. (4. 4)**[58] at constant gate voltage (V_{GS}).

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}} \qquad (4.\ 4)$$

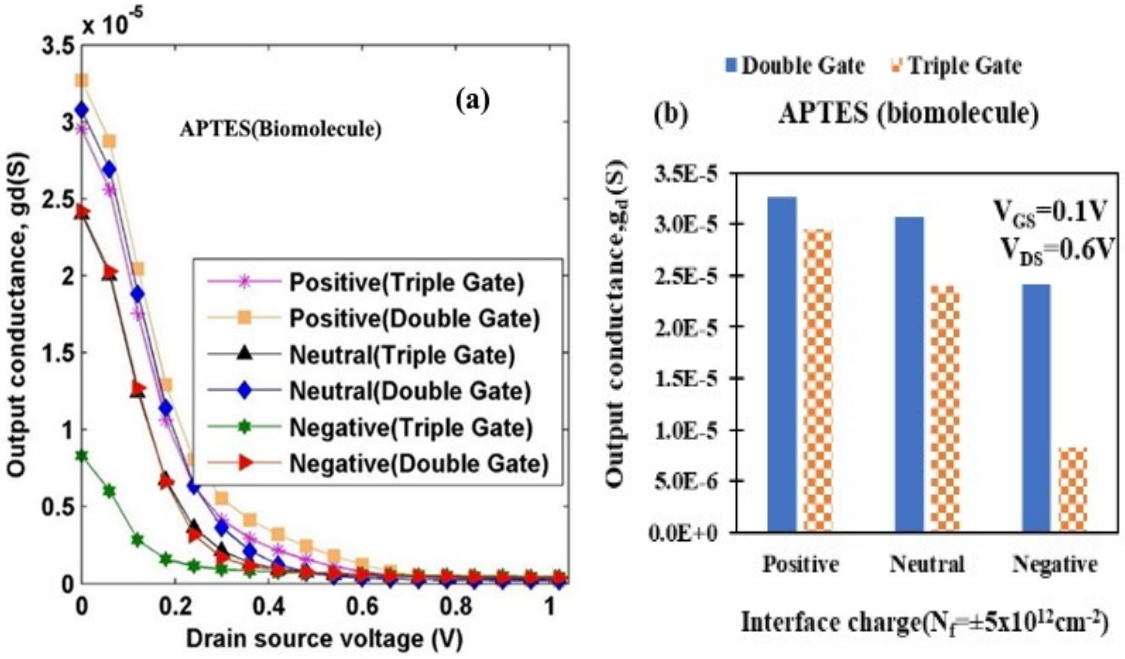

Figure 4. 8. Variation of output conductance along ITCs for n-type double and triple hybrid metal gate all around JL-NWFET, ($V_{DS} = 0.6V$ and $V_{GS} = 0.1V$).

c) Evaluation of Device Gain (g_m/g_d) & Device Efficiency (g_m/I_D)

The device's efficiency in generating transconductance (g_m/I_D) is a crucial metric in the design of analog circuits. Because it indicates the amplification (gm) obtained from the device divided by the energy provided to generate this amplification, the g_m/I_D ratio is a direct measurement of the MOSFET's efficiency (I_D). It is a measure for evaluating how well the gate voltage controls the drain current[60]. In analog applications, it is preferred to have a stronger capability to convert DC power into AC gain performance at a given drain bias. This capability is related to greater g_m/I_D values. **Figure 4. 9(a)** shows a comparison of g_m/I_D for undamaged and damaged double and triple gate devices.

Furthermore, a device with negative (positive) fixed charges has higher (lower) g_m/I_D than an undamaged device. At V_{GS}= 1.0V and V_{DS}=0.6V, g_m/I_D in the case of negative (positive)

localized charges is 46.9 % (16.34 %) higher (lower) than the undamaged for double gate devices and 36.9% (66.2%) for triple gate devices. This variation in g_m/I_D is caused by variations in g_m and I_D introduced by localized charges.

Furthermore, a device with negative (positive) fixed charges has higher (lower) g_m/I_D than an undamaged device. At V_{GS}= 1.0V and V_{DS}=0.6V, g_m/I_D in the case of negative (positive) localized charges is 46.9 % (16.34 %) higher (lower) than the undamaged for double gate devices and 36.9% (66.2%) for triple gate devices. This variation in g_m/I_D is caused by variations in g_m and I_D introduced by localized charges.

Another important electrical parameter of the MOSFET device is intrinsic voltage gain (A_V), a key parameter in analog circuits used to describe the maximum gain for an amplifier in the transistor configuration. The effect of localized charges on g_m/I_D for the double and triple metal gate JL-GAA NWFETs is shown in **Figure 4. 9(b).** Several studies have investigated the effects of this parameter have lately been published[58], [61] because transconductance can indicate a transistor's ability to convert a gate voltage modulation to a variation of the drain current[61] and is obtained using **(eq.4.5)**[61].

$$A_V = \frac{dV_{out}}{DV_{in}} = \frac{dI}{dV_g}\frac{dV_d}{dI} = g_m \frac{1}{gd} = g_m r_o \qquad (4.5)$$

Figure 4. 9(b) illustrates the variation of intrinsic voltage gain, including interface trap charge for n-type double and triple hybrid metal gate dielectric modulated GAA-JL- NWFET. The strong inversion region indicates that a triple hybrid metal gate has a greater intrinsic voltage gain at a negative interface trap charge than a double hybrid metal gate. Furthermore, in all three situations, i.e., undamaged device and device having positive and negative localized charges, a high g_m/g_d is obtained in the subthreshold region, demonstrating that triple metal gate GAA JL-NWFET is more promising than double gate devices for low-power applications. So, the effect of localized charges on g_m, g_d, g_m/I_D, and g_m/g_d is significantly stronger in subthreshold and linear regions of operation than in saturation; it is clear that localized charges are detrimental to the device when employed for low-power applications.

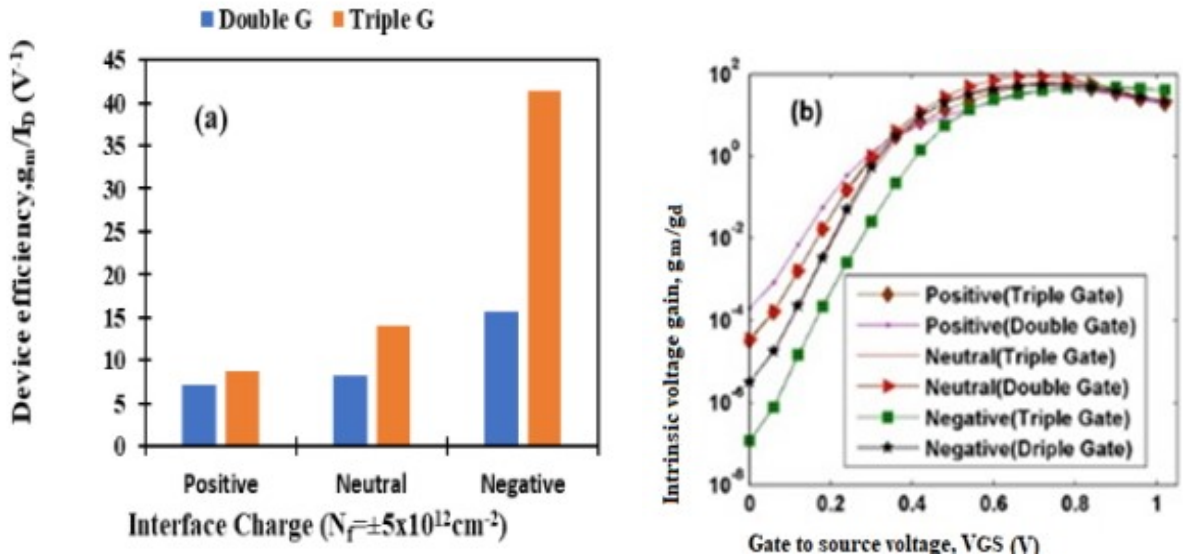

Figure 4. 9. Variation of **(a)** device efficiency and **(b)** intrinsic voltage gain along ITCs for n-type double and triple hybrid metal GAA-JL NWFET, ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$).

4.3.3 Sensitivity for different biomolecules

In this section, variations in a variety of electrical parameters, such as surface potential, subthreshold slope, threshold voltage, switching ratio, device efficiency, output resistance, and transconductance, were investigated on triple hybrid metal GAA-JL NWFET-based biosensor in order to establish how the sensor would respond to or be influenced by a variety of biomolecules in the presence of localized charge.

4.3.3.1 Impact of ITCs on Surface Potential-Based Sensitivity

During the fabrication process, localized charges are created. High-field-induced hot carriers will permanently damage the Si/SiO_2 interface close to the drain side if the electric field is sufficiently strong. Due to the fact that the electrical performance of the device is influenced by the addition of band bending provided by localized interface charges [62]. The density of localized charges and the gate-oxide capacitance play a role in the amount of variation that occurs in the voltage of the flat band [13]. The surface potential, which defines the threshold voltage fluctuation, is imperative to interpreting the proposed device's sensitivity following uniform biomolecule interaction in the targeted cavity [1]. Since the device's threshold voltage, drain-induced barrier lowering, and other electrical properties are all directly affected by variations in surface potential. The change in surface potential caused by localized charges should be kept as low as feasible so that there is minimal deterioration[14]. **Figure 4. 10** depicts the variation in the surface potential profile positively localized charges for different biomolecules in THM GAA JL MOSFET architecture. It clearly shows that surface potential increases with biomolecule dielectric constants in positively localized charges within a damaged area. This relative shift in potential is essential for determining the biosensor's sensitivity [13]. It is clear that the potential profile throughout the channel shifts when biomolecules are present, and this shift results in a higher value for the profile when the

dielectric constants are high. The surface potential of the part of the channel (drain side) over which various biomolecules were immobilized is determined by the dielectric constant value in the nanocavity region[1]. The effective gate oxide capacitance increases as the cavity is filled with various biomolecules ($K_{bio} > 1$), which in turn increases the coupling between the gate and the charge carriers flowing through the channel. Negatively charged biomolecules further encourage coupling due to their stronger binding capabilities than neutral biomolecules, decreasing surface potential. Strong coupling between the gate and the channel reduces the surface potential, and this coupling is increasing with the increase of K_{bio}, this variation of surface potential is clearly depicted in **Figure 4. 10**.

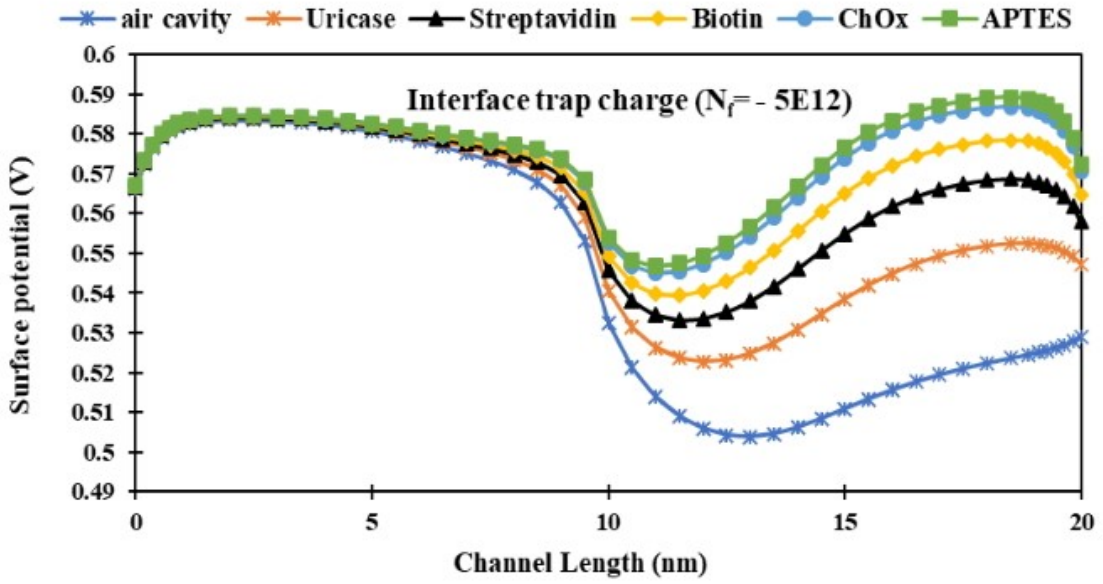

Figure 4. 10. Describes the effect of different biomolecules on surface potential as a function of channel length in the case of negative ITC for n-substrate THM-GAA-JL-NWFET[2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Potential variation for neutral biomolecules is depicted in

Figure 4. 11. It is evident that the presence of biomolecules changes the potential profile along the channel. The graph shows that the lowest surface potential rises in proportion to the dielectric constant. Near the drain side, a cavity of 10 nm is considered for biomolecule immobilization. When different biomolecules are filled in the cavity region, a higher variation in surface potential is observed, as illustrated in

Figure 4. 11. The dielectric constant value in the nanocavity region determines the surface potential of the portion of the channel (drain side) over which various biomolecules were immobilized [1], [2]. The surface potential on the source side of the device, which is not covered by the dielectric materials, is lower. This leads us to the conclusion that the surface potential of the dielectric-modulated THM-GAA-JL-NWFET varies more when the dielectric constant of the nanogap cavity changes. Furthermore, this variation in the surface potential can be utilized as a sensing metric to assess the presence of specific biomolecules that are

trapped within the nanocavity region. This can be accomplished by comparing the change in the surface potential to a known value.

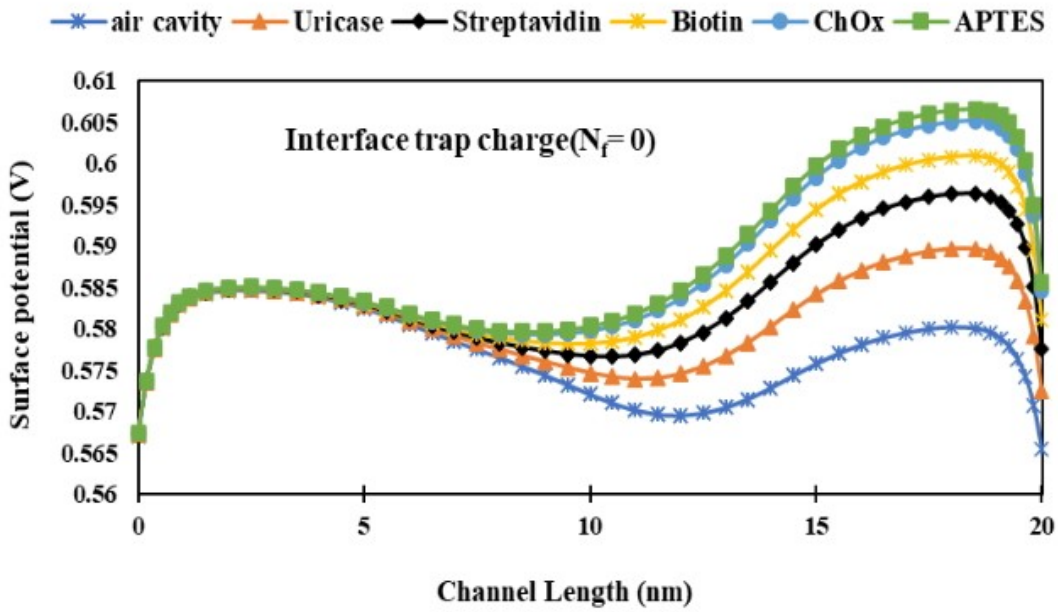

Figure 4. 11. Describes the effect of different biomolecules on surface potential as a function of channel length without ITC for n-substrate THM-GAA-JL-NWFET[2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Figure 4. 12 demonstrates the variation in surface potential profile along the channel length for different biomolecules on the THMG GAA JL NWFET in the case of a positively localized charge. The graph shows that the lowest surface potential rises in proportion to the dielectric constant. Near the drain end, a cavity of 10 nm length is considered. When biomolecules are uniformly immobilized in the cavity region, the potential changes from lower to higher due to the presence of biomolecules in the nanogap cavities at the drain end. Changes in surface potential and subthreshold current are observed when biomolecules are present in the nanogap cavity or vacuum gate dielectric due to changes in gate-to-channel capacitance over a larger area [13]. As shown in

Figure 4. 12, the dielectric constant value in the nanocavity region determines the surface potential of the portion of the channel (drain side) over which various biomolecules were immobilized. The surface potential on the source side of the device, which is not covered by dielectric materials, is lower. This leads us to the conclusion that the surface potential of the THM-GAA-JL-NWFET varies more when the dielectric materials of the nanogap cavity change. The shift in the surface potential can be utilized as a sensing metric to assess the presence of various biomolecules trapped within the nanocavity region.

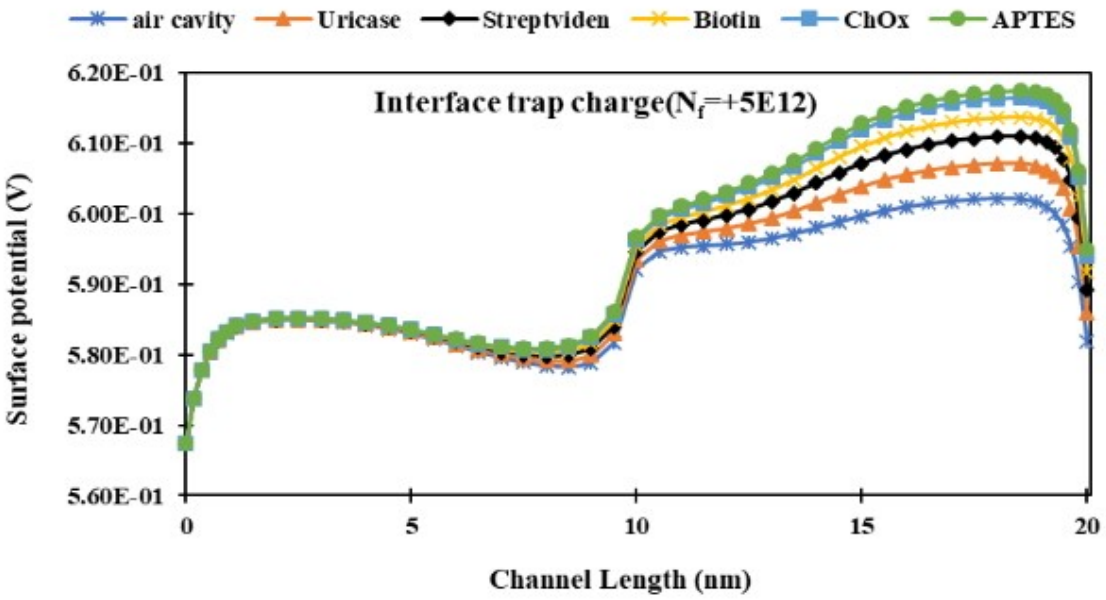

Figure 4. 12. Describes the effect of different biomolecules on surface potential as a function of channel length in the case of positive ITC for n-substrate THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

During the fabrication process, localized charges are produced. High-field-induced hot carriers will permanently damage the Si/SiO_2 interface near the drain side if the electric field is sufficiently strong. Further band bending caused by localized interface charges modifies the device's electrical performance. The density of localized charges and the capacitance of the gate oxide determine how much the flat-band voltage shifts. **Figure 4. 13** shows variation in surface potential profile with different biomolecules in the case of localized charges in the damaged drain side regions. In the case of the negative (positive) interface localized charges, the minimum surface potential appears in the negatively damaged region with respect to the undamaged region [9]. Hence, the shift in the lowest surface potential is due to the presence of localized charges. Degradation can be kept to a minimum by minimizing the potential channel changes caused by localized charges [13]. As shown in **Figure 4. 13**, positive and negative localized charges cause the surface potential to increase /decrease, respectively, with respect to the undamaged device. The significance of localized charges increases proportionally to the density of such charges. Higher surface potential difference is observed at the drain side for different biomolecule dielectric constants. This is because the drain side THM-GAA-JL-NWFET structure has a weak electric field due to a high dielectric constant.

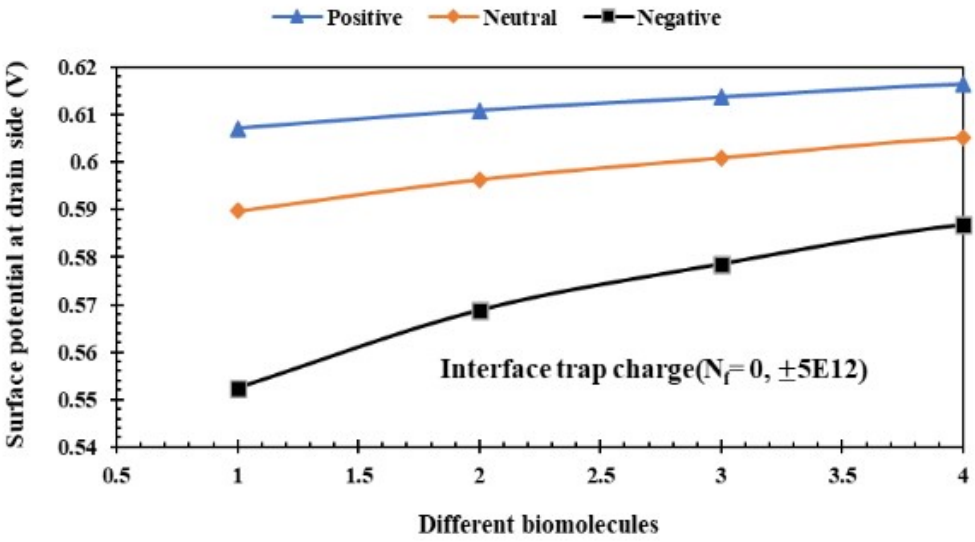

Figure 4. 13. Describes the effect of interface trap charges on surface potential in the case of different biomolecules for n-substrate THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

4.3.3.2 Impact of ITCs on Transfer Characteristics and Sensitivity

a) Subthreshold current

As threshold voltage, channel length, and gate oxide thickness decrease, high leakage current in nanoscale devices contributes significantly to power dissipation in CMOS circuits[63], [64]. When the gate-to-source voltage of a MOSFET is less than the threshold voltage, a current flows between the source and drain. This current is known as subthreshold conduction, sub-threshold leakage, or subthreshold drain current [3], [68]. Leakage current, also known as off current (I_{OFF}), is mostly caused by subthreshold current (i.e., weak inversion current) in the THM-GAA-JL-NWFET. It is essential to maintain a very low value for I_{OFF} in order to keep the circuit's standby power consumption to a minimum. This can be achieved by keeping I_{OFF} as low as possible. By introducing biomolecules in the nanogap cavity, the subthreshold slope can be reduced. Since biomolecules absorbed in the nanogap raise the gate capacitance, lowering subthreshold current and boosting device performance. The rapid increase in leakage current is also caused by the absorption of high k biomolecules in the cavity, which increases gate capacitance and decreases the threshold voltage roll-off. Effect of different biomolecules on subthreshold slope in the case of TCs is depicted in **Figure 4. 14**. Coupling between the gate and the charge carriers moving through the channel is enhanced when the cavity is filled with a variety of biomolecules ($K_{bio} > 1$). Also, subthreshold current is shown in **Figure 4. 14** to rise (decrease) due to the presence of positive (negative) localized charges.

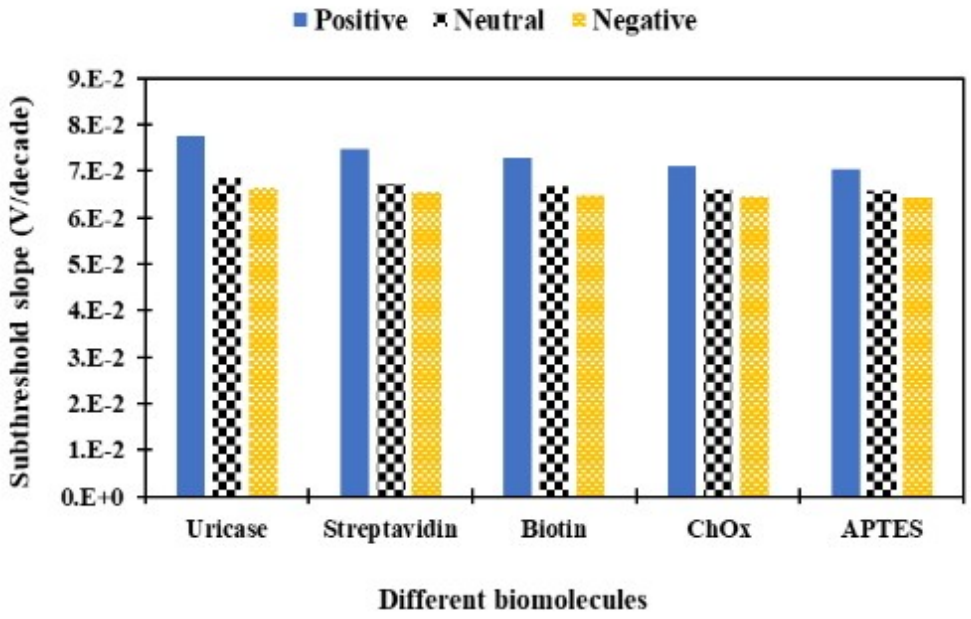

Figure 4. 14. Describes the effect of different biomolecules on subthreshold slope in the case of interface trap charges for n-substrateTHM-GAA-JL-NWFET[2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

b) Switching (I_{ON}/I_{OFF}) ratio

For switching applications, where a high value of on-current to off-current ratio (I_{ON}/I_{OFF}) is required, the variation introduced in I_{ON}/I_{OFF} due to localized charges is just as crucial as subthreshold degradation. Even though the drain current rises (reduced) when positive (negative) interface localized charges are present in all regions (subthreshold, linear, and saturation), the order of shift in the off-current is greater than the shift in the on-current. As a result, the overall result is an increased I_{ON}/I_{OFF} in the case of negative localized charges and decreased in the case of positive fixed charges as illustrated in

Figure 4. 15. In addition, the highest switching ratio is observed at the highest dielectric value, as clearly depicted in

Figure 4. 15. This leads to a low subthreshold slope at the highest dielectric value since the effective gate oxide capacitance increases as the cavity is filled with various biomolecules ($K_{bio} > 1$), which in turn increases the coupling between the gate and the charge carriers flowing through the channel. As a result, a biosensor with a low subthreshold slope will have a high degree of sensitivity. As shown in

Figure 4. 15, the density of negatively charged biomolecules is primarily responsible for the increase in the switching ratio.

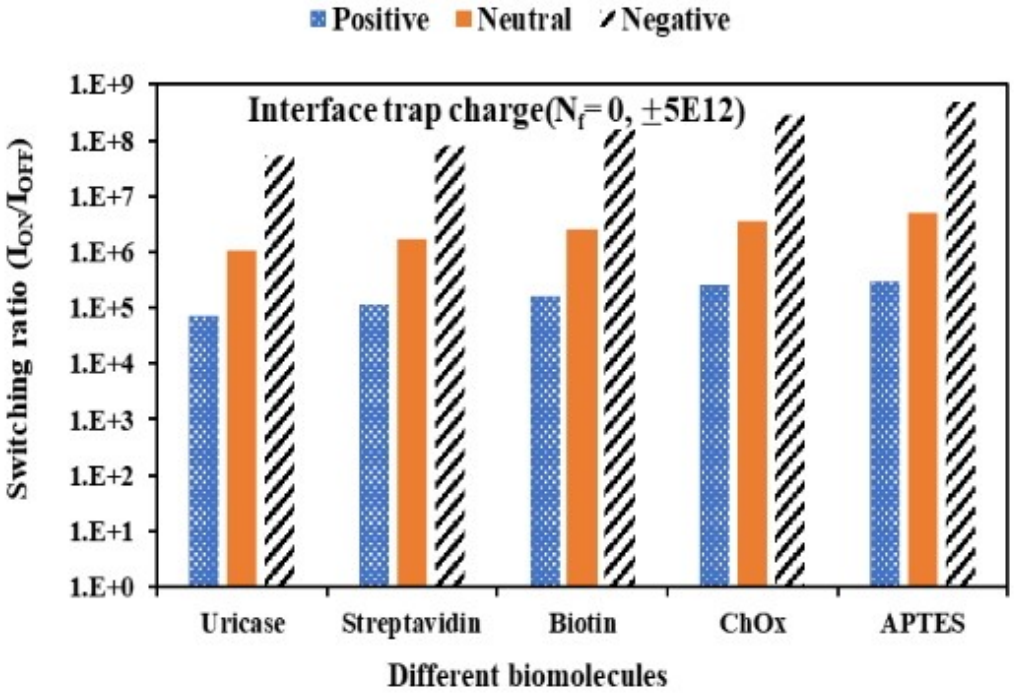

Figure 4. 15. Describes the effect of different biomolecules on the switching ratio in the case of interface trap charges for n-substrate THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

c) Shifting threshold voltage (ΔV_{th})

The threshold voltage of a MOSFET device is an important metric to investigate while studying device sensitivity [66], [67]. Every change in threshold voltage has an immediate and direct impact on the performance of the device. **Figure 4. 16** illustrates how the threshold voltage sensitivity (ΔV_{th}) of the THM-GAA-JL-NWFET varies with different biomolecules, and it can be obtained using **(eq.4.1).** The shift in threshold voltage induced by the gate oxide capacitance increases as $K_{bio} > 1$ value rises in addition to the density of localized charge as shown in **Figure 4. 16**. At the APTES biomolecule, for example, the shift threshold voltage is decreased by 30.40% and increased by 52.50%, respectively, for cases of positive and negative localized charge densities compared to an undamaged device. The density of the localized charges directly affects threshold voltage variations. This indicates that the change in the threshold voltage rises larger when there is a higher concentration of electrically charged particles. **Figure 4. 16** demonstrates that the rate of change of threshold voltage is higher for negatively localized charges in comparison to positively localized charges. This is because there has been a more significant shift in the minimum surface potential for negatively localized charges. Generally, changes in the flat-band voltage caused by positive and negative traps at the oxide-channel interface have a side effect on threshold voltage, drain current, and other performance metrics of MOSFET device. The formula for calculating the change in flat-band voltage is given in the equation (eq.4.6 &4.7).

$$\Delta V_{fb} = \frac{qN_f}{C_{OX}} \tag{4. 6}$$

$$C_{OX} = \frac{2\varepsilon_{OX}}{t_{Si} \ln(1 + \frac{2t_{OX}}{Si})} \tag{4. 7}$$

Where ε_{OX} is the permittivity of the oxide, q is the charge, t_{OX} is the thickness of the oxide, t_{Si} is the thickness of the silicon film and N_f is the interface charge density.

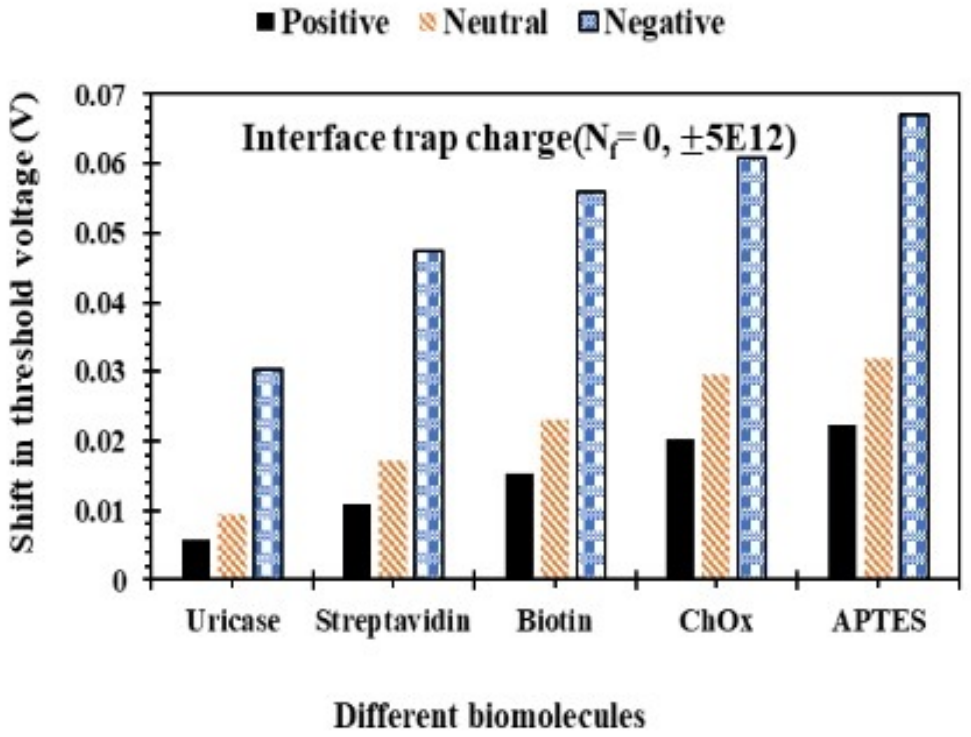

Figure 4. 16. Describes the effect of different biomolecules on shift threshold voltage in the case of interface trap charge for n-type THM-GAA-JL-NWFET[2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

d) Drain current sensitivity ($S_{I_{OFF}}$)

The effect of localized charges on the THM-GAA-JL-NWFET architecture's subthreshold drain current is depicted in **Figure 4. 17**. Since the subthreshold current is inversely proportional to the effective dielectric constant of the gate oxide, the sensitivity of the subthreshold current shift ($S_{I_{OFF}}$) has been decreasing as the biomolecule dielectric constant increases. When the value of the biomolecule K_{bio} increases, the capacitance of the gate oxide also increases, which gives the gate a greater ability to exert control over the flow of charge carriers [54]. Subthreshold current decreases with increasing dielectric constant of the biomolecule at constant gate voltage due to increased effective gate oxide capacitance. As depicted in **Figure 4. 17**, negatively charged biomolecules have a greater binding capacity than positively charged and neutral biomolecules.

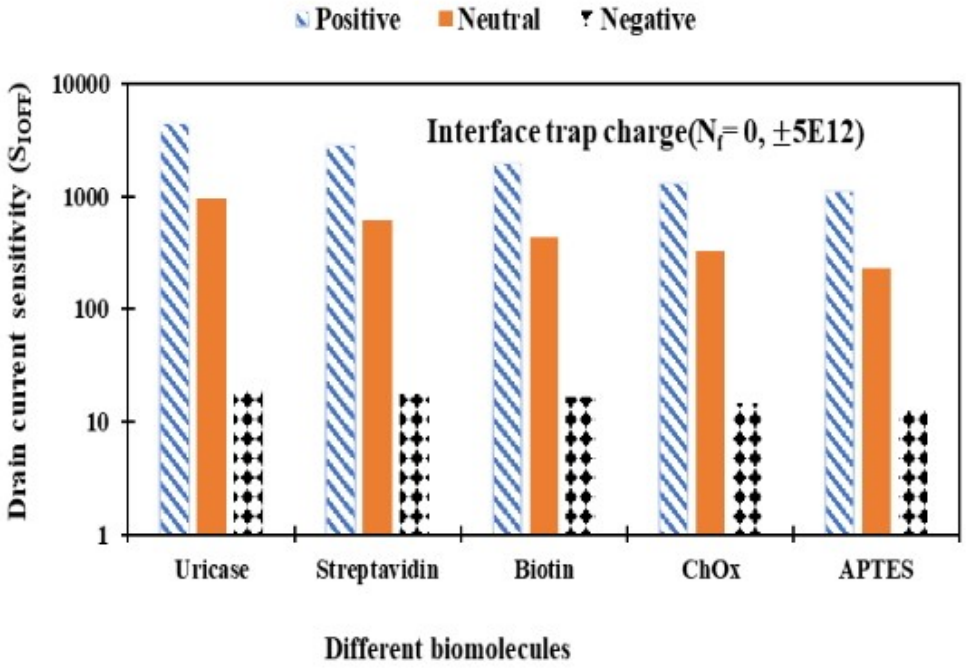

Figure 4. 17. Describes the effect of different biomolecules on drain current sensitivity in the case of interface trap charge for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

4.3.3.3 Impact of ITCs on Analog Performance

a) Transconductance (g_m)

The THM-GAA-JL-NWFET analog performance is measured by its transconductance (g_m), drain conductance (g_d), device efficiency, intrinsic voltage gin (A_V), and early voltage, among other characteristics. Transconductance is proportional to the transistor gain and measures how well the gate can regulate the drain current. The transconductance g_m of any device determines its gain; thus, its value should be high enough to have a high gain. g_m performance changes with gate voltage, and the peak value of g_m has been observed at low gate bias for the presence of positive and negative localized charges, as depicted in **Figure 4. 18**, while g_m decreases at high gate voltage due to mobility degradation. Transconductance decays as a consequence of a decrease in drain current caused by localized charges. In the subthreshold region, an increase (reduction) in transconductance is caused by positive (negative) fixed charges when V_{GS} is less than V_{th}. However, if the region is strongly inversion, as indicated by V_{GS} greater than V_{th}, the transconductance will be more significant for negatively localized charges than positive ones. Compared to the saturation region, the subthreshold and linear sections experience more significant degradation brought on by localized charges than the saturation region. This is due to the fact that when V_{GS} is greater than V_{th}, the influence of localized charges on band bending is reduced. The optimum direct current bias point for the device is determined by its transconductance at its maximum value. The value of transconductance is obtained using **(4. 3).** Therefore, transconductance measures the effectiveness of a MOSFET in controlling the current flow between the source and drain terminals, given a voltage applied to the gate terminal.

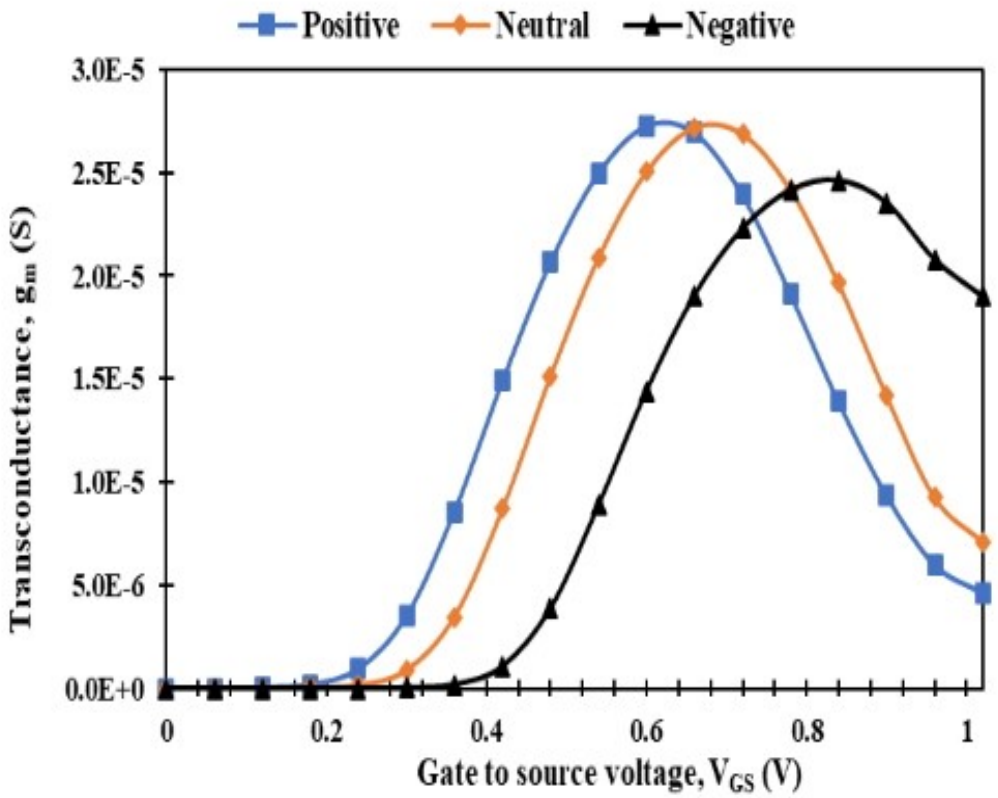

Figure 4. 18. Describes the effect of localized trap charges on transconductance for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.6V$).

b) Drain conductance (g_d)

Figure 4. 19 depicts the variation of g_d as a function of gate voltage with or without interface trap charges. Drain conductance (g_d) is also used to calculate the device's intrinsic gain. g_d is quite high in the linear area and begins to drop as drain voltages above the pinch-off voltage. In the saturation region, g_d performance is unaffected by changes in other parameters. As can be observed in **Figure 4. 19**, the increase in output resistance responsible for the considerable improvement in the analog performance and driving capabilities also completely suppresses the drain conductance under negative trap conditions.

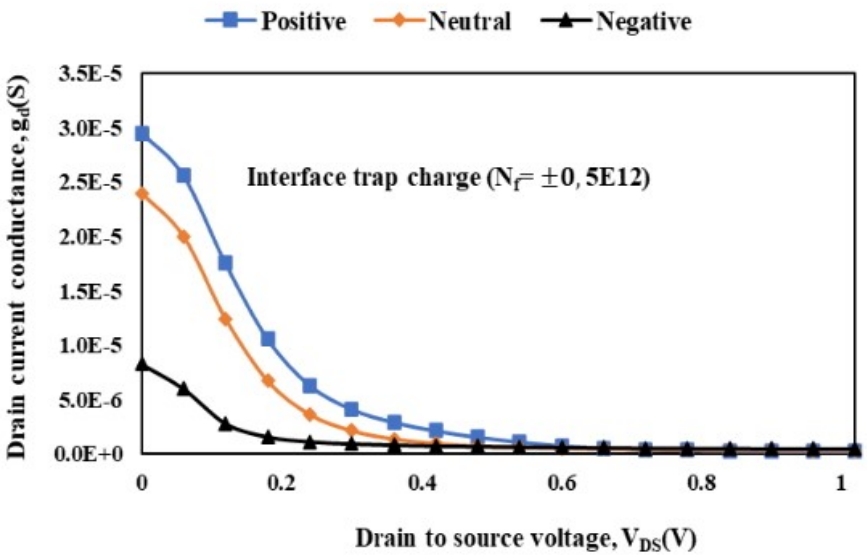

Figure 4. 19. Describes the effect of localized trap charges on drain conductance for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 0.6V$ and $V_{DS} = 1.0V$).

c) Intrinsic voltage gain (A_V)

Intrinsic gain (A_V) is defined as the ratio of transconductance (g_m) to output conductance (g_d) is obtained using **(4. 5)**. To achieve a larger A_V , the g_d value in analog circuit design should be lower. The intrinsic benefit is maximized by increasing the value of g_m and decreasing the value of g_d. The intrinsic gain value rises as a result of the negative trap charges depicted in

Figure 4. 20.

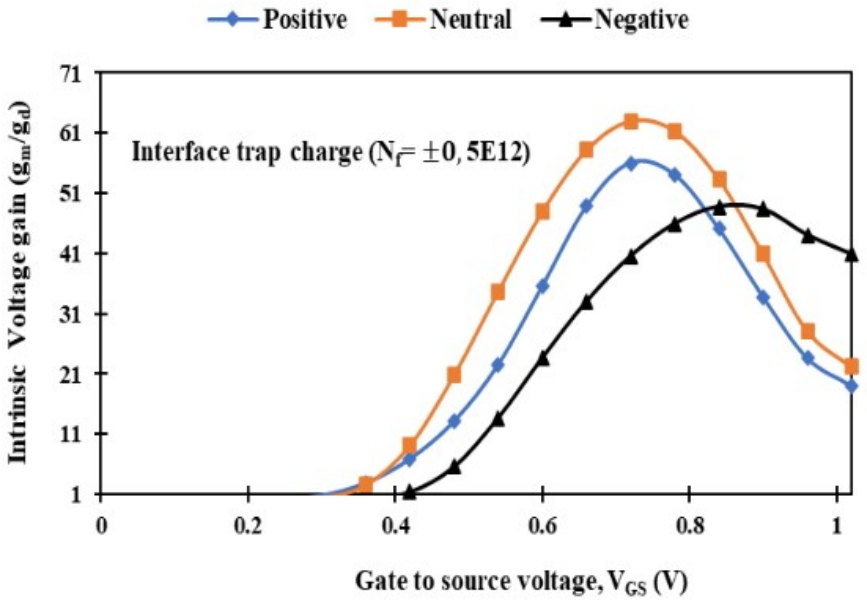

Figure 4. 20. Describes the effect of localized trap charges on intrinsic voltage gain for n-type triple hybrid metal GAA-JL NWFET[2], ($V_{GS} = 0.6V$ and $V_{DS} = 1.0V$).

d) Device efficiency (g_m/I_D)

Device efficiency, also referred to as the transconductance generation factor, is an essential parameter in the design of analog circuits that evaluates the effectiveness of the transconductance generation and is expressed by the formula (g_m/I_D) [57]. It refers to the efficiency of the device in amplifying or switching electronic signals. Device efficiency (g_m/I_D) ratio is a direct measure of the MOSFET's efficiency, as it shows the device's amplification (g_m) divided by the energy provided to produce this amplification (I_D). It is a metric for evaluating the degree to which the gate voltage regulates the drain current [68]. In analog applications, higher g_m/I_D ratios indicate more transconductance and, consequently, stronger capability to transfer DC power into AC gain performance at a given drain bias. **Figure 4. 21** illustrates the device efficiency performances with gate voltage variation for THM-GAA-JL-NWFET structures with and without traps. When the gate bias is very low, the device efficiency value is at its best, whereas in the strong inversion area, the device efficiency value is very low, reflecting the amount of power that any device is able to dissipate. Likewise, a device with a negative (positive) fixed charge has a more significant (smaller) g_m/I_D than undamaged device, as shown in **Figure 4. 21**.

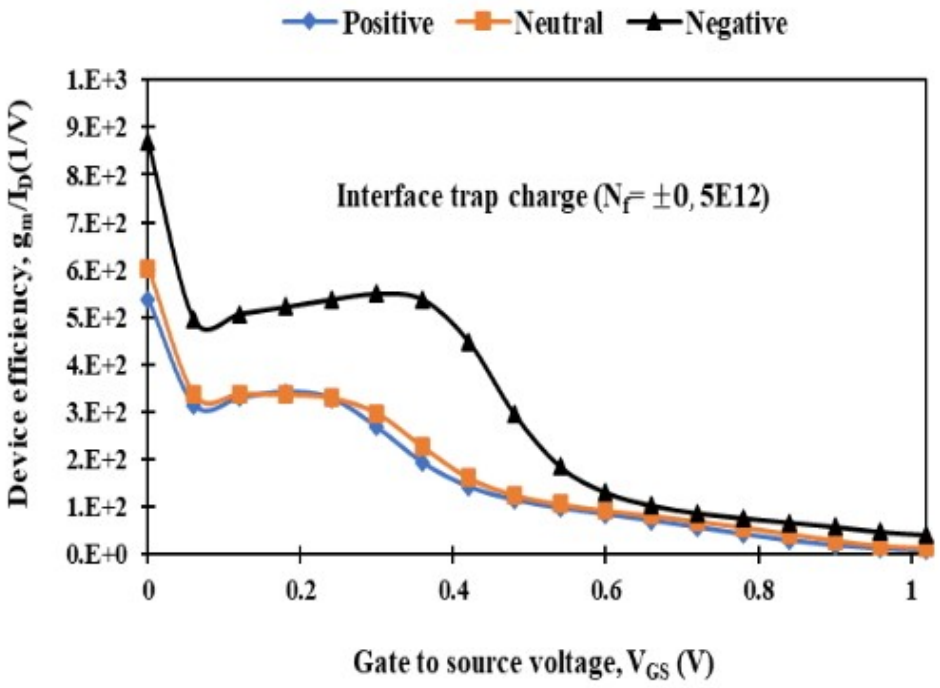

Figure 4. 21. Describes the effect of localized trap charges on device efficiency for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 0.6V$ and $V_{DS} = 1.0V$).

e) Early voltage (V_{EA})

The drain-source current through a MOSFET fluctuates as a function of the drain-source voltage, and the Early voltage characterizes this proportionality (V_{EA}), also known as the Early effect or the Early voltage coefficient. The voltage represents the MOSFET's output characteristic curve's slope. In electronic circuits, especially amplifier designs, it is a crucial

parameter for modelling the behavior of MOSFETs. The influence of localized charges on early voltage is depicted in **Figure 4. 22**. The effect of channel length modulation (CLM) can also be evaluated by monitoring the early voltage[57]. However, the early voltage performance of the THM-GAA-JL-NWFET device shows the exact opposite scenario. For better analog performance in MOSFET devices, the early voltage ($V_{EA} = I_D/g_m$) should be high. **Figure 4. 22** indicates that positive localized charges have a high early voltage value due to channel potential screening from increased drain bias. At the sub-threshold region, the early voltage value is extremely low. Yet, early voltage is improved as gate bias is increased [57]. For this reason, high-performance amplifier designs benefit significantly from the use of MOSFETs with a low Early voltage.

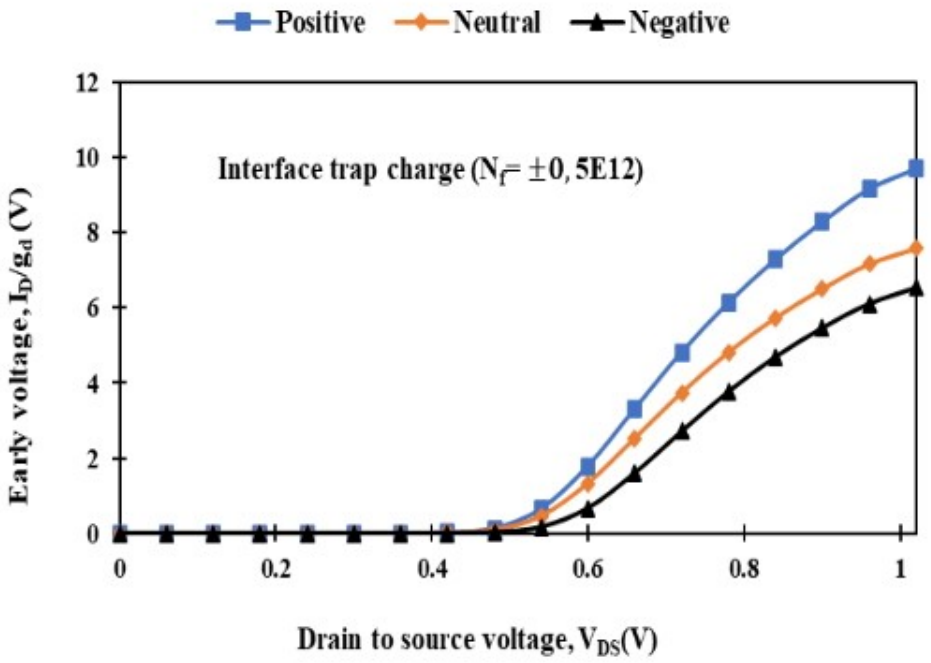

Figure 4. 22. Describes the effect of localized trap charge on early voltage for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 0.6V$ and $V_{DS} = 1.0V$).

f) Output Resistance ($R_{out} = 1/g_d$)

One of the most crucial characteristics of an analog device is its output resistance (R_{out})[1], [57]. This parameter is critical in determining the gain and stability of amplifiers and other electrical circuits that utilize MOSFETs. The voltage gain in an analog circuit is directly proportional to R_{out}. The output resistance model is vital for excellent reliability and scalability in MOSFET. In the case of interface trap charges, **Figure 4. 23** shows the output resistance ($1/g_d$) of the proposed device with various biomolecules. This highlights the value of increased small-signal output resistance, As the output resistance determines the MOSFET's intrinsic gain upper limit. As shown in **Figure 4. 23**, output resistance decreases/increases for positive (negative) interface trap charge with respect to undamaged region and decreases as biomolecule dielectric constant value increases. Therefore, output resistance is a crucial factor to take into account when considering which MOSFETs to employ.

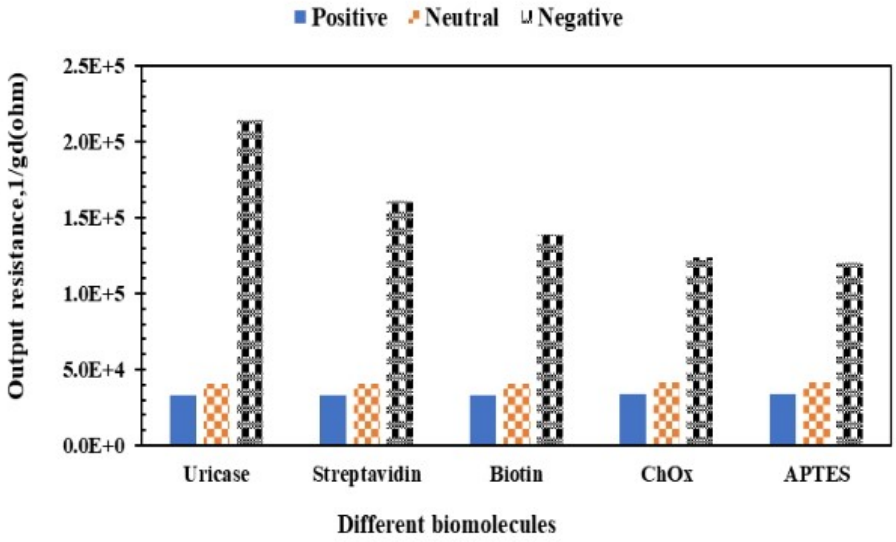

Figure 4. 23. Describes the effect of different biomolecules on output resistance in the case of interface trap charges for n-type THM-GAA-JL-NWFET [2], ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Generally, Interface trap charges have significant side effects, including a reduction in the subthreshold current due to an underlying shift in the slope of the subthreshold potential[19]. The device's subthreshold current needs to be low so that it can switch rapidly, resulting in substantial low power consumption[57]. Also, immobilized biomolecule in the nanogap cavity significantly impacts subthreshold current. **Table 4. 2** shows the impact of localized charges on drain current for three different biomolecules (Uricase $\varepsilon = 1.54$, Biotin $\varepsilon = 2.10$, and APTES $\varepsilon = 3.57$). When the dielectric constant of the cavity in a THM GAA-JL NWFET is increased, the device becomes more robust to the short channel effect. Hence, a higher dielectric constant provides better immunity against localized charges' degradation effects and immunity against short-channel effects. Thus, the performance degradation caused by localized charges depends also on the biomolecule dielectric constant value. **Table 4. 2** summarizes the impact of localized charges on I_{OFF}, I_{ON}, and I_{ON}/I_{OFF} where negative (positive) ITCs cause the ratio to increase (decrease), the main performance metrics for digital and sensing applications.

Table 4. 2: Impact of localized charges on I_{OFF}, I_{ON}, and I_{ON}/I_{OFF} for different biomolecules (Uricase $\varepsilon = 1.54$, Biotin $\varepsilon = 2.10$, and APTES $\varepsilon = 3.57$).

ITCs	I_{OFF}			I_{ON}			I_{ON}/I_{OFF}		
	Uricase	**Biotin**	**APTES**	**Uricase**	**Biotin**	**APTES**	**Uricase**	**Biotin**	**APTES**
0	4.50E-13	2.01E-13	1.24E-13	4.89E-7	5.01E-7	5.08E-7	1.09E+6	2.49E+6	4.09E+6
+5E12	7.11E-12	3.12E-12	1.79E-12	3.99E-7	4.42E-7	4.59E-7	5.61E+4	1.41E+5	2.56E+5
-5E12	8.60E-15	1.07E-15	5.10E-16	5.15E-7	5.31E-7	5.24E-7	5.99E+7	4.95E+8	1.03E+9

As is evident from **Table 4. 2**, I_{OFF} degradation is much more significant than I_{ON} degradation due to localized charges; thus subthreshold region is the worst affected region. Also, subthreshold degradation was observed in the presence of biomolecules in the nanogap cavity. Since localized charges degrade the device's subthreshold characteristics, they play a detrimental role when the device is to be used for switching and sensing applications. Since the switching ratio is the ratio of the on-to-off time of a MOSFET to its off-to-on time, it follows that faster switching times are preferable. Applications that demand rapid switching, such as power electronics, benefit from transistors with a high switching ratio and a low subthreshold current.

4.4 Summary

An accurate device modelling is crucial for predicting performance loss in future nanometer-scale device dimensions due to radiation damage, hot carrier damage, and process damage caused by localized charges. This chapter presents the impact of different ITCs on the electrical characteristics of new simple and computationally efficient double and triple hybrid metal gate dielectric modulated gate all around junctionless silicon nanowire FET-based biosensors. A step is introduced into the potential profile as a result of the presence of localized charges at the Si-SiO_2 interface. This step causes a shift in the threshold voltage of the device, as well as a degradation of the subthreshold current. Also, interface trap charges change shifting threshold voltage, switching ratio, transconductance, output conductance, intrinsic voltage gain, device efficiency, leakage current, and subthreshold slope in the presence of APTES biomolecule in both devices. For instance, the results of SS at negative ITCs are $(62.6 \text{ and } 60.3)\text{mV/decade}$ for double and triple hybrid metal gate devices, respectively. Improved switching ratio (4.18×10^6 and 4.12×10^8) and transconductance (7.88×10^{-6} and 1.90×10^{-5}) has been examined at negative ITC for double and triple THG-high-k-GAA-JL-NWFET, respectively, when APTEs biomolecule interacts in the nanogap cavity. Reduced and rising leakage currents due to negative and positive ITCs are, 93.6% and 1,343.5%, respectively, have been investigated in the proposed device with respect to undamaged region. Furthermore, a device with negative (positive) fixed charges has higher (lower) g_m/I_D than an undamaged device. For instance, at V_{GS}= 1.0V and V_{DS}=0.6V, g_m/I_D in case of negative (positive) localized charges is 46.9 % (16.34 %) higher (lower) than the undamaged for double gate device and 36.9% (66.2%) for triple gate device due to variation of g_m/I_D caused by variations in g_m and I_{ds} introduced by localized charges. Also, the impact of localized charge on electrical parameters of THM GAA JL NWFET with different biomolecules has been studied. The result verifies that the performance of the device is enhanced in negative than positive SiO_2 interface localized with respect to undamaged region.

Generally, in this study, negative ITC enhances the output characteristics, such as switching ratio, transconductance, device efficiency, and intrinsic voltage gain (A_V) of triple metal gate compared to double hybrid metal gate dielectric modulated gate-all-around junctionless silicon NWFET device, when different biomolecule interacts in the nanogap cavity. Our proposed device is a novel biomarker compared to single and double hybrid metal gate devices when different biomolecules interact in the nanogap cavity. When the device is going to be utilized in an environment sensitive to biomolecules, localized charges can be hazardous since they significantly impact how sensitive the device is to biomolecules. Because these localized charges are certain to be present in a practical device, an investigation into the estimation of performance degradation as a function of biomolecules is required in order for the device to be optimized in accordance with the results of the study. The next chapter will discuss the impact of different work functions on Numerical Modeling and gate optimization on the triple hybrid dielectric modulated junctionless gate all around SiNWFET-based biosensors.

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CHAPTER -5

Numerical modelling for triple hybrid gate optimization dielectric modulated junctionless gate all around SiNWFET based uricase and ChO_X biosensor

Abstract

This chapter presents an analytical model of a dielectric modulated junctionless surrounding-triple-hybrid metal(THM) gate SiNWFET-based uricase and ChO_X biosensor was developed at 40nm technology (20nm gate length) to study the impact of different gate engineering optimization effects with different metal work-functions on device performance. Using a parabolic approximation to solve Poisson's equation in a cylindrical coordinate system yields the surface-channel potential, which forms the basis of the mathematical study. The electrical parameters like surface channel potential, sub-threshold current, threshold voltage, and electric field are analyzed mathematically. Device characteristics such as cavity thickness, channel thickness, cavity length, and different gate electrode work functions are explored to optimize biosensing performance for uricase and ChO_X biomolecules. Three types of gate optimization (gate engineering), denoted by M_ϕ(4.86, 4.96 &4.50eV), O_ϕ(4.96, 4.86 &4.50eV), and Q_ϕ(4.86, 4.50 &4.96eV) each have three different metal work-function, have been incorporated as gate electrode including uricase and cholesterol oxidase (ChO_X) biomolecules coated within the nanocavity to determine their impact on the device's performance. Numerical simulations performed using ATLAS-TCAD simulator are used to verify and evaluate the analytical results, and they show excellent agreement with the simulated results. The study concludes that nanocavity coated with ChO_X dielectric and having tunable work-function optimized at "O" signifies better output results in device performance and in sensitivity metrics such as shifting threshold voltage, switching ratio, transconductance, intrinsic voltage gain, and device efficiency. For instance, the switching ratio in the case of ChO_X biomolecule for three different gate engineers (M, O, and Q) are $5.22*10^5$, $1.36*10^{6,}$ and $2.18*10^{4,}$ respectively. The study investigates that the proposed devices with optimizing gate electrode work function at "O" suggest new opportunities for future ultra-large-scale integration (ULSI) development and a viable competitor to deep-submicron mainstream MOSFETs for low-power applications in addition to its efficient device performance.

5.1 Introduction

Polysilicon with a double-type doping profile (P or N) has conventionally been used as conductive gate materials for bulk MOSFETs[1]–[3]. As CMOS technology continuously scales down to ultra-small device size[4]–[6], metal gate electrodes need to be presented to alleviate harmful effects of the doped polysilicon gate, like high parasitic resistance, gate electrode depletion, and power consumption[3], [7]. A depletion layer near the polysilicon/oxide interface is developed due to reduced active dopant levels in the polysilicon gate when the device is biased in strong inversion, which in turn results in dishonored device characteristics[8], the so-called polysilicon depletion or poly-depletion effect [9] and leads to capacitance and drain current value reduction in addition to the undesirable variation of the threshold voltage due to unexpected electronic circuit output results and polysilicon depletion effect[9]. To reduce those polysilicon depletion effects like threshold voltage roll-off, parasitic gate resistance, and short channel effects (SCEs)[11], optimizing gate electrodes with tunable (high metal) work functions instead of the polysilicon gate is crucial[12]–[14] under the high-k dielectric gate oxide[15]. Also, different researchers inspect various approaches like surrounded gate metals[16], fully silicide gates, multi-gate device structures[2], [17], and composite metal gates with tunable work functions[18] to curtail polysilicon depletion effects. Different researchers' evidence approved that metal gate electrodes with high work function used as gate electrodes (interface) to alleviate problems caused by a polysilicon gate in the enhancement of ultra-small scall devices [19]. Since “gate resistance-capacitance delay becomes a critical concern in designing electronic circuits with very short and thin gate oxides” [11], [20] under small-scale dimensions. Unlike polysilicon electrodes, which have two work-function only (N or P, type), electrodes(metal) can set almost any work function for CMOS devices. Currently, different researchers have proved that the tuned work function lies between 4.50eV and 5.00eV and effectively operates for CMOS transistors[15], [21], [22] under high-k dielectric gate oxide in ultra-small scall device development since tunable electrode work-function is crucial in determining the appropriate threshold voltage values and suppresses short channel effects[21], [23]. In ultra-small scale device architecture, not only the polysilicon gate but also the fabrication process for NWFET is difficult due to the severe doping necessities at (drain, channel, and source) in the area of nano dimension gaps[24], [25], and the gate has less control over the drain current. These challenges in fabricating process of NWFETs are addressed by developing junctionless (JL) FETs since there are no doping concentration gradients between the source and drain(in the device)[24], [26], [27] even if the device is heavily-doped. To eliminate the junction from the transistor and make it junctionless, the doping profile should be uniform in the source/drain and substrate regions. Because basic physical properties such as drain-induced barrier lowering (DIBL) sub-threshold swing, parasitic resistance, transconductance, I_{ON}/I_{OFF} ratio, and other physical properties have been improved in the junctionless phenomenon [28].

Furthermore, the gate-all-around (GAA) architecture allows comprehensive drain current gate control[16], [29]. The voltage applied across the gate terminal controls the rate at which electrons can flow through the wire. An electrically separated metal electrode serves as the gate in the GAA JL-NWFET, which makes use of NW of silicon.

Advanced device structures like multi-metal gate and junctionless gate-all-around (GAA) nanowire FETs have received crucial attention due to better scalability and amended capacitive coupling in gate-to-channel regions[30]. However, optimization of gate electrode work function on the multi-gate uricase and ChO_X biosensor devices have not yet been well investigated in the ultra-small scale device dimension[31]. Different works explore that, SiNWFET-based uricase and ChO_X biosensors have low cost, low power consumption, and easy-to-use on-site monitoring, even by non-medical staff, to achieve effective surveillance of blood metabolites at home[32], [33]. The prime origins of mortality and disability linked to abnormal glucose concentration problems are caused by an imbalance of blood metabolites and diabetes[34], [35]. So, controlling and managing the amounts of uric acid, cholesterol, and glucose concentration in human fluids is essential for living a healthy life[35]. As a result, SiNWFET-based uricase and ChO_X biosensors have been actively investigated to detect cholesterol[36], uric acid[37], [38], and glucose concentration due to their high sensitivity, simplicity, and low cost[37], [39], [40] and their higher specific surface area for enzyme immobilization than planar electrodes, which improves sensitivity[41], [42] when uricase and ChO_X biomolecules are immobilized in the nanogap cavity in the form of an aqueous solution.

In this chapter, we have proposed to study optimization of different gate electrode work-function on the electrical output properties, such as drain current (I_{DS}), sub-threshold swing (S), transconductance(g_m), threshold voltage(V_{th}), surface potential, device efficiency (g_m/I_{DS}), output conductance(g_d), switching ratio(I_{ON}/I_{OFF}), intrinsic voltage gain (g_m/g_d) by modelling triple hybrid metal gate dielectric modulated junctionless gate all around SiNWFET-based uricase and ChO_X biosensor.

5.2 Device Structure and Simulation Models

5.2.1 Device Structure

The designed structure for n-type triple hybrid metal gate dielectric modulated junctionless gate all around NWFET-based uricase and ChO_X biosensor has been proposed, as shown in **Figure 5. 1**. Here L_1 (6nm), L_2 (8nm) L_3 (6nm) are the lengths of the gate $\mathbf{G_1(\Phi_1)}$, $\mathbf{G_2}$ $\mathbf{(\Phi_2)}$ and $\mathbf{G_3(\Phi_3)}$ respectively and L_4 (10nm) are the length of the nanogap cavity and silicon dioxide (SiO_2) which are near to drain and source end, respectively, where ($L_{ch} = L_1 + L_2 + L_3 = 20nm$) is the length of hafnium oxide dielectric (HfO_2) and an interface layer oxide (SiO_2). T_{high-K}, $T_{bio}$and T_{OX} are the thickness of hafnium oxide ($\in = 25$), biomolecule cavity, and interface ($SiO_2, \in = 3.9$) gate oxides, respectively, and 2R is the channel's diameter (silicon film thickness). All of the technology parameters and power supplies align with what the ITRS roadmap recommends [43] for 20 nm gate-length technology. Three different gate optimization techniques are designed on n-channel surrounding gate MOSFET to realize the effect of gate materials on device performance. The target biomolecules (Uricase $\in = 1.54$ and $ChO_X, \in = 3.30$) are detected in the cavity region and assumed to be immobilized and interact with the cavity uniformly[44]. Doping concentration $N_D = 1x10^{19}cm^{-3}$ is applied uniformly for TM-GAA-JL-NWFET from source to drain through the channel regions to study the impacts of gate work-function variation. Since Hafnium dioxide ($HfO_2, \varepsilon = 25$) has a higher permittivity

than silicon dioxide ($SiO_2, \varepsilon = 3.9$), it is employed as the gate oxide material in this analysis, with an effective oxide thickness (EOT) considered T_{High-K} corresponds to 1.5nm, as shown in **Table 5. 1**. The proposed device calibration output result has been authenticated with the experimental results of papers[46].

Table 5. 1: Designed parameters for THM-high-k GAA-JL-SiNWFE.

Physical Parameters			Parameter values
Channel length (nm)			20.00
High-k (HfO_2) Oxide thickness (nm)			1.50
Interface Oxide thickness SiO_2 (nm)			0.30
Nanogap cavity length (nm)			10.00
Length/thickness of Source/Drain (nm)			10.00
Thickness of nanogap cavity (nm)			1.00
Silicon film diameter (nm)			10.00
Source/Drain & Channel Doping (N_D+)			$10^{19}cm^{-3}$
Oxide Dielectric constant, HfO_2 & SiO_2)			25.00 & 3.90
Gate work-function variables	Gate work-function values (Φ)		
	$\boldsymbol{\Phi_1(eV)}$	$\boldsymbol{\Phi_2(eV)}$	$\boldsymbol{\Phi_3(eV)}$
M	4.86	4.96	4.50
O	**4.96**	**4.86**	**4.50**
Q	4.86	4.50	4.96

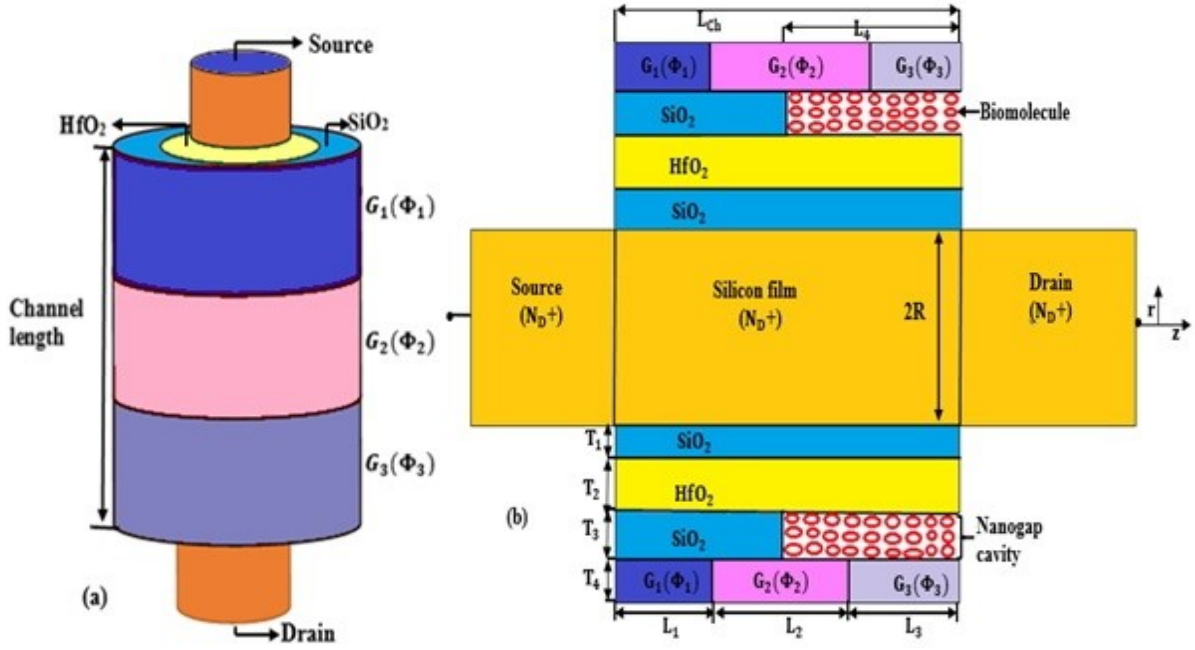

Figure 5. 1. Illustrates **(a)** 3D representation diagram and (**b)** 2D view of n-type triple hybrid metal gate dielectric modulated gate all around JL-NWFET.

5.2.2 Simulation Models

Using the ATLAS-3D device simulator tool, several simulations were carried out to analyze the electrical properties of dielectric modulated triple hybrid metal GAA JL-NWFETs with different gate engineering, including uricase and cholesterol oxidase (ChO_X) neutral biomolecules along the materials specified in **Table 5. 1**. We incorporate carrier recombination and generation models for carrier mobility in the simulation. Concentration-dependent mobility (CONMOB)[47] and bandgap narrowing (BGN) models are applied to verify doping versus mobility and high channel doping profile (for doping profile is more significant than $10^{18} cm^{-3}$). Ignoring impact ionization effect, Boltz–man transport and Shockley–Read–Hall (SRH) models account for the recombination of minority carriers within the semiconductor[47]. The Lombardi CVT mobility model accounted for field-dependent mobility in perpendicular/parallel [47] at room temperature(300K). Furthermore, two numerical methods, Newton and Gummel [47], have been considered to obtain better convergence when obtaining numerical solutions. Due to the channel's radius being more significant than 4nm, the simulation does not consider the Quantum confinement effect.

Table 5. 2: Model parameters applied in the simulations [47].

Physical models	**Parameter**	**Value and unit**
(SRH) Shockley–Read–Hall carrier recombination	$TAUN_0$ $TAUP_0$	1.0×10^{-7}S 1.0×10^{-7}S
(BEN) Bandgap narrowing	BGN.E BGN.N	6.92×10^{-3}V $1.310^{17}\mathrm{cm}^{-3}$
Lombardi CVT mobility	BN.CVT BP.CVT	$4.75 \times 10^{7}\mathrm{cm}/(\mathrm{s})$ $9.925 \times 10^{6}\mathrm{cm}/(\mathrm{s})$

Table 5. 3: Constant parameters applied in this simulation [47].

Parameters	**Symbols**	**Values and units**
Electron affinity of silicon	χ_{Si}	~4.17eV
Silicon Bandgap Energy	E_g	~1.08eV
Permittivity of silicon	ε_{Si}	11.8
Boltzmann constant	K_B	$\sim 1.381 \times 10^{-23}\mathrm{JK}^{-1}$
Electronic charge	q	$\sim 1.6\mathrm{x}10^{-19}\mathrm{C}$
Room Temperature	T	300K
Planck's constant	h	$\sim 6.63\mathrm{x}10^{-34}\mathrm{JS}$
Silicon intrinsic carrier concentration	n_i	$\sim 1\mathrm{x}10^{10}\mathrm{cm}^{-3}$

5.3 Potential and Subthreshold Current Modeling

5.3.1 Surface Potential Analysis

A higher source to drain metal gate work function in small channel radius junctionless transistors enables the metal gate to deplete the silicon channel safely [48]. The channel portion of the proposed device shown in **Figure 5. 1(b)** is divided into three distinct regions for the potential distribution's analytical expressions. Assuming uniform impurity doping concentration ($N_D = 1 \times 10^{19} cm^{-3}$) through the channel. The $Si - SiO_2$interface is considered to be free of trap charges. Based on this assumption, Poisson's equation in corresponding regions ignoring source/drain depletion regions in the electrostatic potential $\varphi(r, z)$ calculation is written as;

$$\frac{1}{r}\frac{\partial}{\partial r}\varphi_1(r,z)+\frac{\partial^2}{\partial r^2}\varphi_1(r,z)+\frac{\partial^2}{\partial z^2}\varphi_1(r,z)=-\frac{-qN_D}{\varepsilon_{Si}} \quad (5.1)$$

$For \;\; 0 \le z \le L_1 \;, \; 0 \le r \le R$

$$\frac{1}{r}\frac{\partial}{\partial r}\varphi_2(r,z)+\frac{\partial^2}{\partial r^2}\varphi_2(r,z)+\frac{\partial^2}{\partial z^2}\varphi_2(r,z)=-\frac{-qN_D}{\varepsilon_{Si}} \quad (5.2)$$

$For \;\; L_1 \le z \le L_1 + L_2 \;, \; 0 \le r \le R$

$$\frac{1}{r}\frac{\partial}{\partial r}\varphi_3(r,z)+\frac{\partial^2}{\partial r^2}\varphi_3(r,z)+\frac{\partial^2}{\partial z^2}\varphi_3(r,z)=-\frac{-qN_D}{\varepsilon_{Si}} \quad (5.3)$$

$For \;\; L_1 + L_2 \le z \le L \;, \; 0 \le r \le R$

Where L_1, L_2 and L_3 are for region-I, region-II, and region-III channel/gate lengths. The channel's potential distribution is denoted by $\varphi_i(r, z)$", q" is the electronic charge, the homogeneous silicon film (channel) doping density is N_D, and the permittivity of silicon channel (Si) is ε_{Si}. The electrostatic potential $\varphi_i(r, z)$ is solved using the superposition technique and split into $V_i(r)$ and $U_i(r, z)$ was written as;

$$\varphi_i(r,z) = V_i(r) + U_i(r,z) \; for \; i=1, \; 2 \; \& 3 \quad (5.4)$$

Applying a one-dimensional solution of Poisson's and two-dimensional solutions to the homogeneous Laplace equation with boundary conditions, for (eq. **(5. 4)** i.e.

$$\frac{1}{r}\frac{\partial V_i(r)}{\partial r}+\frac{\partial^2 V_i(r)}{\partial r^2}=-\frac{-qN_D}{\varepsilon_{Si}} \; and \; i=1, \; 2 \; \& 3. \quad (5.5)$$

$$\frac{1}{r}\frac{\partial U_i(r,z)}{\partial r}+\frac{\partial^2 U_i(r,z)}{\partial r^2}+\frac{\partial U_i(r,z)}{\partial z}=0 \; and \; i=1, \; 2 \; \& 3. \quad (5.6)$$

Since the electric field at the center of the silicon channel is vanished [49].

$$\left.\frac{\partial \varphi_i(r,z)}{\partial r}\right|_{r=0} = 0, \; i=1, \; 2 \; \& 3. \quad (5.7)$$

and there is a continuous electric field at the interface of (Si/SiO_2);

$$\left.\frac{\partial \varphi_i(r,z)}{\partial r}\right|_{r=R} = \frac{\varepsilon_{OX}}{\varepsilon_{Si} t_{OXeff}}\left[V_{gs} - \phi_{M_iS} - \varphi_i(r=R,z)\right],\ i=1,\ 2\ \&3. \tag{5. 8}$$

Here ϵ_{OX} is the dielectric constant of SiO_2, ϵ_{HfO_2} is the dielectric constant of HfO_2, t_{OXeff} is effective oxide thickness (EOT) obtained using the gate stack ($SiO_2 + HfO_2$) [50], [51]is given by;

$$t_{OX\ eff} = t_1 + \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} t_2 \tag{5. 9}$$

Where t_1 and $t_2$are the thicknesses of SiO_2 and HfO_2 respectively and Φ_{M_iS} are gate and channel work-function differences given by;

$$\phi_{MS} = \phi_M - \phi_{Si} \tag{5. 10}$$

Where $\Phi_M$stands metal work-functions and ϕ_{Si} stands silicon channel work function, written as[47];

$$\phi_{Si} = \chi_{Si}(T=300K) + q\phi_F + \frac{E_g(T,N_D)}{2q} \tag{5. 11}$$

$$\phi_F = \frac{KT}{q} ln\left(\frac{n_i}{N_D}\right) \tag{5. 12}$$

Here, ϕ_F is channel's Fermi potential χ_{Si} is the silicon electron affinity, n_i is inherent carrier concentration and $E_g(T, N_D)$ are temperature and doping dependent on silicon bandgap energy [47];

$$E_g(T,N_D) = E_g(300k) + E_{g\alpha}\left(\frac{(300K)^2}{300K + Eg\beta} - \frac{T^2}{T + E_{g\beta}}\right) - \Delta E_g(N_D) \tag{5. 13}$$

E_g(300K) specifies the energy band gap at 300K, $E_{g\alpha} = 4.73 \times 10^4$eV/K and $E_{g\beta} = 636$K. $\Delta E_g(N_D)$ is the amount of energy needed to narrow the bandgap due to high doping[47];

$$\Delta E_g(N_D) = \beta_E x\left\{ln\left(\frac{N_D}{\beta_N}\right) + \left[\left(ln\left(\frac{N_D}{\beta_N}\right)\right)^2 + \beta_c\right]^{1/2}\right\} \tag{5. 14}$$

Where $\beta_E = 6.92$meV, $\beta_N = 1.3 \times 10^{17}\text{cm}^{-3}$ and $\beta_C = 0.5$ [47]. From eq. **(5. 5**) to **(5. 10**) solutions $V_i(r,)$ can be obtained as follows;

$$V_i(r) = \frac{qN_D}{4\varepsilon_{Si}} r^2 + V_{gs} - V_{fbi} + \frac{qN_D R^2}{4\varepsilon_{Si}} + \frac{qN_D R}{2C_{OX}},\ i=1,2,3. \tag{5. 15}$$

Here C_{OX} is the gate-oxide capacitance. Electron affinity and flat-band voltage of the channel are given as follows;

$$\chi_{Si(T)} = \chi_{Si(300K)} + \beta_c\left[E_{g(T)} - E_{g(300K)}\right] \tag{5. 16}$$

$$V_{fbi}=\left\{\phi_{M1}-\left(\chi_{Si(T)}+\frac{E_g(T,N_D)}{2}-q\phi_f(T)\right)\right. \tag{5. 17}$$

For i=1, $0 \le z \le L_1$

$$V_{fbi}=\left\{\phi_{M2}-\left(\chi_{Si(T)}+\frac{E_g(T,N_D)}{2}-q\phi_f(T)\right)\right.\pm\frac{qN_F}{C_{OX}} \tag{5. 18}$$

For i=2, $L_1 \le z \le L_1+L_2$

$$V_{fbi}=\left\{\phi_{M3}-\left(\chi_{Si(T)}+\frac{E_g(T,N_D)}{2}-q\phi_f(T)\right)\right.\pm\frac{qN_F}{C_{OX}} \tag{5. 19}$$

For i=3, $L_1+L_2 \le z \le L_1+L_2+L_3=L$

The general solution for $U_i(r,z)$ using Fourier–Bessel series and separation of variable approach is [49];

$$U_i(r,z)=\sum_{n=1}^{\infty}\left[A_{ni}e^{\left(\frac{\alpha_n z}{R}\right)}+B_{ni}e^{\left(\frac{-\alpha_n z}{R}\right)}\right]J_0\left(\frac{\alpha_n r}{R}\right),i=1,2,3. \tag{5. 20}$$

where A_{ni} and B_{ni} are coefficients and α_n is eigenvalue calculated using the following equation [52] given as;

$$\frac{\varepsilon_{OX}R}{t_{OXeff}}J_0(\alpha_n)-J_1(\alpha_n)\alpha_n=0 \tag{5. 21}$$

The first kind Fourier-Bessel function of order i, is denoted by $J_i(x)$[52]. Coefficients of Fourier-Bessel series $A_{n1}, B_{n1}, A_{n2}, B_{n2}, A_{n3}$, and B_{n3} are determined based on the boundary conditions. Assuming that source-drain depleted region potential is independent of "r. ", **(e.q. 5.1)** is written using Poisson's equation;

i) At the source end, electrostatic potential is written as;

$$\varphi_1(r,z)\big|_{z=0}=V_{bi} \tag{5. 22}$$

Here V_{bi} is built potential.

ii) At the drain end, electrostatic potential is written as;

$$\varphi_3(r,z)\big|_{Z=L}=V_{bi}+V_{ds} \tag{5. 23}$$

Where V_{DS} is drain bias voltage; and interface electric potential in the three regions is continuing and expressed as;

$$\varphi_1(r,z)\big|_{Z=L_1}=\varphi_2(r,z)\big|_{Z=L_1} \tag{5. 24}$$

$$\varphi_2(r,z)\big|_{Z=L_1+L_2}=\varphi_3(r,z)\big|_{Z=L_1+L_2} \tag{5. 25}$$

Interface electric fields in the three areas are written as;

$$\left.\frac{\partial\varphi_1(r,z)}{\partial z}\right|_{Z=L_1} = \left.\frac{\partial\varphi_2(r,z)}{\partial z}\right|_{Z=L_1} \tag{5. 26}$$

$$\left.\frac{\partial\varphi_2(r,z)}{\partial z}\right|_{Z=L_1+L_2} = \left.\frac{\partial\varphi_3(r,z)}{\partial z}\right|_{Z=L_1+L_2} \tag{5. 27}$$

Coefficients $A_{n1}, B_{n1}, A_{n2}, B_{n2}, A_{n3}$, and B_{n3} of equation (5. 20) is obtained using Fourier–Bessel series and boundary conditions (**eq.(5.** 22 **and (5.** 27**)** as [52];

$$A_{n1} = \left[-T_{n1} e^{\left(\frac{-\alpha_n L}{R}\right)} + T_{n2}\cosh\frac{a_n(L_1-L)}{R} + T_{n3}\cosh\frac{a_n(L_1+L_2-L)}{R} + T_{n4} \right] x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5.28}$$

$$B_{n1} = \left[T_{n1} e^{\left(\frac{\alpha_n L}{R}\right)} - T_{n2}\cosh\frac{a_n(L_1-L)}{R} - T_{n3}\cosh\frac{a_n(L_1+L_2-L)}{R} - T_{n4} \right] x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5.29}$$

$$A_{n2} = \left\{ \left[-T_{n1} + T_{n2}\cosh\frac{\alpha_n L_1}{R} \right] e^{\left(-\frac{\alpha_n L}{R}\right)} - T_{n3}\cosh\frac{\alpha_n(L_1+L_2-L)}{R} + T_{n4} \right\} x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5.30}$$

$$B_{n2} = \left\{ \left[T_{n1} - T_{n2}\cosh\frac{\alpha_n L_1}{R} \right] e^{\left(\frac{\alpha_n L}{R}\right)} + T_{n3}\cosh\frac{\alpha_n(L_1+L_2-L)}{R} - T_{n4} \right\} x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5. 31}$$

$$A_{n3} = \left\{ \left[-T_{n1} + T_{n2}\cosh\frac{\alpha_n L_1}{R} + T_{n3}\cosh\frac{\alpha_n(L_1+L_2)}{R} \right] e^{\left(\frac{-\alpha_n L}{R}\right)} + T_{n4} \right\} x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5. 32}$$

$$B_{n3} = \left\{ \left[T_{n1} - T_{n2}\cosh\frac{\alpha_n L_1}{R} - T_{n3}\cosh\frac{\alpha_n(L_1+L_2)}{R} \right] e^{\left(\frac{\alpha_n L}{R}\right)} - T_{n4} \right\} x \left(2\sinh\frac{\alpha_n L}{R} \right)^{-1} \tag{5. 33}$$

$$\text{Where } T_{n1} = V_{bi} S_{no} - S_{n1} \tag{5. 34}$$

$$T_{n2} = S_{n2} - S_{n1} \tag{5. 35}$$

$$T_{n3} = S_{n3} - S_{n2} \tag{5. 36}$$

$$T_{n4} = (V_{bi} - V_{DS}) S_{no} - S_{n4} \tag{5. 37}$$

$$S_{no} = \frac{2J_1(\alpha_n)}{\alpha_n \left[J_1^2(\alpha_n) J_0^2(\alpha_n) \right]} \tag{5. 38}$$

$$\text{and } S_{ni} = V_{GS} S_{no} - U_{ni} \tag{5. 39}$$

$$\text{where } U_{ni} = -\left[\Phi_{MiS} + \frac{qN_{Dit_{OXeff}R}}{2\varepsilon_{OX}} + \frac{qN_{Di}R^2}{4\varepsilon_{Si}} \right] S_{no} + \frac{qN_{Di}\left[R^2\alpha_n J_1(\alpha_n) - 2R^2 J_2(\alpha_n) \right]}{2\varepsilon_{Si}\left[J_1^2(\alpha_n) + J_0^2(\alpha_n)\alpha_n^2 \right]} \tag{5. 40}$$

Differentiating surface potential $\varphi(r = R, Z)$ with respect to z, gives channel electric field $E(z)$ in the z-direction.

$$E_i(z) = \sum_{n=1}^{\infty} A_{ni} e^{\left(\frac{\alpha_n z}{R}\right)} - B_{ni} e^{\left(\frac{\alpha_n z}{R}\right)} \times \left(\frac{\alpha_n}{R} \right) J_o(\alpha_n), \text{ where } i=1,2,3 \tag{5. 41}$$

Figure 5. 2 shows the analytical and simulating results of surface potential in the case of uricase and ChO_X biomolecules for THM GAA-JL-SiNWFET. The simulation findings can be utilized to optimize the device's performance by providing a comprehensive understanding of the

device's behavior. The ATLAS TCAD simulation results and analytical models are consistent with one another. This ensures the accuracy and reliability of the models and simulations, giving engineers and researchers confidence in their abilities to make design and optimization decisions for electrical devices.

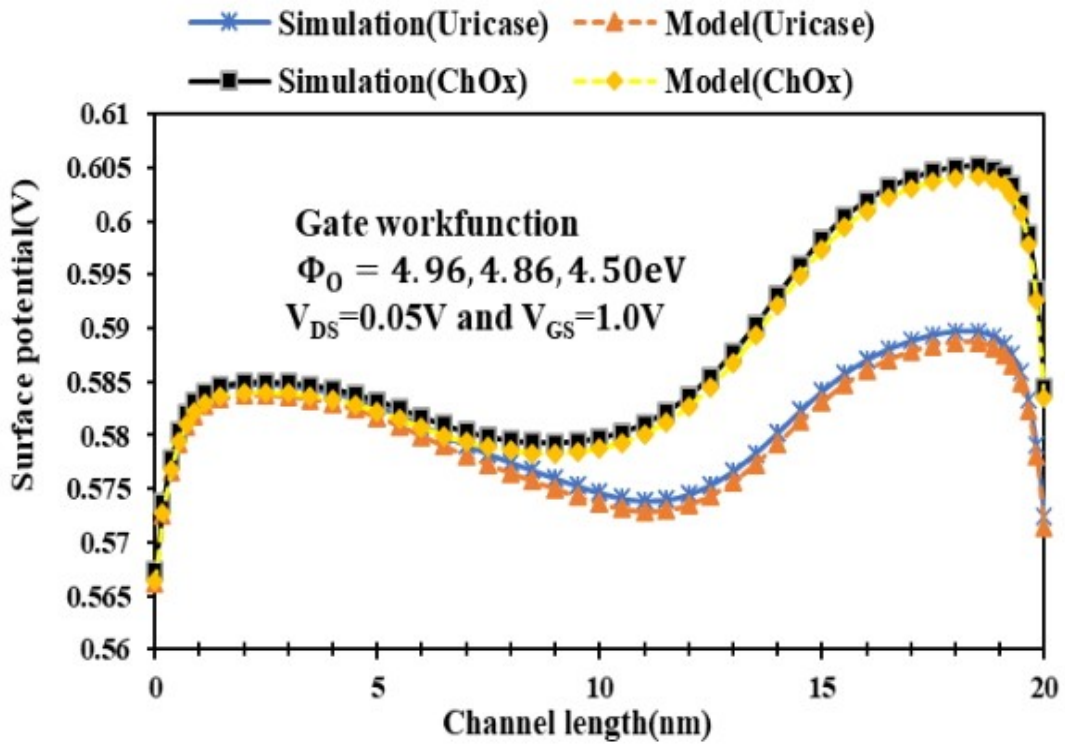

Figure 5. 2. Illustrates analytical and simulating results of surface potential along the channel for n-type THM GAA-JL-SiNWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Figure 5. 3 depicts the effect of different biomolecule species on the THM GAA-JL-SiNWFET surface potential. Towards the drain end, a cavity of 10 nm is proposed. When different biomolecules are immobilized in the cavity region, the potential varies more. The relative shift in potential is essential for determining the biosensor's sensitivity [39], [53]. The presence of biomolecules causes a significant shift in the potential profile along the channel. The effective gate oxide capacitance rises as the cavity fills with various biomolecules ($\varepsilon_{bio} > 1$) leading to enhanced coupling between the gate and the charge carriers moving through the channel. High coupling between the gate and the channel [54] reduces the channel potential, and this coupling increases when ε_{bio} increases. This variation in channel potential due to different biomolecules is depicted in **Figure 5.3.** An immobilized biomolecule recognition element is typically located on the gate surface of a metal-oxide-semiconductor field-effect transistor (MOSFET), which serves as the biosensor.

Table 5. 4: Illustrates dielectric constants for different biomolecules[45].

Dielectric materials	**Uricase**	**Streptavidin**	**Biotin**	**ChO_x**
Dielectric constants (ε)	1.50	2.10	2.63	3.30

Uricase and ChO_X Two enzyme types can serve as recognition elements in the proposed device. Uricase can detect uric acid, a biomarker for metabolic disorders such as gout. ChO_X is capable of detecting glucose, a biomarker for diabetes. Overall, while uricase and ChO_X can be effective recognition elements in MOSFET biosensors, reliable and accurate detection of the target biomolecules requires careful optimization and validation of the biosensor design and operation. When an enzyme immobilizes in the cavity, it can alter the local charge density on the MOSFET's surface, thereby influencing the device's surface potential. Uricase, for instance, catalysis, is the transformation of uric acid into allantoin and hydrogen peroxide, which may release or consume electrons and cause surface potential. In a similar manner, ChO_X catalysis, the conversion of glucose to gluconic acid and hydrogen peroxide, which can also cause the surface potential, as shown in

Figure 5. 3. As a result, the enzyme concentration and activity, as well as the MOSFET's sensitivity to variations in charge density, determine the magnitude of the impact on the device's surface potential.

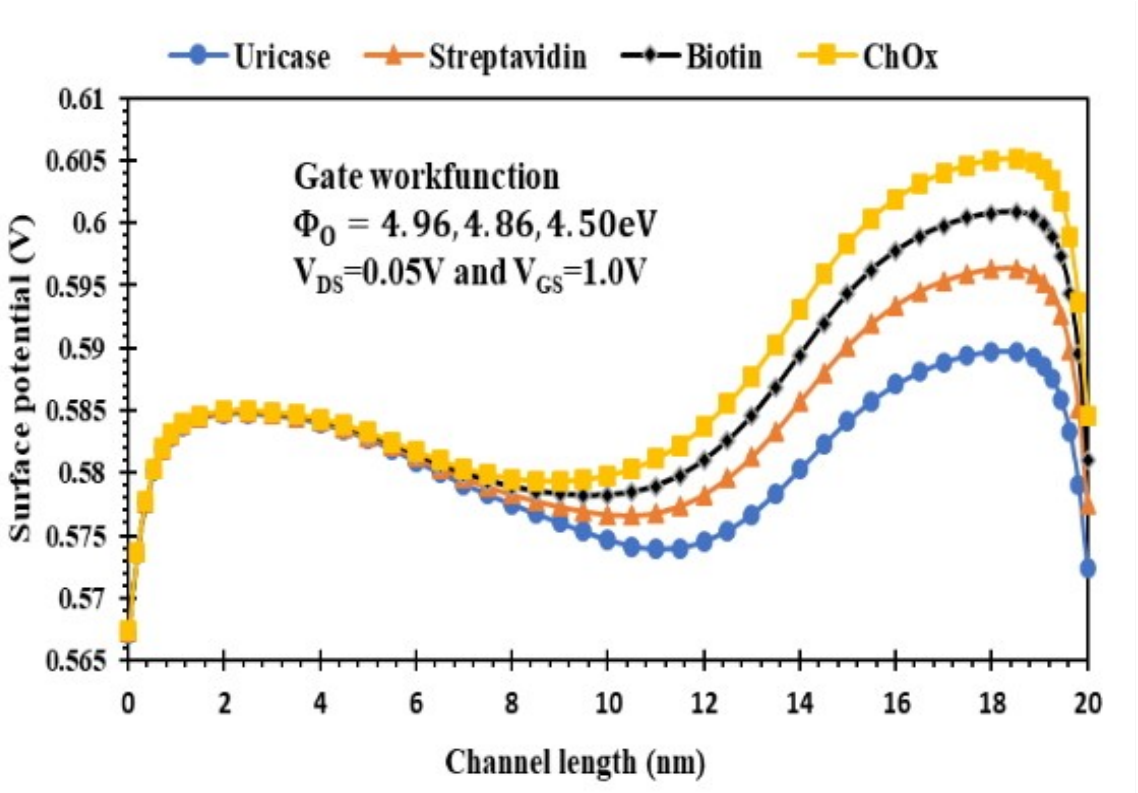

Figure 5. 3. Illustrates impact of different biomolecules on surface potential along the channel for n-type THM GAA-JL-SiNWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

5.3.2 Subthreshold Current Modelling

A surface potential solution is used to analyze the subthreshold current [56]. In constant electron quasi-Fermi potential $\phi_i(z)$, carrier mobility from source to drain in the z-direction is determined using current density $J_i(z)$;

$$J_i(r,z) = -q\mu_n n(r,z)\frac{d\phi_n(z)}{dz} \quad (5.42)$$

Here $n(r,z)$ is inherent carrier concentration and $\mu_n$is carrier mobility. Integrating the current density $J_i(r,z)$ along "z" in polar coordinates under complete depleted channel length gives drain current below threshold voltage [57].

$$I_{Sub} = q\mu_n d\phi_i(z) \times 2\pi \int_0^R rn_i exp\left\{q\left[\phi(r,z) - \phi_i(z)\right]\right\} / KTdr \quad (5.43)$$

Where "T" is thermal temperature, and "K" is Boltzmann's constant. From $z = 0$ to $z = L$, I_{sub} expressed as;

$$I_{Sub} = KT\mu_n\left(n_i^2 / N_a\right)\left\{1 - e^{\left(\frac{-q}{KT}V_{DS}\right)}\right\} / \int_0^L \left(1/2\pi \int_0^R re^{\frac{q\phi(r,z)}{KT}}dr\right)dz \quad (5.44)$$

Where $\mu_n$is silicon's constant mobility model ($\mu_n = 1417 cm^2/V.S$).

5.3.3 Threshold voltage (V_{th}) Modeling

The lowest (V_{GS})wanted to establish a conducting path between the source and drain terminals in a MOSFET device is known as the threshold voltage (V_{th})[58]. The threshold voltage for non-zero substrate bias voltage(V_{GS}) is written as;

$$V_{th} = \Phi_{MS} - 2\phi_F - 2\frac{Q_{BO}}{C_{OX}} - \frac{Q_B}{C_{OX}} \quad (5.45)$$

$$Where\ Q_{BO} = -\sqrt{2qN_D\varepsilon_{si}\left|2\phi_F\right|}, Q_B = -\sqrt{2qN_D\varepsilon_{si}\left|-2\phi_F + V_{GS}\right|}$$

C_{OX} is gate to oxide capacitance and Q_{OX} is gate to oxide charge density due to lattice imperfection at the interface.

5.4 Results and Discussion

5.4.1 Transfer characteristics

The work was verified and confirmed by applying the same models to THMGAA JL SiNWFET that were used to execute the device simulations for Surrounding Gate Junctionless MOSFET [55]. It is crucial to thoroughly test and verify its accuracy and reliability before applying the simulation model to a new device. The models required to make the simulations are meaningful since the simulated data are very close to the simulated results [55]. Device on-current/off-current are affected by increased dielectric constant biomolecule with different metal gate work-functions, as shown in **Figure 5. 4**.

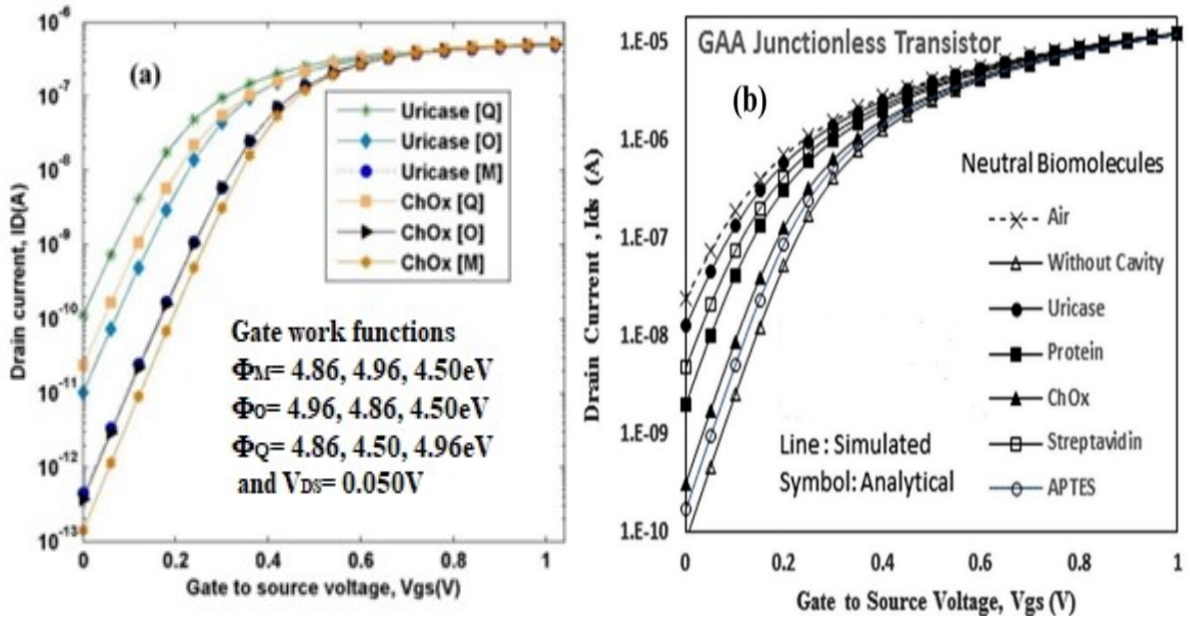

Figure 5. 4. Effect of different gate electrode work-function and dielectric materials on I_D-V_G and **(a)** proposed device and **(b)** referenced work [55] biosensor devices, ($V_{DS} = 0.05V$).

5.4.2 Impact of work-function (Φ_M) on the sensitivity (S)

A critical technological challenge for the triple gate MOSFET device is to find gate electrodes with appropriate tuneable electrode work functions designed for the desired (V_{th})/threshold voltages[57]. Threshold voltages for n-channel devices in a CMOS circuit can be optimized by adjusting the work function difference between the gate electrode and the intrinsic silicon film[59]. **Figure 5. 5(a)** illustrates the variation of threshold voltage when gate electrode work function increases from source to drain (denoted by "O", leading to the lower tunnelling path, thereby raising the tunnelling probability and reducing the ambipolar conduction (both positive and negative ions can move in the opposite direction)[56]. Replacing a higher dielectric constant in the nanogap cavity increases threshold voltage, as **Figure 5. 5(a)** describes**.** The shift threshold voltage (V) is illustrated in **Figure 5. 5(b),** which signifies the sensitivity of proposed devices with a tuneable work function labelled "O," which leads to improved device performance. Calculation of shifting the threshold voltage (ΔV_{th}) is described by **(eq. 5.46)** [40].

$$\Delta V_{th} = V_{th(Bio)} - V_{th(Air)} \tag{5. 46}$$

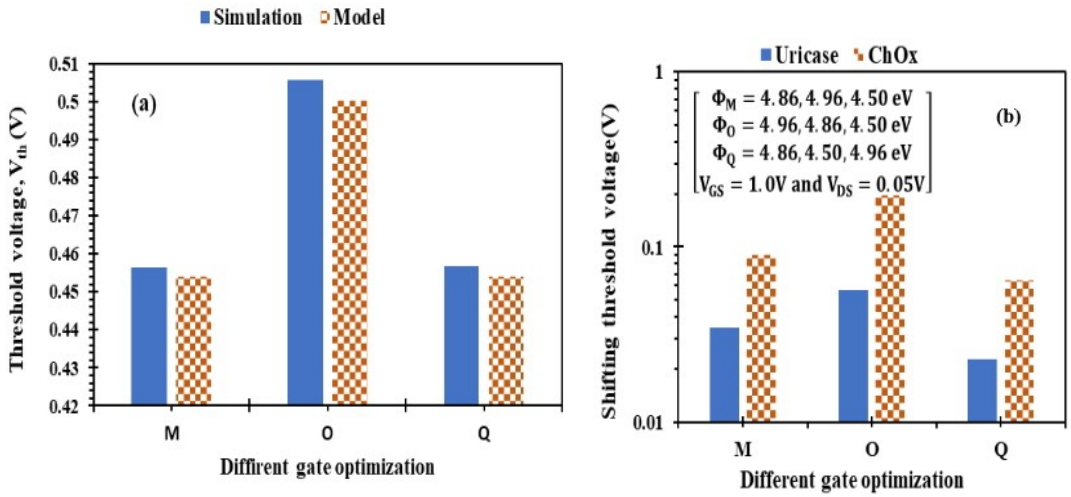

Figure 5. 5. Effect of different gate engineering on **(a)** threshold voltage and **(b)** shifting threshold voltage for n-type THM GAA-JL-SiNWFET, ($V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Figure 5. 6(a) depicts the effect of various gate electrode work-functions on device sensitivity$(S_{I_{OFF}})$ in the presence of biomolecules. It signifies that as a biomolecule dielectric constant increases, $S_{I_{OFF}}$ increased at optimized gate work-function tunned at "O" compared with" M, and "Q." For instance, percentage change /improvement of current sensitivity ($S_{I_{OFF}}$) due to different gate work functions are 16.21% when "O" compared with "M" and 30.96% compared to "Q" at ChO_X dielectric material when $V_{DS} = 0.05V$ & $V_{GS} = 1.0V$. We examine that ChO_X dielectric material and gate work function sited by "O" improve current sensitivity compared to uricase dielectric material. Current sensitivity of the proposed device for uricase and ChO_X dielectric material, including different gate work-functions, is obtained using **(eq. 5.47)** [55].

$$S_{I_{OFF}} = \left.\frac{I_{OFF}(\text{with biomolecule})}{I_{OFF}(\text{without biomolecule})}\right|_{V_{GS}=0V} \tag{5. 47}$$

Not only sensitivity ($S_{I_{OFF}}$) of our device is improved over the referenced works, also switching ratio, surface potential, short channel effects (SCEs), and leakage /tunnelling currents are more enhanced compared to the referenced[7] shown in **Figure 5. 6(b),** this is due to new technologies incorporated in our device modelling, such as device dimension, device structure, high-k gate oxide material (HfO_2), and optimized gate electrode work functions.

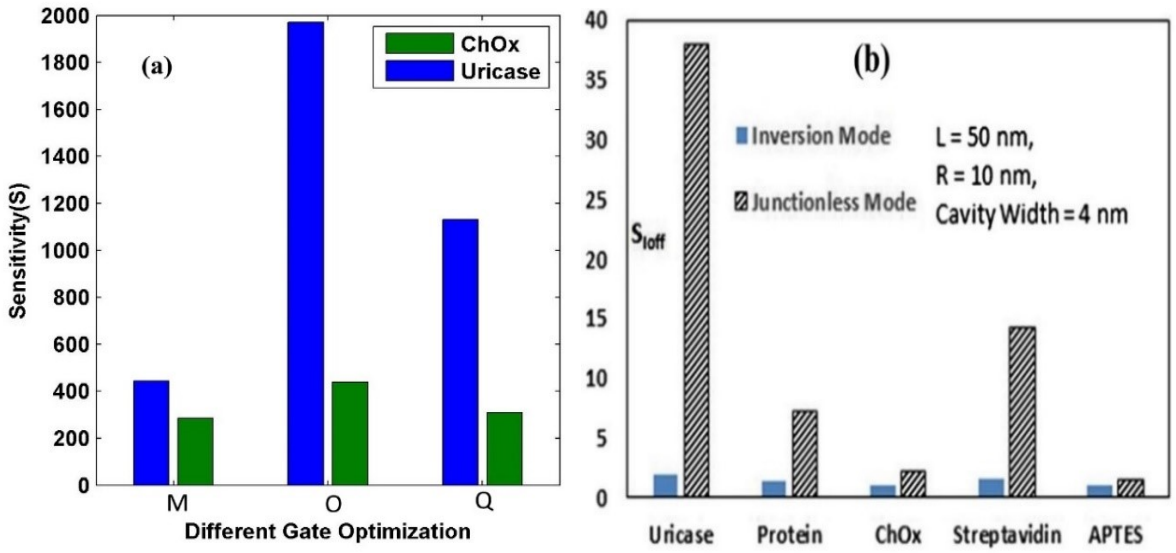

Figure 5. 6. Sensitivity parameter ($S_{I_{OFF}}$) for **(a)** for THM GAA-JL-SiNWFET device and **(b)** existing work[55], $V_{GS} = 1.0V$ and $V_{DS} = 0.05V$).

Figure 5. 7. Illustrates the switching ratio for the proposed device's different gate electrode work functions and leakage currents. Increasing the on-off current ratio indicates overall improvement in drive current with a low leakage current in low stand power (LSTP) logic technology, even though the on-current decreased with a rise in gate electrode work function.[60]. The highest switching ratio is achieved at "O" compared with M and Q gate tunable work function, in addition to improved device performance at "O," as illustrated in **Figure 5. 7(a).** The value of leakage current indicated by M and Q is higher than that of "O." This indicates that the gate electrode work function sited by "O" suppresses tunnelling current at weak inversion region enhance on current, as shown in **Figure 5. 7(b).** For instance, the percentage variation of leakage current in all cases is 80.97% decreases when tunable gate work-function marked by "O" compared with "M" and 83.64% reduces when "O" is compared with "Q" in the presence of ChO_X dielectric material in the nanogap cavity region. In the case of uricase dielectric material, the percentage variation is expressed as 59.90% decrease as a result of tunable gate work-function "O" is compared with "M" and 67.20% decrease when "O" is compared with that of "Q" at a constant drain to source current $V_{DS} = 0.05V$ and $V_{GS} = 1.0V$). From this, it is possible to elucidate that higher dielectric materials with tunable gate electrode work function signify CMOS devices' performance at ultra-small scale device dimensions.

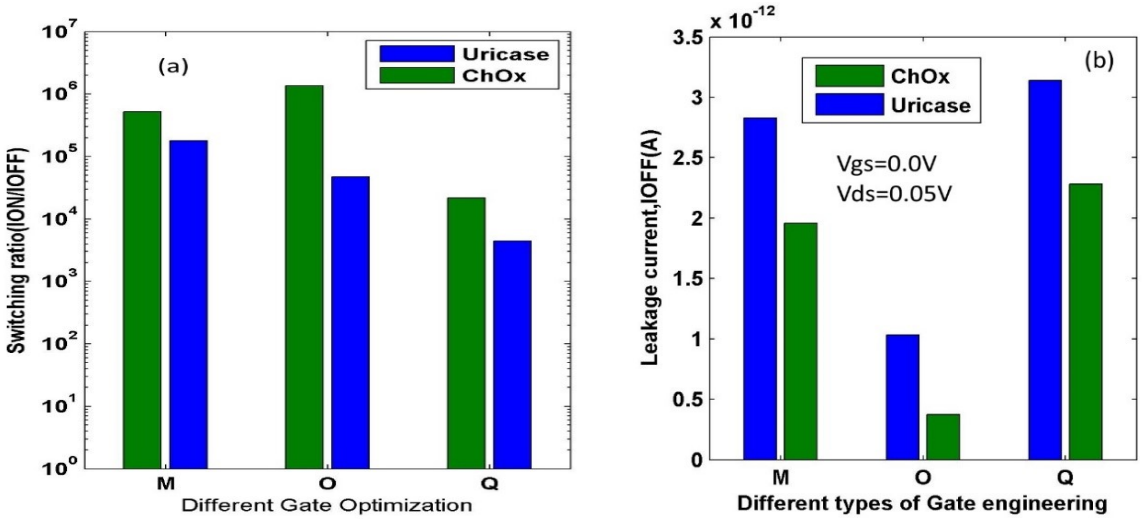

Figure 5. 7. Impact of different gate engineering on **(a)** switching ratio and **(b)** leakage current in the case of uricase and ChO_X biomolecules for n-type THM GAA-JL-NWFET, ($V_{DS} = 0.05V$ and $V_{GS} = 1.0V$).

Figure 5. 8. Shows a lower sub-threshold slope when the gate has a tunable electrode work function sited "O" while at 'M" and "Q" sub-threshold slope slightly increases due to the short channel effect at ultra-small channel length and hot carriers. While threshold voltage and drain mobility increase when the gate work function increases from source to drain through the channel designed at "O."

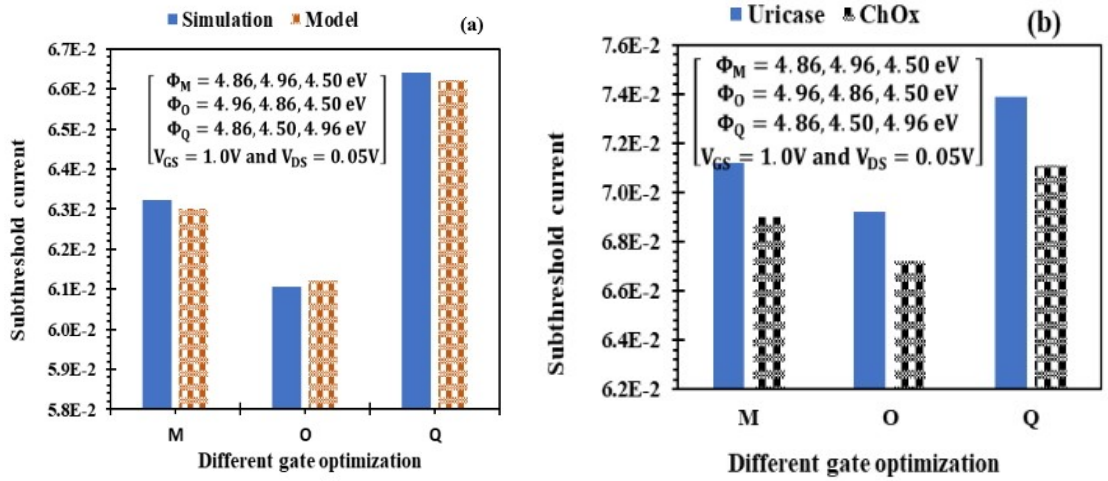

Figure 5. 8. Effect of different gate engineering on **(a)** analytical and simulation result of subthreshold current and **(b)** variation of subthreshold current in the case of uricase and ChO_X biomolecules for n-type THM GAA-JL-NWFET, ($V_{DS} = 0.05V$ and $V_{GS} = 1.0V$).

Figure 5. 9) illustrates how cavity length impacts device transfer properties with various biomolecules. Simulated results were obtained utilizing cavity lengths of 5 nm, 10 nm, and 15 nm while maintaining gate length, doping profile, and nanogap cavity thickness, keeping constant at constant room temperature. **Figure 5. 9(a)** shows how different biomolecules affect the switching ratio at various cavity lengths. Higher switching ratio variation is examined when

nanogap cavity length decreases due to lower parasitic capacitances and higher carrier mobility, thereby lowering leakage current. It's also interesting to note that the nanoscale size gap significantly affects the electrical characteristics of FETs. As a result, a significant change in switching ratio (due to the dielectric constant and cavity length variation) is used as a detection/sensing metric for a specific biomolecule. Moreover, one of the critical parameters for the designed biosensor device is sensitivity. As the nanogap cavity length increases, leakage current/tunnelling current increases, as reflected in **Figure 5. 9 (b),** due to lower dielectric constant [61].

Overall, we conclude that the cavity gap length must be optimized for better performance, allowing sub-20-nm THM-high-K-GAA-JL-NWFETs to be used as high-speed, low-noise, and high-sensitivity biosensors for the detection of a variety of diseases.

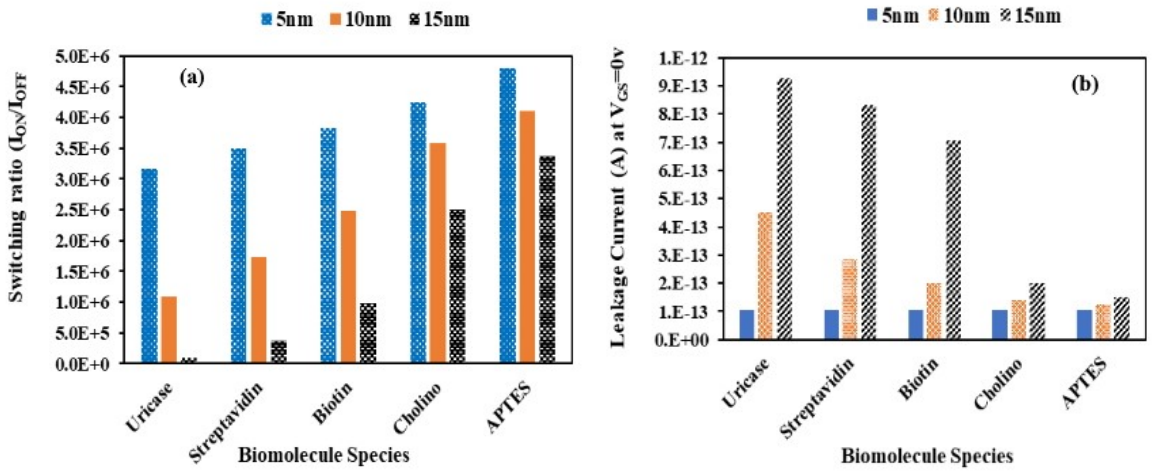

Figure 5. 9. Directs the impact of nanogap cavity length variation on **(a)** switching ratio and **(b)** leakage current in the case of different biomolecules in n-type THM GAA-JL-NWFET, ($V_{DS} = 0.05V$ and $V_{GS} = 1.0V$).

5.4.3 Transconductance (g_m) and output conductance (g_d)

The parameters transconductance (g_m) and output conductance (g_d) have significance in characterizing Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices. Transconductance (g_m) measures drain current variation with a gate-source voltage (V_{GS}), keeping the drain-source voltage (V_{DS}) constant to describe device load drivability [5], [7], [62]. The switching speed of a circuit and voltage gain of MOSFET amplifiers are also characterized by transconductance. Since linearity and distortion are crucial issues in designing several circuits[12]. The highest transconductance describes the circuit's capability for high-speed operation[63]. The nonlinearity of the device can be analyzed by determining the higher-order derivatives of $I_{DS} - V_{GS}$ at a constant drain-source voltage, and it designates harmonic distortion. Better linearity and lower distortion are examined under higher-order transconductance with lower amplitude [64]. The immobilized dielectric constant in the nanogap cavity affects device operation/linearity, as shown in **Figure 5. 10**. Device transconductance (g_m) in terms of drain current, and the gate-source bias voltage is given by **(e.q. 5.48)**[62].

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=0.6V} = \sqrt{\mu_n C_{OX}\left(\frac{W}{L}\right) I_D} = \frac{2I_D}{V_{GS} - V_{th}} \quad (5.48)$$

In the case of the gate-to-source voltage, transconductance variation, including different gate electrode work functions, is illustrated in **Figure 5. 10(a).** It clearly shows that higher transconductance is obtained as the gate work function increases from drain to source through the channel (labelled tunable work function at "O"), as shown in **Figure 5. 10(b).** This occurs because the gate material with the highest work function near the source end acts as the "control gate," while the gate material with the lowest work function near the drain end acts as the "screening gate," protecting the channel region under the first gate from the effects of a changing drain bias [65]–[67]. For instance, the percentage changes of transconductance labelled by "O" is 4.49% compared to "M" and 52.77% compared to "Q" using (uricase,$\varepsilon = 1.50$) dielectric material and 5.88% compared to "M" and 52.94% compared to "Q" using ($ChO_X, \varepsilon = 3.30$) dielectric material, labelled at "O." This examines that a critical gate engineering with tunable gate electrode work function should be applied when CMOS device modelling in ultra-small-scale dimension.

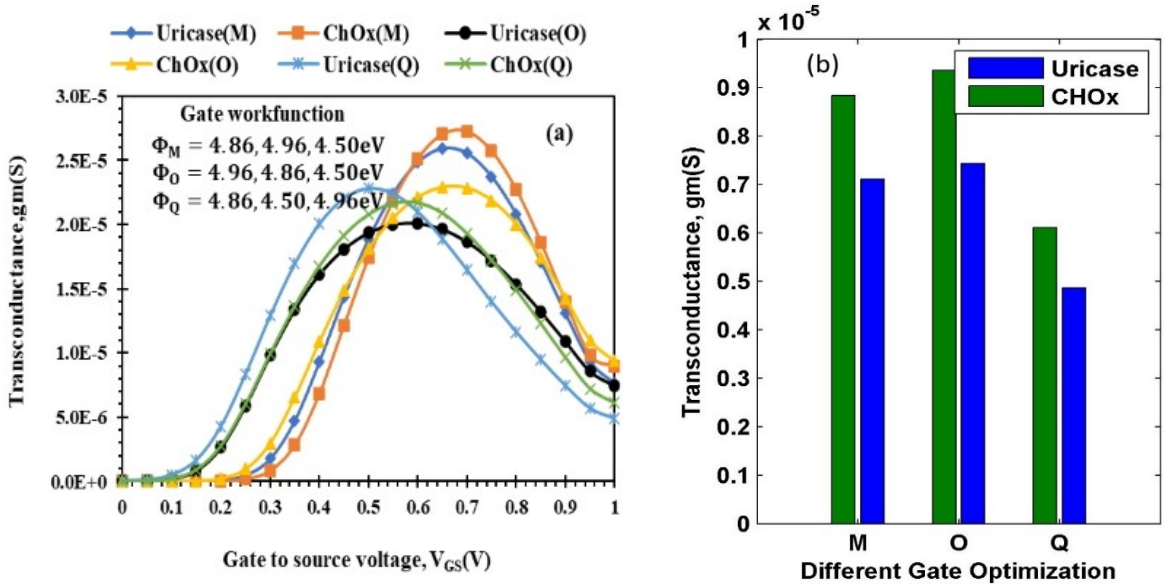

Figure 5. 10. Effect of different gate engineering on transconductance **(a)** with gate voltage and **(b)** at ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$) in the case of including uricase and ChO_X biomolecules for n-type THM GAA-JL-NWFET.

Another critical parameter to indicate CMOS linearity is device output conductance, defined with different drain currents in varying drain voltage at constant gate voltage[62]. **Figure 5. 11**) illustrates the proposed device output conductance with different gate work functions noted by "M, O, and Q," including uricase and ChO_X dielectric materials itching on the nanogap cavity. Ander lower inversion region, higher output conductance is experienced, while as bias voltage increases, the output conductance decreases and comes to cloth each other, as illustrated by **Figure 5. 11(a)**. The output conductance (g_d) in terms of drain current, and a drain-source bias voltage is given by **(e.q.5.49)**[62].

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=0.6V} = \mu C_{OX}\frac{W}{L}\left(V_{GS} - V_{th} - V_{DS}\right) \quad (5.\ 49)$$

The decreasing percentage change of output conductance labelled at "O" is 36.42% and 43.65% compared to labelled work functions of "M" and "Q," respectively, at ChO_X a dielectric material, while at uricase, dielectric materials are 30.68% and 40.92%. This signified gate engineering work function and coated dielectric materials of nanocavity affect the CMOS device performance.

In summary, the transconductance (g_m) and output conductance (g_d) characteristics are crucial in MOSFET characterization. A high g_m value indicates excellent sensitivity and rapid switching, but a low g_d value indicates strong output resistance and gain. As a result, optimizing these parameters is critical in designing and optimizing MOSFET devices for various applications.

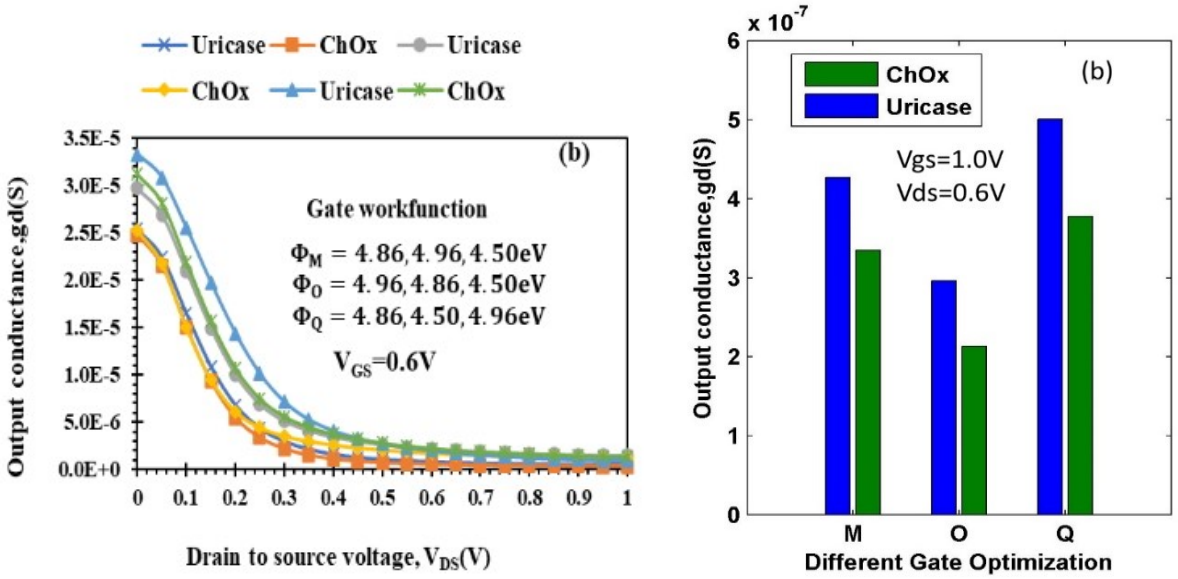

Figure 5. 11. Effect of different gate engineering on **(a)** Drain conductance as a function of gate voltage and **(b)** at ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$) for n-type THM GAA-JL-NWFET.

The intrinsic voltage gain (g_{m/g_d} or $g_m R_O$) of the transistor signifies the maximum voltage gain provided by a single transistor, playing a vital role in high-gain amplifiers. **Figure 5. 12(a)** illustrates the variation of inherent voltage gain with different gate work-function, including dielectric gate material in the nanogap cavity noted by M, O, and Q. It is observed that at dielectric material, ($ChO_X, \epsilon = 3.3$) tunable work function labelled by "O" is much higher compared to that of "M and Q." The degradation of the output resistance under work function marked by "M and Q" of scaled CMOS technology is moderately caused by the DIBL effect[68]. As illustrated in **Figure 5. 12(b),** the intrinsic voltage gain is high at "O" work function compared to "M and Q" at $V_{DS} = 0.6V$ and $V_{GS} = 1.0V$. The percentage change or improvement of inherent voltage gain, labelled by "O," is 31.58% compared to that of "M" and 187.61% compared to that of "Q" at ChO_X dielectric material. In the same manner, at uricase dielectric material, transconductance labelled by "O" is 25.93% compared to "M" and 94.29% compared to "Q." This signifies gate engineering work-function with the nanogap cavity

dielectric materials affects the intrinsic voltage gain and CMOS device performance. Mathematical expression of $\frac{g_m}{g_d}$ **or** $g_m R_O$ written as[68].

$$Intrinsic\ voltage\ gain(G) = \frac{g_m}{g_d} = g_m R_o \tag{5. 50}$$

Where R_o is the output resistance given by $\frac{1}{g_d}$ [69].

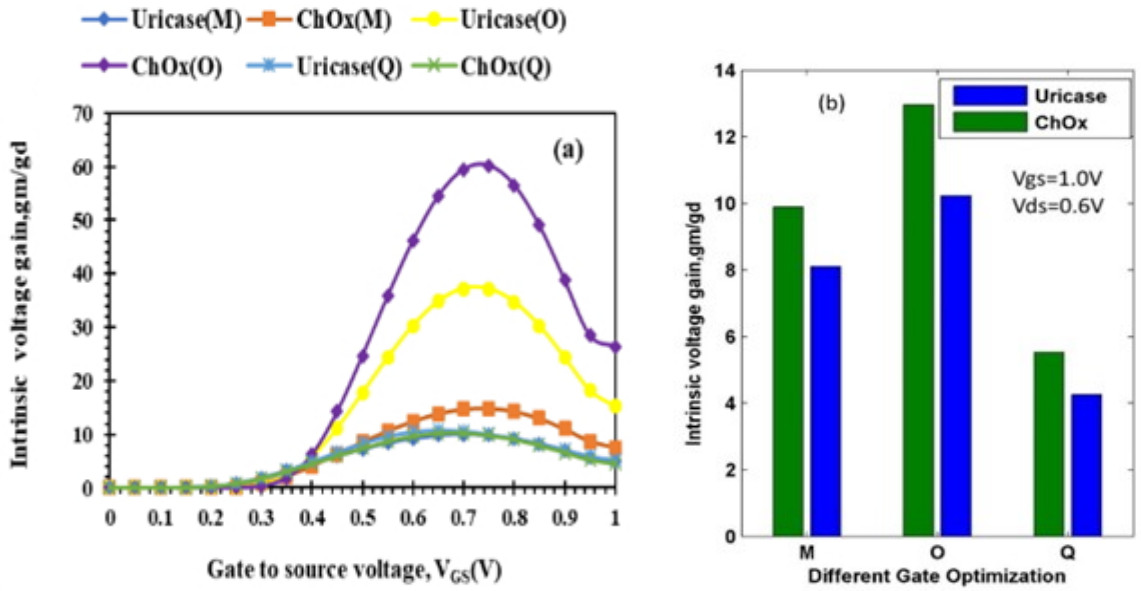

Figure 5. 12. Effect of different gate engineering on **(a)** intrinsic voltage gain vs gate voltage and **(b)** at ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$) for n-type THM GAA-JL-NWFET.

As a result, while designing and optimizing MOSFET devices for high intrinsic voltage gain, the electrode material and designed structure should be carefully examined. While ensuring robustness and manufacturability, the electrical characteristics of the electrodes should be optimized to maximize transconductance and minimize parasitic capacitances and resistances.

Figure 5. 13(a) illustrates the effect of gate engineering labelled "M, O, and Q" on the output resistance. It is observed that tunnelable work function marked by "O" has the highest output resistance than "M and Q." The gate engineering design at "O" experienced a less short channel effect due to increasing work function from source to drain, providing more mobility across the channel. **Figure 5. 13(b)** clearly describes the effects of coated dielectric material on the output resistance. The percentage change of output resistance labelled by "O" is 75.71% compared to "M" and 203.70% compared to "Q" at ChO_X a dielectric material. For uricase dielectric material, increment of output resistance labelled by "O" is 75.93% compared to "M" and 167.97% compared to "Q." This signifies gate engineering work function, including nanogap cavity dielectric material, affects the CMOS device performance.

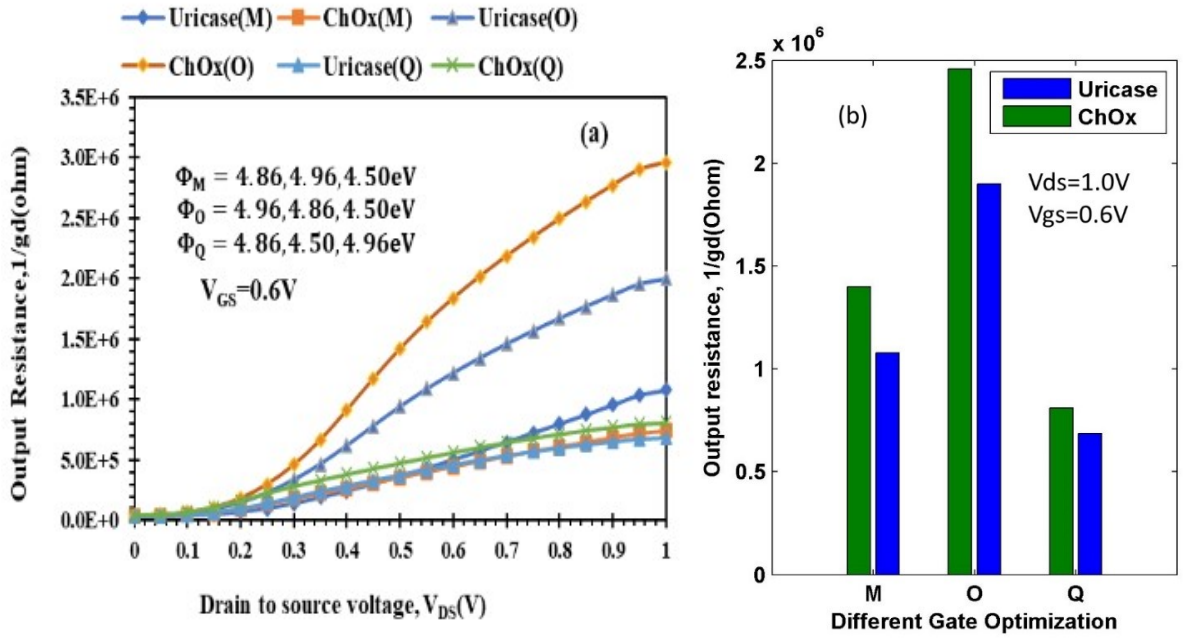

Figure 5. 13. Impact of different gate engineering on **(a)** output resistance vs gate voltage and (**b)** at ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$) for n-type THM GAA-JL-NWFET.

Figure 5. 14(a) illustrates the transconductance ratio over drain current (g_m/I_D) including different gate electrode work-function labelled by "M, O, and Q," undercoated cavity with uricase and ChO_X dielectric material signifies maximum value in weak inversion (WI) and decreases the value in strong inversion region. **Figure 5. 14(b)** clearly describes the impact of uricase and ChO_X dielectric material when $V_{DS} = 0.6V$ and $V_{GS} = 1.0V$ over device efficiency. Percentage increment of device efficiency (g_m/I_D) designated at "O" is 18.01% compared to "M" and 56.38% compared to "Q" at ChO_X dielectric material and for Uricase dielectric material, the increment of device efficiency labelled by "O" is 19.92% compared to "M" and 56.5% compared to "Q." This improvement is due to potential barrier reduction in the channel due to higher electrode work-function act as "control Gate" and dielectric material near the drain side improves the gate, resulting in speed-to-power dissipation performance[12]. This signifies gate engineering work function and dielectric materials in the nanogap affect CMOS device performance. In addition to metal electrodes, gate capacitance is an important parameter in MOSFET devices, and it can be influenced by the material used for the gate electrode. Increasing the gate capacitance using high-k dielectric materials can enhance the device's performance.

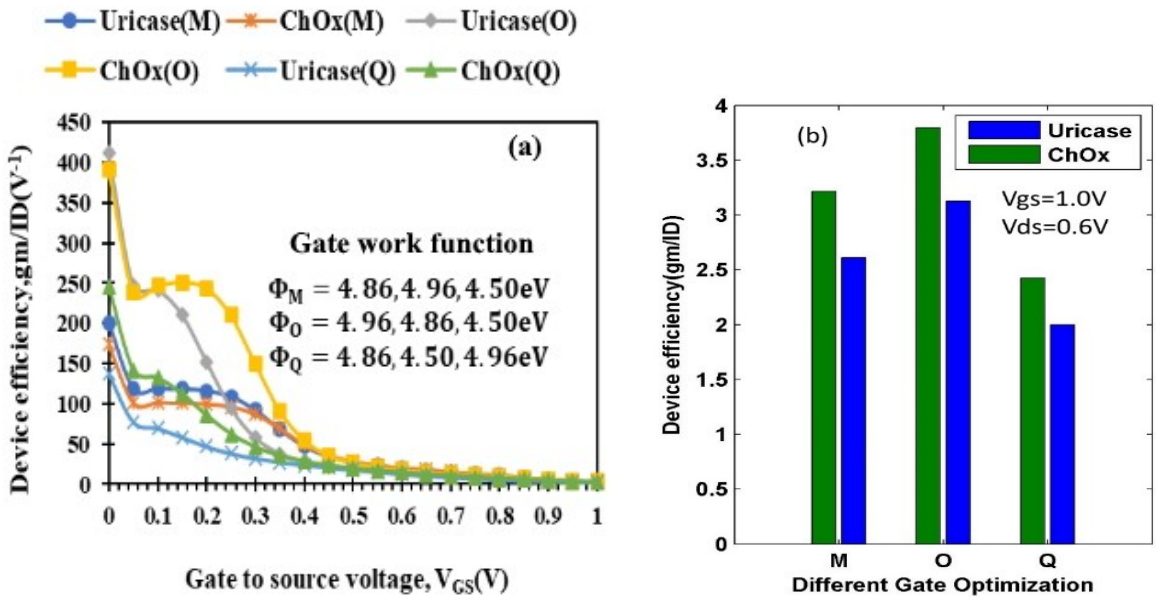

Figure 5. 14. Effect of different gate engineering on **(a)** device efficiency vs gate voltage and **(b)** at ($V_{DS} = 0.6V$ and $V_{GS} = 1.0V$) for n-type THM GAA-JL-NWFET.

Table 5. 5: Summarizes a comparison between the performance indicators for the two dielectric materials (uricase and ChO_X) for n-type THM GAA-JL-NWFET at a constant gate-to-source voltage ($V_{GS} = 1.0V$).

Gate work-function variables (eV)	Intrinsic voltage gain(V^{-1})		Switching (I_{ON}/I_{OFF}) ratio		Output resistance($1/g_d$)		Device efficiency		Transconductance, g_m(S)	
	Uricase	ChO_X	Uricase	ChO_X	Uricase	ChO_X	Uricase	ChO_X	Uricase	ChO_X
M	8.10	9.88	$1.78x10^5$	$5.22x10^5$	$1.08x10^6$	$1.40x10^6$	2.61	3.22	$7.12x10^{-6}$	$8.84x10^{-6}$
O	10.20	13.00	$4.75x10^5$	$1.36x10^6$	$1.90x10^6$	2.46x6	3.13	3.80	$7.44x10^{-6}$	$9.36x10^{-6}$
Q	4.25	5.22	$4.40x10^3$	$2.18x10^4$	$6.85x10^5$	$8.10x10^5$	2.00	2.43	$4.83x10^{-6}$	$6.12x10^{-6}$

In conclusion, MOSFET device performance can be significantly improved by carefully selecting the electrode material. When designing and optimizing MOSFET devices, it is important to take into account how the use of different electrode materials may affect the device's electrical properties, reliability, and manufacturability to achieve the necessary performance characteristics.

5.5 Summary

Based on a 2D solution of Poisson's equation, a new numerical model for triple hybrid metal gate dielectric modulated gate-all-around junctionless nanowire FET-based uricase and ChO_X biosensor was successfully developed to investigate the effects of gate electrode work function during gate engineering/optimization. The theoretical modelling and simulation results are in good agreement and accurately predict the device's behavior. The analytical modelling contains an electrostatic potential, threshold voltage, subthreshold current, and electric field, including neutral biomolecules (uricase and ChO_X) and different metal work-function. The effect of gate electrode work function and dielectric materials on device sensitivity, linearity (transconductance, intrinsic voltage gain, output conductance), switching ratio, leakage current, subthreshold voltage, device efficiency, and shifting threshold voltage of the proposed device has been studied. The simulated results reveal that the voltage and current sensitivity increase when the tunable gate work function increases from source to drain across the channel. For instance, sensitivity improvement (S_{Cur}) is 16.21% when "O" compared with "M" and 30.96% compared to "Q" when ChO_X, a dielectric material, is immobilized on the cavity at designed gate engineering denoted by "O." This improvement of current and voltage sensitivities makes the THM-GAA-JL-NWFET-based ChO_X biosensor designed at "O" clearly indicates better output results compared to "M" and "Q" in terms of sensitivity, switching ratio, and device efficiency, as summarized in **Table 5. 5.** In addition to the metal work function, higher dielectric constant of biomolecules and properly optimized nanogap cavity length signifies improved output results in transconductance, surface potential, switching ratio, and intrinsic voltage gain; so that THM-GAA-JL-NMOSFET based ChO_X biosensor designed at "O" responsible for better detection/sensing different concentration levels of cholesterol. Since cholesterol oxidase (ChO_X) is an enzyme that catalyzes the oxidation of cholesterol to cholestenone by reducing the oxygen molecule to H_2O_2 (hydrogen peroxide). In addition to clinical applications, cholesterol oxidase has broader industrial potential. For example, cholesterol oxidase is used for steroid (lipid/fat) analysis in food samples and is also employed as a biosensor to quantify serum cholesterol concentrations, which is important for cardiovascular disease diagnosis and other lipid abnormalities.

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CHAPTER -6

Summary and future scope of the work

6.1 Summary

Chapter-1: Devices with low power consumption and outstanding performance are in high demand in modern microelectronics. The never-ending quest for devices that can perform at higher speeds leads to a continuous reduction in device size. The transistors are evolving from single-gate to multi-gate structures to decrease power consumption, improve performance, increase packing density, and reduce device dimension. However, as the MOSFET gate length is scaled down to 15-20 nm, leakage current and short channel effects drastically increase. A brief introduction, along with transistor evolution, has been discussed in this chapter. Various MOS scaling challenges, like drain-induced barrier lowering, velocity saturation, hot carrier effect, channel length modulation, punch-through, and leakage current, have been reviewed and discussed in Chapter One. In this chapter, some of the engineering techniques developed to improve the electrical efficiency of conventional devices have been reviewed and discussed, along with a brief review of MOS scaling and challenges. For instance, gate dielectric engineering, gate electrode engineering, and junctionless transistors (gated register) are some of the engineering schemes that have been discussed in Chapter One for improving device performance under ultra-scall device design. Finally, the latest device structure with new principles for continuous scaling of semiconductor device size for enhancing the device's performance and operation speed has been discussed in this chapter.

Chapter-2: The detection of various gases has applications in various industries, including the medical business, agriculture, and environmental studies. For instance, Hydrogen is an odourless, colourless, and highly combustible gas utilized as a medium for energy storage and used to generate power fuel cells. Due to the need for reliable and cost-effective gas detection systems, such as fueling stations, healthcare, industry, and environment monitoring, to mitigate the risk of gas leaks. This chapter discusses a computationally efficient two-dimensional analytical model for JL-GAA SiNWFET with cylindrical geometry incorporated to detect hydrogen gas. As a result of its surrounding gate structure and larger surface-to-volume ratio, the JL-GAA SiNWFET with a catalytic palladium metal gate demonstrates superior sensitivity to the typical bulk MOSFET for detecting hydrogen gas molecules has been proposed. Electrical parameters like surface potential, threshold voltage, subthreshold current, electron concentration, and hole concentration (charge concentration) have been examined. The analytical results, also analyzed using 2D poisonous equation and boundary values, show good agreement with the simulated data, offering an excellent foundation for designing and optimizing biomolecule-containing JL-GAA SiNWFETs. Change in subthreshold current caused by a change in the work function of the gate metal as a result of gas molecule reactivity at the surface of the gate catalytic metal is utilized as the sensitivity parameter, which provides very high sensitivity when compared to threshold voltage change. When the work function of Palladium metal gate material is changed, hydrogen molecules adsorbed at the surface

dissociate into hydrogen atoms due to the weakening of the H-H bond. Some hydrogen atoms are also adsorbed at the metal/oxide interface, which changes the device's electrical characteristics. The device's sensitivity in the subthreshold range is also desirable since it offers a low-cost, low-power hydrogen gas sensor. Hydrogen gas sensitivity of JL-GAA-SiNWFET was compared with bulk MOSFET and GAA-MOSFET existing devices in terms of the subthreshold current sensitivity ($S_{I_{off}}$), and found that JL-GAA SiNWFET's hydrogen gas sensor device shows better sensitivity than bulk MOSFET and GAA-MOSFET. The sensitivity metric in this sensor is subthreshold current or off-state current. It has been demonstrated that JL GAA SiNWFET sensors have much higher sensitivity than conventional MOSFET sensors due to their high surface-to-volume ratio, low leakage current, nearly ideal subthreshold characteristics, and effective gate control. Thus, the JL GAA SiNWFET sensor with palladium catalytic metal gate is a promising hydrogen gas sensor due to its high sensitivity and ease of fabrication.

Chapter-3: In this chapter, a dielectric modulated triple hybrid metal gate-all-around junctionless nanowire transistor was presented for the first time and compared with single, double, and triple hybrid metal gate transistors for various disease sensing applications employing atlas-3D device simulation tool. In this chapter, single, double and triple hybrid metal gate dives electrical characteristics such as subthreshold slope, drain-off sensitivity $(S_{I_{OFF}})$, surface potential, switching ratio(I_{ON}/I_{OFF}), output conductance (g_m) output resistance $(1/g_m)$, and transconductance (g_m), have been studied in the presence of biomolecules in the nanogap cavity by extracting vast simulation results. The effect of different biomolecule dielectric and nanogap cavity lengths on device's performance has been examined. The result shows that including a high-k and customized gate for DM THMG-GAA-JL-FET-based biosensors significantly boosts carrier velocity and efficiency, eliminates DIBL, hot-carrier effect, and other SCEs reduces power dissipation. In this chapter, DM THMGAA-JL-NWFET-based biosensor has been investigated as a low power consumed, improved sensitivity, and a promising technology for detecting neutral biomolecules in providing efficient nano-scale and very sensitive biosensors to meet future demands.

Chapter-4: In this chapter, a complete study was carried out to analyze the impact of localized charges on sensitivity, linearity, and circuit performance on double and triple hybrid metal gate JL GAA NW FET compared with existing works, and it can be seen that there is a significant device performance degradation in the presence of positive localized charges which should be estimated in advance in order to use the device in various sensing applications. The model reproduces the variations in device characteristics, such as surface potential, threshold voltage, switching ratio, subthreshold swing, and drain current, as a function of device parameters and density, along with different localized charges. Just like charges at the Si-SiO_2 interface play a significant role in the study of device reliability and performance, localized charge also plays a vital role in examining MOSFET for sensing applications. So, this chapter is devoted to exploring the impact of trap charge/localized charge on double and triple metal gate junctionless GAA SiNWFET for biosensing applications. For instance, in both devices, changes in shifting threshold voltage, switching ratio, transconductance, output conductance, intrinsic voltage gain, device efficiency, leakage current, and subthreshold slope in the presence

of biotin and APTES biomolecule have been investigated along with a localized charge. For example, the results of SS at negative ITCs are $(62.6 \text{ and } 60.3)\text{mV/decade}$ for double and triple hybrid metal gate devices, respectively. Improved switching ratio (4.18×10^{6} and 4.12×10^{8}) and transconductance ($7.88 \times 10^{-6}\ and\ 1.90 \times 10^{-5}$) has been examined at negative ITC for double and triple THG-high-k-GAA-JL-NWFET, respectively, when APTEs biomolecule uniformly immobilized in the nanogap cavity.

Finally, this chapter concludes that the negative ITC enhances the output characteristics, such as switching ratio, transconductance, device efficiency, and intrinsic voltage gain (A_V) for triple metal gate compared to double hybrid metal gate-all-around junctionless silicon NWFET devices when biotin and APTES biomolecules uniformly immobilized in the nanogap cavity compared to positive trap/localized charge.

Chapter-5: This chapter examines an analytical model of a gate stack surrounding triple hybrid metal gate NWFET at different gate optimization to improve sensing application performance. Three different gate electrode engineering (optimization) designated "M, O, and Q" with three different work functions have been included in this study. Based on a 2D solution of Poisson's equation, a new numerical model for triple hybrid metal gate dielectric modulated gate-all-around junctionless nanowire FET-based uricase and ChO_X biosensor and vast simulation results were successfully developed to investigate the effects of gate electrode work function during gate engineering/optimization. The analytical model for surface potential, threshold voltage, subthreshold current, and electric field, including neutral biomolecules (uricase and ChO_X) at different gate electrode materials has been carried out in this chapter. The analytical model, which is based on the surface-potential approach and parabolic approximation, has shown remarkable agreement in comparison to the simulated results. Also, the effect of different gate electrodes designated "M, O, and Q" and dielectric materials on device electrical characteristics such as transconductance, intrinsic voltage gain, output conductance, switching ratio, leakage current, subthreshold voltage, device efficiency, and shifting threshold voltage of a gate stack surrounding triple hybrid metal gate NWFET have been studied. Also, the effect of nanogap cavity length on the electrical properties of THM-GAA-JL-NWFET-based biosensors was investigated in this chapter. Finally, the simulation findings reveal that the performance of the THM-GAA-JL-NWFET is enhanced when the source-to-drain tunable gate work function is increased across the channel (denoted by "O"); thus, THM-GAA-JL-NMOSFET based uricase and ChO_X biosensor designed at "O" is responsible for better detection/sensing.

6.2 Future scope

The main objective of this thesis was to elaborate on Gate Stack GAA JL-NWFET sensors for various sensing applications, i.e., biosensors and hydrogen gas sensors. Another objective of the present research work was to address issues related to interface trap charges present at the Si-SiO_2 interface of the GAA MOSFET and to study their impact on the device sensing performance. In addition to these objectives, impacts of gate electrode optimization on device performance were examined. All objectives are accomplished through analytical formulations and extensive simulations; however, certain aspects remain unrevealed.

1. The analytical model and simulations performed for the Gate Stack GAA Junctionless NWFET biosensor were applicable for a device where measurement was taken under a dry environment. The developed model will be modified for use in a watery/wet environment, and a comparison between the two devices will be taken in future work.
2. The presented work only emphasized on fixed localized charges. The impact of mobile charges on the performance of junctionless gate stack GAA NWFET sensor can be considered a future extended work.
3. The impact of localized charges on device sensitivity is only considered over the Gate Stack GAA JL NWFET biosensor. Another crucial issue is the effect of localized charges on the noise behavior of Gate Stack GAA JL NWFETs; thus, a noise model can be developed in the future to address this issue.
4. The present research work explored Gate Stack GAA JL NWFET hydrogen gas and biosensor sensing applications, but not yet for pH and pressure sensors. This will be future work.
5. In the future, an equivalent circuit model for Gate Stack GAA JL NWFETs with localized charges could be developed for use in circuit simulators.
6. The effect of localized charges on the reliability and performance of digital circuits such as SRAM cells and other analog circuits like op-amps can be investigated in future work.

Silicon
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ORIGINAL PAPER

Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor

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Abstract
In this work, a junctionless(JL) gate all around (GAA) silicon nanowire field-effect transistor sensor for the detection of hydrogen (H_2) has been carried out. The sensors are designed to specify hydrogen gas (H_2) existence. Unsafe conditions can result if hydrogen escapes and accumulates in an enclosed space throughout the purifying process; this is why we try to investigate technologically ultra-small-scale hydrogen gas sensor devices. The sensor also showed satisfactory characteristics for ensuring safety when handling hydrogen and remarkable selectivity for monitoring H_2, among other gases, such as LPG, NH_3, and CO. The temperature and palladium (Pd) gate work function variations in the translation processes are well-thought-out throughout a change in palladium (Pd) gate work function following exposure to the hydrogen gas molecule (H_2). Due to its sensitivity to H_2 gas, palladium (Pd) is employed as a gate electrode in H_2 gas detection. Shift in threshold voltage (V_{th}), Ion and Ioff as a result of the metal work function at the gate changing when gas is present; these changes can be regarded as sensitivity parameters for sensing hydrogen gas molecules. ATLAS-3D device simulator has been conducted at low drain bias voltage (0.05V). This study focuses on temperature variation (300K to 500K) and palladium (Pd) metal gate work function variations (5.20eV to 5.40eV) to examine the existence of hydrogen molecule(H_2) and its effect on the performance of junctionless SiNW-GAA field-effect transistor gas sensors. When the sensitivity $\left(S_{I_{OFF}}\right)$, of proposed JL-GAA-SiNWFETis compared with GAA-MOSFET and bulk MOSFET, JL-GAA-SiNWFET shows improved sensitivity. The results show that as 150mV Pd work function shifts at the gate, the sensitivity improvement with JL-GAA-SiNWFET-based hydrogen gas sensors are 51.65% and 124.51% compared with GAA-MOSFET and MOSFET, respectively. High dielectric oxide (HfO_2) and interface oxide (SiO_2) is also employed at the gate to overcome electron tunneling. The study of this work proves that a silicon nanowire field-effect transistor with a junctionless gate all around catalytic palladium (Pd) metal gate is the best candidate for sensing hydrogen gas molecules than a bulk metal oxide semiconductor field-effect transistor (MOSFET).

Keywords Hydrogen gas-sensor · Junctionless(JL) · Silicon nanowire FET · Gate-all-around (GAA)

1 Introduction

Hydrogen is recognized as one of the most significant clean energy carriers and the ultimate fossil fuel candidate and renewable energy source [1] because of its high heat of combustion, low minimum ignition energy, and high combustion velocity. Due to its robust reducing characteristics, hydrogen is also employed in metal smelting, petroleum extraction, semiconductor processing, glass-making, and the daily chemical industry, among other things [2]. It is owing to the growing demand for gas sensing sensors for seismic monitoring applications, environmental monitoring, medical and automotive industries, in addition to domestic usages, such as detecting pollutants, fueling stations, petroleum refineries, and detecting certain types of bacterial infection, which are continuously at high perilous of gas leakage[1–6]. Designing a hydrogen gas sensor based on a GAA-JL-SiNWFET device is an exciting option for gas sensors. It offers low power consumption, high sensitivity, low cost, portability,

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technology compatibility, on-chip integration, small size, and CMOS compatibility [7, 8]. Humans cannot smell hydrogen gas since it is colorless and tasteless [9, 10]. It is easily flammable and explosive due to its low explosion energy and extensive flammable range. As a result, an effective and reliable hydrogen sensing device is required for hydrogen manufacturing and consumption, monitoring and managing hydrogen concentrations in nuclear reactors and coal mines, and detecting and alarming H_2 leakage during storage, transportation, production and usage [1, 3, 6, 7]. As a result, such sensors seem to be among the most straightforward, inexpensive, and efficient tools for real-time measurement or gas leak detection [10]. Due to various reasons, different types of SiNWFET-based hydrogen gas detecting devices have been designed in recent years to identify gas molecules by analyzing the induced change in work function at the surface of an attractive film [6, 9]. Numerous types of gas detectors are available, but FET-based gas detectors have received much attention [11]. Device engineering is being used in this area of research and development, including modeling and evaluating the field-effect device to improve sensitivity [5]. Floating gate MOSFETs [12], SOI MOSFETs, dual-gate MOSFETs [13], and now nanowire MOSFETs [14] have all been considered in device engineering. A high surface area to volume ratio is necessary to boost sensitivity by raising the potential for surface interactions [8]. Gas sensors in this device depend on the interaction of a thin Pd layer with hydrogen gas [9, 15, 16]. A junctionless nanowire transistor is a gated resistor with the same doping type on the source, channel, and drain without junctions [17]. For example, leakages are always a hazard at gas stations and refineries, and early recognition is thoughtful to minimize dangers and accidents[1, 2]. A silicon nanowire Field Effect Transistor (SiNWFET sensors are an enticing proposition for gas sensing [9] due to technology compatibility) [18] for on-chip integration, portability, low power consumption, and the ability to detect both weakly bound strongly bonded and chemical bonding species at room temperature [19, 20]. The detecting mechanism is the interfacial adsorption of disassociated hydrogen molecules into the palladium gate results in the formation of a dipole layer, which alters the gate's work function and causes a significant shift in threshold voltage (ΔV_{th}) [3, 9, 19]. For example, different catalytic gate metals have been utilized to realize the hydrogen gas sensor, such as Palladium [15, 21], Platinum[1], [7], and poly-methylmethacrylate-platinum[8]. Semiconductors such as silicon nanowires (SiNWs) and thin films have been utilized as sensing materials for the development of high hydrogen gas sensors in recent years [1] [9] due to their huge specific surface area and unique electron transportation characteristics.

Numerous nanoelectronics devices with multiple gate materials, for instance, floating gate MOSFETs [20], Palladium (Pd) gate MOSFETs [22], and Tunnel-FET (TFET) [23], etc., have been designed to boost the sensitivity of SiNWFET based sensors [16]. The planer MOSFET is the most ideal among them because of its production ease, although it has a number of drawbacks in the ultra-small scall dimension, such as short channel effects (SCEs), Subthreshold Swing [24–26]. Under ambient conditions, a junctionless catalytic metal gate-all-around silicon nanowire FET [27–31] device is best for overcoming these issues and providing better performance in terms of sensitivity and response time. Because of a more active surface interaction of hydrogen gas molecules with palladium [19], nanostructure palladium gate materials have a high attraction for hydrogen gas and provide superior sensing capability [22, 32] than bulk palladium materials. Due to these and other physical significance, we employed Nanowire palladium materials as gate electrodes for our proposed device.

In this work, high-k materials for gate oxide, like hafnium oxide(HfO_2) and interface oxide (SiO_2), were chosen to develop new and high-performance electrical devices at the nanoscale that has relied heavily on gate dielectric materials [33–35]. Since hafnium oxide(HfO_2) provides the most excellent and powerful dielectric materials, enhancing the sensing performance compared to other simulated dielectric materials [33, 36] in controlling tunneling/leakage current. The significance of utilizing Pd metal gate as a catalyst to improve SiNW thin film H_2-sensing performance is the straightforward synthesis, which allows for precise control of the thicknesses of SiNW and Pd metal gate to produce detectors with the maximum possible sensitivity [37]. Because palladium electrode selectively absorbs hydrogen gas and produces palladium hydride, as it is employed in various industries [22].

Therefore, we have designed a p-type substrate junctionless gate-all-around SiNWFET-based sensor to investigate hydrogen gas using Atlas-3D-TCAD device simulator tool.

1.1 Device structure

The designed structure for our proposed device is illustrated in Fig. 1) here, L (20nm) is the length of dielectric material (HfO_2), channel, (SiO_2) is an interface oxide layer and T_1 T_2, and T_3 are the thickness of the metal Gate, hafnium oxide, and interface (SiO_2) oxides, respectively, and 2R is channel diameter (silicon film thickness), as shown in Table 1. The device gate length is 20nm for all simulations, and source and drain lengths are each 10nm, as shown in Table 1. To achieve a tolerable threshold voltage, a high doping concentration ($1x10^{19}cm^{-3}$) was applied uniformly through the channel

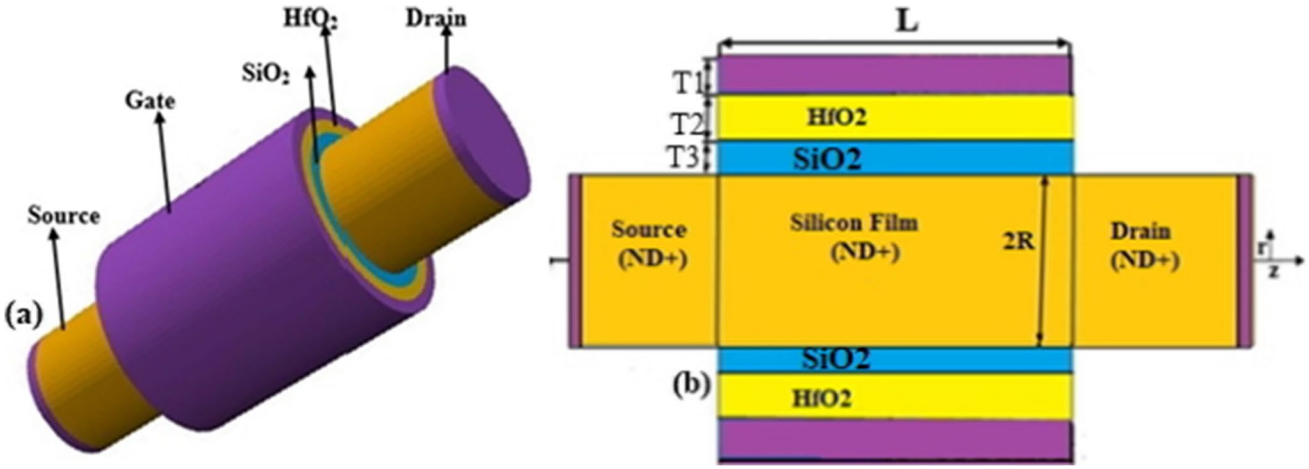

Fig. 1 illustrates **(a)** 3D representation diagram and **(b)** 2D cross-sectional view for p-type substrate cylindrical JL-GAA-SiNWFET-based hydrogen sensor

Table 1 Technology parameters

Device Parameters	GAA-JL-SiNWFET
Channel length (nm)	20.00
Thickness of oxide HfO_2 & SiO_2 respectively, (nm)	1.50 & 0.30
Interface Oxide (SiO_2) thickness, (nm)	1.00
Oxide (SiO_2) length, (nm)	20.00
Source and Drain length/thickness (nm)	10.00
Hafnium Oxide (HfO_2) length, (nm)	20.00
Radius of silicon film (nm)	10.00
Drain, Source & Channel Doping (N_D+)	$10^{19}cm^{-3}$
Oxide dielectric constant, HfO_2 & SiO_2	25.00 & 3.90
Reference gate work function (Palladium), (eV)	5.20

from the source to drain for our designed p-type substrate devices. The supply gate-source voltage (0.6V) with a consistent drain-source voltage (0.05V) have been employed for all simulations.

1.2 Simulation methodology

Silvaco TCAD-ATLAS tool is used for all simulations in this work. Concentration-dependent mobility, drift-diffusion, and field-dependent mobility models are activated to incorporate electron mobility models [38]. To account for the recombination of majority and minority charge carriers, the Shockley-Read-Hall (SRH) recombination model is also activated [39]. The drift-diffusion model also accounts for the driving current caused by the charge carrier following. Due to heavy source and drain doping, Fermi Dirac Statistics have been introduced. The Boltzmann transport statistics and concentration, voltage, and temperature(CVT) [39] Lombardi mobility model [16] have accounted for parallel and perpendicular field mobility [39]. Palladium(Pd) has a high affinity for hydrogen, making it an excellent material for detecting hydrogen storage (reversibly introduced) [10, 40, 41]; when interacting with the palladium surface, Van der Waals forces interact between hydrogen gas molecules and palladium atoms [22].

Figure 1 demonstrates (a) the three-dimensional structures and (b) the two-dimensional cross-sectional view of the p-type palladium metal gate Junctionless (JL) GAA SiNWFET-based hydrogen gas sensor. The GAA SiNWFET structure includes a 40 nm long p-type doped channel and applied $1x10^{19}$ cm^{-3} doping concentration from the source to drain through the channel uniformly. Palladium metals were applied as the gate material because hydrogen molecules at the palladium surface breakdown when H_2 gas is exposed to a palladium metal gate, which causes dissociated molecules to diffuse into the gate [10, 22].

In this study, we have considered the catalytic metal gate method to describe the behavior of JL-GAA-SiNWFET based hydrogen gas sensor. The Pd work function must be a critical factor in altering the electrical field properties of the device as it changes [40]. The H_2 gas molecules break down at the metal surface of the metal gate (Pd) after exposure to the gas [40], and the disassociated molecules subsequently diffuse within the metal gate, as shown in Fig. 2b**.** Consequently, some hydrogen atoms diffuse through the gate metal, eventually producing the dipole at and within the interface by changing the metal-work function. As a result, we have examined the $\mathbf{I_{ON}/I_{OFF}}$

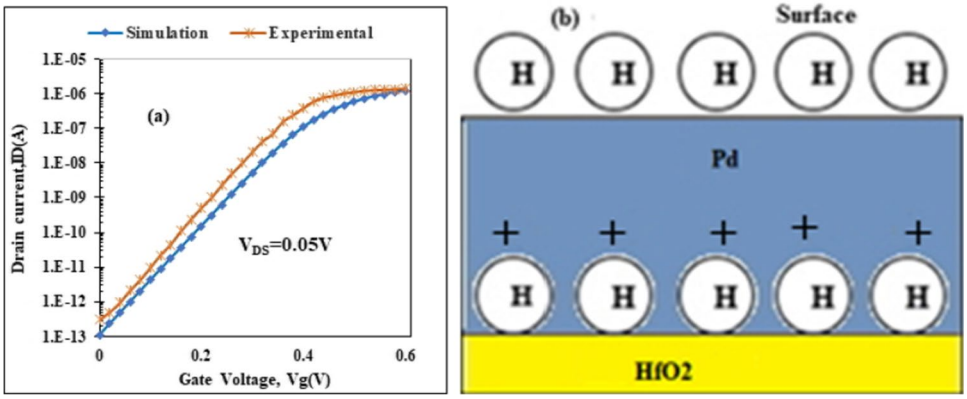

Fig. 2 illustrates (**a**) Calibration with simulation results at V_{DS}=0.05V with the experimental result [42] and (**b**) 2D Electrical dipole generation at the Pd/HfO_2 interface

ratio, drain-off sensitivity **(S_{Ioff}),** and the proposed device's performance shift in threshold voltage.

1.3 Analytical modeling

Using boundary conditions, surface potential in the radial direction is obtained;

$$\phi_S(z) = Ae^{kz} + Be^{-kz} + \boldsymbol{\Phi} \tag{1}$$

Here k is described by

$$k = \sqrt{\frac{2\varepsilon_{OX}}{\varepsilon_{Si}R^2\ln\left(1+\frac{t_{OX}}{R}\right)}} \tag{2}$$

And Φ is given by

$$\boldsymbol{\Phi} = V_{gs} - V_{fb} - qN_{Si}/\varepsilon_{Si}k^2 \tag{3}$$

I) As a function of z, the surface potential is given by:

$$\phi(r=0,z) = \phi_c(z) \tag{4}$$

II) At the center of silicon substrate's electric field is zero and expressed as:

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=0} = 0 \tag{5}$$

At the boundary of silicon oxide, the electric field is computed as follows:

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{C_{OX}}{\varepsilon_{si}}\left(V_{gs} - V_{fb} - \phi\left(r=\frac{t_{si}}{2},z\right)\right) \tag{6}$$

Oxide capacitance per unit area (C_{ox}) is obtained;

$$C_{OX} = \frac{\varepsilon_{OX}}{(R/2)\ln\left(1+\frac{t_{OX}}{R}\right)} \tag{7}$$

Here, t_{Si} is silicon thickness, R is silicon (channel) radius, $\varepsilon_{Si}$is permittivity of silicon, and ε_{OX} is oxide layer permittivity. The variation in the catalytic metal work function at the metal surface by the reactivity of gas molecules is denoted by $\Delta\Phi_m$, and the flat-band voltage is $V_{fb,}$ and V_{fb} is described by [5, 9];

$$V_{fb} = \phi_m - \phi_{Si} \pm \boldsymbol{\Delta\Phi}_m \tag{8}$$

where ϕ_{Si} represents for a silicon work function and is obtained by;

$$\phi_S = \frac{E_g}{2} + \chi + q\phi_{fp} \tag{9}$$

The value of $\Delta\Phi_m$is expressed using Eq. (10)**:**

$$\Delta\phi_M = \boldsymbol{cont.}(\boldsymbol{\Phi}_m) - \left(\frac{RT}{4F}\right)lnP \tag{10}$$

Where T is for absolute temperature, P is for partial hydrogen gas pressure, R is for hydrogen gas constant, and F is for Faraday's constant. A and B are coefficients obtained using source and drain boundary conditions and determined using the formula;

$$A = \frac{\left(V_{bi}+\phi\right)\left(1-e^{-kL}\right)+V_{ds}}{2\sinh(kL)} \tag{11}$$

$$B = \frac{\left(V_{bi}+\phi\right)\left(e^{kL}-1\right)-V_{ds}}{2\sinh(kL)} \tag{12}$$

As illustrated below, the quasi-fermi-potential changes along the channel direction are used to calculate the drain current from the source to the drain.

$$\phi(r,z) = \phi_S(z) + \frac{C_{OX}}{2\varepsilon_{Si}R}\left(V_{gs} - V_{fb} - \phi_S(z)\right)\left(r^2 - R^2\right) \tag{13}$$

As seen below, the subthreshold current is determined using a 2-D potential relation.

$$I_{sub} = 2\pi R\mu q n_i \frac{\int_{V_S}^{V_d} e^{-qV(z)/KT} dv(z)}{\int_0^L \frac{dz}{\int_0^R e^{q\phi(r,z)/KT} dr}} \tag{14}$$

2 Threshold Voltage (V_{th}) Modeling

For a p-channel MOSFET device, threshold voltage(V_{th}) in an enhancement mode can be obtained [43] using Eq. (15).

$$V_{th} = V_{(T,0)} + \gamma\left(\sqrt{|V_{SB} + 2\varphi_F|} - \sqrt{|2\varphi_F|}\right) \tag{15}$$

where V_{th} is the threshold voltage, $2\varphi F$ is the surface potential, V_{SB} is the source-to-body substrate bias, $V_{(T,0)}$ is the zero substrate bias threshold voltage, and (γ) is a constant body effect parameter given by;

$$\gamma = \left(t_{OX}/\varepsilon_{OX}\right)\sqrt{2q\varepsilon_{Si}N_A} \tag{16}$$

Here, t_{ox} is oxide thickness, ε_{ox} is the relative permittivity of oxide, N_A is the doping concentration, q is the charge of an electron, and $\varepsilon_{Si}$is the relative permittivity of silicon semiconductors.

Temperature affects the threshold voltage of a CMOS device, in addition to how oxide thickness affects threshold voltage as shown in Eq. (2);

$$\varphi_F = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{17}$$

Where n_i is the silicon intrinsic doping Parameter, k is Boltzmann's constant, φ_F is the contact potential, and T is Temperature[12].

$$n_i = 5.2x10^{15}xT^{3/2}xexp\left(\frac{-E_g}{2KT}\right) \tag{18}$$

Here E_g is the bandgap energy of the silicon channel material. For GAA-JL-SiNWFET, the equation for the threshold voltage depending upon the device's radius is given by Eq. (19) [44].

$$V_{th} = \Delta\varphi + \frac{KT}{q}\ln\left(\frac{8KT\varepsilon_{Si}}{q^2 n_i}\right) - \frac{2KT}{q}\ln\left[R\left(\frac{1+t_{OX}}{R}\right)^{\frac{2\varepsilon_{Si}}{\varepsilon_{OX}}}\right] \tag{19}$$

Here **R** is the device's radius, and the work function difference is $\Delta\varphi$.

Summary of fabrication flowchart for the proposed device[24] Fig. 3.

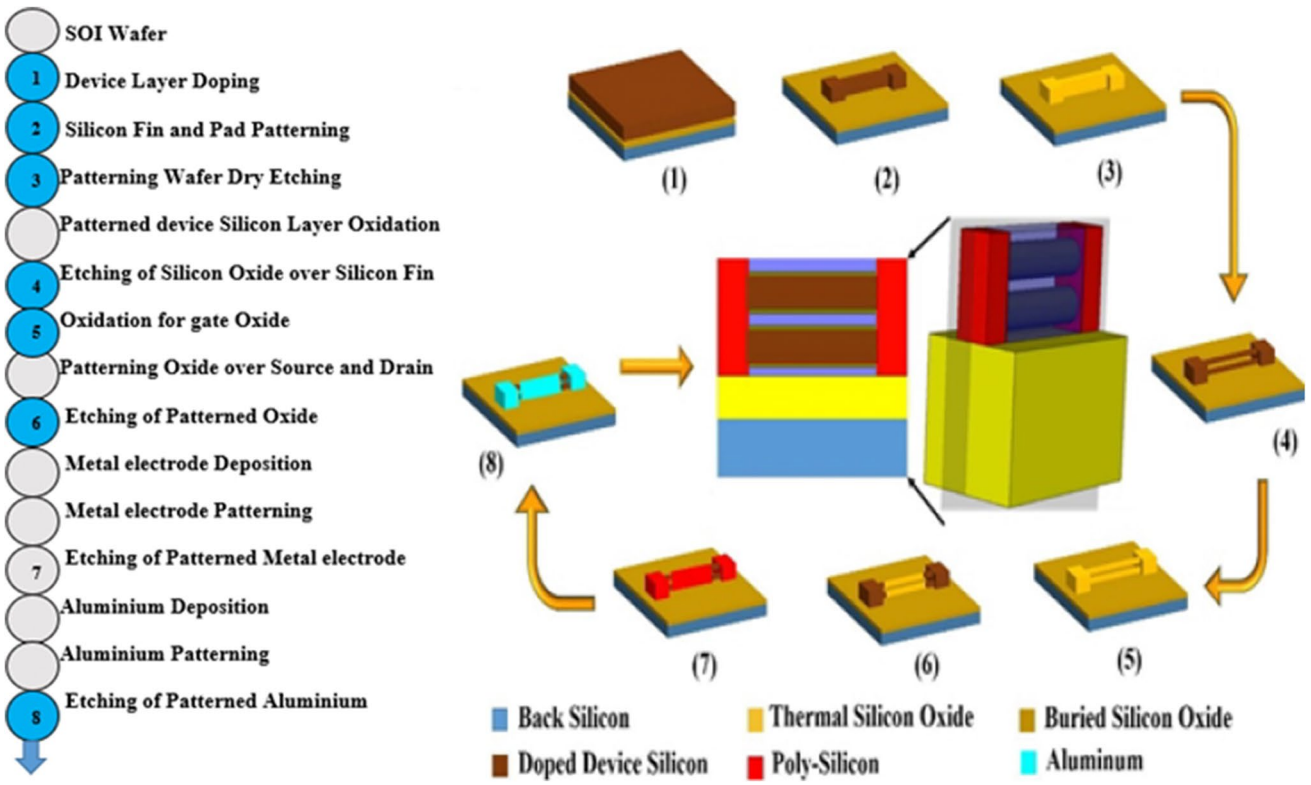

Fig. 3 Describes the fabrication process flowchart and schematic view for the JL-GAA-SiNWFET fabrication process, adapted [24]

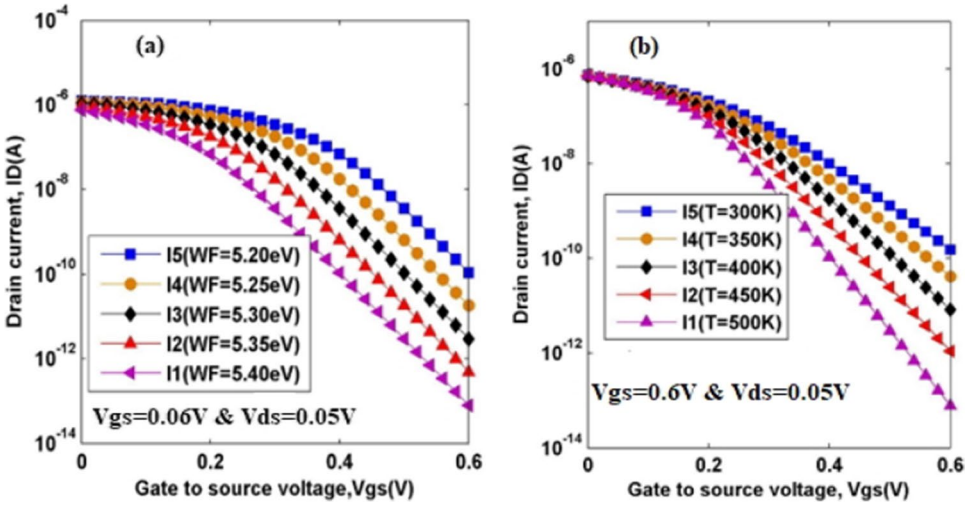

Fig. 4 illustrates the impact of **(a)** palladium (Pd) work function and **(b)** Temperature on I_D-V_G for p-type substrate cylindrical JL-GAA-SiNWFET

3 Results and Discussion

3.1 Change in drain current

In this work, a change in drain current can also be considered a critical characteristic for identifying hydrogen gas molecules. The change in drain current for a p-type gate-all-around junctionless SiNWFET sensor with a palladium metal gate work function and temperature variation is depicted in Fig. 4. The work function of the catalytic metal gate is controlled by the chemical reaction of hydrogen gas molecules on its surface [22]. In this case, the device's hydrogen gas sensitivity is expressed as a change in the threshold voltage and drain current [20]. For instance, shifting in drain current for the proposed device when the work function changes from 5.20eV to 5.40eV is $1.08x10^{-10}$A and when the temperature varies from 300K to 500K is $1.0x10^{-8}$A, as illustrated in Fig. 4a and b, respectively. In both cases, OFF-current changes rapidly in puny inversion region and is inversely proportional to hydrogen gas concentration due to the impact of metalwork function and temperature variation. As a result, the subthreshold zone provides substantially higher sensitivity while operating at low power, resulting in a low-cost hydrogen gas sensor device. This enhanced sensitivity in the subthreshold region is attributable to different band bending in the nonappearance of Fermi level restraining caused by a shift in palladium metal gate work function following hydrogen gas molecule surface reactivity [9]. We conclude that the proposed device will be desirable for detecting hydrogen gas molecule leaks that could have severe impacts, like an explosion, and the device's sensitivity is obtained Eq. (20).

a) **Change in surface potential**

Figure 5a shows the change in surface potential induced by a shift in the palladium metal work function (5.20 and 5.40 eV). The work function of the catalytic metal gate is altered by the reactivity of hydrogen gas

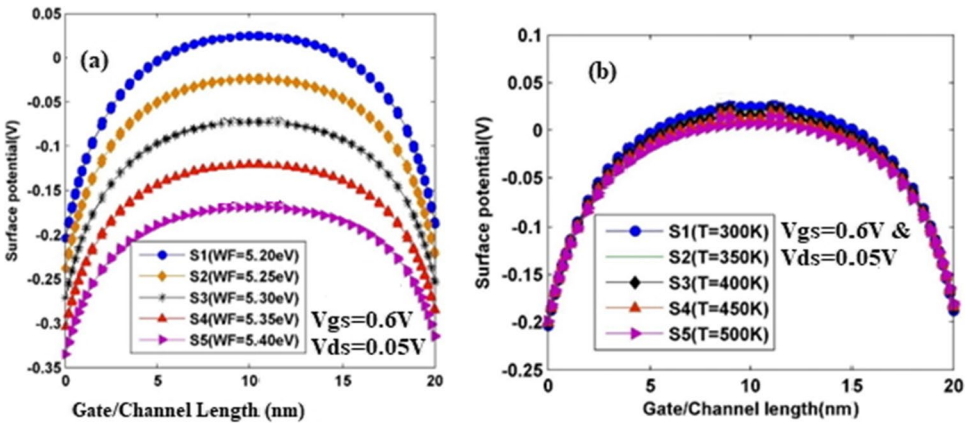

Fig. 5 impact of **(a)** palladium (Pd) work function and **(b)** Temperature on center potential (V) for p-type substrate cylindrical JL-GAA-SiNWFET

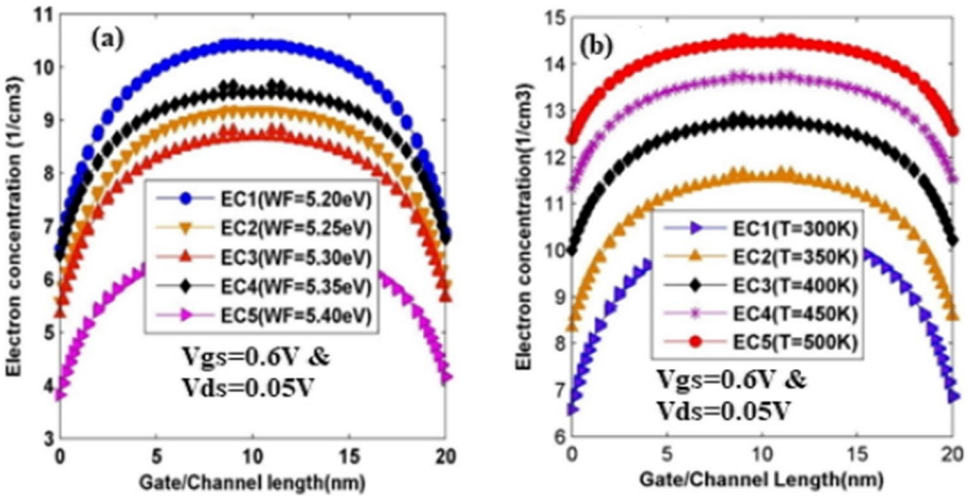

Fig. 6 influence of **(a)** palladium (Pd) gate work- function and **(b)** Temperature variation on electron concentration (1/cm^3) for p-type substrate cylindrical JL-GAA-SiNWFET

molecules at the gate surface, resulting in further band bending and a change in flat-band voltage, as indicated by Eq. (8) [3, 9].

Figure 5a shows that adjusting the work function impacts the surface potential of p-channel junctionless GAA-SiNWFETs with palladium (Pd) metal gates. The work function of the catalytic metal gate is altered by the reactivity of hydrogen gas molecules at the gate surface, resulting in considerable band bending and a shift in flat-band voltage [3, 5], which causes electrical outputs. Such as drain current, surface potential, and threshold voltage (V_{th}) shift when the flat-band voltage varies [45]. Using a palladium catalytic metal gate, it is feasible to sense the existence of hydrogen gas molecules by measuring the shifting of $\mathbf{I_{OFF}}$, switching ratio, and $\mathbf{V_{th,}}$ as clearly described in Fig. 6. Variation of temperature also impacts surface potential, as depicted in Fig. 5b) and significantly represents the proposed device sensing capability.

b) **Change in electron mobility**

The electron mobility throughout the channel was also extracted, as shown in Fig. 6. The change in electron concentration due to the shift in palladium metal work function (5.20 and 5.40 eV) is examined in Fig. 6a). The work function of the catalytic metal gate is altered by the reactivity of hydrogen gas molecules at the gate surface, leading to different band bending and a shift in flat-band voltage [3, 9], causing mobility of electrons across the channel. As seen in Fig. 6), the shift in electron concentration in the channel region is substantially more significant than in the source and drain regions. Because the electric field in the channel is affected by electron concentration and the flow of charges in the channel [24]. Figure 6b) shows the impact of temperature on electron concertation for the proposed device.

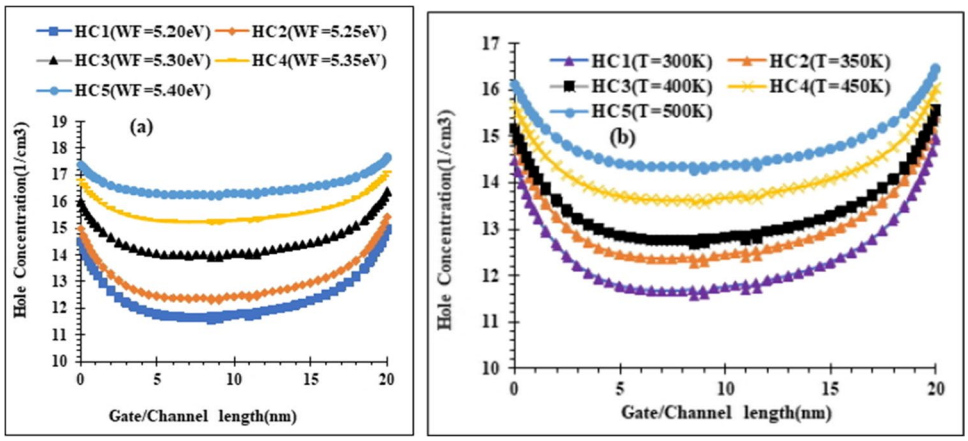

Fig. 7 effect of **(a)** palladium (Pd) work function and **(b)** Temperature variation on hole concentration (1/cm^3) for p-type substrate cylindrical JL-GAA-SiNWFET

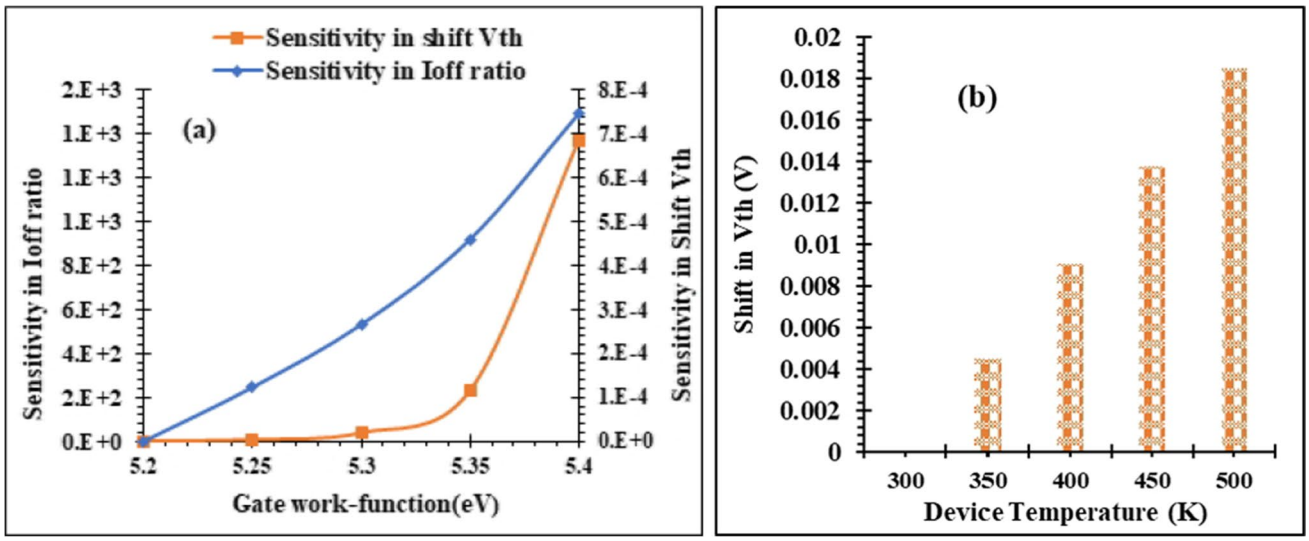

Fig. 8 effect of **(a)** palladium (Pd) metal gate work and **(b)** Temperature on I_{OFF}-current ratio for p-type substrate cylindrical JL-GAA-SiNWFET

c) **Change in hole mobility**

The hole mobility throughout the channel was also extracted, as shown in Fig. 7. The change in hole concentration due to the shift in palladium metal work function (5.20 and 5.40 eV) is examined in Fig. 7a). The reactivity of hydrogen gas molecules at the catalytic metal gate surface alters the gate metal's work function, resulting in further band bending and a change in flat-band voltage [3, 9]. As shown in Fig. 7), the channel's hole concentration difference is considerably less than in the source and drain regions. Because the electric field in the channel is affected by hole concentration, the flow of charges in the channel is also influenced, resulting in drain current and, eventually, device sensitivity. The effect of temperature on hole concentration is depicted in Fig. 7b), and device performance should be significant at room temperature. We examine that the proposed technology has shown to be promising for hydrogen gas detection applications.

d) **Shifting in drain current and threshold voltage**

The impact of palladium (Pd) work function and temperature variations on device sensitivity are investigated to assess device performance and stability shown in Fig. 8. Figure 8a reflects the sensitivity of gate all around junctionless SiNWFETs as a palladium metal work function in terms of $\mathbf{I_{off}}$ ratio and shift in threshold voltage (ΔV_{th}). It can be shown that gate all around junctionless SiNWFETs has better sensitivity at higher palladium (Pd) metalwork functions [41]. Since the flat-band voltage changes as the palladium gate's metal work function rise due to higher band bending. Due to variations in the palladium metal gate work function, a change in flat-band voltage induces a shift in drain current, threshold voltage(Vth), and [9]. It is thus feasible to identify the existence of hydrogen gas molecules by monitoring changes in I_{ON}, ΔV_{th}, and I_{OFF}.

Consequently, some hydrogen atoms diffuse through the gate metal, eventually producing the dipole at and within the interface by changing the metalworking function. In this regard, we have examined the I_{ON}/I_{OFF} ratio, drain-off sensitivity **($\mathbf{S_{Ioff}}$),** and shift in threshold voltage of the proposed devices extracting those output results during the simulation, and factors can be regarded as sensitivity variables. We have also shown electron and hole mobility and potential surface distribution along the channel, and carrier transport mechanism has been obtained through NEGF model simulations to obtain the drain current, surface potential, electron and hole mobility and subsequently threshold voltage concerning variation Pd work function and temperature.

When the work function is increased, sensitivity changes exponentially, as seen in Fig. 8a), and it may be estimated using Eq. (20)**.**

$$S_{I_{OFF}} = \frac{I_{OFF(\mathit{after gas reaction})} - I_{OFF(\mathit{before gas reaction})}}{I_{OFF(\mathit{before gas reaction})}} \tag{20}$$

Another essential parameter employed in detecting gas molecules is shifting threshold voltage (ΔV_{th}) and defined as the difference between the threshold voltage with and without hydrogen gas adsorption is defined as (ΔV_{th}) is depicted in Fig. 8) as a function of palladium metal gate work function and temperature. Higher (ΔV_{th}) and $S_{I_{OFF}}$ (shown in Fig. 8) reflects higher palladium metal gate and temperature values, indicating that JL-SiNWFET is well suited for hydrogen gas sensing. As the palladium metal work function

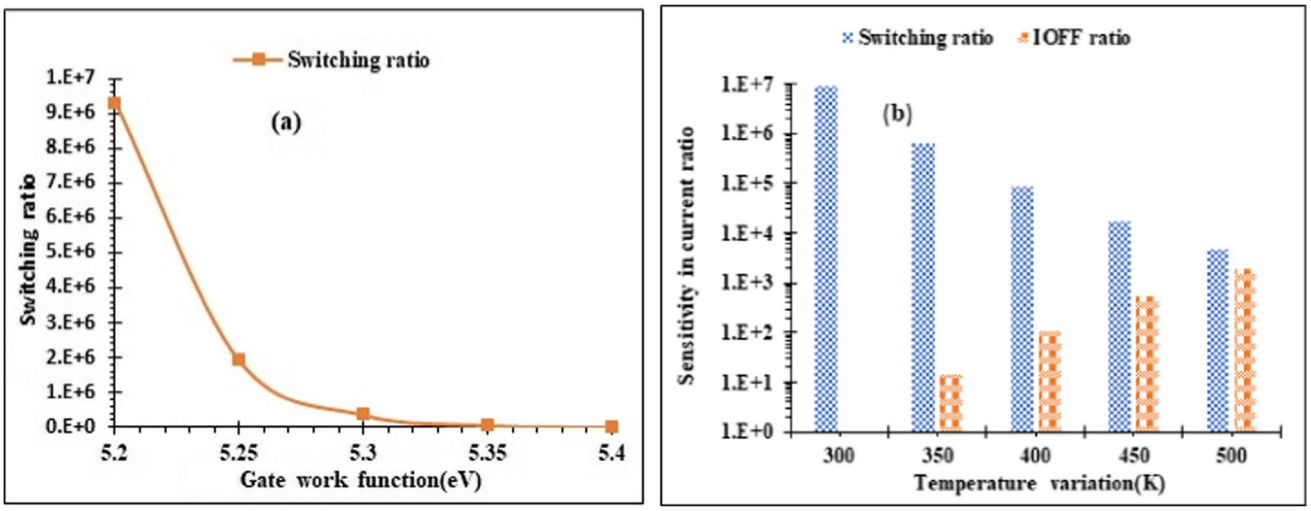

Fig. 9 effect of **(a)** palladium (Pd) metal gate work function on switching ratio and **(b)** Temperature on shifting threshold voltage for p-type substrate cylindrical JL-GAA-SiNWFET

and temperature increase, a shift in threshold voltage (Vth) arise, resulting in increased hydrogen gas molecule concentration, as seen in Fig. 8), which can be calculated using Eq. (21)**.**

$$\Delta V_{th} = \left| V_{th(\textit{aftergasreaction})} - V_{th(\textit{beforegasreaction})} \right| \tag{21}$$

The impact of palladium (Pd) work function and temperature variations on device switching ratio using different Pd work functions and temperatures to assess device performance and stability as illustrated in Fig. 9. Figure 9a reflects the impact of varying palladium metal work functions on the switching ratio for junctionless gate all around SiNWFETs device. Our proposed device has a lower switching ratio at higher palladium(Pd) metalwork functions. Sensitivity in the switching ratio is lowered as temperature rises (as illustrated in Fig. 9b); sensitivity in terms of I_{OFF} ratio increases as temperature increases (Fig. 9b).

Figure 10 effect of palladium (Pd) work function variation on **(a)** switching ratio and **(b)** leakage current reflects the impact of changing the work function on the switching ratio and leakage current characteristics on our suggested device**.** Figure 10**)** illustrates the analytical model validation with

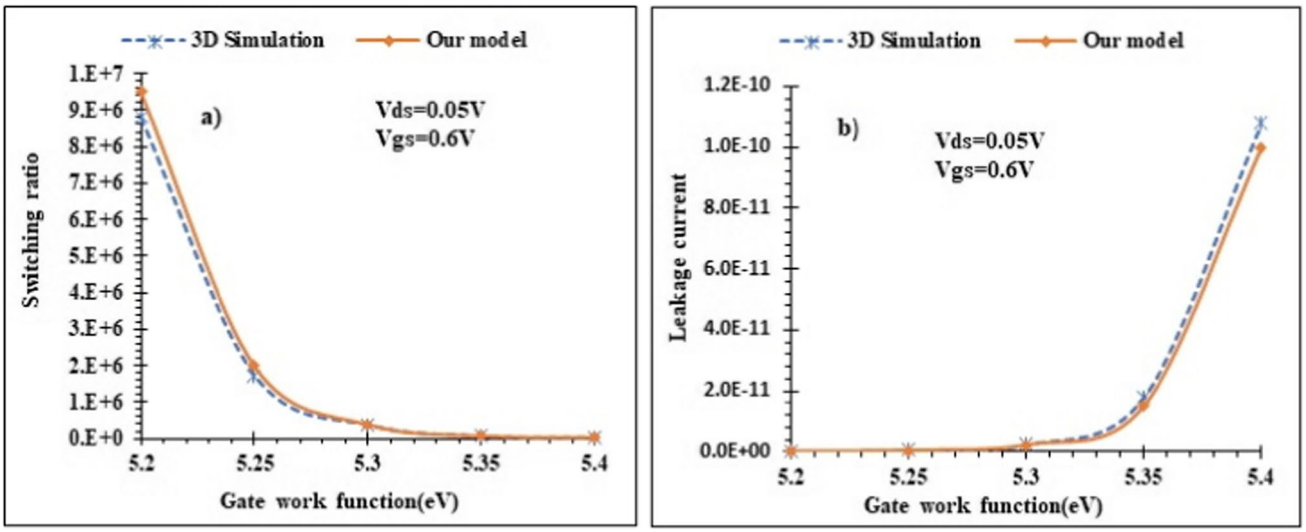

Fig. 10 effect of palladium (Pd) work function variation on **(a)** switching ratio and **(b)** leakage current for p-type substrate cylindrical JL-GAA-SiNWFET

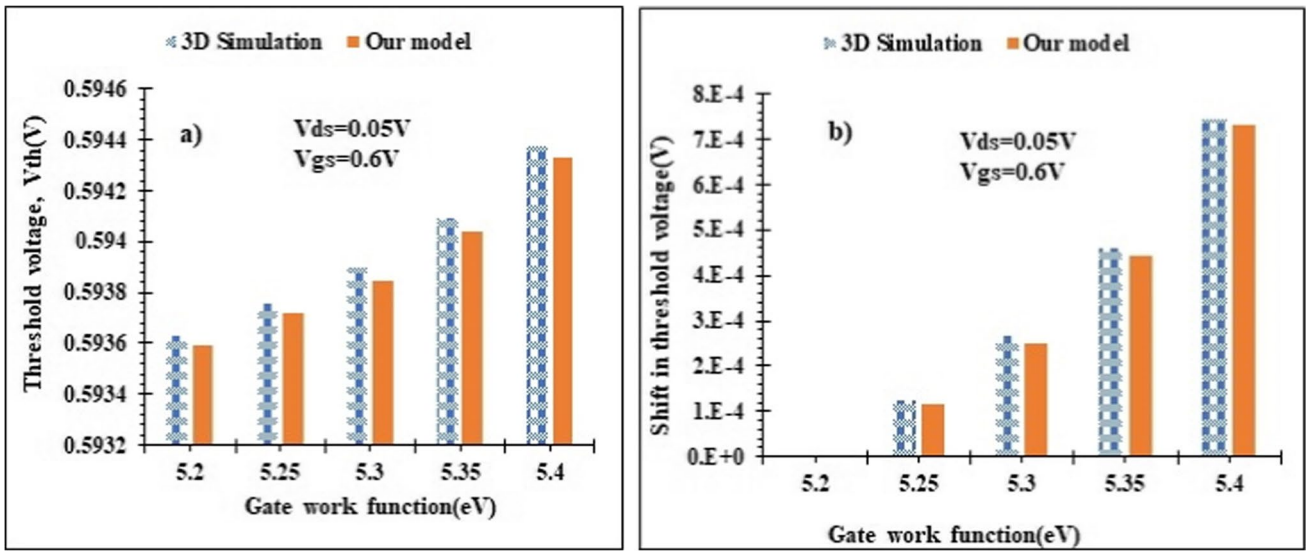

Fig. 11 impact of palladium (Pd) work function variation on **(a)** threshold voltage (V_{th}) and **(b)** shifting on threshold voltage(ΔV_{th}) for p-type substrate cylindrical JL-GAA-SiNWFET

the simulation results, which is validated more by the close proximity of our proposed devices.

Figure 11) illustrates the influence of changing the work function on the threshold voltage and shifting threshold voltage characteristics on our suggested device. Figure 11) clearly demonstrates that the analytical model is validated more by the proximity of our proposed device's analytical and simulated results.

Table 2 Examines sensitivity comparison of bulk MOSFET, GAA MOSFET, and JL-GAA-SiNWFET device concerning Off-state current for hydrogen gas sensor after and before gas reaction generated by gas molecules when the threshold voltage of all devices was adjusted at the same

Table 2 Pd gate sensitivity comparison shows the p-type substrate of bulk MOSFET, GAA-MOSFET, and JL-GAA-SiNWFET

$$S_{I_{OFF}} = \frac{I_{OFF(after\,gas\,reaction)} - I_{OFF(before\,gas\,reaction)}}{I_{OFF(before\,gas\,reaction)}}$$

	Previously designed device [5]		*Proposed device*
Shifting in Pd work function	Bulk-MOSFET $t_{Si}=20nm$	GAA MOSFET $t_{Si}=20nm$ R=10nm	JL-GAA-SiNWFET $t_{Si}=10nm$ R=5nm
$\Delta\Phi_m=50$mV	5.08	5.96	6.17
$\Delta\Phi_m=100$mV	4.56	33.10	37.80
$\Delta\Phi_m=150$mV	102	151	229

Device parameters: Drain, Source, and Channel doping (N_{Si})=$10^{19}cm^{-3}$. Oxide thickness is 1.5&0.3nm, oxide dielectric constants (HfO_2 & SiO_2 are 25.0 & 3.90, respectively), channel length(L)=40nm, drain to source voltage (V_{DS})=0.05V, gate to source voltage (V_{GS})=0.6V, and radius(R)=5nm.

values. When the sensitivity of JL-GAA-SiNWFET was compared to the sensitivity of bulk MOSFET and GAA MOSFET, the sensitivity was found to be more in JL-GAA-SiNWFET because the sensitivity ($S_{I_{off}}$) equation tells us that the hole mobility is related to the subthreshold leakage current. This provides that the subthreshold current in bulk MOSFET and GAA MOSFET devices is higher than JL-GAA-SiNWFET. Since the JL-GAA-SiNWFET structure experience, a higher surface-to-volume ratio and its channel exposed to more effective gate control than others at gate-source voltage are zero, resulting in a more significant variation in subthreshold current when the work function of the gate metal was altered as the gas molecules react with the catalytic metal gate. For instance, the sensitivity $\left(S_{I_{OFF}}\right)$, of proposed JL-GAA-SiNWFET compared with GAA-MOSFET and bulk MOSFET, JL-GAA-SiNWFET shows improved sensitivity. The results show that as 150mV work function shift of Pd at the gate, the sensitivity improvement with JL-GAA-SiNWFET based hydrogen gas sensors is 51.65% and 124.51% compared with GAA-MOSFET and MOSFET, respectively. Due to high dielectric oxide(HfO_2) and interface oxide(SiO_2) suppressing electron tunneling and hole mobility at gate-source voltage vanishes.

Finally, we have summarized the results here; as we have studied different articles, hydrogen is one of the essential future clean energy sources on the road to a more sustainable world and replacing fossil fuels [45, 46]. For instance, the availability of hydrogen may serve as one of the primary drivers of the energy shift and decarbonization [37]. In order to handle hydrogen safely, robust sensors are highly desired. Particularly, it has been shown that the active materials

(Palladium) employed in these sensors exhibit the high sensitivity to H_2 required for practical applications and that nanostructuring of these materials enables a reduction in response time of the sensors and a close approximation to the industry standard [22]. Due to these and other applications, we studied and designed a Palladium gate modulated JL-GAA-SiNWFET based hydrogen sensor, and it is crucial in applications where health is of particular significance due to their unique qualities, particularly their innately low fire risk, making them the technology of choice; for instance, in mass transit hydrogen-powered vehicles and H_2 accidental leakage [5]. Integrating the palladium electrode in the proposed device enhances device sensitivity performance, lifetime, and reliability. Therefore palladium electrode material is a very sensitive and selective material for H_2 and does not require oxygen to carry out [45]**.** For various applications, Palladium JL-GAA-SiNWFET based hydrogen sensor has been examined; since hydrogen is odorless compared to gasoline fuel, it is used for the detection of H_2 leakage in the area of hydrogen fueling stations [37], hydrogen pipelines distribution and transmissions [15], cryogenic hydrogen storage tanks(since such storage tanks constantly release H_2, leads to change in partial pressure), hydrogen fuel cells (utilized in automobiles and can serve as a backup for generators and small power plants) [41], its water resistance (since, the majority of fuel cells operate with surplus liquids, including water) [20], hydrogen safety and control(increased use of hydrogen fuel leads to more H_2 infrastructure incidents) [15], and widely used in industrial settings due to their dependability and excellent sensitivity of H_2. Because of the increasing need for hydrogen fuel, efficient hydrogen detection is crucial in many industries for everyday safety and process development. Not only these, Junctionless Gate-All-Around SiNWFET-based hydrogen gas sensor is excellent electrostatic control of short channel effects (SCEs). Due to these and other physical significance, we have studied Palladium integrated junctionless gate all around SiNWFET-based hydrogen gas sensor.

4 Conclusion

Through Silvaco-TCAD simulations and analytical model development, this work verified a Junctionless GAA silicon Nanowire transistor with a palladium (Pd) metal gate as a viable sensor for detecting hydrogen gas based on an electrical detecting approach. The resulting analytical model's shifting threshold voltage (ΔV_{th}) and shifting subthreshold current (S_{IOFF}) sensitivities are consistent with simulation data. These results indicate higher sensitivity values at higher palladium metal work function and temperature variations due to increased gas surface covering over the Pd metal gate $|\Delta\phi_m|$. We have examined that the catalytic palladium metal gate JL-GAA-SiNWFET sensor has a higher hydrogen gas molecule sensitivity than GAA-MOSFET and conventional bulk MOSFET due to its larger surface-to-volume ratio in addition to improved performance. As is confirmed in Table 2, the percentage improvement in the subthreshold drain current ratio's sensitivity ($S_{I_{OFF}}$) are 124.51% and 51.65% when JL-GAA-SiNWFET compared with bulk MOSFET and GAA-MOSFET, respectively. So, the sensitivity parameter for hydrogen gas sensing in this investigation involves a change in subthreshold current, and it is a critical concern in addition to shifting threshold voltage((ΔV_{th}). This finding provides novel promises for using Pd island gate junctionless gates all around SiNW field-effect transistor sensors to detect hydrogen gas and is applicable for industries such as petrochemical plants, nuclear reactors, hydrogen manufacturing facilities, petroleum refineries, space launching, leak detection, fuel cells, medical diagnostics, and nuclear power plants.

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Data Availability The authors mentioned above have all relevant data related to this study effort and will be willing to disclose it if asked to do so in the future.

Authors' Contribution

All of the authors contributed to the study's inception and design.

Compliance with Ethical Standards The authors have reviewed all of the Ethical Standards and are expected to adhere to them in the future.

Conflict of Interests The authors declare they have no competing interests.

Consent to Participate & for the Publication Since the study report in question is for a 'non-life science journal,' So 'Not Applicable' in this case.

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ORIGINAL RESEARCH ARTICLE

Sensitivity Analysis of Biomolecule Nanocavity Immobilization in a Dielectric Modulated Triple-Hybrid Metal Gate-All-Around Junctionless NWFET Biosensor for Detecting Various Diseases

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Abstract

In this paper, a novel biomolecule nanocavity immobilization in a dielectric modulated triple-hybrid metal gate-all-around (THM-GAA) junctionless (JL) NWFET has been proposed to improve sensitivity for detecting various diseases. A comparative analysis of the dielectric modulated triple-hybrid metal gate-all-around JL-NWFET biosensor has been carried out with unique and double-hybrid metal gate (DHM) transistors immobilizing different biomolecules (neutral) such as streptavidin, ChO_X, APTES, uricase, and biotin in the nanogap cavity region. The simulation results were analyzed using the Atlas-3D device simulation tool. The work shows that higher work-function and higher dielectric materials near the drain suppress/overcome short-channel effects and quantum mechanical tunneling caused by hot-carrier and electron scattering due to a high electric field and saturation velocity. The impact of neutral biomolecules on device output characteristics such as switching (I_{ON}/I_{OFF}) ratio, shifting threshold voltage (ΔV_{th}), intrinsic voltage gain $\left(g_m/g_d\right)$, drain off-current sensitivity $\left(S_{I_{OFF}}\right)$, subthreshold slope, transconductance $\left(g_m\right)$, output conductance $\left(g_d\right)$, surface potential and output resistance $\left(1/g_d\right)$ has been studied. Sensitivity of the proposed device for detecting a specific neutral biomolecule was examined using a drain off-current ratio, and the results were compared with available works. The result shows a higher sensitivity in a triple-hybrid metal gate transistor than a unique and double-hybrid metal gate transistor in addition to available works, as we have discussed under the results and discussion section. For example, drain off-current sensitivity ($S_{I_{OFF}}$) in a triple-hybrid metal gate when a biotin biomolecule is immobilized uniformly in the nanogap cavity was 217.6% and 46.43% higher than a unique and double-hybrid metal gate transistor, respectively. We found that the proposed device can detect a specific biomolecule to diagnose different biomarkers for diseases such as breast and lung cancer.

Keywords Atlas-3D · biomolecule immobilization · dielectric modulated · THM · GAA-JL-NWFET

Introduction

Recently, biomolecular species detection is considered significant research for detecting biological diseases such as cardiovascular disease,[1] Alzheimer's disease,[2] breast cancer,[3] ovarian cancer, viral infections, and Ebola.[4] However, detection of biomolecules such as uricase, APTES, streptavidin, ChO_X and biotin using a conventional method such as spectrometry, optical measurements, and surface plasmon resonance involve multi-stage processes and are unsuitable for online monitoring.[5,6] For instance, detecting the DNA sample complex using an optical microarray reader is very expensive and leads to superfluous DNA labels in a single region of a microarray.[4] Also, these label procedures make the sample preparation more time-consuming and complex. In addition to device fabrication complexity, there is a growing demand for launching conservative clinical laboratories in remote areas, military fields, and rural areas to detect biomolecules. To overcome these and other drawbacks, the newer FETs such as tunnel field-effect transistors,[7] gate-all-around junctionless transistors,[8] and FinFET[9] have emerged because of their low power consumption, easy scalability,

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and high packing density under small-scale node technology.[10] Detection using NWFET-based biosensors enables the integration of boosting and analyzing circuits on the same chip by minimizing both cost and space,[11] and as a result, NWFET-based biosensors have sparked a lot of attention in recent years. There is a huge demand for efficient technologies that can rapidly and effectively analyze biological constituents such as biomolecules and cells with quick, specific drug detection (label-free).[12] As the technology has grown, MOSFET size has decreased to an increase in the number of transistors in a single chip and boost transistor efficiency.[13] Thanks to today's microelectronic technology, miniaturized biosensors downsized to ultra-small-scale device size leads to a significant improvement of electrical sensor detection of NWFET-based biosensors to actually work at the cell scale[14] because the ability to measure a single cell represents a significant step forward in understanding numerous biological phenomena.[15] NWFET-based sensors can detect the molecules, which are of nanometer size.[16] For example, various biological species such as atoms (0.1 nm), DNA (1 nm), proteins (10 nm), and viruses (10 -100 nm) are found at nanometer scale.[17–20] The proposed device detecting site/nanocavity with 10-nm thickness can fit with those biological molecules such as DNA, atoms, and proteins. Previously, written works such as low-power silicon nanowire-based inversion mode MOSFETs have been demonstrated for the detection of DNA[1, 8] proteins[4, 5, 8, 21–23] and pH levels.[24, 25] But at present, fabricating conventional FET biosensors at ultra-small-scale device size has critical issues such as short-channel effect (SCEs), drain-induced barrier lowering (DIBL), hot-electron effect, threshold voltage instability, impact ionization effect, sub-threshold swing, and gate tunneling current.[5, 26–28] For instance, at small-scale device dimensions, it is problematic to maintain low drain off-current (I_{OFF}) at the same time maintaining a significant drain on-current (I_{ON}). This leads to a short-channel effect (SCEs) and quantum mechanical tunneling.[29, 30] At the nanoscale regime, problems related to an ultra-sharp doping profile due to a "diffusion of impurities between a *p*- or *n*-type drain/source (D/S) region and an *n*- or *p*-type substrate/body region [give] rise [to] an interface charge which develops parasitic gate resistance in the manufacture of ultra-small-scale devices".[31]

In recent years, multi-gate, junctionless device structures such as surrounding-gate-FET, Fin-FETs, and double-gate (DG)-FET have been proposed, which can control and alleviate SCEs and enhance electrostatic gate controllability.[32, 33] So, junctionless dielectric modulated multi-gate MOS field-effect transistors are the most hopeful candidate architecture in CMOS fabrication technology due to their protection from short-channel effects (SCEs) and random dopant profile effect (RDE).[23] When the thickness of MOSFET gate oxide (SiO_2) reaches an extremum limit (around 1 nm and below), a hot-electron effect arises leading to short-channel effects, consequently degrading device performance.[26, 28, 34] To overcome those problems related to gate oxide thickness in the case of small-scale device fabrication, silicon dioxide (SiO_2) gate insulator should be substituted with high-k dielectric gate oxide material such as hafnium oxide (HfO_2, $\varepsilon = 25$) using gate engineering device scaling, keeping adequate oxide thickness (EOT) as constant.[28, 31, 35, 36] The interface oxide (SiO_2) layer limits the fringing electric field across the channel.[37]

This paper examines the impact of different biomolecules on the proposed device's output electrical characteristics (sensitivity analysis of biomolecule nanocavity immobilization in a dielectric modulated triple-hybrid metal gate-all-around (THM-GAA) junctionless NWFET biosensor) using the Atlas-3D device simulation tool to analyze a specific biomolecule for the detection of various diseases.

Device Structure and Its Working Principle

The designed structure for the proposed device is illustrated in Fig. 1. Gate lengths of G_1, G_2 and G_3 are L_1(6 nm), L_2(8 nm), andL_3(6 nm), respectively, L_4 (10 nm) is the length of the nanogap cavity and silicon dioxide (SiO_2) which are near the drain and source ends, respectively, and L (20 nm) is the length of the high-k oxide (HfO_2) and the interface oxide layer (SiO_2). T_1 T_2, T_3, and T_4 are thicknesses of the metal gate, biomolecule cavity, hafnium oxide, and interface (SiO_2) oxides, respectively, and 2R is the thickness of silicon film. The work functions of each metal gate are described in Table I. A tunable work function has been used to reduce the ionization effect induced by a high electric field near the drain end,[38] threshold voltage fluctuation, parasitic gate resistance, and channel doping fluctuation[39] in modeling the THM-GAA-JL-NWFET biosensor. The target biomolecules are assumed to be immobilized and interact uniformly with the device in the nanogap cavity region. Biomolecules such as APTES ($\varepsilon = 3.57$)), Choli oxidase (ChO_x, $\varepsilon = 3.30$), streptavidin ($\varepsilon = 2.10$), biotin($\varepsilon = 2.63$), and uricase($\varepsilon = 1.54$) were simulated interchangeably by presenting their dielectric constant in the cavity region. The air cavity ($\varepsilon = 1.0$) was also considered by introducing its dielectric constant in the cavity[31] and does not react with SiO_2 and HfO_2 oxide materials[32] leading to production of a unique trace of binding event due to a change in electrical properties. This can be used as the recognition layer in the nanogap cavity.[8] Because of this, the proposed device can further be used to identify various diseases depending on the biomolecule under investigation. For instance, biomolecules such as uricase are responsible for detecting uric acid in human blood serum,[40] and APTES can detect cancer cells[1] and

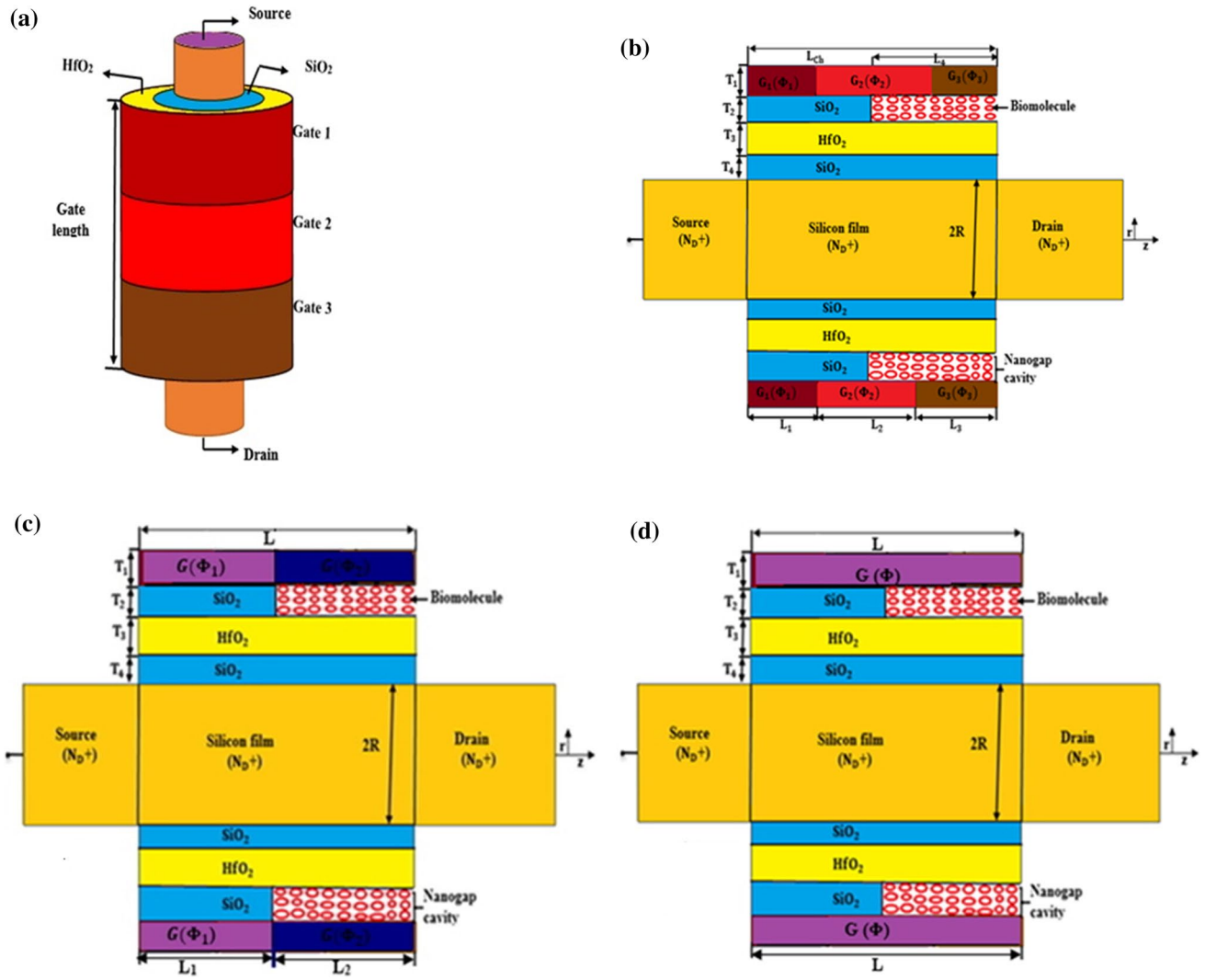

Fig. 1 (a) Illustrates the 3D schematic diagram. (b), (c), and (d) are 2D cross-sectional interpretations of n-type junctionless dielectric modulated unique, double-, and triple-hybrid metal gate-all-around NWFET biosensors, respectively.

Table I Designed parameters of double- and triple-hybrid metal GAA-JL-NWFET.

Physical device parameters	DHM-GAA-JL-NWFET		THM-GAA-JL-NWFET		
Channel length (nm)	20.0		20.0		
Oxide thickness,HfO_2 & SiO_2 (nm)	1.5 & 0.3		1.5 & 0.3		
Source oxide thickness SiO_2(nm)	1.0		1.0		
Source oxide length,SiO_2 (nm)	10.0		10.0		
Length of the cavity (nm)	10.0		10.0		
Length and thickness of source/drain (nm)	10.0		10.0		
Thickness of the cavity (nm)	1.0		1.0		
Thickness of siliconfilm (nm)	10.0		10.0		
Source/drain & channel doping (N_D+)	1×10^{19} cm^{-3}		1×10^{19} cm^{-3}		
HfO_2 and SiO_2 dielectric constants	25.0 & 3.9		25.0 & 3.9		
Metal gate work-function (eV)	4.50	4.894	4.50	4.86	4.96

thyroid diseases.[41] High doping concentration ($1\times10\ cm^{-3}$) has been applied uniformly during modeling of the THM-GAA-JL-NWFET biosensor through the channel from source to drain to have a tolerable threshold voltage variation and decreasing band gap separation.[42, 43]

Numerous simulations have been carried out using the materials listed in Table I and the Atlas-3D device simulator tool to study the impact of different biomolecules on electrical output characteristics in unique, double-, and triple-hybrid metal GAA-JL-NWFET.

Models incorporated in the simulations are carrier recombination and generation models for carrier mobility.[43] Doping versus mobility and high channel doping profile have been verified using the concentration-dependent mobility (CONMOB)[44] model along with the band gap narrowing (BGN) model. The carrier-carrier scattering (CCSMOB)[43] model has been used in the simulation is considered in our work due to the impact of high doping level, electron concentration, and hole concentration. Boltzman transport equations and Shockley–Read–Hall (SRH) were also used to account for the recombination of minority carriers under semiconductors without an impact ionization model.[44] The drift-diffusion model describes drain current as a function of drain voltage, including device surface potential that satisfies the model equations. The default values of the drift-diffusion model found in the ATLAS TCAD tool[43] are applied to describe the density of electron and hole change due to transport, generation, and recombination processes in the simulation,[45] and it is examined by Boltzmann transport approximation equations[46, 47] for accurate numerical simulation results.

The average time it takes an excess minority carrier to recombine is known as carrier lifetime and is determined by the SHR recombination lifetime model,[48, 49] and it can be used with the continuity equation to carry out carrier and recombination creation.[2] The statistics of recombination and creation of holes and electrons in semiconductors that occur via the trapping process are also described by the Shockley–Read–Hall (SRH) model.[50] The Concentration, Voltage, and Temperature (CVT) model has been applied in the simulation to study parallel and perpendicular field-dependent carrier and doping-dependent mobility.[44] Since the channel's radius is not less than 4 nm, quantum effect is not considered in our model.

Results and Discussion

Comparative Analysis on Dielectric Modulated Double- and Triple-Hybrid Metal GAA-JL-NWFET-Based Biosensors on Electrical Transfer Characteristics

The impact of biomolecules on subthreshold slope in both devices is illustrated in Fig. 2a. It is clear that, as the dielectric constant rises, subthreshold swing decreases because the biomolecule dielectric constant and metal work-function modulate electrostatic gate control by reducing threshold voltage roll-off through the channel such as with high-k materials, thereby improving gate control capacity.[51] In our study, for the APTES ($\varepsilon = 3.57$)

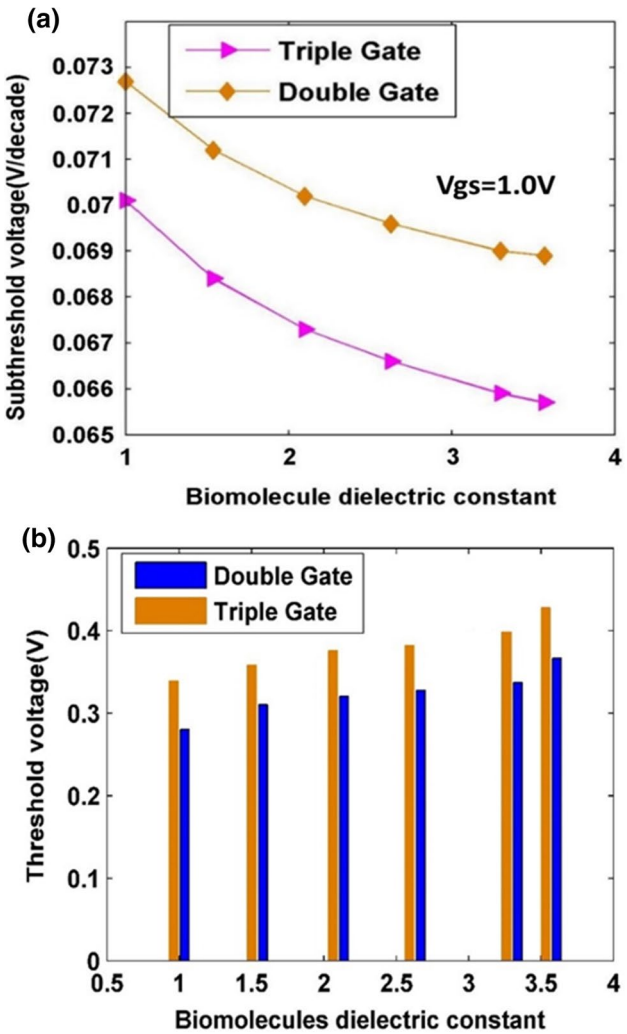

Fig. 2 Variation of (a) subthreshold slope (b) threshold voltage (V_{th}) versus biomolecules for n-type double- and triple-hybrid metal gate-all-around junctionless NWFET at a constant ($V_{DS} = 0.05$ V and $V_{GS} = 1.0$ V).

biomolecule, results of subthreshold slope in both devices are 6.90×10^{-2} V/decade and 6.50×10^{-2} V/decade for a double- and triple-hybrid metal gate transistor, respectively. Because of work-function (Φ_{G3}) suppression, there is a hot-electron effect and increase in carrier mobility through the silicon film.[52]

Figure 2b illustrates the impact of neutral biomolecules on the threshold voltage (V_{th}) for n-type double- and triple-hybrid metal gate-all-around junctionless NWFET. In both cases, as the dielectric constant rises, threshold voltage increases because threshold voltage roll-off is minimized by gate dielectric materials.[53] For instance, in the neutral APTES ($\varepsilon = 3.57$) biomolecule, the threshold voltage (V_{th}) in both devices are 0.33 V and 0.47 V for a double- and triple-hybrid metal gate, respectively, at $V_{GS} = 1.0$ V and $V_{DS} = 0.05$ V, which means there is 42.42% more improvement observed in the triple-hybrid than the double-hybrid metal gate. This threshold voltage variation (shift) indicates enhanced sensitivity in the triple-hybrid metal gate compared to the double-hybrid metal gate due to uniformity of carriers on the channel by the metal gate work-function.

Figure 3a demonstrates the effect of the neutral (APTES) biomolecule on drain current for unique, double-, and triple-hybrid metal gate-all-around junctionless NWFET. The tunneling current in the triple-metal gate is lower than a single- and double-metal gate because the gate work-function overpowers parasitic resistance and increases gate capacitive controllability.

Figure 3b illustrates impacts of neutral (air, uricase, streptavidin, biotin, ChO_X, and APTES) biomolecules to study their significant effect on leakage current in the case of double- and triple-hybrid metal gate devices, and the result shows that as the dielectric constant increases, leakage current decreases because the higher biomolecule dielectric constant increases gate electrostatic controllability by reducing electron tunneling from the gate and enhances gate control capacity.[51] This is because a higher gate dielectric oxide suppresses reverse tunneling current from the drain by creating a potential barrier in the channel region.[54] For instance, in the APTES ($\varepsilon = 3.57$) biomolecule, leakage current measurements in both devices are 2.32×10^{-12} A and 1.24×10^{-13} A for a double- and triple-metal gate, respectively. The work-function (Φ_{G2}) in the triple-metal gate forms barrier potential in the channel region, which enhances the driving current from source to drain lowering the high electric field and short-channel effect in the triple-metal gate compared to the double-metal gate device.[52]

Figure 4 demonstrates the effect of the biotin biomolecule on the output conductance and transconductance for unique, double-, and triple-hybrid metal gate-all-around junctionless NWFET. The output conductance (g_d) shown in Fig. 4a examines the first-order derivative of I_D, with

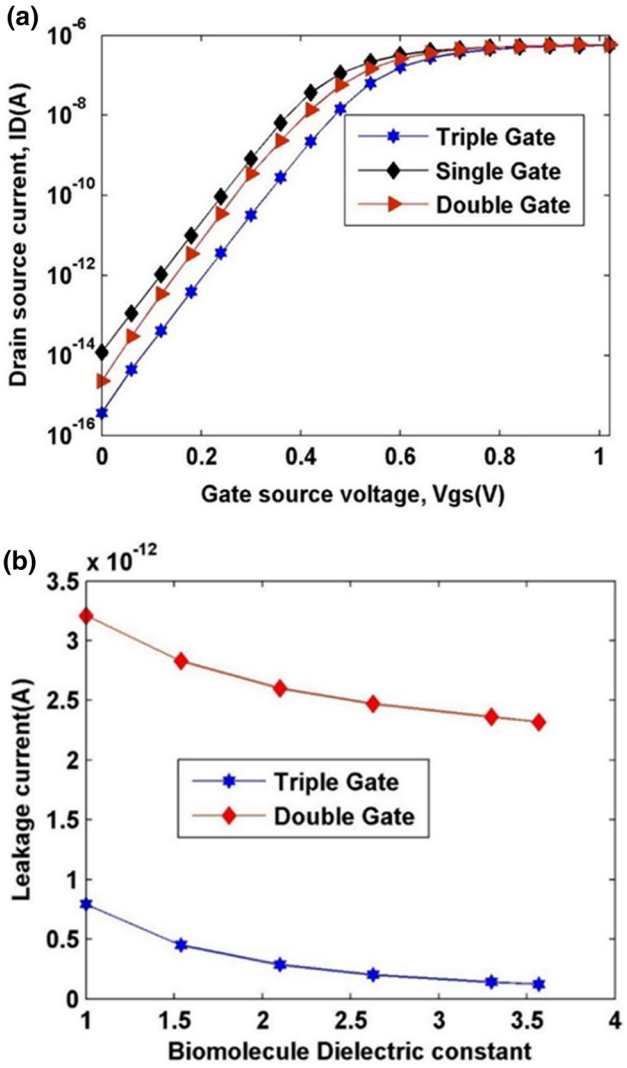

Fig. 3 (a) Drain current (I_D-V_G) and (b) leakage current comparison including different biomolecules for n-type unique, double-, and triple-hybrid metal gate-all-around JL-NWFET at ($V_{DS} = 0.05$ V and $V_{GS} = 1.0$ V).

respect to V_{DS} at constant $V_{GS} = 0.6$ V for all unique, double-, and triple-hybrid metal gate-all-around junctionless NWFET. It clearly shows that the triple-hybrid metal gate device shows lower output conductance (g_d) under a weak inversion region than the unique and double-hybrid gates due to lower drain-induced barrier lowering, short-channel effect, and parasitic resistance under the triple-hybrid metal gate device.[36, 55] The transconductance g_m described in Fig. 4b is the first-order derivative of I_D, with respect to gate-source voltage (V_{GS}) at constant $V_{DS} = 0.1$ V in the case of different gate engineering designs. At the cut-off region (gate-source bias voltage is equal to zero) and the weak inversion region (gate-source bias voltage is less than threshold voltage), higher transconductance in the case of unique and double-hybrid metal gates are recorded than

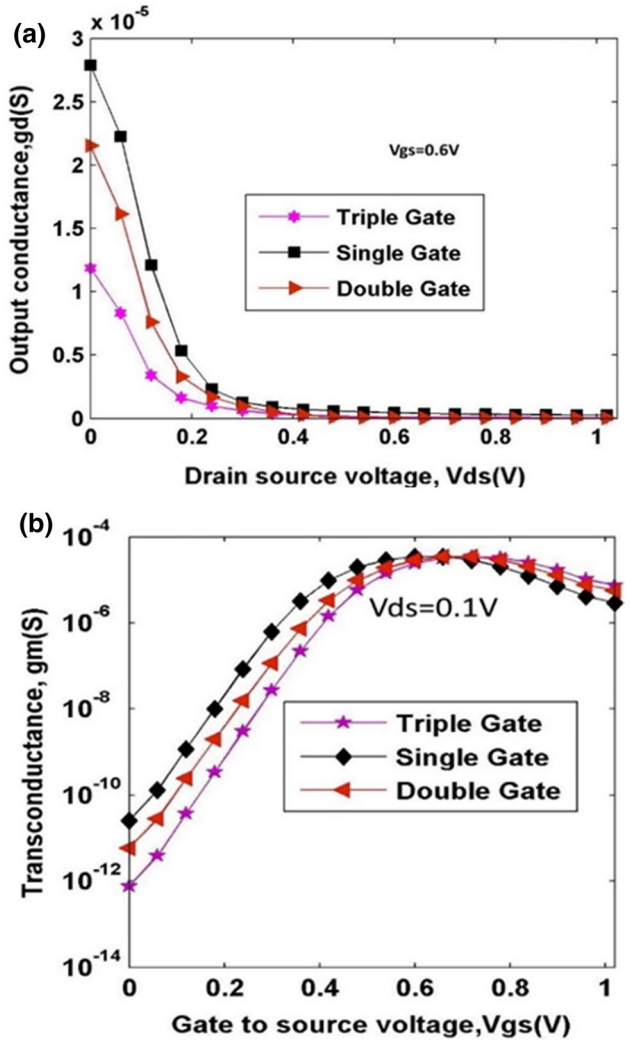

Fig. 4 Illustrates (a) the output conductance and (b) transconductance (g_m) comparisons for *n*-type unique, double-, and triple-hybrid metal gate-all-around JL-NWFET.

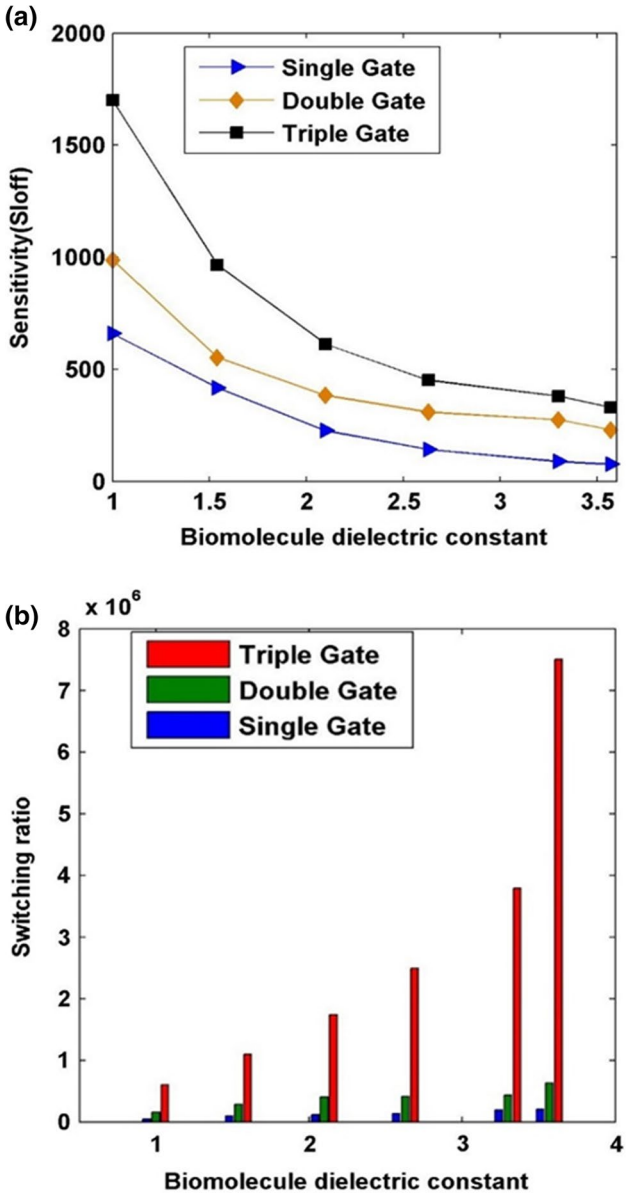

Fig. 5 Impact of biomolecules on (a) the sensitivity ($S_{I_{off}}$) and (b) switching ratio for n-type single-, double-, and triple-hybrid metal gate-all-around JL-NWFET at (V_{DS} = 0.05 V and V_{GS} = 1.0 V

triple-hybrid metal gate devices, while higher transconductance is recorded under the triple-hybrid metal gate device than unique and double-hybrid metal gate devices at the strong inversion region at $V_{GS} = 0.7$ V and $V_{DS} = 0.1$ V as shown in Fig. 4b. For instance, transconductance (g_m) measurements at constant $V_{GS} = 0.7$ V and $V_{DS} = 0.1$ are 2.34×10^{-5},2.63×10^{-5} and 2.72×10^{-5} siemens (S) in the case of unique, double-, and triple-hybrid metal gate devices, respectively. The percentage improvement of double and triple hybrid metal gates compared with unique metal gate devices are 12.39% and 16.24%, respectively. This is because the different gate work-function of THM-GAAJL-NWFET increases electrostatic coupling in the channel and improves carrier mobility, and surface potential across the channel proves the enhanced performance of the proposed device.[36]

Sensitivity Analysis and Switching Ratio Including Different Biomolecules

The impact of different biomolecules on drain off-current sensitivity ($S_{I_{off}}$) for unique, double-, and triple-hybrid metal gate-all-around JL-NWFET at $V_{DS} = 0.05$ V and $V_{GS} = 1.0$ V is illustrated in Fig. 5a. It clearly shows that the change in drain off-current sensitivity is higher for all devices at a lower dielectric constant due to lower electrostatic gate control and higher tunneling current. In contrast, as the dielectric constant of biomolecules increases, the change in drain off-current sensitivity

decreases due to impacts of higher dielectric constant modulating gate electrostatic control. For instance, drain off-current sensitivity using the triple-hybrid metal gate-all-around JL-NWFET for uricase ($\varepsilon = 1.54$) and APTES ($\varepsilon = 3.57$) biomolecules are 1.70×10^3 and 3.30×10^2 , respectively. This higher variation of drain off-current sensitivity in both cases indicates that tunneling current/leakage current controllability of thinner gate oxide increases for higher cavity dielectric material, as illustrated in Fig. 3b.

Figure 5b illustrates the impact of neutral biomolecules on switching ratio $\left(I_{ON}/I_{OFF}\right)$ for unique, double-, and triple-hybrid metal gate-all-around JL-NWFET at $V_{DS} = 0.05$ V and $V_{GS} = 1.0$ V. It clearly shows that the change in switching ratio $\left(I_{ON}/I_{OFF}\right)$ increases as the biomolecule's dielectric constant increases; therefore, the drain off-current ratio decreases since a higher biomolecule dielectric constant suppresses tunneling current and improves gate electrostatic controllability, and a higher gate work-function difference offers higher band bending near the source end, which increases the carrier mobility.[37] For instance, the switching ratio $\left(I_{ON}/I_{OFF}\right)$ is 6.26×10^5 and 7.50×10^6 for double- and triple-hybrid metal gate devices, respectively, when the APTES ($\varepsilon = 3.57$) biomolecule is immobilized in both nanocavity regions at the same condition. This higher switching ratio in the triple-hybrid metal gate is due to a potential barrier created in the channel region by gate work-function suppressing reverse tunneling from the drain [54] and indicates better device sensitivity when target biomolecules are immobilized uniformly in the targeted site. In addition to switching ratio, the new figure of merit used to determine device sensitivity under the weak inversion region is called drain off-current sensitivity $\left(S_{I_{OFF}}\right)$ is obtained using Eq. 1;[8]

$$S_{I_{OFF}} = \frac{I_{OFF[\text{with biomolecule}]}}{I_{OFF[\text{without biomolecule}]}}\Big|_{\text{at}\,V_{gs=0\,V}} \tag{1}$$

Drain Off-Current Sensitivity ($S_{I_{off}}$) of the THM-GAA-JL-FET Biosensor for Different Biomolecules

Figure 6 depicts the comparison of drain off-current sensitivity $\left(S_{I_{off}}\right)$ of dielectric modulated triple hybrid metal gate GAA-JL-FET with available work's[8] when different biomolecules were immobilized in the nanogap cavity. It clearly, depicts higher sensitivity variation when various biomolecules were uniformly immobilized on the nanogap cavity biosensor devices. This higher drain off-current sensitivity $\left(S_{I_{off}}\right)$ of dielectric modulated THM-GAA-JL-FET is attributed to its higher electrostatic gate control capability than the available works,[8] along with increased metal work-function value $\left(G_{\Phi 3}\right)$ that allows uniform carrier mobility in the inversion/channel region.

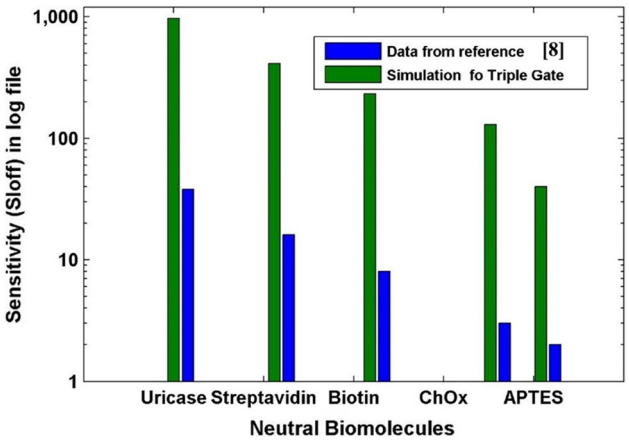

Fig. 6 Illustrates drain off-current sensitivity ($S_{I_{off}}$) comparison with available works[8] of n-type dielectric modulated triple hybrid metal-GAA-JL-FET, including different biomolecules.

Drain off-current sensitivity $\left(S_{I_{off}}\right)$ of the dielectric modulated triple-hybrid metal GAA-JL-FET,[8] switching ratio, and surface potential are improved over already available works,[8] due to new technologies incorporated in our device modeling such as device dimension, device structure, gate oxide material (high-k), and optimized gate electrode work-functions. Since our device has three oxide layers, namely, interface layer (SiO_2), high-k layer (HfO_2) and nanogap cavity layer, which is different from already available works, the new technology is more robust and controls tunneling current under 20-nm technology node and minimizes short-channel effects; this makes our work a better candidate for detecting various diseases caused by neutral biomolecules.

Effect of Nanogap Cavity Length on Device Sensitivity

Figure 7 depicts the effect of cavity length on the device transfer characteristics when different biomolecules were immobilized uniformly in the targeted site. The simulation results took place using 5-nm, 10-nm, and 15-nm cavity lengths, keeping gate length and nanogap cavity thickness constant. Figure 7a depicts the impact of different biomolecules on shifting threshold voltage at different cavity lengths. For instance, at 5-nm cavity length, shifting threshold voltage $\left(\Delta V_{th}\right)$ is lower than 10- and 15-nm cavity lengths due to a very small number of biomolecules embedded in the cavity region, contributing negligible significance to the change of the threshold voltage.[8] Higher threshold voltage variation is observed when nanogap cavity length increases, i.e., at half of the gate length, as shown in Fig. 7. Because the cavity length is determined based on the size of biomolecules to be detected (for instance, the size of

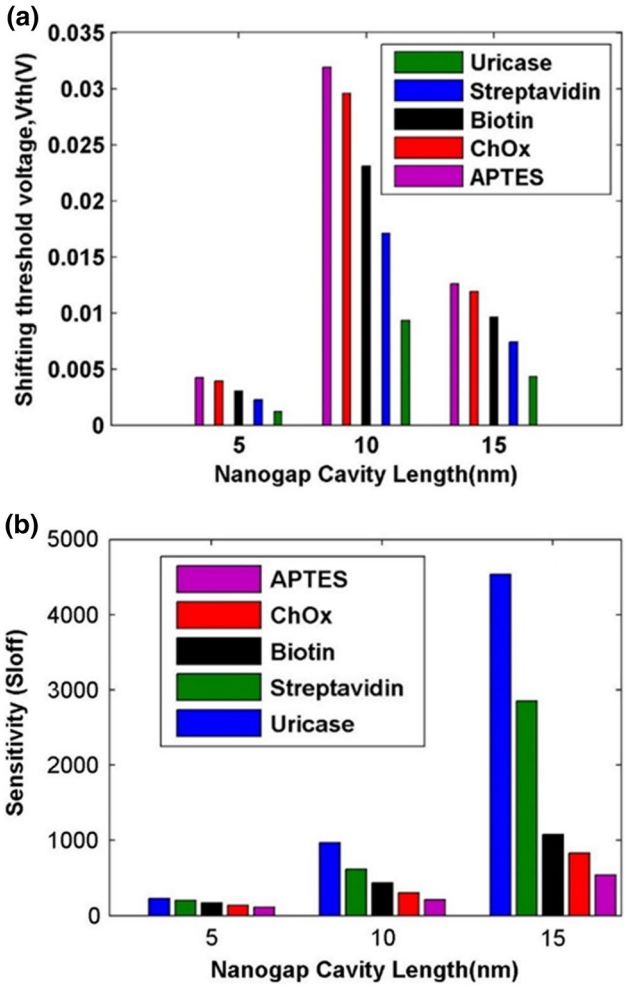

Fig. 7 Effect of cavity length on **(a)** shifting threshold voltage (ΔV_{th}), (b) drain off-current sensitivity ($S_{I_{off}}$) with different biomolecules for an n-type dielectric modulated triple-hybrid metal gate-all-around JL-NWFET at ($V_{DS} = 1.0$ V and $V_{DS} = 0.05$ V).

streptavidin and biotin are approximately 6-7 nm),[56] the sensitivity would have been high for biomolecules with dimensions approaching the cavity length. Therefore, it is also important to note that the gap in the nanoscale size significantly impacts the FET's electrical characteristics. I_{ON} reaches a maximum value/saturation when the gate length is almost fully covered by a higher dielectric biomolecule constant and threshold voltage roll-off (threshold voltage fluctuation) almost constant, leading to a decrease in threshold voltage due to small band bending amplitude in the case of higher biomolecule dielectric constant. Maximum drain current occurs because the channel gets "pinched off" at the drain end and leads to current saturation behavior in the case of higher gate dielectric biomolecules. Therefore, at $\frac{L_{gate}}{L_{nanogap}} > 0.5$, change in threshold voltage reaches saturation level, and a shift in threshold voltage is reduced. In this study, we have investigated higher threshold voltage variation (ΔV_{th}) observed at 10-nm cavity length compared to other cavity lengths obtained using Eq. 2[57] as described in Fig. 7a.

$$\Delta V_{th} = V_{th(\int_{bio}>1)} - V_{th(\int_{air}=1)} \tag{2}$$

where $(\varepsilon_{bio} > 1)$ represents the neutral biomolecule dielectric constant and $(\varepsilon_{air} = 1)$ is air or reference dielectric constant.

Figure 7b illustrates a higher drain off-current sensitivity $(S_{I_{off}})$ at higher cavity length and higher dielectric constant value because increasing biomolecules can increase gate electrostatic controllability, thereby lowering short-channel effects, reducing threshold voltage fluctuation and hot-electron effects. At smaller nanogap cavity length, the drain off-current sensitivity is almost the same among different biomolecules when nanogap cavity length is short, indicating that fewer biomolecules have no significant impact on the device performance.

Effect of Different Biomolecules on Device Surface Potential

An important output characteristic of FET-based biosensors is center/surface potential, which determines the threshold voltage variation, signifying the proposed device's sensitivity after biomolecules interact in the targeted cavity uniformly. Figure 8 clearly illustrates the effect of biomolecules on surface potential distribution along the channel for an *n*-type-triple hybrid metal GAA-JL-NWFET biosensor. The potential deforms under the cavity regions from lower to higher due to nanogap cavities present at the drain ends. Uniform surface potential emerges at the source end (as no nanogap cavity exists in that region), which indicates the impacts of dielectric constant. As the different biomolecules are immobilized in the cavity (near the drain end), channel region surface potential rises because the higher dielectric constant of the biomolecule impacts device operation for device performance modulation, as illustrated in Fig. 8. That means a higher inversion charge/channel was created, thus leading to an increased surface potential corresponding to the biomolecule dielectric constant even if input drain-source voltage (V_{SD}) is constant.

Figure 8 shows that the portion of the channel (drain side) over which different biomolecules were immobilized has lower to higher surface potential depending on the value of the dielectric constant interacting with the nanocavity region. In comparison, the uncovered gate portion of the device (source side) has lower and almost the same surface potential. So, we can conclude that the surface potential of the dielectric modulated THM-GAA-JL-NWFET varies

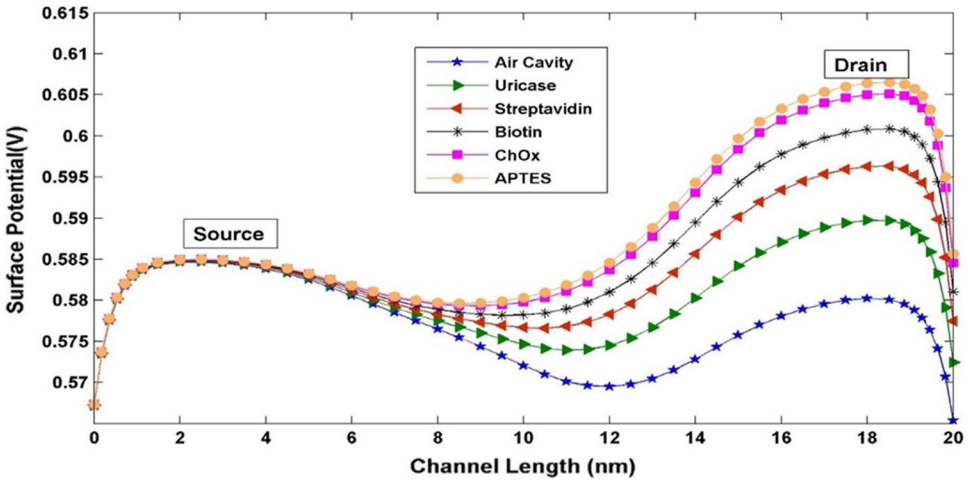

Fig. 8 Impact of different biomolecules on the surface potential for an n-type dielectric modulated triple-hybrid metal gate GAA-JL-NWFET at (V_{GS} = 1.0 V and V_{DS} = 0.0 5 V).

more with the nanogap cavity dielectric constant. It will be a better candidate for robust sensitivity of the device in the area of biomedical applications.

Effect of Biomolecules on Proposed Device Output Results Includes Transconductance, Output Conductance, Device Efficiency, Intrinsic Voltage Gain, and Output Resistance

In Fig. 9 both transconductance and output conductance are nonlinear parameters used to determine the analog performance of the proposed device. As illustrated in Fig. 9b, output conductance is higher under the weak inversion region than in the strong inversion region. This is because, in weak inversion regions, higher DIBL and SCEs affect carrier mobility along the channel, which affects the device performance and efficiency. As the dielectric constant of biomolecules (neutral) increases, voltage gain also increases at the strong inversion region due to inversion charge interaction on the channel as dielectric constant increases in this region and g_m increases while g_d decreases at a strong inversion region causing variation of intrinsic voltage gain $\left(\frac{g_m}{g_d}\right)$ as illustrated in Fig. 10a. The mathematical expression of intrinsic voltage gain (A_V) is given by Eq. 3, [58]

$$|A_V| = \frac{g_m}{g_d} \tag{3}$$

Figure 10b illustrates increased output resistance $\left(1/g_d\right)$ of the proposed device as the dielectric constant increases starting from a strong inversion region since higher dielectric constant increases carrier mobility through the channel and decreases the output conductance, thereby modulating gate controllability. So, it is possible to say that output resistance is an essential

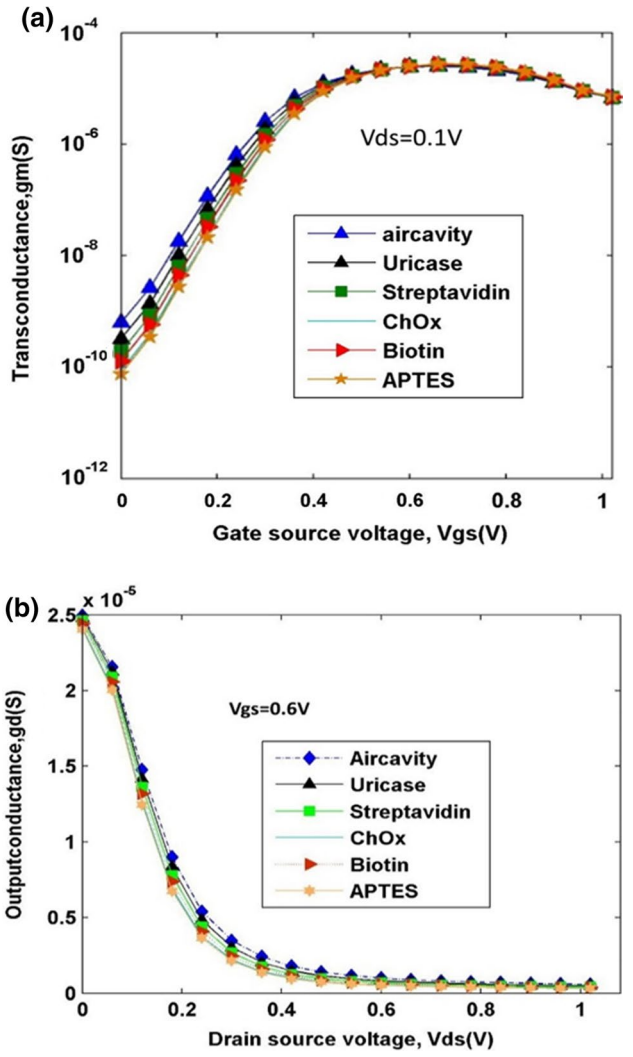

Fig. 9 Effect of biomolecules on (a) transconductance (g_m) log file and (b) output conductance (g_d) for an *n*-type triple hybrid metal GAA-JL-NWFET.

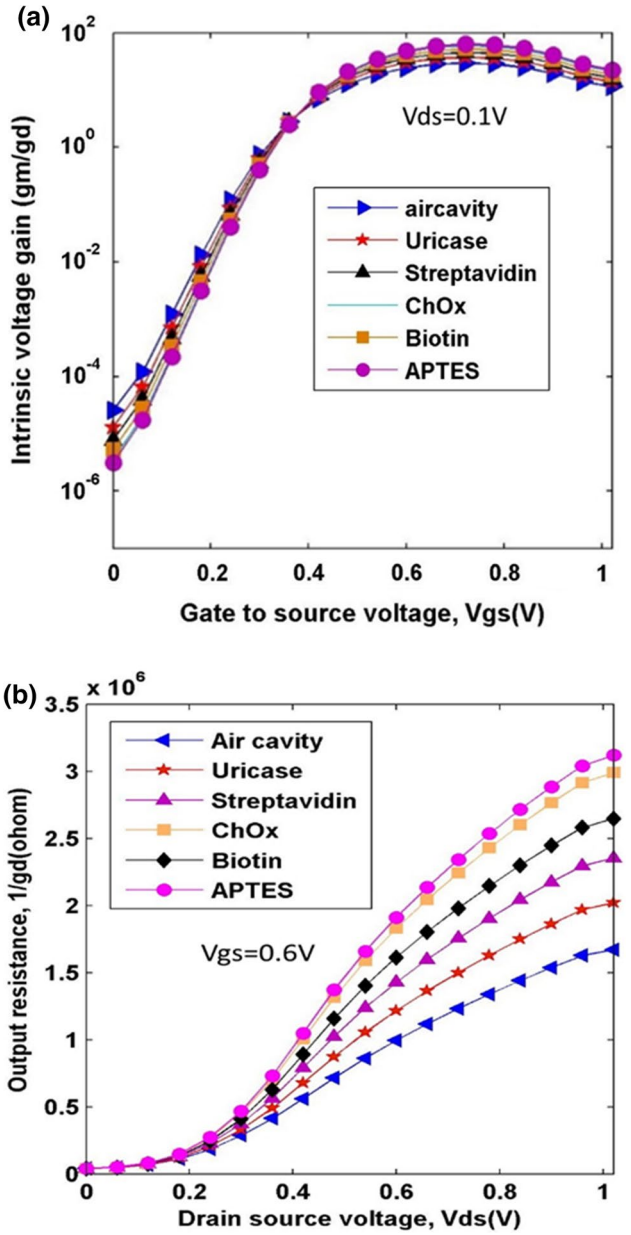

Fig. 10 Impact of different biomolecules on (a) intrinsic voltage gain $\left(\frac{g_m}{g_d}\right)$ log file and (b) output resistance $(1/g_d)$ for an *n*-type triple hybrid metal gate-all-around JL-NWFET.

characteristic of a transistor, in which its maximum R_{out} determines the maximum gain of the transistor. The output resistance $\left(R_{\text{out}}\right)$ of a transistor is given by Eq. 4.[59]

$$R_{\text{Out}} = \frac{1}{g_d} \tag{4}$$

Conclusion

In this work, the effect of an *n*-type dielectric modulated triple-hybrid metal gate-all-around junctionless nanowire transistor etched nanocavity to the immobilized biomolecule was presented and compared with unique and double-hybrid metal gate transistors to detect various diseases. The results were verified using the Atlas-3D device simulation tool. In both devices, electrical output characteristics, such as subthreshold slope, surface potential, drain off-current sensitivity $\left(S_{I_{\text{OFF}}}\right)$, switching ratio $\left(I_{\text{ON}}/I_{\text{OFF}}\right)$, transconductance $\left(g_m\right)$, output conductance $\left(g_m\right)$ and output resistance $\left(1/g_m\right)$, have been studied, including different biomolecules. We have observed lower leakage current and higher sensitivity results in a triple-hybrid metal gate than the available unique and double-hybrid metal GAA-JL-NWFET biosensor devices. For instance, leakage current using uricase biomolecule is 2.83×10^{-12}A for a double-hybrid metal gate and 4.50×10^{-13}A for triple-hybrid metal GAA-JL-NWFET. Another significant improvement of the triple-hybrid metal gate over the double-hybrid metal gate is device sensitivity, i.e., for the APTES biomolecule. Shifting the threshold voltage (ΔV_{th}) is 3.59×10^{-3} V for a double-hybrid metal gate and 3.19×10^{-2} V is for a triple-hybrid metal gate, so that 788.6% improvement was observed in the triple-metal gate compared with a double-hybrid metal gate. In addition to the biomolecule dielectric constant value, nanogap cavity length impacts the proposed device performance. The 10-nm cavity length has been investigated for better sensitivity, due to lower drain off-current and higher variation of threshold voltage shifting (ΔV_{th}) at this nanogap cavity length. Based on our investigations, we have concluded that the n-type triple-hybrid metal gate-all-around junctionless nanowire transistor with a 10-nm nanocavity length shows potential as a candidate for detection of neutral biomolecules (APTES, choli oxidase (ChO_x), streptavidin, biotin, and uricase) in the area of biomedical application. So, we can say our device can be used to diagnose and detect early, rapidly transmitted biomarkers of diseases such as breast and lung cancer (APTES) and uric acid in human blood serum (uricase).

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Conflict of interest The authors declare that they have no conflict of interest.

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TCAD Analysis and Modelling of Gate-Stack Gate All Around Junctionless Silicon NWFET Based Bio-Sensor for Biomedical Application

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***Abstract*--In the present day, metallic oxide semiconductor field-effect transistor-based bio-sensors have been frequently used for various purposes due to their low cost and other properties. In this work, high-k Gate-Stack gate-all-around junctionless Silicon Nanowire FET (SiNWFET) is proposed for neutral biomolecule species detection and enhanced the device performance by introduced gate stack and high metal gate work-function. In particular, neutral biomolecule species like Streptavidin, Uricase, APTES, Protein and ChO_x are considered in our study. Subthreshold slope, drain induced barrier lowering (DIBL), leakage current, transconductance, and shifting threshold voltage were considered for study the bio-sensor response. Effect of cavity thickness, cavity length, High-k dielectric thickness, and its length on the detection of the device has also become examined. The results in gate stack junctionless gate all around SiNWFET shows better performance in terms of DIBL, transconductance, leakage current, I_{ON}/I_{OFF} ratio and subthreshold slope. The high-k dielectric oxide (HfO_2) has been identified for chemical compatibility and thermal stability properties on metal oxide semiconductor transistor as a gate oxide to mitigate the gate tunneling current and short channel effects.**

Keywords: - ATLAS-3D, Bio-sensor, Gate-Stack Gate-all- around (GS-GAA), Junctionless, SiNWFET, Neutral-biomolecule

I. INTRODUCTION

The integrated circuit industry has shown a lot of technological progress since the past years. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a fundamental component of the Integrated Circuit (IC)[1]. The integrated circuit had advanced with increasing the number of on-chip transistors every generation and reducing the physical device size[2]. It has attracted many possibilities of novel structures in MOSFET devices.

With the development of Moore's law, the size of the transistor is decreasing so fast, led to various problems like mechanical tunneling, short channel effect (SCEs) and drain induced barrier lowering effect will be prominently related to a reduction of device size as channel length comparable to bandwidth [3][4]. It causes body-bias and electron tunneling into the gate or body/substrate and generally degrades device performance [5].

To overcome doping profile complexity, Junctionless MOSFET (JLMOSFET) without any pn-junction in the source-drain channel path is used for tiny channel length and thickness transistors [6]. It has a homogeneous and uniform doping profile throughout the source- channel-drain, unlike a junction-based (JB) inversion mode (IM) transistor[6][7].

In addition to Junctionless MOSFET, several devices related to different geometry have been proposed and validated experimentally [6][8]. Nowadays, junctionless multi-gate device structures are used due to their scaling capability, enhancing gate controllability, low cost, reducing short channel effects, and more controlling power over the channel region[10].

From many multi-gate MOSFET devices structures, Cylindrical Gate All Around Transistor device has preferred; due to its superior electrostatic control ability over the channel and transport property. In this device, the silicon channel is wholly surrounded by the metal gate to suppress short channel effects[11]. It is considered as one of the best multi-gate structures as it shows better gate controllability and excellent CMOS compatibility[12] [4].

Apart from device miniaturization, junctionless gate all around transistor has an increasing demand of establishing conventional clinical laboratories in rural, remote areas and military fields for the detection of biomolecular species [13] [14] and also overcome problems like short channel effects, hot-electron, and threshold voltage roll-off[15][16].

Reducing gate dielectric oxide thickness (< 2nm) increases mechanical tunneling and short channel effects, which can degrade the circuit operation and device performance [17][18]. Also, continually decrease gate oxide thickness led to direct tunneling[19] and excessive leakage currents in Si-based MOS Devices. The material hafnium Oxide (HfO_2) of the high-k dielectric family has better thermal stability, and large energy bandgap (5.8ev) as compared to silicon (1.1ev) can reduce problems related to short channel effect[20] and HfO_2 is also known as a better electrical insulator, and it is a stable, inorganic colorless solid compound[19][20]. Using HfO_2 in MOS device Modeling as gate Oxide, results in a better gate control over SiO_2[20].

In this paper, we have proposed, n-type junctionless gate stack gate all around silicon nanowire-based biosensor transistor using the method of gate material engineering (GME) at reduced gate oxide thickness (<2.0) using high-k material (HfO_2) as gate oxide above silicon dioxide layer with the metal gate having high work-functions to realize the impact of neutral biomolecule dielectric constant variation on transfer characteristics of the proposed device, such as I_{ON}/I_{OFF} ratio,

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shifting threshold voltage, and drain-current sensitivity of GS-GAAJLT for the first time.

II. DEVICE STRUCTURE AND SIMULATIONS

Table 1. Device parameter and structure

Parameters	GAAJLT	GS-GAAJLT
Channel length (nm)	20	20
Work function (eV)	4.8	4.8
Gate Oxide thickness (nm)	SiO_2=1.8	SiO_2=0.3 & HfO_2=1.5
Diameter of silicon film (nm)	10	10
Source/Drain & Channel Doping (N_D++)	$10^{19}cm^{-3}$	$10^{19}cm^{-3}$
Oxide Dielectric constant	SiO_2=3.9	HfO_2=20.0

Based on the above device specification, numerous simulations were carried out using atlas-3D device simulator tool for both GAA-JL-SiNWFET and Gate Stack GAA JL-SiNWFET structure. "Fig.1", shows (a) 3D-schematic and (a) 2D cross-sectional view of gate stack junctionless gate all around transistor with silicon nanowire channel thickness (t_{si}=10nm) and channel length (L= 20 nm). Source and drain lengths are considered to be 10 nm long. Both oxide thicknesses are 1.8nm (t_{ox} = 0.3nm + thigh-k = 1.5nm). Length of a metal Gate denoted by l_1 and L_2 represents SiO_2 and cavity lengths near to the metal gate, respectively, their sum equal to the channel length. In this study, neutral biomolecules are simulated by introducing their dielectric constant in the cavity region; such as choli oxidase (ChO_X =3.3), protein=2.5, uricase=1.54, streptavidin=2.1, and APTES=3.57. also, the air cavity is considered by introducing it's dielectric constant, ϵ =1.00 [12][21].

Fermi-Dirac Statics also used for simulation. Doping versus mobility can be demonstrated by concentration-dependent mobility (CONMOB)[22]; this model used to simulate band gap mobility in the high channel doping along the bandgap narrowing (BGN) model. Shockley–Read–Hall (SRH) model along the Boltz-man transport model has been used to account recombination of minority carriers within the drift or diffusion approximation in the semiconductor without impact ionization model. Carrier-carrier scattering mobility model (CCSMOB) has been used at higher carrier concentration. For perpendicular and parallel field-dependent mobility, the CVT mobility model has been used[22].

III. GATE OXIDE THICKNESS FOR GS-GAAJLT

Gate insulator equivalent oxide thickness (EOT) in this study obtained use "(1)", [23].

$$T_{SiO_2}=T_{high\text{-}k}\times\frac{\epsilon_{SiO_2}}{\epsilon_{High\text{-}k}} \qquad (1)$$

So that, 20nm channel length and 10nm diameter silicon film nanowire was warped by 0.3nm and 1.5nm thick Gate oxides, SiO_2 (ϵ=3.9) and HfO_2 (ϵ=20), respectively. Source /drain and silicon channel all are uniformly doped ($10^{19}cm^{-3}$) with n-type material/impurity.

A high work-function metal gate electrode (4.8eV) was used here to obtain a necessary threshold voltage, and it suppresses DIBLeffects and parasitic gate resistance by enhancing the drive current and transconductance. Gold (Au) electrode has a low electrical resistivity at 20 °C(2.44 μΩ cm) [24]. Because of these properties, it is often used in MOSFET device modeling as an electrode. So, we have used it as a gate electrode in our device structure.

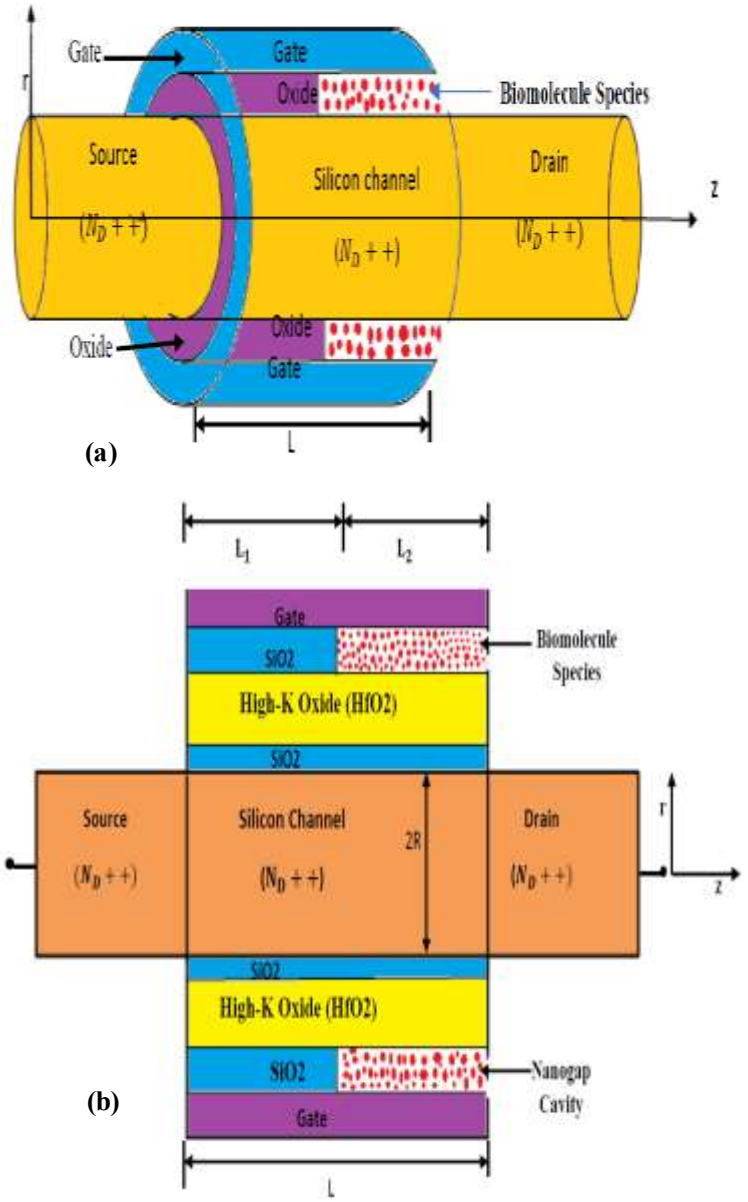

Fig.1 (a) 3D schematic Structure and (b) 2D cross-sectional view with cavity region of gate stack junctionless GAA-SiNWFET.

IV. DEVICE CALIBRATION

To validate our work, the models applied to the device simulation for GAAJLT[11] were applied to GS-GAAJLT. The calibration methods used in this simulation are

demonstrated in "Fig.2", by changing the dielectric constant in the cavity region, neutral biomolecules can be studied in both GS-GAAJLT and GAAJLT device structure.

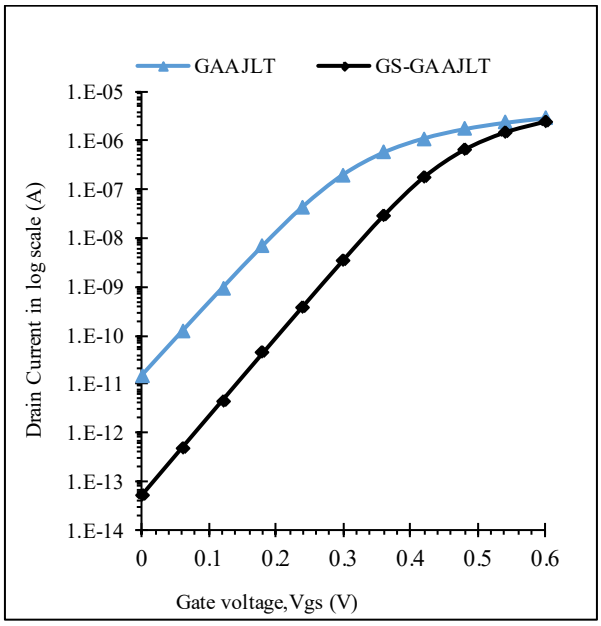

Fig.2. Calibration simulation results of the two devices without a cavity region at V_{DS}= 0.1V.

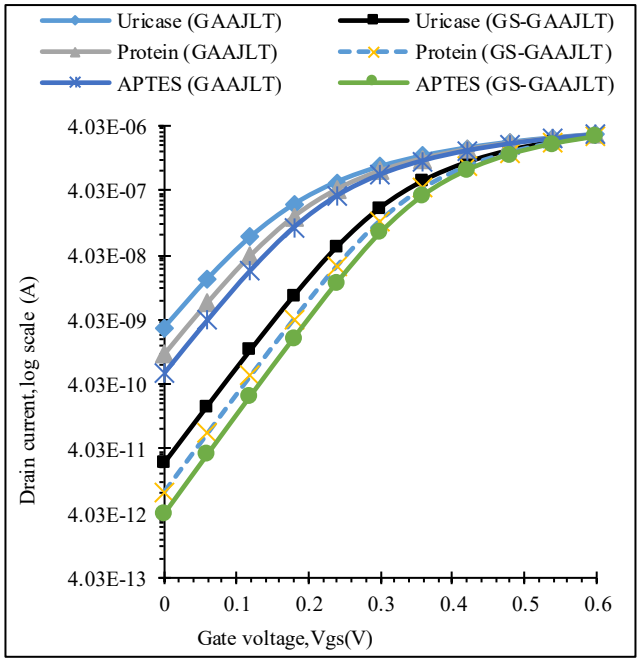

Fig.3. Drain current transfer characteristics of neutral biomolecule species in both devices at V_{DS}= 0.1V.

As we have seen from figure 2 and 3, in both cases I_{OFF} is lower under GS-GAAJLT than GAAJLT. The reason is that hafnium oxide (HfO_2) produces high gate capacitance with a neutral biomolecule, which leads to more drive current, I_D thereby reducing leakage current, DIBL, SCE, and SS in GS-GAA-SiNWFET[25]. Gate dielectrics of SiO_2 is used to make compatible HfO_2 dielectric in the GS-GAAJLT. Since, HfO_2 is a useful tool to improve electron transport efficiency and uniformity of electric field distribution in the channel region[19][26]. Also, HfO_2 suppress the fringing electric field, resulting in an increase in on-state current in GS-GAAJLT[27].

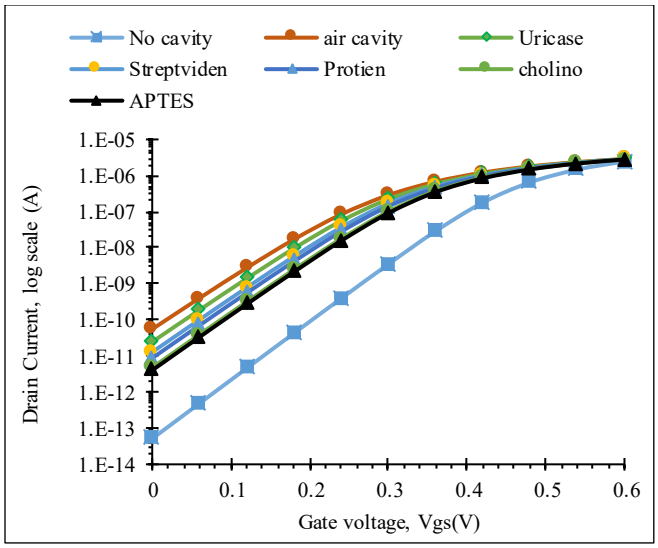

Fig. 4. Drain current transfer characteristics of junctionless gate stack gate all around bio-sensor SiNWFET at V_{DS}= 0.1V.

When a cavity region is filled by target biomolecule dielectric constant, drain ON and OFF current changes are observed. The result shows that, as neutral biomolecule dielectric constant increases, both I_{ON} and I_{OFF} -currents vary. But the shift in OFF-current is more significant than the change in ON-current due to the presence of neutral biomolecules in the nanogap cavity. In this case, OFF-current shows higher sensitivity than ON-current because the shift/change in the dielectric is more effective below the threshold voltage so that the new figure of merit $S_{I_{OFF}}$ use "(3)", has been introduced to study device sensitivity.

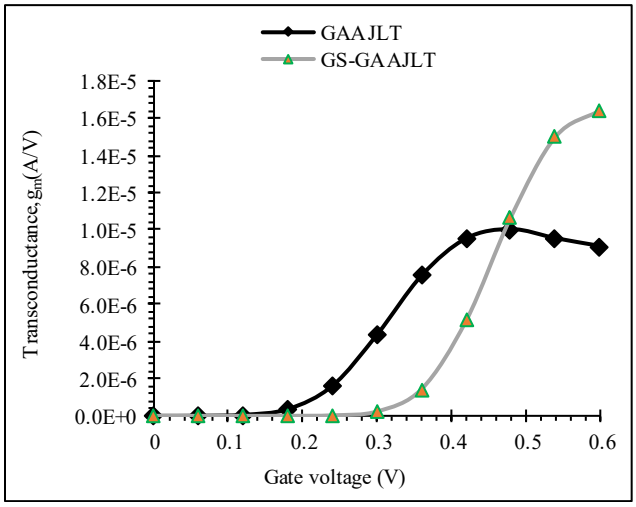

Fig.5. Transconductance variation(g_m) with V_{GS} for both device at V_{DS}=0.1V.

"Fig.5", Demonstrates the comparison of transconductance characteristics in both devices, GS-GAAJLT shows an increase in g_m by 79.63% at V_{DS}=0.1V and V_{GS}=0.6V without cavity region in both devices. The charge density created by HfO_2 in the GS-GAAJLFET shows improved drain current and transconductance[20], thereby reducing hot carrier's effects.

V. Result and Discussion

A) Drain induced barrier lowering

Due to different gate oxide dielectrics and layer structure, the extracted results are different in both devices. High-k gate oxide (HfO_2) in GS-GAAJLT reduces hot-carrier effects, SCEs, and velocity saturation[27]. And also reduces DIBL; it can be obtained use "(2)",[23].

$$DIBL=\frac{\Delta V_{th}}{\Delta V_{DS}} \qquad (2)$$

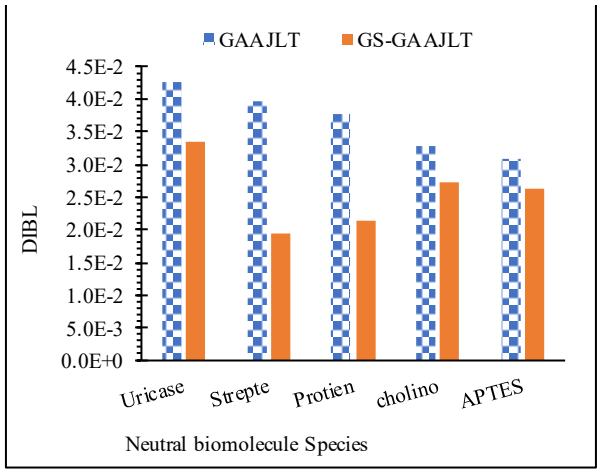

Fig.6. Comparison of DIBL in GS-GAAJLT and GAAJLT at V_{D1} and V_{D2}=0.1V and 3V, respectively at (V_{GS}=0.6V& V_{DS}=0.1V).

B) Subthreshold slope (SS)

The subthreshold slope can be defined as the reciprocal of the slope of the log (I_{DS}) vs. V_{GS}, and it should be small as possible since it determines the amount of voltage swing necessary to switch a device from its "OFF" state to its "ON" state[28]. Fig.7.Illustrates the variation of subthreshold slope for different biomolecule species in both devices. For instance, at APTES, neutral biomolecule SS in GS-GAAJLT is 63mV/decade while 73mV/decade is in GAAJLT. The reason is that mobility (electron and holes) transport efficiency of the GS-GAAJLT device improved by HfO_2[20][21] and reduction of bandwidth and SCEs in the channel.

C) Leakage current

"Fig.7", illustrates variation of leakage current and subthreshold slope for different biomolecule species in both devices. For instance, (without cavity region), the OFF-current is decreased by $3.42x10^{-3}$ times in GS-GAAJLT. That means, extracted values OFF-current in both GAAJLT and GS-GAAGJLT are $1.5x10^{-11}$ and $5.13x10^{-14}$ Ampere respectively. In general, when the neutral biomolecule is present in the cavity region near to HfO_2 gate oxide, gate control is improved incredibly leads to an increase of gate capacitance, reduces threshold voltage roll-off[14], and reduces short channel effects in GS-GAAJLT.

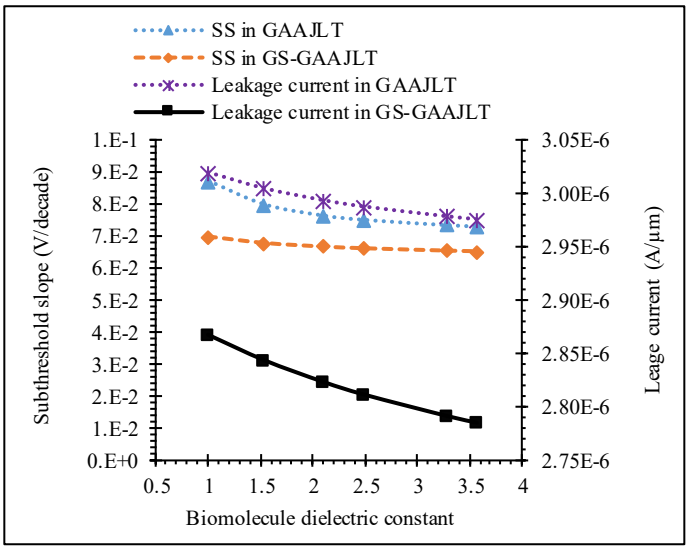

Fig.7. Effect of biomolecule species on subthreshold slope and leakage current for both devices at (V_{GS}=0.6V& V_{DS}=0.1V).

D) Switching (I_{ON}/I_{OFF}) ratio

"Fig.8", demonstrates higher switching (I_{ON}/I_{OFF}) ratio in gate stack gate all around junctionless silicon nanowire transistor. This proves that High-k gate oxide controls short channel effects in the gate stack junctionless gate all around transistor compared to GAAJLT. We examine that, OFF-current decreases in Hafnium oxide gate device than SiO_2 device due to high mobility carries and low bandwidth in HfO_2 gate oxide [19][23] transistor.

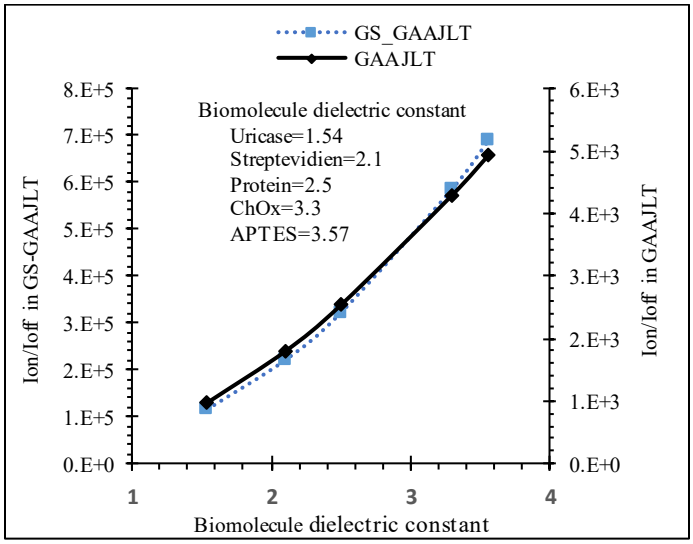

Fig.8. Effect of biomolecule species on switching (I_{ON}/I_{OFF}) ratio on both devices at (V_{GS}=0.6V& V_{DS}=0.1V).

VI. The Sensitivity of Neutral Biomolecule Species

A) Variation of Sensitivity with I_{OFF} ratio ($S_{I_{OFF}}$)

Using different biomolecule dielectric constants in the cavity region, and changing the cavity thickness and length, the sensitivity of the devices was studied. The result shows that $S_{I_{OFF}}$ is increased by 96% in GS-GAAJLT than GAAJLT using APTES neutral biomolecule species in the same condition, this is the effect of hafnium oxide (HfO_2) gate material, and it is more demonstrated by "Fig. 9,10 and 11". Sensitivity ($S_{I_{OFF}}$) of the device is obtained use "(3)" [11],

$$S_{I_{OFF}} = \frac{I_{off}(\text{With Biomolecule Species})}{I_{off}(\text{Without Biomolecule Species})} \Big| \text{at } V_{gs}=0 \qquad (3)$$

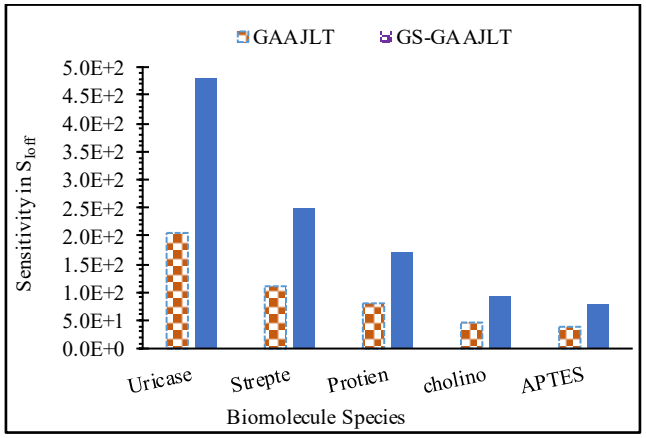

Fig.9. Effect of biomolecule Species on drain-off current sensitivity parameter in both devices at (V_{GS}=0.6V& V_{DS}=0.1V).

Variation of sensitivity is demonstrated by "Fig.12", when the nanogap cavity increases from 0.5nm to 1.5nm; due to large number of neutral biomolecules present in the nanogap cavity region. Increasing the nanogap cavity thickness leads to a higher number of neutral biomolecules to be settled in the nanogap cavity. So, the effect of biomolecules on the device performance is enhanced, and its sensitivity increases as a result of a high-k gate oxide material.

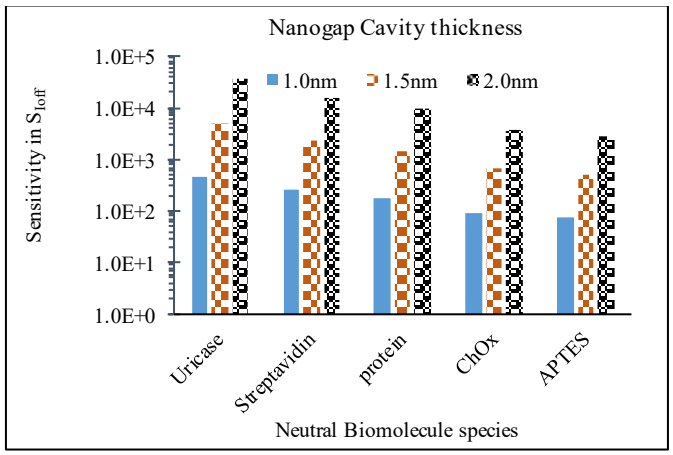

Fig.10. Effect of biomolecule species on drain OFF-current sensitivity parameter in GS-GAA-JLT at (V_{GS}=0.6V& V_{DS}=0.1V).

B) Variation of Sensitivity with shifting threshold Voltage

The ΔV_{th} increases with the biomolecule dielectric constant because the gate voltage exerts higher potential on the channel barrier through the capacitive coupling effect of the neutral biomolecule species and reduces threshold voltage roll-off and mechanical tunneling[29].

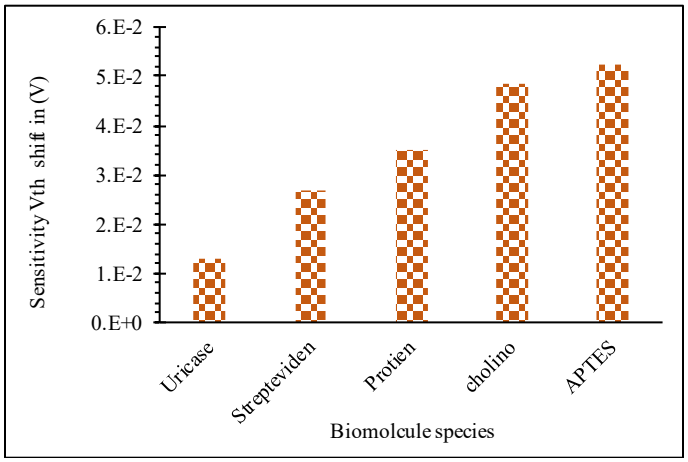

Fig.11. Threshold voltage shifting with neutral biomolecules in the GS-GAA-JLT device at (V_{GS}=0.6V& V_{DS}=0.1V).

"Fig. 11 and 12", demonstrates, shifting threshold voltage depends on high-k dielectric constant, neutral biomolecule dielectric constant, and nanogap cavity thickness. Both threshold voltage shifting and I_{OFF} ratio are used to detect neutral biomolecule species[11][29]. Sensitivity of the device in terms of shifting threshold voltage (ΔV_{th}) can be obtained use "(3)",[29],

$$\Delta V_{th} = |V_{th}(\epsilon_{bio}) - V_{th}(\epsilon_{air})| \qquad (3)$$

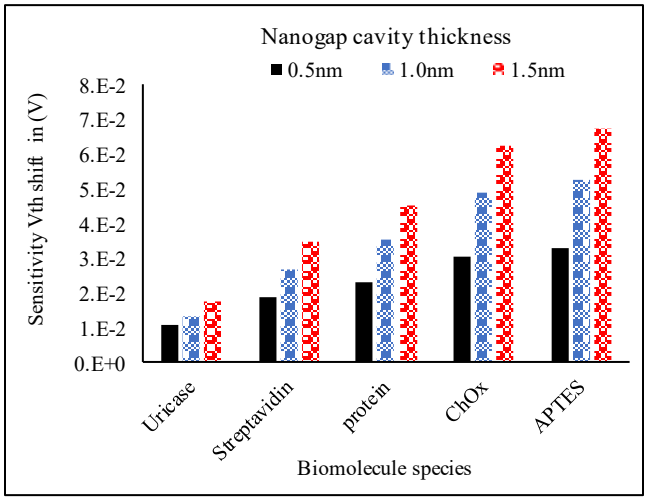

Fig.12. Threshold voltage shifting with biomolecules along with cavity thickness in GS-GAAJLT at (V_{GS}=0.6V& V_{DS}=0.1V).

VII. CONCLUSION

In this paper, the sensitivity of junctionless gate stack gate all around silicon nanowire field-effect transistor for detection of neutral bio-molecules species has been studied. Transfer characteristics such as DIBL, drain current, transconductance, subthreshold slope also examine in the study. The effect of cavity thickness and length of the device also observed. The result shows that electrical characteristics, i.e., subthreshold slope, leakage current, and DIBL, are lower in GS-GAAJLT. Transconductance and switching (I_{ON}/I_{OFF}) ratio shows better results in gate stack gate all around junctionless transistor. So that I_{OFF} ratio has been taken as a sensing metric for the detection of neutral biomolecule species. Sensitivity in terms of I_{OFF} ratio in GS-GAAJLT using APTES neutral biomolecule in both devices in the same condition is improved by 96% than GAAJLT in our study. We can conclude that GS-GAA-JL-SiNWFET based biosensors can be used for effective diagnosis of biomarker diseases such as Ebola virus[30], gamma-Aminobutyric acid (GABA)[31] and breast cancer[32][33][26].

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Interface Trap Charge Analysis of Junctionless Triple Metal Gate High-k Gate All Around Nanowire FET-Based Biotin Biosensor for Detection of Cardiovascular Diseases

Mekonnen Getnet Yirak and Rishu Chaujar

1 Introduction

Recently, the primary area of research interest is reduced semiconductor device size to satisfy the need for smaller integrated circuits (ICS) with the same functionality and increase the number of ICs in a single chip for better device performance [1]. As the size of technology is continually decreasing, the number of transistors in a single chip and transistors operation speeds are increases [2]. However, hugely scaling down device dimensions arises various problems the so-called short channel effects (SCEs), such as mobility degradation, threshold voltage roll-off, low on-current, high off-current, hot carrier, and impact ionization effect, parasitic resistance/capacitances, DIBL, and a substrate with defects, are worsening to achieve improved device performance with better reliability [3, 4]. Another problem of CMOS transistor is p–n junction related problem, which requires expensive fabrication techniques [5, 6] due to diffusion of impurities between p- or n-type drain/source region and n- or p-type body region pose great difficulty in the production of short channel/small scale devices. To continue Si CMOS device scaling, down to ultra-small device dimension, and to suppress device scaling-related problems, different approaches have been examined. For instance, a novel multi-gate structure such as double metal gat or surround gate MOS [7], replacing SiO_2 gate oxide by high-k dielectric material [8, 9], gate engineering, metal gate rather than polysilicon gate [10], and junctionless transistors having uniform doping profile from source to drain through the channel region [11] have been designed. Effective oxide thickness (EOT) can be scaled down to an ultra-small device dimension using a high-k gate dielectric material without increasing gate tunneling current [12].

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Similarly, replacing the polysilicon gate with a metal gate electrode (MG), depletion effect caused by the polysilicon gate is reduced [13]. Replacing polysilicon gate by metal gate electrode reduces parasitic capacitance and depletion effects caused by a polysilicon gate. But impact of interface charges trapped at buried oxide/channel interfaces due to hot carrier effects carried by the fabrication process, plasma etching, and high electric field effect along with ultra-small device dimension, arise defects/impurities or damage the gate oxide, are not well addressed. These will be serious issues on device performance [14–16], and Large traps at the interface of oxide/channel alter device electrostatics. Also, the impact of interface trap charges on the performance of junctionless surrounding gate all around nanowire-based biotin biosensor is not reported [17]. NWFET-based biosensor has become a primary focus for many researchers for the following reasons; these are easy scalability, cost-effective, label-free for detection, compatibility with bulk CMOS, high sensitivity, fruitful on-chip integration, less response time for detection and lower fabrication cost, and low power consumption [18–20]. The operation of biosensor technology lies in the fact of the successful translation of biological properties of the biomolecule to equivalent electronic properties. In case of NWFET-based biotin biosensor, the same action has been done by first finding the same electronic properties in dielectric constant and charge density and studding electrical parameters, such as threshold voltage, drain current, transconductance, surface potential, corresponding to the absence and presence of biomolecules in the NWFET-based biosensor. Critical challenges that enact the sensitivity of FET biosensors are DIBL [16], hot carrier effects, short channel effects, as a result of narrow the imperfect interface region on oxide/channel interface due to high electric field in case of short channel device [20].

In this article, n-type junctionless (JL) TM-high-k GAA—NWFET-based biotin biosensor has been proposed for the first time to study the impact of interface trap charges on device sensitivity by considering interface charges near or at the Si-SiO_2/channel, as shown in Fig. 1b.

2 Device Structure and Simulations

The device structure of n-type triple metal high-k gate all around junctionless NWFET-based biotin biosensor with interface trap charge used in this work has been illustrated in Fig. 1. Here, L_1(6 nm), L_2(8 nm), L_3(6 nm) are the lengths of gate one, gate two, gate three, respectively, and L_4 is the length for both nanogap cavity and silicon dioxide (SiO_2), which are near to drain and source end respectively is (10 nm), L is channel length (20 nm). T_1, T_2, T_3, and T_4 are the thickness of metal gate, nanogap cavity, hafnium oxide, and interface (SiO_2) oxides, respectively, and 2R is the diameter of the channel. A 0.3 nm thickness of SiO_2 interface layer is considered between hafnium oxide and silicon film to create more compatible hafnium oxide with silicon film. The three gate materials are G_1, G_2, and G_3 having different work function denoted by $\Phi_{G1} = 4.86$, $\Phi_{G2} = 4.96$ and $\Phi_{G3} = 4.50$,

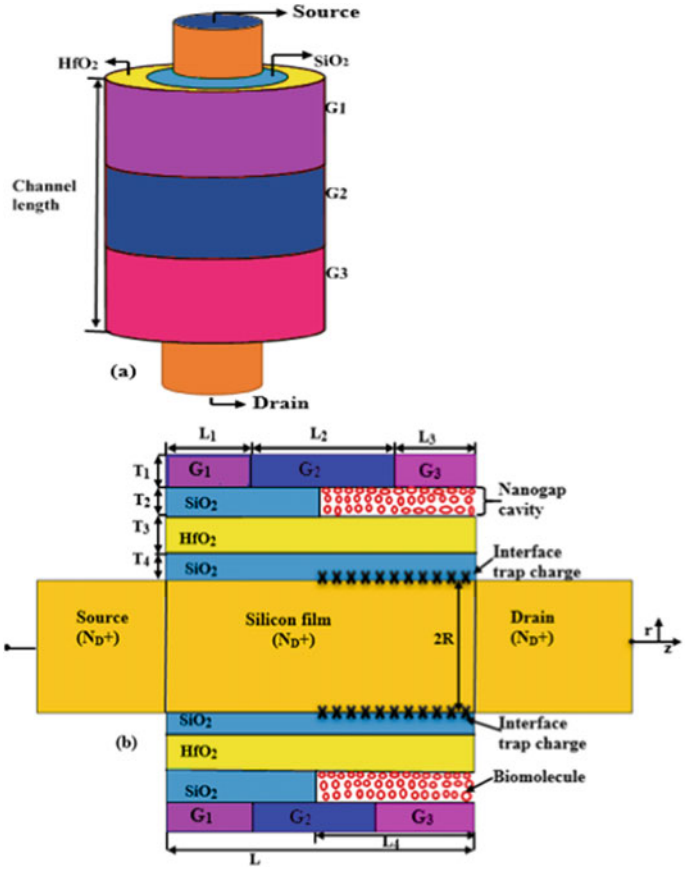

Fig. 1 **a** 3-D schematic structure and **b** 2-D cross-sectional view with cavity region for n-type triple metal gate high-k GAA-JL-NWFET

respectively. The work function (Φ_{G1}) near to the source is used to control electron saturation velocity, the work function (Φ_{G2}) between source end and drain end is used to control potential profile along the channel, which intern reduces SCEs and lower work function near to drain (Φ_{G3}) is used for screening effects [3–5]. HfO_2 is used to over com quantum mechanical tunneling [6]. The nanogap cavity region is used as a detecting site in which the target biomolecules are assumed to be uniformly immobilized in the nanogap cavity region. Biotin ($\epsilon = 2.63$), and air ($\in = 1$) cavity regions are considered by introducing their dielectric constant material [8]. Interface trap charge (ITCs) ($N_f = \pm 5 \times 10^{16}\,cm^{-2}$) and neutral charge ($N_f = 0$) are considered interchangeably for all simulations (see Table 1).

In this work, electrical properties of triple metal gate high-k GAA-junctionless NWFET device structure have been characterized using the "atlas 3-D" device simulator tool. Concentration-dependent mobility (CONMOB) [9] model was used

Table 1 Proposed device structural parameters

Parameters	TG-GAA-JL-NWFET		
Channel length (nm)	20		
Gate oxide thickness (nm)	$HfO_2 = 1.5$ and $SiO_2 = 0.3$		
Oxide thickness near to the source (nm)	$SiO_2 = 1$		
Oxide length near to the source (nm)	$SiO_2 = 10$		
Nanogap cavity length (nm)	10		
Source/Drain thickness (nm)	10		
Source/Drain length (nm)	10		
Nanogap cavity thickness (nm)	1		
The diameter of silicon (nm)	10		
Interface trap charges (ITCs)	$\pm 5 \times 10^{12}\,cm^{-2}$		
Source/Drain and channel doping (N_D+)	$10^{19}\,cm^{-3}$		
Oxide dielectric constant	$SiO_2 = 3.9$ and $HfO_2 = 25.0$		
Gate Work functions (eV)	$\Phi_{G1} = 4.86$	$\Phi_{G2} = 4.96$	$\Phi_{G3} = 4.50$

to simulate bandgap mobility within the high channel doping along the bandgap narrowing (BGN) model. Shockley–Read–Hall model along with the Boltzmann transport model was used to account recombination of minority carriers [9]. Carrier–carrier scattering mobility model (CCSMOB) was used at higher carrier concentration. For parallel and perpendicular field-dependent mobility, CVT model has been used [10]. Carrier transport equation can be solved using Gummel's and Newton's numerical methods. But models of quantum mechanical effects have not been invoked in this simulation because the radius of the silicon film is not less than 4 nm [11]. Interface charge density ($N_f = \pm 5 \times 10^{12}\,cm^{-2}$) has been introduced as localized charge at the Si–SiO_2 interface near to drain end.

3 Results and Discussion

In this study, output characteristics of triple metal gate high-k gate all around junctionless nanowire FET-based biotin biosensor has been examined by incorporating interface trap charges at Si–SiO_2/channel interface.

3.1 *Effect of Different ITCs on Drain Current*

Figure 3 demonstrates the simulated results of I_D-V_G transfer characteristics on log scale at $V_D = 0.05$ V with different interface trap charges, including air and biotin biomolecule for a triple metal gate. It is clear that higher leakage current for positive interface trap charges (ITCs) is observed compared to negative ITCs; this is because negative ITC reduces short channel effects and hot carrier effects while positive ITCs reduces charge carriers within the channel raises depletion layer to get thicker across the reverse junction that permits the flow of charge carriers in off-state. For biotin biomolecule, lower leakage is examined compared to air; the reason is that biotin biomolecule acts as high-k dielectric material and improves gate electrostatic control [13]. For instance, I_{OFF} for biotin biomolecule at ($N_f = \pm 5 \times 10^{12}$ cm^{-2}) are 3.12×10^{-12} A and 4.07×10^{-16} A for positive and negative interface trap charge, respectively, at $V_{GS} = 0$ and $V_{DS} = 0.05$ V. JL-NWFET-based biotin biosensor is the device that uses biological molecules (biotin) to detect the presence of chemicals. Biotin biomolecule in FET device is an interface condition in the boundary as the link between the oxide of the FET and the analyte (an aqueous solution) which contains the bio-sample for purification and detection of various biomolecules and it is a water-soluble vitamin that functions as a prosthetic group in carboxylation reactions. In addition to its detection, biotin has multiple roles in gene regulation [14, 15]. Figure 2 demonstrates/validates the calibration simulation results of our proposed device.

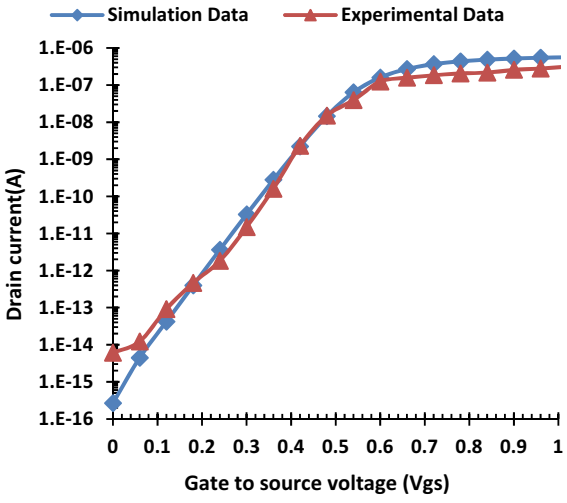

Fig. 2 Simulation and experimental calibration results [12] for n-type triple metal gate high-k GAA-JL-NWFET without nanogap cavity and interface charges

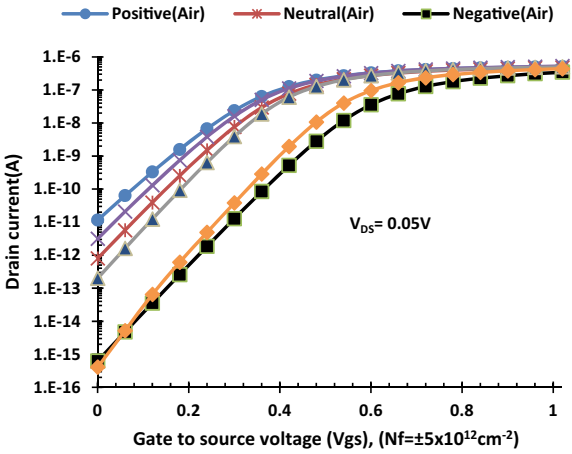

Fig. 3 Impact of interface trap charges on I_D-V_G, with air and biotin biomolecule for n-type triple metal gate high-k gate all around junctionless NWFET

3.2 *Impact of Interface Trap Charges on Switching Ratio and Leakage Current*

Figure 4 illustrates the variation of (a) switching ratio (b) leakage current, with different interface trap charges for n-type triple metal gate high-k GAA-JL-NWFET at $V_{DS} = 0.05$ V and $V_{GS} = 1.0$ V with air and biotin biomolecules. It is clear that higher leakage current and lower switching ratios are examined for air compared to biotin biomolecule. The reason is that the lower gate dielectric constant raises gate parasitic resistance and short channel effects. At higher dielectric constant (biotin) biomolecule, higher switching ratio and lower leakage current are explored with negative interface trap charges (ITCs) compared to positive and neutral ITCs due to an increasing number of mobility carriers across the channel by negative ITCs, thereby reducing DIBL [16, 17].

3.3 *Impact of Interface Trap Charges (ITCs) on Total Current Density*

Figure 5 demonstrates higher variation of total current density in the case of biotin biomolecule compared to air in the presence of ITCs. Example, ($N_f = \pm 5 \times 10^{12}$ cm^{-2}) total current density for biotin ($\epsilon = 2.63$) are 8.44×10^5 A/cm^2 and 2.39×10^5 A/cm^2 for positive and negative ITCs, respectively, and air ($\epsilon = 1.0$) are 6.06×10^5 A/cm^2 and 1.32×10^5 A/cm^2 for positive and negative ITCs, respectively. The improved total current density of biotin biomolecule in comparison to air is 39.3% and 81% for positive and negative ITCs, respectively. This variation of overall current density indicates that our proposed device can detect biomolecules.

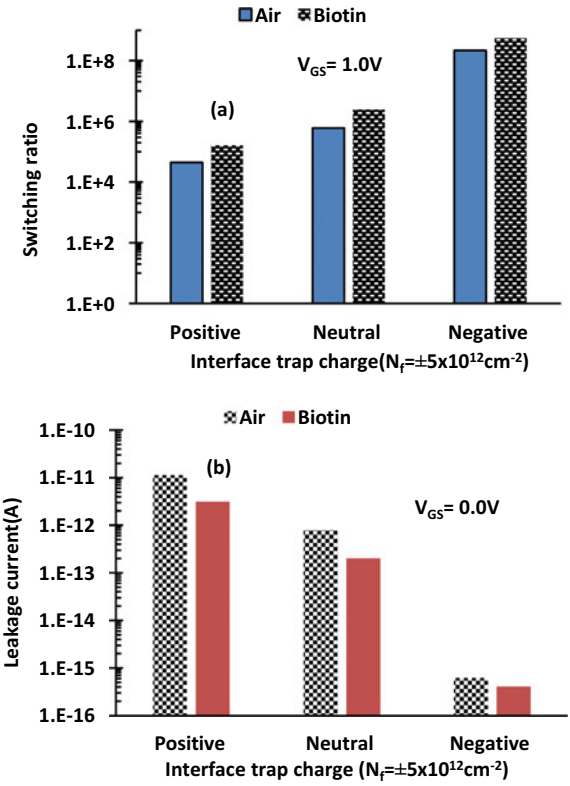

Fig. 4 Variation of **a** switching ratio **b** leakage current, with interface trap charges for n-type triple metal gate high-k GAA-junctionless NWFET

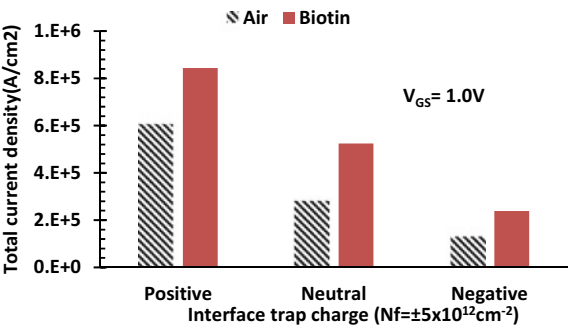

Fig. 5 Variation of total current density at drain end with ITCs for n-type triple metal gate high-k GAA-JL-NWFET

3.4 Effect of Interface Trap Charges (ITCs) on Sensitivity ($S_{I_{OFF}}$)

Figure 6 illustrates a higher drain-off current ratio ($S_{I_{off}}$) for positive and neutral than negative interface trap charges (ITCs); this is the result of higher leakage current due

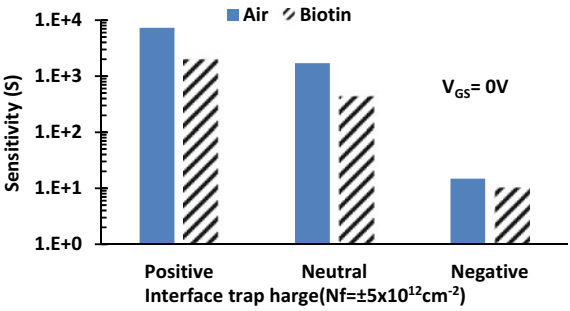

Fig. 6 Variation of drain-off current ratio with interface trap charges for n-type triple metal gate high-k GAA-JL-NWFET

to positive and neutral interface trap charges (TCs) led to higher drain-off current ratio ($S_{I_{off}}$) than negative ITCs; because of SCEs and DIBL effect experienced by positive and neutral interface trap charges (ITCs). For instance, at higher dielectric constant (biotin), drain of current ratio is smaller than that of lower dielectric constant (air); this indicates that high dielectric materials enhance gate electrostatic control, thereby reduces gate tunneling current. Sensitivity ($\mathbf{S_{I_{off}}}$) or drain-off current ratio is given by Eq. (1)

$$S_{I_{off}} = \frac{I_{off}\text{ (with biomolecule Species)}}{I_{off}\text{ (without biomolecule Species)}} \Big| \text{at} V_{gs} = 0 \tag{1}$$

3.5 *Impact of ITCs on the Device Transconductance*

Transconductance (g_m) of a MOSFET characterizes its analog performance, and it is given by Eq. (2) [19] at constant drain-source voltage.

$$g_m = 2\left(\frac{I_{D\,ON}}{(V_{GS\,ON} - V_{th})^2}\right) V_{eff} \tag{2}$$

where (V_{GSON}, I_{DON}) is a fixed point on the curve when the device is ON, and V_{eff} is effective (overdrive) or excess gate voltage, which is the difference between the gate to source bias voltage and the threshold voltage, i.e., ($V_{eff} = V_{GS} - V_{th}$). Transconductance ($g_m$), also known as mutual conductance or transfer admittance, is a property of certain electronic components and is used to analyze MOSFET amplifiers.

As shown in Fig. 7b, transconductance for negative interface trap charge (ITCs) is higher than positive ITC, due to reduced hot carrier and DIBL effects in the presence of negative ITCs at strong inversion region. Example, at $V_{GS} = 1.0\,V$ and $V_{DS} = 0.6\,V$ for $N_f = \pm 5 \times 10^{12} cm^{-2}$ of ITCs, 20.3, and 33.7% are enhanced/raised transconductance of the device for negative and positive ITCs when

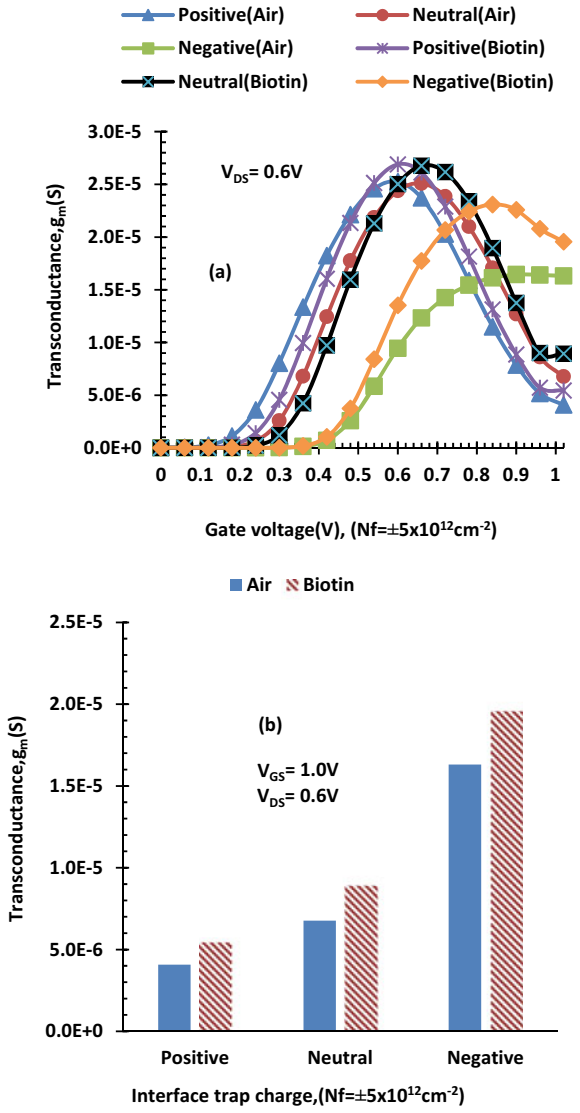

Fig. 7 Variation of **a** transconductance **b** transconductance at $V_{DS} = 0.6$ V with ITCs for n-type triple metal gate high-k gate all around JL-NWFET

biotin biomolecule immobilizes/interacts with the nanogap cavity region compared to the air cavity. So that biotin biomolecule at negative interface trap charges delivers higher device gain (amplification) and more drive current experience lower SCEs [20] due to increased carrier injection by negative (interface trap charges) ITC across the channel.

4 Conclusion

In this study, the effect of different interface trap charges (ITCs) on transfer characteristics of TG-high-k-GAA-JL-NWFET-based biotin biosensor has been examined. These different ITCs cause the change in total current density, switching ratio, transconductance, leakage current, and drain-off current ratio when air and biotin biomolecule immobilize interchangeably on the nanogap region. In this study, drain-off current ratio is taken as a sensing metric to study the impact of ITCs on device sensitivity. In our research, for biotin biomolecule, enhanced drain-off current ratio (S) is 72.9% for positive and 29.7% for negative ITCs compared to air. The result indicates that biotin biomolecule shows a strong dependency on negative ITCs for increasing output parameters like switching ratio, transconductance, drain-on current, and total current density. Finally, we have concluded, negative ITC has a positive impact on our proposed device performance compared to positive ITC. In our study, we have examined that biotin biomarker for the silicon-based device presents reactive amine groups on the silicon surface for detecting cardiovascular diseases.

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