DESIGN AND COMPARISION OF DIFFERENT DOMINO TECHNIQUES

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Submitted by:

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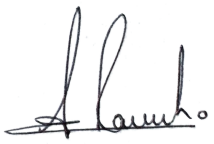
I, Anurag Ravish, Roll No. 2K19/VLS/04 student of MTech (VLSI Design and Embedded Systems), hereby declare that the project Dissertation titled "Design and Comparison of Different Domino Techniques" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.



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CERTIFICATE

I hereby certify that the Project Dissertation titled "Design and Comparison of Different Domino Techniques" which is submitted by Anurag Ravish, Roll No. 2K19/VLS/04 of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Date: 28-07-2021

SUPERVSOR

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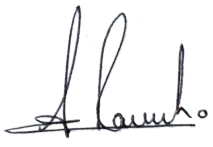

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ABSTRACT

Domino Logic gates are getting into the trend in designing the high-speed microprocessor due to their several advantages over static CMOS logic gates. The primary benefit of dynamic circuits incorporates speed and small chip region. But dynamic circuits also have several disadvantages such as huge leakage power dissipation and poor noise immunity. Power dissipation boosts drastically in high fan-in logic gates due to a rise in parasitic capacitance at the dynamic node. Owing to which the charging-discharging component of power dissipation amplifies, along with this noise margin of the logic gate also degrades. Many academics have put forward several compositions of domino circuits in order to tackle the problem of noise immunity and power dissipation.

In this work, different domino techniques have been studied and a new composition of domino circuit has been proposed. In the proposed design both evaluation and keeper circuitries have been modified to minimize power dissipation and improve noise immunity respectively without affecting delay. Basically, in keeper setup, two keeper transistors in series have been utilized instead of one as in standard domino logic circuit. While in evaluation setup a transistor in diode configuration has been utilized along with a mirror transistor and an evaluation transistor. All the circuits have been simulated on a cadence virtuoso platform in a 180nm technology node. Three performance parameters that are average power dissipation, unity noise gain (UNG), and the number of transistors used are calculated to justify the efficiency of the proposed domino design. Results show that the proposed domino circuit gives around 81.1% reduction in power dissipation and 56% improvement in noise immunity than conventional domino without footer transistor circuit.

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List of Symbols and Abbreviations

PLA	=	Programmable logic array
NMOS	=	N-channel metal-oxide-semiconductor
PDN	=	Pull-down network
CMOS	=	Complementary metal-oxide-semiconductor
t_{pLH}	=	Low to high propagation delay
t_{pHL}	=	High to low propagation delay
IC	=	Integrated circuits
NI	=	Noise immunity
PD	=	Power dissipation
PDP	=	Power delay product
CD	=	Conventional Domino
BTBT	=	Band to band tunnelling
PMOS	=	P-channel metal-oxide-semiconductor
DFD	=	Diode footed domino
HSD	=	High-speed domino
VCD	=	Voltage Comparison domino
CKCCD	=	Controlled keeper current comparison domino
LPD	=	Low power domino
SA	=	Sense amplifier
UNM	=	Unity noise margin

CHAPTER 1

INTRODUCTION

In recent times, the inclination has been observed towards dynamic circuits for designing high fan-in gates which are the elementary unit in modelling advanced microprocessors [1]. Other examples where dynamic circuits being used are flash memory, comparators, multiplexer, programmable logic array (PLA) [1], etc. In comparison to static gates, dynamic gates have numerous benefits for instance almost half the sum of transistors being utilised to model logic circuit as compared to static gate and evade static power dissipation. Dynamic circuits use a succession of the precharge and evaluation phase, with the addon of a clock signal. Although, there are several disadvantages also for instance poor noise margin and poor signal integrity with the rise in the number of inputs [1].

1.1DYNAMIC LOGIC

The elementary modelling of the NMOS dynamic logic gate is depicted in Fig. 1.1. In which PDN is designed in the same manner as NMOS-PDN in static CMOS gate. The working of dynamic circuits is sundered into two periods, being precharge and evaluation period which being decided by clock signal level (taken as CLK in Fig. 1.1) [2].

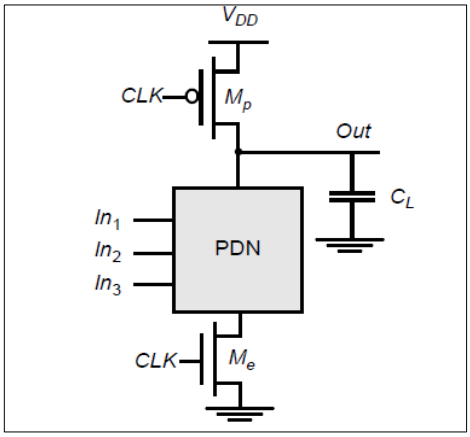

Figure 1.1: Dynamic circuit with n-type transistor PDN [2].

1.1.1 Precharge

CLK signal is at low in this phase, causing output node to precharge to logic high due to p-type precharge transistor (M_p). While n-type evaluation transistor (M_e) operating in cut-off

mode. Hence no path exists between the ground and out node. In this phase, static power dissipation is evaded due to the presence of transistor (M_e) [2].

1.1.2 Evaluation

CLK signal is at logic high in this phase, making the transistor M_p to operate in cut off mode while switching on transistor M_e. Depending upon the set of inputs and the structure of the PDN out node will be discharged conditionally. A small resistance path will occur between the ground and out node if at minimum one input is at logic high, which will discharge out node to logic low. PDN will remain deactivated in case no input is at logic high, hence logic high stored in output node capacitance C_L, during the precharge phase remain intact. Where C_L mathematical representation given by equation 1.1.

$$C_L = C_{junction} + C_{wire} + C_{input} \quad (1.1)$$

Where $C_{junction}$, C_{wire} and C_{input} are junction, wire, and input capacitances of fanout gate respectively. In this phase, the only probable path that exists between node OUT and source is to ground. If the OUT node based on input vector discharged to logic low, it will be charged in the next precharge phase only. Hence restricting the transitions of the input set to one. In dynamic circuits, the OUT node can achieve a high impedance position in the evaluation phase if all inputs are at logic low (means PDN is deactivated). Whereas, this is not the case for static circuits where a small resistance path always exists between the OUT node and either logic high or ground [2]. The edge voltage of dynamic inverter is equal to limit voltage (V_{Tn}) of n-type transistor in PDN [2].

1.2 SPEED AND POWER DISSIPATION OF DYNAMIC LOGIC

Enhanced performance and compact area are key improvements provided by dynamic circuits. A logic function could be realized with a fewer number of transistors indicates the reduction in output load capacitance. At the end of the precharge phase, the OUT node holds a logic high state. So, in the evaluation phase, if all inputs at logic low, the OUT node will maintain the state achieved in the precharge phase (hence, $t_{pLH} = 0$). Whereas, $1 \rightarrow 0$ transition of OUT node needs discharging of output load capacitance through PDN (hence, t_{pHL} is directly proportional to C_L and PDN's current plunging competencies). The existence of evaluation transistor in series with PDN degrades the performance of logic gate, due to further addition of series resistance. The serviceability of the logic gate won't be affected if the evaluation transistor is removed, although it would cause a rise in static power dissipation

and loss of speed. Conditional to the necessity, for instance, to model a gate with lower average power dissipation or with improved noise margin a dynamic circuit with and without evaluation transistor can be used respectively [1].

Dynamic circuits offer a substantial reduction in power dissipation, because for the following reasons:

- In dynamic circuits output load capacitance has been reduced significantly as fewer transistors are required to implement a given function.
- As Dynamic circuits allow a maximum of one transition in the evaluation phase, so chances of glitches reduced to zero.
- No contention between the supply voltage and ground as the precharge transistor operates in a cut-off mode in the evaluation phase [2].

1.3 SIGNAL INTEGRITY ISSUE

Better performance results can be achieved using dynamic circuits. Although, for the proper functioning of dynamic circuits few deliberations must be comprehended. Significantly below are fours problems that should be considered while designing dynamic circuits are [2]:

- Charge leakage
- Charge sharing
- Capacitive coupling
- Clock feedthrough

1.4 DOMINO LOGIC CIRCUIT

Domino logic circuit comprises of NMOS PDN same as in static circuit to implement a given function in series with a static CMOS inverter as portrayed in Fig. 1.2.

Operation

- In the precharge phase, the dynamic node is rushed to logic high via a precharge transistor, as a result, the output of the CMOS inverter will attain a logic low level.
- In the evaluation phase, PDN creates a path for the dynamic node to discharge depending upon the input set, as a result of that output of the CMOS inverter switches from logic low to a high level.

In case the output of one domino gate is input to other, in that case, it must be made certain that at the end of the precharge phase input set to domino logic gate are at a logic low level.

Only low to high transition must take place in the evaluation phase at inputs. The accuracy of the domino gate will be definite if only one low to high transition is made at the inputs in the evaluation time slot. As a result, two signal integrity issues that are charge distribution and leakage effects have been avoided. The existence of a static CMOS inverter improves noise margin significantly, due to two reasons: first, fan-out of the dynamic gate is now directed by small output resistance CMOS inverter, and second, this inverter lowers the capacitance of the output node by separating internal dynamic node and load capacitances [2].

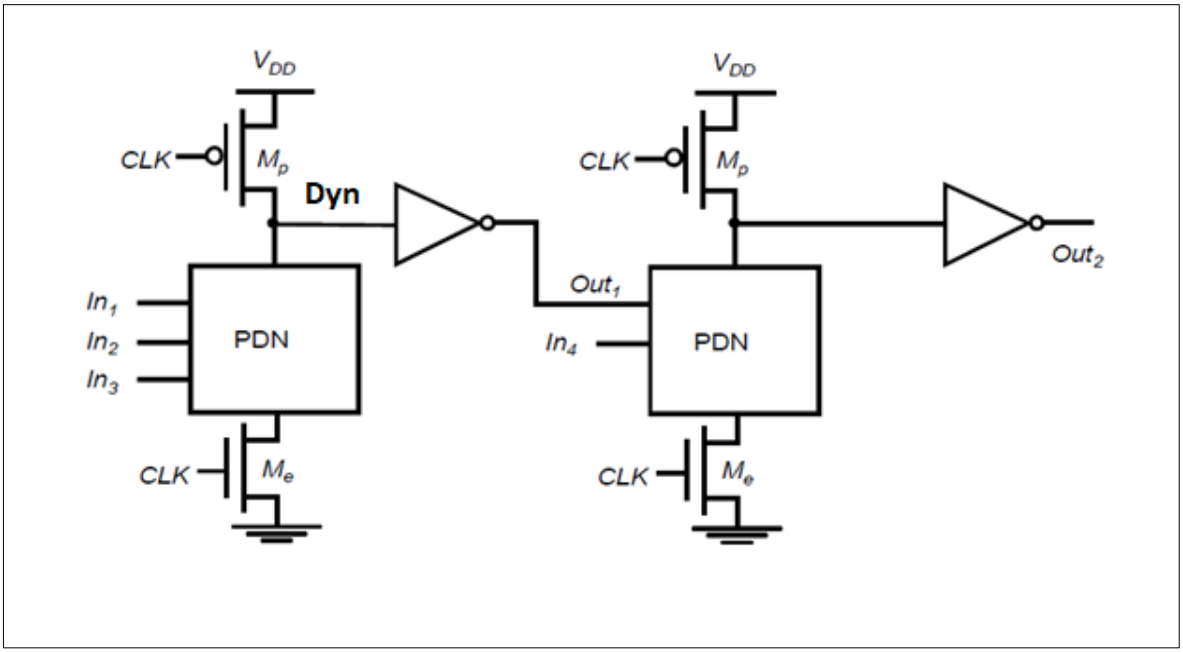

Figure 1.2: Typical domino logic gate [2].

Advantage

- As the only delay that exists is due to low to high transition at the output node (i.e., t_{pLH}), whereas $t_{pHL} = 0$. Therefore, high promptness in logic gates can be accomplished.

Disadvantage

- Only non-inverting output can be obtained while realizing a given function, as every domino gate is followed by a CMOS inverter.

1.5 OBJECTIVE

With the advancement in technology, a precipitous development has been seen in portable gadgets [3]. As a result, power dissipation in IC has been a topic of concern among

researchers. It has been seen domino circuits experience excessive process variation in performance and NI, alongside experiences excessive power dissipation as the count of input to logic gate grows [4][5]. To diminish this excessive PD, source voltage must be cut down with cut down of technology node, causing shortfall of performance. With the aim of overcoming this shortfall in performance threshold voltage (V_{TH}) of the transistor also needs to be cut down. Equation 2.2 expresses the rapid reliance of sub threshold current over the threshold voltage of a transistor, hence an exponential upsurge in spillage current occurs through cut down of edge voltage [3]. The mathematical expression of sub-threshold current articulated in equation 2.2 [6][7]:

$$I_{sub-threshold} = I_o(1 - e^{-\frac{V_{DS}}{V_T}})(e^{\frac{-V_{GS}-V_{TH}-\eta V_{DS}}{nV_T}}) \quad (2.2)$$

Where I_o is articulated in equation 2.3 [10]:

$$I_o = \mu_o C_{ox} \frac{W}{L}(n-1)V_T^2 \quad (2.3)$$

Here, V_{GS} and V_{DS} are the transistor gate to source and drain to source voltages respectively. Where threshold voltage (V_{TH}) of the transistor and thermal voltage V_T can be articulated as [7]:

$$V_T = KT/q \quad (2.4)$$

η denotes DIBL coefficient, n denotes sub-threshold swing coefficient of the transistor, μ_o denotes zero-bias mobility, C_{ox} denotes gate oxide capacitance, where width is termed as W and length is labelled as L for the transistor, correspondingly [7].

Subsequently, due to the rise in leakage current, leakage power dissipation ascends which directs to poorer NI (particularly in high fan-in logic gates) [4][5]. Therefore, sub-threshold current, performance, power dissipation, and NI have become the key parameters that must be taken care of while modelling high-end microprocessors [3].

Thus, to accomplish a noteworthy cut back in power dissipation, all the factors of PD must be reduced. Preferably these factors should be uncovered which influences PD in high-end microprocessors and embedded designs in modern technology the most. In this case, PD of logic gates is the sum of three factors as articulated in equation 2.4 [2]:

$$P_{avg} = P_{sitching} + P_{short-ckt} + P_{leakage} \quad (2.4)$$

where $P_{sitching}$, $P_{short-ckt}$ and $P_{leakage}$ is the PD due to charging and discharging of output load capacitance, PD due to contention between source and ground while transition, and PD because of spillage current allied with Metal oxide silicon devices individually.

Mathematical expression for the first factor in equation (2.4) can be articulated as [2]:

$$P_{sitching} = \alpha_{0\to1} C_L V_{DD} V_{Swing} f \quad (2.5)$$

where $\alpha_{0\to1}$, termed switching bustle, is the probability $0 \to 1$ switch at output node for every time period of clock, C_L denotes the load capacitance, f defines the utmost probable occurrence speed of change in inputs (in this it is clock speed) and V_{Swing} defines the maximum voltage swing at the output node for a logic circuit.

While transistor dimensions are being cut down with the advancement in technology progressively, leakage current linked to the transistor is increasing at the same pace and transistor characteristics dependencies over-temperature have also risen [4][6]. As a result, performance, robustness, and NI are worsening slowly [21]. Henceforth, decrease in leakage current is the utmost priority in domino circuits, and sub threshold leakage current is the major factor in leakage current.

1.6 THESIS STRUCTURE

The thesis work has been organized over five chapters. Chapter 1 gives the basic introduction about dynamic circuits its advantages over static CMOS circuits, working and problems associated with it. Moreover, it gives typical explanation and working of domino circuits which fall in the category of dynamic circuits. Finally, objective of this work has been described. Chapter 2 is basically a literature survey of all the domino techniques that has been put forward by various respected academicians in order to tackle the issue associated with domino logic gates discussed in chapter1. Chapter 3 describe the proposed design, where mathematical analysis of keeper setup has been performed along with explanation of modification made in evaluation setup, and working of proposed design. Simulation results of various domino technique and proposed design have been compared in chapter 4, along with the discussion on tool and environment used to carry out simulation, and the sizing of transistor used to attain fixed delay. Finally, Chapter 5 concludes the work performed in this thesis and give future scope of work that can be done in this field.

CHAPTER 2

LITERATURE SURVEY OF VARIOUS DOMINO LOGIC CIRCUIT

Numerous designs have been proposed by academics in order to worn down the issues conversed thoroughly in chapter 1 that are NI, PD, and performance. Design practices examined in view of this study credibly typified within three segments. In the first segment, with the aim of trimming down process variation and at least PDP boosting NI the keeper setup has been restyled [3][8][19]. In the second segment, the evaluation setup has been restyled to trim down the sub-threshold spillage current at the minimum PDP [10][11]. Whereas in third segment, both evaluation and keeper setups have been modified to achieve least PD, good NI and performance [1]. In this chapter, all these techniques have been discussed thoroughly starting with conventional domino.

2.1 CONVENTIONAL DOMINO WITH AND WITHOUT EVALUATION TRANSISTOR

Typical conventional domino circuits put forward in [12] are illustrated in Fig. 2.1. As at the commencement of the precharge period all inputs to the domino logic gate are at a low level, evaluation transistor can be excluded as it would lower clock load and boost pull-down run [2]. Though, leakage current would boost as evaluation device has been excluded which directs to further PD. Thus, there are two kinds of CD logic circuits one with evaluation transistor and the other without evaluation transistor as illustrated in Fig. 2.1a and 2.1b correspondingly.

In the evaluation phase, the serious issue is the inevitable leakage currents flowing within the PDN in standby mode (i.e., when all the inputs in the input set are at a logic low level). The key reasons for leakage current are, BTBT current, gate tunneling current, and sub-threshold current. Furthermore, due to charge sharing in PDN the dynamic node voltage is defiled to 0 and results in deficient NI [9] as conversed in chapter 1. To tackle the issue of poor NI and signal integrity, a keeper transistor (PMOS) whose source connected to source voltage, drain to the dynamic node of the domino circuit, and the gate is connected to the output of the CMOS inverter. It forestalls the undesirable discharging of the dynamic node triggered by the leakage currents and charge sharing of the PDN in evaluation period.

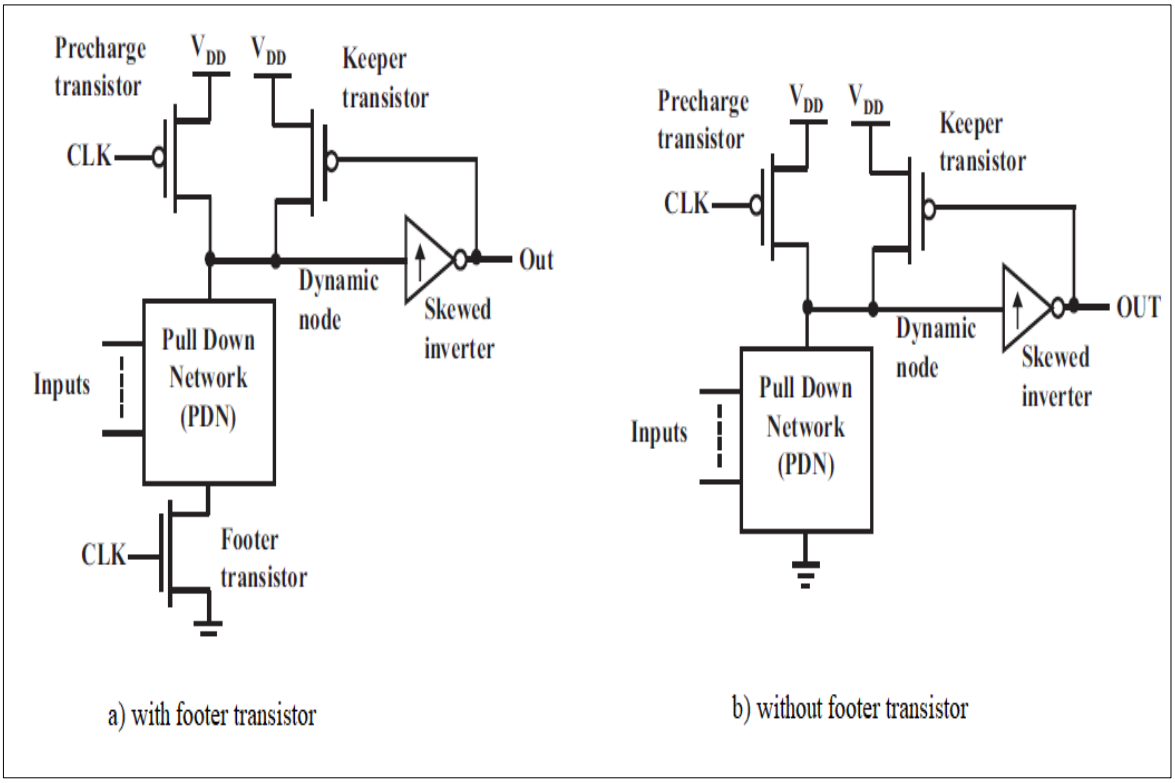

Figure 2.1: Circuit diagram of CD logic gate [9].

In this manner, the circuit heftiness has been enhanced. Even though the sturdy keeper advances heftiness of the dynamic nodes, however there is a deterioration in performance and PDN, because of the strife between the PDN and keeper. Therefore, domino gate operations have been afflicted by both sub-threshold leakage current and noise basis [6]. Consequently, in a typical domino logic gate there subsists a trade-off between delay and NI. To proffer an approach to executes this compromise, the guardian proportion K is named as the proportion of the current drivability of the keeper transistor to that of the PDN transistor:

$$K = \frac{\mu_p(\frac{W}{L})_{keeper\_transnitor}}{\mu_n(\frac{W}{L})_{evaluation\_transnitor}} \tag{2.5}$$

where mobility of hole and electron are labeled as $\mu_p$and μ_n respectively. W/L portrays the proportion of width to the length of the transistor. As the keeper proportion upturns via growing the dimesnion of the keeper transistor, NI enhances; on the other hand, PD and t_{PLH} (evaluation delay) intensify. These hitches are direr in high fan-in dynamic gates because of the large number of NMOS transistors associated with the dynamic node. Thus, the keeper dimension upsizing tactic is not valuable as the technology node is being trimmed down so reducing the size of a transistor is not an option anymore [9].

2.2 DIODE FOOTED DOMINO

Herein, the domino circuit has been mutated by inserting an n-type MOS device in a diode formation (gate and drain terminals associated) in series with PDN, as depicted in Fig. 2.2, which depicts an example of the n-input OR gate using the DFD technique [8]. The diode footer (transistor M_1) trim down the subthreshold leakage as a result of the stacking effect [6]. Owing to the leakage current flowing through PDN at the commencement of the evaluation phase (i.e, standby mode), there is some voltage drop introduced through the diode footer (transistor M_1).

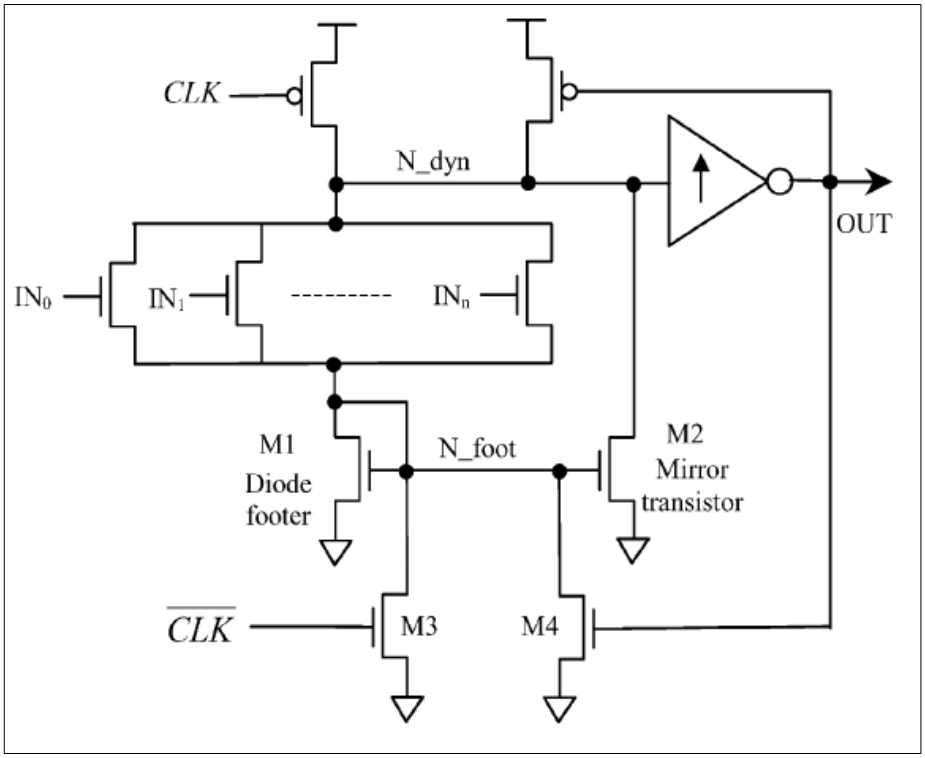

Figure 2.2: N-bit OR gate implemented via DFD practice [8].

For the transistors in PDN Gate to source voltage (V_{gs}) turn out to be negative as a consequence of this voltage drip, set off an exponential decline in the leakage current. Furthermore, source to body voltage (V_{sb}) grow due to this voltage drip through diode formation transistor which in turn amplifies the body effect of the PDN transistors. Hence, leakage current comes down as edge voltage of PDN transistors increase because of body effect [6]. Conversely, diode formation transistor strengthens the switching threshold voltage of the logic gate making it twice the threshold of an n-type transistor (i.e., $2V_{tn}$). NI of the logic gate straightforwardly corresponding to the gate threshold voltage, in other words, the better the logic gate threshold voltage lesser it is prone to noise but at a price of degraded performance. Reduction in evaluation current due to diode formation

transistor is the main reason behind the decline in performance. To enhance performance, transistor $M_2$is used termed as mirror transistor as articulated in Fig. 2.2. to emulate the current through PDN and sink it out of the N_dyn node [8].

Thus, absolute PDN current is the sum of the current through the PDN plus the mirrored current through the N_dyn node. The mirror ratio (M) is termed as the ratio of the current steerability of transistor M_2 to that of M_1 (i.e., fotter formation transistor):

$$M = \frac{(\frac{W}{L})_{M2}}{(\frac{W}{L})_{M1}} \tag{2.6}$$

In the precharge period, the clock signal to the logic gate is at a low level, hence turning the transistors M_3 and M_2, ON and OFF respectively. Transistor M_2 is operating in cut-off mode, which helps in avoiding contention between source and ground in the precharge period when the N_dyn node is charging. There exist two feedback loops one in evaluation setup and the other in keeper setup both helps in speeding up charging and discharging of the output node of a logic gate to boost performance. Speed could be maneuvered through altering variable M. The feedback loop in the evaluation setup further helps in avoiding static power dissipation in the evaluation period. Owing to diode formation transistor in evaluation setup leakage current has been reduced significantly, hence a small keeper will do the work. Transistor M_2 (mirror transistor) cause a small increment in leakage current by steering leakage current from node N_dyn, hence affecting the robustness of the logic gate. Therefore, here occurs a compromise among speed and heftiness offered by mirror ratio manoeuvring. Amplifying the size of keeper transistor in CD has exact consequences as subsiding of mirror ratio in DFD [8].

2.3 VOLTAGE COMPARISON BASED DOMINO

Herein, the VCD technique is structurally divided into two junctures as depicted in Fig. 2.3. The first juncture implements the given logic function in PDN, while the second juncture compares the voltage through PDN and based on voltage difference produces output. To compare the voltage across PDN (i.e., across NODE A and NODE B) a differential sense amplifier is used. VCD helps in reducing voltage sway at Node A (i.e., of parasitic capacitance), which in turn trim downs switching factor of PD [9]. The switching factor of

PD becomes a major concern in high fan-in domino gates as the parasitic capacitance increases drastically in that case.

An n-input OR gate has been modelled using the VCD technique as depicted in Fig. 2.4. Two signal integrity issues have been taken care of by the precharge transistor (M_{p1}) that are charge sharing and leakage current of PDN. Transistor M_{p1} precharge Node A parasitic capacitance to a high level in the precharge period. To avoid incorrect output signal being produced, Node B will be discharged in the precharge period via M_{Dis} transistor as it might have charged stored from previous evaluation period that might affect next evaluation period output.

To compare voltage drip through PDN, an asymmetric SA is utilized as depicted in Fig. 2.4, being composed of transistors M_1, M_2, M_3, M_4, M_5 and M_6, accompanied by CMOS inverter and precharge transistor (M_{p2}).

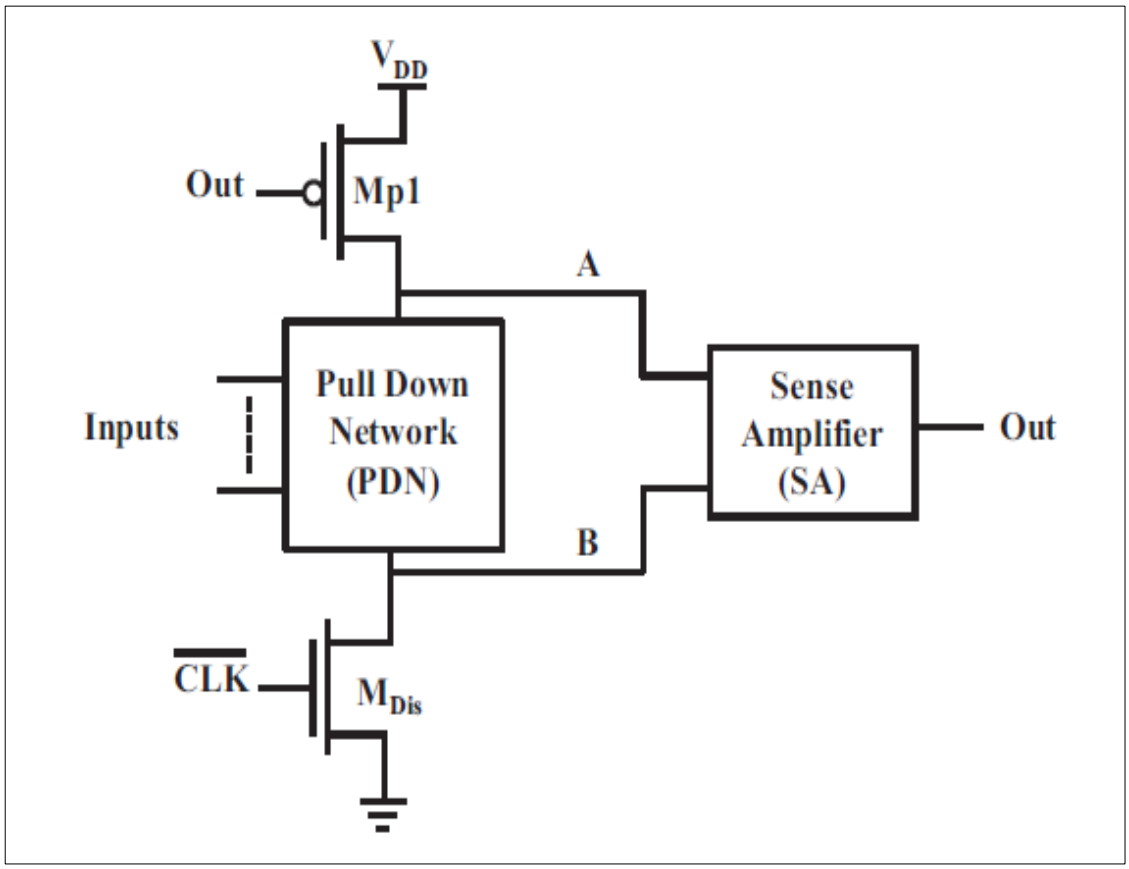

Figure 2.3: Structure of VCD-based logic gate [9].

The switching threshold of VCD based logic gate has been improved by a factor of 2 to that NMOS transistor threshold voltage, because of M_4 transistor. Consequently, NI improves

and leakage current has been trimmed down with the sacrifice of speed. Transistor M_2 act as a mirror transistor, whose sizing influences NI, delay, and PD. M is termed as the ratio of W/L of transistor M_2 to that of M_1 as articulated in equation 2.7:

$$M = \frac{(\frac{W}{L})_{M_2}}{(\frac{W}{L})_{M_1}} \tag{2.7}$$

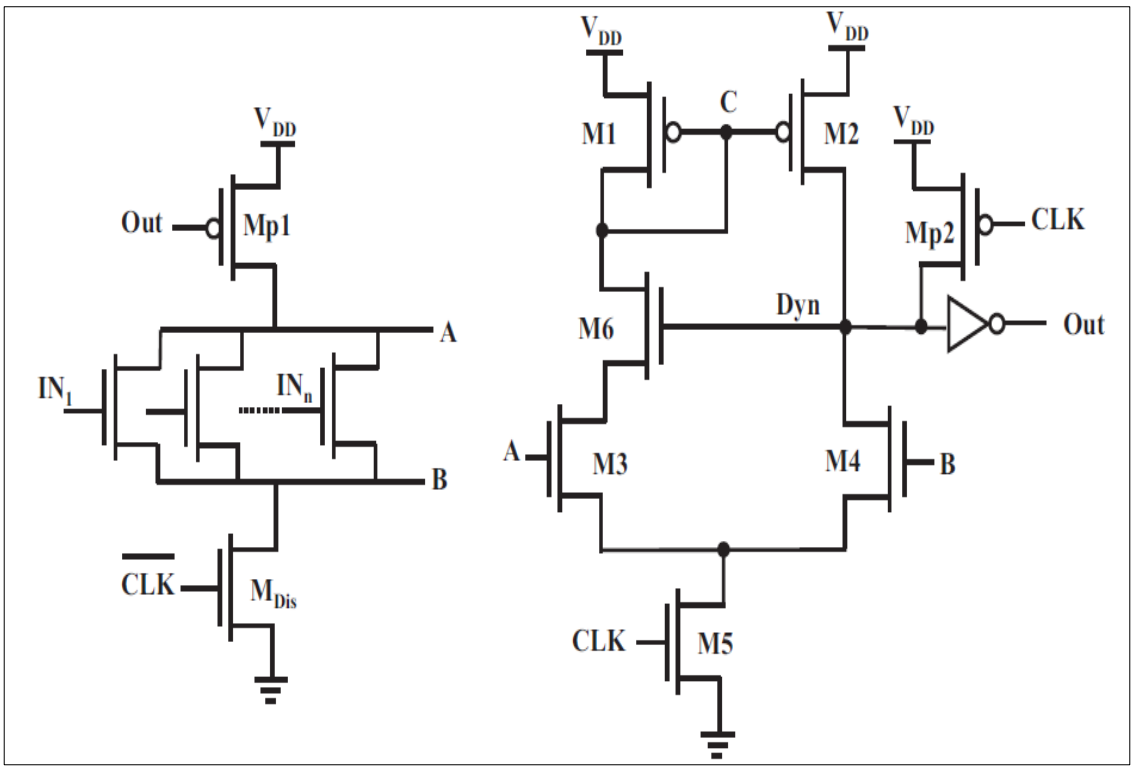

Figure: 2.4. N-bit OR gate designed using VCD [9].

Depending upon the requirement of logic gate M can be adjusted, with its strengthening performance and PD degrade while NI improves, on the other hand with its weakening performance improves at the price of decline in NI. In VCD-based logic gates contrasting to CD logic gate, Dyn node is not connected to PDN. As depicted in Fig. 2.4. only transistor M_4 is connected to Dyn node among pull-down transistors. Hence, parasitic capacitance decreases significantly at the Dyn node in comparison to CD where n number of transistors are connected to the Dyn node [9].

2.4 LOW POWER DOMINO

An n-input OR gate implemented using the LPD technique depicted in Fig. 2.5. In LPD based logic gate, contrasting to CD gate PDN Node is not directly connected to static CMOS

inverter to achieve reduced voltage sway at Node A (parasitic capacitance). Thus, switching component of PD has been reduced significantly. Only M_2 is connected to Dyn node among all other pull-down transistors as depicted in Fig. 2.5., in contrast to CD-based OR logic gate where n number of transistors in PDN are connected to Dyn node.

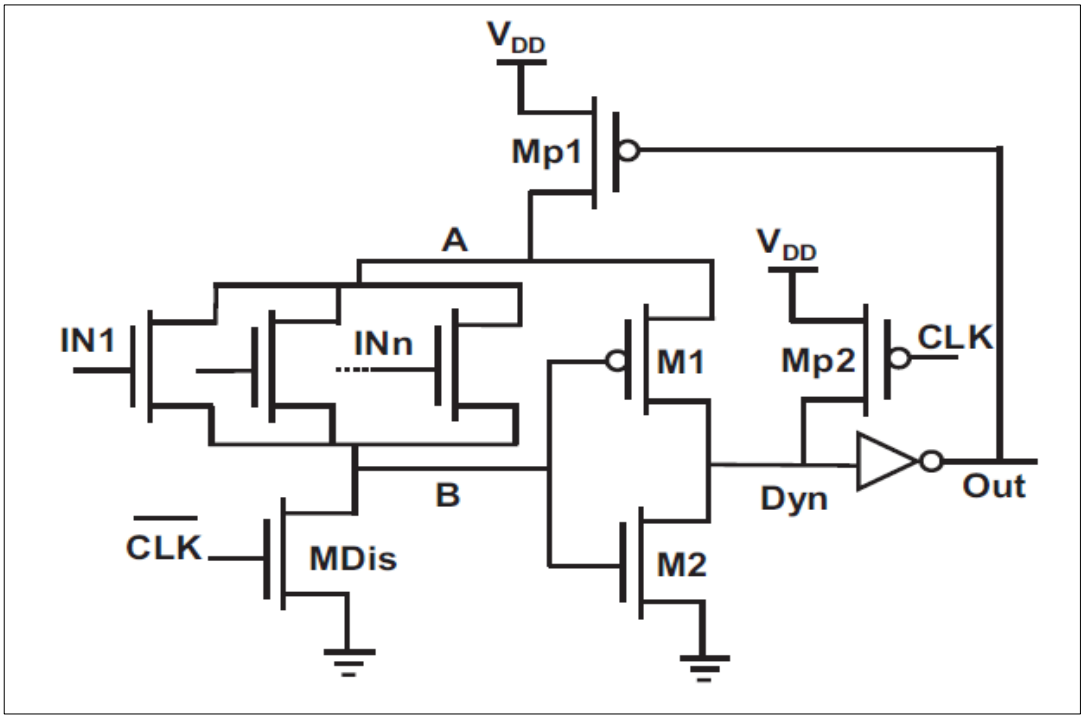

Figure 2.5: N-bit OR gate implemented using LPD [3].

Thus, an LPD circuit have full voltage sway at Dyn node (having small parasitic capacitance), while PDN Node A and B have half the voltage sway w.r.t sway at Dyn node (Node A and Node B have large parasitic capacitance due to the huge number of transistors in PDN) in contrast to CD logic gate. Accordingly, PD in the case of LPD based logic gates has been trimmed down particularly for high fan-in logic gates owing to half voltage sway at Node A and B of PDN. Fig. 2.5 articulates that the key idea behind the LPD technique is to produce output signal based on voltage variance through PDN (i.e., across Node A and Node B). In the event, when the logic gate is in standby mode (i.e., all inputs are at logic low level) $V_A > V_B$ due to lack of linkage between Node A and B. Or else, in the case when at minimum one input is at logic height then voltages V_A and V_B are approximately equal. Hence, taking into account voltage at Node A and Node B output voltage can be interpreted as articulated in equation 2.9 & 2.10 [3] :

$$V_A > V_B + V_{tp} \implies M_1: ON \; and \; V_{out} = 0 \tag{2.9}$$

$$V_A \cong V_B \; and \; V_B > V_{tp} \implies M_2: ON \; and \; V_{out} = V_{DD} \tag{2.10}$$

In the LPD circuit, Node A and Dyn are being charged by transistors M_{p1} and M_{p2} respectively, and Node B is discharged via M_{diss} transistor. Furthermore, the voltage level at the Dyn node is maintained by M_1 keeper transistor. Moreover, M_1 is being controlled via voltage through PDN. So in contrast to the CD logic gate, there is almost negligible strife between transistor M_1 and M_2. As a result, delay and PD have been trimmed down significantly in LPD [3]. Both leakage and switching components of PD have been reduced considerably, resulting in overall lowering down of total PD.

In standby mode (when all inputs in the input set are at a logic low level, in the evaluation phase) PDN transistors will be operating in cut-off mode, hence only leakage current will flow through PDN. Accordingly, the parasitic capacitance at Node B will be charged to some extent owing to the leakage current, giving rise to the following effects in PDN transistors:

- Source to body voltage (V_{sb}) comes into the picture, owing to leakage current some voltage drip occurs across M_2. Hence, the threshold voltage of PDN transistors increases caused by the body effect as articulated in equation 2.11.
- V_{gs} of PDN transistor became negative due to voltage drip across M_2, causing an exponential decline in leakage current.
- Also, a decline in drain induced barrier lowering and V_{ds} also observed.

$$V_{th} = V_{th0} + \gamma(\sqrt{-2 * \varphi_f + V_{sb}} - \sqrt{(-2 * \varphi_f)}) \quad (2.11)$$

In a nutshell, it has been observed leakage current reduced considerably in LPD logic gates owing to a rise in threshold voltage and decline in V_{gs} and V_{ds} of PDN transistors. LPD logic gates exhibit a switching threshold voltage almost twice NMOS transistor threshold voltage because the source of PDN transistors is connected M_2 gate. Hence, with the boost in the switching threshold of the LPD based logic gate, NI improves at the price of performance.

2.5 CONTROLLED KEEPER CURRENT COMPARISON DOMINO

In general, p-type keeper transistor dimensions are required to be augmented to enhance NI. In case, NI is 1/10 of source voltage width of p-type keeper transistor can be augmented to 1/10 of worst-case PDN transistors width. However, augmentation of keeper size is not possible as the technology node is being trimmed down, and also it gives rise to PD and amplified contention between source and ground (via path formed by keeper setup and

PDN). Keeper transistor needs to be turned off in case at minimum one input in the input vector is at a high level, to resolve these issues. Dyn_n node voltage drops off to zero in two situations: each of two i.e., if input set forms a transmission path for Dyn_n node to discharge to ground or leakage current in PDN amplified due to temperature or availability of various leakage paths causing Dyn_n node to discharge, are true. The p-type keeper transistor must not be switched off in the second case. Conversely, current in the second case is greater than the first case. So, differentiating between these two cases by the use of reference current is the main idea behind the CKCCD technique [11].

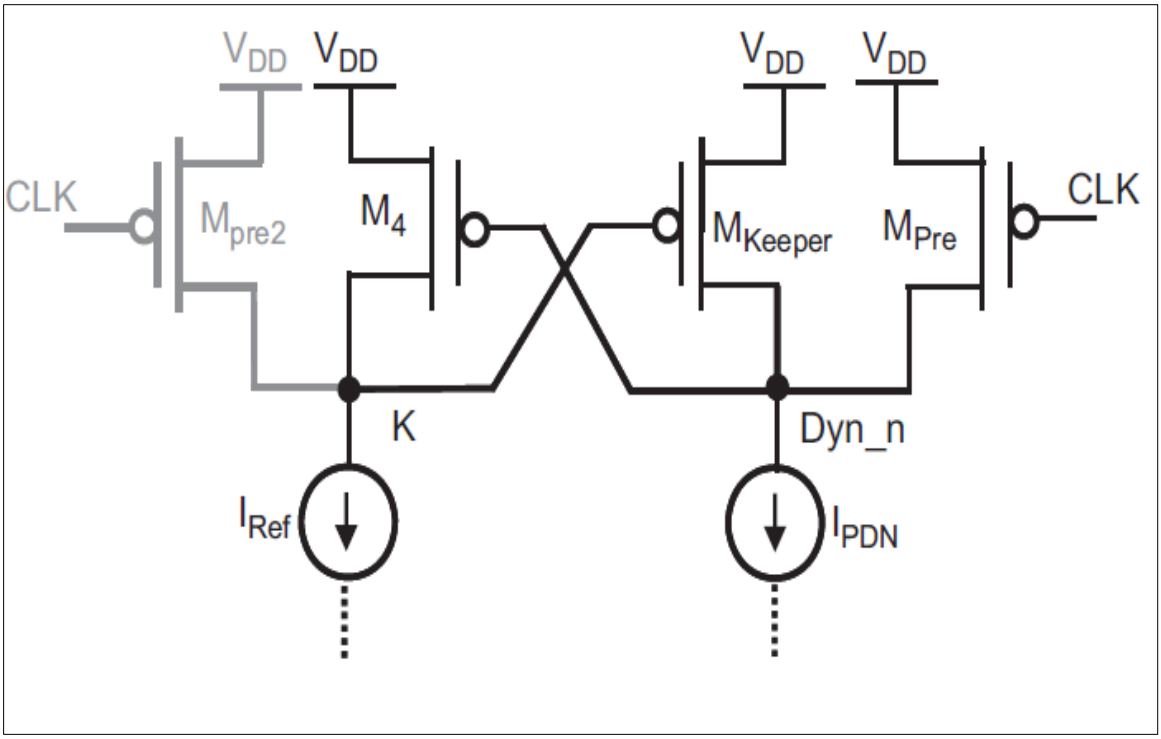

Figure 2.6: Basic working concept of CKCCD [11].

Inside the CKCCD technique, a comparison of reference and PDN current is performed. In standby mode (i.e., when all inputs are at logic low level) no transmission pathway exists between Dyn_n node and ground, so only leakage current traverses in PDN, hence keeper remains switched ON (as spillage current is not as much as reference current). The outline of this technique is abstractly articulated in Fig. 2.6. So, depending upon which current is more p-type keeper transistor will be turned ON or OFF. With an intention to discharge K node M_{pre2} transistor has been uninvolved and consequently switching ON keeper transistor in the precharge period, which in turn enhances NI. Thus, contrasting to HSD techniques that will be discussed next in this chapter, where the keeper is operating in cut-off mode at the commencement of the evaluation period, it is operating in a linear region in this

technique. An n-input OR gate modelled using the CKCCD technique has been depicted in Fig. 2.7[11].

In CKCCD based logic gate a diode formation n-type transistor is connected in series with PDN as demonstrated in Fig. 2.7, to trim down leakage current in PDN when the logic gate is operating in standby mode (i.e., all inputs to the logic gate are at a low level) owing to stacking effect [14].

There are three ways due to which leakage current in PDN is reduced owing to voltage drip through M_1.

- V_{gs} of PDN transistors turn negative.
- Due to the rise in V_{sb} of PDN transistors body effect amplifies, which in turn enhances V_{tn} (threshold voltage of PDN transistors).
- Drain induced barrier lowering and V_{ds} drop off to certain extinct.

Resulting due to the above reasons, the leakage factor of PD has been trimmed down significantly [11].

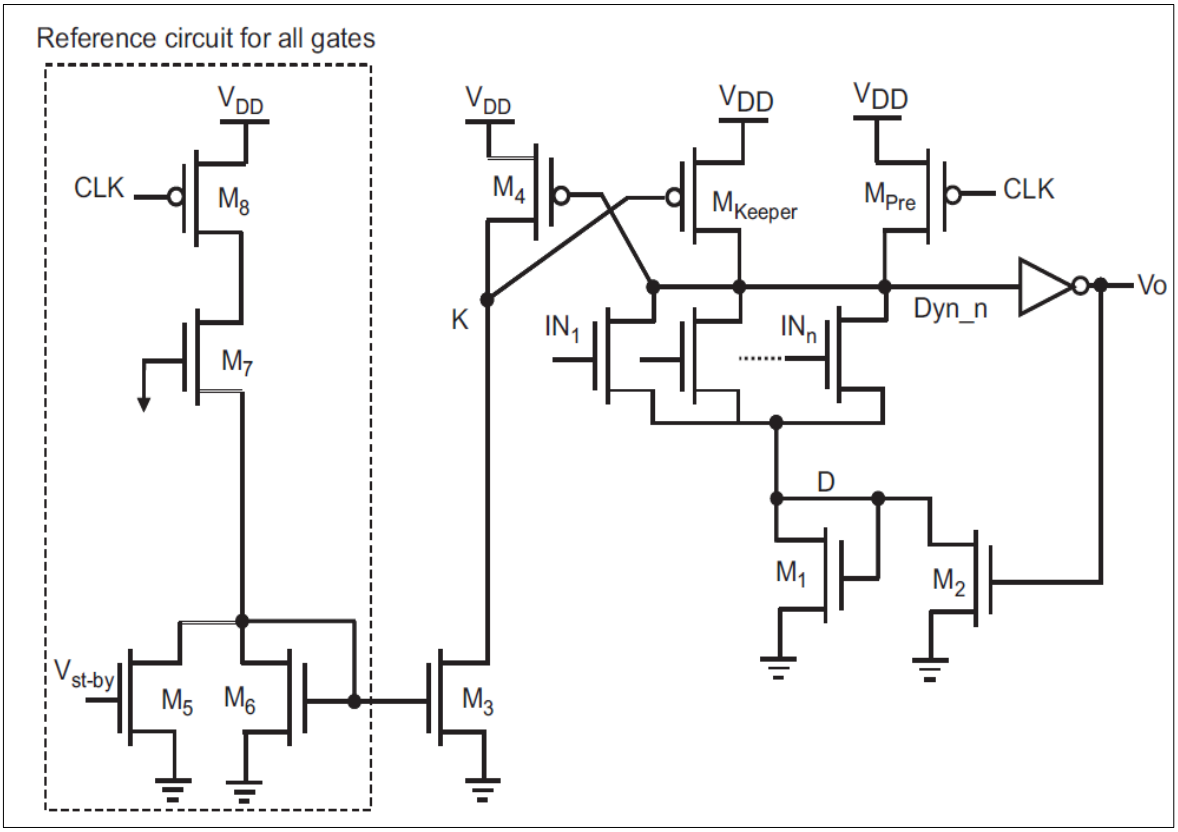

Figure 2.7: N-bit OR gate implemented using CKCCD [11].

Given that a small keeper would do the work, as leakage current in PDN has reduced substantially. Conversely, NI can be improved via boosting keeper dimensions, particularly for high fan-in OR gates. Likewise, NI can be further enhanced as a result to boost in

reference current caused by amplifying W_3/W_6 ratio. Similarly, performance can be enhanced by reducing W_{kepper}/W_4 ratio [11].

As depicted in Fig 2.7. the left-hand side of the circuit which is the reference current circuit comprises of $M_5 - M_8$. In standby mode, M_5 will be switched ON, while operating in a cutoff mode in active mode to trim down stand-in PD. Reference current should be more than leakage current in PDN and less than PDN flow current when at minimum one input in input vector is at logic high, to safeguard its accurate functioning. So, dimensions of M_5 transistor can be varied to adjust reference current. In the CKCCD technique reference circuit is a duplication of the pull-down network, therefore reference current will also vary with temperature in the same manner as leakage current in PDN varies. Hence making gate designed using the CKCCD technique temperature-independent [11]. CKCCD based logic gates have high robustness and NI owing to the enhanced threshold voltage of logic gate due to diode formation transistor M_1 [11].

2.6 HIGH-SPEED DOMINO

An 8-input OR gate modelled using the HSD technique as depicted in Fig. 2.8. The primary thought behind this method to give a deferred clock to keeper device utilizing two CMOS inverter and, one n-type and one p-type transistor whose gate is connected to the output of the CMOS inverter I_3 as portrayed in Fig. 2.8.

2.6.1. High-speed domino operates as follows:

In the precharge period, the clock signal to the logic gate is at a low level, hence the Dy_n node is charged to logic high. While transistor P_1 and N_1will operate in cut-off and linear regions respectively, owing to its gate voltage the transistor Q_2 will be switched OFF. As a result, at the commencement of the evaluation phase Q_2 will remain OFF, thus trimming down strife between keeper setup and PDN. HSD-based logic gates have a high speed with no short circuit [10]. In case when tardy clock level become logic high, two situation arises:

- In the case at minimum, one input in the input vector is at logic high, Dy_n node discharge to logic low, and gate output to logic high level. As a result, N_1 will operate in the linear region, owing to which keeper remain in cut off mode as its gate is at a logic high level because N_1 will act as a pass transistor in this case.

- Conversely, in standby mode (i.e., when input set is at logic low level in evaluation phase) Dy_n node and output node maintain logic high and low level respectively. And the gate of keeper transistor Q_2 discharged via N_1, hence Q_2 operates in linear region in this case.

Hence, as the keeper is operating in the linear mode it will reimburse for leakage current and uphold voltage level high at Dy_n node. So the problem of strife between the power supply and the ground when both keeper and PDN transistor operate in linear mode has been solved by switching keeper OFF at the commencement of the evaluation phase. For that reason, dimensions of keeper can be enhanced to support a regulated NI, without disturbing performance and PD. To avoid strife between the precharge transistor and PDN, the clock signal to HSD based logic gate must reach beforehand input signal. In conditional domino-based logic gates, this is the most significant condition that must be taken care of [14].

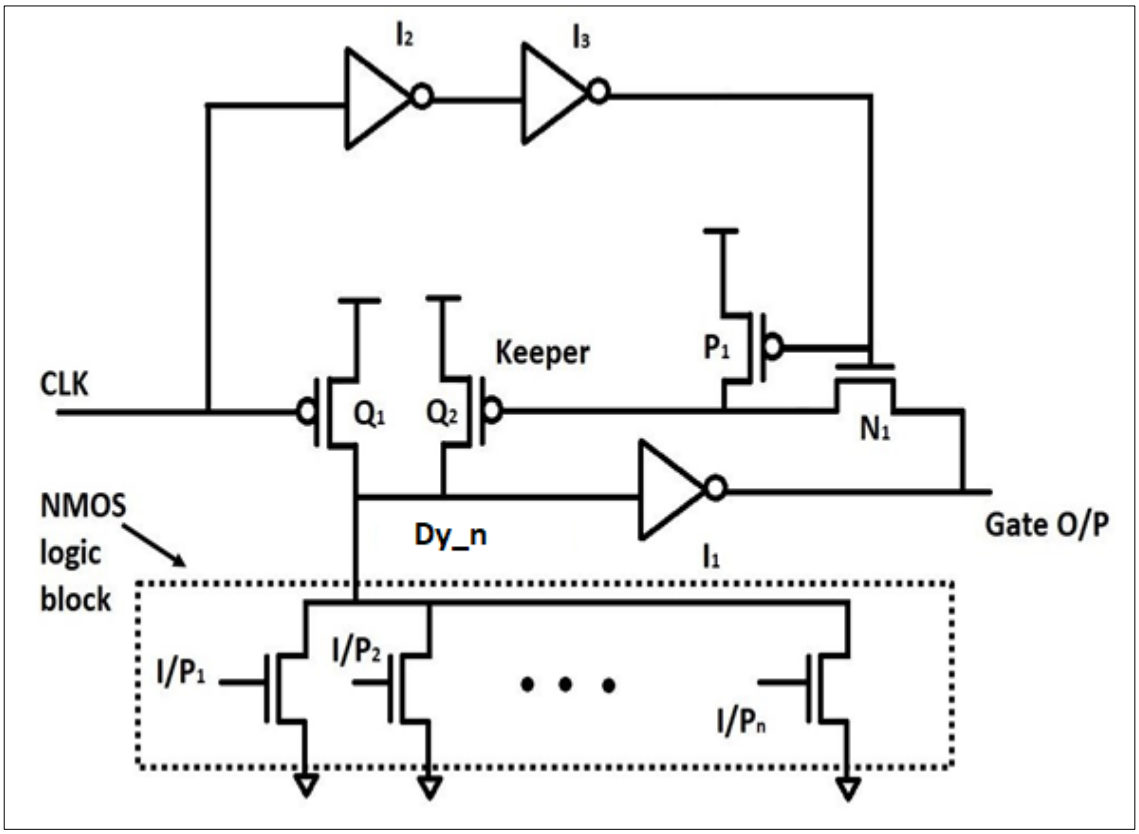

Figure 2.8: 8-input OR gate implemented using HSD [10].

Small dimension transistors (i.e., N_1 and P_1) being used to connect the gate of the keeper to the delayed clock and output node in the precharge and evaluation period, hence these transistors will have the least contribution in clock loading. The key devices that are responsible for clock loading are the precharge transistor and two inverters used in clock

delaying circuitry. HSD-based logic gates demonstrate minimum dynamic PD. The dominance of HSD-based logic gates can be seen in deep-submicron technology nodes, where the leakage component is the key reason for overall PD [10].

2.7 DESIGN PRESENTED IN A. KUMAR ET. AL.

In reference [1], a new design of domino gate has been put forward in which both keeper and evaluation setup have been modified. Firstly, in evaluation setup evaluation transistor has been replaced by two N-type transistors namely M_{n1} and M_{n2} with small threshold voltage, to enhance the threshold voltage of transistors in PDN. Transistor M_{n1} has been utilized in diode formation in series with PDN, in order to trim down leakage current flowing through PDN transistors in standby mode i.e., when the input set is at the logic low level in the evaluation phase [6][15].

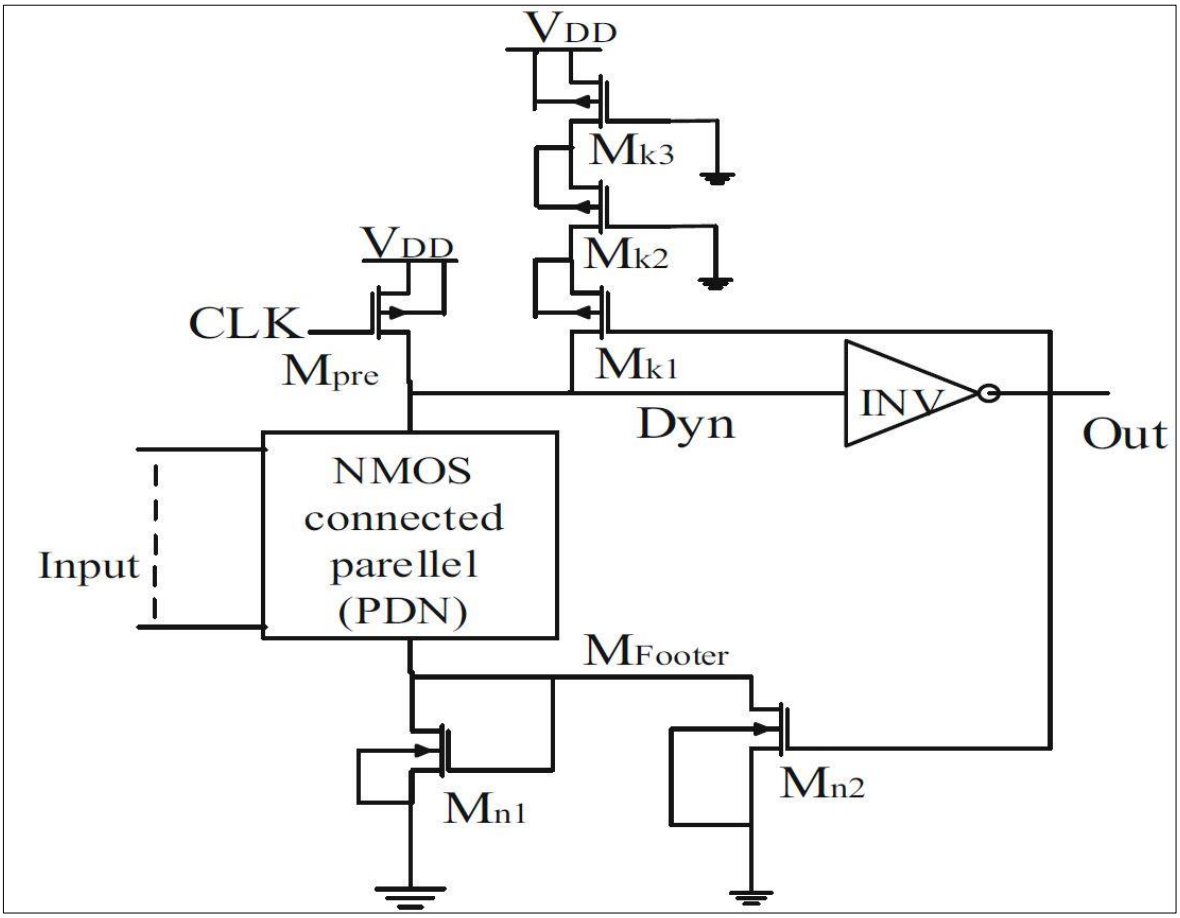

Fig. 2.9. Circuit diagram of logic gate based on domino composition given in reference [1]

Due to this leakage current, some voltage drop will occur through the diode formation transistor. As a result of this voltage drop, the gate to source voltage of PDN transistors

becomes negative in turn enhancing the body effect [8][16]. Owing to which the threshold voltage of PDN transistors increases as articulated in equation 2.11, hence trimming down leakage PD. Also, there will be a rise in drain to source voltage and reduction DIBL due to this voltage drip which will further reduce leakage current, hence PD in standby mode. Additionally, in the case at minimum one input in the input set is at logic high then M_{n2} offers a path to Dyn node to discharge to ground via PDN and M_{n2}. A low threshold voltage transistor M_{n2} is utilized in order to offer speedy discharging to the Dyn node in the evaluation period. Secondly, in keeper setup instead of one keeper transistor three transistors are used namely M_{k1}, M_{k2} and M_{k3}. Where gate of M_{k1} is connected to the CMOS inverter output node, while the gate of M_{k2} and M_{k3} are connected to the ground. This formation of keeper transistors as portrayed in Fig.2.9, trims down the closed-loop gain of feedback loop present in keeper setup. Which in turn trims down variations in performance and enhances NI [1].

In this domino design dimensions of the keeper and precharge transistors can be kept at a minimum as both trans-conductance and leakage current have been trimmed down significantly. Additionally, through amplifying dimensions of M_{n1} and M_{n2} transistor both performance and noise margin can be enhanced while keeping power dissipation minimum.

CHAPTER 3

PROPOSED DESIGN

In this chapter, an innovative domino technique has been put forward and discussed in depth. The main objective of this new circuit is to relegate PD and process variations in speed. In order to achieve that both evaluation setup and keeper setup have been tailored. In the keeper setup, the closed-loop gain of feedback control formed by keeper (PMOS) transistor whose gate allied to static CMOS inverter output has been reduced, to trim down variations in speed. Meanwhile, in evaluation setup a diode formation transistor allied in sequence with PDN to reduce leakage current which in succession trim downs leakage factor of PD at the cost of degraded speed. Speed can be uplifted back to normalcy with the help of a mirror transistor while retaining NI.

3.1 Analysis of feedback loop

To comprehend this new technique, initially feedback aspect in keeper setup of CD which was discussed in chapter 2 is put under scrutiny, alongside understanding how tailored keeper setup might help in trimming down process variations in the proposed technique [17]. Mathematical articulation of the feedback component can help in getting a clearer picture. In CD keeper transistor is the key factor backing process variations [18].

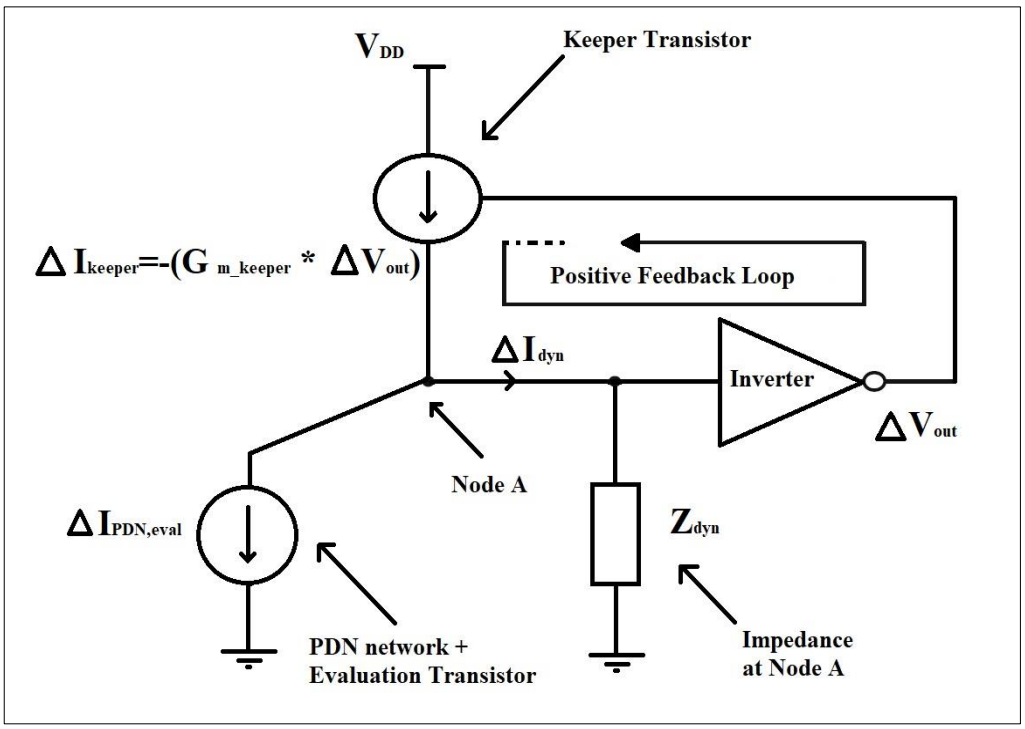

Figure 3.1. Simplified circuit of CD with evaluation setup as depicted in Fig. 2.1b.

Fig. 3.1. is the streamlined setup of CD presented in Fig. 2.1b of chapter 2, to compute the small-signal closed-loop gain. $\Delta I_{PDN,eval}$ is an independent & ΔI_{Keeper} is a dependent current source which are replacements for NMOS-PDN accompanied by evaluation setup and keeper setup respectively. ΔV_{Out} which is output node voltage regulates ΔI_{Keeper}, the small-signal expression for this can be articulated as in equation 3.1[16]:

$$\Delta I_{Keeper} = -(G_{m\_keeper} * \Delta V_{Out}) \tag{3.1}$$

G_{m_keeper}, denotes transconductance of keeper transistor. Consequently, the small-signal node A voltage can be portrayed as articulated in equation 3.2:

$$\Delta V_A = Z_{dyn} * \Delta I_{dyn} \tag{3.2}$$

Z_{dyn} denotes (parasitic capacitance) impedance at Node A and ΔI_{dyn} is articulated in equation 3.3:

$$\Delta I_{dyn} = \Delta I_{PDN,eval} - \Delta I_{Keeper} \tag{3.3}$$

T is termed as the feedback loop gain, formed between the keeper setup and static CMOS inverter as portrayed in equation 3.4:

$$T = A_{inv} * G_{m\_keeper} * Z_{dyn} \tag{3.4}$$

Gain of the inverter is symbolized by A_{inv}. When the evaluation phase commences node A and output node will achieve high and low levels respectively, as a result A_{inv} will be smaller than one [17]. Additionally, at the same instant as keeper (PMOS) transistor is operating in the linear region, hence its transconductance is small. So, it can be assumed that at the commence of the evaluation phase the value of closed-loop gain T is positive and smaller than one as both A_{inv} and $G_{m\_keeper} * Z_{dyn}$ have values smaller than one.

$$S = 1/(1 - T) \tag{3.5}$$

Equation 3.5. gives the sensitivity of closed-loop gain linked with the feedback loop in keeper setup as portrayed in Fig. 3.1. to process variations, as suggested in the fundamentals of control system [19] [20]. As per equation 3.5 when T approximates to one, then S approximates to infinity leads to a rise in process variation in current ΔI_{dyn}. In the view of the fact that, ΔI_{dyn} (small-signal current) controls the voltage declivity and delay across node A. Hence delay of the domino circuit has become more susceptible to process variations. However, when T approximates to infinity then S approximates to one under these

circumstances ΔI_{dyn} is less susceptible to process variations [16]. In simple words, process variation mounting in domino circuit due to the presence of feedback between keeper setup and inverter can be abated by trimming down closed-loop gain T.

To trim down closed-loop gain, any one of the three parameters can be lessened as articulated in equation 3.4. Trimming down of keeper (PMOS) transistor transconductance (G_{m_keeper}) is chosen to boost the speed of the proposed domino circuit, meanwhile dodging any divergence in PD and NI, as it is hard to regulate A_{inv} and Z_{dyn} .

In this new technique, two keeper transistors in place of one are used namely M_{k1} and M_{k2} as portrayed in Fig. 3.2 to cut back total transconductance. Gate of keeper transistor M_{k1} is connected to the output node and of M_{k2} is connected to the ground. Transistor M_{k2} behaves as equivalence resistance as articulated in equation 3.6 [16]:

$$R = [\mu_p C_{ox} \left(\frac{W}{L}\right)_{k2} (V_{DD} - |V_{tp}|)]^{-1} \tag{3.6}$$

Thus, the overall effective keeper transconductance ($G_{m,effective}$) can be articulated as [16]:

$$G_{m,effective} = \frac{G_{m,k1}}{1+G_{m,k1}*R} \tag{3.7}$$

Where R is the equivalence resistance for keeper transistor M_{k2} and $G_{m,k1}$ is transconductance for keeper transistor M_{k1}. Equation 3.7 articulates that the effective transconductance has been reduced by a factor of $(1 + G_{m,k1} * R)$, which sequentially causes a drop in closed-loop gain portrayed in equation 3.4 by the same amount. Hence, the speed of domino circuits for a given function is now susceptible to a lesser extent to process variations.

3.2 Evaluation network modification

In general, for CD logic gates having large fan-in, when all inputs are at a logic low level in the evaluation phase (i.e., the logic gate is in standby mode) amplified leakage current flows in NMOS-PDN [6][15]. Although, new domino technique discussed in this chapter consists of an NMOS transistor M_{d1} in diode formation connected in series with PDN as portrayed in Fig. 3.2 to tackle this issue of leakage current. Fig. 3.2. shows an n-bit OR-gate designed using the proposed domino technique. This reduction in leakage current in PDN has been caused by stacking effected produced by series connection of the transistor M_{d1} and PDN.

In standby mode (i.e., when all inputs to the domino circuit are at logic low in the evaluation phase), a voltage drop arises across the transistor M_{d1} due to the flow of leakage current through NMOS transistors of PDN. Owing to this voltage drop, V_{gs} (gate to source voltage) of NMOS transistors in PDN turn out to be negative triggering exponential decay in leakage current as per equation 1.2 of chapter 1. Moreover, some amount of V_{sb} (source to body voltage) also generated for NMOS transistors in PDN due to which threshold voltage increases because of body effect [1][11]. Equation. 3.8 provides the mathematical expression for threshold voltage and its dependency over V_{sb} [7].

$$V_{th} = V_{th0} + \gamma(\sqrt{-2 * \varphi_f + V_{sb}} - \sqrt{(-2 * \varphi_f)}) \tag{3.8}$$

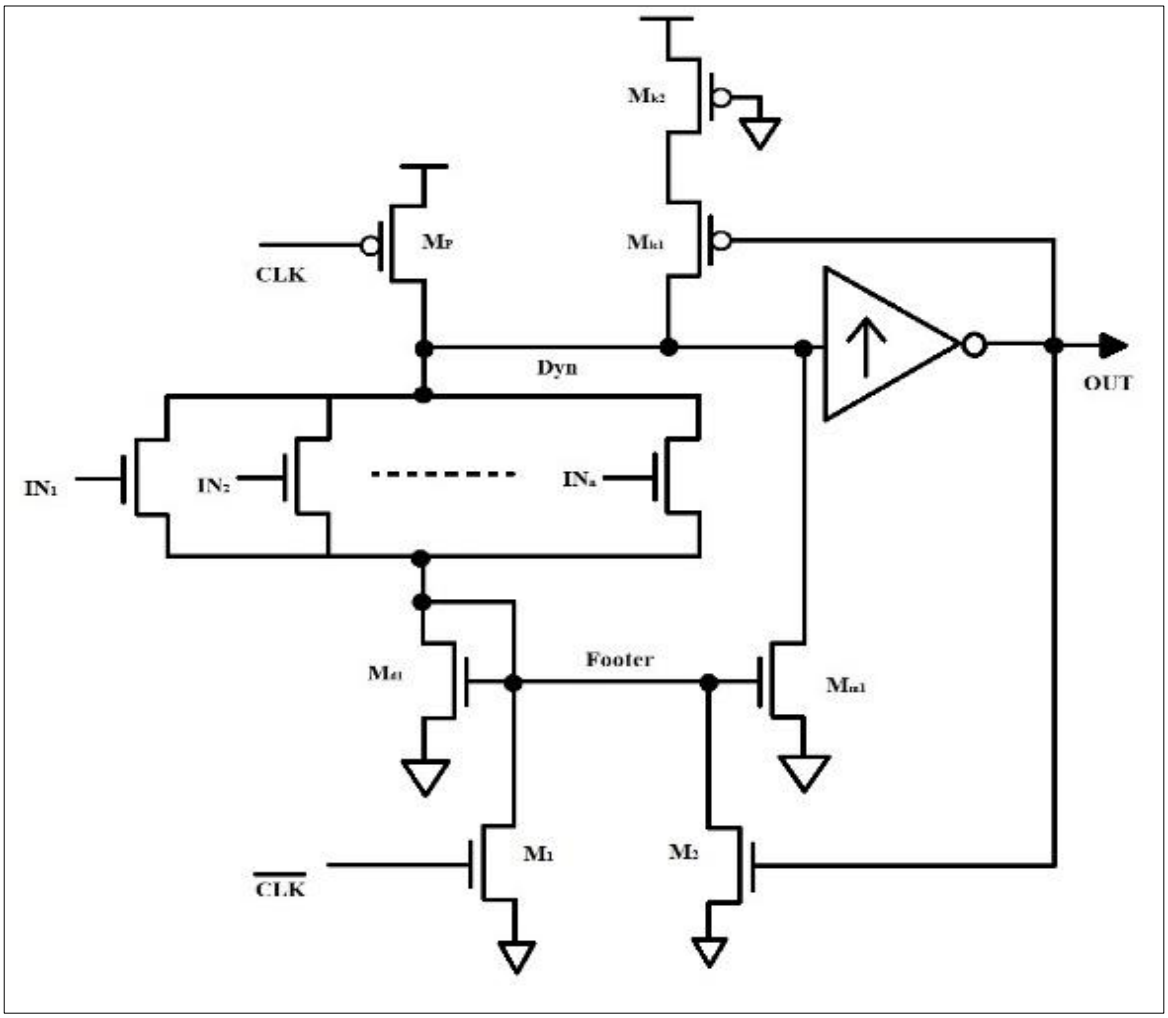

Figure 3.2. Circuit diagram of proposed domino technique.

Furthermore, the switching threshold voltage for the proposed domino circuit is twice the threshold voltage of the NMOS transistor because of the transistor in diode formation (M_{d1}) ensuing enhanced NI at the price of speed. The root cause of the shortfall in performance is due to the decline in the current driving potential of PDN, because of transistor M_{d1}

connected in diode formation to PDN. To fix this hindrance created by a transistor M_{d1}, a mirror transistor M_{m1} positioned in evaluation setup whose drain connected to the dynamic node of domino circuit and gate of both transistor M_{d1} and M_{m1} tied together and being controlled by transistor M_1 as portrayed in Fig. 3.2. Resulting in total PDN current as the sum of the current through PDN and current mirrored by transistor M_{m1} from node Dyn. The ratio of transistor size of M_{m1} to that of M_{d1} is labelled as mirror ratio (M) as articulated in equation 3.9:

$$M = \frac{\left(\frac{W}{L}\right)_{m1}}{\left(\frac{W}{L}\right)_{d1}} \tag{3.9}$$

The mirror ratio (M) can be varied to achieve the required speed for the domino circuit. In the precharge phase, transistor M_2 is accountable for discharging of Dyn node if more than one input is at a logic high level by establishing a path linking node Dyn and ground. The new technique discussed in this chapter is highly efficient in reducing leakage current flowing through PDN, which indicated diminution of charge sharing problem at Dyn node. This confirms efficient charging and discharging of parasitic capacitance at the Dyn node, resulting in improvement of NI.

3.3 Working

Fundamentally, the domino logic circuit works in two phases based on clock signal level, In the precharge and evaluation phase when the clock signal is low and high respectively.

3.3.1 Precharge phase

In the precharge phase, as the clock signal to the domino circuit is at logic low, causing transistor M_p to turn ON. Eventually, Dyn node begins charging to a logic high level due to PMOS transistor M_p. As a result, the output of the static inverter switches to or maintain logic low level depending on previous sate of output node(which is also the output node of the domino circuit). The output of the inverter is connected to the transistor M_2 and M_{k1}, hence will be turned OFF and ON respectively. During this phase transistor M_1 is turned ON, to drive the transistor M_{m1} (mirror transistor) OFF to evade contention between the source voltage and ground via path established through node Dyn and transistor M_{m1}. Inputs set is required to be at logic low to evade contentions between power supply and ground, hence NMOS transistors in PDN operate in cut-off mode (i.e., turned OFF), as discussed in chapter 1.

3.3.2 Evaluation phase

In this period, as the clock signal to domino circuit is logic 1, causing transistor M_p operate in cut-off mode (i.e., turned OFF). Conditional to the input set transistor M_{k1} and M_2 will be turned ON or OFF. Two cases arise conditional to the state of input set:

- In the first case, all the inputs are at logic low (i.e., domino circuit is in standby mode), hence Dyn node and output node will uphold logic high and low level respectively. All the PDN transistors operate in cut-off mode (i.e., remain turned OFF), at the same time the diode formation transistor M_{d1} diminishes sub-threshold leakage current via stacking effect. And the status of transistors that were there in the precharge phase stay put.
- In the second case, when at least one of the inputs to the dynamic circuit in the input set is at logic high. In that case, dependent on the NMOS transistor in PDN whose input (gate voltage) is at logic high will be turned ON and give a way to Dyn node to release. Consequently, static CMOS inverter output changes to logic high level and transistor M_{k1} will be turned off (i.e., operate in cut-off mode). Due to the feedback loop that exists in evaluation setup (output node of dynamic circuit is connected to the gate of keeper transistor M_2), footer node will be connected to the ground, when at least one input is at logic high. Hence, boost up the discharging of the Dyn node. In the end, Dyn and output node will accomplish logic low and high level respectively.

CHAPTER 4

SIMULATION RESULTS AND COMPARISON

The circuits researched in this work have been simulated on a cadence virtuoso platform where circuit designing has been done on Spectre and ADE L has been used for carrying out DC and Transient analysis. 8-bit OR gate have been built utilizing standard domino with and without evaluation transistor (Fig. 4.1), the high speed domino (HSD Fig. 4.7), the diode footed domino (DFD Fig. 4.5), domino composition given in [1] (Fig. 4.9), and proposed domino design (Fig. 4.11) in 180nm CMOS technology node. Simulation of all 8-bit OR gates designed has been carried out at a bottlenecking temperature, i.e., 110℃, 1.8V supply voltage, at 50MHz clock frequency, and in order to mimic the effect of high fanout a 5fF capacitance have been connected to the output node. All three performance parameters, i.e., average PD, UNM, and the absolute sum of transistors utilized in designing 8-bit OR gates have been premeditated under the similar delay state i.e.,120ps (iso-delay) and are examined under most pessimistic scenario by considering all inputs in input vector at logic 0 in precharge period and just one input is at logic 1 in the evaluation period. In order to authenticate the efficiency of the proposed domino design among other domino designs being simulated.

4.1 NOISE IMMUNITY AND POWER CONSUMPTION METRIC

The average PD of each 8-bit OR gate is computed. In order to compute the NI quantitatively the following noise metric is used.

4.1.1 Noise margin

Unity noise margin (UNM) is used to calculate noise metrics in this study. UNM is equal to the amplitude of the input source which generates an equal amount of amplitude at the output node [11].

$$\text{UNM} = \{V_{in} : V_{noise} = V_{out}\} \tag{4.1}$$

Input supply that is utilized to compute UNM behave just like real noise pulse which is the result of glitches, ground bounce, crosstalk, etc.

4.2 TRANSISTOR SIZING AND SIMULATION

For all 8-bit OR gate designed using different domino techniques as discussed above the width and length of all transistors is kept to the minimum i.e., $W_{min} = 3L_{min}$ and L_{min} respectively, where $L_{min} = 180nm$. In order to achieve the desired delay of 120ps (i.e., iso-delay) dimensions of certain transistors have been varied. The ratio of the width of PMOS to NMOS transistor of the inverters is set to 2, except those are specified in Table 4.1-4.5.

4.2.1 Convention Domino with And Without Evaluation Transistor

For CD as depicted in Fig. 4.1 and Fig 4.3., which articulates the schematic of 8-bit OR gate built with CD with and without evaluation transistor [7][12], keeper and precharge transistors size have been altered in order to achieve 120ps (iso-delay). Whereas Fig. 4.2 and Fig.4.4 portray the transient waveforms obtained after simulation, and Table 1 gives sizing of all transistors utilized in designing CD with and without evaluation transistor.

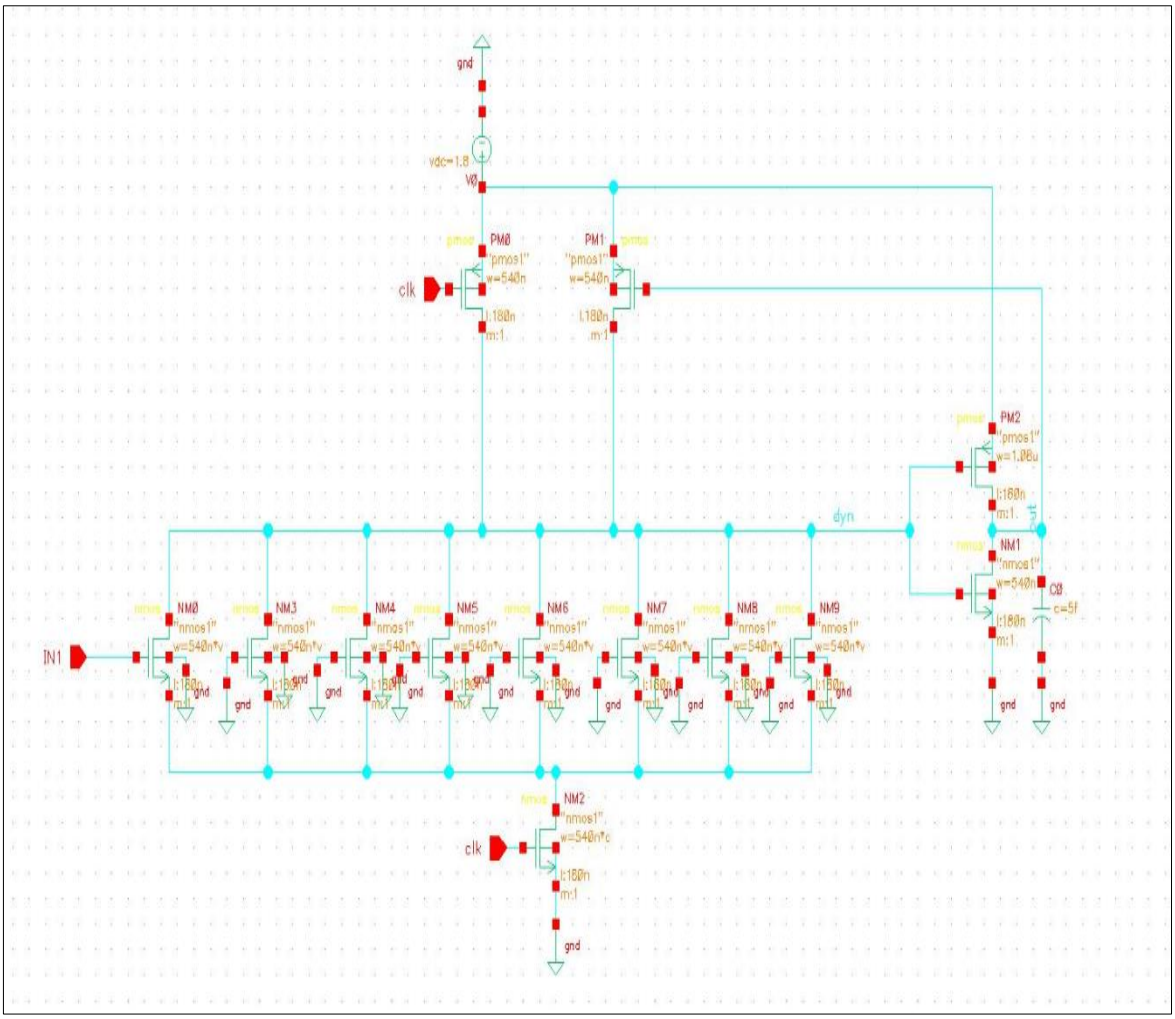

Figure 4.1: Schematic diagram of 8-bit OR gate implemented using CD with evaluation transistor technique.

Figure 4.2: Simulated output waveform of 8-bit OR logic implemented using CD with evaluation transistor technique.

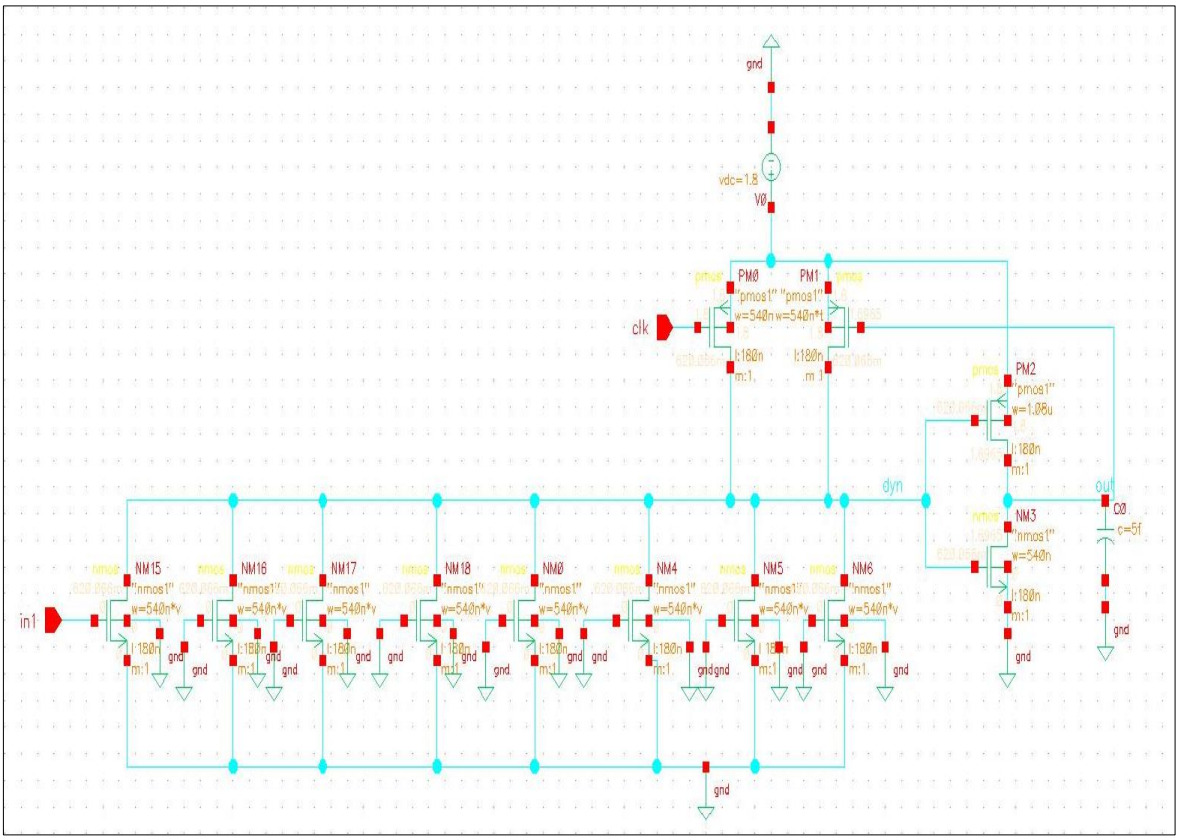

Figure 4.3: Schematic diagram of 8-bit OR gate implemented using CD without evaluation transistor circuit.

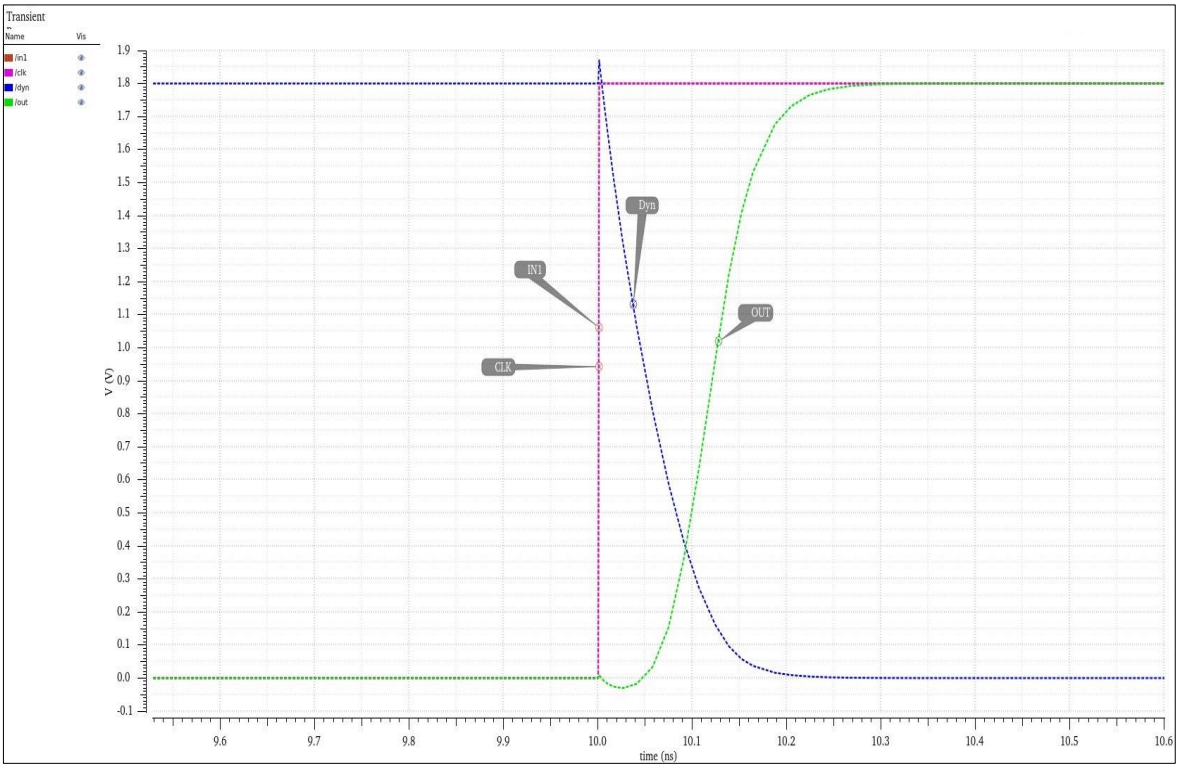

Figure 4.4: Simulated output waveform of the 8-bit OR logic implemented using CD without evaluation transistor circuit.

conventional domino with evaluation transistor	Fan-in (delay)	$W_{precharge}$	W_{keeper}	$W_{pull-down\ transistor}$	$(\frac{W_p}{W_n})_{inverter}$	$W_{evaluation}$
	8-bit t_p=120ps	$3L_{min}$	$3L_{min}$	$12L_{min}$	$(\frac{6L_{min}}{3L_{min}})$	$7.5L_{min}$

conventional domino without evaluation transistor	Fan-in (delay)	$W_{precharge}$	W_{keeper}	$W_{pull-down\ transistor}$	$(\frac{W_p}{W_n})_{inverter}$
	8-bit t_p=120ps	$3L_{min}$	$3L_{min}$	$3.3L_{min}$	$(6L_{min}/3L_{min})$

Table 4.1. Size of all transistors used in implementing 8-bit OR gate using CD with and without evaluation transistor.

3.2.2 Diode Footed Domino

Fig. 3.5 and Fig. 3.6 depict the schematic and transient waveform obtained after stimulation of the 8-bit OR gate tailored by utilizing the diode-footed domino (DFD) technique, respectively. To attain the desired delay, dimensions of mirror, keeper, and Precharge transistors have been altered. Table 2 gives sizing of all transistors utilized in designing DFD.

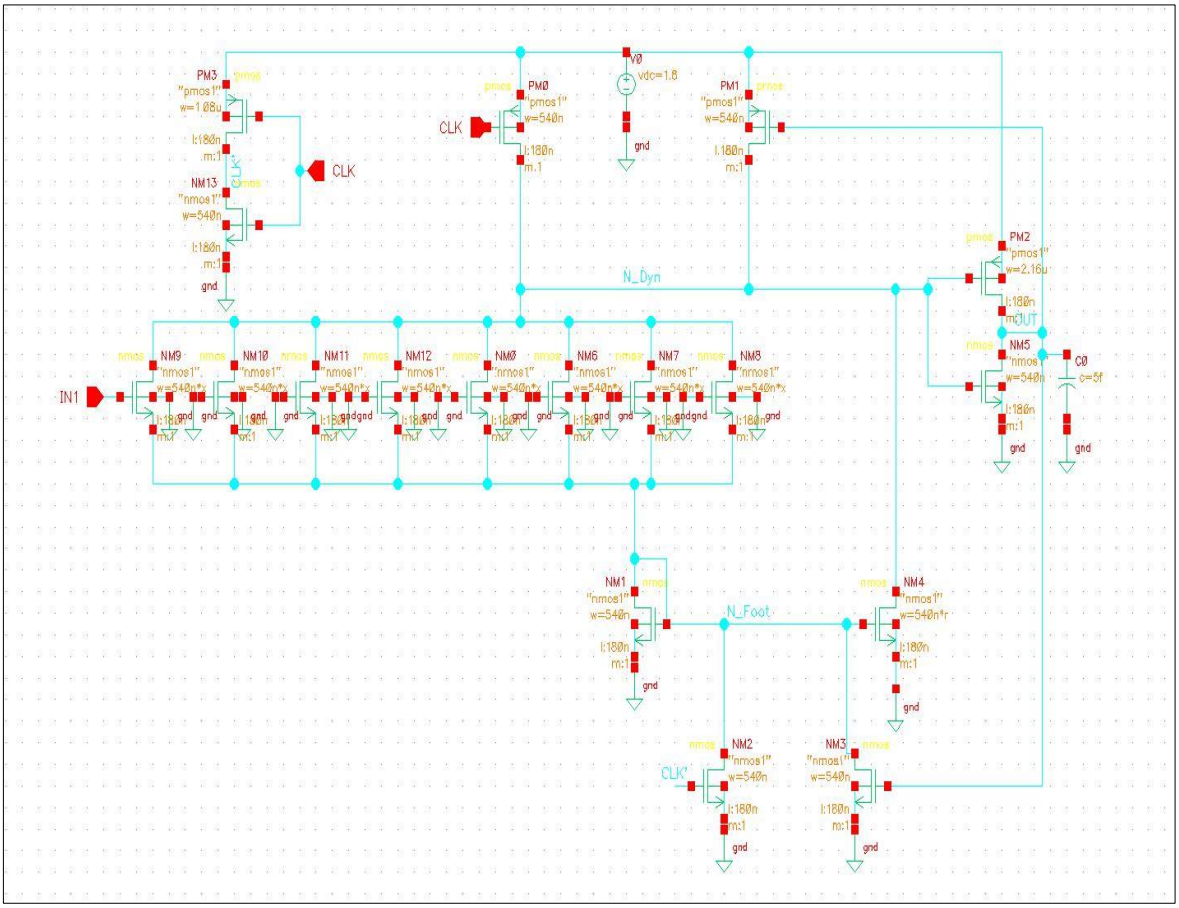

Figure 4.5: Schematic diagram of 8-bit OR gate realised using DFD.

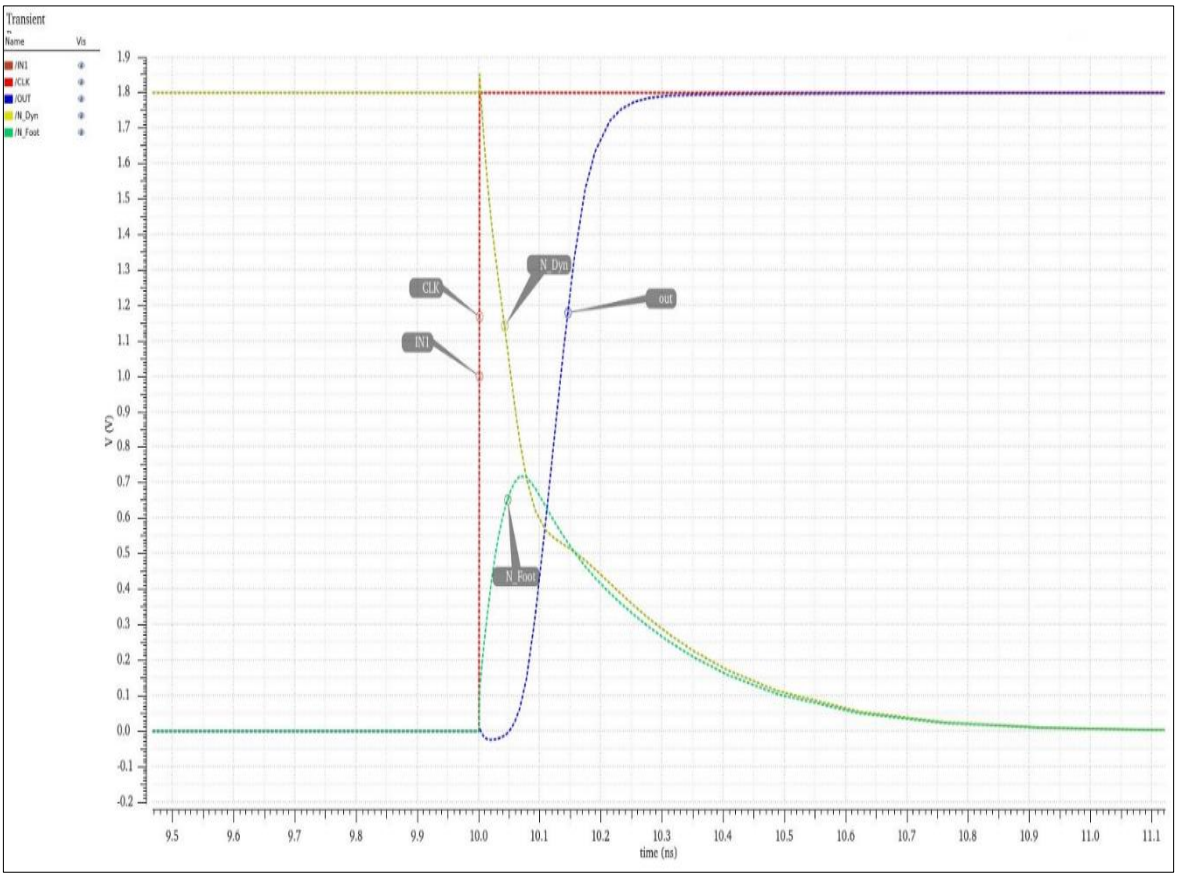

Figure 4.6: Simulated output waveform of 8-bit OR logic implemented using DFD.

Fan-in (delay)	W_{p1}	W_{keeper}	W_{M1}	$(W_{M2})_{Mirror\ transistor}$	W_{M3}
8-bit t_p=120ps	$3L_{min}$	$3L_{min}$	$3L_{min}$	$63L_{min}$	$3L_{min}$
Fan-in (delay)	W_{M4}	$(\frac{W_p}{W_n})_{Inverter}$	$(\frac{W_p}{W_n})_{Clock\ Inverter}$	W_{IN1}	
8-bit t_p=120ps	$3L_{min}$	$\frac{12L_{min}}{3L_{min}}$	$\frac{6L_{min}}{3L_{min}}$	$21L_{min}$	

Table 4.2: Size of all transistors used in implementing 8-bit OR gate using DFD.

4.2.3 High Speed Domino

Fig 4.7 and Fig. 4.8 portray schematic of high speed domino (HSD) based 8 bit OR gate and transient waveform obtained after simulation, respectively. The dimension of the keeper transistor M_k and transistors M_{n1} and M_{p1} are altered to accomplish given propagation delay. Table 4.3 gives the sizing of all transistors utilized in designing HSD.

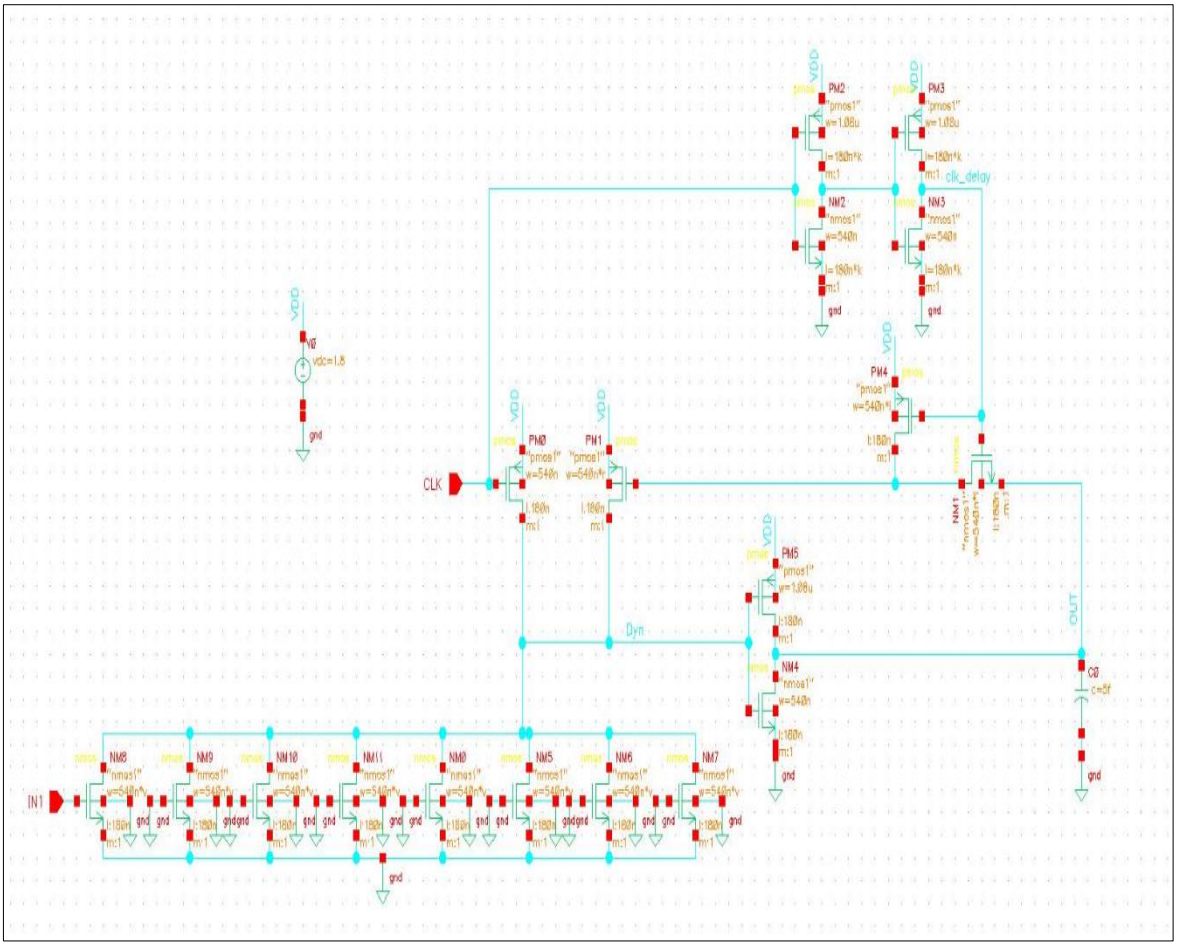

Figure 4.7: Schematic diagram of 8 bit OR gate realised using HSD.

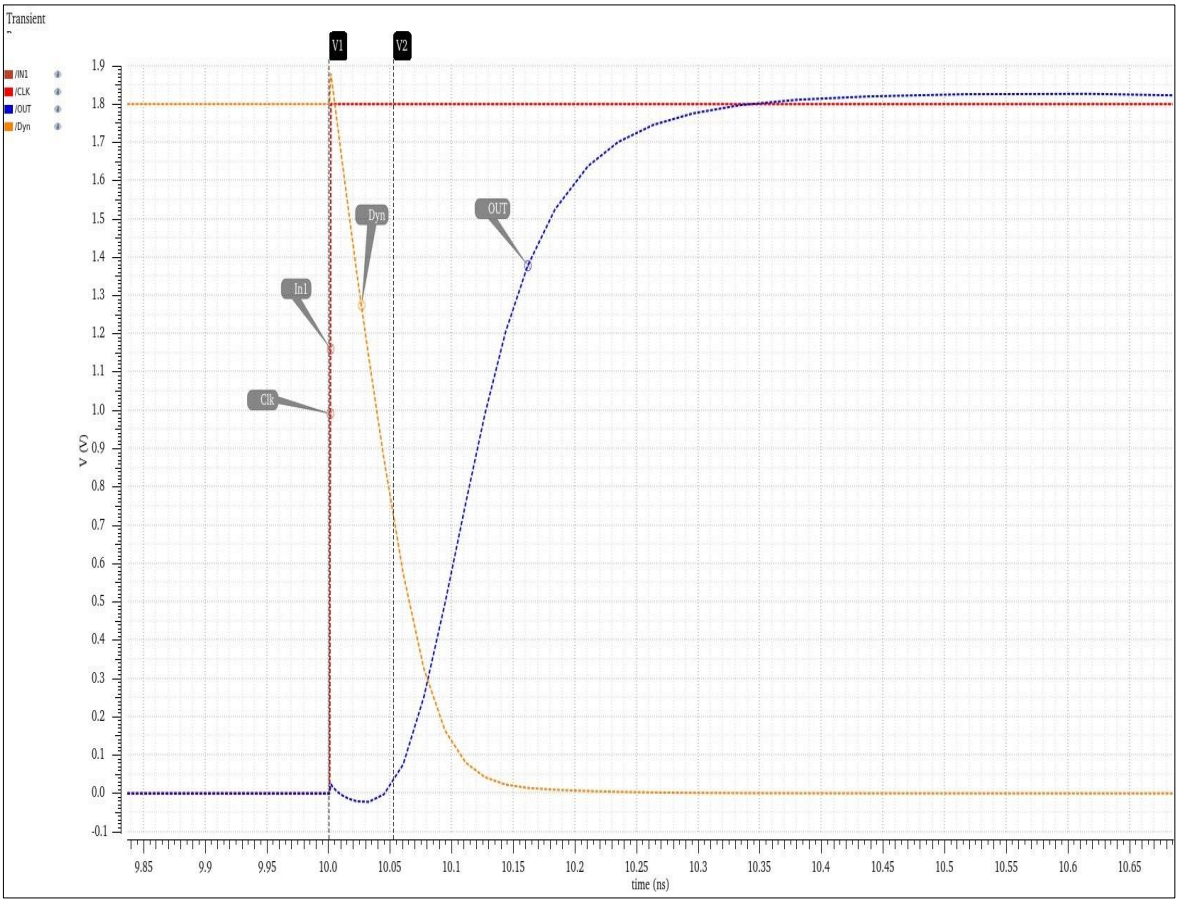

Figure 4.8: Simulated output waveform of 8-bit OR logic implemented using HSD.

Fan-in (delay)	W_{p1}	W_{N1}	W_{Q1}	W_{Q2}	$(\frac{W_P}{L_P})_{\text{Inverter 1}}$
8-bit t_p=120ps	$15L_{min}$	$15L_{min}$	$3L_{min}$	$27L_{min}$	$6L_{min}/5L_{min}$

Fan-in (delay)	$\left(\frac{W_N}{L_N}\right)_{\text{Inverter 1}}$	$(\frac{W_P}{L_P})_{\text{Inverter 2}}$	$\left(\frac{W_N}{L_N}\right)_{\text{Inverter 2}}$	$(\frac{W_P}{W_N})_{\text{Output Inverter}}$
8-bit t_p=120ps	$\frac{3L_{min}}{5L_{min}}$	$\frac{6L_{min}}{5L_{min}}$	$\frac{3L_{min}}{5L_{min}}$	$\frac{6L_{min}}{3L_{min}}$

Table 4.3. Size of all transistors used in implementing 8-bit OR gate using HSD.

3.2.4 Design presented in A. Kumar et. Al.

Fig 4.9 and Fig 4.10 portray the schematic and transient waveform of 8 bit OR gate realised using domino technique in refs. [1]. In order to attain preferred delay and high NI size of transistors in evaluation setup that are M_{n1} and M_{n2} varied. Along with that, the length of the keeper transistor is kept at a minimum. Length of transistor M_{n1} can be varied to overcome sub-threshold leakage current in PDN. Table 4.4 gives the sizing of all transistors utilized in designing an 8-bit OR gate using this technique.

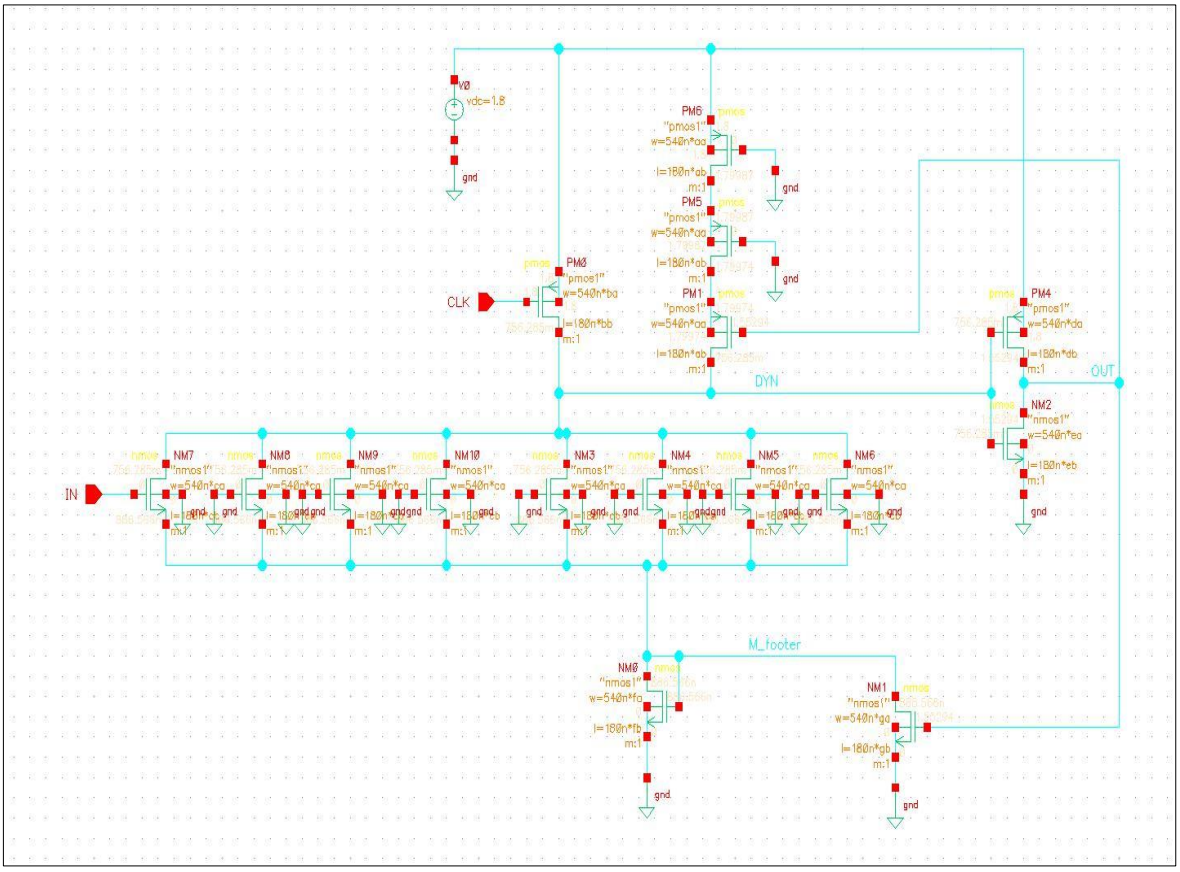

Figure 4.9: Schematic diagram of 8 bit OR gate realised using domino design proposed in A. Kumar et. Al.

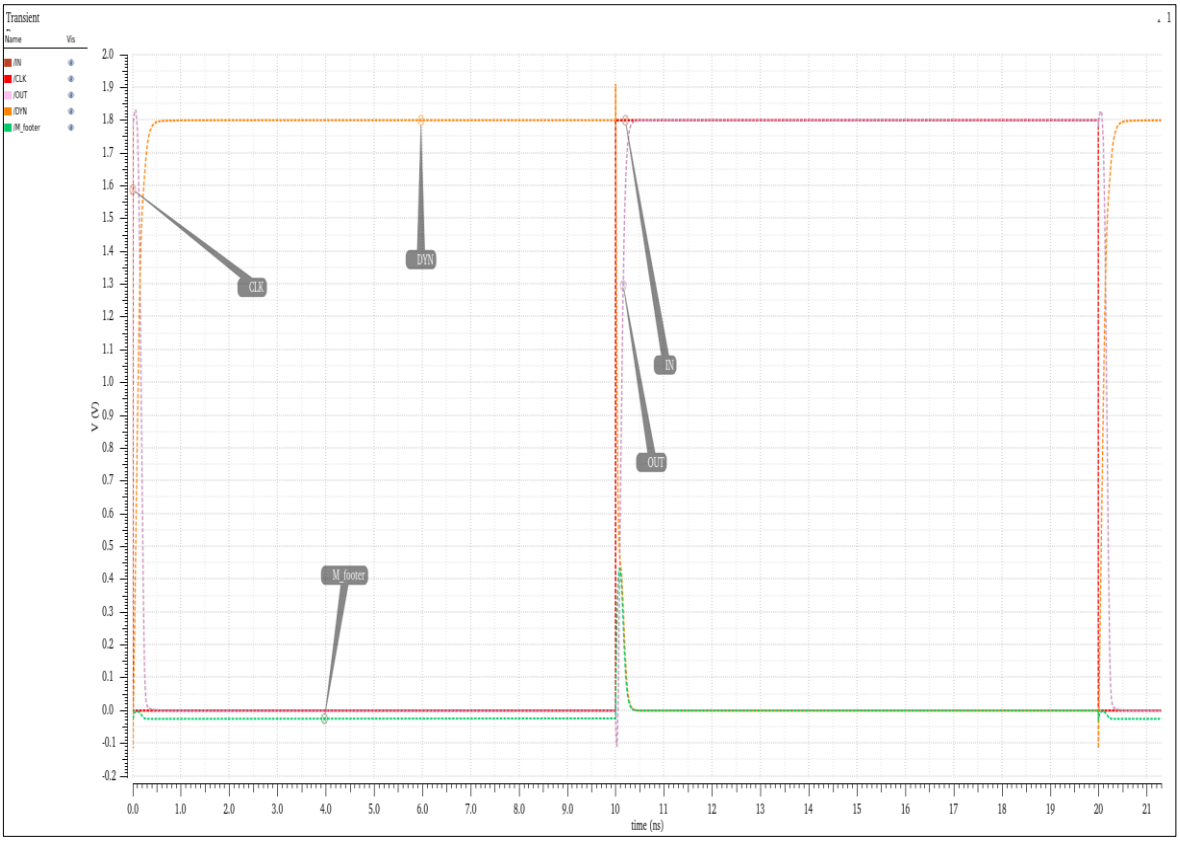

Figure 4.10: Simulated output waveform of 8 bit OR gate realised using domino design proposed in A. Kumar et. Al.

Fan-in (delay)	$(\frac{W}{L})_{k3}$	$(\frac{W}{L})_{k2}$	$(\frac{W}{L})_{k1}$	W_{pre}	W_{n1}
8-bit t_p=120ps	$3L_{min}/6L_{min}$	$3L_{min}/6L_{min}$	$3L_{min}/6L_{min}$	$10.5L_{min}$	$240L_{min}$

Fan-in (delay)	W_{n2}	$(\frac{W_p}{W_n})_{Inverter}$	W_{PDN}
8-bit t_p=120ps	$20.4L_{min}$	$\frac{7.5L_{min}}{3L_{min}}$	$15L_{min}$

Table 4.4: Size of all transistors used in implementing 8-bit OR gate using design given in A. Kumar et. Al.

3.2.5 Proposed Design

Generally, in a domino circuit transistor in the pull-down, evaluation and keeper setup are accountable for the delay, PD, and NI. Fig. 4.11 and Fig. 4.12 depict the schematic diagram and transient waveform of 8 bit OR gate realised via utilizing the proposed domino technique, respectively. In evaluation setup transistor M_2 offers a discharging pathway to node Dyn when at minimum one input is at logic 1. And transistor M_{d1} in a diode formation reduces leakage current in standby mode in the evaluation period. Current mirror transistor M_{m1} refill the dip in PDN current due to M_{d1}. So, the width of the transistor M_{m1} kept at high and, width and length of transistors M_2 and M_{d1}varied. In keeper circuitry, the size of the keeper transistor M_{k1} is kept at a minimum and of M_{k2} varied to attain anticipated delay (iso-delay i.e., 120ps). Table 4.5 gives the sizing of all transistors utilized in designing an 8-bit OR gate using this proposed design.

Fan-in (delay)	$(\frac{W}{L})_{k1}$	W_{k1}	W_p	W_{PDN}	W_{d1}
8-bit t_p=120ps	$6L_{min}/2L_{min}$	$3L_{min}$	$3L_{min}$	$18L_{min}$	$3L_{min}$

Fan-in (delay)	W_{m1}	$(\frac{W_p}{W_n})_{Inverter}$	W_1	$(\frac{W_p}{W_n})_{Clock\ Inverter}$	W_2
8-bit t_p=120ps	$57L_{min}$	$\frac{12L_{min}}{3L_{min}}$	$3L_{min}$	$\frac{6L_{min}}{3L_{min}}$	$3L_{min}$

Table 4.5: Size of all transistors used in implementing 8-bit OR gate using proposed Domino circuit.

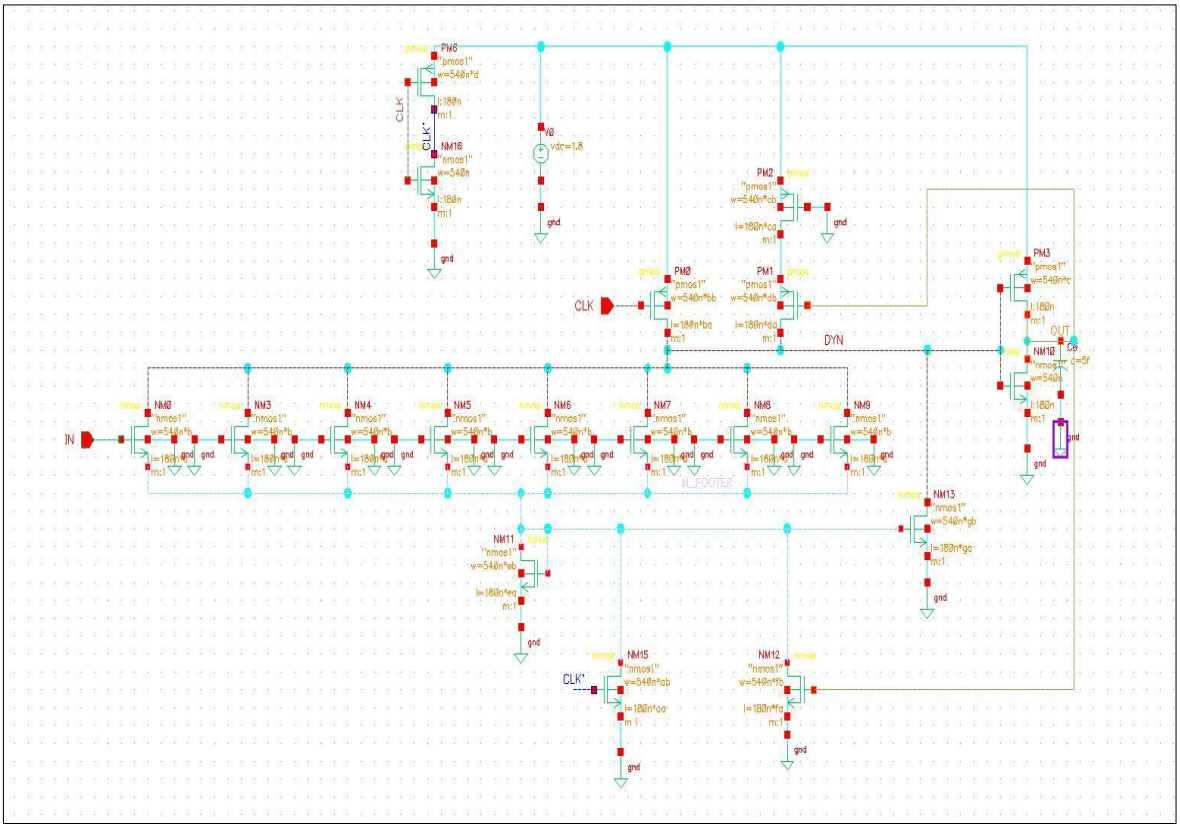

Figure 4.11: Schematic diagram of 8-bit OR gate implemented using proposed domino design.

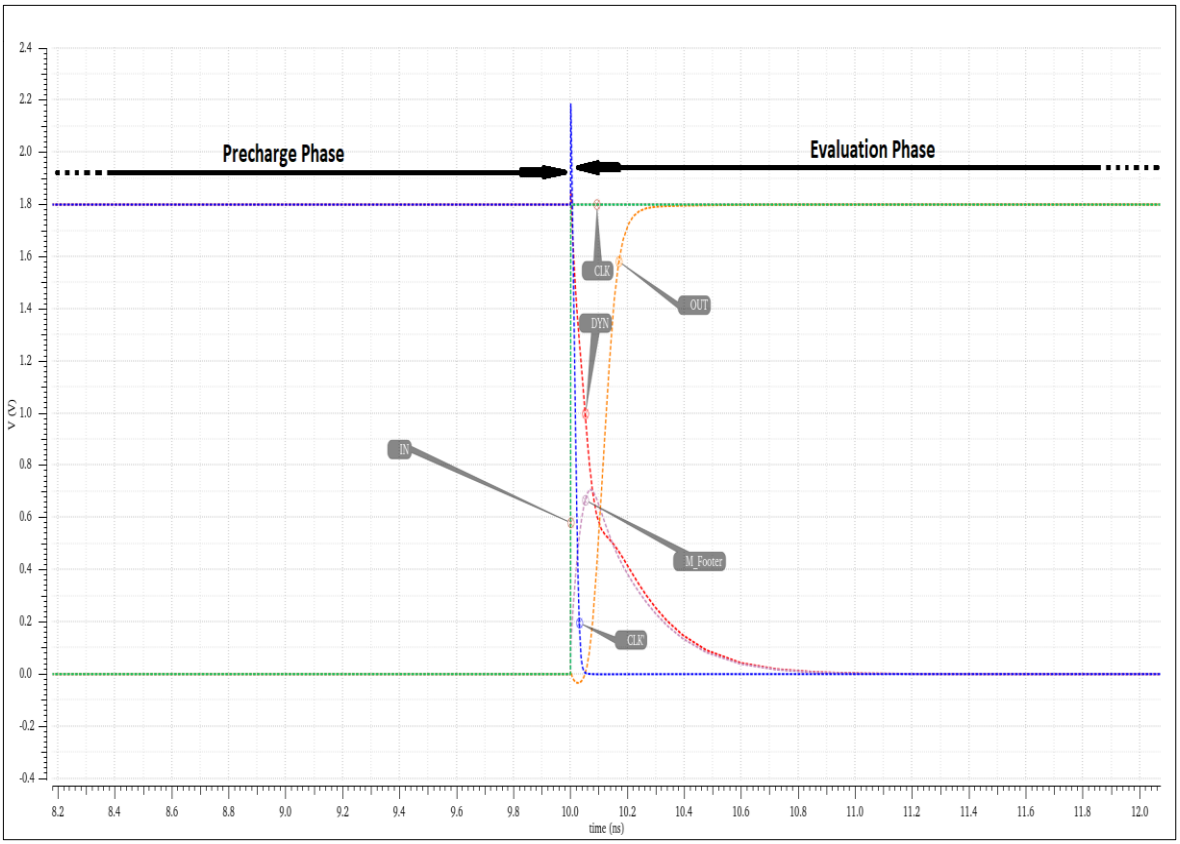

Fig. 4.12: Simulated output waveform 8-bit OR gate implemented using proposed domino design.

3.3 SIMULATION AND RESULTS

Simulated results demonstrations that the proposed domino design gives a substantial drop in PD and enhancement in noise margin at the cost of the increased number of transistors. Table 4.6 reveals the values of PD, UNM, and the number of transistors attained after simulating the 8-bit OR gate using all the above-discussed domino techniques and proposed design. Whereas, Fig. 4.13 shows the variation of normalized power dissipation and normalized delay at different process corners. Fig. 4.14-4.15 portrays the comparisons of conventional domino without evaluation transistor and proposed design for variations of normalized power dissipation with respect to node voltage and normalized delay with respect to temperature, respectively. Fig. 4.13-4.15 illustrates that the process variations are less in the proposed design. Whereas Fig.4.16-4.18 articulates graphical representation of normalized results illustrated in Table 4.6.

	Conventional domino without evaluation transistor [12]	Conventional domino with evaluation transistor [12]	High speed domino [10]	Diode footed domino [8]	Domino technique in refs. [1]	Proposed Domino design
Power dissipation (PD) (in µW)	66.52	49.41	23.58	15.95	49.12	12.36
Unity noise margin (UNM) (in V)	0.949	0.783	0.720	1.081	1.095	1.102
Total number of transistors used in designing 8-bit OR gate	12	13	18	18	16	19

Table 4.6. PD, UNG, and the number of transistors used for all simulated domino techniques in this work.

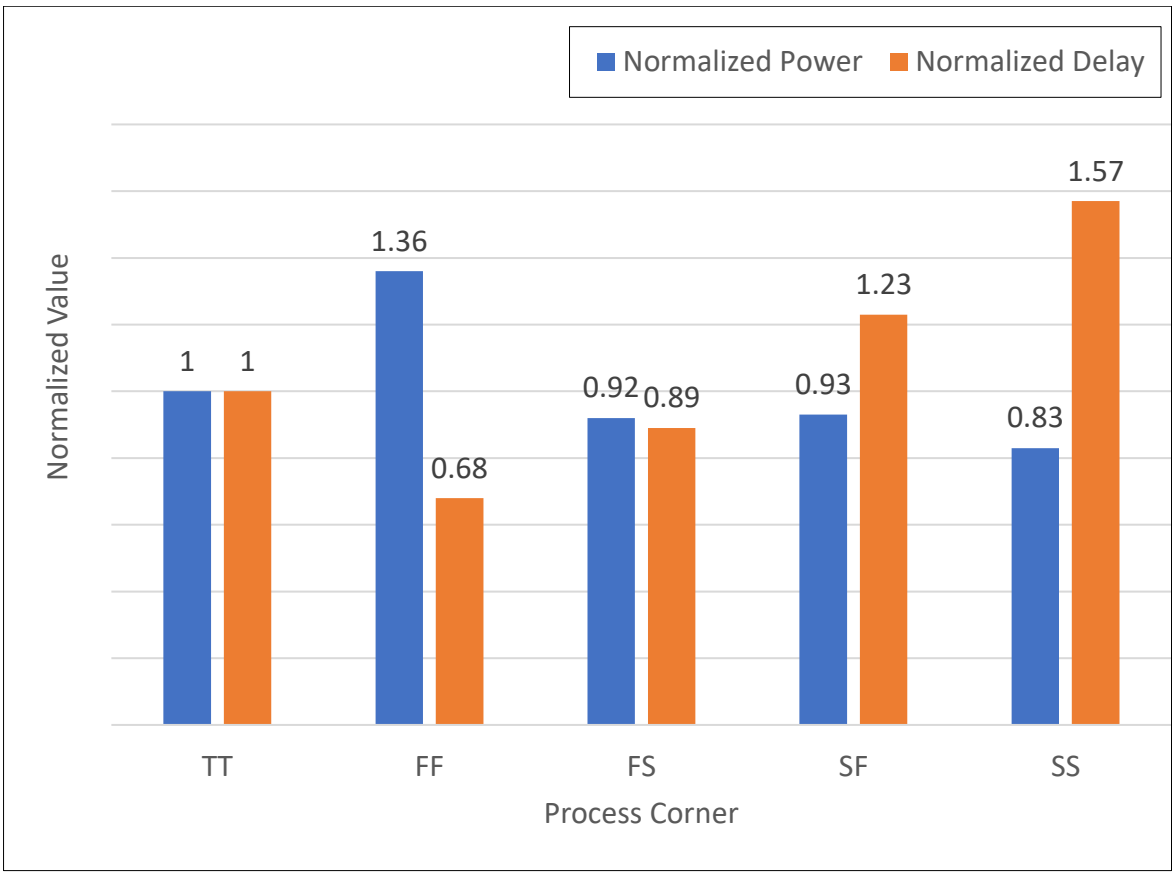

Fig. 4.13. Corner analysis for 8 bit OR gate realised via proposed design of normalized PD and normalized delay.

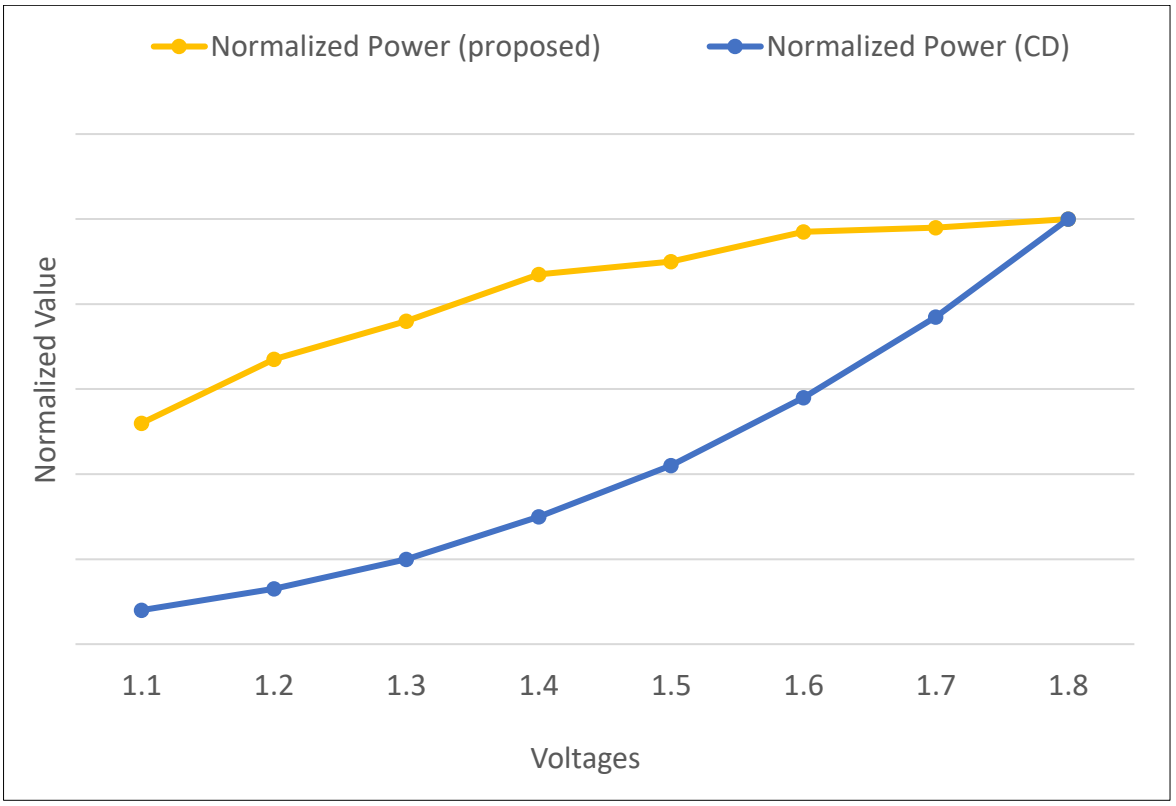

Fig. 4.14. Node voltages vs normalized PD graph for 8 bit OR gate realised via conventional domino without evaluation transistor and proposed domino technique.

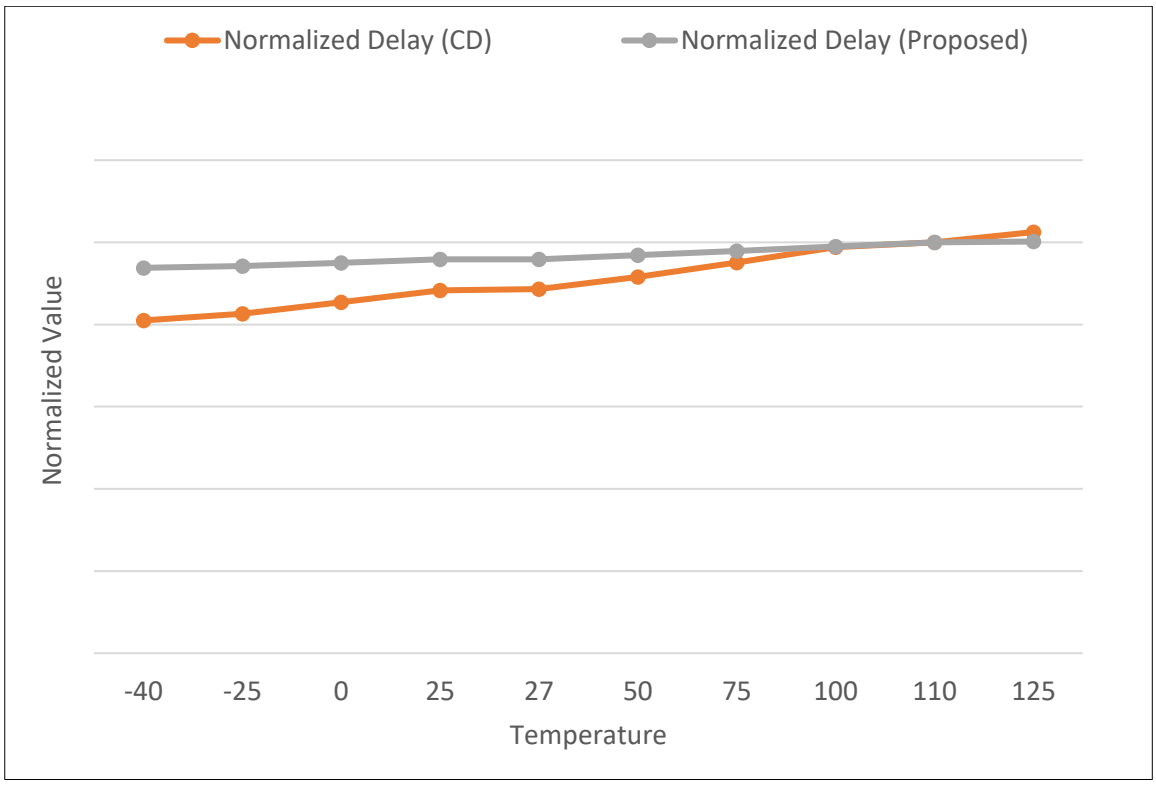

Fig. 4.15. Temperature vs normalized delay graph for 8 bit OR gate realised via conventional domino without evaluation transistor and proposed domino technique.

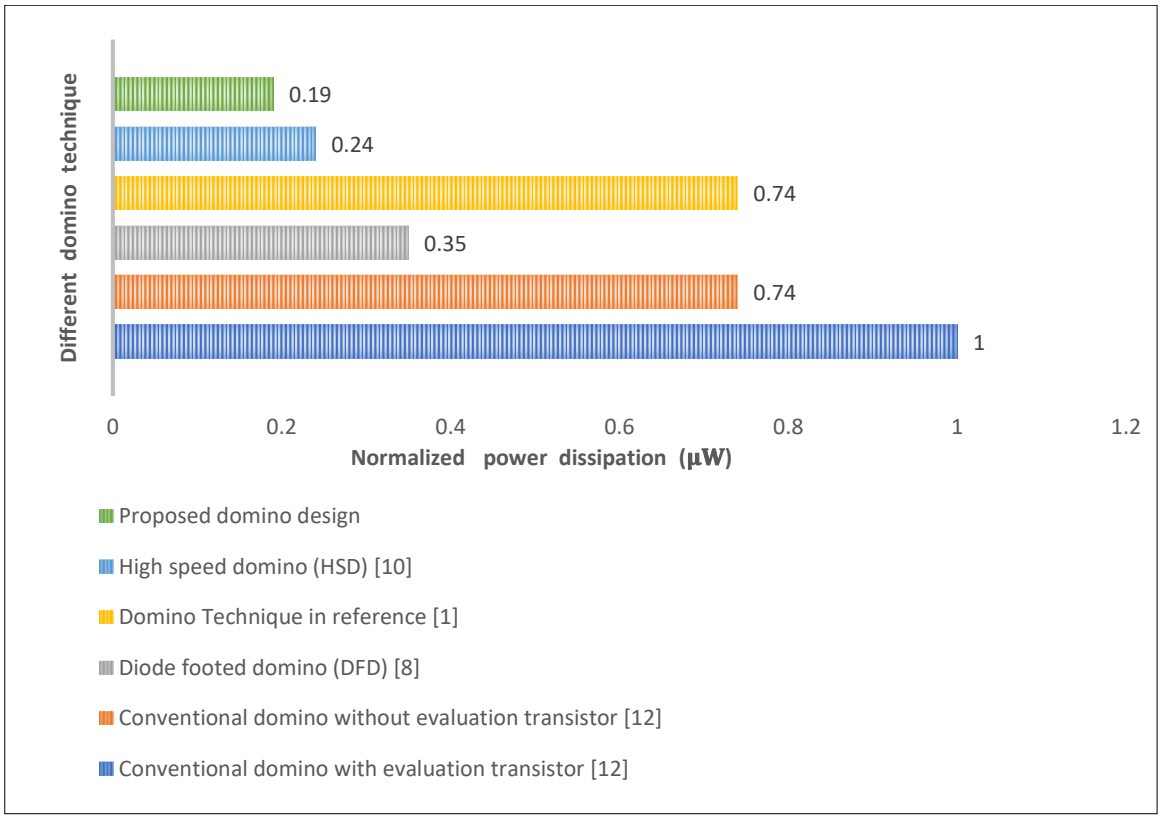

Figure 4.16: Evaluation of the normalized average PD of 8 bit OR gate realised via various domino circuit practices.

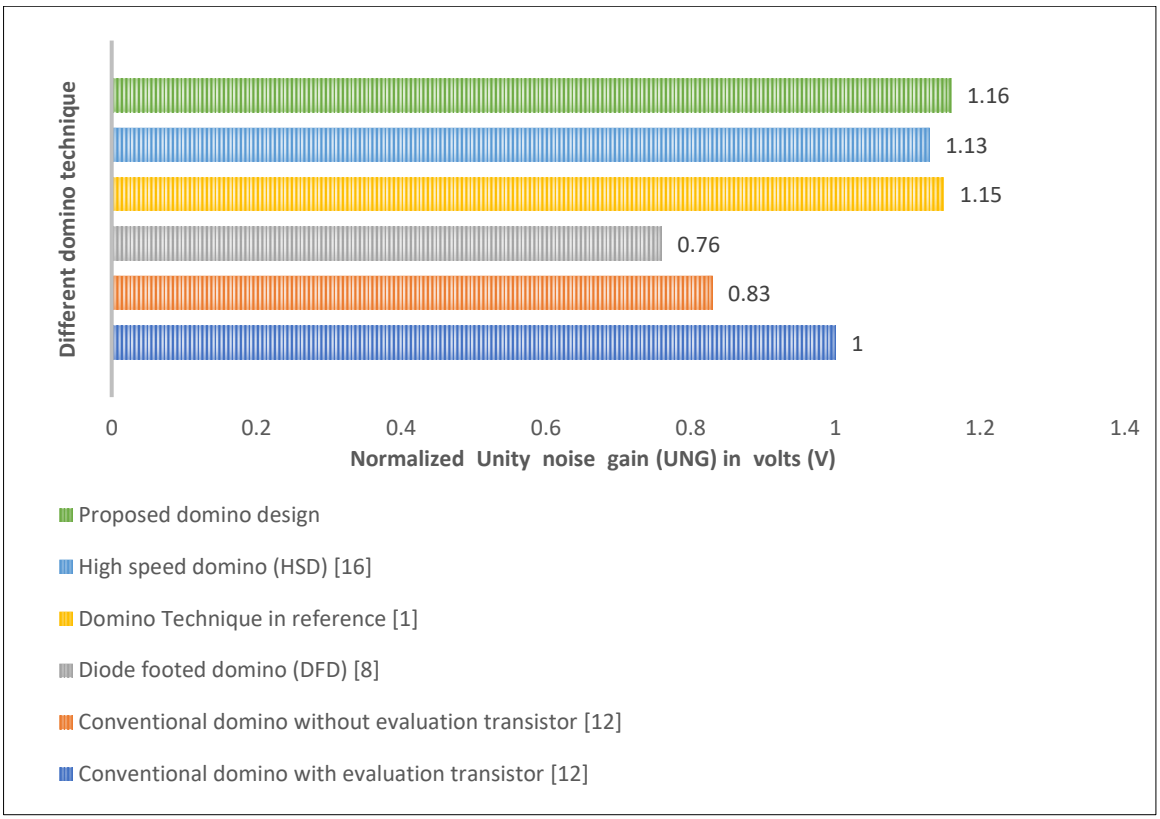

Figure 4.17: Evaluation of the normalized UNG of 8 bit OR gate realised via various domino circuit practices.

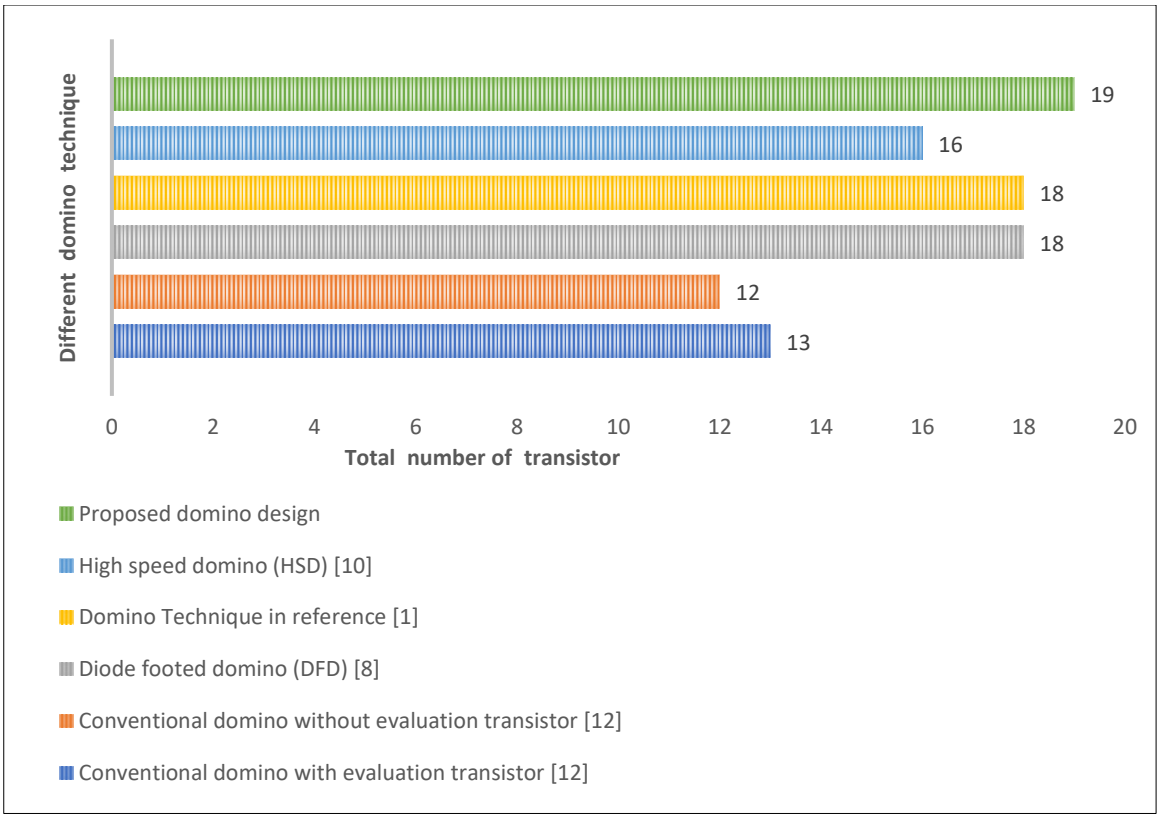

Figure 4.18: Evaluation of the whole sum of transistors utilized in 8 bit OR gate realised via various domino circuit practices.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION AND FUTURE SCOPE

In this work, different types of domino logic techniques have been discussed and a new type of domino design has been proposed. In the proposed design both evaluation and keeper setup have been remodelled in order to reduce power dissipation and process variations in delay, and enhance NI. 8-bit OR-gate has been designed and simulated in cadence virtuoso using standard domino with and without evaluation transistor , high speed domino (HSD) technique, diode footed domino (DFD) technique, technique given in A. Kumar et. Al. and proposed design, for same delay (i.e.,120ps iso-delay) to validate that the efficiency proposed design. Evaluation of all three performance parameters (that are PD, NI, and the number of transistors used in modelling 8-bit OR gate), illustrate that the proposed domino logic circuit gives the best results, with an 81.1% reduction in power dissipation and 56% improvement in noise immunity than conventional domino logic circuit. Also, process variations in delay and power have been trimmed down significantly in the proposed design. Therefore, this new technique can be used in designing modern high-speed dynamic circuits such as MUX, read path register, PLA, etc. Further research can be done in remodelling the circuitry to gate the power supply to decrease PD further for low-power VLSI circuits.

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APPENDIX 1: LIST OF PUBLICATIONS

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Jain College of Engineering
Belagavi, India

IEEE BANGALORE SECTION

2nd International Conference of Emerging Technology
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21st – 23rd May 2021

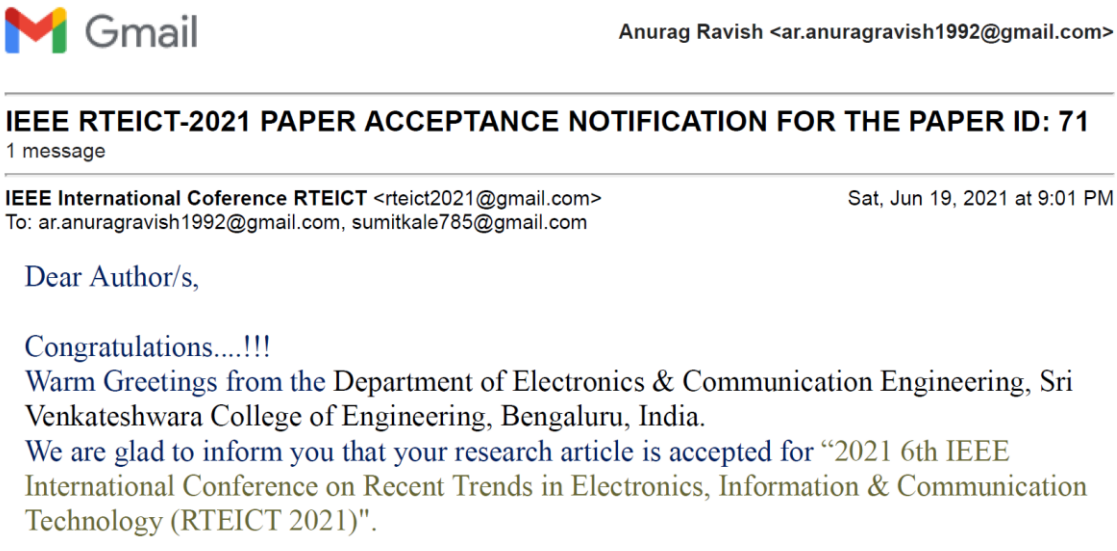
Certificate

This is to certify that Dr./Prof./Mr./Ms. ***Anurag Ravish*** *Affiliation Delhi Technological University has presented A Comparative Analysis of Domino Techniques for Improved Performance in 2nd International Conference of Emerging Technology (INCET 2021) during 21st to 23rd May 2021.*

Dr. Krupa Rasane
Convener INCET 2021

Dr. K. G. Vishwanath
General Chair - INCET 2021

[2] **Accepted**: Paper Id: 71, Conference - 6th IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT 2021)



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