# ANALYSIS AND CONTROL OF MULTILEVEL INVERTER FOR POWER QUALITY IMPROVEMENT

A Thesis Submitted in Partial Fulfillment of the Requirements for the Award of the Degree of

**DOCTOR OF PHILOSOPHY**

**Submitted by**


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# DECLARATION

I hereby certify that the work which is presented in this thesis entitled "**Analysis and Control of Multilevel Inverter for Power Quality Improvement"** submitted in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy in the Department of Electrical Engineering, Delhi Technological University, Delhi. This is an authentic record of my own work carried out under the supervision of Dr. Alka Singh. The matter presented in this thesis has not been submitted elsewhere for the award of a degree

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Date: __/__/____

# CERTIFICATE

On the basis of candidates' declaration, I hereby certify that the work which is presented in this thesis entitled "**Analysis and Control of Multilevel Inverter for Power Quality Improvement"** submitted to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy, is an original contribution with the existing knowledge and faithful record of the research work carried out by him under my guidance and supervision.

To the best of my knowledge, this work has not been submitted in part or full for the award of any degree elsewhere

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# ABSTRACT

Modern power distribution systems face two challenges from increasing electronic-based loads and integrating renewable energy sources. Distribution networks experience problems with current-based power quality as a result of these power-related electronic devices. Power quality problems include issues like poor power factor, load imbalance, harmonics in the supply current, voltage regulation, and others. To mitigate these issues, a shunt active power filter (SAPF) is used. This can be done by a number of controllers. In the case of a normal grid condition, the unit-in-template approach can be utilized to extract the synchronization signals. When the grid deteriorates due to voltage sag, swell, distortion, and DC offset problems present in the grid. Therefore, it is also essential to employ effective PLL algorithms to estimate synchronization template signals..

The grid-connected system is connected to the point of common coupling (PCC) via a voltage source converter, and the non-linear loads are also connected. Due to their efficiency and compactness, the power electronic-based loads are growing every day. Reactive power is drawn by the non-linear loads, which lowers the quality of the power and introduces harmonics into the system, which increases losses. To address the aforementioned problems, SAPF is built and configured to perform power factor correction, reactive power compensation, and harmonic mitigation. In order to enhance the power quality in distribution systems, it is advised to comply to a range of international standards based on IEEE and IEC. IEEE-519 standards for grid current harmonic mitigation should be followed. According to the IEEE-519 standard, the Total Harmonic Distortion Factor in grid current should be less than 5%. In addition, the IEEE-1547 standard mentions the allowable harmonic content that can be injected by PV systems when connected to the grid.

In this thesis work, the SAPF is created for single-phase distribution systems utilizing Matlab Simulink software. Dynamic load conditions evaluate the effectiveness. In a single-phase system, a 5-level cascaded H-Bridge Multilevel Inverter replaces the standard 2-level inverter. MLI has a number of benefits over a normal 2-level inverter since it switches operated at a lower frequency and experiences fewer switching losses. The harmonic content decreases as the number of levels rises. The CHB-MLI system has the necessary flexibility

thanks to its modular design. A phase-shifted pulse width modulation technique produces the gate pulses by comparing the generated reference currents with the actual supply current signals.

The performance of the SAPF is dependent on the different control algorithms used to extract the harmonics from the non-linear load current. In the literature, various conventional and adaptive control techniques are addressed. The performance of the control algorithm is assessed using a number of important considerations, such as the degree of computational complexity, the degree of filtration, oscillations, overshoot, settling time, mean square error, phase-locked loop (PLL) requirement, memory requirement, and the THD obtained in grid current and convergence behavior of fundamental load current under dynamic conditions. To enhance the power quality of distribution networks, SAPF needs to be appropriately controlled for further processing and control. Its controller is based on extracting the fundamental component of load current for the generation of reference current. This thesis involves designing new control algorithms to retrieve the fundamental load current component. This study proposes, develops, and tests a variety of control algorithms.

The SAPF efficiency is also impacted by how precisely the control algorithm extracts the reference current and compensates for the harmonics produced by the load. The areas of active noise cancellation, signal enhancement, noise filtering, echo cancellation, etc., have all been covered by adaptive signal processing techniques over the past few decades. Least Mean Square (LMS), Synchronous Reference Frame Theory (SRFT), and Notch Filter are common algorithms used for the estimation of fundamental component of load current components. A method of parallel tangent (PARTAN-LMS) algorithm has been developed to operate under distorted grid conditions, and some advanced adaptive control algorithms, such as Normalized Least Mean Absolute Third (NLMAT), Normalized Huber (NHuber), and Robust Shrinkage Affine Projection Sign Algorithm (RSAPS), have also been implemented.

The grid must be synchronized with power electronic converters for effective control. The voltage-based electrical quality of Indian systems can occasionally be problematic. Harmonics, phase angle jumps, frequency shifts, voltage sag, swell, and DC offset are

common issues with voltage signals used for synchronization. To resolve these voltage-based power quality problems, open-loop and closed-loop synchronization approaches can be applied. Phase-locked loops are a frequently employed part of synchronization techniques. The phase-locked loop technique is required for quick and accurate detection of the grid phase angle and frequency for integration. The chosen method of synchronization has an impact on the stability and accuracy of the control system. Grid collapse could result from inaccurate PLL information. It is necessary to look for an appropriate PLL that can be applied in real-time, has a simpler structure, and can address the weak grid problems. For the 5-Level CHB-MLI controller to operate, the synchronization controller also keeps track of grid voltage, phase, and frequency information.

This thesis presents three grid-synchronization techniques for single-phase systems: Synchronous Reference Frame Theory (SRF-PLL), Second Order Generalized Integrator (SOGI-PLL), and Third Order Sinusoidal Integrator (TOSSI-PLL). SRF-PLL is the traditional and frequently employed PLL under typical circumstances. However, this PLL does not accurately track frequency and phase angle when the grid is distorted. Therefore, finding alternatives to SRF-based PLLs is essential. For handling various grid anomalies, orthogonal signal generator (OSG) based PLL has been widely used and implemented in recent years.

Additionally, compared to SRF-PLL, its tracking capability is quite good and accurate. The most commonly used OSG- PLL is SOGI-PLL, but its performance deteriorates especially in DC-offset conditions; therefore, one more PLL, i.e., TOSSI-PLL, has been implemented to tackle grid abnormalities which exhibits good performance as compared to SRF-PLL and SOGI-PLL. The findings of extensive mathematical modeling, simulations and experiments have been presented in this thesis. The effectiveness of the synchronization algorithms has been demonstrated through simulation and experimental testing under various grid voltage conditions such as voltage sag and swells, phase shift, and DC offset and also tested under sudden load variations

In grid-connected systems, photovoltaic (PV) based voltage source converters (VSC) serve the dual purposes of bidirectional active power transfer to the grid and load. They can be controlled to achieve grid current balancing, harmonic reduction, reactive power balance,

and improvement of the supply side power factor to unity. The PV source can be integrated through a DC-DC boost converter using the double-stage topology, or it can be linked directly to the VSC at its DC link using the single-stage topology. Fewer devices are required in a single stage, and it offers improved control. Additionally, because of independent Maximum Power Point Tracking, it has an increased operation region and more flexibility. In this thesis, a single-stage, single-phase grid-connected system has been presented. The PV arrays are connected to the DC link side of the 5-Level CHB-MLI. The proposed system can operate in two modes, day and night. During the day, the active power is injected into the grid, and during the night, the solar arrays are disconnected; the SAPF will do the harmonics compensation and make the system power factor unity. The system is tested under distorted grid conditions. Two PLLs viz. SRF-PLL and Modified Notch Filter SOGIPLL (MNFSOGI-PLL) is implemented to generate the unit template and reference current. The SRF-PLL fails to work in distorted grid conditions, but MNFSOGI-PLL exhibits good performance under the distorted grid, especially to handle DC offset. To enhance the quality of the power, offer reactive power compensation, and inject active power into the grid, these system configurations will be implemented and analyzed using simulation models and experimental prototypes.

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| | |
|---|---|
| $V_g/V_s$ | Grid/source voltage |
| $i_g/i_s$ | Grid/source current |
| $i_L$ | Load current |
| $i_c$ | Compensating current |
| $V_{dc\text{-}ref}$ | Reference DC link voltage |
| $V_{dc1}$ | DC link voltage across capacitor-1 |
| $V_{dc2}$ | DC link voltage across capacitor-2 |
| $V_{dc}$ | DC link voltage |
| $f_{sw}$ | Switching Frequency |
| $\Delta I_{cr-pp}$ | Peak to Peak ripple current |
| m | Number of voltage levels |
| $m_f$ | Modulation index |
| $i_s$ | Source current |
| $i_s$* | Reference supply current |
| $f_{cr}$ | Carrier frequency |
| $f_m$ | Modulating Frequency |
| $v_{sp}$ | In-phase component |
| $v_{sq}$ | Quadrature component |
| $w_{avg}$ | average weight |
| $k_d$ | Proportional gain |
| $k_i$ | Integral gain |

| | |
|---|---|
| $w_p$ | Fundamental component of load current |
| $w_{eff}$ | Effective average weight |
| $u_p$ | Unit vector template |
| $\theta$ | Actual phase angle |
| $\hat{\theta}$ | Estimated phase angle |
| $\omega_{eff}$ | normal grid frequency |
| $\hat{\omega}$ | estimated frequency |
| $A_v$ | amplitude of grid voltage |
| $\Delta f$ | Difference between estimated and actual frequency |

# LIST OF SYMBOLS

| | |
|---|---|
| PQ | Power Quality |
| PCC | Point Of Common Coupling |
| VSC | Voltage Source Converters |
| SAPF | Shunt Active Power Filter |
| DSTATCOMs | Distribution Static Compensators |
| DVRs | Dynamic Voltage Restorers |
| UPQCs | Unified Power Quality Conditioners |
| CHB-MLI | Cascaded Multilevel Inverter |
| MLI | Multilevel Inverter |
| PWM | Pulse Width Modulation |
| PS-PWM | Phase Shift Pulse Width Modulation |
| THD | Total Harmonic Distortion |
| LMS | Least Mean Sqaure |
| SRFT | Synchronous Reference Frame Theory |
| OSG | Orthogonal Signal Generator |
| PLL | Phase Lock Loops |
| SOGI | Second –Order Generalized Integrator |
| TOSSI | Third-Order Sinusoidal Signal Integrator |
| PARTAN-LMS | Parallel Tangent Least Mean Square |
| MNFSOGI | Modified Notch Filter Second –Order Generalized Integrator |

# Chapter 01

# Introduction

## 1.1 General Introduction

In the past, electricity was mainly produced using centralized, massive power plants typically placed far from the load or consumer centers and adjacent to the primary energy source (for example, coal mines).Traditional fossil fuels like coal, gas, or oil were used to generate electricity in thermal power stations, which had huge revolving generators. A passive network of lengthy transmission lines is used to transport the generated electricity. In the end, the client receives electricity through the (radial) distribution network. In such a system, power only flowed in one direction: from the generating station to the customers. Furthermore, because there were hardly any nonlinear loads in the utility, the problem with power quality (particularly distortion of the voltages/currents) was not as severe.

There has been a significant drift from this tendency over the past two decades. The depletion of fossil resources, decreased efficiency owing to transmission over great distances, and the high expense associated with enhancing transmission capability are the causes of the drift. This trend has also been significantly influenced by growing environmental concerns about centralized power plants' hazardous and greenhouse emissions. These problems can be addressed using renewable energy sources based on electrical generation, such as wind, solar, fuel cells, etc. In contrast to centralized power plants, localized energy generation, or producing energy locally to load centers, is an option. There is no longer a state monopoly, and the generating unit's generation capacity can range from a few kW to several MW. In addition to environmental regulations and technical advancement, deregulation has significantly altered the structure of generating, transmission, and distribution and brought about new circumstances in the electricity generation industry. Several new technologies are presently used for electricity generation.

## 1.2 Modern Distribution System and Power Quality

Electric Power Quality (PQ) is a word used to describe how vital power is generated, transmitted, distributed, and utilized in AC electrical systems [4,5]. The AC supply systems can become contaminated for various reasons, including natural ones like lightning, flashovers, equipment failure, and faults and induced ones such as voltage distortions and notches**.** Different customer devices, which draw non-sinusoidal current and act as nonlinear loads, also contaminate the supply system. Due to the risk of equipment failure or malfunction, power quality is often measured in terms of voltage, current, or frequency variation of the supply system [6]. The existence of voltage harmonics, surge, spikes, notches, sag/dip, swell, imbalance, fluctuations, glitches, flickers, outages, and other issues are typical power quality issues related to the voltage at the Point of Common Coupling (PCC) where multiple loads are connected. Due to various system disturbances or the existence of different nonlinear loads like furnaces, uninterruptible power supplies, and variable speed drives, these issues are prevalent in the supply system. However, some power quality issues with current drawn from the AC mains include low power factor, reactive power load, harmonic currents, unbalanced currents, and an excessive neutral current in poly-phase systems because of imbalance and harmonic currents produced by some nonlinear load. These power quality issues result in a capacitor bank failure, a higher distribution system, electric machine losses, noise, vibrations, overvoltages, excessive current due to resonance, etc. Several methods have been developed to mitigate these issues in existing systems and technology that will be developed soon [7]. The design and development engineers working in the fields of power electronics, power systems, electric drives, digital signal processing, and sensors have opened up a new path for research and development (R&D) activities. According to the nature of the loads, such as voltage-fed loads, current-fed loads, or a combination of both, a series of power filters are of various types, such as passive, active, and hybrid in shunt, series, or a combination of both configurations are used externally to mitigate these problems in existing nonlinear loads. Custom power devices, such as Distribution Static Compensators (DSTATCOMs), Dynamic Voltage Restorers (DVRs), and Unified Power Quality Conditioners (UPQCs) [8] are used for mitigating current, voltage, or

both types are used to mitigate current, voltage, or both types of power quality issues.

## 1.3 State of Art

Increasing power electronic-based loads and integrating renewable energy sources present significant problems for modern power distribution systems. These power-related electronic devices cause current-based power quality issues in distribution networks. Poor power factor, load imbalance, harmonics in the supply current, voltage regulation, etc., are prominent power quality issues. The shunt active power filter (SAPF) reduces these problems. Several controllers can accomplish this task. The unit-in-template approach can be used to extract the synchronization signals; this method works well in the case of normal grid conditions. However, voltage sag, swell, distortion, and DC offset issues might occur when the grid weakens. Consequently, efficient PLL techniques are also required to be used for estimating synchronizing template signals.

In grid-connected systems, photovoltaic (PV) based voltage source converters (VSC) serve the dual purposes of bidirectional active power transfer to the grid and load. They can be controlled to achieve grid current balancing, harmonic reduction, reactive power balance, and improvement of the supply side power factor to unity. The PV source can be integrated through a DC-DC boost converter using the double-stage topology, or it can be linked directly to the VSC at its DC link using the Single Stage Topology. In the literature, various MPPT methods that help maximize the power from the PV array are discussed, including Incremental Conductance and Perturb and Observe algorithms.

At the point of common coupling(PCC), using a voltage source converter, the PV source and nonlinear loads are also connected to the grid. These power electronic-based loads are preferred due to their compactness and higher efficiency. The nonlinear loads draw reactive power, degrading the power's quality and injecting harmonics into the system, which raises losses. SAPF is designed and controlled to perform power factor correction, reactive power compensation, and harmonic mitigation to resolve the above-mentioned issues. It is recommended to follow various international standards based on IEEE and IEC to improve the power quality in distribution systems. Grid current

harmonic mitigation should comply with IEEE-519 standards. According to the IEEE-519 standard, the Total Harmonic Distortion Factor in grid current should be less than 5%. In addition, the IEEE-1547 standard mentions the allowable harmonic content that can be injected by PV systems when connected to the grid.

The SAPF is developed using Matlab Simulink software for single-phase distribution systems in this work. Dynamic load conditions are simulated to analyze the performance of the system. The conventional 2-level inverter is replaced in a single-phase system with a 5-level cascaded H-Bridge Multilevel Inverter. MLI provides various advantages w.r.t to traditional 2-level inverters, as it operates at a low switching frequency and reduces switching losses. As the number of levels increases, the harmonic content is reduced. The modular design of CHB-MLI provides the required flexibility in the system. A phase-shifted pulse width modulation scheme generates the gating pulses by comparing the generated reference currents with the actual supply current signals.

The SAPF's performance is based on various control algorithms employed to extract the harmonics from the nonlinear load current. The literature survey discusses different traditional and adaptive control algorithms. The evaluation of the control algorithm's performance is based upon a variety of critical factors, including the degree of computational complexity, the degree of filtration, oscillations, overshoot, settling time, mean square error, phase-locked loop (PLL) requirement, memory requirement, and the THD obtained in grid current and convergence behavior of fundamental load current under dynamic conditions.

SAPF needs to be appropriately controlled for further processing and control. Its controller is based on extracting the fundamental component of load current for current reference generation. This study involves designing new control algorithms to retrieve the fundamental component of load current. This study proposes, develops, and tests a variety of control algorithms.

The effectiveness of SAPF also depends upon how accurately the control algorithm extracts the reference current and compensates for the harmonics generated by the load. Various time and frequency domain algorithms have been presented in the literature viz; Synchronous Reference Frame Theory, Instantaneous Reactive Power Theory, Second Order Generalized Integrator, etc. These are time-based conventional algorithms. Some

other time domain algorithms, such as Composite and model observer-based algorithms, Kernel incremental learning algorithms, perform well but require tuning several parameters, substantially high arithmetical operations, and additional filters. Besides, various frequency-domain algorithms such as Kalman Filter; Fourier transforms; have also been implemented to control SAPF and distribution static compensator (DSTATCOM).

Over the last few decades, adaptive signal processing techniques have covered various fields such as active noise cancellation, signal enhancement, noise filtering, echo cancellation, etc. Due to its simple structure, the most common adaptive algorithm is the Least Mean Square (LMS), Normalized LMS (NLMS); Recursive LMS (RLMS); Variable Step Size (VSS) LMS (VSSLMS); Least Mean Fourth (LMF) Algorithm, Leaky Least Mean Fourth Algorithm, LMS-LMF, Normalized Least Mean Fourth, Weiner Filter and Adaptive Neuro-Fuzzy Inference system based LMS. Some advanced adaptive control algorithms, such as Normalized Least Mean absolute third (NLMAT), Normalized Huber (NHuber), and Robust Shrinkage Affine Projection Sign Algorithm (RSAPS), are also developed and discussed in this thesis. However, most conventional algorithms have been applied to a single-phase H-bridge conventional 2-level inverter.

For effective control, power electronic converters must be synchronized with the grid. Indian grids have issues, and typical problems include voltage sag, swell, harmonics, phase angle jumps, frequency changes, and DC offset. Both open-loop and closed-loop synchronization techniques can be used to overcome these synchronizing problems. Phase-locked loops are commonly used components of synchronization methods. The phase angle and frequency of the grid must be quickly and precisely detected by selecting the phase-locked loop method. The synchronization method affects the control system's stability and precision. Inaccurate PLL information may even lead to grid collapse. Appropriate PLL techniques must be searched, and preferably, they should have a simplified structure and be implemented easily in real time. Synchronization technique in the form of a Phase Locked Loop plays an essential role in synchronization during the grid-connected mode. The synchronization controller tracks the information of grid voltage, phase, and frequency for the working of the 5-Level CHB-MLI controller also. In addition, their aspects are also discussed in this

thesis.

Various PLLs, such as Synchronous Reference Frame Theory (SRFT), are studied and developed in the literature. SRF-PLL is widely used and performs well in normal conditions. But under distorted grid conditions, this PLL does not track frequency and phase angle accurately. Hence, it is essential to find alternatives to SRFT-based PLLs. In recent years, orthogonal signal generator (OSG) based PLL has been widely used and implemented to handle various grid abnormalities. Also, its tracking performance is quite good and accurate compared to SRF-PLL.The most commonly used OSG- PLL is generalized sinusoidal integrator (SOGI-PLL), and other PLLs discussed in the literature are Cascaded Generalised Integrator (CGI) PLL, Second Order Generalised Integrator Fuzzy Logic Controller (SOGI-FLL), Mixed Second- and Third-Order Generalized Integrator (MTOGI), Discrete Fourier Transform, Notch Filter and Kalman Filtering, Enhanced Third-Order Generalized Integrator PLL, Modified SOGI-FLL and zero-crossing detector, Adaptive spline-based PLL, MNF-SOGI, DSOGI, ISOGI, Digital Phase-Locked Loop and Gradient Descent Least Squares Regression Based Neural Network which has been had been discussed in recent years. PLLs such as SRFT, SOGI, MNF-SOGI, and TOSSI have been developed and tested in this thesis work on the CHB-MLI system.

## 1.4 Scope of Work

Based on the exhaustive literature review on the design, control, and analysis of the grid-tied system with and without PV. It has been identified that the conventional 2-level inverter cannot perform well, especially in the case of medium voltage (MV) and high voltage(HV) systems. In that case, the multilevel inverters are required to handle MV and HV with less PIV rating, dv/dt stress, low electromagnetic interference, etc. In addition, the significant role of selecting the control algorithms is essential to mitigate the harmonics generated by the nonlinear load. The chosen control algorithm should be fast under dynamic conditions, have zero-steady state error, and robust performance without increasing the algorithm's complexity.

In case of distorted grid conditions, selecting appropriate synchronization techniques

is crucial to consider variation in grid parameters and estimate the fundamental component of nonlinear load current suitably. One of the objectives of the proposed research work is to design and develop MLI based single-phase grid-tied with and without PV systems in the laboratory to improve the various power quality issues. A detailed description of the proposed work in this thesis is as follows:

- **Designing and Development of a Single Phase Multilevel Inverter Based Shunt Active Power Filter**

The system configuration of a single-phase system has been discussed in detail. The power components for the single-phase system involve an IGBT-based H-bridge VSC, DC-link capacitor, interfacing inductors, single-phase programmable supply, and linear and nonlinear loads. Voltage and current sensors are employed to sense the different required parameters from the single-phase grid-tied PV system. The sensed signal has been given to the ADC channels of DSP. In the single-phase system, conventional 5-level multilevel inverter-based VSC has been employed. The PV array has been designed and integrated into CHB-MLI.

- **Performance Evaluation of MLI-based SAPF using Conventional Control techniques**

Three conventional control algorithms viz Least Mean Square (LMS), Synchronous Reference Frame Theory (SRFT), and Notch Filter are developed in this chapter. The mathematical formulation of control algorithms has been discussed to extract the fundamental component of the load current. The single-phase grid-connected system feeds the nonlinear load. The control techniques are designed to improve the system power factor unity and quickly regulate the DC link voltages due to sudden load current variations. The estimated weights are further utilized to generate peak amplitude and consequently required to generate reference current. Furthermore, the PWM gating sequence for the 5-Level cascaded H- Bride inverter is developed. The detailed simulation and experimental results have been thoroughly discussed under steady state and dynamic load conditions.

- **Development of Algorithms for Fundamental Component Estimation**

  Advanced adaptive control algorithms viz Normalized Huber (NHUBER), Normalized Least Mean Absolute Third (NLMAT), and Robust Shrinkage Affine Projection Sign (RSAPS) algorithms have been discussed. The system is developed and modeled in MATLAB/Simulink, and the proposed adaptive control algorithm is tested in low prototype scaled-down hardware. A detailed analysis of the simulation and experimental results has been discussed. A comparative table discusses the performance aspects of the developed control algorithm using dSPACE-1104.

- **Power Quality Improvement under distorted grid conditions using Phase Lock Loops**

  Various single-phase synchronization techniques viz; Synchronous Reference Frame (SRF-PLL), Second –Order Generalized Integrator (SOGI-PLL), and Third-Order Sinusoidal Signal Integrator (TOSSI-PLL) have been developed and tested under multiple grid abnormalities like voltage sag/swell, DC-offset, phase shift, and polluted grid voltage conditions. Both open-loop and closed-loop simulation and experimental results have been taken. Furthermore, the SAPF system has been employed for reactive power compensation and harmonic mitigation. In addition, the use of the Parallel Tangent Least Mean Square (PARTAN-LMS) algorithm for closed-loop validation of results with SOGI-PLL has also been demonstrated.

- **Power Quality Improvement using Single Phase MLI based Grid Connected PV system**

  In this chapter, two integrated PV arrays have been interfaced at individual DC links of 5-level CHB-MLI-based VSC, allowing active power into the grid. The performance of SRF-PLL, SOGI-PLL, and MNFSOGI-PLL have been compared under normal and distorted grid conditions. Implementing an appropriate control algorithm is necessary for active and reactive power balancing and power quality enhancement. The designed control algorithms are then tested using simulation, and the experimental results have been validated using the OPAL-RT (OP4510) real-time simulator. Performance aspects are studied for steady and dynamic state conditions involving load changes and irradiation variations.

## 1.5 Outline of Chapters

The content of the thesis work has been divided into the following chapters:

**Chapter 1:** This chapter presents an introduction and background for the various power issues, sources of harmonics, and various methods of mitigation

**Chapter 2:** This chapter includes a literature review on system configuration and control for single-phase grid-connected systems, conventional and adaptive control algorithms, synchronization techniques, Single stage PV integration to the grid, and fundamental component estimation techniques.

**Chapter 3**: This chapter discusses the system configuration of the single-phase grid-connected system, the design of power components for sensing various electrical parameters, and the use of other equipment such as dSPACE-1104, OPAL-RT(OP4510) real-time simulator, Digital storage oscilloscope (DSO). Power Quality analyzer etc., for the system. Also, it discusses the modeling of PV for grid integration

**Chapter 4:** This chapter includes designing and modeling of conventional adaptive control algorithms for single phase 5-level multilevel inverter based grid connected system

**Chapter 5:** This chapter includes designing and modeling of advanced conventional adaptive control algorithms for single phase 5-level multilevel inverter based grid connected system

**Chapter 6:** This chaptger discusses the implementation of synchronization and control techniques for power quality improvement in single-phase under the normal and distorted grid.

**Chapter 7:** This chapter discusses the PV integration to the grid in a single stage for a single-phase system.

**Chapter 8:** This chapter summarizes various conventional and adaptive control algorithms, grid synchronization techniques, control algorithms, and the PV integration to

the grid in a single-phase system. The future scope of work in this area is also presented at the end.

# Chapter 02

# Literature Survey

## 2.1 General Introduction

The previous chapter thoroughly discusses the introduction to various PQ issues, mitigation methods, and the compensator's need with different IEEE standards. In grid-connected systems, photovoltaic (PV) based voltage source converters (VSC) serve the dual purposes of bidirectional active power transfer to the grid and load. They can be controlled to achieve grid current balancing, harmonic reduction, reactive power balance, and improvement of the supply side power factor to unity. The PV source can be linked directly to the VSC at its DC link using the single-stage topology. An effective control algorithm is required for grid synchronization under distorted grid conditions to control the VSC. In the present chapter, an extensive literature survey has been done on the identification adaptive control algorithm for the estimation fundamental component of load current and further generates the reference currents.

Furthermore, various grid synchronization techniques have also been reviewed to make the system robust. Various methods are also examined to extract the maximum from PV in the integrated grid system. Based on the literature survey, the different configurations for single-phase grid-connected strategies have been implemented in the proposed system.

## 2.2 Literature Survey on Various Power Quality (PQ) issues

In the last few years, the reactive power burden has been a challenging issue for power engineers. Due to the extensive use of power electronics-based loads in commercial, residential, and industrial categories, various PQ problems have affected the distribution level. Primary causes of various PQ problems include load switching, variable speed drives (VSDs), arc furnaces, different rectification circuits in load and grid sides, and non-linear loads[1-2]. These loads are significantly non-linear and categorized as current and voltage harmonic sources. As the percentage of such load increases, reactive power demand, feeder losses due to excessive heating of conductors, poor power factor, voltage sag and swell, and poor voltage regulation increase, causing detrimental effects on power transfer capability

[3]. This results in causing an undesirable effect on nearby connected transformers and equipment [4]. Therefore, the exhaustive survey on various PQ problems, methods of mitigation, and different international standards are studied and analyzed in this chapter.

Non-linear demands a high magnitude of reactive power; this component will inject a great extent of voltage and current harmonics in the system, resulting in poor power factor in the grid side and making the source current non-sinusoidal. It is mandatory to have limited THD(%) in grid current and voltages as per the Institute of Electrical and Electronics Engineers (IEEE) and International Electrochemical Commission(IEC) as standards presented in [5-6]. The practices recommended to monitor the characteristics of the single, and poly-phase systems are regulated by IEEE 1159:2009 [7-8] and used by manufacturing companies and research scholars. The recommended practices and harmonics control in electric power system is regulated by IEEE 519:1992 [9]. The IEEE 1547:2018 standard, which is a revision of IEEE 1547:2003 [10], lays out the measures and specifications for the connecting of distributed energy sources to electric power systems (EPSs) and related interfaces [11].

Several harmonic mitigation techniques, such as passive filters, active power line conditioners, and hybrid filters, have been suggested and employed [12-18]. The availability of less expensive controlling devices, such as DSP-/field-programmable-gate-array-based systems, and recent advancements in switching technology make active power line conditioners a viable choice for harmonic compensation. An active power filter (APF) of the shunt type is widely used to remove the current harmonics. To reduce PQ issues with voltage, such as voltage sag, voltage swell, flickers, voltage fluctuations, voltage imbalance, and voltage harmonics, an active series compensator is connected in series at the load end. Examples of series active power filters include DVRs and Solid State Static Series Compensators (SSSCs) [19]. The DSTATCOM, or shunt active power filters, are extensively used in the distribution system [23-25]. It can be used in a shunt-connected mode as a VSC or Current Source Inverter (CSI) to the PCC. DSTATCOM has been utilized to solve current-related PQ issues such as voltage regulation, load balancing, and reactive power compensation. Due to improvements in switching devices, DSTATCOM is now widely used to overcome PQ problems [26-27]. The term "hybrid active power filter" refers to simultaneously operating two active power filters. A hybrid active power filter example is

the UPQC [28-30]. It allows for PQ improvement for both voltage and current-related PQ issues, but it is difficult to manage, necessitates more switches, and is more expensive.

## 2.3 Literature Survey on Various Inverter Topologies

Literature review shows SAPF has usually realized a conventional two-level inverter as a SAPF unit for a single-phase distribution system[31-32]. The problem with this traditional inverter is the high switching frequency and high dv/dt stress across switches for high-power applications, which may lead to malfunctioning across switches. An additional line frequency transformer is also required to be connected, which increases the overall cost of the system for medium and high voltage distribution. Therefore, for high-power applications, its applicability is limited. However, MLI is emerging as a preferred configuration of SAPF, especially for high-power applications [33]. It can operate at a low switching frequency, and the harmonic content is reduced as the number of levels increases. The modular approach gives the required flexibility

The literature survey presents three benchmark MLI topologies[34-39]. Nabae introduced the first one, and Takahashi [36] and is named the 3-level Diode Clamped Multilevel Inverter (DCMLI). This paper introduced the concept of a midpoint Neutral Point Clamped (NPC) inverter. The second well-known configuration is Flying Capacitor MLI (FCMLI), presented by Meynard and Foch[37] and Lavieville*et al.*[38] in the 1990s. It involves capacitors instead of clamping diodes and is known as a capacitor-clamped inverter. In the mid-1970s, Baker and Bannister [39] proposed a series of connections of H-bridges, popularly known as cascaded H-bridge MLI (CHB-MLI). It is a packed module structure, easy to use, and requires simple switching. CHB-MLI is used as the SAPF unit triggered by Phase shifted (PS) modulation scheme[40].

Additionally, CHB multilevel inverters are created by serially connecting several inverters [41]. This construction can improve the low voltage of the individual devices connected in series. Traditionally, in order to get the necessary voltage, several inverters must be linked in series. Every single inverter module has the exact same circuit design and control scheme. Therefore, the CHB inverter has a high degree of modularity [42-44]. As a result, replacing faulty modules is simple and quick. Additionally, this sophisticated control strategy makes it very easy to prevent defective units without disrupting the power supply to

the load terminals, thereby ensuring continuous availability [45-46]. For a variety of applications, numerous cascaded multilevel inverter topologies have been developed and implemented [47-49]. The detailed analysis of switching losses and power requirements of switches are thoroughly discussed in [50-51]

## 2.4 Literature Survey on Grid Synchronization Schemes

Due to the rising use of renewable energy sources in grid-connected distributed generation (GCDG) systems and the resulting power quality problems, the estimation of the grid parameters is affected [52]. To maintain the steady operation of the GCDG system, accurate grid phase, frequency, and voltage estimates are required. The phase-locked loops (PLLs) are an essential component of GCDG systems for grid connections and synchronization of the voltage source inverter (VSI). However, the GCDG system suffers from several power quality problems due to grid disturbances, including voltage sag/swell, harmonics, frequency oscillations, and dc offset. This affects the PLL's ability to track frequency and phase [53]. Therefore, synchronizing the system with the grid under grid disturbances requires a robust PLL approach. It enhances grid-connected system performance and reduces power quality problems. Researchers have also suggested several PLL techniques, some of which do not perform well under distorted grid conditions. Researchers have employed SRF-PLL as a typical PLL implemented to generate synchronization signals and phase and frequency estimation[54-56]. Therefore, PLL must extract fundamental components in adverse grid conditions and synchronize the VSI with the GCDG system.

In the literature, many single-phase PLLs have been developed and presented forward. Power-based PLLs (pPLLs) [57-63] and quadrature signal generation-based PLLs (QSG-PLLs) [64-77] are the two main types of PLLs are classified. The primary difference between single-phase PLLs may be found in their phase detector block ( PD), which forms the basis for classification.

In recent years, orthogonal signal generator (OSG) based PLL has been widely used and implemented to handle various grid abnormalities. Also, its tracking performance is quite good and accurate compared to SRF-PLL [78-81]. However, under frequency variations in the grid, the OSG-PLL generates an error in the estimation of Phase and frequency. OSG-PLL, Second-Order Generalized Integrator (SOGI-PLL), and Park-PLL

retain their performance even in frequency deviation and are widely used by researchers or power engineers for the grid-connected system. For SOGI to operate effectively under variable frequency conditions, SOGI-FLL has been recommended [82-83]. To determine the frequency of the input signal, the FLL block is realized. However, SOGI-FLL has a limited filtering capability and provides unsatisfactory results when the grid voltage has a DC offset. Orthogonal signal generation (OSG) is required for a single-phase PLL. One-phase PLLs frequently employ OSG techniques such as the transfer delay, all-pass filter, Hilbert transform, and Second-Order Generalized Integrator (SOGI) [82-87]

It is well known that the SOGI-PLL cannot handle the DC-offset disturbances in the grid. However, the DC offset should be less than 1% and 0.5% of their respective rated grid currents, according to standards IEC61727 and IEEE 1547-2003 [88-89]. This effect deteriorates the tracking performance of SOGI-PLL. Therefore, the estimation of Phase and frequency contains an error of significant deviation. Therefore, a new PLL viz. Modified Notch Filter based SOGI-PLL(MNFSOGI-PLL) [90] has been discussed, which only takes care of DC offset voltages and has the rejection capability of inter-subharmonics. The dynamic performance of MNFSOGI-PLL has been carried under various grid abnormalities, viz. voltage sag/swell, DC offset, polluted grid, and Phase shift conditions. Later, the MNFSOGI-PLL is implemented for a single phase single stage grid-connected PV array system to extract the fundamental load current for the generation of reference current under non-linear load with a normal and distorted grid[90].

## 2.5 Literature Survey on Adaptive Control Algorithms for SAPF

The effectiveness of SAPF depends upon how accurately the control algorithm extracts the reference current and compensates for the harmonics generated by the load. Various time and frequency domain algorithms have been presented in the literature [91-99]. Some of the conventional algorithms are very popular and effective such as Synchronous Reference Frame Theory (SRFT)[91]; Instantaneous Reactive Power Theory[92]; Symmetrical Component-based Theory[93]; algorithms based on the cancellation of double frequency components [94-95]; Several new algorithms have been proposed and include Composite and Model Observer-Based Algorithm[96-97]; Kernel Incremental Learning Algorithm[97-98]. These algorithms perform well but require tuning several parameters,

substantially high arithmetical operations, and additional filters. Besides, various frequency-domain algorithms such as Kalman Filter[99] and Fourier Transform[100] have also been implemented for the control of SAPF and distribution static compensator (DSTATCOM).

Over the last few decades, adaptive signal processing techniques have been applied to various fields, such as active noise cancellation, signal enhancement, noise filtering, echo cancellation, etc. Due to its simple structure, the most common adaptive algorithm is the least mean square (LMS) presented in[101]. Its limitation is that its weight convergence performance depends upon the step size, and its variation directly influences the performance. Later, a Normalized Least Mean Square (NLMS) was proposed to overcome the limitation of the LMS algorithm [102]. Unfortunately, the performance of LMS and NLMS is highly dependent upon the choice of step size parameter. There is a trade-off between steady-state error and convergence while deciding the optimum step size. Hence, several papers have focused research on this issue[103].

One solution is to avoid the fixed step size and adopt a variable step size (VSS) based adaptive technique. The adaption must ensure good algorithm performance with very low steady-state error and a fast convergence rate. Paper [103] discusses a simple VSS-LMS algorithm is presented which is controlled by the variable step size and the minimization of Mean Square Error (MSE). However, the VSS-LMS algorithm needs to update the step–size at the instant of sudden variation in the input signal and depends on the initialization of the input weight vector. Authors in[104-105] have presented another classical approach to an adaptive algorithm known as Least Mean Fourth (LMF) and Least Mean absolute third (LMAT). Both LMF and LMAT techniques perform better than the conventional LMS algorithm in terms of MSE, rate of convergence, and steady-state error.

In recent years, the implementation of different adaptive algorithms[105] based on adaptive-linear-element (ADALINE) to estimate the fundamental frequency component of load current has been presented. Qasim et al. [106] demonstrated three adaptive algorithms, two for frequency and voltage estimation and the third for extracting load current. Besides, particle swarm optimization (PSO) is used to enhance the dynamic performance of each ADALINE. Chilipi et al. [107] presented a New Least Mixed Norm (LMMN) algorithm. In this scheme multichannel LMMN structure is used to extract all dynamic harmonics of load current and simultaneously reduces the error produced by the LMMN filter, thus improving

the dynamic performance. Paper [108] Badoni et al. implemented a discrete-time filter widely known as the Weiner filter to minimize the MSE and extract components of load current. In[109], a Kalman-based H∞ filter is used to estimate the positive sequence current quickly. Also, the adaptive rules of the Kalman algorithm regulate the dc-link voltage with considerable variations in grid and load disturbances. In the literature, some of the authors presented Artificial Neural Network (ANN) based techniques for compensation. Different ANN structures such as the Adaptive euro Fuzzy inference system (ANFIS) are reported in[110], Radial functional neural network[111], feed-forward ANN, and adaptive linear neural (ADALINE) has presented in[112]. Among these, feed-forward ANN is very popular and widely used. Paper [113] mentioned using an ANFIS-LMS-based control algorithm to mitigate PQ problems. Some authors implemented the Harmony Search algorithm[114] and; Radial Basis Function Neural Network Algorithm [115] to control MLI and J. Tandekar *et al.*[116] has implemented the Power Balance (PQ) theory to control CHB-MLI, and Sushree Sangita Patnaik *et al.* [117] have presented the $i_d$-$i_q$ control algorithm for 3-level CHB-MLI.

Paper [118] discusses the multiple complex coefficient filter MMCF-SOGI-based control algorithm. Manoj et al. [119] have presented an Adaptive zero attraction least mean square(ZA-LMS) algorithm. Some other algorithms mentioned in recent papers include the Adaptive neural network-based method [120]; Wiener filter [121]; Gauss Newton-based controller [122] and Affine projection algorithm [123]; combined (ATC-DLMS) diffusion estimation [124]; the Z2-proportionate diffusion algorithm [125], and all these have been reported in recent years.

Some more algorithms have also been reviewed for adaptive filtering, viz Alhaj Hussain *et al.* [126] have presented the combined LMS-LMF algorithm, which shows better performance. In addition, some advanced adaptive control algorithms available in the literature viz Pinaki Mitra *et al* [127] has discussed artificial immune adaptive control algorithm for DSTATCOM; In [128] author presented improved Widrow-Hoff algorithm to improve grid current by extracting the fundamental load current; adaptive weighted zero attracting (RZA) control algorithm have been presented in [129]; optimal control of DSTATCOM has been discussed by Pavitra *et al* [130]on implementing adaptive Laguerre filter; adaptive signal processing algorithms with accelerated convergence and noise immunity with PARTAN-LMS [131]; Diffusion normalized Huber adaptive filtering

algorithm (NHuber)[132]; Robust Shrinkage Affine-Projection Sign Adaptive-Filtering Algorithms(RSAPS)[133]; New Normalized Least Mean Absolute Third Algorithm[134]. Some pattern recognition-based artificial neural network (ANN) based techniques have also been discussed in the literature to mitigate PQ problems. M.Qasim *et al.*. [135] presented the application of ANN for SAPF, Neural network-based conductance estimation [136], adaptive neuro-fuzzy inference system[137], ANN-based predictive and adaptive control [138].

## 2.6 Literature Survey on Grid-Connected PV-based Distribution System

The penetration of renewable energy sources, such as wind and photovoltaic (PV) generation in the electricity sector, has significantly increased over the past ten years [139-140]. As a result, maintaining power system stability, reliability, and power quality becomes a mandatory and challenging task for system operators. Consequently, various nations have implemented grid codes that govern the connection of renewable energy sources to the utility system [141-144].

PV generation systems are scalable, pollution-free, fuel-cost-free, and require little maintenance. However, PV energy generation faces several challenges, including high installation costs, poor efficiency, and energy generation dependent on the weather [146-149]. When considering the impact of various weather conditions, the usual solar system efficiency ranges between 9% and 17% [150]. Since solar energy depends on the weather, effective control techniques are essential to ensuring the PV systems' effective and secure operation. Various tracking algorithms have been discussed in the literature to extract the maximum power from the solar PV array [151-153]. Due to their ease of implementation, traditional MPPT techniques are frequently used in a variety of applications, including those involving Fractional Short-Circuit Current (FSCC), Fractional Open-Circuit Voltage (FOCV), Hill Climbing, and Perturb & Observe, strategies [154-155].

Due to the quantity of solar light and advanced power electronics technology, a grid-tied PV system is prevalent. This research contributes to developing a fundamental conceptual framework for an improved grid-tied system. According to control investigation, frequency, Phase, and amplitude of voltage are the essential characteristics that must be

measured and managed for grid-tied applications. At the same time, synchronization is a significant challenge in the operation of grid-tied inverters. According to their operational and technological specifications, PV systems have the benefit of operating in islanding/standalone mode and grid integrated mode, as presented in Aisyah et al.[156]; Murillo-Yarce et al., [157]; To track grid frequency and Phase angle, several grid synchronization methods for converter-based resources are mentioned by Hariri et al. [158]; Jaalam et al. [159]; and Panigrahi et al. [160].

Based on control, the on-grid synchronization methods described in the current literature are divided into single-phase and three-phase systems. The author highlights several methods for estimating phase angle and grid frequency. Since several grid synchronization strategies have been introduced in the literature over the past few decades, this work focuses on providing an overview of the recent developments in the methodology, including advanced algorithms, and emerging technologies, to enhance grid synchronization accuracy, robustness, and efficiency. According to Pádua et al. [161] and Sridharanand & Babu [162], the grid synchronization technique is further categorized into open-loop and closed-loop systems and other control algorithms viz Zero Crossing Detection (ZCD) (Jaalam et al., [159]; Khan[163] Konara et al. [164]; Discrete Fourier Transform (DFT) (Honorato and Silva, [165]; Neves et al., [166]; Pádua et al. [167]; Silva and Nascimento[168], Kalman Filter (Ahmed et al., [169]; Freijedo et al., [170] Golestan et al., [171]; Meersman et al. [172]; Devi and Kadam, [173] are also mentioned in the literature. However, the open-loop approach is restricted by the absence of PLL. Open-loop procedures are less advantageous since a lack of real-time frequency tracking with steady-state faults creeps in, while the closed-loop approach is a better alternative. Due to its ease of use, dependability, and efficiency, PLL is the closed-loop approach for grid synchronization that is employed most often used by Meersman et al.[172]. The performance of several single-phase PLL and three-phase PLL synchronization techniques (Boyra and Thomas, [174]; Golestan et al., [175]; Jaalam et al., [159]; Golestan et al., [176]) and their comparison is presented based on their benefits and drawbacks.

When the load requirement is less than the amount of power generated by the integration of PV arrays, it is possible to inject active power into the grid. No DC-DC converter is used in a single-stage arrangement. However, a DC-DC converter is utilized in a

double-stage configuration. Both configurations are well documented in the literature. Maximum Power Point Approach (MPPT) control algorithm is implemented to provide a reference DC-link voltage [177-178].

## 2.7 Identified Research Gap

After extensive review, the following research gap has been identified

1. Fast and new adaptive control techniques should be exploited to extract the harmonics from distorted grid and to generate reference current
2. Extensive investigation of Multilevel Inverters used as shunt compensator for medium voltage distribution systems should be exploited.
3. Non-PLL and PLL-based fast and efficient synchronization techniques based on different types of adaptive filters, such as least mean squares (LMS) filters and its family should be exploited
4. Synchronization techniques considering polluted grid, weak grid and different loading conditions are to be addressed. Also, a fair comparison of these is required based on both simulation and experimental studies

## 2.8 Research Objectives

1. Investigation on mitigation of PQ Problems in single phase Distribution System using Multilevel Inverter as shunt compensator
2. Design, develop, and performance analysis of various new and advanced adaptive control algorithms
3. Investigations on Mitigation of PQ Problems in Distorted Grid System
4. Investigations on grid-connected PV systems for Multilevel Inverter
5. Testing of the experimental setup control algorithms under different loading, polluted grid conditions

## 2.9 Conclusion

This chapter presents extensive literature surveys on various power quality (PQ) issues, their mitigation methods, the selection of inverter topology, and their control. To estimate the fundamental component of load current and to generate the reference current various time and frequency domain adaptive control algorithms have also been discussed under abnormal and distorted grid conditions. Different grid synchronization PLLs are presented to tackle several grid abnormalities. Various configurations and control of single-stage grid connected PV systems have also been discussed. Based on the extensive research, the research gaps have been identified, and further, the research objectives are formulated.

# Chapter 3

# Designing and Development of a Single Phase Multilevel Inverter Based Shunt Active Power Filter

This chapter explains the design and development of a grid-connected single-phase SAPF system without and with a PV interface. Design calculations are essential for the SAPF system to function correctly. The design calculations are carried out for several components for the SAPF system. After that, simulation and real-time experimental validation have been presented. PV module modeling and PV array design coupled to single-stage grid connected system is also covered in this chapter.

## 3.1 Introduction

The single-phase SAPF system configuration is shown in Fig 3.1. Under various loading scenarios, it has been employed for reactive power compensation and harmonic mitigation in single-phase systems. Additionally, the system performance has been analyzed under polluted grid conditions.

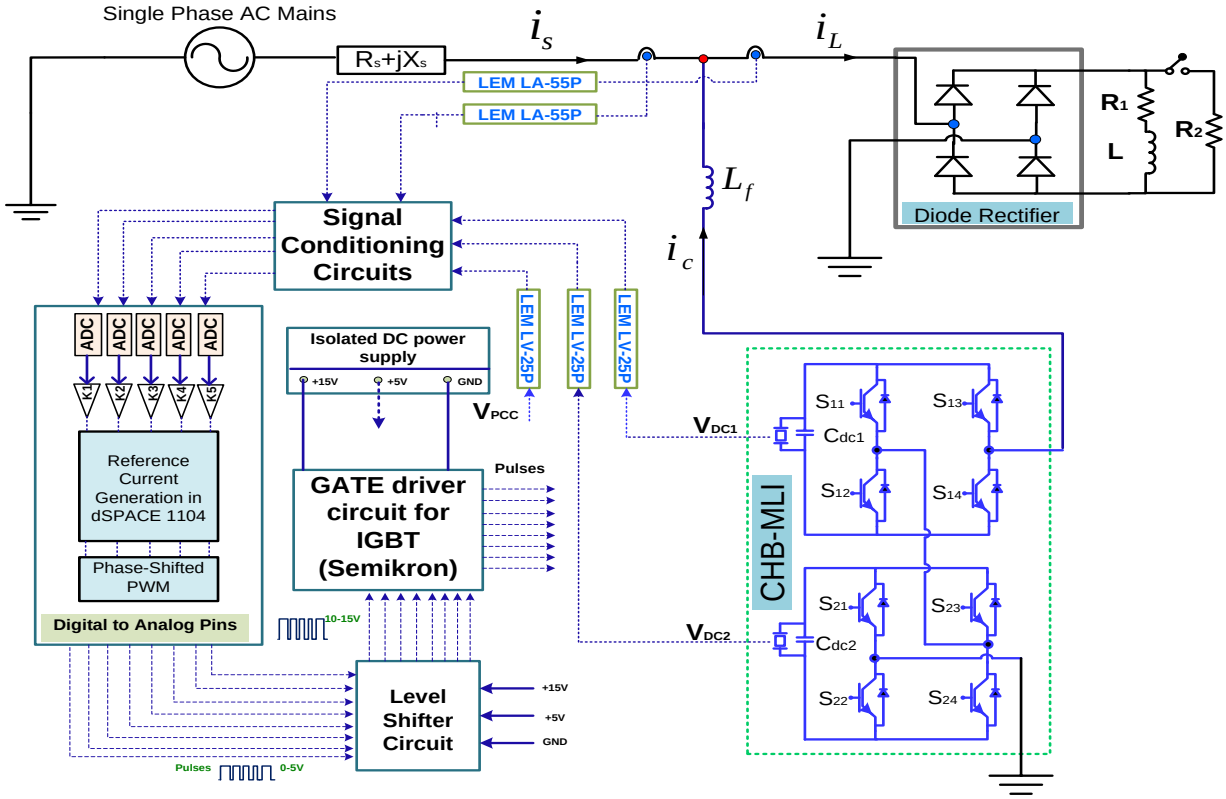



**Fig 3.1** Proposed System configuration

The system configuration for a single-phase, single-stage grid-connected PV system is shown in Fig 3.2. A 5-level CHB-MLI is shown with two H-bridges connected in cascade configurations.The PV array has been linked directly to the VSC's DC-link in this setup. In this setup, no DC-DC converter has been employed hence a single-phase grid-connected PV system is considered. The DC-link voltage's reference voltage, which is the maximum power point voltage, is achieved using the MPPT approach. Active power injection into the grid is facilitated by this design.

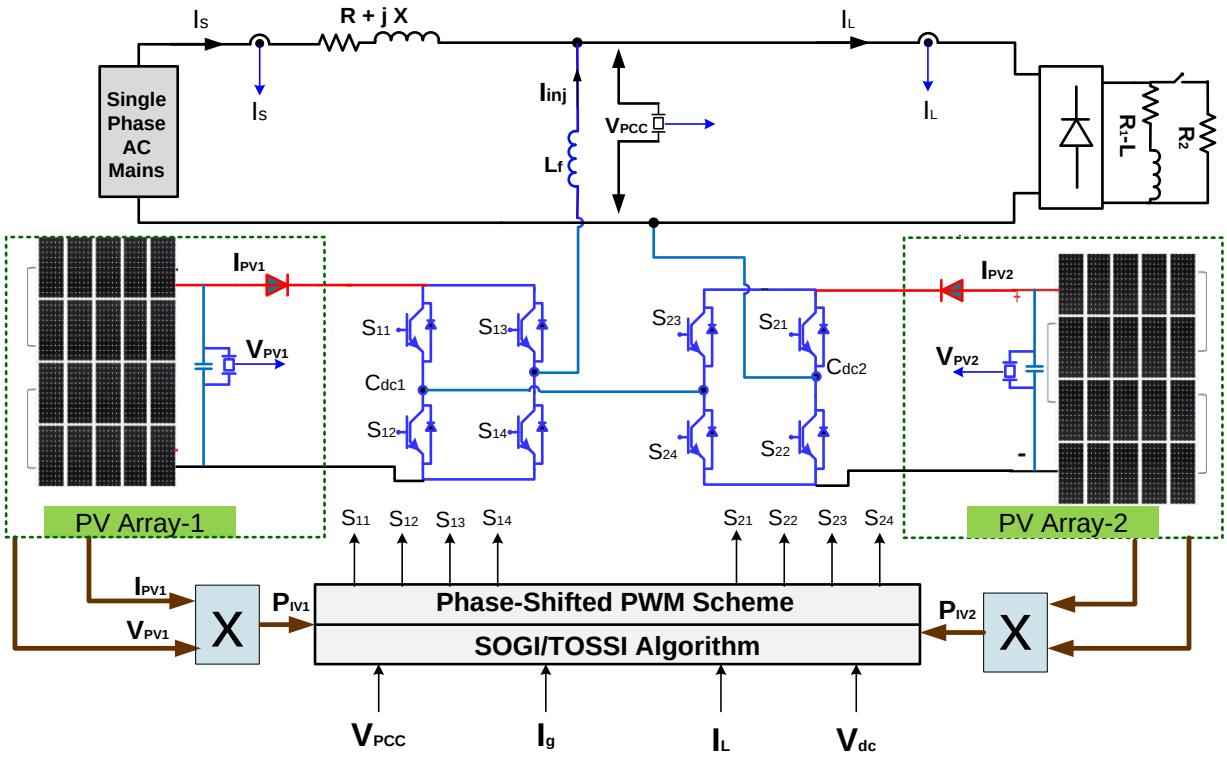



**Fig 3.2** single Stage grid-connected PV systems for 5-level CHB-MLI

The principal parts required for the setup are as follows: single-phase programmable supply; dSPACE 1104 board; auxiliary DC supply; voltage and current sensors; H-bridge VSC; DSO; interfacing inductor; resistive load; load side inductor; diode bridge rectifier. The design of every component of a single-phase grid connected system is discussed in detail. The following design quantities been considered.

1. DC link capacitors
2. Interfacing inductors

3. DC reference value
4. Current and Voltage sensors
5. PV array configuration
6. Amplification Circuits

As already discussed in the literature review, SAPF has usually realized a conventional two-level inverter for a single-phase distribution system. The problem associated with this conventional inverter is the high switching frequency and high dv/dt stress across switches for high power applications, which may lead to malfunctioning occurring across switches. An additional line frequency transformer is also required to be connected, which increases the overall Cost of the system for medium and high voltage distribution. Therefore, for high-power applications, its applicability is limited. However, MLI is emerging as a preferred configuration of SAPF, especially for high-power applications 2. It can operate at a low switching frequency, and as the number of levels increases, the harmonic content is reduced. The modular approach gives the required flexibility in the system.

## 3.2 Different topologies of conventional Multilevel Inverters

The literature survey presents three benchmark MLI topologies [33-34]. The first one is introduced by Nabae, and Takahashi, and is named the 3-level Diode Clamped Multilevel Inverter (DCMLI). This paper introduced the concept of a midpoint Neutral Point Clamped (NPC) Inverter [36]. The second well-known configuration is Flying Capacitor MLI (FCMLI) introduced by Meynard and Foch and Lavieville*et al.* in the 1990s[37]. It involves the basic idea of using capacitors instead of clamping diodes and is also known as a capacitor clamped inverter. In the mid-1970s, Baker and Bannister proposed a series of connections of H-bridges popularly known as cascaded H-bridge MLI (CHB-MLI)[39]. It is a packed module structure, easy to use, and requires simple switching. In this dissertation, CHB-MLI is controlled as the SAPF unit triggered by Phase Shifted (PS) modulation scheme

### 3.2.1 Diode Clamped Inverter[35]

The diode clamped inverter, which uses a diode as a clamping device to connect the dc bus voltage to achieve steps in the output voltage, is the most widely used multilevel structure. Nabae, Takahashi, and Akagi's 1981 neutral point converter design was simply a three-level diode-clamped inverter [36]. Two pairs of switches and two diodes comprise a three-level diode-clamped Inverter. Each switch pair operates in complementary mode, and the access to mid-point voltage is provided by the diodes. Each of the three inverter phases of a three-level inverter shares a common dc bus that has been separated into three levels by two capacitors. Likewise, 5-level configurations have been designed, as shown in Fig 3.3(a). The 5-level output voltage is shown in Fig 3.3(b), and the switching states of 5-level configurations is tabulated in Table 3.1

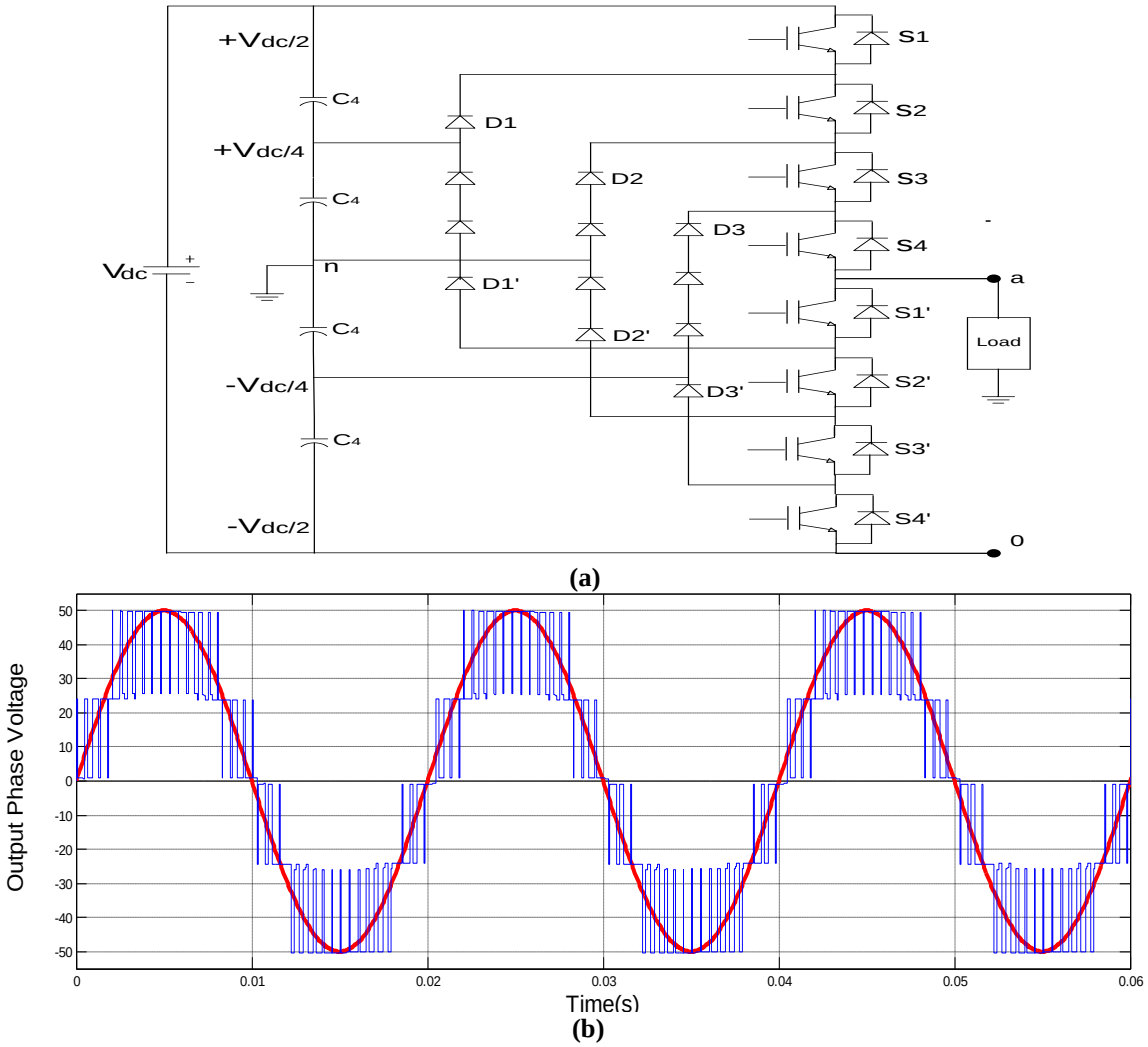


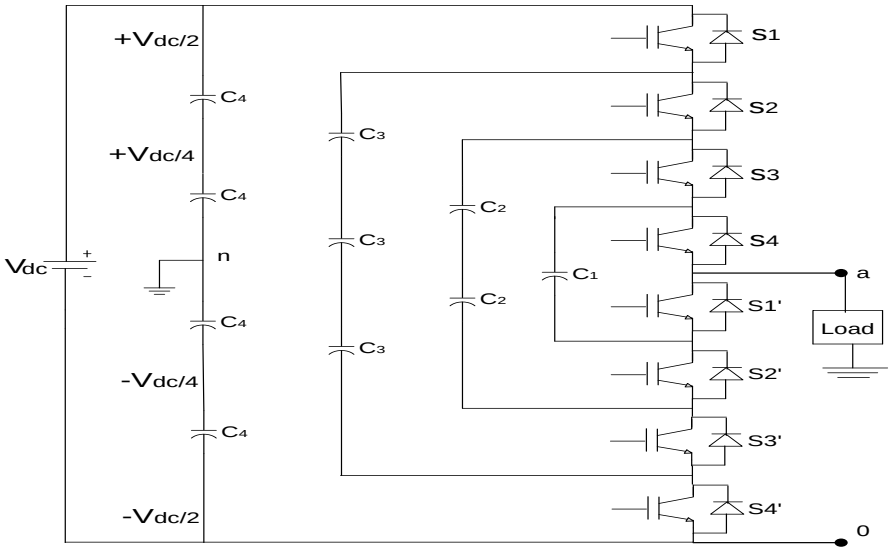

**Fig 3.3** (a) Generalized structure of 5-level DCMLI (b) 5-level output voltage

**Table-3.1.** Switching states in one leg of the five-level Diode Clamped Inverter

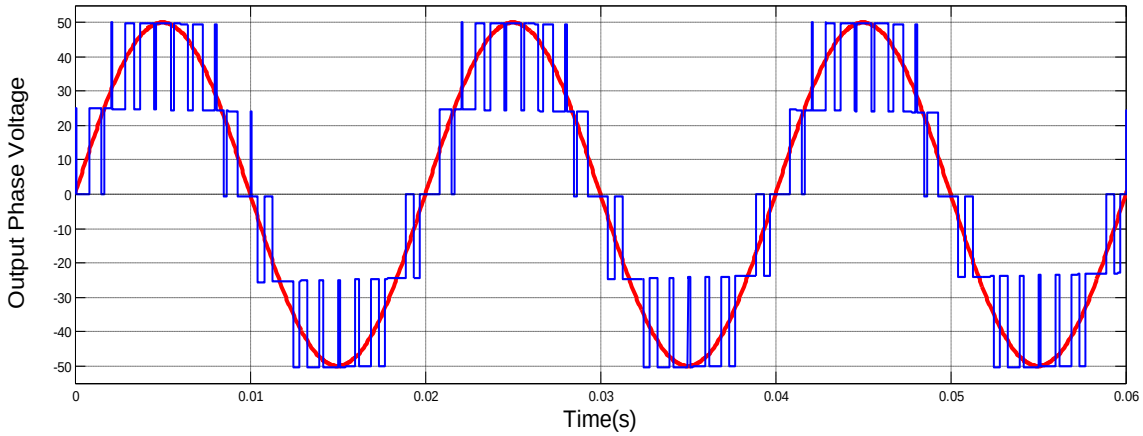
| Levels | SWITCH STATES | | | | | | | | Output Voltage (Van) |
|---|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S1' | S2' | S3' | S4' | |
| 2 | ✓ | ✓ | ✓ | ✓ | | | | | $V_{dc}$ |
| 1 | | ✓ | ✓ | ✓ | ✓ | | | | $V_{dc}/2$ |
| 0 | | | ✓ | ✓ | ✓ | ✓ | | | 0 |
| -1 | | | | ✓ | ✓ | ✓ | ✓ | | $-V_{dc}/2$ |
| -2 | | | | | ✓ | ✓ | ✓ | ✓ | $-V_{dc}$ |

### 3.2.2 Flying Capacitor

Meynard and Fochin proposed the capacitor-clamped inverter, also called the flying capacitor, in 1992 [37]. This Inverter structure is identical to that of the diode-clamped inverter, with the exception that the inverter uses capacitors in place of clamping diodes. Switching cells with capacitor clamps are connected in series to create a flying capacitor. The dc side capacitors in this architecture are arranged in a ladder structure, with each capacitor's voltage varying from the capacitor behind it. The magnitude of the voltage steps in the output waveform is determined by the voltage difference between two adjacent capacitor legs. The switching states of the five -level capacitor clamped inverters are tabulated in Table 3.2 and its topology and output voltage is shown in Fig 3.4(a-b).




**(a)**




**(b)**

**Fig 3.4** (a) Single-Phase Capacitor-clamped multilevel inverter for 5-level (b) Output Phase voltage of five-level MLI.

**Table-3.2** Switching states of 5-level FCMLI inverter

| GENERATION OF LEVEL | SWITCH STATES | | | | | | | | OUTPUT VOLTAGE (Van) |
|---|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S1' | S2' | S3' | S4' | |
| 2 | ✓ | ✓ | ✓ | ✓ | | | | | $V_{dc}/2$ |
| 1 | ✓ | ✓ | ✓ | | ✓ | | | | $V_{dc}/4$ |
| 0 | ✓ | ✓ | | | ✓ | ✓ | | | 0 |
| -1 | ✓ | | | | ✓ | ✓ | ✓ | | $-V_{dc}/4$ |
| -2 | | | | | ✓ | ✓ | ✓ | ✓ | $-V_{dc}/2$ |

### 3.2.3 Cascaded H-Bridge Multilevel Inverter

The cascaded multilevel inverter comprises several H-bridge inverter units, each with its independent dc source, and is coupled in series or cascade, as illustrated in Fig 3.6. (a). By connecting the dc source to the ac output side using various configurations of the four switches S1, S2, S3, and S4, each H-bridge can generate three different voltage levels: +Vdc, 0, and –Vdc as depicted in Fig 3.5(a-b). The flexibility of the cascaded-H bridge topology allows for the simple growth of the number of levels without adding undue complication to the power circuit. Inverters with series H-bridges were presented in 1975 in a paper[9]. The two researchers, Lai and Peng, properly designed the cascaded multilevel inverter. Since then, the CMI has been used in various applications and has proven to be

more effective in high-power applications. Each H-bridge's output is linked in series with the others such that the output voltage waveform produced is the total of all the outputs from every H-bridge. The switching states for 5-level inverter are tabulated in Table 3.3 and the power flow circuit diagrams for 5-level is represented in Fig 3.7. The output phase voltage has 2s+1, where 's' denotes the number of H-bridges utilized for each Phase. For a 3-level and 5-level multilevel inverter, respectively, one H-bridge and two H-bridges per Phase are needed.

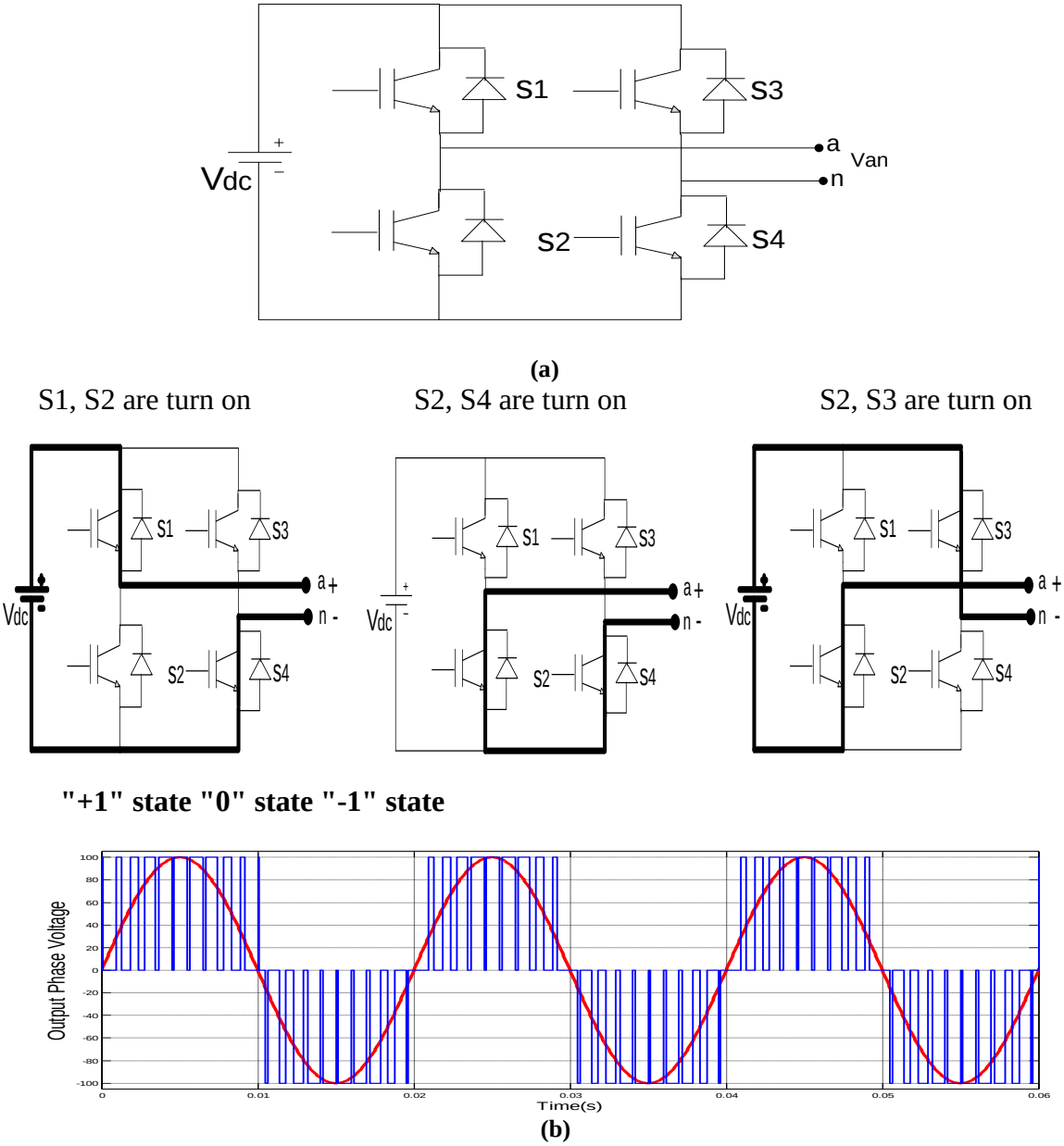
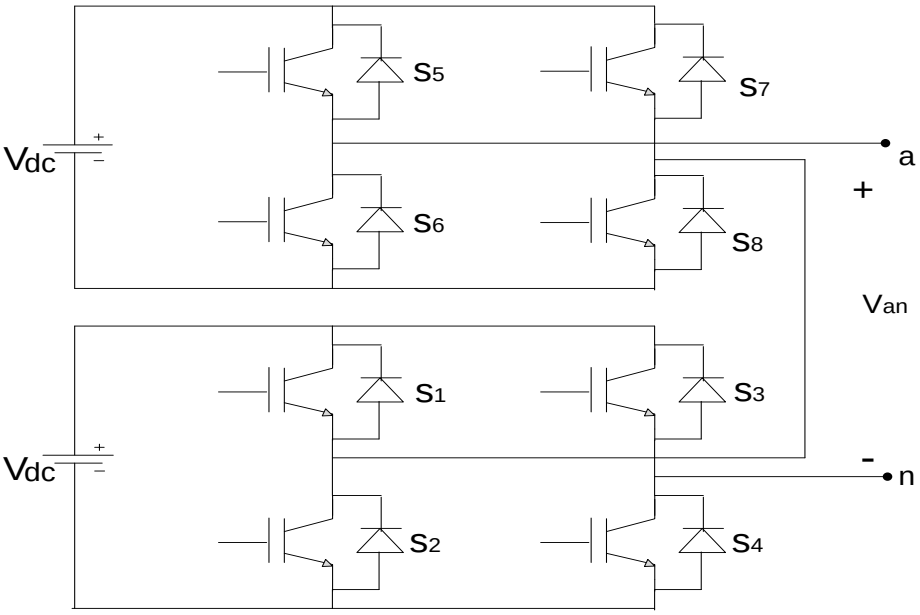
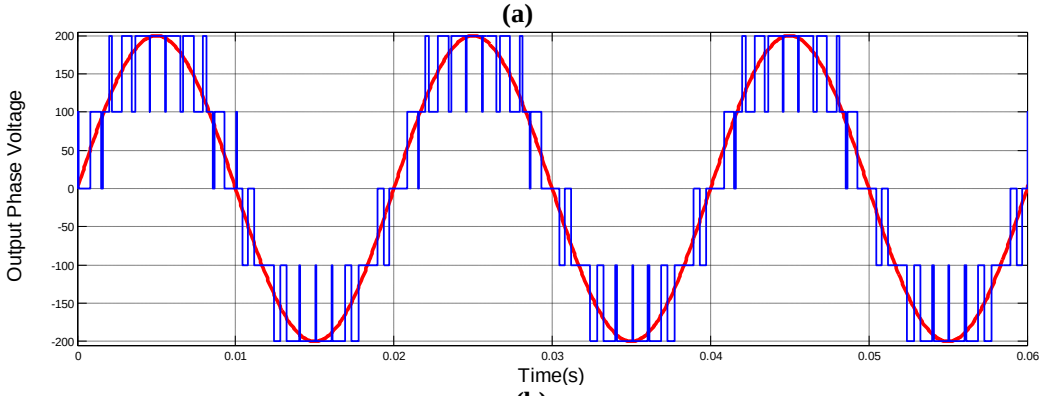



**Fig 3.5** Topology of the three-level Cascade H-Bridge inverter (a) In single-phase (b) Switching states




**(a)**

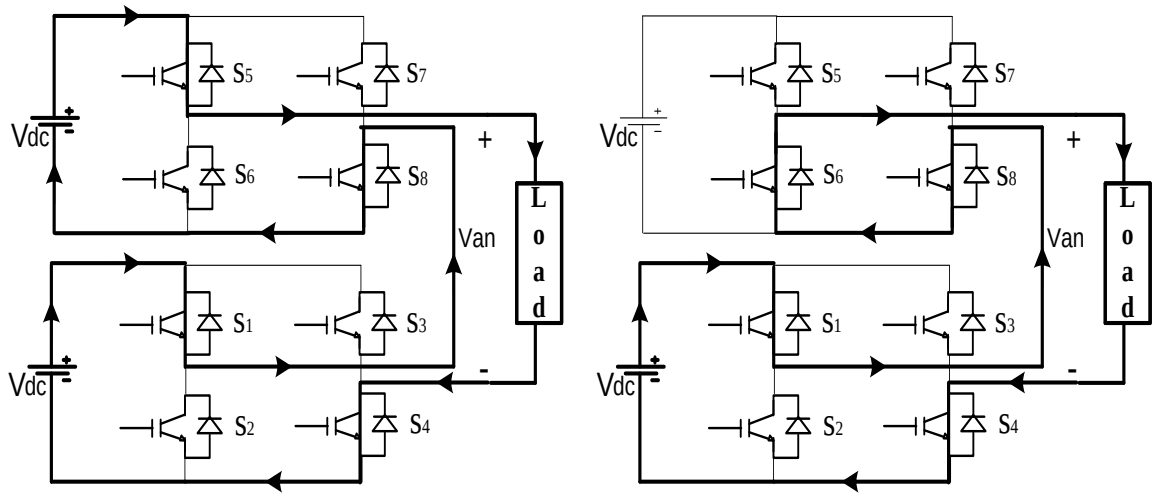



**(b)**

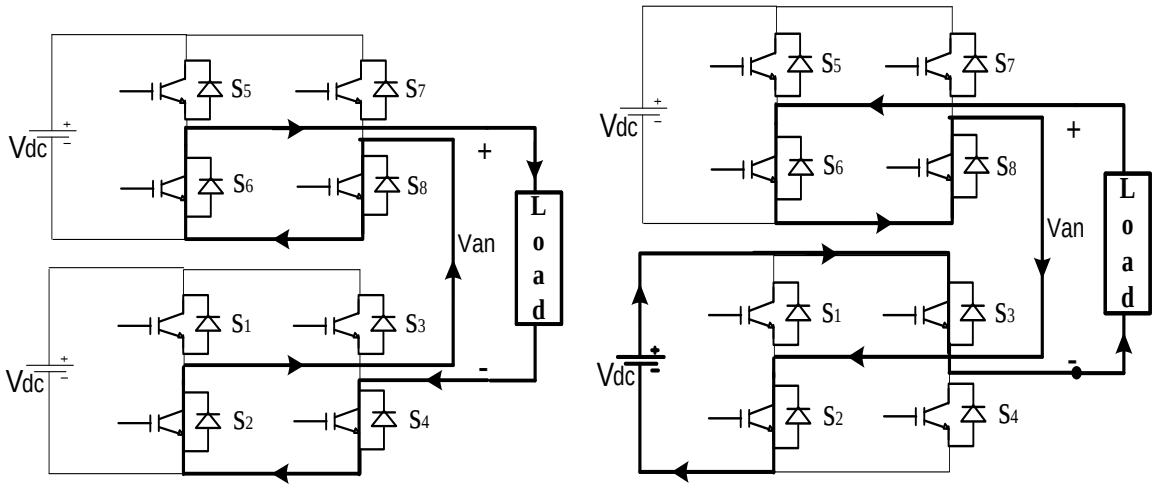
**Fig 3.6** (a) Single phase structures of Cascaded H-Bridge MLI for 5-level (b) Output phase voltage.

**Table 3.3 :** Switching states in one leg of the five-level Cascaded H-Bridge inverter

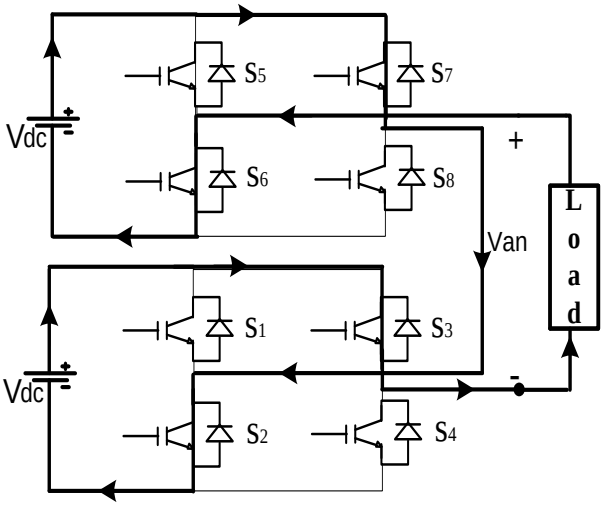
| GENERATION OF LEVEL | SWITCH STATES | | | | | | | | OUTPUT VOLTAGE (Van) |
|---|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | |
| 2 | ✓ | | | ✓ | ✓ | | | ✓ | 2Vdc |
| 1 | ✓ | | | ✓ | | ✓ | | ✓ | Vdc |
| 0 | | ✓ | | ✓ | | ✓ | | ✓ | 0 |
| -1 | | ✓ | ✓ | | ✓ | | ✓ | | -Vdc |
| -2 | | | | | | | | | -2Vdc |




**"+2" state "+1" state**




**"0" state "-1" state**




**"-2" state**

**Fig 3.7** CHBMLI for 5-level Switching states

## 3.3 Proposed Five-Level MLI-based System Configuration

The proposed system of grid-connected CHB-MLI bases SAPF is shown in Fig 3.8. Assuming symmetrical configuration i.e. ($V_{dc1}$=$V_{dc2}$) in the steady state, a phase shift pulse width modulation [28] is adopted to generate firing pulses. Thus each H-bridge produces three voltage levels +$V_{dc}$,0, -$V_{dc}$. From Fig 3.8, by turning the switches $S_{11}$ and $S_{14}$ of the upper H-bridge, it is possible to set $V_{a1}$=+$V_{dc}$ and by turning ON switches $S_{12}$ and $S_{13}$ it is possible to set $V_{a2}$= -$V_{dc}$. Moreover, to generate 0 level by turning ON either $S_{11}$ and $S_{12}$ or $S_{13}$ and $S_{14}$.It is noticed that the switching state of $S_{1x}$, $S_{2x}$ (x=1,2) must be complimentary to switches $S_{x3}$, $S_{x4}$ (x=1,2) to prevent sudden dead short circuits on the switches of the inverter. The switching function for CHB-MLI can be expressed as

$T_1 = S_{11}.S_{14} – S_{12}.S_{13}$ (3.1)

$T_2 = S_{21}.S_{24}-S_{22}.S_{23}$ (3.2)

The value of $T_x$(1,2) represents the charging and discharging of capacitor under dynamic conditions.

Series loss denote the losses in resistance and series resistance (ESR) represents equivalent losses in inductors. Parallel losses are the losses in dc link capacitance parallel to shunt resistance corresponding to the H-bridge's active power loss. The differential equation by applying KVL in between interfacing inductor and grid can be derived as:

$$V_{pcc} = RI_c + L\frac{dI_c}{dt} + T_1V_{dc1} + T_2V_{dc2} \quad (3.3)$$

where the variable $V_{pcc}$ represents the voltage at point of common coupling (PCC), L denotes the inductance of interfacing inductor and R represents the ESR. The variable $V_{dc1}$, $V_{dc2}$ denote the actual dc link voltages of the CHB-MLI. According to Kirchhoff's law the current flowing in DC link capacitors $C_1$ and $C_2$ can be expressed as

$$I_{c1} = C_1\frac{dV_{dc1}}{dt} = I_{01} - I_{R1} \quad (3.4)$$

$$I_{c2} = C_2\frac{dV_{dc2}}{dt} = I_{02} - I_{R2} \quad (3.5)$$

where $R_1$ and $R_2$ are the equivalent resistances of each H-bridges representing the power losses. The variables $I_{01}$ and $I_{02}$ represent the total dc link current of the individual H-bridge. Let the vector of the variables can be written as $X_2$ = [$I_c$, $V_{dc1}$, $Vd_{c2}$]$^T$ and $U_2$= [$V_{pcc}$,

0, 0]$^T$ as input vector rearranging equations (3.4-3.5), the state equations can be expressed in matrix form as:

$$\dot{X}_2 = A_2 X_2 + B_2 U_2 \tag{3.6}$$

where

$$A_2 = \begin{Bmatrix} -\frac{R}{L} & -\frac{f_1}{L} & -\frac{f_1}{L} \\ -\frac{f_1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ -\frac{f_2}{C_2} & 0 & 0 \end{Bmatrix} \quad B_2 = \begin{Bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{Bmatrix} \tag{3.7}$$

The mathematical equation of MLI based shunt active power filter depends upon switching function and passive elements of SAPF. Therefore proper designing of interfacing inductor and dc link capacitor plays an important role for satisfactory operation of CHB-MLI SAPF.

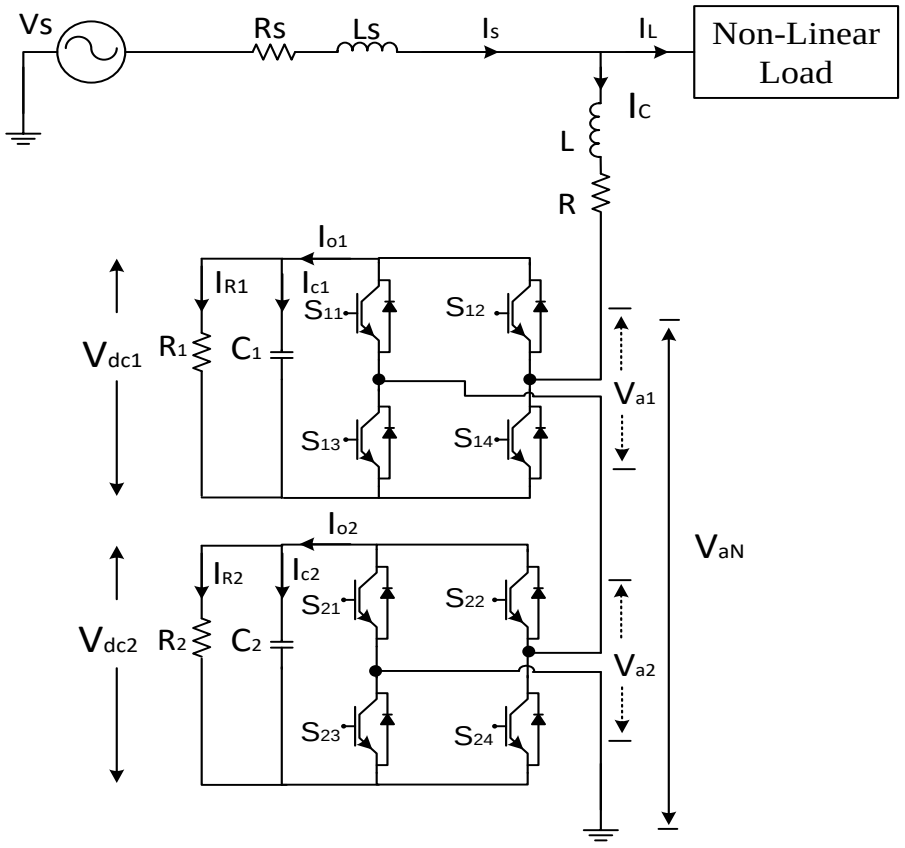



**Fig 3.8** Schematic of CHB-MLI-based Shunt Filter

## 3.4 Design and development of Shunt Compensator

The design of the interfacing inductor and the DC link capacitors and their reference dc values are discussed next.

### 3.4.1 Design of DC link Capacitor [25-26]

Proper designing of DC-link capacitors is needed, which is calculated using the following relation. Its expression can be given as

$$C_{dc} = \frac{K_L v_s i_c T}{2(V_{dc-ref}^2 - V_{dc}^2)} \tag{3.8}$$

where $v_s$ is taken as 110V(rms) AC, $i_c$ = 4A, compensating current, T=0.02sec, $V_{dc\text{-}ref}$ = 200V, $V_{dc}$=190V, considering a voltage drop of 10V, $K_L$=1.5 overloading factor ,$C_{dc}$=2707.69 μF is calculated and for this system it is taken as 3000μF in experimentation and for simulation studies.

### 3.4.2 Design of Interfacing Inductor[25-26]

The value of $L_f$ is calculated as

$$L_f = \frac{V_{dc,ref}}{12\,(m-1)\, f_{sw}\, \Delta I_{cr-pp}} \tag{3.9}$$

$V_{dc\text{-}ref}$ =200V, $f_{sw}$ =5 kHz is the switching frequency, m= 5 represents voltage levels, $\Delta I_{cr-pp}$ = 0.2 peak to peak ripple current. The computed value is 4.16mH, and the value selected is 3mH and 5mH for experimentation and simulation, respectively

### 3.4.3 Calculation of reference DC link voltage[25-26]

The selection of dc-link reference voltage is important, and usually, for healthy and effective compensation, its value should be higher than the supply voltage. The magnitude of the dc bus capacitor voltage is decided according to the active power requirement of the system. It can be calculated as

$$V_{dc-ref} = \frac{\sqrt{2}V_s}{\sqrt{3}m_f} \tag{3.10}$$

Here, $V_s$ = 110V is the source voltage, and $m_f$=0.8 is the modulation index. The dc reference value is calculated as 112.25V for each H-bridge. A combined value of 200V is taken as this system total dc reference voltage.

### 3.4.4 Design and Development of Current Sensors [24]

LEM makes an LA-25P current sensor for sensing the grid and load current. It provides galvanic isolation between electronic and power circuits. According to the application, this transducer connection has been made. With a conversion ratio of 1000:1, it provides a nominal value of 25A while shorting the input pins (1,2,3,4,5) and output pins (6,7,8,9,10), as shown in Fig 3.9. A ±15V supply is required to operate this sensor, the output voltage is measured across resistance ($R_{io}$), and the signal is fed to the amplification circuit. The experimental representation of the current sensor is shown in Fig 3.9.

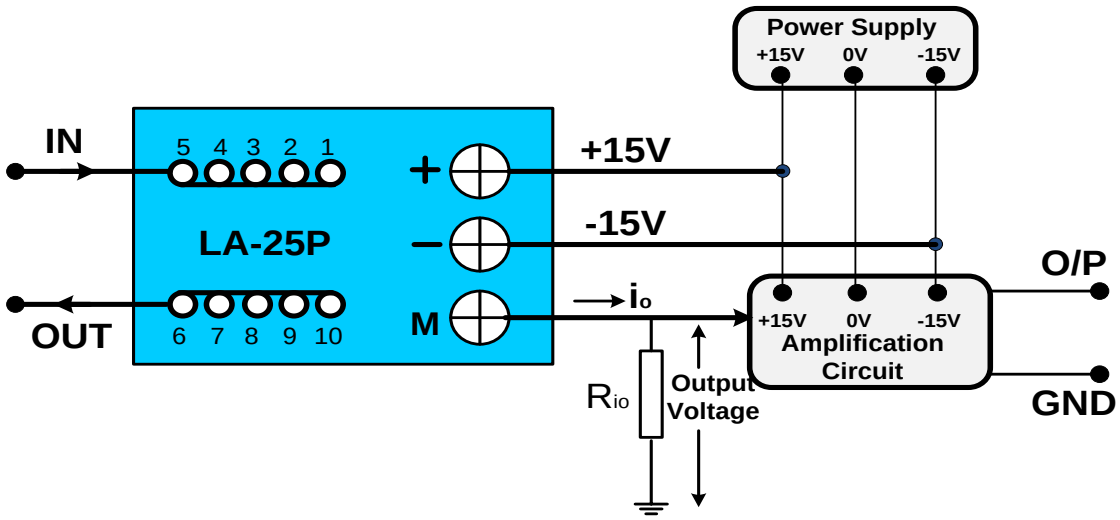



**Fig 3.9** Connection diagram of current sensor

### 3.4.5 Design and development of Voltage Sensor[24]

LEM makes LV-25P voltage sensors are used for sensing the PCC voltage and voltage across DC link capacitors. This sensor has a conversion ratio of 2500:1000; it provides the nominal value of 25V while shorting the input pins (1,2,3,4,5) and output pins (6,7,8,9,10), as shown in Fig 3.10. A ±15V supply is required to operate this sensor. The input voltage signal is fed to +HT and -HT terminals; the output voltage is measured across

terminal M across resistance ($R_{vo}$), and a further signal is provided to the amplification circuit . The experimental representation of the voltage sensor is shown in Fig 3.10

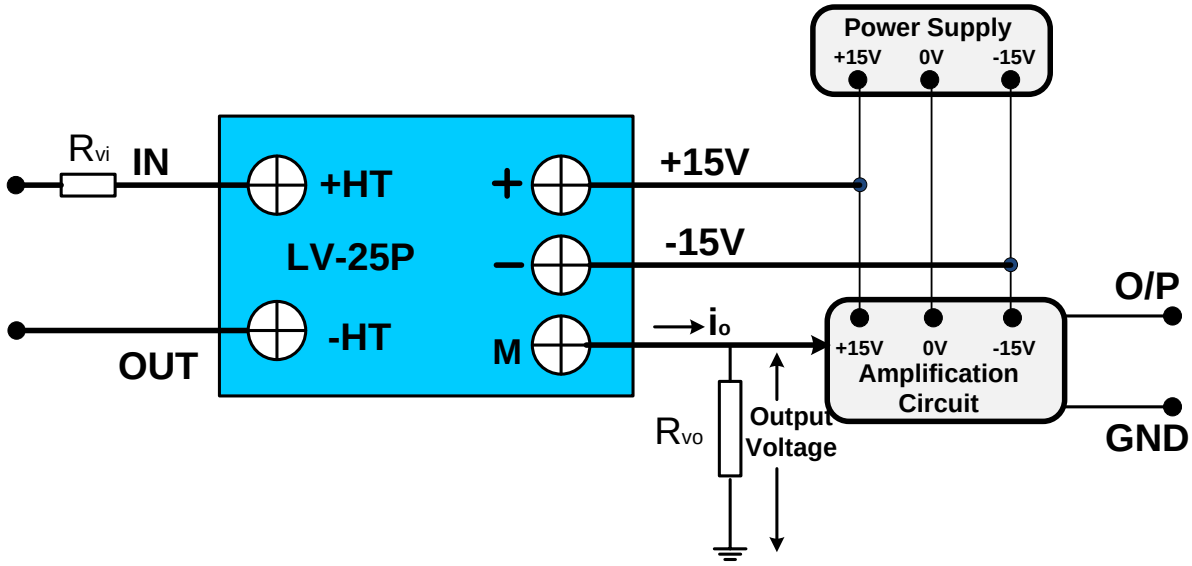



**Fig 3.10** Connection diagram of voltage sensor

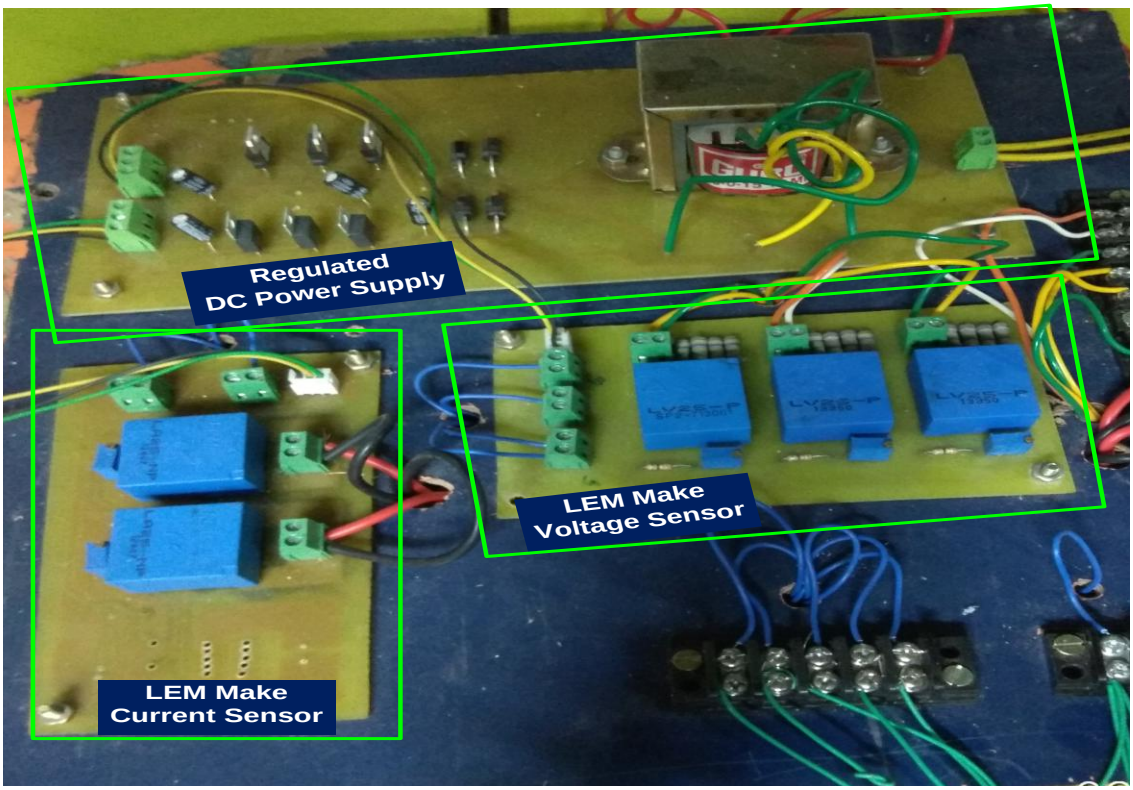
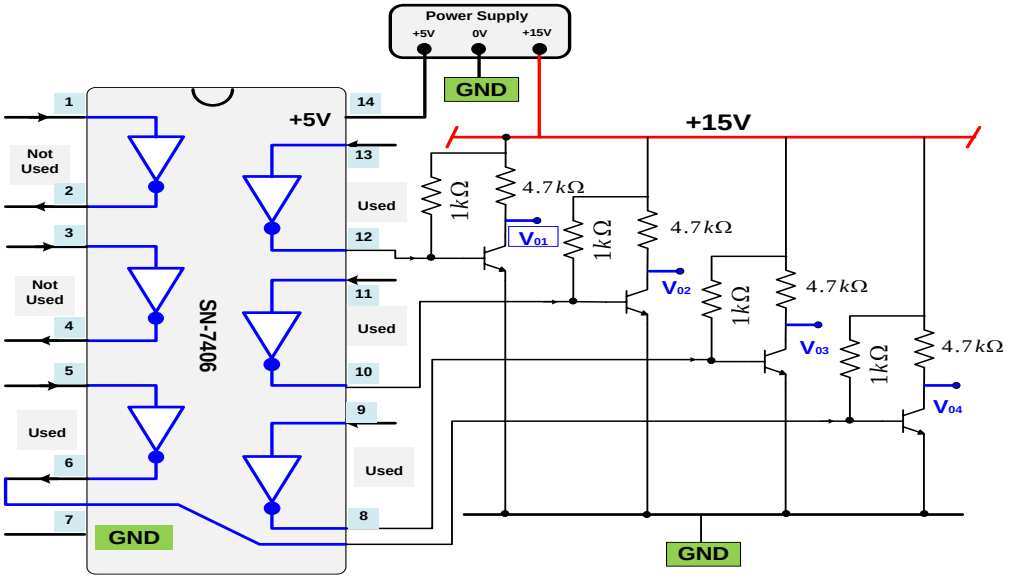


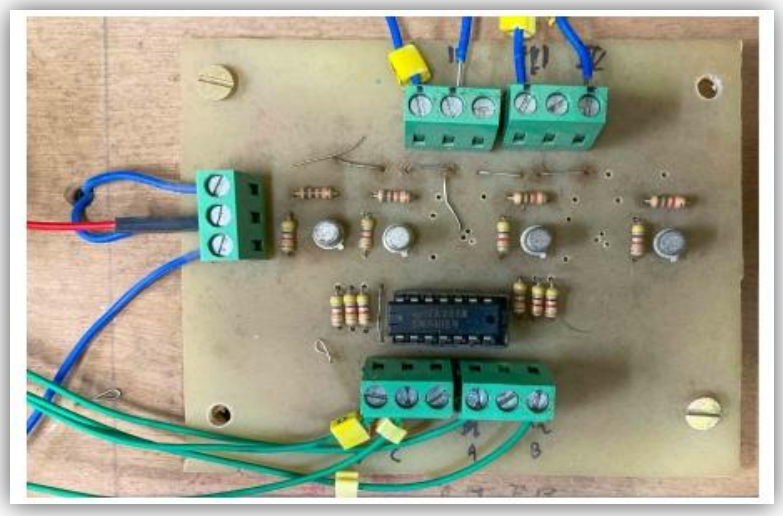

**Fig 3.11** Experimental connections of Current and Voltage sensors

### 3.4.6 Design of Amplifier Circuit[24]

The dSPACE-1104 generates a PWM signal of nearly +5V, and the voltage needed to trigger the IGBTs is +15V. Therefore, an amplification circuit has to be connected between the dSPACE-1104 and the driver circuit (SKYPER-32 pro), as shown in Fig 3.12(a). It consists of AND Gate IC-7406 and transistor 2N222. IC required +5V DC supply, and the NPN transistor needed a +15V DC supply. The experimental photograph of the circuits is shown in Fig 3.12 (b).




(a)



(b)

**Fig 3.12 (**a) Amplification Circuit diagram (b) Practical Implementation of Amplification circuit driver circuit

### 3.4.7 Design of Phase Shifted PWM Scheme

The switching pulses of CHB-MLI are generated by using the Phase shift modulation control technique [40]. A triangular carrier wave is compared with a signal generated by sensed source current ($i_s$) and reference supply current ($i_s$*). In this modulation scheme, the carrier signals are Phase shifted by angle and are given by

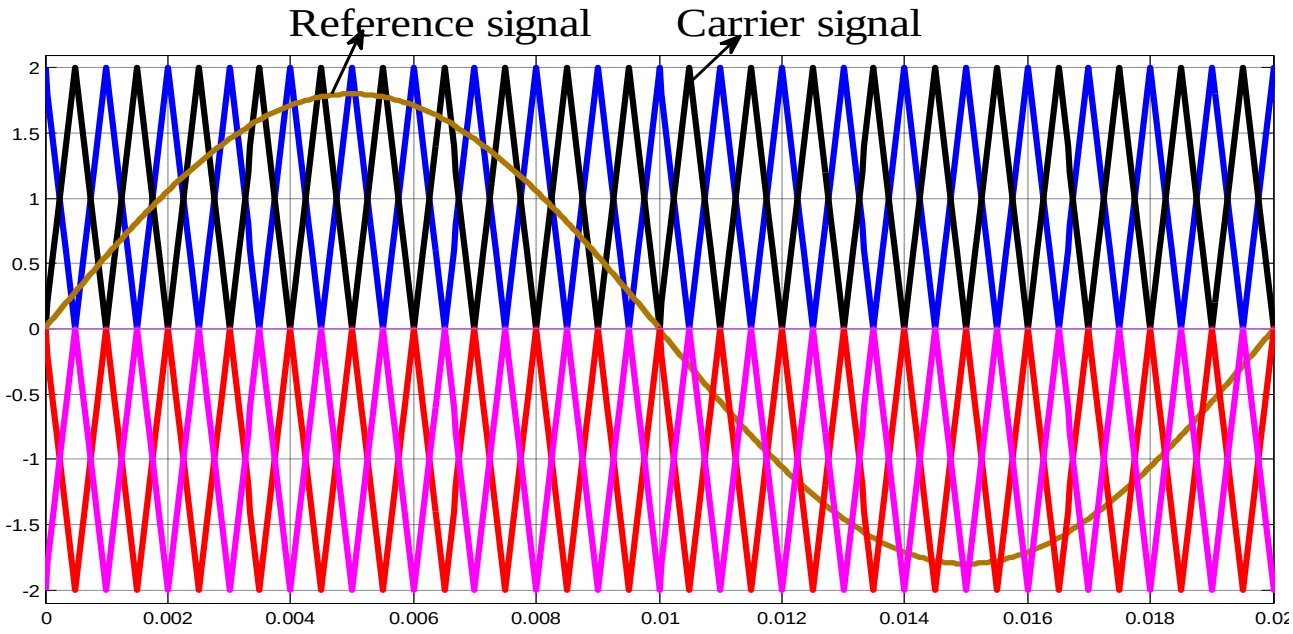
$$\phi_{cr} = \frac{360^0}{m-1} \tag{3.11}$$

where m denotes the number of output voltage levels. In the proposed CHB-MLI SAPF, the modulating signal is selected as the reference signal. It is compared with a triangular carrier signal (f=5kHz) at every instant to decide the switching pulses of IGBT switches. Fig 3.13 shows the PS-PWM technique, and the modulation frequency ( $m_f$ ) index is defined as

$$m_f = \frac{f_{cr}}{f_m} \tag{3.12}$$

where $f_{cr}$ and $f_m$ represent the frequency of the carrier and modulating signal, respectively. The switching frequency of the inverter can be calculated with the following expression

$$f_{inv} = (m-1) f_m \times m_f \tag{3.13}$$



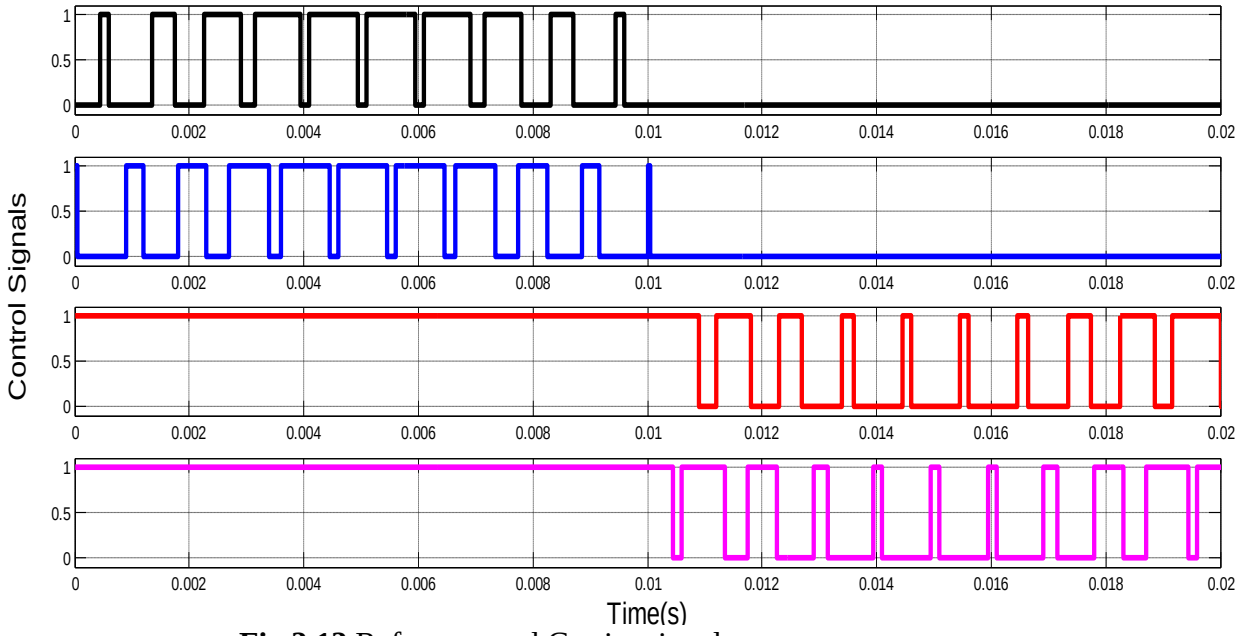



**Fig 3.13** Reference and Carrier signals at $m_f = 20$, $m_a = 0.9$

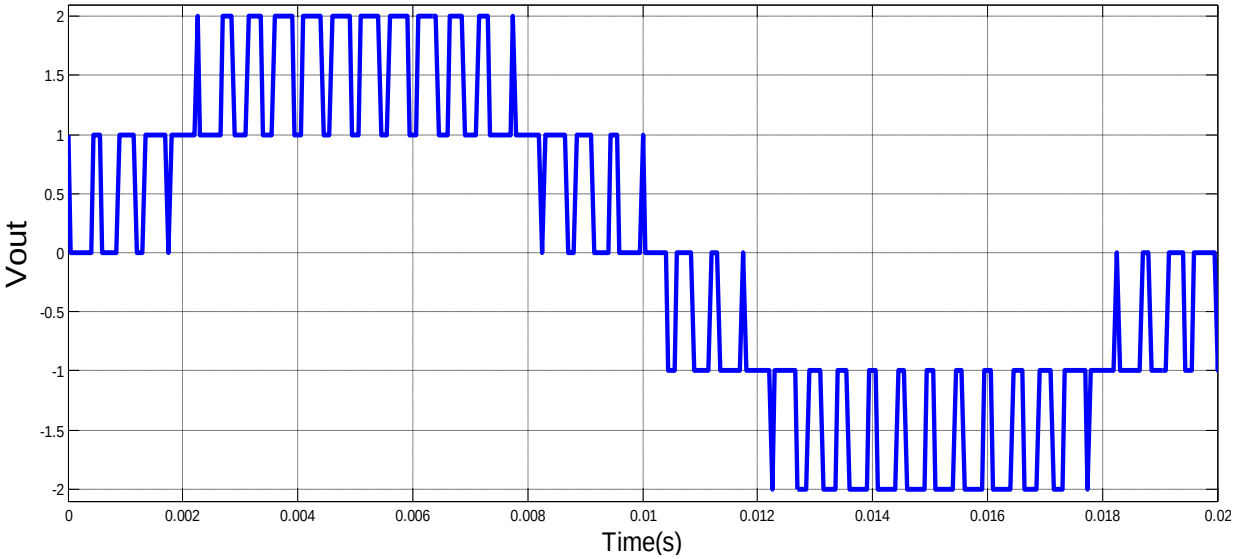



**Fig 3.14** Output Phase Voltage ($V_{out}$) of 5-level MLI

### 3.4.8 Design of PV array module[25]

Around the world, there is a significant concern with the use of energy resources and their exhaustion soon. Power engineers and researchers are compelled to look into new energy sources because the current natural energy sources are finite, and the power demand is increasing exponentially. In nature, solar energy is widely accessible and it is cost-free. The question is how to effectively and efficiently extract this energy. Significant benefits of solar energy over traditional power systems include:

1. Solar cells use the photovoltaic effect to directly convert solar energy into electricity before even passing through a thermal process.
2. Solar cells are suitable for isolated and distant locations since they are dependable, modular, long-lasting, and typically maintenance-free.
3. Solar cells are silent and should last for at least 20 years. Solar cells can only convert energy at 17–20%.
4. Due to the often low solar intensity, huge areas of solar cell modules are needed to produce enough usable electricity.

A practical inverter circuit that injects harmonic free currents into the grid system is necessary for a solar system that is connected to the grid. The PV array injects a ripple current into the grid. The amount of the ripple depends on the switching frequency, the number of isolated input voltage levels, and an interconnecting inductor. A power circuit topology's level count can lower the ripple in the output current. Because the voltage differential across the inductor is smaller when the levels are higher, the ripple is reduced. The filter effect diminishes as the number of levels increases since the switching frequency can be decreased. Therefore, using multilayer inverters to connect a PV system to the grid is an obvious choice.

A solar cell can be modeled in several ways, taking various factors into account. The single-diode model with series and parallel resistance is thought to be simpler to model and closer to the practical diode [1,128]. Fig. 3.15 depicts the single-diode model with series and shunt resistance.

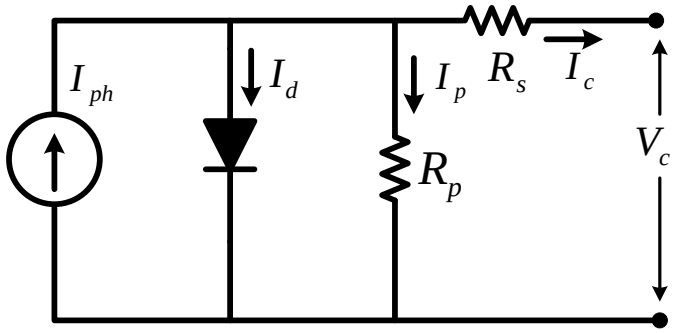



**Fig 3.15** Single Diode model of PV array

By using KCL the equation of output current (IC) is calculated as

$$I_c = I_{ph} - I_d - I_p$$

(3.14)

$$I_c = I_{ph} - I_o\left[\exp(\frac{V_c + IR_s}{a}) - 1\right] - \frac{V_c + IR_s}{R_p} \quad (3.15)$$

where, Photo Current = $I_{Ph}$; diode current=$I_d$; leakage current in parallel resistors=$I_p$;and ideality factor =a ; can be defined as

$$a = \frac{N_s\, A k T_c}{q} \quad (3.16)$$

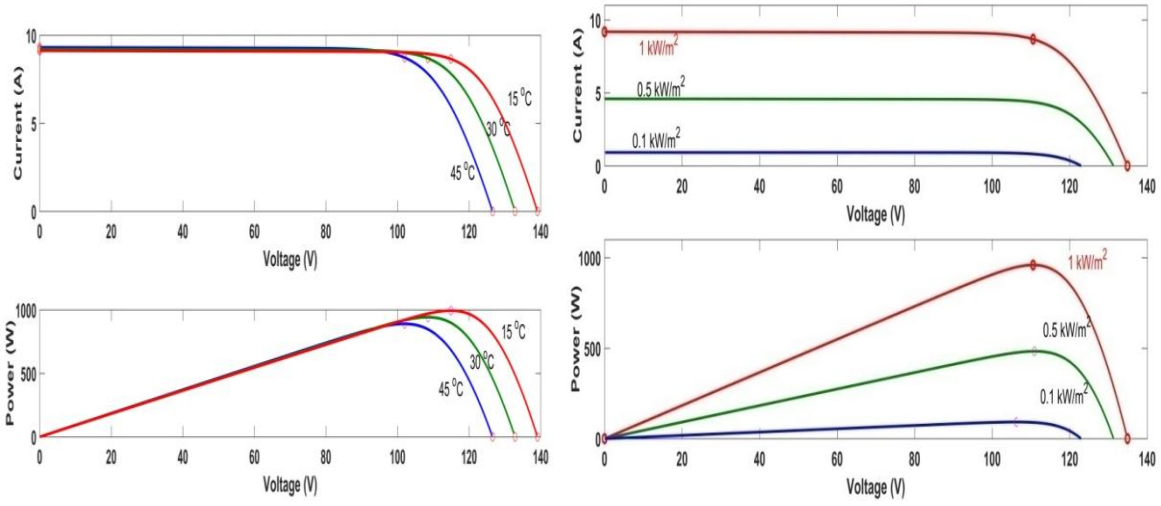
where k= Boltzmann constant =1.381x10$^{-23}$; q=1.602x10$^{-19}$;A= diode ideality factor, whose value is considered to be 1.4 for silicon polycrystalline array module; $N_s$= no. of cells in series of PV array; $T_c$= temperature. In the MATLAB/Simulink, the PV panel considered parameters are tabulated in Table 3.4

Table 3.4: User-defined parameters of PV array module

| **Parameters** | **Ratings** |
|---|---|
| Maximum power | 319.858W |
| Cells per module ($N_{cell}$) | 72 |
| Open Circuit Voltage ($V_{oc}$) | 44.97V |
| Short Circuit Current ($I_{sc}$) | 9.18A |
| Voltage at maximum power $V_{mp}$ | 36.85V |
| Current at maximum power $I_{mp}$ | 8.68A |
| Shunt Resistance $R_{sh}$ | 577.829Ω |
| Series Resistance $R_{se}$ | 0.3304 Ω |
| Temperature coefficient of $V_{oc}$ (%/deg.C) | -0.31 |
| Temperature coefficient of $I_{sc}$ (%/deg.C) | 0.069 |

In particular, the irradiance and temperature significantly impact the PV array module's performance. Fig 3.16(a,b) shows a module's P-V and I-V curves. The PV current and the power fluctuate significantly as the irradiance changes, as shown in Fig 3.16(a). Nevertheless, the variance in PV power production is less noticeable as the PV module's

temperature changes. Low power is produced at higher temperatures, while a PV array's output power is higher at lower temperatures, as depicted in Fig 3.16(b).




(a) (b)

**Fig 3.16** I-V and P-V Characteristics (a) Fixed temperature of 25°C at varying irradiance (b) Fixed irradiance of 1000w/m$^2$ at varying temperatures

### 3.4.9 Experimental Hardware Setup

The performance of various time-domain, adaptive algorithms is tested experimentally using a scaled-down prototype model developed in the laboratory. It consists of single Phase CHB-MLI, dc link capacitors $C_1$ and $C_2$, interfacing inductor $L_f$, and diode rectifier used as non-linear load. Three voltage sensors (LEM LV-25) are used to sense the source and dc link voltages. Two current sensors (LEM LA-25P) sense load and source currents. The sensed input is fed to a digital signal processor (DSP) through the channels of ADC (Analog to Digital converter). The DSP generates pulse width modulation (PWM) pulses which are driven by gate drive and isolation circuits to enhance the amplitude of PWM signals. The algorithms are executed in real-time with a sampling time of 50µs. A 4-channel DSO (Agilent X-2014A) and Fluke power quality analyzer (43-B) is used to visualize the steady and dynamic results

**Table 3.5: List of control parameters of experimental testing**

| S.No. | Control parameters | Experimental values |
|---|---|---|
| 1. | Source voltage (Vs) | 110V (rms), AC |

| | | |
|---|---|---|
| 2. | Source side inductance | 200V |
| 3. | Interfacing inductor | 3mH |
| 4. | Non-linear load | R=40Ω and L=90mH |
| 5. | DC link reference value | 200V |
| 6. | DC link capacitance | $C_{DC}$=3500µF |
| 7. | PI controller gains | $K_p$=1.3, $K_i$=0.96 |
| 8. | Switching frequency | 5kHz |

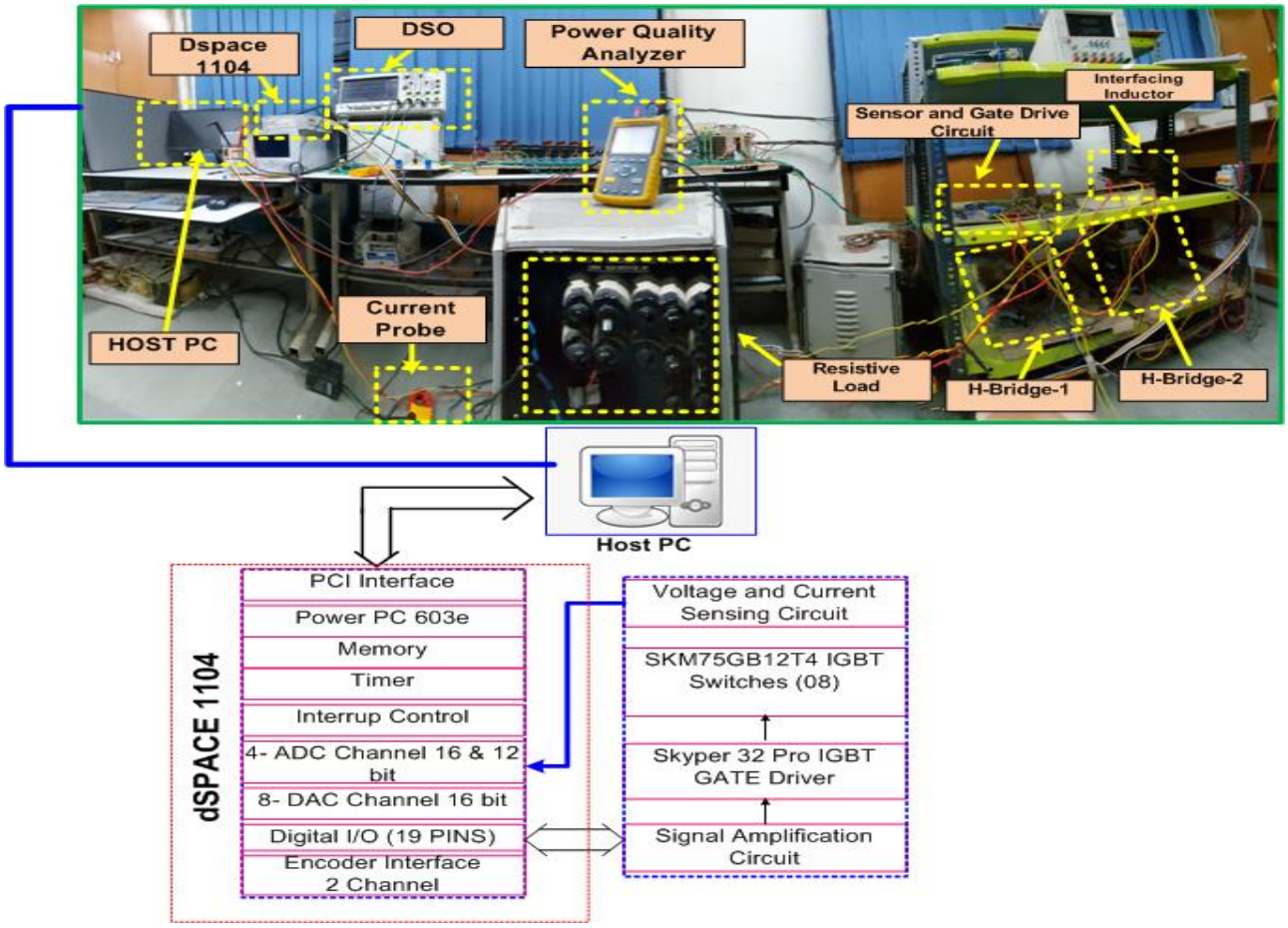



**Fig 3.17** Scaled down prototype model of the proposed system

## 3.5 Comparison between Conventional 2-level and 5-Level Multilevel Inverter

The generalized system configuration showing conventional two-leg configuration is shown in Fig 3.18(a). Two H-bridge in cascade connection are used to generate 5-level AC

output voltage as shown in Fig 3.18(b). Here, the generalized function '$S_z$' defines a switching function for the output of a bridge, which is mathematically given in Equation 3.17. It is controlled so that two switches in each bridge do not remain switched on simultaneously. Two switching functions 'Sxj' and 'Syj' are defined as a generalized function for each leg of CHB-MLI. As shown in Fig 3.18(b), 'x' denotes the first leg and 'y' denotes the second leg. Furthermore, j=‘1' represents the upper bridge, and j=‘2' the lower bridge. The switching states and voltage levels are given in Table 3.6 and Table 3.7.

The symbols $R_1$ and $R_2$ represent the equivalent power losses in the upper and lower bridge and $C_{DC1}$ and $C_{DC2}$ denote the dc-link capacitors. $I_{pxj}$ and $I_{pyj}$ represent the current in leg 'x' and leg ‘y’, respectively.

The generalized function ‘$S_{xj}$’ and ‘$S_{yj}$’ is represented as

$$S_z = \begin{Bmatrix} S_{xj} = \begin{Bmatrix} +1 & if\ upper\ switch = ON \\ -1 & if\ lower\ \ switch = ON \end{Bmatrix} \\ S_{yj} = \begin{Bmatrix} +1 & if\ lower\ switch = ON \\ -1 & if\ upper\ switch = ON \end{Bmatrix} \end{Bmatrix} \qquad (3.17)$$

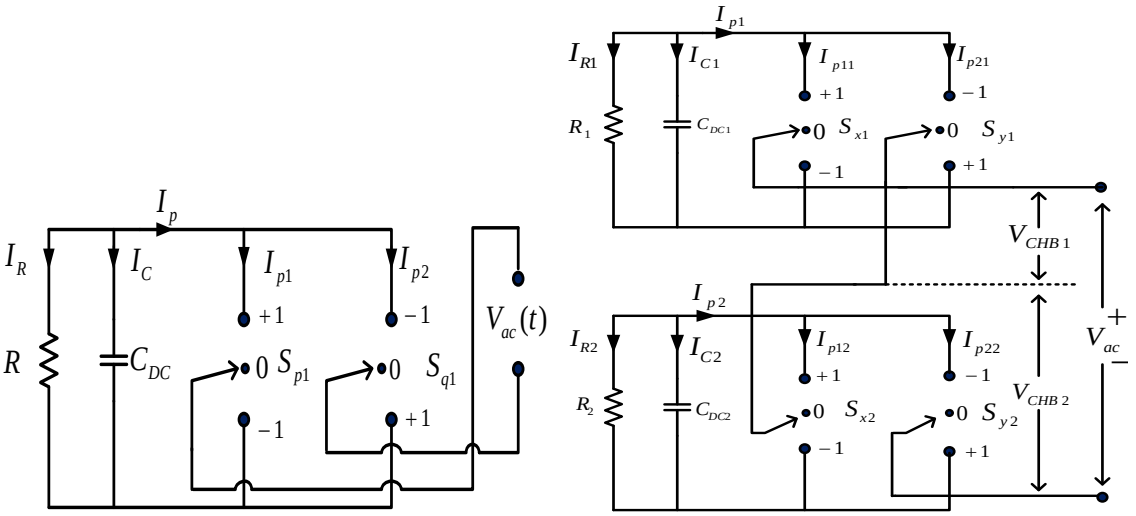



**Fig 3.18** (a) Circuit of conventional 2L Inverter (b) Circuit of 5L CHB-MLI

The output of CHB-MLI is represented as

$$V_{inv}(t)=\sum_{k=1}^{n}V_k(t) \tag{3.18}$$

$$\text{where, } V_k(t)=\sum_{k=1}^{n}(S_{xj}+S_{yj})\frac{V_{dc}}{2} \tag{3.19}$$

The output of the 5-level CHB Inverter in terms of switching function is given by Equation 3. The output voltage of the 2-level inverter is represented as

$$V_{ac}(t)=\sum_{k=1}^{n}(S_{pj}+S_{qj})V_{dc} \tag{3.20}$$

$S_{pj}$ and $S_{qj}$ represent the switching function of the 2-level inverter, as shown in Fig 3.18. Different switching states and switching levels of 5-level and 2-level inverters are shown in Table 3.6 and 3.7, respectively.

**Table 3.6:** Switching combinations for 2L inverter

| Level | $S_{pj}$ | $S_{qj}$ | $V_k(t)$ | PIV |
|---|---|---|---|---|
| Level- (1) | +1 | -1 | V | $V_{dc}$ |
| Level-(-1) | -1 | +1 | -V | $V_{dc}$ |

**Table 3.7:** Switching combinations for 5L inverter

| **Level** | $S_{x1}$ | $S_{y1}$ | $S_{x2}$ | $S_{y2}$ | $V_k(t)$ | **PIV** |
|---|---|---|---|---|---|---|
| Level-(2) | +1 | +1 | +1 | +1 | 2V | $V_{dc}/2$ |
| Level-(1) | +1 | +1 | +1 | -1 | V | $V_{dc}/2$ |
| Level-(0) | -1 | +1 | +1 | -1 | 0V | $V_{dc}/2$ |
| Level(-1) | +1 | -1 | -1 | -1 | -V | $V_{dc}/2$ |
| Level(-2) | -1 | -1 | -1 | -1 | -2V | $V_{dc}/2$ |

### 3.5.1 Loss calculation in CHB-MLI and Conventional 2-level inverter [50]

Generally, losses in any power switch include the total of (i) switching losses (ii) conduction loss (i.e., ON state loss), (iii) Blocking loss (i.e., off state loss), and an additional leakage current loss which is practically neglected in computations. The average conduction loss in a switch is expressed as

$$P_{c(loss)}(avg) = \frac{1}{\pi}\int_0^{\pi}\left[N_s(t)\,\rho_{cs}(t)\,i_c(t) + N_d(t)\,\rho_{cd}(t)\,i_c(t)\right] \tag{3.21}$$

where, $\rho_{cs}(t) = \left[V_s + R_s\, i^{\beta}(t)\right] i_c(t)$ (3.22)

$$\rho_{cd}(t) = \left[V_d + R_d\, i\ (t)\right] i_c(t) \tag{3.23}$$

$\rho_{cs}(t)$ and $\rho_{cd}(t)$ represent instantaneous conduction losses in transistors and diodes, $V_s$ and $V_d$ denote the ON-state voltage drops, and equivalent ON-state resistance is denoted by $R_s$ and $R_d$, respectively, and the transistor characteristics is given by β. $i_c(t)$ is the current carried by the switch at given instant of time. From Equation 3.21, the conduction loss is further represented as

$$P_{c(loss)}(avg) = \frac{1}{\pi}\int_0^{\pi}\left[\left\{N_s(t)V_s + N_d(t)V_s\right\} i_c(t) + \left\{N_s(t)\,R_s i_c^{\beta+1}(t)\right\} + \left\{N_d(t) i_c^2(t)\right\}\right] d(\omega t) \tag{3.24}$$

where, $N_s(t)$ and $N_d(t)$ represent the instantaneous number of conducting diodes and transistor devices. Similarly, total switching losses in an inverter can be calculated by aggregating the individual switching losses, and also, a linear approximation of voltage and current is considered for a switching period. This is mathematically represented during ON and OFF intervals. Energy loss in the switch during turn ON is given by

$$E_{on,k} = \int_0^{T_{ON}} V_{CE}\, i(t)\, dt \tag{3.25}$$

$$E_{on,k} = \int_0^{T_{ON}} \left[\left\{V_{o,k}\,\frac{T}{T_{ON}}\right\}\left\{-\frac{I}{T_{ON}}(T - T_{ON})\right\}\right] dt \tag{3.26}$$

$$E_{on,k} = \frac{1}{6} V_{o,k}\, I\, T_{ON} \tag{3.27}$$

where, $E_{on,k}$ is the turn ON loss of $k^{th}$ switch, $T_{ON}$ is the turn ON time, I and I' is the current in the switch after turning ON and OFF respectively, $V_{o,k}$ is the magnitude of the blocked voltage at $k^{th}$ switch. Energy loss in the switch during turn-off is represented as

$$E_{on,k} = \int_0^{T_{OFF}} V_{CE}\, i(t)dt$$

(3.28)

$$E_{on,k} = \int_0^{T_{OFF}} \left[ \left\{ V_{o,k} \frac{T}{T_{OFF}} \right\} \left\{ -\frac{I'}{T_{OFF}} (T - T_{OFF}) \right\} \right] dt \tag{3.29}$$

$$E_{on,k} = \frac{1}{6} V_{o,k}\, I' T_{OFF} \tag{3.30}$$

Let $f_k$ be the switching frequency; hence, in one second, $k^{th}$ switch will do $f_k$ transitions. Hence assuming $I = I'$ then the total switching power losses can be calculated as

$$P_s = \sum_{k=1}^{2n+2} \left[ \frac{1}{6} V_{o,k}\, I\, (T_{ON} + T_{OFF})\, f_k \right] \tag{3.31}$$

The total inverter loss can be obtained using Equation 3.25 and Equation 3.21, given as

$$P_{total} = P_{c(loss)}(avg) + P_s \tag{3.32}$$

As compared to a conventional 2L inverter, the proposed system operates with a lower switching frequency (taken as 5 kHz) and a Phase Shifted PWM scheme implemented to generate firing pulses. From Eq 3.31, $V_{o,k}$ is the blocking voltage, I is the switch current, and $f_k$ is the switching frequency. It is assumed for simplicity, in a particular switch $T_{ON}=T_{OFF,}$ and it will carry the same current I. Thus, $P_s$ can be represented as

$$P_s = \zeta V_0 f \quad where, \zeta = \left[ = \frac{1}{6} V_{o,k}\, I\, (T_{ON} + T_{OFF})\, f_k \right] \tag{3.33}$$

In 5-Level CHB -MLI, eight power switches are used with voltage blocking capacity $\frac{V_{dc}}{2}$ each (refer to Table 3.7), the switch power loss can be expressed as

$$P_{s/CHB-MLI/5-Level} = 4\zeta V_{dc} f_s \quad (3.34)$$

Similarly, for conventional 2L inverter switching loss can be represented as

$$P_{s/2-Level} = 4\zeta V_{dc} f_s \quad (3.35)$$

The power loss incurred in Equation 3.34 is lower than in Equation 3.35. Generally, conventional 2-L inverters adopt a hysteresis current control scheme that involves variable switching frequency. In addition, high switching frequency also results in high switching losses. These losses sometimes seem to be relatively high for DSP, and microcontrollers to generate firing pulses of power electronics switches

As far as Cost is concerned, double voltage blocking switches are relatively costly. The cost factor is defined by

$$\alpha = \frac{Power\ switch\ rated\ at\ 2V_o\ and\ I_o}{Power\ switch\ \ ratedat\ V_o and\ I_o}$$

(3.36)

Practically, the factor $\alpha$ varies widely, and it depends upon the power requirement of the switches as given in [51]. The per unit cost of power switches for 2-L and CHM-MLI 5-Level is expressed as

Switch Cost for CHB inverter = 2(N-1) (3.37)

Switch Cost for 2-L inverter= 4 (3.38)

Thus, the overall Cost of the proposed system is higher than the conventional 2L inverter. However, for medium voltage distribution systems, the CHB-MLI offers various advantages like operation at the lower switching frequency, low total harmonic distortions (THD), less electromagnetic interference (EMI), low voltage stress across switches, and also offers redundant states to operate in fault tolerance mode. The advantages mentioned above of CHB-MLI make the system more reliable.

## 3.6 Conclusion

This chapter covers the design and development of a single-phase grid-connected SAPF with and without PV integration. The details of the experimental prototype setup, design equations, and system configuration have been presented. A single-stage, single-phase grid-connected PV system is considered which is capable of accommodating a PV array. The advantages of multilevel inverters over conventional 2-level inverters have been considered thoroughly. Apart from the design aspects of CHB-MLI 5-level inverters, the switching logic and switching loss aspects have been discussed in this chapter,

# Chapter-04

# Performance Evaluation of MLI based SAPF using Conventional Control Techniques

## 4.0 Introduction

In this chapter, three conventional control algorithms viz Least Mean Square (LMS), Synchronous Reference Frame Theory (SRFT), and Notch Filter algorithm are developed and modeled to extract the fundamental component of the load current. The single phase grid connected system is considered in this chapter which feeds non-linear load. The control techniques are designed and integrated with a voltage regulator over the DC link voltage to improve the system power factor to unity. The estimated weights are further utilized to generate peak amplitude and consequently also required to generate reference current furthermore, the gating sequence for the 5-Level cascaded H-Bride inverter is generated. The detailed simulation and experimental results have been thoroughly discussed in this chapter after discussing the mathematical modeling of the controllers developed.

## 4.1 Basic Compensation principles of SAPF

A single-phase distribution system connecting SAPF and load at the point of common coupling (PCC) is shown in Fig 4.1. The active and reactive power of SAPF can be controlled using Equations 4.1 and 4.2. SAPF can control the active power by varying $\delta_{ST}$. The active power input charges the DC link capacitor as a result, and the capacitor voltage also raises the internal voltage of SAPF ($V_{st}$) rises. The reactive power (Q) control is obtained by varying the difference between $V_{st}$ and $V_{pcc}$. In this paper, CHB-MLI (SAPF) is controlled to meet the reactive power demand of the load

$$P_{st} = \frac{V_{st} V_{pcc}}{X_{st}} \sin \delta_{st} \tag{4.1}$$

$$Q_{st} = \frac{V_{pcc}(V_{st} \cos\delta_{st} - V_{pcc})}{X_{st}} \cong V_{pcc} \frac{(V_{st} - V_{pcc})}{X_{st}} \tag{4.2}$$

Fig 4.2 describes the phasor diagram of voltage at PCC ($V_{pcc}$), SAPF current ($I_{st}$), and inverter output voltage ($V_{st}$) form in the PQ plane. The interfacing inductive

reactance of the inverter is represented as $X_{st}$ , and source reactance is $X_s$ . The SAPF supplies (+Q) reactive to PCC i.e., $V_{st}$ is higher than the $V_{pcc}$. Similarly, it will absorb (-Q) where $V_{pcc}$ voltage leads the converter output voltage $V_S$. However, in practice, the converter is associated with inherent internal losses such as non-idealities in power semiconductor switches and passive elements. So, capacitance's voltage magnitude continuously decreases to compensate for these losses. Therefore, to regulate the capacitance-voltage, there is a small phase shift of $\delta_{ST}$ is introduced in between the SAPF and PCC voltage.

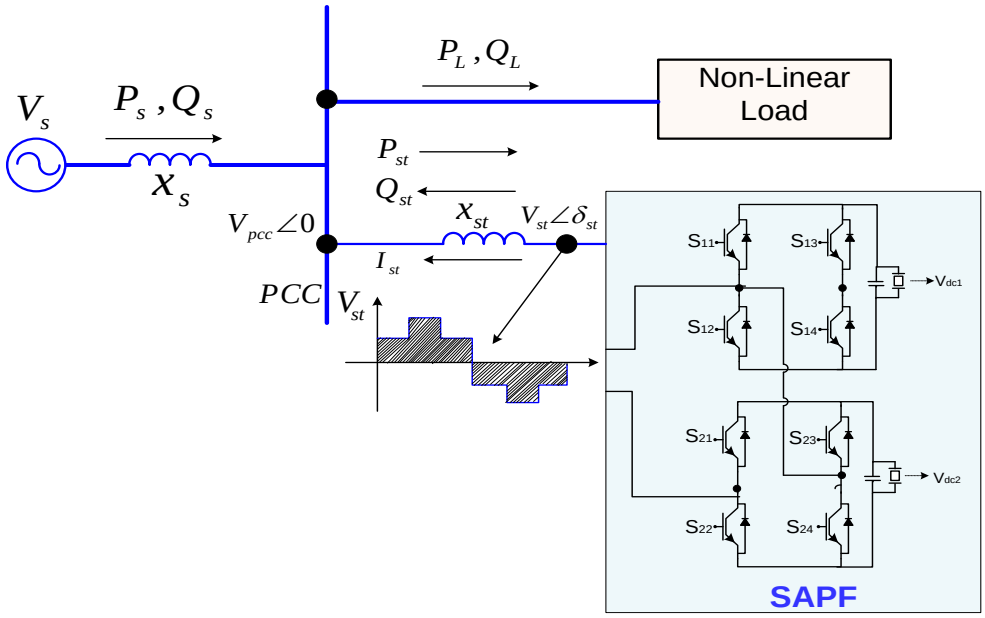



**Fig 4.1** Schematic of single-phase distribution system

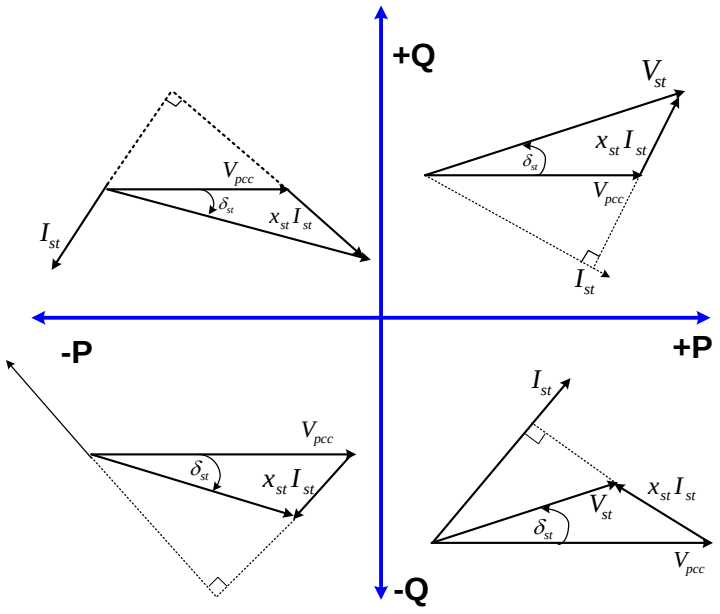



**Fig 4.2** Operating Characteristics of SAPF

## 4.2 Switching Configurations of 5-Level CHB-MLI

The generalized system configuration is shown in Fig 4.3. Two H-bridge in a cascaded connection are used to generate a 5-level AC output voltage. Here, the generalized function '$S_z$' defines a switching function per unit of output voltage, which is mathematically given in Equation 4.3. It is switched so that two switches in each bridge do not remain switched on simultaneously.

In Equation 4.3, two switching functions, 'Sxj' and 'Syj' are defined as a generalized function for each leg of CHB-MLI. As shown in Fig 4.3 'x' denotes the first leg, and 'y' denotes the second leg. Furthermore, j= '1' for the upper bridge and j='2' for a lower bridge. The different switching states, along with varying levels of voltage, are given in Table 4.1

The symbols $R_1$ and $R_2$ represent the equivalent power losses in the upper and lower bridge, and $C_{dc1}$ and $C_{dc2}$ denote the dc-link capacitors; $I_{pxj}$ and $I_{pyj}$ represent the current in leg 'x' and leg 'y', respectively

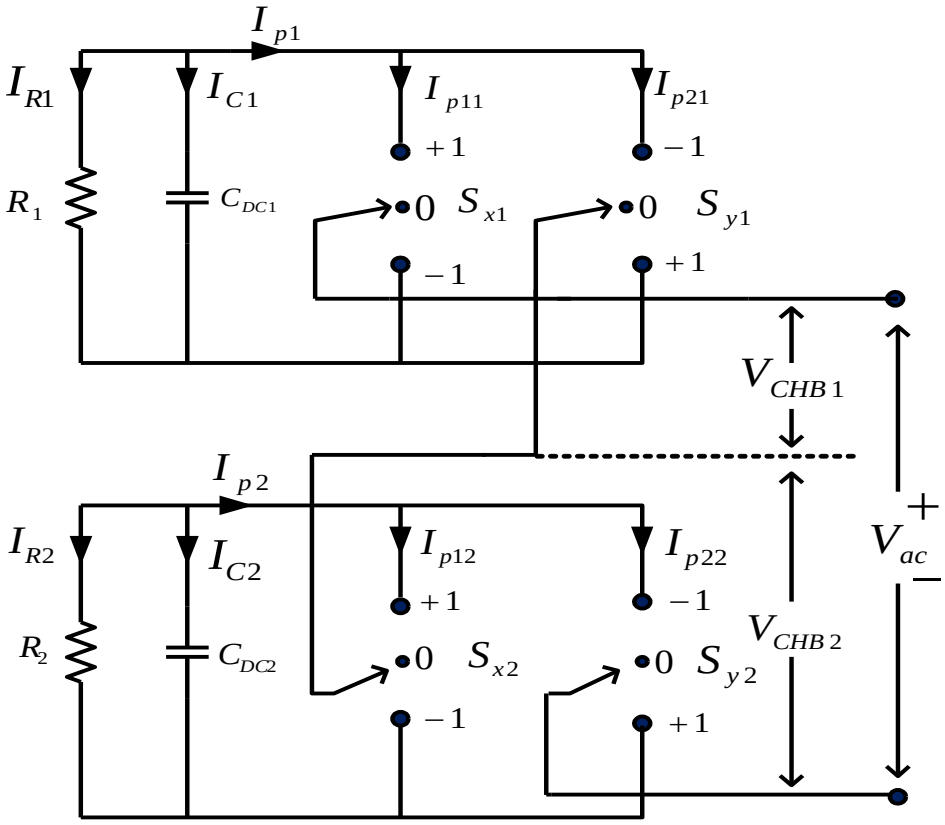



**Fig 4.3** Generalized circuit of 5-level MLI

**Table-4.1** Switching States and corresponding voltage levels

| **Voltage levels** | **$V_{CHB1}$** | **$V_{CHB2}$** | **$S_{x1}$** | **$S_{y1}$** | **$S_{x2}$** | **$S_{y2}$** |
|---|---|---|---|---|---|---|
| 2 $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | +1 | +1 | +1 | +1 |
| $V_{dc}$ | $V_{dc}$ | 0 | +1 | +1 | -1 | +1 |
| | $V_{dc}$ | 0 | +1 | +1 | +1 | -1 |
| | 0 | $V_{dc}$ | -1 | +1 | +1 | +1 |
| | 0 | $V_{dc}$ | +1 | -1 | +1 | +1 |
| 0 | $-V_{dc}$ | $V_{dc}$ | -1 | -1 | +1 | +1 |
| | $V_{dc}$ | $-V_{dc}$ | +1 | +1 | -1 | -1 |
| | 0 | 0 | +1 | -1 | -1 | +1 |
| | 0 | 0 | +1 | -1 | +1 | -1 |
| | 0 | 0 | -1 | +1 | -1 | +1 |
| | 0 | 0 | -1 | +1 | +1 | -1 |
| $-V_{dc}$ | $-V_{dc}$ | 0 | -1 | -1 | -1 | +1 |
| | $-V_{dc}$ | 0 | -1 | -1 | +1 | -1 |
| | 0 | $-V_{dc}$ | +1 | -1 | -1 | -1 |
| | 0 | $-V_{dc}$ | -1 | +1 | -1 | -1 |
| $-2V_{dc}$ | $-V_{dc}$ | $-V_{dc}$ | -1 | -1 | -1 | -1 |

$$S_z = \begin{Bmatrix} 1 \ if \ S_{x1}, S_{y1}, S_{x2}, and \ S_{y2} = 1 \\ \frac{1}{2} \ if \begin{Bmatrix} case-1 \ S_{x1}, S_{y1} = 1 \ and \ (S_{x2} \& S_{y2}) \ are \ of \ opposite \ sign \\ case-2 \ S_{x2}, S_{y2} = 1 and \ (S_{x1} \& S_{y1}) \ are \ of \ opposite \ sign \end{Bmatrix} \\ 0 \ if \begin{Bmatrix} case-1 \ S_{x2,} \ S_{y2} = 1 and \ (S_{x1} \& S_{y1}) \ are \ of \ opposite \ sign \\ case-2 \ S_{x1}, S_{y1} = 1 \ and \ (S_{x2} \& S_{y2}) \ are \ of \ opposite \ sign \\ case-3 \ (S_{x1} \& S_{y1}) \ and \ (S_{x2} \& S_{y2}) \ are \ of \ opposite \ sign \end{Bmatrix} \\ -\frac{1}{2} \ if \begin{Bmatrix} case-1 S_{x1}, S_{y1} = -1 \ and \ (S_{x2} \& S_{y2}) \ are \ of \ opposite \ sign \\ case-2 \ S_{x2}, S_{y2} = -1 \ and \ (S_{x1} \& S_{y1}) \ are \ of \ opposite \ sign \end{Bmatrix} \\ -1 \ if \ S_{x1}, S_{y1}, S_{x2} \ and \ S_{y2} = -1 \end{Bmatrix} \quad (4.3)$$

## 4.3 Operation of 5-Level Shunt Active Power Filter

Fig 4.4 shows the schematic diagram of single-phase 5-level CHB-MLI SAPF connected to single-phase grid AC mains feeding the non-linear load. The sensed input variables are voltage at the point of common coupling (PCC), load current ($i_L$), source current ($i_s$), and dc bus voltages $V_{dc1}$, $V_{dc2}$. An interfacing inductor ($L_f$) is connected in CHB-MLI to reduce the ripples in ac output. SAPF unit is current-controlled using several adaptive control techniques to inject suitable compensating current in phase opposition to eliminate the harmonics generated by the load current. For effective operation of the CHB-MLI, both the dc-link voltages must be maintained at a constant

level, and the conventional PI controller realizes this function. All the developed controllers are first simulated and thoroughly tested using MATLAB/Simulink platform. The performance of various algorithms are tested experimentally using a scaled-down prototype model developed in the laboratory. It consists of single phase CHB-MLI, dc link capacitors $C_1$ & $C_2$, interfacing inductor $L_f$, and diode rectifier used as non-linear load. Three voltage sensors (LEM LV-25) are used to sense the source and dc link voltages. Two current sensors (LEM LA-25P) are used to sense the load and source current. The sensed input is fed to a digital signal processor (DSP) through ADC (Analog to Digital converter) channels. The DSP generates pulse width modulation (PWM) pulses which are driven by gate drive and isolation circuits to enhance the amplitude of PWM signals. A 4-channel DSO (Agilent X-2014A) and Fluke power quality analyzer are used to visualize the steady and dynamic results.

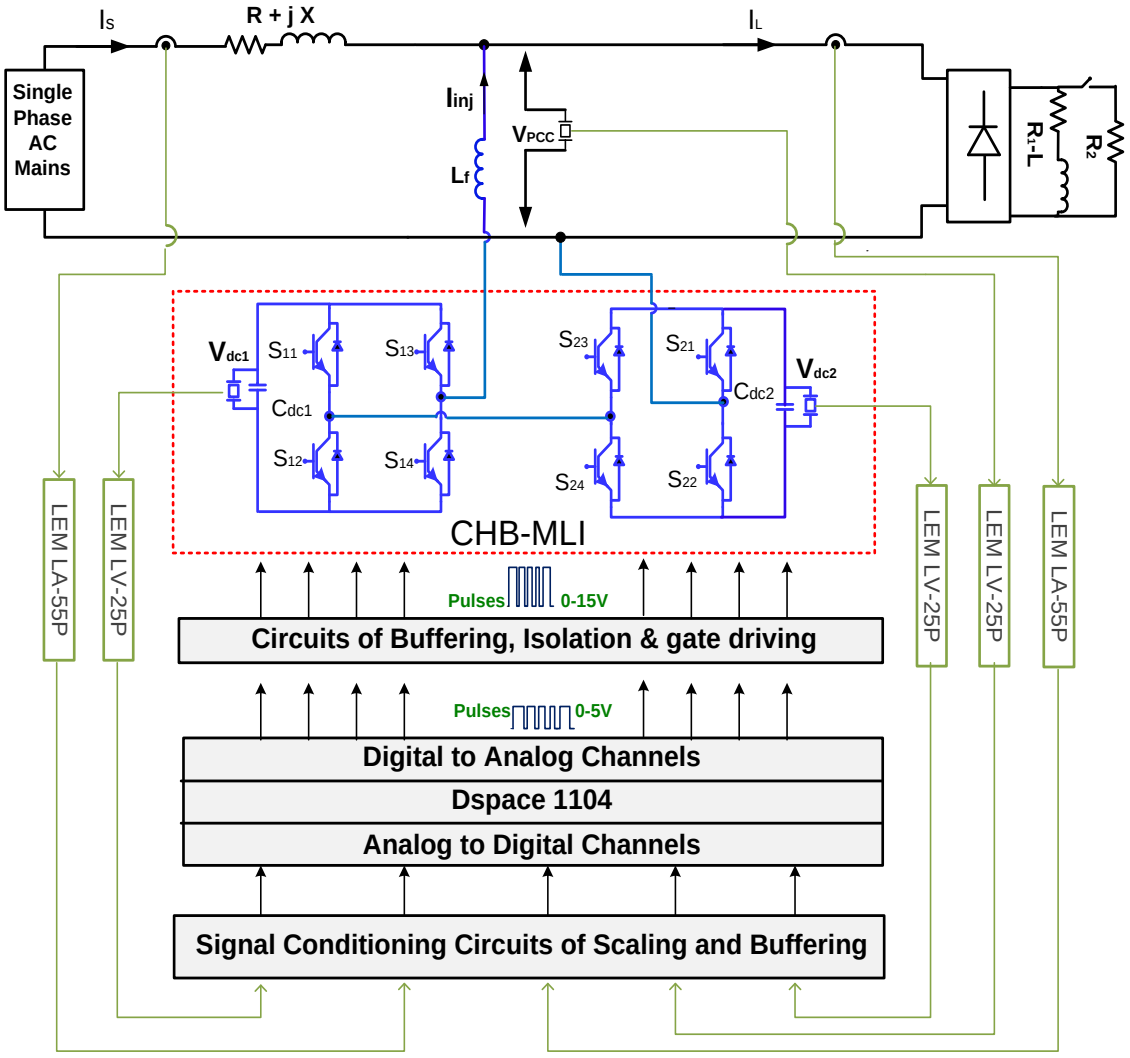



**Fig 4.4** Schematic diagram of the proposed system

## 4.4 Generalized Structure of Control Algorithm

The generalized control scheme diagram of CHB-MLI is shown in Fig 4.5. In this chapter, the controller is developed using the Least Mean Square(LMS), Synchronous Reference Frame Theory (SRFT), and Notch filter. The adaptive controller updates the weights adaptively from the previous value. The convergence of all algorithms is also analyzed during sudden transients in a later section of this chapter.

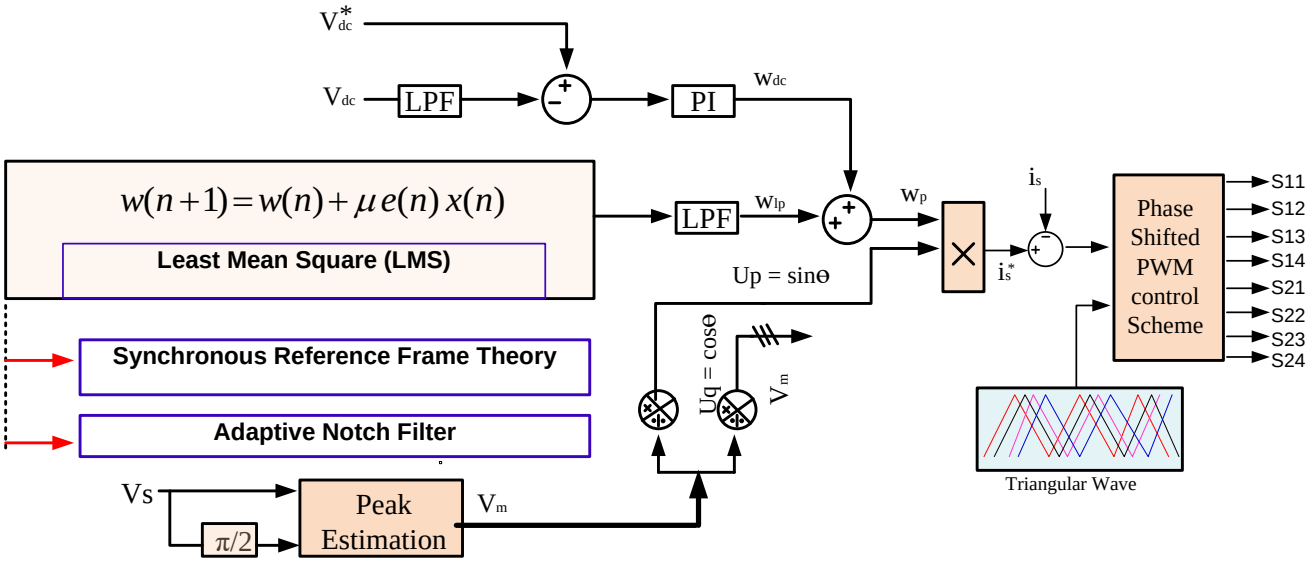



**Fig 4.5** DSP implementation of conventional algorithms

A non-linear signal is basically composed of two components, namely fundamental and harmonic, which are superimposed over each other. These signals are represented by as:

$$i_L(t) = i_{Lf}\sin(\omega t + \phi_f) + \sum_{k=3,5,7...}^{\infty} i_{Lk}\sin(\omega t + \phi_k) \tag{4.4}$$

$$i_L(t) = i_f(t) + i_k(t) \tag{4.5}$$

The load can further be classified into:

$$i_k(t) = \sum_{k=3,5,7...}^{\infty} i_k\sin(\omega t)\cos(\phi_k) + \cos(\omega t)\sin(\phi_k) \tag{4.6}$$

$$i_f(t) = i_f\sin(\omega t)\cos(\phi_f) + i_f\cos(\omega t)\sin(\phi_f) \tag{4.7}$$

Replacing $i_f\cos(\phi_f), i_f\sin(\phi_f), i_k\cos(\phi_k), i_k\sin(\phi_k)$ by $\omega_{a1}, \omega_{b1}, \omega_{ak}, \omega_{bk}$, respectively, the expression can be written as

$$i_f(t) = \omega_{a1}\sin(\omega t) + \omega_{b1}\cos(\omega t) \tag{4.8}$$

$$i_k(t) = \sum_{k=5,7,9....}^{\infty}(\omega_{ak}\sin(\omega t)) + \omega_{bk}\cos(\omega t)) \tag{4.9}$$

The estimated load current can be expressed as

$$i'_L(t) = [\omega_{a1}\ \omega_{b1}\ \omega_{ak}\ \omega_{bk}]^T[X] \tag{4.10}$$

$$\text{where}\,[X] = [\sin(\omega t)\cos(\omega t)\sin(k\omega t)\cos(k\omega)] \tag{4.11}$$

The error between the sensed value of load current ($i_L$) and the estimated value of current ($i_p$) is given as,

$$e(n) = i_L(n) - i_p(n) \tag{4.12}$$

The load current $i_p(n)$ can be calculated from the weight ( $w^T$ ), and the input vector is given by

$$i_P(n) = w^T\ x(n) \tag{4.13}$$

where the weight vector is given as,

$w = [w_{a1}w_{b1}w_{a3}w_{b3}\ldots]^T$ ; and the input vector

$x(n) = [\sin\omega n\ \cos\omega n\ \sin 3\omega n\ \cos 3\omega n.....]$

Substituting the value of Equation 4.12 in Equation 4.13, then,

$$e(n) = i_L(n) - w^T\ x(n) \tag{4.14}$$

## 4.5 Estimation of switching losses for CHB-MLI

The control algorithm not only estimates the fundamental component of load current but also computes the switching loss requirement of CHB-MLI. The sensed dc link voltage $V_{dc}$ is subtracted from the reference dc voltage $V_{dc\text{-}ref}$ to generate the error (e), which is then further processed into the PI controller to meet the switching loss of CHB-MLI, represented as

$$e = V^*_{dc-ref} - V_{dc} \tag{4.15}$$

The output of the PI controller at the $k^{th}$ sampling instant is given as

$$w_{loss} = k_p\, e_{dc} + k_d \int_0^{t_d} e_{dc}\, dt \tag{4.16}$$

Discretizing equation 4.16, then

$$w_{loss}(k) = k_p\, e_{dc}(k) + k_d \sum_{j=0}^{n} e_{dc}(k)\,\tau_d \tag{4.17}$$

For n=1,

$$w_{loss}(1) = k_p\, e_{dc}(1) + k_i\,[e_{dc}(0) + e_{dc}(1)]\,\tau_d \tag{4.18}$$

For n=2,

$$w_{loss}(2) = k_p\, e_{dc}(2) + k_i\,[e_{dc}(0) + e_{dc}(1) + e_{dc}(2)]\,\tau_d \tag{4.19}$$

The generalized calculated loss equation is given as

$$w_{loss}(k) = w_{loss}(k-1) + k_d\,[e_{dc}(k) - e_{dc}(k-1)] + k_i\, e_{dc}(k)\,\tau_d \tag{4.20}$$

where $k_i$ and $k_d$ denote the proportional and integral gains of the PI controller, and the effective weight average $w_{avg}$ is given by

$$w_{eff} = w_{avg} + w_p \tag{4.21}$$

## 4.6 Estimation of Unit Vector template

The grid supply voltage signal ($v_s$) is shifted by T/4 to obtain $90^0$ shifted quadrature components ($v_{sq}$). The in-phase component ($v_{sp}$) is the same as the input signal, and both the in-phase and quadrature components are used to estimate the peak value of supply ($V_m$) using Equations 4.22 to 4.25. The peak value is further used to generate the unit vector template, mathematically given as

$$V_{sp} = V_m \sin \omega t \tag{4.22}$$

$$v_{sq} = V_m \sin(\omega t + \pi/4) \tag{4.23}$$

$$V_t = \sqrt{v_{sp}^2 + v_{sq}^2} = V_m \tag{4.24}$$

The unit vector template can be calculated as

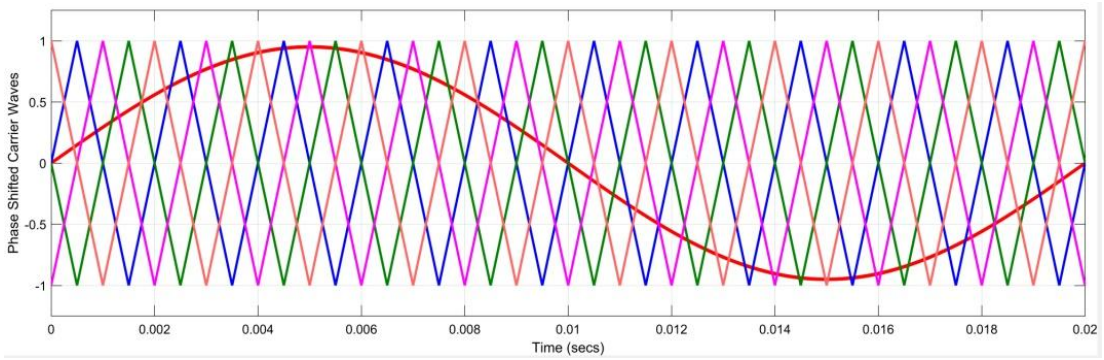
$$u_p = \frac{v_{sp}}{V_m} = \sin \omega t \tag{4.25}$$

## 4.7 Generation of Firing Pulses

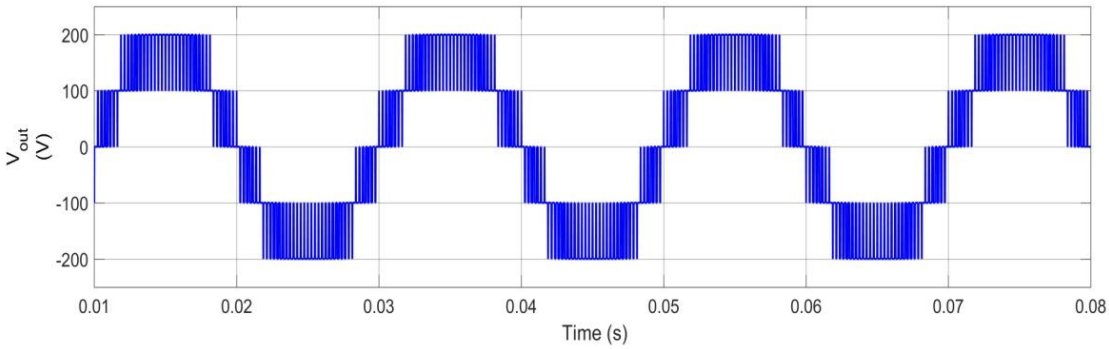
The reference current ($i_s$*) is calculated by multiplying of input signal with unit vector template ( $u_P$ ) and effective active loss ( $w_{eff}$ ) component, given as

$$i_s^* = w_{eff} * u_P \tag{4.26}$$

The source current is subtracted from obtained reference current and then further compared with the Phase shifted (PS) PWM technique employed for pulse generation. Furthermore, switching pulses are generated for controlling the Insulated Gate Bipolar transistors (IGBTs) of CHB-MLI through necessary isolation and buffer circuits. Fig 4.6 (a-b) shows the waveforms of the 5-level PS-PWM scheme and output phase voltage of CHB-MLI.




(a)




(b)

**Fig 4.6 Phase** Shifted scheme for 5-level CHB-MLI and output voltage of 5-level CHB-MLI

## 4.8 Extraction of the fundamental component of load current using Least Mean Square Algorithm

The fundamental component of load current ($I_f$) has been extracted from various control algorithms

### 4.8.1 Mathematical Formulation of Adaptive Control

Adaptive control algorithms have been widely used in diverse fields, such as noise cancellation, echo cancellation, and harmonics filtration. The performance is

measured by convergence behavior shown by the algorithm under extreme dynamic conditions. The most conventional and widely accepted adaptive control algorithm is Least Mean Square (LMS) developed by Widrow[102], which led to several adaptive control algorithms with numerous applications, especially in the field of telecommunications and signal processing. The control block diagram of the LMS algorithm is shown in Fig 4.7. For the LMS algorithm, the weight update vector equation can be written as

$$w(n+1)=w(n)+\mu e(n)\,x(n) \tag{4.27}$$

where μ is the learning rate for the least mean square technique

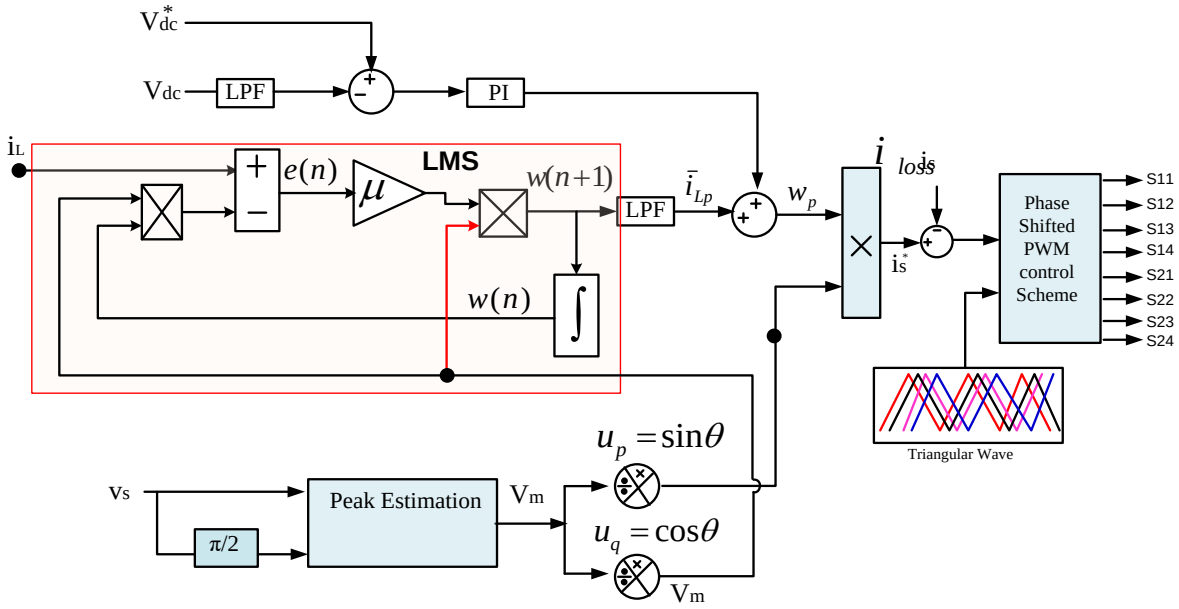



**Fig 4.7** Control block implementation with LMS algorithm

## 4.8.2 Simulation Results of LMS Algorithm

The proposed system is designed in MATLAB/Simulink to validate the simulation results and tested under varying load conditions. A single-phase 110V AC supply feeds power to a non-linear load and meets the switching losses. LMS algorithm is used to control CHB-MLI. Moreover, the reference current is generated and compared with PS-PWM to generate firing pulses for IGBTs. The proposed system achieves a unity power factor by mitigating all the harmonics generated by the non-linear load.

Fig 4.8 shows the simulated waveforms of PCC voltage ($V_{pcc}$), source current ($i_s$), load current ($i_L$), compensating current ($i_c$), inverter output voltage ($v_{inv}$), total dc link

voltage ($V_{dc}$). At t=0.4s, the load is increased till t=0.6s. Fig 4.8 the load current has increased from 3A to 6A (at t=0.4s) and decreased to 3A (at t=0.6s). Similarly, the source varies as the load is increased or decreased. However, it is clearly observed that the source current is perfectly sinusoidal. It is seen that the dc link voltage quickly self-regulates to a reference value of 200V.

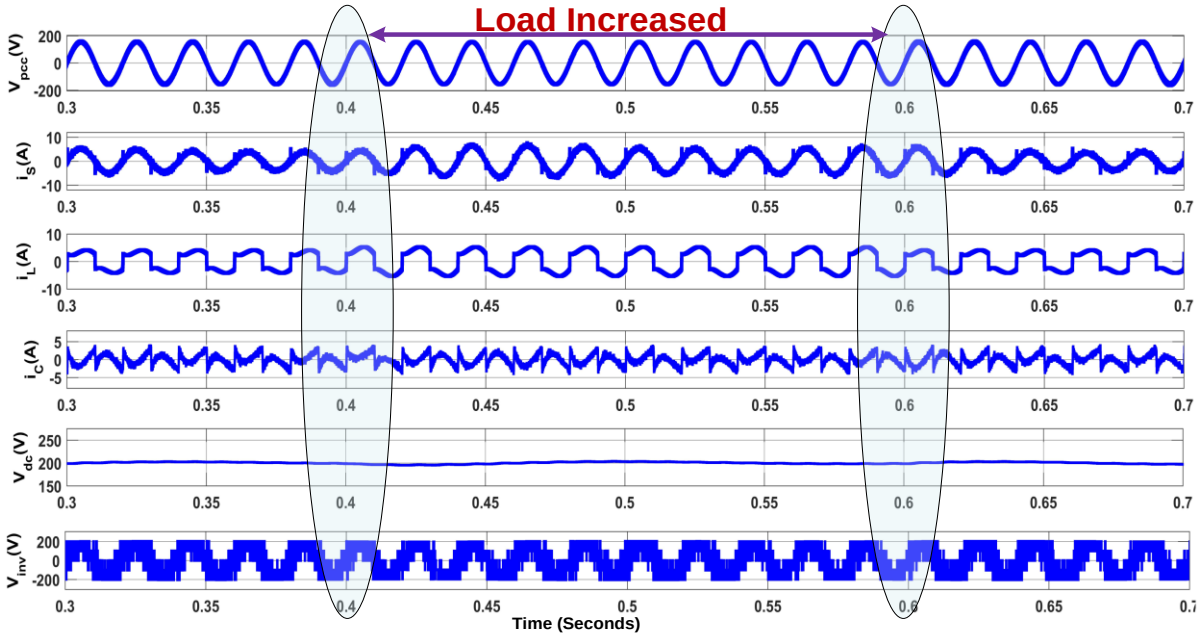
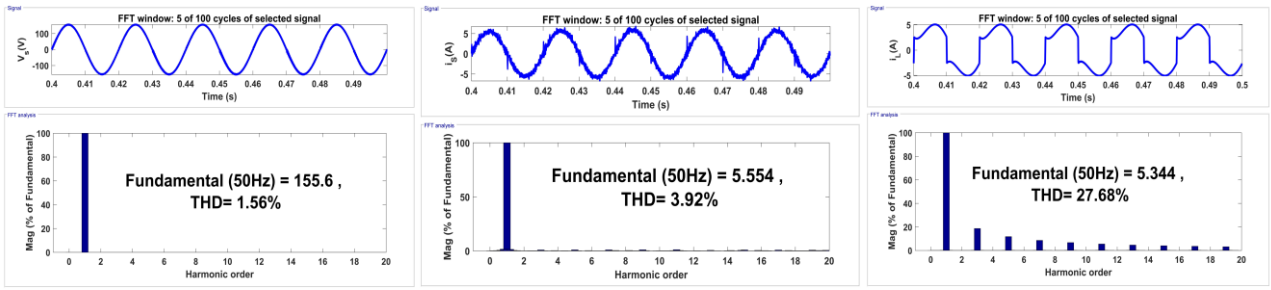



**Fig 4.8** Simulated waveforms of $v_s$,$i_s$,$i_L$,$i_C$, $V_{dc,}$ and $v_{inv}$ during load variation at t=0.4s and t=0.6s with LMS algorithm

Fig 4.9 (a-c) shows the harmonic spectra of the source current load current and source voltage. Before compensation, the source feeds the non-linear load and has a THD of 27.68%, similar to the load current, as shown in Fig 4.11(c). However, after compensation using SAPF, the THD of source current reduces drastically to 3.92%. The compensator regulates the dc link voltage via the PI controller and improves the harmonic profile of the source current by injecting compensating current in PCC.




(a) (b) (c)

**Fig 4.9 (a-c)** Waveforms of $v_s$ , $i_{S,}$ and $i_{L,}$ along with THD analysis

Fig 4.10 shows the intermediate results with the LMS algorithm. The measured parameters are load current $i_L$(A), error (e), estimated fundamental weight $w_P$(A), and inverter output voltage $v_{inv}$(V) under dynamic load conditions. As seen in Fig 4.10, the load is increased from 0.4s to 0.6s. The fundamental weights converge quickly with 2~3 cycles.

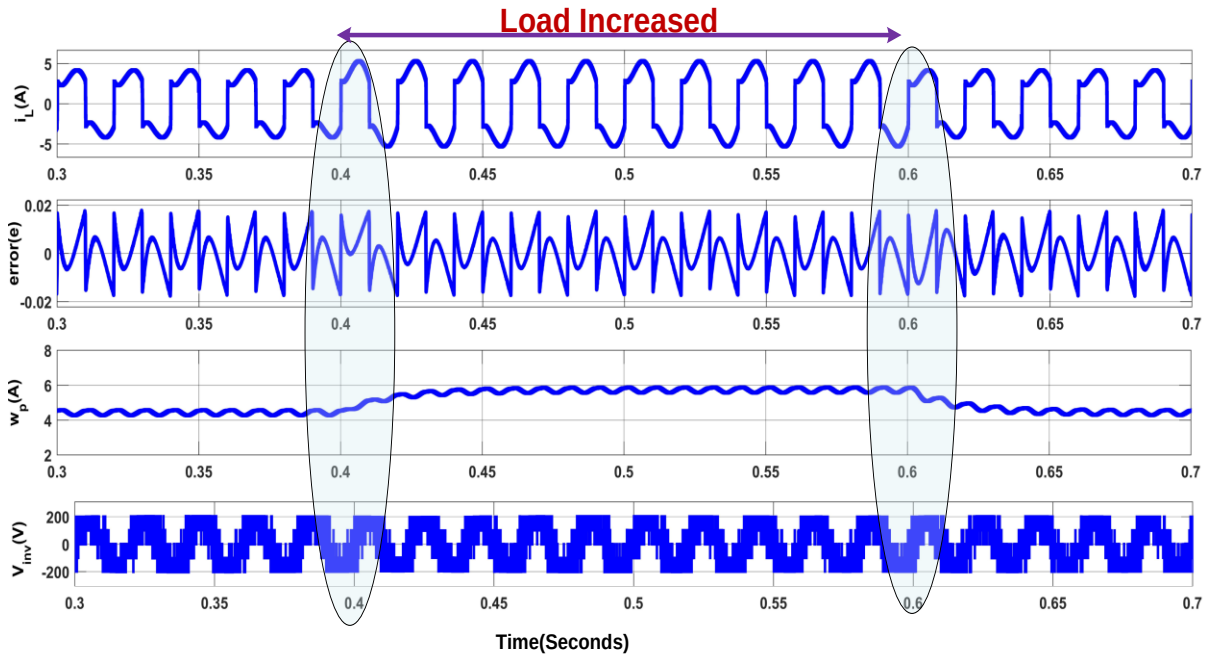


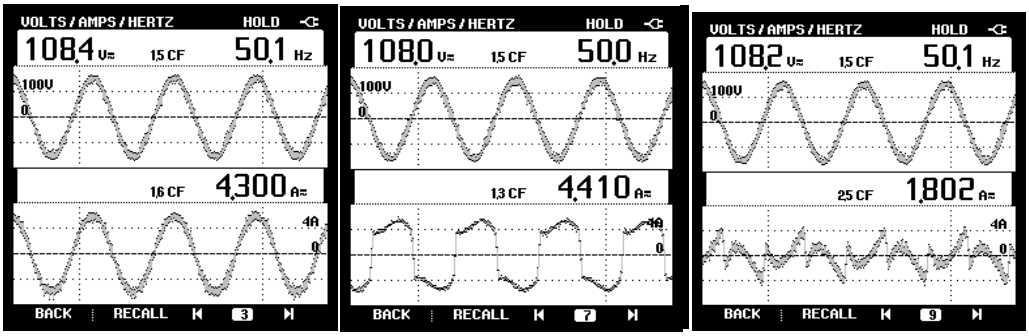

**Fig 4.10** Simulation Results of load current $i_L$(A), $w_p$(A), $i_C$(A) and $V_{dc}$(V) with LMS algorithm

### 4.8.3 Experimental Results with LMS Algorithm

, The scaled-down prototype model for a single-phase system is modeled, developed, and tested in the laboratory using a dSPACE 1104 microcontroller to validate the proposed adaptive LMS algorithm. A single phase 110V (RMS) 50 Hz supply feeds the non-linear load. A bridge diode rectifier is considered a non-linear load along with an R-L load for experimentation. The hardware setup includes an inverter circuit, a gate drive circuit, and measuring and conditioning circuits. A CHB-MLI circuit is designed using SEMIKRON SKM75GB12T4 IGBT array having a rating of 1200V, 75A. On the DC side of the inverter, two ALCON make connected electrolytic capacitors (3000µF) are connected. An interfacing inductor of value 3mH interconnects CHB-MLI to the grid. Three voltage sensors (LV-25P) are used in the proposed system to sense the voltage of the PCC ($V_{pcc}$) and the DC link voltage of capacitor-1 ($V_{DC1}$), and the DC link

voltage of capacitor-2 ($V_{DC2}$), respectively. The load current ($i_L$) and source current ($i_S$) are also sensed using two current sensors (LA-25P). By using correct scaling and gain correction factors, these voltage and current signals are amplified and brought back to their original value. Furthermore, the proposed control algorithm estimates reference current, as a result of which the dSPACE-1104 microcontroller produces a PWM voltage that is amplified to +15V using SEMIKRON make gate drive circuits (SKYPER 32 pro) to trigger SAPF IGBTs. The simulation results are verified by implementing the LMS algorithm experimentally.

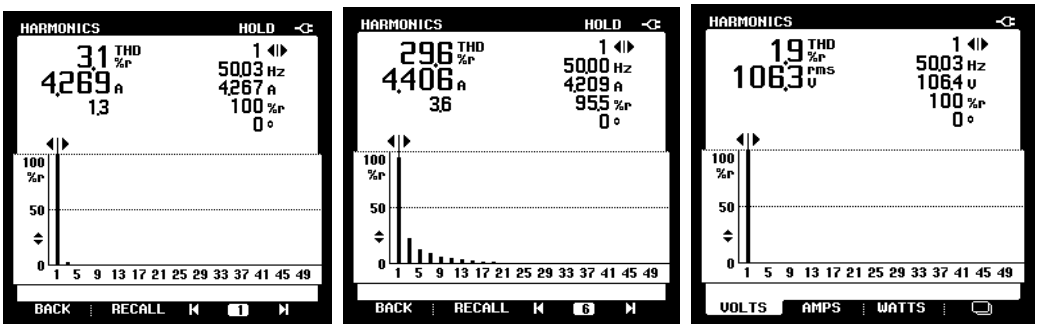
Fig 4.11 (a-c) depicts the steady-state waveforms of the proposed system. With respect to voltage across PCC ($V_{pcc}$), the source current ($i_s$), load current ($i_L$), and compensating current($i_C$) are shown to be highly distorted.




(a) (b) (c)

**Fig 4.11 (a-c)** Steady-state simulated waveforms of $v_s$ w.r.t $i_s$, $i_L$, $i_C$ ) with LMS algorithm

Before compensation, the supply feeds a non-linear load with THD of 29.6%, as shown in Fig 4.12(b). Hence the THD of the supply current is the same as that of the load current. After compensation, the source current THD is reduced to 3.1% (at $i_S$= 4.269A RMS), as depicted in Fig 4.12(a). The THD of the source voltage is 1.9% in undistorted conditions, as given in Fig 4.12(c). The proposed controller quickly estimates the fundamental weight, which settles down after the convergence.

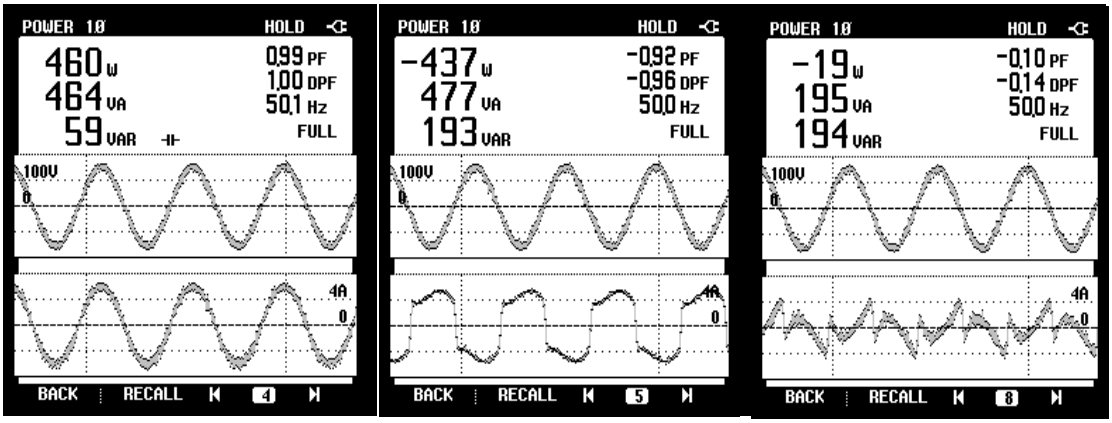



(a) (b) (c)

**Fig 4.12 (a-c)** Steady state THD analysis of $i_s$,$i_L$,$V_s$ ) with LMS algorithm

It is depicted in Fig 4.13(a-c) that the load demand an active power of 0.437kW and reactive power of 0.193kVAR.The active supply power is 0.460kW, which satisfies not only the load demand but also meets the switching losses of CHB-MLI.

The compensator supplies 0.194KVAR of the load-required reactive power, as desired by the controller. The desired power flow is maintained between the source, load, and compensator, and it is observed the source current is sinusoidal and ideally in phase with the supply voltage.




(a) (b) (c)

**Fig 4.13 (a-c)** Steady-state active and reactive power in source, load, and compensator side with LMS algorithm

Fig 4.14(a-b) shows the dynamic results of $v_s$, $i_L$, $i_s$, $V_{dc}$ under dynamic load conditions. It is observed from the waveforms that the proposed algorithm can extract the fundamental active component of load current within (3~4 cycles) and make the source current sinusoidal as well as in phase with the supply voltage. In addition, PI controller quickly stabilizes the dc link voltage to its reference value of 200V, which shows the LMS control algorithms works satisfactorily under varying load condition.

Fig 4.14 (c-d) shows the waveforms of $i_S$, $V_{dc1}$, $V_{dc2}$, and $V_{dc}$. It is seen that during load variation, both the dc link voltages are self-balancing. They quickly stabilize their dc voltages to 100V each within a few cycles and total dc link voltages to 200V within very few oscillations.

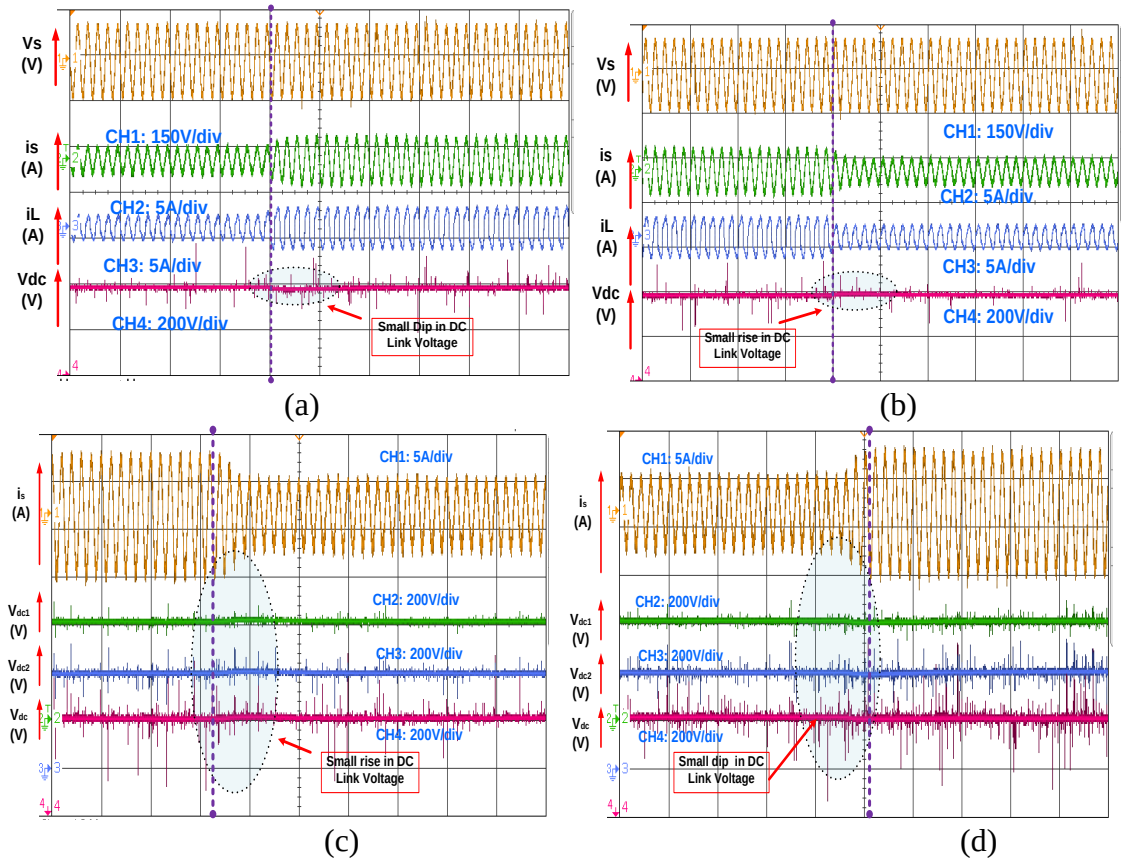



**Fig 4.14** Experimental Waveforms (a,b) $V_s$,$i_s$,$i_L$,$V_{dc}$ (c,d) $i_S$, $i_L$,$V_{dc1}$, $V_{dc2}$, $w_p$, and error under dynamic load variations

Fig 4.15 shows the intermediate results, such as estimated weights ($W_P$) concerning load current variation. It is concluded that the estimated fundamental active component is also varying on varying the load. However, the steady-state value converges quickly to nw values. These results depict the satisfactory working of the LMS algorithm.

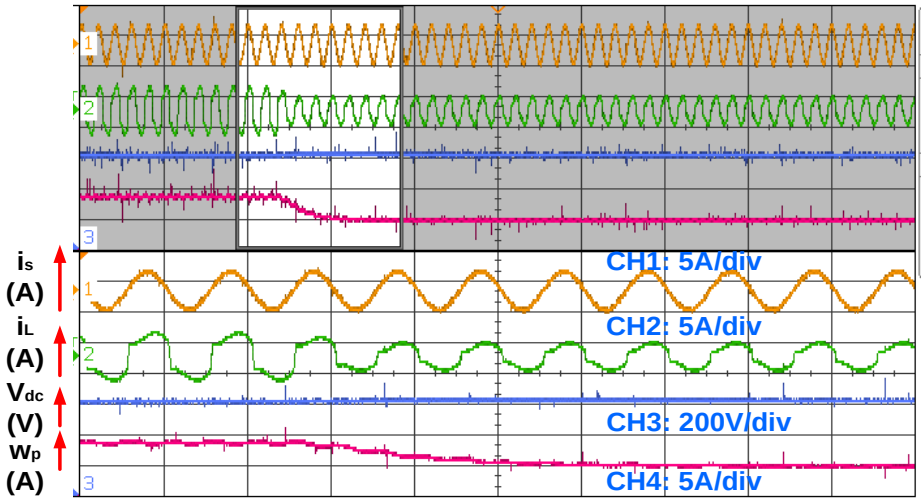



**Fig 4.15** Experimental waveforms of is, $i_L$, $V_{dc}$, and $w_p$ under dynamic load variations

## 4.9 Extraction of fundamental component of load current using Synchronous Reference Frame Theory (SRFT)

The block diagram of the SRFT control algorithm is shown in Fig 4.16. To formulate the SRFT algorithm, an imaginary vector is to be created, providing a delay $\pi/2$ in the input voltage signal. In recent years, Parks transformation-based control techniques have been frequently used to extract the fundamental load current. The primary benefit of the d-q reference frame is its simplicity in an application for controlling the algorithms of the shunt active power filter that calculate the fundamental active, reactive, and harmonic components. Similarly, IRPT (Instantaneous Reactive Power Theory), widely known as p-q theory, is extensively used by researchers and industries for shunt compensation. Recently this concept of the p-q theory has been applied to a single-phase system. In which an imaginary variable shifted by $90^o$ orthogonally, and a replica of voltage/current is utilized as required in p-q and d-q theory. The utility of Park's transformation can be applied to a single-phase system. The transformation of load current into α,β frame is represented as

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_L(\omega t + \phi) \\ i_L(\omega t + \frac{\pi}{2} + \phi) \end{bmatrix} \tag{4.28}$$

Using the relationship of transforming α,β to d-q quantities gives

$$\begin{bmatrix} i_{Ld} \\ i_{Ld} \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{4.29}$$

The transformer d,q component of the load is composed of DC and ac (harmonics) components are represented as

$$i_{Ld} = \bar{i}_{Ld} + \tilde{i}_{Ld} = i_{L\alpha}\sin\omega t - i_{L\beta}\cos\omega t \tag{4.30}$$

$$i_{Lq} = \bar{i}_{Lq} + \tilde{i}_{Lq} = i_{L\alpha}\cos\omega t + i_{L\beta}\sin\omega t \tag{4.31}$$

Using LPF (low pass filter), ac components can easily filter out. In addition, the reference current is generated using the DC magnitude of the load current, so this theory's indirect control technique is considered.

Now, to generate the reference source current, the α,β is generated using inverse transformations, represented as

$$\begin{bmatrix} i^*_{S\alpha} \\ i^*_{S\beta} \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}^{-1} \begin{bmatrix} i^*_{Ld} \\ i_{L\beta} \end{bmatrix} \tag{4.32}$$

$$\begin{bmatrix} i^*_{S\alpha} \\ i^*_{S\beta} \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}^{-1} \begin{bmatrix} i^*_{Ld} + i_{DC} \\ i_{L\beta} \end{bmatrix} \tag{4.33}$$

Here, $i_{DC}$ is the current needed to maintain the dc link voltage constant. Further, the sinusoidal reference current is calculated as

$$i^*_S(\omega t) = \sin\omega t\,(\bar{i}_{Ld} + i_{DC}) \tag{4.45}$$

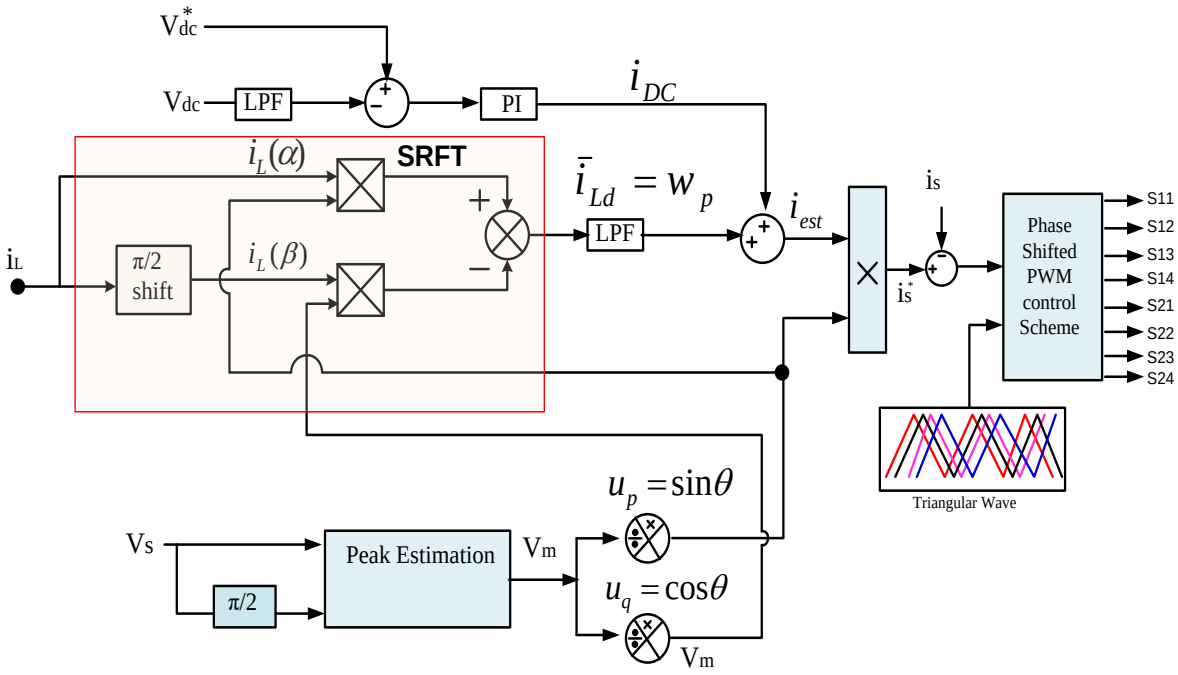



**Fig 4.16** Block diagram of the SRFT control algorithm

### 4.9.1 Simulation Results with SRFT Algorithm

Fig 4.17 shows the simulated waveforms of PCC voltage ($V_{pcc}$), source current ($i_s$), load current ($i_L$), compensating current ($i_c$), inverter output voltage ($V_{inv}$), total dc link voltage ($V_{dc}$). At t=0.4s, the load is increased till t=0.6s. As seen in Fig 4.17, the load current has increased from 3A to 6A (at t=0.4s) and decreased to 3A (at t=0.6s). Similarly, the source varies as the load is increased or decreased. It is seen that the dc link voltage quickly self-regulates to a reference value of 200V.

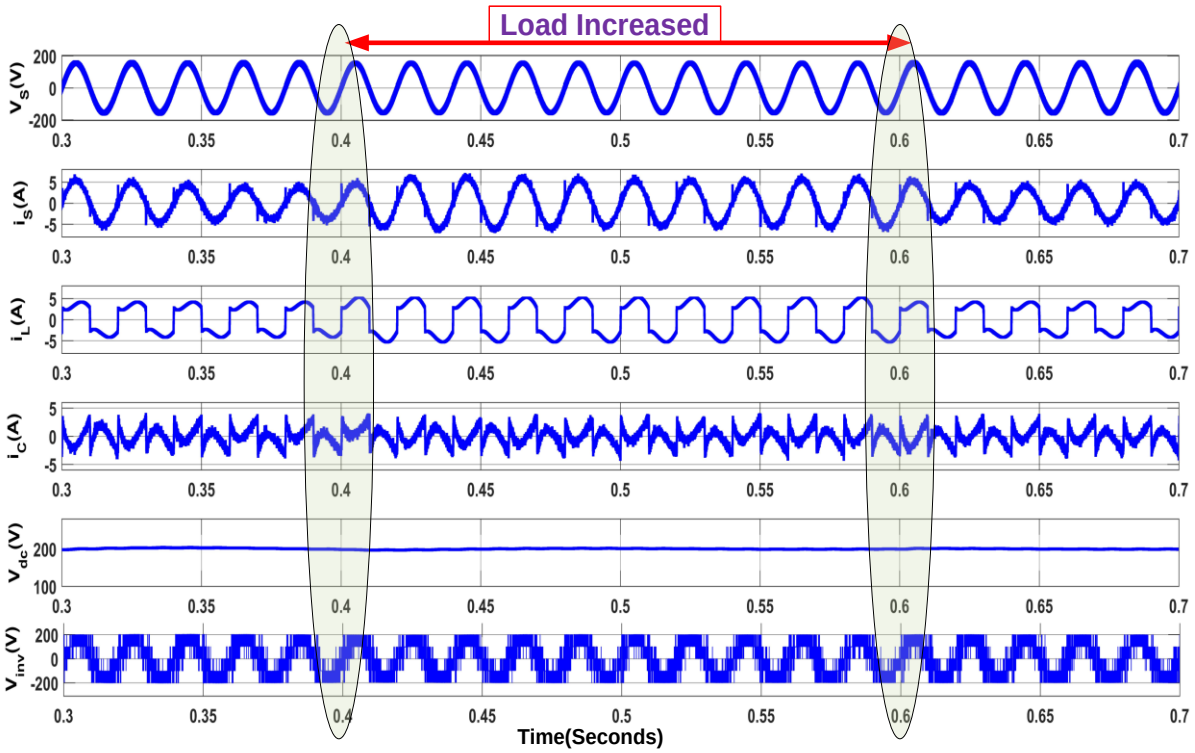
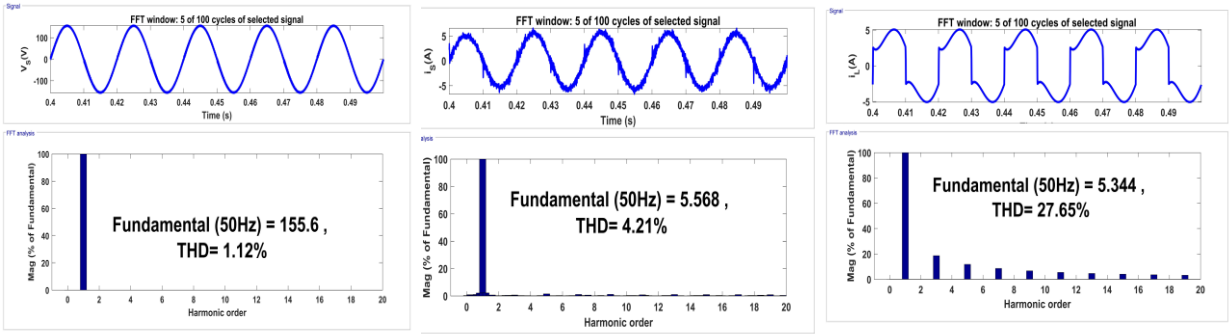



**Fig 4.17** Simulated waveforms of $v_{s.}$, $i_s$, $i_L$, $i_C$, $V_{dc,}$ and $V_{inv}$ during load variation at t=0.4s and t=0.6s with SRFT

Fig 4.18(a-c) shows the harmonic spectra of source current load current and source voltage. Before compensation, the source feeds the non-linear load and has a THD of 27.65%, similar to the load current, as shown in Fig 4.18(c). However, after compensation using SAPF, the THD of source current reduces drastically to 4.21%. The compensator regulates the dc link voltage via the PI controller and improves the harmonic profile of the source current by injecting compensating current in PCC. This shows adequate compensation using the SRFT algorithm




(a) (b) (c)

**Fig 4.18 (a-c)** Waveforms of $v_{s,}$ $i_S$ and $i_L$ along with THD analysis with SRFT algorithm

Fig 4.19 shows the intermediate results, such as estimated weights ($W_P$) concerning load current variation. It is concluded that the estimated fundamental active component also varies on varying the load. These results depict the satisfactory working of the SRFT algorithm.

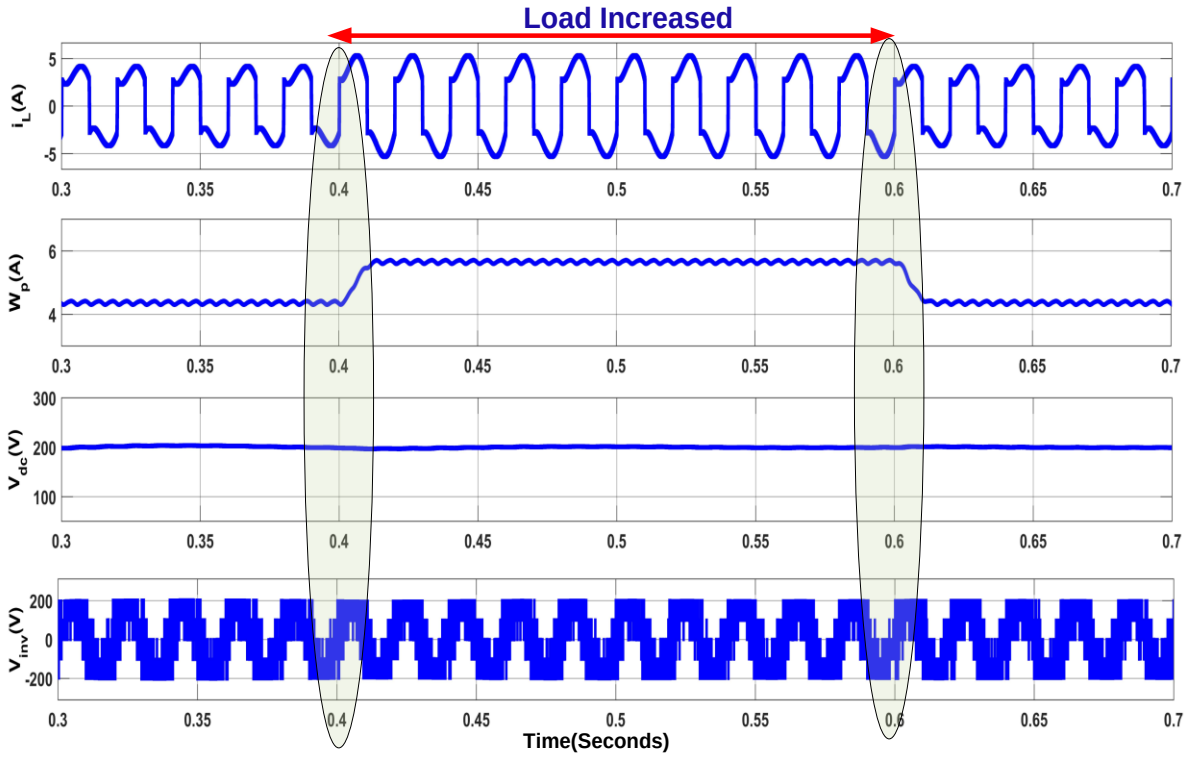
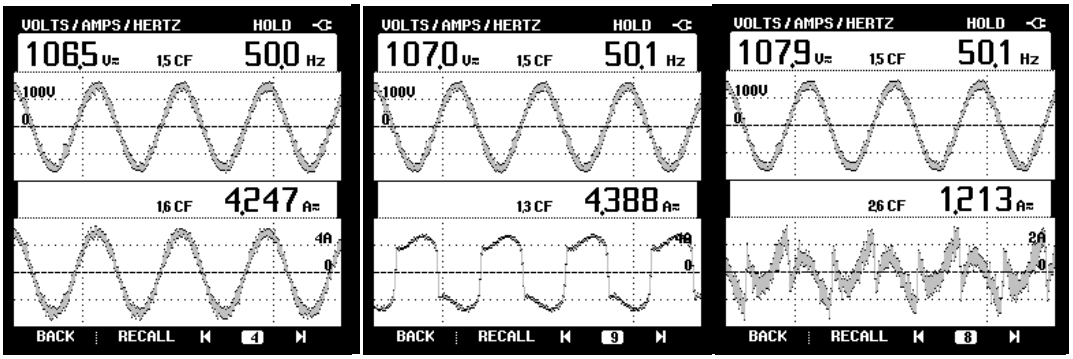



**Fig 4.19** Simulation Results of load current $i_L$(A), $w_p$(A), $i_C$(A) and $V_{dc}$(V) with SRFT

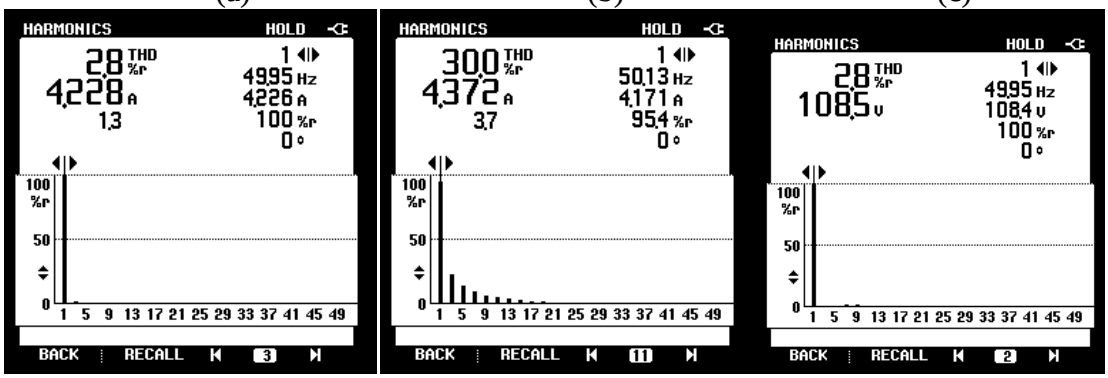
## 4.9.2 Experimental Results with SRFT Control Algorithm

Steady-state experimental results of the proposed system are presented in Fig 4.20(a-e). It depicts the voltage of PCC ($V_{pcc}$), source current ($i_s$), load current ($i_L$), and compensating current ($i_C$). Source current follows load current with a THD of 30% before compensation. The THD of source current is reduced to 2.8% after compensation. The injected SAPF current mitigates the harmonics generated by the non-linear load. The %THD of PCC voltage is 2.8%, as shown in Fig 4.22(e), which is relatively higher than other conventional algorithms.

Furthermore, the supply current is nearly sinusoidal and in phase with the source voltage. The recorded waveforms show that the proposed system works satisfactorily and the obtained %THD of $V_{pcc}$(V) and $i_S$(A) is within stipulated IEEE-519 standards.



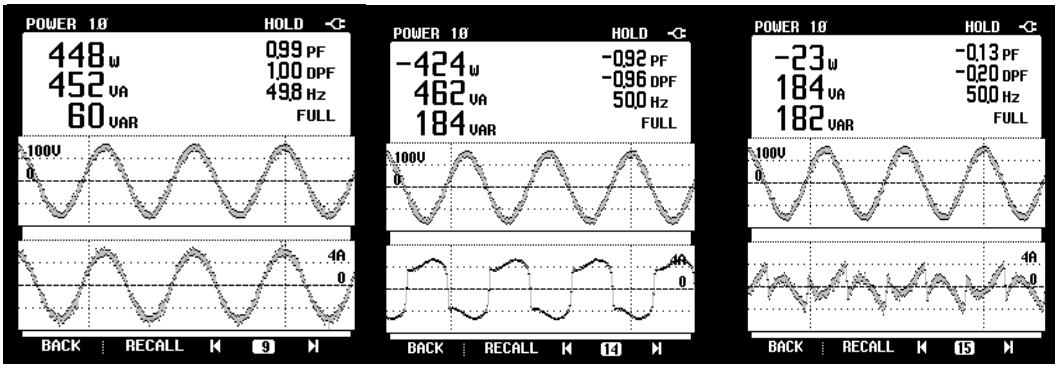

(a) (b) (c)




(d) (e) (f)

**Fig 4.20** Steady-state performance of the system (a) $v_S$ and $i_S$ (b) $v_S$ and $i_L$ (c) $v_S$ and $i_C$ along with harmonic spectrum (d) %THD of $i_S$ (e) %THD of $i_L$ and (f) % THD of $v_S$ using SRFT

The steady-state power requirements in the system are shown in Fig 4.21(a-c). The load has a real and reactive power demand of 424W and 184VAR, and the SAPF meets the reactive power demand of the load by feeding 182VAR. The grid supplies 448 W to meet the load active power and switching losses.




(a) (b) (c)

**Fig 4.21 (a-c)** Waveforms of active and reactive power flow in the system using SRFT

The performance of the proposed system under dynamic load conditions is shown in Fig 4.22(a-d). The waveforms of PCC voltage ($V_{pcc}$), source current ($i_S$), load current

($i_L$), and total DC link voltage ($V_{DC}$) are depicted. As shown in Fig 4.22(a), a sudden change in load increases the load current, and the fast action of the PI controller regulates the total DC link voltage quickly to the reference value of 200V ± 2V. Similarly, the system performance under a decrease in load is depicted in Fig 4.22(b).

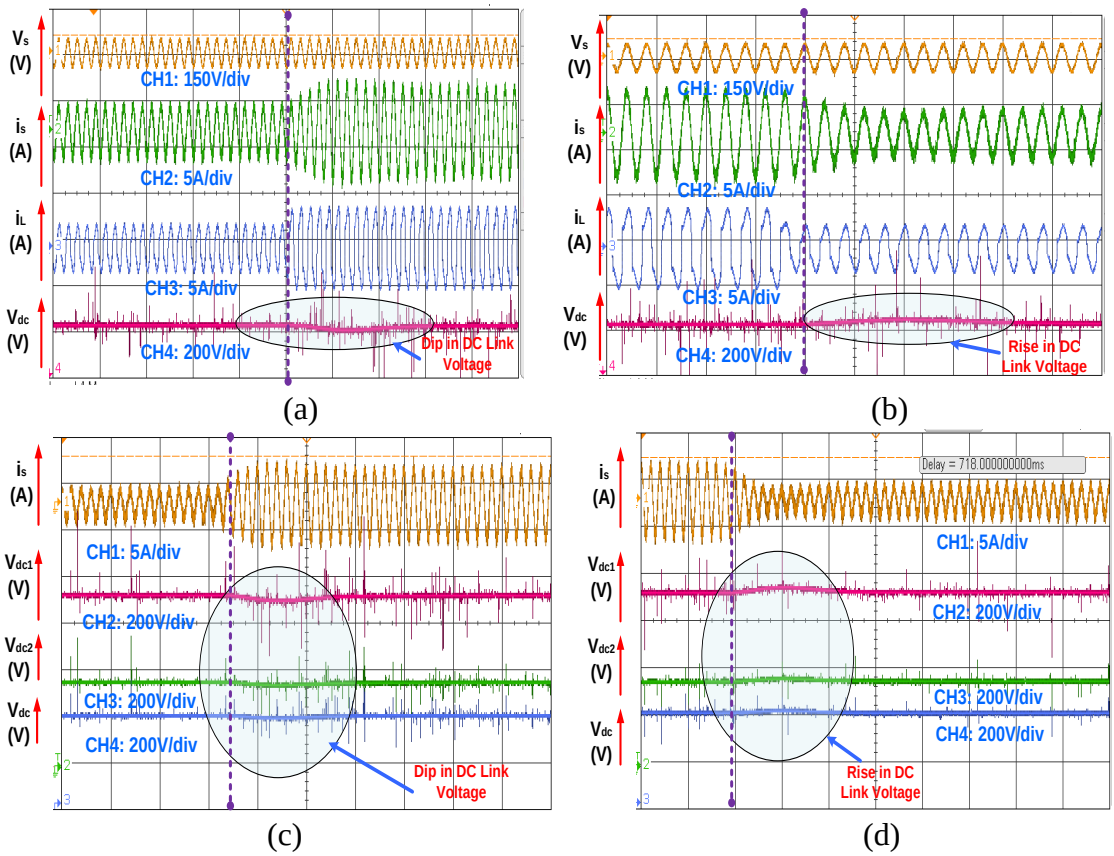



**Fig. 4.22 (a-d)** Dynamic performances with SRFT algorithm

Similarly, Fig 4.24(c-d) depicts the performance of DC link voltages across both capacitors under varying loads. It is clearly observed that the DC link voltage quickly restored to the base value of 100V each within a few cycles after load variations.

The intermediate results of the system are shown in Fig 4.23 under sudden decrement in load. Fig 4.23 shows the source current ($i_S$), load current ($i_L$), estimated eight ($w_{eff}$), and total DC link voltage ($V_{DC}$) on the oscilloscope.. The tuned PI controller on the DC link voltage easily restores the voltage to the 200V reference value. This result depicts the satisfactory performance of the SRFT algorithm. The SRFT algorithm effectively computes the fundamental estimated component in 3~4 cycles, and all parameters reach a steady state within a few cycles.

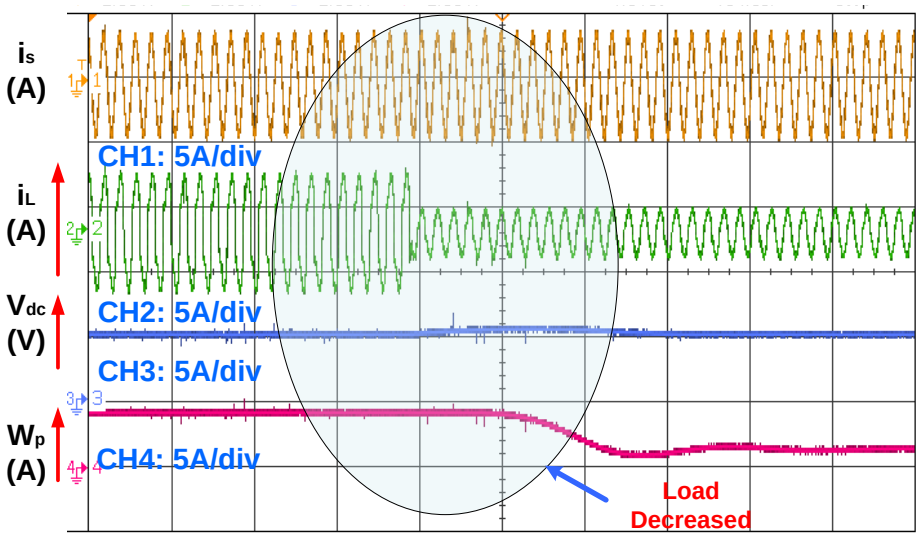



**Fig 4.23** Dynamic behaviour of the proposed system $i_S$(A). $i_L$(A), $V_{DC,}$ and $W_p$ under decrease in load with SRFT algorithm

## 4.10 Introduction to Notch Filter (NF)

The typical block diagram of the Notch filter applied to sense the load current, and its digital implementation is given in Fig 4.24. The transfer function of the NF can be given as

$$T(s,\phi)=\frac{s^2+\theta^2}{s^2+\zeta\,\theta+\theta^2} \tag{4.34}$$

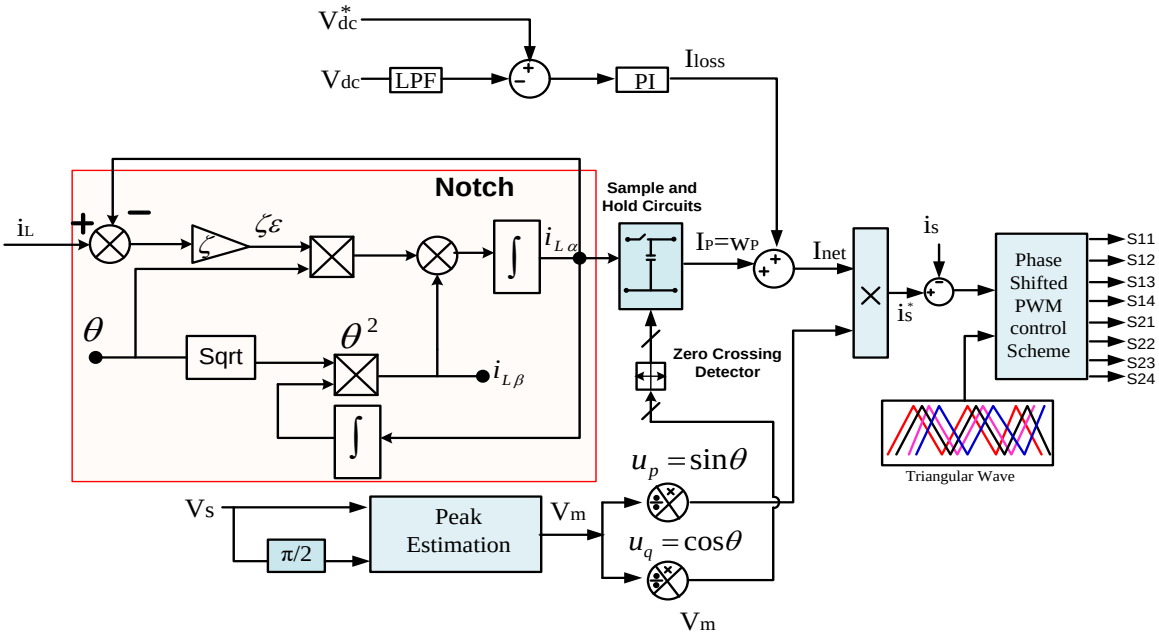



**Fig 4.24** Control algorithms digital implementation in dSPACE-1104 processor with Notch filter

This filter has two parameters $\zeta$ = damping constant and $\theta$ = phase angle. In NF, the mechanism is to control the $\zeta$ , and in this system, the frequency is assumed to be constant. Moreover, the Notch filter computational burden is reduced due to constant frequency. Basically, a Notch filter uses two integrators to extract the fundamental component from the input signal. Bandwidth and settling time is varied by changing the damping constant $\zeta$ . The effect of the variation $\zeta$ is shown in the Bode plot in Fig 4.25

There is a trade-off in choosing the value $\zeta$ . As bandwidth increases, the settling time decreases or vice-versa. The Notch filter is not designed to estimate the frequency but the frequency response curve depends upon $\zeta$ . As a result, phase error varies. Therefore, the value $\zeta$ is judiciously selected so that the phase is set to a minimum of 2.5 degrees. In this paper, $\zeta$ =0.5 is taken, as it is found to give a satisfactory performance under transient and steady-state conditions.

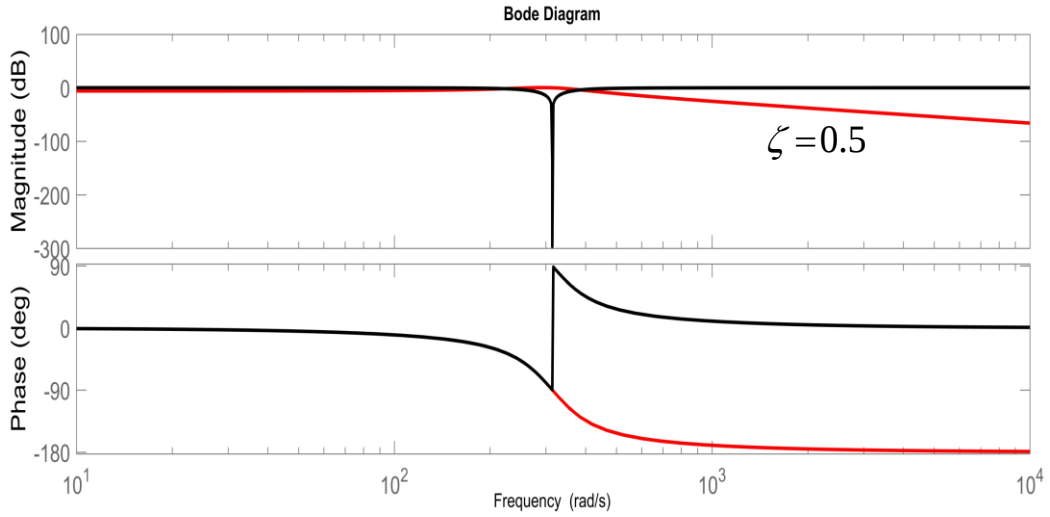



**Fig 4.25** Bode diagram of Adaptive Notch Filter

Before generating reference current, the switching loss requirement of CHB-MLI must be estimated and provided by the grid. The actual dc voltage is compared with the reference dc voltage to generate the error ($e_{dc}$). It is further processed to the PI controller to meet active loss component ($I_{loss}$) and also regulate the dc link voltage to set value, given by

$$e_{dc} = V_{dc} - V_{dc}^{*} \tag{4.35}$$

$$I_{loss}(n) = I_{loss}(n-1) + k_p\,(e_{dc}(n) - e_{dc}(n-1)) + k_i\, e_{dc}(n) \tag{4.36}$$

In Equation 4.36, the integral and proportional gain of the PI controller is represented by $k_i$ and $k_p$. Now finally reference current is estimated $i_s$*, which is governed by multiplying the active component ($I_{net}$) with the in-phase unit vector template given by

$$i_s^* = I_{net} \sin\phi \tag{4.37}$$

The proposed system also implemented a sample & hold circuit(S and H) and zero current detector circuit (ZCD), the extracted fundamental load current is fed to S and H circuit, and it is synchronized with the ZCD when the unit synchronizing template crosses the zero then ZCD generated the triggering the signal which is further fed to S and H circuit. The S and H logic circuits capture the samples of the sensed load current once receiving the signal from the ZCD circuit. As a result, an accurate and fast estimation of the signal is achieved.

### 4.10.1 Simulation Results with Notch Filter

Fig 4.26 shows the simulated waveforms of PCC voltage ($V_{pcc}$), source current ($i_s$), load current ($i_L$), compensating current ($i_c$), inverter output voltage ($V_{inv}$), total dc link voltage ($V_{dc}$). At t=0.4s, the load is increased till t=0.6s. As seen in Fig 4.26, the load current has increased from 3A to 6A (at t=0.4s) and decreased to 3A (at t=0.6s). Similarly, source current varies as the load is increased or decreased. It is seen that the dc link voltage quickly self-regulates to a reference value of 200V.

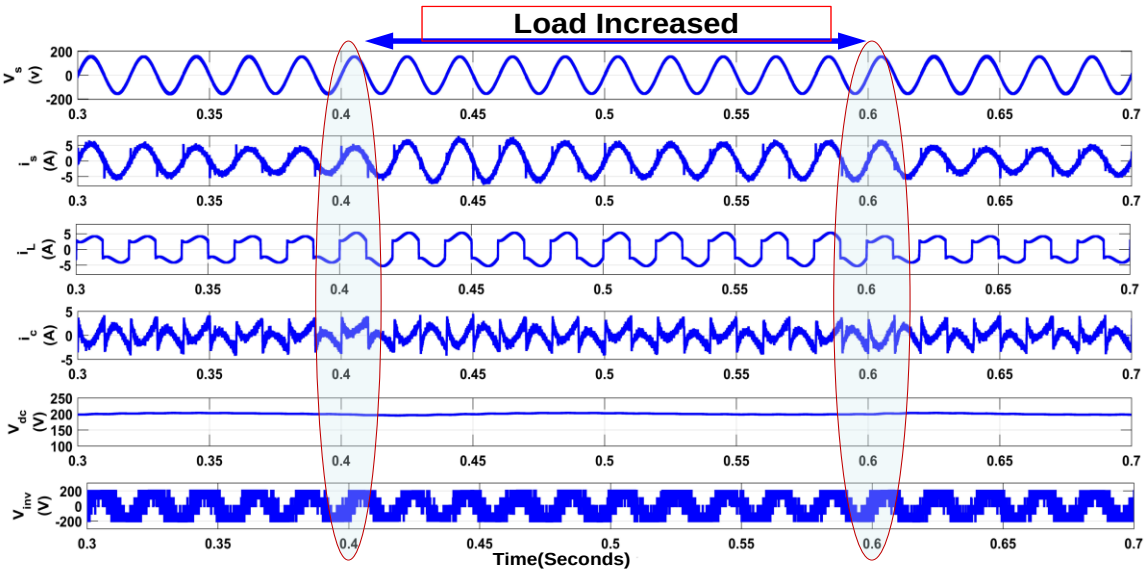
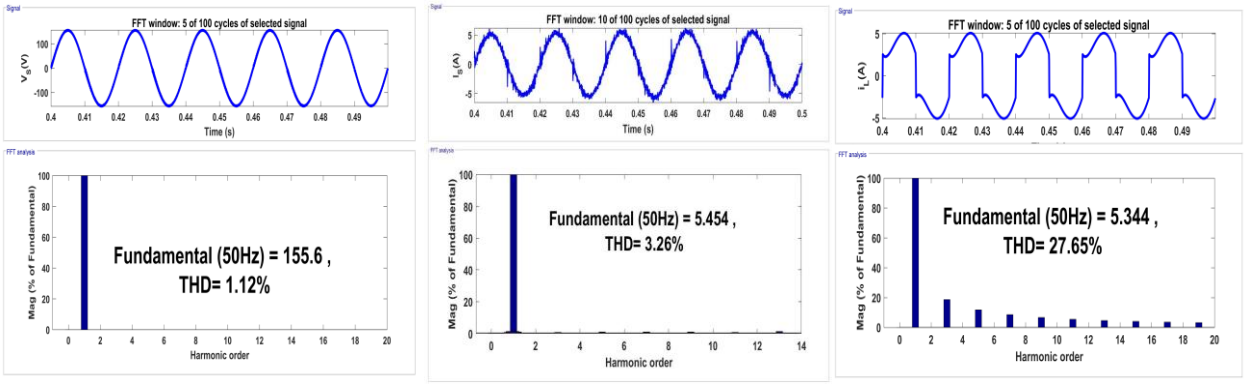



**Fig 4.26** Simulated waveforms of $v_s$, $i_s$, $i_L$, $i_C$, $V_{dc}$ and $V_{inv}$ during load variation at t=0.4s and t=0.6s with Notch Filter

Fig 4.27(a-c) shows the harmonic spectra of source current load current and source voltage. Before compensation, the source feeds the non-linear load and has a THD of 27.65%, similar to the load current, as shown in Fig 4.27(c). However, after compensation using SAPF, the THD of source current reduces drastically to 3.26%. The compensator regulates the dc link voltage via the PI controller and improves the harmonic profile of the source current by injecting compensating current in PCC.




(a) (b) (c)

**Fig 4.27 (a-c)** Waveforms of $v_s$ $i_S$ and $i_L$ along with THD analysis with Notch Filter

Fig 4.28 shows the intermediate results, such as estimated weights ($W_P$) with respect to variation of load current. It is concluded that the estimated fundamental active component varies on varying the load, but it converges soon with 1~2 cycles with a Notch filter. These results depict the satisfactory working of the Notch filter.

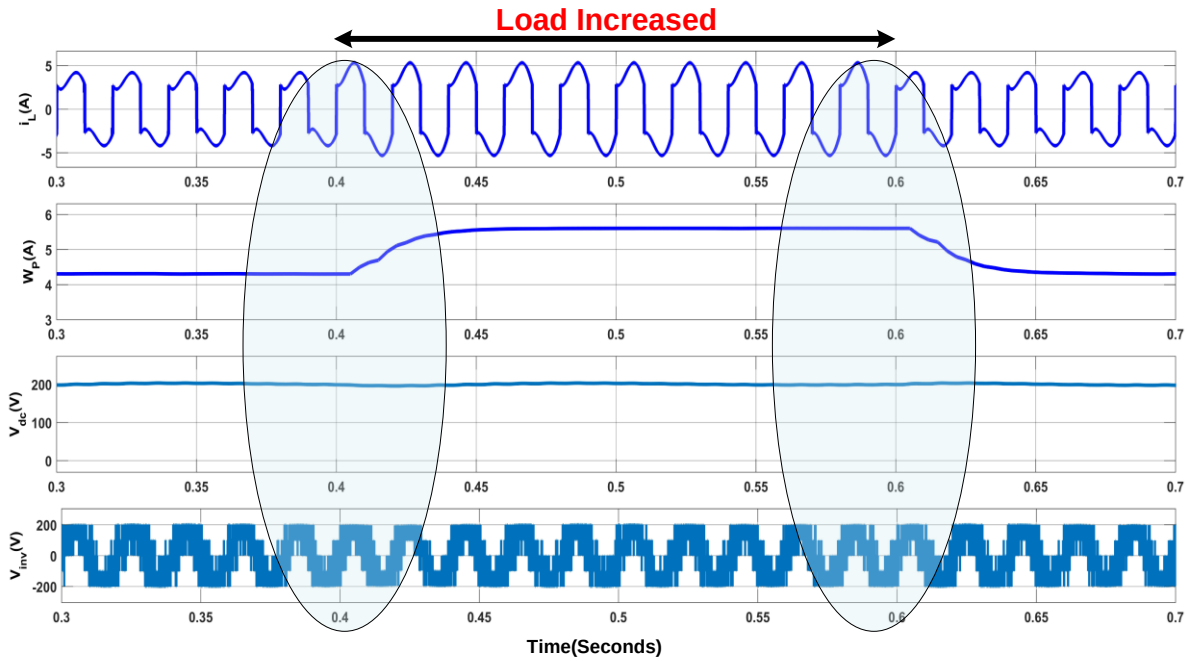
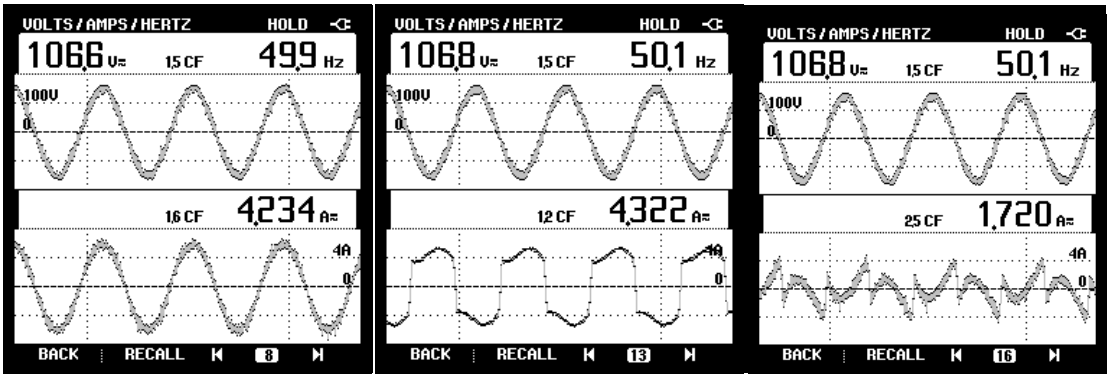



**Fig 4.28** Simulation Results of load current $i_L$(A), $W_p$(A), $V_{dc}$(V) and $V_{inv}$ (V) with Notch Filter

## 4.10.2 Experimental Results with Notch Filter

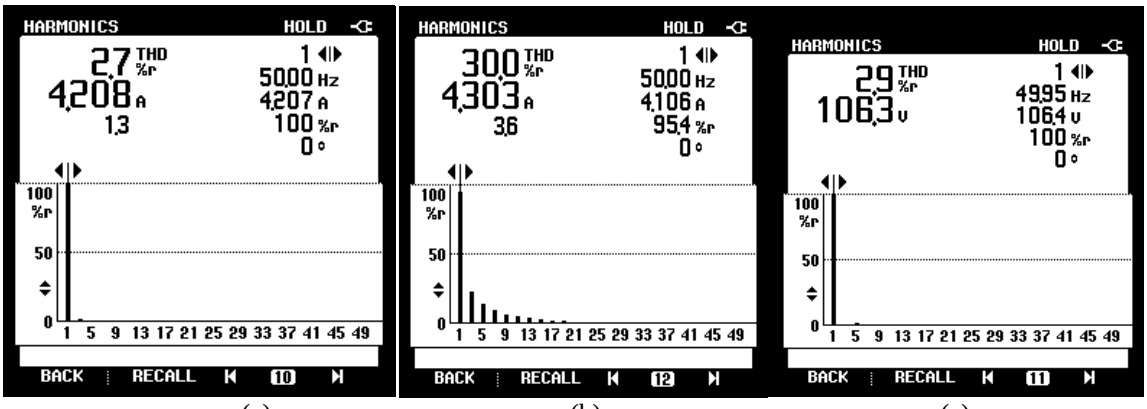
Fig 4.29(a-c) depicts the steady-state waveforms of the proposed system. Concerning voltage across PCC ($V_{pcc}$), the source current ($i_s$), load current ($i_L$), and compensating current($i_C$) is shown




(a) (b) (c)

**Fig 4.29 (a-c)** Steady-state simulated waveforms of $v_s$ w.r.t $i_s$, $i_L$, $i_C$ with Notch filter

Before compensation, the source current feeds a non-linear load with a THD of 30%, as shown in Fig 4.30(b). After compensation, the source current THD is reduced to 2.7% (at $i_S$= 4.208A RMS), as depicted in Fig 4.30(a). The source voltage THD is 2.9% in undistorted conditions, as given in Fig 4.30(c). The proposed controller quickly estimates the fundamental weights and settles the convergence within 1~2 cycles.



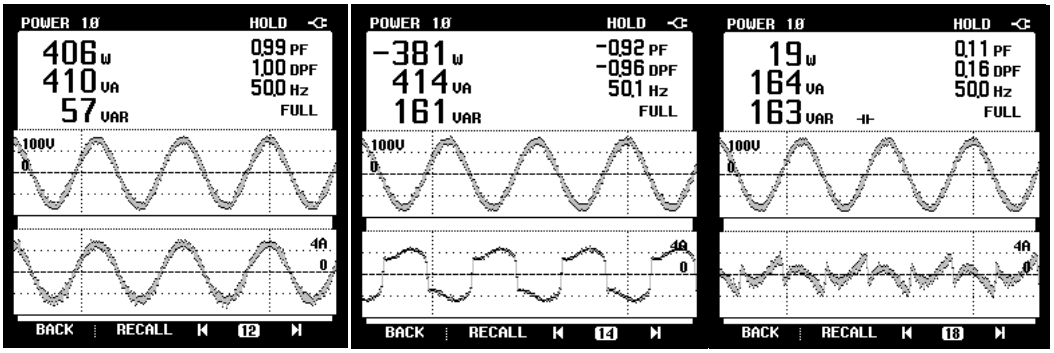

(a) (b) (c)

**Fig 4.30 (a-c)** Steady-state THD analysis of $i_s$, $i_L$, $V_s$ with Notch filter

It is depicted in Fig 4.31(a-c) that loads demand an active power of 0.381kW and reactive power of 0.161kVAR.The active supply power is 0.406kW, which satisfies not only the load demand but also meets the switching losses of CHB-MLI.

The compensator supplies 0.163KVAR of the load-required reactive power, as desired by the controller. The desired power flow is maintained between the source, load,

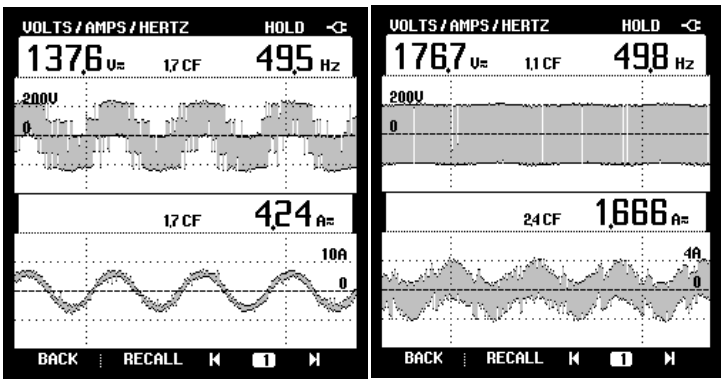
and compensator, and it is observed the source current is sinusoidal and ideally in phase with the supply voltage.




(a) (b) (c)

**Fig 4.31 (a-c)** Steady-state active and reactive power in source, load, and compensator side with Notch filter

Fig 4.32(a-b) shows the steady-state output voltage waveforms of 2-level and 5-level inverters. MLI possesses low switching losses; reduced harmonic is injected at PCC and can synthesize suitable output voltage. The five-level inverter voltage is clearly visible and has lower harmonic content than the two-level inverter.




(a) (b)

**Fig 4.32(a,b)** shows the output voltage waveform of 5-level MLI w.r.t $i_s$ and output voltage of 2-level inverter w.r.t $i_c$ with Notch filter

The performance of the proposed system under dynamic load conditions is shown in Fig 4.33(a-b). The waveforms of PCC voltage ($V_{pcc}$), source current ($i_S$), load current ($i_L$), and total DC link voltage ($V_{DC}$) are shown. As shown in Fig 4.33 (a), a sudden change in load increases the load current, and the fast action of the PI controller regulates the total DC link voltage quickly to the reference value of 200V ± 2V. Similarly, the system's performance under a decrease in load is depicted in Fig 4.33(b).

Fig 4.33 (c-d) shows the waveforms of $i_L$, $V_{DC1}$, $V_{DC2,}$ and $V_{DC}$ during sudden perturbation in load. It is seen from the waveforms that both DC link voltages of capacitors have reached ~100V within a few cycles. Hence the total DC link voltage remains stable and well-regulated even during dynamic load conditions.

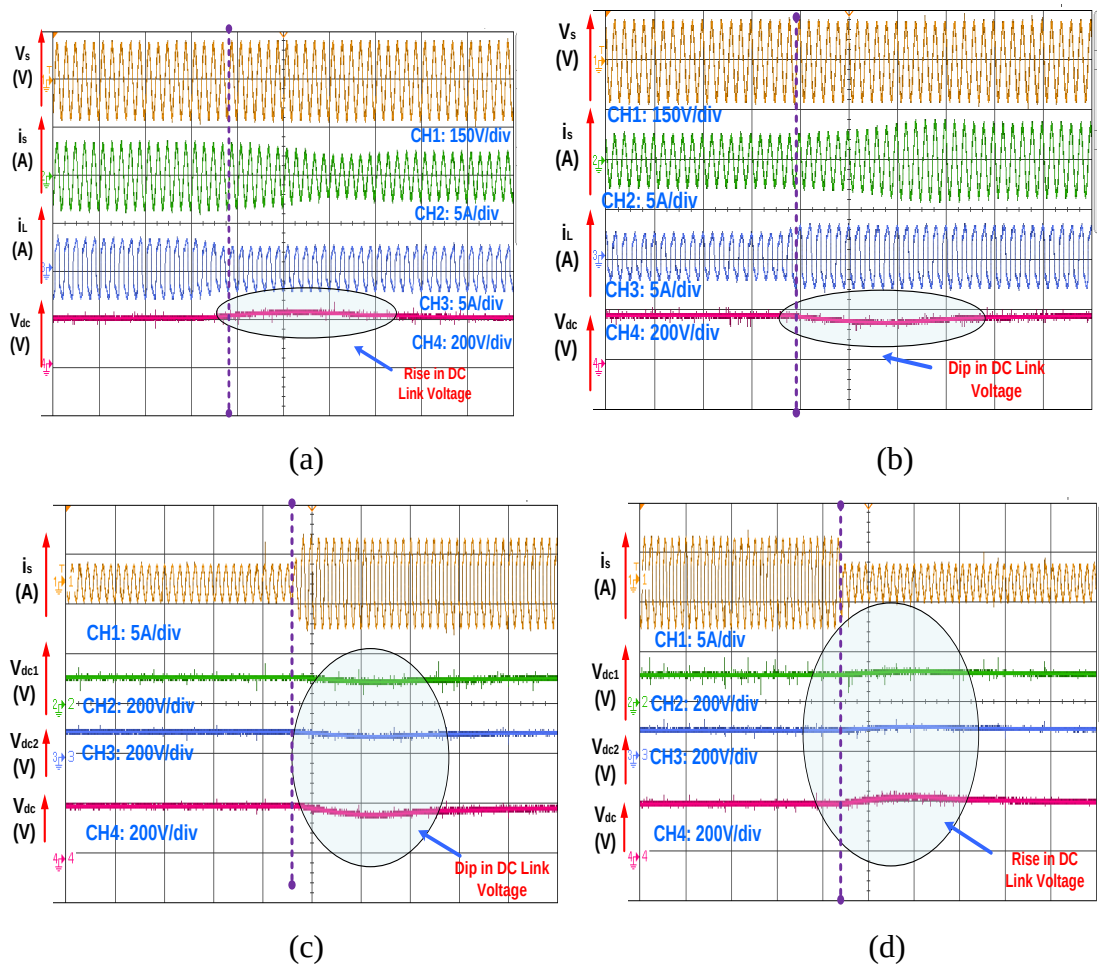



**Fig 4.33** Dynamic behavior of the system with Notch filter

The intermediate results of the system are shown in Fig 4.34 under simultaneous increase and decrease of load. It shows estimated eight ($W_{IP}$), individual DC link voltages across capacitors $V_{dc1}$ & $V_{dc2}$ and total DC link voltage ($V_{DC}$) on an oscilloscope. Fig 4.34 shows that on increasing or decreasing the load, the DC link voltage slightly varies, showing a voltage dip and rise, respectively. The tuned PI controller on the DC link voltage easily restores the voltage to the 200V reference value. This result depicts the satisfactory performance of the Notch algorithm. The Notch algorithm effectively computes the fundamental estimated component, and all parameters reach steady within a few cycles.

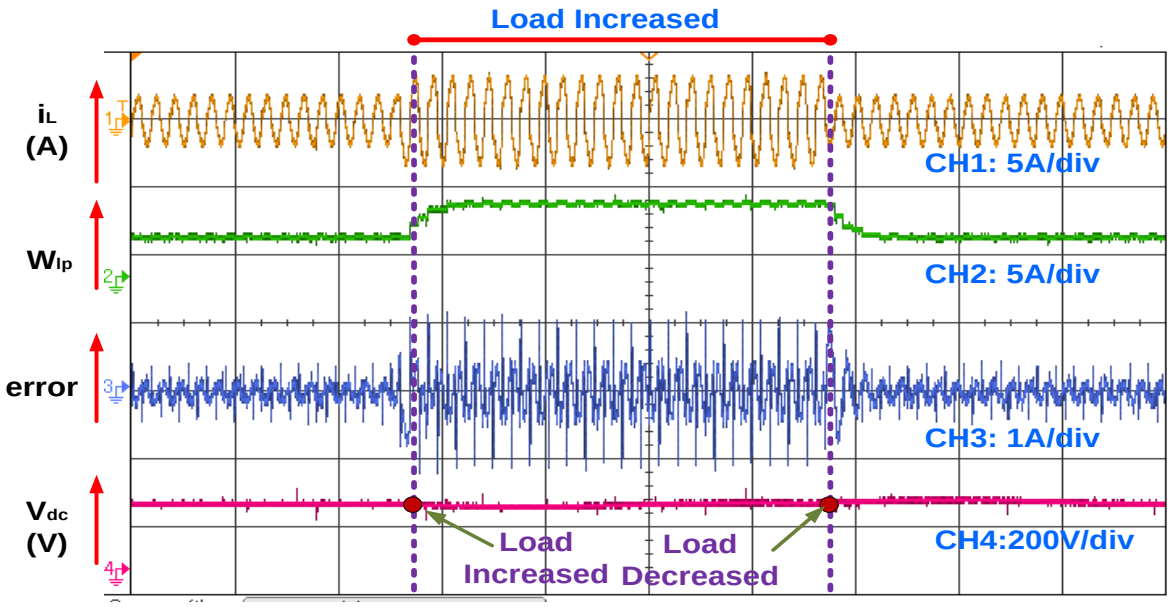



**Fig 4.34** Dynamic behaviour of the Notch filter $i_L$, $w_{lP}$, error(r), and $V_{dc}$ under increase and decrease in load

## 4.11 Comparative Analysis of LMS, SRFT, and Notch Filter Algorithm

The performance of conventional algorithms viz LMS, SRFT, and Notch are presented in this section. The performance is tested by various parameters such as convergence rate, steady state error, dc-link voltage variations, THD analysis of source and load current, harmonic compensation, etc. have been considered in this analysis.

- **Weight Convergence:** Fig 4.35 and Fig 4.36 show the simulation and experimental performance of fundamental estimated active power component convergence analysis for LMS, SRFT, and Notch filter algorithms, respectively. It is observed in Fig 4.37 that the Notch filter achieves weight convergence within 1~2 cycle. However, the convergence achieved by SRFT requires approximately 3~4 cycles; on the other hand, the convergence rate performance of LMS is faster than SRFT but suffers from oscillations. The system is tested under dynamic load change at t=0.4s and t=0.6s.
- **Harmonic spectrum and THD analysis:** The grid current distortion in LMS is found to be 3.92%, 4.21% with SRFT, and 3.26% with the Notch filter when the load current shows a THD of 26.68%. The detailed conventional adaptive control

algorithms are presented in Table 4.1, and power flow parameters for the proposed controllers are tabulated in Table 4.2.

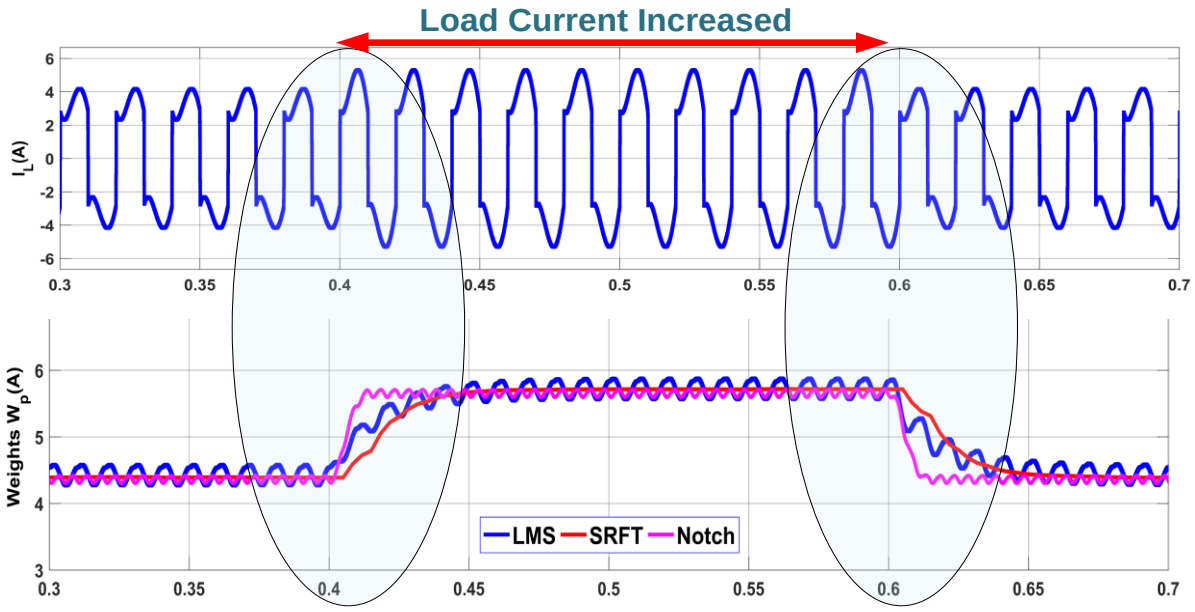



**Fig 4.35** Simulation-based performance comparison of fundamental weights under varying load during t=0.4s to 0.6s with LMS, SRFT, and Notch

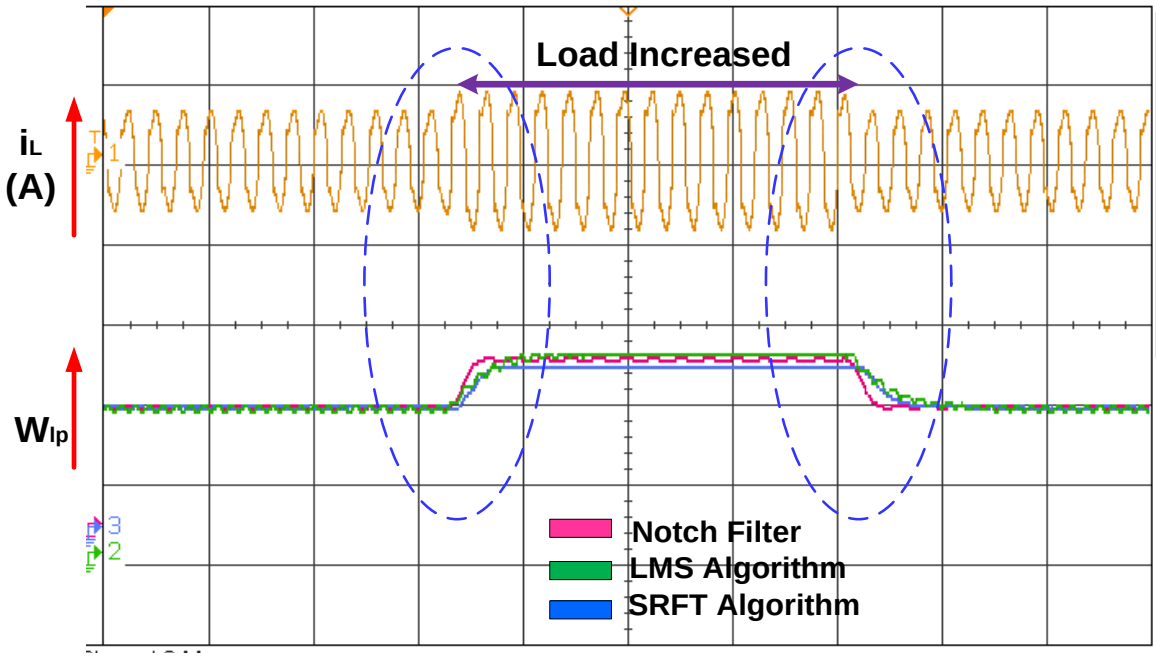



**Fig 4.36** Experimental-based performance comparison of fundamental weights under varying load with LMS, SRFT and Notch

**Table 4.2: Comparison of Adaptive Control Techniques**

| S.No. | Features | | LMS | SRFT | Notch |
|---|---|---|---|---|---|
| 1. | PLL required | | Not required | Required | Not Required |
| 2. | Transformation required | | No | Yes | No |
| 3. | Convergence | | Slower (2~3 cycles) | Slower (3~4 cycles) | **Faster (1~2 cycles)** |
| 4. | Oscillations in fundamental weights | | More | Less | Very less |
| 5. | THD of current (Simulation study) | Supply current | 3.92% | 4.21% | **3.26%** |
| 6. | | Load current | 26.68% | 26.68% | 26.68% |
| 6. | THD of current (Experimental study) | Supply current | 3.1% | 2.8% | **2.7%** |
| 7. | | Load current | 29.6% | 30% | 30% |
| 8. | Error | | Less | Moderate | More |
| 9. | DC link Voltage Oscillations | | 2V | 3-4V | 5-6V |
| 10. | Sampling time | | 50μs | 60μs | 50μs |

**Table 4.3 Power and power factor comparison on control algorithms**

| S.No. | Parameters | LMS | SRFT | Notch |
|---|---|---|---|---|
| 1. | Source Power | Ps=460W<br>Qs=59VAR | Ps=448W<br>Qs=60VAR | Ps=406W<br>Qs=57VAR |
| 2. | Load Power | $P_L$=437W<br>$Q_L$=193VAR | $P_L$=424W<br>$Q_L$=184VAR | $P_L$=381W<br>$Q_L$=161VAR |
| 3. | Compensating Power | $P_c$=19W<br>$Q_c$=194VAR | $P_c$=23W<br>$Q_c$=182VAR | $P_c$=19W<br>$Q_c$=163VAR |
| 4. | Power Factor | 0.99 | 0.99 | 0.99 |

## 4.12 Conclusion

Conventional adaptive control algorithms have been developed for the control of SAPF in this chapter. The algorithms have been designed and implemented to improve several power quality problems at the distribution level. Extensive test results backed with simulation and experimental results have been presented for the designed SAPF. A phase-shifted PWM scheme is designed and implemented for generating the switching pulses for 5-level CHB-MLI. The performance of the algorithms has been compared in terms of convergence speed, harmonics compensation, error minimization, computational complexity, THD, sampling time, and PLL requirement.

Further, the developed Notch Filter controller has been compared with LMS and SRFT-based control algorithms for SAPF. The comparison results for the adaptive controls viz. LMS, SRFT and Notch are tabulated in Table 4.1. Simulation results indicate that the grid current distortion with the Notch filter is found to be least, i.e., 3.26% after compensation, 3.92% with LMS, and 4.21% with the SRFT control algorithm when the load current shows a THD of 26.68%. In experiments also, the THD obtained using the Notch filter is also found to be less, i.e., 2.7% after compensation, 3.1% with LMS, and 2.8% with the SRFT control algorithm. The obtained values of THD of supply currents are observed to be the lowest with the Notch filter among different algorithms considered in simulation and experimentation.

Moreover, all algorithms viz. LMS, SRFT, and Notch filter meet the IEEE-519 standard in a very satisfactory manner. The weight convergence is relatively fast, achieving convergence using the Notch filter within 1~2 cycles. However, SRFT takes 3~4 cycles, and LMS takes 2~3 cycles to converge. In addition, all algorithms quickly stabilize the dc link voltage to the reference value of 200V using the PI controller. All these results show good system response under open and closed-loop conditions and under load variations.

# Chapter 05

# Performance Evaluation of MLI based SAPF using Advanced Adaptive Control Algorithms

## 5.0 Introduction

In the previous chapter, conventional adaptive control algorithms were discussed to control 5-level CHB-MLI on a single-phase grid-connected system. In this chapter, advanced adaptive control algorithms are developed and discussed. The system is first developed and modeled in MATLAB/Simulink, and proposed adaptive control algorithms are tested on a low-cost prototype developed in the laboratory. The detailed analysis of simulation and experimental results have been discussed in this chapter

## 5.1 Single phase Grid connected system for 5-Level SAPF

Fig 5.1 shows the schematic diagram of single-phase 5-level CHB-MLI SAPF connected to single-phase grid AC mains feeding the non-linear load. The SAPF can be controlled by

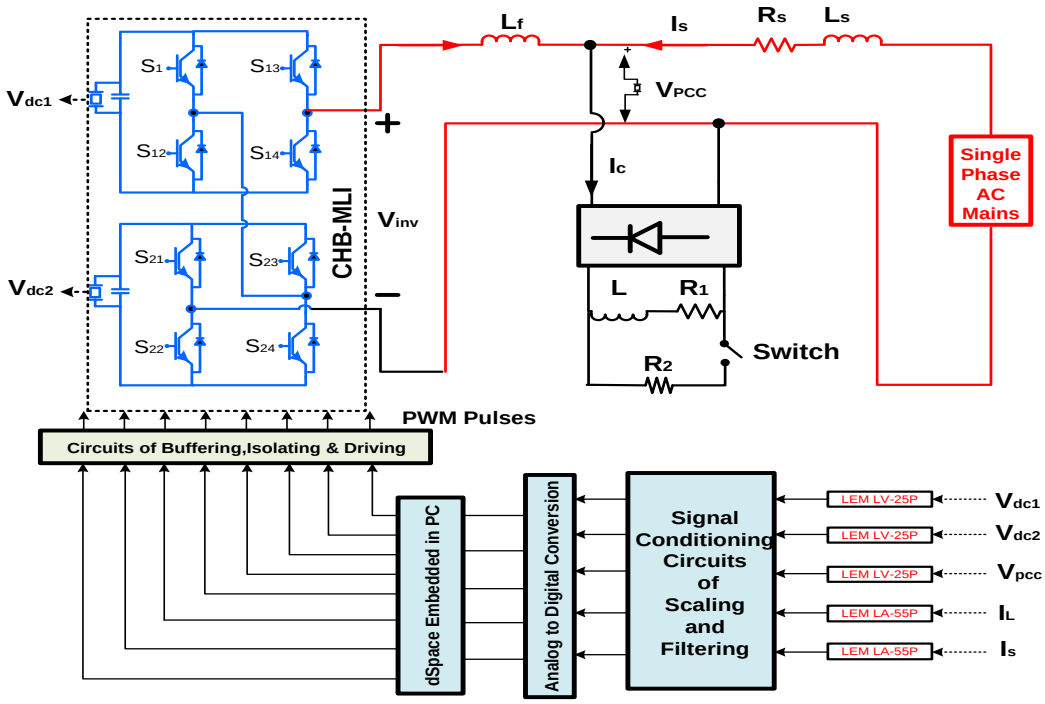



**Fig 5.1** Schematic of the proposed system

sensing the input variables, viz. voltage at the point of common coupling (PCC), load current ($i_L$), source current ($i_s$), and dc bus voltages $V_{dc1}$, $V_{dc2}$. An interfacing inductor ($L_f$) is connected in CHB-MLI to reduce the ripples in ac output. SAPF unit is current-controlled using developed techniques to inject suitable compensating current in phase opposition to eliminate the harmonics generated by the load current. The effective operation of the CHB-MLI can be done by controlling both the dc-link voltages at a constant level, and the conventional PI controller realizes this function. The system is simulated using MATLAB/SIMULINK.

## 5.2 Generalized Structure of Control Algorithm

The generalized control scheme diagram of CHB-MLI is shown in Fig 5.2. In this chapter, the controller is developed using Normalized Least Mean Absolute Third (NLMAT), Normalized Huber (NHuber), and Robust Shrinkage Affine Projection Sign (RSAPS) algorithms based adaptive control algorithm, which updates the weights adaptively from the previous value. The convergence of all algorithms is also analyzed during sudden load transients in a later section of this chapter

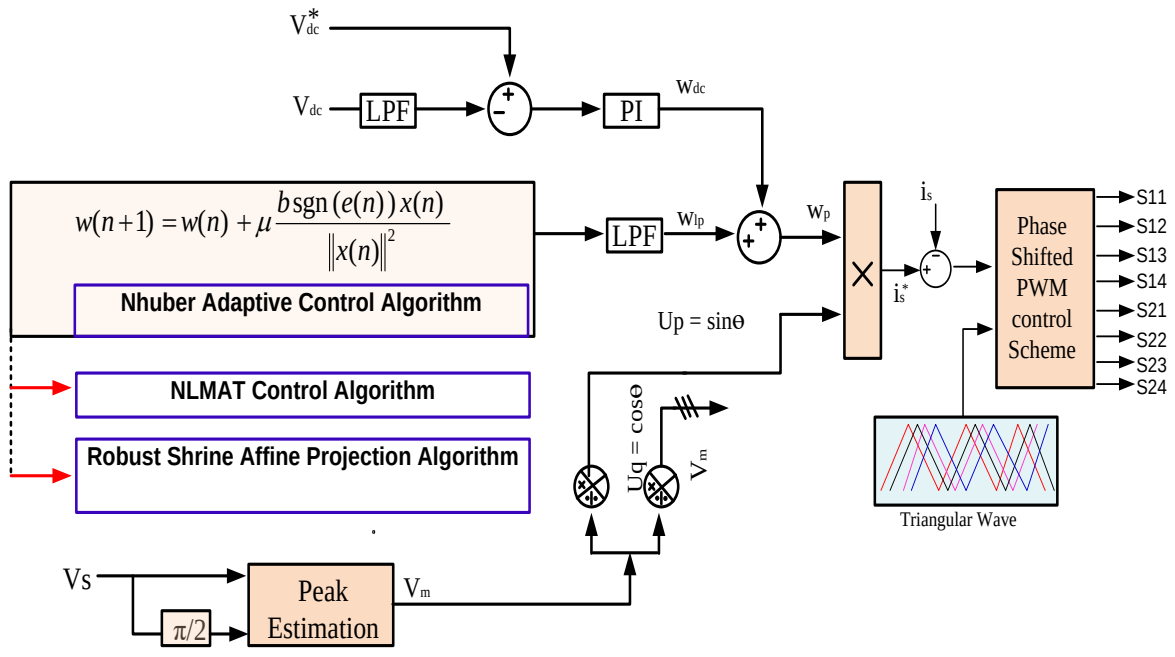



**Fig 5.2** DSP implementation of advanced adaptive control algorithms on CHB-MLI

## 5.3 Extraction of the fundamental component of load current from control algorithms

The fundamental component of load current is extracted from the control algorithms discussed in this section.

### 5.3.1 Non-linear Adaptive Normalized Least Mean Absolute Algorithm Third (NLMAT)

In this section, NLMAT algorithm is used to extract the fundamental component of load current. The DSP implementation of NLMAT algorithm is shown in Fig 5.3. NLMAT is the modification of LMAT algorithm. The LMAT algorithm realizes an optimum function that is minimized. This function, J, is chosen as the third power of absolute error; that is MSE function is defined as

$$J(k)=E\left\{ i_L(k)-\hat{i}_{Lf}(k)\right\}^3=E\left\{e^3(k)\right\} \tag{5.1}$$

$i_L(k)$ is the actual load current and $\hat{i}_{Lf}(k)$ is the estimated load at $k^{th}$ sampling instant. Further the estimated current may be represented as

$$\hat{i}_{Lf}(k)=\sum_{k=0}^{M-1} w_M x(k-M)=w^T x(k) \tag{5.2}$$

where M is the order of filter [Mx1] vector. The filter coefficient is described as $w=\left[w_0(k)\ w_1(k)\ w_2(k)\ .....w_{M-1}(k)\right]$ of order [Mx1] and $x(k)=\left[x(k)\ x(k-1).....x(k-M+1)\right]$is the vector of input parameters. The error can be defined as

$$e(k)=i_L(k)-\hat{i}_{Lf}(k) \tag{5.3}$$

$$e(k)=i_L(k)-w^T x(k) \tag{5.4}$$

Similar to conventional LMS and NLMS algorithms, the objective is to minimize the MSE. This can be achieved using the Steepest descent algorithm, and the weight is updated

until the optimum value is reached. The weights are iteratively determined till minimum MSE is achieved using the weight updating rule given below.

$$w(k+1)=w(k)-\frac{\mu}{3}\nabla_{w(n)}\,e(k) \tag{5.5}$$

where the gradient of $\nabla_{w(k)}\left|e(n)\right|^3$ w.r.t to $w(k)$ is represented as

$$\nabla_{w(k)}(k)=-3e^2(k)\,sign[\,e(k)\,]\,x(k) \tag{5.6}$$

Using Equation 5.5 and Equation 5.6, the weight updating rule of NLMAT is expressed as

$$w(k+1)=w(k)+\mu\,e^2(k)\,sign[e(k)]\,x(k) \tag{5.7}$$

where μ is the step size, and its value should be chosen such that the weights converge quickly under sudden load variations, sign[x] is a function of variable x, for x≥0, then sign[x]=1; otherwise, sign[x]=0. The performance NLMAT algorithm is satisfactory, but its convergence depends on the variations in load current or input supply. To mitigate the drawbacks of NLMAT, the NLMAT algorithm can be developed further by minimizing the following equation.

$$\min_{(n+1)}\left\{\frac{1}{3}\left|d(k)-w^T(k+1)\,x(k)\right|^3+\frac{1}{2}\left\|x(k)\right\|^2\left\|w(k+1)-w(k)\right\|^2\right\} \tag{5.8}$$

where $\|\bullet\|$ is the Euclidean norm of a vector. Taking the derivative of Equation 5.8 w.r.t to $w(k+1)$ and equating to zero gives the new weight-updating equation

$$-e^2(k)\,sign[e(k)]x(k)+\left\|x(k)\right\|^2[w(k+1)-w(k)]=0 \tag{5.9}$$

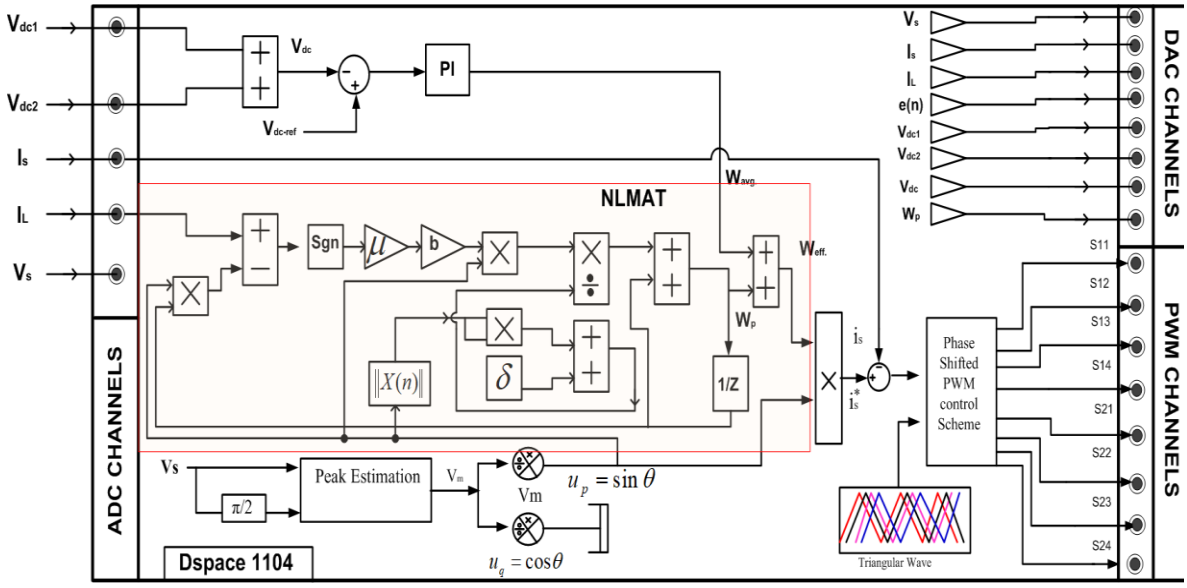



**Fig 5.3** DSP implementation of NLMAT control algorithm using dSPACE-1104

Thus, the weight-updating equation can be expressed as

$$w(k+1)=w(k)+\frac{e^2(k)\,sign[e(k)]}{x^T(k)\,x(k)}x(k) \tag{5.10}$$

In Equation 5.10, a very small parameter $\xi$ is added in the denominator to prevent numerical instability in the case $x^T(k)x(k)$ it is very small and approaches zero. Thus, the final weight updating equation is represented as

$$w(k+1)=w(k)+\frac{e^2(k)\,sign[e(k)]}{\xi+x^T(k)\,x(k)}x(k) \tag{5.11}$$

### 5.3.1.1 Simulation Results with NLMAT Algorithm

The proposed system is designed in MATLAB/Simulink and tested under varying load conditions using MATLAB/Simulink. A single-phase 110V (ac) supply feeds power to a non-linear load and meets the switching losses. NLMAT algorithm is used to control CHB-MLI. Moreover, the reference current is generated, and compared with PS-PWM to generate firing pulses for IGBTs. The proposed system achieves a unity power factor of supply current and mitigates all the harmonics generated by the non-linear load. Fig 5.4 shows the simulated waveforms of PCC voltage ($v_{pcc}$), source current ($i_s$), load current ($i_L$), compensating current ($i_c$), inverter output voltage ($V_{inv}$), total dc link voltage ($V_{dc}$) under dynamic load conditions at t=0.4s and t=0.6s.

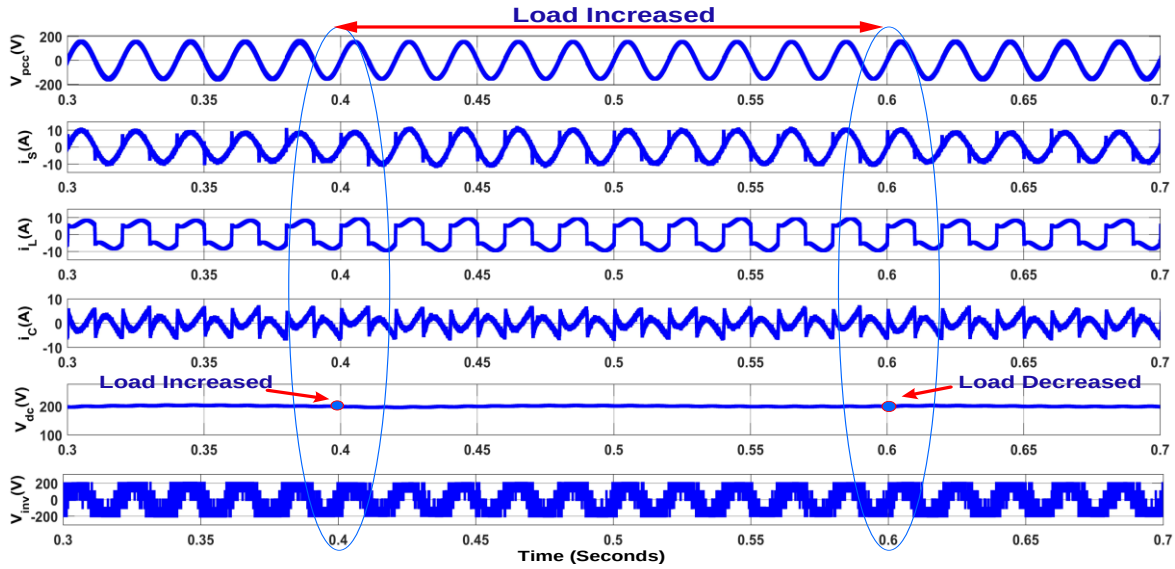



**Fig 5.4** Simulated waveforms of $v_s$, $i_s$, $i_L$, $i_C$, $V_{inv}$ and $V_{dc}$ during load variation at t=0.6s and t=1s with NLMAT Algorithm

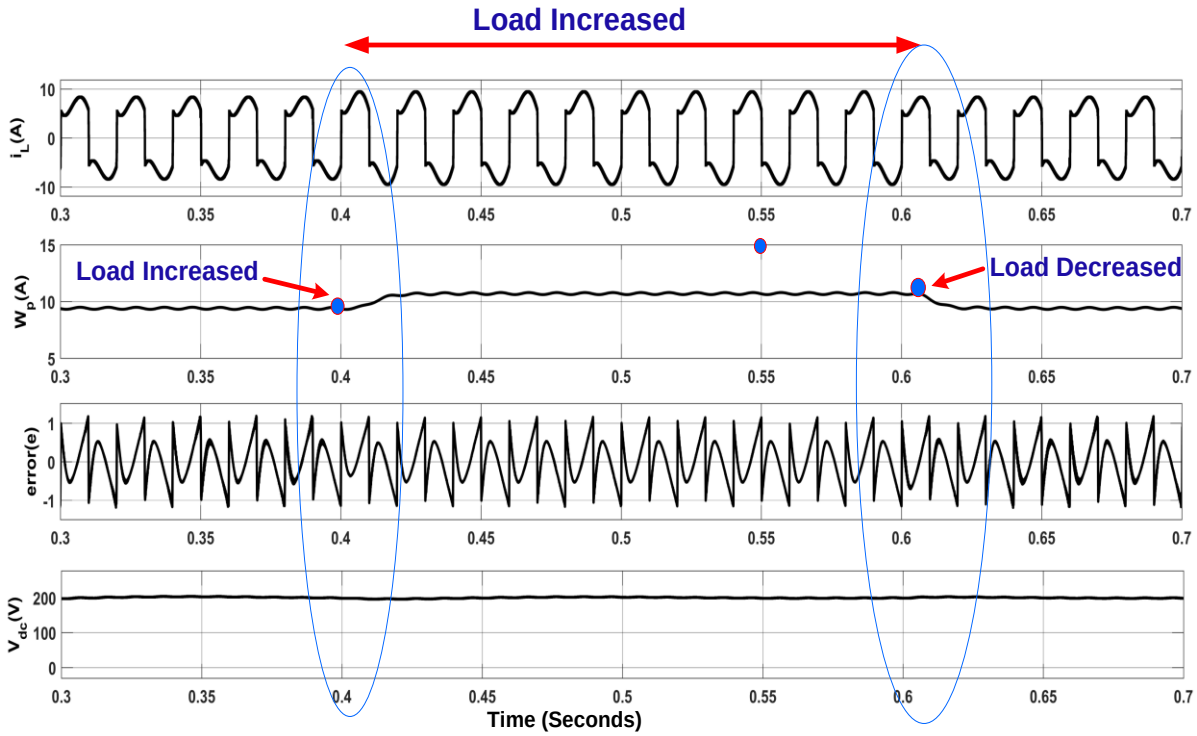
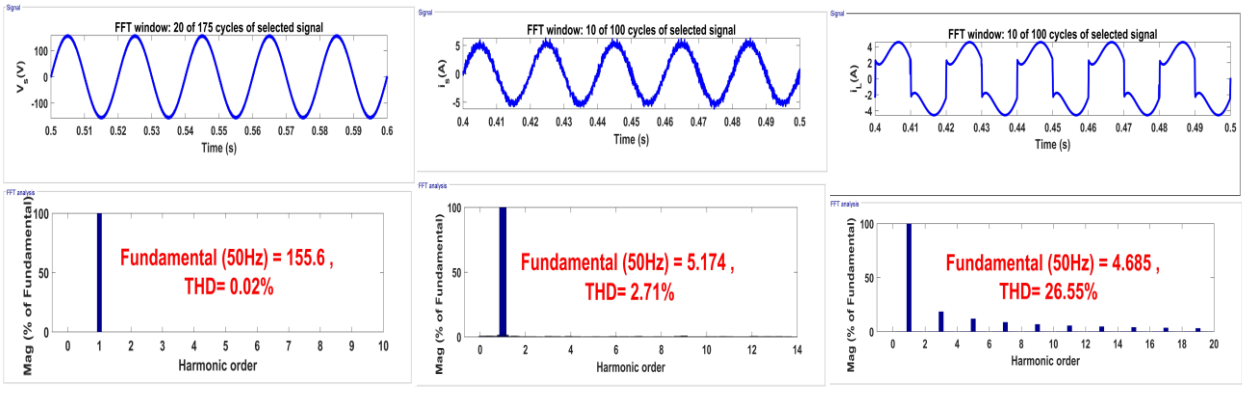



**Fig 5.5** Simulation Results of load current $i_L$(A), $w_p$(A), $i_C$(A) and $V_{dc}$(V) with NLMAT Algorithm

Fig 5.6 (a-c) shows the harmonic spectra of source current load current and source voltage. Before compensation, the source feeds the non-linear load and has a THD of 26.55%, similar to the load current as shown in Fig 5.6(c). However, after compensation using SAPF, the THD of source current reduces drastically to 2.71%. The compensator regulates the dc link voltage via the PI controller and improves the harmonic profile of the source current by injecting compensating current.




(a) (b) (c)

**Fig 5.6 (a-c)** Waveforms of $v_s$., $i_S$, and $i_L$ along with THD analysis with NLMAT Algorithm

### 5.3.1.2 Experimental Results with NLMAT Algorithm

Fig 5.7(a-c) depicts the steady-state waveforms of the proposed system. With respect to voltage across PCC ($V_{pcc}$), the source current ($i_s$), load current ($i_L$), and compensating current($i_C$) are shown. Fig 5.7 (d-f) Steady-state simulated waveforms of $v_s$ w.r.t $i_s$, $i_L$, $i_C$ with NLMAT algorithm. Before compensation, the source current feeds a non-linear load with a THD of 27.7%, as shown in Fig 5.7(e). After compensation, the source current THD is reduced to 2.9% (at $i_S$= 2.9A RMS), as depicted in Fig 5.7(d). The source voltage THD is 1.9% in undistorted conditions, as given in Fig 5.7(f). The proposed controller quickly estimates the fundamental weights and settles them after convergence in 1~2 cyles.

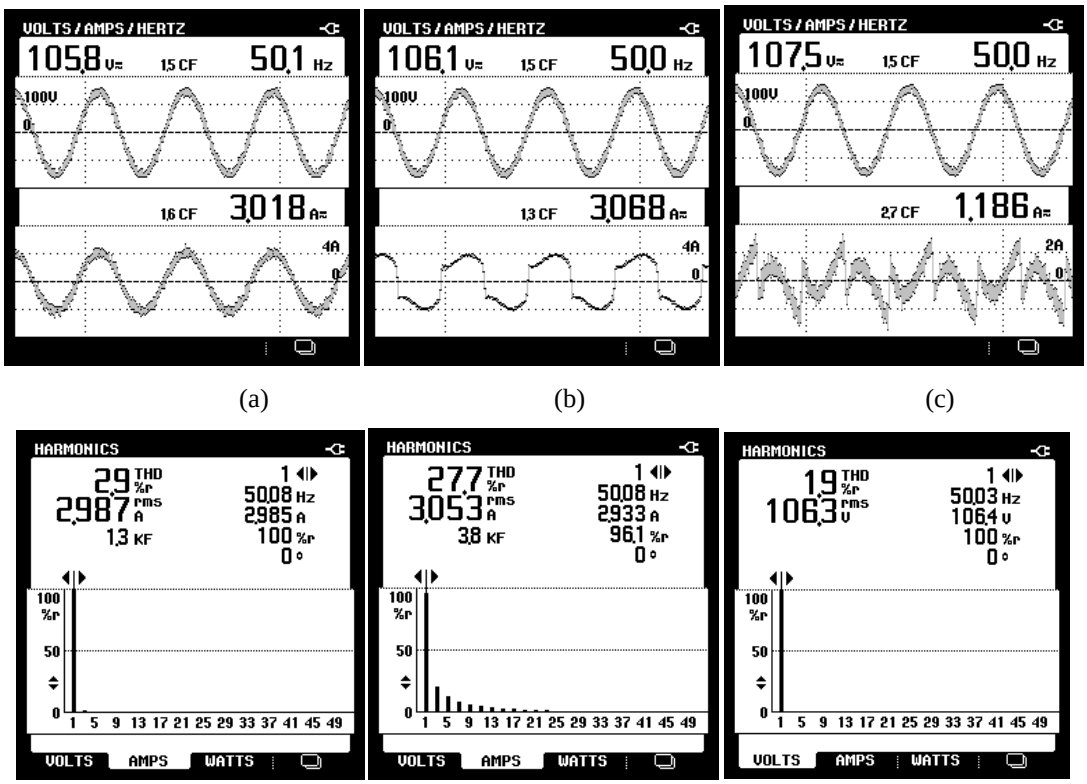
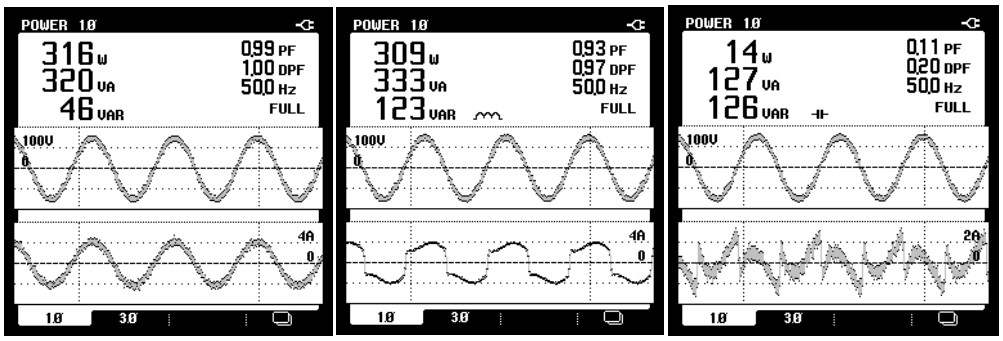



**Fig 5.7 (a-f)** shows the steady state results of source current ($i_s$), Load current ($i_L$), and compensating current ($i_c$) with respect to PCC voltage($V_{pcc}$) and associated THD values

It is depicted in Fig 5.8(a-c) that loads demand an active power of 0.309kW and reactive power of 0.123kVAR.The active supply power is 0.316kW, which satisfies not only the load demand but also meets the switching losses of CHB-MLI.

The compensator supplies 0.126KVAR of the load-required reactive power, as desired by the designed controller. The desired power flow is maintained between the source,

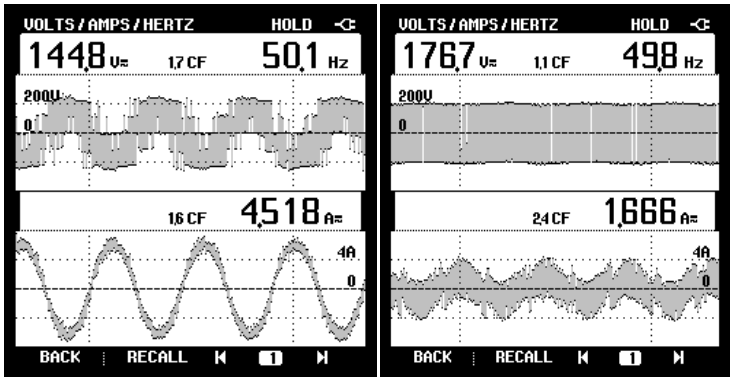
load, and compensator, and it is observed that the source current is sinusoidal and ideally in phase with the supply voltage.




(a) (b) (c)

**Fig 5.8 (a-c)** Steady-state active and reactive power in source, load, and compensator side with NLMAT algorithm

Fig 5.9(a-b) show the steady-state output voltage waveforms of 2-level and 5-level inverter. MLI possesses low switching losses; reduced harmonic is injected at PCC and MLI can synthesize good output voltage. The five-level inverter voltage has lower harmonic content than the two-level inverter.




(a) (b)

**Fig 5.9(a,b) O**utput voltage waveform of 5-level MLI w.r.t $i_s$ and output voltage of 2-level inverter w.r.t $i_c$ with NLMAT Algorithm

Fig 5.10(a-b) shows the dynamic results of $v_s$, $i_L$, $i_s$, $V_{dc}$ under dynamic load conditions. It is observed from the waveforms that the proposed algorithm can extract the fundamental active component of load current and make the source current sinusoidal and in phase with the supply voltage. In addition, the PI controller quickly stabilizes the dc link voltage to its reference value, and shows that NLMAT control algorithms work satisfactorily under varying load conditions.

Fig 5.10 (c) shows the waveforms of $i_S$, $V_{dc1}$, $V_{dc2}$, $V_{dc}$. It is seen that during load variation, both the dc link voltages are self-balancing. They quickly stabilize their DC link voltages to 100V each within a few cycles, and total dc link voltages stabilize to 200V within a few cycles. Fig 5.10 (d) shows the intermediate results such as error, and estimated weights ($W_{lP}$). It is concluded that the estimated fundamental active component is also varying on varying the load. These results depict the satisfactory working of the NLMAT algorithm.

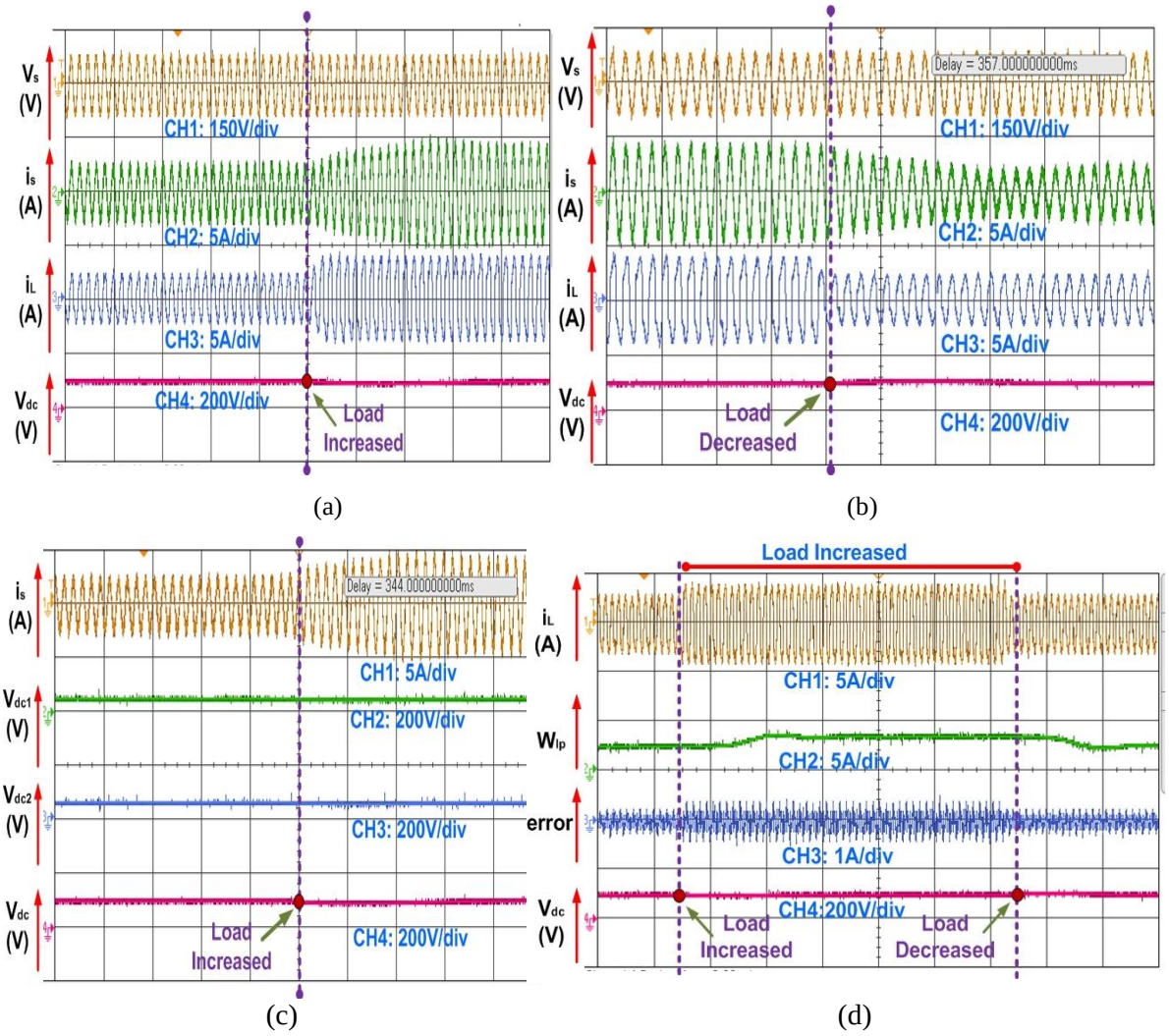



**Fig 5.10** Experimental waveforms of **(a,b)** $V_s$, $i_s$, $i_L$, $V_{dc}$ (c,d) $i_S$, $i_L$, $V_{dc1}$, $V_{dc2}$, $w_p$ and error under dynamic load variations with NLMAT algorithm

### 5.3.2 Non-linear Adaptive Normalized Huber (NHuber) Control Algorithm for 5-Level Distribution Static Compensator

The block diagram of the NHUBR control algorithm is shown in Fig 5.11

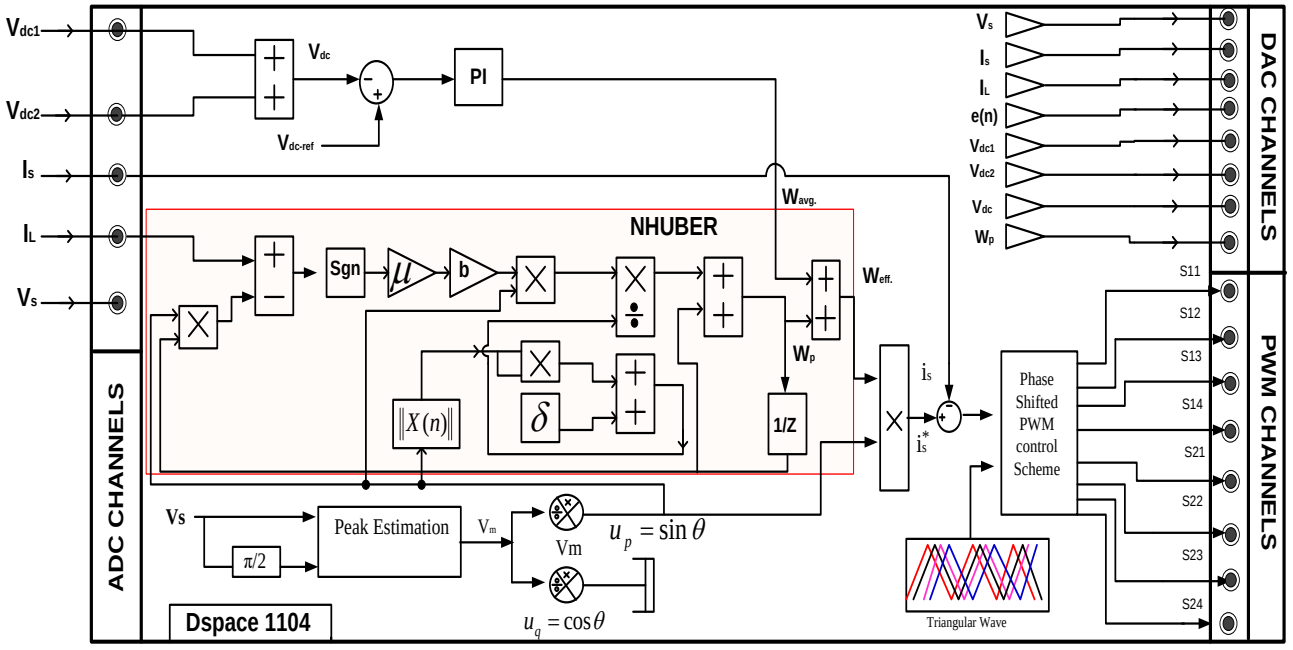



**Fig 5.11** Reference supply current estimation using N-Huber Algorithm using dSPACE-1104 under normal grid condition

### 5.3.2.1 Mathematical analysis of Non-linear Adaptive Normalized Huber (NHuber) Adaptive Control Algorithm

$i_{Lf}$ is the fundamental component of load current extracted from the NHuber algorithm and represented as

$$i_{Lf} = x^T(n)\,\omega(n-1) \tag{5.12}$$

$$e(n) = i_{L} - x^T(n)\,\omega(n-1) \tag{5.13}$$

where, x(n) = [x(n) x(n-1) ……x(n-M+1)] $^{T}$ (Mx1) input signal vector and w(n) = [ $w_o$ $w_1$ ……. $w_{(M-1)}$] is the weighted vector of NHuber filter at instant n. M is a total number of matrix vector.

The objective of the algorithm is to reduce the Huber cost function, defined as

$$J(i)=\begin{cases}\frac{1}{2}e^2(n), & |e(n)|\le b \\ b\,|e(n)|-\frac{1}{2}b^2 & |e(n)|>b\end{cases} \tag{5.14}$$

There is a trade-off to choosing the value of b, which is a contant value to be decided suitably. It has been observed that for a large value of b system may lose convergence, and for a low value, the tracking performance of the NHuber algorithm worsens. In addition, the stability of the NHuber algorithm is also affected by the eigenvalues of the autocorrelation matrix of input signals. Thus, the design of NHuber cost function is given by

$$J(n)=\frac{1}{2}\left|d(n)-w^T(n+1)\,x(n)\right|^2+\frac{1}{2}\left\|x(n)\right\|^2\left\|w(n+1)-w(n)\right\|^2 \tag{5.15}$$

where d(n) is the desired response, based on Equation 5.15

$$\frac{\partial J(n)}{\partial w(n+1)}=-e(n)\,x(n)+\left\|x(n)\right\|^2[\,w(n+1)-w(n)\,]=0 \tag{5.16}$$

Thus, weight updating Equation 5.16 is as follows:

$$w(n+1)=w(n)+\mu\frac{e(n)\,x(n)}{\left\|x(n)\right\|^2} \tag{5.17}$$

where μ is the step size. If |e(n)|>b , then

$$J(n)=b\left|d(n)-w^T(n+1)\,x(n)\right|-\frac{1}{2}b^2+\frac{1}{2}\left\|x(n)\right\|^2\left\|w(n+1)\;w(n)\right\|^2 \tag{5.18}$$

Thus, based on Equation 5.18

$$\frac{\partial J(n)}{\partial w(n+1)}=-b\,\mathrm{sgn}(e(n)\,x(n)+\left\|x(n)\right\|^2[w(n+1)-w(n)]=0 \tag{5.19}$$

The final weight updating (5.19) is given as

$$w(n+1)=w(n)+\mu\frac{b\,\mathrm{sgn}(e(n))\,x(n)}{\left\|x(n)\right\|^2} \tag{5.20}$$

To avoid division by a small numbers a very small positive constant $\delta$ is added to Equation 5.17 and Equation 5.20. Thus, the final weight updating equations of NHuber is defined as follows

$$w(n+1)=\begin{cases} w(n)+\mu\dfrac{e(n)\,x(n)}{\delta+\|x(n)\|^2} & |e(n)|\le b \\ w(n)+\mu\dfrac{b\,\mathrm{sgn}(e(n))\,x(n)}{\delta+\|x(n)\|^2} & |e(n)|>b \end{cases} \tag{5.21}$$

In this section, based on the weight updating Equation 5.20, the fundamental active power weight (wp) component of load current is estimated for |e(n)|>b.

### 5.3.2.2 Simulation Results with NHuber Algorithm

The simulink model of the proposed system is developed in MATLAB. The performance of the system is tested under normal grid conditions. The entire system is simulated using MATLAB/Simulink. The CHB-MLI unit is modeled and controlled for power factor correction, dc-link voltage control, harmonics mitigation, and reactive power compensation. Fig 5.12 depicts the simulation results, and Fig 5.13 shows the simulation results of intermediate signals.

An uncontrolled rectifier is connected at the dc side of the system, which is considered a non-linear load. Fig 5.12 shows the observed quantities like source voltage ($v_s$), source current ($i_s$), load current ($i_L$), compensating current ($i_C$), total dc link voltage ($V_{dc}$), and inverter output voltage ($V_{inv}$) under varying load at t=0.4s and t=0.6s, the corresponding load current increases from 5A to 8A and is decreased back to original value at t=0.6s. The following observations have been observed in the system response.

1. During dynamic load changes simulated at t=0.4s and t=0.6s, the total dc-link voltage ($V_{dc}$) sets itself to its reference value of 200V i.e., self-regulation is achieved within 1~2 cycles.
2. The CHB-MLI is suitably controlled so that the compensator current ($i_c$) cancels the effect of disturbances generated by the load at all times, even during load changes. The resulting source current is sinusoidal, smoothly controlled and in phase with the source voltage.

3. It is also observed that the performance of the PI controller action is relatively smooth. It is seen clearly that the PI controller quickly regulates each capacitor's dc - link voltages.
4. The power factor and displacement factor are almost unity in steady and transient state conditions.

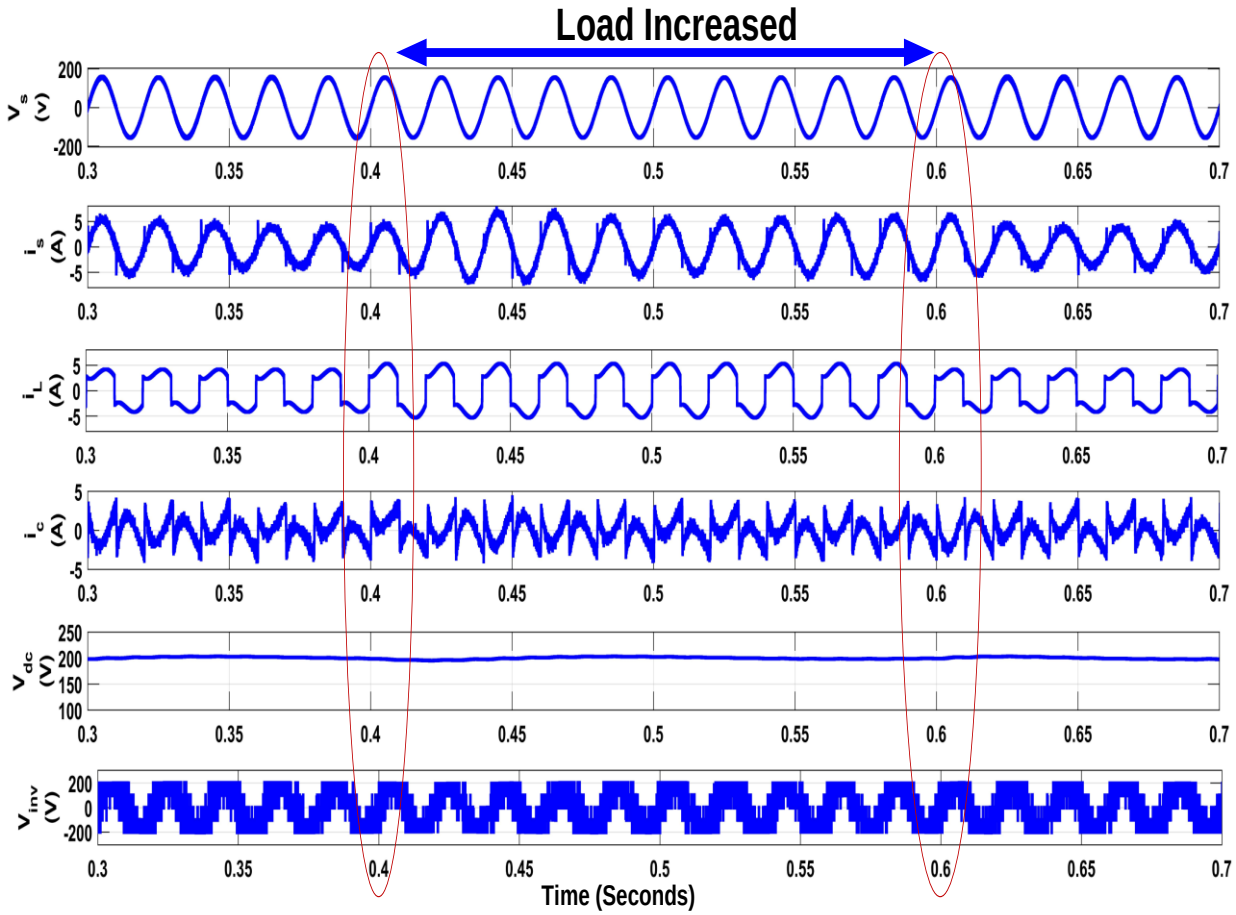



**Fig 5.12** Simulated waveforms of $v_s$, $i_s$, $i_L$, $i_c$, $V_{dc}$, $V_{inv}$ during sudden load variation at t=0.4s and t=0.6 s with NHuber algorithm

Fig 5.13 shows the waveforms of load current ($i_L$) weight ($w_p$), error(e), and $V_{dc}$. The control algorithm senses the parameters and calculates the updated weights corresponding to the fundamental component of the load current. Furthermore, the reference current is generated and compared with a triangular wave to generate PWM pulses of CHB-MLI.

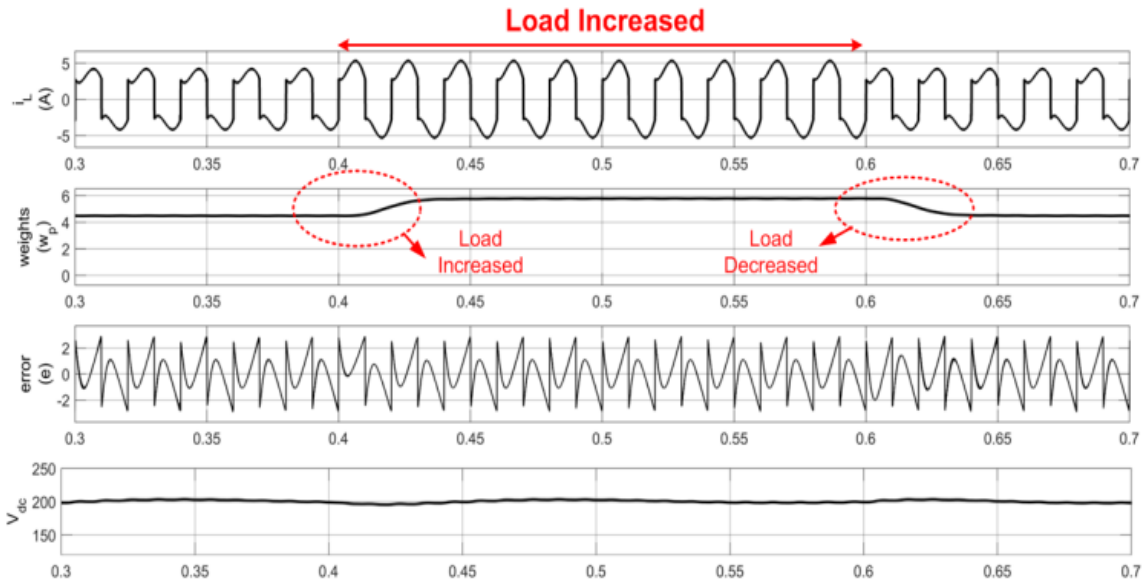
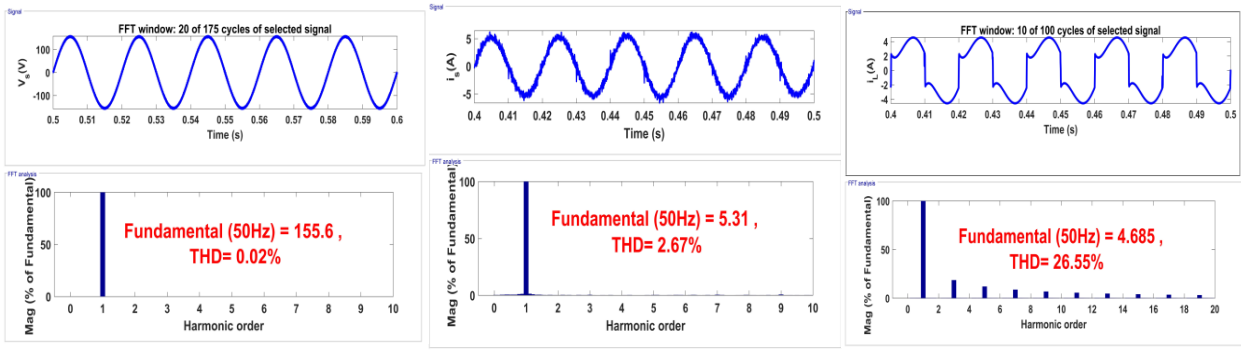



**Fig 5.13** Simulation waveforms of $i_L$, weights ($w_p$),error (e), and $V_{dc}$ during sudden variation of load at t=0.4s and t=0.6 s with NHuber algorithm

As the non-linear load increases, the active power and estimated component of load current varies accordingly. It is observed from the results that the proposed algorithm effectively calculates the fundamental component of load current under steady-state as well as dynamic load conditions. The estimated values are detected fast, requiring only 1~2 cycles for achieving convergence. Fig 5.19 (a-c) shows the harmonic spectrum of source voltage ($V_s$), Source current ($i_s$), and load current ($i_L$). It is observed that THD of $i_L$ is reduced from 24.16% to 2.67% in $i_s$ after compensation.




(a) (b) (c)

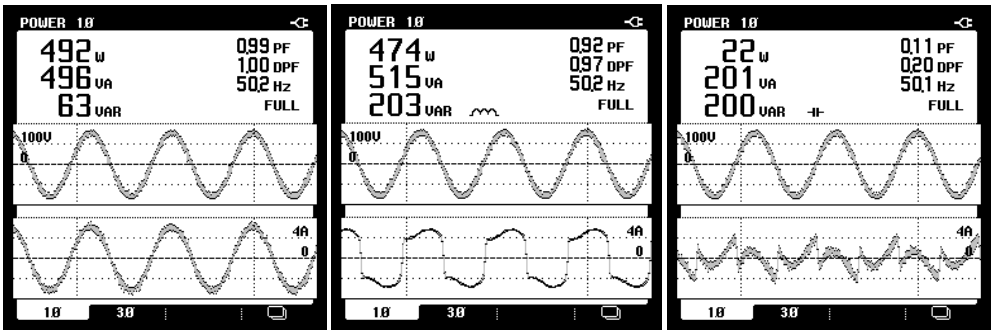
**Fig 5.14 (a-c)** Harmonic spectra of (a) PCC voltage, Vs, (b) grid current is, (c) load current, $i_L$ in PFC mode with NHuber algorithm

### 5.3.2.3 Experimental Results with NHuber Algorithm

A single-phase 110V, 50Hz system feeds a non-linear load. This load is conFigd by connecting a series R-L branch and variable resistance unit at the ends of a diode rectifier. The voltage signals such as $v_s$, $V_{dc1}$, $V_{dc2}$ is sensed using LV-25V voltage sensors, and current signals iL are sensed using LA-25P current sensors.

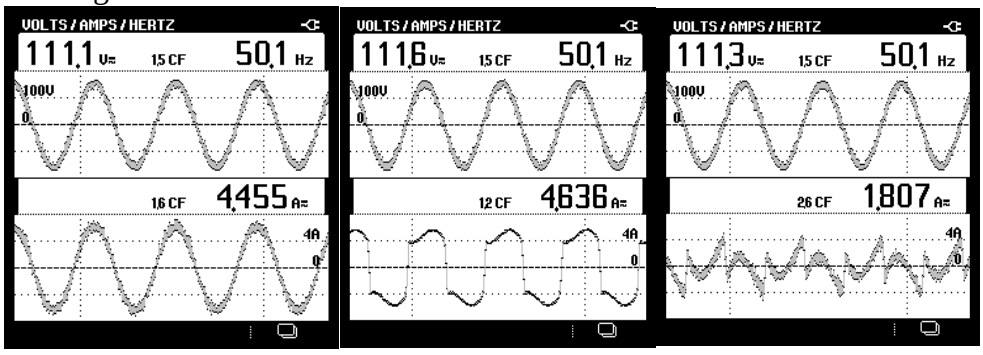
The proposed control algorithm generates the reference current and further generates PWM pulses buffer and isolation circuits to trigger IGBTs of CHB-MLI. The digital signal processor dSPACE-1104 processes the control algorithm and bring PWM signals out.

It is clear from Fig 5.15(a-c) that the load demands an active power of 0.474kW and reactive power of 0. 203kVAR.The active supply power required by the system is 0.492kW, which satisfies not only the load demand but also meets the switching losses of CHB-MLI. The compensator supplies 0.200KVAR of the reactive power required by the load, as desired by the controller. The desired power flow is maintained between source, load, and compensator and it is observed the source current is sinusoidal and perfectly in phase with the supply voltage.

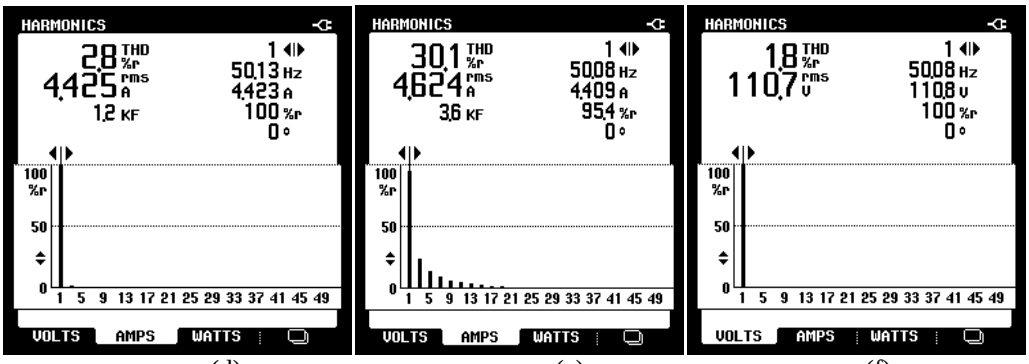



(a) (b) (c)

**Fig 5.15 (a-c)** Steady state active and reactive power in source, load and compensator side with NHuber algorithm




(a) (b) (c)

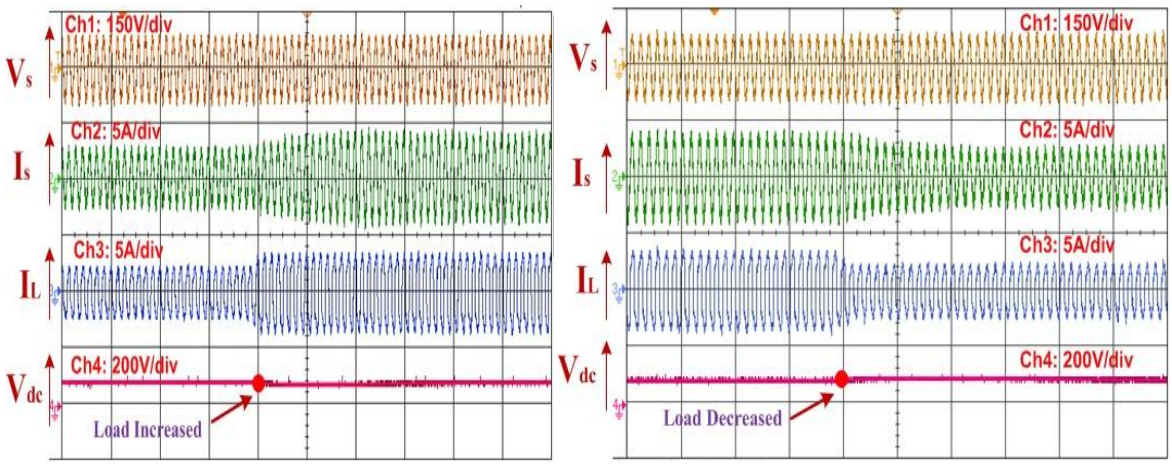



(d) (e) (f)

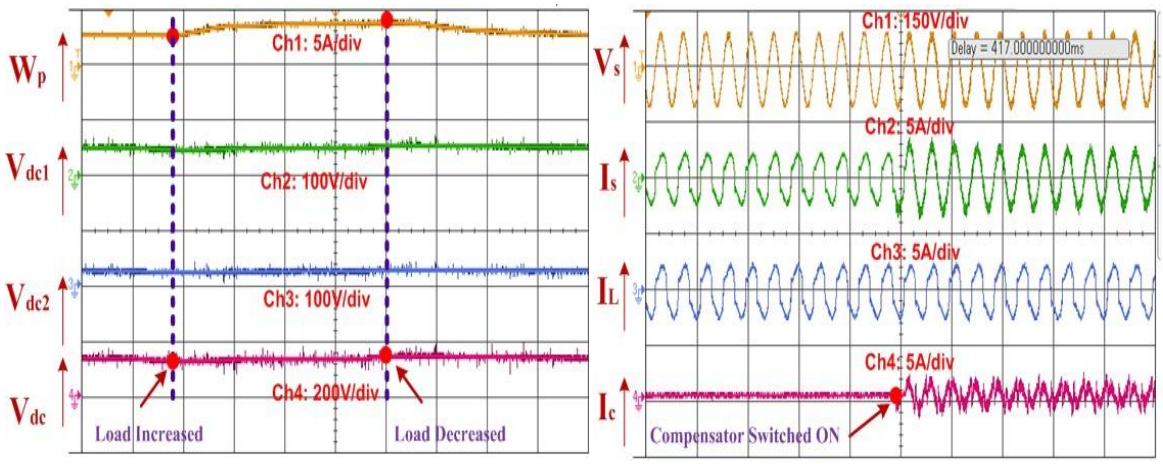
**Fig 5.16 (a-f) S**teady state results of source current ($i_s$), Load current ($i_L$), and compensating current ($i_c$) with respect to PCC voltage($V_{pcc}$) and associated THD values

Fig 5.16(a-f) shows the steady-state waveforms of $i_c$, $i_L$, with respect to PCC voltage $V_{pcc}$ followed by its %THD spectrum. It is observed that after compensation, current ($i_s$) THD is reduced to 2.8%, and the THD of the supply voltage is 1.8%. These results show the highly satisfactory performance of the NHuber control algorithm to achieve unity power at the source side. The proposed system also achieves the stipulated IEEE standards, thereby meeting PQ standards effectively.

Fig 5.17 (a-d) shows the system's dynamic performance under varying load conditions. The parameters $v_s$, $i_s$, $i_L$, $V_{dc1}$, $V_{dc2}$, $V_{dc}$, $i_{C,}$ and weights during sudden load variations are shown. It is observed from Fig 5.22 (a) that the source current is almost sinusoidal and in phase with voltage after compensation. DC link capacitors self-regulate the voltages within a few cycles processed through the PI controller. Intermediate weights get converge quickly during sudden load variations.




(a) (b)




(c) (d)

**Fig 5.17 (a-d)** Weights($w_p$), dc link voltage of capacitor 1 ($V_{dc1}$), dc link voltage of capacitor-2 ($V_{dc2}$) and total dc link voltage ($V_{dc}$), source voltage ($V_s$), source current ($i_s$), load current ($i_L$) and compensating current ($i_c$) with Nhuber Algorithm

### 5.3.3 Robust Shrinkage Affine Projection Sign (RSAPS) Control Algorithm for 5-level shunt compensation

The digital implementation of the proposed scheme is shown in Fig 5.18. The SAPF is controlled by RSAPS adaptive filtering technique. Appropriate firing pulses are generated for the control of CHB-MLI as a compensator.

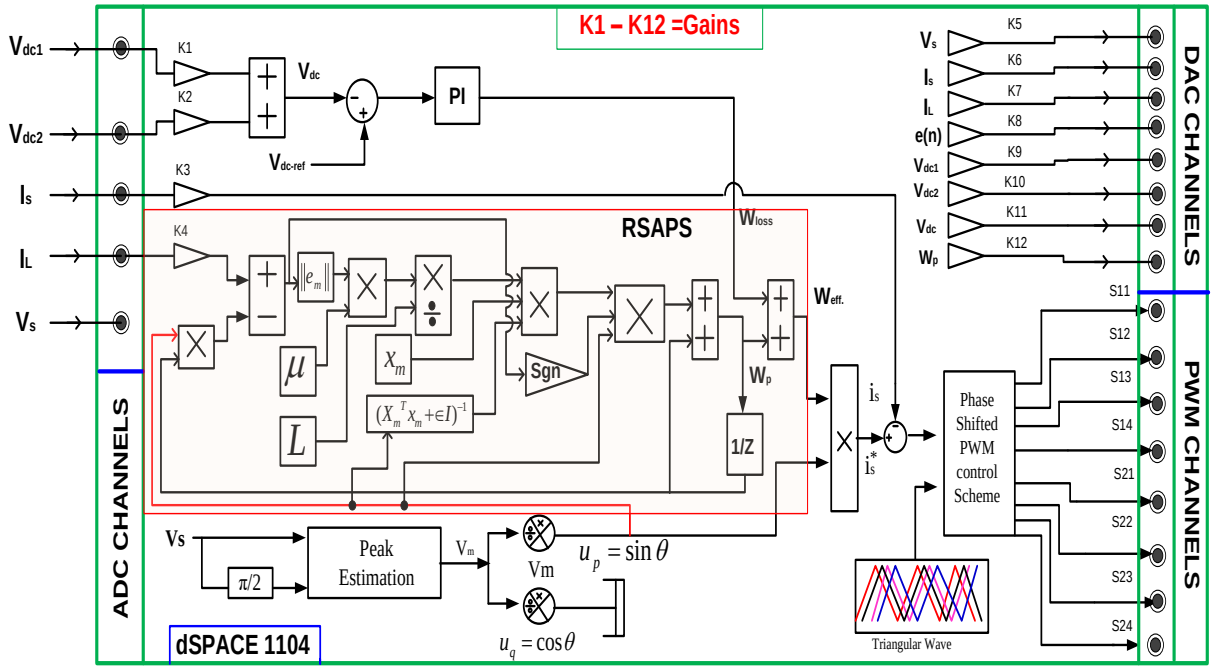



**Fig 5.18** Detailed block diagram of proposed controller with RSAPS Algorithm

### 5.3.3.1 Mathematical analysis of Robust Shrinkage Affine Projection Sign (RSAPS) Algorithm

The Robust Shrinkage Affine Projection Sign (RSAPS) is a standard adaptive filtering algorithm that employs multiple input vectors[133]. Now, the RSAPS algorithm is designed by minimizing the cost function, J, given as

$$\min_{w} . J(w) = 0.5 \left\| d_m - x_m^t w \right\|_1 \tag{5.22}$$

where $d_m = [d(m)\ d(m-1) \ldots\ldots d(m-L+1)]^T \in R^{Lx1}$ is the desired vector for system identification, $w \in R^{Mx1}$ is an adaptive weight vector and $x_m = [x_m\ x_{m-1} \ldots\ldots x_{m-L+1}] \in R^{MxL}$ is the input signal matrix. Equation 5.22 is made of continuous function and $J(w)$ can be approximated by the minimization function

$$\hat{J(w)} = 0.5 \left\| O_i^{0.5} (d_m - x_m^t\ w) \right\| \tag{5.23}$$

Where $O_i^{0.5} = dig\left\{ \frac{1}{\sqrt{|e_i(1)|}}, \frac{1}{\sqrt{|e_i(2)|}} \ldots\ldots \frac{1}{\sqrt{|e_i(L)|}} \right\}$ and $e_i$ is the priority error signal which is commonly used for any adaptive identification algorithm and $O_i$ is the diagonal matrix of the error signal, its expression can be given by

$$e_i = d_m - x_m^t\ w_{i-1} \tag{5.24}$$

The weight updating equation of the proposed RSAPS algorithm is derived by minimizing the cost function $J(w)$ , represented as

$$w_i = w_{i-1} + Y_m\ x_m (x_m^t\ x_m + \varepsilon I)^{-1} O_{i-2}\ e_i \tag{5.25}$$

where $Y_m$ is obtained by settling the gradient $J(w)$ with respect to $w$ equating to zero. The values of m, $d_m$, and $x_m$ is updated, and the process is carried forward until convergence is achieved. This approach makes Equation 5.25 offline. To achieve real-time weight updation, Equation 5.25 is realized with i=m, and hence, the new weight updating equation is given by

$$w_m = w_{m-1} + Y_m\ x_m (x_m^t\ x_m + \varepsilon I)^{-1} \operatorname{sgn}(e_m) \tag{5.26}$$

It is assumed that $O_{i-2}e_i \cong O_i e_i = \text{sgn}(e_m)$ . This approach of real-time implementation is commonly used in the $l_1$ norm of the LMS algorithm, but exact minimization $\hat{J}(w)$ is not achieved hence Equation 5.26 obtained is needed to be modified as given below

$$Y_k = \frac{\|e_k\|_1}{L} \tag{5.27}$$

Here L is constant to be in the range of 1 to 5[133]. From Equation 5.26 and Equation 5.27, the final weight updating equation is calculated as

$$w_i = w_{i-1} + \mu \frac{\|e_m\|}{L} (x_m^t x_m + \varepsilon I)^{-1} \text{sgn}\, e_m \tag{5.28}$$

where μ is the step size parameter, and a suitable value between 0 and 1 is selected. Further, the RSAPS Equation 5.28 is implemented to obtain the fundamental active power component of load current, as depicted in Fig 5.18. For load current $i_L$(m), desired response d(m), input vector x(m) and the weight vector w(m) is expressed as

$$x(m) = [\, x_1(m)\ x_2(m)\ x_3(m).....x_N(m)\,]^T \tag{5.29}$$

where, $x_1(m) = [\sin w_1 m\Delta t\ \cos w_1 m\Delta t\ ]^T$

$$w(m) = [\, w_1(m)\ w_2(m)\ w_3(m).....w_N(m)\,]^T \tag{5.30}$$

and here, $w_1(m) = [w_{1p}(m)\ w_{1q}(m)]^T$ , and $w_{1p}$ *and* $w_{1q}$ denotes the in-phase and quadrature weight component.

From Equation 5.29 and Equation 5.30, the updating expression of output error and weights can be expressed as

where

$$e(m) = i_L(m) - \begin{bmatrix} w_{1p}(m) \\ w_{1q}(m) \\ w_{2p}(m) \\ w_{2q}(m) \\ - \\ - \\ - \\ - \\ w_{Np}(m) \\ w_{Nq}(m) \end{bmatrix}^T * \begin{bmatrix} \sin \omega_1 m\Delta t \\ \cos \omega_1 m\Delta t \\ \sin 2\omega_2 m\Delta t \\ \cos 2\omega_2 m\Delta t \\ - \\ - \\ - \\ - \\ \cos N\omega_1 m\Delta t \\ \sin N\omega_1 m\Delta t \end{bmatrix} \tag{5.31}$$

The load current is composed of various fundamental and harmonic components and can be defined as

$$\begin{bmatrix} i_{L1}(m) \\ i_{L2}(m) \\ i_{L3}(m) \\ - \\ - \\ i_{LN}(m) \end{bmatrix} = \begin{bmatrix} i_{L1p}(m)+i_{L1q}(m) \\ i_{L2p}(m)+i_{L2q}(m) \\ i_{L3p}(m)+i_{L3q}(m) \\ - \\ - \\ i_{LNp}(m)+i_{LNq}(m) \end{bmatrix} = \begin{bmatrix} \omega_{1p}(m).\sin\omega_{1m}m\Delta t+\omega_{1q}(m).\cos\omega_{1m}m\Delta t \\ \omega_{2p}(m).\sin 2\omega_{2m}m\Delta t+\omega_{2q}(m).\cos 2\omega_{2m}m\Delta t \\ - \\ - \\ \omega_{Np}(m).\sin N\omega_{Nm}m\Delta t+\omega_{Nq}(m).\cos N\omega_{Nm}m\Delta t \end{bmatrix} \quad (5.32)$$

Using Equation 5.32 at $m^{th}$ sampling instant, the SAPF injects the compensating current estimated as

$$i^{*}_{inj}(m)=i_{L1(q)}(m)+\sum_{h=2}^{N} i_{Lh}(m) \quad (5.33)$$

$$i^{*}_{inj}(m)=\omega_{1q}(m)*\cos\omega_1 m\Delta t+\sum_{h=2}^{N}\left\{\omega_{hp}(m)*\sinh\omega_1 m\Delta t+\omega_{hq}(m)*\cosh\omega_1 m\Delta t\right\} \quad (5.34)$$

### 5.3.3.2 Simulation Results with RSAPS Algorithm

The simulation analysis of the proposed system is discussed in this section. The robustness and performance of the proposed system have been studied under steady state, and dynamic load conditions and simulations have been performed using MATLAB/Simulink software. A single-phase AC supply feeds power to the diode rectifier and R-L branch, which acts as a non-linear load. The response of several signals has been analyzed and presented in Fig 5.19 and Fig 5.20.

Fig 5.19 shows plots of source voltage ($v_S$), source current ($i_S$), load current ($i_L$), DC link voltage across capacitor-1 ($V_{dc1}$), DC link voltage across capacitor-2 ($V_{dc2}$), total DC link voltage ($V_{dc}$). In addition, some intermediate signals, such as estimated fundamental weights ($w_{eff}$) error signal (e) and output voltage of 5-level CHB-MLI have also been observed, as shown in Fig 5.20. The load current is varied at time $t_1$=0.4s and $t_2$=0.6s by changing load.

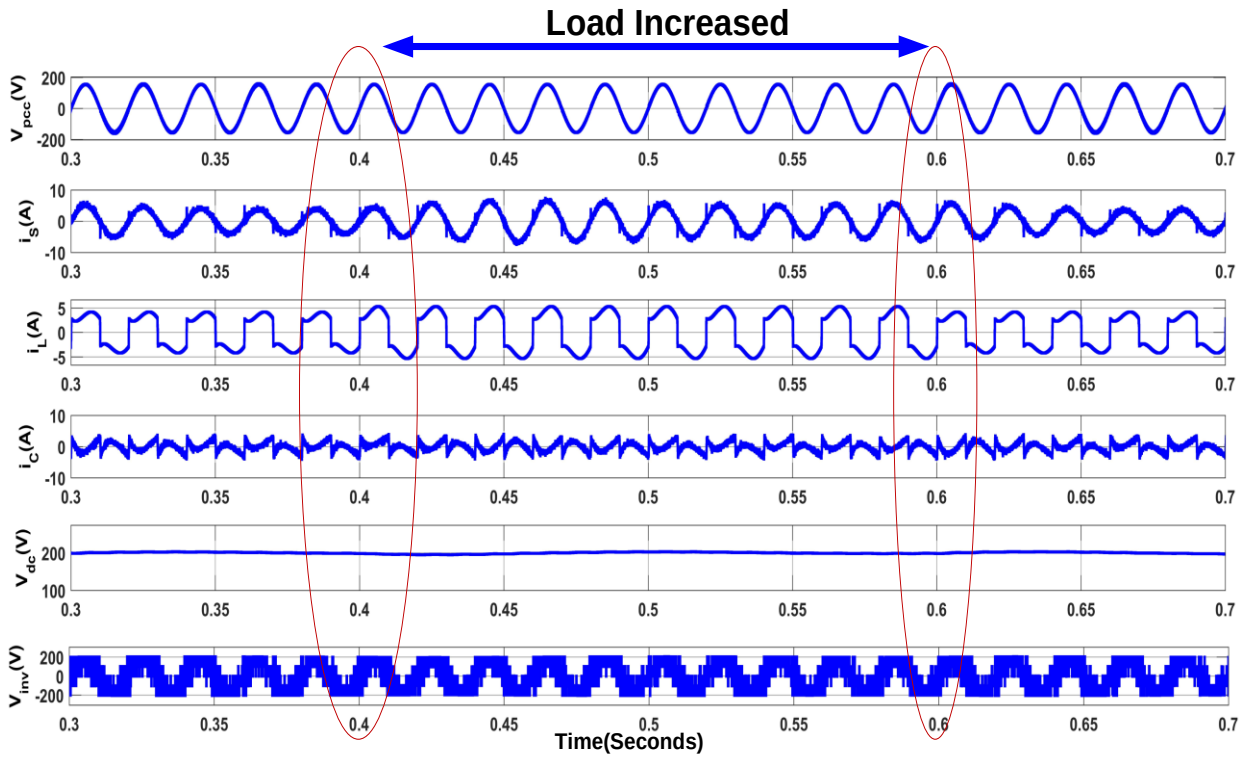



**Fig 5.19** Simulated waveforms of $V_s$, $i_s$, $i_L$, $i_c$, $V_{dc}$, $V_{inv}$ during sudden load variation at t=0.4s and t=0.6 s with RSAPS algorithm

The DC link voltage varies at the instants of load variation, which can be observed in Fig 5.19. A minor variation in total (and individual) DC link voltages has been observed compared to the reference value (200V). However, due to the PI controller's fast action, the DC link reaches the reference value within a few cycles.

The intermediate waveforms of $i_L$, $w_{est}$, error (e), and inverter output voltage ($V_{inv}$) are shown in Fig 5.20. At $t_1$=0.4s and $t_2$=0.6s, the load varies, and the computed fundamental weight component of the load current changes accordingly. This demonstrates that the proposed RSAPS algorithm can accurately estimate the fundamental active power component within a few cycles, and the adaptive algorithm can estimate the new weight value under varied load conditions.

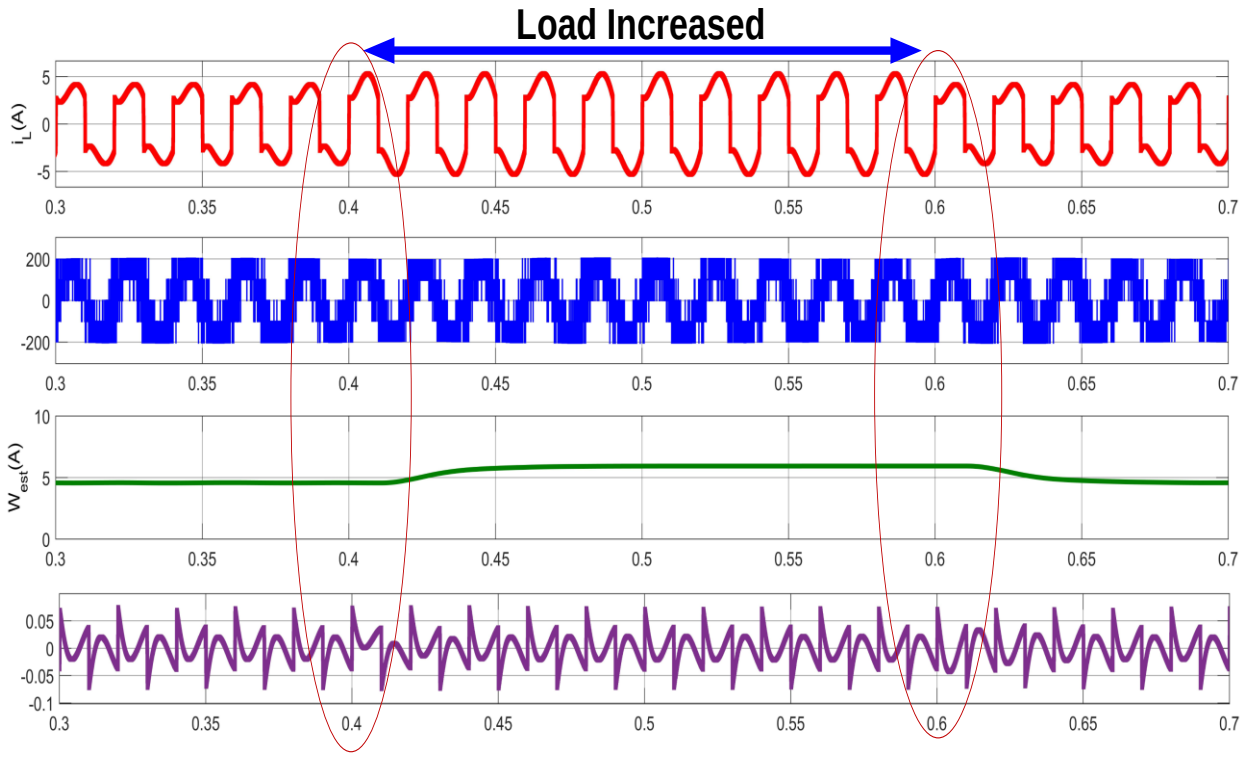
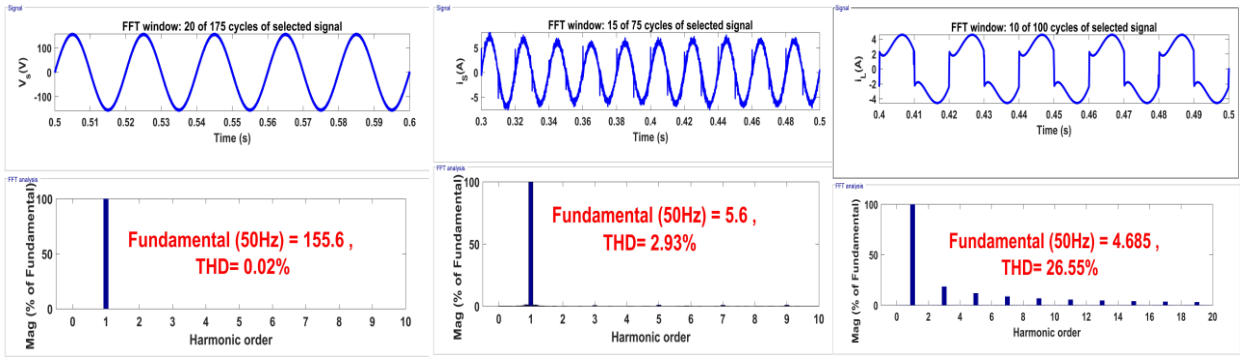



**Fig 5.20** Intermediate system behavior under dynamic load change at t=0.4s and t=0.6s with RSAPS algorithm

Fig 5.21(a-c) shows the harmonic spectra of source current load current and source voltage. Before compensation, the source feeds the non-linear load and has a THD of 17.55%, similar to the load current, as shown in Fig 5.36(c). However, after compensation using SAPF, the THD of source current reduces drastically to 2.56%.




(a) (b) (c)

**Fig 5.21** Harmonic spectra of (a) PCC voltage, vs, (b) grid current is, (c) load current, $i_L$in PFC mode with RSAPS algorithm

### 5.3.3.3 Experimental Results with RSAPS Algorithm

Steady-state experimental results of the proposed system are presented in Fig 5.22(a-e). It depicts the voltage of PCC ($V_{pcc}$), source current ($i_s$), load current ($i_L$), and compensating current ($i_C$). Source current follows load current with a THD of 28.7% before compensation. The THD of source current is reduced to 2.4 % after compensation. The injected SAPF current mitigates the harmonics generated by the non-linear load. The %THD of PCC voltage is 1.9%, as shown in Fig 5.22(e).

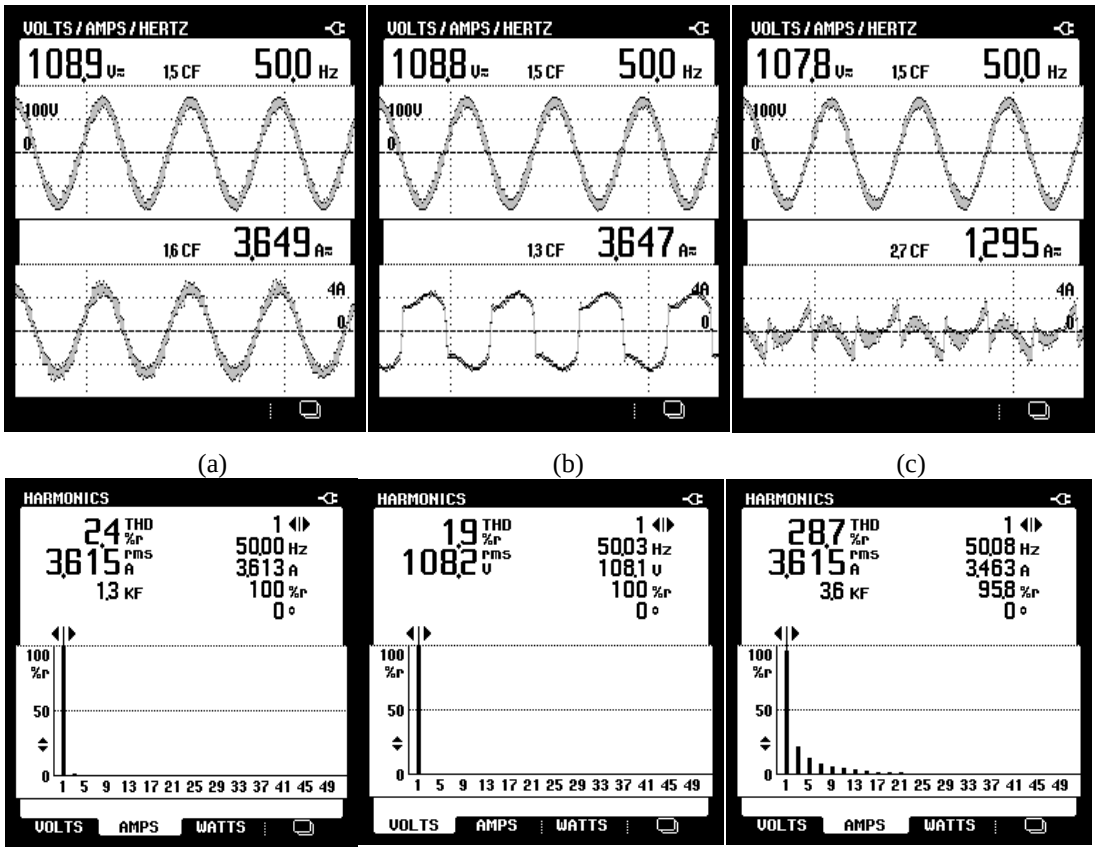
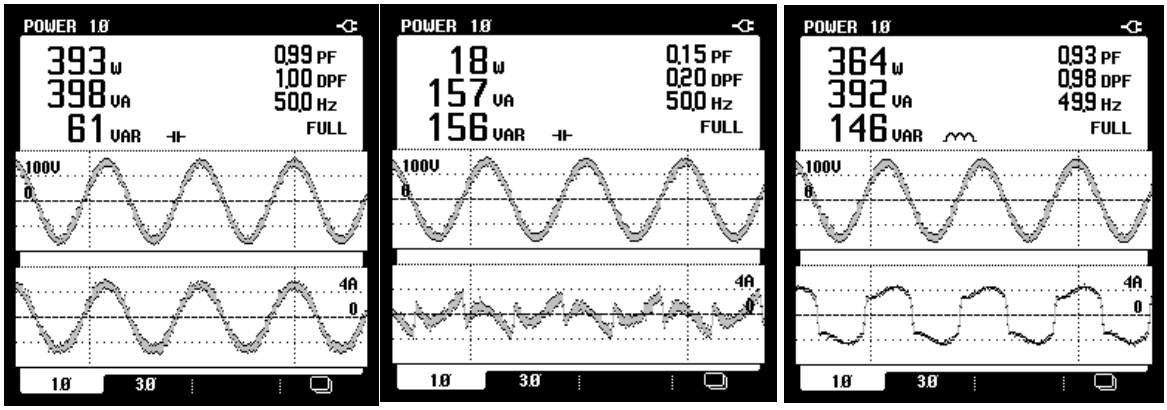



**Fig 5.22** Steady-state performance of the system (a) $v_S$ and $i_S$ (b) $v_S$ and $i_L$ (c) $v_S$ and $i_C$ along with harmonic spectrum (d) %THD of $i_S$ (e) %THD of $v_S$ and (f) % THD of $i_L$

Furthermore, the supply current is nearly sinusoidal and in phase with the source voltage. The recorded waveforms show that the proposed system works satisfactorily, and the obtained %THD of $V_{pcc}$(V) and $i_S$(A) is within stipulated IEEE-519 standards. The

steady-state power requirements in the system are shown in Fig 5.23(a-c). The load has active and reactive power demands of 364W and 146VAR, and the SAPF meets the reactive power demand of the load by feeding 156VAR. The grid supplies 393 W to meet the real power of the load along with the switching losses




(a) (b) (c)

**Fig 5.23** Steady-state active and reactive power in source, load, and compensator side with RSAPS algorithm

The performance of the proposed system under dynamic load conditions is shown in Fig 5.24. The waveforms of PCC voltage ($V_{pcc}$), source current ($i_S$), load current ($i_L$), and total DC link voltage ($V_{DC}$) are shown. In Fig 5.24(a), a sudden change in load increases the load current, and the fast action of the PI controller regulates the total DC link voltage quickly to the reference value of 200V ± 2V. Similarly, the performance of the system under a decrease in load is depicted in Fig 5.24(b), Fig 5.24(c), and Fig 5.24(d) shows the waveforms of $i_L$, $V_{DC1}$, $V_{DC2,}$ and $V_{DC}$ during sudden perturbation in load. It is observed from the waveforms that both DC link voltages of capacitors have reached ~100V within a few cycles. Hence the total DC link voltage remains stable and well-regulated even during dynamic load conditions.

The intermediate results of the system are shown in Fig 5.25 under simultaneous increase and decrease of load. Fig 5.25 shows load current ($i_L$), estimated eight ($w_{eff}$), error (e), and total DC link voltage ($V_{dc}$) on the oscilloscope. The DC link voltage varies with increasing or decreasing the load, showing a voltage dip and rise, respectively. The tuned PI controller on the DC link voltage easily restores the voltage to the 200V reference value. This result depicts the satisfactory performance of the RSAPS algorithm. The fundamental

estimated component is effectively computed by the RSAPS algorithm, and all parameters reach a steady state within a few cycles.

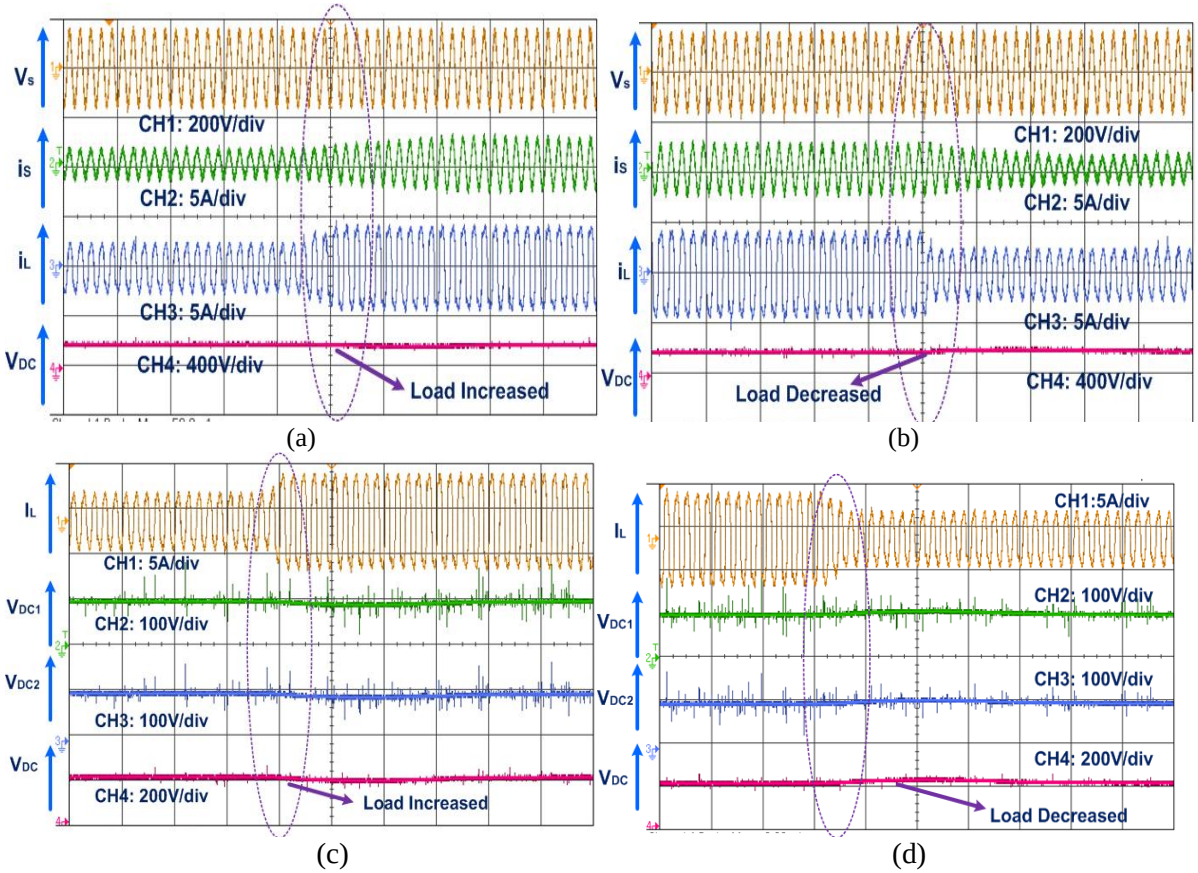



**Fig 5.24** Dynamic behavior of the proposed system with RSAPS algorithm

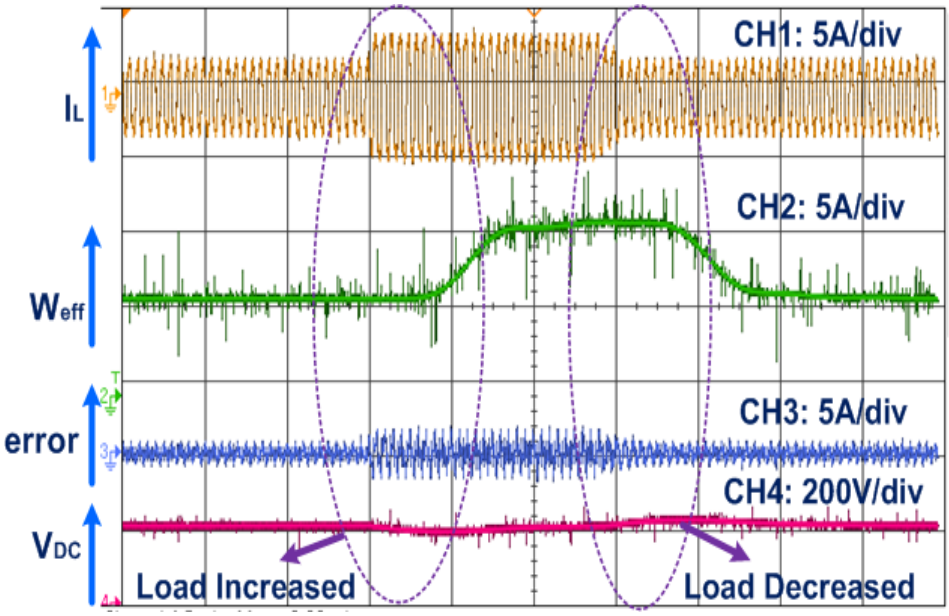



**Figure 5.25 Dynamic** behavior of the proposed system (a) $I_L$ , $w_{eff}$ , error(e) and $V_{DC}$ under increase and decrease in load with RSAPS algorithm

## 5.4 Comparative Performance of NLMAT, NHuber, and RSAPS Algorithms

In this chapter, to mitigate the PQ issues, the fundamental component of load current is extracted by the three advanced adaptive control algorithms, viz. NLMAT, NHuber and RSAPS.These algorithms are effective in harmonic mitigation and reactive power compensation and make the system source current near the unity power factor. The system's performance feeding non-linear load is tested and verified through simulation and experimental results under dynamic load conditions.

Fig 5.26 and Fig 5.27 show the simulation and experimental performance of fundamental estimated active power component convergence analysis with NLMAT, NHuber, and RSAPS algorithms. It is observed from Fig 5.26 that the NLMAT and Nhuber achieve weight convergence within 1~2 cycle. However, the convergence achieved by RSPAS requires approximately 3~4 cycles. The system is tested under dynamic load change at t=0.4s and t=0.6s

The comparison tables have been tabulated based on the simulation and experimental results achieved. Table 5.1 shows that the source current THD is reduced to 2.9% from 27.7% with NLMAT, 2.8% from 30.1% with NHuber, and 2.4% from 28.7% in RSAPS algorithms.

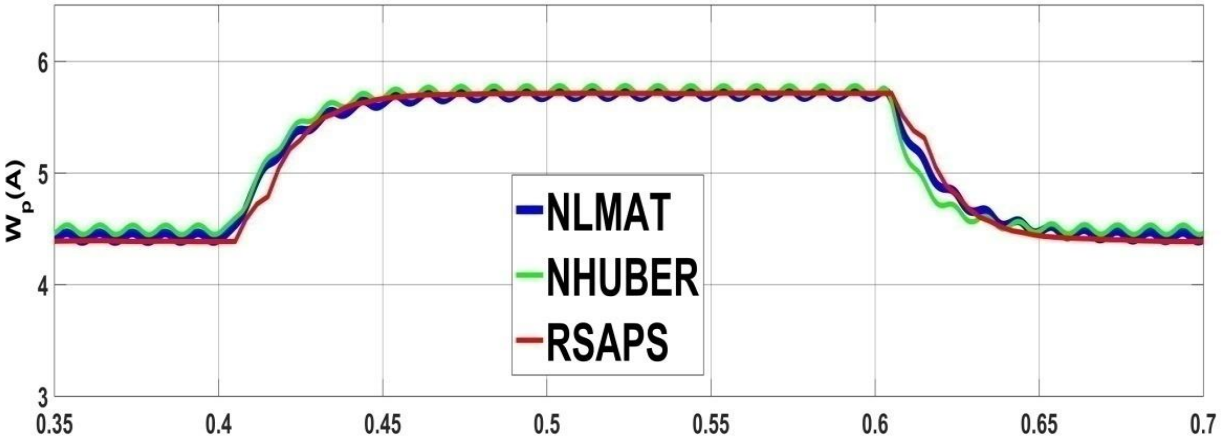



**Fig 5.26** Simulation-based performance comparison of fundamental weights under varying load during t=0.4s to 0.6s with NLMAT, NHuber, RSAPS

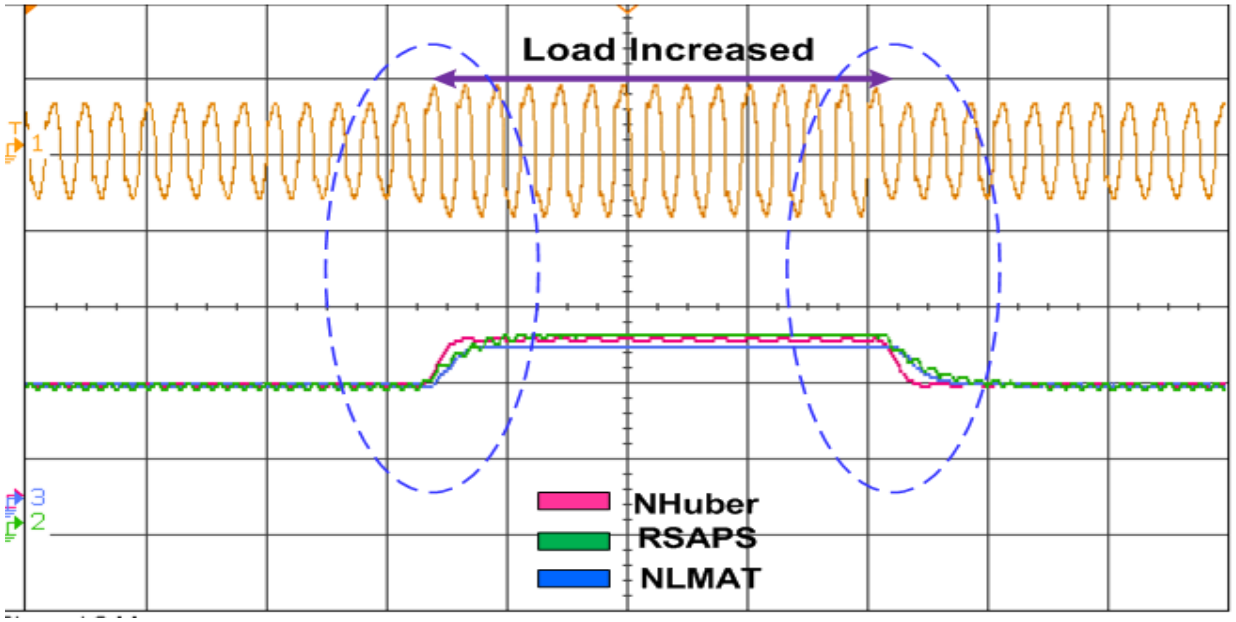



**Fig 5.27** Experimental-based performance comparison of fundamental weights under varying loads with NLMAT, NHuber, RSAPS

Table 5.2 shows the proposed system's active and reactive power requirements to satisfy the load required and meet the switching loss. Using the NLMAT algorithm, the load demands an active power of 0.309kW and reactive power of 0.123kVAR. The active supply power is 0.316kW, which satisfies not only the load demand but also meets the switching losses of CHB-MLI. Similarly, with the NHuber algorithm, the load demands an active power of 0.474kW and reactive power of 0. 203kVAR.The compensator supplies 0.200KVAR of the reactive power required by the load, as desired by the controller, and in the RSAPS algorithm, the load has a real and reactive power demand of 364W, and 146VAR and the SAPF meets the reactive power demand of the load by feeding 156VAR.

**Table 5.1 Comparative Performance of NLMAT, NHuber and RSAPS Algorithms**

| S.No. | Features | NLMAT | NHuber | RSAPS |
|---|---|---|---|---|
| 1. | PLL required | Not required | Not required | Not Required |
| 2. | Transformation required | No | No | No |
| 3. | Convergence | **Fast (2~3 cycles)** | **Fast (1~2 cycles)** | Moderate **(3~4 cycles)** |
| 4. | Oscillations in fundamental | Less | Moderate | Moderate |

| | | | | | |
|---|---|---|---|---|---|
| | weights | | | | |
| 5. | THD of current (Simulation study) | Supply current | 2.71% | **2.67%** | 2.93% |
| | | Load current | 23.55% | 23.55% | 23.55% |
| 6. | THD of current (Experimental study) | Supply current | 2.9% | 2.8% | **2.4%** |
| 7. | | Load current | 27.7% | 30.1% | 28.7% |
| 8. | DC link Voltage Oscillations | | 2V | 1-2V | 2-3V |
| 9. | Sampling time | | 60µs | **50µs** | 60µs |

**Table 5.2** Active and Reactive power comparison of different control algorithms

| S.No. | Parameters | NLMAT | NHuber | RSAPS |
|---|---|---|---|---|
| 1. | Source Power | Ps=316W<br>Qs=46VAR | Ps=462W<br>Qs=63VAR | Ps=393W<br>Qs=46VAR |
| 2. | Load Power | $P_L$=309W<br>$Q_L$=123VAR | $P_L$=474W<br>$Q_L$=203VAR | $P_L$=309W<br>$Q_L$=123VAR |
| 3. | Compensating Power | $P_c$=14W<br>$Q_c$=126VAR | $P_c$=22W<br>$Q_c$=200VAR | $P_c$=14W<br>$Q_c$=126VAR |
| 4. | Power Factor | 0.99 | 0.99 | 0.99 |

## 5.5 Conclusion

The proposed system is developed and tested using three advanced adaptive control algorithms: NLMAT, NHuber, and RSAPS. The response of all control algorithms is tested under load variations and normal grid supply. Both simulation and experimental investigations have been studied in detail.

The experimental THD of grid current obtained using the RSAPS algorithm is much less (2.4%) than in other adaptive control algorithms. However, simulation results indicate the THD obtained with NHuber algorithm is less (2.67%) while 3.71% with NLMAT and

2.93% with RSAPS. Thus, small variations are observed in the obtained results, although all techniques meet IEEE standards perfectly well.

It is also observed that the RSPAS shows a slightly slower convergence (3~4 cycles) of the fundamental weight component while NLMAT and NHuber performance is better in convergence, i.e., within 1~3 cycles. NHuber algorithm suffers from few oscillations in the fundamental weights, but the sampling time requirement of NHuber is found to be less, i.e., 50μs. In the case of DC link voltage oscillations, NHuber gives a fast response and quickly converges to a steady state of 200V.

The complexity of the RSPAS algorithm is highest as compared to other algorithms viz. NLMAT and NHuber. All the advanced adaptive algorithms work satisfactorily under sudden dynamic load variations. The simulation and experimental results obtained are satisfactory and in agreement with each other.

# Chapter 06

# Performance Evaluation of MLI-based SAPF under Distorted Grid Conditions

## 6.0 Introduction

In the past, rotating generators played a dominant role in power system generation. These generators have a high moment of inertia and can withstand overvoltage/over current for longer than generators integrated with power electronics. Additionally, the penetration of the non-linear load was not substantial; hence the issue of power quality was not problematic. However, during the previous two decades, the situation has drastically shifted.

The use of power electronics converters for a distributed generation has expanded recently. The power electronic converters are used for various industrial applications in addition to power generation, such as motor drives, renewable energy integration, traction, and power quality conditioners. Before being integrated into the modern power system, these power electronic converters also require the correct grid parameter information, failing which they may seriously affect the grid's capability to operate and control. Frequency, amplitude, and phase angle information are required for grid-tied converter applications. This has encouraged researchers to look for the best algorithms that could deliver accurate information on these variables for successful grid synchronization. The synchronization unit plays a crucial role among the different controlling elements of the converters

Because non-linear loads and other electronic converters have affected the grid power quality, relying on conventional synchronization systems based on zero-crossing detection is no longer advisable. Several researchers have reported various methods to quickly and reliably estimate the grid parameters when the grid voltage is not ideal. This chapter discusses and analyzes a number of the frequently used single-phase PLL systems through MATLAB/Simulink models. Later, the following PLLs' performance was verified and tested experimentally under different grid abnormalities. The PLLs considered for the detailed study include:

1. Synchronous Reference Frame Theory (SRFT-PLL)
2. Sinusoidal Orthogonal Grid Integrator (SOGI-PLL)
3. Third Order Sinusoidal Integrator (TOSSI-PLL)

The following cases are considered to evaluate the performance of the PLLs:

*Case 1: Voltage sag and distorted grid*

*Case 2: Frequency variation*

*Case 3: DC –offset*

*Case 4: Phase Shift*

## 6.1 Synchronous Reference Frame Theory (SRFT-PLL)

The generalized block diagram of QSG-based SRFT-PLL is shown in Fig 6.1. It consists of estimated frequency ( $\hat{\omega}$), phase angle( $\hat{\theta}$ ), and normal grid frequency ( $\omega_{eff}$ ). The input grid voltage ( $v_g$ ) is phase-shifted $\frac{\pi}{2}$ to generate the orthogonal component $v_\beta$ for Park transformation. The grid voltage is assumed to be distorted and represented as

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sum_{h=-\infty, h\neq 0}^{h=\infty} V_h \begin{bmatrix} \cos(h\omega + \phi_h \\ \sin(h\omega + \phi_h \end{bmatrix} \tag{6.1}$$

where $v_h$ *and* $\phi_h$ represents the amplitude and phase angle of the harmonic components, respectively. After Park's transformation, the voltages have been described as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{6.2}$$

By using Equation 6.1 and 6.2, further the voltages can be represented as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sum_{h=-\infty, h\neq 0}^{h=\infty} V_h \cos(h\omega + \phi_h - \hat{\theta}) \\ \sum_{h=-\infty, h\neq 0}^{h=\infty} V_h \sin(h\omega + \phi_h - \hat{\theta} \end{bmatrix} \tag{6.3}$$

In case the grid is assumed to be distortion less or $\phi_1$ is smaller enough then , we can get

$$V_q = V_1 \sin(\omega + \phi_1 - \hat{\theta}) = V_1 \sin(\theta - \hat{\theta}) \tag{6.4}$$

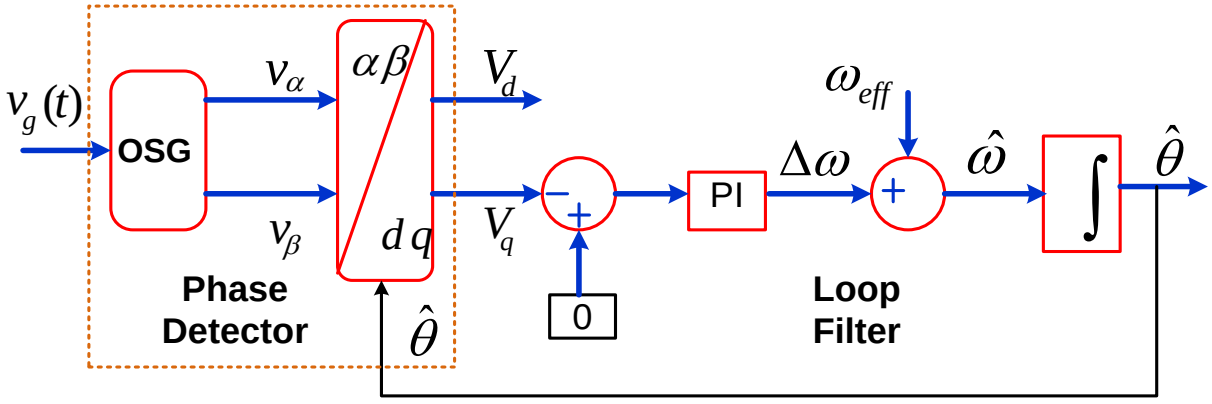



**Fig 6.1** Generalized block diagram of SRF-PLL

Equation 6.4 $\theta$ and $\hat{\theta}$ represents the actual and estimated phase angle, respectively. This can further be simplified when the phase difference is small, and it can be defined as

$$V_q = V_1(\theta - \hat{\theta}) \tag{6.5}$$

The objective of the SRF-PLL is to converge $V_q \to 0$ . To achieve this the transformed $V_q$ signal is fed to the loop filter where the PI controller generates an error signal $\Delta\omega$ , then further added to the normal grid frequency $\omega_{eff}$ then the estimated frequency ( $\hat{\omega}$ ) is obtained. The frequency signal $\hat{\omega}$ is fed to the voltage-controlled oscillator (VCO) to generate the phase angle $\hat{\theta}$ .

### 6.1.1 Simulation Results with SRF-PLL

The proposed system is tested by considering various abnormalities in the grid such as (i) phase shift of $90^o$ (ii) distorted grid (iii) 20% of voltage sag and swell (iv) 20% of DC offset component in the grid voltage

#### 6.1.1.1 Case I: Under distorted Grid and Voltage Sag

In this case the grid is considered to have voltage sag during $t_1$=0.1s to $t_2$=0.2s and distortion in grid voltage during $t_3$=0.35s to $t_4$=0.45s as shown in Fig 6.2. It is observed that the step change in amplitude signal (voltage sag is the present case) and also, in case of grid distortion, subsequent oscillations in peak to peak frequency of 2.2Hz can be visible. However, the SRF-PLL is able to estimate the phase angle correctly $\hat{\theta}$ .

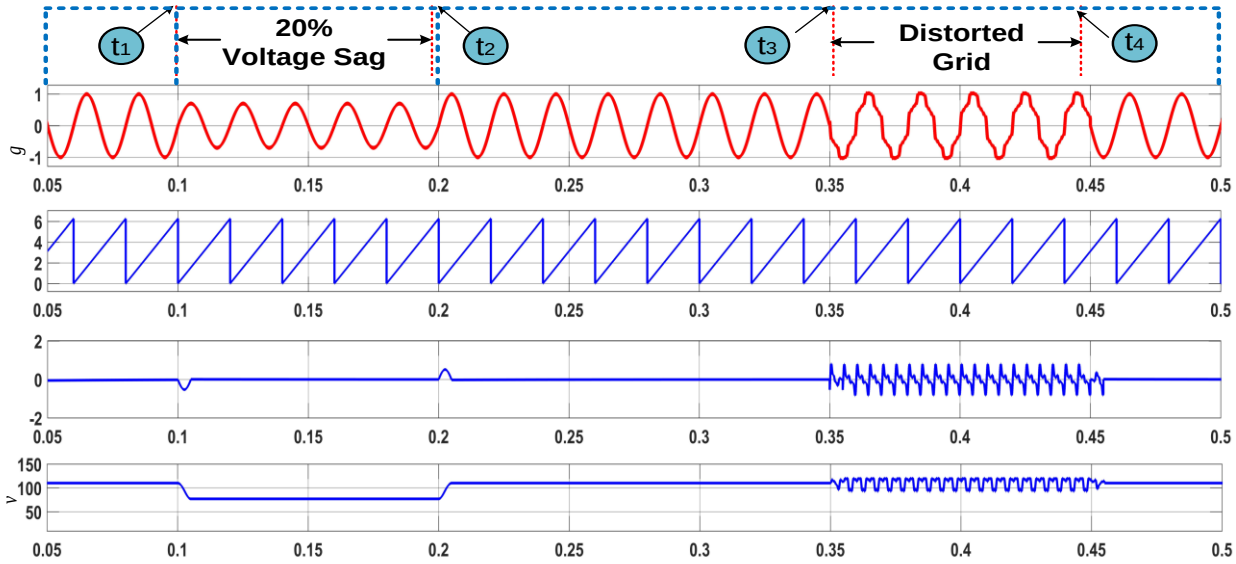



**Fig 6.2** Simulation performance of SRF-PLL under 20% voltage sag and distorted grid

(where, $v_g$ =per unit grid voltage, $\hat{\theta}$ = estimated phase angle, $\Delta f$ = $f_{est.}$ –$f_{act.}$ and $A_v$ = amplitude of grid voltage )

### 6.1.1.2 Case II: Phase Shift of $\pi/2$ and 20% DC-offset

In this case, the grid is considered to have phase shift during $t_1$=0.1s to $t_2$=0.2s and 20% of DC offset is added in grid during $t_3$=0.35s to $t_4$=0.45s as shown in Fig 6.3. It is observed from the Fig that the step change in phase angle of $90^o$ affects the frequency estimation drastically, and also, in the case of 20% DC –offset wide, oscillations can be visible. However, the SRF-PLL correctly estimates the phase angle $\hat{\theta}$ but cannot eliminate the DC –offset.

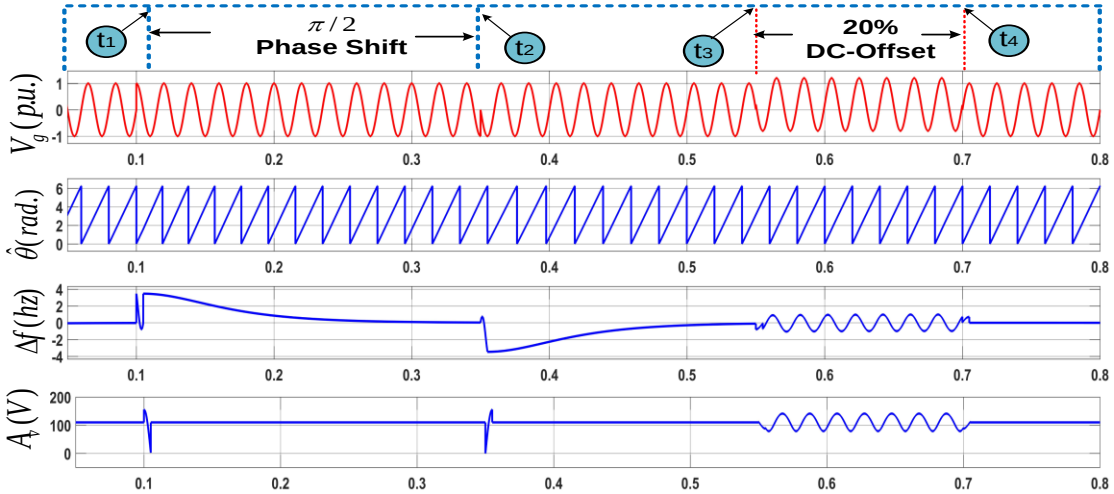



**Fig 6.3** Simulation performance of SRF-PLL under $\pi/2$ phase shift and 20% DC - Offset

### 6.1.2 Experimental Results with SRF-PLL

The behavior of different parameters of SRF-PLL is also tested experimentally. The system is tested considering various abnormalities in the grid such as (i) phase shift of $90^{o}$ (ii) distorted grid (iii) 20% of voltage sag and swell (iv) 20% of DC offset component in the grid voltage

#### 6.1.2.1 Case I: Distortion in Grid Voltage

It is clearly visible from experimental results from Fig 6.4 that under the distorted grid condition, the SRF-PLL can accurately track the phase angle $\hat{\theta}$ , but sustained oscillations are clearly seen in $\Delta f$ . The magnitude of these oscillations is near ± 2 Hz, and some oscillations are also observed in the amplitude $A_v$ (V) tracking under distorted grid conditions.

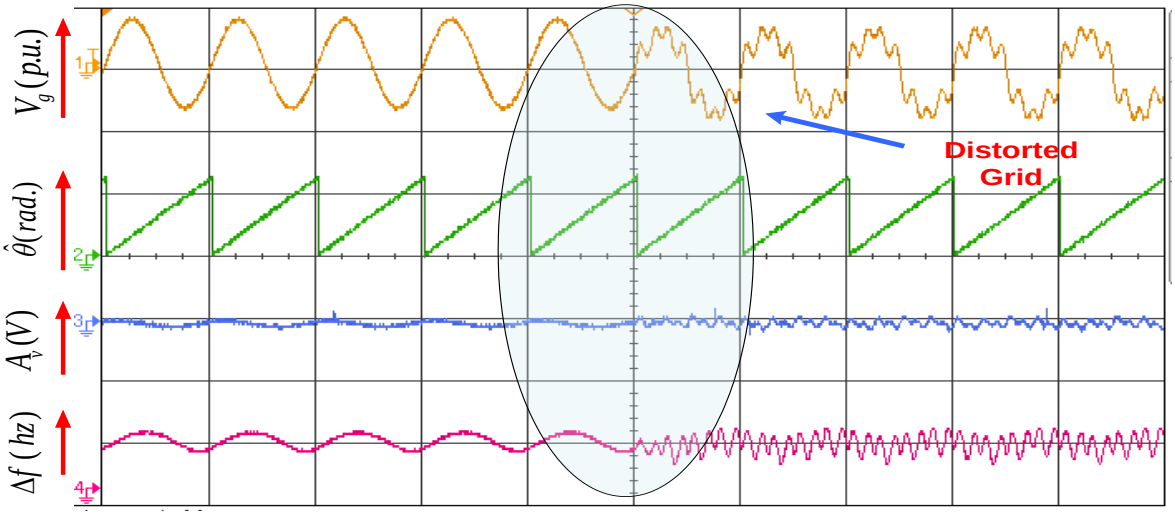



**Fig 6.4** Experimental performance of SRF-PLL under distorted grid conditions

Thus, it is clearly observed that SRF-PLL performance is satisfactory under normal grid conditions, but its performance deteriorates under the distorted grid and DC offset conditions.

#### 6.1.2.2 Case II: Phase Shift of $\pi/2$

Figure 6.5 (experimental findings) shows that the SRF-PLL accurately monitors the phase angle even when there is a phase shift of $\pi/2$ in the grid voltage condition. However, the huge deviation is readily obvious in frequency $\Delta f$ while there is minimal change in the

amplitude $A_V\,(V)$

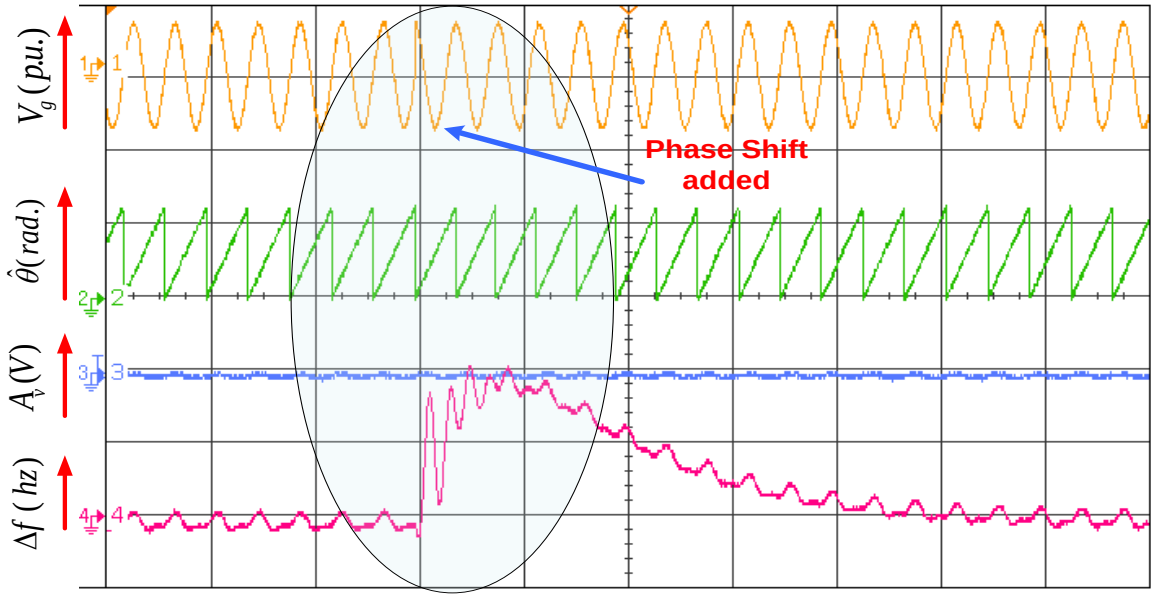



**Fig 6.5** Experimental performance of SRF-PLL under phase shift of $\pi/2$

### 6.1.2.3 Case III: DC-Offset

The SRF-PLL is tested by introducing a 20% DC offset in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$, but sustained oscillations are visible in $\Delta f$ and the amplitude $A_v$ (V), as shown in Fig 6.5.

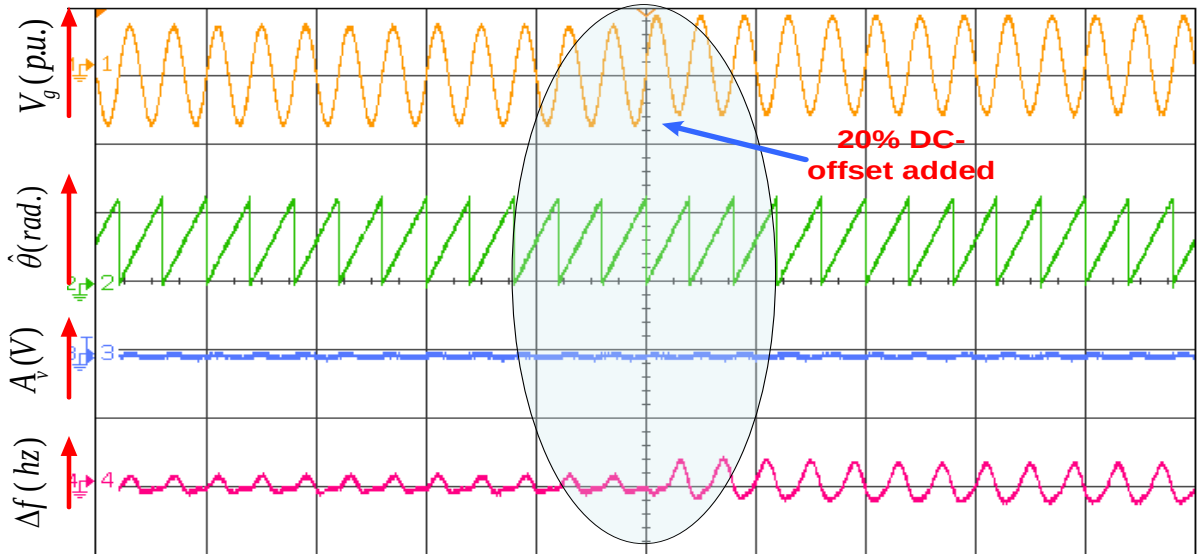



**Fig 6.6** Experimental performance of SRF-PLL under 20% DC-offset in grid voltage

### 6.1.2.4 Case IV: Voltage Sag and Swell

Now the SRF-PLL is tested under voltage sag/swell in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$ , but a significant deviation is visible in $\Delta f$ as well as in the amplitude $A_v$ (V) as shown in Fig 6.6.

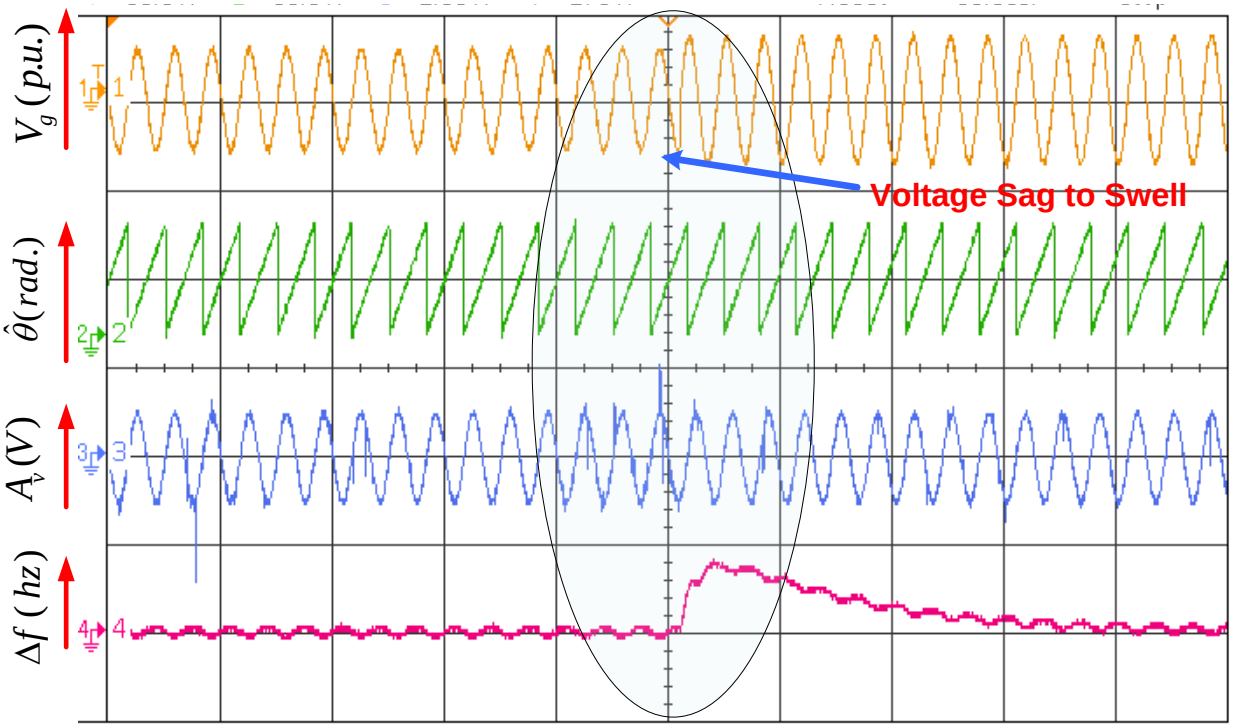



**Fig 6.7** Experimental performance of SRF-PLL under grid voltage variation from sag to swell

The SRF-PLL is tested under different test cases, viz. distorted grid, phase angle change of $\pi/2$ , voltage sag/swell, and DC offset conditions. The simulation and experimental results validate the findings. It is observed that the SRF-PLL works satisfactorily in normal grid conditions, but its performance deteriorates in abnormal grid conditions, especially in the case of DC offset grid conditions.

## 6.2 Second Order Generalized Integrator (SOGI-PLL)

The basic structure of SOGI-PLL block is depicted in Fig 6.8, where $v_g$ is the grid voltage is the grid frequency taken as $2\pi f$ rad/s in this paper and the estimated frequency and phase

angle is represented as $\omega_{est}$ and $\widehat{\theta}$. The SOGI-PLL blocks generate two signals, viz. an in-phase voltage signal $v_\alpha$ and quadrature signal $v_\beta$. The closed-loop transfer functions of the output signals are represented as $T_\alpha(s)$, and $T_\beta(s)$ in Equation 6.6 and Equation 6.7, where k stands for gain adjustment factor and the selected value is a trade-off between the filtering performance and response time.

$$T_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\omega_{est}s}{s^2 + k\omega_{est}s + \omega_{est}^2} \tag{6.6}$$

$$T_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k\omega^2_{est}}{s^2 + k\omega_{est}s + \omega_{est}^2} \tag{6.7}$$

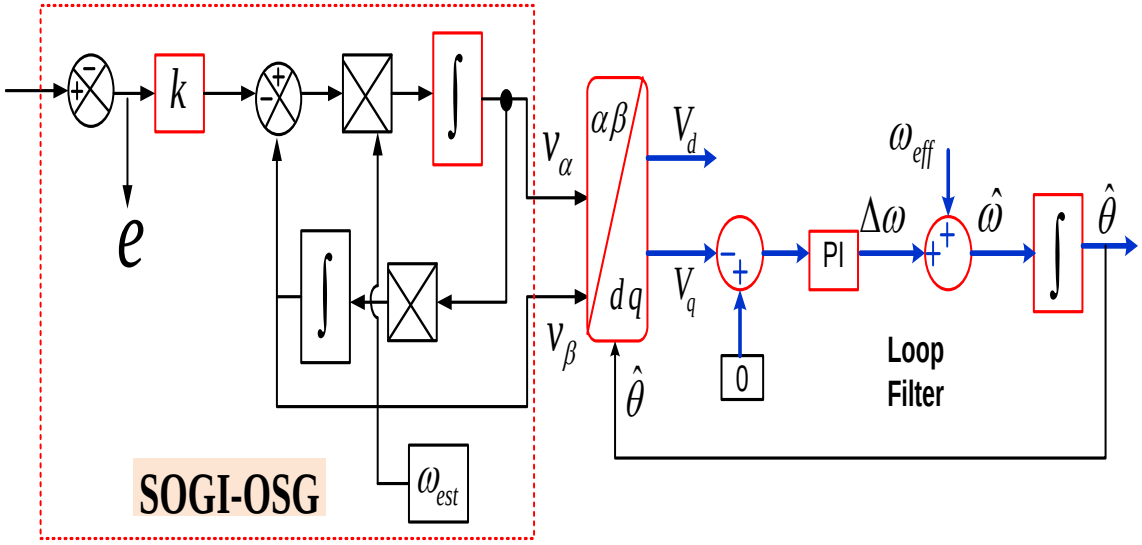
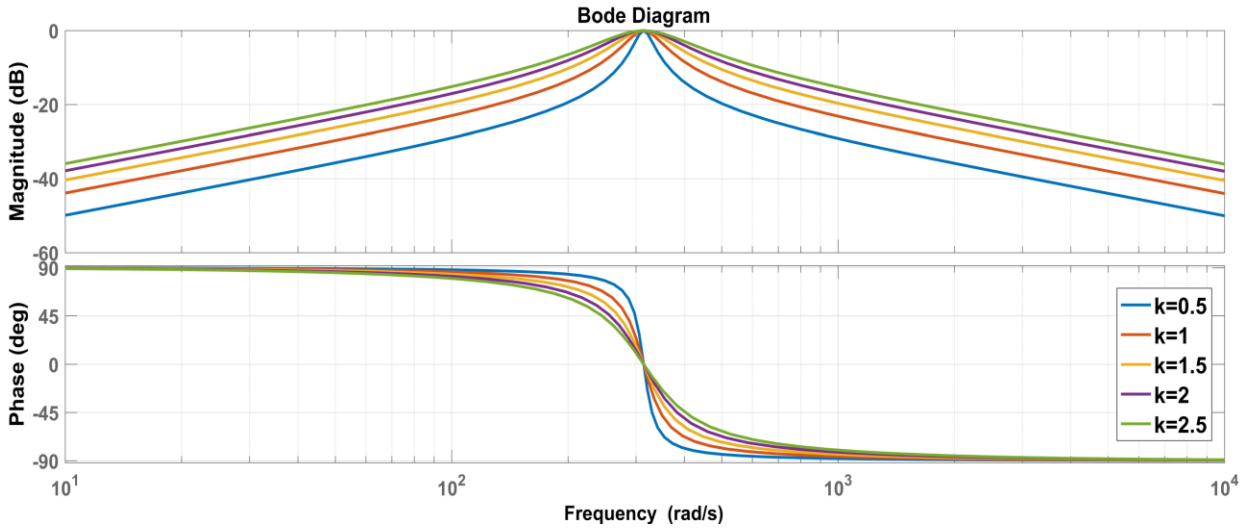
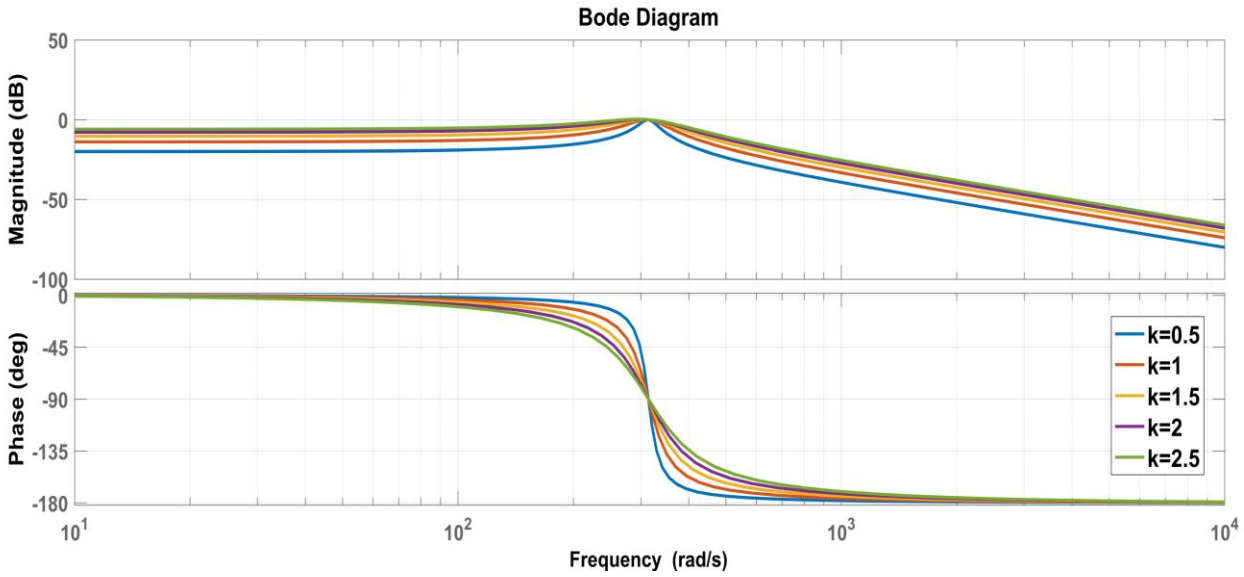



**Fig 6.8** Basic Structure of SOGI-PLL

Bode plots of the in-phase and quadrature SOGI-PLL transfer functions are shown in Fig 6.8(a-b) for different values gains (k). The Bode characteristics of $T_\alpha(s)$ show that it acts as a band pass filter, and the characteristics of $T_\beta(s)$ shows its behavior as a low pass filter with a phase shift of $90^o$ from the in-phase component. The transfer function gain k is varied from 1 to 2.5 with a step change of 0.5. The selected value of 1.5 is considered in the system where the SOGI-PLL gives optimal performance and quickly estimates the desired parameters.




(a)




(b)

**Fig 6.9** Bode plots for (a) In-phase component $T_\alpha(s)$ (b) Quadrature component $T_\beta(s)$

## 6.2.1 Simulation Results of SOGI-PLL

The SOGI-PLL is tested by considering various abnormalities in the grid such as (i) phase shift of $90^o$ (ii) distorted grid, (iii) 20% of voltage sag and swell (iv) 20% of DC offset component in the grid voltage

### 6.2.1.1 Case I: Grid Harmonics and Voltage Sag

In this case, the grid is considered to have a voltage sag of 0.2 pu during $t_1$=0.1s to $t_2$=0.2s and distortion in grid voltage during $t_3$=0.35s to $t_4$=0.45s, as shown in Fig 6.10. As observed from the Fig, the step change in amplitude signal (voltage sag is the present case) the amplitude variation is less, i.e., settles within two cycles. Likewise, in the case of grid distortion or harmonics, the subsequent fewer oscillations in the peak-to-peak frequency of 0.4Hz and peak-to-peak amplitude is 8.5V less than SRF-PLL, which can be visible in Fig 6.10. However, the SOGI-PLL correctly estimated the phase angle $\hat{\theta}$.

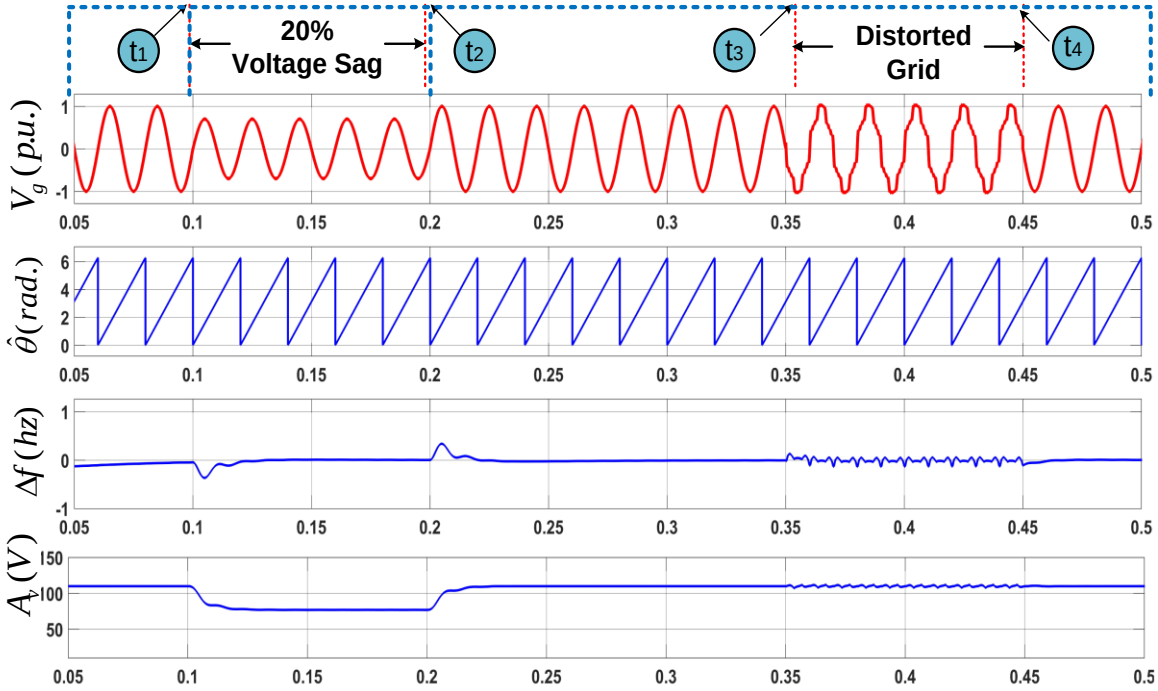



**Fig 6.10** Simulation performance of SOGI-PLL under 20% voltage sag and distorted Grid

### 6.2.1.2 Case II: Phase Shift of $\pi/2$ and 20% DC-offset

In this case, the grid is simulated to have a phase shift of $\pi/2$ from $t_1$=0.1s to $t_2$=0.2s, and 20% of DC offset is added in grid voltage during $t_3$=0.35s to $t_4$=0.45s, as shown in Fig 6.11. As the Fig shows, the step change in phase angle of $90^o$ affects the frequency estimation. A sharp overshoot and undershoot are marked in amplitude estimation (peak to peak) with a magnitude of 105V, and the settling time is 22ms under this distortion. Now

also, in the case of 20% DC –offset wide, oscillations can be visible with a peak-to-peak frequency of 6Hz and peak-to-peak oscillation in amplitude is 185.6V. These results clearly indicate that the performance of SOGI-PLL is good under harmonics in the grid or even in voltage sag or swell conditions but its performance deteriorates in case of DC-offset and phase-shift. Thus, the SOGI-PLL correctly estimated the phase angle $\hat{\theta}$ but could not eliminate the DC –offset.

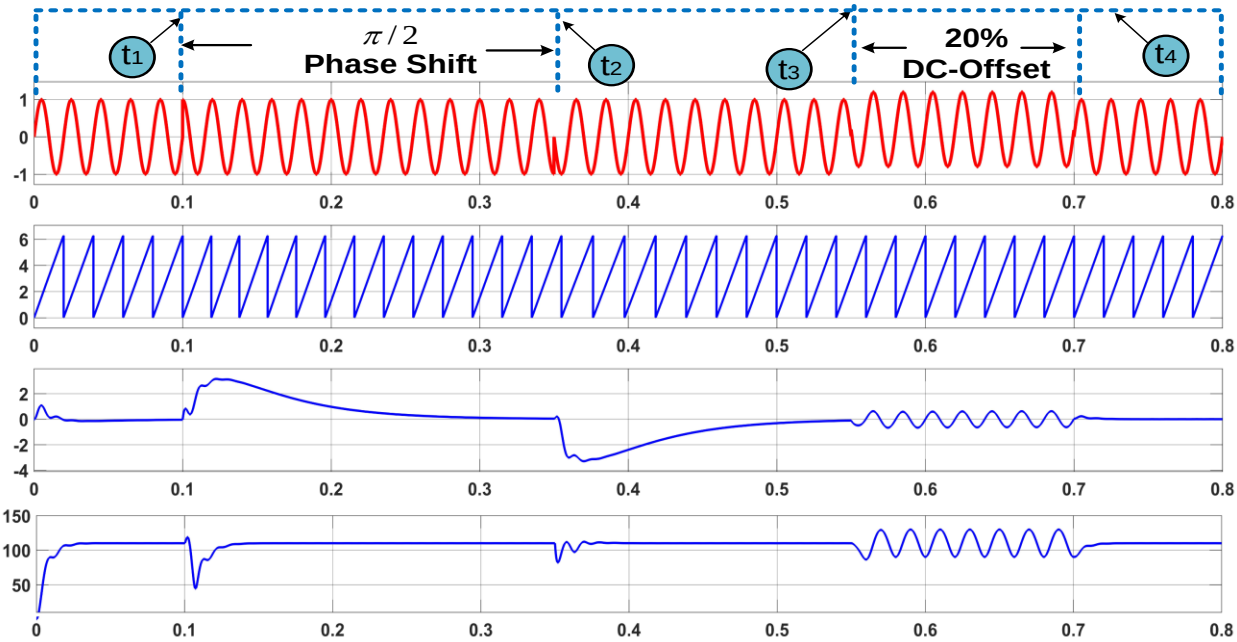



**Fig 6.11** Simulation performance of SOGI-PLL under $\pi/2$ phase shift and 20% DC - Offset

## 6.2.2 Experimental Results of SOGI-PLL

The performance of SOGI-PLL is also tested experimentally under varied test cases. The system is tested considering various abnormalities in the grid such as (i) phase shift of $90^{o}$ (ii) distorted grid (iii) 20% of voltage sag and swell (iv) 20% of DC offset component in the grid voltage

### 6.2.2.1 Case I: Distortion in Grid Voltage

It is clearly observed from the experimental results from Fig 6.12 that under distorted grid condition, the SOGI-PLL accurately track the phase angle $\hat{\theta}$ but sustained oscillations are seen in $\Delta f$ nearly of ± 2 Hz, and some fluctuations are also seen in the amplitude $A_v$ (V) .

### 6.2.2.2 Case II: Distortion in Phase Shift of $\pi/2$

It is observed from Fig 6.13 experimental results that under phase shift $\pi/2$ in the grid voltage condition, the SOGI-PLL accurately tracks the phase angle $\hat{\theta}$ but the significant deviation is visible in $\Delta f$ and in the amplitude $A_v$ (V).

### 6.2.2.3 Case III: DC-Offset

The SOGI-PLL is tested by introducing a 20% DC offset in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$ , but large oscillations are visible in $\Delta f$ and the amplitude $A_v$ (V) as shown in Fig 6.14. Its performance deteriorates in this condition.

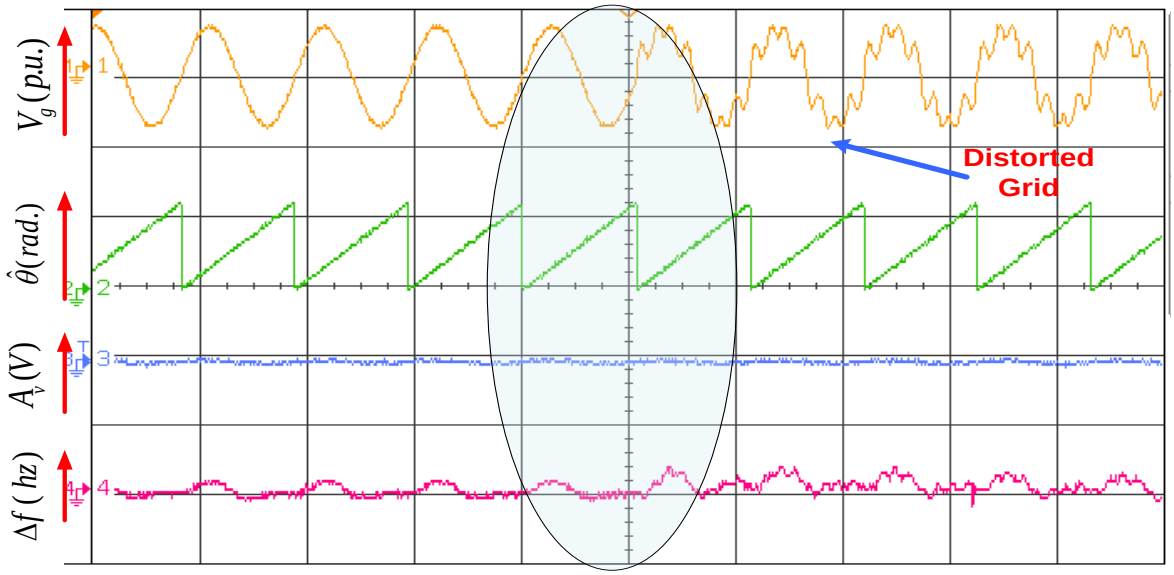



**Fig 6.12** Experimental performance of SOGI-PLL under distorted grid conditions

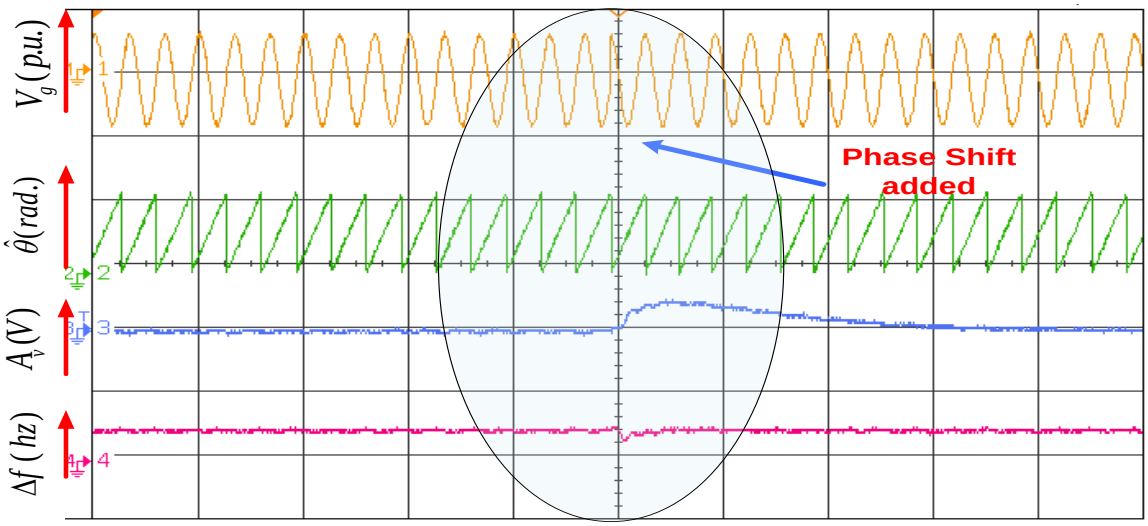



**Fig 6.13** Experimental performance of SOGI-PLL under phase shift of $\pi/2$

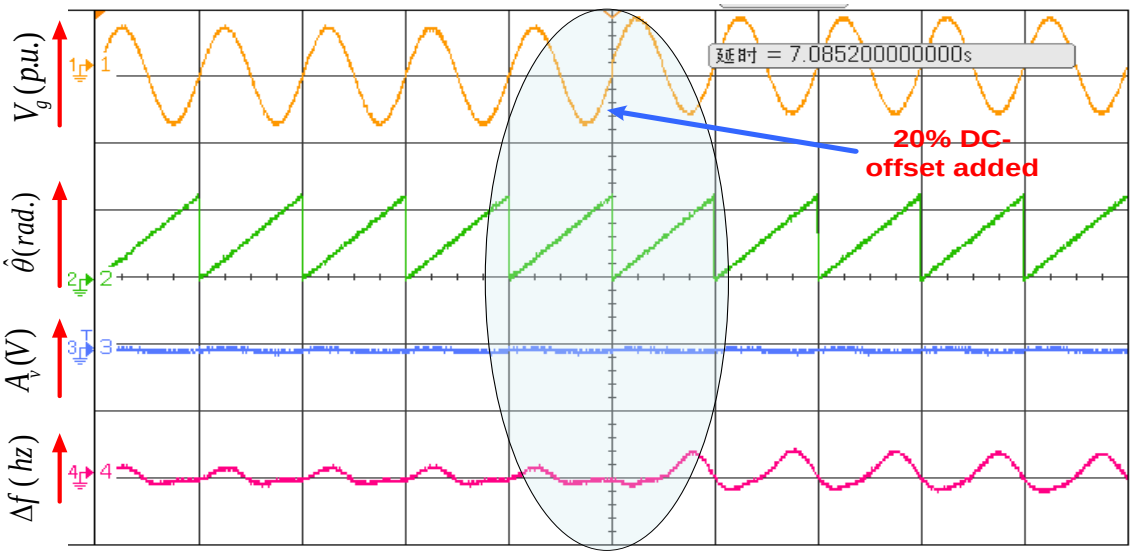



**Fig 6.14** Experimental performance of SOGI-PLL under 20% DC-offset in grid voltage

### 6.2.2.4 Case IV: Voltage Sag and Swell

Now the SOGI-PLL is tested with voltage sag/swell in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$ , but a significant deviation is clearly visible in $\Delta f$ and has little effect on amplitude $A_v$ (V), as shown in Fig 6.15

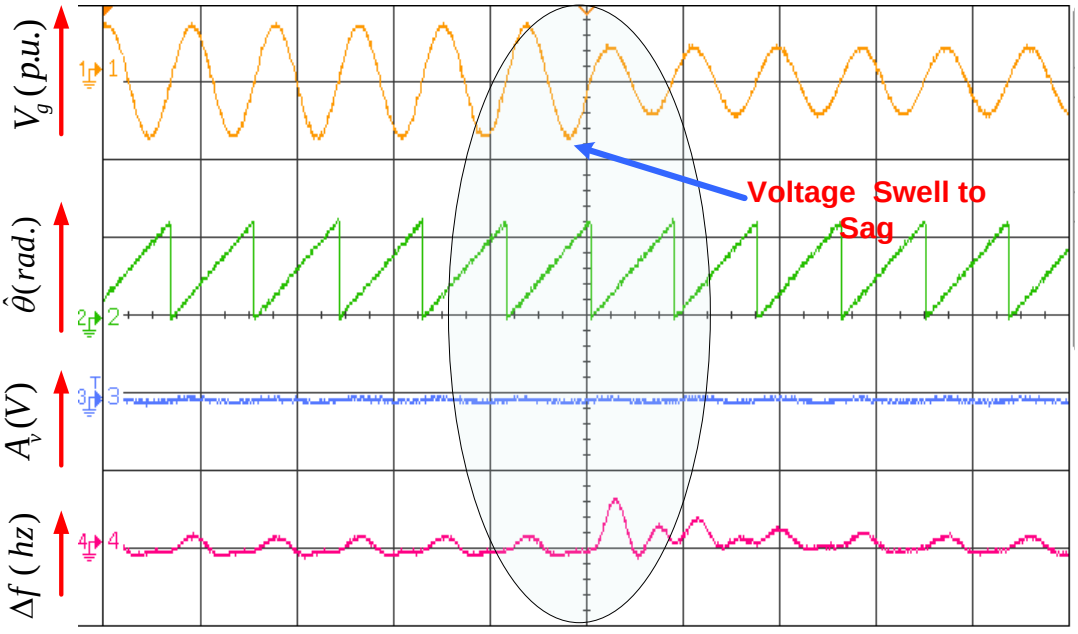



**Fig 6.15** Experimental performance of SOGI-PLL under grid voltage variation from swell to sag

The SOGI-PLL is tested both in simulation and experimentally. Results show that the SOGI –PLL performs better than SRF-PLL because the oscillation, overshoot, or undershoot and settling time with SOGI-PLL are lower than SRF-PLL. However, SOGI-PLL is highly dependent on the choice of gain parameters(k). It is observed that the SOGI-PLL works satisfactorily in normal grid conditions, but its performance deteriorates in abnormal grid conditions, especially in the case of DC offset and phase shift.

## 6.3 Third-Order Sinusoidal Integrator (TOSSI-PLL)

The generalized block diagram of the TOSSI algorithm is shown in Fig 6.16. It contains two orthogonal signals for each $90^0$ phase shift, and this happens when the resonant frequency ($\omega_n$) is equal to the supply frequency ($\omega_s$). The closed-loop transfer function of the TOSSI algorithm can be obtained using the MASON Gain formula given as follows

$$T_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{\alpha_1 \omega_n^2 s}{s^3 + \alpha_2 \omega_n s^2 + (\alpha_1 + 1)\omega_n^2 s + \alpha_2 \omega_n^3} \tag{6.8}$$

$$T_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{\alpha_1 \omega_n^3}{s^3 + \alpha_2 \omega_n s^2 + (\alpha_1 + 1)\omega_n^2 s + \alpha_2 \omega_n^3} \tag{6.9}$$

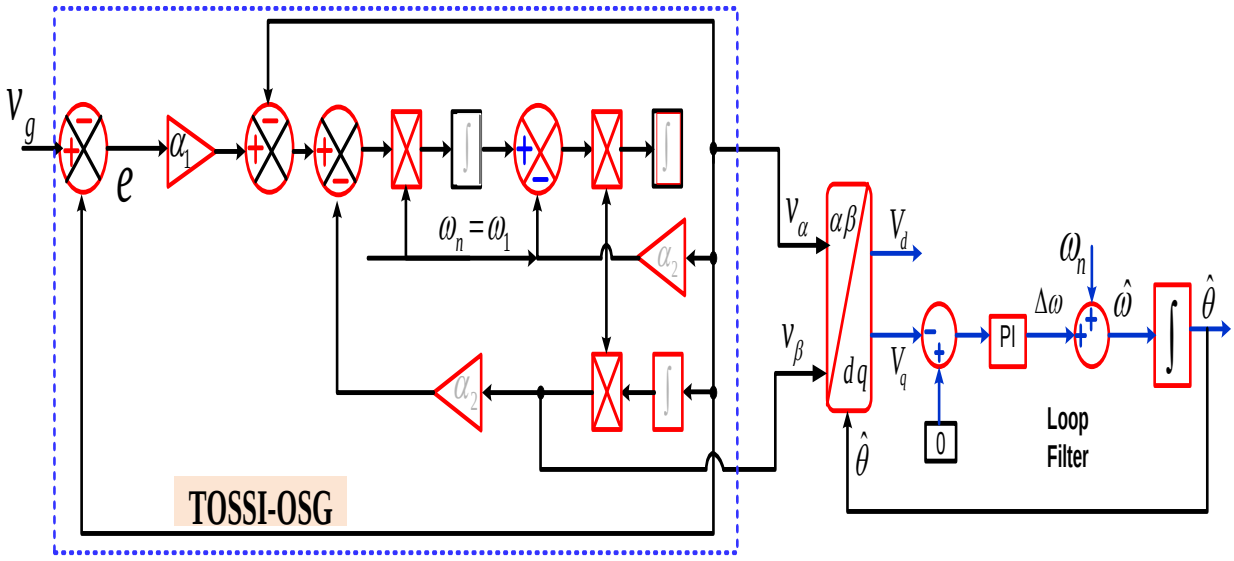



**Fig 6.16** Generalized Block diagram of TOSSI-PLL

From Equation 6.8 and Equation 6.9, the natural frequency of TOSSI ($\omega_n$) is set to the fundamental frequency of the grid to extract the fundamental component of frequency from grid voltage or current. It is also seen that there are two design variables, $\alpha_1$, and $\alpha_2$. These parameters control the system's bandwidth and influence the output response. There is a trade-off to choosing the accurate values of these parameters so that the desired level of damping is achieved and the system can perform dynamically. The damping factor of $\zeta$=0.707 is selected. The parameter $\alpha_1$ is set to 2.5, and in case of distorted grid voltage and current conditions, the value of $\alpha_1$ is set to be less than 2.5. Once the $\alpha_1$ is set, the value of $\alpha_2$ is tuned for fast dynamic performance. The Bode plot analysis of the transfer function of the TOSSI algorithm is shown in Fig 6.17 for $\omega_n$= 314 rad/sec. The plot considers the variation of the parameter $\alpha_2$ from 0 to 1. The Bode characteristics of the transfer function $T_\alpha(s)$ act as a bandpass filter, and the characteristics of $T_\beta(s)$ is shown in Fig 6.1 behave as a low pass filter with a phase shift of 90$^o$ of an in-phase component

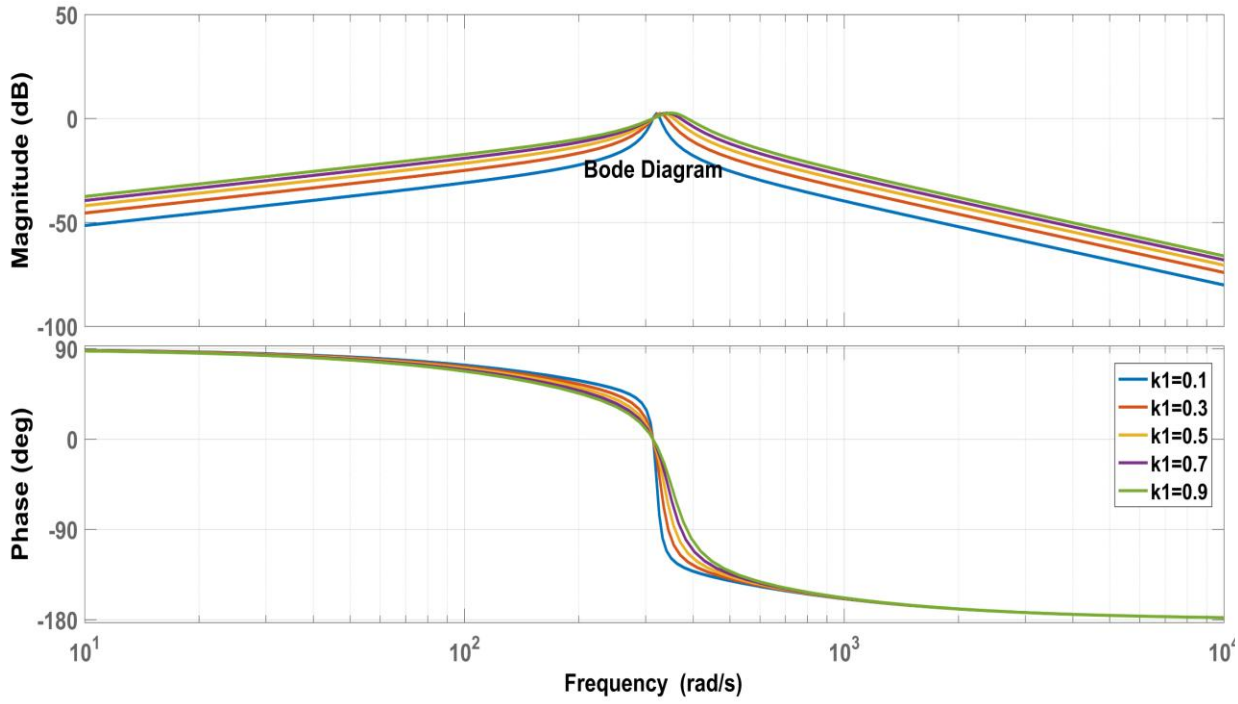



**Fig 6.17** Bode plot of TOSSI –PLL for in-phase component $T_\alpha(s)$

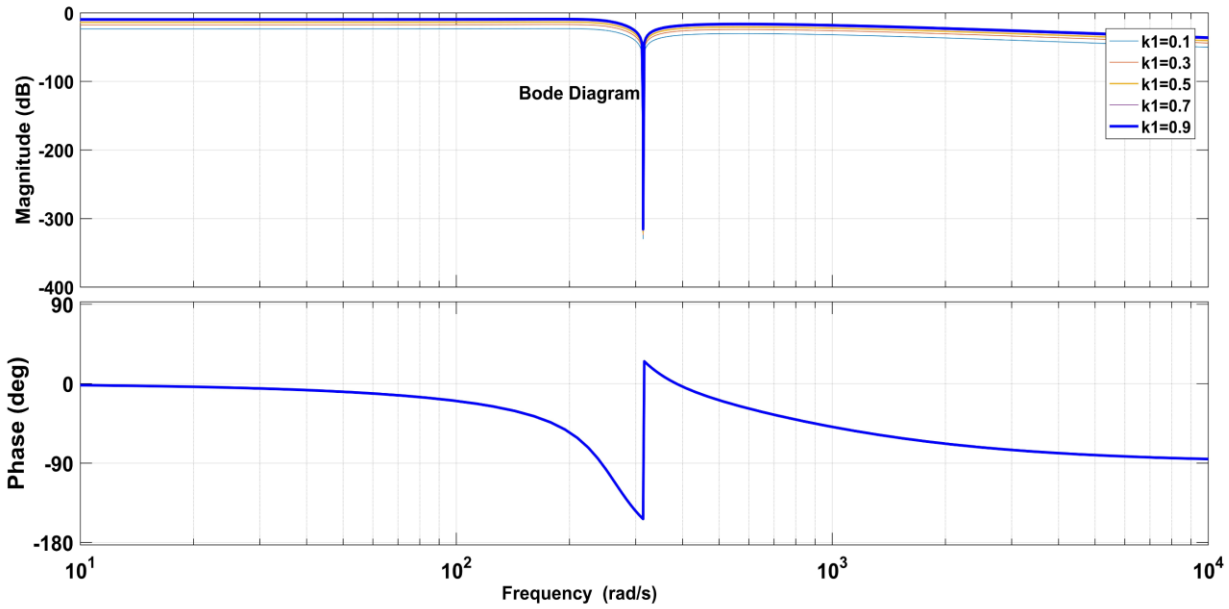



**Fig 6.18** Bode plot of TOSSI –PLL for quadrature component $T_{\beta}(s)$

### 6.3.1 Simulation Results with TOSSI-PLL

The TOSSI-PLL is tested by considering various abnormalities in the grid, such as (i) phase change of $\pi/2$ (ii) harmonics in the grid, (iii) voltage sag and swell, and (iv) 20% of DC offset in the grid voltage

#### 6.3.1.1 Case I: Grid harmonics and Voltage Sag

In this case, the grid is considered to have a voltage sag of 0.2 pu during $t_1$=0.1s to $t_2$=0.2s and distortion in grid voltage during $t_3$=0.35s to $t_4$=0.45s as shown in Fig 6.19. Fig 6.19 shows that the step change in amplitude signal (voltage sag), then the frequency and amplitude response are good, and both take less than 1~2 cycles to reach a steady state with the least deviation. Similarly, in the case of grid distortion least oscillations can be visible in $\Delta f$ & $A_{vpp}$ (V). Thus, the TOSSI-PLL correctly estimates the phase angle $\hat{\theta}$ under distorted grid condition.

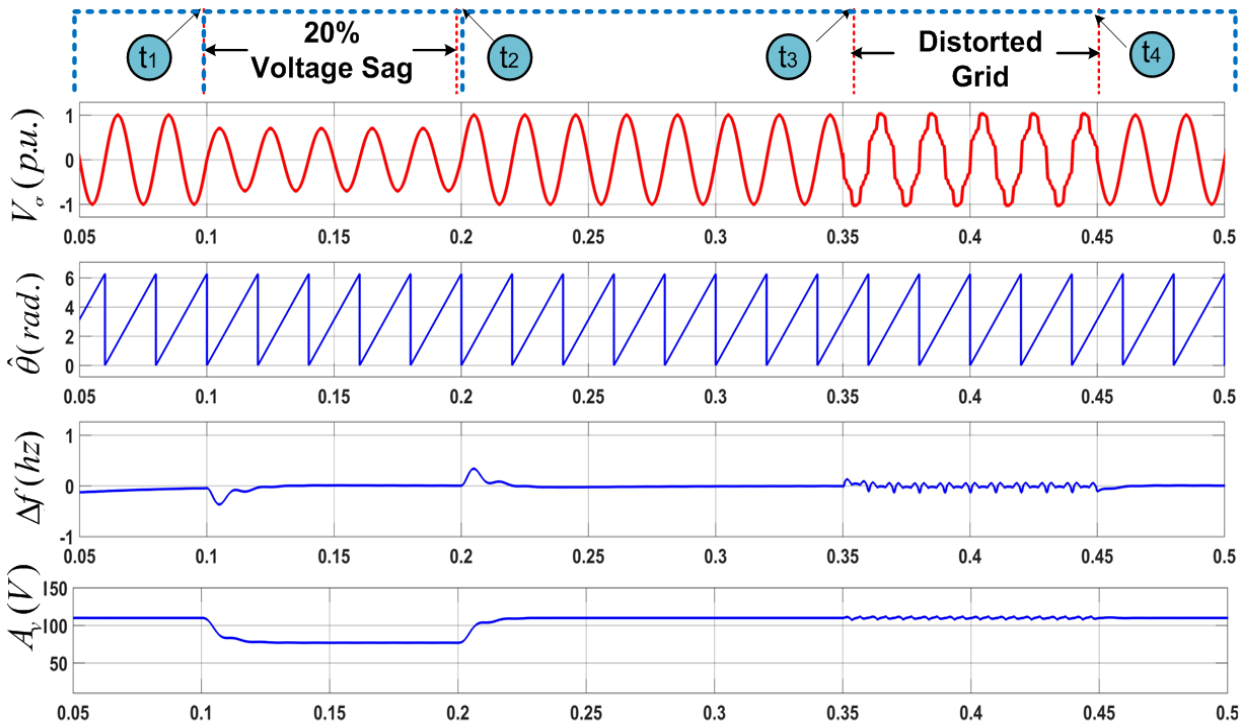



**Fig 6.19** Simulation performance of TOSSI-PLL under 20% voltage sag and distorted Grid

### 6.3.1.2 Case II: Phase Shift of $\pi/2$ and 20% DC-offset

In this case, a sudden phase shift $\pi/2$ is considered in grid voltage during $t_1$=0.1s to $t_2$=0.2s, and 20% of DC offset is added in the grid during $t_3$=0.35s to $t_4$=0.45s as shown in Fig 6.20. As seen from the Fig, the step change in phase angle of $90^{o,}$ like other PLLs in TOSSI-PLL, also shows the peak-to-peak frequency overshoot and undershoot and very least in the case of peak to peak to peak amplitude $A_{vpp}$(V) was observed. During the case of 20% DC –offset the oscillations seen in $\Delta f$ and $A_{vpp}$(V) is least among SRF-PLL and SOGI-PLL. However, the TOSSI-PLL correctly estimates the phase angle $\hat{\theta}$ but can handle the DC –offset.

## 6.3.2 Experimental Results with TOSSI-PLL

The behavior of different parameters of TOSSI-PLL is also tested experimentally. The system is tested considering various abnormalities in the grid such as (i) phase change of $90^o$, (ii) distorted grid, (iii) voltage sag/swell, (iv) 20% of DC offset in the grid voltage

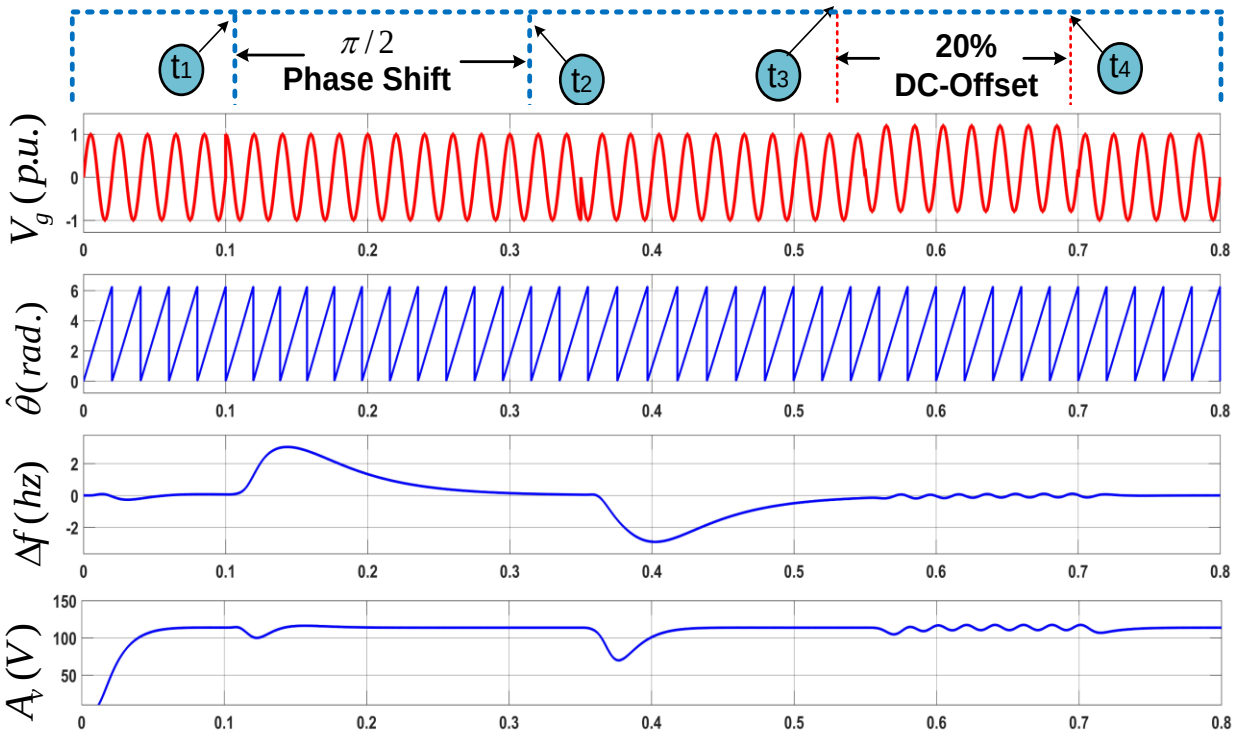



**Fig 6.20** Simulation performance of SOGI-PLL under $\pi/2$ phase shift and 20% DC - Offset

### 6.3.2.1 Case I: Distortion in Grid Voltage

It is visible from Fig 6.21 that under distorted grid condition, the TOSSI-PLL accurately track the phase angle $\hat{\theta}$ , but the least oscillations are seen in $\Delta f$ tracking. The fluctuations are near to ± 1 Hz, and almost zero oscillations are seen in the amplitude $A_v$ (V).

### 6.3.2.2 Case II: Phase Shift of $\pi/2$

It is seen from Fig 6.22 experimental results that under phase shift of $\pi/2$ in the grid voltage condition, the TOSSI-PLL accurately tracks the phase angle $\hat{\theta}$ , but the measurable deviation is clearly visible in $\Delta f$ . However, the least effect is seen in the tracked amplitude (V) compared to other PLL algorithms such as SRFT-PLL and SOGI-PLL considered in this chapter.

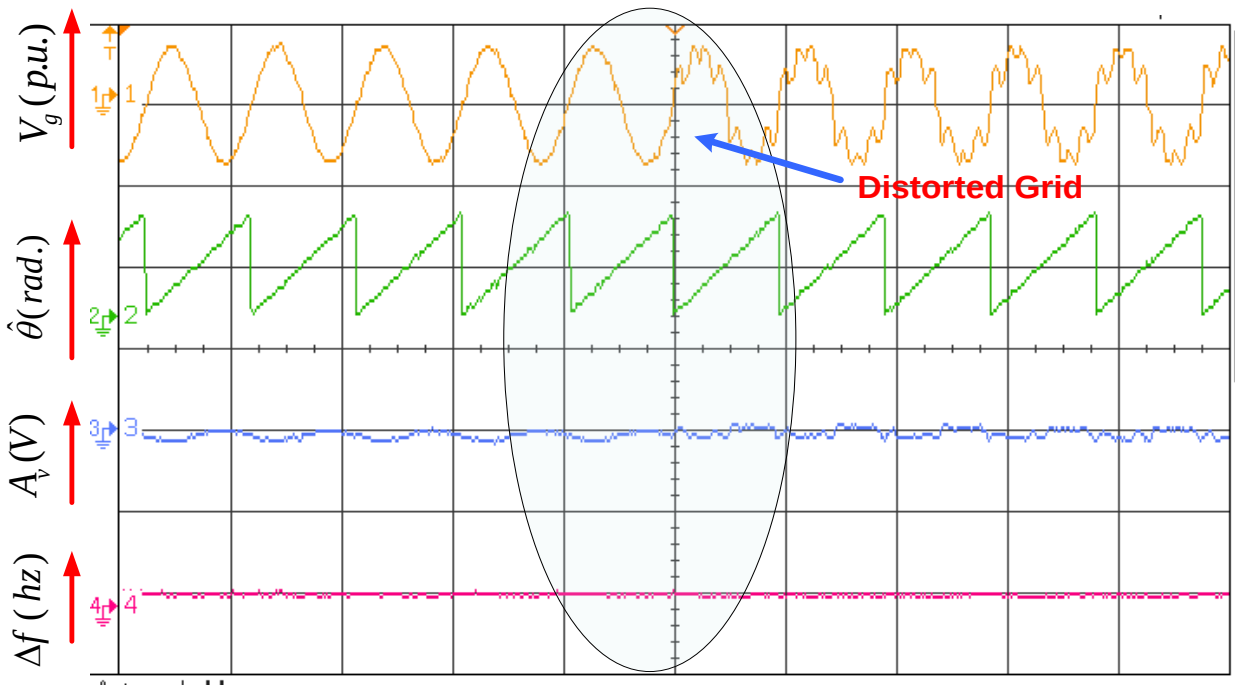



**Fig 6.21** Experimental performance of TOSSI-PLL under distorted grid conditions

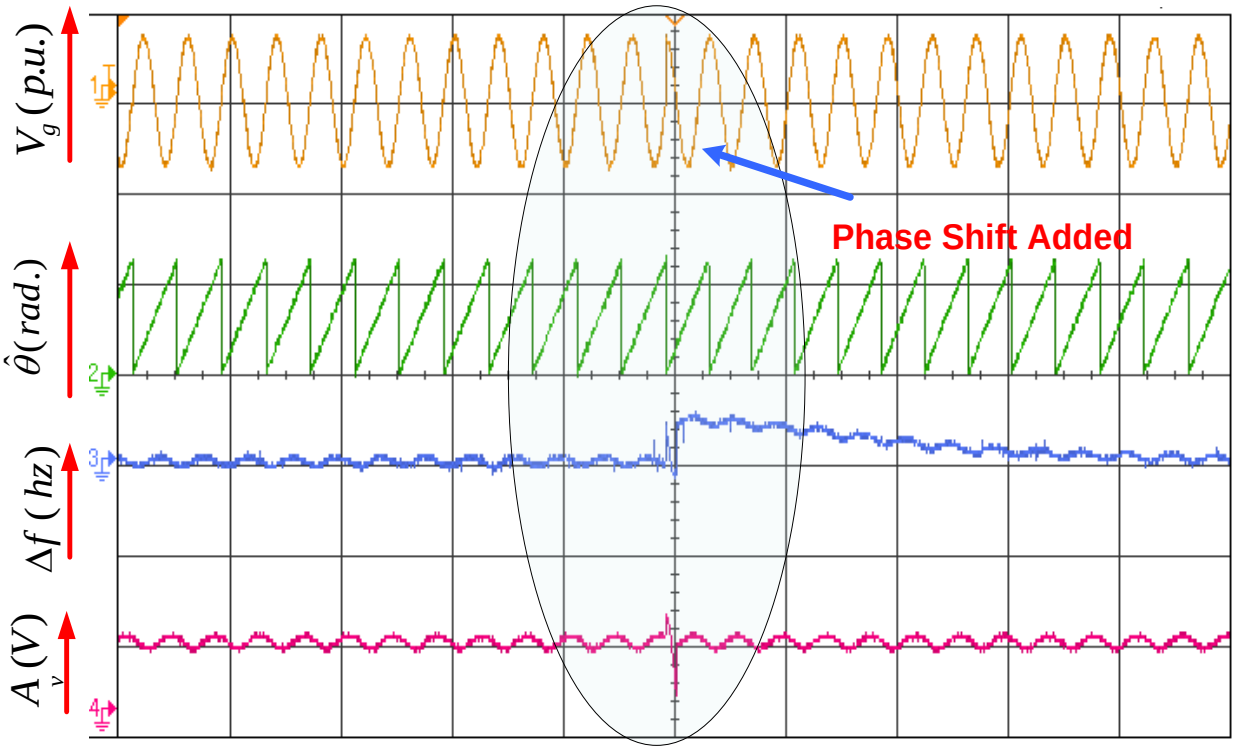



**Fig 6.22** Experimental performance of TOSSI-PLL under phase shift of $\pi/2$

### 6.3.2.3 Case III: DC-Offset

The TOSSI-PLL is tested by introducing a 20% DC offset in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$ , but the very low oscillations are visible in $\Delta f$ the amplitude $A_v$ (V), as shown in Fig 6.23.

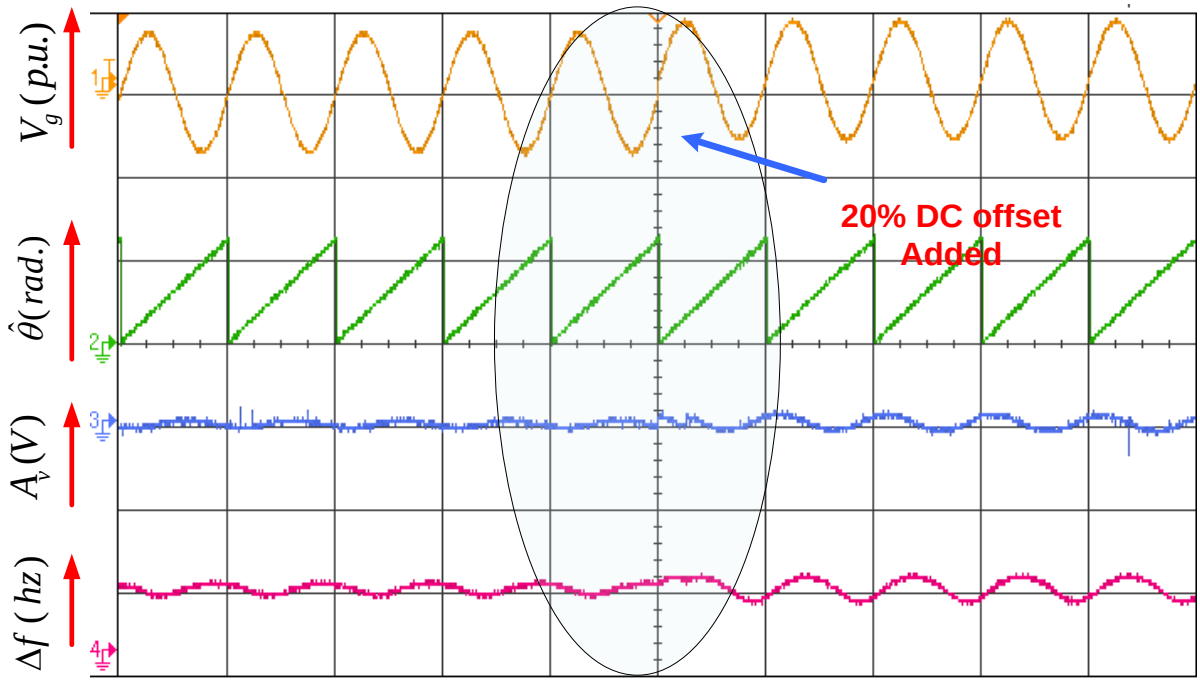



**Fig 6.23** Experimental performance of TOSSI-PLL under 20% DC-offset in grid voltage

### 6.3.2.4 Case IV: Voltage Sag and Swell

Now, the TOSSI-PLL is tested with voltage sag/swell in the grid voltage. In this case, also PLL accurately tracks the phase angle $\hat{\theta}$ , but small oscillations are visible in $\Delta f$ , but almost zero fluctuations in amplitude $A_v$ (V) are observed during voltage sag/swell, as shown in Fig 6.24.

The TOSSI-PLL is tested both in simulation and experimentally. It is observed that the TOSSI-PLL not only works satisfactorily in normal grid conditions but also performs satisfactorily under various grid abnormalities.

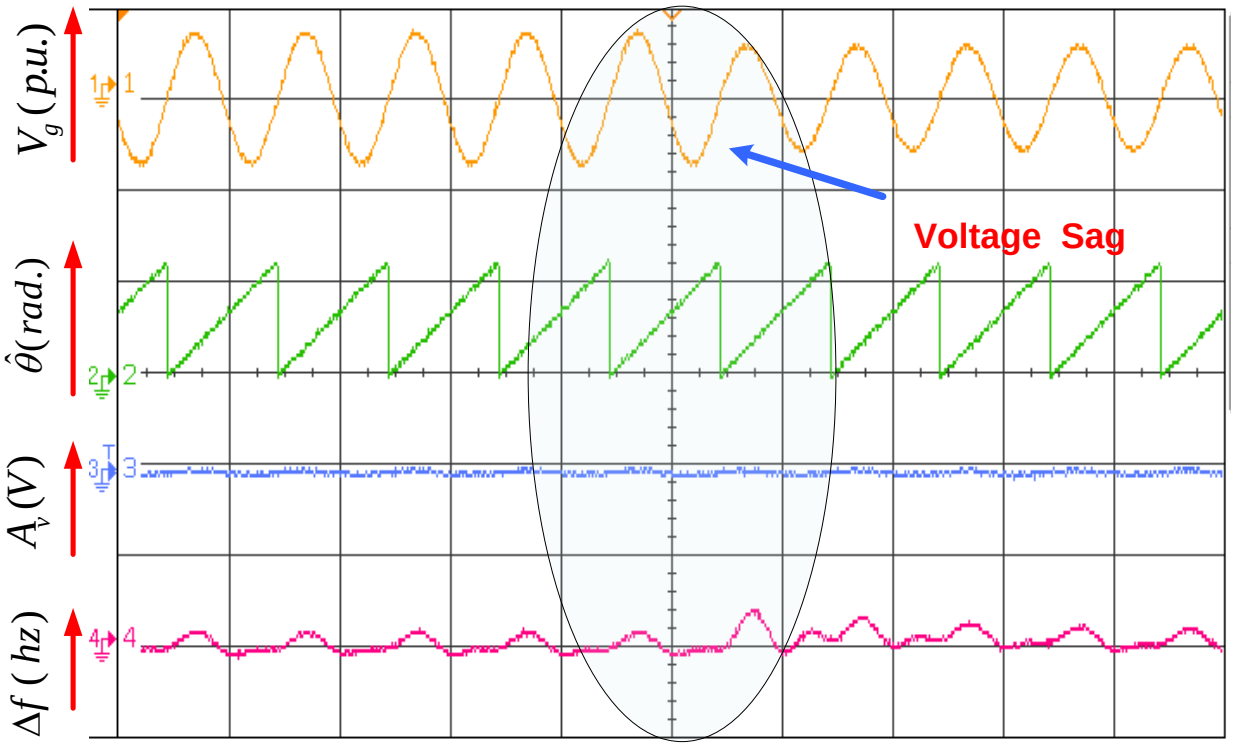



**Fig 6.24** Experimental performance of TOSSI-PLL under grid voltage variation from Swell to Sag

## 6.4 Comparison of SRF-PLL, SOGI-PLL, and TOSSI-PLL

The performance of SRF-PLL, SOGI-PLL, and TOSSI-PLL are compared under various distortions in the grid voltage. The main objective of these PLLs is to generate the perfect synchronizing signal from the input signal under abnormal grid voltage conditions. It is observed from Fig 6.25 to Fig 6.28 that the SRF-PLL filter performs poorly in grid distortion and DC offset conditions. SOGI-PLL works satisfactorily in harmonic distortion of gird voltage, but its performance deteriorates in case of phase shift and DC offset. On the other hand, the TOSSI-PLL performs better than SRF-PLL and SOGI-PLL. It is observed that the variation in frequency and amplitude of grid voltage under DC-offset shows the

least oscillations in TOSSI-PLL, as shown in simulation and experimental results. It has outstanding frequency tracking capability, the most negligible oscillations, and quick estimation of signals under different dynamic conditions, and it is easy to implement. However, the TOSSI-PLL suffers from a delay in the response during grid variations.

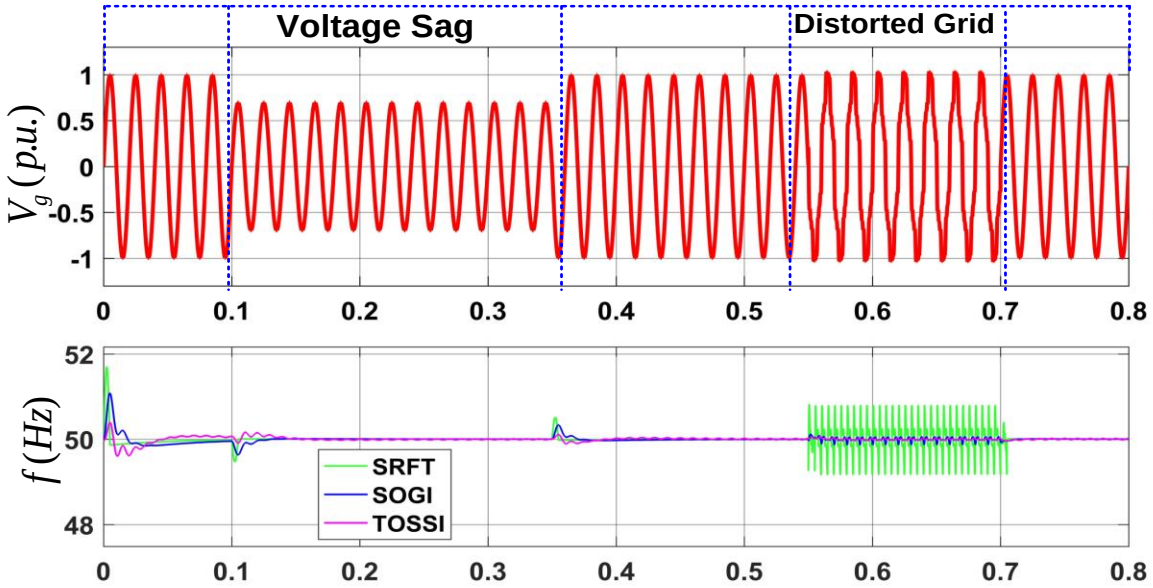



**Fig 6.25** Frequency Variation of SRF-PLL, SOGI-PLL & TOSSI-PLL under voltage sag/swell and distorted grid

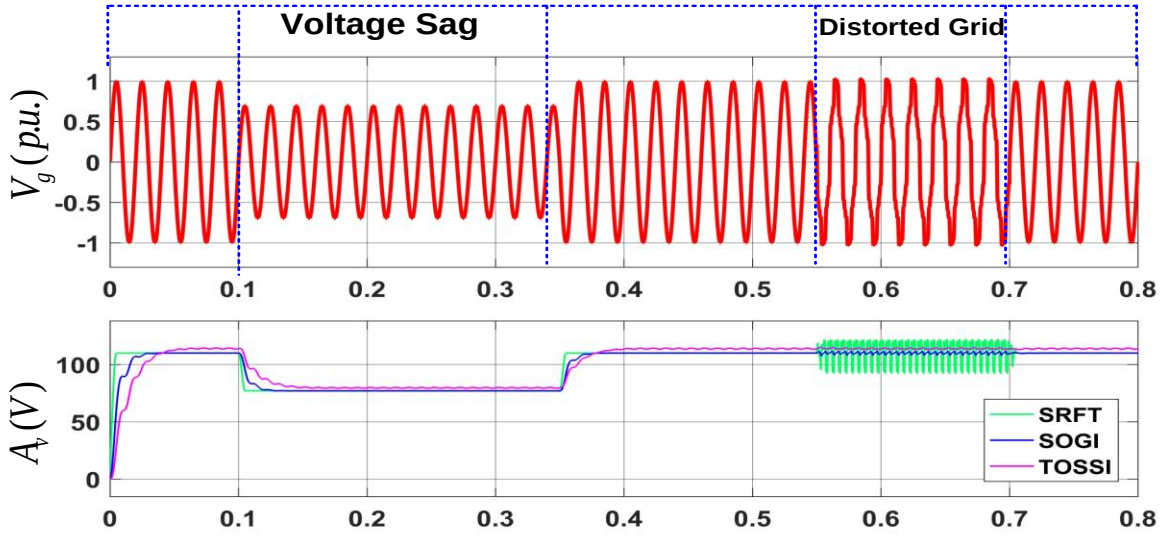



**Fig 6.26** Amplitude Variation of SRF-PLL, SOGI-PLL & TOSSI-PLL under voltage sag/swell and distorted grid

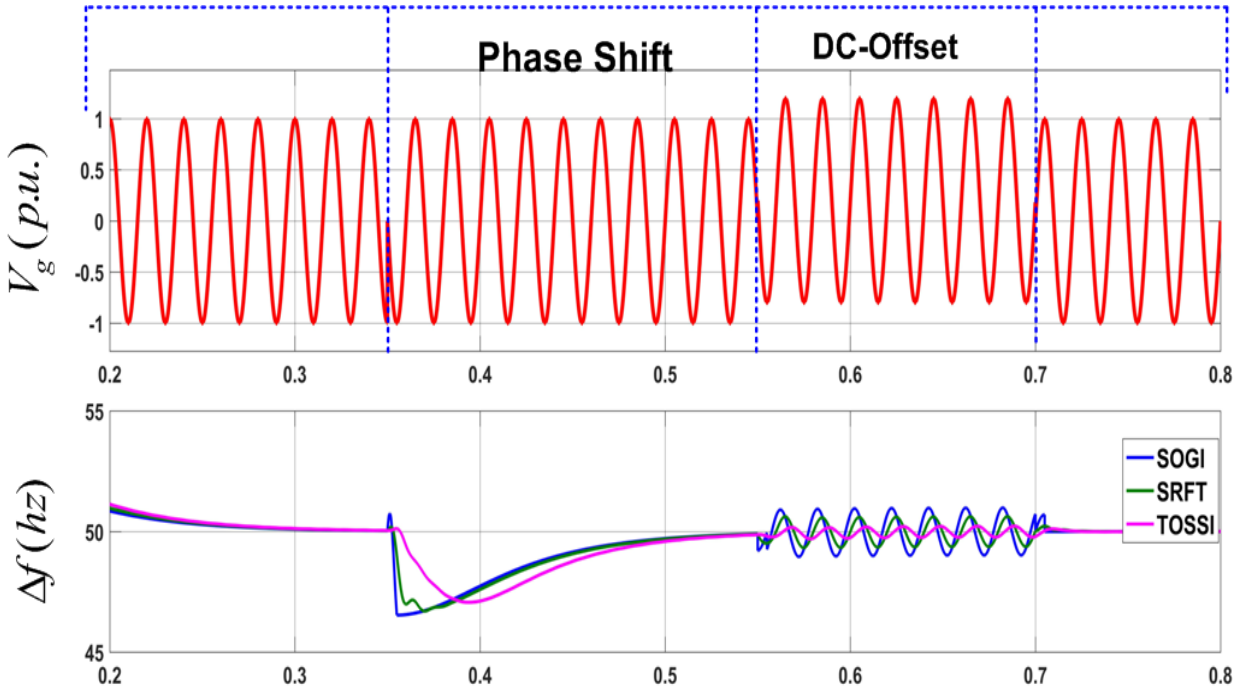



**Fig 6.27** Frequency Variation of SRF-PLL, SOGI-PLL & TOSSI-PLL under phase shift and DC-offset

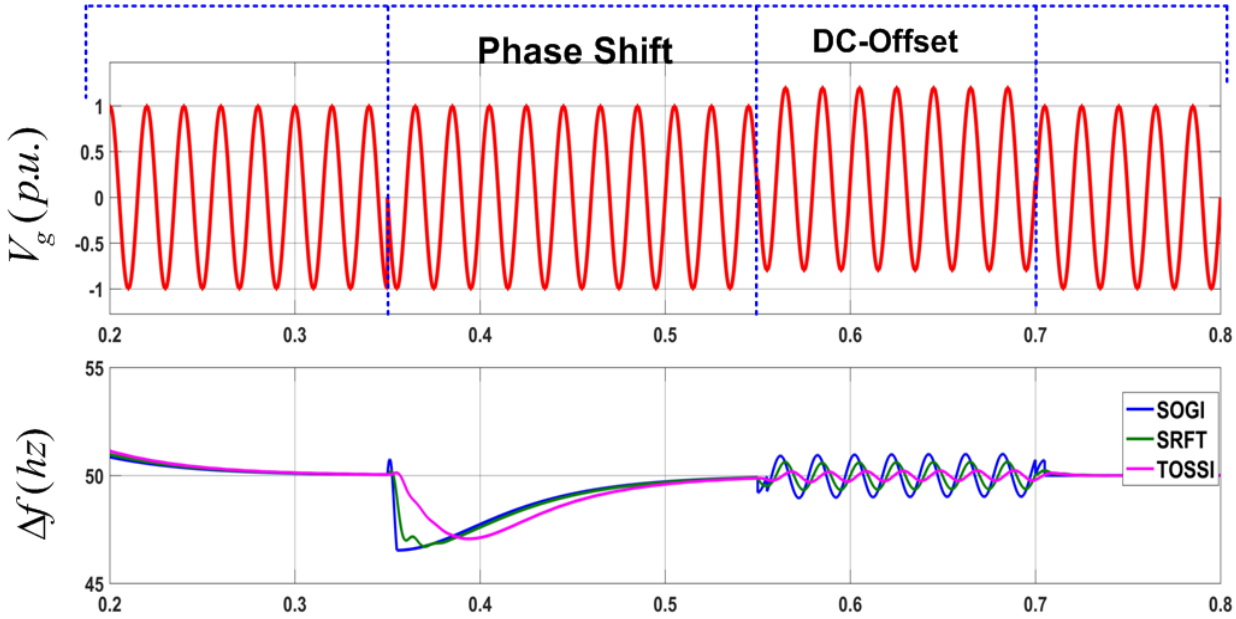



**Fig 6.28** Amplitude Variation of SRF-PLL, SOGI-PLL & TOSSI-PLL under phase shift and DC-offset

The evaluation of the various synchronization approaches under different grid voltage cases has been discussed after the extensive simulation and experimental performances of the suggested synchronization techniques. For the various grid voltage conditions, a performance comparison of the single-phase synchronization technique has been tabulated in Table 6.1. Especially in the case of DC-offset TOSSI-PLL gives good results and shows very low oscillations in the estimation of frequency and amplitude but suffers from the delay in response during dynamics.

Table 6.1 shows the performance comparison of single-phase grid synchronization techniques

| Cases | SRF-PLL | SOGI-PLL | TOSSI-PLL |
|---|---|---|---|
| Voltage Sag of 20% | Moderate | Good | Best |
| DC-offset of 20% | Unsatisfactory | Unsatisfactory | Moderate |
| Phase Shift of $\pi/2$ | Unsatisfactory | Moderate | Moderate |
| Harmonics in Grid | Unsatisfactory | Good | Good |

One application of the proposed synchronization technique, the SOGI-PLL, has been implemented with the design and development of the Parallel Tangent (PARTAN-LMS) algorithm to control 5-level SAPF. The work involves closed-loop control of the system under distorted grid conditions, which is discussed in the further sections

## 6.5 Extraction of the fundamental component of load current using PARTAN-LMS algorithm under Distorted Grid Conditions

The fundamental component of load current has been extracted the Parallel Tangent (PARTAN)-LMS algorithm has been developed and implemented to control 5-level CHB-MLI for harmonic compensation. Oguz Tanrikulu [131] has proposed the PARTAN method for searching space between two variables. Nowadays, this method of parallel tangent has been used extensity to increase learning rate in Artificial Neural Networks (ANN) and multilayer perceptron models. Hence, the concept of PARTAN is incorporated into the LMS algorithm, resulting in the PARTAN-LMS algorithm. The proposed algorithm is tested

extensively for its convergence properties under dynamic load conditions. The block diagram is shown in Fig 6.29

The proposed system is also tested under abnormal grid voltage conditions. An orthogonal set of unit voltage templates are generated by a second-order generalized integrator (SOGI) phase lock loop (PLL) under distorted grid conditions.

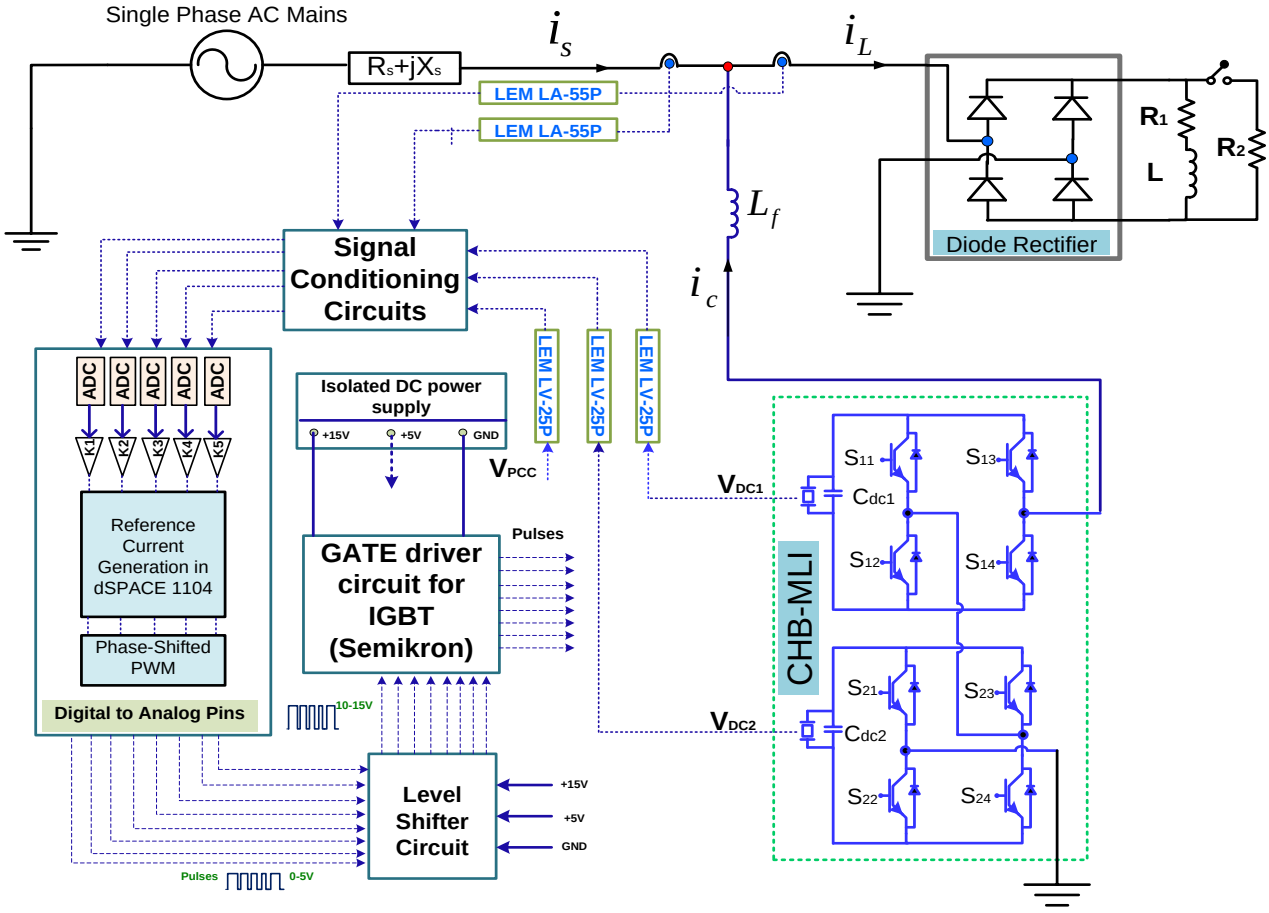



**Fig 6.29** System configuration of PARTAN-LMS Algorithm

### 6.5.1 Modeling and generation of reference current by PARTAN-LMS algorithm

Fig.6.30 represents the complete control scheme of the proposed PARTAN LMS algorithm. The overall control scheme is implemented to extract the fundamental load current corresponding to the active power weight component. The first step involves extracting synchronization signals in the form of sine and cosine templates from the grid. A

SOGI block is used for this purpose which generates perfectly sinusoidal unit templates even in the presence of abnormalities in the grid voltage. The basic structure of SOGI block is depicted in Fig.2, where $V_g$ is the grid voltage is the grid frequency taken as 2πf rad/s in this paper and the estimated frequency and phase angle is represented as $\omega_{est}$ and $\hat{\theta}$ .The SOGI blocks generate in-phase voltage signal $V_\alpha$ and quadrature signal $V_\beta$ .The closed-loop transfer functions of the output signals are represented as $T_\alpha(s)$ and $T_\beta(s)$ in (6.10) and (6.11) where k stands for gain adjustment factor and the selected value is trade-off between the filtering performance and response time.

$$T_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\omega_{est}s}{s^2 + k\omega_{est}s + \omega_{est}^2} \tag{6.10}$$

$$T_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k\omega^2_{est}}{s^2 + k\omega_{est}s + \omega_{est}^2} \tag{6.11}$$

The block diagram of the proposed algorithm is shown in Fig 6.29. Fig 6.30 depicts that the summation of individual DC link voltages across capacitor-1 and capacitor-2 for CHB-MLI achieves the total DC link voltage. It is essential to regulate the DC link voltage to reference voltage $V_{DC\text{-}ref}$ by comparing it to the sensed full DC link voltage $V_{DC}$ ($V_{DC1}$ + $V_{DC2}$), and the resulting DC link error is given as

$$e_{DC} = V_{DC-ref} - V_{DC} \tag{6.12}$$

The DC link error is fed to the proportional and integral controller to obtain the DC loss component, given as

$$w_{loss} = \alpha_P e_{DC}(n) + \alpha_I \sum_{n=1}^{t} e_{DC}(n) \tag{6.13}$$

where $\alpha_P$ and $\alpha_I$ denote the proportional and integral gains of the PI controller. Furthermore, to generate the reference current ($i_{gP}$) and fundamental component of load current $w_{LP1}$, a PARTAN LMS block is used. The estimated reference current is a function of the sine template generated by SOGI-PLL and the fundamental component of sensed load current ($i_L$) and can be represented as

$$[i_{gP}, w_{est}] \Rightarrow f_{PARTAN-LMS}(i_L, \sin\theta) \tag{6.14}$$

Moreover, $w_{est}$ is calculated as

$$w_{est} = w_{loss} + w_{LP1} \tag{6.15}$$

The reference grid ($i_{g\text{-}ref}$) is defined as

$$i_{g-ref} = \Gamma \; i_{gP} \tag{6.16}$$

For unity power factor (UPF) operation $\Gamma$ =1. The reference grid current is compared with the actual sensed source current, and the switching pulses for CHB-MLI are generated using phase-shifted pulse width modulation scheme. The complete control algorithm is shown in Fig 6.30.

The PARATAN-LMS algorithm generates the reference current, and the necessary weight updating equation and time constant analysis are discussed. The weight updating equation for load current is defined as

$$h_{k+1} = h_{k-1} + \mu(1+\beta)\, e_k \; \mu_k + \beta(h_{k-1} - h_{k-3}) \tag{6.17}$$

where h denotes the updated weight, μ is the step size parameter ranging from 0 to 1; β is the momentum term. The error in actual and estimated fundamental load current is defined as

$$e_k(m) = i_{La} - x_k \; h^T{}_k \tag{6.18}$$

$$e_k(m) = i_{La} - i_{Lf} \tag{6.19}$$

$i_{Lf} = x_k h_k^T$ is the fundamental component of load current extracted from the PARTAN-LMS algorithm. In Equation 6.24 β denotes the momentum term, which increases convergence speed. In this paper, μ=0.008 and β=0.6 have been selected for simulation and experimentation.

For load current $i_L(k)$, desired response d(k), input vector x(k) and the weight vector h(k) is expressed as

$$x(k) = [\, x_1(k) \; x_2(k) \; x_3(k) \ldots\ldots x_N(k) \,]^T \tag{6.20}$$

where, $x_1(k) = [\sin w_1 k\Delta t \;\; \cos w_1 k\Delta t \;]^T$

$$h(k) = [\, h_1(k) \; h_2(k) \; h_3(k) \ldots\ldots h_N(k) \,]^T \tag{6.21}$$

here, $h_1(k) = [h_{1_p}(k) \; h_{1q}(k)]^T$

Using equation (6.27) and equation (6.28), the updating expression of output error and weights can be expressed as

$$e(k)=i_L(k)-\begin{bmatrix} h_{1p}(k) \\ h_{1q}(k) \\ h_{2p}(k) \\ h_{2q}(k) \\ - \\ - \\ - \\ - \\ h_{Np}(k) \\ h_{Nq}(k) \end{bmatrix}^T * \begin{bmatrix} \sin \omega_1 k\Delta t \\ \cos \omega_1 k\Delta t \\ \sin 2\omega_2 k\Delta t \\ \cos 2\omega_2 k\Delta t \\ - \\ - \\ - \\ - \\ \cos N\omega_1 k\Delta t \\ \sin N\omega_1 k\Delta t \end{bmatrix} \tag{6.22}$$

The load current is composed of fundamental and various harmonic components that can be defined as

$$\begin{bmatrix} i_{L1}(k) \\ i_{L2}(k) \\ i_{L3}(k) \\ - \\ - \\ i_{LN}(k) \end{bmatrix} = \begin{bmatrix} i_{L1p}(k)+i_{L1q}(k) \\ i_{L2p}(k)+i_{L2q}(k) \\ i_{L3p}(k)+i_{L3q}(k) \\ - \\ - \\ i_{LNp}(k)+i_{LNq}(k) \end{bmatrix} = \begin{bmatrix} h_{1p}(k).\sin \omega_{1k} k\Delta t + h_{1q}(k).\cos \omega_{1k} k\Delta t \\ h_{2p}(k).\sin 2\omega_{2k} k\Delta t + h_{2q}(k).\cos 2\omega_{2k} k\Delta t \\ - \\ - \\ h_{Np}(k).\sin N\omega_{Nk} m\Delta t + h_{Nq}(k).\cos N\omega_{Nk} k\Delta t \end{bmatrix} \tag{6.23}$$

Using Equation 6.30, at $k^{th}$ sampling instant the DSTATCOM injects the compensating current estimated as

$$i^*_{inj}(k)=i_{L1(q)}(k)+\sum_{h=2}^{N} i_{Lh}(k) \tag{6.24}$$

$$i^*_{inj}(m)=\omega_{1q}(m)*\cos\omega_1 m\Delta t + \sum_{h=2}^{N}\left\{\omega_{hp}(m)*\sinh \omega_1 m\Delta t+\omega_{hq}(m)*\cosh\omega_1 m\Delta t\right\} \tag{6.25}$$

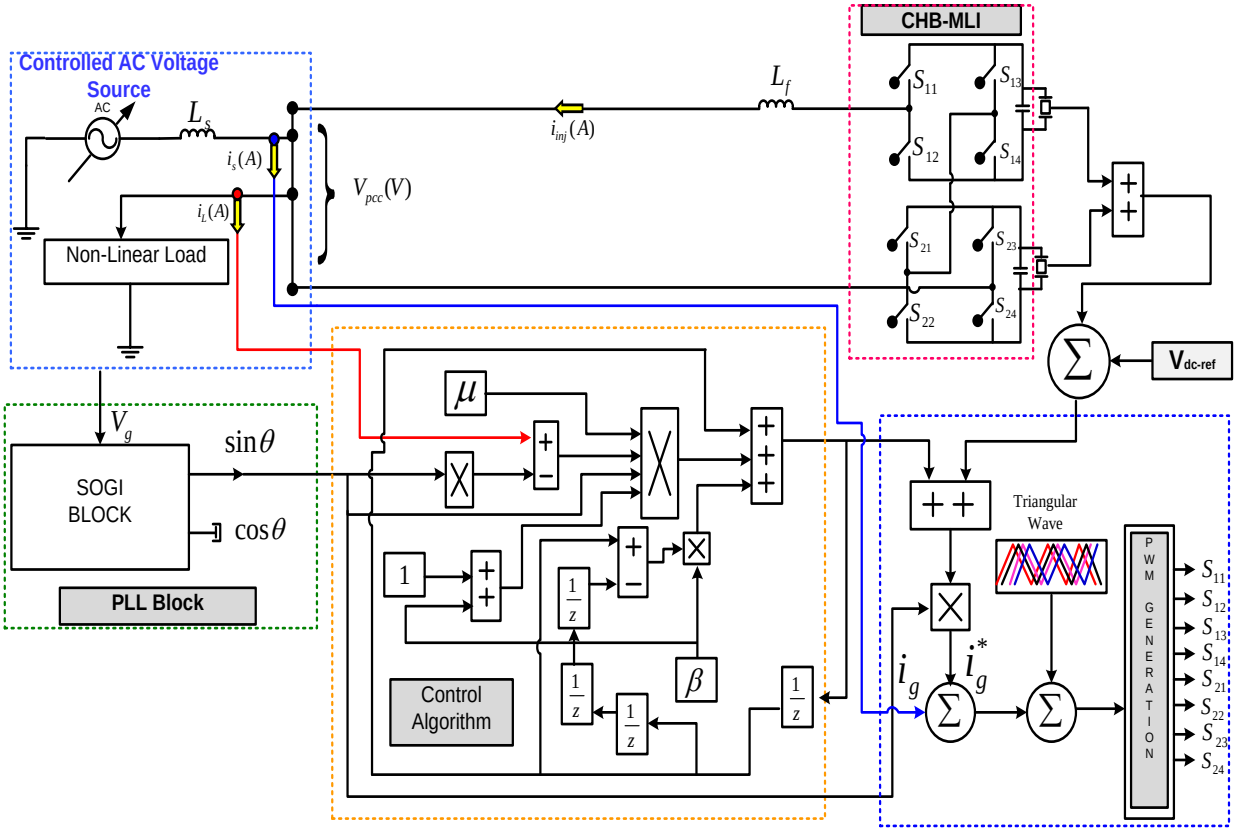



**Fig 6.30** Control Scheme block diagram of PARTAN-LMS Algorithm

### 6.5.1 Simulation Results with PARTAN-LMS Algorithm

The Simpower system toolbox of MATLAB is used to model and implement the proposed PARTAN-LMS algorithm. The system is modeled and tested under normal and abnormal grid conditions like distortion in supply voltage, voltage sag, and voltage swell conditions feeding the non-linear load.

The system is tested under dynamic load variations under normal grid conditions. Fig 6.31 shows load variations at t=1s when the load current is increased from 5A to 7.5A and at t=1.3s load current decreases to 5A. During these load changes, the total DC voltage magnitude across both capacitors varies slightly by ±2.5V. Due to the rapid action of the PI controller, the DC link voltages reach the steady state reference value quickly.

Fig 6.32 depicts the waveforms of $i_L$(A), $V_{DC1}$, $V_{DC2}$, and total DC link voltage $V_{DC}$. It is observed from this Fig that the DC link voltages of both the capacitors are self-balancing in nature, and their values settle to reference value i.e., 100V each.

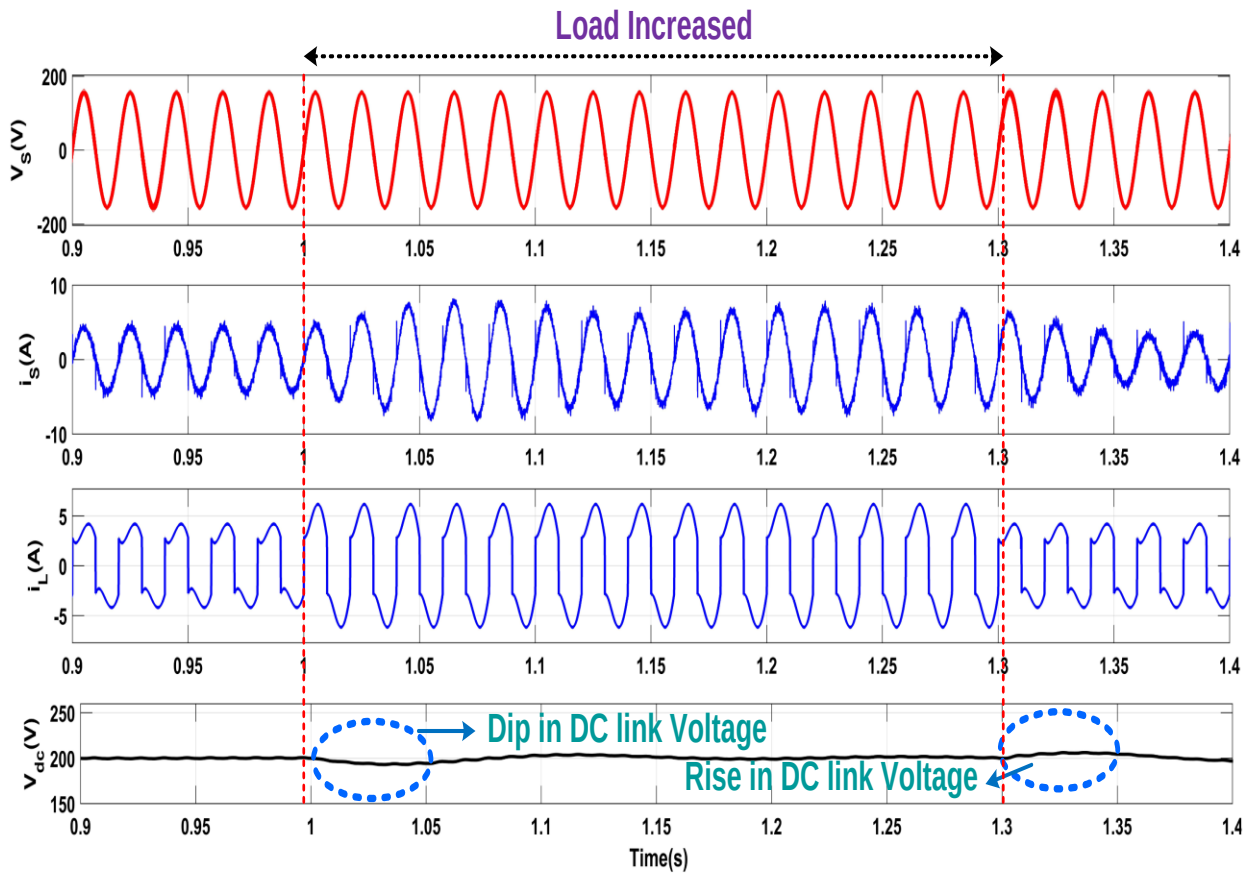



**Fig 6.31** Simulation results of grid voltage $v_g$(V), grid current $i_g$(A), load current $i_L$(A) and total DC link voltages $V_{dc}$(V)

The proposed system is also tested under voltage sag and swell conditions simulated in the grid. Fig 6.33 depicts the waveforms of $V_{pcc}$(V), phase angle $\theta$, unit sine template $\sin\theta$, and estimated voltage amplitude $V_t$(V). The system uses the SOGI-PLL-generated voltage templates for synchronization. The voltage swell of 20% is incorporated at t=0.4s, and a sag of 20% is added at t=0.5s, as shown in Fig 6.33. During sag and swell conditions, the proposed system can estimate the correct templates, and the estimated voltage magnitude is tracked correctly.

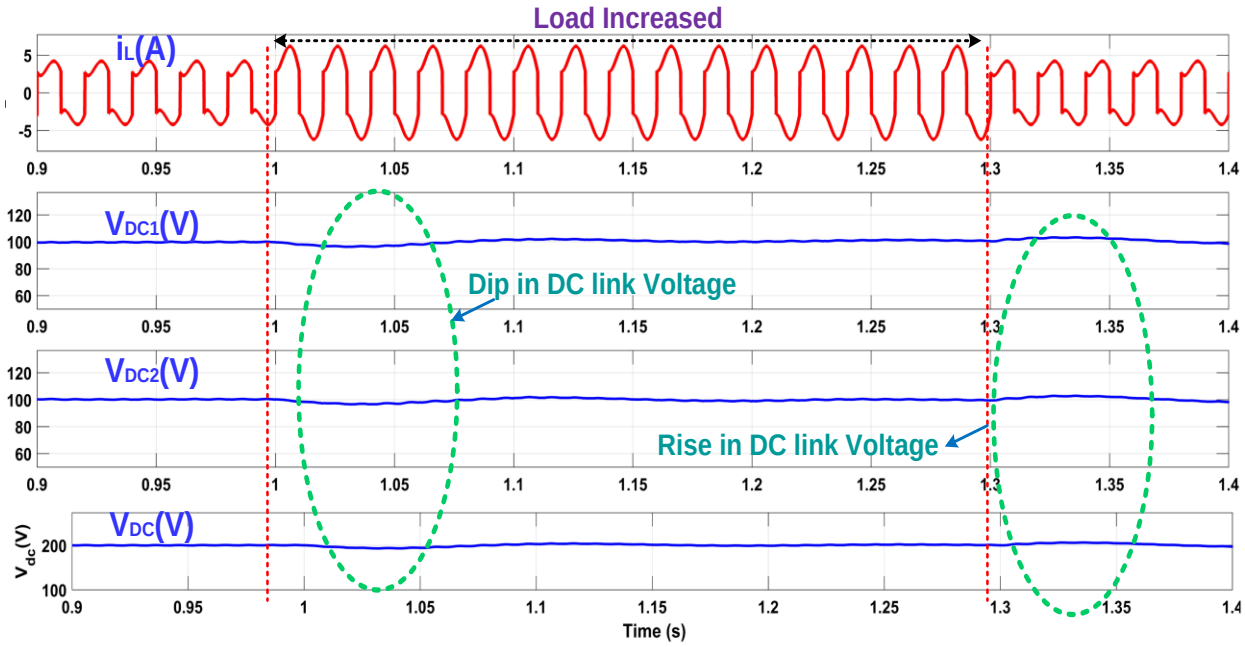



**Fig 6.32** Dynamic waveforms of $i_L$(A),$V_{DC1}$(V), $V_{DC2}$(V) and $V_{DC}$(V) under step change in load at t=1s and t=1.3s

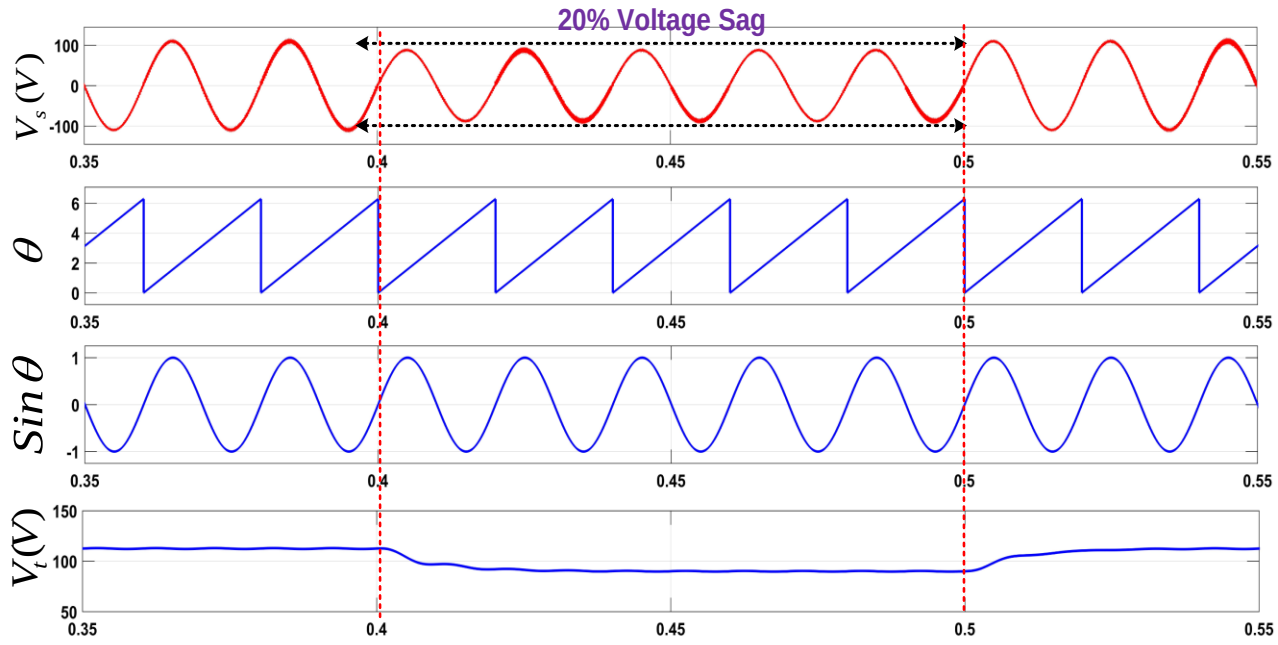



**Fig 6.33** Waveforms of $V_{pcc}$(V), phase angle $\theta$ , unit sine template $\sin\theta$ estimated voltage amplitude $V_t$(V) under voltage swell at t=0.4s to 0.5s

Now, the closed loop performance of the system is tested for dynamic load variations and in distorted voltage grid conditions. The grid voltage distortion of magnitude

$V_s(t) = 110\sin\omega t + 49.50\sin 3\omega t + 14\sin 5\omega t$ is added at=0.4s till t=0.5s as depicted in Fig 6.34

The Fig 6.34 shows the waveforms of $V_{pcc}$(V), $i_S$(A), $i_L$(A), $i_C$(A),$V_{DC}$(V) and $V_{inv}$(V) under voltage distortion and step change in load during t=0.4s to 0.5s

Fig 6.35(a-c) shows the distorted voltage having THD of 24.74%, source current THD of 3.83%, and the load current THD under distorted grid is found to be 32.26% respectively. The obtained THD in $i_S$(A) lies within IEEE-519 standards

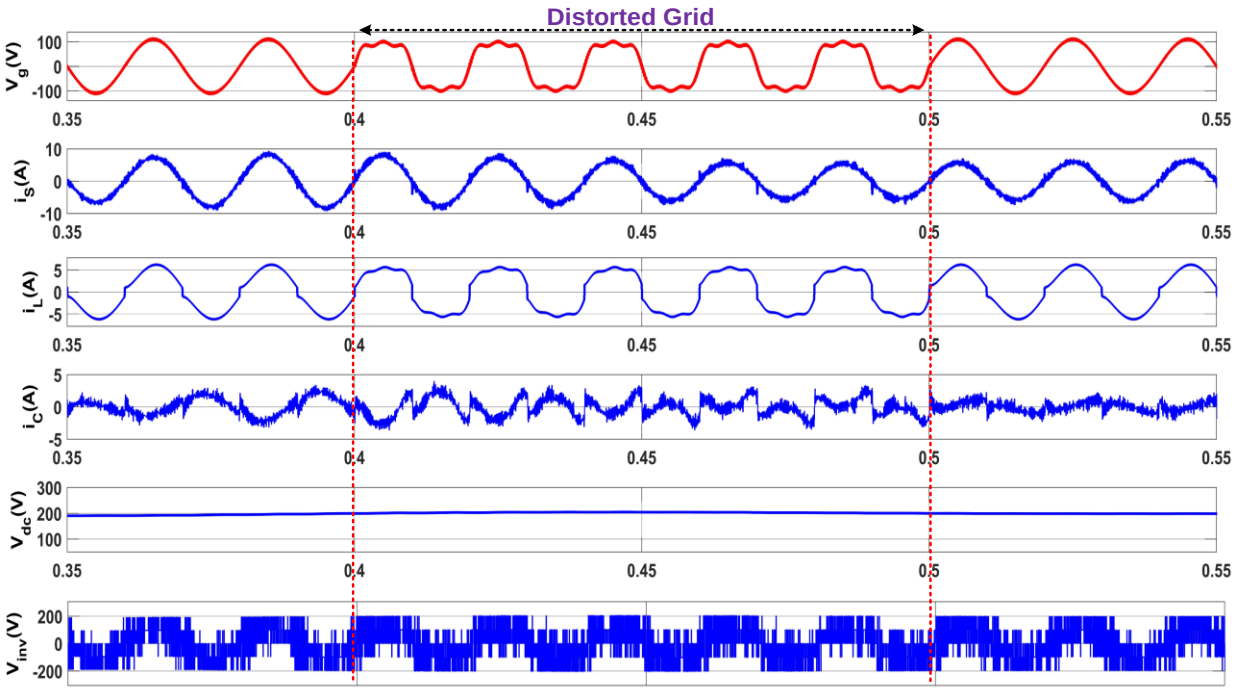
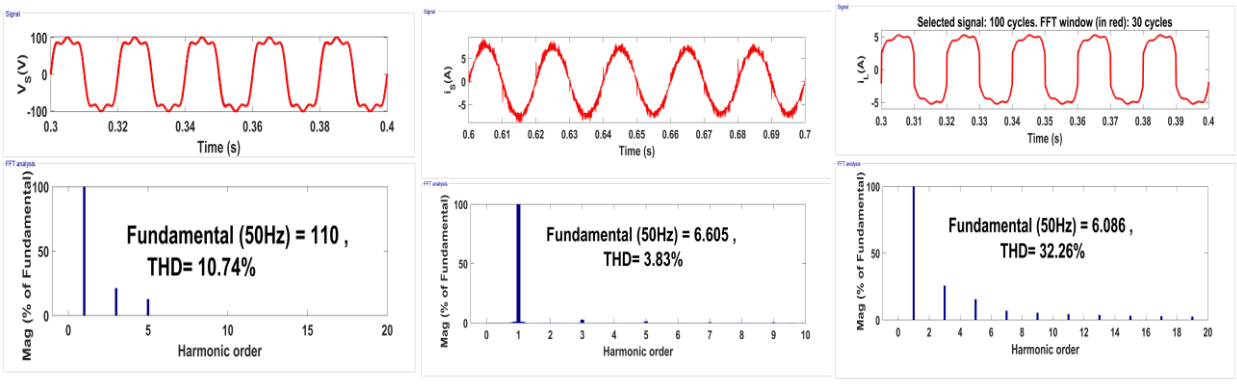



**Fig 6.34** Dynamic state waveforms of $V_{pcc}$(V), $i_S$(A), $i_L$(A), $i_C$(A), $V_{DC}$(V) and $V_{inv}$(V) under distorted grid voltage and varying load




(b) (c)

**Fig 6.35** Harmonic spectrum THD of (a) Source Voltage $v_S$(V) (b) Source Current $i_S$(A) (c) Load current $i_L$(A) under distorted grid

### 6.5.2 Experimental Results with PARTAN-LMS Algorithm

Fig 6.36 (a-c) shows the steady-state waveforms obtained using the PARTAN-LMS algorithm. The steady waveforms of source voltage $v_s$(V) w.r.t to source current $i_S$(A), load current $i_L$(A), compensating current $i_C$(A). Fig 6.36(d) shows the experimental results of THD obtained in distorted voltage as 12.2%. The load current shows THD of 30.1%, as depicted in Fig 6.36(e), and the source current THD is found to be 3.8%, as shown in Fig 6.36 (f). The compensator injects current, which significantly reduces the THD of supply current as per IEEE-519 stipulated standards.

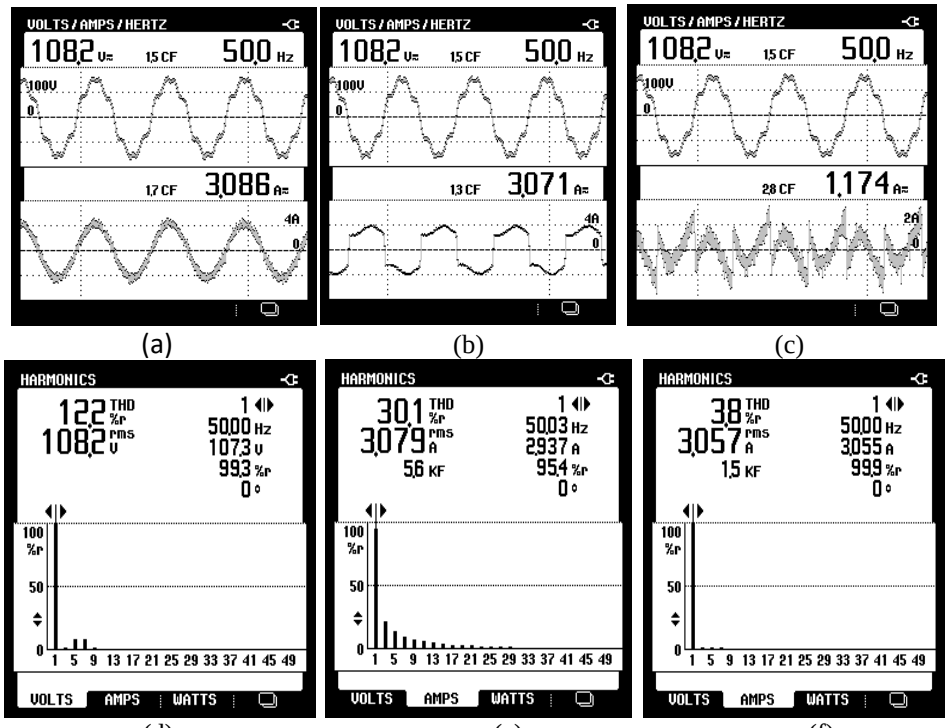
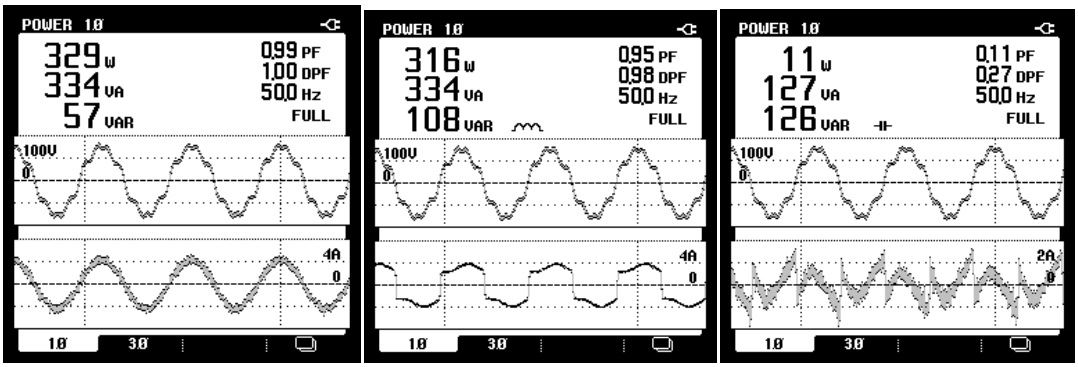



**Fig 6.36** Harmonic spectrum (THD) analysis (a) $v_s$ (V) with $i_S$(A) (b) $v_s$ (V) with $i_L$(A) (c) $v_s$ (V) with $i_C$(A) (d) THD of $v_s$ (V) (e) THD of $i_L$(A) and (f) THD of $i_S$(A)

The active power demand and reactive power demand of the load in the proposed system are observed to be 0.316kW and 0.108KVAR, as shown in Fig 6.37(a). The supply meets the active power requirement of the load and switching load requirement of CHB-MLI. As illustrated in Fig 6.37(c), the compensator reactive power 0.126kVAR can satisfy the load's reactive energy requirement (0.108kVAR) and improves the power factor to 0.95 to 0.99. The supply current is purely sinusoidal in nature, even under distorted grid

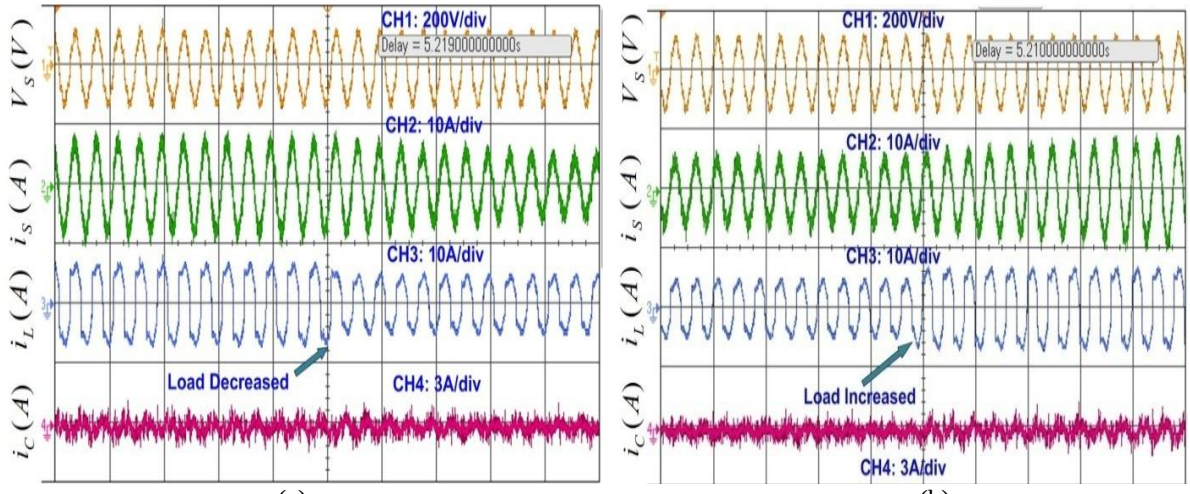
conditions.




(a) (b) (c)

**Fig 6.37** shows the active and reactive power flow in 5-Level SAPF control by PARTAN-LMS

Fig 6.38(a-b) shows the waveforms of $V_s$ (V), $i_S$(A), $i_L$(A), and $i_C$ (A) under distorted voltage grid conditions and with a step decrease in load. Adequate compensation is obtained in this case




(a) (b)

**Fig 6.38** Experimental waveforms of $V_s$(V), $i_S$(A),$i_L$(A) and $i_C$(A) under varying load and distorted grid

Fig 6.39 (a) shows the effect of load variation on the magnitude of DC link voltages. A slight rise and dip have been observed in $V_{dc}$ due to a decrement and increment in load, respectively. Fig 6.39 (b-c) shows the estimated weight component ($w_{est}$) quickly within 1~2 cycles using the proposed algorithm. Results show that steady state weight values are obtained during sudden decrement and increment in load. The corresponding effect of load variations is observed on channels CH1, CH2, CH3, and CH4 in Fig 6.39(b-c).

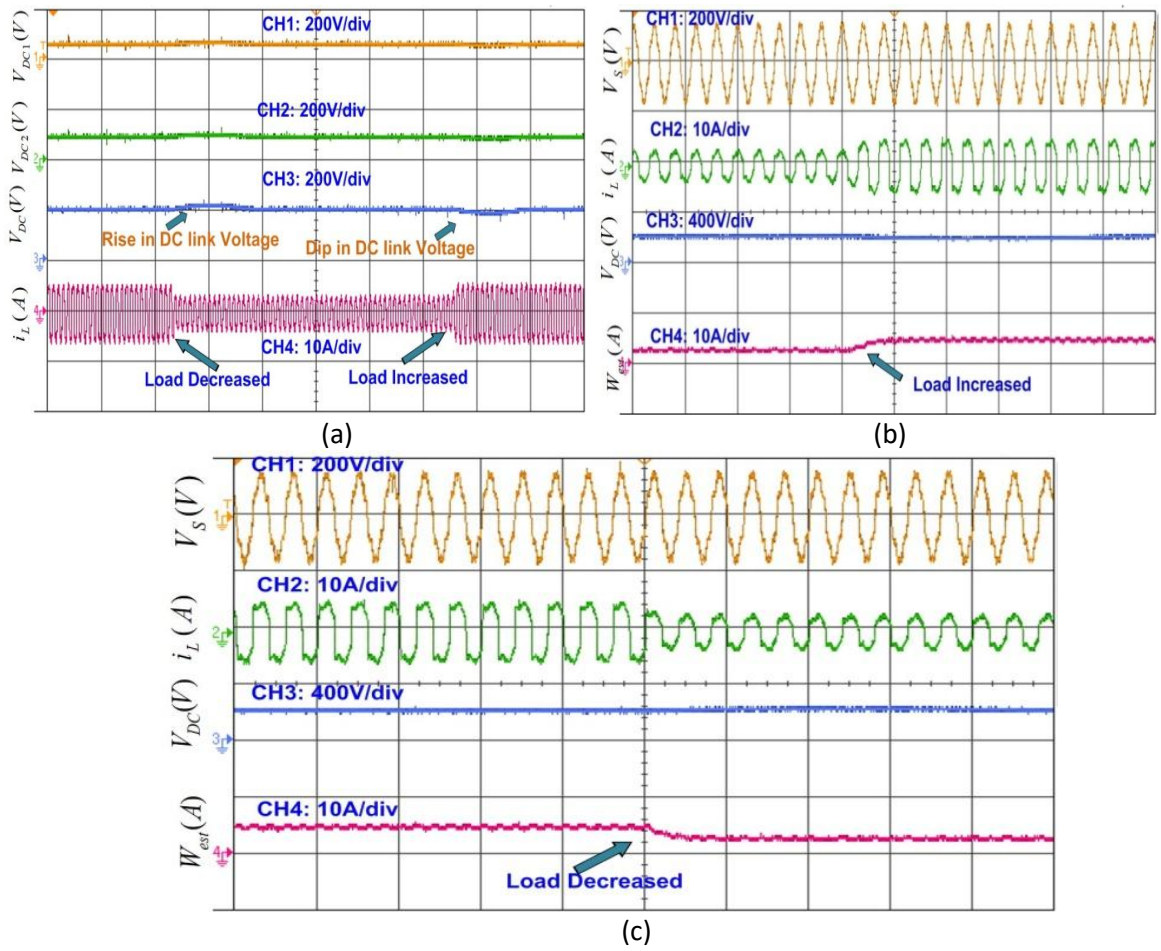



**Fig 6.39** Variation in DC link voltages, source current, load current, and fundamental estimated weights

In Fig 6.40 (a-b), 20% voltage sag and swell have been added to the source voltage ($V_s$). The SOGI filter accurately estimates the $\theta$ and $\sin\theta$ as shown in CH2 and CH3. In addition, the effect of voltage variation is correctly observed in the estimated terminal voltage ($V_t$), and unit templates are accurately computed.

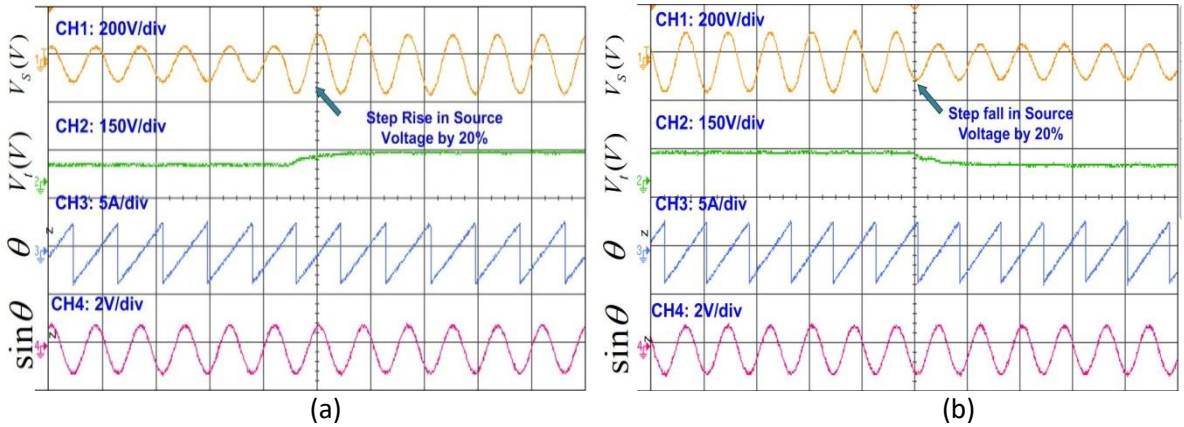



**Fig 6.40** Waveforms of $v_s$(V), $V_t$(V), $\theta$ and $\sin\theta$ under voltage sag and swell

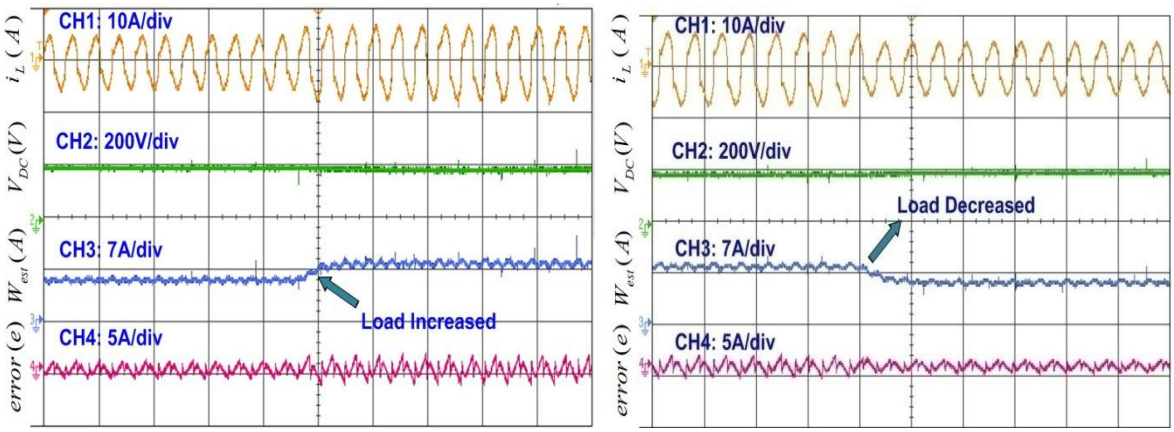



**Fig 6.41** Intermediate results of $w_{est}$, error with reference to DC link voltage and load current under varying load

The illustrated waveforms justify the performance of the proposed PARTAM-LMS algorithm implemented for compensation. The algorithm computes the fundamental active power component of load current correctly and fast. There is no need for complex balancing circuits to balance the two DC link voltages. In addition, the obtained THD of source currents is within 5% as per stipulated limits. The proposed algorithm can also improve the system power factor to near unity even under distorted voltage grid conditions as it is integrated into SOGI-PLL.

## 6.6 Comparative Analysis of PARTAN-LMS algorithm with Conventional Algorithms

The proposed PARTAN-LMS algorithm is compared with the conventional Least Mean Square (LMS) and Recursive Least Mean Square (RLMS) algorithms in terms of computational time, steady state error, system complexity, weight convergence, and varying load conditions. The detailed comparison is tabulated in Table 6.2. Fig 6.42 shows the performance comparisons of weights using different adaptive algorithms w.r.t load current. The effectiveness of the proposed algorithm is reflected in the quick convergence of weights during a step change in load. However, it is well-known that convergence depends upon the values of step size parameters. There is always a trade-off to choosing the optimal step size value or allowable limit to achieve fast convergence. It was observed that a good balance

between fast convergence and lower steady-state error is required. In the proposed PARTAN-LMS, the step size value is taken as μ=0.008, and a momentum term (β=0.6) is also introduced to minimize the steady state error and improve convergence. The oscillations with the LMS algorithm in weight estimation is observed to be more, and hence it will take more time to converge while the PARTAN-LMS converges quickly with very low oscillations.

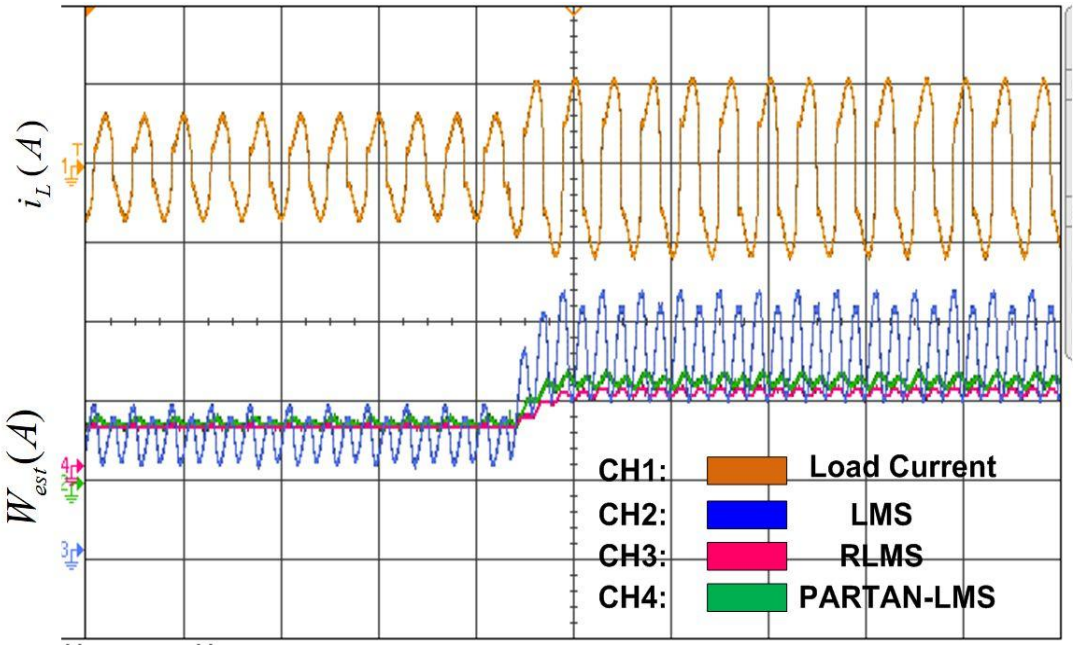



**Fig 6.42** Performance comparisons of weights using different adaptive algorithms w.r.t load current

**Table 6.2:** Comparison of PARTAN-LMS with the conventional algorithm

| S.No | Parameters | PARTAN-LMS | RLMS | LMS |
|---|---|---|---|---|
| 1. | Type of Filter | Adaptive | Adaptive | Adaptive |
| 2. | Estimation of fundamental weights | Low overshoot of ± 0.2A | Moderate overshoot of ± 0.5A | High overshoot of ± 1A |
| 3. | THD of supply current (A, RMS) **(under distorted grid)** | 3.83% | 4.2 % | 4.5% |
| 4. | THD of supply current (A, RMS) **(under normal Grid)** | 2.52% | 3.9% | 4.2% |
| 5. | THD of Load current (A, RMS) | 32.26% | 32.26% | 32.26% |
| 6. | Steady-state error | Less | Higher than | Higher than |

| | | | | |
|---|---|---|---|---|
| | | (± 0.2%) | PARTAN-LMS (± 0.65%) | RLMS (± 0.95%) |
| 7. | Convergence | **Faster (1~2 cycles)** | Moderate (3~4cycles) | Lower (4~ 5cycles) |
| 8. | Complexity | Low | Moderate | High |
| 9. | Sampling time | 45µs | 65µs | 70µs |

## 6.7 Conclusion

Grid-synchronization methods for single-phase systems have been presented in this chapter. The SRF-PLL, SOGI-PLL, and TOSSI-PLL have been investigated. The findings of extensive mathematical modeling, simulations and experiments have been presented. The effectiveness of the synchronization techniques has been demonstrated through simulation and experimental testing under various grid voltage conditions such as voltage sag and swell, phase shift, and DC offset, and also tested under sudden load variations.

It was observed that the TOSSI-PLL exhibits the best performance for amplitude and frequency tracking and estimation under grid voltage variations. TOSSI-PLL estimates frequency with high accuracy, but some delay in convergence is also observed. During the polluted and voltage sag/swell grid conditions, TOSSI-PLL and SOGI-PLL both work satisfactorily to estimate frequency and amplitude. However, in the case of DC-offset conditions, both SRFT and SOGI PLLs fail to estimate the accurate frequency and amplitude. The TOSSI-PLL gives negligible frequency and amplitude estimation oscillations even under DC-offset conditions and distorted grid cases.

Further in this chapter, PARTAM-LMS adaptive control algorithm has been implemented for a single-phase grid-connected system for harmonic compensation under distorted grid conditions. The 5-level CHB-MLI is used as a SAPF unit which is controlled by the PARTAN-LMS algorithm and serves multiple objectives.

Power quality is improved with reactive power compensation, power factor improvement, and harmonic reduction. The control algorithm estimates the fundamental active power component from load current under voltage swell, sag, and distorted grid conditions. The TOSSI-PLL suffers from delay during dynamics, so the SOGI-PLL-based synchronization technique has been used to generate unit sine templates under distorted grid

conditions.

In the laboratory, a basic prototype model has been developed to test the effectiveness of the proposed configuration. Extensive simulation and experimental results have been demonstrated, and THD obtained in utility grid voltage and current with PARTAN-LMS algorithm is <5% as required by IEEE-519 standard. Finally, comparing different LMS techniques highlights the enhanced results obtained using the developed technique.

# Chapter -07

# Power Quality Improvement using Single Phase MLI based Grid Connected PV System

## 7.0 Introduction

Single phase grid synchronization PLLs and single-phase SAPFs and their control algorithms have been covered in the previous chapters. In this chapter, PV arrays have been interfaced to a single-phase grid using VSC, which also gives additional ability to inject active power. Two PV arrays of 0.954kW rating have been interfaced at the DC links of each of the H bridge forming the 5-level MLI. The implementation of an appropriate control algorithm is necessary for active and reactive power balancing as well as power quality enhancement. The designed control algorithm must be able to estimate the fundamental current component, estimate the non-linear load current, acquire synchronization from the grid voltage signal, use the MPPT algorithm, regulate the DC linkvoltages, and estimate the feed-forward current from the PV array.

## 7.1 Single-Stage Grid-Connected PV system

The single-stage grid-connected PV system is shown in Fig.7.1.Two PV arrays of rating 0.958kW each have been connected to the DC links of 5-level CHB-MLI.The system operates in two modes: day (mode-1) and night (mode-2). During the day, the PV arrays supply active power to the grid; during the night, the system acts as a SAPF unit and provides harmonic compensation. In addition, the proposed system also provides flexibility to integrate more PV arrays to increase the number of voltage levels. The SAPF can be controlled by sensing the input variables, viz. voltage at the point of common coupling (PCC), load current ($i_L$), source current ($i_s$), and dc bus voltages $V_{dc1}$, $V_{dc2}$. An interfacing inductor ($L_f$) is connected in CHB-MLI to reduce the ripples in ac output. SAPF unit is current-controlled using developed techniques to inject suitable compensating current in phase opposition to eliminate the harmonics generated by the load current. The effective operation of the CHB-MLI can be done by controlling both the dc-link voltages of PV arrays at a constant level and this function is realized by the conventional PI controller and

Maximum Power Point Tracking (MPPT) technique. The system is simulated using MATLAB/SIMULINK.In a single-stage grid-connected PV system, a DC-DC boost converter is not needed; instead, the MPPT technique generates the reference voltage and maintains the DClink to extract the maximum power possible from the PV.

### 7.1.1 Extraction of Fundamental Component of Load Current

For the single-phase grid-connected PV system, three control algorithms viz SRFT-PLL, SOGI-PLL, Modified Notch Filter (MNFSOGI-PLL), and TOSSI-PLL have been developed, and discussed andtheir performance has been compared. Due to the superior performance of the MNFSOGI-PLL under distorted grid conditions, the M NFSOGI-PLL has been explored and studied with the traditional SOGI and SRFTcontroller for the single-stage and single-phase grid-connected PV system.

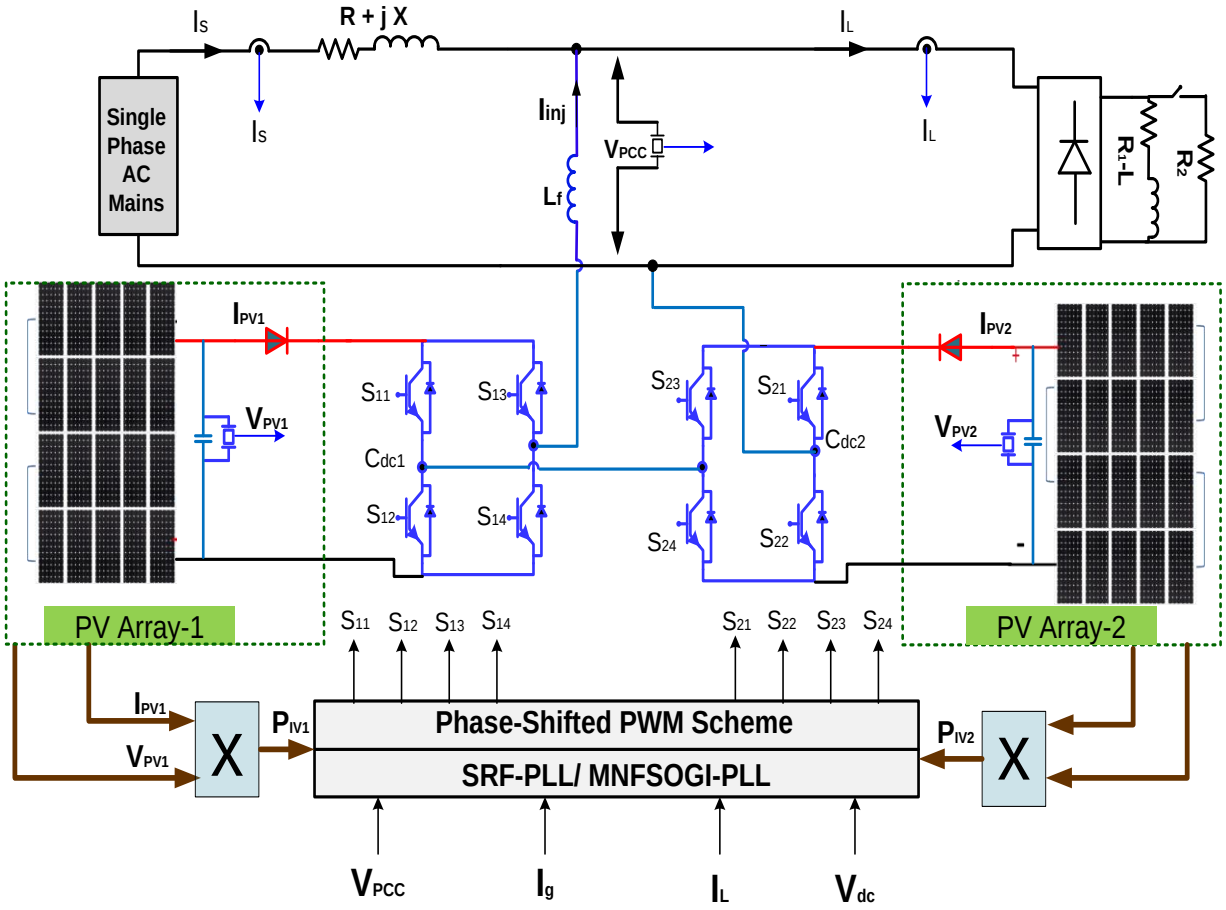
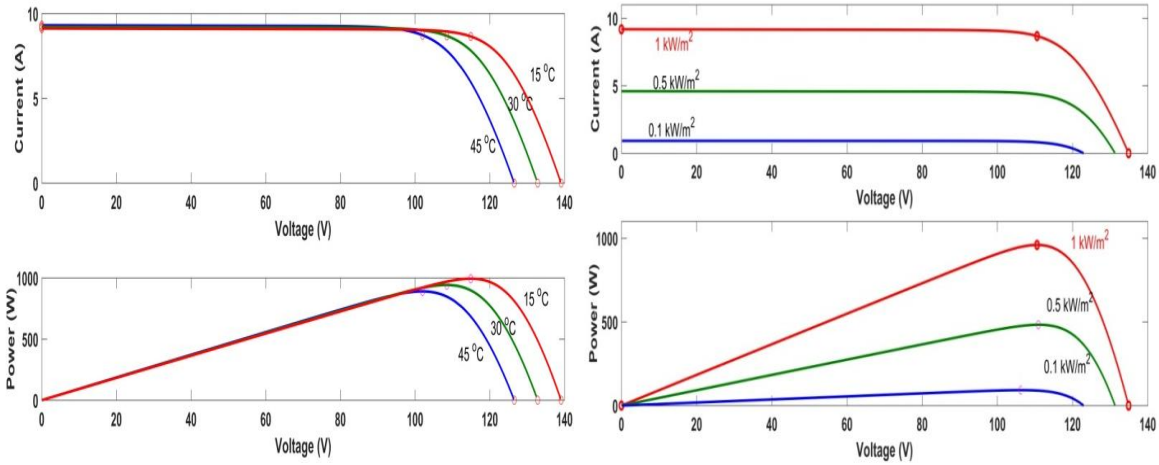



**Fig 7.1**Single Stage grid-connected PV system for 5-level CHB-MLI

### 7.1.2 Maximum Power Tracking Concept

In particular, the irradiance and temperature significantly impact the PV array module's performance. Fig 7.2 (a,b) shows module P-V and I-V curves for the 0.958kW rating of PV arrays. The PV current and the power changes are observed to fluctuate significantly as the irradiance changes as shown in Fig 7.2(a). Nevertheless, the variance in PV power production is less noticeable as the PV module's temperature changes. Low power is produced at higher temperatures, while a PV array's output power is higher at lower temperatures, as depicted in Fig 7.2(b).

Maximum PowerPoint refers to the point on the P-V and I-V curves when power is at its maximum for the given irradiance and temperature. The maximum power point voltage ($V_{mpp}$), and maximum power point current ($I_{mpp}$), respectively, refer to the voltage and current at the maximum power point ($P_{mp}$).




(a) (b)

**Fig 7.2** I-V and P-V Characteristics (a) Fixed temperature of 25°C at varying irradiance (b) Fixed irradiance of 1000W/$m^2$at varying temperatures

Several MPPT algorithms have been developed and used in the literature[145-150], including-Perturb and Observe (P and O), incremental conductance (INC), and soft computing-based techniques like fuzzy logic and ANN-based algorithms. The P and O technique for single-stage grid-connected PV systems is depicted in a flow chart in Fig 7.3. It is one of the simplest and easiest to implement algorithms that have been studied. It also offers good tracking performance. The maximum output power voltage ($V_{mpp}$) isobtained by collecting current and voltage samples at different irradiance.Furthermore, the collected data

is used to calculate the power and compare it with the previous values. The mathematical expressions of PandO algorithm for a single-phase PV integrated grid-connected system are as follows:

$$\begin{aligned} &if && \Delta P\times\Delta V>0 \Rightarrow V_{new}=V_{old}+\Delta V \\ &and\ if && \Delta P\times\Delta V<0 \Rightarrow V_{new}=V_{old}-\Delta V \\ &at\ MPPT && \Delta P\times\Delta V=0 \Rightarrow V_{new}=V_{old}\ ,\Delta V=0 \end{aligned} \tag{7.1}$$

The above expression generates the $V_{mpp}$ and is further required to find the $V_{dc\text{-}ref}$.

The reference maximum power voltage is updated with step size $\Delta V$ as given in Equation 7.1. For a double-stage,PV array-based grid-connected system,the MPPT algorithm (PandO) generates the DC-DC converter's duty cycle. The mathematical expressions are given in Equations 7.2

$$\begin{aligned} &if && \Delta P\times\Delta V>0 \Rightarrow D_{new}=D_{old}-\Delta D \\ &and\ if && \Delta P\times\Delta V<0 \Rightarrow D_{new}=D_{old}+\Delta D \\ &at\ MPPT && \Delta P\times\Delta V=0 \Rightarrow D_{new}=D_{old}\ ,\Delta D=0 \end{aligned}$$

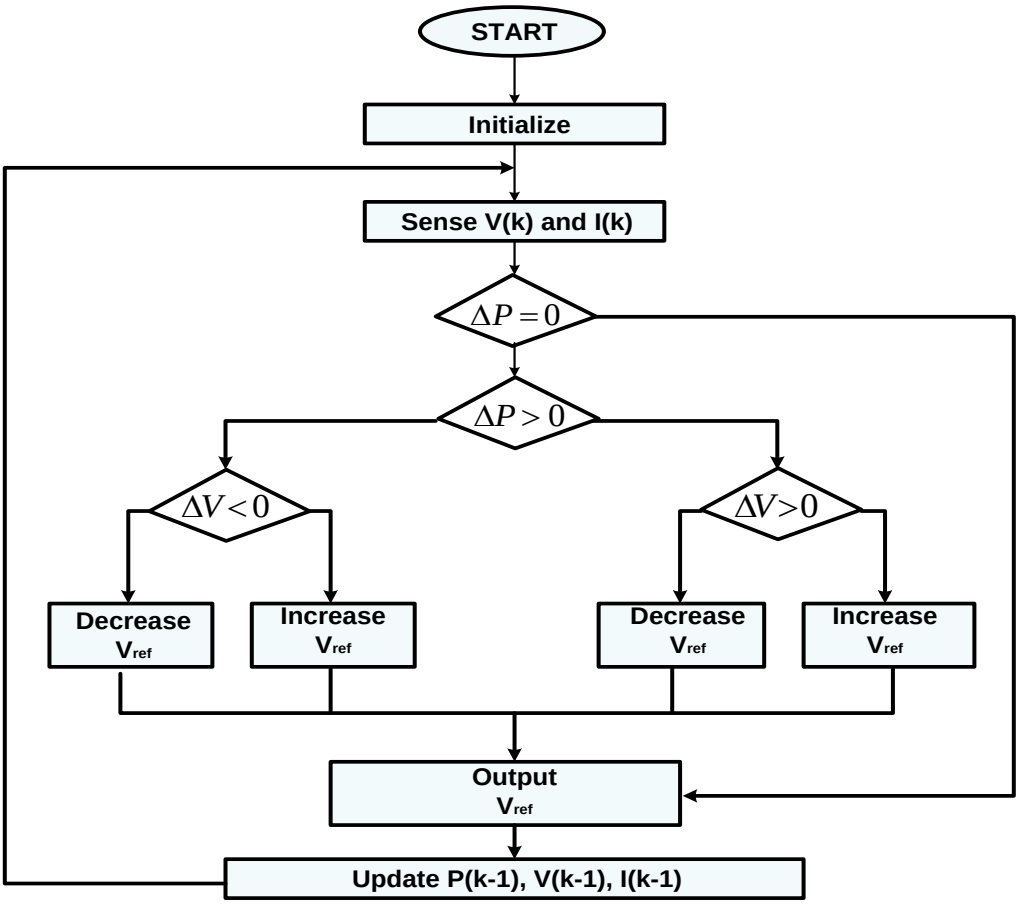



**Fig 7.3** Flow chart of Perturb and Observealgorithm [151]

### 7.1.3 Estimation of Feed Forward Current

According to its capacity and rating, the PV array uses VSC 5-level MLI to transfer active power to the grid. In an ideal situation, PV power is provided at the output of VSC ($P_{pv}$=$P_c$), resulting in a negligible loss for the inverter. In this case, $P_c$ stands for the AC side power of the MLI, while $P_{pv}$ is the power produced by the PV and is given as

$$P_{PV}=V_{PV}*I_{PV} \tag{7.3}$$

Here, $V_{PV}$ is the summation of output voltages obtainedfrom PV-arrays. Similarly, the $I_{PV}$ is the output current.

### 7.1.4 DC Loss Calculation and Generation of Reference Current

The proposed PV interfaced MLI serves two purposes (i) to provide active power to the AC grid and (ii) to compensate for the harmonics generated by the non-linear load and make a unity power factor on the supply side. For the effective operation of the proposed system under both conditions, it is necessary to control the fluctuations in DC link voltages obtained across PV arrays. Therefore,proportional–integral (PI) control is used to manage the DC link voltages. The DC link error can be estimated as

$$e_{DCe}=e_{DC-ref}-e_{DC} \tag{7.4}$$

The error signal is fed to the PI controller, and $I_{loss}$ is calculated, as shown in Fig 7.4.Mathematically it can be represented as

$$I_{loss}(n+1)=I_{loss}(n)+k_p\{e_{DCe}(n+1)-e_{DCe}(n)\}+k_i e_{DCe}(n+1) \tag{7.5}$$

where $k_p$ and $k_i$ are the proportional and integral gains, respectively, and the dynamic system performance of current and voltage can be improved by the feed-forward term $P_{PV}$which can be estimated as

$$I_{PV}=\frac{2(P_{PV1}+P_{PV2})}{V_t} \tag{7.6}$$

The reference current is generated by multiplying the unit synchronizing template with the estimated load current, represented as

$$i_{gr}^{*}=u_p I_{est} \tag{7.7}$$

$$I_{est} = I_{loss} + I_f - I_{PV} \tag{7.8}$$

The fundamental estimated load current is $I_{est}$, the fundamental load current is $I_{f,}$and PV feed-forward current is $I_{PV}$. The generated reference current is subtracted from the actual grid current, and further, this signal is compared with phase-shifted PWM technique to generate firing pulses for 5-Level CHB-MLI as shown in Fig 7.4.

## 7.2 Performance of PV integrated Single Phase SAPF using SRFT –PLL

The complete control structure for single-stage with SRFT control technique is shown in Fig. 7.4.The following test cases have been studied

1. Normal grid conditionsunder varying solar irradiance and load
2. Distorted grid conditions under varying solar irradiance and load

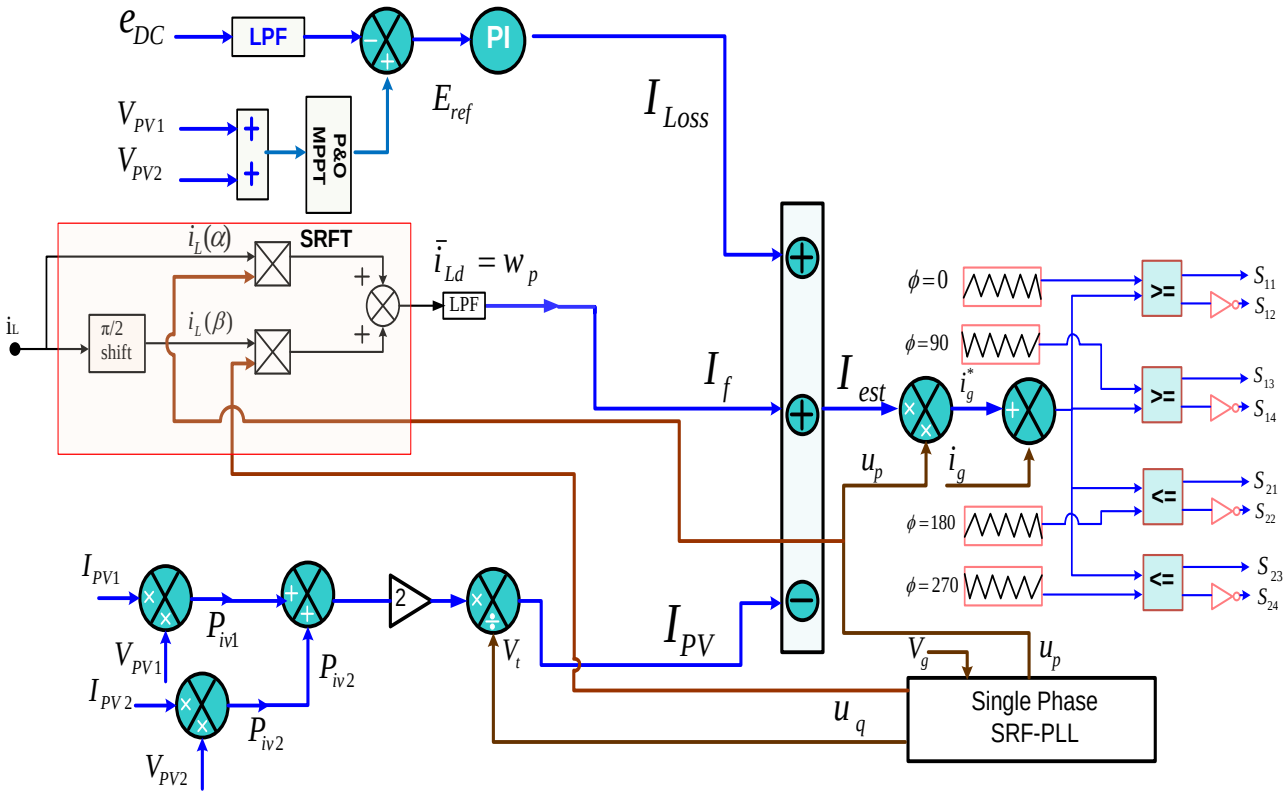



**Fig 7.4** Single Phase single stage PV array based SRFT-PLL

### 7.2.1 Simulation Results Of Single Phase Single Stage PV Array Based SRF-PLLunder Normal Grid Conditions

The MATLAB/Simulink platform has been used to simulate a single-phase, single-stage grid-connected PV system. The DC-link of the CHB-MLI is connected to twoPV strings with three modules, each rating of 0.318kW have been linked in series for power injection. For a single-phase system to control the DC link voltages of CHB-MLI, an MPPT technique is implemented, and its output is compared with the reference DC link voltage. For the purpose of improving power quality, this system is evaluated under normal and polluted grid conditions. During mode-1 operation, the system works with a PV–SAPF providing active and reactive power to the grid. During mode-2, PV arrays are not utilized; therefore, the system acts as a normal SAPF to mitigate the harmonics generated by the load.

The detailed discussion on SRFT-based SAPF control has already been covered in Chapter-04 Section 4.9. In this chapter, the SRFT algorithm is implemented to extract the fundamental component of load current for PV integrated grid connected system. Fig 7.5 depicts the results of grid voltage $v_g$(V), grid current $i_g$(A), load current $i_L$(A) and total DC link voltage $V_{DC}$(V) with a change in solar irradiance of 1000W/m$^2$ to 600 W/m$^2$ and dynamic load conditions during normal grid conditions.

At t=0.3s, the solar irradiance is varied from 1000W/m$^2$ to 600W/m$^{2,}$ and at t=0.5s again irradiance is restored to 1000 W/m$^2$. It is observed that then the amount of solar PV currents extracted from panels decreasesduring variation of solar irradiance from 1000W/m$^2$ to 600W/m$^2$. However,a very nominal risehas been observed on PV array open circuit voltages viz$V_{pv1}$ and $V_{pv2,}$as shown in Fig7.5.The output PV power is also reduced due to irradiance variation.

Now, during load variation during t=0.6 to 0.7s, no variation is seen in PV array output currents, and a nominal variation in PV-array output voltages has been observed, due to which the PV array output power varies, as shown in Fig 7.5. The detailed variation in PV array parameters are tabulated in Table 7.1

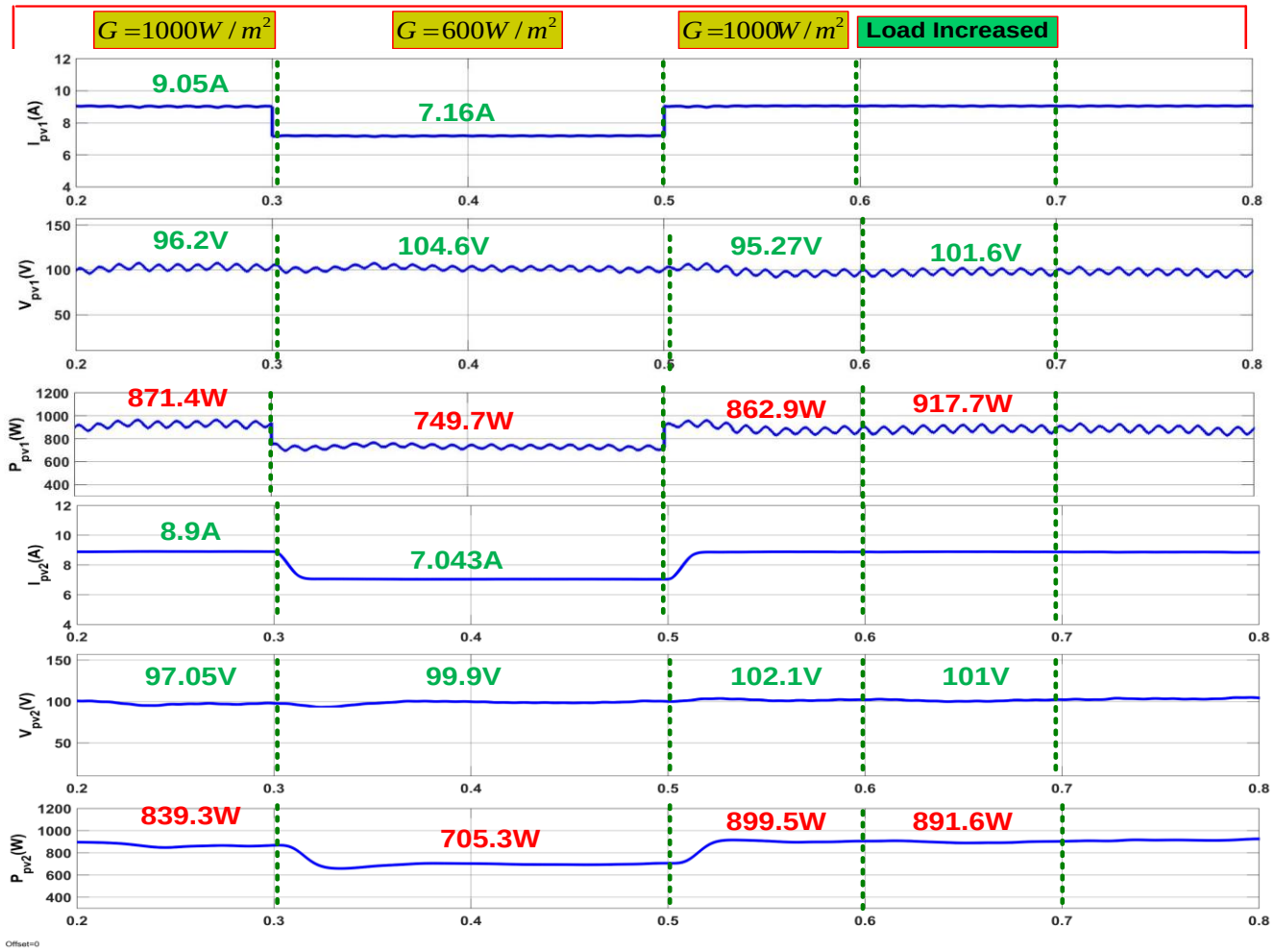



**Fig 7.5** Performance of Grid parameters during sudden irradiance variation and load for SRFT-PLL

During the initial period from 0≤t≤0.3s, at an irradiance of 1000W/m$^2$, the load power requirement is ($P_L$= 158.2W,$Q_L$= 32.53VAR), which is satisfied by the power generated from PV- integrated compensator, i.e., 5-level CHB-MLI ($P_c$=1789W,$Q_c$=64.9VAR). The compensator's extra remaining active and reactive power is fed to the source (Ps=-1631W, Qs= -31.81VAR) and makes the system power factor unity and the grid current out of phase with grid voltage, as shown in Fig 7.6.

Thesolar irradiance is variedfrom ***0.3s ≤t ≤0.5s.*** ***A***t that time,the load power requirement remained unchanged; however, the compensator power altered the grid power, as shown in Fig 7.6.

Now, the load is varied at an irradiance of 1000W/m$^2$from 0.5s≤ t≤ 0.6s, as shown in Fig 7.6. During this interval, the load is increased, so the load demands additional active

power, but reactive power remains almost unaltered, i.e. ($P_L$= 205W, $Q_L$= 33.25VAR).The compensator power adjusts itself and satisfies the load power requirement, i.e.(Pc= 1771W, Qc= 67.57VAR).

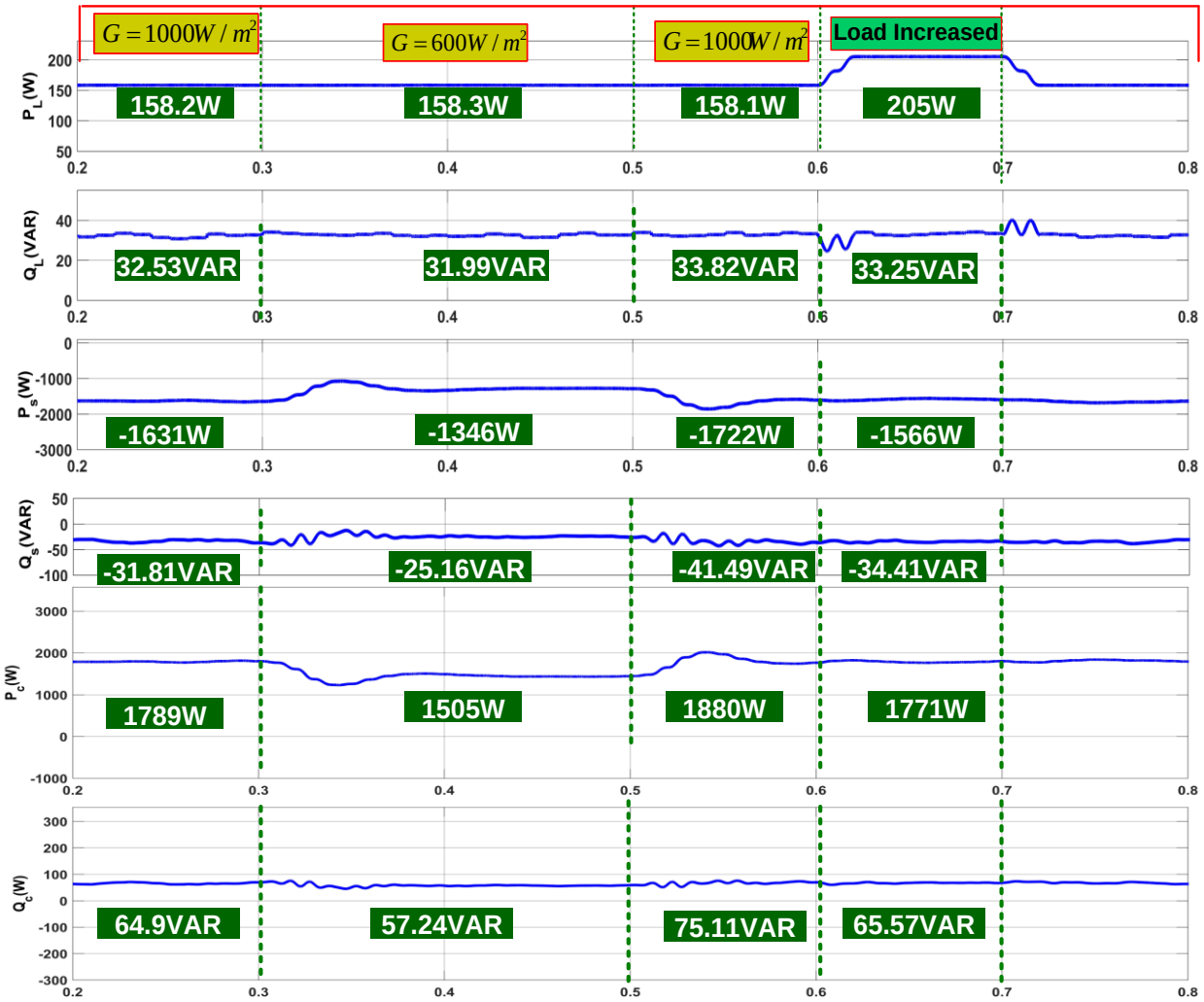



**Fig7.6** Simulation results of source power ($P_s$,$Q_s$), load power ($P_L$, $Q_L$), and compensating power ($P_c$,$Q_c$) under sudden variation of irradiance and load

The simulation results of grid voltage $v_g$(V), grid current $i_g$(A), load current $i_L$(A), and the total DC link voltage $V_{dc}$(V) have been shown in Fig 7.7 under varying solar irradiation and dynamic change in load during t=0.3s to 0.5s and t=0.5s to 0.7s respectively.PV arrays feed power to the grid, and since the power extracted is more than the load, the grid current is out of phase with respect to grid voltage, as shown in Fig 7.7.

However, during the transition in solar radiations from 1000W/m$^2$ to 600W/m$^2$, the small effect has been in total DC link voltages.

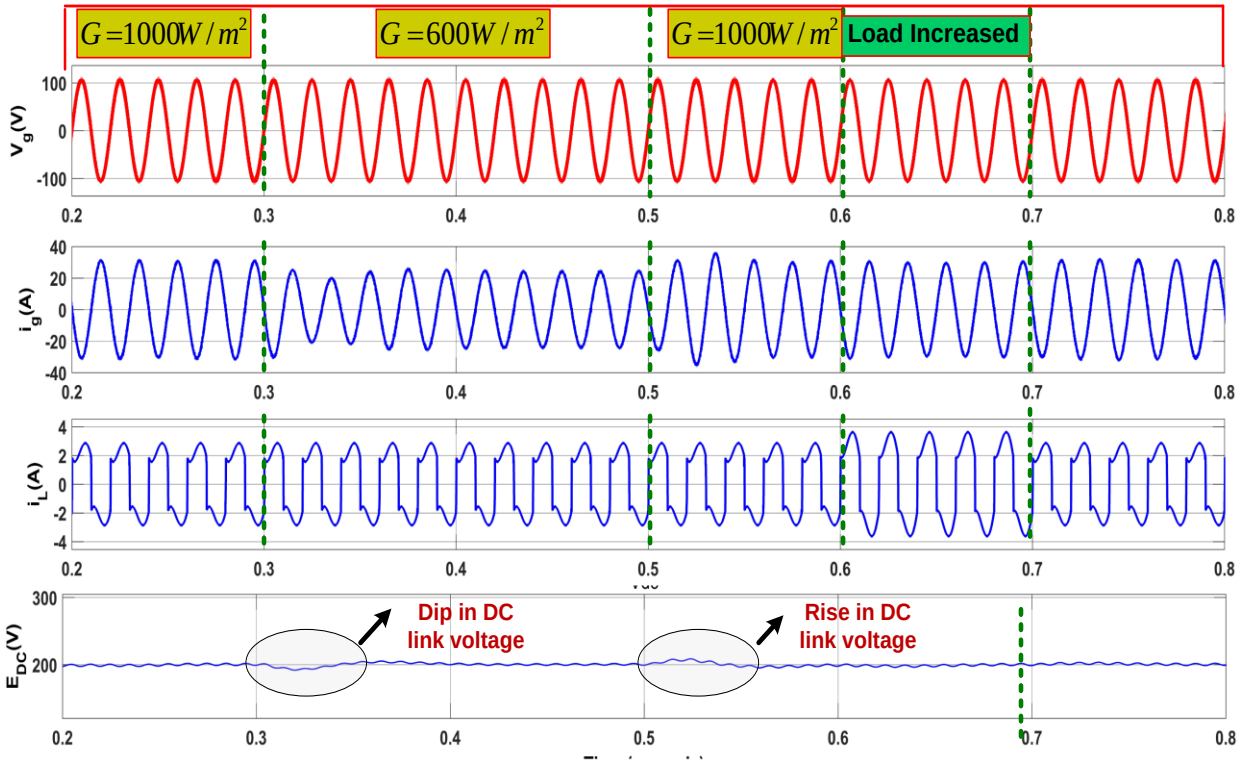



**Fig 7.7** Simulation of parameters for single phase grid connected system under varying solar irradiation and load with SRFT algorithm

### 7.2.2 Simulation Results of Single-Phase Single-Stage PV Array-based SRF-PLL under Distorted Grid Conditions

Now, the proposed system is tested under distorted grid conditions. The grid is simulated by considering some odd number of harmonics in the voltage and running the model in MATLAB/Simulink. During 0.2s ≤ t ≤ 0.6s, the grid is considered to be normal, and after t ≥ 0.6s, the grid is considered to be polluted, as shown in Fig 7.8. The solar irradiation varies from 1000W/m$^2$ to 600W/m$^2$ at t=0.3s and it is restored to 1000W/m$^2$ at t=0.5s. During the polluted grid conditions, the SRFT algorithms cannot free the source current from harmonic distortion to less than 5% limit. Therefore the THD (%) obtained inthegrid current $i_g$(A)is high.

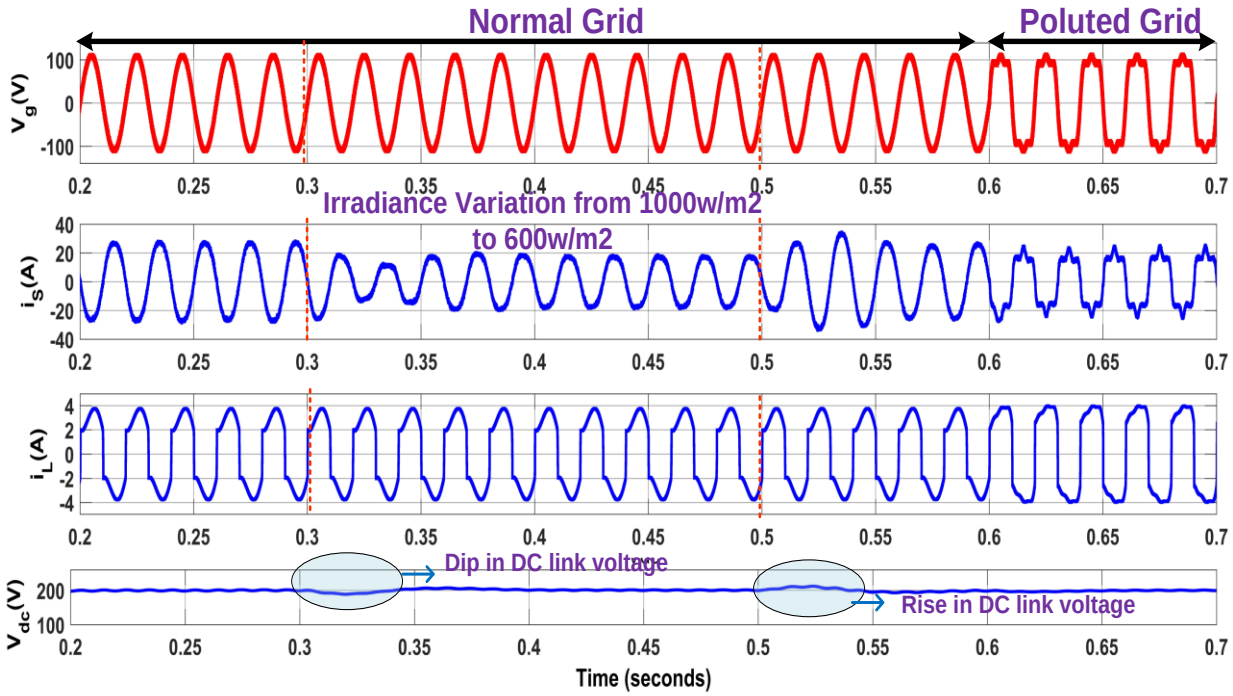



**Fig 7.8** Simulation results of single stage single phase PV array grid connected system under distorted grid conditions with SRFT algorithm

Fig 7.9 shows that during time interval t<0.3s, the source is receiving power from the compensator (Ps=-1538W, Qs=-26.36VAR), which means the PV array is feeding the active power to the grid and making the grid current out of phase w.r.t. grid voltage as clearly depicted in Fig 7.8.In addition, the reactive power requirement of load and source is met by the compensator as desired so that almost unity power factor is obtained on the grid side.

The solar irradiance is varied from ***0.3s ≤t ≤0.5s.*** *A*t that time,the load power requirement remained unchanged; however, the compensator's power self adjustsas shown in Fig 7.6.

Now, the load is increased at constant irradiance of 1000W/m$^2$ from 0.5s≤ t≤ 0.6s, as shown in Fig 7.9. During this interval, the load demands more active power, but reactive power remains unaltered, i.e. ($P_L$= 220.5W, $Q_L$= 35.8VAR). The compensator power active power is altered and satisfies the load power requirement, i.e.($P_c$= 1778W, $Q_c$= 71.12VAR) and the remaining power of compensator is fed to source i.e.($P_s$= -1557W, $Q_s$= -35.34VAR). The different levels of PV array output voltages ($V_{PV1}$ and$V_{PV2}$), output currents ($I_{PV1}$and $I_{PV2}$) and output powers ($P_{PV1}$and $P_{PV2}$) are depicted in Fig 7.10.

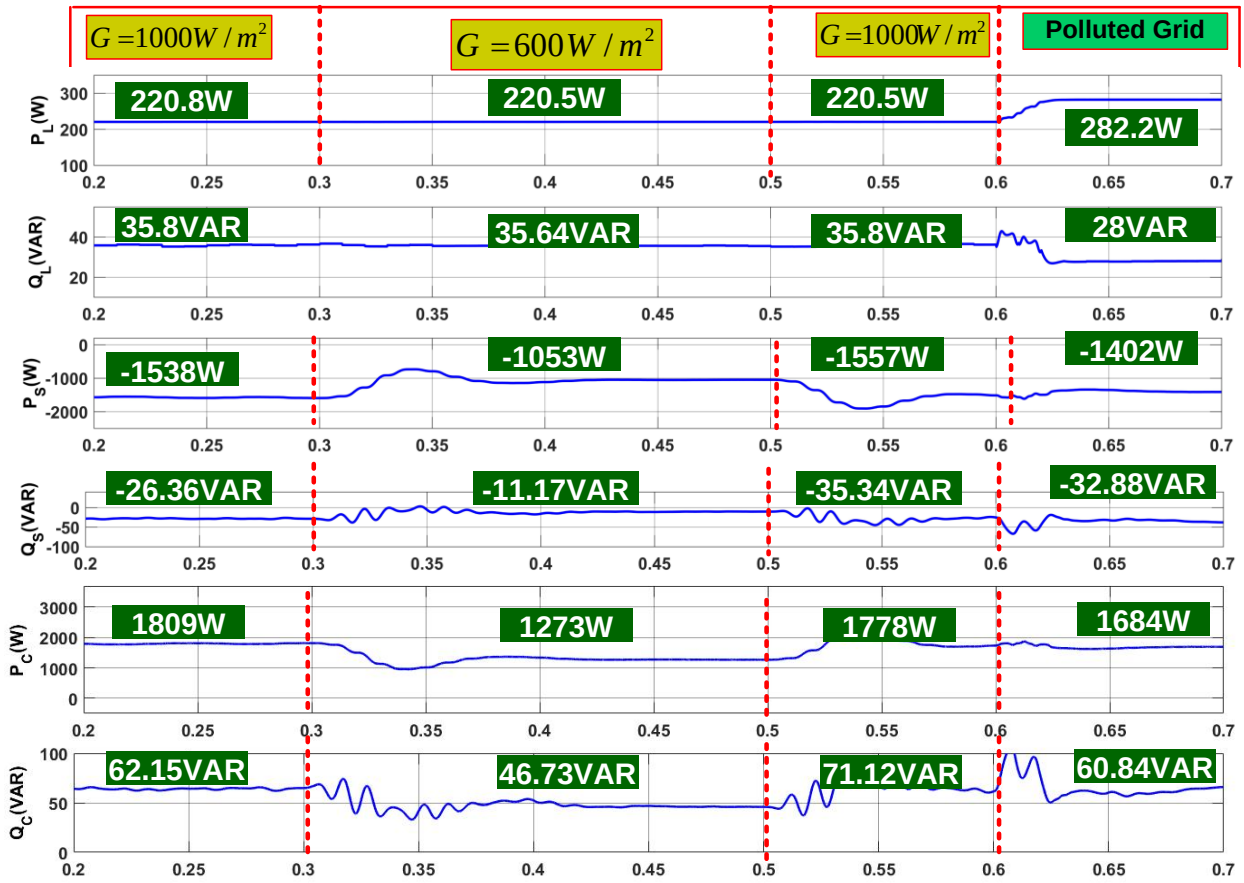



**Fig 7.9**Simulation of different levels of power received in the system

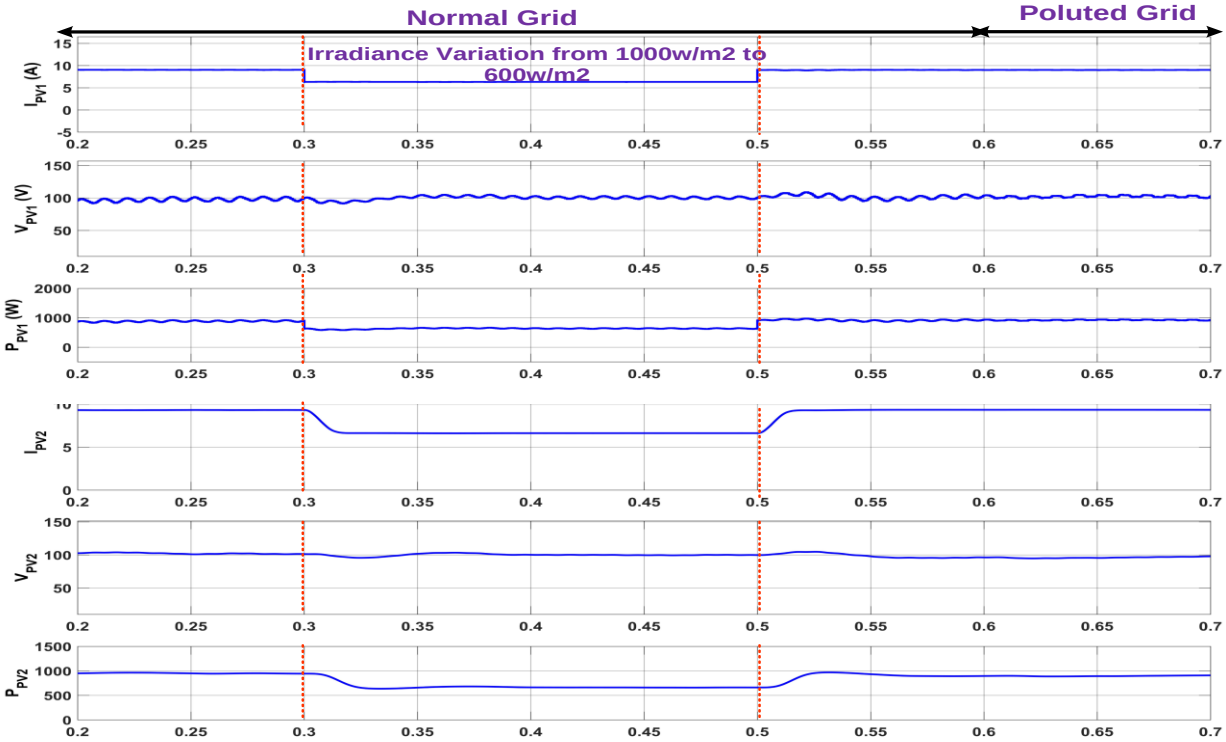



**Fig7.10**Simulated results of PV array output voltages ($V_{PV1}$, $V_{PV2}$), PV currents ($I_{PV1}$, $I_{PV2}$) and PV power ($P_{PV1}$, $P_{PV2}$) under normal and distorted grid conditions

The %THD performance of SRFT-PLL under normal grid conditions is shown in Fig 7.11(a-c), and for abnormal grid conditions are shown in Fig 7.11(d-f).During the normal grid conditions, the load current THD of 27.85% has been reduced to 4.23% for the grid current as shown in Fig 7.11(b-c). The obtained THD lies within IEEE-1547 standards. In this case, the grid voltage THD is found to be 1.51%, as depicted in Fig 7.11(a).

Now, the case of distorted grid conditions is considered. In this case, the voltage grid harmonics are computed to be 10.79%, as shown in Fig 7.11(d) and the load harmonics are found to be very high, about 36.86% as shown in Fig 7.11(f).The SRFT-PLL fails to estimate the sine and cosine templates correctly; therefore,the THD (%) of grid current is found to be very high i.e., 19.07%, as shown in Fig 7.11(e), under polluted grid conditions.

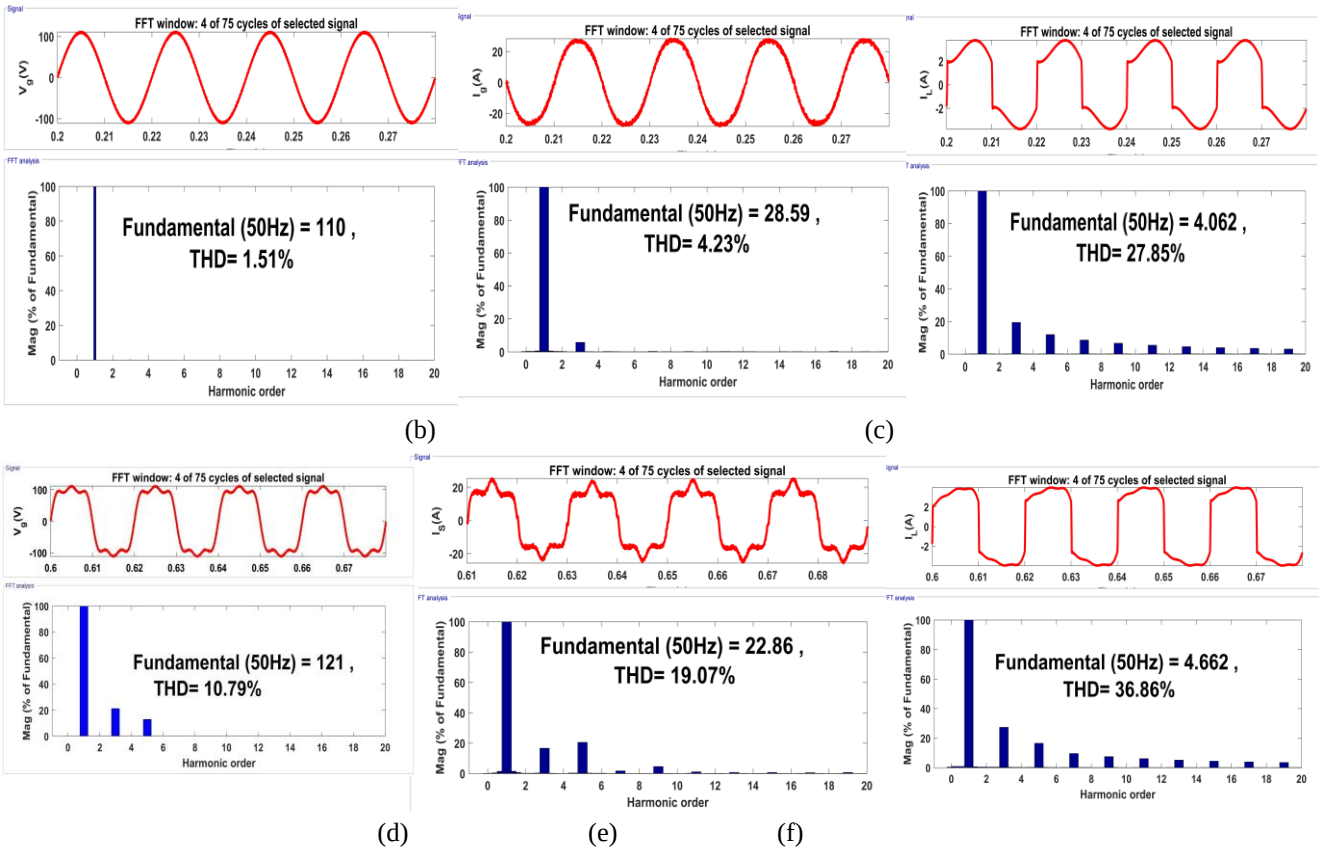



**Fig 7.11Case I(a-c) :** THD(%) performance (a)grid voltage $v_g$(V), (b)grid current $i_g$(A) and(c) Load current $i_L$(A) of single stage PV array with SRF-PLL under normal grid conditions **Case II(d-f):** THD(%) (d) grid voltage (e) grid current (f) load current under polluted grid conditions

### 7.2.3 Experimental Results OfSingle Phase Single StageIntegrated PV System-Based SRF-PLL under Normal Grid Conditions

The proposed system is modeled in MATLAB-Simulink and the results obtained have been experimentally verified using OPAT-RT. The experimental prototype model is shown in Fig 7.12.The outcomes of MATLAB simulations are confirmed by OPAL-RT controller-based hardware-in-loop (HIL) system implementation. OPAL-RT and MATLAB/Simulink work together well and validate different control algorithms considered in this chapter. It includes two primary components, viz., the RT-Lab simulation environment and the second is HIL platform. OPAL-RT engine has an FPGA processor, which works very fast in processing the signals.

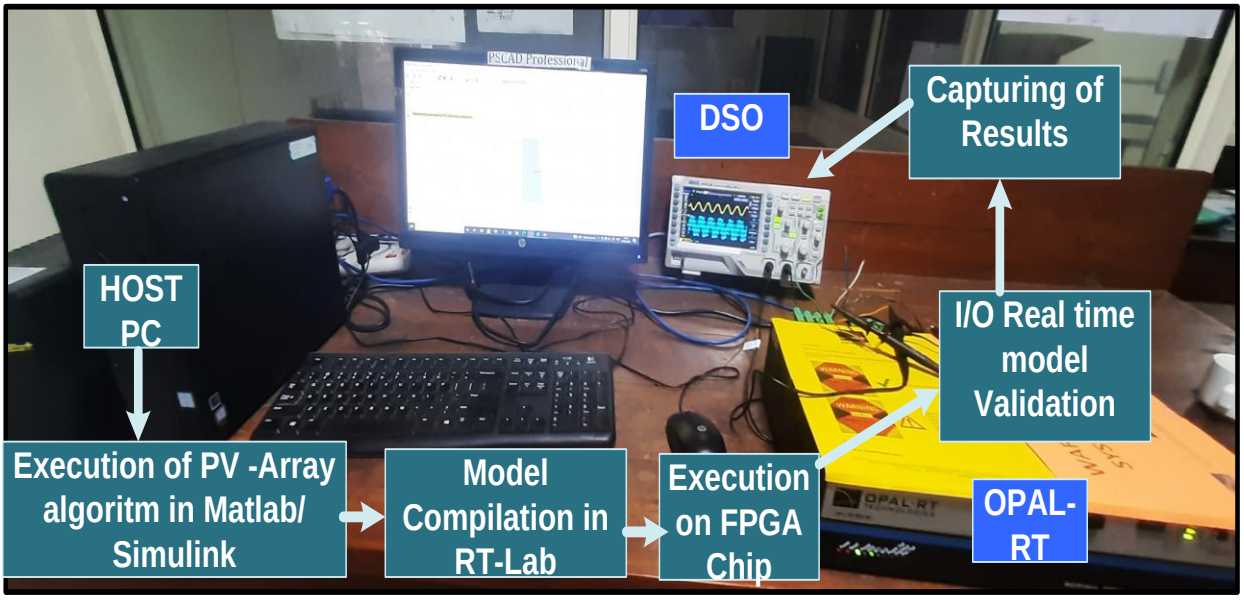



**Fig7.12** Experimental implementation of the proposed algorithm on OPAL-RT

Fig 7.13(a,b) shows the experimental results obtained using OPAL-RT. The solar irradiance is varied from 1000W/m$^2$ to 600W/m$^2$,and the intermediate signals viz. PV array-1 output voltage $V_{PV1}$(V), PV array-2 output voltage $V_{PV2}$(V), PV-1 and PV-2output current $I_{pv1}$and $I_{pv2}$are shown in Fig 7.13(a). The output rating of each PV array is 0.954kW.

Fig 7.13(b) shows the parameters viz. grid voltage $v_g$(V), grid current $i_g$(A), total DC link voltage $V_{dc}$(V), and load current $i_L$(A) during solar irradiance variation from 1000W/m$^2$ to 600W/m$^2$. It is observed that during irradiance variation, the DC link voltage quickly stabilizes to 200V within 1~2 cycles.

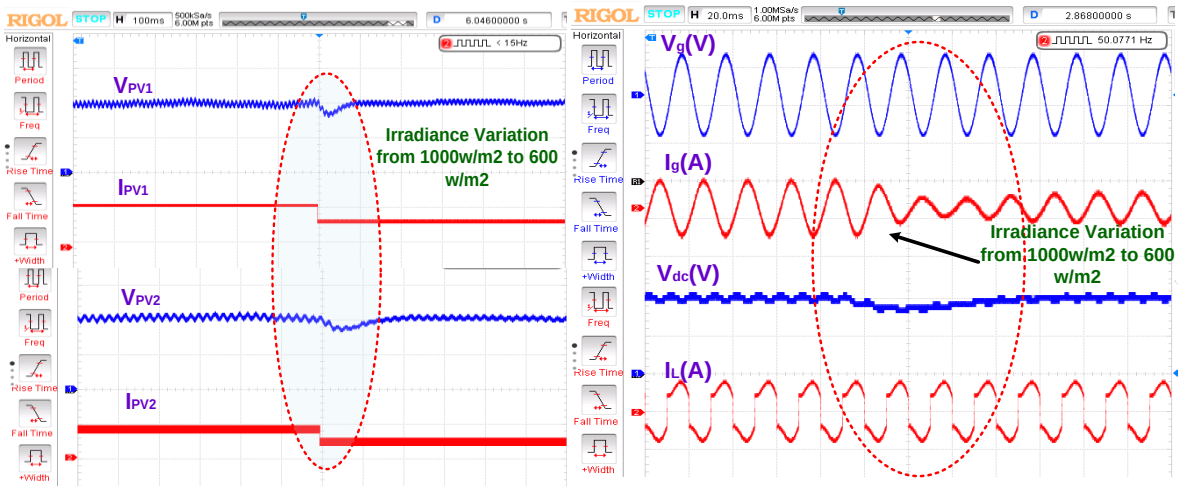



**Fig 7.13(a-b)** Experimental results of parameters for single phase grid connected SRF-PLL

Similarly, the active power received from PV arrays is shown in Fig 7.14.It is observed that during solar irradiance from 1000W/m$^2$ to 600W/m$^2$, a reduction in active power is observed from 870W to 749W, as depicted in Fig 7.14, but the power is quickly stabilized to a new steady state value.

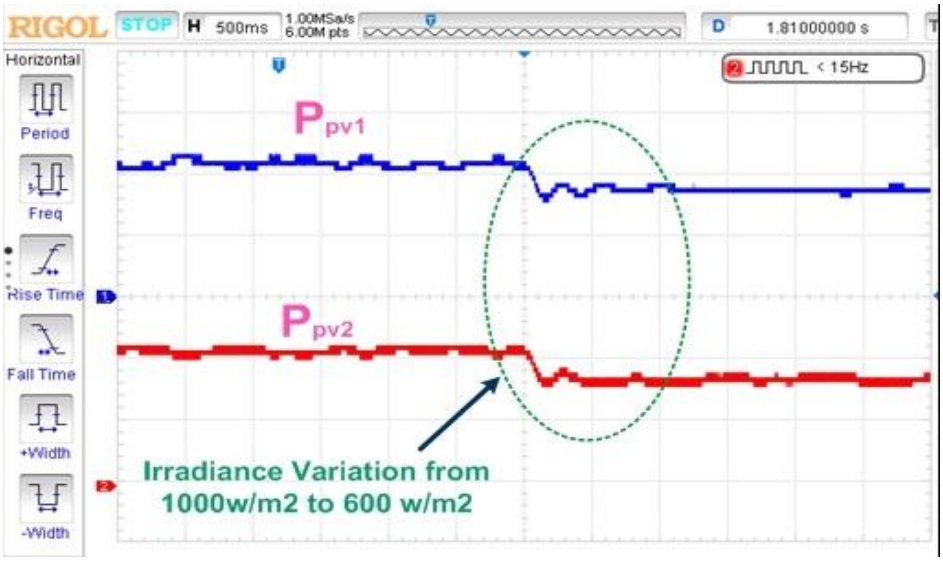
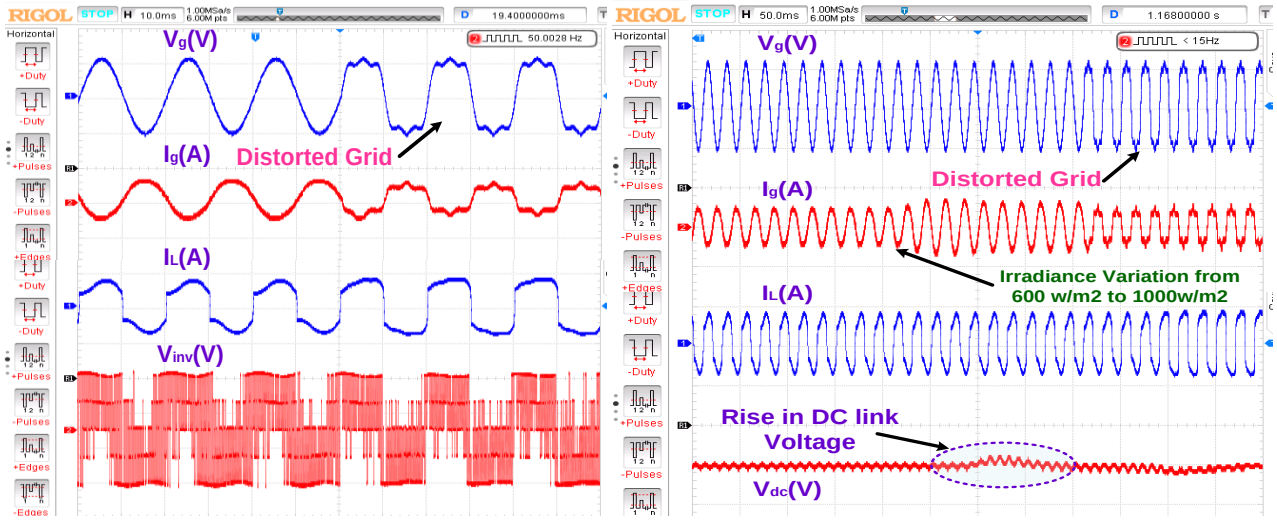



**Fig 7.14** Power outputs of PV arrays under irradiance variations from 1000W/m$^2$ to 600W/m$^2$

### 7.2.4 Experimental Results of Single Phase Single-Stage Grid Connected PV System under Distorted Grid Conditions with SRFT-PLL

The single-stage grid-connected system is now tested experimentally for distorted grid conditions. Fig 7.15(a-b) shows the experimental results obtained during the polluted grid.SRFT-PLL performance is unsatisfactory underpolluted grid conditions. The THD(%) obtained in the grid current is 19.07%, which does not lie within IEEE-1547 standards (<5%).However, the settling time of DC link voltage is quite good under varying solar irradiance, as shown in Fig 7.15




(a) (b)

**Fig 7.15** Experimental results of Single stage single phase PV array grid integrated SRF-PLL

## 7.3 Performance ofPV integrated Single Phase SAPF using MNFSOGI-PLL

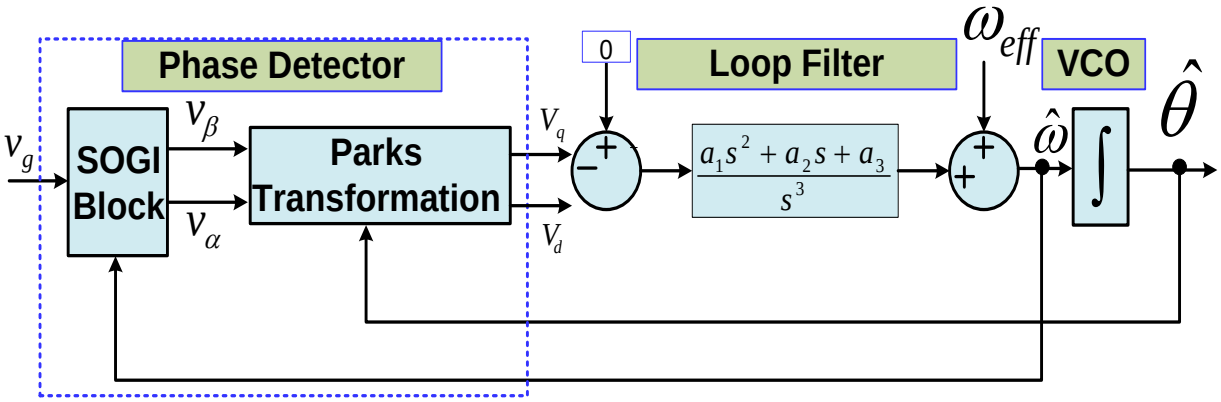
This section considers the impact of various grid abnormalities, viz. DC offset, voltage sag or swell, phase shift, and frequency variations. The accurate estimation of phase, frequency, and voltage is necessary to implement PV array grid-connected systems effectively.Furthermore, the grid synchronization of voltage source converters (VSIs) and phase lock loop (PLLs) circuits play a crucial role in the system.

For polluted grid systems, the PLL technique is required to accurately estimate phase, frequency, and voltage. In the previous section, the SRF-PLL was implemented to for the generation of unit templates and to handle the grid abnormalities. But it was observed

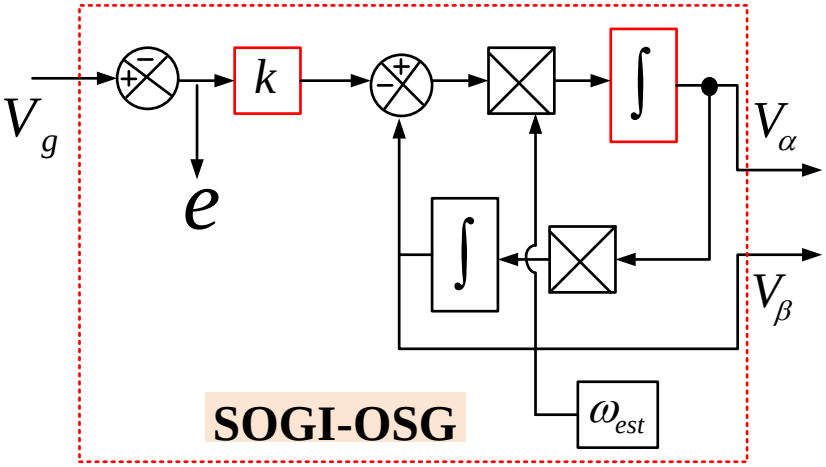
that the tracking performance of SRF-PLL is relatively poor, resulting inthe grid current having a high THD (%) under distorted grid conditions. In recent years, orthogonal signal generator (OSG) based PLL has been widely used and implemented to handle various grid abnormalities. Its tracking performance is quite good and accurate compared to SRF-PLL. OSG-PLL, Second Order Generalized Integrator (SOGI-PLL)retrain their performance even in various grid abnormalities and are widely used by researchers or power engineers for the grid-connected system.

But it is well known that SOGI-PLL cannot handle the DC-offset disturbances in the grid. This effect deteriorates the tracking performance of SOGI-PLL. Therefore, the phase and frequency estimation contain an error of significant deviation—accordingly, a new PLL, viz. Modified Notch Filter SOGI-PLL(MNFSOGI-PLL) has been discussed, which not only takes care of DC offset voltages but also shows rejection capability of inter-subharmonics. The dynamic performance of MNFSOGI-PLL has been observed under various grid abnormalities, viz. voltage sag/swell, DC offset, polluted grid, and phase shift conditions. Later, the MNFSOGI-PLL is implemented for a single-phase, single-stage grid-connected PV array system to extract the fundamental load current component and generation of reference current under non-linear load with the normal and distorted grid.

The typical generalized structure of conventional SOGI-PLL is shown in the Fig. 7.16(a,b). As shown in Fig 7.16(a), the loop filter plays a crucial role in reducing the phase error to zero and obtaining the estimated frequency $\hat{\omega}$ andangle $\hat{\theta}$. It is a second-order transfer function, and the steady state and dynamic performance depend on the functioning ofthe loop filter.




(a)




(b)

**Fig 7.16** Generalized structure (a) SOGI-PLL block (b) SOGI block

A generalized block diagram of Modified Notch Filter-SOGI-PLL is shown in Fig 7.17.The DC offset mainly affects the quadrature output signal of SOGI. So the transfer function model for quadrature signal is represented using the transfer function relating $V_{\beta 1}(s)$ to $V_g(s)$ given below:

$$T(s)=\frac{V_{\beta 1}}{V_g}\frac{k\,\omega_{eff}\;s(\omega_{eff}-s)}{(s+\omega_{eff})(s^2+k\omega_{eff}\,s+\omega_{eff}^2)} \tag{7.9}$$

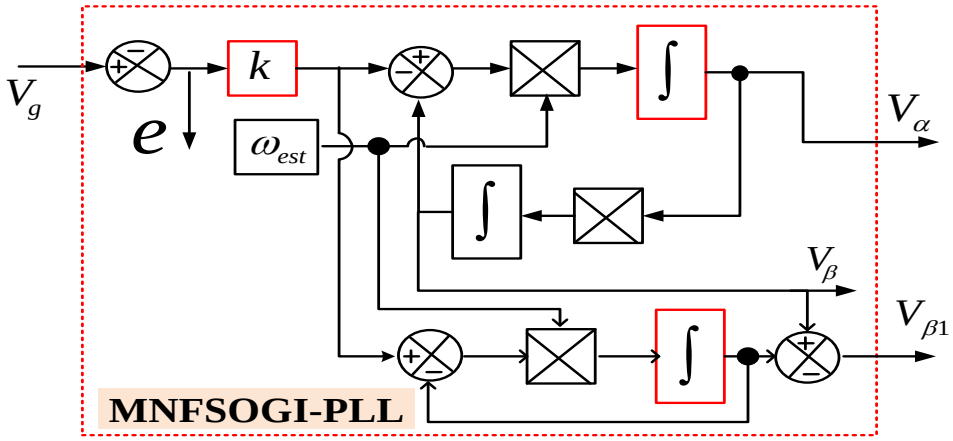



**Fig7.17** Generalized block diagram of MNFSOGI-PLL

In the quadrature component, an additional loop with an integrator is added to handle the DC offset component, as shown in Fig 7.17. In Equation 7.9,there is a trade-off to choose the value of k properly. It has been observed that large value of k will have a fast dynamic response, but the filtering effect is worse. Hence for the considered system, the

value of k is selected to be 1.42. The complete block diagram of the MNFSOGI-PLL is shown in Fig 7.18. Here, the output of the $w_{eff}$ is fed back to the MNFSOGI-PLL phase detector block to improve the dynamic performance. The loop filter shown takes care of various grid abnormalities like voltage sag/swell, polluted grid, phase shift issues, and DC–offset disturbances.

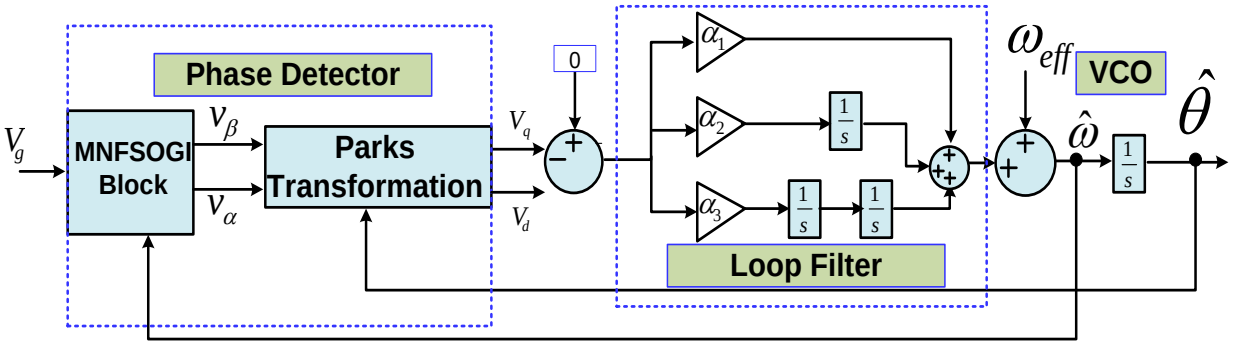



**Fig 7.18** Block diagram of MNFSOGI-PLL

In this case, the grid voltage is considered to have a phase shiftof $\pi/2$ during $t_1$=0.1s to $t_2$=0.2s, and 20% of DC offset is added in the grid during $t_3$=0.35s to $t_4$=0.45s as shown in Fig 7.19. It is observed from the Fig that the MNFSOGI-PLLdoesn't showpeak-to-peak frequency overshoot, and the undershoot is also to be significantly less. Negligible oscillations with peak-to-peak amplitude $A_{vpp}$ (V) wasobserved in amplitude tracking. In addition, during the case of 20% DC –offset, the fluctuations seen in $\Delta f$ and $A_{vpp}$ (V)arenegligibleas compared to SRF-PLL and SOGI-PLL.

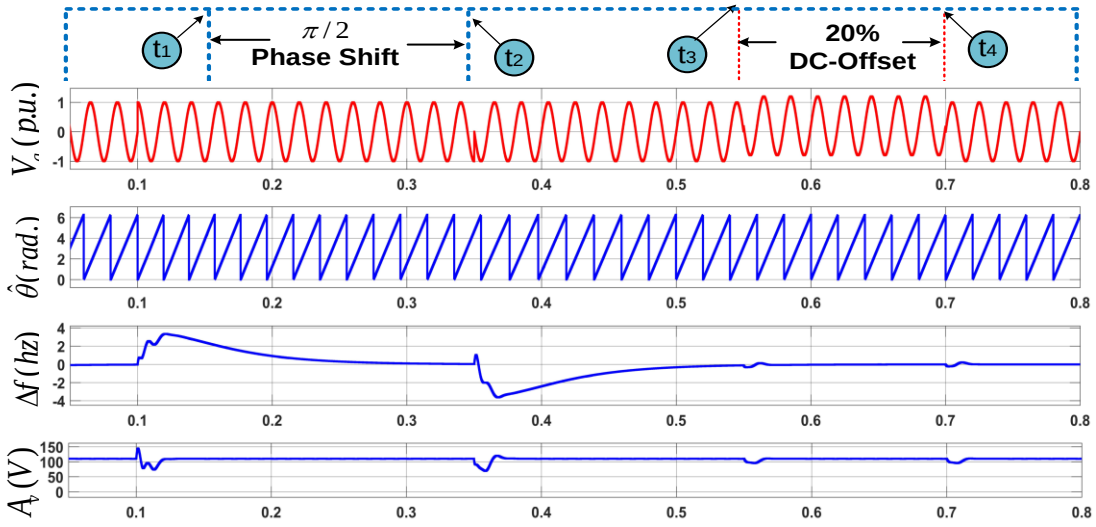



**Fig 7.19** Simulation performance of SOGI-PLL under $\pi/2$ phase shift and 20% DC - Offset

The voltage swellof 0.2 per unitis considered during $t_1$=0.1s to $t_2$=0.2s, and distortion in rid voltage during $t_3$=0.35s to $t_4$=0.45s, as shown in Fig 7.20.As observed from Fig 7.20, the peak-to-peak frequency estimation and the peak-to-peak amplitude oscillations during voltage swell are observed to be less with MNFSOGI-PLL. Similarly, in the case of grid distortion,almost negligiblefluctuations are visible in $\Delta f$ and $A_{vpp}$ (V). The MNFSOGI-PLL correctly estimates the phase angle $\hat{\theta}$.

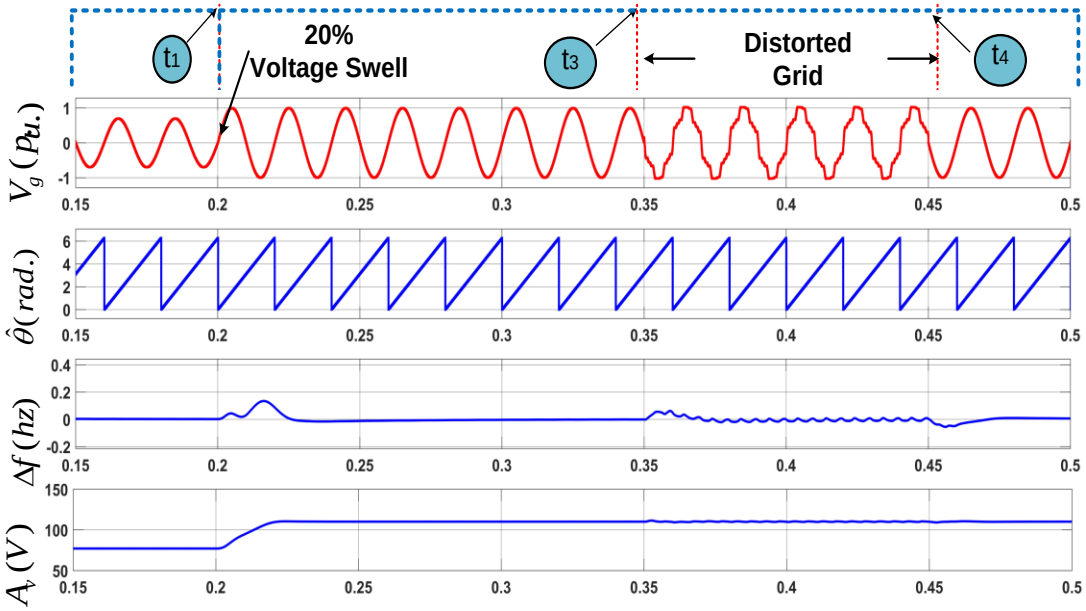



**Fig 7.20** Simulation performance of MNFSOGI-PLL under 20% voltage sag and distorted grid

### 7.3.1 Simulation results with Single-Phase Single Stage PV Array-based MNFSOGI-PLL underNormal Grid Conditions

The simulation results of grid voltage $V_g$(V), grid current $i_g$(A), load current $i_L$(A), and the total DC link voltage $V_{dc}$(V) for the MNFSOGI-PLL has been shown in Fig7.21 under varying solar radiation and dynamic changes in load during t=0.3s to 0.5s and t=0.5s to 0.7s respectively. PV arrays feed power to the grid; therefore, the grid voltage waveform is observed to be out of phase with respect to grid voltage, as shown in Fig 7.21. However, during the transition in solar irradiations from 1000W/m$^2$ to 600W/m$^2$the DC link voltage remains the same and well regulated.

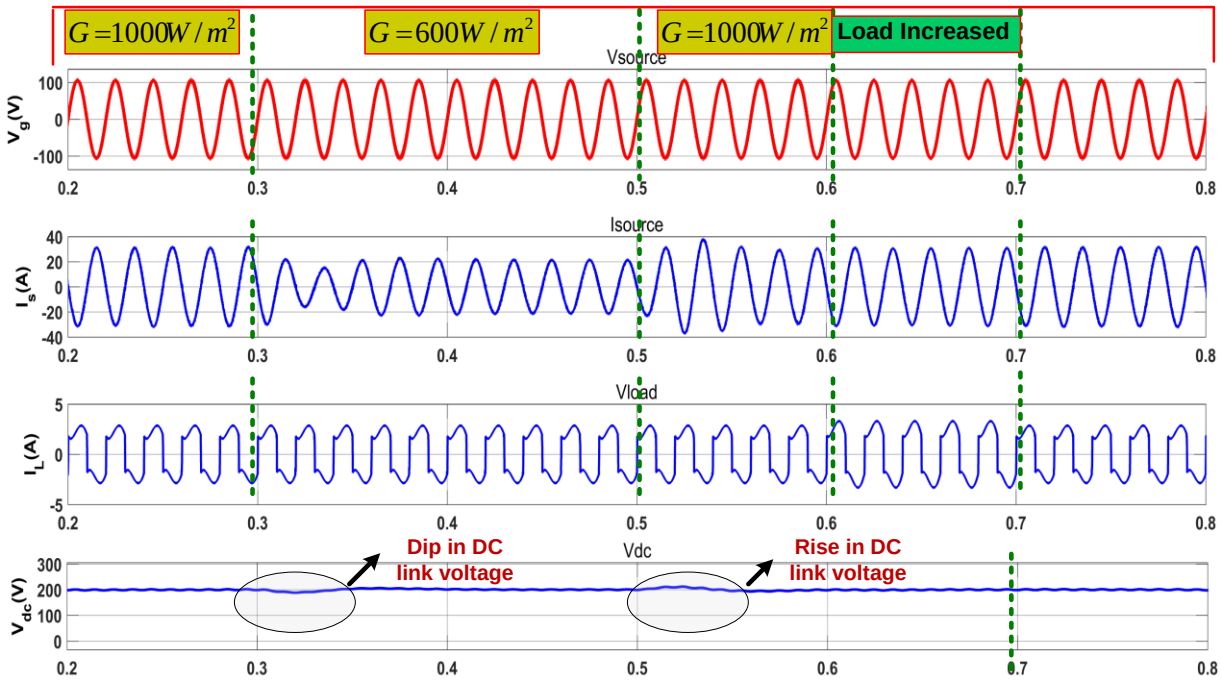



**Fig 7.21** Simulation of parameters for single phase grid connected system under varying solar radiation and load

The performance of PV array output current and voltages obtained during the different modes of operations is shown in Fig 7.22. It depicts the results of grid voltage $v_g$(V), grid current $i_g$(A), load current $i_L$(A), and total DC link voltage $V_{DC}$(V) with a change in solar irradiance of 1000W/m$^2$to 600 W/m$^2$ dynamic load conditions during normal grid conditions.

From Fig 7.22 at time interval t=0.3s, the solar irradiance is varied from 1000W/m$^2$ to 600W/m$^{2,}$ and t=0.5s again resumes to 1000 W/m$^2$. It is observed that then the amount of solar PV currents extracted from panels decreases during variation of solar irradiance from 1000W/m$^2$ to 600W/m$^2$. However, a very nominal rise has been observed on PV array open circuit voltages viz $V_{pv1}$ and $V_{pv2,}$ as shown in Fig7.22. The output PV power is also reduced due to irradiance variation.

Now, during load variation during t=0.6 to 0.7s, no variation is seen in PV array output currents, but a minor variation in PV-array output voltages has been observed, due to which the PV array output power varies, as shown in Fig 7.22

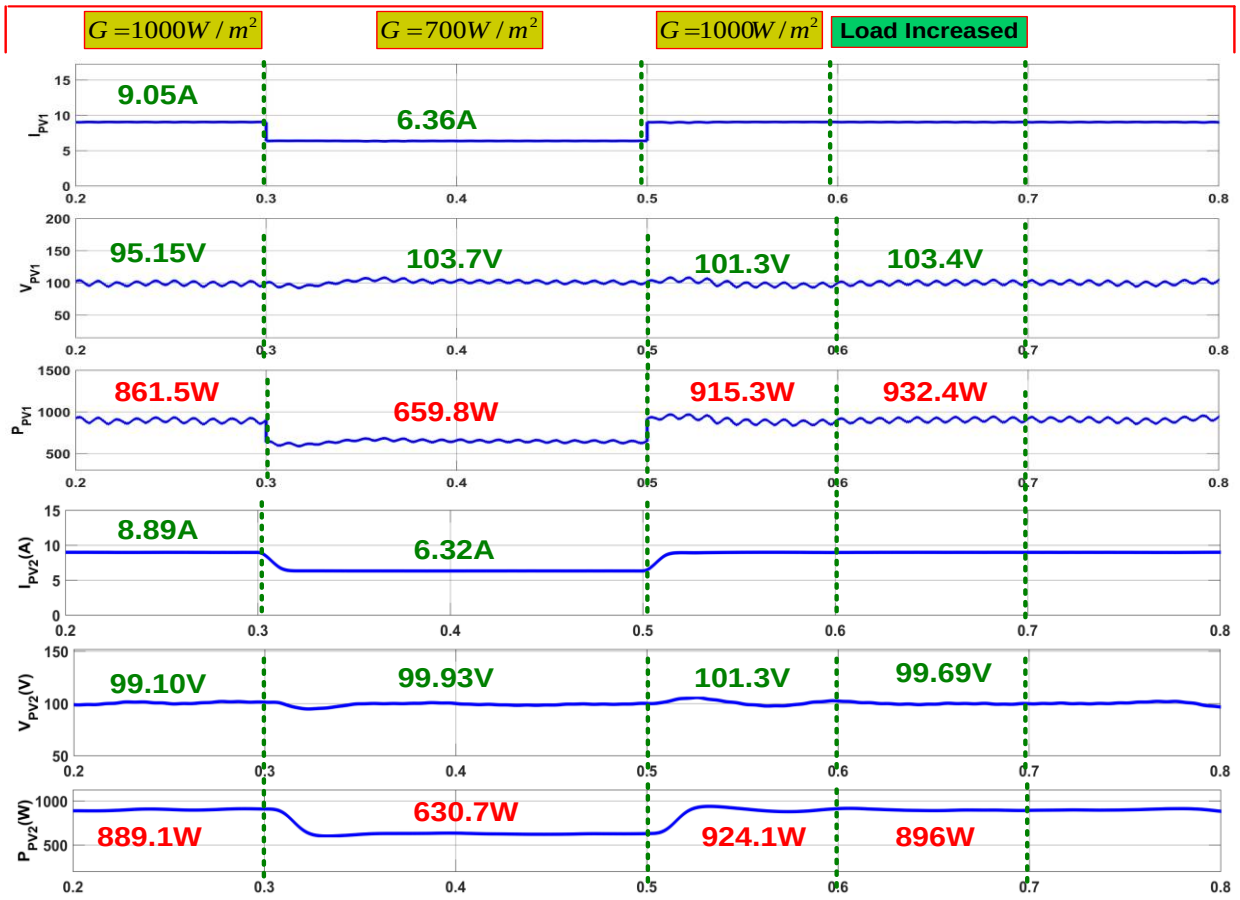



**Fig 7.22** Performance of grid parameters during sudden irradiance variation and load with MNFSOGI-PLL

During the initial period from 0≤t≤0.3s, at an irradiance of 1000W/m$^2$, the load power requirement is ($P_L$= 158.3W, $Q_L$= 32.56VAR), which is satisfied by the power generated from the PV-integrated compensator, i.e., 5-level CHB-MLI ($P_c$=1782W, $Q_c$=78.41 VAR). The compensator remaining active and reactive power is fed to the source (Ps=-1624W, Qs= -46.16VAR) and makes the system power factor unity and the grid current out of phase with grid voltage, as shown in Fig 7.23

The solar irradiance varies from ***0.3s ≤t ≤0.5s. A***t that time,the load power requirement remained unchanged; however, the compensator power altered the grid power, as shown in Fig 7.23

Now, the load is varied at an irradiance of 1000W/m$^2$ from 0.5s≤ t≤ 0.6s, as shown in Fig 7.23. During this interval, the load is increased, so the load demands active power, but

reactive power remains unaltered, i.e. ($P_L$= 186.33W, $Q_L$= 33.44VAR). The compensator power adjusted itself and satisfied the load power requirement, i.e.(Pc= 1768W, Qc= 75.75VAR).

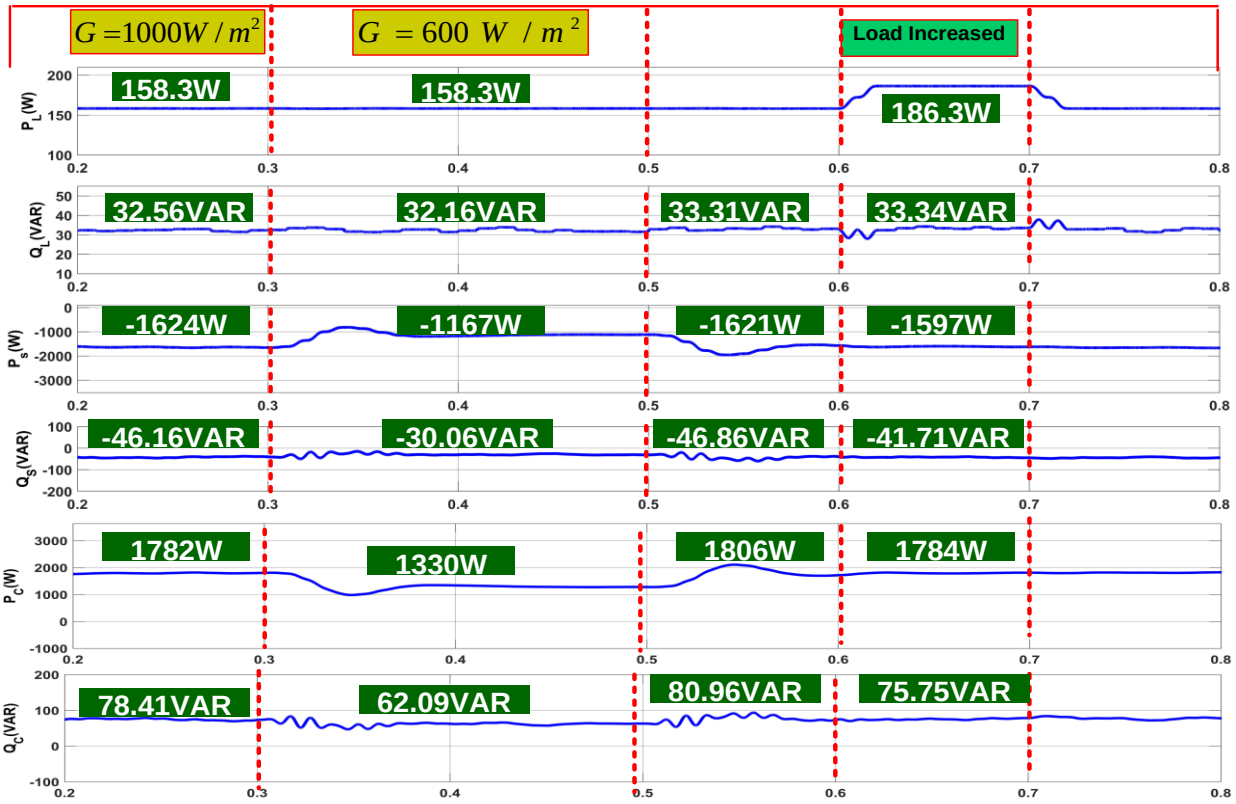



**Fig 7.23** Simulation results of source power ($P_s$,$Q_s$), load power ($P_L$, $Q_L$), and compensating power ($P_c$,$Q_c$) under sudden variation of irradiance and load

### 7.3.2 Simulations results with Single Phase Single Stage PV Array-based MNFSOGI-PLL underDistorted Grid Conditions

TheMNFSOGI-PLL algorithm is simulated and modeled in MATLAB/Simulink under distorted grid conditions. The grid is polluted by adding some odd number of harmonics in the simulation. During 0.2s ≤ t ≤ 0.6s, the grid is considered normal, and after t > 0.6s, the grid is considered polluted, as shown in Fig 7.24. The solar irradiation varies from 1000W/$m^2$ to 600W/m2 at t=0.3s and regains to 1000W/$m^2$ at t=0.5s.The reduction in solar

irradiance is considered during 0.3s ≤ t ≤ 0.5s, the grid current is sinusoidal and out of phase with the grid voltage.

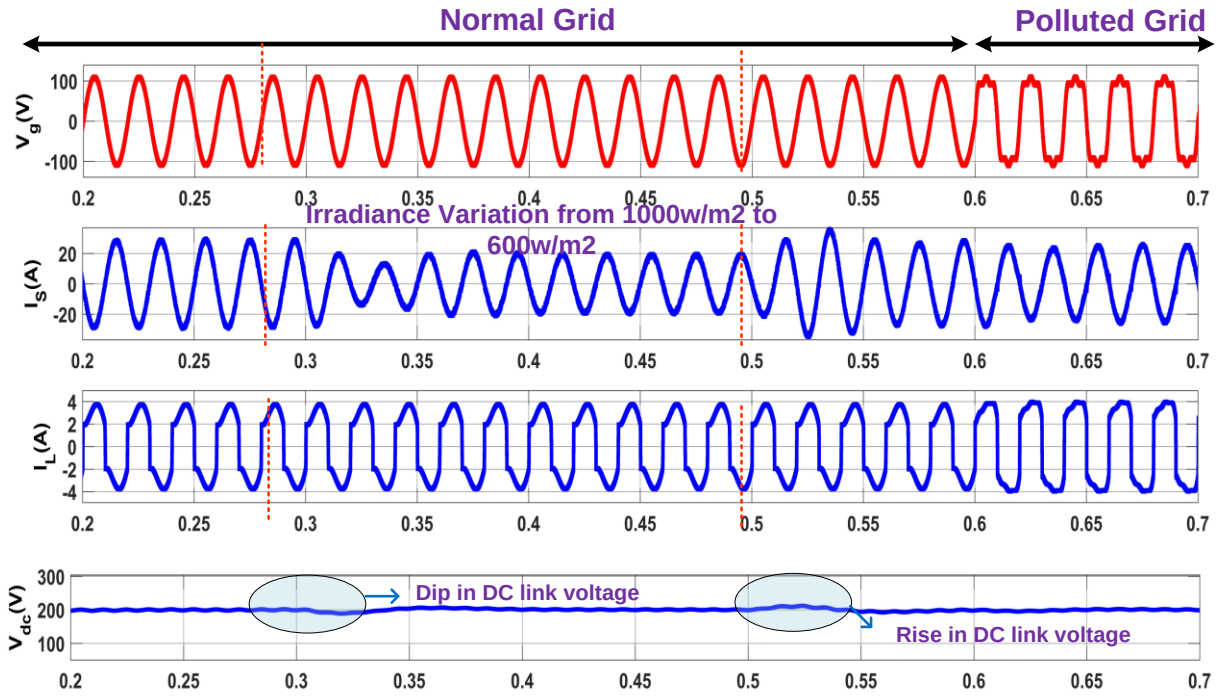



**Fig 7.24** Simulations results of single stage single phase PV array grid connected system under distorted grid conditions

Fig 7.25 shows that during time interval t<0.3s, the source is receiving power from the compensator ($P_s$=-1568W, $Q_s$=-39.99VAR), which means the PV array is feeding the active power to the grid and making the grid current out of phase w.r.t. grid voltage as clearly depicted in Fig 7.25. In addition, the reactive power requirement of load and source is met by the compensator so that almost unity power factor is obtained on the grid side.

The solar irradiance varies from ***0.3s ≤t ≤0.5s.*** At that time,the load power requirement remained unchanged; however, the compensator power generated altered the grid power, as shown in Fig 7.25

Now, the load is increased at an irradiance of 1000W/$m^2$ from 0.5s≤ t≤ 0.6s, as shown in Fig 7.25. During this interval, the load demands more active power, but reactive power remains unaltered, i.e. ($P_L$= 283.4W, $Q_L$= 27.74VAR). The compensator power active power altered and satisfied the load power requirement, i.e.(Pc= 1736W, Qc= 146.2VAR), and the

remaining power of the compensator is fed to the source, i.e.(Ps= -1465W, Qs= -118.7VAR).

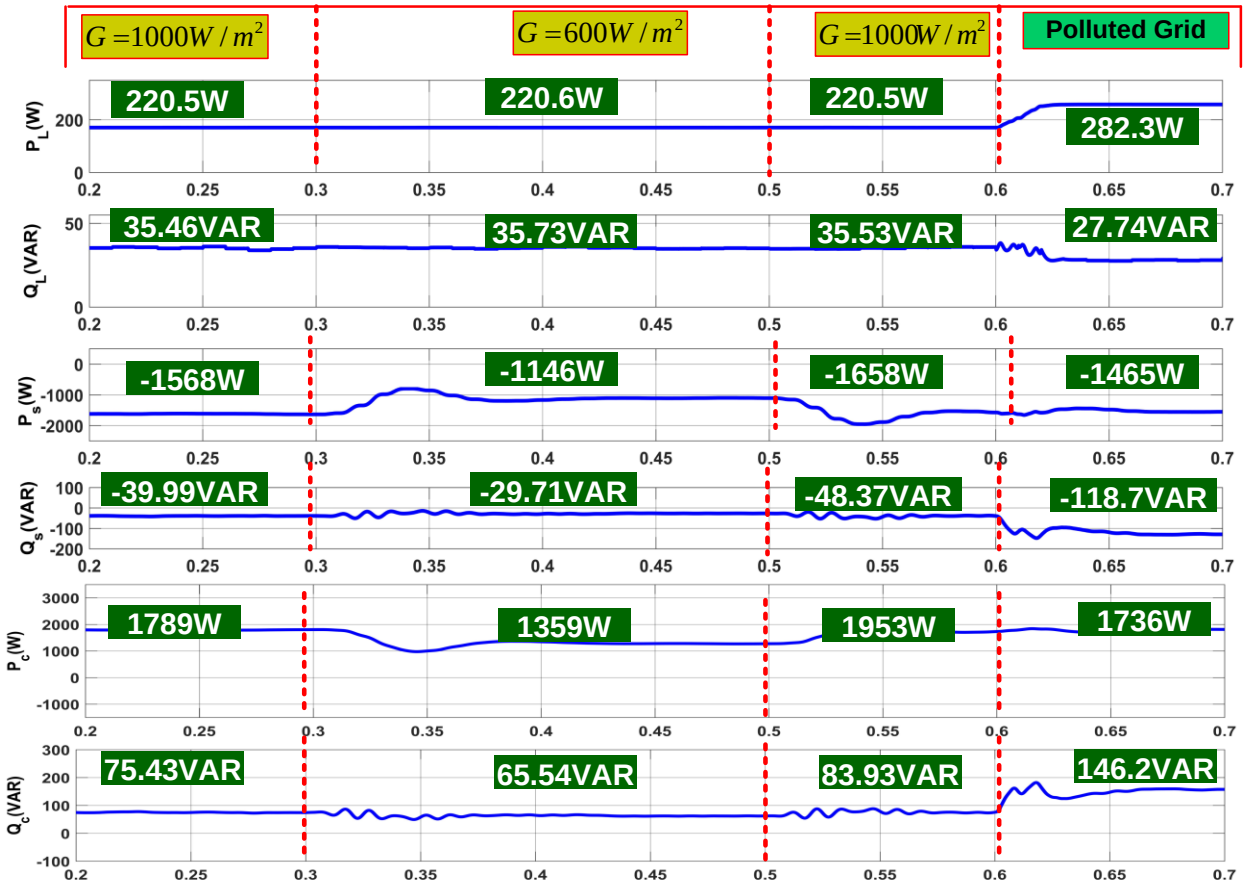
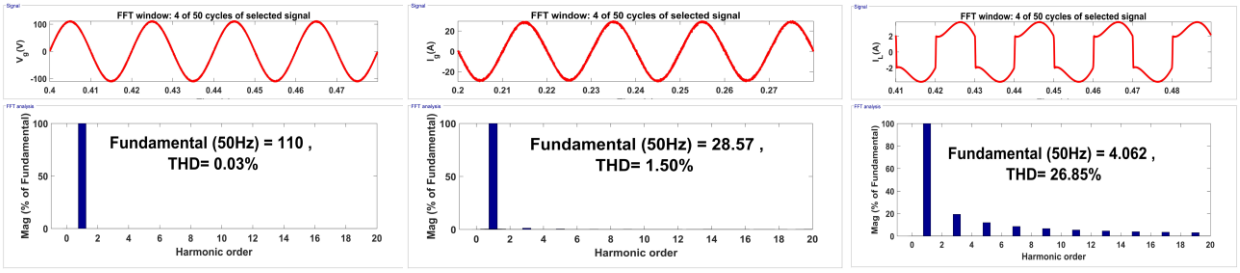


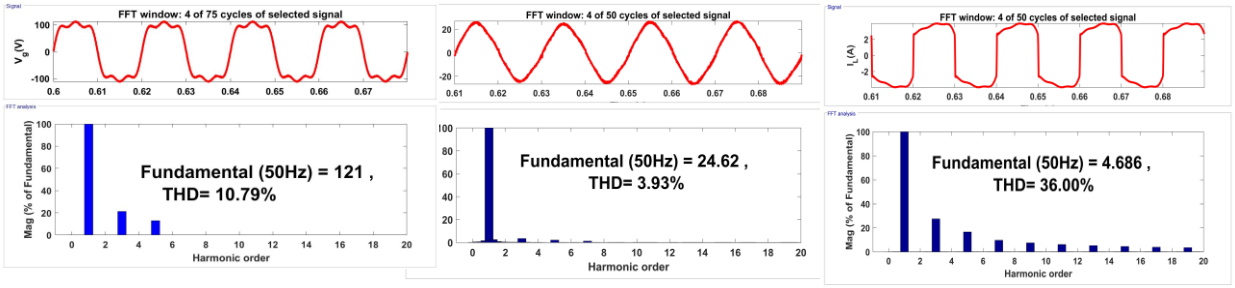

**Fig 7.25** Simulation of different levels of power received in the system

The %THD performance of SMNFSOGI-PLL under normal grid conditions are shown in Fig 7.26(a-c), and the abnormal grid conditions are shown in Fig 7.26(d-f). During the normal grid conditions, the load current THD of 26.85% has been reduced to 1.50% for the grid current, as shown in Fig 7.26(b-c). The obtained THD is within IEEE-1547 standards. In this case, the grid voltage THD is 0.03%, as depicted in Fig 7.26(a).

Now, consider the case of distorted grid conditions. In this case, the voltage grid harmonics are found to be 10.79%, as shown in Fig 7.26(d) and the load harmonics is found to be very high, about 36.86%, shown in Fig 7.26(f).The MNFSOGI-PLLaccuratelyestimates the sine and cosine templates correctly. Therefore, the THD (%) of grid current is low, i.e.,3.93%, as shown in Fig 7.26(e) under polluted grid conditions.




(a) (b) (c)




(d) (e) (f)

**Fig 7.26Case I-(a-c)** THD(%) performance (a)grid voltage $v_g$(V), (b)grid current $i_g$(A) and (c) Load current $i_L$(A) of single stage PV array with MNFSOGI-PLL under normal grid conditions

**Case II(d-f):** THD(%) (d) Grid voltage (e) grid current (f) load current under polluted grid conditions

### 7.3.3 Experimental Results of Single Phase Single Stage PV Array Based MNFSOGI-PLL under Normal Grid Conditions

Fig 7.27 (a,b) shows the experimental results obtained from OPAL-RT. The solar irradiance is varied from 1000W/m$^2$ to 600W/m$^2$ then the effect has been seen on parameters viz PV array-1 output voltage $V_{PV1}$(V), PV array-2 output voltage $V_{PV2}$(V), PV-1 and PV-2output current $I_{pv1}$and $I_{pv2}$ respectively as shown in Fig 7.27(b).

Fig 7.27(a) shows the parameters viz. grid voltage $v_g$(V), grid current $i_g$(A), total DC link voltage $V_{dc}$(V), and load current $i_L$(A) during solar irradiance variation from 1000W/m$^2$ to 600W/m$^2$.It is clearly observed that during solar irradiance variation, the DC link voltage quickly stabilizes to 200V within 1~2 cycles. The grid currentis sinusoidal but out of phase with the grid voltage.

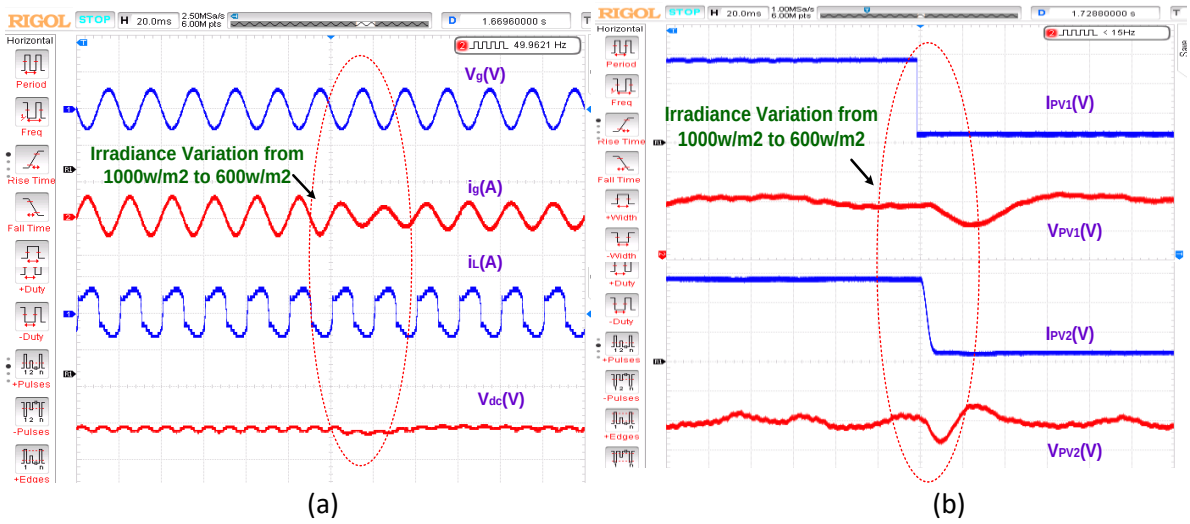



**Fig 7.27(a-b)** Hardware in loop results (a) grid voltage $v_g$(V) , grid current $i_g$(A), load current $i_L$(A) and DC link voltage $V_{dc}$(V) (b) PV array output voltage and currents under sudden varying solar irradiance

Likewise, the active power received from PV arrays is shown in Fig 7.28. It is observed that during solar irradiance from 1000W/m$^2$ to 600W/m$^2$, a reduction in active power injected by the PV panels as depicted in Fig 7.28, but the power is quickly stabilized to a steady state value. The active power is reduced from 871W to 749W.

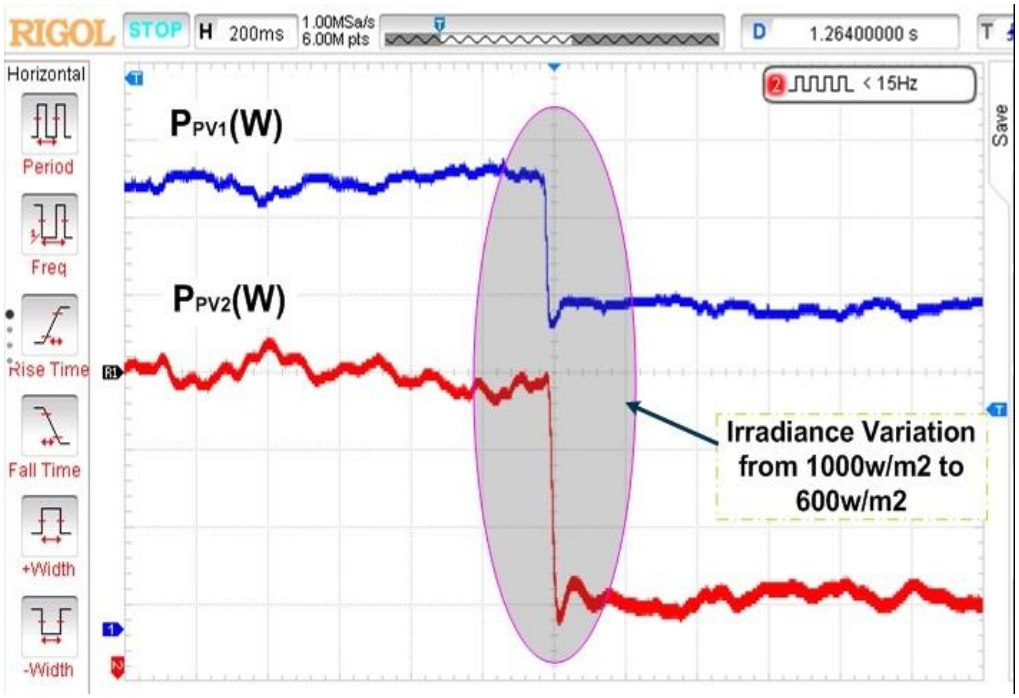



**Fig 7.28** PV array output powers ($P_{PV1}$and $P_{PV2}$) under varying solar irradiance

### 7.3.4 Experimental Results of Single Phase Single Stage PV Array Based MNFSOGI-PLL under Distorted Grid Conditions

The single-stage grid-connected PV system controlled by MNFSOGI-PLL is now tested experimentally under distorted grid conditions. Fig 7.29 shows the experimental results obtained during the polluted grid. The performance of MNFSOGI-PLL is satisfactory under polluted grid conditions.

The performance of grid voltage $v_g$(v) and grid current $i_g$(A) is shown in Fig 7.29. It is observed that during solar irradiance variation from 1000W/m$^2$ to 600W/m$^2$ the grid current varies accordingly, and it is out of phase with grid voltage which means the PV array is feeding power to the grid. In addition, under the distorted grid condition, the grid current is sinusoidal in shape with a THD(%) of 3.93%, which lie within IEEE-1547 standards (<5%). The effect in active and reactive power at the source and load side during variation of solar irradiance is depicted in Fig 7.30

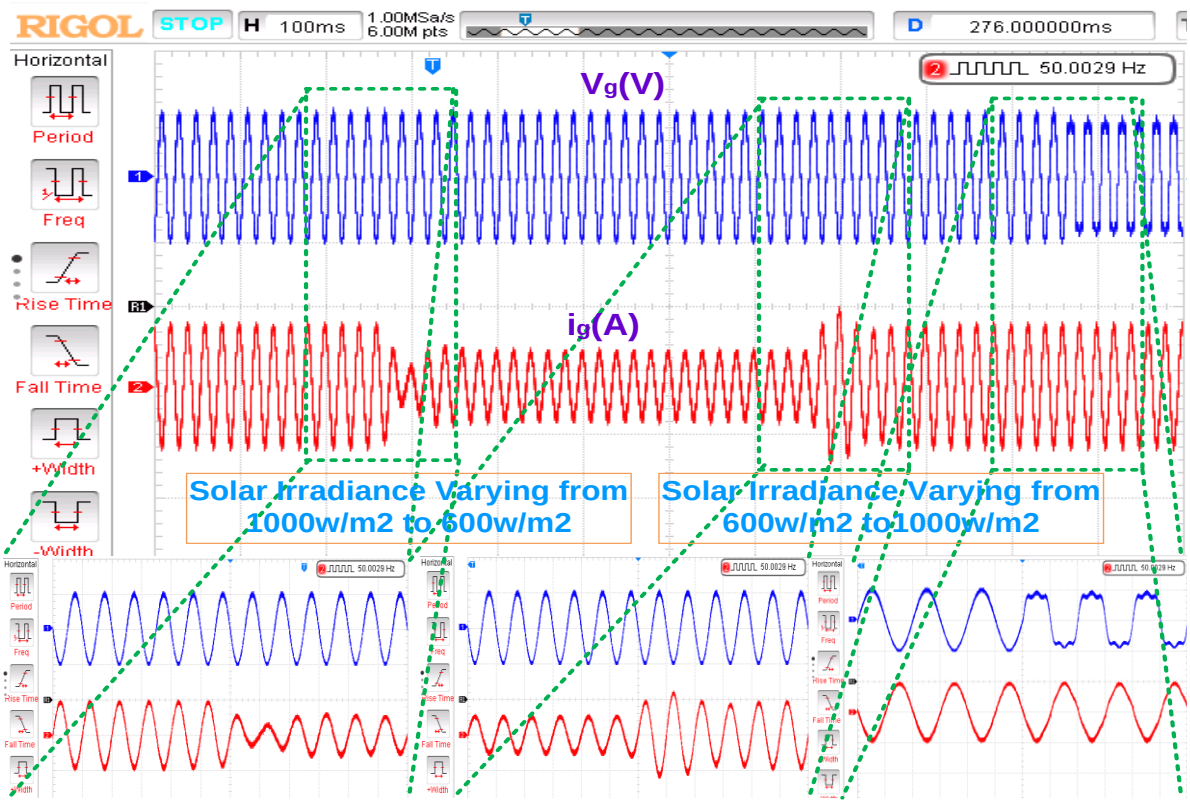



**Fig 7.29** Hardware in loop results of grid voltage $v_g$(V) and grid current $i_g$(A) under varying solar irradiance and polluted grid conditions

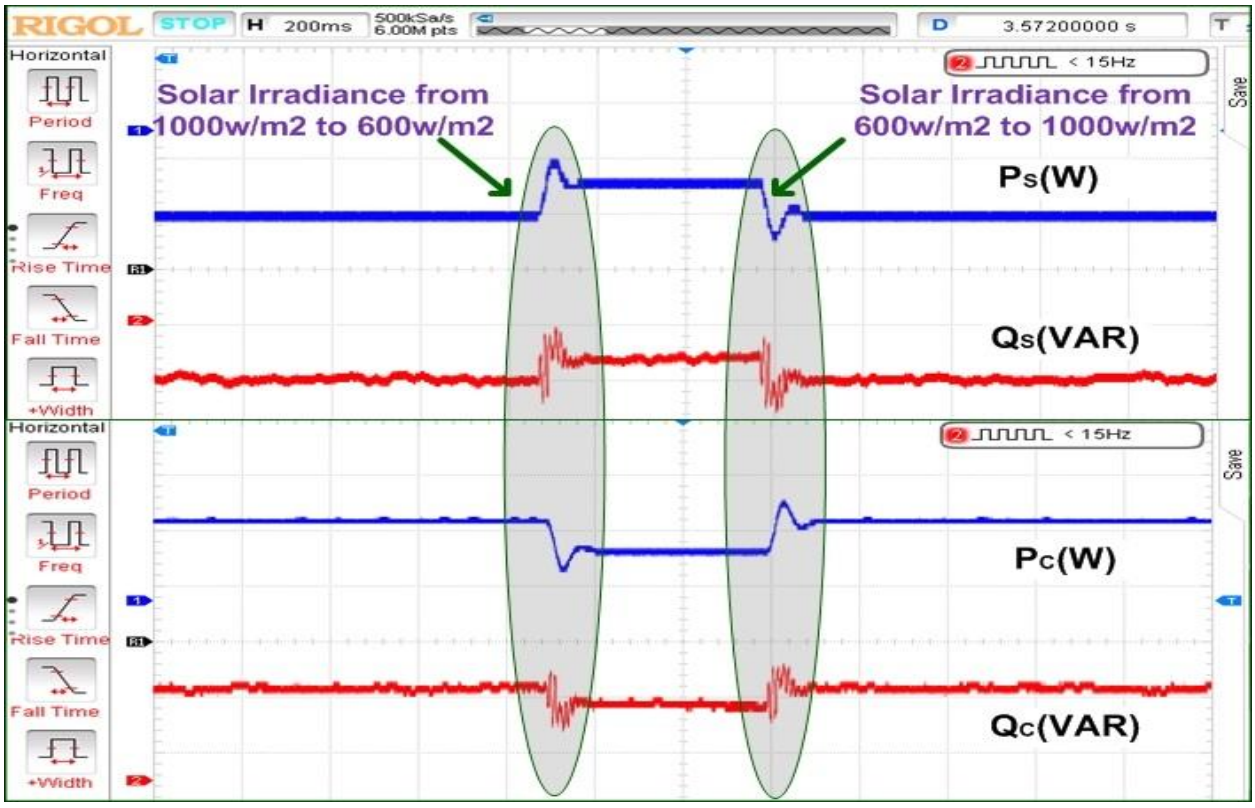



**Fig 7.30** Source and load side Active and Reactive power flow in proposed system

## 7.4 Comparative Performance of PLL Algorithm in Single Phase PV Integrated Grid Connected System

The performance of SRF-PLL, SOGI-PLL, and MNFSOGI-PLL are compared under various distortions suchas voltage sag and swells, phase shift, and DC offsetin the grid voltages. It is observed from Figs 7.31 and 7.32 that the SRF-PLL filter gives the worst performance underdistortedgrid and DC offset conditions. The SOGI-PLL works satisfactorily in distorted grid conditions, but its performance worsens under DC offset conditions.

It was observed that the MNFSOGI-PLL exhibits the best performance for amplitude and frequency estimation during the variation in grid voltage. MNFSOGI-PLL estimates frequency with high accuracy, but some delay in convergence is also observed. During the polluted and voltage sag/swell grid conditions, MNFSOGI-PLL and SOGI-PLL work satisfactorily to estimate frequency and amplitude. However, in the case of DC-offset

conditions, both SRFT and SOGI fail to estimate the accurate frequency and amplitude. The MNFSOGI-PLL gives negligible frequency and amplitude estimation oscillations even under DC-offset conditions and distorted grid cases, as shown in Figs 7.31 and 7.32.

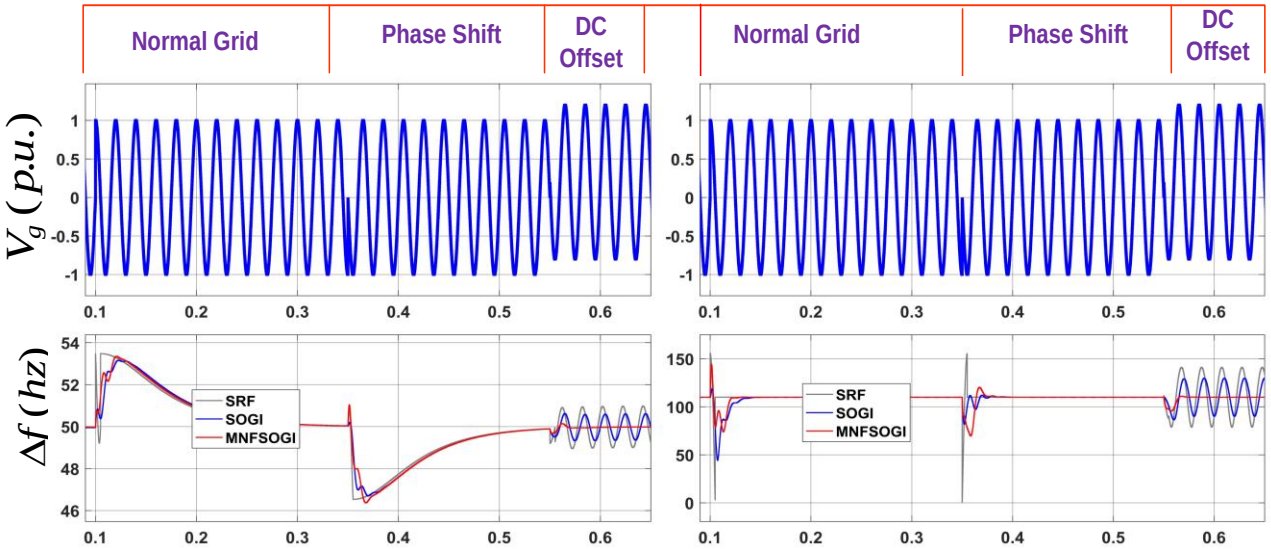



**Fig 7.31** Frequency and amplitude variation of SRF-PLL, SOGI-PLL, and MNFSOGI-PLL under phase shift and DC-offset

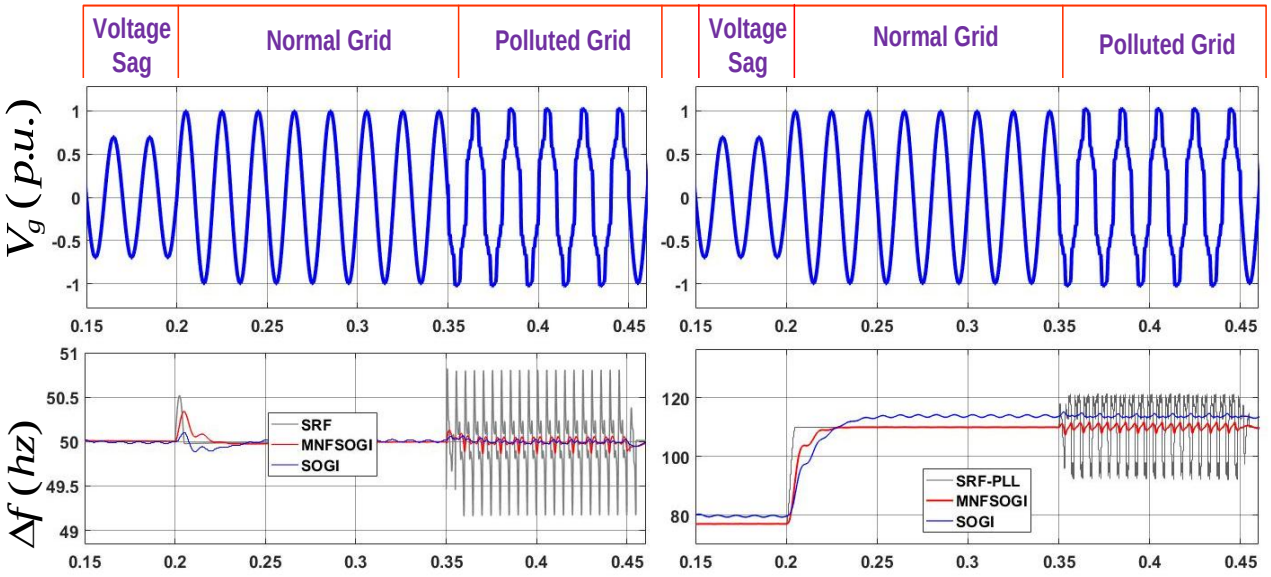



**Fig 7.32** Frequency and Amplitude Variation of SRF-PLL, SOGI-PLL,and MNFSOGI-PLL under voltage sag and distorted grid

## 7.5 Conclusion

In this chapter, the design and development of single-phase PV systems have been thoroughly covered. Experimental prototype setup, design equations, and system configuration have also been presented. In a single-stage, single-phase systemtwo identical PV arrays are interfaced to the DC link side of 5-Level CHB-MLI. The proposed method can operate well in both the modes, day and night. During the day, the active power is injected into the grid, and during the night, the solar arrays do not contribute; hence the SAPF is controlled to provide harmonic compensation to enhance the quality of the power. Further, the compensator is controlled to offer reactive power compensation, and inject active power into the grid.

The PV integrated system is tested under normal and abnormal grid conditions using SRF-PLL and MNFSOGI-PLL grid synchronization techniques. The open and closed loop performance of SRF-PLL with PV integration is thoroughly analyzed in simulation and experimentation. It is observed that the SRF-PLL fails to estimate the fundamental component of load current accurately from the non-linear load. The obtained grid current has a %THD of 19.07%, which is very high as per the requirement of IEEE-1547 standards for PV – integration. However, in the case of MNFSOGI-PLL, the %THD in grid current is found to be 3.93% which lies within IEEE-1547 standards.

The system has been tested extensively using MATLAB/ Simulink as well as OPALRT-4510 simulator, and the results are satisfactorily under normal and distorted grid conditions.

# Chapter 8
# Conclusions and Future Scope

## 8.1 Conclusions

Chapter 01 presents an introduction and background for the various power issues, sources of harmonics, and various mitigation methods. Chapter 2 discusses the extensive literature survey presented for with and without PV grid-integrated systems. A literature survey on different topologies of inverters has been presented, which can be used as SAPF unit in the system. Various adaptive control algorithms are also presented to estimate the fundamental component of load current and to generate reference current under abnormal and distorted grid conditions. Several grid synchronization techniques are also presented to tackle various grid abnormalities. Based on the extensive research, the research gaps have been identified, and further, the research objectives have been formulated

Chapter 03 discusses the design and development of a single-phase gridconnected without and with PV integration. The details of the experimental prototype setup, design equations, and system configuration have been presented. A single-stage, single-phase grid-connected PV system can accommodate PV arrays. The advantages of multilevel inverters over conventional 2-level inverters have been discussed thoroughly. Apart from the design aspects of CHB-MLI 5-level inverters, the switching logic and switching loss aspects have been discussed in detail in this chapter.

Chapter 04 presents the conventional adaptive control algorithm that has been developed for the control of 5-level SAPF. It has been designed and implemented to improve several power quality problems at the distribution level. Extensive tests backed with simulation and experimental results have been presented for control algorithms. A phase-shifted PWM scheme is designed and implemented for generating the switching pulses for CHB-MLI. The performance of the algorithms has been compared in terms of convergence speed, harmonics compensation, error minimization, computational complexity, THD, sampling time, and PLL requirement. Further, the developed notch filter controller has been compared with LMS and SRFT-based control algorithms for SAPF. The comparison results for the adaptive controls viz. LMS, SRFT, and Notch filter are tabulated. The obtained values of THD of supply currents are observed to be the lowest with the Notch filter as compared to other algorithms in simulation and experimentation.However, all algorithms meet the IEEE-519 standard. The weight convergence is faster with the notch filter under load variations thanusingother conventional algorithms.

Chapter 05 presents the 5-level SAPF interfaced to grid developed and tested with advanced adaptive control algorithms such as NLMAT, NHuber, and RSAPS. The response of all control algorithms is tested under load variations and normal grid supply. Both simulation and experimental results meet IEEE standards. The experimental THD of grid current obtained in the RSAPS algorithm is much less (2.4%) than that obtained with other adaptive control algorithms. However, simulation investigations show the THD obtained in NHuber is less (2.67%). It is observed that the RSPAS shows a slightly higher convergence time in obtaining the fundamental weight component, while NLMAT and NHuber performance is

better than RSAPS. All the advanced adaptive algorithms work satisfactorily under sudden dynamic load variations. The simulation and experimental results obtained are satisfactory and in agreement with each other.

Chapter 06 discusses grid-synchronization methods for single-phase systems, including SRF-PLL, SOGI-PLL, and TOSSI-PLL. The findings of extensive mathematical modeling, simulations and experiments have been presented. The effectiveness of the synchronization algorithms has been demonstrated through simulation and experimental testing under various grid voltage conditions such as voltage sag and swells, phase shift, and DC offset, and also tested under sudden load variations.The TOSSI-PLL exhibits the best amplitude and frequency estimation performanceunder grid voltage variation. TOSSI-PLL estimates frequency accurately, but some delay in convergence is expected. During the polluted and voltage sag/swell grid conditions, TOSSI-PLL and SOGI-PLL work satisfactorily to estimate frequency and amplitude. However, in the case of DC-offset conditions, both SRFT-PLL and SOGI-PLL fail to estimate the accurate frequency and amplitude. The TOSSI-PLL gives negligible frequency and amplitude estimation oscillations even under DC-offset conditions and distorted grid cases.

Further in this chapter, PARTAM-LMS adaptive control algorithm has been implemented for a single-phase grid-connected system for harmonic compensation under distorted grid conditions. The 5-level CHB-MLI is used as a SAPF unit which is controlled by the PARTAN-LMS algorithm and serves multiple objectives. The TOSSI-PLL suffers from slight delay during dynamics, so the SOGI-PLL-based synchronization technique has been used to generate unit sine templates under distorted grid conditions. The simulation and

experimental results obtained are satisfactory and in agreement with each other.

Chapter 07 presents the design and development of single-phase PV systems. Experimental prototype setup figures, design equations, and system configuration have also been presented. In a single-stage single, phase system, the two identical PV arrays of each rating of 0.954kW are connected to the DC link side of 5-Level CHB-MLI. The proposed system can operate in two modes, day and night. During the daytime, the active power is injected into the grid, and during the night, the solar arrays are disconnected; the SAPF provides harmonics compensation and improves the system power factor to unity. The PV integrated system is tested under normal and abnormal grid conditions using SRF-PLL and MNFSOGI-PLL grid synchronization techniques. The open and closed loop performance of SRF-PLL with PV integration is thoroughly analyzed in simulation and experimentation. It is observed that the SRF-PLL fails to estimate the fundamental component of load current accurately from the non-linear load. The obtained grid current has a high %THD with SRF-PLL. However, in the case of MNFSOGI-PLL, the %THD in grid current is found to be less and lies within the IEEE-1547 standard required for PV – integration.

## 8.2 Future Scope

Research is a never-ending process. The end of a research work actually signals the start of many additional possibilities for future research. A research project's completion opens the door to new research problems. Future research in this area will focus on the following aspects:

1. Identification of adaptive digital filters. These filters reduce the system complexity

and require less computation time to implement in digital signal processors.

2. The conventional PI controllers may be replaced with advanced controllers.
3. Identification and implementation of reduced device count (RDC) based multilevel inverter topologies.
4. The development of new synchronization methods, particularly under DC-offset conditions need more to be identified.
5. Possibility of makinga hybrid system by integrating renewable energy resources such as fuel cells, wind power, and PV arrays in the DC link side of Multilevel inverters

## Publications

### Details of Publications in SCI/SCIE/ESCI Journals

1. P. Bansal and A. Singh, A. Nonlinear adaptive normalized least mean absolute third algorithm for the control of five-level distribution static compensator. International Journal of Circuit Theory and Application, Wiley; 2021; 49(9): 2840– 2864. https://doi.org/10.1002/cta.3045
2. P. Bansal and A. Singh, A. Nonlinear adaptive normalized Huber control algorithm for 5-level distribution static compensator. Journal of Electrical Engineering, Springer, 104, 1635–1648 (2022). https://doi.org/10.1007/s00202-021-01424-0
3. P. Bansal and A. Singh (2021) Multilevel Inverter Based Power Quality Enhancement Using Improved Immune Control Algorithm, International Journal of Electronics, Taylor and Francis, 108:12, 1999-2018, doi: 10.1080/00207217.2020.1870754.
4. P. Bansal and A. Singh. Closed Loop Control Using RSAPS Algorithm for 5-Level CHB Multilevel Inverter. International Journal of Control and Automation for Electrical Systems, Springer, 33, 998–1011 (2022). https://doi.org/10.1007/s40313-021-00864-0

### Details of Publications in International Conferences

1. P. Bansal and A. Singh, "Adaptive Notch Filter Control Algorithm for 5-Level Distribution Static Compensator," 2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC), 2020, pp. 1-5, doi: 10.1109/STPEC49749.2020.9297721

2. P. Bansal and A. Singh, "Control of Multilevel Inverter as Shunt Active Power Filter using Maximum Versoria Criterion," 2019 IEEE International Conference on Power Electronics, Control and Automation (ICPECA), 2019, pp. 1-6, doi: 10.1109/ICPECA47973.2019.8975392.

3. P.Bansal, Alka Singh , "**Optimal Harmonic Current Extractor using Digital Warped Filter for a Single –Phase PV Integrated Grid-Tied System with 5-Level DSTATCOM"** accepted for publication in IEEE conference SEFET-2023 to be held during 9th -12th August 2023, being organized by the Department of Electrical Engineering, ITER, **Siksha 'O' Anusandhan (Deemed to be University),** Bhubaneswar, Odisha, India

### Details of Publications in Book Chapter

1. P.Bansal, Alka Singh 'Design and Control using the ISOGI-Q Algorithm for Grid Integration of PV-Array' to publish in book - Internet of Energy – A Pragmatic Approach to Sustainable Development, Taylor and Francis (2022)-(Accepted)

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