ENERGY EFFICIENT VOLTAGE LEVEL SHIFTER DESIGN IN NTV REGIME

A

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY

IN

CONTROL AND INSTRUMENTATION (2021-2023)

SUBMITTED BY:

Mohit Rikhari
2K21/C&I/02

UNDER THE SUPERVISION OF

Prof. PRAGATI KUMAR

Dr. CHAUDHRY INDRA KUMAR

DEPARTMENT OF ELECTRICAL ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering) Bawana Road, Delhi-110042

MAY 2023

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering) Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Mohit Rikhari, Roll No – 2k21/C&I/02 student of M. Tech. (Control & Instrumentation), hereby declare that the project Dissertation titled "**ENERGY EFFICIENT VOLTAGE LEVEL SHIFTER DESIGN IN NTV REGIME**" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi

Date: **(Mohit Rikhari)**

ELECTRICAL ENGINEERING DEPARTMENT

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering) Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled "**ENERGY EFFICIENT VOLTAGE LEVEL SHIFTER DESIGN IN NTV REGIME**" which is submitted by Mohit Rikhari, whose Roll No. is 2k21/C&I/02, Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi **Prof. PRAGATI KUMAR**

Date: (**SUPERVISOR)**

Chaudhary Inder Kumar

Place: Delhi **Dr. CHAUDHARY INDRA KUMAR**

Date: (**SUPERVISOR)**

ABSTRACT

The constant demand for power efficient electronic systems has led to the exploration of low-power design techniques in various aspects of integrated circuits. In particular, voltage level shifters play a crucial role in bridging voltage domains within a system. This thesis focuses on the design and optimization of energy-efficient voltage level shifters operating in the Near-Threshold Voltage (NTV) regime. This work presents a low power and high-speed voltage level shifter circuit which can convert near threshold voltages to super threshold region. The proposed structure improves performance and speed by implementing a low power buffer to minimize power losses in the previous designs. High delay owing to fall transition has been mitigated using a pass transistor, which improves the overall speed of operation of the circuit without using any multi-threshold devices. Only 11 transistors are used for the proposed circuit. The circuit can shift input voltages as low as 0.3 V to 1V output voltage. The proposed LS was implemented using 45nm CMOS technology and incurs power dissipation of 12.78nW with propagation delay of 4.106 ns for a 0.4V/ 1 MHz signal. The designed circuit shows high speed performance as compared to other circuits present in the literature over a wide range of temperature.

ACKNOWLEDGEMENT

I would like to thank to all people who have helped and inspired me during my dissertation work throughout the year. I sincerely acknowledge the earnestness and patronage of my supervisors **Prof. Pragati Kumar** and **Dr. Chaudhary Indra Kumar**, Department of Electrical Engineering, Delhi Technological University, New Delhi, for their valuable guidance, support and motivation throughout this project work. The valuable hours of discussion and suggestion that I had with them have undoubtedly helped in supplementing my thoughts in the right direction for attaining the desired objective.

I wish express my gratitude to my beloved parents and friends for their understanding and support. Above all, thanks to Almighty for blessing and guiding me throughout my life.

Mohit Rikhari

(2k21/C&I/02)

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

VLSI	Very Large-Scale Integration
PMOS	P-channel Metal Oxide Semiconductor
NMOS	N-channel Metal-Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
NTV	Near Threshold Voltage
LS	Level Shifter
WCMLS	Wilson Current Mirror based Level Shifter
RCC	Regulated Cross-Coupled
DCL	Double Current Limiter

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

One of the most popular methods for lowering power consumptions in low power digital circuits is voltage scaling. In fact, the number of cores and voltage scaling of digital cores on modern processors have both greatly grown. Voltage scaling to regions well below the threshold voltage of device, known as subthreshold region, does consume low power but it is not the most energy efficient region to operate the device. Rather, operation of circuit at voltage level close to threshold voltage, called near threshold voltage (NTV) operation proves to be more energy efficient. Thus arises the need for speed and power efficient Level shifter (LS) Circuits operating in NTV region.

Operating near threshold voltage has several benefits in terms of power efficiency and performance. Here are some of the benefits of near-threshold voltage operation:

1. Power Efficiency: One of the significant advantages of operating near threshold voltage is reduced power consumption. Transistors operating at lower voltages experience lower leakage currents, which results in reduced power dissipation. Since power consumption is directly proportional to the square of the voltage, operating at lower voltages can lead to significant power savings.
2. Energy Efficiency: Near-threshold voltage operation enables energy-efficient computing. By lowering the supply voltage, the energy consumed per operation is reduced. This is particularly beneficial for battery-powered devices, where energy efficiency is crucial to prolong battery life.
3. Increased Integration Density: Operating at lower voltages allows for increased integration density or packing more transistors on a chip. The reduced voltage levels allow for smaller transistor sizes, enabling higher transistor counts and more complex circuits within the same chip area.
4. Improved Performance-Per-Watt: Near-threshold voltage operation can offer improved performance-per-watt compared to traditional operating voltages. While individual operations might take longer due to slower transistor switching, the overall energy efficiency can lead to higher performance per unit of power consumed.

1.2 OPERATION IN NEAR-THRESHOLD VOLTAGE (NTV) REGION

The operational sphere of Near-Threshold Voltage (NTV) embodies a unique transistor functioning segment within the broader scope of Complementary Metal-Oxide-Semiconductor (CMOS) technology. It is particularly significant for electronic engineering designs aimed at maximizing power conservation. This operational sphere serves as an intermediary between two polar transistor operational areas, namely the sub-threshold and super-threshold zones, achieving a harmony between energy consumption and performance delivery.

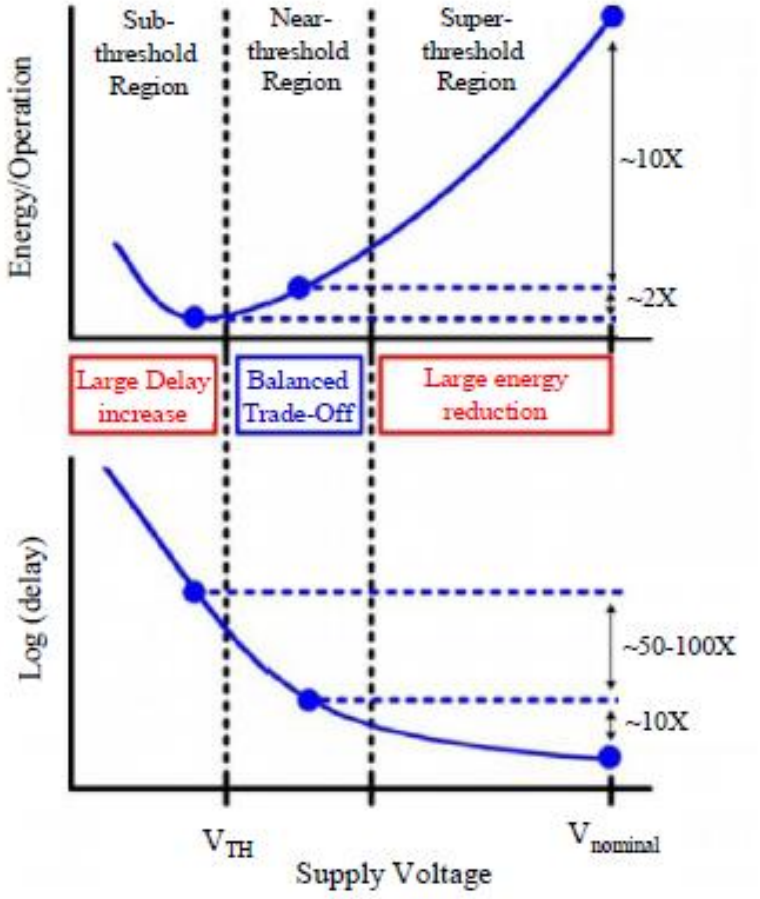

Fig. 1.1 Energy and delay in different operating regimes.

The sub-threshold region is marked by gate-source voltages dropping below the threshold voltage (Vth), pushing transistors into an OFF state. This region is characterized by minimal leakage currents, yet it suffers from an inherently slow performance due to reduced drive strength. This sluggishness restricts its widespread utility.

Conversely, the super-threshold region is characterized by gate-source voltages soaring significantly above the threshold voltage. This area offers high-performance output due to enhanced drive strength, but it is also notorious for high energy expenditure, posing issues for energy-sensitive applications.

The Near-Threshold Voltage (NTV) territory offers a solution to balance these contrasting operational aspects. By allowing transistors to function marginally above their threshold voltage, it fosters a synergy between power efficiency and performance output. This region is particularly successful in securing significant energy savings while delivering satisfactory performance for a multitude of applications.

NTV region operation gains prominence in power-sensitive systems, including wearable devices, Internet of Things (IoT) devices, and any scenario where power efficiency is the overriding consideration. Transistors functioning in this regime can adeptly manage power budgets while maintaining an acceptable performance level, which is crucial given the proliferation of computing and increasing demand for mobile electronic devices.

In near-threshold voltage (NTV) regime, the operating voltage of a digital circuit is very close to the threshold voltage of the transistors used in the circuit. This operating condition poses challenges for reliable and robust circuit operation. One of the challenges in NTV operation is the need for voltage level shifters. Here's why voltage level shifters are required in near-threshold voltage regime:

1. Signal Integrity: Near-threshold voltage operation can lead to reduced noise margins, meaning the voltage difference between logic high and logic low levels becomes smaller. This reduced voltage swing can make it challenging for signals to be reliably propagated from one stage to another. Voltage level shifters are used to boost or shift the logic levels of signals to ensure proper signal integrity and reliable data transfer between different voltage domains.
2. Compatibility with Peripheral Circuits: In a system, there may be peripheral circuits or components that operate at higher voltages than the NTV circuit. For example, input/output (I/O) interfaces, memory interfaces, or communication interfaces may require higher voltage levels. Voltage level shifters are necessary

to interface between the NTV circuit and these peripheral circuits, ensuring proper communication and compatibility.

3. Robustness against Process Variations: Near-threshold voltage operation is highly sensitive to process variations, such as transistor threshold voltage variations, due to the smaller voltage margins. Voltage level shifters can help mitigate the impact of process variations by providing appropriate voltage scaling and translation, thus improving the robustness of the circuit against these variations.
4. Power Supply Regulation: Near-threshold voltage operation is highly dependent on power supply stability. Voltage level shifters may incorporate voltage regulators or supply clamps to ensure a stable and regulated supply voltage for the circuit. This helps in maintaining proper functionality and reducing the effects of voltage droops or fluctuations.

Overall, voltage level shifters play a crucial role in near-threshold voltage operation by addressing the challenges related to signal integrity, compatibility with peripheral circuits, robustness against process variations, and power supply regulation. They enable reliable operation and interconnection of circuits operating at different voltage levels, ensuring proper functionality and performance in the near-threshold voltage regime.

As per the scope of this thesis, a voltage level shifter designed for NTV regime operation aims to efficiently elevate near-threshold voltages to super-threshold levels and vice versa. This conversion ensures smooth interoperability between different components of a circuit operating at varying voltage levels, thereby guaranteeing power-efficient and uninterrupted communication within the electronic system. The core of this thesis revolves around designing an energy-efficient voltage level shifter suitable for NTV regime operation—a vital facet of progressive, low-power electronic design.

Given the surge in demand for low-power electronic devices and the exponential expansion in applications such as IoT, wearable technology, and mobile electronics, it is clear that the relevance and necessity for NTV regime operation will continue to rise. Therefore, this thesis's exploration and contributions to NTV regime operation and the design of efficient voltage level shifters are not only relevant but essential to the current and future state of electronic design and engineering.

1.3 VOLTAGE LEVEL SHIFTERS

Voltage level shifters, also known as level translators, are integral components in the realm of electronic design. They serve a crucial role in bridging the gap between diverse sections of a circuit that operate at differing voltage levels. By facilitating seamless communication and data transfer between these varying voltage domains, they ensure the overall functionality and performance of an electronic system.

Level shifters exhibit the capability to convert low-level voltage signals to higher voltage levels and vice versa. This ability is of paramount importance in today's complex electronic systems, where different parts of a circuit—such as the core logic and peripheral devices—may need to operate at different voltages due to varying performance or power requirements.

Propagation delay and power dissipation are two crucial factors that often define the performance of level shifters. The time it takes for a signal to travel from the level shifter's input to its output is known as the propagation delay, and the amount of power used during this entire procedure is known as the power dissipation. A level shifter that achieves the best balance between speed and power efficiency would have a small propagation delay and low power dissipation.

There are many different types and configurations of level shifters, each with advantages and disadvantages. The single-supply, dual-supply, and bi-directional level shifters are the three most popular types. The simplest form is the single-supply level shifter, which is frequently employed when the ground reference for the two voltage domains is the same. When the two voltage domains have independent power supplies, the dual-supply type is used. As their name implies, bi-directional level shifters may convert voltage levels in both directions and are appropriate for data bus applications.

The difficulty in creating level shifters, despite the variety of level shifters on the market, comes in balancing the trade-offs between several parameters, including speed, power efficiency, complexity, and cost. For instance, a level shifter made for high speed might use more power, but one made for low power might have longer propagation delays.

The goal of this research work is to design a voltage level shifter that is energy-efficient and capable of functioning in the near-threshold voltage (NTV) regime. To achieve this, a design must be created that not only reduces power loss and propagation delay but also keeps its reliability even when working with low input voltages. By facilitating more effective and dependable communication across various voltage domains inside a circuit, such a voltage level shifter would significantly advance the field of low-power electronic design

1.4 NEED FOR A VOLTAGE LEVEL SHIFTER

In Very Large Scale Integration (VLSI) circuits, voltage level shifters play a crucial role due to the increasing need for low power consumption in numerous applications. As technology continues to scale down, the operation voltage of digital circuits has decreased accordingly to reduce dynamic power consumption. This power optimization has led to heterogeneous systems where different parts of the circuit operate at different voltage levels, creating a necessity for voltage level shifters. Voltage level shifters are used to bridge these circuits operating at different voltage levels by converting signal levels from a lower voltage domain to a higher one, or vice versa, without degrading signal integrity. This ensures proper functioning and interoperability between the disparate voltage domains.

Moreover, voltage level shifters are essential in technologies such as Near-Threshold Voltage (NTV) operations, where voltage supplies are significantly lower than traditional circuits. Here, voltage level shifters become critical to balance performance, power, and reliability, and achieve energy-efficient operations. In conclusion, the voltage level shifter is an indispensable component in modern VLSI circuits, significantly contributing to the energy efficiency and power optimization of these systems.

1.5 THESIS ORGANISATION

The content of the thesis is organized in four chapters:

Chapter I – Includes the introduction about level shifters and NTV region. It explains the need for level shifters and how operation of LS in NTV region offers the best tradeoff point with good performance and low power consumption

Chapter II – This chapter gives a detailed literature review of the various circuits of level shifter. It mentions their salient features along with research gaps amongst those.

Chapter III – This chapter includes the proposed design low power buffer based LS, it discusses its working and salient features. It also contains the various simulations and results for the proposed circuit. Outcome of the research is also included in this chapter

Chapter IV – This includes conclusion of the work and any further future scope.

CHAPTER 2

LITERATURE REVIEW

2.1 CONVENTIONAL LEVEL SHIFTER

The circuit schematic of conventional LS is shown in Figure 2.1, it is based on differential cascade voltage switch (DCVS) type architecture. The circuit comprises of thick gate oxide MOS transistors MP1, MP2, MN1 and MN2 for overcoming voltage stress. For a low or logic 0 input, MN2 starts conducting which pulls down node Q2. This turns on MP1 and Q1 node gets charged to VDDH level or logic 1, which gets inverted by the output inverter so that the output is low. For a high input, MN1 starts conducting and MN2 turns off, this pulls down Q1 node, which turns on MP2 and Q2 node gets charged up to VDDH. A logic 0 signal at Q1 gets inverted to give a high output at VDDH level.

The conventional LS suffers with two major demerits. Firstly, due to thick gate oxide layer of MN1 and MN2 transistor the circuit cannot work at low core voltages. Secondly, due to contention between pull-down transistors (MN1 and MN2) and pull-up (MP1 and MP2), the strengths of pull-up and pull-down networks have to be properly balanced to get proper output, this is difficult to achieve when circuit works at deep sub-threshold voltage ranges thus making the circuit unsuitable for voltage translation from deep sub-threshold voltages.

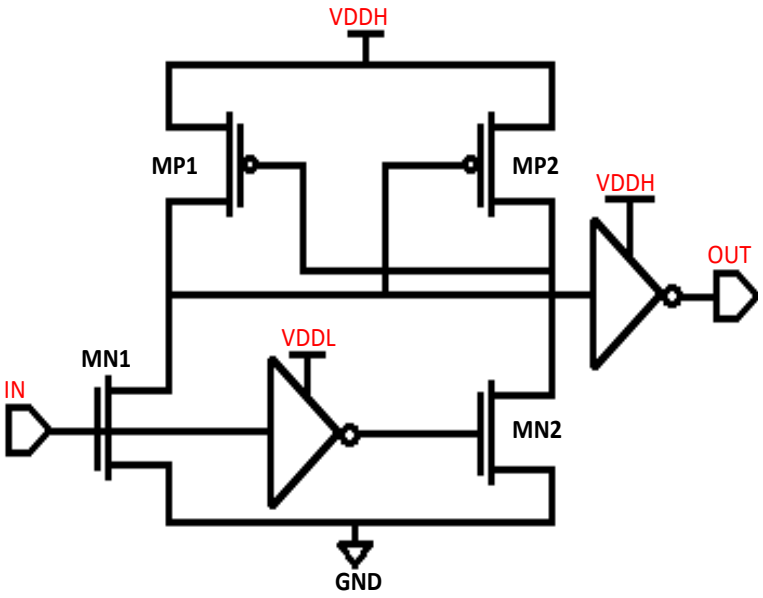

Figure - 2.1 Conventional voltage level up shifter

2.2 Previous Level Shifter Designs

The LS in [1] implements a reduced-swing output buffer and a pass transistor in the design to reduce delay and decrease the static power consumption. The proposed LS in [2] incorporates zero-Vt transistor as well as analog circuit techniques to make LS suitable to work in ultralow core voltages and minimize static power losses. In LS [3] LVT transistors are used in pull down network and input inverter to mitigate static power losses and address contention problem of pull up and pull down network. In [4] self-adapting pull up networks along with split input inverting buffer is used to increase speed of operation and reduce power consumption A feedback transistor is used by the Wilson current mirror level shifter (WCMLS) [5] to stop static current, but this leads to a high static current flowing at the first inverter of output buffer. Additionally, the input inverter and the charge sharing via feedback transistor significantly slows down the speed of the fall transition.

In order to increase the speed of the circuit, the LSs in [6] and [7] uses multi-threshold CMOS transistors to reduce the pull-up network while boosting the pull-down network. In [6] a multiplexer can be added to the standard architecture for further optimizations, and the input supply voltage can also be used as the select signal. LS with current limiter in [8] presents a LS which incorporates a self-controlled current limiter by detecting error, this setup used an error signal generated from output signal to control the current mirror and it also incorporates multi threshold MOS transistor hence optimizing the delay. P.K Machiraju et al. in [9] presented an efficient voltage level translators which could translate the voltage up or down based on the input voltage applied. In [10] stacking technique is utilized which helps minimize leakage power and currents, hence making circuit suitable for low power applications. Q.A Khan et al. in [11] proposed a single supply LS, which helps in minimizing layout congestion and pin count with zero static current consumption. In LS mentioned in [12] a two stage operation is utilized incorporating techniques like varying transistor size, use of multi-threshold devices to increase the strength of pull down network while using a virtual supply to bring down pull up network current driving capability. Stage 2 helps in achieving rail-to-rail swing. A two-level driver circuit for driving ultrasonic transducers is suggested in [13] and is based on the 0.18 um HV SOI CMOS technological method. In [14] for ultra low voltage application from subthreshold to above threshold, a write assist is utilized. It also uses body biasing of NMOS transistor

to compensate for mismatch and process variations. The LS in [15] uses close loop negative feedback circuit to control current, hence improving upon both delay and power profile. In [16] the LS incorporates a quasi inverter for fast charging and discharging of nodes. In [17] a high voltage driver circuit using adapted level shifter is implemented in 65 nm TSMC technology node. The adaptive LS makes use of stacked CMOS transistors. The Passive LS in [18] work by translating the median value of incoming signal.

In [19] the LS optimizes delay, area and power-delay product (PDP) with the use of single power rail. Figure 2.2 shows the energy efficient level shifter. The circuit uses threshold voltage drop of M1 to create a virtual VDDL for the input inverter consisting oof M2 and M5, thus increasing robustness and voltage stress problem at the input inverter level. The circuit schematic is shown below.

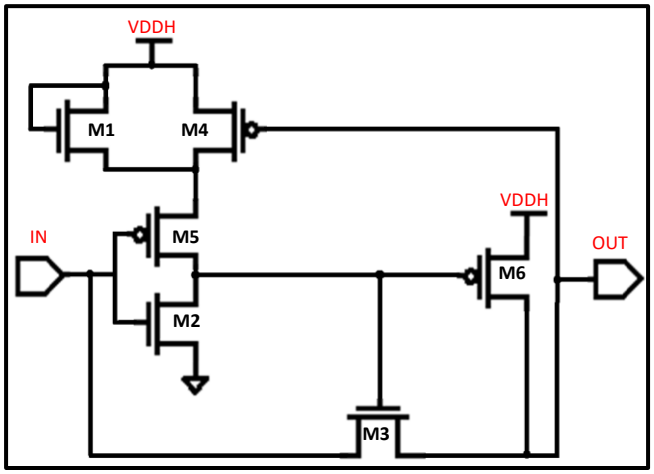

Figure - 2.2 Energy efficient topology based level shifter

Also, the source of M3 is connected to the input terminal, which further helps in reducing leakage currents during rising edge transition of the input voltage. In [20], it is also possible to use the back gate of transistors to lower the threshold voltage of the transistor and lower the static power consumption of the LS designed.

2.3 REFLECTED OUTPUT WILSON CURRENT MIRROR BASED LEVEL SHIFTER

The circuit diagram of a reflected output WCMLS [21] is shown in Figure 2.2 The circuit is a modified WCMLS architecture. For a rising edge transition, MN2 is turned on which pulls down node Q3, this turns on MP3 and hence discharges node Q2 through MP3, MN2 and ground. A discharged Q2 turns on MP5 and output will be high at VDDH

voltage level. For a low input, MN2 gets turned off and Q4 node gets discharged through pass transistor, which turns on MP2 and through an initially discharged Q2, Q1 discharges and turns on MP1 MP4 and Q3 gets charged, which turns on MN3 and output becomes low. The circuit incorporates a pass transistor MN1, current limiting diode MP3 in series and a split input inverter consisting of MP5 and MN3 to optimize delay and power consumption, but the delay is still significant.

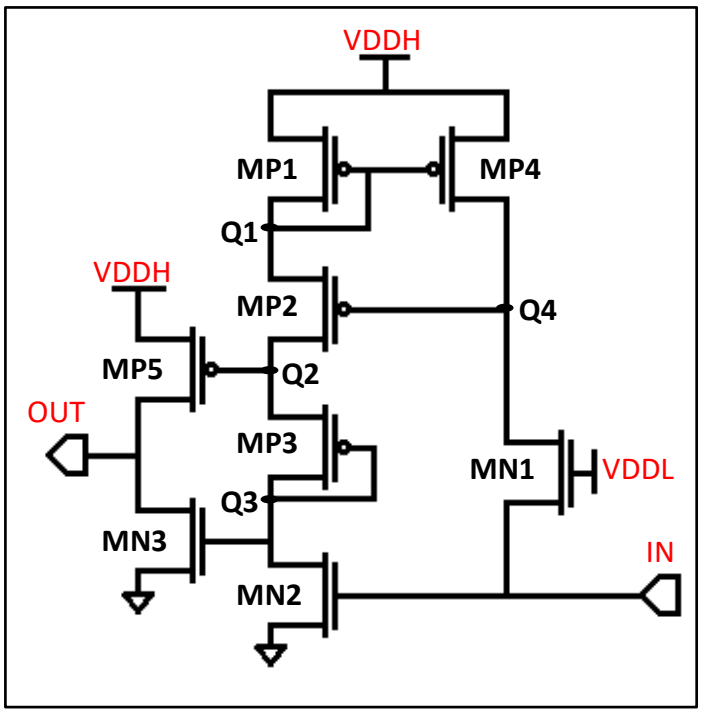

Figure – 2.3 Reflected output WCMLS [21]

2.4 DOUBLE CURRENT LIMITER BASED LEVEL SHIFTER

The circuit schematic of a double current limiter based LS [22] is shown in Fig 2.3 The circuit incorporates double current limiters MN1-MN4 and MN2-MN5 to achieve better power delay product and mitigate contention between pull-up and pull-down networks. For a low input, MN6 turns on through VDDL inverter and pulls down Q2 node, which turns on MP1 and Q1 gradually charges to a reduced swing voltage level through MN1 and MN2 diodes. Output inverter inverts the weak logic 1 signal at Q1 to give a good logic 0 at output, so that the output is low. For a high input signal MN3 turns on, pulling down node Q1, which turns on MP2 and pulls up Q2 node, this turn of MP1 and the logic

0 signal discharged Q1 node is inverted to give a logic 1 signal at the output with a full swing.

The circuit incorporates 12 transistors and has high delay for fall transition due to slow charging of Q1 node through double current limiter MP2-MP3, hence overall speed of operation of circuit is slow and reduced swing at Q1 node causes significant power loss in the output inverter. Hence overall delay and power consumption of the circuit is still significant.

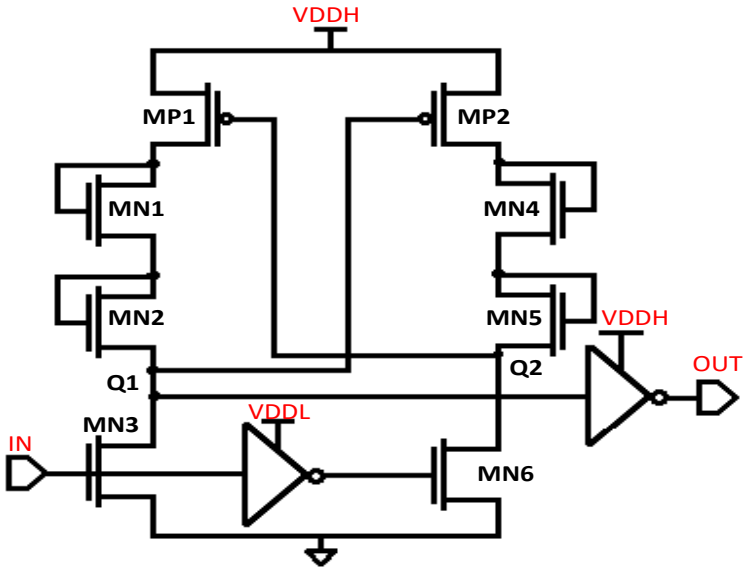

Figure – 2.4 Double current limiter based LS

2.5 REGULATED CROSS COUPLED PULL-UP NETWORK BASED LEVEL SHIFTER

The circuit schematic of a regulated cross coupled pull up network based LS [23] is shown in figure 2.4. The circuit employs MP1, MP2, MP4 and MP5 transistors as regulated cross-coupled pull-up network, these help in the regulation of pull-up network strength, which also helps in mitigation of contention. MN1, MN2 are used in the pull-down network. This circuit also incorporates MP3 and MP6 transistors as current limiters which also help in controlling the dynamic power losses during switching. Output is taken through a split input which further reduces switching power loss as compared to a normal common input inverter.

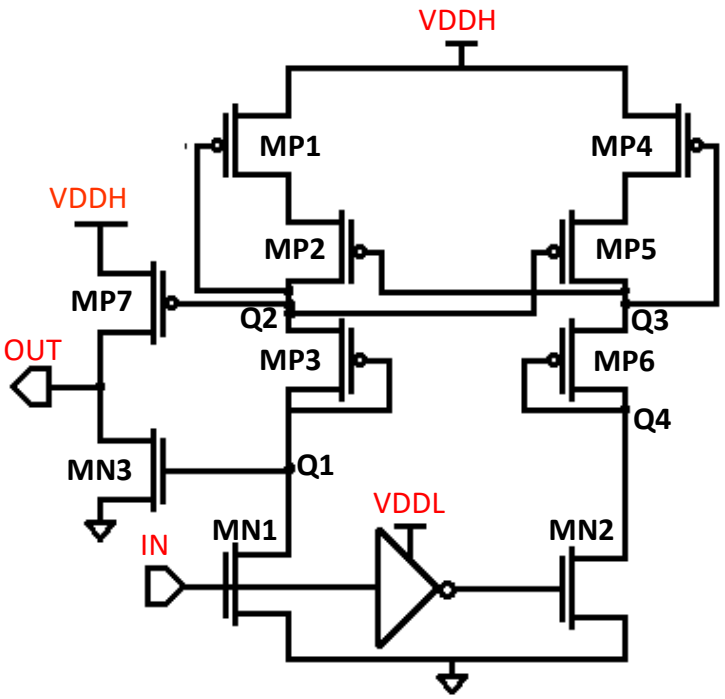

Figure – 2.5 Regulated cross coupled Pull up network based LS

With a rising edge pulse at the input, MN1 turns ON and pulls down node Q1, this turns on MP3 due to low voltage level at its gate terminal and hence its drain and source terminal gets shorted which pulls down node Q2. Due to pull down of node Q2, MP7 is turned ON, which pulls up output node to VDDH level. For a falling edge transition, Input inverter inverts the input voltage signal and sends a high voltage level at the input of MN2 transistor, which turns MN2 ON and pulls down node Q4 and consequently node Q3 is pulled down by turning MP6 ON. Due to low voltage level at Q3, MP2 is turned ON, which along with MP1 and MP3 charges node Q1 to turn on MN3 and hence we get low voltage level (0 V) Output.

CHAPTER 3

DESIGINED LEVEL SHIFTER

3.1 LOW POWER VOLTAGE BUFFER BASED LEVEL SHIFTER

The proposed level shifter circuit is designed in 45nm CMOS technology which converts near threshold voltages, as low as 0.3 V to above threshold voltages with fast speed of operation and low power consumption. The circuit diagram of the proposed design is shown in Figure 3.1 below.

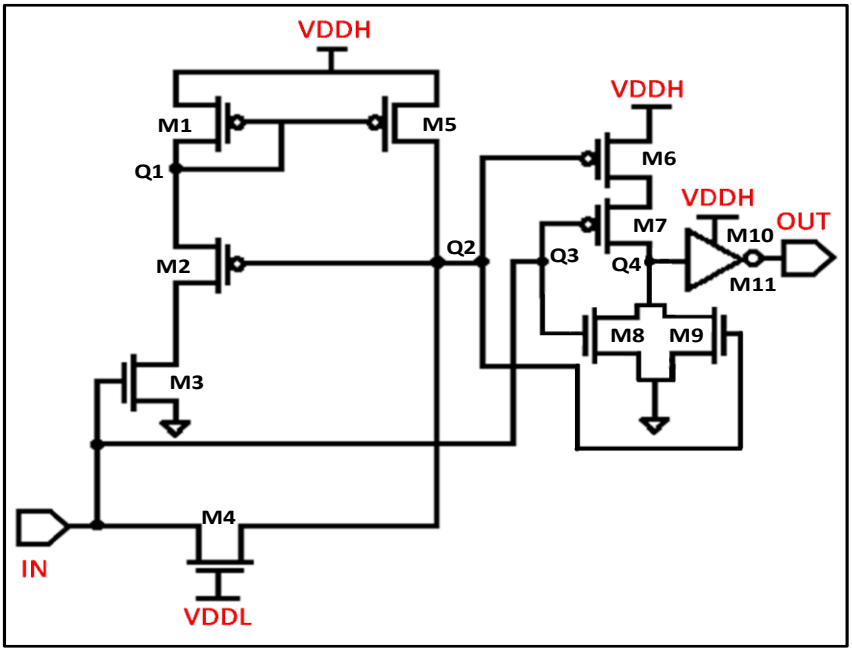

Figure – 3.1 Low power voltage buffer based LS

The circuit comprises of 11 transistors M1 to M11. The circuit is a modified WCMLS structure and includes a low power buffer constituting of MOS transistors M6-M11 that incorporates a C-element structure comprising of M7 and M8 to minimize static power loss. The circuit also incorporates a pass transistor M4 to optimize fall transition delay of the proposed design. Hence, improving upon the overall delay of the circuit and increasing speed of operation of circuit while balancing the tradeoff between speed and power dissipation.

Initially when the input voltage signal is at low level (0V), the pass transistor M4 passes the low voltage signal and discharges node Q2 to a lower voltage level, which turns on MOS transistors M6, as the gate terminal of M6 received a low voltage signal. Due to a low input signal at node Q3, M7 also gets turned on, hence due to conduction of M6 and M7 transistor, Q4 node starts charging and reaches to a high voltage level which gets inverted by M10-M11 output inverter to give a low voltage signal (i.e 0 V) at output. Also, with Q2 discharged M2 is turned ON, but current in M1-M2-M3 is cut off since M3 and M1 are in OFF state at this point. Now, for a low voltage to High voltage transition of input signal M4 gets turned off due to a negative gate to source voltage and M3 turns on, this leads to discharging of node Q1, which in turn supplies a low voltage signal at the gate of MOS transistors M1 and M5. This sets up flow of a reference current through M1-M2-M3 transistors which gets mirrored through transistor M5, to charge node Q2. This, along with a high voltage signal at input, turn on MOS transistors M9 and M8 respectively, which pulls down node Q4 and through inverter action of M10-M11, output gets high with a full rail swing of VDDH.

3.2SIMULATION AND RESULTS

We have used Cadence Virtuoso tool for the analysis of our circuit and its validation. We have designed our circuit using Cadence gpdk 45nm CMOS mixed signal technology. For the simulation Supply rail was kept at 1 V.

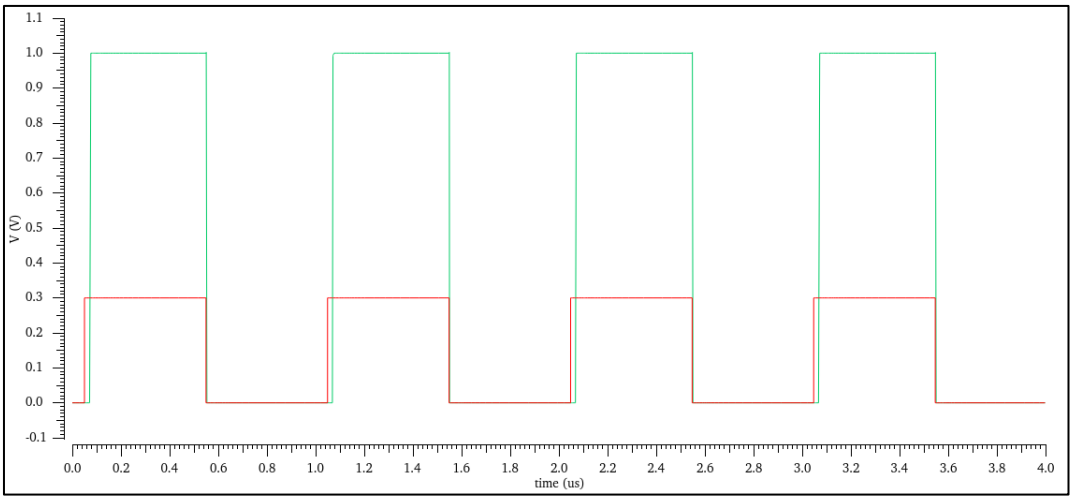

Figure – 3.2 Input Output Waveform of the designed Circuit with Vin at 0.3V

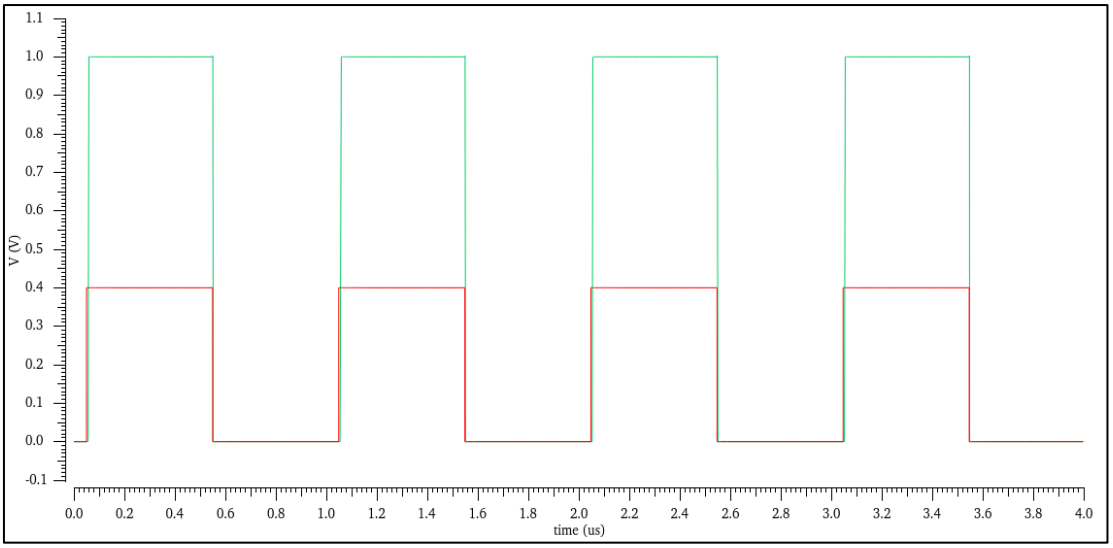

Figure – 3.3 Input Output Waveform of the designed Circuit with Vin at 0.4 V

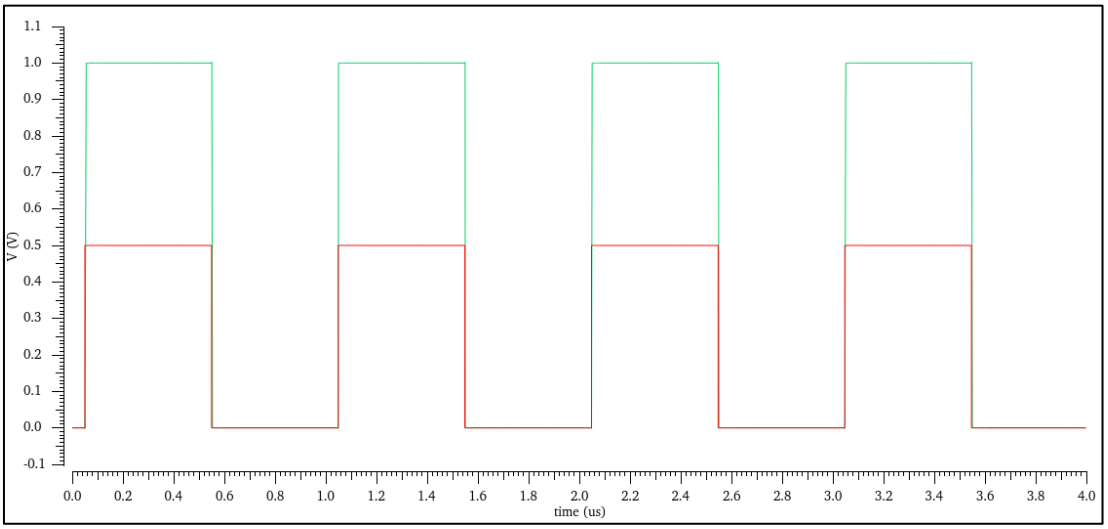

Figure – 3.4 Input Output Waveform of the designed Circuit with Vin at 0.5 V

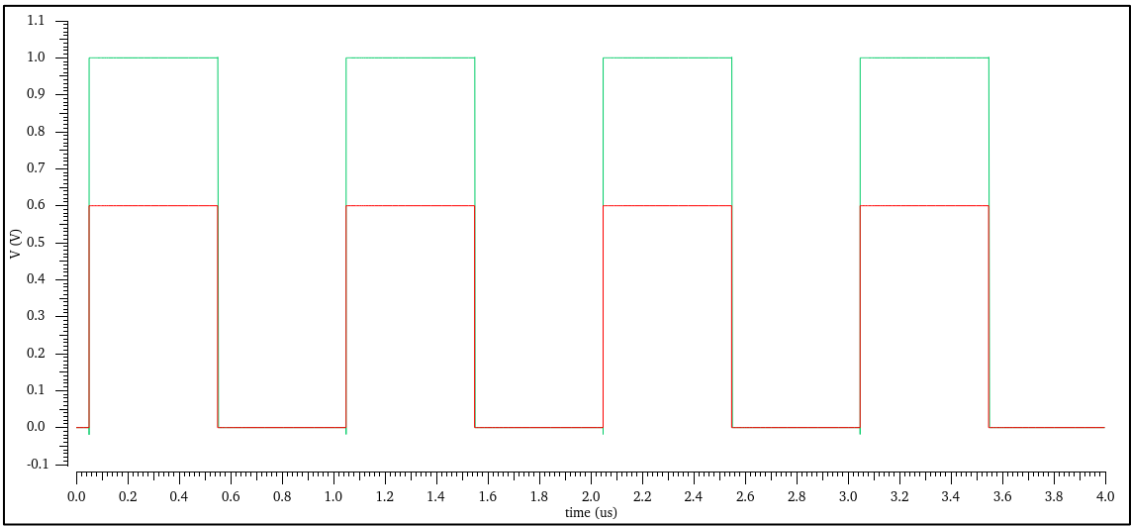

Figure – 3.5 Input Output Waveform of the designed Circuit with Vin at 0.6 V

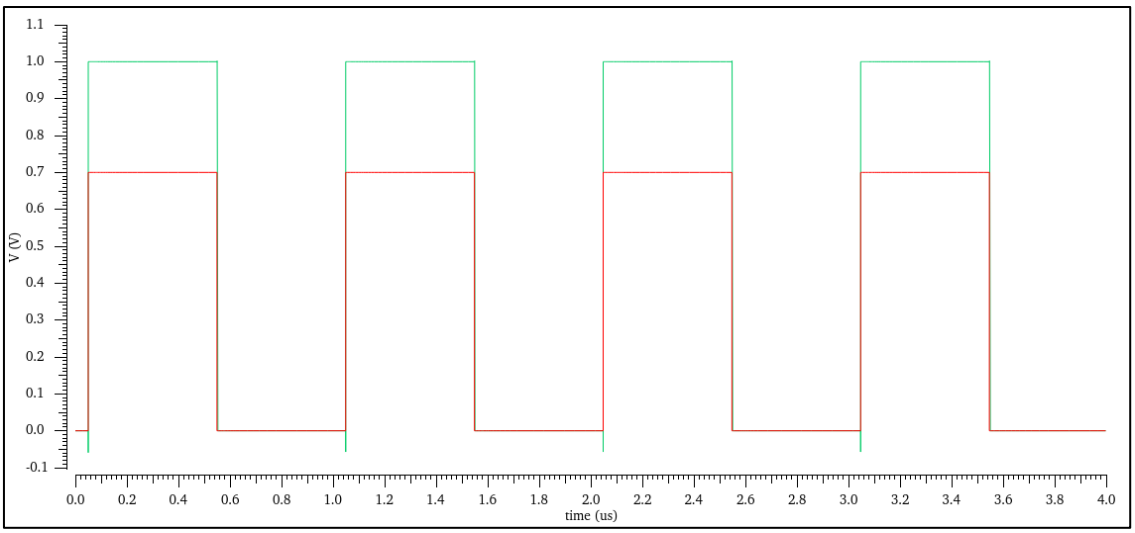

Figure – 3.6 Input Output Waveform of the designed Circuit with Vin at 0.7 V

The Input and output waveforms of the designed level shifter circuit are shown in figure 3.2 to figure 3.6 for input voltage as low as 0.3V to up to 0.7V. Input voltages are shown in red, while output is indicated by green lines in these waveforms. The above analysis shows the robustness of the design, which works effectively at the Near-Threshold Voltage Region (NTV) as well as above threshold voltage. When we go below 0.3V input voltage the delay of the circuit increases significantly due to slow charging and discharging of the nodes at lower voltages.

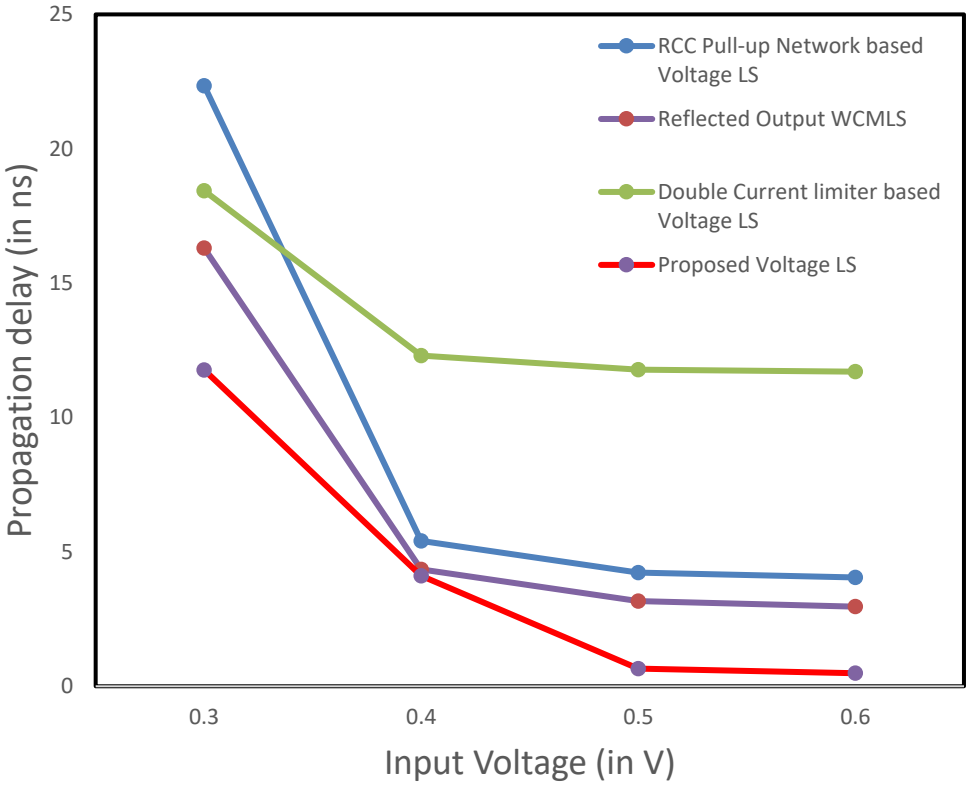

Figure – 3.7 Comparison of propagation delays of various Voltage LS circuit

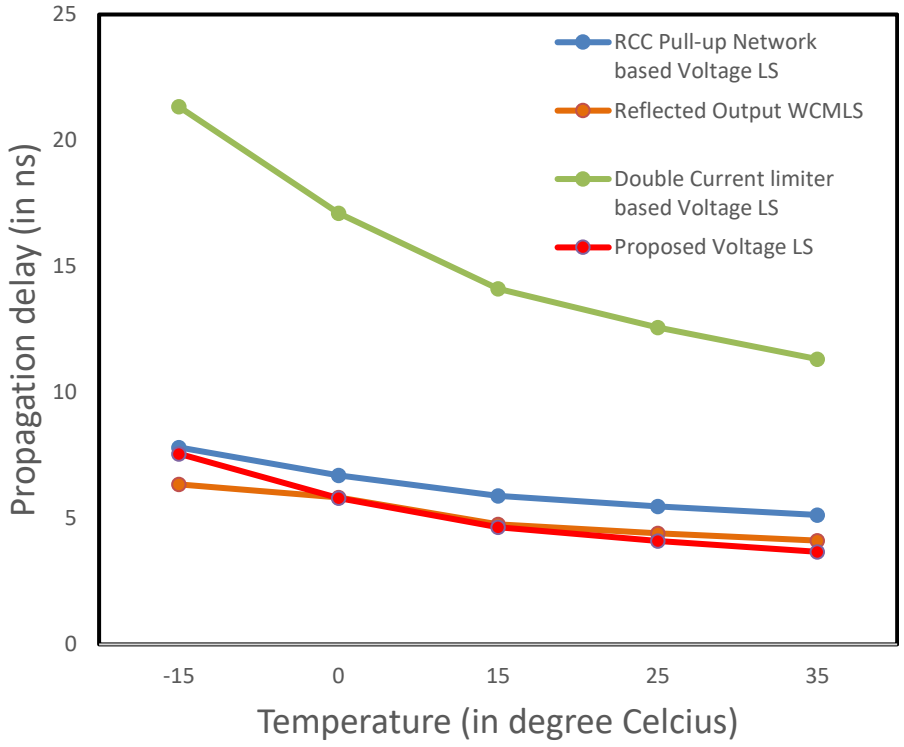

Figure – 3.8 Variation of propagation delays of different voltage LS with respect to Temperature

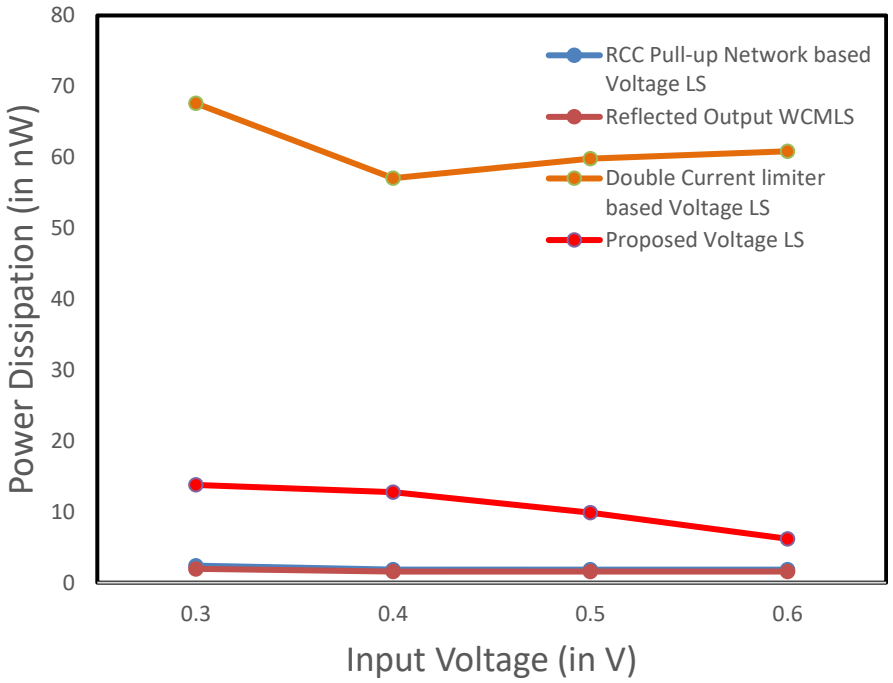

Figure – 3.9 Comparison of Power dissipation of different voltage LS

The configuration of transistors, defined by features such as the channel width (W) and length (L), plays a pivotal role in the design of circuits. The proportion (W/L), also known as the aspect ratio, impacts a range of essential transistor properties including current flow, operational speed, power consumption, and noise tolerance. For example, enhancing the transistor's width can escalate its current conduction capability, thereby increasing its speed. However, this can also inadvertently augment parasitic capacitances, potentially resulting in higher power loss. Similarly, shortening the channel length can boost speed but may exacerbate short-channel effects and augment leakage currents, which could negatively impact the circuit's power efficiency and dependability. Therefore, fine-tuning the dimensions of a transistor is a vital process in striking the optimal balance between speed, power, and noise margins in circuit design. The subsequent table showcases the aspect ratios of the transistors utilized in our proposed model, exemplifying this intricate equilibrium.

TABLE - 3.1 Aspect ratios of MOS Devices

Transistor	**W/L ratio**	**Transistor**	**W/L ratio**
M1	2.67	M7	2.67
M2	2.67	M8	5.33
M3	2.67	M9	2.67
M4	2.67	M10	2.67
M5	2.67	M11	2.67
M6	2.67		

Table 3.1 shows the aspect ratios of the 11 transistors used in the design. M8 transistor is provided with higher width as compared to the rest of the transistors so as to increase its current driving capability to discharge Q4 node. Input Voltage directly appears at the gate terminal of M8, this voltage level is significantly lower as compared to the supply rail level. This would cause higher delays during the rising edge transition of the input, hence to strengthen this transistor its aspect ratio is increased significantly.

From the figure 3.7 we can see that the proposed level shifter design offers the lowest propagation delays with respect to other modes described in the literature, the proposed model also offers significantly lower delay over a wide range of temperatures as shown in figure 3.8.

The proposed circuit also consumes less power due to low power voltage buffer which used C-element. The C-element helps in minimizing static power losses of the circuit by cutting off any leakage current flowing through it. The same can be observed in Figure 3.9, where the proposed level shifter shows better power performance with respect to DCL LS model

TABLE - 3.2 Delay and power analysis of different LS designs

LS model	Propagation delay (in ns)	Power dissipation (in nw)
Double current limiter based	12.309	57.04
RCC pull-up network based	5.405	1.8437
Reflected output WCMLS	4.349	1.564
Proposed Model	4.106	12.78

3.3 SUMMARY

From the various simulation data and results we have successfully ensured developing a voltage level shifter capable of converting near-threshold voltages to the super-threshold region with improved speed and minimized power losses. The proposed structure uses a low-power buffer and a pass transistor to enhance performance, overcoming the high delay issues associated with fall transitions in prior designs. With the utilization of only 11 transistors, the proposed circuit demonstrates its efficiency by converting input voltages as low as 0.3V to 1V output voltage. Implemented using 45nm CMOS technology, the voltage level shifter exhibits a power dissipation of 1.278nW and a propagation delay of 4.106 ns for a 0.4V/ 1 MHz signal, demonstrating significant improvements over existing designs. The Proposed structure can convert deep subthreshold voltages as well but delay will be significantly increased hence the proposed level shifter can be used in Near-threshold region and not below that.

CHAPTER 4

CONCLUSION AND FUTURE SCOPE

This work introduces a level shifter design that boasts both power and delay efficiency. The proposed schematic leverages a low-power output buffer fortified with a C-element to neutralize leakage currents, thereby curbing static power dissipation. To minimize delay, a pass transistor has been incorporated in the design, optimizing the fall transition delay and enhancing the overall operational speed. The design blueprint of the proposed circuit utilized 45nm CMOS technology. The post-layout analysis of this low-power, output buffer-based level shifter illustrates improved performance metrics in both power consumption and delay, showcasing an advantage over previous designs. The circuit has the capability to efficiently convert low input voltages of 0.3V to higher output voltages of 1V, accomplishing this feat with reduced power consumption. The scheme also elevates operational speed significantly.

The design demonstrates effective performance across an extensive range of voltages and temperatures, a testament to its versatility and robustness. Future improvements could focus on enhancing the sturdiness of the proposed design through the utilization of multi-threshold devices. The incorporation of body biasing could facilitate the creation of these multi-threshold devices, subsequently broadening the input voltage range that the level shifter can handle. This study sets the stage for the development of more efficient, high-performance level shifters that can significantly contribute to low power applications in digital circuit design.

REFERENCES

[1] V. L. Le and T. T. Kim, "An Area and Energy Efficient Ultra-Low Voltage Level Shifter With Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 5, pp. 607-611, May 2018, doi: 10.1109/TCSII.2018.2820155.

[2] Kyoung-Hoi Koo, Jin-Ho Seo, Myeong-Lyong Ko and Jae-Whui Kim, "A new level-up shifter for high speed and wide range interface in ultra deep sub-micron," 2005 IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, Japan, 2005, pp. 1063-1065 Vol. 2, doi: 10.1109/ISCAS.2005.1464775.

[3] M. Lanuzza, P. Corsonello and S. Perri, "Low-Power Level Shifter for Multi-Supply Voltage Designs," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 12, pp. 922-926, Dec. 2012, doi: 10.1109/TCSII.2012.2231037.

[4] Lanuzza, M. et al. (2017) “An ultralow-voltage energy-efficient level shifter,” IEEE Transactions on Circuits and Systems II: Express Briefs,64(1),pp.61–65. Available at: https://doi.org/10.1109/tcsii.2016.2538724.

[5] S. Lütkemeier and U. Rückert, “A subthreshold to above-threshold level shifter comprising a Wilson current mirror,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[6] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, pp. 388-391, 2015.

[7] P. Gosatwar and U. Ghodeswar, "Design of voltage level shifter for multi-supply voltage design," 2016 International Conference on Communication and Signal Processing (ICCSP), 2016, pp. 0853-0857, doi: 10.1109/ICCSP.2016.7754267

[8] L. Wen, X. Cheng, S. Tian, H. Wen and X. Zeng, "Subthreshold Level Shifter With Self-Controlled Current Limiter by Detecting Output Error," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 4, pp. 346-350, April 2016, doi: 10.1109/TCSII.2015.2504025.

[9] P. K. Machiraju and D. Y. Pushpamithra, "A novel energy efficient voltage level shifter," 2014 International Conference on Science Engineering and Management Research (ICSEMR), Chennai, India, 2014, pp. 1-4, doi: 10.1109/ICSEMR.2014.7043658.

[10] Kumar, M., Arya, S.K. and Pandey, S. (2010) 'Level shifter design for low power applications', International Journal of Computer Science and Information Technology, 2(5), pp. 124–132. doi:10.5121/ijcsit.2010.2509.

[11] Q. A. Khan, S. K. Wadhwa and K. Misri, "A single supply level shifter for multi- voltage systems," 19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06), 2006, pp. 4 pp.-, doi: 10.1109/VLSID.2006.24.

[12] S. N. Wooters, B. H. Calhoun and T. N. Blalock, "An Energy-Efficient Subthreshold Level Converter in 130-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 4, pp. 290-294, April 2010, doi: 10.1109/TCSII.2010.2043471.

[13] H. -C. Lee et al., "A High Voltage Driving Chiplet in Standard 0.18-μm CMOS for Micro-Pixelated LED Displays Integrated With LTPS TFTs," in IEEE Transactions on Circuits and Systems for Video Technology, vol. 32, no. 10, pp. 7204-7211, Oct. 2022, doi: 10.1109/TCSVT.2022.3168051.

[14] E. Låte, T. Ytterdal and S. Aunet, "An Energy Efficient Level Shifter Capable of Logic Conversion From Sub-15 mV to 1.2 V," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 11, pp. 2687-2691, Nov. 2020, doi: 10.1109/TCSII.2020.2966654

[15] M. Karimi et al., "A 1.99-ns 0.5-pJ Wide Frequency Range Level Shifter With Closed-Loop Negative Feedback," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 174-177, doi: 10.1109/NEWCAS49341.2020.9159830

[16] C. Q. Tran, H. Kawaguchi and T. Sakurai, "Low-power high-speed level shifter design for block-level dynamic voltage scaling environment," 2005 International Conference on Integrated Circuit Design and Technology, 2005. ICICDT 2005., Austin, TX, USA, 2005, pp. 229-232, doi: 10.1109/ICICDT.2005.1502637.

[17] S. Pashmineh and D. Killat, "Self-biasing high-voltage driver based on standard CMOS with an adapted level shifter for a wide range of supply voltages," 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2015, pp. 1-4, doi: 10.1109/NORCHIP.2015.7364405.

[18] X. Lai and F. Yuan, "Passive voltage level shifters for analog signaling," 10th IEEE International NEWCAS Conference, 2012, pp. 481-484, doi: 10.1109/NEWCAS.2012.6329061.

[19] R. Llanos, D. Sousa, M. Terres, G. Bontorin, R. Reis and M. Johann, "Energy-efficient Level Shifter topology," 2015 25th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2015, pp. 148- 151, doi: 10.1109/PATMOS.2015.7347600.

[20] K. Usami, M. Igarashi, F. Minami, T. Ishikawa, M. Kanzawa, M. Ichida, et al., "Automated low-power technique exploiting multiple supply voltages applied to a media processor," IEEE Journal of Solid-State Circuits, vol. 33, pp. 463-472, 1998.

[21] Kabirpour, S. and Jalali, M. (2020) “A power-delay and area efficient voltage level shifter based on a reflected-output Wilson Current Mirror Level Shifter,” IEEE Transactions on Circuits and Systems II: Express Briefs, 67(2), pp. 250–254. Available at: https://doi.org/10.1109/tcsii.2019.2914036.

[22] S. Gundala, M. M. Basha and S. Vijayakumar, "Double Current Limiter High Performance Voltage Level Shifter for IoT Applications," 2020 5th International Conference on Communication and Electronics Systems (ICCES), 2020, pp. 285-288, doi: 10.1109/ICCES48766.2020.9137901.

[23] S. Kabirpour and M. Jalali, "A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network," IEEE Transactions on Circuits and Systems II: Express Briefs, 2018

[24] H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy and S. Borkar, "Near-threshold voltage (NTV) design — Opportunities and challenges," DAC Design Automation Conference 2012, 2012, pp. 1149-1154

[25] S. R. Hosseini, M. Saberi and R. Lotfi, "An energy-efficient level shifter for low-power applications," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 2015, pp. 2241-2244, doi: 10.1109/ISCAS.2015.7169128.

[26] S. Karmakar, J. A. Chandy and F. C. Jain, "Design of Ternary Logic Combinational Circuits Based on Quantum Dot Gate FETs," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 5, pp. 793-806, May 2013, doi: 10.1109/TVLSI.2012.2198248.

[27] E. Maghsoudloo, M. Rezaei, M. Sawan and B. Gosselin, "A High-Speed and Ultra Low-Power Subthreshold Signal Level Shifter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64,no.5,pp. 1164-1172, May 2017, doi: 10.1109/TCSI.2016.2633430.

[28] https://whatis.techtarget.com/definition/CMOS-complementary-metal-oxide-semiconductor

[29] H. Kawaguchi, K. Kanda, K. Nose, S. Hattori, D. D. Antono, D.Yamada, T. Miyazaki, K. Inagaki, T. Hiramoto, and T. Sakurai, “A 0.5-V, 400-MHz, VDD-Hopping Processor with Zero-VTH FDSOI Technology,” ISSCC, Feb. 2003, pp. 106-107.

[30] R. N. Ray, M. M. Tripathi and C. I. Kumar, "High Performance Energy Efficient CMOS Voltage Level Shifter Design," 2022 2nd International Conference on Intelligent Technologies (CONIT), Hubli, India, 2022, pp. 1-5, doi: 10.1109/CONIT55038.2022.9847677.

[31] X. Hao, F. Yang, M. He, Y. Zheng, Y. Guo and H. Liao, "A 93.7% peak efficiency DC-DC buck converter with all-pass network based passive level shifter in 55 nm CMOS," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), 2016, pp. 445-448, doi: 10.1109/ISCAS.2016.7527266.