VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS IN IMPLEMENTATION OF FILTERS AND OSCILLATORS

Dissertation submitted in
Partial fulfilment of the requirement
for the award of the degree of

MASTER OF TECHNOLOGY
in
VLSI AND EMBEDDED SYSTEM DESIGN
by

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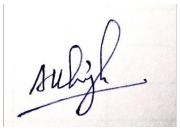
CERTIFICATE

This is to certify that the major project II titled "**VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS IN IMPLEMENTATION OF FILTERS AND OSCILLATORS**" is a bona-fide record of work done by **CHARU GUPTA, Roll No. 2K18/VLS/20** at **Delhi Technological University** for partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI Design and Embedded system. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.



Date: 25-8-2020

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CANDIDATE'S DECLARATION

I, CHARU GUPTA, Roll No 2K18/VLS/20 student of M.Tech (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project titled **"VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS IN IMPLEMENTATION OF FILTERS AND OSCILLATORS**" which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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Date: 24-8-2020

ACKNOWLEDGEMENT

Generally, individuals set aims, but more often than not, their conquest are by the efforts of not just one but many determined people. This complete project could be accomplished because of contribution of a number of people. I take it as a privilege to appreciate and acknowledge the efforts of all those who have, directly or indirectly, helped me achieving my aim.

I take great pride in expressing my unfeigned appreciation and gratitude to my learned mentor **Dr. A. K. SINGH,** Department of Electronics and Communication Engineering, DTU for his invaluable inspiration, guidance and continuous encouragement throughout this project work. His critics and suggestions on my experiments have always guided me towards perfection. This work is simply the reflection of his thoughts, ideas, concepts and above all his efforts. Working under his guidance has been a privilege and an excellent learning experience that I will cherish for a long time.

Finally, I extend my deep appreciation to my family and friends, for all that they meant to me during the crucial time of the completion of my project.

CHARU GUPTA

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ABSTRACT

The use of new, active building blocks is favoured for higher frequency range. Several active building blocks have recently been presented in which a powerful and versatile active building block is a VDCC (Voltage Differencing Current Conveyor).

It has features of both an operational transconductance amplifier and current conveyor such as low supply voltage and power, transferring both current and voltage to the respective terminals, well-developed IC topology and having electronically tunable transconductance. The VDCC is used in many applications in signal processing circuits, in particular in many oscillators and filters.

The work presented includes grounded and floating simulators of inductors, and their use in filter design. In addition, both grounded and floating inductance simulators use only one current conveyor (VDCC) differentiating voltage and few passive elements. It has been used in numerous filter-to-oscillator applications.

Multiplier capacitor circuit based on VDCC in which a grounded capacitance multiplies by a variable tuning factor. The value of this tuning factor is attuned by grounded VDCC resistances or transconductances.

New arbitrary general grounded impedance scaling configuration using two VDCCs and three grounded resistances was introduced. The circuit presented may increase or decrease the values of any generalized grounded impedance by variation in variation of bias current or grounded resistance.

Current-mode universal biquadratic filter composed of one VDCC and three grounded passive components based on VDCC. It realized all the five standard filtering function using same circuit structure with some changes in position of input current. This circuit is also capable of setting orthogonal control over Q (Quality factor) and ω_0 (Centre frequency).

In this project, I also analysed the working of three oscillator circuit and finally proposed one oscillator circuit base on VDCC. All three oscillators are quadrature oscillator. First oscillator circuit architecture, there's just one VDCC, two resistors and two condensers. It is regulated in current mode by single-resistance controlled

sinusoidal oscillators (SRCOs). It offers independent control of FO (Frequency of Oscillation) and CO (Condition of Oscillation) across various resistances. Hence, have independent CO and FO.

In second design of oscillator, the used VDCC block has some modification such as instead of W_n terminal copy of W_p is used. This is quadrature sinusoidal oscillator which consists of one VDCC, two capacitors and three resistors. CO and FO are independent of one another.

In third design of oscillator two VDCCs are used along with two resistors and capacitors. This oscillator produces sinusoidal quadrature oscillation in both current and voltage mode. CO and FO are independent of each other.

In my proposed design of oscillator used two VDCC, three resistors and two capacitors. All passive components are grounded which is perfect for IC monolithic manufacture. The oscillation frequency and the oscillation condition are independent of one another. Oscillators are used in numerous applications in the area of communications, control system, sound system, instruments etc.

All the simulation in this project and result verification is done on PSPICE software using 180nm technology.

CHAPTER 1

Introduction

1.1 Overview

For development of microelectronic circuits, the primary requirement is of extremely low supply voltage and lower power consumption. Extreme speed and accuracy are must be needed in many applications, to fulfill the above requirement many trade off solutions are used in practice.

Current mode circuits are added in the process of development of technologies which are used in analog signal processing. All the information is in the form of current in current mode circuits, whereas in voltage mode all information's are available in the form of voltage. Current mode circuits have various advantages as compared to voltage mode circuits such as it is less affected by voltage fluctuations, power consumption is low at higher frequency, low cross talk, switching noise is also low, speed of operation is high and it works well for low voltage and low power applications.

Active elements are required for various applications of analog signal processing, therefore development of active elements are very significant aspect in analog signal processing. In literature there are many active elements which is having electronically controllable property are introduced. They provide capability to single parameter control like voltage gain, input resistance, transconductance, transresistance and current gain. But recently multi parameter control methodologies of different types are introduced. General approach of voltage difference voltage at input is rectify to present VDCC (Voltage Differencing Current Conveyor). It is very useful device which is combination of OTA (Operational transconductance amplifier) as first stage and second generation of current conveyors (CCII) as second stage, both of them acts like sub blocks of VDCC active building block. OTA transconductance and input resistance of current input terminal of second-generation current conveyor (CCII) offers independent controlling of two parameters. But all the facts in the VDCC are theoretical and only simulation based. It is used in numerous applications several times. The CMOS based structure of VDCC block is as shown in Fig.1.3. Different applications use CMOS based structure of VDCC.

Two active blocks form VDCC block one is operational transconductance amplifier (OTA) and second one is MO-CCII (multiple output current conveyor II). VDCC structure from inside is shown in Fig.1.1.

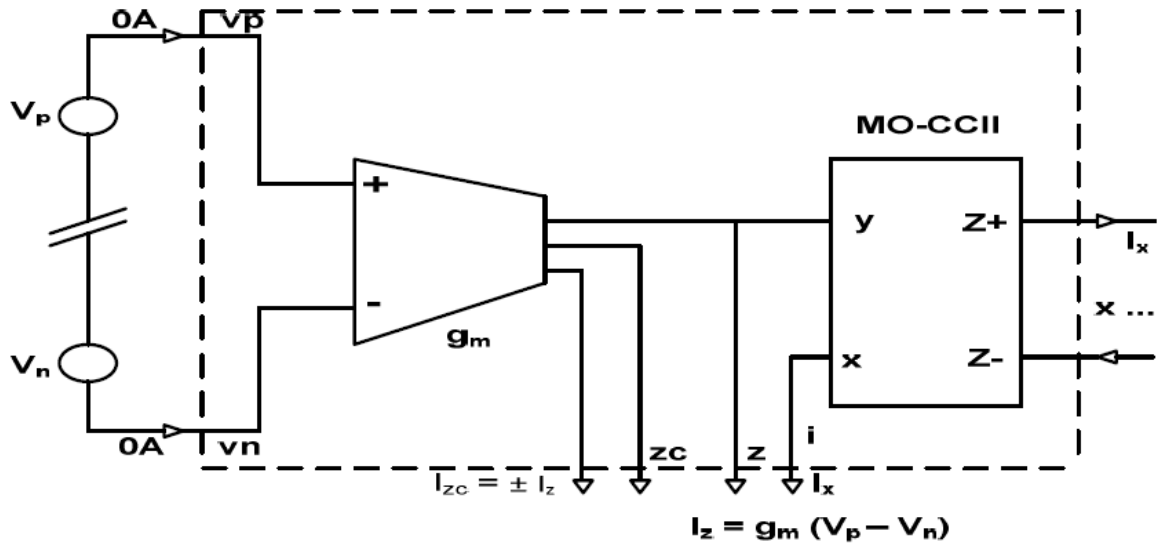

Fig.1.1 VDCC block with activated elements [1]

1.2 Current Conveyor Differentiated Voltage (VDCC)

The active VDCC Description building block is as shown in Fig. 1.2, has six terminals, input terminals P and N are input terminals and W_p, W_n, Z, X are output terminals and all terminals have a high input impedance except for X terminal.

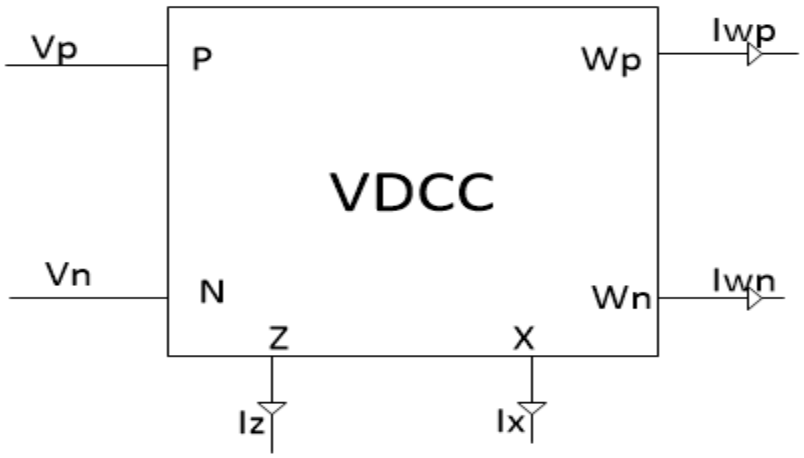

Fig.1.2 Circuit symbol of the VDCC [5]

The ideal VDCC matrix for port is as shown below:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

From this matrix the equation of currents and voltages is obtained as::

$$I_z = g_m (V_P - V_N)$$

$$V_X = V_Z$$

$$I_{WP} = I_X$$

$$I_{WN} = -I_X$$

Transconductance gain (g_m) is obtained from above equation by converting differential input voltage (V_p - V_n) to output current (I_z) and next stage is current conveyor in which the current is transferred from X terminal to W_p and W_n terminals. Transconductance gain for balanced CMOS (complementary semiconductor of metal oxides) is as follows:

$$g_m = \sqrt{\mu_n C_{ox} I_B (\frac{W}{L})}$$

In this case μ_n is the mobility of the NMOS transistor carrier, L and W are the effective channel length and width respectively, C_{ox} is the oxide capacitance per unit area and I_B is the bias current. As shown in Fig 1.3, VDCC implementation using CMOS has 22 transistors in its circuit as shown with supply voltages as V_{DD} and V_{SS}, and biasing currents are I_{B1} and I_{B2}. Aspect ratios (W and L ratio) of each transistor are modified to match the application requirement.

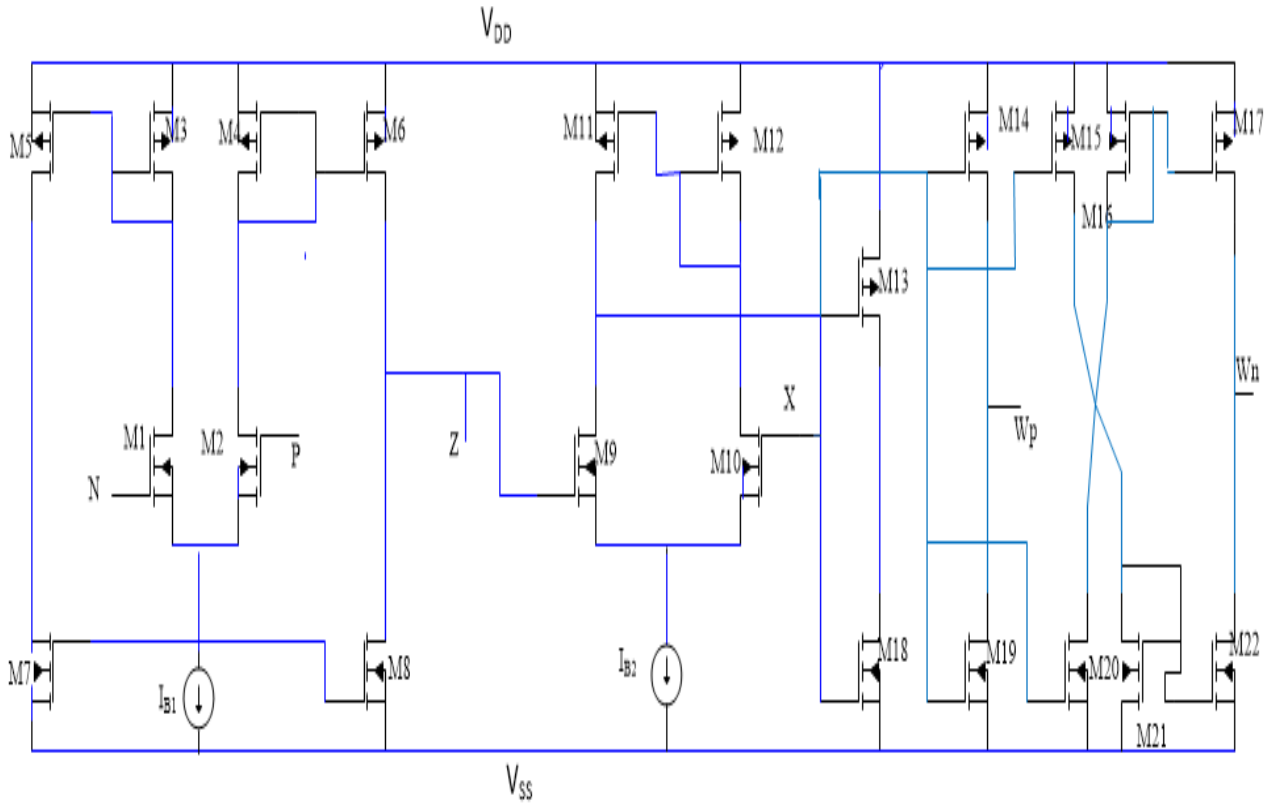

Fig.1.3 CMOS implementation of the VDCC [5]

CHAPTER 2
Simulation of inductance based on VDCC and design filter

2.1 Introduction

Inductance realization in integrated circuits creates various problems in systems. For several reasons such as spreading passive inductors magnetic energy and more parasitic effect compared to other elements and bulky in IC, passive inductance is not used instead of inductance simulators at high frequency. There are different types of grounded and floating inductance simulators being implemented using active building blocks such as operational amplifiers (op-amps), current conveyors, operational feedback amplifiers, current controlled conveyors, operational mirrored amplifiers, current differencing buffered amplifiers (CDBA), etc. Inductance simulators previously introduced suffer from the various drawbacks:

1. Needs passive components to match condition.
2. Usage of three or more participating active numbers.
3. Usage of passive components in large numbers.
4. Currently simulators of negative and lossy inductance have been learned.

Numbers of active building blocks have recently been introduced, the VDCC (Voltage Differentiating Current Conveyor) is one of the active building blocks providing electronically tunable transconductance gain along with transfers of both voltage and current to their respective terminals, and is also used in the design of multiple types of inductance simulators and active filters by using minimums

2.2 The structure of VDCC-based inductance simulator

The inductance simulator based on VDCC is the way shown in Fig.2.1. It uses one VDCC structure with one grounded capacitor and one resistor. The VDCC's P and W_N terminals are grounded like shown. The grounded inductor is indicated in Fig. 2.1 and the arrangement of the floating inductor is shown in Fig. 2.2, both using a single VDCC structure with one resistor and one capacitor.

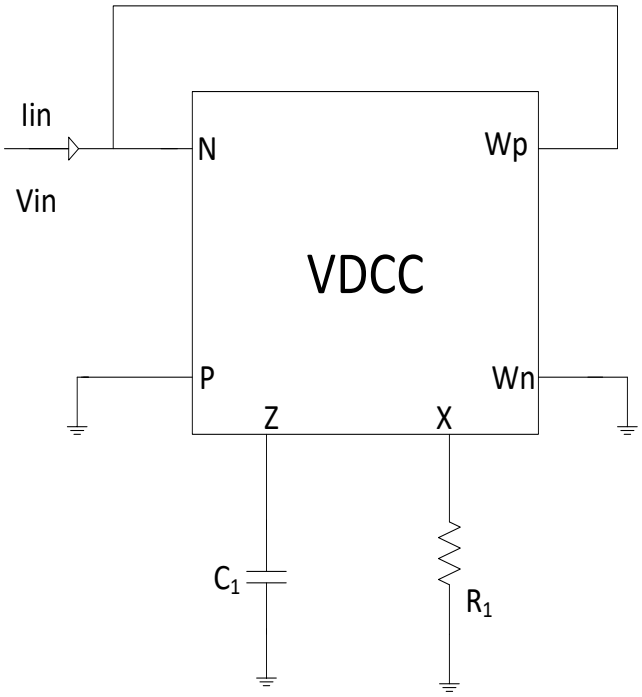

Fig. 2.1. Grounded inductance simulator [5]

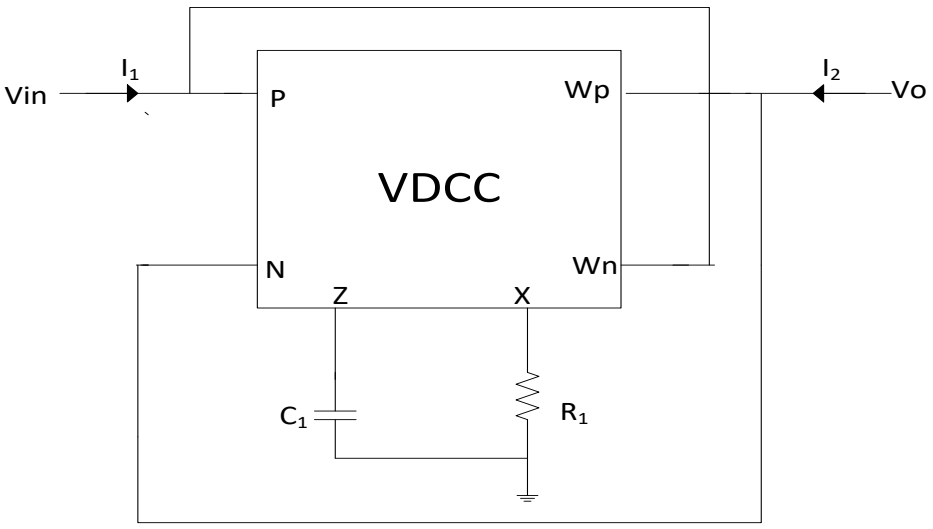

Fig.2.2. Floating inductance simulator [6]

2.3 Impact on VDCC of parasitic impedance in grounded inductor

Influence of parasitic impedance is inspected in order to determine the performance of the inductance simulator in different frequency regions. Fig.2.1 shows the pure inductance simulator now considering modified topology with certain parasitic impedances and the non-ideal equivalent circuits shown respectively in Fig.2.3. Continuing to follow from Fig. 2.3(a), RP3 appears on Z terminal resulting in first stage output resistance while RP1, RP2, CP1 and Lx appear on WP and X terminals in second stage. Impedance of the inductance simulator can be formulated in the light of the above effects as:

$$Z_{IN} = R_{P1} // \frac{1}{sC_1} // [s(\frac{C_1(R_1+R_{P2})}{g_m}) + \frac{L_X}{g_m R_{P3}} + \frac{(R_1+R_{P2})}{g_m R_{P3}} + \frac{s^2 C_1 L_X}{g_m}]$$

The circuit elements are derived from this equation as from Fig. 2.3(b)

$$L_{Equ} = (\frac{C_1(R_1+R_{P2})}{g_m}) + \frac{L_X}{g_m R_{P3}}$$

$$R_S = \frac{(R_1+R_{P2})}{g_m R_{P3}} - \frac{\omega^2 C_1 L_X}{g_m}$$

$$C_P = C_{P1}$$

$$R_P = R_{P1}$$

Parasitic inductance Lx is the element influencing L_{Equ}. From Fig. 2.3[b], it can be shown that the low frequency region of the inductance limits the RS series resistance, the value of which depends primarily on the R_{P2} and R_{P3} parasitic resistances. As the R_S resistance value decreases, the output impedance at port Z (R_{P3}) increases. Cascade techniques are being used to implement this. Negative resistance achieved by active elements can be overcome by terminal Z balancing the R_{P3} and increasing the region of the low frequency field. Whereas, the high-frequency performance of the circuits is governed by R_P and C_P, which are equal to R_{P1} and C_{P1}. In addition to these lower C_{P1} values and higher R_{P1} values, the high frequency performance of the circuit will be improved. Also, from the above equations in high-frequency regions, the value of R_S resistance is affected by both ω_0 and L_X. In high frequencies, therefore, the R_S resistance value may be negative, which may eventually result in a stability problem.

In order to prevent this, $R_S>0$ should be satisfied which results in the following inequalities:

$$\left(\frac{R_{P1}+R_{P2}}{R_{P3}}\right) > (2\pi f)^2 C_1 L_X$$

Where f is operating frequency and maximum operating frequency, without affecting stability

$$f_{max} = \frac{1}{2\Pi}\sqrt{\frac{R_1+R_{P2}}{C_1 L_X R_{P3}}}$$

Now parasite inductance (Lx) must be reduced to increase X terminal fmax.

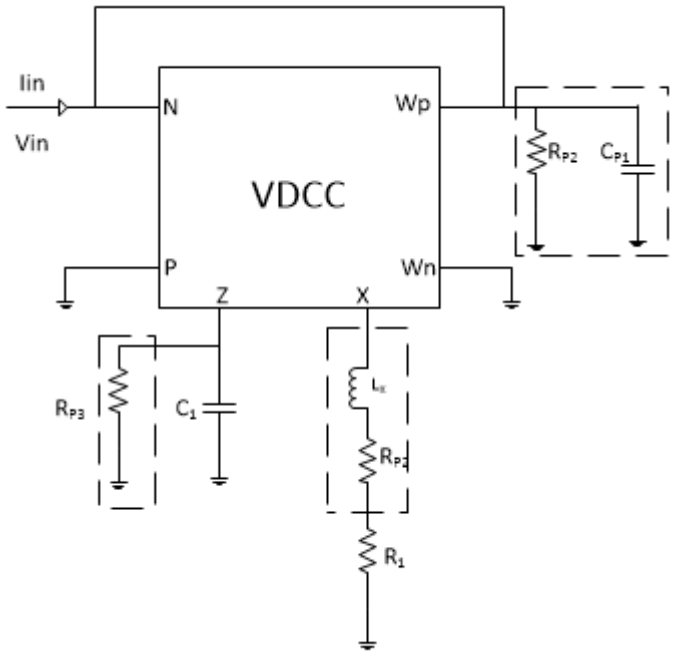

Fig 2.3 (a) Parasitic-component inductance simulator [5]

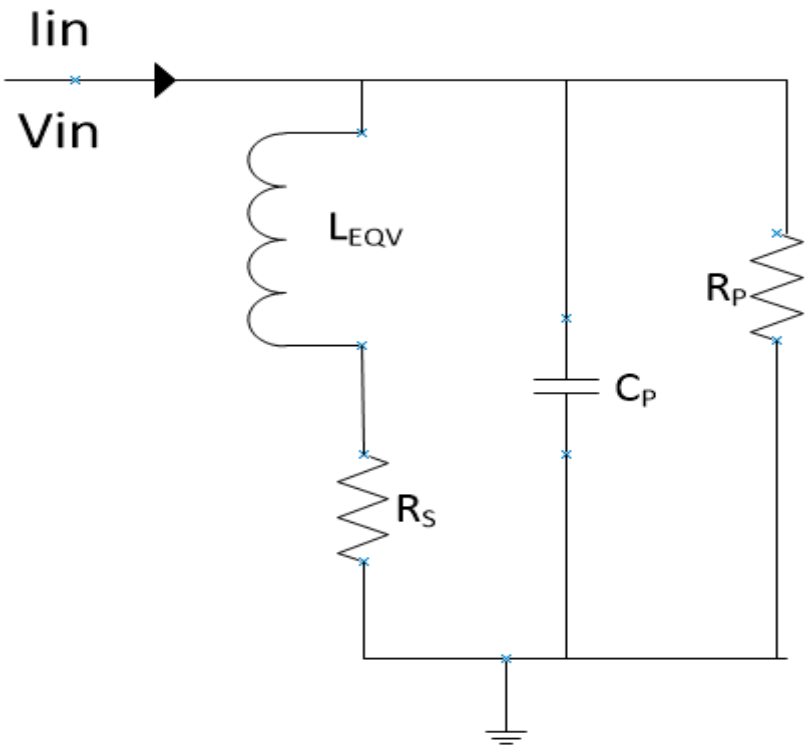

Fig.2.3 (b) Parasitic impedances effect on VDCC [5]

2.4 3rd order Butterworth High Pass filter

To examine the performance of the grounded simulated inductor, we form the High Pass butterworth filter in third order as shown in Figure 2.4.In passive structure of High Pass butterworth filter we replace grounded inductor by simulated inductance based on VDCC

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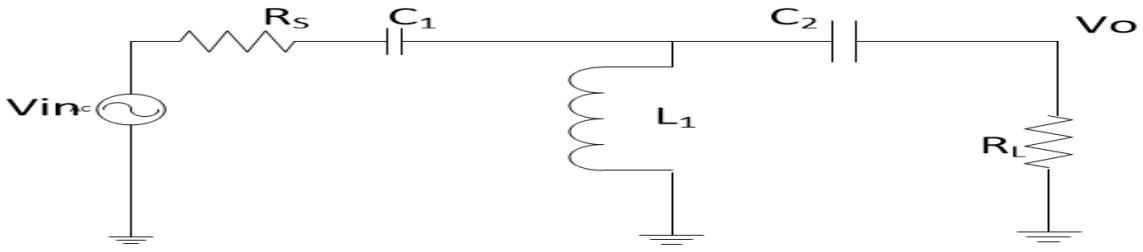
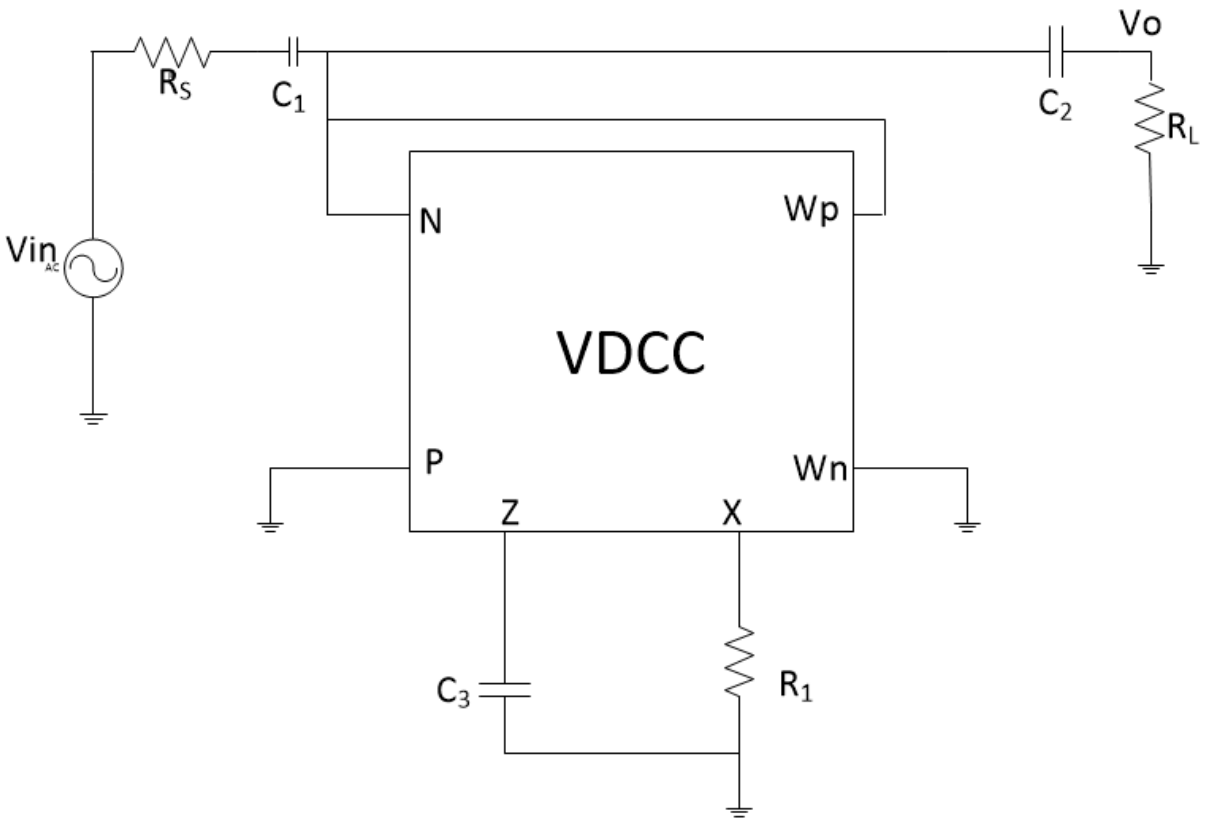


(a)



(b)

Fig 2.4 Butterworth third-order filter (a) Passive realization (b) VDCC-based simulation of inductance

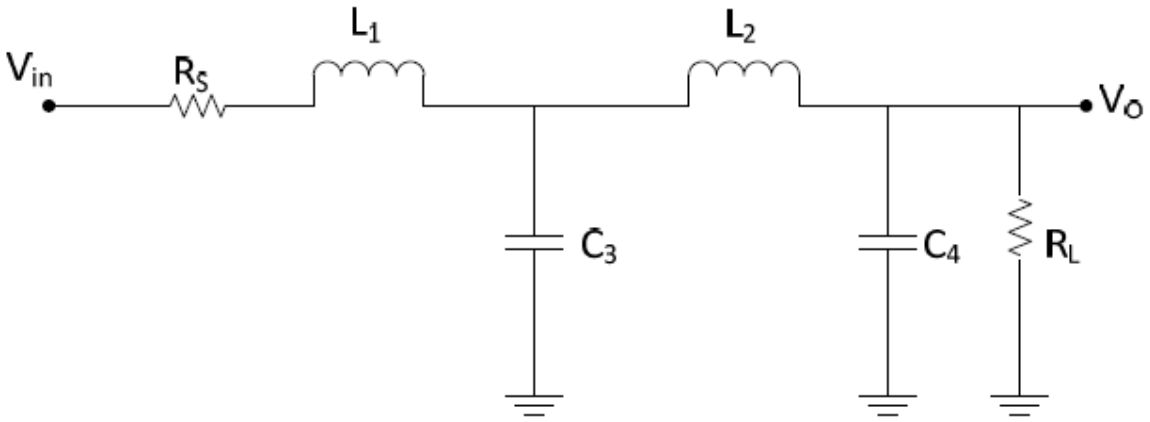
2.5 4th order Low Pass Butterworth filter ladder

Figure 2.5(a) shows a passive prototype of the fourth order Low Pass butterworth lader filter. Floating inductor is used in this circuit which can be replaced by the simulated inductance. Figure 2.2 shows the simulated floating inductance based on VDCC which is used to design a fourth-order LPF as shown in figure 2.5(b).The transfer function for fourth order low pass butterworth filter is given by

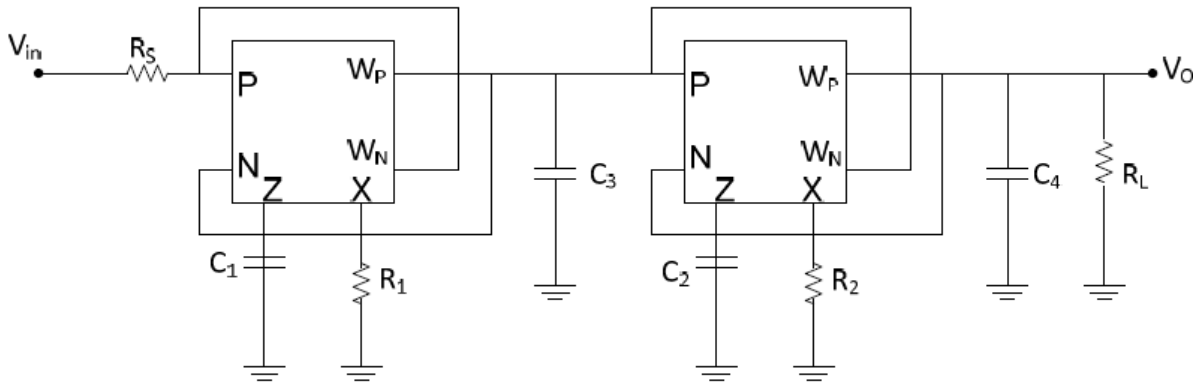
$$\frac{V_o}{V_{in}} = \frac{\frac{1}{L_1L_2C_1C_2}}{S^4+S^3\left(\frac{R_S}{L_1}+\frac{1}{R_LC_4}\right)+S^2\left(\frac{1}{L_1C_3}+\frac{1}{L_1C_3}+\frac{1}{L_1C_3}+\frac{R_S}{R_LC_4L_1}\right)+S\left(\frac{1}{L_1R_LC_4C_3}+\frac{R_S}{L_1L_2C_4}+\frac{1}{L_2R_LC_4C_3}+\frac{R_S}{L_2C_3L_1}\right)+\left(\frac{1}{L_1L_2C_1C_2}+\frac{R_S}{L_1L_2C_3C_4R_L}\right)}$$

Where $L_1 = \frac{R_1C_1}{g_{m1}}$ and $L_2 = \frac{R_2C_2}{g_{m2}}$

g_{m1} and g_{m2} are transconductances of two VDCC blocks respectively.



(a)



(b)

Fig. 2.5. Fourth order Butterworth Low Pass filter (a) Passive prototype (b) floating inductor simulator based on VDCC[6]

2.6 Simulation and Results

Simulation is performed using PSPICE software to verify the operation of the circuit. The technology parameter used is of TSMC 180 nm. Value of Width to length (W / L) ratios of each transistor used in VDCC CMOS [5] is shown in Table 5.1. $V_{DD}= -V_{SS}=0.9V$ are the supply voltage values and the bias current is $I_{B1}=50\mu A$ and $I_{B2}=100\mu A$ respectively, therefore the trans-conductance value obtained is $g_m=277.833\mu A / V$.

Simulation of inductance is performed on the circuit shown in Fig.2.1 with the passive component values $R_1=4K$ and $C_1=20$ pF corresponding to the inductance value $L_{eq}=0.29mH$. The value of parasite elements as shown in Fig.2.3 is $R_{P1}=141$ K, $R_{P2}=.043$ K, $R_{P3}=362k$, $C_{P1}=0.91pF$ and $L_x=2.2\mu H$.

The inductor and ideal inductor based on VDCC is simulated, and its impedance vs. frequency characteristics are shown in Fig.2.9. And it is concluded that, within the frequency range 30kHz to 20MHz, the ideal and VDCC dependent simulated responses are almost identical. By using this inductance simulator using VDCC we build High Pass filter in third order by replacing inductor. $R_S= R_L= 9K$ and $C_1= C_2= 16$ pF and $L_1= .795mH$ are passive element values. Simulation and response of it is shown in Fig 2.20 and Fig 2.21.

To build third order High Pass filter as shown in Fig 2.4 the value of passive components are $R_L = R_S = 9K$ and $C_1 = C_2 = 16pF$ and $L_1 = 796.77uH$. And the value of passive component used in simulation of inductor based on VDCC as $R_1= 4\ k\Omega$ and $C_3= 20$ pF. That results in a 1MHz frequency of 3dB. Figure 2.19 and Figure 2.21 shows the output of both an ideal and simulated third-order high pass filter.

To design the circuit of 4^{th} order butterworth filter as shown in Fig 2.4 (a), the passive elements are selected as $R_L = R_S = 2K\Omega$ and $C_1 = 0.1384nF$, $C_2 = 0.03nF$ and $L_1 = L_2 = 0.2434mH$ and its response is shown in Fig 2.23. By using floating inductance simulator as shown in Fig 2.2 instead of inductor form fourth order low pass filter and its response is shown in Fig 2.25. taking the value of passive components are as $R_1 = 3.23K\Omega$, $R_2 = 8K\Omega$ and $C_3 = C_4 = 1n$.

Table 2.1

Transistors	W/L(µm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

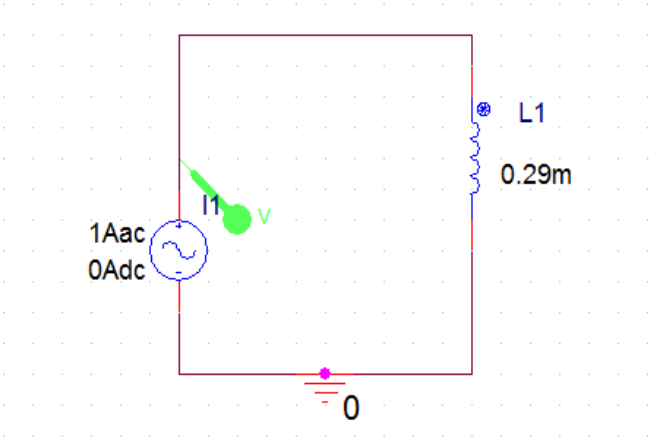


Fig.2.6 Schematic of Passive inductor [5]

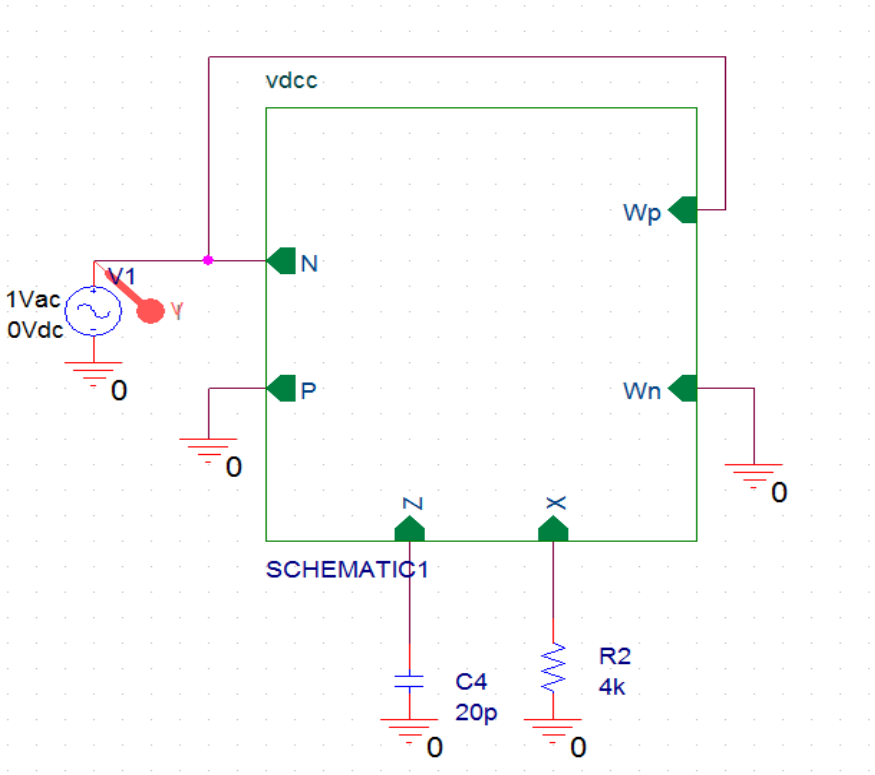


Fig. 2.7 Schematic of inductance simulator [5]

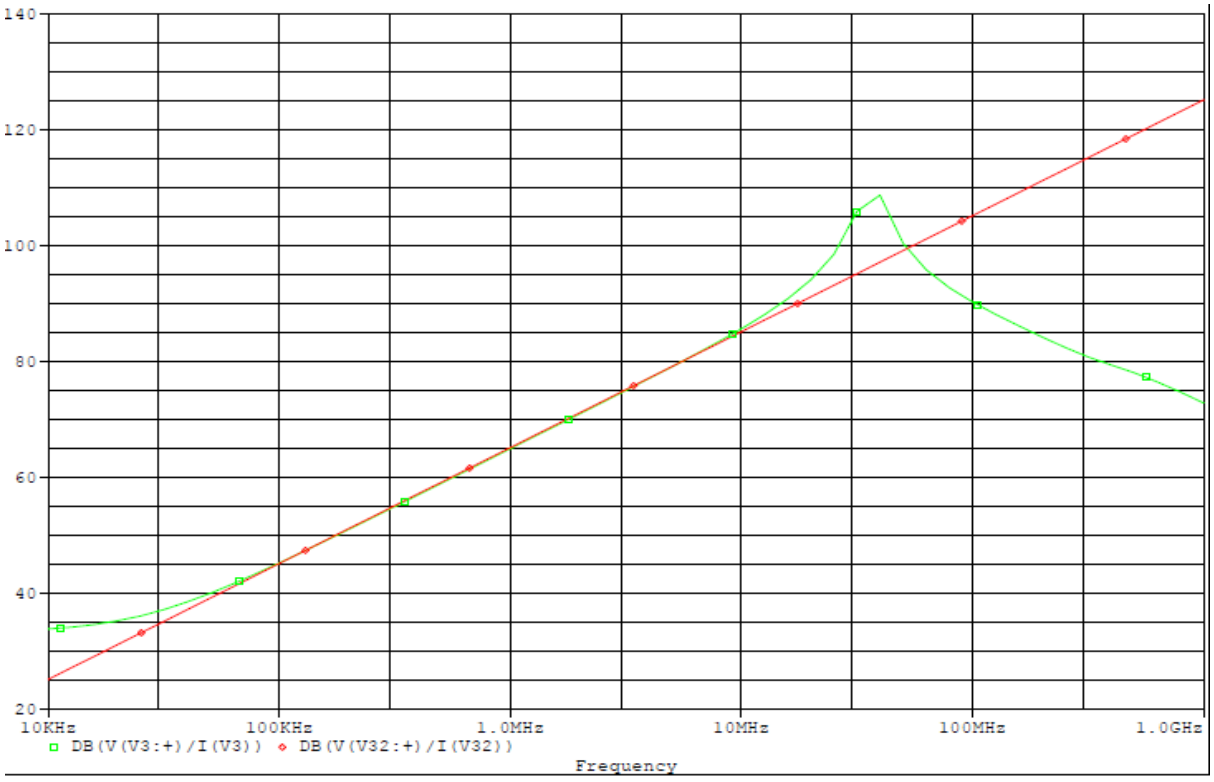


Fig 2.8 VDCC-based inductance simulator & passive inductor response

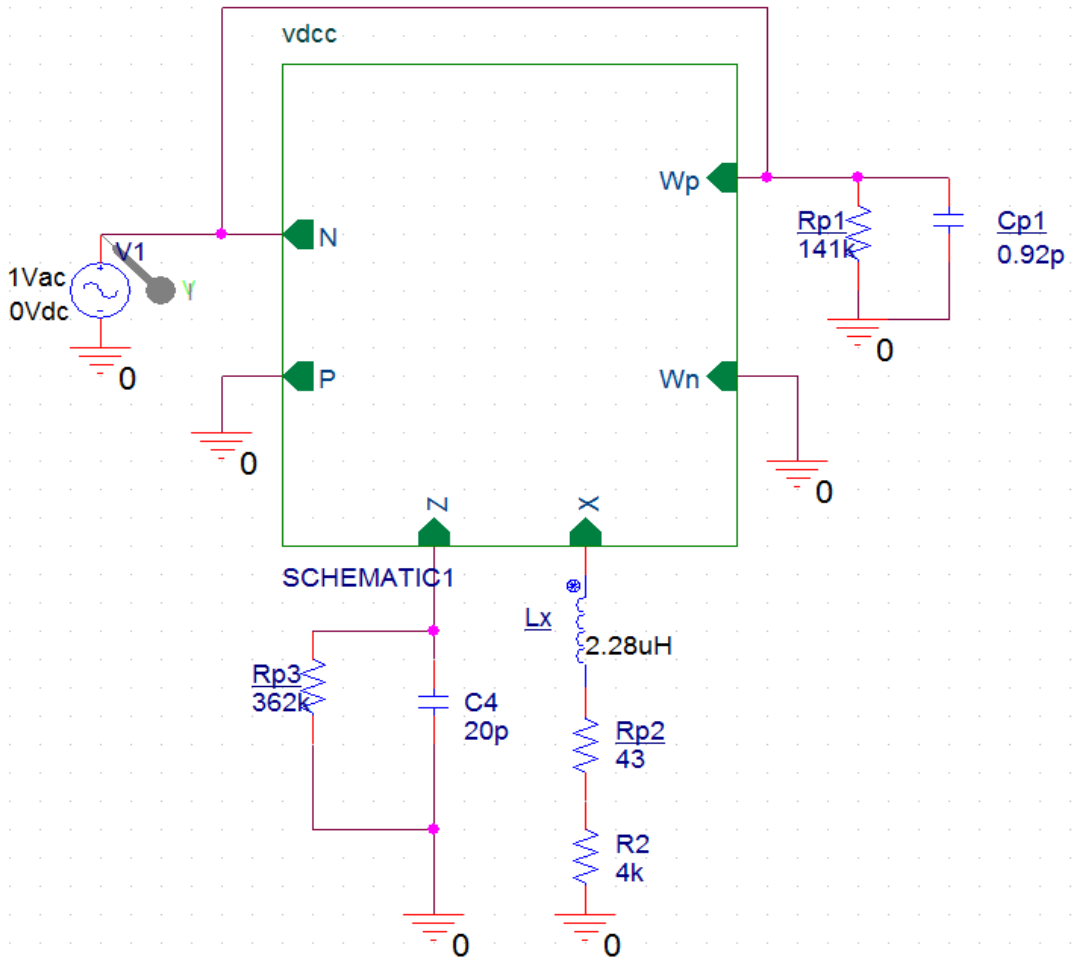


Fig.2.9 Parasitic-element inductance simulator schematic [5]

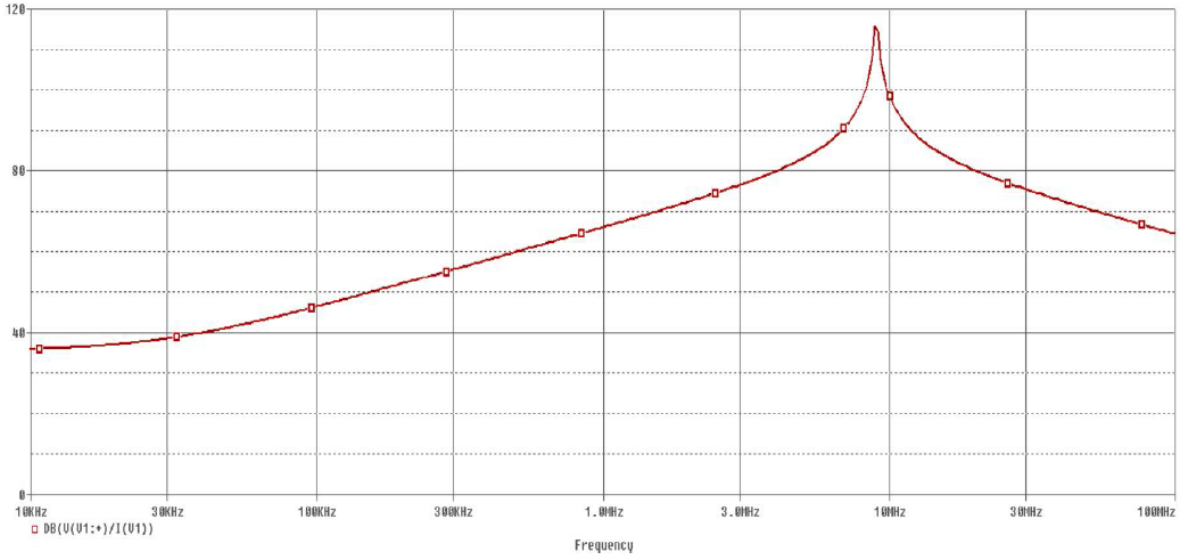


Fig. 2.10 A simulator inductance response with parasitics elements

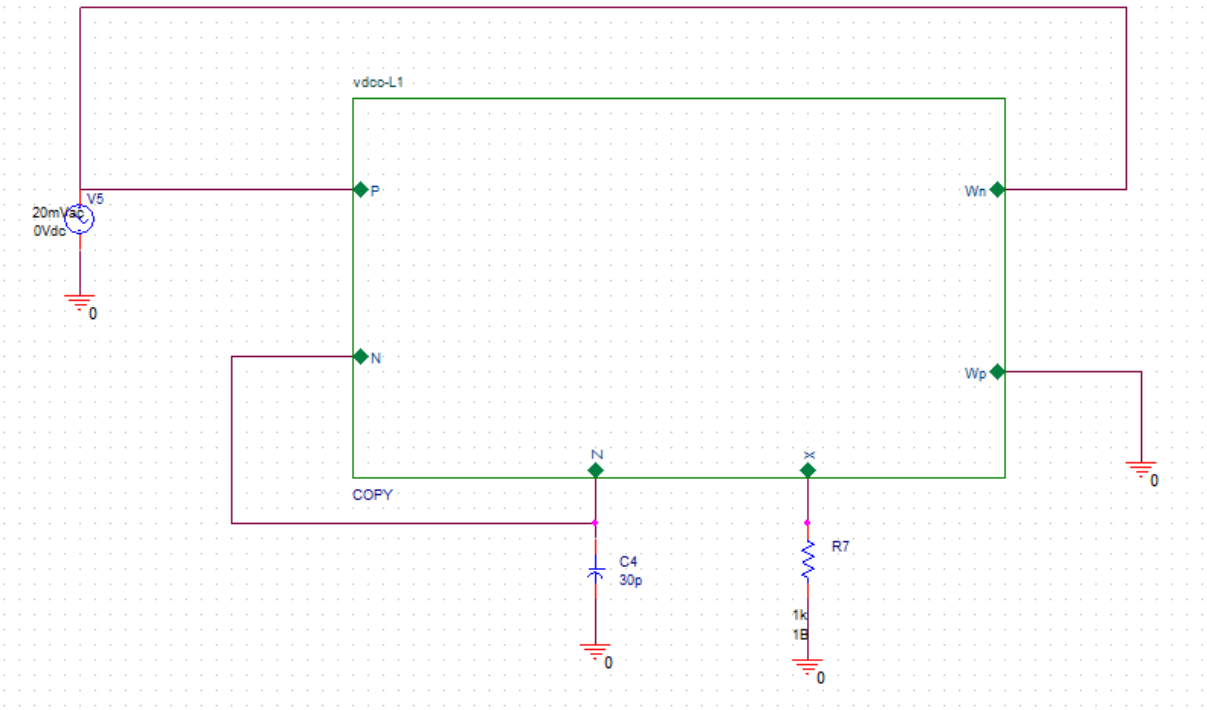


Fig. 2.11 Schematic of inductance simulator (L series with R) [5]

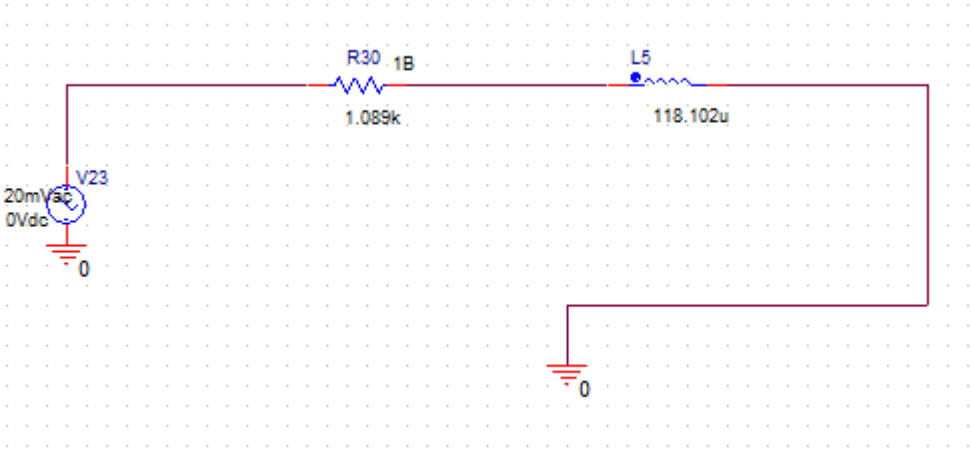


Fig 2.12 Schematic of equivalent of inductance simulator [5]

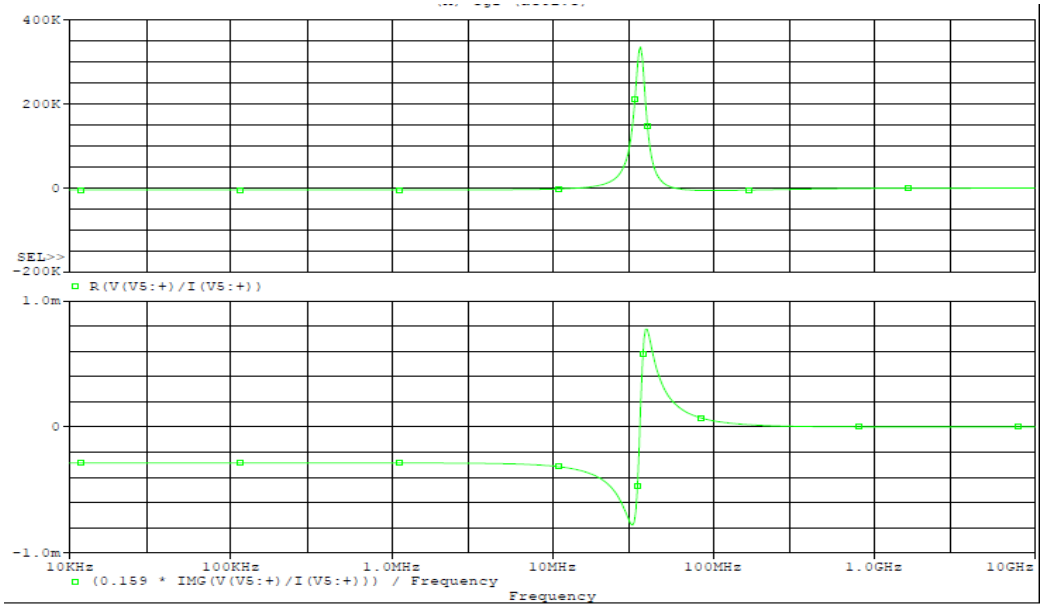


Fig 2.13 Response of inductance vs frequency VDCC based inductance simulator

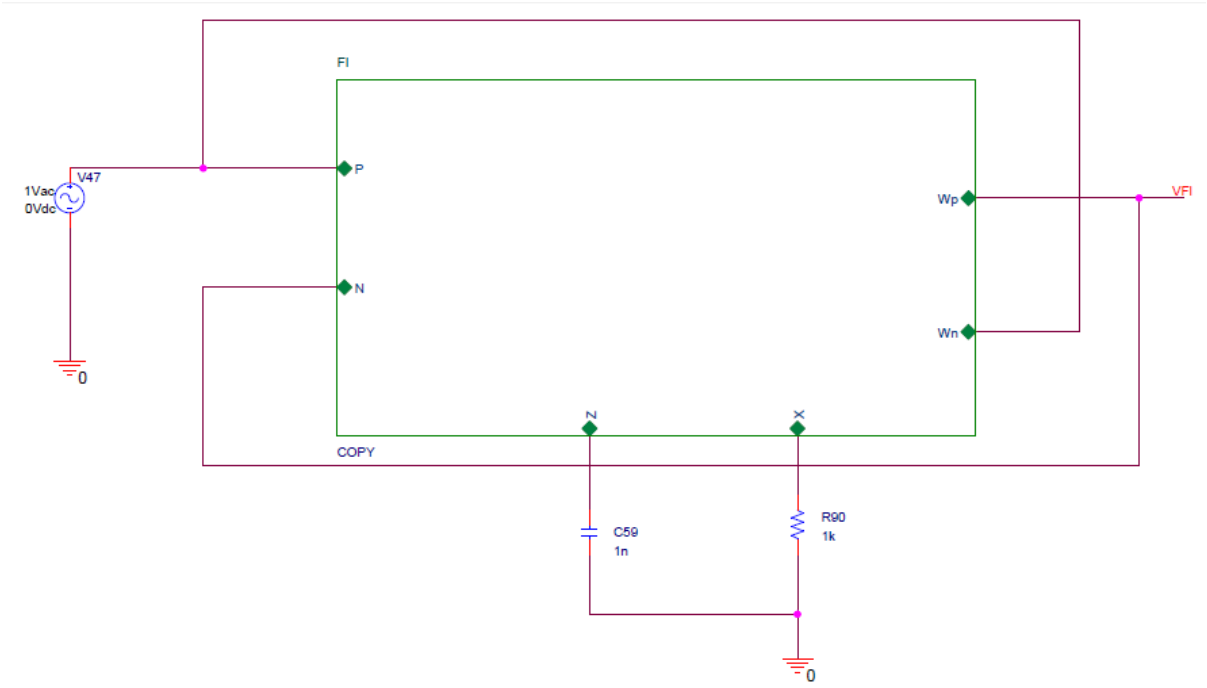


Fig.2.14 Schematic of Floating inductance simulator [6]

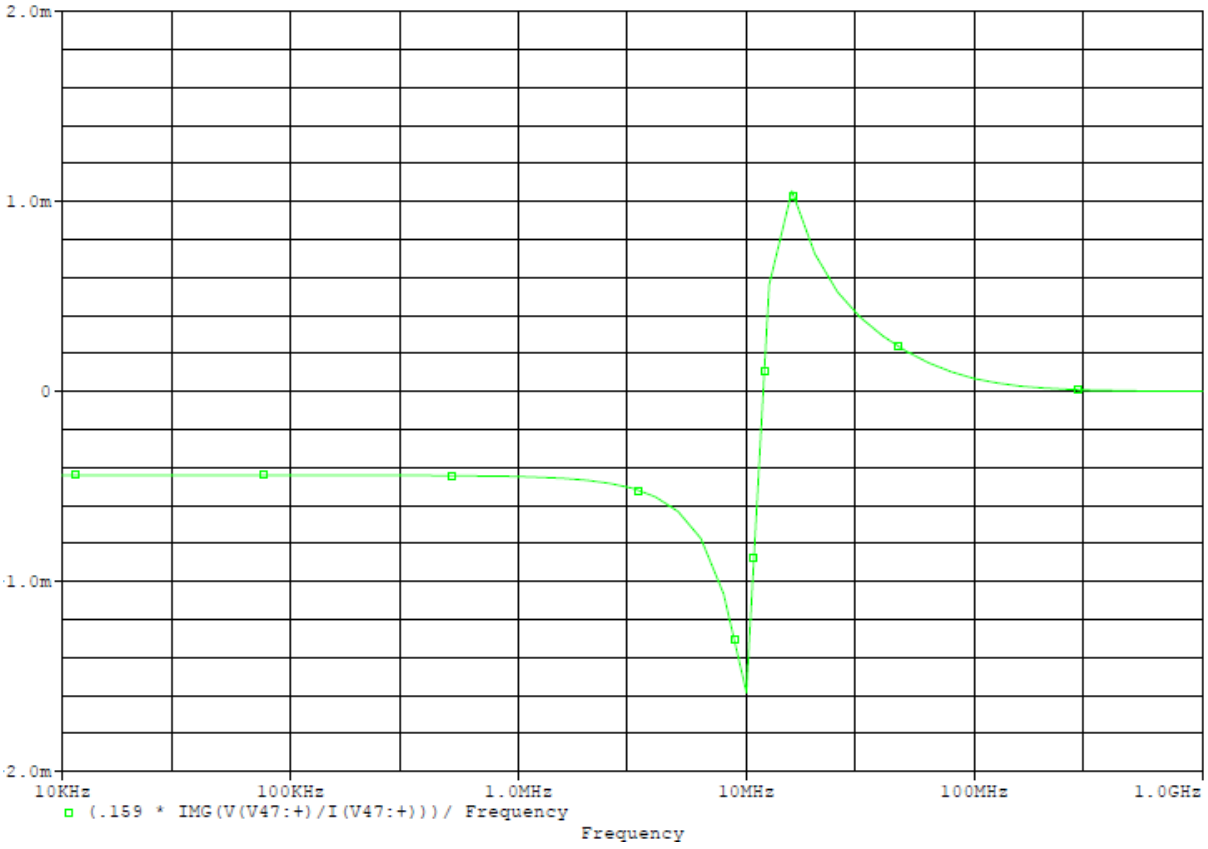


Fig 2.15 Plot of inductor of floating inductance simulator

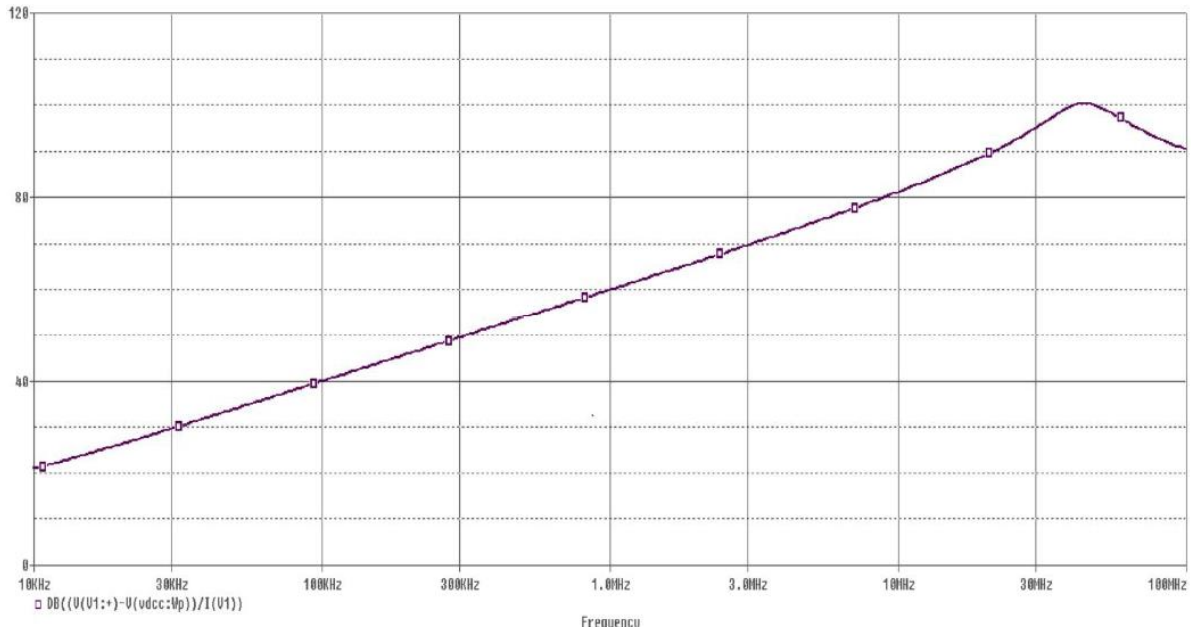


Fig. 2.16 Impedance vs. Simulator frequency of floating inductance response

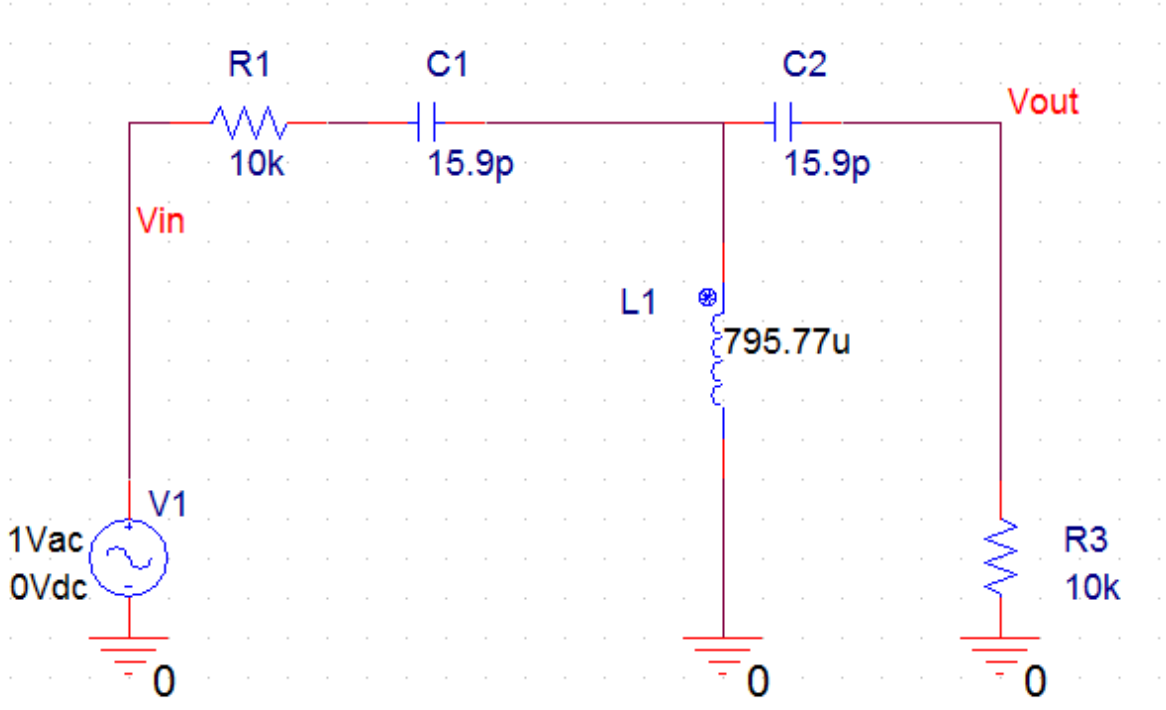


Fig.2.17 Third-order schematics High Pass Butterworth filter Passively realized [5]

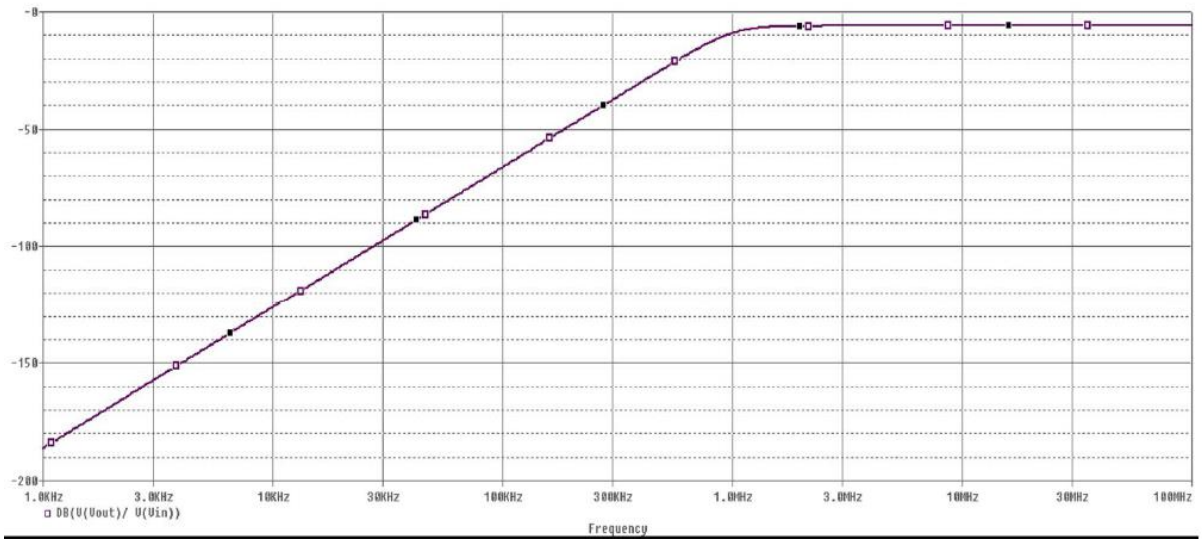


Fig. 2.18 Third-order response of High Pass Butterworth filter Passively realized

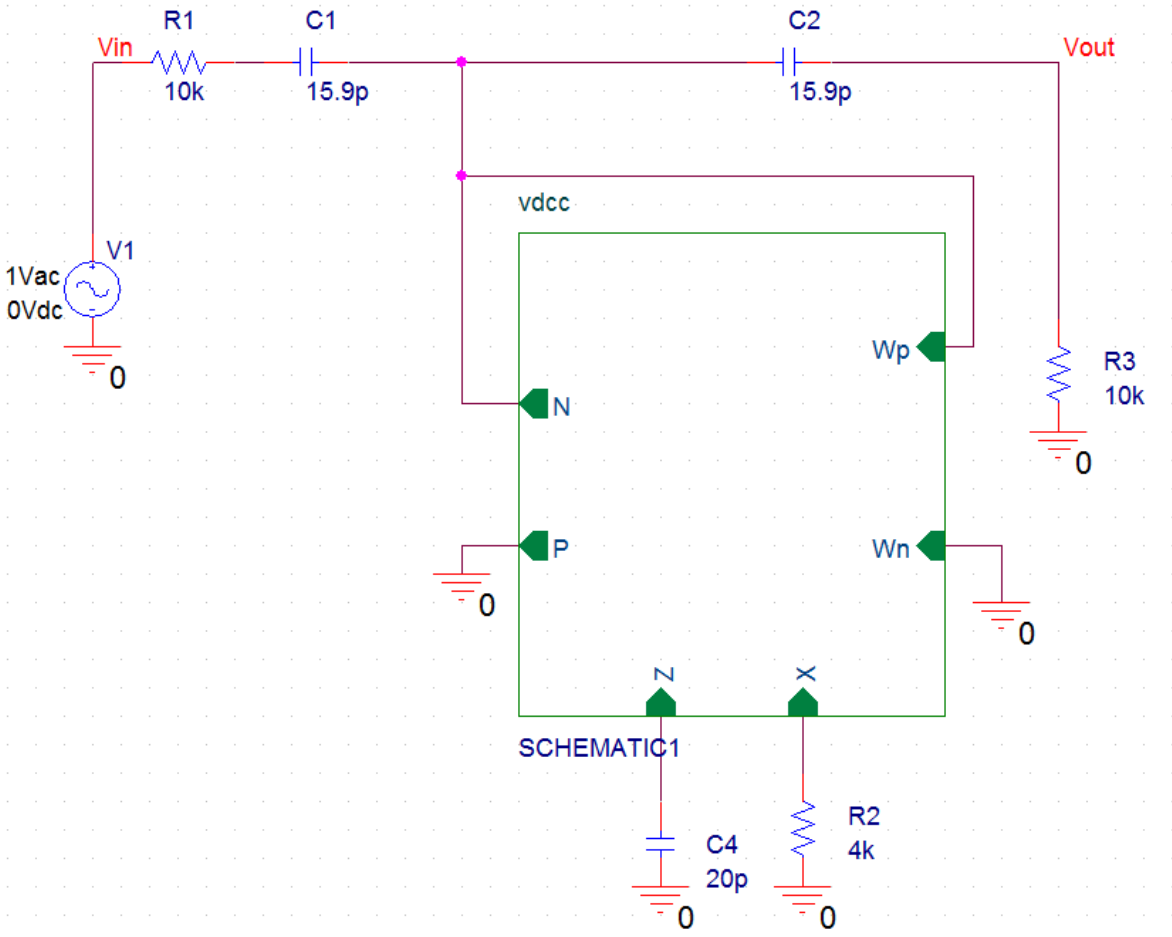


Fig.2.19 Realization of third order High Pass Butterworth filter based on inductance simulator schematic [5]

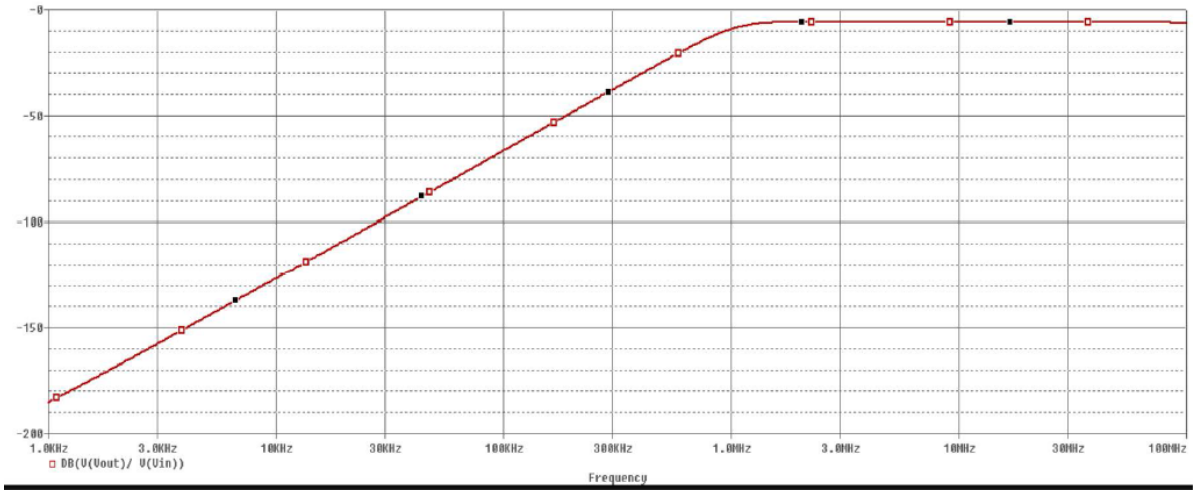


Fig. 2.20 Simulator-based inductance response of third-order High Pass Butterworth filter

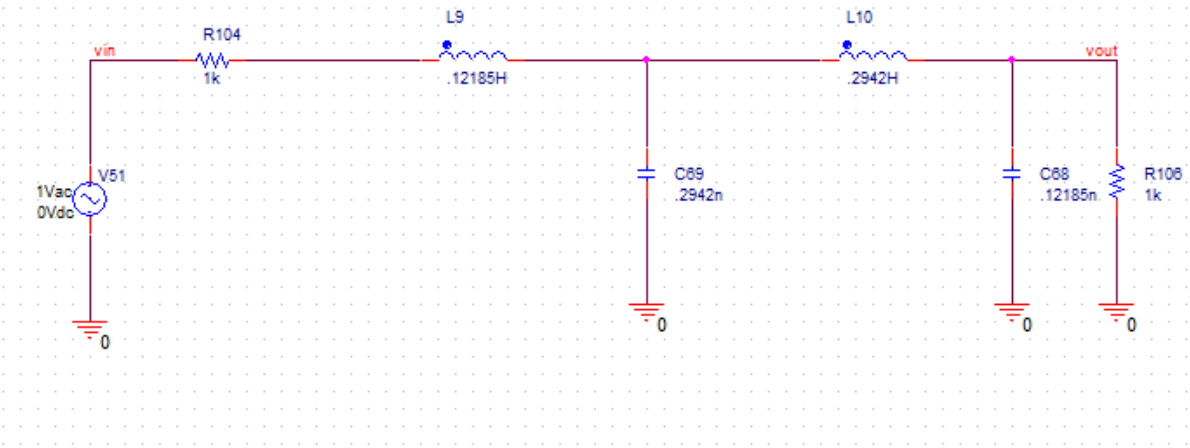


Fig.2.21 Passively realized 4th-order Low Pass Butterworth filter schematic [5]

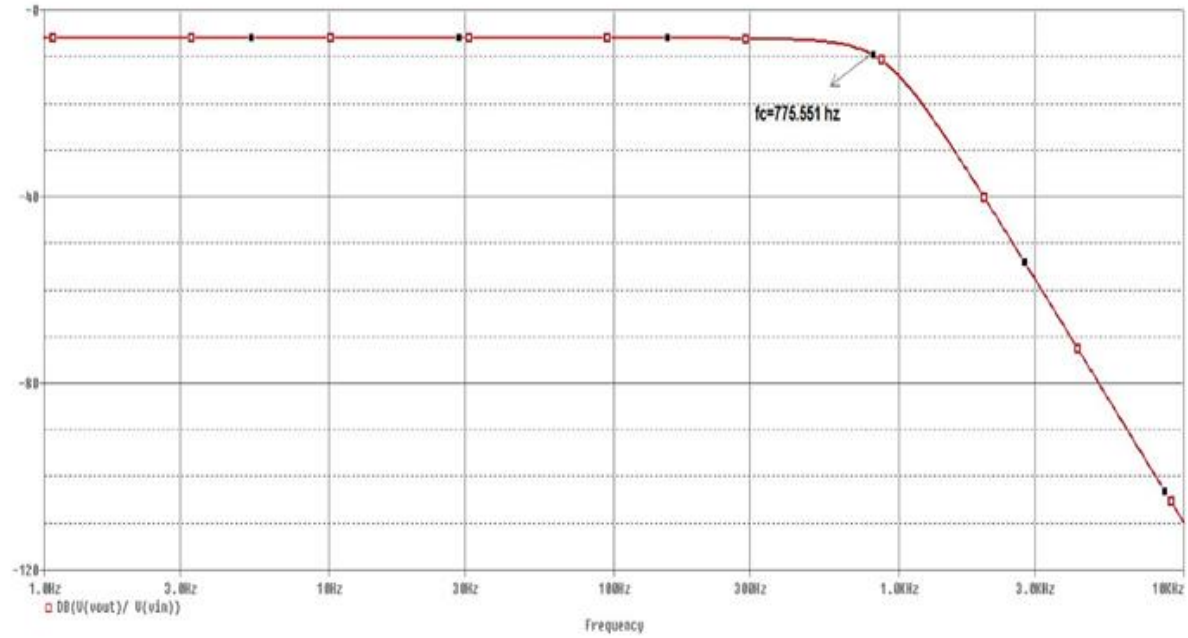


Fig. 2.22 Passively realized fourth order response of Low Pass Butterworth filter

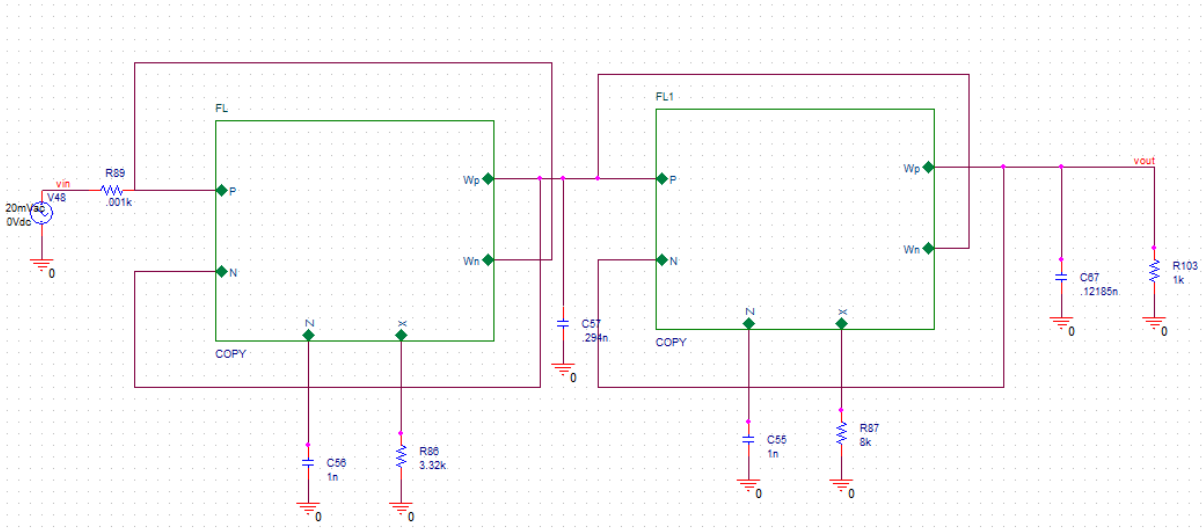


Fig.2.23 Realization of 4th-order High Pass Butterworth filter based on inductance simulator schematic [5]

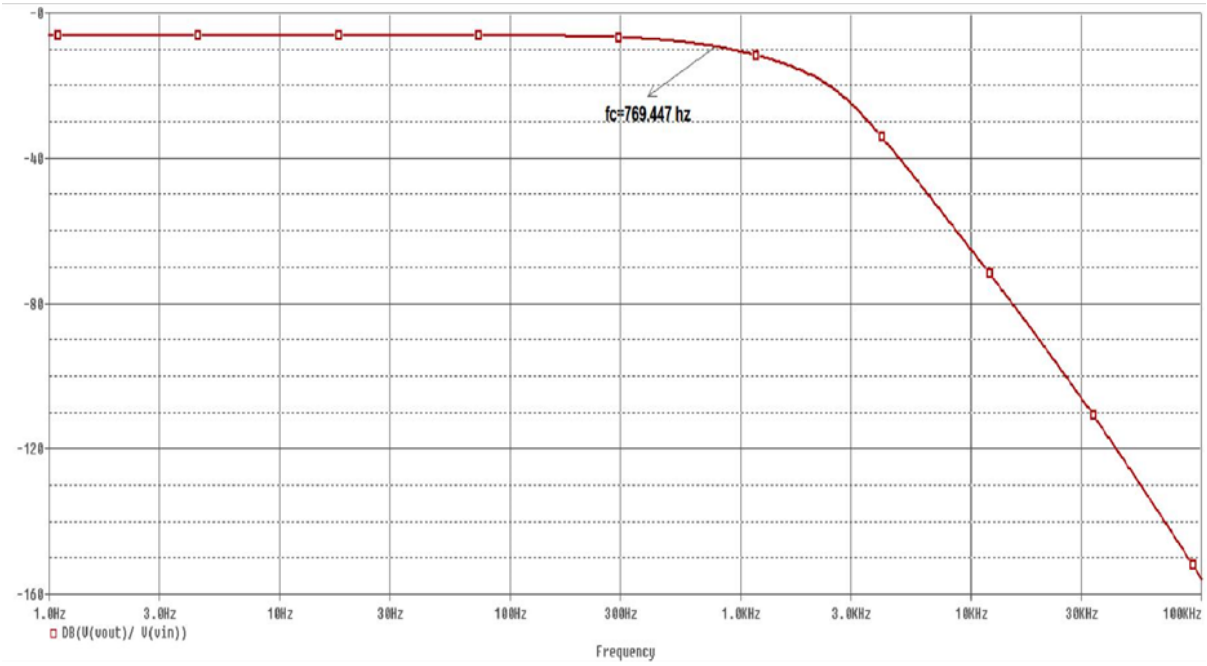


Fig.2.24 Simulator-based inductance response of the fourth-order Low Pass Butterworth filter

CHAPTER 3

CAPACITOR MULTIPLIER CIRCUIT WITH VDCCs

3.1 Introduction

A capacitance is a passive element that in almost all electronic systems has different applications. Large value capacitances are needed in many analog circuit applications as oscillator circuits, active filtering circuits, and circuit parasite cancellation. But, it is not possible to use condensers of great value in integrated circuits as their monolithic manufacturing is difficult. Therefore, it is preferable to use low value condenser and multiply it by desired value using a capacitance multiplier circuit.

Throughout literature, researchers have documented various capacitance multiplier circuits from different active components. Also reported were capacitance multipliers based on operational transconductance amplifier (OTA), which have the advantage of electronic tunability but the problem is that dynamic range is poor. Similarly, floating impedance inverter capacity multiplier was presented that has electronic control facilities but limited high frequency behaviour.

Voltage differencing current conveyor (VDCC) generates a new multiplier capacitance circuit. The design presented is composed of two VDCCs and three grounded resistors.

The circuit has the advantages:

1. Electronic / resistance adjustable multiplication factor
2. Grounded resistors are used which make this configuration suitable for implementation on the chip.
3. This does not require matched resistors or VDCCs.
4. Under non-ideal conditions the behavior and the low sensitivity indexes of the tuning factor have not changed.

3.2 Capacitive multiplier based on VDCC

Fig.3.1 shows the VDCC based capacitance multiplier. It consists of two VDCC and three grounded resistance and one grounded capacitance to be multiplied in order to obtain desired large capacitor value.

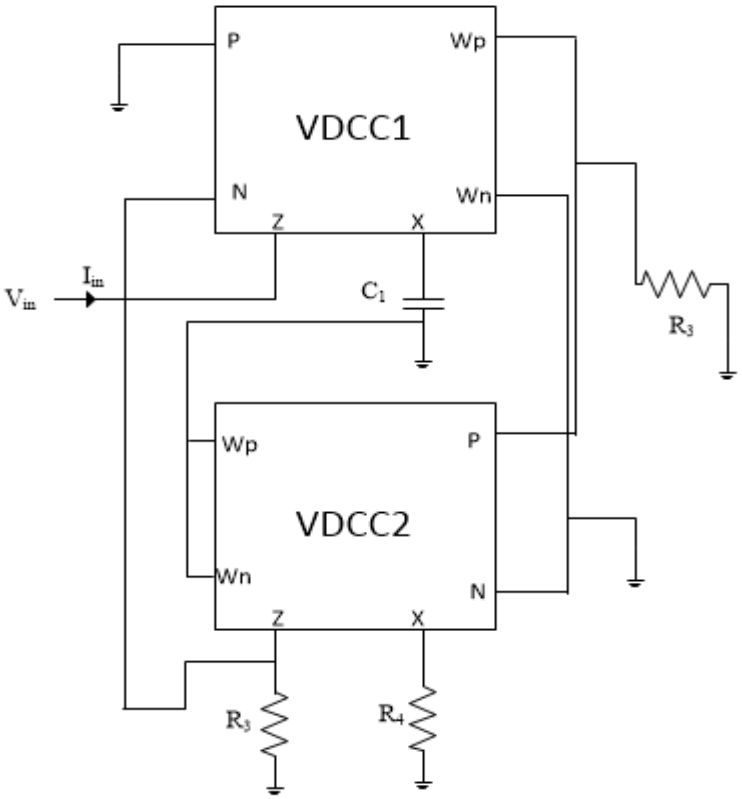


Fig. 3.1 VDCC based capacitance multiplier [16]

From the analysis of above circuit we get equivalent impedance of circuit as follows:

$$Z_{EQ} = \frac{1}{sC_1R_2R_3g_{m1}g_{m2}}$$

$$= \frac{1}{sC_1R_2R_3g_{m1}g_{m2}}$$

$$= \frac{1}{sC_1K} \quad \text{...(3.1)}$$

Where, $K = R_2R_3g_{m1}g_{m2}$ …(3.2)

Hence, From Eq. (3.1) we evident that the circuit acts as a capacitance multiplier for capacitance C_1 and the factor of multiplication is 'K'. The Eqation (3.2) represent that the multiplication factor value 'K' varies by R_2 and R_3 (grounded resistances). Electronic tunability of 'K' can be done through transconductance g_{m1} and g_{m2}. Thus, one can increase or decrease the value of grounded capacitance C1 by using the circuit through multiplication factor, which is an adjustable resistor / electronic.

3.3 Analysis of Non Ideal

The matrix for VDCC's non-ideal mathematical model can be defined as VDCC's current transfer errors (γ_{wp}, γ_{wn}), voltage transfer error (β) and transconductance gain error (α).

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{wp} \\ 0 & 0 & 0 & -\gamma_{wn} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

The matrix equations are for currents and voltages:

$$I_Z = \alpha g_m (V_P - V_N)$$

$$V_X = \beta V_Z$$

$$I_{WP} = \gamma_{wp} I_X$$

$$I_{WN} = -\gamma_{wn} I_X$$

To analyse multiplier circuit impedance as shown in Fig. 3.1 Using the non-ideal VDCC mathematical model we obtain:

$$Z_{EQ} = \frac{\beta_1 \beta_2}{sC_1 R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_2 \gamma_{wp1}}$$

$$= \frac{\beta_1 \beta_2}{sC_1 (R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_{2\_} \gamma_{wp1})}$$

$$= \frac{1}{sC_1 K_{NON\ IDEAL}} \quad \text{...(3.3)}$$

Where , $$K_{NON\ IDEAL} = \frac{R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_2 \gamma_{wp1}}{\beta_1 \beta_2} \quad \text{...(3.4)}$$

Where α_1,α_2 are error in transconductance, β_1, β_2 are errors in voltage transfer errors of two VDCC first and second and γ_{wp1} is error in current of first VDCC.

On consideration of VDCC's non-ideal model, from Eq. (3.3) and (3.4) it should be noted that the configuration still acts as a grounded impedance multiplier with the "$K_{NON\text{-}IDEAL}$" scaling factor, which is slightly lower than "K". It is therefore evident that in both ideal and non-ideal condition, circuit behaviour remains the same, which is a very important advantage of the circuit presented.

3.4 Application

A low pass filter is built using a grounded capacity multiplier VDCC baesd as a grounded capacitance. The low pass filter circuit of the first order RC built from passive elements is shown in Fig. 3.2 and its use of a grounded capacitance circuit based on VDCC is shown in figure 3.3

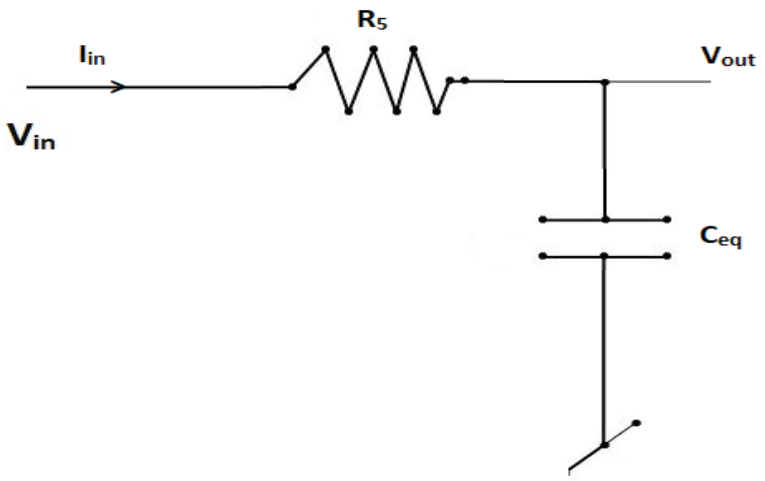


Fig. 3.2 first order Low Pass filter with passive component

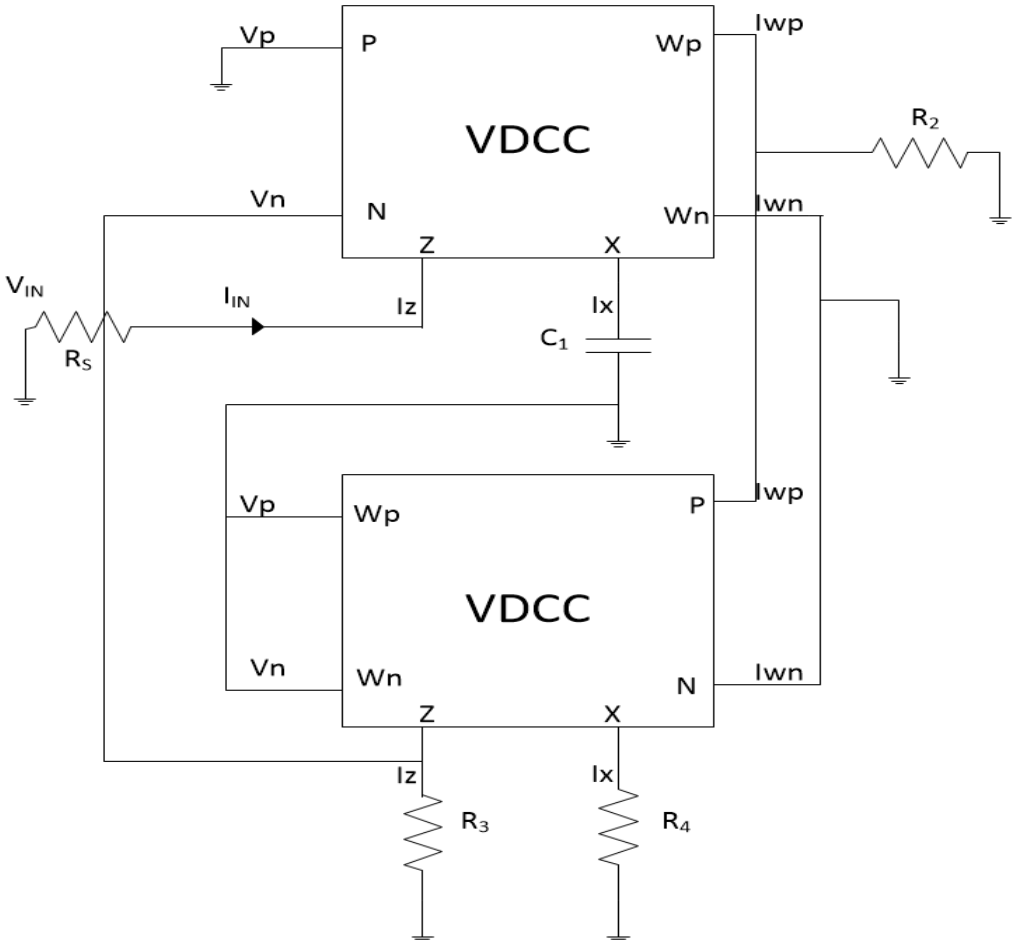


Fig. 3.3 Implementation of filter using VDCC based capacitance multiplier circuit [16]

3.5 Simulation and Results

SPICE simulations must be conducted using CMOS VDCC [5] to verify the presented circuit and low pass filter circuit made with the aid of the presented circuit. For configuration value of passive component as shown in Figure 3.1 are as C_1=0.1nF and $R_2 = R_3 = R_4$=1 K together with supply voltage of ±0.9VDC. The results of the simulations for the amplitude and phase response are shown in Figure 3.5 and 3.6 respectively. Now to study the effect of scaling factor resistance control is shown in Fig.3.9 and it indicates the input impedance for different values of resistance R3. Similarly, Fig.3.10 shows the effect of electronic tuning factor change with bias currents Ib1 of both VDCC. The response of filter circuit can be seen in Fig.3.12 and take the value of passive elements during simulation as R_2=R_3=R_4=1K, Rs= 10k and C_1=0.1nF.

TABLE 3.1

Transistors	**W/L(μm)**
M_1-M_4	**3.6/1.8**
M_5-M_6	**7.2/1.8**
M_7-M_8	**2.4/1.8**
M_9-M_{10}	**3.06/0.72**
M_{11}-M_{12}	**9/0.72**
M_{13}-M_{17}	**14.4/0.72**
M_{18}-M_{22}	**0.72/0.72**

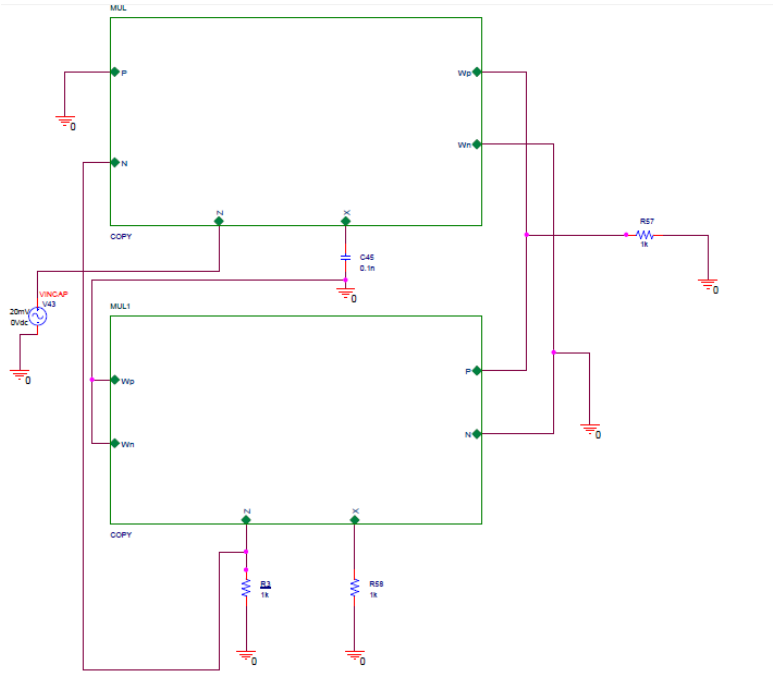


Fig. 3.4 Schematic of capacitance multiplier [16]

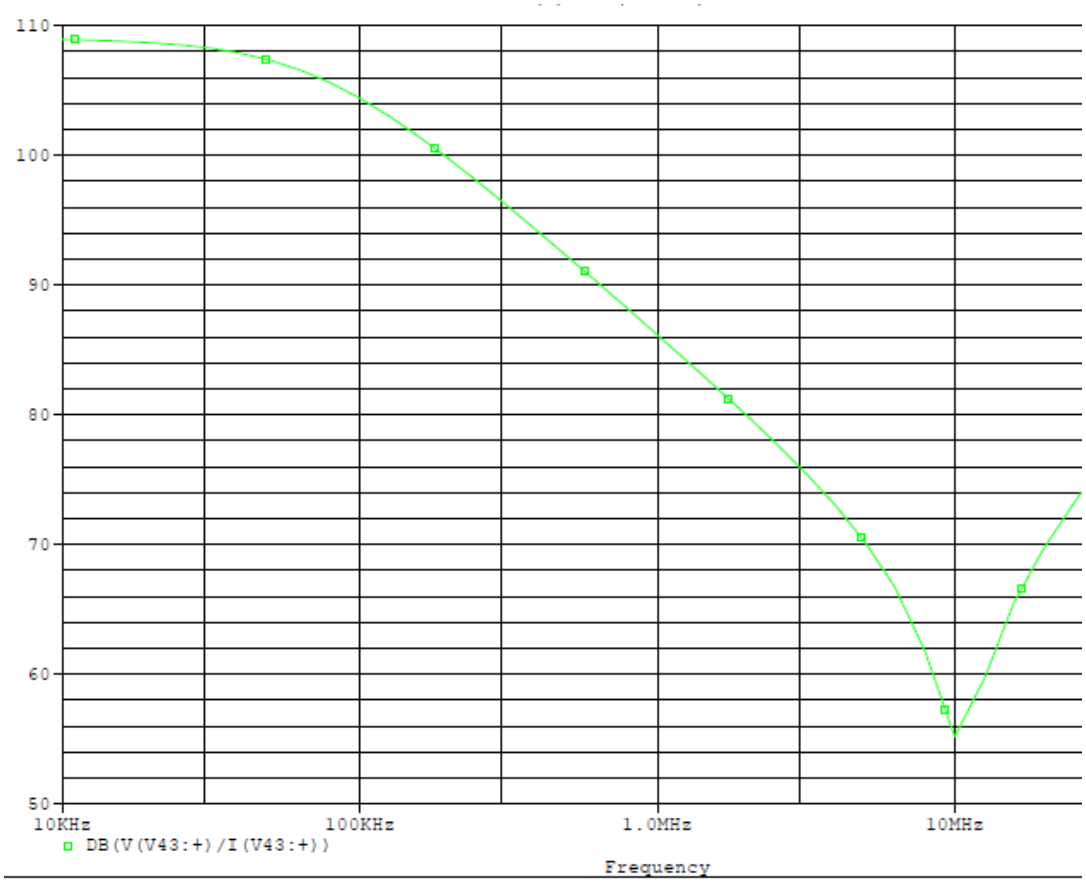


Fig 3.5 Capacitive multiplier circuit magnitude response

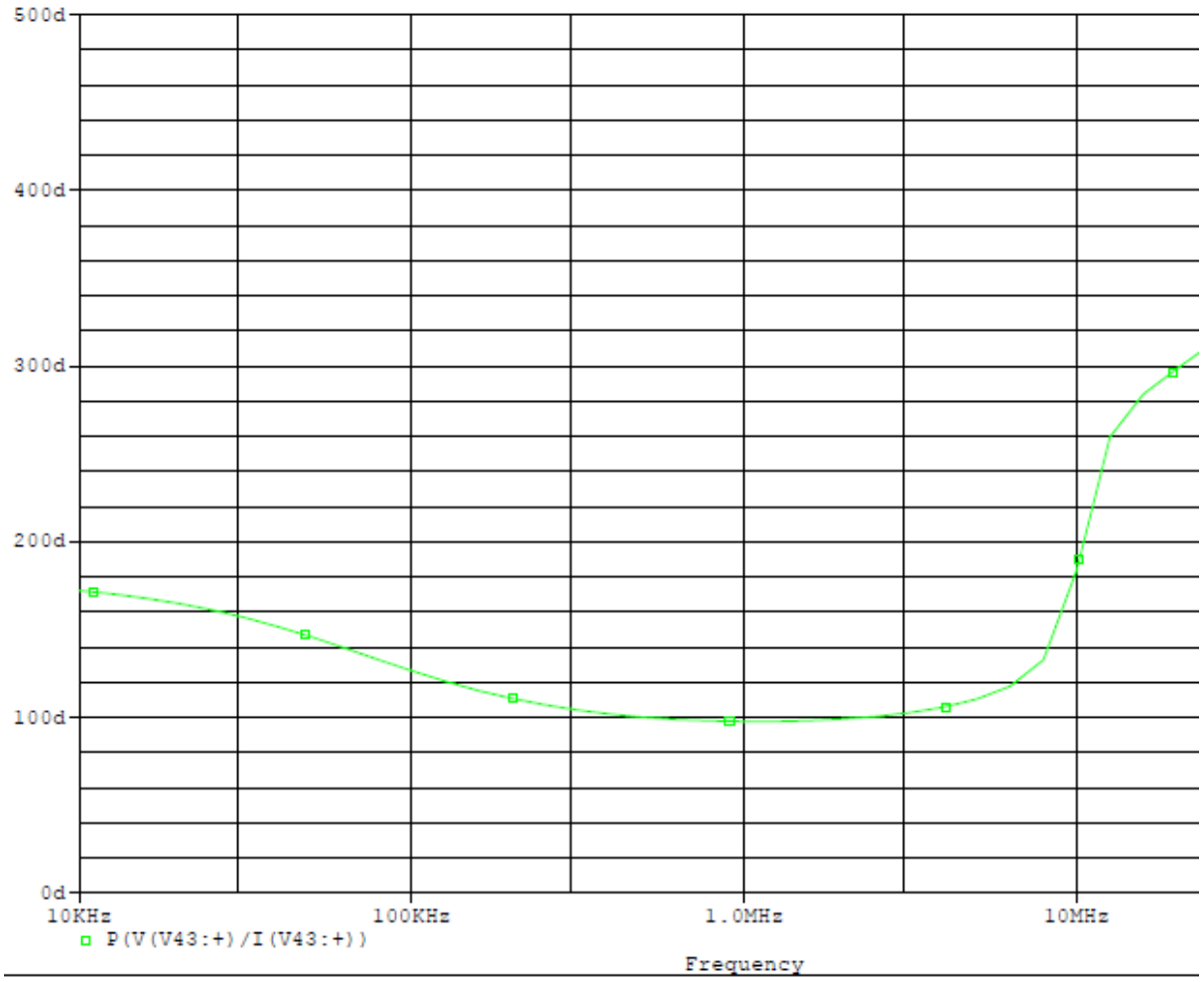


Fig 3.6 Capacitive multiplier circuit phase response

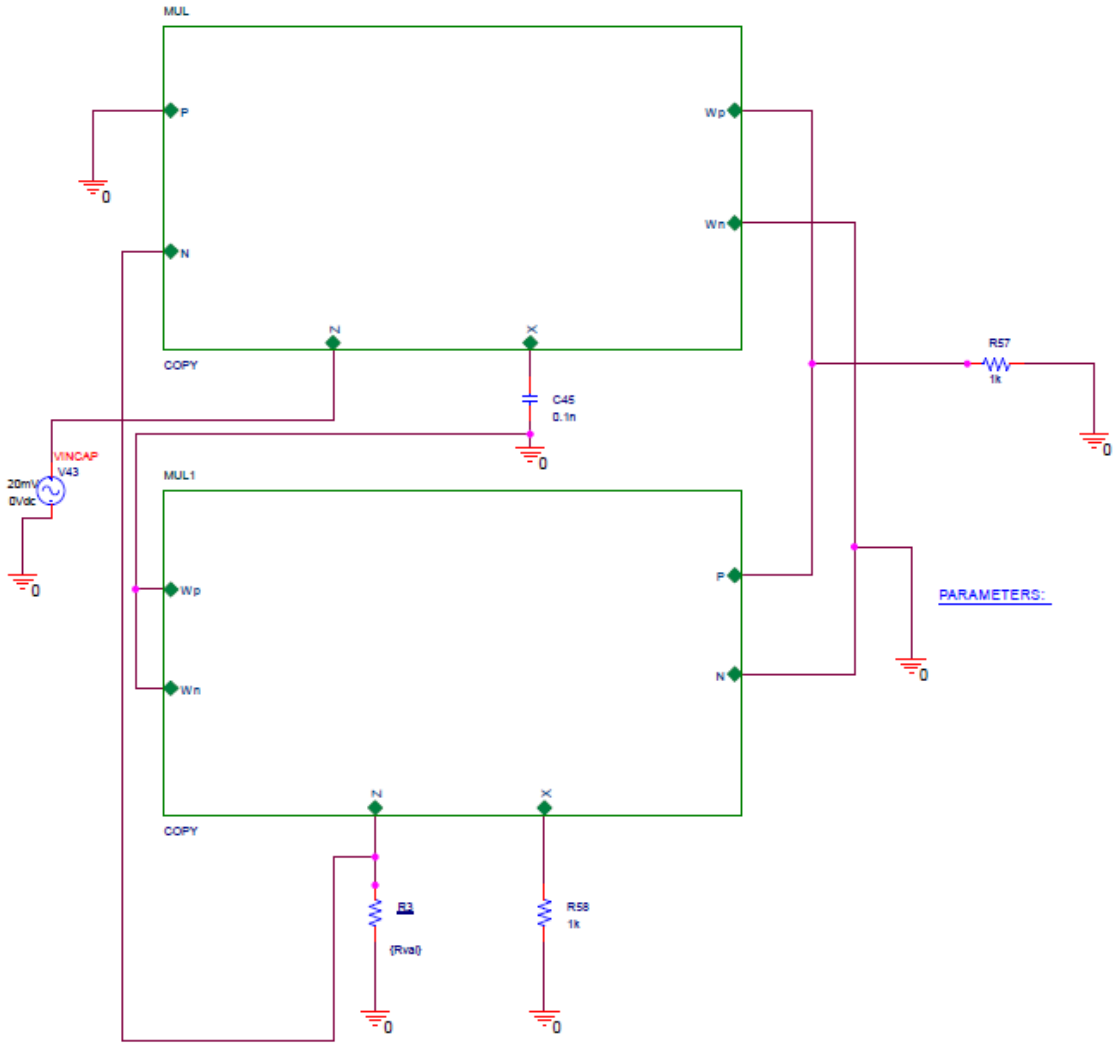


Fig. 3.7 Schematic of capacitance multiplier with R_3 as variable [16]

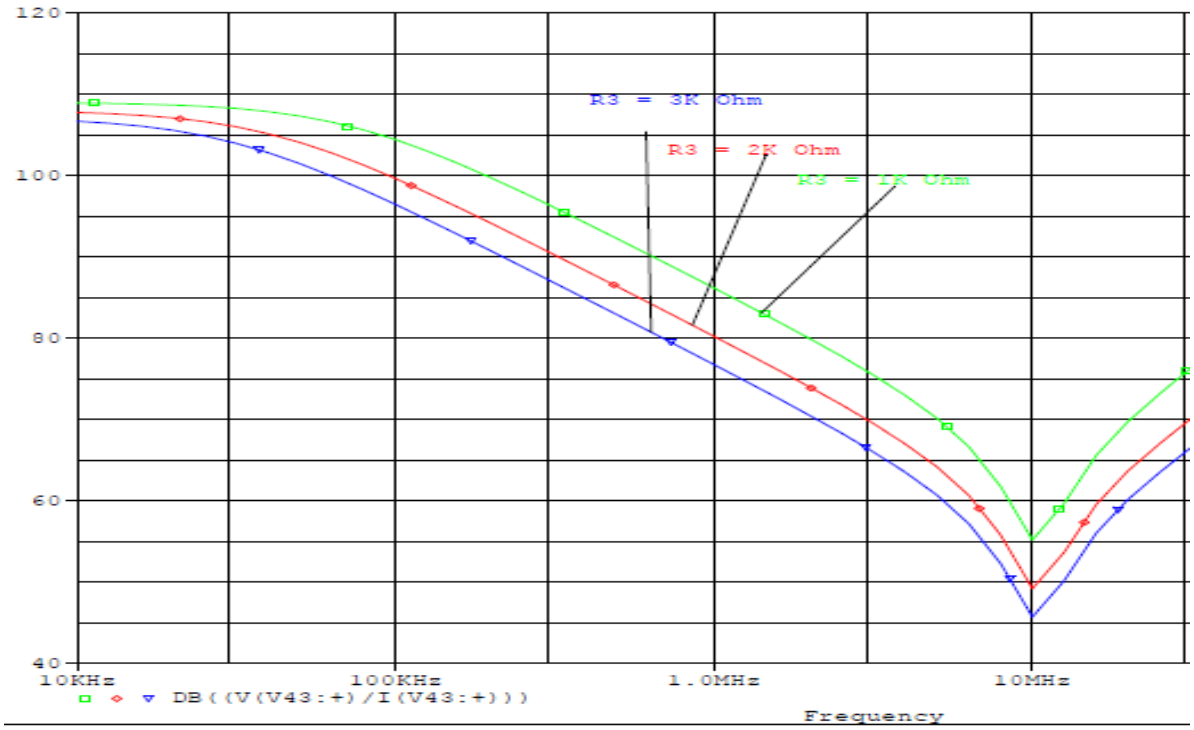


Fig. 3.8 Magnitude response of Capacitance multiplier circuit by varying grounded resistance R_3

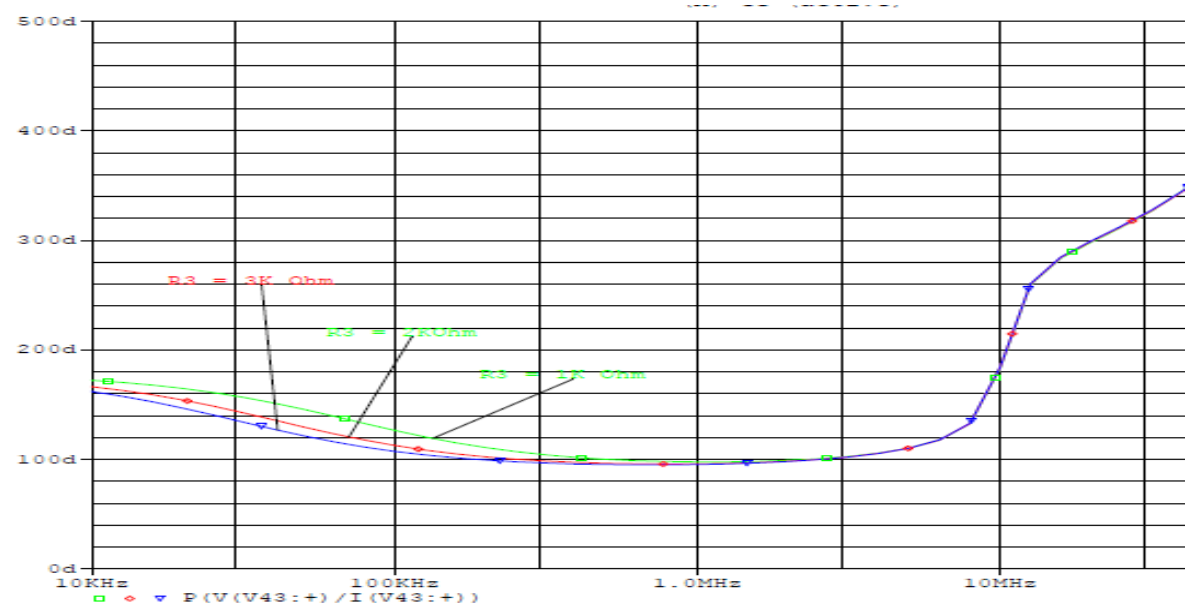


Fig.3.9 capacitance multiplier phase response with variable resistance R_3

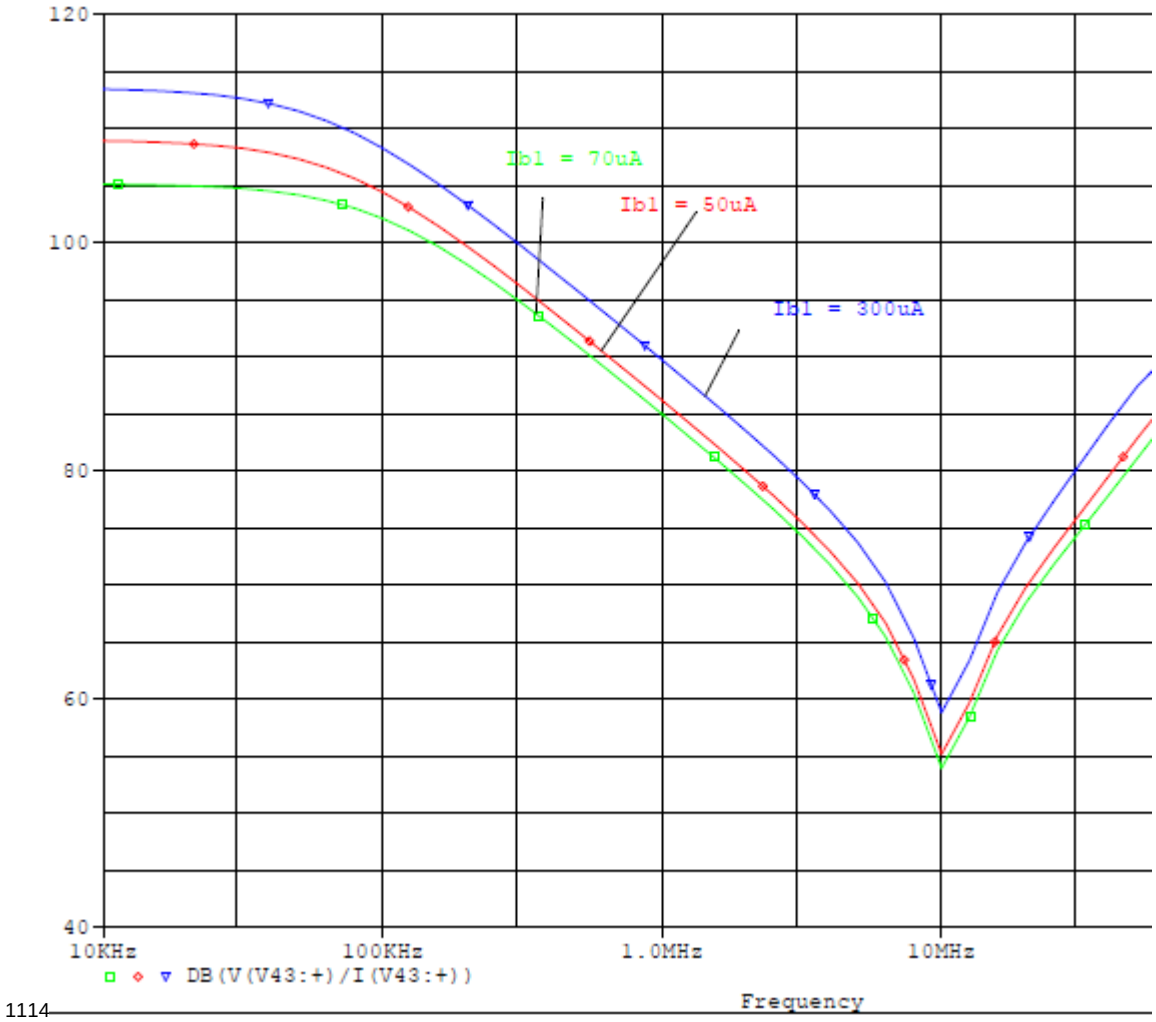
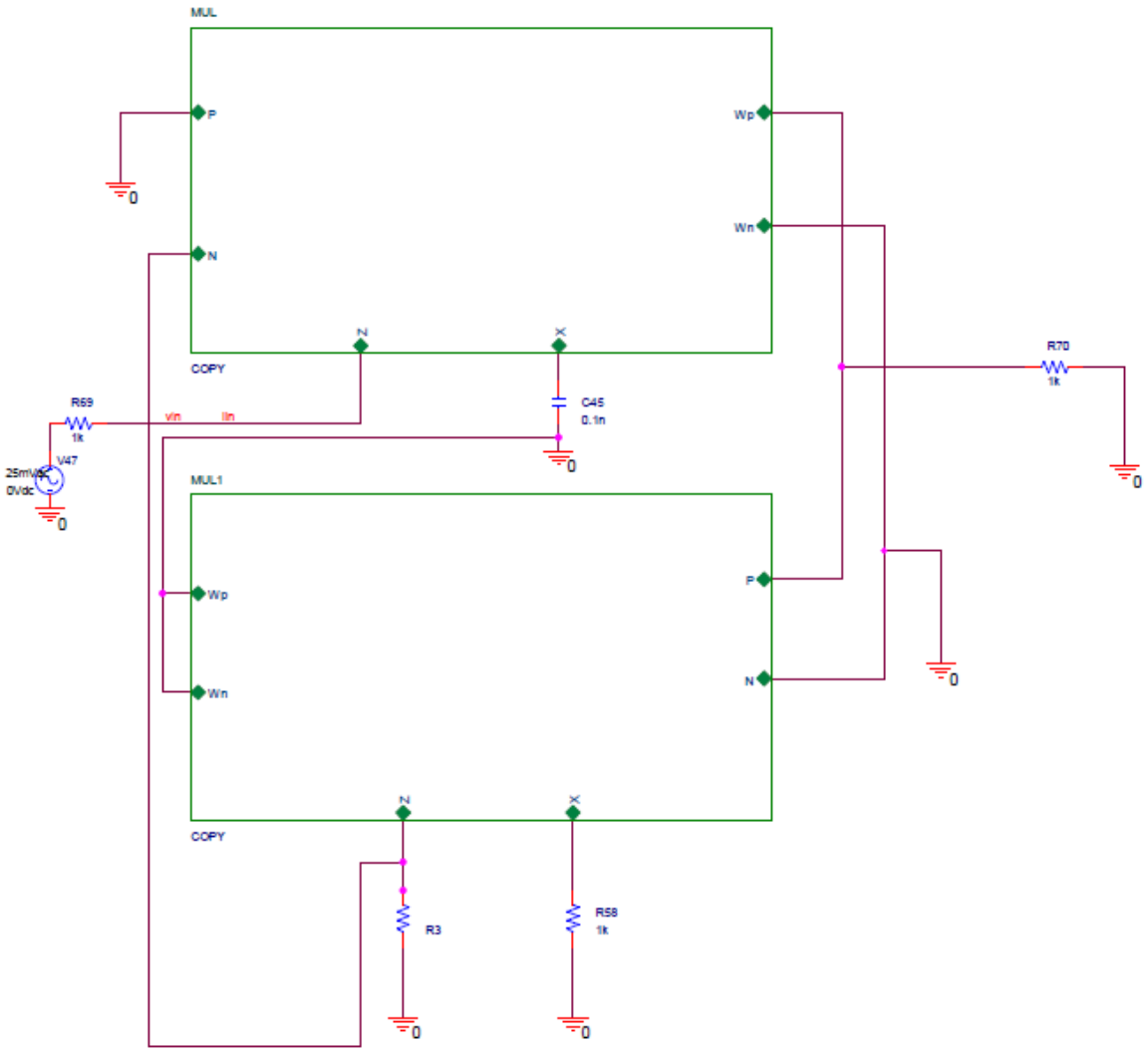
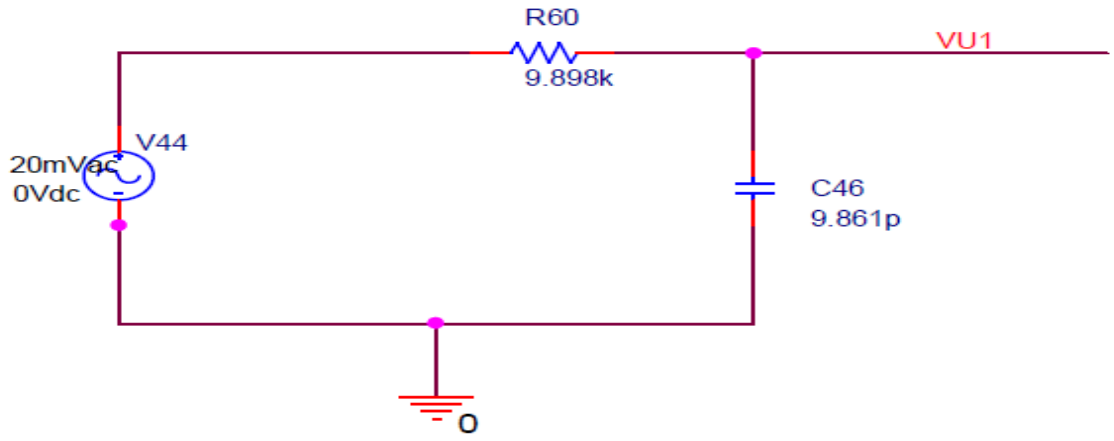


Fig. 3.10 Impedance response of capacitance multiplication on varying bias currents I_{b1} of both VDCCs



(a)



(b)

Fig.3.11 Implementation of filter on schematic (a) with two VDCC
(b) with passive component

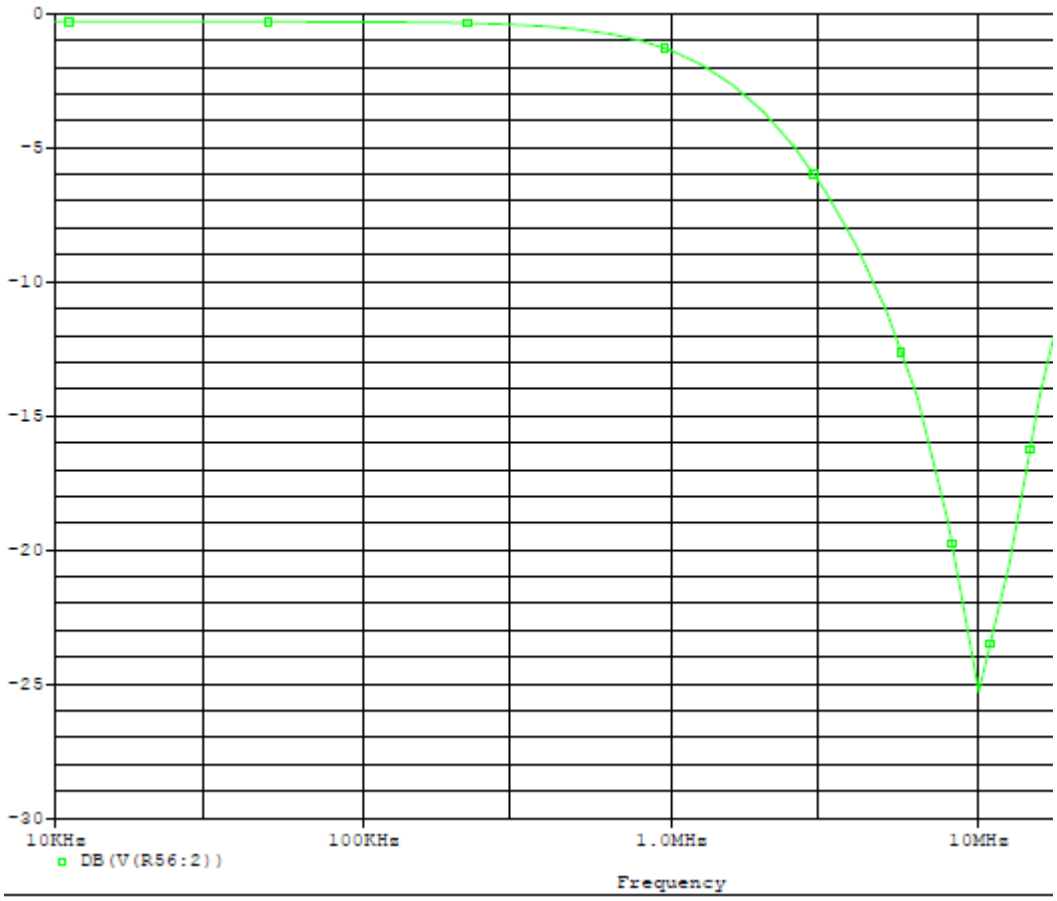


Fig.3.12. Response of Low Pass filter design.

CHAPTER 4

Grounded Impedance Scaling Configuration with VDCC

4.1 Introduction

From the point of view of efficient realization chip area, it is not suitable for chip large value capacitors, inductors, and resistances, as large impedances consume more area on the chip. For such applications, impedance scaling circuits or multipliers that employ active elements become useful. In literature, several researchers [1-14] presented significant no. of impedance simulation circuits. Few of those simulation impedance circuits are capable of multiplying grounded impedance. But there are one or more following disadvantages to these circuits, which are:

1. Floating passive elements are employed in circuit configuration
2. Non-electronic scaling.
3. Need of matched active/passive elements.

Thus, impedance scaling circuit based on VDCC with electronic and resistive scaling. This circuit configuration consists of only two VDCCs and three grounded resistors. Under ideal and non-ideal conditions, the working of this circuit remains the same and is also free from the constraints that match active and passive elements.

4.2 VDCC Based Grounded IMPEDANCE SCALING CONFIGURATION

The impedance multiplier circuit configuration consisting of two VDCCs together with three grounded resistances is shown in Fig 4.1.

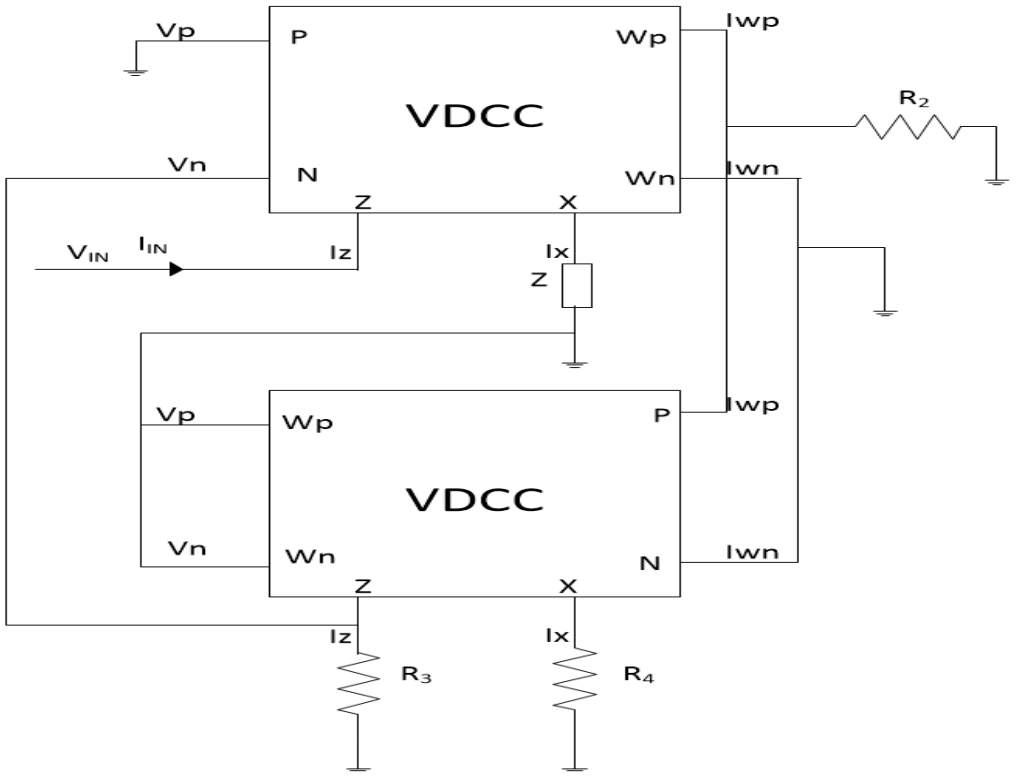


Fig.4.1 Configuration of Grounded Impedance scaler [17]

From the analysis of configuration of Fig 4.1, the impedance is obtained as :

$$Z_{EQ} = \frac{V_{in}}{I_{in}} = \left(\frac{1}{R_2 R_3 g_{m1} g_{m2}}\right) Z$$

$$= K*Z \qquad \ldots(4.1)$$

Where $$K = \frac{1}{R_2 R_3 g_{m1} g_{m2}} \qquad \ldots(4.2)$$

Where g_{m1} and g_{m2} are transconductance gains of VDCC-1 and VDCC-2. Now, from equation 4.1 it is evident that presented circuit configuration can scale up or scale down the impedance of "Z" by a multiplication factor 'K'. From equation (4.2), it is observed that the value of 'K' can be varied by varying the value of $R_2/R_3/g_{m1}/g_{m2}$. Hence, both electronic and resistive scaling is possible. 'Z' is either a single passive element or a combination of passive elements.

On considering non ideal current and voltage transfer constants among different terminal of VDCC, characteristics equations of VDCC have to be modified. On considering the voltage transfer error(β), current transfer errors (γ_{wp}, γ_{wn}) and transconductance gain error (α) of VDCC, the non – ideal mathematical model of VDCC can be define as:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{wp} \\ 0 & 0 & 0 & -\gamma_{wn} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

The matrix equations are for currents and voltages:

$$I_Z = \alpha g_m (V_P - V_N)$$

$$V_X = \beta V_Z$$

$$I_{WP} = \gamma_{wp} I_X$$

$$I_{WN} = -\gamma_{wn} I_X$$

Analyzing the multiplier circuit impedance shown in Fig. 4.1 We obtain the non-ideal VDCC mathematical model as follows:

$$Z_{EQ} = \frac{\beta_1 \beta_2}{R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_2 \gamma_{wp1}}$$

$$= \frac{\beta_1 \beta_2}{(R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_{2\_} \gamma_{wp1})}$$

$$= \frac{1}{sC_1 K_{NON\ IDEAL}} \quad \text{...(4.3)}$$

Where, $K_{NON\ IDEAL} = \frac{\beta_1 \beta_2}{(R_2 R_3 g_{m1} g_{m2} \alpha_1 \alpha_{2\_} \gamma_{wp1})}$ ...(4.4)

Where, α_1, α_2 are error in transconductance, β_1, β_2 are error in voltage transfer for two VDCC and γ_{wp1} is the error in current transfer of VDCC-1.

From Eq. it is noted (4.3) and (4.4) that the configuration still acts as a grounded impedance multiplier with a "$K_{NON\text{-}IDEAL}$" scaling factor that is slightly lower than "K." It is also clear that in both ideal and non-ideal situation the circuit behaviour remains the same, which is a very significant benefit of the presented circuit.

4.4 Application:

Active filter architecture is used to check the functioning of impedance scaling circuit configuration. A High Pass filter is constructed using a grounded resistor based on the VDCC configuration. The conventional filtering circuit for the RC High Pass is given in Fig.4.4.

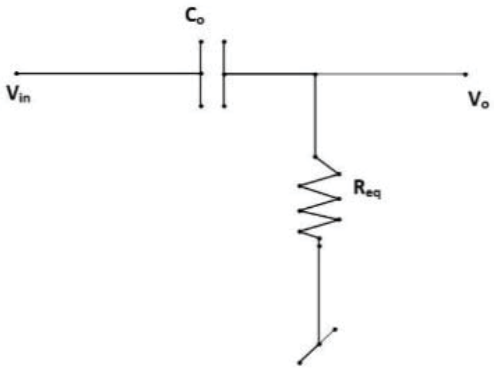


Fig 4.2 Conventional High Pass filter [17]

Fig.4.2 illustrates the active equivalent of the filtering configuration by replacing passive resistance with the impedance scaling circuit based on VDCC working in grounded resistance mode.

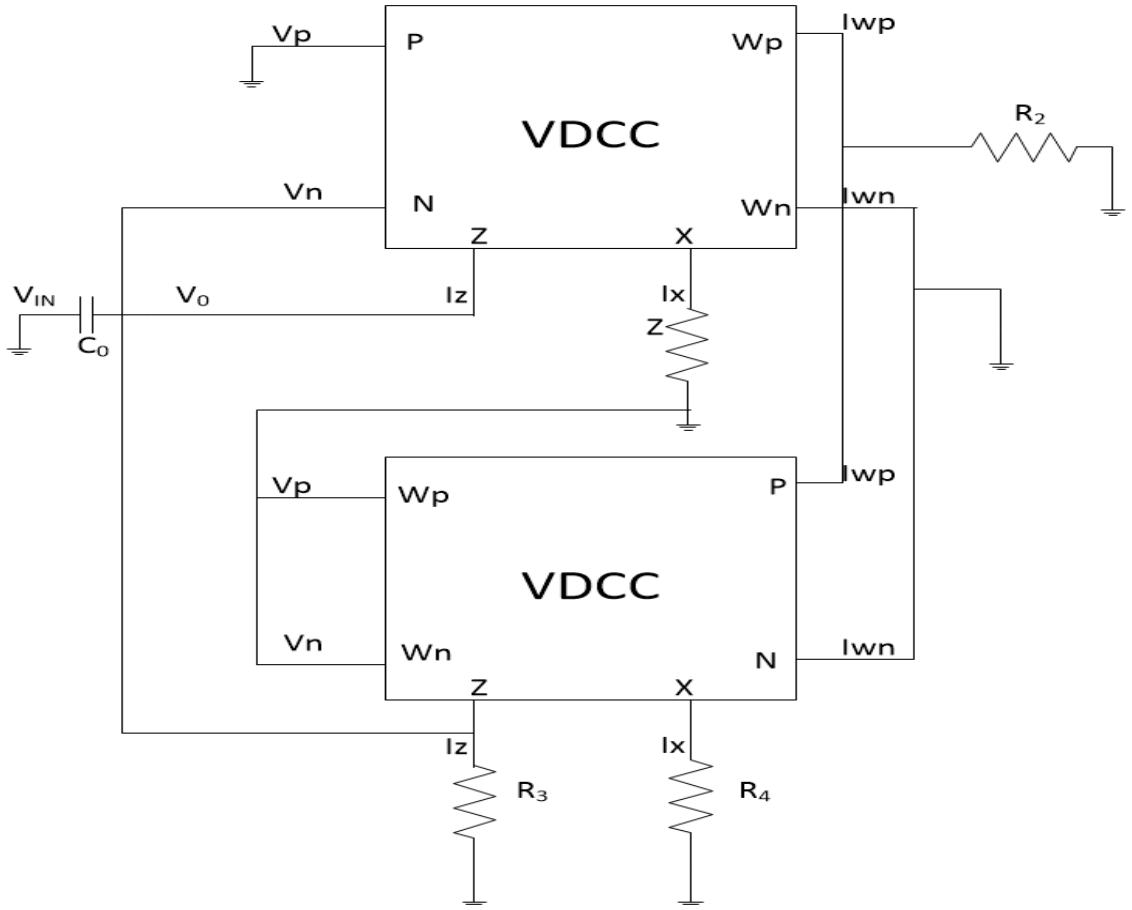


Fig.4.3. High Pass filter using VDCC based grounded impedance scaling circuit [17]

4.5 Simulation and Results

To verify the functioning of the established circuit configuration as a scaling circuit of grounded resistance, assume Z_1 as a value resistance of 1K. The scaling response of this grounded resistance through R_2 is shown in Fig.4.5 showing the input impedances with varying R_2 and the value of R_3 is 1 K while now assume the scaling of Z as Co=0.01nF through R_2 is shown in Fig. 4.7. Suppose $Z = sL_o$ is shown in Fig 4.8 to scale Z by R_2.

Now, to reflect the electronic scaling of impedance by bias currents of using VDCC, the simulations for different values of biasing currents have to be carried out. To show the electronic scaling in place of Z_1 we attach 1KΩ resistor and then simulations have been done for $I_{b1}$of both VDCCs equal to 10μA, 30μA, 50μA keep I_{b2} remain same as 10μA. Fig.4.11 shows the response of the frequency plots.

In order to study the electronic scaling of the grounded capacitor, replace the Z1 with grounded capacitance C1 of the value 0.01mF, simulations have to be made again for different values of biased currents (I_{b1} of both VDCCs equal to 10μA, 30μA, 50μA keep I_{b2} the same as 10μA remain). The results of the simulation are set out in Fig.4.13. Likewise, substitute the Z_1 with grounded inductor of value 0.1mH for electronic scaling of grounded inductance, and the answer is shown in Fig.4.15.

The High Pass filter is also realized in PSPICE using the VDCC-based impedance scaling circuit configuration (given in fig 5.3). The passive element values of passive elements are chosen as $R_1 = R_3$=1 K, C_2=0.01nF. Figure 4.17 shows the frequency response of this filter for different R_2 values.

Table 4.1

Transistors	W/L(μm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

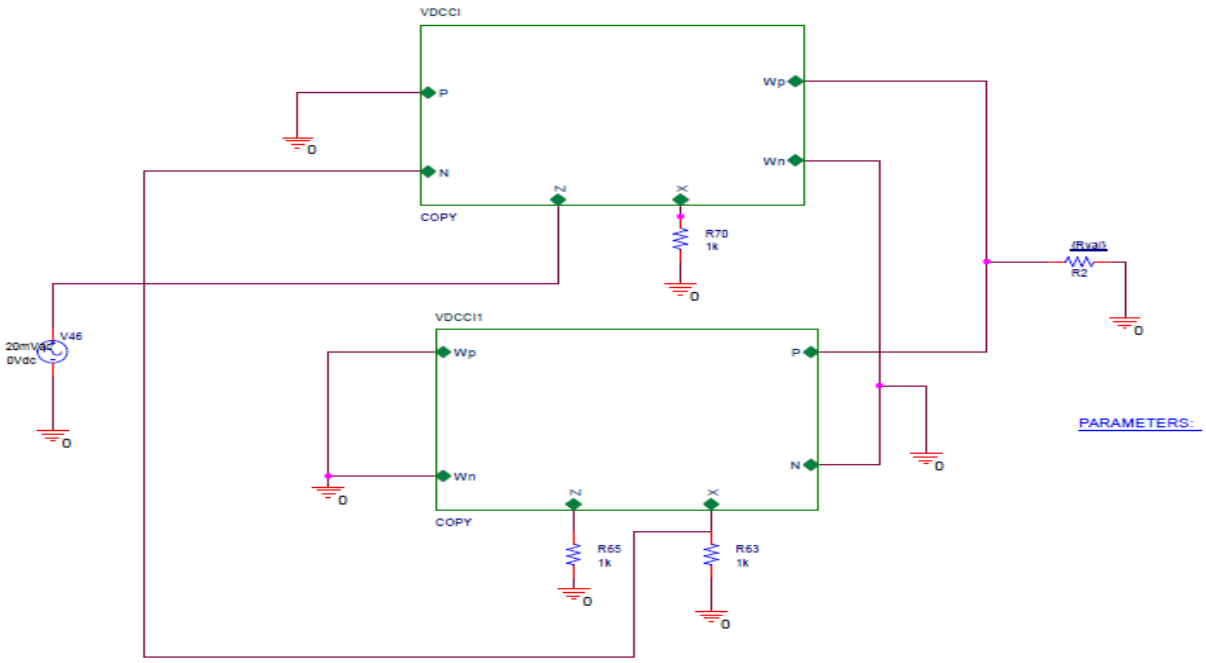


Fig 4.4 Schematic of scaling grounded impedance configuration for $Z=R_1$ and vary resistance R_2

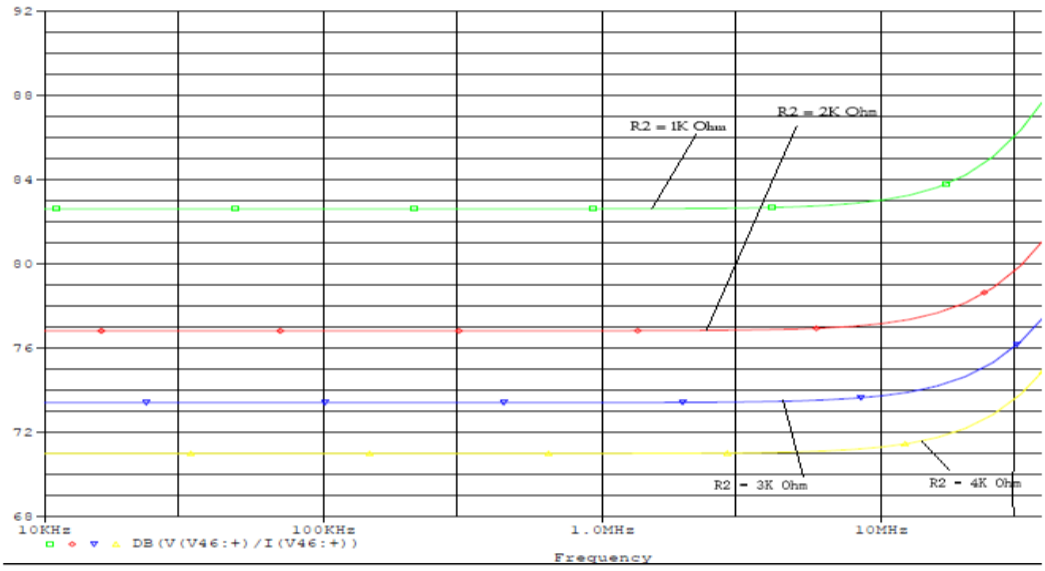


Fig.4.5. Response of resistive scaling of $Z=R_1$ through resistance R_2.

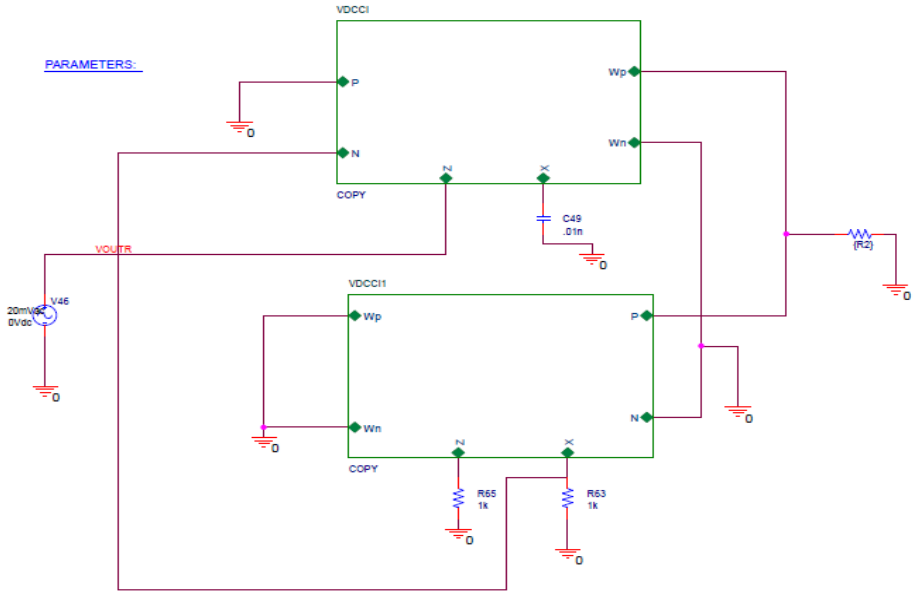


Fig 4.6 Schematic of scaling grounded impedance configuration for $Z=1/sC_1$ by vary resistance R_2

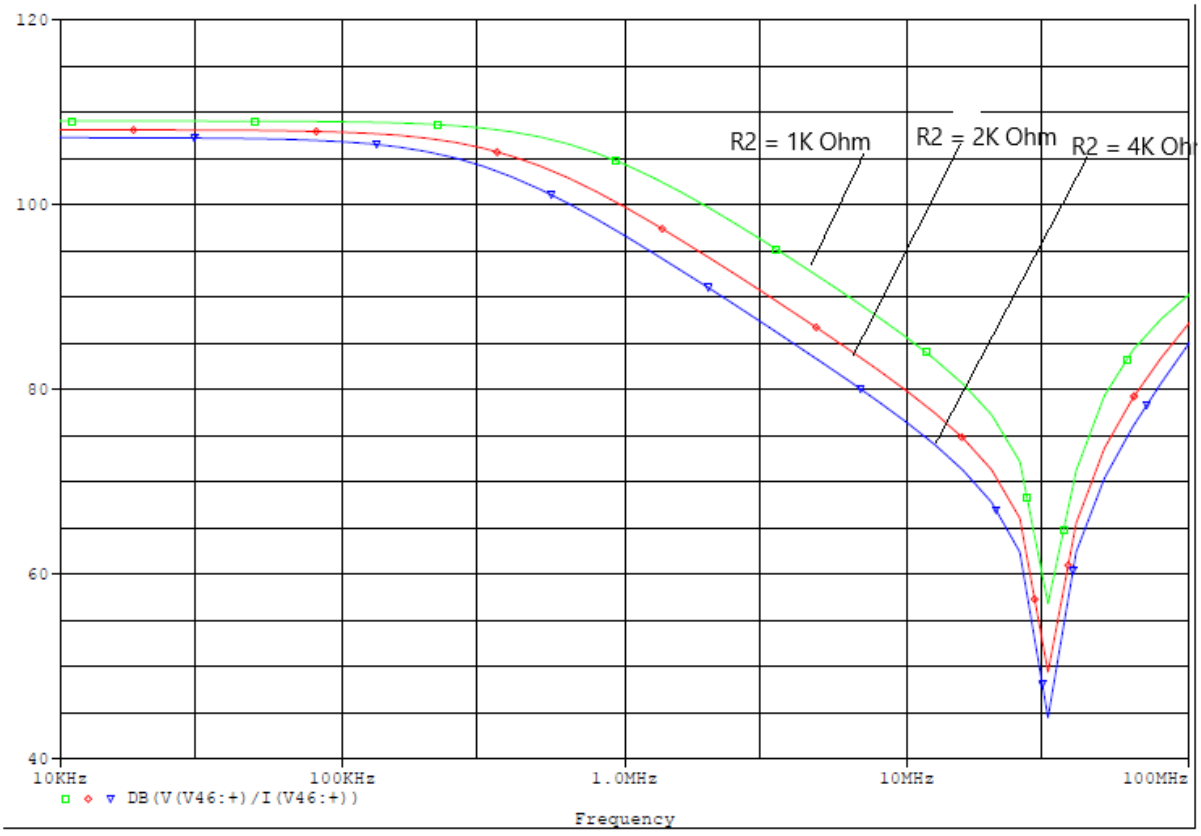


Fig.4.7. Response of resistive scaling for Z=1/sC1 through resistance R2.

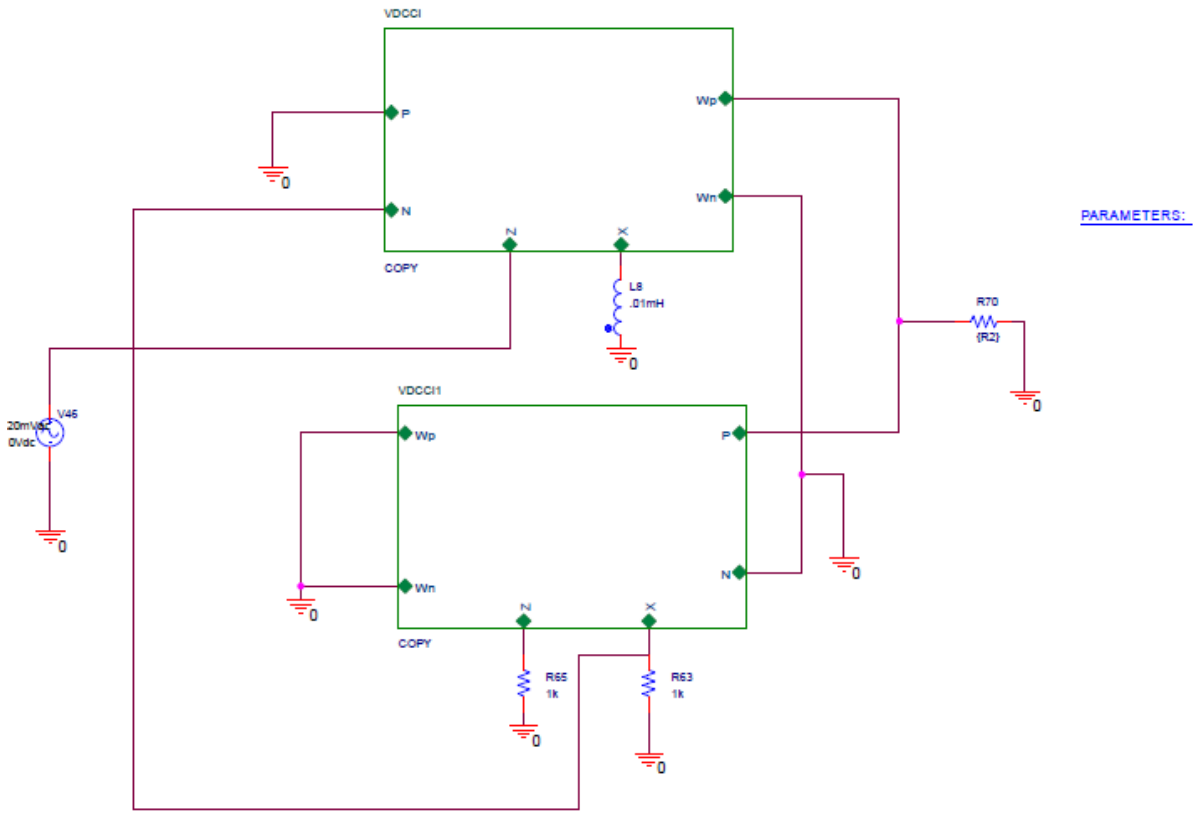


Fig 4.8: Schematic of scaling grounded impedance configuration for Z= sL_1 by varying resistance R_2

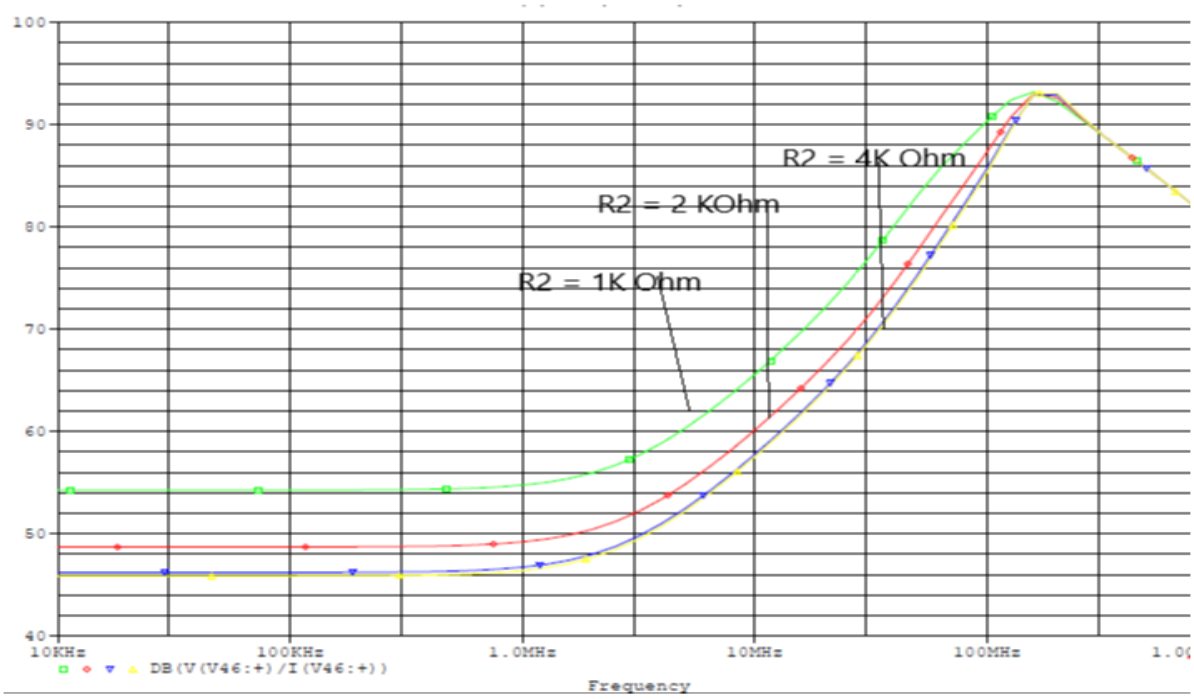


Fig.4.9. Response of resistive scaling for Z=sL_1 through resistance R_2.

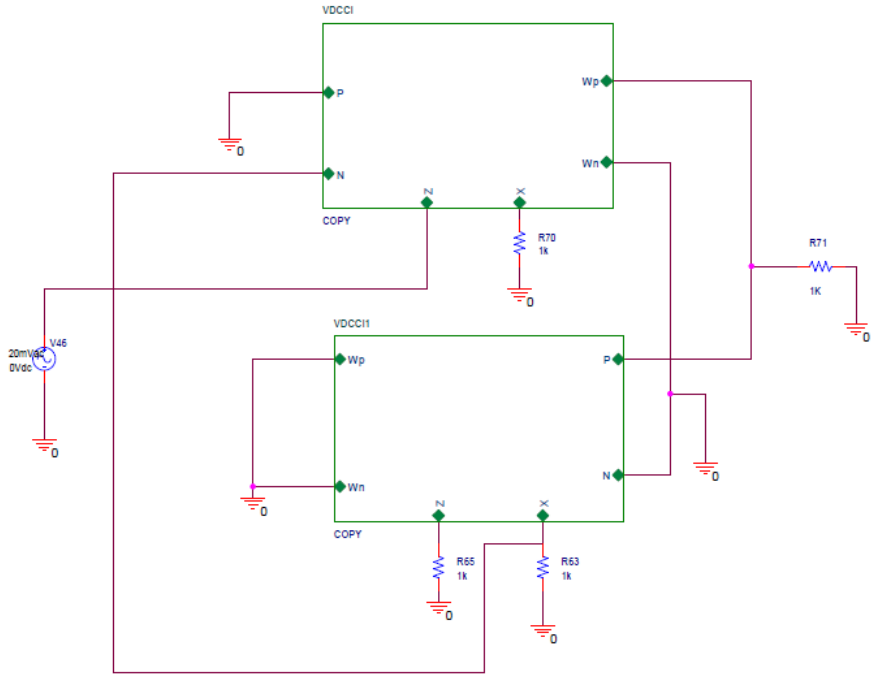


Fig 4.10: Schematic of scaling grounded impedance configuration for $Z=R_1$

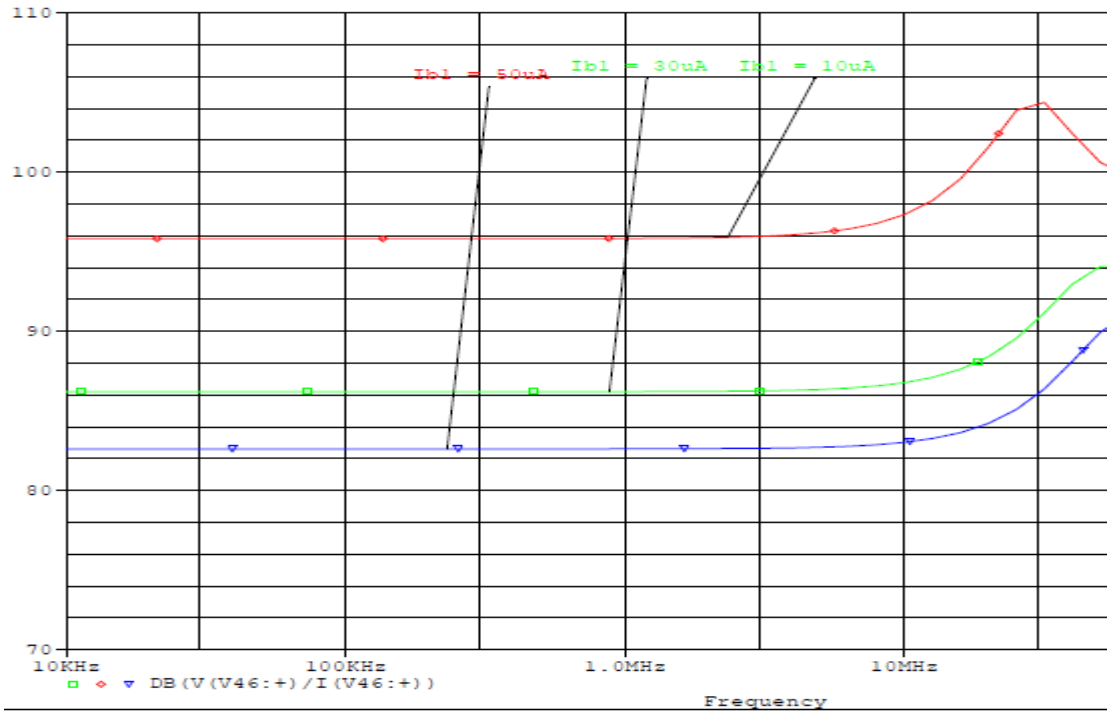


Fig.4.11.Response of resistive scaling of $Z=R_1$ for different values of I_{b1}(bias currents) of Both VDCC.

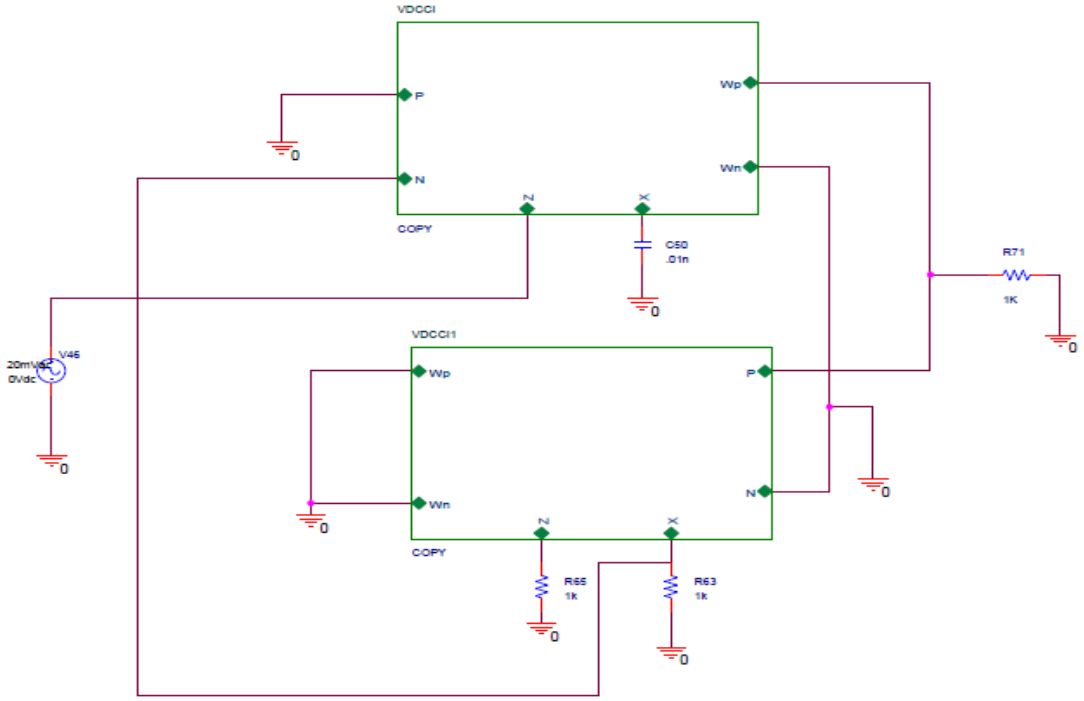


Fig 4.12 Schematic of scaling grounded impedance configuration for $Z=1/sC_1$

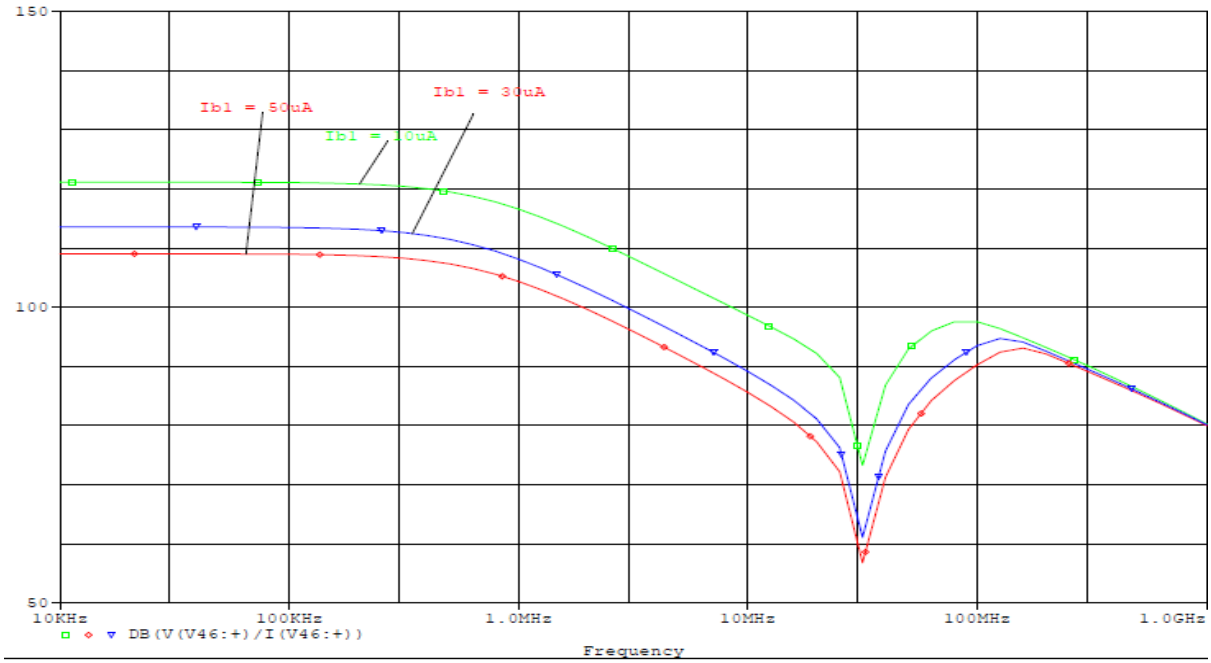


Fig.4.13. Response of impedance scaling of $Z=1/sC_1$ for different bias currents (Ib1) values of both VDCC

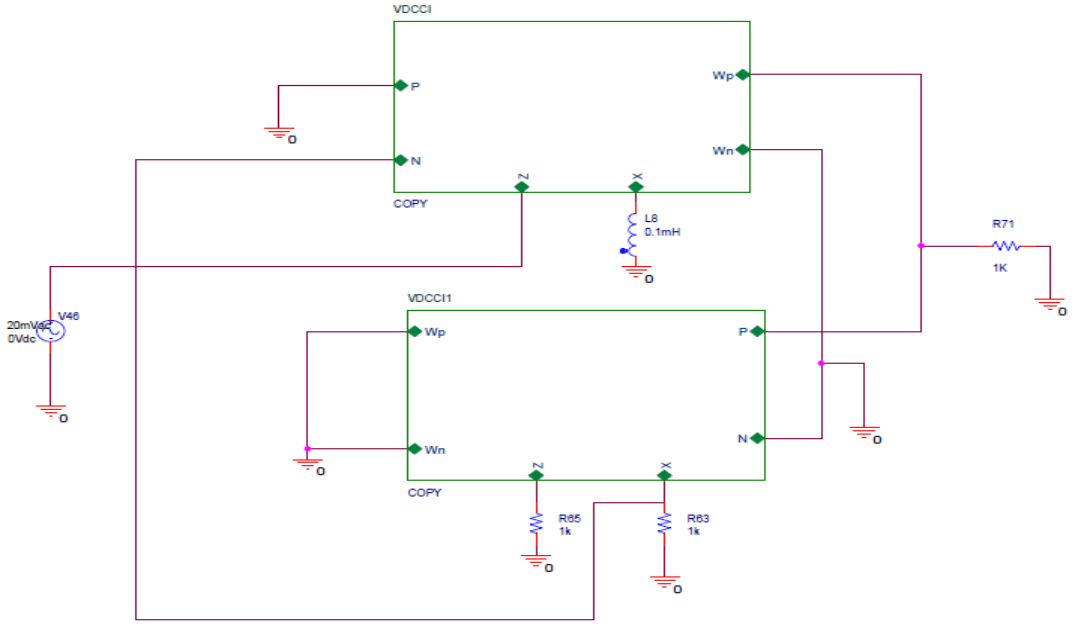


Fig 4.14 Schematic of grounded impedance scaling configuration for $Z=sL_1$

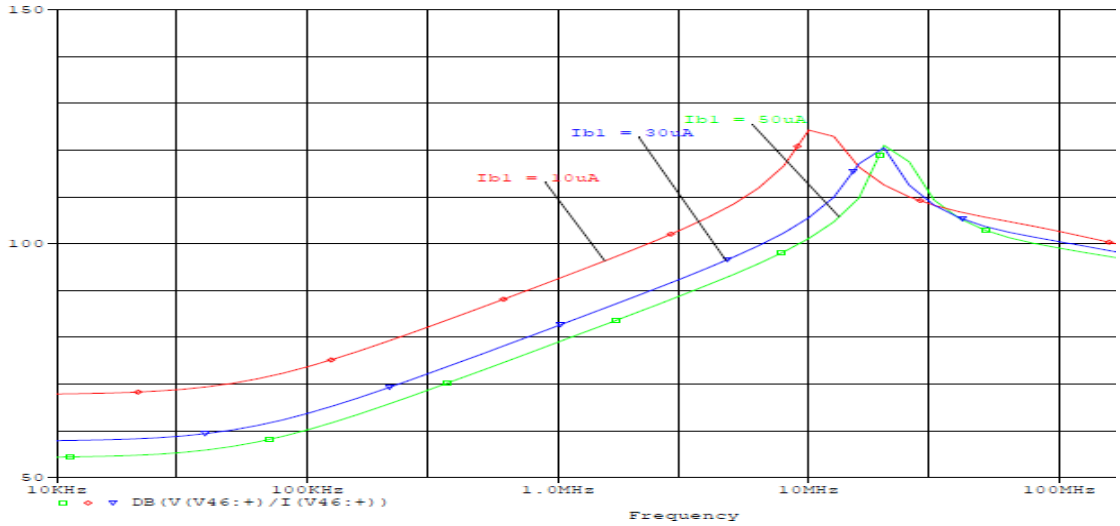


Fig.4.15. Response of impedance scaling of $Z = sL_1$ through differen values of t bias currents (I_{b1}) of VDCC -1 and VDCC-2

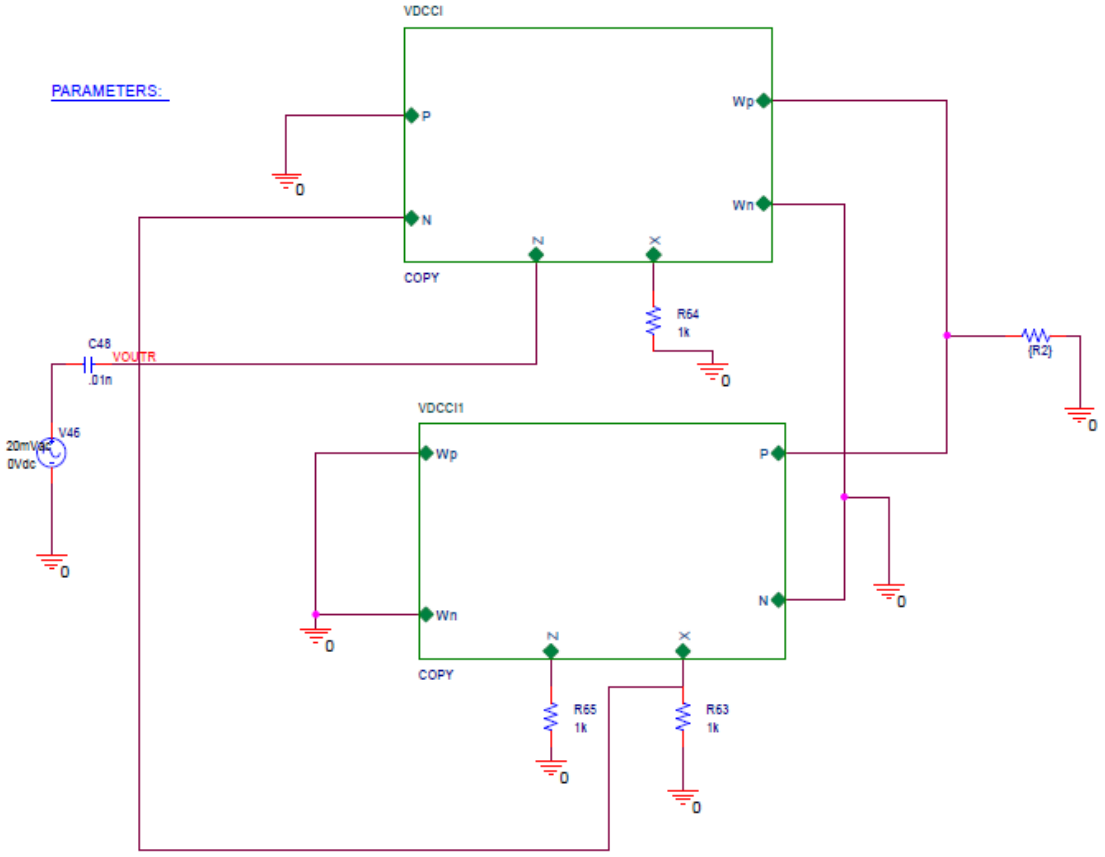


Fig 4.16 Schematic of active implementation of RC High pass filter circuit

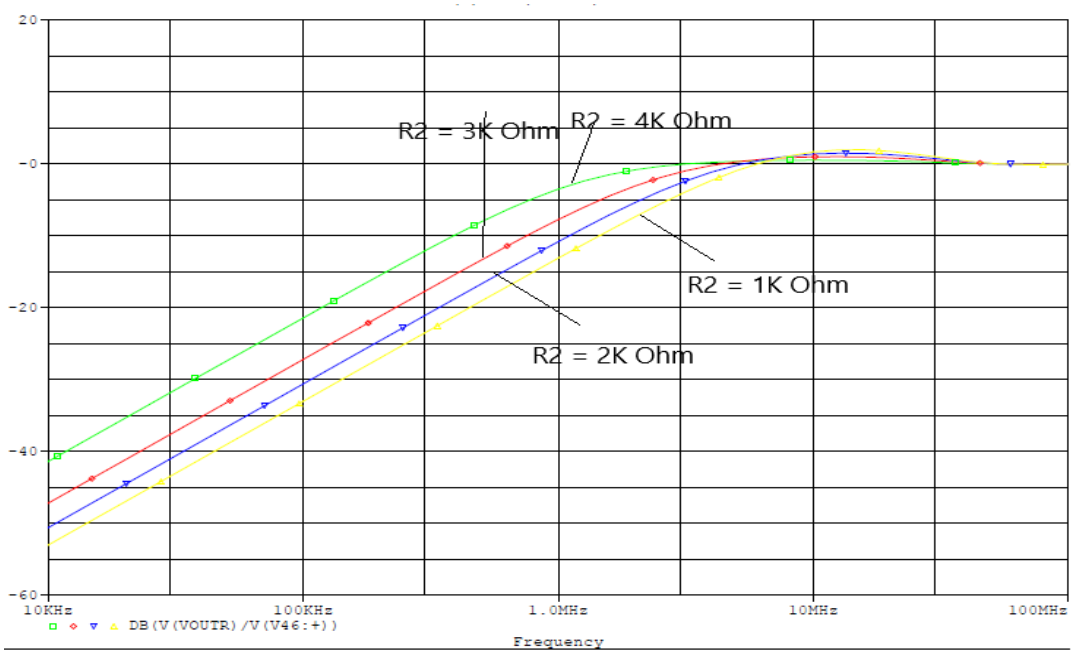


Fig.4.17 High Pass-Filter response

CHAPTER 5

Universal Biquadratic Filter in Current-mode

5.1 Introduction

Analog filters are widely used in many electronics system as in three-way loudspeaker as a cross-over network and phase locked loop (PLL) FM stereo demodulator [19]. Mainly, the universal circuit is required as they reduce the chip area, cost, consumption of power and they are suitable to integrate on chip. Hence the many no. of universal circuits are introduced [20]-[29]. Some of them function as mode of current [19]-[24] and others as voltage [20]-[23], current mode has advantage over the voltage mode like greater linearity, operate at higher frequency, wider dynamic range, circuitry is simple, power dissipation is less. One input and three-output structure of Low Pass, Band Pass and High pass types are presented [26]–[27]. But has disadvantage as some output current flow by the capacitor and driving the load is also very difficult. In [27]–[28], universal filters having one output and three inputs have been presented. All these filter generate five standard filtering functions but they are complicated as they are using two active building blocks along with it passive component matching condition is also required for filtering function achieved successfully.

The presented circuit using one VDCC, grounded one resistor and grounded two capacitor overcome all the above disadvantages. It realized all the five standard filtering function using same circuit structure with some changes in position of input current. This circuit also set orthogonal control over Q and ω_0.

5.2 VDCC based current mode universal filter

The structure presented here is shown in fig. 5.1 Universal biquadratic filter with three input terminals and one terminal output in current mode.

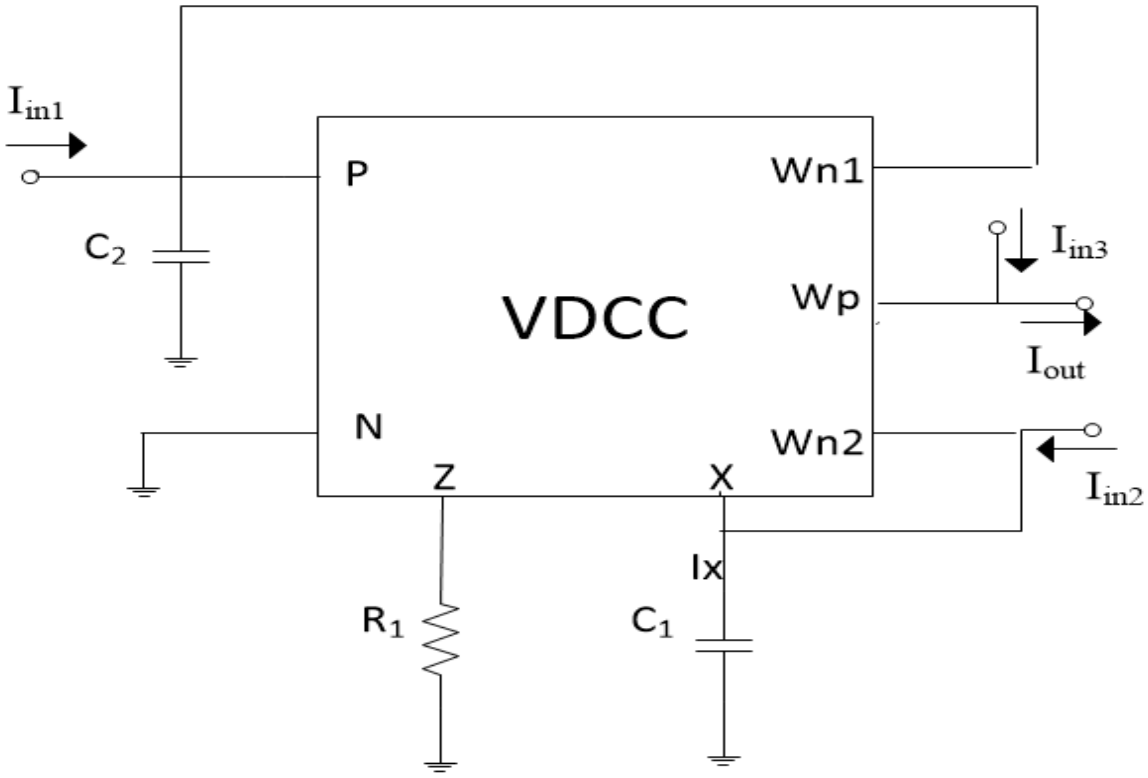


Fig 5.1 Circuit of biquadratic filter in current mode [18]

From analysis of above circuit we obtained following current transfer:

$$I_{OUT} = \frac{D(S)I_{in3} + \left(S/R_1C_1\right)I_{in2} + \left(g_m/R_1C_1C_2\right)I_{in1}}{D(S)} \qquad \ldots 5.1$$

where, $D(S) = S^2 + S/(R_1C_1) + g_m/(R_1C_1C_2)$

From equation 5.1 it is clear that presented circuit provide the variation in current transfer function by attaching the input current at different terminals. Standard five filter can be obtained as :

- Low Pass filter – $I_{in1} = I_{in}$ and $I_{in2} = I_{in3} = 0$
- Band Pass filter – $I_{in2} = I_{in}$ and $I_{in1} = I_{in3} = 0$
- High Pass filter – $I_{in3} = I_{in}$ and $I_{in1} = I_{in2} = 0$
- Band Stop filter – $I_{in1} = 0$ and $Iin_2 = I_{in3} = I_{in}$
- All Pass filter – $I_{in1} = I_{in}$ and $Iin_2 = 2I_{in3}$ and $I_{in1} = 0$.

From the circuit presented, we can achieve all five standard quadratic filtering functions by using the same circuit topology. The value of the Q and ω_0 parameters of these universal filter are as follows:

$$\omega_0 = \sqrt{\frac{g_m}{R_1 C_1 C_2}} \quad \ldots 5.2$$

$$Q = \sqrt{\frac{g_m R_1 C_1}{C_2}} \quad \ldots 5.3$$

From the above two equation 5.2 & 5.3 it is noted that ω_0 can be tuned from the value of capacitor C1 and C2 and keep the value g_m/R_1 to be same whereas value of Q is controlled by the $g_m R_1$ and maintaining ratio of capacitors C_1/C_2 to be constant. From all this we conclude that presented circuit of filter provides orthogonal control of the filters parameter Q and ω_0.

Sensitivity of the parameter ωo relative to values of trans-conductance gain and passive components are equal to half only.

$$S_{g_m}^{\omega_0} = -S_{R_1}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2}$$

Sensitivity of the parameter Q relative to values of trans-conductance gain and passive components are equal to half only.

$$S_{g_m}^{Q} = S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

Therefore, presented circuit of universal filter exhibits a satisfactory value of a sensitivity.

5.3 Simulation and results

Presented circuit shown in fig 5.1 has value of passive component as resistor R_1 = 4.4K and the value of capacitors as C_1 = C_2 =30pF.All these setting has done to obtain universal biquadratic filter with Q = 1 and $f_0 = 1/2\pi$. Simulated frequency response of standard filters, LP, HP, BP and BS filters, shown respectively in Figures 5.3, 5.4, 5.5 and 5.6. From the simulation results we realize that the natural frequency is 1.22MHz. Therefore, the average frequency deviation is around 0.82 percent. Figure 5.7 shows simulated filter response of the Band Stop (BS) at different capacitor values of 50 pF, 30 pF and 10 pF. From simulated response we conclude that natural frequency is tuned at capacitor value is varied.

Table 5.1

Transistors	**W/L(μm)**
M_1-M_4	**3.6/1.8**
M_5-M_6	**7.2/1.8**
M_7-M_8	**2.4/1.8**
M_9-M_{10}	**3.06/0.72**
M_{11}-M_{12}	**9/0.72**
M_{13}-M_{17}	**14.4/0.72**
M_{18}-M_{22}	**0.72/0.72**

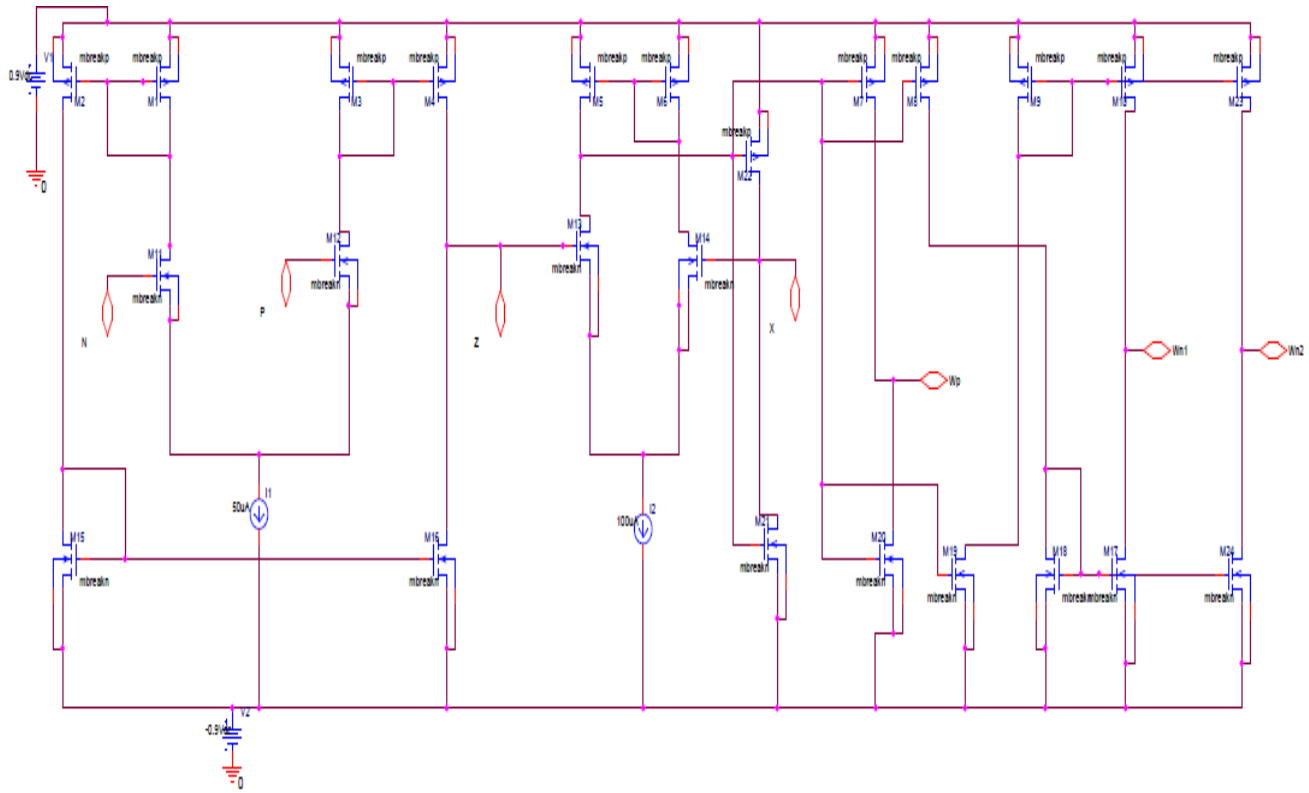


Fig 5.2 Schematic of VDCC using CMOS [18]

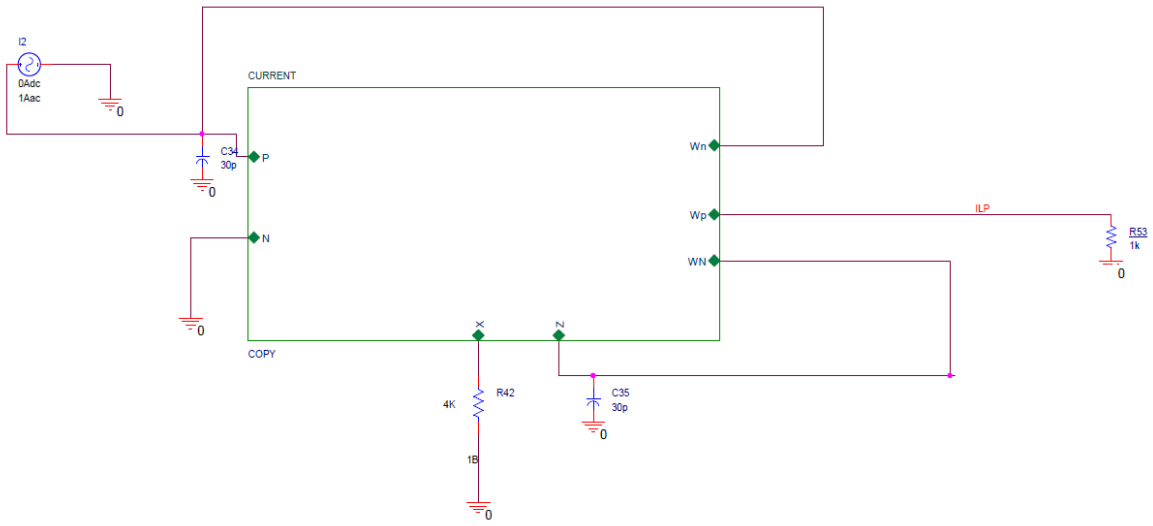


Fig 5.3 Current biquadratic filter schematic for Low Pass filter [18]

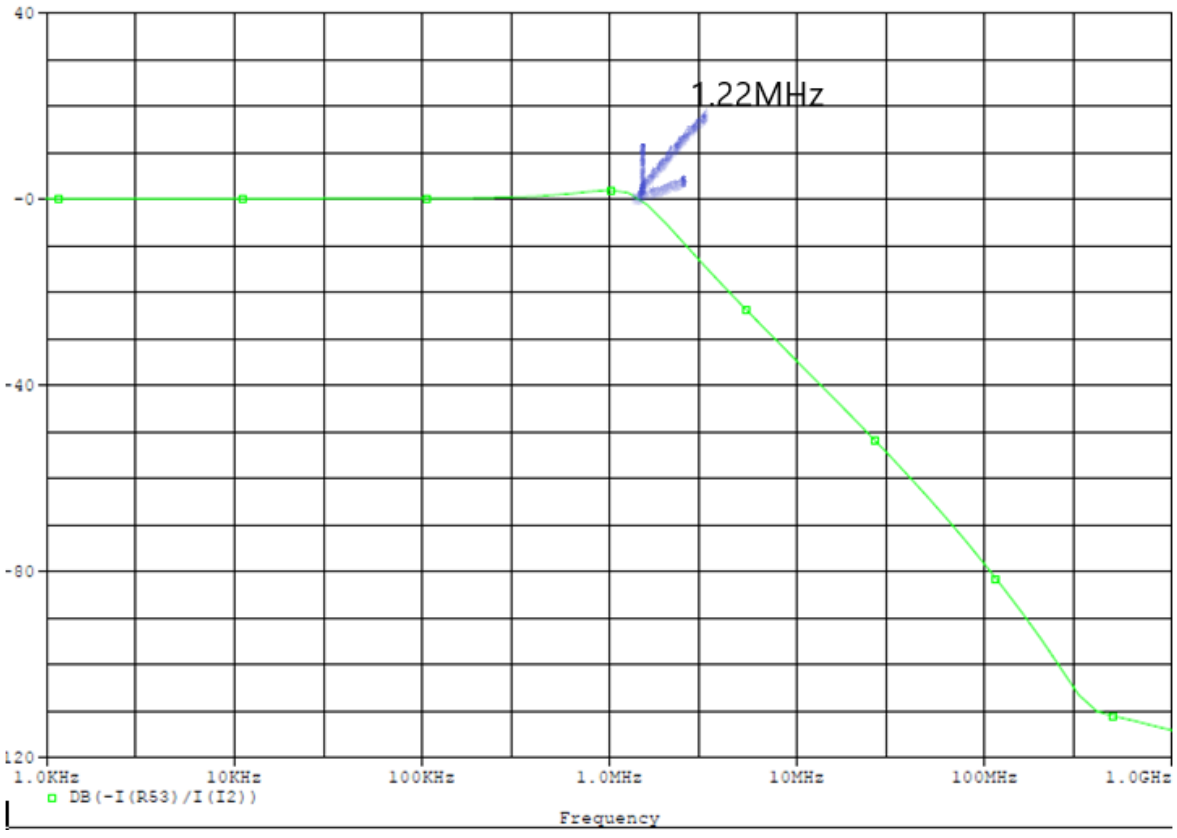


Fig 5.4 Frequency response of current biquadratic filter for Low Pass filter

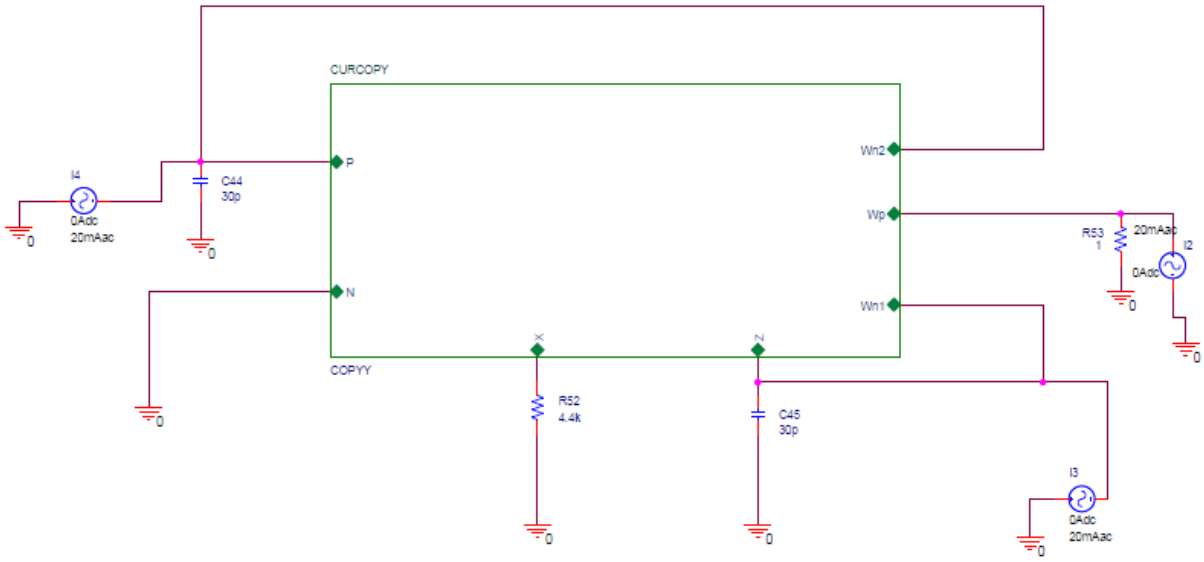


Fig 5.5 Current biquadratic filter schematic for High Pass filter [18]

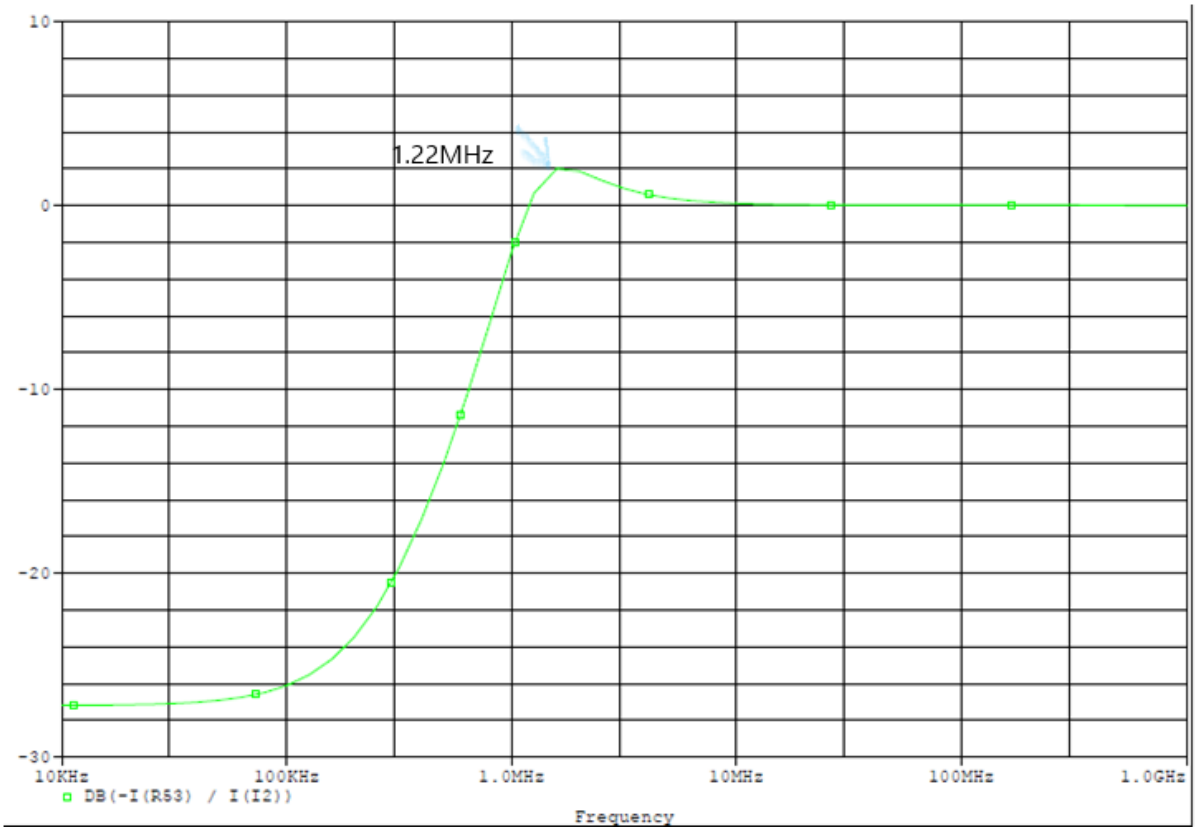


Fig 5.6 Response of current biquadratic filter for Hgh Pass filter

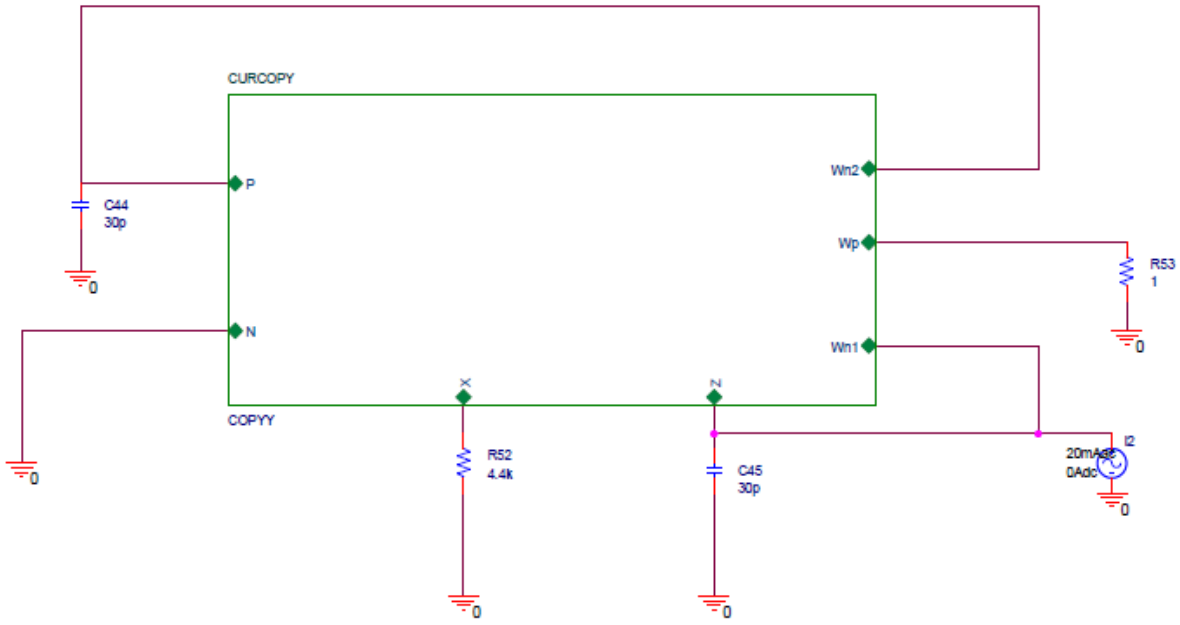


Fig 5.7 Current biquadratic filter schematic for Band Pass filter [18]

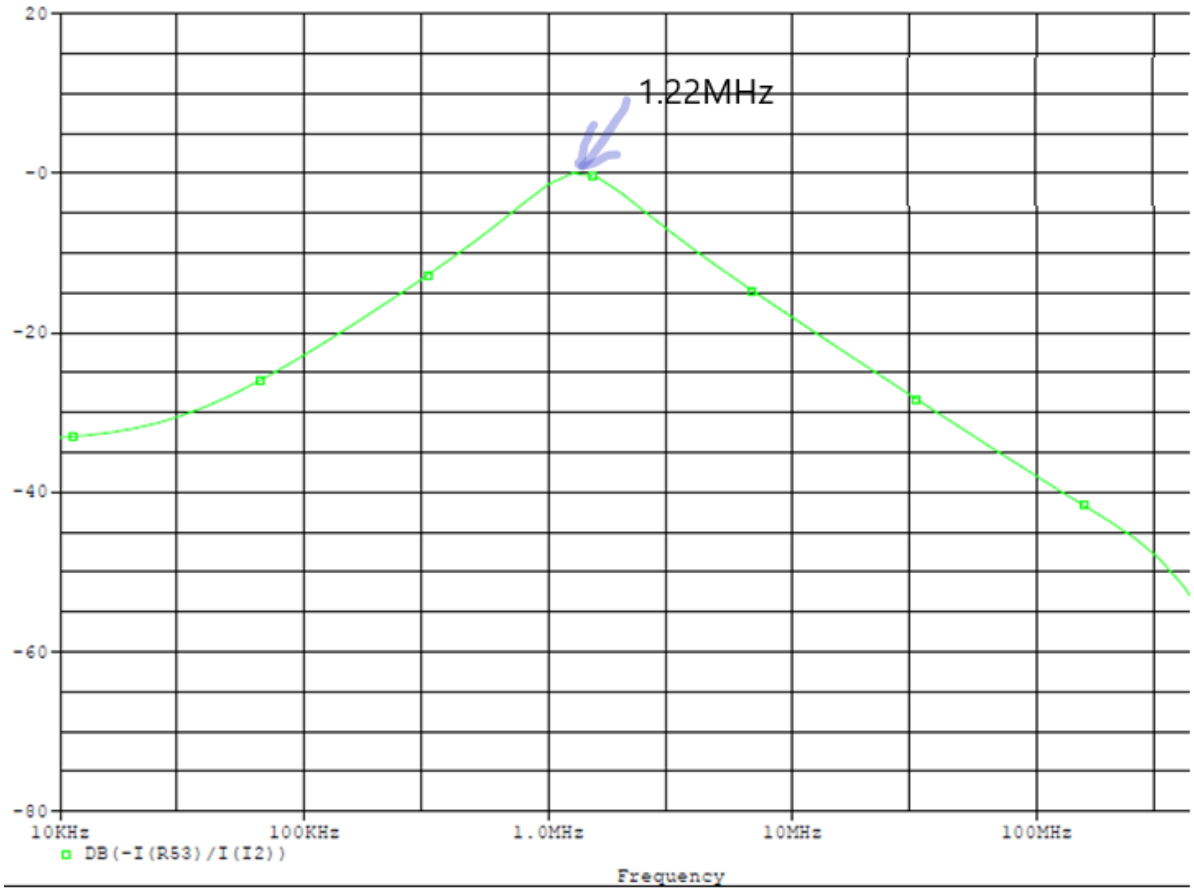


Fig 5.8 Response of current biquadratic filter for Band Pass filter

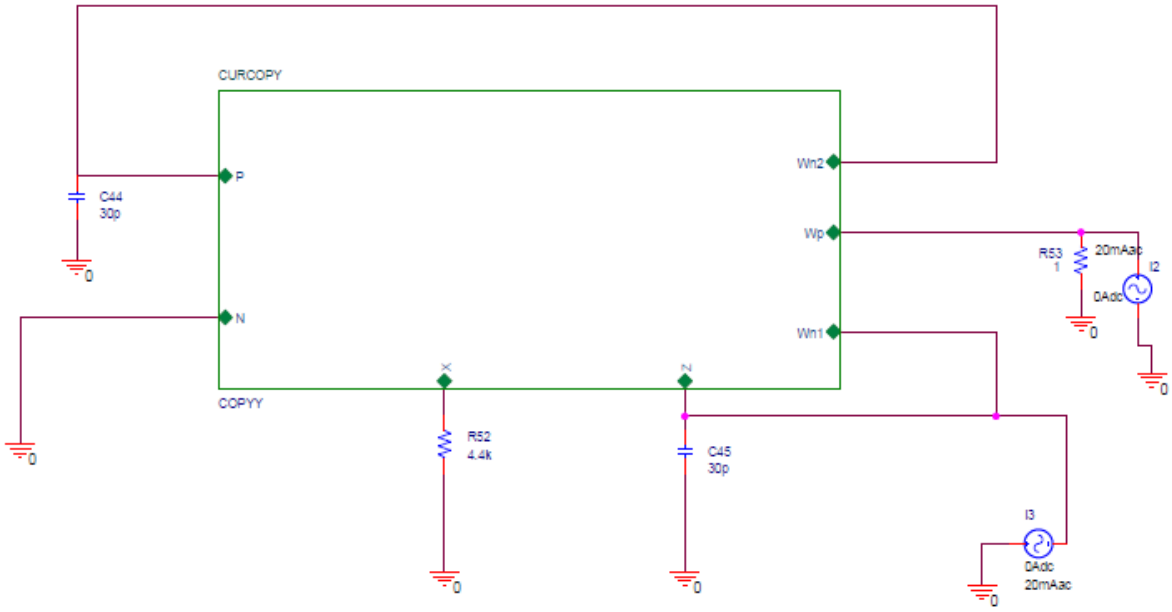


Fig 5.9 Current biquadratic filter schematic for Band Stop filter 18]

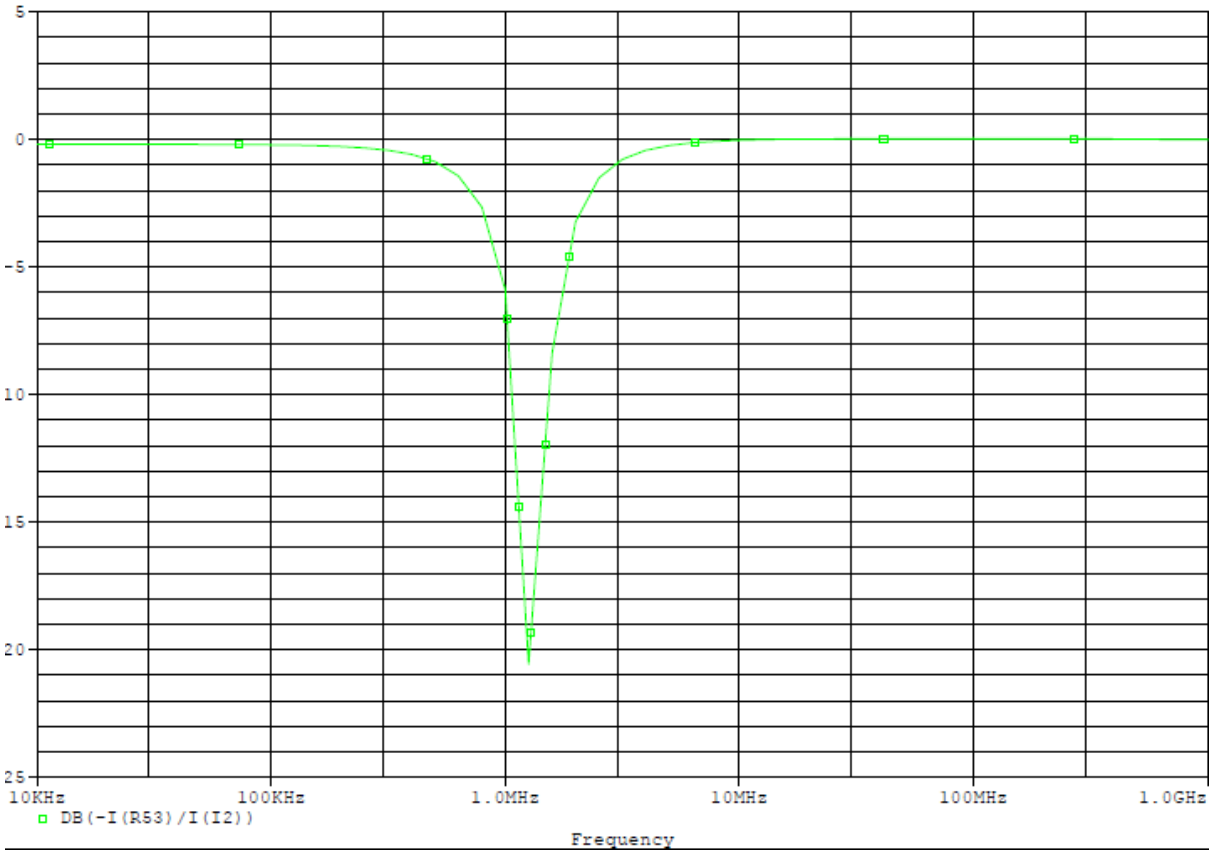


Fig 5.10 Response of current biquadratic filter for Stop Band filter

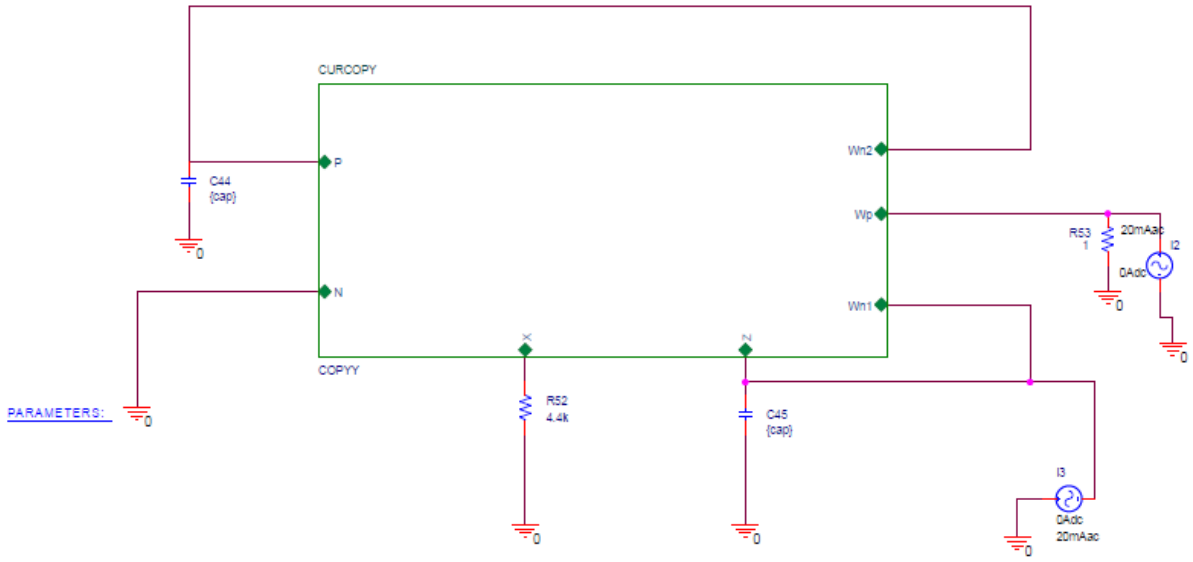


Fig 5.11 Current biquadratic filter schematic for Band Stop filter with varying capacitor [18]

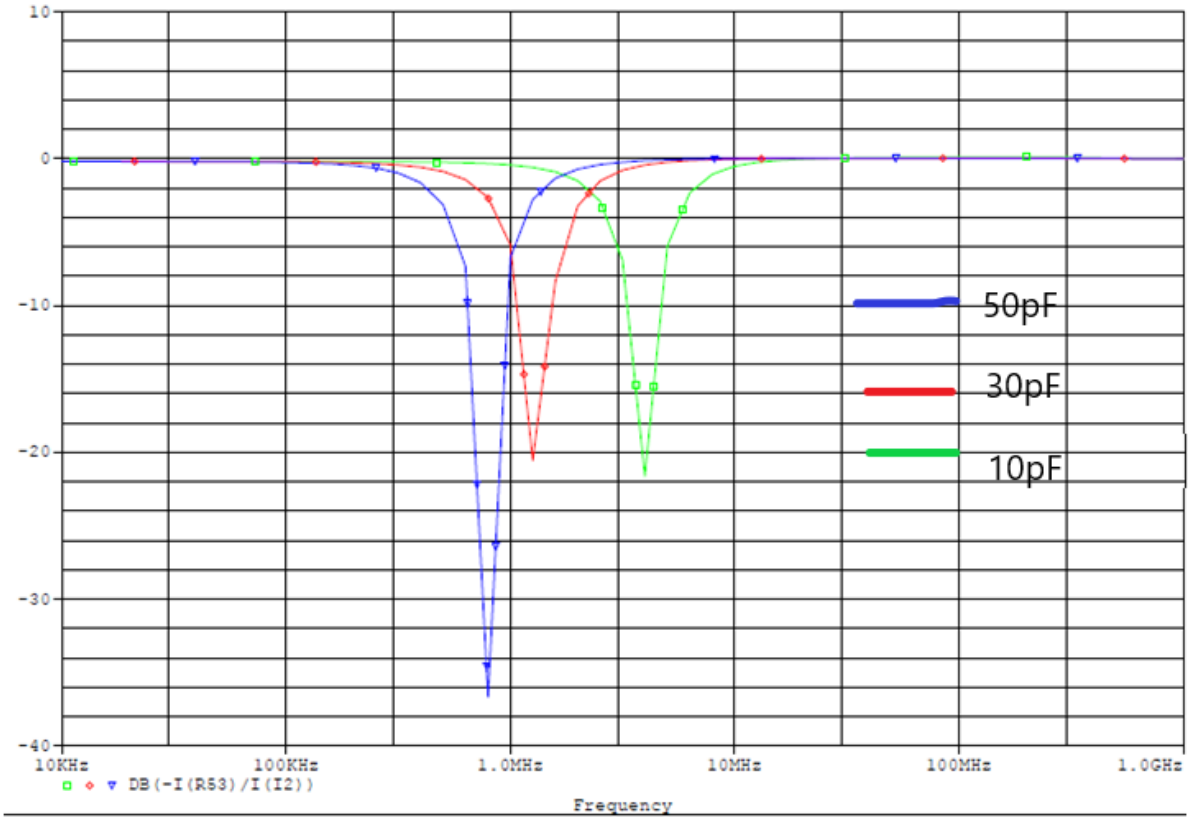


Fig 5.12 Frequency response of current biquadratic for Band Stop filter

CHAPTER 6

Single VDCC-based Explicit Current- Mode SRCO

6.1 Introduction

Special attention is now given to a single active block based on single resistance controlled sinusoidal oscillators (SRCOs)[31-43] that operate mainly in SRCOs current mode. There are no. of advantages of using single resistance ABB like it save chip area, manufacturing cost and power dissipation in comparison of two ABBs. Because of larger bandwidth and higher linearity, current mode operation is more used as compared to voltage mode.

6.2 VDCC- based SRCO

The VDCC transfer voltage and current to its relevant terminals along with it provide electronically tunable transconductance gain.VDCC provides many applications. It has 6 terminals in which only X terminal has low impedance as compared to other terminals.

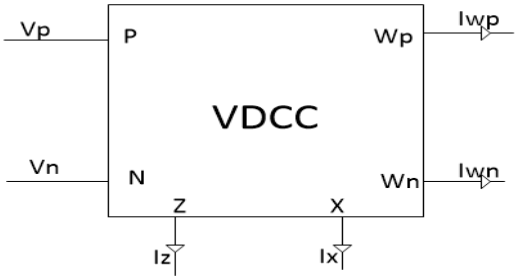


Fig 6.1 VDCC block diagram representation

The ideal VDCC matrix for port is as shown below:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

A new explicit current mode SRCO oscillator is presented using single VDCC and with minimum number of passive elements. Figure 6.2 shows configuration. The present circuit has the benefits of:

1. Independent condition of oscillation and frequency of oscillation with explicit.

2. Having good stability in terms of frequency.

3. Low passive and active sensitivities.

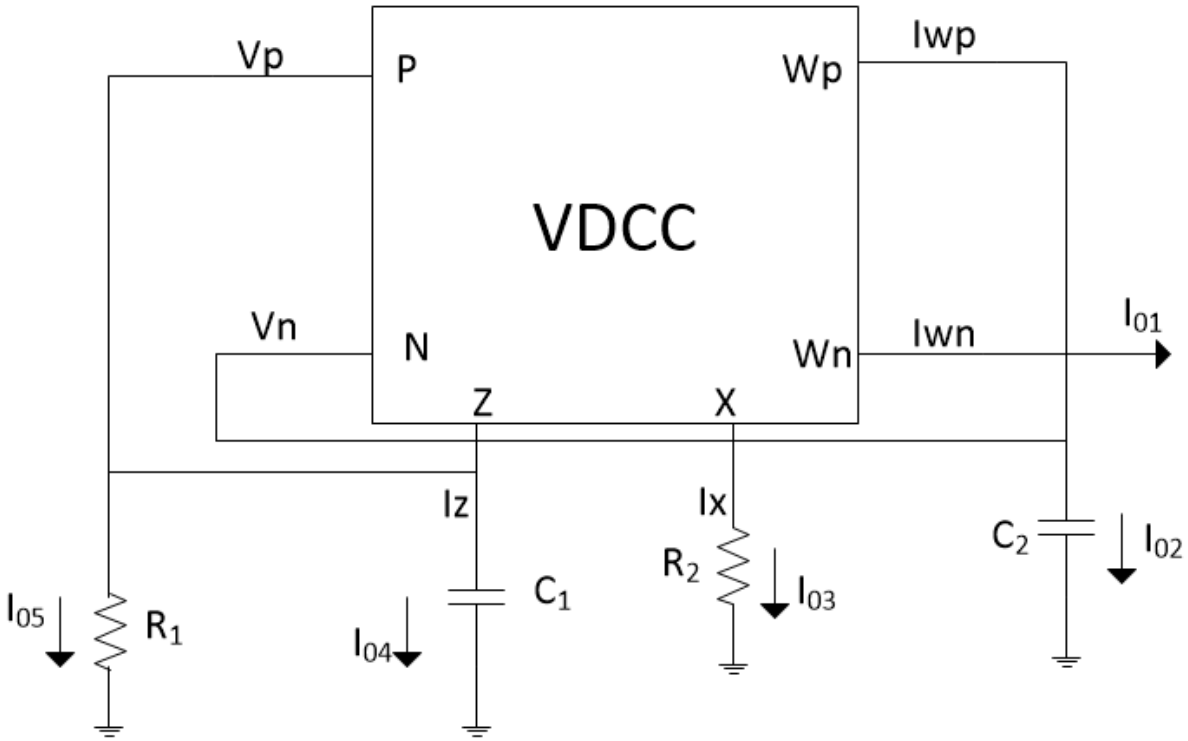


Fig. 6.2 SRCO circuit [30]

From the above circuit analysis characteristic equation obtained is as follows:

$$S^2 + S^1 \frac{1}{C_1}\left(\frac{1}{R_1} - g_m\right) + \frac{g_m}{R_2 C_1 C_2} = 0 \qquad \ldots 5.1$$

From equation 5.1 we obtained oscillation condition and frequency of oscillation of frequency as follows:

$$\frac{1}{C_1}\left(\frac{1}{R_1} - g_m\right) \leq 0 \qquad \ldots 5.2$$

And

$$\omega_0 = \sqrt{\frac{g_m}{R_2 C_1 C_2}} \qquad \ldots 5.3$$

From equation 5.2 & 5.3 we conclude that CO is controlled by R_1 where as FO is controlled by R_2. Therefore both FO and CO are independent to each other.

The following two open loops transfer function are also obtained from the presented circuit:

$$\frac{\mathrm{I_{01}}}{\mathrm{V_{in}}} = \frac{S(\frac{C_2 g_m}{R_2})}{S^2+S^1(\frac{1}{R_1C_1})+\frac{g_m}{R_2C_1C_2}} \quad \ldots 5.4$$

$$\frac{\mathrm{I_{04}}}{\mathrm{V_{in}}} = \frac{S^2 g_m}{S^2+S^1(\frac{1}{R_1C_1})+\frac{g_m}{R_2C_1C_2}} \quad \ldots 5.5$$

We obtained the natural frequency and bandwidth from above equations 5.4 and 5.5 as follows:

$$\omega_0 = \sqrt{\frac{g_m}{R_2C_1C_2}}$$

$$\text{B.W.} = \frac{1}{R_1C_1}$$

Now we can see that both ω_0 and B.W. are independent tunable.

From the 3rd mode of operation, current transfer functions for fig. 5.2 given as:

$$\frac{I_{01}(s)}{I_{04}(\mathrm{s})} = -\frac{1}{SR_2C_1}$$

$$\frac{I_{02}(s)}{I_{04}(s)} = \frac{1}{SR_2C_1}$$

$$\frac{I_{03}(s)}{I_{04}(s)} = -\frac{1}{SR_2C_1}$$

$$\frac{I_{05}(s)}{I_{04}(s)} = -\frac{1}{SR_1C_1}$$

For sinusoidal state above equations become as follows:

$$\frac{I_{01}(\mathrm{j}\omega)}{I_{04}(j\omega)} = \frac{1}{\omega R_2C_1} e^{j90^0}$$

$$\frac{I_{02}(j\omega)}{I_{04}(j\omega)} = \frac{1}{\omega R_2C_1} e^{-j90^0}$$

$$\frac{I_{03}(j\omega)}{I_{04}(j\omega)} = -\frac{1}{\omega R_2 C_1} e^{-j90^0}$$

$$\frac{I_{05}(j\omega)}{I_{04}(j\omega)} = -\frac{1}{\omega R_1 C_1} e^{-j90^0}$$

Now we conclude there is 90^0 phase difference between I_{01} and I_{04} and that of -90^0 between I_{02} and $I_{04,}$ I_{03} and $I_{04,}$ I_{05} and $I_{04.}$

Therefore, there is a quadrature form between the currents I_{01} and $I_{04,}$ I_{02} and $I_{04,}$ I_{03} and $I_{04,}$ I_{05} and $I_{04.}$ Hence the circuit working is similar to quadrature oscillator.

6.3 Simulation and Results

The passive component value is set to $C_1 = C_2 = 0.01$nf, $R_1 = 3.675$ K and $R_2 = 10$K. Following the output waveform results, verify the validity of the presented configuration and we obtained an oscillation frequency of 2.56MHz and a total harmonic distortion of 1.65%. It is clear from fig.5.7 phase shift between two current waveforms is 89.49^0 i.e. quadratic in nature.

Table 6.1

Transistors	**W/L(μm)**
M_1-M_4	**3.6/1.8**
M_5-M_6	**7.2/1.8**
M_7-M_8	**2.4/1.8**
M_9-M_{10}	**3.06/0.72**
M_{11}-M_{12}	**9/0.72**
M_{13}-M_{17}	**14.4/0.72**
M_{18}-M_{22}	**0.72/0.72**

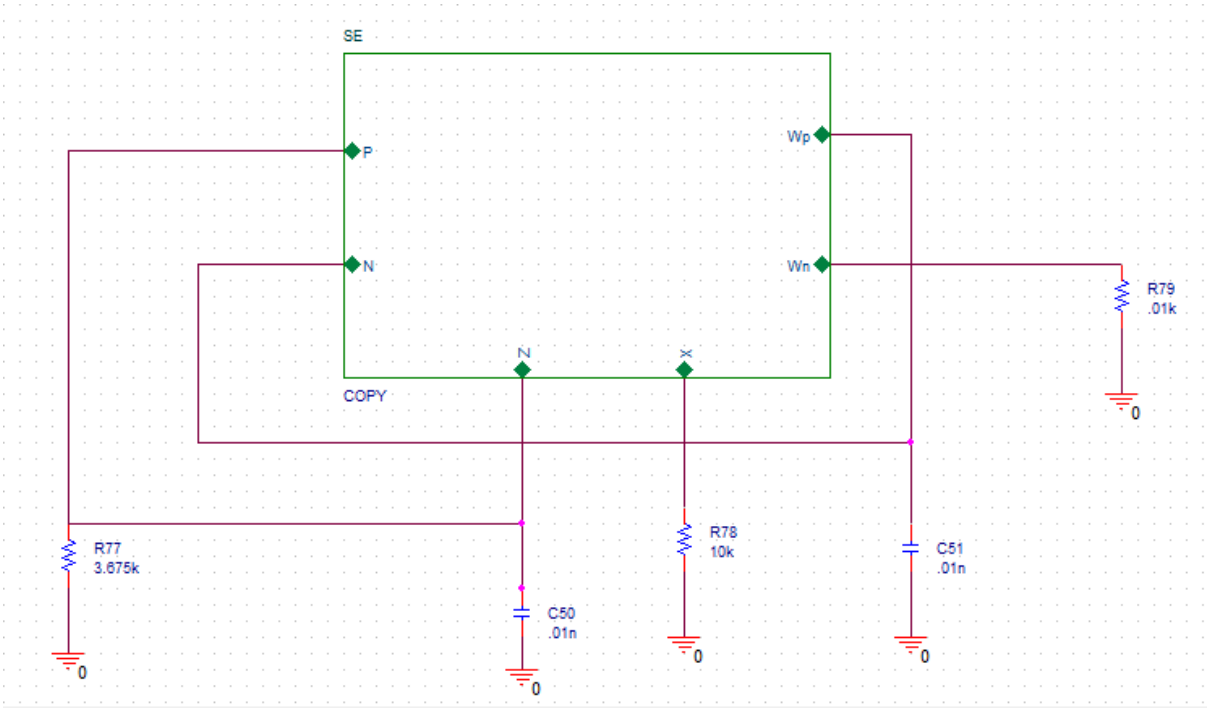
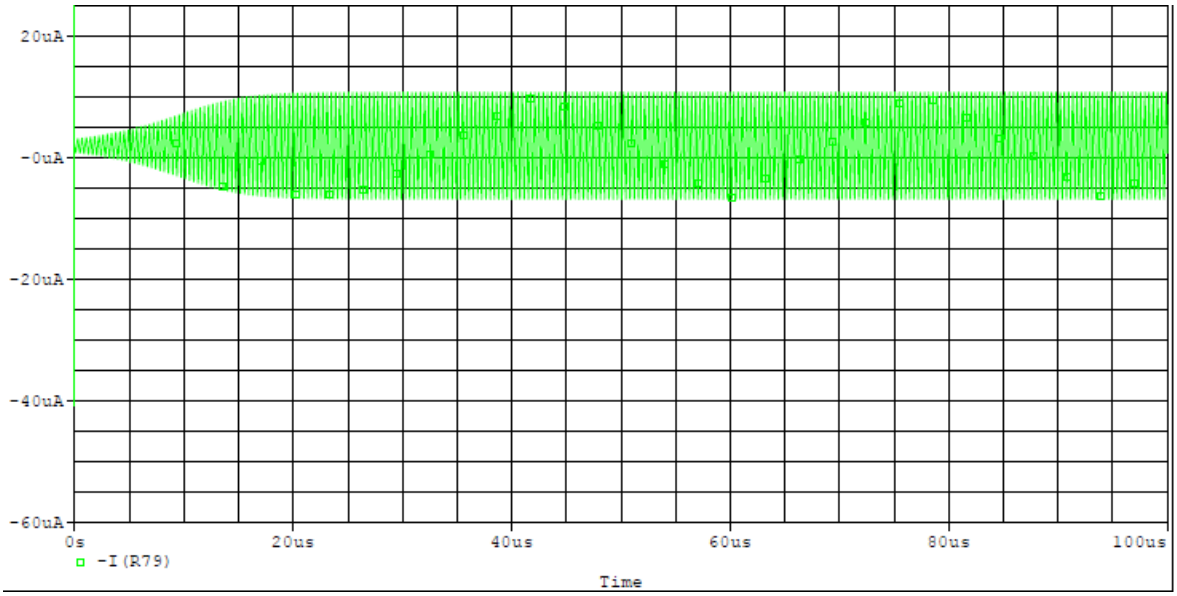
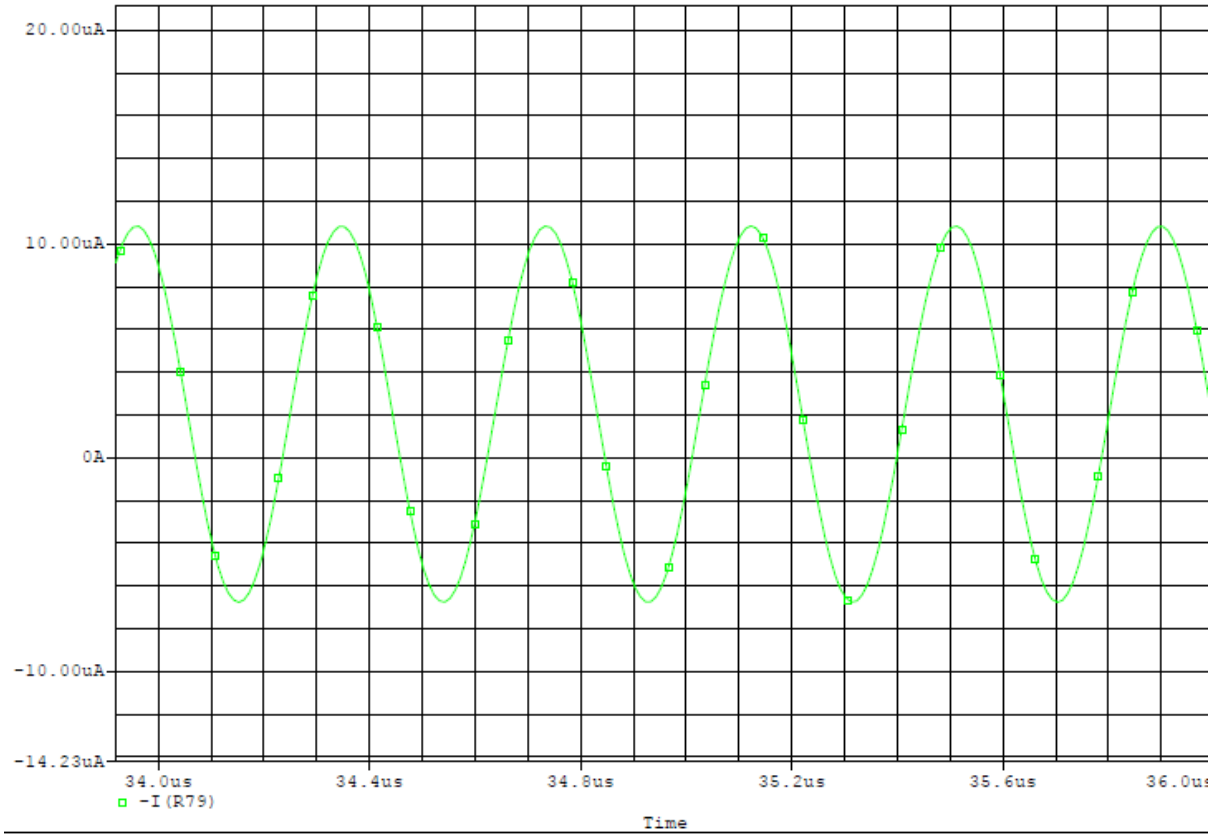


Fig 6.3 Schematic of SRCO [30]

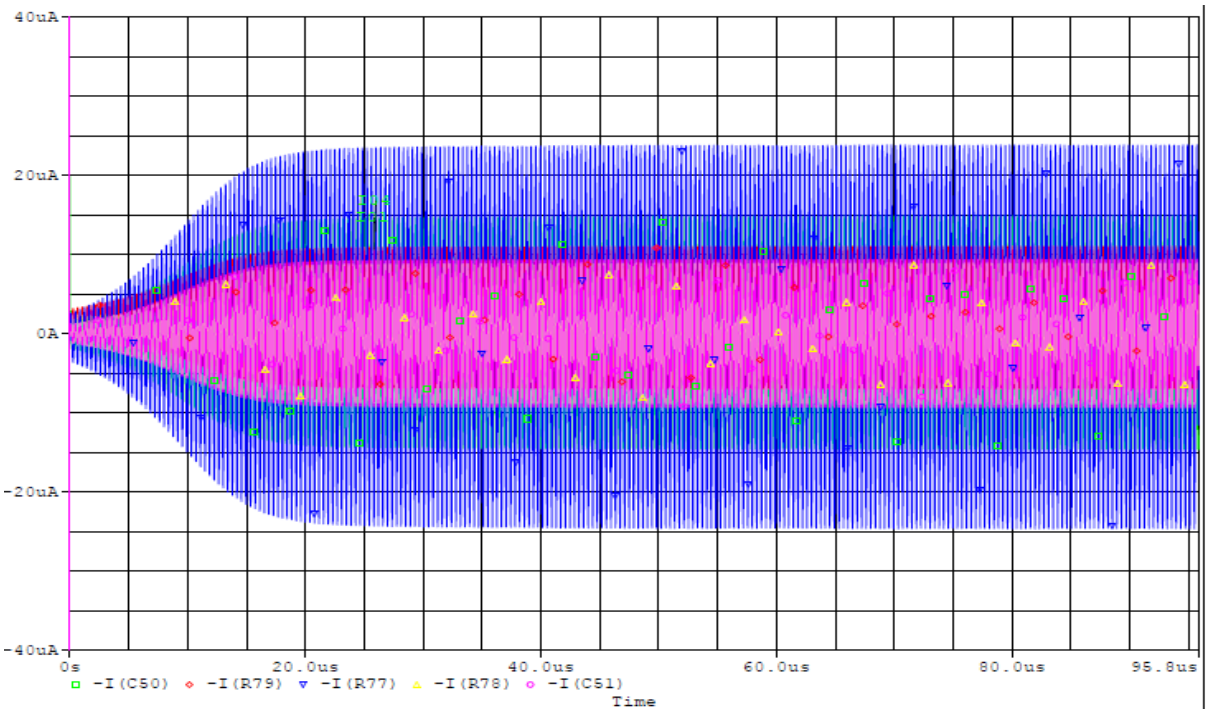


(a)

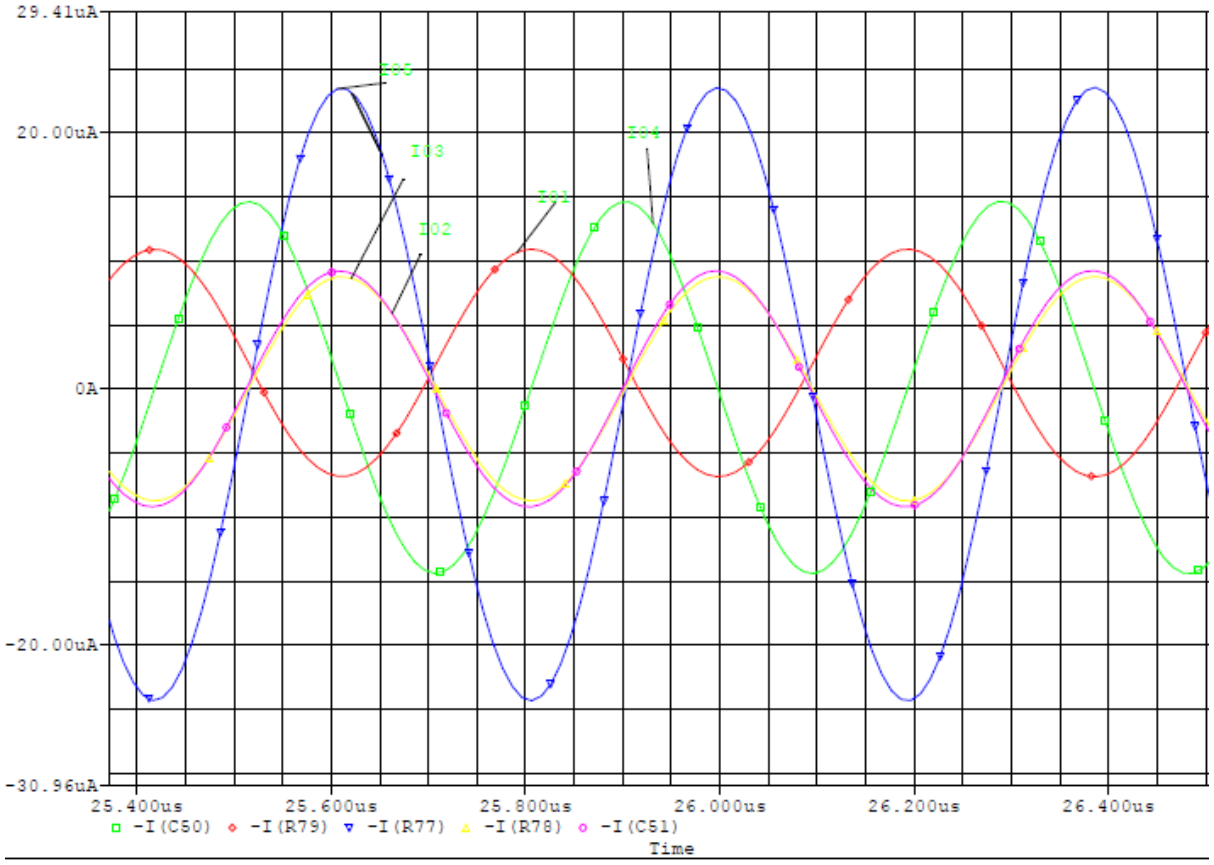


(b)

Fig 6.4 (a) Output of transient (b) Output of steady state response

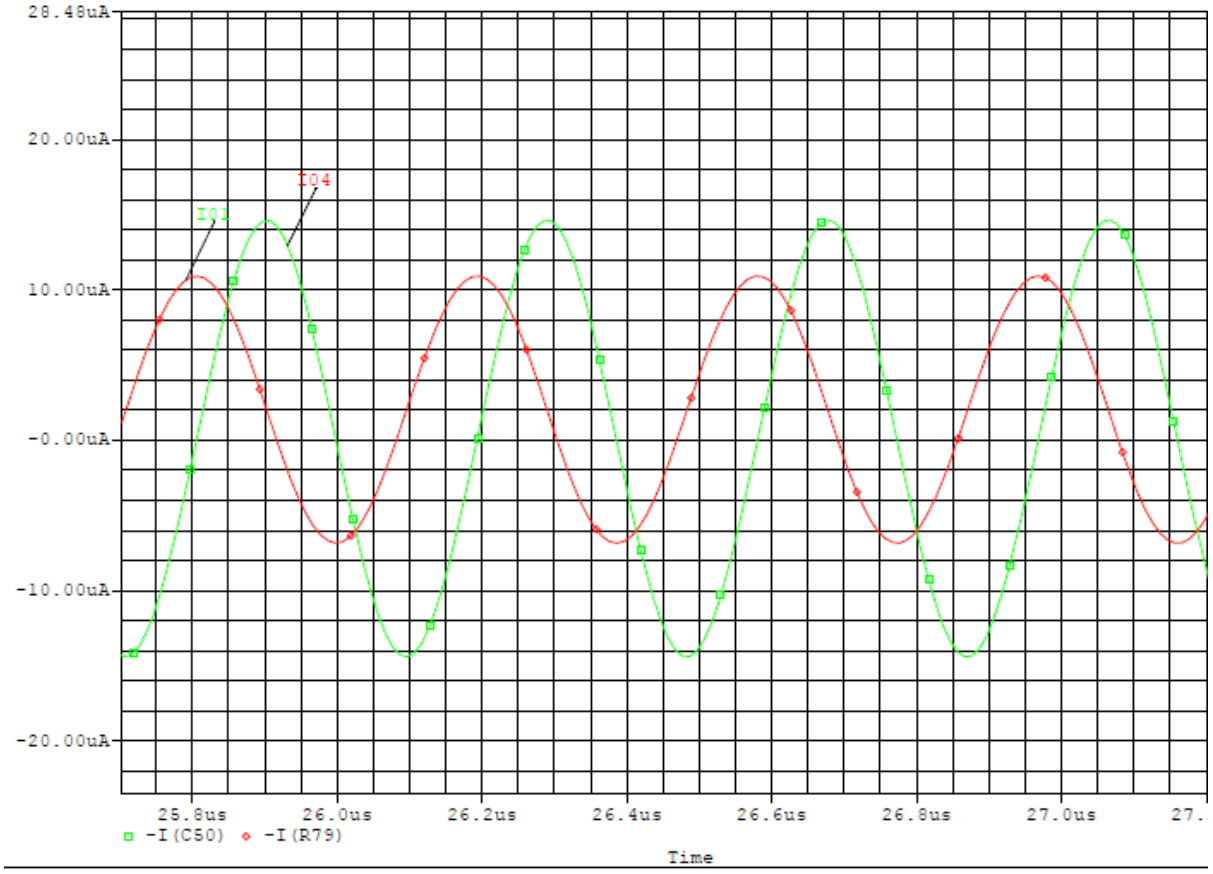


(a)

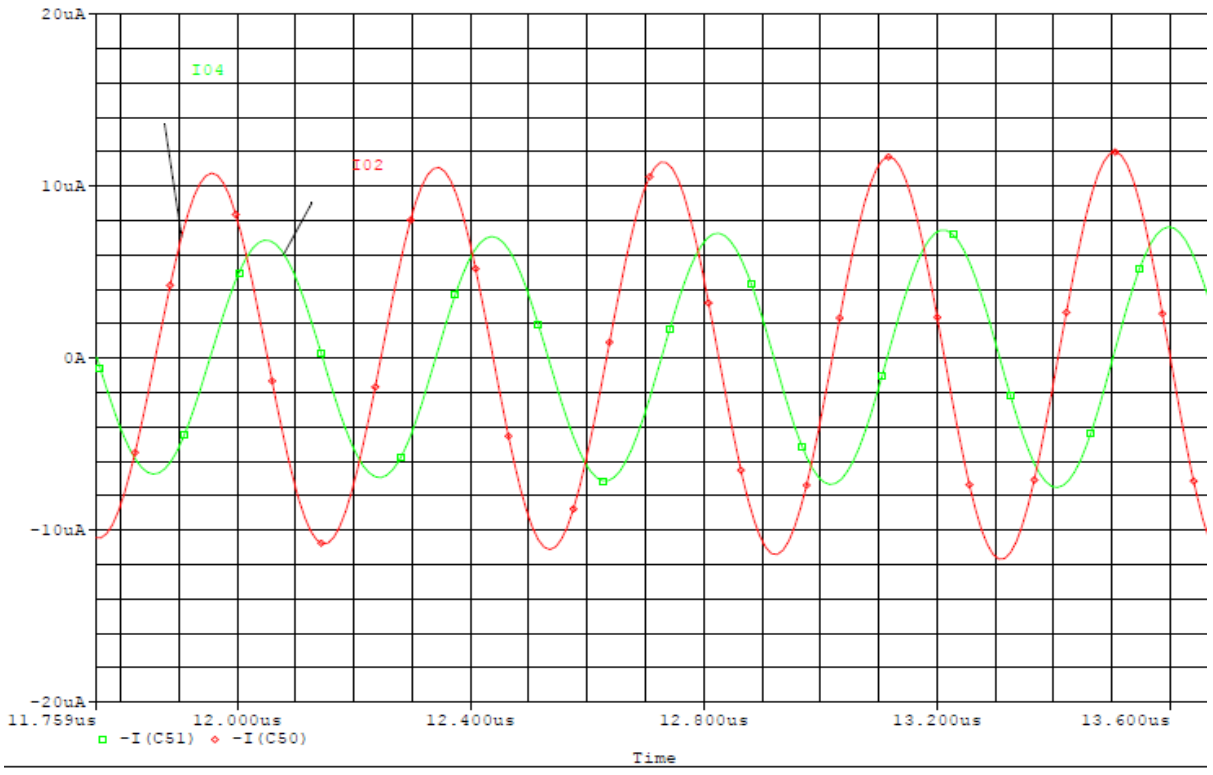


(b)

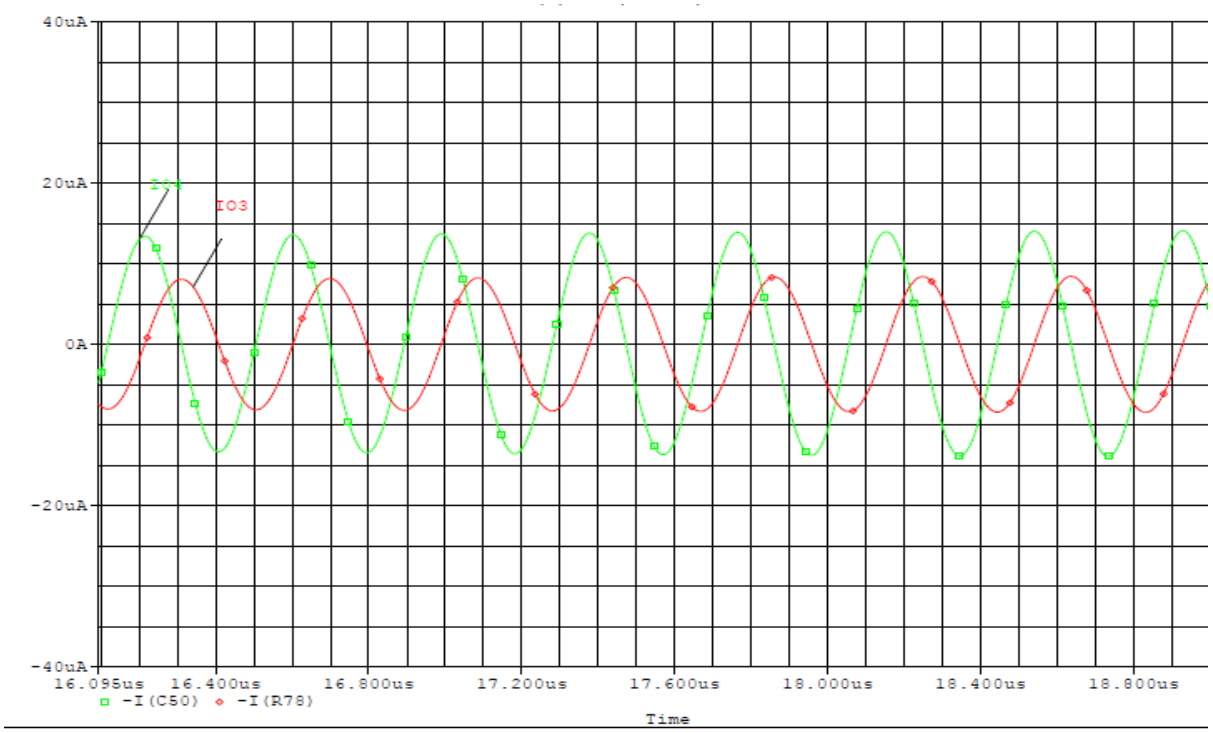
Figure 6.5 (a) Transient output (b) Steady-state response output


28.48uA
20.00uA
10.00uA
-0.00uA
-10.00uA
-20.00uA
I04
I01
25.8us
26.0us
26.2us
26.4us
26.6us
26.8us
27.0us
27.
-I(C50)
-I(R79)
Time

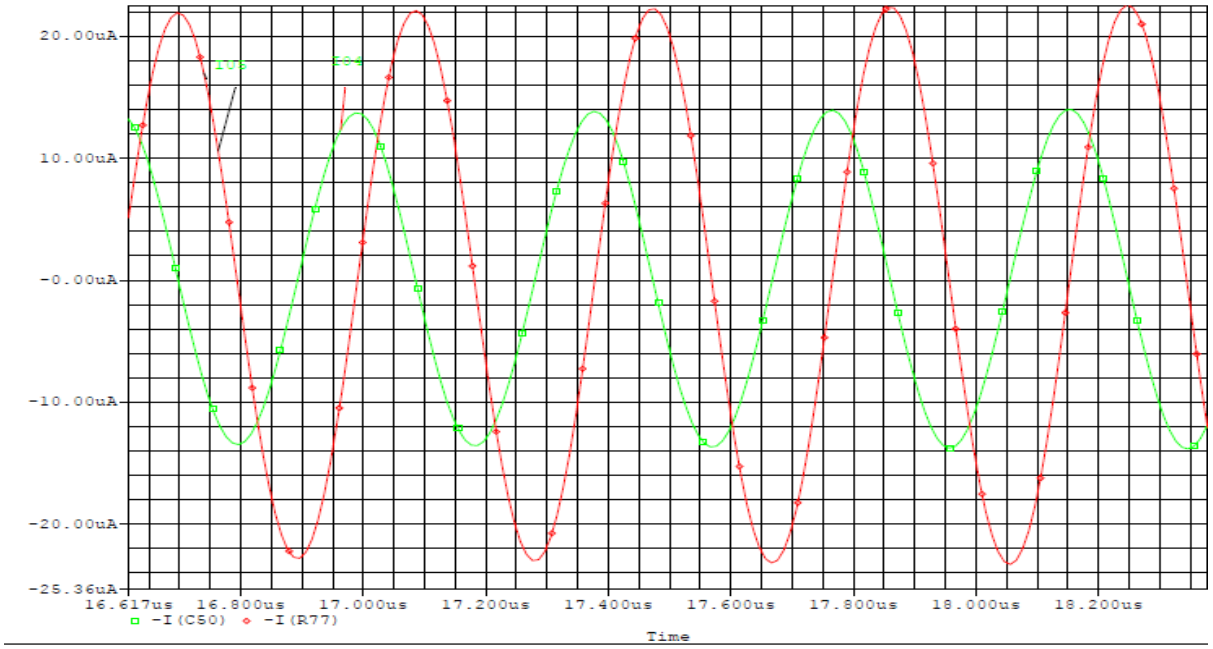
(a)


20uA
10uA
0A
-10uA
-20uA
I04
I02
11.759us
12.000us
12.400us
12.800us
13.200us
13.600us
-I(C51)
-I(C50)
Time

(b)



(c)



(d)

Fig 6.6 Quadratic wave forms between currents

CHAPTER 7

Sinusoidal Quadrature Oscillator with Independent Control

7.1 Introduction

Quadrature oscillators are those having 90 degree phase difference between two sinusoidal signals. Oscillators are used for signal processing that have different types of solicitations in the area of communications, control system, sound system, instruments etc. [1]. Special attention has recently been given to electronically tunable active building blocks as using them in analog circuits means we get more fine tuning compared to adjusting the passive device value. Recently it was reported that VDCC [5] is a versatile active building block that is used to create analog signal processing circuits. This is because VDCC has electronic controllability.

The quadrature sinusoidal oscillator consists of single VDCC, two grounded capacitors and three resistors which are suitable for chip implementation. FO and CO are independent of each other.

7.2 Voltage differencing current conveyors (VDCC)

The VDCC transfer voltage and current to its relevant terminals along with it provide electronically tunable transconductance gain. Symbolic VDCC notation is displayed in fig. 7.1 has five terminals. Only X terminal has low impedance as compared to other terminals.

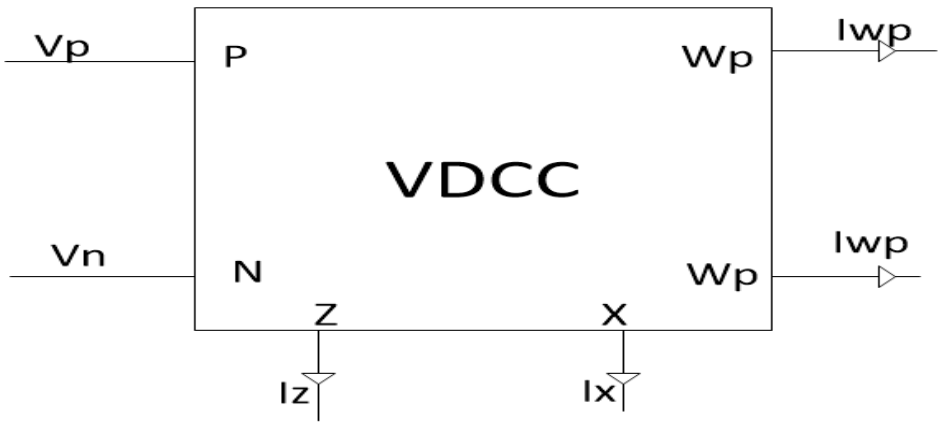


Fig 7.1 VDCC block representation [44]

Matrix for ideal VDCC is:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

Current and Voltage equation from matrix can be obtained as:

$$I_Z = gm\ (V_P - V_N)$$

$$V_X = V_Z$$

$$I_{WP} = I_X$$

7.3 VDCC-based Sinusoidal Quadrature Oscillator

The oscillator presented is composed of a single VDCC, two grounded capacitors and three resistors. I generate two sinusoidal waveforms that differ in phase 90^0. The presented circuit is shown in fig 7.2, the quadrature output voltages are described respectively as V_{o1} and V_{o2}.

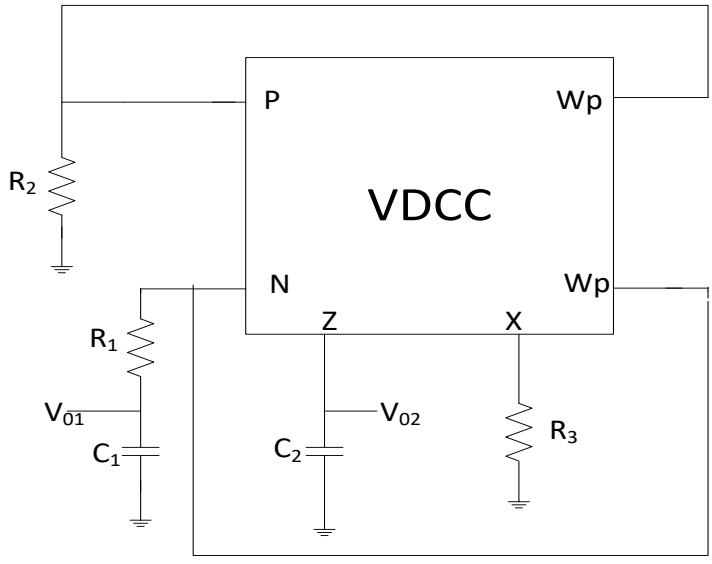


Fig 7.2 Quadrature sinusoidal oscillator [44]

Characteristic equation is obtained for the above oscillator quadrature as:

$$S^2\, C_1C_2R_3 + SC_2(R_1 - R_2) + g_m = 0 \qquad \ldots 7.1$$

From equation 7.1 we obtained CO and FO as follows:

$$R_1 \;\leq\; R_2 \qquad \ldots 7.2$$

And

$$\omega_0 = \sqrt{\frac{g_m}{R_3C_1C_2}} \qquad \ldots 7.3$$

From equation 7.2 & 7.3 we infer that the oscillation state and the oscillation frequency are independent of one another. With the aid of g_m you can tune FO

From the analysis of fig 7.2 circuit the voltage transfer function of the output voltages V_{o1} and V_{o2} is derived as follows:

$$\frac{V_{o1}}{V_{o2}} = \frac{1}{SC_1R_3} \qquad \ldots 7.4$$

From Eq. 7.4, it is observed the phase difference of V_{o2} and V_{o1} is 90^0

7.4 Simulation and Results

To verify the presented oscillator in Fig 7.2, we have to designed and simulated VDCC in Fig 7.1 using CMOS TSMC 180nm technology [22] as shown in Fig 7.3. Aspect ratio of each transistor in CMOS VDCC is according to table 7.1 , supplied voltages as ±0.9 VDC, biasing currents I_{b1} is 42µA and I_{B2} is 100µA respectively, Hence the value of trans-conductance obtained is g_m=262.65µA/V.

Values of passive component of presented circuit are resistor R_1 = 1.18K, R_2 = 2.2K, R_3 = 2K and the value of capacitors as $C_1 = C_2$ = .08nF.

From the results of simulation we come to know that frequency of oscillation f_0 is 340KHz. But theoretical frequency of oscillation is 323KHz. So there is 5% deviation in frequency of oscillation because of some parasitic elements and current/ voltage tracking error. From Fig 7.5 it is obtain that oscilltor circuit generate two sinusoidal waveform which have 90^0 phase between them, hence it is verified that prsented circuit is quadratic sinusoidal oscillator circuit.

Table 7.1

Transistors	W/L(μm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{15}	14.4/0.72
M_{18}-M_{20}	0.72/0.72

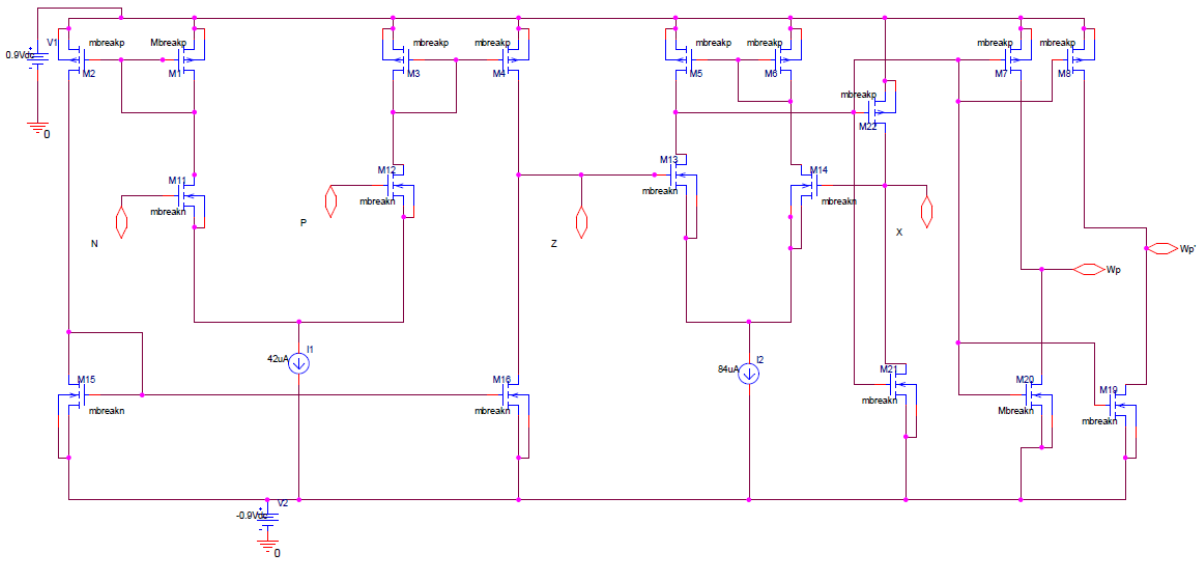


Fig 7.3 CMOS based VDCC schematics

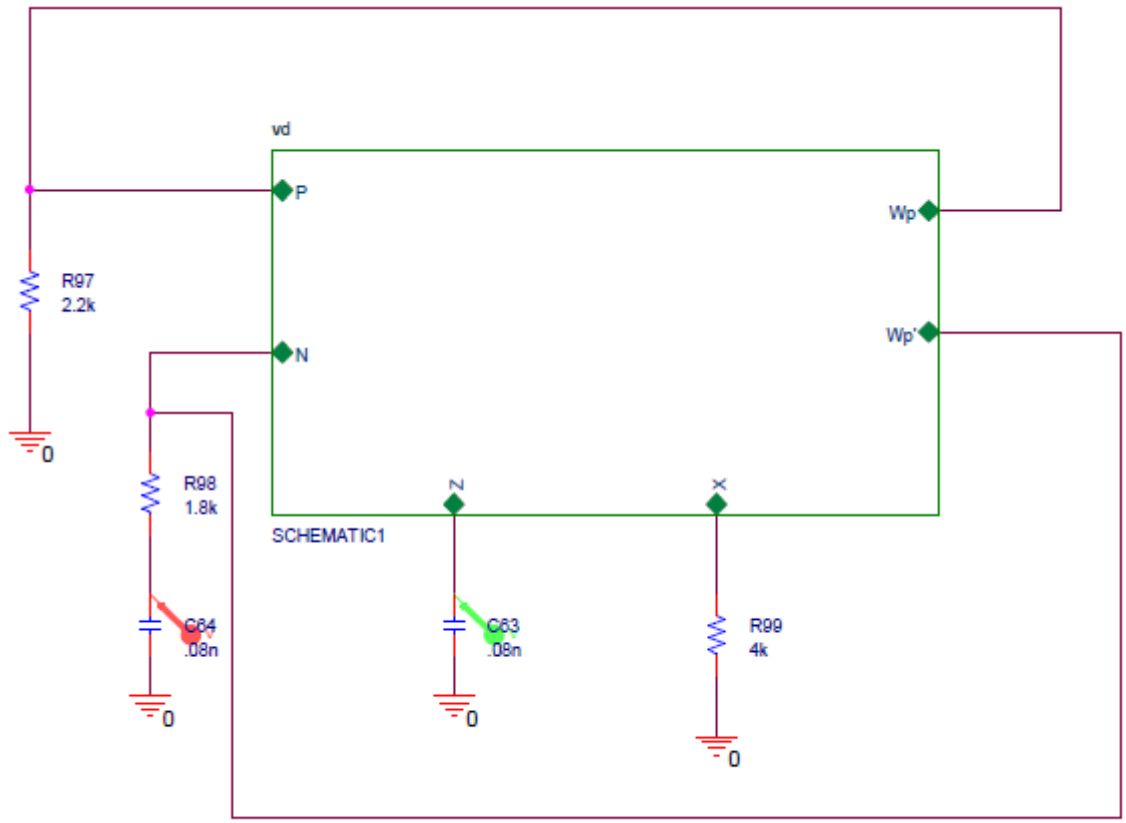
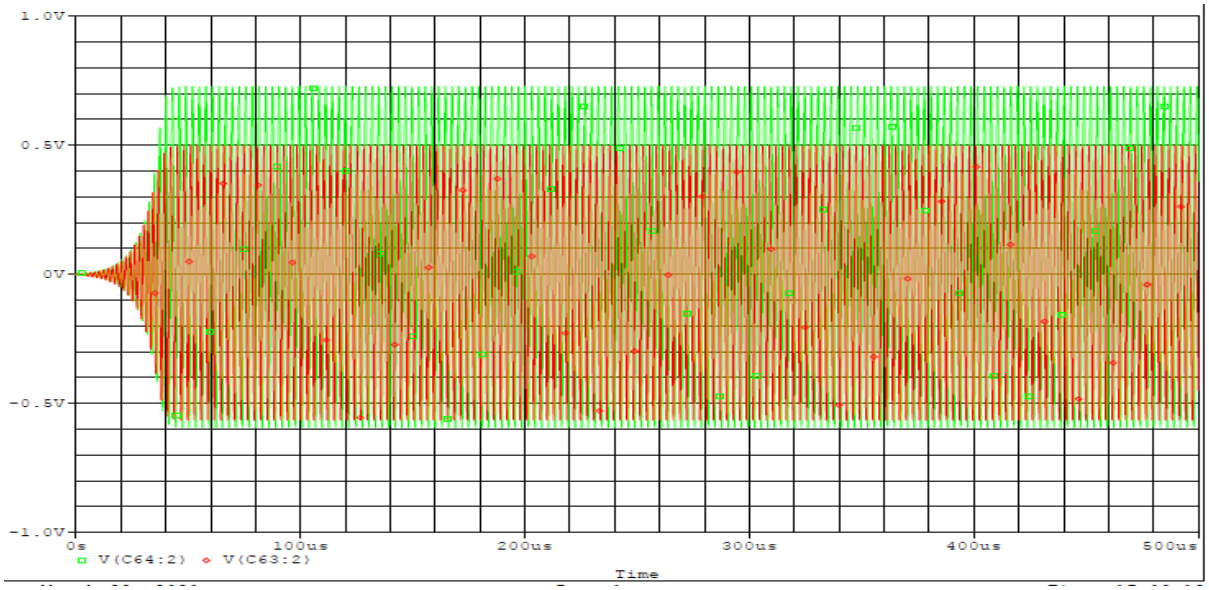
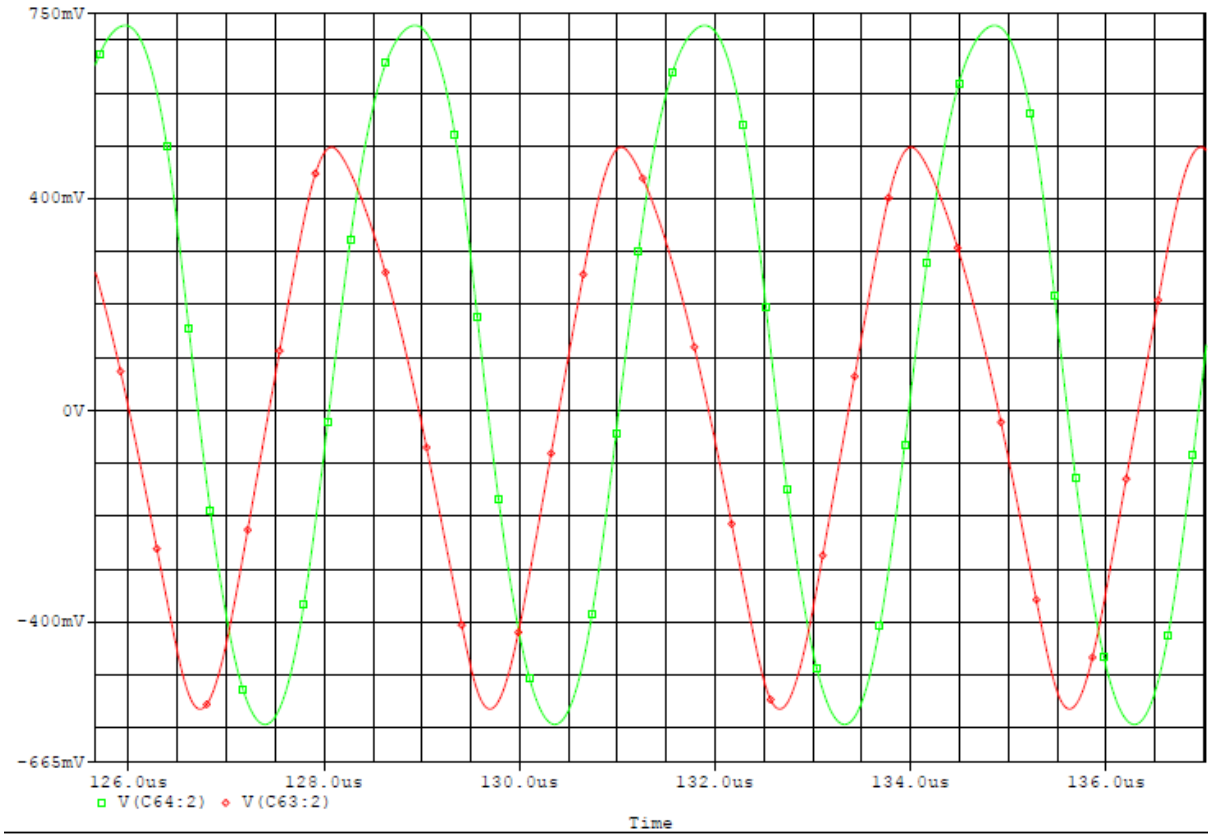


Fig 7.4 Quadrature sinusoidal oscillator schematics



(a)



(b)

Fig 7.5 (a) Output of transient (b) Output of steady state response

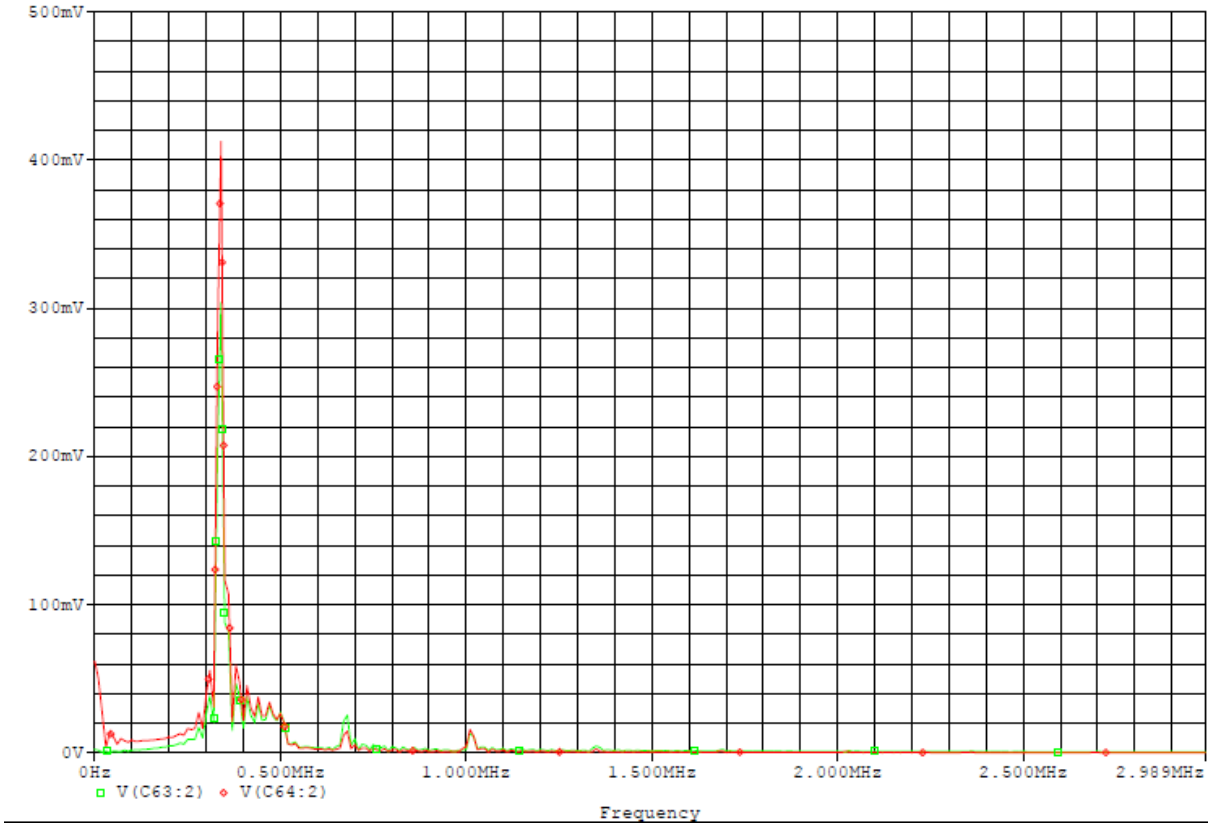


Fig 7.6 Output spectrum of voltage V_{01} & V_{02}

CHAPTER 8

Dual Mode Quadrature Sinusoidal Oscillator

8.1 Introduction

Oscillator has several communications, signal processing, measurement, instrumentation and control applications. An oscillator which provides two sinusoidal waves having 90^0 phase shift known as quadrature sinusoidal oscillator. Dual mode quadrature sinusoidal oscillator generates oscillation in both voltage and current mode and generated waves are sinusoidal having 90^0 phase.

In literature, by employing various active building block dual-mode quadrature sinusoidal oscillators has been presented in [47] - [51]. But they do have one or more drawbacks:

(i) Not good for monolithic integration

(ii) FO and CO depend on each other

(iii) Both FO and CO has dependent resistive control

(iv) Explicit quadrature Current Mode outputs are also not available that is desirable for additional current followers to take out currents and for sensing.

VDCC overcomes all these disadvantages and reported a new sinusoidal quadrature oscillator Current Mode and Voltage Mode consisting of two VDCCs, two capacitors and two resistors with the following advantages:

1. All passive components are grounded.

2. Both the FO and CO are electronically autonomous controls.

3. Independent FO and CO tuning is unique, even under a non-ideal configuration.

4. Explicit Current Mode quadrature outputs are available with high impedance.

5. Low impedance quadrature Voltage Mode outputs are available.

6. Low active / passive, and low active sensitivity.

7. Frequency stability is fine.

8.2 Dual mode Oscillator quadrature based on VDCC

Dual mode sinusoidal oscillator quadrature consisting of two active voltage differentiating current conveyors (VDCCs) building blocks, two condensers and two resistors as shown in Fig 8.1 This concept circuit uses only passive elements that are grounded and have isolated resistor or electronic tuning for Oscillation Condition as well as for Oscillation Frequency.

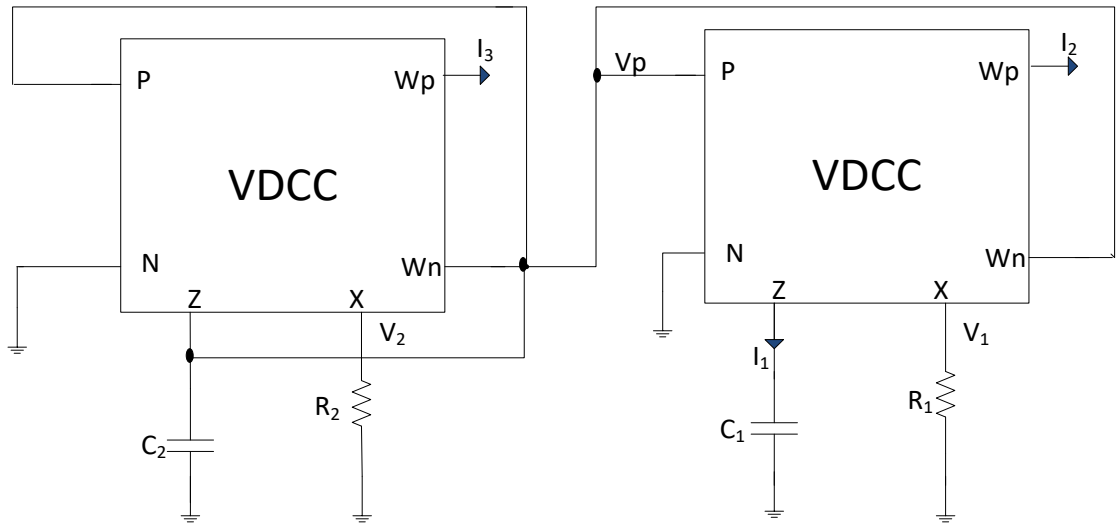


Fig 8.1 circuit of dual mode quadrature oscillator [46]

From the above circuit analysis characteristic equation obtained is as follows:

$$S^2 + S\frac{1}{C_2}\left(\frac{1}{R_2} - g_{m2}\right) + \frac{g_{m1}}{R_1C_1C_2} = 0 \qquad \ldots 8.1$$

From equation 8.1 we obtained CO and FO as follows:

$$\left(\frac{1}{R_2} - g_{m2}\right) \leq 0 \qquad \ldots 8.2$$

And

$$\omega_0 = \sqrt{\frac{g_{m2}}{R_1C_1C_2}} \qquad \ldots 8.3$$

From equation 8.2 & 8.3 we conclude that CO is controlled by R_2 or g_{m2} where as FO is controlled by R_2. Therefore both FO and CO are independent to each other.

Following current transfer functions for fig. 8.1 given as :

$$\frac{I_2(s)}{I_1(s)} = \frac{1}{SR_1C_1}$$

$$\frac{I_2(s)}{I_3(s)} = \frac{g_m R_2}{SR_1C_1}$$

For sinusoidal state above equations become as follows:

$$\frac{I_2(j\omega)}{I_1(j\omega)} = \frac{1}{\omega R_1 C_1} e^{-j90^0}$$

$$\frac{I_2(j\omega)}{I_3(j\omega)} = \frac{g_m R_2}{\omega R_2 C_1} e^{-j90^0}$$

Now we conclude there is -90^0 phase difference between I_2 and I_1, I_2 and I_3. Therefore, there is a quadrature form between the currents I_2 and I_1, I_2 and I_3.

We also obtain Voltage transfer functions from the analysis of Fig 8.1 as Follows :

$$\frac{V_1(s)}{V_2(s)} = \frac{g_{m1}}{sC_1}$$

For sinusoidal state above equations become as follows:

$$\frac{V_1(j\omega)}{V_2(j\omega)} = \frac{g_{m1}}{sC_1} e^{-j90^0}$$

Now we conclude there is -90^0 phase difference between voltages. Therefore, there is a quadrature form between the voltages V_1 and V_2.

8.3 Non – Ideal VDCC model analysis of oscillator

When considering constants of non-ideal current and voltage transfer between different VDCC terminals, the characteristics of VDCC equations must be changed. Taking into consideration VDCC's voltage transfer error(β), current transfer errors (γ_{wp}, γ_{wn}) and transconductance gain error (α).

Non – ideal mathematical model of VDCC can be define as:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{wp} \\ 0 & 0 & 0 & -\gamma_{wn} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

$$I_Z = \alpha g_m (V_P - V_N)$$

$$V_X = \beta V_Z$$

$$I_{WP} = \gamma_{wp} I_X$$

$$I_{WN} = -\gamma_{wn} I_X$$

On analysing circuit of oscillator circuit as shown in Fig. 8.1 considering non-ideal mathematical model of VDCC we obtain characteristic equation as:

$$s^2 + s\frac{1}{C_2\beta_1\beta_2}\left(\frac{\beta_1\gamma_{Wn2}}{R_2} - \beta_1\beta_2\alpha_2 g_{m2}\right) + \cdots \quad \ldots + \frac{g_{m1}\alpha_1\gamma_{Wn1}}{R_1C_1C_2\beta_1} = 0 \qquad \ldots 8.4$$

From equation 8.4 we obtain CO and FO as follows:

CO: $$\frac{\beta_1\gamma_{Wn2}}{R_2} - \beta_1\beta_2\alpha_2 g_{m2} \leq 0 \qquad \ldots 8.5$$

FO: $$\omega_0 = \sqrt{\frac{g_{m1}\alpha_1\gamma_{Wn1}}{R_1C_1C_2\beta_1}} \qquad \ldots 8.6$$

From equation 8.5 and 8.6 , it is noted that even under non-ideal conditions CO and FO are independent tunable as well. CO is tuned by g_{m2} or β_2 or $\beta_1$or γ_{Wn2} whereas FO is tuable by α_1 or g_{m1} or γ_{Wn2} , it is conclude from this that there is good non ideal behaviour of presented oscillator.

8.4 Simulation and Results

The passive component value is set to $C_1 = C_2 = 0.01$nf, $R_1 = 5$ K, and $R_2 = 3.65$K. Figures 8.3 and 8.4 display simulated oscillator output response in voltage mode and current mode respectively. Output spectrum of voltages V_1 and V_2 is shown in Fig. 8.5, from which we conclude frequency of oscillation is equals to 328.015 KHz.

Table 8.1

Transistors	**W/L(μm)**
M_1-M_4	**3.6/1.8**
M_5-M_6	**7.2/1.8**
M_7-M_8	**2.4/1.8**
M_9-M_{10}	**3.06/0.72**
M_{11}-M_{12}	**9/0.72**
M_{13}-M_{17}	**14.4/0.72**
M_{18}-M_{22}	**0.72/0.72**

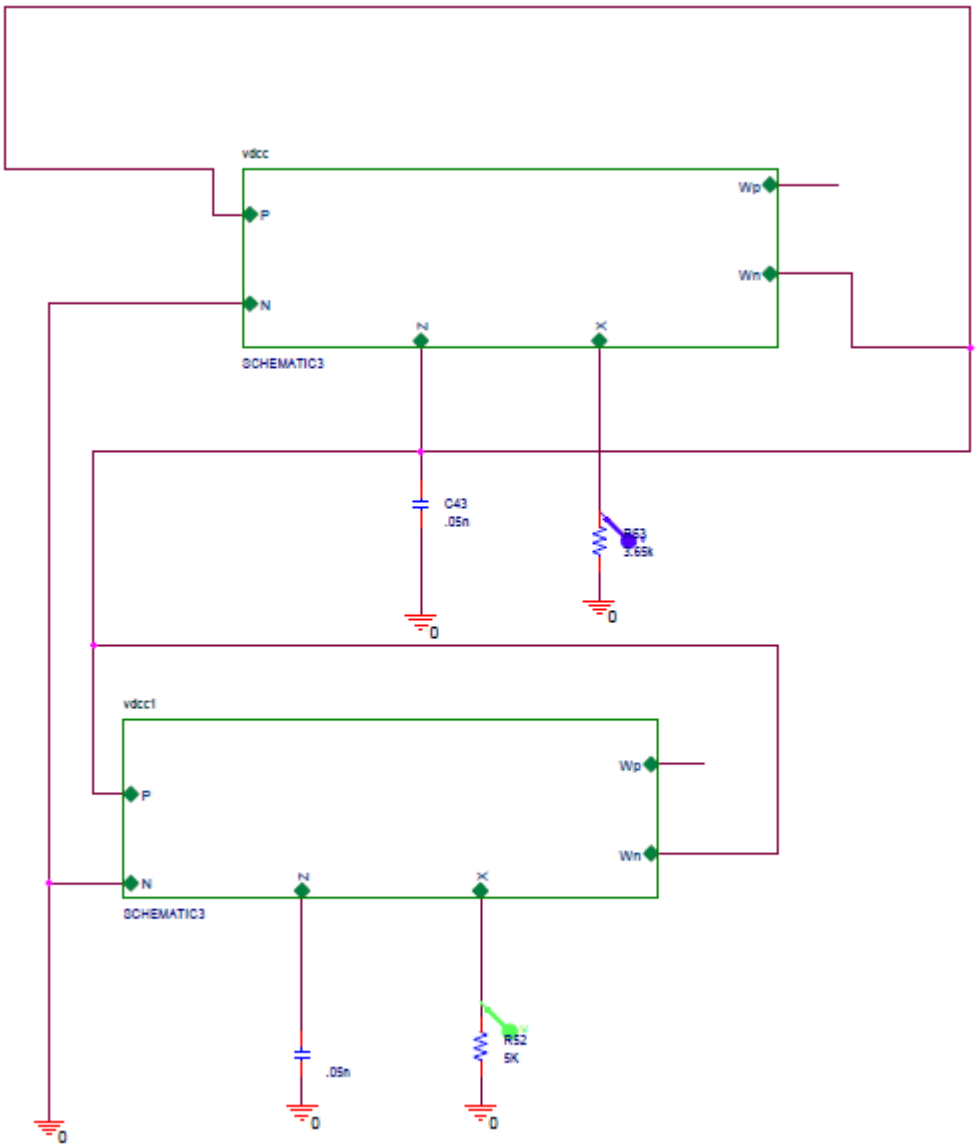
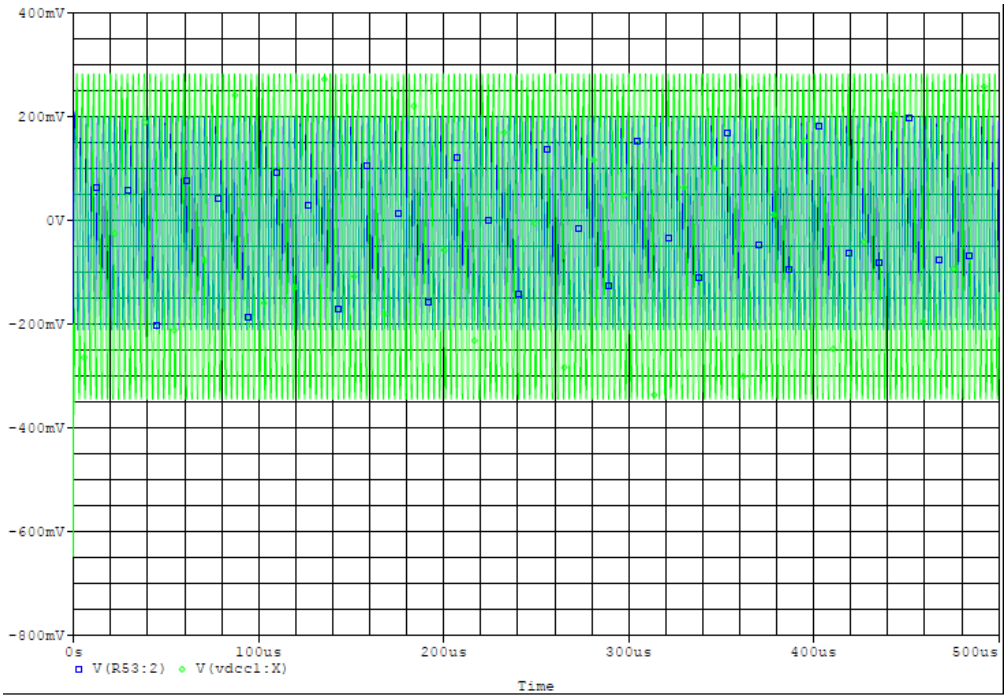
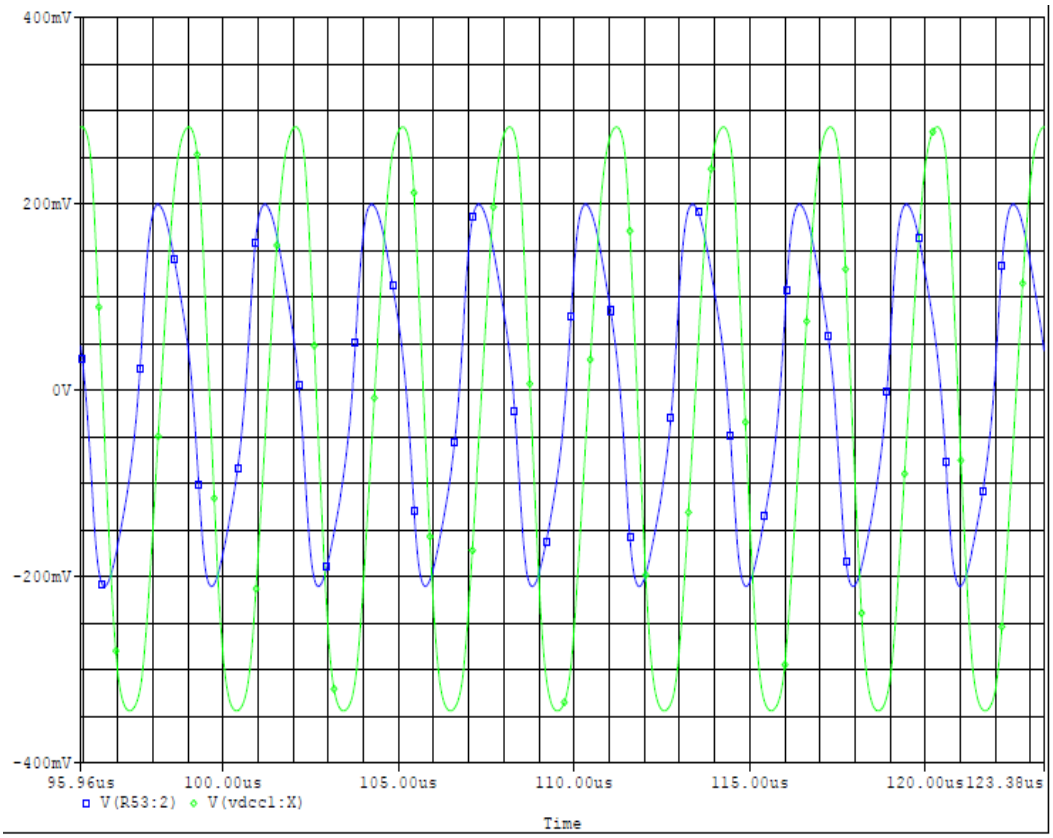


Fig 8.2 Schematic of dual mode quadrature sinusoidal oscillator [46]

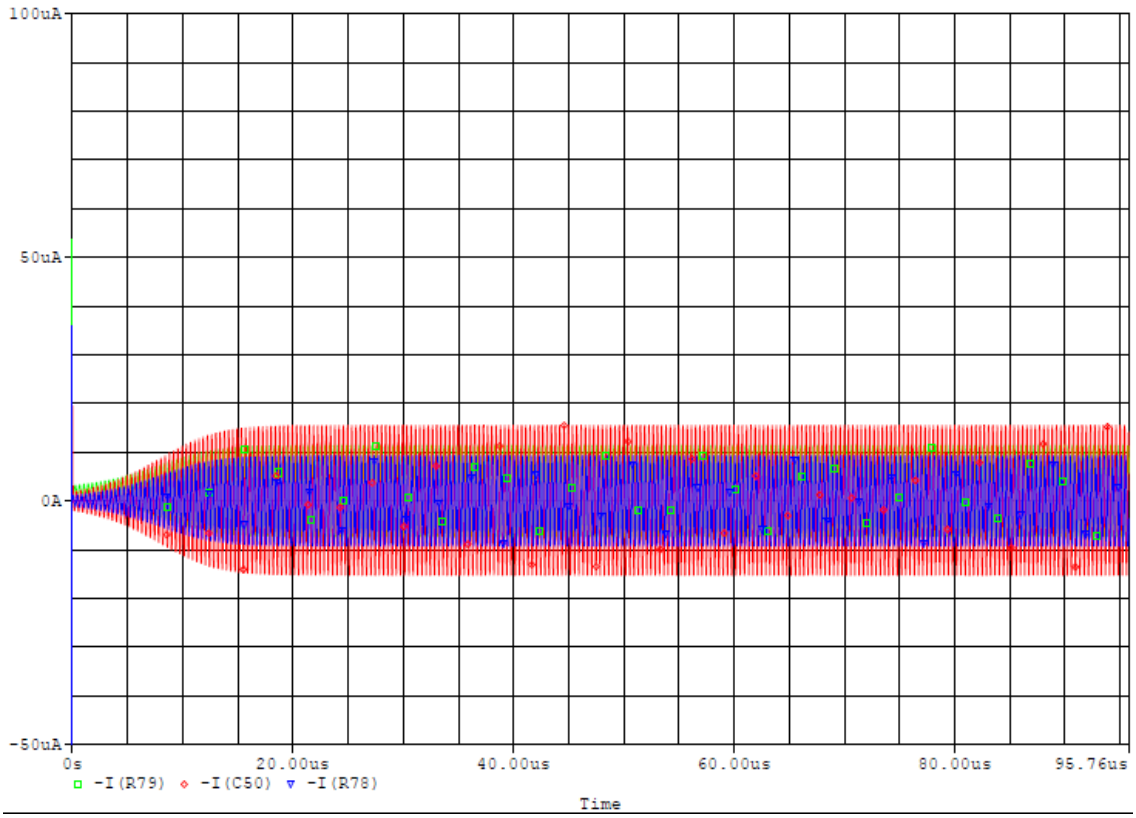


(a)

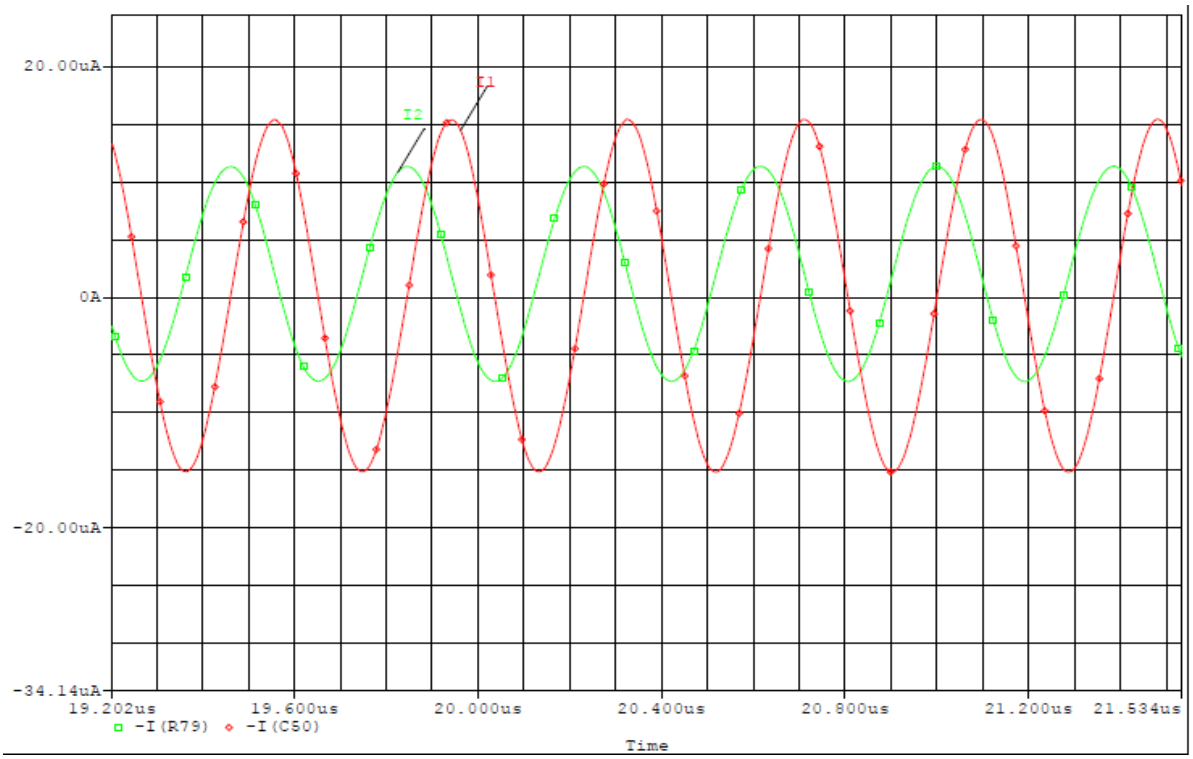


(b)

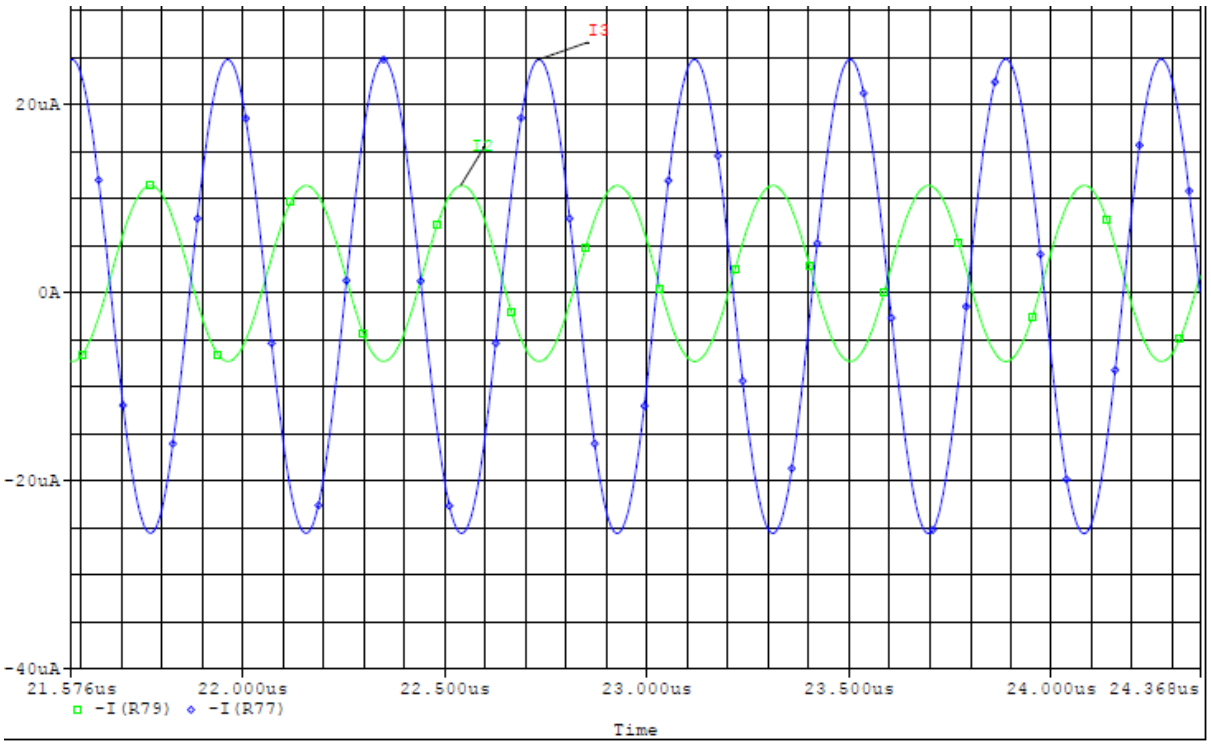
Fig 8.3 (a) Output of transient between V_1 and V_2 (b) Output of steady state response betweenV_1 and V_2


100uA
50uA
0A
-50uA
0s
20.00us
40.00us
60.00us
80.00us
95.76us
-I(R79)
-I(C50)
-I(R78)
Time

(a)


20.00uA
0A
-20.00uA
-34.14uA
I2
C1
19.202us
19.600us
20.000us
20.400us
20.800us
21.200us
21.534us
-I(R79)
-I(C50)
Time

(b)



(c)

Fig 8.4(a) Output of transient of I_1, I_2 and I_3 (b) Output of steady state response of I_1 and I_2 (c) Output of steady state response of I_2 and I_3

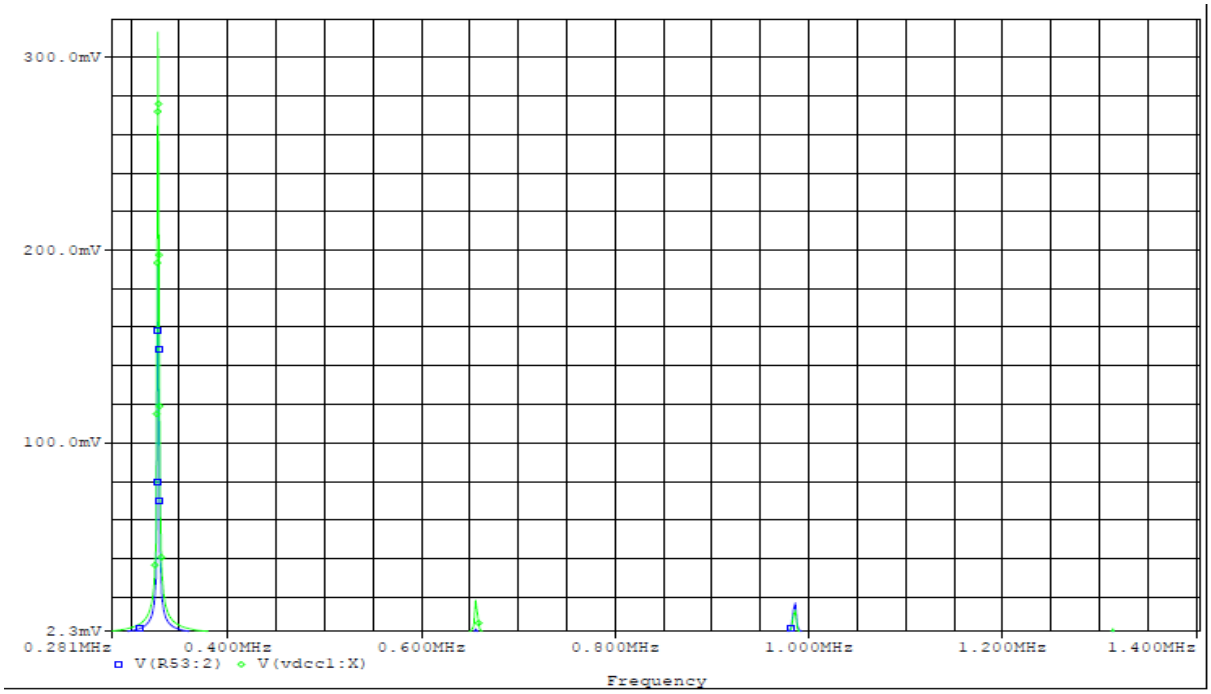


Fig 8.5 Output spectrum of voltage V_1 and V_2

CHAPTER 9

Quadrature Sinusoidal Oscillator Using VDCCs

9.1. Introduction

A quadrature sinusoidal oscillator (QSO) circuit is a circuit that provides 90^0 phase difference in two sinusoidal waveforms and has several applications in measurement systems, communication, instrumentation, and control systems [52]. They are used in measuring devices in vector generators or selective voltmeters and these oscillators are used in quadrature mixers, single-side generators and direct conversion receivers in communication systems [53].

To make quadratic sinusoidal quadratic oscillator I used the voltage differencing current conveyor (VDCC).

9.2. VDCC based quadrature sinusoidal oscillator

Figure 9.1 displays the proposed oscillator quadrature circuit using VDCCs. This consists of two parallel connecting VDCCs along with three resistors and two capacitors. All passive components are grounded which is the key advantage of this proposed circuit of oscillators.

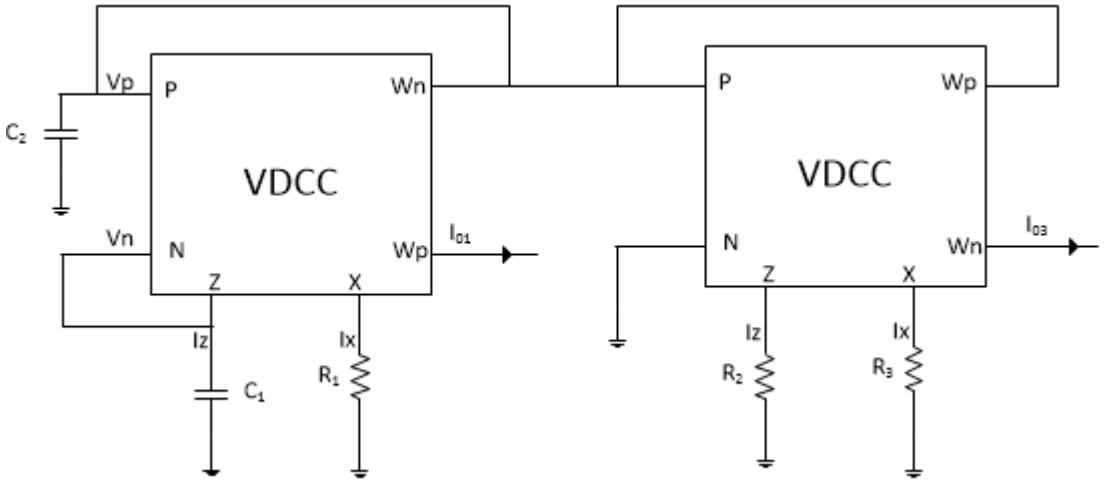


Fig 9.1 VDCC based proposed quadratic oscillator

Analysis of the configuration as shown in figure 2 which gives the following equation of characteristic.

(CE):

$$S^2C_1C_2R_1R_3 + S(g_{m1}C_2R_1R_3 - g_{m2}C_1R_1R_3) + g_{m1}R_3 - g_{m1}g_{m2}R_1R_2 = 0 \quad \ldots(9.2)$$

The oscillation condition and the oscillation of frequency are defined from equation (9.2) as:

CO:

$$g_{m1} <= \frac{g_{m2}C_1R_2}{C_2R_3} \quad \ldots(9.3)$$

FO:

$$\omega_0 = \sqrt{\frac{g_{m1}R_3 - g_{m1}g_{m2}R_1R_2}{C_1C_2R_1R_3}} \quad \ldots(9.4)$$

We conclude from equation (9.3) and (9.4), that oscillation frequency can be tuned by R_1 and oscillation condition can be adjusted by the value of R_2 and R_3.

Now, we obtain the relationship between current I_{01} and I_{02} as follows for quadrature oscillator design:

$$\frac{I_{01}}{I_{02}} = \frac{1}{SC_1R_1} \quad \ldots(9.5)$$

Under sinusoidal steady state :

$$\frac{I_{01}}{I_{02}} = \frac{j}{\omega_0 C_1R_1} \quad \ldots(9.6)$$

We infer from equation (6) that the phase difference between current I_{01} and I_{02} is 90 degrees which means both are quadratic to each other. Thus we get a quadratic circuit of oscillator.

9.3. Simulation Results

To verify the presented oscillator in Fig 7.2, we have to designed and simulated VDCC in Fig 7.1 using CMOS TSMC 180nm technology [22] as shown in Fig 7.3. Aspect ratio of each transistor in CMOS VDCC is according to table 7.1 , supplied voltages as ±0.9 VDC, biasing currents I_{b1} is 42μA and I_{B2} is 100μA respectively, Hence the value of trans-conductance obtained is g_m=262.65μA/V. The value of the passive circuit component shown as C_1 =.09n, C_2 =.08n, R_1 =3K, R_2 =10K, R_3 = 10.05K in figure 9.1.

On PSPICE, the output waveform of transient and steady responses is shown in Figure 9.3(a) and (b) in voltage mode, and Figure 9.5(a) and (b) in current mode respectively. Figure 9.4 in voltage mode and Figure 9.6 in current mode show the output spectrum, where the generated wave frequency is 247.399KHz. These output waveforms confirm that the proposed oscillator circuit is valid. Current I_{01} and I_{02} generated transient and steady waveform, shown in figures 9.7(a) and (b), shows that the proposed oscillator is a quadratic oscillator.

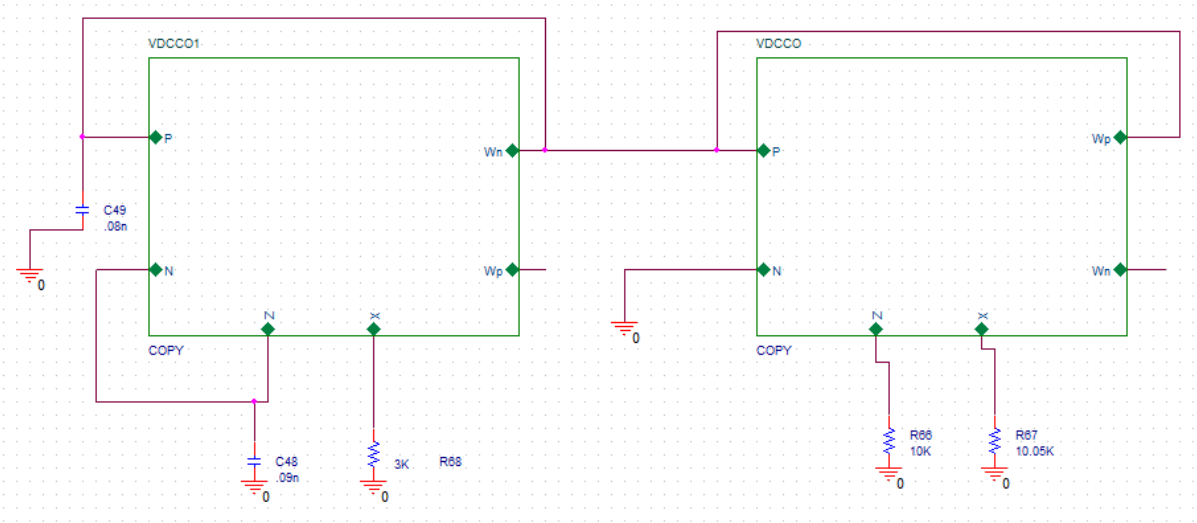
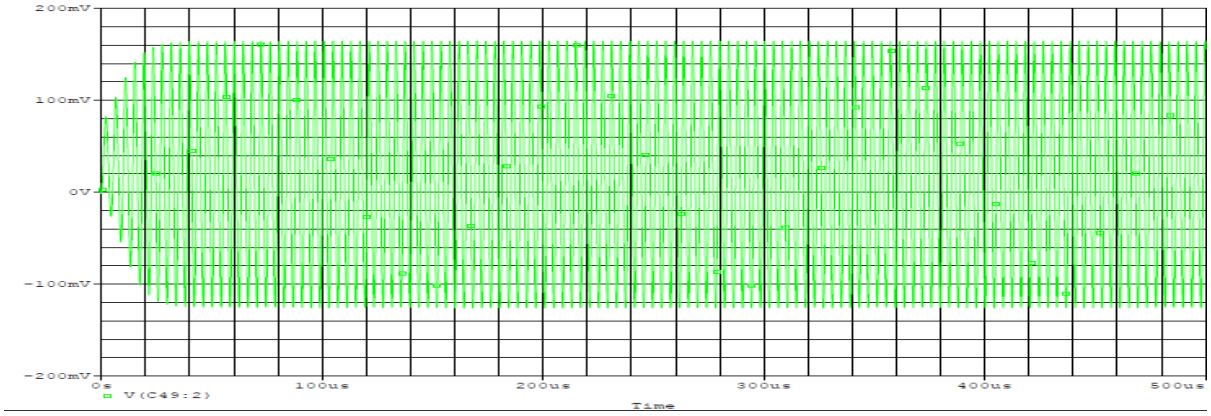
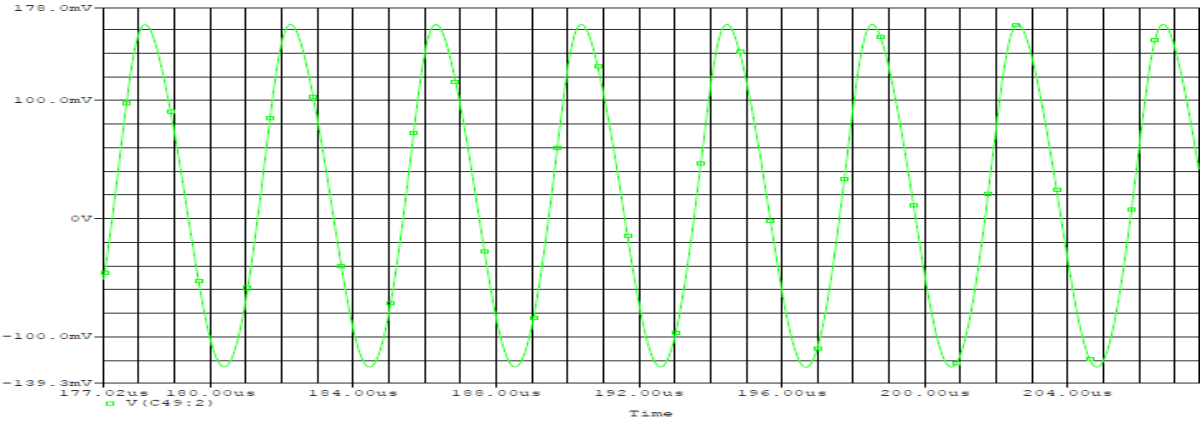


Fig 9.2 Schematic of quadrature sinusoidal oscillator



(a)



(b)

Fig. 9.3 (a) Transient output waveform (b) Steady state response of the output at feedback (Voltage mode)

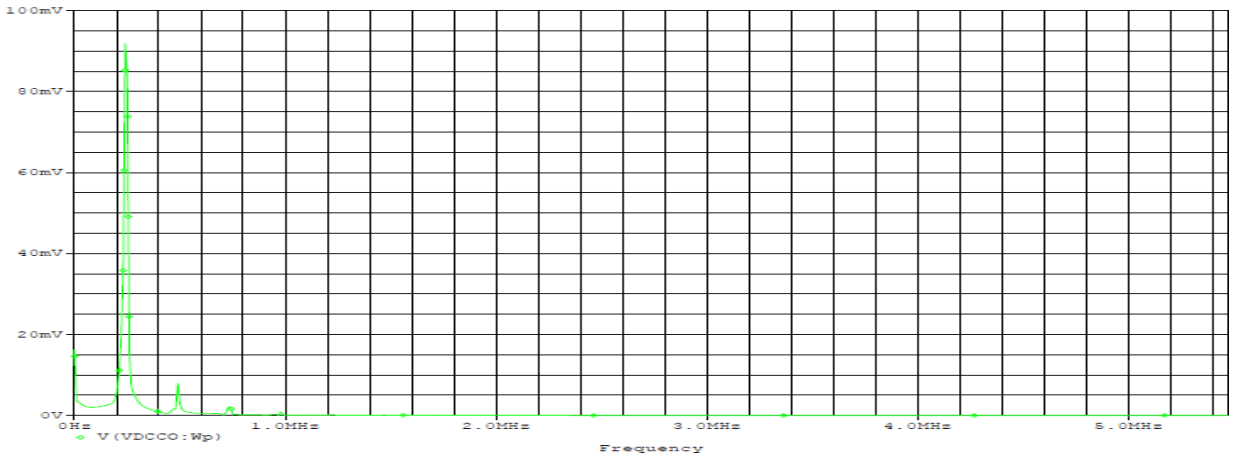


Fig. 9.4 Simulation result of the output spectrum (Voltage mode)

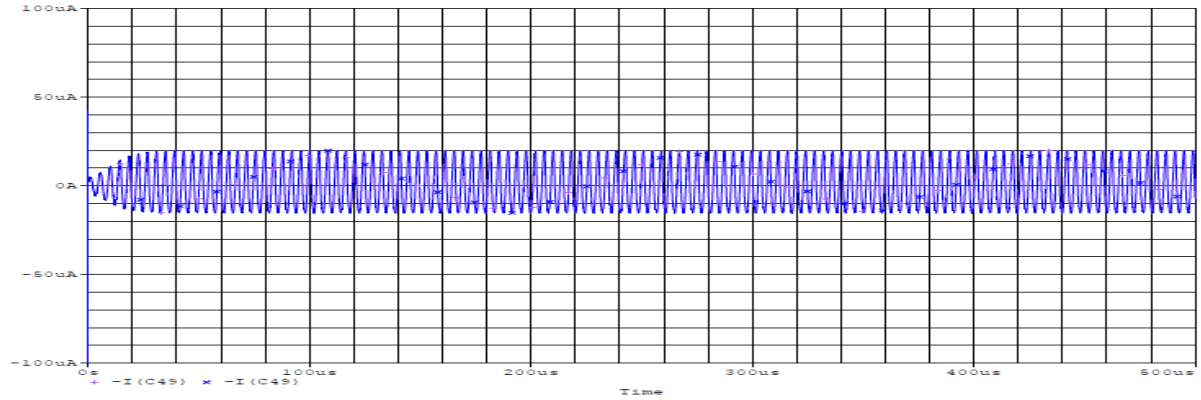


Fig. 9.5. Transient output waveform (Current mode)

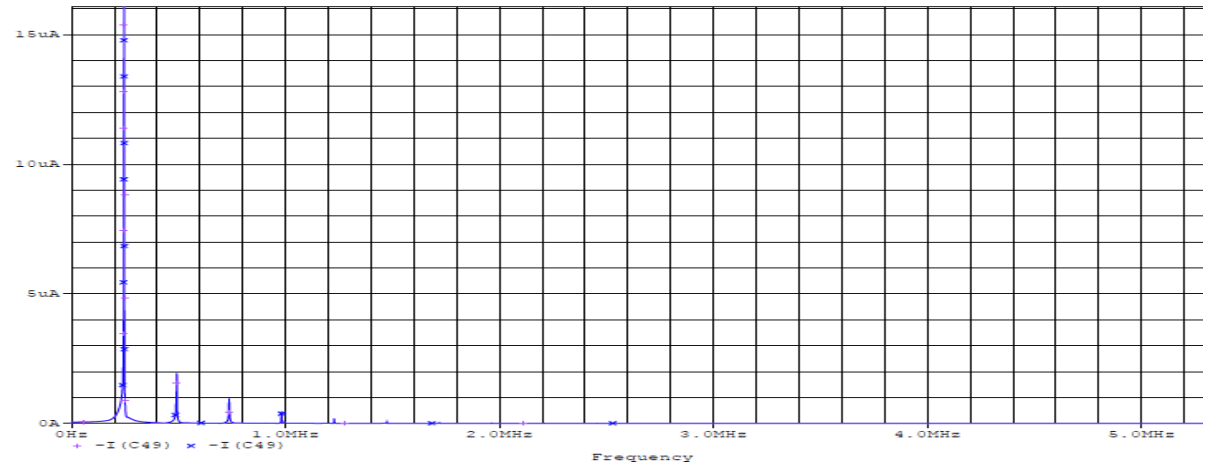
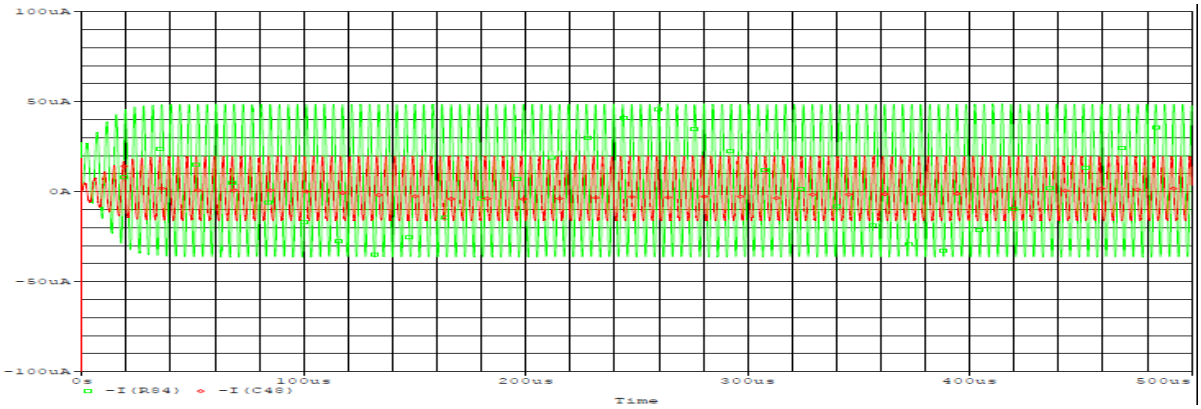
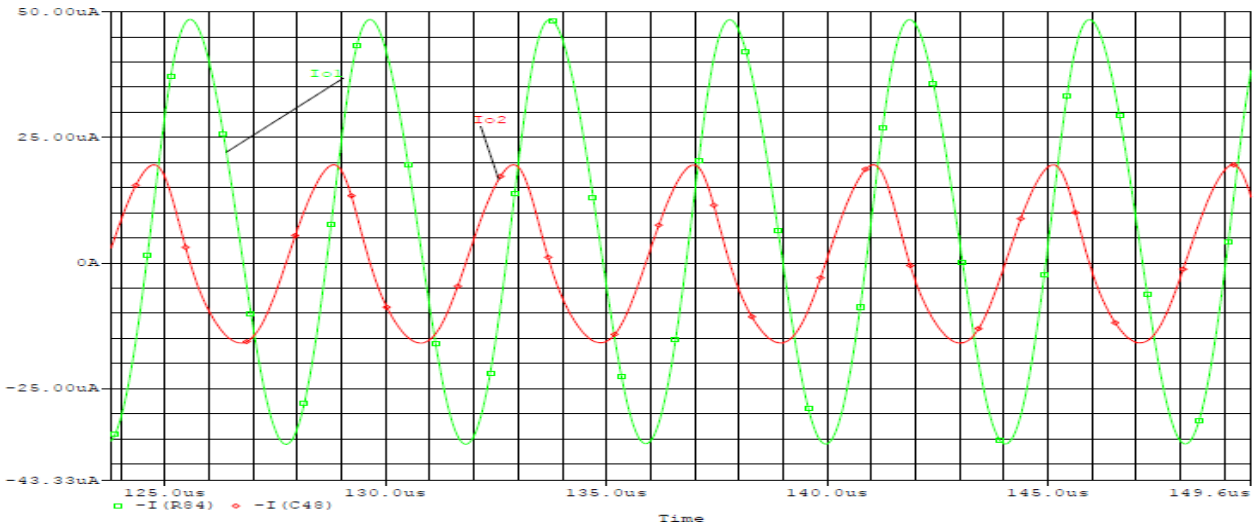


Fig. 9.6. Simulation result of the output spectrum (Current mode)



(a)



(b)

Fig. 9.7. (a) Transient output waveform, (b) Steady state response of the current I_{01} and I_{02}.

Conclusion

VDCC is emerging as a robust and versatile active building block in analog circuit design, among many active building blocks used in the processing of analog signal.

VDCC-based grounded and floating inductance simulator, using third-order High Pass Butterworth filter design and fourth-order Low Pass filter design. All four circuits are successfully studied. The circuit operation is verified by simulation with PSICE.

A grounded capacity multiplier circuit based on VDCC has been shown. This circuit can multiply a grounded capacitance through tuning factor, there is no requirement for any conditions that fit. It also offers non-ideal behaviour under undeviated conditions. Simulations under PSPICE simulation shall check the operation of the presented multiplier circuit.

Multiplier circuit based on VDCC grounded impedance with electronic or resistive scaling presented. This circuit either raises or scales down the values of any standard grounded impedance by electronic or grounded resistance variation. There is no requirement for any conditions that fit. Under non optimal conditions the operation of the circuit remains the same. Simulations under PSPICE simulation verify the workings of the developed multiplier.

Using one VDCC a universal biquadratic filter is presented consisting of three grounded passive components, since they are all grounded it is easy to integrate. There is orthogonal parameter (Q & ω_0) control and low passive and active sensitivity of both parameters. Results of PSPICE simulation verify the functioning of the presented circuit.

It presents a novel configuration of the sinusoidal oscillator using single VDCC with 90^0 phase difference. This oscillator circuit provides waveform quadrature voltage with no additional phase shifter circuit required. This consists only of grounded elements, and is suitable for IC technology. Oscillation frequency can be electronically tuned. Circuit performance is verified through PSPICE simulations.

A new configuration utilized grounded elements that make it suitable for monolithic integration. In addition to the dual mode quadrature oscillator, the presented circuit has many

advantages, such as independent resistivity and electronic tuning regulation of FO and CO, low active or passive responsiveness, strong frequency stability and evasion Simulations under PSPICE simulation check the workings of the built oscillator.

Using VDCC a new sinusoidal oscillator quadrature (QSO) circuit was introduced. The proposed circuit employs five passive ground components (three grounded resistors and two grounded condensers). CO and FO are mutually independent. PSPICE simulations have confirmed performance of the proposed configuration.

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