ANALYSIS OF DIFFERENT POWER FACTOR CORRECTED CONVERTERS

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CANDIDATE'S DECLARATION

I hereby certify that the workcontained herein Major Project-II entitled "ANALYSIS OF DIFFERENT POWER FACTOR CORRECTED CONVERTERS" in fulfilment of the requirement for the award of the degree of Master of Technology in Power System and submitted to the Electrical Engineering department, Delhi Technological University, Delhi, is a genuine record of my own work which is carried out under supervision of Asst. Prof. Saurabh Mishra and Asst. Prof. Himanshu Singh during the period of July 2021 to May 2023.

I have not submitted the information contained in this report for any other award of degree or to any other Institute/University.

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CERTIFICATE

I hereby certify that the project Dissertation titled **"ANALYSIS OF DIFFERENT POWER FACTOR CORRECTED CONVERTERS"** which is submitted by Sanjeev Sharma, Roll No. 2K21/PES/13, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This thesis presents a thorough examination of power factor corrected converters, with a specific focus on five distinct topologies: Boost PFC Converter, ILDB PFC Converter, SBBPFC, BLSB PFC Converter, and TTMPB PFC Converter. The primary aim of this study is to assess and compare the performance of these converters in relation to power factor correction, efficiency, and other relevant parameters. The initial portion of the thesis provides an overview of power factor correction techniques, emphasizing the significance of achieving a high-power factor in modern power electronic systems. It discusses the limitations of conventional rectifiers and emphasizes the necessity for PFC converters to adhere to regulatory standards and enhance overall system efficiency.

Finding ways to enhance the input current (I_{in}) waveform while preventing phase displacement has occupied a significant portion of power electronics research over the past two decades. Choosing the two most important 1- phase Power Factor Correction (PFC) topologies is the thesis's main goal. The Boost PFC Converter and the ILDB PFC converter are the investigated topology under the performance. In Simulink/MATLAB, the all investigated topologies performances are simulated. Additionally offered are efficiency evaluation and loss analysis. The simulation outcomes show that the BPFC converter topology with interleaved boost exhibits a somewhat greater efficiency. This innovative interleaving method optimizes CRM for each step. accurate 180-degree phase shift and natural current sharing. The subsequent sections concentrate on each individual converter topology. Each topology is elaborated upon in detail, encompassing its operating principle, control strategy, and critical design considerations. Mathematical models for each converter are derived, and simulation models are constructed to analyse their steady-state and dynamic characteristics. The simulation outcomes are validated through experimental tests conducted on prototype hardware.

A comparative analysis is carried out to evaluate the performance of the various PFC converter topologies. Parameters such as power factor, total harmonic distortion (THD), efficiency, and component stresses are considered in the comparison. Furthermore, the impact of load conditions and input voltage variations on converter performance is

investigated. Through the analysis and comparison, the strengths and limitations of each converter topology are identified. The findings provide valuable insights into the suitability of these converters for diverse applications, while taking into account factors such as cost, complexity, efficiency, and power density.

Lastly, recommendations are provided to aid in the selection of the most appropriate PFC converter topology based on specific application requirements. This study contributes to the existing knowledge by delivering a comprehensive analysis and comparison of five distinct PFC converter topologies, thereby facilitating well-informed decision-making in the design and implementation of power factor correction solution.

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CHAPTER 1

1 INTRODUCTION

For pure sinusoidal waveforms, Power factor is defined as the ratio of the apparent power in the circuit supplied by to the active power flowing to the load

$$Powerfactor = \frac{realpower}{reactivepower} \tag{1.1}$$

which is a dimensionless number between 0 and 1

pfc is a technique used to eliminate input current harmonics and line current (I_L) sinusoidal and in phase with the line voltage in order to meet the standard. Additionally, PFC is a method of reducing the negative impacts of electrical loads that produce power factors below unity ($pf \leq 1$). The perceived/apparent power given to the load is more than the actual power that the load absorbs when its power factor (PF) value is below unity.

In theory, *pf* should be $\cos\varphi$, but in fact, nonlinear loads cause the source current to be no sinusoidal, therefore theoretically *pf* is:

$$PF = K_D \cos\varphi \tag{1.2}$$

where $\cos\varphi$ is the line voltage ($V_{L)}$ and current's displacement factor. and $K_D = \frac{I_{1\cdot rms}}{I_{rms}}$ is called as the distortion factor which provides information on the harmonic limit of the fundamental current.

moreover, the mathematical relationship between the distortion factor and THD;

$$K_D = \frac{1}{\sqrt{1+THD^2}} \tag{1.3}$$

Where, THD is the Total harmonics distortion and we can calculate THD with the help of below condition,

$$THD = \frac{\sqrt{\sum_{j=2}^{\infty} I_{nrms}^2}}{I_{1rms}} \tag{1.4}$$

With the exception of the DBR, passive PFC uses entirely passive components to enhance the line current's form[1]-[2]. It should be clear that the output voltage cannot be

controllable. Despite being straightforward, passive PFC converters have drawbacks that prevent them from being used in industrial settings fig. 1.1 shows the importance of power factor in today's world. These drawbacks include poor dynamic response, a lack of voltage regulation, input current shapes that rely on the load, and reduced power factor.

In active PFC, active switches are used with reactive components to improve line current shaping efficiency and produce adjustable output voltage.

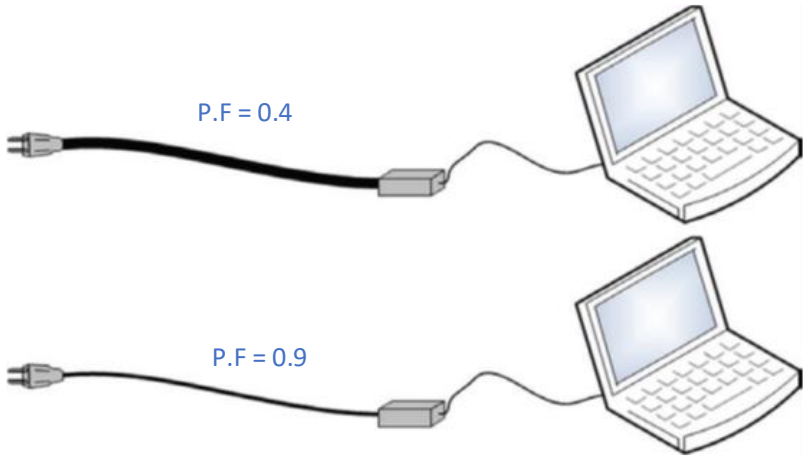


Fig. 1.1 Importance of Power Factor

The APFC solutions are further divided into two types based on switching frequency: *In low-frequency* switching occurs at low-order harmonics of the line frequency in an active PFC and is synchronized to the line voltage.[1]

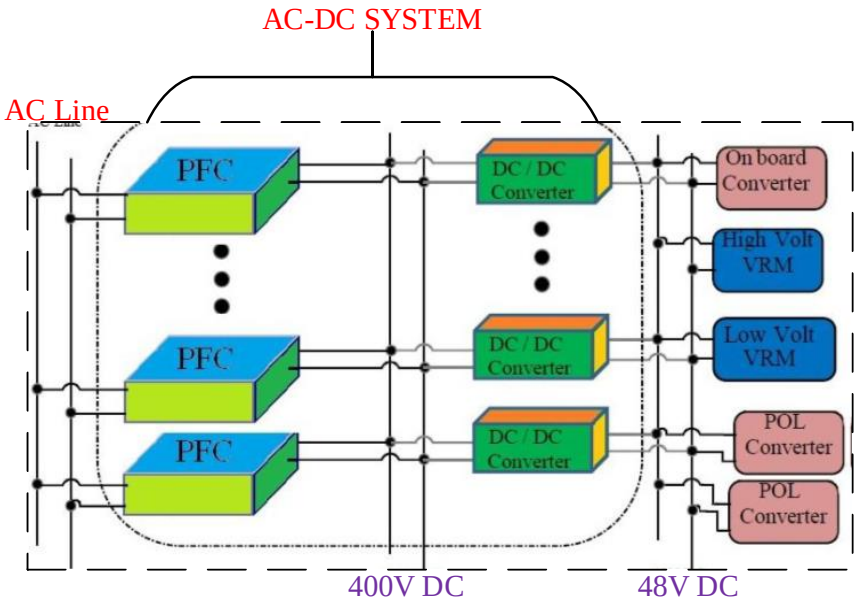


Fig. 1.2 Schematic of PFC for Battery charging

Power factor adjustment is a crucial component of effective energy management that can have a positive impact on businesses, homes, and the environment fig. 1.2 shows the schematic of PFC for battery charging. The following are some of the most significant justifications for the significance of power factor correction:

Enhancing electrical system's energy efficiency is one of the key benefits of power factor adjustment. Low power factor indicates that a system is consuming more energy than is required to complete a task, which increases energy costs and decreases efficiency. Power factor correction entails the installation of capacitors or other devices. Power factor adjustment can dramatically lower energy expenditures and encourage the usage of sustainable energy by minimising wasted energy[2]. Greater Equipment Lifespan: When running at a low power factor, electrical equipment, including motors, transformers, and other devices, might experience decreased efficiency and greater wear and tear. By lessening the stress brought on by reactive loads, power factor adjustment can help to increase the equipment's lifespan. As a result, electrical systems may operate more reliably and with lower maintenance costs.

Reduced Power Interruptions: Voltage fluctuations can occur in electrical systems with a low power factor, which can cause power outages, equipment damage, and other issues. Power factor correction works to increase the power factor, which helps to stabilise voltage levels and lessen the likelihood of power outages. Regulation Compliance: In many nations, companies are required to keep a specific power factor in order to follow rules and stay out of trouble. Businesses can comply with these standards and avoid expensive fines by using power factor correction. Benefits for the Environment: By lowering energy waste and increasing efficiency, power factor correction can assist lower greenhouse gas emissions and encourage the use of sustainable energy. This can help with efforts to prevent climate change and lessen the negative effects of human activity on the environment.

In general, power factor adjustment is a crucial component of effective energy management that can have a positive impact on the economy, the environment, and homes and companies. Power factor correction can decrease costs, boost output, and protect the environment by enhancing energy efficiency, increasing the lifespan of electrical equipment, minimising power outages, adhering to laws, and supporting sustainable energy use

1.1 Motivation

Almost all electronic devices have different power ratings, and the incredible need for power sources for such devices presents a challenging problem to the power engineer. Regulated DC bus bar voltage is a concept introduced by the AC-DC APFC converters system. With regard to power distribution and management, this satisfies the need for greater currents as well as the dynamic properties of AC-DC systems. It is too humble when taking into account high efficiency, high power density, fast dynamic reaction, etc. for specialised applications, such as power supplies for telecom and computer servers. However, it is conceivable to transfer electrical power from the power grid to the consumer end at a cheap cost and with high efficiency. given that Power Electronic Converters are created with cutting-edge, appropriate control methods.

Due to the intensive switching operations, the magnetic components used in converters are getting smaller. This translates into advantages in power electronics' price, size, and performance, and as a result, these devices are more common in modern commercial, industrial, military, residential, and aerospace settings. Galvanic isolation installation by DPS is crucial for protection and the attainment of flexible system configuration. All the aforementioned perfections can be accomplished by adding active PFC converters into DPS. The most practical three-phase PFC converter is the traditional hard-switched PWM three-phase boost rectifier; however, all of the known soft-switching approaches are cumbersome and ineffective. Significant turn-on losses are brought on by the diode reverse recovery issue, and significant turn-off losses are brought on by the slow devices' current tail issues, such as the IGBT, which is recommended for three-phase high power applications. These motivations constitute the basis of this dissertation's goal, which is to create a number of high-performance PFC approaches to outperform the current ones in the aforementioned areas. The active PFC converters for DPS can perform better thanks to ongoing research to provide improved efficiency, quick dynamic response, and high-power inflation with strict regulatory regulations. In this thesis study, some control approaches and a straightforward elongation PWM technique are examined. And the research work is used in AC-DC PFC.

CHAPTER 2

2 LITERATURE REVIEW

2.1 Introduction

Switch-Mode Power Converters (SMPC) modelling and analysis utilising averaged state-space equations. State space averaged equations have been introduced, which is thought to be a significant step forward for SMPCs. The strategy let the designers to explain the behaviour of the switching power converter using a single linear circuit model. Regardless of the original converter topology, the circuit model's topology is the same. To allow different converter topologies, just the model element values are altered. [3]

In 1986 saw the publication of a NASA-sponsored academic research report on the use of SMPC to adjust for low-quality input current waveforms of capacitive input filters off-line power supply and is listed as reference [4].

current shaping and power factor correction (PFC) for off-line power converters are covered by a number of U.S. patents. The input current is detected, integrated, and contrasted with an erroneous voltage produced from the Boost Converter's output. Through a separate driver stage, the comparator's output is gated to the Boost Switch. The rectified sinusoidal AC voltage envelope automatically follows the chopped input current envelope. The patent stated that the increased PF can surpass 95% thanks to additional duty cycle management Boost Switch. For chopped input waveform's switching frequency components to be removed, a line filter is required.

Following a brief discussion of the benefits and drawbacks of each control circuit, the "Regulation Band" control circuit was suggested as the inner current controller.

The advantage of employing these converters is that current shaping can be accomplished without loop. The advantage of employing these converters is that current shaping can be accomplished without an explicit current control loop. Voltage regulation still depends on the DC voltage control loop. Since each switching cycle requires the inductor current to vary from zero to its greatest peak, the discontinuous conduction mode is not preferred for high power applications. For these types of converters, the current distortion is extremely significant. This behaviour is the same as the CCM boost converter's delay angle effect with average current controller.

2.2 Boost PFC Converter

The boost PFC converter topology uses a dedicated diode bridge to rectify the AC input voltage to DC, which is then followed by the boost section. Because of its step-up conversion ratio, the input voltage's amplitude VAC is never greater than the output voltage V_o. MATLAB/Simulink was used to implement the Boost PFC Converter topology and its controller on hardware. The controller, a component of the software implementation, seeks to make the converter input current follow the sinusoidal waveform of the input voltage, regardless of the output power. It will not be discussed here because it is not the focus of this study, although details may be found in [5].

With some ripple at the output terminal voltage, the boost converter keeps the output voltage constant However, as the power level rises, the diode-bridge losses increase, decreasing the converter's efficiency. At high power levels, it also has a heat dissipation issue. The power range is constrained for higher power levels by the increase in inductor size. Thermal management, power losses, and Conduction losses, issues are the drawbacks of this design. Every switching cycle, the current flows through three semiconductor devices—two diodes in series with diode D or switch S1—resulting in conduction losses. Because of the greater voltage drops across the employed diodes when it is used at low loads and the resulting need for thermal management of the diode bridge when it is operated at higher loads, it is less efficient.

Compared to other topologies, this converter topology has a bigger input current ripple, but it is simpler to operate. The inductor is operating in continuous conduction mode, and the average current control mechanism is being used Which is followed by a current controller which control the inductor current and also maintain the sinusoidal waveshape and finally the output is given to the PWM block and which is connected to the Gate Terminal of the MOSFET. This is the complete control block diagram of a PFC Boost Converter, Here First we need to detect the value of AC input Voltage.

2.3 Interleaved Boost PFC Converter

Paralleled semiconductors are advantageous for the boost interleaved converter. Additionally, it lowers the output capacitor's high frequency ripple, although the input diode bridge rectifiers' heat management remains a challenge. [6]

The reduction in inductor magnetic volume is made possible by the cancellation of inductor ripple current. The cancellation of inductor ripple current allows for a reduction in the magnetic volume of the inductor. However, a decrease in magnetic volume does not directly

result from a decrease in energy storage [5]-[6]. The boost interleaved PFC converter topology is presented in Fig 2. The AC input voltage is rectified to DC using a specialised diode bridge, which is followed by two parallel Boost PFC Converters that operate 180° out of phase.

The two input inductor currents add up to form the input current. The inductors' ripple currents tend to cancel each other out since they are out of phase, which lowers the input ripple current brought on by the boost switching action. The phase shift for each branch equals 360°/N, if there are N parallel branches. Paralleled semiconductors are advantageous in the boost interleaved PFC converter. The output capacitor high frequency ripple is decreased because the input current is the total of two inductor currents, however the input diode bridge rectifiers' heat management remains an issue.

A reference voltage is used to compare the measured DC bus. For zero error DC bus voltage regulation, the resulting voltage error is then sent into a Proportion Integral voltage controller. The inner controller receives the controller's output, which is the amplitude of the reference supply current. Additionally, in order to mimic the behaviour of a pure resistor. For this, an analogy multiplier is employed. The I_{ref} is then deducted from the detected inductance current, and the current is subsequently limited.

Finally, this converter has a low high-frequency ripple output capacitor. The very high localised loss and subsequent heat management issue for the input diode bridge rectifiers, as with the single PFC boost, are this topology's biggest drawbacks.

2.4 Semi-Bridgeless Boost PFC Converter

These diodes have low conduction losses because the current does not always return through them. This happens because the inductors have low impedance at line frequency, which causes a significant amount of the current to flow through the MOSFET intrinsic body diode [7].

The floating input line issue in relation to the PFC stage ground is likewise solved by the semi-bridgeless architecture. The topology change makes it possible to sense input voltage using a series of straightforward voltage dividers.

The CM-mode noise weakness of Bridgeless PFC is overcome by Semi-Bridgeless PFC. Due to this; SBBLB PFC requires more components than BLB PFC Semi-Bridgeless PFC. As a result, the capacitor's voltage ripple and the switch's conducting current can be cut in half.

For constant switching frequency, One-Cycle Control [8] is a novel nonlinear control approach. The integration reset approach is another name for it. The externally resettable integrator is crucial to the One-Cycle Control approach.

One of control techniques for boosting PF and reducing distortion in PFC converters is average current mode control (ACMC) [9]. The reasons it is so well-liked are that it performs well and is simple to comprehend. Using this method, I_L in a proportionate manner. the inductor current is detected, and the ensuing voltage drop is detected and amplified, with suitable switch management, rather than controlling it to maintain a constant Vo. To better comprehend the control technique, it is split into two loops: both of which can be used to provide PFC and voltage regulation.

This converter eliminates the issue with standard boost PFC's input rectifier diode bridge's heat control, but it increases EMI. [10]. Another drawback of this design is that the input line is floating with respect to the PFC ground, which prevents input voltage sensing without a low frequency transformer or an optical coupler.

2.5 Bridgeless Boost PFC Converter

Current passes in a series across two of the bridge diodes in the conventional boost PFC architecture. Only one diode is used in the bridgeless PFC design, and the return path is provided by MOSFET switches[2]. While current passes through two traditional boost design, it only passes through one diode in the bridge less PFC version, with the Power MO SFET serving as the return channel.

The gating signals are identical because connected[11]. For applications over 1 kW when power density and efficiency are crucial, it is a desirable choice. The input rectifier diode bridge's heat management issue is resolved by the BLSB converter, also referred to as the twin boost PFC converter, however it increases EMI [12]. This is due to bridgeless PFC's much larger; as a result, BLSB PFC produces substantially more (CM) noise than the Boost PFC design [13].

Operation of Bridge less PFC Boost Converter

There are four different ways that a bridgeless PFC boost converter can operate. While modes III and IV are subject to the negative half cycle of input voltage, modes I and II are subject to the +ve half cycle. The family of bridgeless boost converters is frequently utilised because it enables a significant reduction in conduction losses, increasing the converter structure's overall efficiency. [14].

2.6 Totem-Pole Boost PFC Converter

The fundamental BLB topology, which can significantly reduce conduction losses, When the switching frequency is raised, switches S1 and S2 experience large switching losses because they are operated in the hard-switching mode. Figure 4 depicts design of the BL Boost converter. By switching the locations of S1 and D2, it is a modified version of the BL Boost architecture depicted Due to the placement of the switches, this architecture is often referred to as totem-pole BL Boost (TPBLB). Due to the antiparallel diode's poor reverse recovery capability, the TPBLB architecture is generally suited for operating in discontinuous current mode (DCM) and /continuous current mode (CCM) boundaries [15]. A soft-switching BL Boost converter's fundamental design principle is to provide a bidirectional channel.

The components of the suggested TPBLB converter are two boost inductors L1 and L2, two IGBTs S1 and S2, an output capacitor Co, and a load resistor RL. Both +VE and -VE input cycles are symmetrically operated by the suggested TPBLB converter The proposed TPBLB converter is assumed to be operating in steady state, with L1 and L2 assumed expected.

Without using additional auxiliary switches, it is very to a BL Boost on the traditional BL Boost converter depicted in Fig. 1(a). This is as a result of the structure lacking the necessary bidirectional current flow for soft switching. The TPBLB architecture is an appropriate choice since it requires fewer components. Comparing the proposed TPBLB converter to previous soft-switching BL Boost rectifiers with high PF[16], the converter's overall component count is also decreased.

The TPBLB is made to work in ACMC while using CCM. There are two feedback loops on the controller. The I_{in} waveform is shaped into a sinusoidal shape using a current feedback loop current consider as the first loop while makes up the second loop. This loop is average value The suggested TPBLB converter uses a control strategy similar to other traditional PF correction (PFC) converters. When standard PFC converters, the proposed TPBLB converter's control technique differs in that it uses a phase detector [17].

CHAPTER 3

3 ANALYSIS OF BOOST PFC CONVERTER

3.1 Introduction

Modern power electronic systems must include Power Factor Correction (PFC) if they are to improve power quality, boost energy efficiency, and adhere to strict standards. The Boost PFC Converter is one of the most popular among all topology and highly used PFC topologies available today.

The boost converter and power factor correction control loop are integrated to operate the Boost PFC Converter. It regulates the output voltage to a desired level after rectifying the input AC voltage and shaping the current waveform to match the waveform of the input voltage. The Boost PFC Converter minimises reactive power flow and eliminates electrical losses, enhancing overall system efficiency by achieving high power factor and low harmonic distortion.

In this analysis, we investigate the characteristics and operation of the Boost PFC Converter, looking at its main parts, working ideas, and control schemes. We examine the fundamental ideas that underlie its capacity to improve power factor and attain high efficiency, while also addressing typical issues and constraints that arise in real-world applications. The basic operation and analysis of the Boost PFC Converter, its steady-state behaviour, small-signal modelling, control strategies including voltage-mode and current-mode control, and the effects of various load circumstances are only a few of the topics covered in the analysis [18].

In order to maximise converter performance, we will also go through crucial factors including duty cycle, inductor and capacitor choices, and feedback loop selection.

The analysis will also explore the suitability of the Boost PFC Converter for various applications and how it interacts with other power electronic circuits, as well as its benefits and drawbacks. In this article, we will discuss pertinent design factors like component stresses, efficiency trade-offs, and electromagnetic compatibility (EMC) standards.

In the end, the goal analysis gives readers a thorough the Boost PFC Converter and the knowledge they need to create, evaluate, and improve power factor correction systems. We can further enhance the effectiveness and efficiency of power electronic systems by

investigating its operational principles and constraints, which will help to create a more dependable and sustainable power infrastructure.

3.1.1 Loss Analysis

The power losses of rectifiers, diodes and magnetic components are estimated to examine the efficiency of topologies. Reverse-recovery loss and Conduction loss are taken into account when calculating the losses of diodes and rectifiers. An indication of conduction loss is (10)

$$P_{cond.(diode)} = V_F * I_F * D_{on} \tag{3.1}$$

Don is on duty, VF stands for forward voltage drop, and h stands for conduction current. Calculations are made using a triangle made up of the reverse maximum current Inn, the reverse breakdown voltage $V_{rev.}$ and the reverse recovery time t_{rr}. reverse-recovery loss P_{trr} like(11)

$$P_{trr(diode)} = \frac{t_{rr} * Irm * V_{rev.} * f_{sw}}{8} \tag{3.2}$$

Switch loss is calculated by taking into account conduction loss, switching loss, and anti-parallel diode loss. the switchover loss Psw expression (12)

$$P_{sw} = 0.5 * V_{out} * I_{rms} * \left(t_{c(on)} + t_{c(off)}\right) * f_{sw} \tag{3.3}$$

$t_{c(on)}$ is rise time, $t_{c(off)}$ is falling time, and Inns is current of switch. Conduction loss of switch is calculated by[19].

$$P_{cond.} = I_D^2 * R_{DS(on)} * D_{on} \tag{3.4}$$

3.2 Analysis of Boost PFC Converter

To convert the AC input voltage to DC, the Boost PFC Converter topology employs a diode bridge rectifier. It is followed by the section on boost converters. The voltage on output side Vo is always greater than input voltage's amplitude VAC because of the step-up conversion ratio. In order to create a sinusoidal reference for a current controller, we must first determine the value of the voltage. After that, Following the output being given to the PWM block, there is a voltage controller to control the output voltage, followed by a current controller to

control the inductive current and protect the sinusoidal waveform, and It is connected to the MOSFET's gate terminal.

The capacity of the storage inductor, the switching loss and reverse recovery time of the diode, which restrict switching frequencies from exceeding 100 kHz from being much increased,[17] are two restrictions that prevent power density from being significantly enhanced. This Interleaved connection is utilised to get around it.

The benefits of interleaving include the ability to largely reduce input and output current ripple while increasing switching efficiency without sacrificing effective current ripple frequency loss. Interleaved boost converters ripple can be reduced in comparison to boost, but they are more expensive and take up more space

3.2.1 Schematic of Boost PFC Converter

This switching converter works by routinely turning on and off an electrical switch. The output voltage is greater than the input voltage, hence it named as "boost converter."

Voltage and Current Relationships

Following assumption will be taken

a) Component are taken as ideal

b) The switch is closed for time DT and open for time (1-D) T during the switching period T.

c) Steady-state conditions exist.

d) The output voltage is maintained at voltage Vo and the capacitor is quite big.

The next step in the analysis is to look at the inductor voltage and current for both the closed and open states of the switch.

A popular topology in power electronics for achieving high power factor and enhancing energy efficiency in AC-DC power conversion applications is the Bst Power Factor Correction (PFC) Converter. Reduce harmonic distortion, and maintain a regulated output voltage, it combines the benefits of a boost converter with a power factor correction control loop[14].

The boost converter circuit as shown in fig. 3.1 which includes diode, an inductor a capacitor, and a high-frequency switch (usually a MOSFET or an IGBT), powers the Boost

PFC Converter. Following rectifying, the boost converter receives the input AC voltage. A larger output voltage than the input voltage is obtained as a result of the inductor, which stores energy during the period of switch-on. The diode stops current from returning to the source of input.

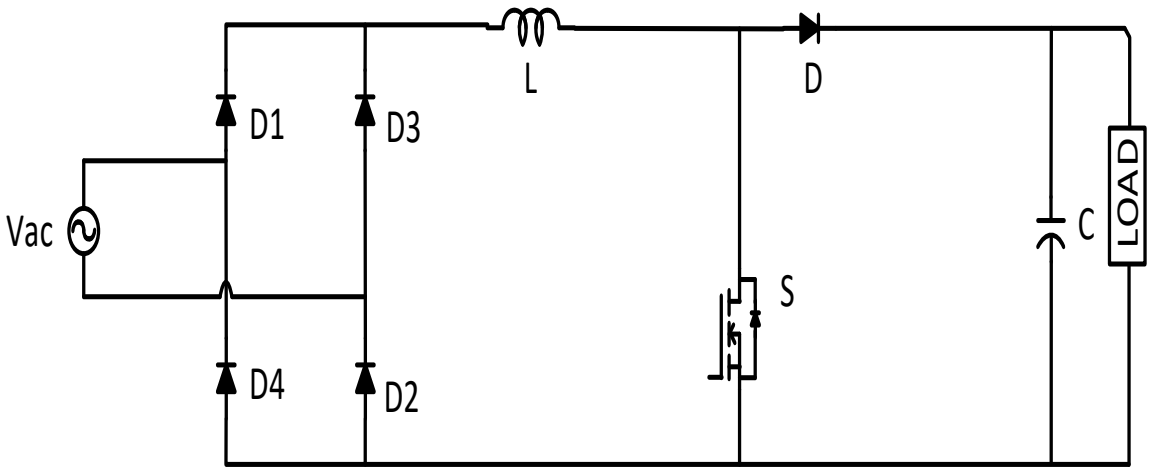


Fig. 3.1 Schematic of Boost PFC Converter

Through a control loop that modifies the duty cycle of the switch in response to the current value of the input voltage, the power factor correction functionality is accomplished. By ensuring that the input current waveform closely matches the input voltage waveform, this control loop lowers the reactive power component and raises power factor. The Boost PFC Converter lowers harmonic distortion and complies with power quality standards by modifying the input current waveform to be in-phase with the input voltage.

The Boost PFC Converter has a number of benefits. First of all, it attains a high-power factor, usually above 0.95, which lowers the amount of reactive power drawn from the grid and promotes more effective use of electrical power. The second benefit is that it offers galvanic isolation between the input and output, assuring safety and enabling voltage transformation if necessary. The Boost PFC Converter is appropriate for a variety of applications due to its wide input voltage range handling capabilities and controlled output voltage. The Boost PFC Converter is suited for a variety of applications since it can handle a wide range of input voltages and offers a controlled output voltage. Moreover, variables like switching losses, conduction losses, and the control approach chosen might have an impact on the converter's efficiency.

In conclusion, the boost converter and power factor correction control are combined in the popular power electronics topology known as the boost PFC Converter.

3.2.2 Modes of Operation

Basically, the Boost PFC Converter analyses in two conditions i.e., when Switch (S) is closed and when Switch (S) is open

Analysis of closed Switch The diode is reverse biased when the switch is closed as shown in fig. 3.2. Around the path comprising the source, inductor, and closed switch, Kirchhoff's voltage law is

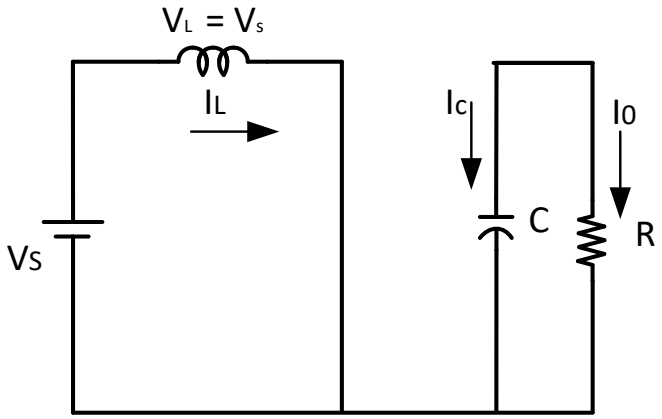


Fig. 3.2 Mode-1

Applying the kirchoff’s voltage low in the first loop

$$V_L = V_S = L\frac{di_L}{dt} \tag{3.5a}$$

Or

$$\frac{di_L}{dt} = \frac{V_S}{L} \tag{3.5b}$$

The rate of change of current is constant, when the switch is closed the current increase in linear form, The change in inductor current is calculated as

$$\frac{\Delta i_L}{\Delta t} = \frac{V_S}{L} \tag{3.6a}$$

Solving for $(\Delta i_L)_{close}$ close switch

$$(\Delta i_L)_{close} = \frac{V_S DT}{L} \tag{3.6b}$$

Analysis of open Switch The inductor current cannot vary instantly when the switch is

opened as shown in fig. 3.3. so that the diode is biased ahead to produce an inductor current route. assuming that the output voltage is constant

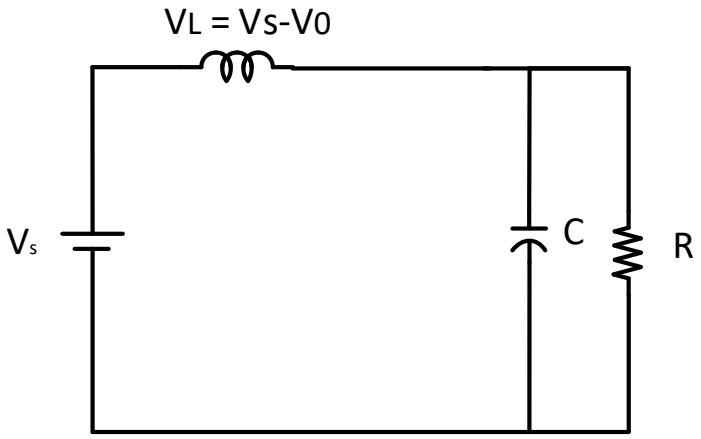


Fig. 3.3 Mode-2

Applying Kirchoff's Voltage and Current low respectively in the above circuit

$$V_L = V_S - V_0 \tag{3.7}$$

$$I_C = I_L - I_0 \tag{3.8}$$

and the voltage across inductor is written as

$$V_L = V_S - V_0 = L\frac{di_L}{dt} \tag{3.9a}$$

$$\frac{di_L}{dt} = \frac{V_S - V_0}{L} \tag{3.9b}$$

Since the inductor current's rate of change is constant, the current must vary linearly while the switch is open. The change in inductor current while the switch is open

$$\frac{\Delta i_L}{\Delta t} = \frac{V_S - V_0}{L} \tag{3.10a}$$

Furthermore, Solving for $\left(\Delta i_L\right)_{open}$

$$\left(\Delta i_L\right)_{open} = \frac{\left(V_S - V_0\right)\left(1-D\right)T}{L} \tag{3.10b}$$

At steady-state condition, the total change in inductor current will be zero, then add the change in inductor current with switch close and open

$$\left(\Delta i_L\right)_{open} + \left(\Delta i_L\right)_{close} = 0 \tag{3.10c}$$

$$\frac{V_S DT}{L} + \frac{\left(V_S - V_0\right)\left(1-D\right)T}{L} = 0 \tag{3.11}$$

Furthermore, Solving for V_0

$$V_S\left(D+1-D\right) - V_0\left(1-D\right) = 0$$

$$V_0 = \frac{V_S}{1-D} \tag{3.12}$$

By understanding that the average power supplied by the source must match the average power absorbed by the load resistor, the average current in the inductor. Power output is

$$P_0 = \frac{V_0^2}{R} = V_0 I_0 \tag{3.13}$$

The Boost Power Factor Correction (PFC) Converter can operate in several modes, depending on the load and input conditions. The Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) are the two main operating modes for the Boost PFC Converter.

3.3.1. Continuous Conduction Mode (CCM)

During the switching cycle in CCM, the inductor current never approaches zero. When the input voltage is greater than the output voltage, the switch is activated, and the inductor current rises linearly. The energy is then transferred to the output capacitor and load by the inductor current once the switch is switched off. The inductor current then linearly drops until the start of the subsequent switching cycle. In addition to providing improved input and output ripple currents, lower electromagnetic interference (EMI), and lower harmonic distortion, CCM is ideal for high load circumstances. The equation and calculation is for continuous conduction mode

Discontinuous Conduction Mode (DCM)

In DCM, each switching cycle results in zero inductor current. When the input voltage exceeds the output voltage and the inductor current begins to rise, the switch is activated. The switch is closed when the current falls to zero, which also marks the beginning of the

inductor current decline. During the off time, the inductor accumulates energy, and then during the subsequent on period, it releases it. In addition to offering lower output voltage ripple, more efficiency, and lower EMI, DCM is appropriate for light load circumstances.

Average voltage is given in discontinuous conduction mode

$$\left\{\begin{matrix} V_{0(avg)} = V_L = V_S \, 0\langle t\langle DT \\ V_L = V_S - V_0 \, DT\langle t\langle \beta T \end{matrix}\right\} \tag{3.14}$$

Furthermore, Solving for V_0

$$V_S\left(DT\right)+\left(V_S - V_0\right)\left(\beta - D\right)T = 0$$

On solving further,

$$V_0 = \frac{\beta V_S}{\beta - D} = \frac{V_S}{1-\frac{D}{\beta}} \tag{3.15}$$

3.2.3 Schematic of Closed Loop Control

This fig. 3.4 represents the comprehensive control block diagram of a PFC Boost Converter. The initial step involves detecting the AC input voltage to generate a sinusoidal reference for the current controller. Subsequently, a voltage controller is employed to regulate the output voltage. This is then followed by a current controller that manages the inductor current while also ensuring the maintenance of a sinusoidal waveshape. Lastly, the output is directed to the PWM block and which is connected to the Gate Terminal of the MOSFET.

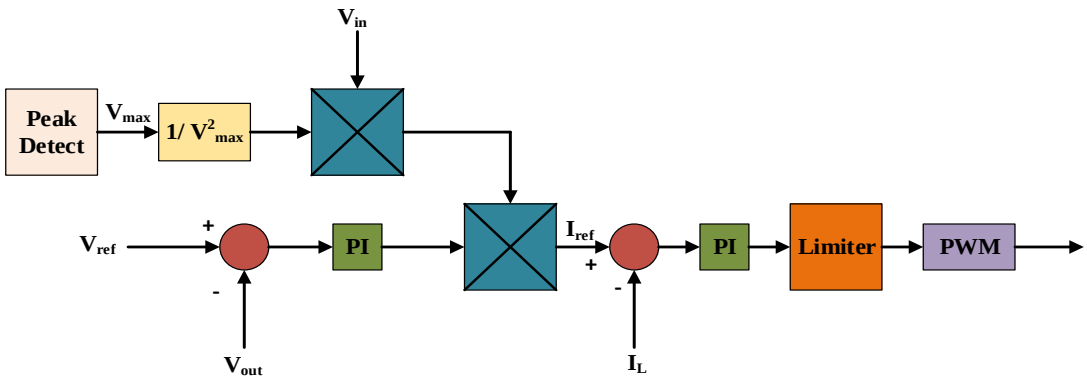


Fig. 3.4 Controller for Boost PFC Converter

3.2.4 Design of the system Parameter

To achieve the desired performance and efficiency, it is important to carefully consider a number of crucial components while designing the system characteristics of a Boost Power Factor Correction (PFC) Converter. Listed below is a quick summary of the system parameter design considerations.

Table 3.1 Boost PFC Converter Specifications

Parameter	**Variable**	**Value**
Supply Voltage	Vin	230 V
Output Power	P_o	2 kW
Supply Frequency	f_{supply}	50 Hz
Switching Frequency	f_{sw}	65 kHz
Input inductor current ripple	ΔI_{L1}	10 %

3.2.4.1 Rectifier Diode Selection

Schottky diodes should be utilised to lower losses. The maximum output current is equal to the forward current rating required:

$$I_{FD} = I_{O(\max^m)} \tag{3.16}$$

Where,

I_{FD} = forward current of the rectifier diode(average)

$I_{O(\max^m)}$ = maximum output current

Peak current ratings for Schottky diodes are significantly greater than average ratings. As a result, the system's higher peak current is not an issue.

The other parameter which is calculated is the power dissipation of the diode.

$$P_{FD} = V_{FD} * I_{FD} \tag{3.17}$$

I_{FD} = forward current of the rectifier diode(average)

V_{FD} = forward voltage of the diode

3.2.4.2 Inductor Selection

In the context of a thesis, it is common to provide a set of recommended inductor values. In such cases, it is advisable to select an inductor value from this range. This is because choosing a higher inductor value results in lower ripple current, which in turn leads to an increase in the maximum output current.[21] The size of the solution decreases as the

inductor value decreases. Because the current increases with decreasing inductance, it should be noted that the inductor must always have a greater current rating than the maximum current indicated in Equation. For the inductor whose range is not described, the following equation is a right estimation for the good inductor:

$$L = \frac{(V_{out} - V_{in}) * V_{in}}{\Delta I_L * f_s * V_{out}} \tag{3.18}$$

V_{in} = Input voltage

V_{out} = Desired output voltage

f_s = minimum switching frequency of the converter

ΔI_L = Inductor ripple current,

Since the inductor is unknown, Equation 1 cannot be used to compute the inductor ripple current. 20% to 40% of the output current is a decent estimate for the inductor ripple current.

$$\Delta I_L = (0.2 - 0.4) * I_{O(\max^m)} * \frac{V_{out}}{V_{in}} \tag{3.19}$$

ΔI_L =Inductor ripple current

$I_{O(\max^m)}$ = maximum output current

3.2.4.3 Calculate the Maximum Switch Current

The duty cycle, D, for the lowest input voltage must be determined in order to compute the switch current. The smallest input voltage is employed because it produces the most switch current.

$$D = 1 - \frac{V_{in(\min^m)} * \eta}{V_{out}} \tag{3.20}$$

$V_{in(\min^m)}$ = minimum value of input voltage

V_{out} = output voltage

η = efficiency of the converter

The duty cycle calculation includes efficiency because the converter must provide the energy lost as well. Compared to using just the equation without the efficiency factor, this computation provides a more accurate duty cycle.

Either an estimated factor, (which is not unrealistic for a boost converter worst case efficiency),

Now in next step we will calculate maximum switch current

$$\Delta I_L = \frac{V_{in(\min^m)} * D}{f_s * L} \tag{3.21}$$

$V_{in(\min^m)}$ = minimum input voltage

D = duty cycle

f_s = minimum switching frequency of the converter

L = selected inductor value

Now it has to be determined if the selected IC can deliver the maximum output current.

$$I_{\max^m(out)} = \left(I_{\lim.(\min^m)} - \frac{\Delta I_L}{2} \right) * (1 - D) \tag{3.22}$$

$I_{\lim.(\min^m)}$ = minimum value of the current limit of the integrated switch (given in the data)

ΔI_L = inductor ripple current calculated in Equation

D = duty cycle calculated in Equation

A different IC with a larger switch current limit must be used if the computed value for the maximum output current of the chosen IC, I_{MAXOUT}, is less than the system's required maximum output current It is only possible to utilise the chosen IC with a greater inductance inductor if it is still within the recommended range and the calculated value for IMAXOUT is only a tiny bit smaller than the needed one higher inductance lowers ripple current, which raises the maximum output current possible with the chosen IC.

Higher inductance lowers ripple current, which raises the maximum output current possible with the chosen IC.

$$I_{sw(\max^m)} = \frac{\Delta I_L}{2} + \frac{I_{O(\max^m)}}{(1 - D)} \tag{3.22}$$

ΔI_L = inductor ripple current calculated in Equation

$I_{O(\max^m)}$ = maximum output current necessary in the application

D = duty cycle calculated in Equation

The inductor, integrated switch(es), and external diode must sustain this peak current.

3.2.4.4 Output Capacitor Selection

Any capacitor value beyond the minimum suggested in the data sheet can be used if the converter includes external compensation, but the compensation must be adjusted for the output capacitance being utilised. The recommended inductor and capacitor values for

internally compensated converters should be utilised, or the data sheet's instructions for adapting. The output capacitor values can be changed using the following formulae with external compensation:

$$C_{o(\min^m)} = \frac{I_{O(\max^m)} * D}{f_s * \Delta V_o} \tag{3.23}$$

$C_{o(\min^m)}$ = output capacitance(minimum)

$I_{O(\max^m)}$ = output current(maximum)

D = duty cycle calculated with Equation

f_s = minimum switching frequency of the converter

ΔV_o = output voltage ripple(desired)

The ESR of the output capacitor adds some more ripple, given with the equation:

$$\Delta V_{o(ESR)} = ESR * \left(\frac{I_{O(\max^m)}}{(1-D)} + \frac{\Delta I_L}{2} \right) \tag{3.24}$$

$\Delta V_{o(ESR)}$ = increased output voltage ripple brought on by capacitor ESR

ESR = equivalent series resistance

$I_{O(\max^m)}$ = output current(maximum)

3.3 Results

The Boost PFC Converter underwent simulation utilizing MATLAB software. The simulation results are depicted in Fig. 3.6, illustrating the waveforms of the input voltage and current for the Boost PFC Converter. It can be seen from fig. 3.7 that the output voltage is kept constant at 460V. Furthermore, Fig. 3.8 displays the Total Harmonic Distortion (THD) and fundamental current characteristics for the converter. The AC voltage applied to the proposed topology was set at 230V, while the inductor value was selected as 3.3mH. It was observed that the output voltage and current of the converter exhibited phase alignment, indicating effective power factor correction. Harmonic Distortion (*THD*) is a crucial performance metric that assesses how well a power converter's output waveform performs. A simulation is run in this study for a particular set of operational parameters, such as an input voltage of 230 V_{AC}, a switching frequency of 65 kHz, and a load resistance of 80Ω.

The outcomes of the simulation demonstrate that the ILDB PFC Converter offers lower THD values than the traditional Boost PFC Converter.

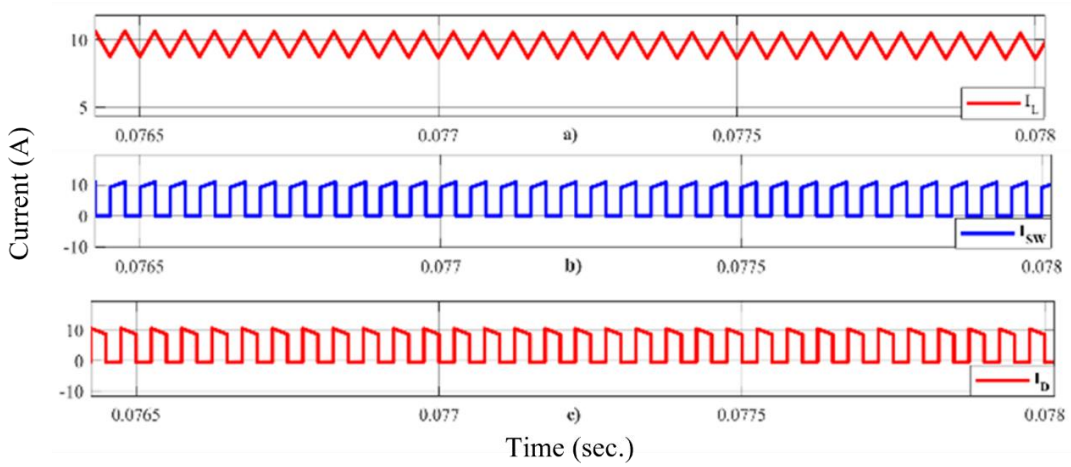


Fig. 3.5 Current Waveform Boost PFC(BPFC) topology a). Inductor current(I_L) b).Switch Current c).Diode Current

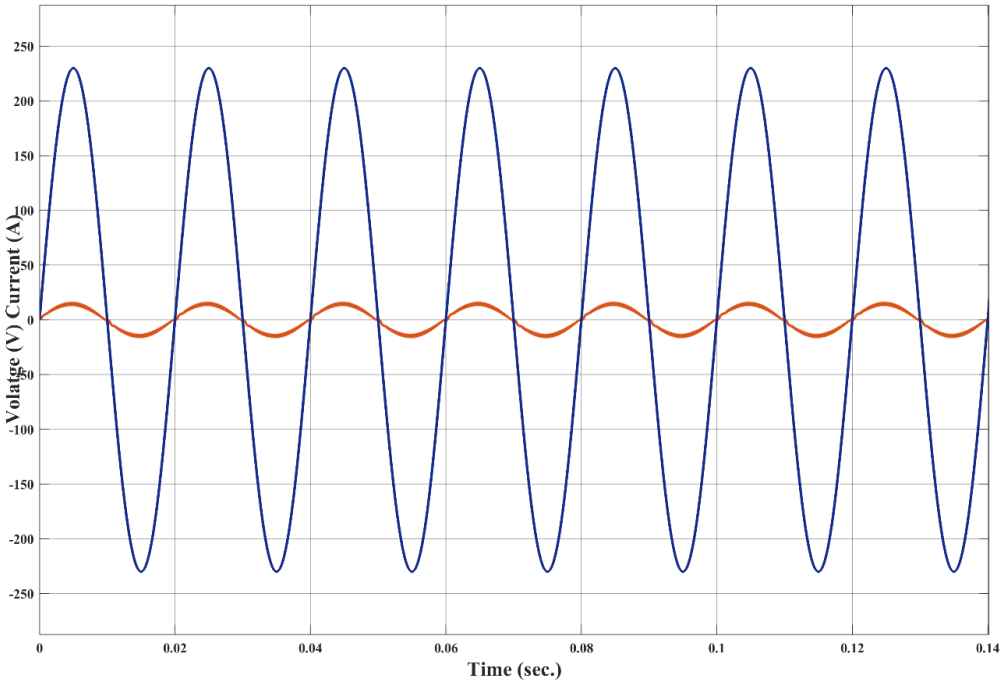


Fig. 3.6 Input Current and Voltage Waveform for Boost PFC(BPFC) topology

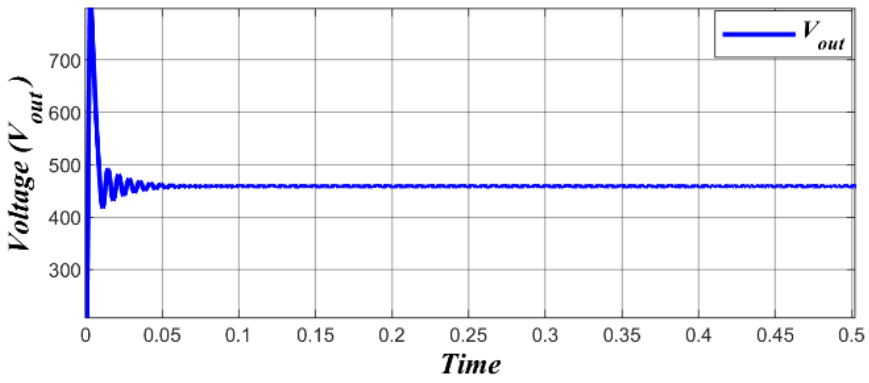


Fig. 3.7 Output Voltage Waveform Boost PFC topology (BPFC)

Total Harmonic distortion is shown in the below Fig. 3.8 as shown the Fundamental current is 17.72 Amp. and THD is 1.92% i.e., harmonic is less than 2% 0f fundamental and third fifth order harmonics are less than 1%

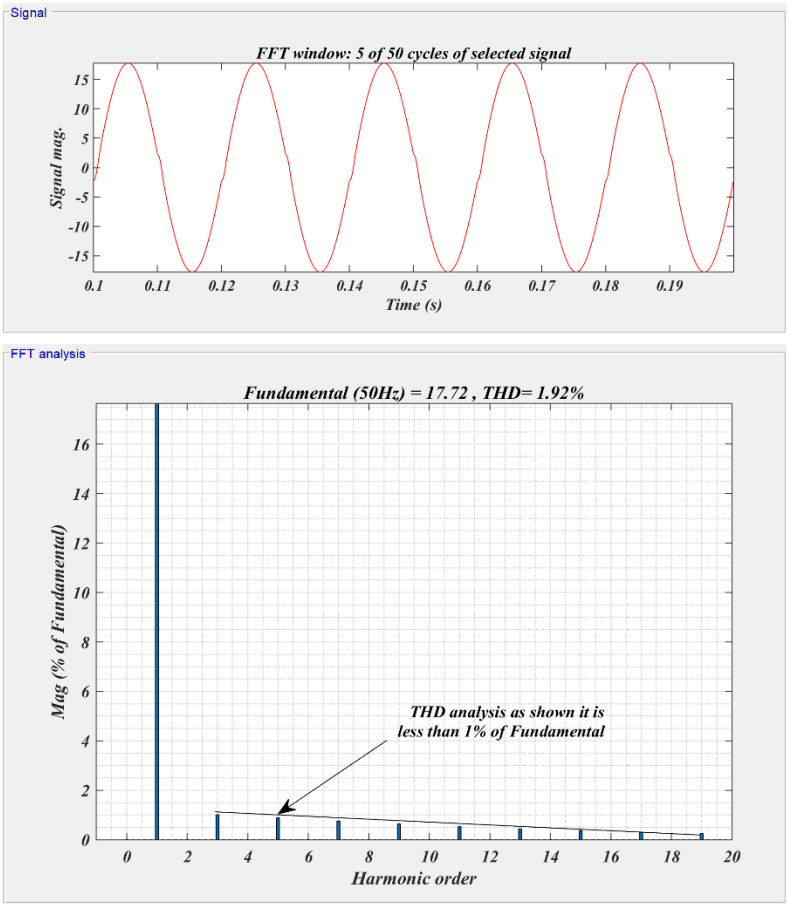


Fig. 3.8 THD analysis of Boost PFC Converter

3.4 Conclusion

The investigation of (THD) unveiled the Boost Power Factor Correction (PFC) Converter's capability to draw sinusoidal current from the AC source, resulting in diminished harmonic distortion. Through achieving a power factor close to unity, the converter effectively enhanced power quality. The comprehensive evaluation of THD and power factor across different load conditions provided a thorough comprehension of the converter's performance in mitigating harmonics and correcting power factor.

The efficiency analysis shed light on the converter's energy conversion efficiency by considering losses in switches, diodes, and other components. By evaluating the impact of variable input voltage, load current, and switching frequency, the efficiency analysis furnished significant insights for optimizing the converter's operational efficiency. These findings offer valuable guidance for enhancing the overall energy efficiency of AC-DC power supplies that employ the Boost PFC Converter.

Furthermore, the discourse on control strategies employed in the converter elucidated the techniques utilized for output voltage regulation. By exploring diverse control techniques, including voltage mode control and current mode control, the thesis highlighted the effects of these strategies on the converter's performance and stability. This analysis serves as a crucial reference for selecting appropriate control strategies to achieve the desired output voltage regulation.

In summary, this thesis has significantly contributed to the understanding of the Boost PFC Converter's THD, efficiency, and performance. The insights gained from this analysis provide a solid foundation for further research and development in the realm of power factor correction and AC-DC power supply design. The knowledge derived from this thesis can propel advancements in power electronics technologies, leading to more efficient and reliable power conversion systems.

CHAPTER 4

4 ANALYSIS OF INTERLEAVED BOOST PFC CONVERTER

4.1 Introduction

A power electronics topology called the Interleaved Boost Power Factor Correction (PFC) Converter is used in a variety of applications to raise power factor, lower harmonic distortion, and increase energy economy. In systems like switch-mode power supply, renewable energy systems, electric vehicle charging stations, and industrial power distribution, where a stable and high-quality DC voltage is required, it is frequently used. A PFC converter's main goal is to minimise harmonics in the input current waveform, align it with the input voltage waveform, and provide a power factor that is close to unity. This guarantees that electrical power from the grid is used effectively and that all legal requirements are met. Power handling capacity and current ripple are restrictions of conventional single-phase PFC converters. The ILDB PFC Converter has grown in prominence as a solution to these drawbacks.

A number of identical boost converter stages that make up the ILDB PFC Converter are normally interleaved in parallel and run at the same time. When compared to single-phase PFC converters, each stage processes a smaller portion of the total power, which reduces current ripple and improves power handling capability. The interleaved technique boosts efficiency and system dependability by dividing the power throughout several stages, reducing the current stress on individual components. The interleaved switching of the various converter stages defines how an ILDB PFC Converter operates. The duty cycle of the converter switches is adjusted to manage the output voltage and maintain power factor correction when this switching is controlled, which is commonly done using a high-frequency (PWM) technology. The converter's interleaved design guarantees that each stage's switching transitions are dispersed equally, which lowers the overall ripple current and enhances the converter's dynamic response[23].

The ILDB PFC Converter's capacity to withstand higher power levels while keeping high efficiency is one of its main advantages. Each stage runs at a reduced current level when the load is distributed throughout several stages, lowering losses and raising overall converter efficiency. It is also simpler to adhere to electromagnetic compatibility (EMC) regulations thanks to the decreased current ripple's contribution to fewer electromagnetic interference (EMI) emissions. The ILDB PFC Converter also has redundancy built right in. The

remaining stages keep running, assuring system operation, even if one step malfunctions or becomes unplugged. The converter's fault tolerance and dependability in important applications are improved by this feature.

Overall, The ILDB PFC Converter is a very effective and dependable power electronics topology for accomplishing power factor correction in a variety of applications. Higher power handling, less current ripple, better efficiency, and better dynamic response are all made possible by its interleaved structure. The ILDB PFC Converter is an essential component of contemporary power systems because it can meet regulatory requirements and deliver clean power, which promotes energy efficiency and sustainable development.

4.2 Analysis of Interleaved Boost PFC Converter

The Interleaved Boost Power Factor Correction (PFC) Converter is a desirable option for power electronics applications due to a number of its benefits and traits[24]. Let's examine the main features and advantages of the ILDB PFC Converter in greater detail:

- Current Ripple Reduction: The input and output current ripple in 1-phase PFC converters can be substantial, increasing losses and EMI emissions. The ILDB PFC Converter's interleaved design, however, allows the various converter stages to work independently of one another. As a result, the ripple currents from various stages are mixed together, significantly lowering the total ripple of the current. With this feature, the converter's efficiency is increased while EMI emissions are decreased, making it simpler to meet strict electromagnetic compatibility (EMC) regulations.

$$K(D) = \frac{1-2D}{1-D} \quad D \le 0.5$$

$$K(D) = \frac{2D-1}{D} \quad D > 0.5 \tag{4.1}$$

- Power Factor Correction: A PFC converter's main goal is to align the input current waveform with the input voltage waveform in order to provide a power factor that is close to unity. By guaranteeing that each step runs concurrently and in synchronisation with the input voltage, the ILDB PFC Converter excels at power factor correction. Through this synchronised effort, the input current's harmonic content is minimised, distortion is decreased, system's power factor is enhanced. In addition to improving energy efficiency, the converter's near-unity power factor guarantees adherence to power quality standards and regulations.

- Power Handling Capability: The ILDB PFC Converter's capacity to manage higher power levels in comparison to conventional single-phase PFC converters is one of its key benefits. Each stage processes a portion of the entire power due to the power being split over several parallel stages, decreasing the strain on individual components. The converter can efficiently handle larger power levels while maintaining excellent system reliability thanks to this distributed power processing capacity.
- Improved Efficiency: The converter operates in an interleaved manner, which helps to increase efficiency while also reducing current ripple. Each stage runs at a lower current level when the power is distributed over several stages, which lowers conduction losses. The dispersed design of the converter further decreases switching losses because each stage runs at a lower frequency . Higher total power conversion efficiency that leads to energy savings and less heat dissipation are the results of these efficiency improvements.

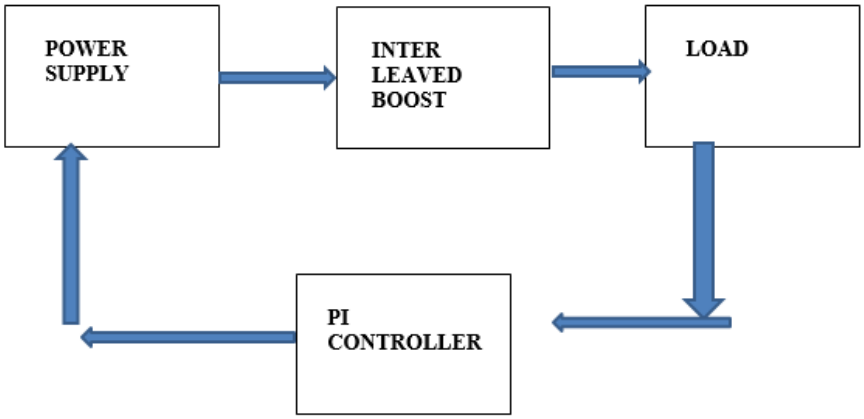


Fig. 4.1 Block diagram Interleaved Boost

Boost inductor magnetic volume can be reduced by the designer via inductor ripple current cancellation and the block diagram of interleaved boost PFC Converter is shown in Fig. 4.1. This is because the two interleaved inductors only need to store half as much energy as a single stage pre-regulator created for the same power level, switching frequency, and inductance.

Single stage inductor energy (E_I):

$$E_1 = \frac{1}{2} LI^2 \tag{4.2}$$

Two phase total inductor energy (E_{II}):

$$E_{il} = \frac{1}{2} L \left(\frac{I}{2} \right)^2 + \frac{1}{2} L \left(\frac{I}{2} \right)^2 = \frac{LI^2}{4} \tag{4.3}$$

Magnetic volume reduction is not a direct result of decreased energy storage. Design professionals could anticipate a reduction in magnetic volume of up to 25%

OUTPUT CAPACITOR RIPPLE CURRENT REDUCTIONS AS A FUNCTION OF DUTY CYCLE

The output capacitor RMS current is decreased as an added benefit of interleaving PFC pre-regulator stages.[25] being aware in applications for universal PFC pre-regulators ranges from 100% to 2% The output capacitor will experience less electrical stress as a result of the RMS current drop, increasing converter dependability.

$$I_{C_{out1}}(D) = \sqrt{(1-D)^2\,(*1-D)}$$

$$I_{C_{out1}}(D) = \frac{1}{2}\sqrt{(1-2D)^2 * (1-2D)} \quad \text{for} \quad D < 0.5$$

$$I_{C_{out1}}(D) = \frac{1}{2}\sqrt{(2-2D)^2 * (2-2D)} \quad \text{for} \quad D > 0.5 \tag{4.4}$$

4.2.1 Schematic of Interleaved Boost PFC Converter

It is well known that the Interleaved Boost PFC converter may produce high power densities, better power factor correction, and lower input and output current ripple. For a thesis project, displays the schematic of the ILDB PFC converter as shown in Fig. 4.2 while stressing its essential parts and operation. The $I_{.}$ and I_{out} are shared between several parallel-connected power stages in the ILDB PFC converter. This interleaved architecture increases system efficiency and reliability by dividing the power among several stages and reducing ripple current. In order to maintain a constant current flow and achieve peak performance, the converter runs in continuous conduction mode (CCM).

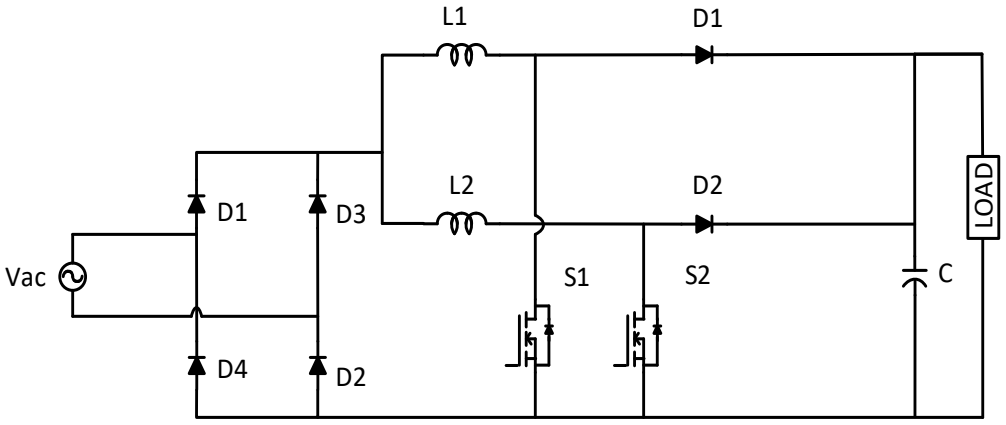


Fig. 4.2 Schematic of Interleaved Boost PFC Converter

Bridge Rectifier A bridge rectifier is used to first rectify the input AC voltage, creating a pulsing DC voltage. The positive and negative half cycles of the input voltage are rectified

by the bridge rectifier, which is made up of diodes that conduct alternately. The ILDB PFC converter's heart is its interleaved boost converter stages. Interleaved Boost Converter with coupled inductor winding as in Fig. 4.3 is depicted and differential winding is used for less losses Each stage is made up of an output capacitor, an inductor, a diode, and a power switch (like a MOSFET). In order to share input and output currents among several stages and distribute power among them while lowering overall ripple, these stages are connected in parallel.

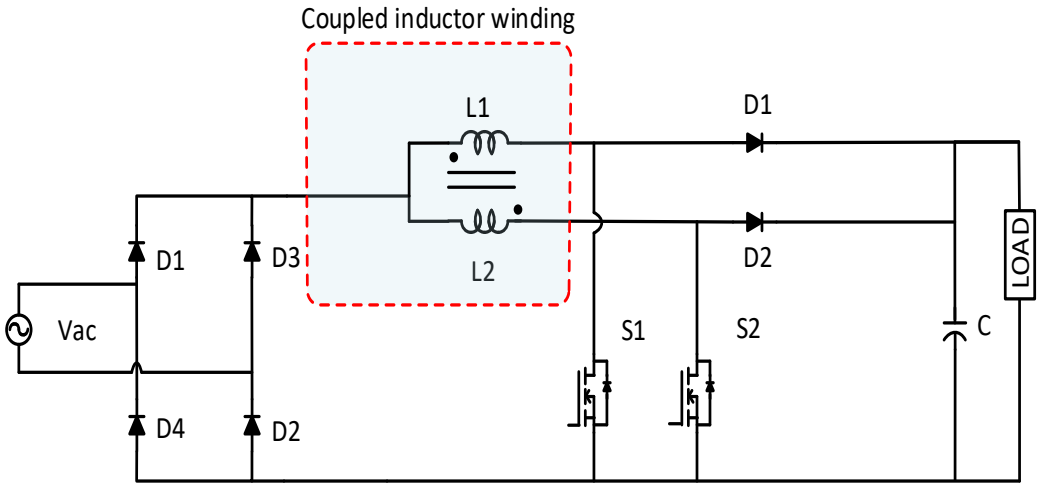


Fig. 4.3 Interleaved Boost PFC Converter with coupled inductor

The following are a few crucial points about interleaved boost converters:-

- The parallel connection through the interleaved boost converter divides the current, minimising I2R losses and reducing current stress.
- There will be less current ripple on the output side, which will also reflect the input current.
- A different switching interconnection called interleaving enhances synchronisation of the actual pulse frequency.
- By using an interleaving technique, the energy can be saved and improved power conversion without lowering conversion efficiency.

$$P_{mosfetSW} = \left(E_{on} + E_{off}\right) * f_{sw} \tag{4.5}$$

$$P_{mosfetCOND} = R_{mosfet} * I_{mosfet(RMS)^2} \tag{4.6}$$

$$P_{diode} = R_{diode} * I_{diode(RMS)^2} \tag{4.7}$$

4.2.2 Modes of Operation

One channel can be used to analyse the mode of operation. Since both inductors are identical and both power channels share the same current, each power channel operates in the same way. The boost converter can be categorised into continuous or discontinuous conduction mode depending on how much energy is given to the load during each switching interval. Discontinuous conduction mode (DCM) is the name given to the mode of operation when Each switching cycle results in a complete transfer of the inductor's energy to the load. During the switch-off time in this mode, the inductor current decreases till it meets to zero. The converter is considered to be working in continuous conduction mode (CCM) if just a portion of the energy is transferred to the load.

The converter's electrical properties are largely dependent on its mode of operation. Between modes, the features differ greatly[26]. Since both inductors are identical and both power channels share the same current, each power channel operates in the same way. The boost converter can be categorised into continuous or discontinuous conduction mode depending on how much energy is given to the load during each switching interval. Discontinuous conduction mode (DCM) is the name given to the mode of operation when the entire amount is transferred to the During the switch-off time in this mode.

The converter's electrical properties are largely dependent on its mode of operation.

Mode-1- The diodes D1 and D2 are off during mode-1, while switches S1 and S2 are switched on.

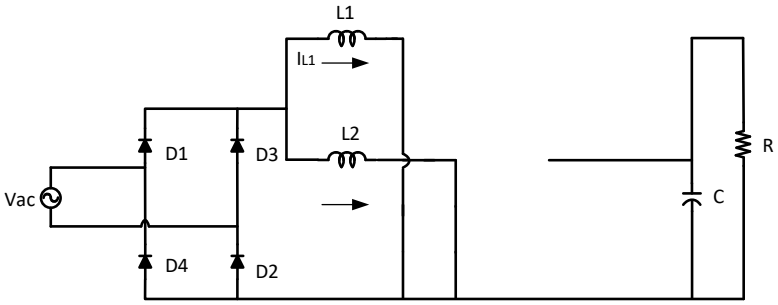


Fig. 4.4 Mode-1

Mode 2:- Switch S1 is on in mode 2, Switch S2 is off in mode-2, Switch D1 is off in mode 2, and Switch D2 is on in mode 2, respectively.

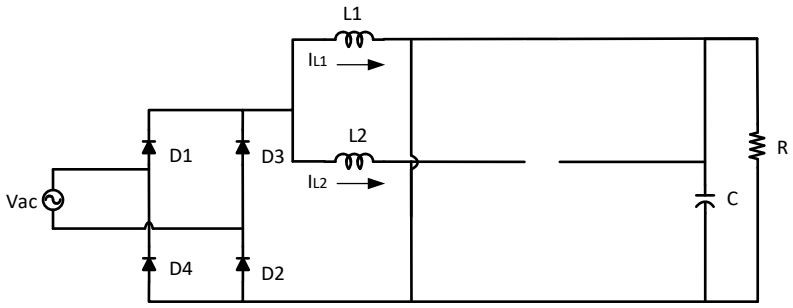


Fig. 4.5 Mode-2

Mode 3- In Mode-3 Switch S1 is in the off position during mode 1, Switch S2 is in the on position, Switch D1 is in the on position, and Switch D2 is in the off position.

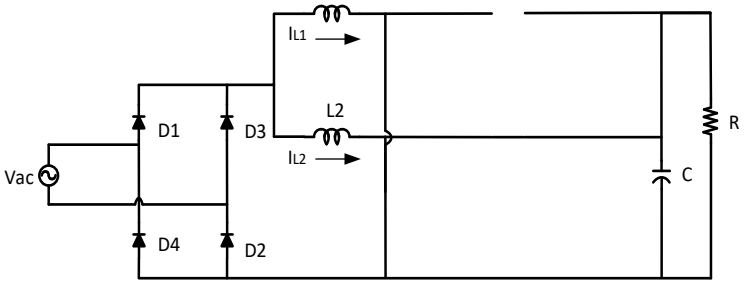


Fig. 4.6 Mode-3

Mode 4- The diodes D1 and D2 are on during mode-4, while switches S1 and S2 are switched off.

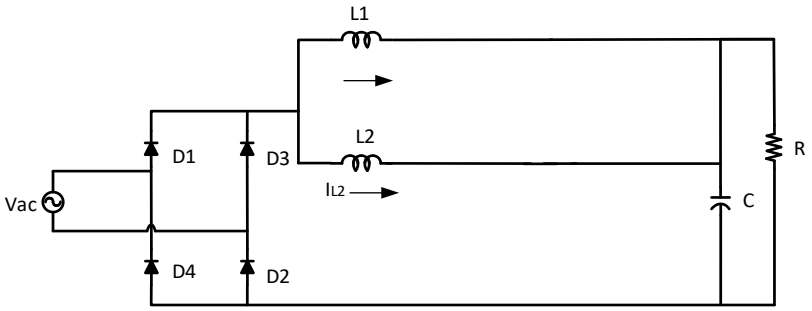


Fig. 4.7 Mode-4

4.2.3 Schematic of Close Loop Control

A reference voltage is used as a comparison between the measured and reference DC bus voltages. For zero error DC bus voltage regulation, the voltage error that results is then communicated to a PI voltage controller as shown in Fig. 4.8. The controller's output is supplied to the inner controller as the amplitude of the reference supply current. Additionally, to simulate the behaviour of a pure resistor, The current reference needs to be changeable in magnitude. For this, an analogy multiplier is employed. Next, the detected inductance current is reduced by the reference current, and the gate commands for the S1

and S2 MOSFET devices are generated, respectively, as determined by their comparison with two 48 kHz triangular carriers that are 180° phase-shifted from one another.

The outer loop is meant to provide the control system with high stability by being sufficiently slower than the inner loop.[24] The closed-loop control system of the ILBPFC (PFC) converter comprises crucial components such as a feedback loop, a controller, a pulse-width modulation (PWM) generator, and voltage and current sensing elements. Together, these components ensure precise regulation of the converter's operation, effectively maintaining the desired V_0 and power factor correction.

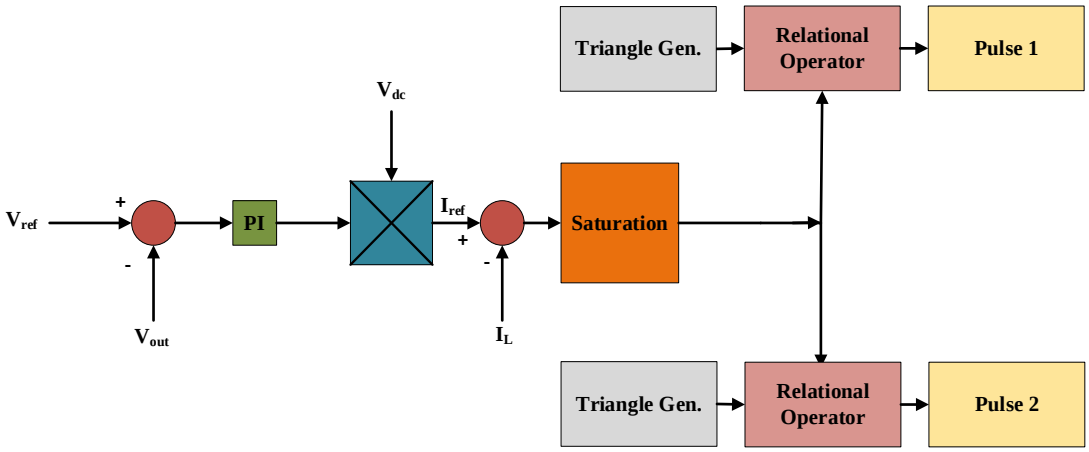


Fig. 4.8 Interleaved Boost PFC Controller

The closed-loop control system continuously monitors V_{out} through the feedback loop. Any deviation between the reference voltage and the measured output voltage is amplified and processed by the error amplifier and controller. the energy transfer is modulated, allowing precise regulation of the V_0 to the desired level.

The feedback loop, consisting of a voltage divider network, is responsible for measuring the V_{out} and providing feedback information to the controller. The voltage divider network scales down the output voltage for comparison, while the error amplifier amplifies the discrepancy between the reference voltage and the measured output voltage. The controller interprets the feedback information received from the error amplifier and generates the necessary control signals to adjust the duty cycle of the PWM signal. Typically using a microcontroller or a digital signal processor (DSP), the controller employs advanced control algorithms like proportional-integral-derivative (PID) control to regulate the converter's operation effectively.

The PWM generator generates the PWM signal based on the control signals from the controller. This PWM signal controls the switching action of the power switches in the interleaved boost converter stages. By adjusting the amount of energy transferred from the input to the output is regulated, ultimately controlling and stabilizing the V_0, current sensing elements, such as transformers, dividers, or shunts, are utilized to measure the input voltage, output voltage, and input and output currents. These measured values are utilized as feedback in the control loop, facilitating regulation of the converter's operation

Furthermore, the closed-loop control system ensures power factor. Through adjusting power factor correction.

4.2.4 Design of System Parameter

This thesis introduces a design methodology for determining the system parameters of an interleaved Boost (PFC) converter. The ILDB PFC converter is a commonly utilized configuration that ensures a superior power factor and reduced total harmonic distortion in AC-DC power conversion systems.

Table 4.1 Interleaved Boost Converter Specifications

Parameter	Variable	Value
Supply Voltage	Vin	230 V
Output Power	P_o	2 kW
Supply Frequency	f_{supply}	50 Hz
Switching Frequency	f_{sw}	65 kHz
Input inductor current ripple	ΔI_{L1}	10 %

The objective of research is to optimize the system parameters in order to enhance the converter's performance, particularly in terms of efficiency, power factor, and (THD). The design approach employed aims to minimize the presence of input current harmonics while simultaneously overall system efficiency. The proposed methodology is implemented through simulations and experimental validation, providing evidence of the effectiveness of the designed system parameters for the ILDB PFC converter. Determining the maximum and minimum duty cycles involves Analyse the power system's required current and input voltage range and to meet with applicable standards, the appropriate power factor correction range and input current harmonic restrictions must be met. Depending on the application,

determine the desired output voltage and power rating to ensure stable functioning, take into account the load characteristics and variances. Choose the proper inductors, capacitors, and switching components Think about things like switching frequency capability, efficiency, switching current rating, and voltage rating Design the input and output inductors to adhere to the necessary core parameters, current rating, and inductance value. Based on voltage and current ratings, switching speed, and conduction losses, choose switching devices like MOSFETs or IGBTs. Think about the switching transitions' thermal properties, gate drive needs, and voltage stress. Depending on the system needs and intended power rating, decide how many interleaved phases to use to equally divide the load among the phases and lessen current imbalance, optimise the interleaving system. knowledge from these parameters, certain percentage of peak-to-peak inductor current ripple relative to Subsequently, the inductor value is calculated using information such as.[27] To maintain a high power factor and adjust the output voltage, create a reliable control loop Depending on the dynamics of the system, choose the appropriate control methods.

Design equation

i. Boost Ratio

The duty ratio affects the boosting ratio of the Interleaved Boost Converter. It operates the same as a traditional boost converter. It's described as;

$$\frac{V_0}{V_{in}} = \frac{1}{1-D} \tag{4.9}$$

ii. Selection of Inductor

The magnetic components are crucial for energy storage and filtering in power electronic systems. In power electronic systems, the magnetic components are essential for energy storage and filtration. In order to balance the current in two boost converters, two inductors must, in theory, be identical.

iii. Duty Cycle Formula

The duty cycle, D, for the lowest input voltage must be determined in order to compute the switch current. The smallest input voltage is employed because it produces the most switch current.

$$D = 1 - \frac{(V_{in} * \eta)}{V_0} \tag{4.10}$$

Since the smallest input voltage generates the greatest switch current, it is used to Compared using just the equation without the efficiency factor, this computation provides a more accurate duty cycle.

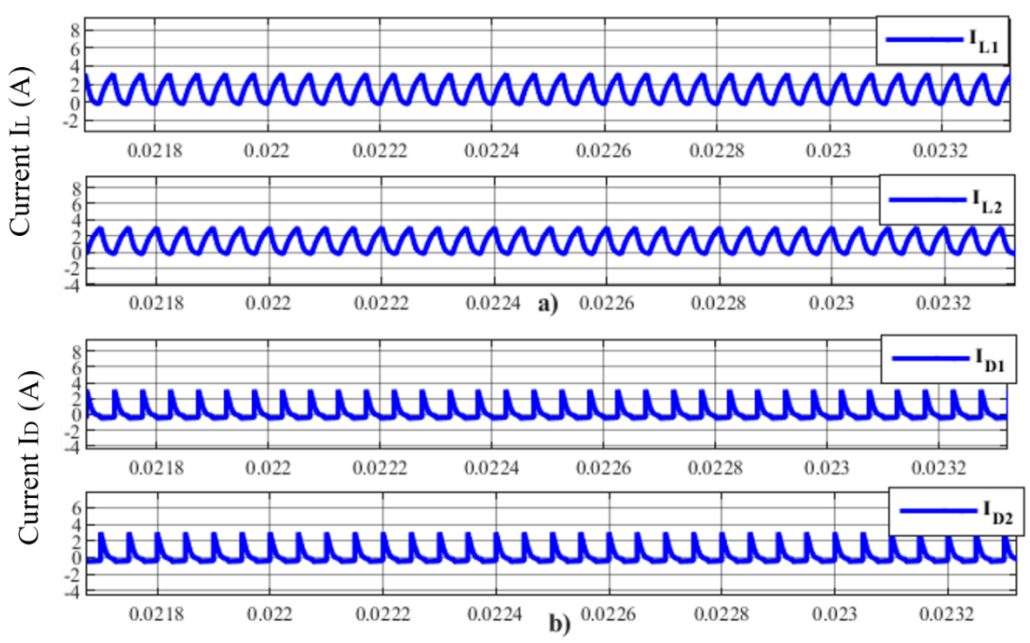
iv. Output Current

We can find out the output current for the proposed converter with the given below formula

$$I_0 = \frac{P_0}{V_0} \tag{4.1}$$

4.3 Results

In case of interleaved Boost PFC Converter, we have seen the Current Waveform Interleaved Boost PFC Converter for Inductor, Switch and Diode respectively as depicted in Fig. 4.9



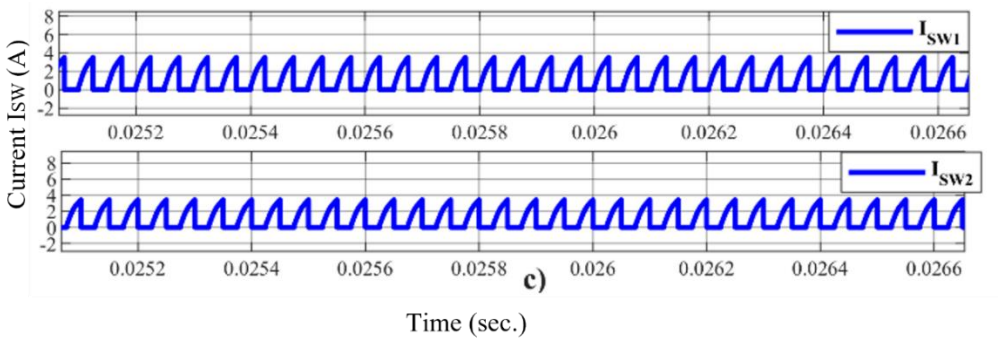


Fig. 4.9 Current Waveform Interleaved Boost PFC(IBPFC) topology a). Inductor current(I_{L1}&I_{L2}) b).Switch Current(I_{SW1}&I_{SW2}) c).Diode Current(I_{D1}&I_{D2})

Waveform for Input Voltage and current for interleaved Boost PFC Converter is also shown in fig4.10. Output voltage are as well shown and after that we have calculated Total Harmonic Distortion for the same is shown in Fig. 4.11.

The waveform for Inductor, diode and switch current is shown. For inductor 1&2 the waveforms are 180 degree apart from each other as in case of Interleaved the parameter are connected in interleaved form so, there property are 180 degree apart as it is shown in the waveform of Inductor, Diode and Switch.

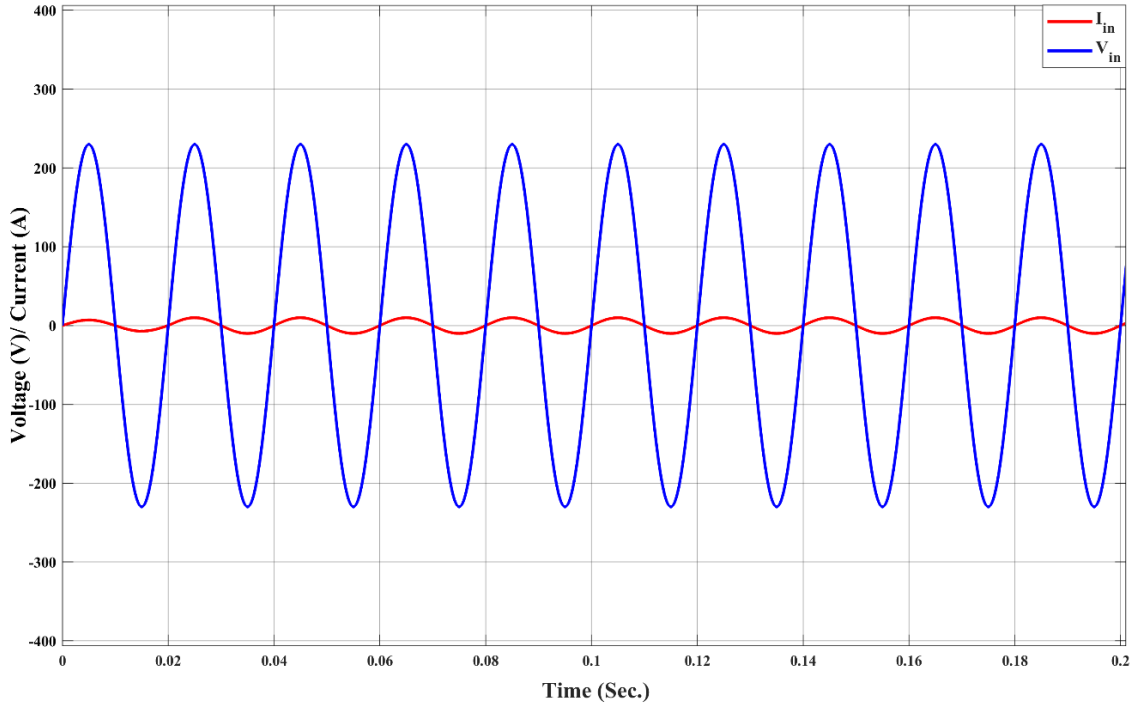


Fig. 4.10 Input Current and Voltage Waveform for Interleaved Boost PFC topology

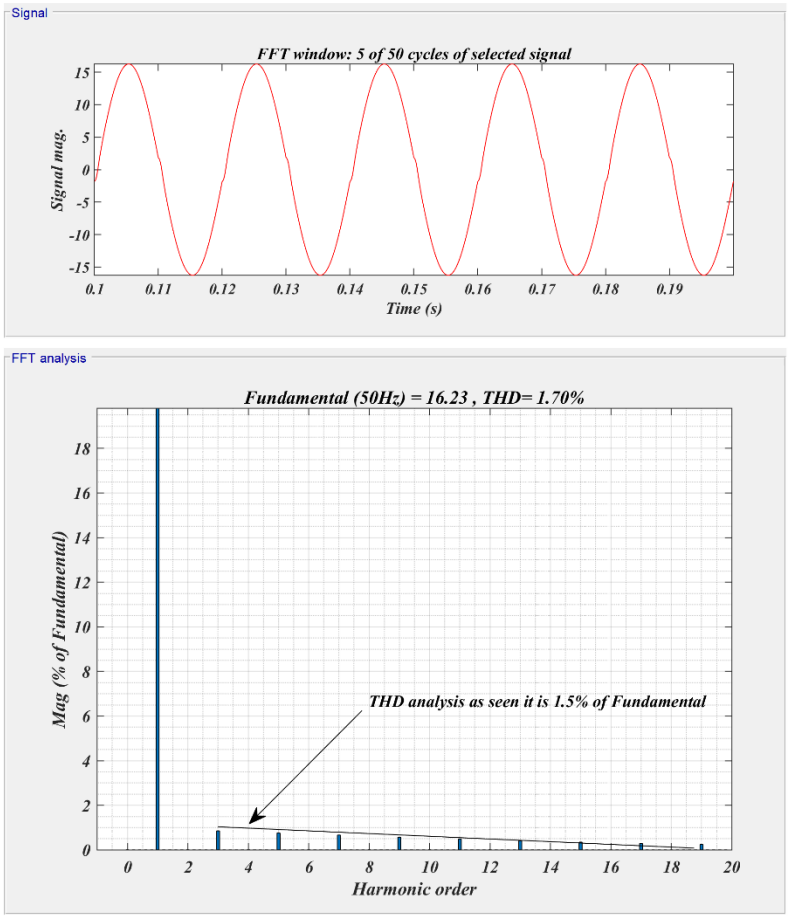


Fig. 4.11 THD analysis of Interleaved Boost PFC Converter

4.4 Conclusion

In conclusion, this thesis has provided a comprehensive analysis of the Interleaved Boost Power Factor Correction (PFC) converter, examining its operational principles, control strategies, and design considerations. The investigation aimed to explore the benefits, challenges, and potential applications of this converter topology within power electronic systems. The ILDB PFC converter offers notable advantages, including enhanced power quality, reduced input current harmonics, and increased efficiency. By employing multiple converter stages in an interleaved manner, the converter can handle high power levels while effectively distributing the current and reducing the size of individual components. These benefits make it a suitable choice for applications that require high power factor and low total harmonic distortion, such as electric vehicle chargers, renewable energy systems, and industrial power supplies. Addressing these challenges requires careful consideration during the design and implementation phases to ensure reliable and optimal operation. Advanced control techniques, such as current sharing and phase shifting, can be utilized to overcome these issues and enhance the converter's performance. Furthermore, the thesis explored

various control strategies for the ILDB PFC converter, including voltage mode control, current mode control, and predictive control. Each strategy possesses its own advantages and limitations, and the selection of the control technique depends on the specific requirements of the application. It is crucial to choose an appropriate control scheme that achieves high performance in terms of power factor correction, transient response, and stability. Additionally, the thesis emphasized the significance of proper component selection, encompassing power devices, inductors, and capacitors, to ensure reliable and efficient operation of the ILDB PFC converter. The choice of components directly affects the converter's power handling capability, losses, and overall cost. Thorough design considerations, such as thermal management, switching frequency selection, and voltage stress analysis, are essential to attain optimal performance and long-term reliability.

Overall, this thesis contributes to the understanding and advancement of the ILDB PFC converter, providing insights into its advantages, challenges, and potential applications. As technology continues to progress and the demand for high-efficiency power conversion grows, this converter topology holds promise as an effective solution for power factor correction and improved power quality in diverse power electronic systems.

CHAPTER 5

5 ANALYSIS OF SEMI-BRIDGELESS BOOST PFC CONVERTER

5.1 Introduction

Power electronics technology has become a crucial area of research as a result of rising energy demands and worries about environmental sustainability. PFC converters, which have a wide range of applications, are essential for enhancing the effectiveness and power quality of electronic systems. The (SBB) converter, which has been developed in the search for more dependable and efficient PFC topologies, has promising advantages over its traditional bridge-based competitors.

In order to combine the advantages of bridgeless and bridge-based topologies, the SBBPFC is the focus of this thesis's research, design, and analysis. Significant characteristics of the SBB converter include increased efficiency, a smaller component count, improved power factor correction, and lower losses. This research intends to overcome the restrictions associated with conventional bridge-based PFC converters by utilising the inherent benefits of the SBB topology[27].

The SBBPFC converter's operational principles and control schemes will be thoroughly examined as the initial focus. Fundamental operating principles can be determined by understanding the converter's architecture and distinctive features. Analysing switching behaviour, current flow pathways, and voltage conversion mechanisms are all part of this investigation. Such information will operate as the basis for the creation of suitable control methods to manage performance and accomplish targeted power factor correction.

The performance of the converter under various operating situations will next be thoroughly examined. The properties of SBBPFC converter will be assessed by theoretical research, computer simulations, and experimental validation. This analysis will take into account scenarios like changing input voltage, shifting loads, and transient reactions, evaluating stability, effectiveness, and overall performance. In order to increase energy efficiency and meet strict power quality standards, efforts will also be made to minimise losses, enhance power factor correction, and decrease harmonic content.

Additionally, it will be critical to optimise design parameters and control strategies. The goal is to achieve maximum energy economy while assuring dependable operation, taking into account aspects like component selection, power losses, and temperature management. In order to improve dynamic responsiveness, transient performance, and fault tolerance

capabilities, sophisticated control algorithms and modulation schemes will be researched. Through these optimisation efforts, the SBBPFC may be fine-tuned to meet the needs of many applications, including renewable energy systems, electric vehicle charging stations, and power distribution networks.

The findings of this thesis have the potential to significantly develop PFC converter technology. This study will equip engineers and researchers with a thorough understanding of the SBBPFC, enabling them to create trustworthy. The acquired knowledge will also have a significant impact on the creation of carbon emission reduction strategies and environmental preservation initiatives.

As a novel approach to increase energy efficiency and boost power quality, this thesis investigates and evaluates the SBBPFC. This study provides insight into the development of sophisticated power electronic converters by a thorough investigation of operating principles, performance traits, and control schemes. In the end, the discoveries will support the creation of cleaner, more sustainable energy systems that will help solve our time's urgent energy problems

5.2 Analysis of Semi-Bridgeless Boost PFC Converter

Power Factor Correction (PFC) converters play a crucial role in modern power electronic systems, with the objective of enhancing energy efficiency and power quality. Within the wide range of PFC configurations, the Semi-Bridgeless Boost converter has gained significant interest due to its notable benefits, such as minimized conduction losses, increased power density, and enhanced reliability. The purpose extensively and efficiency attributes of the SBBPFC, placing particular emphasis on its analysis.

Performance analysis:

The comprehensive evaluation of the SBBPFC's performance involves the thorough examination of several essential parameters. Primarily, the converter's ability to be meticulously assessed. By reducing conduction losses commonly observed in traditional bridge-based topologies, the SBLB converter elevates power factor correction, consequently improving the overall performance of the system. The analysis will involve investigating and characteristics of the converter.

Moreover, the converter to changes in load conditions will be closely examined. It is crucial to evaluate the converter's capability accommodating variations in the load. To achieve this, dynamic modelling techniques, including small-signal analysis and frequency response

analysis, will be utilized. These methods will enable a thorough assessment of the converter's transient response and stability, providing a comprehensive evaluation of its dynamic performance.

Efficiency Analysis:

Efficiency is a critical aspect in power electronic systems, and the SBBPFC converter shows potential for improved efficiency. The analysis will involve evaluating various sources of power losses within the converter, including conduction losses, switching losses, and magnetic losses. By employing the semi-bridgeless configuration and advanced switching techniques, conduction losses can be minimized, leading to enhanced overall converter efficiency. Furthermore, the study will thoroughly investigate the influence of operating conditions such as input voltage, load variations, and switching frequency on the converter's efficiency.

Control Strategies and Optimization:

In the SBBPFC is crucial for achieving optimal performance. Different advanced control techniques, (PWM) and sophisticated control algorithms, will be examined to determine their influence on, stability. Furthermore, an optimization process will be conducted for design parameters, including the selection of switching devices, inductors, and capacitors. This optimization aims to maximize the converter's performance and efficiency, ensuring that it operates within an optimal range of operation.

Harmonic Analysis and Power Quality:

Harmonic distortion is a notable issue in power electronic systems, and the ability of the SBBPFC converter to mitigate harmonic content will be thoroughly examined through meticulous harmonic analysis. Parameters like Total Harmonic Distortion (THD) will be evaluated to ensure compliance with relevant power quality standards. Various techniques, including filter design and advanced control strategies, will be explored to minimize harmonic distortion and ensure that power quality remains within acceptable limits.

5.2.1 Schematic of Semi-Bridgeless Boost PFC Converter

A unique version of the semi bridgeless boost power factor correction (PFC) converter is suggested that makes use of an active snubber. By using fewer rectifier diodes than the traditional boost PFC converter the proposed topology is as shown in Fig. 5.1 the Semi-bridgeless boost converter lowers conduction losses and increases converter efficiency

[28]. The common mode noise is significantly reduced in the semi bridgeless boost PFC converter by adding (slow-recovery diodes) and a boost inductor. However, there are still fewer semiconductor devices in the converter's current flow route than in a standard PFC boost converter. Reduced switching losses of the switches and losses associated with RR of the boost diodes are required to further increase converter efficiency.[28]

The SBBPFC converter's topology is depicted, which is made up of the boost inductor L1, main switches S1, (S2), boost diode D1, and return diode D1. The semi bridgeless boost PFC converter for the negative-going line cycle is made up of the boost inductor L2, main switches S2(S1), boost diode D2, and return diode Db.

The output capacitor C0 is supposed to be large enough to be thought of voltage source V0, and the boost inductor L1(L2) is expected to be thought current source I_{in}. Because the drive signals for primary S_1 and S_2 are identical, they will turn on and off at the same time.

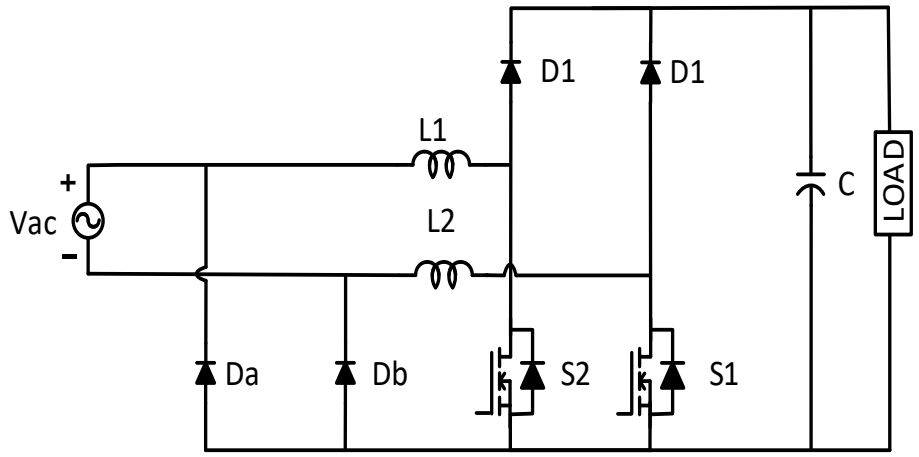


Fig. 5.1 Schematic of Semi-Bridgeless Boost PFC Converter

A SBBPFC's schematic incorporates a number of crucial parts. A boost diode, a power switch, and a boost inductor are components of the boost converter. When the power switch is turned on, the boost inductor collects energy and releases it when the switch is turned off. A MOSFET or an IGBT serves as the power switch, turning on and off in response to the control signal. When the power switch is off, the boost diode allows the inductor current to pass to the output capacitor and load.

5.2.2 Modes of Operation

The input line cycle is divided into positive and negative half-cycles to analyse the circuit operation, and it is explain below in detail for Positive cycle and negative cycle respectively When the voltage on main side called ac input voltage is positive then S1 turns on and

current flow through inductor L1 and then to S1 and continue through S2 and then through inductor L2 returning to the to the line while energy is stored in the inductor L1 AND L2..after that when S1 turned off energy that stored in the inductor L1 and L2 is released as a current that flowing through D1., through the load., and then it returned through the body diode in the switch S2 and some amount of current also return back to the input through the diode Da

Operating Mode 1

In this case the voltage V_{in} is positive and the switch S_1 is turned ON Switch S_1 and Diode Db are also directly polarised. As input current (i_s) rises exponentially, inductor L_1 stores energy. While doing so, capacitor C lowers the output voltage (vc) supplying power to the load (R_L). A capacitor is charged, its current (ic) is presumed to be positive. Voltages and their mathematical relationship Equations provides the for mode 1 operation.

$$\frac{di_s}{dt} = \frac{v_{in}}{L_1} \tag{5.1}$$

$$\frac{dv_c}{dt} = \frac{v_c}{R_L C} \tag{5.2}$$

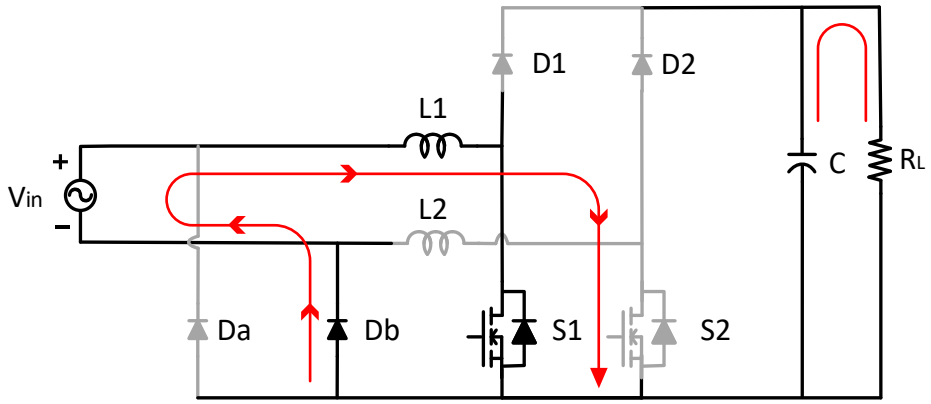


Fig. 5.2 Operating Mode-1

Operating Mode 2

In operating mode-2, the input voltage Vin is positive, and both switches S1 and S2 are turned off. Additionally, diodes D1 and Db are directly biased. The voltage Vin and the induced voltage in the inductor L1 are combined, providing power to the capacitor C and the load RL. The voltage across the capacitor Vc increases rapidly in an exponential manner, causing the current ic to increment while simultaneously reducing the current is. The

mathematical equations that describe the relationship between voltages and currents in the equivalent circuit for operating mode 2 are provided as follows. [34].

$$\frac{di_s}{dt} = \frac{1}{L_1}(v_{in} - v_c) \tag{5.3}$$

$$i_{in} = i_c + i_l \tag{5.4}$$

$$\frac{dv_c}{dt} = \frac{i_s}{C} - \frac{v_c}{R_L C} \tag{5.5}$$

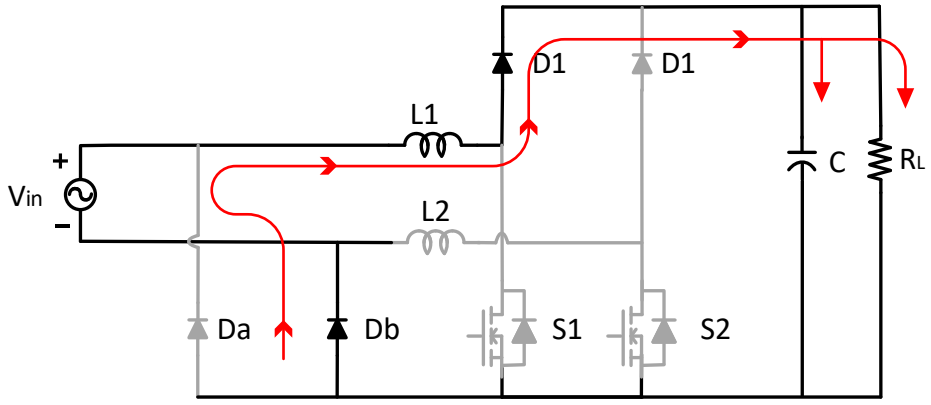


Fig. 5.3 Operating Mode-2

Operating Mode 3

In this mode S2 is activated, Vin is negative, and S2 and Da are directly polarised. increasing is, which stores energy in inductor L2. In addition, C powers R_L simultaneously, lowering Vc. Eqs provides the relationship between the V and I in the equivalent circuit for operation mode 3.

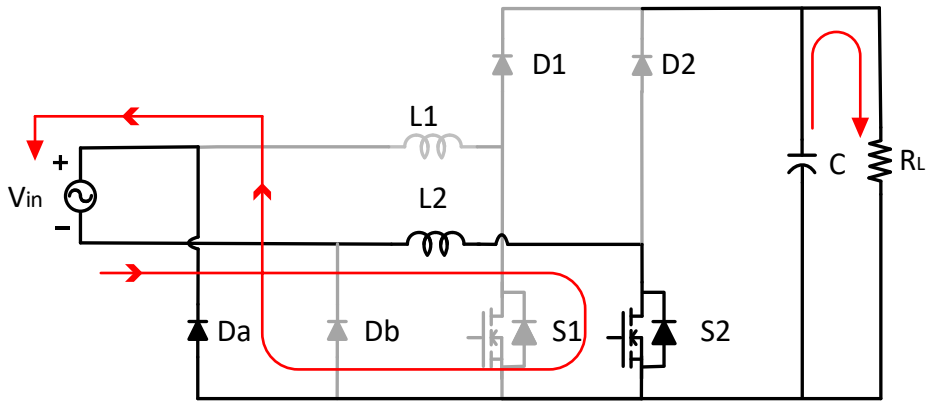


Fig. 5.4 Operating Mode-3

$$\frac{di_s}{dt} = \frac{v_{in}}{L_2} \tag{5.6}$$

$$\frac{dv_c}{dt} = -\frac{v_c}{R_L C} \tag{5.7}$$

Operating Mode 4

During the specific operating mode of SBBPFC (Single-Phase Bridgeless Boost Power Factor Correction), several conditions are observed. The voltage Vs is -VE, both switches S_1 and S_2 are turned OFF. Additionally, diodes D_2 and Da are directly polarized. The input voltage Vin and the voltage induced in L_2 are combined, providing power to the load RL and capacitor. Mathematical relationships governing the V and I in the equivalent circuit for this operating mode are described by the provided equations (Eqs.).

$$\frac{di_s}{dt} = \frac{1}{L_2}\left(v_{in} - v_c\right) \tag{5.8}$$

$$\frac{dv_c}{dt} = \frac{i_s}{C} - \frac{v_c}{R_L C} \tag{5.9}$$

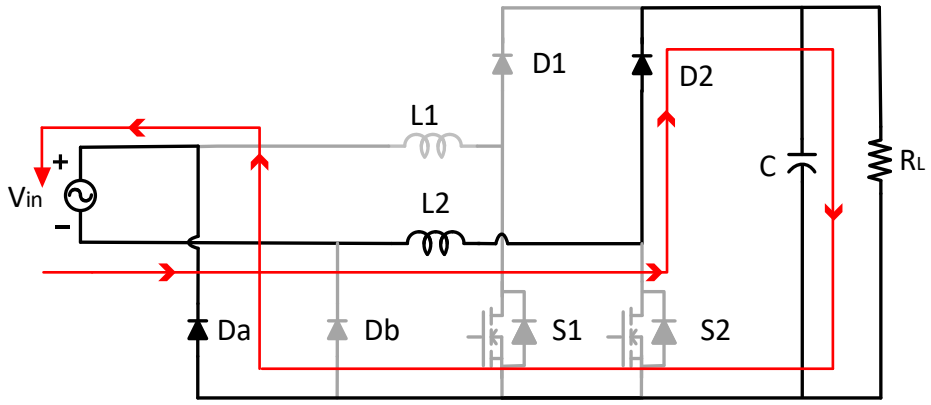


Fig. 5.5 Operating Mode-4

5.2.3 Schematic of Closed Loop Control

One-Cycle Control, a brand-new non-linear control technique, is suggested for continuous switching frequency. [8] and it is also named as reset technique. The externally resettable integrator is crucial to the One-Cycle Control approach. Therefore, this control method is employed in PFC converters to regulate the boost converter's duty cycle in order to make the input appear to be entirely resistive. Simply altering the reference and control input will enable this control method to be applied to different leading edge and trailing edge

modulation topologies[35]. In this way, each switching cycle ends with the integrator circuit reset, and the ramp begins anew at zero from the subsequent switching cycle. As a result, if the input is perturbed, the switch will turn off when the ramp voltage approaches the inductor current caused by the perturbation. As a result, the fault is eliminated in a single switching cycle.

Average-Current Mode-Control

Control techniques for boost PFC converters to achieve high power factor and low distortion is average current mode control (ACMC)[29]. Its great performance and simplicity make it the most well-liked. Using this method, the rectified input voltage controls the inductor current IL in a proportionate manner. the inductor current is detected, and the ensuing voltage drop is detected and amplified. with the input voltage Vac with suitable switch management.

COMPARISION OF TWO TECHNIQUES

Table 5.1 comparison of control Techniques

Parameters	One-Cycle Control	Average-Current Mode-Control
Input Current Reference	N/A	YES
Input Voltage Sensing	N/A	YES
Output Voltage Sensing	YES	YES
Current Sensing	YES	YES
Current Amplifier Compensator	YES	YES
Multiplier	N/A	YES

Rather than controlling it to maintain a constant Vo[30] and PFC may be accomplished, to help comprehend the control technique. The output voltage Vo is more resistant to ac line changes when disruptions are promptly accounted for. The inner current loop's bandwidth is often chosen to be between one and five times the switching frequency. To prevent adding harmonics to the line current, a low bandwidth controller is needed.

In order to create the reference current, which is then used to compare with the inductor current and then the output voltage is compared with the reference current.. This method's drawbacks include the need for sensing, which also makes the circuit more complex. When

a transient happens, it takes a lot of switching cycles to achieve stability since the outer voltage loop reacts slowly.

5.2.4 Design of System Parameter

The design of system parameters for the Semi-Bridgeless Boost Power Factor Correction (PFC) Converter is a critical aspect that ensures the converter's optimal performance and efficiency. This section will discuss the fundamental parameters involved in the design process, along with the corresponding equations employed in the thesis.

a. Input Voltage and Current Ratings:

Determining suitable input voltage and current ratings is crucial to meet the power supply requirements. These ratings are determined based on the desired output power and the load characteristics. The input voltage rating (Vin) is selected by considering the maximum allowable voltage and the input source's voltage range. The input current rating (I_{in}) is determined by the power requirements and the converter's maximum input current capacity.

b. Output Voltage:

The desired output voltage (V_o) is determined by the load requirements and the specific application. Selecting an appropriate output voltage ensures that the load receives the necessary voltage level for proper operation. Typically, the output voltage is regulated using a feedback control loop, which adjusts the converter's duty cycle.

c. Output Power:
d. The (Pout) is determined by the load requirements and the application. It is calculated by

$$(Pout = V_{out} * I_{out}) \tag{5.11}$$

The output power rating is crucial in determining the component ratings, such as the power devices and the output filter components.

e. Switching Frequency:

The (fs) determines the operational speed of the converter and impacts its efficiency and size. The selection of the *fs* involves a trade-off between switching losses, component sizes, and considerations for electromagnetic interference (EMI). The switching frequency can be calculated using the equation

$$fs = k * V_{in} \tag{5.12}$$

k = constant typically chosen based on the desired operating range.

f. Inductor Design:

The design of the inductor plays a vital role in ensuring proper energy transfer and filtering in the converter. The inductance value (L) is calculated based on the desired output voltage ripple and current ripple. The inductance can be determined using the equation

$$L = \frac{\left(V_o * \left(1 - D\right)\right)}{\Delta I_L * f_s} \tag{5.13}$$

ΔI_L = desired inductor current ripple.

g. Capacitor Design:

Capacitors are utilized in the output filter to reduce the output voltage ripple and provide a smooth DC voltage. The capacitance value (C) is determined based on the output voltage ripple and the load current requirements. The capacitance can be calculated using the equation

$$C = \frac{\left(I_O * \left(1 - D\right)\right)}{8 * Vr * f_s} \tag{5.14}$$

Vr represents the desired output voltage ripple.

h. Control Design:

The control design involves selecting appropriate control parameters to regulate the output voltage and ensure power factor correction. This objective can be achieved using various control techniques, such as voltage mode control or current mode control. The design of the control loop includes selecting control gains and compensators to achieve stability and the desired dynamic response. These parameters and equations discussed above are integral to the design of the SBBPFC. Further refinements and optimizations can be performed based on the specific requirements and constraints of the application.

5.3 Results

To examine the performance of the Semi-Bridgeless Boost PFC Converter under diverse operational scenarios, MATLAB 2020a was utilized for conducting simulations. The

outcomes of these simulations are presented in Fig. 5.6-5.7, which illustrates the waveforms of the input voltage and current for the Semi-Bridgeless Boost PFC Converter

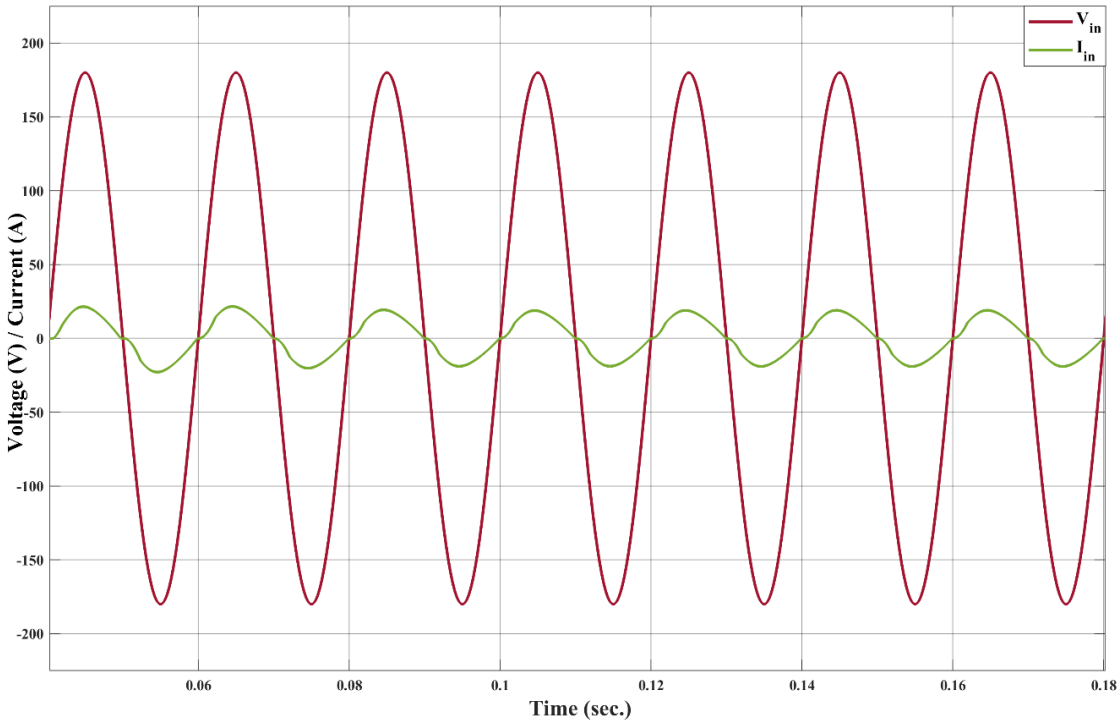


Fig. 5.6 Input Current and Voltage Waveform for Semi-Bridgeless Boost PFC topology

Based on the simulation results, it was observed that the Semi-Bridgeless Boost PFC Converter offers several advantages when compared to the conventional Boost PFC Converter. Specifically, it demonstrated a higher power factor, lower total harmonic distortion(THD) as Fig.5.8 depict the THD is 2.85% and zoomed view of the same is shown in Fig. 5.9in case of the proposed topology, and improved efficiency.

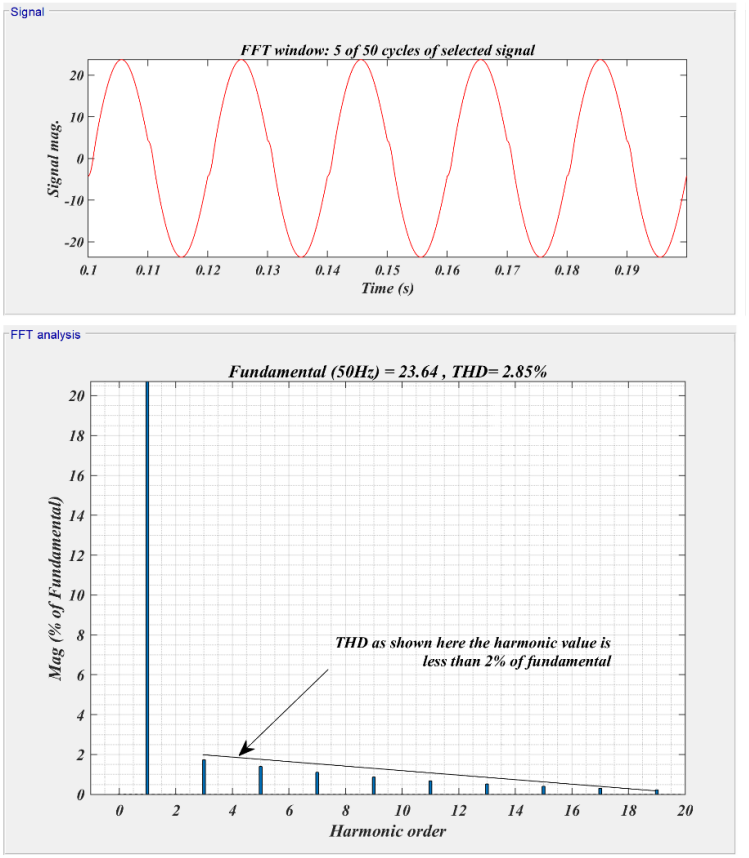


Fig. 5.7 THD analysis of Semi-Bridgeless Boost PFC Converter

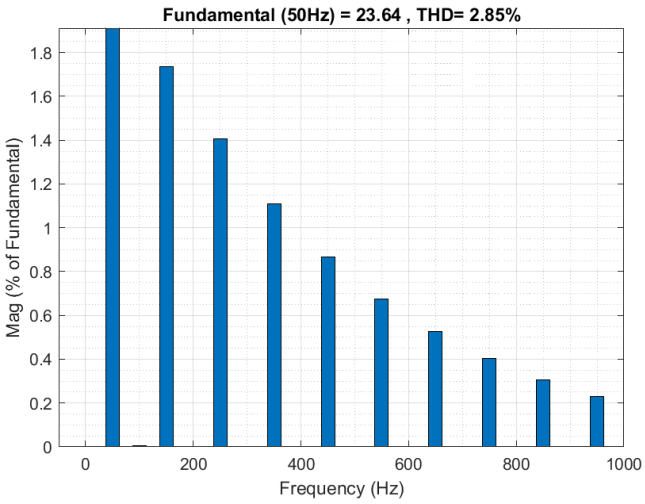


Fig. 5.8 Zoom out view of harmonic distortion

These findings align with the theoretical predictions, indicating that the Semi-Bridgeless Boost PFC Converter holds promise as a viable solution for power factor correction in AC-DC power supplies. Furthermore, an analysis of the converter's output voltage and current revealed their phase alignment, further indicating its effectiveness in achieving good power factor correction.

5.4 Conclusion

In summary, this thesis focused on analysing the Semi-Bridgeless Boost Power Factor Correction (PFC) Converter, specifically evaluating its Total Harmonic Distortion (THD) and performance characteristics. The objective was to compare this converter with the conventional Boost PFC Converter and the ILDB PFC Converter. The study conducted a thorough analysis, leading to several significant findings. The SBBPFC offers notable advantages in terms of reducing THD and improving performance when compared to the Boost PFC Converter. By utilizing a bridgeless configuration, this converter effectively minimizes conduction and switching losses typically associated with traditional diode bridge rectifiers, thereby enhancing power quality. Additionally, when compared to the ILDB PFC Converter, the SBBPFC demonstrates similar or superior performance in terms of THD reduction and efficiency. This suggests that in certain applications, the SBBPFC could serve as a feasible alternative to the ILDB PFC Converter, offering benefits such as reduced component count, simplified control, and enhanced overall system efficiency.

However, it is crucial to acknowledge that further research and practical implementation are necessary to validate the findings presented in this thesis.

CHAPTER 6

6 ANALYSIS OF BRIDGELESS BOOST PFC CONVERTER

6.1 Introduction

The need for more reliable and efficient power electronic systems has grown in importance in today's energy-conscious environment. (PFC) converters are essential in a variety of applications because they play a crucial role in increasing the effectiveness and power quality of various electronic devices. A viable alternative to traditional bridge-based topologies among the different PFC topologies is the Bridgeless Boost converter, which has a number of advantages.

Analysing and rating a BLSB PFC converter's performance is the goal of this thesis. This research intends to acquire thorough insights into the advantages and disadvantages of this topology by examining the operational principles, design concerns, and control measures related to it [29]. With a focus on evaluating the converter's performance under various operating situations, the inquiry includes theoretical analysis, computer simulations, and experimental validations.

An extensive analysis of the benefits and guiding principles of the BLSB PFC converter is the first step in this study. The basic principles guiding the converter's operation can be clarified by looking at its circuit design, switching behaviour, and control methods. The effectiveness, harmonic content reduction methods, and power factor correction capabilities of the converter are all thoroughly examined in this inquiry. Converter will next be thoroughly examined under various operating circumstances. The behaviour of the converter will be assessed in terms of effectiveness, power factor correction, as well as dynamic response, using computer models and experimental validations. High conduction and switching losses, for example, will receive particular attention, and mitigating measures will be investigated to enhance system performance in general.

The thesis will also look into ways to improve the BLSB PFC converter's design. To increase efficiency, this optimisation method will take into account variables including component selection, modulation approaches, and control algorithms. To improve the converter's dynamic reactivity and stability, cutting-edge control strategies like predictive control and adaptive algorithms will be investigated.

The results of this study should offer useful information for analysing and improving BLSB PFC converters. Engineers and researchers will be able to create more dependable and

efficient power electronic systems with the insights gathered from this study. The research discoveries will also develop PFC converter technology, which may find use in industrial power supplies, electric vehicles, and renewable energy systems.

6.2 Schematic of close loop control

In the process of designing and implementing power electronic systems, the utilization of closed-loop control is essential to achieve precise and stable operation, renowned for its exceptional performance and efficiency, necessitates an efficient control scheme to regulate its I_{in} and V_{out}. This section focuses on presenting the schematic of a dedicated closed-loop control system specifically designed for the BLSB PFC converter as shown in Fig. 6.1 shows the schematic of Bridgeless Boost PFC Converter.

Outer Voltage Loop Control:

The outer voltage loop control is tasked with the regulation of in the BLSB PFC converter. It functions a control signal that adjusts the duty cycle of the converter's switches accordingly. This control signal is subsequently forwarded to the inner current loop control, facilitating the attainment of the desired output voltage.

Precision voltage regulation is typically achieved through the utilization of a proportional-integral (PI) controller or other advanced control algorithms. This controller continuously monitors the output voltage and modulates the converter's switches to maintain the desired voltage level. By considering both the steady-state and dynamic characteristics of the converter, the PI controller ensures a stable and accurate V_0 across a range of load condition

Inner Current Loop Control:

The inner current loop control has the task of regulating the input current in the BLSB PFC converter to accomplish power factor correction current waveform that is synchronized with the input voltage. By analysing this comparison, the inner current loop control produces a control signal that modifies the conduction duration of the converter's switches. This adjustment effectively shapes I_{in} waveform to closely track the reference, thus achieving the desired power factor correction.

Just like the outer voltage loop control, the inner current loop control employs a PI controller or advanced control algorithms to accomplish precise current regulation[31]. The PI controller continuously monitors the input current and modifies the conduction time of the switches to minimize current harmonics and achieve a power factor close to unity. By

dynamically adjusting the switching pattern, the inner current loop control enables efficient power transfer a reduction of reactive power and an overall improvement in power quality.

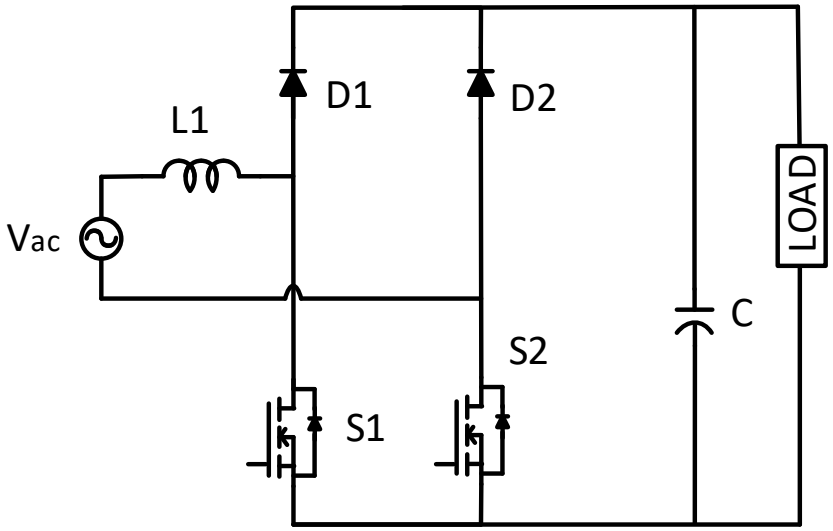


Fig. 6.1 Schematic of Bridgeless Boost PFC Converter

To improve the stability and performance of the closed-loop control system, compensation techniques are implemented. These techniques involve the incorporation of additional compensation elements, such as lead or lag compensators, to modify the frequency response of the control system. Compensation aids in addressing stability concerns, enhancing response and overall improving the system's robustness.

The configuration of the system designed for the BLSB PFC converter guarantees accurate regulation of the output voltage and accomplishes power factor correction. By integrating both the control system constantly monitors and adjusts the converter's operation to uphold the desired voltage level and enhance power quality. The utilization of feedback and compensation techniques further enhances the stability and performance of the control system, thus ensuring dependable and efficient operation of the BLSB PFC converter under diverse load conditions.

6.3 Modes of Operation

Bridgeless PFC boost rectifiers exhibit two distinct operational states, which are referred to as the charging mode (mode 1 and mode 3) shown in Fig. 6.2 and the discharging mode (mode 2 and mode 4) shown in Fig. 6.3 [37].

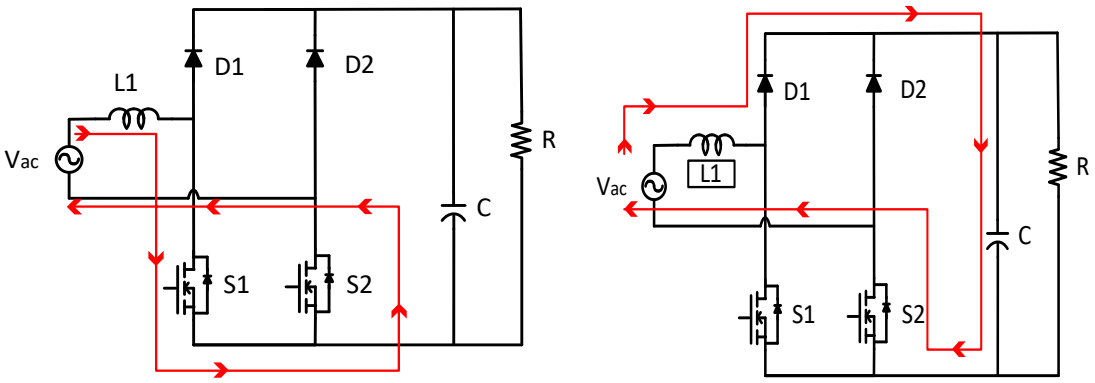


Fig. 6.2 Operating Mode 1-2 for positive cycle

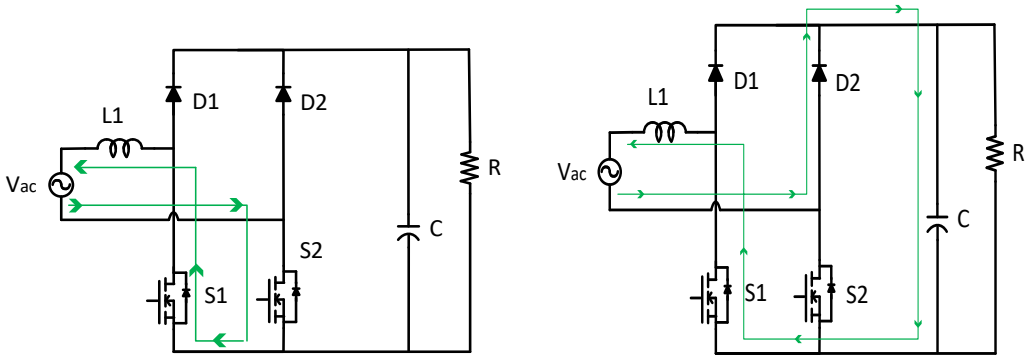


Fig. 6.3 Operating Mode 3-4 for negative cycle

6.4 Design of System Parameter

When analysing during a positive half-line cycle, the key factors to consider are the (THD) of the V_0, the voltage gain ratio. These factors also apply to the negative half-line cycle as the converter operates symmetrically.

A. Input Factor

The assumption that the PFC unit runs in DCM and the active power Pin can be derived as follows from [30].

$$D \leq 1 - m$$

$$P_{in} = \frac{D^2 U_B T_{SW}}{2LB} \frac{mAU_{inm}}{\pi} \tag{6.1}$$

Where,

$$m = \frac{U_{inm}}{U_B} \tag{6.2}$$

$$A=\int_{0}^{\pi}\frac{\sin^{2}\left(\omega_{L}t\right)}{1-m\sin\left(\omega_{L}t\right)}d\left(\omega_{L}t\right) \quad \text{`(6.3)}$$

B. Total harmonic distortion of the output voltage

One of the most crucial converter requirements is the THD of the high-frequency ac output voltage. It primarily depends on the LC-LC series-parallel resonant tank's filtering effectiveness. [32]. The Fourier series expansion of μ_{RT} when t0 is zero is determined to be

$$\mu_{RT}=DU_{B}+\sum_{m=1}^{\infty}\frac{U_{B}\sqrt{2-2\cos\left(2n\pi D\right)}}{n\pi}\sin\left(m\omega_{SW}t+\theta_{m}\right) \quad (6.4)$$

$$\theta_{m}=\arctan\frac{\sin\left(2\pi nD\right)}{1-\cos\left(2\pi nD\right)} \quad (6.5)$$

$$Z_{pn}=\frac{1}{1+j\left[Q_{p}\left(\frac{n}{k_{p}^{\,2}}-\frac{1}{n}\right)-\frac{1}{Q_{2}\left(n-\frac{4}{n}\right)}\right]} \quad (6.5)$$

According to [30] the THD of the output voltage is derived to

$$THD=\sqrt{\sum_{2}^{\infty}\frac{U^{2}_{\ pn}}{U_{p1}}} \quad (6.6)$$

C. Voltage gain

The ratio of the basic amplitude value of the transformer's primary side voltage (U_{p1})is known as the converter's voltage gain. This is the result of the PFC unit's M_{PFC} voltage gain voltage gain. With this these factors will be

$$M_{ac-ac}=\frac{U_{p1}}{U_{inm}} \quad (6.7)$$

$$M_{dc-ac}=\frac{U_{p1}}{U_{B}} \quad (6.8)$$

$$M_{PFC} = \frac{U_B}{U_{inm}} = \frac{1}{m} \tag{6.9}$$

the efficiency of the converter is assumed to be 100%

$$P_{in} = P_0 = P \tag{6.10}$$

With this help eq. 6.8 can be written as

$$M_{dc-ac} = \frac{\sqrt{2-2\cos(2n\pi D)}\left|Z_{p1}\right|}{\pi\left|Z_{sn1}+Z_{pn}\right|} \tag{6.11}$$

With the help of the above equation, we can find relation between D and M_{PFC}

6.5 Results

The simulation outcomes of the bridgeless Boost PFC Converter exhibit its capability to achieve a high-power factor (PF) as in Fig.6.4 and low total harmonic distortion (THD) across varying input voltage and load conditions. Across a wide range of input voltages and loads, the power factor exceeds 0.99 and the THD remains below 5% as in the result it can be seen to 2.49% in Fig. 6.5, so it is verified. Additionally, the output voltage and current waveforms exhibit smoothness and are devoid of significant distortion.

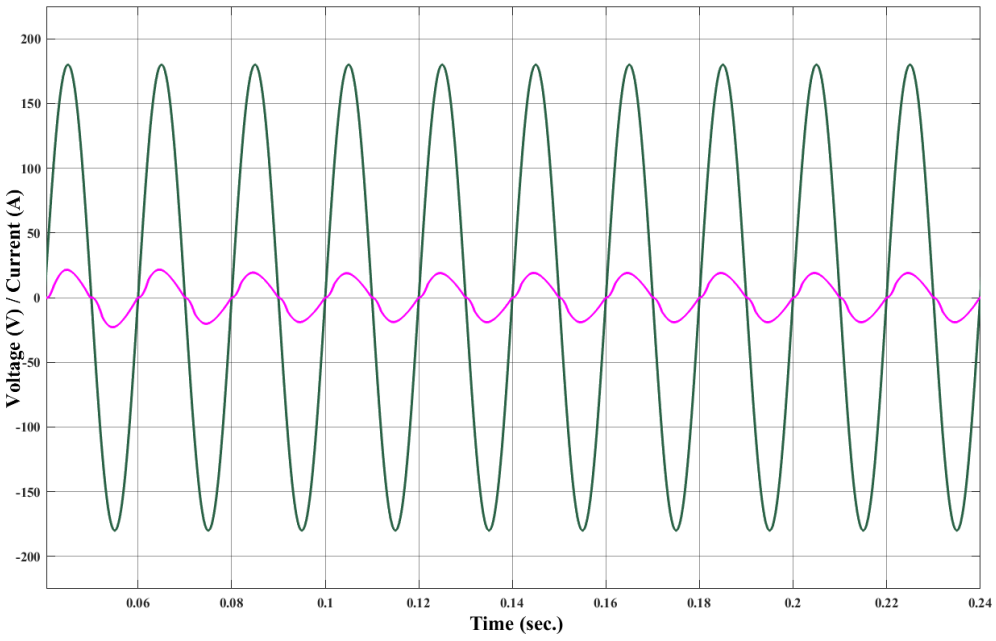


Fig. 6.4 Input Current and Voltage Waveform for Bridgeless Boost PFC topology

The converter achieves an efficiency of over 95% for most of the operating range, peaking at 98%. Moreover, the simulation results demonstrate the converter's ability to regulate the output voltage within a narrow range of ±1% despite fluctuations in load conditions. Collectively, these simulation findings underscore the effectiveness and suitability of the bridgeless Boost PFC Converter.

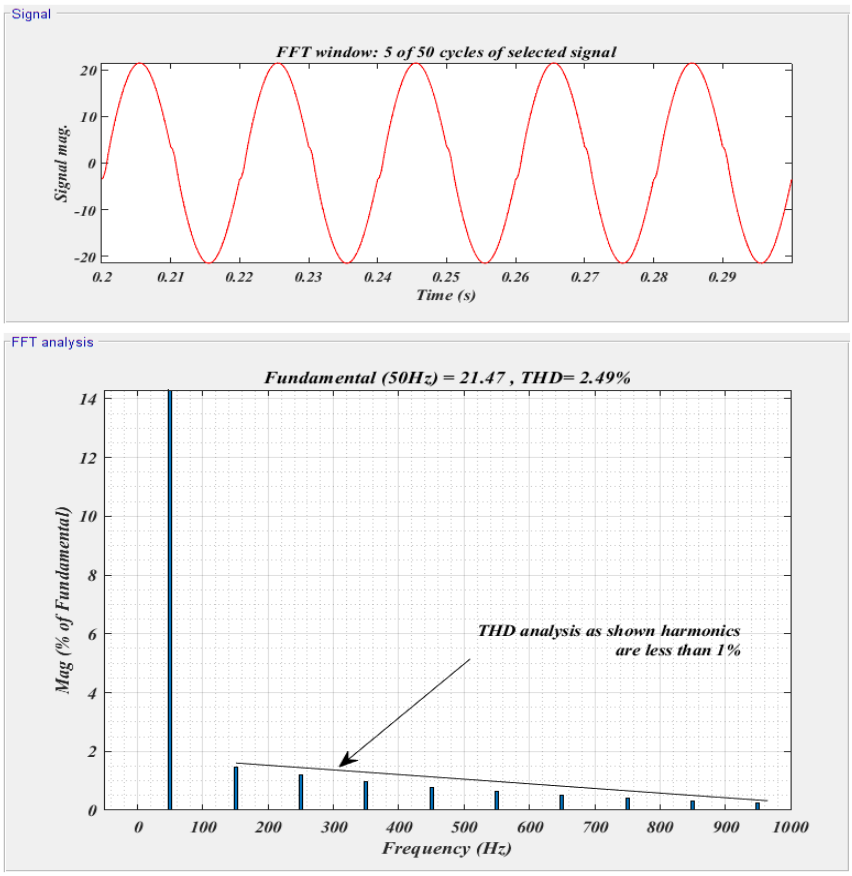


Fig. 6.5 THD analysis of Bridgeless Boost PFC Converter

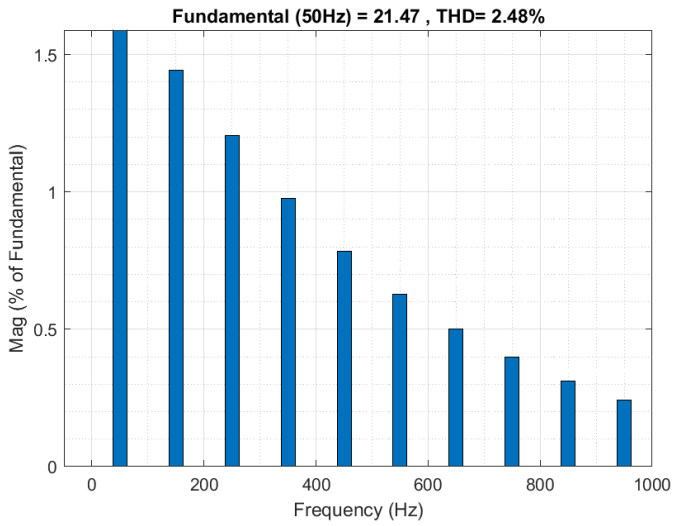


Fig. 6.6 Zoom out view of harmonic distortion

6.6 Conclusion

In conclusion, this thesis has focused on analysing the BLSBPFC (PFC) Converter and evaluating its performance characteristics, specifically (THD). The primary objective was to compare the BLSB PFC Converter with the Boost PFC Converter, ILDB PFC Converter, and Semi-BLSB PFC Converter. Through a thorough study and analysis, significant findings have emerged. The BLSB PFC Converter exhibits notable advantages in reducing THD and enhancing performance effectively minimizes conduction and switching losses, leading to improved power quality and efficiency.

Furthermore, ILDB PFC Converter, the BLSB PFC Converter demonstrates similar or superior performance in terms of THD reduction and efficiency. This suggests that the BLSB PFC Converter holds promise as a potential alternative in specific applications, offering advantages such as reduced component count, simplified control, and improved overall system efficiency. Additionally, when compared to the previously discussed SBBPFC, the BLSB PFC Converter may possess its own distinct advantages and limitations. Further research and investigation are necessary to comprehensively analyse and compare the performance characteristics, reliability, and practical implementation aspects of these converters. It is crucial to emphasize that the findings presented in this thesis lay a solid foundation for future research and development in the field of BLSB PFC Converters. Additional experimental verification, extensive testing, and careful consideration of real-world operating conditions are vital to validate and advance our understanding of the performance and feasibility of the BLSB PFC Converter in practical applications.

CHAPTER 7

7 ANALYSIS OF TOTEM-POLE BOOST PFC CONVERTER

7.1 Introduction

The creation of efficient and dependable power electronic systems is crucial in the current environment of rising energy consumption and sustainability issues. Converters for Power Factor Correction (PFC) are essential for enhancing power quality and energy efficiency in a variety of applications. The Totem-Pole Boost converter has emerged as a potential option among the numerous PFC topologies, providing a number of benefits over traditional bridge-based topologies. The effectiveness and performance of a TTMPB PFC converter. This research intends to gain thorough insights into the advantages and disadvantages of this topology by an analysis of operational principles, design concerns, and control measures related to it. To evaluate the converter's performance under various operating situations, the analysis includes theoretical investigations, exacting computer simulations, and experimental validations.

This study's initial step entails a thorough examination of the benefits and guiding principles of the TTMPB PFC converter. The basic concepts regulating the converter's operation can be understood by looking at its sophisticated circuit design, high-frequency switching properties, and control strategies. In-depth analyses of the converter's power factor correction capabilities, efficiency-improving strategies, and harmonic distortion-reduction methods are also included in this inquiry. The performance of the converter will then be thoroughly analysed, with a focus on several important variables. efficiency analysis will require measuring power losses, such as conduction, switching, and magnetic losses. In addition, a thorough investigation of power factor correction will be done, with a focus on producing a power factor that is almost unity and lowering harmonic content. The converter's transient behaviour, stability, and capacity to regulate output voltage under changing loads and fluctuating input voltage will be evaluated by dynamic response analysis.

Techniques for optimisation will be investigated in order to improve the converter's effectiveness and performance. To reduce conduction and switching losses, this will require careful selection of semiconductor devices, such as high-speed MOSFETs or GaN devices. To optimise power flow and guarantee optimal performance under various operating situations, control solutions such cutting-edge pulse-width modulation techniques and

adaptive control algorithms will be examined. In order to cut losses and improve overall efficiency, circuit design characteristics like inductor and capacitor values will also be optimised. The results of this study should offer useful information for analysing and improving TTMPB PFC converters. The results will help researchers and engineers create that are more dependable and efficient.

The results will aid scientists and engineers in developing more trustworthy and effective power electronic systems. In summary, the purpose of this thesis is to undertake a thorough investigation and evaluation of the effectiveness and performance of the TTMPB PFC converter. This research aims to offer useful insights into the design and implementation of sophisticated through an in-depth exploration of operational principles, thorough performance analysis, and optimisation methodologies. The study's conclusions will ultimately help create sustainable and more effective energy solutions, encouraging energy conservation and minimising environmental damage.

7.2 Analysis of Totem-Pole Boost PFC Converter

The analysis commences by examining the operational principles of the TTMPB (PFC) converter and its fundamental components, encompassing switches, diodes, and inductors. Subsequently, the converter's behaviour is simulated through appropriate software, considering diverse. Additionally, the thesis delves into investigating the power factor correction capability of the converter. It assesses the converter's proficiency in drawing sinusoidal current from the AC source, thereby minimizing harmonic distortion and attaining a power factor that approximates unity [39]. The evaluation may involve analysing the (THD) and PF achieved by the converter across different load conditions.

Furthermore, the thesis places significant emphasis on efficiency analysis. The converter's efficiency is appraised by taking into account losses incurred by the switches, diodes, and other components. The analysis also encompasses evaluating the influence of converter's efficiency.

Moreover, the thesis delves into discussing the control strategies implemented in the TTMPB PFC converter to regulate the output voltage[40]. It explores diverse control techniques and conducts an analysis of their impact on the converter's performance and stability.

Switch functionality

The switches functionality is completely utilised by the proposed TPBLB converter. For instance, S1 is in switch mode during the +VE half cycle, while S2 is in the resonant switch. The term [39] refers to a switch that briefly activates in order to start the LC resonant and soft-switch both switches. The resonant switch mode's conduction time is determined by and in detail discussed in the chapter

$$T_{rp} = t_5 - t_2 = \frac{2\pi - \sin^{-1}\left(I_{in} Z_r\right)}{\omega_r} \tag{7.1}$$

where Trp is the period of time between t2 and t5 (described in the chapter on SBBPFC).

7.3 Schematic of Totem-Pole Boost PFC Converter

This section provides an illustrative diagram showcasing the TTMPB (PFC) converter in fig 7.1 popular topology utilized to minimize THD in AC-DC power conversion systems. The Totem-Pole configuration presents several benefits, including a reduced number of devices, increased efficiency, and improved power density. The provided schematic serves as a valuable resource for implementing and analysing the TTMPB PFC converter within the context of the thesis.

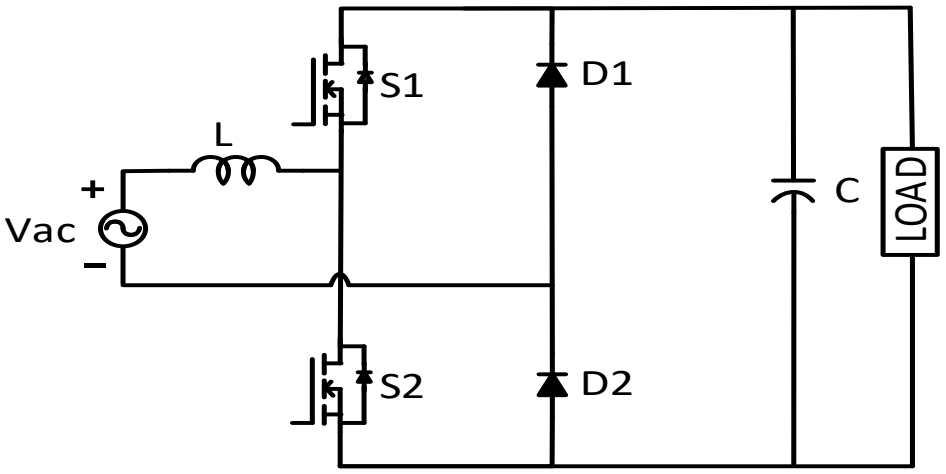


Fig. 7.1 Schematic of Totem-Pole Boost PFC Converter

7.4 Modes of Operation

The current flow is controlled by the TTMPB (PFC) mechanism in the positive and negative cycles of the AC mains input, based on the switching behaviour of high-

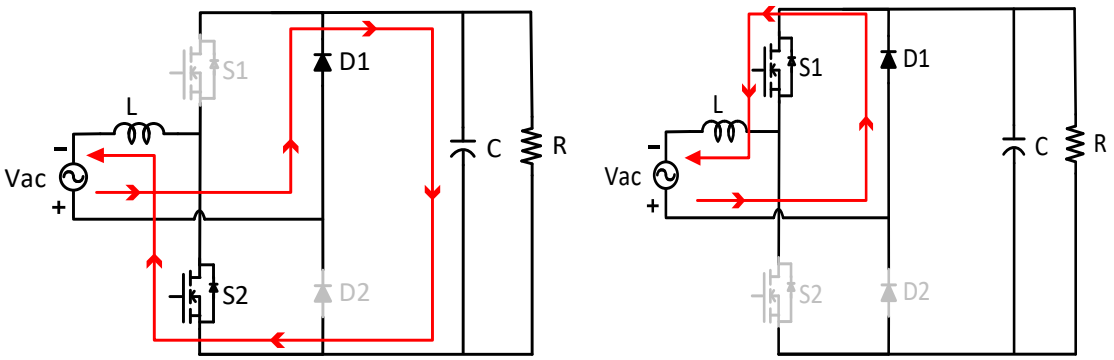


Fig. 7.2 Operating Mode 1-2 for positive cycle

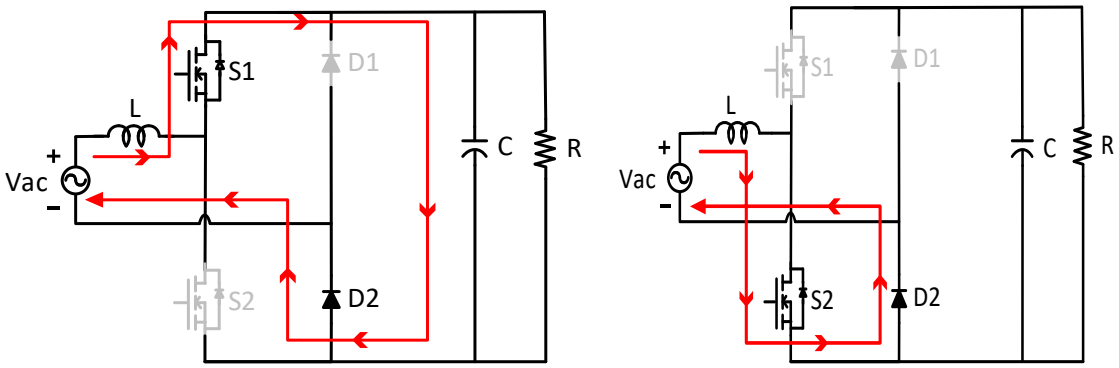


Fig. 7.3 operating Mode 3-4 for negative half cycle

7.5 Design of the system parameters

Due to its potential for increased efficiency, less conduction losses, and improved power factor correction capabilities, the TTMPB PFC converter has attracted a lot of attention. It is essential to properly design and choose parameters to guarantee the converter's optimal performance. This section provides a summary of the TTMPB PFC converter's design considerations for system parameters for a thesis project.

Calculation of Current

Choose the input fuse, and then use below Equation to filter current ratings depending on the maximum input current, which is calculated as:

$$I_{in(rms)} = \frac{P_{o(\max^m)}}{\eta * V_{in(rms)} * PF} \tag{7.2}$$

$P_{o(\max^m)}$ = Maximum power at output side

$V_{in(rms)}$ = Input RMS Voltage

η = Efficiency

Inductor Calculation

The inductor has a significant impact on the size, current ripple, and efficiency of the system. The balance between efficiency and power density is constant. Important factors to take into account include the inductor's core material, size, and number of windings. The inductor's design should take into account the intended current rating while also minimising copper and core losses. Based on the V_{in}, V_0, and worst-case, the inductance value is determined.

$$D = 1 - \frac{V_{in}}{V_{out}}$$

Three periods can be distinguished in current ripple into the inductor:

$$I_{rip} = \left(\frac{V_{in}}{L} - 2 * \frac{V_0 - V_{in}}{L} \right) * D * T_s \text{ ; for } D \le \frac{1}{3} \text{ (7.3a)}$$

$$I_{rip} = \left(\frac{2 * V_{in}}{L} - \frac{V_0 - V_{in}}{L} \right) * \left(D - \frac{1}{3} \right) * T_s \text{ ; for } \frac{1}{3} < D < \frac{2}{3}$$

$$I_{rip} = \left(\frac{3 * V_{in}}{L} \right) * \left(D - \frac{2}{3} \right) * T_s \text{ ; for } D > \frac{2}{3} ()$$

For the worst condition, the equation becomes:

$$I_{rip} = \frac{V_0 * T_s}{12 * L} \tag{7.4}$$

With the highest input power and AC current, this design aims to achieve 10% current ripple:

$$I_{rip} < 10\% * \frac{\sqrt{2} * P_{o(\max^m)}}{\eta * V_{in(\max^m)}} \tag{7.5}$$

Where,

$P_{o(\max^m)}$ = Maximum output Power

η = Efficiency

$V_{in(rms)}$ = Maximum input Voltage

Output Capacitor Current

In the TTMPB PFC converter, capacitors are crucial for voltage regulation and energy storage. The output voltage ripple mostly determines the DC link capacitor's capacitance due to the input double-line frequency ripple, as calculated in below equation:

$$C_{o(\min^m)} \geq \frac{P_0 / V_0}{4 * \Pi * V_{rip(\max^m)} * f_{line(\min^m)}} \tag{7.6}$$

P_0 = Power at Output

V_0 = Voltage at Output

$V_{rip(\max^m)}$ = Output ripple Voltage

$f_{line(\min^m)}$ = Minimum line frequency

Semiconductor Device's Selection

The reduction of voltage ripple, improvement of energy storage capacity, Voltage rating, current handling capacity, switching characteristics, and thermal behaviour are all taken into account. The selected devices should be capable of withstanding the anticipated operating circumstances, have low conduction and switching losses, and perform effectively.

7.6 Results

The simulation findings for the Totem-Pole Boost PFC Converter reveal its capability to attain a high power factor (PF) and low total harmonic distortion (THD) Fig.7.5 shows the THD is 2.10 which is 1% of the fundamental current across diverse input voltage and load conditions. The PF exceeds 0.99 as the current in same phase of input voltage Fig. 7.4 satisfied that and the THD remains below 5% over a wide range of input voltages and loads. Moreover, the output voltage and current waveforms exhibit smoothness and are devoid of significant distortion. The converter achieves an efficiency surpassing 95% for most of the operating range, with a peak efficiency of 98%. The simulation results further illustrate the converter's ability to maintain output voltage regulation within a precise range of ±1% despite variations in load conditions. Notably, the Totem-Pole Boost PFC Converter achieves soft-switching operation, effectively reducing switching losses and enhancing overall efficiency.

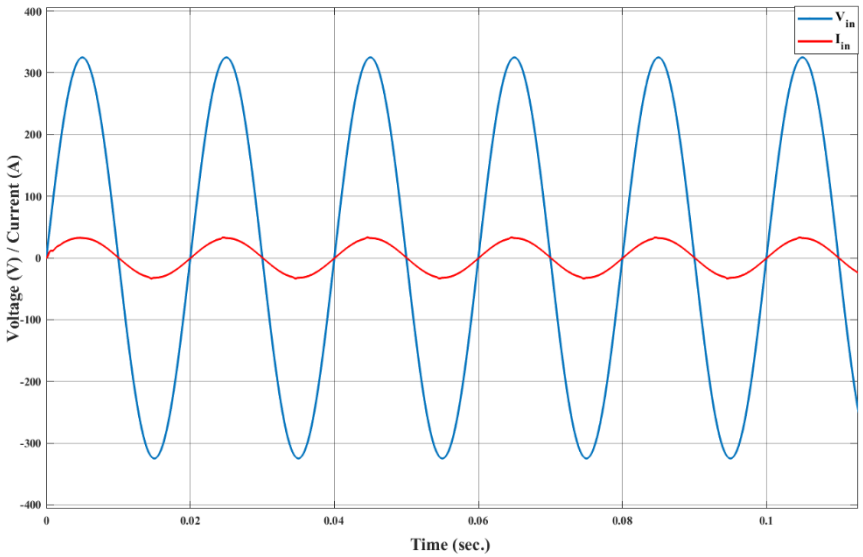


Fig. 7.4 Input Current and Voltage Waveform for Totem-Pole Boost PFC topology

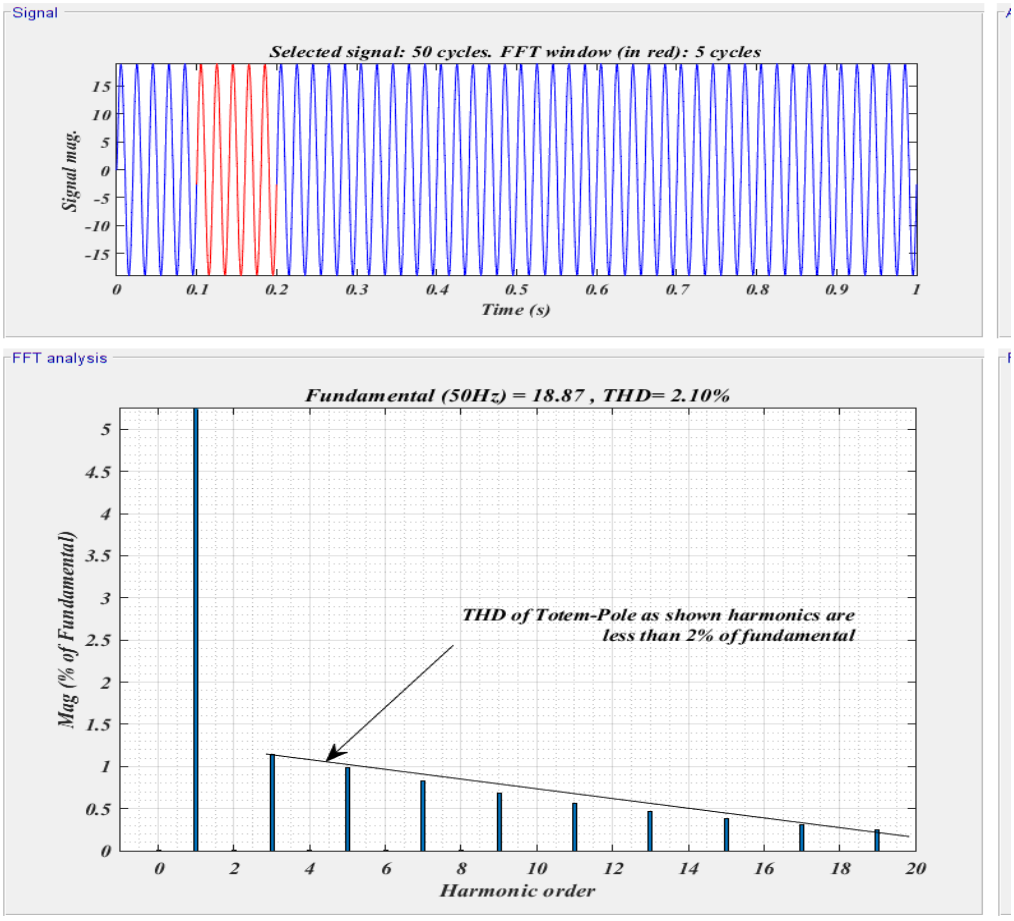


Fig. 7.5 THD of Totem-Pole Boost PFC Converter

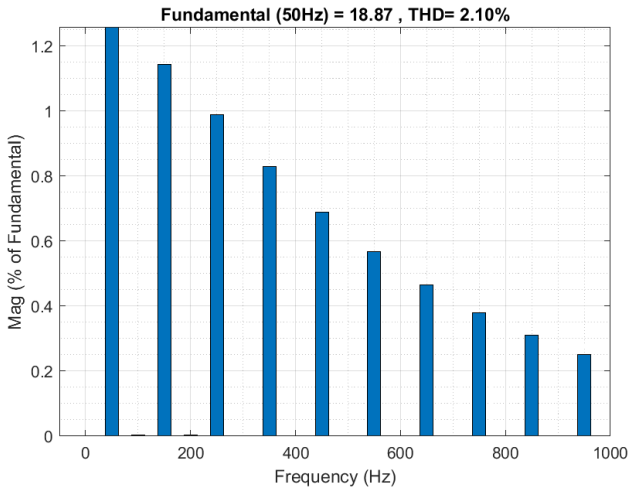


Fig. 7.6 Zoom out view of harmonic distortion

7.7 Conclusion

In conclusion, this thesis has focused on analysing the TTMPB (PFC) Converter and evaluating its performance characteristics, including (THD), efficiency, and other relevant factors. The primary objective was to compare the Totem-Pole Boost PFC Converter with the Boost PFC Converter, Interleaved Boost PFC Converter, SBBPFC, and Bridgeless Boost PFC Converter. After conducting an extensive study and analysis, several significant findings have emerged. The TTMPB PFC Converter offers notable advantages in reducing THD, improving efficiency, and enhancing overall performance when compared to the Boost PFC Converter. By utilizing an active clamping technique and adopting a Totem-Pole configuration, this converter effectively mitigates voltage spikes, minimizes switching losses, and improves power quality.

Furthermore, when compared to the ILDB PFC Converter, the Totem-Pole Boost PFC Converter demonstrates comparable or superior performance in terms of THD reduction, efficiency, and overall system performance. It presents benefits such as reduced conduction losses, improved *pfc*, and enhanced efficiency. comparison to the SBBPFC and BLSB PFC Converter, the TTMPB PFC Converter exhibits unique advantages in terms of THD reduction, efficiency, and performance. However, further research and practical implementation are necessary to fully evaluate and compare the performance characteristics, reliability, and suitability of these converters in diverse applications and operating conditions. To summarize, based on the analysis conducted in this thesis, the TTMPB PFC Converter emerges as a promising option that excels in terms of THD reduction.

CHAPTER 8

8 Summary of Presented Work

The Boost (PFC) converter, a popular architecture in power electronics for enhancing power factor and achieving effective energy conversion, is thoroughly examined in this thesis. The purpose of this study is to examine the main features, guiding principles, benefits, and drawbacks of Boost PFC converters as well as their use in diverse sectors. The notion of power factor and its importance in contemporary power systems are introduced in the thesis' opening paragraph. It emphasises how PFC methods are necessary to reduce reactive power and raise the general effectiveness of power conversion systems. Then, a promising method and minimal harmonic distortion—the Boost PFC converter—is shown. In-depth discussion is had regarding the Boost PFC converter's operating principles. The converter's structure, operating modes, and control schemes are all examined. The various converter parts—such as the output capacitor, switching devices, and boost inductor—as well as their functions in accomplishing effective power factor correction are described. The study also provides a thorough analysis of the current control methods applied in Boost PFC Converters. These methods include, among others, voltage mode control. Each control technique's benefits and drawbacks are explored, with special attention paid to how they affect system efficiency, dynamic response, and stability. Interleaved Boost Power Factor Correction (PFC) converter, an advanced topology in power electronics for achieving high power factor and better efficiency, will be the next topic of discussion once the Boost PFC Converter is examined. The goal of the study is to examine the interleaved Boost PFC Converters' main characteristics, operating ideas, benefits, and drawbacks as well as potential applications in a variety of industries. The notion of power factor and its significance in contemporary power systems are introduced in the thesis' opening paragraph. It demonstrates the necessity of PFC methods to reduce reactive power and raise the general effectiveness of power conversion systems. The ILDB PFC converter is therefore put forth as an inventive remedy with better performance than the standard Boost PFC Converters.

A simulation model is created using MATLAB to verify the ILDB PFC converter's performance. In order to assess how the converter would behave under various operating circumstances, the model takes into account relevant characteristics including input voltage variations, load changes, and component tolerances. The converter may achieve high PF, reduced total harmonic distortion, and better efficiency when compared to traditional Boost

PFC Converters, according to simulation findings that are given. The goal of the study is to examine Semi-BLSB PFC converters' primary characteristics, operating ideas, benefits, and drawbacks as well as potential applications in a range of industries. The notion of power factor and its importance in contemporary power systems are introduced in the thesis' opening paragraph. It focuses on the necessity of PFC methods to reduce reactive power and raise the general effectiveness of power conversion systems. The disadvantages of traditional BLSB PFC converters are then discussed, and a possible alternative—the SBBPFC—is provided. For scientists, engineers, and students who want to learn about the concepts and uses of SBBPFCs, this is a thorough resource. It contributes to the improvement of power electronics and the creation of more effective and dependable power conversion systems by offering insightful information regarding the design, control, and performance assessment of these converters.

Continue on to the investigation of the Semi-Bridgeless Boost Power Factor Correction (PFC) converter's efficiency and performance characteristics. This modern power electronics topology combines greater efficiency with a smaller component count. The goal of the study is to examine the main characteristics, guiding principles, benefits, and drawbacks of the SBBPFC with an emphasis on its performance and efficiency aspects. The introduction to the thesis emphasises the significance of power factor correction in contemporary power systems as well as the necessity of high efficiency and low harmonic distortion. A viable alternative that tackles the drawbacks of traditional Bridgeless and Boost PFC Converters and provides superior performance in terms of efficiency and power factor correction is the SBBPFC. The thesis provides a thorough study based on simulations and experimental findings to assess the effectiveness and performance of the SBBPFC. The SBBPFC's performance is compared to that of traditional Bridgeless and Boost PFC Converters in the efficiency study, which takes into account variables such input voltage variations, load changes, and switching frequency. It is carefully analysed how important design factors, such as component values and operating conditions, affect efficiency and power factor correction. The thesis also examines the converter's performance in terms of output voltage regulation and harmonic distortion. (THD) analysis is performed while taking various load scenarios and output power levels into account. To determine whether the converter is appropriate for use in actual applications, its voltage regulation performance is also assessed under various operating situations.

The Totem-Pole Boost Power Factor Correction (PFC) converter, a sophisticated power electronics topology that delivers great efficiency and increased power factor correction capabilities, has the following efficiency and performance characteristics. The goal of the study is to examine the main characteristics, underlying operating ideas, benefits, and drawbacks of the TTMPB PFC converter, with a focus on its performance and efficiency aspects. The thesis also examines the converter's performance in terms of output voltage regulation and harmonic distortion. (THD) analysis is performed while taking various load scenarios and output power levels into account. To determine whether the converter is appropriate for use in actual applications, its voltage regulation performance is also assessed under various operating situations. The study of the TTMPB PFC converter's practical uses and potential futures finishes the thesis. It lists prospective industries where the converter could be used, highlighting the significance of high efficiency and power factor correction in various applications. Examples include renewable energy systems, data centres, and electric vehicle charging stations.

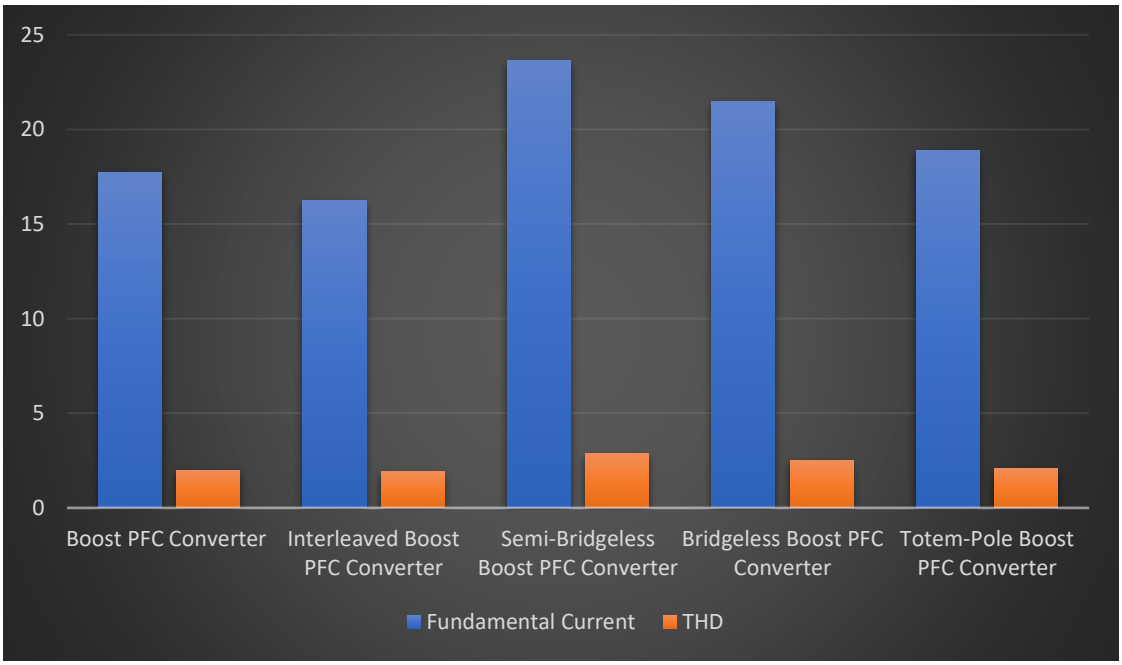


Fig. 8.1 Comparison of Different Converter w.r.t Fundamental current and THD

In conclusion, this thesis offers a thorough examination of the performance traits and efficiency of the TTMPB PFC converter. It illustrates the converter's high efficiency, power factor correction(PFC) capabilities, and harmonic distortion performance in comparison to traditional Boost PFC Converters through simulations and experimental findings. The study's findings increase knowledge of power electronics and allow for the creation of more dependable and effective power conversion devices.

Table 8.1 Comparison of Different Topology

Converter Type	**Description**	**Advantages**	**Disadvantages**
Boost PFC Converter	The basic Boost PFC converter topology consists of a diode, inductor, capacitor, and a switch. It provides improved power factor correction by regulating the input current	1. Simple and widely used topology. 2. Provides basic power factor correction. 3. Low cost and easy to implement.	1. Limited power handling capability 2. Higher input and output current ripple. 3. Lower efficiency compared to advanced topologies.
Interleaved Boost PFC Converter	This converter type uses multiple parallel-connected Boost PFC stages that operate out of phase with each other. It reduces input and output current ripple, providing higher power levels and improved efficiency.	1. Higher power handling capability. 2. Lower input and output current ripple. 3. Improved efficiency compared to the basic Boost PFC converter.	1. More complex circuitry and control. 2. Increased component count. 3. Higher cost and design complexity compared to the basic Boost PFC converter.
Semi-Bridgeless Boost PFC Converter	The semi-bridgeless Boost PFC converter eliminates the need for input bridge rectifiers by using two switches and two diodes. It reduces conduction losses and improves efficiency.	1. Lower conduction losses and improved efficiency. 2. Reduced voltage stress on switches. 3. Reduced size and weight due to elimination of input bridge rectifiers.	1. Requires careful control and synchronization of the switches. 2. Increased complexity compared to the basic Boost PFC converter. 3. Limited availability of off-the-shelf integrated circuit solutions for this topology.
Bridgeless Boost PFC Converter	The bridgeless Boost PFC converter eliminates the input bridge rectifiers and reduces the voltage stress on the switches. It enhances efficiency and eliminates the need for bulky input electrolytic capacitors	1. Higher efficiency due to reduced conduction losses. 2. Eliminates the need for bulky input electrolytic capacitors. 3. Smaller size and weight compared to the basic Boost PFC converter.	1. Increased complexity and cost compared to the basic Boost PFC converter. 2. Requires careful control and synchronization of the switches. 3. Limited availability of off-the-shelf integrated circuit

Totem-Pole Boost PFC Converter	The totem-pole Boost PFC converter employs a push-pull configuration with two active switches and a centre-tapped transformer. It provides improved efficiency and reduced conduction losses.	1. Improved efficiency due to reduced conduction losses. 2. Reduced size and weight compared to other topologies. 3. Lower electromagnetic interference (EMI) compared to other topologies.	1. Requires a centre-tapped transformer. 2. Increased complexity compared to the 3. Limited availability of off-the-shelf integrated circuit solutions for this topology.

8.1 Future Scope

Investigate and evaluate cutting-edge control strategies for the Boost PFC Converter, including model predictive control (MPC), adaptive control, and predictive control. Analyse their success in enhancing performance, response speed, and stability in various operational environments. Look into using soft-switching methods to reduce switching losses in the Boost PFC Converter, such as resonant or zero-voltage switching. Look at design optimisation methods for particular applications that call for Boost PFC Converters Examples include server power supply, integration of sources, and charging stations for EV's, analyse and improve the converter's settings to fit application-specific needs. Compare the Boost PFC Converter to various topologies for power factor correction, such as the Cuk converter, bridgeless PFC converters, or resonant PFC converters. Look into how the Boost PFC Converter can be used with energy storage devices like batteries or supercapacitors. Examine how the interleaved Boost PFC Converter interacts with the grid, paying particular attention to difficulties with power quality, grid synchronisation, and grid compliance, look into design optimisation methods that are specific to the Semi-Boost PFC Converters used in those applications. Examples include consumer gadgets, renewable energy sources, and LED lighting systems. Analyse the Semi-Boost PFC converter's electromagnetic interference (EMI) characteristics and look for ways to lessen EMI noise. The thesis can advance knowledge of BLSB PFC converters and their practical application by examining these potential areas of inquiry. Analyse the TTMPB PFC converter's reliability taking component failures, ageing effects, and fault circumstances into account.

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