IN-MEMORY COMPUTATION USING STATIC RANDOM ACCESS MEMORIES

A DISSERTATION REPORT

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I, Stuti, Roll No. 2K21/VLS/23 student of M. Tech (VLSI Design & Embedded system), hereby declare that the project Dissertation titled **"In-Memory Computation using Static Random Access Memories"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is unique and has not been copied without proper citation. This work has never before been used to give a degree, diploma associateship, fellowship, or other equivalent title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"In-Memory Computation using Static Random Access Memories"** which is submitted by **Stuti Singh, 2K21/VLS/23**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a documentation of the student's projectwork completed under my supervision. To the best of my knowledge, this work hasnever been submitted in part or in full for any degree or diploma at this university or anywhere else.

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ABSTRACT

The fundamental tenets of Von Neumann architecture have served as the foundation for a majority of modern digital computing systems. In traditional Von Neumann systems, data is stored in separate memory units, and instructions are fetched and executed one at a time. This sequential nature creates a significant delay between instruction fetch, data access, and execution, leading to reduced system performance. The Von Neumann architecture has revealed bottlenecks that hinder system performance and efficiency. These include the Von Neumann bottleneck, caused by sequential processing of instructions and data, and the limited bandwidth between the CPU and memory. In order to overcome these bottlenecks, In-Memory Computing (IMC) has emerged as a promising solution. IMC leverages the parallelism and proximity of data and computation within memory, enabling faster and more efficient processing. It reduces data transfer requirements, alleviating the Von Neumann bottleneck, and improving overall system performance. IMC involves performing computations directly within memory rather than relying on separate processing units. By adopting this approach, the requirement for data transfer between memory and processor is eliminated, leading to reduced latency and enhanced system performance. In-Memory Computing (IMC) is poised to revolutionize the way we process and analyze data. It eliminates the need for data movement, resulting in unprecedented speed and efficiency. This paradigm shift opens up new possibilities for real-time analytics, large-scale data processing, and complex computational tasks. IMC can accelerate machine learning algorithms, enhance artificial intelligence applications, and enable rapid decision-making in various domains. Additionally, IMC has the potential to reduce power consumption and energy requirements, contributing to greener and more sustainable computing systems. As research and development in IMC progresses, the transformative impact on the future of computing is expected to be profound, paving the way for unprecedented capabilities and advancements in data-driven technologies

The significance of SRAM for In-Memory Computing (IMC) cannot be overstated. It serves as the primary storage medium for data and computation, allowing fast and direct access to data. It also exhibits low power consumption, making it ideal for energy-efficient computing systems. It also offers high-density storage, allowing large amounts of data to be stored in a compact memory array. Overall, SRAM is a key component for realizing the potential of in-memory computing.

The use of 8T SRAM cells for In-Memory Computing (IMC) has gained significant attention due to their unique characteristics and benefits. These cells offer advantages over traditional 6T SRAM cells, such as improved stability, reduced read-disturb failures, and increased noise immunity. They enable efficient and reliable storage of data while supporting computational operations within the memory array, minimizing data movement and reducing latency. The use of 8T SRAM cells in IMC architectures can lead to enhanced system performance, reduced power consumption, and increased efficiency. Additionally, the scalability and compatibility of 8T SRAM cells with existing fabrication technologies make them a viable option for integrating IMC into various computing systems. As research and development in IMC continue to advance, the use of 8T SRAM cells is expected to play a crucial role in unlocking the full potential of in-memory computing.

Through this work, I present an approach to In-memory computing that uses SRAM cells and is capable of processing Boolean operations in addition to the standard storage operations. The boolean computations, including NOR, OR ,NAND AND, XOR, are accomplished through the utilization of an 8T SRAM cell.. In addition, we also propose a novel in-memory computation methodology using a Transmission Gate based SRAM Cell. This proposed IMC scheme offers an improvement of 22.6% in average power over an IMC based on the traditional 8T SRAM cell. This design also shows an improved delay performance for NAND, NOR and XOR operations. All simulations are carried out in LTSPICE using 32 nm CMOS process technology.

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LIST OF ABBREVIATIONS

S.No	Abbreviation	Full Name
1.	IMC	In Memory Computation
2.	BL	Bit Line
3.	BLB	Bit Line Bar
4.	RBL	Read Bit Line
5.	RBLB	Read Bit Line
6.	WBL	Write Bit Line
7.	WBLB	Write Bit Line Bar
8.	SRAM	Static Random Access Memory
9.	CMOS	Complementary metal-oxide semiconductor
10.	8T SRAM	8 Transistor Static Random Access Memory
11.	IC	Integrated Circuit
12.	WL	Word Line

CHAPTER 1

INTRODUCTION

1.1 Technology trends

In-memory computation is becoming increasingly popular due to the increasing volume and complexity of data being generated and processed in various domains. IMC eliminates the requirement for continuous data movement between the CPU and memory, reducing latency and improving overall system performance. This approach enhances the efficiency of data processing, enabling faster and more efficient execution of tasks compared to traditional computing architectures. This trend has gained momentum due to the availability of high-capacity and affordable memory, advancements in memory technologies, and the exponential growth of data-intensive applications. It offers the potential for faster data access, parallel processing, and improved efficiency, making it an attractive solution for addressing the limitations posed by the Von Neumann architecture and driving innovation in computing systems.

1.2 Motivation

In recent times, the computing industry has witnessed a substantial surge in the demand for increased speed and energy efficiency. This heightened demand can be attributed to various factors, including the widespread use of data-intensive applications, the rapid growth of artificial intelligence and machine learning, and the emergence of innovative technologies like virtual reality and the Internet of Things (IoT). To process and analyze data at faster speeds, there has been a strong focus on developing innovative architectures. This demand for speed and energy efficiency is likely to continue driving advancements in computing systems as technology continues to evolve.

The Von Neumann architecture is a foundation framework for the design of modern computing systems. It emphasizes the concept of a stored-program computer, where both instructions and data are stored in the same memory space, and the sequential processing of instructions by a central processing unit (CPU). Additionally, it emphasizes the use of a shared memory unit, accessible by both the CPU and input/output (I/O) system, enabling efficient data transfer and manipulation. However, data-intensive applications, such as

machine learning, big data analytics, and large-scale simulations, are limited by the von Neumann bottleneck due to its sequential nature where instructions and data need to be fetched from memory one at a time, leading to a delay in processing and increased latency and reduced throughput. To overcome the Von Neumann bottleneck, various techniques such as pipelining, and parallel processing have been employed to mitigate its impact.

In-memory computing is emerging as a promising approach to overcome the Von Neumann bottleneck and enhance system performance. It entails the direct storage and processing of data within the primary memory, thereby eliminating the necessity for frequent data transfers between the CPU and external memory. It is a key advantage for data-intensive operations, as it allows for quick and direct access to data, enabling faster computations and reducing processing time. It also enables parallel and distributed processing on a larger scale, allowing for the simultaneous processing of multiple tasks and increasing system throughput and efficiency. Advancements in-memory technologies, such as the development of high-capacity and affordable RAM modules, have made in-memory computing more accessible and feasible.

SRAM-based in-memory computing (IMC) is becoming increasingly popular due to its advantages in real-time data processing, high-speed analytics, and low-latency applications. SRAM offers fast and low-latency data access, allowing for faster data processing and analysis. It also allows for efficient parallel processing and supports high-speed data transfers, making it suitable for workloads that demand both speed and scalability. As demand for real-time data processing and low-latency applications continues to grow, the popularity of SRAM-based IMC is expected to increase further. The implementation of 6T SRAM-based In-memory computing involved the use of 6T SRAM cells as primary storage units for data and computations. To enable in-memory computing, the SRAM cells were equipped with additional circuitry and logic gates to perform computation operations directly within the memory cells. The fundamental idea involves the measurement of voltage on pre-charged bit lines through the activation of multiple rows of storage bit cells. However, since 6T-SRAM bit cells possess coupled read-write paths, ensuring data integrity within these cells becomes essential to mitigate potential read-disturb failures. CMOS 8T SRAM cells are commonly employed to address the read-disturb failure issue in in-memory computation. It is an extended version of the traditional 6T SRAM cell, incorporating additional transistors to separate the read and write paths. This reduces the risk of read-disturb failures and provides independent access to the bit line during read mechanism. However, the use of CMOS 8T SRAM cells

introduces additional complexity and increases the area overhead, but it is a crucial step in mitigating read-disturb failures and improving the stability of in-memory computation systems. CMOS 8T SRAM cells are continuously being optimized to create reliable and durable in-memory computing architectures, making them essential for efficient and durable computing. Initial implementation laid the foundation for further advancements and research in this field.

This thesis follows the pattern by presenting an In-memory computation scheme using SRAM cells that offers low-latency and low-power computing.

1.3 Contribution

Detailed study continuously expands the realm of knowledge, allowing for the emergence of new questions, ideas, and understandings that contribute to human progress and advance various fields of study. Through this dissertation, we aim at the following:

- Implementation and analysis of existing in-memory computation schemes to understand their strengths, weaknesses, and performance trade-offs.
- Evaluation of performance, power consumption, area efficiency, and reliability for the selection of SRAM cells for efficient and high-performance in-memory computing systems.
- Design and analysis of an in-memory computation scheme with an efficient SRAM cell and a thorough analysis of its performance, power consumption

The emphasis of this research is to create an In-memory computation scheme that uses high-speed and low components.Existing IMC is implemented and studied to select an efficient SRAM cell design that balances read and write speeds, power efficiency, and area utilization. The performance of the devised IMC scheme is evaluated through simulation and analysis.

1.4 Thesis Organization:

This thesis aims to explore the design and implementation of in-memory computation using different SRAM cells. The organization of the thesis is as follows:

- CHAPTER 1- This section provides an overview of the topic, highlighting the significance of In-memory computation and the importance of low-power SRAM cells for IMP. This chapter discusses the technology trends, motivation,

contribution, and thesis organization.

- CHAPTER 2- A comprehensive review of relevant literature is conducted, covering topics such as in-memory computation, SRAM cell topologies, and previous studies on in-memory computation using SRAM cells. This section identifies research gaps and forms the basis for the proposed work.
- CHAPTER 3- This chapter discusses the In-memory-computation methodology, which uses different SRAM cells tailored for in-memory computation. It explores different SRAM cell architectures that are designed in the literature.
- CHAPTER 4-This chapter illustrated the proposed scheme for In-memory computation using efficient Transmission gate-based SRAM cells. Design considerations such as power consumption, performance, area, and reliability of the used SRAM cell components are discussed
- CHAPTER 5- This chapter presents simulation results and the performance of the proposed design. Comparative analysis is conducted to assess the power consumption, computational speed, accuracy, and other relevant metrics of the proposed In-memory computation architecture.
- CHAPTER 6- This chapter summarizes the research findings, highlights the contributions of the thesis, and discusses its limitations. Suggestions for future research directions and improvements are provided, concluding the thesis.

The afterword section of the thesis provides a list of references to acknowledge and cite previous research, strengthening the credibility of the thesis.

CHAPTER 2

LITERATURE REVIEW

It is always essential to review the existing research in a field. The purpose of conducting a literature review is to build a solid understanding of the topic by examining prior studies. This helps to avoid duplication of efforts and acknowledge the contributions of other researchers. Additionally, a literature review helps to identify contradictions, research gaps, conflicts, and unresolved issues in previous studies. In this chapter, the literature review of the previous work is discussed .

2.1 PREVIOUS REPORTED WORK:

A. Agrawal et al. [1,] propose a novel approach to perform Boolean computations within SRAM arrays. This design integrates computation capability into the SRAM array itself, eliminating the need for separate logic unitsThis design presents benefits in terms of power efficiency, reduced latency and minimal area usage, and. compared to traditional architectures, and opens up possibilities for developing energy-efficient and high-performance computing systems.

A. K. Rajput et al. [2], presents a novel approach to leverage the 8T SRAM cell for performing both Boolean and arithmetic functions within the memory architecture. The paper demonstrates the feasibility and benefits of in-memory computation using the 8T SRAM cell, showcasing improvements in power consumption and area overhead compared to conventional architectures. This work contributes to the development of more efficient and high-performance computing systems by integrating computation capabilities into memory cells.

A. Jaiswal et al. [3], proposed multibit dot-product engine offers improved power efficiency, area utilization, and computation speed. This paper demonstrates the potential of utilizing the 8T digital SRAM array as an in-memory multibit dot-product engine (DPE) with analog-like functionalities. An approximate analog-digital DPE can be realized by employing analog voltages on the read ports of the 8T SRAM array and analyzing the resulting output current. The authors demonstrate the resilience of their

proposal to nonidealities such as line resistances and transistor threshold voltage variations.

C. Yeswanth et al. [4]. address the limitations of conventional computing architectures and propose an alternative approach where the computational tasks are performed within the memory itself. The focus of this paper is on leveraging the capabilities of 8T SRAM cells to implement Boolean and logical functions, eliminating the need for separate logic units and reducing data movement.

C. Premalatha et al. [5], presents a comparative study of different SRAM cell designs in the context of 90nm technology. The importance of selecting an appropriate SRAM cell design based on the specific requirements and constraints of a given application is highlighted. The effect of process variations and voltage scaling on the performance of the different SRAM cell designs is analyzed. They highlight the trade-offs between power consumption, area overhead, and reliability in the context of process variations.

J. Sharma et al. [6] ,propose the use of transmission gates in an 8T SRAM cell, which effectively reduces leakage current. The paper investigates various parameters of the TG8T SRAM cell during the write operation at 0.7V, including leakage current, leakage power, delay, and signal-to-noise ratio (SNR). The results, demonstrate the improvements achieved by the TG8T SRAM cell design. The proposed variability-aware SRAM cell design using transmission gates presents a viable solution for addressing leakage and delay issues in advanced SRAM designs.

M. Kang et al. [7] ,presents a novel approach to leverage the existing infrastructure of a standard 6T SRAM array for implementing in-memory inference processing. The paper introduces a multi-functional inference processor architecture that can perform various tasks, including activation, dot product, pooling, and normalization, using the inherent parallelism of the SRAM array. The proposed architecture demonstrates promising results in terms of computational efficiency, power consumption, and area utilization

S. Jeloka et al. [8], provides an overview of configurable memories, focusing on TCAM, BCAM, and SRAM technologies. It explores design challenges and trade-offs associated with these memory types and highlights the advantages and limitations of using push-rule 6T bit cells for logic-in-memory applications. A novel CAM structure that incorporates a conventional push-rule 6T SRAM bit cell, leading to a significant improvement in array

density compared to traditional CAM designs is proposed

V. Aswini et al. [9], propose an 8T SRAM cell based on transmission gates, optimized for biomedical applications.The proposed 8T SRAM cell utilizes transmission gate structures to enhance stability and reduce leakage power. The design is optimized to address the challenges posed by biomedical environments, ensuring reliable operation even in the presence of noise and variability.

W. Kang et al. [10], a cost-effective platform utilizing Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) for performing bitwise logic operations. The aim is to overcome the challenges posed by the memory and power limitations. The proposed platform achieves this by leveraging the existing peripheral circuitry within the memory, enabling logic operations to be executed directly within the memory without the need for additional processing units. This approach offers a cost-efficient solution for addressing the memory and power-related issues.

J. Chen et al. [11], propose a novel 8T compute an SRAM (CSRAM) architecture tailored for high-speed and reliable in-memory searching and logic-in-memory computations. The design incorporates specialized features such as pMOS access transistors and split-WLs dedicated to compute access. It also utilizes an elevated precharge voltage scheme and a low-skewed inverter-based sensing amplifier, aimed at enhancing the sensing speed. Experimental validation demonstrates the reliability and superior performance of the proposed design. Overall, this work presents an innovative and efficient solution for SRAM-based in-memory computing applications.

T. -L. Tsai et al. [12] ,explore the challenges involved in testing these 8T SRAMs and propose techniques and methodologies to ensure their functionality and reliability. The paper discusses testing strategies for various operations, such as in-memory arithmetic, logic operations, and memory-based algorithms. The importance of comprehensive testing to guarantee accurate and dependable in-memory computations is emphasized. The findings and insights presented in this paper contribute to the development of effective testing approaches for In-Memory-Computing 8T SRAMs, facilitating their successful integration into advanced computing systems.

P. Raikwal et al. [13], presents a comprehensive analysis of the research conducted on the design and performance enhancements of an 8T SRAM cell. The paper introduces a novel

single-ended 8T SRAM cell that offers low power consumption and high read static noise margin.It utilizes differential wordlines allows for enhanced read capability by decoupling the storing nodes from the bit line during the read operation. It demonstrates that the proposed cell exhibits reduced propagation delay compared to the conventional 6T SRAM cell, making it suitable for high-speed applications.

P. Swetha et al. [14], propose the use of TGD8T SRAM Cell , which replaces the Pass Transistors in the feedback path of the existing D8T SRAM Cell with Transmission Gates. This modification minimizes the voltage drop across the Pass Transistors, resulting in reduced Read Destruction and improved data transmission speed. The results demonstrate substantial improvements in speed and performance metrics, such as access time, power consumption, and read stability. The proposed SRAM cell design shows superior performance characteristics.

D. Najafi et al. [15], propose novel low-leakage six-transistor static random access memory (SRAM) cell for in-memory computing applications. The proposed SRAM cell is designed using IGFinFET technology, offering advantages such as reduced transistor count and decoupled read and write operations, making it an ideal candidate for in-memory computing.

Q. Dong et al. [16], address the challenge of reducing power consumption in SRAM designs while maintaining reliable operation at low voltages. The proposed 4 + 2T SRAM architecture aims to provide efficient searching and in-memory computing capabilities by incorporating additional transistors to the traditional 6T SRAM cell.

T. Yoo et al. [17], presents a novel dual-ported embedded dynamic random-access memory (DRAM) array design that enables in-memory computation of deep neural networks (DNNs) while maintaining compatibility with logic circuits. The proposed 4T DRAM array design offers a promising approach to enable efficient and low-power in-memory computations while maintaining compatibility with logic circuits.

CHAPTER 3

MEMORY CELL ARCHITECTURES AND IN-MEMORY COMPUTING STRATEGIES

This chapter discusses the critical aspects of memory cell architectures and the strategies employed in in-memory computing. Memory cells are fundamental units that store and retrieve data in computing systems, and their architecture plays a crucial role in determining system performance, power consumption, and efficiency. In-memory computing is an emerging approach to address the performance limitations of traditional computing systems, offering the potential for significant speed improvements and reduced data movement. This chapter aims to provide a comprehensive overview of memory cell architectures and explore various strategies employed in in-memory computing, paving the way for efficient and high-performance computing systems.

The structure of this chapter is organized as follows:

- Discussion of different SRAM cell architectures is defined in section 3.1.
- Examination of case studies and practical implementations of memory cell architectures used for in-memory computing strategies and the working principles of an IMC scheme with the implementation of Boolean operations is discussed in section 3.2.

3.1 Static Random Access Memory (SRAM)

In-memory computing (IMC) relies on the efficient and effective operation of memory cells to perform computations within the memory subsystem SRAM cells have garnered considerable interest due to their speed, reliability, and suitability for performing computations directly within the memory subsystem in IMC applications.1]. SRAM cells offer fast access times, data locality, high bandwidth, energy efficiency, scalability, and flexibility. These features enable efficient and high-performance computation within the memory subsystem, reducing latency and improving overall system performance. Additionally, SRAM cells provide excellent data locality and bandwidth, reducing the memory bottleneck and increasing available data bandwidth. Finally, SRAM-based IMC offers scalability and flexibility, allowing for easy expansion of memory capacity by

adding more cells. SRAM-based IMC is an indispensable component in modern computing systems, meeting the demand for faster, more energy-efficient, and versatile computation. Understand the concept and operation of SRAM.

The choice of SRAM cell architecture for IMC plays a crucial role in achieving efficient and high-performance computation within the memory subsystem. Various SRAM cell architectures have been developed and utilized to address the specific challenges and requirements of IMC applications. Following different SRAM cell architectures used in IMC schemes and their significance in enabling efficient in-memory computation are highlighted.

3.1.1 6T SRAM Cell

The 6T SRAM cell is a widely used SRAM cell architecture due to its simplicity and stability[5]. It consists of six transistors arranged in a cross-coupled configuration, with two pairs of CMOS inverters and two access transistors (M5 and M6) as illustrated in Fig 3.1. This configuration ensures that stored data remains stable even without a power supply. The access transistors control the read and write operations by enabling or disabling the connection between the memory cell and the bit lines. When a read operation is performed, one of the access transistors is activated, allowing the stored data to be sensed on the bit lines. In a write mechanism, the desired data is driven onto the bit lines, and the access transistors are activated to write the data into the cross-coupled inverters.

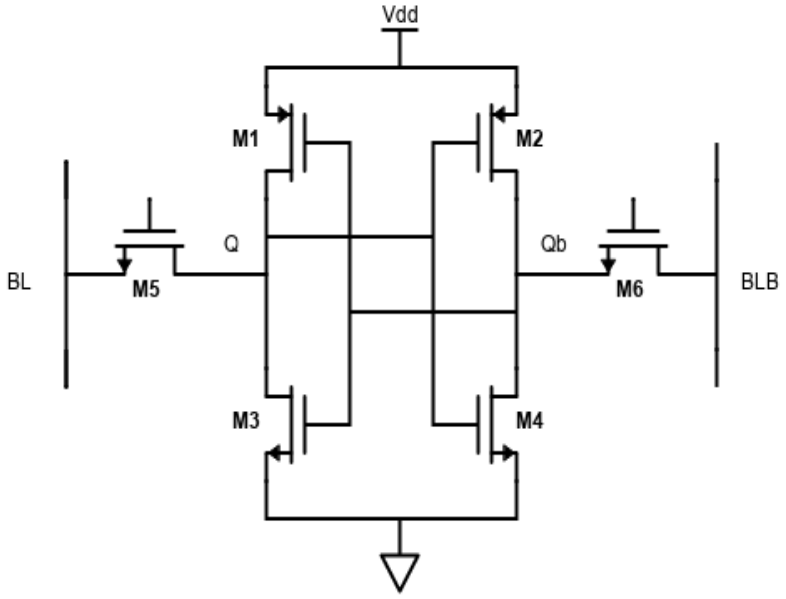


Fig. 3.1 Schematic of 6T SRAM cell[5]

Due to its compact size, simplicity, and stability, the 6T SRAM cell is extensively utilized in IMC applications. It is used to perform computations directly within the memory subsystem, reducing system latency and improving performance. However, it has drawbacks such as read-disturb failures due to its coupled read and write paths. This limits the ability to perform certain types of computations, requiring additional error correction mechanisms or more complex SRAM cell architectures.

3.1.2 8T SRAM Cell

The 8T SRAM cell is an advanced SRAM cell architecture that has gained attention for its improved read stability and reduced read-disturb failures compared to the traditional 6T SRAM cell. It consists of eight transistors, including two pairs of cross-coupled inverters, two pass transistors, and two isolation transistors as shown in Fig 3.2[1]. The cross-coupled inverters form the storage latch and are responsible for retaining the data. During read and write operations, the pass transistors regulate access to the storage latch, whereas the isolation transistors serve to separate the storage latch from the bit lines.

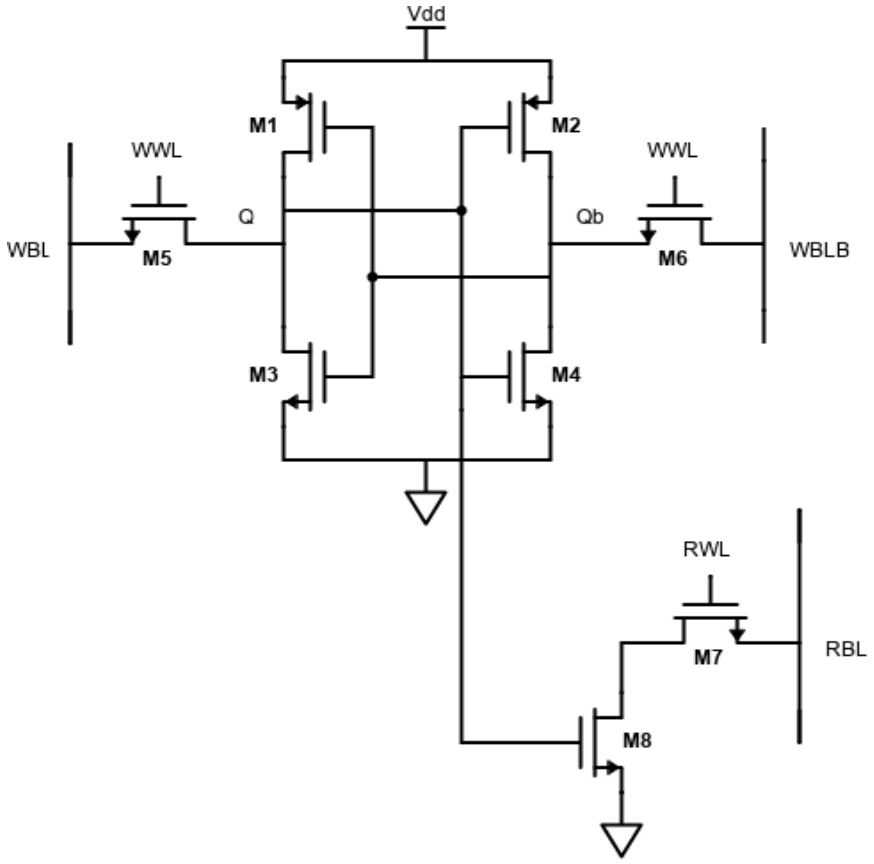


Fig. 3.2 Schematic of 8T SRAM cell[1]

Node Q and Qb are storage nodes similar to the conventional 6T SRAM. M5 and M6 access transistors which are activated by the write word line WWL and connect the storage nodes (Q and Qb) to the bit lines (WBL and WBLB). The two additional transistors (M7 and M8) were added to the 6T SRAM cell design to improve performance and address limitations. The read mechanism is initiated by pre-charging the RBL (Read Bit Line) to VDD. If Q is ’0’, M8 will be ’ON’ and the RBL will be influenced and discharged to 0; if Q is ’1’, M8 will be ’OFF’ and the RBL will still be charged to VDD.
The additional transistors M7 and M8 allow stored data on the storage nodes to influence the voltage levels on the bit lines, improving noise immunity, reducing susceptibility to voltage variations, and providing better resistance to soft errors. Additionally, the 8T SRAM cell allows for more precise control of data storage and manipulation, enabling higher computational precision.

The 8T SRAM cell is particularly well-suited for IMC applications due to its improved stability and reduced read-disturb failures. By decoupling the read and write paths, the 8T SRAM cell minimizes interference between these operations, reducing the chances of read-disturb failures that can occur in the 6T SRAM cell. Additionally, the 8T SRAM cell allows for the integration of additional functionality, such as error correction codes or power reduction techniques, which can enhance the reliability, error detection, and power efficiency of IMC systems. However, the 8T SRAM cell has some drawbacks, such as its increased area and complexity compared to the 6T SRAM cell, which can impact overall chip area and manufacturing costs. Additionally, the additional transistors introduce additional switching activity and parasitic capacitance, resulting in increased energy consumption.

3.2 In-Memory Computation Methodology

In-memory computing (IMC) using SRAM cells is a promising approach that revolutionizes traditional computing paradigms. SRAM (static random-access memory) cells, known for their fast access times and low power consumption, are utilized not only for data storage but also for performing computations directly within the memory itself. This approach eliminates the need for frequent data transfers between the processor and memory, significantly reducing latency and improving overall system performance. IMC with SRAM cells allows for parallel and distributed processing, leveraging the

interconnectedness of the memory arrays to perform computations efficiently. The proximity of computation to data enables faster processing of large datasets and complex algorithms. Moreover, the integration of computational capabilities within SRAM cells offers scalability and flexibility, enabling the design of custom accelerators tailored to specific computational tasks.

3.2.1 IMC Scheme using 8T SRAM cell

The main purpose of 8T SRAM cell based in-memory computing (IMC)[1] is to enable the simultaneous activation of multiple read word lines (RWL1 and RWL2) in an 8T SRAM array as shown in Fig 3.3. This allows for the connection of multiple read-bit lines (RBLs) to a sensing scheme ie skewed inverters(I1,I2,I3&I4) in this case, enabling parallel reading and processing of data.. By leveraging the multiple read capabilities of the 8T SRAM cell-based IMC, significant improvements in computational performance and efficiency can be achieved.

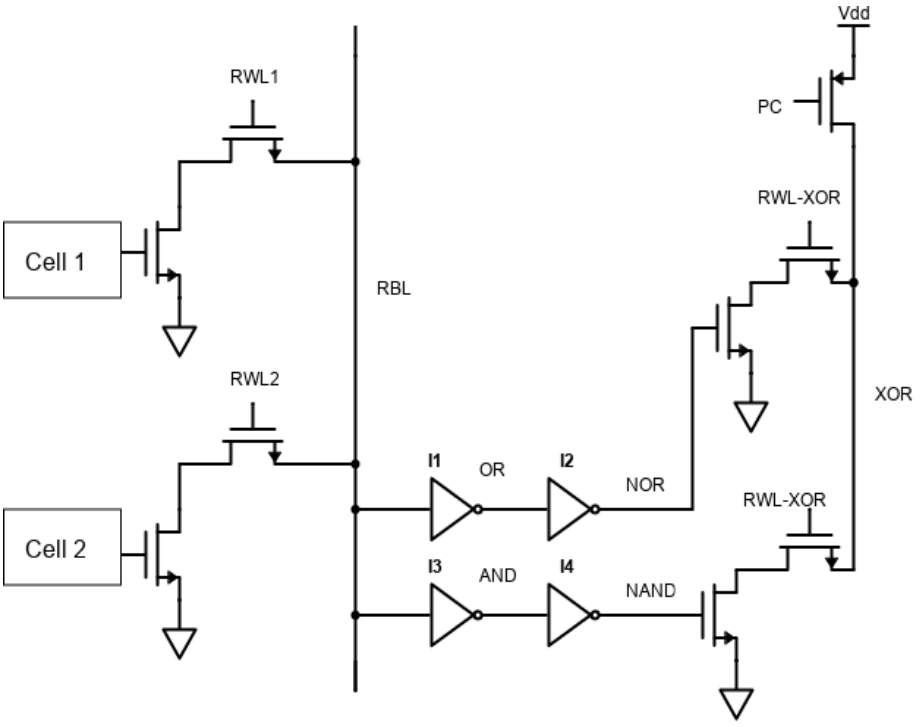


Fig. 3.3 IMC Schematic using standard 8T SRAM cell[1]

Figure 3.3 illustrates two 8T SRAM cells, namely Cell1 and Cell2. Each cell comprises six transistors, including two pairs of cross-coupled inverters and two pass transistors. The cross-coupled inverters form the storage latch, which retains the stored data. There are two isolation transistors that are connected to the read bit line RBL and these lines are wired NORed through the read bit-line to implement various boolean operations

3.2.2 Working Principle

In-memory computing (IMC) utilizing the 8T SRAM cell enables direct execution of NOR, NAND, and XOR operations within the memory, eliminating the need for data transfers to external computational units. [2]. These logical operations are accomplished by leveraging the unique characteristics of the 8T SRAM cell structure. Through this work, logic operations (NAND, AND, NOR, OR,XOR) are implemented by leveraging the isolated read approach and the two-port cell structure. During a read operation, the desired input is read from the cells and the access transistors connected to the selected row are activated. This enables the connection of the selected cells to the read-bit lines (RBLs) and skewed inverters. The stored data in the selected cells are then sensed through the skewed inverters. These lines are wired through the read bit-line to implement the desired boolean operation.

a) NOR/OR Operation: NOR functionality is implemented utilizing the idea that the 8T cells already have two concurrently active read-word lines. These lines are wired NORed through the read bit-line to implement the boolean operation. RWL1 and RWL2 activate the transistors connected to Cell1 and Cell2 as shown in Fig. 3.3.If the input at cell1 and cell2 is case ‘00” ,the pre-charged capacitor at the RBL will stay charged to ‘Vdd” and discharges if any of the inputs of cell 1 or cell 2 is read as logic ‘1’ ,thus following the truth table of NOR as shown in Table I.

b) NAND/AND Operation: Nand function is also implemented similarly to the NOR function. For case ‘00’ Here we need to activate the ground transistors through the RWL1 and RWL2 for a shorter duration of time such that for input case ‘01’/’10’, the precharged capacitor at RBL is not fully discharged and can be read as logic ‘1’ by the help of the skewed inverters.

c) XOR Operation: The output of AND and NOR are fed into NOR to acc to the eqn.

XOR=(Output(AND)) NOR (Output(NOR))

For realizing a bit-wise XOR boolean operation using an 8T SRAM cell as shown in Fig. 3 .3

Table 3.2 – Truth Table for Boolean Operations

A	B	NAND	NOR	XOR
0	**0**	1	1	0
0	**1**	1	0	1
1	**0**	1	0	1
1	**1**	0	0	0

CHAPTER 4

MODIFIED IN-MEMORY COMPUTATION SCHEME USING TRANSMISSION GATE BASED 8T SRAM CELLS

In this chapter, a modified in-memory computation (IMC) scheme utilizing transmission gate (TG) based SRAM cells is discussed. The use of TG-based SRAM cells offers unique advantages in terms of improved performance, reduced power consumption, and increased computational capabilities. This chapter presents an in-depth analysis of the modified IMC scheme, including the architecture, working principle, and performance evaluation.

The following is the arrangement of this chapter:

- Section 4.1 provides a detailed explanation of the structure and characteristics of the TG-based SRAM cell. The architecture and operation of the TG-based SRAM cell are discussed, highlighting its benefits in terms of improved data access and reduced power.
- Section 4.2 introduces the modified IMC scheme that leverages the advantages of TG-based SRAM cells. The scheme involves integrating computational functionalities into memory arrays by using transmission gates. Modifications to the traditional IMC scheme were made to accommodate TG-based SRAM cells, including the design of control circuitry and logic operations.
- Finally, section 4.3 compares the 8T SRAM cell and the TG 8T SRAM cell, focusing on their structural differences, functional characteristics, and applicability in IMC applications. By understanding their advantages and limitations, researchers and designers can make informed decisions when selecting the most suitable cell structure for specific IMC schemes. This comparison serves as a valuable reference for optimizing IMC systems.

4.1 Transmission Gate-based SRAM cell

In this section, we explore the SRAM cell that utilizes Transmission Gate, which is a

promising alternative to traditional SRAM designs. The transmission gate-based SRAM (TG-SRAM) cell is a promising alternative to traditional SRAM cell designs. It leverages transmission gates, which are electronic switches, to enhance the performance, power efficiency, and functionality of SRAM-based memory systems. It offers improved performance, power efficiency, and potential for in-memory computation. By understanding the structure and working principle of TG-SRAM cells, researchers and designers can explore their advantages and leverage them in various applications. The TG-SRAM cell represents a significant advancement in memory cell architecture and paves the way for more efficient and powerful memory systems.

4.1.1 Transmission Gate

A transmission gate is an electronic switch used in digital circuits and memory designs.It consists of complementary metal-oxide-semiconductor (CMOS) transistors connected in a parallel configuration. When the control signal is in a high state, the transmission gate is activated, facilitating the flow of current between the input and output terminals.. When the control signal is low, the transmission gate is turned off, effectively isolating the input and output terminals. This controlled access offered by the transmission gate is utilized in TG-SRAM cells to enable selective read and write operations, enhancing the functionality, performance, and power efficiency of memory systems[14].

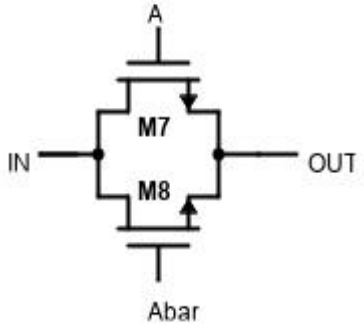


Fig. 4.1 Schematic of Transmission Gate

4.1.2 SRAM Cell Based on Transmission Gate

The Transmission Gate-Based SRAM (TG-SRAM) cell is an integrated SRAM cell design that consists of a cross-coupled latch formed by two inverters[9]. Here a Transmission Gate instead of the conventional pass transistors are used for the read path in the SRAM cell. The transmission gate(M7&M8) is strategically placed within the cell, connecting the latch to the bit lines and word lines. memory system, making it a promising

choice for various memory-intensive applications. When a read operation is initiated, the word line corresponding to the desired cell is activated, turning on the transmission gate connected to the bitline. This allows the stored data to propagate through the transmission gate and appear on the bitline. The incorporation of transmission gates in the SRAM cell structure enhances the functionality, performance, and power efficiency of the SRAM cell.

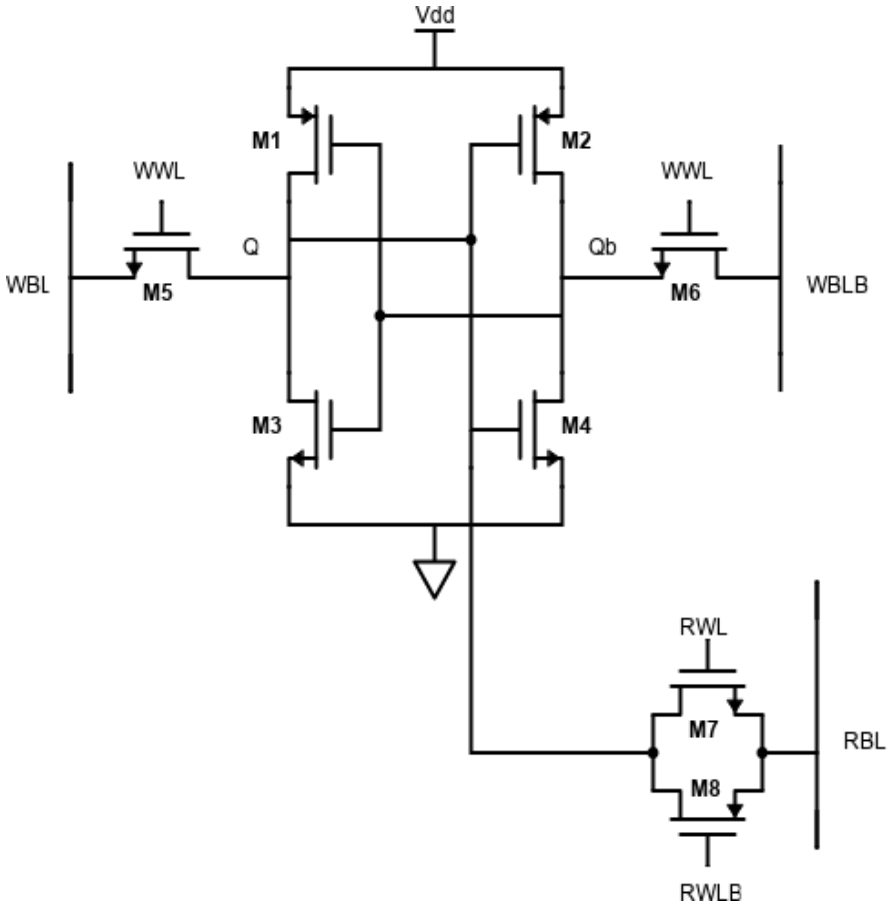


Fig. 4.2 Schematic of Transmission Gate based 8T SRAM [9]

4.2 Modified IMC using TG-based SRAM cells

Through this work, an In-memory computation scheme based on using a Transmission Gate instead of the conventional pass transistors for the read Path in the SRAM cell is proposed. The write mechanism is identical to the earlier designs. For the read path Transmission gate which is driven by complementary read lines RWL and RWLB is deployed. When the read lines are enabled the data from the storage nodes is read through transistors M7 and M8 into the Read Bit line (RBL) as shown in Fig. 4.3

The proposed Modified In-Memory Computation (IMC) scheme utilizing Transmission Gate-Based 8T SRAM cells aims to enhance the computational capabilities within memory arrays. The transmission gates provide controlled access to the SRAM cells,

facilitating the execution of various computational tasks directly within the memory subsystem. The proposed approach provides the benefits of reduced latency and power consumption associated with data transfers, and enables faster and more energy-efficient computations. Further research and optimization is necessary to fully realize the potential of the proposed scheme, including exploring innovative circuit designs, developing efficient control mechanisms, and investigating algorithms that can exploit the computational capabilities of the memory arrays. The proposed scheme holds great promise in advancing the field of in-memory computing, as it offers the potential for faster and more energy-efficient computation across a wide range of applications. This scheme opens up new possibilities for accelerating processing tasks and improving overall system performance. The reduction in latency and power consumption associated with data transfers can have significant implications for various domains, such as data-intensive applications, artificial intelligence, machine learning, and emerging technologies.

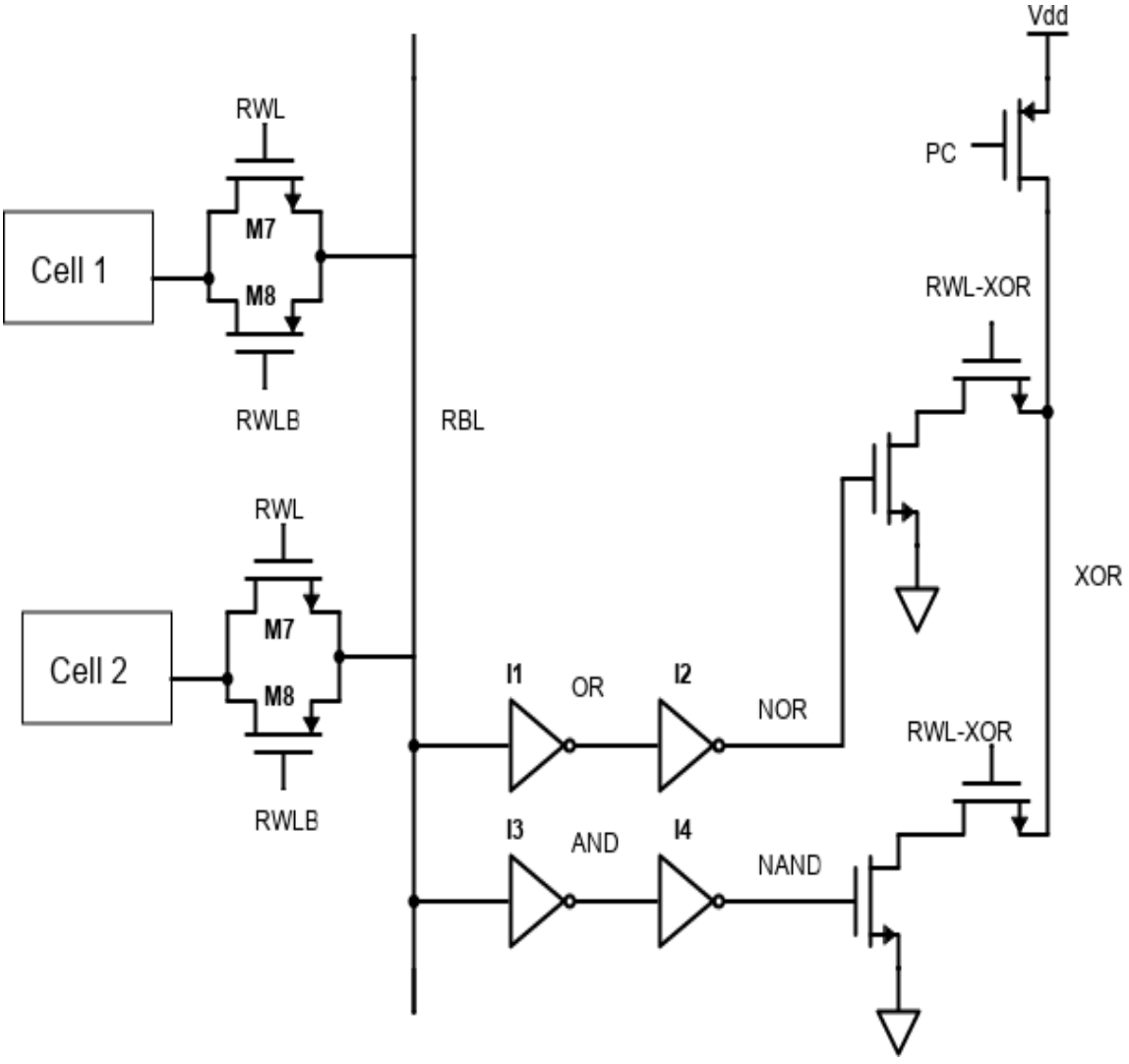
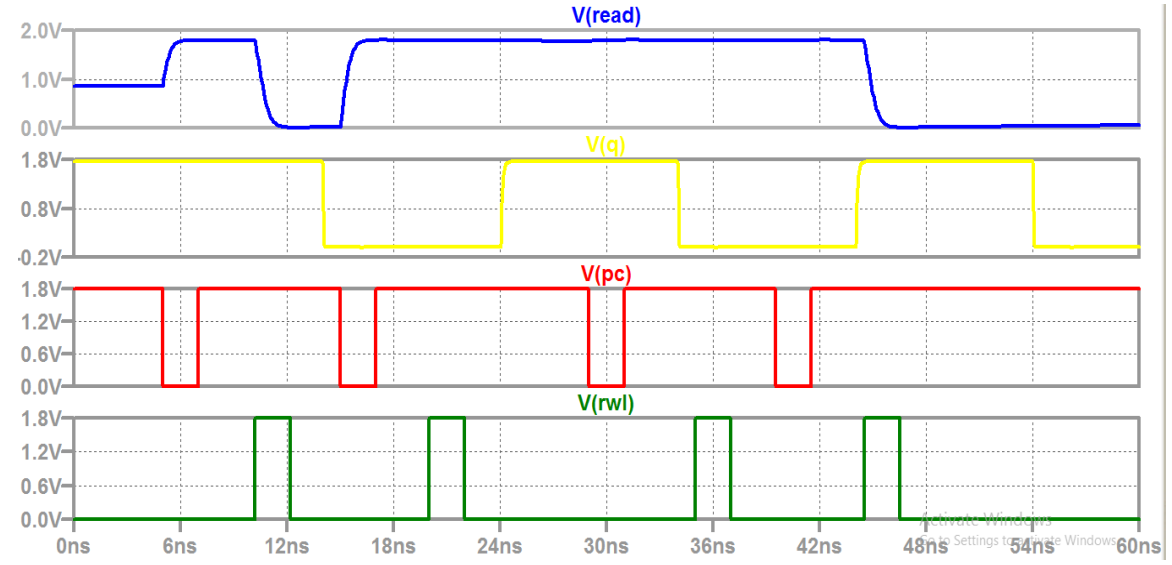


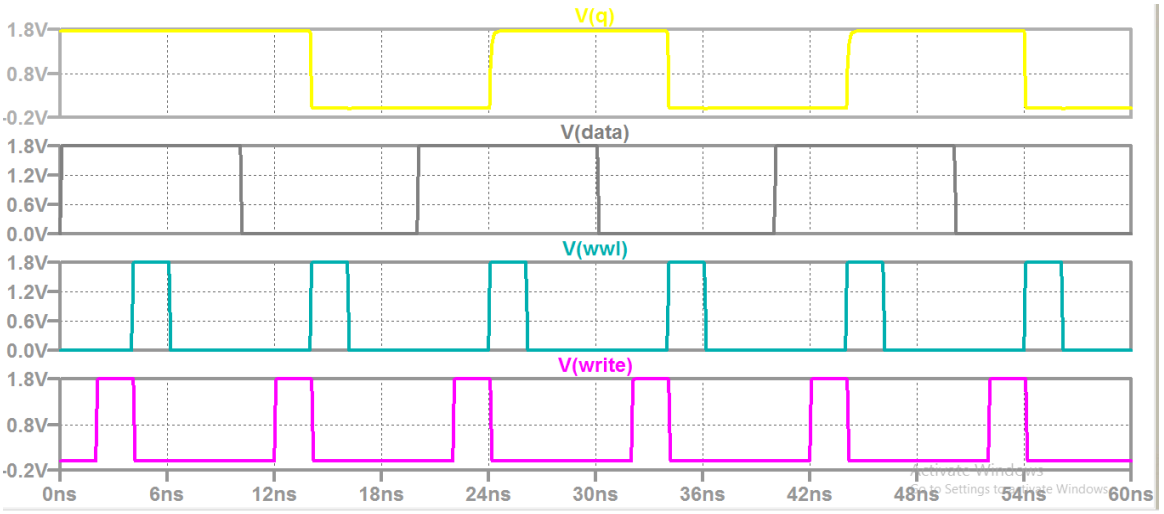
Fig. 4.3 Proposed IMC Schematic using Transmission Gate based 8T SRAM cell.

4.3 Performance comparison of 8T SRAM and Transmission Gate based 8T SRAM cell

In this section, we will compare and analyze the characteristics of the 8T SRAM and TG 8T SRAM architectures. We will examine their performance metrics, power consumption, latency and computational capabilities. The comparison will provide insights into the strengths and weaknesses of each architecture, helping in the selection and optimization of SRAM cell designs for specific memory system requirements. By understanding the trade-offs between the two architectures and doing this comparative analysis, we have made informed decisions to achieve the desired balance between performance, power efficiency, and computational capabilities in memory-intensive applications which formed the basis of the proposed design.

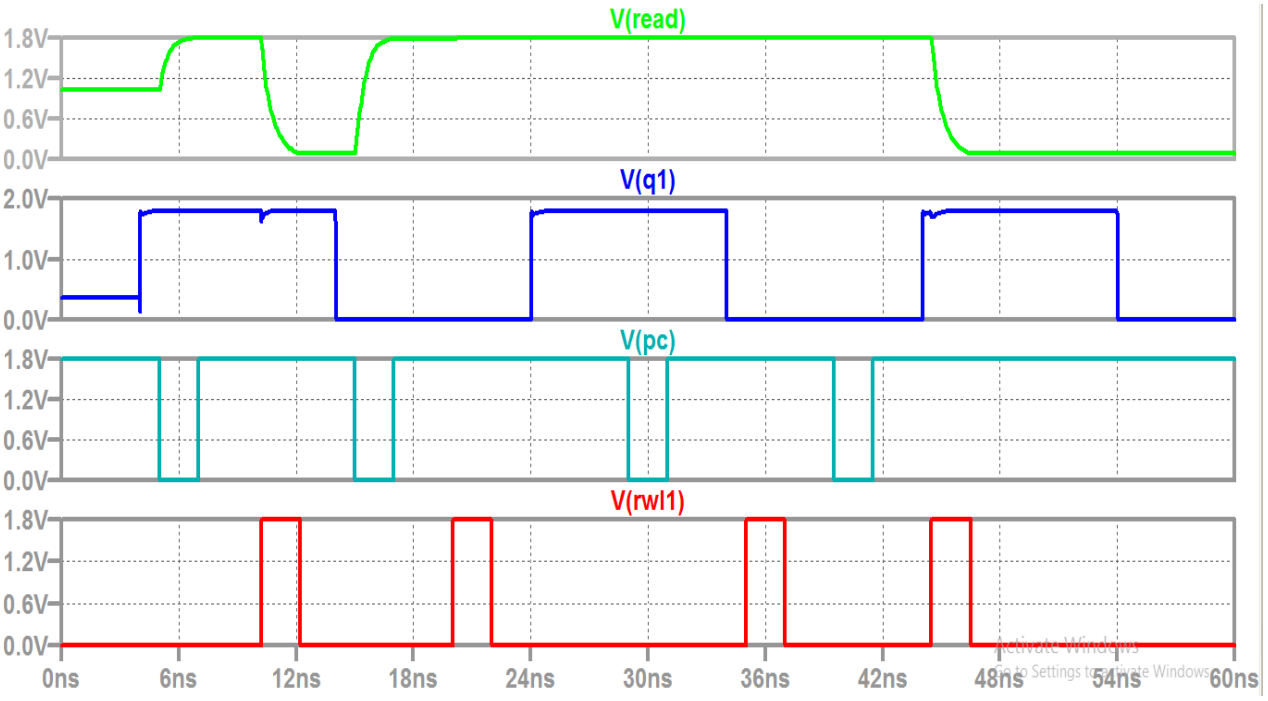


(a)

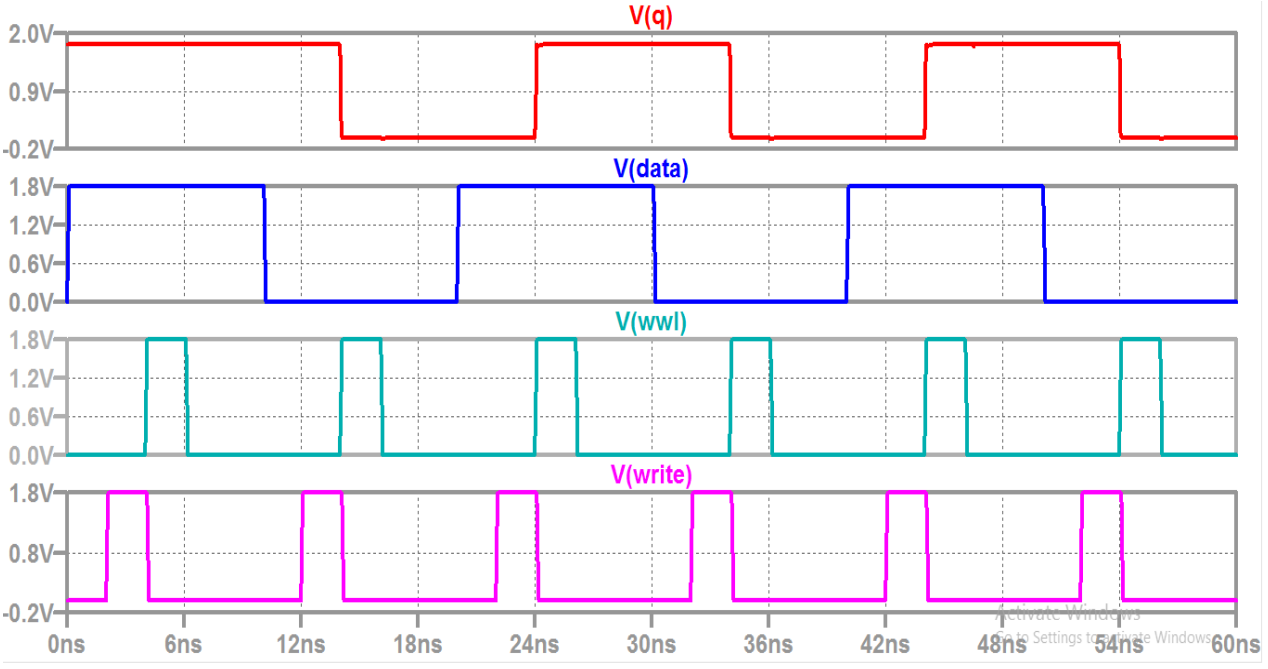


(b)

Fig. 4.4 Simulation results of 8T SRAM (a) Read (b) Write



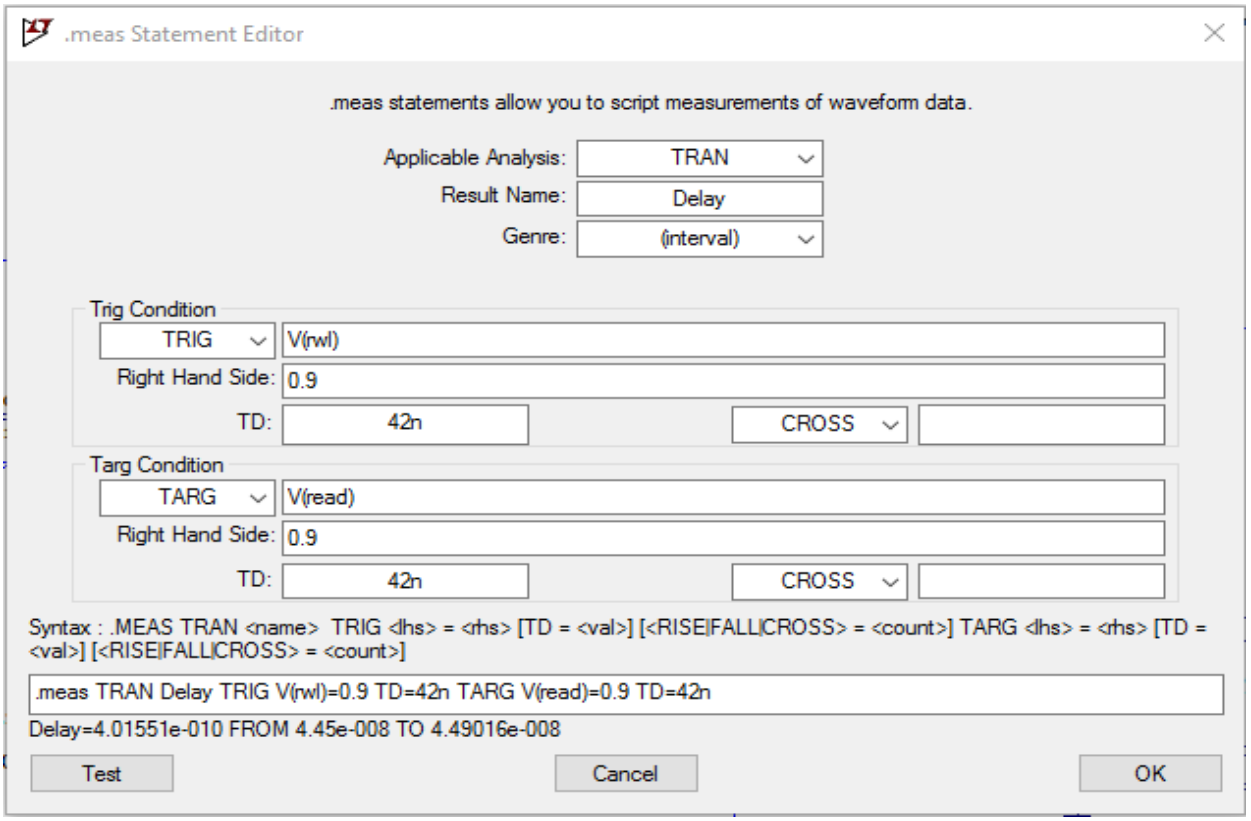
(a)



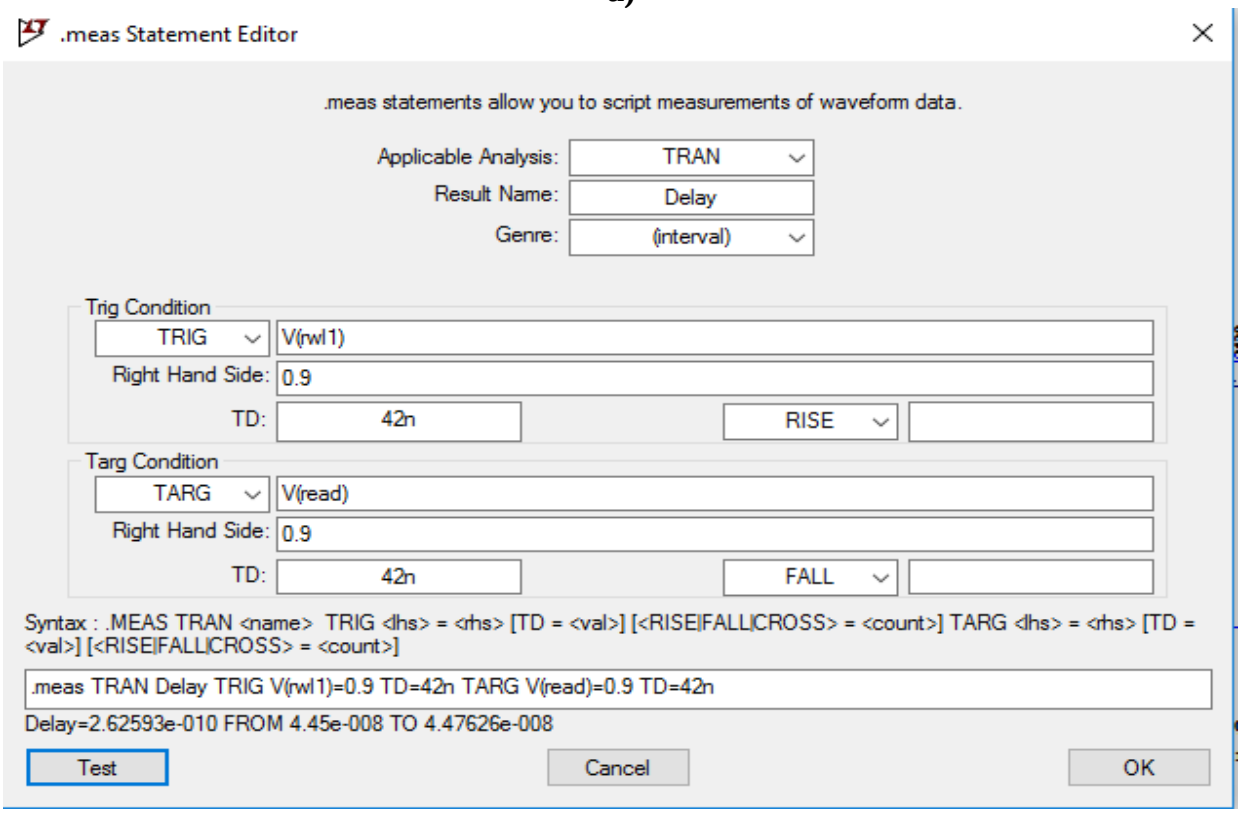
(b)

Fig. 4.5 Simulation results of Transmission Gate based 8T SRAM (a) Read (b) Write

Fig 4.4 and Fig 4.5 illustrates the simulation results of the read and write operations of two different SRAM cell configurations: the 8T SRAM and the TG-based 8T SRAM cells. The 8T SRAM cell consists of eight transistors, including two access transistors and six storage transistors, while the TG-based 8T SRAM cell incorporates transmission gates for improved operation.



a)



(b)

Fig. 4.6 Delay results of (a) 8T SRAM Cell (b) Transmission Gate based 8T SRAM Cell

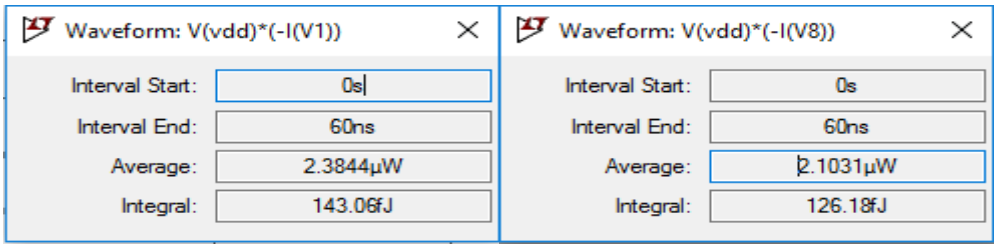


Fig. 4.7 Power results of (a) 8T SRAM Cell (b) Transmission Gate based 8T SRAM Cell

Table 4.1 shows the Performance of 8T SRAM cell and Transmission Gate based 8T SRAM cell

SRAM Cell	Power (µW)	Delay (ps)
8T SRAM Cell	2.384	401.55
Transmission Gate 8T SRAM Cell	2.103	262.59

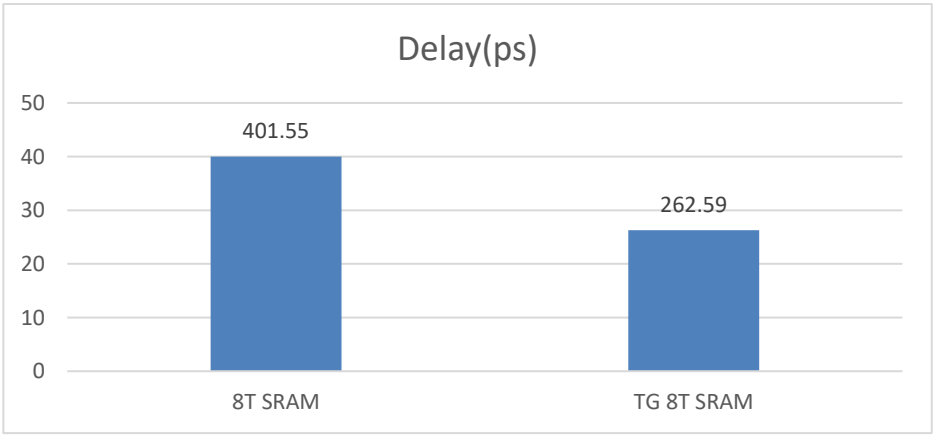


Fig. 4.8 Delay Comparision of 8T SRAM cell and Transmission Gate based 8T SRAM cell

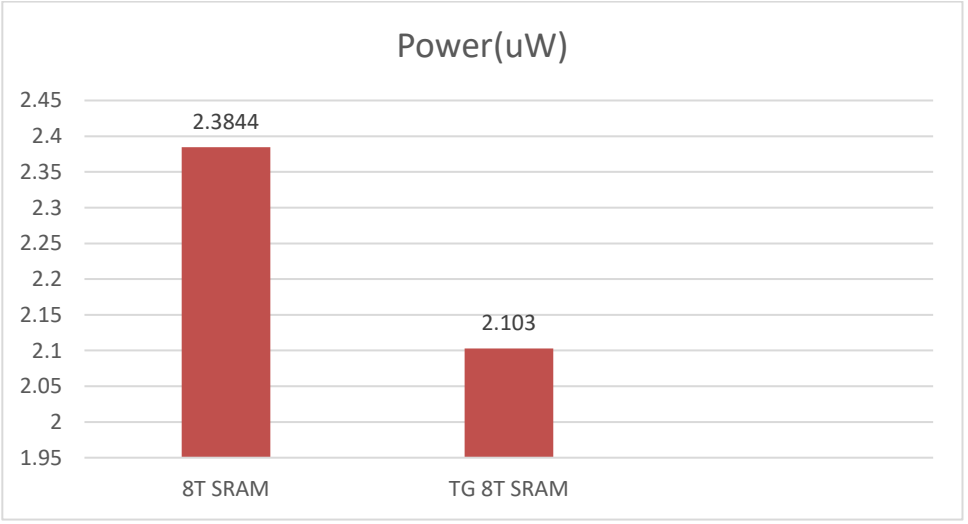


Fig. 4.9 Power Comparision of 8T SRAM cell and Transmission Gate based 8T SRAM cell

CHAPTER 5

SIMULATIONS AND RESULTS

In this section, the simulation results and a comprehensive comparison between IMC implementations using 8T SRAM cells and TG-based 8T SRAM cells is discussed. The simulation studies involve various metrics such as read and write latencies, power consumption, area efficiency, and computational capabilities. By evaluating these metrics, we can gain insights into the strengths and weaknesses of each architecture and determine their suitability for different IMC applications. The IMC operations for both the configurations ie 8T SRAM and Transmission Gate based 8T SRAMare simulated on LT spice using 32nm PTM technology. The sizing parameters for 8T cell IMC and the proposed 8T cell using Transmission Gate IMC are kept identical.Transient analysis was carried out on all three models to confirm thatthe hold, read, and write procedures worked properly. Similar read/write signals, input data signals, and precharge signals were used to replicate the models, and skewed inverters, precharge circuits, and write signals were used for all models. Fig. 5.1-5.6 presents the outcomes of the simulation. Here we can see the Boolean operations ie NAND/AND, NOR/OR, andXOR are implemented successfully.

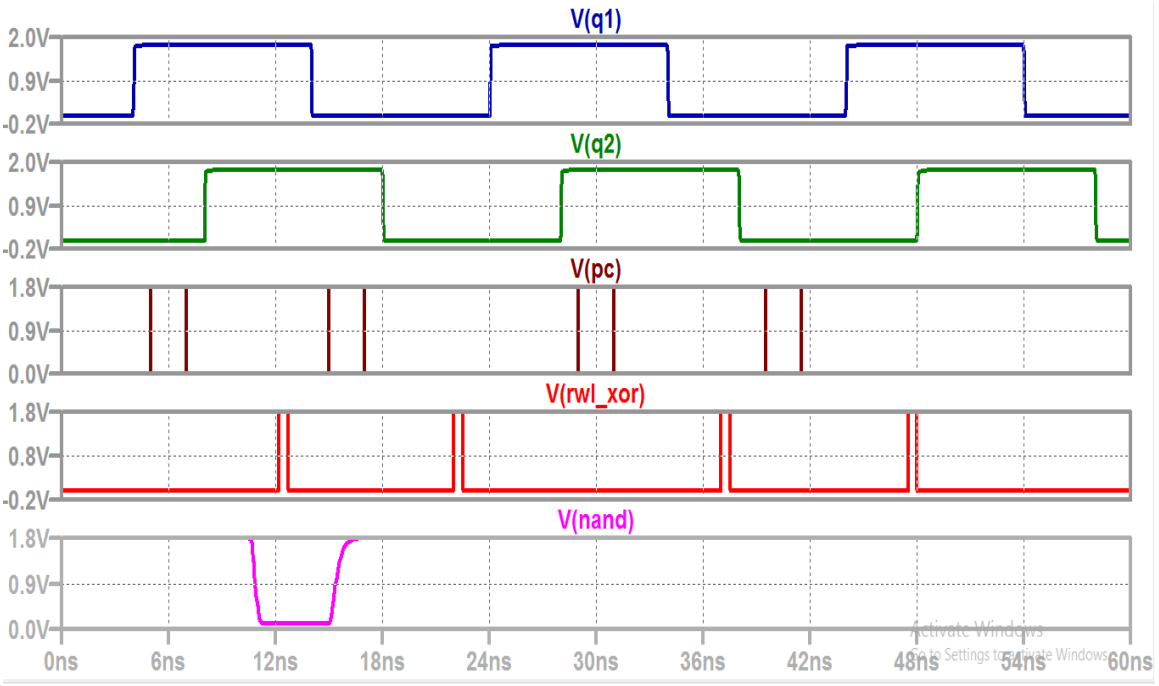


Fig. 5.1 IMC NAND Output using 8T SRAM

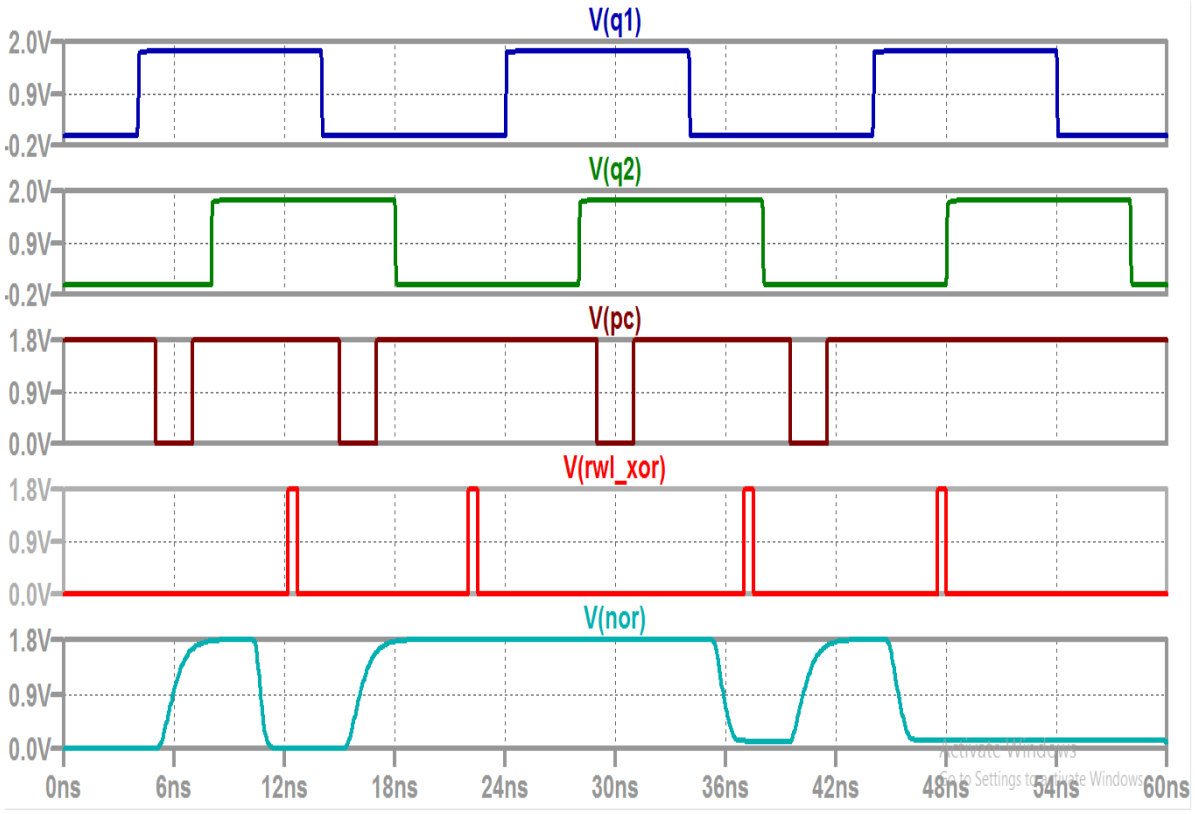


Fig. 5.2 IMC NOR Output using 8T SRAM

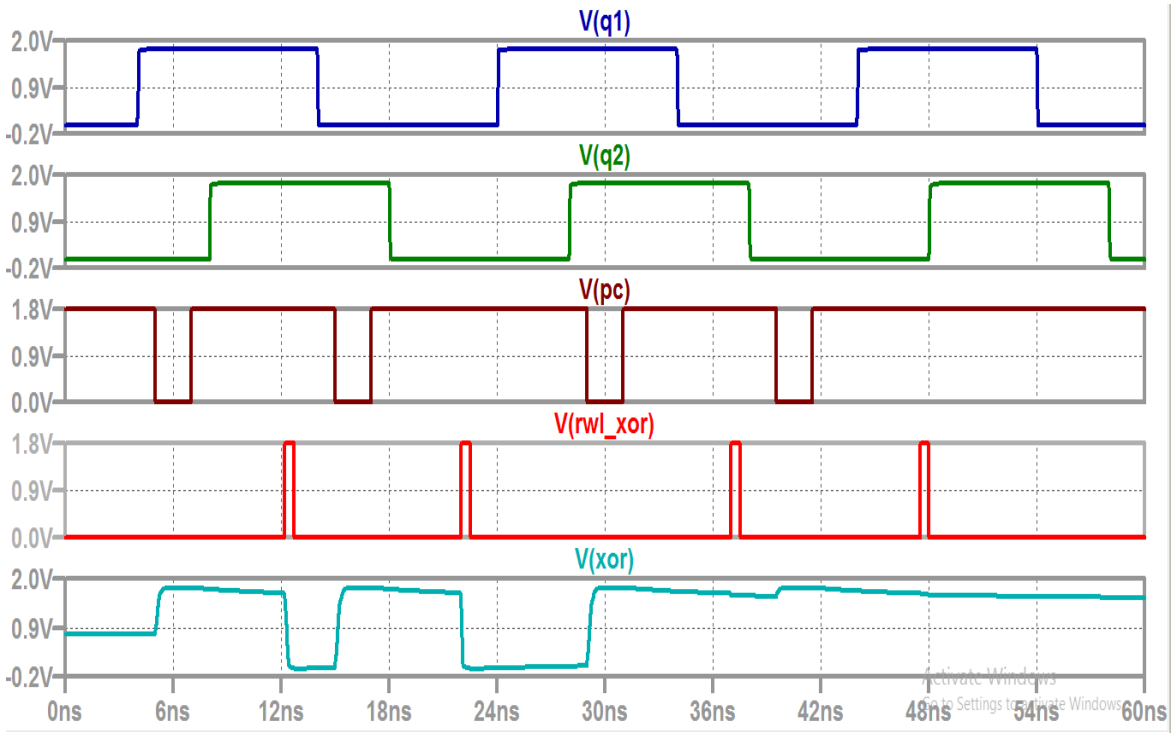


Fig. 5.3 IMC XOR Output using 8T SRAM

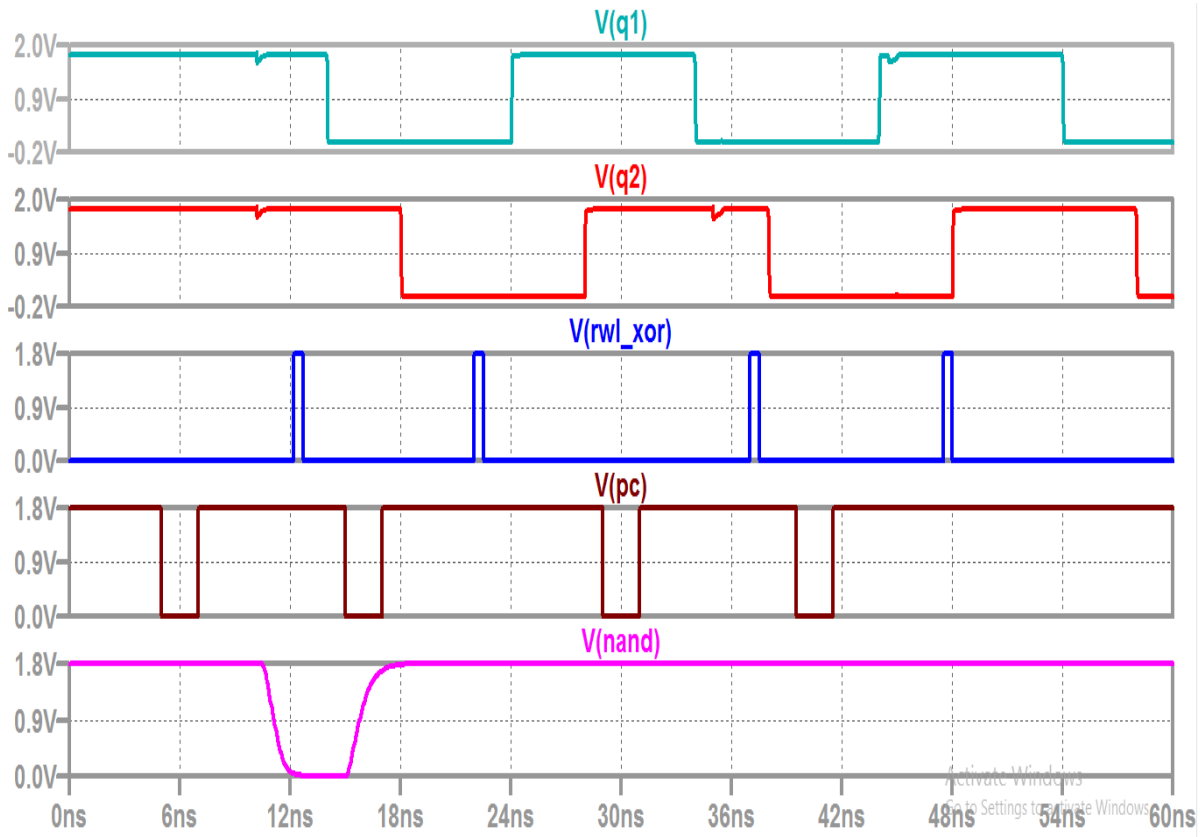


Fig. 5.4 IMC NAND Output using Transmission Gate based 8T SRAM

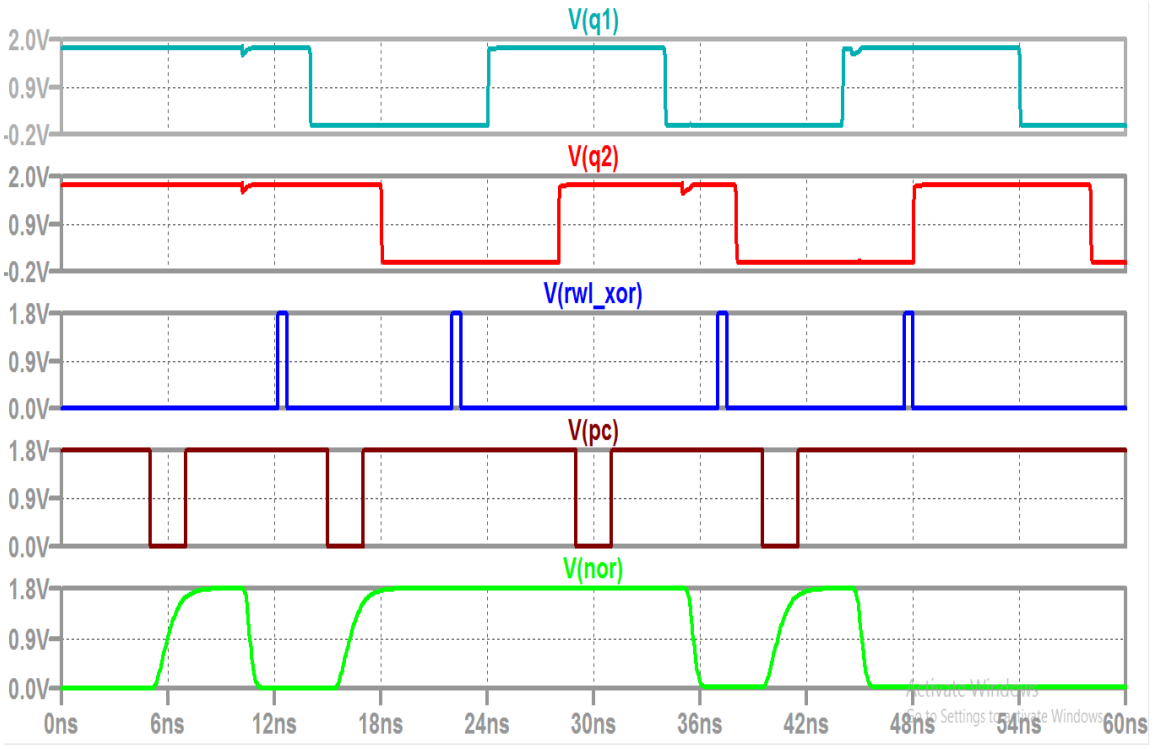


Fig. 5.5 IMC NOR Output using Transmission Gate based 8T SRAM

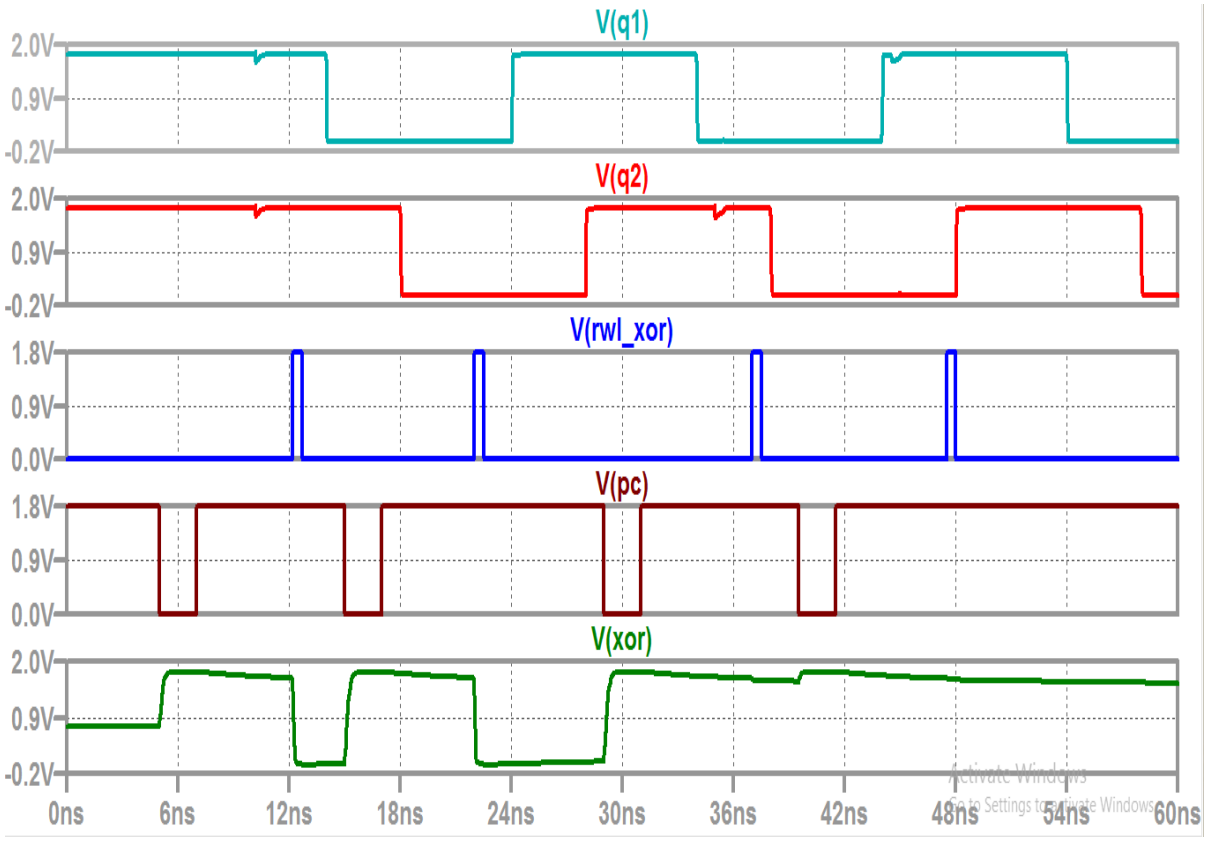
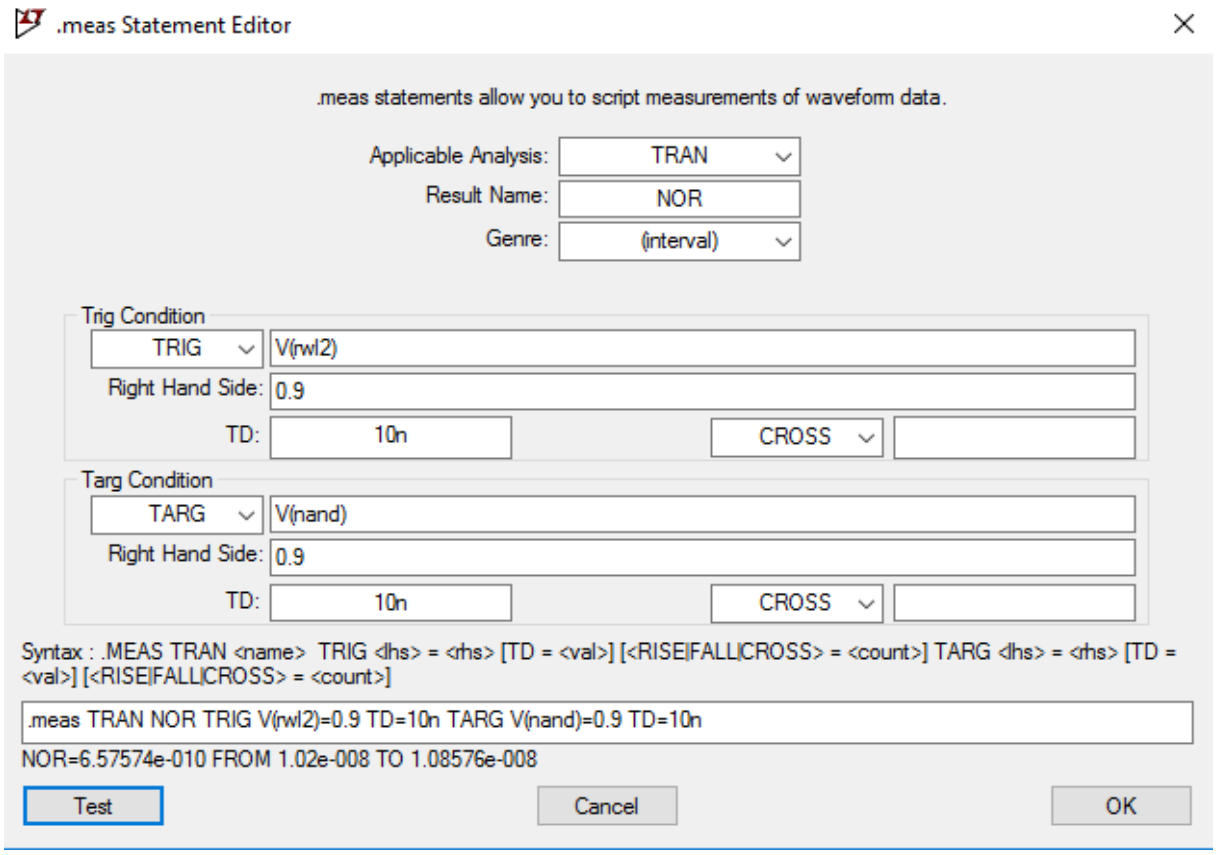


Fig. 5.6 IMC XOR Output using Transmission Gate based 8T SRAM



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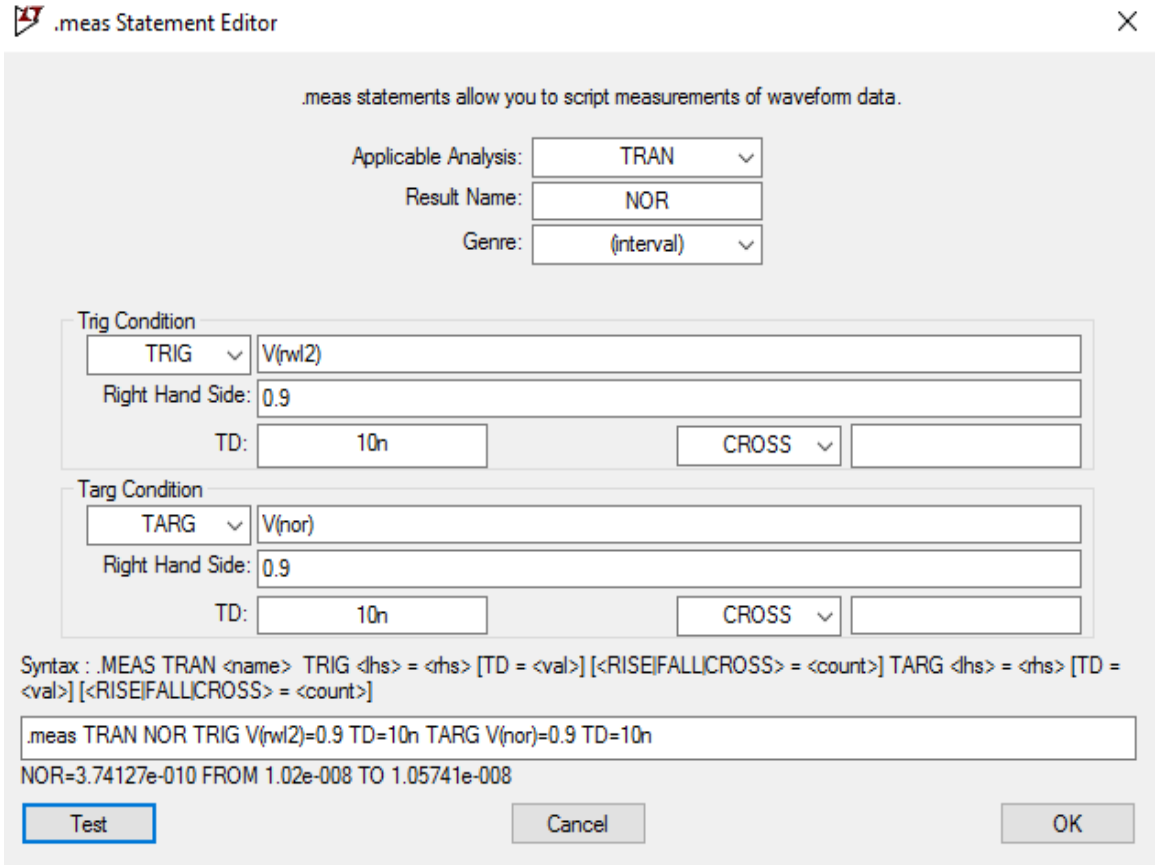
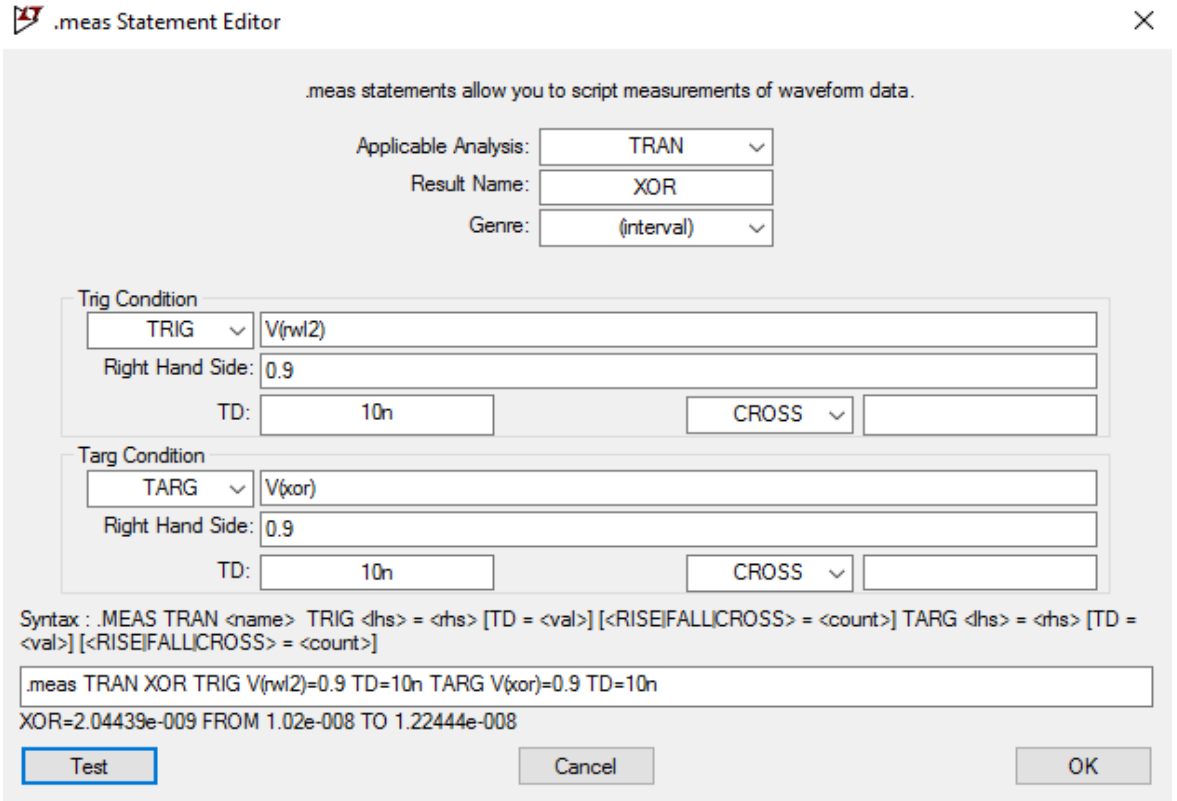
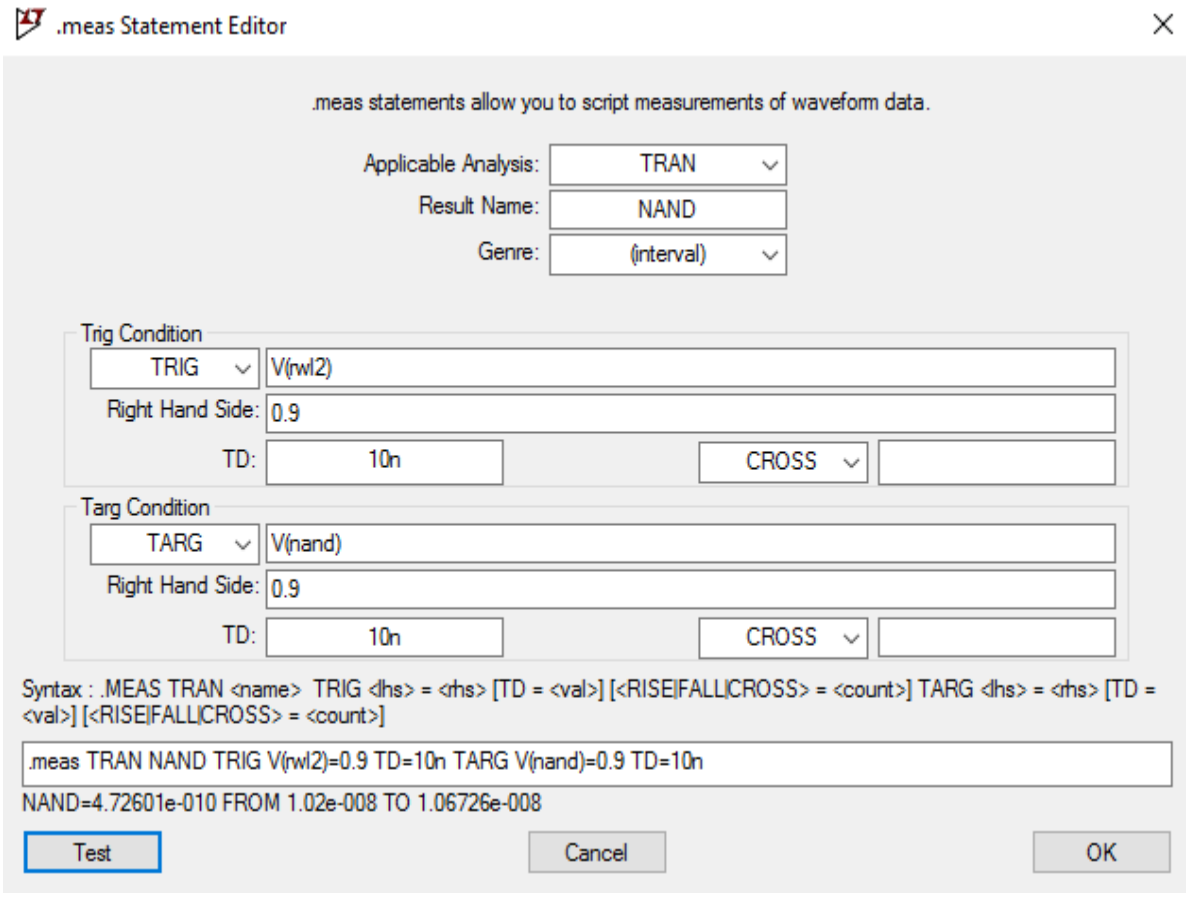


(b)

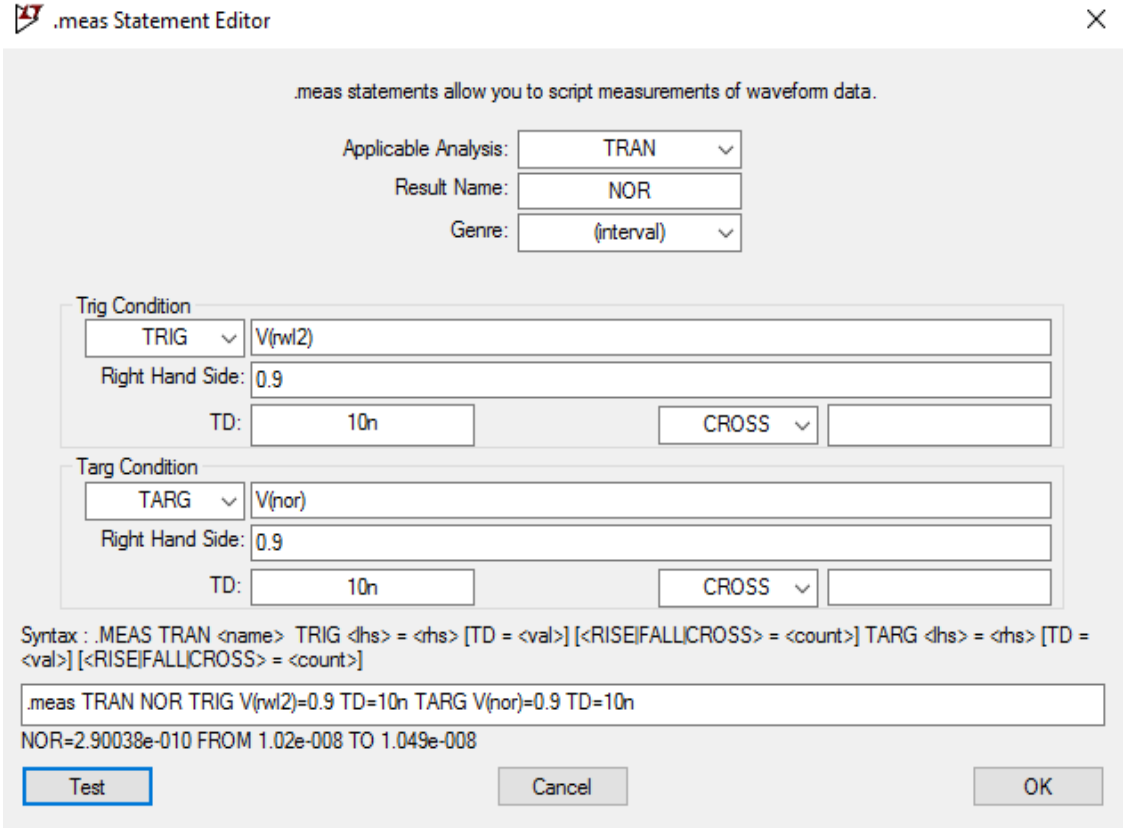


(c)

Fig. 5.7 Delay results of IMC using 8T SRAM Cell (a)NAND (b) NOR (c) XOR operation


.meas Statement Editor
.meas statements allow you to script measurements of waveform data.
Applicable Analysis: TRAN
Result Name: NAND
Genre: (interval)
Trig Condition
TRIG V(rwl2)
Right Hand Side: 0.9
TD: 10n CROSS
Targ Condition
TARG V(nand)
Right Hand Side: 0.9
TD: 10n CROSS
Syntax : .MEAS TRAN <name> TRIG <lhs> = <rhs> [TD = <val>] [<RISE|FALL|CROSS> = <count>] TARG <lhs> = <rhs> [TD = <val>] [<RISE|FALL|CROSS> = <count>]
.meas TRAN NAND TRIG V(rwl2)=0.9 TD=10n TARG V(nand)=0.9 TD=10n
NAND=4.72601e-010 FROM 1.02e-008 TO 1.06726e-008
Test
Cancel
OK

a)


.meas Statement Editor
.meas statements allow you to script measurements of waveform data.
Applicable Analysis: TRAN
Result Name: NOR
Genre: (interval)
Trig Condition
TRIG V(rwl2)
Right Hand Side: 0.9
TD: 10n CROSS
Targ Condition
TARG V(nor)
Right Hand Side: 0.9
TD: 10n CROSS
Syntax : .MEAS TRAN <name> TRIG <lhs> = <rhs> [TD = <val>] [<RISE|FALL|CROSS> = <count>] TARG <lhs> = <rhs> [TD = <val>] [<RISE|FALL|CROSS> = <count>]
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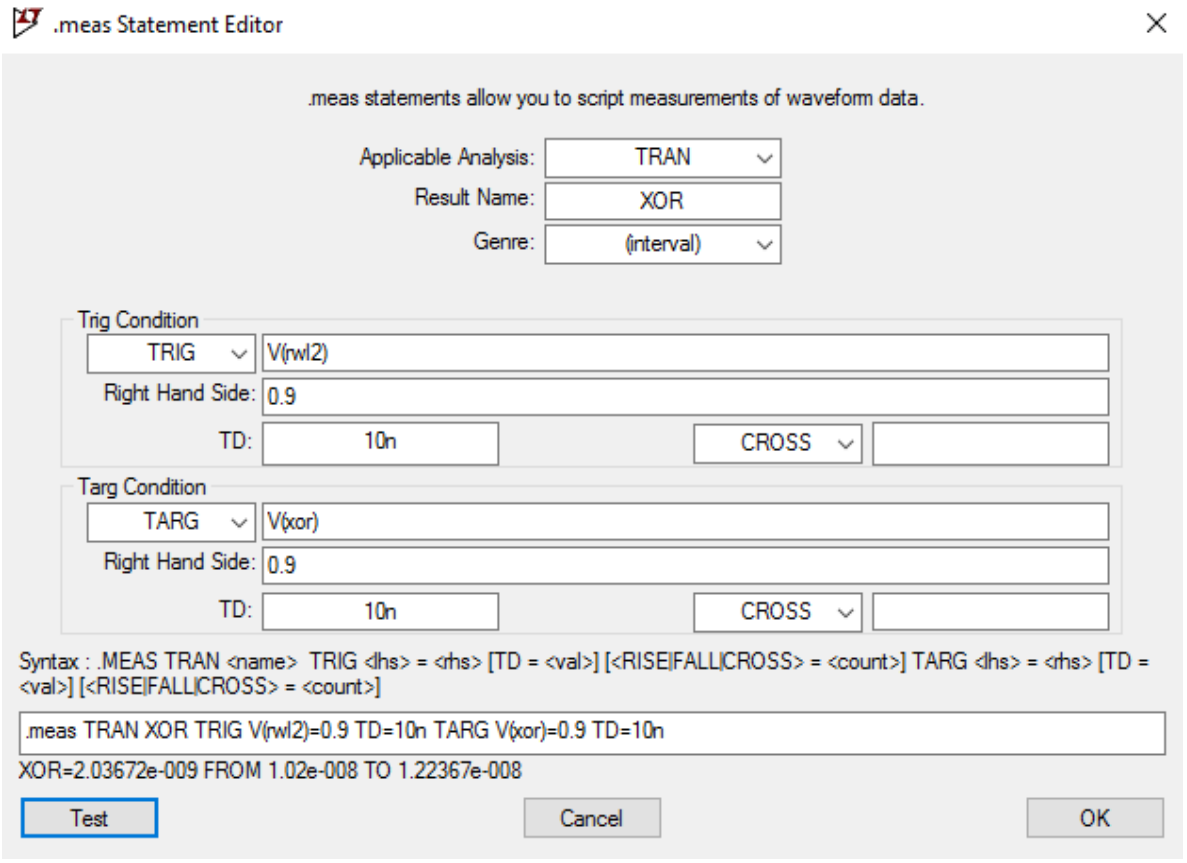
Test
Cancel
OK

(b)



(c)

Fig. 5.8 Delay results of IMC using Transmission Gate based 8T SRAM Cell (a)NAND (b) NOR (c) XOR operation

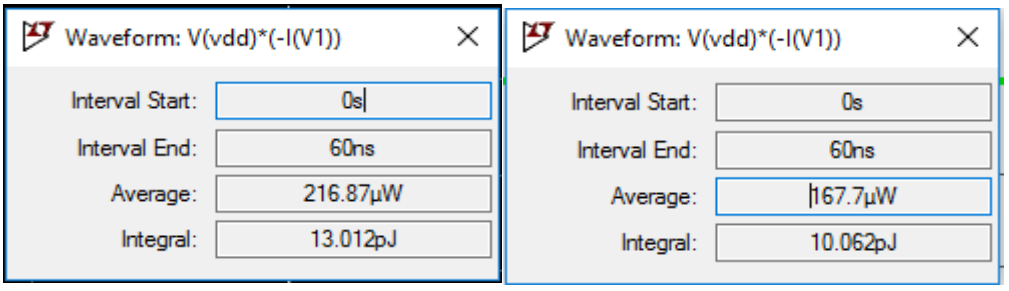


Fig. 5.9 Power results of IMC using (a) 8T SRAM Cell (b) Transmission Gate based 8T SRAM Cell

Table 5.1- shows the Power Performance of IMC Schemes using different SRAM Cells

Methodology	Power (µW)
In-Memory computation using traditional 8T SRAM cell	216.87
Proposed In-Memory computation using traditional Transmission Gate based 8T SRAM cell	167.7

Table 5.2- shows Delay Performance of IMC Schemes for boolean functions using different SRAM Cells

Methodology	NAND(ps)	NOR(ps)	XOR(ps)
In-Memory computation using traditional 8T SRAM cell	657.57	374.12	2044.39
Proposed In-Memory computation using traditional Transmission Gate based 8T SRAM cell	472.60	290.01	2036.70

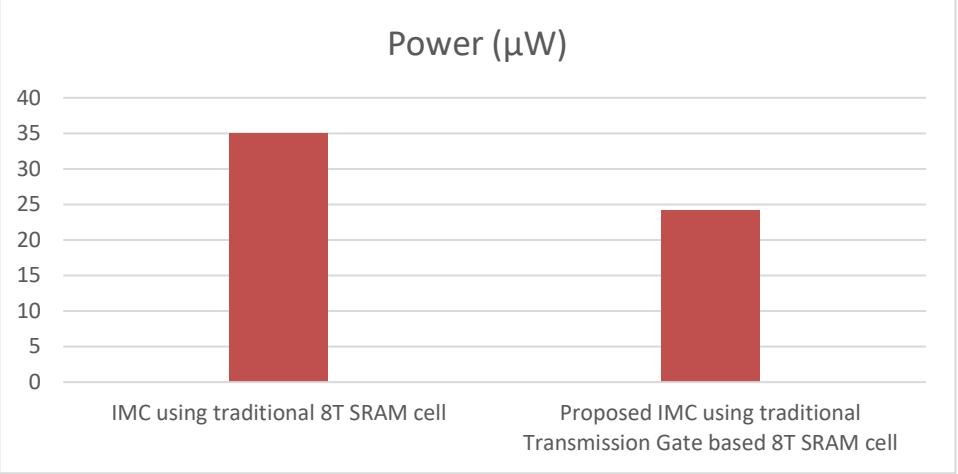


Fig. 5.10 Delay Comparison of IMC Schemes for Boolean operations using different SRAM Cells

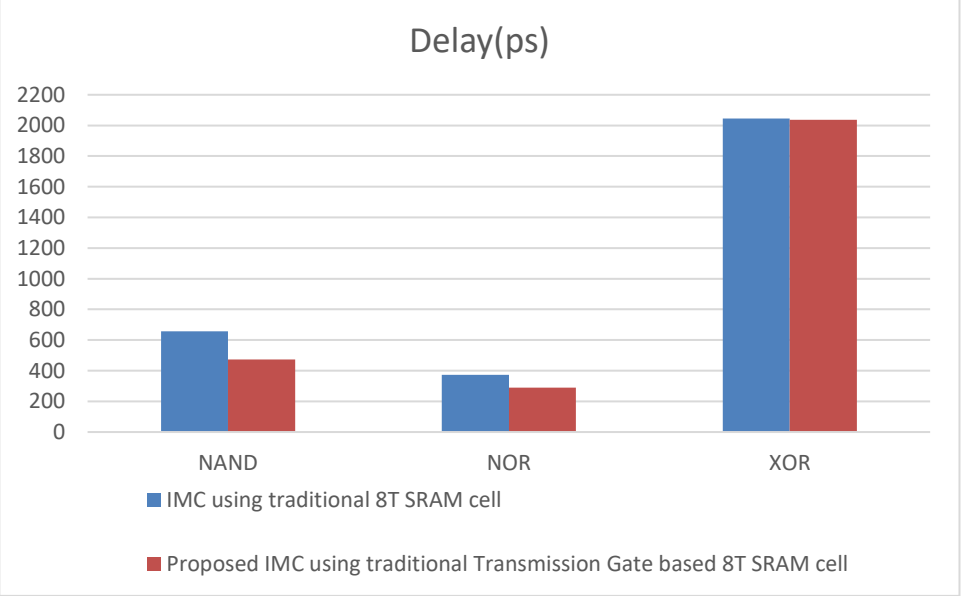


Fig. 5.11 Delay Comparison of IMC Schemes for Boolean operations using different SRAM Cells

The proposed IMC scheme is implemented using the TG SRAM. Table I and Table II shows the performance of the delay and average power consumption of the IMC scheme using 8T SRAM cell and the proposed IMC using the Transmission Gate based 8T SRAM cell. This IMC scheme shows to have a less average power consumption and less delay than the IMC using the traditional 8T SRAM cell.. Through simulation studies and comparisons, it can be observed that IMC using SRAM cells utilizing Transmission Gates offers reduced delay and power consumption. The introduction of transmission gates in the SRAM cell structure enables more efficient data access and manipulation, leading to faster computational operations within the memory array.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In this thesis, we have explored the concept of In-Memory Computation (IMC) and investigated the use of different SRAM cell architectures, for implementing IMC. Through extensive research and analysis, we have gained valuable insights into the strengths, limitations, and potential improvements of these architectures.

First, we examined the 8T SRAM cell and its suitability for IMC applications. The 8T SRAM cell, with its simple and stable structure, offers excellent data retention and stability. It provides reliable read and write capabilities, low leakage power, and high noise immunity. However, its larger area and higher power consumption pose challenges in achieving optimal performance and efficiency for memory-intensive computations.

To overcome some of these challenges, the use of the Transmission Gate based (TG) 8T SRAM cell for IMC is discussed.. The introduction of transmission gates into the 8T SRAM cell architecture enhances its functionality and flexibility. The transmission gates allow for controlled data access, enabling more efficient read-and-write operations. This improves the computational capabilities within the memory array, making it well-suited for in-memory computations.

Through simulation studies and performance comparisons, we have observed that IMC using TG-based 8T SRAM cells exhibits several advantages. It offers an improvement of 22.6 % in average power over an IMC based on the traditional 8T SRAM cell. This design also shows an improved delay performance for NAND, NOR, and XOR operations. The fine-grained data routing and selective access provided by the transmission gates result in faster computations and optimized power usage.

Based on these findings, we propose a design for IMC using Transmission Gate 8T SRAM cells. This design aims to enhance the performance and efficiency of IMC systems by leveraging the benefits of the TG-based SRAM cell architecture. The proposed design considers factors such as data access, latency power consumption, and area efficiency to achieve an optimised performance and energy efficiency. The In-Memory computation scheme for both the configurations ie 8T SRAM and Transmission Gate based 8T SRAM are simulated on LT spice using 32nm PTM technology.

In conclusion, the study presented in this thesis contributes to the field of In-Memory Computation by evaluating the use of 8T SRAM cells and proposing the adoption of Transmission Gate-based 8T SRAM cells for improved performance and power efficiency. The findings underscore the importance of selecting appropriate SRAM cell architectures for specific IMC applications and highlight the potential of TG-based SRAM cells in addressing the challenges of memory-intensive computations. The TG-based SRAM cell architecture provides finer control over data routing and parallelism in computations, resulting in reduced latency and improved system performance. Additionally, the selective data access made possible by transmission gates allows for optimized power consumption. IMC using TG-based SRAM cells holds great potential to address the elevating demands for high-performance and energy-efficient computation systems. It is well-suited for applications that require real-time processing, data-intensive computations, and low-power consumption.

As further research and development continue, we anticipate the proposed design to pave the way for more advanced and efficient IMC systems, enabling transformative advancements in data-intensive computing

6.2 FUTURE SCOPE

This thesis on In-Memory Computation (IMC) using 8T SRAM cells presents several promising avenues for future research. One potential area of exploration is the optimization of the TG-based SRAM cell design, which can be further refined to improve performance, power efficiency, and area utilization. Additionally, the scope of the research can be extended to include more complex computational functions like full adder, full subtractor, shift operations etc beyond basic logic operations. Additionally, evaluating the performance of IMC with real-world workloads can provide insights into the practical applicability and scalability of the proposed design. Future studies can also focus on developing energy optimization techniques to enhance the power efficiency of IMC using TG-based SRAM cells. Finally, hardware implementation and validation can provide a more accurate assessment of performance, power consumption, and other metrics. These efforts will contribute to the ongoing development and evolution of In-Memory Computation systems, enabling more efficient and powerful computing solutions for various applications.

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