STUDY OF LEAKAGE POWER REDUCTION TECHNIQUES IN CMOS CIRCUITS

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CANDIDATE'S DECLARATION

I, Ravi Ratan Jha, a student of M.Tech (VLSI and Embedded Systems), hereby declare that the project dissertation titled **"STUDY OF LEAKAGE POWER REDUCTION TECHNIQUES IN CMOS CIRCUITS"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University , Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "**STUDY OF LEAKAGE POWER REDUCTION TECHNIQUES IN CMOS CIRCUITS**" which is submitted by **Ravi Ratan Jha (2K21/VLS/16)** of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record ofthe project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Date: 30/05/2023 **Prof. Neeta Pandey**

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A successful project can never be prepared by the efforts of the person to whom the project is assigned, but it also demands the help and guardianship of people who helped in completion of the project. I would like to thank all those people who have helped us in this research and motivated me throughout my studies.

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ABSTRACT

Now a days power dissipation has become major issues in CMOS VLSI circuits due to limited life span of the battery. The leakage power dissipation is one of the prime concern at lower technology nodes. It is a difficult and challenging task to design a CMOS circuit without any leakage issue. Also at lower technology nodes, the leakage current increases. So, there is a need to study techniques which reduces leakage current.

In this study, the leakage power reduction techniques in CMOS circuits namely ONOFIC, stack ONOFIC, LECTOR and LCPMOS have been investigated. Here the basic logic gates namely NAND, NOR and sequential circuits like D flip flop and Up counters also have been examined. It is found that these techniques offer higher resistance to the path when in OFF state due to which it reduce the leakage current when compare to conventional circuits.

In this work for simulation LT Spice tool has been used and all the circuits are examined using 32nm technology node. Using ONOFIC technique on an average 79.57% leakage power have been reduced in static circuits and 95.69% leakage power have been reduced in sequential circuits. Using stack ONOFIC technique on an average 34.02% leakage power have been reduced in static circuits and 94.51% leakage power have been reduced in sequential circuits. Using LECTOR technique on an average 98.47% leakage power have been reduced in static circuits and 98.34% leakage power have been reduced in sequentialcircuits. Using LCPMOS technique on an average 85.364% leakage power have been reduced in static circuits.

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CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

There reduction in power consumption is prime concern in VLSI circuits and systems due to proliferation of wireless and portable electronic systems.

The total power dissipation in a CMOS circuit consists of static and dynamic power dissipation during the mode of operation, but in standby mode it is due to leakage current.

The dynamic power dissipation (P_{Dyn}) occurs during switching event i.e. charging and discharging of load capacitor C_L. The short circuit power dissipation (P_{SC}) results because of non zero rise time and fall time in input. The static power dissipation in a CMOS circuit can be given by the leakage current in each transistors used in the design. Thus, the power consumption (P_T) is given by equation (1)-

$$\mathbf{P_T = P_{Dyn} + P_{SC} + P_{Stat}} \quad (1)$$

P_{Stat} is power dissipation due to static current mainly leakage current.

1.1.1 Static CMOS Leakage Sources

There are several types of static CMOS leakage sources which are shown in Fig. 1.1 and explained below-

- **Reverse Bias P-N Junction Leakage-** This type of leakage is due to the drift of minority carriers near the edge of depletion region and generation of e-hole pairs inside of depletion region. Its magnitude is very small and can be neglected. But due to increase in electric field across the reverse biased P-N junction, sufficient amount of current flow occurs due to band to band tunneling.

- **Sub-Threshold Leakage-** This leakage is a weak inversion current that flows between the drain and source terminals of transistors even when the applied V_G is lesser than the V_{th}. With the reduction in threshold voltage this weak inversion current increases exponentially and it make the design of CMOS circuits having low voltage low power (LVLP). V_{th} roll offs and drain induced barrier lowering

(DIBL) these effects make the sub-threshold leakage worsens.

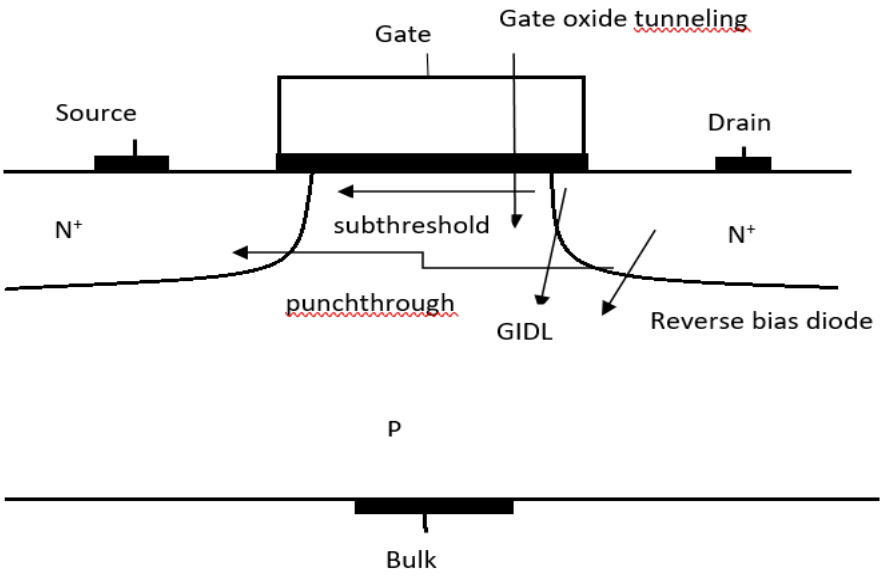

Fig.1.1 Static CMOS Leakage Sources

- **Gate Induced Drain Leakage (GIDL)-** This occurs for V_G less than zero and large value of V_D. The reason behind it is the large electric field inside the overlapped area of drain and gate which causes the band to band tunneling.

- **Punch Through-** This occurs when the value of V_D is large and the depletion regions of drain and source are very close. Here due to punch through the gate region lose the control over the current flow in channel and the slope of subthreshold starts degrading.

- **Gate Oxide Tunneling-** This occurs when there is the large electric field in the gate oxide region which causes F-N tunneling inside the oxide and direct tunnel through the gate region. In normal device conditions F-N tunneling is very less and can be ignored but when the oxide layer thickness is lower than 2-3 nms the direct tunneling event is important and considerable.

1.1.2 Dynamic Power Consumption

The dynamic power enters the scene as a result of the charging and discharging activities of load capacitances as shown in Fig. 1.2.

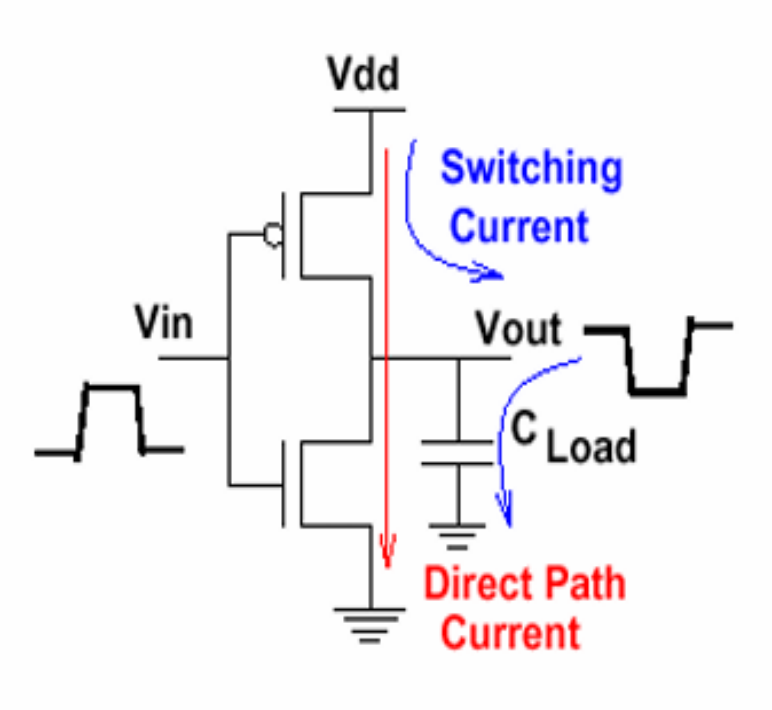

Fig. 1.2 Dynamic Power Consumption

The mathematical equation can be given as-

$$P_{Dyn} = V_{DD}^2 * C_L * N * f \quad (2)$$

Where C_L is load capacitance, V_{DD} is power supply voltage, N is switching activity factor, f is signal frequency.

1.1.3 Short Circuit Power Consumption

Because of the transitions occur in transistor, for short duration of time both the PMOS and NMOS are in ON condition and due to which a short circuit current flow in both the transistors which leads to the short circuit power dissipation shown in Fig. 1.3.

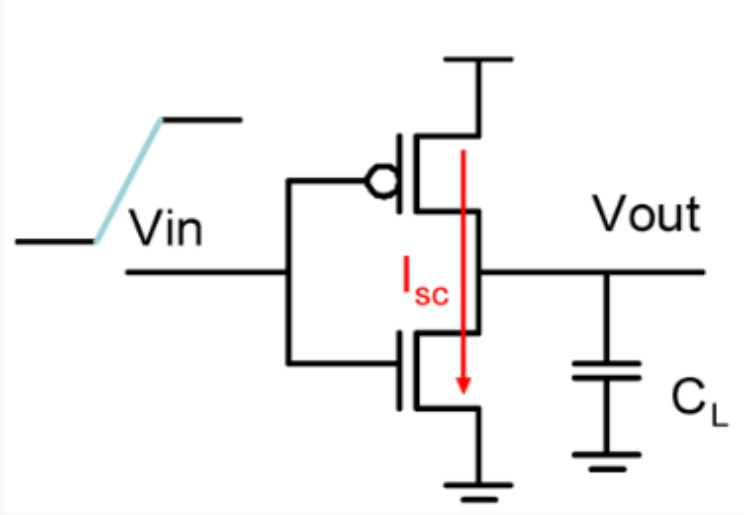

Fig. 1.3 Short Circuit Power Consumption

1.2 MOTIVATION

One of the main problems with modern CMOS VLSI circuits is power dissipation. Regarding battery life in battery-operated systems, as well as other factors like reliability, cooling cost, etc., excessive power dissipation is not advised. It also shortens the duration of the battery's life. Currently, an important concern in CMOS VLSI circuit design is leakage power dissipation. It is a difficult and challenging task to design a CMOS circuit without any leakage issue. Also at lower technology nodes, the leakage current increases. So, there is a need to study techniques which reduces leakage current.

1.3 ORGANISATION OF WORK

In this work the contents are divided into six chapters. Chapter 2 containing various leakage power reduction techniques namely ONOFIC, stack ONOFIC, Lector and LCPMOS in brief. Chapter 3 explains the impact of leakage reduction techniques on universal gates. Chapter 4 explains the impact of leakage reduction techniques on D-FF. Chapter 5 explains the impact of leakage reduction techniques on up-counter circuit. Chapter 6 consist of conclusion and future scope of the work.

CHAPTER 2
LEAKAGE POWER REDUCTION TECHNIQUES

In the conventional CMOS circuit there is a PDN having nMOS which is connected with GND rail and a PUN having pMOS which is connected with power supply V_{DD} as shown below in Fig. 2.1.

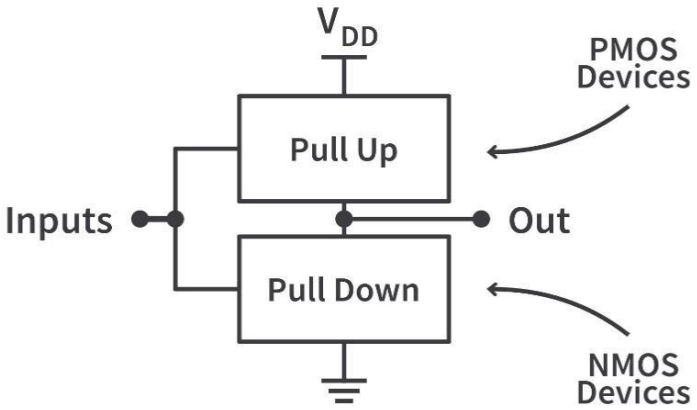

Fig. 2.1 Conventional CMOS Circuit

This circuit is a basic part in all the other techniques which will be discussed.

In nano scale technology node the importance of VLSI design with low power applications is more. The various methods of reducing leakage power can be seen as the building blocks of VLSI circuits in low power applications.

In order to reduce the leakage current in nano scale technology there are various methodologies and research have been done. There are various level of abstraction in low power circuit design in order to reduce the leakage parts. In order to reduce the current due to leakage, circuit level methodologies are more efficient and powerful but logic has to accept the cost of more transistors in the circuits.

2.1 ONOFIC

In ONOFIC technique[2] of leakage power reduction, a logic block which consisting of a pMOS Tr. and a nMOS Tr. is connected between the PUN and the PDN in a specific manner shown in Fig. 2.2. This logic block is called as ON-OFF logic block. Generally we use PMOS transistors in PUNs and NMOS transistors in PDNs. The basic reason behind this is the nMOS Tr. can allow the logic “0” without any distortion and pMOS Tr. can allow the logic “1” without any distortion, so we can achieve maximum swing

between V_{DD} and GND. In this approach we inserted only one logic block between PUNs and PDNs hence it is less complex.

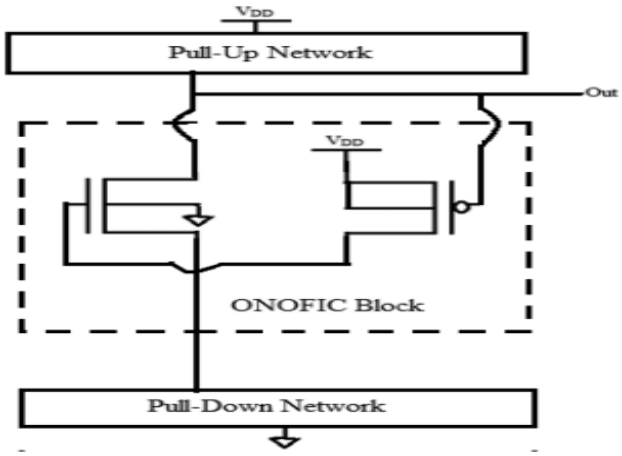

Fig. 2.2 ONOFIC Technique for CMOS Circuit

For any logic output both PMOS and NMOS should work in ON-OFF condition. This block is providing maximum equivalent resistance in the path of leakage current in OFF condition and it provides minimum equivalent resistance in ON condition which decreases the leakage current. Depending upon the output logic these transistors must be either in cutoff or in triode(linear) region. Fig. 2.2 shows the ON-OFIC technique. In this block the transistors are connected in specific manner such that source terminal of PMOS is connected to V_{DD} and the gate of PMOS is connected to output whereas the gate of NMOS is connected to drain terminal of PMOS.

2.2 Stack ONOFIC

In stack ONOFIC[1] technique the intermediate block having two nMOS Tr. also known as leakage control transistors (LCT) and one pMOS , are connected in particular way such that the drain terminal of pMOS is attached with gate of the both nMOS Tr. and gate terminal of pMOS Tr. is attached with the output of logic as shown in Fig. 2.3.

This block is providing maximum equivalent resistance in the path of leakage current in OFF condition and it provides minimum equivalent resistance in ON condition which reduces the leakage current. This technique is known as stack ONOFIC because for each output logic block should be either in ON state or in OFF state. The logic block of this technique affects the power dissipation by decreasing the current due to leakage in CMOS circuit.

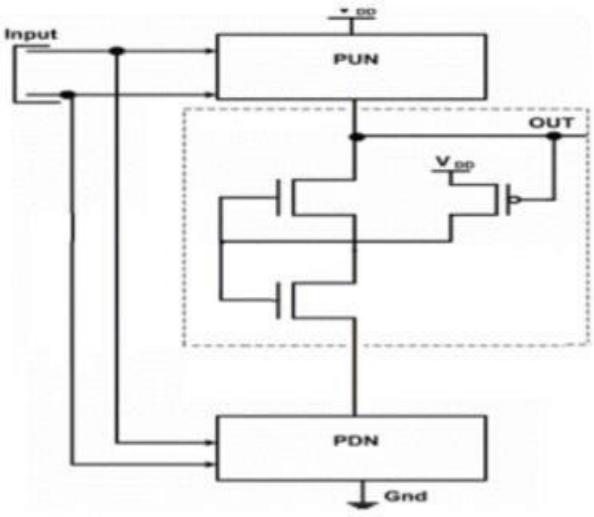

Fig. 2.3 Stack ONOFIC Technique for CMOS Circuit

2.3 LECTOR

The fundamental behind LECTOR[2] method in reduction of current due to leakage depends upon the proper stack of transistors in the way between V_{DD} and GND.

It is derived from the concept that a path having more than one OFF transistors between V_{DD} and GND has less chances of leakage current when compare to single OFF transistor between V_{DD} and GND.

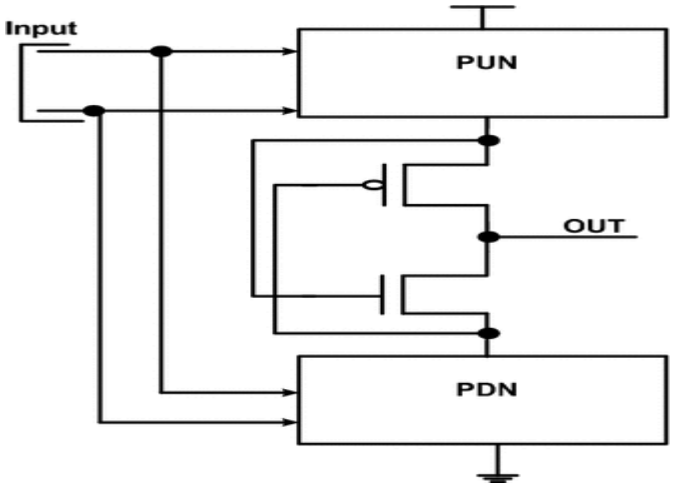

Fig. 2.4 LECTOR Technique for CMOS Circuit

Fig. 2.4 indicates the circuit of LECTOR. Here in logic block between PUN and PDN two leakage control transistors are connected as shown. Gate of both the transistors in logic block is controlled by the source of others so it is also called as self controlled

stacked transistors in which no outside circuit is needed. The connection of LCT ensures the maximum resistance in the path between V_{DD} and GND which decreases the leakage current possibility. In this method a pMOS is inserted near the PUN and nMOS is inserted near the PDN and gate terminal of every LCT is governed by source of other transistor. One LCT is in cut off mode and offer extra impedance in the way from V_{DD} and GND which decreases the sub-threshold leakage current and hence the static power.

2.4 LCPMOS

In LCPMOS technique[3] of leakage power reduction, one transistor (Leakage Control Transistor) is used which is governed by the output of the logic circuit. LCT used in this circuit increases the equivalent resistance of the path between the pull down network and ground due to which it increases the path resistance between V_{DD} and ground which helps in decreasing the leakage current as shown below in Fig. 2.5.

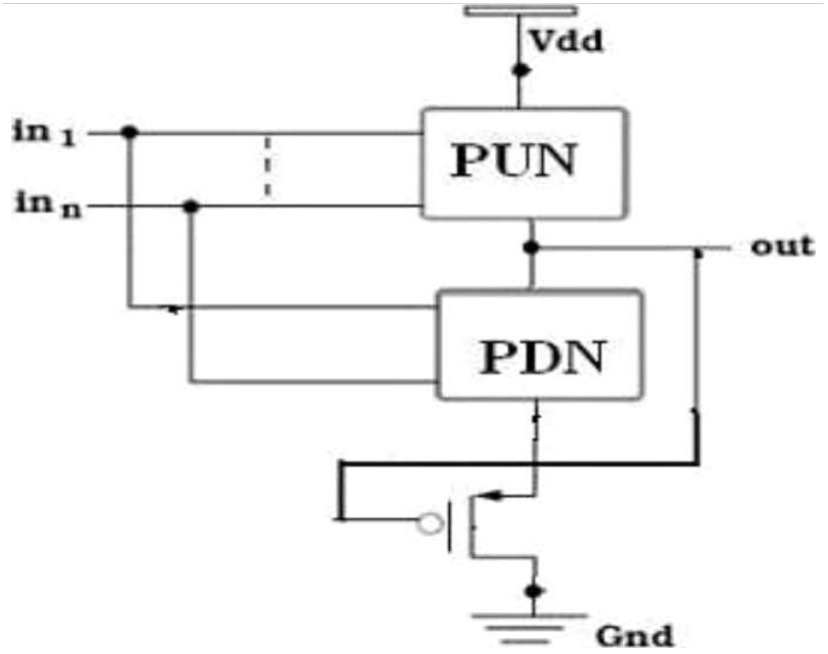

Fig. 2.5 LCPMOS Technique for CMOS Circuit

2.5 SUMMARY

In this chapter various leakage power reduction techniques such as ONOFIC, stack ONOFIC, LECTOR and LCPMOS have been discussed briefly along with their

circuit representation. These all techniques are self controllable and governed by output itself and do not require any extra signal which reduces the routing complexity.

CHAPTER 3
LEAKAGE REDUCTION TECHNIQUES ON UNIVERSAL GATES

In this chapter, the impact of various leakage power reduction techniques as discussed in Chapter 2, has been studied and compared on different universal gate circuits such as two input NAND gate and two input NOR gate which comes under the category of static circuits. The simulations are performed on LT spice tool at 32 nm technology node.

3.1 ONOFIC TECHNIQUE ON UNIVERSAL GATES

Here I have implemented ONOFIC leakage reduction techniques on universal gate circuits which are static circuits. Static CMOS is a logic circuit design technique whereby the output is always strongly driven due to it always being connected to either VDD or GND (except when switching). The ONOFIC technique has been simulated on 2 input NAND gate and 2 input NOR gate which are as follows:

3.1.1 TWO INPUT NAND GATE

Fig. 3.1 shows the schematic of 2 input NAND gate incorporated with the ONOFIC technique. The ONOFIC block is added between the pull up and pull down network to reduce the leakage current in the circuit.

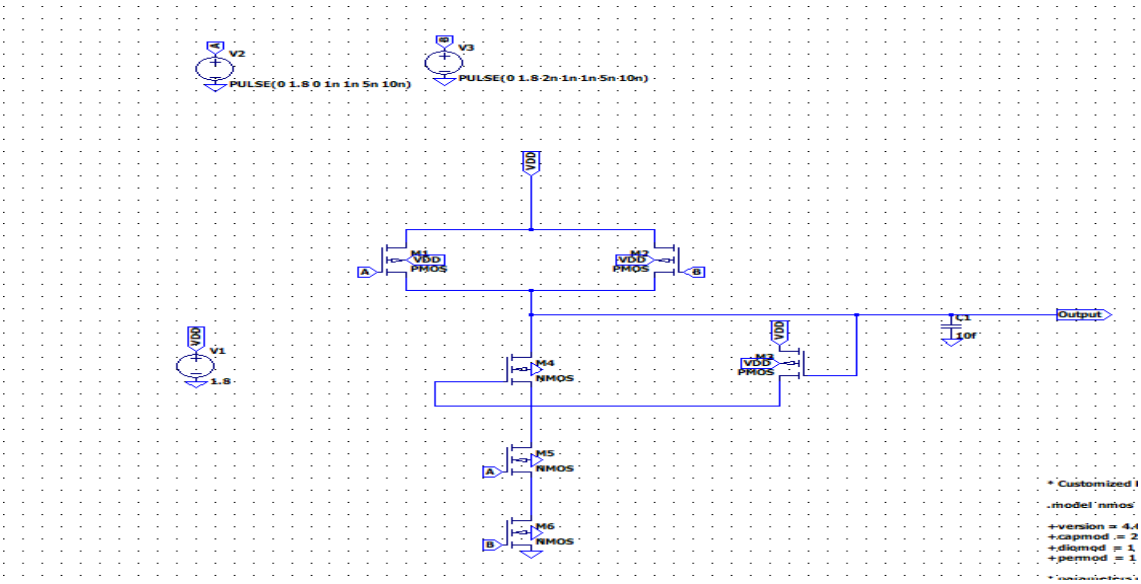

Fig 3.1 Two input NAND gate using ONOFIC

When both the inputs are HIGH the corresponding output is LOW and the PMOS of the ONOFIC block is ON and thereby the NMOS is also ON and it provides minimum resistance to the path in the ON state. For other input combinations the output is logic HIGH and correspondingly the ONOFIC block is OFF offering high resistance to the path and thereby reducing the leakage current.

For input A and input B the minimum voltage level is 0 V and the maximum voltage level is 1.8 V. The rise and fall time for both the inputs are 1ns.The time period for both inputs are 10ns.V_{DD} is 1.8 V and the load capacitance at the output will be 10 fF. The output waveform of this technique is shown in Fig 3.2, from the figure we can conclude that the circuit performs the desired function of NAND gate even after incorporating the ONOFIC block.

For the input combination (1,1) the output is low and for other inputs the output is high, thereby verifying with the functionality of the 2 input NAND gate. Since the voltage swing is full we can also conclude that the high noise margin property is intact and the circuit is immune to the noise.

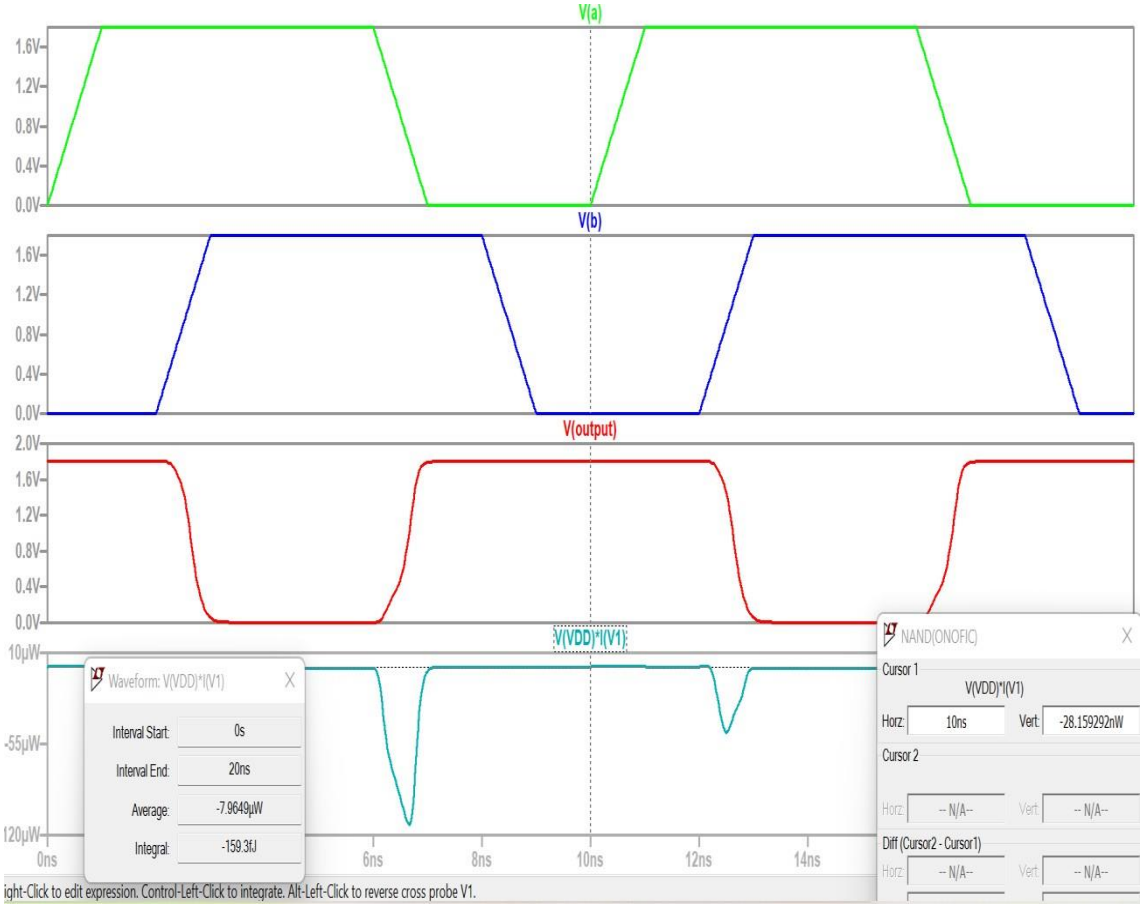

Fig. 3.2 Output of two input NAND gate using ONOFIC

In conventional 2 input NAND gate the average power consumption for all possible input combinations is 1.606µW, after applying ONOFIC technique the average power consumption for all possible input combinations is 239.67 nW which shows that power consumption has been reduced.

3.1.2 TWO INPUT NOR GATE

The schematic of 2 input NOR gate is shown in Fig 3.3. When either of the input is HIGH, the output is LOW, so the PMOS in ONOFIC block is ON and the drain of PMOS is connected to gate of NMOS, so the NMOS is also ON and the ONOFIC block offers minimum resistance to the path. When both the inputs are low the output should be logic high which will turn OFF the ONOFIC block, providing maximum resistance in the path which will reduce the leakage current. For input A and input B the minimum voltage level is 0 V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns.V_{DD} is 1.8 V and the load capacitance at the output will be 10fF.

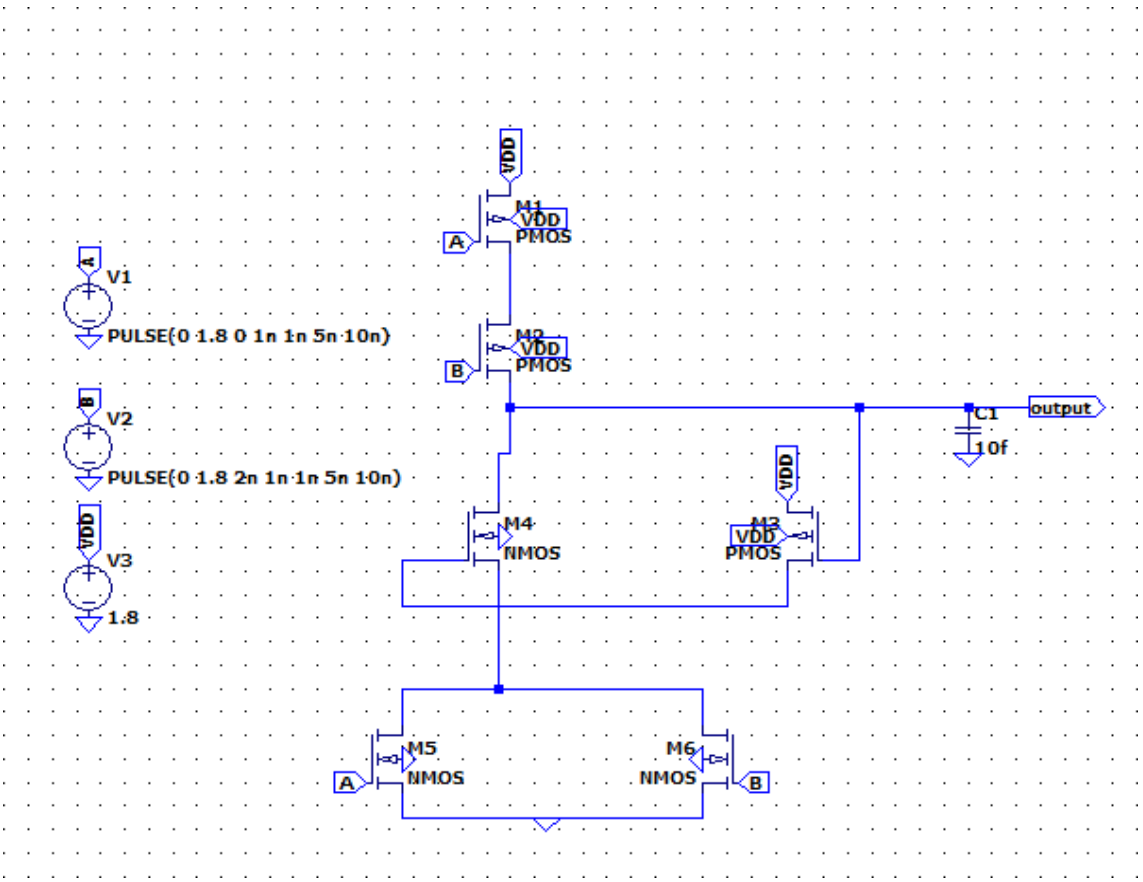

Fig. 3.3 Schematic of two input NOR gate using ONOFIC

The output of the above circuit is shown in Fig 3.4. The output is HIGH only when both the inputs are LOW and otherwise the output is LOW, verifying the functionality of the conventional 2 input NOR gate. Since the output swing is from 0 to V_{DD} we could conclude that the noise margin of this circuit is high and the circuit is immune to noise.

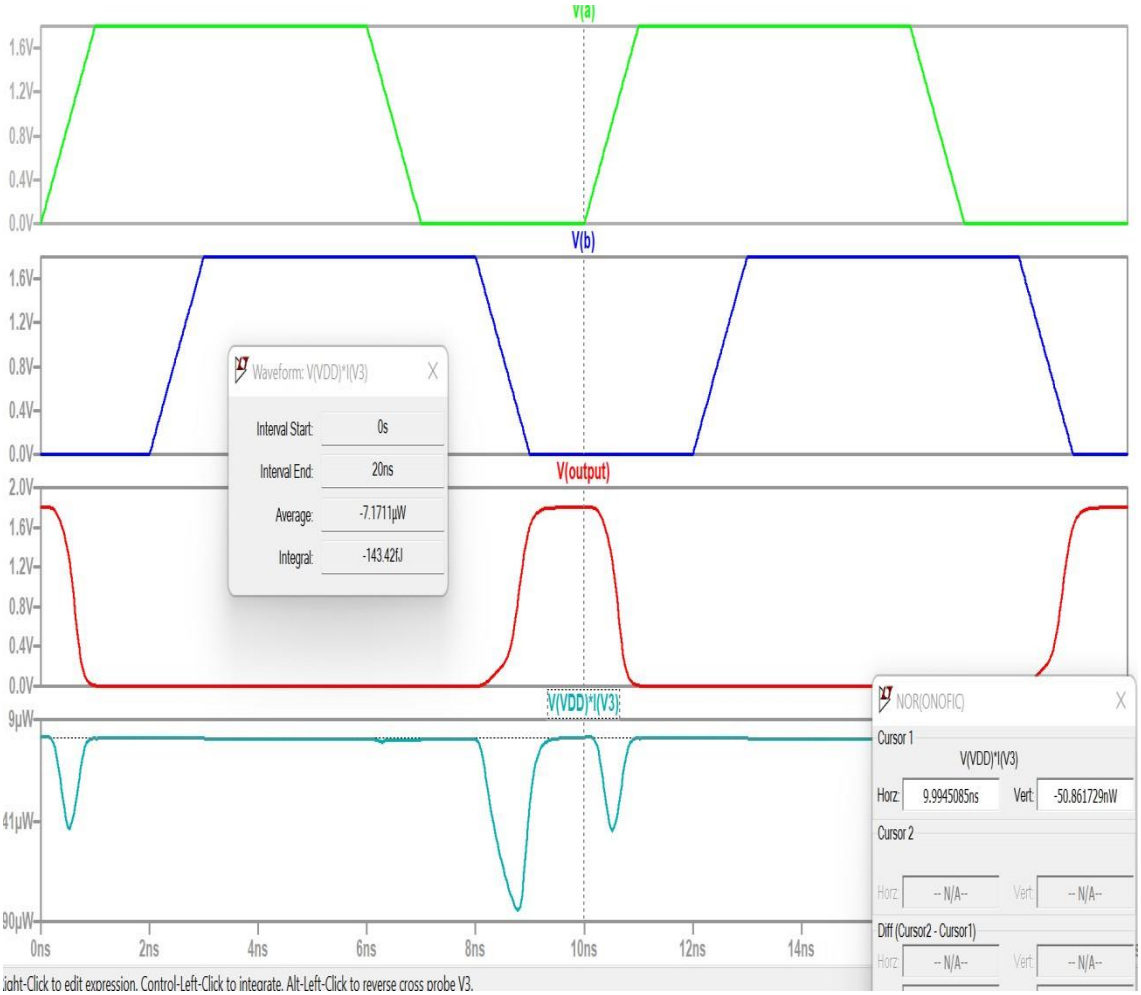

Fig 3.4 Output of two input NOR gate using ONOFIC

In conventional 2 input NOR gate the average power consumption for all possible input combinations is 909.784 nW, after applying ONOFIC technique the average power consumption for all possible input combinations is 274.29 nW which shows that power consumption has been reduced.

3.2 Stack ONOFIC TECHNIQUE ON UNIVERSAL GATES

Here I have implemented Stack ONOFIC leakage reduction techniques on universal gate circuits which are static circuits. Static CMOS is a logic circuit design technique whereby

the output is always strongly driven due to it always being connected to either VDD or GND (except when switching). The Stack ONOFIC technique has been simulated on 2 input NAND gate and 2 input NOR gate which are as follows:

3.2.1 TWO INPUT NAND GATE

Fig 3.5 shows the schematic of 2 input NAND gate incorporated with the stack ONOFIC technique. The stack ONOFIC block is added between the pull up and pull down network to reduce the leakage current in the circuit. When both the inputs are HIGH the corresponding output is LOW and the pMOS of the stack ONOFIC block is ON and thereby both the nMOS is also ON and it presents minimum resistance to the path in the ON state. For other input combinations the output is logic HIGH and correspondingly the stack ONOFIC block is OFF offering high resistance to the path and thereby reducing the leakage current.

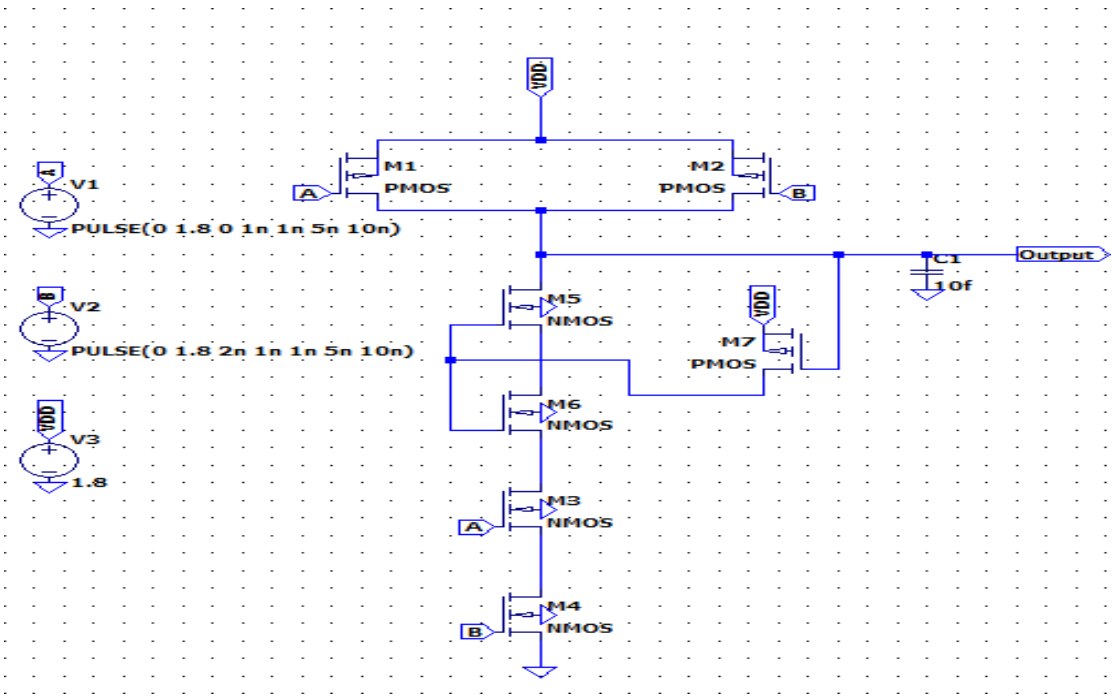

Fig 3.5 Schematic of two input NAND gate using stack ONOFIC technique

For input A and input B the minimum voltage level is 0V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8V and the load capacitanceat the output will be 10fF. The clock signal having time period 10ns is applied to the circuit.

The output waveform of this technique is shown in Fig 3.6, from the figure we can conclude that the circuit performs the desired function of NAND gate even after incorporating the STACK ONOFIC block. For the input combination (1,1) the output is low and for other inputs the output is high, thereby verifying with the functionality of the 2 input NAND gate.

Since the voltage swing is full we can also conclude that the high noise margin property is intact and the circuit is immune to the noise.

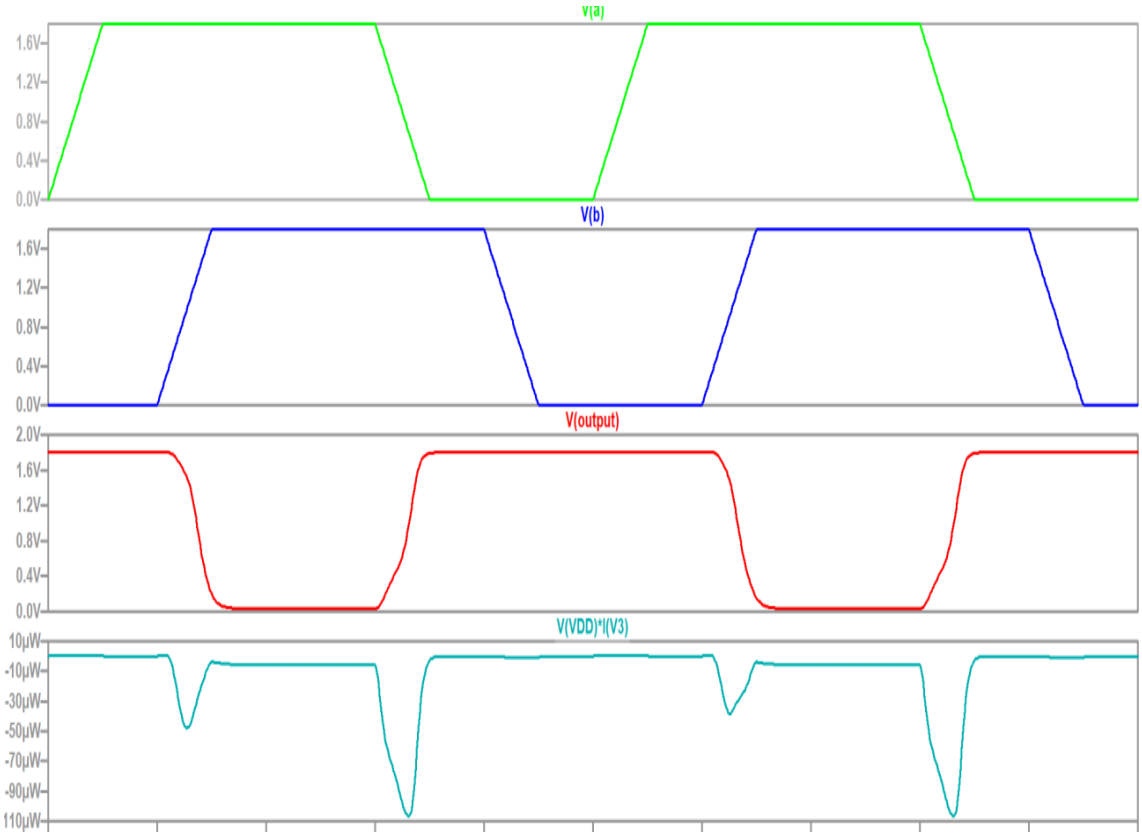

Fig 3.6 Output of two input NAND gate using stack ONOFIC technique

In conventional 2 input NAND gate the average power consumption for all possible input combinations is 1.606 µW, after applying stack ONOFIC technique the average power consumption for all possible input combinations is 1392.391 nW which shows that power consumption has been reduced.

3.2.2 TWO INPUT NOR GATE

The schematic of 2 input NOR gate is shown in fig 3.7. When either of the input is HIGH, the output is LOW so the pMOS in stack ONOFIC block is ON and the drain of pMOS

is connected to gate of nMOS , so the nMOS is also ON and the ONOFIC block offers minimum resistance to the path . When both the inputs are LOW the output should be logic HIGH which will turn OFF the stack ONOFIC block, providing maximum resistance in the path which will reduce the leakage current.

For input A and input B the minimum voltage level is 0 V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8 V and the load capacitance at the output will be 10fF.

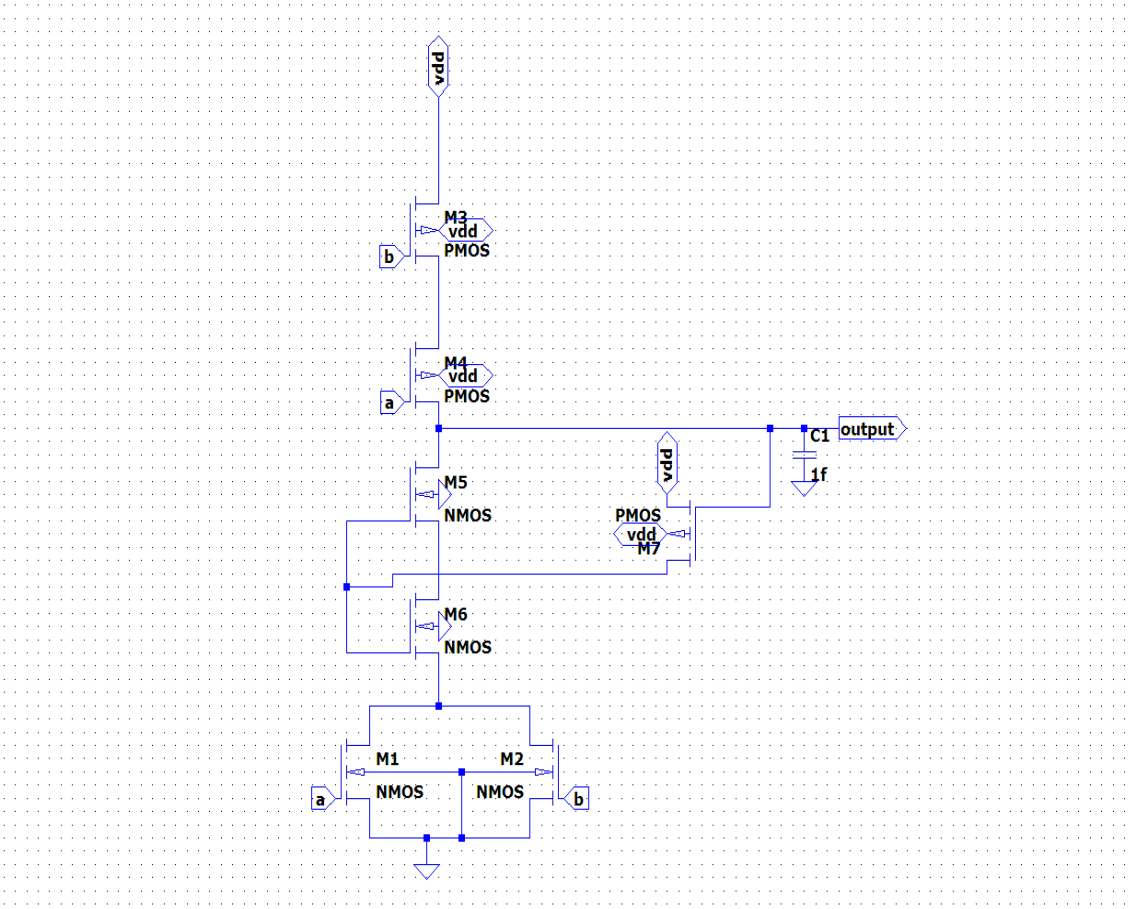

Fig 3.7 Schematic of two input NOR gate using stack ONOFIC technique

The output of the above circuit is shown in fig 3.8. The output is HIGH only when both the inputs are LOW and otherwise the output is LOW, verifying the functionality of the conventional 2 input NOR gate. The output swing is from 0 to V_{DD} so we could conclude that the noise margin of this circuit is high and the circuit is immune to noise .

In conventional 2 input NOR gate the average power consumption for all possible input

combinations is 909.784 nW, after applying stack ONOFIC technique the average power consumption for all possible input combinations is 267.6 nW which shows that power consumption has been reduced.

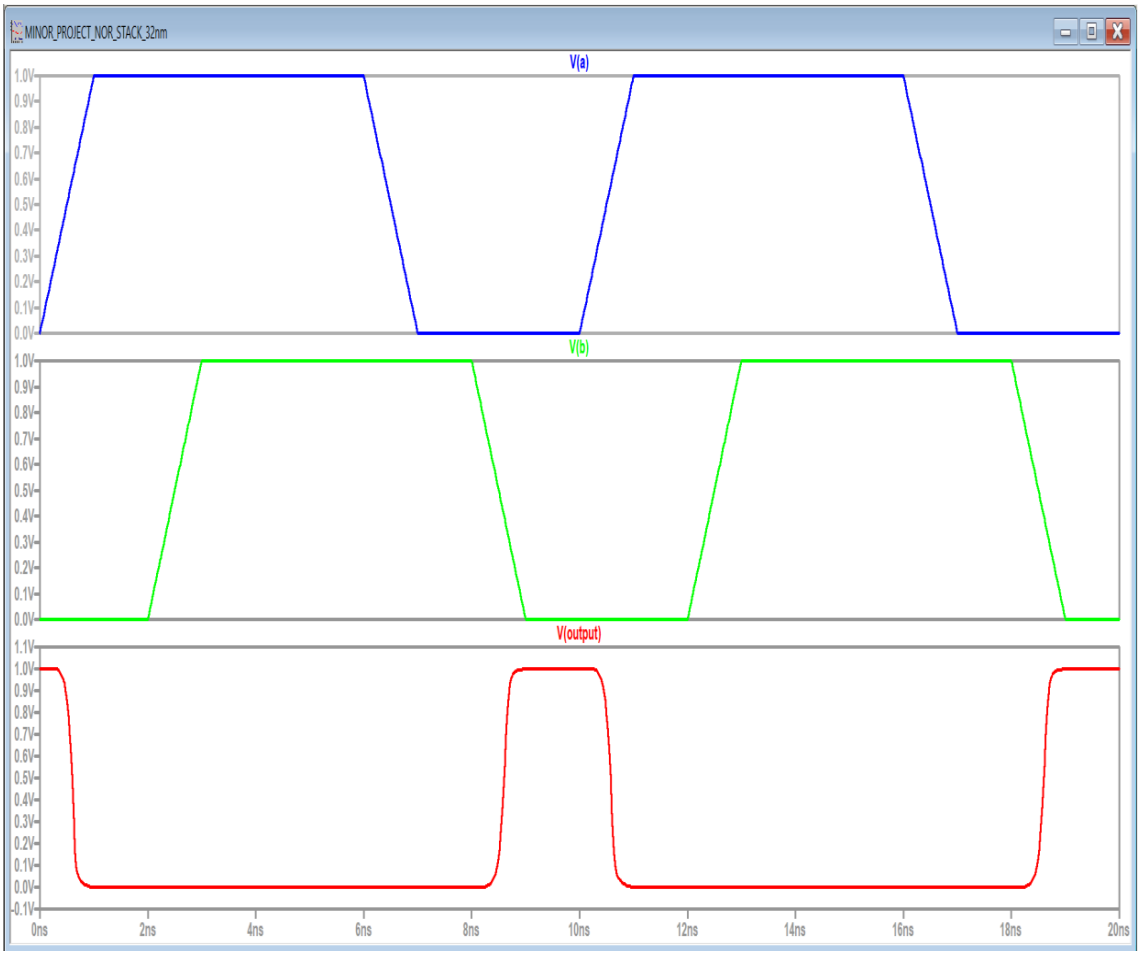

Fig 3.8 Output of two input NOR gate using stack ONOFIC technique

3.3 LECTOR TECHNIQUE ON UNIVERSAL GATES

Here I have implemented LECTOR leakage reduction techniques on universal gate circuits which are static circuits. Static CMOS is a logic circuit design technique whereby the output is always strongly driven due to it always being connected to either VDD or GND (except when switching). The LECTOR technique has been simulated on 2 input NAND gate and 2 input NOR gate which are as follows:

3.3.1 TWO INPUT NAND GATE

Fig 3.9 shows the schematic of 2 input NAND gate incorporated with the LECTOR

technique. The LECTOR block is added between the pull up and pull down network to reduce the leakage current in the circuit. The LECTOR block offering high resistance to the path and thereby reducing the leakage current.

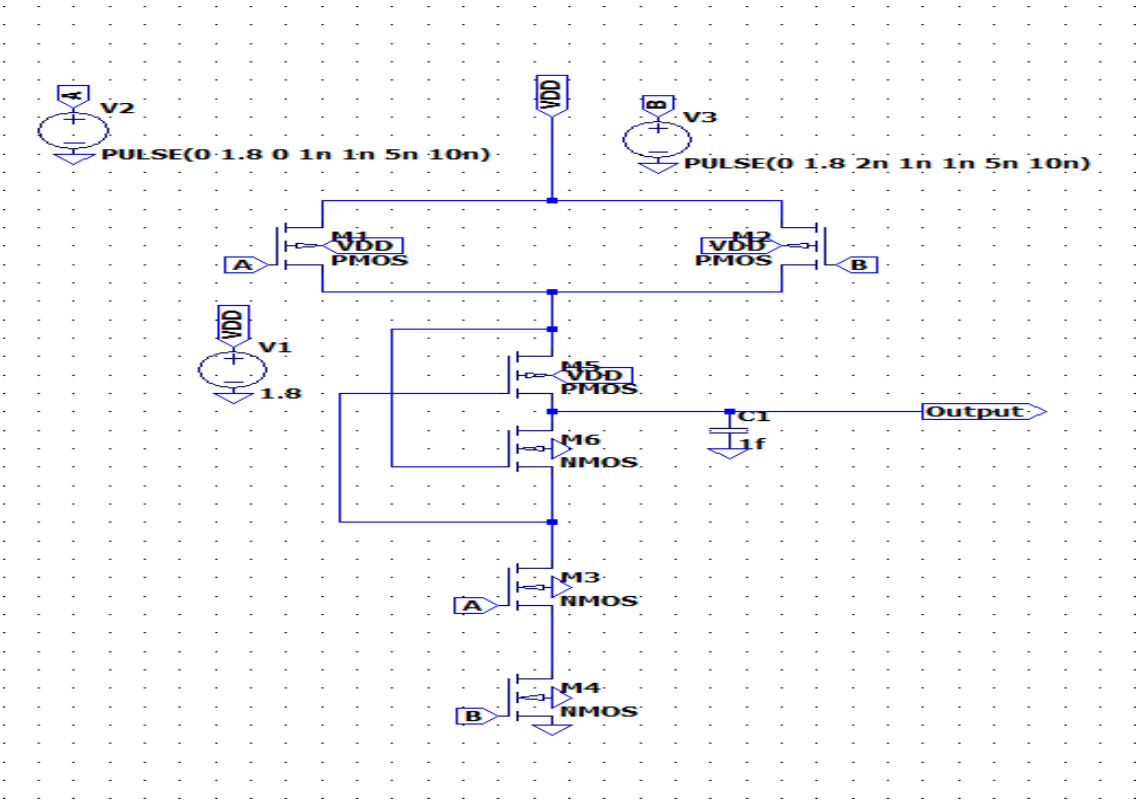

Fig 3.9 Two input NAND gate using Lector technique

For input A and input B the minimum voltage level is 0V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8V and the load capacitanceat the output will be 10fF. The clock signal having time period 10ns is applied to the circuit.

The output waveform of this technique is shown in Fig 3.10, from the figure we can conclude that the circuit performs the desired function of NAND gate even after incorporating the LECTOR block. For the input combination (1,1) the output is low and for other inputs the output is high, thereby verifying with the functionality of the 2 input NAND gate.

Since the voltage swing is full, we can also conclude that the high noise margin property

is intact and the circuit is immune to the noise.

In conventional 2 input NAND gate the average power consumption for all possible input combinations is 1.606 µW, after applying LECTOR technique the average power consumption for all possible input combinations is 20.544 nW which shows that power consumption has been reduced.

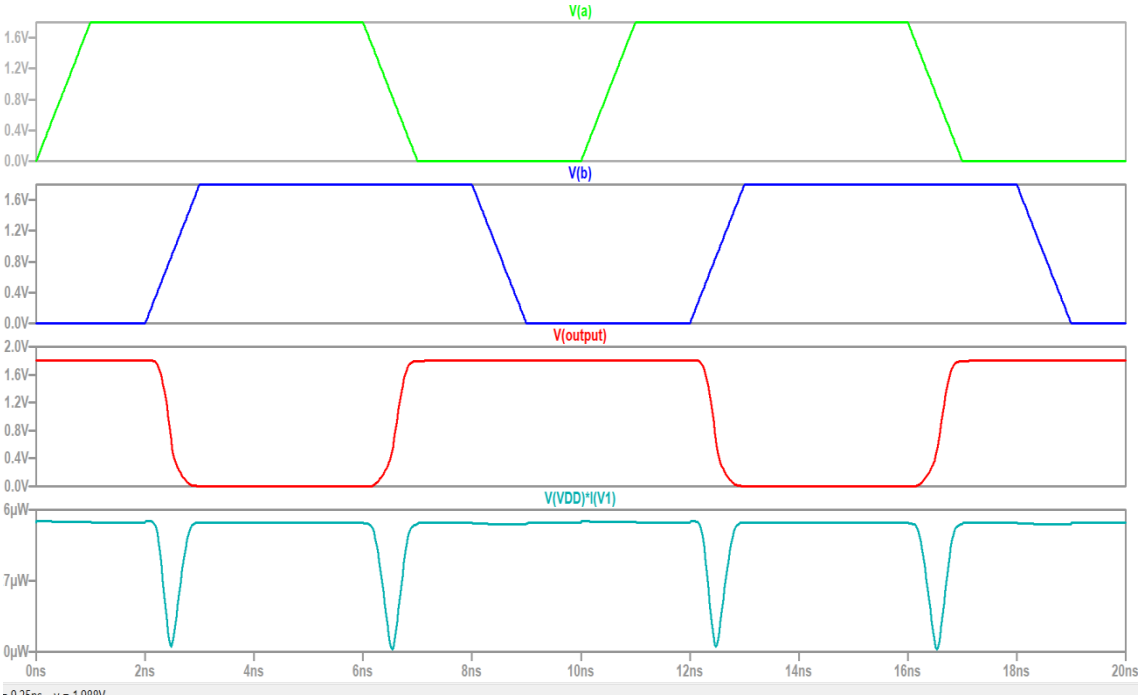

Fig 3.10 Output of two input NAND gate using Lector technique

3.3.2 TWO INPUT NOR GATE

Fig 3.11 shows the schematic of 2 input NOR gate incorporated with the LECTOR technique. The LECTOR block is added between the pull up and pull down network to reduce the leakage current in the circuit. The LECTOR block offering high resistance to the path and thereby reducing the leakage current.

For input A and input B the minimum voltage level is 0V and the maximum voltage level is 1.8V.delay for input A is 0ns whereas delay provided to input B is 2ns. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8V and the load capacitanceat the output will be 10fF. The clock signal having time period 10ns is applied to the circuit.

The output of the above circuit is shown in fig 3.12. The output is high only when both the inputs are low and otherwise the output is low, verifying the functionality of the

conventional 2 input NOR gate . The output swing is from 0 to V_{DD} so we could conclude that the noise margin of this circuit is high and the circuit is immune to noise .

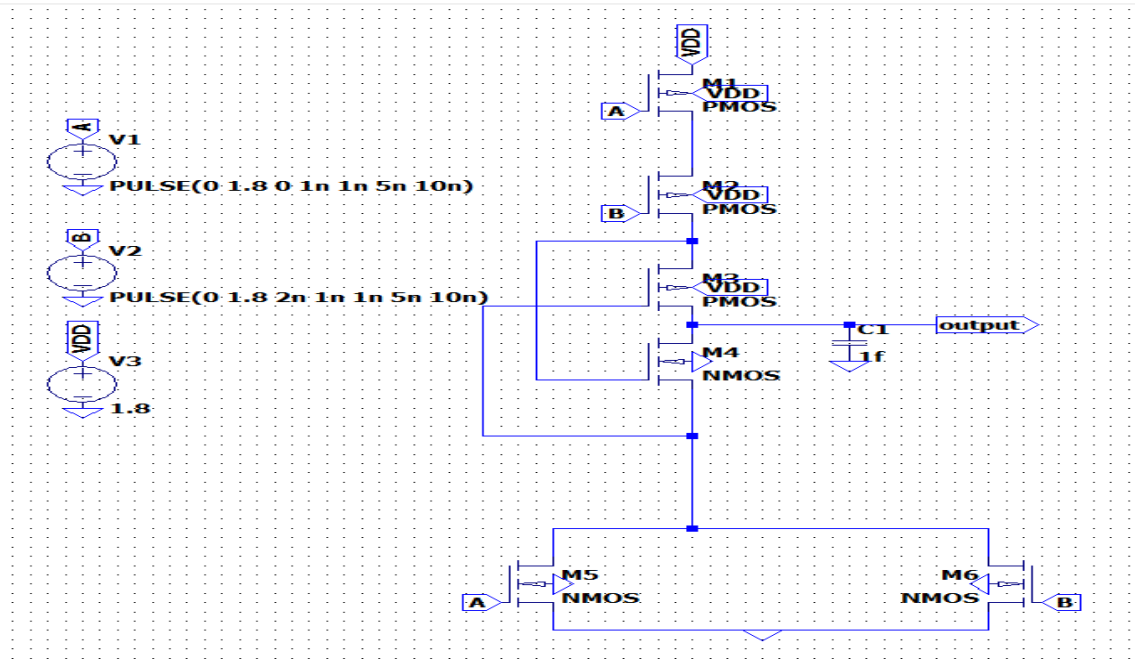

Fig 3.11 Two input NOR gate using Lector technique

In conventional 2 input NOR gate the average power consumption for all possible input combinations is 909.784 µW, after applying LECTOR technique the average power consumption for all possible input combinations is 17.73 nW which shows that power consumption has been reduced.

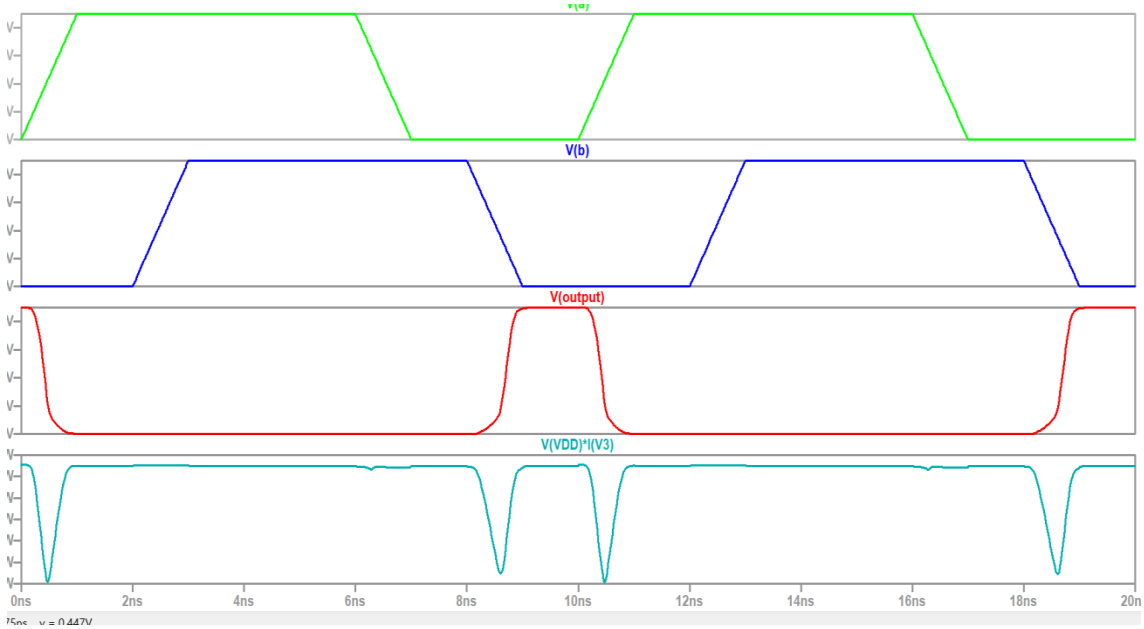

Fig 3.12 Output of two input NOR gate using Lector technique

3.4 LCPMOS TECHNIQUE ON UNIVERSAL GATES

Here I have implemented LCPMOS leakage reduction techniques on universal gate circuits which are static circuits. Static CMOS is a logic circuit design technique whereby the output is always strongly driven due to it always being connected to either VDD or GND (except when switching). The LCPMOS technique has been simulated on 2 input NAND gate and 2 input NOR gate which are as follows:

3.4.1 TWO INPUT NAND GATE

Fig 3.13 shows the schematic of 2 input NAND gate incorporated with the LCPMOS technique. The LCPMOS block is added between the pull down network and GND to reduce the leakage current in the circuit. The LCPMOS block offering high resistance to the path and thereby reducing the leakage current.

For input A and input B the minimum voltage level is 0V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8V and the load capacitanceat the output will be 0.01fF. The clock signal having time period 10ns is applied to the circuit.

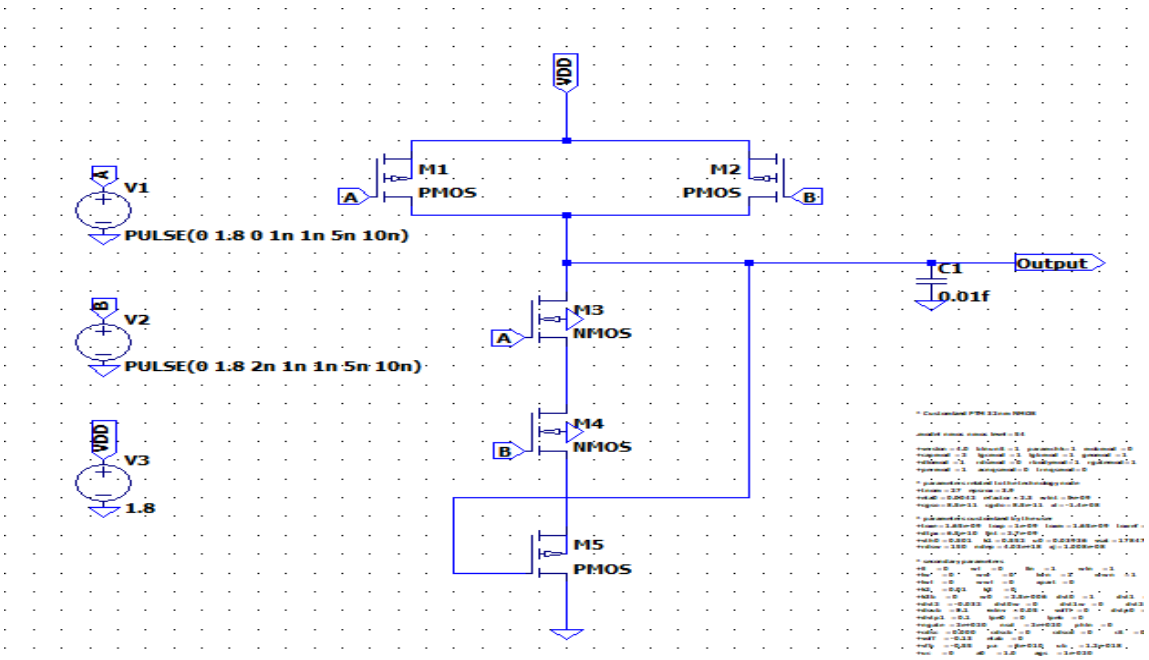

Fig 3.13 Two input NAND gate using LCPMOS technique

The output waveform of this technique is shown in Fig 3.14, from the figure we can conclude that the circuit performs the desired function of NAND gate even after

incorporating the LCPMOS block . For the input combination (1,1) the output is low and for other inputs the output is high, thereby verifying with the functionality of the 2input NAND gate.

Since the voltage swing is full we can also conclude that the high noise margin property is intact and the circuit is immune to the noise.

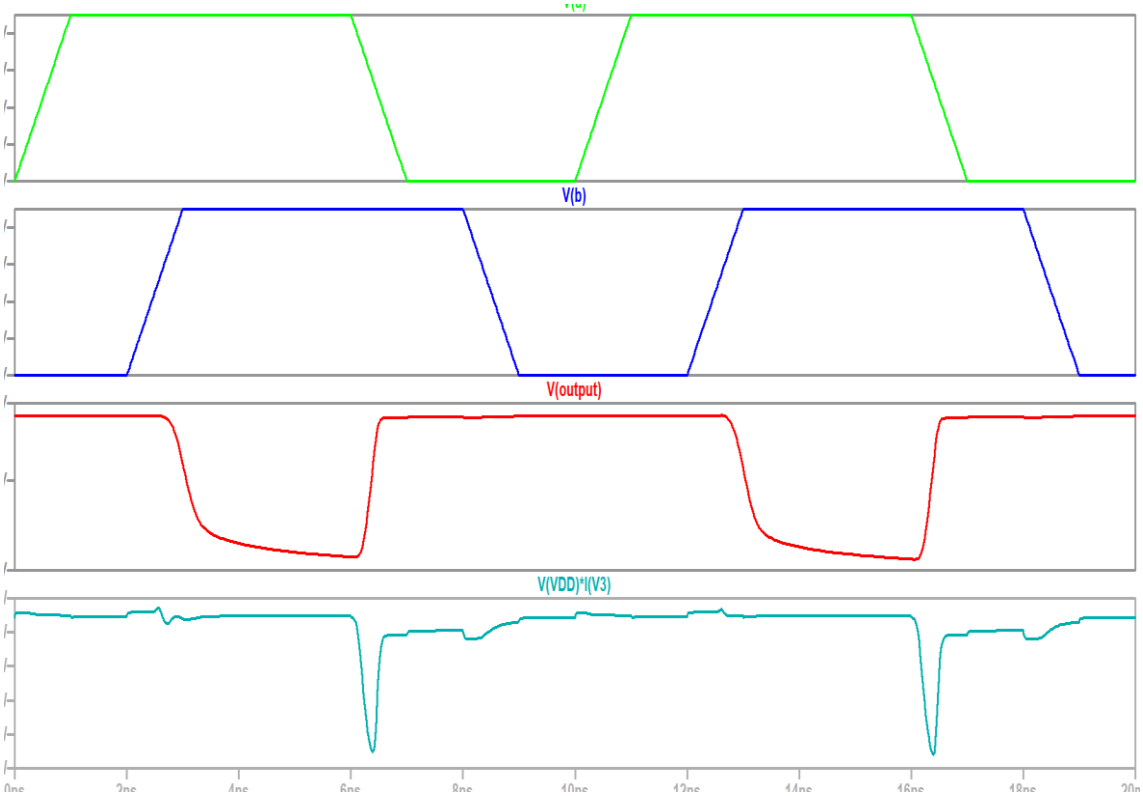

Fig 3.14 Output of two input NAND gate using LCPMOS technique

In conventional 2 input NAND gate the average power consumption for each possible input combinations is 1.606 µW, after applying LCPMOS technique the average power consumption for each possible input combinations is 220.609 nW which shows that power consumption has been reduced.

3.4.2 TWO INPUT NOR GATE

Fig 3.15 shows the schematic of 2 input NOR gate incorporated with the LCPMOS technique. The LCPMOS block is added between the pull down network and GND to reduce the leakage currentin the circuit. The LCPMOS block offering high resistance to the path and thereby reducing the leakage current.

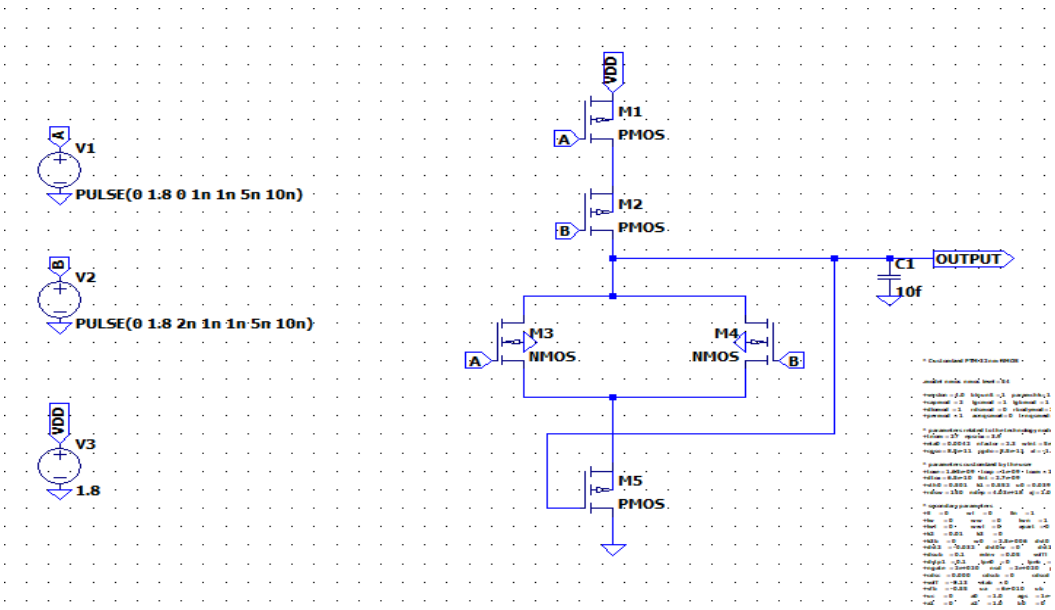

Fig 3.15 Two input NOR gate using LCPMOS technique

For input A and input B the minimum voltage level is 0V and the maximum voltage level is 1.8V. The rise and fall time for both the inputs are 1ns. The time period for both inputs are 10ns. V_{DD} is 1.8V and the load capacitance at the output will be 10fF.

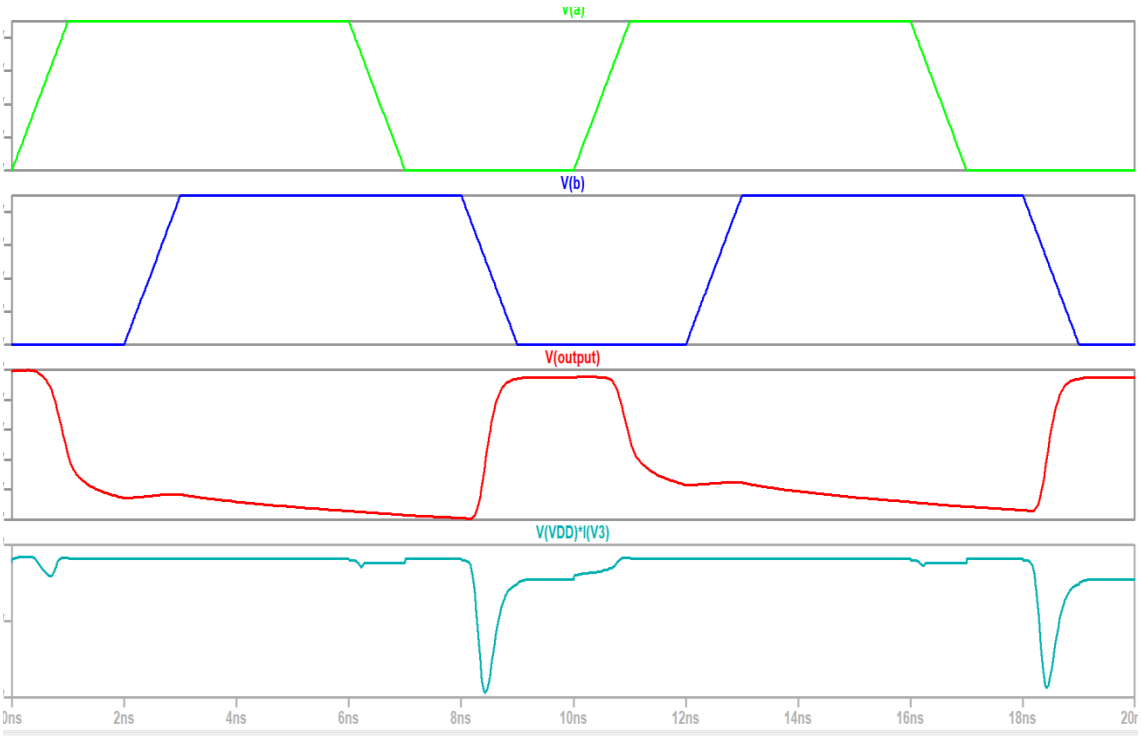

Fig 3.16 Output of two input NOR gate using LCPMOS technique

The clock signal having time period 10ns is applied to the circuit. The output of the above circuit is shown in Fig 3.16. The output is high only when both the inputs are low and otherwise the output is low, verifying the functionality of the conventional 2 input NOR gate. The output swing is from 0 to V_{DD} so we could conclude that the noise margin of this circuit is high and the circuit is immune to noise.

In conventional 2 input NOR gate the average power consumption for each possible input combinations is 909.784 nW, after applying LCPMOS technique the average power consumption for each possible input combinations is 147.6 nW which shows that power consumption has been reduced.

3.5 SUMMARY

In this chapter , I discussed the impact of various leakage power reduction techniques on universal gates like NAND and NOR.

The tabular comparison of power consumption for each input combinations and after including each technique is shown below in table 3.1 and 3.2:

Table 3.1 Power comparison among different NAND gates

Inputs (A,B)	Conventional	ONOFIC	Stack ONOFIC	LECTOR	LCPMOS
0,0	204.34 nW	18.029 nW	14.585 nW	18.267 nW	356.65 nW
0,1	262.75 nW	18.898 nW	15.172 nW	19.815 nW	341.84 nW
1,0	18.518 nW	17.402 nW	14.807 nW	17.596 nW	168.39 nW
1,1	5.939 µW	904.36 nW	5.525 µW	26.496 nW	15.558 nW
Average→	1.606 µW	239.672nW	1392.391 nW	20.544nW	220.609nW

Table 3.2 Power comparison among different NOR gates

Inputs (A,B)	Conventional	ONOFIC	Stack ONOFIC	LECTOR	LCPMOS
0,0	517.66 nW	35.64 nW	39.93 nW	37.924 nW	538.53 nW
0,1	2.823 µW	549.75 nW	517.37 nW	21.741 nW	28.72 nW
1,0	236.17 nW	183.57 nW	201.37 nW	10.958 nW	23.001 nW
1,1	62.305 nW	328.26 nW	311.731 nW	325.88 pW	218.96 pW
Average→	909.784 nW	239.67 nW	267.6 nW	17.73 nW	147.6 nW

CHAPTER 4
LEAKAGE REDUCTION TECHNIQUE IN D-FF

In combinational circuits the output of any state depends upon the present inputs only and there is absence of memory element in combinational circuits. There is no role of clock signal in the design of combinational circuits.eg- half adder, full adder, MUX etc. In case of sequential circuits the output of any state depends upon the present inputs as well as past outputs. The sequential circuits consist of memory elements also in feedback path. In sequential circuit clock signal is also present.eg- flipflops, counters, registers etc.

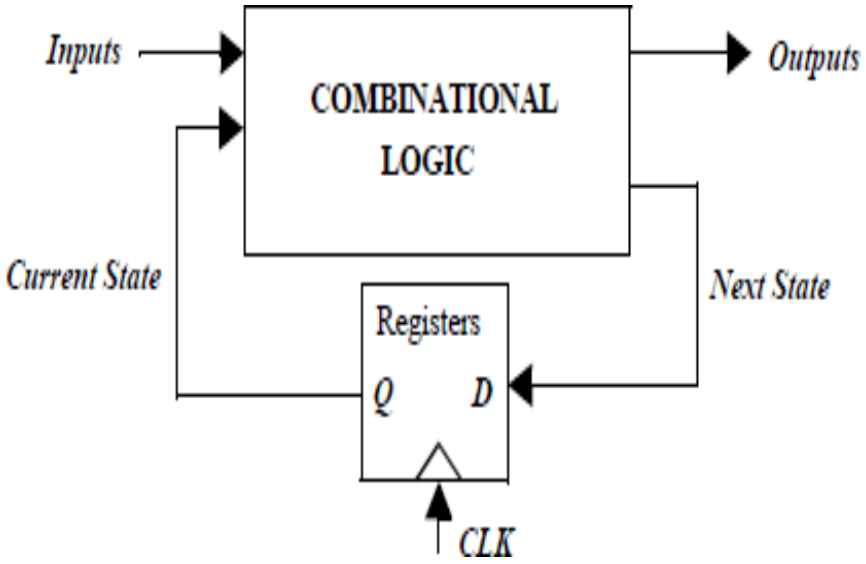

Fig 4.1 Sequential Circuit

In this chapter, the impact of various leakage power reduction techniques as discussed in Chapter 2, has been studied and compared on D-FF circuit which consist of inverters and transmission gates. The inverters used in D-FF circuit have been implemented using different leakage power reduction techniques and then inserted in the D-FF design. The simulations are performed on LT spice tool at 32 nm technology node.

4.1 ONOFIC TECHNIQUE ON D-FF

Here D FF is implemented using transmission gates and CMOS inverters as shown below in Fig. 4.2. The inverters used in this design is implemented using ONOFIC technique[5].

The input D value is in between 0V and 1 V i.e. maximum value is 1 V and minimum is 0 V. No delay is applied to input and the rise and fall time is 0.1ns.

The time period of the input is 30ns. The clock signal which is applied having time period of 16 ns and both rise and fall time is 0.1ns.

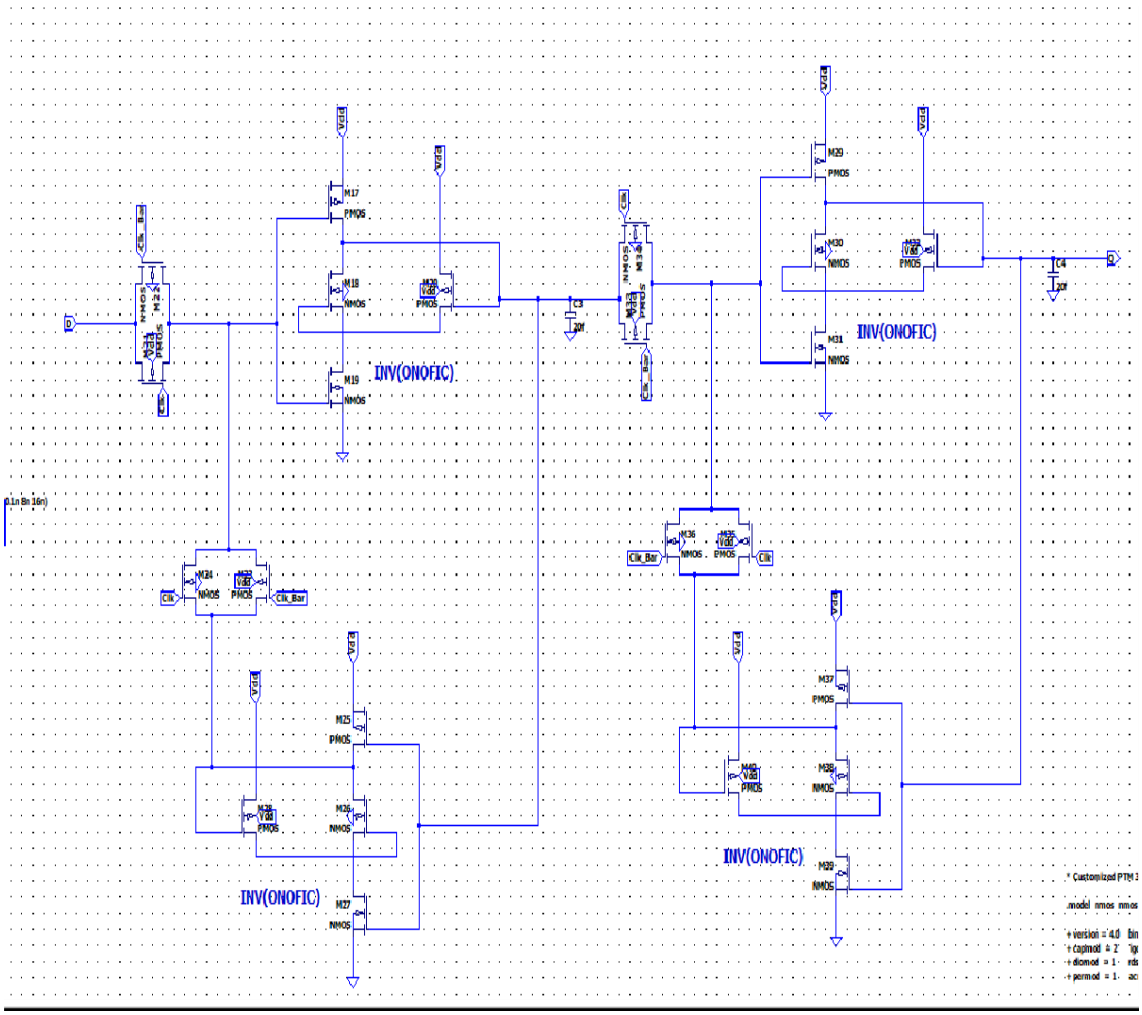

Fig 4.2 Schematic of DFF using ONOFIC technique

The output waveform shown in fig 4.3 justify the functionality of DFF i.e. output Q follows the input D between two positive edges of the clock signal.

In conventional D-ff the power consumption is 4.302 µW, after applying ONOFIC technique thepower consumption is 381.07 nW which shows that power consumption has been reduced.

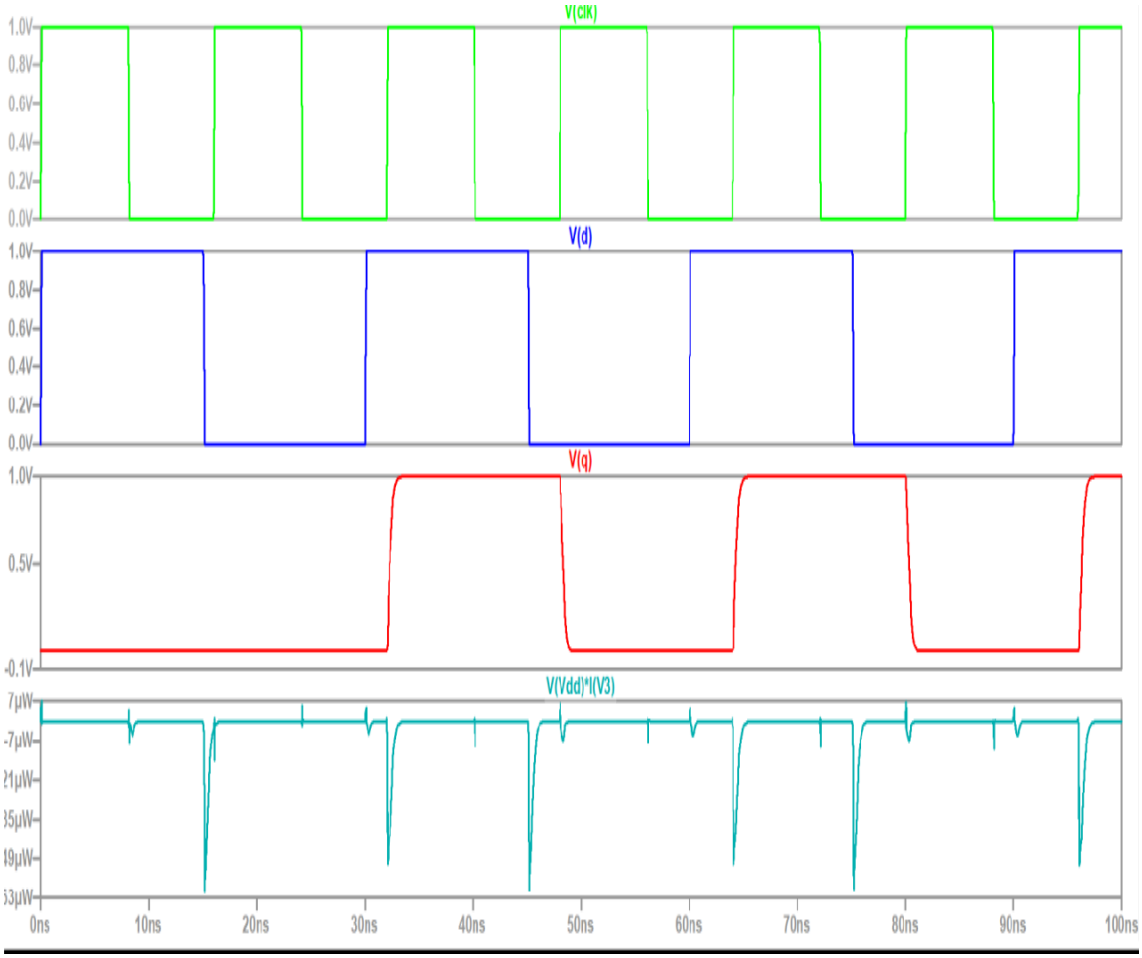

Fig 4.3 Output of DFF using ONOFIC technique

4.2 STACK ONOFIC TECHNIQUE ON D-FF

Here D FF is implemented using transmission gates and CMOS inverters as shown below in Fig. 4.4. The inverters used in this design is implemented using stack ONOFIC technique. The input D value is in between 0V and 1 V i.e. maximum value is 1 V and minimum is 0 V. No delay is applied to input and the rise and fall time is 0.1ns. The time period of the input is 30ns. The clock signal which is applied having time period of 16 ns and both rise and fall time is 0.1ns.

The output waveform shown in Fig 4.5 justify the functionality of DFF i.e. output Q follows the input D between two positive edges of the clock signal.

In conventional D-ff the power consumption is 4.302 µW, after applying stack ONOFIC

technique the power consumption is 395.28 nW which shows that power consumption has been reduced.

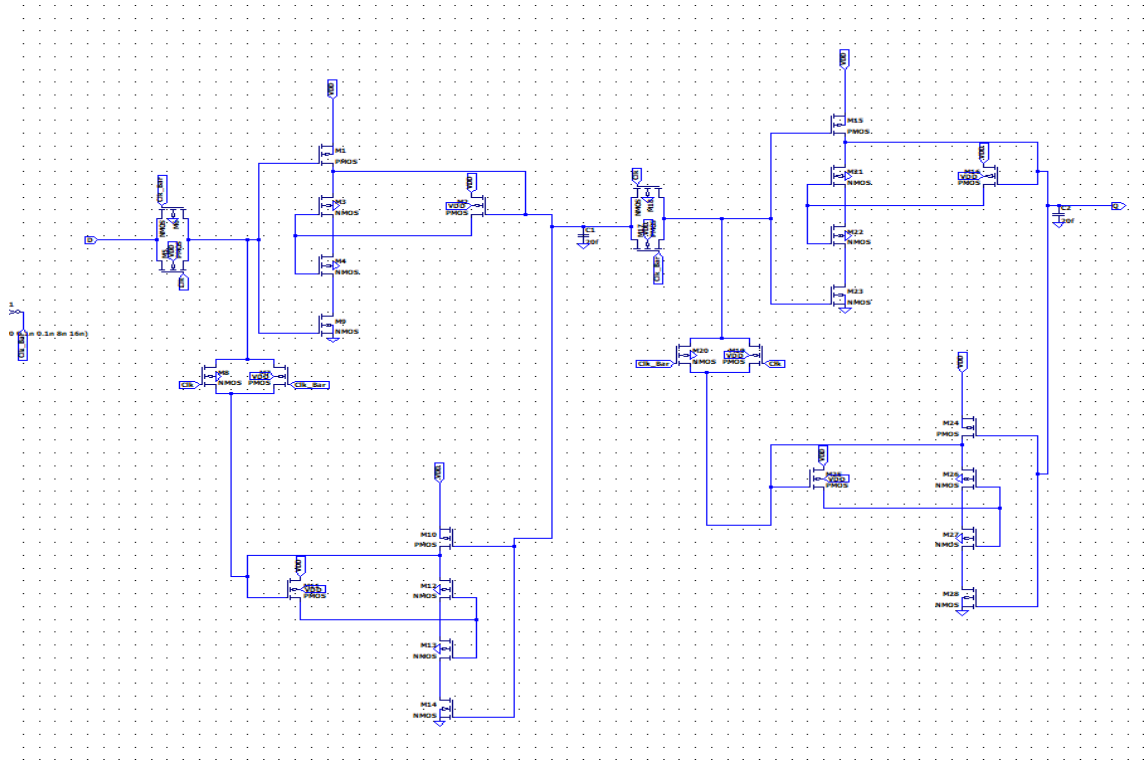

Fig 4.4 Schematic of DFF with stack ONOFIC

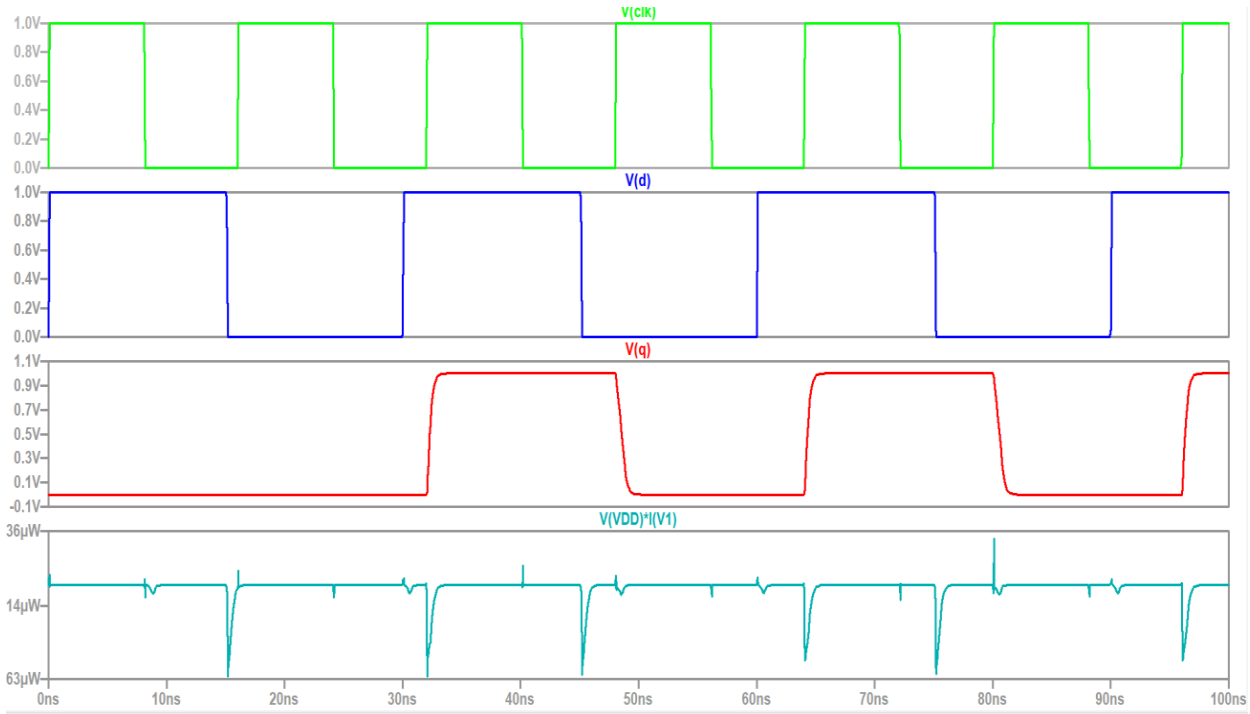

Fig 4.5 Output of DFF using stack ONOFIC

4.3 LECTOR TECHNIQUE ON D-FF

Here D FF is implemented using transmission gates and CMOS inverters as shown below in Fig. 4.6. The inverters used in this design is implemented using LECTOR technique. The input D value is in between 0V and 1 V i.e. maximum value is 1 V and minimum is 0 V. No delay is applied to input and the rise and fall time is 0.1ns. The time period of the input is 30ns. The clock signal which is applied having time period of 16 ns and both rise and fall time is 0.1ns.

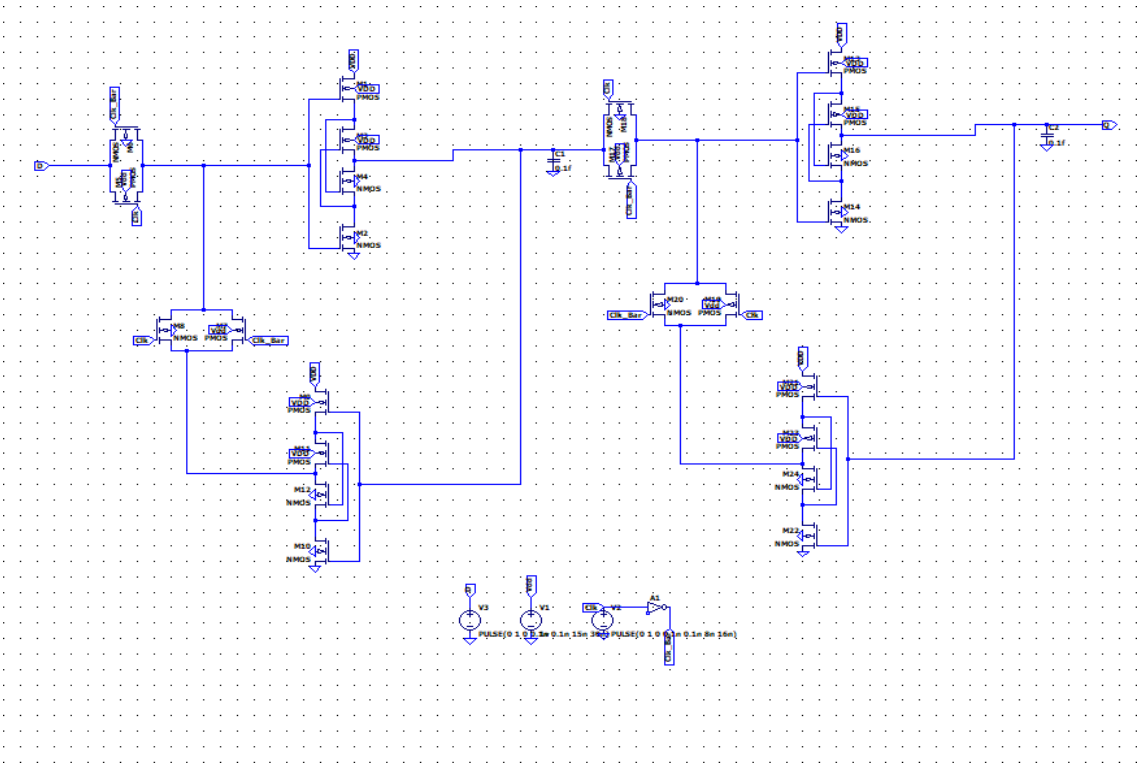

Fig 4.6 Schematic of DFF with Lector

The output waveform shown in Fig 4.7 justify the functionality of DFF. i.e. output Q follows the input D between two positive edges of the clock signal.

In conventional D-ff the power consumption is 4.302µW, after applying LECTOR technique the power consumption is 37.14 nW which shows that power consumption has been reduced.

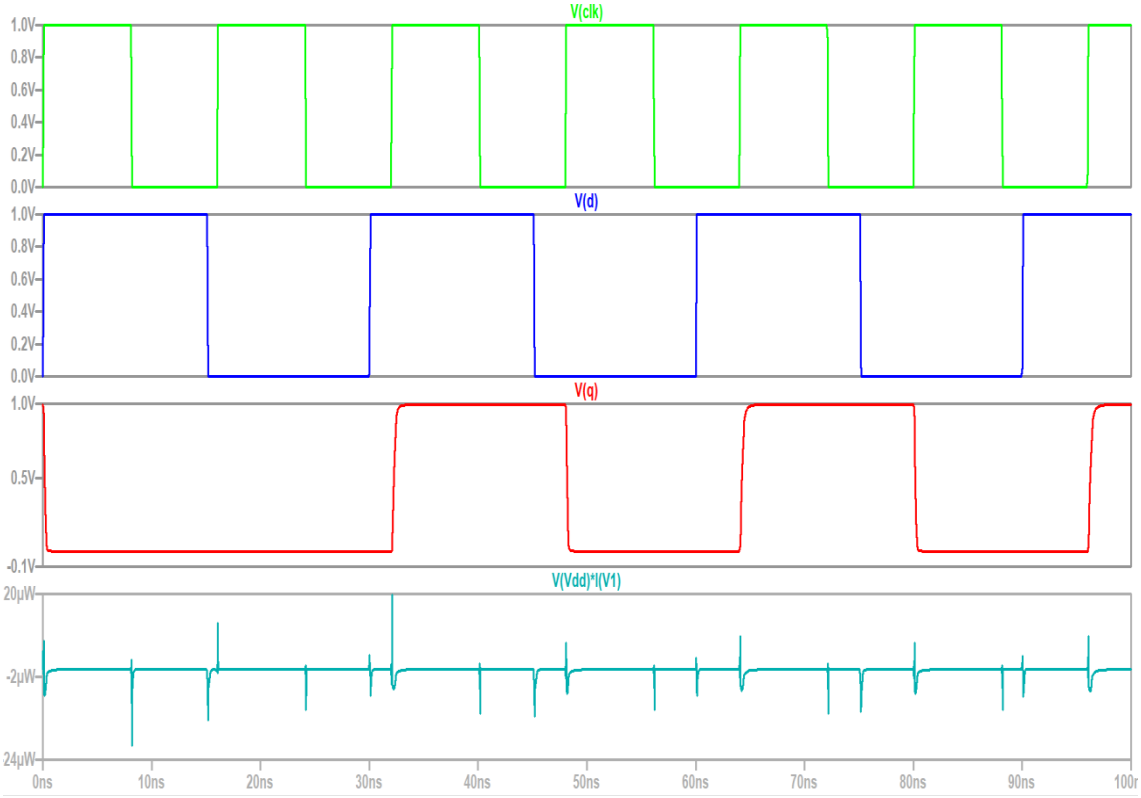

Fig 4.7 Output of DFF using Lector

4.4 SUMMARY

In this chapter , I discussed the impact of various leakage power reduction techniques on D-FF.

The tabular comparison of power consumption for each clock combinations and after including each technique is shown below in table 4.1 :

Table 4.1 Power comparison among different D-FF circuits

CLK	Conventional	ONOFIC	Stack ONOFIC	LECTOR
0	6.899 µW	740.3 nW	766.85 nW	67.388 nW
1	1.705 µW	381.07 nW	395.28 nW	37.13 nW
Average→	4.305 µW	560.685 nW	581.05 nW	52.259 nW

CHAPTER 5
LEAKAGE REDUCTION TECHNIQUE IN UPCOUNTER

In this chapter, the impact of various leakage power reduction techniques as discussed in Chapter 2, has been studied and compared on 4-bit asynchronous up-counter circuit which consist four D-ffs. The inverters used in D-FF circuit have been implemented using different leakage power reduction techniques and then inserted in the D-FF design. The simulations are performed on LT spice tool at 32 nm technology node.

5.1 ONOFIC TECHNIQUE ON UPCOUNTER

In this work 4-bit asynchronous upcounter with ONOFIC technique has been implemented. Truth table for 4-bit asynchronous upcounter is given in table 5.1 below. Fig 5.1 shows the schematic of 4 bit asynchronous up counter with ONOFIC block. The ONOFIC block is incorporated towards the input and output side as well for maximum protection of the circuit from leakage power.

Here four DFFs have been used which consist of transmission gates and inverters. The inverters used in these DFFs are made using ONOFIC technique.
V_{DD} is 1.8V and the load capacitance at the output is 10fF. The clock signal having time period 10 ns is applied to the circuit.

Table 5.1 Truth Table for 4-bit down counter for ONOFIC

Counter State	Q3	Q2	Q1	Q0
0	0(L)	0(L)	0(L)	0(L)
1	0(L)	0(L)	0(L)	1(H)
2	0(L)	0(L)	1(H)	0(L)
3	0(L)	0(L)	1(H)	1(H)
4	0(L)	1(H)	0(L)	0(L)
5	0(L)	1(H)	0(L)	1(H)
6	0(L)	1(H)	1(H)	0(L)
7	0(L)	1(H)	1(H)	1(H)
8	1(H)	0(L)	0(L)	0(L)
9	1(H)	0(L)	0(L)	1(H)
10	1(H)	0(L)	1(H)	0(L)
11	1(H)	0(L)	1(H)	1(H)
12	1(H)	1(H)	0(L)	0(L)

13	1(H)	1(H)	0(L)	1(H)
14	1(H)	1(H)	1(H)	0(L)
15	1(H)	1(H)	1(H)	1(H)

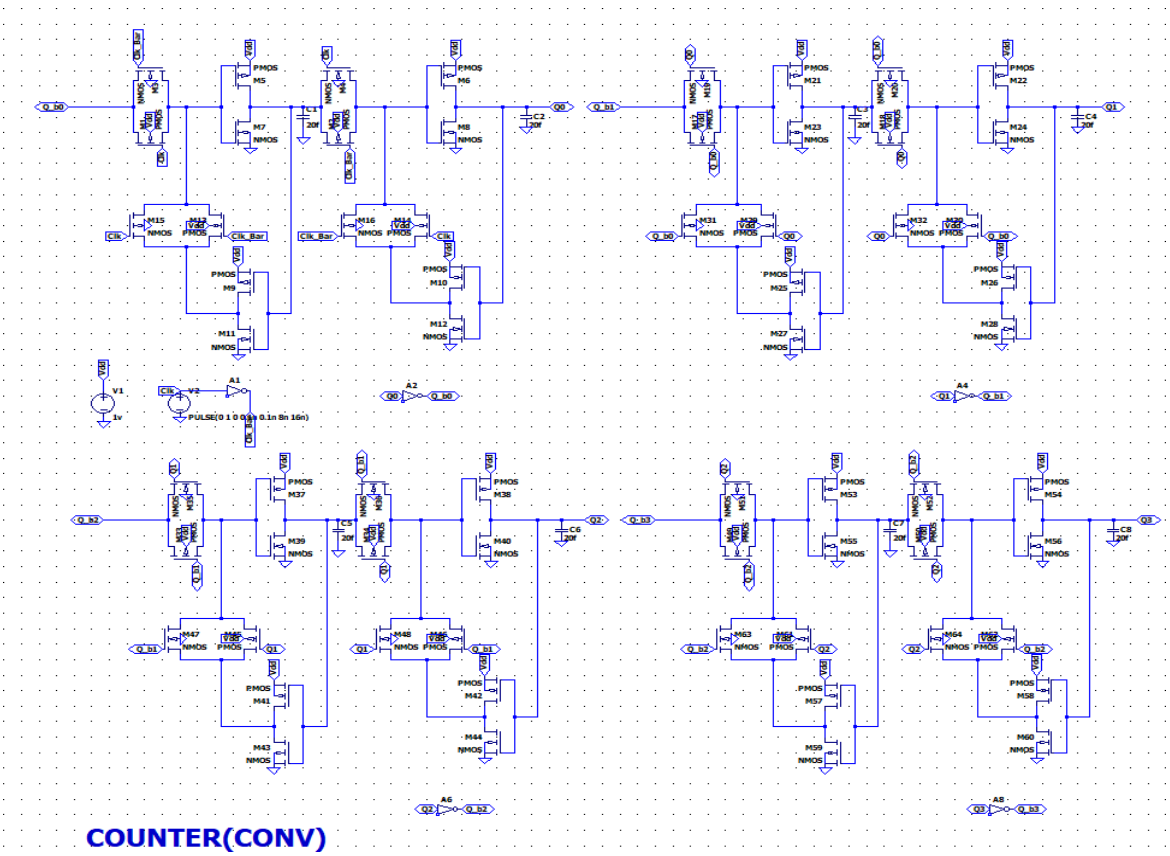

Fig 5.1 Up counter using ONOFIC technique

Fig 5.2 shows the output waveform where we can observe the sequence of Q3 Q2 Q1 Q0 as:

0000,0001,0010,0011,0100,0101,0110,0111,1000,1001,1010,1100,1101,1110,1111,0000,0001…….

The decimal equivalent of above sequence is :

0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,……which shows the functionality of upcounter has been verified.

In conventional 4-bit upcounter the power consumption is 7.103 µW, after applying ONOFIC technique the power consumption is 109.52 nW which shows that power consumption has been reduced.

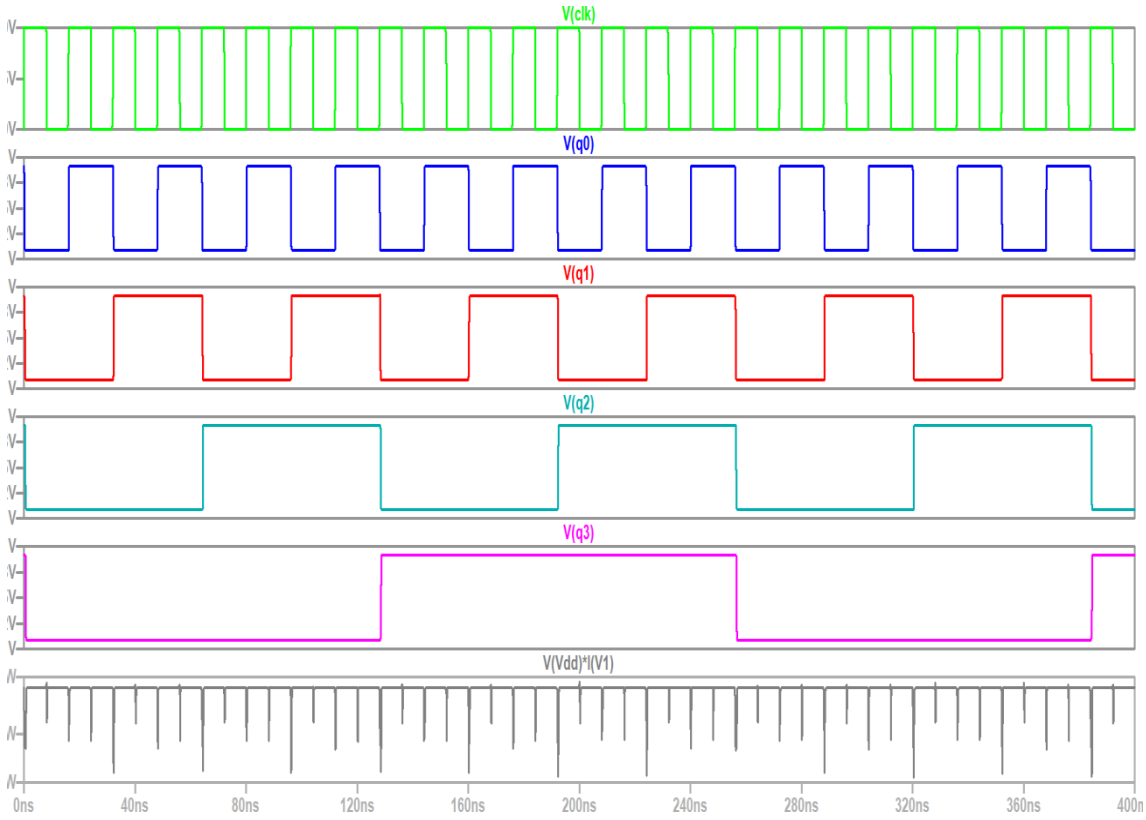

Fig 5.2 Output waveform of 4-bit Upcounter

5.2 STACK ONOFIC TECHNIQUE ON UPCOUNTER

In this work 4-bit asynchronous up counter with stack ONOFIC technique has been implemented.Truth table for 4-bit asynchronous up counter is given in table 5.2 below.

Table 5.2: Truth Table for 4-bit down counter for stack ONOFIC

Counter State	Q3	Q2	Q1	Q0
0	0(L)	0(L)	0(L)	0(L)
1	0(L)	0(L)	0(L)	1(H)
2	0(L)	0(L)	1(H)	0(L)
3	0(L)	0(L)	1(H)	1(H)
4	0(L)	1(H)	0(L)	0(L)
5	0(L)	1(H)	0(L)	1(H)
6	0(L)	1(H)	1(H)	0(L)
7	0(L)	1(H)	1(H)	1(H)
8	1(H)	0(L)	0(L)	0(L)
9	1(H)	0(L)	0(L)	1(H)
10	1(H)	0(L)	1(H)	0(L)
11	1(H)	0(L)	1(H)	1(H)

12	1(H)	1(H)	0(L)	0(L)
13	1(H)	1(H)	0(L)	1(H)
14	1(H)	1(H)	1(H)	0(L)
15	1(H)	1(H)	1(H)	1(H)

Fig 5.3 shows the schematic of 4 bit asynchronous up counter with stack ONOFIC block. The stack ONOFIC block is incorporated towards the input and output side as well for maximum protection of the circuit from leakage power.

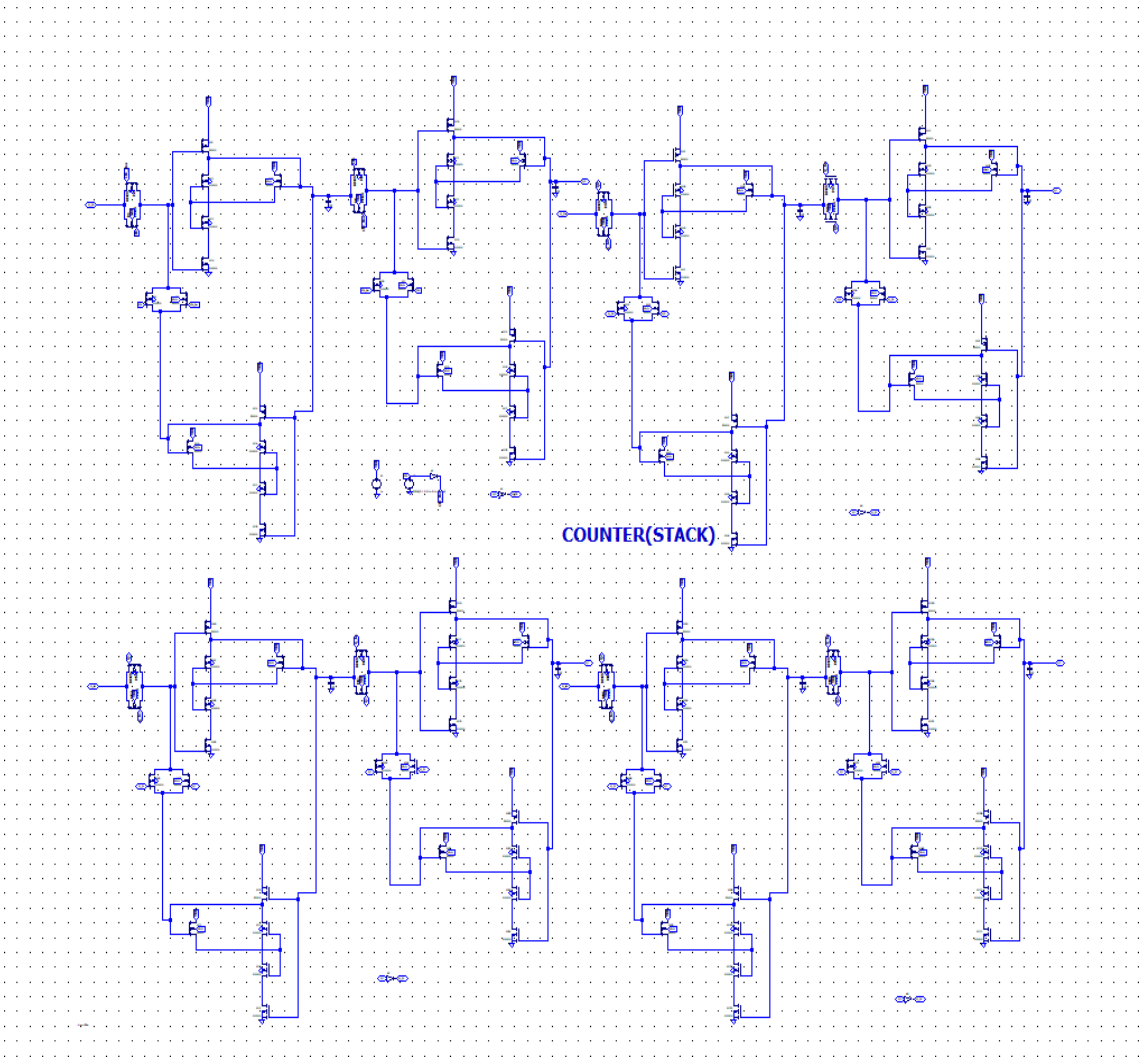

Fig 5.3 Counter using stack ONOFIC

Here four DFFs have been used which consist of transmission gates and inverters. The inverters used in these DFFs are made using Stack ONOFIC technique.

V_{DD} is 1.8V and the load capacitance at the output is 10fF. The clock signal having time period 10 ns is applied to the circuit.

Fig 5.4 shows the output waveform where we can observe the sequence of Q3 Q2 Q1 Q0

as:

0000,0001,0010,0011,0100,0101,0110,0111,1000,1001,1010,1100,1101,1110,1111,0000,0001…….

The decimal equivalent of above sequence is :

0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,……which shows the functionality of upcounter has been verified.

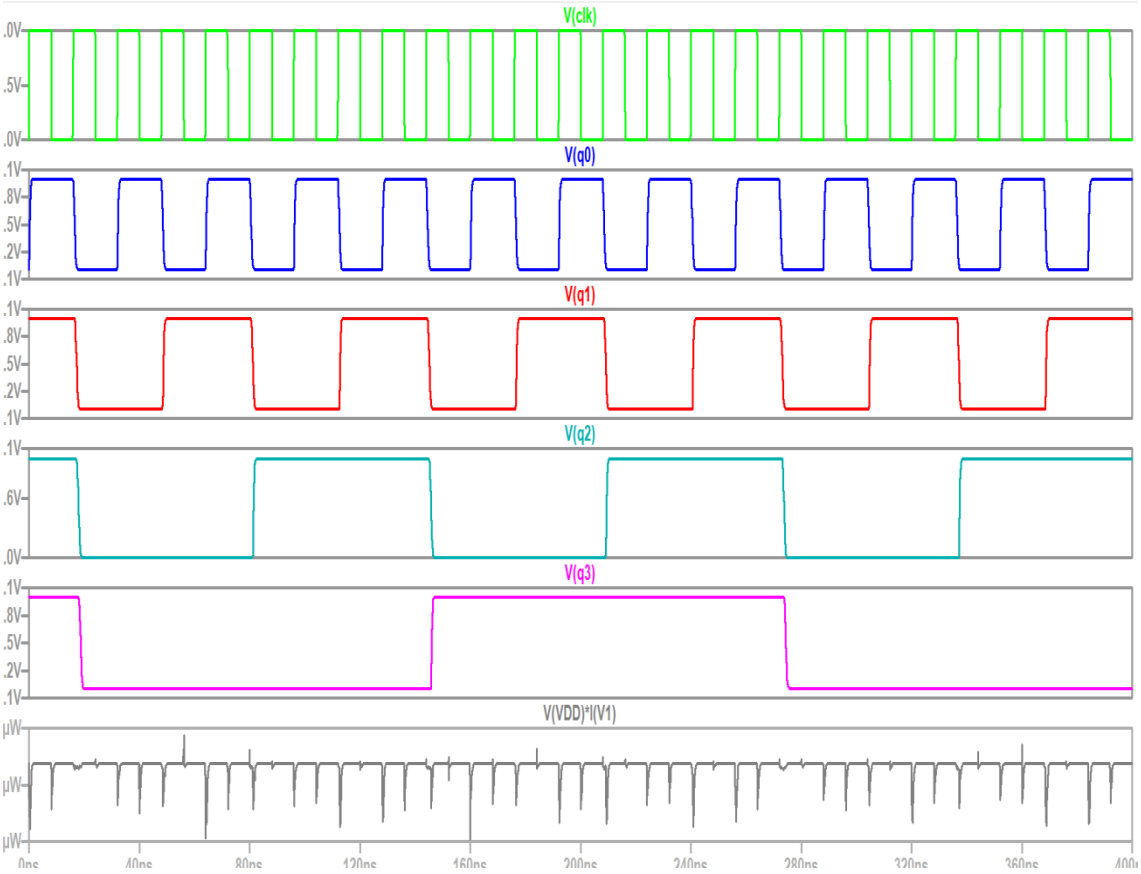

Figure 5.4: Output of 4-bit Upcounter

In conventional 4-bit up counter the power consumption is 7.103µW, after applying stack ONOFIC technique the power consumption is 117.16 nW which shows that power consumption has been reduced.

5.3 LECTOR TECHNIQUE ON UPCOUNTER

In this work 4-bit asynchronous up counter with LECTOR technique has been

implemented. Truth table for 4-bit asynchronous up counter is given in table 5.3 below.

Table 5.3 Truth Table for 4-bit down counter for Lector

Counter State	Q3	Q2	Q1	Q0
0	0(L)	0(L)	0(L)	0(L)
1	0(L)	0(L)	0(L)	1(H)
2	0(L)	0(L)	1(H)	0(L)
3	0(L)	0(L)	1(H)	1(H)
4	0(L)	1(H)	0(L)	0(L)
5	0(L)	1(H)	0(L)	1(H)
6	0(L)	1(H)	1(H)	0(L)
7	0(L)	1(H)	1(H)	1(H)
8	1(H)	0(L)	0(L)	0(L)
9	1(H)	0(L)	0(L)	1(H)
10	1(H)	0(L)	1(H)	0(L)
11	1(H)	0(L)	1(H)	1(H)
12	1(H)	1(H)	0(L)	0(L)
13	1(H)	1(H)	0(L)	1(H)
14	1(H)	1(H)	1(H)	0(L)
15	1(H)	1(H)	1(H)	1(H)

Fig 5.5 shows the schematic of 4 bit asynchronous up counter with LECTOR block. The LECTOR block is incorporated towards the input and output side as well for maximum protection of the circuit from leakage power.

Here four DFFs have been used which consist of transmission gates and inverters. The inverters used in these DFFs are made using LECTOR technique.

V_{DD} is 1.8V and the load capacitance at the output is 10fF. The clock signal having time period 10 ns is applied to the circuit.

Fig 5.6 shows the output waveform where we can observe the sequence of Q3 Q2 Q1 Q0 as:

0000,0001,0010,0011,0100,0101,0110,0111,1000,1001,1010,1100,1101,1110,1111,0000,0001…….

The decimal equivalent of above sequence is :

0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,……which shows the functionality of upcounter has been verified.

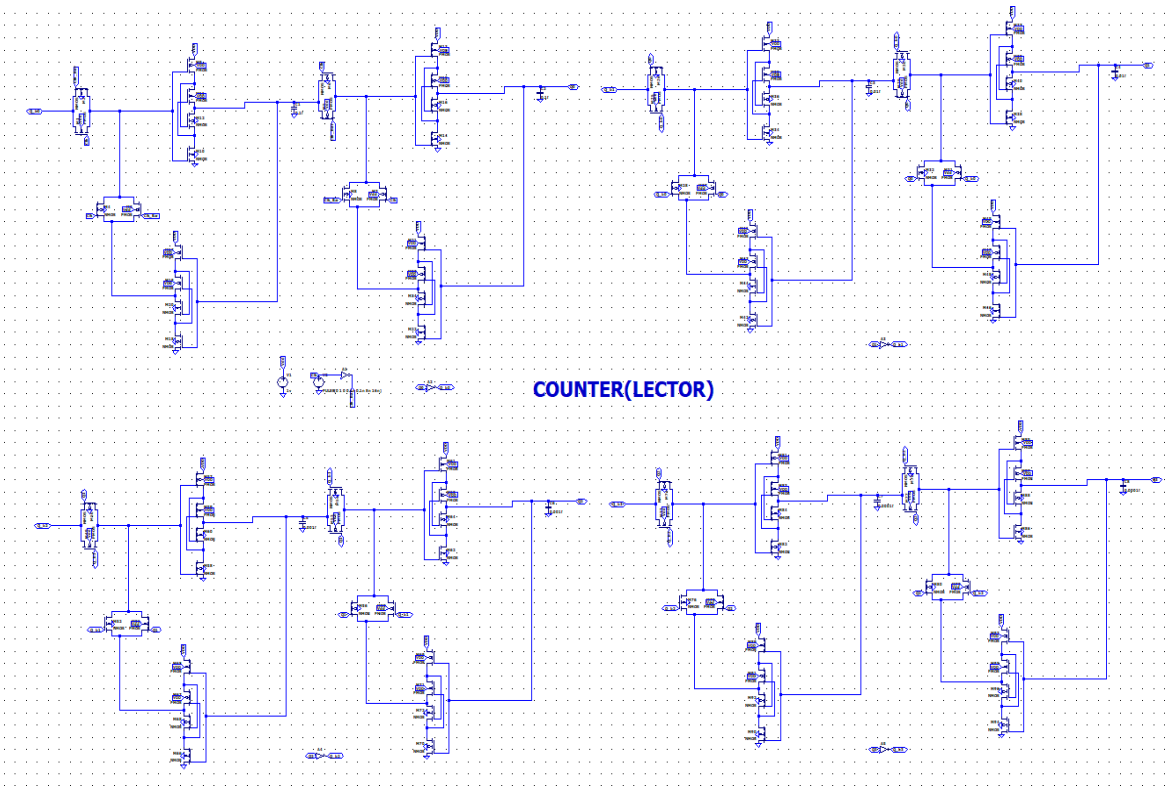

Fig 5.5 Counter using Lector

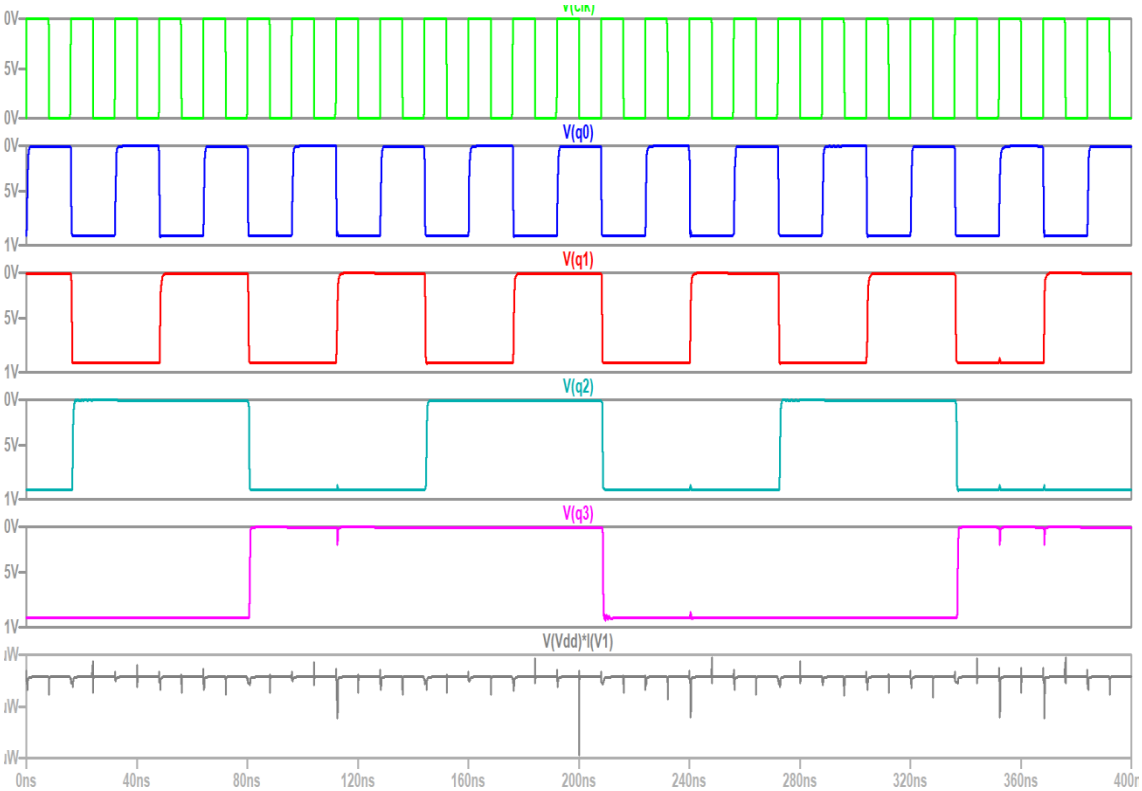

Fig 5.6 Output of 4-bit Upcounter using Lector

5.4 SUMMARY

In this chapter , I discussed the impact of various leakage power reduction techniques on 4-bit asynchronous upcounter.

The tabular comparison of power consumption for each clock combinations and after including each technique is shown below in table 5.4 :

Table 5.4 Power comparison among different upcounter circuits

CLK	Conventional	ONOFIC	Stack ONOFIC	LECTOR
0	7.956 µW	107.04 nW	114.69 nW	30.674 nW
1	6.249 µW	109.52 nW	117.16 nW	34.193 nW
Average→	7.103 µW	108.28 nW	173.27nW	32.43 nW

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

Power reduction in the circuit is an important task as over the years we focus on performance optimization which involves reduction of power consumed as well. Also in the battery operated devices, for battery lifespan lower power consumption in the circuit is of prime importance.When the technology node scales down, the leakage power increases so there is a need to study techniques for its reduction.

The average power for all possible input combinations of universal gates such as NAND and NOR after implementing various leakage power reduction techniques which are discussed in Chapter 2 have been studied.

The average power for all possible input combinations of 2 inputs NAND gate in conventional circuit is 1.606µW, after applying ONOFIC technique the average power is 239.672 nW, after applying Stack ONOFIC technique the average power is 1392.391 nW, for LECTOR based NAND the average power is 20.544 nW and for LCPMOS technique the average power is 220.609 nW.

It means using ONOFIC technique 85.08 %, using Stack ONOFIC technique 13.3 %, using LECTOR technique 98.73 % and using LCPMOS 86.26 % leakage power has been saved.

The average power for all possible input combinations of 2 inputs NOR gate in conventional circuit is 909.784 nW, after applying ONOFIC technique the average power is 239.67 nW , after applying Stack ONOFIC technique the average power is 267.6 nW , for LECTOR based NOR the average power is 17.73 nW and for LCPMOS technique the average power is 147.6 nW.

It means using ONOFIC technique 73.66 %, using Stack ONOFIC technique 70.59 %, using LECTOR technique 98.05 % and using LCPMOS 83.78 % , leakage power has been saved.

The average leakage power for all possible clock combinations of D-FF after implementing various leakage power reduction techniques which are discussed in Chapter 2 have been studied.

The average power for all possible clock combinations of D-FF in conventional circuit is 4.305 µW, after applying ONOFIC technique the average power is 560.685 nW, after

applying Stack ONOFIC technique the average power is 581.05 nW, for LECTOR based D-FF the average power is 52.259 nW .
It means using ONOFIC technique 86.98 %, using Stack ONOFIC technique 86.50 %, using LECTOR technique 98.78 % , leakage power has been saved.

The average leakage power for all possible clock combinations of 4-bit upcounters after implementing various leakage power reduction techniques which are discussed in Chapter 2 have been studied.

The average power for all possible clock combinations of 4-bit upcounter in conventional circuit is 7.103 µW, after applying ONOFIC technique the average power is 108.28 nW, after applying Stack ONOFIC technique the average power is 173.27 nW, for LECTOR based 4-bit upcounter the average power is 32.43 nW .
It means using ONOFIC technique 98.47 %, using Stack ONOFIC technique 97.56 %, using LECTOR technique 99.5 % , leakage power has been saved.

LCPMOS is more power efficient than ONOFIC and stack ONOFIC when we deal with small circuits. But for complex circuits LCPMOS doesn't produce correct logical behaviour of the circuits.
For small as well as complex static circuits LECTOR technique is best. But LECTOR technique requires more chip area than ONOFIC and LCPMOS.
For sequential circuits like D-FF and up counter also LECTOR technique gives best result.

6.1 FUTURE SCOPE

As a future scope, these leakage reduction techniques could be added to combinational circuits like full adders, multiplexers, demultiplexers, decoders, parity checker. This leakage power reduction technique can also be used in different sequential circuits like flip flops, latches, counters, registers etc., circuits like these form an integral part of many design concept and hence incorporating these leakage techniques proves to be very useful in saving the leakage power at lower technology nodes.

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