A COMPARATIVE ANALYSIS AND DESIGN OF DYNAMIC LATCHED COMPARATORS

A PROJECT REPORT

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IN
VLSI DESIGN AND EMBEDDED SYSTEM

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CANDIDATE'S DECLARATION

I, Mahima Singh Yadav Roll No. 2K21/VLS/25, of M.Tech. VLSI Design and Embedded System, hereby declare that the project Dissertation titled "A comparative analysis and design of dynamic latched comparators" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, is original and not copied from any source without proper citation. This work has never been the foundation for the awarding of a Degree, Diploma, Associateship, Fellowship, or other similar title or recognition.

Place: Delhi

Date: 31/05/2023 **MAHIMA SINGH YADAV**

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CERTIFICATE

I hereby certify that the Project Dissertation titled "A comparative analysis and design of Dynamic Latched Comparators" submitted by Mahima Singh Yadav, Roll No. 2K21/VLS/25 of Department of electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any degree or diploma to this University or elsewhere.

Place: Delhi
Date: 31/05/2023

DR. RAJESH BIROK
SUPERVISOR

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MAHIMA SINGH YADAV

ABSTRACT

In an attempt to study various comparators, a comparative analysis of different dynamic latch comparators have been performed. The performance of the conventional dynamic latch comparator, Double tail dynamic latch comparator, charge sharing dynamic comparator and modified double tail dynamic latch comparator have been done to display the improvements achieved. Further a new circuit has been proposed displaying the same functionality.

Transient analysis has been observed for each circuit. Effect of delay on circuit's robustness in form of Monte Carlo Simulations has been performed. As the need for low power, high speed comparator's is of utmost importance day by day, the circuits present a vivid picture of their performance.

All the simulations are carried out using Cadence Virtuoso tool with a supply voltage of 1.5V, differential input voltage of 20mv and common mode voltage of 1.2V in 130 nm CMOS technology node at a temperature of 27-degree Celsius.

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List of Symbols, Abbreviations

NMOS: N Channel Metal Oxide Semiconductor

PMOS; P Channel Metal Oxide Semiconductor

CMOS: Complementary Metal Oxide Semiconductor

STDLC: Single Tail Dynamic Latched Comparator

DTDLC: Double Tail Dynamic Latched Comparator

MDTDLC: Modified Double Tail Dynamic Latched Comparator

SCDLC: Shared Charge Dynamic Latched Comparator

PDLC: Proposed Dynamic Latched Comparator

PDP: Power Delay Product

ADC: Analog to digital Converter

IC: Integrated Circuit

CHAPTER 1

INTRODUCTION

1.1 Overview

The need for portable battery-operated gadgets is rising in the modern age, and low voltage methods for high-speed purposes are taking a significant hit. Typical portable electronics devices, such as wireless communication systems, cell-operated healthcare gadgets, etc., are being developed with the rapid rise of semiconductor technology. One of the most crucial elements in any of these applications is battery life. Low power, low voltages are therefore extremely necessary. By adopting a wider oxide film or greater supply levels, IC costs can be decreased as well. Low voltage & low power comparator are often highly critical and necessary in integrated circuits where ADC or DAC plays a vital role. The goal application's execution, which depends on the construction modelling and kind of it, is significantly impacted by the comparator. The resolution and efficiency of the Analog to digital converter are directly impacted by the comparison device's input signal band; associated input offset value, and latency. As we focus on the process variances, lower feature size techniques, the device's efficiency level will be substantially impacted. Comparators are categorised into many types depending on their behaviour, usefulness, such as continuous or discrete time comparators, voltage based or current-based comparators. Detection of signals are other uses of comparators..

1.2 Basics of CMOS Comparator

After op - amps, comparators are arguably the most commonly employed electrical circuits globally. Comparators are often employed in high quantities in analogue to digital converters since they are known as 1-bit ADC. To begin the A/D transition, the input must initially be sampled. The digital version of the analogue input is then calculated using the sampled signal and a set of comparators. The comparator's judgement reaction time governs how quickly it can convert data. In addition, comparators are used for a variety of different purposes, including as data transmission, zero-crossing sensors, peak

detection systems, switching voltage controllers. A CMOS comparator's fundamental capabilities include determining if a signal is larger or lesser than 0 as well as comparing an input signal to a given signal and producing binary output as a consequence of the comparison. Figure 1.1 depicts the representation schematically and the fundamental functioning of a voltage comparator, which may be viewed as a circuitry for making decisions..

1.2.1 Definition

A circuitry that generates a binary output depending on comparison of an analog signal with an other analog signal or else reference voltage is known as comparator.

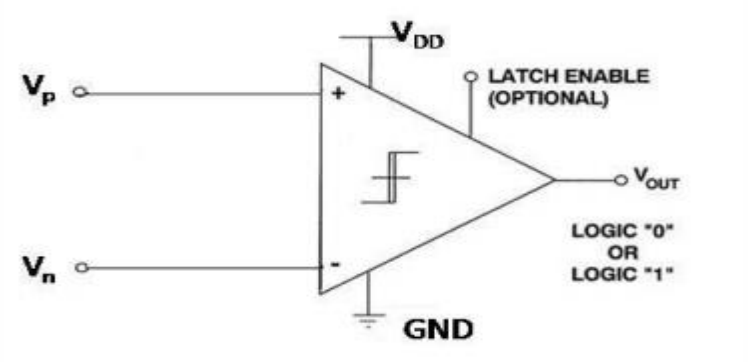


Fig. 1.1: Comparator Schematic [14]

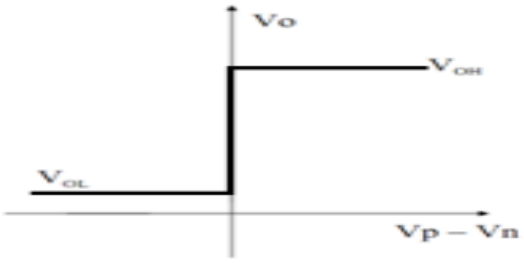


Fig 1.2: Ideal voltage transfer characteristic of comparator [14]

The design representation for the comparator is shown in Figure 1.1, and its ideal transfer properties are shown in Figure 1.2. Vn is reference voltage (fixed Voltage level) supplied to the comparator's negative end, and the input signal (pulse voltage) sent to the comparator's positive input end is denoted by Vp. So, when Vp, the comparator's input, is at a voltage

higher than Vn, the reference value, the comparator's result is a logic high, but if Vp is at a voltage lower than that of Vn, the comparator's result is a logic low.

In case : $V_n < V_p$, V_o= logic high.

In case : $V_n > V_p$, V_o= logic low.

1.3 TOOLS USED

Tools used for carrying out the project are Cadence Virtuoso . Cadence Virtuoso is used for constructing the schematics and simulating them to observe their characteristics.

1.4 ORGANIZATION OF WORK

The description of how the work was structured during the project's accomplishment has been demonstrated:

In this report, a dynamic comparator is compared, and the results indicate decreased power usage and delay.

The review of literature and list of different comparators are presented in **Chapter 2**. The comparator’s characteristics and features are described in **Chapter 3**. In **Chapter 4**, the comparators are analysed, and their functionality is explained. The simulation based observations of the transients, and result deduced are presented pictographically in **Chapter 5**. The related conclusion and future plan for the project are covered in **Chapter 6** .

CHAPTER 2

LITERATURE SURVEY

2.1 LITERATURE REVIEW

Researchers have developed an analog comparator over the past few decades utilising some great ideas. Jeon and Kim have helped with the creation of a dynamic latch comparator [3]. It can decrease hysteresis response, power usage, and latch offset value & delay.

[A] Conventional Dynamic Latch comparator:

Figure 2.1 shows the traditional dynamic comparator [7]. It was originally brought out by Kobayashi, Nogami, and others. The dynamic latch comparator recreates the input value into a full fledged digital level output signal via a positive feedback technique [1]. Since it is a clock regeneration comparator, high-speed ADC frequently uses this.

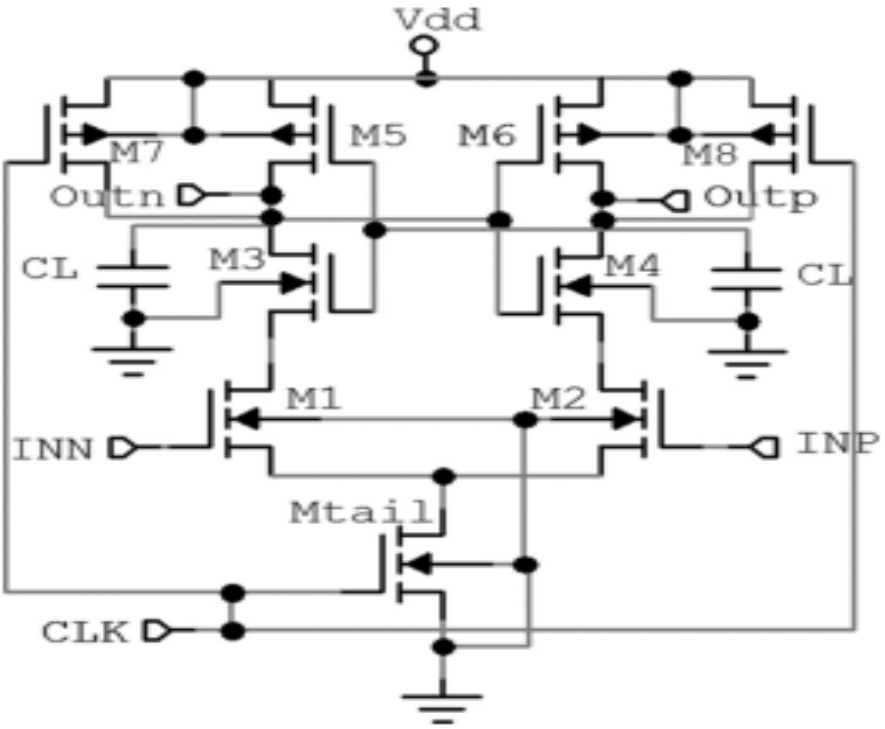


Fig. 2.1: STDLC [1]

[B] Double Tail-Dynamic latched Comparator:

The researchers who looked at this circuit were Schinkel, Mensink, Klumperink, et al. [6] Compared to a traditional dynamic comparator, this one requires less mounting and can operate at a low voltage supply. This circuit has two tail transistors: Mtail1 is short and enables a low current in input side for low offset, while Mtail2 is broad and provides considerable current during the latching phase, leading to quick latching (Fig. 2.2).

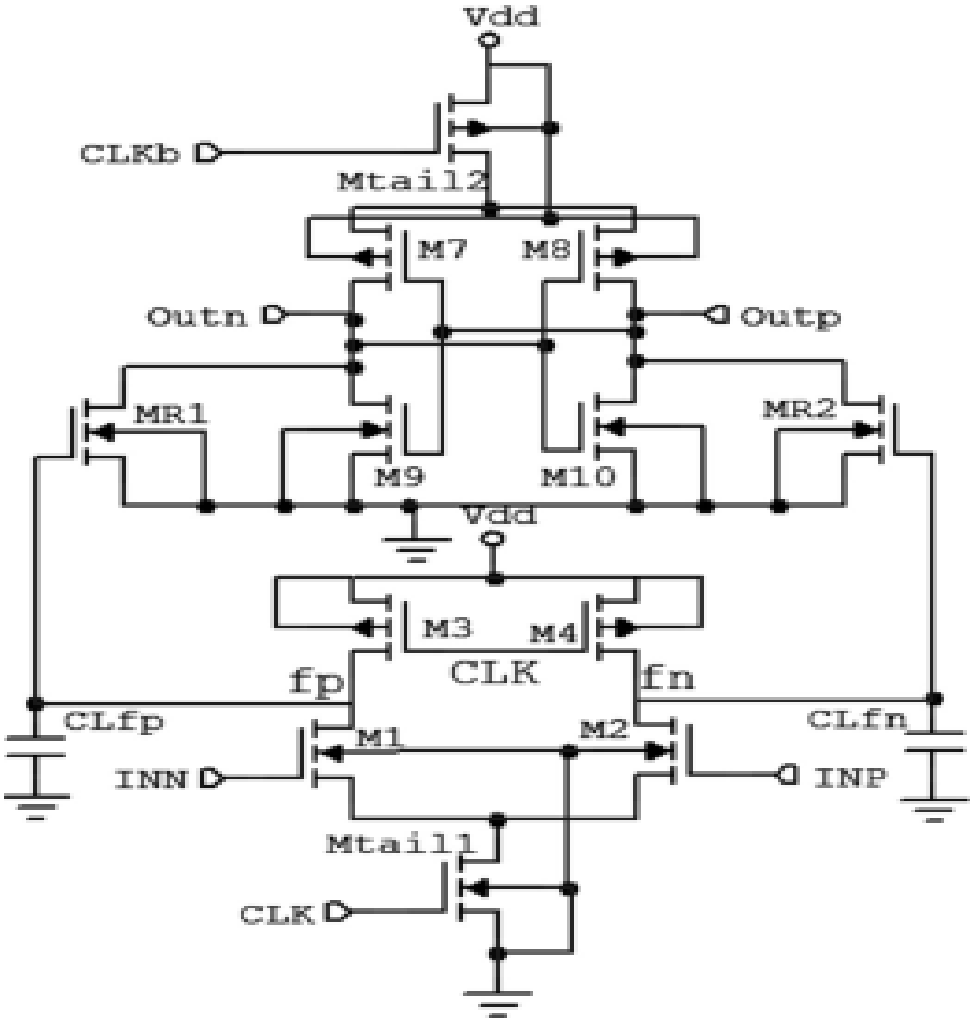


Fig. 2.2: DTDLC [1]

[C] Modified Double Tail Dynamic Latched Comparator

It has been observed that the disparity in terminal voltage at fn and fp has an influence on the rate of latch regeneration in traditional double tail comparator. The efficacy of the comparator will rise if the variation in voltage magnitude at the terminal is greater. To accomplish it, two control transistors were cross-coupled in parallel to M3 , M4 as illustrated in Fig 2.3. Mashhadi et al. [9] developed and researched the architecture of modified double tail.

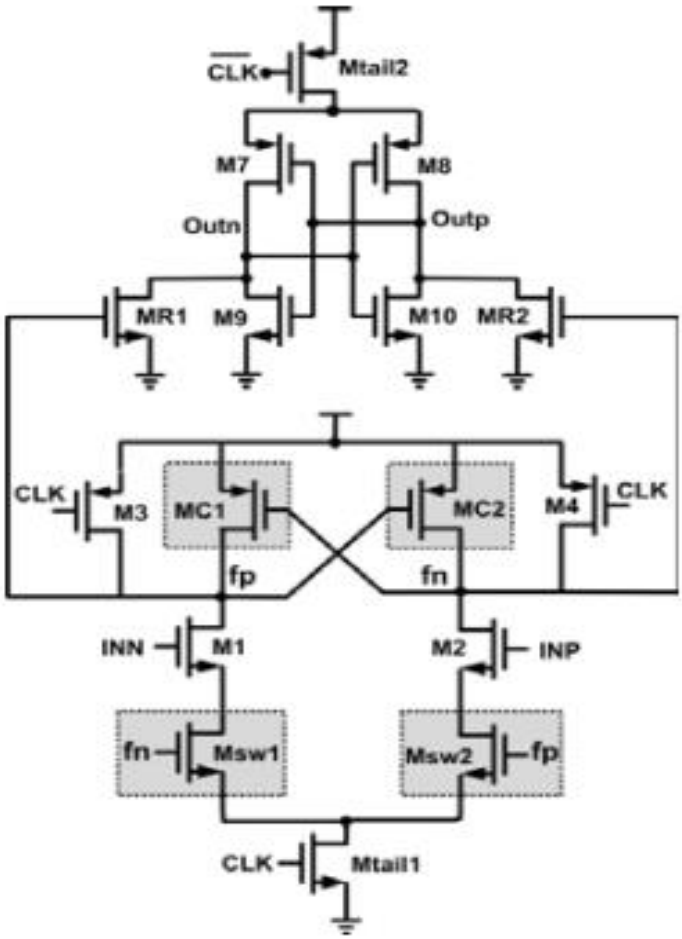


Fig. 2.3: MDTDLC [9]

[D] Shared charge Logic Dynamic Latch Comparator:

Savani and Devashrayee et al.[1] presented the dynamic latch comparator to enhance the performance index of conventional comparator based on the examination of STDLC and DTDLC and the addition of the basic notion of shared charge logic. Simulation using 130 nm CMOS technology was done, and the outcomes showed characteristics like latency, power, and PDP had been reduced. Fig. 2.4 contains a representation of the architecture under discussion.

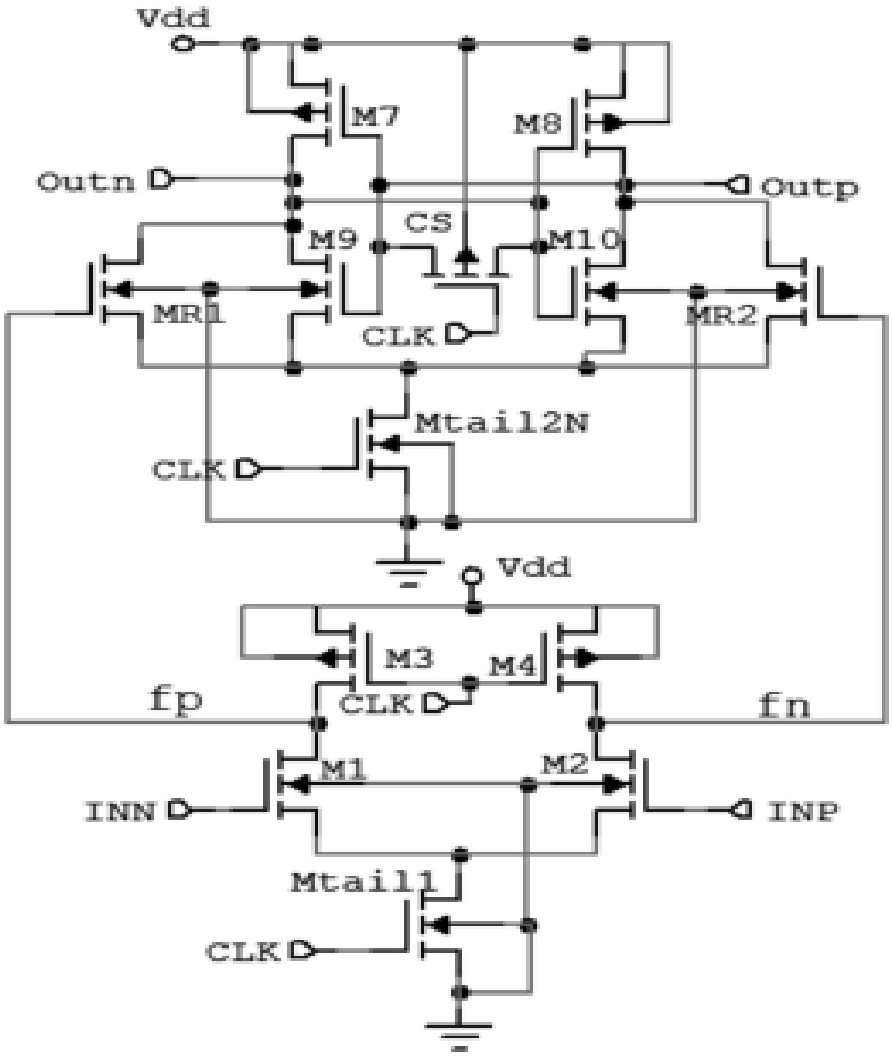


Fig. 2.4: SCDLC [1]

CHAPTER 3
COMPARATOR CHARACTERISTICS

Both the static as well as dynamic features of the comparator will be looked upon in this section.

The optimal attributes of the comparator are depicted in Figure 3.1.

3.1 Static Characteristics:

Gain, output high (VOH) and low states (VOL), , Offset ,Input Resolution, Noise make up static characteristics.

3.1.1 Gain:

The gain of comparator is expressed as follows:

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}\text{-}V_{OL}}{\Delta V} \text{ where } \Delta V \text{ is the input voltage change}$$

First-Order Model for a Comparator:

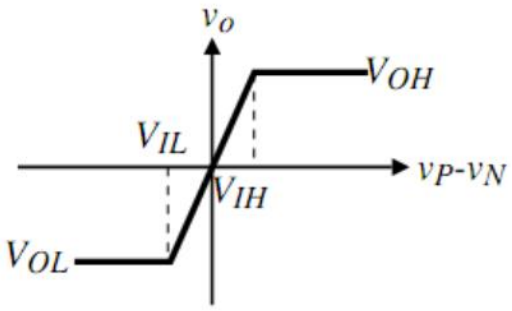


Figure 3.1 First-Order Model of Comparator [14]

VIH= Value of the smallest possible input voltage for which the output voltage is VOH

VIL= Value of the largest possible input voltage for which the output voltage is VOL.

$$\text{The voltage gain is } A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

3.1.2 Resolution: In order to make the output fluctuate to acceptable binary levels, the input voltage must shift. That change in input voltage is termed as resolution.

3.1.3 Offset: It can be categorised in two ways visually (i) systematic offset and (ii) random offset. Misaligned input transistors (misconfigured threshold levels and mismatched transconductance parameter β=μCox W/L) cause offset in operational amplifiers and comparators.

a) Input Offset Current: The variation amongst the various currents reaching the input ends of a balanced amplifier is termed input offset current.

b) **Input Offset Voltage**: The potential that has to be supplied between the input ports in order to balance the amplifier is referred as the input offset voltage.

c) Output Offset Voltage: When the two input ends are connected to ground, the output offset potential is the dc voltage that is produced at the output node.

3.1.4 Noise: A comparator's noise is analyzed as if it was bias in the transition area. Jitter is brought on by an ambiguity in the transition area brought on by noise.

3.1.5 Input Common Mode Range (ICMR): It could be described as the input voltage range when the comparator operates correctly and satisfies all necessary requirements.

3.2 Dynamic Characteristics:

Gain and Propagation delay make up the comparator's dynamic properties.

3.2.1 Propagation delay:

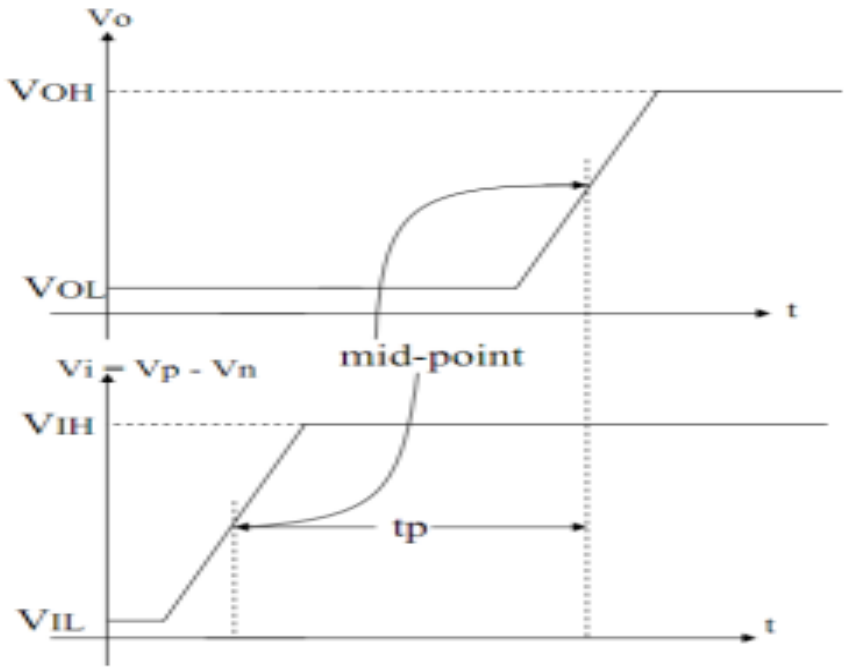


Figure 3.2: Comparators Propagation delay

How quickly an amplifier reacts to given input is referred to as the propagation delay. Propagation delay, expressed simply, is the interval between an input and an output.

The propagation time delay characteristics of the comparator are shown in Fig. 3.2. It is estimated as follows:

Propagation time delay= (Rising Propagation Delay + Falling Propagation Delay) /2

3.2.2 Slew Rate: Slew rate is the rate at which the voltage at output node changes in relation to time.

$$SR= dVout/dt$$

The dynamics might be constrained by the slew rate if the speed of rising or falling off a comparator increases significantly. The Slew rate can be stated with following result:,

$$I=C\ dV/dt$$

wherein I is the capacitor's current ,V is the voltage applied across it. The voltages speed also gets constrained if the current does. Consequently, we have the following for a comparator with a slew rate limit:

$$t_p = \Delta T = \Delta V/SR = (VOH - VOL)/ 2*(SR)$$

wherein SR= comparator’s slew rate.

CHAPTER 4

METHODOLOGY AND IMPLEMENTATION

4.1 Architecture of Conventional single tail current dynamic latch comparator:

Figure 4.1 depicts the schematic structure of a typical dynamic latch comparator with a single tail current. It has large input impedance, rail-to-rail output fluctuation, and no static power usage. The reset phase as well as regeneration phase are the two distinct parts of the comparator's functioning. CLK is low and M9 transistor is off during the reset phase. The reset transistors (M4, M8) are switched ON during this stage, pulling both the Outn and Outp output terminals to Vdd. This criterion is the prerequisite for the evaluation step. During the reset phase, the M4, M8 transistors are employed to achieve a correct logical level at the output node.

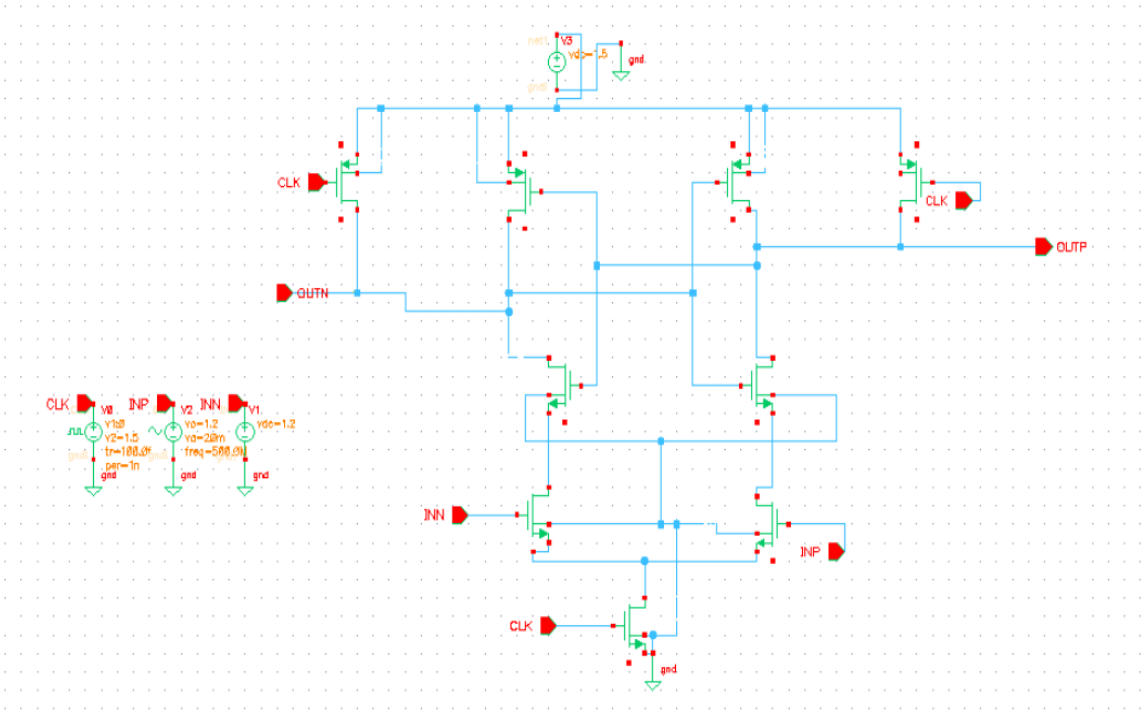


Fig. 4.1: Schematic of STDLC

Transistor M9 is switched ON while transistors M4 , M8 are turned off when CLK changes to Vdd, and the circuit enters the comparison phase. The output nodes Outp and Outn, which were precharged to VDD in the preceding reset phase, begin dropping at separate paces. The corresponding/relative input voltage values, or INN and INP, determines the rate of discharge. Presuming that VINP is more than VINN , the Outp terminal would drop more quickly than Outn. Within that scenario, the Outp terminal (which is emptied by the transistor M5's drain current) reaches Vdd - |Vthp| prior to the Outn terminal reaching this potential. Transistor M6 in this example, switches ON to start the regeneration process brought on by cross-coupled inverter. Outp entirely drops to ground after being fully charged Outn to Vdd.

4.2 Architecture of Double Tail dynamic latch comparator (DTDLC):

The design structure of a traditional dynamic latch comparator based on dual tail current is shown in Figure 4.2 [1]. The comparator has 2 distinct tail currents as well as fewer stacked transistors as compared to a comparator with single tail current. Lower tail current in differential phase for smaller offset and higher tail current during latch phase for rapid latching are both separately enhanced by double tail. The comparator operates as follows. Phase of reset: When CLK = 0, transistors M1 and M10 are switched OFF, and transistors M12 and M11 begin precharging two intermediate nodes, fn and fp, to produce voltage Vdd, this is known as the precharging phase. Eventually, intermediate transistors MR5 and MR7 cause output nodes Outn and Outp to discharge to the ground.

Phase of evaluation: When CLK changes to Vdd, transistors M1 , M10 switches on, transistors M11 ,M12 are switches OFF, and voltage at nodes fp and fn begin to drop at a speed determined by the tail current and equivalent capacitive load at node fn (fp). This creates differential potential values among fn and fp . Transistors at the intermediate phase transmit the voltage to inverter that are cross-coupled, while at same moment, transistors M5 , MR7 offer safeguard by lowering kickback noise.

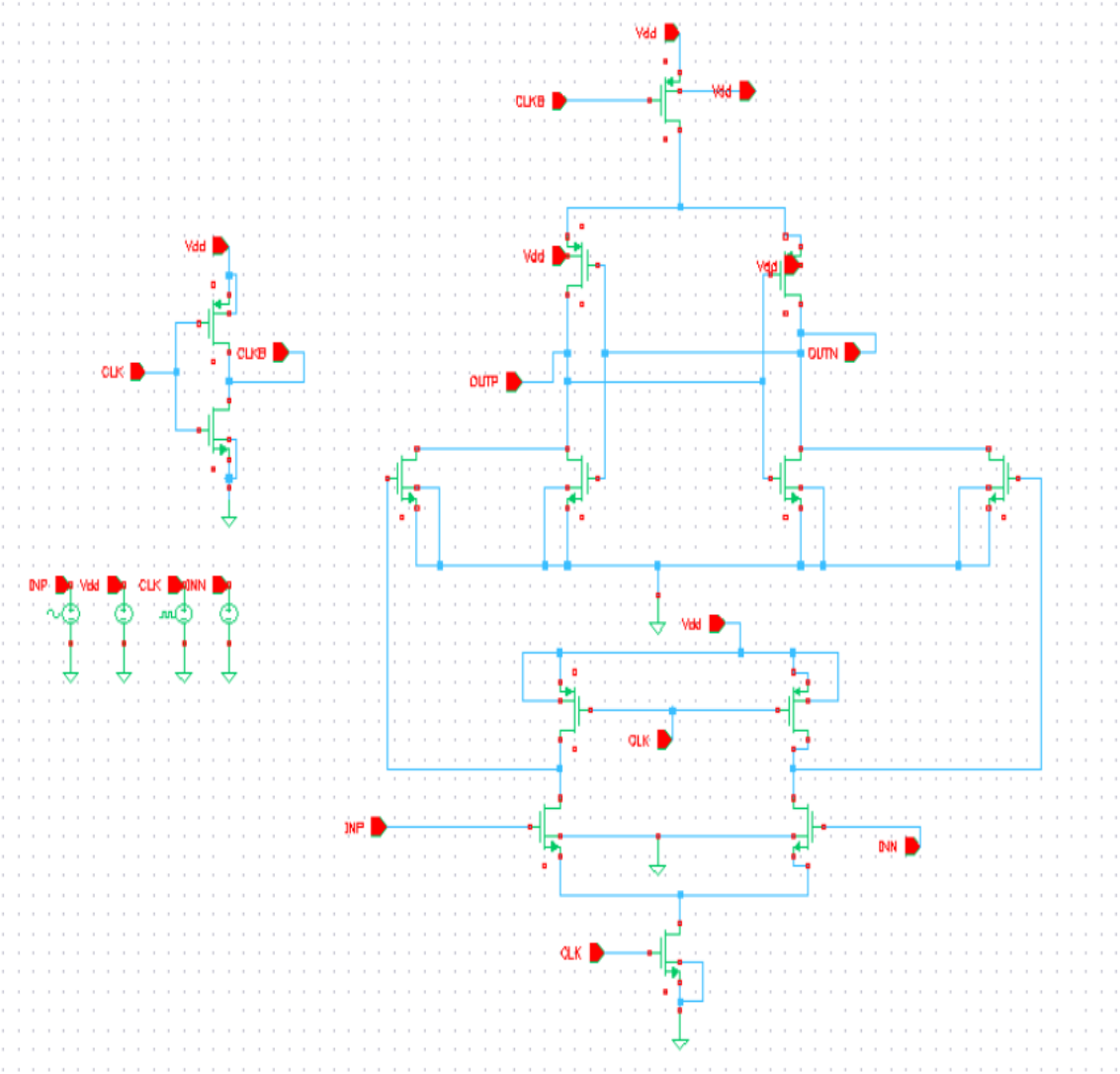


Fig. 4.2: Schematic of DTDLC

4.3 Architecture of Modified Double tail dynamic latched comparator:

The design for the modified double-tail dynamic latch comparator is shown in Fig. 4.3. The improved comparator is constructed using double-tail architecture due to the structure's superior functioning in low-power usage. The comparator's primary goal is to raise Vfn/fp in order to accelerate regeneration of latch. To accomplish this, two control transistor (M11 , M12) are cross-coupled in parallel with M15 and M16 in the first stage.

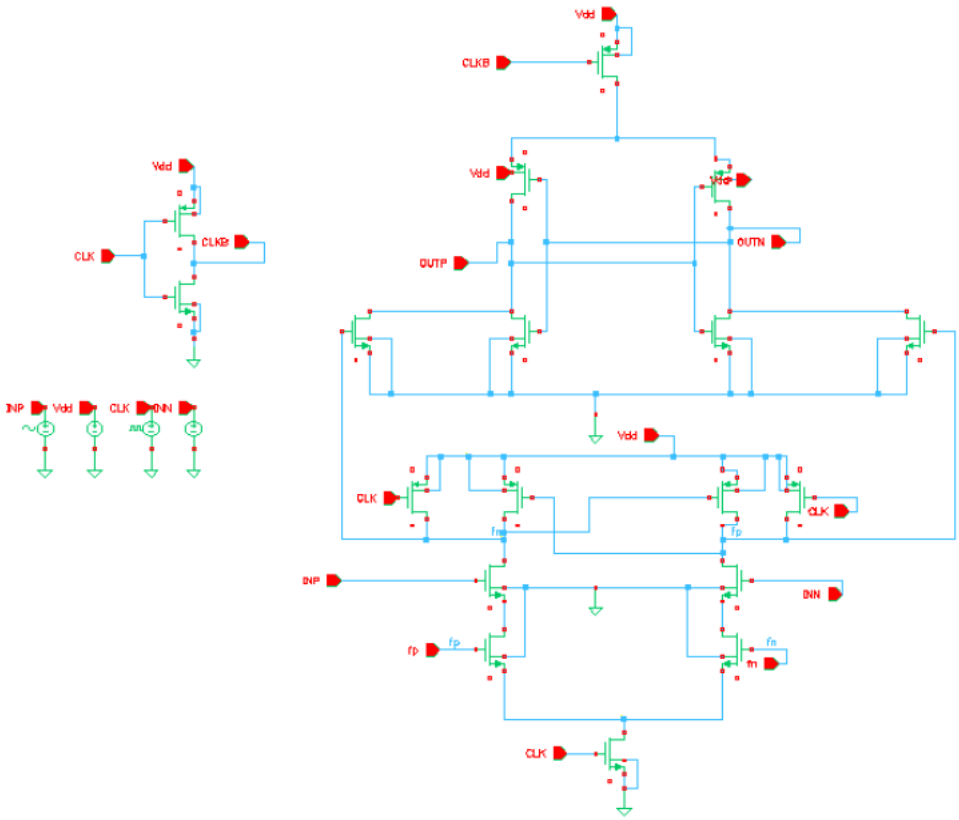


Fig. 4.3: Schematic of MDTDLC

The comparator works in the manner described ahead. M15 and M16 pull both the fn, fp nodes to supply voltage in the reset phase (CLK = 0, M1, Mtail10 are off to prevent static power), which turns off M11 and M12. Both of the latch output signals are reset to zero by intermediary stage transistors M5 and M7. The comparator operates as : M15 and M16 pull the fn , fp nodes to supply voltage in the reset stage (CLK = 0, M10 , M1 are off to prevent static power), which turns off M11 and M12. Both of the latch outputs are reset upto zero by intermediary stage transistor M5 and M7.

M15, M16 are turned off in the decision-making stage (CLK = VDD, M1, M10 are on). Moreover, the controlling transistor remain still off at the start of the stage. Based on voltage levels at input, fn, fp begin to decline at varying speeds. If Vinp > Vinn, then fn would decline faster than fp (as M17 provides larger current as that of M18). The associated PMOS transistor M11 begins to switch on as longer as fn keeps dropping,

bringing the fp node up to supply voltage. As a result, M12 is off, enabling fn to drop entirely.

In this structure, shortly after comparator senses, for example, that node fn drops quickly, transistor (M11) turns on, pulling the terminal fp to supply voltage, in contrast to standard dual dynamic comparator, in which Vfn/fp is function of gm of input transistor and voltage level difference at input. As a result, as time progresses, the gap among fn, fp rises exponentially, which reduces regeneration period of latch. The thing to keep in mind is when one of the control transistor (like M11) goes active, current from power supply is pulled to the ground through the input and tail transistor (such M11, M18, and M10), which causes static power usage. Two nMOS transistors M17 and M18 are employed underneath the input transistors to solve this problem. The two transistors are on at the start of the decisive stage and fn , fp start to drop at varying rates since both nodes are pre-charged to supply voltage. Control transistors will respond in a way to enhance their potential gap the moment comparator senses that any of the fn or fp node is draining more quickly.If fp were to be lifting up to supply voltage and fn needed to be fully discharged, the switch in fp's charging route would be open , while the switch attached to fn would be closed to facilitate for the full dropping of the fn terminal. Stating in different terms, M17, M18 and control transistor operate in a manner that mimics the action of latch.

4.4 Architecture of Shared charge double tail comparator:

The schematic of architecture of shared charge DLC is depicted in fig. 4.4. Distinct kinds of reset mechanisms are employed during the reset stage of all dynamic latched comparators to produce a logically valid value during the evaluation stage. In this reset method, output nodes are either drained to ground or pulled up to VDD. While in Dual Tail DLC, the output terminals are drained to GND, in Single tail DLC, they are charged to supply voltage. One output node of the comparator is at zero voltage and the other is at VDD once the evaluation step is finished. In the reset phase of the designs that were covered earlier, output ends are either fully drained to GND or charged upto supply voltage. The next evaluation stage begins from the zero voltage or the supply voltage, demanding a prolonged time to obtain the evaluation's ultimate result and utilizing more energy. Discharging one node or charging another node also uses more energy during the subsequent reset stage.

The comparator's main concept is to hold the charge using the improved reset mechanism, which reduces latency & energy. The name of this methodology is shared charge logic. A pass transistor is utilised in this method amongst 2 output nodes.

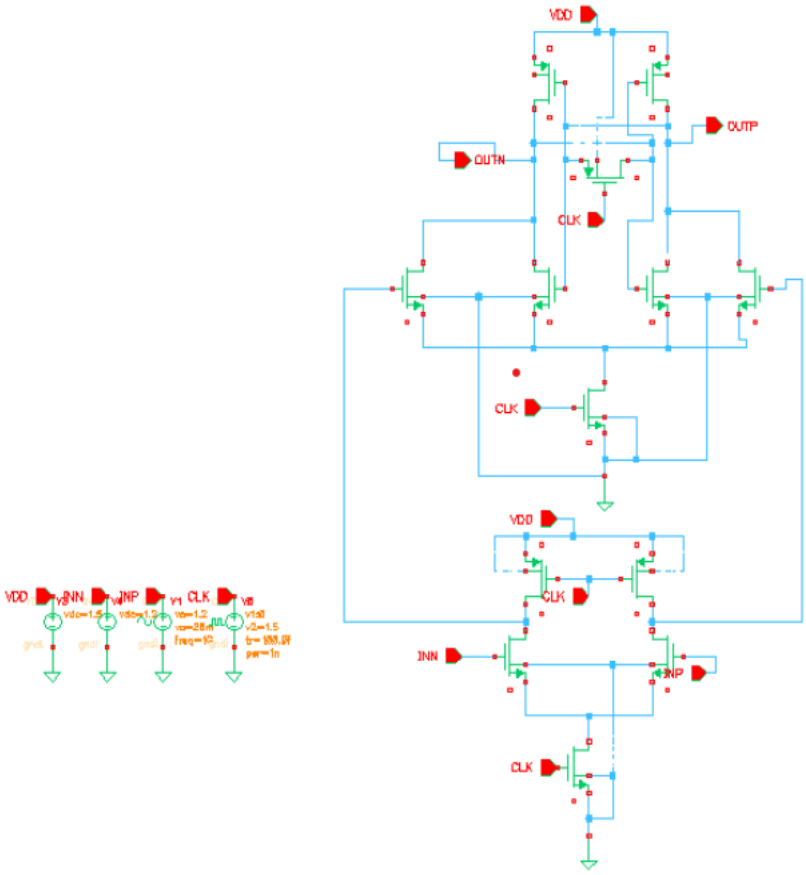


Fig. 4.4: Schematic of SCDLC

During the reset stage, the pass transistor distributes the charge among its two nodes. The input signal may be assessed more quickly during the regeneration stage since the output won't drop below the threshold value level due to the charges distributed by both load capacitances. It accelerates the process. The results of the execution demonstrate a substantial reduction in delay and power saving as a result of this method. Transistors M11, M3 are turned OFF to prevent any consumption of static power once CLK is at zero

voltage. Transistors M10, M8 bring the nodes fn , fp to VDD during this stage.Therefore, resultantly it switches ON transistors M1 and MR4.

In this reset stage, transistor M5 connects the two output nodes Outn and Outp, converting it into a shared charge transistor that distributes the charge between Outn, Outp.

The circuit starts to evaluate when the CLK gets close to VDD. Transistors M11 and M3 are switched ON during this stage, whereas reset transistors M8, M10 are switched OFF. Now, in accordance with the speed determined by input voltages, the fn and fp terminals begin draining via the transistors M13 and M12 at varying rates.

Assuming VINN is greater than VINP, fp decreases more quickly than fn. If we consider the input voltage to be in the opposite state, this event would be different. The main functional difference between this design and others is that in the evaluation stage, decisions are made when both output nodes are almost at 50% the VDD value rather than at two extreme voltage values. Even though the output node's starting status is at 1/2 the voltage supply level, it requires less time to evaluate and uses less power.

4.5 Proposed Dynamic Latched Comparator:

This comparator, like other comparators, operates in two distinct stages. During the reset phase, CLK = 0 and CLK = VDD, therefore both tail transistors are turned off, and the drain and source terminals of F3 and F4 are charged to VDD through F5,F7, and F6,F8. If OUTP and OUTN have any accumulated charge from earlier cycles, they are discharged to ground through F13 and F14. Clock cycles are now reversed during the assessment phase, and tail transistors are turned on. The conductances of paths F1 and F2 are affected by the voltages VINP and VINN. Fa will switch off F4 and turn on F10, causing node Fb to be at VDD, which will turn off F9 and turn on F3 to allow the Fa node to be totally drained. As long as node Fb is turned on, OUTP will discharge to ground through F14.OUTP will also switch on F11 and turn off F15, keeping OUTN at VDD. OUTN will cause F12 to switch off, so disconnecting the charging channel of OUTP, and will turn on F16 to assist OUTP in being entirely drained.

To ensure the specified precision of comparison, two distinct clocks are required, with correct synchronization between them. During the reset phase, the top level transistor prevents any power use. The figure is shown in Fig 4.5.

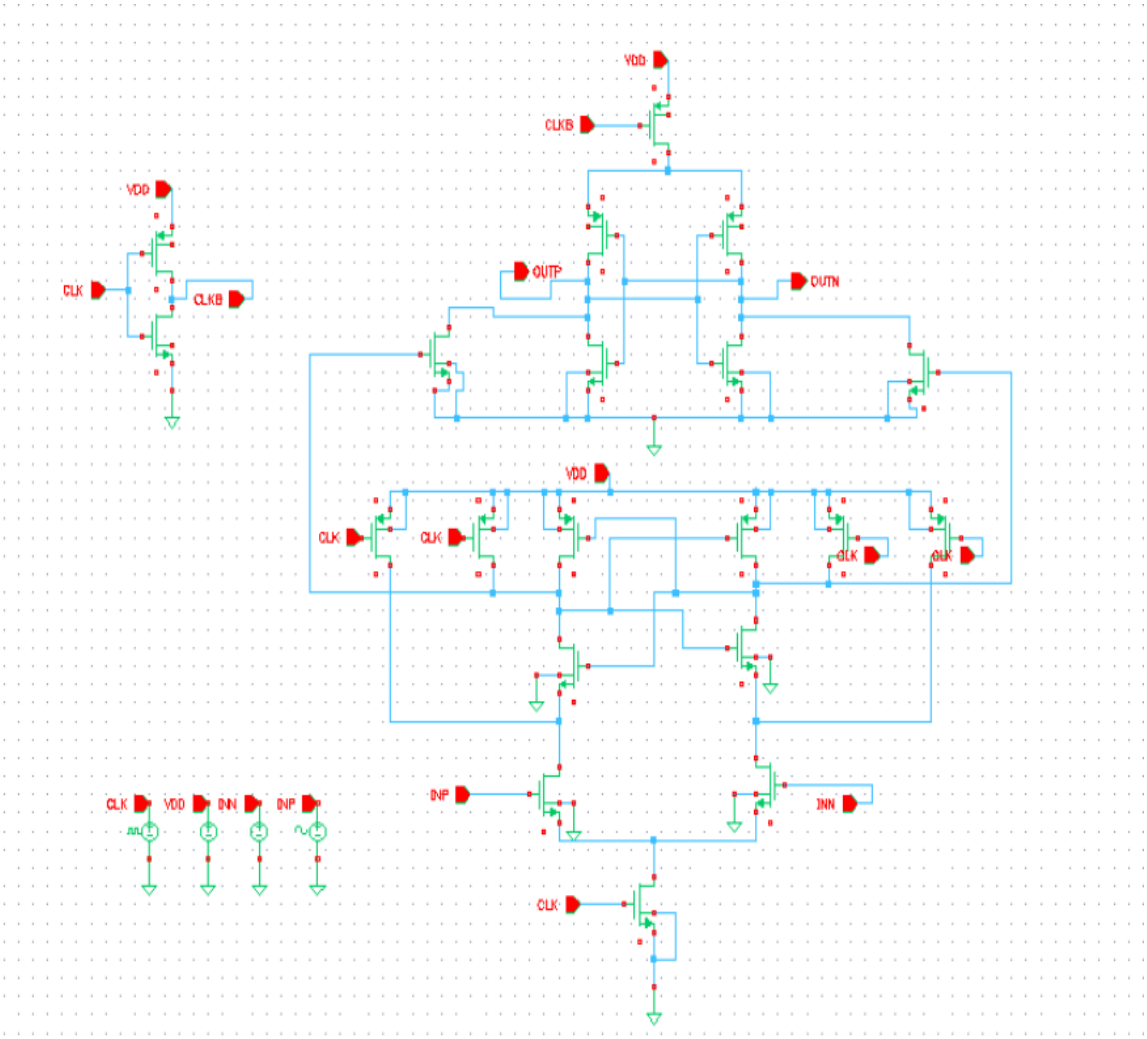


Fig. 4.5: Schematic of PDLC

CHAPTER 5

SIMULATION RESULTS AND ANALYSIS

5.1 SPECIFICATIONS

Simulations were performed on the Cadence Virtuoso tool by constructing schematics for all architectures of dynamic-latched comparators. The analyses were done 130 nm technology node.

Temperature: 27-degree centigrade

Offset voltage: 1.2 V

VDD : 1.5V

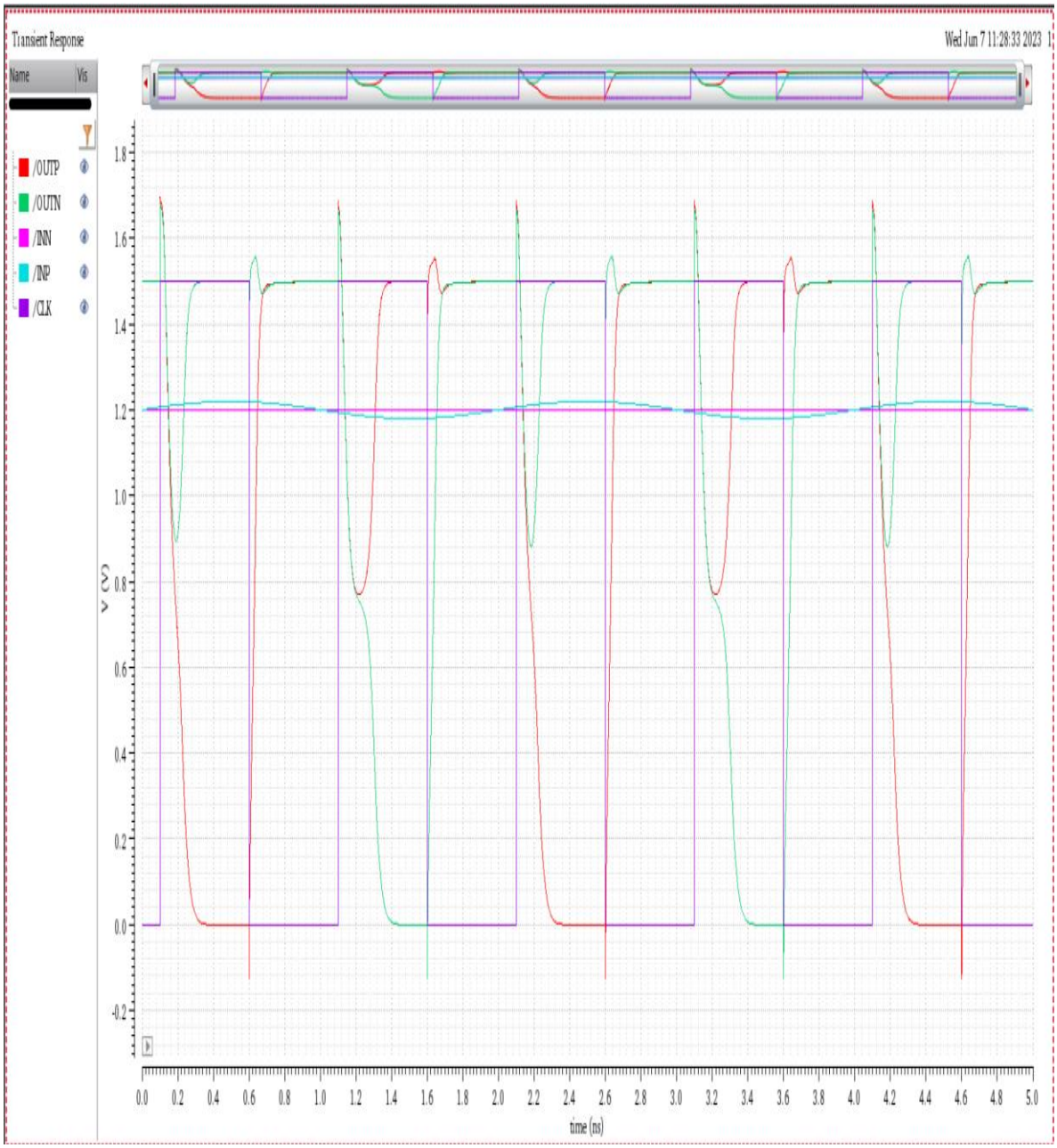
INP: It is a sine wave with frequency 0.5Ghz ,an offset voltage of 1.2 V and amplitude of 20 mV.

INN: It is DC voltage of 1.2 V

CLK: It is a clock wave of duration 5ns with rise time and fall time 0.1ps and its pulse width of 0.5ns and time period of 1ns.

5.2 TRANSIENT ANALYSIS

All the 5 architecture's transient analysis was done to verify the correct functioning of the circuit. The models were simulated using the same input data signal and a similar common mode input voltage to ensure the reliability of the performance comparison results. The simulation outputs are depicted in Fig. 5.1.


Transient Response
Wed Jun 7 11:28:33 2023
Name
Vis
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/INP
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1.6
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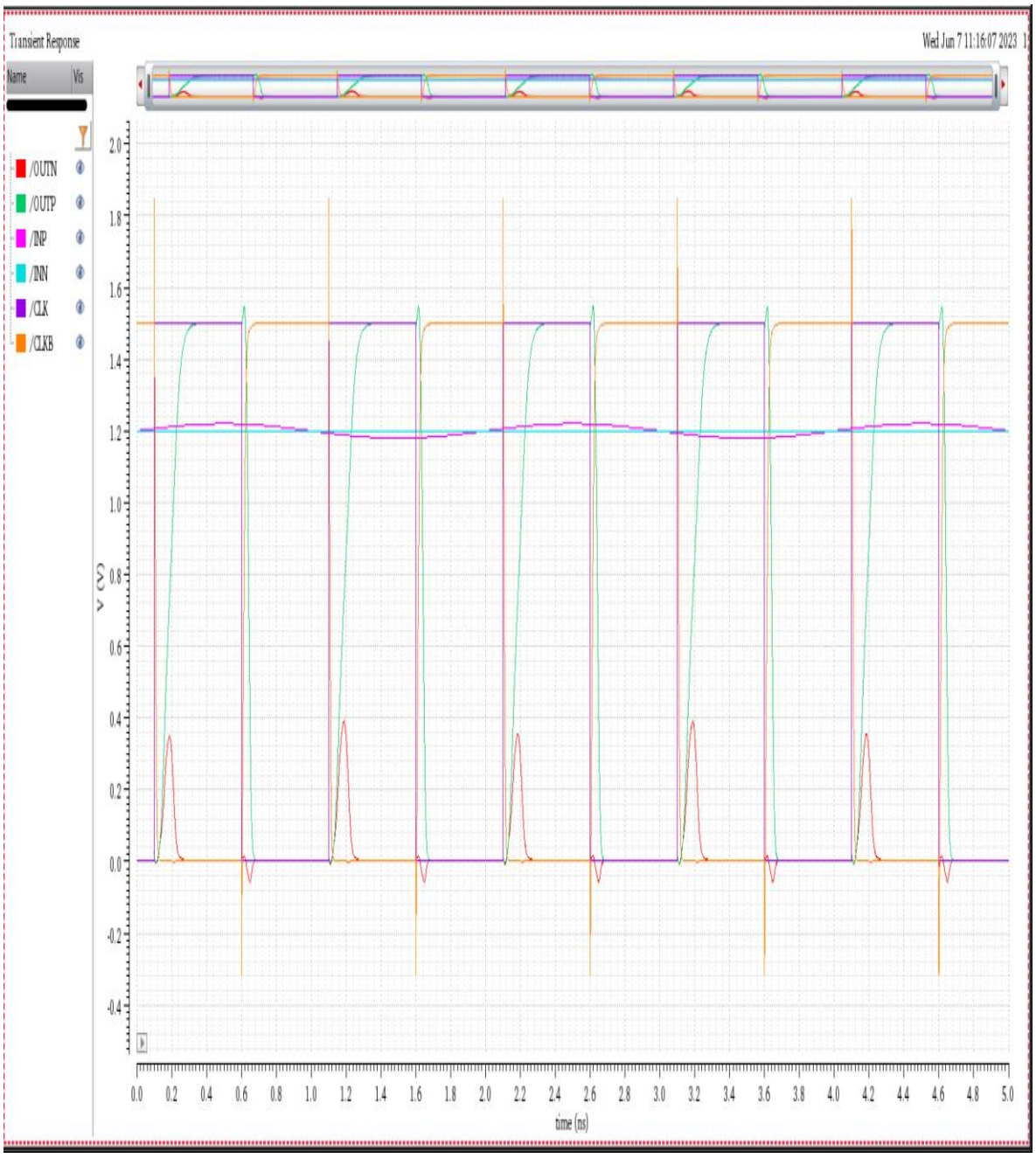
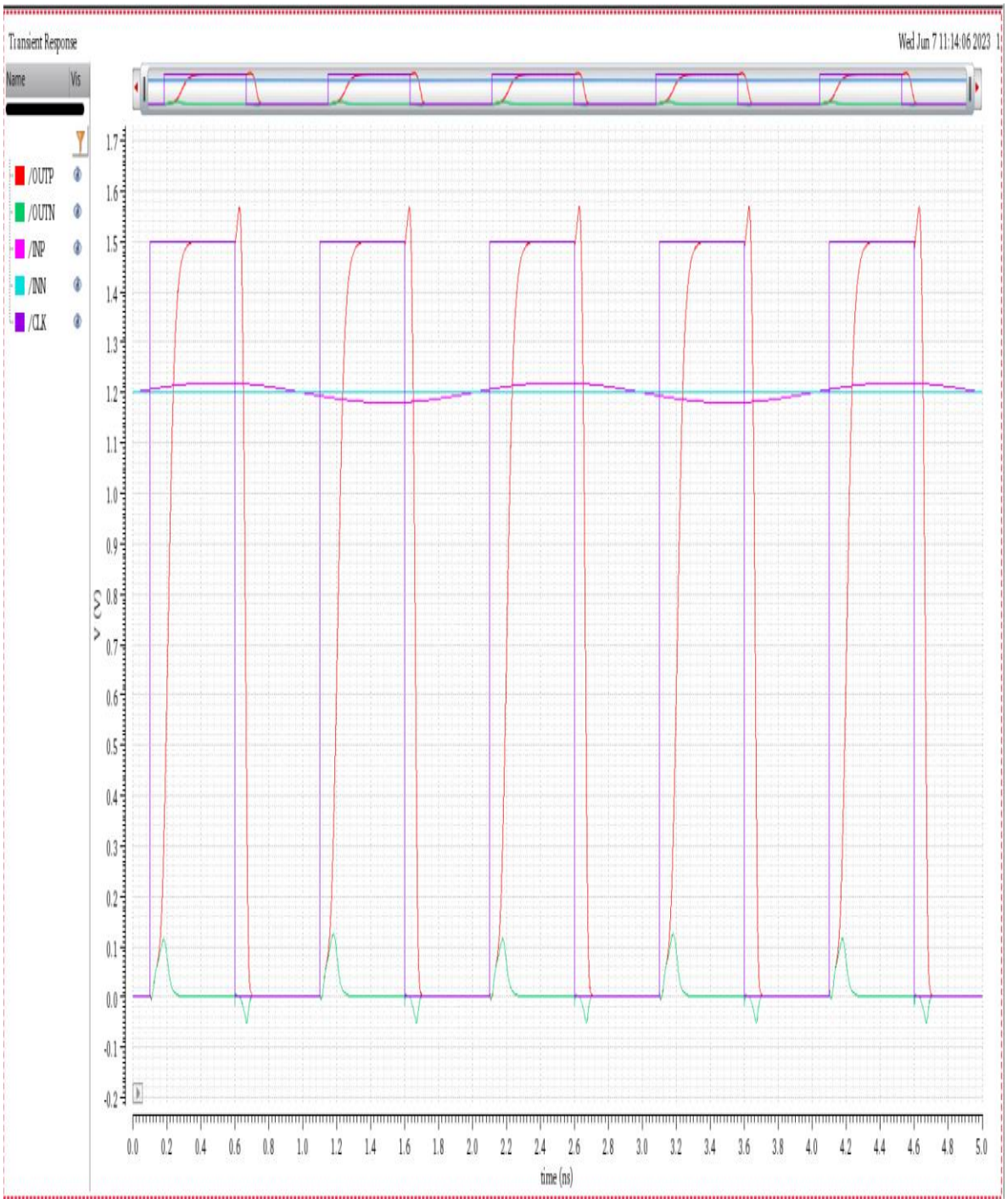
-0.2
V (V)
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0
time (ns)

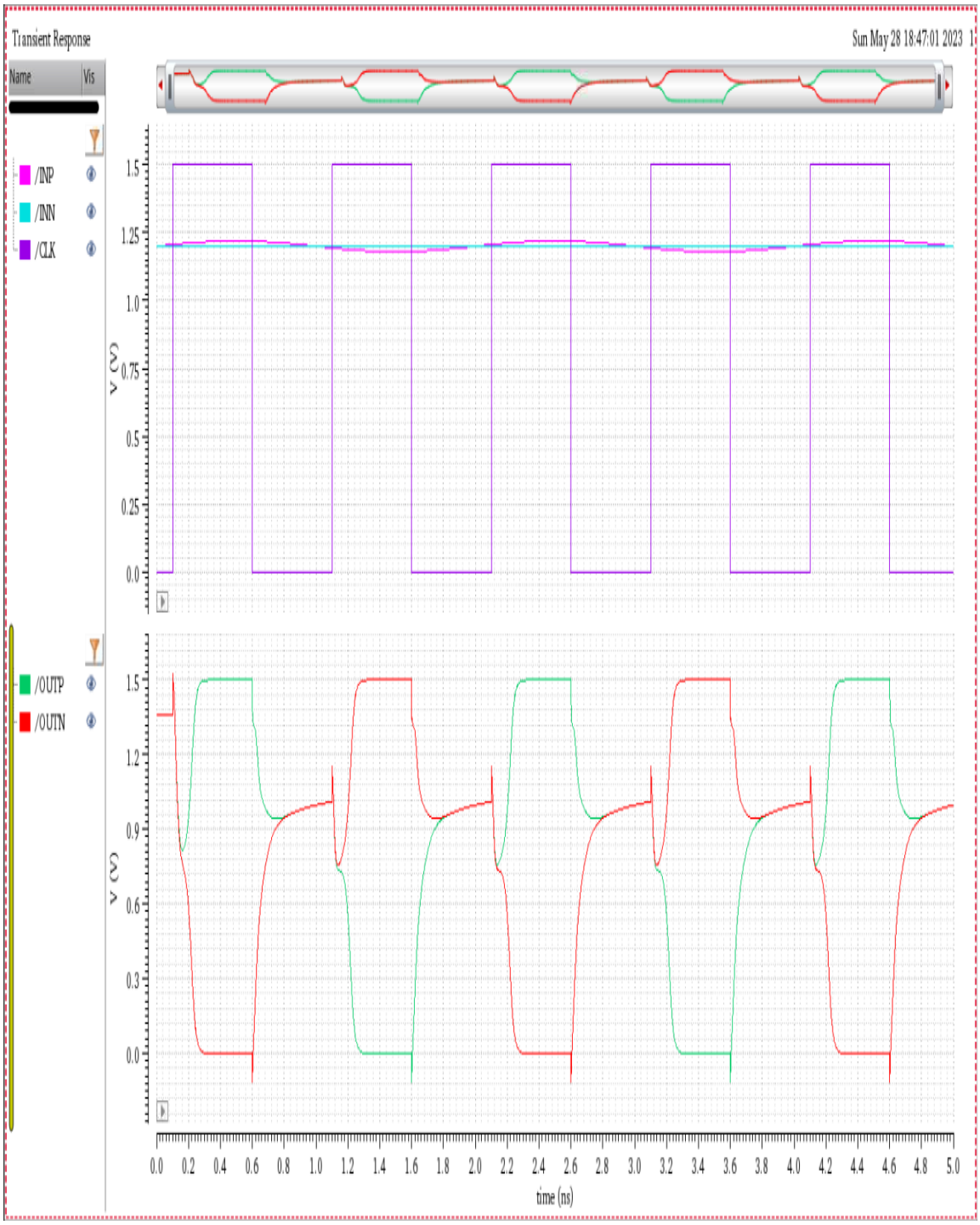
(a)


Transient Response
Wed Jun 7 11:16:07 2023
Name
Vis
/OUTN
/OUTP
/INP
/INN
/CLK
/CLKB
V (V)
time (ns)

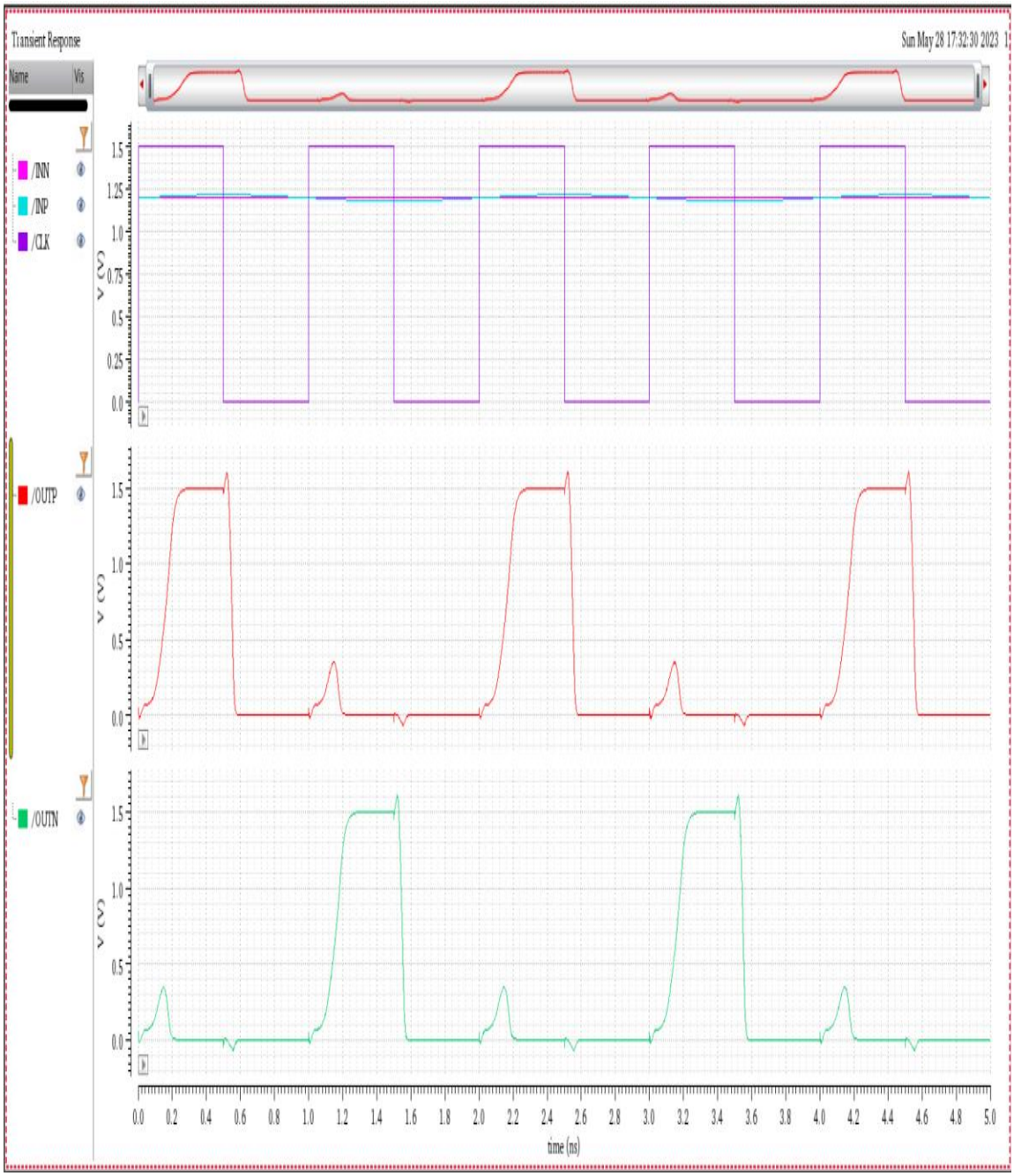
(b)


Transient Response
Wed Jun 7 11:14:06 2023
Name
Vis
/OUTP
/OUTN
/INP
/INN
/CLK
V (V)
time (ns)

(c)


Transient Response
Sun May 28 18:47:01 2023
Name
Vis
/INP
/INN
/CLK
/OUTP
/OUTN
V (V)
time (ns)

(d)

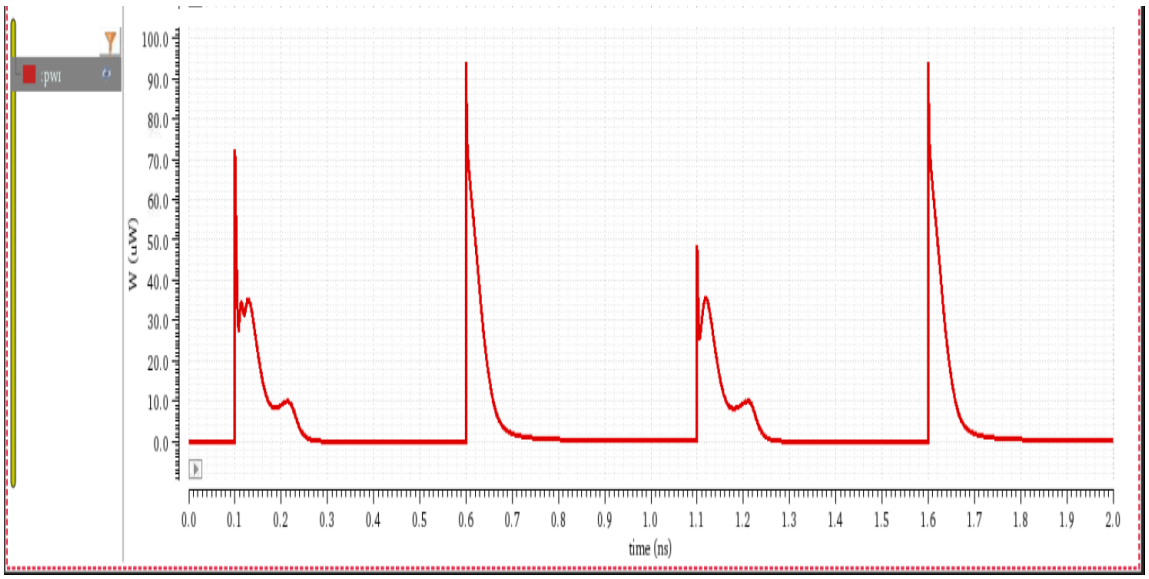


(e)

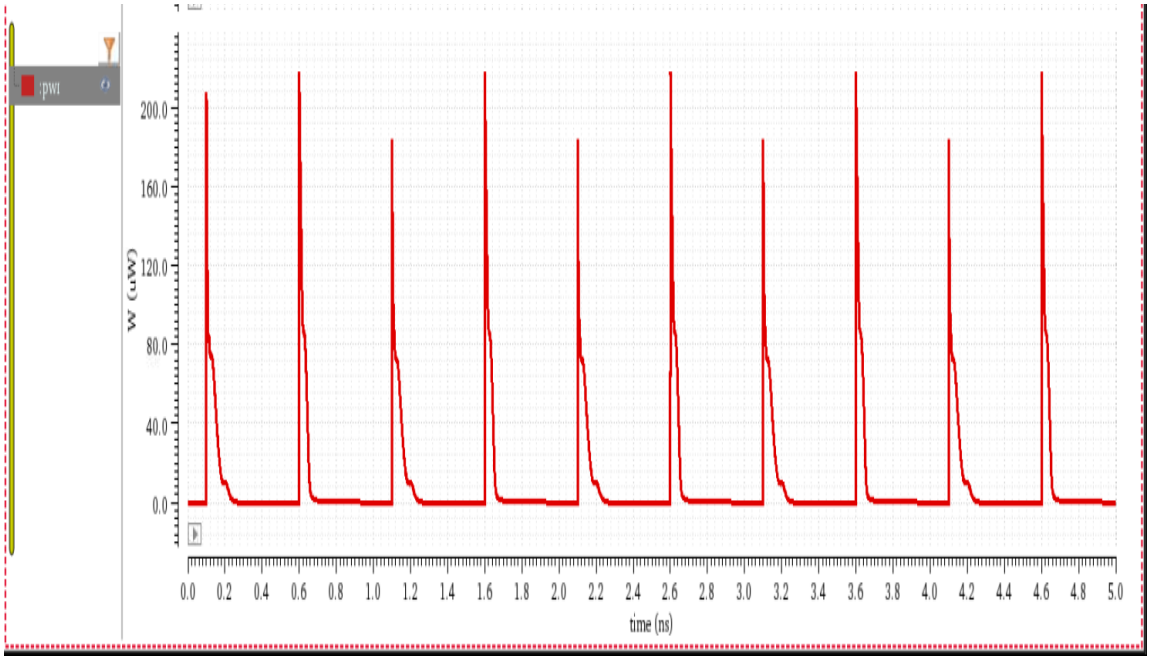
Fig. 5.1: Transient analysis of (a)STDLC (b) DTDLC (c) MDTDLC (d) SCDLC (e) PDLC

5.3 POWER CONSUMPTION

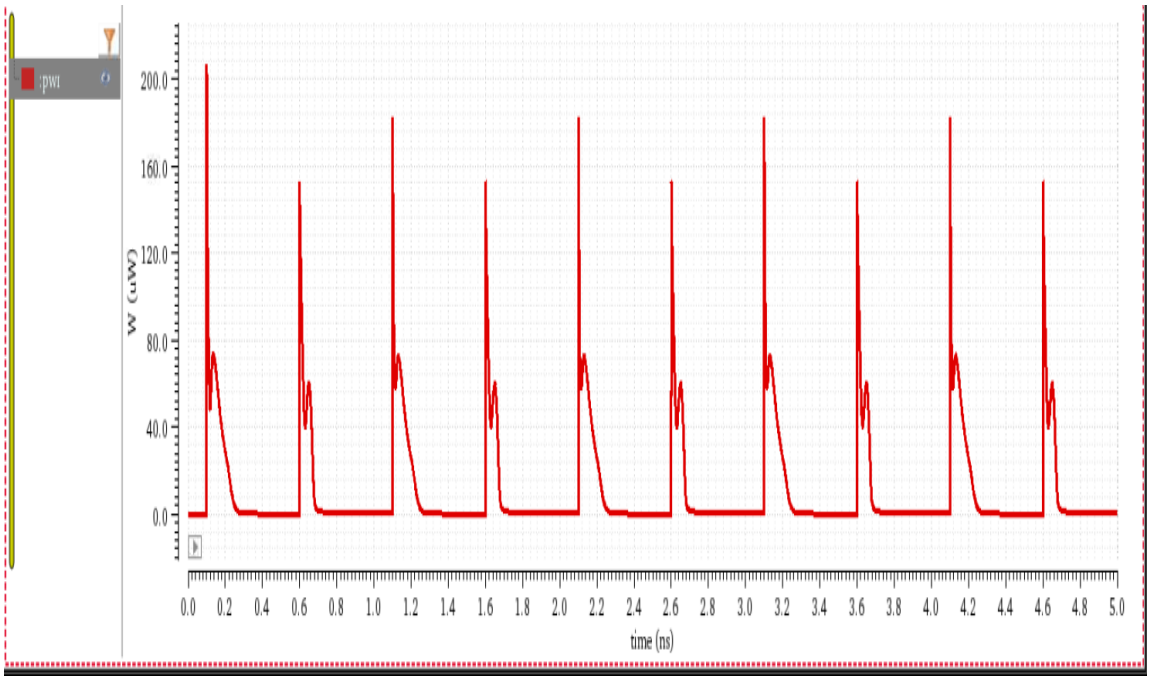
A visual comparison of the five models in terms of power consumption is shown. in Fig. 5.2.



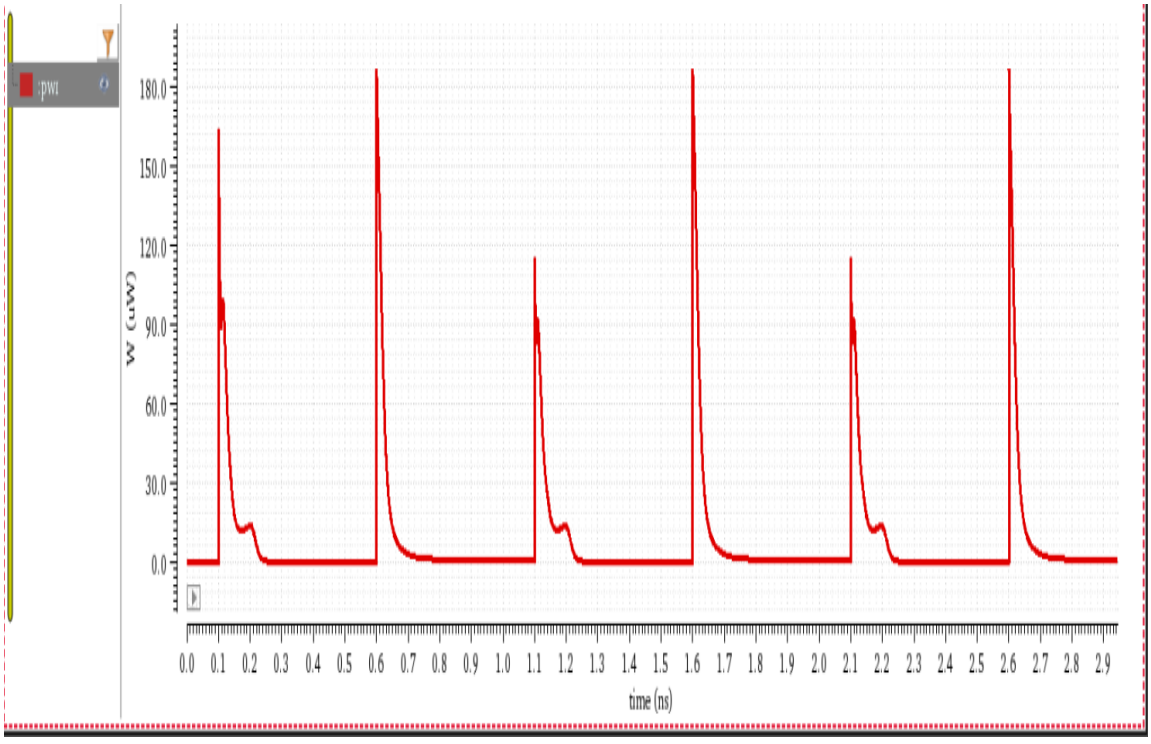
(a)



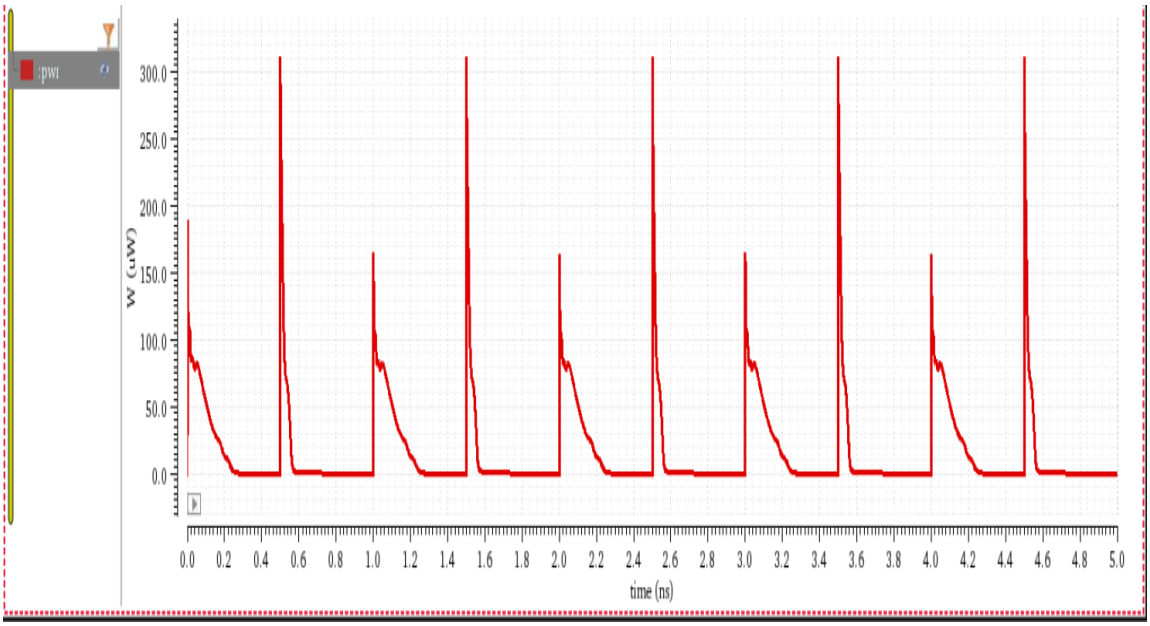
(b)


:pwr
200.0
160.0
120.0
80.0
40.0
0.0
W (uW)
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0
time (ns)

(c)


:pwr
180.0
150.0
120.0
90.0
60.0
30.0
0.0
W (uW)
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9
time (ns)

(d)



(e)

Fig. 5.2: Power of: a) STDLC, (b) DTDLC, (c) MDTDLC (d) SCDLC (e) PDLC

Architecture	**Total Average Power**
STDLC	5.269µW
DTDLC	10.28µW
MDTDLC	11.36µW
SCDLC	7.927µW
PDLC	17.69µW

Table. 5.1. Power Consumption

5.4 DELAY

Architecture	Delay
STDLC	58.63ps
DTDLC	65.62ps
MDTDLC	85.65ps
SCDLC	70.205ps
PDLC	106.68ps

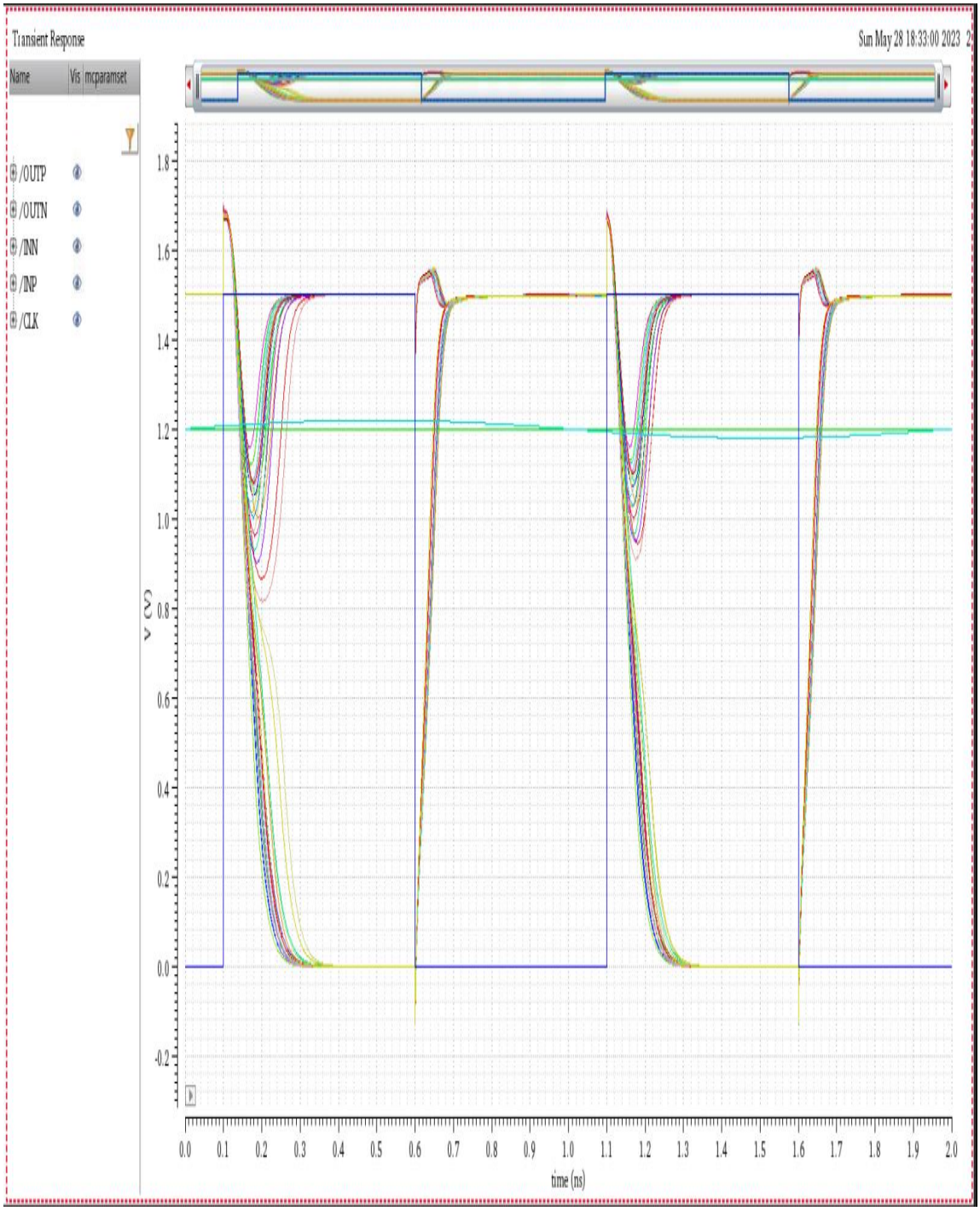
Table. 5.2: Delay comparison

5.5 POWER DELAY PRODUCT:

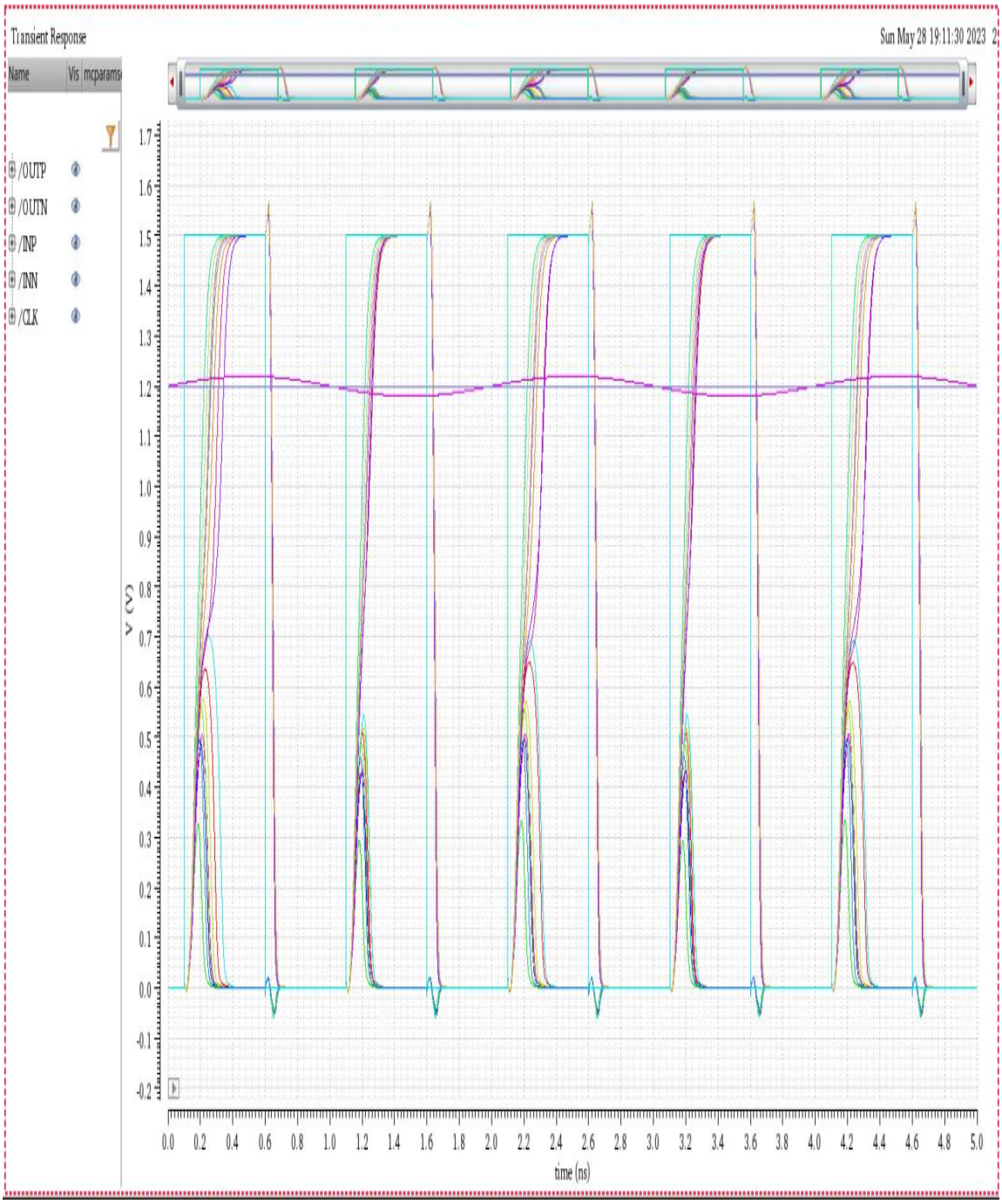
Architecture	PDP(f)
STDLC	0.3089
DTDLC	0.674
MDTDLC	0.9729
SCDLC	0.5565
PDLC	1.887

Table. 5.3: Power Delay Product(PDP) comparison

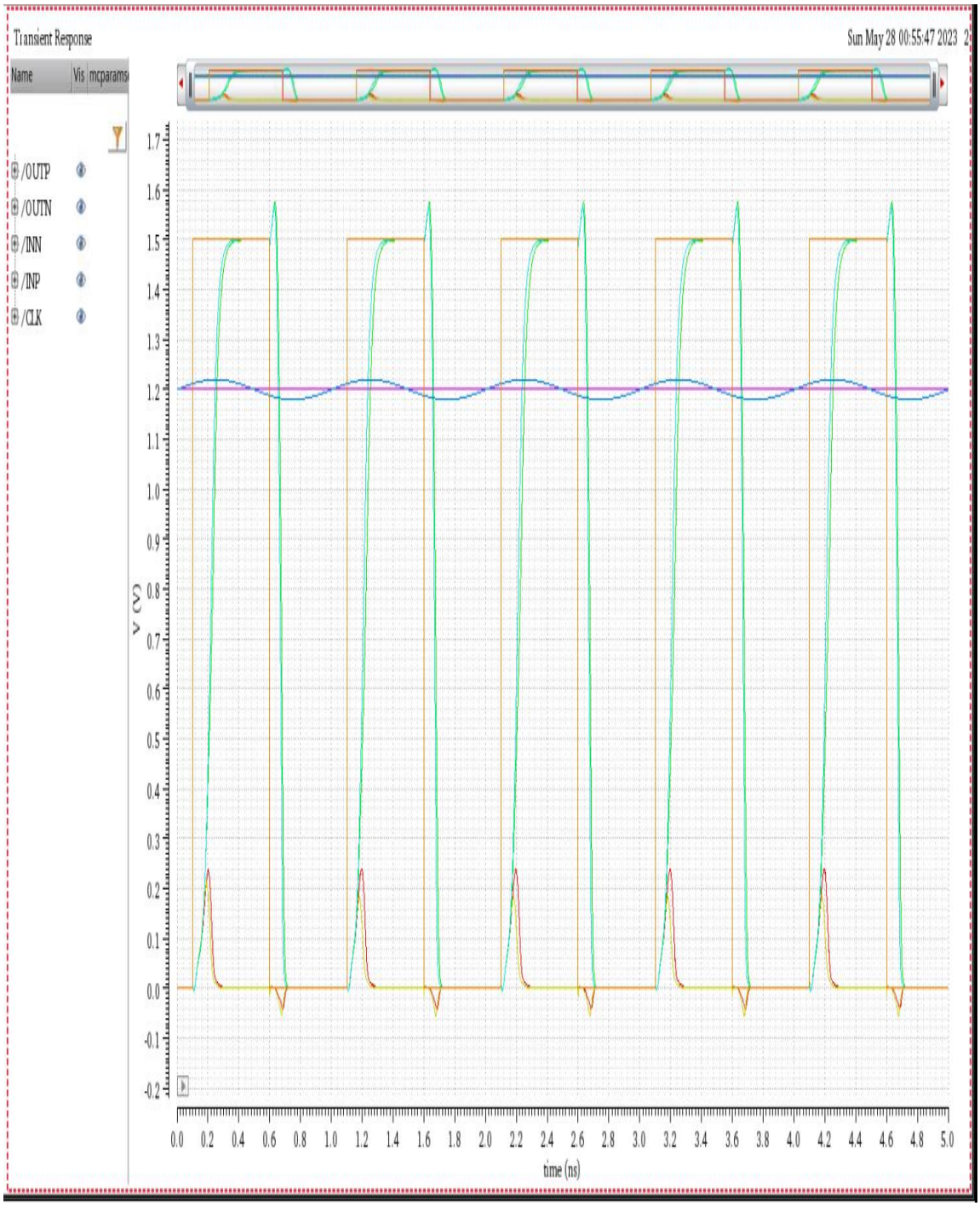
5.6 MONTE CARLO SIMULATIONS:



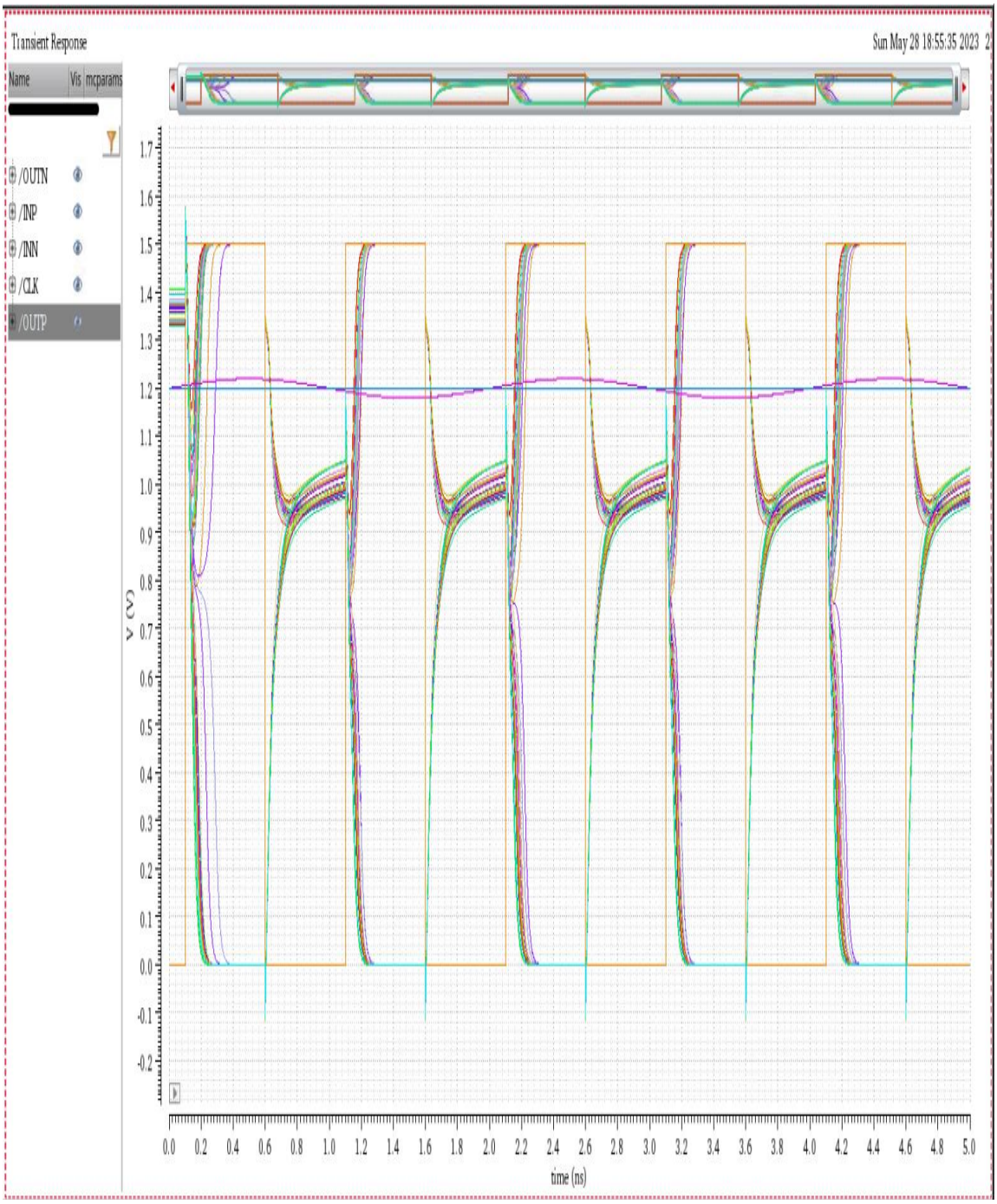
(a)


Transient Response
Sun May 28 19:11:30 2023
Name
Vis
/OUTP
/OUTN
/INP
/INN
/CLK
V (V)
time (ns)

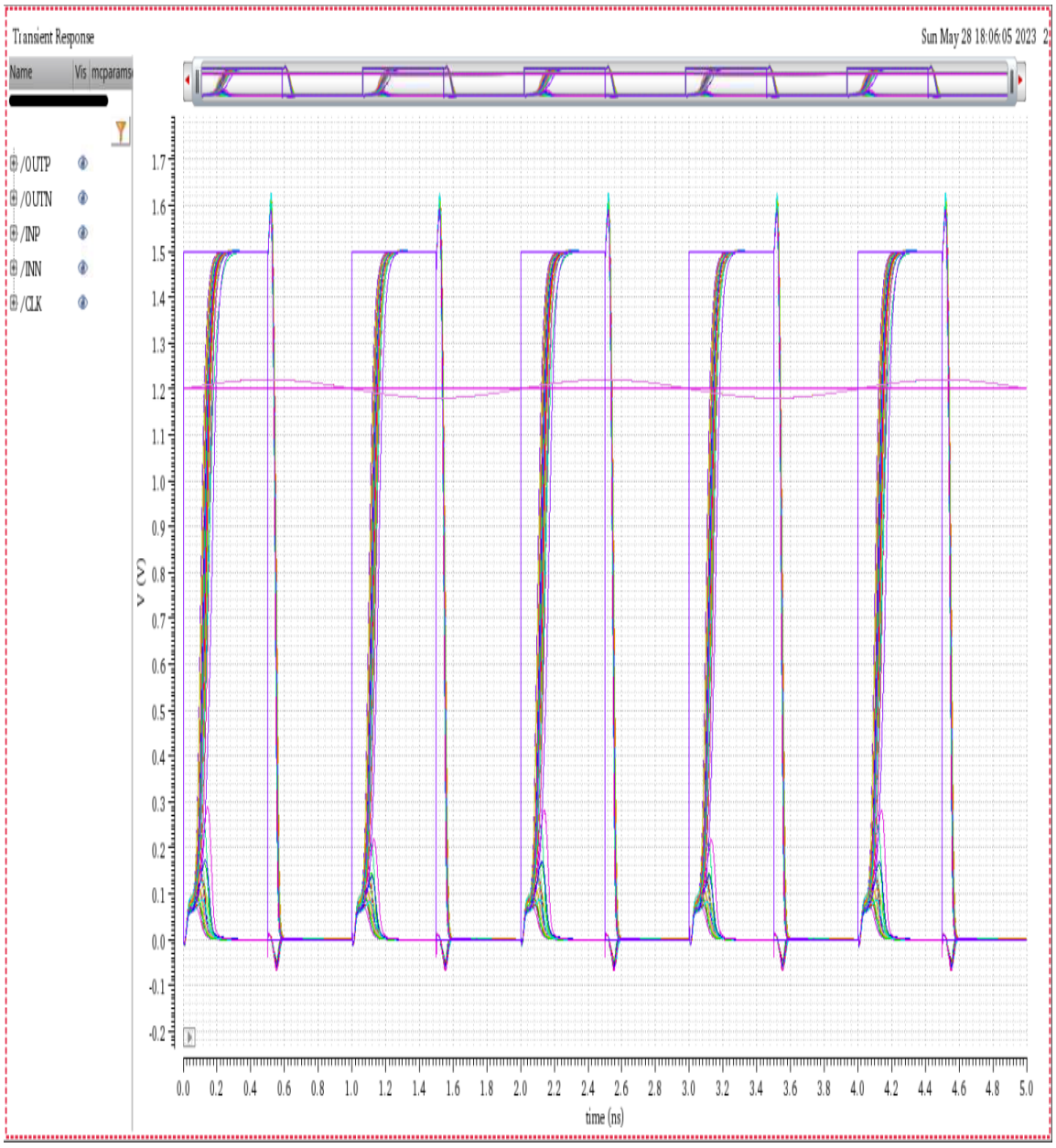
(b)


Transient Response
Sun May 28 00:55:47 2023
Name
Vis
mcparams
/OUTP
/OUTN
/INN
/INP
/CLK
V (V)
time (ns)

(c)


Transient Response
Sun May 28 18:55:35 2023
Name
Vis
mcparams
/OUTN
/INP
/INN
/CLK
/OUTP
v (V)
time (ns)

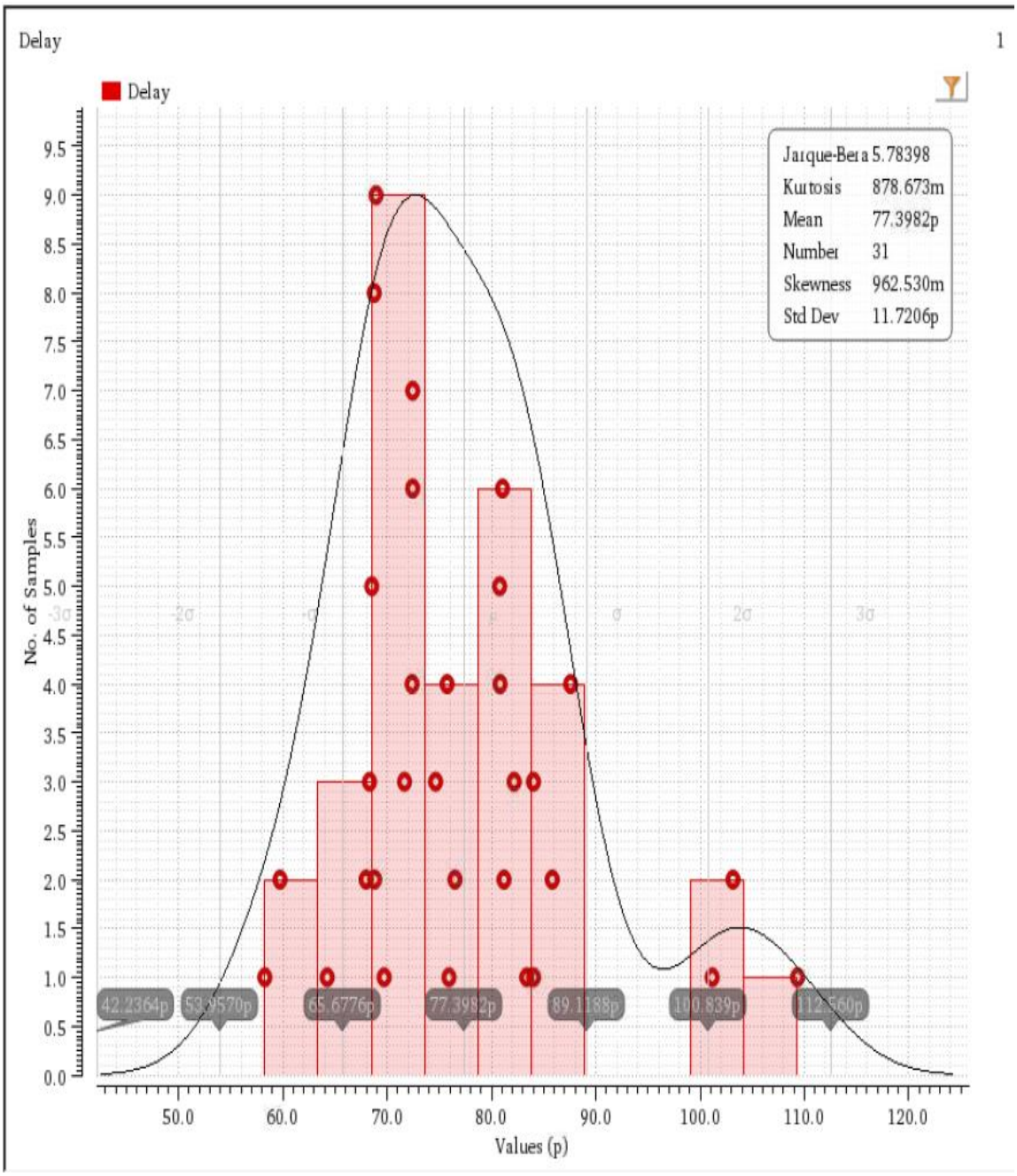
(d)



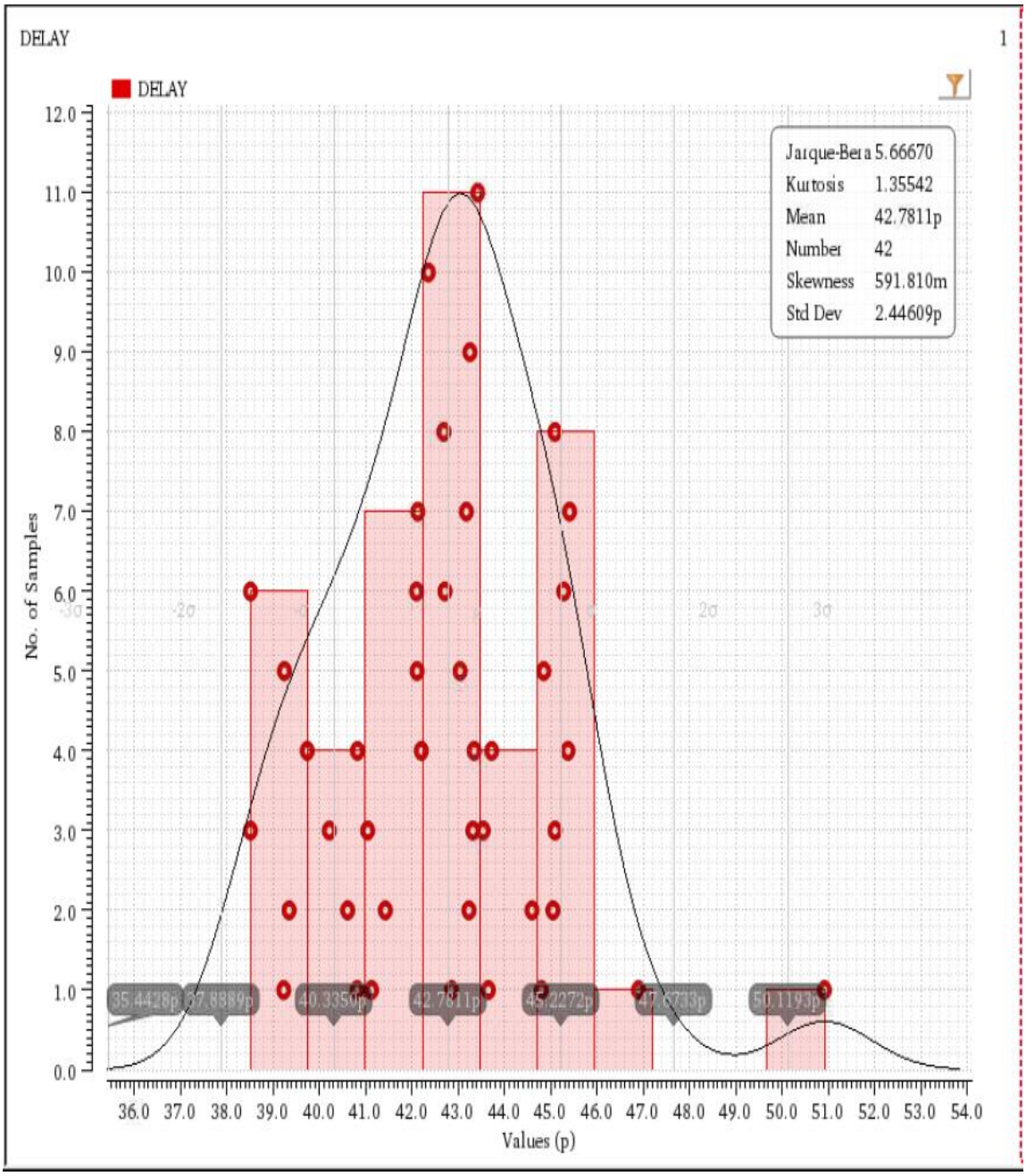
(e)

Fig 5.3:Monte Carlo Simulations of: a) STDLC, (b) DTDLC, (c) MDTDLC (d) SCDLC (e)PDLC

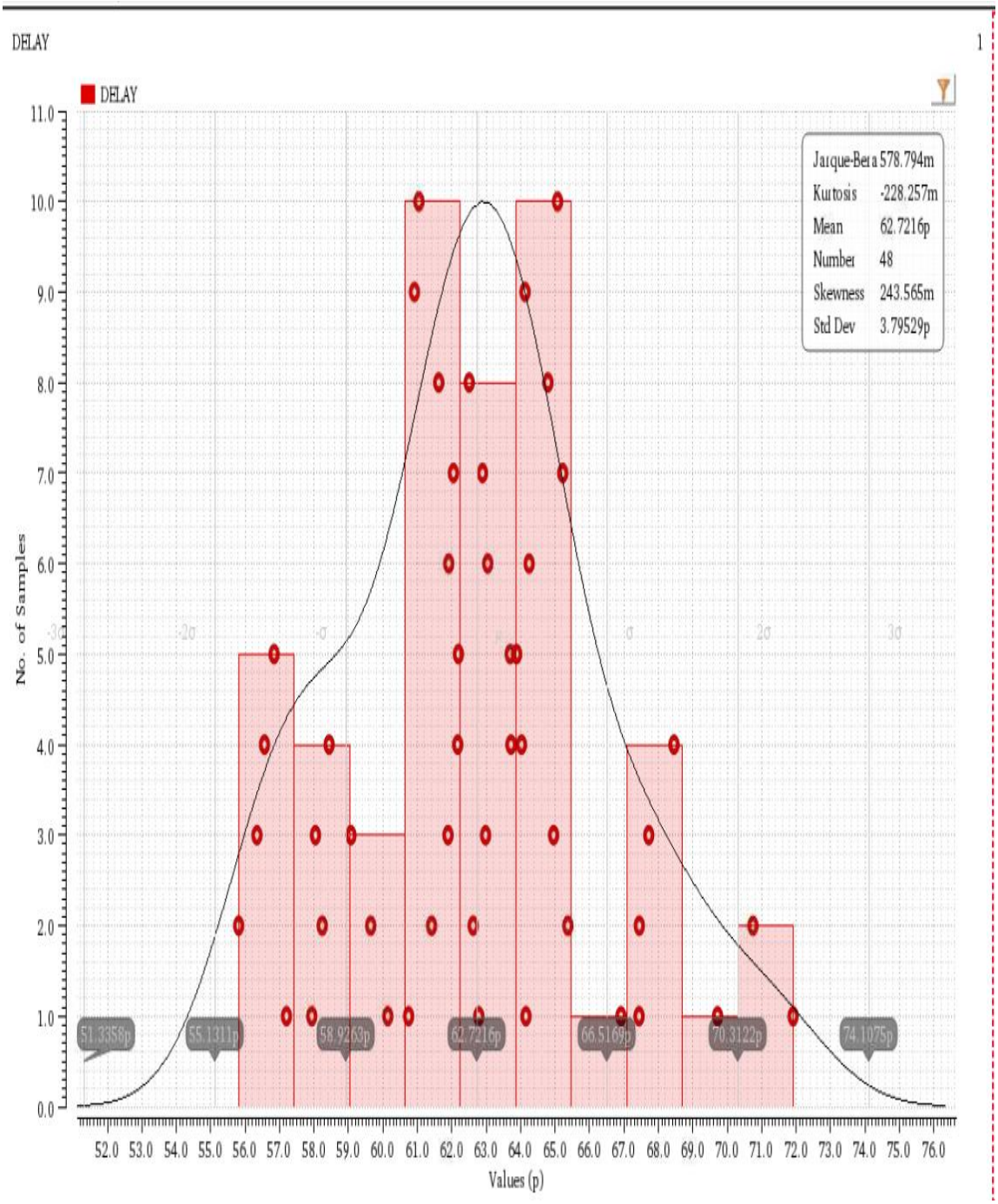
5.7 HISTOGRAM FOR DELAY:



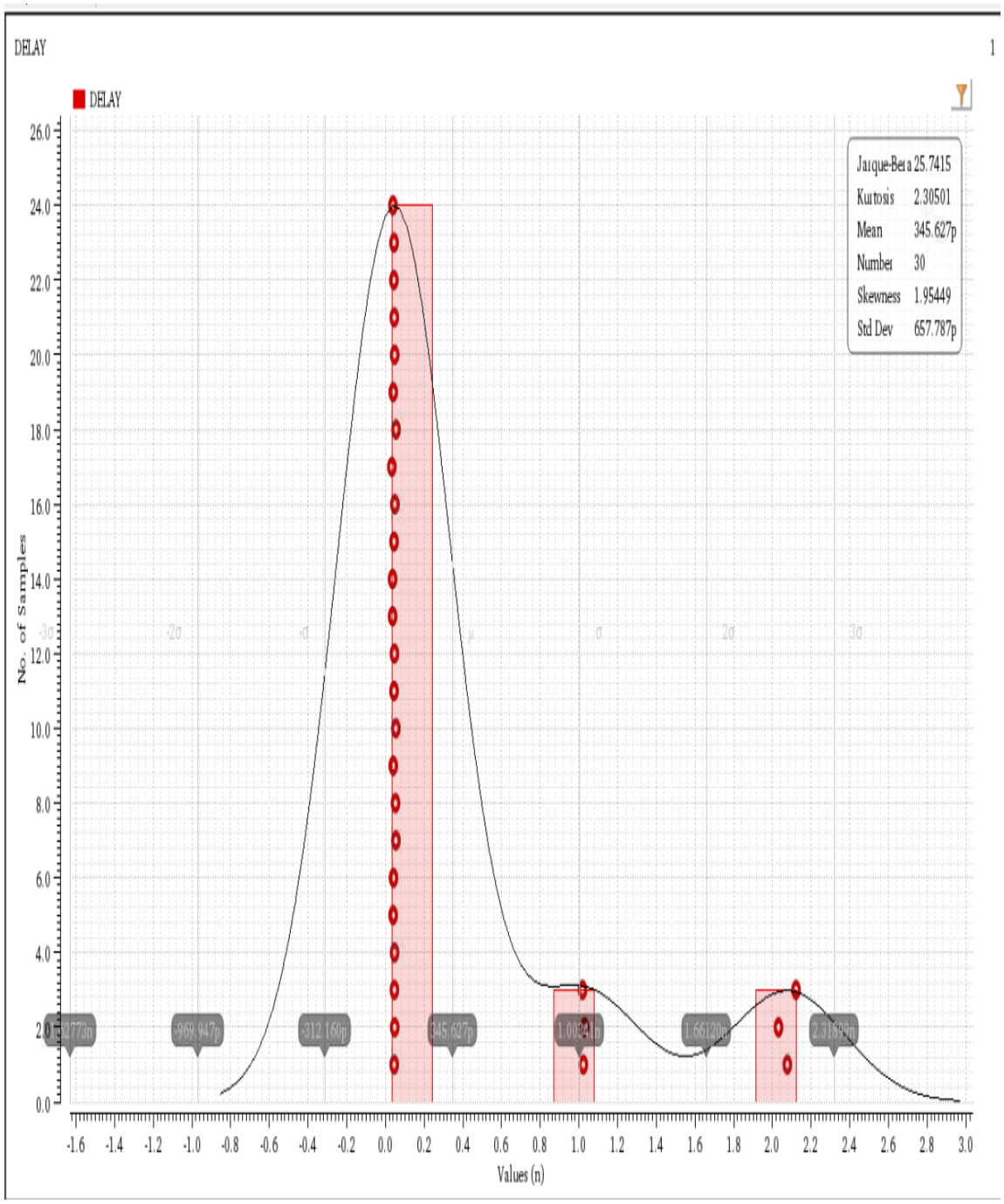
(a)


DELAY
1
DELAY
Jarque-Bera 5.66670
Kurtosis 1.35542
Mean 42.7811p
Number 42
Skewness 591.810m
Std Dev 2.44609p
No. of Samples
Values (p)
-3σ
-2σ
2σ
3σ
35.4428p
37.8889p
40.3350p
42.7811p
45.2272p
47.6733p
50.1193p

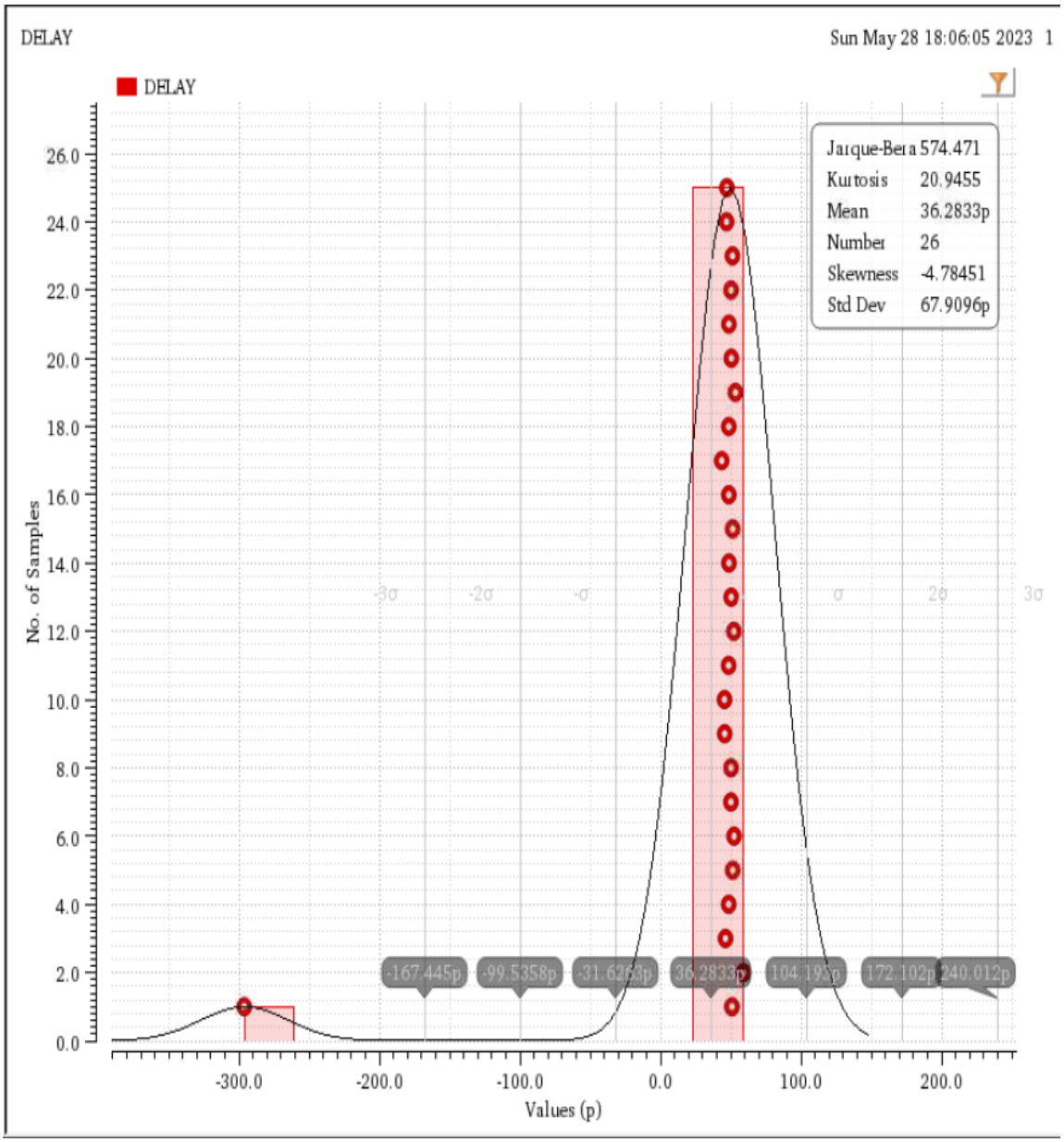
(b)


DELAY
1
DELAY
Jarque-Bera 578.794m
Kurtosis -228.257m
Mean 62.7216p
Number 48
Skewness 243.565m
Std Dev 3.79529p
No. of Samples
Values (p)
51.3358p
55.1311p
58.9263p
62.7216p
66.5169p
70.3122p
74.1075p

(c)


DELAY
1
DELAY
Jarque-Bera 25.7415
Kurtosis 2.30501
Mean 345.627p
Number 30
Skewness 1.95449
Std Dev 657.787p
No. of Samples
Values (n)

(d)



(e)

Fig. 5.4:Histogram for Power for: a) STDLC, (b) DTDLC, (c) MDTDLC (d) SCDLC (e)PDLC

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

To summarize, dynamic comparators have been investigated with various existing architecture. Simulation of the comparator shows that shared charge logic based comparator has significantly lesser power along with high operation speed and consequently it outcomes as a notably lower power-delay product (PDP). There were improvements seen in every subsequent comparator.

Architecture	Yield	Mean	Standard Deviation
STDLC	62%	77.39ps	11.721
DTDLC	84%	42.781ps	2.44
MDTDLC	96%	60.721ps	3.7995
SCDLC	60%	345.627ps	657.787
PDLC	52%	36.283p	67.99096

Table 5.4: Variation of parameters for different architecture

Future Work:

We can compare all the simulated circuits at different technology nodes and can compare the relative changes. We can incorporate newer technologies of FINFET in the transistors used in the circuits and check for further enhancements. There is also a possibility of analysing these circuits using transmission gates.

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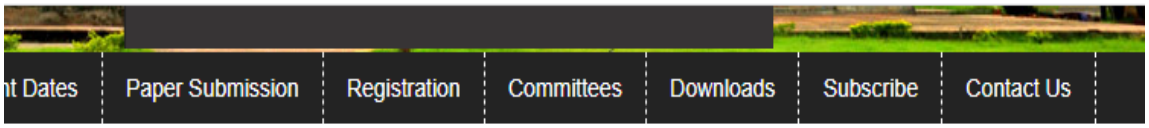

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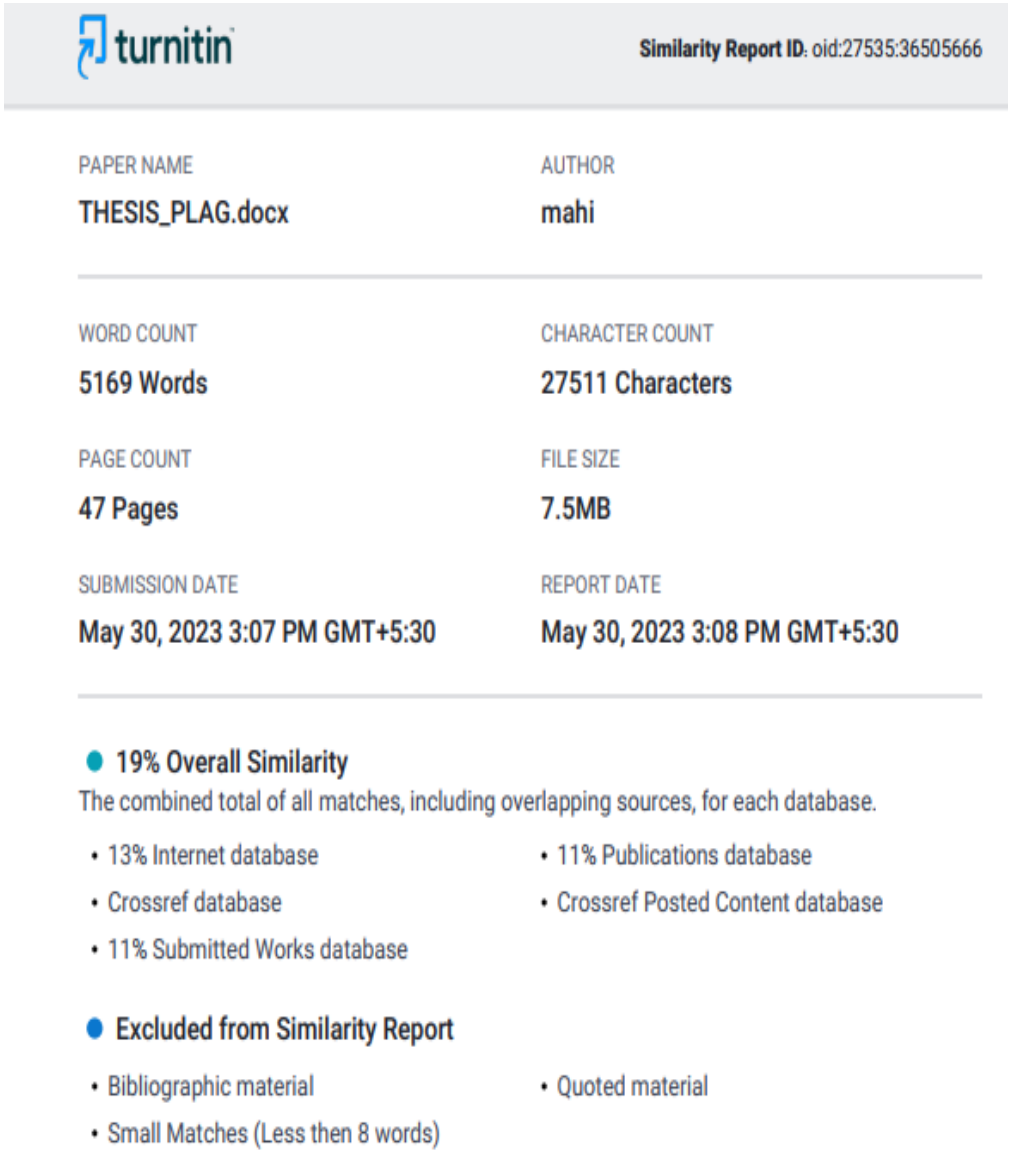

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