M. Tech (VLSI Design and Embedded System)

Mayank Shekar

2023

Performance Analysis of Memristor based SRAM and Conventional 6T SRAM Cell

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEM

SUBMITTED BY:

MAYANK SHEKHAR

2K21/VLS/14

UNDER THE SUPERVISION OF

Prof. S. Indu
PROFESSOR

ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

MAY 2023

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, MAYANK SHEKHAR (2K21/VLS/14), student of M.Tech (VLSI Design and EMBEDDED SYSTEM), hereby declare that the project Dissertation "Performance analysis of Memristor based SRAM and Conventional 6T SRAM cell" which is submitted by me to the Department of Electronics and Communication Engineering, DELHI TECHNOLOGICAL UNIVERSITY, DELHI in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, fellowship or other similar title or recognition.

Place: Delhi Mayank Shekhar

Date: May 31, 2023

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled "Performance analysis of Memristor based SRAM and Conventional 6T SRAM cell" which is submitted by MAYANK SHEKHAR Roll No. 2K21/VLS/14 to the department of Electronics and Communication Engineering, Delhi Technological University, Delhi in the partial fulfilment of the requirement for the award of the degree of Master of Technology, is record work of the report work carried out by student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date**:** May 31, 2023

Prof. S. Indu

SUPERVISOR

Professor

Department of ECE, DTU

ACKNOWLEDGMENT

I would like to express my deep sense of gratitude to my highly respected and esteemed guide, Prof. S. Indu ma'am for suggesting the topic of my project and for giving me complete freedom and flexibility to work on this topic. She has been very encouraging and motivating and the intensity of encouragement has always increased with time. Without her constant support and guidance, I would not have been able to complete this work. I extend my sincere thanks to all my friends who have patiently helped me directly or indirectly in accomplishing this work successfully.

Mayank Shekhar

2K21/VLS/14

MTech: VLSI Design and Embedded System

(2021-2023)

ABSTRACT

In current times, the number of transistors on a chip are increasing day by day. With the advancement in technology the numbers are only expected to increase. The increase in numbers of transistors on chip in turn increases the power consumption and it also increases the difficulty of fabricating the chip. There is a need of a device which can substitute the transistors on chip. Memristor is one such element. In this report, I have discussed about memristor which can be an alternative to transistors. Different types of combinational logic possible with the help of memristors is discussed. Using that, a memristor based SRAM is designed. The newly developed circuit is then compared with the traditional 6T SRAM cell. The comparison is done on the basis of delay and power. After that there is an attempt to reduce the power consumption in memristor based SRAM using MTCMOS technique. All the circuits are implemented on LTspice software.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

1.1 Introduction:

As we are developing in the field of technology, the electronic circuits are becoming more advanced and thus the transistors density on a chip used in a particular device is increasing rapidly. According to the famous Moore's law, the number of transistors on a chip is increased to double every 2 years. But the increase in the number of the number of transistors on the chip comes with its own challenges. After a certain number of transistors on the chip, it becomes difficult to include more transistors. The challenges include increase in power consumption, cost, efficiency and difficulty to develop the circuit.

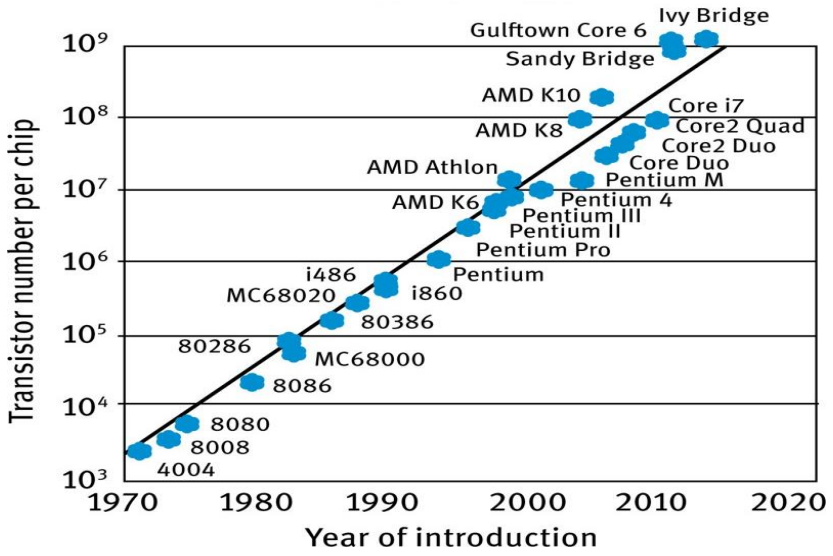


Figure 1: Moore's Law

There are different types of ideas which have been put proposed, over the years, so that the Moore's law can be continued. One of such idea is to find a small piece of component which can replace the traditionally used transistor and still the functionality of our circuit do not change. The new component, which can be used, is a memristor. The concept of Memristor was given by Professor Chua in 1971, but the first memristor was realized as late as in 2008, in HP Labs.

The words "memory" and "resistor" are combined to form the name "memristor," as this device functions similarly to a resistor, whose resistance varies depending on the amount of charge that has gone through it. Due to its ability to store data without needing a constant power source like standard RAM, it is a perfect option for use in non-volatile memory systems.

By enabling the development of "neuromorphic" systems that resemble the behavior of organic neurons, memristors also have the potential to revolutionize computing. The creation of extremely effective and potent artificial intelligence systems may result from this.

Memristors have demonstrated promise in a number of different applications besides memory and computation, including neural network modelling, adaptive filtering, and analogue signal processing.

In conclusion, the discovery and development of the memristor have expanded the field of electronics and have the potential to significantly progress a number of different sectors.

There are different types of Memristor based logics, which are used to develop the different circuits. Some of them only uses memristors, some of them are a hybrid combination of a memristor and CMOS components. In this report we will be mainly discussing the circuits which are developed using a hybrid combination of memristor and CMOS components.

This report includes discussion of memristor, the model of memristor, the spice model of memristor, memristor based logic and then the LTspice based simulations of some of the memristor using logic. After that we developed SRAM using memristor and then compared it with the conventional 6T SRAM. All the circuits were developed on LTspice software.

CHAPTER 2: MEMRISTOR

2.1 Introduction:

The theoretical framework was given by Dr. Leon Chua in 1971. But the first memristor was fabricated in 2008 at HP Labs. It is a circuit element which is having a dynamic resistance and it depends on the voltage applied across the negative and positive terminals.

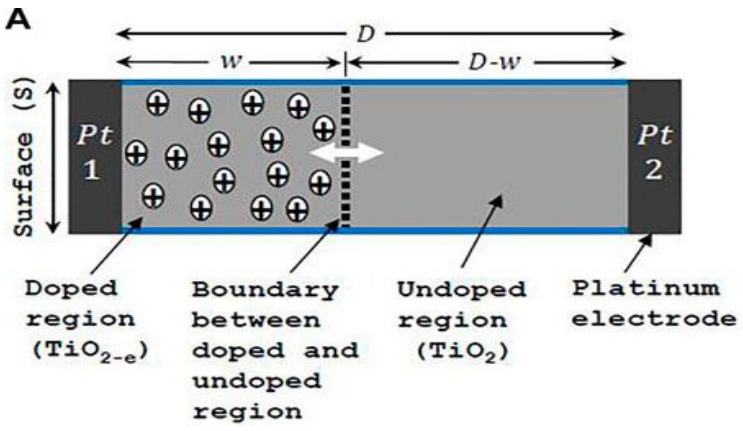


Figure 2: Memristor [2]

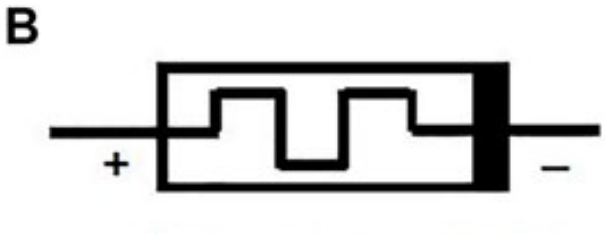


Figure 3: Memristor Symbol [2]

Whenever we switch to new element, the first question that pops up in our mind is, why? What was the need of a new element. Is it performing better than the existing element? Will it be a good alternative? Will it be able to achieve the same level of performance? Will it consume more power or will it be more efficient. To give some idea, there are several advantages of using memristor over CMOS. Unlike CMOS, memristors do not need a constant power supply to preserve their state. The fabrication of memristor is very easy in comparison to the fabrication of CMOS. Memristors can be packed with greater density than CMOS transistors, according to the results of research done so far. This enables circuit integration to be larger and storage capacity to be higher.

After the first fabrication of Memristor at HP labs, several other device structures of memristors have been published. Various types of modeling techniques are now available for modeling of memristor. The fabrication of memristor opened a path for extensive search in the area of resistive based memories. Memristors also plays a crucial role in digital logic circuits and neural network acceleration.

The resistance value of a memristor is not fixed and depends on the previous current flow through the device, which is its non-volatile property. In simpler terms, the device has the ability to remember its previous resistance value. The memristor exhibits a dynamic relationship between voltage and current, where a voltage exceeding the positive threshold voltage results in low resistance state and a voltage exceeding negative threshold voltage results in high resistance state. Otherwise, the state remains unchanged from its previous value.

There are different types of logics based on memristor. The division of categories for memristor based logic can be done on the basis of logical state variable used. Logical state variable can be either memristance or voltage response. IMPLY also known as Material Implication and MAGIC also known as Memristor-Aided Logic, uses memristance as logical state variable. MRL also known as Memristor Ratioed Logic, uses voltage response as logical state variable. Material Implication (IMPLY) and Memristor-aided Logic (MAGIC) are purely memristors based logics whereas Memristor Ratioed Logic (MRL) is a hybrid logic of memristor and CMOS components. The CMOS transistor is well compatible with memristors, as the memristors could be introduced on the available metal layer of CMOS. Introduction of these memristors logics help in reducing the area of the conventional CMOS logic circuits.

2.2 Generic Voltage-Controlled Memristor Model

The model which I used in this project is given below:

$$\frac{dx}{dt} = \begin{cases} \frac{1}{e^{x-a}} & v > 1.2 \\ 0 & -1.2 \le v \le 1.2 \\ \frac{-1}{e^{-x-a}} & v < -1.2 \end{cases}$$

$$R(x) = \begin{cases} R_{ON} & x \ge 0 \\ R_{OFF} & x < 0 \end{cases}$$

$$i(t) = \frac{1}{R(x)} v(t)$$

The given equations represent the relationship between different variables in a memristor circuit. The state variable 'x' is influenced by the voltage 'v' measured across the memristor, a parameter 'a', and the current 'i' flowing through it. The value of 'dx/dt' changes only when

the input voltage exceeds certain threshold levels. When 'dx/dt' equals zero, 'x' remains unchanged. However, when 'dx/dt' equals either '1/(e^(x-a))' or '-1/(e^(-x-a))', 'x' starts to increase or decrease rapidly, respectively. By solving these equations, we can observe that for 'v' greater than 1.2, 'x' increases monotonously with increasing 'a', while for 'v' less than -1.2, 'x' decreases monotonously with increasing 'a'. Therefore, we can conclude that as the value of 'a' increases, the memristor can switch between different values more quickly.

2.3 Spice Model

The spice model for the memristor which I have used for this project is given below. The below spice model is used to generate the symbol of memristor in LTspice, and further it was used to design the digital circuits.

```
.subckt erzhi TE BE

.params X0 = -2, R0 = 1000, R1 = 100

.func dx(V,X) = IF(V>1.2,1/EXP(X-10),IF(V>-1.2,0,-1/EXP(-X-10)))
.func Rm(x) = IF(X<0,R0,R1)
.func Gm(V,X) = V / Rm(X)

Cx XSV 0 {1}
.ic V(XSV) = X0

Gx 0 XSV value = {dx(V(TE,BE),V(XSV,0))}
Gm TE BE value = {Gm(V(TE,BE),V(XSV,0))}

.ends erzhi
```

CHAPTER 3: LOGIC CIRCUITS

3.1 Memristor Ratioed Logic Circuits (MRL)

While designing the circuits we take Vhigh as the binary state 1 and Vlow as the binary state 0. For Or, let's take an example, when Vin1 is high or at binary state1, then the resistance for the memristor1 is low resistance, Ron. Similarly, when Vin2 is low or at a binary state 0, then the resistance for memristor2 is high resistance, Roff. Thus, the output resistance can be expressed as:

$$V_{out} = \frac{R_{OFF}}{R_{ON} + R_{OFF}} V_{high} \approx V_{high} = 1$$

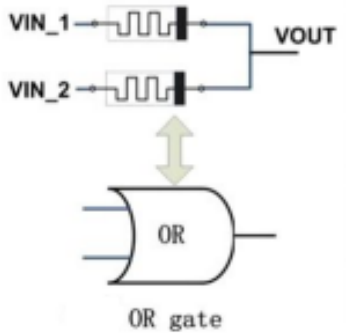


Figure 4: OR gate using memristor [1]

Similarly, for different inputs, that is Vin1 and Vin2 are 11, 00 and 01, we can check that the results obtained are in coherence with the truth table of OR gate.

Designing of AND gate could be done in similar way as that of OR gate, but in this case just the polarity of the memristors will change.

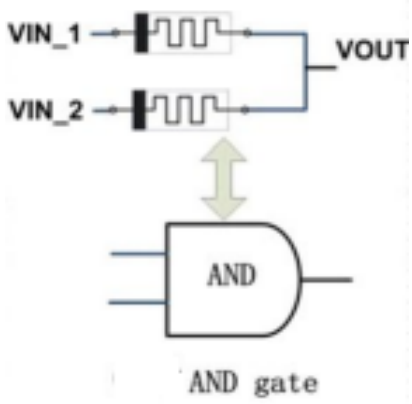


Figure 5: AND gate using memristor [1]

As we can see from the above equation, the output voltage is not exactly one, but it is approximately equal one. So to nullify this effect we can add a CMOS inverter after the OR gate to boost the signal. Thus, we will get the circuit of NOR gate.

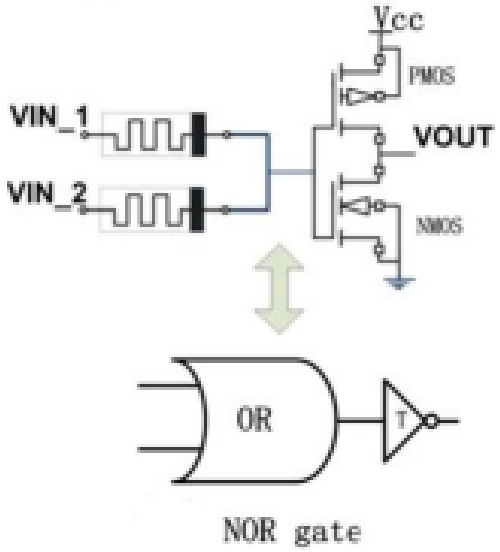


Figure 6: NOR gate using Memristor [1]

We can also construct N input gates using memristors, we just need to connect the one end of all the memristors together, from where we need to take the output, one such example of N-input NOR gate is given below:

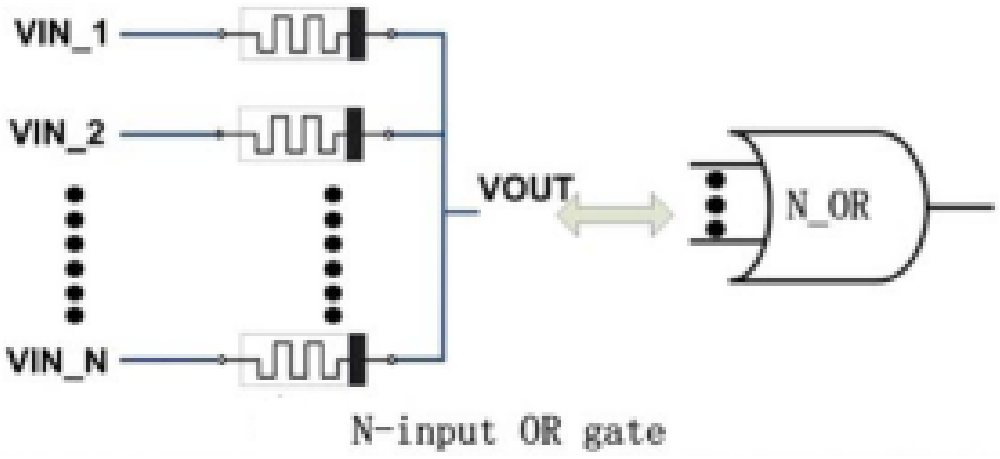


Figure 7: N-input OR gate using Memristor [1]

Generally for NOT gate, researchers use CMOS inverters, but we can also construct a NOT gate using one NMOS transistor and one memristor. The front end of the memristor is connected to DC voltage Vcc and the input voltage is connected to gate of the NMOS and the output voltage is taken from the drain of NMOS.

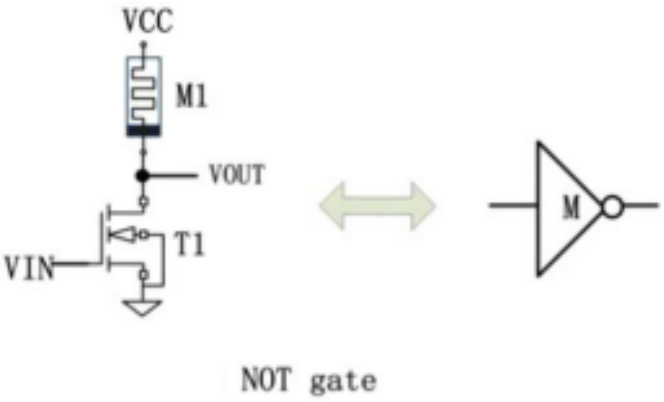


Figure 8: NOT gate using memristor [1]

When the given signal is at high voltage level, the transistor is turned on, and since the memristor is connected to Vcc, means the value of resistance will be Ron. Since the transistor is on, the resistance offered by transistor is very minimal. As we applied the voltage divider in above case, we will apply the same here also. Rt is the resistance offered by transistor.

When the input voltage applied is logic 1, then the output is given by:

$$V_{OUT} = \frac{R_T}{R_{ON} + R_T} V_{CC} \approx 0$$

Similarly, when the input voltage is logic 0, then the output is given by:

$$V_{OUT} = \frac{R_T}{R_{ON} + R_T} V_{CC} \approx 1$$

If we replace the DC voltage, Vcc with any other input signal, for example a signal A, we will be able to get the value of A.Bbar, as shown below. For A=1, B=1 the memristor offer low resistance and transistor will also offer low resistance so output is zero. For A=1, B=0, the memristor offer low resistance and transistor offer high resistance, as the transistor is off, so the output becomes 1. When A=0, the output sets to 1, regardless of the value of B.

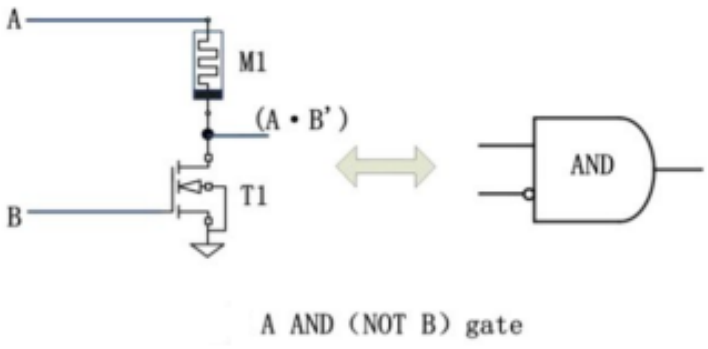


Figure 9: A And (Not B) gate [1]

We can also construct 2 input NOR in the similar fashion, the circuit for 2 input NOR is shown below. When both inputs are 0, then both the transistors are off and they offer high resistance thus the output is 1, since the memristor is offering a low resistance, Ron. When one of the inputs is 1, that is one of the transistors is on, then there is a connection between output and ground. Thus, the output value is 0. When both the inputs are one, both the transistors are on, and there is a connection from output to ground, so the output is zero. Thus, it is following the truth table of NOR gate.

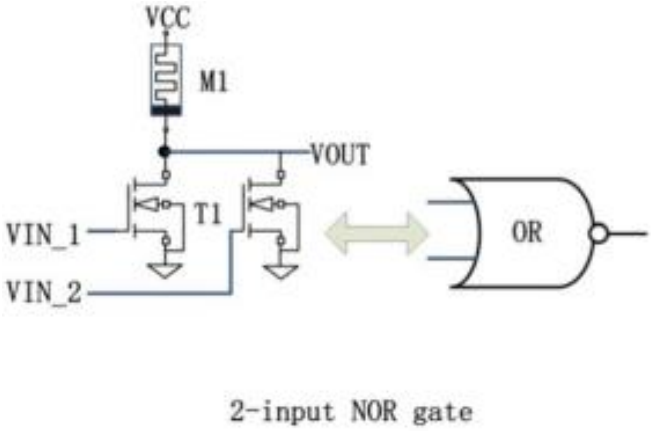


Figure 10: 2-input NOR gate using memristor [1]

3.2 Memristors based Combinational Logic Circuits

We are able to design several gates by using Memristor ratioed logic (MRL). Similarly, we can use them to design different types of combinational circuits. The circuits which are designed using Memristor ratioed logic (MRL), when compared with conventional CMOS circuits, decreases the energy consumption and the total number of elements used. In the

following sections we will design encoder, decoder, mux and 1 bit comparator using memristor ratioed logic.

3.2.1 Encoder using Memristor

Encoder is a circuit which have '2^n' number of lines at the input side and it has 'n' number of outputs. The circuit will make the output lines high, which are binary equivalent of the input. The diagram is shown below along with the truth table:

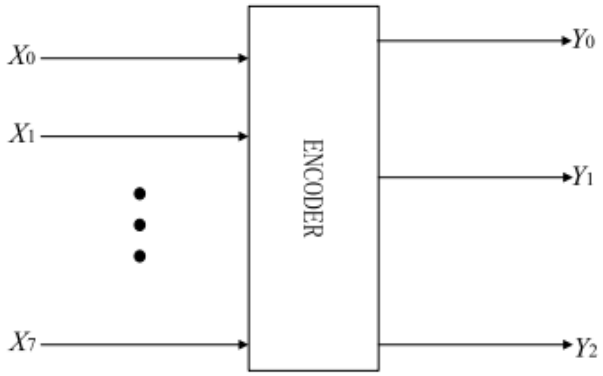


Figure 11: Block Diagram of Encoder

Table 1: Truth table of Encoder

X0	X1	X2	X3	X4	X5	X6	X7	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

The output equations can be derived from the truth table. The equations come out to be:

$$Y_2 = X_4 + X_5 + X_6 + X_7$$
$$Y_1 = X_2 + X_3 + X_6 + X_7$$
$$Y_0 = X_1 + X_3 + X_5 + X_7$$

We can develop the circuit for encoder using the above equations. We already know how to design a n-input NOR gate. So, we will use NOR gate in continuation with a NOT gate to design the output equations. For each output equation, i.e., Y2, Y1, Y0, we will require a 4-input NOR gate in continuation with a NOT gate. For a 4-input NOR gate we will need 4

NMOS and 1 memristor. For a NOT gate we will need 1 NMOS and 1 memristor. So, for the whole circuit of encoder, we will require 15 NMOS and 6 memristors.

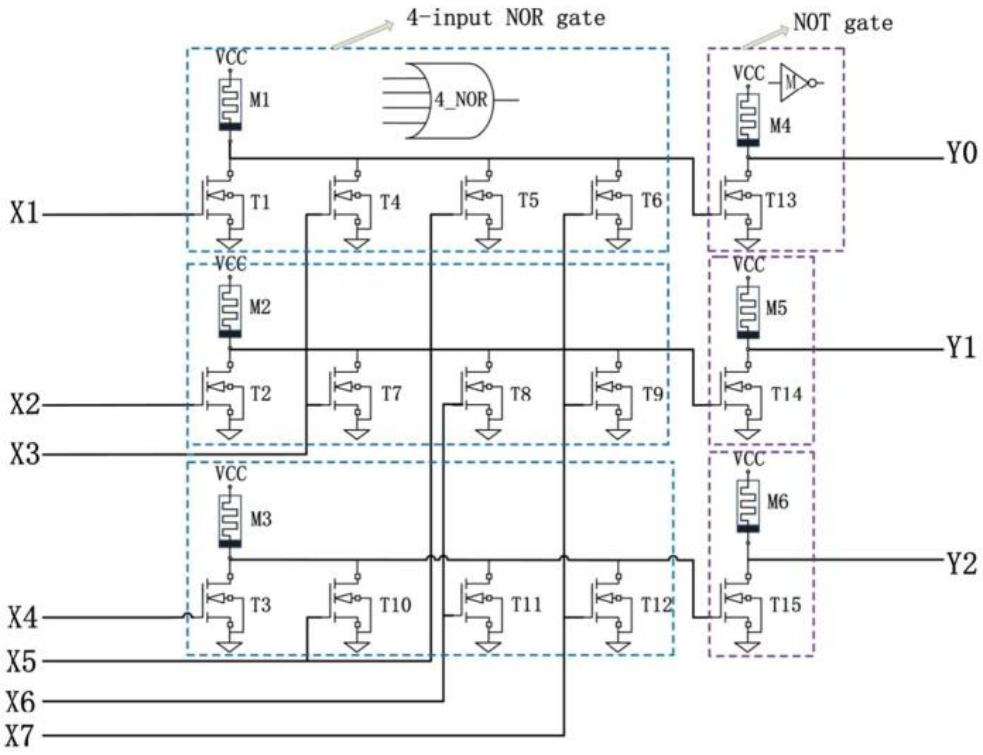


Figure 12: 3-bit Encoder [1]

3.2.2 Decoder using Memristor

Decoder is a circuit which has ‘n’ number of lines at the input side and ‘2^n’ number of lines at the output side. The circuit performs exact opposite of an encoder. The decoder turns that output line high which is equivalent to the decimal value of the input provided at the input lines. The block diagram is shown below along with the truth table:

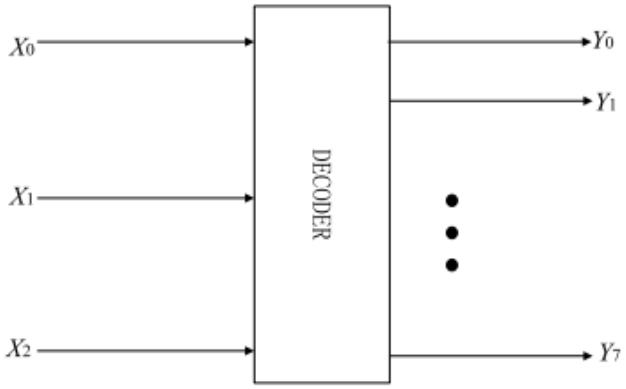


Figure 13: Block diagram of Decoder

Table 2: Truth table of Decoder

X2	X1	X0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

The output equations can be derived from the truth table. The equations come out to be:

$$Y_0 = \overline{X_2 X_1 X_0}, \quad Y_1 = \overline{X_2} X_1 X_0, \quad Y_2 = \overline{X_2} X_1 \overline{X_0}$$
$$Y_3 = \overline{X_2} X_1 X_0, \quad Y_4 = X_2 \overline{X_1 X_0}, \quad Y_5 = X_2 \overline{X_1} X_0$$
$$Y_6 = X_2 X_1 \overline{X_0}, \quad Y_7 = X_2 X_1 X_0$$

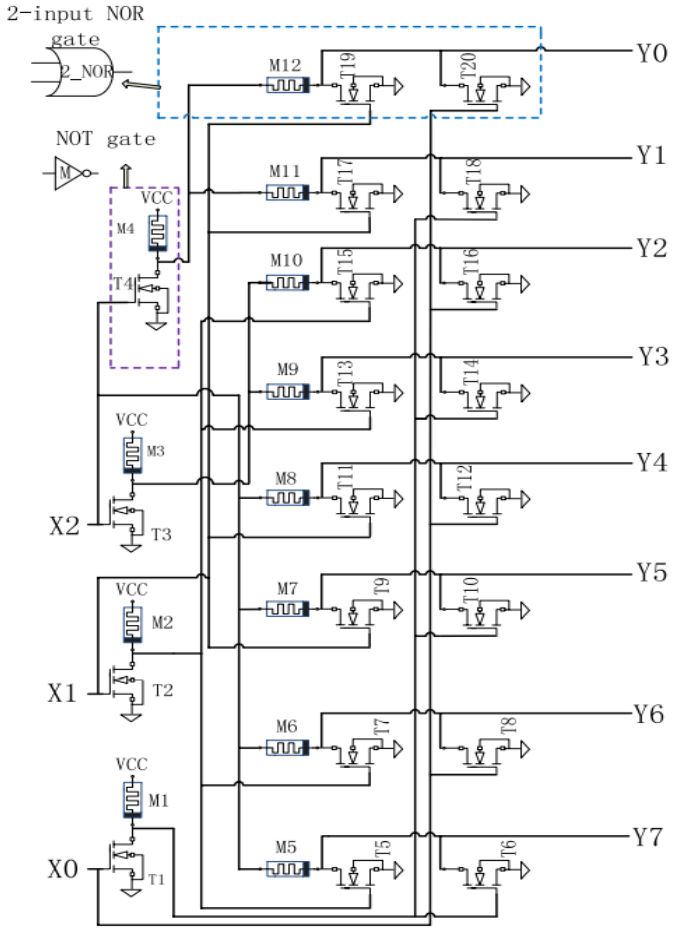


Figure 14: 3-bit Decoder

3.2.3 Multiplexer using Memristor

Multiplexer or more commonly known as Mux, is a combinational circuit, which acts like a switch. This circuit has '2^n' number of input lines, 'n' number of select lines, and 1 line at the output side. The select lines are used to select the input which is passed on to the output line. The block diagram and the truth table of 4x1 mux is shown below:

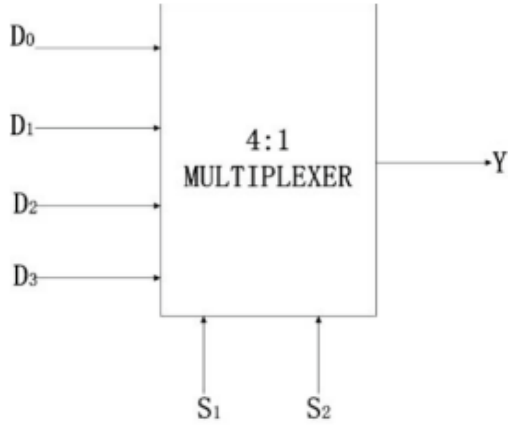


Figure 15: Block Diagram 4x1 multiplexer

Table 3: Truth Table of Multiplexer

INPUT		OUTPUT
S2	S1	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

The output equation can be derived from the truth table. The equation comes out to be:

$$Y = D_0\overline{S_2}\overline{S_1} + D_1\overline{S_2}S_1 + D_2S_2\overline{S_1} + D_3S_2S_1$$

The circuit diagram of the multiplexer developed using memristor is shown below. The combination of memristor3 and transistor3 is used to invert the select line S1, similarly the combination of memristor3 and transistor9 is used to invert the select line signal S2. The combination of memristor5, transistor5 and transistor10 is used as a 3 input NOR gate, where the DC input for memristor5 is replaced with the input signal D3. Thus, we will get the term D3S2S1. Similarly for the other terms we can use the combination of memristors and transistors to develop a NOR gate and obtain that term.

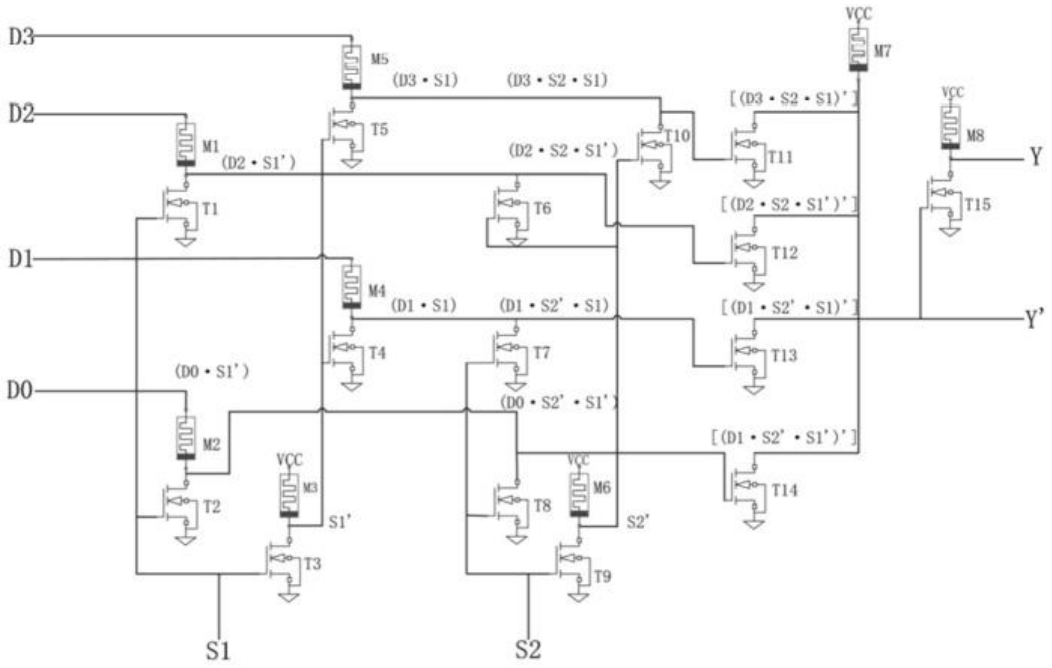


Figure 16: 4x1 Multiplexer [1]

3.2.4 Numerical Comparator using Memristor

A numerical comparator is a circuit, which is used to compare two inputs. The output is obtained as greater than, less than or equal to. The block diagram comparator is shown below along with the truth table:

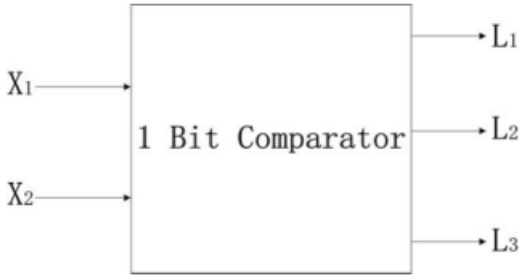


Figure 17: Block Diagram of 1-bit comparator

Table 4: Truth Table of Comparator

X1	X2	L1(X1>X2)	L2(X1<X2)	L3(X1=X2)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

The output equations can be derived from the truth table. The equations come out to be:

$$L_1 = X_1\overline{X_2}$$
$$L_2 = \overline{X_1}X_2$$
$$L_3 = \overline{\overline{X_1}X_2 + X_1\overline{X_2}}$$

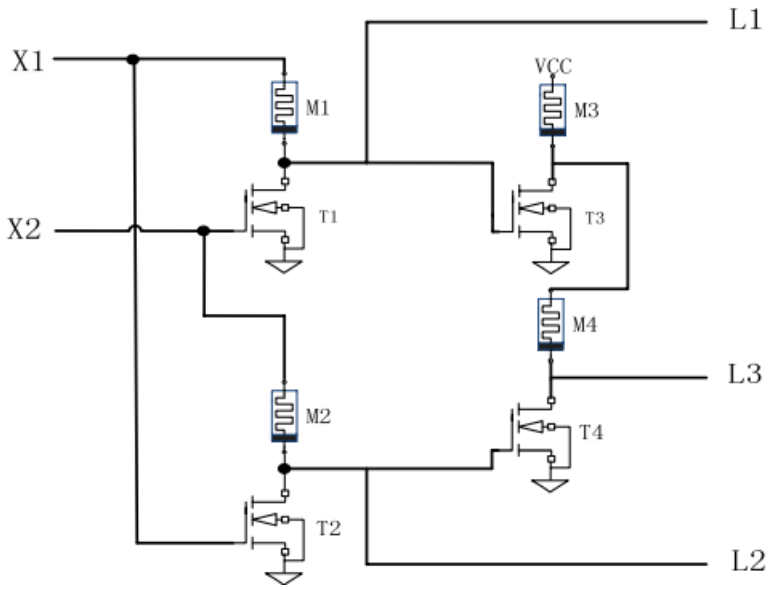


Figure 18: 1-bit Comparator [1]

The results we got from simulating the combinational circuits developed using memristor, were all up to mark. All the circuits were following their truth tables. We will now proceed to develop a SRAM using memristor and will check if we can design that circuit with proper functionality. After that we will compare the power and delay performances of the circuit with conventional 6T SRAM circuit.

CHAPTER 4: SRAM

4.1 Conventional 6T SRAM

Static random-access memory (SRAM) chips use a specific form of memory cell called a typical 6T SRAM cell. It comprises of two access transistors, two pull-up resistors, and six transistors grouped in a cross-coupled design. The state of the cross-coupled inverters serves as a single bit of data stored in the cell.

The access transistors are turned on during read or write operations on the cell to allow current to travel between the cell and the outside circuitry. The data input is stored in one of the inverters during a write operation, and the inverters' states are sensed and amplified to create an output signal during a read operation.

Due to its quick access times and low power consumption, the traditional 6T SRAM cell is utilised in many high-speed applications. Data storage and retrieval mistakes can be brought on by a variety of noise and interference, though, which is a weakness of the system. Numerous adjustments and improvements, such as shrinking the cell size, incorporating redundancy, and utilising more sophisticated circuit designs, have been suggested as solutions to these problems.

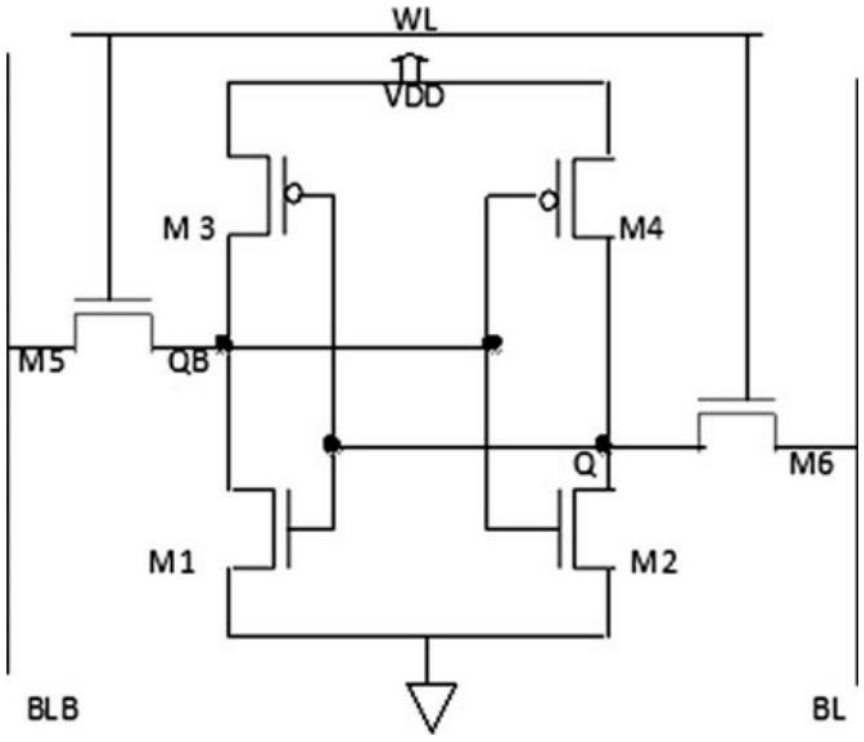


Figure 19: Conventional 6T SRAM [8]

4.2 Memristor Based SRAM

We are now designing the SRAM with the memristor. Memristor will be used in this instance to develop SRAM because we have already used it to develop an inverter. The basic storage component of the SRAM cell in this architecture is created by joining two memristor-based inverters together back-to-back. To control how data enters and leaves the cell, two more transistors are utilized as access transistors. Overall, this design resembles the common 6T SRAM cell, except instead of using PMOS transistors, it uses memristors.

The output waveforms demonstrated that the memristor-based SRAM cell was working. The calculations were carried out for the total power dissipation and delay using the software. The results were then contrasted with the results for the standard SRAM cell.

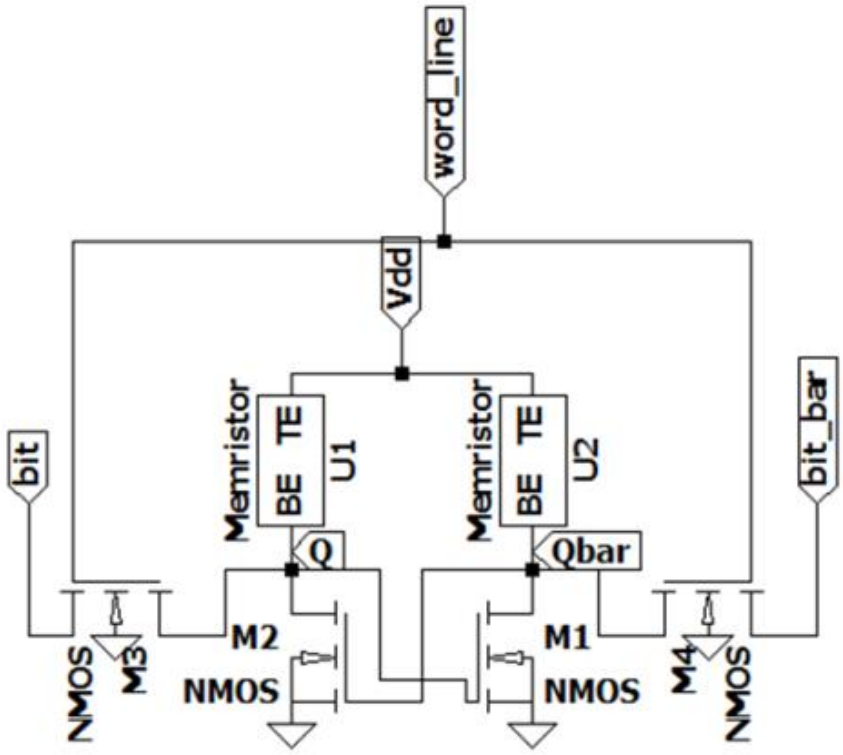


Figure 20: Memristor based SRAM [7]

Calculations were performed for power and delay for both the circuits. It was found that power consumption of memristor based SRAM was higher when compared to the conventional 6T SRAM.

There are different types of power reduction techniques which can be applied to the newly designed circuits so that the power consumption can be reduced. One such technique which helps in decreasing the power consumption of the circuit is MTCMOS technique. This

technique was used in the new circuit and the results were obtained, which is explained in the following pages.

Table 5: Comparison Table 1

Circuit	Power	Delay
Conventional 6T SRAM	355.58nW	15.06ps
Memristor based SRAM	92.192uW	8.53ps

4.3 MTCMOS Technique

Digital circuits employ the MTCMOS (Multi-Threshold CMOS) technology to save power consumption by selectively turning off portions of the circuit when they are not in use. Utilizing transistors with various threshold voltages in various circuit components is the fundamental concept behind MTCMOS. Higher threshold voltage transistors require more voltage to turn on, but they also use less power once they are operating. Power consumption can be decreased without sacrificing performance by utilizing high-threshold transistors in circuit components that are seldom used, like memory cells, and low-threshold transistors in circuit components that are regularly used, like logic gates.

The way MTCMOS operates is by segmenting the circuit into multiple power domains that can each be individually regulated. It is possible to cut off a domain's power supply while it is not in use, thereby shutting down that section of the circuit. The power supply can be restarted, and the circuit can start up once more when the domain is required. However, MTCMOS also makes the design process more difficult and necessitates close attention to timing and power sequencing concerns.

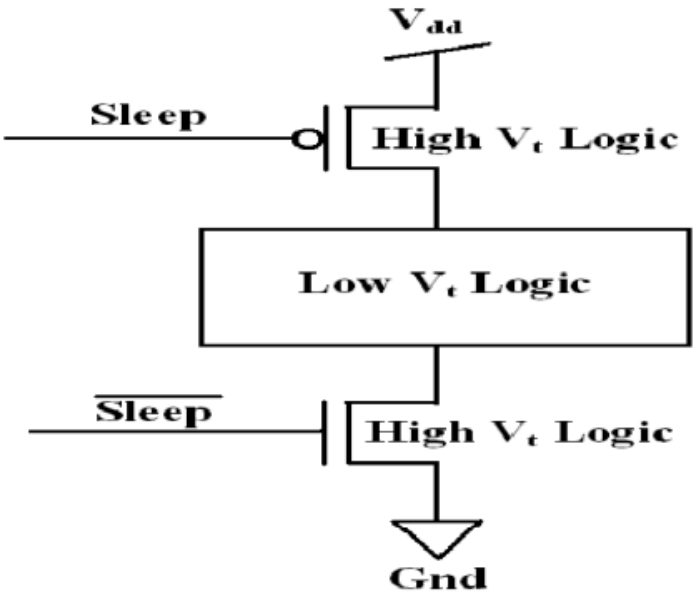


Figure 21: MTCMOS Technique

4.4 Memristor based SRAM using MTCMOS Technique

The circuit was developed using two high threshold voltage transistors, which are standby transistors, and the already designed memristor based SRAM. The circuit developed is shown below.

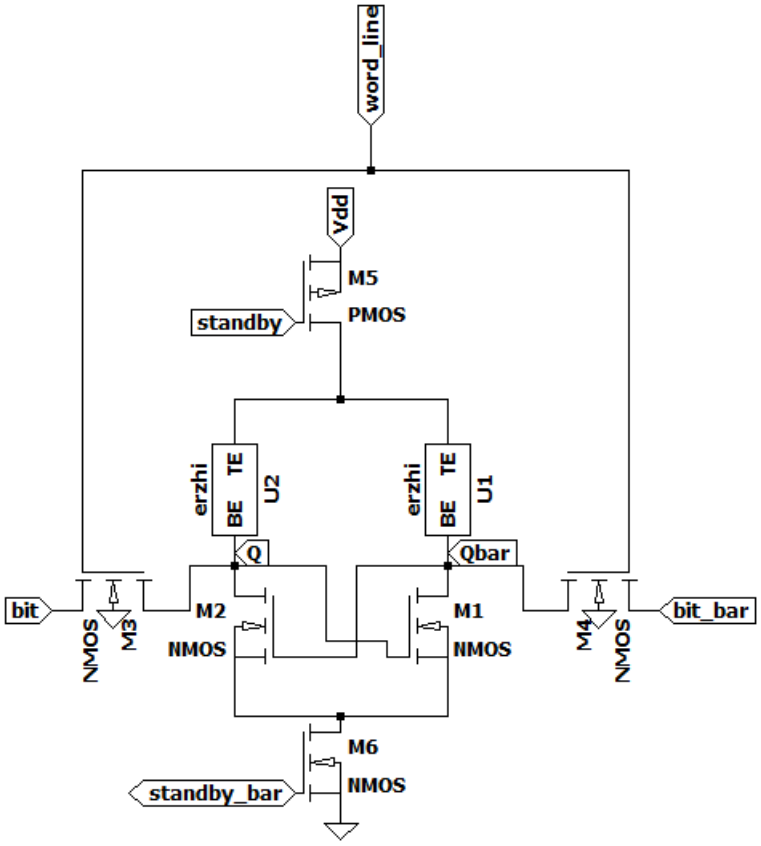


Figure 22: Memristor based SRAM using MTCMOS Technique

After using the MTCMOS technique the power consumption of the MTCMOS SRAM cell reduced and it was found to be below the power consumption of conventional 6T SRAM cell.

Table 6: Comparison Table 2

Circuit	Power
Conventional 6T SRAM	355.58nW
Memristor based SRAM	92.192uW
Memristor based SRAM using MTCMOS Technique	290.98nW

CHAPTER 5: SCHEMATICS AND SIMULATIONS

4.1 NOT gate

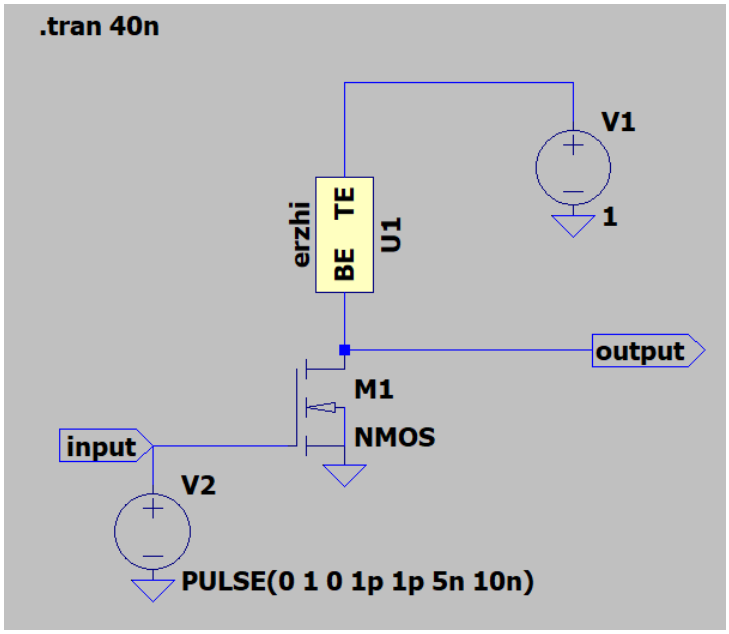


Figure 23: Schematic of NOT gates

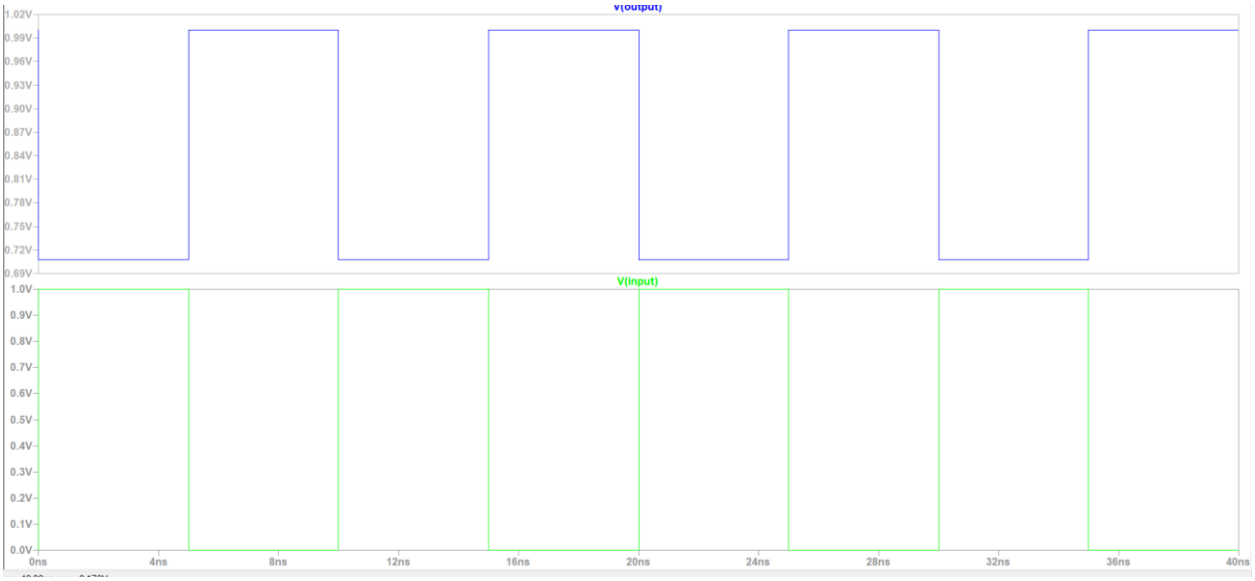


Figure 24: Simulation results of NOT gate

4.2 A and (NOTB)

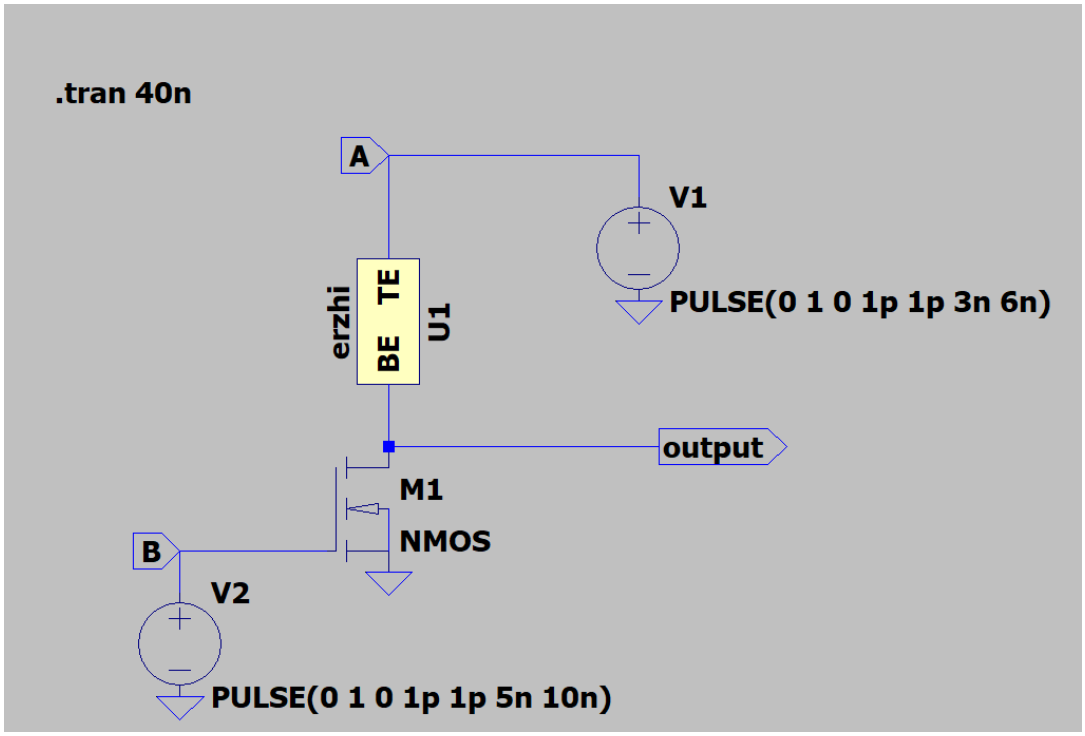


Figure 25: Schematic of A and (NOTB)

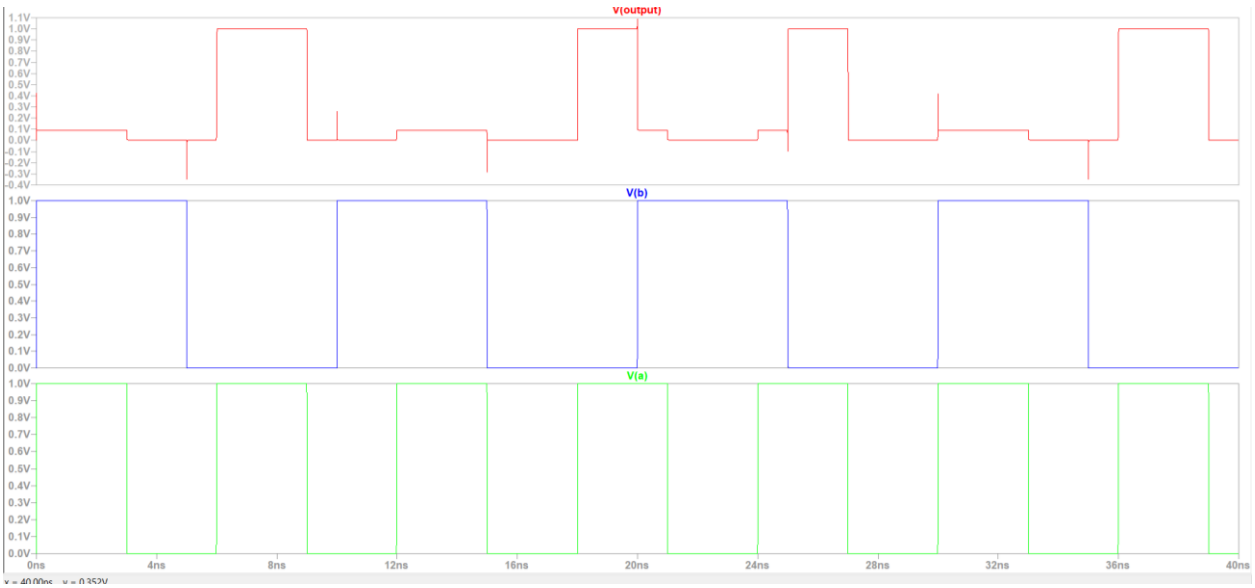


Figure 26: Simulation results for A and (NOTB)

4.3 NOR gate

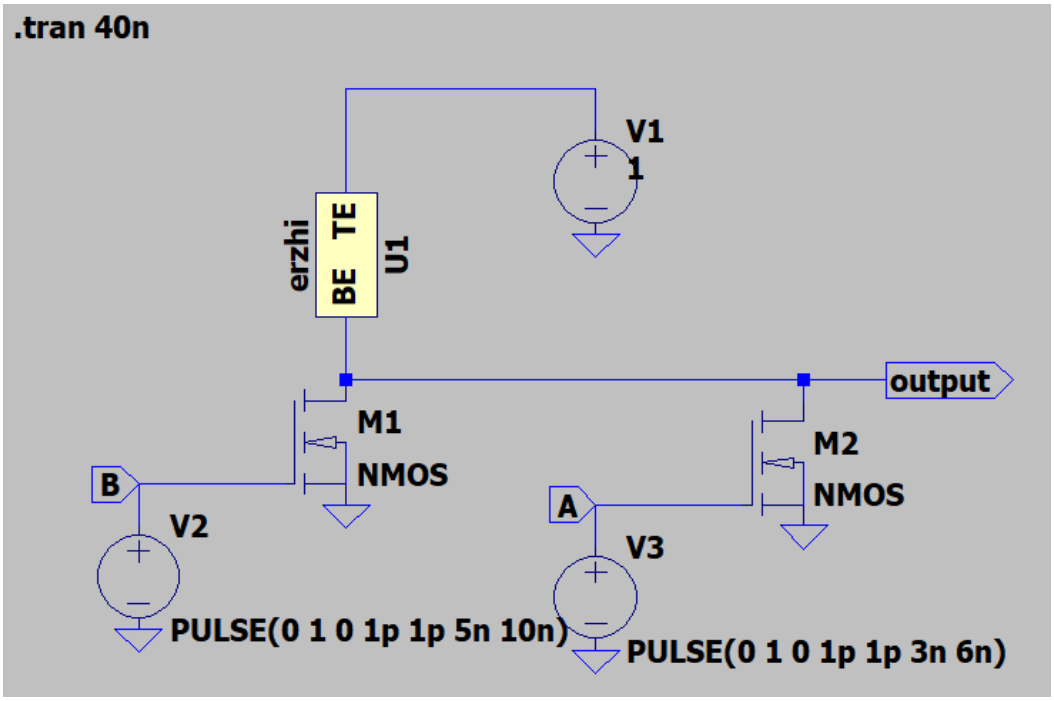


Figure 27: Schematic of NOR gate

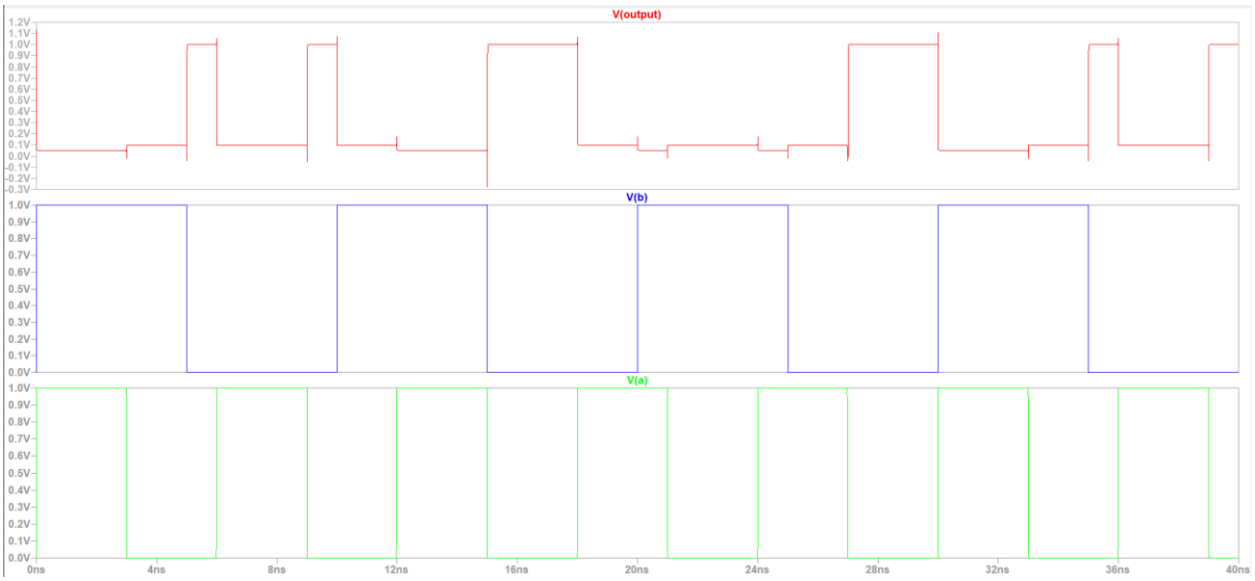


Figure 28: Simulation results of NOR gate

4.4 Encoder

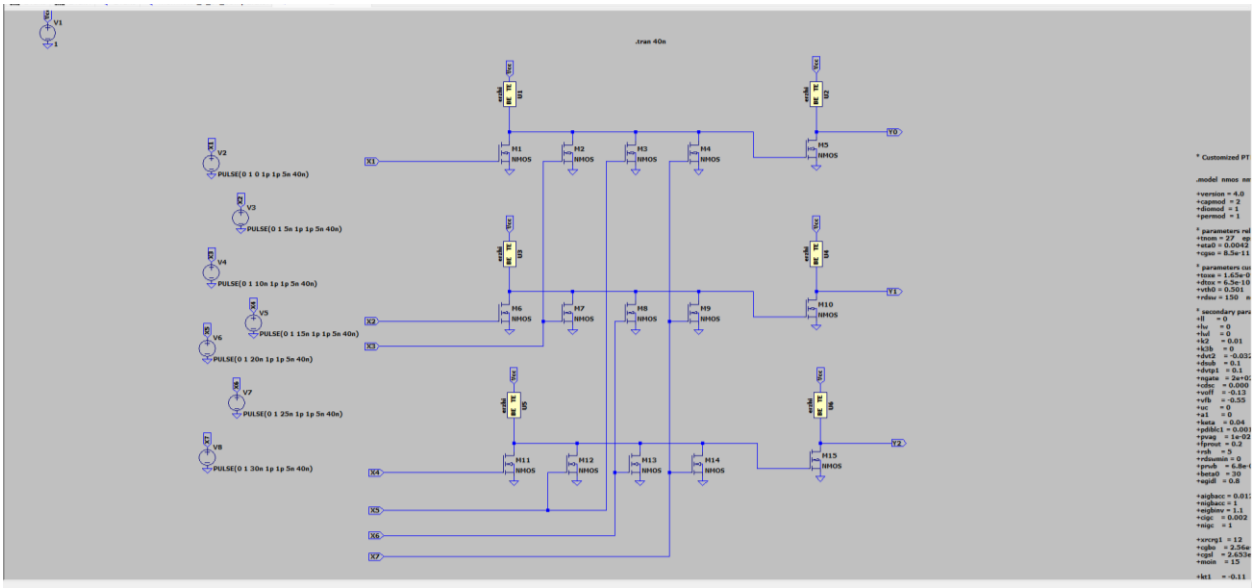


Figure 29: Schematic of Encoder

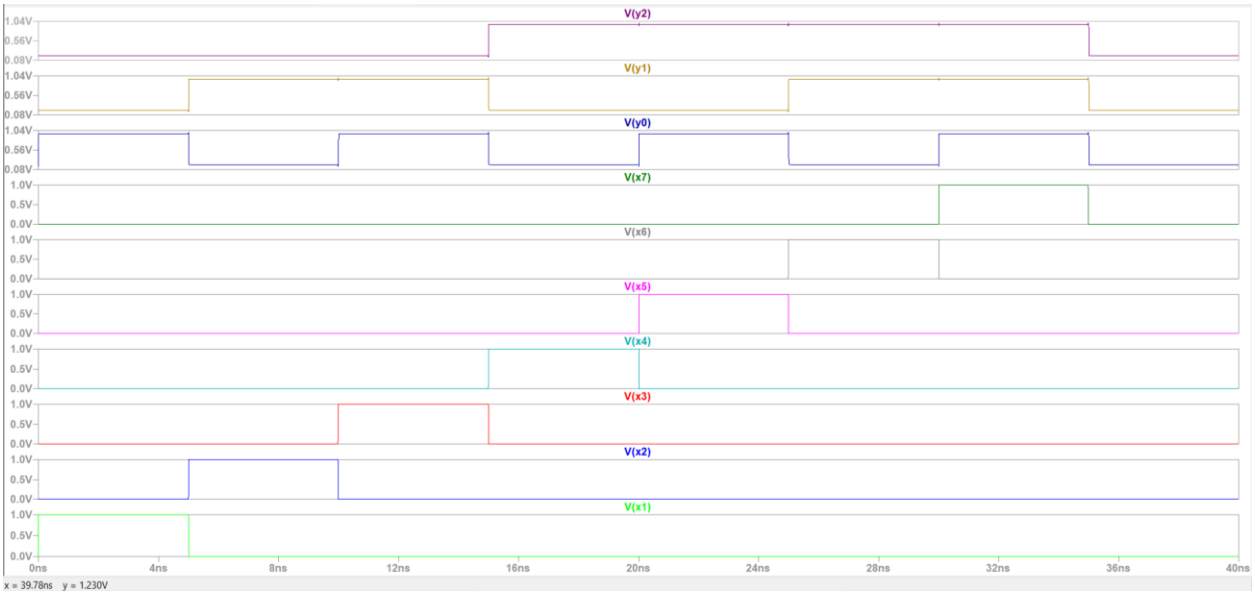


Figure 30: Simulation results of Encoder

4.5 Decoder

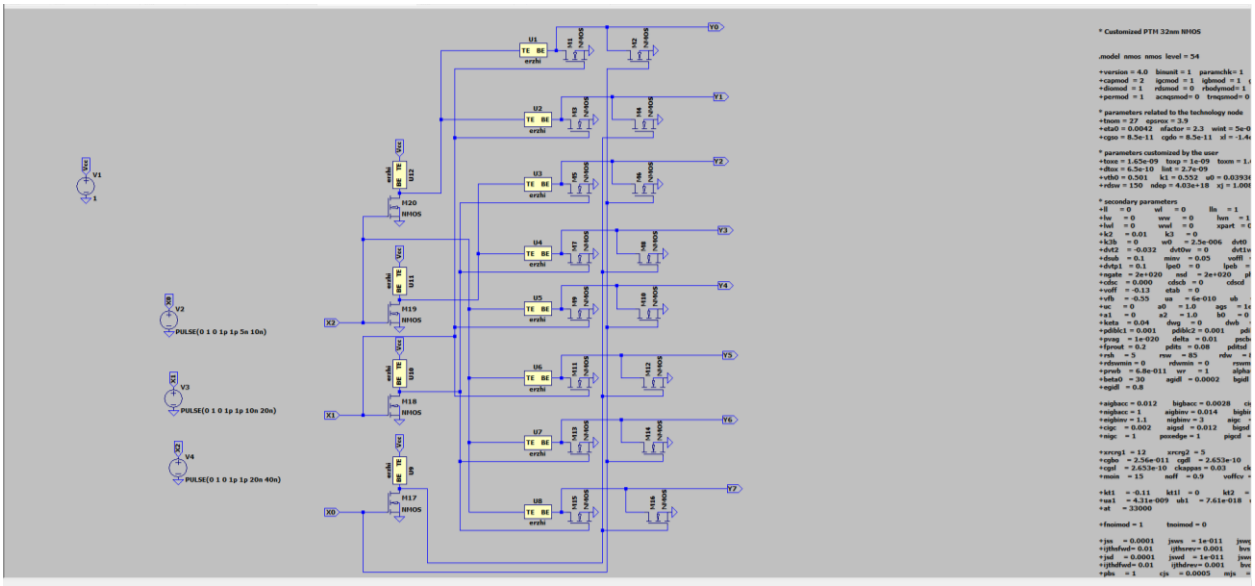


Figure 31: Schematic of Decoder

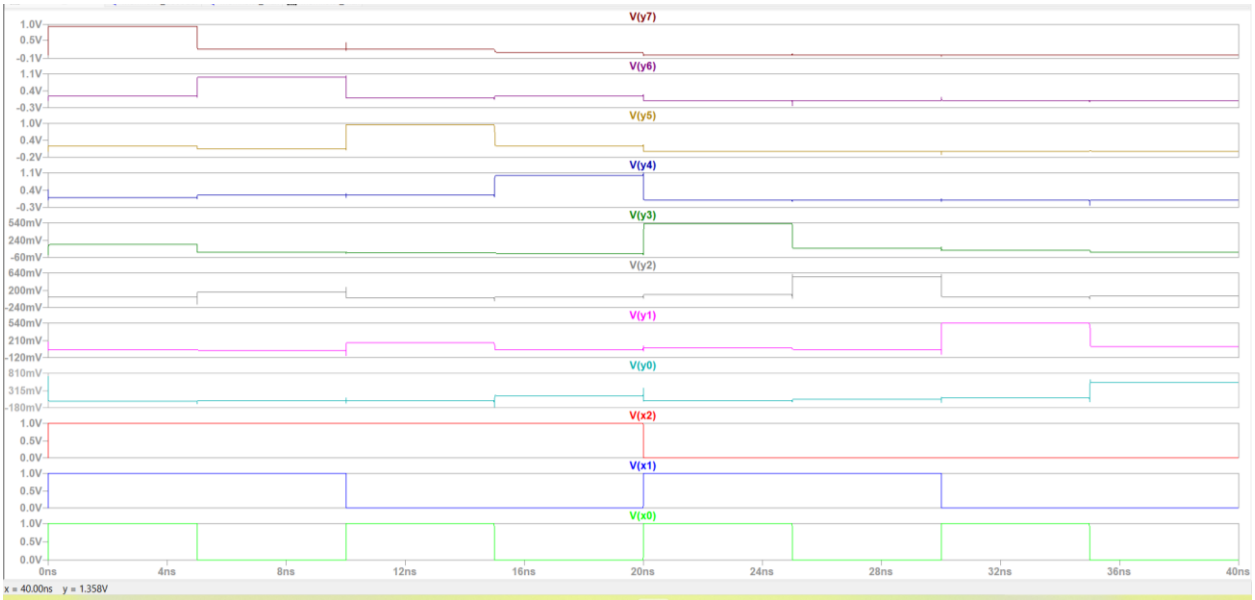


Figure 32: Simulation results of Decoder

4.6 Multiplexer

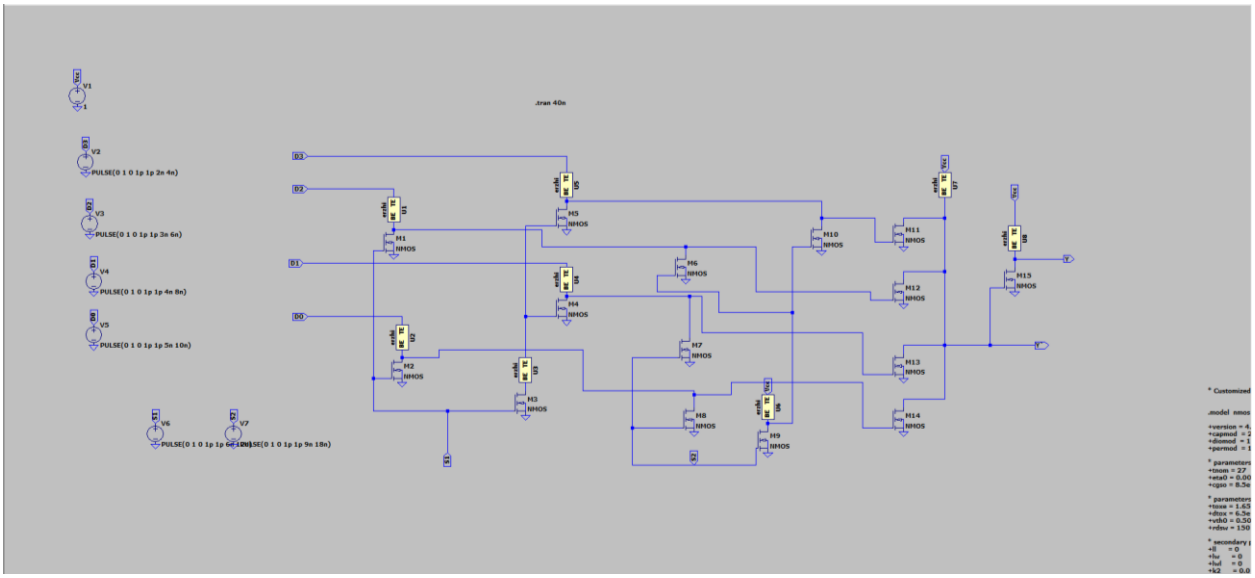


Figure 33: Schematic of Multiplexer

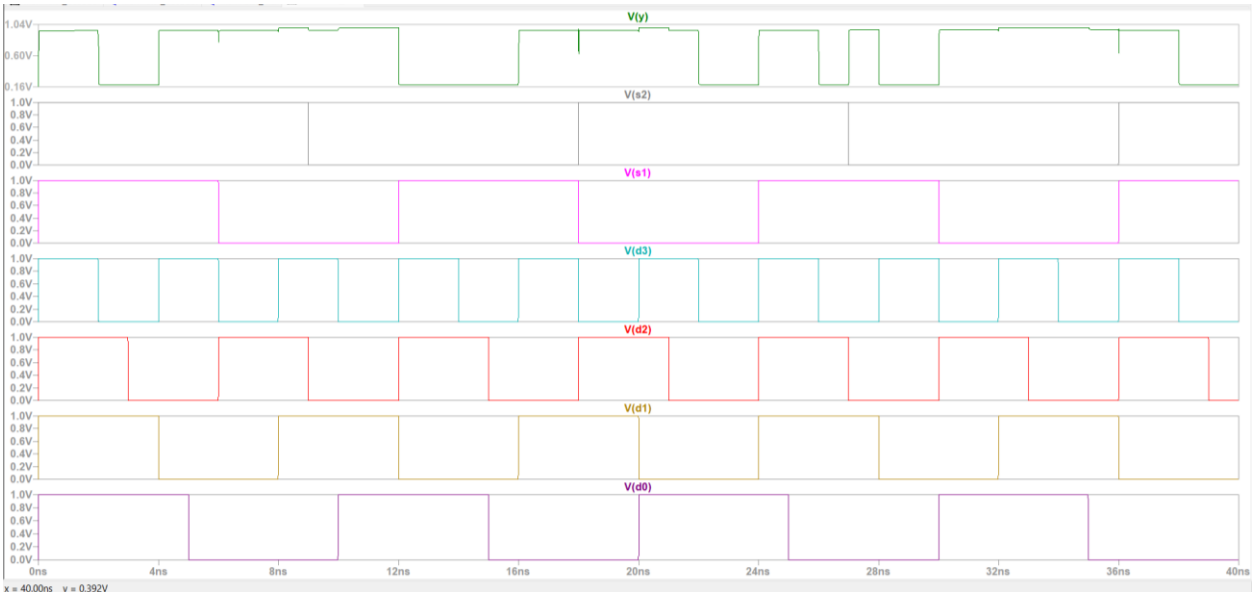


Figure 34: Simulation results of Multiplexer

4.7 1-bit comparator

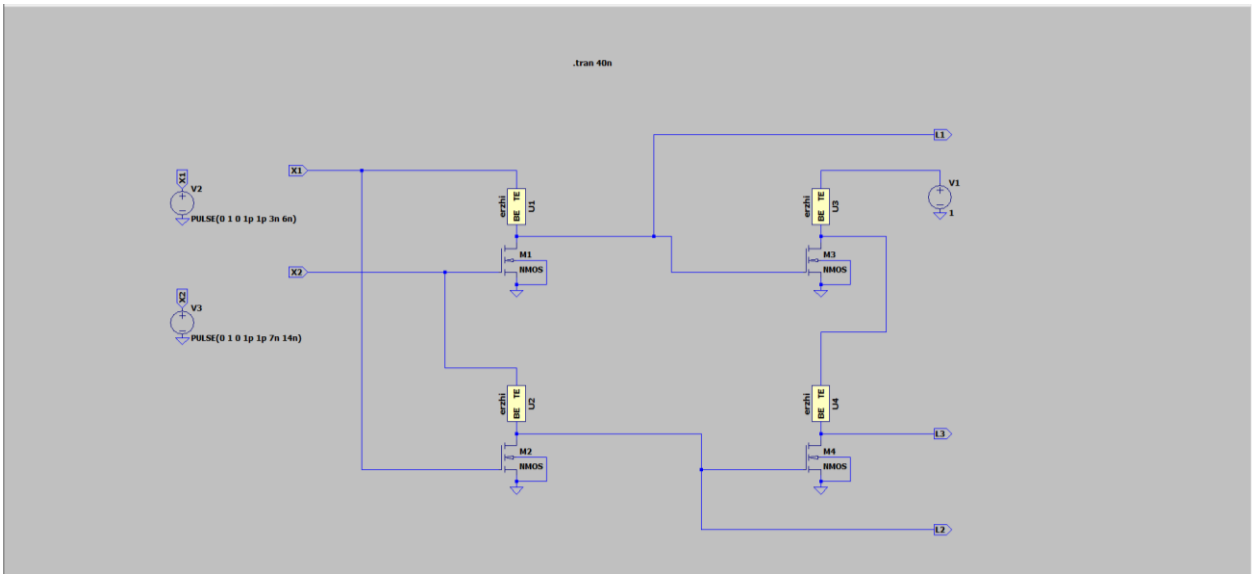


Figure 35: Schematic of 1-bit comparator

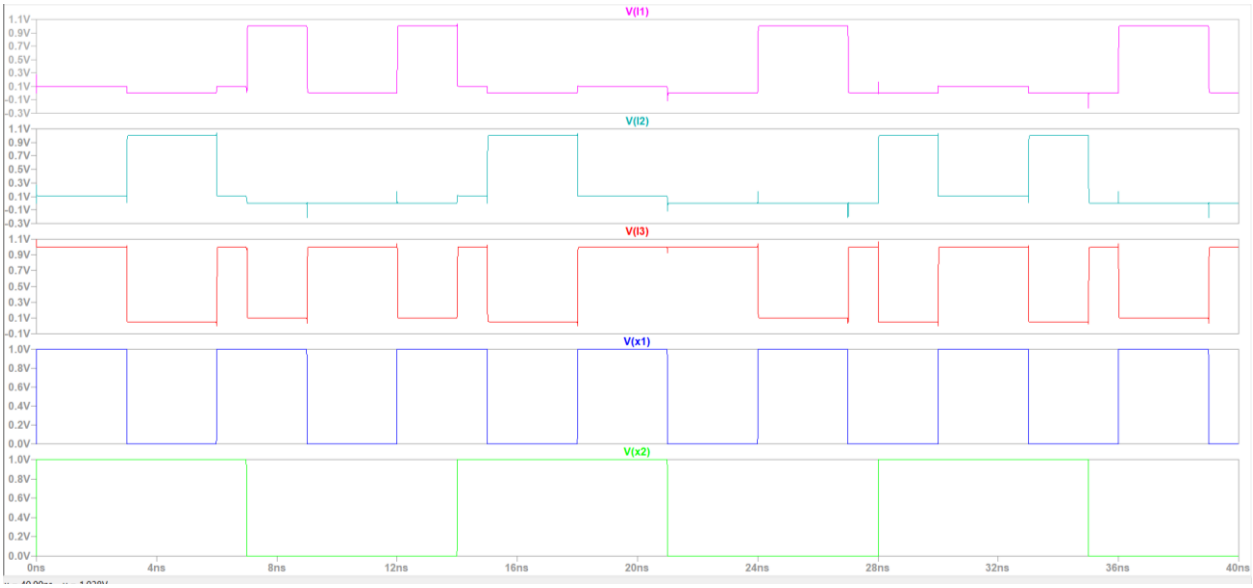


Figure 36: Simulation results of 1-bit comparator

4.8 Conventional 6T SRAM

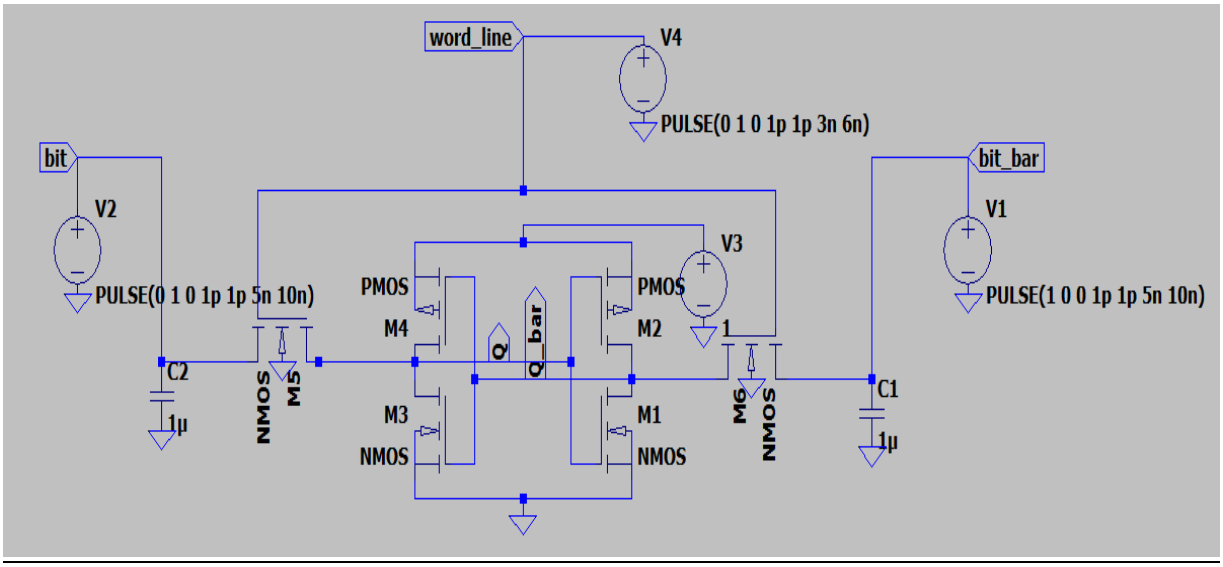


Figure 37: Schematic of conventional 6T SRAM

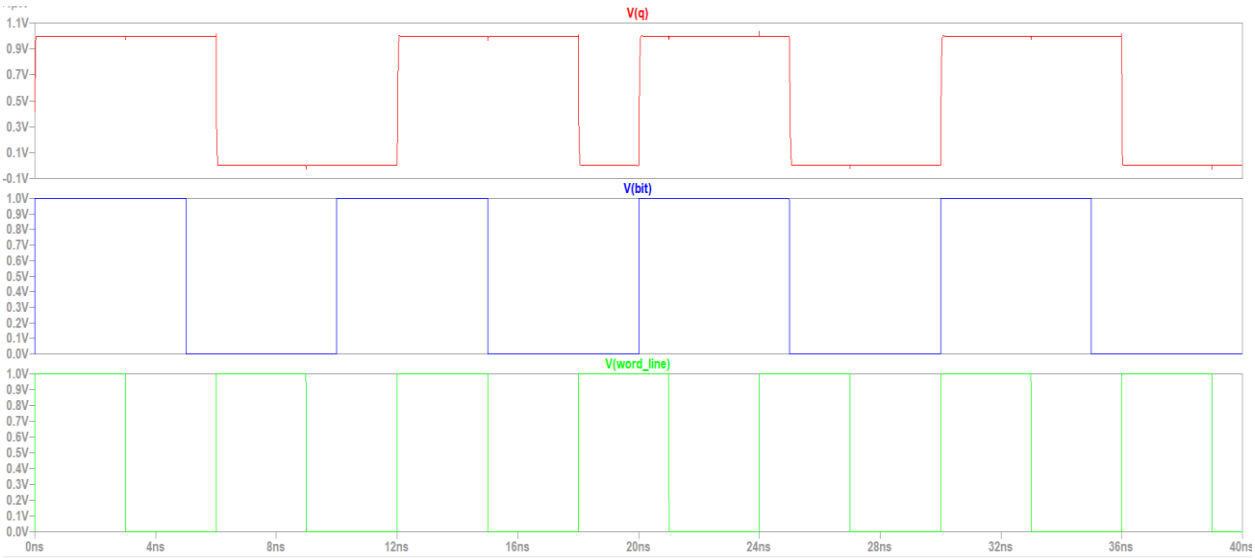


Figure 38: Simulation results of conventional 6T SRAM

4.9 Memristor based SRAM

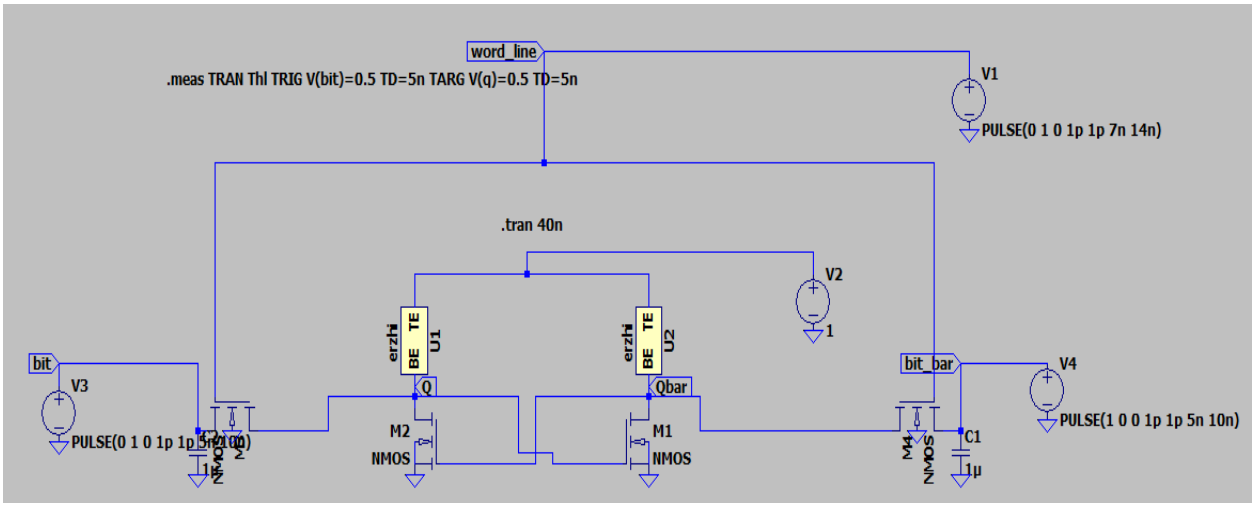


Figure 39: Schematic of Memristor based SRAM

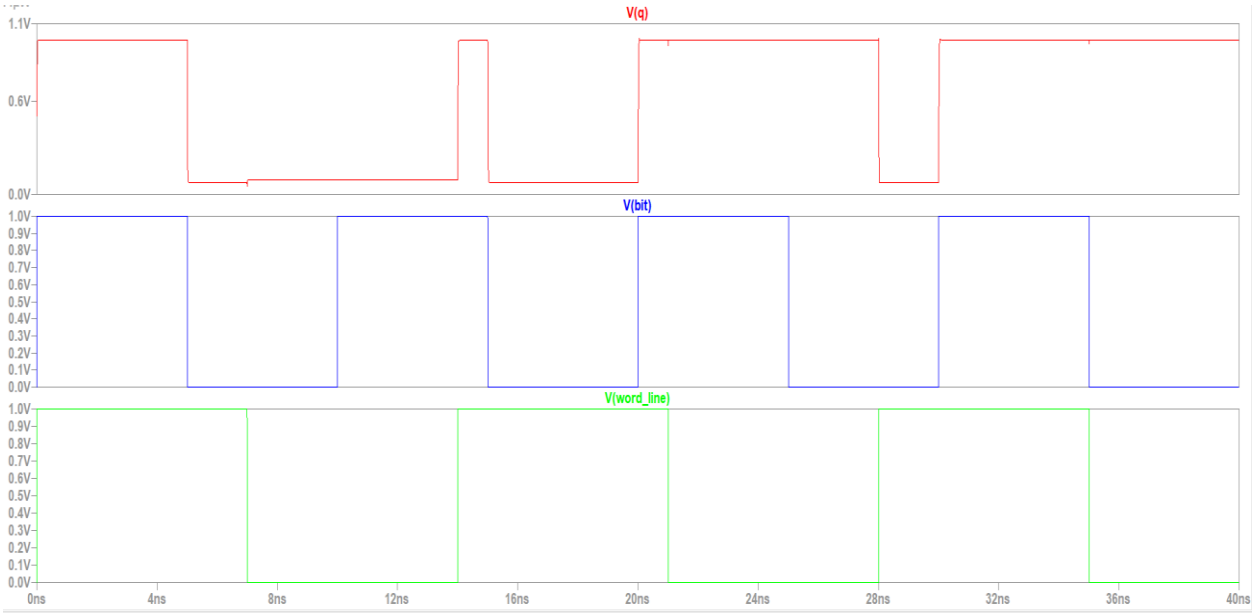


Figure 40: Simulation results of memristor based SRAM

4.10 Memristor based SRAM using MTCMOS Technique

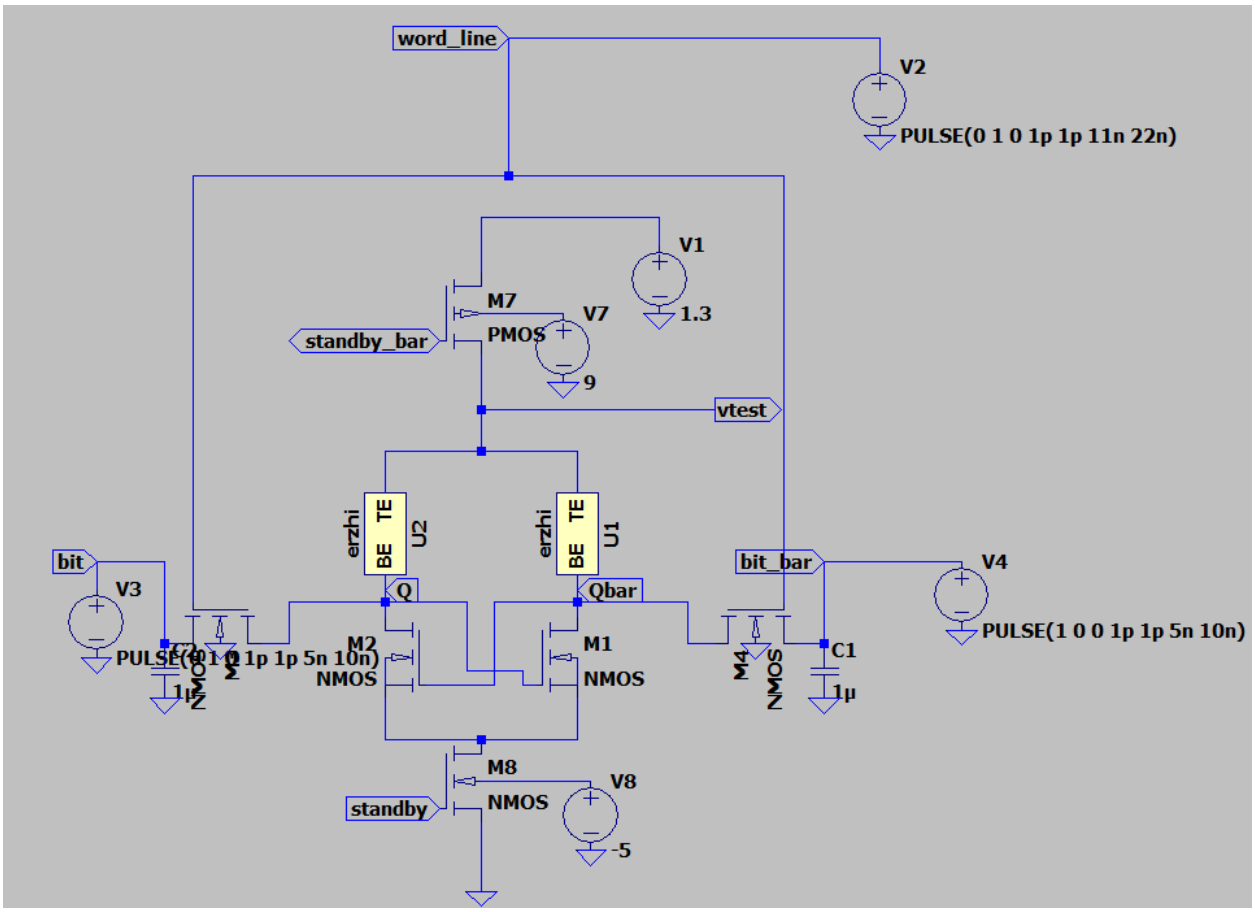


Figure 41: Schematic of Memristor based SRAM using MTCMOS Technique

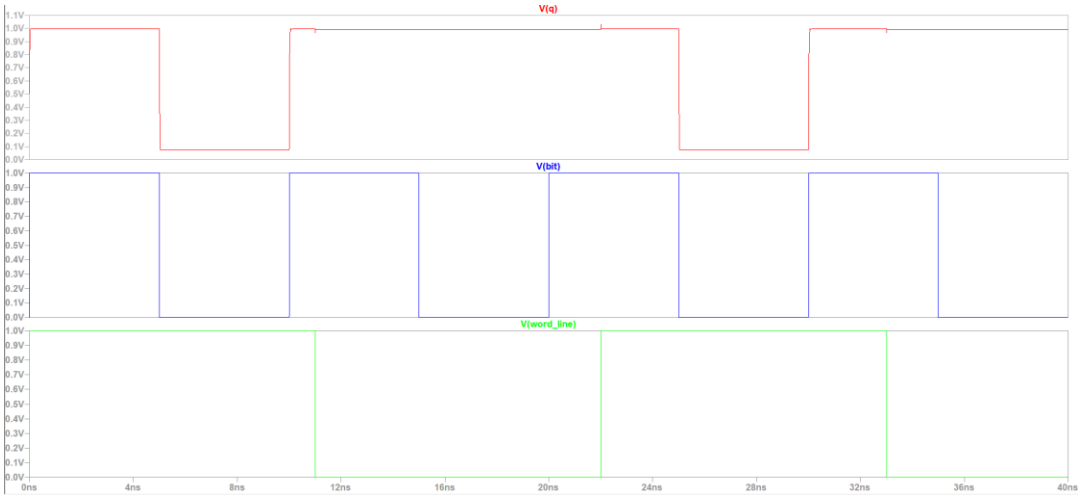
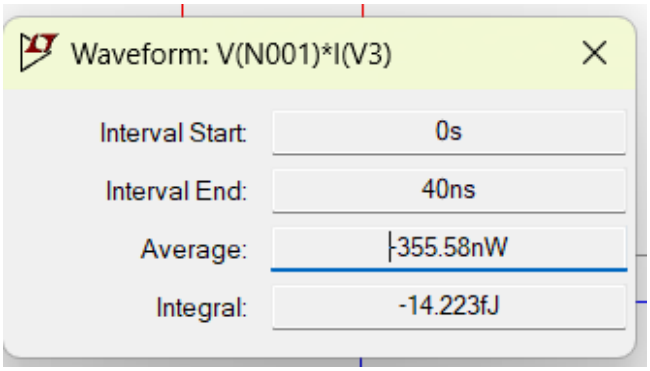


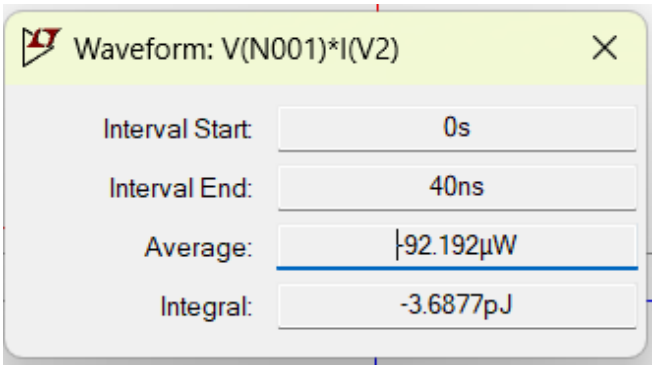
Figure 42: Simulation results for Memristor based SRAM using MTCMOS Technique

4.11 Power Comparison

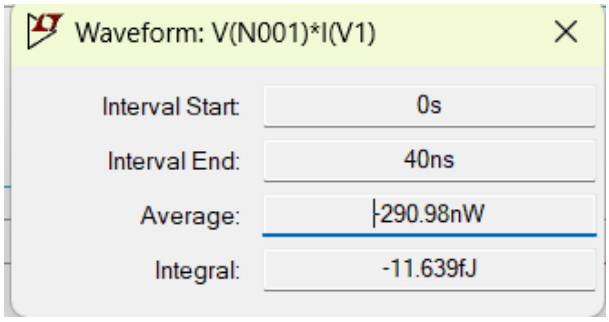
Conventional 6T SRAM



Memristor based SRAM



Memristor based SRAM using MTCMOS Technique



CHAPTER 6: CONCLUSION

Memristor is a device which is having a dynamic resistance. The value of resistance depends upon the voltage applied across the terminals. This device can be seen as a replacement of transistors in designing of circuits. The fabrication of this device is very easy when compared with the MOS transistor. Also, it gives better delay results when compared to the conventional CMOS circuits. Different combinational circuits were developed to check the proper functioning of the device. After that, the device was used to develop SRAM cell. A comparison was done between the developed device and the conventional six transistor-based SRAM. It was found that newly developed circuit using memristor was having high power consumption. To reduce this, MTCMOS technique was used. The technique helped in decreasing the power consumption in considerable amount. So with usage of power reduction techniques in vlsi, we can develop circuits with memristors which can give comparable results to the conventional circuits.

REFERENCES

[1] Liu, G., Shen, S., Jin, P. et al. Design of Memristor-Based Combinational Logic Circuits. Circuits Syst Signal Process 40, 5825–5846 (2021). https://doi.org/10.1007/s00034-021-01770-1

[2] Wang, X., Jin, C., Eshraghian, J.K. et al. A Behavioral SPICE Model of a Binarized Memristor for Digital Logic Implementation. Circuits Syst Signal Process 40, 2682–2693 (2021). https://doi.org/10.1007/s00034-020-01611-7

[3] Yakopcic, C., Taha, T.M., Subramanyam, G., Pino, R.E. (2012). Memristor SPICE Modeling. In: Kozma, R., Pino, R., Pazienza, G. (eds) Advances in Neuromorphic Memristor Science and Applications. Springer Series in Cognitive and Neural Systems, vol 4. Springer, Dordrecht. https://doi.org/10.1007/978-94-007-4491-2_12

[4] Kyoungrok Cho, Sang-Jin Lee, Kamran Eshraghian, Memristor-CMOS logic and digital computational components, Microelectronics Journal, Volume 46, Issue 3, 2015, Pages 214-220, ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2014.12.006.

[5] Agarwal, T. (2014, June 15). Buy Electronics & Electrical Projects in India. https://www.edgefx.in/memristor-know-memristor-technology/

[6] Memristor.AI. (n.d.). https://memristor.ai/

[7] Jeffry Louis, V., Gopal Pandey, J. (2019). A Novel Design of SRAM Using Memristors at 45 nm Technology. In: Sengupta, A., Dasgupta, S., Singh, V., Sharma, R., Kumar Vishvakarma, S. (eds) VLSI Design and Test. VDAT 2019. Communications in Computer and Information Science, vol 1066. Springer, Singapore. https://doi.org/10.1007/978-981-32-9767-8_48

[8] Tripathi, T., Chauhan, D.S., Singh, S.K., Singh, S.V. (2017). Implementation of Low-Power 6T SRAM Cell Using MTCMOS Technique. In: Bhatia, S., Mishra, K., Tiwari, S., Singh, V. (eds) Advances in Computer and Computational Sciences. Advances in Intelligent Systems and Computing, vol 553. Springer, Singapore. https://doi.org/10.1007/978-981-10-3770-2_44

[9] S. Hemantha, A. Dhawan and H. Kar, "Multi-threshold CMOS design for low power digital circuits," TENCON 2008 - 2008 IEEE Region 10 Conference, Hyderabad, India, 2008, pp. 1-5, doi: 10.1109/TENCON.2008.4766689.

[10] V. S. Baghel and S. Akashe, "Low Power Memristor Based 7T SRAM Using MTCMOS Technique," 2015 Fifth International Conference on Advanced Computing & Communication Technologies, Haryana, India, 2015, pp. 222-226, doi: 10.1109/ACCT.2015.58.