IMPLEMENTATION OF NANOWIRE RECONFIGURABLE FET AS A BIOSENSOR WITH IMPROVED SENSITIVITY

MAJOR PROJECT

REPORT IN THE

FULFILLMENT OF REWARD

FOR DEGREE

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEMS

Submitted by

Divyansh Singh (2K21/VLS/06)

Under supervision of

Mr. Anurag Chauhan (Assistant Professor)

Dr. Sumit Kale (Assistant Professor)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)Bawana Road,
Rohini, Delhi- 110042

CANDIDATE'S DECLARATION

I, Divyansh Singh 2K21/VLS/06, student of M.Tech (VLSI Design and EMBEDDED SYSTEM), hereby declare that the Major Project 1 report "Implementation of Nanowire Reconfigurable FET as a biosensor with improved sensitivity**",** which is submitted by me, to the department of Electronics and Communication Engineering, DELHI TECHNOLOGICAL UNIVERSITY, DELHI in partial fulfillment of the requirement for degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, fellowship or other similar title or recognition.

Divyansh Singh(2K21/VLS/06)
Date:30-05-2023 M.Tech (VLSI Design and Embedded System)
Place: Delhi Department of Electronics & Communication Engineering

CERTIFICATE

I hereby certify that the Major Project 1 report titled "Implementation of Nanowire Reconfigurable FET as a biosensor with improved sensitivity", which is submitted by Divyansh Singh (2K21/VLS/06) to the department of Electronics and Communication Engineering, Delhi Technological University, Delhi in the partial fulfillment of the requirement for degree of Master of Technology, is record work of the report work carried out by student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Prof. O P Verma
(Head of Department)

Date:30-05-2023
Place: Delhi

Dr. Sumit Kale
(Assistant Professor),
Supervisor

Mr. Anurag Chauhan
(Assistant Professor),
Supervisor
Department of Electronics and Communication Engineering
Delhi Technological University

ABSTRACT

Reconfigurable FET can be used as both p type and n type as per the requirement by applying voltage to the electrodes accordingly. Nanowire RFET has got a structure with two gates, one acting for the biasing and the other for current control (that is ON or OFF). The structure is like Nanowire heterostructure. The technique used here is dielectric modulation and based on that the variation in threshold voltage related sensitivity. These find major applications in Programmable Logic Arrays since can be programmed as p type or n type. The RFET used in this project has been developed as a biosensor by creating a cavity and then filling it with neutral biomolecules, whose permittivity is varied. The simulated of the structure has been done and the sensitivity has been calculated using Silvaco TCAD tool.

ACKNOWLEDGEMENT

I would like to express my deep sense of gratitude to my highly respected and esteemed guides, Dr. Sumit Kale and Mr. Anurag Chauhan for suggesting the topic of my Major project 1 and for giving me complete freedom and flexibility to work on this topic. They have been very encouraging and motivating and the intensity of encouragement has always increased with time. Without their constant support and guidance, I would not have been able to complete this work. I extend my sincere thanks to all my friends who have patiently helped me directly or indirectly in accomplishing this work successfully.

Divyansh Singh(2K21/VLS/06)
M.Tech (VLSI Design and EMBEDDED SYSTEM)
Department of Electronics & Communication Engineering

CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

1.1 Introduction to FET

A crucial electrical component widely used in the electronics industry is the field – effect transistor, or FET.

The FET is an ubiquitous discrete electronic device found in circuits for RF technologies, power management, electronic switching, and basic amplification.

Nevertheless, integrated circuits are where the field effect transistors, or FET, is most often used. FET circuits use a lot lesser power than IC that uses the bipolar transistor technology in this application. The extremely huge size integrated circuits can function as a result. The power consumed will be order of magnitude higher and the power produced would be far too big to dissipate from IC if bipolar technology were utilized.

The field-effect transistor uses an electric field to change the topology and subsequently the conductivity of free carriers in a semiconductor. Such FET transistors also are known as unipolar transistors since they carry out a single-carrier kind of operation. High input impedance characterizes all FET configurations. Since the input current controls the conductance of a non-FET transistor, the input impedance is minimal. The conductivity is controlled by a voltage placed at the terminals of a field-effect transistor. When a voltage is applied to gate, an electric field is created inside the device that attracts and repels charges that are conveyed between the two terminals. The density of such charge carriers also has an impact on conductivity.

FETs are classified majorly as:

a. **Junction FET:**

A reverse bias diode junction serves as the gate contact in a junc. FET, or JFET. The channel, which may either be it of N type or P type, constitutes the structure. Therefore, the channel is constructed using semiconductor diodes such that the voltage on diode has impact on the channel.

Just the diodes reverse current may flow between them when it is operating in reverse bias, essentially insulating it from channel. The JFET, that was formed initially, is the very basic sort of FET. However, it continuously offers top notch service in many technology fields.

The two types of JFET are shown in the figure.

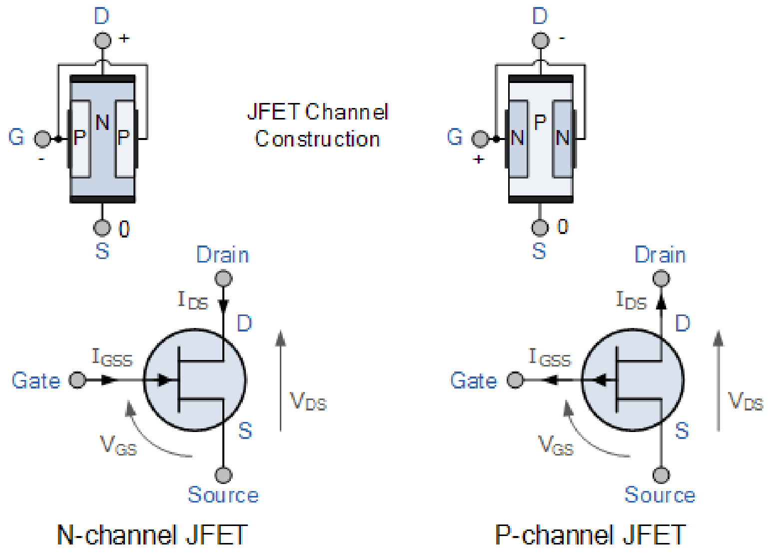


Fig 1.1: N and P types of JFET with their symbols

The characteristics of JFET are as follows:

1. Drain or Output Characteristics.

The drain characteristics or output characteristics is the line drawn between the drain current Id and the drain to source voltage VDS with the gate-to-source voltage VGS serving as the parameter. This trait is comparable to the collector trait of a Bipolar Junction T:

i. Drain Feature With gate- shorted

Figure shows the circuit diagram for figuring out an N-channel JFET's drain characteristic with a shorted-gate. and another graphic illustrates the gate shorted with drain feature.

Initially, even though the channel is completely open, there is no flow of current when the drain to source voltage Vds is 0 because there is no attractive potential at the drain. This results in a drain current Ip of 0. The N-type bar functions as a straightforward semiconductor resistor for low applied voltage Vna, and there is linear rise of drain current with Vds till the knee point. The channel ohmic zone is the area of the curve where the FET acts like a typical resistor.

The electrical voltage lowering across the source and the channel area reverse-biases the gate junction as the drain current ID increases. The gate junction's reverse-biasing is not constant throughout. Ultimately, channel gets pinched off at a voltage called Vds. With an increase in Vds, the current through the drain no longer rises. It gets closer to a steady saturation value. The pinch-off voltage is the level of the voltage Vds when the channel gets pinched off (all of the channel's free charges are eliminated). The point of the curve when Id starts to become unvaried and reach a constant value is known as the pinch-off voltage or simply Vp. The Id increases with a rise in voltage Vds obeying a reverse square law from the knee point to pinch-off point.

The pinch-off zone is the area of the characteristic where the drain current ID is relatively constant. The saturation area or amplifier region are other names for it. Since the drain current (or simply output current) is nearly constant in the area, the JFET functions as a CCD (constant current device). When employed as an amplifier, it is the JFET's typical working zone. The Id saturation current, abbreviated Idss, is the drain current or simply Id in the pinch-off zone where VGS = 0.

It should be taken into account that the drain current is kept almost constant in the pinch-off and start of saturation region by the channel resistance increasing proportionally to the gain in VDS, and the reverse bias needed by the gate-channel junction is entirely provided by the decrease in voltage across the channel resistance caused by the flow of Ids and not by external bias because VGS = 0.

The equation for Shockley's drain current in the pinch-off area is presented where Idss is the current through drain when the gate is shorted to the source, VGS (0FF) is the gate-source cut-off voltage, and VGS is the drain current at a certain gate-source voltage.

When the drain-source voltage, Vds, is raised constantly, the gate-channel junction eventually reaches a point of failure. The current is now quickly increasing. and it's possible to damage the JFET. This occurs as a result of an avalanche effect caused by the high-velocity acceleration of the charge carriers that make up the current in saturation region at the gate channel junction.

2. JFET Transfer Characteristic

By matching the drain to source voltage, VDS, which is constant and measuring the drain current, ID, for different values of the gate-source voltage, VGS, one can experimentally estimate the transfer characteristics for a JFET. It is comparable to a transistor's or a vacuum tube's transconductance property. It has been noted that

(i) Drain current drops as less than zero gate-source bias increases.

When VGS = 0, the drain current ID = IDSS.

When VGS = VD, the drain current, ID, is zero.

By recording and graphing the values of the drain current, Id corresponding to different values of the gate-source voltages, VGS for a constant drain-source voltage, one can also deduce the transfer characteristic from the drain characteristic.

It should be pointed out that P-channel JFET functions similarly to and has comparable properties to an N-channel JFET, with the exception that the polarities of the VGS and VDS are flipped and the channel particles are holes rather than electrons.

Advantages and Disadvantages of JFET:

JFETs combine a number of the advantages of both traditional bipolar transistors as well as vacuum tubes.

The following list includes a few of these:

1. It is a unipolar (one kind of carrier) device since it only operates with the flow of the majority of carriers. In contrast, both majority as well as minority carriers participate in conduction in a typical transistor, which is why it is frequently referred to as a "bipolar transistor." One further illustration of a unipolar device is the vacuum tube.

2. It is easier to produce, smaller in size, more durable, has a longer lifespan, and is more effective. In IC form, fabrication is easier and requires less space.

3. It contains a reverse biassed input circuit (gate to source), which results in a high standard of separation between input and the output circuits, and an input impedance that is high (of the order of 100 M Q). However, a typical transistor has a forward biassed input circuit, which results in a low input impedance for a typical transistor.

4. It functions similarly to a vacuum tube in that the input voltage regulates the output current and the control grid (which corresponds to the gate in JFET) delivers a very little current due to the reverse biassed gate. Due to the fact that input current determines output current, a JFET is fundamentally a device driven by voltage whereas a regular transistor is a device operated by current.

5. A JFET employs voltage on the gate terminal to control the drain current, which is the current between the drain and source, as opposed to an ordinary transistor, which controls the drain current by a current flowing into its base. Therefore, the transconductance (also known as the ratio of the drain current to the gate-source voltage) is used to describe the gain of JFETs as opposed to conventional transistors.

6. Unlike a regular transistor, a JFET has no junction, and it conducts electricity using bulk current carriers made of N-type or P-type material for semiconductors rather than crossing junctions. Therefore, JFET does not have the intrinsic noise of tubes (due to high-temperature operation) or that of regular transistors (due to junction transitions).

7. It is comparatively radiation resistant.

8. It has superior thermal stability since it has a negative coefficient of temperature of resistance.

9. Because of its great power increase, it is not necessary to use driver stages.

10. It makes a great signal chopper since it displays no offset voltage with zero drain current.

11. It possesses square law features, making it particularly helpful in television and radio receiver tuners.

Drawbacks:

1. The primary disadvantage of JFETs is that they have a relatively low gain-bandwidth product when compared to conventional transistors.

2. A greater propensity for harm when handled.

3. poor voltage gains of JFETs are caused by their poor transconductance.

4. More expensive in comparison to BJT's.

b. MOSFET:

Effect of Silicon Field Transistors and, Metal Oxide sometimes called to as MOSFETs, are electronic components that are fitted in circuits as switch or for amplifying multiple voltage. This voltage lead device has three terminals.

The following names are given to the MOSFET’s terminals:

• Source

• Drain

• Gate

• Source

 The MOSFET’s foundation is a p-type semiconductor.

 The diagram’s n+ symbol represents an n-type impurity that is heavily doped into the two kinds of bases.

 The source and drain terminals come from the heavily doped areas of the base.

 A coating of silicon dioxide is applied to the substrate as insulation.

 The silicon dioxide is stored on top of a thin, isolated metallic plate that serves as a capacitor.

 The thin metal plate containing the gate electrode is removed.

 Then, a voltage source is coupled in between two n-type areas to create a DC circuit.

The functioning of a MOSFET is reliant on electrical variations occurring within channel width along with the motion of carriers, as observed by the MOSFET design below (holes or electrons). By source side, the charge carrier enters a channel, leaving via drain.

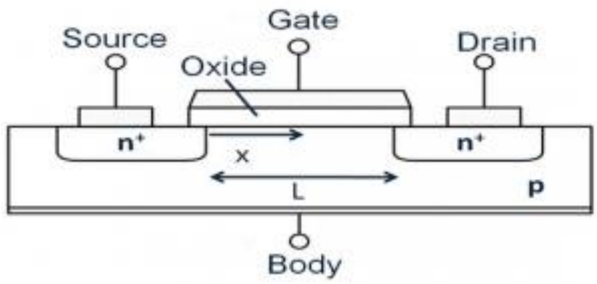


Fig 1.2: Structure of a n channel MOSFET

The MOSFET has following types of functionalities:

i. **Enhancement type:** If there is negligible voltage applied across the gate terminals of transistors, then it is non conducting. If gate terminal exposed to the highest voltage, gadget exhibits better conductive power.

ii. **Depletion type:** The channel exhibits its highest conductance in the absence of any voltage applied crosswise gate terminal. Channel conductive power decreases when either a negative or positive voltage is applied crosswise the gate electrode.

MOSFET Operating Regions

It is observed that a MOSFET has three operational areas. We'll talk about those areas here.

Cut-Off Area

The MOSFET will turn OFF in the cut-off zone since there is going to be no conduction there. The MOSFET acts as an open switch in this situation.

Ohmic Area

The ohmic zone is one wherein the current (IDS) rises as the value of VDS rises. MOSFETs are employed as amplifiers when they are designed to function in this range.

Area of Saturation

When VDS surpasses the pinch-off voltage Vp, the MOSFETs enter the saturation area, where their IDS remain constant despite a rise in VDS.

MOSFET as switch:

MOSFET character	VGS < 0	VGS = 0	VGS > 0
N-type Enhancement	OFF	OFF	ON

N-type Depletion	OFF	ON	ON
P-type Enhancement	ON	OFF	OFF
P-type Depletion	ON	ON	OFF

Switches frequently make use of MOSFETs. The MOSFET's configuration when utilized as a switch is seen in the circuit below.

Table 1.1: switching MOSFETs of the N-channel and P-channel types

The Enhancement mode N-channel MOSFET is utilized in the circuit configuration to turn a basic bulb "ON" and "OFF." To power on a device the input fate voltage Vgs is set to a proper positive voltage, and to power off the level of voltage is made a negative value or 0.

The table above summarizes the characteristics of switching for MOSFETs of both the N-channel and P-channel types.

Advantages of MOSFET:

• Even while operating at low voltage levels, it produces increased efficiency.

• Due to the absence of gate current, the input impedance is higher, increasing the switching frequency of the device.

•These gadgets just require a little amount of electricity and power to operate.

Disadvantages of MOSFET:

• Device becomes unstable if worked at extensive voltage levels..

• Thin coating of oxide on the devices raises the possibility of device breakdown when driven by electrostatic charges.

1.2 Introduction to RFET

In order to improve the usefulness of electronic systems, new strategies are needed as CMOS scaling approaches physical constraints in the following ten years. Device-level reconfigurability holds the possibility of realizing more sophisticated systems with fewer devices. To implement such a hardware reconfiguration, several intriguing notions have been put up during the past five years. The RFET, one of these, can be viewed as an edge extension of present tech with only minor changes and even flowcharts simplifications. This device could be configured between being an n-channel and p-channel behaviour by applying an electrical signal. Metallic source and metallic drain (S/D) regions are a characteristic of RFETs. The Schottky barriers are controlled by supplementary polarity gates (PGs) (SB). Switching from N to P FETs is now possible by choosing which carrier is tunneled into.[1]

Principle of Operation of RFET:

The SB-MOSFET concept serves as the foundation for RFETs [2], [3]. Any one of electrons or holes will conduct in the metallic S/D regions. Mixture of carriers into the channel is bad because S/D metals process utility is not in alignment with its silicon potential of the valence/conduction bands, requiring adjustment by the Schottky barrier height near to the source. The thermionic (carriers whose sufficient energy to overcome its energy gap) with such field emissions (carrier tunnelling through barrier). Current determined by transport processes. Metal process utility that are near to the silicon midgap are chosen in order to obtain symmetrical N/P transfer properties. Owing to comparatively large electron or hole schottky barrier (which is almost 1⁄2 the silicon energy bandgap, or 0.56 eV), the thermionic emission is thus quite low. The three-Gates RFET configuration at lower drain voltage (VDS tending to 0V) is depicted in Fig. 1.3 as being modulated by the PGs in terms of the front channel energy bands. As shown, the PG voltage is supplied with regard to S/D allows for modulation of the energy barrier height, which is connected to carrier tunneling. In Figure 1.3 a, positive PG biases allow holes to tunnel towards to the valence band whereas negative voltages allow electrons to tunnel to conduction band from metallic source (Fig. 1.3 b). Near to the front channel at which electrostatic control caused by polarity gates allows for a sharper band bending, this carrier injecting is more effective. The control gate (CG), on the other hand, is in charge of regulating the current flow via causing (in the OFF-state) or not (in the ON-state) a potential barrier in the centre of the channel.

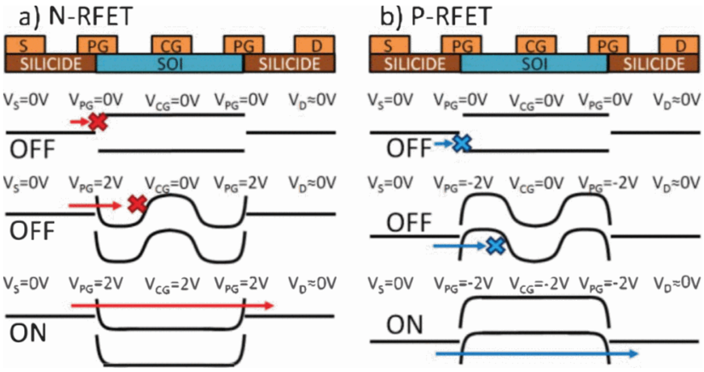


Fig 1.3: The energy band diagram of 3 gate RFET where Programmable gate selects the carrier type and Conduction gate controls the flow of current [1]

1.3 Advantages and limitations of RFET

Advantages:

- No need for doping in S/D areas (no random dopant fluctuations)

  Random dopant fluctuation is a type of process variation brought on by changes in the concentration of implanted impurities. RDF in the channel area of MOSFET transistors can change the transistor's characteristics, particularly the threshold voltage. Because there are fewer dopants overall in more recent process methods, the addition or removal of only few impurity atoms may drastically change transistor characteristics. As a result, RDF has a stronger impact. Because RDF is a local kind of process variation, the dopant concentrations in two nearby transistors may change noticeably. [4]

- Fewer manufacturing stages and a reduced thermal cost (no dopant activating, epitaxy, or S/D implantation) [1]

- Feasible component number reduction for equivalent logic operations

- Reversible operation: Since only the voltages applied at the program and control gates decide the functioning of the RFET, as the structure is exactly similar for both.

Challenges:

- Demonstrate the benefit on entire systems and provide the necessary computer-aided design (TCAD) tool for investigating the benefits of programmable components in ultra-high integrated circuits.

- Improve the Ion current and Ion/Ioff current ratio. [5]

- Implement the device using cutting-edge CMOS technology.

- Consolidate reconfigurable circuitry and sensors into a single technological platform.

Chapter 2

2.1 Overview of Nanowire RFET

The nanowire reconfigurable transistor (figures 2.2(a), (b)) is a concept representation with two separate gate electrodes is built on a presumably intrinsic silicon nanowire (figure 2.1(a)) with silicidation-formed intruded NiSi2 contacts in the bottom-up realisation illustrated here by Heinzig et al [6], Si core produced with a radius of 10 nm. thermally formed wrapping SiO2 shell for the two upper gates, oxidation is used which is used as a gate dielectric electrodes. One gate electrode is referred as as the program gate / polarity gate effectively inhibits the injection of just one charge carrier type, electron or holes. At that same time, the injection of another kind of charge carrier may be regulated by the control gate, which is the other gate electrode

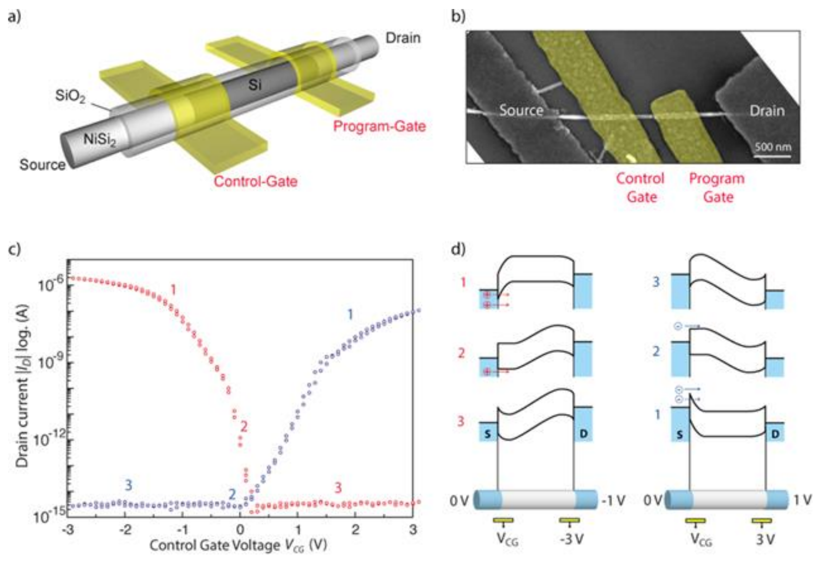


Fig 2.1: The reconfigurable nanowire FET (a) schematic (b) top view (c) transfer characteristics for p and n type (d) energy band diagram

Figure 2.1(c) depicts the nanowire RFET transfer characteristic and the related band diagram for varying combinations and states. Vds applied and then a negative potential of program gate Vpg enable P-type behaviour (figure 2.1(a) red curve). The higher electron barrier at the drain side prevents electron injection in all p-type configuration states 1 to 3. A negative voltage on control gate electrode causes substantial band bending at source side, with holes being injected from the metal to semiconductor through tunnelling through the thinning barrier & thermionic emission across the barrier (state 1) [5,7].

Band bending decreases as Vcg rises till flatband occurs (state 2). Since this state creates the transition between tunneling and thermionic emission, the transfer curve simply shows a distinctive kink. The energy barrier at greater Vgc prevents the injection of holes, as demonstrated by off current flow at the measuring limit. Switching the polarities of Vds and Vpg prevents hole injection in all states 1-3, converting the RFET to an n-type behaviour depicted by the blue dotted line in figure 2.1. (c). [6]

The RFET's driving current is primarily restricted by tunnelling across the Schottky barrier, which begins using simply gate junction. Because changes in the effective barrier near the junction is less than a change in the barriers for thermionic emission at the centre of the junction, the gradient of the transfer curve within that area is smaller than in a traditional FET or the idea with concurrent barrier control [7]. The efficient blockage of both electron and hole injection in RFET off-state lowers charge buildup within the channel. As a result, very low off current and large on/off ratios are possible [6]. As a result, the RFET idea has particular promise for the utilisation of narrow BG materials. [8]

Figure 2.1(c) shows that the on currents of the p and n type configurations differ by many orders of magnitude. The VG -IDS characteristic exhibits a similar asymmetric behaviour in every SBFETs using Si NiSi2 junction, including the other ideas outlined in the preceding section. The fundamental reason is the NiSi2's workfunction of source and drain contacts, that is not precisely at the middle of silicon bandgap. Because electrons have a greater Schottky barrier than holes, thermionic and tunnelling currents are reduced, resulting in lower n-type currents.

Chapter 3

Nanowire RFET as a biosensor

3.1 Structure

To meet the ever-increasing need for quick and with power efficiency logic operations, following below par manufacturing costs of Integrated circuits (ICs), the microelectronics industry is undergoing a fast development via rapid downscaling of device scale. This notion of shrinking is critical in improving device performance and achieving desired increased efficiency. Yet, it has been shown that when dimension is reduced to the nanoscale zone, MOSFET using traditional planar technology can no longer support Moore's law. [10]

Traditional downscaling has several physical restrictions, including reliability concerns, unwanted SC effects, higher Ig current, reduced subthreshold slope, greater power utilization, and so on [11] [12]. As a result, an alternative way to overcoming the fundamental challenges of scalability requires the use of novel technology or the implementation of few modern design, which then solves the power crises and short channel concerns. According to recent literature research, double gate topologies, FinFETs, and totally depleted Silicon On Insulator technologies provide increased device functioning due to greater gate electrical control and the capability to dramatically reduce SC effects.

Additional ground breaking development is achieved by using 1 Dimensional channel geometries such as CNT(Carbon Nano Tubes), silicon nanowires, which are when wrapped in a gate all around way cater the finest controllability of the channel and exhibit the better Ion:Ioff ratio in contrast to planar and some other multigate equivalents [13], [14], [15]. Because of its intriguing shape and intrinsic device physics, ultrathin nanowires as next generation electronics may be modulated. And such possible device architecture is ambipolar silicon nanowire, also known as reconfigurable-field effect transistors (FETs), which have the unusual reconfigurable feature of creating p-type and n-type properties depending on the bias polarity [16].

Many RFETs have been described with the dual gate and three gate architectures as control and programme gates for regulating and switching the device's drain current and polarities [17]. In RFETs, conventional ohmic source/drain (S/D) connections are replaced with schottky metal S/D contacts, which decreases fringe capacitive effects, high access resistance, and variability difficulties [18,19]. Because dual polarity devices can be created using the similar nanowire structure, the reconfigurable behaviour may be used with complicated circuit design for enabling complementary with reprogrammable CMOS functioning with a smaller number of transistors. Consequently, RFETs that enable multi-functionalities inside an unit device by implementing any n type or p type behaviour via alternative biassing configurations provide an excellent substitute to the usual trend of ultra-scaling.

This contributes to increasing the variety of functionalities per transistor without lowering the device shape, resulting in better integrated package densities at a lower cost [21], [22]. According to recent literature findings, RFET-based complex circuits outperform standard CMOS circuits in aspects of propagation latency, space consumption, and power. Furthermore, the distinct property of reconfigurability generates a safe hardware system using innovative camouflage circuits [23]. Thus, RFET devices, with their known advantages, are attracting great exploration attention to investigate its multiple application in a variety of disciplines [20].

Due to its feasibility with basic CMOS higher sensitivity, fabrication technology, and miniaturisation, a few FET-based biosensors are gaining widespread attention in the biosensor areas for label-free sensing of charged and neutral bio molecules [24].

Vertical nanogaps are carved underneath the gate material in dielectric modulated (DM) FET to fix the bio-molecules, that upon interacting with the device affects transistor electrostatic with assess its sensitivity appropriately. But, the expensiveness, structural instability, along with limited binding capability of such devices limit their use as biosensors [25], [26].

As a result, gate underlap DM FETs are gaining traction for a possible choice of FETbased biosensors, with the gate underlap cavity produced by etching both of the gate materials with gate dielectric [27]. Model results of nanogap implanted bio sensors with bio targets restricted to the etched underlap area are seen reported in latest studies. Junctionless FETs and Quad Gate DM MOSFETs are widely employed as biosensors, with fluctuations in drain current, potential shift, and cutoff voltage deviation serving like biosensor sensing metrics [28], [29], and [30].

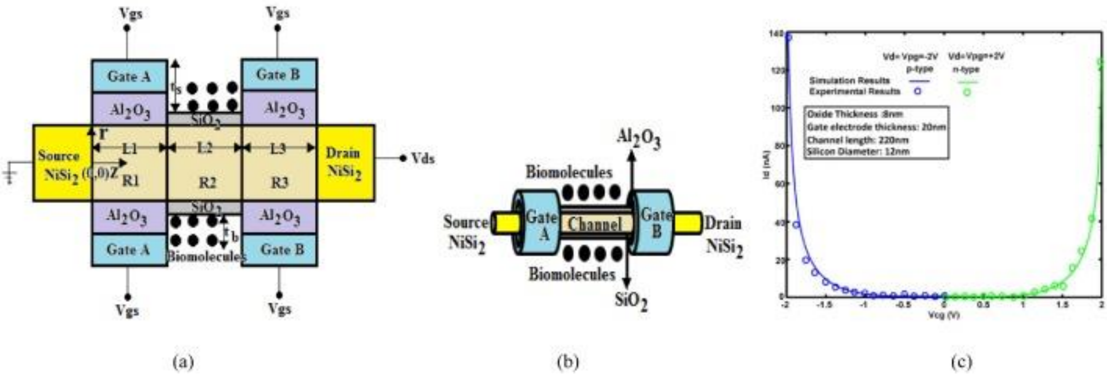


Fig 3.1: Example of Nanowire FET as a biosensor [9]

Figure 3.1(a) and (b) illustrate a two-dimensional cross sectional view as well as a three dimensional schematic depiction of a nanowire reconfigurable FET to utilised as a biosensor.

3.2 Sensitivity of a biosensor

Field-effect transistor-based biosensors have emerged as a key technology for detecting ions, pH, deoxyribonucleic acid (DNA), as well as other macromolecules in physiologically relevant fluids. These sensors are appealing due to their great sensitivity in detecting charged analytes. This has been a push to make them even more sensitive. A biosensor shown in figure 3.2 is implemented by growing HfO2 on the SiO2 and then the biomolecules have been placed above the channel region between source and the drain.

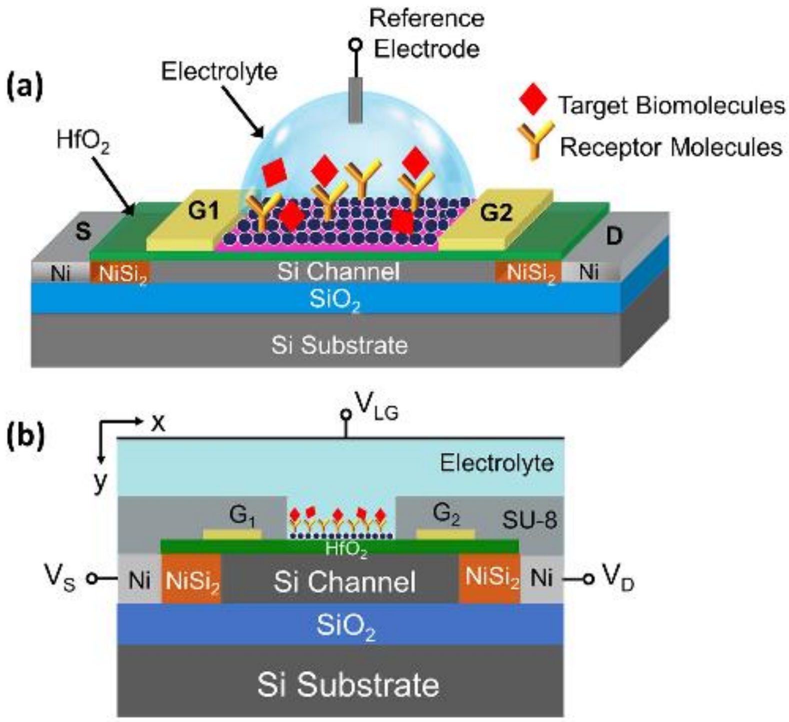


Fig 3.2: Biosensor using RFET [31]

The sensitivity of a biosensor can be judged on the basis of some factors. Some of them are central potential variation and threshold voltage variation, which can be done on neutral as well as charged biomolecules.

When a positive/negative gate voltage is applied in the existence of a fixed positive/negative drain bias, it behaves as a n (p) type FET wherein potential barrier reduces with increasing Vgs, demonstrating that our developed model is capable of accurately capturing the reconfigurable attribute. Variations in the dielectric constant and charge density of neutral biomolecules affect the flat band voltage, which is represented in the minimal central potential shift. As a result, this potential variance is compensated for, showing the RFET's bio-sensing response.

For examining the trend of a biosensor, the influence of dielectric constant fluctuation of immobilised neutral molecules entirely filling the underlap region is taken into account. When the dielectric constant of bio targets goes from unity to a higher value, the lowest central potential of the RFET working as a n (p)-type increases, reflecting a steady decrease in the transistor potential barrier.

Chapter 4

Implementation of RFET as a biosensor

4.1 Structure:

The structure taken here is of nanowire RFET with Gate work function= 4.63 and Source/Drain work function of 4.65. The relative permittivity HfO_2 is taken as 25 and it works as an oxide with cavity at the cathode side. The control gate here is referred to as the cathode. The cavity here that we place is taken for biomolecules to be inserted. The biomolecules of neutral nature is studied here for sensitivity calculation. The variation of permittivity is studied in reference to the change in threshold voltage for both n type and p type FET. Silicon of radius R which is varied along with cavity height for optimization of the parameters and then we shall proceed with varying k(permittivity of Biomolecules). The relative permittivity of spacer used is 80.
The major parameters that we measure in here are:

- Threshold voltage(Vt1)
- Subthreshold Slope
- Ion
- Ioff
- Ion/Ioff
- Transconductance(gm)

The structure that has been simulated using Silvaco TCAD is shown in the figure 4.1.

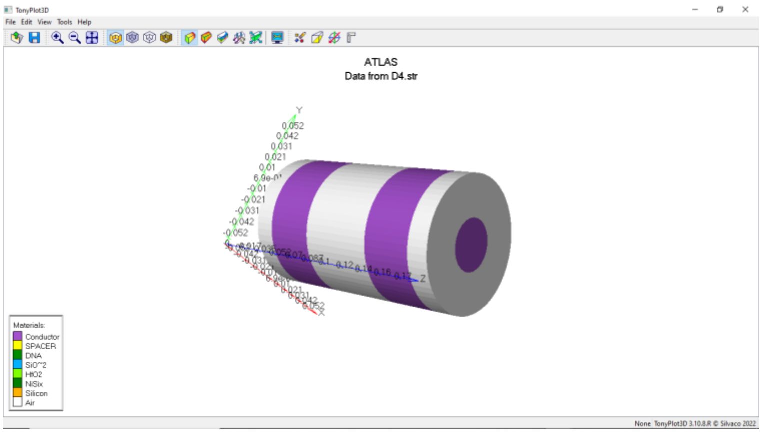


Fig 4.1: 3D structure using Tonyplot 3D

Lsource=37nm

Ldrain=37nm

Lgap=5nm

Lmid=6nm

Doping= 1 e12

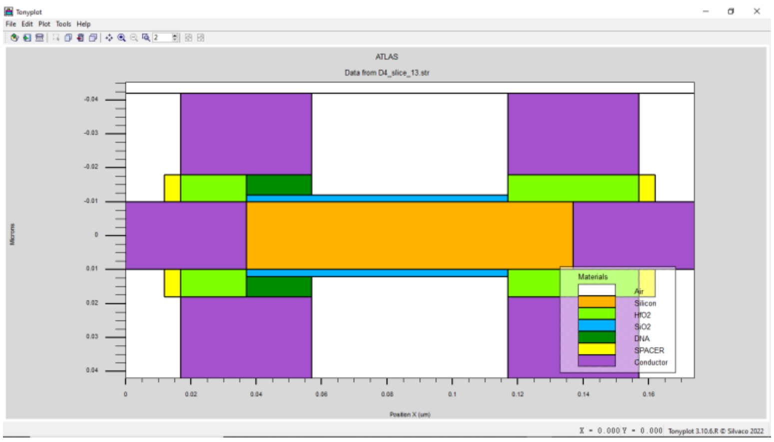


Fig 4.2: Plane cut structure using Tonyplot

4.2 Optimization of Parameters

After varying various parameters for optimization, it is found that the major effect on the properties of the biosensor FET is observed by varying Radius R of the silicon and the cavity height C, where the biomolecules are to be inserted.

Some equations indicating important relations between various parameters:

$$\frac{d^2\phi_{CR}(z)}{dz^2} - \frac{1}{\lambda_{CR}^2}(\phi_{CR}(z) - \phi_{CR}) = 0$$

$$\lambda_{C1} = \sqrt{\frac{4\varepsilon_{si}t_{si} + C_{o1}t_{si}^2}{16C_{o1}}}$$

Where lambda is scaling parameter.

$$C_f = \frac{2\varepsilon_b}{n\pi L_2}\sinh\left(\cosh^{-1}\left(\frac{(t_{Al_2O_3} - t_{SiO_2}) + t_{gate}}{t_{Al_2O_3} - t_{SiO_2}}\right)\right)$$

The above equation is for cavity being full, the capacitance for that

$$\phi_{C1} = V_{gs} - \eta_1$$

$$\eta_1 = V_{fb1} \pm \frac{qN_{ch}\lambda_{C1}^2}{\varepsilon_{si}} \text{and } V_{fb1} = \phi_m - \phi_{si}$$

$$\phi_{C1}(z) = A_1 \exp\left(\frac{z}{\lambda_{C1}}\right) + B_1 \exp\left(-\frac{z}{\lambda_{C1}}\right) + \phi_{C1}$$

$$V_{bi,d} = \chi + \frac{E_g}{2} + \phi_f - \varphi_d - \Delta\Phi_{b,d} + V_{ds}$$

Table 4.1: Optimizing radius keeping cavity height fix at 6nm with k=1

Radius Vary@6nm cavity	5nm	10nm	20nm	30nm
Vt(V)	1.153	1.728	2.474	2.622
Sub Vt(V/decade)	0.2484	0.4074	0.6103	0.7096
Ion/Ioff	35200.1	20990.4	3340.1	626.8
Ion(A)	4.2 e-09	1.5 e-08	1.1 e-08	4.9 e-09
Ioff(A)	1.2 e-13	7.15 e-13	3.41 e-12	7.87 e-12
gm	9.75 e-09	1.56 e-08	2.16 e-08	1.31 e-08

Table 4.2: Optimizing Cavity height keeping radius at 10 nm with k=1

Cavity vary@ radius=10nm	4nm	6nm	8nm	10nm
Vt(V)	1.48	1.73	1.98	2.19
Sub Vt(V/decade)	0.3374	0.4074	0.4806	0.5414
Ion/Ioff	25532.3	20990.4	15259.8	11077.1
Ion(A)	1.7 e-08	1.5 e-08	1.2 e-08	8.9 e-09
Ioff(A)	6.6 e-13	7.1 e-13	7.6 e-13	7.9 e-13
gm	1.99 e-08	1.56 e-08	1.29 e-08	1.12 e-08

For radius we see the most optimum results with R=10 nm and after fixing that and varying the cavity height, we find that the most optimized results are obtained with C= 4 nm

Hence the parameters have been optimized

Below are pictures for simulated of the same.

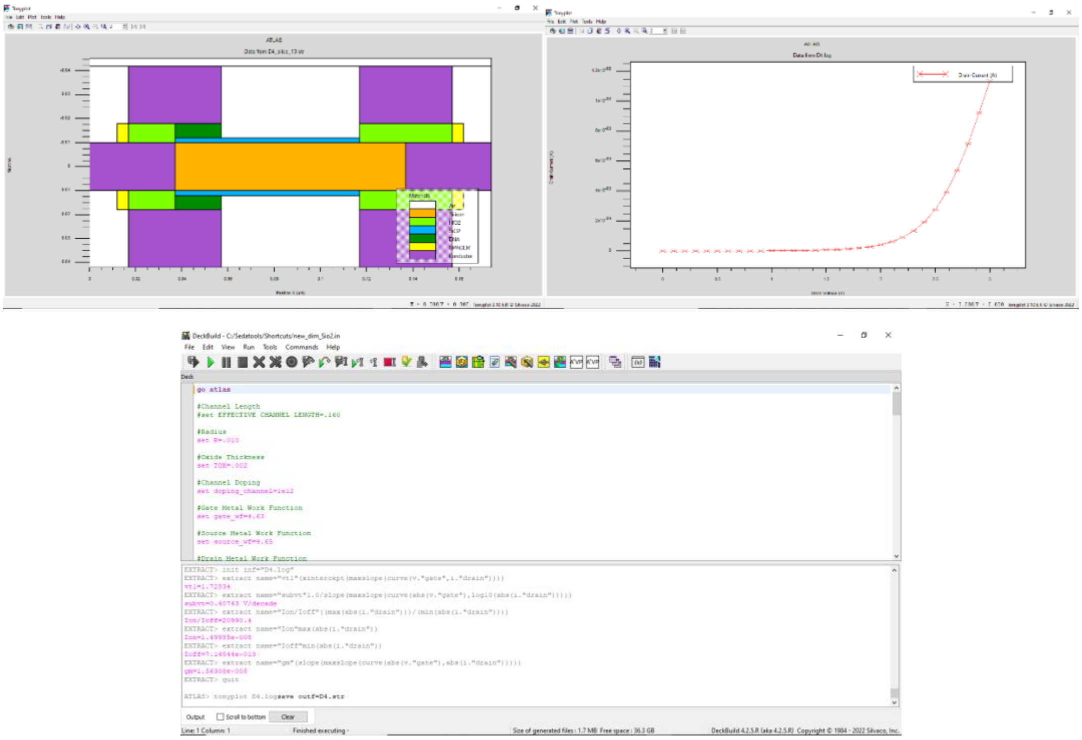
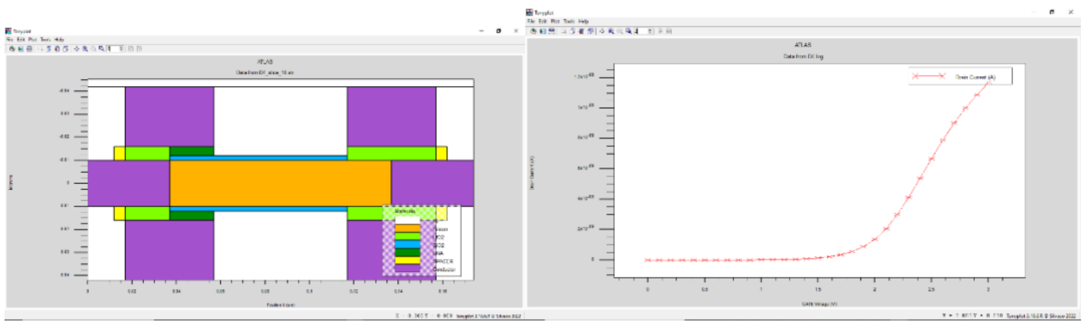


Fig 4.3: Simulated for radius =10nm keeping cavity at 6nm



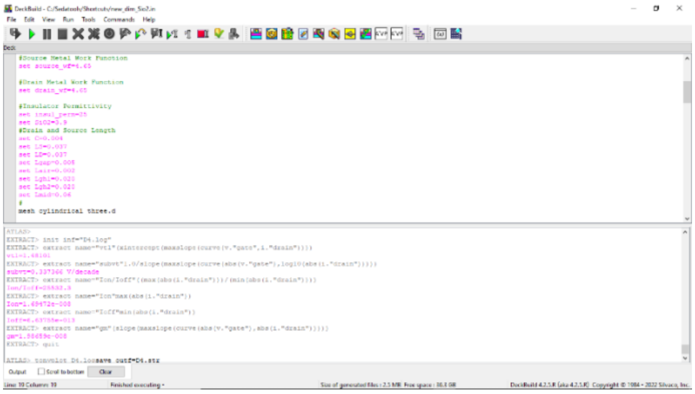
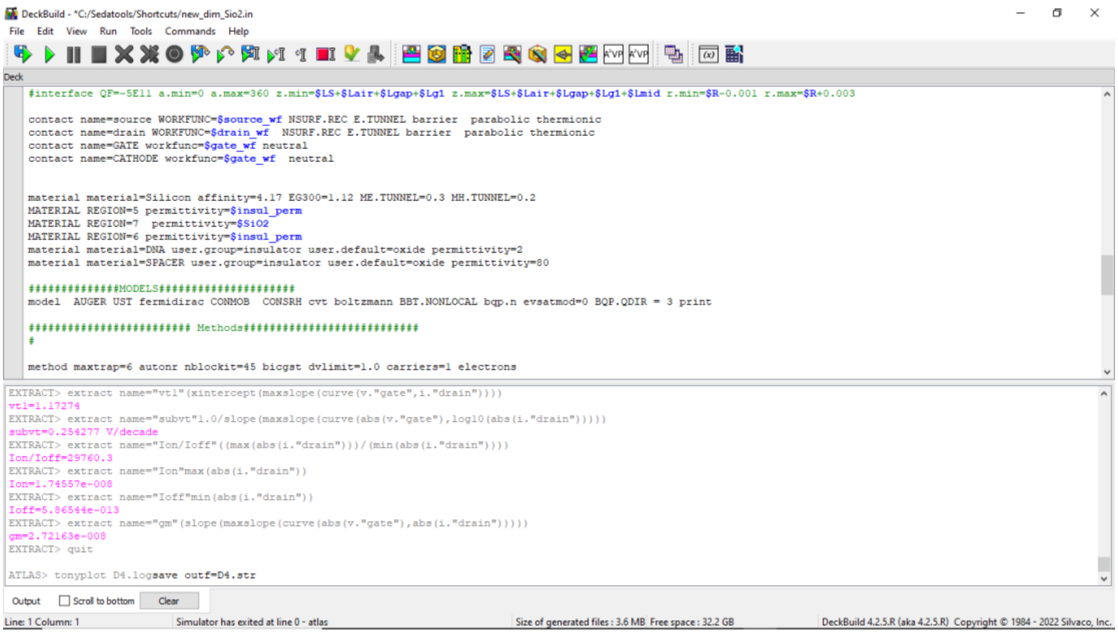


Fig 4.4: Simulated for cavity = 4nm keeping radius =10nm

4.3 Simulated as n type for varying k

Taking optimized parameters and simulating for n type by taking Vdrain= 1V, Vcathode= 2V, and varying Vgs from 0 to 2V with a step of 0.1 V.



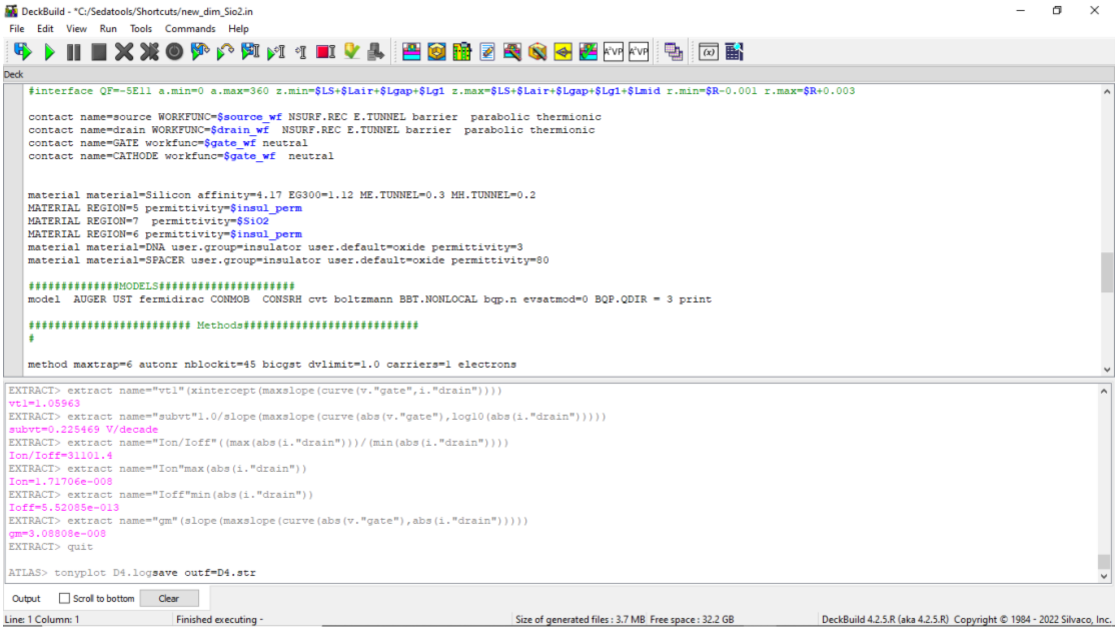
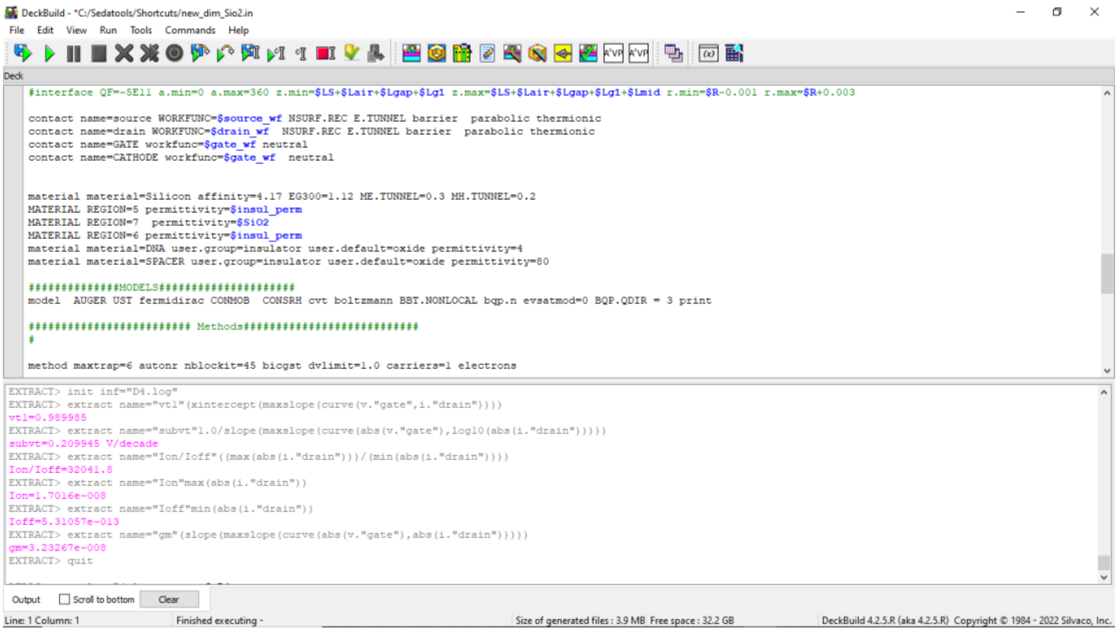


Fig 4.5: Simulated results for k=2,3 for n type



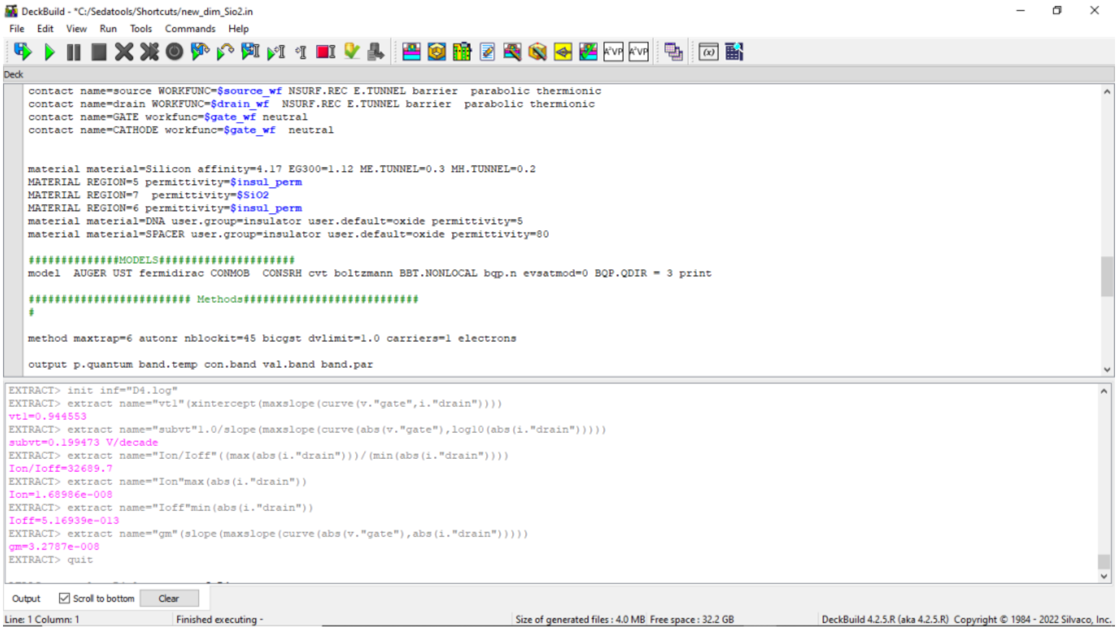
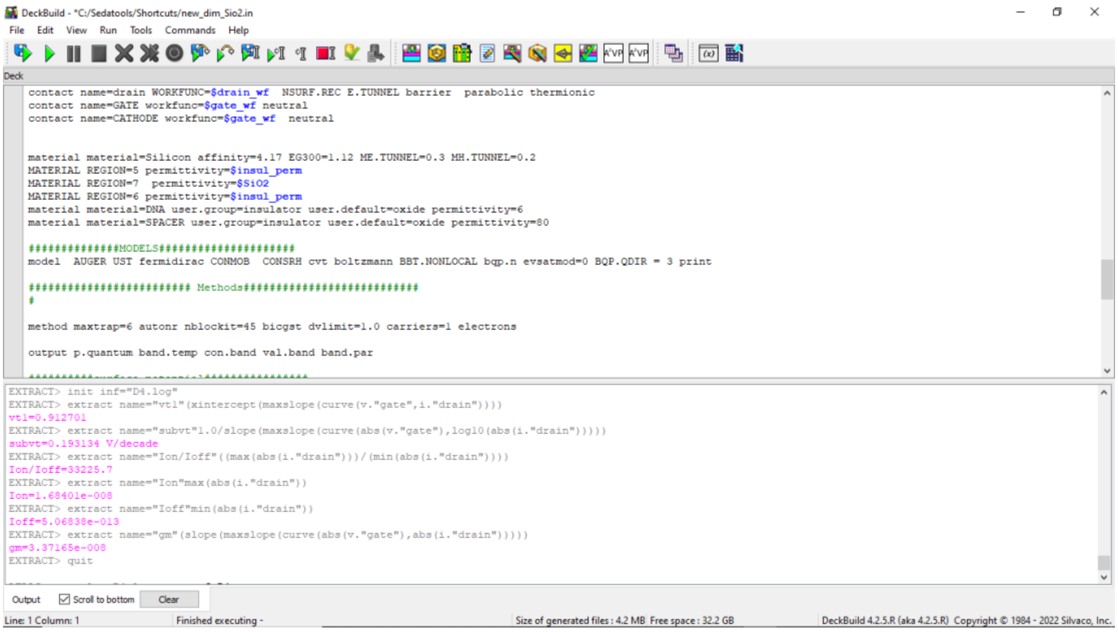


Fig 4.6: Simulated results for k=4,5 for n type



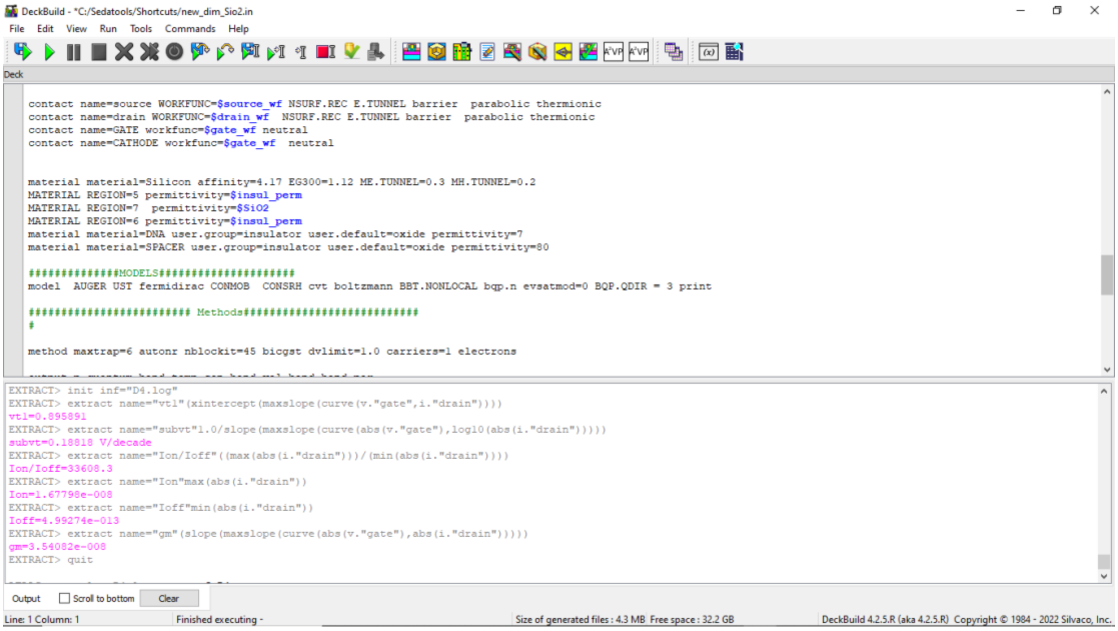
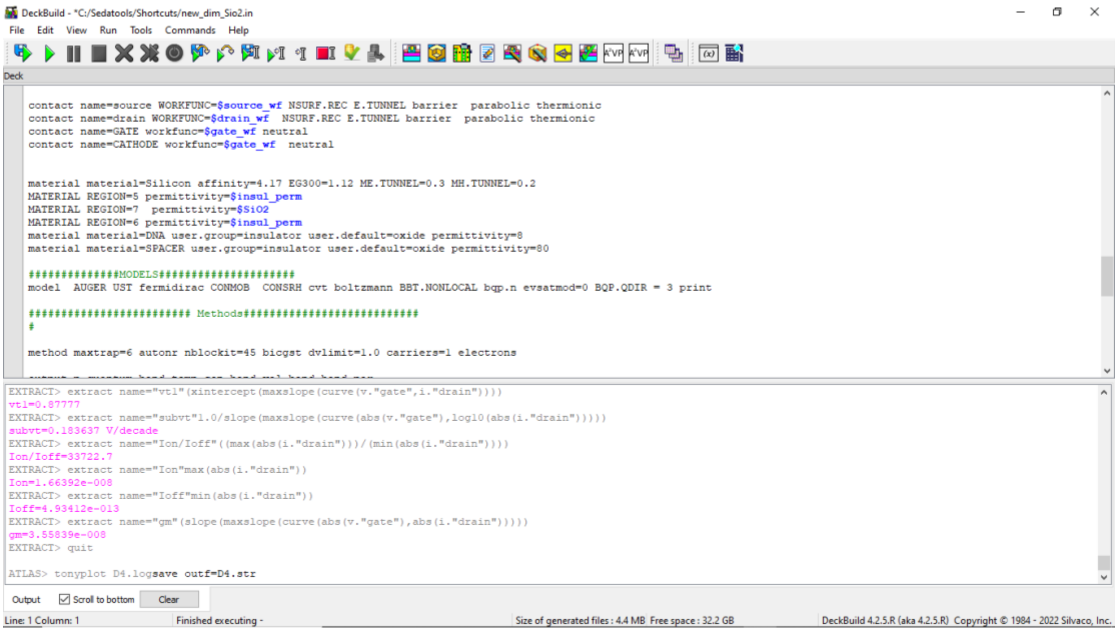


Fig 4.7: Simulated results for k=6,7 for n type



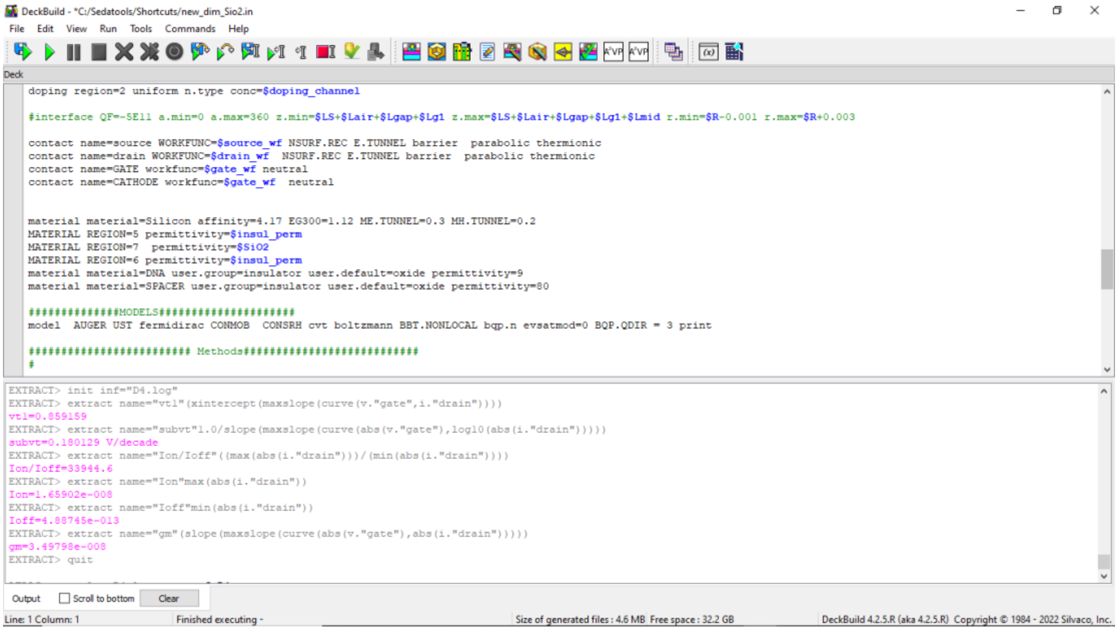
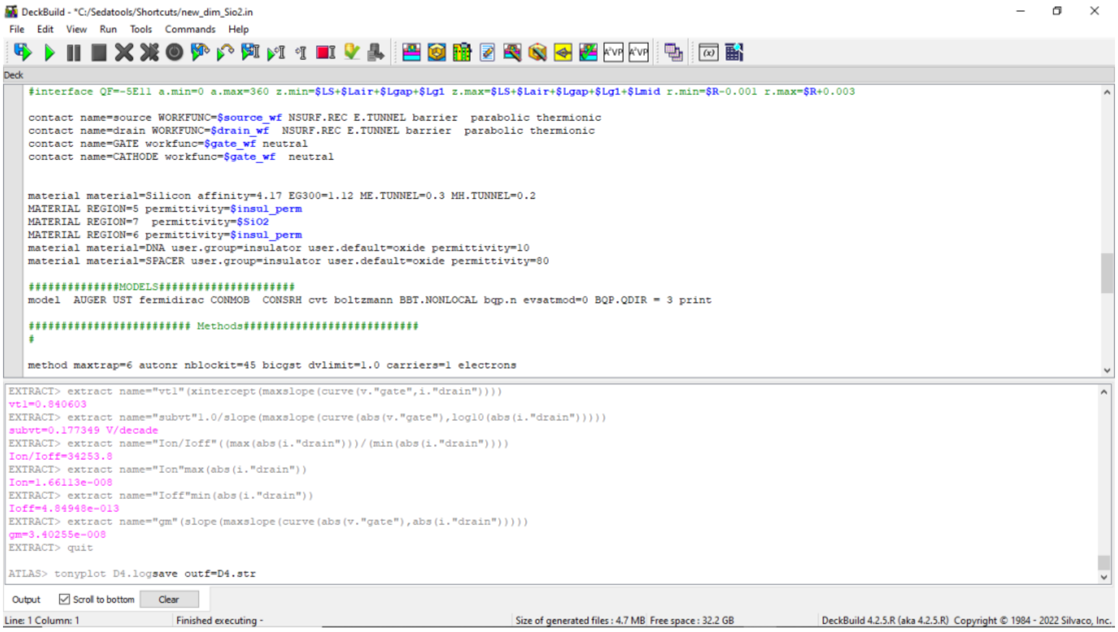


Fig 4.8: Simulated results for k=8,9 for n type



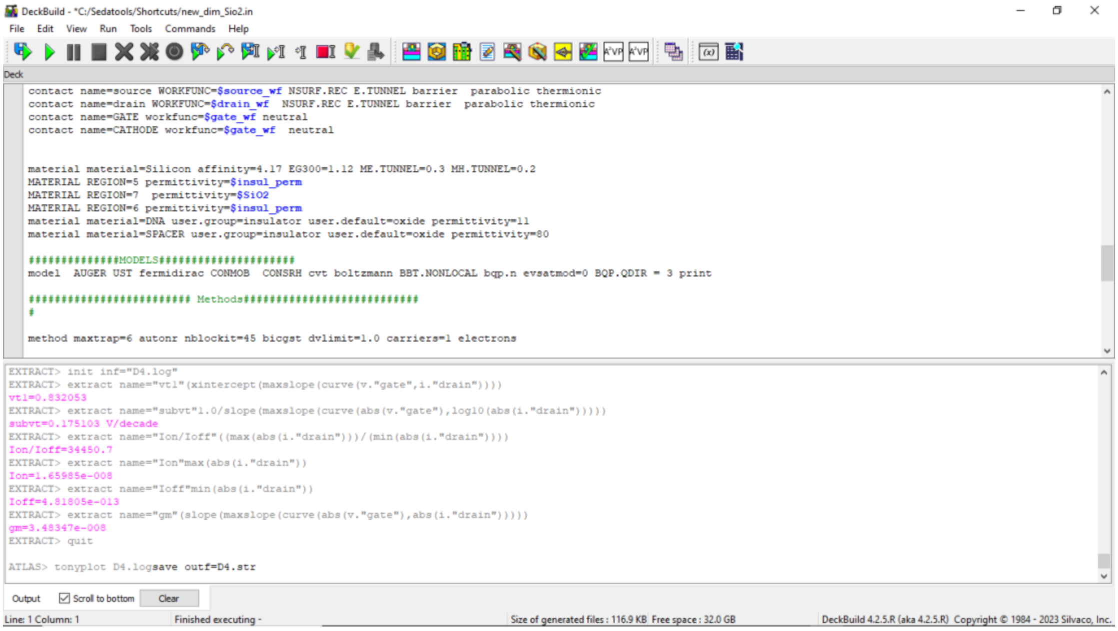


Fig 4.9: Simulated results for k=10,11 for n type

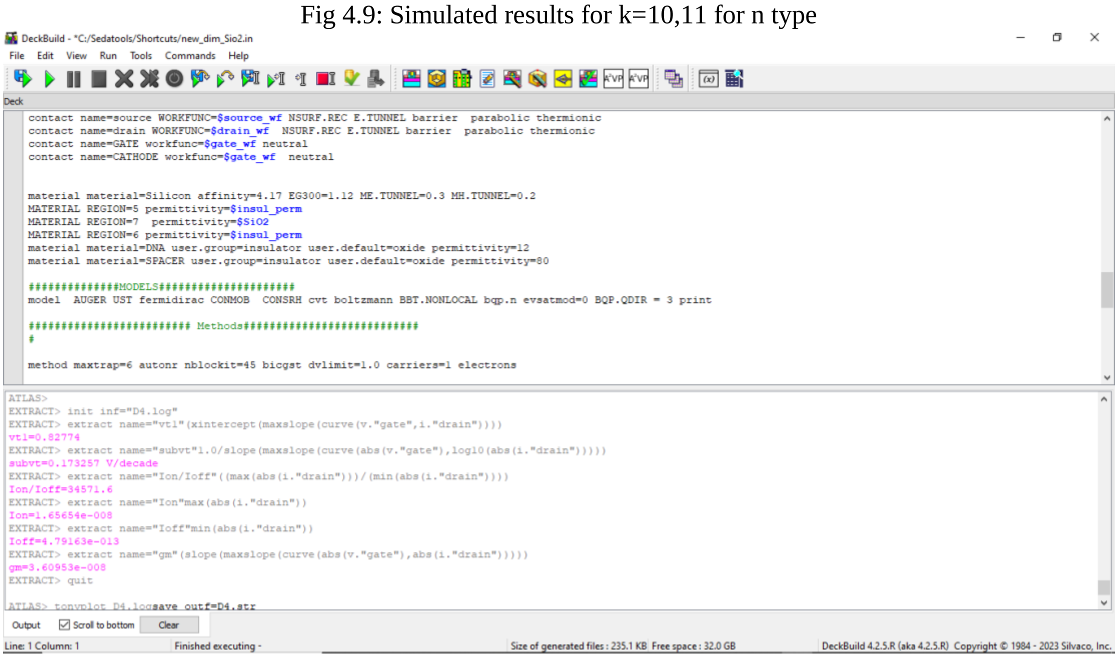


Fig 4.10: Simulated results for k=12 for n type

4.4 Simulated as p type for varying k:

Taking optimized parameters and simulating for n type by taking Vdrain=-1, Vcathode=-2 and varying Vgs from 0 to -3 taking -0.1 as a step.

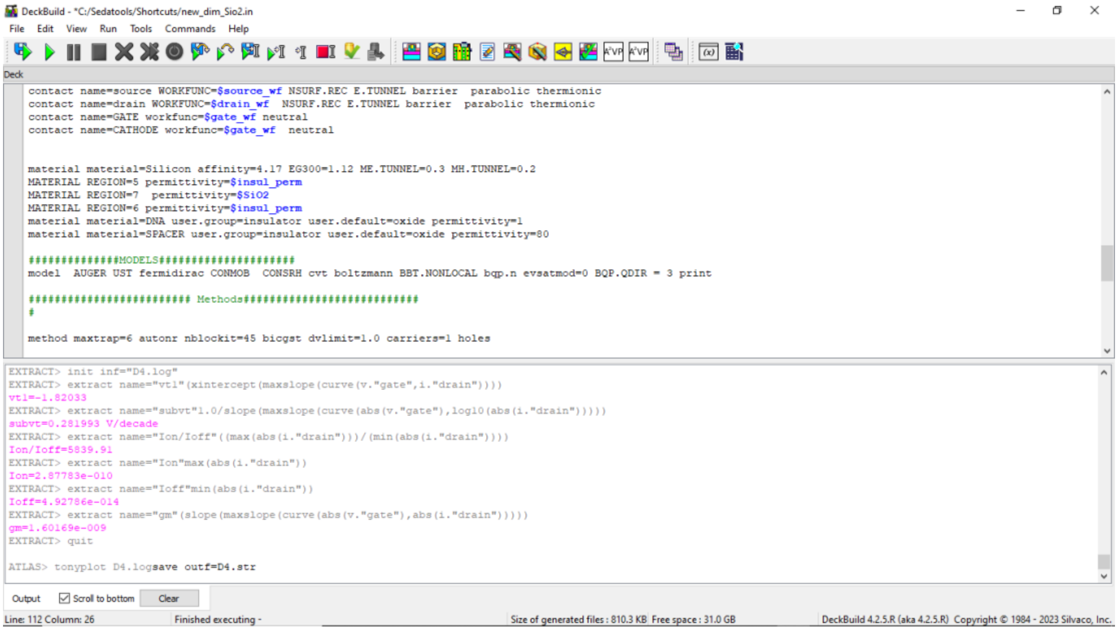
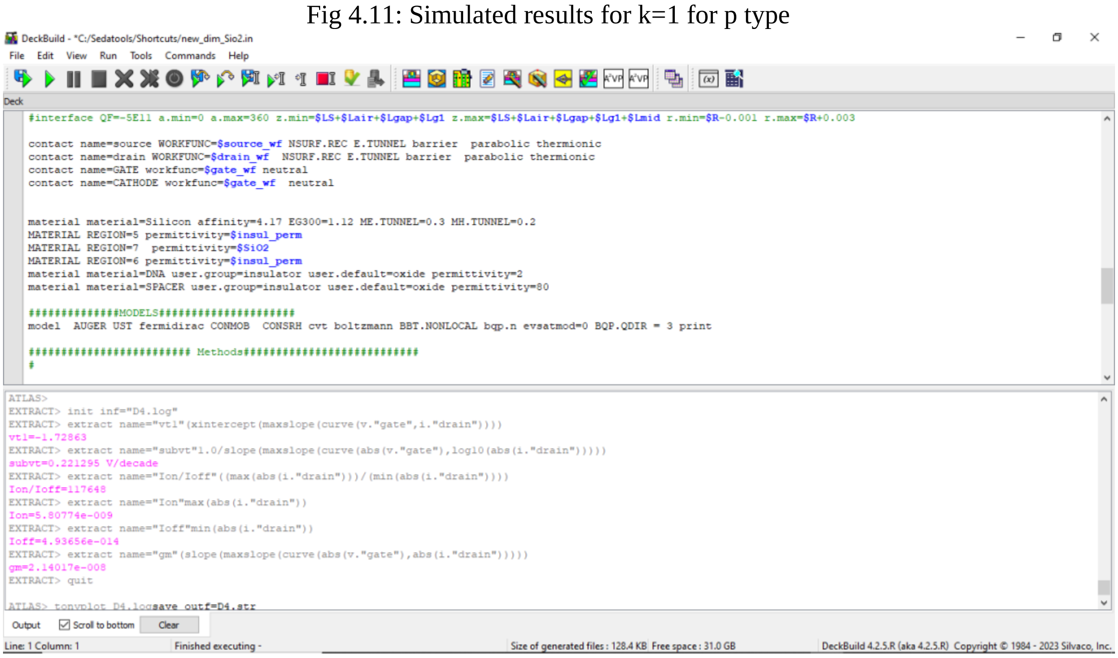


Fig 4.11: Simulated results for k=1 for p type



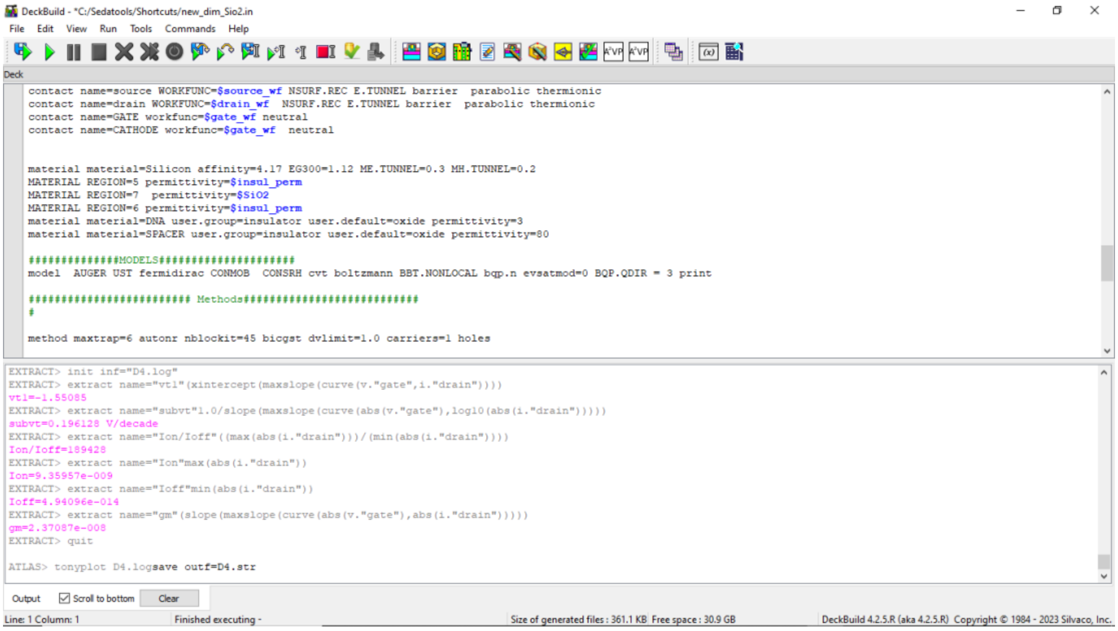
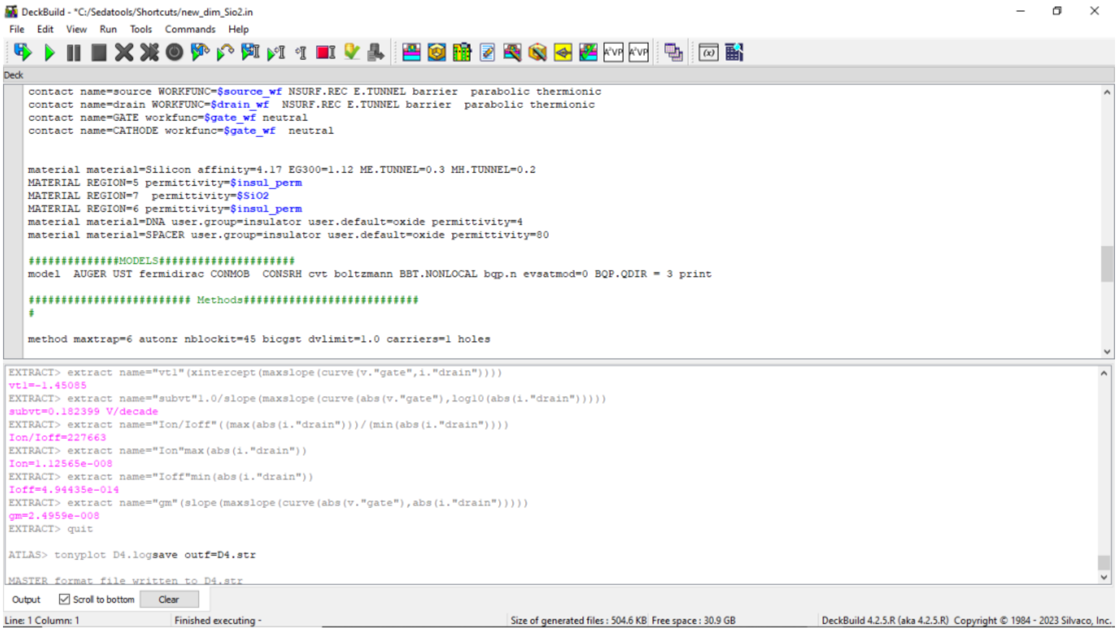


Fig 4.12: Simulated results for k=2,3 for p type



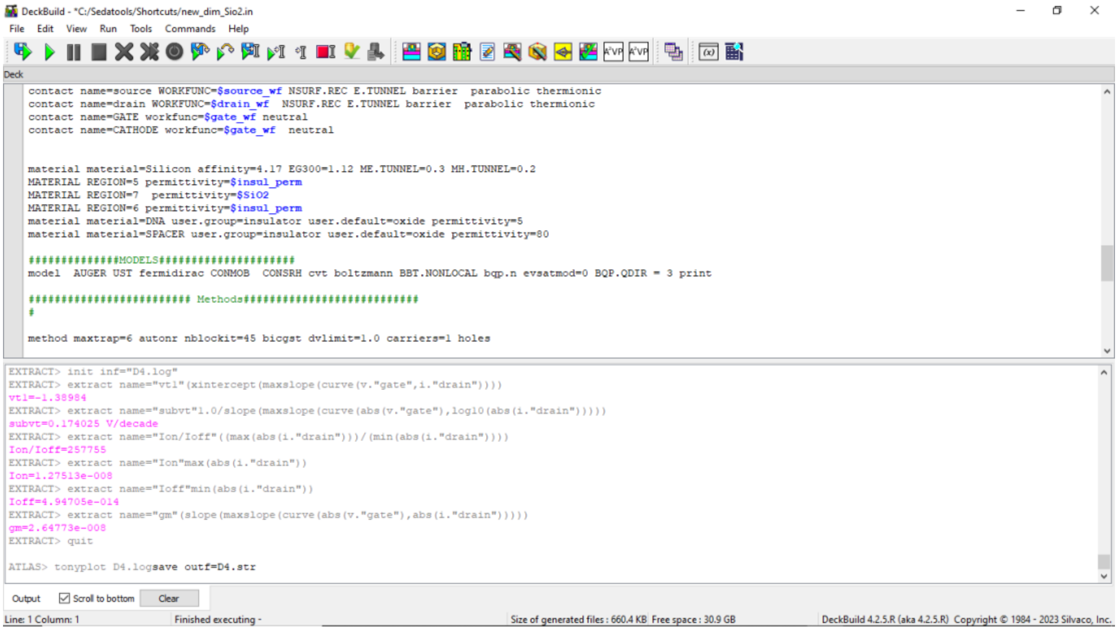
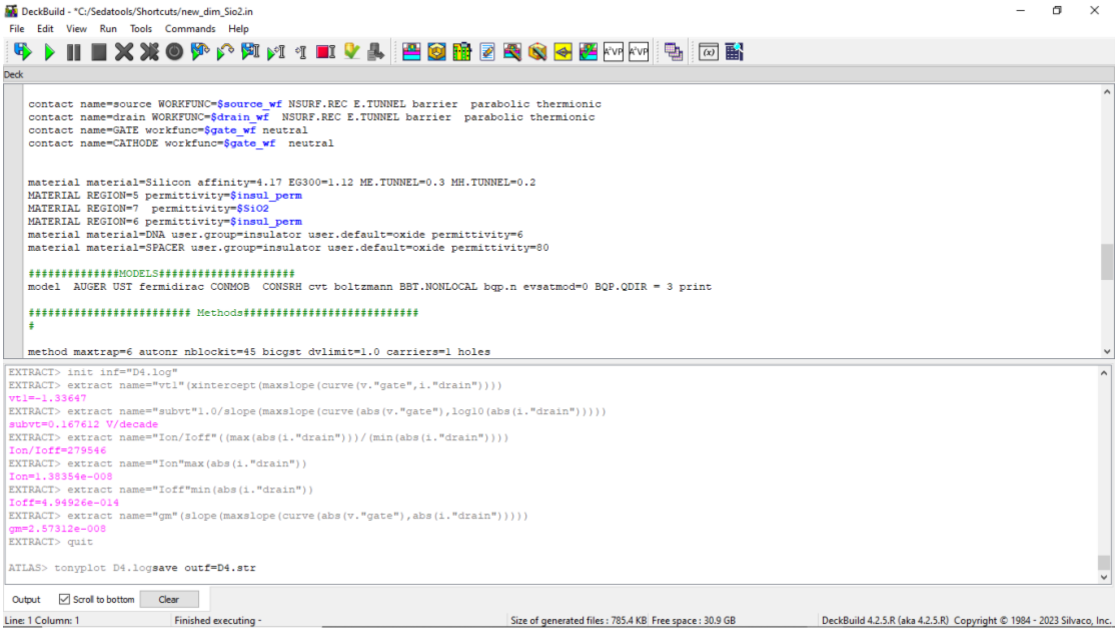


Fig 4.13: Simulated results for k=4,5 for p type



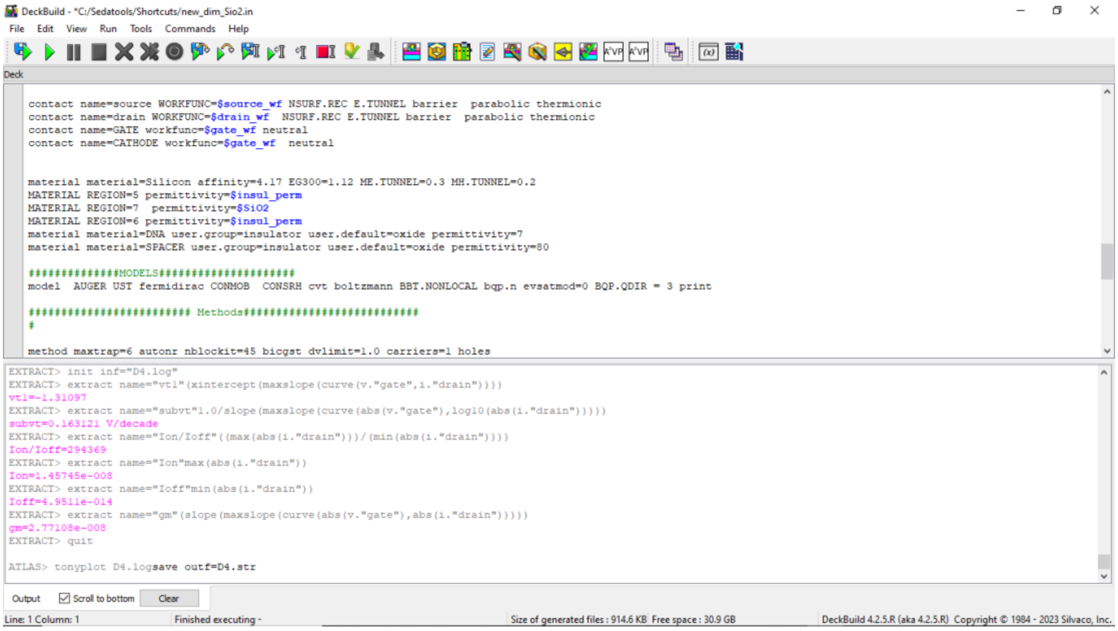
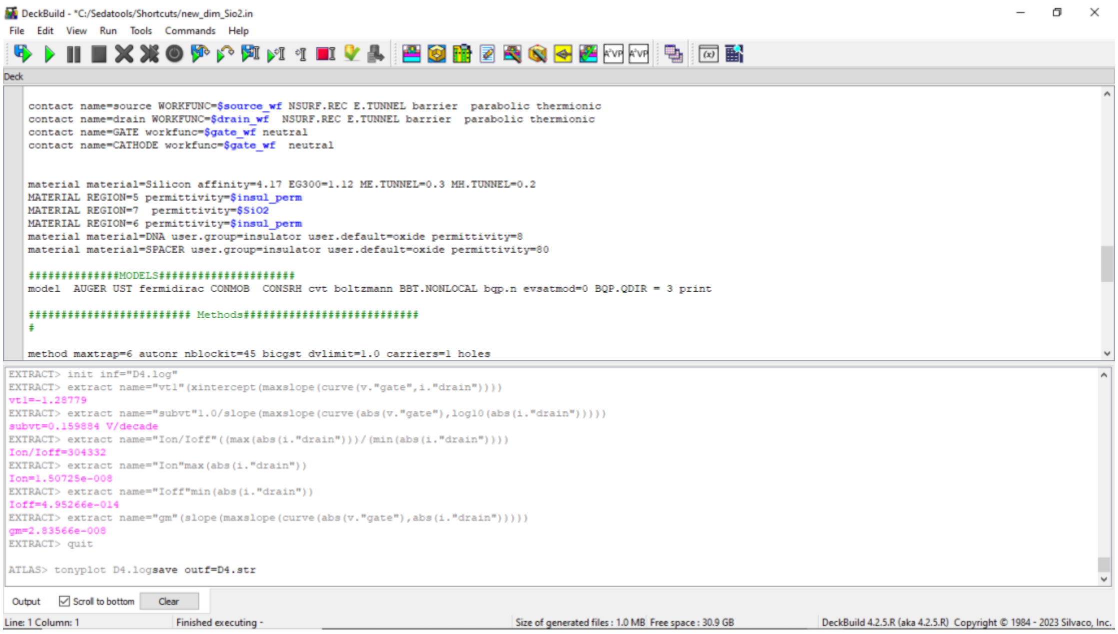


Fig 4.14: Simulated results for k=6,7 for p type



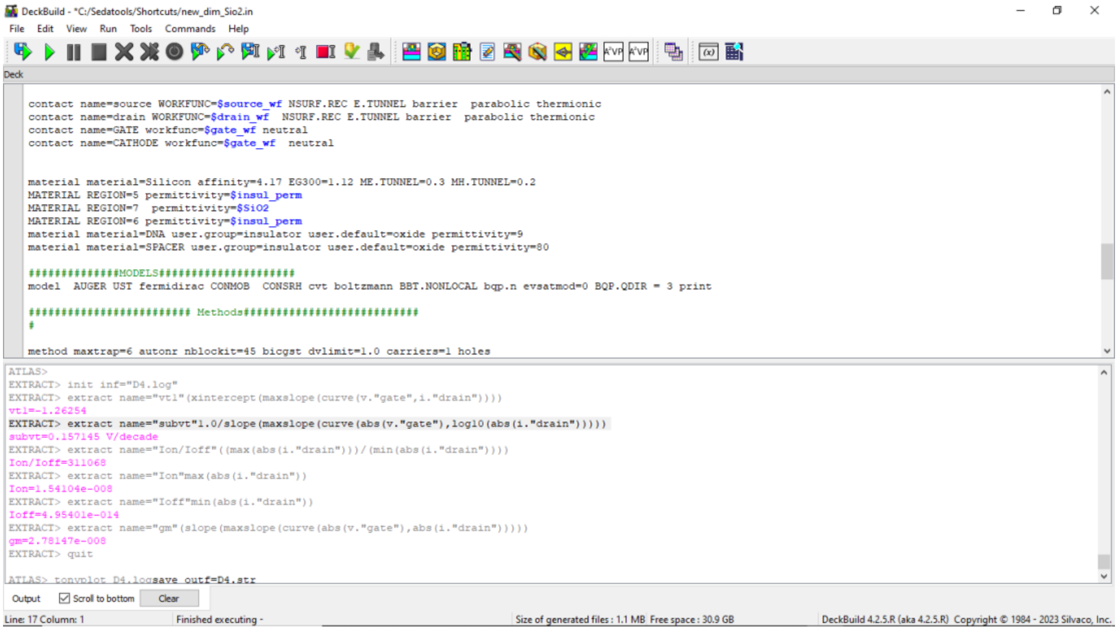
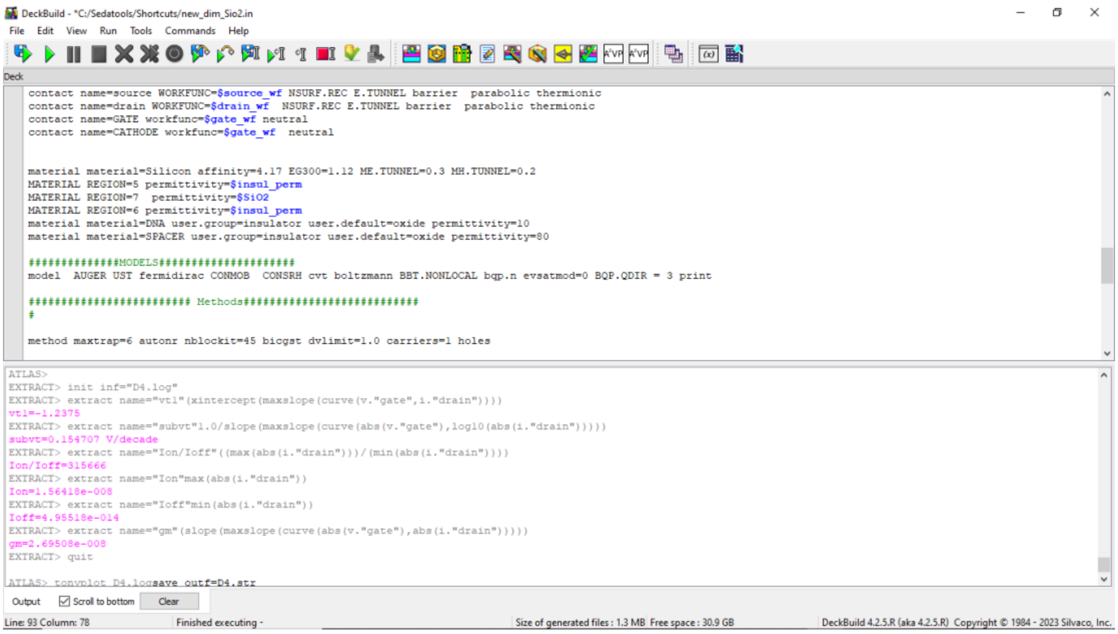


Fig 4.15: Simulated results for k=8,9 for p type



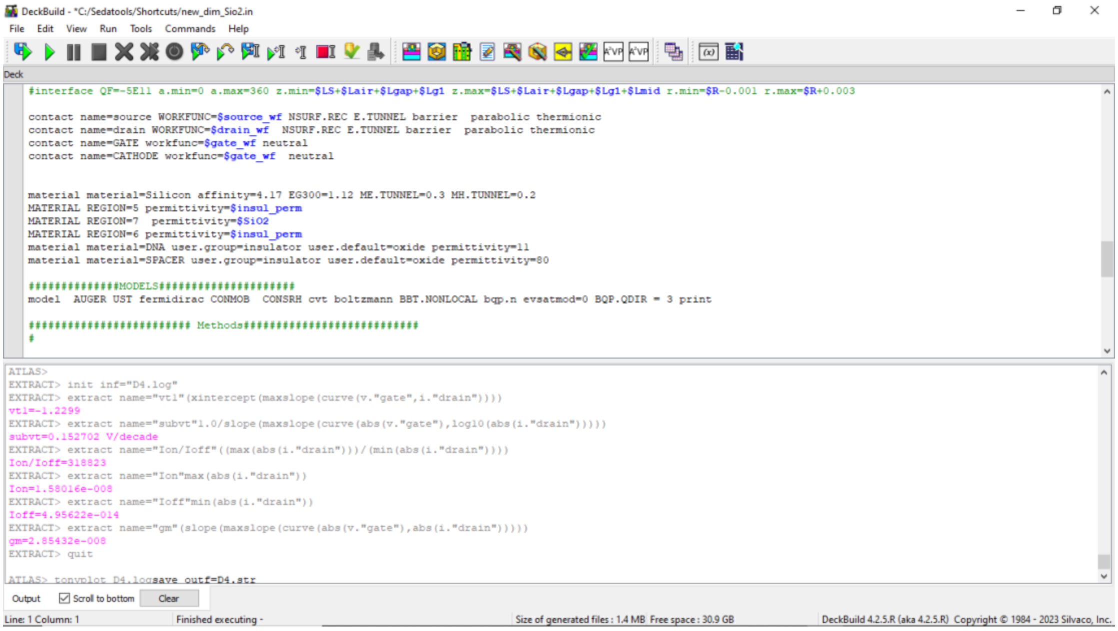


Fig 4.16: Simulated results for k=10,11 for p type

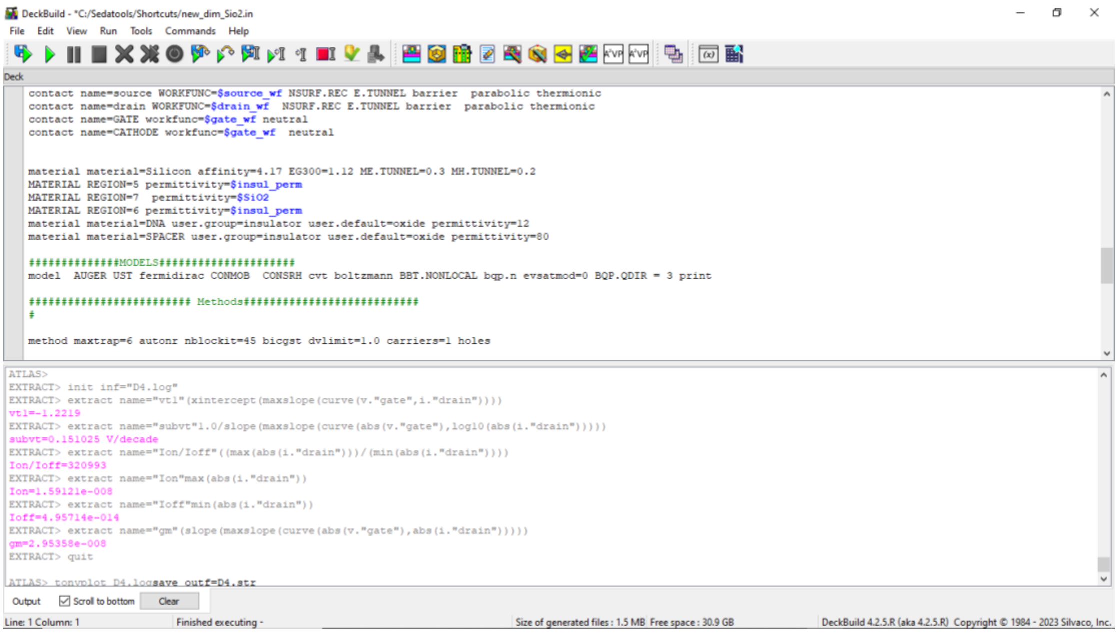


Fig 4.17: Simulated results for k=12 for p type

Energy Band Diagram:

1. EBD for n type in off state:

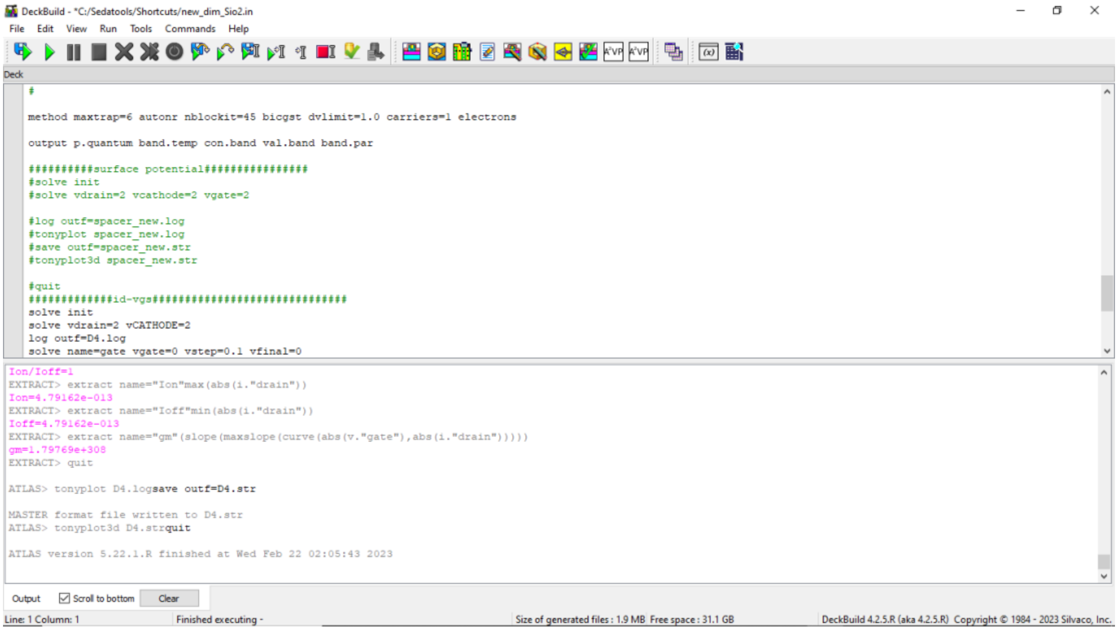


Fig 4.18: Simulated results for n mode in Off state

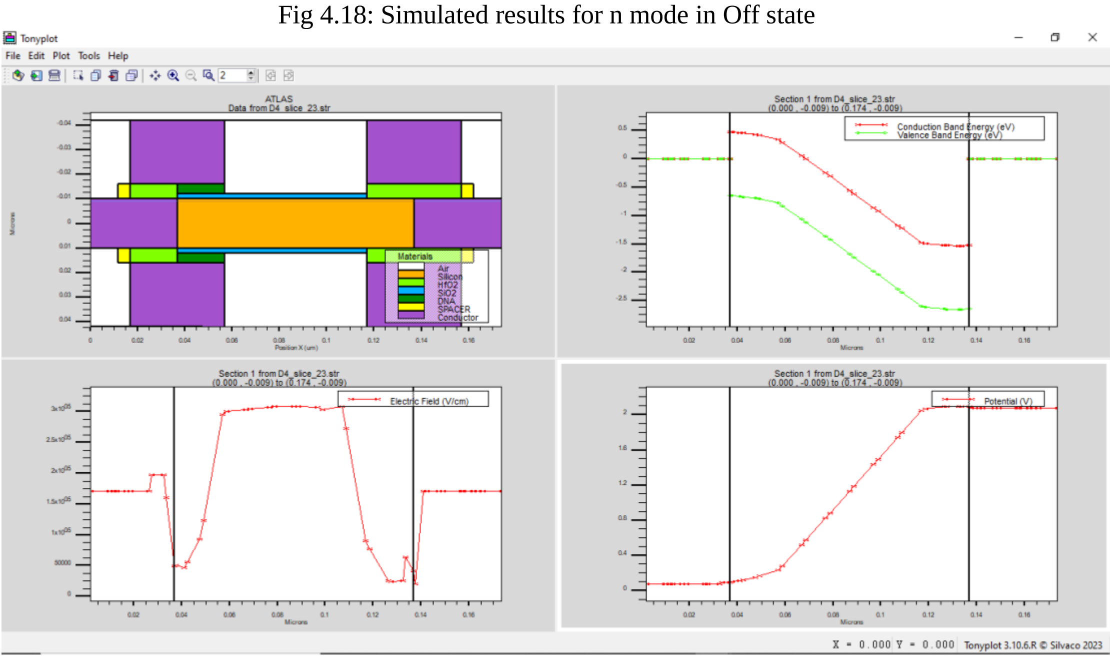


Fig 4.19: EBD of n type in OFF state

2. EBD for n type in on state:

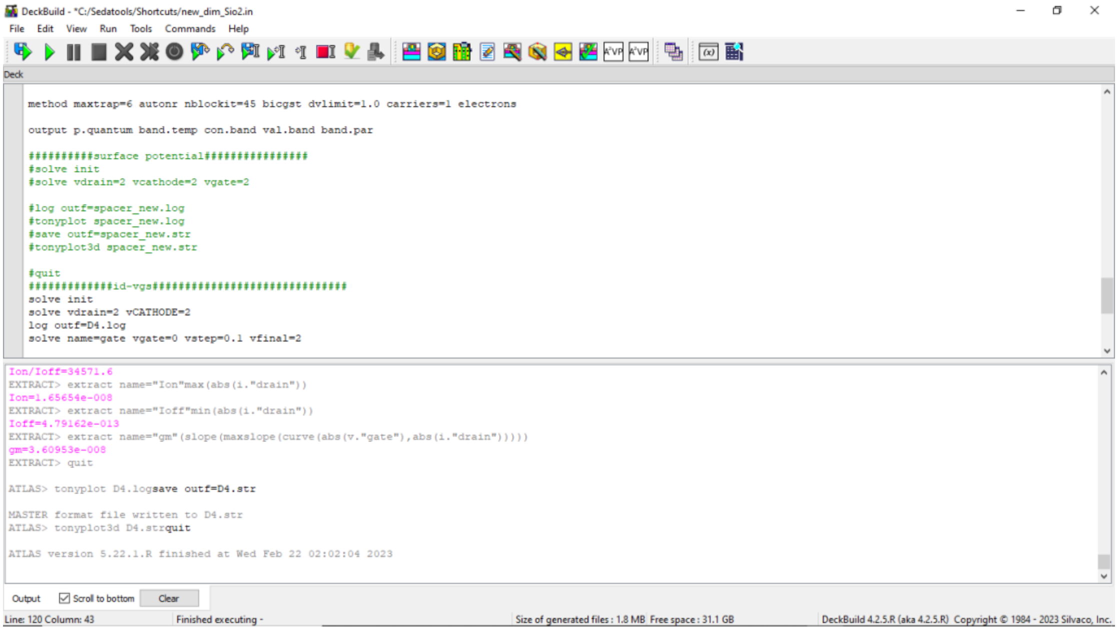


Fig 4.20: Simulated results for n mode in ON state

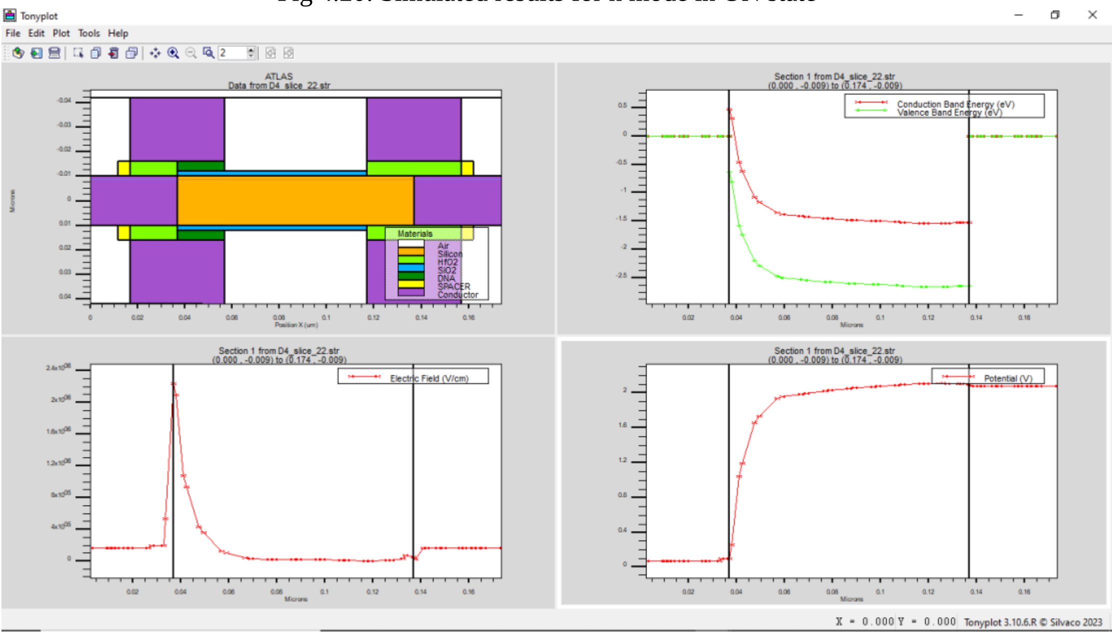


Fig 4.21: EBD of n type in ON state

3. EBD of p type in the off state:

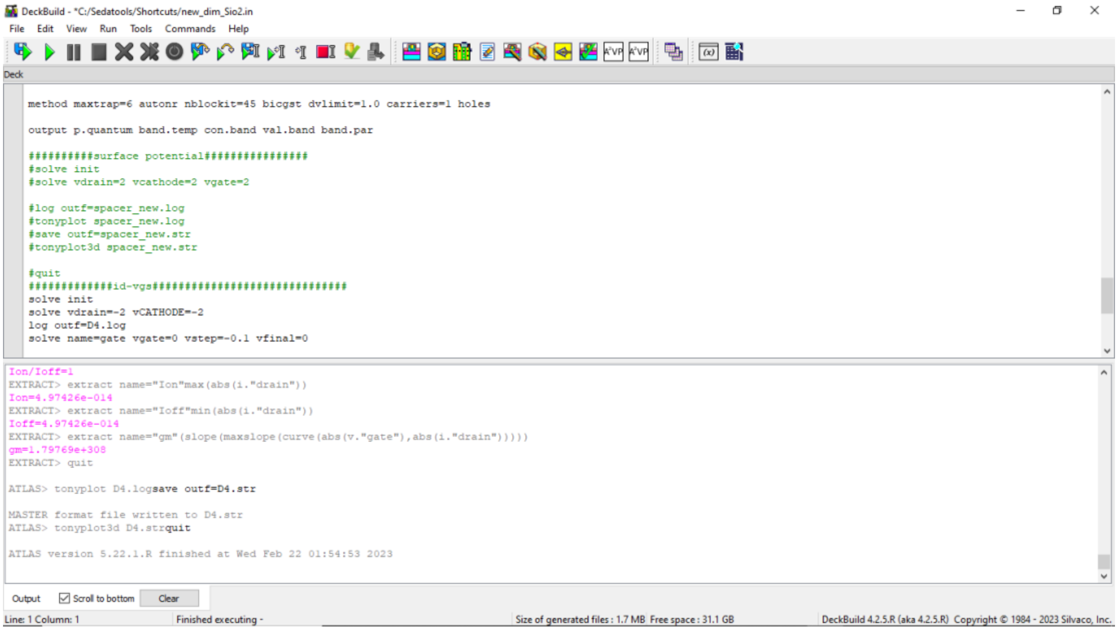


Fig 4.22: Simulated results for p mode in Off state

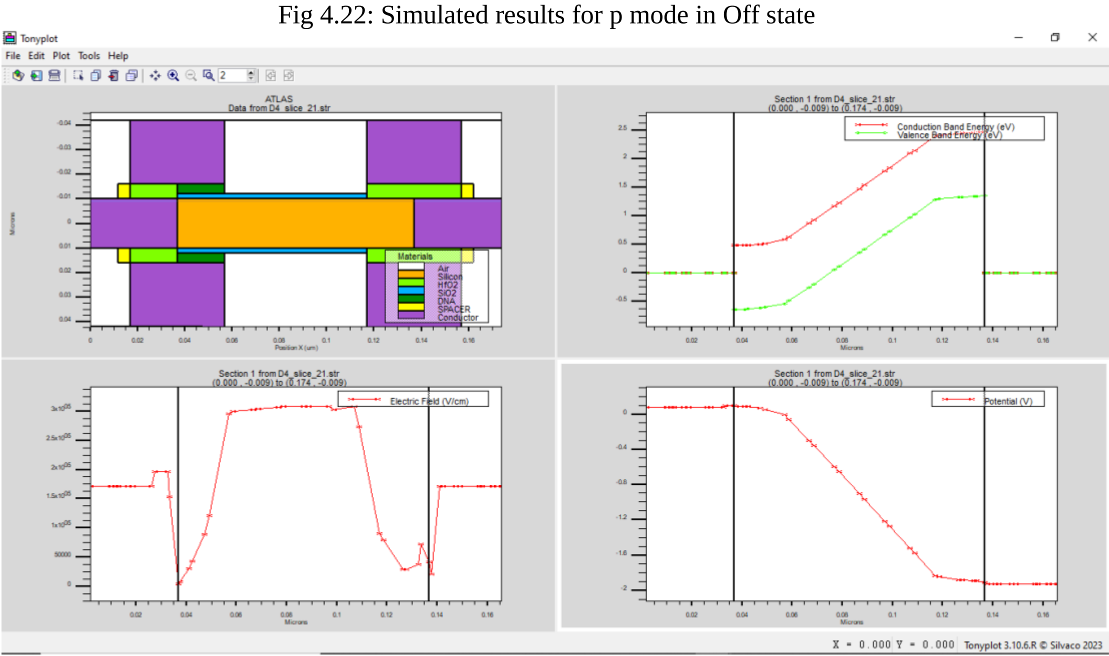


Fig 4.23: EBD of p mode in ON state

4. EBD of p type in on state:

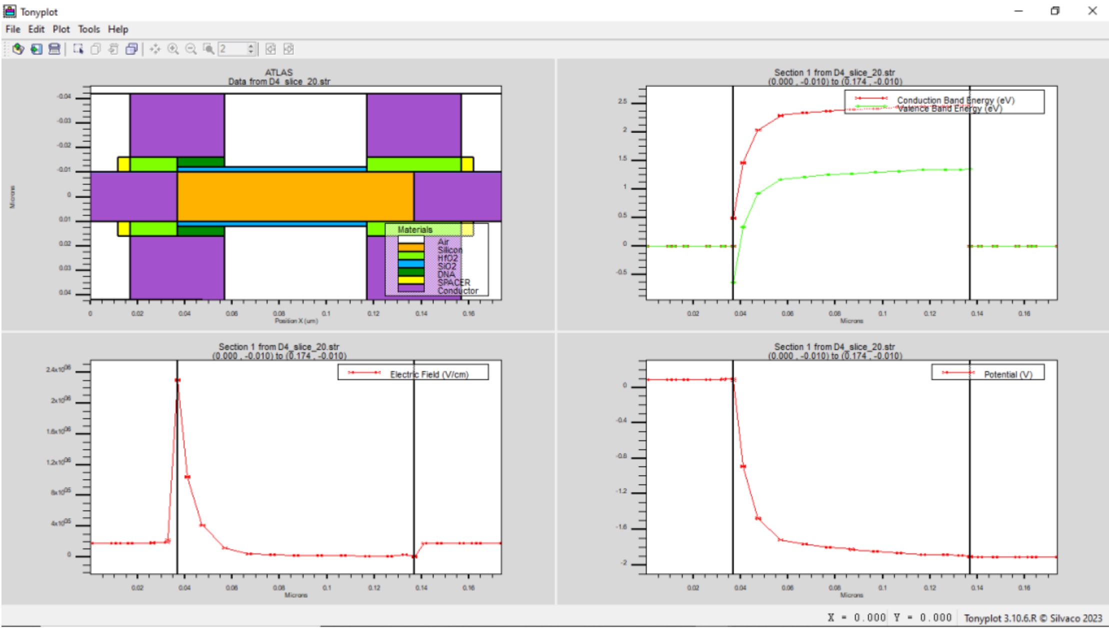


Fig 4.24: EBD of p mode in ON state

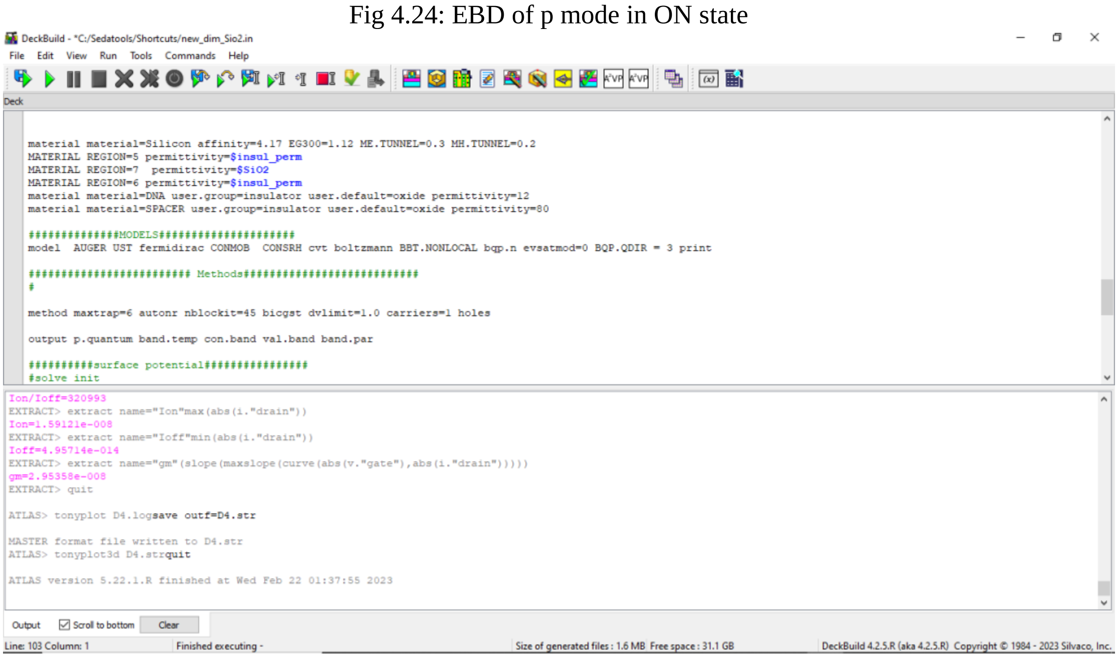


Fig 4.25: Simulated results for p mode in ON state

n type with Nf= 5 e12

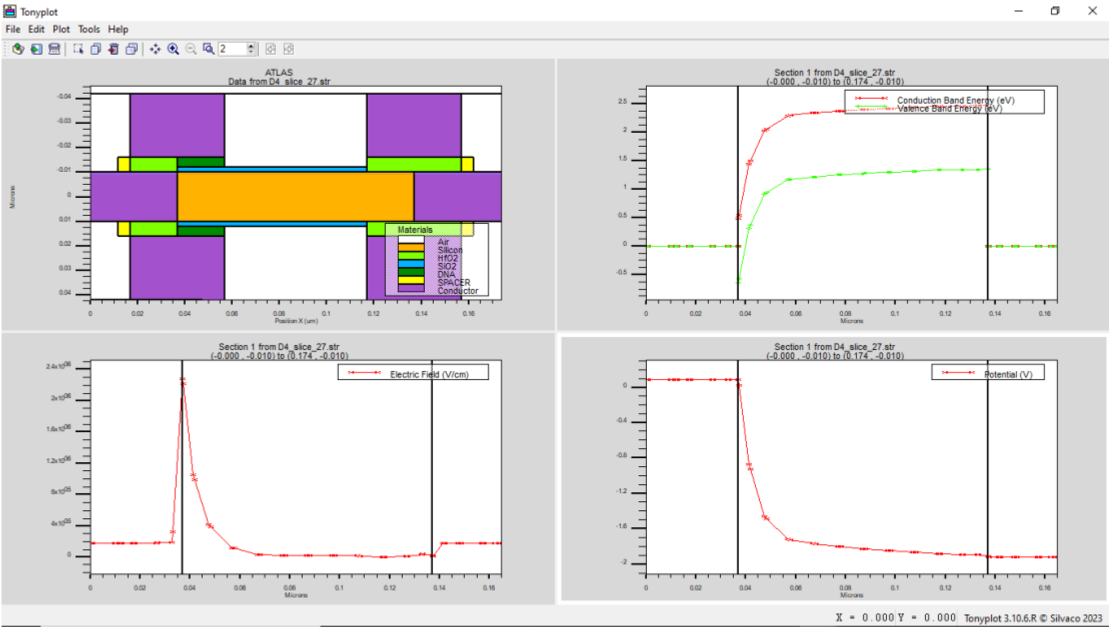


Fig 4.26: EBD for n type with Nf = 5 e12

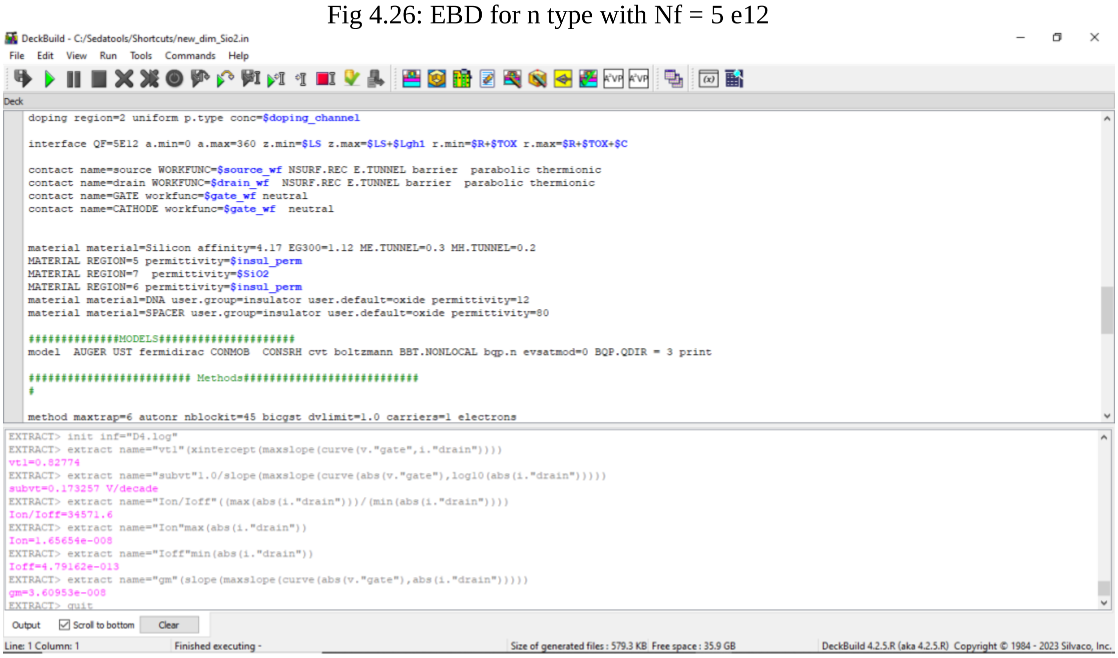


Fig 4.27: Simulated results of n type for Nf = 5 e12

p type with Nf= 5 e12:

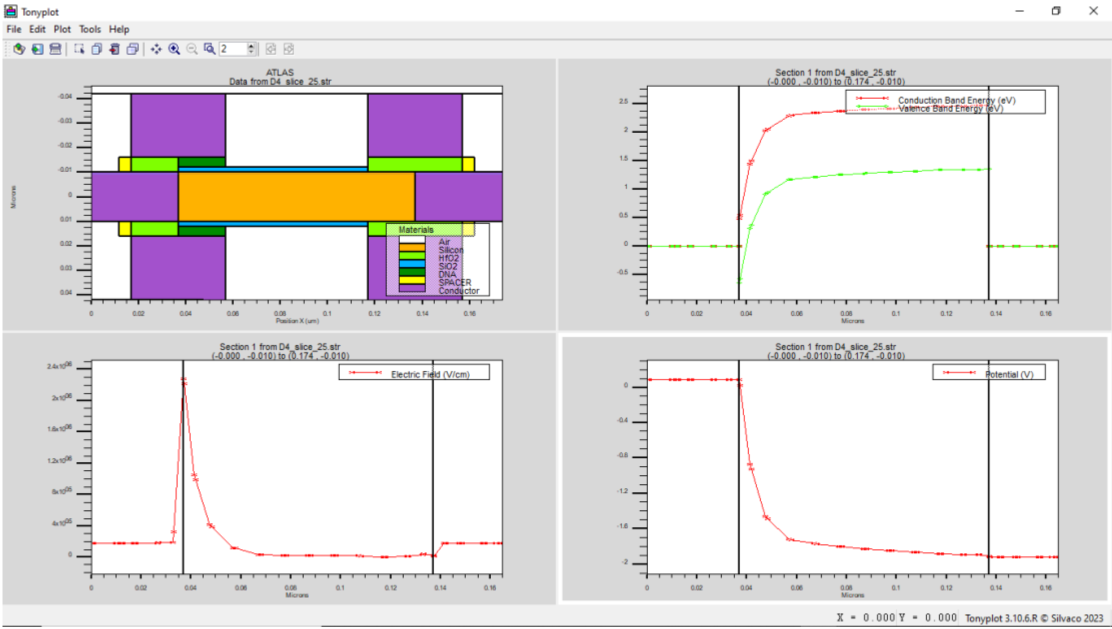


Fig 4.28: EBD for p mode with Nf = 5 e12

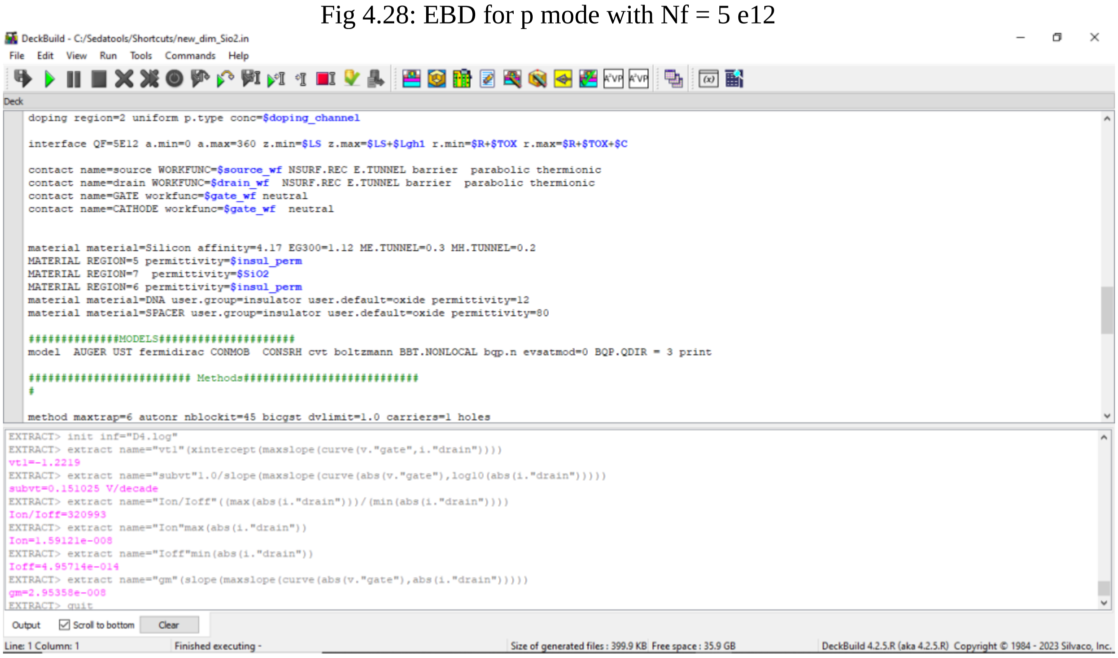


Fig 4.29: Simulated results for p mode with Nf = 5 e12

n type with Nf= -5 e12

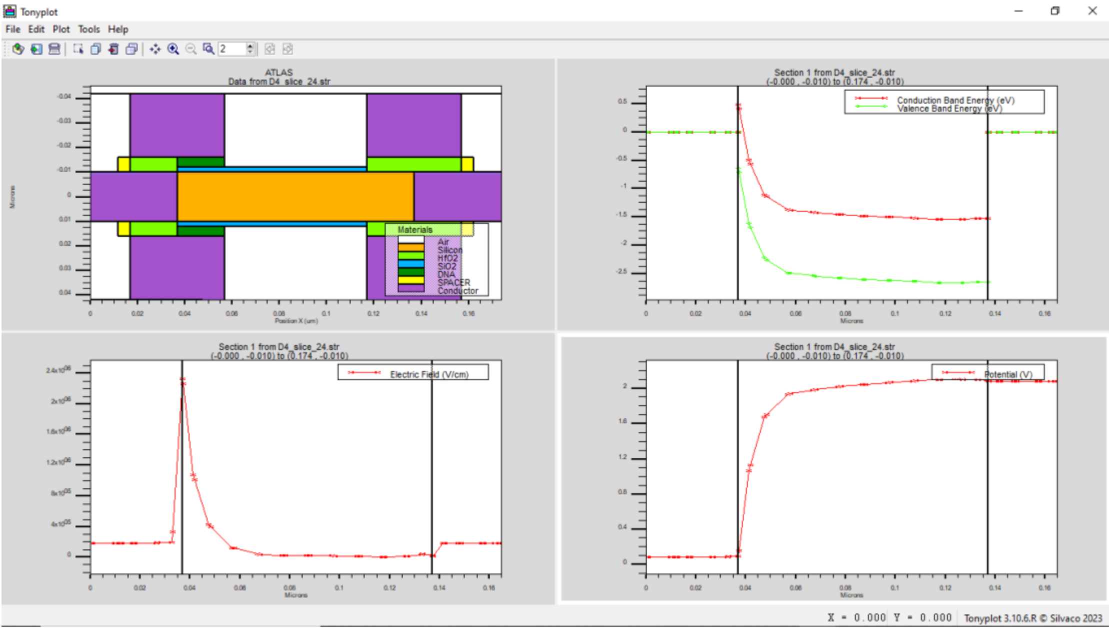


Fig 4.30: EBD for n mode with Nf = -5 e12

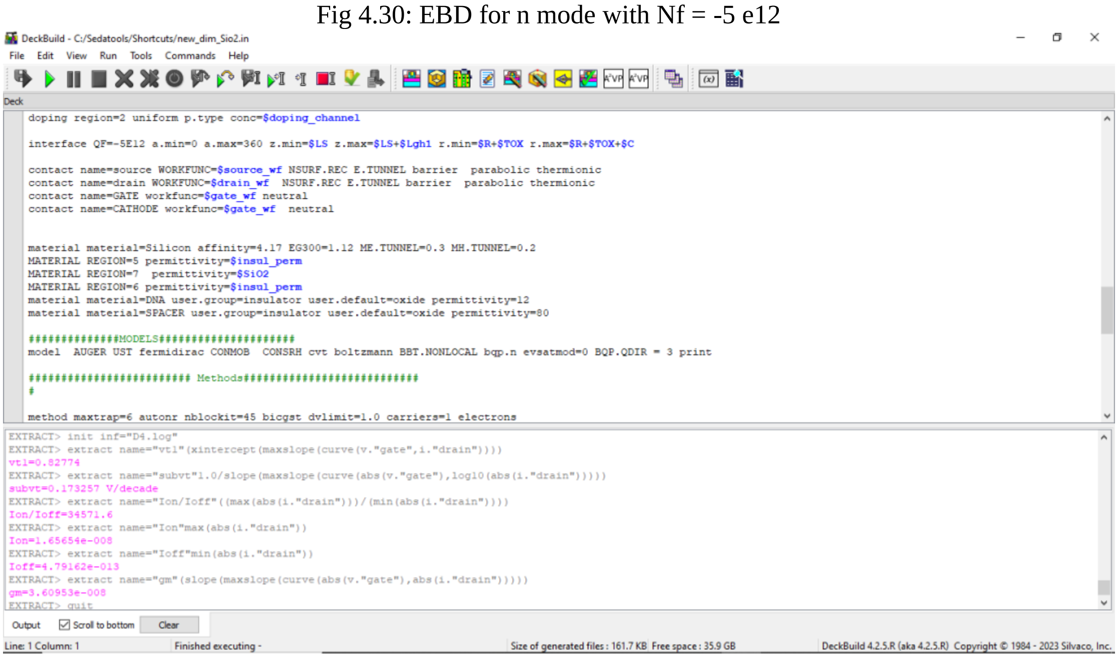


Fig 4.31: Simulated results for n mode with Nf = -5 e12

p type with Nf = -5 e12:

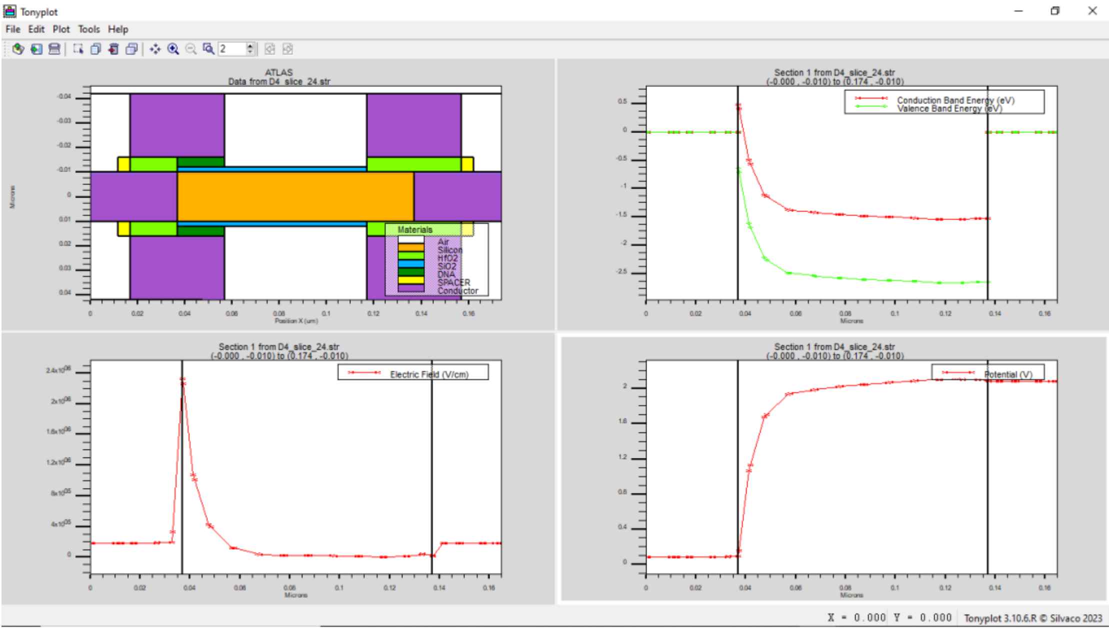


Fig 4.32: EBD for p mode with Nf = -5 e12

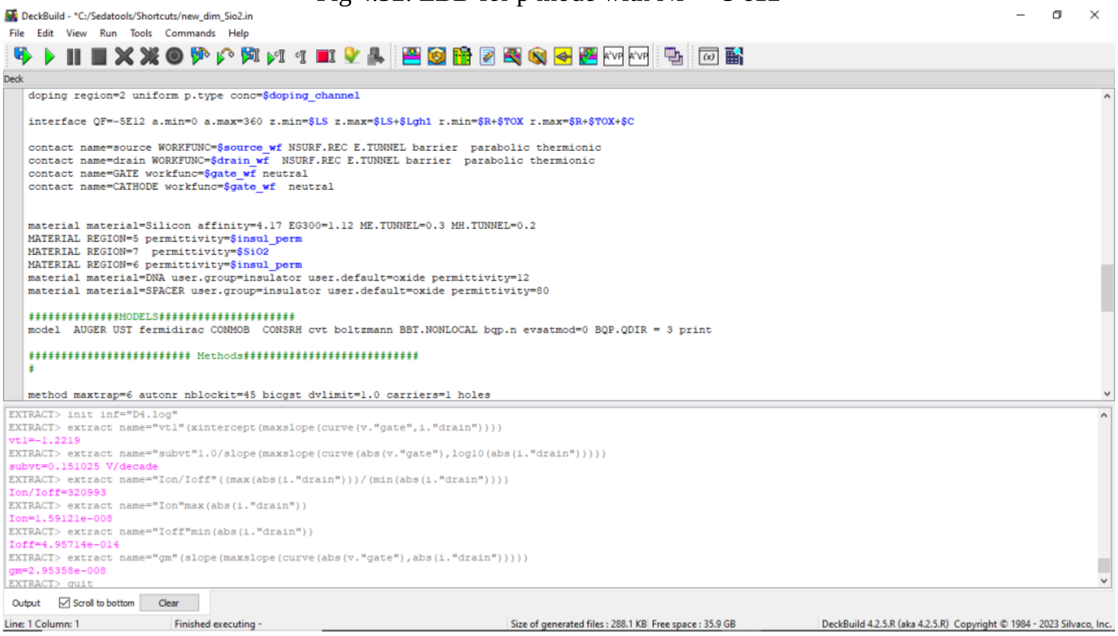


Fig 4.33: Simulated results for p mode with Nf = -5 e12

4.5 Sensitivity calculation for n and p type:

Sensitivity= [Vt(k=1) -Vt(k>1)]/Vt(k=1)

Applying this formula in n type simulated for different k values we have the table below 4.3. And for p type we have table 4.4.

For k=1, the threshold voltage we found out was 1.48 V for n type.

For k=1, the threshold voltage we found out was -2.20 V for p type

Table 4.3: Sensitivity calculation for n type for varying k

Varying k for n type	Vt	Sensitivity
K=2	1.17935	20.3%
K=3	1.06214	28.2%
K=4	0.991039	33.03%
K=5	0.946984	36.01%
K=6	0.913011	38.3%
K=7	0.896655	39.41%
K=8	0.878891	40.6%
K=9	0.860535	41.86%
K=10	0.842132	43.2%
K=11	0.832039	43.8%
K=12	0.827807	44.07%

Table 4.4: Sensitivity calculation for p type for varying k

Varying k for p type	Vt	Sensitivity
K=2	-1.73068	21.42%
K=3	-1.55278	29.5%
K=4	-1.45321	34.02%
K=5	-1.39104	36.8%
K=6	-1.33914	39.2%
K=7	-1.31155	40.41%
K=8	-1.28903	41.48%
K=9	-1.26434	42.6%
K=10	-1.23844	43.77%
K=11	-1.23005	44.15%
K=12	-1.22222	44.5%

Conclusion

The reconfigurable nanowire FET has been implemented as a biosensor and there been improved sensitivity noticed from the reference paper. The sensitivity for n type has been found quite improved with values for k=2,4,6,8, etc and the sensitivity for p type is also quite promising with values for k=2,4,6,8,etc. Thus the required result for improved sensitivity for neutral biomolecules have been established using threshold voltage for calculation with the help of SILVACO TCAD tool for device modeling.

References

1. C. Navarro, S. Barraud, S. Martinie, J. Lacord, M. . -A. Jaud and M. Vinet, "Reconfigurable field effect transistor for advanced CMOS: A comparison with FDSOI devices," 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), 2016, pp. 5-8, doi: 10.1109/ULIS.2016.7440038.
2. M.p. Lepselter and S.M. Sze, "S-IGFET: An insulated-gate field-effect transistor using Schohttky barrier contacts for source and drain", *Proc. IEEE*, vol. 56, no. 8, pp. 1400-1968.
3. L. Gaben et al., "Stacked-Nanowire and FinFET transistors: guidelines for the 7nm node", *In proceedings of the 2015 International Conference on Solid State Devices and Materials*.
4. Asenov, A. Huang, Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulated study, Electron Devices, IEEE Transactions, 45 , Issue: 12
5. Mikolajick T, Heinzig A, Trommer J, Baldauf T Weber WM. The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. *Semicond. Sci. Technol.* 2017; 32 (4): 043001. https://doi.org/10.1088/1361-6641/aa5581. doi:10.1088/1361-6641/aa5581.
6. André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M. Weber *Nano Letters* 2012 *12* (1), 119-124DOI: 10.1021/nl203094h
7. J. Appenzeller, M. Radosavljević, J. Knoch, and Ph. Avouris Phys. Rev. Lett. 92, 048301 – Published 28 January 2004
8. Trommer J *et al.* 2014 Material prospects of reconfigurable transistor (RFETs)—from silicon to germanium nanowires *MRS Proc.* 1659 225–30
9. Priyanka Saha, Dinesh Kumar Dash, Subir Kumar Sarkar,
10. Nanowire reconfigurable FET as biosensor: Based on dielectric modulation approach, Solid-State Electronics, Volume 161, 2019, 107637, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2019.107637.

11. D'Agostino F, Quercia D. Introduction to VLSI design (EECS 467), Short-Channel Effects in MOSFETs, December 11th (2000).
12. D. Rechem, S. Latreche The effect of short channel on nanoscale SOI MOSFETs Afr Phys Rev, 2 (38) (2008), pp. 80-81
13. A.S. Verhulst, B. Sorée, D. Leonelli, W.G. Vandenberghe, G. Groeseneken Modeling the single-gate, double-gate, and gateall- around tunnel field-effect transistor
14. Pritha Banerjee, Priyanka Saha, Subir Kumar Sarkar Analytical modelling and performance analysis of gate engineered tri-gate SON MOSFET
15. Maik Simon, Andr'e Heinzig, Jens Trommer, Tim Baldauf, Thomas Mikolajic k, Walter M. Weber Top-down technology for reconfigurable nanowire FETs with symmetric on-currents
16. Ghader Darbandy, Martin Claus, Michael Schroter High-performance reconfigurable si nanowire field-effect transistor based on simplified device design IEEE Trans Nanotechnol, 15 (2) (2016)
17. W.M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, T. MikolajickRec onfigurable nanowire electronic—a review Solid-State Electron, 102 (2014), pp. 12-24
18. A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, W.M. Weber Reconfigurable silicon nanowire transistors Nano Lett, 12 (1) (2011), pp. 119-124
19. J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, W.M. Weber Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors IEEE Trans Nanotechnology, 14 (4) (2015), pp. 689-698
20. A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, W.M. Weber Reconfigurable silicon nanowire transistors Nano Lett., 12 (1) (2012), pp. 119-124
21. D. Martin, *et al.*Direct probing of Schottky barriers in Si nanowire Schottky barrier field effect transistors Phys Rev Lett, 107 (21) (2011) pp. 216807–1–216807-5

22. A. Bhattacharjee, S. Dasgupta Impact of gate/spacer-channel underlap, gate oxide EOT, and scaling on the device characteristics of a DG-RFET IEEE Trans Electron Devices, 64 (8) (2017), pp. 3063-3070
23. A. Chen, X.S. Hu, Y. Jin, M. Niemier, X. Yin Using emerging technologies for hardware security beyond PUFs Proc. 2016 Design, Autom. Test Eur. Conf. Exhib. (2016), pp. 1544-1549
24. B. Buvaneswari, N.B. Balamurugan 2D analytical modeling and simulated of dual material DG MOSFET for biosensing application Int J Electron Commun (AEÜ), 99 (2019), pp. 193-200
25. H. Im, X.-J. Huang, B. Gu, Y.-K. Choi A dielectric-modulated field-effect transistor for biosensing Nature Nanotechnol, 2 (7) (2007), pp. 430-434
26. B. Gu, T.J. Park, J.-H. Ahn, X.-J. Huang, S.Y. Lee, Y.-K. Choi Nanogap field-effect transistor biosensors for electrical detection of avian influenza Small, 5 (21) (2009), pp. 2407-2412
27. J.-Y. Kim, J.-H. Ahn, D.-I. Moon, T.J. Park, S.Y. Lee, Y.-K. Choi Multiplex electrical detection of avian influenza and human immunodeficiency virus with an underlap-embedded silicon nanowire field-effect transistor Biosens Bioelectron, 55 (2014), pp. 162-167
28. Ajay, Rakhi Narang, Manoj Saxena, Mridula Gupta Drain current model of a four-gate dielectric modulated MOSFET for application as a biosensor IEEE Trans Electron Devices, 62 (8) (2015)
29. Ajay, Rakhi Narang, Manoj Saxena, Mridula Gupta Modeling and simulated investigation of sensitivity of symmetric split gate junctionless FET for biosensing application IEEE Sens J, 17 (15) (2017)
30. J.M. Kinsella, A. Ivanisevic Biosensing: taking charge of biomolecules Nature Nanotechnol, 2 (2007), pp. 596-597
31. Kalra, Sumeet, Mamidala Jagadesh Kumar and Anuj Dhawan. “Reconfigurable FET Biosensor for a Wide Detection Range and Electrostatically Tunable Sensing Response.” *IEEE Sensors Journal* 20 (2020): 2261-2269.